Chapter 2. Input PFC Circuit

2.1 Introduction

The principle operation of the boost PFC circuit, which is selected for the input PFC of the VSD system, is explained in this chapter. The design and loss equations to calculate main power component values in the boost PFC circuit are derived. The predicted efficiency of the boost PFC preregulator is obtained with derived analytical equations and compared with experimental results. The harmonic contents in the input current of the boost PFC circuit is compared with the modified IEC 1000-3-2 standard for a 120V ac source to validate the effects of the PFC circuit.

In a VSD, the ac utility input voltage is converted to dc with a rectifier circuit, as shown in Figure 1.2. This circuit has the advantages of simplicity, low cost, high reliability, and no need of control. But, it also has the disadvantages of low PF due to the presence of rich harmonics and high peak current magnitude, as shown in Figures 2.1(i) and (ii). The input current and voltage waveforms in Figure 2.1(i) are obtained by PSpice simulation of Figure 1.4 and normalized to the peak values. The harmonic spectrum of the input current is shown in Figure 2.1(ii). Their magnitudes are normalized to the fundamental component, that is 60Hz in this case.

The input circuit of an off-line VSD consists of rectifier diodes to convert ac into pulsating dc and filter capacitors to smooth the pulsating dc voltage as shown in Figure 1.2. This input circuitry presents rich harmonic currents to ac power systems, which is quite different from motor loads because it appears as a nonlinear load to ac power systems. In the input circuit, ac current pulses occur because the filter capacitor remains charged to near the peak value of the ac input voltage. During most of the input voltage half cycle, the rectifier diodes remain reverse biased, thus no current flows. Because filter capacitors partly discharge during each half cycle, the input voltage exceeds the capacitor voltage for a short time near the peak value of the input voltage. As the input voltage surpasses the capacitor voltage, the input current begins to flow abruptly into the capacitor. After the capacitor is charged to near the peak value of the input voltage, and the input voltage begins to decrease, the input current falls to zero.

The input current pulse has a high peak value and is extremely distorted with respect to a sinusoidal waveform [23, 36, 37]. It contains high amounts of harmonic components as illustrated in Figure 2.1(ii). These harmonic currents add current drain from the ac power line, imposing the need for higher wiring capacity and contributing to the resultant low power factor. Any harmonic current, except the fundamental component, do not deliver power to the load. However, these harmonic currents increase total line current more than actually required by the user. As a result, it requires higher current ratings of wires and circuit breakers in the utility resulting in additional installation cost to the utility company. Also it causes overheating of power lines and distribution transformers. Under extreme conditions, other sensitive electronic equipments connected to the same power line are affected by EMI noise.

As required by various standards, the line harmonics produced by a VSD must be below certain limits, requiring higher input PF. High PF is desirable to both the user and the utility company because it is possible to get maximum power from an ac service outlet and to utilize the generated power efficiently and cleanly. It is possible to reduce wiring and power transformer losses in the utility network with a high PF. With increasing demand for more power and better

power quality from a standard power line, the PFC circuit becomes an integral part of a VSD in the near future.

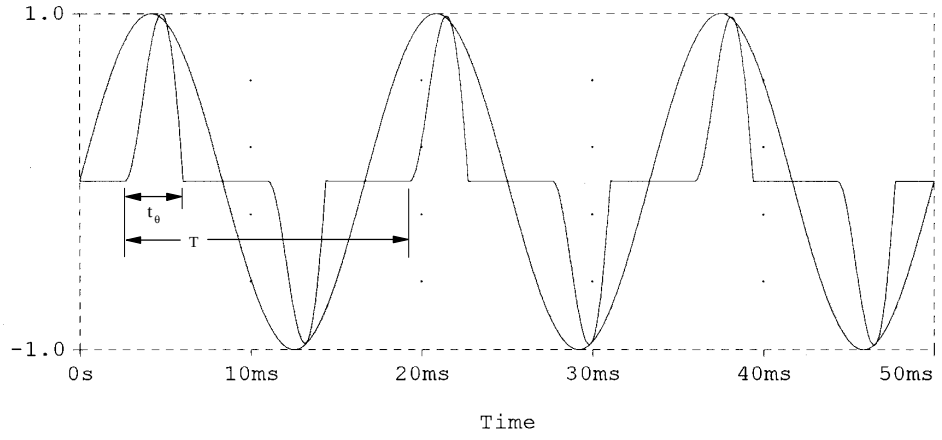
The input power factor (PF) is defined as the ratio of the real power over apparent power as,

$$\text{Power Factor} = \frac{\text{Real Power}}{\text{Apparent Power}}$$

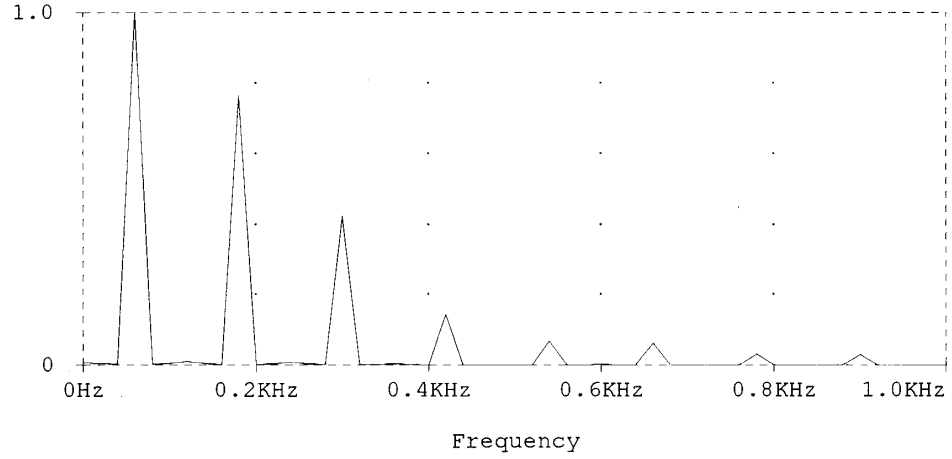
$$= \frac{V_{rms} \cdot I_1 \cdot \cos\phi}{V_{rms} \cdot I_{rms}}$$

$$= \frac{I_1}{I_{rms}} \cdot \cos\phi$$

$$= K_d \cdot K_\phi . \tag{2.1}$$



(i) Normalized input ac voltage, v_s and current, i_s.



(ii) Normalized harmonic spectrum of current i_s.

Figure 2.1 An example of current harmonic contents in diode rectifier circuit with capacitor.

where V_{rms} is the ac input rms voltage, I_{rms} is the ac input rms current, I_1 is the fundamental component of I_{rms} and $cos\phi$ is the phase angle between input ac voltage and the fundamental current.

If the input ac voltage is assumed to be a pure sinusoid, the PF becomes the product of distortion factor, K_d, and displacement factor, K_ϕ as shown in equation (2.1). K_d is the ratio of the fundamental rms current, I_{rms}^1 to total rms current, I_{rms}. K_d is regulated by IEC 1000-3-2 for small power levels and by IEEE Std 519-1992 for higher power levels. K_ϕ is the cosine of the phase angle between input ac voltage and the fundamental current, which is regulated by utility companies.

The input rms current, I_{rms} in a diode rectifier circuit with capacitor which is shown in Figure 2.1(i) is expressed as,

$$I_{rms} = \sqrt{I_1^2 + I_3^2 + \cdots + I_n^2} \text{ , A.} \tag{2.2}$$

where I_n is the n^{th} rms harmonic current. The expression of the n^{th} harmonic current, using the Fourier transformation of the impulse current in Figure 2.1(i), is [23]:

$$I_n = \frac{8\alpha K}{\pi} \cdot \sum_{n=1,3,5\cdots}^{\infty} \left[\frac{cos n\alpha\pi}{1 - (n\alpha\pi)^2} \right] \cdot cos\, n\omega t \text{ , A.} \tag{2.3}$$

where,

$$\alpha = \frac{t_\theta}{T}. \tag{2.4}$$

t_θ is the duration of current conduction, T is the period of line frequency, K is the crest factor of the current and n is the harmonic order. The even harmonics are not included in equation (2.3) because the waveshape of both the positive and negative half periods are equal.

The modified IEC 1000-3-2 Class A and D input harmonic current limits for a 120V ac source summarized in Table 1.2 are utilized as the reference to validate the effectiveness of PFC circuits in VSD systems.

2.2 Principle of Operation of the Boost PFC Circuit

PFCs reshape the distorted input current waveform to approximate a sinusoidal current that is in phase with the input voltage. There are several effective techniques for achieving a sinusoidal input current waveform with low distortion. Two typical techniques for PFCs are passive correction and active correction. In this study, only the single-phase input circuitry is considered.

Passive PFC techniques [36, 37] shape the input current waveform by using a passive input filter consisting of inductors and capacitors. Because it operates at the line frequency of 60Hz, passive filters require relatively large fixed-value inductors and capacitors to reduce the low frequency harmonic currents. These filters use resonant pass or resonant trap circuits sensitive to both frequency and load. It is difficult to achieve near unity power factor with passive filters.

Also, very large currents may circulate in the filter. However the passive filter is an effective PFC solution in cases where the line frequency, line voltage and load are relatively constant.

An active PFC performs much better and is significantly smaller and lighter than the passive PFC circuit. The active PFC circuits operate at a higher switching frequency than the line frequency to allow a large reduction in the size and cost of passive filter elements. Their function includes active waveshaping of the input current, filtering of the high frequency switching, feedback sensing of the source current for waveform control and feedback control to regulate output voltage.

Buck, boost, flyback and other converter topologies are used for the active PFC circuits. The boost circuit-based PFC topology is the most popular [38-41] and is employed in this study. The boost PFC circuit is an economical solution to comply with the regulations. It can be implemented with a dedicated single chip controller, making the circuit relatively simple with a minimum number of components. The boost inductor in the boost PFC circuit is in series with the ac power line. Therefore the input current does not pulsate minimizing conducted EMI at the line. This allows the size of the EMI filter and the conductors in the input circuit to be reduced. This topology inherently accepts a wide input voltage range without an input voltage selector switch. For example, the Unitrode UC3854 PF controller chip accepts an input voltage of 75 - 275V ac and a frequency of 50 - 400Hz [39]. It cannot limit overcurrent at start-up or fault conditions since there is no switch between the line and the output. The output voltage of a boost PFC circuit should be higher than the peak value of the maximum input voltage. Although this is a simple topology, it must be designed to handle the same power as the main power converter. Only the single-phase boost PFC circuit operating in the continuous inductor current mode is discussed in this study.

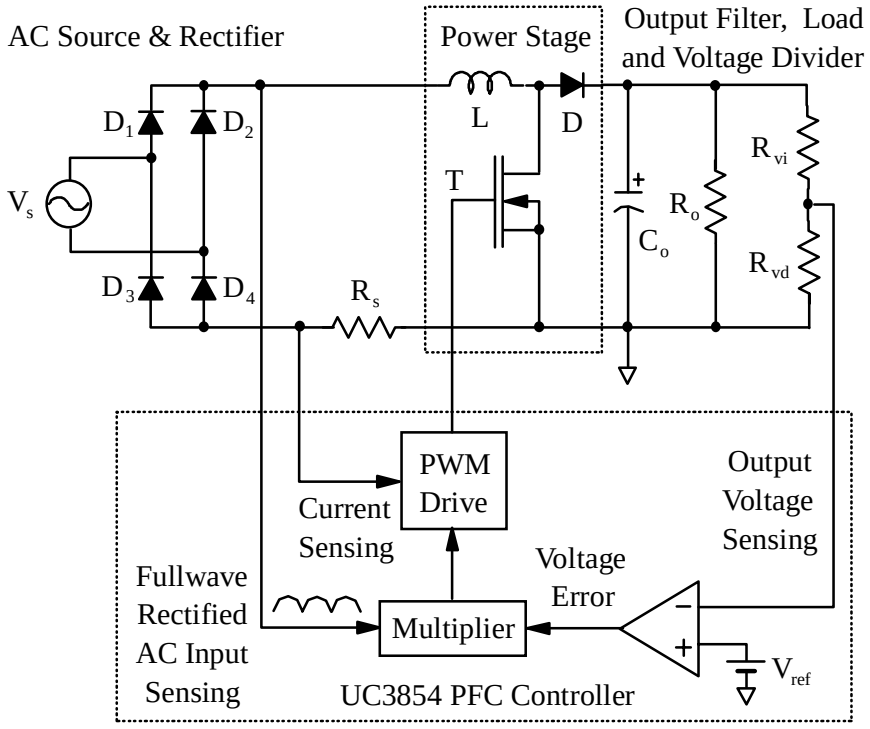


Figure 2.2 A simplified block diagram of a single-phase boost PFC circuit.

The simplified block diagram of the boost PFC circuit is shown in Figure 2.2 [39, 70]. This circuit has two control loops: one is the fast acting internal current loop. It defines the input current shape to be sinusoidal and forces it in phase with the input voltage. The other is the external voltage loop which regulates the output dc voltage. The voltage loop should not react to the 120Hz rectified mains variations, so its bandwidth is between 10 to 20Hz. The current loop usually has a bandwidth frequency of less than one tenth of the switching frequency.

The principle operation of boost PFC is as follows [39]: the rectified sinusoidal input voltage goes to a multiplier circuit, providing a current reference to the multiplier and a feedforward signal proportional to the rms value of the line voltage. The filtered dc output voltage of boost PFC is compared to a reference voltage, V_{ref} and amplified. The error amplifier senses the variations between the output voltage and the fixed dc reference voltage. The error signal is then applied to the multiplier. The multiplier's output follows the shape of the input ac voltage, with an average value inversely proportional to the rms value of the ac input voltage. This signal is compared to the current signal sensed by R_s in a pulsewidth modulation (PWM) circuit. The inductor current waveform follows the shape of the rectified ac line voltage. The gate drive signal controls the inductor current amplitude and maintains a constant output voltage.

2.3 Design of the Boost PFC Preregulator

The voltage and current ratings of the switch, diodes and passive components for the boost PFC preregulator are discussed in this section [39, 62, 63]. Based on the obtained ratings for major power components, the loss equations are derived.

The PFC stage is at least rated to the maximum input power rating of the VSD system given by,

$$P_f(max) = \frac{P_o(max)}{(\eta_m \cdot \eta_c)} \text{ , W.} \tag{2.5}$$

where $P_f(max)$ is the maximum power rating of the PFC stage, $P_o(max)$ is the maximum output power of the VSD system, η_m is the efficiency of the motor and η_c is the efficiency of the corresponding converter or inverter.

Input Rectifier Bridge Diode

The peak input current occurs at the minimum input line voltage with the maximum output power. The peak input current is expressed as,

$$I_{in}(pk) = \frac{\sqrt{2} \cdot P_f(max)}{\eta_f \cdot V_{in}(min)} \text{ , A.} \tag{2.6}$$

where η_f is the efficiency of the PFC stage.

The current flowing through each diode is a half-wave rectified sine wave. Therefore the average current through each diode is

$$I_{bd}(ave) = \frac{2I_{in}(pk)}{\pi} \text{ , A.} \tag{2.7}$$

And the minimum voltage rating for the input rectifier diode is $V_{in}^{pk}(max)$.

Boost Switch

The minimum voltage rating of the boost switch is the output voltage of the PFC stage. The peak current rating is the same value as in the input rectifier bridge diode case shown in equation (2.6). The rms boost switch current is expressed as [40]:

$$I_{sw}(rms) = I_{in}(pk) \cdot \sqrt{\frac{1}{2} - \frac{4V_{in}(pk)}{3\pi V_o}} \text{ , A.} \tag{2.8}$$

Boost Diode

The minimum voltage and current ratings of the boost diode have the same value as in the boost switch case. The rms current of the boost diode is given by [40],

$$I_d(rms) = 2I_{in}(pk) \cdot \sqrt{\frac{V_{in}(pk)}{3\pi V_o}} \text{ , A.} \tag{2.9}$$

Boost Inductor

The inductor value is based on the current ripple in the boost inductor, which is usually chosen as a fraction of $I_{in}(pk)$. The inductance value is expressed as,

$$L = \frac{V_{in}^{pk}(min) \cdot d(max)}{f_s \cdot \Delta i} \text{ , H.} \tag{2.10}$$

where $V_{in}^{pk}(min)$ is the peak minimum input voltage, f_s is the switching frequency, Δi is the ripple current and $d(max)$ is the maximum duty cycle expressed as,

$$d(max) = 1 - \frac{V_{in}^{pk}(min)}{V_o}. \tag{2.11}$$

V_o is the output voltage.

The rms boost inductor current is expressed as [40]:

$$I_L(rms) = \frac{I_{in}(pk)}{\sqrt{2}} \text{ , A.} \tag{2.12}$$

Output Capacitor

The output capacitance for a given output voltage ripple is obtained by integrating the charging current into the capacitor over the entire switching period. The output capacitance is,

$$C_o = \frac{I_o(max)}{4\pi f_l \cdot \Delta V_{or} \cdot \eta_f} \text{ , F.} \tag{2.13}$$

where $I_o(max)$ is the maximum output current, f_l is the line frequency and ΔV_{or} is the output ripple voltage.

Controller Design

The design of the control circuit for the PFC preregulator is not discussed here, since it is found in several references [38-40, 70].

2.4 Efficiency Evaluation for the Boost PFC Preregulator

Efficiency evaluation for the Boost PFC converter is carried out with the estimation of individual losses in the converter. The loss model of the Boost PFC preregulator is obtained by adding up individual loss models of major power components in the converter. The predicted efficiency obtained with the developed loss model is compared with the measured efficiency for validation.

2.4.1 Derivation of Loss Models

The derivation of switching and conduction losses of the major power components in the PFC preregulator is explained in this section. The obtained device ratings and duty cycles in the previous section are summarized in Table 2.1. The loss equations for major power devices are derived based on ratings and duty cycles and listed in Table 2.2 [40].

The switching loss is estimated with considering turn-on and turn-off transients of the switching device since both the maximum voltage and current are applied to the device during these incidents. The switching loss equation is derived under the assumption of the overlapped area by the maximum voltage and current as a triangular waveform.

The conduction loss model for each switch device varies with device type [4]. For the MOSFET device used in the 300W PFC, the drain-to-source on-resistance is considered. The collector-to-emitter saturation voltage of the IGBT device is considered for 2kW PFC. The reverse recovery time is used to estimate the switching loss of the boost diode. The conduction loss of the boost inductor is calculated with a dc equivalent resistance.

All other loss models are derived with measured data and manufacturer's data sheets. The details of major power component values of the prototype PFC preregulators are given in Appendix A.

Table 2.1
Ratings for power components in the boost PFC preregulator.

Device	Duty Cycle	Ratings		
		Voltage	Current	
			Peak	rms
Bridge rectifier	1	$V_{in}(pk)$	$I_{in}(pk)$	$\frac{2I_{in}(pk)}{\pi}$: average
Switch	d	$V_o+\Delta V_{or}$	$I_{in}(pk)$	$I_{in}(pk)\sqrt{\frac{1}{2}-\frac{4V_{in}(pk)}{3\pi V_o}}$
Diode	1-d	$V_o+\Delta V_{or}$	$I_{in}(pk)$	$2I_{in}(pk)\sqrt{\frac{V_{in}(pk)}{3\pi V_o}}$
Inductor	1	$V_o+\Delta V_{or}$	$I_{in}(pk)$	$\frac{I_{in}(pk)}{\sqrt{2}}$

Table 2.2
Losses for power components in the boost PFC preregulator.

Device	Duty cycle	Losses	
		Conduction	Switching
Bridge rectifier	1	$I_{bd}(ave)\cdot V_{fb}$	-
Switch	d	$I_{sw}(rms)\cdot V_{CE}(sat)$ (IGBT) $I_{sw}^2(rms)\cdot R_{ds}(on)$ (MOSFET)	$\frac{1}{2}I_{sw}(rms)V_o f_s(t_r+t_f)$
Diode	1-d	$I_d(rms)\cdot V_f$	$\frac{1}{2}I_d(rms)V_o f_s t_{rr}$
Inductor	1	$\frac{1}{2}I_{in}(pk)^2\cdot R_{dc}$	-

where, V_{fb} = forward voltage drop of the input bridge rectifier, V
$V_{CE}(sat)$ = collector-to-emitter saturation voltage of IGBT switch, V
$R_{ds}(on)$ = drain-to-source on-resistance of MOSFET switch, Ω
t_r = rise time of switch device, s
t_f = fall time of switch device, s
V_f = forward voltage drop of power diode, V
t_{rr} = reverse recovery time of power diode, s
R_{dc} = dc resistance of inductor, Ω

The total loss models for 300W and 2kW PFC preregulators are obtained based on equations listed in Tables 2.1 and 2.2. For the 300W PFC, the loss model is expressed in terms of rated output power, P_{ro} which corresponds to motor speed, *n*.

$$P_{pfc}(300W) = (9.0\times10^{-6})P_{ro}^2 + (2.6\times10^{-2})P_{ro} + 2.3 \text{ , W.} \quad (2.14)$$

It should be mentioned that the constant term in the equation indicates the power supply loss of PFC controller circuit since its power is supplied from the output terminal of the PFC preregulator.

The loss model for the 2kW PFC is derived in terms of the rated output power as:

$$P_{pfc}(2kW) = (0.37\times10^{-6})P_{ro}^2 + (0.04)P_{ro} \text{ , W.} \quad (2.15)$$

The derived loss models are used to estimate the efficiency of the boost PFC preregulator in succeeding sections.

2.4.2 Efficiency Evaluation with Analysis and Experiment

The analytical and experimental procedures to predict and measure the efficiency of the boost PFC preregulator are explained in this section. Two PFC preregulators, a 300W one for 250W SRM-based VSD system and a 2kW one for 1hp DCM- and 4hp PMBDC-based VSD systems with a single-phase 120V ac power source are developed. The loss models for the above mentioned PFC preregulators are derived based on loss equations of key power components in previous section. A MOSFET and an IGBT switching device are used to implement the 300W and 2kW PFC preregulator, respectively. For comparison of both the measured and predicted efficiencies, the output power varies from 100W to 1400W, with 100W increments for the 2kW PFC preregulator. The maximum output power is limited to 1,400W due to the limited range of the instrument. In the case with the 300W PFC, the rated output powers which is the function of the speed of a 250W SRM, is used directly to study the efficiency of the input PF corrected SRM-based VSD system. The speed range varies from 100r/min to 2300r/min with 100r/min increments. This is equivalent to the rated output power varying from 4.17W to 95.83W with increments of 4.17W.

The experimental setup to measure the input and output power of the PFC preregulator is illustrated in Figure 2.3. Efficiency is evaluated as the ratio of the output power over the input power. The measured efficiency, η_m is obtained by following equation:

$$\eta_m = \frac{V_o \cdot I_o}{P_{in}}. \quad (2.16)$$

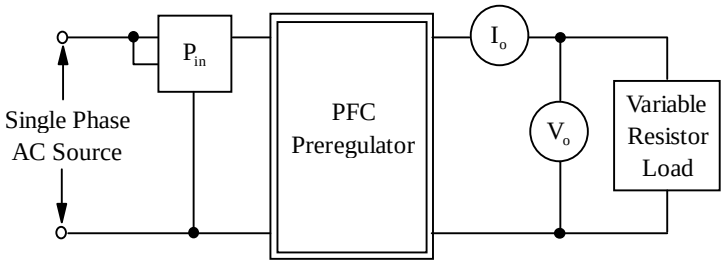


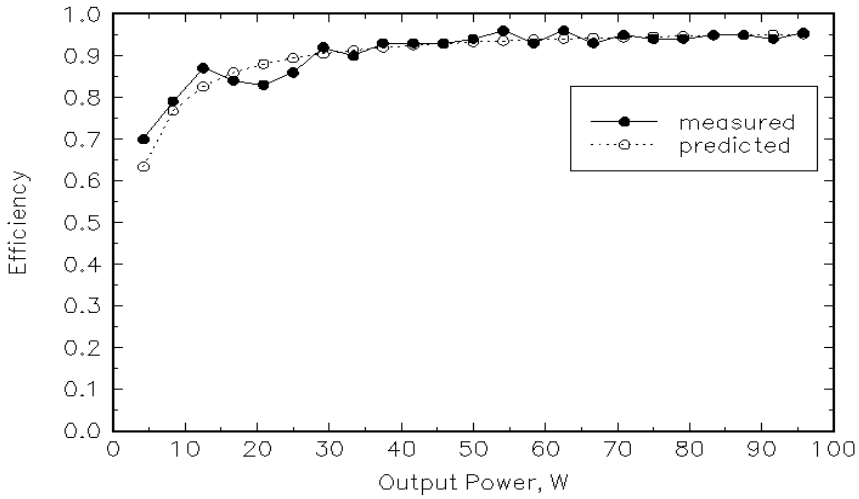
Figure 2.3 Experimental test setup for efficiency measurement of the developed PFC preregulator.

For efficiency prediction, the input power is obtained by adding all the losses of the major power components in the PFC circuit to the rated output power, P_{ro}. The predicted efficiency, η_p is expressed as,

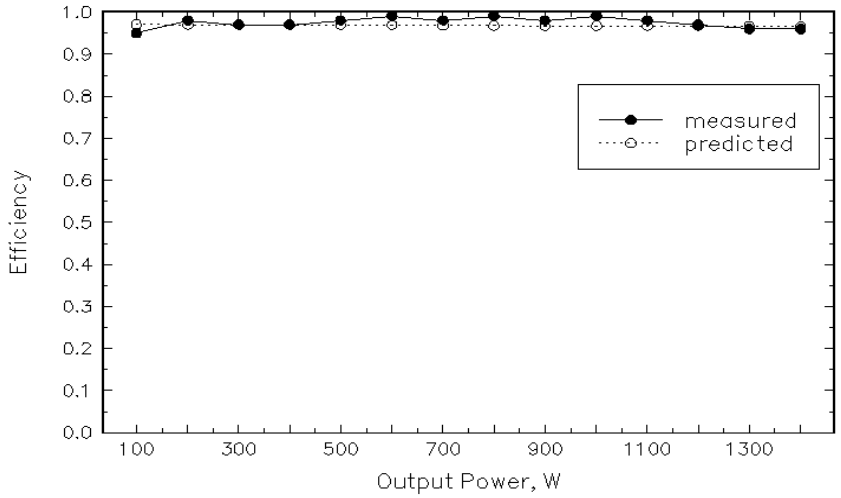
$$\eta_p = \frac{P_{ro}}{P_{ro} + P_{pfc}} . \tag{2.17}$$

where, P_{pfc} indicates the total losses in either the 300W or 2kW PFC preregulators which were derived in previous section.

The measured and predicted efficiencies are compared in Figures 2.4(i) and (ii) for 300W and



(i) 300W PFC preregulator

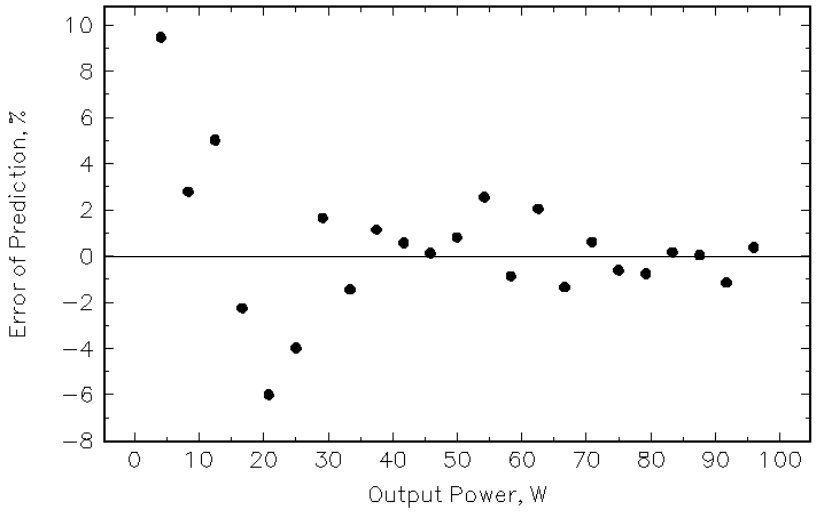


(ii) 2kW PFC preregulator

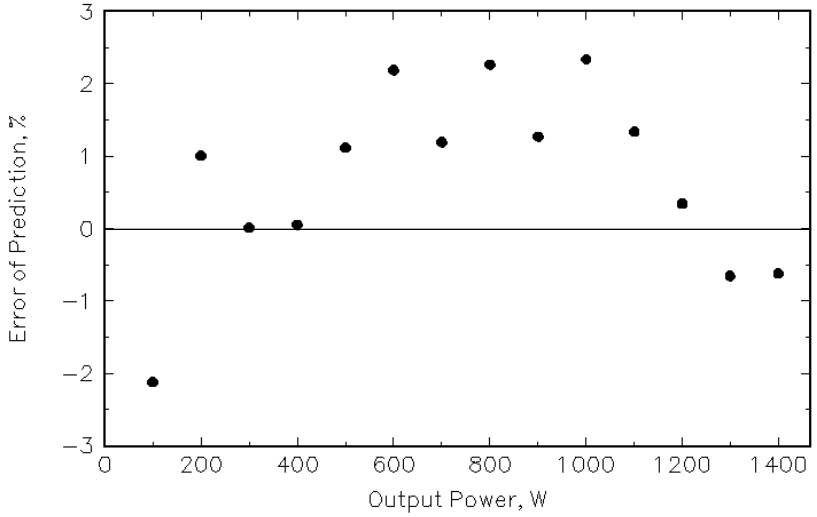
Figure 2.4 Measured and predicted efficiencies versus output power for the developed boost PFC preregulators.

2kW PFC, respectively, to validate the developed loss models. The predicted efficiency for 300W PFC preregulator is obtained with equation (2.14) and for the 2kW PFC preregulator, equation (2.15) is used. In Figure 2.4(i), the tested maximum output power is decided by the maximum speed of a 250W SRM drive, which is 96W at 2300r/min. The efficiency of the 300W PFC preregulator is less than 90% below 30W output power due to the fact that fixed losses are more dominant than the dynamic losses. For output power beyond 40W, the efficiency is in the range of over 90%. Also, the efficiency improves with increasing the load, i.e., in this case with speed. The efficiency of the 2kW PFC preregulator shows evenly above 95% over the entire output power range.

The scatter diagram of the prediction error is shown in Figures 2.5(i) and (ii). The error of prediction is defined as,



(i) 300W PFC preregulator



(ii) 2kW PFC preregulator

Figure 2.5 Error of prediction versus output power with the developed loss models for 300W and 2kW boost PFC preregulators.

$$\text{Error of Prediction} = \left(\frac{\text{Measured Value - Predicted Value}}{\text{MeasuredValue}}\right)\times 100\ ,\ \%\ . \qquad (2.18)$$

The above equation indicates how much the predicted value deviates from the measured value in percent. The error of prediction versus output power is shown in Figure 2.5(i) for the 300W PFC preregulator and in Figure 2.5(ii) for the 2kW PFC preregulator. The magnitude of prediction error is reduced as output power is increased. This is due to the fact that losses such as switch conduction and switching losses increase as output power increases. The prediction error of the 300W PFC preregulator is within ±10%. But, beyond 25W output power, it reduces to within ±4%. For the 2kW PFC case, the prediction error is within ±3% over the entire speed range. The minimum and maximum prediction errors and other statistical values are listed in Table 2.3 [71, 72]. The accuracy of the loss model for the 2kW PFC preregulator is higher than the loss model for the 300W one.

In conclusion, the predicted efficiency closely matches the measured efficiency over the entire power range in both cases. This validates the derived loss models which give practically useful estimates for losses in the boost type PFC preregulator. It should be mentioned that the derived loss model does not show good accuracy in the low output power range. Furthermore the derived loss models for the 300W and 2kW PFC preregulators are used to predict the efficiency of various PF-corrected VSD systems in succeeding studies.

Table 2.3
Statistical analysis of efficiency prediction errors for
300W and 2kW PFC preregulators.

	Fig. 2.4(i) 300W PFC	Fig. 2.4(ii) 2kW PFC
Total Observation	23	14
Minimum Error	-6.00	-2.12
Maximum Error	9.47	2.34
Mean	0.39	0.70
Median	0.16	1.07
Variance	9.06	1.63
Standard Deviation	3.01	1.27
Standard Error	0.63	0.34

2.5 Input Current Harmonics in the Boost PFC Preregulator

In this section, the magnitude of harmonic contents in the input current of the boost PFC preregulator is investigated through experimental measurement and compared with the modified IEC 1000-3-2 standard listed in Table 1.2.

The sample input current waveform and its harmonic content for the 2kW PFC preregulator with a 1400W load is shown in Figure 2.6. Steady-state harmonics are measured using the FFT (Fast Fourier Transformation) with rectangular window. The input ac current closely follows the sinusoidal voltage waveform as designed. The PF of this operating point is calculated as 99% with equations (2.1) and (2.2). The comparison of the measured input current harmonic spectra magnitude with the modified IEC 1000-3-2 Class A limit is shown in Figure 2.7. The harmonic spectra of the input current with the PFC circuit is much improved compared with the rectifier circuit with capacitor shown in Figure 1.4. This validates the effectiveness of the input PFC.

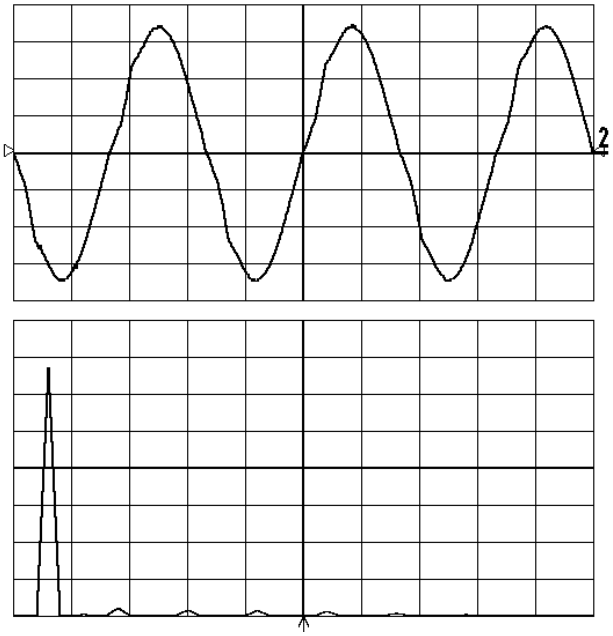


Figure 2.6 Typical waveforms of the 2kW PFC preregulator with 1.4kW load.
(Top) input current (5A/div , 5ms/div)
(Bottom) input current harmonic spectra (2.5A/div , 0.1kHz/div)

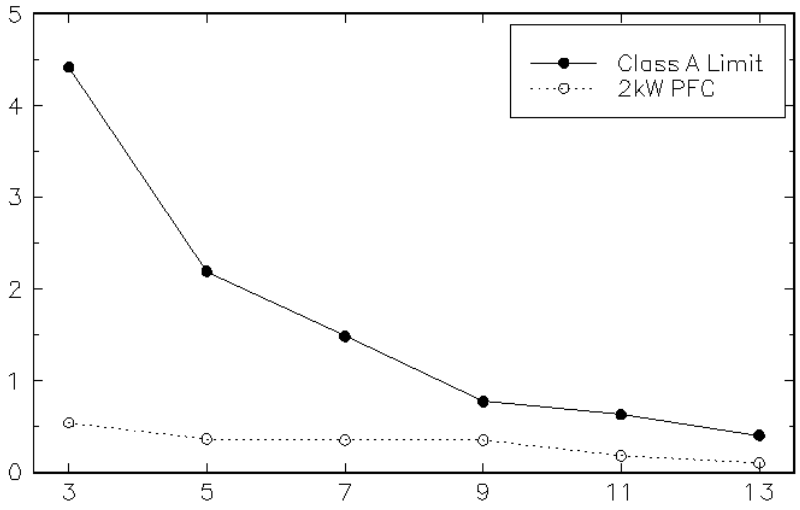


Figure 2.7 Comparison of measured input current harmonic spectra from Figure 2.6 with modified IEC 1000-3-2 Class A harmonic current limit.

2.6 Conclusions

The analysis and design of the front-end boost PFC converter for VSD applications are presented in this chapter. Analytical expressions for ratings and losses of key power components are derived. Based on these derivations, the analytical loss calculations for efficiency prediction are verified with prototype 300W and 2kW PFC preregulators. The total loss models for 300W and 2kW PFC preregulators are derived and utilized to predict the overall converter efficiency.

The measured and predicted efficiencies closely match for both PFC preregulators. The efficiency of the 300W PFC preregulator is less than 90% below 600r/min due to relatively low output power. But above this operating point, the efficiency exceeds 93%. The efficiency of the 2kW PFC preregulator exceeds 95% for the entire output power range because the fixed losses are smaller than the tested output power. The prediction error is within +7% and -5% for the 300W PFC preregulator and ±2% for the 2kW PFC. The scatter diagram of the prediction error is developed and statistical analysis of the error is performed to evaluate the derived loss model. Developed loss models for the 300W and 2kW PFC preregulator yield the precise efficiency predictions, except lower output level for the 300W circuit.

The magnitude of the input line current harmonic spectra is greatly reduced with the PFC preregulator. The magnitude of odd harmonic currents are compared with the modified IEC 1000-3-2 Class A limit for a 120V ac power source to validate the effects of the PFC circuit. They exceed the limits with a significant margin. Therefore the effectiveness of the front-end PFC preregulator is validated.

The derived loss models for the 300W and 2kW PFC preregulators are utilized further to predict overall system efficiencies for the 250W SRM-300W PFC preregulator, 1hp DCM-2kW PFC and 4hp PMBDC-2kW PFC based VSDs.