MODELING AND CONTROL OF ZERO-VOLTAGE TRANSITION THREE-PHASE PWM BOOST RECTIFIER

by

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(ABSTRACT)

Average and small signal modeling of zero-voltage transition three-phase boost rectifier is performed. The effect of ZVT is introduced in the existing model for the three-phase boost rectifier using the time-averaging equivalent circuit approach. The small signal model is derived from the average model. The small signal characteristics are compared to the corresponding characteristics without ZVT. A model is also developed for the independent analog current controller. The models are experimentally verified. In order to perform in-depth study of control approaches, a switching model is also developed. The models are used to investigate various control approaches.

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1. Introduction

The three-phase PWM boost rectifier shown in Fig. 1 is a very attractive topology due to its continuous input currents and high efficiency. However, the size of input filter needed to meet the EMI specs can be quite large. The size of input filter can be reduced by increasing the switching frequency.

Switching losses become a major concern in all applications requiring high switching frequency. Hence soft switching has become a necessity in all high power applications, especially in three-phase power conversion. A number of soft-switched topologies have been developed using resonant and quasi-resonant schemes [1],[2]. Several soft-switched three-phase PWM boost rectifiers have been presented in [3]. A very attractive topology is based on zero-voltage transition (ZVT) technique [4], and is shown in Fig. 2.1.

The three-phase boost rectifier must operate in closed loop in order to achieve unity power factor. Accurate large and small signal models of the rectifier power stage are required to design the controller. It was shown in [5] and [6] that the small signal characteristics of a dc/dc converter change significantly with the introduction of zero-voltage switching. Although the three-phase boost rectifier has been modeled in [7] and

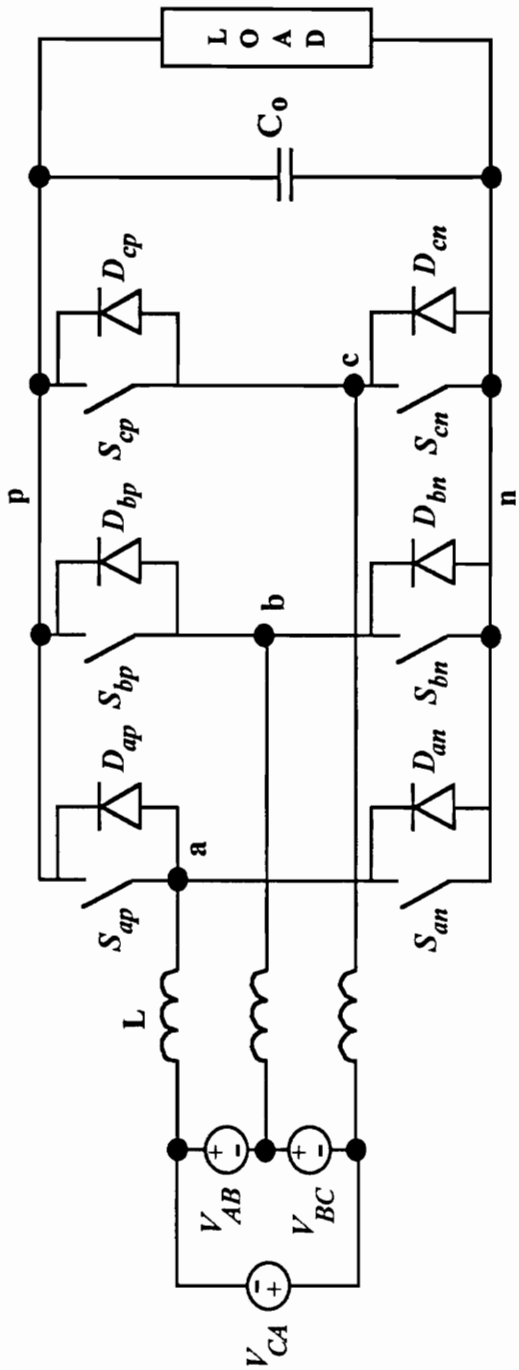


Fig.1 Three-phase PWM boost rectifier

[8], no effort has been made to analyze the effect of zero-voltage switching on small-signal characteristics. The objective of this thesis is to study the effect of soft-switching on the modeling of three-phase boost rectifier. In particular, this thesis concentrates on modeling of ZVT three-phase boost rectifier. The average model developed in [8] is modified to include ZVT, similarly as was done for the modeling of the ZVT dc/dc boost converter, using the time-averaging equivalent circuit approach [9]. The small signal model is derived from the average model and the transfer functions are compared to the corresponding transfer functions of the conventional three-phase boost rectifier to show the effect of ZVT.

The ZVT three-phase boost rectifier requires simple analog control [3]. Three independent controllers are used to model the controller. The design process for the controller is illustrated for a particular set of parameters. The closed loop transfer functions are analyzed. Large signal simulations of the average model are used to interpret the relation between controller performance and its parameters. Also, the drawbacks of the existing controller are highlighted and alternative approaches are investigated with large signal simulations.

In order to investigate the controller performance more deeply, a switching model of the ZVT three-phase boost rectifier is developed in Saber schematic version, Design Star [12]. Switching model is simulated and it is used to confirm the interpretations of the average model. The models are experimentally verified on a practical 6 kW converter.

2. Description of the Converter and its Operation

2.1. Description of the Power Stage

The circuit diagram of three-phase ZVT boost rectifier is shown in Fig. 2.1. This circuit is different from the conventional boost rectifier due to the presence of the dc rail diode, D. The presence of the dc rail diode allows standard ZVT scheme [4] to be implemented on the dc side. The diode isolates the output capacitor and the load from the bridge when the ZVT circuit is activated. All the switches in the bridge operate with soft-switching and with space vector modulation. But, in order to activate the auxiliary ZVT network only once during the switching period, the turn-on instants of the bridge switches should be synchronized. The auxiliary network is similar to the one used in dc/dc ZVT boost converter [4]. It consists of a resonant inductor L_r, an auxiliary switch S_{aux}, and an auxiliary diode D_{aux}, besides the effective capacitance across the bridge, C_r.

2.2. Description of the Current Controller

Although the current control schemes used to control the inverter like linear control, hysteresis control, delta modulation, fuzzy control, etc., can be used to control the three-phase boost rectifier, simple schemes such as the one using three independent analog

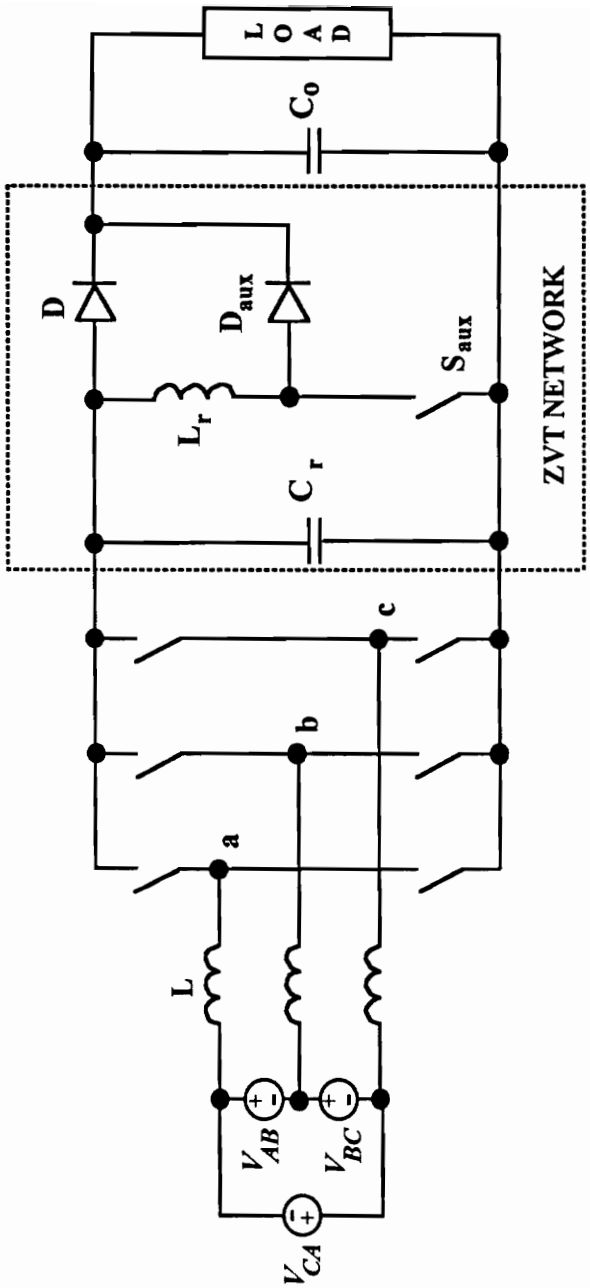


Fig. 2.1 Circuit diagram of ZVT three-phase PWM boost rectifier

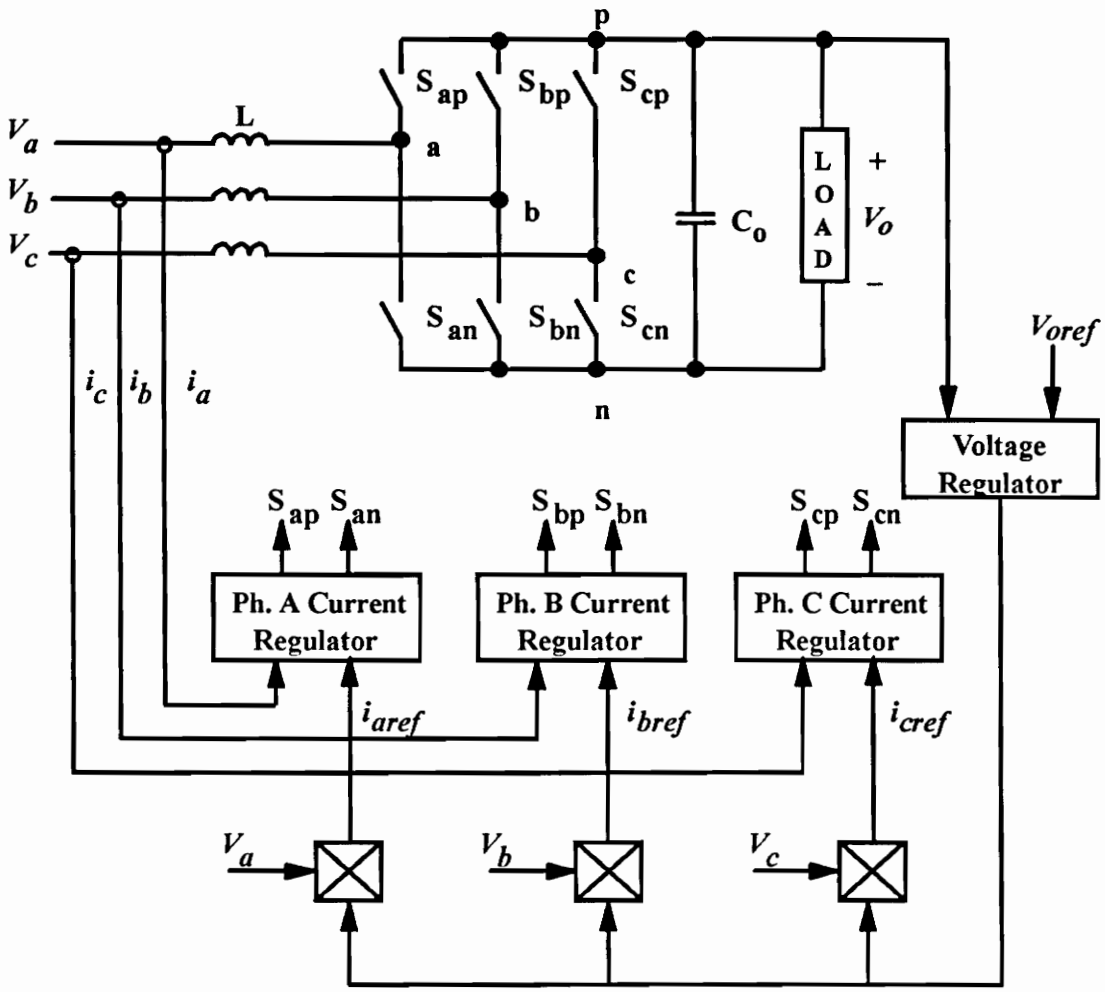


Fig. 2.2 Independent Control of three-phase PWM boost Rectifier

control loops [3], shown in Fig. 2.2 are preferred since the rectifier function is simpler when compared to the inverter function. Although the independent analog control scheme is very simple, it has several drawbacks, as listed in [3]. Most importantly, the independent action of the three controllers can produce severe interference among the three phases causing distortions in the current waveforms. This is because three phase currents always sum up to zero so that only two of the them are independent, but the controllers attempt to control all three independently. To avoid this, six-step PWM can be used. However, the independent analog control scheme can be used with the ZVT three-phase boost rectifier due to the presence of the dc rail diode which provides automatic six-step operation [3].

In the independent analog control scheme, the sinusoidal current reference for each phase is generated by the product of the voltage compensator output and a signal proportional to the corresponding input phase voltage. This scheme is similar to the one used in single-phase power factor correction (PFC) circuit. Hence, three standard power factor correction chips, such as UC1854, can be used for each phase, as shown in Fig. 2.3. The inputs to each chip are: the sensed and rectified current signal, and the corresponding sensed and rectified input phase voltage.

Another input to this chip is the rms value of the corresponding input phase voltage. The rms value is squared within the chip. Hence, the current reference for phase a, created within the chip is [11]:

$$i_{aref} = \frac{k v_a v_c}{n (v_{arms})^2}$$

where k is the internal gain of the chip, n is the voltage sensing transformer turns ratio, and v_c is the output of the voltage compensator. Division by $(v_{arms})^2$ provides an input voltage feed-forward, so that when the input voltage decreases the current reference will proportionally increase so that the power drawn from the input depends only on v_c. The effect of feedforward will be further investigated in Chapter 4.

The output of the chip controls either the top switch or the bottom switch depending on the polarity of the input phase voltage, through the switch decoder and zero-crossing detector.

In the six-step PWM rectifier operation, the input phase current that has instantaneously largest absolute value flows only through one of the diodes in the corresponding bridge leg. For e.g., during a 60° interval of the input phase currents when $i_a > 0$, $i_b < 0$, and $i_c < 0$, the current i_a has the largest absolute value and it will flow through the diode D_{ap} in Fig. 2.1. During that interval, the current i_b will flow through the switch S_{bp} or the diode D_{bn}, while the current i_c will flow through the switch S_{cp} or the diode D_{cn}, depending on the PWM action. If the PWM controller were to close the switch S_{ap}, the current i_a would still flow through the diode D_{ap}. But if the controller closes the switch S_{an} then the current in the dc-rail diode would tend to reverse in

direction which would be prevented by the dc-rail diode and the current i_a would again flow through diode D_{ap}. In this way, as mentioned earlier, the dc-rail diode imposes six-step operation on the bridge, regardless of the PWM controller action. But in order to do so, it relies on the instantaneous value of the maximum input phase current. However, this will also produce interference at the beginning of each 60° segment when one of the currents is zero and the other two have the same absolute value. If the switching current ripple is relatively large, the phase current with the largest absolute value will change several times thus causing distortion in all three currents. This could be minimized if the switches in the leg corresponding to the largest current are disabled during the whole 60° interval. The independent control scheme with the disabling logic is as shown in Fig. 2.4. The disabling logic circuit is implemented with a group of logic gates. The logic senses the maximum input phase voltage and disables the switches in the corresponding leg during a particular 60° segment. As an example, when phase a is maximum, the switches S_{ap} and S_{an} are disabled.

This scheme is very easy to implement. The use of single-phase PFC chip for the independent control of three-phase currents makes the implementation even more simple and cheap as it reduces the number of components, thereby reducing the amount of space utilized. However, it will be observed in Chapter 4 through average model that rectification of error signal can produce severe distortions in the input phase currents. Possible solutions and alternative approaches are also discussed in Chapter 4.

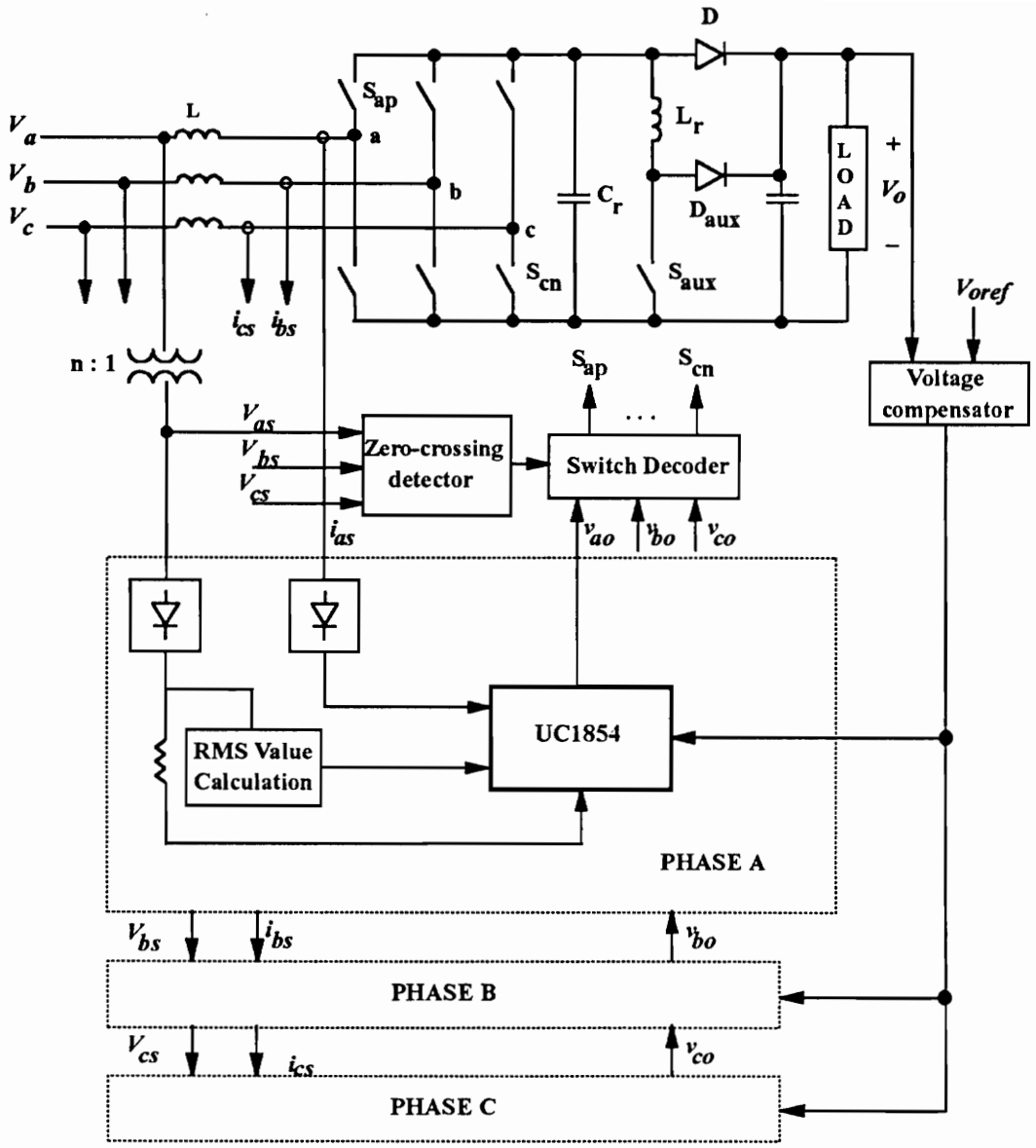


Fig. 2.3 Current control scheme using UC1854

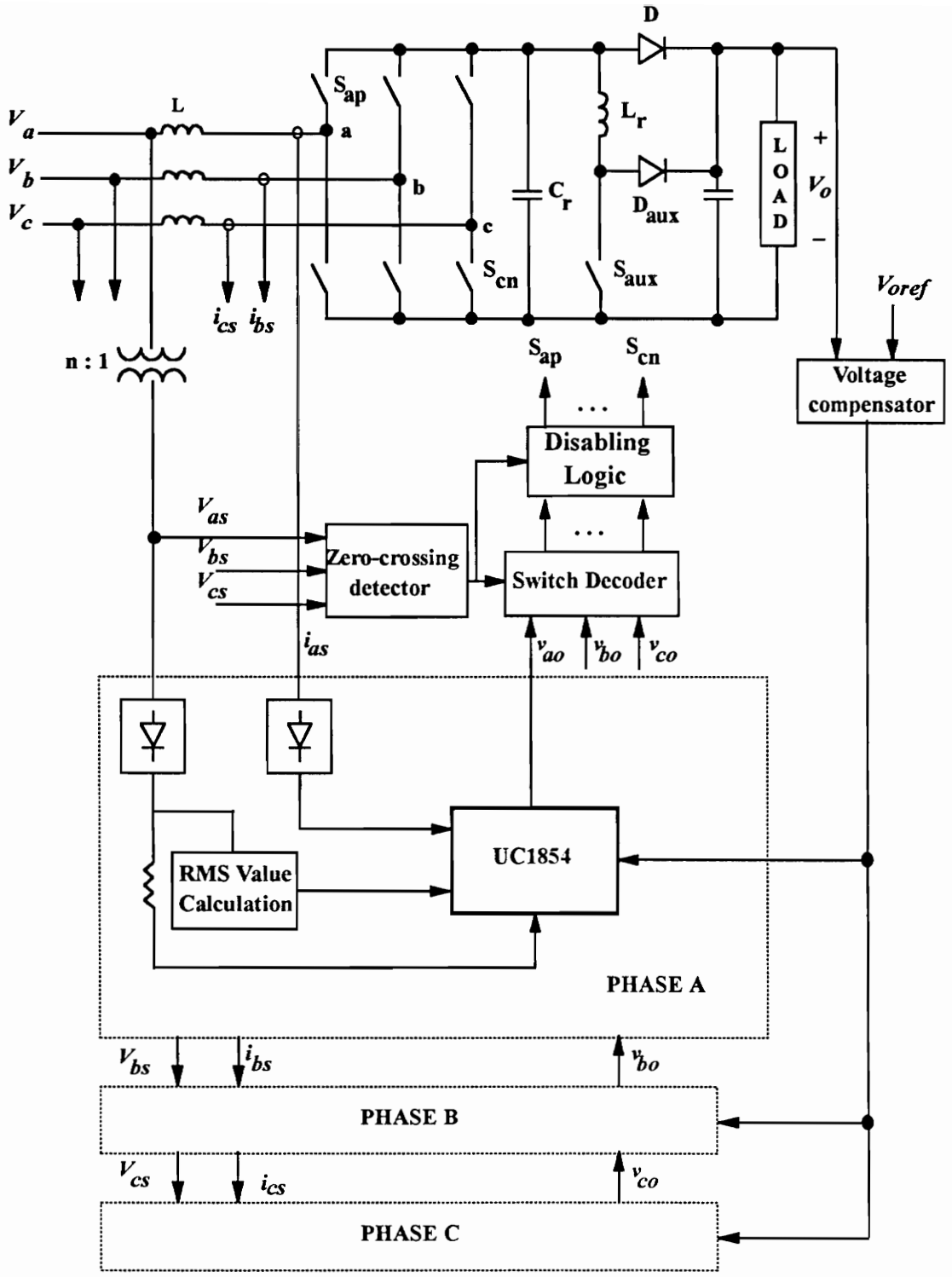


Fig. 2.4 Independent current control scheme with disabling logic.

2.3. Description of ZVT Operation

The ZVT operation of the circuit shown in Fig. 2.1, operating with unity power factor, is illustrated for the 60° interval within the input line period when $i_a > 0$, $i_b \leq 0$, $i_c \leq 0$. It is assumed that the switching sequence is arranged in such a way that at the beginning of switching cycle, only three anti-parallel diodes D_{ap}, D_{bn}, and D_{cn} conduct, as shown in Fig. 2.5a. Switches S_{ap} and S_{an} are disabled and the current i_a flows through the anti-parallel diode D_{ap}. In the standard PWM boost rectifier, the switches S_{bp} and S_{cp} are turned on immediately after this state, causing large reverse recovery currents through the anti-parallel diodes D_{bn} and D_{cn}, and the dc-rail diode D. To avoid this, the ZVT circuit is activated.

Period T_0 to T_1 : The auxiliary switch S_{aux} is turned on at time T_0, as shown in Fig. 2.5b. This causes the current through the resonant inductor, i_{Lr}, to linearly ramp up until it reaches the instantaneous peak value of the maximum input phase current, which is i_a in the 60° segment under consideration. Current through the dc-rail diode, i_D, simultaneously starts reducing until it reaches zero at time T_1. This time interval is given by

$$T_1 - T_0 = \frac{L_r i_{ins}}{v_o}, \tag{2.1}$$

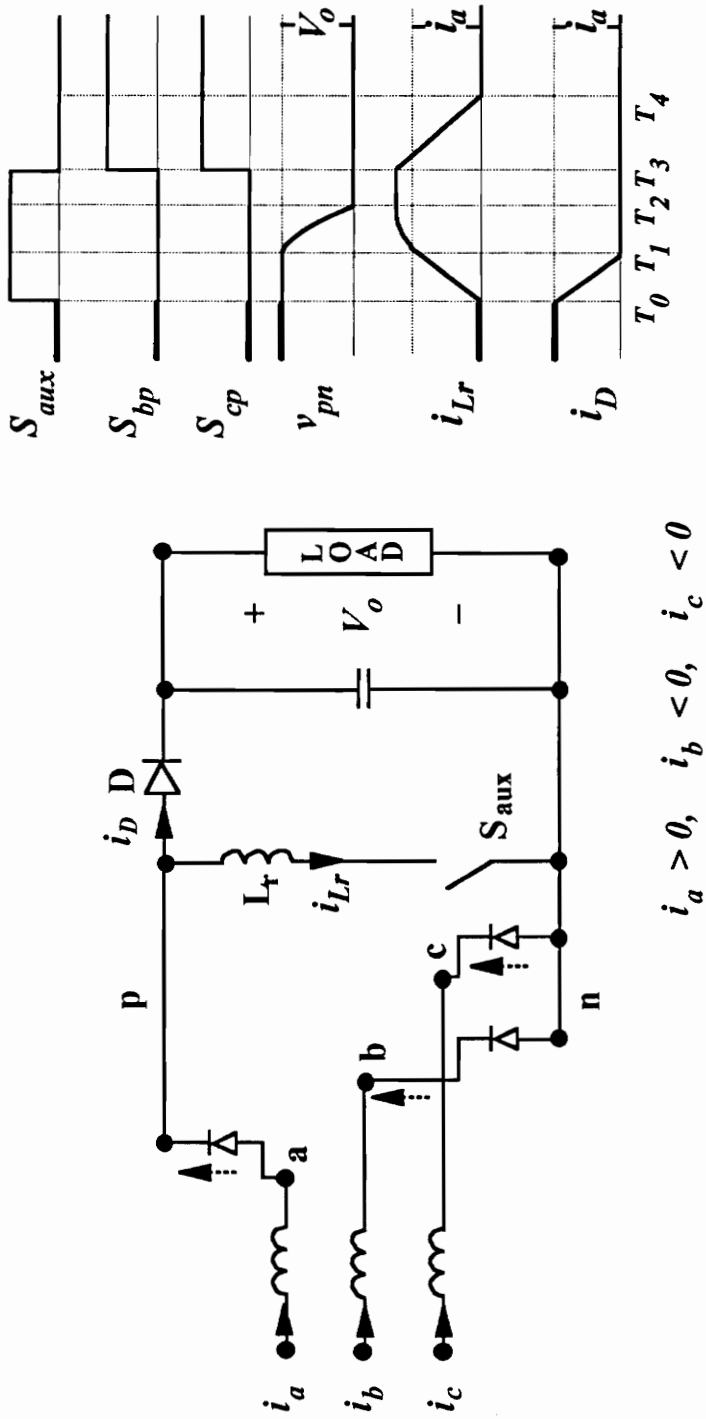


Fig. 2.5a Principle of operation : prior to time T_0

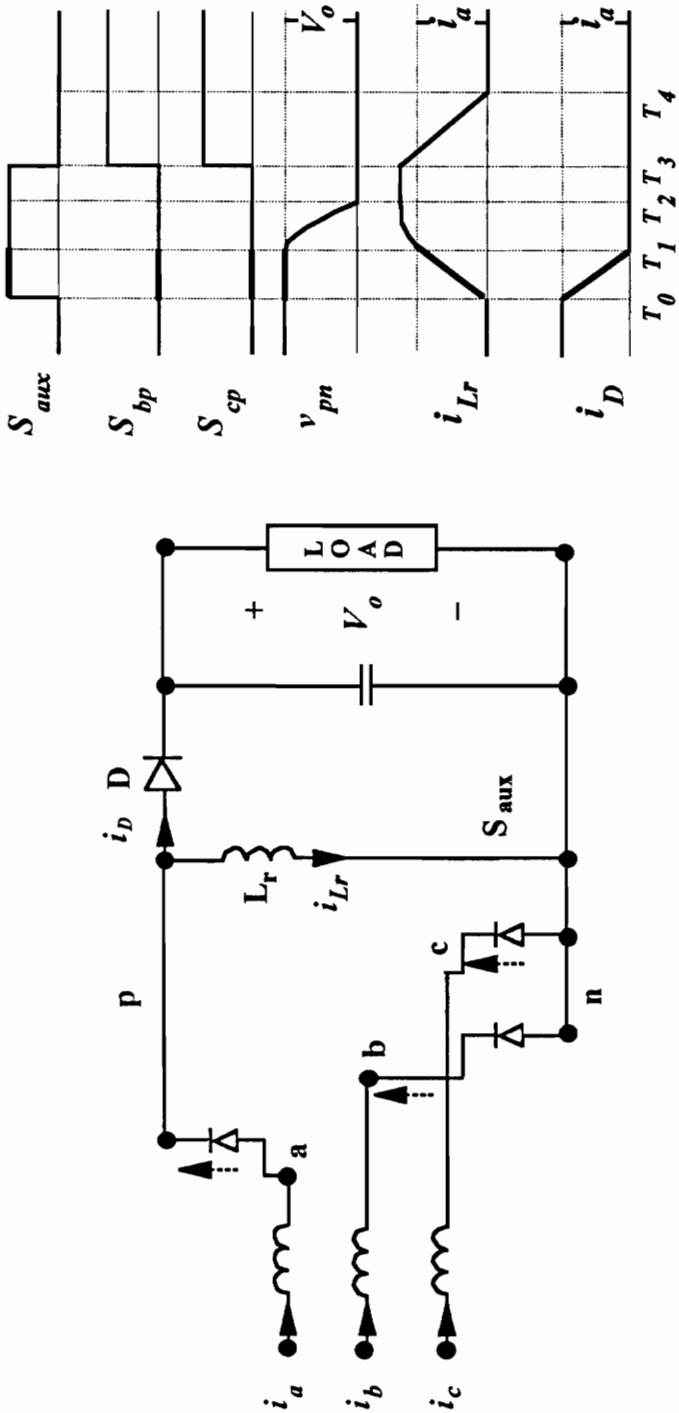


Fig. 2.5b Principle of operation : period $T_0 - T_1$

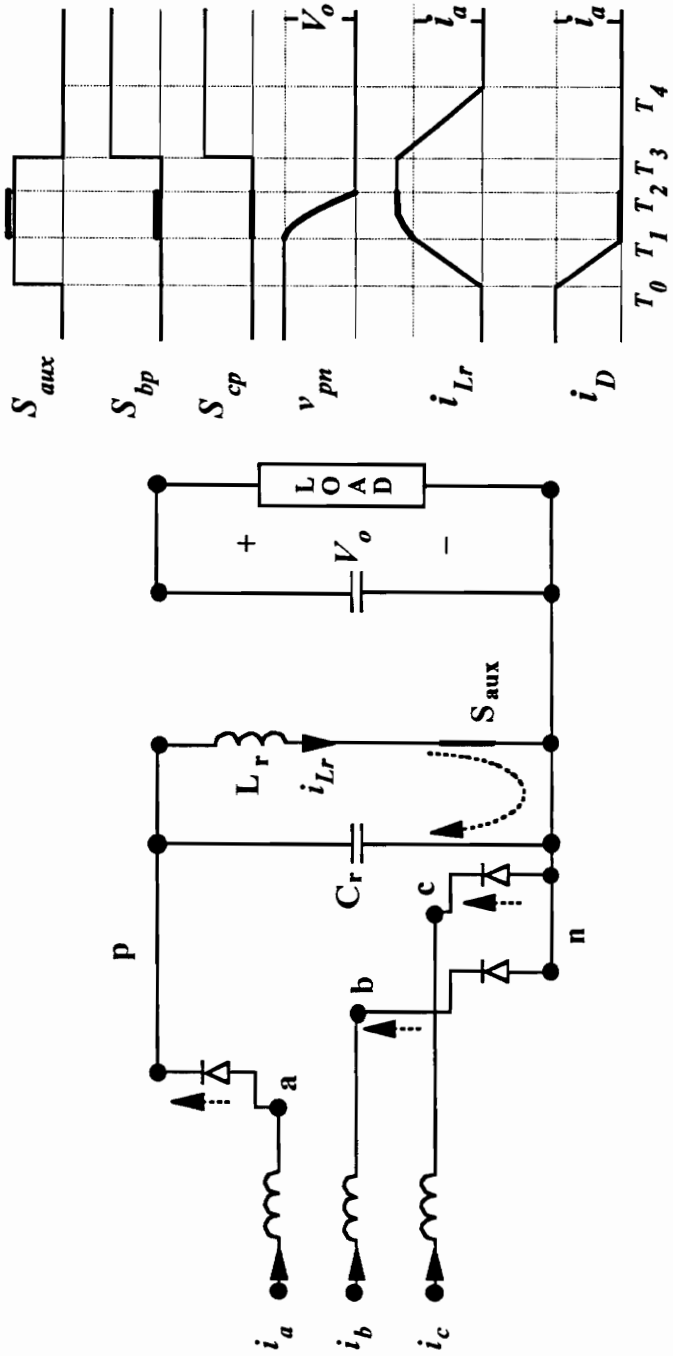


Fig. 2.5c Principle of operation : period $T_1 - T_2$

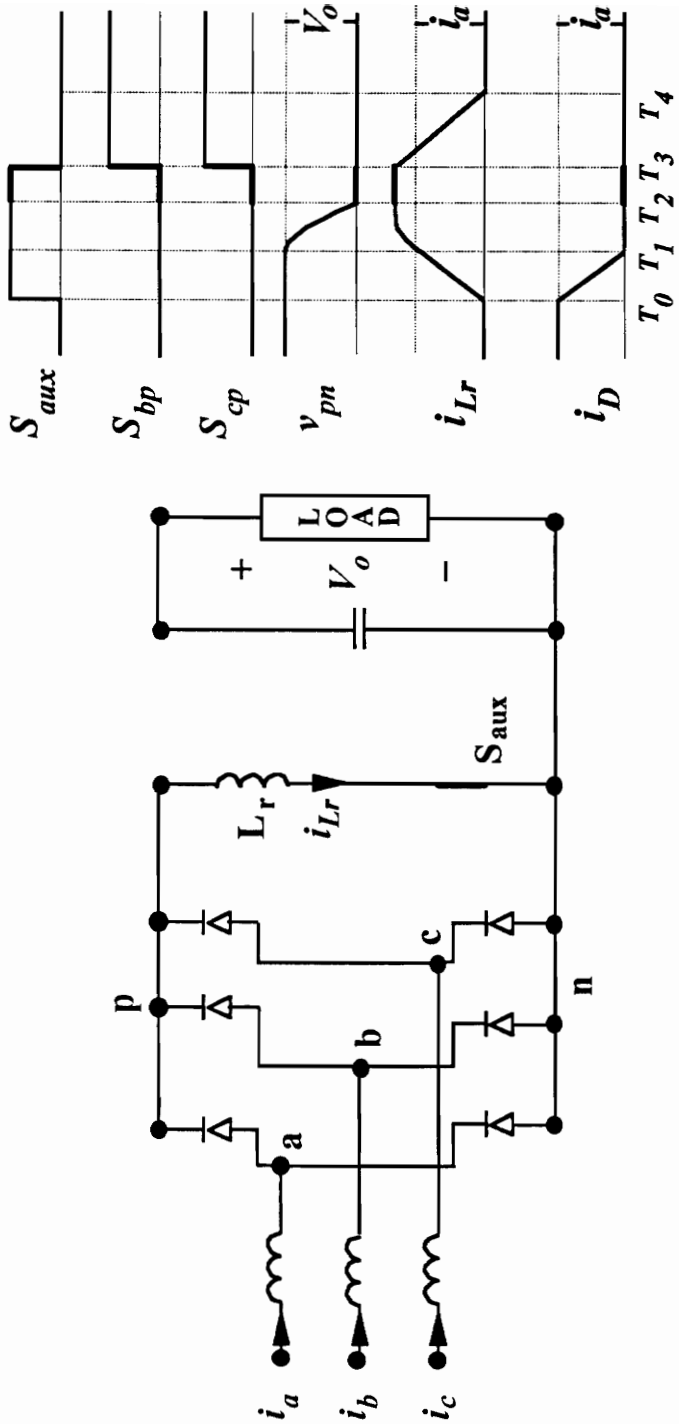


Fig. 2.5d Principle of operation : period $T_2 - T_3$

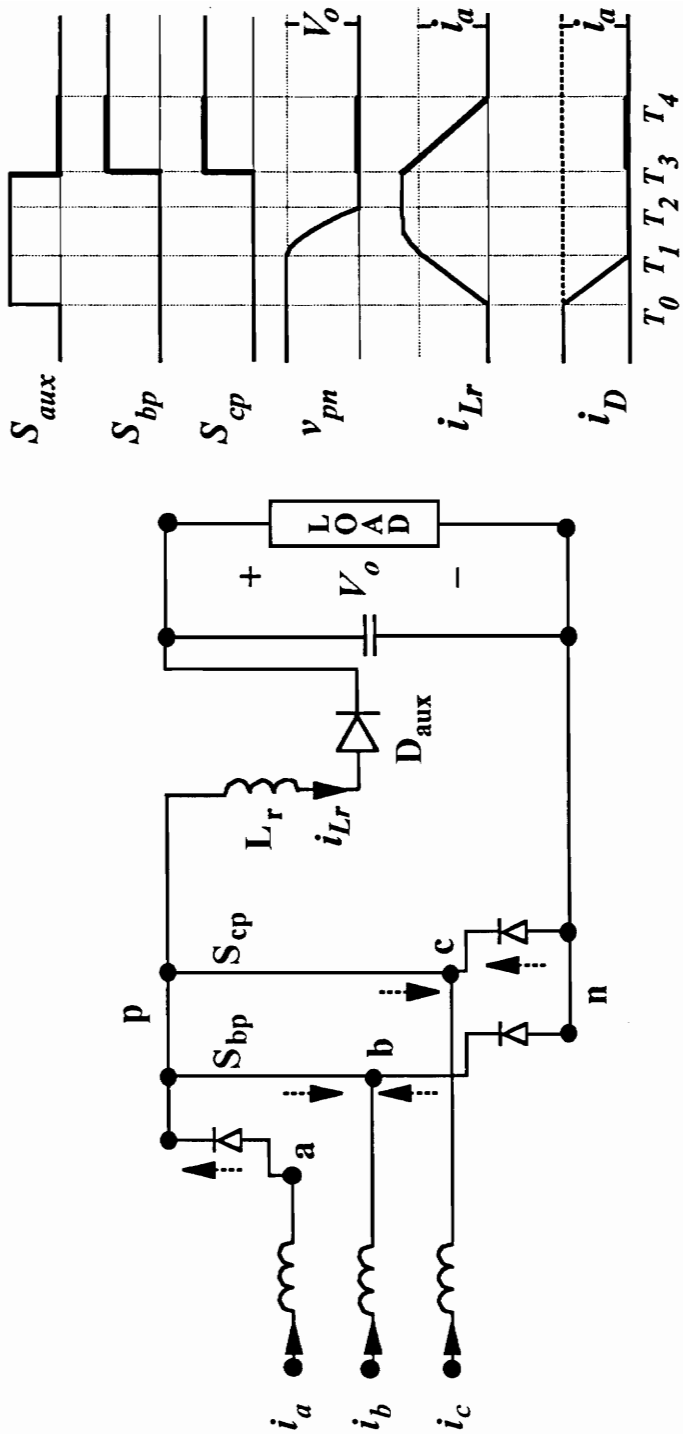


Fig. 2.5e Principle of operation : period $T_3 - T_4$

where i_{ins} is the instantaneous value of the largest input current in the present 60° interval and v_o is the output voltage.

Period T_1 to T_2 : Diode D turns off at time T_1, as shown in Fig. 2.5c. If the diode D is a fast recovery diode, then its reverse recovery current will be negligible because of the controlled dv/dt and di/dt at turn-off. After time T_1, the resonant inductor current, i_{Lr}, continues to increase due to resonance between the resonant inductor, L_r, and the resonant capacitor C_r. In the process, the bridge output voltage, v_{pn}, reduces in a resonant fashion until it reaches zero at time T_2. This produces a zero vector at the bridge input. This resonant period is given by

$$T_2 - T_1 = \frac{\pi}{2}\sqrt{L_r C_r}\,, \tag{2.2}$$

Period T_2 to T_3 : Once the bridge output, v_{pn}, reduces to zero, the remaining anti-parallel diodes in the bridge also start conducting, as shown in Fig. 2.5d. The switches S_{bp} and S_{cp} can be turned on any time after their anti-parallel diodes start conducting. Current through the resonant inductor, i_{Lr}, remains constant during this period.

Period T_3 to T_4 : The switches S_{bp} and S_{cp} are turned on as shown in Fig 2.5e. The auxiliary switch, S_{aux}, is turned off at time T_3. Its voltage is clamped to the output voltage due to conduction of the auxiliary diode, D_{aux}. The duty cycle of the auxiliary

switch, d_{aux}, which determines the delay between the auxiliary switch and the main switch turn-on, has to satisfy the following condition in order to achieve zero-voltage switching:

$$d_{aux}T_s = (T_3 - T_0) \geq (T_1 - T_0) + (T_2 - T_1), \tag{2.3}$$

where T_1-T_0 and T_2 - T_1 are given by (2.1) and (2.2) respectively, and T_s is the total switching period.

After time T_3, the energy stored in the resonant inductor is transferred to the output capacitor through the auxiliary diode, D_{aux}. D_{aux} stops conducting at time T_4 when the energy stored in L_r is completely transferred to the capacitor. This time interval is given by:

$$T_4 - T_3 = \left(\frac{L_r i_{ins}}{v_o} + \sqrt{L_r C_r} \right), \tag{3.4}$$

This completes the soft-transition period. The operation of this circuit after T_4 is same as its PWM counterpart. The circuit operation and the waveforms are cyclically symmetrical during other 60° intervals.

3. Modeling of the Converter Power Stage:

3.1 Modeling Approach

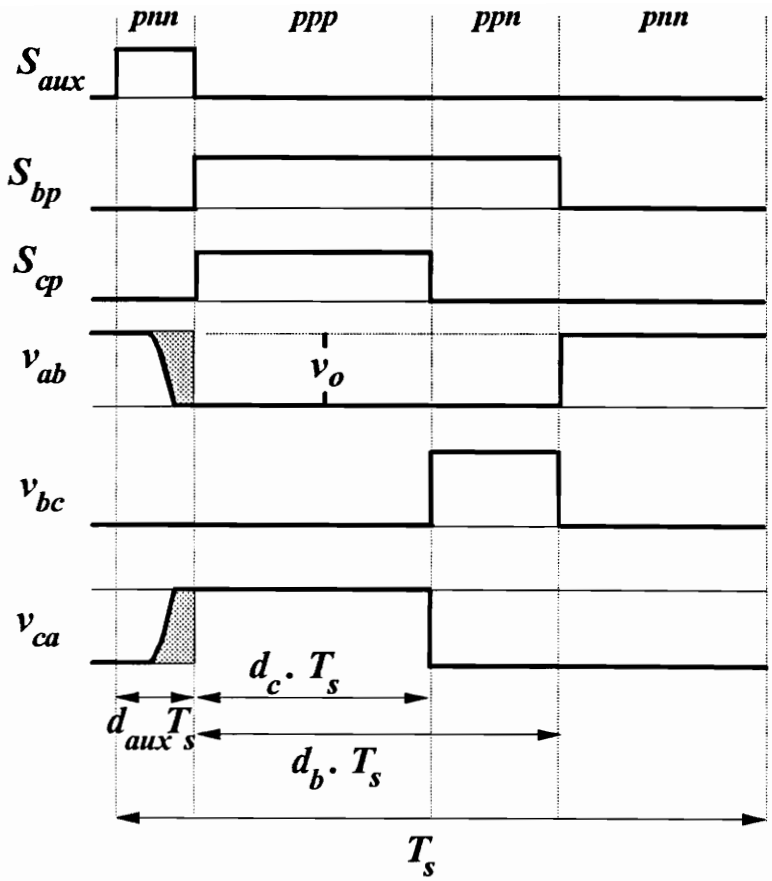
The dc/dc ZVT boost converter was modeled and experimentally verified using time-averaging equivalent circuit approach, [5] and [9]. This approach can be considered as an extension of the state-space averaging approach.

It was observed in the previous chapter that the bridge input voltages change earlier in case of ZVT boost rectifier when compared to standard PWM boost rectifier. Also, the output capacitor is charged through two diodes. ZVT does not have any influence on the remaining part of the circuit operation. Hence, the only need is to quantify these two changes in the existing models of the standard PWM boost rectifier, [7],[8], using time-averaging equivalent circuit approach [9]. In this, the commutation circuit dynamics are neglected.

3.2 Derivation of Average Model in Stationary Coordinates

3.2.1 : Line Voltages at the Bridge Input

Consider the line voltages at the bridge input nodes, a, b, and c. If the ZVT circuit were not activated, the average line voltages at the bridge input would be, [8],

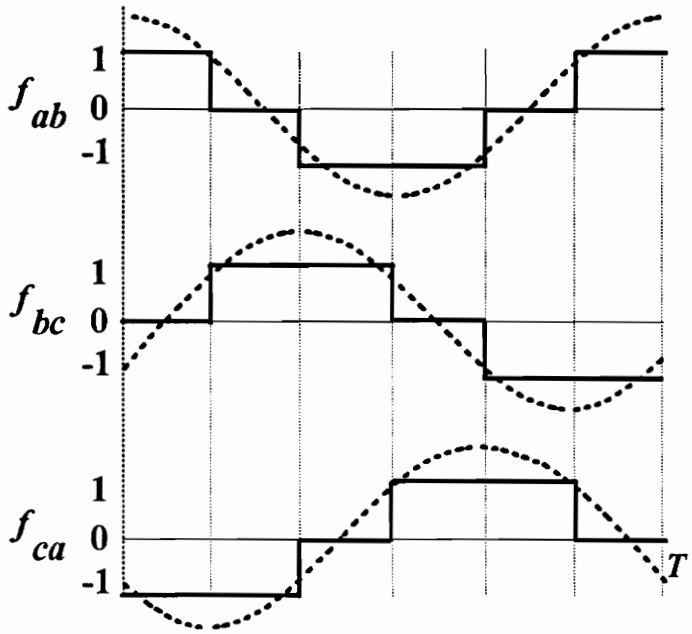


$$v_{ab} = d_{ab} \cdot v_o - \Delta d \cdot v_o$$

$$v_{bc} = d_{bc} \cdot v_o$$

$$v_{ca} = d_{ca} \cdot v_o + \Delta d \cdot v_o$$

Fig. 3.1 Line voltages at the bridge input during one switching cycle when $i_a > 0,\ i_b < 0,\ i_c < 0$



——— *function*

---------- *first harmonic approximation*

Fig. 3.2 Modeling the change in effective duty cycle

$$v_{ab} = d_{ab} \cdot v_o, \quad v_{bc} = d_{bc} \cdot v_o, \quad v_{ca} = d_{ca} \cdot v_o \tag{3.1}$$

In (3.1), $d_{ab} = d_a - d_b$, $d_{bc} = d_b - d_c$ and $d_{ca} = d_c - d_a$, where d_i $(i=a,b,c)$ are duty cycles of the switches S_{ip}. Due to the action of the ZVT circuit, $d_{ab} \cdot v_o$ decreases and $d_{ca} \cdot v_o$ increases by the average value of the shaded area in the waveforms of v_{ab} and v_{ca} respectively, shown in Fig. 3.1. This shaded area can be easily calculated from Figs. 3.1 and 2.5, and the effective change in duty cycles is given by

$$\Delta d = d_{aux} - \frac{T_1 - T_0}{T_s} - \frac{2}{\pi}\frac{T_2 - T_1}{T_s} \tag{3.2}$$

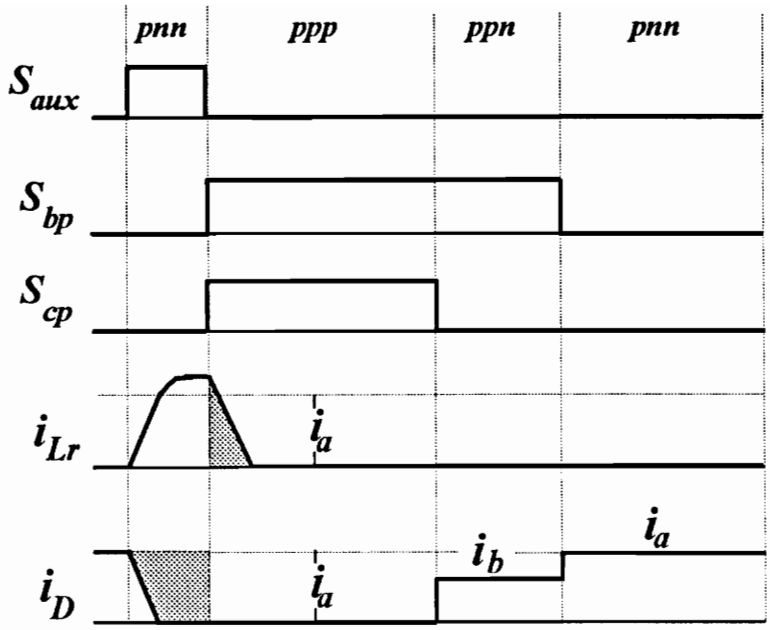
In (3.2), $T_1 - T_0$ and $T_2 - T_1$ are given by (2.1) and (2.2) respectively. The change in effective duty cycle, Δd, is the same throughout the 60° interval and changes cyclically within the line period. As a result, the average model of the three-phase PWM boost rectifier can be modified so that

$$\begin{aligned} v_{ab} &= (d_{ab} - f_{ab} \cdot \Delta d)v_o, \\ v_{bc} &= (d_{bc} - f_{bc} \cdot \Delta d)v_o, \\ v_{ca} &= (d_{ca} - f_{ca} \cdot \Delta d)v_o. \end{aligned} \tag{3.3}$$

where f_{ab}, f_{bc} and f_{ca} are quasi-square wave functions which represent the cyclical change in duty cycles and are shown in Fig. 3.2.

3.2.2 Current Charging the Output Capacitor:

Consider the current charging the output capacitor. The average value of the current supplying the output capacitor and the load without ZVT would be, [8],



$$i_p = d_{ab} \cdot i_{ab} + d_{bc} \cdot i_{bc} + d_{ca} \cdot i_{ca} - i_x$$

Fig. 3.3 Modeling the change in current charging the output capacitor

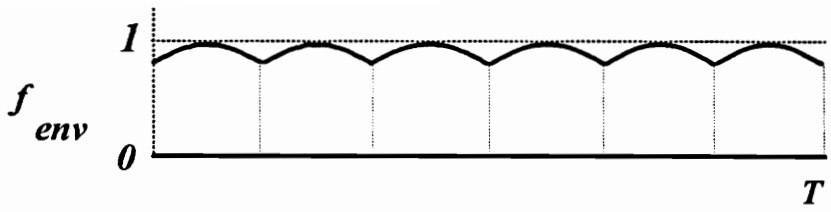


Fig. 3.4 Modeling the change in current charging the output capacitor

$$i_p = d_{ab} \cdot i_{ab} + d_{bc} \cdot i_{bc} + d_{ca} \cdot i_{ca},$$

where

$$i_{ab} = (i_a - i_b)/3,\ i_{bc} = (i_b - i_c)/3,\ i_{ca} = (i_c - i_a)/3.$$

With ZVT this current not only decreases by the amount i_{Ds}, which is the average value of the shaded part of the waveform of i_D in Fig. 3.3, but also has an additional component through the diode D_{aux} which is equal to the average value of the shaded part of the waveform of i_{L_r} in Fig. 3.3, i.e.

$$i_p = (d_{ab} \cdot i_{ab} + d_{bc} \cdot i_{bc} + d_{ca} \cdot i_{ca}) - i_x, \tag{3.3}$$

where

$$i_x = i_{Ds} - i_{L_{rs}}. \tag{3.4}$$

The components i_{Ds} and $i_{L_{rs}}$ can be easily derived from Figs. 2.5 and 3.3 and are given by

$$i_{Ds} = \left(d_{aux} - \frac{T_1 - T_0}{2T_s} \right) i_{ins}, \tag{3.5}$$

$$i_{L_{rs}} = \frac{T_4 - T_3}{2T_s} \left(i_{ins} + \frac{v_o}{\sqrt{L_r / C_r}} \right) \tag{3.6}$$

In (3.5) and (3.6), T_1 - T_0 and T_4 - T_3 are given by (2.1) and (2.4) respectively. i_{ins} is the instantaneous peak value of the current charging the output capacitor. It is not constant and it varies during consecutive 60° intervals. This behavior of i_{ins} can be characterized by

a function f_{env} shown in Fig. 3.4. Then i_{ins} can be expressed in terms of the amplitude of input currents, I_m, and f_{env} as follows:

$$i_{ins} = f_{env} \cdot I_m \tag{3.7}$$

The remaining part of the circuit is linear and can be described by, [8],

$$\begin{aligned} v_{AB} &= 3L\frac{di_{ab}}{dt} + v_{ab}, \\ v_{BC} &= 3L\frac{di_{bc}}{dt} + v_{bc}, \\ v_{CA} &= 3L\frac{di_{ca}}{dt} + v_{ca}, \end{aligned} \tag{3.8}$$

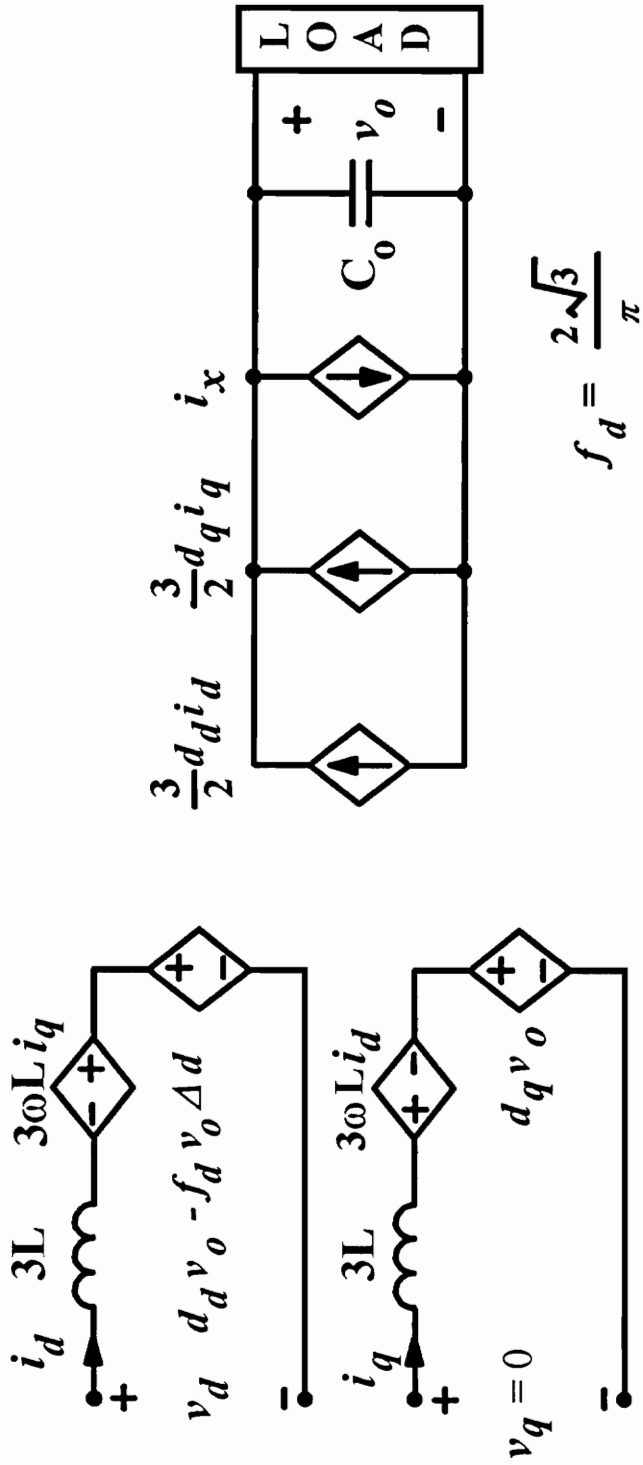
and

$$i_p = C\frac{dv_o}{dt} + i_o \tag{3.9}$$

Equations (3.1) to (3.9), together with (2.1), (2.2), and (2.3) represent the average model of the ZVT three-phase PWM boost rectifier in stationary coordinates.

3.3 Derivation of Average Model in Rotating Coordinates

The average model in stationary coordinates cannot be linearized to give a small signal model as the variables are sinusoidal in steady state. Hence the model is transformed to rotating reference frame using the d-q coordinate transformation, [7], [8]. However, d-q transformation of the functions in Figs. 4.2 and 4.4 would also result in time varying variables in steady state. The approximate models can be derived if the quasi-square wave



$$f_d = \frac{2\sqrt{3}}{\pi}$$

Fig. 3.5 Average model in rotating coordinates

functions f_{ab}, f_{bc} and f_{ca} are substituted by their first harmonics before the coordinate transformation. The first harmonic approximations of f_{ab}, f_{bc} and f_{ca} are given by

$$f_{ab} \approx \frac{2\sqrt{3}}{\pi}\cos(\omega t),\ f_{bc} \approx \frac{2\sqrt{3}}{\pi}\cos\left(\omega t - \frac{2\pi}{3}\right),\ f_{ca} \approx \frac{2\sqrt{3}}{\pi}\cos\left(\omega t + \frac{2\pi}{3}\right) \tag{3.10}$$

The function f_{env} is represented with its average value, $3/\pi$. The resulting model in rotating reference frame is shown in Fig. 3.5. The angular frequency of the rotating reference frame is equal to the line frequency $2\pi f_l$, and the d-axis is aligned with the voltage v_{ab}. Variables f_{ab}, f_{bc} and f_{ca} are also transformed into d-q frame and the corresponding d and q components are given by

$$f_d = \frac{2\sqrt{3}}{\pi},\ f_q = 0 \tag{3.11}$$

3.4 Small signal model

The average model shown in Fig. 3.5 can be linearized to give a linear time-invariant small signal model. The linearized equations are shown below:

$$\frac{d\hat{i}_d}{dt} = \frac{1}{3L}\hat{v}_d + \omega\hat{i}_q - \frac{V_o}{3L}\hat{d}_d + \left(\frac{D_d}{3L} + \frac{f_d \cdot \Delta d}{3L}\right)\hat{v}_o + \frac{f_d \cdot V_o}{3L}\Delta\hat{d}, \tag{3.12}$$

$$\frac{d\hat{i}_q}{dt} = -\omega\hat{i}_d - \frac{V_o}{3L}\hat{d}_q - \frac{D_q}{3L}\hat{v}_o, \tag{3.13}$$

$$\frac{d\hat{v}_o}{dt} = \frac{3D_d}{2C}\hat{i}_d + \frac{3I_d}{2C}\hat{d}_d + \frac{3D_q}{2C}\hat{i}_q - \frac{1}{C}\hat{i}_x, \tag{3.14}$$

where

$$\Delta\hat{d} = d_{aux} - \frac{3L_r}{\pi T_s}\left(\frac{1}{V_o}\hat{i}_d - \frac{I_d}{V_o^2}\hat{v}_o\right), \tag{3.15}$$

and

$$\hat{i}_x = \left[\frac{3d_{aux}}{\pi} - \frac{3\sqrt{L_r C_r}}{\pi T_s} - \frac{18L_r I_d}{\pi^2 V_o T_s}\right]\hat{i}_d + \left(\frac{9L_r I_d^2}{\pi^2 V_o^2 T_s} - \frac{C_r}{T_s}\right)\hat{v}_o. \tag{3.16}$$

The above equations are derived under the assumption of unity input displacement factor, when the steady state value of the direct component of the input current, I_d is equal to I_m, the amplitude of the input phase currents, and the quadrature component, I_q is zero. In (3.12) -(3.16) uppercase letters denote steady state values, while the symbol, ^ denotes small-signal perturbation.

To study the effect of ZVT, this small signal model was simulated for a 6 kW converter (parameters are in Appendix A) and the results were compared with the corresponding results for PWM converter..

Fig. 3.6(a) to Fig. 3.6(g) show all the small signal transfer functions of the three-phase boost rectifier with and without ZVT. There is a slight decrease in the dc gain, and significant increase in damping introduced by ZVT in all the transfer functions. This result is in agreement with previous results for dc/dc converters, [5], [6]. To illustrate the damping and change in dc gain with ZVT, the value of resonant inductor, L_r was varied and the corresponding control to output transfer functions are as shown in Fig. 3.7. The

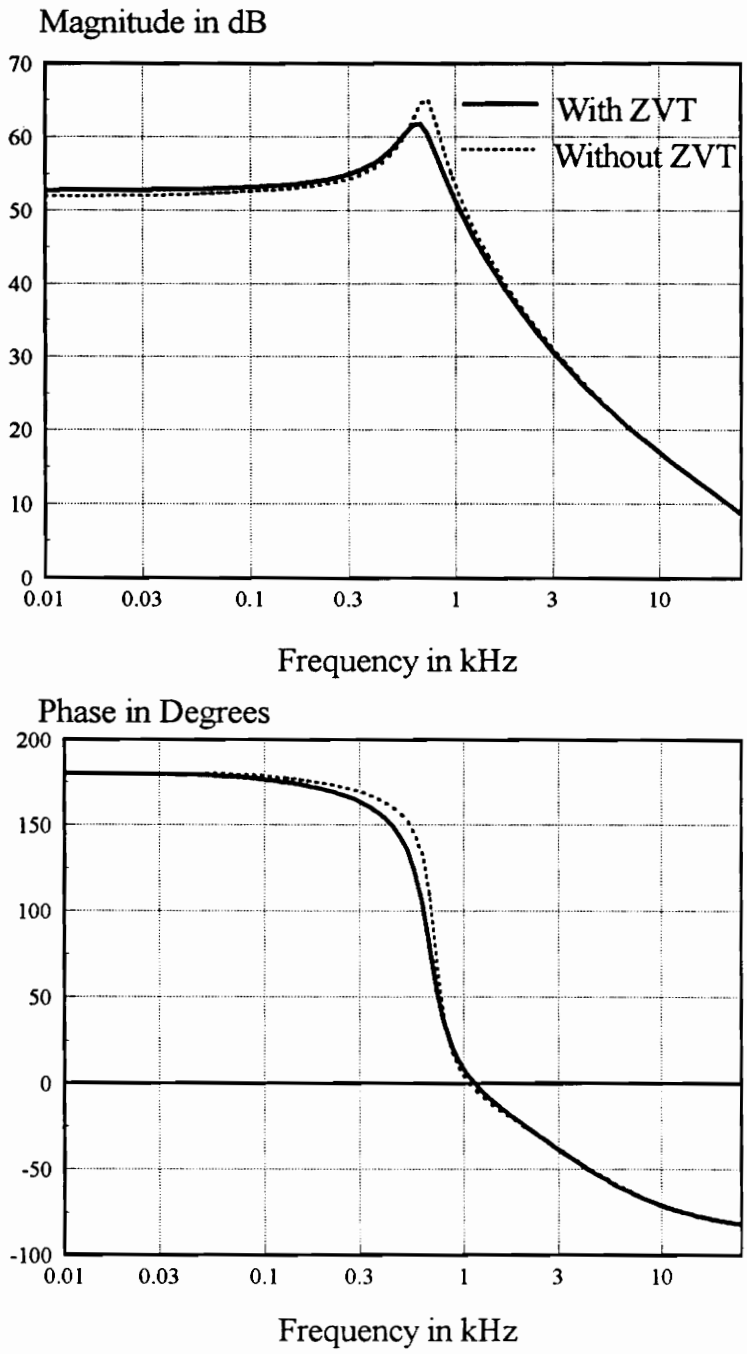


Fig 3.6(a). $\hat{v}_o$ / $\hat{d}_d$ transfer function

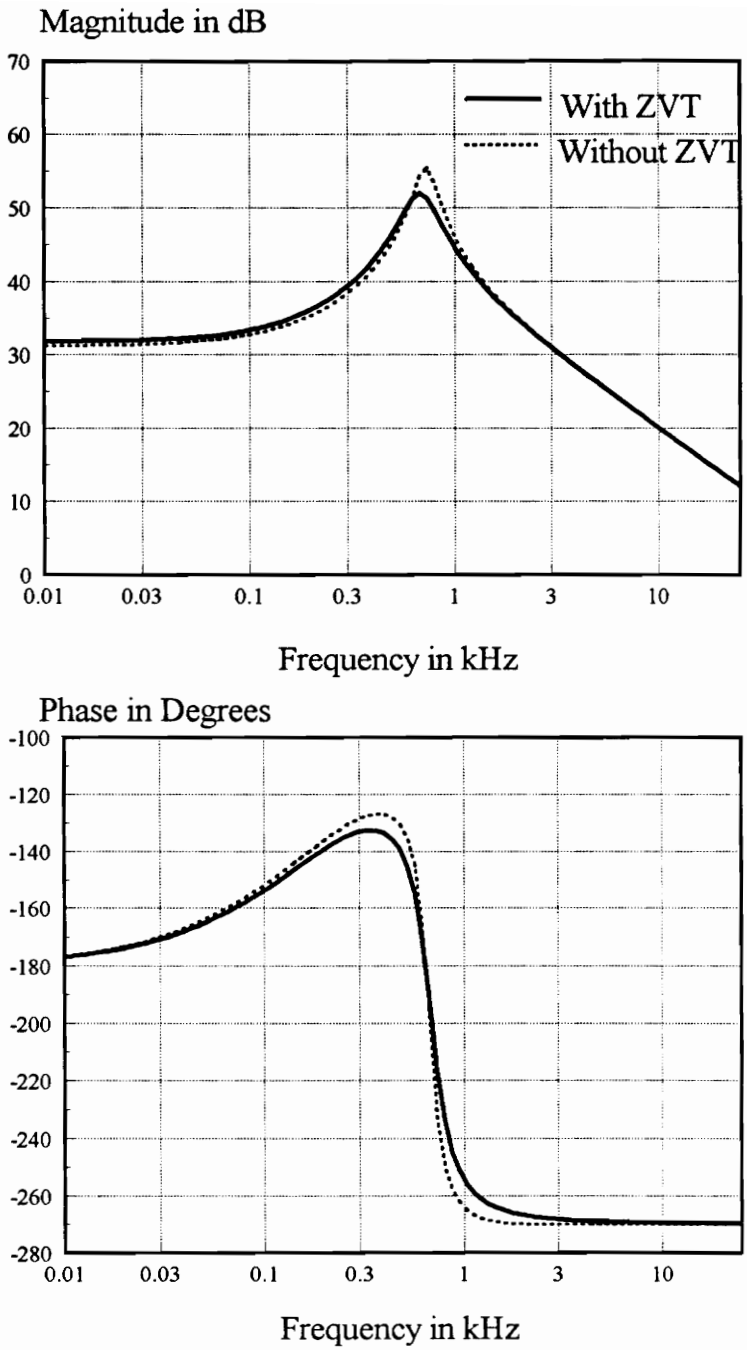


Fig 3.6(b). $\hat{i}_d$ / $\hat{d}_d$ transfer function

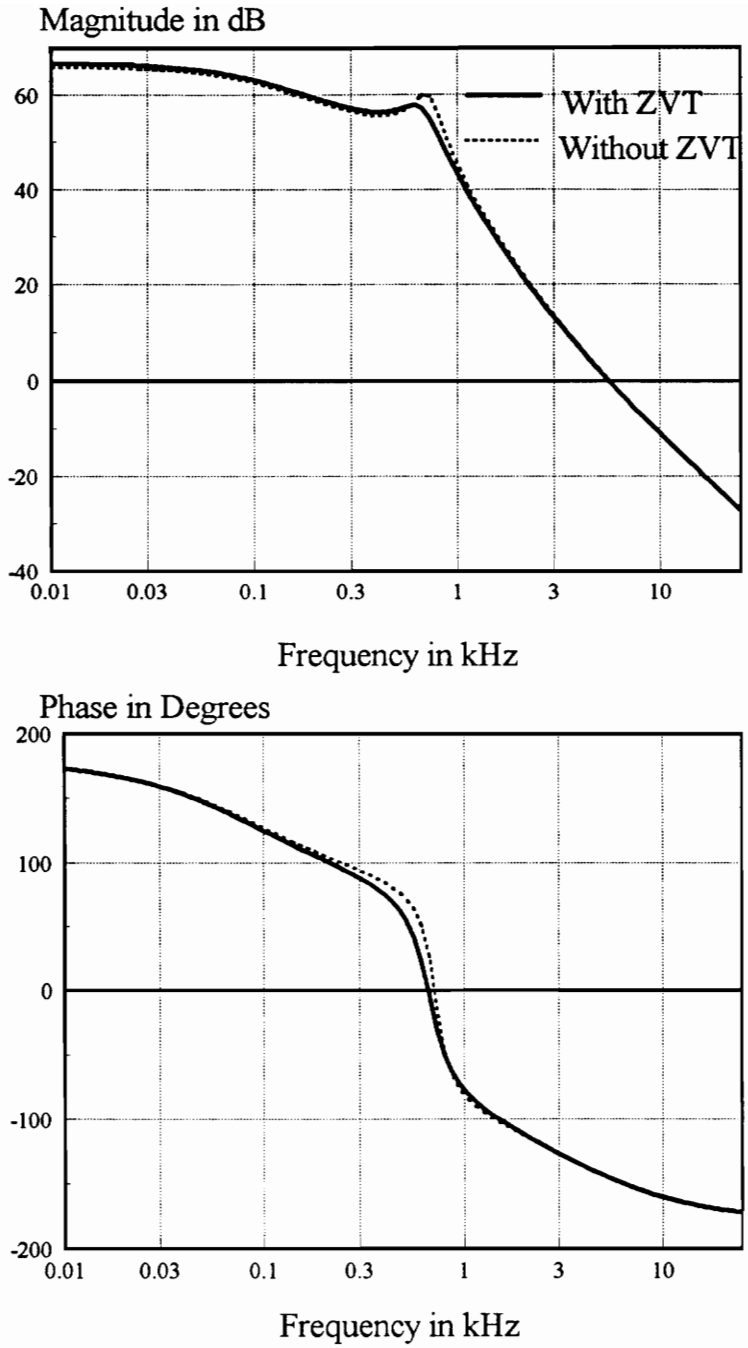


Fig 3.6(c). $\hat{v}_o$ / $\hat{d}_q$ transfer function

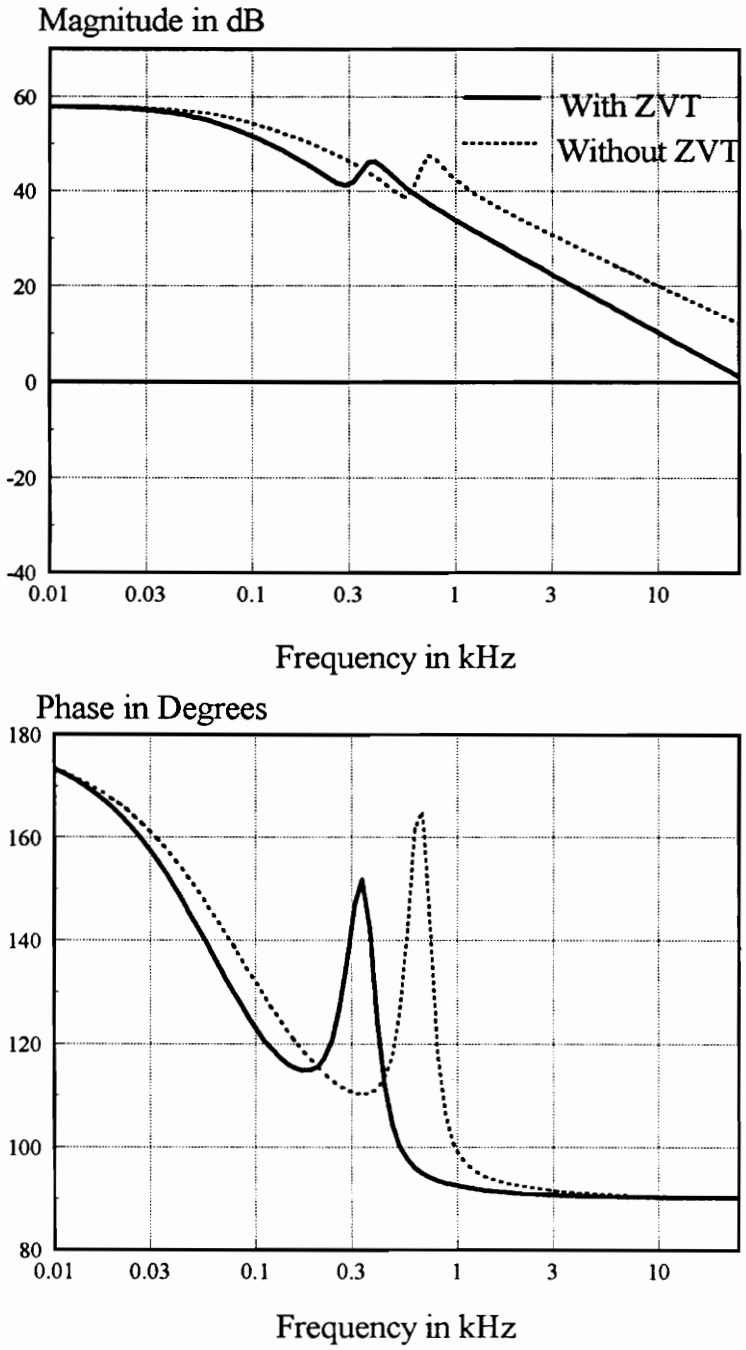


Fig 3.6(d). $\hat{i}_q$ / $\hat{d}_q$ transfer function

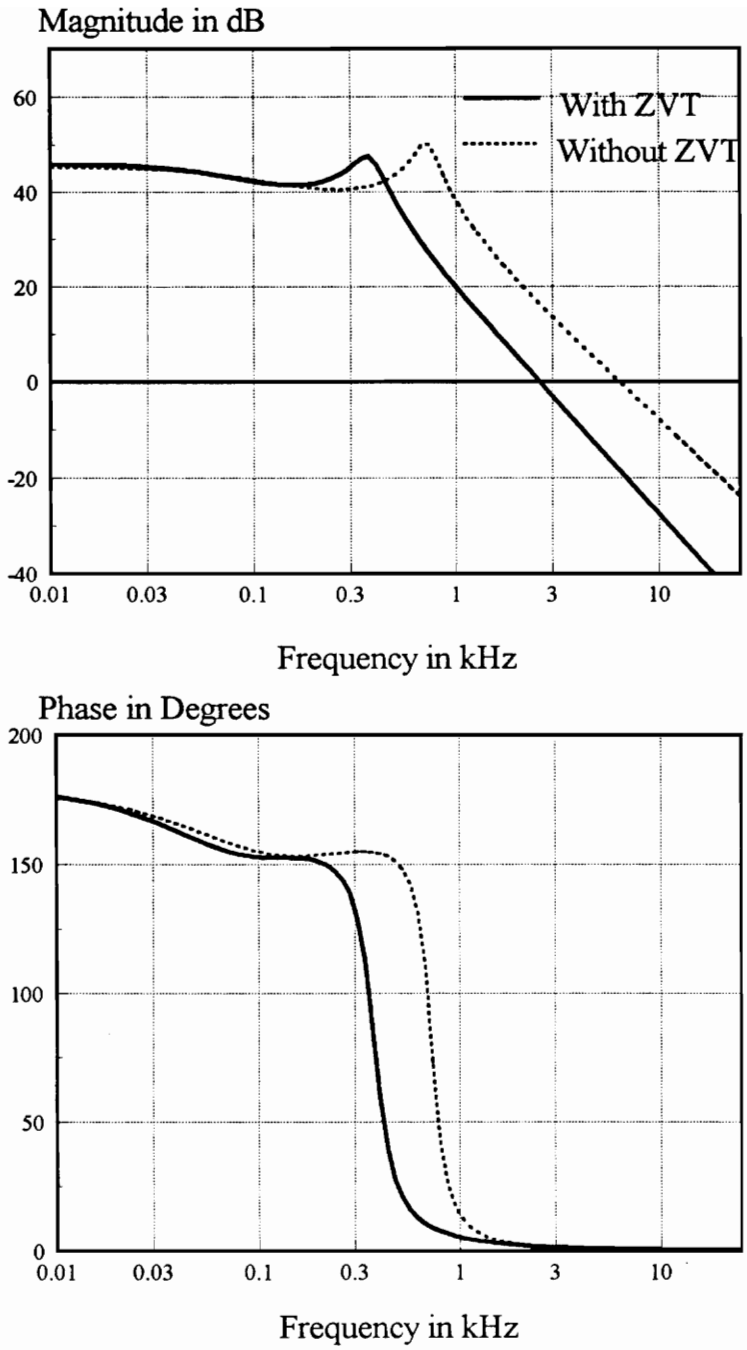


Fig 3.6(e). $\hat{i}_d$ / $\hat{d}_q$ transfer function

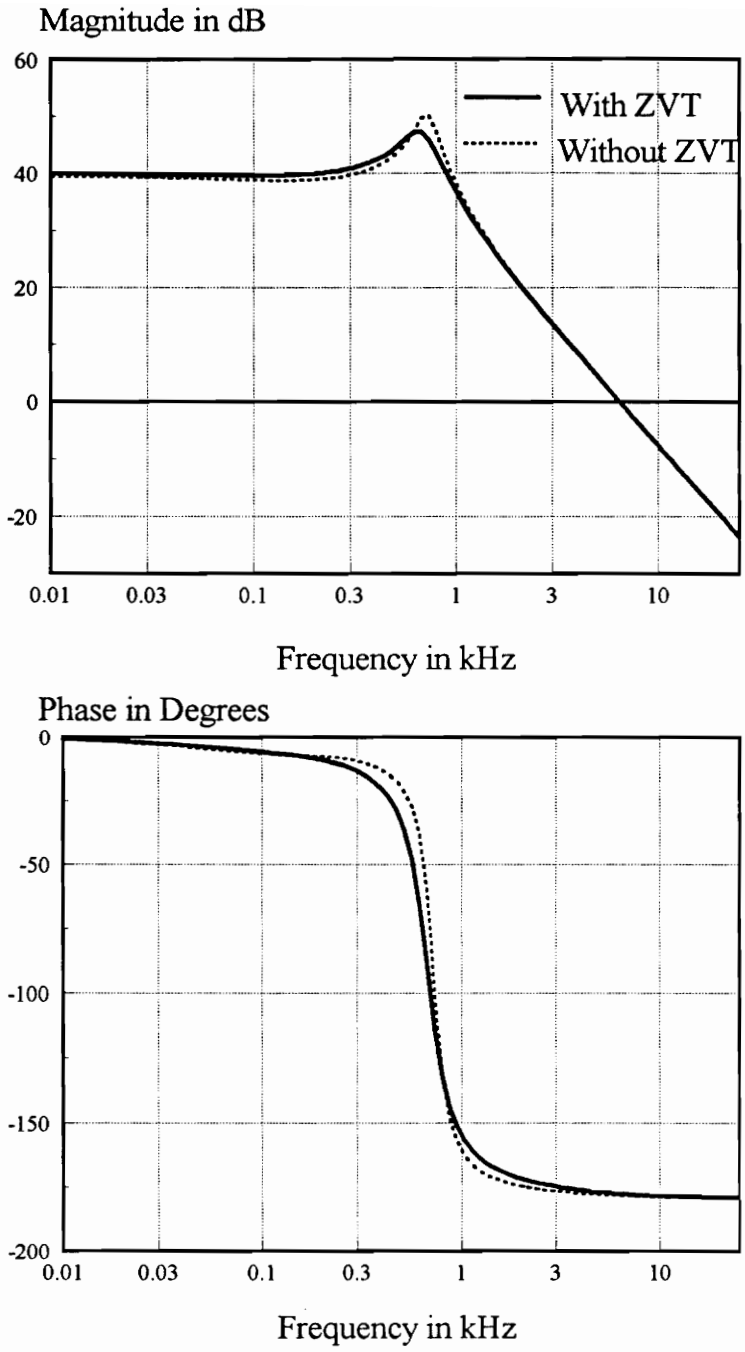


Fig 3.6(f). $\hat{i}_q$ / $\hat{d}_d$ transfer function

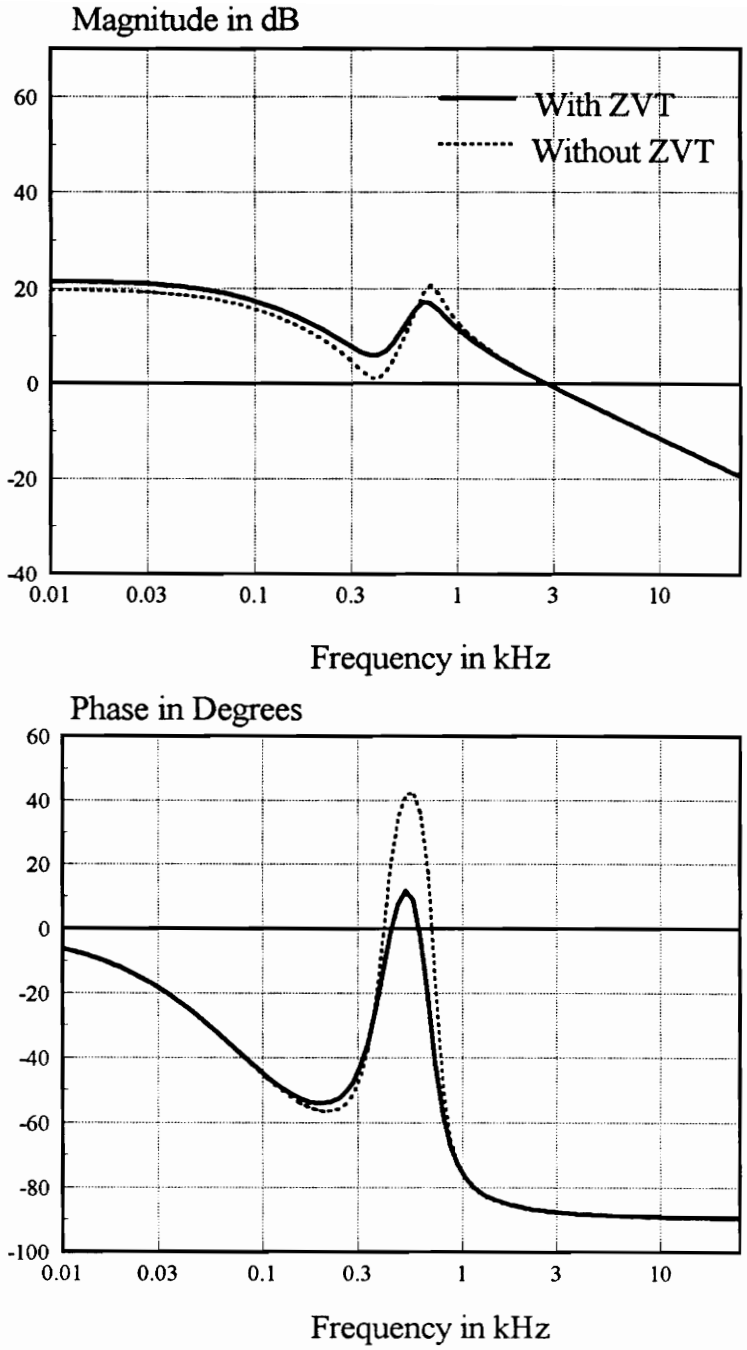


Fig 3.6(g). Output impedance transfer function

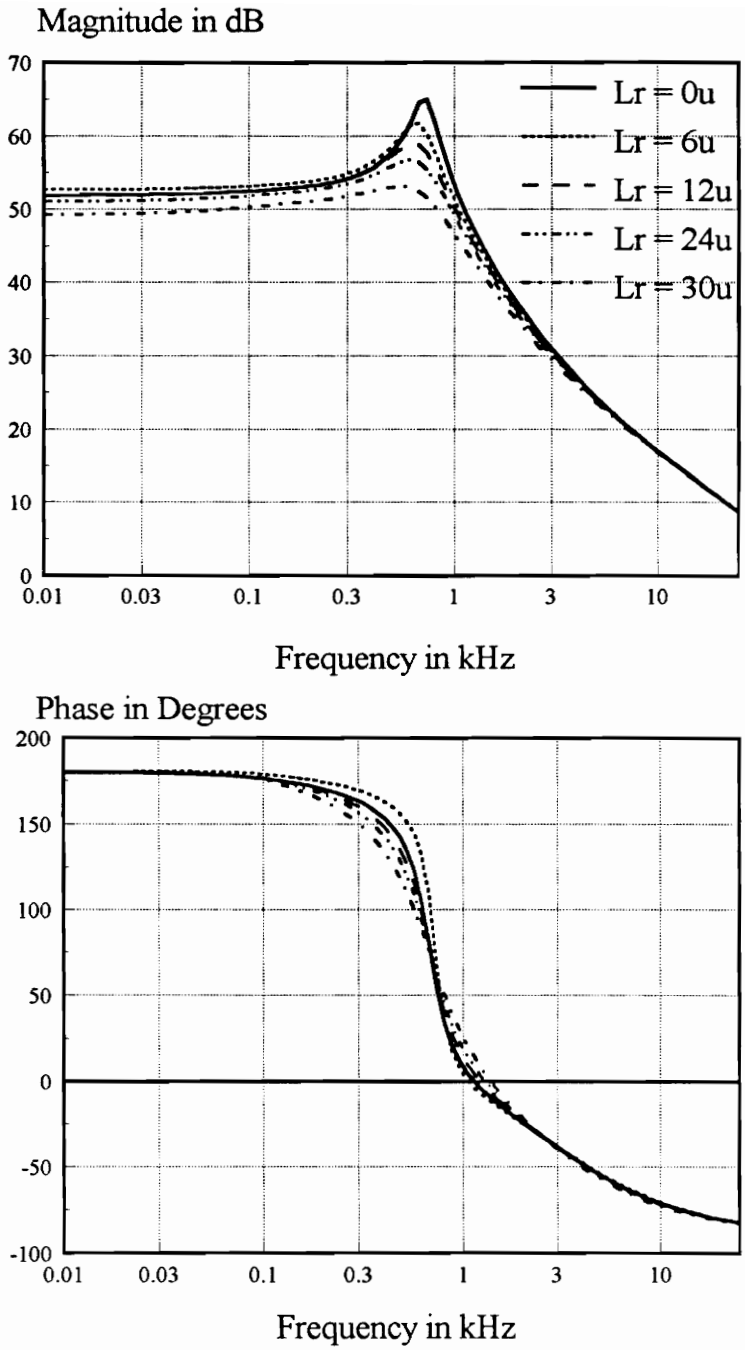


Fig 3.7. $\hat{v}_o$ / $\hat{d}_d$ *transfer functions using different values of Lr*

double pole is first damped and then split as the value of L_r is increased. The ZVT network introduces feedback in $\hat{i}_d$ and $\hat{v}_o$ through $\Delta\hat{d}$ and $\hat{i}_x$. The term proportional to $\hat{v}_o$ in (3.15) results in the change of dc gain in (3.12) while the term proportional to $\hat{i}_d$ in (3.15) introduces damping in (3.12). Similarly, the term proportional to $\hat{i}_d$ in (3.16) affects the dc gain in (3.14) and the term proportional to $\hat{v}_o$ results in damping of (3.14).

3.5 Conclusions

In this section, the existing average model of the standard PWM boost rectifier [7],[8], is modified to include the effect of ZVT. The effect of ZVT is included by using time-averaging equivalent circuit approach. In this, the commutation circuit dynamics are neglected. Also, the capacitor, inductor and the switch resistances have been neglected. It is found that when compared to the standard PWM case, the only changes occur in average line voltages at the bridge input and the current charging the output capacitor. The average model obtained in stationary coordinates is transformed to obtain a time-invariant model in rotating coordinates. The average model in rotating coordinates is linearized and perturbed to obtain a small-signal model. The small-signal characteristics of the ZVT three-phase boost rectifier are compared to the corresponding transfer functions of conventional PWM boost rectifier.

It is shown that small signal characteristics of the three-phase boost rectifier vary appreciably due to ZVT. The ZVT action changes the dc value of the duty cycle and it

inherently introduces feedback from the output voltage and from the direct component of the input current. As a consequence, the maximum duty cycle is limited to some value less than unity and the transfer function damping is significantly increased.

4. Current Loop Modeling and Design

4.1. Introduction

A number of schemes (e.g. hysteresis control, delta modulation, fuzzy control, etc.) have been used in the past to control the phase currents of the three-phase boost rectifier. One of the simplest schemes uses three independent analog control loops [3], shown in Fig. 2.2. However, as pointed out earlier, it is difficult to achieve six-step PWM operation using this control. This scheme can be readily used with ZVT three-phase boost rectifier, due to the presence of the dc-rail diode. The dc-rail inherently provides automatic six-step PWM operation.

In this analog control scheme, the sinusoidal current reference for each phase is generated by the product of voltage compensator output and a signal proportional to the corresponding input phase voltage. This scheme is very similar to the one used in single-phase power factor correction circuit. Hence, three standard PFC chips like UC1854 can be used for controlling each phase current.

The PFC chip, UC1854 (UC2854, UC3854) uses average current mode control to achieve fixed frequency current control with stability and low distortion. This chip has all the necessary control functions like voltage amplifier, current amplifier, frequency

modulator and analog multiplier/divider built inside it. Using three such chips for each of the three independent controllers can considerably reduce the number of components in the circuit, thereby allowing considerable cost reduction and reduced space utilization. The independent analog current control scheme using UC1854 is shown in Fig. 2.3. This scheme has already been described in Section 2.2. In this chapter, the modeling approach of this scheme will be discussed using the average model. The procedure for designing the average current controller will be illustrated. The drawbacks of this scheme will be discussed and the improvements and alternative approaches will be investigated through simulations of average models. Two interesting cases of the feedforward gain will be simulated in order to obtain the feedforward gain.

4.2. Modeling Approach

The power stage model of the ZVT three-phase boost rectifier was developed in the preceding chapter in rotating coordinates. Hence, irrespective of the control approach used, the power stage model should have control inputs in rotating d-q coordinates.

The modeling approach for the controller is shown in Fig. 4.1. In this approach, the three phase currents are rectified and scaled by the current sensor gain and fed to an error amplifier. (If the phase currents are not accessible, then the power stage currents in rotating coordinates, i_d and i_q, are inverse transformed to obtain currents in stationary coordinates, i_a, i_b and i_c). The other input to the error amplifier is the reference created

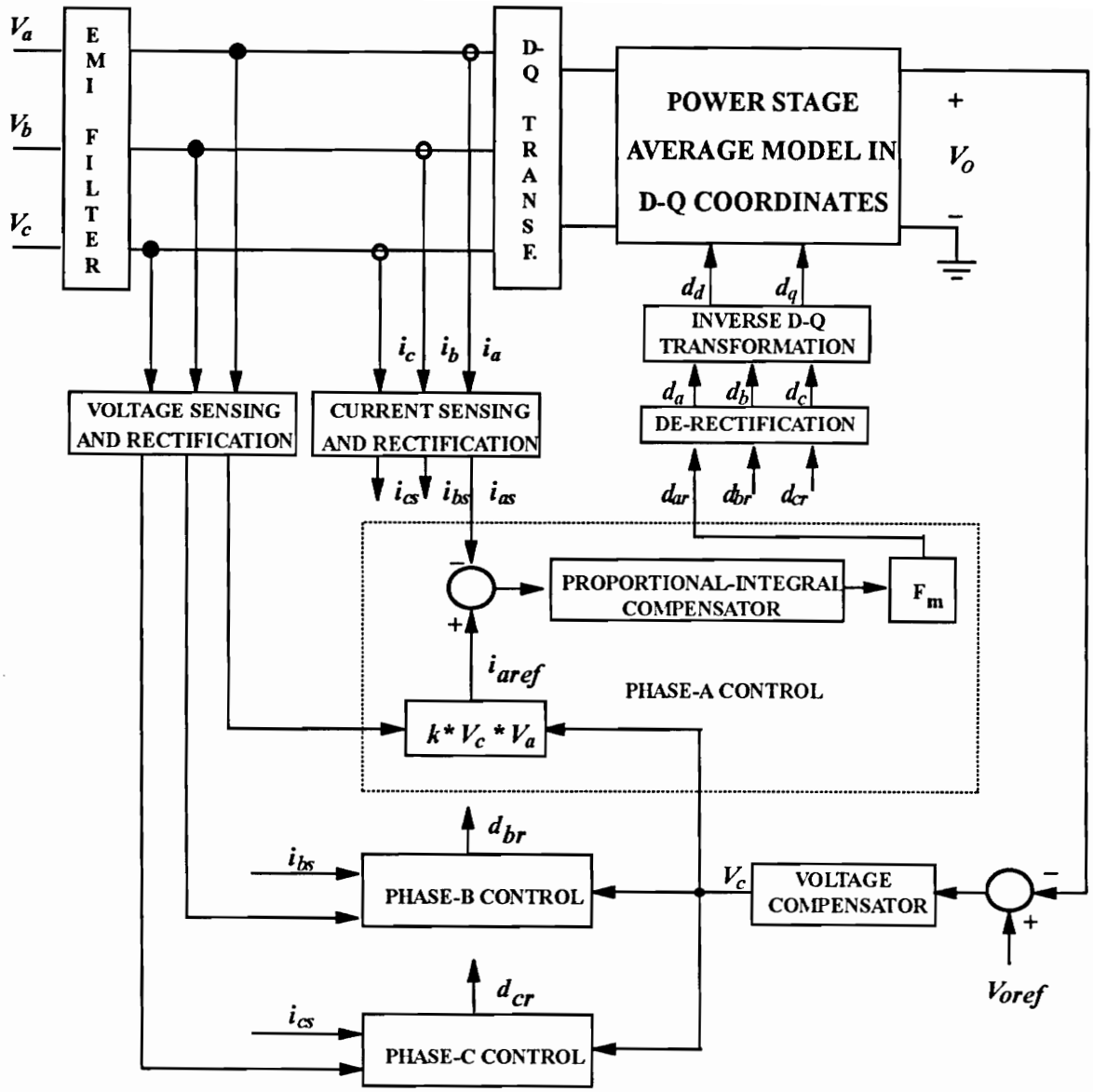


Fig. 4.1 Modeling approach for controller using UC1854

from the output of the voltage compensator, v_c, and the corresponding sensed and rectified input phase voltage scaled by a factor k, which is the internal gain of the chip. The output of the error amplifier is fed to a proportional - integral (PI) compensator. The output of the three PI compensators should be de-rectified and scaled by the modulator gain F_m, to obtain the phase duty cycles in stationary coordinates d_a, d_b and d_c. Since the control inputs to the power stage model should be in rotating coordinates, d_a, d_b and d_c are transformed to control inputs in rotating coordinates d_d and d_q.

4.3 Current Controller Design

The controller modeled in Fig. 4.1 is designed using the same approach as in [10]. However, the control design is easier with soft-switching since, as observed in chapter 3, ZVT introduces significant damping in open-loop transfer functions. Moreover, the standard design approach, [10], can still be used with soft-switching.

The state-space model of the compensators is written in line-to-line variables. The equations describing line ab current controller are [10]:

$$\begin{aligned} \frac{du_{iab}}{dt} &= \frac{d(u_{ia} - u_{ib})}{dt} = -3K_i F_m e_{ab} \\ d_{ab} &= u_{iab} - 3K_p F_m e_{ab} \\ e_{ab} &= R_i(i_{abref} - i_{ab}) \\ i_{abref} &= k v_{ab} v_c / (3n) \end{aligned} \tag{4.1}$$

where $i_{abref} = i_{aref} - i_{bref}$, R_i is the current sensor gain, k is the internal gain of the chip, n is the voltage sensing transformer turns ratio, u_i is the output of the integrator in the PI compensator, v_c is the output of the voltage compensator, K_p is the current compensator proportional gain, K_i is the current compensator integral gain, and F_m is the modulator gain. The equations for other two lines are same as (4.1) with change in subscripts.

For design purpose, it is essential to transform the three current controllers to d-q reference frame, [10]. The model obtained for the controller in d-q reference frame is as shown in Fig. 4.2, [10], where e_d and e_q are the errors e_{ab}, e_{bc}, and e_{ca} transformed to rotating d-q reference frame, and are given by:

$$\begin{aligned} e_d &= R_i(i_{dref} - i_d), \\ e_q &= R_i(i_{qref} - i_q) \end{aligned} \tag{4.2}$$

where $i_{dref} = kV_m v_c/(3nR_i)$ and $i_{qref} = 0$ are current references in d-q coordinate frame. The complete model of the converter in d-q rotating coordinates is shown in Fig. 4.3. Using this model, the compensator is designed following the guidelines listed below:

1) Choose a desired bandwidth, normally between one-fifth and one-half of the switching frequency, f_s.

The bandwidth of the current loop is determined by the pole given by [10]:

$$p = -\frac{1}{3L} K_p F_m R_i V_o \tag{4.3}$$

Knowing the bandwidth, the proportional gain, K_p can be calculated from (4.3).

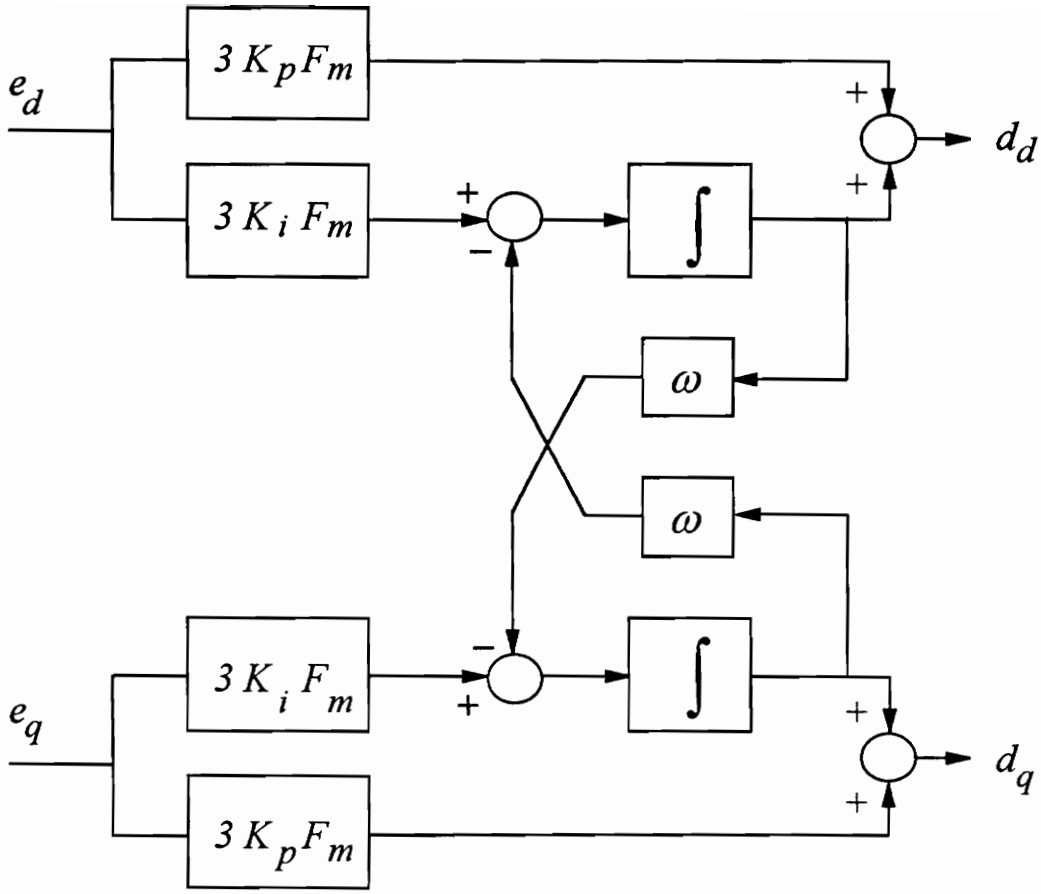


Fig. 4.2 Current compensator model in d-q coordinates

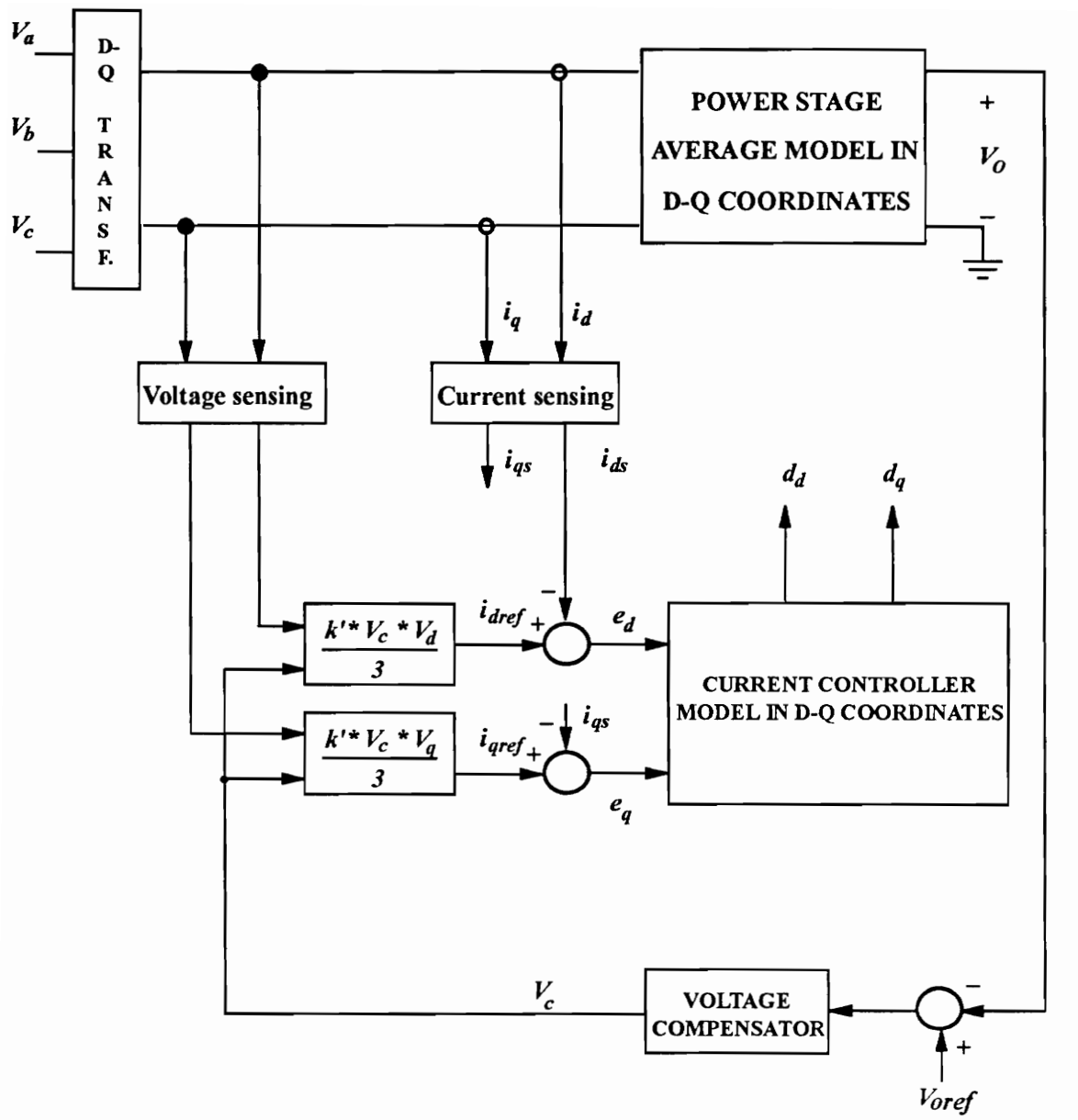


Fig. 4.3 Complete average model in d-q coordinates

2) Choose K_i so that cross-coupling is reduced below the desired level. The cross-coupling rejection at dc depends on K_p and K_i. After selecting K_p, K_i can be determined to reduce the cross-coupling below the desired level.

The design is based on the closed loop direct transfer functions, $G_{dd} = \hat{i}_d / \hat{i}_{dref}$ and $G_{qq} = \hat{i}_q / \hat{i}_{qref}$ and the closed loop cross transfer functions, $G_{dq} = \hat{i}_q / \hat{i}_{dref}$ and $G_{qd} = \hat{i}_d / \hat{i}_{qref}$, [10]. A good control design will provide good regulation of input currents, $G_{dd} \approx 1$ and $G_{qq} \approx 1$, and high rejection of cross-coupling, $G_{qd}/G_{dd} \approx 0$ and $G_{dq}/G_{qq} \approx 0$.

The use of Saber simulator simplifies the design to a great extent if the "vary" command is used:

1) Vary the proportional gain, K_p and plot a series of curves for the direct transfer functions. From these plots, choose the value of K_p satisfying the required bandwidth.

2) Vary the integral gain, K_i and plot a series of curves for the cross-transfer functions. From these plots, choose the value of K_i satisfying the required reduction in cross-coupling.

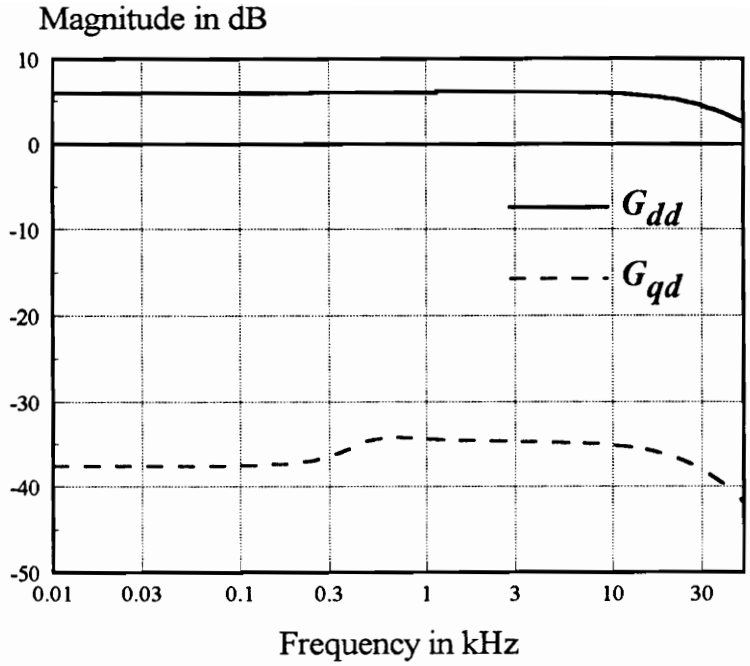
Using the above procedure, the controller was designed for a 6 kW converter. The controller was designed to obtain a bandwidth of around 20 kHz. (Controller and power stage parameters are in Appendix A).

4.4 Closed Loop Transfer Functions

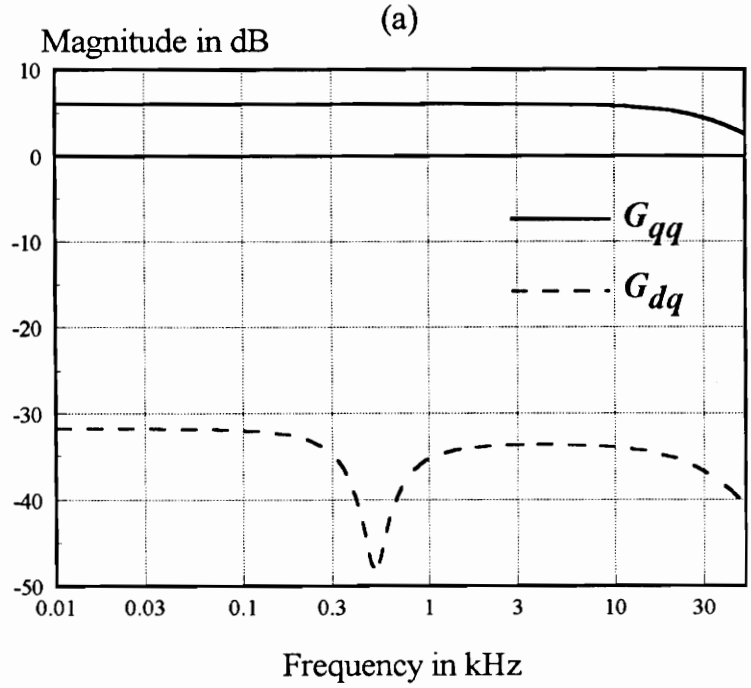
The closed loop average model discussed in Section 4.2 and shown in Fig. 4.1 is implemented in Saber simulation software and simulated for the parameters shown in Appendix A.

The current controller was designed using the guidelines listed in previous section. The desired direct and cross transfer functions are as shown in Fig. 4.4(a) and (b) for i_d and i_q respectively. Also, the design procedure using Saber model (discussed in previous section) is illustrated in Fig. 4.4(c) and (d). In Fig. 4.4(c), K_p is varied and the direct transfer function, G_{dd} is plotted. The value of K_p satisfying the required bandwidth is chosen. In Fig. 4.4(d), K_i is varied and the cross-transfer function, G_{dq} satisfying the required reduction in cross-coupling is chosen. The designed controller parameters are listed in Appendix A.

The transfer functions of interest are control to output voltage, $\hat{v}_o/\hat{v}_c$, control to direct component of the input current, $\hat{i}_d/\hat{v}_c$, control to quadrature component of the input current, $\hat{i}_q/\hat{v}_c$ and the output impedance. The closed loop transfer functions are as shown in Figs. 4.5 to 4.8. From Fig. 4.5 it is observed that the control to output transfer function resembles the corresponding transfer function of dc/dc boost converter with a low-frequency pole and a right-half plane zero. This makes the voltage compensator design as straightforward as in the case of dc/dc converter. The output impedance with

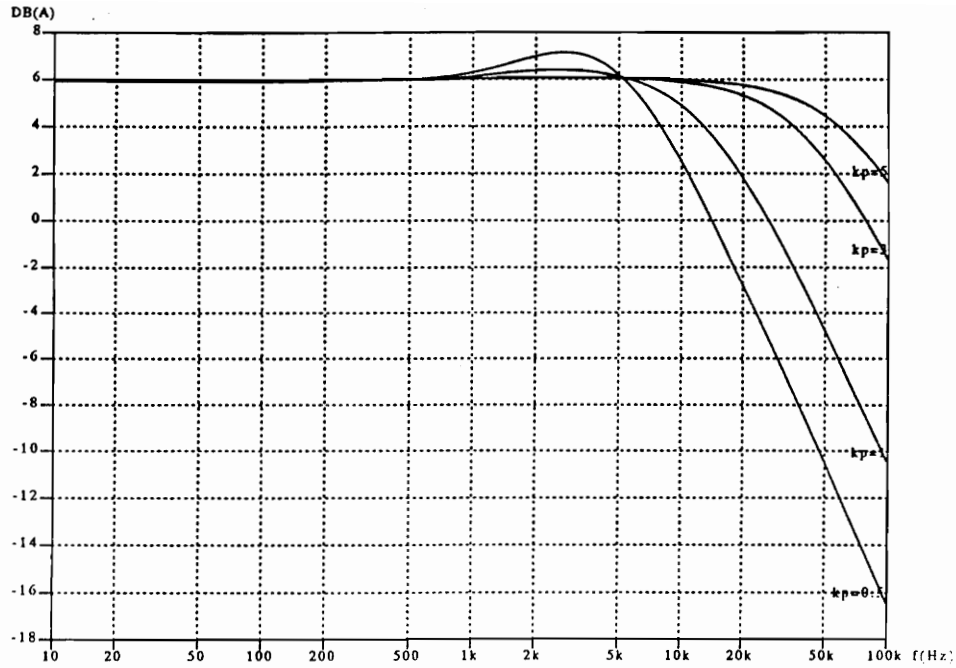


(a)

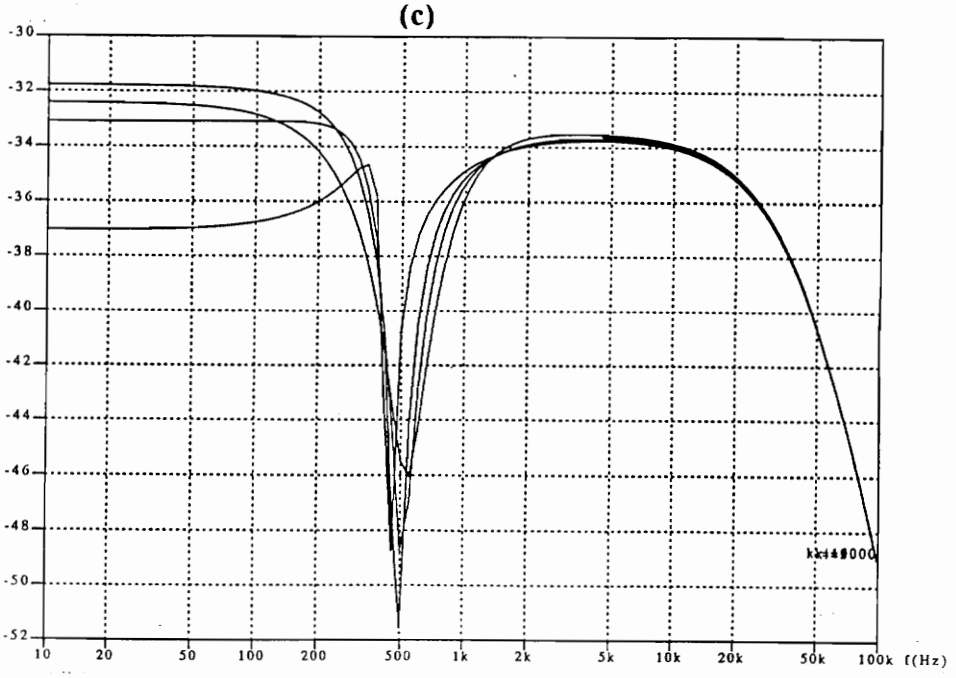


(b)

Fig 4.4. Direct and Cross Transfer functions for (a) $\hat{i}_d$ and (b) $\hat{i}_q$



(c)



(d)

Fig 4.4. Compensator design using Saber (c) G_{dd} and (d) G_{dq}

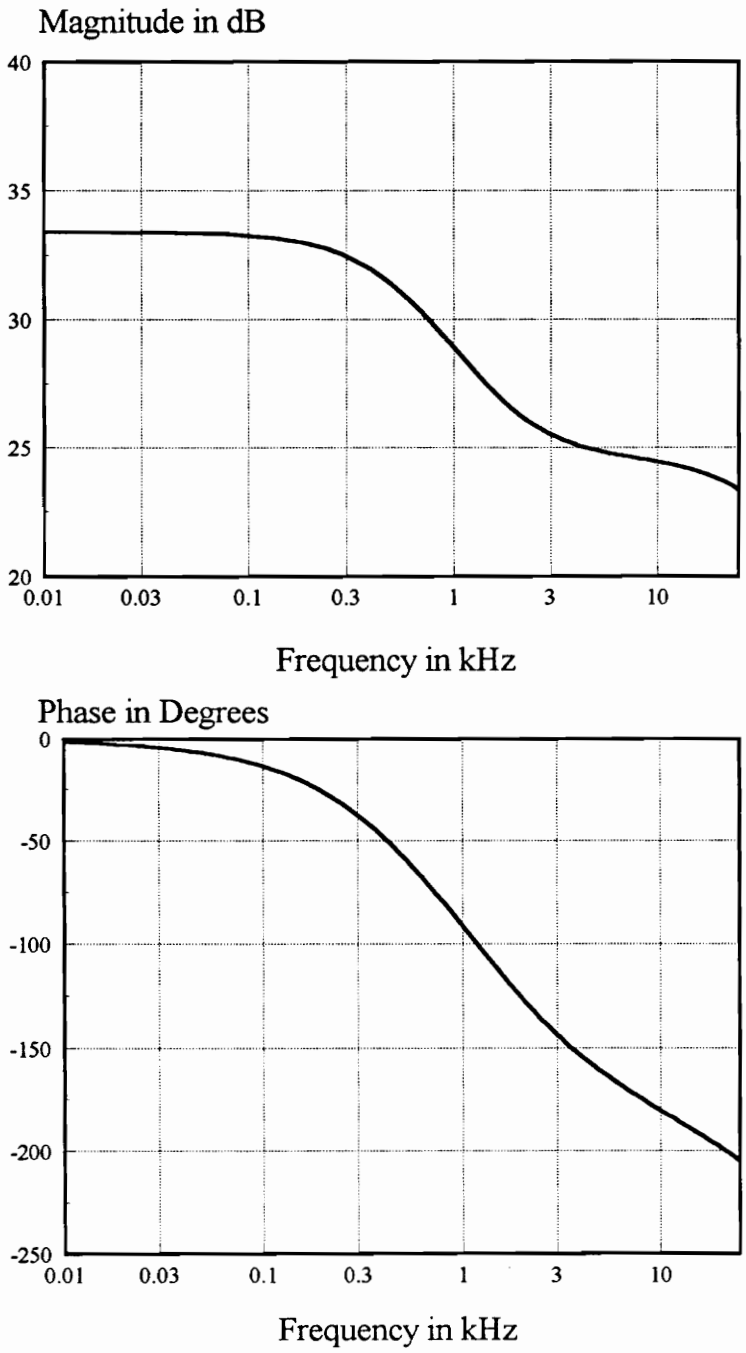


Fig 4.5. Control to output transfer function with closed current loop

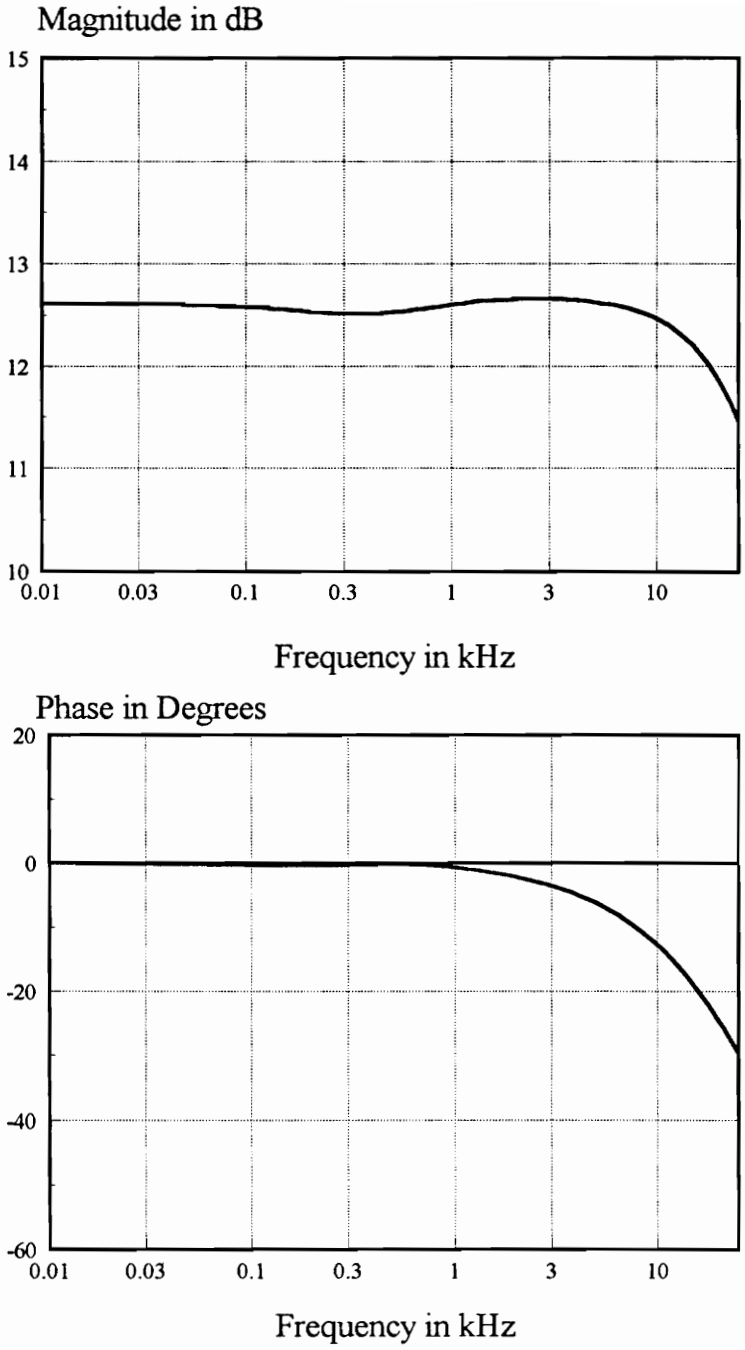


Fig. 4.6 Control to $\hat{i}_d$ transfer function with closed current loop

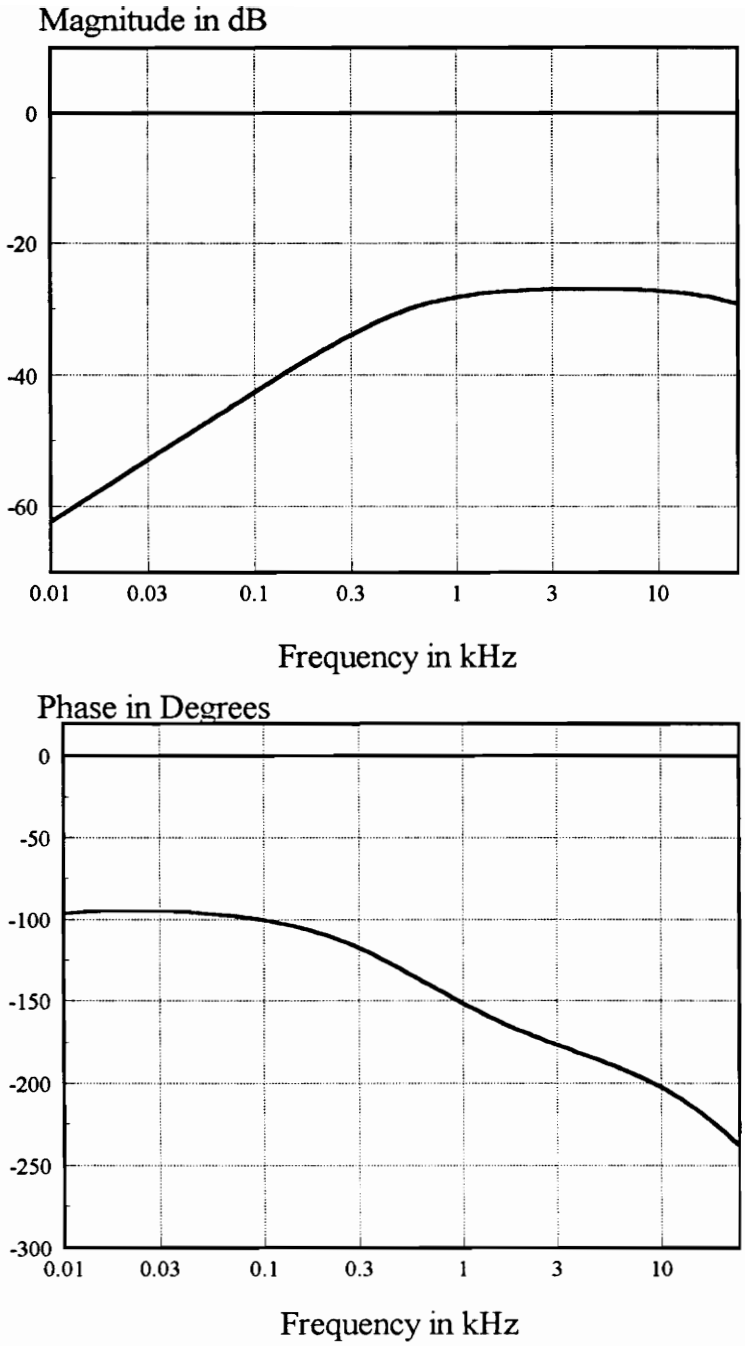


Fig. 4.7 Control to $\hat{i}_q$ transfer function with closed current loops

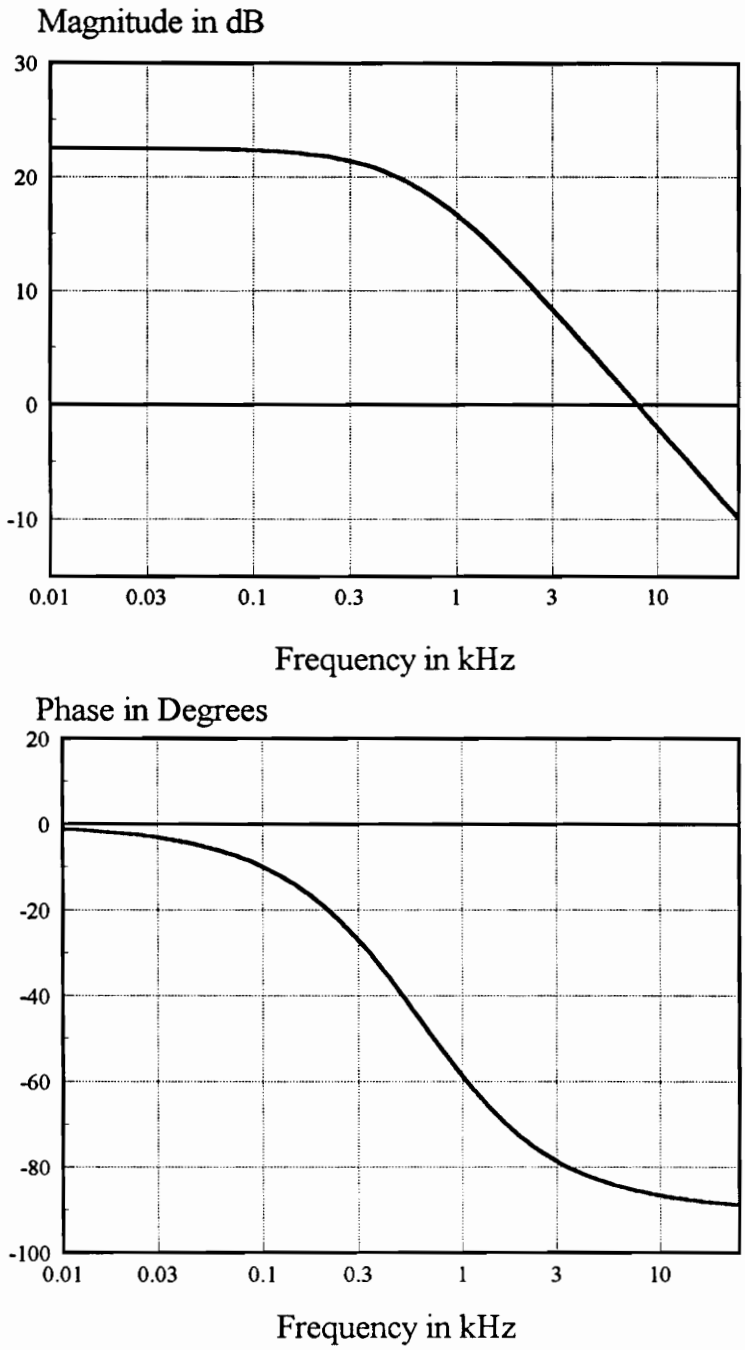


Fig 4.8 Output Impedance with closed current loops

closed current loops is higher than the open-loop output impedance. Fig. 4.6 shows the current loop bandwidth to be around 20 kHz.

4.5 Large Signal Analysis

The closed loop average model shown in Fig. 4.1 is simulated for the parameter values listed in Section 4.4. The simulated waveforms of the input phase current, and the compensator output are as shown in Fig. 4.9 for one phase. Severe distortions are observed in the current waveforms at all zero-crossings.

Since the controller using UC1854 PFC chip requires rectification of sensed input currents and voltages, additional circuitry is needed to distribute the modulator outputs to the upper or lower switches in the bridge, depending on the polarity of the corresponding input voltage. The swapping of the signals to the upper and lower switches is performed by the switch-decoder block shown in Fig. 2.3. The switch-decoder block has to swap the signals at the modulator output whenever the feedback sign changes at zero-crossings due to rectification of the current error signal. In other words, whenever the feedback sign changes due to change in polarity of current error signal (at zero-crossings due to rectification), the switch-decoder block has to swap the signals at the modulator output. If the two actions are not performed simultaneously due to the transient time required by the controller, the swapping signal issued by switch-decoder block will not correspond to the feedback sign. Hence, severe distortions will arise in the current waveforms.

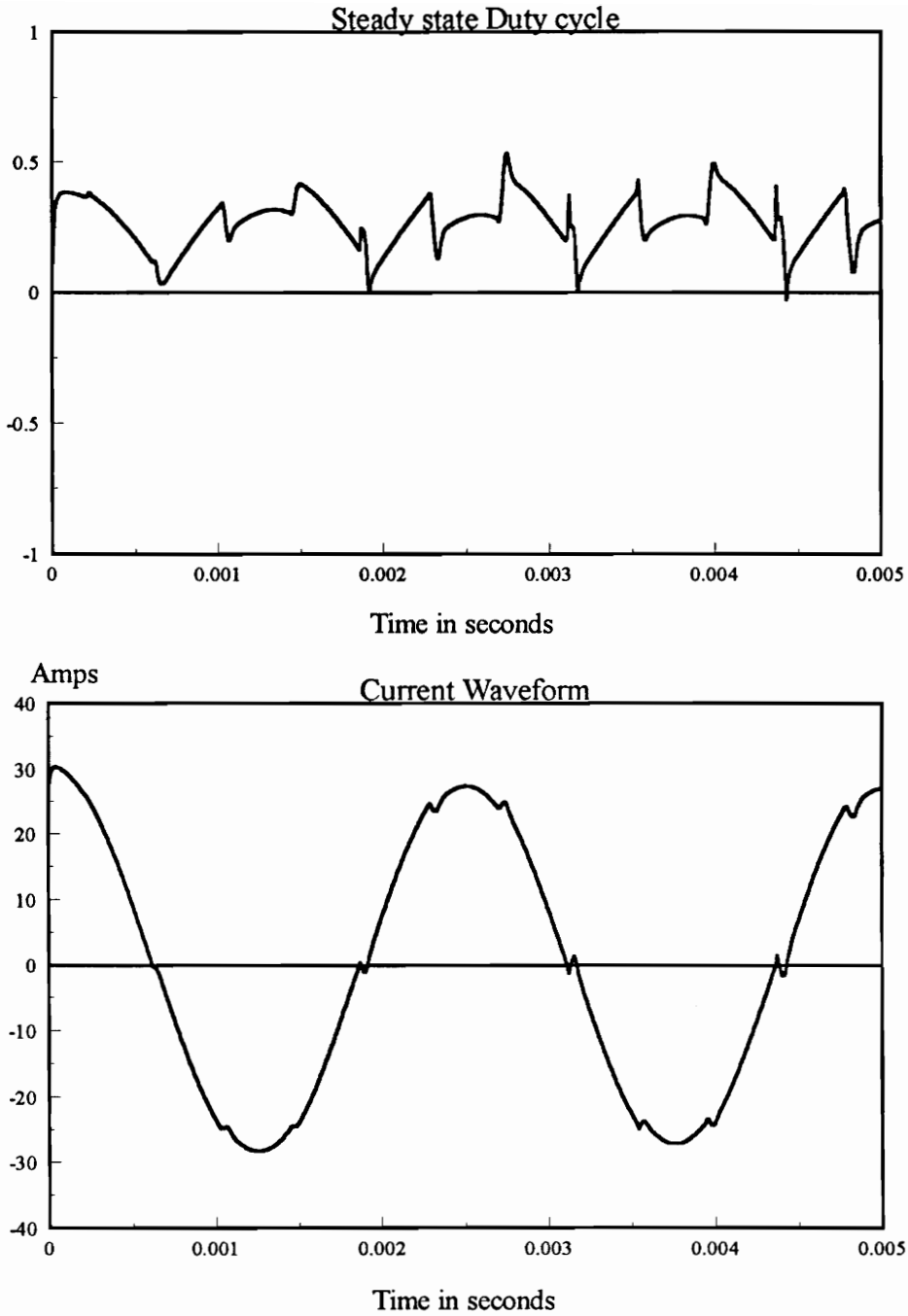
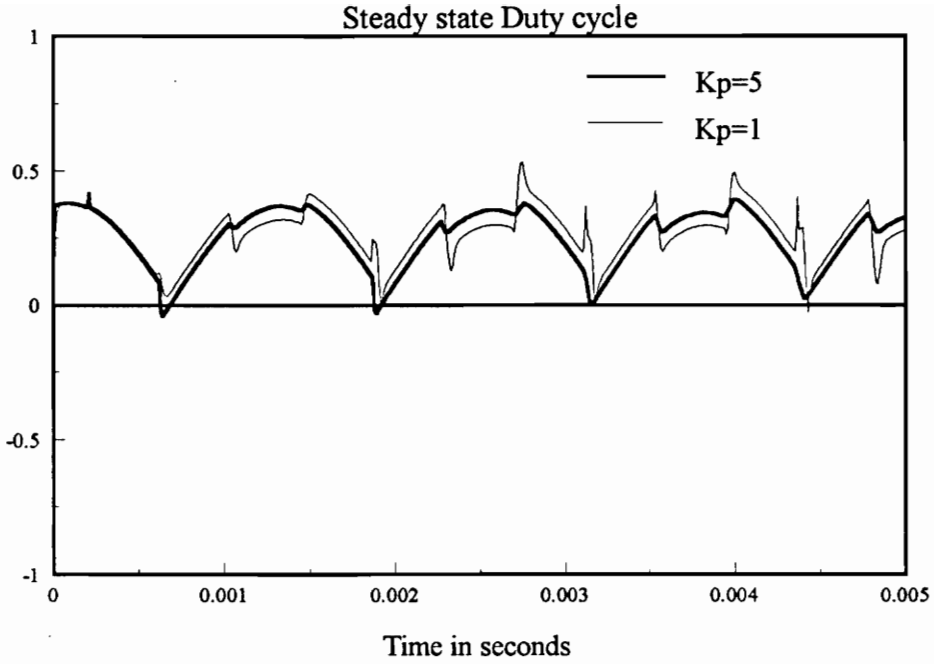


Fig.4.9 Steady state duty cycle and current

In the model shown in Fig. 4.1, the de-rectification block performs similar function as the switch-decoder block. Whenever the feedback sign changes at zero-crossings, the de-rectification block has to change the polarity of the controller outputs. But due to the transient time required by the controller, there will exist some time-interval during which the de-rectification block will not conform to feedback sign and severe distortions will arise in current waveforms. The distortion in one current waveform at its zero-crossing will create distortions in the other two current waveforms since the three phase currents always sum up to zero.

The distortions in the current waveforms can be reduced by increasing the proportional gain, K_p, (which is directly related to the bandwidth). By increasing K_p, the transient time required by the controller to conform to the feedback sign will reduce and the distortions will reduce. Fig. 4.10 shows the improvement in compensator output and phase current when the bandwidth is increased. However, there is a practical limitation to increase in bandwidth. Increasing proportional gain makes the circuit more susceptible to noise. Hence, there has to be some trade-off between the desired bandwidth and the distortions in currents. This is the major limitation of this control approach. Hence, it is concluded from this observation that when the controller inputs are rectified, severe distortions can arise in the input current waveforms at all zero-crossings.

One possible solution to this problem is to use discrete op-amps and analog multipliers/dividers to obtain the same functions obtained in the PFC chip. The main advantage is that the sensed current signal and the voltage reference need not be rectified.



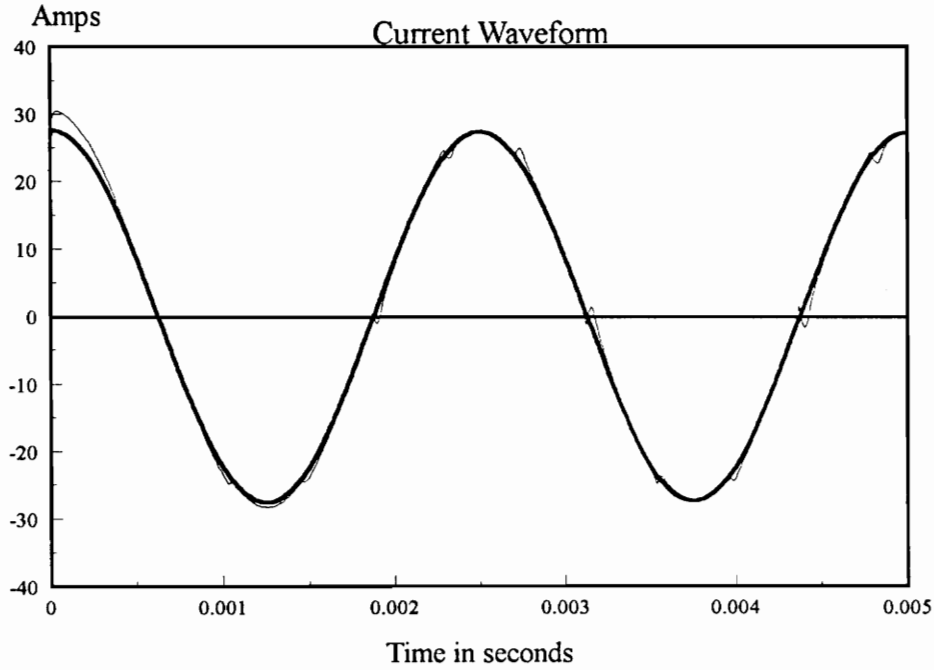


Fig. 4.10 Improvement in waveforms with increase in Kp

This eliminates the input current distortions at zero crossings. Simulated waveforms in Fig. 4.11 show that the steady state duty cycles (and hence the current waveforms) are significantly improved when error signal is not rectified, for the same control bandwidth. For the circuit parameters listed in Appendix A, the proportional gain of the controller has to be increased by at least five times in order to get comparable current waveforms with rectification of error signals. Increasing the proportional gain by five times is not practicable since the bandwidth will then become close to the switching frequency (as seen in Fig. 4.4(c)). On the other hand, the second approach needs large number of analog multipliers/dividers for its implementation. This significantly increases the cost and space utilization besides the complexity. Additional factors arising when the error signal is not rectified due to the modulator ramp cannot be investigated with average model. These factors have been investigated further in Chapter 5 with the switching model.

The modeling approach for the type of controller using discrete components is same as the one using PFC chip, and is shown in Fig. 4.12. The crucial difference is that none of the sensed signals are rectified. Hence, the outputs of the three PI compensators scaled down by the modulator gain directly give the duty cycles d_a, d_b and d_c and there is no need for de-rectification of error signals. These control inputs are then transformed to control inputs in rotating coordinates, d_d and d_q. Since this average model does not involve de-rectification, the simulated current waveforms will not have any distortions.

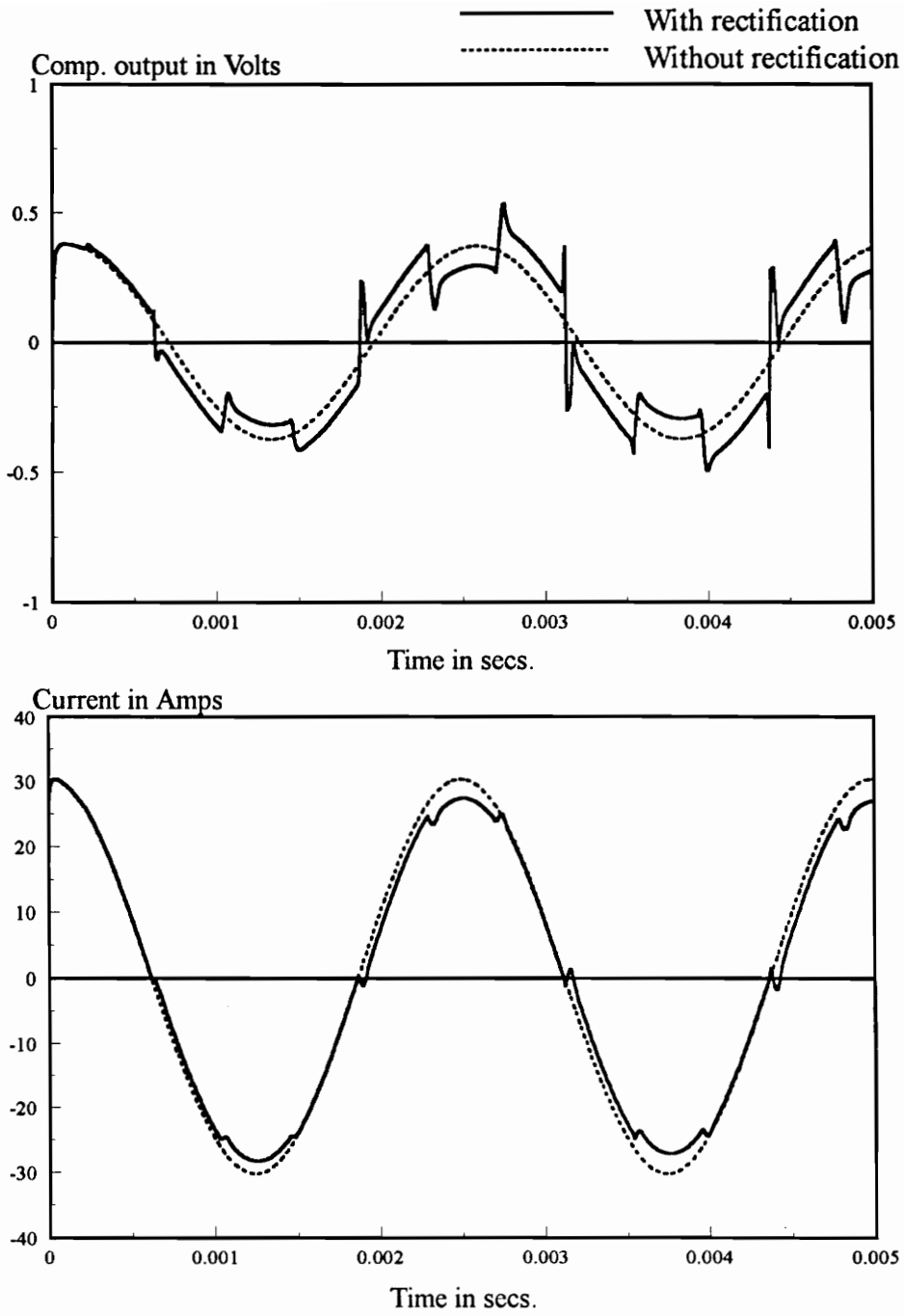


Fig. 4.11 Improvement without rectifcation of error signals

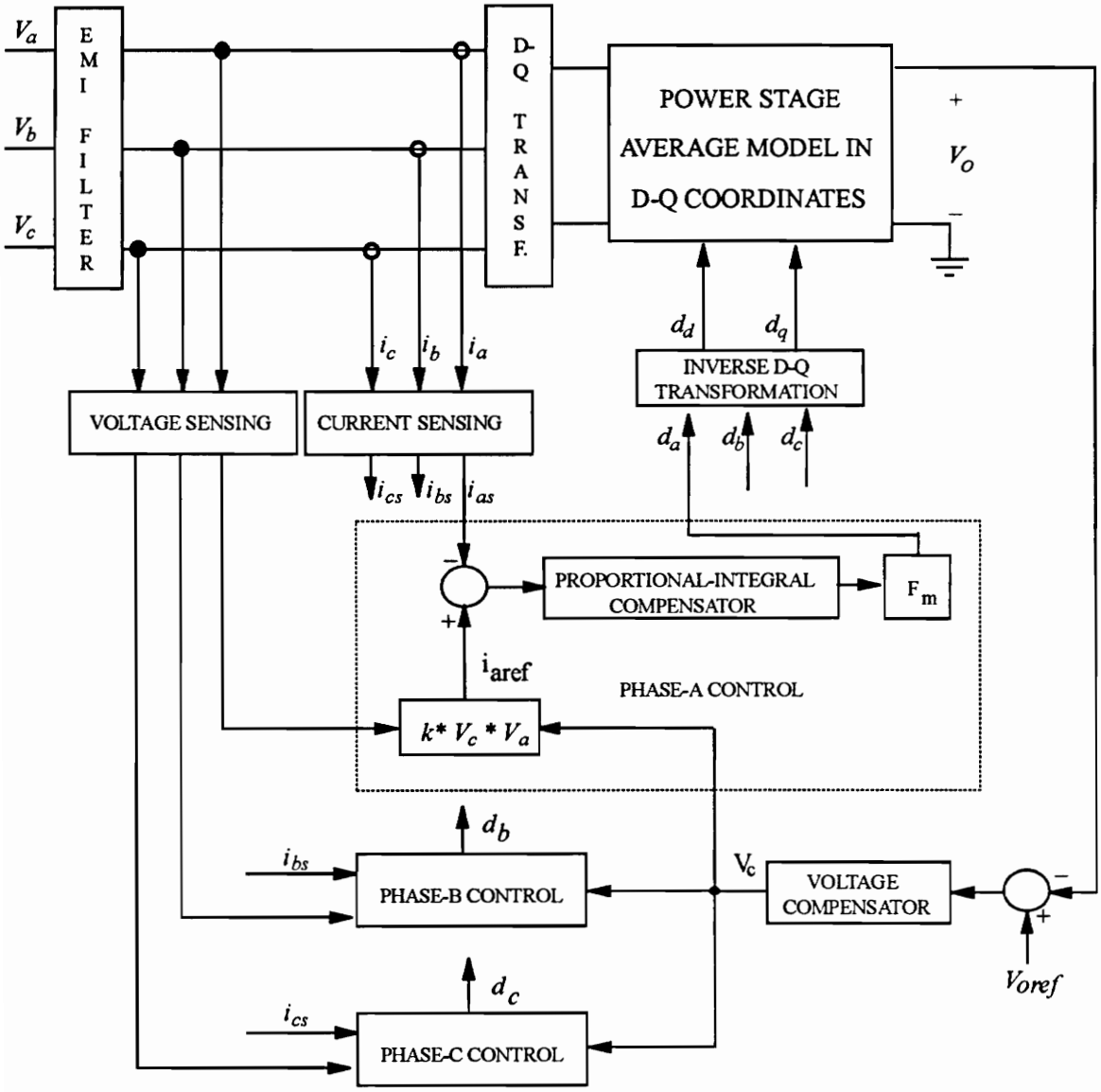


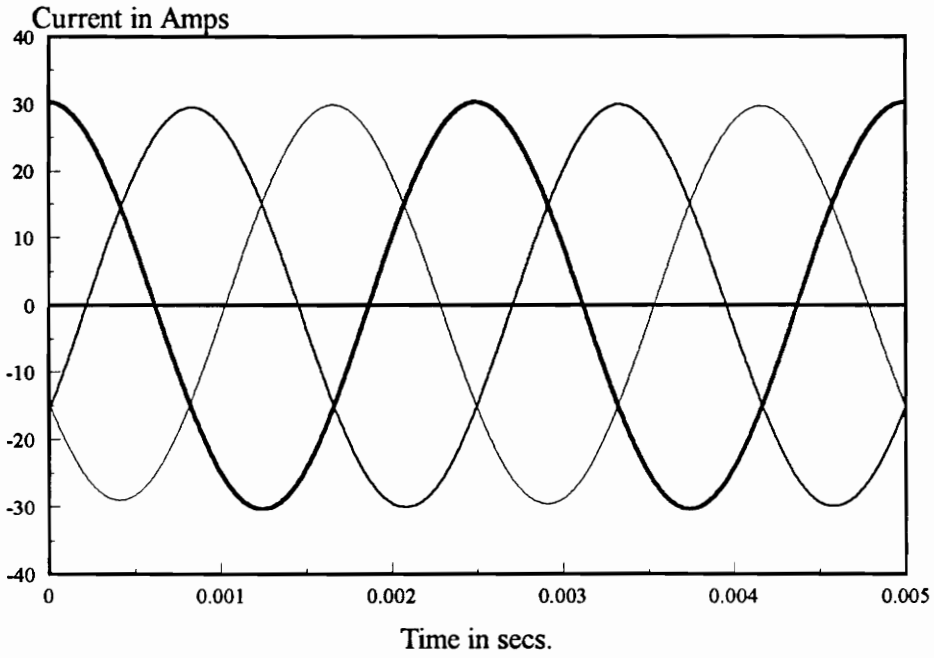
Fig. 4.12 Modeling approach for controller using discrete components

4.6 Feedforward action

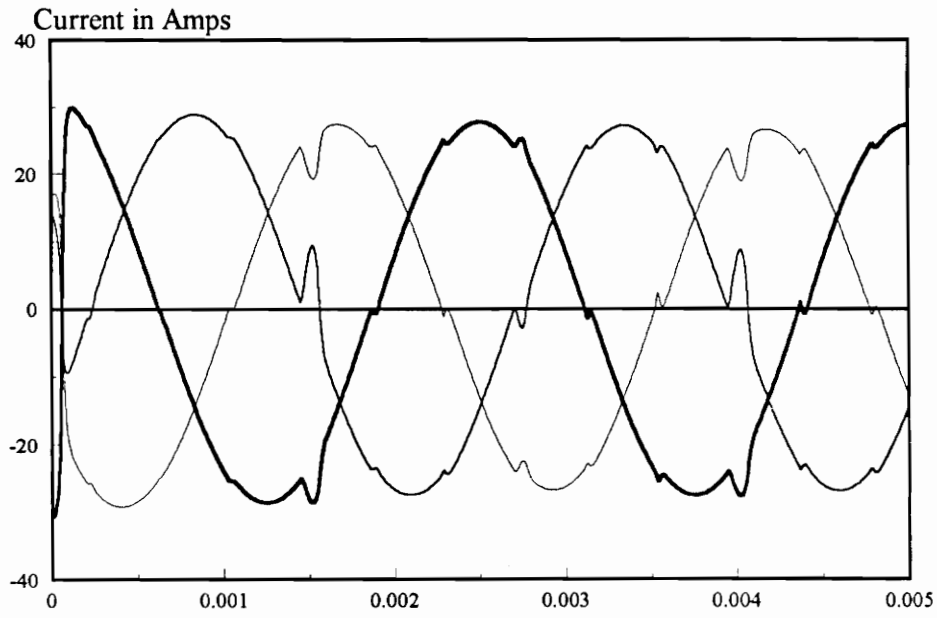
When the closed loop average model discussed in previous sections is operated under conditions of three percent imbalance in amplitude of phase voltages, then the current waveforms without rectification of error signals is as shown in Fig. 4.13(a). If the error signals are rectified, then the current waveforms deteriorate even more under the conditions of imbalance, as shown in Fig. 4.13(b). However, as shown in Fig. 4.13(c), the output voltage ripple is very high in both cases. To solve this problem and to compensate for changes in output voltage due to changes in input voltage, a feedforward term should be introduced. The current reference with feedforward is modified. The reference for phase a will be :

$$i_{aref} = \frac{k v_a v_c}{n v_{ff}} \tag{4.4}$$

In equation (4.4), i_{aref} is the current reference to phase a controller, k is the internal gain of the chip, n is the voltage sensing transformer turns ratio, v_c is output of the voltage compensator. v_{ff} is the feedforward gain. The choice of feedforward is critical in this type of controller. Several configurations of feedforward can exist. In order to obtain the feedforward gain which gives the best results, two prominent cases of feedforward are studied, namely $v_{ff} = (v_{arms})^2$ and $v_{ff} = (v_{arms})$, using the modified closed loop average model shown in Fig. 4.14 with $v_{ff} = (v_{arms})$. The output voltage waveform under these



(a)



(b)

Fig. 4.13 Comparision with imbalance (a) without (b) with rectifcation

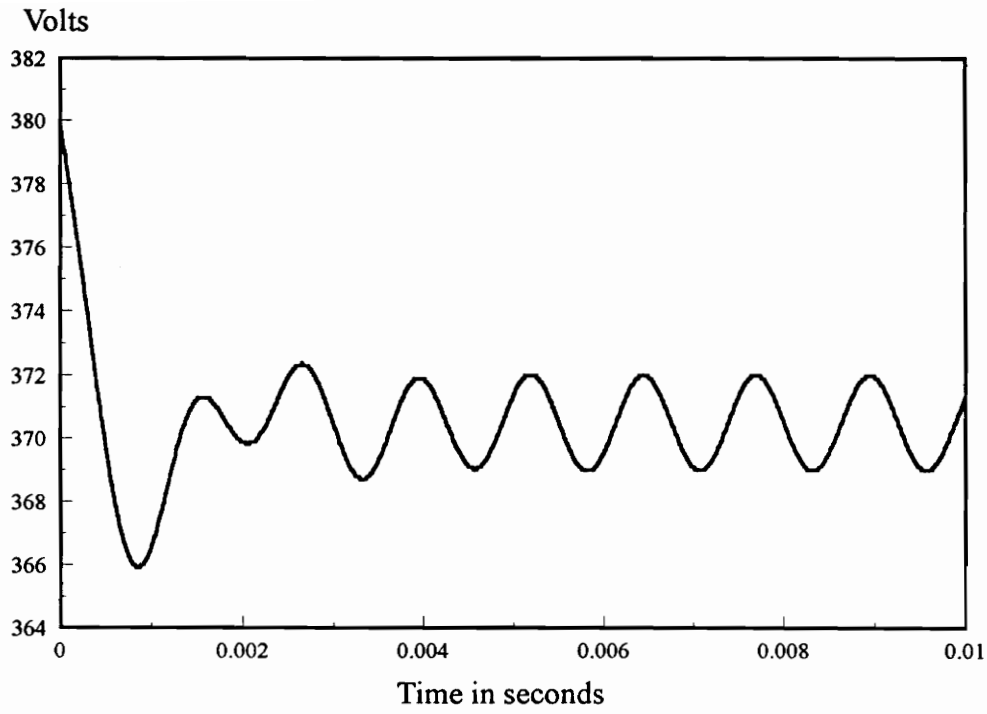


Fig. 4.13(c) Output voltage with imbalance

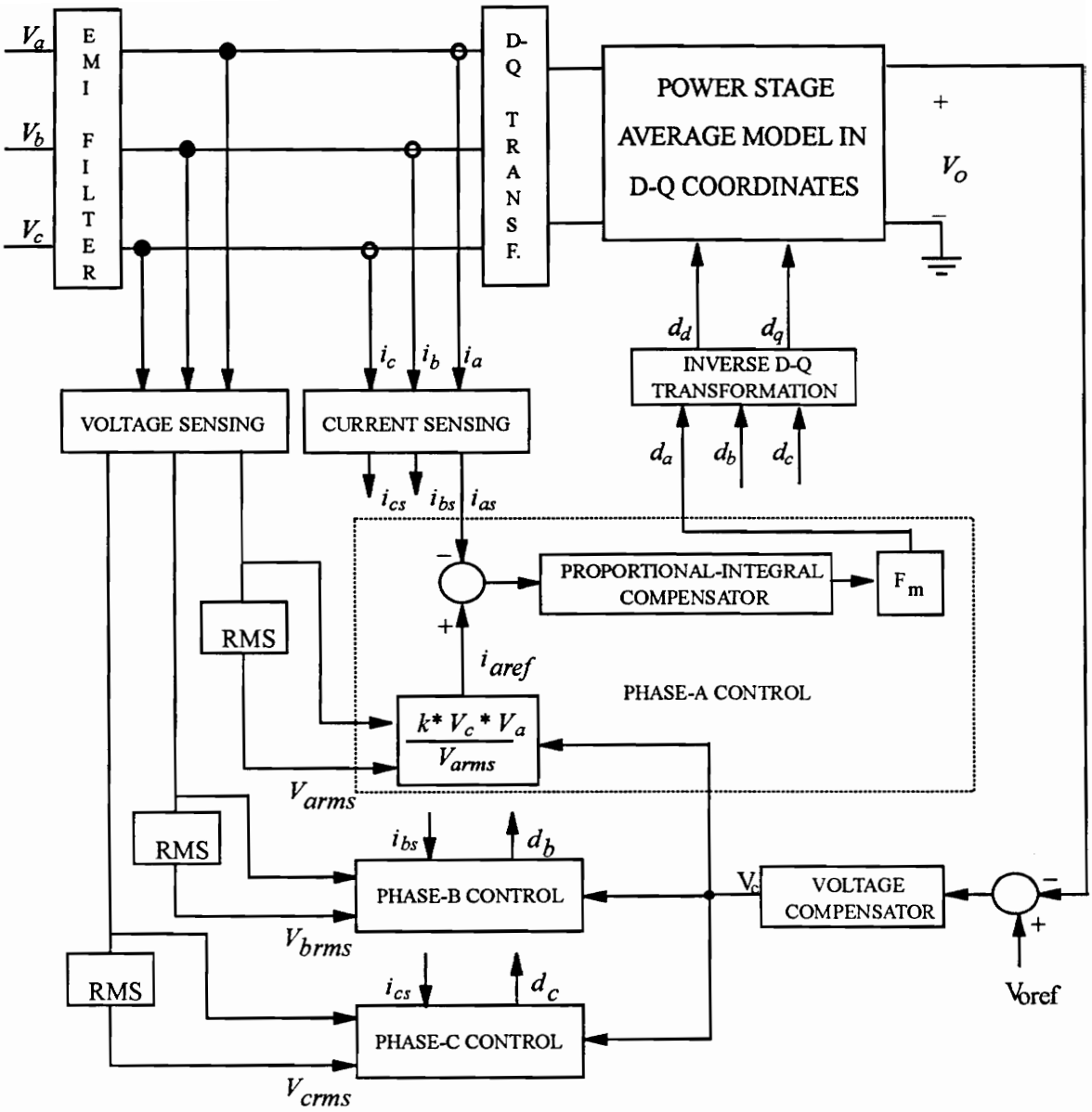


Fig. 4.14 Complete average model with feedforward

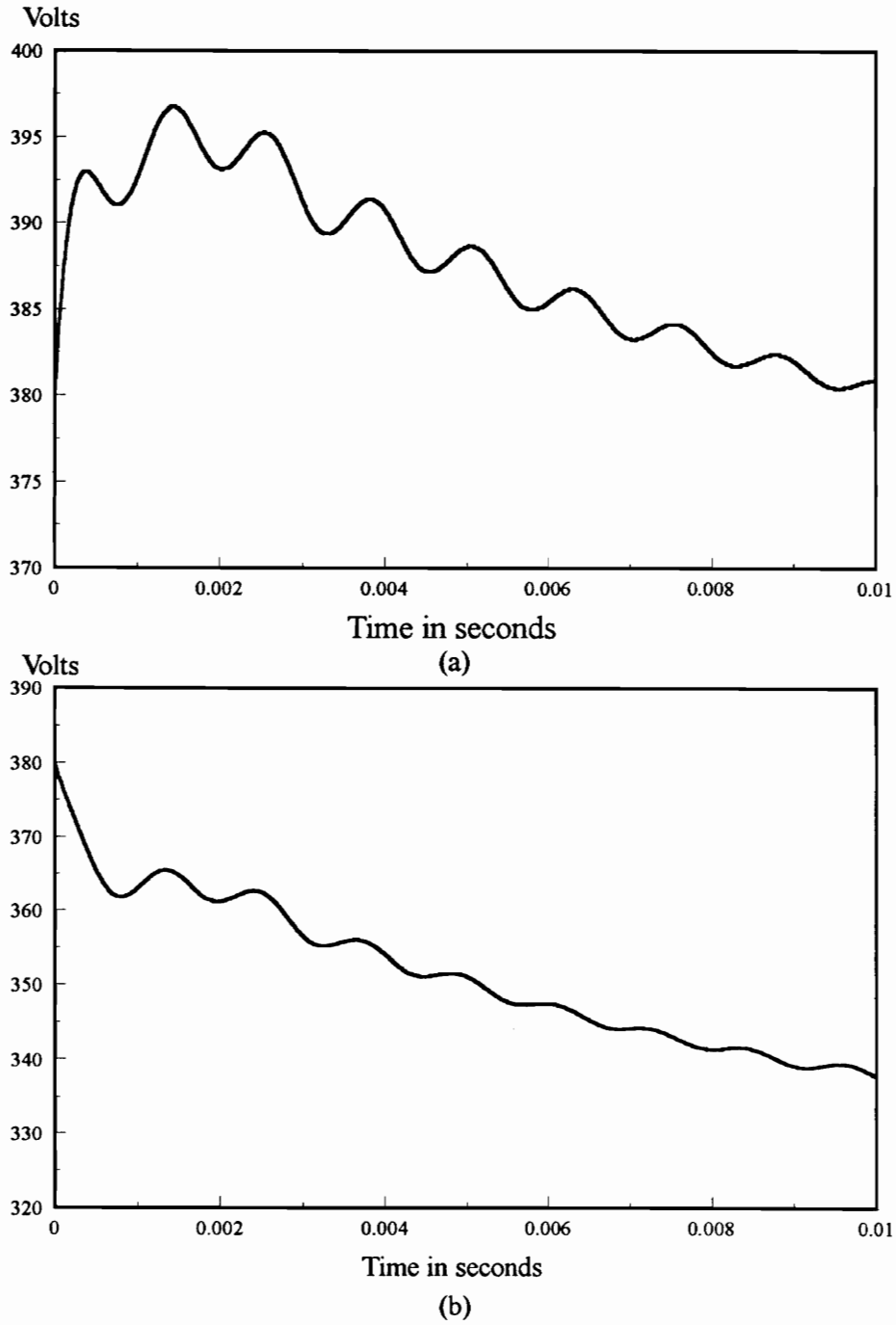


Fig. 4.15 Output voltage (a) with $v_{ff} = (v_{rms})$ *(b) with* $v_{ff} = (v_{rms})^2$

two cases is as shown in Fig. 4.15. $v_{ff} = (v_{rms})^2$ gives relatively lesser ripple than $v_{ff} = (v_{rms})$.

4.7 Operation with Disabling Logic

The disabling logic is implemented in the average model through a Saber element template. The average model with disabling logic is as shown in Fig. 4.16. With disabling logic, the steady state duty cycles are no longer sinusoidal, but are as shown in Fig. 4.17(a). However, the steady state line to line duty cycles are still sinusoidal. The average model shown in Fig. 4.16 was simulated for the parameters enclosed in Appendix A. The current waveforms are as shown in Fig. 4.17(b). It is observed that transients caused by the disabling logic produce additional distortions in the current waveforms. The reason for this is that the output of the disabled controller requires some transient time to reach a desired value after it is enabled again. Once again, this delay can be reduced by increasing the proportional gain of the current compensator.

4.8 Design of the Voltage Loop

As seen in Fig 4.5, the control to output transfer function with closed current loops is similar to the corresponding transfer function of a dc-dc boost converter, with a dominant low frequency pole and a right-half plane zero. Hence, the voltage compensator design can be the same as that of a dc-dc boost converter. A two-pole, one-zero

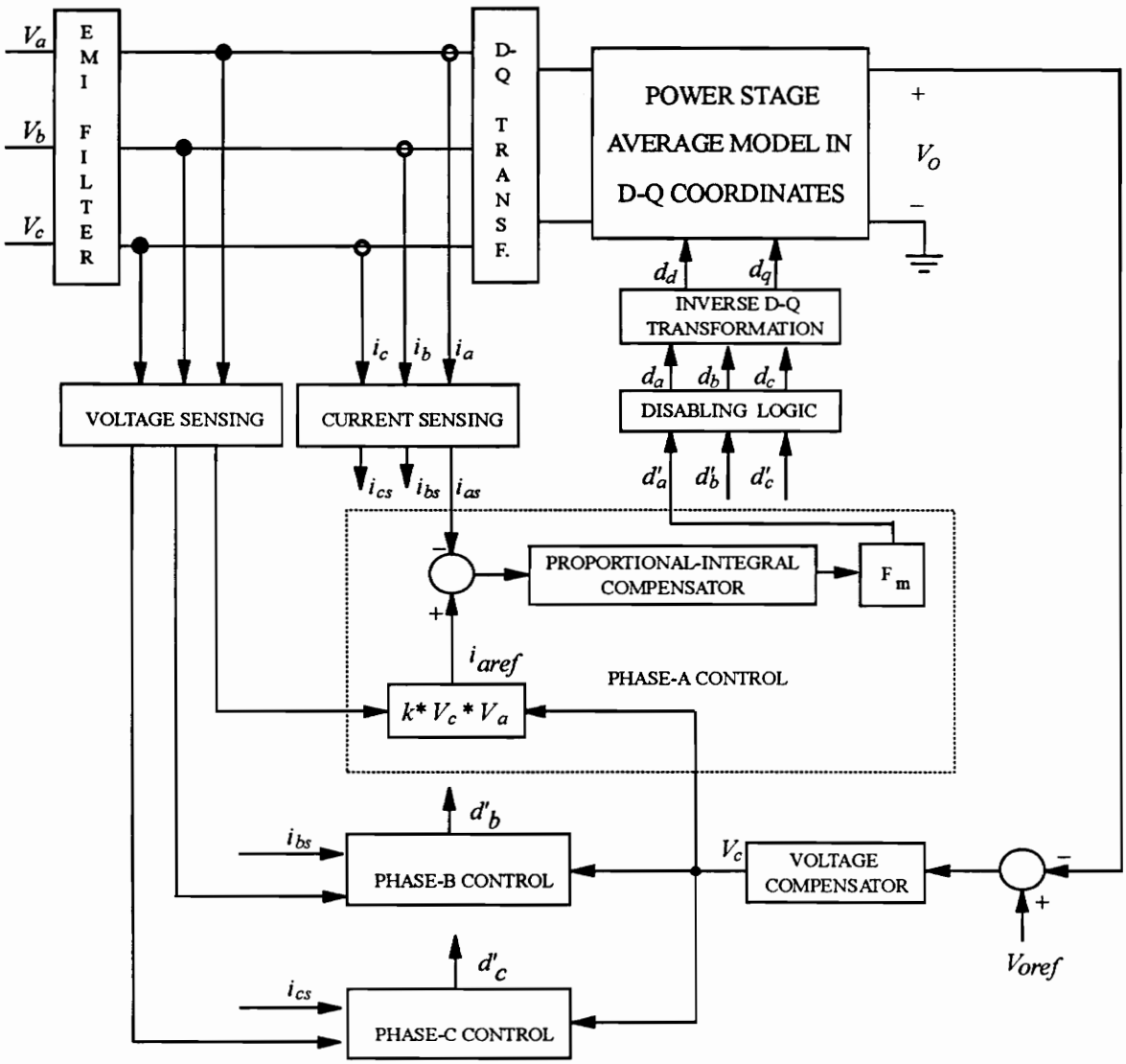


Fig. 4.16 Average model with disabling logic

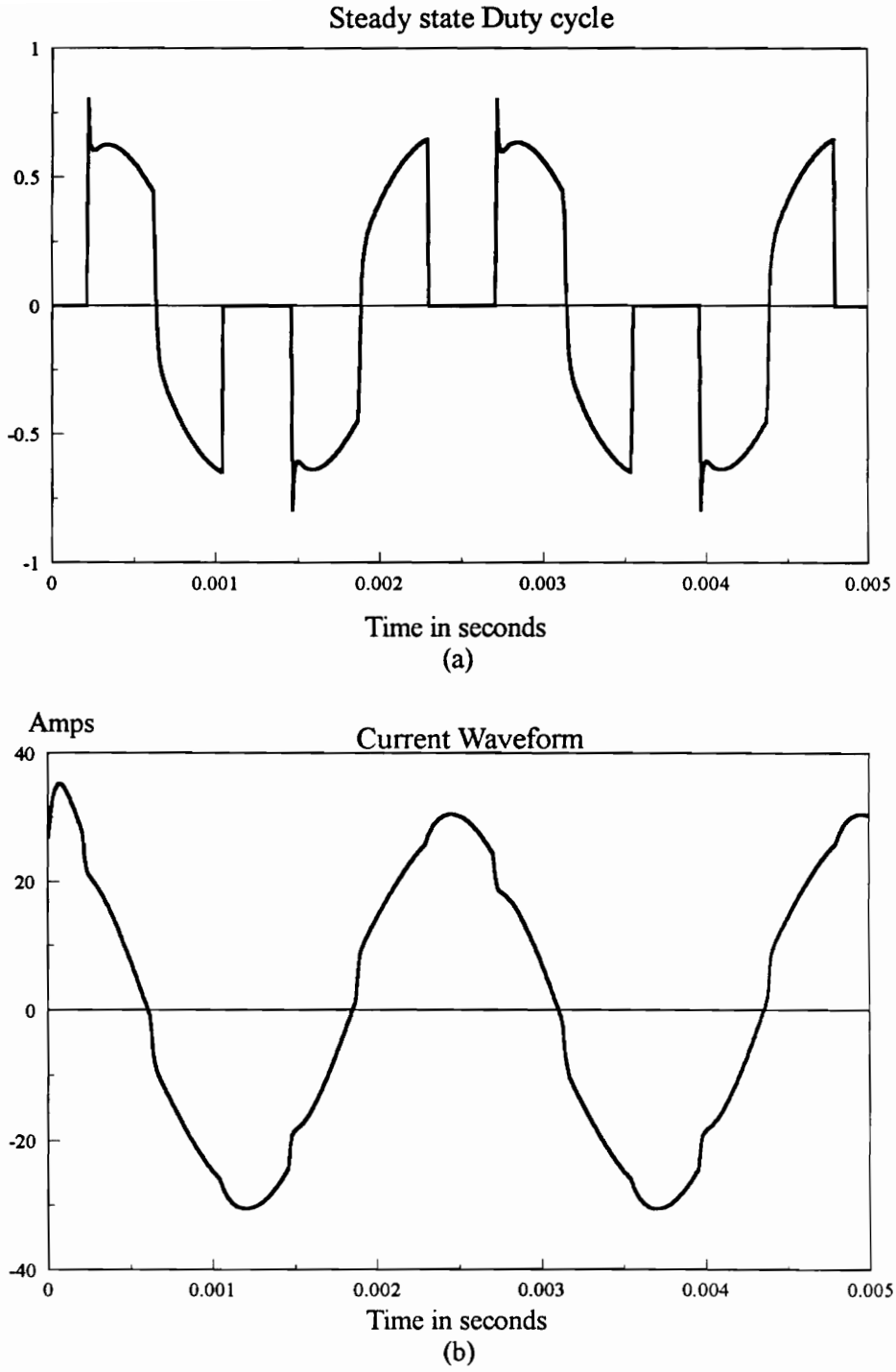


Fig. 4.17 Waveforms with disabling logic (a) duty cycle (b) current

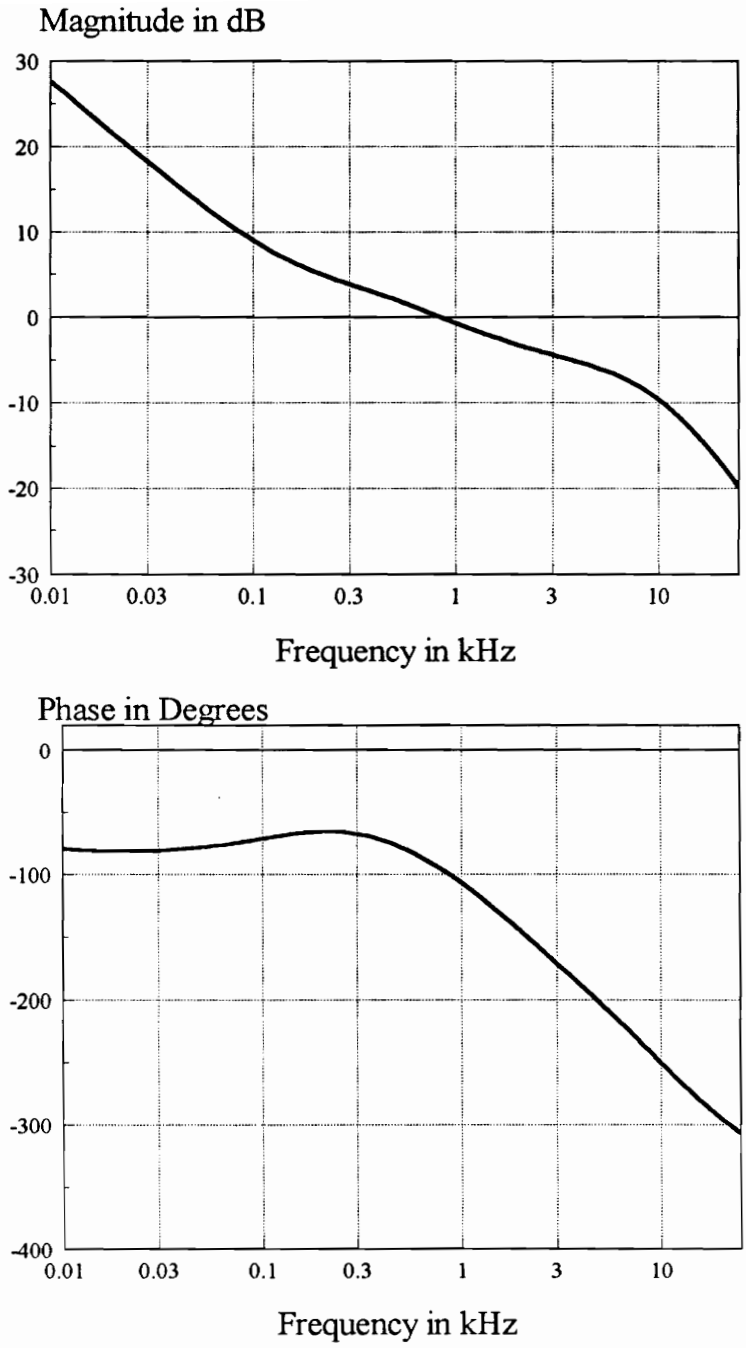


Fig 4.18 Voltage loop gain

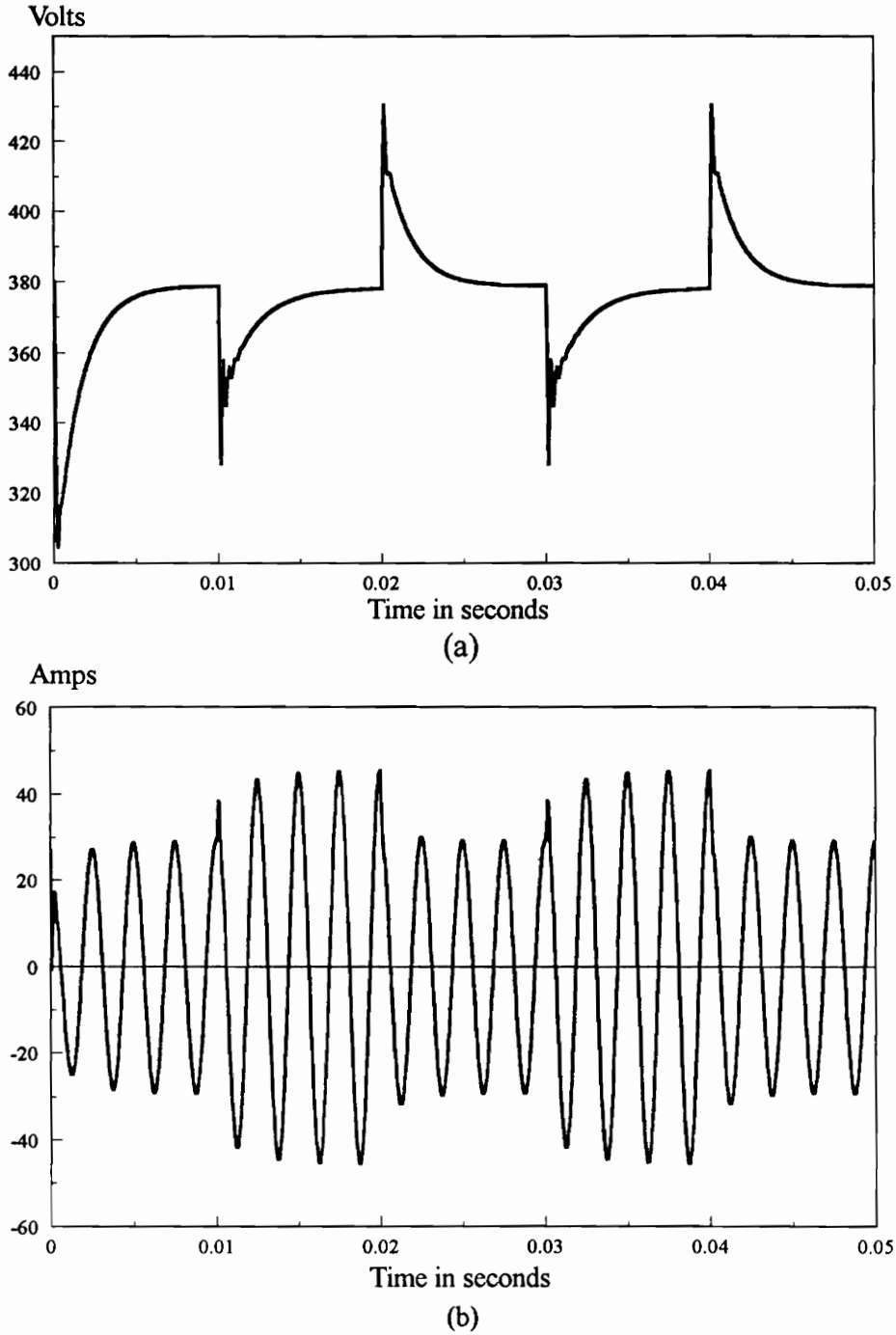


Fig. 4.19 Transient analysis (a) output voltage (b) input current for 33% step change in load

compensator would suffice for the voltage loop. In the present case, the voltage loop was designed with a bandwidth of around 1 kHz, as shown in Fig. 4.18.

The converter with closed current and voltage loops was subjected to a step change in load. The response of the system is as shown in Fig. 4.19. As in the case of dc-dc converters, the response can be improved by increasing the bandwidth.

4.9 Experimental Verification

4.9.1 Experimental Verification of the Power Stage Model

The three-phase ZVT PWM boost rectifier does not work without closed current loops because the average voltage across the input inductors cannot be controlled precisely enough just by sinusoidaly varying duty cycles, d_a, d_b, and d_c. Hence, it is not possible to experimentally verify the open-loop small signal transfer functions. Moreover, the-closed loop transfer functions are dominated by the current loop. Hence, it is difficult to observe the effect of ZVT in closed loop transfer functions because the dominant effect of the ZVT is the increase in power stage damping, which is also caused (but to a much higher degree) by the current loop.

Another much less pronounced effect of ZVT is the change in dc gain. In order to verify the change in dc gain, the input voltage to a 5 kW experimental circuit (parameters are enclosed in Appendix A) was varied and the corresponding change in output voltage (normalized) introduced by ZVT is plotted. The results are compared to the

corresponding results obtained from the average model. The comparison is shown in Fig. 4.20. The change in dc gain is a function of the input current and output voltage. At low input voltages, the change in dc gain is very low as both the input current and output voltage are very low in magnitude. But as the input voltage increases, the change in dc gain increases as both the input current and the output voltage increase. It can be seen that there is quite close agreement between experimental and simulated results.

4.9.2 Experimental Verification of the Controller Model

A good model for the controller should be able to produce the same kind of waveforms as observed in an experimental circuit. Two kinds of disturbances were observed in the current waveforms obtained from the experimental circuit. A good model should be able to identify the reasons for each of the distortions. Fig. 4.21(a) compares the current waveforms obtained from the experimental circuit with the current waveforms obtained through large signal simulation of average model. The error signals are rectified in this case. Fig. 4.21(b) shows the same set of waveforms with disabling logic. In order to identify clearly the reasons for each of the distortions, the error signals are not rectified. A close similarity is observed between experimental and simulated waveforms, which validate the predictions of the average model. From these results it can be concluded that distortions in current waveforms can be caused due to rectification of error signals (Fig. 4.21(a)) and due to disabling logic (Fig. 4.21(b)).

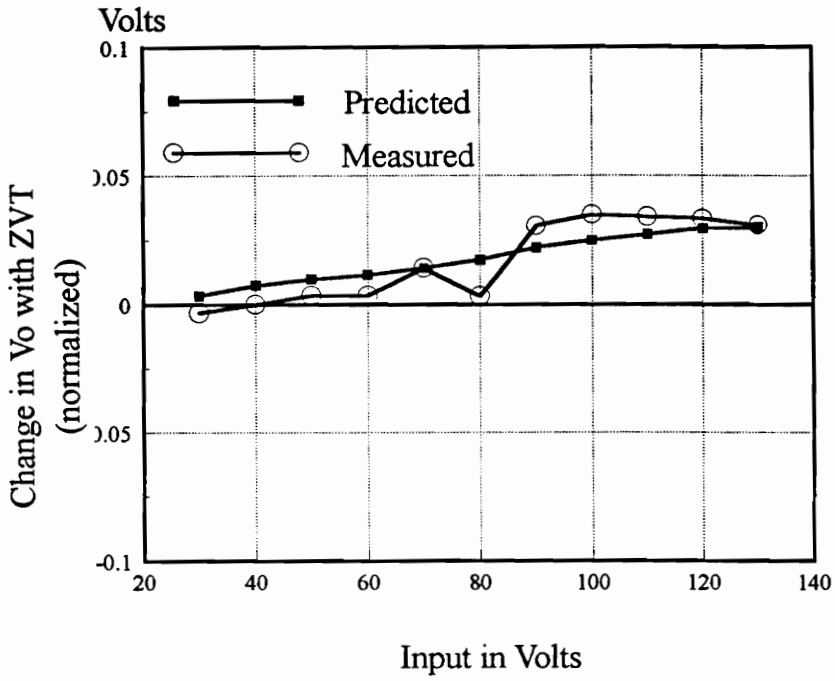
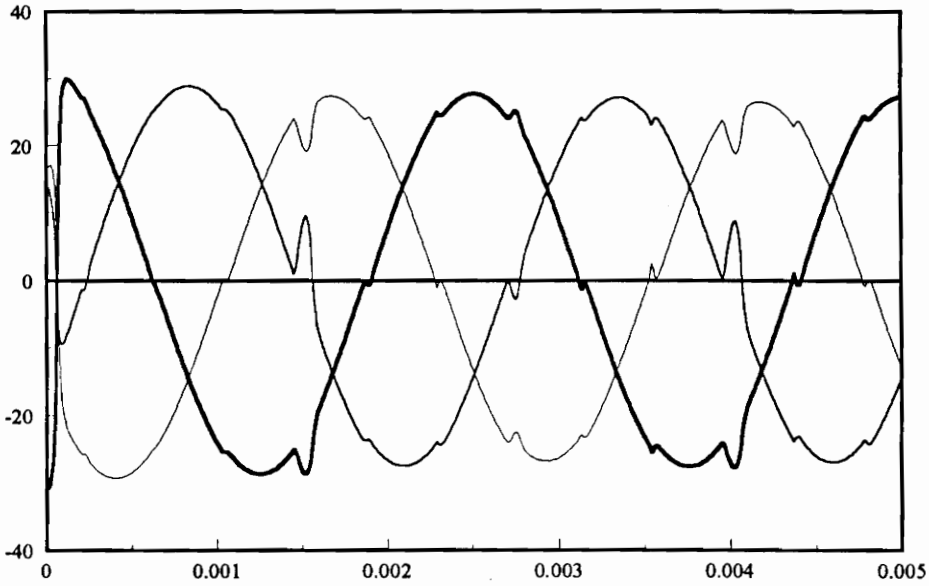


Fig. 4.20 Experimental verification- power stage

Amps Experimental Waveform

Amps Simulated Waveform



Time in seconds

Fig. 4.21(a) Experimental verification of current controller model- Distortions due to rectification of error signals (with 3% imbalance)

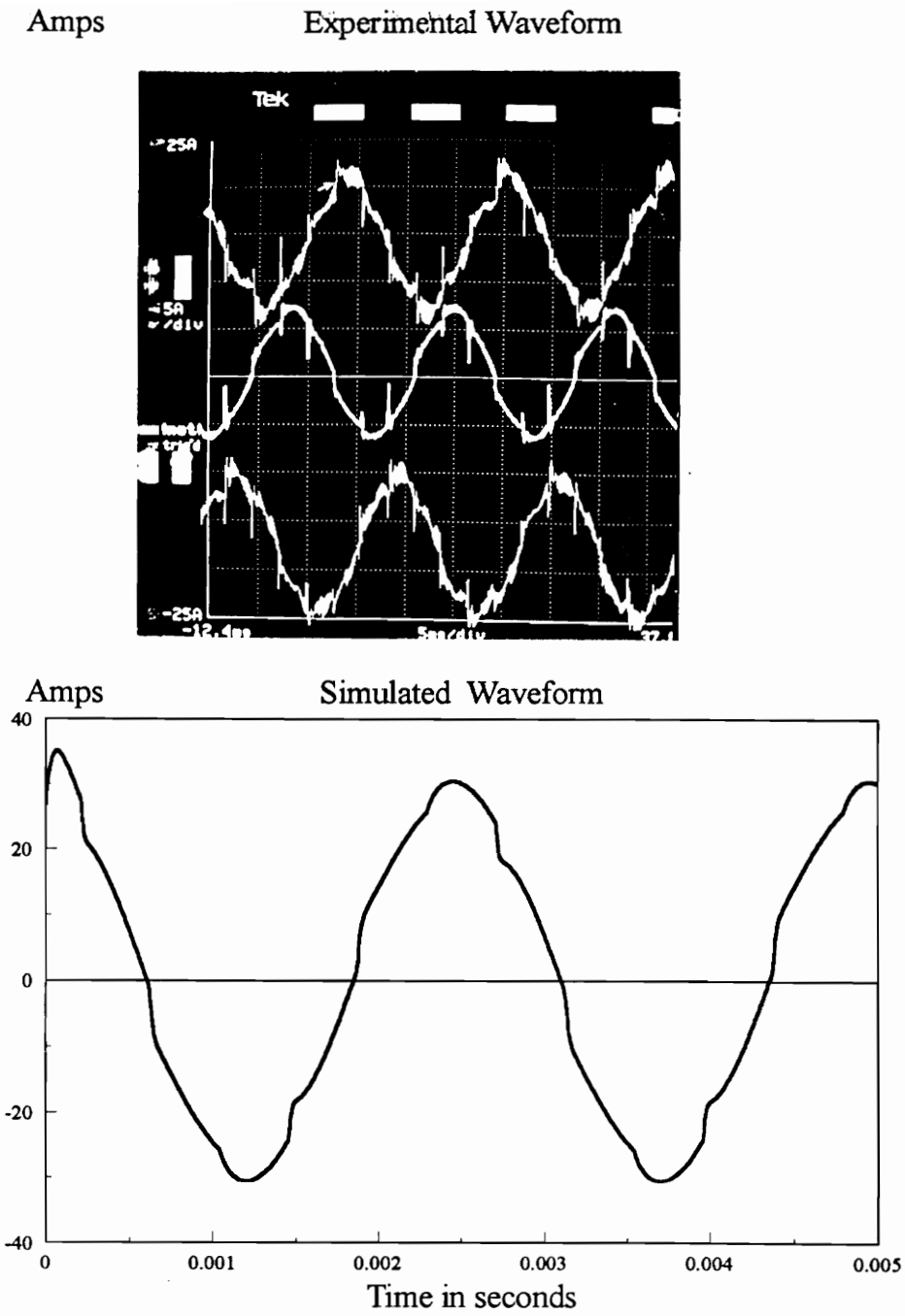


Fig. 4.21(b) Experimental verification of current controller model Distortions due to disabling logic

4.9 Conclusions

The controller modeling and design issues for the three-phase ZVT PWM boost rectifier have been discussed. The average current controller is modeled in stationary coordinates, and is transformed to rotating coordinates for ease of design. The controller is designed using the same procedure as in [10]. The large signal simulations of the closed loop average model show sever distortions in the input current waveforms when the error signal is rectified. The distortions can be reduced by increasing the proportional gain K_p. The distortions can be removed if the error signal is not rectified and the controller is built with discrete components instead of UC1854 PFC chip. However, this increases the cost and space utilization due to increased complexity. Moreover, disabling logic imposes additional constraints on the controller. Disabling logic introduces distortions in the current waveforms, even without the rectification of error signals. The operation with disabling logic will be investigated further in Chapter 5 using the switching model.

Two prominent cases of feedforward gain were simulated with the average model in order to investigate the performance with different feedforward algorithms. From the simulations, it was concluded that dividing the current reference by $v_{ff} = (v_{arms})^2$ gives the best results.

5. Switching Model of ZVT Three-Phase PWM Boost Rectifier

In order to verify the controller designed using the average model, a switching model was developed in Saber schematic version, Design star. The power stage consists of ideal switches and diodes. Three sinusoidal voltage sources are used as input to the power stage. The power supply neutral is connected to the ground terminal. The current sensing is implemented with ideal current-controlled voltage source with gain equal to current sensor gain, R_i. The current controller used in the model is standard proportional-integral (PI) compensator. The proportional and integral gains are obtained from the designed values in Chapter 4. The rectification of error signals is approximated by an absolute value. Fig. 5.1 shows the relevant waveforms obtained from simulations of switching model, illustrating the action of ZVT network.

It was observed in Chapter 4 that distortions can be produced in input currents due to rectification of error signals and due to disabling logic. However, it was also shown that distortions due to rectification of error signals can be avoided if discrete components are used for the controller instead of UC1854 PFC chip, or in other words if the error signal is not rectified. But the distortions due to disabling logic will still exist even

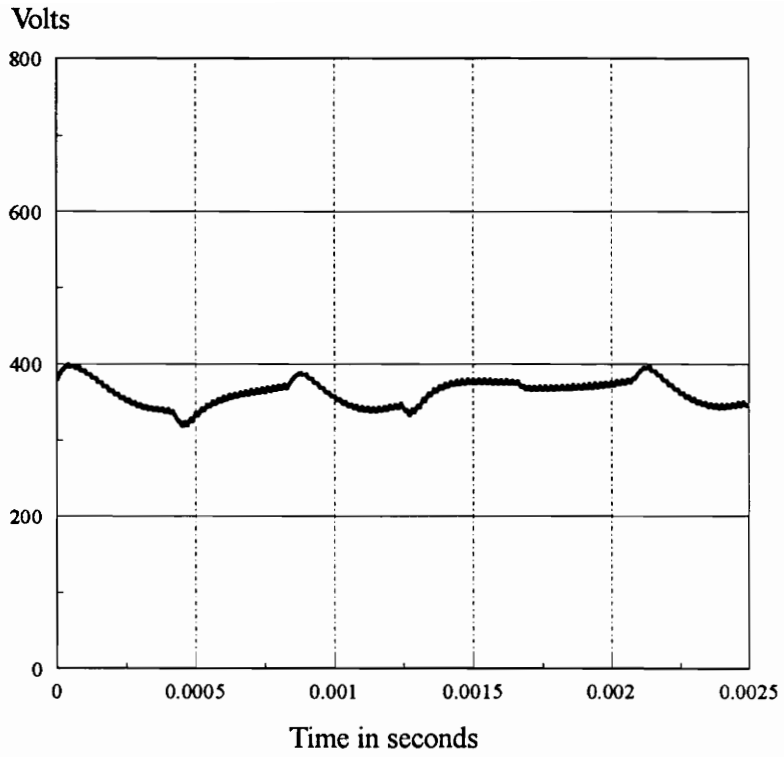


Fig 5.1(a) Output voltage waveform of the switching model

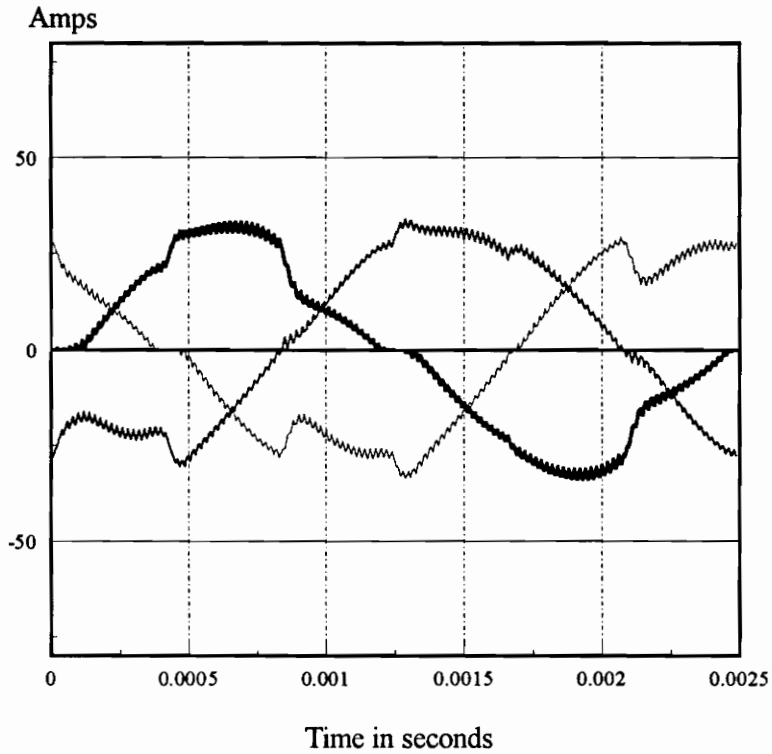


Fig 5.1(b) Current waveforms of the switching model

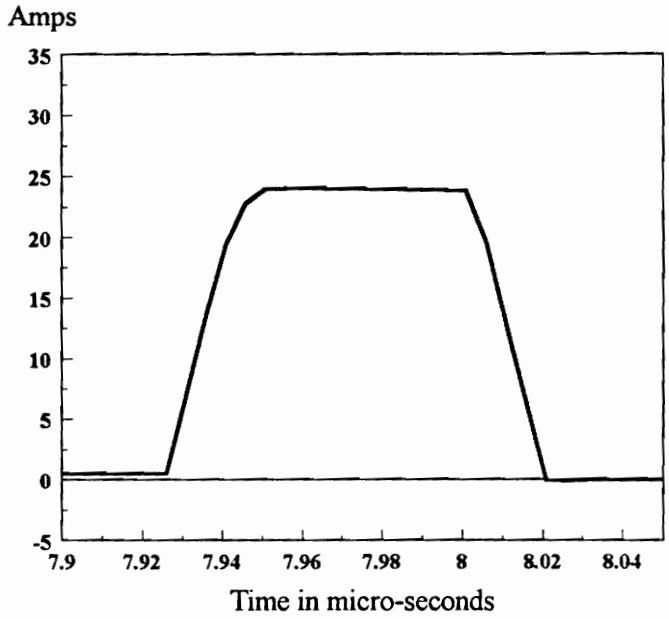


Fig 5.1(c) Current through resonant inductor

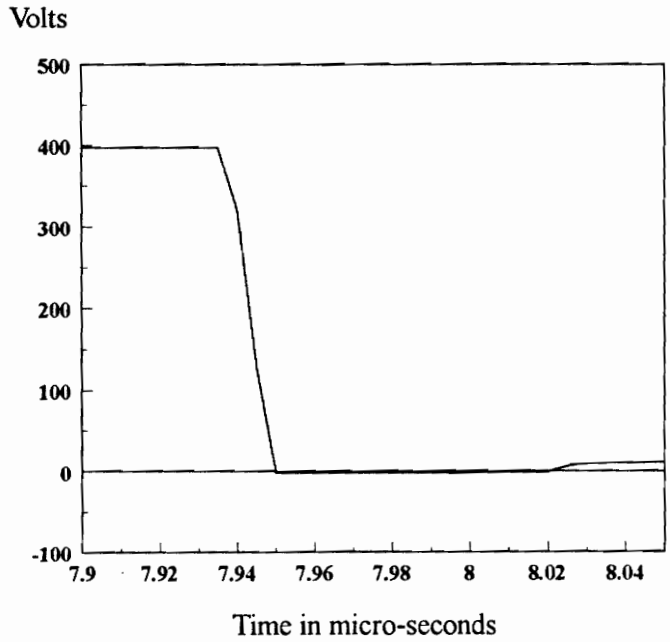


Fig 5.1(d) Voltage across the bridge output

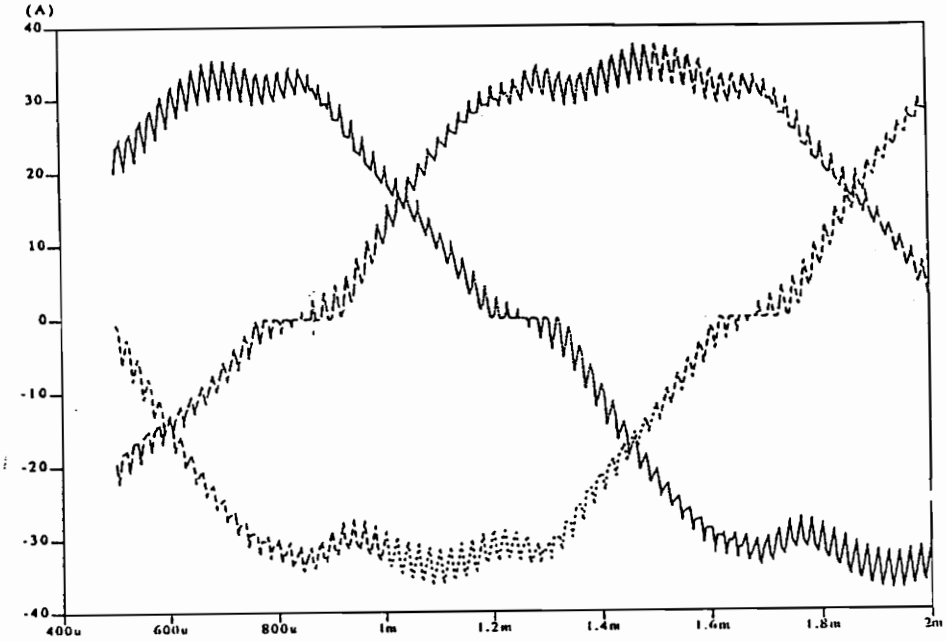


Fig 5.2(a) Current waveforms with rectification of error signals, kp =1

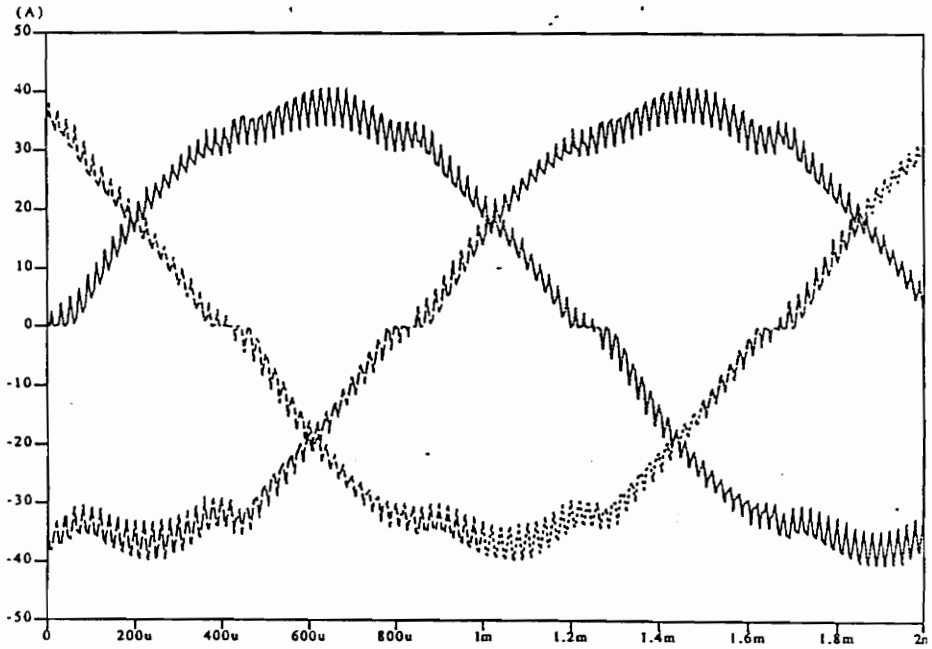


Fig 5.2(b) Current waveforms without rectification of error signals, Kp =1

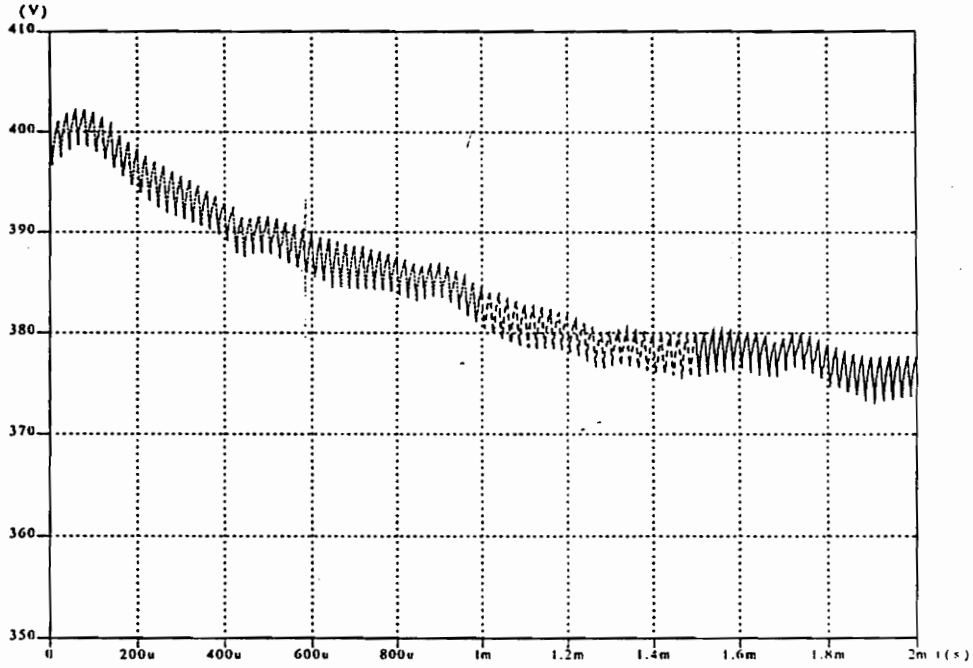


Fig. 5.2(c) Output voltage

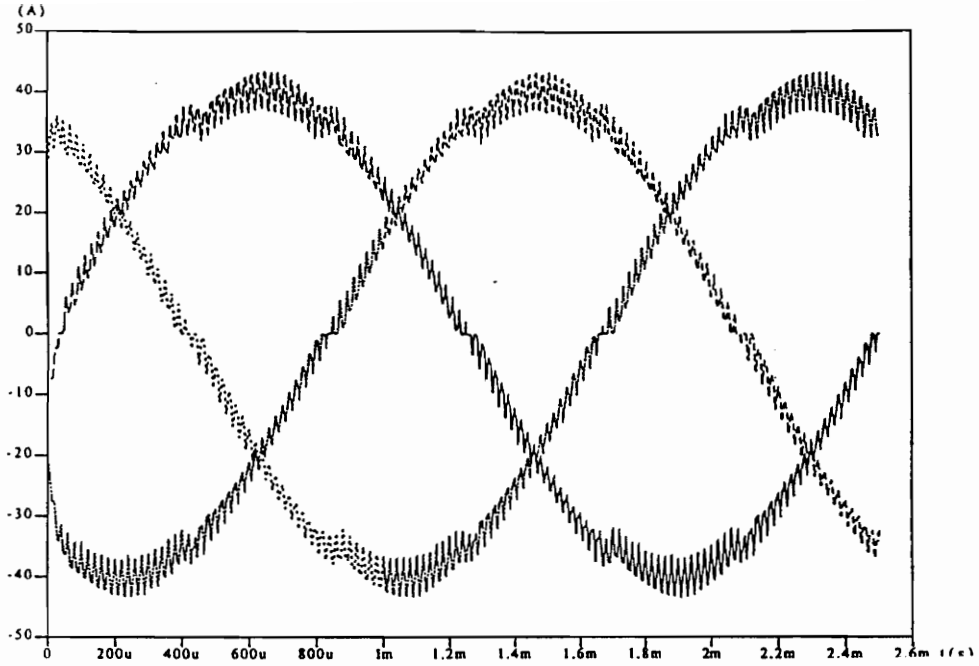


Fig 5.3(a) Current waveforms with rectification and with Kp =5

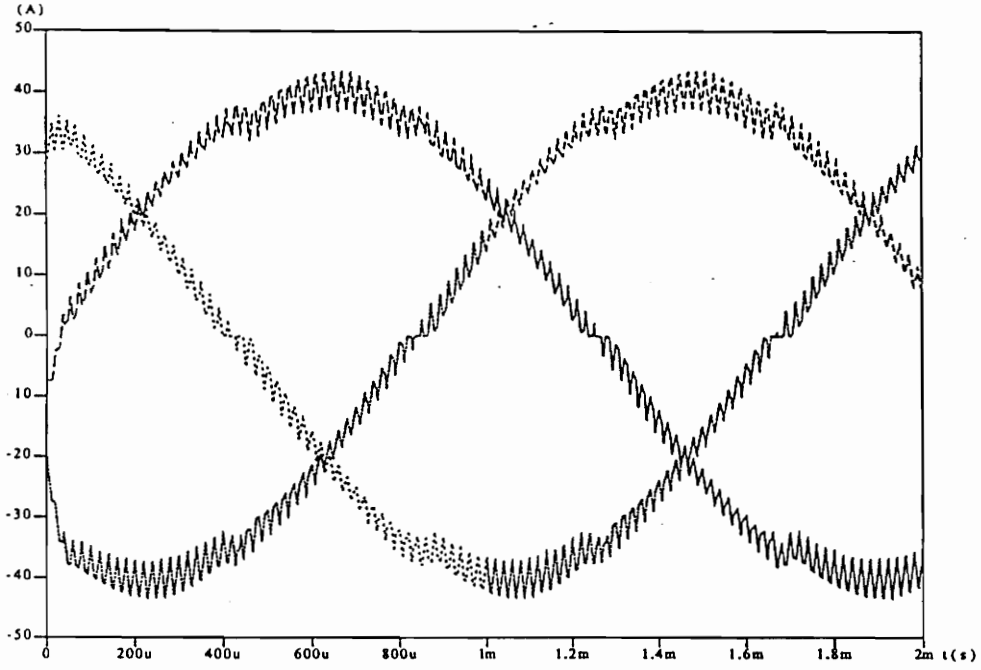


Fig 5.3(b) Current waveforms without rectification and with Kp =5

without rectification of error signals. In order to investigate the controller performance with disabling logic, the switching model was simulated with and without rectification of error signals, and with three percent imbalance. Also, in order to make the model more realistic, relative tolerance is introduced into the three controller parameters. Moreover, in order to improve the performance of the controller with disabling logic, the input to the controller is also disabled during the segment when the corresponding phase current is the largest. The disabling logic is implemented with a group of logic gates. When the error signal is not rectified, the modulator is implemented with two bipolar ramps, one for the top switch and one for the bottom switch.

The simulation results with and without rectification of error signal are shown in Fig. 5.2. The results clearly show that, as predicted by the average model, the operation without rectification of error signal gives less distortions in current waveforms even with disabling logic.

From the above simulation results it can be concluded that although the disabling logic introduces additional disturbances even when the error signals are not rectified, the disturbances are not as severe as the disturbances introduced at zero-crossings due to rectification of error signals. It can also be concluded that for optimal performance of the controller, the error signals should not be rectified. Moreover, the rectification cannot be ideal in a practical circuit and this will exaggerate the zero-crossing problem. With very high proportional gain, the current waveforms with rectification of error signals are comparable to the waveforms without rectification of error signals, as shown in Fig. 5.3.

6. Conclusions

In order to enable analysis and control design of the ZVT three-phase boost rectifier, switching, average, and small signal modeling was performed. The ZVT effects do not change sinusoidally nor they are constant in steady state. This causes some low-frequency harmonic distortion, but this effect was not further investigated. In order to obtain time-invariant d-q model, only the first order effects of ZVT were taken into account. The resulting approximation should not cause large errors, especially in the linearized model. Additional assumptions used in the model derivations are that all components are ideal, and that the circuit operates with unity displacement factor.

It is shown that small signal characteristics of the three-phase boost rectifier vary appreciably due to ZVT. The ZVT action has two effects:

I. It changes the dc value of the duty cycle.

II. It introduces feedback from the output voltage and direct component of the input current.

The most pronounced consequences are that the first effect limits the maximum duty cycle to some value less than unity, while the second effect significantly increases transfer function damping.

A simple analog control scheme with three independent current controllers can be used to control the three phase currents of the converter. The design procedure for the current controllers is illustrated for one particular set of parameters. The independent control scheme was originally implemented with three UC1854 PFC chips. The use of the PFC chips requires the rectification of error signals. It has been shown through simulations of average and switching models that severe distortions can arise in current waveforms due to two reasons:

I. Rectification of error signals,

II. Disabling logic.

Rectification of error signals can cause severe distortions in the input current waveforms due to the inability of the current compensator to replicate the zero-crossings. Disabling logic can introduce distortions in the current waveforms because the output of the disabled compensator diverges from the actual value during the period it is disabled. The distortions can be reduced by increasing the proportional gain, which is directly related to the bandwidth. However, there is a practical limitation to increase in bandwidth because the circuit becomes susceptible to noise.

In order to compensate for changes in output voltage due to changes in input voltage, and to compensate for imbalance in input phase voltages, feedforward from the input voltage should be used. To obtain the feedforward term which gives the best results,

two important cases were simulated, $v_{ff} = (v_{rms})$ and $v_{ff} = (v_{rms})^2$. From the simulation results it is concluded that $v_{ff} = (v_{rms})^2$ gives less ripple in the output voltage.

It was not possible to verify the transfer function damping introduced by ZVT because the three-phase boost rectifier can work only with closed current loops. The damping introduced by the current loops is more pronounced than one introduced by ZVT. However, the change in low-frequency gain produced by ZVT has been experimentally verified on a 5 kW experimental circuit. Also, the waveforms obtained using the controller model are very similar to those obtained from a practical circuit. Hence, the closed-loop average model can be used as a very effective tool in predicting and reducing the irregularities in the current waveforms of a three-phase boost rectifier.

The effects of ZVT were approximated with their first order harmonics (on the input side) in order to reduce the complexity in modeling. However, the ZVT effect causes low-frequency harmonic distortion if the approximations are not made. Future work should investigate this aspect in detail. Also, only two cases of feedforward terms in the current-controller have been investigated. Future work should investigate other possible cases.

Appendix A:

Parameters used in the models:

Power Stage Parameters:

Input phase voltage (rms), Vph(rms)= 90 Volts

Line frequency , fl = 400 Hz

Output voltage, Vo = 380 Volts

Boost inductors, L = 400uH

Output capacitor, Co:= 20uH

Resonant inductor, Lr = 6uH

Resonant Capacitor, Cr =5nF

Switching frequency, fs == 50kHz

Controller Parameters:

Current sensor gain, Ri = 0.5

Proportional gain of the current compensator , Kp = 1

Integral gain of the current compensator, Ki = 5k

Modulator Gain, Fm = 0.2

Voltage sensing transformer turns ratio, n =20

Parameters used for experimental verification:

Power Stage Parameters:

Line frequency , fl = 60 Hz

Boost inductors, L = 550uH

Output capacitor, Co:= 330uH

Resonant inductor, Lr = 11uH

Resonant Capacitor, Cr =6.87nF

Switching frequency, fs == 50kHz

Controller Parameters:

Current sensor gain, Ri = 0.16

Proportional gain of the current compensator , Kp = 9.2697

Integral gain of the current compensator, Ki = 61.801k

Modulator Gain, Fm = 0.2

Voltage sensing transformer turns ratio, n =20

Appendix B: Netlists

The MAST language in Saber makes the simulation software more versatile. Due to its enhanced programming capability, especially in simulating unusually large circuits, Saber was chosen to implement all the models. The netlists for the complete average model of the ZVT three-phase PWM boost rectifier are enclosed in the following pages. The netlists contain both standard templates, [12] and user defined templates. The user defined templates are written using the MAST programming language.

```
# This netlist is for designing the average current controller for the
# three-phase ZVT PWM boost recifier.
# The controller in this file is in stationary coordinates
# Without disable logic, without rectification


#-----------------------------------------------------------------------
# Enter parameters

# Power stage parameters


# Resonant circuit parameters

number  lr      =3u                         # Resonant inductor
number  cr      =1n                         # Resonant Capacitor
number  Daux    =0.1                        # Auxiliary switch duty cycle

# Converter parameters

number  fs      =50k                        # Switching Frequency
number  fl      =400                        # Line frequency
number  l       =400u                       # Boost inductor
number  rl      =300m                       # Resitance of the boost ind
number  Co      =20u                        # Output Capacitor
number  R       =25.79                      # Output Resistance
number  Vo      =380                        # Output Voltage
number  pi      =3.1416                     # pi
number  Vd      =90*sqrt(2)*sqrt(3)         # Input voltage
number  w       =2*pi*fl                    # Line Frequency
number  Po      =5.6k                       # Output power
number  Id      =Vo*Vo/(R*1.5*Vd)           # Id Steady state value
number  Vm      =Vd                         # Amplitude of input voltage
number  Im      =3*Id/pi                    # Maximum input phase current
number  Io      =Po/Vo                      # Output Current
number  Dd      =Vd/Vo                      # Dd
number  Dq      =-2*w*l*Vo/(R*Vd)           # Dq
number  Dm      =sqrt(Dd*Dd+Dq*Dq)          # Maximum duty cycle
number  deto1   =Lr*Im/Vo                   # Delta To1
number  deto2   =pi*sqrt(lr*Cr)/2           # Delta To2
number  deltad  =-Daux + deto1*fs + 2*deto2*fs/pi # Delta D
number  fd      =2*sqrt(3)/pi               # fd

# Controller parameters
number  Ri      =0.5                        # Current sensor gain
number  Fm      =0.2                        # Modulator gain
number  KP      =1
number  KI      =5k
number pisq     =pi*pi
number rt3      =sqrt(3)
#-----------------------------------------------------------------------
# Front End processing Block
#-----------------------------------------------------------------------

# Phase Volatges

vs.va           a6 0            =Vm/rt3,fl,0            # Phase A
vs.vb           b6 0            =Vm/rt3,fl,-2*pi/3      # Phase B
vs.vc           c61 0           =Vm/rt3,fl,2*pi/3       # Phase C
#-----------------------------------------------------------------------

#-----------------------------------------------------------------------
# D-Q transformation Block
```

```
# D - block

vs.vd1          d1 0            =2/3,fl,pi/6     # 2/3cos(wt+pi/6)
vs.vd2          d2 0            =2/3,fl,-pi/2 # 2/3cos(wt-pi/2)
vs.vd3          d3 0            =2/3,fl,5*pi/6   # 2/3cos(wt+5pi/6)
v.vd            vd1 vds         =Vd              # Input Vd
v.vds           vds 0           =ac=(0,0)

#-----------------------------------------------------------------------

# Q Block

vs.vq1          q1 0            =2/3,fl,2*pi/3   # -2/3sin(wt+pi/6)
vs.vq2          q2 0            =2/3,fl,0        # -2/3sin(wt-pi/2)
vs.vq3          q3 0            =2/3,fl,4*pi/3   # -2/3sin(wt+5pi/6)
v.vq            vq 0            =dc=0    # input Vq

#-----------------------------------------------------------------------

l.Ld            2 31            =3*l,ic=15.55
r.rd            31 3            =3*rl
l.Lq            5 61            =3*l,ic=4.641
r.rq            61 6            =3*rl
c.Co            9 0             =Co,ic=380
r.ro            9 0             =R
r.rll           9 sw            =2*R

# Voltage controlled switch

sw_vc.s         sw 0 cont 0 =model=(vt=5,vh=lm,ron=lu,roff=lg)

# Control voltage for the volage controlled switch

v.conv  cont 0  =tran=(pulse=(vl=0,v2=15,td=10m,tr=lu,tf=lu,pw=10m,per=20m

#-----------------------------------------------------------------------

ccvs.vl         i(l.Lq) 2 vd1   =k=3*w*l         # 3*w*l*iq
mult.v2         d 0 9 0 3 4                      # dd*vo

#  Modeling of fd*deltaD*vo

vcvs.v3         9 0 41 4        =k=fd*Daux-fd*fs*sqrt(Lr*Cr)
ccvs.vida       i(l.ld) ida 0   =k=1
ccvs.viqa       i(l.lq) iqa 0   =k=1
squarer.idsq    ida 0 x1 0
squarer.iqsq    iqa 0 y1 0
spe2.sum        xy 0 x1 0 y1 0  =e=[0,1,1]
sqrt.ipsqrt     xy 0 41 0       =k=fd*Lr*fs*3/pi

#-----------------------------------------------------------------------

ccvs.v4         i(l.Ld) vq 5    =k=3*w*l
mult.v5         q 0 9 0 6 0

#-----------------------------------------------------------------------

ccvs.id1        i(l.Ld) 911 0   =k=1.5  # 3/2*id
mult.id2        911 0 d 0 912 0         # 3/2*dd*id
```

```
vccs.id          912 0 0 9        =k=1

ccvs.iq1         i(l.Lq) 913 0    =k=1.5  # 3/2*iq
mult.iq2         913 0 q 0 914 0          # 3/2*iq*dq
vccs.iq          914 0 0 9        =k=1

# Effect of ZVT on the secondary side

# Modeling ix


vdiv.fir         xy 0 9 0 xyz 0
vccs.f1          xyz 0 0 9        =k=9*fs*Lr/pisq
vccs.f2          41 0 9 0         =k=(Daux-fs*sqrt(Lr*Cr))/( fd*Lr*fs*3/pi)
vccs.f3          9 0 0 9          =k=Cr*fs/2


#-----------------------------------------------------------------
# Transformation of id & iq to ia, ib, ic

itrans.iabc      ida iqa ia ib ic =fl,pi

#-----------------------------------------------------------------
# Phase A control

vcvs.iref1       a6 0 irf1 0       =k=0.02907
contno.iacon     irf1 vc ia daa 0 =Ri,Fm,Kp,Ki
#-----------------------------------------------------------------


# Phase B control

vcvs.iref2       b6 0 irf2 0      =k=0.02907
contno.ibcon     irf2 vc ib db 0 =Ri,Fm,Kp,Ki
#-----------------------------------------------------------------


# Phase C control

vcvs.iref3       c61 0 irf3 0     =k=0.02907
contno.iccon     irf3 vc ic dc 0 =Ri,Fm,Kp,Ki

#-----------------------------------------------------------------

# De - rectifcation
#drec.dabc       a6 b6 c61 daa5 db5 dc5 0 daa db dc

# Calculation of dab, dbc and dca


sum.dab          daa 0 db 0 dab 0         =k1=1,k2=-1      # dab = da - db
sum.dbc          db 0 dc 0 dbc 0          =k1=1,k2=-1      # dbc = db - dc
sum.dca          dc 0 daa 0 dca 0         =k1=1,k2=-1      # dca = dc - da

#-----------------------------------------------------------------

# Transformation of dab, dbc and dca to dd and dq

#-----------------------------------------------------------------

# dd - block

mult.dd1         d1 0 dab 0 dd1 dd2                # 2/3*cos(wt+pi/6)*dab

mult.dd2         d2 0 dbc 0 dd2 dd3                # 2/3*cos(wt-pi/2)*dbc
```

```
mult.dd3        d3 0 dca 0 dd3 0                # 2/3*cos(wt+5pi/6)*dca

vcvs.ddd        dd1 0 d 0       =k=1
#-----------------------------------------------------------------------

# dq - Block

mult.dq1        q1 0 dab 0 dq1 dq2              # -2/3*sin(wt+pi/6)*dab

mult.dq2        q2 0 dbc 0 dq2 dq3              # -2/3*sin(wt-pi/2)*dbc

mult.dq3        q3 0 dca 0 dq3 0                # -2/3*sin(wt+5pi/6)*dca

vcvs.dqq        dq1 0 q 0       =k=1            # Duty cycle dq
#-----------------------------------------------------------------------

#v.vch  vc vc1          =dc=3.6405
#v.vchat vc1 0          =ac=(-1,0)

#-------------------------------------------------------------
# Voltage compensator

vcvs.vcoin      9 0 coin 0      =k=0.01
r.r111          coin opin       =1
r.r211          opin op2        =1k
c.c211          op2 opout       =1u
c.c111          opin opout      =1n
v.vref          ref 0           =3.8

oab.vopamp      ref opin opout 0 =a=100k,fu=10me,rin=1me,rout=0,f2=1me
v.v1111         v111 0          =dc=300
vdiv.vch2       opout 0 v111 0 vc 0

#-----------------------------------------------------------
```

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Vita

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He joined Virginia Power Electronics Center in Spring 1994 as a graduate research assistant. He was actively involved in research at VPEC in the areas of modeling and control of three-phase and dc-dc converters. His areas of interest include modeling and control, motion control and off-line applications.