Analysis of Direct-Soldered Power Module / Heat Sink Thermal Interface for Electric Vehicle Applications

by

Junhyung Kim

Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
In partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

Presented to:

Dr. Jason Lai (Chair)

Dr. Dushan Boroyevich   Dr. Dan Y. Chen

April 27, 2001
Blacksburg, Virginia

Keywords: void reduction, thermal resistance, soldering, inverter and electric vehicle

Analysis of Direct-Soldered Power Module / Heat Sink Thermal Interface for Electric Vehicle Applications

Junhyung Kim

(Abstract)

Reducing the thermal impedance between power module and heat sink is important for high-power density, low-cost inverter applications. Mounting a power module by directly soldering it onto a heat sink can significantly reduce the thermal impedance at the module / heat sink interface, as compared to the conventional method of bolting the two together with a thermal grease or some other interface materials in between. However, a soldered interface typically contains a large number of voids, which results in local hot spots. This thesis describes approaches taken to reduce voids in the solder layer through surface treatment, solder paste selection, and adjustment in solder-reflow conditions. A 15MHz scanning acoustic microscope (SAM), a non-destructive inspection tool, was used to determine the void content at the module / heat sink interface. The experimental results show that a significant reduction in thermal resistance can be achieved by reducing the void content at the soldered module / heat sink interface. Moreover, a comparison of the thermal resistances in cases using the worst soldering, which contains the largest voided area, Thermstrate^{TM} and thermal grease are presented. Thermal performances of the modules are studied by simulation with *Flotherm*.

This work was sponsored by Virginia Power Technologies (VPT) under the DOE CARAT (Cooperative Automotive Research for Advanced Technology) Program.

To my mother

Acknowledgement

It is difficult to find adequate words to express my appreciation to the many people who have contributed in countless ways to this project. To begin with, I would like to thank my advisor, Dr. Jason Lai, for his virtuous patience and continued support since I have been at Center for Power Electronics Systems (CPES). I will always be grateful to him for allowing me to become a member of the CPES. I am also grateful to my other committee members, Dr. Dushan Boroyevich for his valuable help during the course of this research, and Dr. Dan Y. Chen for taking the time to serve on my committee.

I also wish to thank all of the other CPES students for their help, especially Bo Yang, David Chen, Rengang Chen, Jinghong Guo, Xiaoyan Wang and Heath Kouns. I will not forget their all supports and guidance during my stay.

I am also thankful to the CPES staff for their assistance and kindness, especially Trish Rose, Dan huff, Elizabeth Tranter, Mike King, Suzanne Graham, Teresa Shaw, Lesli Farmer, and Steve Chen.

I like to thank Mr. Byeong-Mun Song, Dr. Seung-Yo Lee and Mr. Suk-Won Kim for their guidance and encouragement for this research.

Also, I sincerely appreciate Mr. Jae-Young Choi for his guidance and invaluable support during my days in the area of power electronics.

I have been honored to be a member in the CPES team and cherish the opportunities to work with all the CPES members. The memories of countless nights we spent working together in the lab and all discussions we had are unforgettable.

I owe a special expression of gratitude to my brother and sister for their unwavering love and support for my study in Virginia Tech.

To my beloved family, I owe perhaps the greatest debt of all. God truly blessed me with the most wonderful wife and son in the world. Thank you, Jeonghwa and Minjae.

Thank God.

Analysis of Direct-Soldered Power Module / Heat Sink Thermal Interface for Electric Vehicle Applications

Contents

Chapter I. Introduction 1

Chapter II. Thermal Management for Electric Vehicles 5

2.1. Package Consideration for Electric Vehicles 5

2.2. Thermal Impedance Issues in High-Power Inverters for Electric Vehicles 7

2.3. Thermal Impedance Reduction by Voids Control 11

Chapter III. Reducing Voids at the Soldered IGBT / Heat Sink Interface 12

3.1. Investigation of Previous Research 12

3.1.1. Characteristics of Voids 12

3.1.2. Previous Research for Reducing Voids 14

3.2. New Challenge for Reducing Voids 16

3.2.1. Proposed Approach 16

3.2.2. Experimental Setup and Direct-Soldering Process 19

3.3. Experimental Results and Discussions 26

3.3.1. Introduction of Scanning Acoustic Microscopy (SAM) 26

3.3.2. Experimental Setup for SAM 28

3.3.3. Results and Conclusions 30

Chapter IV. Thermal Coupling Test 32

4.1. Experimental Implementation 32

4.2. Measurement and Comparison of the Thermal Resistances of Cases 1,2 and 3 35

4.3. Measurement and Comparison of the Thermal Resistances in Cases Using the Worst Soldering, Thermstrate and Thermal grease (Silicon Compounds) 51

4.4. Summary 69

Chapter V. Thermal Modeling and Analysis 71
5.1. Introduction 71
5.2. Model of the IGBT/ Heat Sink Module 72
5.3. The Thermal Simulation Results 77

Chapter VI. Conclusions and Future Work 83
6.1. Conclusions 83
6.2. Future Work 84

References 85

Vita 87

Figures

Fig. 2.1. Motor/ Inverter Module 6
Fig. 2.2. The equivalent circuit of the inverter 8
Fig. 2.3. An inverter and soldered IGBT/ heat sink module 9
Fig. 3.1. The mechanism of void formation 13
Fig. 3.2. The inside structure and assembly flow of the MG50J2YS1 18
Fig. 3.3. NC-559 paste and the reflow soldering system 18
Fig. 3.4. Power module mounting arrangement 19
Fig. 3.5. The reflow profile of NC-559 21
Fig. 3.6. Procedures for providing test module 24
Fig. 3.7. The process for Case 1 25
Fig. 3.8. The reflow profile of Cases 1, 2 and 3 in the experiment 25
Fig. 3.9. A block diagram of the setup used for acoustic C-scan imaging 27
Fig. 3.10. Experimental setup for the SAM 29
Fig. 3.11. The sonix machine 29
Fig. 3.12. The acoustic images 31
Fig. 4.1. Device construction and the measuring points 33
Fig. 4.2. The experimental main circuit configuration 33
Fig. 4.3. The heat transfer mechanism of the test module 34
Fig. 4.4. The test unit 35
Fig. 4.5. The comparison of the thermal resistances at -1°C (30°F) 40
Fig. 4.6. The comparison of the thermal resistances at 49°C (120°F) 45
Fig. 4.7. The comparison of the thermal resistances at 74°C (165°F) 50
Fig. 4.8. Acoustic images showing 53
Fig. 4.9. The comparison of the thermal resistances at -1°C (30°F) 48
Fig. 4.10. The comparison of the thermal resistances at 49°C (120°F) 63
Fig. 4.11. The comparison of the thermal resistances at 74°C (165°F) 68
Fig. 4.12. Increases in thermal resistances caused by rising temperatures 70
Fig. 5.1. The construction of the geometry 73
Fig. 5.2. The geometry of the IGBT/ heat sink for 28W, 40W and 50W simulations 74

Fig. 5.3. The geometry of the IGBT/ heat sink with a large heat sink for 100W simulations 75
Fig. 5.4. The simulation results at 28W for cases using the direct-soldering method (a) and thermal grease (b) 79
Fig. 5.5. The simulation results at 40W for cases using the direct-soldering method (a) and thermal grease (b) 80
Fig. 5.6. The simulation results at 50W for cases using the direct-soldering method (a) and thermal grease (b) 81
Fig. 5.7. The simulation results at 100W with a heat sink (80*120*80) for cases using the direct-soldering method (a) and thermal grease (b) 63

Tables

Table 1.1. Thermal conductivity of interface materials ... 1
Table 4.1. The results of the thermal coupling test for Case 1, at ambient temperature -1°C (30°F) ... 36
Table 4.2. The results of the thermal coupling test for Case 2 (E1 C1), at ambient temperature -1°C (30°F) ... 37
Table 4.3. The results of the thermal coupling test for Case 2 (E2 C2), at ambient temperature -1°C (30°F) ... 38
Table 4.4. The results of the thermal coupling test for Case 3, at ambient temperature -1°C (30°F) ... 39
Table 4.5. The results of the thermal coupling test for Case 1, at ambient temperature 49°C (120°F) ... 41
Table 4.6. The results of the thermal coupling test for Case 2 (C1 E1), at ambient temperature 49°C (120°F) ... 42
Table 4.7. The results of the thermal coupling test for Case 2 (C2 E2), at ambient temperature 49°C (120°F) ... 43
Table 4.8. The results of the thermal coupling test for Case 3, at ambient temperature 49°C (120°F) ... 44
Table 4.9. The results of the thermal conductivity test for Case 1, at ambient temperature 74°C (165°F) ... 46
Table 4.10. The results of the thermal conductivity test for Case 2 (E1 C1), at ambient temperature 74°C (165°F) ... 47
Table 4.11. The results of the thermal conductivity test for Case 2 (E2 C2), at ambient temperature 74°C (165°F) ... 48
Table 4.12. The results of the thermal conductivity test for Case 3, at ambient temperature 74°C (165°F) ... 49
Table 4.13. Thermal conductivities of selected metallic solids ... 51
Table 4.14. The result of the thermal coupling test for Case a), at ambient temperature -1°C (30°F) ... 54

Table 4.15. The result of the thermal coupling test for Case b), at ambient temperature -1°C (30°F) ... 55
Table 4.16. The result of the thermal coupling test for Case c), at ambient temperature -1°C (30°F) ... 56
Table 4.17. The result of the thermal coupling test for Case d), at ambient temperature -1°C (30°F) ... 57
Table 4.18. The result of the thermal coupling test for Case a) at ambient temperature 49°C (120°F) ... 59
Table 4.19. The result of the thermal coupling test for Case b) at ambient temperature 49°C (120°F) ... 60
Table 4.20. The result of the thermal coupling test for Case c) at ambient temperature 49°C (120°F) ... 61
Table 4.21. The result of the thermal coupling test for Case d) at ambient temperature 49°C (120°F) ... 62
Table 4.22. The result of the thermal coupling test for Case a), at ambient temperature 74°C (165°F) ... 64
Table 4.23. The result of the thermal coupling test for Case b), at ambient temperature 74°C (165°F) ... 65
Table 4.24. The result of the thermal coupling test for Case c), at ambient temperature 74°C (165°F) ... 66
Table 4.25. The result of the thermal coupling test for Case d), at ambient temperature 74°C (165°F) ... 67
Table 4.26. Rth vs. temperature ... 69
Table 5.1. The size of each layer ... 73
Table 5.2. Thermal properties of materials ... 76
Table 5.3. The heat sink temperatures at 28W, 40W and 50W ... 77
Table 5.4. The sizes of the heat sink ... 77
Table 5.5. The peak temperature difference ... 78

Chapter I. Introduction

Insulated-gate-bipolar-transistor (IGBT) modules are gaining acceptance in the power electronics industry because of their high input impedance and low on-drop characteristics [1]. Recently, IGBTs are also becoming popular power devices for electric vehicle (EV) applications because EVs require high-power density, low-cost inverters. To achieve the goals of high-power density and low cost for an inverter, a new heat sink interface mounting method for the IGBT power module / heat sink is proposed. In order to attach the IGBT onto the heat sink, interface materials, such as thermal grease, thermstrate, phase- change material etc., have been conventionally used to transfer heat efficiently from a rigid, rough, uneven surface (a heat spreader of an IGBT) to another rigid, rough, uneven surface (a heat sink). Two rigid, rough, uneven surfaces may only meet at about 1/10,000 of their surface areas if the interface materials are not applied. Theoretically, they will touch at only three points [2]. The remainders of the two surfaces are separated by air, which is a very poor thermal conductor. Table 1.1 shows the thermal conductivity of major interface materials [3]. Air is 8,333 times less thermally conductive than aluminum.

Table 1.1. Thermal conductivity of interface materials.

Material	Air	Copper	Aluminum	Silver	Water	Lead
Thermal Conductivity (W/m.°K) at 300K	0.024	385	200	419	0.59	42

To remove this thermal barrier the air must be replaced by a good thermally conductive material that will contact all areas of both surfaces, even down in the little surface pores; however this is not as easy as it sounds. Some of the potential problems are as follows.

Thermal grease is inexpensive and easily conforms to rough, uneven surfaces. It readily flows into the microscopic pores of the component and the heat sink when a low closure force is applied to the component; however, it is very messy and time-consuming to apply. The end result is invariably too much or too little.

Thermstrate™ (hereafter thermstrate) is a material that does not flow and migrate. Moreover, it is clean and easy to apply; however thermstrate must be fairly thick, which increases its thermal resistance and allows it to conform fairly easily to large gaps, but which also requires enormous closure force to reach small surface pores that cover the component and heat sink surfaces. Electronic components cannot withstand such force. Sometimes the thermal resistance tests on these materials are done at 300 psi. This closure force is obtained by torquing down symmetrically spaced bolts in a laboratory test set-up, which does not exist on the production floor. No electronic component can survive such pressure.

Another considerable weakness of the both of these interface materials is that they still have high thermal resistivity due to the limitation inherent in the large areas of air contact. Therefore, the system power consumption is also limited by the relatively high thermal resistance.

The direct-soldering method can solve this problem by replacing the air with Pb67Sn33; thus, the efficiency of heat transfer is greatly enhanced. However, the direct-soldering method involves a different problem of reducing air bubbles called voids in the interface area.

There has been little research published on the individual aspects of reducing voids. Most researches are related to copper substrate bonding, wafer adhesive bonding and wire bonding.

Paul W. Barnes (1998) used a technique referred to as the pressure variation method to achieve a void-less result. The principle of the pressure variation method is the use of external gas pressure to compress the air trapped in the joint. He conducted the process with a press, a vacuum in a nitrogen environment [4].

William W. So, et al. (2000) conducted a fluxless process of fabricating In-Au joints on copper substrates. Based on the oxidation-free fluxless bonding technology, they have developed a bonding process to manufacture In-Au joints on copper substrates. The author's goal was to create void-free joints on copper substrates using a fluxless process in a high-vacuum condition [5].

Frank Niklaus, et al. (2000) presented void-free, full-wafer adhesive bonding. In their work, they defined guidelines for void-free adhesive bonding of a10cm-diameter wafer using benzocyclobutene (BCB) and a press in a vacuum condition [6].

Jin Onuki, et al. (2000) used thin Ag film and a vacuum condition to achieve a new void-free soldering process in large-area, high-power IGBT modules. Their new process consists of two steps. First, Ar^+ ions are used to clean the surfaces of the Ni-plated films on both the metal and the AIN substrates by coating them with a thin Ag film. Second, the Pb-Sn solder that is sandwiched between the two substrates is heated in a vacuum at 503K for five minutes, and then cooled in an N_2 atmosphere [7].

Shuji Sato, et al. (1999) introduced a new method to prevent voids at the interface between the IGBT and the heat sink. They used hydrogen to avoid surface deoxidizing. Their technique is relatively simple, with only the adjustment to the solder foil reflow profile [8].

Most of these previous works use some chemical materials and a vacuum to achieve the no-void condition. The new approach for reducing voids, introduced by this thesis, uses equipments, a typical solder paste and a reflow soldering system, which solders surface-mount devices (SMDs).

The proposed approach reduces voids through both solder paste selection and the soldering process itself, which includes temperature control and the pre-heating process. When the solder paste is heated, a white smoke, which is a gas emission from the flux, is

observable. When the preheated heat spreader of IGBT is attached to the heat sink with the melted paste, the surrounding air can presumably be captured inside the joint area because it traps air when the paste melts inconsistently. To eliminate emissions from the paste and absorption of gas from surrounding areas, it is worthwhile to lengthen the time for which the area around the paste is soaked. When the paste is heated, it changes first to a gel state, then to liquid. If a constant temperature could be maintained in the soak zone of the interface, thus prolonging the gel state, then the paste could be flattened and melted at the same time. Therefore, one requirement is that the preheated heat spreader of IGBT be assembled on the heat sink after the gas emissions have dissipated from the paste. Three different cases are used in the experiment to make a voids-rate comparison.

A comparison of heat distribution for both direct-soldered and thermal grease cases is presented by *Flotherm* simulation at 100W power loss. It can predict different heat distributions of each case at 100W.

In Chapter II, both the significance of packaging for electric vehicle applications and the necessity of direct-soldering at the interface between the IGBT and the heat sink are explained.

In Chapter III, the previous research projects aimed at reducing voids are introduced. The improvement of thermal contact by void reduction at the soldered IGBT / heat sink interface, without using chemical materials or / and a vacuum, is also discussed. Both the experimental process for void reduction and the results of the experiment are given. The void formations are inspected by a scanning acoustic microscope (SAM).

In Chapter IV, thermal resistance measurements are taken by thermal coupling tests conducted at 0°C, 50°C and 75°C, and the results of the thermal resistances are compared by a graph.

In Chapter V, thermal resistances obtained by the preceding experiments are simulated by *Flotherm*, a thermal analysis tool. A comparison of heat distribution for both direct-soldered and thermal grease cases is presented by *Flotherm* simulation.

Conclusions are drawn in Chapter VI. Future research projects are also suggested in this chapter.

Chapter II. Thermal Management for Electric Vehicles

2.1 Package Consideration for Electric Vehicles

Integration of an inverter for a 75hp high-speed induction motor, which is especially designed for electric vehicle, is rather complex, due to the incompatibility of materials and the high power level. Moreover, high-density packaging creates high heat fluxes within a limited area and volume for thermal dissipation. As the power density of power inverters continues to grow, packaging issues for the treatment of these heat fluxes become increasingly important and vital for product size and quality.

Figure 2.1 shows miniaturization of the motor / inverter module. This is a significant improvement in the packaging of electric vehicles, because a small module can reduce both weight and price of the vehicles. However, the small module size creates makes a problem of heat transfer. In this thesis, reducing the thermal impedance between power device case and heat sink is a main focus toward reducing the conduction and switching losses as well as improving system stability, which is unsatisfactory in current models due to some components sensitivities in temperature.

As mentioned, thermal management is a considerable challenge in the recent project because the induction motor uses a smaller heat sink and lower-rating power devices than do the usual compact motor-inverter modules. To realize the high- power density, low-cost inverter, soldering the power device onto the heat sink is a challenging method when assembling the module.

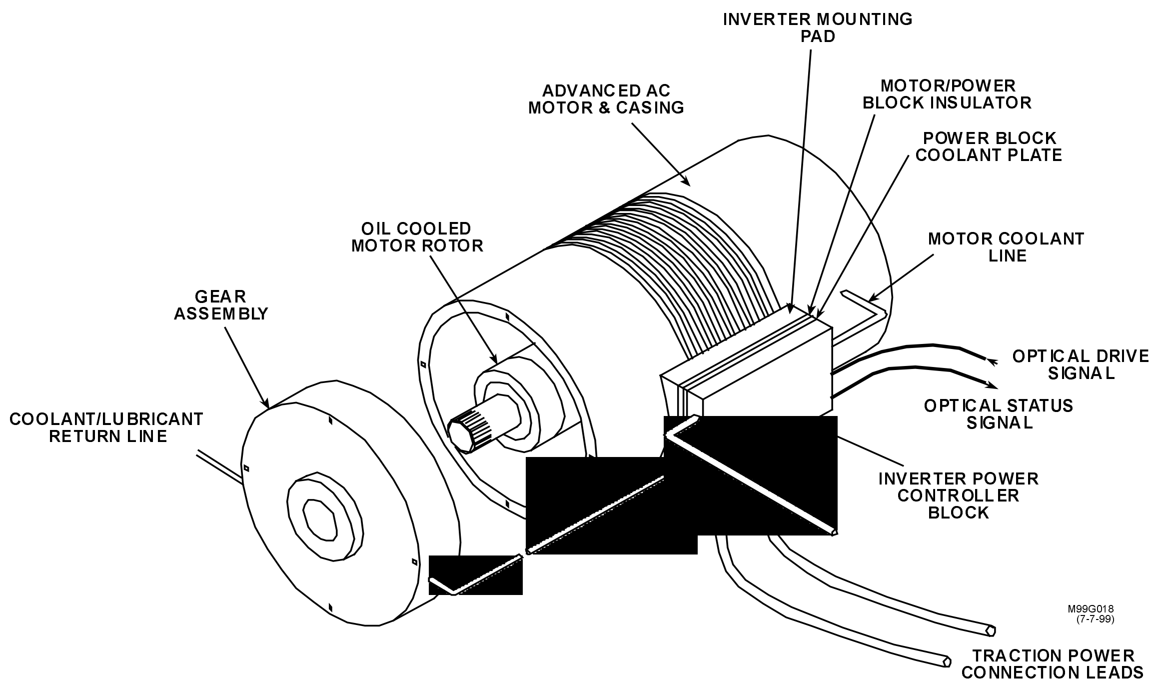


Figure 2.1. Motor / inverter module.

2.2 Thermal Impedance Issues in High-Power Inverters for Electric Vehicles

The thermal impedance between the semiconductor junction and the heat sink limits the power available to the power device during short-term periods of high power, such as acceleration or hill climbing. In this thesis, the insulated gate bipolar transistor (IGBT) is used as a power device. The thermal interface between the IGBT case and the heat sink represents a significant portion of the junction to sink thermal impedance.

The automotive specifications dictate that the system must meet certain levels of torque and power when operating in a 50°C ambient temperature environment. It is also known that conventional cooling systems cannot sustain a heat sink even at temperatures of less that 20°C above the ambient. Since silicone power devices such as IGBTs are generally rated for a maximum safe operating temperature of 150°C, during transient overload periods, the system is limited to maximum power levels that will result in a maximum difference of 80°C between the IGBT junction temperature and the heat sink temperature. In previous tests by Virginia Power Technologies (VPT), it has been found that at zero speed and maximum torque (300 A motor-line current), the temperature difference between the IGBT base plate and the heat sink (directly under the base plate) is 40°C, representing 50% of the available temperature gradient. Figure 2.2 shows the equivalent circuit of the inverter and the concentrated area of this research, R_{c-s}.

This thermal resistance R_{c-s}, commonly known as the case-sink thermal impedance, clearly limits the maximum power level that can be safely developed during hill climbing and acceleration periods. The contact thermal resistance between the IGBT base plate and the heat sink is related to the flatness and finish of the two contacting surfaces, and to the pressure developed by the mounting system. Various products for minimizing the case-sink thermal impedance are available in the marketplace, and the product known as thermstrate is presently used in inverters for VPT [9].

In this research, especially, the use of a soldered interface is investigated.

In summary, reducing the size of the power inverter in electric vehicles is a critical issue because of the limited space available under the hood. However, when the power inverter's size is reduced, heat dispersal becomes problematic. Since the power density of inverters continues to grow, thermal issues are becoming extremely important and vital for product quality, especially for electric vehicles. When the 300A current flows through the IGBT, the IGBT generates several hundreds watt of heat. Finding a way both transmit this heat out of the IGBT module and to raise durability to a level comparable to that of the modules typically used in cars was yet another development challenge.

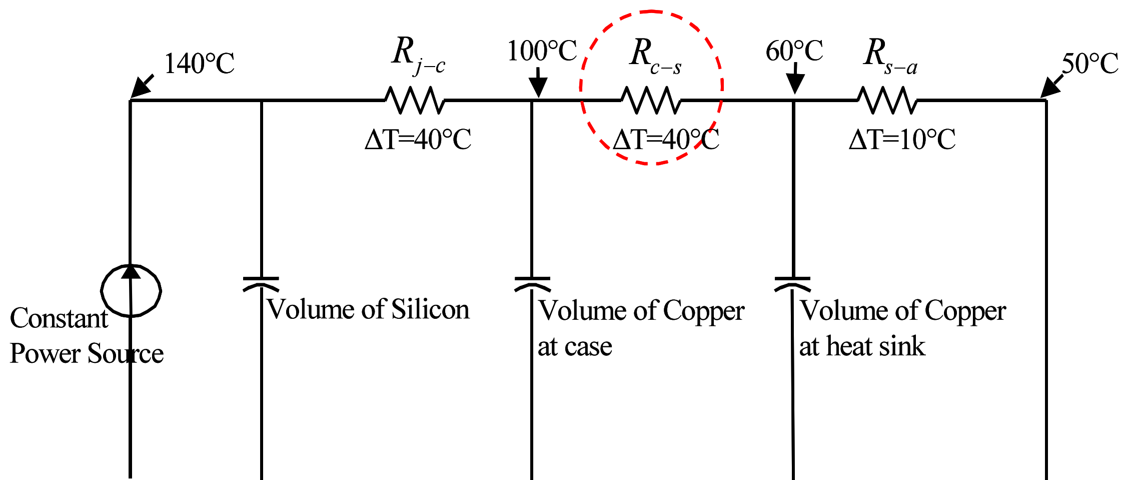


Figure 2.2. The equivalent circuit of the inverter.

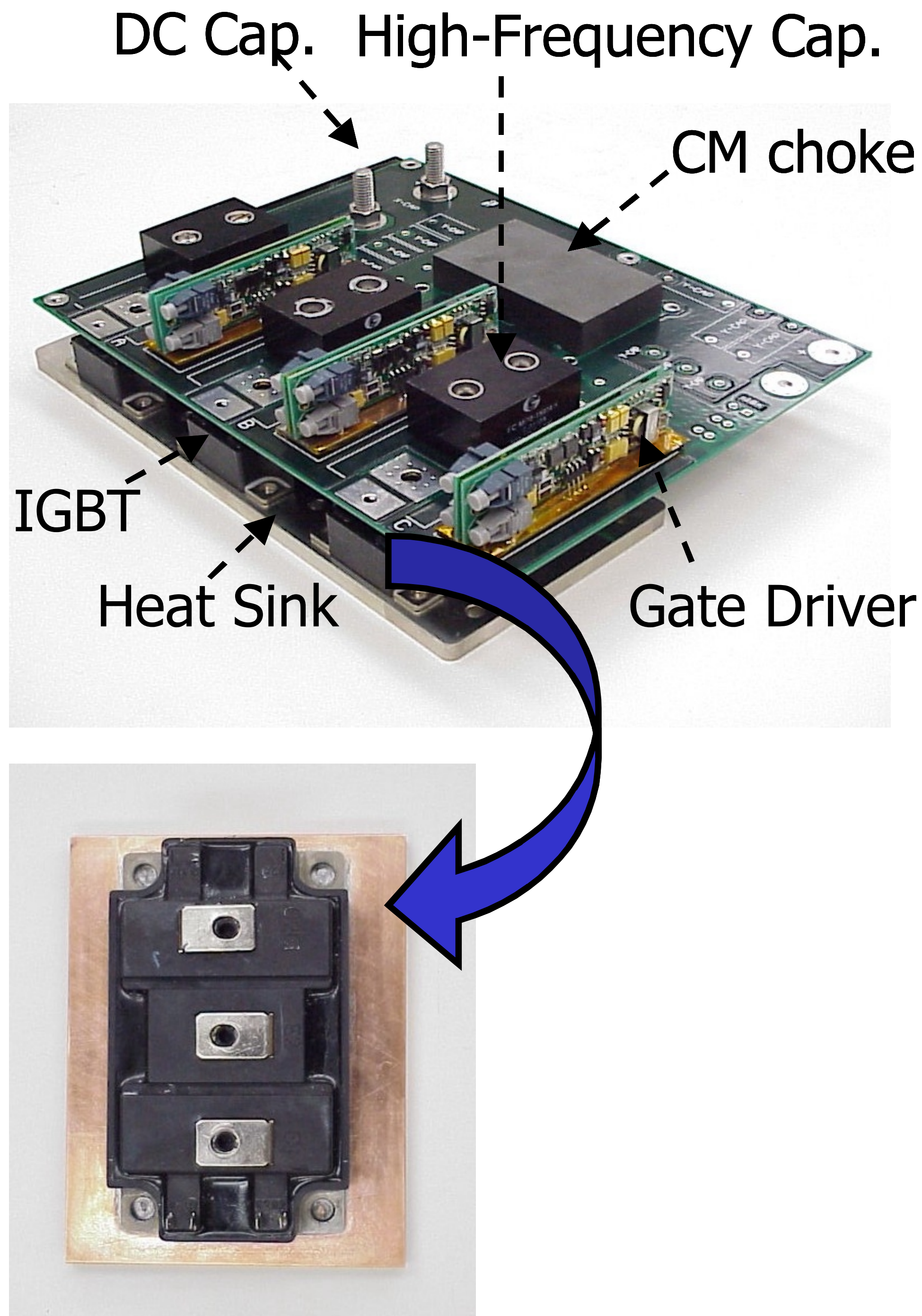


Figure 2.3. An inverter and soldered IGBT/ heat sink module.

In the past, thermal grease (silicone compound) was used to attach the power module to the heat sink. Thermstrate has also been used because of its better thermal conductivity at high temperatures. Recently, the direct-soldering method is developed to achieve better thermal conductivity.

The proposed research mainly focuses on characterization of the thermal impedance of the solder interface between the IGBT base plate and the heat sink. Figure 2.3 shows a well-packaged inverter for electric vehicle applications and a soldered IGBT / heat sink module.

The module in Figure 2.3 will be housed in a water-cooled aluminum case lined with grease. Accordingly, the heat generated by the IGBT is radiated in the following path: silicone →solder → IGBT case →solder →heat sink →grease →aluminum case → coolant.

By reducing the thermal impedance of the soldered IGBT / heat sink, better thermal conductivity can be achieved; however, when assembling the module, soldering quality imposes another challenge. If the soldering leaves many air bubbles, the thermal conductivity can be worse than when thermal grease is used.

2.3 Thermal Impedance Reduction by Voids Control

Power modules that integrate power devices such as power diodes and switches, either metal oxide field effect transistors (MOSFETs) or IGBTs are widely used in high-power electronics systems because they simplify system design, improve system performance and reliability, and reduce system cost. To prevent the power modules from overheating due to the generated heat that results from power loss, the modules are cooled by mounting them on heat spreaders or sinks. In mounting the power modules, thermal grease, thermstrate and solder have been used to establish good thermal contact between the module and the heat spreader or sink by eliminating surface irregularities. Recently, the direct-soldering technique for mounting power modules was employed in building inverter-motor propulsion drives for hybrid electric vehicle applications [10]. A problematic issue found in using the soldering method is the existence of voids at the soldered interface, which results in local hot spots. The voids increase thermal impedance, heat losses, cracks, and delaminating at the interface between the power device and the heat sink. The two major causes of void formation at the solder interface areas are absorption of gas from the surrounding area and emission of gas from the solder paste when it is melted. Therefore, eliminating these two factors from the soldering process can substantially reduce voids.

A few methods for reducing voids in large areas, such as IGBT base plates, will now be discussed. In Chapter III, methods for reducing voids in the interface area are introduced.

Chapter III. Reducing Voids at the Soldered IGBT / Heat Sink Interface

In this chapter, methods for reducing voids at the soldered interface, without using special chemical materials or a vacuum, are explained. Previous research into reducing voids and the SAM inspection tool are also introduced.

3.1. Investigation of Previous Research

3.1.1. Characteristics of Voids

A. Mechanisms of void formation:

- Solidification of molten metals; minimization of free energy, which dictates the spherical shape [Klein]
- Mechanical entrapment of air that surrounds the liquid solder material [Der Marderosian]
- Flux undergoes a chemical reaction when tarnish films are removed from metallized substrates [Roos-Kozel]
- Out-gassing is caused by the flux in the paste [Manko]
- Amount of out-gassing flux gets entrapped in the solder during reflow; bubbles are entrapped within liquid solder [O'Hara]
- Gas generation by the metallization of substrates, components or the solder powder surface during fluxing [Prasad]
- Physical evaporation of the solvents and rheological additives in the paste vehicle; moisture present or incomplete curing of the laminate [Klein]
- Stress applied during processing [Roos-Kozel]
- Solder melts inconsistently within the surface, then it traps air [Shuji Sato et al.]

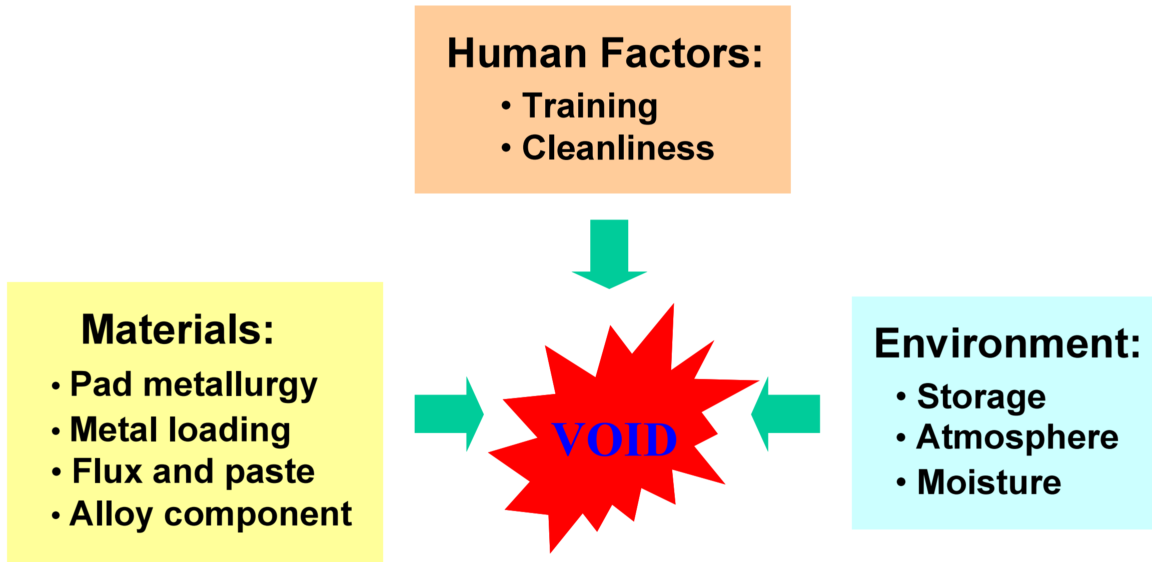


Figure 3.1. The mechanism of void formation.

B. Void Theory

- Covered joints are less likely to expel voids than are uncovered joints
- Amount of large voids increases when the total void content is higher
- Void motion within a joint due to temperature gradients (re-circulation flow) indicates that the greater the total gas volume produced, the greater the probability of coalescence

3.1.2. Previous Research for Reducing Voids

There has been little research published on the individual aspects of reducing voids. Most research is related to copper substrate bonding, wafer adhesive bonding and wire bonding.

Paul W. Barnes, et al. (1998) used a technique referred to as the pressure variation method to achieve a void-less result. The principle of the pressure variation method is the use of external gas pressure to compress the air trapped in the joint. He conducted the process with a press, a vacuum in nitrogen environment. The critical point is to sustain the ability to precisely control the vacuum, gas pressurization, heat ramp and heat dwell step, and temperature uniformity.

William W. So, et al. (2000) conducted fluxless process of fabricating In-Au joints on copper substrates. Based on the oxidation-free fluxless bonding technology, they have developed a bonding process to manufacture In-Au joints on copper substrates. The dice are deposited with an indium- rich Au / In / Cr multilayer structure in a single high-vacuum cycle to prevent oxidation. Immediately following deposition, the outer Au layer interacts with the In layer to form an $AuIn_2$ inter-metallic compound. This compound is quite stable, and can thus protect the In layer against oxygen penetration when it is exposed to the ambient environment. On the other hand, Oxidation can easily be prevented by the use of molten In during the bonding process. The substrate is deposited with Cr and Au. The dice are bonded to the substrates at 180°C in an inert environment. Nearly void-free joints have been obtained, as examined by a 75MHz SAM. The author’s

goal is to create void- free joints at copper substrates using a fluxless process in a high-vacuum condition.

Frank Niklaus, et al. (2000) presented void-free full-wafer adhesive bonding. In their work, they defined guidelines for void-free adhesive bonding of a10cm-diameter wafer. The author of this paper has systematically investigated the influence of different bonding parameters on void formation in the bond. The polymer material, the bonding pressure, pre-curing time, and temperature for the polymer have shown significant influence on void formation. Process parameters for achieving void-free bonds using benzocyclobutene (BCB) and photo-resist coatings as adhesive materials are given.

Jin Onuki, et al. (2000) used thin Ag film and a vacuum condition to achieve a new void-free soldering process in large-area, high-power IGBT modules. A new void-free process for the solder joint between a chip-mounted AIN substrate and a metal substrate for use in large-areas has been investigated. The following new process consists of two steps. First, the Ar^+ ions are used to clean the surface of the Ni-plated films on both the metal and the AIN substrates by coating them with a thin Ag film. Secondly Pb-Sn solder that is sandwiched between the two substrates is heated in a vacuum at 503K for five minutes, and then cooled in an N_2 atmosphere.

Shuji Sato, et al. (1999) introduced a new method to prevent voids at the interface between IGBT and heat sink using a solder foil. They used hydrogen to avoid surface deoxidizing to achieve the goal. Their technique is relatively simple, because of the adjustment they made to the solder foil reflow profile.

Most of this previous work uses some chemical material and a vacuum to achieve the no-voids condition. The new approach for reducing voids, introduced by this thesis, uses equipments that solder of surface-mount devices (SMDs).

3.2. New Challenge for Reducing Voids

3.2.1. Proposed Approach

The two major causes of void formation at the solder interface areas are absorption of gas from the surrounding area and emission of gas from the solder paste when it is melted. Therefore, eliminating these two factors from the soldering process can substantially reduce voids. Research has been conducted in the use of different materials for void reduction [5 – 7]. Temperature profile control can also be used to reduce voids [8]. The proposed approach reduces voids through both solder paste selection and the soldering process itself, which includes temperature control and the pre-heating process.

The solder paste used in this experiment is NC-559 paste (Pb-Sn), which is a no-clean solder cream, is VOC-free, halide-free and non-hygroscopic, and is designed to meet the requirements for reliable solder joints in SMD PC board assemblies. This cream was formulated to replace RMA, a kind of solder paste, and water-soluble solder creams, and often the benefit of eliminating the added steps, cost and potential hazards of cleaning by solvents or water. This formula was designed to have a wider process window and better compatibility than previous no-clean formulations. This cream exhibits long print life in continuous-printing operations. Customers who have long delays between print strokes, however, may need to re-shear the cream upon resumption of printing.

SIKAMA's lowest-priced reflow soldering system is a full-featured reflow machine that is capable of handling moderate production runs of SMDs and hybrid circuits, as well as curing adhesives and soldering components. This system, generally used to solder SMDs in the lab, was used to realize a reduced number of voids. Its compact tabletop size makes it a perfect fit in a prototyping lab or rework station. A Toshiba N-channel IGBT, the MG50J2YS50 (91mm × 33.3mm), and Ni-plated copper heat sink (105 mm × 48 mm) are used for this experiment. Figure 3.2 shows the inside structure and assembly flow of the MG50J2YS50. Figure 3.3 shows the NC-559 paste and the conduction soldering system.

An SAM [11] is the inspection tool used to observe void formation. The thermal impedance resulting from different soldering processes was characterized using a constant current source injection into the power diode. The junction temperatures can be calculated based on the diode voltage drop. The heat sink and case temperatures are observed with temperature probe measurements, and the thermal impedance is then calculated using the measured temperature and injected power.

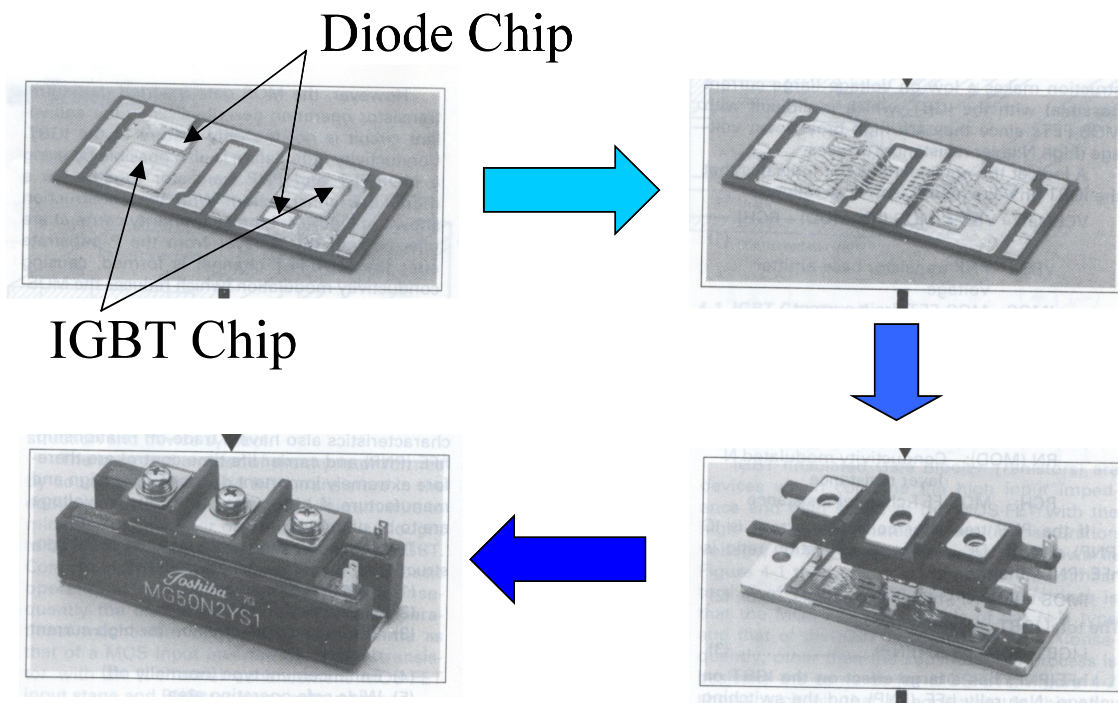


Figure 3.2. The inside structure and assembly flow of the MG50J2YS1.

Figure 3.3. NC-559 paste and the reflow soldering system.

3.2.2. Experimental Setup and Direct-Soldering Process

A. Module Mounting

Figure 3.4 shows the arrangement for mounting the IGBT module on top of the heat sink plate. In conventional mounting methods, the power module is bolted down, and the interface material between the IGBT power module and heat sink plate is typically thermal grease, which reduces the air gaps in between and thus reduces the thermal impedance. With the direct-soldered method, there is no need for bolting, and the interface material is the melted solder.

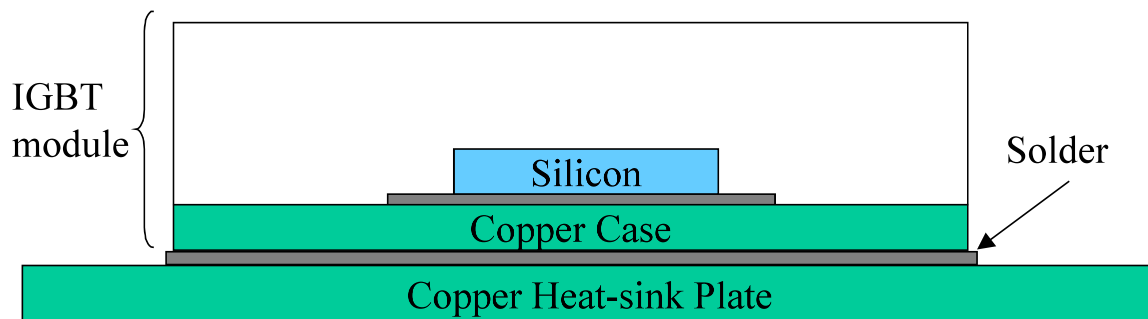


Figure 3.4. Power module mounting arrangement.

When direct-soldering the IGBT module onto the heat sink, one of the most important challenges involves void reduction. Since there are two ways in which voids are formed, any effort to eliminate those two factors will be effective in reducing the incidence of voids. The solder material can be solder foil or paste. In this research, NC-559 solder paste is used. The ultimate goal of the typical NC-559 reflow process is to achieve high-quality solder joints on all of the component leads of a particular assembly, and to do this consistently. The process involves heating the leads, pads and cream above the melting point of the alloy so that the solder on the leads and pads and in the cream reflows into a homogenous fillet. Consistency in the process is dependent on the ability to control the application of heat, as well as, the variation of heat both across the board and from board

to board. This controlled heating is called the profile. The typical profile includes three zones: preheat, dry or soak, and reflow or spike. The goal of the preheat zone is to uniformly bring the assembly up to temperature, uniformly, generally at a rate of 2°C per second or less. This will minimize the potential for thermal shock to the components that may occur due to varying heat capacities. The preheat zone also begins to dry out some of the solvents added to the cream for printing and releasing. The second zone continues the drying out of solvents to prevent out-gassing and possible spattering of the cream. This zone, sometimes called the soak zone, is also where the flux begins to remove the oxides from the surfaces of the leads, pads, and the cream itself. The resins and / or higher-boiling-point solvents remain as a cover to prevent the re-oxidation that would readily occur at elevated temperatures. In the reflow or spike zone, the temperature is quickly raised 20-40° C above the melting point of the alloy. It is here that the solder wets the surfaces and forms the intermetallic bonds. The intermetallics of Pb63/Sn37 and other high-tin alloys with copper are Cu3Sn on the copper side, and a relatively irregular and rough Cu6Sn5 on the solder side. The period of time above reflow is called the dwell time, and is typically 30-60 seconds long. The dwell time should be long enough to allow for all of the joints to reach temperature and form bonds. A dwell time that is too long can lead to excessive intermetallic formation. Both of the intermetallics are brittle, and if they make up a large portion of the fillet they can lead to premature failure of the joint. Figure. 3.5 shows the reflow profile of NC-559.

The recommended profile is not a line, but is instead a zone or band. The width of this band is defined by the upper and lower temperatures that will still give satisfactory results for the particular cream. This band is also referred to as part of the process window: the larger the band, the larger (or more forgiving) the window.

Besides variation across the board, there can also be have variation across the oven. This is sometimes caused by the heat sinking of the conveyer system, the air-flow variations near the sides, or non-uniformity across the heating element. Another source of variation is from the ability of an oven to hold temperature and recover after a board passes through. This is called the load factor of the oven. This will vary from oven to

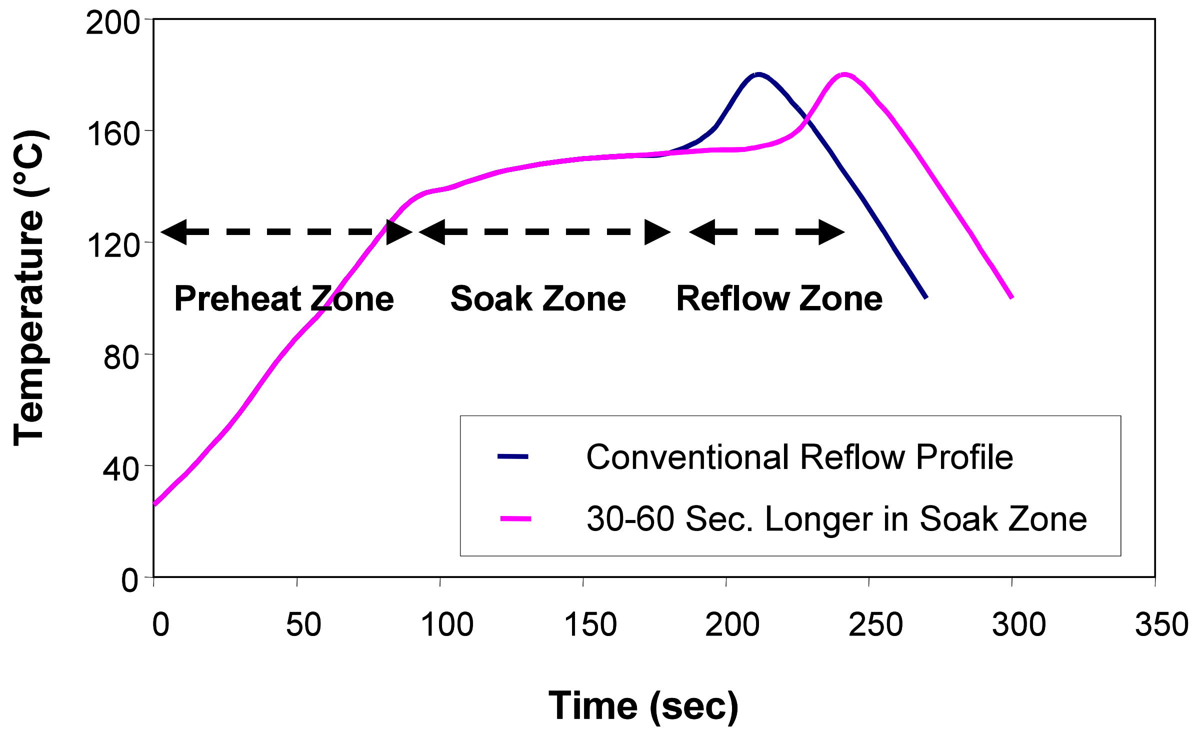


Figure. 3.5. The reflow profile of NC-559.

oven, but a starting point would be between one-half and one board length between boards. The actual method of heating is not as important as the ability to control the heating in a repeatable manner [12].

B. Soldering Process

When solder paste is heated, a white smoke, which is a gas emission from the flux, is observable. When the IGBT is attached to the heat sink with the melted paste, the surrounding air can presumably be captured inside the joint area because it traps air when the paste melts inconsistently. To eliminate emissions from the paste and absorption of gas from surrounding areas, it is worthwhile to lengthen the time for which the area around the NC-559 paste is soaked. When the paste is heated, it changes first to a gel state, then to liquid. If a constant temperature could be maintained in the soaking zone of the interface, thus prolonging the gel state, then the paste could be flattened and melted at the same time. Therefore, one requirement is that the IGBT be assembled on the heat sink after the gas emissions have dissipated from the paste. There are three cases used in the experiment to make a voids-rate comparison.

Case 1: The IGBT and heat sink are first immersed in a solution of 20% H_2SO_4 to clean the surfaces, and then the bottom of the IGBT and the heat sink are scrubbed by a fine sand paper. The scrubbing action is a common technique for removing oxide from a base metal. Second, the surfaces are cleaned using acetone and alcohol to re-deoxidize, and then high-temperature insulation tape is applied to the heat sink as a guideline for placing the module. Third, 1.4g of the paste is spread uniformly on the untaped area, and then the IGBT is assembled on the paste of the heat sink. To maintain the position of the IGBT on the heat sink when they are baked, two screws are mounted into two holes of the heat sink.

Finally, the unit is baked on a conduction soldering system following the suggested NC-559 reflow profile that is shown Figure 3.5. The soak zone is almost 60 seconds longer than the conventional profile in order to allow sufficient time for dissipation of the gas emissions. In an experiment setup, it is very difficult to sustain the recommended

profile because of human factors, different environments, etc. The detailed data pertaining to the profile for each case will be presented.

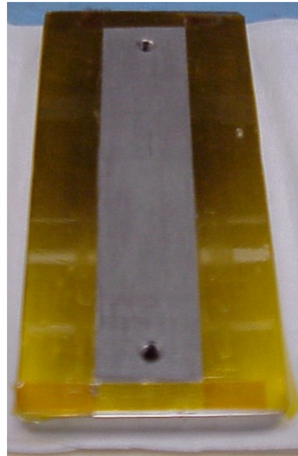
Figure 3.6 shows the process involved with preparing the heat sink. Figure 3.6 (a) shows a clean heat sink; Figure 3.6 (b) shows the separation of the taped area and the paste area; Figure 3.6 (c) shows the IGBT module sitting on top of the heat sink. Figure 3.7 shows the process for Case 1.

When Case 1 is baked, some white gas is observable from each edge of the IGBT. An acoustic image (see Figure 3.6 (a)) shows that the edges are very dark. The results indicate there are no voids, which seems to say that the voids can be reduced from the joint area if the IGBT is attached after the white smoke is gone. That idea is reflected in the Case 2.

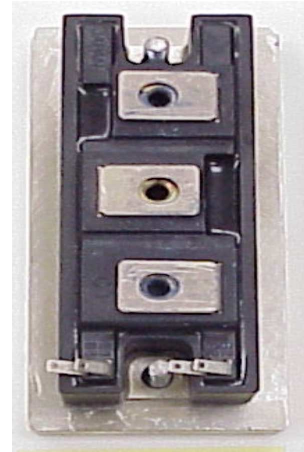
Case 2: For the second case, the procedure is the same as that through the second step of the first case. However, to eliminate emissions from the paste and to melt the paste constantly, the IGBT is placed on the heat sink just after the paste is melted. During the extended soak zone, both factors should be eliminated. However, the temperature falls drastically when the IGBT is attached at the melting point. From this phenomenon, it is expected that the melted paste will be partly solidified at the instant at which the cold heat spreader of the IGBT makes contact. Preheating the heat spreader of the IGBT could prevent the solidification. This idea is reflected in Case 3.

Case 3: For the third case, the procedure is the same as for the second case, except that the bottom of the IGBT is heated before it is attached to the heat sink. However, care should be taken to avoid oxidization of IGBT's heat spreader. In the experiment, the IGBT was heated to 120°C by the conduction soldering system.

(a)



(b)



(c)

Figure 3.6. Procedures for providing test module: (a) the clean heat sink; (b) the heat sink with NC 559 paste; (c) the heat sink with IGBT module.

Figure 3.7. The process for Case 1.

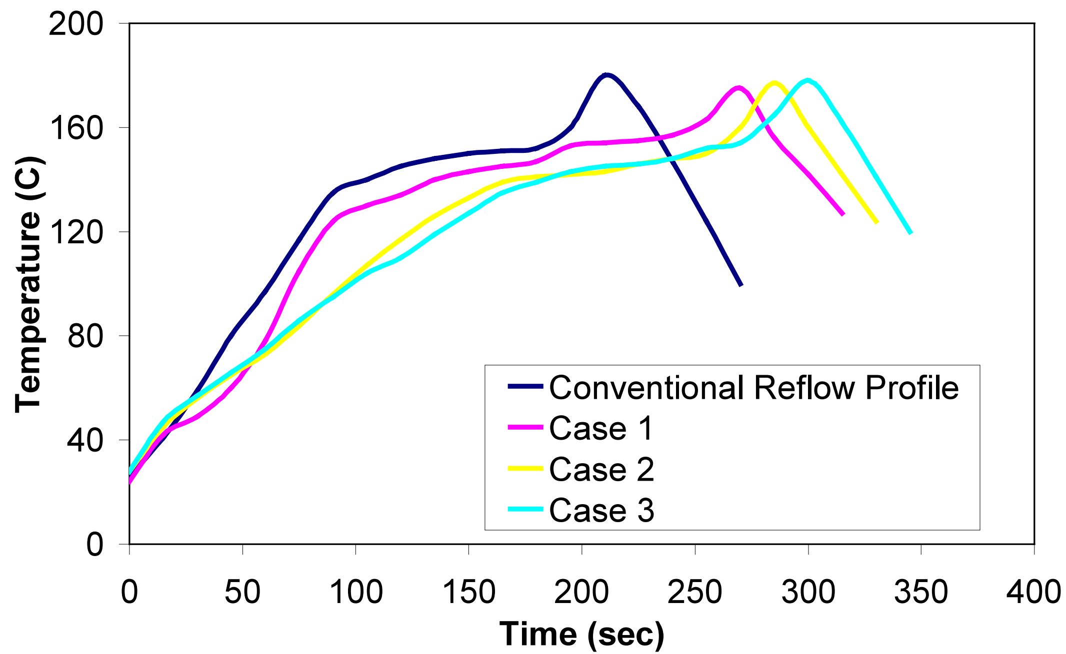


Figure 3.8. The reflow profile of Cases 1, 2 and 3 in the experiment.

3.3. Experimental Results and Discussions

3.3.1. Introduction of Scanning Acoustic Microscopy (SAM)

The SAM is of particular interest for investigating subsurface features in materials, such as voids, pores and cracks.

The first acoustic microscopes were built in the early 1970s [13-16]. Lemons and Quate [15] developed the first SAM in 1974. Two kinds of acoustic microscopes are generally in use—point focus and line focus. SAMs are of the point-focus variety, in which a focused beam is scanned over and penetrates a specimen immersed in water; the depth of penetration depends on the acoustic frequency and material properties. With the SAM, interference fringes are eliminated because the acoustic energy is focused over a diameter of less than one wavelength, and the image is formed by scanning one point at a time [17]. The microstructures of specimens prepared for metallographic examination can also be investigated using an SAM because different phases have different elastic constants.

The Lemons and Quate microscope [15] employed a through-transmission approach and was used to image a 200-mesh copper electron microscope grid. With the through-transmission technique, one transducer sends the signal while another receives it. The SAM used in the work described here, however, uses the reflection technique, whereby a single transducer sends and receives the signal. This circumvents the problem of aligning two transducers.

The transducer is made of piezoelectric ZnO sandwiched between layers of gold; the lens is made of single-crystal sapphire or silicon, both of which have high velocities of sound as compared to the water couplant [16,17]. The attenuation of acoustic waves is small in single-crystal sapphire and silicon, which is another reason for their use in lenses [18]. An early SAM for detecting internal flaws in materials was developed by Gilmore, et al [19]. Their system uses broadband acoustic pulses with a center frequency in the range of 10-100MHz and a single-crystal silicon acoustic lens.

Figure 3.9 shows the mechanism of the SAM used in this thesis.

Acoustic microscopy has many applications for the study of material properties and phenomena [17,18,20-22].

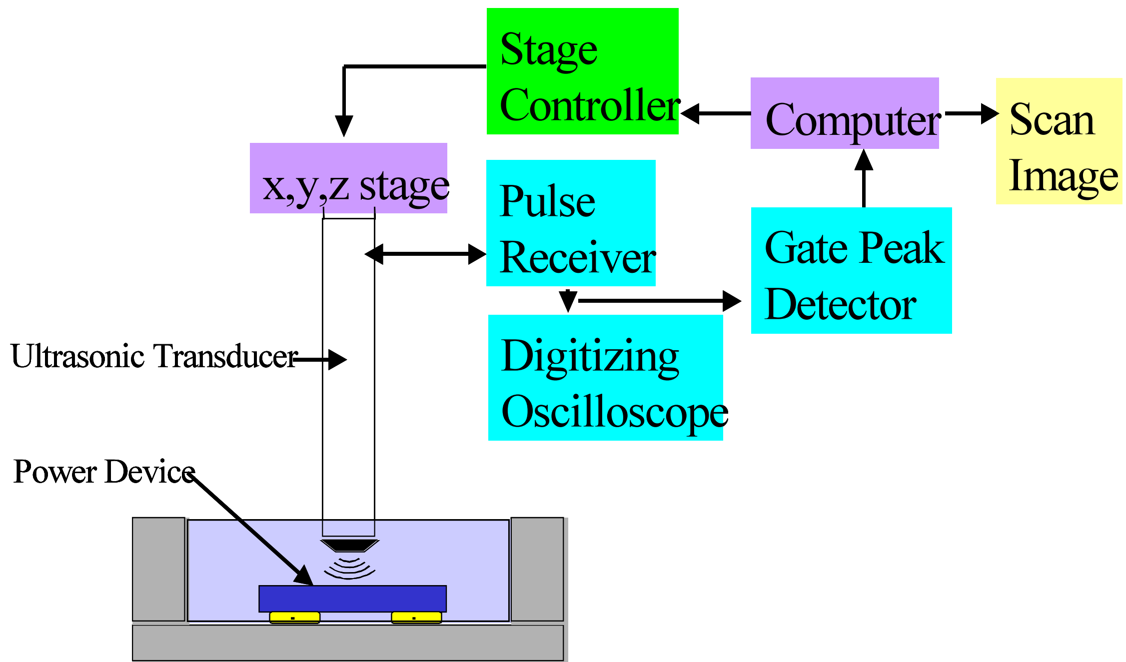


Figure 3.9. A block diagram of the setup used for acoustic C-scan imaging.

3.3.2. Experimental Setup for the SAM

In order to characterize the soldered interface, an SAM will be used to image the module with a 15MHz, 1.5” focal-length transducer. The soldered device is put into water for scanning. To scan the soldered interface of the device, the capturing section should set on the solder attach zone shown in Figure 3.10 To achieve optimal resolution, the gain can be adjusted. The test procedures are as follows.

1) Immerse device in water and hold it.
2) Adjust transducer’s focus
3) Set the scanning section
4) Set gain for good resolution
5) Choose C-scan

Figure 3.11 shows the Sonix machine and SAM experimental setup.

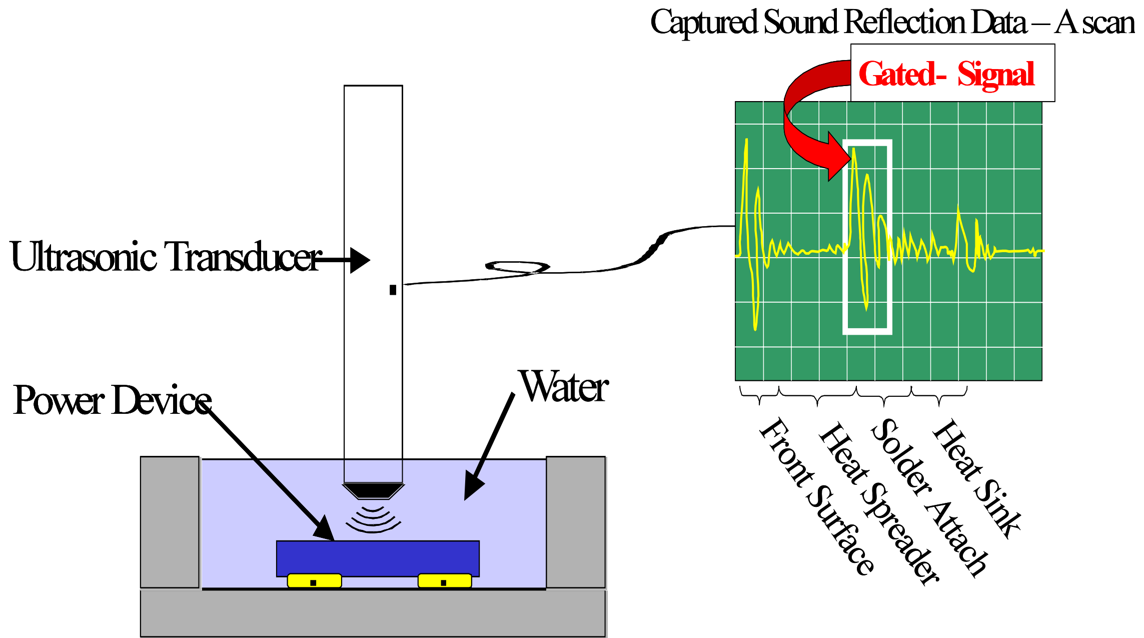


Figure 3.10. Experimental setup for the SAM.

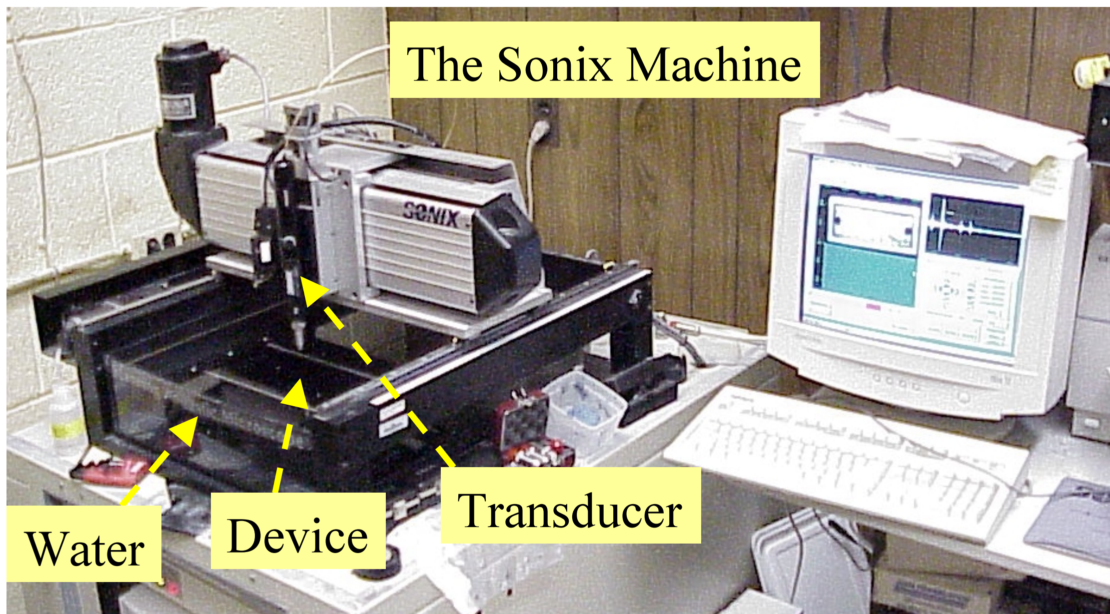


Figure 3.11. The sonix machine.

3.3.3. Results and Conclusions

Results

To evaluate the quality of the solder joints, the SAM is now employed. Voids show up with very high contrast in acoustic images because of mismatches in acoustic impedance between the voids and surrounding material. The image of Case 2 shows fewer void formations than that of Case 1. Figure 3.12 shows the acoustic images of Cases 1, 2, and 3.

Conclusions

In summary, new processes that do not require the use of a vacuum or other chemical materials have been applied to reduce voids in solder joints. While the concept for reducing voids in solder joints is relatively simple, the implementation can be difficult because of many unexpected factors during the experiments. Voids can be developed in the solder joint between the IGBT and the heat sink if the processes are not done carefully; moreover, these voids impede the thermal conductivity. Chapter IV proposes a way to measure thermal resistance in order to discover a relationship between the void rate and the thermal resistance of a device. This relationship could point to a link between fewer voids and low thermal resistance.

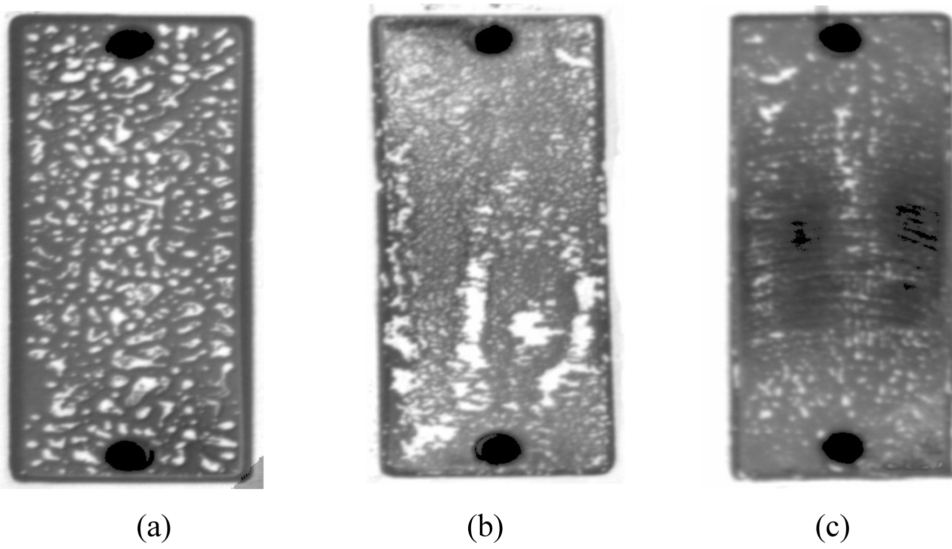


Figure. 3.12. The acoustic images: (a) Case 1; (b) Case 2; and (c) Case 3.

Chapter IV. Thermal Coupling Test

In this chapter, to obtain the thermal resistances, the thermal coupling test of the direct- soldered IGBT / heat sink module is illustrated. This type of test will show the thermal resistances of Cases 1, 2 and 3, which are described in Chapter III, in addition to other cases, which use thermstrate or thermal grease (silicon compounds). The thermal resistance of each case is obtained by calculation. Then, the comparison of the thermal resistance for each case will be presented by graph. The experimental setup for the test is also shown.

4.1. Experimental Implementation

The purpose of the experiment is to determine the effect of both voids formations and interfacial materials used to attach the IGBT to the heat sink on thermal conductivity. The IGBT / heat sink module for the test is shown in Chapter III. A diode in the IGBT module will be supplied a 20A constant current source. Moreover, the module will be set in a thermal chamber to maintain a constant ambient temperature for the heat sink. A digital thermometer will measure the temperatures for the heat spreader of the IGBT and the bottom of the heat sink every 15 seconds and a multi-meter will measure the forward voltage drop of the diode. The surfaces on which the measuring points will be located are cleaned and scrubbed before the test is conducted.

Figure 4.1 shows the device construction and the measuring points.

Figure 4.2 shows the circuit for the test.

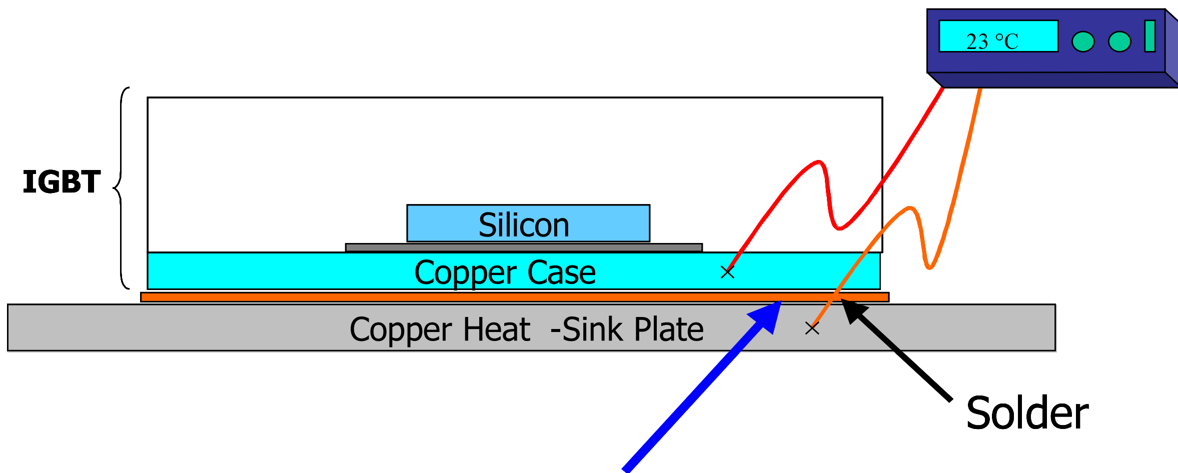


Figure 4.1. Device construction and the measuring points.

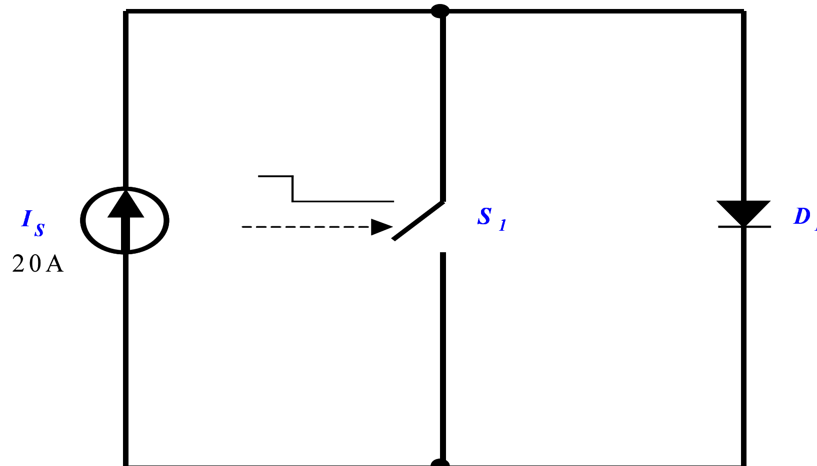


Figure 4.2. The experimental main circuit configuration.

If a constant 20A current is applied E2 through C2 of the IGBT module, then the current flows through the diode of the IGBT module, and the temperature of the IGBT module (Tc) will be increased by the power loss, 20A*Vf. By increasing the temperature of the IGBT module, the temperature of the heat sink (Ts) will also increase. The heat is transferred from the silicon to the IGBT case, and then to the solder, and then to the heat sink. Figure 4.3 shows the heat transfer mechanism of the test module.

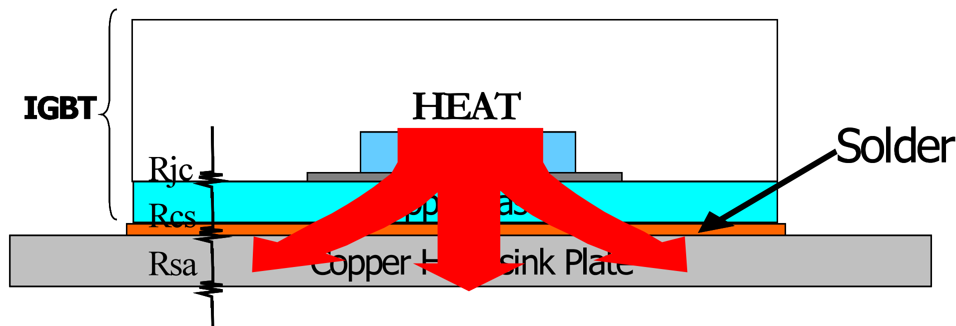


Figure 4.3. The heat transfer mechanism of the test module.

The purpose of this chapter is to investigate R_{c-s} for Case 1, 2 and 3, as well as in cases using Thermstrate and thermal grease. Accordingly, Tc, Ts and the applied power for the IGBT module should be known by measurement, as follow:

$$R_{c-s} = \frac{\Delta T}{P} = \frac{Tc - Ts}{20A * Vf},$$

where Tc is the temperature of the IGBT case,

Ts is the temperature of the heat sink, and

Vf is the forward voltage drop of the diode in the IGBT module.

In theory the measurement of R_{c-s} is simple, but it has proven very difficult to duplicate measurements amongst different test labs. There are too many variables involved, including the type of package, the heat sink flatness and finish, and such environmental factors as time, pressure and temperature.

4.2. Measurement and Comparison of the Thermal Resistances for Cases 1, 2 and 3

To measure Tc, Ts, and *Vf* , the test unit is built up as shown in Figure 4.4. Ch1 and Ch2 are the input lines of the digital thermometer; Ch1 measures the temperature of the IGBT heat spreader, and Ch2 measures the temperature of the heat sink.

The test results for Case 1, 2 and 3 are shown by the following tables. Case 2, two tests are conducted by connecting E1, C1 and E2, C2 because of the unregulated void formation of case 2. See the Figure 3.12 (b) for acoustic image of Case2.

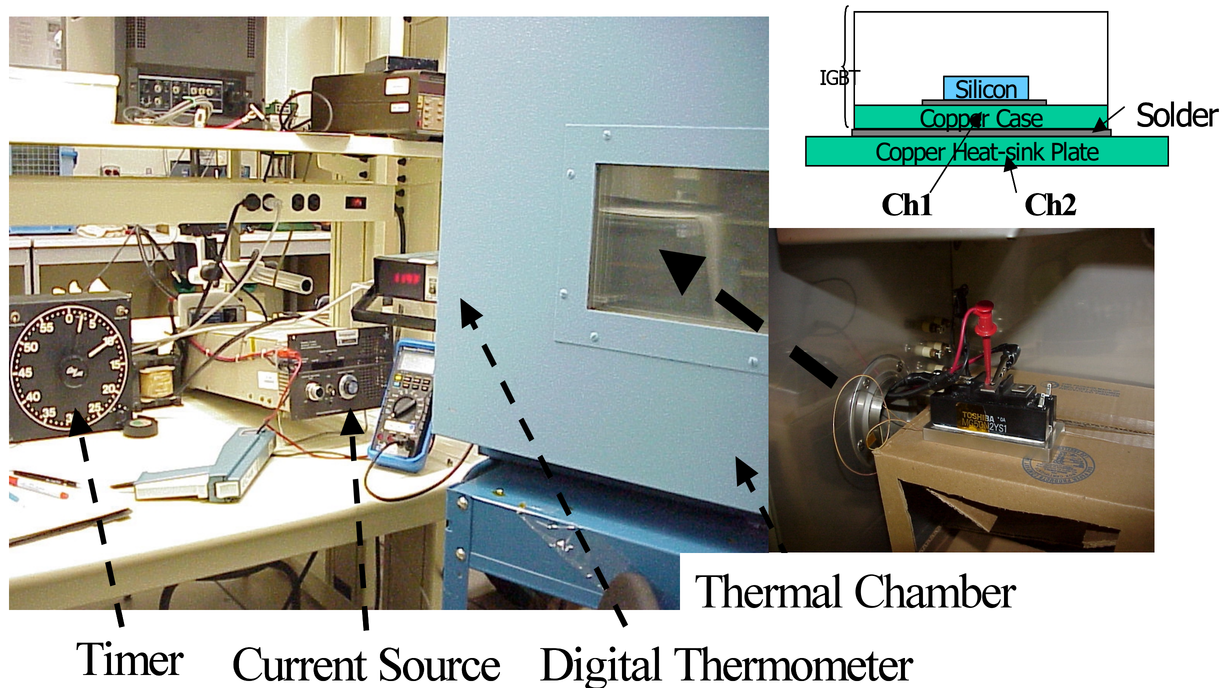


Figure 4.4. The test unit.

Table 4.1. The results of the thermal coupling test for Case 1, at ambient temperature, -1°C (30°F).

CASE 1	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
	0	-1.111111111	-1.111111111		0	
	15	1.111111111	1.111111111	1.358	0	0
	30	3.333333333	3.333333333	1.35	0	0
	45	5	5	1.343	0	0
	60	6.666666667	6.666666667	1.336	0	0
	75	8.333333333	8.333333333	1.33	0	0
	90	10.55555556	10	1.323	0.555555556	0.019912
	105	12.22222222	11.66666667	1.317	0.555555556	0.020013
	120	13.88888889	13.33333333	1.311	0.555555556	0.0201
	135	15	14.44444444	1.305	0.555555556	0.020187
	150	16.11111111	15	1.3	1.111111111	0.040552
	165	17.77777778	16.66666667	1.294	1.111111111	0.04076
	180	20	18.88888889	1.289	1.111111111	0.04094
	195	22.22222222	21.11111111	1.283	1.111111111	0.041152
	210	23.33333333	22.22222222	1.279	1.111111111	0.041367
	225	24.44444444	23.33333333	1.274	1.111111111	0.041583
	240	26.66666667	25.55555556	1.269	1.111111111	0.041803

Table 4.2. The results of the thermal coupling test for Case 2 (E1 C1), at ambient temperature, -1°C (30°F).

CASE 2 (E1 C1)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E1 and C1 are connected	0	-1.111111111	-1.111111111		0	
Case 2 at Thesis	15	1.111111111	1.111111111	1.432	0	0
	30	3.333333333	3.333333333	1.424	0	0
	45	5	5	1.416	0	0
	60	6.666666667	6.666666667	1.409	0	0
	75	8.333333333	8.333333333	1.402	0	0
	90	10	10	1.395	0	0
	105	11.11111111	11.11111111	1.388	0	0
	120	12.77777778	12.77777778	1.382	0	0
	135	13.88888889	13.88888889	1.376	0	0
	150	15.55555556	15.55555556	1.37	0	0
	165	17.22222222	16.66666667	1.363	0.555555556	0.021467
	180	18.33333333	17.77777778	1.357	0.555555556	0.02155
	195	19.44444444	18.88888889	1.35	0.555555556	0.021651
	210	20.55555556	20	1.343	0.555555556	0.021718
	225	21.66666667	21.11111111	1.336	0.555555556	0.021804
	240	22.77777778	22.22222222	1.329	0.555555556	0.02189

Table 4.3. The results of the thermal coupling test for Case 2 (E2 C2), at ambient temperature, -1°C (30°F).

CASE 2 (E2 C2)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E2 and C2 are connected	0	-1.111111111	-1.111111111		0	
Case 2 at Thesis	15	1.111111111	1.111111111	1.344	0	0
	30	3.333333333	3.333333333	1.337	0	0
	45	5	4.444444444	1.33	0.555555556	0.020886
	60	6.666666667	6.111111111	1.324	0.555555556	0.02098
	75	8.888888889	8.333333333	1.318	0.555555556	0.021076
	90	9.444444444	8.888888889	1.313	0.555555556	0.021156
	105	11.11111111	10.55555556	1.307	0.555555556	0.021253
	120	13.33333333	12.77777778	1.301	0.555555556	0.021351
	135	13.88888889	13.33333333	1.296	0.555555556	0.021433
	150	15.55555556	14.44444444	1.29	1.111111111	0.043066
	165	16.66666667	15.55555556	1.286	1.111111111	0.0432
	180	17.77777778	16.66666667	1.281	1.111111111	0.043369
	195	18.88888889	17.77777778	1.277	1.111111111	0.043505
	210	20.55555556	19.44444444	1.272	1.111111111	0.043676
	225	21.66666667	20	1.267	1.666666667	0.065772
	240	22.22222222	20.55555556	1.263	1.666666667	0.06598

Table 4.4. The results of the thermal coupling test for Case 3, at ambient temperature, -1°C (30°F).

CASE 3	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
The Smallest Voided Area	0	-1.111111111	-1.111111111		0	
	15	1.666666667	1.666666667	1.521	0	0
	30	3.888888889	3.888888889	1.519	0	0
	45	6.111111111	6.111111111	1.517	0	0
	60	7.777777778	7.777777778	1.515	0	0
	75	9.444444444	9.444444444	1.513	0	0
	90	11.11111111	11.11111111	1.511	0	0
	105	12.77777778	12.77777778	1.509	0	0
	120	14.44444444	14.44444444	1.507	0	0
	135	16.11111111	16.11111111	1.505	0	0
	150	17.77777778	17.77777778	1.503	0	0
	165	19.44444444	19.44444444	1.501	0	0
	180	20.55555556	20	1.499	0.555555556	0.018531
	195	22.22222222	21.66666667	1.497	0.555555556	0.018556
	210	23.88888889	23.33333333	1.495	0.555555556	0.01858
	225	25.55555556	25	1.493	0.555555556	0.018605
	240	26.66666667	26.11111111	1.491	0.555555556	0.01863

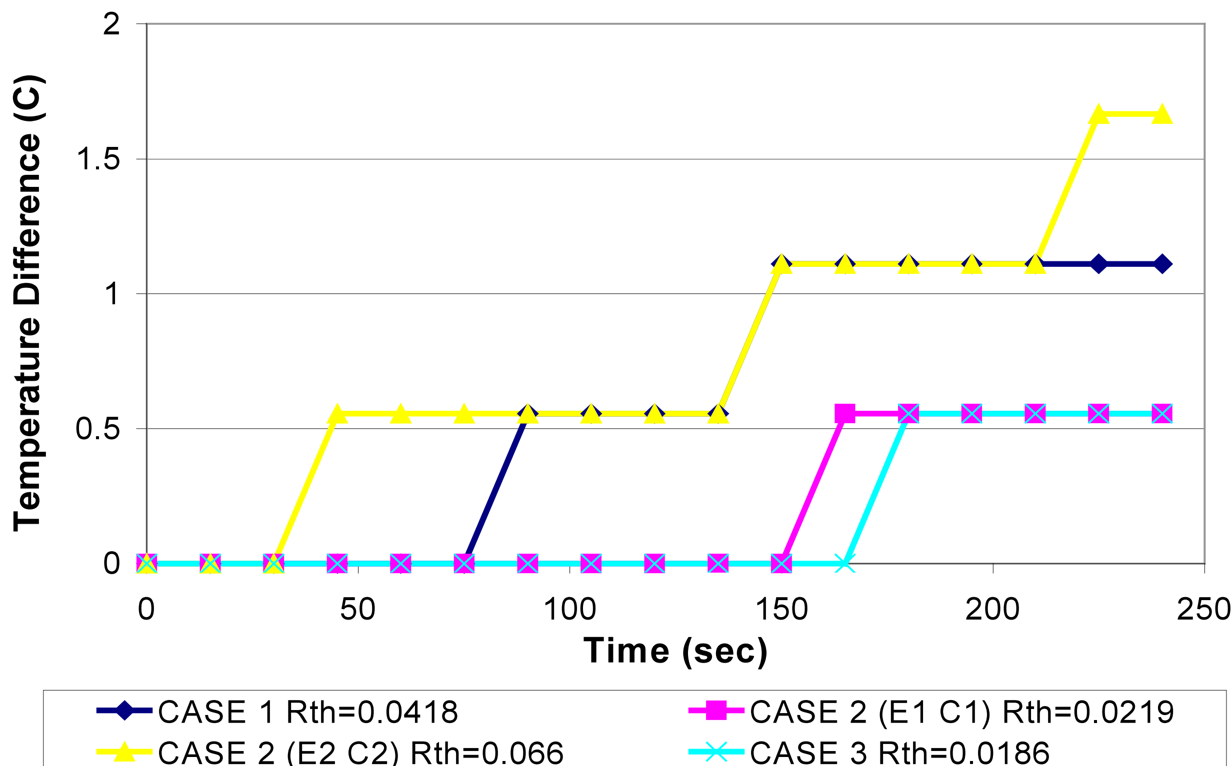


Figure 4.5. The comparison of the thermal resistances at -1°C (30°F).

Table 4.5. The results of the thermal coupling test for Case 1, at ambient temperature 49°C (120°F).

CASE 1	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
	0	48.88888889	48.88888889		0	
	15	50.55555556	50.55555556	1.271	0	0
	30	52.22222222	52.22222222	1.266	0	0
	45	53.88888889	53.88888889	1.262	0	0
	60	55.55555556	55.55555556	1.259	0	0
	75	56.66666667	56.66666667	1.254	0	0
	90	57.77777778	57.22222222	1.251	0.555555556	0.022204
	105	59.44444444	58.88888889	1.247	0.555555556	0.022276
	120	60.55555556	60	1.244	0.555555556	0.022329
	135	61.66666667	61.11111111	1.24	0.555555556	0.022401
	150	63.33333333	62.22222222	1.237	1.111111111	0.044912
	165	64.44444444	63.33333333	1.234	1.111111111	0.045021
	180	65.55555556	64.44444444	1.231	1.111111111	0.04513
	195	66.66666667	65.55555556	1.228	1.111111111	0.045241
	210	67.77777778	66.66666667	1.225	1.111111111	0.045351
	225	68.33333333	67.22222222	1.223	1.111111111	0.045426
	240	69.44444444	68.33333333	1.222	1.111111111	0.045463

Table 4.6. The results of the thermal coupling test for Case 2 (C1 E1), at ambient temperature 49°C (120°F).

CASE 2 (E1 C1)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E1 and C1 are connected	0	48.88888889	48.88888889		0	
	15	50.55555556	50.55555556	1.344	0	0
	30	52.22222222	52.22222222	1.337	0	0
	45	53.88888889	53.88888889	1.33	0	0
	60	55	55	1.324	0	0
	75	56.66666667	56.66666667	1.318	0	0
	90	58.33333333	58.33333333	1.313	0	0
	105	59.44444444	59.44444444	1.307	0	0
	120	60.55555556	60.55555556	1.301	0	0
	135	61.66666667	61.66666667	1.296	0	0
	150	62.77777778	62.22222222	1.29	0.555555556	0.021533
	165	63.88888889	63.33333333	1.286	0.555555556	0.0216
	180	65	64.44444444	1.281	0.555555556	0.021684
	195	66.11111111	65.55555556	1.277	0.555555556	0.021752
	210	67.22222222	66.66666667	1.272	0.555555556	0.021838
	225	67.77777778	67.22222222	1.267	0.555555556	0.021924
	240	68.88888889	68.33333333	1.263	0.555555556	0.021993

Table 4.7. The results of the thermal coupling test for Case 2 (C2 E2), at ambient temperature 49°C (120°F).

CASE 2 (E2 C2)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E2 and C2 are connected	0	48.88888889	48.88888889		0	
	15	50.55555556	50.55555556	1.244	0	0
	30	51.66666667	51.66666667	1.239	0	0
	45	53.33333333	52.77777778	1.235	0.555555556	0.022492
	60	54.44444444	53.88888889	1.232	0.555555556	0.022547
	75	55.55555556	55	1.228	0.555555556	0.02262
	90	56.66666667	56.11111111	1.225	0.555555556	0.022676
	105	57.77777778	57.22222222	1.222	0.555555556	0.022731
	120	58.88888889	58.33333333	1.219	0.555555556	0.022787
	135	60	59.44444444	1.216	0.555555556	0.022844
	150	61.11111111	60	1.213	1.111111111	0.0458
	165	62.22222222	61.11111111	1.209	1.111111111	0.045952
	180	63.33333333	62.22222222	1.207	1.111111111	0.046028
	195	64.44444444	63.33333333	1.204	1.111111111	0.046142
	210	65	63.88888889	1.202	1.111111111	0.046219
	225	66.11111111	64.44444444	1.199	1.666666667	0.069502
	240	67.22222222	65.55555556	1.197	1.666666667	0.069618

Table 4.8. The results of the thermal coupling test for Case 3, at ambient temperature 49°C (120°F).

CASE 3	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
The Smallest Voided Area	0	48.88888889	48.88888889		0	
	15	51.11111111	51.11111111	1.454	0	0
	30	53.33333333	53.33333333	1.45	0	0
	45	55	55	1.447	0	0
	60	56.66666667	56.66666667	1.444	0	0
	75	58.88888889	58.88888889	1.441	0	0
	90	60.55555556	60.55555556	1.438	0	0
	105	62.22222222	62.22222222	1.435	0	0
	120	63.33333333	63.33333333	1.432	0	0
	135	65	65	1.429	0	0
	150	66.66666667	66.66666667	1.427	0	0
	165	67.77777778	67.22222222	1.425	0.555555556	0.019493
	180	69.44444444	68.88888889	1.422	0.555555556	0.019534
	195	70.55555556	70	1.42	0.555555556	0.019562
	210	72.22222222	71.66666667	1.418	0.555555556	0.019589
	225	73.33333333	72.77777778	1.416	0.555555556	0.019617
	240	74.44444444	73.88888889	1.414	0.555555556	0.019645

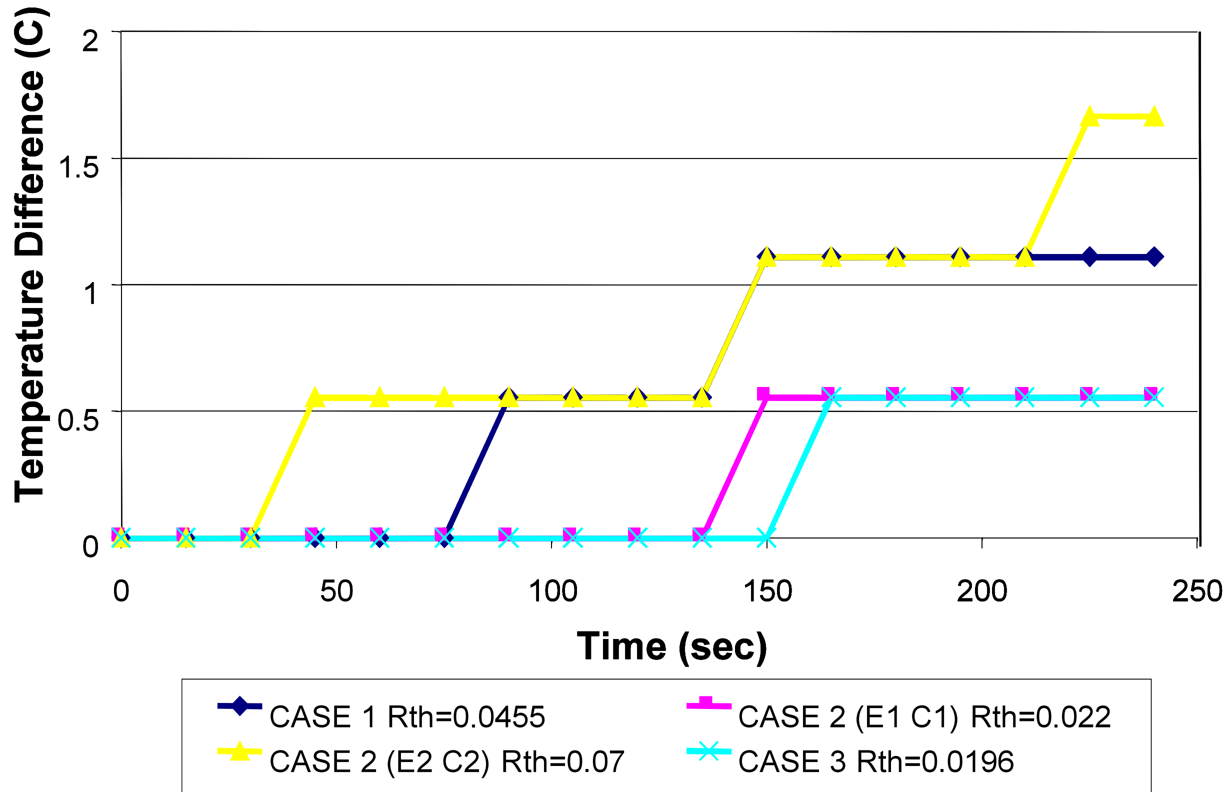


Figure 4.6. The comparison of the thermal resistances at 49°C (120°F).

Table 4.9. The results of the thermal conductivity test for Case 1, at ambient temperature 74°C (165°F).

CASE 1	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	Rth C
	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.242	0	0
	30	77.22222222	77.22222222	1.238	0	0
	45	78.88888889	78.88888889	1.235	0	0
	60	80	80	1.231	0	0
	75	81.66666667	81.11111111	1.228	0.555555556	0.02262
	90	82.77777778	82.22222222	1.225	0.555555556	0.022676
	105	84.44444444	83.88888889	1.222	0.555555556	0.022731
	120	85	84.44444444	1.218	0.555555556	0.022806
	135	86.11111111	85.55555556	1.216	0.555555556	0.022844
	150	87.22222222	86.66666667	1.212	0.555555556	0.022919
	165	88.33333333	87.22222222	1.207	1.111111111	0.046028
	180	89.44444444	88.33333333	1.205	1.111111111	0.046104
	195	90.55555556	89.44444444	1.203	1.111111111	0.046181
	210	91.66666667	90.55555556	1.201	1.111111111	0.046258
	225	92.77777778	91.66666667	1.199	1.111111111	0.046335
	240	93.33333333	92.22222222	1.198	1.111111111	0.046374

Table 4.10. The results of the thermal conductivity test for Case 2 (E1 C1), at ambient temperature 74°C (165°F).

CASE 2 (E1 C1)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E1 and C1 are connected	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.249	0	0
	30	77.22222222	77.22222222	1.245	0	0
	45	78.33333333	78.33333333	1.242	0	0
	60	79.44444444	79.44444444	1.239	0	0
	75	80.55555556	80.55555556	1.237	0	0
	90	82.22222222	82.22222222	1.235	0	0
	105	83.33333333	83.33333333	1.232	0	0
	120	84.44444444	84.44444444	1.229	0	0
	135	85.55555556	85	1.226	0.555555556	0.022657
	150	86.11111111	85.55555556	1.224	0.555555556	0.022694
	165	87.22222222	86.66666667	1.221	0.555555556	0.02275
	180	88.33333333	87.77777778	1.219	0.555555556	0.022787
	195	89.44444444	88.88888889	1.217	0.555555556	0.022825
	210	90	89.44444444	1.215	0.555555556	0.022862
	225	91.11111111	90.55555556	1.213	0.555555556	0.0229
	240	92.22222222	91.66666667	1.211	0.555555556	0.022938

Table 4.11. The results of the thermal conductivity test for Case 2 (E2 C2), at ambient temperature 74°C (165°F).

CASE 2 (E2 C2)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
E2 and C2 are connected	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.204	0	0
	30	77.22222222	77.22222222	1.2	0	0
	45	78.88888889	78.33333333	1.197	0.555555556	0.023206
	60	80	79.44444444	1.194	0.555555556	0.023264
	75	81.11111111	80.55555556	1.191	0.555555556	0.023323
	90	82.22222222	81.66666667	1.188	0.555555556	0.023382
	105	83.88888889	83.33333333	1.185	0.555555556	0.023441
	120	85	83.88888889	1.183	1.111111111	0.046962
	135	86.11111111	85	1.181	1.111111111	0.047041
	150	87.22222222	86.11111111	1.179	1.111111111	0.047121
	165	88.33333333	87.22222222	1.177	1.111111111	0.047201
	180	88.88888889	87.77777778	1.175	1.111111111	0.047281
	195	90.55555556	89.44444444	1.173	1.111111111	0.047362
	210	91.11111111	89.44444444	1.171	1.666666667	0.071164
	225	92.22222222	90.55555556	1.169	1.666666667	0.071286
	240	93.33333333	91.66666667	1.167	1.666666667	0.071408

Table 4.12. The results of the thermal conductivity test for Case 3, at ambient temperature 74°C (165°F).

CASE 3	Time(sec)	Ch1 Temp.(C	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	Rth C
The Smalleat Voided Area	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.418	0	0
	30	77.77777778	77.77777778	1.414	0	0
	45	79.44444444	79.44444444	1.41	0	0
	60	81.11111111	81.11111111	1.406	0	0
	75	82.77777778	82.77777778	1.403	0	0
	90	84.44444444	84.44444444	1.399	0	0
	105	86.11111111	86.11111111	1.396	0	0
	120	87.22222222	87.22222222	1.393	0	0
	135	88.88888889	88.33333333	1.39	0.555555556	0.019984
	150	90	89.44444444	1.387	0.555555556	0.020027
	165	91.66666667	91.11111111	1.384	0.555555556	0.020071
	180	92.77777778	92.22222222	1.381	0.555555556	0.020114
	195	94.44444444	93.88888889	1.379	0.555555556	0.020143
	210	95.55555556	95	1.376	0.555555556	0.020187
	225	96.66666667	96.11111111	1.373	0.555555556	0.020231
	240	97.77777778	97.22222222	1.371	0.555555556	0.020261

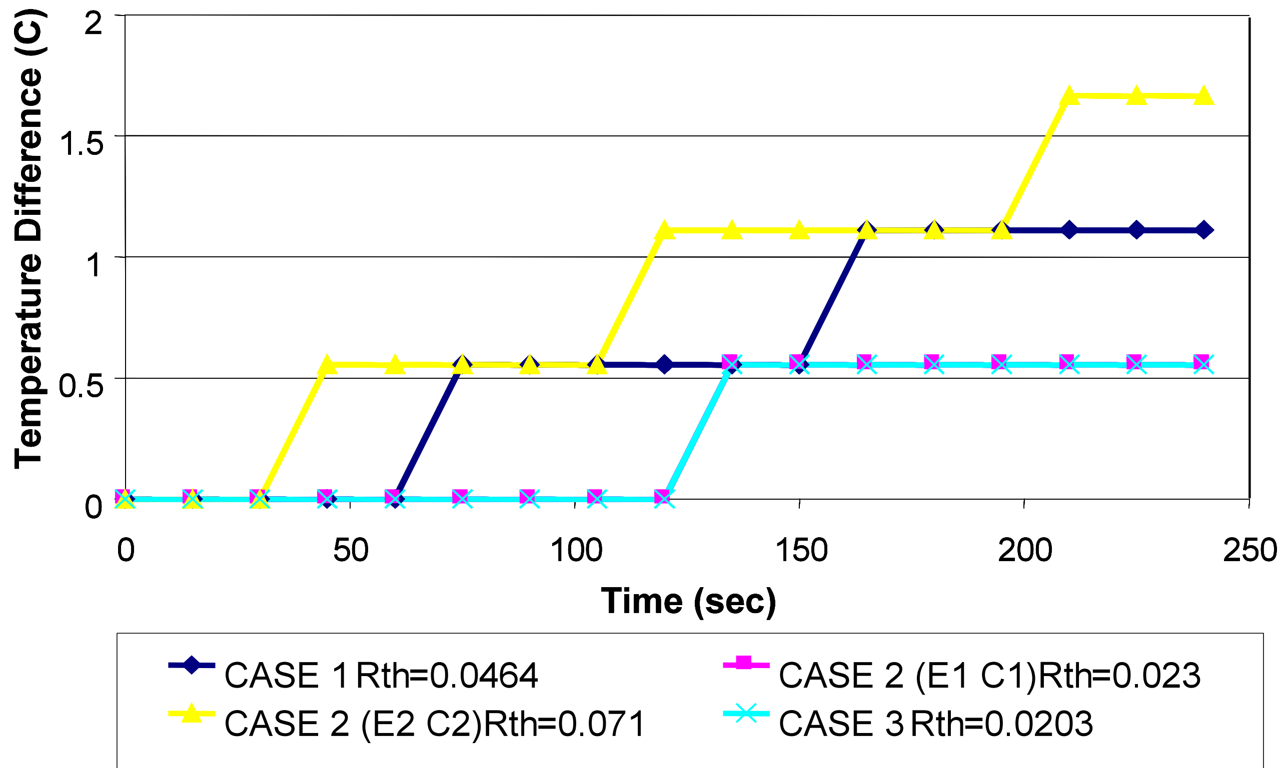


Figure 4.7. The comparison of the thermal resistances at 74°C (165°F).

4.3. Measurement and Comparison of Thermal Resistances in Cases Involving the Worst Soldering, Thermstrate and Thermal Grease (silicon compounds)

Using the test unit shown in Figure 4.4, the thermal resistances in cases involving the worst soldering, thermstrate and thermal grease (silicon compounds) are now measured.

If the worst soldering case occurs due to different human factors, environment, and materials, the thermal resistance is changed, as illustrated by the acoustic image in Figure 4.8 (b), which contains many voids.

The use of pressure to mount the IGBT, such as in methods involving thermal grease and thermstrate, has been popular because it is easy to use and in expensive. Even now, thermal grease is widely used due to its low cost; however the thermal conductivity of thermal grease worsens dramatically within increases environmental temperature. Table 4.13 shows the thermal conductivities of lead, thermstrate (aluminum) and thermal grease (silicon compounds).

Table 4.13. Thermal conductivities of selected metallic solids.

Composition	Properties at Various Temperature (K) Thermal Conductivity, k (W/ m*K)			
	100 K	200 K	300 K	350K
Aluminum	302	257	237	234
Lead	39.7	36.7	35.3	34.6
Silicon	884	264	148	108

As previously mentioned, R_{c-s} is a function of many factors, such as flatness and surface preparation of both the IGBT and the heat sink, type of insulation pad and / or thermally conductive compound, mount-down pressure, and the area of the heat-flow path. The best-conducting contact is metal-to-metal, but there are always air voids in the joint area. Depending upon the thermal and electrical requirements of the system, thermal grease or some non- insulating grease-replacement material, (such as thermstrate) is used to eliminate voids between the IGBT and the heat sink.

Thermal grease (silicon compound) is effective in reducing R_{c-s} when the maximum air gap between surfaces is less than 1mil and the environmental temperatures are low. This means that the flatness of the surfaces is very important in determining whether or not to use thermal grease. There are many objections to the use of thermal grease, including their messiness, and the possibility of out-gassing and drying out with time. Recently, thermstrates are used by many package engineers because of their very low cost and good thermal conductivity at high environment temperature. Thermstrate withstands modest heat and pressure and achieves relatively low resistance [23].

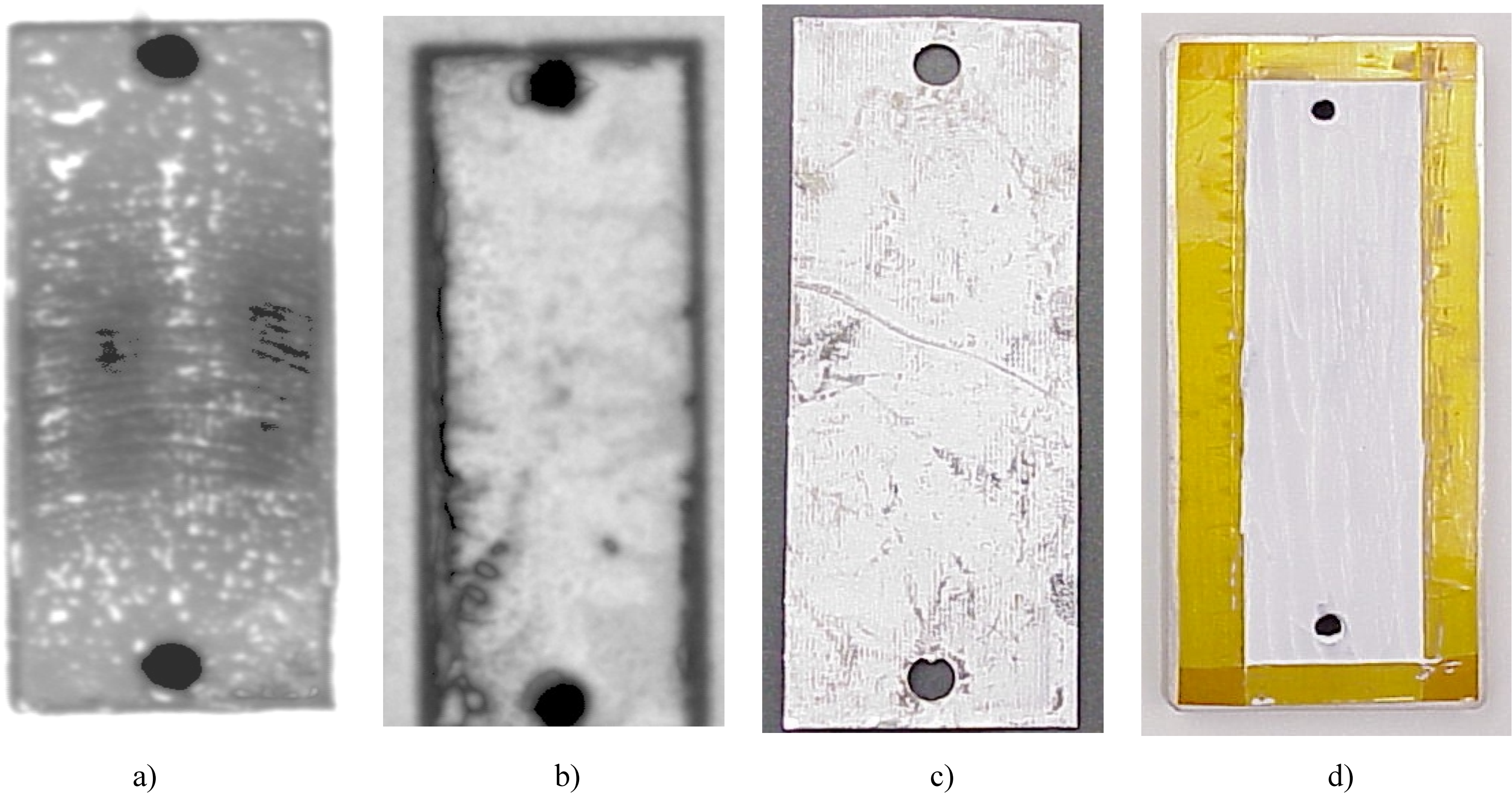


Figure 4.8. Acoustic images showing: Case a) the smallest voided case, Case b) the worst soldering case, Case c) case using thermstrate, and Case d) case using thermal grease.

Table 4.14. The result of the thermal coupling test for Case a), at ambient temperature -1°C (30°F).

CASE 3	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	Rth C
The Smallest Voided Area	0	-1.111111111	-1.111111111		0	
	15	1.666666667	1.666666667	1.521	0	0
	30	3.888888889	3.888888889	1.519	0	0
	45	6.111111111	6.111111111	1.517	0	0
	60	7.777777778	7.777777778	1.515	0	0
	75	9.444444444	9.444444444	1.513	0	0
	90	11.11111111	11.11111111	1.511	0	0
	105	12.77777778	12.77777778	1.509	0	0
	120	14.44444444	14.44444444	1.507	0	0
	135	16.11111111	16.11111111	1.505	0	0
	150	17.77777778	17.77777778	1.503	0	0
	165	19.44444444	19.44444444	1.501	0	0
	180	20.55555556	20	1.499	0.555555556	0.018531
	195	22.22222222	21.66666667	1.497	0.555555556	0.018556
	210	23.88888889	23.33333333	1.495	0.555555556	0.01858
	225	25.55555556	25	1.493	0.555555556	0.018605
	240	26.66666667	26.11111111	1.491	0.555555556	0.01863

Table 4.15. The result of the thermal coupling test for Case b), at ambient temperature -1°C (30°F).

CASE b)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
It is the worst case of voids formation.	0	-1.111111111	-1.111111111		0	
	15	1.666666667	0.555555556	1.352	1.111111111	0.041091
	30	3.888888889	2.222222222	1.348	1.666666667	0.06182
	45	5.555555556	3.888888889	1.344	1.666666667	0.062004
	60	7.222222222	5.555555556	1.341	1.666666667	0.062143
	75	8.888888889	7.222222222	1.338	1.666666667	0.062282
	90	10	8.333333333	1.335	1.666666667	0.062422
	105	11.66666667	10	1.332	1.666666667	0.062563
	120	13.33333333	11.66666667	1.329	1.666666667	0.062704
	135	14.44444444	12.77777778	1.326	1.666666667	0.062846
	150	16.11111111	14.44444444	1.323	1.666666667	0.062988
	165	17.77777778	15.55555556	1.32	2.222222222	0.084175
	180	18.88888889	16.66666667	1.317	2.222222222	0.084367
	195	20	17.77777778	1.314	2.222222222	0.084559
	210	21.11111111	18.88888889	1.312	2.222222222	0.084688
	225	22.77777778	20.55555556	1.309	2.222222222	0.084882
	240	23.33333333	21.11111111	1.307	2.222222222	0.085012

Table 4.16. The result of the thermal coupling test for Case c), at ambient temperature -1°C (30°F).

CASE c)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
A thermstrate is used as interfacial materia	0	-1.111111111	-1.111111111		0	
	15	1.111111111	1.111111111	1.437	0	0
	30	3.333333333	2.777777778	1.436	0.555555556	0.019344
	45	5	4.444444444	1.435	0.555555556	0.019357
	60	7.222222222	6.666666667	1.434	0.555555556	0.019371
	75	8.888888889	8.333333333	1.433	0.555555556	0.019384
	90	10.55555556	10	1.432	0.555555556	0.019398
	105	12.22222222	11.11111111	1.43	1.111111111	0.03885
	120	13.88888889	12.77777778	1.429	1.111111111	0.038877
	135	15.55555556	14.44444444	1.428	1.111111111	0.038904
	150	16.66666667	15.55555556	1.427	1.111111111	0.038932
	165	18.33333333	17.22222222	1.426	1.111111111	0.038959
	180	20	18.33333333	1.425	1.666666667	0.05848
	195	21.11111111	19.44444444	1.423	1.666666667	0.058562
	210	22.22222222	20.55555556	1.422	1.666666667	0.058603
	225	23.88888889	22.22222222	1.421	1.666666667	0.058644
	240	25	23.33333333	1.42	1.666666667	0.058685

Table 4.17. The result of the thermal coupling test for Case d), at ambient temperature -1°C (30°F).

CASE d)	Time(sec)	Ch1 Temp.(C)	Ch1 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
0.4g Silicone Heat Sink Compound	0	-1.111111111	-1.111111111		0	
	15	1.111111111	1.111111111	1.432	0	0
	30	3.333333333	3.333333333	1.43	0	0
	45	5.555555556	5	1.429	0.555555556	0.019439
	60	7.222222222	6.666666667	1.428	0.555555556	0.019452
	75	8.888888889	8.333333333	1.427	0.555555556	0.019466
	90	10.55555556	10	1.425	0.555555556	0.019493
	105	12.22222222	11.11111111	1.424	1.111111111	0.039014
	120	14.44444444	13.33333333	1.423	1.111111111	0.039041
	135	16.11111111	15	1.421	1.111111111	0.039096
	150	17.22222222	16.11111111	1.42	1.111111111	0.039124
	165	18.88888889	17.77777778	1.419	1.111111111	0.039151
	180	20.55555556	18.88888889	1.418	1.666666667	0.058768
	195	21.66666667	20	1.416	1.666666667	0.058851
	210	23.33333333	21.66666667	1.415	1.666666667	0.058893
	225	24.44444444	22.77777778	1.414	1.666666667	0.058934
	240	25.55555556	23.88888889	1.413	1.666666667	0.058976

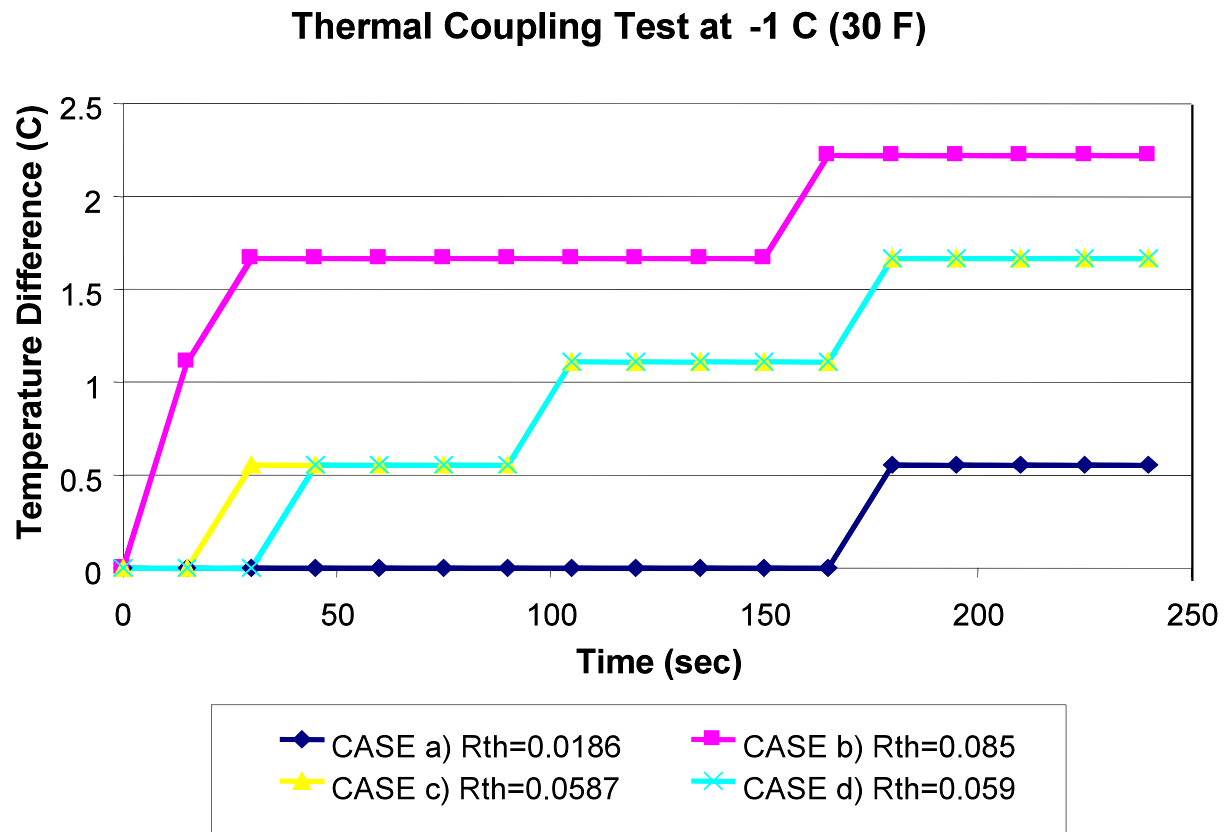


Figure 4.9. The comparison of the thermal resistances at -1°C (30°F).

Table 4.18. The result of the thermal coupling test for Case a) at ambient temperature 49°C (120°F).

CASE a)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
It has almost no voids in the solder joint.	0	48.88888889	48.88888889		0	
	15	51.11111111	51.11111111	1.454	0	0
	30	53.33333333	53.33333333	1.45	0	0
	45	55	55	1.447	0	0
	60	56.66666667	56.66666667	1.444	0	0
	75	58.88888889	58.88888889	1.441	0	0
	90	60.55555556	60.55555556	1.438	0	0
	105	62.22222222	62.22222222	1.435	0	0
	120	63.33333333	63.33333333	1.432	0	0
	135	65	65	1.429	0	0
	150	66.66666667	66.66666667	1.427	0	0
	165	67.77777778	67.22222222	1.425	0.555555556	0.019493
	180	69.44444444	68.88888889	1.422	0.555555556	0.019534
	195	70.55555556	70	1.42	0.555555556	0.019562
	210	72.22222222	71.66666667	1.418	0.555555556	0.019589
	225	73.33333333	72.77777778	1.416	0.555555556	0.019617
	240	74.44444444	73.88888889	1.414	0.555555556	0.019645

Table 4.19. The result of the thermal coupling test for Case b) at ambient temperature 49°C (120°F).

CASE b)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
It is the worst case of voids formation.	0	48.88888889	48.88888889		0	
	15	51.11111111	50.55555556	1.244	0.555555556	0.022329
	30	52.77777778	51.66666667	1.239	1.111111111	0.044839
	45	54.44444444	53.33333333	1.235	1.111111111	0.044984
	60	56.66666667	55.55555556	1.232	1.111111111	0.045094
	75	57.77777778	56.11111111	1.228	1.666666667	0.067861
	90	58.88888889	57.22222222	1.225	1.666666667	0.068027
	105	60.55555556	58.88888889	1.222	1.666666667	0.068194
	120	61.66666667	60	1.219	1.666666667	0.068362
	135	62.77777778	61.11111111	1.216	1.666666667	0.068531
	150	63.88888889	62.22222222	1.213	1.666666667	0.0687
	165	65.55555556	63.33333333	1.209	2.222222222	0.091903
	180	66.66666667	64.44444444	1.207	2.222222222	0.092056
	195	67.77777778	65.55555556	1.204	2.222222222	0.092285
	210	68.88888889	66.66666667	1.202	2.222222222	0.092439
	225	70	67.77777778	1.199	2.222222222	0.09267
	240	70.55555556	68.33333333	1.197	2.222222222	0.092825

Table 4.20. The result of the thermal coupling test for Case c) at ambient temperature 49°C (120°F).

CASE c)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
thermstrate is used as interfacial material.	0	48.88888889	48.88888889		0	
	15	50.55555556	50.55555556	1.396	0	0
	30	52.77777778	52.22222222	1.393	0.555555556	0.019941
	45	55	54.44444444	1.39	0.555555556	0.019984
	60	56.66666667	56.11111111	1.388	0.555555556	0.020013
	75	58.33333333	57.77777778	1.385	0.555555556	0.020056
	90	60	59.44444444	1.382	0.555555556	0.0201
	105	61.66666667	60.55555556	1.38	1.111111111	0.040258
	120	63.33333333	62.22222222	1.377	1.111111111	0.040345
	135	65	63.88888889	1.375	1.111111111	0.040404
	150	66.66666667	65.55555556	1.372	1.111111111	0.040492
	165	67.77777778	66.66666667	1.37	1.111111111	0.040552
	180	69.44444444	67.77777778	1.368	1.666666667	0.060916
	195	70.55555556	68.88888889	1.366	1.666666667	0.061005
	210	72.22222222	70.55555556	1.364	1.666666667	0.061095
	225	73.33333333	71.66666667	1.362	1.666666667	0.061185
	240	74.44444444	72.77777778	1.36	1.666666667	0.061275

Table 4.21. The result of the thermal coupling test for Case d) at ambient temperature 49°C (120°F).

CASE d)	Time(sec)	Ch1 Temp.(C)	Ch1 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
0.4g Silicone Heat Sink Compound	0	48.88888889	48.88888889		0	
	15	51.11111111	51.11111111	1.383	0	0
	30	53.33333333	52.77777778	1.38	0.555555556	0.020129
	45	55	54.44444444	1.377	0.555555556	0.020173
	60	57.22222222	56.66666667	1.374	0.555555556	0.020217
	75	58.88888889	58.33333333	1.372	0.555555556	0.020246
	90	60.55555556	59.44444444	1.369	1.111111111	0.040581
	105	61.66666667	60.55555556	1.366	1.111111111	0.04067
	120	63.33333333	62.22222222	1.364	1.111111111	0.04073
	135	65	63.88888889	1.362	1.111111111	0.04079
	150	66.66666667	65.55555556	1.359	1.111111111	0.04088
	165	68.33333333	66.66666667	1.357	1.666666667	0.06141
	180	69.44444444	67.77777778	1.355	1.666666667	0.061501
	195	71.11111111	69.44444444	1.352	1.666666667	0.061637
	210	72.22222222	70.55555556	1.35	1.666666667	0.061728
	225	73.33333333	71.66666667	1.348	1.666666667	0.06182
	240	74.44444444	72.77777778	1.346	1.666666667	0.061912

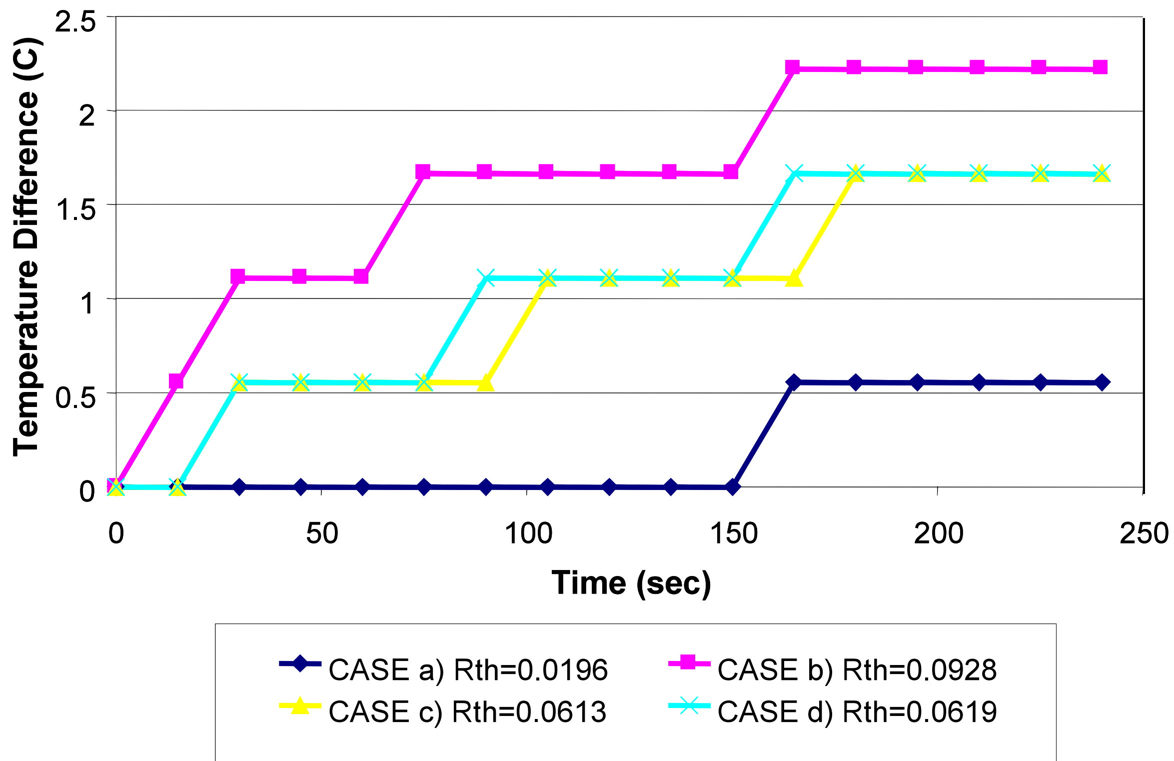


Figure 4.10. The comparison of the thermal resistances at 49°C (120°F).

Table 4.22. The result of the thermal coupling test for Case a), at ambient temperature 74°C (165°F).

CASE a)	Time(sec)	Ch1 Temp.(C	Ch2 Temp.(C	Diode Froward Voltage Drop (V	C=D-F (Temp. difference C	**Rth C**
It has almost no voids in the solder join	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.418	0	0
	30	77.77777778	77.77777778	1.414	0	0
	45	79.44444444	79.44444444	1.41	0	0
	60	81.11111111	81.11111111	1.406	0	0
	75	82.77777778	82.77777778	1.403	0	0
	90	84.44444444	84.44444444	1.399	0	0
	105	86.11111111	86.11111111	1.396	0	0
	120	87.22222222	87.22222222	1.393	0	0
	135	88.88888889	88.33333333	1.39	0.555555556	0.019984
	150	90	89.44444444	1.387	0.555555556	0.020027
	165	91.66666667	91.11111111	1.384	0.555555556	0.020071
	180	92.77777778	92.22222222	1.381	0.555555556	0.020114
	195	94.44444444	93.88888889	1.379	0.555555556	0.020143
	210	95.55555556	95	1.376	0.555555556	0.020187
	225	96.66666667	96.11111111	1.373	0.555555556	0.020231
	240	97.77777778	97.22222222	1.371	0.555555556	0.020261

Table 4.23. The result of the thermal coupling test for Case b), at ambient temperature 74°C (165°F).

CASE b)	Time(sec)	Ch1 Temp.(C	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	C=D-F (Temp. difference C)	**Rth C**
It is the worst case of voids formation.	0	73.88888889	73.88888889		0	
	15	76.11111111	75.55555556	1.186	0.555555556	0.023421
	30	77.77777778	77.22222222	1.182	0.555555556	0.023501
	45	79.44444444	78.33333333	1.178	1.111111111	0.047161
	60	80.55555556	79.44444444	1.173	1.111111111	0.047362
	75	81.66666667	80	1.171	1.666666667	0.071164
	90	83.33333333	81.66666667	1.168	1.666666667	0.071347
	105	84.44444444	82.77777778	1.164	1.666666667	0.071592
	120	85.55555556	83.88888889	1.161	1.666666667	0.071777
	135	86.66666667	85	1.157	1.666666667	0.072025
	150	87.77777778	85.55555556	1154	2.222222222	9.63E-05
	165	88.88888889	86.66666667	1.151	2.222222222	0.096534
	180	90	87.77777778	1.148	2.222222222	0.096787
	195	91.11111111	88.88888889	1.146	2.222222222	0.096956
	210	92.22222222	90	1.143	2.222222222	0.09721
	225	93.33333333	91.11111111	1.14	2.222222222	0.097466
	240	94.44444444	92.22222222	1.138	2.222222222	0.097637

Table 4.24. The result of the thermal coupling test for Case c), at ambient temperature 74°C (165°F).

CASE c)	Time(sec)	Ch1 Temp.(C)	Ch2 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
thermstrate is used as interfacial material.	0	73.88888889	73.88888889		0	
	15	75.55555556	75.55555556	1.357	0	0
	30	77.77777778	77.77777778	1.354	0	0
	45	79.44444444	78.88888889	1.35	0.555555556	0.020576
	60	81.66666667	81.11111111	1.348	0.555555556	0.020607
	75	82.77777778	82.22222222	1.345	0.555555556	0.020653
	90	84.44444444	83.33333333	1.342	1.111111111	0.041398
	105	86.11111111	85	1.339	1.111111111	0.04149
	120	87.22222222	86.11111111	1.337	1.111111111	0.041552
	135	88.88888889	87.77777778	1.335	1.111111111	0.041615
	150	90	88.88888889	1.332	1.111111111	0.041708
	165	91.66666667	90.55555556	1.33	1.111111111	0.041771
	180	92.77777778	91.11111111	1.328	1.666666667	0.062751
	195	94.44444444	92.77777778	1.325	1.666666667	0.062893
	210	95.55555556	93.88888889	1.322	1.666666667	0.063036
	225	96.66666667	95	1.32	1.666666667	0.063131
	240	97.77777778	96.11111111	1.318	1.666666667	0.063227

Table 4.25. The result of the thermal coupling test for Case d), at ambient temperature 74°C (165°F).

CASE d)	Time(sec)	Ch1 Temp.(C)	Ch1 Temp.(C)	Diode Froward Voltage Drop (V)	M=P-R (Temp. difference C)	**Rth C**
0.4g Silicone Heat Sink Compound	0	73.88888889	73.88888889		0	
	15	76.11111111	76.11111111	1.343	0	0
	30	77.77777778	77.22222222	1.34	0.555555556	0.02073
	45	80	79.44444444	1.336	0.555555556	0.020792
	60	81.66666667	80.55555556	1.334	1.111111111	0.041646
	75	83.33333333	82.22222222	1.331	1.111111111	0.04174
	90	84.44444444	83.33333333	1.328	1.111111111	0.041834
	105	86.11111111	84.44444444	1.325	1.666666667	0.062893
	120	87.77777778	86.11111111	1.322	1.666666667	0.063036
	135	88.88888889	87.22222222	1.32	1.666666667	0.063131
	150	90.55555556	88.88888889	1.317	1.666666667	0.063275
	165	91.66666667	90	1.315	1.666666667	0.063371
	180	93.33333333	91.11111111	1.312	2.222222222	0.084688
	195	94.44444444	92.22222222	1.31	2.222222222	0.084818
	210	96.11111111	93.88888889	1.308	2.222222222	0.084947
	225	97.22222222	95	1.306	2.222222222	0.085077
	240	98.33333333	96.11111111	1.303	2.222222222	0.085273

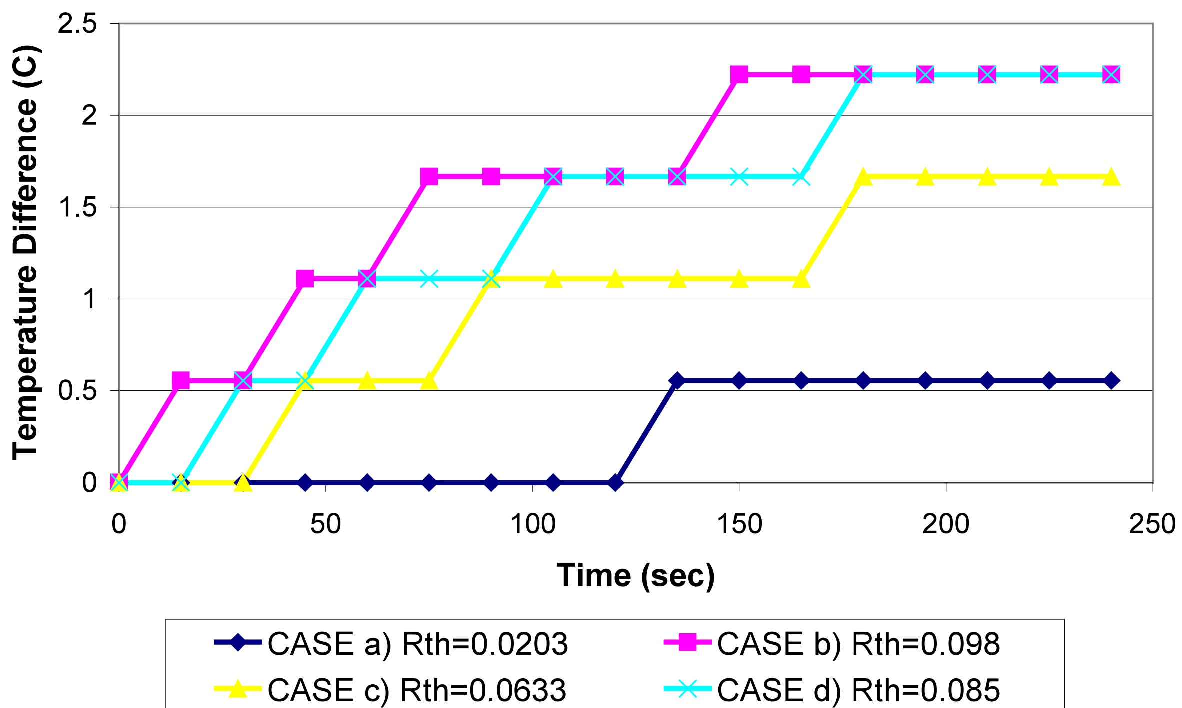


Figure 4.11. The comparison of the thermal resistances at 74°C (165°F).

4.4. Summary

In Chapter VI, the thermal resistances for Case 1, 2 and 3, described in Chapter III, are calculated by measuring Tc, Ts, and *Vf* for each case. The comparison of thermal resistances is presented by the graph in the figures.

Moreover, the thermal resistances for the smallest voided case, the worst soldering case, cases using thermstrate, and those using thermal grease are also obtained and presented. The thermal resistances of all cases are also compared by graphically.

To prove the linear characteristics of the cases, the tests are conducted in three environmental temperatures, -1 °C, 49 °C and 74 °C. The thermal resistances increase as the temperatures increase because of interface material properties, as shown in table 4.13.

Table 4.26 shows the increase of Rth vs. those of temperature.

Figure 4.12 shows the increase in thermal resistances caused by rising temperatures.

Table 4.26. Rth vs. temperature.

Temperature (°C)	Case 1	Case 2 (E1 C1)	Case 2 (E2 C2)	Case 3 Case a)	Case b)	Case c)	Case d)
-1	0.0418	0.0219	0.066	0.0186	0.085	0.0587	0.059
49	0.0455	0.22	0.07	0.0196	0.0928	0.0613	0.0619
74	0.0464	0.23	0.072	0.0203	0.098	0.0633	0.085

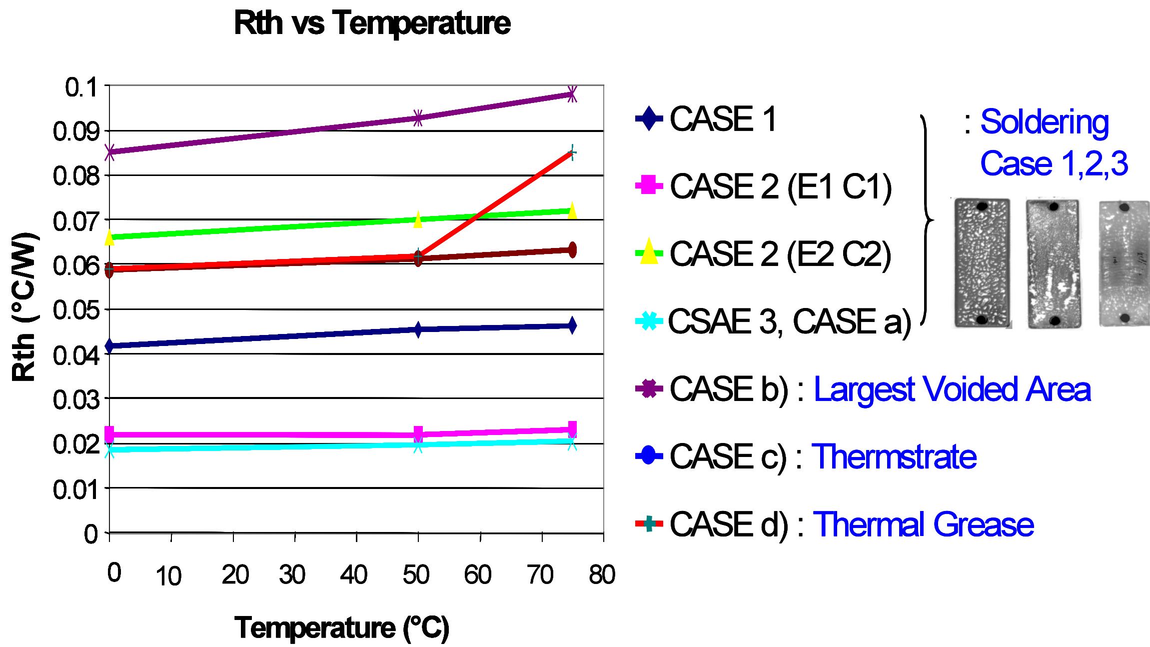


Figure 4.12. Increases in thermal resistances caused by rising temperatures.

As indicated in Figure 4.11, at 74°C, the thermal resistance of the thermal grease is dramatically increased due to the material property. The other cases show linear characteristics. The thermal resistance of case 3 is 4 times better than that of case d) at 74°C ambient temperature.

Chapter V. Thermal Modeling and Analysis

In this chapter, the thermal modeling and analysis for the cases in Chapter IV are introduced. After modeling the IGBT / heat sink module with the thermal interface, simulation will be conducted by *Flotherm*. The temperature profile in the module is shown by the *Flotherm* simulation. Results of the simulation in steady state are also discussed.

5.1. Introduction

As mentioned, the temperature increase is a factor that can lead to power failure in the modules. For this reason, reducing thermal resistances between each layer and selecting the optimal heat sink are quite important to thermal management of the system.

The goal of the thermal modeling and analysis in this chapter is to show the improvements in heat dissipation gained by using direct-soldering instead of conventional thermal grease, and to offer guidelines for heat sink design in systems for further applications.

The simulation tool is *Flotherm*, which can achieve more accurate thermal analysis and modeling. *Flotherm* is based on computational fluid dynamics (CFD), which calculate heat transfer coefficients by actual airflow conditions, and CFD-based finite volume analysis software. *Flotherm* is widely used in industry for modeling thermo-mechanical structures.

Using the smallest voided area R_{th} of the direct-soldering and thermal grease cases R_{th}, the thermal dissipations of each case are shown by experiment and simulation at 28W, 40W and 50W. After verifying that the experiment results and simulation results agree, the thermal distributions of the smallest voided area interface and the thermal grease interface at 100W power loss are simulated with a large heat sink.

5.2. Model of the IGBT/ Heat Sink Module

The IGBT's thermal energy is conducted first to the AlN (aluminum nitride) DBC (direct bond copper) substrate and the heat spreader, then through the interface material, and is finally dissipated to the environment. Therefore, the thermal characteristics between the IGBT and the heat sink need to be properly defined. In *Flotherm*, the project manager and drawing board can help to configure the geometry of the power module / heat sink. Ascertaining the detailed geometry is important for accurate *Flotherm* simulation. The visualization window inspects geometry and simulation results.

The project manager consists of the following: the top-level menu, which provides high-level access to all the functions available in the project manager window; the standard button bar, which provides quick access to a subset of the menu bar functions; the application-specific button bar, which provides quick access to functions specific to the project manager window; the title bar; and the statue bar.

The drawing board is a graphical application window for creating, moving and editing geometry. By default, the window can be maximized for ease of working on a model. The drawing board operates dynamically with the project manager and visualization application windows.

The visualization window provides for 2-D and 3-D views of the geometry and solution results. The geometry can be displayed as wire-frame, fully rendered or a combination of both. The visualization planes can be defined to display the solution results and plane selection [24].

Figure 5.1 shows the construction of the geometry.

Figure 5.2 shows the geometry of the IGBT / heat sink.

Figure 5.3 shows the geometry of the IGBT / heat sink when a large heat sink is used.

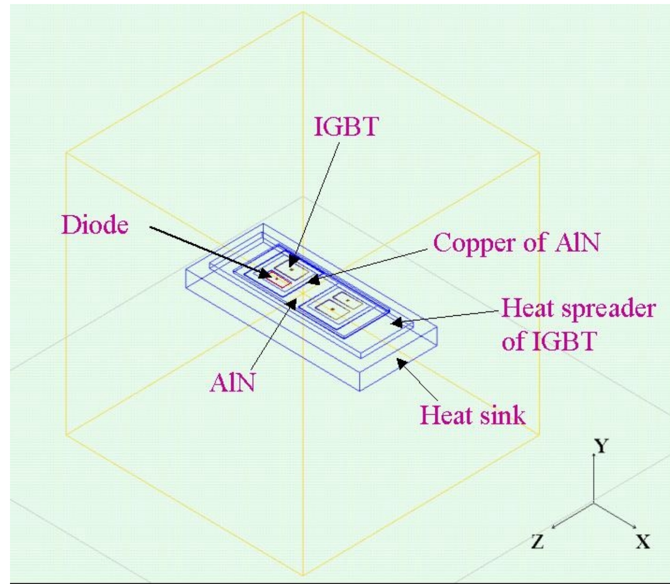


Figure 5.1. The construction of the geometry.

Table 5.1. The size of each layer.

	X (mm)	Y (mm)	Z (mm)
Heat Sink	110	10	49
Interface	96	0.3	33.3
IGBT Heat Spreader	96	3	33
Solder for Copper under AlN	70.53	0.127	29
Copper under AlN	70.53	0.254	29
AlN	70.53	1	29
Copper1 on AlN	24.4056	0.254	26.126
Copper2 on AlN	24.4056	0.254	26.126
Solder1 for Copper1 on AlN	20	0.127	20
Solder2 for Copper2 on AlN	20	0.127	20
Silicon under Source	13	0.254	5.969

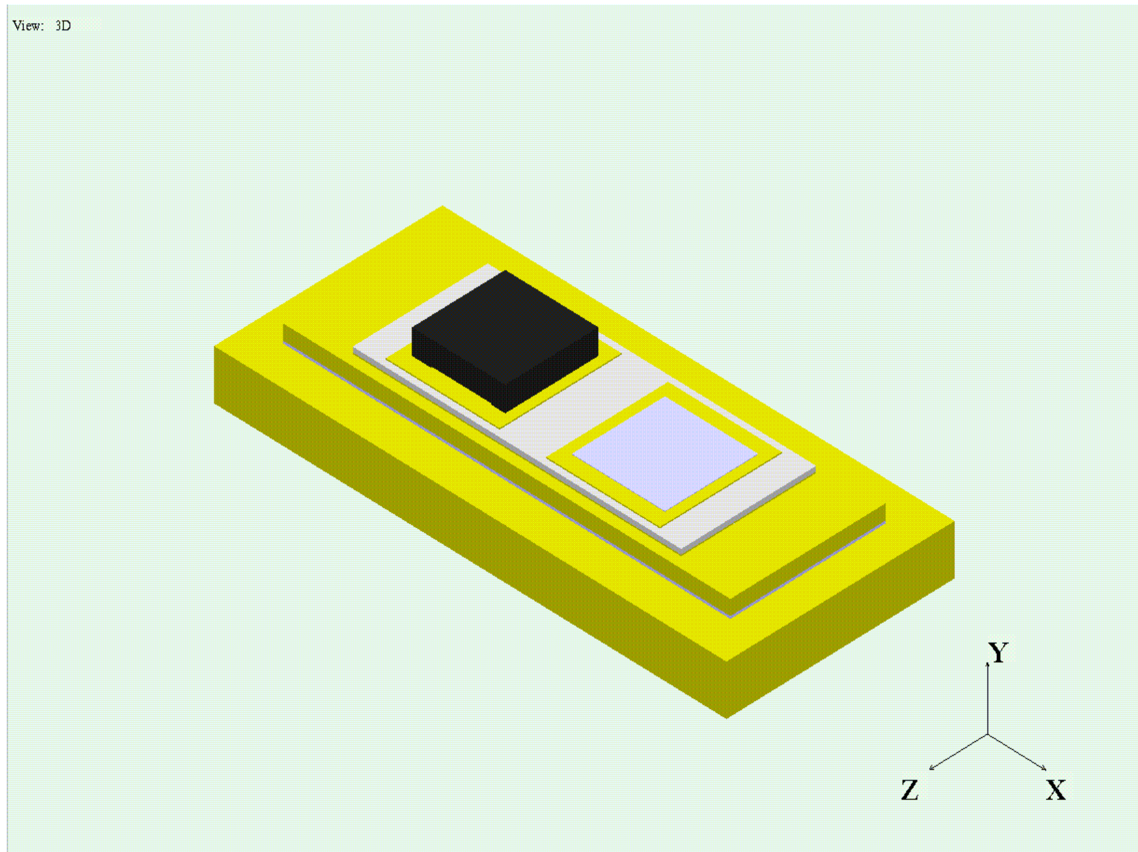


Figure 5.2. The geometry of the IGBT/ heat sink for 28W, 40W and 50W simulations.

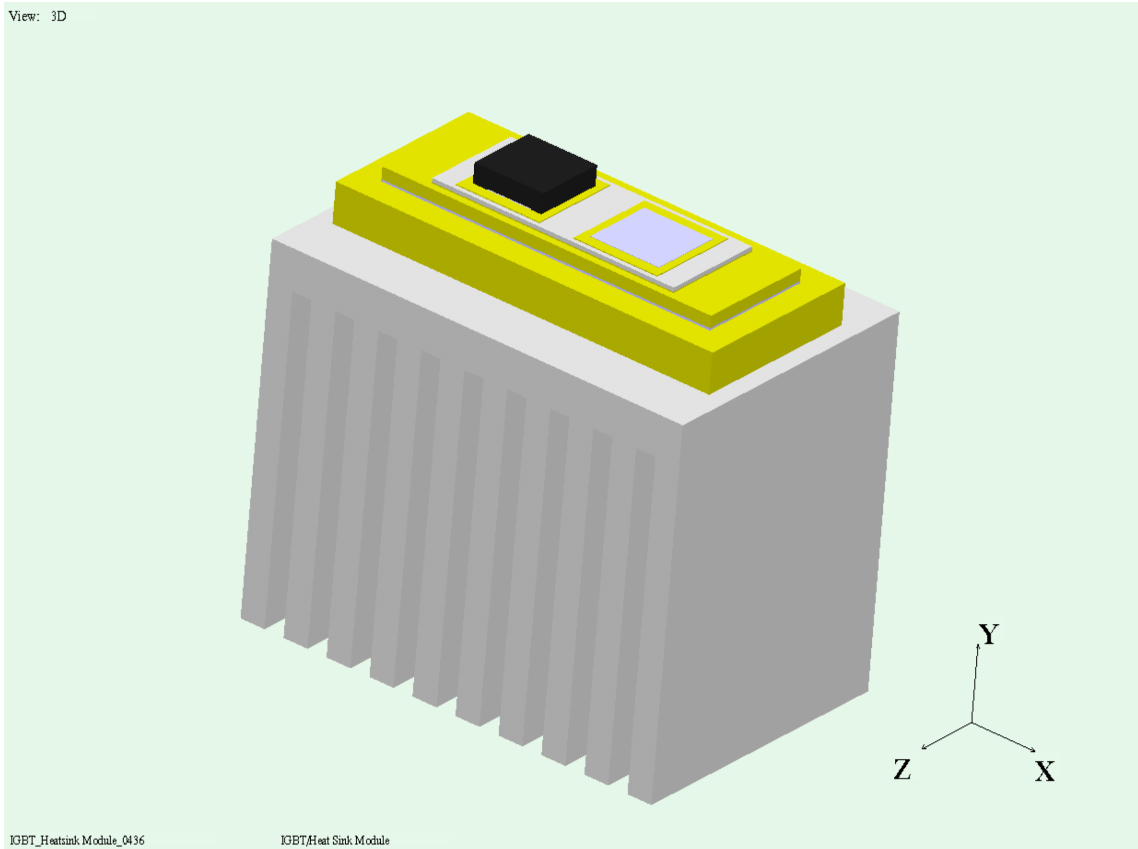


Figure 5.3. The geometry of the IGBT/ heat sink with a large heat sink for 100W simulations.

In the drawing board, cuboids are selected for the heat sink, the solder or thermal grease at the interface area, the heat spreader of the IGBT, the solder under the copper of the substrate, the copper of the substrate, the AlN substrate, the copper for the upper side of the substrate, the solder, the silicon, and the heat source.

The typical packaging materials and their properties used in this modeling are listed in Table 5.2.

Table 5.2. Thermal properties of materials.

Materials	Cu	AlN	Si	63Sn37Pb	Al
k (W/m*K)	393	180	136	51	240
Specific Heat (J/m^3Kg)	383	734	703	150	920

5.3. The Thermal Simulation Results

For temperature prediction at high power loss, such as 100W in this case, the experimental temperature distributions at three power loss points should match those obtained by simulation. These three points are set at 28W, 40W and 50W.

Figure 5.4 shows the simulation results for cases using the direct-soldering method and thermal grease at 28W.

Figure 5.5 shows the simulation results for cases using the direct-soldering method and thermal grease at 40W.

Figure 5.6 shows the simulation results for cases using the direct-soldering method and thermal grease at 50W.

The heat sink temperatures measured by experiment are presented in Table 5.3.

Table 5.3. The heat sink temperatures at 28W, 40W and 50W.

At Ambient Temperature, 49ºC	Power Loss		
	28W	40W	50W
Direct-Soldering	73.9ºC	85.2ºC	95.6ºC
Thermal Grease	72.8ºC	83.9ºC	94ºC

Table 5.4. The size of the heat sink.

	X (mm)	Y (mm)	Z (mm)	Thickness (mm)	Number of Internal Fins
Size	80	120	80	10	8

After displaying the three results, the 100W power loss is simulated. Figure 5.7 shows the temperature distribution at 100W power loss with a large heat sink (also see Table 5.4).

Table 5.5 shows the simulated peak temperature difference between cases using the direct-soldering method and the thermal grease.

Table 5.5. The peak temperature difference.

	28W	40W	50W	100W (with a Large Heat Sink)
Direct-Soldering	95.4192ºC	115.328ºC	131.916ºC	140.982ºC
Thermal Grease	96.2827ºC	116.557ºC	133.448ºC	144.759ºC
Difference (ºC)	0.8635	1.229	1.532	3.777

From the comparison of Table 5.3 with Figure 5.4, 5.5 and 5.6, it can be observed that thermal modeling gives very good trend predictions. Therefore, CFD thermal modeling has been found to be a fast and cost-effective tool for improving and optimizing the thermal management.

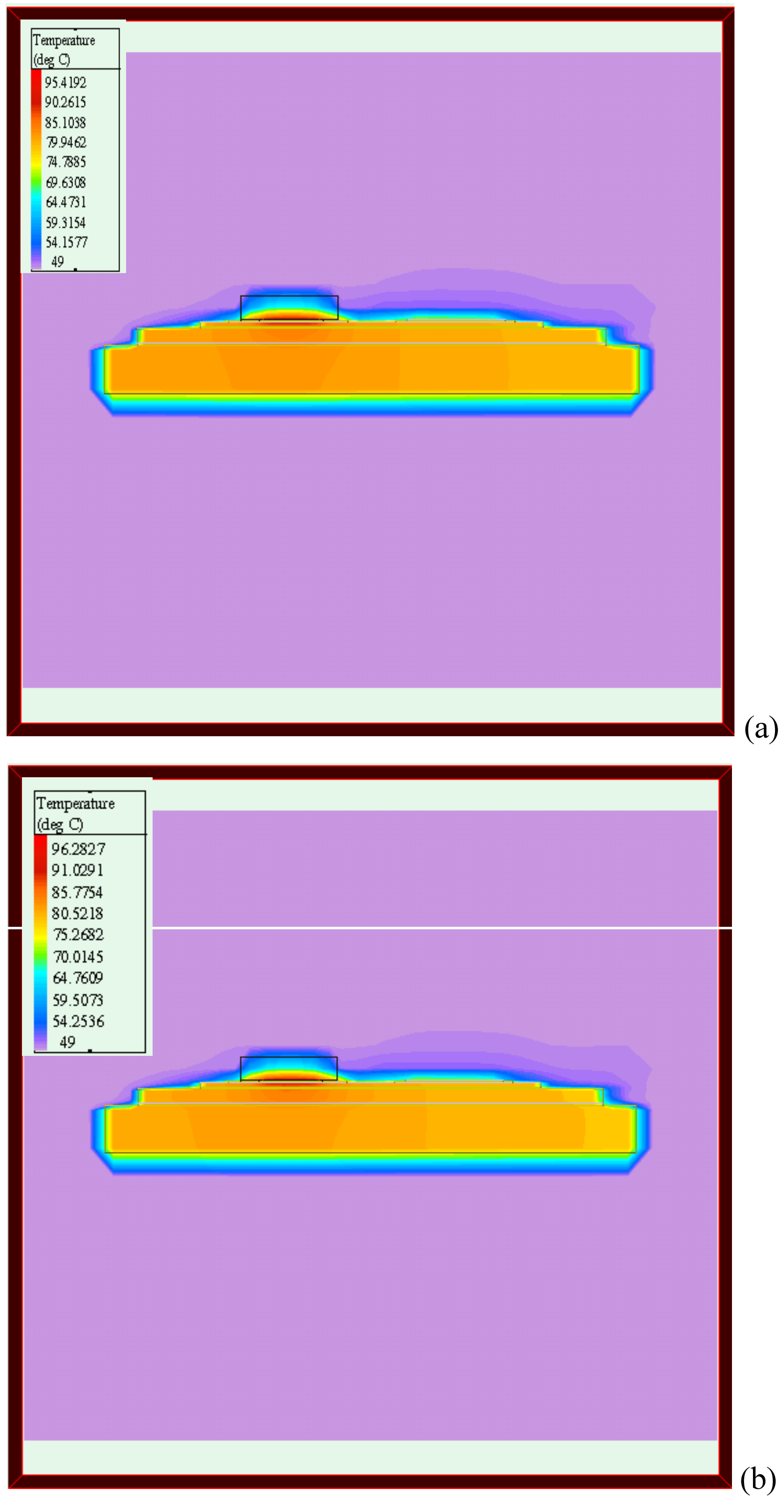


Figure 5.4. The simulation results at 28W for cases using the direct-soldering method (a) and thermal grease (b).

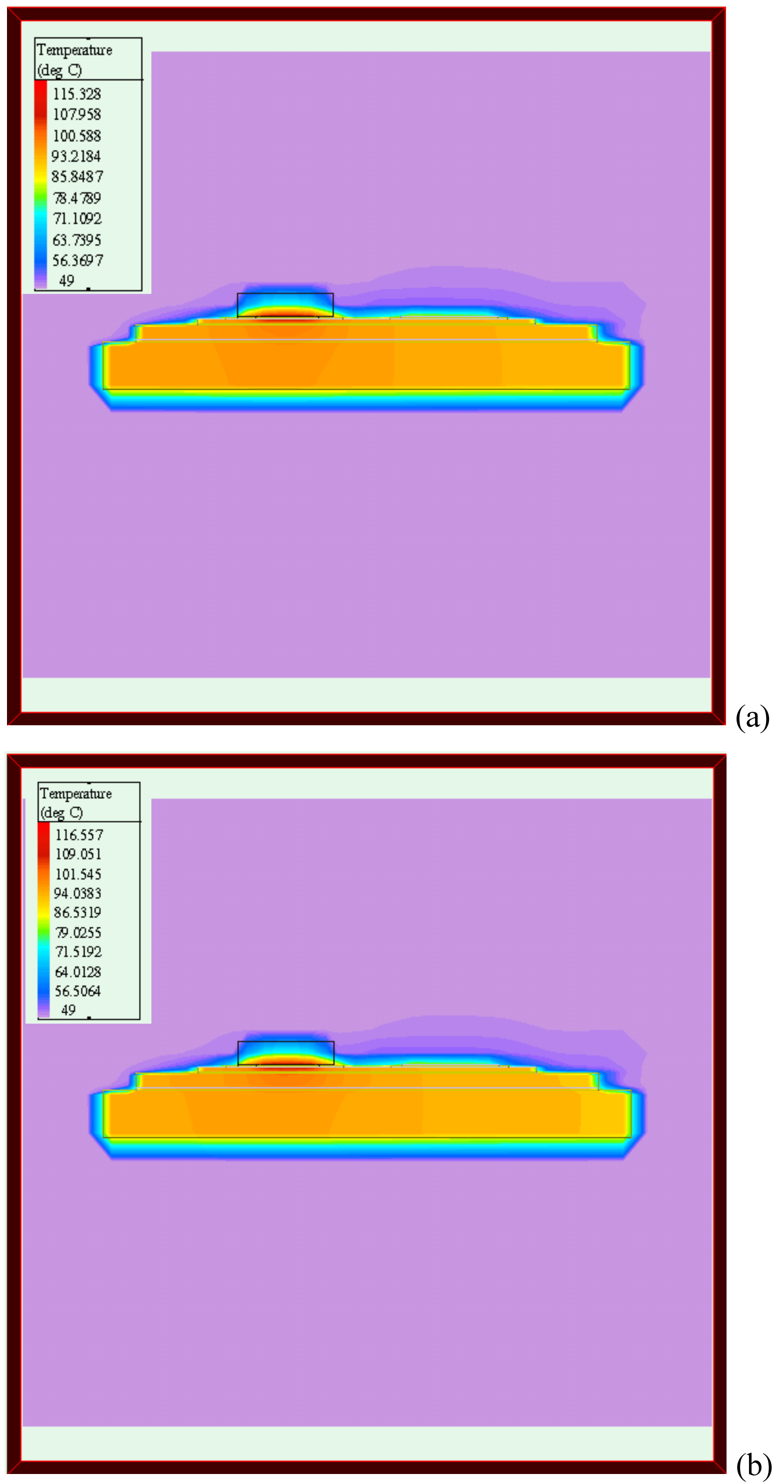


Figure 5.5. The simulation results at 40W for cases using the direct-soldering method (a) and thermal grease (b).

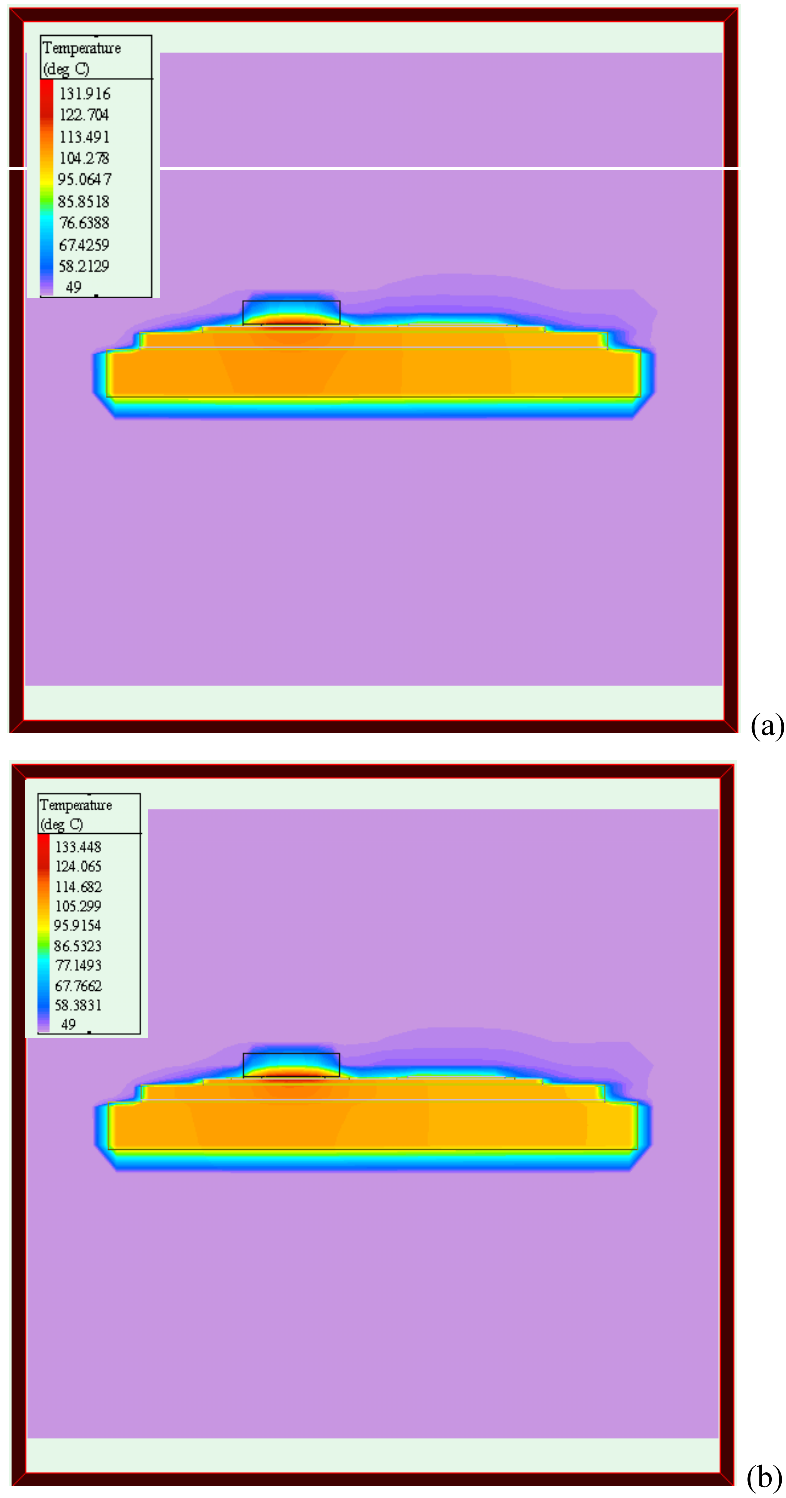


Figure 5.6. The simulation results at 50W for cases using the direct-soldering method (a) and thermal grease (b).

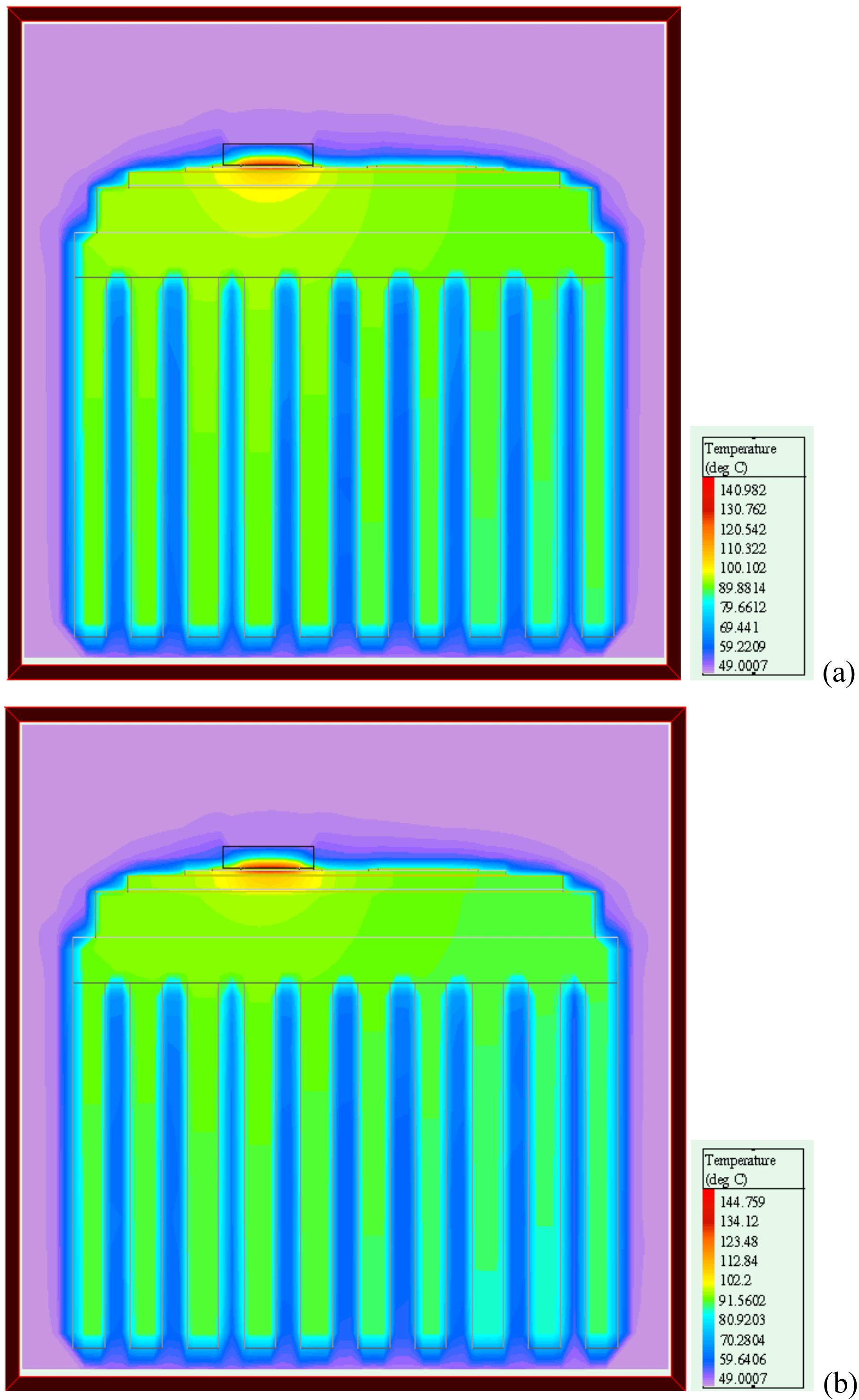


Figure 5.7. The simulation results at 100W with a heat sink (80*120*80) for cases using the direct-soldering method (a) and thermal grease (b).

Chapter VI. Conclusions and Future Work

6.1. Conclusions

The major design challenges in today's state-of-the-art, high-power density, power-conversion circuits are increasingly related to thermal management issues. Thermal grease and thermstrate are the current state-of-the-art technologies, for thermal interface materials to attach IGBT onto a heat sink; however, they still have high-thermal resistance due to limitation inherent in the large areas of air contact.

Direct-soldering gives a good solution to reduce the thermal resistance; however one considerable problem is reducing voids in the soldered interface area. If there are many air bubbles in the area, the thermal resistance of the direct-soldering can be higher than that of the conventional methods. The new methods to eliminate the voids are proposed in this thesis.

Thermal coupling tests verify the excellence of direct soldering with the smallest voided area for achieving low thermal resistance. The thermal resistance comparison of other cases is also presented. From the test results, the thermal resistance of direct-soldering case is four times lower than that of the thermal grease case at ambient temperature 74°C.

Thermal modeling and analysis are conducted using *Flotherm*. Heat distribution of each case using direst-soldering and thermal grease is displayed with 3D models. It shows a temperature difference for both cases.

The direct-soldering method is very useful for electric vehicle applications because of the need for high-power density and low-profile inverters. Moreover, thermal management is a critical issue because of the severe environment where electric vehicles are run.

In summary, it has been demonstrated that the reduction of thermal resistance in the interface using the direct-soldering method can especially solve the power limitation problem in high-power density, low-profile inverters for electric vehicle applications.

6.2. Future Work

In the future, research should be further conducted in the following directions.

Using the measured power loss of a system, *Flotherm* simulation can predict temperature distributions of the power module and a heat sink by using the different interface materials.

For instance, it can be simulated with conduction and switching losses of 350W in the one IGBT and conduction loss of 150W in the one diode, in the IGBT power module. The power losses of a real system are measured by experiment.

From this simulation, the thermal dissipation of the power module at the different cases, the direct-soldering and thermal grease, should make a difference.

It can be possible to use a 300A power module with the direct-soldering method in place of a 400A power module with the conventional thermal grease.

References

[1] Wuchen Wu, et al., "Thermal Stress Related Packaging Failure in Power IGBT Modules," Proceedings of 1995 International Symposium on Power Semiconductor Devices & ICs, Yokohama.

[2] http://www.orcusinc.com

[3] Frank P. Incropera and David P. DeWitt, "Fundamentals of Heat and Mass Transfer," Third edition

[4] Paul W. Barnes "Void Free Die Attachment for Multi-chip Modules Using Solder Alloy," 1998 International Conference on Multi-chip Modules and High Density Packaging.

[5] William W. So and Chin C. Lee, "Fluxless Process of Fabricating In-Au Joints On Copper Substrates," IEEE Transactions On Components and Packaging Technologies, Vol. 23, No. 2, June 2000.

[6] Frank Niklaus, Peter Enoksson, Edvard Kalvesten and Goran Stemme, "Void Free Full Wafer Adhesive Bonding," IEEE 2000.

[7] Jin Onuki and Yasunori Chonan, "A New Void Free Soldering Process in Large Area, High Power IGBT Module, " in Proceedings of ISPSO 2000, May 22-25, Toulouse, France.

[8] Toyota Technical Review, Vol. 48, No. 2, March. 1999, pp. 29~30.

[9] "Integrated Cooling System for Induction Motor Traction Drives", CARAT Program phase one final report, Charles E. Konrad, November 7, 1999.

[10] Toyota Technical Review, Vol. 48, No. 2, March. 1999.

[11] Shatil Haque and Guo-Quan Lu, "Thermal Management of Power Electronics Modules Via Acoustic Micrography Imaging," in Conference Record of Applied Power Electronics Conference, Feb. 2000, New Orleans, LA.

[12] Data sheet of NC-559 series, AMTECH.

[13] L.W. Kessler, P.R. Palermo and A. Korpel, "Practical High Resolution Acoustic Microscopy," Acoustical Holography, Vol. 4, ed. G. Wade (New York: Plenum Press, 1972), pp. 51-71.

[14] J.A. Cunningham and C.F. Quate, "High-Resolution Acoustic Imaging by Contact Printing," Acoustical Holography, Vol. 5, ed. P.S. Green (New York: Plenum Press, 1973), pp.83-102.

[15] R.A. Lemons and C.F. Quate, "Acoustic Microscope—Scanning Version," Applied Physics Letters, 24 (4), February 15, 1974, pp. 163-165.

[16] H.K. Wickramasinghe, "Scanning Acoustic Microscopy: A Review," J. Microscopy, 129, Part 1, January 1983, pp. 63-73.

[17] C.F. Quate, A. Atalar, and H.K. Wickramasinghe, "Acoustic Microscopy with Mechanical Scanning—A Review," Proceedings of the IEEE, 67 (8), August 1979, pp. 1092-1114.

[18] A. Briggs, Acoustic Microscopy, ed. R. Brook, et al. (Oxford, U.K.: Clarendon Press, 1992), p. 58.

[19] R.S. Gilmore, et al., "Acoustic Microscopy from 10 to 100 MHz for Industrial Applications," Phil. Trans. of the Royal Soc. of London A, 320, 1986, pp. 215-235.

[20] M. Hoppe and J. Bereiter-Hahn, "Applications of Scanning Acoustic Microscopy–Survey and New Aspects," IEEE Trans. on Sonics and Ultrasonics, SU-32 (2) March 1985, pp. 289-301.

[21] G.A.D. Briggs, et al., "Acoustic Microscopy of Old and New Materials," Acoustical Imaging, 17, 1989, pp. 1-16.

[22] A. Briggs, ed., Advances in Acoustic Microscopy, Vol. 1 (New York: Plenum Press, 1995).

[23] Ralph E. Locher, New Package for Pressure Mounting, application brief AB-9801, IXYS 1998.

[24] Training Course, Flotherm Version 2.1.

Vita

The author, Junhyung Kim, was born in Daegu, Korea, on November 5, 1972. He completed his B.S. degree in electrical engineering from Dong-A University, Pusan, Korea in 1998. He then joined the Center for Power Electronics Systems of Virginia Tech in 1998 for his master degree in electrical engineering. His primary interests are inverters, power packaging, and modeling of DC- DC converters.

He would be joining Elgar Electronics Corporation in San Diego as a new product develop engineer after his graduation.