

DQ-Frame Small-Signal Stability Analysis of AC Systems with Single-Phase and Three-Phase Converters

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(ABSTRACT)

The widespread integration of power converters in applications such as microgrids and data centers has introduced significant stability challenges. This dissertation presents a novel approach to modeling and comprehensive stability analysis for both single-phase and three-phase converters, addressing vital gaps in the existing literature. The first part of the dissertation (Chapters 2 to 4) focuses on single-phase power supply units, proposing an impedance model and a loop gain model based on dq-frame analysis. These models have been validated through extensive experimental testing, demonstrating their effectiveness in stability analysis across a range of system configurations, including single-phase, three-phase three-wire, and three-phase four-wire systems. The second part (Chapters 5 and 6) examines three-phase converters used for integrating renewable energy into microgrids. It introduces a grid-forming control, followed by a detailed investigation into its impedance modeling and stability assessment. This part specifically tackles the challenges posed by the appearance of right-half-plane poles in stability analysis, proposing a new stability margin index to address these issues. The efficacy of these research findings is further substantiated by the development and implementation of a Power-Hardware-in-the-Loop testbed, providing practical validation. Overall, this dissertation has enhanced the modeling, understanding, and management of stability issues in power electronics systems, offering valuable insights and methodologies that are likely to influence future research and development in the field.

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(GENERAL AUDIENCE ABSTRACT)

Power electronics play a crucial role in many of today's advanced technologies, including Renewable Energy (like wind and solar power), Electric Vehicles, Cloud Computing, and Artificial Intelligence. In renewable energy, power electronics are key for converting energy sources for efficient grid integration. Electric vehicles rely on power converter systems for charging their batteries and driving their motors. Similarly, in Cloud Computing and Artificial Intelligence, power electronics ensure that the computers and servers in data centers have a steady and reliable power supply for operation. However, using these advanced power electronics on a large scale, like in wind farms or data centers, can lead to challenges, including many reported system instability issues. These issues highlight the importance of a thorough analysis and understanding of the behavior and interaction of power electronics systems.

In addressing these challenges, power electronics converters, conceptualized as a blend of circuits and control systems, demand comprehensive modeling from the ground up. Such modeling is essential to understanding their behavior, ranging from individual components to the entire system. This is key to establishing a clear connection between intricate design details and overall system performance. With power electronics systems becoming more complex and the continual emergence of new technologies, there remains a significant array of unanswered questions, especially in the domain of stability analysis for AC power electronics systems. This dissertation delves into two prominent modeling methods for stability analysis: impedance modeling and loop gain modeling. By exploring and addressing specific gaps identified in prior research, this work aims to contribute to a more profound understanding and enhanced application of these critical methods.

The research presented in this dissertation is methodically divided into two main sections. The first section, including Chapter 2 to Chapter 4 is dedicated to exploring single-phase converter power supply units (PSUs) systems. This section introduces innovative models for analyzing their stability, applicable to single-phase PSUs in various system configurations, including both single-phase and three-phase setups. This modeling approach is a significant step forward in understanding and enhancing the stability of single-phase PSU loads. The second section, including Chapter 5 and Chapter 6, delves into the analysis of three-phase converters used in integrating renewable energy sources into microgrids. A notable feature of these converters is their grid-forming control mechanism. This part also explores modeling the impact of these converters on microgrid stability. Moreover, the issue of right-half-plane (RHP) poles in impedance analysis that can affect stability analysis is addressed. It proposes innovative methods for assessing stability margin in such conditions.

In conclusion, this research made advancements in the modeling for stability analysis of power converter systems. For single-phase converters, the developed impedance model and loop gain model, based on dq-frame analysis, have been proven to be accurate. These models are versatile for stability analysis in various AC systems with single-phase PSU loads. In the study of three-phase converters, the grid-forming converter was successfully designed to support the grid as a distributed energy resource interface. This design contributes positively to microgrid stability. Furthermore, to address the presence of RHP poles in stability analysis, a new stability margin index was defined to better understand and manage these challenges. These findings represent important steps forward in the field of power electronics and contribute valuable insights for future research and development.

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Chapter 1

Introduction

1.1 Background

Power electronics infrastructure serves as a cornerstone in several contemporary fields, including Renewable Energy, Electric Vehicles, and Artificial Intelligence. Its pivotal role becomes apparent in each domain's operations. For instance, in Renewable Energy, such as wind and solar power, power electronics converters are indispensable for facilitating seamless grid integration. Similarly, Electric Vehicles rely on these converters for critical functions such as battery charging and motor drive. Moreover, the backbone of Artificial Intelligence resides in data centers, where multi-stage power supply converters are essential for continuous operation.

However, the integration of massive power converters into various systems has introduced significant system-level challenges, prominently among them being instability issues. In 2017, a Texas wind farm experienced sub-synchronous resonance—an occurrence characterized by very low-frequency oscillations [1]. These events often stem from interactions between wind power converters and the grid, influenced by factors such as the converter's phase-locked-loop design, the grid's short circuit ratio, or the presence of static var compensators or series capacitors. Despite prior efforts to mitigate such risks, including the installation of damping controllers, unforeseen occurrences persisted due to inaccuracies in the modeling process. On the other hand, the integration of grid-tied inverters for distributing renewable energy into the grid has been observed to reduce the grid's inertia, adversely affecting its stability. Unlike conventional grids supported by large-scale generators to sustain inertia and reliability, modern grids require alternative approaches to maintain stability. Hence, emerging control concepts, such as grid-forming control, have been developed for grid-tied converters for the purpose of sustaining grid inertia. Examining the impact of grid-forming converters on grid stability is a crucial investigation with significant value.

Similarly, instability issues also manifest in data centers, where low-frequency oscillations have been observed in facilities such as the META data center [2]. A data center has many single-phase power supply unit (PSU) loads to power the servers. Such instability is mainly due to the interactions of the many PSU loads and the distribution lines. These incidents not only result in equipment damage but also pose significant risks to data and capital. Since the server loads are bought from the vendors with encryption, and the infrastructure is designed and constructed by META, an operation with unreasonable design of source and load may have occurred.

Given the complexity and criticality of modern power electronics infrastructure, there is a need for in-depth analysis and understanding of stability issues across different converters and systems. The following paragraphs introduce the technical approaches for small-signal stability analysis of power electronics systems.

1.2 Evolution of Small-Signal Stability Analysis Approaches in Power Electronics Systems

Small-signal analysis involves evaluating system behavior around a certain operating point, therefore, small-signal stability denotes if it stays stable under certain conditions. The techniques for small-signal stability analysis in power electronics systems have been under investigation for several decades. Several approaches exist for analyzing small-signal instability issues, among which impedance analysis, loop gain analysis, and eigenvalue analysis are notable [3] –[5]. The main challenges of power electronics stability analysis include various controls, nonlinearity, multi-vendors, and black-box models [6]. Hence, the ability to measure its dynamic characteristics becomes crucial. Advancements in measurement tools enable the measurability of impedance and loop gain analyses, although under different conditions.

A negative feedback loop is used to achieve a desired output despite any input disturbances or component variations. The loop gain-based criterion has a long history, with Heinrich Barkhausen first recognizing the importance of loop gain as a parameter for characterizing electronic feedback amplifiers in 1921. Further development was made by Hendrik Wade Bode and Harry Nyquist at Bell Labs in the 1930s [7]-[9]. Loop gain analysis is also critical to understanding the performance

and stability of power electronics closed-loop systems [7], [8]. Power converters are typically designed with a loop gain of reasonable cutoff frequency and sufficient margin before being installed in the field. Such designs are generally based on an average model with an ideal source and at a given operating point. Experimental measurements are also needed due to the components' non-ideality and the model accuracy limits [9]-[11]. To measure loop gain, a primary scheme is to inject a small-signal perturbation at one node of the feedback loop and then measure the forwarded and returned nodes of the injection node, as shown in Figure 1-1. Measuring converters' loop gain has become a common industry practice as a specification of the product [12], [13].

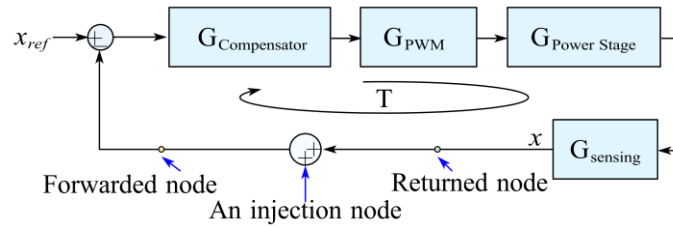


Figure 1-1 Block diagram of loop gain and a measurement method.

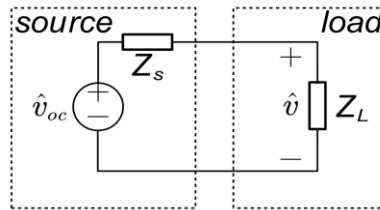


Figure 1-2 Source and load impedance definition.

On the other hand, impedance-based stability analysis originated in 1976 when R. D. Middlebrook developed a criterion for filter design of DC-DC buck converters to avoid any instability issues [10]. The impedance ratio Z_s/Z_L , shown in Figure 1-2, appears to be like the loop gain of a cascaded system in all the closed-loop transfer functions, therefore it is also named minor loop gain. Stability can still be determined using the usual techniques, including phase and gain margins, and the Nyquist stability tests of the impedance ratio term. At the same time, the actual voltage loop gain of the converter with consideration of the filter's impact can be determined based on the Extra element theorem [9]. Therefore, there are two distinct approaches to determining the stability boundary of the regulator when modified by the addition of an input filter: the loop gain-based approach and the impedance analysis approach. It can be verified that the two approaches

predict identical closed-loop poles and characteristic equations [10]. Hence, the two approaches should predict identical stability conditions and boundaries.

After the impedance criterion developed by R. D. Middlebrook to deal with the filter-converter system, it was extended to systems with dc-dc converters on both the source and load sides [11], [12]. Later, in the mid-1990s, Mohamed Belkhat applied a similar concept to the dq impedance of three-phase AC systems based on the rotating frame theory [13]. Since then, impedance-based stability analysis has been widely employed to analyze three-phase AC systems [14]-[17]. There are also other types of impedance-based analysis. The sequence impedance, employing harmonics linearization, linearizes in the frequency domain, thereby obtaining a complex transfer function. The modified sequence impedance, proposed later, serves to identify the equivalence between DQ impedance and sequence impedance. At the same time, the loop gain-based approach is still used to study the stability of AC systems with three-phase converters [18]-[21]. These two approaches are acknowledged to be effective for assessing system stability.

However, there are practical implementation differences between the two approaches. For any application, it mainly involved two kinds of participating entities, the system integrators and converter vendors. For system integrators, such as utility ERCOT, Google, etc., most components are from different vendors and they may not have access to each converter's information, so impedance analysis becomes more applicable. Terminal impedance is measurable without any need for internal access, and the system integrators can define specifications for each vendor to ensure an overall stable operation [22]. On the other hand, for converter vendors such as ABB, and Delta Electronics, although impedance analysis has also gained much attention, loop gain analysis is still more common among design engineers. In these cases, the loop gain measurement function can be directly enabled in the digital controller [23]. The measurement data can be extracted and sent to a designed central control to assess the stability of the system. It does not require an additional instrument to measure system impedance. However, adding such a device would require extra costs and detailed design considerations. For instance, selecting the appropriate measurement technique, voltage/power rating, hardware integration with the existing system, and maintenance

of the device are some of the potential challenges that may arise during its design and implementation. Also, loop gain analysis can be used to assess transient response.

1.3 Motivations and Objectives

Numerous research has investigated both impedance and loop gain approaches for power electronics system stability analysis. This dissertation aims to advance the current research on these two approaches by addressing gaps that remain unexplored in existing literature. Central to this effort is the focus on modeling, which provides essential tools for system designers to ensure stability in advance.

The research has two main objectives: Firstly, to investigate single-phase converters, including impedance analysis of one single-phase PSU load, and the subsequent stability analysis of systems incorporating such loads, followed by a loop gain analysis. Secondly, the study extends to three-phase converters, including analyzing the stability impact of a grid-forming converter and analyzing the open-loop RHP poles in impedance analysis.

1.4 Dissertation Outline and Summary of Contributions

In this dissertation, analysis of single-phase converters is shown in Chapter 2, Chapter 3, and Chapter 4, analysis of three-phase converters is shown in Chapter 5 and Chapter 6, and the DQ frame modeling concept is employed for both loop gain analysis and impedance analysis.

Chapter 2 proposes a fully analytical model for the input d-q impedance of a single-phase PFC converter, considering the impact of different control loops and the cascaded dc-dc converter load. The model shows that a higher dc voltage control bandwidth will result in a wider frequency range of the negative resistor, and the cascaded dc-dc converter load will result in a lower magnitude and phase of the d-d channel term at low frequency. The model is verified by measured impedance.

Chapter 3 proposes impedance models within the time-invariant framework for systems with single-phase loads in different system configurations, including single-phase systems, three-phase three-wire systems, and three-phase four-wire systems. The proposed models can be used for impedance specifications and assist system-level design from the stability perspective. Both

simulation and experimental results validate the model and demonstrate its effectiveness in analyzing the stability of systems with single-phase loads.

Chapter 4 proposes a novel voltage loop gain model based on the d-q frame concept for a single-phase converter. The proposed voltage loop gain model is more accurate for the converter when it is presented in a single-phase system than the quasi-static approximation method, which even failed to analyze the case when it is present in a three-phase system. The proposed loop gain model reveals the mechanism of how the source dynamics are coupled into the control loops of PFC, filling the gap in analyzing the stability of AC systems with single-phase loads using the loop gain method. The accuracy of the loop gain model is verified through simulations and experiments.

Chapter 5 presents the design of a grid-forming converter equipped with a novel frequency-power droop loop, enhancing its capability for grid-support functions. This chapter derives an accurate impedance model for the converter and assesses its stability impact on a microgrid. To validate the study's findings, a power-hardware-in-the-loop (PHIL) testbed is developed.

Chapter 6 focuses on possible right-half-plane (RHP) poles in the minor loop gain when applying forbidden-region-based stability criteria. The presence of these poles can significantly alter the characteristic loci, rendering many traditional stability-margin criteria inapplicable. To address this challenge, an alternative stability margin index is proposed for such scenarios. The results are validated using the PHIL testbed introduced in the previous chapter, which incorporates a converter with impedance measuring functions.

The final chapter provides a comprehensive summary of the dissertation's findings.

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Chapter 2

Impedance Modeling and Validation of a Single-Phase Power Supply Unit

2.1 Introduction

Many applications require a power factor correction circuit (PFC) in front of an isolated step-down dc-dc converter such as the electric vehicle (EV) onboard charger and the power supply unit (PSU) used in telecom and data center servers. A PSU with a totem-pole topology is shown in Figure 2-1 [1], [2]. Dynamic interactions between the power source and many PFCs may bring unwanted effects to the system, such as low-frequency oscillations and even instabilities. Several data centers have been reported to suffer from low-frequency resonance instability [3], [4]. Similar instability could happen in a future distribution system with many EV chargers working together [5]. To better understand and avoid similar issues, it is important to model and analyze the stability of such systems.

For stability analysis of both ac and dc systems, the impedance-based method is widely adopted nowadays. Compared with other methods, such as eigenvalue analysis and loop-gain analysis, the impedance-based analysis does not need internal parameters of the system [6] - [10]. As such, in practice system integrators can use instrumentation to measure the impedance of the power source and specify requirements for the load impedance according to the desired stability margins, which are typically based on the Nyquist Stability Criterion for dc interfaces, and on the Generalized Nyquist Criterion (GNC) for ac interfaces [11]-[13].

The impedance-based stability analysis has been investigated in depth in dc and three-phase ac systems, but it is still underexplored in single-phase systems given its inherent time-varying nature [14]. Impedance modeling for single-phase loads, especially in medium-voltage railway systems, has been studied in existing literature, in which several methods have been developed. These methods can be categorized into three kinds, harmonic linearization, d - q modeling, and dynamic

phasors. Harmonic linearization is based on the linear time-periodic (LTP) framework, which is used to address the sinusoidal time-varying behavior by linearizing the model in the frequency domain instead of the time domain [15]-[19]. However, the resulting impedance is usually a large dimensional matrix. To simplify the model, Ref. [20] proposed sequence impedance modeling by decomposing the system into a positive- and a negative-sequence subsystem. Ref. [3] then used the sequence impedance modeling approach to develop the overall input impedance models of single-phase PFC converters to study the resonance phenomenon experienced in Facebook data centers. Ref. [21] extended the impedance model into a 3-by-3 matrix concerning the frequency coupling effect of the phase-locked loop (PLL). Ref. [22] proposed a simpler and more efficient equivalent single-input-single-output (SISO) model for single-phase system modeling, and Ref. [17] further addressed the high-frequency coupling effect to improve model accuracy using a similar approach.

However, it is often desirable to transform an LTP system into an approximated linear time-invariant (LTI) system to apply well-known LTI system analysis tools. One approach for single-phase system analysis is to create virtual frames by phase-shifting and then transforming the artificial three-phase system into a virtual synchronous reference ($d-q$) frame where dc operating points may be readily obtained. This in turn makes possible the derivation of small-signal impedances using linearization [14]. Yet another alternative approach was presented in [23], which proposed the use of dynamic phasors and showed their equivalence with the $d-q$ modeling-based method when the dc dynamics are ignored. This however represents a shortcoming since the dc bus dynamics are one of the key factors impacting low-frequency instability, and as such, they should be modeled.

Among all the existing methods, the $d-q$ modeling-based method is straightforward and mathematically solid. Although this idea has been investigated in the literature, the impedance modeling of a single-phase PFC converter in the virtual $d-q$ frame has not been covered, which is important for the stability analysis in low voltage distribution systems such as data centers [24] - [27]. To fill this gap, this dissertation proposes a fully analytical model for the input $d-q$ impedance of a single-phase PFC converter, considering the impact of different control loops and the cascaded

dc-dc converter load. This chapter first introduces the virtual d - q frame modeling method of a single-phase PFC converter and addresses the frequency coupling impact, then derives the PFC converter's small-signal impedance in the virtual d - q frame and shows the impedance experimental measurement results.

2.2 PFC Converter Model in the D-Q Frame

2.2.1 Modeling of a PFC Converter in the Virtual D-Q Frame

This section introduces the virtual d - q modeling method and its application for a single-phase PFC converter. The rationality and impact of the LTI system approximation are first explained. A totem-pole topology PFC converter operating in continuous-current-mode is studied, the circuit, and control of which are shown in Figure 2-1. Its controller contains a proportional-resonant (PR) based current controller, a proportional-integral (PI) based dc voltage controller, and a phase tracking unit by scaling the input voltage by a gain of $1/|V_{ac}|$, and an ac voltage feedforward control. The PFC converter parameters are defined in Table 2-1. Its power-stage average model in one switching cycle is shown in Figure 2-2 (a). The relationship between the input and output of the switching network can be described using (2-1) and (2-2).

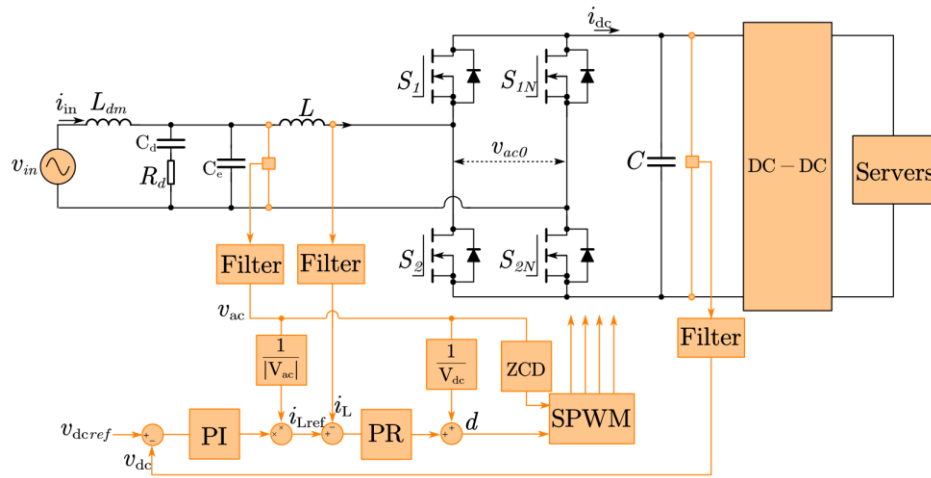


Figure 2-1 Single-phase totem-pole PFC and cascaded dc-dc converter load.

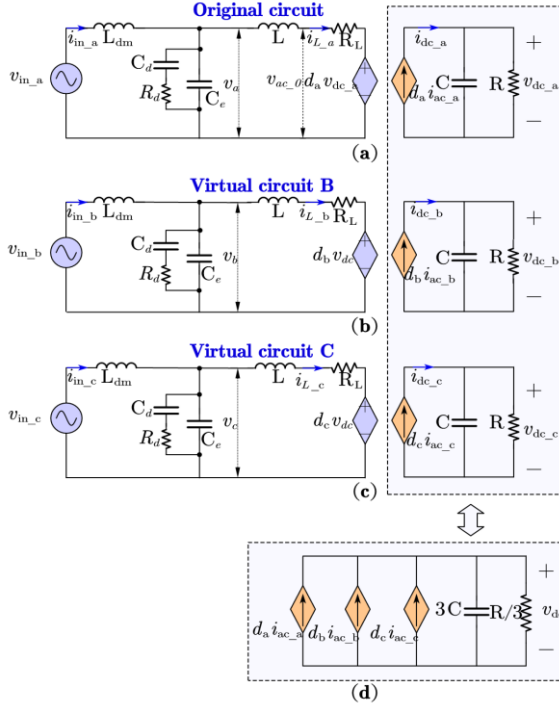


Figure 2-2 PFC model and equivalent circuit based on virtual frames.

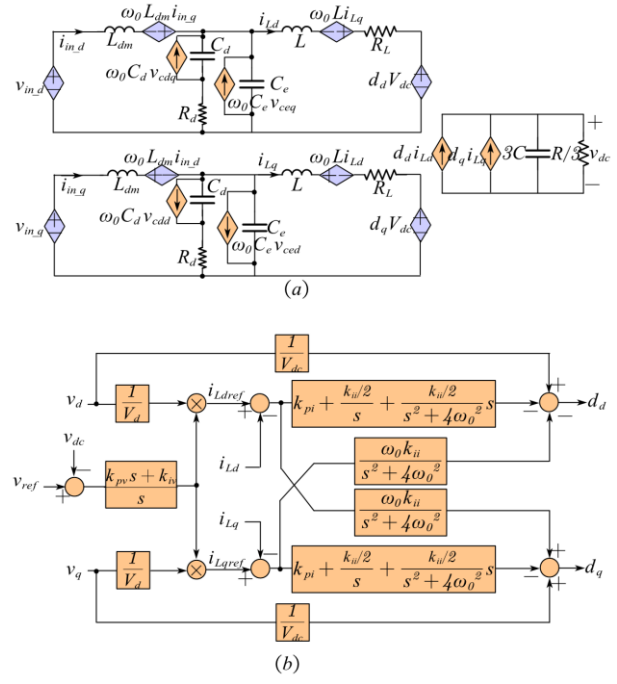


Figure 2-3 d-q frame model.

$$v_{ac0} = d_a \cdot v_{dc_a} \quad (2-1)$$

$$i_{dc_a} = d_a \cdot i_{L_a} \quad (2-2)$$

Table 2-1 PFC converter parameters.

Symbol	Description	Value	Symbol	Description	Value
P	PFC rated power	4.5 kW	L_{dm}	Input EMI filter differential mode inductance	15uH
V_{ac}	PFC-rated input rms voltage	240 V _{rms}	C_d	Input EMI filter damping branch capacitor	2 uF
I_{ac}	PFC-rated input rms current	18.8 A _{rms}	C_e	Input EMI filter differential mode capacitor	2 uF
f_0	PFC input voltage fundamental frequency	60 Hz	C_{dm}	Equivalent filter differential mode capacitor	4 uF
ω_0	PFC input voltage angular frequency	376.8 rad/s	f_{sw}	Switching frequency	100 kHz
L	Inductance of the PFC boost inductor	170 uH	k_{ii}	Current PR controller integral gain	0.125
C	Capacitance of the PFC output capacitor	1.7 mF	k_{pi}	Current PR controller proportional gain	0.02

R	Resistance of dc load	35 Ω	k_{iv}	DC voltage controller integral gain	5.44
V_{dc}	DC Voltage	400 V	k_{pv}	DC voltage controller proportional gain	0.136

For a three-phase converter, a common method for small-signal analysis is through modeling in the d - q frame to obtain time-invariant operating points. For a single-phase PFC converter, a similar method can be used by creating two virtual frames. As is shown in Figure 2-2 (a), the original PFC converter (with resistor load) is considered as Phase A, and by phase-shifting, all its electrical variables by -120° and 120° , virtual Phase B and Phase C circuits are created as shown in figures (b) and (c). Because Phase B and Phase C circuits are created through phase-shifting, the dc bus dynamics of the three circuits are considered the same. The double line-frequency ripples of the dc-bus voltage are ignored considering that their magnitude is much smaller than the dc voltage average value. Therefore, the dc buses of the three circuits can be combined into one dc bus, as is shown in Figure 2-2 (d). By aligning the Park transformation angle with v_{in_a} , the virtual three-phase circuit in Figure 2-2 is converted into the d - q frame as shown in Figure 2-3 (a). The controllers of the original PFC and the two virtual circuits can also be combined and transformed into the d - q frame as derived below. For the current loop and input voltage feedforward control, the three circuits' controller models can be written as (2-3).

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \frac{1}{V_{dcref}} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - PR \left(\begin{bmatrix} i_{Laref} \\ i_{Lbref} \\ i_{Lcref} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \right) \quad (2-3)$$

$$PR = k_{pi} + \frac{k_{ii}s}{s^2 + \omega_0^2} \quad (2-4)$$

Applying the d - q transform to (2-3) there exists [30],

$$\begin{bmatrix} d_d \\ d_q \end{bmatrix} = \frac{1}{V_{dcref}} \begin{bmatrix} v_d \\ v_q \end{bmatrix} - \mathbf{G}_{PR} \left(\begin{bmatrix} i_{Ldref} \\ i_{Lqref} \end{bmatrix} - \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} \right) \quad (2-5)$$

$$\mathbf{G}_{PR} = \begin{bmatrix} k_{pi} + \frac{k_{ii}/2}{s} + \frac{k_{ii}s/2}{s^2 + 4\omega_0^2} & \frac{k_{ii}\omega_0}{s^2 + 4\omega_0^2} \\ -\frac{k_{ii}\omega_0}{s^2 + 4\omega_0^2} & k_{pi} + \frac{k_{ii}/2}{s} + \frac{k_{ii}s/2}{s^2 + 4\omega_0^2} \end{bmatrix} \quad (2-6)$$

Considering the dc voltage loop and input phase tracking,

$$\begin{bmatrix} i_{La_{ref}} \\ i_{Lb_{ref}} \\ i_{Lc_{ref}} \end{bmatrix} = \begin{bmatrix} (V_{dcref} - v_{dc_a}) \cdot PI \cdot \frac{v_a}{|V_{ac}|} \\ (V_{dcref} - v_{dc_b}) \cdot PI \cdot \frac{v_b}{|V_{ac}|} \\ (V_{dcref} - v_{dc_c}) \cdot PI \cdot \frac{v_c}{|V_{ac}|} \end{bmatrix} = \frac{(V_{dcref} - v_{dc}) \cdot PI}{|V_{ac}|} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2-7)$$

$$PI = k_{pv} + \frac{k_{iv}}{s} \quad (2-8)$$

Applying Park's transform to (2-7), it becomes,

$$\begin{bmatrix} i_{Ld_{ref}} \\ i_{Lq_{ref}} \end{bmatrix} = \frac{(V_{dcref} - v_{dc}) \cdot PI}{V_d} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (2-9)$$

The whole controller's d - q frame format can be derived, as shown in Figure 2-3 (b).

2.2.2 Justification and Impact of Time-Invariant Approximation

With negligible power loss for a high-efficiency high power factor PFC converter, the input ac power p_{ac} and output dc power p_{dc} are balanced,

$$p_{ac} = p_{dc} = v_{ac} i_{ac} = \frac{V_{ac} I_{ac}}{2} (1 + \cos(2\omega_o t)) \quad (2-10)$$

which causes a double-line frequency component in the dc bus voltage and its magnitude is mainly limited by the dc capacitor value. From (2-1), the dc bus double-line frequency ripples result in a third harmonic component on the ac side, and back and forth, an infinite number of harmonics appear, which is known as frequency coupling. Because of these harmonics, the system is still mildly periodic in the d - q frame instead of being time-invariant. However, although these harmonics lead to a certain error in the d - q frame modeling results, the approximated LTI model can account for all the important behavior of the system because the magnitude and number of harmonics are much smaller than the fundamental components.

Figure 2-4 (a) and (b) showcase the frequency response of a PFC converter using the parameters in Table 2-1. Figure 2-4 (a) shows the input ac current frequency spectrum when no perturbation is added. The response frequency points are dominated by f_o and $3f_o$ with small $5f_o$ and $7f_o$ components. Figure 2-4 (b) shows the current frequency spectrum when a 90 Hz (f_p) voltage perturbation with a magnitude of 0.5 % of the input voltage is added. Because of the frequency coupling characteristics, there will be an infinite number of harmonics in the current excited by

the voltage perturbation. The dominant response frequency points are f_p , and $f_p \pm 2f_0$ in addition to f_0 , $3f_0$, $5f_0$, and $7f_0$. The frequency response at $f_p - 2f_0$ and $f_p + 2f_0$ are around 0.08 % and 0.02 % which are much smaller than that at f_p , which is 0.52 %. As illustrated, the ac side harmonics result from the dc voltage double-line frequency ripples through frequency coupling, so decreasing these ripples should attenuate harmonics. Figure 2-4 (c) shows the decreasing ratio of the frequency response at $f_p - 2f_0$ and $f_p + 2f_0$ to f_p with higher dc capacitance and smaller dc voltage ripples. As observed, the maximum sum of the dominant harmonics is lower than 20 % of the original perturbation at f_p , which renders the reasonable assumption to consider the weakly periodic system as a time-invariant system. Figure 2-4 (d) shows the ac current frequency spectrum when adding a 180 Hz (f_p) voltage perturbation with a magnitude of 0.5% of the input voltage. Compared with Figure 2-4 (b), the amount of f_p ($3f_0$) component is much higher because most of it results from the original power stage frequency couplings. Therefore, the measured impedance at f_p does not reflect the actual small-signal impedance at f_p .

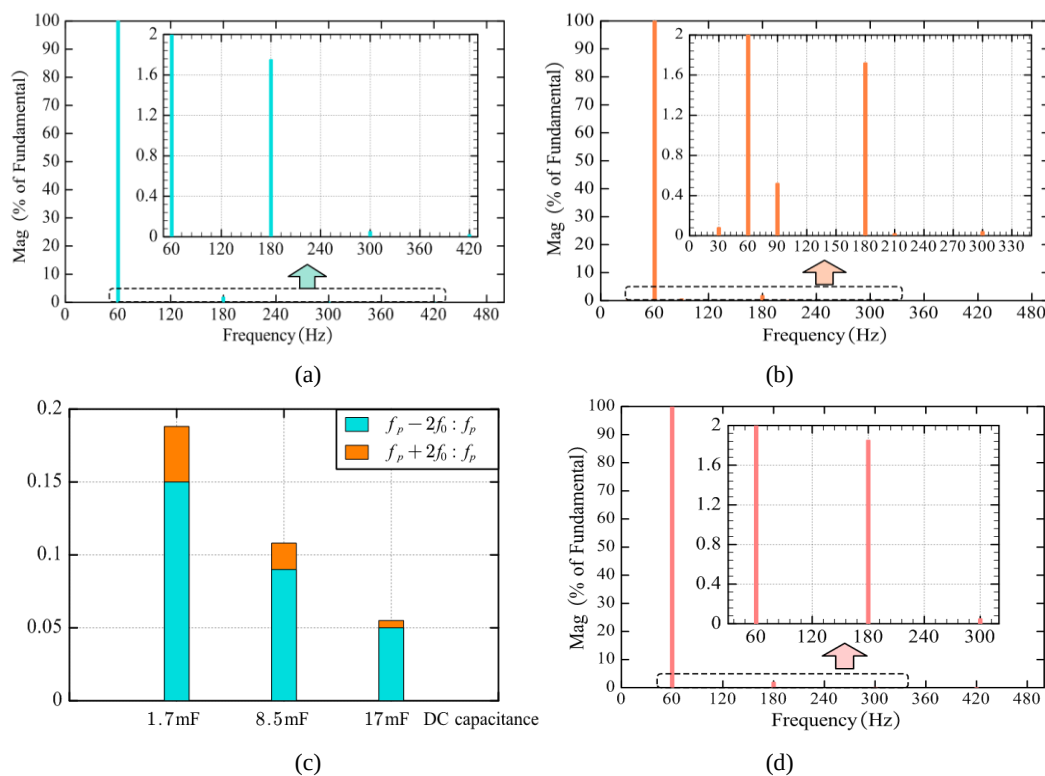


Figure 2-4 (a) Current frequency spectrum without perturbation; (b) Current frequency spectrum with 90Hz perturbation; (c) Current response ratio with different dc capacitance; (d) Current frequency spectrum with 180Hz perturbation

2.3 PFC Impedance Model in the D-Q Frame

In this section, following the modeling method illustrated in Section II, the small-signal impedance model of a PFC converter is derived assuming an operating point at a rated condition. The different control loops and the cascaded dc-dc converter loads' impact are analyzed.

2.3.1 Open-loop Impedance Model

With a time-invariant operating point, the PFC converter d - q model in Figure 2-2 (a) can be linearized, yielding its small-signal model as shown in Figure 2-5. Figure 2-6 shows the linear dynamics with a time-invariant operating point in the d - q frame. Note that the block diagram in Figure 2-6 only includes the parts without the input filter, which are added as the last step when calculating the impedance $\mathbf{Z}_{\text{filter_PFC}}$ in all the following sections using (2-11).

$$\mathbf{Z}_{\text{filter_PFC}} = \left(\mathbf{Y}_{\text{PFC}} + \mathbf{Y}_{\text{C}_e} + \left(\mathbf{Z}_{\text{C}_d} + \mathbf{Z}_{\text{R}_d} \right)^{-1} \right)^{-1} + \mathbf{Z}_{\text{L}_{dm}} \quad (2-11)$$

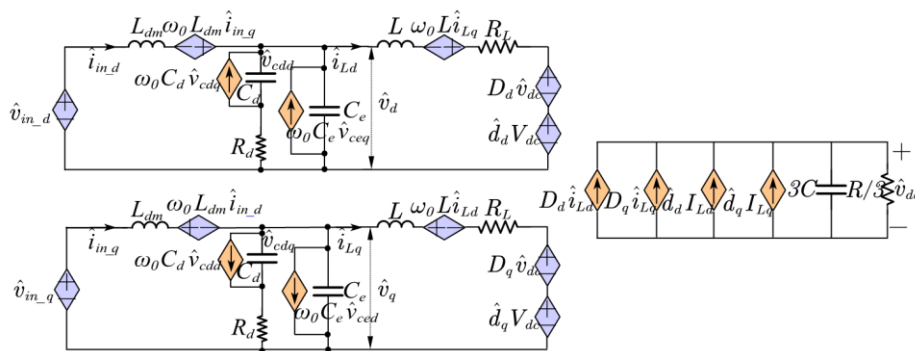


Figure 2-5 Open-loop circuit small-signal model

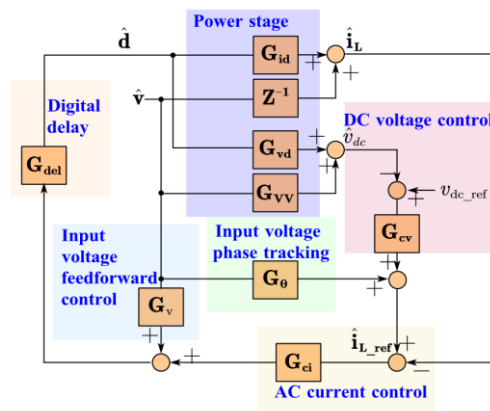


Figure 2-6 PFC converter small-signal model in block diagram

where $\mathbf{Y}_{\text{PFC}}$ is the d-q admittance of the PFC without the input filter, $\mathbf{Y}_{\text{Ce}}$ is the d-q admittance of the cap C_e , $\mathbf{Z}_{\text{Cd}}$, $\mathbf{Z}_{\text{Rd}}$, and $\mathbf{Z}_{\text{Ldm}}$ are the d-q impedance of the cap C_d , resistor R_d , and inductor L_{dm} respectively. The purple shade in Figure 2-6 identifies the power stage dynamics. $\mathbf{G}_{id}$ denotes the transfer function matrix from $\hat{\mathbf{d}}$ to $\hat{\mathbf{i}}_L$, $\mathbf{Z}$ denotes the transfer function matrix from $\hat{\mathbf{i}}_L$ to $\hat{\mathbf{v}}$, $\mathbf{G}_{vd}$ denotes the transfer function matrix from $\hat{\mathbf{d}}$ to $\hat{v}_{dc}$, and $\mathbf{G}_{vv}$ denotes the transfer function matrix from $\hat{\mathbf{v}}$ to $\hat{v}_{dc}$. The open-loop impedance of the PFC converter using the parameters in Table 2-1 is depicted in Figure 2-7, one case is without damping for the input filter, and the other is with damping resistance of 2 Ω . The approximated values of the open-loop impedance in different frequency ranges are shown in Table 2-2.

For Z_{dd} , a resonant point between the boost inductor and dc capacitor exists at around 200 Hz, which is

$$f_r = \frac{1}{2\pi} \cdot V_{ac} / (V_{dc} \sqrt{2LC}) \quad (2-12)$$

For Z_{dd} and Z_{qq} , the resonant points of the filter impedance are at around 6 kHz and 20 kHz respectively. Adding the damping resistor mainly weakens the resonance at f_2 .

$$f_1 = \frac{1}{2\pi} \cdot 1 / \sqrt{LC_{dm}} \quad (2-13)$$

$$f_2 = \frac{1}{2\pi} \cdot 1 / \sqrt{C_{dm} / (1/L + 1/L_{dm})} \quad (2-14)$$

Table 2-2 The four elements of open-loop impedance

Frequency	Z_{dd}	Z_{dq}	Z_{qd}	Z_{qq}
< 1Hz	$V_{ac}^2/(2P)$	-	-	-
< 1kHz	-	$-\omega_0 L$	$\omega_0 L$	sL
> 30kHz	sL_{dm}	$-\omega_0 L_{dm}$	$\omega_0 L_{dm}$	sL_{dm}

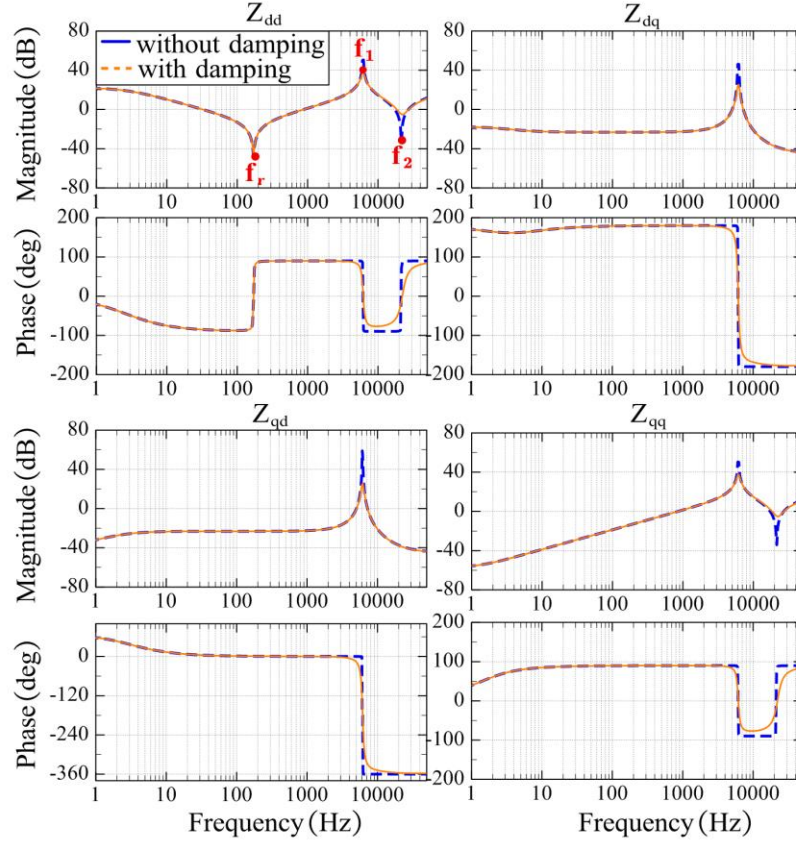


Figure 2-7 Bode plot of small-signal open-loop impedance

2.3.2 Impact of Current Control and Input Voltage Phase Tracking

To identify the current control's impact on the impedance, it is first assumed that the current reference phase is assigned arbitrarily with no perturbation. The blocks highlighted in yellow symbolize the current controller's dynamics in Figure 2-6. The PFC converter impedance is then calculated by (2-15) and (2-16). $\mathbf{T}_i$ is the open-loop gain of the current loop, $\mathbf{G}_{ci}$ denotes the PR controller dynamics defined in (2-6), $\mathbf{G}_{del}$ corresponds to the control delay as shown in (2-17), and T_{del} is estimated as 1.5 times one switching cycle.

$$\mathbf{Z}_{PFC_cu} = \mathbf{Z}(\mathbf{I} + \mathbf{T}_i) \quad (2-15)$$

$$\mathbf{T}_i = \mathbf{G}_{id} \mathbf{G}_{del} \mathbf{G}_{ci} \quad (2-16)$$

$$\mathbf{G}_{del} = \begin{bmatrix} \frac{1 - 0.5sT_{del}}{1 + 0.5sT_{del}} & 0 \\ 0 & \frac{1 - 0.5sT_{del}}{1 + 0.5sT_{del}} \end{bmatrix} \quad (2-17)$$

$\mathbf{G}_\theta$ is defined to represent the dynamics of the input voltage phase tracking, which can be derived as

$$\mathbf{G}_\theta = \begin{bmatrix} I_d/V_d & 0 \\ 0 & I_d/V_d \end{bmatrix} \quad (2-18)$$

To observe the impact of the current control loop and phase tracking on the input impedance, the calculated impedance of three conditions: open-loop, with only current control, with both current control and phase tracking, are shown in Figure 2-8. Compared with the open-loop condition, adding a current loop eliminates the resonance between the dc capacitor and boost inductor at 200 Hz for Z_{dd} , and the resonance between the boost inductor and C_{dm} at 6 kHz in all Z_{dd} , Z_{dq} , Z_{qd} , and Z_{qq} , while the resonance between L_{dm} and C_{dm} at 20kHz is not impacted because only the boost inductor current is controlled. Adding the current loop also results in resonance in four elements at 120 Hz because of the PR controller. Below 1 Hz, the integrator feature of the PR controller is dominant, so a 20 dB/dec gain reduction and -90° phase change can be observed in Z_{dd} and Z_{qq} while adding the input voltage phase tracking eliminates this feature and results in resistor characteristic in Z_{dd} and Z_{qq} within the current loop's bandwidth.

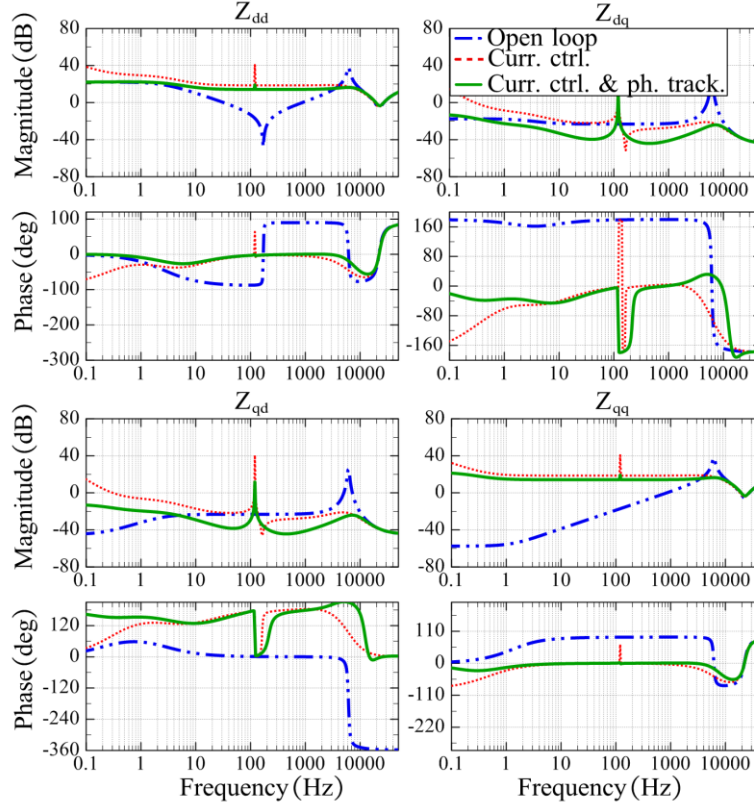


Figure 2-8 Impedance plot: blue: open-loop; red-dotted: with current loop; green-dashed-dotted: with current loop and phase tracking

2.3.3 Impact of the DC Voltage Control

The dc voltage control dynamics are modeled by the blocks shadowed in pink in Figure 2-6, considering which the input impedance is,

$$\mathbf{Z}_{\text{PFC_cu_ph_cv}} = \text{inv} \begin{pmatrix} \mathbf{Z}^{-1} - \mathbf{G}_{\text{id}} \text{inv} (\mathbf{I} + \mathbf{G}_{\text{del}} \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{cv}} \mathbf{G}_{\text{vd}}) \cdot \\ (\mathbf{G}_{\text{del}} \mathbf{G}_{\text{ci}} (\mathbf{G}_{\text{cv}} \mathbf{G}_{\text{vv}} - \mathbf{G}_{\theta})) \\ (\mathbf{I} + \mathbf{G}_{\text{id}} \text{inv} (\mathbf{I} + \mathbf{G}_{\text{del}} \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{cv}} \mathbf{G}_{\text{vd}}) \mathbf{G}_{\text{del}} \mathbf{G}_{\text{ci}}) \end{pmatrix}. \quad (2-19)$$

where $\mathbf{G}_{\text{cv}}$ denotes the voltage controller dynamics.

$$\mathbf{G}_{\text{cv}} = \left(k_{\text{pv}} + \frac{k_{\text{iv}}}{s} \right) \begin{bmatrix} V_{\text{d}}/V_{\text{d}} \\ V_{\text{q}}/V_{\text{d}} \end{bmatrix} \quad (2-20)$$

With (2-19) and (2-20), Figure 2-9 shows the impedance results in four scenarios: with only current control and input voltage phase tracking, also including dc voltage control with different bandwidths ($f_{\text{dc_bw}}$) namely 6 Hz, 15 Hz, and 24 Hz. From Figure 2-9, adding the dc voltage control

mainly impacts Z_{dd} below 100 Hz and Z_{dq} , Z_{qd} because of the d - q frame coupling effects, while Z_{qq} is not affected at all. This is because the d axis is aligned with the original circuit input voltage vector and under the unity power factor control, the ac side power is delivered through the d channel to the dc channel. Most significantly, having the dc voltage control results in a negative resistor characteristic of the Z_{dd} element at the frequency range lower than f_{dc_bw} , with a gain of $|V_d/I_d|$ and a phase of -180° . With the increase of f_{dc_bw} , the negative resistance characteristic maintains a higher frequency, which is unfavorable for system stability. At the frequency range higher than f_{dc_bw} , the impedance characteristics are the same as without the dc voltage control.

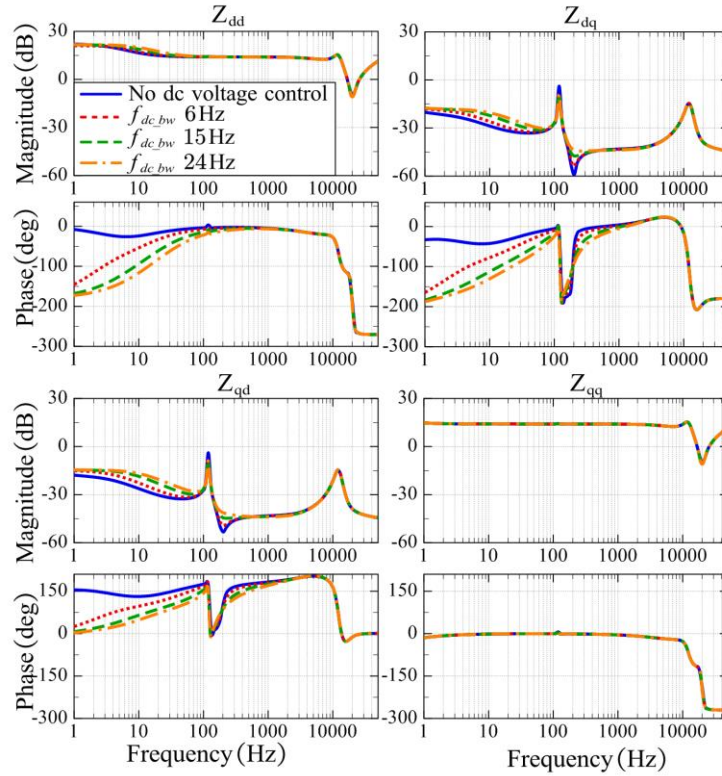


Figure 2-9 Impedance bode plot: blue: no voltage control; red-dotted: $f_{dc_bw} = 6\text{Hz}$; green-dashed: $f_{dc_bw} = 15\text{Hz}$; orange-dashed-dotted: $f_{dc_bw} = 24\text{Hz}$

2.3.4 Impact of Input Voltage Feedforward Controls

To improve the dynamic response of the dc bus voltage to the input voltage variation, an input voltage feedforward control scheme is added by directly feeding the input voltage with a gain of

$1/V_{dc}$ to the duty cycle. The block highlighted in blue in Figure 2-6 describes these added dynamics as,

$$\mathbf{G}_v = \begin{bmatrix} 1/V_{dc} & 0 \\ 0 & 1/V_{dc} \end{bmatrix} \quad (2-21)$$

The input impedance can then be calculated as follows,

$$\mathbf{Z}_{\text{PFC_cu_ph_cv_ff}} = \text{inv} \left(\mathbf{Z}^{-1} - \mathbf{G}_{id} \text{inv} (\mathbf{I} + \mathbf{G}_{del} \mathbf{G}_{ci} \mathbf{G}_{cv} \mathbf{G}_{vd}) \cdot \right. \\ \left. (\mathbf{G}_{del} \mathbf{G}_{ci} (\mathbf{G}_{cv} \mathbf{G}_{vv} - \mathbf{G}_\theta) - \mathbf{G}_{del} \mathbf{G}_v) \right) (\mathbf{I} + \mathbf{G}_{id} \text{inv} (\mathbf{I} + \mathbf{G}_{del} \mathbf{G}_{ci} \mathbf{G}_{cv} \mathbf{G}_{vd}) \mathbf{G}_{del} \mathbf{G}_{ci}) \quad (2-22)$$

There are also other kinds of input voltage feedforward control schemes used in many PFC applications. Scheme 2 is shown in Figure 2-10 (a) [29], with the input voltage RMS value monitored and fed into the current controller reference value. Scheme 3 is shown in Figure 2-10 (b) [33], [34]. By estimating and canceling the double-line frequency ripples of the dc voltage signal, the dc voltage loop bandwidth can be increased. The double-line frequency ripples can be estimated using

$$f(v_{ac}) = \frac{P}{2\omega_0 CV_{dc}} \cos\left(2\omega_0 t + \frac{\pi}{2}\right) = \frac{P}{2\omega_0 CV_{dc}} \left(1 - 2\left(\frac{v_{ac}}{|V_{ac}|}\right)^2\right) T_{\frac{\pi}{2}} \quad (2-23)$$

The impedance bode plot without and with the three kinds of input voltage feedforward control schemes are plotted in Figure 2-11. For Scheme 3, the dc voltage loop bandwidth is increased to around 100 Hz while for the other three scenarios, it is kept at 6 Hz. Figure 2-11 shows the negative resistor behavior of the Z_{dd} term extends to higher frequencies after adding the input voltage feedforward control, and the increase is larger with Scheme 2 and more so with Scheme 3. The negative impedance characteristic extending to a higher frequency range could be potentially detrimental to system stability.

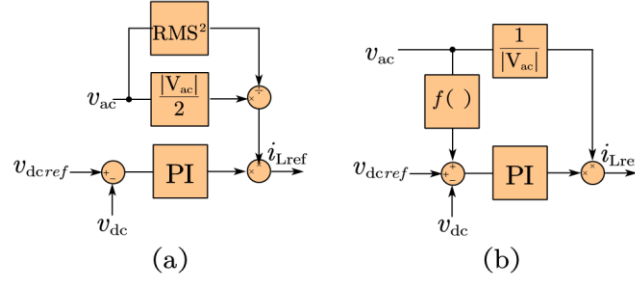


Figure 2-10 Input voltage feedforward control (a) Scheme 2 (b) Scheme 3.

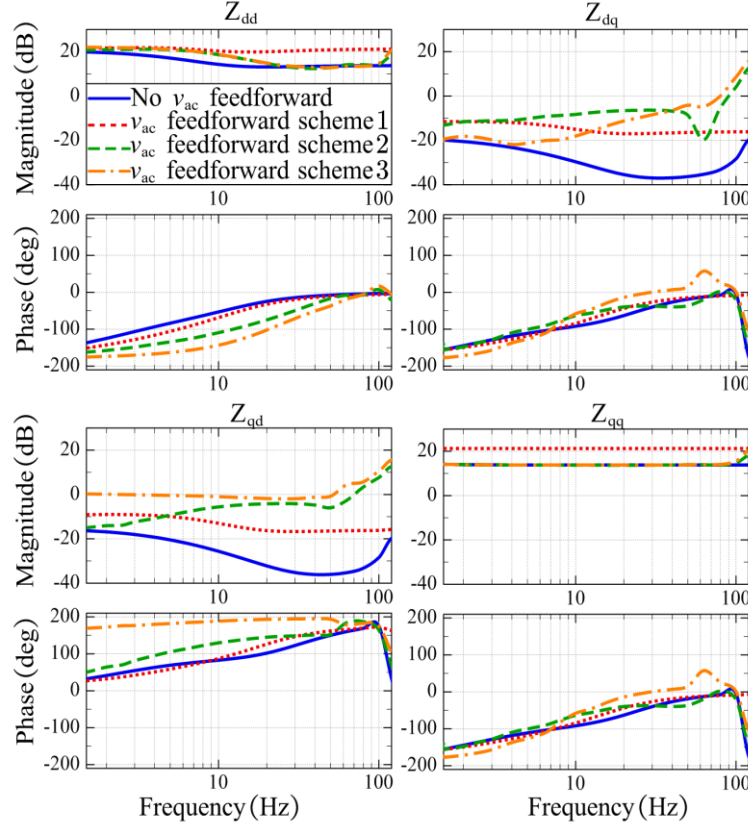


Figure 2-11 Impedance with different input voltage feedforward controls.

2.3.5 Impact of the Cascaded DC-DC Converter Load

The previous sections all assume a resistor load for the PFC converter. Since a PSU is composed of an ac-dc PFC converter and a cascaded dc-dc converter, this section aims to analyze the dc-dc converter's impact on the front-end PFC converter impedance. Generally for such applications, the dc-dc converter utilizes an LLC resonant converter topology to provide isolation. Ref. [35] shows that the LLC input impedance can be modeled as a negative resistor up to the voltage loop

bandwidth of the converter, which is similar to a buck converter. Figure 2-12 shows the PFC converter impedance with resistor load R , negative resistor load $-R$, and dc-dc converter load, all with the same power consumption. The dc-dc converter load utilizes a generic buck converter with a switching frequency of 100 kHz, a current control loop bandwidth of 10 kHz, and a dc voltage loop bandwidth of 1 kHz. The overlap of the orange and green dotted curves shows that using a negative resistor load can represent the dynamics of the dc-dc converter load in the whole frequency range when modeling the PFC converter input impedance.

Compared with a resistor load, having a negative resistor load mainly results in a gain and phase reduction at 2 Hz to 10 Hz for Z_{dd} . Generally, the gain and phase reduction of Z_{dd} at low frequency is more detrimental to system stability.

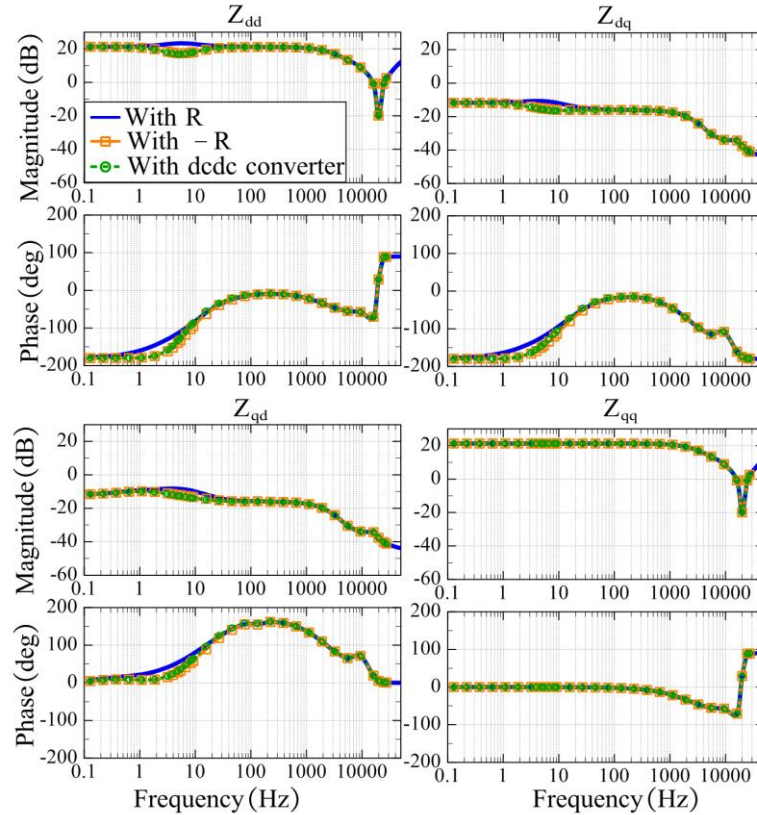


Figure 2-12 PFC converter impedance with a resistor and dc-dc converter loads.

2.3.6 Comparison of CCM and TCM operation

The previous sections assume a CCM mode operation. There are other types of operation modes, such as Triangle Mode Operation (TCM). A simulation study was carried out to compare the impedance results of PFC in CCM and TCM operations. The TCM is implemented following [2]. Figure 2-13 shows the Z_{dd} and Z_{qq} under CCM and TCM operations. It shows that the impedance characteristics of the two modes are similar in the low-frequency range, and the difference lies in the high frequency impedance. Under TCM mode, the converter has a higher equivalent current loop bandwidth, and has an input filter with a higher cutoff frequency, due to the higher inductor current ripples. Therefore, the blue curve has a higher resonant point than the orange curve for both the Z_{dd} and Z_{qq} terms.

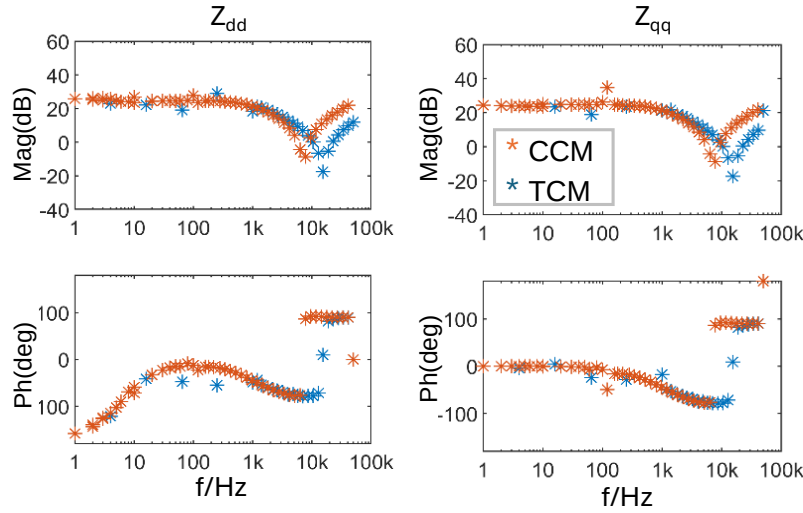


Figure 2-13 Comparison of Z_{dd} and Z_{qq} for CCM and TCM operations.

2.4 Experimental Validation of PFC Impedance Model

Several Silicon Carbide MOSFET-based single-phase PFC converters are built. They have the same topology, control design, and parameters as in Figure 2-1 and Table 2-1. A few commercial PSUs with part number FLATPACK2 241119. 905B are also tested. Figure 2-14 shows the experimental setup.

2.4.1 DQ Impedance Measurement Methods

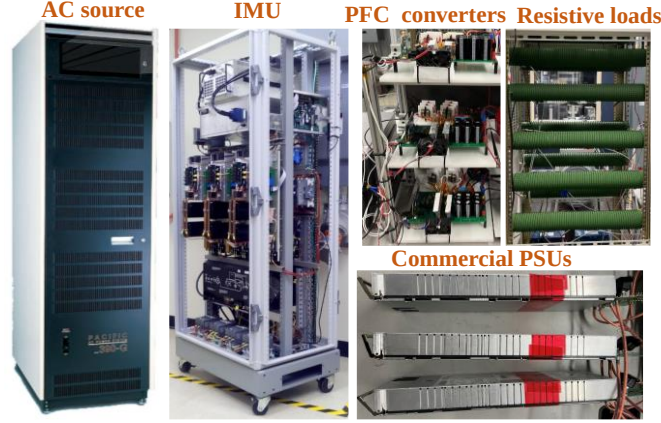


Figure 2-14 Experimental setup of impedance measurement.

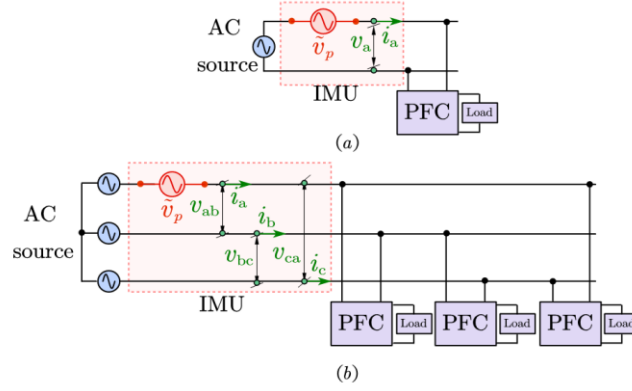


Figure 2-15 Impedance measurement setup (a) Single-phase (b) Three-phase

A single-phase measurement setup configuration is shown in Figure 2-15 (a). The IMU is connected between the source and the PFC converter while injecting a voltage perturbation in series with the circuit. The PFC converter voltage response v_a and current response i_a are measured. Then $\pm 120^\circ$ phase shifts are applied to the v_a and i_a data so the other two sets of data in frame B and frame C are created. By aligning the d axis with v_a , the three-phase voltage and current vectors are transformed into the $d-q$ frame, with which the $d-q$ impedance is then calculated. A three-phase measurement setup configuration is shown in Figure 2-15 (b). Three PFC converters with the same parameters are connected to a three-phase ac source, and the IMU in series with the circuit injects a single-phase voltage perturbation. The PFC converter side three-phase voltage and current response are measured and processed. By aligning the d frame with v_{ab} , and performing

Park's transform for the measured voltage and current variables, the d - q impedance can be extracted. It is hereby stated that these two kinds of methods are equivalent thus producing the same result. This is because the single-phase method utilizes the single-phase response to virtually create the two other phase responses and transform the data into the d - q frame, while the three-phase method obtains the three-phase response by measurement. Ideally, if the three PFC converters are the same, the small-signal model of the three-phase setup is equivalent to the single-phase setup with virtual frames. As an example, the impedance measurement results of the single-phase commercial PSU load using the two methods are shown in Figure 2-16, which are very close to each other.

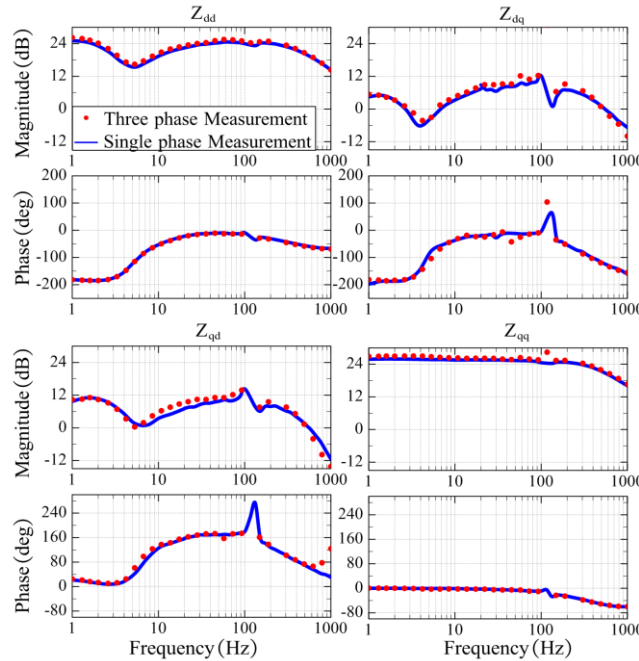


Figure 2-16 Comparison between single-phase and three-phase measurement

2.4.2 Impedance Experimental Validation

The impedance results shown in this section for both the PFC converter and PSU are obtained using the single-phase measurement setup shown in Figure 2-15 (a).

Figure 2-16 shows the PFC converter measured impedance at around $235V_{\text{rms}}$, $375V_{\text{dc}}$, 4.2kW , and the modeling results at the same operating point using the model in Section 2.3, which match well except for around 120 Hz given the presence of the dc-bus double line-frequency ripples that

induce the ac side third harmonics through frequency coupling, mixing the small-signal response and operating point response, as was explained in Section 2.2.2. The mismatch in Z_{dq} and Z_{qd} mainly results from the system error because the off-diagonal terms are too small. Another important point is that this mismatch is also not critical because the PFC converter impedance is diagonally dominant, and the off-diagonal terms have a negligible effect on the minor loop gain construction.

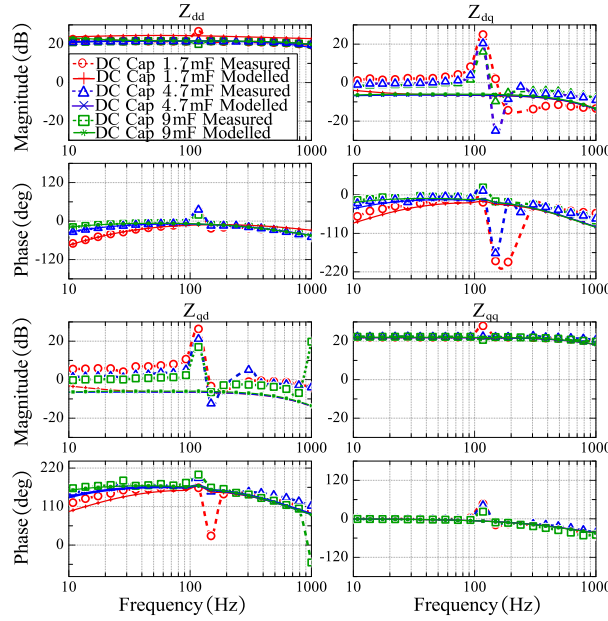


Figure 2-17 Modeled and measured impedance with different dc capacitance.

Figure 2-17 shows the PFC converter impedance modeling and measurement results with different dc capacitance values. As was analyzed, with a higher dc capacitor value and smaller dc-bus voltage ripples, the resulting power stage ac side third harmonics are lower, therefore the modeling result matches the measurement results better.

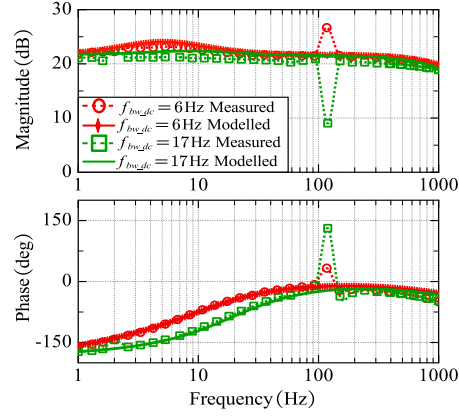


Figure 2-18 Modeled and measured Z_{dd} with different dc voltage loop bandwidths.

Figure 2-18 shows the PFC converter measurement and modeling results of the Z_{dd} element with 6 Hz and 17 Hz dc voltage-loop bandwidths. As analyzed, an increase in the dc voltage loop bandwidth extends the frequency range of negative impedance characteristic of Z_{dd} , which is potentially detrimental to the system stability. The measurement results matched well the modeling results thus verifying this analysis. Also, with the increase of dc voltage bandwidth, the amount of dc voltage double line-frequency ripples propagating to the current reference is larger and the resulting power stage ac side third harmonics are higher, the modeling results deviate further from the measurement results at 120 Hz.

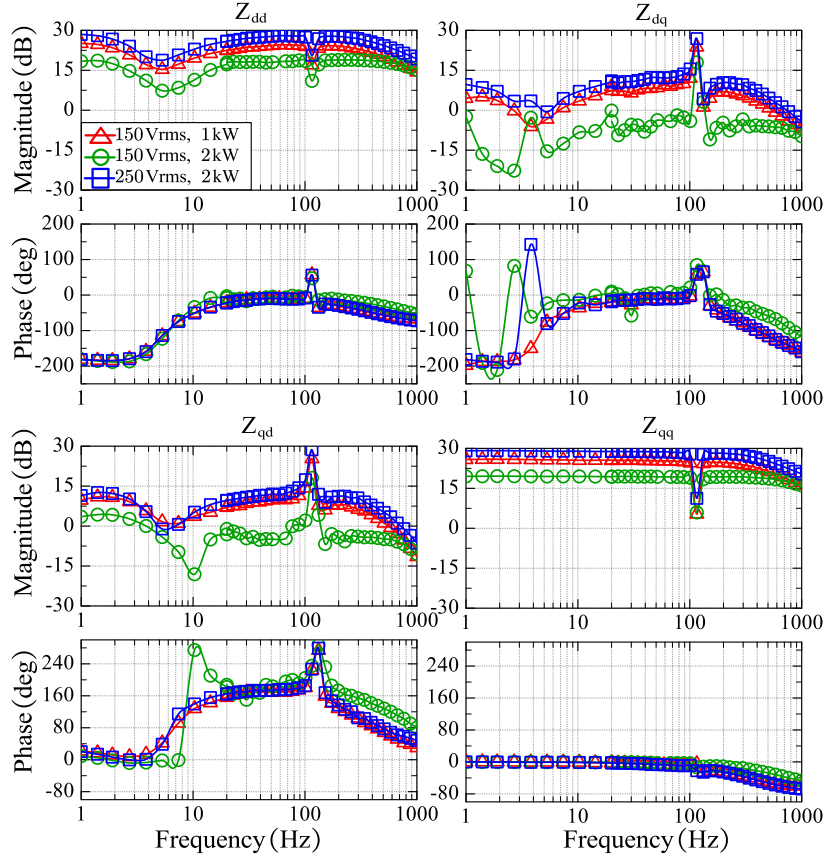


Figure 2-19 Commercial PSU input impedance at different power and voltage

Figure 2-19 shows the measurement results of the commercial PSU which contains a PFC and a cascaded dc-dc converter load. The output dc voltage is regulated at 55 V. The measurements are conducted at three operating points: 150 V_{rms}, 1 kW; 150 V_{rms}, 2 kW; 250 V_{rms}, 2 kW. Comparing the red and green curves, with the same input voltage, increasing power results in a reduction of impedance gain, which is prone to result in an impedance interaction between the PSU loads and the source. Comparing the green and blue curves, with the same power, reducing the input voltage results in a reduction of impedance gain and is more likely to cause dynamic interaction between the PSU load and its ac source. Compared with the impedance shown in Figure 2-18 for a PFC with resistor load, the PSU load impedance has a gain reduction at a few hertz for Z_{dd} , Z_{dq} , and Z_{qd} , matching the analysis in Section 2.3.5, which is due to the negative resistance characteristic of the dc-dc converter.

2.5 Summary and Conclusions

This chapter models the small-signal impedance of a single-phase PFC converter in the virtual d - q frame. Some important features of the PFC impedance are discussed. The examples show how the proposed model can be used to predict the stability of a system with single-phase loads. Some useful conclusions are drawn as follows.

- 1) The d - q frame impedance model for the single-phase PFC converter is accurate enough and can be extended to other PFCs with different topologies. The time-invariant system approximation is reasonable because it can cover all important dynamics.
- 2) The PFC's dc voltage controller results in the negative resistor characteristic of the PFC impedance Z_{dd} term, and the cascaded dc-dc converter's negative resistance characteristic reduces the gain and phase of the PFC impedance Z_{dd} term at low frequency. Both could be detrimental to system stability.

2.6 Reference List of Chapter 2

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Chapter 3

Impedance-based Stability Assessment of AC Systems with Single-phase PSUs

3.1 Introduction

Researchers have developed various impedance-based approaches for AC system stability analysis, including the sequence impedance approach, the d-q impedance method, and the dynamic phasors method, etc. These methods have been used to model and study three-phase balanced converter systems, such as the voltage source converter [1] - [3].

The above-mentioned methods have also been applied to model other types of systems, such as single-phase systems and three-phase unbalanced systems. For instance, Ref. [4], Ref. [5], and Ref. [6] employed the sequence impedance concept to model and analyze the stability of systems with single-phase converters. Based on d-q domain analysis, Ref. [7] — Ref. [10] created virtual frames for single-phase loads and transformed the artificial ‘balanced three-phase systems’ into their virtual d-q frames to obtain DC operating points and conduct small-signal analysis.

A three-phase four-wire system is another type of system that cannot always be analyzed using techniques applicable to a balanced three-phase three-wire system. This is due to the presence of non-negligible neutral line impedance, possible unbalanced conditions, and single-phase load dynamics. While Ref. [4] analyzed the stability of such a system using sequence impedance, it may be difficult for some engineers and students to understand the time-periodic framework, since it may involve challenging concepts such as frequency domain linearization, exponentially modulated periodic signals, etc [11]. Therefore, investigating the possibility of analyzing such systems’ stability in a linear-time-invariant (LTI) framework is desirable. The virtual frame concept, which is used for single-phase converter modeling to achieve a time-invariant system, holds promise for this purpose. When there is no neutral line impedance in the four-wire system, the three phases of the four-wire system can be treated as independent single-phase systems since

they are wholly decoupled. However, modeling the system becomes challenging when there are non-negligible neutral impedances.

Some literature has addressed three-phase four-wire converter. Ref. [12] and Ref. [13] designed the current control of an unbalanced three-phase four-wire voltage source converter by creating virtual circuits of each phase. Ref. [14] utilized the dq0 modeling method for an unbalanced four-wire converter, but its effectiveness for four-wire systems with single-phase loads is uncertain due to the differing DC bus dynamics of the loads among the three phases.

This section utilizes single-phase PSU impedance developed in Chapter 2, developing a virtual dq-frame-based system model for the scenarios when such PSUs are presented in a single-phase system configuration, three-phase three-wire system configuration, and three-phase four-wire system configuration. These models enable the modeling and analysis of different PSU systems in a time-invariant framework.

3.2 Single-phase System

3.2.1 System Model

A single-phase system shown in Figure 3-1 composed of a single-phase ac source with line impedance and a PSU load is studied. Following the virtual d-q frame impedance modeling method shown in Section 2 for a single-phase PSU load, the d-q frame impedance of the grid side Z_g can also be modeled as (3-1)

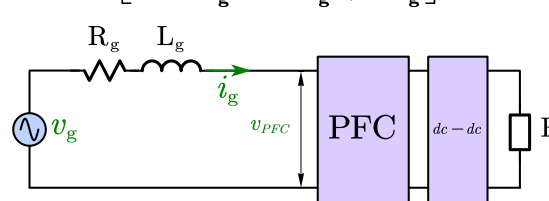
$$\mathbf{Z}_g = \begin{bmatrix} R_g + sL_g & -\omega L_g \\ \omega L_g & R_g + sL_g \end{bmatrix} \quad (3-1)$$


Figure 3-1 Single-phase system configuration

The system minor loop gain $\mathbf{L}$ is,

$$\mathbf{L} = \mathbf{Z}_g \mathbf{Y}_{\text{PSU}} \quad (3-2)$$

which is a 2-by-2 matrix since both $\mathbf{Z}_g$ and $\mathbf{Y}_{psu}$ are second-order matrices. Accordingly, the Nyquist diagram of this interface has two characteristic loci, which are simply the trajectories described by the two eigenvalues of $\mathbf{L}$ in the complex plane when the frequency variable “s” traverses the standard Nyquist contour.

3.2.2 Experimental Verification

To verify the effectiveness of using (3-2)**Error! Reference source not found.** for the single-phase system stability analysis, two experimental cases are tested. The PSU is with part number FLATPACK2 241119. 905B, which is operated at 2.5 kW using an electronics load and with an input voltage of 152 Vrms. The Pacific Power AC source working in single-phase mode emulates the single-phase grid. Some inductors and resistors are inserted in between the PSU load and the ac source as the line impedance, the parameters of which are shown in Table 3-1.

Table 3-1 Grid Impedance Parameters

No. Case	R_g	L_g
1	2Ω	8.6mH
2	2Ω	12.9mH

To calculate the eigenvalues of the minor loop gain, the PSU load impedance is measured using the single-phase impedance measurement setup introduced in Section 2.4. The test waveforms and the Nyquist plot of Case 1 are shown in Figure 3-2. The time-domain results show a stable operation. At the same time, there are no encirclements of $(-1, 0)$ in the Nyquist plot.

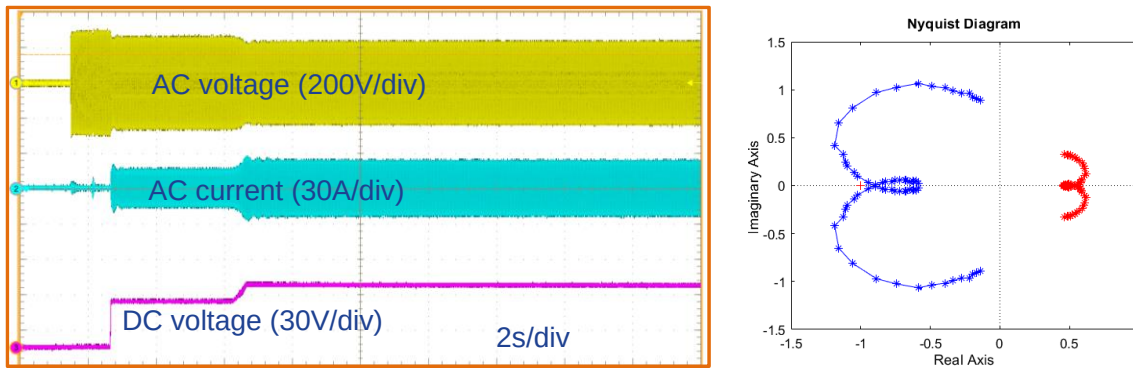


Figure 3-2 Case 1 time-domain test results and Nyquist Plot.

The test waveforms and the Nyquist plot of Case 2 are shown in Figure 3-3. The time-domain results exhibit low-frequency oscillations at around 2.7 Hz after the PSU input voltage decreased to the studied operating point 152Vrms. Correspondingly, there are two encirclements of the critical point (-1, 0) in the Nyquist plot in the vicinity of 2.8 Hz.

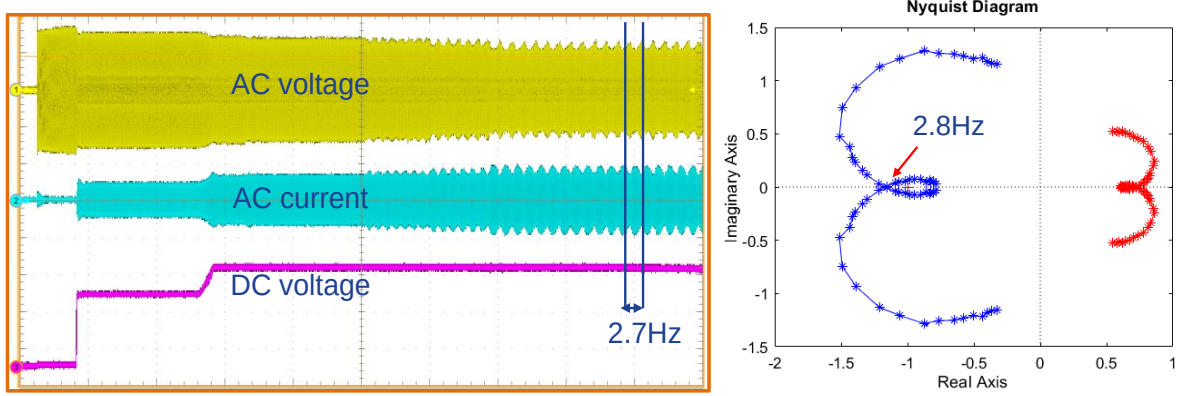


Figure 3-3 Case 2 time-domain test results and Nyquist Plot.

The above results and analysis verify both the PSU d-q impedance model and the single-phase system minor loop gain model. Therefore, such a virtual d-q frame modeling approach can be extended to other single-phase systems for stability analysis purposes.

3.2.3 Discussion on system with source impedance with low X/R ratio

The case demonstrations are with high grid impedance X/R ratio. For medium or high-voltage transmission, the grid impedance X/R is large to help reduce power losses [14]. Ref. [15] and Ref. [16] show low-frequency small-signal instability cases for a medium-voltage drive system. The discussion below is intended for a low-voltage distribution system where the grid side X/R ratio is relatively small.

Using the virtual *d-q* frame modeling method illustrated in Section 2, the system operating point in the *d-q* frame can be calculated using (3-3)~(3-5) when aligning the Park transform angle with φ_{PFC} and under unity power factor operation.

$$V_{gd} = I_{gd}R_g + V_{PFCd} \quad (3-3)$$

$$V_{gq} = \omega_0 L_g I_{gd} \quad (3-4)$$

$$3P = V_{PFCd} I_{gd} \quad (3-5)$$

The voltage vectors have the following relationship. V_g is the magnitude of v_g .

$$\frac{3}{2} V_g^2 = V_{gd}^2 + V_{gq}^2 = (V_{PFCd} + R_g I_{gd})^2 + (\omega_0 L_g I_{gd})^2 \quad (3-6)$$

which can be simplified as a second-order equation of I_{gd}^2 ,

$$(R_g^2 + \omega_0^2 L_g^2) (I_{gd}^2)^2 + \frac{3}{2} (4PR_g - V_g^2) I_{gd}^2 + 9P^2 = 0 \quad (3-7)$$

which only has a solution on the following condition,

$$(4PR_g - V_g^2)^2 - 16P^2 (R_g^2 + \omega_0^2 L_g^2) \geq 0 \quad (3-8)$$

yielding (3-9) since $R_g < V_g^2/4P = Z_{base}/2$

$$R_g + \sqrt{R_g^2 + \omega_0^2 L_g^2} \leq \frac{V_g^2}{4P} = \frac{V_{g_rms}^2}{2P} = \frac{1}{2} Z_{base} \quad (3-9)$$

If the grid impedance is too large and not satisfying (3-9), the input voltage of the PFC will be too low to operate, so the system will not have an operating point. Since an operating point is the foundation of small-signal analysis, the grid impedance should be limited by (3-9) in this study.

The interface for stability analysis is chosen at the input of the PFC converter. The grid side impedance in the d - q frame is

$$\mathbf{Z}_g = \begin{bmatrix} R_g + sL_g & -\omega_0 L_g \\ \omega_0 L_g & R_g + sL_g \end{bmatrix} \quad (3-10)$$

The PFC converter admittance in the d - q frame is denoted as $\mathbf{Y}_{PFC}$. The system stability can then be assessed using the following return ratio according to GNC.

$$\mathbf{L}_{sys} = \mathbf{Z}_g \cdot \mathbf{Y}_{PFC} \quad (3-11)$$

The PFC impedance shown in Figure 2-16 is diagonally dominant, and so is $\mathbf{Y}_{PFC}$. Different from other PLL-based grid-tied inverters, the negative resistance characteristic of the PFC converter impedance is caused by the dc voltage control with a relatively lower bandwidth. In the mid-frequency range (60 Hz~1 kHz) both Z_{dd} and Z_{qq} appear to be a resistor, which is very stable for any kind of source, so the stability study is conducted in the low-frequency range (< 60 Hz).

For a low voltage distribution system, the line X/R ratio is small, so at low frequency, Z_{gdd} and Z_{gqq} can be approximated as R_g and the grid impedance is also diagonally dominant; hence the minor loop gain can be approximated as (3-12),

$$\mathbf{L}_{\text{sys}} \approx \begin{bmatrix} Z_{gdd} Y_{\text{PFCdd}} & 0 \\ 0 & Z_{gqq} Y_{\text{PFCqq}} \end{bmatrix} \quad (3-12)$$

The multi-input-multi-output (MIMO) system stability analysis can then be simplified to two SISO systems. Further, since both Z_{gqq} and Z_{PFCqq} are resistive and inherently stable, it is only necessary to analyze the $Z_{gdd}Y_{\text{PFCdd}}$ term [13]. A case study is conducted. The single-phase grid voltage is 240 V_{rms}. Table 3-2 shows the line impedance and actual PFC input voltages. Figure 3-4 shows the Z_{PFCdd} term of the PFC converter and the Z_{gdd} term of the different grid impedance. The PFC and grid impedance gain curves only have an intersection when the grid impedance is relatively large (> 0.3 p. u.), which cannot happen in practice because the system may collapse according to (3-9). In addition, the phase difference is much smaller than 180° where the gain curves may intersect; therefore, low-frequency small-signal instability is not likely to occur in such a system before the system collapses.

The time-domain simulation results of the four cases are shown in Figure 3-5. Case 1 to Case 3 are all stable and operate normally, while the voltage of Case 4 collapses. To avoid the system collapsing, the grid impedance should be limited as illustrated in (3-9). Case 1 ~ Case 3 satisfies the (3-9) while Case 4 does not meet (3-9), which is the reason why the system collapses for Case 4. This collapsing is not a small-signal instability, but a large-signal operating point issue.

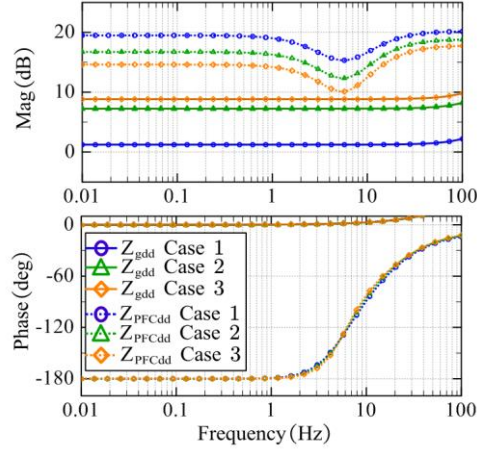


Figure 3-4 DD element of the grid and PFC impedance at low frequency

Table 3-2 Line impedance parameters

No. Case	Case1	Case2	Case3	Case4
L_g	917 μH	1.8 mH	2.2 mH	2.56 mH
R_g	1.152 Ω	2.304 Ω	2.76 Ω	3.23 Ω
Total Z_g	0.117 p.u.	0.233 p.u.	0.28 p.u.	0.33 p.u.
V_{PFC}	307 V	262 V	232 V	Collapse

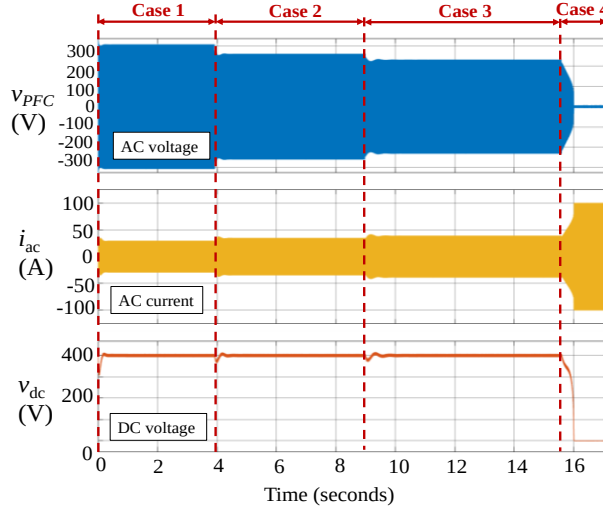


Figure 3-5 Time-domain simulation waveforms of the four cases

The stability analysis of a balanced three-phase three-wire system is like that of the single-phase system showcased in this section, so similar conclusions can be drawn for a such system.

3.3 Three-phase-three-wire system

3.3.1 System Model

A three-phase three-wire system shown in Figure 3-6 is studied. The interface for analysis is chosen to be the input terminal of three PSU converters.

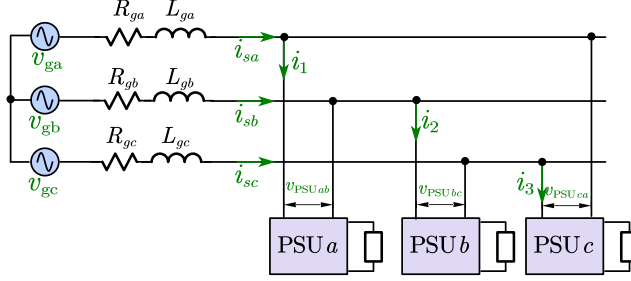


Figure 3-6 Three-phase three-wire configuration

Following the modeling method in Figure 3-6 is considered as in phase X, i.e., phase ab's equation is,

$$v_{PSUabX} = v_{gabX} - Z_{ga} i_{saX} + Z_{gb} i_{sbX} \quad (3-13)$$

The other two virtual frames Y and Z are created by 120° and -120° phase shifts, so the phase ab branch's equation in frame Y and Z are described as,

$$v_{PSUabY} = v_{gabY} - Z_{ga} i_{saY} + Z_{gb} i_{sbY} \quad (3-14)$$

$$v_{PSUabZ} = v_{gabZ} - Z_{ga} i_{saZ} + Z_{gb} i_{sbZ} \quad (3-15)$$

$$i_{saX} = i_{1X} - i_{3X} \quad (3-16)$$

Since (3-13)~(3-16) are balanced in frames X, Y, and Z, by aligning Park transform angle with v_{PSUabX} , the phase ab model in the virtual d - q frame can be derived as follows,

$$\begin{bmatrix} v_{PSUabd} \\ v_{PSUabq} \end{bmatrix} = \begin{bmatrix} v_{gab d} \\ v_{gab q} \end{bmatrix} - \mathbf{Z}_{ga} \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} + \mathbf{Z}_{gb} \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} \quad (3-17)$$

$$\begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} = \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} - \begin{bmatrix} i_{3d} \\ i_{3q} \end{bmatrix} \quad (3-18)$$

Similarly, the phase bc model in the virtual d - q frame can be derived as follows,

$$\begin{bmatrix} v_{PSUbcd} \\ v_{PSUbcq} \end{bmatrix} = \begin{bmatrix} v_{gbc d} \\ v_{gbc q} \end{bmatrix} - \mathbf{Z}_{gc} \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} - (\mathbf{Z}_{gb} + \mathbf{Z}_{gc}) \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} \quad (3-19)$$

$$\begin{bmatrix} \dot{i}_{sbd} \\ \dot{i}_{sbq} \end{bmatrix} = \begin{bmatrix} \dot{i}_{2d} \\ \dot{i}_{2q} \end{bmatrix} - \begin{bmatrix} \dot{i}_{1d} \\ \dot{i}_{1q} \end{bmatrix} \quad (3-20)$$

After linearization, the small-signal relationships are,

$$\begin{bmatrix} \hat{v}_{PSUabd} \\ \hat{v}_{PSUabq} \end{bmatrix} = -\mathbf{Z}_{ga} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \mathbf{Z}_{gb} \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} \quad (3-21)$$

$$\begin{bmatrix} \hat{v}_{PSUbcd} \\ \hat{v}_{PSUbcq} \end{bmatrix} = -\mathbf{Z}_{gc} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} - (\mathbf{Z}_{gb} + \mathbf{Z}_{gc}) \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} \quad (3-22)$$

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} = (\mathbf{Y}_{PSUa} + \mathbf{Y}_{PSUc}) \begin{bmatrix} \hat{v}_{PSUabd} \\ \hat{v}_{PSUabq} \end{bmatrix} + \mathbf{Y}_{PSUc} \begin{bmatrix} \hat{v}_{PSUbcd} \\ \hat{v}_{PSUbcq} \end{bmatrix} \quad (3-23)$$

$$\begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} = \mathbf{Y}_{PSUb} \begin{bmatrix} \hat{v}_{PSUbcd} \\ \hat{v}_{PSUbcq} \end{bmatrix} - \mathbf{Y}_{PSUa} \begin{bmatrix} \hat{v}_{PSUabd} \\ \hat{v}_{PSUabq} \end{bmatrix} \quad (3-24)$$

The d-q average model and small-signal model are shown in Figure 3-7 (a) and (b), (c) and (d) respectively.

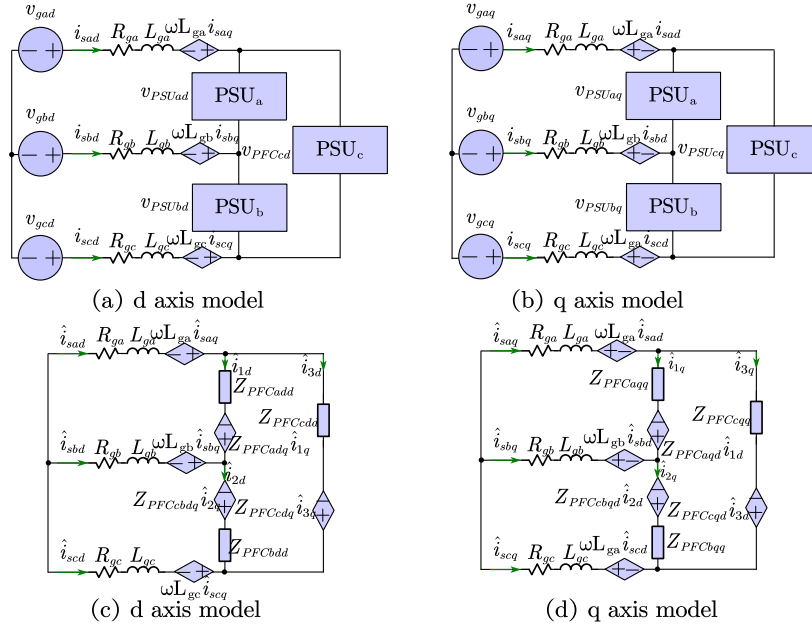


Figure 3-7 Average model ((a), (b)) and small-signal model ((c), (d)) in the d-q frame of the artificial system

From (3-21)~(3-24), the source and load side impedance for such a system are,

$$\mathbf{Z}_{\text{source}} = \begin{bmatrix} \mathbf{Z}_{ga} & -\mathbf{Z}_{gb} \\ \mathbf{Z}_{gc} & \mathbf{Z}_{gb} + \mathbf{Z}_{gc} \end{bmatrix} \quad (3-25)$$

$$\mathbf{Y}_{\text{load}} = \begin{bmatrix} \mathbf{Y}_{PSUa} + \mathbf{Y}_{PSUc} & \mathbf{Y}_{PSUc} \\ -\mathbf{Y}_{PSUa} & -\mathbf{Y}_{PSUb} \end{bmatrix} \quad (3-26)$$

Since $\mathbf{Z}_{ga}$, $\mathbf{Z}_{gb}$, $\mathbf{Z}_{gc}$, $\mathbf{Y}_{PSUa}$, $\mathbf{Y}_{PSUa}$, $\mathbf{Y}_{PSUc}$ are all 2-by-2 matrixes, $\mathbf{Z}_{source}$ and $\mathbf{Y}_{load}$ are 4-by-4 matrixes. The expressions of $\mathbf{Z}_{ga}$, $\mathbf{Z}_{gb}$, and $\mathbf{Z}_{gc}$ are shown in (3-27). The $\mathbf{Y}_{PSUa}$, $\mathbf{Y}_{PSUa}$, and $\mathbf{Y}_{PSUc}$ are the single-phase d-q impedance of each PSU referring to the vector v_{PSUab} .

$$\begin{cases} \mathbf{Z}_{ga} = \begin{bmatrix} R_{ga} + sL_{ga} & -\omega L_{ga} \\ \omega L_{ga} & R_{ga} + sL_{ga} \end{bmatrix} \\ \mathbf{Z}_{gb} = \begin{bmatrix} R_{gb} + sL_{gb} & -\omega L_{gb} \\ \omega L_{gb} & R_{gb} + sL_{gb} \end{bmatrix} \\ \mathbf{Z}_{gc} = \begin{bmatrix} R_{gc} + sL_{gc} & -\omega L_{gc} \\ \omega L_{gc} & R_{gc} + sL_{gc} \end{bmatrix} \end{cases} \quad (3-27)$$

3.3.2 Experimental Verification

To verify the stability analysis models in (3-25) and (3-26) developed, four tests are carried out using an experimental setup configured as Figure 3-6. The Pacific Power ac source in its three-phase mode is used to emulate the three-phase grid. A few resistors and inductors are inserted in between the ac source and the PSU loads. For such a scenario, the 4-by-4 matrix model is used. The parameters of the four cases are shown in Table 3-3.

Table 3-3 Grid impedance and power level parameters of the four cases.

Case	Source impedance	Phase a Power	Phase b Power	Phase c Power
1	1Ω	2.5kW		
2	1Ω+4.3mH	2.5kW		
3	1Ω	2.1kW	2.5kW	2.3kW
4	1Ω+4.3mH	2.1kW	2.5kW	2.3kW

The time-domain tests and the Nyquist plots derived using the source and each PSU's impedance based on the 4-by-4 matrix models are shown in Figure 3-9 ~ Figure 3-12 respectively. Case 1 and Case 2 are both three-phase balanced, while Case 3 and Case 4 both have a 10% unbalanced level. Case 1 and Case 2 are both three-phase balanced, while Case 3 and Case 4 both have a 10 % unbalanced level. Case 1 and Case 3 are stable in the time domain, with no encirclements shown in their Nyquist plots, and Case 2 and Case 4 are unstable with around 3Hz oscillations and two encirclements of (-1, 0) in their Nyquist plots.

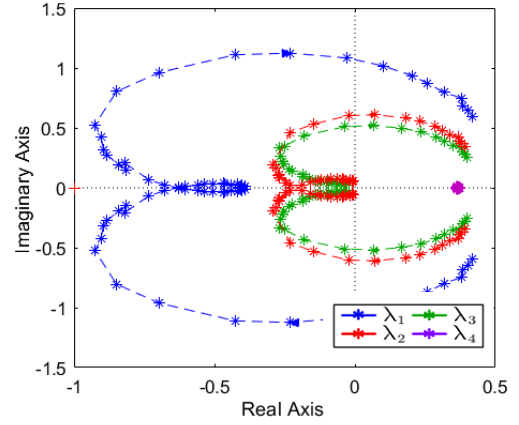
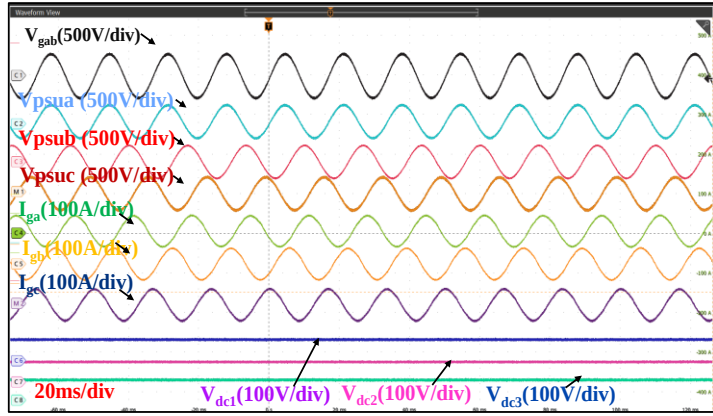


Figure 3-8 (1)Time-domain waveforms, and (2) Nyquist Diagram of Case 1.

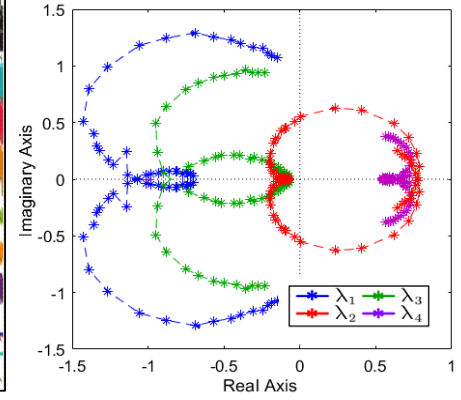
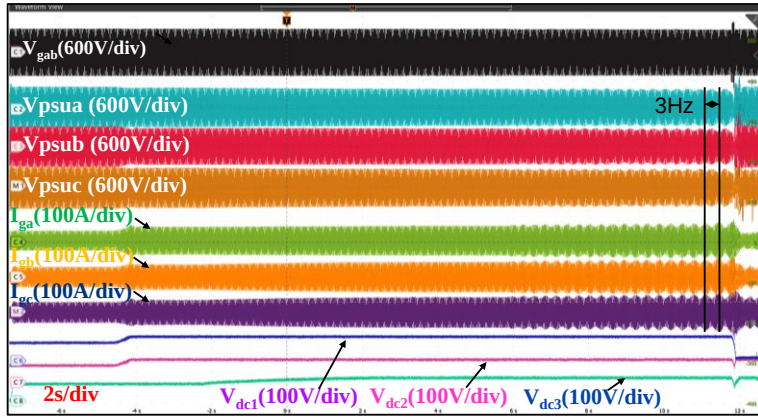


Figure 3-9 (1)Time-domain waveforms, and (2) Nyquist Diagram of Case 2.

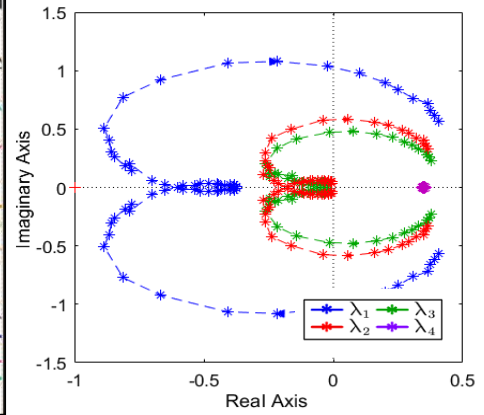
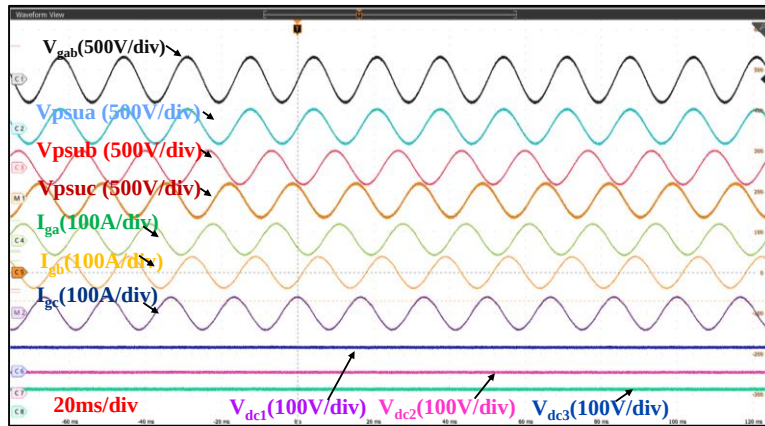
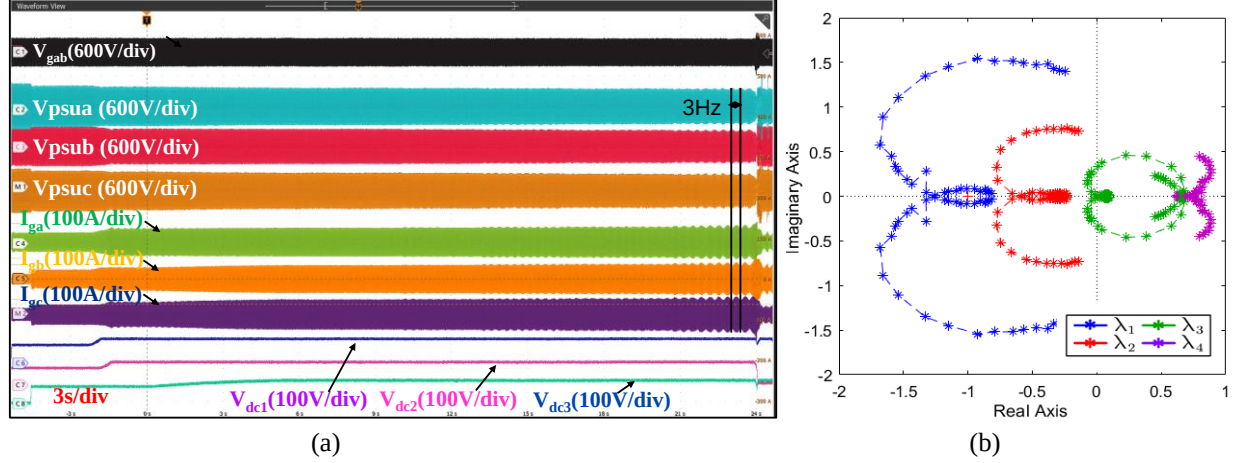


Figure 3-10 (1)Time-domain waveforms, and (2) Nyquist Diagram of Case 3.



The above results and analysis verify the three-phase-three-wire system minor loop gain model. Therefore, such a virtual d-q frame modeling approach can be extended to stability analysis of other systems with similar configurations. For a system with a low X/R ratio in the line impedance, small-signal instability is also not likely to happen before the system confronts operating points issues with large line impedance.

3.4 Three-phase-four-wire system

3.4.1 System Model

This section proposes a virtual d-q frame model for a three-phase four-wire system with single-phase loads, as shown in Figure 3-12 (a). The main idea of the modeling approach is shown in Figure 3-12. By considering each phase as a single-phase circuit while still considering the coupling among the three single-phase circuits, another two virtual frames y and z are constructed for each phase, and a d-q frame model can be obtained by Park's transformation. This process can also be derived mathematically using the circuit equations as shown below. Firstly, the equations describing the original system are

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \begin{bmatrix} Z_{ga} + Z_{gn} & Z_{gn} & Z_{gn} \\ Z_{gn} & Z_{gb} + Z_{gn} & Z_{gn} \\ Z_{gn} & Z_{gn} & Z_{gc} + Z_{gn} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}. \quad (3-28)$$

Defining transformation matrix $\mathbf{T}_a$, $\mathbf{T}_b$, $\mathbf{T}_c$ so that

$$\begin{bmatrix} v_{ax} \\ v_{ay} \\ v_{az} \end{bmatrix} = \mathbf{T}_a \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \begin{bmatrix} v_{bx} \\ v_{by} \\ v_{bz} \end{bmatrix} = \mathbf{T}_b \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \begin{bmatrix} v_{cx} \\ v_{cy} \\ v_{cz} \end{bmatrix} = \mathbf{T}_c \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3-29)$$

$$\mathbf{T}_a = \begin{bmatrix} 1 & 0 & 0 \\ a & 0 & 0 \\ a^2 & 0 & 0 \end{bmatrix}, \mathbf{T}_b = \begin{bmatrix} 0 & 1 & 0 \\ 0 & a & 0 \\ 0 & a^2 & 0 \end{bmatrix}, \mathbf{T}_c = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & a \\ 0 & 0 & a^2 \end{bmatrix} \quad (3-30)$$

$$a = e^{-j120^\circ} \quad (3-31)$$

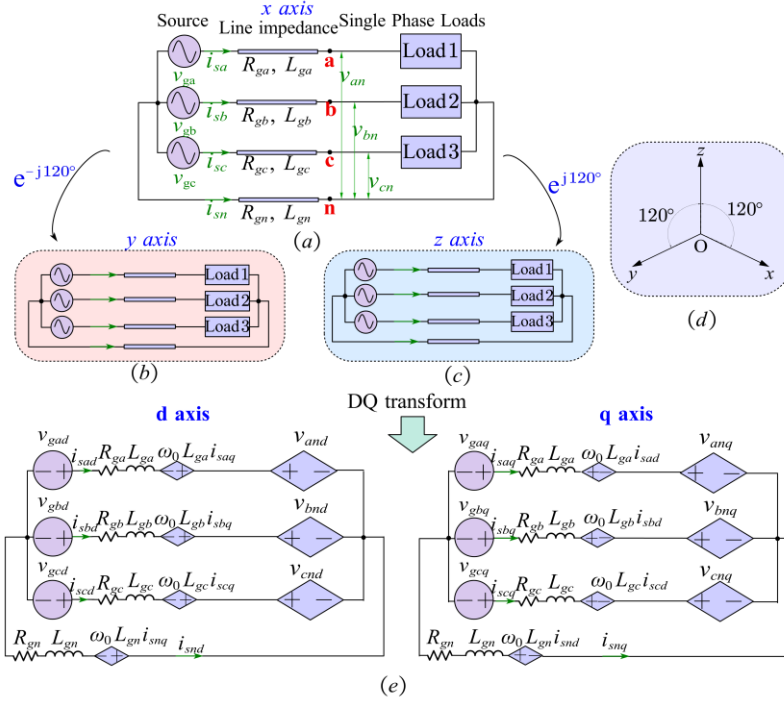


Figure 3-12 Virtual d-q frame modeling method: (a) the original systems; (b) the virtual frame y system; (c) the virtual z frame system; (d) the frame difference of x, y, and z; (e) the dq model.

Multiplying $\mathbf{T}_a$, $\mathbf{T}_b$, and $\mathbf{T}_c$ respectively to the (3-28) yield

$$\begin{bmatrix} v_{anx} \\ v_{any} \\ v_{anz} \end{bmatrix} = \begin{bmatrix} v_{gax} \\ v_{gay} \\ v_{gaz} \end{bmatrix} - Z_{ga} \begin{bmatrix} i_{sax} \\ i_{say} \\ i_{saz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \quad (3-32)$$

$$\begin{bmatrix} v_{bnx} \\ v_{bny} \\ v_{bnz} \end{bmatrix} = \begin{bmatrix} v_{gbx} \\ v_{gby} \\ v_{gbz} \end{bmatrix} - Z_{gb} \begin{bmatrix} i_{sbx} \\ i_{sby} \\ i_{sbz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \quad (3-33)$$

$$\begin{bmatrix} v_{cnx} \\ v_{cny} \\ v_{cnz} \end{bmatrix} = \begin{bmatrix} v_{gcx} \\ v_{gcy} \\ v_{gcx} \end{bmatrix} - Z_{gc} \begin{bmatrix} i_{scx} \\ i_{scy} \\ i_{scz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \quad (3-34)$$

$$\begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} = - \left(\begin{bmatrix} i_{sax} \\ i_{say} \\ i_{saz} \end{bmatrix} + \begin{bmatrix} i_{sbx} \\ i_{sby} \\ i_{sbz} \end{bmatrix} + \begin{bmatrix} i_{scx} \\ i_{scy} \\ i_{scz} \end{bmatrix} \right) \quad (3-35)$$

By applying the dq transformation to (3-32) ~ (3-35), the system's dq frame model can be derived as

$$\begin{bmatrix} v_{and} \\ v_{anq} \end{bmatrix} = \begin{bmatrix} v_{gad} \\ v_{gaq} \end{bmatrix} - \mathbf{Z}_{ga} \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix}, \quad (3-36)$$

$$\begin{bmatrix} v_{bnd} \\ v_{bnq} \end{bmatrix} = \begin{bmatrix} v_{gbd} \\ v_{gbq} \end{bmatrix} - \mathbf{Z}_{gb} \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix}, \quad (3-37)$$

$$\begin{bmatrix} v_{cnd} \\ v_{cnq} \end{bmatrix} = \begin{bmatrix} v_{gcd} \\ v_{gcq} \end{bmatrix} - \mathbf{Z}_{gc} \begin{bmatrix} i_{scd} \\ i_{scq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix}, \quad (3-38)$$

$$-\begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix} = \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} + \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} + \begin{bmatrix} i_{scd} \\ i_{scq} \end{bmatrix}. \quad (3-39)$$

Equation (3-40) shows the expressions of $\mathbf{Z}_{ga}$, $\mathbf{Z}_{gb}$, $\mathbf{Z}_{gc}$, and $\mathbf{Z}_N$.

$$\begin{aligned} \mathbf{Z}_{ga} &= \begin{bmatrix} R_{ga} + sL_{ga} & -\omega_0 L_{ga} \\ \omega_0 L_{ga} & R_{ga} + sL_{ga} \end{bmatrix}, \quad \mathbf{Z}_{gb} = \begin{bmatrix} R_{gb} + sL_{gb} & -\omega_0 L_{gb} \\ \omega_0 L_{gb} & R_{gb} + sL_{gb} \end{bmatrix} \\ \mathbf{Z}_{gc} &= \begin{bmatrix} R_{gc} + sL_{gc} & -\omega_0 L_{gc} \\ \omega_0 L_{gc} & R_{gc} + sL_{gc} \end{bmatrix}, \quad \mathbf{Z}_N = \begin{bmatrix} R_{gn} + sL_{gn} & -\omega_0 L_{gn} \\ \omega_0 L_{gn} & R_{gn} + sL_{gn} \end{bmatrix} \end{aligned} \quad (3-40)$$

With (3-36)~(3-39), the original system's model in the virtual d - q frame can be pictured in a circuit diagram, as shown in Figure 3-12 (e). This method essentially treats each phase as a single-phase circuit while still preserving the coupling effects among the three phases because they are also in the same three-phase system.

Since the two virtual frame circuits are created by phase-shifting the original system, the stability condition of the original three-phase system is equivalent to that of the two virtual circuits and the new system in the XYZ coordinate. Therefore, the stability of the original system can be assessed by performing an impedance analysis on the small-signal model of the system based on Figure 3-12 (d).

3.4.2 Impedance Model for Stability Analysis

For impedance-based small-signal stability analysis, the main steps include first defining an interface for analysis, then obtaining the upstream impedance and downstream admittance, defining the minor loop gain matrix, and finally applying the Generalized Nyquist Criterion (GNC)

to the minor-loop-gain. For impedance analysis, this section groups the power source and the distribution line as the upstream subsystem, and the single-phase loads as the downstream subsystem. With the time-invariant system d - q model in Figure 3-12 (d), it is feasible to perform a small-signal analysis. In this section, the impedance models of a four-wire system with single-phase PSU loads are first derived. Then they are simplified for a dominant neutral inductor scenario and further simplified for three-phase balanced cases.

3.4.2.1 A Generic Model

Assuming a certain equilibrium operating point, the following small-signal relationships can be obtained after linearizing (3-41)~(3-44).

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = -\mathbf{Z}_{ga} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (3-41)$$

$$\begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = -\mathbf{Z}_{gb} \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (3-42)$$

$$\begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = -\mathbf{Z}_{gc} \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (3-43)$$

$$-\begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} \quad (3-44)$$

For each single-phase PSU load, the relationship between its input voltage and current small-signal components is its d - q admittance, as shown in (3-45) ~ (3-47).

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} = \mathbf{Y}_{PSUa} \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \begin{bmatrix} Y_{PSUadd} & Y_{PSUadq} \\ Y_{PSUaqd} & Y_{PSUaqq} \end{bmatrix} \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} \quad (3-45)$$

$$\begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} = \mathbf{Y}_{PSUb} \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = \begin{bmatrix} Y_{PSUbdd} & Y_{PSUbdq} \\ Y_{PSUbqd} & Y_{PSUbqq} \end{bmatrix} \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} \quad (3-46)$$

$$\begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} = \mathbf{Y}_{PSUc} \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \begin{bmatrix} Y_{PSUcdd} & Y_{PSUcdq} \\ Y_{PSUcq d} & Y_{PSUcq q} \end{bmatrix} \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} \quad (3-47)$$

Given (3-41)~(3-47), the small-signal model in the virtual d - q frame is shown in Figure 3-13. The interface for impedance analysis is chosen to be the input of the PSU loads. From the interface, the upstream impedance is defined as follows.

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \\ \hat{v}_{bnd} \\ \hat{v}_{bnq} \\ \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \mathbf{Z}_{\text{source}} \cdot \begin{bmatrix} -\hat{i}_{sad} \\ -\hat{i}_{saq} \\ -\hat{i}_{sbd} \\ -\hat{i}_{sbq} \\ -\hat{i}_{scd} \\ -\hat{i}_{scq} \end{bmatrix} \quad (3-48)$$

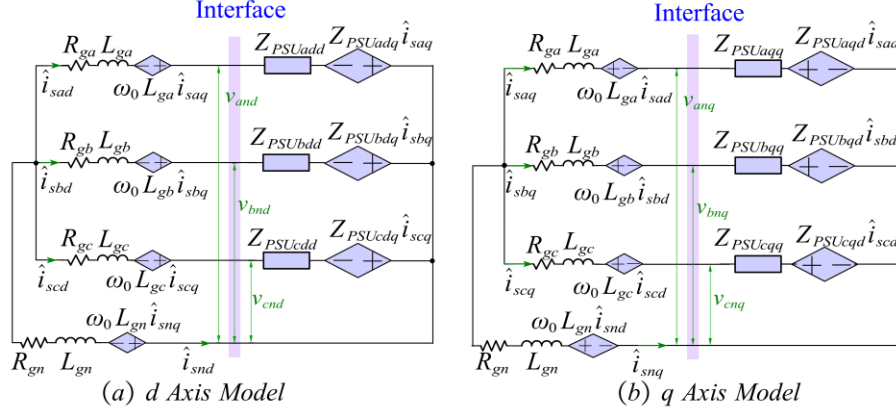


Figure 3-13 Small-signal model of a four-wire system in the d-q frame.

From (3-41)~(3-44) and (3-48), the upstream impedance is

$$\mathbf{Z}_{\text{source}} = \begin{bmatrix} \mathbf{Z}_{\text{N}} + \mathbf{Z}_{\text{ga}} & \mathbf{Z}_{\text{N}} & \mathbf{Z}_{\text{N}} \\ \mathbf{Z}_{\text{N}} & \mathbf{Z}_{\text{N}} + \mathbf{Z}_{\text{gb}} & \mathbf{Z}_{\text{N}} \\ \mathbf{Z}_{\text{N}} & \mathbf{Z}_{\text{N}} & \mathbf{Z}_{\text{N}} + \mathbf{Z}_{\text{gc}} \end{bmatrix}. \quad (3-49)$$

The off-diagonal terms of (3-49) denote the coupling among the three phases. Looking at the interface, the downstream admittance is defined as follows.

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \\ \hat{i}_{sbd} \\ \hat{i}_{sbq} \\ \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} = \mathbf{Y}_{\text{load}} \cdot \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \\ \hat{v}_{bnd} \\ \hat{v}_{bnq} \\ \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} \quad (3-50)$$

From (3-41)~(3-44) and (3-50), the downstream impedance is defined as follows.

$$\mathbf{Y}_{\text{load}} = \begin{bmatrix} \mathbf{Y}_{\text{PSUa}} & 0 & 0 \\ 0 & \mathbf{Y}_{\text{PSUb}} & 0 \\ 0 & 0 & \mathbf{Y}_{\text{PSUc}} \end{bmatrix} \quad (3-51)$$

Notably, $\mathbf{Y}_{\text{PSUa}}$, $\mathbf{Y}_{\text{PSUb}}$, and $\mathbf{Y}_{\text{PSUc}}$ are defined with the d -axis aligned with v_{anx} . The system minor loop gain is defined as

$$\mathbf{L}_{\text{sys}} = \mathbf{Z}_{\text{source}} \cdot \mathbf{Y}_{\text{load}}. \quad (3-52)$$

Since $\mathbf{Z}_{\text{ga}}$, $\mathbf{Z}_{\text{gb}}$, $\mathbf{Z}_{\text{gc}}$, $\mathbf{Z}_{\text{N}}$, $\mathbf{Y}_{\text{PSUa}}$, $\mathbf{Y}_{\text{PSUb}}$, and $\mathbf{Y}_{\text{PSUc}}$ are all 2×2 matrices, $\mathbf{Z}_{\text{source}}$, $\mathbf{Y}_{\text{load}}$, and $\mathbf{L}_{\text{sys}}$ are 6×6 matrices. If the system has negligible neutral-line impedance, (3-49) and (3-51) become

$$\mathbf{Z}_{\text{source}} = \begin{bmatrix} \mathbf{Z}_{\text{ga}} & 0 & 0 \\ 0 & \mathbf{Z}_{\text{gb}} & 0 \\ 0 & 0 & \mathbf{Z}_{\text{gc}} \end{bmatrix} \quad (3-53)$$

$$\mathbf{L}_{\text{sys}} = \begin{bmatrix} \mathbf{Z}_{\text{ga}} \mathbf{Y}_{\text{PSUa}} & 0 & 0 \\ 0 & \mathbf{Z}_{\text{gb}} \mathbf{Y}_{\text{PSUb}} & 0 \\ 0 & 0 & \mathbf{Z}_{\text{gc}} \mathbf{Y}_{\text{PSUc}} \end{bmatrix}. \quad (3-54)$$

Therefore, the three phases are decoupled and become three independent single-phase circuits. Thus, the model in (3-52) is the same as using the existing virtual d - q frame modeling method to analyze each phase as a single-phase circuit.

3.4.2.2 System with Dominant Neutral-Line Inductor

In some data center power systems, a three-phase four-wire system may be equipped with a high neutral-line inductor due to the purpose of limiting short-circuit currents in fault conditions, or due to thinner cable design with lower current capacity compared with three-phase lines. The system model can be simplified from the generic one discussed above. Since the phase impedance is much smaller than the neutral-line impedance, it is neglected. Equations (3-41)~(3-44) can then be written as follows.

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \mathbf{Z}_{\text{N}} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = \begin{bmatrix} Z_{Ndd} & Z_{Ndq} \\ Z_{Nqd} & Z_{Nqq} \end{bmatrix} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (3-55)$$

Equations (3-45)~(3-47) and (3-55) yield the following.

$$\begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = (\mathbf{Y}_{PSUa} + \mathbf{Y}_{PSUb} + \mathbf{Y}_{PSUc}) \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} \quad (3-56)$$

From (3-55) and (3-56), the system's small-signal model in the virtual d - q frame can be pictured in Figure 3-14. From the interface, the upstream impedance is defined as

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \mathbf{Z}_{source} \cdot \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (3-57)$$

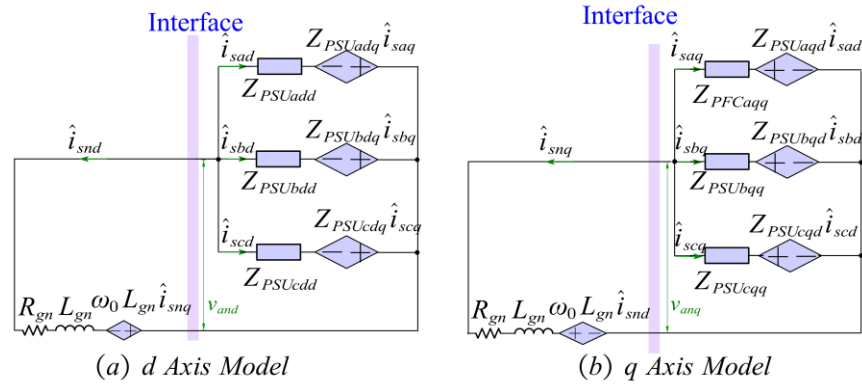


Figure 3-14 Small-signal model of a four-wire system with a dominant neutral inductor in the d - q frame.

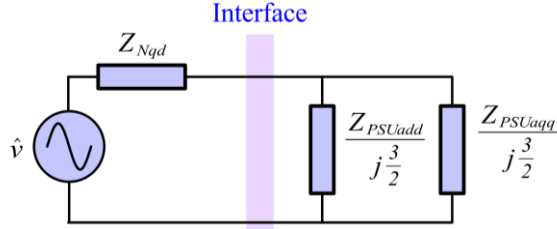


Figure 3-15 Equivalent small-signal model of a balanced-four-wire system with dominant neutral line inductance in the d - q frame.

From (3-55), $\mathbf{Z}_{source}$ is equal to $\mathbf{Z}_N$. Looking at the interface, the downstream admittance is defined as follows.

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \mathbf{Y}_{load} \cdot \begin{bmatrix} -\hat{i}_{snd} \\ -\hat{i}_{snq} \end{bmatrix} \quad (3-58)$$

Therefore, for dominant neutral inductor scenarios, $\mathbf{Z}_{\text{source}}$, $\mathbf{Y}_{\text{load}}$, and $\mathbf{L}_{\text{sys}}$ are 2×2 matrices. Notably, the operating points on the d-q frame of PSU for phase *a*, phase *b*, and phase *c* are different because they are transferring to the *d-q* frame aligning with the same angle.

From (3-56), the downstream impedance is

$$\mathbf{Y}_{\text{load}} = \mathbf{Y}_{\text{PSUa}} + \mathbf{Y}_{\text{PSUb}} + \mathbf{Y}_{\text{PSUc}}. \quad (3-59)$$

For the three-phase balanced case, the difference among $\mathbf{Y}_{\text{PSUa}}$, $\mathbf{Y}_{\text{PSUb}}$, and $\mathbf{Y}_{\text{PSUc}}$ results from a different operating point only because of the phase-angle difference.

$$\begin{cases} \mathbf{Y}_{\text{PSUb}} = \mathbf{T}_{-\frac{2\pi}{3}} \mathbf{Y}_{\text{PSUa}} \mathbf{T}_{-\frac{2\pi}{3}}^{-1} \\ \mathbf{Y}_{\text{PSUc}} = \mathbf{T}_{\frac{2\pi}{3}} \mathbf{Y}_{\text{PSUa}} \mathbf{T}_{\frac{2\pi}{3}}^{-1} \end{cases} \quad (3-60)$$

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos\Delta\theta & \sin\Delta\theta \\ -\sin\Delta\theta & \cos\Delta\theta \end{bmatrix} \quad (3-61)$$

The single-phase PSU's admittance is diagonally dominant if the d-axis is aligned with the input voltage [7]. Therefore, $\mathbf{Y}_{\text{PSUa}}$ is diagonally dominant, and $\mathbf{Y}_{\text{PSUb}}$ and $\mathbf{Y}_{\text{PSUc}}$ can be approximated as (3-62) and (3-63).

$$\mathbf{Y}_{\text{PSUb}} \approx \begin{bmatrix} \frac{1}{4}Y_{\text{PSUadd}} + \frac{3}{4}Y_{\text{PSUaqq}} & -\frac{\sqrt{3}}{4}(Y_{\text{PSUadd}} - Y_{\text{PSUaqq}}) \\ -\frac{\sqrt{3}}{4}(Y_{\text{PSUadd}} - Y_{\text{PSUaqq}}) & \frac{3}{4}Y_{\text{PSUdd}} + \frac{1}{4}Y_{\text{PSUaqq}} \end{bmatrix} \quad (3-62)$$

$$\mathbf{Y}_{\text{PSUc}} \approx \begin{bmatrix} \frac{1}{4}Y_{\text{PSUadd}} + \frac{3}{4}Y_{\text{PSUaqq}} & \frac{\sqrt{3}}{4}(Y_{\text{PSUadd}} - Y_{\text{PSUaqq}}) \\ \frac{\sqrt{3}}{4}(Y_{\text{PSUadd}} - Y_{\text{PSUaqq}}) & \frac{3}{4}Y_{\text{PSUdd}} + \frac{1}{4}Y_{\text{PSUaqq}} \end{bmatrix} \quad (3-63)$$

With a large neutral-line inductance, the grid-side impedance is off-diagonal dominant at low frequencies, such that,

$$|Z_{\text{Ndd}}|, |Z_{\text{Nqq}}| \approx 0 \quad (3-64)$$

With (3-62), (3-63), and (3-64), the minor loop gain of the system can be simplified as

$$\mathbf{L}_{\text{sys}} \approx \begin{bmatrix} 0 & Z_{\text{Ndq}}(Y_{\text{PSUaqq}} + 2Y_{\text{PSUbqq}}) \\ Z_{\text{Nqd}}(Y_{\text{PSUadd}} + 2Y_{\text{PSUbdd}}) & 0 \end{bmatrix}. \quad (3-65)$$

The characteristic equation of (3-65) can be derived as

$$\lambda^2 + Z_{Nqd}^2 \left(\frac{3}{2} Y_{PSUadd} + \frac{3}{2} Y_{PSUaq} \right)^2 = 0 \quad (3-66)$$

So the two eigenvalues can be solved as follows.

$$\begin{cases} \lambda_1 = jZ_{Nqd} \left(\frac{3}{2} Y_{PSUadd} + \frac{3}{2} Y_{PSUaq} \right) \\ \lambda_2 = -jZ_{Nqd} \left(\frac{3}{2} Y_{PSUadd} + \frac{3}{2} Y_{PSUaq} \right) \end{cases} \quad (3-67)$$

From (3-67), λ_1 and λ_2 have a negative phase. In this study, λ_1 is in the left half-plane, which is the critical one for stability analysis. The MIMO system stability analysis is equivalent to analyzing a single-input-single-output (SISO) system, such as that shown in Figure 3-15. For the SISO system, it's sufficient to use a Bode plot criterion to assess system stability. The upstream impedance Z_{source} and downstream impedance Z_{load} are

$$Z_{source} = Z_{Nqd} \quad (3-68)$$

$$Z_{load} = 1 / \left(1 / \left(\frac{Z_{PSUadd}}{j^{\frac{3}{2}}} \right) + 1 / \left(\frac{Z_{PSUaq}}{j^{\frac{3}{2}}} \right) \right) \quad (3-69)$$

At low frequencies, the gain of Z_{PSUadd} and Z_{PSUaq} is negatively proportional to the power level, and Z_{Nqd} is proportional to the neutral-line inductor value, (3-68) and (3-69) reveal that to achieve a similar stability margin when increasing PSU load power by N times, the neutral-line inductor needs to be reduced to 1/N of its original value. This finding is important for performing impedance specifications in such scenarios.

3.4.3 Simulation Verification

In a power-electronics-based system, typical instability issues occur because of the constant-power load behavior of the converters and their dynamic interactions with the inductive line impedance. To verify the proposed impedance-based models for stability analysis of a four-wire system, single-phase PSU loads with circuit and control diagrams are shown in Figure 3-16. are studied in PLECS. A PSU is composed of a front-end PFC and a cascaded DC-DC converter load. A totem-pole topology PFC converter operating in continuous-current mode is studied. Its

controller contains a proportional-resonant (PR) based current controller, a proportional-integral (PI) based DC voltage controller, a phase-tracking unit, and an input voltage feedforward control. At low frequencies, both an isolated DC-DC converter and a non-isolated converter can be modeled as a negative resistor [18]. A buck converter is thus selected as the cascaded DC-DC converter in the simulation study because it is much easier to model. Its controller contains an inner current controller and an output DC voltage controller. Both use a PI controller. The parameters of the PFC and the DC-DC converter are shown in Table 2-1. The subsystem impedance model requires the PSU load's d-q impedance. The d-q impedance of the PSU is obtained based on the modeling and measurement method described in Ref. [7]. The three-phase four-wire system in the simulation is shown in Figure 3-17.

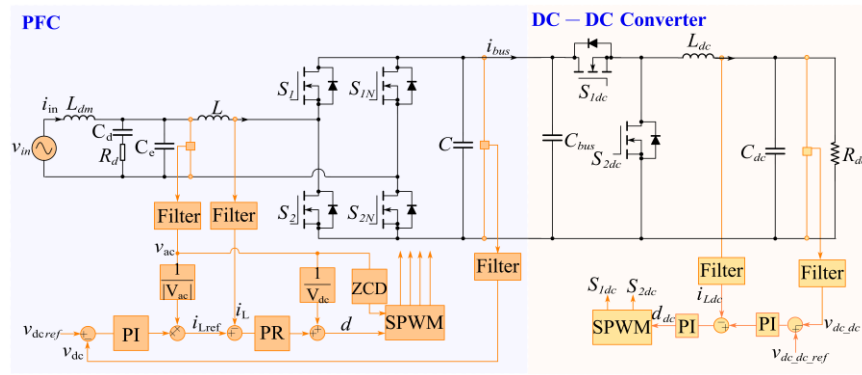


Figure 3-16. PSU structure and control diagrams.

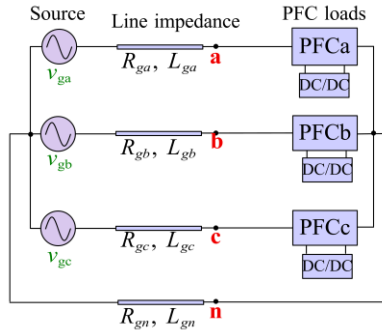


Figure 3-17. System configuration of the simulation study.

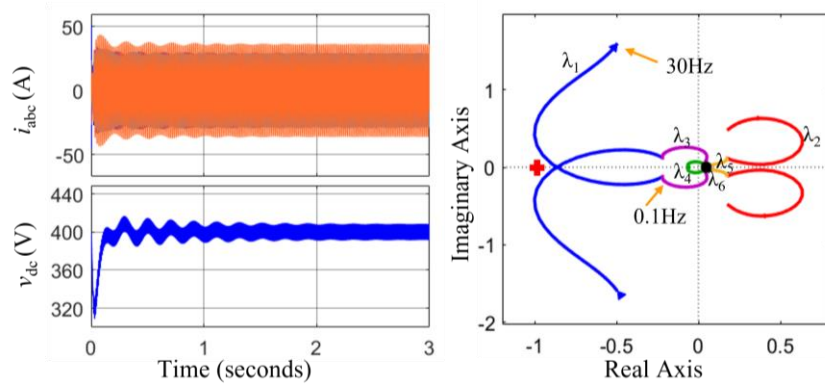


Figure 3-18. AC current, one PSU's DC voltage, and Nyquist plot of Case 1.

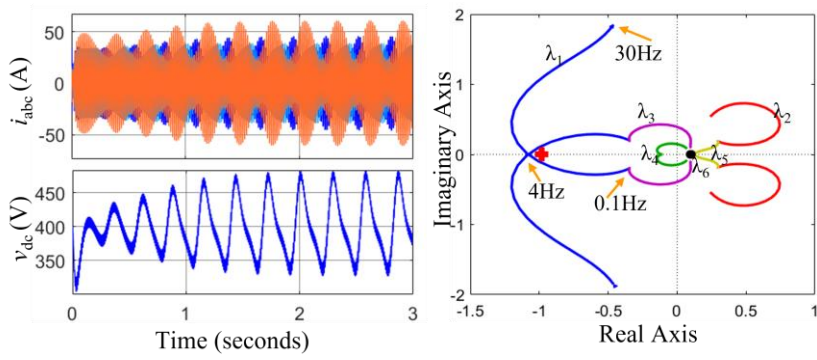


Figure 3-19. AC current, one PSU's DC voltage, and Nyquist plot of Case 2.

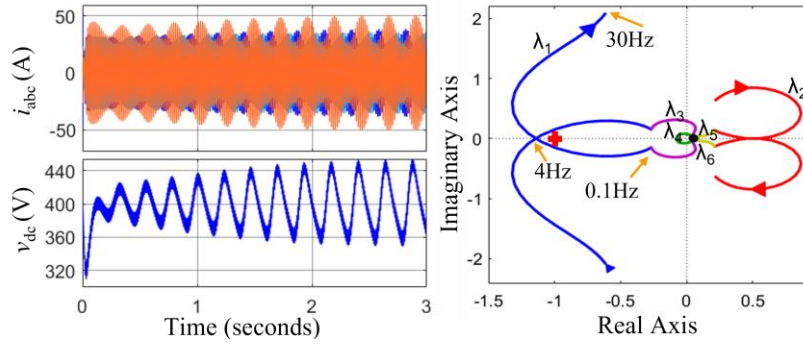


Figure 3-20 AC current, one PSU's DC voltage, and Nyquist plot of Case 3a.

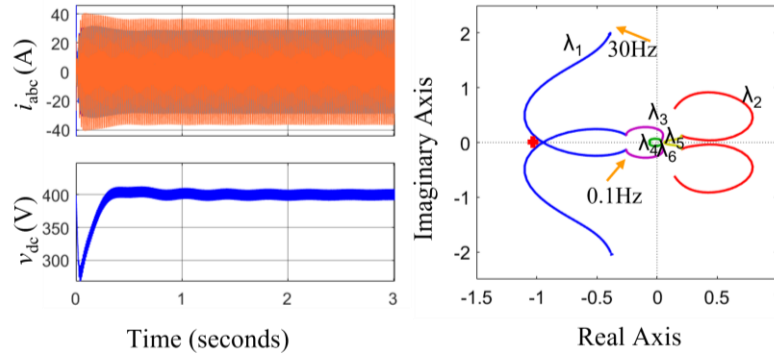


Figure 3-21. AC current, one PSU's DC voltage, and Nyquist plot of Case 3b.

Three ideal voltage sources provide power for the three PFC loads. There is some impedance at the cable in each phase and the neutral cable. To verify the 6×6 impedance matrix models for a generic four-wire system, four cases are conducted. The line impedance, voltage, and power level of each case are shown in Table 3-4. All cases have an unbalanced level of 10 %. The grid's three-phase line impedance is increased for Case 2 compared to Case 1. The neutral inductor is increased for Case 3a compared to Case 1. The PFC controller parameters of Case 1, Case 2, and Case 3a are the same. For Case 3b, the PFC voltage PI controller's proportional and integral gains are decreased to 1/3 that of Case 3a.

The three-phase current, one of the PSU load's DC bus voltages, and the eigenvalue loci obtained in (22), (24), and (25) of the four cases are shown in Figure 3-18 to Figure 3-21, respectively. Case 1 and Case 3b both show stable operation in the time domain and no encirclements of $(-1, 0)$ in the Nyquist plot. Case 2 and Case 3a exhibit 3.7 Hz and 4.3 Hz oscillations respectively and two encirclements of $(-1, 0)$ in their Nyquist plot. The frequency of the point close to $(-1, 0)$ in the Nyquist plot is also close to the corresponding oscillation frequency. The impedance analysis matches the time-domain results. These four cases verify the 6×6 impedance matrix models for stability analysis. They also show that increasing either phase impedance or neutral line impedance is detrimental to stability while changing the PFC controller parameters could help resolve the instability issues.

Table 3-4. Line impedance, and power of Case 1 ~ Case 3.

Case	Phase Impedance	Neutral Inductor	Phase <i>a</i> Power	Phase <i>b</i> Power	Phase <i>c</i> Power
------	-----------------	------------------	----------------------	----------------------	----------------------

1	$0.5\Omega+390\mu\text{H}$	10 mH	4.5 kW	5 kW	5.5 kW
2	$1\Omega+810\mu\text{H}$	10 mH	4.5 kW	5 kW	5.5 kW
3a/3b	$0.5\Omega+390\mu\text{H}$	12 mH	4.5 kW	5 kW	5.5 kW

Table 3-5. Line impedance, and power of Case 4 ~ Case 6.

Case	Neutral Inductor	Phase <i>a</i> Power	Phase <i>b</i> Power	Phase <i>c</i> Power
4	5 mH	9 kW	10 kW	11 kW
5	8 mH	9 kW	10 kW	11 kW
6	5 mH	13.5 kW	15 kW	16.5 kW

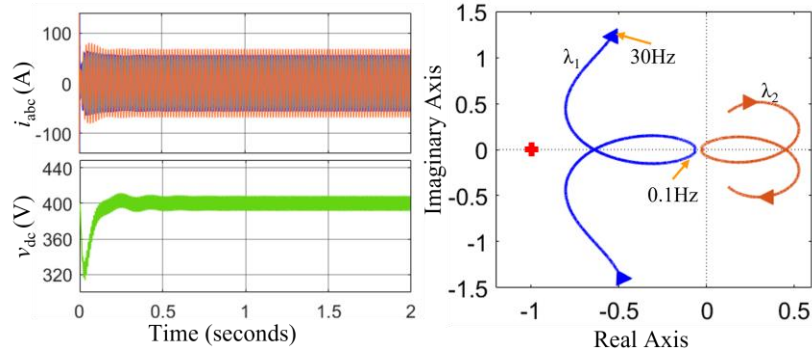


Figure 3-22. AC current, one PSU's DC voltage, and Nyquist plot of Case 4.

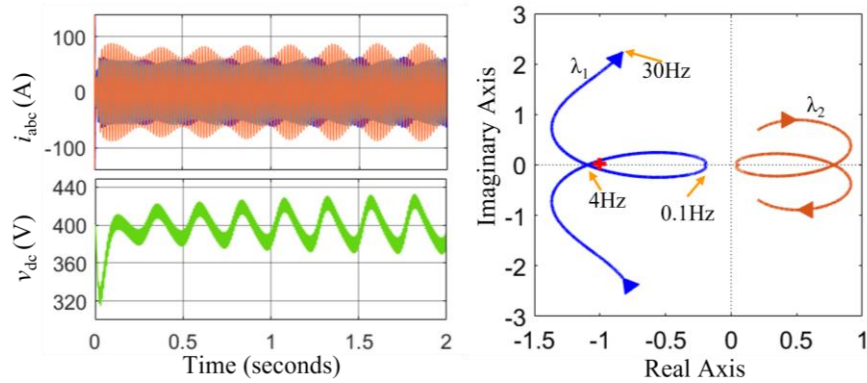


Figure 3-23. AC current, one PSU's DC voltage, and Nyquist plot of Case 5.

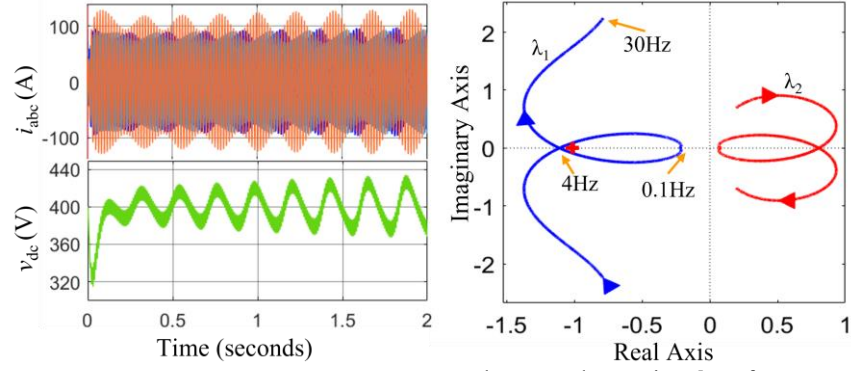


Figure 3-24. AC current, one PSU's DC voltage, and Nyquist plot of Case 6.

To verify the 2×2 impedance matrix model derived for the four-wire system with dominant neutral line inductance, three cases are studied. The neutral inductance, voltage, and power of each case are shown in Table 3-6. For Case 4 and Case 5, there are two identical PSU loads connected to each phase. For Case 6, there are three identical PSU loads connected to each phase. All three cases are at a 10 % unbalance level. The neutral inductor is increased for Case 5 compared to Case 4. The power level of Case 6 is increased compared with Case 4. The three-phase current, one of the PSU load's DC bus voltages, and the eigenvalue loci obtained through (25), (28), and (32) of the three cases are shown in Figure 3-22 to Figure 3-24 respectively.

Case 4 is stable in the time domain and shows no encirclements of $(-1, 0)$ in its Nyquist plot. Case 5 and Case 6 exhibit 4 Hz and 4.5 Hz oscillations respectively and two encirclements of $(-1, 0)$ in their Nyquist plot. The frequency of the point close to $(-1, 0)$ in the Nyquist plot is also close to the corresponding oscillation frequency. The impedance analysis results match the time-domain results, thus verifying the 2×2 impedance matrix models for the dominant neutral inductor scenarios. They also show that increasing either neutral line impedance or system power level is detrimental to stability. To verify the effectiveness of the simplified SISO model for a balanced four-wire system with dominant neutral inductance, two cases are studied, with parameters shown in Table 3-6. The neutral inductor for Case 8 is increased compared to Case 7. The three-phase current, one of the PSU load's DC bus voltages, and the upstream and downstream impedance obtained from the two cases are shown in Figure 3-25 and Figure 3-26 respectively. Case 7 is stable in the time domain. Case 8 shows around 4.5 Hz oscillations. In the impedance Bode plot, at the point of intersection of Z_{source} and Z_{load} , the phase difference of Case 7 is lower than 180° ,

while for Case 8 it's larger than 180° . According to the Bode plot criterion, the impedance analysis matches the time-domain results.

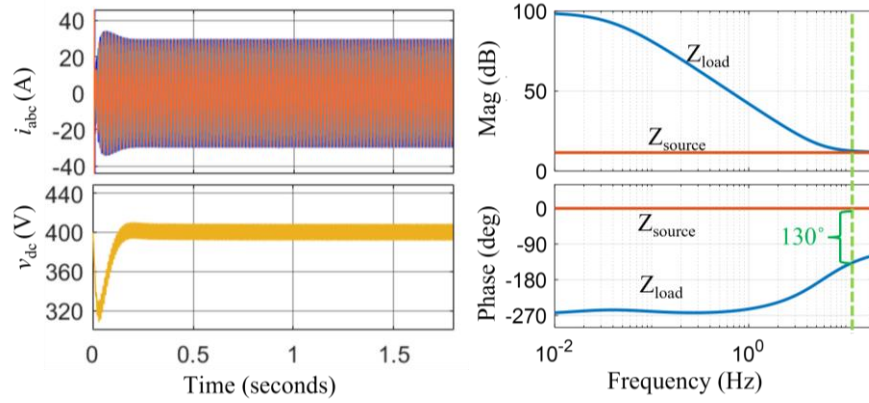


Figure 3-25. AC current, one PSU's DC voltage, and Bode plot of source and load impedance of Case 7: $L_{gn}=10\text{mH}$.

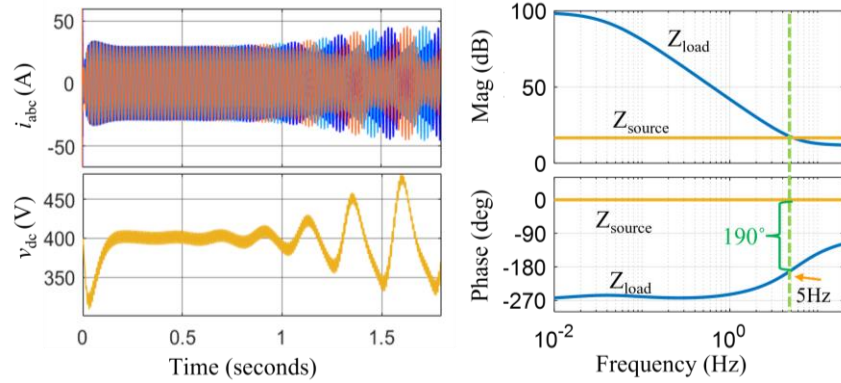


Figure 3-26. AC current, one PSU's DC voltage, and Bode plot of source and load impedance of Case 8: $L_{gn}=18\text{mH}$.

Table 3-6 Line impedance, voltage, and power of Case 7 and Case 8.

Case	Neutral Inductor	Phase a/b/c Power
7	10 mH	5 kW
8	18 mH	

In summary, this section verified the proposed impedance models of the upstream and downstream for stability analysis. Instability issues are a compound result of improper design or operations of both the upstream and the downstream. For example, in a data center power system, the upstream impedance is mainly composed of the distribution line impedance, transformer leakage inductance, and sometimes reactors added for protection. By the proposed model, Case 1 ~ Case 3a, Case 4 and Case 5, Case 7, and Case 8 show that increasing upstream impedance to an

extent could lead to instability; on the contrary, keeping it within a limit is a way to avoid such oscillation issues. Accordingly, in practice, the system operator could reduce the distance and cable length between the substation and the server rooms, redesign the transformer to limit the leakage impedance, or choose other protection schemes to avoid large reactor installation. Some of these changes are related to data center architecture reconstruction, which may require high costs and complexity. Therefore, on the other hand, system operators could choose to modify the downstream side, including asking the power supply vendors to modify their product design or reduce the power of the workload. By the proposed model, Case 3a and Case 3b, Case 4 ~ Case 6 show that reducing the total load power or reducing the PFC controller gain could resolve instability.

The proposed impedance model utilizes the d-q impedance of one PFC converter, which exhibits negative resistor characteristics in the Z_{dd} term. Ref. [19] shows that reducing the PI controller gain of the PFC voltage controller would shift the phase of Z_{dd} higher and further away from -180° , so the negative resistor characteristic is diminished. For Case 3b, the PFC voltage PI controller proportional and integral gains are decreased to 1/3 of that of Case 3a. The phase of the eigenvalue locus 1 of Case 3b around 4 Hz decreases; thus, it moves to the right of the $(-1, 0)$, so no encirclements are exhibited. From a qualitative analysis aspect, the proposed model could characterize the impact of PFC parameters on the system stability. On another note, reducing the PFC PI parameters means degrading the performance of the dc voltage loop. At the same time, it is not critical for the studied system because the cascaded dc-dc converter maintains the high performance of load dc voltage regulation. However, for some other systems, when the cascaded dc-dc converter is absent, some novel active damping control schemes can be designed based on the proposed model to solve the oscillation issues and maintain output voltage regulation performance [20].

3.4.4 Experimental Verification

This section aims to verify the proposed impedance-based stability analysis model in Section III using experimental tests. Figure 3-27 shows the experimental setup. With the same three-phase four-wire configuration as in Figure 3-12 (a), some resistors and inductors representing line

impedance are connected between a three-phase AC source and the PSU loads, which are three commercial PSUs with part number FLATPACK2241119. 905B. These PSUs are with isolated DC-DC converters in the DC stage. The PSUs are connected to resistor loads. Note that these PSUs' internal parameters are not available, which are different from the ones in the simulation study. These PSUs operating voltage range is $100V_{\text{rms}} \sim 275 V_{\text{rms}}$. Due to the available equipment, the test is carried out at about $150 V_{\text{rms}}$. The models can work for any other voltage level as long as the PFC impedance is measured at the corresponding voltage. Each PSU's $d-q$ impedance at different powers and voltages according to the test conditions is measured using an Impedance Measured Unit (IMU). The measurement process and results are shown in Chapter 2.

Case 1 ~ Case 3 is designed to verify the 6×6 impedance matrix models. Table 3-7 shows the parameters of the four-wire system. With other parameters being the same, the system total power is changed from 3 kW to 2.8 kW, and 2.6 kW in Case 1, Case 2, and Case 3 respectively. The time-domain test and the Nyquist plots of the three cases are shown in Figure 3-28 to Figure 3-30, respectively. Case 1 and Case 2 both have low-frequency oscillations at around 4 Hz while Case 3 is stable. Correspondingly, the eigenvalue loci of the calculated 6×6 minor loop gain of Case 1 and Case 2 have encirclements of $(-1, 0)$ while Case 3's does not. The test results of Case 1 ~ Case 3 verify the effectiveness of the 6×6 impedance model to assess the stability of the four-wire system in both balanced and unbalanced conditions. Case 4 ~ Case 7 showcases negligible phase impedance compared with a dominant neutral line inductor to verify the 2×2 impedance matrix model for such a scenario. The system parameters of Case 4 ~ Case 7 are shown in Table 6. Case 4 and Case 5 are balanced. Case 6 and Case 7 are 10 % unbalanced.

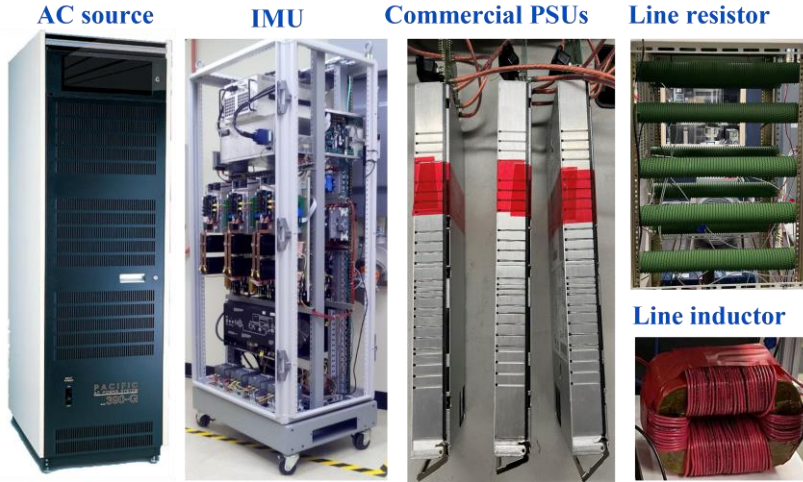


Figure 3-27 Experimental setup.

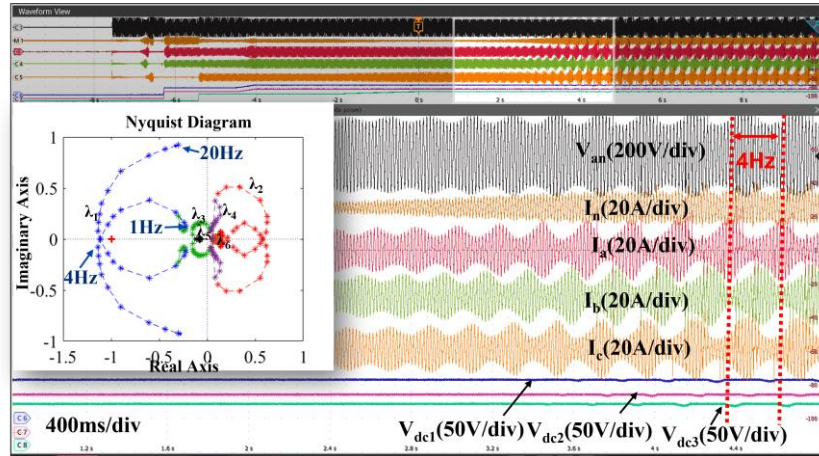


Figure 3-28 Test results and Nyquist plot of Case 1.

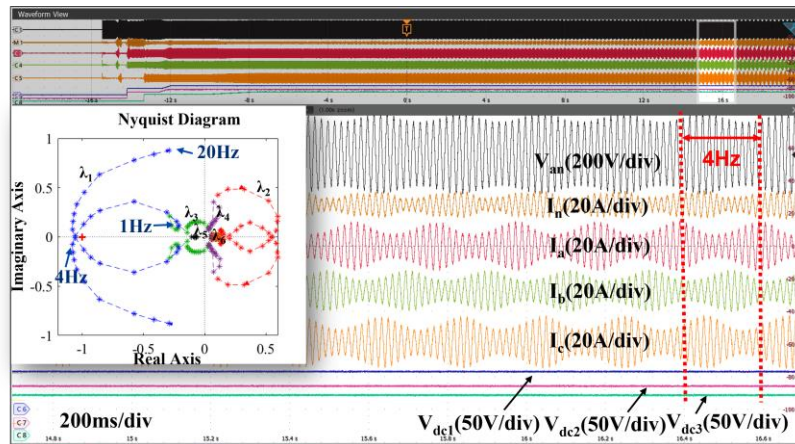


Figure 3-29 Test results and Nyquist plot of Case 2.

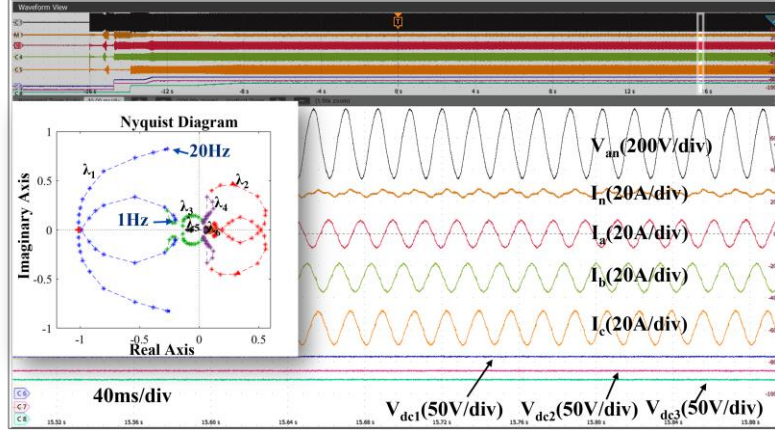


Figure 3-30 Test results and Nyquist plot of Case 3.

Table 3-7. Four-wire system parameters of Case 1 ~ Case 3.

Case	Line Impedance	Neutral Inductor	PSU AC Voltage	Phase <i>a</i> Power	Phase <i>b</i> Power	Phase <i>c</i> Power
1				1 kW	1 kW	1 kW
2	1Ω + 2mH	10 mH	150Vrms	0.8kW	1 kW	1 kW
3				0.8kW	0.8kW	1 kW

Table 3-8. Four-wire system parameters of Case 4 ~ Case 7.

Case	Neutral Inductor	PSU AC Voltage	Phase <i>a</i> Power	Phase <i>b</i> Power	Phase <i>c</i> Power
4	10 mH		1 kW	1 kW	1 kW
5	10 mH	150 Vrms	1.1 kW	1.1 kW	1.1 kW
6	10 mH		1 kW	1.1 kW	1.2 kW
7	4 mH		1 kW	1.1 kW	1.2 kW

The total power of Case 5 ~ Case 7 is 3.3 kW, while that of Case 4 is 3 kW. Compared with Case 6, the neutral line inductor is reduced from 10mH to 4mH for Case 7. The time-domain test and the Nyquist plots using the derived 2×2 impedance matrix models of the four cases are shown in Figure 3-31 to Figure 3-34 respectively. Case 4 is stable, at the same time, there are no encirclements of (-1, 0) in its Nyquist plot. When its total power increases as in Case 5, around 5 Hz low-frequency oscillations occur. Keeping the same total power, by increasing the unbalanced level to 10 % as in Case 6, the system still has low-frequency oscillations. Its loci are like that of Case 5. If further decreasing its neutral inductor is as in Case 7, the system returns to a stable condition. The loci shrink to the right and have no encirclements of (-1, 0). The results of Case 4 ~ Case 7 verify the effectiveness of using the 2×2 impedance matrix model to assess system stability when the neutral line impedance is much larger than the phase line's impedance.

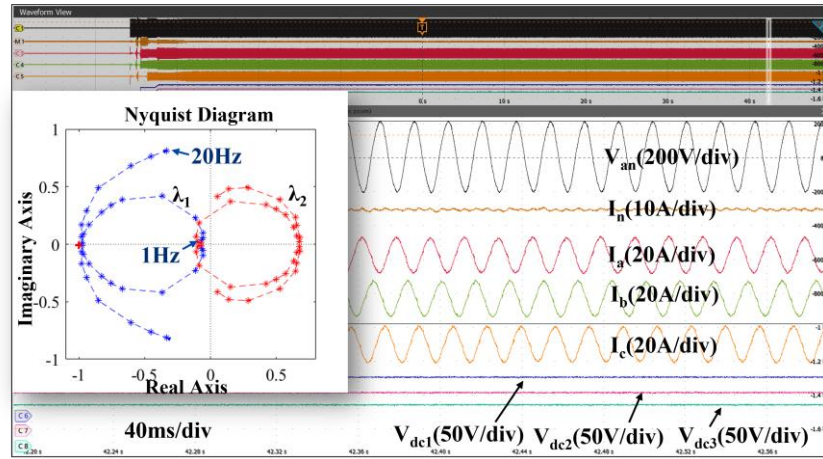


Figure 3-31 Test results and Nyquist plot of Case 4.

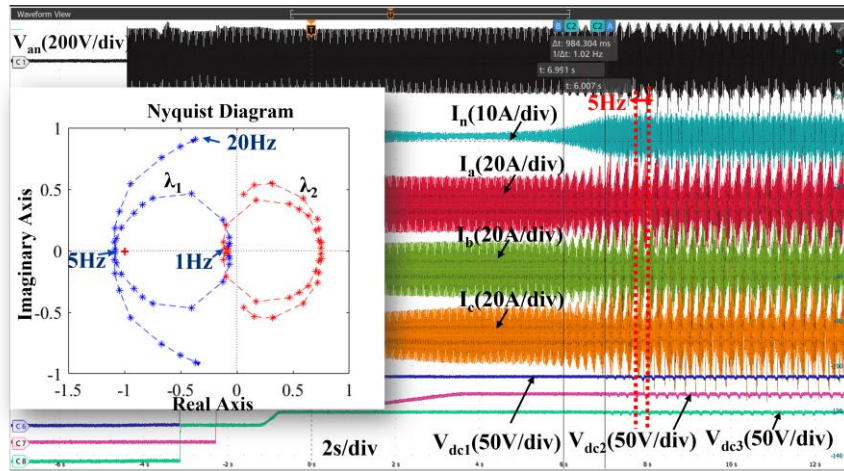


Figure 3-32 Test results and Nyquist plot of Case 5.

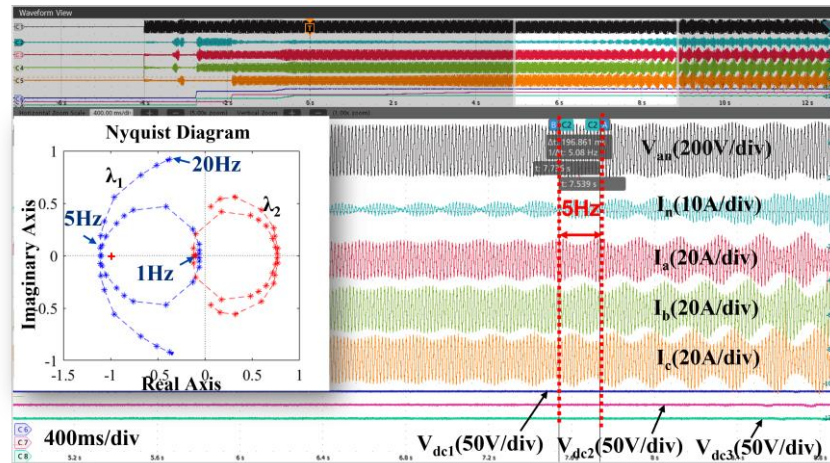


Figure 3-33 Test results and Nyquist plot of Case 6.

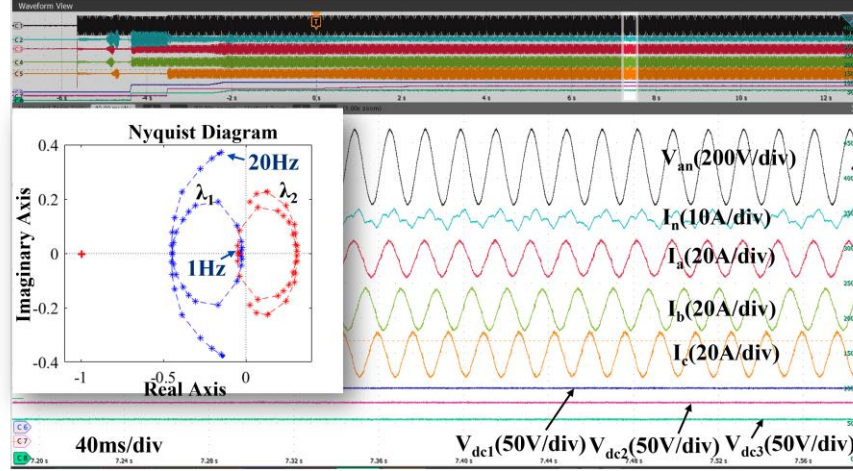


Figure 3-34 Test results and Nyquist plot of Case 7.

To verify the Bode plot criterion for the balanced cases of the four-wire system with a dominant neutral inductor, Case 8 and Case 9 are conducted. The system parameters are shown in Table 3-9. The neutral line inductor is increased from 4mH to 14mH in Case 9 compared to Case 8. The time-domain test results of the three cases are shown in Figure 3-35 and Figure 3-36. Case 8 shows stable operation while Case 9 exhibits around 4Hz low-frequency oscillations. Under a balanced condition, the stability of Case 8 and Case 9 can be assessed using the proposed model of an equivalent SISO system. With the measured PSU load impedance and neutral line impedance, the upstream impedance and downstream impedance of the equivalent SISO system can be calculated, which are shown in Figure 3-37. For Case 8, the load impedance gain is always larger than the upstream impedance gain, therefore the system should be stable. For Case 9, the gain of the upstream impedance and the gain of the downstream impedance have an intersection at around 4 Hz, at which the phase difference is larger than 180° , indicating an unstable operation. The impedance analysis using the Bode plot criterion of both Case 8 and Case 9 matches the time-domain test results.

Table 3-9 Four-wire system parameters of Case 8 and Case 9.

Case	PSU AC Voltage	Power	Neutral Inductor
8	150 Vrms	1 kW	4 mH
9			14 mH

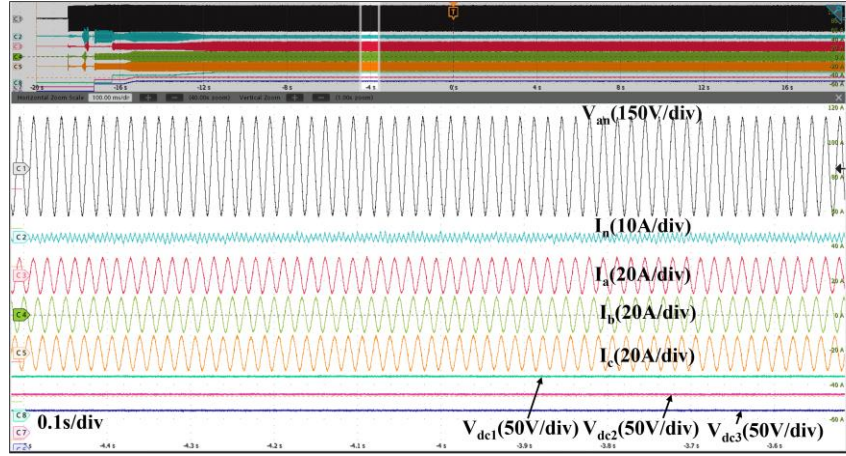


Figure 3-35 Test results of Case 8.

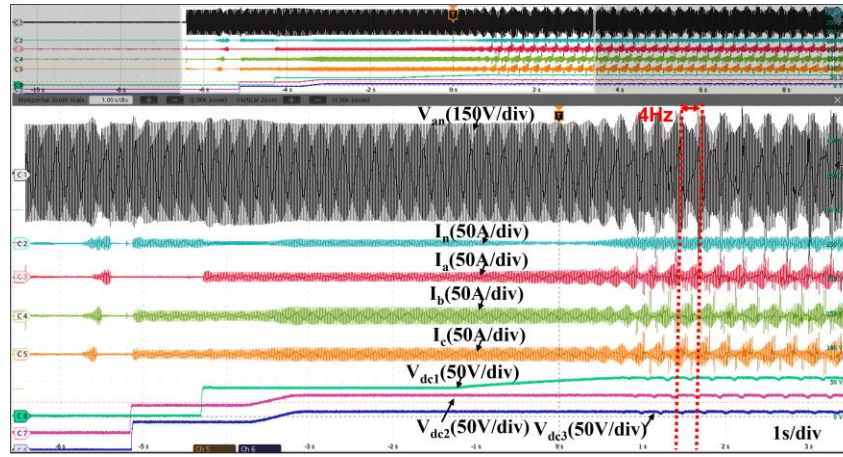


Figure 3-36. Test results of Case 9.

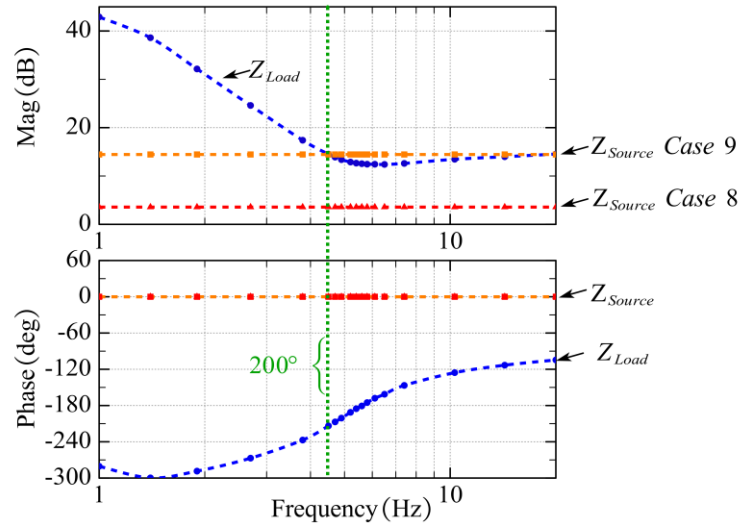


Figure 3-37. Upstream and downstream impedance plot of Case 8 and Case 9.

3.4.5 Discussion on the Neutral Line Design and System Impedance Specifications

When designing line impedance for medium to high-voltage grids, current limiting reactors must be considered alongside current capacity, length, and power loss. By increasing inductive reactance, an extra line reactor can limit fault current, slowing the rate of current rise and transient overvoltage during a fault. Inductive reactance must be low enough to prevent unacceptable voltage drops during normal operation, but high enough to restrict short circuits to switchgear ratings. In low-voltage distribution systems, such as those found in data centers, the application and design of such reactors vary. Some facilities may not use extra line reactors due to cost, construction, or availability considerations. The neutral wire in four-wire systems may still have a higher inductance due to a smaller cross-sectional area compared with the three-phase wires with a larger current capacity. Some facilities may choose to use the same reactor in all four wires to reduce fault current, while others may only place a high reactor in the neutral line to minimize voltage drops during normal operation and reduce cost. The analysis in the previous section shows that the stability impact of neutral wire impedance must be considered.

For the data center application, the unbalance is usually limited to a relatively small level (around 10 %). For such scenarios, (3-68) and (3-69) reveal that to achieve a similar stability margin, when increasing PSU load power by N times, the neutral inductor needs to be reduced to around $1/N$ of its original value. For example, for the studied system in simulation, with 5 kW per phase, the system can be stable with up to around 15 mH neutral inductance, while with 15 kW per phase, the system will not be stable if the neutral inductance increases above 5 mH.

On the other hand, the proposed impedance model provides another aspect that a larger neutral line inductor could help dampen potential high-frequency oscillations. The input filter of the PSU in Figure 2-1 is composed of a 15 μ H differential mode inductor L_{dm} , both 2 μ F for the C_e and C_d of the differential mode capacitor, and a 2 Ω damping resistor R_d . At high frequency (>1 kHz), all three phases' PSU loads' impedances are mainly shaped by their input EMI filter and current loop, which is not impacted by the operating points. Both upstream and downstream impedance are diagonally dominant in the high-frequency range. The system minor loop gain can be simplified as (3-70).

$$\mathbf{L}_{\text{sys}} \approx 3 \begin{bmatrix} Z_{Ndd} Y_{PSUadd} & 0 \\ 0 & Z_{Nqq} Y_{PSUaqq} \end{bmatrix} \quad (3-70)$$

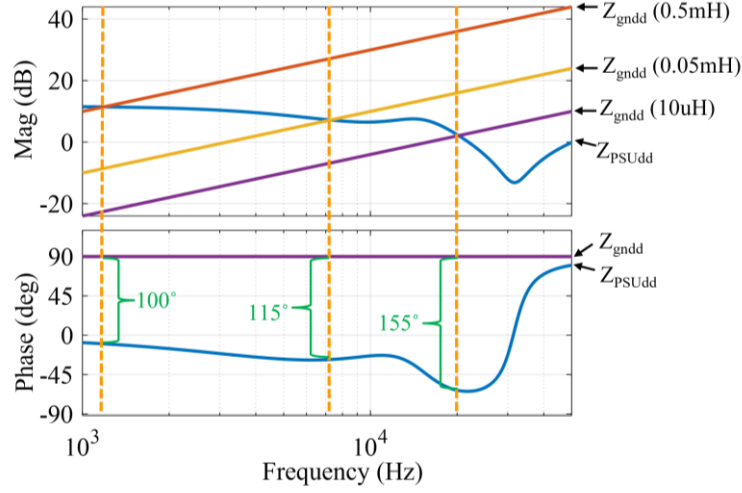


Figure 3-38 Z_{gndd} and Z_{PSUdd} with different neutral inductance.

At high frequency (> 1 kHz), the dd and qq elements of the neutral line and PSU impedance are equal, therefore, assessing (3-70) is equivalent to just checking either the dd or qq element of (3-70) using the Bode plot criterion. If using the dd element, the Z_{Ndd} and Y_{PSUadd} should be overplotted. Figure 3-38 shows a four-wire system with 5 kW per phase and with a different neutral inductor. With 10 uH of neutral inductance, high-frequency oscillations may occur with some perturbations because the system stability margin is just 25° . Increasing the neutral inductance largely increases the stability margin. With 0.5 mH of neutral inductance, the stability margin increases to 80° .

Therefore, when designing the neutral inductor, it is necessary to consider its detrimental impact on the system's low-frequency stability, and its positive impact on the system's high-frequency stability. If the load impedance is given, the impedance of the neutral inductor could be specified within a certain range considering its stability impact. Figure 3-39 provides an example of the design process. The neutral impedance is labeled as Z_n .

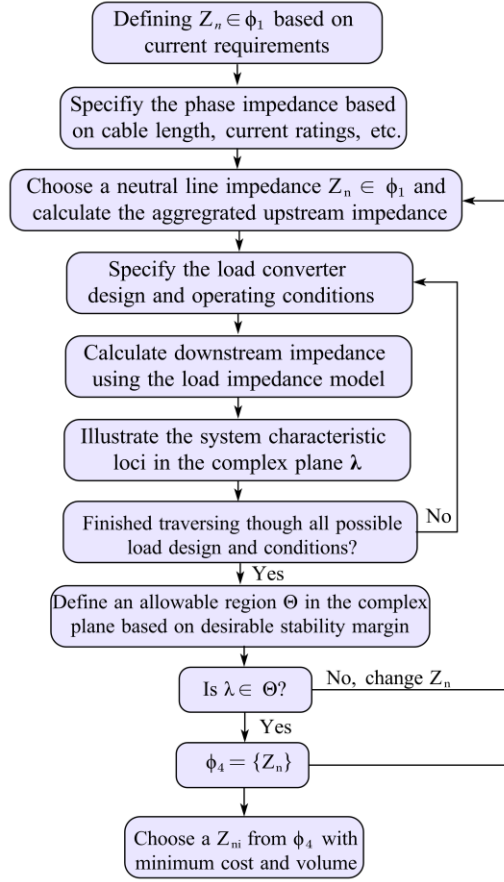


Figure 3-39 Process of designing neutral line inductor.

The proposed model provides a framework for analyzing the stability of a three-phase four-wire system, which can be useful in impedance specifications. If the source and cable impedance are known, the model can be used to map the characteristic loci in the complex plane to the PSU load impedance. Using this mapping, it is possible to define a forbidden region in the complex plane that represents the instability boundary of the system. Conversely, an allowable region can be defined based on the desired system stability margin. By designing the PSU converter control properly, manufacturers can ensure that the PSU impedance is shaped within the allowable region.

During system operation, if the characteristic loci enter the forbidden region, it may be necessary to adjust the PSU impedance to maintain stability. This can be accomplished using the proposed model, which can provide recommendations on the required adjustments based on the system parameters.

3.4.6 Analysis with Generator as the Power Source

Section C analyzed the scenarios with the source subsystem composed of an AC power supply with a certain line impedance. This section aims to cover the scenarios with the source subsystem composed of the backup generator and certain line impedance. The analysis is still based on the virtual d-q frame modeling concept. The source and load impedance models are

$$\mathbf{Z}_{\text{source}} = \begin{bmatrix} \mathbf{Z}_N + \mathbf{Z}_{ga} & \mathbf{Z}_N & \mathbf{Z}_N \\ \mathbf{Z}_N & \mathbf{Z}_N + \mathbf{Z}_{gb} & \mathbf{Z}_N \\ \mathbf{Z}_N & \mathbf{Z}_N & \mathbf{Z}_N + \mathbf{Z}_{gc} \end{bmatrix} \quad (3-71)$$

$$\mathbf{Y}_{\text{load}} = \begin{bmatrix} \mathbf{Y}_{\text{PSUa}} & 0 & 0 \\ 0 & \mathbf{Y}_{\text{PSUb}} & 0 \\ 0 & 0 & \mathbf{Y}_{\text{PSUc}} \end{bmatrix} \quad (3-72)$$

Compared with the AC power supply, which can be modeled as an ideal source in series with resistance and inductance, the generator impedance is generally modeled in the conventional d-q frame (corresponding to the original three phases). Therefore, its impedance model and physical meaning in the virtual d-q frame are not clear. Due to the time limit, this part has not been thoroughly studied. Instead, the generator side impedance in the virtual d-q frame is measured for system analysis.

(3-71) can also be written as

$$\mathbf{Z}_{\text{source}} = \begin{bmatrix} \mathbf{Z}_{gaa} & \mathbf{Z}_{gab} & \mathbf{Z}_{gac} \\ \mathbf{Z}_{gba} & \mathbf{Z}_{gbb} & \mathbf{Z}_{gbc} \\ \mathbf{Z}_{gca} & \mathbf{Z}_{gcb} & \mathbf{Z}_{gcc} \end{bmatrix} \quad (3-73)$$

The first row, second row, and third row of (3-73) are labeled as phase an's, phase bn's, and phase cn's d-q impedance respectively. To obtain the generator side impedance, which is a 6-by-6 matrix, it needs six independent measurements. Figure 3-40 shows the setup for the six measurements. Each two of them has the same setup configuration but linearly independent perturbation signals. For each measurement, the three phase-to-neutral voltages and currents on the generator side are measured. The phase of v_{an} is tracked, so the d-q component of all the voltages and currents can be obtained through Park's transformation. Then the small-signal d-q components of each can be obtained and used to solve the nine 2-by-2 elements in (3-73).

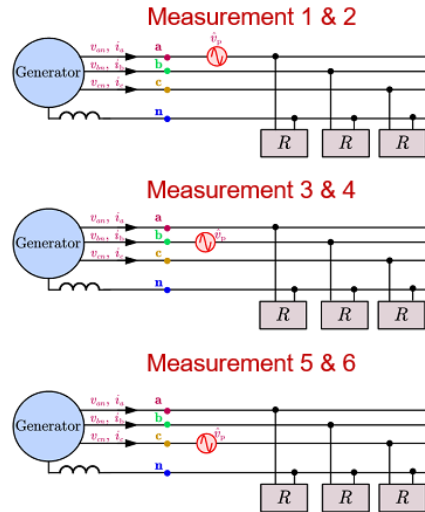


Figure 3-40 Measurement setup

Two cases are studied for this scenario. Table III-12 shows the system parameters.

Table 3-10 System Parameters

Case	AC voltage	DC voltage	Phase a	Phase b	Phase c	Neutral
1	181V _{phrms}	55V	1.3 kW	1.42 kW	1.56 kW	4 mH
2						10 mH

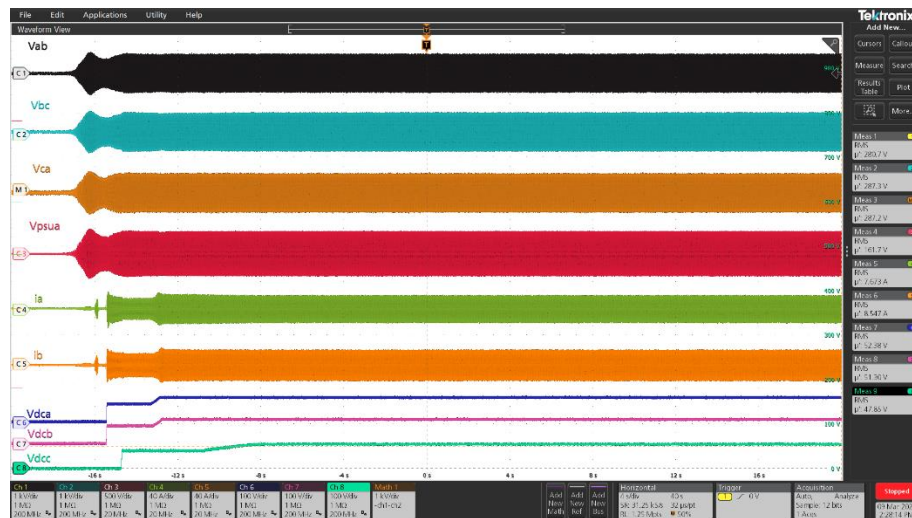


Figure 3-41 Time-domain test results of Case 1

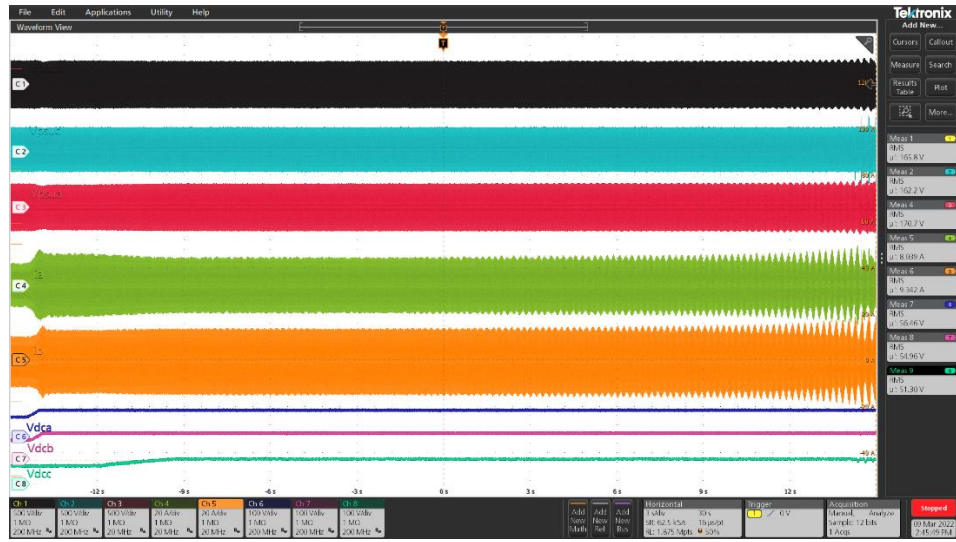
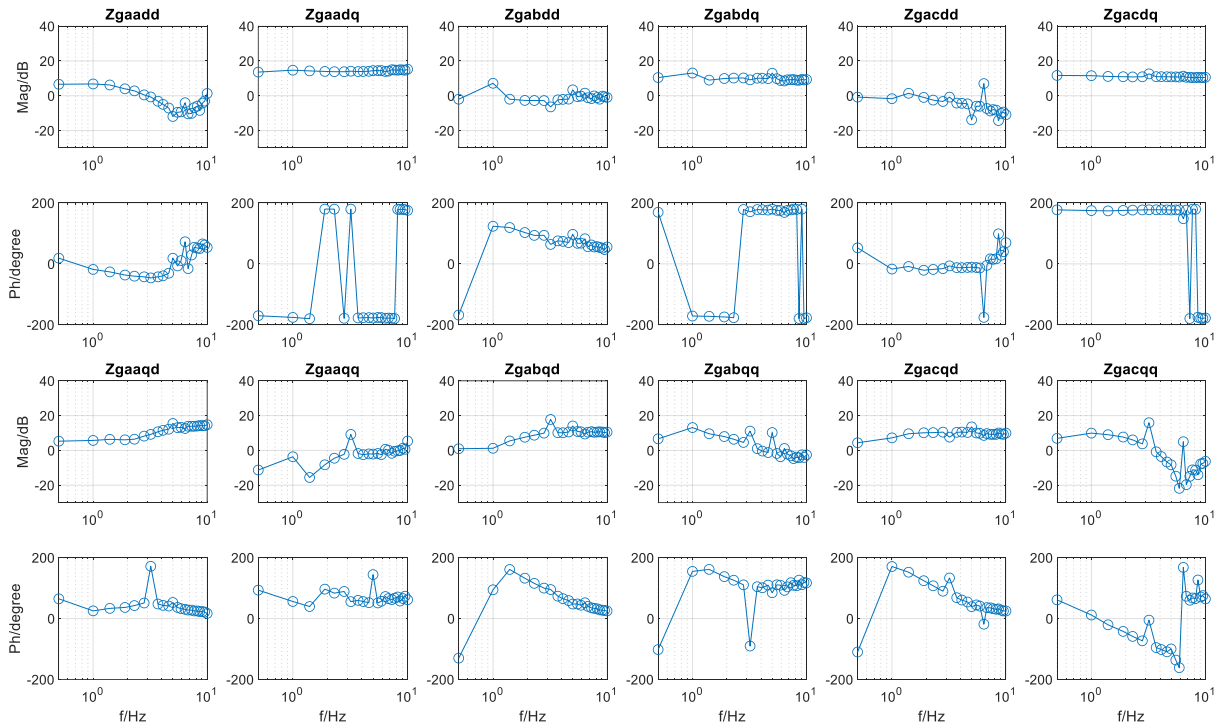


Figure 3-42 Time-domain test results of Case 2

From Figure 3-41 and Figure 3-42, Case 1 is stable, and Case 2 is unstable in the time domain. Using the proposed impedance measurement setup in Figure 3-40, the source side impedance of the two cases can be measured. Figure 3-43 shows the impedance measurement results of Case 2.



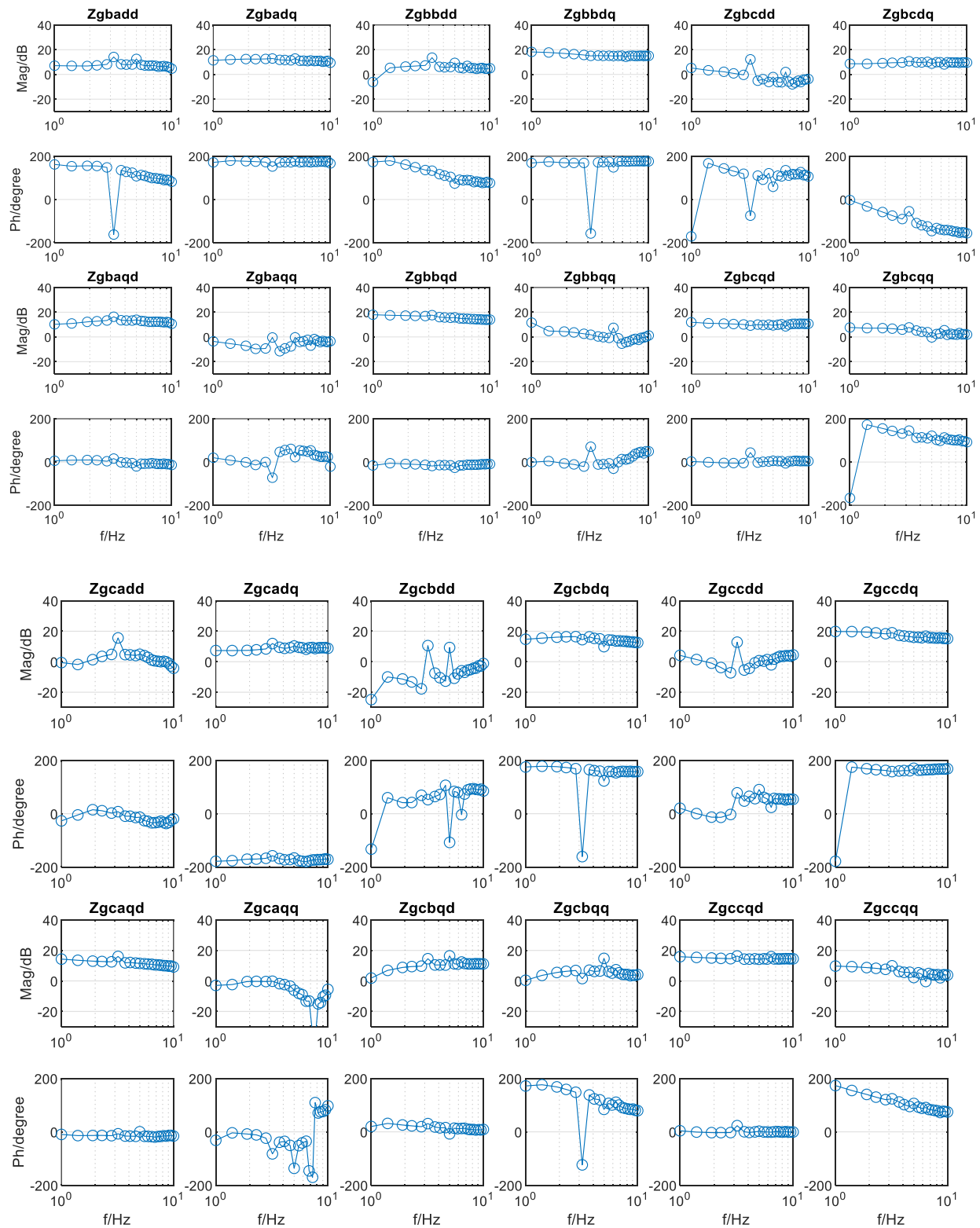


Figure 3-43 Source impedance of Case 2

Figure 3-44 (a) and (b) show the GNC results of Case 1 and Case 2 in the range of 1–20 Hz. The characteristic loci of Case 1 do not have encirclements of $(-1, 0)$ while the characteristic loci of Case 2 have, which are in accordance with the time-domain results. This shows that the proposed impedance model is still valid for systems with a three-phase source like a generator and that the neutral impedance has a significant impact on system stability like the scenarios with an AC power supply. Although at this point the meaning of the generator impedance in the virtual d-q frame is still not clear.

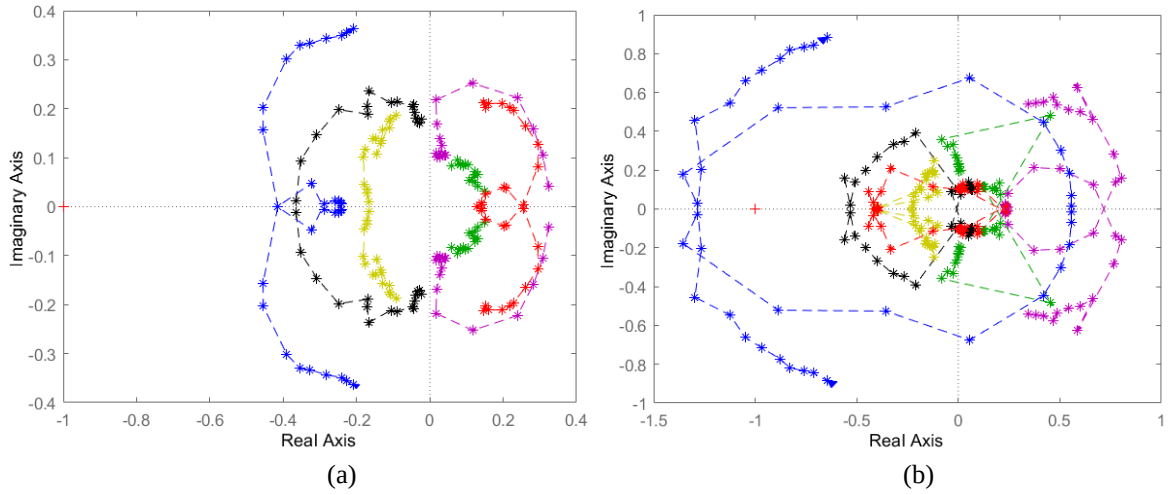


Figure 3-44 GNC results of (a) Case 1; (b) Case 2

3.5 Summary and Conclusions

Within the time-invariant framework, this section proposed impedance models of an AC system with single-phase PSU loads, including a single-phase system, three-phase three-wire system, and three-phase four-wire system for stability analysis purposes. Experiments verify the impedance models. Some useful conclusions are drawn below.

(1) For a single-phase system with a low line X/R ratio and the studied PSU loads, an operating point issue will occur before any small-signal instability. Small-signal instability may happen for a system with a high line X/R ratio. It can be analyzed using a 2×2 impedance model.

(2) The stability of a three-phase three-wire system with single-phase loads in either balanced or unbalanced conditions can be accurately predicted with 4×4 impedance models and GNC.

(3)The stability of a three-phase four-wire system with single-phase loads in either balanced or unbalanced conditions can be accurately predicted with 6×6 impedance models and GNC. It can be simplified as 2×2 impedance models for a system with dominant neutral line inductance. It can be further simplified as 1×1 impedance for three-phase-balanced cases; thus, the Bode plot criterion can be used. A high neutral line inductor design is detrimental to the system's low-frequency stability while it can help damp potential high-frequency resonance.

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Chapter 4

Voltage Loop Gain Modeling and Stability Analysis of AC Systems with Single-Phase PSUs

4.1 Introduction

The previous two chapters utilize the impedance model to analyze the PSU system. This chapter takes a different perspective, loop gain modeling. The loop-gain approach offers unique advantages in some practical implementations. For example, systems with the freedom to configure the converter controller could easily enable its digital controller's loop gain measurement function without the cost and design challenge of adding a dedicated instrument to measure system impedance. The measurement data can then be sent to a central controller to assess the system's stability. Also, in the format of assessing stability, the loop gain result is a scalar, so a Bode plot can be used, while impedance analysis results are in matrix format, so a multiple loci Nyquist plot in the complex plane is necessary [1], [2]. Practically, it may be easier to design an automatic stability margin detection algorithm in a Bode plot than in a Nyquist plot [3], [4].

Although implementing the loop gain approach seems compelling, there is currently a lack of an accurate loop gain model for single-phase PFCs, as their ac-dc time-varying operation presents a challenge. The loop gain analysis method is based on linear system theory. However, power-electronics converters and systems are inherently nonlinear due to their switching networks, which necessitates linearization. Moreover, the process of linearization requires an equilibrium operating point. For a dc-dc converter, a quasi-static approximation can be applied to simplify the modeling of the time-varying voltage and current in the switching terminal, resulting in a time-invariant averaged model that is valid up to half of the switching frequency [5]. For single-phase PFCs, a similar approximation is applied for the switching dynamics. However, the input AC operation still introduces a time-varying component. In most industrial practices, a second quasi-static approximation is assumed by averaging within an AC line cycle [6]-[8]. In other words, freezing the operating points as the root-means-square (RMS) values of the ac components allows for the

realization of a DC equilibrium operating point [9], [10]. While this approximation can work to some extent in practice, it is theoretically unjustified and may not always be accurate or valid [11]. For example, it cannot account for the impact of the source side dynamics on the loop gain, particularly in a three-phase distribution system with phase differences among the three phases. With existing knowledge, the specific shape and characteristics of a single-phase PFC loop gain in an AC system are not fully understood.

Notably, the d-q-frame modeling method, based on rotating frame theory, is a commonly used solution in three-phase systems for transforming time-varying state variables to time-invariant ones. This method has also been extended to single-phase system modeling by creating virtual frames [12]-[14]. Another approach for modeling PFC converters completely disregards the time-invariant assumption and directly analyzes the system under the time-periodic operation. This approach, known as harmonics linearization, performs linearization along the periodic trajectories of the converter [15]-[17]. Based on harmonics linearization, sequence impedance modeling of PFC is further developed [18]. The harmonic state space approach is another modeling method based on the linear time-periodic theory [19]. Only the quasi-static approximation has been employed for single-phase PFC for loop gain analysis. The d-q framework and harmonics linearization methods are only explored for impedance modeling of PFC converters [15], [16].

While stability assessment based on loop-gain measurement is a common practice in the industry, it primarily focuses on a single converter. However, the understanding of loop gain formation remains relatively unexplored when considering AC systems with single-phase loads. The quasi-static approximation approach lacks accuracy for single-phase systems, and no models describe its loop gain in a three-phase system context. This chapter aims to bridge this gap by presenting a methodology that explains the formation of PFC loop gain in single-phase and three-phase AC systems, thereby contributing to the advancement of stability assessment at the system level. The developed model can be used during the system design stage and as preliminary knowledge for online stability monitoring of such systems. It could also be extended to other single-phase converters, such as photovoltaic (PV) inverters.

4.2 PFC Dc Voltage Loop Gain Model for Different Systems Configurations

The small-signal modeling approach of the single-phase PFC converter in different kinds of systems is shown in detail in Chapter 3. Here, the small-signal model is directly used to derive the dc voltage loop gain model. Figure 4-1 (a) shows the small-signal model in the virtual d-q frame. $\mathbf{G}_{id}$, $\mathbf{Z}$, $\mathbf{G}_{vd}$, and $\mathbf{G}_{vv}$, are the power stage transfer functions with input variables as input d-q voltage, d-q duty cycle, and state variables as d-q inductor current and output dc voltage. $\mathbf{G}_\theta$, $\mathbf{G}_{ci}$, $\mathbf{G}_{cv}$, $\mathbf{G}_v$, and $\mathbf{G}_{del}$, denote the dynamics of the zero-crossing detection-based input-voltage phase-tracking unit, current controller, output voltage controller, input voltage feedforward control, and digital control delay, respectively. The detailed expressions of each transfer function matrix are shown in Chapter 2. The studied frequency range is low (< 50 Hz) due to the low voltage control bandwidth, so the input EMI filter's dynamics are neglected in the following modeling. $\mathbf{Z}_T$ denotes the dynamics of the source side, which could include the cable impedance and other PFCs' coupling impact. $\mathbf{Z}_T$ is defined as

$$\hat{\mathbf{v}}_{PFC} = \mathbf{Z}_T \hat{\mathbf{i}}_{PFC}. \quad (4-1)$$

With the linear dynamics diagram in Figure 4-1 (a), the PFC small-signal model can be written as

$$\begin{cases} \hat{\mathbf{i}}_L = \mathbf{Z}^{-1} \hat{\mathbf{v}}_{in} + \mathbf{G}_{id} \hat{\mathbf{d}} \\ \hat{\mathbf{v}}_{dc} = \mathbf{G}_{vv} \hat{\mathbf{v}}_{in} + \mathbf{G}_{vd} \hat{\mathbf{d}} \\ \hat{\mathbf{i}}_{Lref} = \mathbf{G}_\theta \hat{\mathbf{v}}_{in} + \mathbf{G}_{cv} \Delta \hat{\mathbf{v}}_{dc} \\ \hat{\mathbf{d}} = \mathbf{G}_{del} (\mathbf{G}_v \hat{\mathbf{v}}_{in} + \mathbf{G}_{ci} (\hat{\mathbf{i}}_{Lref} - \hat{\mathbf{i}}_L)) \\ \hat{\mathbf{v}}_{in} = \mathbf{Z}_T \hat{\mathbf{i}}_L \end{cases} \quad (4-2)$$

The PFC's voltage loop gain can be derived from (4-2) as

$$\begin{aligned} \mathbf{T}_v &= \frac{\hat{\mathbf{v}}_{dc}}{\Delta \hat{\mathbf{v}}_{dc}} = \frac{\hat{\mathbf{v}}_{dc}}{\hat{\mathbf{v}}_{dc_{ref}} - \hat{\mathbf{v}}_{dc}} \\ &= \mathbf{G}_{vd} \left((\mathbf{G}_{del} (\mathbf{G}_v + \mathbf{G}_{ci} \mathbf{G}_\theta) + \mathbf{G}_{vv}) \mathbf{Z}_T - \mathbf{G}_{del} \mathbf{G}_{ci} \right) \cdot (\mathbf{I} + \mathbf{G}_{id} \mathbf{G}_{del} \mathbf{G}_{ci} - (\mathbf{G}_{id} \mathbf{G}_{del} (\mathbf{G}_v + \mathbf{G}_{ci} \mathbf{G}_\theta) + \mathbf{Z}^{-1}) \mathbf{Z}_T)^{-1} \mathbf{G}_{id} + \mathbf{I} \quad (4-3) \\ &= f(\mathbf{Z}_T) \end{aligned}$$

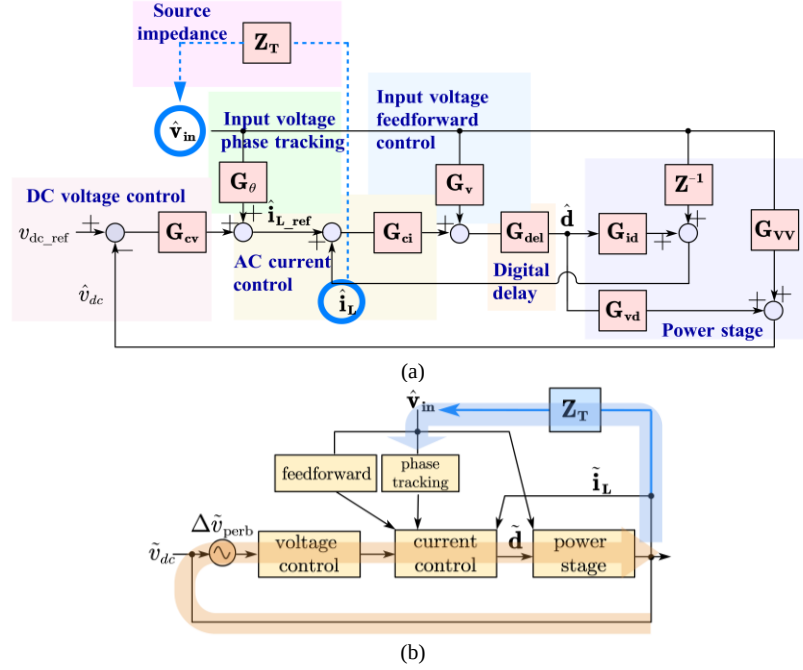


Figure 4-1 Linear dynamics of the single-phase PFC: (a) detailed model; (b) simplified model to highlight the perturbation propagation path.

In Figure 4-1 (a), Z_T causes a perturbation path from the PFC input current to its input voltage and consequently affects the voltage loop gain through the phase tracking, feedforward units, and power stage, as illustrated in Figure 4-1 (b). If Z_T is negligible, the disturbances will not affect the input voltage, and the loop gain will remain unaffected by external components. The source side's specific structure determines the disturbances' propagation path, leading to variations in Z_T . Essentially, Z_T indicates how other components in the system impact the voltage loop. This part derives Z_T for the different system configurations: a single-phase system, a three-phase three-wire system, and a three-phase four-wire system.

4.2.1 Analysis of Z_T for a Single-Phase System

For a single-phase system, as shown in Figure 3-1, Z_T is equal to the d-q impedance of the source side with a minus sign, as shown in (4-4).

$$Z_T = Z_{T1} = - \begin{bmatrix} sL_g + R_g & -\omega_0 L_g \\ \omega_0 L_g & sL_g + R_g \end{bmatrix} \quad (4-4)$$

4.2.2 Analysis of Z_T for a Three-Phase Three-Wire System

The small-signal model of a three-phase three-wire system in Figure 3-6 is as follows,

$$\begin{bmatrix} \hat{v}_{abd} \\ \hat{v}_{abq} \end{bmatrix} = -\mathbf{Z}_{ga} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \mathbf{Z}_{gb} \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix}, \quad (4-5)$$

$$\begin{bmatrix} \hat{v}_{bcd} \\ \hat{v}_{bcq} \end{bmatrix} = -\mathbf{Z}_{gc} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} - (\mathbf{Z}_{gb} + \mathbf{Z}_{gc}) \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix}, \quad (4-6)$$

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} = \begin{bmatrix} \hat{i}_{ad} \\ \hat{i}_{aq} \end{bmatrix} + \mathbf{Y}_{pfcC} \begin{bmatrix} \hat{v}_{abd} \\ \hat{v}_{abq} \end{bmatrix} + \mathbf{Y}_{pfcC} \begin{bmatrix} \hat{v}_{bcd} \\ \hat{v}_{bcq} \end{bmatrix}, \quad (4-7)$$

$$\begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} = \mathbf{Y}_{pfcB} \begin{bmatrix} \hat{v}_{bcd} \\ \hat{v}_{bcq} \end{bmatrix} - \begin{bmatrix} \hat{i}_{ad} \\ \hat{i}_{aq} \end{bmatrix}. \quad (4-8)$$

(4-5) ~ (4-8) can also be pictured using Figure 4-2. $\mathbf{Z}_T$ is defined as (4-10) for such a three-phase three-wire system. It can be derived from Figure 4-2 by breaking the loop at the input of $\mathbf{i}_a$. From the definition, $\mathbf{Z}_T$ is also the d-q impedance with a reversing sign of the source side if looking at the input interface of the PFC connected between Phase A and Phase B.

$$\hat{v}_{ab} = \mathbf{Z}_T \hat{\mathbf{i}}_a \quad (4-9)$$

$$\begin{aligned} \mathbf{Z}_T &= \mathbf{Z}_{T2} \\ &= (\mathbf{I} + \mathbf{Z}_{ga}\mathbf{Y}_{pfcC} - \mathbf{BA}^{-1}\mathbf{Z}_{gc}\mathbf{Y}_{pfcC})^{-1}(-(\mathbf{Z}_{ga} + \mathbf{Z}_{gb}) - \mathbf{BA}^{-1}\mathbf{Z}_{gb}) \end{aligned} \quad (4-10)$$

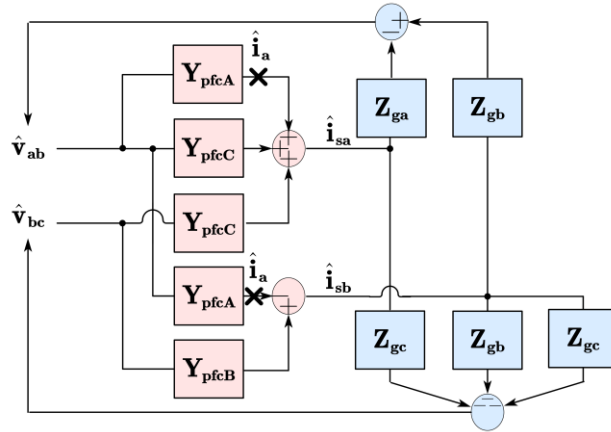


Figure 4-2 Linear dynamics blocks diagram of a three-phase three-wire system.

where

$$\mathbf{A} = \mathbf{I} + \mathbf{Z}_{gc}\mathbf{Y}_{pfcC} + \mathbf{Z}_{gb}\mathbf{Y}_{pfcB} + \mathbf{Z}_{gc}\mathbf{Y}_{pfcB} \quad (4-11)$$

$$\mathbf{B} = \mathbf{Z}_{ga}\mathbf{Y}_{pfcC} - \mathbf{Z}_{gb}\mathbf{Y}_{pfcB} \quad (4-12)$$

With (4-10), the loop gain model of PFC connected to Phase A and Phase B can be calculated using (4-3). From the expression of $\mathbf{Z}_T$ in (4-10), the PFCs connected to all three lines are coupled through the source impedance. Higher line impedance causes a stronger coupling among the three phases.

4.2.3 Analysis of $\mathbf{Z}_T$ for a three-phase four-wire system

The small-signal model of a three-phase four-wire system in Figure 3-12 is as follows,

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = -\mathbf{Z}_{ga} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (4-13)$$

$$\begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = -\mathbf{Z}_{gb} \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (4-14)$$

$$\begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = -\mathbf{Z}_{gc} \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} + \mathbf{Z}_N \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \quad (4-15)$$

$$-\begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} \quad (4-16)$$

$$\hat{\mathbf{i}}_{sa} = \mathbf{Y}_{pfcA} \hat{\mathbf{v}}_{an} \quad (4-17)$$

$$\hat{\mathbf{i}}_{sb} = \mathbf{Y}_{pfcB} \hat{\mathbf{v}}_{bn} \quad (4-18)$$

$$\hat{\mathbf{i}}_{sc} = \mathbf{Y}_{pfcC} \hat{\mathbf{v}}_{cn} \quad (4-19)$$

(4-13) ~ (4-19) can also be plotted as Figure 4-3. $\mathbf{Z}_T$ is defined as (4-20) for the three-phase four-wire system. It can be derived as (4-21) according to Figure 4-3 by breaking the loop at the input of $\hat{\mathbf{i}}_{sa}$.

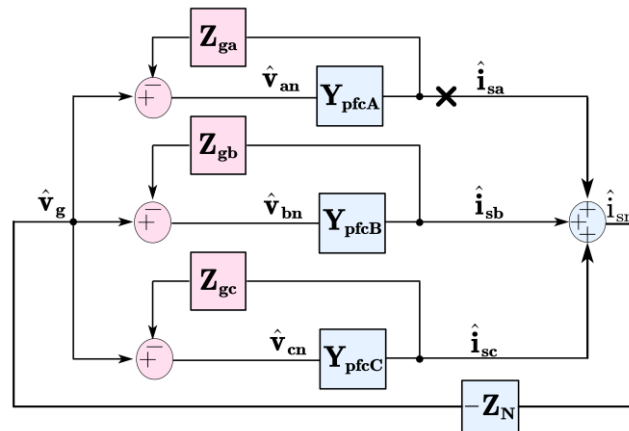


Figure 4-3 Linear dynamics blocks diagram of a three-phase four-wire system.

$$\hat{v}_{an} = \mathbf{Z}_T \hat{i}_{sa} \quad (4-20)$$

$$\mathbf{Z}_T = \mathbf{Z}_{T3} = -\left(\left(\mathbf{I} + \mathbf{Z}_N(\mathbf{Z}_{gb} + \mathbf{Z}_{pfcB})^{-1} + \mathbf{Z}_N(\mathbf{Z}_{gc} + \mathbf{Z}_{pfcC})^{-1}\right)^{-1} \mathbf{Z}_N + \mathbf{Z}_{ga}\right) \quad (4-21)$$

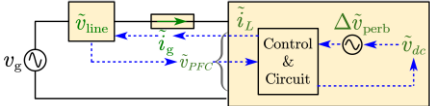
Some three-phase four-wire systems are designed with a higher neutral line impedance to limit short-circuit fault current or due to the use of a smaller cross-sectional area with lower current capacity. The phase impedance is much smaller and is neglected. So $\mathbf{Z}_T$ can be approximated as (4-22).

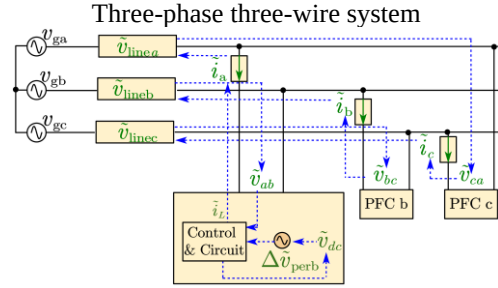
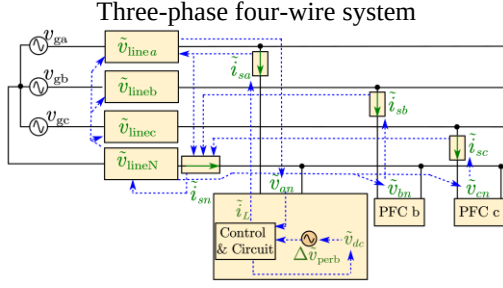
$$\mathbf{Z}_T = \mathbf{Z}_{T4} = -\left(\mathbf{I} + \mathbf{Z}_N(\mathbf{Y}_{pfcB} + \mathbf{Y}_{pfcC})\right)^{-1} \mathbf{Z}_N \quad (4-22)$$

With (4-21) and (4-22), the loop gain model of PFC at Phase A can be calculated using (4-3). With negligible neutral line impedance, the PFC connected to the three phases is decoupled, equivalent to the analysis of three single-phase systems. The three phases are coupled through a nonzero neutral line impedance. The inclusion of the neutral line impedance has two impacts on the loop gain: the neutral line impedance itself and the admittance of the other two phases' PFC's dynamics coupled dynamically through this path. This physical interpretation can be seen from the expression of $\mathbf{Z}_T$.

Table 4-1 summarizes $\mathbf{Z}_T$'s main characteristics, and the perturbation propagation paths in different scenarios.

Table 4-1. Comparison of $\mathbf{Z}_T$ in different configurations of the systems.

System Configuration and Perturbation Paths (blue dotted lines)	Main characteristic
Single-phase system 	▪ $\mathbf{Z}_T$ indicates the line impedance in the dq frame. ▪ The external perturbation travels through the line impedance.



- Z_T represents the overall effect of the perturbation paths: the perturbation travels through the current in phase A, causing a voltage disturbance across both line A and the neutral line impedance. This perturbation then propagates to the voltages over the lines and PFCs connected to phases B and C, affecting the current in lines B and C. This eventually adds up and returns as the neutral line current, impacting the input voltage of PFC a and entering the feedback loop.
- If there is no neutral line impedance, it equals three decoupled single-phase systems.
- For PFC a, the other two phases impact its loop gain through the neutral line impedance. Such an effect is added up to line A impedance.
- Z_T represents the overall effects of the perturbation paths: perturbation within the voltage loop of PFC a affects the input current first, then induces disturbances in the voltage across line A. This perturbation further disturbs the input voltage and current of PFCs c and b due to the line impedance of each phase. Eventually, these perturbations impact the input voltage of PFC a because it is connected between line A and line B.
- For PFC a, the other two phases impact its loop gain through phase line impedance. For example, PFC a and PFC c share the line impedance Z_{ga} and Z_{gc} . With higher Z_{ga} or Z_{gc} , the impact of PFC c on PFC a's controller is greater.

4.3 Simulation Verification

In this section, several case studies are conducted in PLECS to verify the loop gain model proposed in Section 4.2 for a single-phase system, a three-phase three-wire system, and a three-phase four-wire system. The results in the frequency domain are compared. The results obtained through quasi-static approximation are compared for the single-phase system, showing that the proposed model is much more accurate than the quasi-static approximation method. Meanwhile, loop gain is also an indicator of the load transient response behavior. The results in a time-domain simulation are also compared. Furthermore, the quasi-static approximation cannot be used in analyzing the PFC in a three-phase system context because it cannot consider the phase difference among the three phases.

In this study, the dc-dc stage of the converter is designed to be a buck converter with dual-loop control shown in Figure 4-4 for two reasons. One is the dynamic impact of the buck converter on its front-end PFC is similar to that of an isolated LLC converter, which behaves like a negative resistor [33], [34]. And the buck converter is a lot simpler to model. The parameters of the front-

end PFC and the cascaded buck converter are shown in Table 2-1. Table 4-2 summarizes the system's parameters for the case study conducted as follows.

Table 4-2. System parameters for loop gain model verification in simulation.

No. Case	System configuration	Source Impedance (phase)	Source Impedance (neutral)	PFC terminal voltage
Case 1	Single-phase	0	-	340 V
Case 2		$1.5 \Omega + 4 \text{ mH}$		
Case 3		$1.5 \Omega + 11.9 \text{ mH}$		
Case 1	Three-phase-three-wire	$0.5 \Omega + 390 \text{ uH}$	-	340 V
Case 2		$0.5 \Omega + 6 \text{ mH}$		
Case 3		$0.5 \Omega + 390 \text{ uH}$		
Case 1	Three-phase-four-wire	0	6 mH	330 V
Case 2		$0.5 \Omega + 390 \text{ uH}$	3 mH	
Case 3		$0.5 \Omega + 390 \text{ uH}$	6 mH	
Case 4		$0.5 \Omega + 390 \text{ uH}$	9 mH	

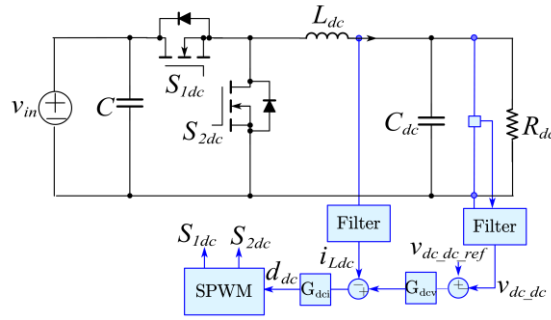


Figure 4-4 The cascaded dc-dc converter.

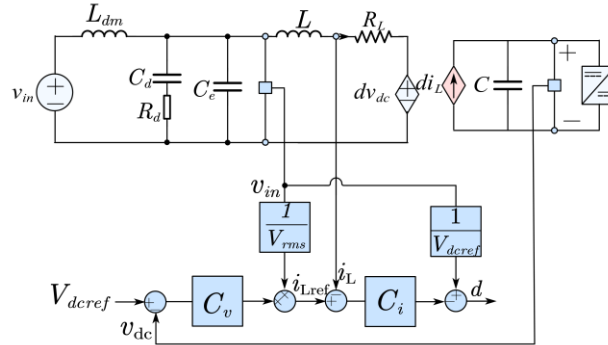


Figure 4-5 Averaged model of the PFC with quasi-static approximation.

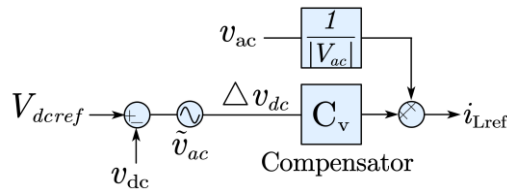


Figure 4-6 Process to extract the dc voltage loop gain of one PFC converter.

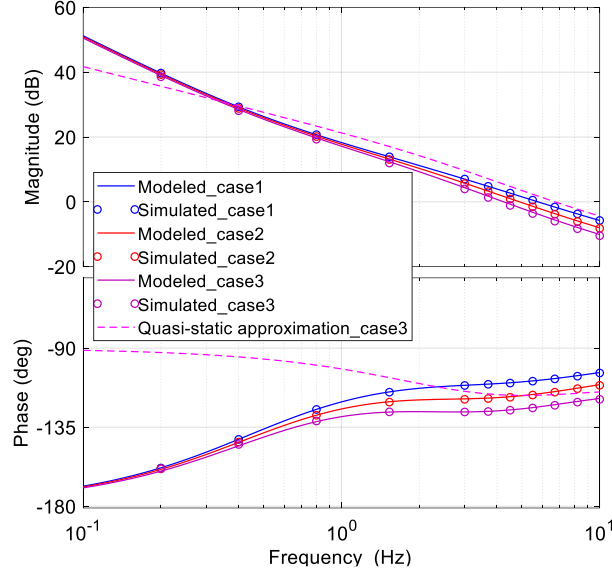


Figure 4-7 Simulation and modeled results of the single-phase system study.

4.3.1 Model verification of a single-phase system

In the following sections, the simulation results are obtained in Simulink/PLECS Blockset, with the frequency response of the analytical model obtained using MATLAB scripts.

The simulated system has a configuration as Figure 3-1. Figure 4-5 shows the model by the quasi-static approximation. The averaged model of the converter power stage is averaged again over a line cycle to eliminate its dependency on time. The input voltage is set as the RMS values of the original ac source [9], [10]. The output of the original PFC voltage controller is the current reference magnitude, which is a dc value with small double-line frequency ripples. In the approximated dc circuit, the double line frequency ripples of the dc side voltage are ignored. Such an approximation can capture some info about the loop gain, but certainly not the precise ones. Figure 4-6 shows the block design to extract the PFC loop gain in simulation. During an ac-dc operation, an ac injection with a magnitude around 3 % of the dc voltage average value is added into the loop. Then the voltage response v_{dc} and Δv_{dc} are collected for different frequency component injections. The magnitude of the corresponding frequency components is extracted by the Fast Fourier Transform (FFT). Then the simulated loop gain can be calculated using (4-23).

$$T_{v_sim} = \frac{\hat{v}_{dc}(s)}{\Delta \hat{v}_{dc}(s)} \quad (4-23)$$

Three cases are conducted. The parameters are shown in Table 4-2. The grid side voltage v_g is modified, and the PFC input voltage is kept at 340 V. The blue, red, and pink curves in Figure 4-7 show the simulated results and the results obtained through the proposed model (4-3) and (4-4), which are accurate for all three cases. The dotted curve shown in Figure 4-7 is the modeled results of Case 3 using the quasi-static approximation when freezing the PFC input voltage as the RMS values of its ac input. The cutoff frequency and phase margin of the ac simulation results are 4 Hz and 55° , while the results of dc approximation are 7 Hz and 65° . The loop gain using quasi-static approximation does not match the actual loop gain.

The reason for a negative feedback loop is to achieve a desired output despite any disturbance or variations of components [11]. For a closed loop system, the transfer function from a disturbance to the output has a factor of $1/(1+T_v)$. Therefore, loop gain also indicates how well the system output can reject disturbance. A larger phase margin of the loop gain can cause a small overshoot and ringing of a system transient response. Therefore, a more accurate loop gain model can quantify the load transient response more accurately. To verify this, a step response test is done using different models. Figure 4-8 (d) is the time-domain simulation of Case 3 with a load step. A step from 48 V to 38 V at 2 seconds is applied to the cascaded dc-dc converter's output voltage reference to change the output load power from 5 kW to 3.1 kW. The blue curve shows the voltage response v_{dc} when applying load step change in Figure 4-8 (a). The red curve is the result after averaging v_{dc} every 120 Hz to filter the 120 Hz components. The yellow curve is the simulation results using the averaged model in Figure 4-8 (c) derived from the d-q frame concept. And the purple curve is the simulation result of the corresponding quasi-static approximation model in Figure 4-8 (b), that is, by applying a dc source with a value of the RMS values of the original ac voltage as the input voltage. Compared with the step response results using the quasi-static approximation, the results obtained by the d-q model are much closer to the actual PFC simulation results.

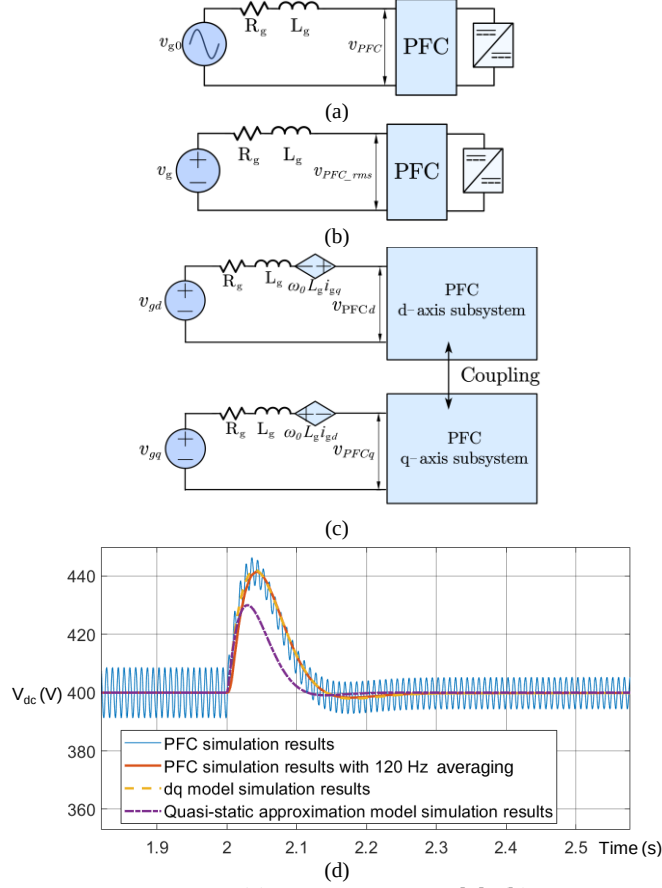


Figure 4-8 Load step response comparisons: (a) PFC average model; (b) quasi-static approximation; (c) PFC average model in dq frame; (d) load step response of the different models in (a)~(c).

4.3.2 Model verification of a three-phase three-wire system

Two cases are conducted to verify the loop gain model proposed for a three-phase three-wire system. The parameters of the system are shown in Table 4-2. The source impedance for each phase increases from $0.5 \, \Omega + 390 \, \mu\text{H}$ to $0.5 \, \Omega + 6 \, \text{mH}$ for Case 2 compared with Case 1, and the grid side voltage is adjusted so the PFC input voltage is 340 V. The three phases are balanced, and the three PFCs work at rated power conditions. The loop gain extraction method is the same as in Figure 4-6. Figure 4-9 shows the loop gain of the PFC converter connected between Phase A and Phase B. The calculation results are based on (4-3) and (4-10) using the proposed model. The proposed model's accuracy is verified by matching the simulated and modeled results. Comparing Case 1 and 2, increasing grid impedance would decrease the phase margin.

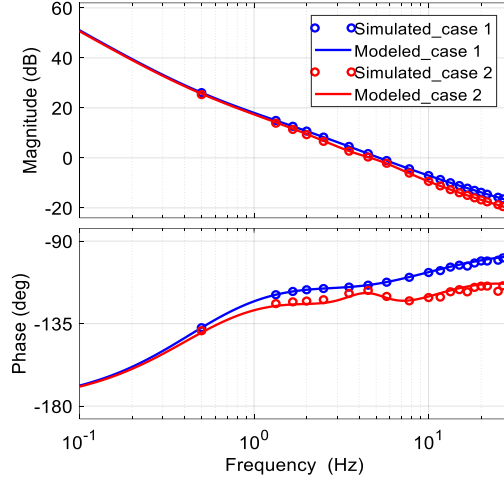


Figure 4-9 Simulation and modeling results of the three-phase three-wire system.

4.3.3 Model verification of a three-phase four-wire system

Four cases are conducted in the simulation study to verify the loop gain model proposed for a three-phase four-wire system. The system configuration is the same as in Figure 3-12. The system parameters are shown in Table 4-2. The source side impedance, including the phase line impedance and the neutral line impedance, are changed for the four cases. The three phases are balanced, and the three PFCs work at rated power conditions. The loop gain extraction method is the same as in Figure 4-6. Figure 4-10 shows the loop gain of Phase A's PFC using the proposed models and the simulation results. For Case 2, Case 3, and Case 4, the modeled results are calculated based on (4-3) and (4-21). For Case 1, the modeled result is calculated based on (4-3) and (4-22). The results through the proposed model are remarkably close to the simulation results, which verify the accuracy of the proposed model. The different loop gain results of the four cases also show the source dynamics could impact the PFC loop gain. For example, the increase of source side impedance, including the phase impedance and neutral line impedance, decreases the phase margin of the PFC converter. This is also compatible with common experience.

4.3.4 Pole-Zero Analysis of the Loop Gain Model

In the previous section, the accuracy of the loop gain was demonstrated through simulation verification, with the frequency response of the analytical model obtained using MATLAB scripts. The models are highly practical, and any changes made to the system's parameters in the codes are immediately reflected in the results, making it easy to identify the effects of system parameters on

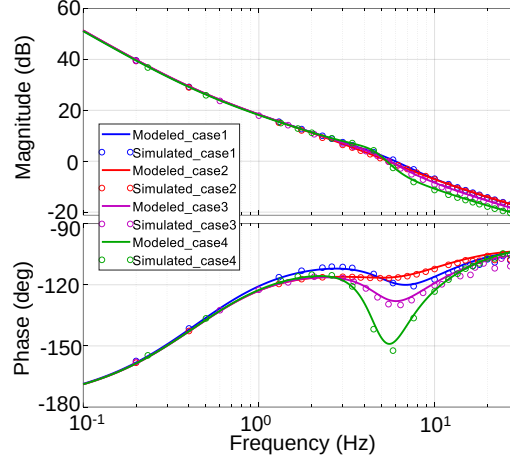


Figure 4-10 Simulation and modeling results of the three-phase four-wire system.

the model's performance. While the current model is highly applicable, a model with explicit zero and pole expressions would also be advantageous, allowing for quick identification of system parameter impacts and providing valuable insights. It is worth noting that the full model in Section II involves high orders, given the system's nonlinearity and complexity. To obtain a simplified expression, certain assumptions must be made, and some loss of accuracy is unavoidable.

When modeling the PFC converter, aligning the input voltage with the d -axis results in the q -axis operating point V_q and I_q being nearly zero under unity power factor operation. If the coupling effect of the source side q -axis on the d -axis is relatively small, the overall q -axis model can be neglected, making the model more straightforward. Furthermore, the cascaded dc-dc converter load can be simplified as a negative resistor in parallel with its input capacitance at low frequency, given its high voltage control bandwidth. With these two approximations, the resulting small-signal model of the single-phase PFC converter can be expressed as (4-24).

$$\begin{cases} \hat{v}_d = sL\hat{i}_d + \hat{d}_d V_{dc} + D_d \hat{v}_{dc} \\ D_d \hat{i}_d + \hat{d}_d I_d = \frac{\hat{v}_{dc}}{Z_{dc}} = \hat{v}_{dc} \left(-\frac{1}{R_{dc}} + sC_{total} \right) \\ \hat{d}_d = -\frac{1}{V_{dcref}} (C_{idd}(\hat{i}_{dref} - \hat{i}_d) - \hat{v}_d) \\ \hat{i}_{dref} = \frac{I_d}{\hat{d}_d} \hat{v}_d + C_v(\hat{v}_{dc,ref} - \hat{v}_{dc}) \\ \hat{v}_d = -Z_s \hat{i}_d \end{cases} \quad (4-24)$$

where R_{dc} is one-third of the equivalence resistance value of the cascaded dc-dc load determined by its voltage and power level, C_{total} is three times the total capacitance of the output of the front-end PFC and input of the dc-dc converter, and Z_s is the equivalent d -axis source impedance.

The loop gain model can then be derived from (4-24) to

$$\frac{\hat{v}_{dc}}{\Delta \hat{v}_{dc}} = \frac{\left(D_d + \frac{I_d}{V_{dc}} \left(\frac{C_{idd} Z_s I_d}{V_d} + C_{idd} - Z_s\right)\right) C_{idd} C_v - \frac{I_d}{V_{dc}} C_{idd} C_v \left(sL + \frac{C_{idd} Z_s I_d}{V_d} + C_{idd}\right)}{\frac{-1 + s R_{dc} C_{total}}{R_{dc}} \left(sL + \frac{C_{idd} Z_s I_d}{V_d} + C_{idd}\right) + D_d \left(D_d + \frac{I_d}{V_{dc}} \left(\frac{C_{idd} Z_s I_d}{V_d} + C_{idd} - Z_s\right)\right)} \quad (4-25)$$

Z_s can be simplified to be $sL_g + R_g$ if the PFC converter is connected to a single-phase system. (4-25) then is further simplified as (4-26) by canceling the trivial orders.

$$the \frac{\hat{v}_{dc}}{\Delta \hat{v}_{dc}} = \frac{(D_d - (Z_s + sL) \frac{I_d}{V_{dc}})(s k_{pv} + k_{iv})(s k_{pi} + k_{ii}/2)}{s^2 \left(s \left(-\frac{L_g + L}{R_{dc}} + C_{total} k_{pi}\right) + \left(D_d^2 - \frac{R_g}{R_{dc}} + C_{total} k_{ii}/2\right)\right)} \quad (4-26)$$

The poles (p_1 , p_2 , and p_3) and zeros (z_1 , z_2 , and z_3) can then be identified from (4-26) as

$$\begin{cases} z_1 = -k_{ii}/2k_{pi} \\ z_2 = -k_{iv}/k_{pv} \\ z_3 = (D_d V_{dc}/I_d - R_g)/(L_g + L) \\ p_1 = 0 \\ p_2 = 0 \\ p_3 = -\frac{D_d^2 - R_g/R_{dc} + C_{total} k_{ii}/2}{-(L_g + L)/R_{dc} + C_{total} k_{pi}} \end{cases} \quad (4-27)$$

Figure 4-11 shows the loop gain analytical results of the single-phase system Case 3 in Table 4-2 using (4-26) and the full model (4-3) and (4-4). The loss of accuracy by the simplification is around 5° in terms of phase margin.

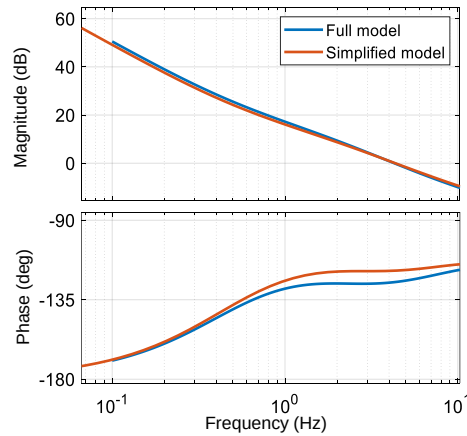


Figure 4-11 Full model and simplified model of the single-phase system Case 3 loop gain results.

From (4-27), the relationship between each system parameter and the loop gain shape can be identified easily. The poles p_1 and p_2 at the origin cause a -180° and -40 dB/dec magnitude change at the low-frequency range. z_1 , z_2 and p_3 are located at low frequency (0.1~10 Hz), while z_3 is around 80 Hz. Therefore, the loop gain shape at the studied frequency range mainly depends on the relative location of z_1 , z_2 , and p_3 . The voltage controller parameters, current controller parameters, and power stage parameters all have an impact on the loop gain result. This simplified model can be used to identify each factor's impact specifically.

When such a PFC converter is connected to a three-phase system, the assumption of ignoring the q -axis dynamics may no longer hold due to the phase difference between the three phases. When modeling the entire system into the d - q frame aligning with Phase A's input voltage, the input impedance of Phase A's PFC is diagonally dominant; however, the impedance of PFCs connected to Phase B and Phase C become not diagonally dominant due to the phase difference. Therefore, the coupling between the d -axis and q -axis is non-negligible for the source dynamics, making it non-neglectable when modeling its impact on the loop gain. Figure 4-12 shows the result when ignoring the d - q frame coupling for Case 2 in Table 4-2. The loss of accuracy is too severe that such simplification is not valid. On the other hand, in practice, various kinds of converters could be connected to a system. Having an analytical model with clear pole-zero expression may not be feasible or necessary. Instead, other methods to analyze the impact of each parameter on the overall loop gain could be employed, for example, sensitivity analysis or parameter identification with a collection of mass amounts of data.

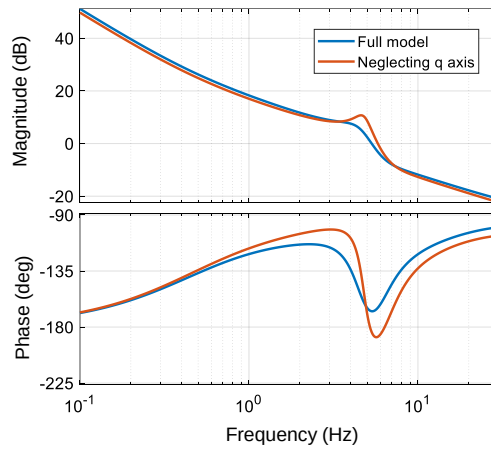


Figure 4-12 Full model and simplified model of the three-phase four-wire system Case 2 loop gain results.

4.4 Stability Analysis using the Loop Gain Model

The purpose of loop gain analysis in this paper is to assess the stability of the distribution system. The first part verifies the loop gain's effectiveness in analyzing stability. The second part compares the loop gain-based and impedance-based analysis results and discusses their practical application differences.

4.4.1 A. Case study using the proposed loop gain model

From the perspective of the voltage loop gain of one PFC converter connected to the system, the proposed loop gain models include the dynamics impact of the other components, which is represented by Z_T as derived in (4-4), (4-10), (4-21), and (4-22). Therefore, the loop gain reflects overall system stability. With the proposed loop gain model verified in Section 4.3 in the frequency domain, this section aims to use the loop gain model to study stability issues of a three-phase four-wire system, which is a typical configuration in a data center power system. The frequency of interest is 0.1 Hz ~ 50 Hz due to the low bandwidth of the voltage loop gain. The parameters of the simulation study are shown in Table 4-3. The PFCs all work at rated conditions. The source impedance or the PFC voltage controller parameters differ among the four cases. Comparing Case 1, Case 2, and Case 3, the three PFCs have the same parameters but the source side neutral impedance increases from 10 mH, 12 mH to 14 mH. Comparing Case 2 and Case 4, the source side impedance is the same, while the integral coefficients of the PFC PI controllers increase to 1.3 times that of Case 2. The time-domain simulation waveforms of the input voltage, current, and output dc bus of the PFC *a* are shown in Figure 4-13. Case 1 and Case 2 are stable, while Case 3 and Case 4 are unstable, oscillating at around 5 Hz.

Table 4-3. System parameters for the stability study.

No. Case	Source Impedance (phase)	Source Impedance (neutral)	k_{pv}	k_{iv}	PFC terminal voltage
Case 1	0.5 Ω + 390 μ H	10 mH	0.136	5.44	340 V
Case 2		12 mH	0.136	5.44	
Case 3		14 mH	0.136	5.44	
Case 4		12 mH	0.136	7.072	

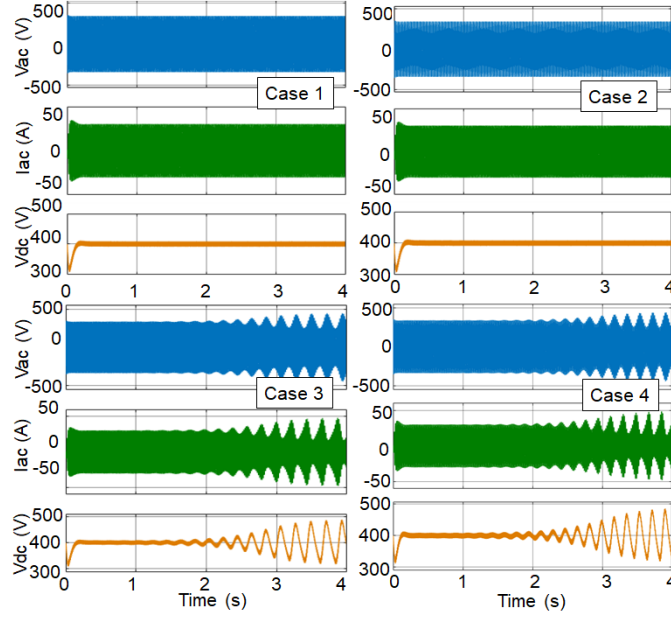


Figure 4-13 Time-domain simulation results of the three-phase four-wire system.

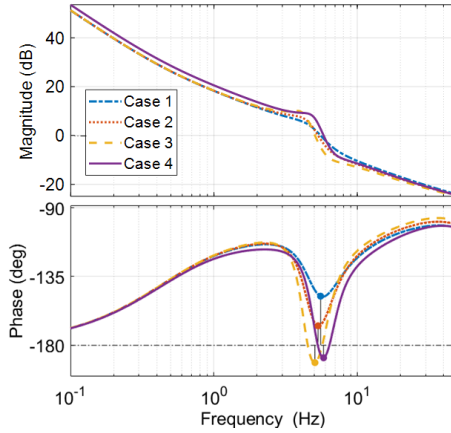


Figure 4-14 Loop gain modeling results of the three-phase four-wire system.

Using (4-3) and (4-21), the loop gain modeling results of the PFC converter connected to Phase A and the neutral line of the four cases are shown in Figure 4-14. The four marked points denote the frequency points of the cutoff frequency of each curve, so the difference between the denoted phase and the -180° line is the phase margin of the PFC loop gain for the four cases. Case 1 and Case 2 have a phase margin above 0, while Case 3 and Case 4 have a negative phase margin. From the Bode plot stability criteria, Case 1 and Case 2 are stable, Case 3 and Case 4 are unstable, and the points where the phase is -180° are also close to 5 Hz for Case 3 and Case 4. This loop gain

domain analysis matches the system time-domain simulation results. The proposed loop gain model can accurately reflect the system stability condition. From the loop gain perspective, the loop gain phase margin decreases with the increase of the source side impedance and the PFC voltage controller integral coefficient. Therefore, the proposed loop gain model can be exploited in studies involving either offline or online stability analysis.

4.4.2 Comparisons of impedance-based and loop gain-based stability analysis

For AC systems with three-phase converters, both the impedance-based and loop gain-based approaches have been presented to analyze stability [22]-[24]. For systems with single-phase loads, impedance analysis with GNC has been presented based on the virtual d-q frame concept [11]. Impedance-based stability analysis requires choosing an interface and obtaining the upstream and downstream impedance. The return ratio matrix $\mathbf{L}_{\text{return}}$ is the multiplication of upstream impedance and downstream admittance. GNC can then be applied to $\mathbf{L}_{\text{return}}$ to assess the system's stability. For the three-phase four-wire system in Figure 3-12, if choosing this interface at the terminal of PFC a , $\mathbf{L}_{\text{return}}$ is derived as

$$\mathbf{L}_{\text{return}} = -\mathbf{Z}_{\text{T}}\mathbf{Y}_{\text{PFC}a}. \quad (4-28)$$

The individual impedance expression $\mathbf{Y}_{\text{PFC}a}$ is in the Appendix. For the four cases shown in Table 4-3, the PFC a 's impedance and the return ratio matrix $\mathbf{L}_{\text{return}}$ are derived, respectively. The eigenvalues loci of the $\mathbf{L}_{\text{return}}$ for the four cases are shown in Figure 4-15. Case 1 and Case 2 don't have encirclements of $(-1, 0)$, while Case 3 and Case 4 have. So, by GNC, Case 1 and Case 2 are stable, and Case 3 and Case 4 are unstable. This result is consistent with the time-domain simulation and loop gain analysis results in Figure 4-13 and Figure 4-14.

Intuitively, since the two approaches are examining the same system, their conclusions are necessarily to be the same. To further examine this, the system closed-loop poles using the two approaches are calculated using (4-29) and (4-30), respectively.

$$1 + T_v = 0 \quad (4-29)$$

$$\det(\mathbf{I} + \mathbf{L}_{\text{return}}) = 0 \quad (4-30)$$

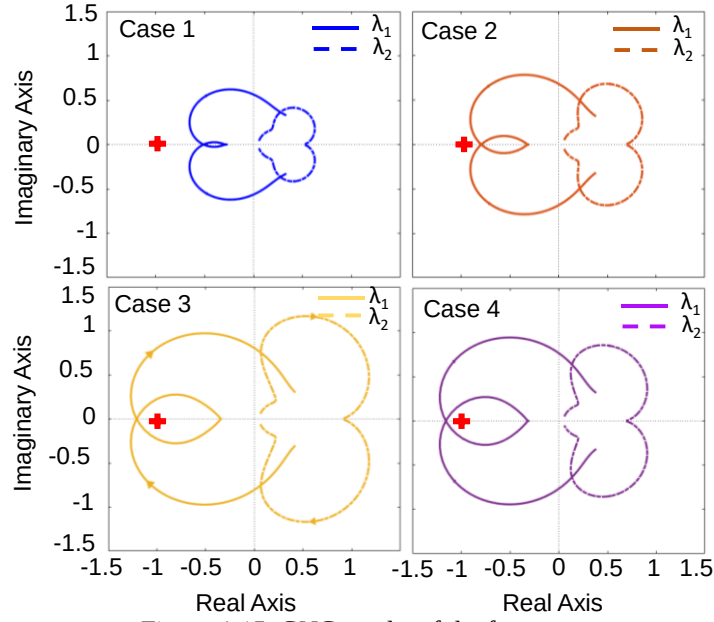


Figure 4-15 GNC results of the four cases.

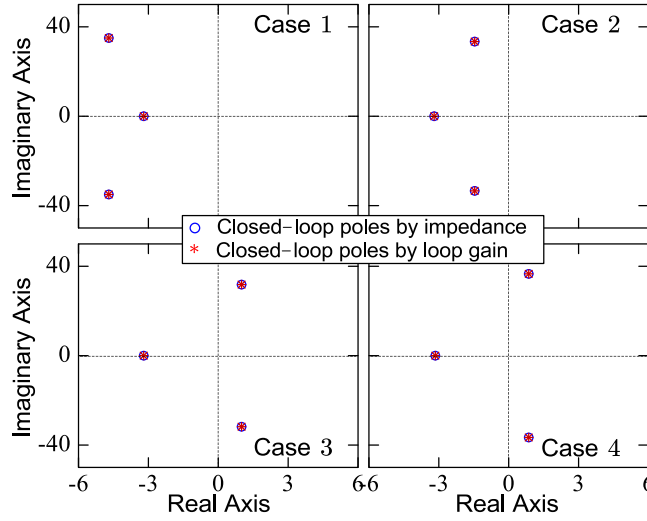


Figure 4-16 Closed-loop poles of the system using (4-29) and (4-30): blue circle: using impedance; red star: using loop gain model.

By solving (4-29) and (4-30), the critical closed-loop poles of the four cases are calculated and shown in Figure 4-16. For the studied system, the critical poles of the four cases obtained by the two approaches are at the same location, denoting a same stability condition and margin. For Case 3 and Case 4, there are two conjugate right-half-plane poles. For Cases 1 and 2, the corresponding

poles move to the left half-plane. This comparison also verifies the accuracy of the loop gain model.

While the loop gain and impedance-based approaches yield the same conclusion for stability analysis, they have different practical applications. The loop gain approach is more convenient to implement in systems with flexibility in configuring the converter controller. This is because the digital controller can directly enable the loop gain measurement function without requiring an additional instrument to measure system impedance. However, adding such a device would require extra costs and detailed design considerations. For instance, selecting the appropriate measurement technique, voltage and power rating, hardware integration with the existing system, and device maintenance are some potential challenges that may arise during its design and implementation.

On the other hand, if only the terminal behaviors are available for most components in the system, an impedance-based approach is more feasible. In this case, there is no need to access the converter control loop. Another difference between the two approaches is in the format of accessing stability. The loop gain result is a scalar; thus, a Bode plot can be used. However, impedance analysis results are in a matrix format, and a Nyquist plot in the complex plane is necessary. Designing and implementing an automatic stability margin detection algorithm using a Bode plot may be more straightforward than a Nyquist plot [15], [16].

4.4.3 Experimental Verification

This section aims to verify the proposed loop gain model using experimental measurement. The models for a single-phase system, a three-phase three-wire system, and three-phase four-wire systems are validated, respectively. Figure 4-17 shows the experimental setup. The single-phase SiC MOSFTE-based PFC converters with resistor load are connected to an AC source through some line impedance. The configurations of the tested systems are the same as shown in Figure 3-6, Figure 3-11, and Figure 3-12. Due to the setup limit, the dc loads of the PFC converters are resistors instead of dc-dc converters. The PFC converters are all controlled using the TMDSCNCD28379D. The design and parameters of the PFC converters are referred to in Figure 2-1 and Table 2-1, except that a first-order low-pass filter with a 0.01-time constant is cascaded to the original PI controller to filter further the double-line frequency components in the control path.

The experiments are conducted at input $100\text{ V}_{\text{rms}}$, 160 V_{dc} , and $35\ \Omega$ load for each PFC converter. To measure the open loop gain of the PFC converter in Phase A, the Software Frequency Response Analyzer (SFRA) function of the control card is used [25]. Because the PFC voltage loop gain usually has a very low cutoff frequency, the measured frequency range is at low frequency. Small-signal perturbations with 8 Volts of magnitude in $1\text{Hz} \sim 40\text{Hz}$ are added to the dc voltage reference, and the real-time dc voltage response is measured. The DSP codes embedded function can automatically calculate the loop gain frequency response at each frequency point.

Figure 4-18 shows the input voltage, input current, and output dc voltage waveforms of the three PFC converters during a loop gain measurement of one PFC for the tested three-phase four-wire system. The injected ac components in the dc voltage of the PFC are connected to Phase A, and the resulting low-frequency response in all three phase voltages and currents can be seen in Figure 4-18 (a). The main parameters of each test are shown in Table 4-4. The source side impedance and the PFC converter controller parameters are changed for different cases. The loop gain of the PFC connected to Phase A is measured using SFRA for each case. The modeling results of the single-phase system, three-phase three-wire system, and three-phase four-wire system are calculated using (4-3) and (4-4), (4-3) and (4-10), (4-3) and (4-41), (4-3) and (4-42), respectively.

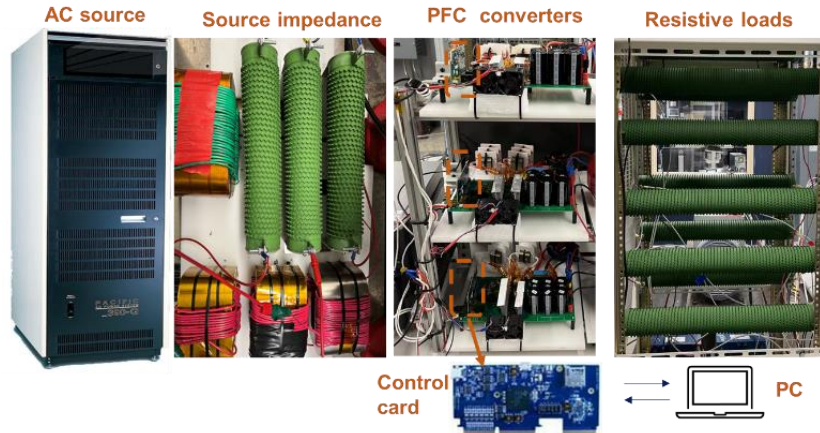
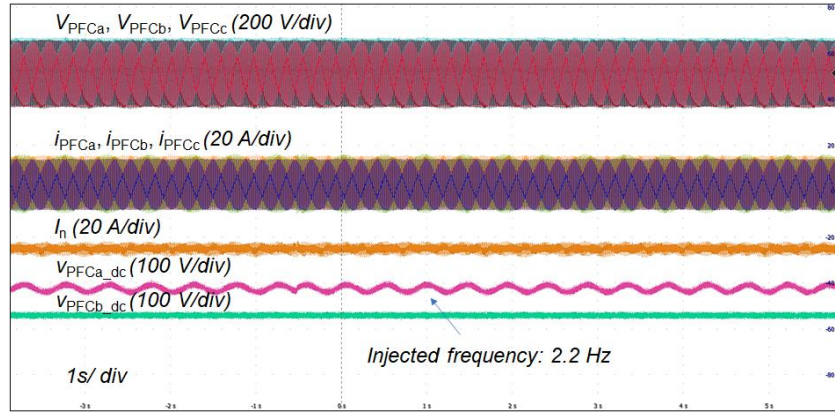
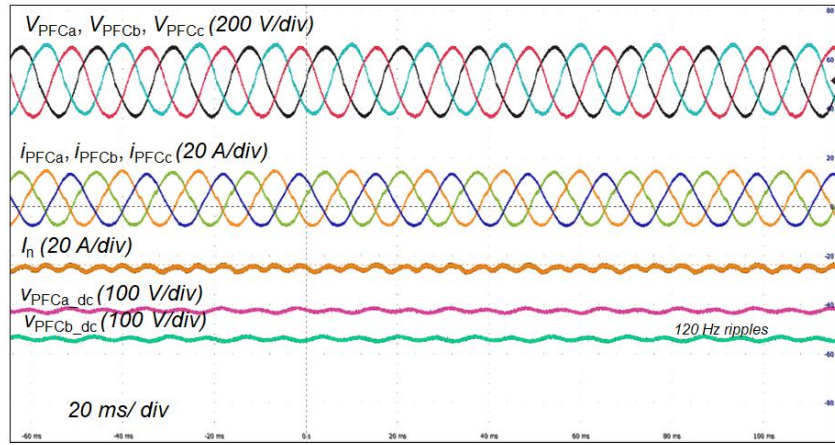


Figure 4-17 Experimental setup.



(a)



(b)

Figure 4-18 Time-domain waveforms during the measurement: (a) with 1s/div; (b) Zoomed-in version of (a) with time resolution of 20 ms/div.

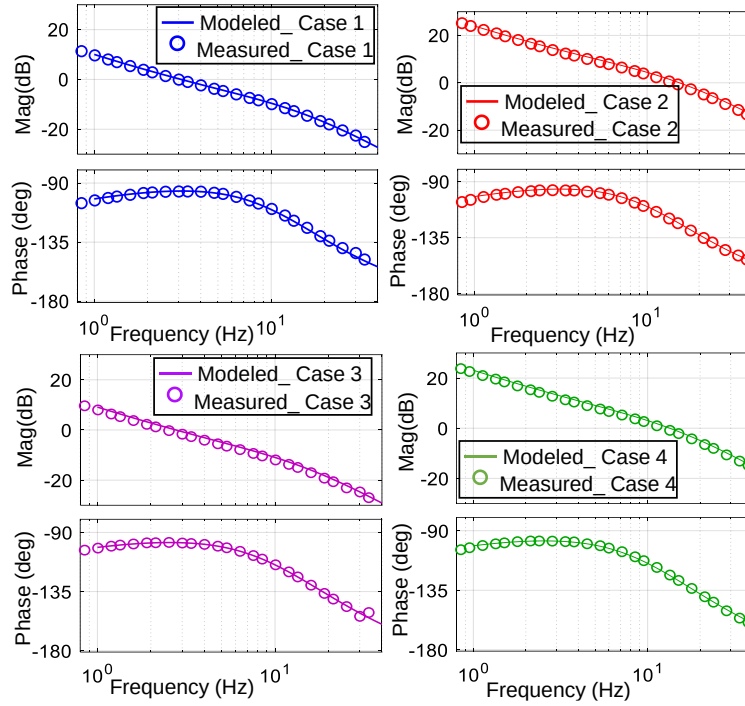


Figure 4-19 Experimental results of the single-phase system.

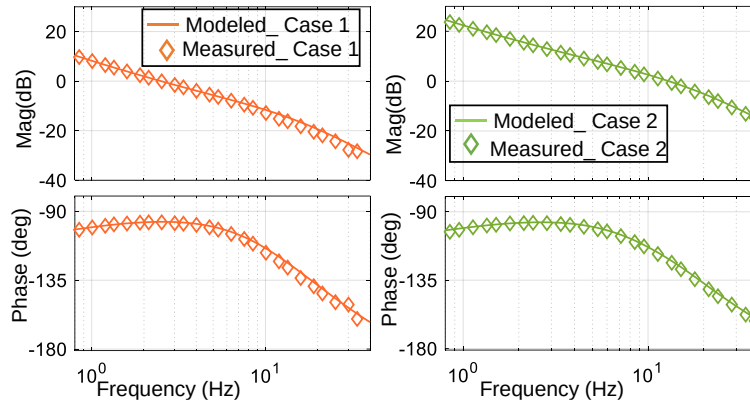


Figure 4-20 Experimental results of the three-phase three-wire system.

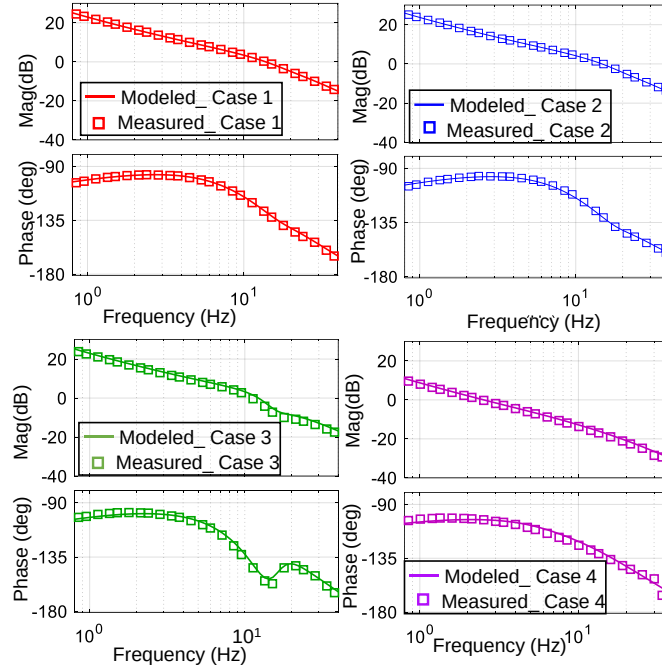


Figure 4-21 Experimental results of the three-phase four-wire system.

Table 4-4. System parameters for loop gain model verification in experiments.

System configuration	No. Case	Source Impedance	PFC k_{iv} , k_{pv}
Single-phase	Case 1	0	5.44, 0.136
	Case 2		27.2, 0.68
	Case 3	$1.3 \Omega + 2 \text{ mH}$	5.44, 0.136
	Case 4		27.2, 0.68
Three-phase-three-wire	Case 1	$1.3 \Omega + 2 \text{ mH}$	5.44, 0.136
	Case 2		27.2, 0.68
Three-phase-four-wire	Case 1	$1.3 \Omega + 2 \text{ mH}$ Neutral: $0.5 \Omega + 4 \text{ mH}$	27.2, 0.68
	Case 2	0 Neutral: $0.5 \Omega + 4 \text{ mH}$	27.2, 0.68
	Case 3	$1.3 \Omega + 2 \text{ mH}$	27.2, 0.68
	Case 4	Neutral: $0.5 \Omega + 10 \text{ mH}$	5.44, 0.136

Figure 4-19 shows the modeling and measurement results of the single-phase system. The modeling results are accurate compared to the measurement results for all four cases. Figure 4-20 and Figure 4-21 show the modeling and measurement results of the three-phase systems connected in a three-wire configuration and four-wire configuration, respectively. For all six cases, the measurement results also match the modeling results. These experimental measurements using SFRA verify the accuracy of the proposed models for each kind of system.

4.5 Summary and Conclusion

This section proposes a novel voltage loop gain model of a single-phase PFC converter based on the virtual d-q frame concept. Simulation and SFRA-based experimental measurements have verified the proposed loop gain model. Some useful conclusions are drawn as follows.

- (1) The proposed loop gain model is valid for whichever kind of system the single-phase PFC is connected to, a single-phase system, a three-phase three-wire system, or a three-phase four-wire system.
- (2) The proposed model is more accurate than the conventional quasi-static approximation in a single-phase system context. In contrast, the quasi-static way cannot be used to model the loop gain in a three-phase system.
- (3) The PFC's controller design and the source side dynamics would impact the loop gain results. The loop gain model can reflect the system stability conditions.
- (4) Loop gain analysis leads to the same conclusion as impedance analysis, but it offers unique application advantages as it does not require the cost and design challenges of employing a dedicated device, which is necessary for the impedance-based approach.

The proposed model can also serve as prior knowledge for loop-gain-based online stability monitoring of ac systems because it instructs understanding of the system parameters and stages' impact on the PFC loop gain.

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Chapter 5

Impedance-based Stability Analysis of a Microgrid with Grid-Forming Inverters

5.1 Introduction

With a growing share of renewable energy sources in U.S. electricity generation, the grid operators are facing an immediate need for additional power to compensate for the ‘duck curve’ to keep the grid stable and secure. Many small to mid-size manufacturing plants have their combined heat and power (CHP) generators which could be designed more flexible (F-CHP) that can be utilized as dispatchable distributed energy resources (DER) [1]. In the future, these F-CHP generators can be designed to be integrated into the grid with a high-power grid-tied converter. In addition to static power compensation, these F-CHP converters would also be designed to conduct grid-support functionalities including participation in voltage regulation and frequency regulation, online stability monitoring, and capable of islanding and microgrid operation modes [2].

On the other hand, renewable energy such as solar, and wind are also integrated into the grid through power-electronics-based converters. With more and more converters connected to the grid, the dynamic interactions among the converters and other grid components may cause instability. These behaviors can be analyzed using impedance-based stability analysis [3]-[5]. From this perspective, the negative resistance characteristic caused by the phase-locked-loop (PLL) or voltage controller, and the dynamics of reactive power-voltage droop control are usually more detrimental to system stability [6], [7]. In this context, the F-CHP converters featuring grid-support functionalities add extra dynamics to the system and might alter system behavior. Moreover, the F-CHP converter can also be designed with grid-forming control to handle both grid-connected mode and islanding mode operation. The virtual-synchronous-machine (VSM) based grid-forming control mimics the dynamics of a generator so is expected to provide more ‘inertia’ to the system

to help stabilize the system [8] – [10]. Therefore, the impact of the grid-forming control of the F-CHP on the system behavior is also an intriguing subject to study.

A Power-Hardware-in-the-Loop (PHIL) testbed is also developed to validate the study. PHIL is an efficient real-time testing platform, connecting a real physical power electronics system to a simulation environment through amplifiers and sensor network interfaces [11]–[14]. By utilizing PHIL, physical equipment can be replaced with virtual models for system integration testing, reducing the cost of full-scale power system testing. PHIL has been used in the system-level study and testing of individual equipment, such as motor drive emulation, power system quality study, microgrid operation, and electric vehicle testing [15] – [18]. Although the accuracy of PHIL has been assessed in estimating impedance for linear systems with passive components, its application in power system stability analysis involving nonlinear models and potential harmonic instability behavior is still under investigation [19].

5.2 System Parameters

The system shown in Figure 5-1 is designed based on the 4.16 kV IEEE 13 bus system. For this study, the spotted loads are removed, all three-phase loads are changed to be balanced power, a couple of PV inverters are connected to node 680 through a step-up transformer, and an F-CHP converter is connected to node 675 through a step-up transformer. All loads are designed to be passive loads. The detailed parameters of the feeders and passive loads are shown in Figure 5-1. According to the IEEE Standard 1547, the voltage profile in this study is required to be in the range of 0.975 p.u. to 1.05 p.u..

In Figure 5-1, the F-CHP converter is designed to compensate duck curve and provide grid support functions. The rated power is 1MW and the rated voltage is $480 V_{llrms}$. For the F-CHP converter, two kinds of control schemes are implemented and compared. One is based on grid-forming control, as is shown in Figure 5-2. The virtual-synchronous-machine (VSM) concept is employed here. The control is mainly composed of five parts: the power-balance synchronization block, which utilizes the active power control to generate the synchronization angle used for the Park's transform; a frequency-active power droop control is integrated into this part; a voltage-reactive power droop control generates the inner voltage potential reference; a virtual impedance

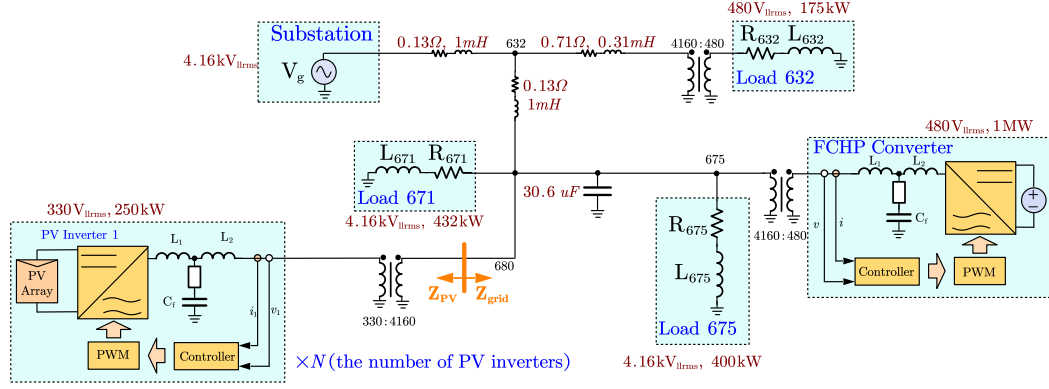


Figure 5-1 A distribution system with F-CHP and PV.

loop generates the current reference; the inner current loop generates the duty cycle for PWM. The other control scheme is conventional PLL-based control, as is shown in Figure 5-3. A PLL is employed to track the terminal voltage and generate the synchronization angle used for the Park's transformation. The ac current is controlled in a synchronous $d-q$ frame using a proportional-integral (PI) controller. An active-power controller generates the d-axis current reference, and a voltage-reactive power droop control generates the q-axis current reference. The PV inverters connected to node 680 are also designed with a grid-tracking control similar to the one shown in Figure 5-3. The difference is that a maximum-power-point-tracking (MPPT) together with a dc voltage controller is used to generate the reference for the d-axis current. All PV converters connected in parallel are assumed to be identical and work at rated conditions. Each is rated at 250 kW, 330 V_{llrms}. The number of PV converters is a variable in this study, which also denotes the different integrated power in the system for the different cases in the following sections. The detailed control parameters of the PV inverter and F-CHP converter are shown in Table 5-1 ~ Table 5-3.

Table 5-1 F-CHP converter parameters with grid-forming control

Symbol	Descriptions	Value
f_{sw_FCHP}	F-CHP converter switching frequency	20 kHz
k_{pi_FCHP}	Current controller PI proportional gain	0.0024
k_{ii_FCHP}	Current controller PI integral gain	0.0094
k_{pq_FCHP}	Q controller PI proportional gain	0
k_{iq_FCHP}	Q controller PI integral gain	-5.3e-4
J_p	Virtual inertia term	2000
a	Lead-lag term 1	2
T	Lead-lag term 2	0.0113
L_v	Virtual inductance	1.9e-4
R_v	Virtual resistance	0.006

Table 5-2 F-CHP converter parameters with grid-tracking control		
Symbol	Descriptions	Value
k_{ppll}	PLL PI proportional gain	1
k_{ipll}	PLL PI integral gain	0.1
k_{pi}	Current controller PI proportional gain	2.35×10^{-4}
k_{ii}	Current controller PI integral gain	0.0094
k_{pp}	Active power controller PI proportional gain	0
k_{ip}	Active power controller PI integral gain	0.002
k_{pq}	Q controller PI proportional gain	0
k_{iq}	Q controller PI integral gain	-0.001

Table 5-3 PV inverter parameters with grid-tracking control		
Symbol	Descriptions	Value
f_{sw_PV}	PV inverter switching frequency	3 kHz
k_{ppll_PV}	PLL PI proportional gain	0.1
k_{ipll_PV}	PLL PI integral gain	1
k_{pi_PV}	Current controller PI proportional gain	0.001
k_{ii_PV}	Current controller PI integral gain	0.315
k_{pv_PV}	Voltage controller PI proportional gain	-3
k_{iv_PV}	Voltage controller PI integral gain	-30
k_{pq_PV}	Q controller PI proportional gain	-1.467×10^{-5}
k_{iq_PV}	Q controller PI integral gain	-0.1467

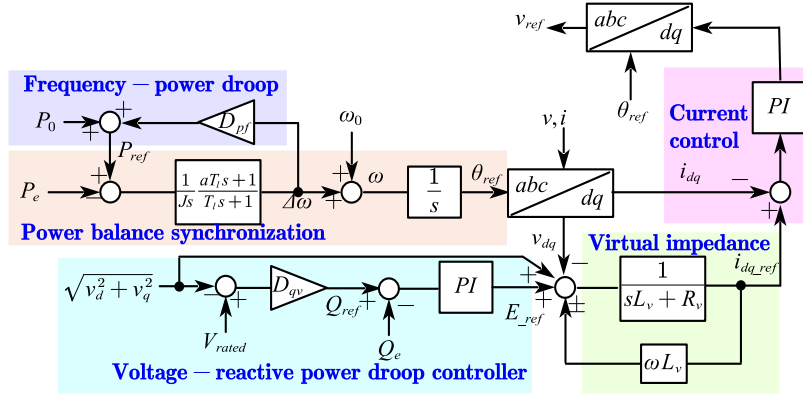


Figure 5-2 F-CHP converter controller based on grid-forming control.

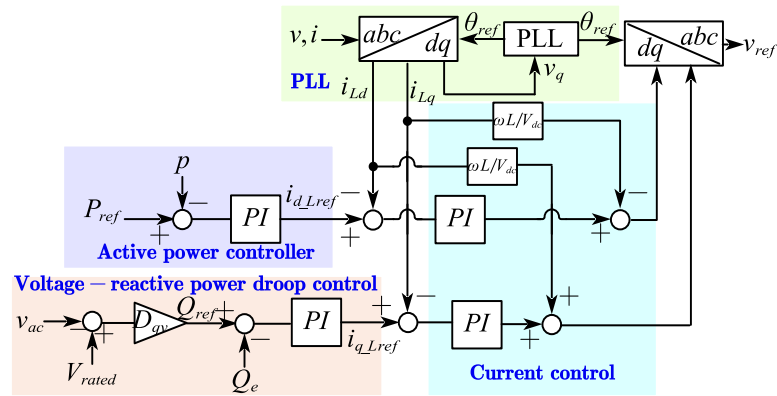


Figure 5-3 FCHP converter controller based on grid-tracking control.

5.3 Testbed Study using Time-domain Simulation

With more PV inverters connected to the system, there is higher active power integration, while at the same time the system's stability margin decreases. Instability issues might occur at a certain point. In this section, a study on the system PV inverter integration capacity is conducted through time-domain simulation in PLECS. First, the systems with and without the F-CHP converter under different loading conditions are compared. Then cases with different F-CHP generation power are compared, followed by the cases with different F-CHP control schemes. The last part studies the cases with and without the Q-V droop of the PV inverters and SVC of the system and points out the origin of the system instability.

Two scenarios: with and without the F-CHP converter connected to the grid, and four load conditions: 10 %, 30 %, 70 %, and 100 % are studied. The 100 % denotes a total of 1 MW load, and the 10 %, 30 %, and 70 % cases are constructed by scaling down all the loads with the same ratio. The F-CHP converter utilizes the grid-forming control shown in Figure 5-2. Figure 5-4 shows the PV inverter integration capacity. The maximum PV power for Case 1~ Case 7 means the system will have oscillation if operating with one more PV inverter. For Case 8 the PV integration is limited by the voltage profile requirement. From Figure 5-4, the F-CHP converter can increase renewable integration amount because it increases system stability margin, especially in heavy load conditions. Figure 5-5 shows the voltage at node 680 voltage with 6 MW of PV power under the condition of Case 7. Around 860 Hz oscillations can be observed, and the per-unit values also exceed the voltage profile requirement because of the oscillations. Figure 5-6 shows a stable operation with 6 MW of PV power under the condition of Case 8.

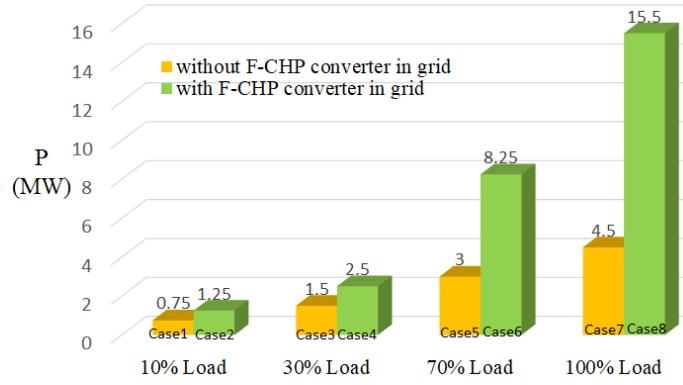


Figure 5-4 PV inverter integration capacity with and without the F-CHP converter in the grid under different loads.

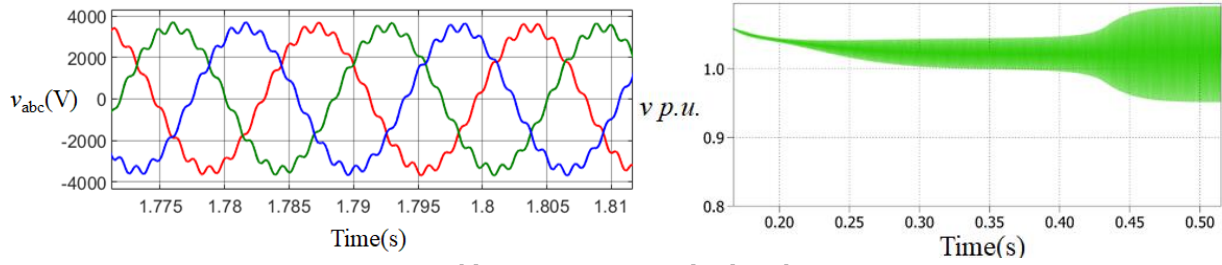


Figure 5-5 V680: unstable, PV 6MW, 100% load, without F-CHP converter.

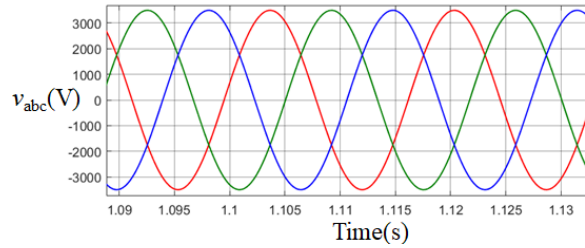


Figure 5-6 V680: stable, PV 6MW, 100% load, with F-CHP converter

Figure 5-7 shows the system PV integration capacity when the F-CHP generates different amounts of active power without triggering instability or violating voltage profile requirements. The F-CHP converter is operating with grid-forming control and the system is with a full-load condition as in Case 8 in Figure 5-4. For the four cases, the PV integration capacity is all limited by the voltage profile requirement. The results are slightly different because the different FCHP power impacts the voltage profile. No stability problems are observed for all four cases. The FCHP converter power does not have an impact on its benefits in helping to increase the system stability margin. This points out that the F-CHP converter's voltage-support function is sufficient to stabilize the system and its active power generation is not required from a dynamic standpoint.

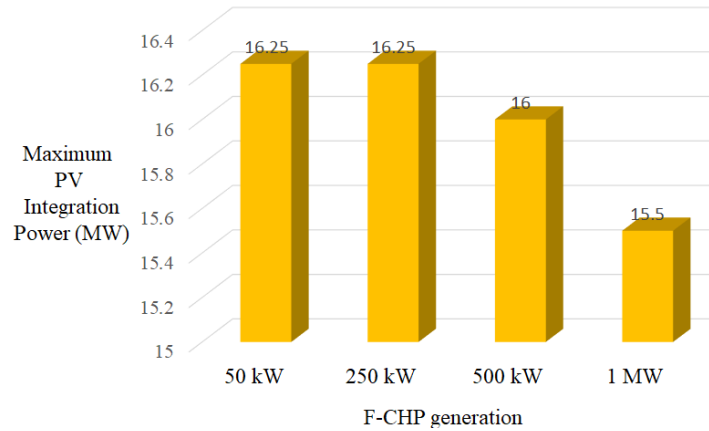


Figure 5-7 Maximum PV integration with different FCHP generation

Figure 5-8 shows the maximum PV integration with F-CHP working in different control modes, namely VSM-based control, VSM-based control with input voltage feedforward (FF) control, PLL-based control, and PLL-based with input voltage FF control. The input voltage is fed to the output of the current controller with a $1/V_{dc}$ gain. All cases are found to be limited by voltage profile requirements. Compared with Case 7 in Figure 5-4, both VSM-based control and PLL-based control demonstrate benefits in increasing system stability, while adding an input voltage feedforward control for both control schemes is detrimental to system stability.

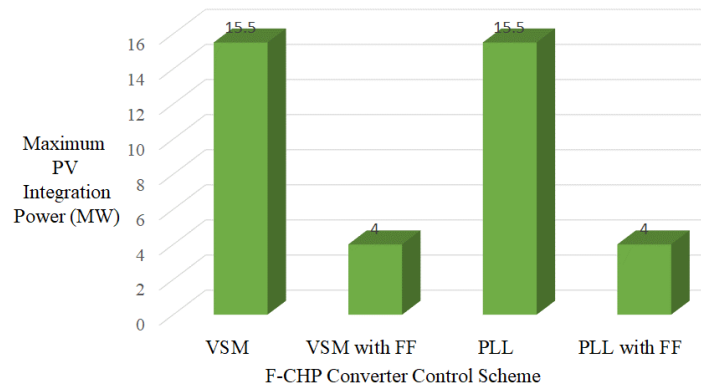


Figure 5-8 Maximum PV integration with different FCHP control

The SVC is found to be critical in observing oscillations in the system study. Figure 5-9 shows the maximum PV integration with and without Q-V droop of the PV inverters, with and without the SVC (C675) in the system. The F-CHP converter is not in the system for this comparative study. The Q-V droop control of the PV inverters can provide an automatic reactive power compensation to improve the voltage profile. However, the simulation results show that when the number of PV inverters exceeds a certain value, the Q-V droop of the PV inverter might have

dynamics interactions with the SVC and cause instability. Removing the Q-V droop slightly increases the PV integration capacity, but it is still limited by the voltage profile because there is no sufficient reactive power compensation. The installed SVC is designed to provide fast-acting reactive power on the electricity transmission networks but it is not enough under the operating conditions. If removing the SVC but keeping the Q-V droop, the PV integration capacity is the most because the possible dynamics interactions are diminished while the control still helps to adjust the voltage within the voltage profile requirements. Therefore, having the F-CHP converter can resolve the instability issues when keeping the Q-V droop control and the SVC to maintain the voltage profiles within the limits.

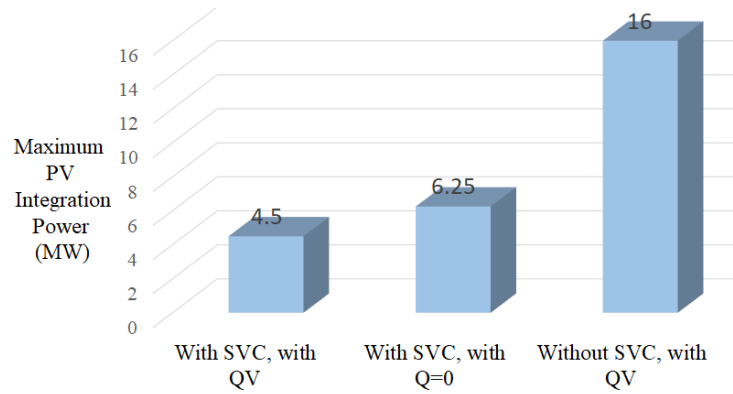


Figure 5-9 Maximum PV integration with/wo SVC or QV droop

5.4 Origin of the Instability analyzed using impedance-based Stability Analysis

The stability of the system shown in Figure 5-1 can be assessed using the Generalized Nyquist Criterion (GNC) based on impedance analysis. The interface to perform stability analysis is chosen at node 680 which is the PV inverter output. Both the PV side impedance $\mathbf{Z}_{pv}$ and the aggregated impedance of the rest of the grid $\mathbf{Z}_{grid}$ are extracted in the simulation. Considering there is a right-half-plane pole caused by the PLL-based control in the PV inverter terminal impedance, the PV admittance instead of impedance is used to calculate the system return ratio matrix, which is defined as,

$$\mathbf{L}_s = \mathbf{Z}_{grid} \cdot \mathbf{Y}_{pv} \quad (5-1)$$

By plotting the eigenvalues of the above matrix $\mathbf{L}_s$ in the complex plane, the stability of the system can be assessed [20]. To employ the impedance-based stability analysis method, the analytical model of the small-signal impedance is derived for both the F-CHP converter and PV

inverter. Meanwhile, simulation models for both are also built-in Simulink. The impedance extracted in simulation based on the frequency-response method is overplotted with the analytical results in Figure 5-10 and Figure 5-11, verifying the analytical results for both the PV inverter model and F-CHP converter model.

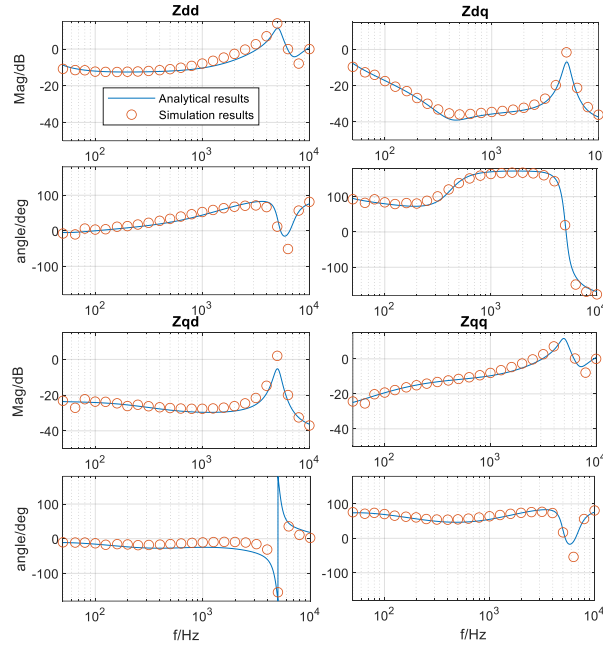


Figure 5-10 F-CHP Impedance Analytical and Simulation Results

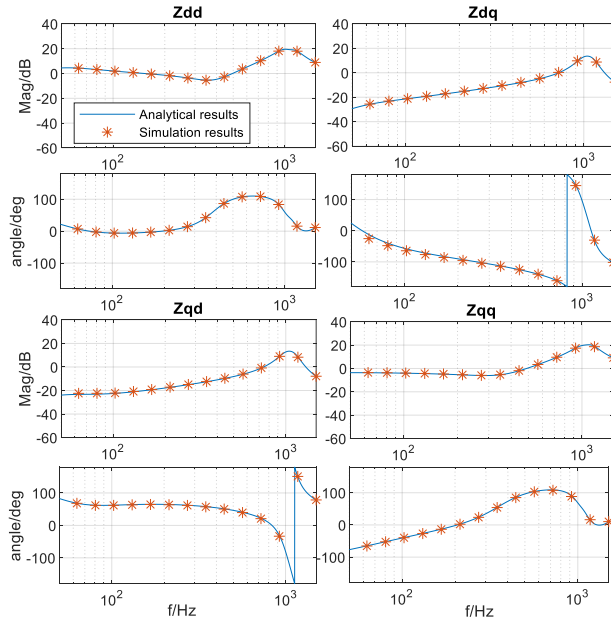


Figure 5-11 PV Impedance Analytical and Simulation Results

With the derived analytical impedance model, the L_s can be calculated using (5-1). Figure 5-12 (a) and (b) show two cases both with 5 MW PV integration and under 100% load conditions. Figure 5-12 (a) is of the system without the F-CHP converter and Figure 5-12 (b) is with the F-CHP converter. The loci in Figure 5-12 (b) are still far away from (-1, 0), showing a decent amount of stability margin, while one of the loci in Figure 5-12 (a) has encirclements of (-1, 0), indicating an unstable or oscillation condition. This comparative study in the frequency domain also shows the benefits of the F-CHP converter in increasing system stability margin, further verifying the results in Figure 5-4. The frequency range of the loci near the (-1, 0) is around 400 Hz~1 kHz, matching the oscillation's frequency range in Figure 5-5. To get an insight into this increase in stability margin, the impedance of the PV and grid side at 400 Hz ~ 1 kHz are analyzed as follows.

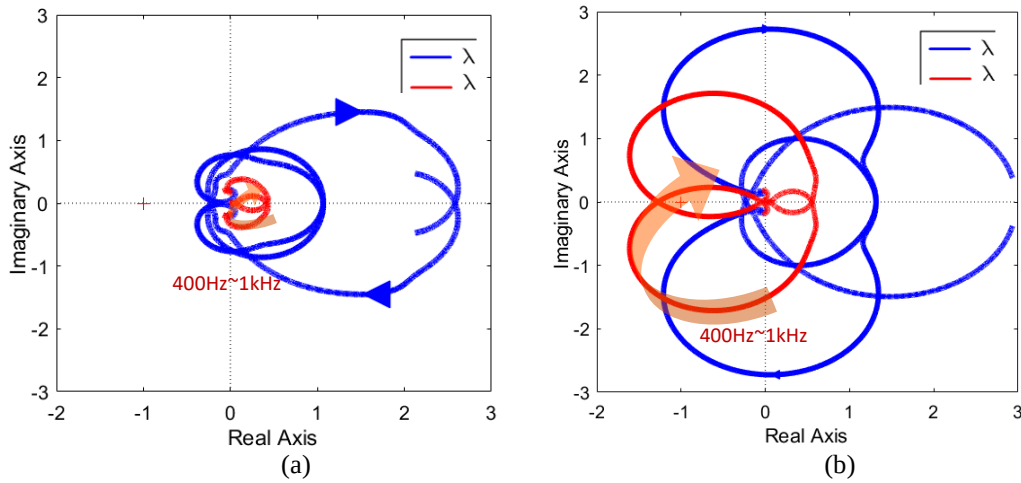


Figure 5-12 Nyquist plot using analytical model: PV: 5 MW, 100% load, (a) without the F-CHP converter; (b) with the F-CHP converter

Figure 5-13 shows the PV side impedance of the two cases in Figure 5-12 (a) and (b). The difference is so small that the grid side impedance seems more critical in resulting in such a different stability margin. Figure 5-14 shows the F-CHP converter impedance (with transformer), and the grid-side impedance with and without the F-CHP converter Z_{CHP} , $Z_{\text{grid_wiCHP}}$, and $Z_{\text{grid_woCHP}}$. $Z_{\text{grid_wiCHP}}$ can be approximated as the parallel impedance of Z_{CHP} and $Z_{\text{grid_woCHP}}$ since the feeder impedance is very small from node 671 to node 675. From Figure 5-13, because of the parallel impedance effect, the gain of $Z_{\text{grid_wiCHP}}$ is smaller than $Z_{\text{grid_woCHP}}$, especially around the two resonant frequency points around 700 Hz and 800 Hz where the PV side impedance

and grid side impedance have possible interactions. This is the key factor of an increased system stability margin after connecting the F-CHP converter to the system.

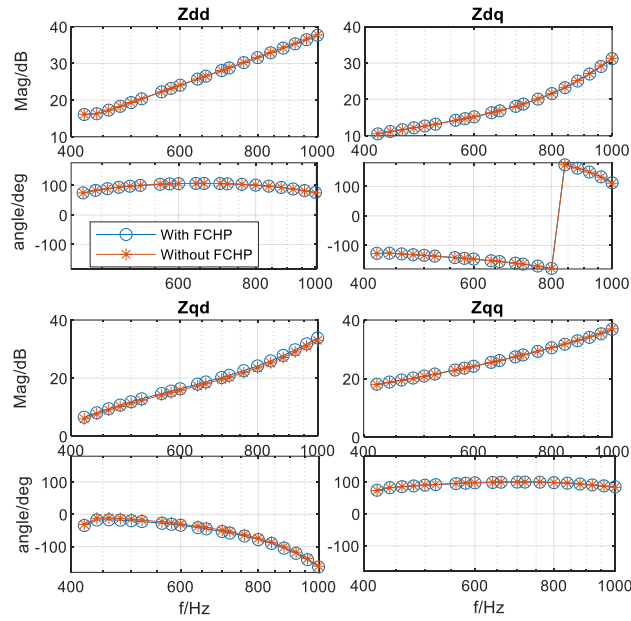


Figure 5-13 PV side impedance with and without F-CHP converter

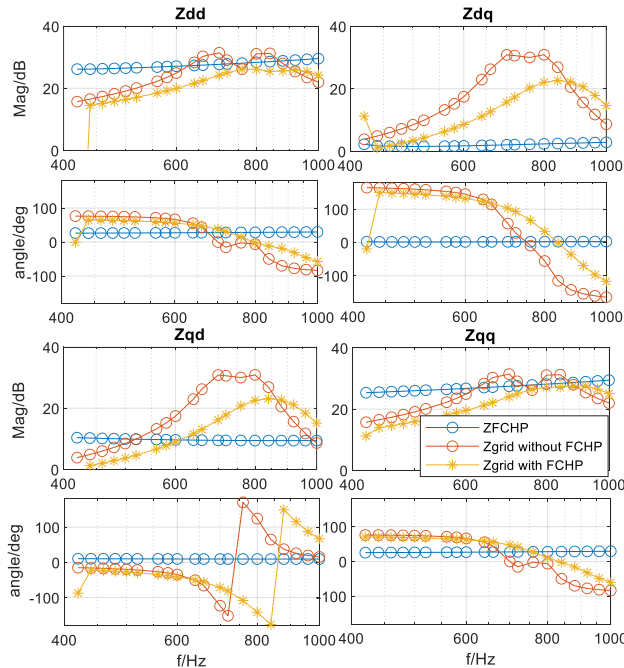


Figure 5-14 FCHP converter impedance, grid impedance with and without F-CHP converter

Figure 5-15 shows the grid side impedance with different power, 50 kW, 250 kW, 500 kW, and 1MW of the F-CHP converter at 5 MW of PV integration. The impedance curves are very close to each other. Therefore, the stability margin benefits brought by the F-CHP converter are not impacted by the amount of active power the F-CHP converter provides but is related to the controller behavior. These results match the results in Figure 5-7 obtained through time-domain simulation.

Figure 5-16 shows the grid impedance with different control modes of the F-CHP converter: grid-forming control, grid-forming control with input voltage feedforward terms, grid-tracking control, and grid-tracking control with input voltage feedforward terms. From the analysis for Figure 5-14, it's found that the gain reduction of $\mathbf{Z}_{\text{grid}}$ is beneficial to increase the system stability margin. Figure 5-16 shows that using grid-forming control or grid-tracking control has similar gain reduction as well as stability margin increase benefits. While adding input voltage feedforward control eliminates these benefits and reduces system stability margin as the case without the F-CHP converter.

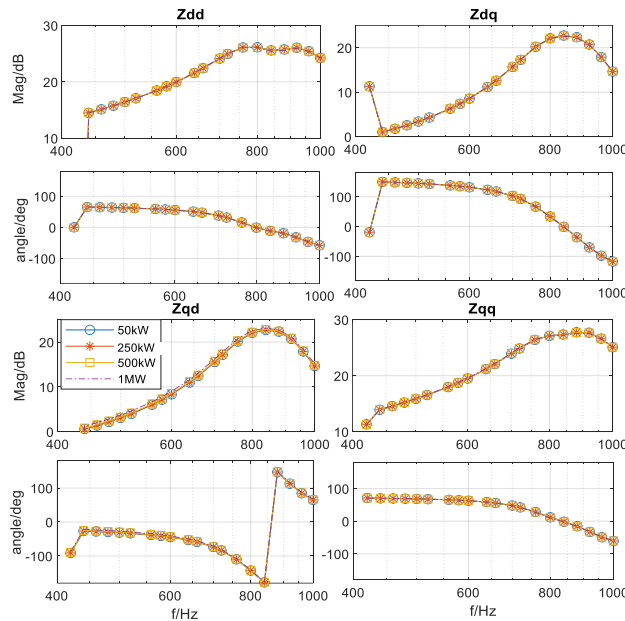


Figure 5-15 Grid impedance with different FCHP generation

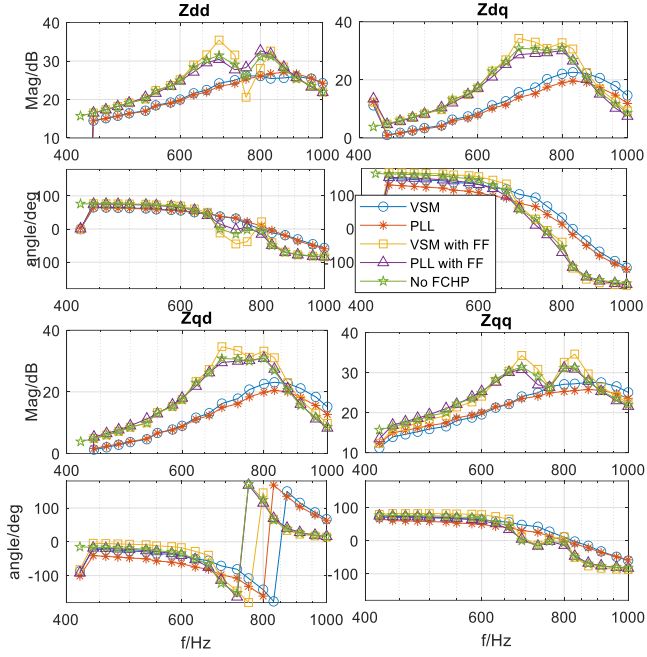


Figure 5-16 Grid side impedance with different FCHP control modes

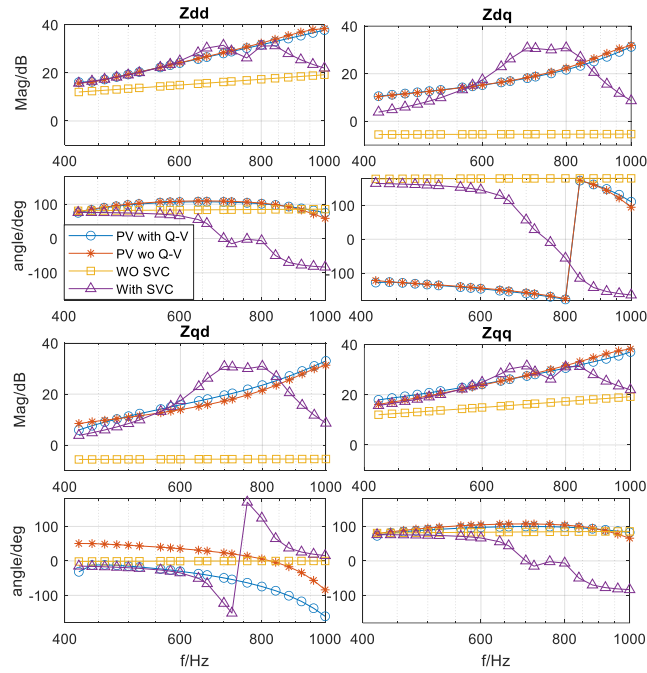


Figure 5-17 PV side impedance with/wo Q-V droop control and grid side impedance with/wo SVC

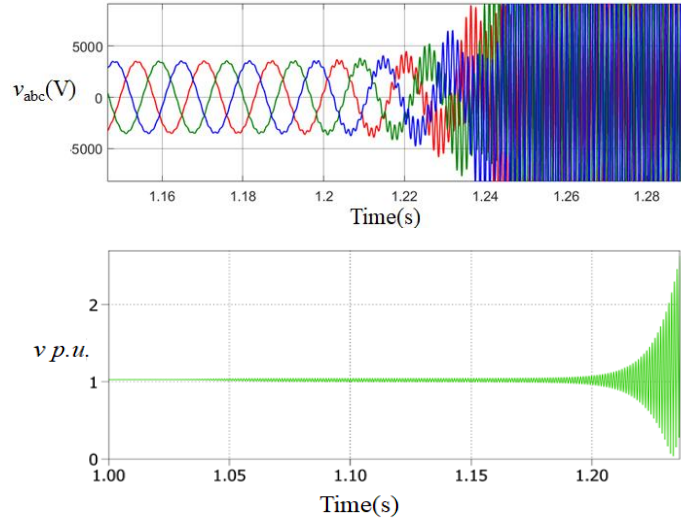


Figure 5-18 V680: unstable, PV 6 MW, 100% load, without F-CHP converter, without limiters in the PV's controllers

Figure 5-17 shows the system without the F-CHP converter but with different PV inverter controls or system components. The time-domain simulation results summarized in Figure 5-9 show that having the SVC and PV with Q-V droop controls together is detrimental to system stability. Figure 5-17 shows that with the SVC, the grid side impedance has a much higher gain in all four elements because of the resonance between the SVC and the inductive and resistive network of the grid. The Q-V droop controller of the PV inverter causes the Z_{qd} term to drop around the 90° phase. This causes a change in the dynamic behavior of the whole system.

The studied system is mainly composed of inductive feeders and loads. The SVC is usually designed to provide quick reactive power compensation to maintain the voltage profiles within required limits. However, with more PV power integrated into the system, the voltage profiles might not be kept within the limits. Therefore, the PV inverters are designed with Q-V droop control to automatically compensate for reactive power. However, this control might interact with the SVC and the inductive components in the grid network and causes instability. With the F-CHP converter, the system stability margin is increased a lot and both SVC and Q-V droop control can be kept to maintain the voltage profiles within limits with much more PV power integration. This study identifies the dynamics benefits of the F-CHP converter in addition to static compensation to duck curves. Based on the discussion above, when designing the inverters with a Q-V droop controller, the SVC should be adjusted or removed to avoid the onset of dynamics interaction. If

using the SVC to compensate for the reactive power, the capacitance value needs to be carefully designed based on the grid network impedance to avoid instability as well as to maintain the voltage profiles.

For the unstable cases, the oscillations shown in Figure 5-5 are limited to a certain magnitude after 0.5 s instead of becoming divergent, which is due to the nonlinear blocks in the PV inverter controller, including all the limiters and dead band in the droop controller. Therefore, there might only be some high-frequency harmonics observed in the system, but the system has already entered the unstable region. Fig. 18 shows the system's unstable behaviors when all the limiter blocks are removed. The system voltages become divergent and collapse at a certain point.

5.5 Development and Evaluation of the PHIL Testbed and Experimental Verification

This section first introduces the PHIL testbed developed to verify this study. A case study using the testbed is then carried out to demonstrate the possible appearance of RHP poles in grid impedance and its impact on stability assessment.

5.5.1 The PHIL testbed

The testbed mainly comprises three pieces of equipment: a grid-tied inverter 675, an OPAL-RT real-time simulator, and an EGSTON COMPISO system.

The grid-tied inverter is a SiC power module-based modular scalable converter. The detailed design, parameters, and performance test results are shown in [21]. The phase-leg current is controlled in the ABC frame using a proportional-resonant (PR) controller. The inverse Park's transform of the reference values in the dq frame gives the reference values. It provides power compensation to the microgrid to cope with the generation fluctuation of the renewables.

Moreover, the converter is designed with a grid stability monitoring function. That means while providing power compensation for the microgrid, at the same time, the grid-tied inverter 675 can measure the grid impedance. A series of small-signal components at different frequencies are added sequentially to the dq frame current reference values, so the inverter can inject current

perturbations into the microgrid, and by collecting the voltage and current response at its terminal, the d-q impedance of the microgrid can be calculated. Two sets of injections are needed to solve the 2×2 impedance matrix using (5-2) [22].

$$\mathbf{Z}_{\text{grid}} = \begin{bmatrix} \hat{v}_{d1} & \hat{v}_{d2} \\ \hat{v}_{q1} & \hat{v}_{q2} \end{bmatrix} \begin{bmatrix} \hat{i}_{d1} & \hat{i}_{d2} \\ \hat{i}_{q1} & \hat{i}_{q2} \end{bmatrix}^{-1} \quad (5-2)$$

The OPAL-RT real-time simulator can be assessed through the desktop software RT-lab, which has Simulink model time compatibility to configure and command the simulator. The step of the simulation platform is 20 us. In this study, the grid-tied converter is connected to the rest of the microgrid through node 675. This grid-tied inverter is labeled as inverter 675 to differentiate it from other grid-tied converters. The microgrid is emulated using the developed Simulink model and interfaces with the inverter 675 through the amplifiers. The terminal voltage 675 is measured in the Simulink model and sent to the amplifiers as voltage setpoints.

The EGSTON COMPISO system has six amplifiers connected to the same DC bus of an internal active front end. It can work in voltage mode or current mode. In this test, three amplifiers are used in three-phase voltage source mode. The setpoints of the amplifiers are received from the OPAL-RT simulator through optical cable pairs. These amplifiers are made of converters with 125 kHz switching frequency and 15 kHz current loop bandwidth.

Figure 5-19 shows the interconnection of the testbed. A transformer is placed between the grid-tied inverter and the amplifiers for EMI isolation. The transformer turns ratio is 1:1 to ensure the same voltage level seen at the grid-tied inverter terminal and the microgrid terminal. Three hall sensors are used as the three-phase current sensor to measure the current flowing into the amplifier and send the results to the OPAL-RT through its analog input ports. The conversion time of the analog input is 2.5 us. A three-phase controlled current source is placed at the model's corresponding interface (node 675). The current sensing results are assigned to these control current sources as the amount of current injected into the microgrid. At the same time, the voltage values across these controlled current sources are measured and sent to the amplifier as setpoints. Figure 5-20 shows a capture of the input voltage, input current, and DC bus voltage waveforms of the inverter 675 during its operation and impedance measurement. The injected small-signal

components on top of the fundamental components in the current waveforms can be seen in Figure 5-20. The injection level is 3 % of the nominal. Other injection signals or identification methods may be explored to achieve a shorter injection time to ensure compliance with grid codes [23], [24], [25], [26].

5.5.2 Verification of the Microgrid Dynamic Emulation

The microgrid model is implemented in the OPAL-RT simulator through the RT-LAB platform. The experimental study's microgrid configuration and load combination are the same as in the simulation study, as shown in Figure 5-1. The substation voltage level is set at 120 V. The inverter 675 provides 30 A of current to the microgrid and monitors the microgrid impedance at the same time. For stability assessment, the analysis interface is chosen at the output terminal of grid-tied inverter 675. Therefore, the impedance of the microgrid side and the inverter side are both needed. Since the grid-tied inverter is local, its inward impedance is available by either modeling or measuring using equipment called Impedance Measurement Unit (IMU). Figure 5-22 shows the grid-tied inverter input impedance at 120 V, 30 A. The q-q channel impedance shows an RHP pole feature (decreasing magnitude and increasing phase) at around 20 Hz, caused by the PLL-based control. The output impedance of the emulated microgrid at the inverter terminal is verified with the analytical results. Figure 5-21 shows one measurement of microgrid impedance $\mathbf{Z}_{\text{grid}}$ obtained by the grid-tied inverter 675 and the corresponding analytical results. The analytical model of the microgrid impedance is obtained by computing the interconnected network impedance with all the components' impedances available. This proves that the amplifier and real-time simulator can replicate the dynamic behavior of the studied microgrid.

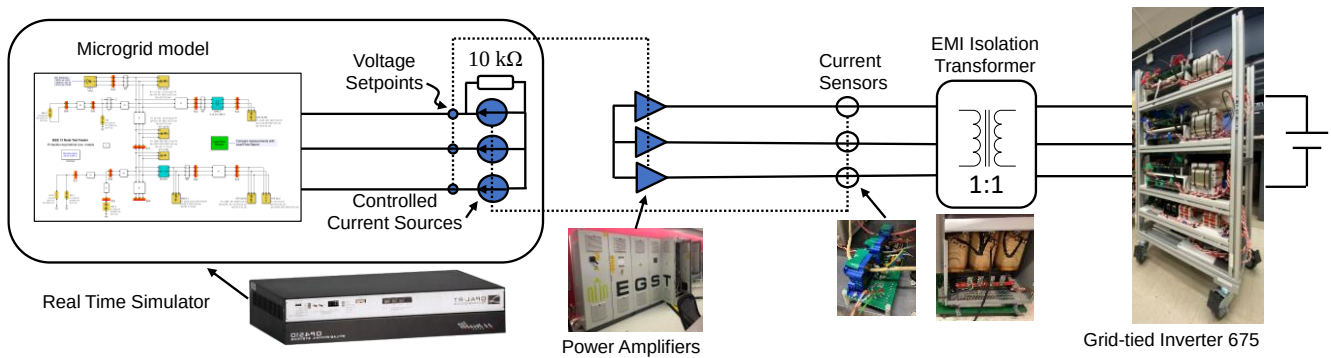


Figure 5-19 Configuration of the PHIL testbed.

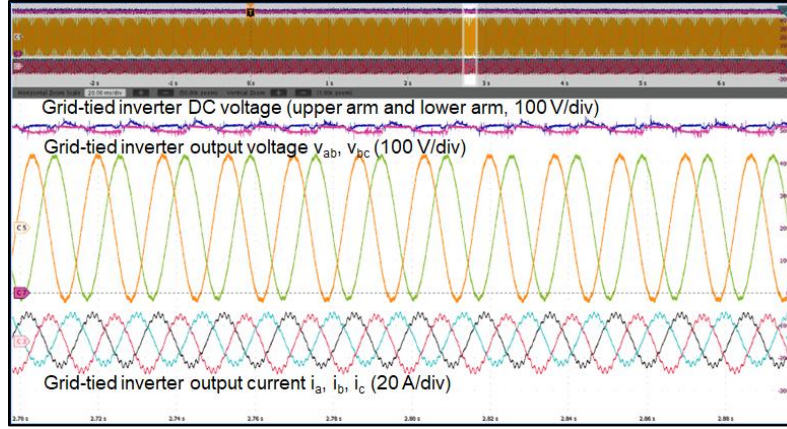


Figure 5-20 Waveforms of the inverter 676 terminal during impedance measurement.

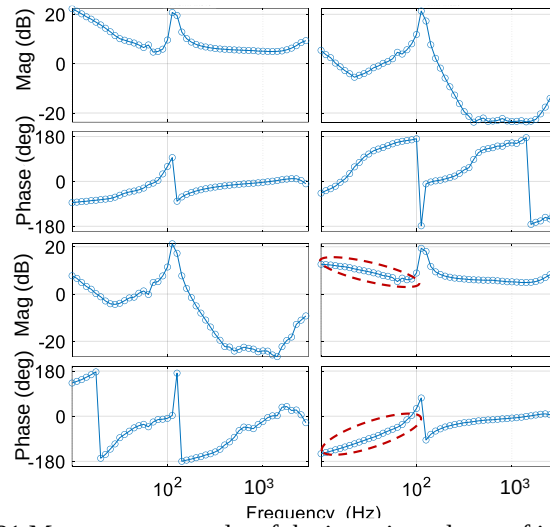


Figure 5-21 Measurement results of the input impedance of inverter 675.

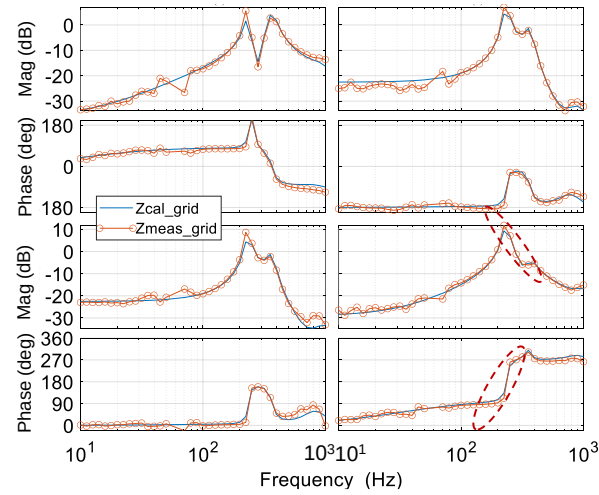


Figure 5-22 Microgrid side impedance: orange curve: measured by the grid-tied inverter 675; blue curve: analytical results based on the model.

5.5.3 Experimental Results

Figure 5-22 shows the test results of the droop operation of the grid-forming converter. The power-frequency droop and reactive power-voltage droop operations can be seen.

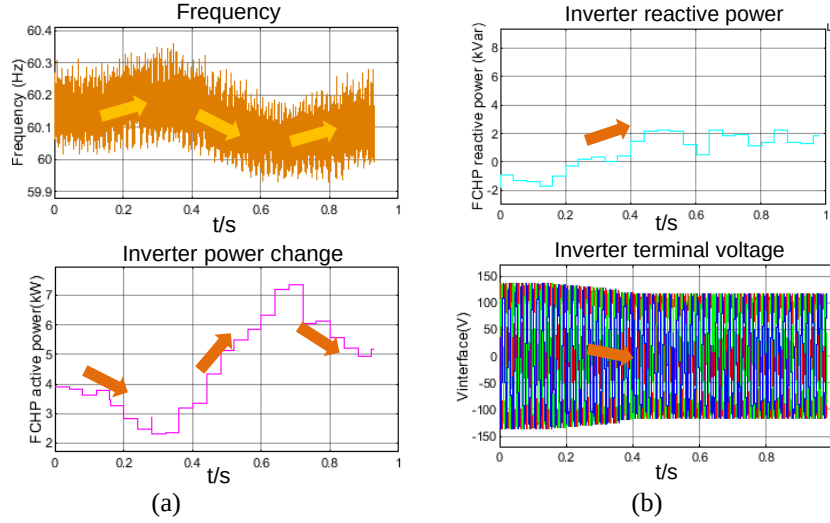


Figure 5-23 Droop operations of the grid-forming converter: (a) P-F droop mode; (b) Q-V droop mode.

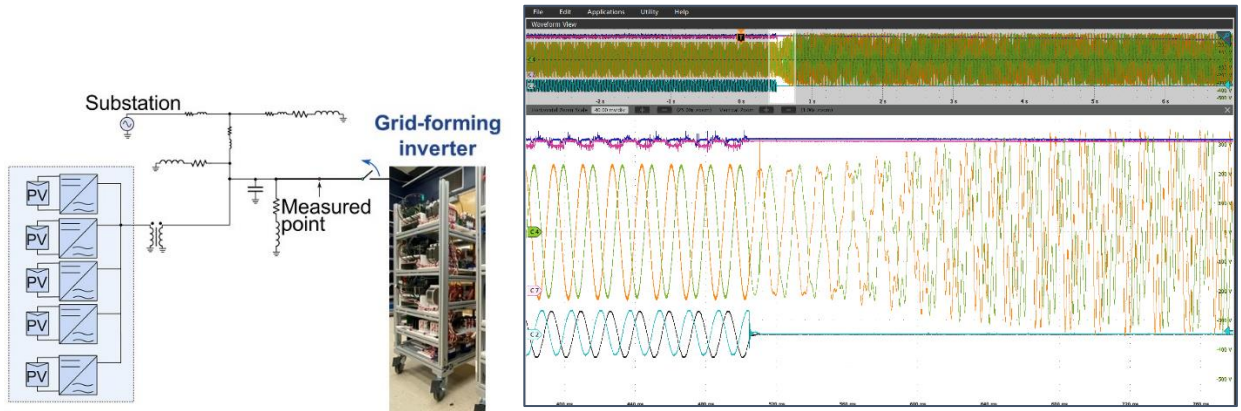


Figure 5-24 Experimental results

Figure 5-23 shows the voltage and current waveforms when the grid-forming converter is disconnected from the rest of the microgrid, and around 300 Hz oscillations can be observed from the terminal voltage, which shows that without the grid-forming converter, the original system becomes unstable. Therefore, with the grid-forming converter (without input voltage feedforward control), the microgrid system has an improved stability margin.

5.6 Summary and Conclusion

This section studies the F-CHP converter's dynamics impact and found that it can help avoid the instability caused by the interactions among PV inverters and the grid network. Therefore, with both keeping the voltage profiles within the limits and a stable operation, the F-CHP converter can help increase the integration capacity of the PV inverters. The instability origin of the system is found to be highly related to the SVC and the Q-V droop of the PV inverters. While removing any of one will avoid instability too but the system voltage profile will not meet requirements with more PV generation. The F-CHP converter could be a solution to these tradeoffs. Experimental verification using a Power-Hardware-in-the-Loop (P-HIL) test setup was carried out. The P-HIL testbed can be used for studying a variety of microgrid configurations without any significant hardware changes.

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Chapter 6

Challenges in Online Impedance-based Stability Analysis: Addressing Open-loop RHP Poles Issues

6.1 Introduction

The increasing integration of converter-based distributed energy sources (DERs) into power grids has created a demand for improved monitoring and control of power system stability. In this regard, impedance-based analysis has emerged as a well-established technique, extensively researched and implemented over the past two decades [1] – [4]. This data-driven approach effectively addresses the challenges posed by inaccessible information and model complexity associated with various grid-connected components. These challenges represent the primary limitations of the conventional eigenvalues approach for stability analysis [5], [6]. Impedance information can be acquired through modeling or direct measurement.

Given that AC power grids are time-varying, the analysis is typically performed in the d-q frame to enable linearization and small-signal analysis [7] – [9]. For instance, Ref. [10] investigates the stability of a three-phase AC system with constant power loads (CPL) using measured d-q frame impedances. Moreover, impedance-based online stability monitoring has emerged as a modern approach for continuously monitoring a power system's impedance in real time [11]–[13]. This allows quantifying stability margins to handle disturbances, detecting stability issues, and implementing adaptive control to respond more effectively to potential problems. Several studies have explored different injection signals or techniques for online impedance measurements, including binary sequences, ternary sequences, impulse signals, orthogonal pseudo-random sequences, and parametric system identification techniques [13]–[17]. These techniques aim to achieve short injection durations while maintaining high accuracy in impedance estimation.

The online impedance measurement results are primarily utilized for stability analysis, relying on the Generalized Nyquist Criterion (GNC) to facilitate decision-making during operation.

Notably, criteria have been established to ensure an adequate margin in the system, including those based on forbidden regions and norm-based criteria [18]–[20]. However, these stability margin criteria often assume the absence of open-loop right-half-plane (RHP) poles in the return ratio matrix, defined as the product of grid-side impedance and inverter-side admittance. This assumption may not always be valid, particularly with an increasing number of power converters on the grid side, which may cause RHP poles to appear in grid-side impedance. RHP poles have been recognized as a limitation in impedance-based stability analysis [21]. Ref. [22] proposes a single-input-single-output (SISO) Bode plot criterion to identify RHP poles by disregarding PLL dynamics. Ref. [23] offers an impedance model that groups all passive components and converters to avoid RHP poles. However, this model is limited to point-to-point HVDC structures and assumes a passive grid. On the other hand, Ref. [24] suggests a settling-angle-based stability criterion to overcome the need for RHP pole information when using GNC-based criteria within the high-frequency range. Nevertheless, the existing literature has not adequately analyzed the origin of RHP poles in distributed grid network impedance and their solutions within the d-q frame impedance and GNC framework.

Several studies have explored adaptive control strategies that utilize measured impedance to improve system performance and stability. These strategies revolve around adjusting the controller gain based on impedance measurements and stability analysis results [25], [26]. However, it is worth noting that most of these papers assume a passive grid model, simplifying the grid as a combination of inductors in series with resistors. Such a simplification becomes inadequate in the presence of power converters acting as power integration interfaces, disregarding the consideration of RHP poles. Neglecting RHP poles and failing to define appropriate stability margins can result in erroneous grid operations when employing adaptive control strategies.

To address this gap, this section investigates the origin, trajectory on the pole-zero map, and impact of RHP poles in microgrid impedance. This study specifically focuses on examining how grid-tied converters affect the presence of RHP poles in the grid-side impedance of a microgrid system, as illustrated in Figure 6-1. The microgrid system is a scaled-down version of the 4.16 kV IEEE 13-node system [27]. To simplify the analysis, the single-phase loads are removed, and the

power of the distributed loads is adjusted to be balanced among the three phases. At node 675, a grid-tied inverter is utilized to integrate the distributed energy source into the grid, and it is designed with a stability monitoring function that measures the real-time grid impedance. The DERs in the system encompass distributed generation units and electricity storage facilities, such as controlled loads. Therefore, two scenarios are investigated in this study: one involving PV inverters and the other involving constant power loads connected to node 680 in Figure 6-1. This section examines the influence of inverters and rectifiers on the appearance of RHP poles in the measured grid impedance $\mathbf{Z}_{\text{grid}}$ and proposes a stability margin index.

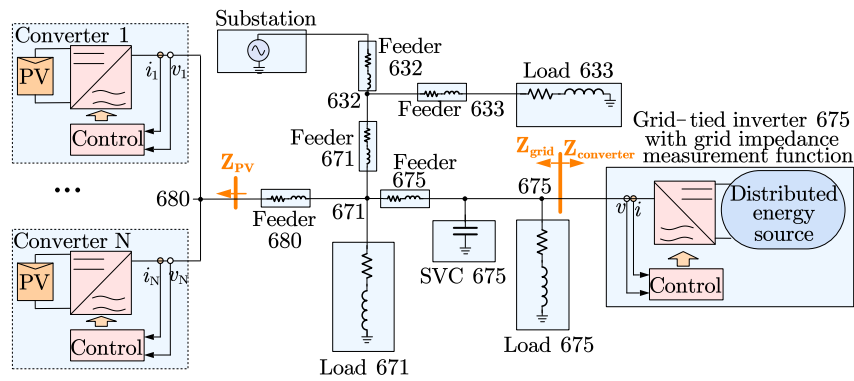


Figure 6-1 Configuration of the microgrid under study.

6.2 Modeling of Terminal Impedance and RHP Poles Feature of Power Converters

The dynamic behavior of the microgrid is altered by many integrated power converters. A converter-level analysis is always a good starting point to reveal the origin and causes of system-level behavior. Therefore, in this section, the converter terminal dq-impedance is modeled, focusing on the RHP poles features of both the inverter and rectifier. The detailed mathematical model results and the converter parameters are shown in Table 6-1.

Table 6-1. Parameters of components in Figure 6-1

Symbol	Descriptions	Value
V_R	Rated voltage	416 V _{llrms}
P	Rated power	25 kW
L_1	LCL filter side inductance	700 μ H
C_f	LCL filter capacitance	25 μ F
L_2	LCL filter grid-side inductance	100 μ H
R_f	LCL filter damping resistance	0.3 Ω
f_{sw_PV}	Switching frequency	20 kHz

V_{dc}	DC bus voltage	870 V
C_{dc}	DC bus capacitance	8 mF
R_{dc}	Rectifier load resistor	30.28 Ω
k_{ppll}	PLL PI proportional gain	1
k_{ipll}	PLL PI integral gain	10
k_{pi}	Current controller PI proportional gain	0.0036
k_{ii}	Current controller PI integral gain	20
k_{pv}	CPL voltage controller PI proportional gain	10
k_{iv}	CPL voltage controller PI integral gain	187

6.2.1 PLL-based Grid-tied Inverters

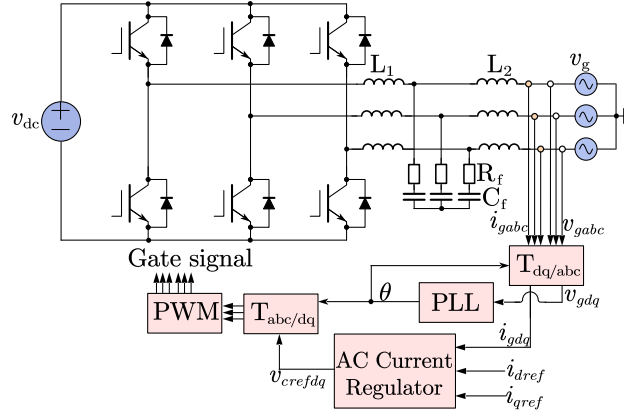


Figure 6-2 Circuit and control diagram of a grid-tied inverter.

Figure 6-2 shows the circuit topology and control diagram of a PLL-based grid-tied voltage source inverter with an LCL filter. For the sake of simplicity, a single series damping resistor is chosen for the LCL filter damping branch. The resistance is designed as 0.3 Ω to attenuate switching harmonics at both the resonance peak and the high-frequency range [28]. It can serve as the second stage of a PV inverter. The first stage is PV panels with a DC-DC converter with output voltage control. Here, the DC side of the converter is assumed to be a constant voltage source. The synchronization angle used for the Park's transform is generated by tracking the terminal voltage with a 20 Hz-bandwidth PLL. A proportional-integral (PI) controller with 1 kHz bandwidth controls the AC current in the d-q frame. The current reference is kept constant. After modeling the converter in the d-q frame, the small-signal impedance of the inverter in the d-q frame can then be determined at a specific operating point [7]. Figure 6-3 illustrates the analytical results of the PV inverter terminal impedance at rated conditions. The PLL results in a negative resistor characteristic at low frequency in the Z_{qq} term. Figure 6-4 illustrates the pole-zero map of the PV impedance. It shows an RHP pole in the Z_{qq} term. The decreasing magnitude and increased

phase feature of the RHP pole can also be seen around 100 Hz in the Bode plot. The same RHP pole also appears in Z_{dq} and Z_{qd} terms due to the coupling between the d and q axes. To show the RHP pole of Z_{qq} analytically, a simplified model for deriving Z_{qq} is shown in Figure 6-5. The PLL dynamics cause the perturbation propagation from the input voltage to the voltage and current in the controller dq frame through the Parks' transformation angle, which is denoted by $\mathbf{G}_{pll}^i$ and $\mathbf{G}_{pll}^v$, respectively. $\mathbf{Z}_{PLL_ic}^{-1}$ is the simplified impedance model considering only current control. The expressions of $\mathbf{G}_{pll}^i$, $\mathbf{G}_{pll}^v$ and $\mathbf{Z}_{PLL_ic}$ are shown in the Appendix. Figure 6-5 yields a simplified model of Z_{qq} as

$$Z_{qq} \approx \frac{V_{dc} k_{ii} (s^2 + V_d k_{ppll} s + V_d k_{ipll})}{s^3 + I_d V_{dc} k_{ii} k_{ppll} s + I_d V_{dc} k_{ii} k_{ipll}} . \quad (6-1)$$

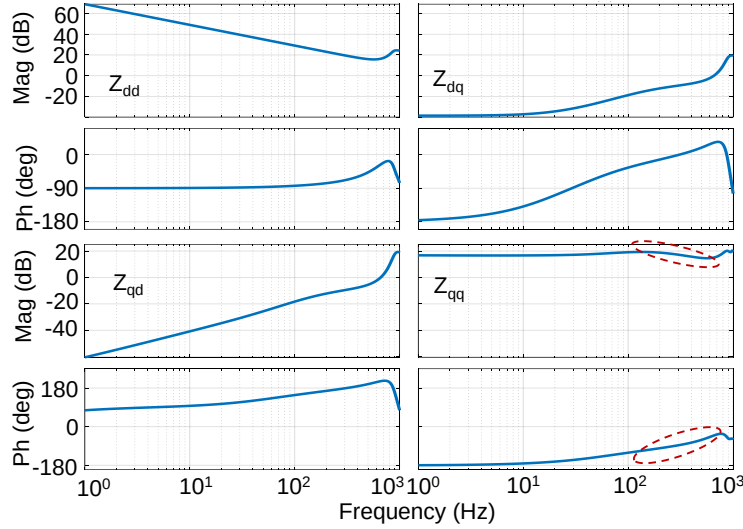


Figure 6-3 Impedance analytical result of a PLL-based grid-tied inverter.

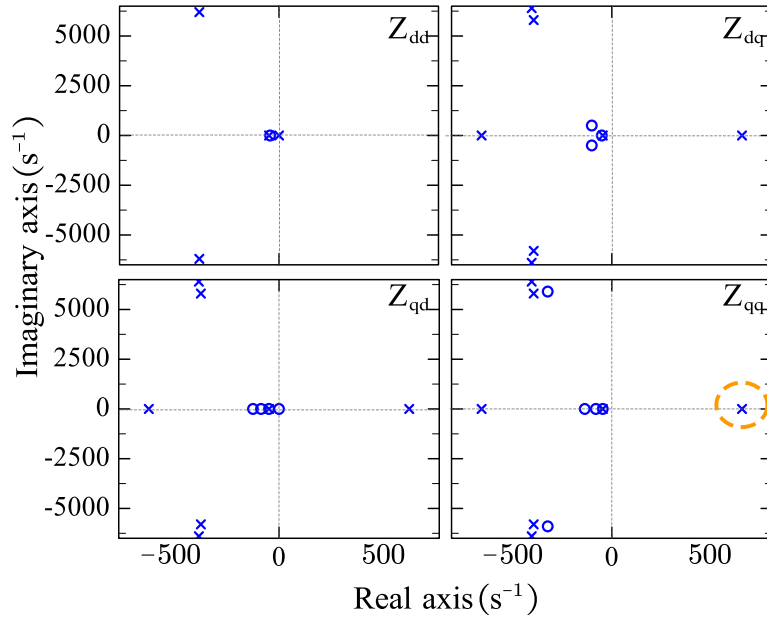


Figure 6-4 The pole-zero map of PLL-based grid-tied inverter impedance.

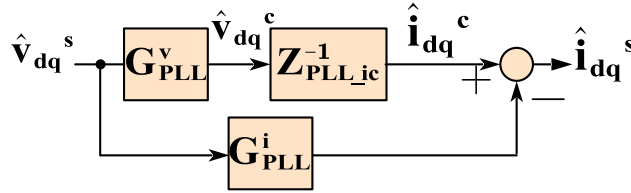


Figure 6-5 Simplified small-signal model of the inverter with PLL dynamics.

The RHP pole location of Z_{qq} can be derived as

$$RHPp_{inv} = \sqrt[3]{-\frac{b}{2} + \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}} + \sqrt[3]{-\frac{b}{2} - \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}} \quad (6-2)$$

where $a = I_d V_{dc} k_{ii} k_{ppll}$ and $b = I_d V_{dc} k_{ii} k_{ipll}$.

6.2.2 Rectifiers with DC Voltage Controller

The microgrid may also contain three-phase rectifiers with DC voltage controllers, such as constant power loads. Figure 6-6 shows the circuit topology and control diagram of a rectifier. The power rating, voltage rating, and power-stage circuit parameters of the rectifier are the same as the inverter. Additionally, a DC voltage control with a PI controller is implemented. The bandwidths of the PLL, current, and voltage control are 20 Hz, 1 kHz, and 80 Hz, respectively, which is a typical range of parameters for standardized converter design.

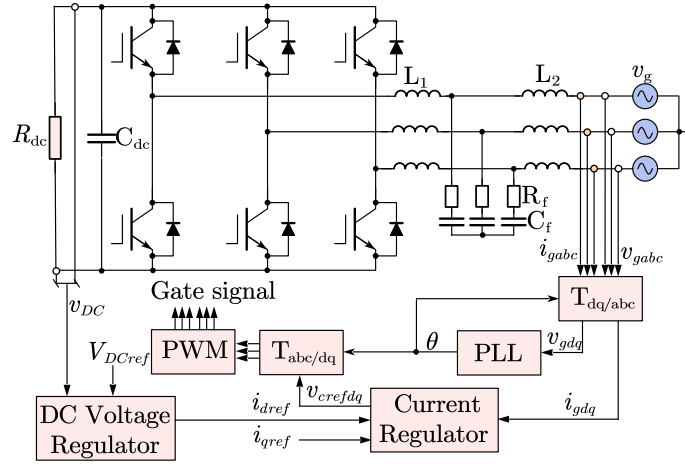


Figure 6-6 Circuit and control diagram of a rectifier.

Figure 6-7 illustrates the analytical results of the rectifier terminal impedance at the rated condition. The DC voltage control results in a negative resistor feature at low frequency in Z_{dd} . Figure 6-8 illustrates the pole-zero map of the rectifier impedance under two different control conditions: the blue mark is with only PLL and the current loop, and the orange mark is with the DC voltage control's dynamics. The pole map shows one RHP pole in the Z_{dd} term resulting from the DC voltage control. The decreasing magnitude and increased phase feature of the RHP pole can also be seen around 200 Hz in the Bode plot. The same pole also appears in Z_{dq} and Z_{qd} terms due to the coupling between the d and q axes.

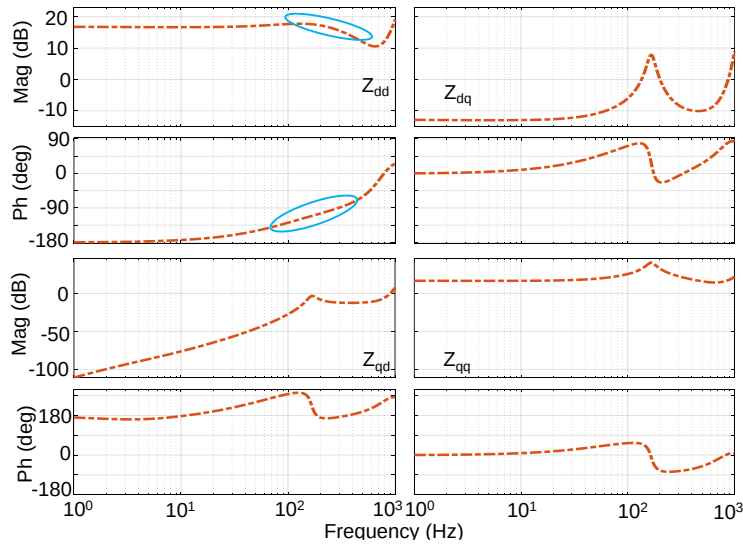


Figure 6-7 Impedance analytical result of the rectifier.

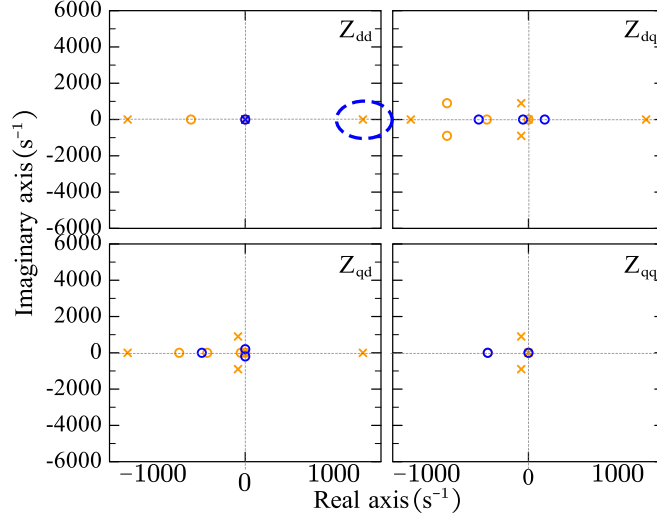


Figure 6-8 The pole-zero map of the rectifier impedance: blue mark: with PLL and current control, orange mark: with PLL, current control, and voltage control.

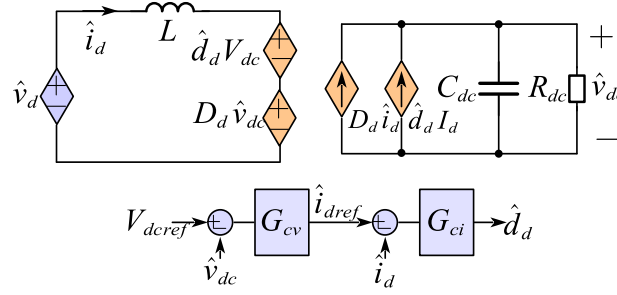


Figure 6-9 Simplified d-channel small-signal model of the rectifier.

This approximate RHP pole location can be found by deriving a simplified model of the rectifier considering just the d channel and the DC voltage and current control, as is shown in Figure 6-9. The input impedance can then be derived as

$$Z_{dd} = \frac{\hat{v}_d}{\hat{i}_d} = sL - G_{ci}V_{dc} + \frac{(D_d - G_{cv}G_{ci}V_{dc})(D_d - G_{ci}I_d)}{sC_{dc} + 1/R_{dc} + G_{cv}G_{ci}I_d}, \quad (6-3)$$

$$G_{ci} = -\left(k_{pi} + \frac{k_{ii}}{s}\right), \quad G_{cv} = k_{pv} + \frac{k_{iv}}{s}. \quad (6-4)$$

The characteristic polynomial of (6-3) is

$$s^4 C_{dc} + s^3 (1/R_{dc} + k_{pv}k_{iv}I_d) - s^2 I_d (k_{pv}k_{ii} + k_{iv}k_{pi}) - sI_d k_{iv}k_{ii} = 0 \quad (6-5)$$

An RHP pole can be derived from (6-5) as

$$RHPp_{rec} \approx \frac{-(1/R_{dc} + k_{pv}k_{iv}I_d)}{2C_{dc}} + \frac{\sqrt{(1/R_{dc} + k_{pv}k_{iv}I_d)^2 + 4C_{dc}I_d(k_{pv}k_{ii} + k_{iv}k_{pi})}}{2C_{dc}} \quad (6-6)$$

The Z_{qq} doesn't exhibit RHP poles with the design parameters when the PLL bandwidths and current loop bandwidth deviate (> 10 times difference). A double RHP pole may also appear in Z_{qq} if the two bandwidths are significantly close. Figure 6-10 shows the Z_{qq} if increasing the PLL bandwidths to 100 Hz and reducing the current control bandwidths to 200 Hz. A pair of double RHP poles appear at around 60 Hz. However, this might not be common since it is more practical to design a much slower PLL control loop than the current loop.

From the analysis above, the inverter and rectifier terminal impedance with a standardized design has inherent RHP poles due to the controller. They can operate with a voltage source stably though they have RHP poles in their terminal impedance.

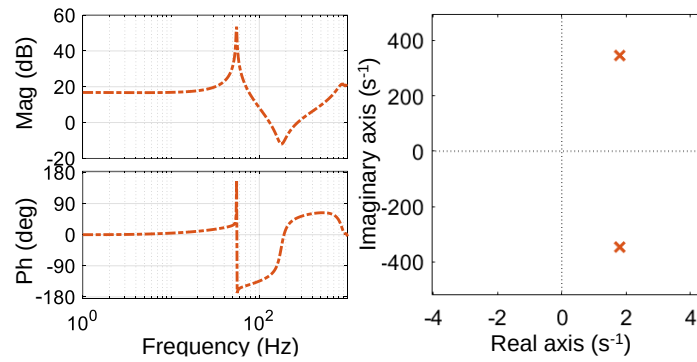


Figure 6-10 The rectifier's q-q channel impedance and its RHP pole when the PLL bandwidth is 100 Hz, and the current bandwidth is 200 Hz.

6.3 RHP Poles Trajectory of System Impedance

When the power converters are connected to the grid to integrate renewable energy or provide power for the loads, these converters will impact the whole microgrid impedance. At the same time, the impact from the converters is altered because of the existence of passive components in the grid. This section aims to study how the grid-tied converters' inherent RHP poles impact the microgrid's terminal impedance and provide some insight into the possible reasons for the appearance of RHP poles. As shown in Figure 6-1, a microgrid is used as an example. The parameters of the system are shown in Table 6-2.

Table 6-2. Power stage parameters and control parameters for Sections II and III

Symbol	Simulation Values	Experimental Values
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Feeder 632	39.4 m Ω , 306.9 uH	11.4 Ω , 88.6 uH
Feeder 633	21.2 m Ω , 91.8 uH	6.1 Ω , 26.5 uH
Feeder 671	38.7 m Ω , 310.8 uH	11.2 Ω , 89.7 uH
Feeder 675	22.5 m Ω , 33.7 uH	6.5 Ω , 9.73 uH
Feeder 680	19.3 m Ω , 155.4 uH	5.6 Ω , 44.8 uH
Load 633	51.9 Ω , 46 mH	4.3 Ω , 3.8 mH
Load 671	26.0 Ω , 23 mH	2.2 Ω , 1.9 mH
Load 675	26.0 Ω , 23 mH	2.2 Ω , 1.9 mH
SVC 692	306.6 uF	1.1 mF

The grid-tied inverter 675 can supply power and measure the microgrid-side impedance $\mathbf{Z}_{\text{grid}}$. With its inward impedance available by either modeling or measuring, the system stability can be assessed by applying GNC to the minor loop gain as in (6-7). The upstream is the microgrid, and the inverter 675 is defined as the downstream to avoid the RHP poles of the inverter impedance's impact.

$$\mathbf{L} = \mathbf{Z}_{\text{grid}} \mathbf{Y}_{\text{converter}} \quad (6-7)$$

The conventional grid mainly comprises passive components that don't have RHP poles in their impedance. So, in practice, it is generally just checking the encirclements of (-1, 0) to determine the system stability. However, this assumption may not always be valid with many grid-tied inverters integrating the renewables. The following study considers two factors, mainly the total number of inverters, denoting the total power integration, and the PLL bandwidths of the inverters since the PLL-based control causes the inverter impedance inherent RHP poles. All the inverters are assumed to work in the same conditions at 25 kW. The substation bus voltage is set as 1.025 p.u., and the passive loads and feeders' parameters are shown in the Table 6-2. The d-q impedance is referred to phase a's voltage phase at node 675, where the grid-tied inverter 675 is connected. It is important to note that the system is stable for all the cases shown below.

Figure 6-11 shows the pole-zero map of the q-q term of the $\mathbf{Z}_{\text{pv}}$ and $\mathbf{Z}_{\text{grid}}$ with different total power while all the inverters' PLL control parameters are kept the same with around 54 Hz bandwidth. The original RHP poles seen at node 680 change slightly due to the voltage level change due to the different power flow. While when looking at node 675, the corresponding poles of the microgrid impedance move to the right with the increase of PV power and start to locate at the right-half plane when the power exceeds 75 kW. Figure 6-12 shows the pole-zero map of the

q-q term of the $\mathbf{Z}_{pv}$ and $\mathbf{Z}_{grid}$ with different inverter PLL parameters while only three inverters are connected in the system, so the total power is 75 kW. The original RHP poles at node 680 change with the different PLL parameters. In node 675, the microgrid impedance has poles that move to the right with the increase of inverter PLL bandwidth and are located at the right-half plane when the PLL bandwidth reaches 50 Hz in the studied system. For both Figure 6-11 and Figure 6-12, the frequency range of the possible RHP poles of $\mathbf{Z}_{grid}$ is close to the original RHP poles of $\mathbf{Z}_{pv}$. Therefore, it can be concluded that the RHP poles of $\mathbf{Z}_{pv}$ produced by the PLL-based control may cause RHP poles as well in $\mathbf{Z}_{grid}$ under high inverter generation or inverter PLL bandwidths. To get an insight into this phenomenon, a simplified system is studied, as shown in Figure 6-13. The microgrid is composed of N inverters in parallel, and the grid side contains an inductive and resistive feeder and a capacitor. The inverter terminal impedance is diagonally dominant in this condition. If ignoring the cross-coupling terms, the grid impedance can be calculated using (6-8).

$$\mathbf{Z}_{grid} = \text{inv}(\mathbf{N} \cdot \mathbf{Y}_{pv} + \mathbf{Y}_{cg} + \mathbf{Y}_g) \approx \begin{bmatrix} Z_{dd} & 0 \\ 0 & Z_{qq} \end{bmatrix} \quad (6-8)$$

$$Z_{qq} \approx 1 / \left(\frac{1}{sL_g + R_g} + sC_g + \frac{N}{Z_{pv_qq}} \right) \quad (6-9)$$

The pole of Z_{qq} appears where,

$$\frac{N}{Z_{pv_qq}} = - \left(\frac{1}{sL_g + R_g} + sC_g \right) \quad (6-10)$$

The points where the impedance of the PV inverters and the combined impedance of other passive components intersect are the locations where the poles of the Z_{qq} transfer function occur. The dominant RHP pole of Z_{pv_qq} is denoted as p_0 . If assuming (6-11) near the intersection point of Z_{pv} and the combined impedance of other passive components,

$$Z_{pv_qq} = \frac{K}{s - p_0} \quad (6-11)$$

(6-10) becomes as follows.

$$s^2 + s(a_1 - a_2) + \frac{K/N - p_0 R_g}{(C_g K/N + 1)L_g} = 0 \quad (6-12)$$

$$a_1 = R_g / L_g \quad (6-13)$$

$$a_2 = p_0 / (C_g K/N + 1) \quad (6-14)$$

The position of the poles of Z_{qq} in the complex plane (right-half-plane or left-half-plane) is determined by a_1 and a_2 . When $a_2 > a_1$, the poles are in the right half plane. As the number and power generation of PV inverters increases, a_2 increases, and at some points, $a_2 > a_1$, which can cause the poles of Z_{qq} to move into the right half-plane. Additionally, as the PLL bandwidth increases, K decreases, causing a_2 to increase, and at some points, $a_2 > a_1$, the poles of Z_{qq} move to the right half-plane. This analysis matches the changes in Figure 6-11 and Figure 6-12.

A case study of the simplified system is carried out. The grid inductance (L_g), resistance (R_g), and capacitance (C_g) are set to 2 mH, 0.088 Ω , and 46 μ F, respectively. Figure 6-14 depicts the current at node O, demonstrating a stable operation of the system. Figure 6-15 (a) illustrates the RHP pole of the PV inverter terminal impedance (Z_{pv}) caused by the PLL-based control. Figure 6-15 (b) displays the RHP poles of the combined grid-side impedance (Z_{grid}). Figure 6-16 shows the q-q channel impedance of Z_{pv} , Z_{grid} , and the combined impedance of the passive components, including the feeder and the capacitor. This case study shows that the RHP pole of Z_{grid} may occur at the intersection of the passive components' impedance and the PV inverter impedance, which is located near the RHP pole of the Z_{pv} , matching the analysis in (6-12) ~ (6-14).

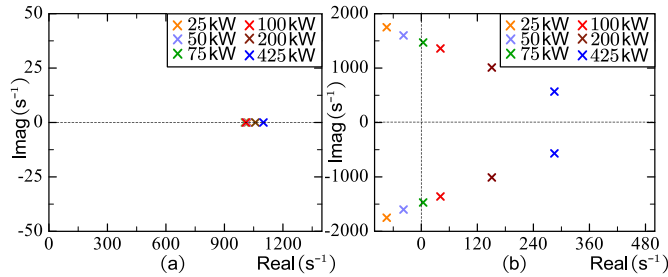


Figure 6-11 Pole-zero map of (a) Z_{pv_qq} (b) Z_{grid_qq} with different PV power and 54 Hz PLL bandwidth.

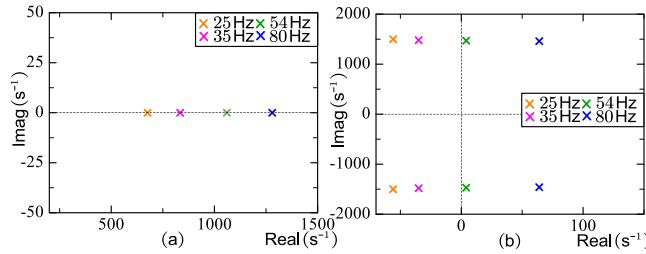


Figure 6-12 Pole-zero map of (a) Z_{pv_qq} (b) Z_{grid_qq} with different PLL bandwidths at 75 kW.

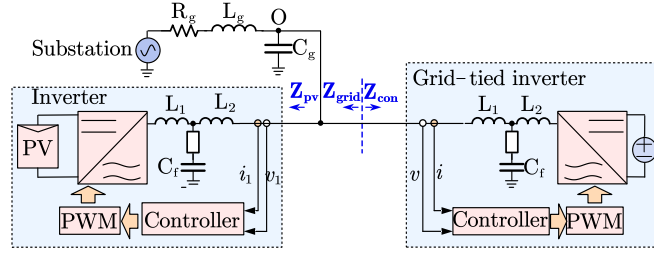


Figure 6-13 Configuration of the simplified system to analyze RHP poles of Z_{grid} .

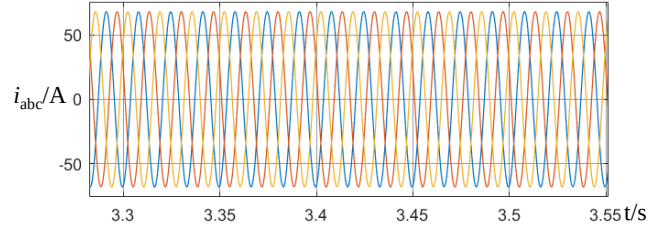


Figure 6-14 Simplified system current waveforms at node O.

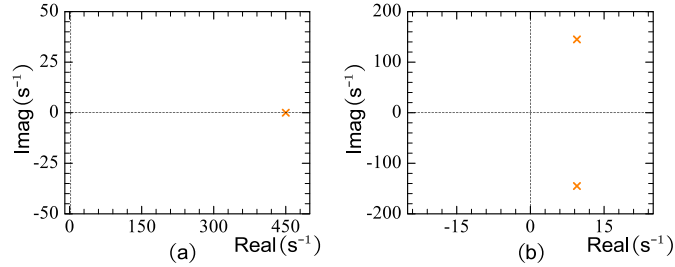


Figure 6-15 RHP pole of (a) Z_{pv_qq} ; (b) Z_{grid_qq} of the simplified system

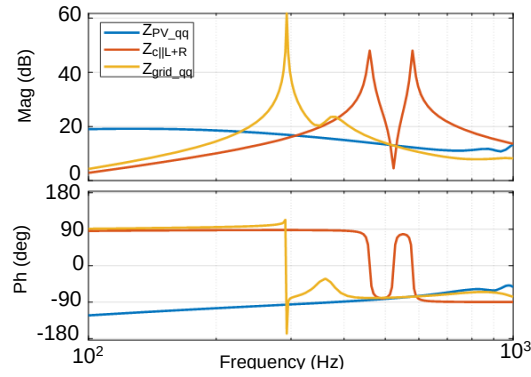


Figure 6-16 The q-q channel impedance of PV inverter, grid passive components, and aggregated impedance.

6.4 Experimental Verification using the PHIL Testbed

6.4.1 Verification of the Microgrid Impedance RHP Poles Trajectory Study with Inverters and Rectifiers

The previous two sections show that the inherent RHP poles of the grid-tied converters may cause RHP poles to appear in the whole microgrid terminal impedance under certain conditions, such as with high converter power levels, high PLL bandwidth, or high DC voltage control bandwidth. To verify this analysis, an experimental study is carried out. The study is divided into two parts: one is with the PLL-based inverters connected to node 680, and the other is with DC voltage control-based rectifiers connected to node 680. The substation voltage level is set at 120 V for all the tests below. For the first set of cases, the inverters' power and PLL parameters are changed to study the trajectory of the possible RHP poles in the microgrid impedance. The system parameters for this scenario are shown in Table 6-3. The grid-tied inverter 675 has a switching frequency of 20 kHz. The system behavior being tested has included any switching dynamics' impact. The system remains stable for all cases except Case 4. The microgrid impedance of all cases except Case 4 is measured by inverter 675. For Case 4, the system becomes unstable, so it is not feasible to perform impedance measurement; therefore, the microgrid impedance is calculated through analytical results based on an approximated operating point. The impedance results are in frequency response format. Then, the impedance is fitted to obtain the corresponding transfer function. The pole-zero information of the impedance can then be extracted. The pole-zero maps of the q-q element of the impedance of the cases in Table 6-2 are shown in Figure 6-17 ~ Figure 6-19. Case 1 to Case 4 is designed with different inverters' output currents but with all other parameters being the same. These cases are used to study the currents' impact on the appearance of the RHP poles. From Figure 6-19, it's seen that with the increase of inverter output current, the corresponding poles of the impedance move to the right and possibly would cross the Imaginary axis and locate in the right-half plane. Case 3, Case 5, and Case 6 are compared to study the impact of the total number of PV inverters integrated on the trajectory of the corresponding poles. From Figure 6-17, more inverters in parallel denoting more renewable integration cause the corresponding poles to move to the right and may be located at the right-half plane. Case 3, Case 7, Case 8, and Case 9 are designed with different PLL controller parameters and bandwidths.

Increasing the PLL bandwidth also results in the corresponding poles moving to the right and may end up in the right-half plane if the PLL bandwidths are high enough, as is shown in Figure 6-18. These test results provide more evidence and strengthen the analysis of the system with inverters illustrated in the previous two sections.

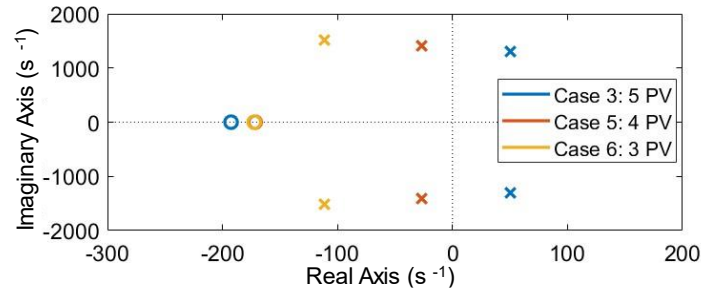


Figure 6-17 Poles trajectory of Z_{grid_qq} with different numbers of inverters integrated.

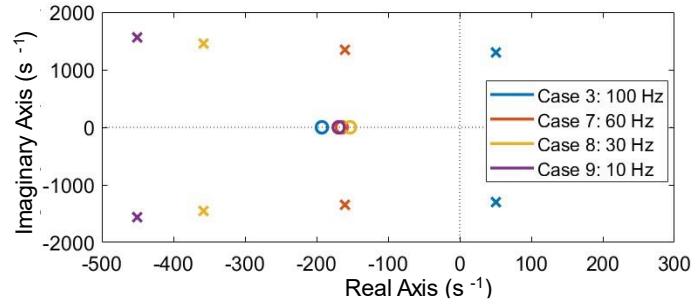


Figure 6-18 Poles trajectory of Z_{grid_qq} with different inverters PLL bandwidths.

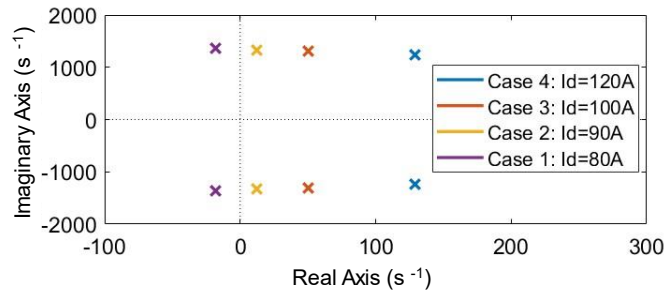


Figure 6-19 Poles trajectory of Z_{grid_qq} with different inverters current.

Table 6-3. System parameters for test 1: with inverters in node 680

No. Case	Number of PV inverters connected	Inverters I_{dref}	Inverters PLL bandwidth	System stability
Case 1	5	80	100 Hz	Stable
Case 2		90		

Case 3		100		Unstable
Case 4		120		
Case 5	4	100		Stable
Case 6	3			
Case 7	5			
Case 8				
Case 9				
		60 Hz		
		30 Hz		
		10 Hz		

The second set of tests is about the microgrid with rectifiers and studies the impact of the rectifier impedance's RHP poles caused by the DC voltage controller. Table 6-4 shows the parameters of the six cases for this test. All six cases are stable. The microgrid impedance of each case is measured by inverter 675. The pole-zero maps of the q-q element of the impedance of the cases in Table 2 are shown in Figure 6-20 and Figure 6-21.

Case 1 ~ Case 4 has 4 rectifiers connected in parallel to node 680, while the DC voltage controller parameters are changed for each case. The corresponding DC voltage bandwidths are changed. With the increased DC voltage loop bandwidth, the corresponding poles move to the right and may be located at the right-half plane under certain conditions. For Case 5 and Case 6, the DC voltage controller parameters are kept the same, while the number of rectifiers connected to the microgrid is changed. With more rectifiers in the microgrid, there is more tendency to result in RHP poles appearing in the microgrid terminal impedance. These test results provide additional support for analyzing the system with rectifiers presented in the previous sections, reinforcing the conclusions drawn in those sections.

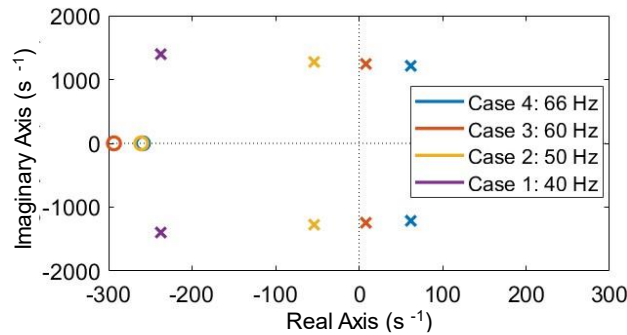


Figure 6-20 Poles trajectory of $Z_{\text{grid_qq}}$ with different DC voltage control bandwidths.

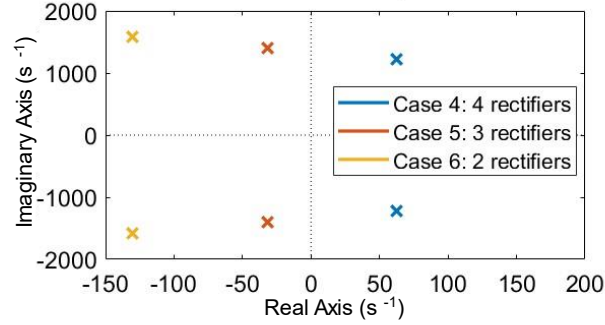


Figure 6-21 Poles trajectory of $Z_{\text{grid_qq}}$ with different numbers of rectifiers.

Table 6-4. System parameters for test 2: with rectifiers in node 680

No. Case	Number of rectifiers connected	Rectifiers' DC voltage bandwidth
Case 1	4	40 Hz
Case 2		50 Hz
Case 3		60 Hz
Case 4		66 Hz
Case 5	3	66 Hz
Case 6	2	

6.4.2 Verification of the impact of RHP poles in stability assessment of the microgrid and a solution

The grid-tied inverter 675 with microgrid-side impedance measurement function terminal impedance has an RHP pole due to the PLL-based control. The usual way of constructing the minor loop gain is by regarding the grid as the source and the inverter as the load to avoid the impact from the RHP poles of inverter impedance, as in (6-7), with the assumption that the grid-side impedance doesn't contain RHP poles.

As is verified in Section 6.3, the microgrid impedance could exhibit RHP poles even when the overall system is stable. If still using (6-7), the minor loop gain could also exhibit RHP poles, such as Case 2 and Case 3 in Table 6-3, and Case 3 and Case 4 in Table 6-4. In these cases, it is no longer valid to only check the encirclements of $(-1, 0)$ to determine the system stability as well as use any forbidden region-based or norm-based stability margin criteria because these are all based on the assumption that there are no RHP poles in the minor loop gain. On the contrary, if using the inverse Nyquist Criterion [19], which is by regarding the grid as the load and the inverter as the

source, as in (6-15), the RHP pole in $\mathbf{Z}_{\text{converter}}$ will still cause the same situation as using the minor loop gain defined by (6-7).

$$\mathbf{L} = \mathbf{Z}_{\text{converter}} \mathbf{Y}_{\text{grid}} \quad (6-15)$$

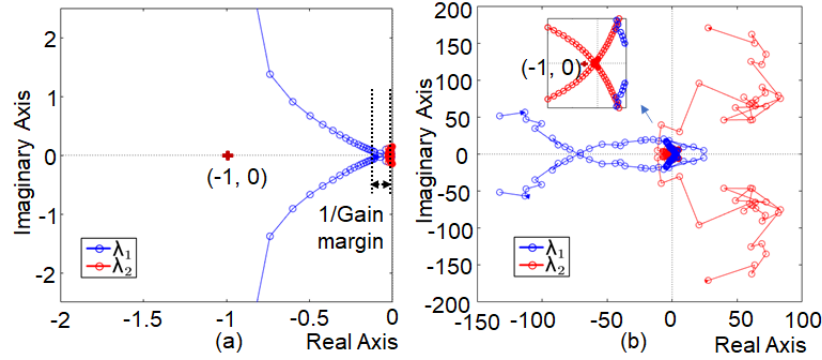


Figure 6-22 Nyquist and inverse Nyquist diagram of Case 1 of Table 1.

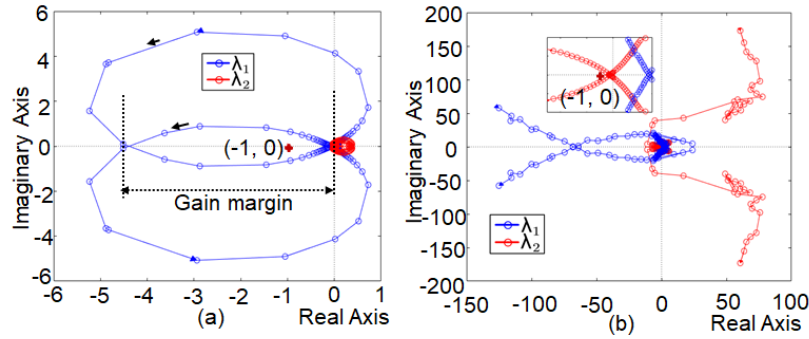


Figure 6-23 Nyquist and inverse Nyquist diagram of Case 2 of Table 1.

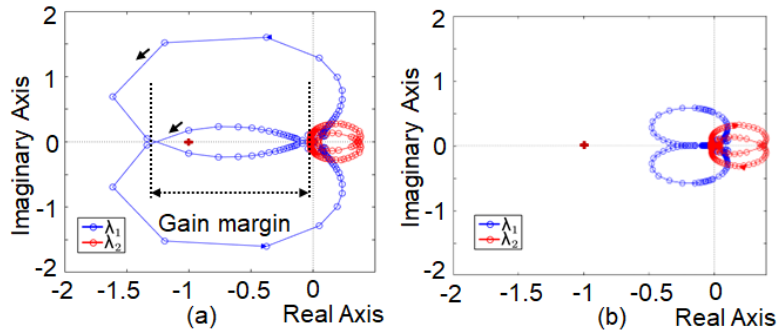


Figure 6-24 Nyquist diagram of (a) Case 3 and (b) Case 4 of Table 1.

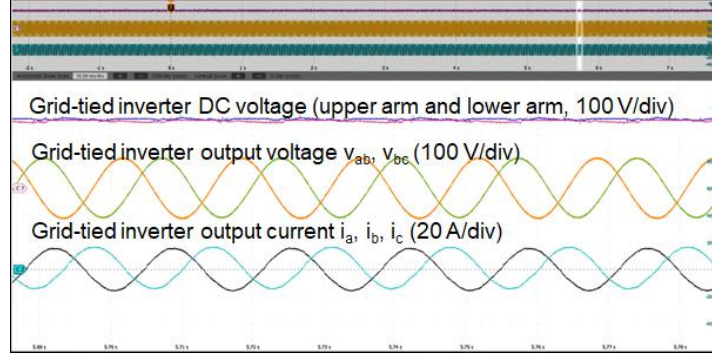


Figure 6-25 Time-domain test waveforms of Case 3 in Table 1.

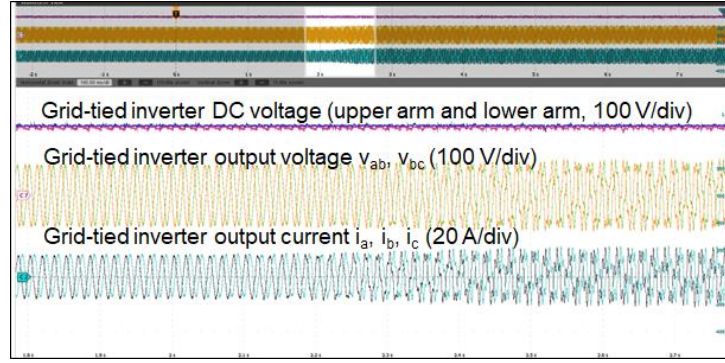


Figure 6-26 Time-domain test waveforms of Case 4 in Table 1.

Case 1~ Case 4 in Table 6-3 is a prime illustration of this. For Case 1, the microgrid impedance doesn't have RHP poles, so the usual way analysis can be implemented as (6-7). Figure 6-22 (a) shows the characteristics of the minor loop gain defined by (6-7), and (b) shows the results using the inverse Nyquist criterion defined in (6-15). Figure 6-22 (a) shows that the system still has a sufficient margin, with no encirclements of $(-1, 0)$ as expected. Figure 6-22 (b) shows one encirclement of $(-1, 0)$, but it still indicates stable operation because of the one RHP pole caused by the grid-tied inverter 675's inward impedance. For Case 2 ~ Case 4, it is still not a good option to use the inverse Nyquist because the RHP poles of grid-tied inverter's impedance; however, using the usual way of defining minor loop gain as (6-7) also would not avoid RHP poles due to the microgrid impedance.

Figure 6-23 (a) shows the characteristic loci of the minor loop gain of Case 2 defined by (6-7), and (b) shows the results using the inverse Nyquist criterion defined as (6-15). Both plots have encirclements of $(-1, 0)$ while the system is stable; therefore, defining a stability margin using any traditional forbidden region-based criteria is not feasible. Figure 6-24 shows the characteristic loci

of Case 3 and Case 4 if defining the minor loop gain as (6-7). Case 3 is stable, and Case 4 is unstable. The time-domain test results are shown in Figure 6-25 and Figure 6-26, respectively. These examples show that if the RHP poles of the microgrid-side impedance are not considered, the online stability assessment could draw a wrong conclusion.

Therefore, stability assessment in grid applications requires knowledge of RHP poles. Pole estimation algorithms can be employed based on the measured impedances during stability monitoring. The conventional forbidden-region criterion can only be used if no RHP pole exists, like in Figure 6-22 (a). Due to the presence of RHP poles, the encirclements of $(-1, 0)$ and stability judgment differ from scenarios without RHP poles. Consequently, a distinct definition of stability margin becomes necessary. This stability margin index is specifically intended for situations where RHP poles are unavoidable. When open-loop RHP poles exist, as depicted in Figure 6-23 (a) and Figure 6-24 (a), the gain margin is defined by taking $\log_{10}$ of the distance between the point where the loci intersect with the negative real axis and the origin $(0, 0)$ on the Nyquist plot. It quantifies how much the gain of the loci can change compared to the current operating condition up to the point where the system becomes unstable. A shrinking characteristic locus towards the right side denotes a reduced gain margin. When the characteristic loci move to the right side of $(-1, 0)$, the gain margin becomes negative, indicating an unstable condition. This proposed index is applicable when RHP poles are present, addressing the gaps in quantifying stability margins for such scenarios. It is a valuable complement to the usual definition of the gain margin in the complex plane, serving as a useful tool for stability analysis when RHP poles cannot be avoided.

Implementing impedance-based stability monitoring involves a centralized central controller communicating with the grid-tied inverter and directing it to constantly measure grid impedance by injecting small disturbances. Concurrently, the central controller can access information from the grid-tied inverter, including its input impedance model. The central controller calculates the grid-tied inverter's impedance using real-time operating point values. With the measured grid impedance and calculated grid-tied inverter impedance, the central controller determines the minor loop gain and obtains characteristic loci, also enabling the detection of RHP poles. Without RHP poles, the system's stability margin can be determined by assessing the distance between the loci

and the critical point (-1, 0). On the other hand, if RHP poles are present, the defined stability margin index is utilized. This process is illustrated in Figure 6-27.

The primary goal of stability monitoring is to provide operational guidance to the system operator. If the stability margin is insufficient, the operator can take appropriate actions to improve it. These actions may include changes in power flow, such as load shedding and renewables integration power shedding, adjusting grid-tied converter's output power, or performing controller tuning. It should be noted that the detailed logic of the necessary actions depends on the specific system in practical application. This could be considered for future work. However, it is not the focus of this study.

Many research papers have proposed specialized converter controls to mitigate specific impedance characteristics, such as the negative resistance induced by PLL or DC voltage control. However, currently, many converters in practical use are designed with a more straightforward approach, incorporating appropriate parameters for the PLL or DC voltage controller to fulfill local converter control objectives. As a result, it is not yet common practice to use those special control designs. This section addresses the critical issue of RHP poles, which can potentially affect systems equipped with commonly designed converters. It would be beneficial as future work to explore other types of converter control designs and investigate if the RHP poles issues also occur for those converters.

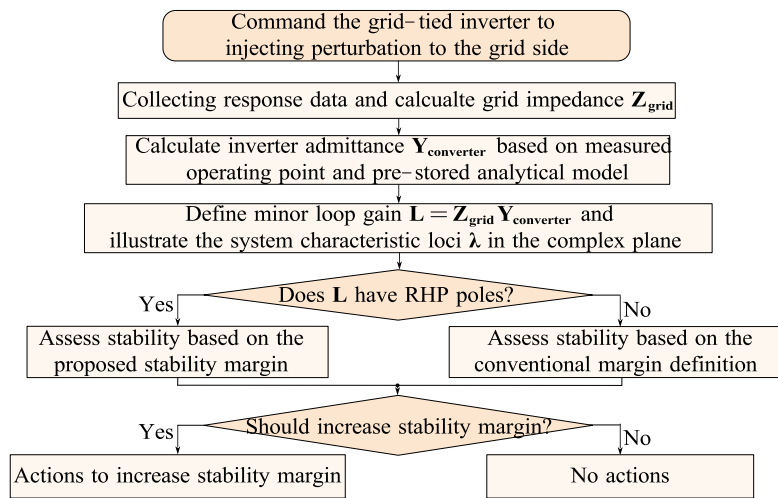


Figure 6-27 Process of impedance-based stability monitoring.

6.5 Summary and Conclusions

In this section, the origin and impact factors of the RHP pole feature of the microgrid impedance are studied; a PHIL testbed was developed to emulate the dynamics of a microgrid and validate the RHP pole study. The conclusions are drawn below.

(1) The DC voltage control results in an RHP pole in a rectifier's d-d channel impedance; the PLL-based control causes an RHP pole in an inverter's q-q channel impedance.

(2) With more inverters or rectifiers in the grids, RHP poles may present in the grid impedance. Higher converter power, higher PLL control bandwidths of the inverter, and higher DC voltage control bandwidths of the rectifier all tend to cause RHP poles to also show up in the whole microgrid impedance.

(3) The presence of RHP poles changes the characteristic loci dramatically; thus, forbidden-region-type stability criteria are no longer applicable. Stability assessment in grid applications requires knowledge of RHP poles. Pole estimation algorithms may be employed based on the measured impedances. New ways of defining the stability margin should be exploited for cases with open-loop RHP poles. This section proposes one kind of stability margin definition to cope with RHP poles

6.6 Reference List of Chapter 6

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Chapter 7

Summary and Conclusions

In this dissertation, analysis of single-phase converters is shown in Chapter 2, Chapter 3, and Chapter 4, analysis of three-phase converters is shown in Chapter 5 and Chapter 6, and the DQ frame modeling concept is employed for both loop gain analysis and impedance analysis. The main work done in this dissertation is summarized as follows.

- 1) Modeled the input impedance in a synchronous dq frame of a single-phase PSU and identified each control loop's impact.
- 2) Proposed an dq-frame-based impedance model within a linear-time-invariant (LTI) framework for stability analysis of an ac system with single-phase PSU loads with experimental validation, including three-phase four-wire system, three-phase three-wire system, and single-phase systems.
- 3) Proposed a dq-frame-based voltage loop gain model of a single-phase PSU when it is presented in a single-phase, a three-phase three-wire, and a three-phase four-wire system, respectively.
- 4) Analyzed the above PSU systems using impedance model and loop gain model.
- 5) Detailed designed a grid-forming converter with grid-support functions compiling IEEE Std 1547.
- 6) Analyzed the grid-forming converter's impact on a microgrid's stability based on impedance analysis.
- 7) Investigated the origin and evolution of RHP poles of impedance in the stability monitoring context of a microgrid and proposed a new stability margin index.

Throughout this work, the following conclusions can be drawn.

- 1) Single-phase PSU input DQ impedance main characteristics include negative resistor load behavior below voltage loop bandwidth of Z_{dd} ; dc-dc converter load causes the gain & phase of Z_{dd} to drop at low frequency.

- 2) The stability analysis of a three-phase four-wire system can be analyzed using 6×6 dq impedance models.
- 3) DQ frame approach is accurate in loop gain modeling: more accurate than the quasi-static approximation in a single-phase system; also valid to be used in a three-phase three/four-wire system.
- 4) The use of additional imaginary “phase-shifted” phases per physical phase is the key to achieving the balanced set of DQ-frames.
- 5) The designed grid-forming converter with grid-support functions compiling IEEE Std 1547 positively impacts a microgrid’s stability.
- 6) The origin of RHP poles in converter terminal impedance are PLL-based control and dc voltage control.
- 7) Higher power and higher control bandwidth of PLL for inverters or dc voltage control for rectifiers, together with SVC, contribute to the emergence of RHP poles in the measured grid impedance. Such RHP poles will lead to wrong conclusions in the GNC-based stability analysis if not appropriately detected. The proposed stability margin index is a solution to such a scenario.

Appendix of Chapter 6

This Appendix explains the small-signal impedance model of the microgrid's inverters, and rectifiers in the simulation study and experimental study.

Figure 8-1 and Figure 8-2 show the small-signal model of the grid-tied inverter and the rectifier in the d-q frame. The $\mathbf{G}_{id}$, $\mathbf{Z}_{in}$, $\mathbf{G}_{vd}$, and $\mathbf{G}_{vv}$ are the power stage transfer function matrixes, $\mathbf{G}_{del}$ denotes the dynamics of the digital controller, $\mathbf{G}_{pll}^i$, $\mathbf{G}_{pll}^v$, and $\mathbf{G}_{pll}^d$ are the dynamics of the PLL control, $\mathbf{G}_{ci}$ and $\mathbf{G}_{dei}$ are the dynamics of the inner current control, and $\mathbf{G}_{cv}$ is the dynamics of the DC voltage control of the rectifier. The terminal impedance of the inverter and the rectifier can be calculated using (8-1) and (8-2).

$$\mathbf{Z}_{inv_pll_cu} = [\mathbf{Z}_{in}^{-1} - \mathbf{G}_{id}\mathbf{G}_{del}((- \mathbf{G}_{dei} + \mathbf{G}_{ci})\mathbf{G}_{PLL}^i - \mathbf{G}_{PLL}^d)]^{-1} \cdot (\mathbf{I} + \mathbf{G}_{id}\mathbf{G}_{del}(- \mathbf{G}_{dei} + \mathbf{G}_{ci})) \quad (8-1)$$

$$\mathbf{Z}_{rec_pll_cu_cv} = \left[\mathbf{Z}_{in}^{-1} + \mathbf{G}_{id}(\mathbf{I} + \mathbf{G}_{del}\mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vd})^{-1}\mathbf{G}_{del} \cdot \right. \\ \left. ((\mathbf{G}_{dei} - \mathbf{G}_{ci})\mathbf{G}_{PLL}^i - \mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vv} + \mathbf{G}_{PLL}^d) \right]^{-1} \cdot (\mathbf{I} + \mathbf{G}_{id}(\mathbf{I} + \mathbf{G}_{del}\mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vd})^{-1}\mathbf{G}_{del}(- \mathbf{G}_{dei} + \mathbf{G}_{ci})) \quad (8-2)$$

$$\mathbf{Y}_{inv_pll_cu} = (\mathbf{I} + \mathbf{G}_{id}\mathbf{G}_{del}(- \mathbf{G}_{dei} + \mathbf{G}_{ci}))^{-1} \cdot [\mathbf{Z}_{in}^{-1} - \mathbf{G}_{id}\mathbf{G}_{del}((- \mathbf{G}_{dei} + \mathbf{G}_{ci})\mathbf{G}_{PLL}^i - \mathbf{G}_{PLL}^d)] \quad (8-3)$$

$$\mathbf{Y}_{rec_pll_cu_cv} = (\mathbf{I} + \mathbf{G}_{id}(\mathbf{I} + \mathbf{G}_{del}\mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vd})^{-1}\mathbf{G}_{del}(- \mathbf{G}_{dei} + \mathbf{G}_{ci}))^{-1} \cdot \left[\mathbf{Z}_{in}^{-1} + \mathbf{G}_{id}(\mathbf{I} + \mathbf{G}_{del}\mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vd})^{-1}\mathbf{G}_{del} \cdot \right. \\ \left. ((\mathbf{G}_{dei} - \mathbf{G}_{ci})\mathbf{G}_{PLL}^i - \mathbf{G}_{ci}\mathbf{G}_{cv}\mathbf{G}_{vv} + \mathbf{G}_{PLL}^d) \right] \quad (8-4)$$

$$G_{PLL} = \frac{sk_{ppll} + k_{ipll}}{s^2 + sk_{ppll}V_d + V_d k_{ipll}} \quad (8-5)$$

$$\mathbf{G}_{PLL}^v = \begin{bmatrix} 1 & G_{PLL}V_{in\ q}^s \\ 0 & 1 - G_{PLL}V_{in\ d}^s \end{bmatrix} \quad (8-6)$$

$$\mathbf{G}_{PLL}^i = \begin{bmatrix} 0 & G_{PLL}I_{L\ q}^s \\ 0 & -G_{PLL}I_{L\ d}^s \end{bmatrix} \quad (8-7)$$

$$\mathbf{G}_{PLL}^d = \begin{bmatrix} 0 & -G_{PLL}D_q^s \\ 0 & G_{PLL}D_d^s \end{bmatrix} \quad (8-8)$$

$$\mathbf{Z}_{PLL_ic} = \begin{bmatrix} \frac{V_{dc} k_{ii}}{s} & 0 \\ 0 & \frac{V_{dc} k_{ii}}{s} \end{bmatrix} \quad (8-9)$$

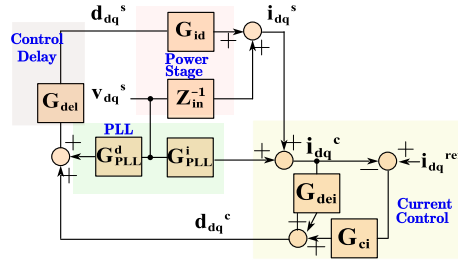


Figure 8-1. Small-signal model of a grid-tied inverter.

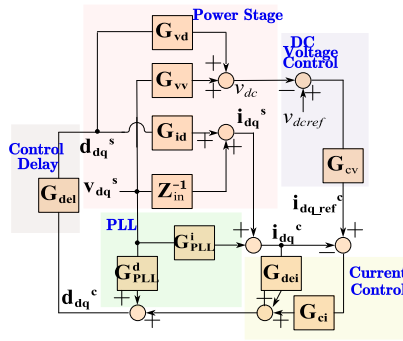


Figure 8-2 Small-signal model of a rectifier.