Circuits and Modulation Schemes to Achieve High Power Density in SiC Grid-connected Converters

Sungjae Ohn

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Dushan Boroyevich (Chair)
Rolando Burgos (Co-Chair)
Khai D.T. Ngo
Guo-Quan Lu
Wei Zhou

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Abstract

The emergence of silicon-carbide (SiC) devices has been a 'game changer' in the field of power electronics. With desirable material properties such as low-loss characteristics, high blocking voltage, and high junction temperature operation, they are expected to drastically increase the power density of power electronics systems. Recent state-of-the-art designs show the power density over 17 kW/dm^3; however, certain factors limit the power density to increase beyond this limit. In this dissertation, three key factors are selected to increase the power density of SiC-based grid-connected three-phase converters. Throughout this dissertation, the techniques and strategies to increase the power density of SiC three-phase converters were investigated.

Firstly, a magnetic integration method was introduced for the coupled inductors in the interleaved three-phase converters. Due to limited current-capacity compared to the silicon insulated-gate bipolar transistors (Si-IGBTs), discrete SiC devices or SiC modules, operate in parallel to handle a large current. When three-phase inverters are paralleled, interleaving can be used, and coupled inductors are employed to limit the circulating current. In Chapter 2, the conventional integration method was extended to integrate three coupled inductors into two; one for differential-mode circulating current and the other for common-mode circulating

current. By comparing with prior research work, a 20% reduction in size and weight is demonstrated.

From Chapter 3 to Chapter 5, a full-SiC uninterruptible power supply (UPS) was investigated. With the high switching frequency and fast switching dynamics of SiC devices, strategies on electromagnetic inference become more important, compared to Si-IGBT based inverters. Chapter 3 focuses on a common-mode equivalent circuit model for a topology and pulse width modulation (PWM) scheme selection, to set a noise mitigation strategy in the design phase. A three terminal common-mode electromagnetic interference (EMI) model is proposed, which predicts the impact of the dc-dc stage and a large battery-rack on the output CM noise. Based on the model, severe deterioration of noise by the dc-dc stage and battery-rack can be predicted. Special attention was paid on the selection of the dc-dc stage's topology and the PWM scheme to minimize the impact. With the mitigation strategy, a maximum 16 dB reduction on CM EMI can be achieved for a wide frequency range.

In Chapter 4, an active PWM scheme for a full-SiC three-level back-to-back converter was proposed. The PWM scheme targets the size reduction of two key components: dc-link capacitors and a common-mode EMI filter. The increase in switching frequency calls for a large common-mode EMI filter, and dc-link capacitors in the three-level topology may take a considerable portion in the total volume. To reduce the common-mode noise emission, different combinations of the voltage vectors are investigated to generate center-aligned single pulse common-mode voltage. By such an alignment of common-mode voltage with different vector combinations, noise cancellation between the rectifier and the inverter can be maximally utilized, while the balancing of neutral point voltage can be achieved by the transition between the combinations. Also, to reduce the size of the dc-link capacitor for the three-level back-to-back converter, a compensation algorithm for neutral point voltage unbalance was developed

for both differential-mode voltage and the common-mode voltage of the ac-ac stage. The experimental results show a 4 dB reduction on CM EMI, which leads to a 30% reduction on the required CM inductance value. When a 10% variation of neutral point voltage can be handled, the dc-link capacitance can be reduced by 56%.

In Chapter 5, a 20 kW full-SiC UPS prototype was built to demonstrate a possible size-reduction with the proposed PWM scheme, as well as a selection of topologies and PWM schemes based on the model. The power density and efficiency are compared with the state-of-the-art Si-IGBT based UPSs.

Chapter 6 seeks to improve power density by a change in a modulation method. Triangular conduction mode (TCM) operation of the three-level full-SiC inverter was investigated. The switching loss of SiC devices is reported to be concentrated on the turn-on instant. With zero-voltage turn-on of all switches, the switching frequency of a three-level three-phase SiC inverter can be drastically increased, compared to the hard-switching operation. This contributes to the size-reduction of the filter inductors and EMI filters. Based on the design to achieve a 99% peak efficiency, a comparison was made with a full-SiC three-level inverter, operating in continuous conduction mode (CCM), to verify the benefit of the soft switching scheme on the power density. A design procedure for an LCL filter of paralleled TCM inverters was developed. With 3.5 times high switching frequency, the total weight of the filter stage of the TCM inverter can be reduced by 15%, compared to that of the CCM inverter.

Throughout this dissertation, techniques for size reduction of key components are introduced, including coupled inductors in parallel inverters, an EMI filter, dc-link capacitors, and the main boost inductor. From Chapter 2 to 5, the physical size or required value of these key components could be reduced by 20% to 56% by different schemes such as magnetic

integration, EMI mitigation strategy through modeling, and an active PWM scheme. An optimization result for a full-SiC UPS showed a 40% decrease in the total volume, compared to the state-of-the-art Si-IGBT solution. Soft-switching modulation for SiC-based three-phase inverters can bring a significant increase in the switching frequency and has the potential to enhance power-density notably. A three-level three-phase full-SiC 40 kW PV inverter with TCM operation contributed to a 15% reduction on the filter weight.

Circuits and Modulation Schemes to Achieve High Power Density in SiC Grid-connected Converters

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General Audience Abstract

The power density of a power electronics system is regarded as an indicator of technological advances. The higher the power density of the power supply, the more power it can generate with the given volume and weight. The size requirement on power electronics has been driven towards tighter limits, as the dependency on electric energy increases with the electrification of transportation and the emergence of grid-connected renewable energy sources. However, the efficiency of a power electronics system is an essential factor and is regarded as a trade-off with the power density. The size of power electronics systems is largely impacted by its magnetic components for filtering, as well as its cooling system, such as a heatsink. Once the switching frequency of power semiconductors is increased to lower the burden on filtering, more loss is generated from filters and semiconductors, thus enlarging the size of the cooling system. Therefore, considering the efficiency has to be maintained at a reasonable value, the power density of Si-based converters appears to be saturated.

With the emergence of wide-bandgap devices such as silicon carbide (SiC) or gallium nitride (GaN), the switching frequency of power devices can be significantly increased. This is a result of superior material properties, compared to Si-based power semiconductors. For grid-connected applications, SiC devices are adopted, due to the limitations of voltage ratings in GaN devices. Before commercial SiC devices were available, the power density of SiC-

based three-phase inverters was expected to go over 20 kW/dm^3. However, the state-of-the-art designs shows the power density around 3 ~ 4 kW/dm^3, and at most 17 kW/dm^3. The SiC devices could increase the power density, but they have not reached the level expected. The adoption of SiC devices with faster switching was not a panacea for power density improvement.

This dissertation starts with an analysis of the factors that prevent power density improvement of SiC-based, grid-connected, three-phase inverters. Three factors were identified: a limited increase in the switching frequency, large high-frequency noise generation to be filtered, and smaller but still significant magnetic components. Using a generic design procedure for three-phase inverters, each chapter seeks to frame a strategy and develop techniques to enhance the power density.

For smaller magnetic components, a magnetic integration scheme is proposed for paralleled ac-dc converters. To reduce the size of the noise filter, an accurate modeling approach was taken to predict the noise phenomena during the design phase. Also, a modulation scheme to minimize the noise generation of the ac-ac stage is proposed. The validity of the proposed techniques was verified by a full-SiC three-phase uninterruptible power supply with optimized hardware design. Lastly, the benefit of soft-switching modulation, which leads to a significant increase in switching frequency, was analyzed. The hardware optimization procedure was developed and compared to hard-switched three-phase inverters.

To My Father,

Ki Sun Ohn

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Chapter 1. Introduction

In this chapter, the motivations, objectives, and an overview of this dissertation are provided. Firstly, the advantages of wide bandgap devices, especially, silicon-carbide (SIC) MOSFETs are reviewed, to clarify their benefits to the grid-connected converters. Also, a survey has been done prepared on the latest design examples of state-of-the-art SiC converters for three-phase applications. From the survey, three main factors which limit the power density of SiC three-phase converters were chosen to define the scope of this dissertation. Moreover, this chapter provides a review of this field, followed by the dissertation outline, and the scope of research.

1.1 Silicon Carbide Devices

Silicon (Si)-based insulated-gate bipolar transistors (IGBT) have been an industry standard for several decades. Mature Si-based technologies enabled low loss characteristics, and high reliability, with low manufacturing cost. With state-of-the-art technologies, the voltage-rating of commercial IGBTs is limited to a 6.5 kV level. The maximum junction temperature is limited to 150℃ in general. The switching frequency of a 1.2 kV or 1.7 kV Si-IGBT for commercial grid-connected converters is normally limited to 20 kHz, due to the switching-loss. However, the performance of a Si-IGBT seems to approach its theoretical limits.

Wide-bandgap (WBG) devices have been expected to be a future replacement for Si-IGBTs, as a result of their superior material performance over silicon. Among various WBG materials,

Silicon carbide (SiC) and gallium nitride (GaN) have proven to be the most promising technologies. The material properties are summarized and compared with that of their Si counterpart in Fig. 1-1 [1]. WBG devices provide higher voltage-ratings, higher switching frequencies, and higher operating temperature ranges, compared to Si-IGBTs.

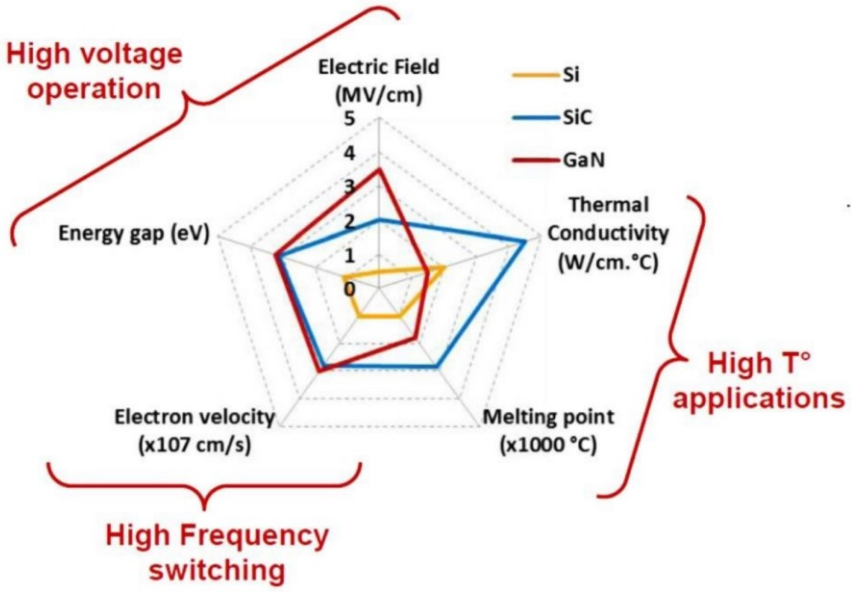


Fig. 1-1. Comparison for material characteristics of WBG devices [1].

SiC devices are considered for ac-dc applications where the dc-link voltage is over 400 V since the voltage rating of commercial GaN devices is limited to 600 V. Currently, Wolfspeed has announced that a voltage-rating of 10 kV will be available for their Gen. 3 SiC MOSFETs. This is 40% higher than the maximum voltage-rating of a mature Si-IGBT [2]. In literature, the switching frequencies of SiC three-phase converters move to near 70 kHz while maintaining good efficiency (>98.5%); the switching frequencies of the state-of-the-art Si-IGBT converters are limited to below 20 kHz [3]. SiC devices can be operated at 200℃ and can be used in

applications where operations in extreme environments are required, such as those in aerospace and the military.

For three-phase low-voltage grid applications, 1.2 kV and 1.7 kV SiC MOSFETs and modules are available from various manufacturers such as Wolfspeed, Rohm, Microchip, STMicroelectronics, General Electric (GE), etc. Improvements in the manufacturing process and massive production enabled the cost reduction of SiC MOSFETs since their first appearance in 2011, as shown in Fig. 1-2 [4]. The trends and prediction for 3.3 kV, 10 kV devices are shown in Fig. 1-3 and Fig. 1-4. The prices for 1.2 kV devices with a current rating between 20 A and 40 A are compared in Table 1-1, based on the pricing on Digikey, as of early 2019. The price of SiC MOSFETs is in the range of 2 ~ 4 times that of Si-IGBTs, enhancing their potential as a replacement. The era of SiC MOSFETs seems to be getting close.

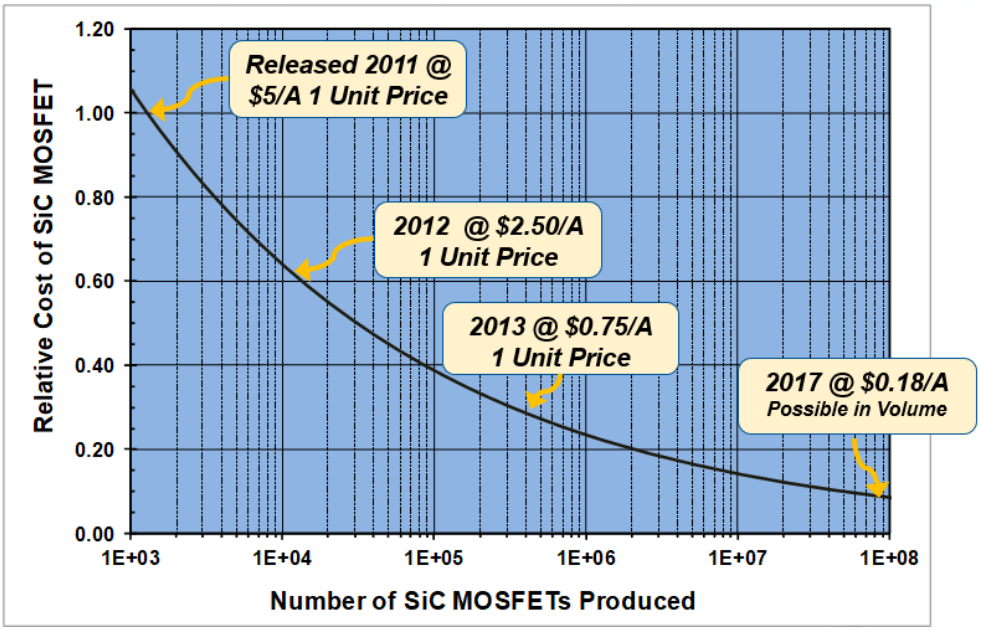


Fig. 1-2. Projected cost trend of 1.2 kV SiC MOSFETs in 2014 [4].

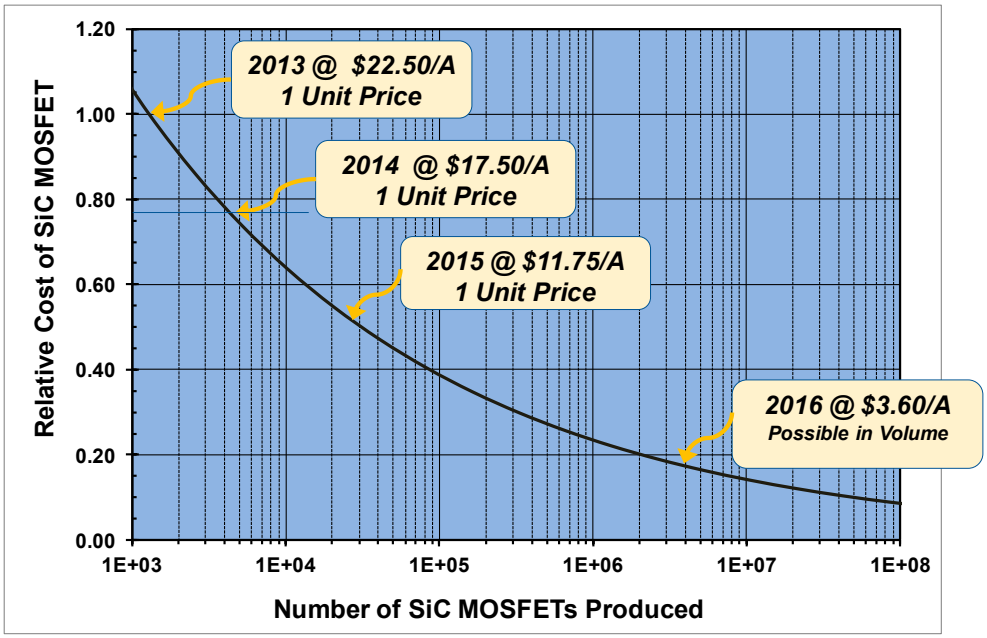


Fig. 1-3. Projected cost trend of 3.3 kV SiC MOSFETs in 2014 [4].

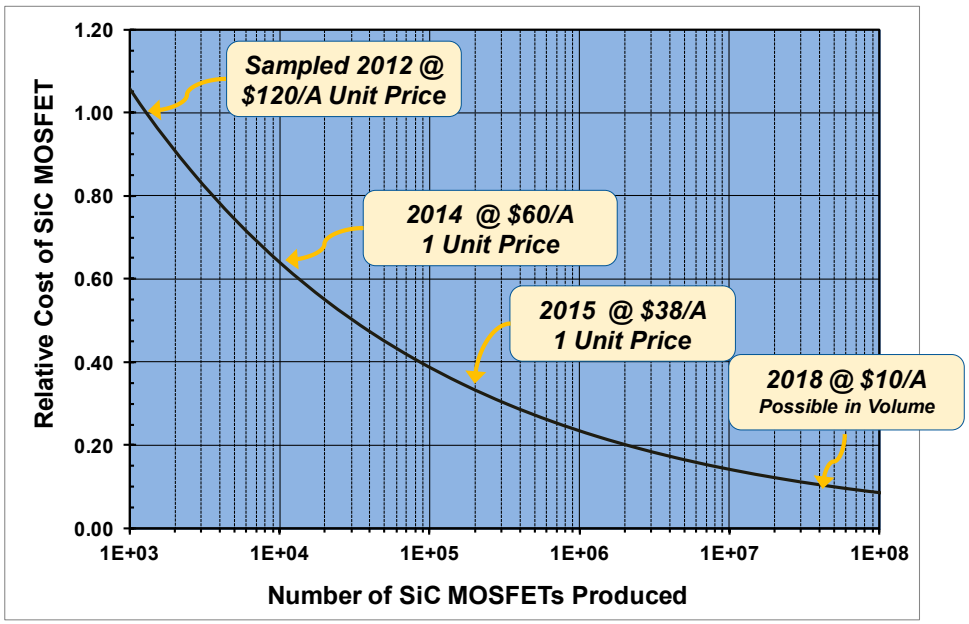


Fig. 1-4. Projected cost trend of 10 kV SiC MOSFETs in 2014 [4].

Table 1-1. Comparison of commercially available Si-IGBTs and SiC MOSFETs from Digikey (2019Feb).

	Parts Number	Manufacturer	Voltage Rating	Current Rating	Power Dissipation	Price
SiC MOSFETs	SCH2080KEC	Rohm Semiconductor	1.2 kV	40 A	262 W	$ 37.7
	C3M0075120J	Wolfspeed	1.2 kV	30 A	113.6 W	$ 12.64
	SCT20N120	STMicroelectronics	1.2 kV	20 A	175 W	$ 15.73
Si IGBTs	IXYH20N120C3D1	IXYS	1.2 kV	36 A	230 W	$ 10.84
	STGWA15H120F2	STMicroelectronics	1.2 kV	30 A	259 W	$ 5.01
	IRG4PH40KDPBF	Infineon Technologies	1.2 kV	30 A	160 W	$ 6.68
	IRG4PH30KDPBF	Infineon Technologies	1.2 kV	20 A	100 W	$ 6.90
	FGA15N120ANTDTU-F109	ON Semiconductor	1.2 kV	20 A	186 W	$ 2.86

1.2 Power Density for Modern Power Electronics

The importance of power density is increasing in modern power electronics [5]. In information technology, the power consumption of servers, telecommunication applications, and data centers has rapidly increased, along with high computing power. On the other hand, the space for the building infrastructure is quite limited. High power per unit volume ($W/in^3, kW/dm^3$) is required for the power electronics to accommodate more power in the limited space. Also, in an effort to build eco-friendly transportation systems, Electric Vehicles (EV) or More Electric Aircrafts (MEA) have gained attention. In these applications, the total weight of the system is directly-related to *km* (*mile*) per charge since the capacity of the battery is limited. Therefore, a high value for the power per unit weight (kW/kg) is a critical design consideration for the power electronics. Also, less weight typically indicates less use of materials and allows for simpler installations, handling, and maintenance. Therefore, the power density has been used to indicate Figure of Merit (FOM) to evaluate the technical advancement of power electronics, similar to Moore's law (transistor density) for microelectronics [5].

A general design procedure for the power electronics design is shown in Fig. 1-5. The power density and efficiency of power electronics is determined by the result of this design procedure. At first, system specifications such as input voltage range, output power range, and standards for power quality and electromagnetic interference (EMI) are given, and a circuit topology can be chosen. With selected topology, a modulation scheme to decide a switching sequence and optimal candidates for power devices can be selected. Then, the design goes through an optimization procedure. In the optimization procedure, a switching frequency for the inverter is selected, and design of filters and a cooling system is done to meet design constraints such as total harmonic distortion (THD), standards for electromagnetic interference (EMI), operating temperature, etc. Next, a different switching frequency is chosen, and the same design steps are performed. By the iteration of this procedure, a Pareto front of power density and efficiency can be drawn, and a design point which gives a good balance between these two performance factors can be selected.

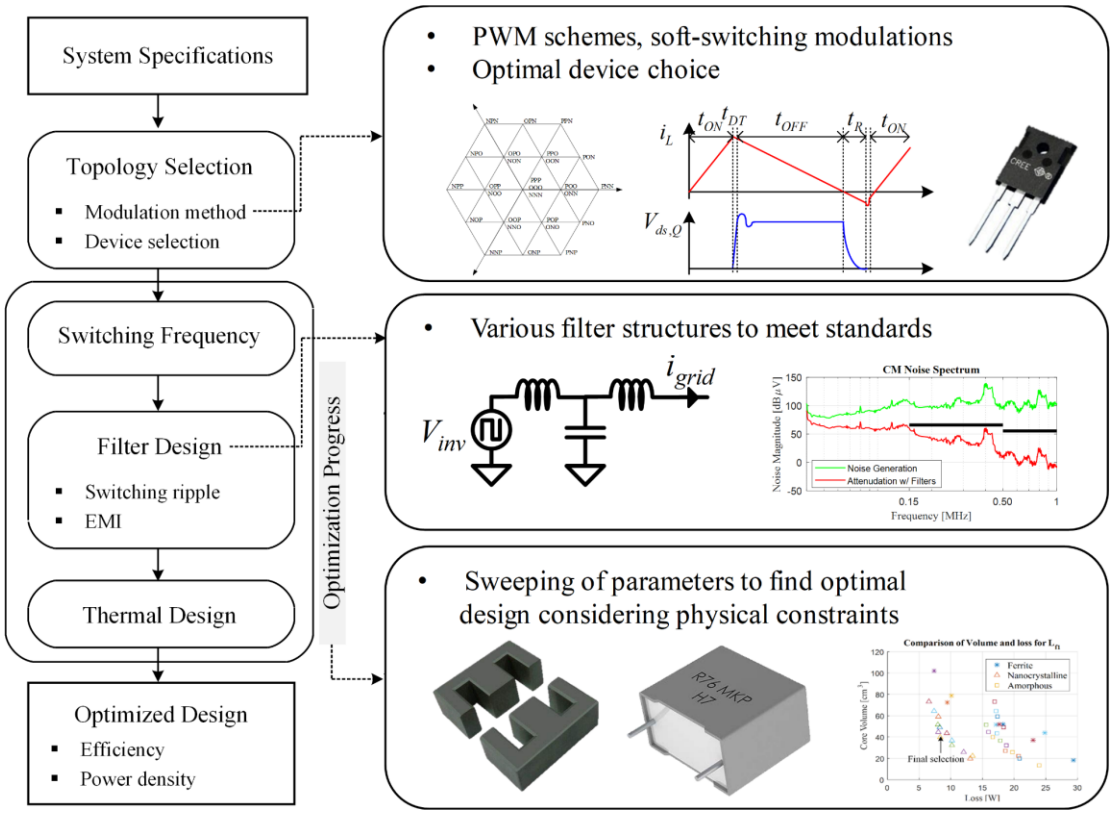


Fig. 1-5. Design procedure of three-phase inverter.

The weight and volume of each component are determined by this design procedure. The magnetic components and heatsinks (or cooling system), significantly contribute to the overall weight, volume, and therefore, the power density. To improve power density, there have been numerous approaches to reduce the size of magnetic components and the cooling system of converters.

Multi-level converters provide more voltage-level, thus smaller current ripple, compared to 2-level. In particular, 3-level topologies with Si-IGBTs are widely used in industrial drives and renewables applications. For PWM schemes, optimal PWM schemes have been investigated to minimize the current distortion. An interleaving technique turns a part of voltage harmonics

into circulating components, and the size of boost inductors can be reduced [6]–[10]. However, additional magnetic components such as common-mode chokes, or coupled inductors to suppress these circulating currents, contribute to a size increase [11]. This contribution of circulating currents blockers is more noticeable when the number of paralleled inverter increases; the size of the boost inductor can shrink quickly, and the number of common-mode chokes or coupled inductors increases [12]–[15].

When the switching-loss of IGBTs can be reduced, the switching frequency can be increased. This will decrease the size of the output filter, or a smaller heatsink can be used. Thus, the power density of the three-phase inverter can be improved. Different techniques have been investigated to reduce the switching-loss by modulation schemes. In discontinuous PWM (DPWM) schemes [16]–[18], one of the three-phase inverters is clamped to one switching state for a certain time period. For instance, the switching state can be clamped to either a positive dc-rail or negative dc-rail in the two-level inverter case. The switching loss can be reduced by one third, compared to the PWM schemes where all three-phases switch once within a switching period. With the same switching loss, the switching frequency can be increased by 50%. However, when the clamping direction changes, there exists a jump in zero-sequence voltage which provokes a pulse current if there is any capacitive load for zero-sequence components.

The switching energy of WBG devices is reported to be concentrated at the turn-on instant. Auxiliary circuits to achieve zero voltage switching (ZVS) turn-on or zero current switching (ZCS) turn-off were investigated which significantly reduce the switching loss of WBG devices [19]–[22]. However, additional passive components for high-frequency resonance

bring complexity in the design and modulation. Triangular Conduction Mode (TCM) modulation to eliminate the turn-on loss does not require additional circuitry to achieve ZVS. This scheme originated from dc-dc converters [23], single-phase applications [24]–[26], and extended to three-phase inverters [27]–[29]. However, the principle of TCM operation highly rely on the current slope and the impact of the three-phase coupling complicates the modeling and analysis. Also, the benefit on the hardware including the EMI filters has not been reported.

Higher-order filters, such as an LCL filter structure, can provide higher attenuation with a relatively smaller size, and became an industry standard for high power renewable systems [30]–[32]. Notch filters to eliminate a specific frequency component were studied [33]. However, there exists a number of resonant frequencies which requires a delicate, either passive- or active-damping scheme, to ensure stability [34]. Magnetic integration schemes were researched to integrate multiple magnetic components in high-order filters or interleaved ac-dc converters [14], [35], [36]. However, most of the integration schemes require a complex assembly or customized core which prohibits its practicability in terms of manufacturability and design. To reduce the size of the cooling system, an optimized design for a different heatsink was investigated, and the water-cooled system was used for high-power applications [37]–[39].

After 30 years of research, from Si die-level improvements to system-level optimized designs, the power density of Si-IGBT based converters seemed to be mature and had approached its limit.

1.3 Power Density with Silicon Carbide Devices and State-of-the-Art Design Examples

SiC and other WBG devices are expected to be game-changers in the power electronics field. With their lower switching-loss characteristics, the switching frequency of these converters is expected to be much higher so the size and weight of the inductors will be drastically reduced. Also, their higher temperature operation above 150°C would demand less need for cooling. Therefore, a drastic increase in power density seems to be attainable. Thirteen years ago in 2006, [5] and [40] showed a road map for power density until 2020. This was based on trends in the last few decades, as shown in Fig. 1-6. With the emergence of WBG devices, the power density of power electronics was expected to reach over 30 kW/dm^3 in 2020. The power densities of current state-of-the-art design examples found in the literature between 2016 – 2018 [3], [41]–[49] are labeled in the same figure. Only three-phase power converters are included in the graph. Most of the designs show around 4 kW/dm^3, and the highest value is around 17 kW/dm^3 [45], which is an example of a water-cooled traction inverter for a motor-drive without any filter components. Even with the emergence of WBG devices, the power density has not had a drastic increase thus far. The improvement of power density is in keeping with its trends since 1994, where the power density has doubled every 10 years.

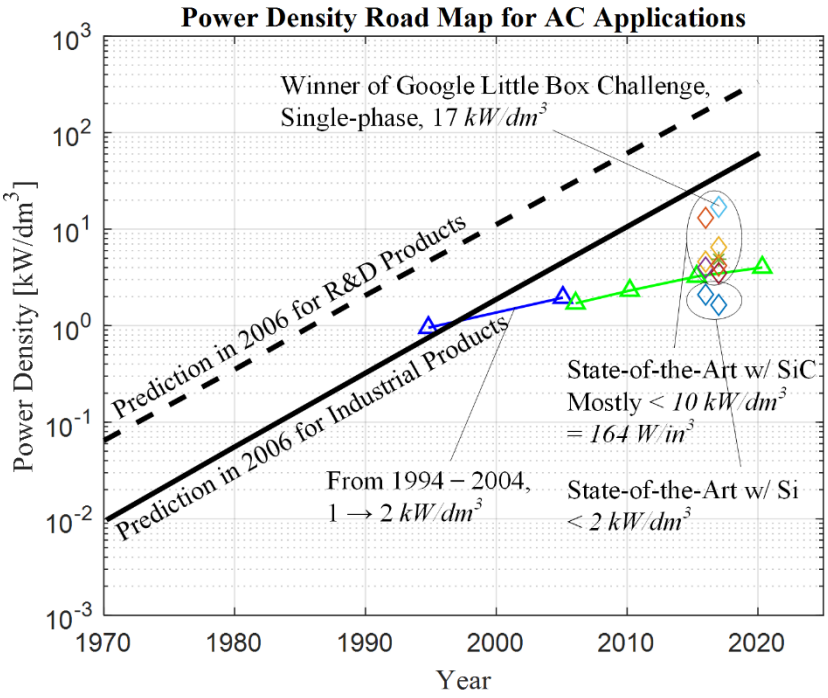


Fig. 1-6. Trends in the power density for three-phase converters since 1970s.

1.4 Limitations for Achieving Higher Power Density

In this section, the key factors that limit the improvement of power density for SiC devices are identified.

1.4.1 Electromagnetic interference

The fast switching of SiC devices can reach over 50 V/ns. In the circuits, multiple parasitic capacitors exist, such as the one between an output of the phase legs to the heatsinks. During the switching instant, large charging currents for these capacitors may flow by the high dv/dt

of SiC MOSFETs, generating high-frequency noise. Also, the increased switching frequency of SiC MOSFETs increases common-mode (CM) noise on the high frequency range.

Generally, the EMI standard such as FCC15, MIL-STD-461, and IEC62040-2 strictly limits the output CM noise of the converters to prevent pollution to the other subsystems. Furthermore, this noise may interfere with the auxiliary circuits, such as the gate drivers, sensors, and protection circuits, and cause malfunctioning.

Passive filters, such as CM chokes, are generally utilized to attenuate CM noise that is located around low frequency (30 ~ 300 kHz), or medium frequency range (0.3 ~ 3 MHz). In general, the value of CM capacitors is limited due to ground current. With the fast switching of SiC devices, the CM EMI filter has to provide more attenuation on this frequency range, and the size of the CM choke becomes much larger than a Si-based converter. In [50], a comparison between CM chokes for a 200 kHz SiC inverter and a 20 kHz Si inverter was performed. The results showed that the size of the CM choke had to be increased by 23 times. In [3], the distribution of the volume is compared between an optimized 5 kW Si-IGBT inverter and a SiC-MOSFET inverter. The portion of volume for EMI filters, over the whole converter volume, drastically increased from 3% to 20% to meet the same EMI standard. This increase in the size of EMI filters will deteriorate possible improvement on the power density by SiC-based power converters.

1.4.2 The limited increase in switching frequency

A survey on the switching frequency has been performed on state-of-the-art SiC-based converters for three-phase ac-dc or ac-ac applications [3], [41]–[49], [51]. The result is shown

in Fig. 1-7. The switching frequency of the design examples with hard-switching remains within 70 kHz, except for the work in [51], which achieves 300 kHz switching frequency with ZVS modulation. The first reason is that the efficiency constraints put a limit on the increase in switching frequency. Most of the literature achieve near or above 98% efficiency, and switching frequency is limited below 70 kHz. Higher switching frequency will result in high switching-loss in devices and larger core-loss in inductors, deteriorating overall efficiency. Secondly, EMI standards put a limit on the selection of switching frequency range. As it was investigated in Section 1.4.1, the size of the EMI filter takes a considerable portion of the volume of SiC converters. With PWM voltage waveform, large harmonics are located at the multiples of switching frequencies. A required attenuation from the EMI filter is mainly determined by the lowest multiple of the switching frequency, which comes into the frequency range of EMI standards. For example, when the EMI regulation starts at 150 kHz, increasing the switching frequency from 70 kHz to 80 kHz may give an increase in the total filter size. This is because the lowest multiple of switching frequency will be located at 210 kHz for the 70 kHz case and 160 kHz for the 80 kHz case. Therefore, an increase in switching frequency will be limited to below 70 kHz range if the switching frequency cannot go far beyond 150 kHz, such as the ZVS modulation cases in [22], [51], [52].

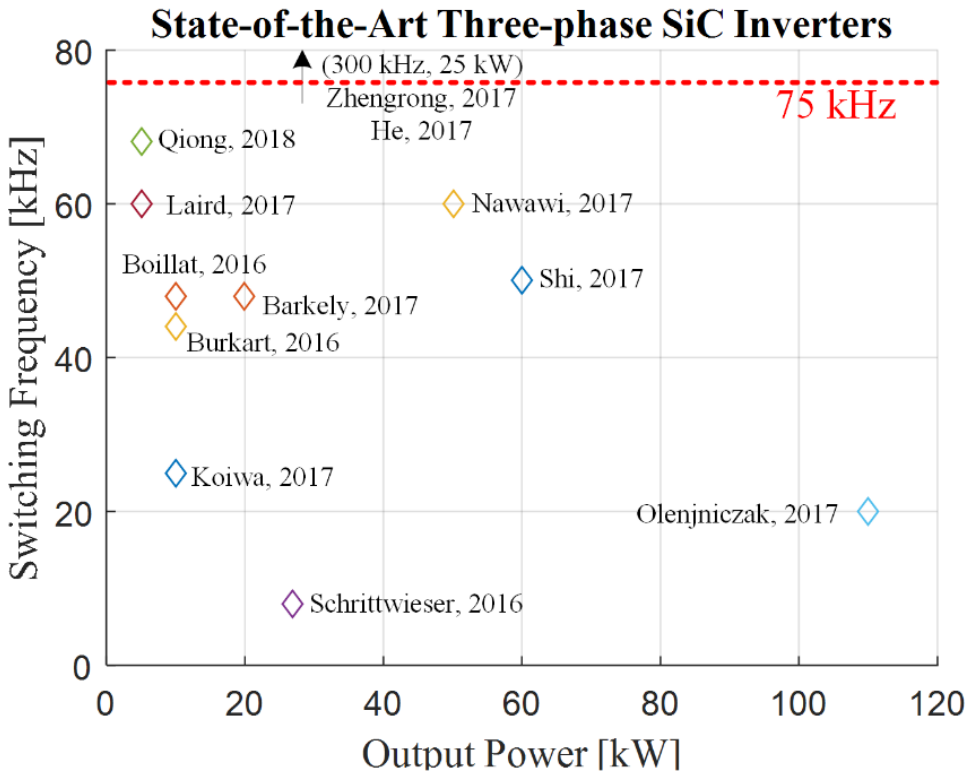


Fig. 1-7. Power rating vs. switching frequency plot for state-of-the-art three-phase SiC converters.

1.4.3 Magnetic components for switching ripple attenuation

The volume and weight of the magnetic component take a huge portion of Si-IGBT converters. The main expectation with WBG devices was that very high switching frequency would be easily achievable. This would make the size of the magnetic components minimal, compared to conventional Si-IGBT based designs. However, with the limited increase in the switching frequency, as mentioned in Section 1.4.2, the size reduction of magnetic components by increasing the switching frequency, is deemed to be limited.

In [3], the design example of an optimized 6 kHz switching Si-IGBT inverter and a 63 kHz switching SiC MOSFET is compared. The contribution of magnetic components for the

filtering of switching frequency ripple is summarized in Fig. 1-8. With 10 times higher switching frequency, the power density of the converter could be increased by 160%. However, the contribution of filter inductors on the total volume is still high. In the volume optimized design, the filter inductors for switching-ripple takes 47% in the SiC-based inverter, and 75% in the Si-based inverter. In the weight design, the filter inductor still takes 65% of the total weight in the SiC design while it takes 79% of the Si-IGBT design. The magnetic components remain the most critical components for power density.

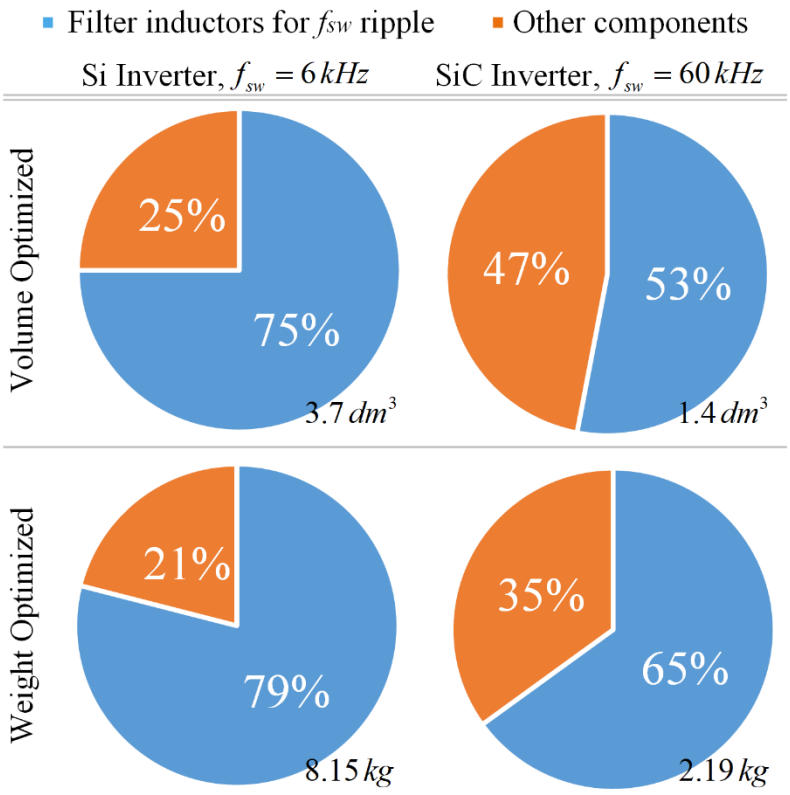


Fig. 1-8. An example of contribution of magnetic components on the total weight and volume in the optimized Si-IGBT and SiC MOSFET based three-phase inverter [3].

1.5 The Scope and Objectives of the Dissertation

Throughout this dissertation, techniques and schemes to break the limitations imposed by the three key factors were investigated. The scope of the research is limited to grid-connected SiC-based converters where the output or input of the converter is connected to the three-phase ac-grid. The power level range is from a few kW to tens of kW, and dc-link voltage ranges from 750 ~ 900V, where the devices with 1.2 kV or 1.7 kV, voltage-rating are used.

Key components are identified for each circuit configuration, and techniques to aim their size-reduction are proposed. For EMI filters, the dissertation focus is on passive filters. Active EMI filters are not considered which may not be easily implemented at this voltage and power level. The focus on EMI was on CM components since the CM parts were regarded to more significantly impact the filter size with the increased switching frequency.

Most of the present work focuses on reducing the specific passive component size, assuming the switching frequency is fixed. A magnetic integration method, using widely-used core shapes, is presented for switching-ripple filters. Modeling to interpret an interaction of common-mode noise, between an ac-ac stage and dc-dc stage connected to energy storage, is investigated to reduce and optimize the size of the passive EMI filter. A PWM scheme which can reduce the size of both the CM EMI filter and dc-link capacitors is proposed for the full-SiC three-level three-phase back-to-back converter. One chapter is dedicated to quantifying a benefit on power density by a soft-switching modulation scheme for three-level three-phase inverters, which may be able to significantly increase the switching frequency, thus power density.

1.6 Dissertation Outline

The outline of this dissertation is as follows, and it is summarized in Fig. 1-9. Firstly, a magnetic integration method is proposed for the interleaved inverters. In [11], [13], [35], [36], it is shown that the total size of magnetic cores and usage of winding material can be reduced by 20% through the integration of multiple magnetic components for a flux-limited design. Without increasing the switching frequency, the power density of paralleled SiC-converters can be improved.

The third, fourth, and fifth chapters are dedicated to power density improvement of the three-phase full-SiC uninterruptible power supply (UPS). In the third chapter, to minimize the size, EMI filters, modeling, and an EMI mitigation strategy are investigated. If the EMI problem is addressed during the design-phase before prototyping, the costs and efforts on EMI remedies can be reduced. For EMI planning, a simplified frequency-domain model can be used to predict and compare the effectiveness of EMI remedies, such as the topologies, PWM schemes, and filter structures. UPS has various modes of operation and the noise mechanism is distinct, depending on the modes of operation. This calls for a deliberate strategy to be set before prototyping. A common-mode equivalent model for the UPS is proposed which highlights the impact of the dc-dc stage and large parasitics of the battery-rack. Based on the model, different topologies and PWM schemes are compared to find a combination with minimal CM noise emission.

A PWM scheme is proposed for the ac-ac stage of a 3-level full-SiC UPS. The 3-level topology requires large DC-link capacitors to handle low-frequency ripple of neutral point voltage. Also, the size of the CM EMI filter increases with a high switching frequency of SiC

devices. The proposed PWM scheme reduces output CM EMI and compensates for low-frequency ripple of neutral point voltage, both on DM voltage and CM voltage on the output. Two key components affecting the power density of the three-level full-SiC converter can be significantly reduced by the proposed PWM scheme.

Fourthly, to demonstrate the increase in the power density by the proposed methods in Chapter 3 and Chapter 4, and the benefit of a SiC device on the power density, the optimization and prototyping of a 20 kW full-SiC UPS are constructed. A detailed design process is discussed. The power density of the prototype is compared with the state-of-the-art UPS with similar topology.

Fifthly, a design with a new modulation scheme is discussed. A Triangular Current Mode (TCM) modulation for a 3-level converter is investigated. With TCM modulation, zero-voltage turn-on can be achieved for all 12 SiC MOSFETs in three phase legs. Since the switching-loss of WBG devices is concentrated in the turn-on instant, the switching loss can be significantly reduced. Therefore, the switching frequency of the converter can be increased much higher than the frequency where the EMI regulation starts, and the size of the EMI filters and passive components can be drastically minimized. A design guideline is presented and a comparison is performed with the CCM case.

Lastly, the conclusion of the work is presented, with a summary of action taken and the direction for future work.

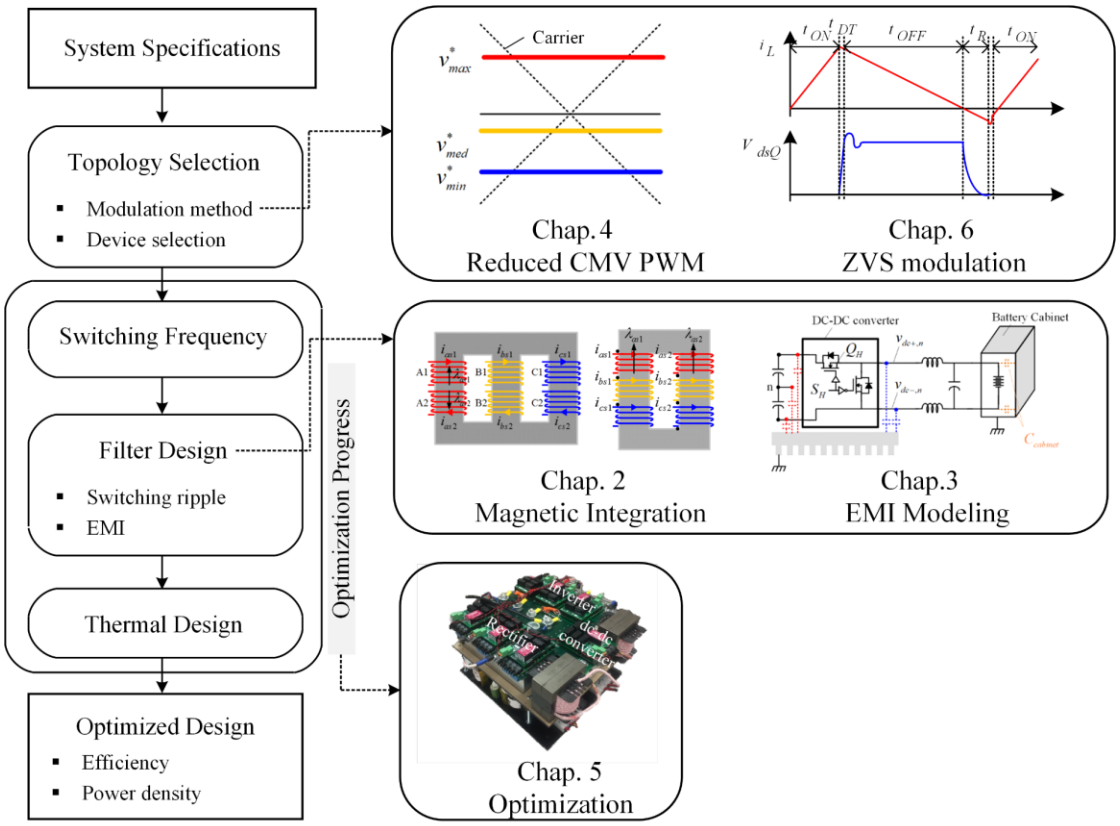


Fig. 1-9. Chapters of the dissertation with the design procedure.

Chapter 2. Differential-Mode and Common-Mode Coupled Inductors for Parallel Three-phase AC-DC Converters

2.1 Chapter Introduction

Compared to the-state-of-the-art Si-IGBTs, the current ratings of SiC devices are limited. To further increase the power capacity of the SiC-based converter, a three-phase converter can operate in parallel and interleaving technique can be used. When several PWM converters are interleaved, the carrier of each converter can be phase-shifted resulting in a certain portion of the harmonics being canceled at the output. As a result, the filter inductors for each converter can be reduced while meeting the total harmonic distortion (THD) requirements at the output [8], [53]. As magnetic components take a large portion for weight and size of power conversion systems [5], interleaving can contribute to a reduction of the size and weight of a power conversion system. In high power applications where magnetic components account for a considerable proportion of the weight of the whole system [31], [54], [55], or in more electric aircraft (MEA) where weight and size reduction are key requirements for power converters [8], [56], [57] the total weight and size and power conversion unit can significantly be reduced with smaller magnetics.

On the other hand, if the interleaved converters share a common AC output and DC-link, circulating current flows between the converters. The circulating current contributes to an additional loss at power devices and filters, deteriorating the efficiency of the system. According to the phase-difference between three-phases, this circulating current can be divided

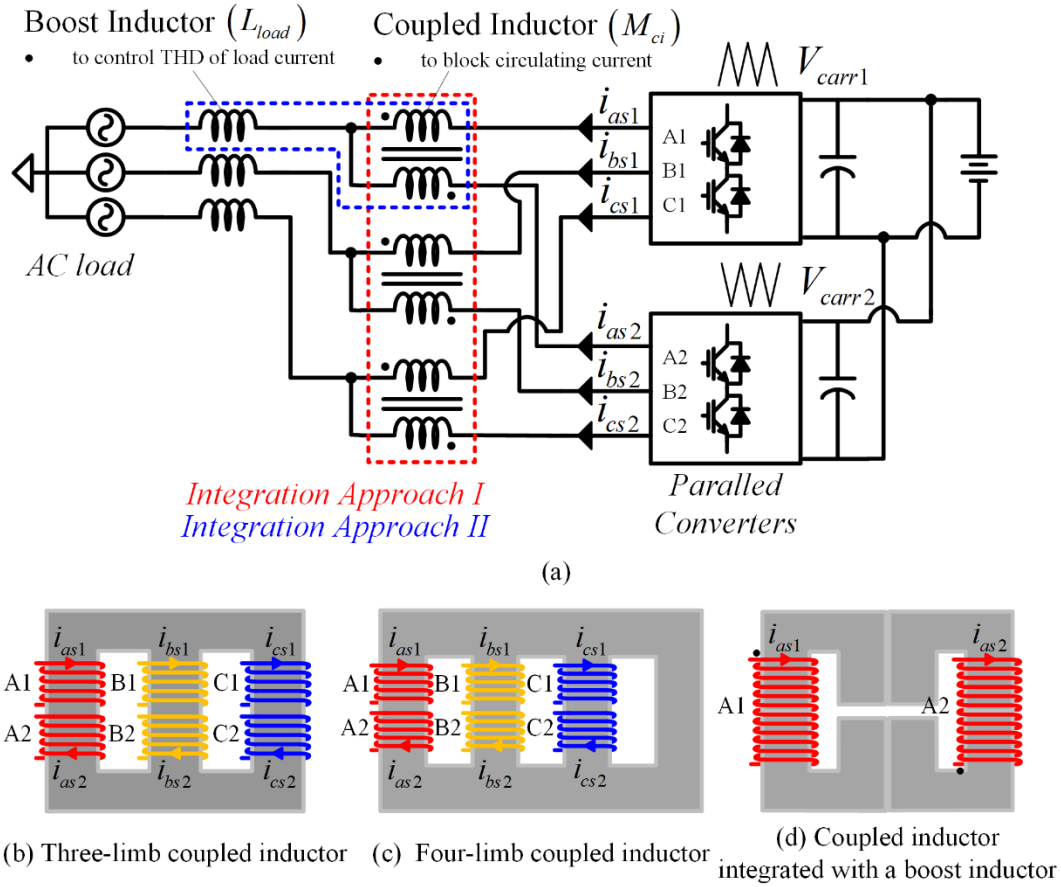


Fig. 2-1. (a) Approaches for magnetic integration in interleaved three-phase converter, (b) Three limb coupled inductor, (c) Four limb coupled inductor, and (d) Coupled inductor integrated with boost inductors.

into differential-mode (DM) components and common-mode (CM) components [8], [54], while the CM circulating current takes the major portion in terms of magnitude [58]. Common-mode chokes or coupled inductors (CIs) can be implemented to suppress CM circulating current. These additional magnetic components increase the size and weight of the overall system and mitigate the benefits of interleaving on the size and weight reduction. In [8], the weight of the coupled inductors was 50% of the total magnetic weight. In [11], the major portion $(>60\%)$ of the total magnetic weight in a motor drive system came from the three coupled inductors on AC-side.

To reduce the size and weight of interleaved converters, researches have been done to integrate magnetic components of three-phase paralleled converters [11], [36], [55], [59]–[62] as shown in Fig. 2-1(a). By the magnetic integration, both total volumes of the magnetic core and copper usage can be reduced which may result in a significant decrease in the system weight and volume.

Researches in [55], [59]–[61] focus on the integration of 3 CIs for three-phases, while the inductance of the load is utilized as the output inductor. Three CIs are integrated into single EI-core as Fig. 2-1(b) for two three-phase converters. This structure can effectively provide an impedance for DM circulating harmonics. However, there is no path inside of the EI-core for the flux by CM current, and the integrated coupled inductor provides only small impedance. Therefore, different schemes are used to eliminate CM circulating current [55], [59]–[61]. In [59], a modified DPWM method is proposed by which the difference between the CM output voltage of two converters is kept at zero. However, the effective switching frequency is doubled for the two phases compared to the conventional DPWM for the same carrier frequency. The same structure has been used for high power motor drive system [55] and STATCOM [60]. In [55], [60], DC-links of paralleled converters are separated, eliminating the path for CM circulating current. However, the number of DC-side components, like capacitors, must be doubled for two paralleled converters, increasing the cost and volume of the system. Furthermore, interleaving loses its benefit on the DC-side. In [61], one more limb is added to EI core as shown in Fig. 2-1(b). The 4^{th} limb provides a path for the flux of CM circulating current. However, it is very difficult to achieve symmetry in a magnetic path between 4 limbs. Also, such a structure is not easy to build from the core shapes which are widely used. The magnetic core may need customization or I-cores would have to be assembled to build such

structures. It is disadvantageous in terms of cost and manufacturability and assembly of I-cores may create inevitable air gaps between the blocks.

Other approaches in [11], [36], [62] integrate the boost inductor with the CI to further reduce magnetic cores material and copper material. In [62], customized U-core is used to integrate single CI and two single-phase boost inductors as shown in Fig. 2-1(d). In [11], the leakage inductance of the CIs is implemented as the boost inductor. In [36], two I-cores are attached on the side of the structure in [61] to integrate two three-phase boost inductors with the 4-limb CIs. However, in these approaches, the CIs and the boost inductor share a magnetic path, and the flux by circulating current must be added on the flux of output current. Since the flux by output current is already relatively large, a dedicated PWM scheme is implemented to reduce the flux by CM circulating current [36], [62] or a material with high saturation magnetic flux density is used [11].

This chapter proposes an integration method of the CIs for three-phase converters. According to DM and CM, and phase-shift by 180°, every harmonic on the frequency spectrum is classified into 4 different groups. Based on this systematical classification, a new integrated structure for CIs has been proposed. In the proposed structure, one core suppresses DM circulating current while the other suppresses CM circulating current. By making a series-connection of these two inductors, the same level of suppression can be provided to both DM and CM circulating current. The proposed inductors can be easily implemented with standard-shape magnetic cores. Furthermore, by separating the flux by DM and CM circulating current, the peak flux density of DM and CM coupled inductor can be reduced. If the size of the core is determined by peak flux density, the proposed integration can give a significant decrease in

the size and weight of the CIs. Furthering [35], the impact of the modulation index (MI) and PWM scheme on maximum volt-seconds is investigated for the proposed CIs. Analytic solutions of volt-seconds for SVPWM and DPWM60° are derived. The result shows that the maximum voltage-seconds on the proposed structure can be reduced by 33% for a wide MI range. The validity of proposed integration and size reduction are verified by both simulation and experiments with 1 kW interleaved converters

2.2 Classification of Sideband Harmonics with 180° Interleaving

2.2.1 Differential-mode and common-mode sideband harmonics

According to the analytic solution of pulse-width modulation (PWM) voltage with carrier-based modulation [63], the output voltage of the PWM converter can be divided into CM and DM components on the frequency spectrum [9]. Analytically, the CM harmonics exist in sideband harmonics at frequencies of $mf_{sw}+3nf_0$ where m is carrier index variable and $3n$ is baseband index variable. The sideband harmonics at the other frequencies can be classified as DM components. These voltages induce DM and CM currents according to the impedance for DM and CM components in the circuit. in Mathematically, DM components $\left(i_{dm,xs}\right)$ and CM component $\left(i_{cm}\right)$ in phase-*x* of converter current can be extracted as (2.1) in time domain where i_{as}, i_{bs}, i_{cs} are phase-A, B, C converter current, respectively.

$$\begin{aligned} i_{cm} &= \frac{i_{as}+i_{bs}+i_{cs}}{3} \\ i_{dm,xs} &= i_{xs}-i_{cm},\ x=a,b,c \end{aligned} \tag{2.1}$$

Based on the phase relationship among the three phases, the equation (2.2) holds for DM current due to phase relation among phase A, B, and C.

$$i_{dm,as} + i_{dm,bs} + i_{dm,cs} = 0 \tag{2.2}$$

The structure of conventional three-phase inductors like Fig. 2-2(a) utilizes the characteristic of differential-mode as (2.2). The DM flux passes across the legs, enabling three single-phase inductors to be integrated into a single EI-core. The structure of conventional CM choke for three-phase application in Fig. 2-2(b) utilizes the characteristic of CM current. With the structure as Fig. 2-2(b), the flux by DM current is canceled in the core, while the flux by CM current can be tightly coupled. With relatively small size, the CM choke provides large impedance only to CM current.

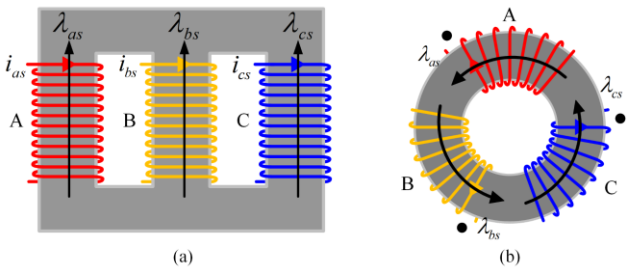


Fig. 2-2. Structure of (a) three-phase inductor, and (b) common-mode choke.

2.2.2 Phase-shift of sideband harmonics by 180° interleaving

Interleaving affects the phase-difference between the current of paralleled converters. The typical circuit diagram for two interleaved converters is shown in Fig. 2-4. With 180° interleaving, the phase of sideband harmonics at $(2m-1)f_{sw}$ is shifted by 180° and these

harmonic currents are canceled out at the output where $m = 1, 2, 3...$. These harmonics are called 'circulating' since they only flow among the paralleled converters. 180° interleaving does not affect the phase of the fundamental current at f_0 and sideband harmonics at $2mf_{sw}$ and the current in these frequencies become load current. Mathematically, load components $\left(i_{load,xs}\right)$ and circulating components $\left(i_{cir,xs}\right)$ in phase-x of converter current can be extracted as (2.3) on time domain. Phase-x current of converter 1 and 2 are labeled as i_{xs1} and i_{xs2}, respectively. Example waveforms of phase-A converter current $\left(i_{as1}\right)$, load current $\left(i_{load,as1}\right)$, and circulating current $\left(i_{cir,as1}\right)$ for a two-level three-phase converter with DPWM60° are shown in Fig. 2-3.

$$\begin{aligned} i_{cir,xs1} &= \frac{1}{2}\left(i_{xs1} - i_{xs2}\right) \quad x = a,b,c \\ i_{load,xs1} &= \frac{1}{2}\left(i_{xs1} + i_{xs2}\right) \quad x = a,b,c \end{aligned} \tag{2.3}$$

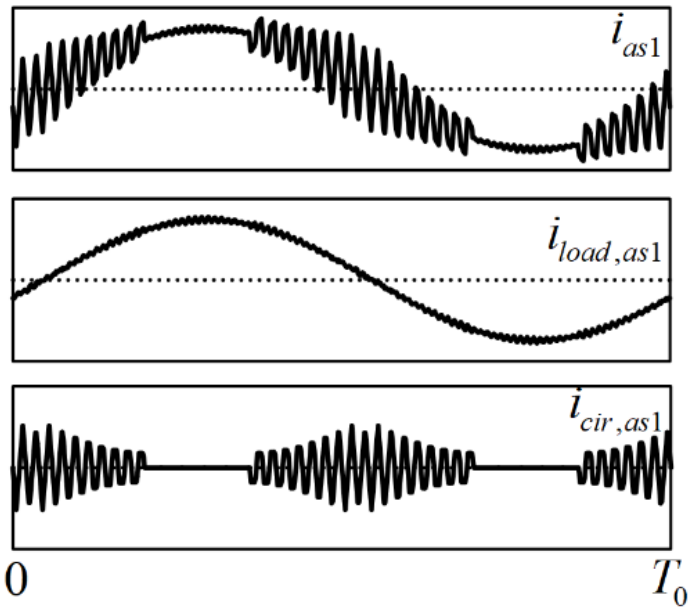


Fig. 2-3. Example waveforms of phase-A converter current $\left(i_{as1}\right)$, load current $\left(i_{load,as1}\right)$, and circulating current $\left(i_{cir,as1}\right)$ for two-level three-phase inverter with DPWM60°.

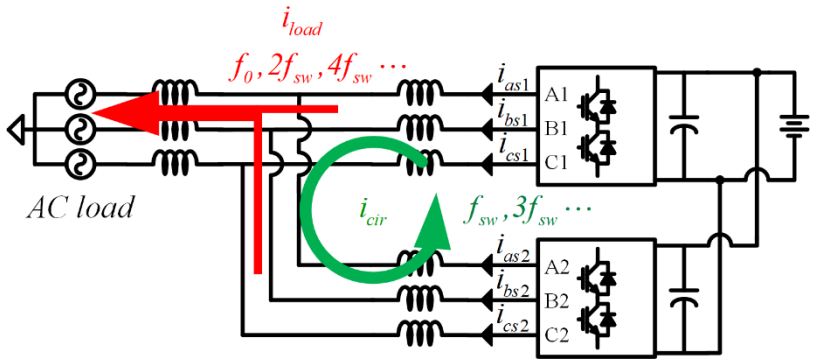


Fig. 2-4. Path of circulating current and load current.

Assuming that two converters are symmetric in every sense, the equation (2.4) holds for the circulating current at $\left(2m-1\right)f_{sw}$ frequencies while (2.5) holds for load current at $2mf_{sw}$.

$$i_{cir,xs1}+i_{cir,xs2}=0, \quad x=a,b,c \tag{2.4}$$

$$i_{load,xs1} = i_{load,xs2}, \qquad x = a,b,c \tag{2.5}$$

These switching frequency circulating harmonics must be attenuated with additional passive filters like coupled inductors. The conventional coupled inductors (CIs) for three-phase converters are shown in Fig. 2-5. The flux by load components as (2.5) cancels in the core and the CI only provides a small inductance of L_{lk}. The flux by circulating components (2.4) is coupled inside of the core and the CIs provide a large impedance of $L_{lk} + 2M_{ci}$ where M_{ci} is the mutual inductance of the CI. In summary, flux by these two components can be written as (2.6) for the winding connected to phase-x of converter 1.

$$\lambda_{xs1} = \left(L_{lk} + M_{ci}\right) i_{xs1} - M_{ci} i_{xs2} = \begin{cases} \left(L_{lk} + 2M_{ci}\right) i_{cir,xs1} & \textit{for circulating component} \\ L_{lk} i_{load,xs1} & \textit{for load component} \end{cases} \tag{2.6}$$

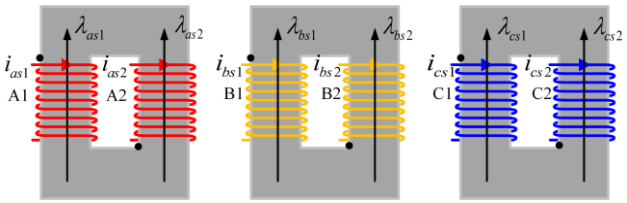


Fig. 2-5. Structure of three separate coupled inductors for three phases.

2.2.3 Summary

Combining DM, CM and phase-shift between two converters, any current in a whole frequency range can be divided into 4 groups as Table 2-1. On converter current of Fig. 2-1, the sum of these 4 groups flows. As an example, phase-A current of converter 1 $\left(i_{as1}\right)$ can be

written as (2.7). The load current $\left(i_{load,as1}\right)$ is the sum of DM component $\left(i_{load,dm,as1}\right)$ at 60 Hz and on $2mf_{sw}$ sidebands, and also CM component $\left(i_{load,cm}\right)$ on $2mf_{sw}$ sidebands. The circulating current on $\left(2m-1\right)f_{sw}$ can also be classified into DM component $\left(i_{cir,dm,as1}\right)$and CM component $\left(i_{cir,cm}\right)$. The direction of current flow is shown in Fig. 2-6 for each group.

$$i_{as1}=i_{load,as1}+i_{cir,as1}=\left(i_{load,dm,as1}+i_{load,cm}\right)+\left(i_{cir,dm,as1}+i_{cir,cm}\right) \tag{2.7}$$

Table 2-1. Classification of converter current harmonics with 180° interleaving.

Between Converters \ Among 3-phases	Differential-mode $i_{dm,as}+i_{dm,bs}+i_{dm,cs}=0$	Common-mode i_{cm}
Load (In-phase) $i_{load,xs1}=i_{load,xs2}$	Group 1: $i_{load,dm}$ Fundamental term at f_0, DM harmonics at $2mf_{sw}$	Group 2: $i_{load,cm}$ CM harmonics at $2mf_{sw}$
Circulating (Out-of-phase) $i_{cir,xs1}+i_{cir,xs2}=0$	Group 3: $i_{cir,dm}$ DM harmonics at $(2m-1)f_{sw}$	Group 4: $i_{cir,cm}$ Low-frequency CM harmonics, CM harmonics at $(2m-1)f_{sw}$

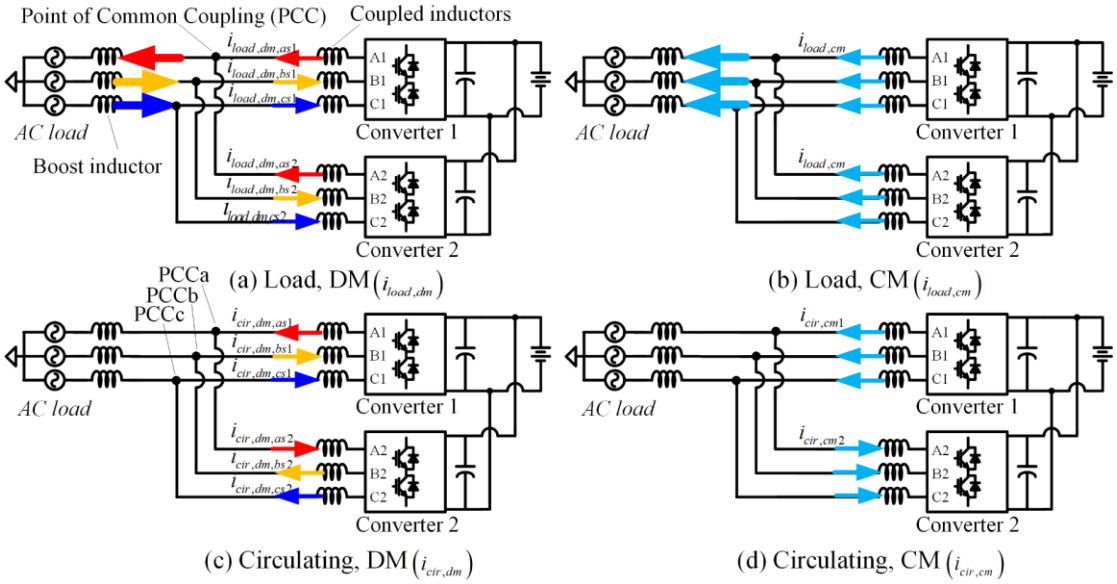


Fig. 2-6. Direction of current flow: (a) Group 1 $(i_{load,dm})$, (b) Group 2 $(i_{load,cm})$, (c) Group 3 $(i_{cir,dm})$, and (d) Group 4 $(i_{cir,cm})$.

With interleaving, the circulating components do not contribute to the load current and the THD of the current after a point of common coupling (PCC) can be low. The CM circulating components in group 4 mainly contribute to a large circulating current [7]. Low frequency circulating components can be eliminated by a controller within control bandwidth [64], [65]. For switching frequency range, either CIs or CM chokes can be used to suppress the CM circulating current in group 4 [1]. The CIs attenuate current of group 3 and 4 and CM choke attenuates the current of group 2 and 4. One observation is that the CM choke does not utilize any characteristic of interleaved converters, while the coupled inductors do not exploit any characteristics of DM and CM, thus leaving a room for improvement.

2.3 Proposed Structure for DM and CM Coupled Inductor

Based on the classification in Section 2.2, a new integrated structure for coupled inductors is proposed. The proposed coupled inductors are comprised of two magnetic cores. One is for a DM coupled inductor (DMCI) to suppress DM circulating harmonics of group 3. The other is a CM coupled inductor (CMCI) to suppress CM circulating harmonics of group 4.

The structure of the DMCI is shown in Fig. 2-7. The letter and number next to the windings indicate to which terminal the winding is connected. For example, the A1 winding is connected to the phase-A output of converter 1. PCCa, PCCb, and PCCc indicate the nodes for point of common-coupling for three-phases. By combining the structure of a conventional three-phase inductor with the coupled inductors, a single E-core with 6 windings can be implemented to suppress DM circulating current. A dot convention for the A1 winding is shown to illustrate how the flux will be coupled.

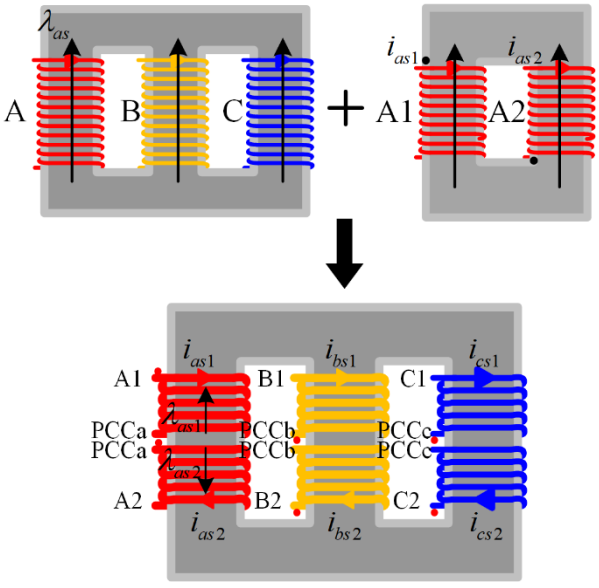


Fig. 2-7. DM coupled inductor.

The equivalent magnetic circuit for the DMCI can be drawn as Fig. 2-8 when the leakage inductance $\left(L_{lk}\right)$ is ignored. $\Re_{leg}$ and $\Re_t$ indicate reluctance of a limb and a transversal part of the magnetic core, respectively. Assuming $\Re_{leg} >> \Re_t$, the mutual inductance of single winding can be written as (2.8) where M_{dm} is coupled inductance and N_{dmci} is turns-number of a single winding. A_{dmci} and l_{dmci} are an effective cross-sectional area and a mean magnetic path length of a single leg, respectively. If we assume that the magnetic path is fully symmetric and leakage inductance is ignored, the flux of winding A1 can be written as (2.9).

$$M_{dm} \approx \frac{N_{dmci}^2}{\frac{3}{2}\Re_{leg}} = \frac{\mu N_{dmci}^2 A_{dmci}}{\frac{3}{2} l_{dmci}} \tag{2.8}$$

$$\lambda_{as1} = M_{dm}\left(i_{as1} - \frac{1}{2}i_{bs1} - \frac{1}{2}i_{cs1}\right) - M_{dm}\left(i_{as2} - \frac{1}{2}i_{bs2} - \frac{1}{2}i_{cs2}\right) \tag{2.9}$$

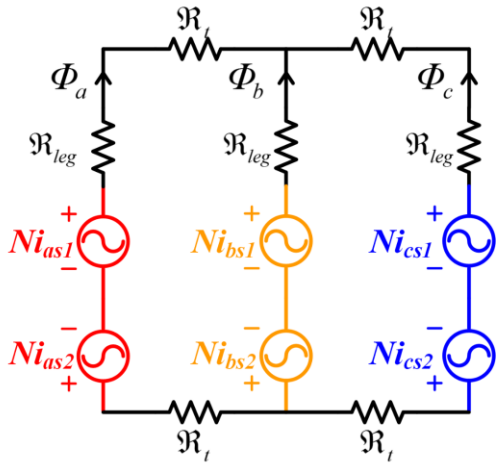


Fig. 2-8. Equivalent magnetic circuit for DM coupled inductor.

For fundamental current and DM harmonics of group 1, the fluxes are canceled in each leg by two windings with a different direction and the size of the core can remain small. For CM currents, no path exists inside the core. Therefore, the flux inside of the core is only generated by circulating DM harmonics of group 3. The effective inductance can be calculated as (2.10) by substituting (2.4), (2.2) into (2.9) and represented with the circuits for 4 groups in Fig. 2-9. As mentioned in Section 2.1, the same structure has been proposed in [55], [59]–[61]. Different schemes have been used to suppress CM circulating current which cannot be attenuated with the structure of the DMCI.

$$\lambda_{as1} = \begin{cases} 3M_{dm} i_{cir,dm,as1} & for\ DM, circulating \\ 0 & for\ the\ other\ groups \end{cases} \tag{2.10}$$

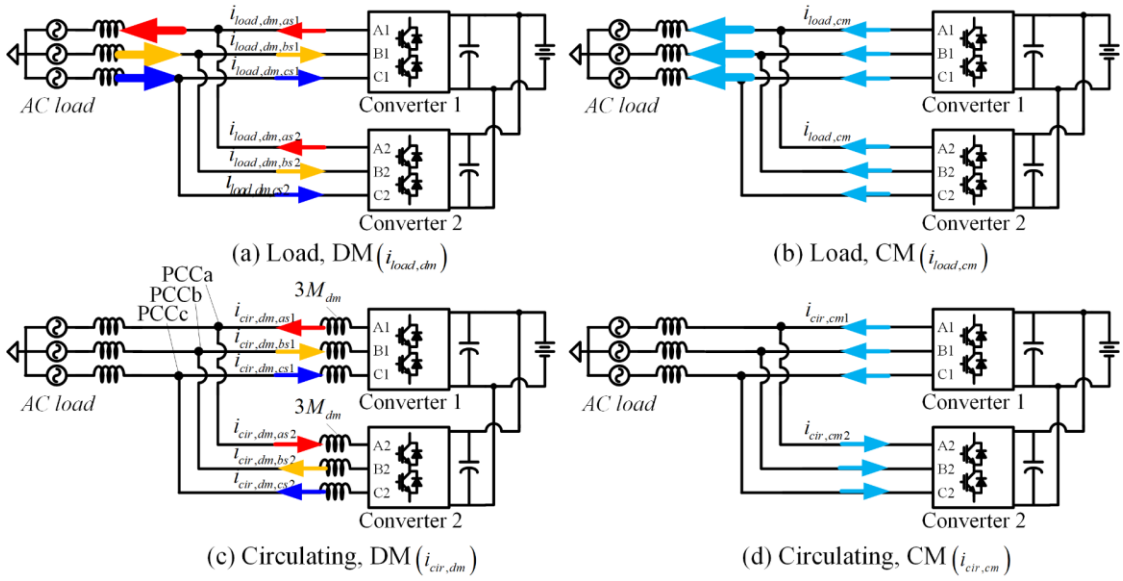


Fig. 2-9. Effective inductances of DMCI for 4 groups of currents.

The structure of the CM coupled inductor (CMCI) is shown in Fig. 2-10. By combining the structure of the CM choke with the coupled inductors, a U-core pair with 6 windings can

effectively couple the flux of CM circulating current. The U-core shape is one example. Further, the proposed CMCI can be implemented with other types of magnetic core like a toroid core with 6 windings, utilizing the same principle.

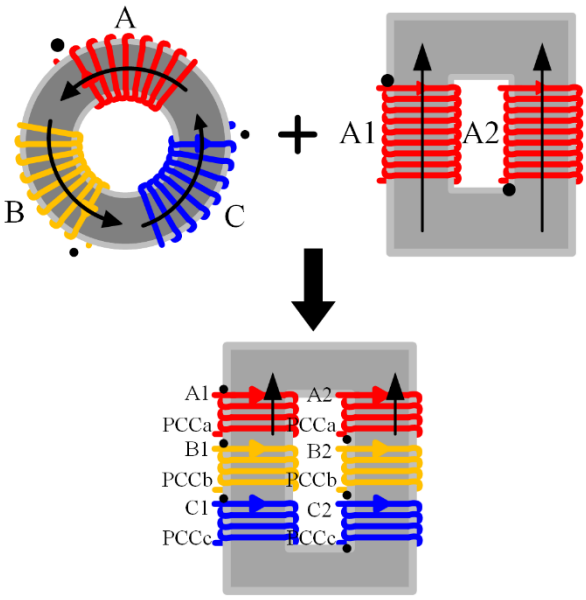


Fig. 2-10. Proposed CM coupled inductor.

The equivalent magnetic circuit for the CMCI is shown in Fig. 2-11. Assuming $\Re_{leg} >> \Re_t$, the mutual inductance of single winding can be written as (2.11) where M_{cm} is coupled inductance and N_{cmci} is turns-number of a single winding. The flux of winding A1 can be written as (2.12).

$$M_{cm} \approx \frac{N_{cmci}^2}{2\Re_{leg}} = \frac{\mu N_{cmci}^2 A_{cmci}}{2l_{cmci}} \tag{2.11}$$

$$\lambda_{as1} = M_{cm}\left(i_{as1} + i_{bs1} + i_{cs1}\right) - M_{cm}\left(i_{as2} + i_{bs2} + i_{cs2}\right) \tag{2.12}$$

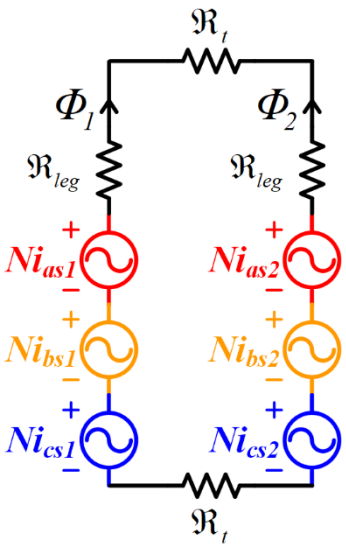


Fig. 2-11. Equivalent magnetic circuit for CM coupled inductor.

For DM components in groups 1 and 3, the fluxes are canceled out in each leg by phase-difference between three-phase as (2.2). For the CM load current of group 2, no flux is generated due to flux cancellation between the two limbs. Therefore, only the CM circulating currents of group 4 generate flux inside of the core. The effective inductance can be calculated as (2.13) by substituting (2.2) ~ (2.5) into (2.12) and represented with the circuits for 4 groups in Fig. 2-12.

$$\lambda_{as1} = \begin{cases} 6M_{cm} i_{cir,cm1} & for\ CM, circulating \\ 0 & for\ the\ other\ groups \end{cases} \tag{2.13}$$

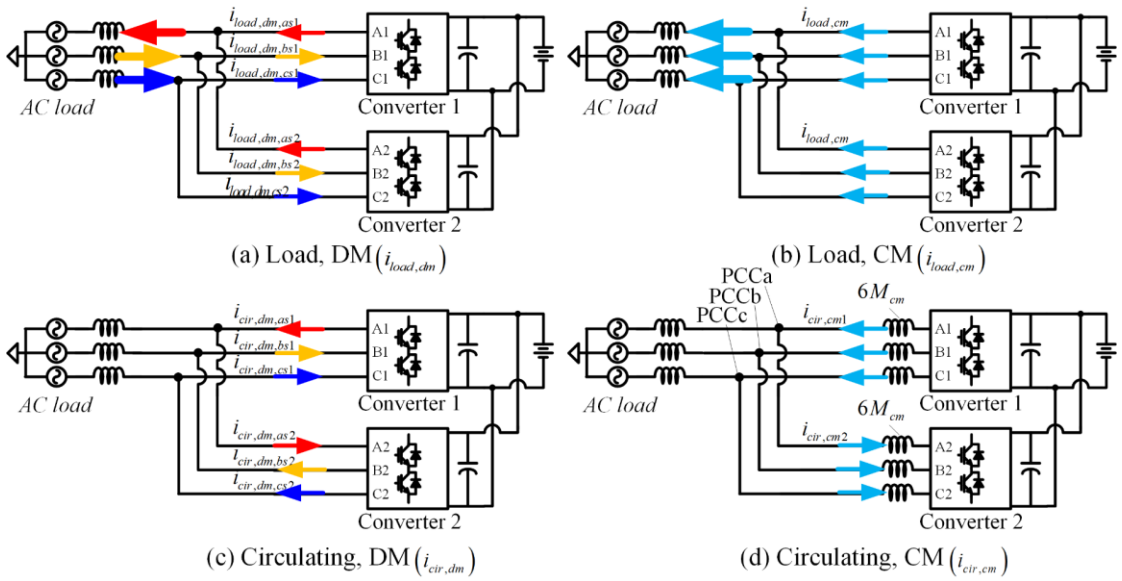


Fig. 2-12. Effective inductances of CMCI for 4 groups of currents.

In the conventional design, one CI is connected to each phase as Fig. 2-13(a). For the proposed DMCI and CMCI, two inductors are connected in series as shown in Fig. 2-13(b). Assuming the leakage inductance (L_{lk}) is negligible, effective inductance provided by the conventional CIs and DMCI, CMCI is summarized in Table 2-2 for 4 groups. With the additional coupling that comes from DM and CM, the proposed structure amplifies effective inductance compared to the conventional CIs. If the coupled inductance of DMCI (M_{dm}) and CMCI (M_{cm}) are designed to have their values as (2.14) they can perfectly replace the conventional CIs.

$$M_{dm}=\frac{2}{3}M_{ci}, M_{cm}=\frac{1}{3}M_{ci} \tag{2.14}$$

Table 2-2. Comparison of effective inductance of three separate coupled inductors and the proposed combination.

Between Converters \ Among 3-phases	Differential-mode $i_{dm,as} + i_{dm,bs} + i_{dm,cs} = 0$	Common-mode i_{cm}
Load (In-phase) $i_{load,xs1} = i_{load,xs2}$	Group 1 $0 \rightarrow 0$	Group 2 $0 \rightarrow 0$
Circulating (Out-of-phase) $i_{cir,xs1} + i_{cir,xs2} = 0$	Group 3 $2M_{ci} \rightarrow 3M_{dm}$	Group 4 $2M_{ci} \rightarrow 6M_{cm}$

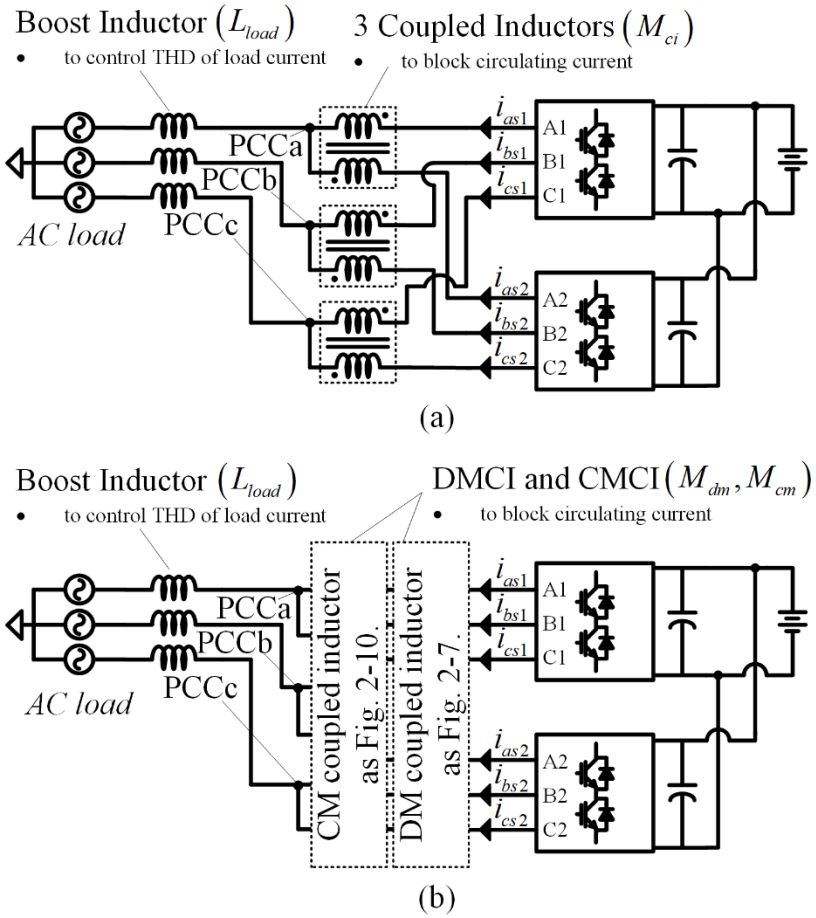


Fig. 2-13. The connection of (a) the conventional coupled inductors, and (b) the proposed DMCI, CMCI.

The prior-arts only utilize the structure of DMCI [55], [59]–[61]. Therefore, different methods have been used to suppress CM circulating current. With the proposed CMCI structure and the series-connection, the DMCI and CMCI can be designed to perfectly replace the conventional CIs with the same impedance but smaller sizes. A specialized PWM scheme to eliminate CM voltage difference [59] is not necessary which increases the switching-loss. The paralleled converters can share the DC-link so that the interleaving can have its benefits on the DC-side [55], [60]. Compared to the structure in [61], the shape of the proposed CMCI adopts widely used core shapes with additional windings and is free from practical issues which may come from complex magnetic structure, e.g., asymmetry of magnetic path or manufacturability. It should be noted that the conduction-loss may increase in the proposed coupled inductors due to its series-connected structure.

2.4 Design Considerations for DMCI and CMCI

2.4.1 Voltage-seconds on DMCI and CMCI considering MI range and PWM scheme

In magnetic designs, the size of the magnetic core is determined by either maximum magnetic flux density $\left(B_{\max}\right)$ or thermal limit [66]. In the flux-limited designs, the size of the coupled inductor is determined by the maximum flux linkage. For CIs, as in Fig. 2-13, the flux-linkage is determined by the time-integral of voltage difference two converters.

The output voltages of a two-level three-phase converter $\left(\overrightarrow{v_{abcs1}}\right)$ can be described by three switching states as (2.15) where S_x is the switching state of phase-*x*. When the output of phase-

x is connected to the positive dc-rail, S_x is 1, and, when connected to the negative dc-rail, S_x is 0.

$$\overrightarrow{v_{abcs1}} - v_{dc}\begin{bmatrix} S_{A1} - \frac{1}{2} \\ S_{B1} - \frac{1}{2} \\ S_{C1} - \frac{1}{2} \end{bmatrix} \tag{2.15}$$

The peak value for volt-seconds difference varies according to MI and PWM methods [67]–[69]. Therefore, possible size-reduction will vary according to the required MI range and PWM scheme.

$$\vec{\lambda}_{cir} = \int_0^{T_{sw}/4} (\overrightarrow{V_{abcs1}} - \overrightarrow{V_{abcs2}})dt \tag{2.16}$$

In [67], the analytical solution of peak volt-seconds is provided for the CIs and common-mode choke in case of SVPWM or DPWM60° [70], [71]. However, in DMCI and CMCI, only DM or CM component generates flux in one magnetic core, respectively. It is not clear how the flux would be distributed in DMCI and CMCI depending on MI and PWM scheme, which eventually determines possible size-reduction. Although DMCI has been found in [55], [59]–[61], the variation of peak flux linkage depending on MI or PWM scheme has not been investigated.

In this section, analytical solutions for maximum flux linkage for DMCI and CMCI are revealed for SVPWM and DPWM60° case. The result shows that the proposed integration

reduces the number of cores as well as the peak flux linkage for magnetic core by decoupling DM, CM flux.

One example of switching state is shown in Fig. 2-14 for SVPWM and DPWM60° when MI = 0.88 and $0 \le \theta < \frac{\pi}{3} - sin^{-1}\frac{1}{MI\sqrt{3}}$, where θ is ab angle for the voltage reference. It is assumed that the voltage reference is identical for the two converters. In the case of SVPWM, the negative peak flux linkage for a single switching period can be written as (2.17) and its DM and CM components can be extracted as (2.18). With given MI, θ that gives the peak flux-linkage can be found. The case for DPWM60° can be derived in a similar way. In the DPWM60° case, several equations exist for peak flux linkage depending on MI. Detailed calculation method of T_0, T_1 and peak flux linkage for the conventional CI can be found in [67], [68]: by space-vector PWM [67] or carrier-based PWM [68].

$$\vec{\lambda}_{cir} = \int_0^{T_0+T_1}\left(\overrightarrow{V_{abcs1}} - \overrightarrow{V_{abcs2}}\right)dt = V_{dc}\begin{bmatrix}-1\\-1\\-1\end{bmatrix}T_0 + V_{dc}\begin{bmatrix}0\\-1\\0\end{bmatrix}T_1 = V_{dc}\begin{bmatrix}-T_0\\-T_0-T_1\\-T_0\end{bmatrix} \tag{2.17}$$

$$\begin{aligned}\vec{\lambda}_{cir,cm} &= -V_{dc}\left(T_0 + \frac{T_1}{3}\right)\begin{bmatrix}1\\1\\1\end{bmatrix}\\ \vec{\lambda}_{cir,dm} &= \vec{\lambda}_{cir} - \vec{\lambda}_{cir,cm} = \frac{V_{dc}}{3}\begin{bmatrix}T_1\\-2T_1\\T_1\end{bmatrix}\end{aligned} \tag{2.18}$$

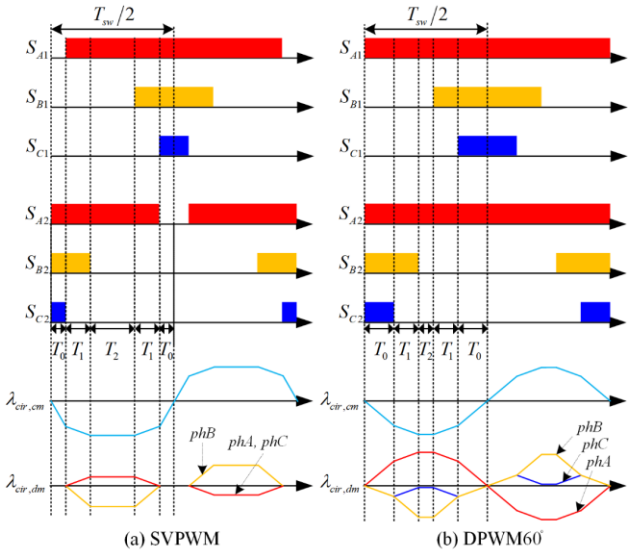


Fig. 2-14. Waveform of switching state at $MI = 0.88$, $0 \le \theta < \frac{\pi}{3} - \sin^{-1}\frac{1}{MI\sqrt{3}}$ (a) SVPWM, and (b) DPWM60°.

Two observations can be noted from Fig. 2-14. First, as there are 3 components in $\vec{\lambda}_{cir,am}$, the phase with the absolute maximum must be found for peak flux linkage. In the example shown in Fig. 2-14, peak DM flux linkage is on phase-B for SVPWM and phase-A for DPWM60°. Secondly, it can be seen in the DPWM60° case, that the DM and CM components for phase-A are out of phase. This indicates that the DM and CM circulating currents may cancel each other to reduce the peak value of total circulating currents. Therefore, the peak value of the total circulating current may not be the sum of the peak value of DM circulating current and CM circulating current.

The analytical equations for peak flux linkages of conventional CIs, DMCI, and CMCI $\left(\lambda_{cir,pk}, \lambda_{cir,dm,pk}, \lambda_{cir,cm,pk}\right)$ are given in Table 2-3 and Table 2-4 as a function of MI and plotted

in Fig. 2-15 and Fig. 2-16 for 2-level SVPWM and DPWM60°. The flux values are normalized by $V_{dc}T_{sw}/4$ which is the maximum value for conventional CIs. The peak flux linkage for CMCI $\left(\lambda_{cir,cm,pk}\right)$ is identical to the one for common-mode choke found in [67]. For DMCI, $\lambda_{cir,dm,pk}$ linearly increases as MI increases in SVPWM. In DPWM60° case, the peak of $\lambda_{cir,dm,pk}$ and $\lambda_{cir,cm,pk}$ happen on MI $= 2/3$. From MI $= \sqrt{7}/3$, the phase corresponding to peak DM flux linkage changes, i.e., from phase-A to phase-B in Fig. 2-14(b) and $\lambda_{cir,dm,pk}$ increases until maximum MI.

Table 2-3. Peak flux linkage as a function of MI: SVPWM.

	$\lambda_{cir,pk}$ for conventional CI	$\lambda_{cir,dm,pk}$ for DMCI	$\lambda_{cir,cm,pk}$ for CMCI
$0 \le MI \le \frac{2}{\sqrt{3}}$	$\frac{V_{dc}T_{sw}}{4}$	$\frac{V_{dc}T_{sw}}{4}\frac{MI}{\sqrt{3}}$	$\frac{V_{dc}T_{sw}}{4}\left(1-\frac{MI}{\sqrt{3}}\right)$

Table 2-4. Peak flux linkage as a function of MI: DPWM60°.

	$\lambda_{cir,pk}$ for conventional CI	$\lambda_{cir,dm,pk}$ for DMCI	$\lambda_{cir,cm,pk}$ for CMCI
$0 \le MI \le \frac{1}{\sqrt{3}}$	$\frac{V_{dc}T_{sw}}{4}\sqrt{3}MI$	$\frac{V_{dc}T_{sw}}{4}MI$	$\frac{V_{dc}T_{sw}}{4}MI$
$\frac{1}{\sqrt{3}} \le MI < \frac{2}{3}$			
$\frac{2}{3} \le MI < \frac{\sqrt{7}}{3}$	$\frac{V_{dc}T_{sw}}{4}$	$\frac{V_{dc}T_{sw}}{4}\left(\frac{5}{6}-\frac{1}{2}\sqrt{MI^2-\frac{1}{3}}\right)$	$\frac{V_{dc}T_{sw}}{4}\left(\frac{5}{6}-\frac{1}{2}\sqrt{MI^2-\frac{1}{3}}\right)$
$\frac{\sqrt{7}}{3} \le MI < \frac{2}{\sqrt{3}}$		$\frac{V_{dc}T_{sw}}{4}\left(\frac{1}{6}+\frac{1}{2}\sqrt{MI^2-\frac{1}{3}}\right)$	

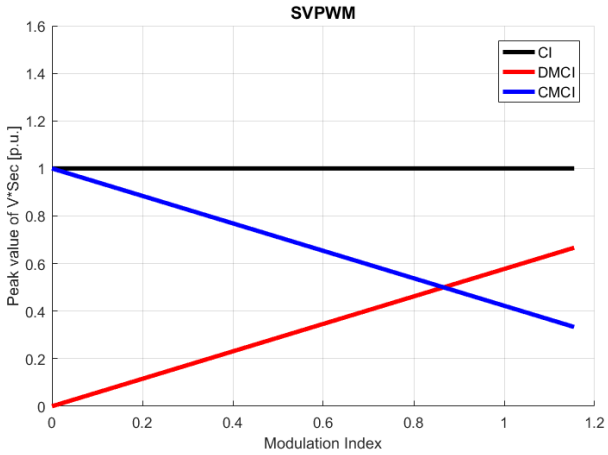


Fig. 2-15. Peak value of normalized volt-seconds: SVPWM.

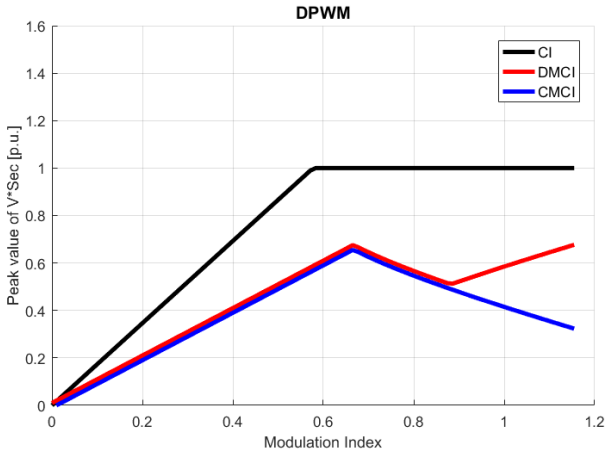


Fig. 2-16. Peak value of normalized volt-seconds: DPWM60°.

When compared to conventional CIs, peak flux linkage of the DMCI and CMCI is 33% smaller within the whole MI range for DPWM60°, and $1/\sqrt{3} \leq MI < 2/\sqrt{3}$ range for SVPWM. This indicates that the proposed integration not only reduces the number of cores from 3 to 2, but also allows the size of each magnetic cores to be smaller than single conventional CI over wide MI range, if thermal constraint permits and the size of the core is determined by maximum flux-density.

The peak value of DM, CM circulating current $\left(i_{cir,dm,pk}, i_{cir,cm,pk}\right)$ can be calculated by (2.20) similar to conventional CI case $\left(i_{cir,pk}\right)$ in (2.19). Note that the peak value for total circulating current may not be the algebraic sum of the peak value for DM and CM components, as these DM and CM components may not be in phase. For the cases where the peak value of circulating current may be given, design criteria for mutual inductance can be (2.19) or (2.20).

$$i_{cir,pk} = \frac{\max\left\{\int\left(V_{xs1} - V_{xs2}\right)dt\right\}}{4M_{ci}} = \frac{\lambda_{cir,pk}}{4M_{ci}} \tag{2.19}$$

$$\begin{aligned} i_{cir,dm,pk} &= \frac{\lambda_{cir,dm,pk}}{6M_{dm}} \\ i_{cir,cm,pk} &= \frac{\lambda_{cir,cm,pk}}{12M_{cm}} \end{aligned} \tag{2.20}$$

2.4.2 Flowchart for designing DMCI and CMCI

In this section, a design flowchart is provided for DMCI and CMCI as shown in. The flowchart assumes specification is given as the peak value of circulating current and that the design process focuses on how DMCI and CMCI can be designed to replace three separate CIs.

First, considering MI range and PWM scheme, desired coupled inductance value can be calculated using (2.19) and Table 2-3, and Table 2-4 for conventional CI [10], [72]. Then, the equivalent inductance for the DMCI, CMCI $\left(M_{dm,}M_{cm}\right)$ can be calculated based on (2.14) which would give the same peak value for total circulating current. Maximum flux-linkage for DMCI and CMCI can be calculated from Table 2-3 and Table 2-4. Finally, with given

M_{dm}, M_{cm} and $\lambda_{cir,dm,pk}, \lambda_{cir,cm,pk}$, DMCI and CMCI can be optimized following a magnetic design optimization process. The value for B_{sat} may come from the limitation of the core material or another upper boundary can be set to control the core-loss in the CIs. Optimization of DMCI and CMCI is not within the scope of this work, therefore the flowchart only illustrates how DMCI and CMCI can be designed from system specifications, using Table 2-3 or Table 2-4.

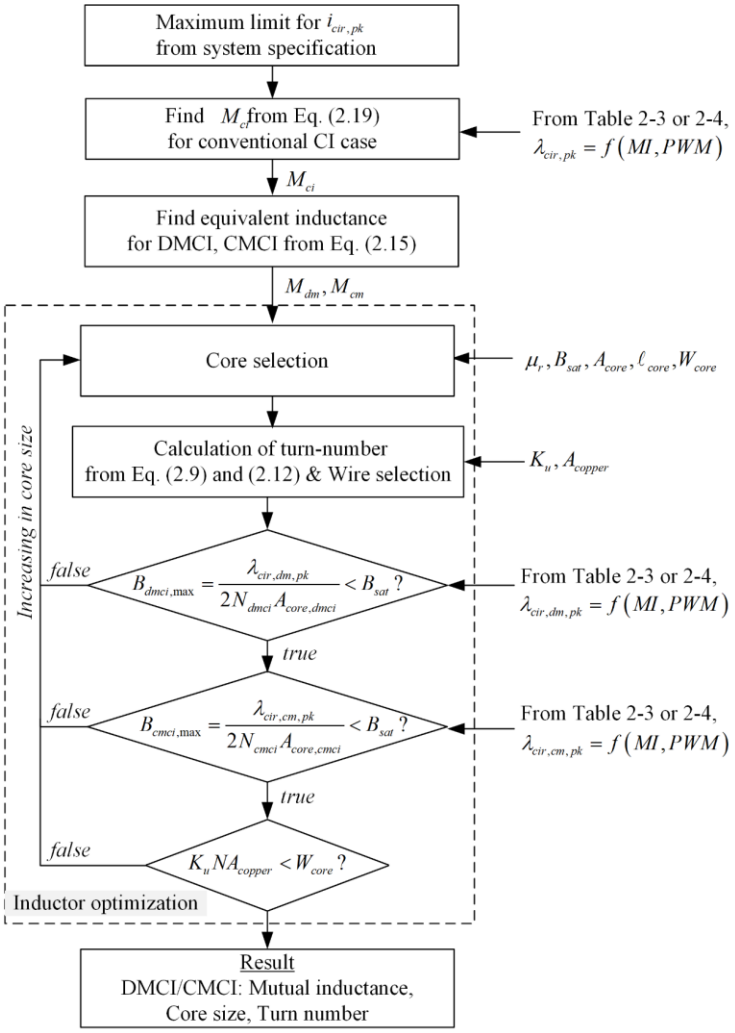


Fig. 2-17. Flowchart for DMCI, and CMCI design.

2.4.3 Remarks on thermally-limited designs

The scope of this work is limited to the case where the size constraint comes from maximum flux-density in the magnetic core. The analytic solutions for modulation index (MI) versus peak magnetic flux for CI, DMCI, and CMCI theoretically support possible size reduction. Before prototyping, a finite element analysis (FEA) has been performed to verify thermal aspects including the wire-loss. The volume loss-density of all three cases showed low value (Conventional CI: 18 mW/cm^3, DMCI: 22 mW/cm^3, CMCI: 36.7 mW/cm^3) compared to thermally-limited designs [66]. This low loss-density mainly comes from low core-loss of the ferrite material (3F3 from FERROXCUBE) and relatively low current density ($2\ A/mm^2$).

However, in other cases, the thermal issue may limit the possible size-reduction. Especially in the coupled inductors, no low-frequency flux exists in the core and it is probable that the size is limited by the temperature rise of the inductor. In such cases, possible size reduction may not be similar to the flux-limited case and the peak flux may not be an accurate indicator to compare the inductor size. The design procedure should consider the difference in thermal models among the conventional CI, DMCI, and CMCI. Since DMCI and CMCI are built with commonly used core shapes, the models for such structures can be extended while an impact from the multi-winding structure should be considered.

2.5 Prototype Design and Simulation Result

Two types of simulation have been conducted. Circuit simulation has been done to verify the feasibility of the proposed coupled inductors. Finite Element Analysis (FEA) has been conducted for magnetic analysis of prototype design as well as to compare loss.

2.5.1 Circuit Simulation

Targeting aircraft applications, 1 kW paralleled 2-level converters as shown in Fig. 2-13 are used for the circuit simulation. Parameters are summarized in Table 2-5. Instead of a three-phase ac load, three 8 Ω resistors $\left(R_{load}\right)$ are used and one 3-phase inductor $\left(L_{load}\right)$ is placed between the resistors and PCC. Two converters are interleaved by 180°. The mutual inductance of DMCI in (2.8) and CMCI in (2.11) is set to have the same impedance as a conventional case, based on (2.14).

Table 2-5. Parameters for PLECS simulation.

Parameter	Value	Parameter	Value
V_{dc}	150 V	f_{sw}	20 kHz
f_0	400 Hz	PWM	DPWM60°
L_{load}	330 μH	R_{load}	8 Ω
M_{dm}	1.0 mH	M_{ci}	1.5 mH
M_{cm}	0.5 mH	Modulation Index	0.96
i_{ds}^*	0 A	i_{qs}^*	4.5 A

The waveforms of load current, converter 1 current are shown in Fig. 2-18 and Fig. 2-19. In the circuit for simulation, no path exists for CM current at the load. Therefore, the current of group 1 $\left(i_{load,dm}\right)$ only flows into the load. Assuming that the leakage inductance is negligible, the coupled inductors only suppress the circulating current $\left(i_{cir,dm}, i_{cir,cm}\right)$ and there is no change in the load current for either case. The waveforms of converter 1 currents are compared in Fig. 2-19. The DM, CM circulating current in groups 3 and 4 and fundamental-frequency $\left(f_0\right)$ components in the group 1 flow in the converter 1 current. The mutual

inductances of DMCI, CMCI is designed to have the same level of attenuation as (2.14) hence THD of the converter 1 current remains the same for both cases.

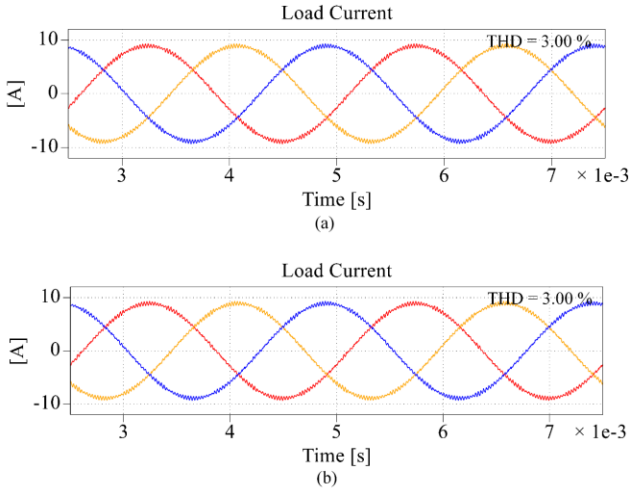


Fig. 2-18. Waveforms of load current with (a) conventional coupled inductors, and (b) DM, CM coupled inductor.

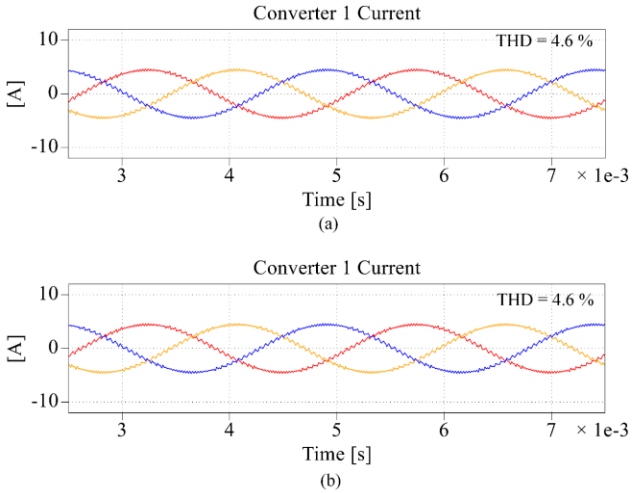


Fig. 2-19. Waveforms of converter 1 current with (a) conventional coupled inductors, and (b) DM, CM coupled inductor.

Flux-linkage of winding A1 (λ_{as1}) is compared in Fig. 2-20. for DPWM60° and SVPWM case. For the conventional one, the DM and CM circulating current in groups 3 and 4 both generate the flux in the CI and the peak value reaches 1.875 $mV \cdot s$ for both PWM schemes. In the proposed coupled inductors, the flux for DM and CM circulating current can be decoupled into two different cores, so its peak value for each core could be reduced. For the DMCI, the peak values are around 1.03 $mV \cdot s$ and, for CMCI 0.84 $mV \cdot s$. This is a reduction of 45% and 55%, respectively. In this case, the reduction on volt-sec. is similar for both DPWM60° and SVPWM cases. From Fig. 2-15 and Fig. 2-16, it can be seen that both PWM scheme shows similar peak flux-linkage after MI = 0.9 as a duration of zero-vector becomes small. Below MI ≅ 0.9, possible reduction on volt-sec. may vary between two PWM schemes.

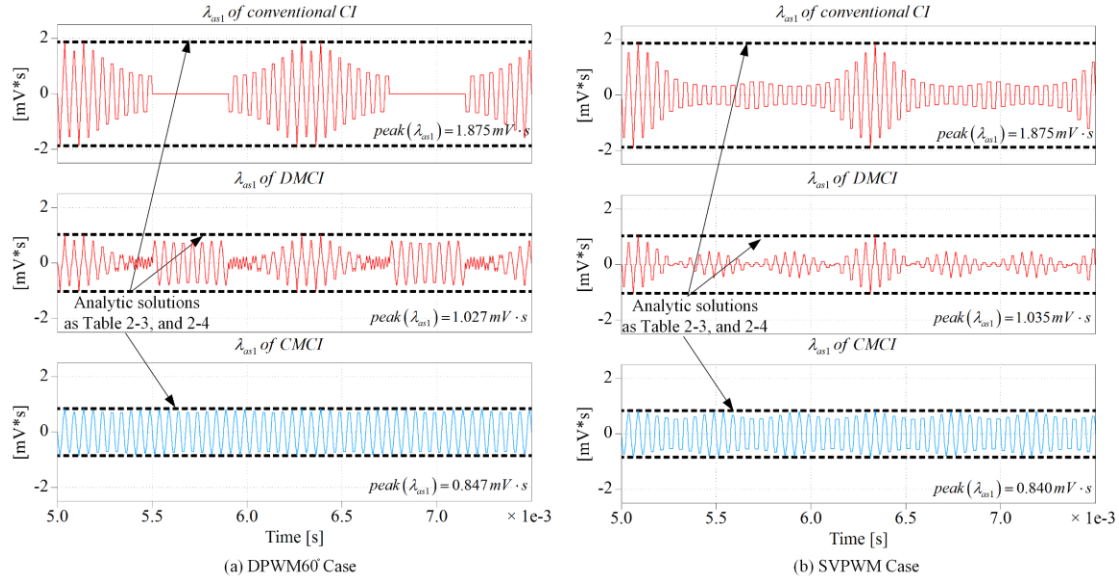


Fig. 2-20. Waveforms the flux of A1 winding: MI = 0.96 (a) DPWM60°, and (b) SVPWM.

2.5.2 Prototype design and finite element analysis (FEA)

Prototype coupled inductors have been designed and FEA has been conducted to verify the size-reduction and to compare loss. The three CIs and the proposed DMCI, CMCI are designed to have a similar maximum magnetic-flux density $\left(B_{\max}\right)$ at MI = 1.0 in the DPWM60° case. The summary of the inductor design is shown in Table 2-6.

Table 2-6. Summary of coupled inductor design.

	CIs	DMCI	CMCI
Material	FERROXCUBE 3F3 $B_{sat} = 0.4\ T, \mu_r = 2000$		
B_{max}	0.24 T	0.23 T	0.19 T
Shape	U67/27/14	E55/28/21	U67/27/14
Core Weight	510.0 g	191.5 g	170.0 g
		361.5 g (-30%)	
Core Volume	155.9 cm^3	65.0 cm^3	52.0 cm^3
		117.0 cm^3 (-25%)	
Wire	Litz wire, AWG 15, 10.5 mΩ/m		
Mutual inductance	1.38 mH	920 uH	393 uH
# of Turns	21	16	12
Wire Length	7.2 m	5.1 m	4.11 m
		9.21 m (+28%)	
Wire Weight	105.6 g	74.8 g	60.3 g
		135.1 g	
Wire Volume	11.9 cm^3	8.41 cm^3	6.78 cm^3
		15.2 cm^3	
Total Weight	615.6 g	496.6 g (-20%)	
Total Volume	167.8 cm^3	132.2 cm^3 (-22%)	

For the core material, 3F3 from FERROXCUBE is selected. Considering the switching frequency (20 kHz), the best choice for CIs could be amorphous. Even low-frequency ferrite materials are targeting up to 200 kHz range. However, due to the availability of the size, and cost of customization to make the three-limb core for DMCI, the ferrite core is used instead.

The initial attempt was to use 3C95 material which has a flat loss characteristic along with the temperature. This is because a thermal analysis on such an integrated structure could not be easily done. Due to the availability of the cores, 3F3 material is selected as a final choice. A boost inductor is separately designed with an amorphous core which is AMCC-008 from Hitachi Metals and used for both cases.

U67/27/14 is used to build both conventional CIs and CMCI. DMCI is built with E55/28/21. The center limb of E55/28/21 has been cut in half to be equal to the area of the side limbs. No air gap exists for the three CIs. Total weight of core has been reduced by 30% and size by 25%. AWG 15 equivalent Litz wire has been used, which gives a current density of 2 A_{rms}/mm^2. The DMCI and CMCI are series-connected and this series-connection of two cores increased the wire length. In the prototype design, the total wire length is increased by 28% in the proposed structure. The total weight and volume, including the wires, are decreased by 20% mainly due to the size-reduction of the magnetic cores.

By FEM simulation, the maximum flux density (B_{max}) has been verified as Fig. 2-21 and core-loss has been simulated. In Fig. 2-21, the numbers below the figures indicate the length, width, and height of the magnetic core for each case. For FEM simulation, the circulating currents from PLECS simulation from Chapter 2.5.1 are used as excitation currents. Coefficients of Steinmetz equation for core-loss calculation are extracted from the datasheet of 3F3 material.

The result is summarized in Table 2-7. For the CI, core loss is around 444.5 mW which brings the sum up to 1334 mW total. For the DMCI and CMCI, core loss is 400 mW and 1020 mW. Total core-loss increases by 6.5%. Conduction loss is 1465 mW for the three CIs and

1874 mW for DMCI and CMCI. Series-connection of DMCI and CMCI contribute to an increase in the conduction-loss. Total loss from coupled inductors increases by 18% from 2.8 W to 3.3 W. However, a 0.5 W is only 0.05% of whole system power rating, which is 1kW, and loss from the coupled inductors does not significantly deteriorate system efficiency in given operating condition.

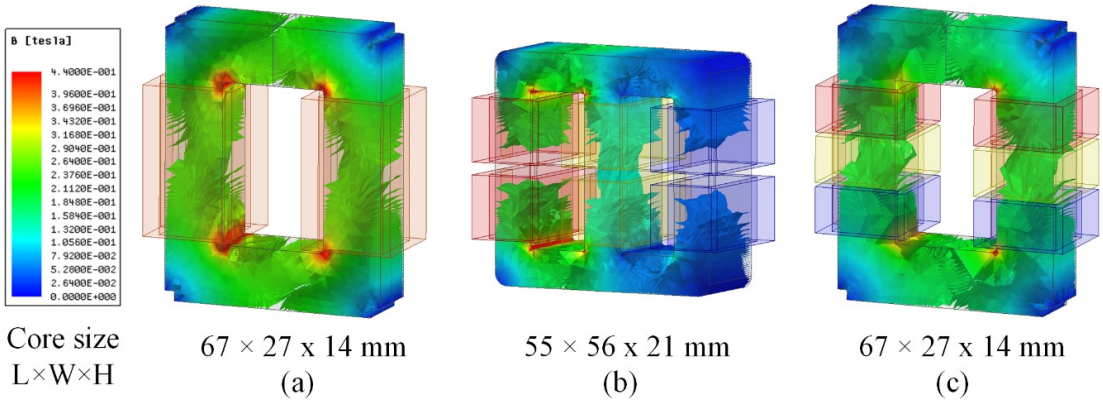


Fig. 2-21. FEA result (a) CI, (b) DMCI, and (c) CMCI.

Table 2-7. Loss comparison.

	CIs	DMCI	CMCI
Core-loss	1333.5 mW	400 mW	1020 mW
		1420 mW (+6.5%)	
Conduction-loss	1465 mW	1038 mW	836.4 mW
		1874.4 mW (+28%)	
Total Loss	2799 mW	1438 mW	1856 mW
		3294 mW (+18%)	

2.6 Comparison with Boost Inductor Integration Scheme

In motor drive application [11], [55], [59]–[61], the load inductance serves an output inductor as in Fig. 2-13. However, in the other applications such as grid-connected converters, a separate inductor exists to attenuate the load-side current ripple. In [36], an integrated inductor has been proposed combining the boost inductor and 3 CIs into one magnetic core to

reduce both the weight of the magnetic cores and the winding material. In this section, a comparison has been performed with the integrated inductor in [36].

The structure of the integrated inductor in [36] is shown in Fig. 2-22. There are three phase-legs, two bridge-legs on the front- and back-side, and one common-leg. Equivalent magnetic circuits for the group 1, 3, and 4 are shown in Fig. 2-23. Based on the magnetic circuit analysis, the effective inductance for each group can be calculated as Table 2-8 where $A_{c,pl}$, $A_{c,cl}$, and $A_{c,bl}$ are the core area of the phase-legs, common-leg, and bridge-leg. $2l_{leg}$ is mean path length of the phase-leg and common-leg. l_g is the air gap between the bridge-legs and phase-legs.

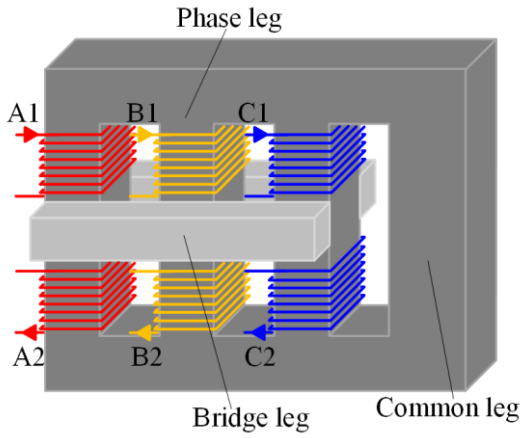


Fig. 2-22. Structure of the integrated inductor in [36].

Two magnetic materials are utilized to build the integrated inductor. Only DM load current with low THD $\left(i_{dm,load,xs}\right)$ generates the flux in the bridge-legs. Therefore, a material with high saturation flux-density $\left(B_{sat}\right)$ and relatively higher core-loss is utilized such as laminated iron cores. The common-leg and phase-legs are built with a material which has high permeability

and low core-loss to handle the flux by high-frequency circulating currents. In [36], a ferrite material with $\mu_r = 2300$, $B_{sat} = 0.47\ T$ is used to build the phase-legs and common-leg.

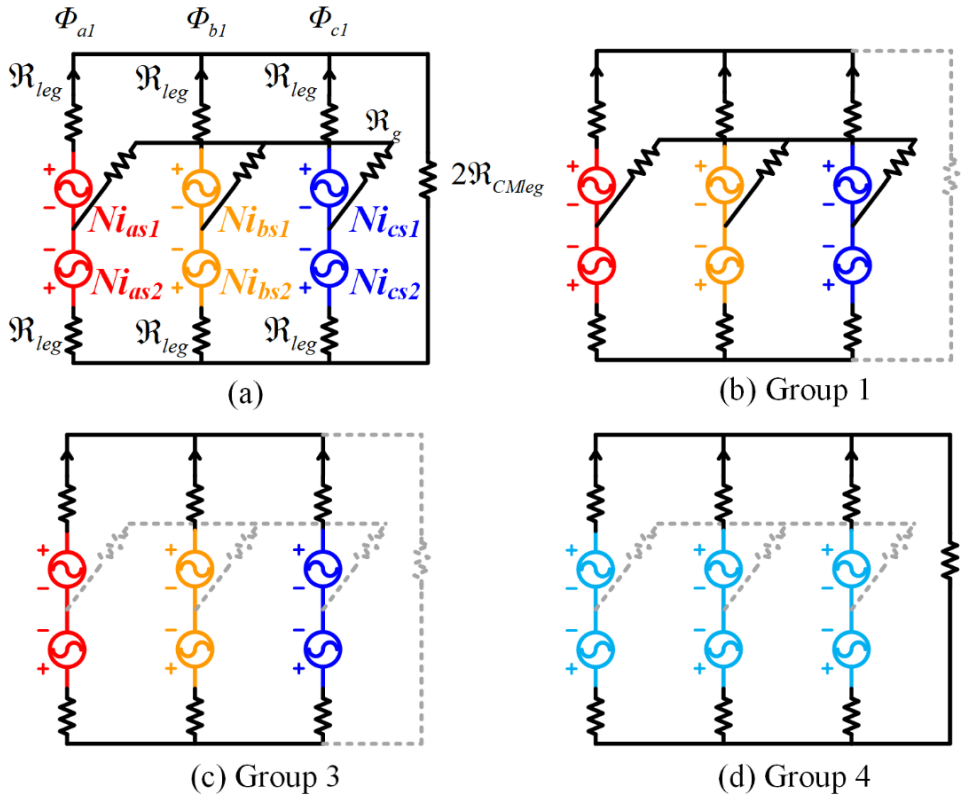


Fig. 2-23. (a) Magnetic circuit of integrated inductor in [36] (b) for DM, load, (c) for DM, circulating, and (d) for CM, circulating.

Table 2-8. Effective inductance of the integrated inductor.

Between Converters \ Among 3-phases	Differential-mode $i_{dm,as} + i_{dm,bs} + i_{dm,cs} = 0$	Common-mode i_{cm}
Load (In-phase) $i_{load,xs1} = i_{load,xs2}$	$L_f = \frac{\mu_0 N^2 A_{c,bl}}{2l_g}$	0
Circulating (Out-of-phase) $i_{cir,xs1} + i_{cir,xs2} = 0$	$M_{dm,eq} = \frac{\mu_0 \mu_r N^2 A_{c,pl}}{l_{leg}}$	$M_{cm,eq} = \frac{\mu_0 \mu_r N^2}{l_{leg}} \frac{A_{c,cl} A_{c,pl}}{A_{c,cl} + 3A_{c,pl}}$

Note that both the large fundamental DM load currents and high-frequency circulating components generate the flux in the phase-legs. From the magnetic and electric circuit analysis, the maximum flux density of the phase-legs $\left(B_{pl,m}\right)$ can be expressed as (2.21). With the given circuit parameters, the maximum volt-sec. for the phase-leg $\left(\lambda_{pl,m}\right)$ is largely determined by the flux term for the output DM current $\left(2L_f i_{load,dm,xs}\right)$. To reduce the size of the phase-legs, it is desirable for the material to have both high B_{sat} and high permeability at the multiples of f_{sw}. If $B_{pl,m}$ is small, $NA_{c,pl}$ term will be large as shown in (2.21) which indicates that either a large turns-number or a large magnetic core is required.

$$B_{pl,m} = \frac{1}{NA_{c,pl}} \max\left(2L_f i_{load,dm,xs} + \frac{\lambda_{cir,dm,xs} + \lambda_{cir,cm}}{2}\right) = \frac{\lambda_{pl,m}}{NA_{c,pl}} \tag{2.21}$$

Therefore, the possible size-reduction will be largely determined by the maximum flux-density available for the high-permeability material $\left(B_{hp,m}\right)$ for the phase-legs. $B_{hp,m}$ may be limited by availability of the materials for target f_{sw}. For an example, most of low-frequency ferrite materials have $B_{sat} < 0.6T$ [73], [74]. Also, thermal constraints may put a limit on $B_{hp,m}$ value. The flux by the circulating currents adds additional core-loss on the phase-legs. If a material with high B_{sat} and relatively higher core-loss is used such as an amorphous core, $B_{hp,m}$ may have to be reduced to mitigate a temperature-rise [75].

Two cases of integrated inductor have been designed to compare size In the first case, a ferrite material has been used and $B_{pl,m}$ is set to $0.25T$. Two E-core pairs (0R48020EC from

Mag-Inc) are stacked and the center-limbs are cut to half to build the phase-legs. In the second case, the phase-legs are built from amorphous cores. Two U-core pairs (AMCC-004 from Hitachi Metal) and an outer strap are assembled to make a three-limb core. $B_{pl,m}$ is set to $1.0\,T$ assuming that the thermal constraints do not put a limit on $B_{hp,m}$ and the core for the common-leg is assumed to be customized to fit the structure. The separate boost inductor with the laminated iron core is assumed to have the same size as the E-core built from AMCC-004. Compared to the case with DMCI, CMCI, and the separate boost inductor, the ferrite design showed a 16% increase in the total weight. A large turns number was required to compensate low $B_{pl,m}$. The design with an amorphous core assembly showed a 20% decrease in the total weight.

Table 2-9 Summary of comparison with the integrated inductor in [36].

	Material	A separate boost inductor, DMCI, and CMCI		Integrated inductor with ferrite core		Integrated inductor with amorphous core	
		Core weight	Wire weight	Core weight	Wire weight	Core weight	Wire weight
Boost inductance	Laminated Iron	400.3 g	105 g	122 g	-	257.4 g	104.8 g
Coupled inductors	Ferrite	361 g	135 g	737.5 g	358 g	-	-
	Amorphous	-	-	-	-	454.0 g	-
Total		761.3 g	240 g	859.6 g (+5%)	358 g (+50%)	711.3 g (-7%)	104.8 g (-40%)
		1.001 kg		1.218 kg		0.813 kg	

In summary, the proposed integrated CIs with a separate boost inductor can provide size-reduction compared to the integrated inductor in [16] which combines both the boost inductor and CIs depending on the maximum flux-density or material choice for the phase-legs.

2.7 Experimental Results with Prototype Design

A prototype has been constructed and an experimental test has been performed. The circuit and parameters for the experiment are as shown in Fig. 2-13 and Table 2-5. The picture of conventional CIs, DMCI, and CMCI is shown in Fig. 2-24. Total weight and size of the CIs could be reduced by 20%.

Fig. 2-24. Size comparison of conventional design and integrated design.

Load currents, converter 1 currents, and circulating currents have been compared. The waveforms for load currents are compared in Fig. 2-25. THD is 3.7% with conventional CIs and 4.0% with the proposed structure. The frequency spectrum shows a good match between the two cases. The waveforms for converter current are compared in Fig. 2-26. THD of converter 1 current is 4.7% and 5.0%. In the frequency spectrum, a small difference exists for f_{sw} sideband harmonics, which contributes to THD difference. In the prototype design, the

mutual inductance for CMCI has a smaller value than the one required for the same level of attenuation ($2M_{ci} = 2.76\,mH > 6M_{cm} = 2.358\,mH$) and the attenuation for CM circulating current is slightly lower in CMCI case.

Circulating currents have been extracted from converter 1 current waveform and the one for phase-A are shown in Fig. 2-27 and Fig. 2-28. As CM load current in group 2 is negligible, current in groups 1, 3 and 4 can be extracted by (2.22). Magnitudes of switching ripple component are similar in two cases, which is within 0.3A with a fundamental current of 4.5A.

$$\begin{aligned} i_{cir,as1} &= \frac{i_{as1} - i_{as2}}{2} \\ i_{cir,cm1} &= \left(i_{as1} + i_{bs1} + i_{cs1}\right)/3 \\ i_{cir,dm,as1} &= i_{cir,as1} - i_{cir,cm1} \end{aligned} \tag{2.22}$$

Several current spikes are observed in the circulating current waveform. The system targets an aircraft application in which the fundamental frequency is 400 Hz and main low-frequency CM circulating currents are located at 1.2 kHz and 2.4 kHz. During the experiment, the bandwidth of a CM circulating current controller was limited to 1 kHz with 20 kHz switching frequency. As a result, the low-frequency CM circulating currents were not able to be fully eliminated. Consequently, the CIs and CMCI went into slight saturation at peak of this low-frequency CM circulating current.

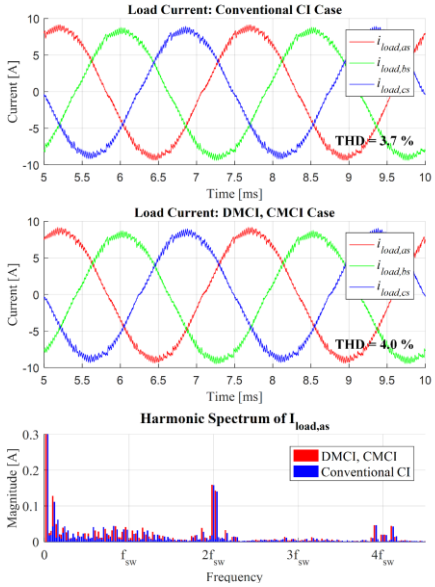


Fig. 2-25. Waveform of phase-A load current (a) with conventional coupled inductors, (b) with DM and CM coupled inductor, and (c) frequency domain comparison.

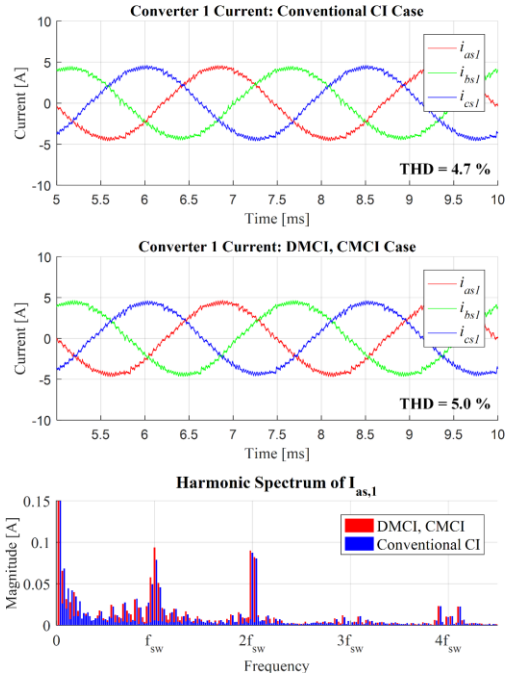


Fig. 2-26. Waveform of converter 1 current (a) with conventional coupled inductors, (b) with DM and CM coupled inductor, and (c) frequency domain comparison.

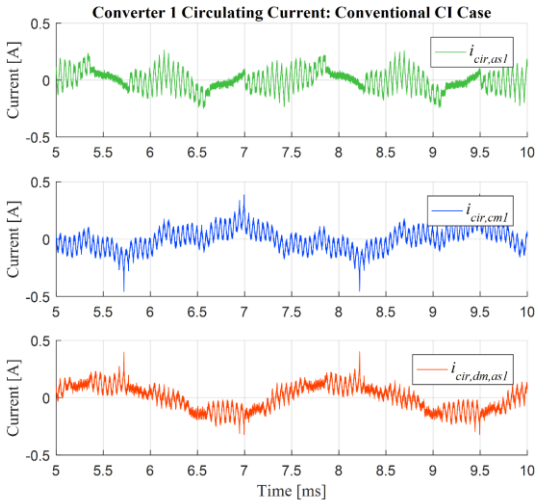


Fig. 2-27. Circulating current in conventional CI case: Total circulating current, CM component, and DM component.

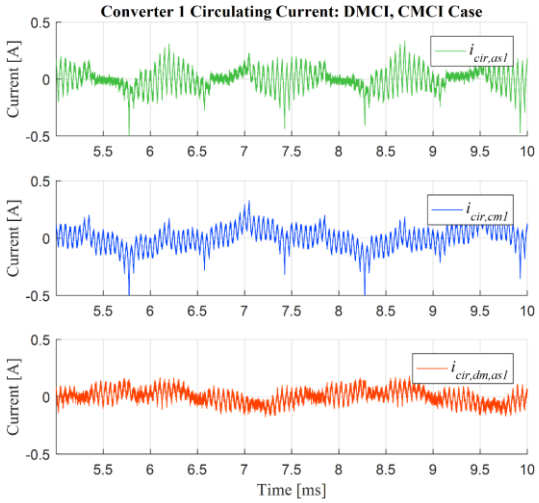


Fig. 2-28. Circulating in DMCI, and CMCI case: Total circulating current, CM component, and DM component.

In a conventional CI case, fluxes of DM and CM components are coupled in the core. Even when phase-A is clamped and $i_{cir,as1}$ is near zero, the saturation of the CIs in the other phases generates spikes in $i_{cir,cm1}$ and thus creates the spikes in $i_{cir,dm,as1}$ as well. On the other hand, no

coupling exists between the DM and CM component with the DMCI and CMCI. The saturation of CMCI is only reflected in $i_{cir,cm1}$ and $i_{cir,as1}$ where $i_{cir,as1} = i_{cir,dm,as1} + i_{cir,cm1}$.

These spikes and the low-frequency CM components cause deviation from the experimental waveforms in Fig. 2-28 and the simulation waveform in Fig. 2-20(a). Note that the design procedure shown in Fig. 2-17 assumes that such low-frequency components do not exist with the zero-sequence current control. In most of the applications where the low-frequency CM circulating component can be located at a much lower frequency than the controller bandwidth, such spikes will not exist. Even with the presence of the saturation spikes, the magnitude of switching ripple components remains similar in the two cases. This can also be confirmed from the frequency spectrum in Fig. 2-26. Also, to handle the low frequency circulating component, the three CIs has to be oversized while only the size of CMCI needs to be increased thanks to the decoupling of CM and DM circulating flux in the proposed combination. Therefore, the experimental results validate that the proposed CIs gives the same level of attenuation for high frequency circulating current with reduced sizes.

2.8 Chapter Summary

In this chapter, an integrated structure for coupled inductors in three-phase paralleled AC-DC converters is proposed. According to differential-mode, common-mode and phase-shift by 180° interleaving, the converter current is classified into 4 groups. Based on this systematic classification, a combination of DMCI and CMCI are proposed to suppress DM and CM circulating current. The structure of DMCI and CMCI combines a conventional three-phase inductor and common-mode choke with a coupled inductor and can be easily implemented

with standard shape cores. Series-connection of two proposed coupled inductors completely replaces the three coupled inductors in the three-phase system. For the flux-limited magnetic designs, analytic solutions for maximum volt-seconds of DMCI and CMCI are derived for SVPWM and DPWM60° case. The results show that maximum volt-second can be smaller in the proposed structure by decoupling of CM and DM component. Based on the analytic solution, design guidelines for the DMCI and CMCI are shown to provide the identical impedance with a smaller size compared to the conventional CIs. Prototypes are designed for 1 kW interleaved converters and their size and weight are compared. With given operating conditions, the volume and weight have been reduced by 20%. Loss comparison has been done with FEM simulation and the prototype design indicates an 18% increase, mainly by conduction-loss. However, the amount of increase is 0.5 W with a system power rating of 1 kW. Experimental results showed that THD of two converter current waveforms remains the same with the size and weight reduction of 20%.

Chapter 3. Three-Terminal Common-Mode EMI Model for EMI Generation, Propagation, and Mitigation in a Full-SiC Three-Phase UPS Module

3.1 Introduction for Chapter 3 to 5.

Throughout chapter 3 to 5, schemes for power density improvement of the full-SiC uninterruptible power supply (UPS) have been presented. In applications such as power supplies for hospitals and data-centers, electric power must be ensured seamlessly even when there exists a power interruption in the main grid. In these applications, a short outage of power may result in a high expense or catastrophic result. To secure ac-power toward load even when the main grid fails, power electronics circuits with energy storage are equipped.

Fig. 3-1 shows an example of a circuit configuration for UPS. One UPS module is comprised of the rectifier, inverter, and a dc-dc stage. The rectifier and inverter together form an ac-ac stage. A battery-rack as energy storage is connected to the dc-link of the ac-ac stage. For tens or hundreds of kW-level, multiple UPS modules are paralleled to increase the power capability and ensure redundancy in case of a module failure.

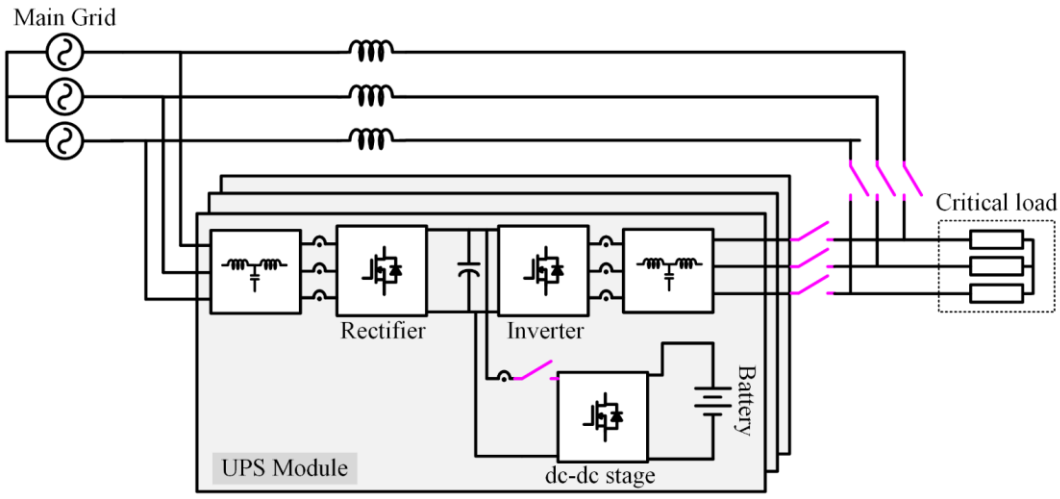


Fig. 3-1. Structure of three-phase modular UPS.

Several operation modes exist depending on power transfer. Depending on the operation mode, a different combination of the rectifier, inverter, and dc-dc stage is involved. In normal condition, the ac-ac stage operates and provide a sinewave voltage to the critical load regardless of distortions on the main grid. Meanwhile, a battery management system (BMS) senses a state-of-charge (SOC) of the battery-rack, and, if the battery-rack is not fully charged, the rectifier and the dc-dc stage operate to charge the battery. Once the main grid fails, the rectifier shuts off and the energy stored in the battery is discharged by the inverter.

Two observations can be made from the operating principle. Firstly, the UPS is comprised of multiple power stages, the power is always transferred through more than two stages. As the double conversion efficiency is the product of the efficiencies of two stages, the efficiency of each stage becomes more important which may see a significant improvement by the adoption of SiC devices. The charge capacity of the battery is limited, and more loss during power conversion will result in shortened hold-up time to serve the critical load. Secondly, noise

phenomena are complex. Multiple power stages together with multiple modes of operations complicate the generation and propagation of noise. Especially, the ac-ac stage and dc-dc stage with the battery rack share the common dc-link and the noise from these stages will be mixed, depending on the operation mode.

From chapter 3 to 5, an EMI modeling, topology selection, improved PWM scheme, and hardware optimization are covered. The system specification is summarized in Table 3-1. A picture of a prototype and measurement setup is shown in Fig. 3-2. Details on topology selection, EMI modeling, employed PWM scheme, and detailed procedure for prototyping will be covered in each chapter.

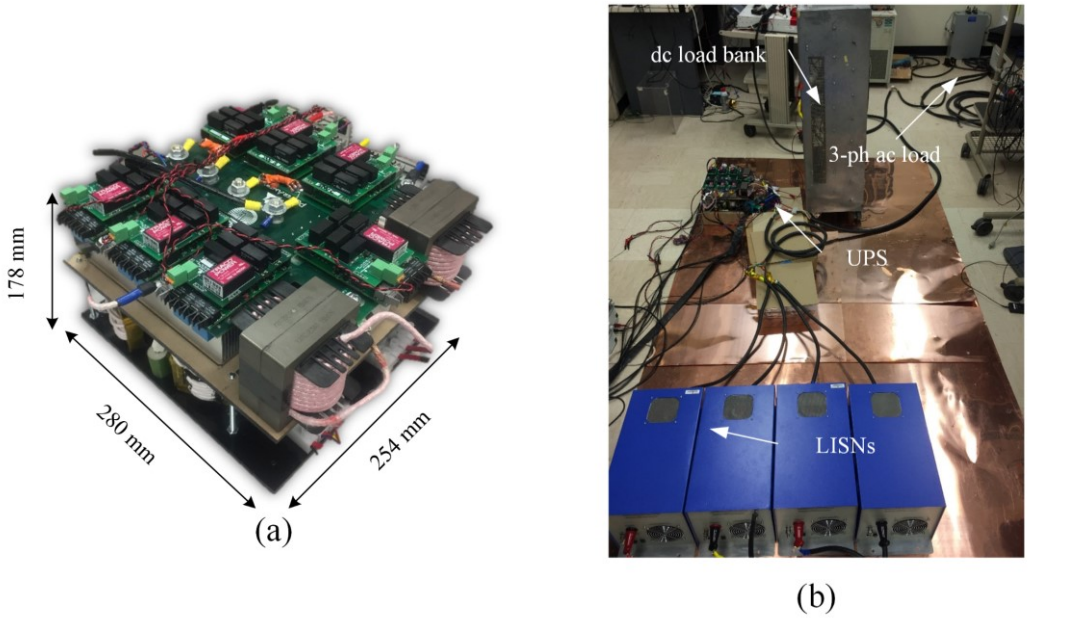


Fig. 3-2. (a) 20 kW full-SiC UPS prototype, and (b) an experimental setup for EMI measurement.

Table 3-1. System specification.

Parameter	Value	Parameter	Value
Grid voltage	480 V	DC-link voltage	800 V
Frequency	60 Hz	Nominal battery voltage	540 V
Power rating	20 kW	THD	2%
EMI standard	IEC62040-2		

3.2 Chapter Introduction

Wideband-gap (WBG) devices have received attention from the industry due to superior performance over Si-based IGBTs. An uninterruptible power supply (UPS) is an application in which ultra-low loss characteristics of WBG devices can significantly improve system efficiency. With mature Si-based IGBT technology, the efficiency of double conversion (ac-ac conversion) is limited below 98% for three-phase UPSs. With SiC devices, 99% efficiency per one power stage is conceivable and double conversion efficiency up to 98% [76], [77] can be obtained.

While the UPS benefits from high-efficiency, electromagnetic interference (EMI) problems arise from high *dv/dt*, *di/dt* of SiC devices and higher switching frequency [78]–[80]. Especially, the common-mode (CM) noise is difficult to deal with, as propagation varies according to physical layout and parasitic components of the system [81]. Since the UPS generally feeds sensitive loads in hospitals or data centers, conductive noise emission is strictly limited from 150 kHz to 30 MHz by standards as IEC62040-2 shown in Table 3-2 [82]. In general, passive filters are used to handle the conductive common-mode (CM) emission, where the magnetic components as common-mode chokes dominate the size and weight of the filters. With increased switching frequency enabled by SiC MOSFETs, the volume and weight of these CM EMI filters may increase significantly [3], [50], [83] since the sizes of these magnetic

components increase. Also, the CM current during converter operation can cause false triggering of protection circuits.

Table 3-2. Conductive EMI limit in IEC62040-2: Category C3 UPS with rated current < 100 A.

Frequency Range [MHz]	Quasi-Peak Limits [dBμV]
0.15 – 0.50	100
0.50 – 5.0	86
5.0 – 30.0	90 to 73

Furthermore, the UPS consists of multiple power conversion stages and has several modes of operation which complicates the EMI problems. The UPS under study comprises a rectifier and an inverter for ac-ac conversion, and an active battery charger with a battery rack as energy storage. IEC62040-2 requires the limit of conductive noise shall be met in the mode of operation with maximum emission [82]. Noise emission, propagation path, and interaction between the stages are distinct since different combinations of the rectifier, inverter and dc-dc converter are active during different modes. This makes a prediction of the EMI spectra difficult and calls for deliberate strategies to be set before prototyping. Especially, literature has reported that large parasitic capacitance up to tens of nanofarad (nF) may exist between battery terminals and metal housing due to a large footprint of the battery [84]–[87]. This large parasitic component provides a propagation path for high-frequency noise and may bring a huge change in noise phenomena when the dc-dc converter operates.

EMI models can be used to predict the EMI spectra and set appropriate EMI strategies during the design phase [88]. A number of researchers have adopted a simplified frequency-domain model. The EMI remedies for a complex system such as UPS or back-to-back

converters can be validated and compared [86], [89]–[94] while the accuracy of the frequency-models are limited at MHz since the model includes only major parasitic components [95]. However, most research focuses only on the ac-ac stage alone. It is not clear how the noise mechanism will be influenced by the operation of the dc-dc converter which interfaces large energy storage to the dc-link of the ac-ac stage.

In [89], a comprehensive EMI analysis is conducted for a modular UPS in both time domain and frequency domain. Based on the model, a parametric study for parasitic components and the impact of interleaving in the modular structure is investigated for the ac-ac stage. However, the scope of the research is limited to the double-conversion mode even though a large battery-rack and an active charger exist in the system. In [90], a filter structure with an artificial ground is proposed to contain the CM noise current for a back-to-back converter system. In [91], [92], a frequency domain model is used to evaluate the filter and provide a design guideline for a UPS [91] or back-to-back converter [92]. In [96]–[98], PWM schemes for a two-level back-to-back converter are proposed which utilize common-mode voltage (CMV) cancellation between the rectifier and inverter to reduce the CM current. However, the scope of these studies is limited to the ac-ac conversion case and does not show how the operation of the dc-dc converter will change the CM noise profile.

In [93], a CM equivalent circuit for a medium voltage dc distribution system is proposed to connect multiple converters and subsystems. Based on the model, the impact of different grounding scheme on the CM current is investigated. However, the experimental result does not include a dc-dc converter and energy storage. The impact of the same on the CM EMI was not investigated.

In [86], the impact of battery connection on the CM EMI is investigated for a UPS with experimental validation. A diode rectifier is used for an input grid and a large battery-rack is directly connected to the dc-link by long cables. With a battery connection, a maximum 20 dB increase is reported in conductive CM EMI over a wide frequency range. However, this increase came from the long cables connecting the battery to the dc-link. A detailed analysis for deteriorated CM EMI is absent. Also, the dc-dc converter is not present in the system. It is uncertain how the topologies or the PWM schemes of the dc-dc stage will influence the CM EMI.

In this chapter, an EMI generation, propagation, and mitigation strategy for a full-SiC three-phase UPS with an active battery charger have been investigated based on a three-terminal CM circuit model, focusing on the impact of the dc-dc converter. Firstly, a three-terminal CM circuit model is presented to link a CM equivalent circuit of the dc-dc stage to the ac-ac stage. The model provides insight on how the CM noise will be generated from the dc-dc converter and interact with the ac-ac stage circuit. Secondly, based on the model, impacts on the noise generation and propagation path by the dc-dc stage have been analyzed. It is predicted that the dc-dc converter contributes to a large increase in the CM noise profile due to its additional noise generation and due to the multiple resonances associated with the battery cabinet. Especially, with a higher switching frequency of SiC devices, the emission from the dc-dc stage can be significant. Thirdly, a comparative evaluation of topologies and PWM schemes has been performed based on the proposed CM EMI model to set a mitigation strategy during a design phase. CMV generation by different combinations of topologies and PWM schemes has been compared for the ac-ac stage and the dc-dc stage. The result highlights that the selection of the topology and PWM scheme for the dc-dc stage plays a critical role in noise

mitigation from the UPS. A 20 kW full-SiC three-level UPS has been built with a SiC three-level module from MICROSEMI. The impact of the dc-dc converter and the mitigation strategy have been verified with the prototype UPS.

3.3 Formulation of the Three Terminal CM Model

In this section, the three terminal CM EMI model is developed to explain the CM EMI behavior of the UPS with a dc-dc converter. A structure of the UPS is shown in Fig. 3-3. A rectifier is connected to a 480V/ 60Hz grid and an inverter is connected to resistive ac loads. The dc-link voltage is 800 V nominal while the battery voltage is 540 V nominal. A dc-dc converter enables bidirectional power flow between the dc-link and the battery. The rectifier, inverter, and dc-dc converter share the dc-link as an energy buffer.

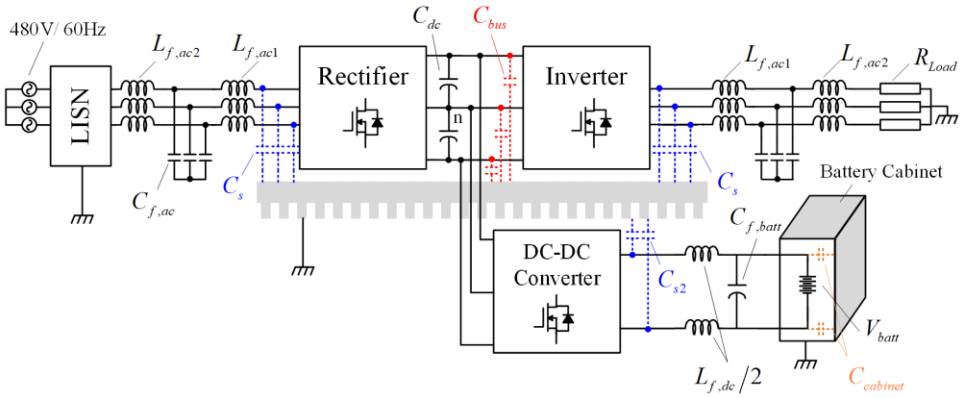


Fig. 3-3. Structure of UPS and parasitic capacitances to the earth.

For ac-side filters, LCL filters have been used for both the rectifier and inverter. A battery-side LC filter is designed to attenuate battery current ripple to 2% of rated current. A dc inductor is split in two and connected to each output port of the dc-dc converter to achieve complete symmetry and balancing for EMI purpose [99]. Heatsinks and a battery cabinet are

connected to the protective earth. The connections between the input-grid ground, protective earth, and the neutral of the three-phase output depend on the grounding scheme or system configuration. In this work, TT grounding is assumed where the three nodes are connected to the same conductive plane [100].

Parasitic capacitances to the earth are marked with dotted lines. These capacitances exist between the heatsink and the three-phase outputs of the rectifier, inverter $\left(C_s\right)$, dc bus $\left(C_{bus}\right)$, and two out ports of the dc-dc stage $\left(C_{s2}\right)$. On the battery side, a parasitic capacitance $\left(C_{cabinet}\right)$ exists between the metal cabinet and the battery terminal. Due to a large footprint of the battery, this capacitance value reaches an order of tens of nF [84]–[87].

3.3.1 Ac-ac stage modeling

The CM equivalent circuit for the ac-ac stage is shown in Fig. 3-4(a). Two inductors in the LCL filter are modeled as RLC branch as in Fig. 3-4(b). $C_{f,ac1}$ and $C_{f,ac2}$ model the equivalent parallel capacitors (EPC) of the inverter-side inductor and grid-side inductor, respectively. $R_{f,ac1}$ and $R_{f,ac2}$ model equivalent parallel resistors of the same. The values of parameters from the experimental setup are summarized in Chapter 3.6. The CMV of the rectifier and inverter can be defined as (3.1). $v_{xn,REC}$ refers to the voltage between the phase-*x* output $\left(x = a,b,c\right)$ of the rectifier and the mid-point of the dc-link. The CMV from the rectifier or inverter is modeled as a single voltage source referring to the mid-point of dc-link as Fig. 3-4(a).

$$v_{cm,REC} = \frac{v_{an,REC} + v_{bn,REC} + v_{cn,REC}}{3}$$
$$v_{cm,INV} = \frac{v_{an,INV} + v_{bn,INV} + v_{cn,INV}}{3} \tag{3.1}$$

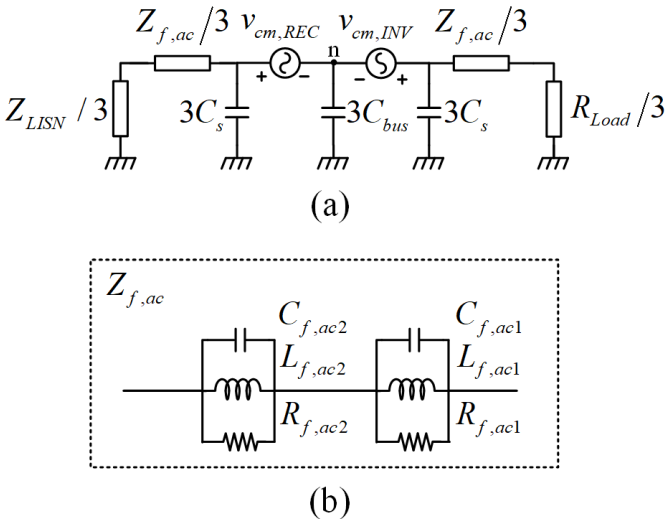


Fig. 3-4. (a) Ac-ac stage CM model, and (b) lumped parameter model for LCL filter.

In this configuration, CM current may propagate to the rectifier- and inverter-side or be shunted back through the parasitic capacitances (C_{bus}, C_s). In a relatively low-frequency range where the noise propagation through C_{bus} and C_s is not significant, most of the noise will flow between the rectifier- and inverter-side path and the CM noise emission will depend on $v_{cm,REC} - v_{cm,INV}$ [96]–[98], [101]. In the UPS application, the voltage reference of the rectifier input voltage and the inverter output voltage is largely determined by the required line voltage. Ideally, the input grid voltage to the UPS and the output voltage to the load are synchronized; however, a small phase difference may exist due to the voltage drop on the filters. Since the output voltages of the rectifier and the inverter are almost identical, the waveform of $v_{cm,REC}$

and $v_{cm,INV}$ will be very similar when the carriers for the rectifier and inverter are synchronized, and PWM schemes for both are identical [96], [101]. Most of the CMV generated from the rectifier and inverter cancel each other. As a result, the CM noise generation from the ac-ac stage alone is not significant.

To observe the effect in the frequency domain, the two-level rectifier and inverter were simulated using ideal switches. The switching frequency is set to 40 kHz and center-aligned Space Vector Pulse Width Modulation (SVPWM) has been used. The modulation index is 0.98 and the phase difference between the rectifier and inverter voltage is 1.5° due to the voltage drop across the LCL filter. A fixed-step simulation with 10 ns step was performed with PLECS. The waveforms of the CMV of the rectifier and the inverter were extracted from the simulation and subtracted to observe the cancellation effect on the frequency domain. The frequency spectrum of the CMV of the rectifier and the CMV of the ac-ac stage are plotted in Fig. 3-5(b) for a frequency range between 150 kHz and 2 MHz. With the presence of this cancellation, the spectrum of CMV has been reduced to 133 dB between 150 kHz – 2 MHz, which is a maximum 22 dB decrease when compared to the single two-level ac-dc converter case.

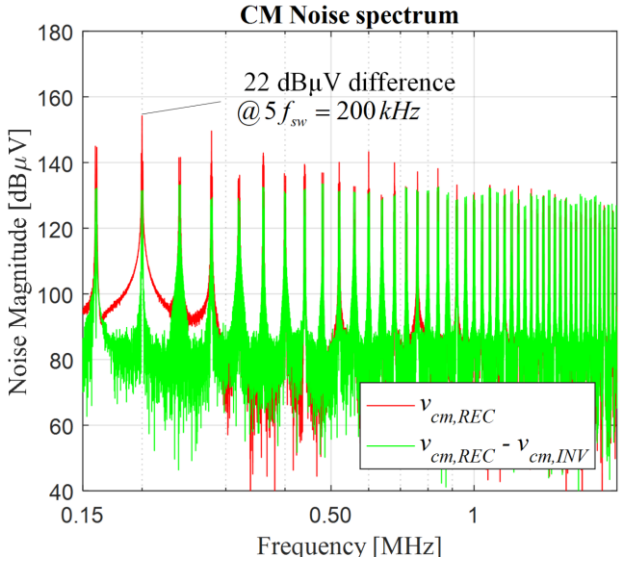


Fig. 3-5. Simulated frequency spectra for CM noise generation of two-level back-to-back converter.

3.3.2 Dc-dc stage modeling

In the UPS, the dc-dc converter connects energy storage to the dc-link of the rectifier and inverter. To link a CM equivalent circuit of the dc-dc stage to the ac-ac stage model, voltage potentials of the dc-dc converter output can be referred to the mid-point of the dc-link. The circuit for the dc-dc stage is shown in Fig. 3-6. The voltage potentials for a positive or negative terminal of the output referred to node *n* are labeled as $v_{dc+,n}(t)$ and $v_{dc-,n}(t)$. CMV output of the dc-dc converter $\left(v_{cm,DCDC}(t)\right)$ can be defined as (3.2).

$$v_{cm,DCDC}(t) = \frac{v_{dc+,n}(t) + v_{dc-,n}(t)}{2} \quad (3.2)$$

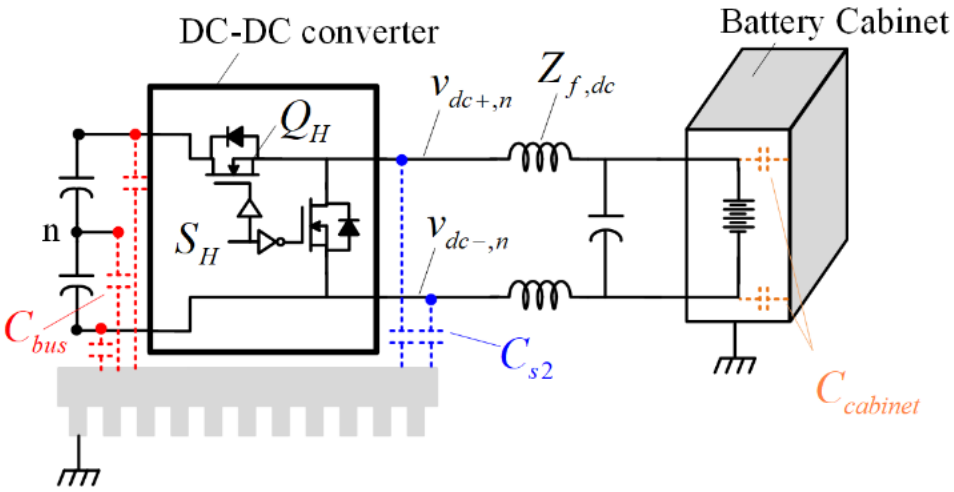


Fig. 3-6. Circuit of dc-dc stage.

The switching function of the high-side MOSFET (Q_H) is defined as $S_H(t)$. $S_H(t)$ equals 1 if Q_H is on, and 0 when Q_H is off as (3.3). When the dc-link voltage is equally split into the upper and lower dc-link capacitor, $v_{dc+,n}(t)$ and $v_{dc-,n}(t)$ can be written in terms of $S_H(t)$ as (3.4). Finally, $v_{cm,dcdc}(t)$ can mathematically be described by a switching state of the dc-dc converter as (3.5) for the noise source of the frequency-domain model. In the actual waveform, the dead time exists and its impact has to be counted.

$$S_H(t)=\begin{cases}1 & when\ \ Q_H\ is\ on\\ 0 & when\ \ Q_H\ is\ off\end{cases} \tag{3.3}$$

$$\begin{aligned} v_{dc+,n}(t) &= V_{dc}\left(S_H(t)-\frac{1}{2}\right)\\ v_{dc-,n}(t) &= -\frac{V_{dc}}{2}\end{aligned} \tag{3.4}$$

$$v_{cm,DCDC}(t)=\frac{v_{dc+,n}(t)+v_{dc-,n}(t)}{2}=\frac{V_{dc}}{2}\left(S_H(t)-1\right) \tag{3.5}$$

A CM equivalent circuit for the dc-dc stage is shown in Fig. 3-7. The CMV generated by the dc-dc converter in (3.5) serves as a voltage source in Fig. 3-7(a). The impedance of dc-side inductors $\left(Z_{f,dc}\right)$ is modeled as an inductor $\left(L_{f,dc}\right)$ with EPC $\left(C_{f,dc}\right)$, and an equivalent parallel resistor $\left(R_{f,dc}\right)$. The battery cabinet is modeled as a series-connected LC circuit. Parasitic inductance of the metal plate of the cabinet connected to the earth is modeled by $L_{cabinet}$. The parasitic capacitance between the terminal of the battery-rack to the metal casing is modeled as $C_{cabinet}$. The impedance between the output terminals of the dc-dc converter to the ground $\left(Z_{eq,DCDC}\right)$ is a series-connection of $Z_{f,dc}/2$ and the impedance of the metal casing which will decide the propagation through the battery-side.

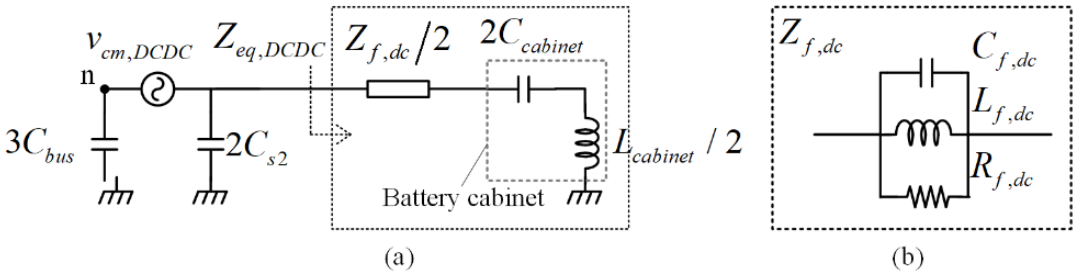


Fig. 3-7. (a) Dc-dc stage CM model, and (b) lumped parameter model for the dc-side inductor.

To observe the noise generation from the dc-dc stage, the two-level bidirectional dc-dc converter was simulated. The duty ratio was 0.625 and the switching frequency was set to 40 kHz. The dead time was not included in the simulation. A fixed-step simulation with 10 ns step

was performed. Waveforms of the switching state and the CMV are shown in Fig. 3-8(a). A magnitude of the CMV step change is $V_{dc}/2$, which is 50% larger than the two-level ac-dc converter case. The frequency spectrum of $v_{cm,DCDC}$ was extracted from the time-domain waveform. To compare the noise generation, the frequency spectrum of the noise sources ($v_{cm,DCDC}$, and $v_{cm,REC}-v_{cm,INV}$ from Fig. 3-5) are compared in Fig. 3-8(b). With the presence of the CMV cancellation in the ac-ac stage, the two-level dc-dc converter generates around 20 dB larger CM noise at 160 kHz. Also, the noise envelope over 5 MHz or higher shows a 10 dB larger magnitude compared to that of the ac-ac stage.

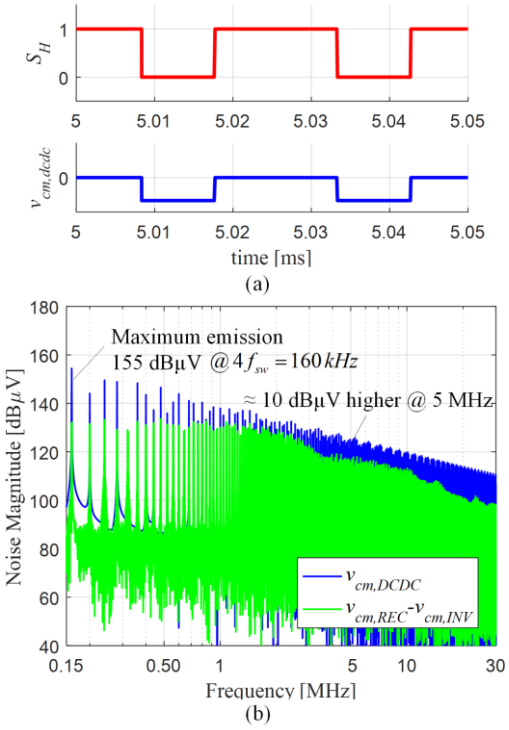


Fig. 3-8. Simulation for CM voltage by two-level dc-dc converter:
(a) time domain waveform, and (b) frequency spectra.

3.3.3 Modeling of UPS for CM EMI

By combining the CM circuit model for the ac-ac stage and dc-dc stage, the complete UPS model is derived as shown in Fig. 3-9. The model provides insight into how CM noise will change when the dc-dc converter operates. CM current from each noise sources will be divided according to the impedance of possible paths at the frequency of the interest which includes the parasitic capacitances C_s, C_{s2}, and C_{bus}. Note that the CM EMI filters are not considered in the model which may largely impact the impedance of noise path and thus propagations. This work's focus is on the analysis of how the dc-dc stage may impact noise phenomena and the minimization of generated noise by the selection of topology and PWM schemes.

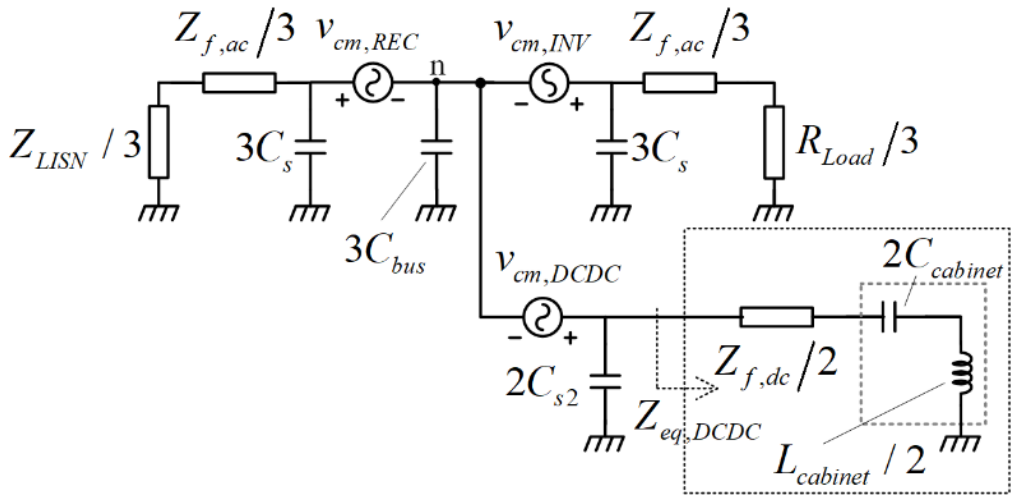


Fig. 3-9. CM EMI model of UPS and noise propagation paths to LISN.

3.4 EMI Analysis of the DC-DC Converter Side Based on the Model

3.4.1 Impact of the dc-dc converter operation on the noise generation

As seen in the frequency spectrum of Fig. 3-8, the CM noise generated by the dc-dc converter is large compared to that of the ac-ac stage. Also, because of the difference in the circuit topology and principle of the switchings between dc-dc stage and ac-dc stage, the time domain waveform of $v_{cm,DCDC}$ is quite different from $v_{cm,REC}$ or $v_{cm,INV}$. It is hard to expect partial cancellation similar to the one between the rectifier and inverter even when the carriers of three stages are synchronized. Therefore, the dc-dc converter switching may inject significant CM noise through the battery cabinet to the earth when the UPS is in battery charging mode or double-conversion (ac-to-ac conversion) with battery charging.

3.4.2 Impact of the dc-dc converter operation on the noise propagation path

When the dc-dc converter operates, the CM noise generated by the rectifier, inverter, and dc-dc converter propagates through the battery cabinet to a ground. Within this path, the parasitic components of the battery cabinet are present and create resonances with the dc inductor. Together with additional CMV generation, these resonances deteriorate the CM noise profile.

The impedances of the dc inductors, and between the battery terminals to the ground were measured using an Agilent 4292A impedance analyzer. A resistor bank with a metal housing shown in Fig. 3-2(b) was used to emulate the battery rack. Capacitors are added between the two terminals and the metal housing to match the parameters of the battery rack in [86]. The

final parameters were estimated based on the curve fitting results shown in Fig. 3-10 and are summarized in Table 3-3. From the extracted parameters, the impedance between the output terminals of the dc-dc converter to the ground $\left(Z_{eq,DCDC}\right)$, as described by (3.6), is shown in Fig. 3-11. Three resonance frequencies exist and each of them is labeled as $f_{res,dc1}$, $f_{res,dc2}$, and $f_{res,dc3}$. Note that a shunt path through the parasitic capacitance $\left(C_{s2}\right)$ is neglected in (3.6).

$$Z_{eq,DCDC} = s\frac{L_{f,dc}}{2} \| \frac{1}{s2C_{f,dc}} \| \frac{R_{f,dc}}{2} + s\frac{L_{cabinet}}{2} + \frac{1}{s2C_{cabinet}} \tag{3.6}$$

Table 3-3. Parameters for dc-dc converter side impedances

Parameter	Value
$L_{f,dc}$	253 μH
$C_{f,dc}$	64.3 pF
$R_{f,dc}$	40 kΩ
$L_{cabinet}$	660 nH
$C_{cabinet}$	10 nF

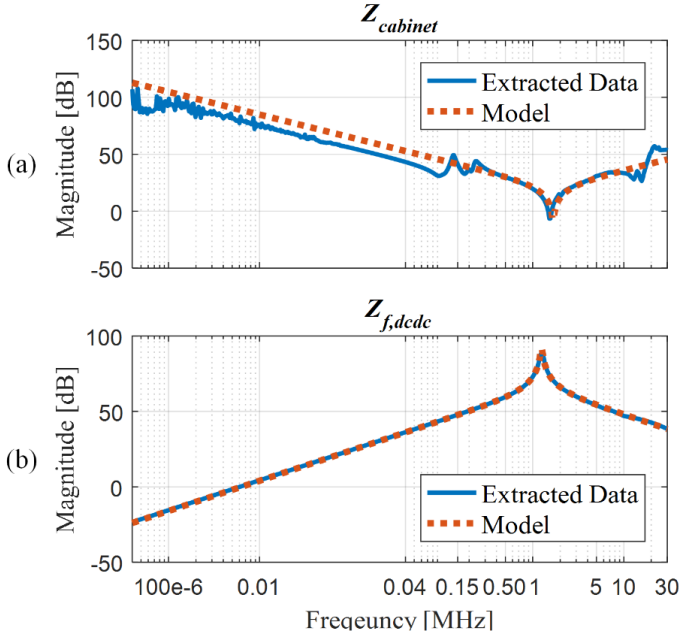


Fig. 3-10. Impedance measurement and model fitting results: (a) battery-terminal to earth, and (b) dc-inductor.

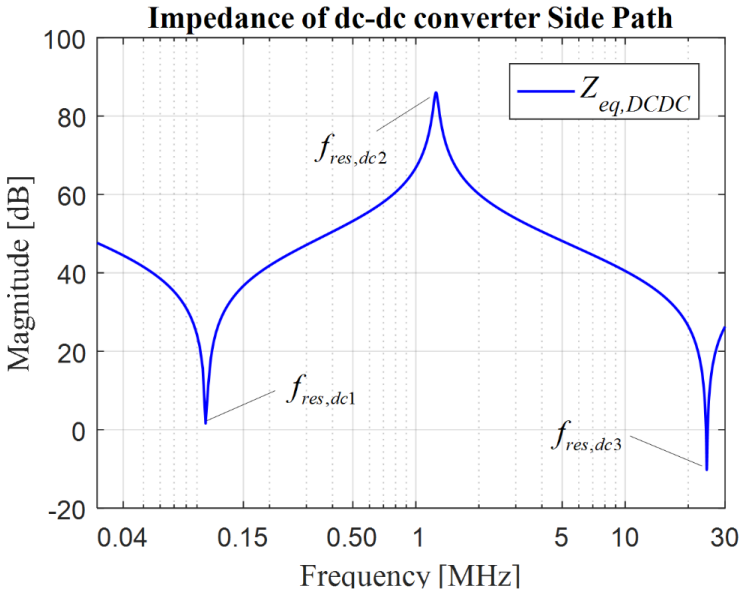


Fig. 3-11. Bode plot for impedance between output terminals of the dc-dc converter to the earth $\left(Z_{eq,DCDC}\right)$.

The first resonant frequency $\left(f_{res,dc1}\right)$ results from the resonance between $L_{f,dc}$ and $C_{cabinet}$. The value of the dc-side inductor$\left(L_{f,dc}\right)$ is relatively large in general to meet a strict high-frequency current ripple constraint for the battery. As $C_{cabinet}$ reaches nF order, $f_{res,dc1}$ as (3.7) can be located within the range of hundreds of kHz.

$$f_{res,dc1} = \frac{1}{2\pi\sqrt{\left(L_{f,dc} + L_{cabinet}\right)C_{cabinet}}} \approx \frac{1}{2\pi\sqrt{L_{f,dc}C_{cabinet}}} \tag{3.7}$$

To illustrate this resonance effect at this relatively low-frequency range, the transfer functions for the CMV of the rectifier, inverter, and dc-dc converter versus the voltage across the line impedance stabilization network (LISN) ($v_{LISN}/v_{cm,REC}$, $v_{LISN}/v_{cm,INV}$, $v_{LISN}/v_{cm,DCDC}$) have been derived when the operation mode is double-conversion with battery charging. The design of the EMI filters may seek to meet the noise limits at this low-frequency range, therefore the change that dc-dc stage brings will significantly affect their design. Note, at this frequency range, the impedance of C_{BUS}, C_s , and C_{s2} is much higher than that of the ac- and dc-side filters with the given parameters in Table 3-7. Therefore, most of the noise propagates through the filters and interaction between the three power stages may be significant for CM noise which is a unique characteristic of UPS compared to a single three-phase inverter or dc-dc converter. Self-resonant frequencies of the filters are located over 1 MHz, and the filters show inductive behavior. Under such conditions, a simplified CM equivalent circuit is shown in Fig. 3-12 without any EMI filter. $v_{LISN}/v_{cm,REC}$, $v_{LISN}/v_{cm,INV}$, and $v_{LISN}/v_{cm,DCDC}$ are plotted in Fig. 3-13 for $C_{cabinet}$ = 1 nF, 10 nF, and 30 nF cases. Depending on the $C_{cabinet}$

value, $f_{res,dc1}$ can be located within 150–500 kHz range like the 1 nF case in Fig. 3-13. Near $f_{res,dc1}$, the three transfer functions show high peaking, and the impact of the CMV from the dc-dc converter is higher than in the other two cases. Even after this resonant frequency, only around 5 dB difference exists between $v_{LISN}/v_{cm,REC}$, $v_{LISN}/v_{cm,INV}$, and $v_{LISN}/v_{cm,DCDC}$, which demonstrates the significant noise emission coming from the dc-dc converter.

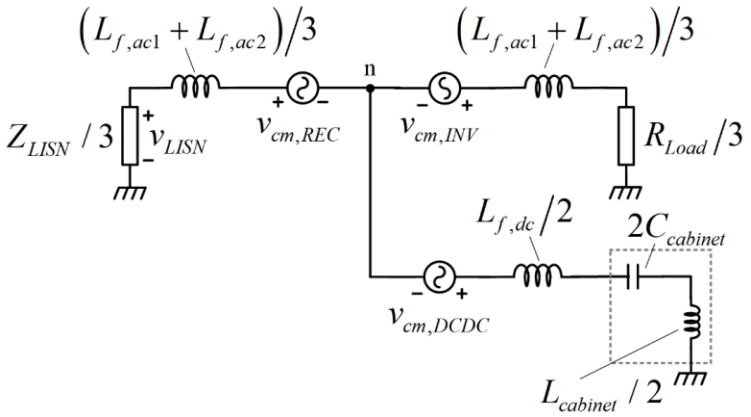


Fig. 3-12. A simplified CM model for a relatively low frequency range.

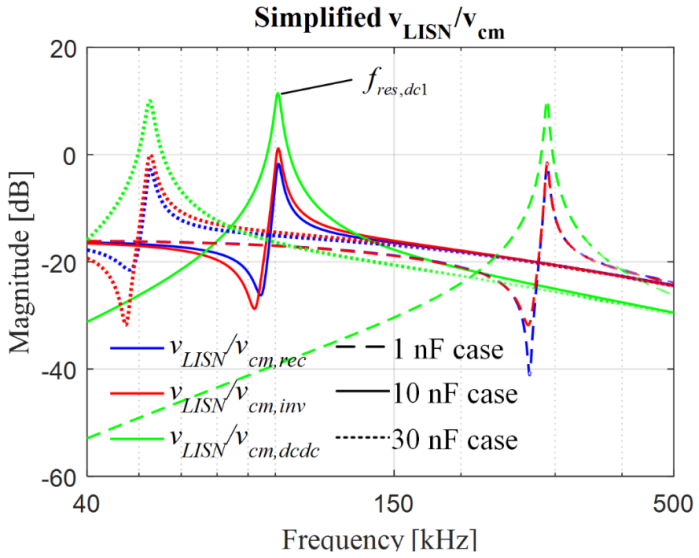


Fig. 3-13. Transfer function from CMV of each stage to LISN voltage in frequency range of 40 – 500 kHz depending on $C_{cabinet}$.

The second resonance $\left(f_{res,dc2}\right)$ at MHz range results from a self-resonant frequency of the dc-inductor as indicated in (3.8). Above this frequency, the dc-inductor starts to show a capacitive behavior. Since the equivalent parallel capacitance (EPC) of the dc-inductor is much smaller than $C_{cabinet}$, the impedance of $Z_{eq,DCDC}$ is largely determined by the EPC.

$$f_{res,dc2} = \frac{1}{2\pi\sqrt{L_{f,dc}C_{f,dc}}} \approx 1.25\,MHz \tag{3.8}$$

Lastly, the parasitic inductance of the battery cabinet resonates with the EPC of dc-inductor over a very high-frequency range, as indicated in (3.9). Due to its large size, the metal cabinet presents parasitic inductance of hundreds of nano-henry (nH) to earth. These two small parasitic components resonate and bring a large increase in the EMI spectrum over 10–30 MHz. It is important to note that the frequency range is nearly as high as the radio-frequency band

according to the given parameters, and accuracy of the lumped parameter model is poor. The exact location of $f_{res,dc3}$ is influenced by the physical geometry of the battery rack and the metal housing.

$$f_{res,dc3} = \frac{1}{2\pi\sqrt{L_{cabinet} C_{f,dc}}} \approx 24\,MHz \tag{3.9}$$

The three-terminal CM model of Fig. 3-9 is simulated with PLECS to observe the impact of the dc-dc converter operation, and to compare the CM noise spectra. Firstly, CMV waveforms from the rectifier, inverter, and dc-dc converter were extracted from the full circuit simulation and used for the voltage sources in the CM equivalent circuit. Three-level Neutral Point Clamped (NPC) converters with SVPWM have been used for the ac-ac stage and a three-level bi-directional dc-dc converter has been used for the dc-dc stage as shown in Fig. 3-18(b). Dead-time is not included in the simulation. To avoid excessive computational effort, a PLECS with ideal devices was used. A fixed step simulation with 10 ns step is used. Minimal resistance below 1 $\mu\Omega$ is added between each voltage sources in Fig. 3-9, and $3C_s$ to prevent a short-circuit between two voltage sources and to ensure convergence of the simulation. The parameters used in the simulation are given in Table 3-7.

For the double-conversion mode, and double-conversion with battery charging, the voltages across LISN are measured and the frequency spectrum of LISN voltage are compared in Fig. 3-14. Compared to the double-conversion mode, there is more than a 10 dB increase in the CM noise over a wide frequency range when the dc-dc converter operates. Near $f_{res,dc1}$ and $f_{res,dc3}$, the simulation result shows a large increase due to the resonance.

The same simulation has been performed for two different $C_{cabinet}$ values; 0.7 nF and 10 nF, to observe the impact of the resonance on the dc-side path. The capacitor values are chosen from an experimental setup in Fig. 3-2(b). The result is shown in Fig. 3-15 when the operating mode is in double-conversion with battery charging. A shift of $f_{res,dc1}$ brings a large variation on the magnitude of harmonics up to 500 kHz. This is important since required attenuation by the EMI filter and the size of the EMI filter will be affected accordingly. After 500 kHz, the overall spectrum remains the same. Because the standards such as IEC62040-2 require that the limitation on conductive EMI should be met in the worst case among different operating modes, this deterioration of the CM EMI by the dc-dc converter operation should be considered for overall EMI mitigation and EMI filter design.

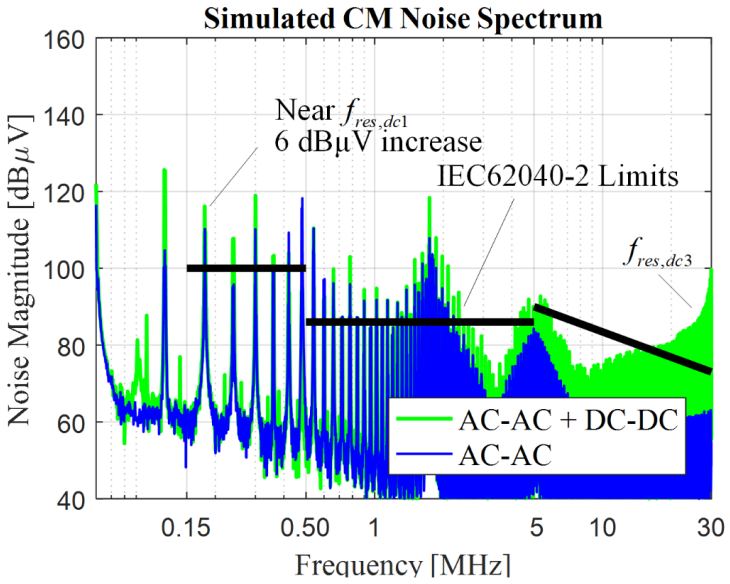


Fig. 3-14. Simulated CM EMI spectrum depending operation of dc-dc converter.

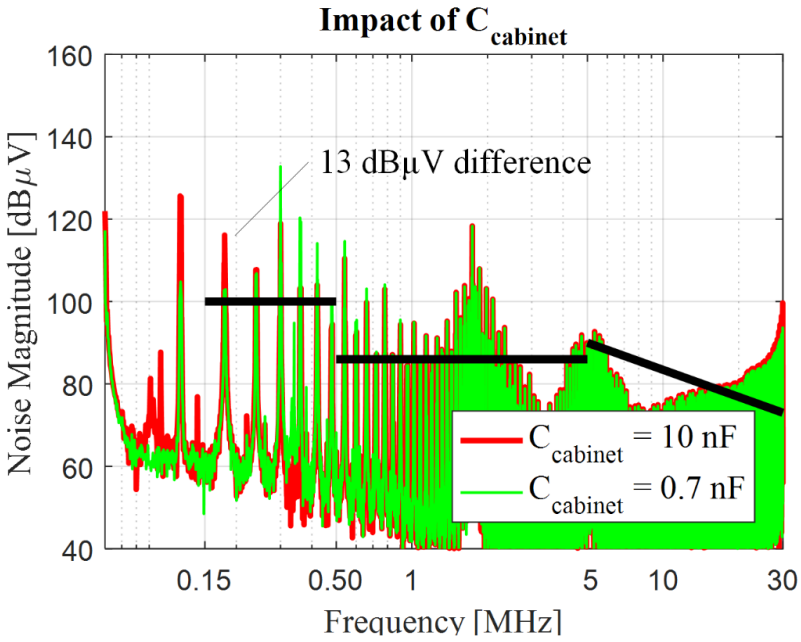


Fig. 3-15. Simulated CM EMI spectrum depending the value of $C_{cabinet}$.

3.5 Topology and PWM Scheme Selection

In this section, an EMI mitigation strategy for UPS is investigated based on the model developed in Section 3.3.3. Frequency spectra of CMV generated from different combinations of topologies and PWM schemes are compared based using simulations of the ac-ac stage and dc-dc stage. Assuming this comparative evaluation is performed during the design phase, ideal switches have been used for the simulation. The dead time and associated influence are not considered. Special attention is given to the selection of the dc-dc converter to minimize its impact on the CM EMI emissions.

3.5.1 Ac-ac stage

When both the rectifier and inverter are operated, most of the CMV generated by the rectifier and inverter cancel each other out as shown in Section 3.3.1. Nevertheless, the CMV of the single ac-dc stage also has to be minimized since this cancelation does not exist depending on the mode of operation, for example, battery charging mode. Therefore, a comparison is made for a single ac-dc converter case. A two-level ac-dc converter is used as a benchmark and, a three-level topology is also considered for topology candidates. Three different PWM schemes for the two cases are compared to find a combination with the least amount of CM noise generation. Only modulation schemes capable of a modulation index range up to 1.15 are considered since the operation of UPS had to be assured under input-voltage variation of –30% to +15%. Additionally, the schemes with the center-aligned carrier are considered, as to not significantly worsen the harmonic quality of DM voltage output.

For the two-level case, SVPWM, Active Zero State PWM1 (AZSPWM1) [102] and Near State PWM (NSPWM) [103] are compared. For the three-level case, SVPWM, reduced CMV (RCMV) PWM [104], and LMZVM [105] are compared. Based on loss simulation results to achieve 99% efficiency, the switching frequency has been chosen as 40 kHz for the two-level case, and 60 kHz for the three-level case. As EMI regulations such as IEC62040-2 specify the limits for conductive EMI starting from 150 kHz, the harmonics from $3f_{sw}$ or $4f_{sw}$, and higher will be located within the limit.

Time domain waveforms of the PWM schemes are shown in Fig. 3-16 and Fig. 3-17. Due to the clamping nature similar to that of DPWM, the switching frequency for two-level NSPWM and three-level RCMV PWM is set to 1.5 times larger than the other PWM schemes. CMV patterns for the PWM schemes and the frequency spectra are compared in Fig. 3-16 and Fig. 3-17. The CM EMI filter should be designed to attenuate critical harmonic within a range of 150 – 500 kHz to meet the standard. A 40dB/dec dotted line which indicates attenuation by a single stage LC filter is drawn and used to compare PWM schemes in terms of noise mitigation. The critical CM harmonics are summarized in Table 3-4.

The results for the two-level PWM schemes are shown in Fig. 3-16. Although AZSPWM1 can suppress significant amounts of CMV at f_{sw} compared to the SVPWM case, the critical CM harmonic at 200 kHz does not decrease. For NSPWM, the $3f_{sw}$ component lies on 180 kHz, and its magnitude is similar to the other two cases. In summary, in a given operating condition, NSPWM and AZSPWM1 for the two-level case could not bring much benefit to the critical CM harmonics between 150 kHz – 500 kHz.

The cases for a three-level ac-dc converter are shown in Fig. 3-17. The critical CM harmonic at 180 kHz in both LMZVM and RCMV PWM case is 15 dB smaller than the SVPWM case. Also, compared to two-level cases, the required attenuation could be 12 dB lower in the three-level case, which will result in smaller CM EMI filter. Another important consideration for three-level converters is the capability of neutral point voltage balancing between two dc-links. LMZVM provides good control of neutral point voltage and therefore the three-level topology with LMZVM is finally selected for the rectifier and inverter implementation.

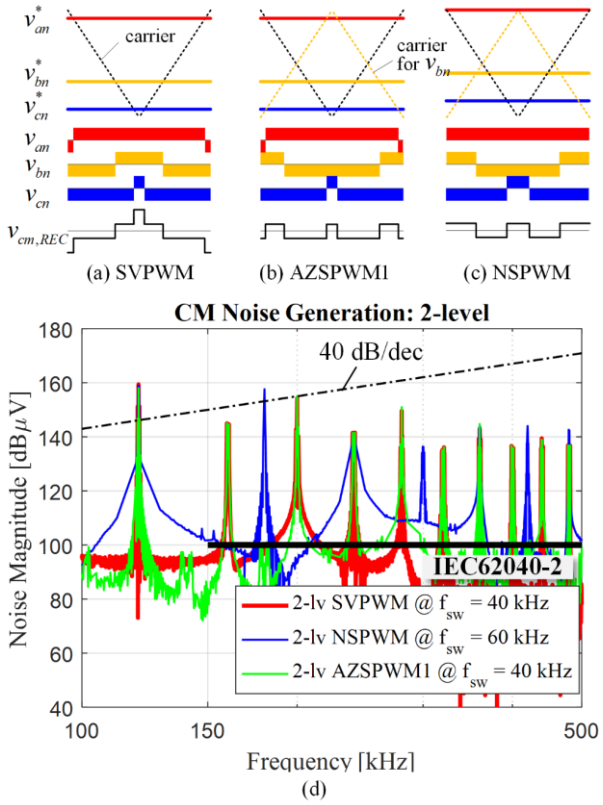


Fig. 3-16. Example of switching pattern for two-level PWM schemes when $v^*_{as} > v^*_{bs} > v^*_{cs}$ (a) SVPWM, (b) AZSPWM1, (c) NSPWM, and (d) comparison of CMV on the frequency spectra.

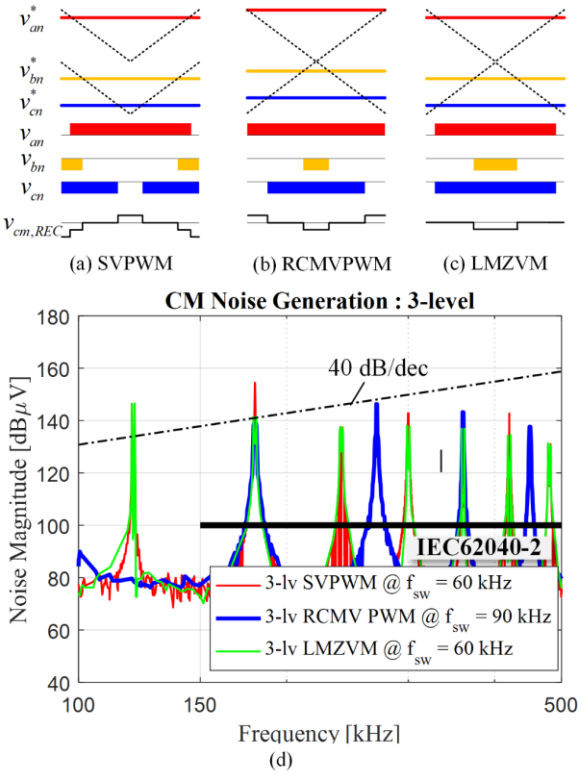


Fig. 3-17. Example of switching pattern for three-level PWM schemes when $v_{as}^* > v_{bs}^* > v_{cs}^*$ (a) SVPWM, (b) RCMVPWM, (c) LMZVM, and (d) comparison of CMV on the frequency spectra.

Table 3-4. CM emission of different PWM schemes.

Topology for ac-dc stage	PWM scheme	Critical CM harmonic for EMI filter design
two-level	SVPWM	155 dBμV at 200 kHz
	NSPWM	158 dBμV at 180 kHz
	AZSPWM1	155 dBμV at 200 kHz
three-level	SVPWM	155 dBμV at 180 kHz
	RCMVPWM	139 dBμV at 180 kHz
	LMZVM	141 dBμV at 180 kHz

3.5.2 Dc-dc stage

In section 3.3.2, it was shown that CMV emission from the dc-dc converter itself can be much larger than the one of the ac-ac stage. Therefore, the selection of the dc-dc stage topology

and its PWM scheme may play a critical role in EMI mitigation. In this work, only non-isolated topologies are considered, with the bi-directional two-level dc-dc converter shown in Fig. 3-18(a) acting as a benchmark.

A three-level bidirectional dc-dc converter as shown in Fig. 3-18(b) was adopted by researchers for high-voltage high-power applications [106]–[108]. With additional voltage-levels, the three-level dc-dc converter reduces the size of the dc inductor. Also, if the NPC three-level topology is used to build three-level phase legs for the ac-ac stage, the dc-dc stage can share the same phase leg and benefits on manufacturability while two diodes across $v_{dc+,n}$ and $v_{dc-,n}$ can be excluded [109]. To avoid shoot-through, two upper-side MOSFETs (Q_1, Q_2) and lower-side MOSFETs (Q_3, Q_4) switch complementarily. The switching states of MOSFET Q_1 and Q_4 are defined as S_H and S_L, respectively. Assuming a balanced dc-link voltage, the output voltage $\left(v_{out,DCDC,3lv}\right)$ and CMV $\left(v_{cm,DCDC,3lv}\right)$ of the three-level dc-dc converter can be described by (3.10).

$$\begin{aligned} v_{out,DCDC,3lv} &= v_{dc+,n} - v_{dc-,n} = \frac{V_{dc}}{2}\left(S_H + S_L\right) \\ v_{cm,DCDC,3lv} &= \frac{1}{2}\left(v_{dc+,n} + v_{dc-,n}\right) = \frac{V_{dc}}{4}\left(S_H - S_L\right) \end{aligned} \tag{3.10}$$

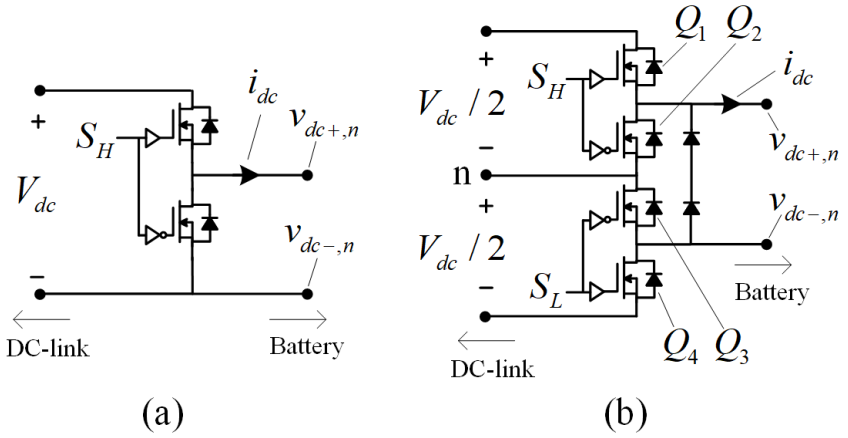


Fig. 3-18. Candidates for dc-dc topology (a) two-level bi-directional dc-dc converter, and (b) three-level bi-directional dc-dc converter based on the NPC phase leg.

There are two switching states governing the output voltage, and different PWM schemes can be used to decide a switching sequence. In [106]–[108], the carriers for S_H and S_L are 180° phase-shifted. Waveforms for CMV and dc-inductor current (i_{dc}) are shown in Fig. 3-19(a). With the same switching frequency, the current ripple can be reduced to a quarter of the current ripple in the two-level dc-dc converter. However, a CMV pulse of $V_{dc}/4$ is generated when either S_H or S_L turns on. The frequency spectrum of the CMV is compared with the two-level case in Fig. 3-20. The CM emission for the three-level interleaved case is very similar to the two-level dc-dc converter case. The difference in the envelope is only 3 dB.

In the second case, two carriers are synchronized so that S_H and S_L always simultaneously switch. The waveforms are shown in Fig. 3-19(b), respectively. Compared to the two-level case shown in Fig. 3-18(a), no benefit exists on the current ripple of i_{dc}. On the other hand, the output CMV $\left(v_{cm,DCDC,3lv}\right)$ always remains zero in the ideal condition. Therefore, the CM noise

emission from the dc-dc converter can be minimized. The high switching frequency of SiC devices can compensate for the increased current ripple.

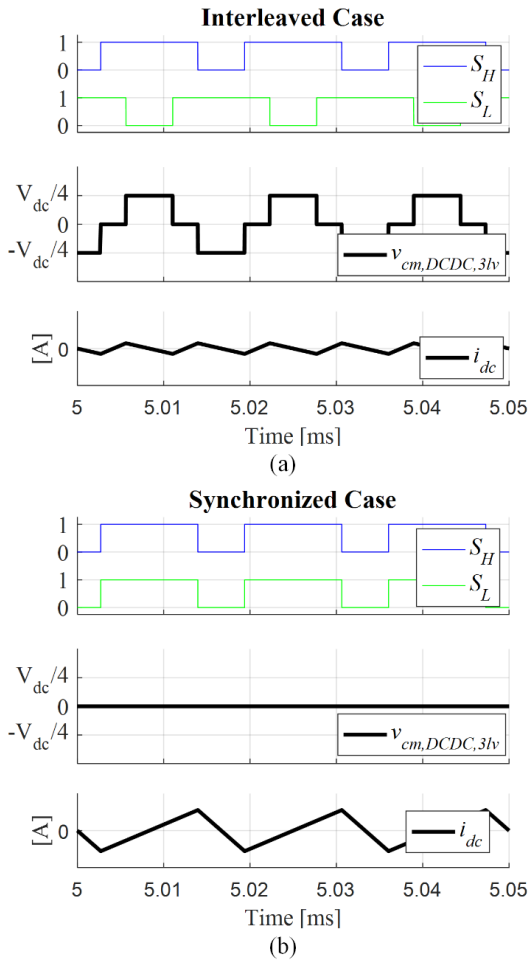


Fig. 3-19. Switching patterns and waveforms for three-level dc-dc converter with (a) interleaved carriers, and (b) synchronized carriers.

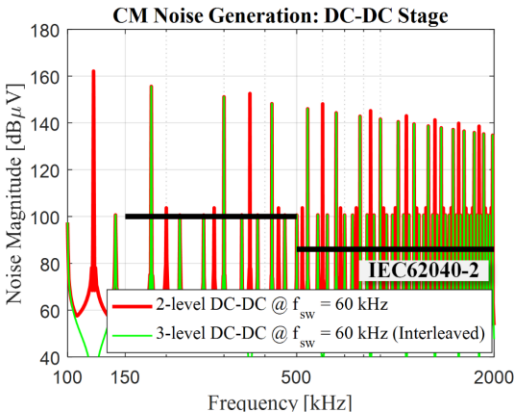


Fig. 3-20. Comparison on CM noise generation for the dc-dc stage.

Based on the comparison, the three-level bi-directional dc-dc converter with a synchronized switching sequence of Q_1 and Q_4 has been selected for the dc-dc stage. In ideal conditions, the CM emission from the dc-dc converter can be eliminated with this combination. Also, it provides good manufacturability by sharing the same NPC phase leg with the ac-ac stage circuit. The final circuit diagram of the UPS is shown in Fig. 3-21. Note that the EMI filter is not included in Fig. 3-21. The EMI containment strategy with choice of optimal filter topology and design of the EMI filter is not covered in this chapter.

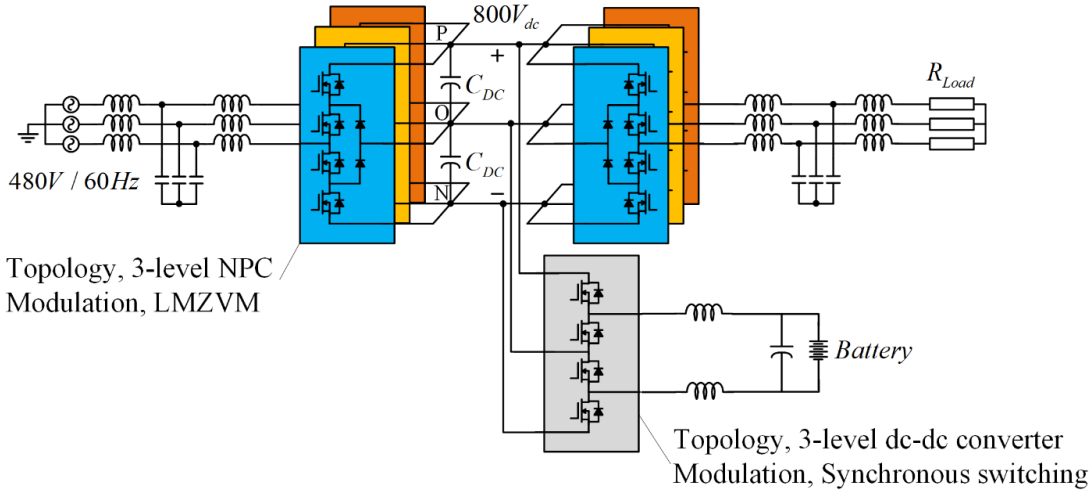


Fig. 3-21. Circuit diagram for a full-SiC UPS with three-level ac-ac stage and three-level dc-dc stage.

3.6 Experimental Results

A 20 kW full-SiC UPS has been built to verify the impact of dc-dc converter operation and the mitigation strategy. 1.2 kV 40 A full-SiC NPC modules (APTMC60TLM55CT3AG from MICROCHIP) were used to build the three-level ac-ac stage. The same module has been utilized to build the three-level dc-dc converter as shown in Fig. 3-18(c). Detailed design of the gate driver and testing procedure are included in Chapter 5.3 and Appendix.A. The external gate resistor is 0.05 Ω for both turn-on and turn-off instant. A double pulse test result for the ac-ac stage phase leg is shown in Fig. 3-22. The SiC MOSFETs switches around $25\,V/ns$. The switching frequency for both the ac-ac stage and dc-dc stage is set to 60 kHz.

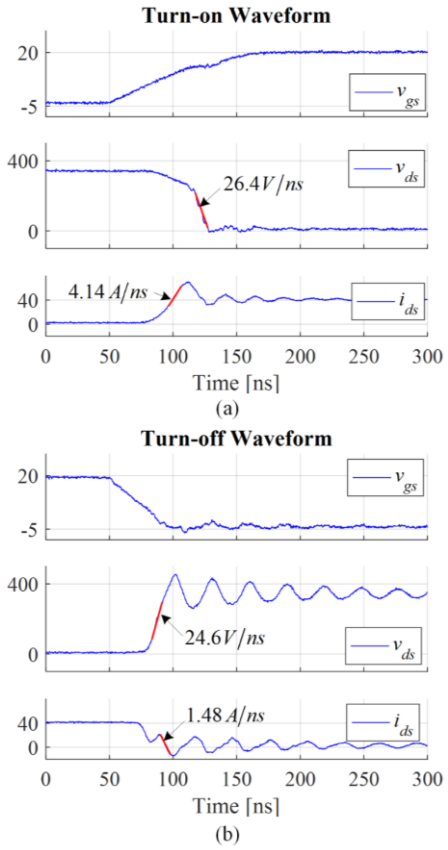


Fig. 3-22. Double pulse test results for *dv/dt*, *di/dt*: (a) Turn-on instant, and (b) Turn-off instant.

Before assembly of every filter component, module, and busbar, the impedance of each has been measured with the Agilent 4294A precision impedance analyzer. C_s and C_{s2} are measured following the method in [110]. The parasitic couplings between the components and impedances of interconnections are not measured. The parameters for the UPS are shown in Table 3-7. An experimental setup with the LISN is shown in Fig. 3-2. To emulate the battery-rack, a 22 Ω, a 12 kW resistor bank with a metal housing is used. Multiple resistors are series- and parallel-connected inside the resistor bank. The metal housing is grounded to a large copper sheet, which serves as the reference ground for the LISNs. Two terminals of the dc load bank are floating and a parasitic capacitance between two input terminals of the resistor bank and

metal housing is measured as 0.7 nF. To emulate a large parasitic capacitance of the battery rack, two 10 nF capacitors are added connecting the two input terminals to the metal housing. The resulting impedance between the terminal and the earth is shown in Fig. 3-10(a). The connection between the two dc inductors and the terminals of the dc load is made with short cables to eliminate the effect from them. MX45 from California Instrument is used for the input-grid and 50 μH LISNs are connected between the input grid and the rectifier as Fig. 3-3. Three LISNs are connected to 20 dB attenuators and the voltage-drops across LISNs are simultaneously measured with a multichannel digital oscilloscope (Tektronix MSO5104). 100 mega-samplings per second(MS/s) is used and the measured data is logged and post-processed offline to extract the DM and CM components. The output of the inverter is connected to 12 Ω three-phase resistor banks with 8 m long three-phase four-wire cables.

An experimental test is designed to verify two aspects. The first goal is to verify the relative deterioration in the CM EMI with respect to the dc-dc converter operation. The CM EMI spectra for the double conversion mode and double conversion with battery charging mode have been compared. The second goal is to verify the mitigation by the topology and PWM scheme selection which was predicted by the model during the design phase. In case I, SVPWM is used for the ac-ac stage and two carriers for the three-level dc-dc converter is interleaved. In case II, the PWM scheme for the ac-ac stage is changed to LMZVM. In case III, the synchronous switching is used for the dc-dc stage. The CM EMI spectrum for three cases in Table 3-5 is measured.

Table 3-5. Three cases for CM noise comparison.

Case	Ac-dc stage		Dc-dc stage	
	Topology	PWM scheme	Topology	PWM scheme
I	three-level NPC	SVPWM	three-level dc-dc	Interleaved
II	three-level NPC	LMZVM	three-level dc-dc	Interleaved
III	three-level NPC	LMZVM	three-level dc-dc	Synchronized

First, the CM noise spectra for two different modes of operation are compared to observe the impact of the dc-dc converter. In the first measurement, only the ac-ac stage is operated at 20 kW full power, and the dc-dc converter was turned off. In the second measurement, 18 kW was transferred to the ac loads through the inverter and 2 kW fed the dc load by the dc-dc converter. Following the case I in Table 3-5, SVPWM has been used for the ac-ac stage and the two carriers for three-level dc-dc converter are interleaved.

The comparison of the CM noise for two different modes of operation is shown in Fig. 3-23. With the dc-dc converter operation, the CM harmonic component at 180 kHz is increased by 6.8 dB. This is critical for the EMI filter design since the corner frequency of the EMI filter will be mainly determined by this component. Over 1–2 MHz, the CM noise has been increased by a maximum of 12.5 dB. Over 2–30 MHz, a high increase in the CM noise was observed, which does not exist in the double-conversion mode.

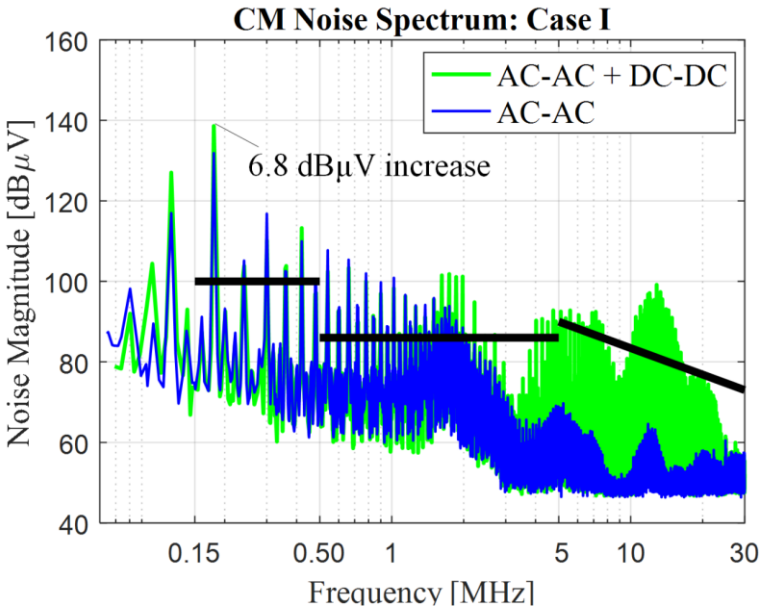


Fig. 3-23. Experimental results for CM EMI depending on the modes of operation.

To verify the impact of parasitic components of the battery cabinet, the additional 10 nF capacitors are removed and the UPS is tested in the same condition when $C_{cabinet}$ is 0.7 nF. According to the calculation, $f_{res,dc1}$ shifts from 100 kHz to 380 kHz. The experimental result is shown in Fig. 3-24 and the variation within 120 – 480 kHz is summarized in Table 3-6. The shift of $f_{res,dc1}$ reduces the magnitude of 120 kHz and 180 kHz more than 15 dB. On the other hand, the component at 420 kHz has increased. From 700 kHz to 10 MHz, the two cases show a similar noise envelope. Therefore, the location of this resonance frequency may largely influence the emission between 150–500 kHz, and should be considered during the design phase.

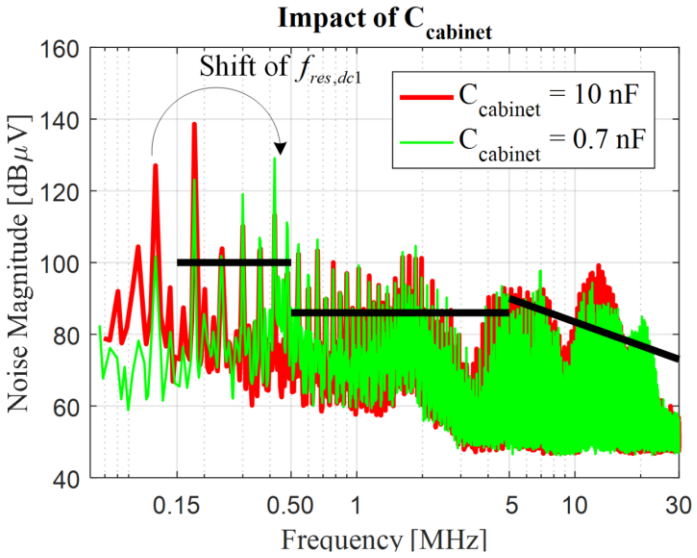


Fig. 3-24. Experimental results for CM EMI depending on the value of $C_{cabinet}$.

Table 3-6. Variation of noise magnitude between 100 – 500 kHz range due to the shift of $f_{res,dc1}$.

Frequency	10 nF case [dBμV]	0.7 nF case [dBμV]	Variation [dBμV]
120 kHz	127	102	-25
180 kHz	139	123	-16
240 kHz	104	102	-2
300 kHz	110	119	+9
360 kHz	104	107	+3
420 kHz	113	130	+17
480 kHz	97	110	-13

Second, the frequency spectra of the three different cases in Table 3-5 were measured to verify the EMI mitigation strategy. $C_{cabinet}$ is set back to 10 nF. The results for double-conversion with battery charging mode are shown in Fig. 3-25. The impact of the PWM scheme of the ac-ac stage is observed in case I and II. Most of the CMV is cancelled between the rectifier and the inverter, and changing the PWM schemes for the ac-ac stage provides a small reduction of the CM EMI. The experimental result shows that only a few dB decrease at 180

kHz and the noise at the high-frequency range does not show a significant change. By comparison of cases II and III, the impact of the dc-dc converter can be observed. In tge case III, the CM emission from the dc-dc converter is minimal and the critical harmonic for the EMI filter design at 180 kHz is reduced by 16 dB. The CM noise from 400 kHz to 10 MHz range also has been decreased by up to 14 dB.

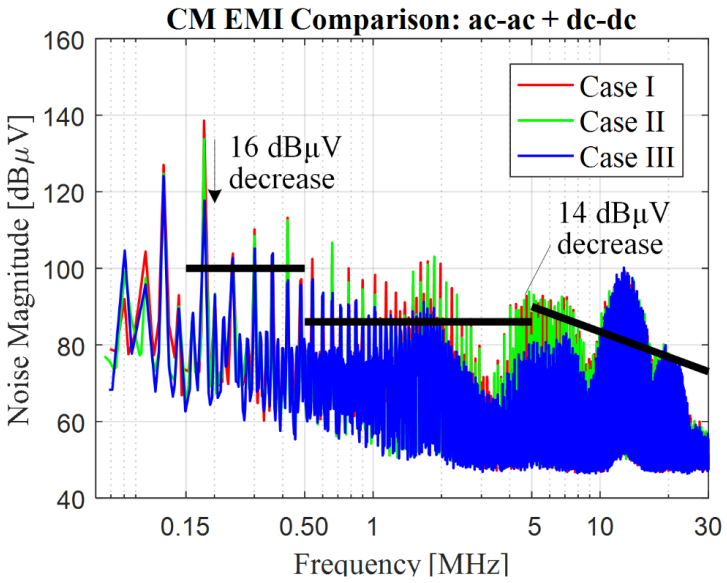


Fig. 3-25. Experimental results for CM EMI depending on the PWM schemes of the ac-ac stage and dc-dc stage in double-conversion and battery charging mode.

The case for battery charging mode is shown in Fig. 3-26. In this mode, subtraction of $v_{cm,REC}$ and $v_{cm,DCDC}$ will be the main noise source within the relatively low frequency range wherein the shunt path through the C_{bus}, C_s, and C_{s2} can be ignored. To simplify the analysis, the PWM scheme for the dc-dc stage is changed first to a synchronized one, eliminating the interaction between the two noise sources. When compared to the case I, it can be observed that noise generation from the dc-dc stage significantly impacts the emission, especially over 1 MHz frequency range. By comparing the green line and case III, the impact of the ac-dc stage

PWM scheme can be observed, which was a reduction between 150 kHz – 2 MHz range. When case III is compared to that of Fig. 3-25, notable increase can be observed from 150 kHz – 1 MHz without a presence of the cancellation between ac-ac stage. The results for the two modes of operation verify the importance of topology and PWM schemes selection for the dc-dc stage in an EMI mitigation strategy.

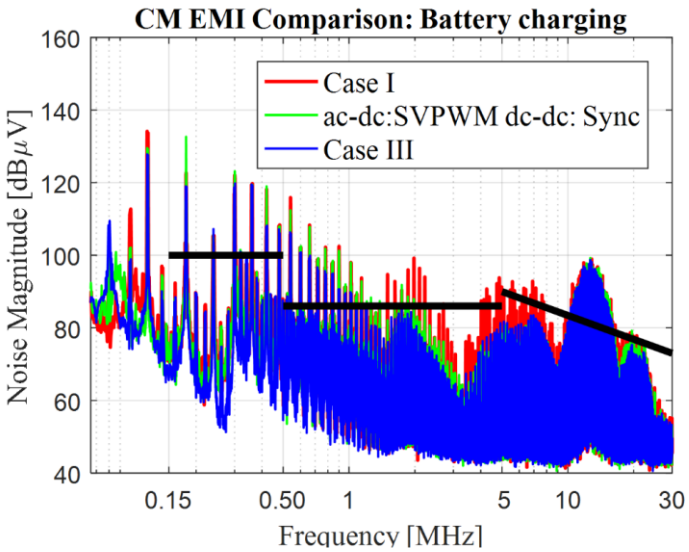


Fig. 3-26. Experimental results for CM EMI depending on the PWM schemes of the ac-ac stage and dc-dc stage in battery charging mode.

A comparison of the frequency spectra between the proposed frequency-domain model and the experimental results are shown in Fig. 3-27. The proposed model captures the change of CM noise according to the mode of operation by CMV cancellation of the ac-ac stage, and also the impact of the dc-dc stage on the low-frequency range, and over MHz range.

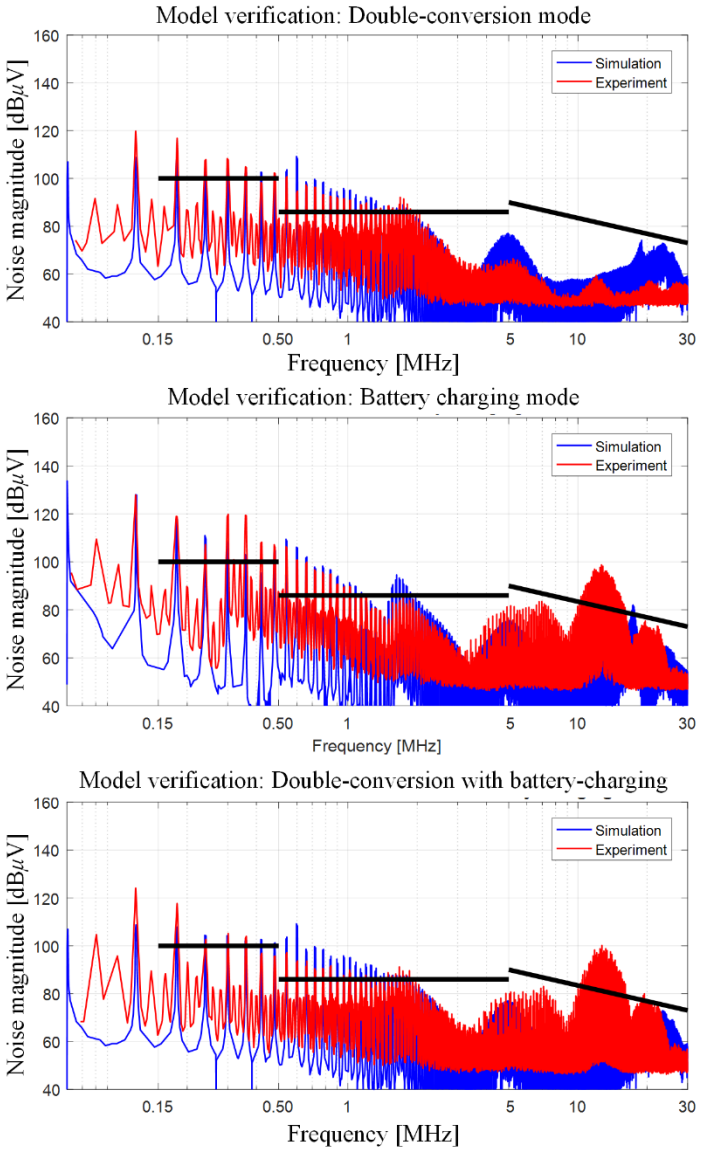


Fig. 3-27. Verification of the frequency-domain model with the measurement.

Table 3-7. Parameters for 20 kW full-SiC UPS.

Parameter	Value	Parameter	Value
$L_{f,ac1}$	90 μH	$L_{f,dc}$	253 μH
$C_{f,ac1}$	25 pF	$C_{f,dc}$	64.3 pF
$R_{f,ac1}$	23 kΩ	$R_{f,dc}$	40 kΩ
$L_{f,ac2}$	44 μH	$L_{cabinet}$	660 nH
$C_{f,ac2}$	9 pF	$C_{cabinet}$	10 nF
$R_{f,ac2}$	6.56 kΩ	C_{bus}	100 pF
$C_{f,ac}$	1.6 μF	$R_{load,ac}$	12 Ω
$R_{load,dc}$	22 Ω	C_{dc}	140 μF
C_s	74 pF	C_{s2}	58.3 pF

3.7 Chapter Conclusion

In this chapter, a three-terminal CM EMI model for a UPS has been developed. Based on the model, EMI generation, propagation, and mitigation strategy of full SiC UPS module have been investigated. By defining the common-mode voltage referred to the mid-point of the dc-link, an EMI model for the dc-dc stage can be connected to that of the ac-ac stage. The impact of the dc-dc converter and battery-rack can be predicted based on the model.

Among the three stages, the additional noise generation of the dc-dc converter is critical with the presence of CMV cancellation between the rectifier and inverter. Even when there is no ac-ac stage CMV cancellation, the dc-dc stage may contribute to high noise generation. Resonance between the dc-inductor and parasitic capacitance of the battery-rack to the earth can result in an increase of CM noise near tens and hundreds of kHz, which could be critical for the EMI filter design. Also, the resonance deteriorates the noise profile in a very high-

frequency range when the dc-dc converter operates. As a result, the output CM EMI of full-SiC UPS drastically deteriorated with the dc-dc converter operation.

As a mitigation strategy of EMI during the design phase, different topologies and PWM schemes were compared for both the ac-ac and dc-dc stages. The double-conversion mode with battery charging, and battery charging mode were chosen for the comparison. Experimental results for a double-conversion mode with battery charging showed that CM noise can be decreased by up to 16 dB in the 150–500 kHz range and around 15 dB over 1 MHz, by minimizing the emissions from the dc-dc converter.

A containment strategy of EMI with a selection of a CM EMI filter structure and an optimized design is not covered in this work and left as future work. The three-terminal CM model can be utilized for designing the ac-side, and also the dc-side EMI filter by providing an understanding of the interaction among the rectifier, inverter, and dc-dc converter. The principle of this work can be extended to other applications such as energy storage systems (ESS), and electric vehicles (EV) where a large battery with an active dc-dc converter is connected to ac-dc converters or interfaces with other power electronics systems.

Chapter 4. Single Pulse Common-Mode Voltage PWM Scheme to Achieve High Power Density for Full-SiC Three-level Uninterruptible Power Supply

4.1 Chapter Introduction

Superior loss characteristics of wide-bandgap (WBG) devices is improving both power density and efficiency of power electronics. With a reduction in the cost, these devices are expected to replace the conventional Si-IGBT based solutions for grid-connected applications. Uninterruptible power supplies (UPSs) as Fig. 4-1 are one of the applications that may highly benefit from the low-loss characteristic of SiC MOSFETs. A double conversion efficiency can be as high as 98% while the power density of the power electronics system can significantly be improved compared to Si-based converters with a switching frequency below 20 kHz. Three-level inverters are widely adopted in grid-connected inverters. Due to its multilevel voltage, the size of the filter stage can be reduced with the same switching frequency. The benefit of WBG-based multi-level inverters has been investigated in [10], [43], [111], [112] With high switching frequency and multi-level voltage, the voltage harmonic can be small and the size of the filter can be minimal. Also, multi-level topologies benefit on electromagnetic interference (EMI).

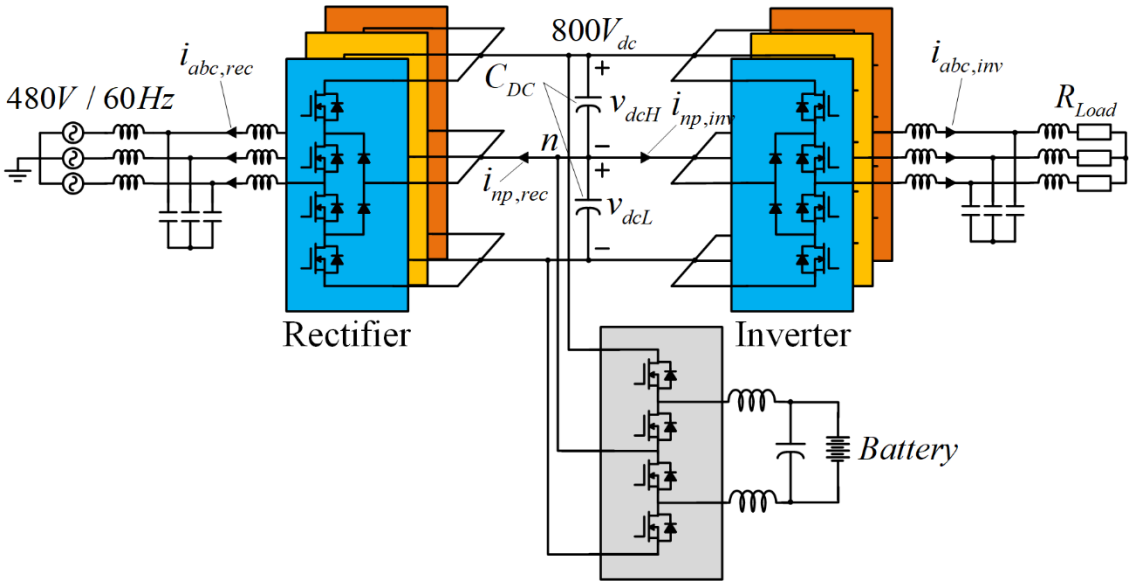


Fig. 4-1. Three-phase uninterruptible power supply comprised of full-SiC Neutral-Point-Clamped (NPC) phase legs.

An increase in switching frequency brings a change in the contributions of power electronics components on total volume [3], [48], [113], [114]. The size of the main boost inductors is reduced compared to Si-IGBT designs. On the other hand, the portion of EMI filters in the total volume increases, especially the common-mode (CM) part. In [3], optimized designs for 5 kW two-level inverter have been compared between a Si-based inverter and a SiC-based inverter. The contribution to the volume of EMI filters increased from 4% to 18%. In [50], the size of common-mode (CM) chokes for CM EMI noise had to significantly increase to meet the EMI standards when the switching frequency increased by 10 times.

Secondly, the contribution of dc-link capacitors may increase in three-level topologies [48], [114]. A low-frequency fluctuation exists on neutral point voltage (NPV) and, if not compensated, the fluctuation causes an error on the voltage synthesis and distort the load current. As the design of filter inductors seeks to be small, utilizing the benefits of both high

switching frequency multi-level voltage, the amount of the distortion can be more severe in a case of full-SiC multi-level inverters. Large dc-link capacitors can suppress this low-frequency fluctuation. However, since the size of these capacitors is not relevant to the switching frequency, the contribution of these capacitors on the total volume may become more noticeable along with a relative decrease in the volume of the other inductive components. The optimization result in [48] showed that the dc-links may take up to 42% of the total volume at 36 kHz switching. Especially in UPS, required hold-up time in a case of power interruption can be handled by a battery and dc-dc stage. DC-link capacitors solely function as an energy buffer, not as storage.

To decrease the volume of the CM EMI filter, reduced CM voltage PWM schemes have been investigated [96]–[98], [102]–[105], [115]–[119]. These schemes target to limit the maximum magnitude of output CMV or the number of transitions within a single switching-period to reduce the emission on the high-frequency range. To achieve these two goals, the basic principles of the PWM schemes can be classified into three. Firstly, the switching of different phases can be synchronized to limit a transition of output CMV [96]–[98], [102], [104], [105], [115]–[118]. Secondly, one of the phases is clamped and there exists no switching within a single switching period, which reduces the number of transitions within a switching cycle from 6 to 4 [103]–[105], [116]. Lastly, the switching states of three-phases are arranged in a way that the maximum magnitude of CMV can be limited [103]–[105], [115], [117]–[119].

For three-level inverters, only vectors with zero CMV can be used to totally eliminate CMV [115]. However, it limits the modulation index (MI) to be below 1. In [104], [116], a flipped carrier or a sawtooth carrier is used to arrange the switching sequence and different zero

sequence-voltages (ZSV) are injected for NPV balancing. In [105], a space-vector modulation which uses a large, medium, and zero-vector (LMZ) is proposed and a large, medium, and small-vector (LMS) combination is used for the NPV balancing. However, all these schemes focus on a single three-level inverter. In a configuration as Fig. 4-1, the CMV cancellation presents between the rectifier and inverter. When the CMV pattern of the rectifier and inverter are different, this cancellation may not be maximally utilized or even CMV emission can be worse. In [96]–[98], a PWM scheme for the two-level ac-ac stage has been developed. A ZSV to synchronize the switching instant between the rectifier and inverter is injected [96], [97] or all switching pulses are rearranged to maximize possible cancellations [98]. However, these schemes are limited to the two-level ac-ac stage.

NPV fluctuation can be compensated on the output voltage synthesis [120], [121]. In [120], [121], NPV unbalance is compensated for output differential-mode voltage (DMV) by using geometry of distorted vector triangles [120] or changing carrier-slopes [121]. However, most of reduced CMV PWM schemes assume a stiff dc-link, and compensation of NPV unbalance mostly focus on DM voltage, not on the CM voltage.

In this chapter, a reduced CMV scheme for the ac-ac stage of the full-SiC 3-level UPS has been proposed. The proposed PWM scheme achieves three goals together to reduce the size of the CM EMI filter and dc-link capacitors; reduced CMV, control of NPV, and compensation of NPV fluctuation on both DMV and CMV. A new vector combination has been proposed based on synchronized switching among three-phases. With the proposed vector combinations, the CMVs of the rectifier and the inverter are a single pulse which is aligned at the center of the switching cycle all the time. Such shape and alignment can easily

utilize CMV cancellation in the three-level ac-ac stage. A carrier-based implementation is presented to avoid complexity for the implementation based on digital signal processors. A drift of NPV can be prevented by choosing one of three different combinations depending on their NP current. A simple compensation method of NPV fluctuation by small dc-link capacitors has been proposed based on the correction of carriers for DM voltage and ZSV for CM voltage. The proposed scheme is verified with the UPS prototype and the experimental setup in Fig. 3-2

4.2 Proposed Switching Sequences

With the topology and PWM scheme proposed in Chapter 3.5.2, the noise generation of the dc-dc stage is zero in ideal condition. Considering the asymmetry in hardware, a perfect synchronized switching may not be feasible, but the generated CM noise from the dc-dc stage is minimal. More details can be found in [122]. The emission of a single ac-dc stage can be reduced by the PWM schemes introduced in Chapter 3.5.1. However, most of the reduced PWM scheme for the 3-level inverter focus on a single ac-dc stage, and the CMV cancellation between the rectifier and inverter is not considered.

In this section, a new vector combination is introduced to minimize CM noise generation from the ac-ac stage. A definition for switching states of a 3-level phase leg is shown in Fig. 4-2(a) and Table 4-1. A space-vector diagram of a single 3-level inverter is shown in Fig. 4-2(b). Depending on the magnitude of the voltage vector, all vectors are classified into large, medium, small, and zero vector. The color of the vector indicates the polarity of the generated CMV: red for positive, blue for negative. The same sequence can be implemented by carriers

$(Carr_H, Carr_L)$ as Fig. 4-2(b) which could be easily implemented with a digital signal processor (DSP). When the modulation signals ($v^*_{max,s}+v^*_{xn}$, $v^*_{med,s}+v^*_{xn}$, and $v^*_{min,s}+v^*_{xn}$) are above zero, they are compared with $Carr_H$. If the modulation signal is larger than $Carr_H$, the switching state is at 'P' state, otherwise 'N' state. When the modulation signals are below zero, they are compared with $Carr_L$, and the switching state is similarly determined as Fig. 4-2(c). If $v_{xn,REC}$ is defined as the pole voltage of the rectifier which is the voltage difference between phase-*x* output and the mid-point, common-mode voltage is defined as (4.1).

$$v_{cm,rec} = \frac{v_{an,rec} + v_{bn,rec} + v_{cn,rec}}{3} \tag{4.1}$$

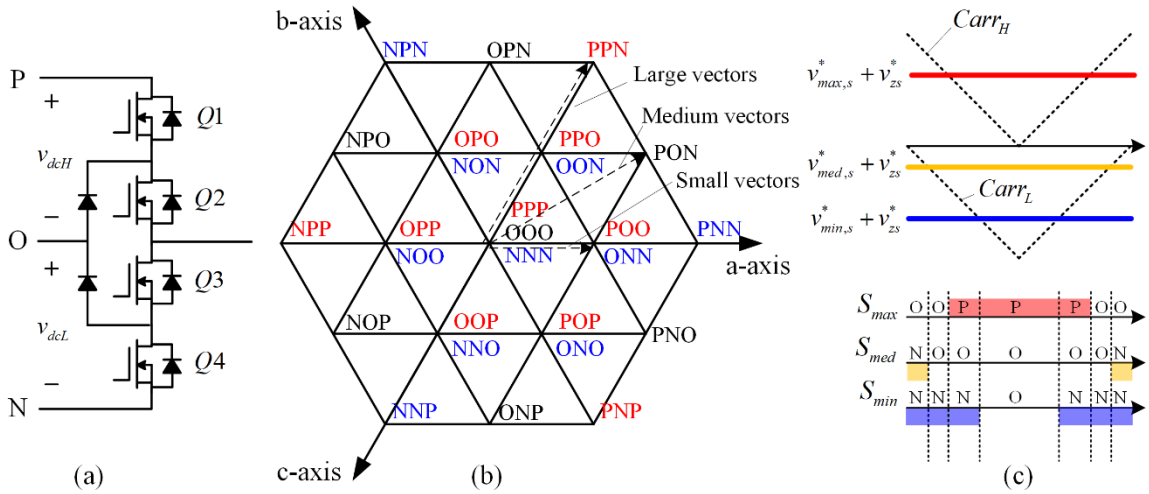


Fig. 4-2. (a) Three switching states of the NPC phase leg. (b) A space vector diagram of a single 3-level inverter (c) Carrier-based implementation.

Table 4-1. Definition of switching states for an NPC phase leg.

Switching state	Q1	Q2	Q3	Q4
P	ON	ON	OFF	OFF
O	OFF	ON	ON	OFF
N	OFF	OFF	ON	ON

The CM equivalent circuit for the ac-ac stage is shown in Fig. 4-3. $Z_{f,ac}/3$ refers to CM impedance of the LCL filter. R_{load} is a load resistor. At a relatively lower frequency range where noise propagation through parasitic capacitance of module outputs (C_s) or dc-bus (C_{bus}) to a heatsink is not dominant, the noise will be determined by subtraction of two noise source as (4.2). Once the rectifier and inverter always have a similar CMV pattern, this cancellation can be maximized to reduce CM noise emission [101].

$$v_{cm,btb} = v_{cm,rec} - v_{cm,inv} \tag{4.2}$$

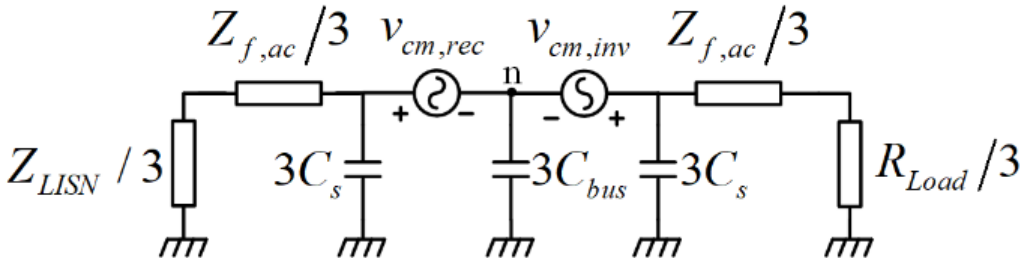


Fig. 4-3. CM equivalent circuit of the ac-ac stage.

LMZ vector combination as Fig. 4-4(a) is introduced in [105]. The reference for a voltage vector on *DQ*-frame is labeled as $\vec{v}_{abcs}$. A combination of large, medium, and zero vector is used to synthesize $\vec{v}_{abcs}$. This combination can cover whole modulation index (MI) range.

Since CMV is only generated by the large vector, CMV with a magnitude of $V_{dc}/6$ is aligned to be a pulse at the center of a switching period (T_{sw}) as Fig. 4-4(a). The number of transitions for the switching states of each phase is twice within T_{sw} which is related to the effective switching frequency of 4 MOSFETs.

The other LMS vector combination in Fig. 4-4(b) utilizes a combination of large, medium, and small vector, and is used for neutral point voltage balancing. However, both the large and small vector generate CMV with a magnitude of $V_{dc}/6$. If the number of transitions of the switching state per T_{sw} is limited to two to maintain the same switching-loss as LMZ vector combination, the three vectors can be arranged as Fig. 4-4. Three CMV pulses exists per T_{sw} when the large or small vectors are used. Therefore, when LMZ and LMS vector combinations are used in the rectifier-inverter configuration, it is apparent that CMV may not cancel each other when they don't operate with the same vector combination, and increasing noise emission.

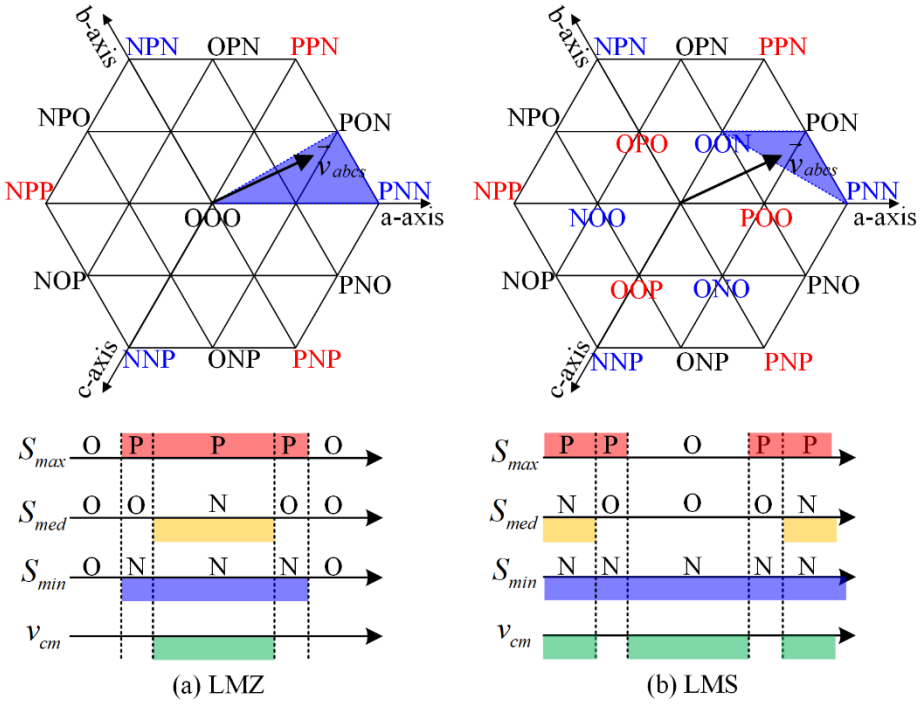


Fig. 4-4. Switching sequences for (a) LMZ, and (b) LMS vector combination.

4.2.1 Medium-Medium-Small (MMS) vector combination

To maximize the ac-ac stage cancellation for CMV, two vector combinations with a similar CMV pattern are required. In this section, a vector combination is proposed to be used with LMZ vector combination in the three-level rectifier-inverter system.

The proposed combination is shown in Fig. 4-5(a) and (b). Two medium vectors which do not generate CMV, and one small vector at the center of T_{sw} are used. CMV with a magnitude of $V_{dc}/6$ is only generated when the small vector is used. While the small vector can be aligned at the center of T_{sw}, the transition of the switching states for all three phases is limited to twice per T_{sw} as the same as the LMZ vector combination. Thus, there exists no additional switching

compared to the LMZ vector combination. These combinations are named as MMS1 and MMS2 combination depending on the polarity of CMV pulse. MMS1 vector combination generates CMV with negative polarity and MMS2 combination with positive polarity.

In LMZ and MMS vector combinations, CMV per T_{sw} is limited to a single pulse which is aligned at the center of T_{sw}. If LMZ and MMS vector combinations with the same polarity of CMV are used together, two center-aligned CMV pulses cancel each other and the CMV cancellation from the three-level ac-ac stage can be maximized. There exist other combinations which use two medium vectors and a small vector such as PON-OON-OPN. However, only combinations where the transition of switching states for all three phases is limited to twice per T_{sw} are considered in this paper to avoid thermal unbalance between the three phases and an increase in switching-loss. The vector space that LMZ and MMSs cover is shown in Fig. 4-6.

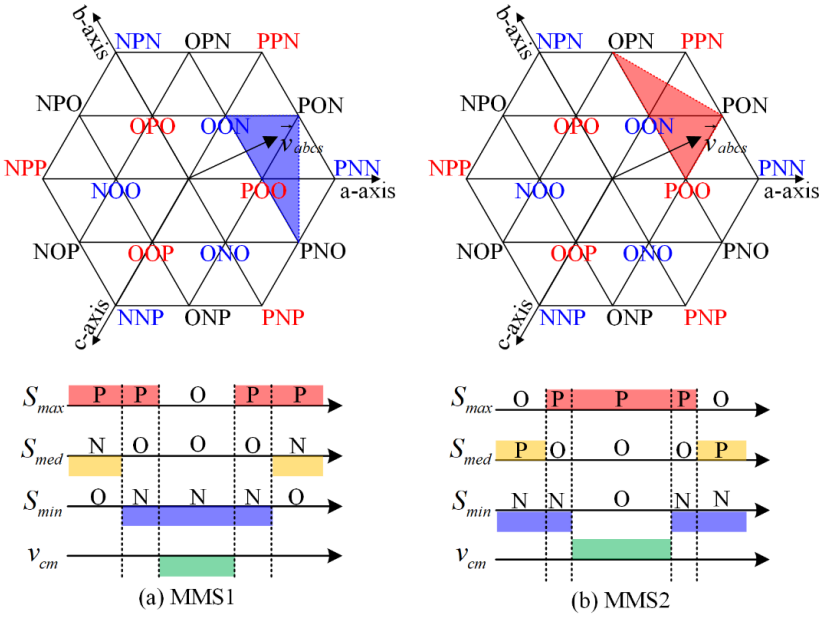


Fig. 4-5. Proposed switching sequences for (a) MMS1, and (b) MMS2 vector combinations.

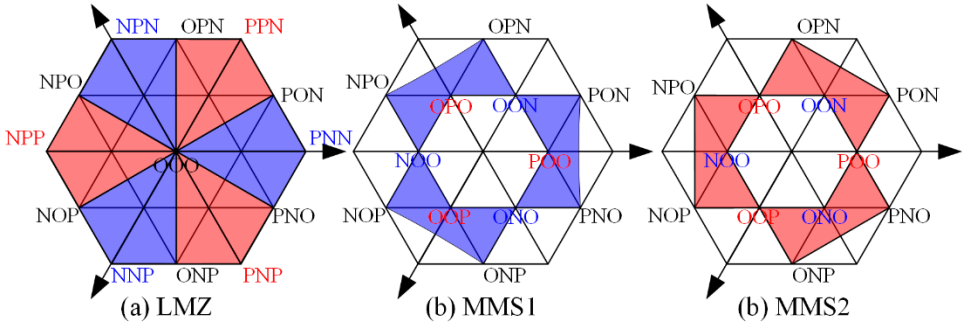


Fig. 4-6. Vector space covered by (a) LMZ, (b), MMS1, and (c) MMS2 vector combinations.

4.2.2 Carrier-based implementation

For a space-vector PWM, a sector for the voltage reference has to be identified. According to the shape of the triangle in Fig. 4-6, the sectors for the proposed MMS combinations cannot be simply determined by modulation index (MI) or voltage angle. In this work, an equivalent carrier-based implementation is used instead. The switching state waveforms in Fig. 4-4(a) and Fig. 4-5 are drawn for the same voltage reference. These vector combinations employ synchronous switching among different phases. The main difference between the three combinations is the choice of two phases to make a synchronized switching. For example, with the given reference in Fig. 4-4 and Fig. 4-5, phase-A and -B for the LMZ, phase-B and -C for the MMS1, and phase-C and -A for the MMS2 switch in a synchronous manner.

The P and N states in the LMZ and MMS vector combinations are arranged in a way that their effect on CMV can be canceled. The choice of carriers decides the allocation of switching states within T_{sw}. Two carriers are used for the three-level ac-dc converters. The upper carrier $(Carr_H)$ decides a transition time between O- and P-state. The lower carrier $(Carr_L)$ similarly decides transition time between O- and N-state. By using the flipped carriers, the sequence

between O-state and P- (or N-) state can be reversed. In this work, two types of a carrier pair are used depending on the slope after the reference updates as shown in Fig. 4-7. Once the carrier pair is defined, zero-sequence voltage (ZSV) can be injected to synchronize the switching instants between the two phases.

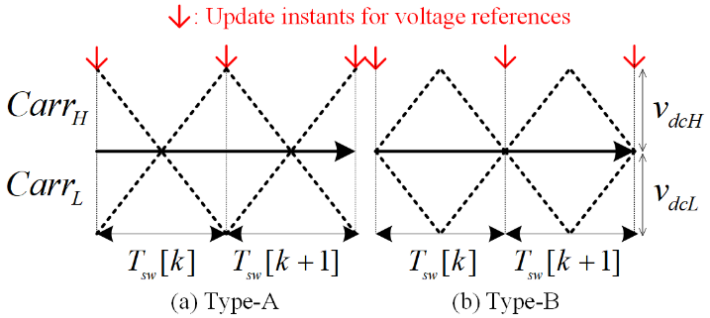


Fig. 4-7. Two types of a flipped carrier pair: (a) Type-A, and (b) type-B.

Examples for the carrier-based implementation are shown in Fig. 4-8. The maximum $\left(v^*_{max,s}\right)$ and minimum $\left(v^*_{min,s}\right)$ values among the three-phase voltage references can be found while $v^*_{med,s}$ refers to the median value. The pole voltage references $\left(v^*_{xn}\right)$ are sums of $\left(v^*_{xs}\right)$ and ZSV $\left(v^*_{zs}\right)$ where $x = a,b,$ or c.

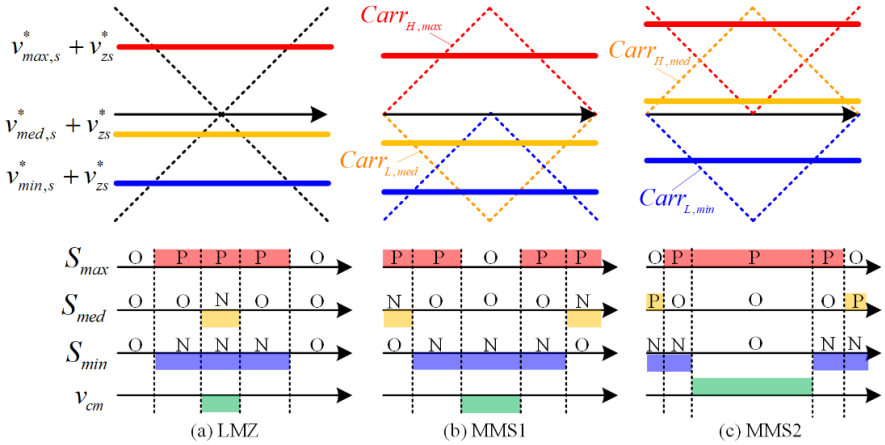


Fig. 4-8. Carrier-based implementation for the LMZ, and MMS vector combination.

For the MMS1 in Fig. 4-8(b), the phases correspond to $v^*_{med,s}$ and $v^*_{min,s}$ switch synchronously. Specifically, transition instants of O → N state for $v^*_{min,s}$ $\left(T_{min,O\to N}\right)$ and N → O state for $v^*_{med,s}$ $\left(T_{min,N\to O}\right)$ are synchronized. To realize such a sequence, different types of the carrier pair can be chosen for $v^*_{med,s}$ and $v^*_{min,s}$, similar to 2-level reduced CMV PWM schemes [103]. The type-B and -A carrier is used for $v^*_{med,s}$, and $v^*_{min,s}$, respectively. By using the type-B carrier for $v^*_{max,s}$, the location of P-state is distributed at the beginning and end of T_{sw} which aligns the CMV pulse at the center. Lastly, ZSV $\left(v^*_{zs,MMS1}\right)$ to make the synchronous switching can be calculated from (4.3), (4.4), and (4.5), when two dc-link capacitors are balanced. The result is (4.6). Since the triangular carriers enforce symmetry, the other switching instant after $T_{sw}/2$ will be automatically synchronized. Note that the impact from the dead-time or asymmetry in the hardware is not considered which may deviate the actual switching instants.

$$T_{med,N\to O} = \frac{T_{sw}}{2}\left(-\frac{v^*_{med,s} + v^*_{zs,MMS1}}{V_{dc}/2}\right) \tag{4.3}$$

$$T_{min,O\to N} = \frac{T_{sw}}{2}\left(\frac{v^*_{min,s} + v^*_{zs,MMS1}}{V_{dc}/2} + 1\right) \tag{4.4}$$

$$T_{med,N\to O} = T_{min,O\to N} \tag{4.5}$$

$$v^*_{zs,MMS1} = -\frac{V_{dc}}{4} + \frac{v^*_{max,s}}{2} \tag{4.6}$$

The type of the carriers for MMS2 vector combination can be similarly derived. To have $v^*_{max,s}$ and $v^*_{med,s}$ switch at the same moment, type-A and -B carrier pair can be used. The carrier pair for $v^*_{min,s}$ is set to be the type-B to distribute N-states at both ends of T_{sw}. For LMZ vector combination, the switching instants of $v^*_{max,s}$ and $v^*_{min,s}$ are in-sync and the type-A carrier pair is used for the three phases. The carrier types and ZSV are summarized in Table 4-2.

Table 4-2. Summary of carrier pairs and zero-sequence voltage for three switching sequences.

		LMZ	MMS1	MMS2
Carrier Types	$v^*_{max,s}$	A	B	A
	$v^*_{med,s}$	A	B	B
	$v^*_{min,s}$	A	A	B
v^*_{zs}		$-\frac{v^*_{max,s} + v^*_{min,s}}{2}$	$-\frac{V_{dc}}{4} + \frac{v^*_{max,s}}{2}$	$\frac{V_{dc}}{4} + \frac{v^*_{min,s}}{2}$

4.3 Neutral Point Voltage Balancing

In NPC topology, two dc-link capacitors exist and the difference between these two voltages is defined as neutral point voltage (NPV) unbalance $\left(\Delta v_{dc}\right)$. The neutral point current of the three-level inverter determines the dynamics of this unbalance. Also, in a practical condition, a drift or divergence of NPV may exist due to any hardware asymmetry. The NPV unbalance must be controlled to ensure that SiC MOSFETs operate within their safe operating area (SOA).

With the rectifier-inverter configuration, the equation for Δv_{dc} can be written with a function of neutral point current of the rectifier $\left(i_{np,rec}\right)$ and inverter $\left(i_{np,inv}\right)$ as (4.7). The duty-ratios for O-state decide a switching-cycle average of neutral point currents by two stages. For example, the duty-ratio of O-state for *x*-phase of the rectifier $\left(d_{Ox,rec}\right)$ can be written as (4.8) where *x* = *a*,*b*, or *c*. With the carrier-based PWM, $d_{Ox,rec}$ is determined by the duration where $v^*_{xn,rec}$ is located between $Carr_H$ and $Carr_L$ as (4.8) where $v^*_{xn,rec}$ is the pole voltage reference for phase-*x* of the rectifier.

$$\Delta v_{dc} = v_{dcH} - v_{dcL} = \frac{1}{C_{dc}} \int \left(i_{np,rec} + i_{np,inv}\right) dt \tag{4.7}$$

$$d_{Ox,rec} = 1 - \frac{\left\| v^*_{xn,rec} \right\|}{V_{dc}/2} \tag{4.8}$$

From $d_{Oa,rec}$, $d_{Ob,rec}$, and $d_{Oc,rec}$, the equation for the switching-cycle average of rectifier-side neutral point current $\left(\bar{i}_{np,rec}\right)$ can be written as (4.9). f the inverter-side can be similarly written as (4.10). The values for $d_{Ox,rec}$ are determined by the PWM method, and the voltage reference. Since the voltage reference of the rectifier and inverter is mainly determined by the line voltage, $d_{Ox,rec}$ and $d_{Ox,inv}$ are very similar once the same PWM methods are used for both sides. The direction of the rectifier and the inverter currents are opposite considering the power flow, thus most of $i_{np,rec}$ and $i_{np,inv}$ cancel out during normal operation. However, due to the power flow toward the battery or the variation of line voltage, the current and MI for the two side may not be identical. Thus $i_{np,rec}$ and $i_{np,inv}$ cannot be fully canceled and deviate Δv_{dc} .

$$\bar{i}_{np,rec} = d_{Oa,rec} i_{a,rec} + d_{Ob} i_{b,rec} + d_{Oc} i_{c,rec} \tag{4.9}$$

$$\bar{i}_{np,inv} = d_{Oa,inv} i_{a,inv} + d_{Ob} i_{b,inv} + d_{Oc} i_{c,inv} \tag{4.10}$$

The NPV control can be achieved by modifying ZSVs of the rectifier or inverter. In this PWM scheme, the degree of freedom for ZSV is dedicated to enforcing the synchronized switching. Therefore, control of NPV drift is done by choosing ZSV among LMZ, MMS1, and MMS2. The MMS1 and MMS2 vector combinations cannot cover the whole vector space, which indicates that the transition among the three sequences is not always available.

In most of the operation condition, grid-connected converters operate with MI > 2/3. In this range, the reference voltage vector is located on the outer hexagon of the 3-level inverter in

Fig. 4-2(b) and (4.11) holds for the three-phase voltage reference. Also, the pole voltage references should not go over the modulation range as (4.12). Under these two conditions, the vector space covered by the three pairs is shown in Fig. 4-6. The LMZ combination covers the whole MI range. The MMS1 and MMS2 together cover the area between 2/3 < MI < 1, and a part of the vector space when MI > 1. Therefore, the LMZ combination can be used for full MI range operation, and the MMS combinations are injected when it is necessary to control the drift of NPV.

$$V_{dc}/2 < v^*_{max,s} - v^*_{min,s} < V_{dc} \tag{4.11}$$

$$\begin{aligned} v^*_{max,s} + v^*_{zs} &< V_{dc}/2 \\ v^*_{min,s} + v^*_{zs} &> -V_{dc}/2 \end{aligned} \tag{4.12}$$

In Fig. 4-9, $i_{np,rec}$ of the LMZ, MMS1, and MMS2 are compared along a single line-cycle under unit power factor condition. Depending on MIs between 0.67 and 1.1, available angles for the MMS1 and MMS2 are limited. When MMS pairs are available, they inject larger i_{np} magnitude than the LMZ combination, and also, have an opposite polarity which can either increase or decrease Δv_{dc}. The value for i_{np} of LMZ, MMS1, and MMS2 can be easily calculated based on the ZSVs in Table 4-2, (4.8), and (4.9).

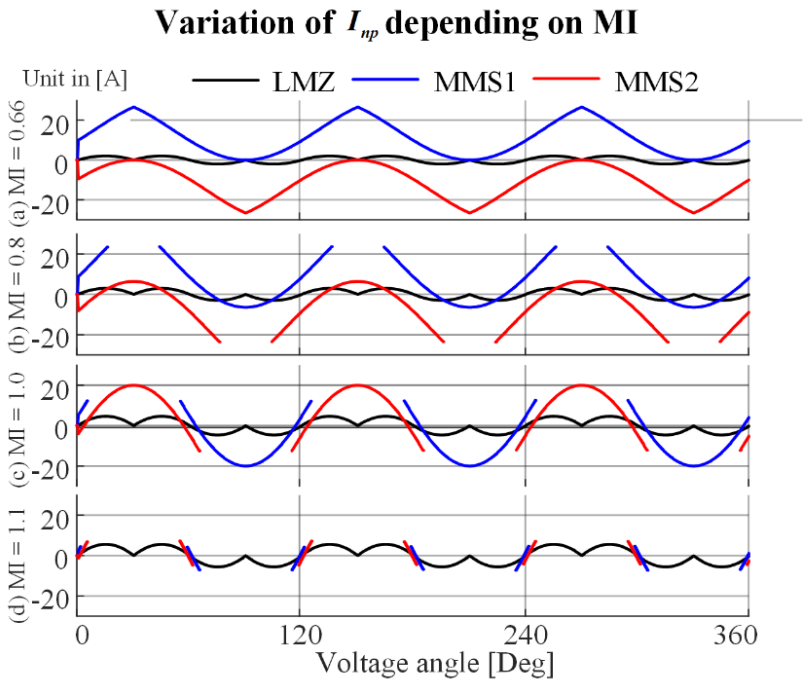


Fig. 4-9. Waveforms of NP current depending MI under unit power factor condition (a) MI = 0.66, (b) MI = 0.8, (c) MI = 1.0, and (d) MI = 1.1.

A simple flowchart for NPV balancing is shown in Fig. 4-10. The balancing algorithm operates when either the moving average of Δv_{dc} goes over a certain limit or instantaneous value of Δv_{dc} is over 60V. Note that, for the control of moving average, 3rd order harmonics have to be filtered which naturally present with small dc-link capacitors. Once the absolute value of Δv_{dc} goes over the limit, ZSV for MMS1 and MMS2 can be checked whether they are available according to (4.11) and (4.12). When either of MMS can be used, i_{np} is calculated and its polarity can be checked. Finally, the combination can be selected among the three to reduce $\left|\Delta v_{dc}\right|$. The controllability of NPV with the non-u.p.f. case is not investigated.

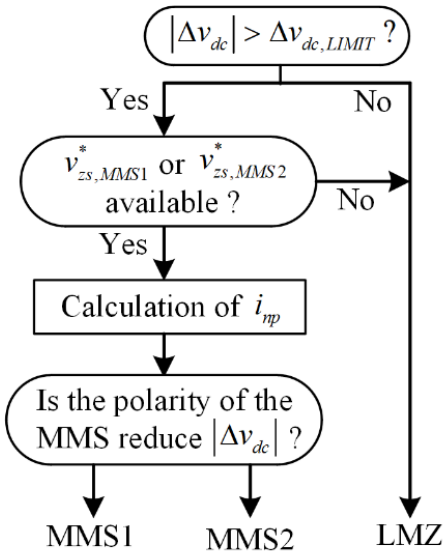


Fig. 4-10. Flowchart for selection among LMZ, MMS1, and MMS2 vector combinations for NPV balancing.

4.4 Compensation of NPV Unbalance for Output DM and CM Voltage

Two major design considerations to size the dc-link capacitors of the three-level inverters can be hold-up time or suppression of 3rd harmonics fluctuation. To ensure the hold-time in case of the power interruption, the capacitors should store large enough energy which increases the size. However, in UPS, dedicated energy storage can support such a functionality and dc-link capacitors may be designed to solely limit the low-frequency ripple on NPV. Thus, the size of the dc-link capacitors does not benefit from the high switching frequency of full-SiC phase leg. Along with size reduction of output filter inductors, dc-link capacitors may take a considerable portion of the total volume.

To further improve the power density, the small film capacitors can be used for the dc-link. In this case, the fluctuation of NPV create an error on the synthesis of output differential-mode

(DM) voltage and the output current will be distorted with low-order harmonics. Since the filter inductors of the full-SiC inverters are designed to be small to maximize the benefit of high switching frequency, the degree of this deterioration by the NPV unbalance will be more severe compared to the Si-based inverters while the THD on the grid-side current and load-side voltages are required to fulfill standards as IEC62040-2 or UPS specification. A simulation result is shown in Fig. 4-11. The parameters for UPS have been summarized in Table 3-7. The total inductance value of the LCL filter was only 143 μH. When Δv_{dc} is at 5% of total dc-link, THD of output current increased from 3% to 9%.

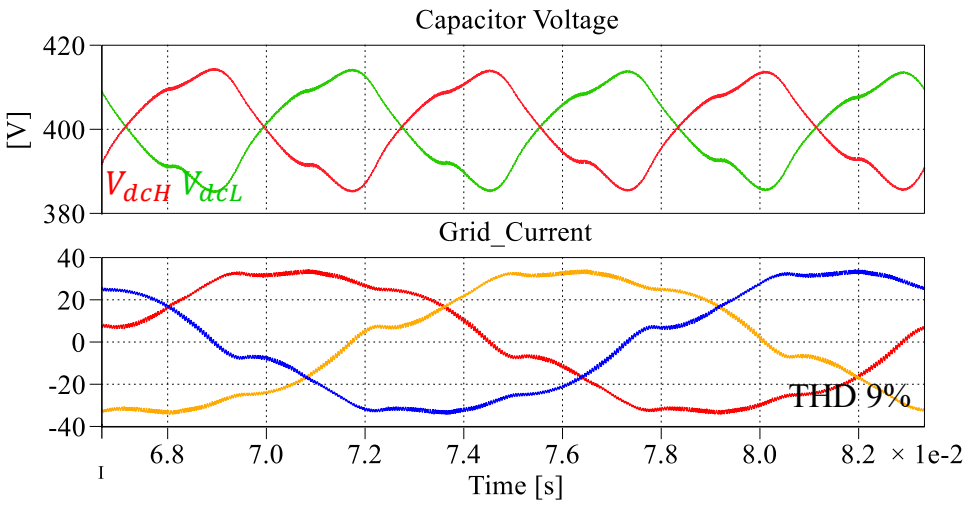


Fig. 4-11. Distortion of output current when magnitude of Δv_{dc} oscillation is 40 V.

For carrier-based PWM schemes, the unbalance can be compensated through modification of carrier length. Instead of using $V_{dc}/2$, actual values for v_{dcH} and v_{dcL} is used to calculate duty ratio as Fig. 4-12 and the error on output DM voltage can be compensated. However, the modification on the carrier may misalign switching instants eventually generate additional glitches on CMV. Such glitches provoke an increase in high-frequency CM noise, which

requires higher attenuation by CM EMI filter or may penetrate through auxiliary circuits and interrupt the proper operation of the control system.

In the proposed reduced CMV scheme, ZSV determines the switching instant once the carriers are selected according to Table 4-2. From the geometry in Fig. 4-12, modified ZSV can be easily derived to re-synchronize the switching. The result is summarized in Table 4-2. By using these ZSVs with modified carriers, the impact of Δv_{dc} on both output DM and CM voltage can be compensated.

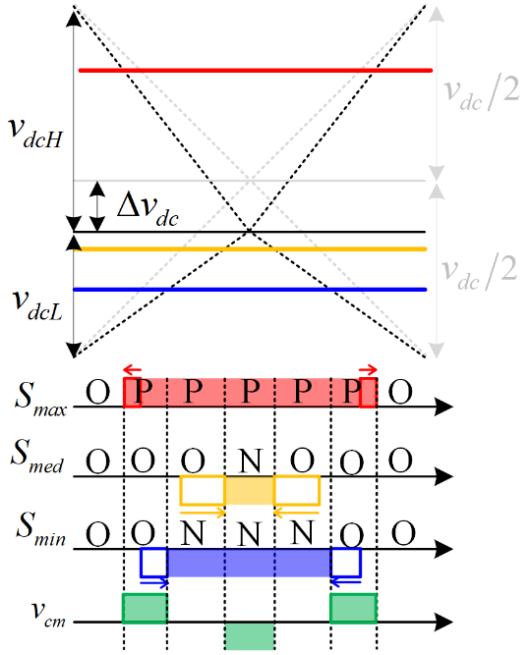


Fig. 4-12. Misalignment of switching instants by modification of carriers.

Table 4-3. Modified ZSV for compensation of dc-link unbalance.

	Modified v_{zs}^{*}
LMZ	$-\frac{\Delta v_{dc}}{2}-\frac{v_{max,s}^{*}v_{dcH}+v_{min,s}^{*}v_{dcL}}{v_{dcH}+v_{dcL}}$
MMS1	$\frac{-v_{dcL}-\Delta v_{dc}}{2}+\frac{v_{max,s}^{*}}{2}$
MMS2	$\frac{v_{dcH}-\Delta v_{dc}}{2}+\frac{v_{\min,s}^{*}}{2}$

4.5 PLECS Simulation

PLECS simulation has been performed to verify the proposed PWM scheme. 3-level NPC inverters are used for the rectifier and inverter as shown in Fig. 4-1. The parameters for the ac-ac stage is the same as Table 3-7. Firstly, the rectifier and inverter operated with 3-level SVPWM. The waveforms of CMV are shown in Fig. 4-13(a) for 15 switching-cycles. CMV of the rectifier and inverter has 6 transitions per T_{sw}, and, with the presence of the cancellation, the 6 glitches are generated. The waveforms of the proposed PWM scheme is shown in Fig. 4-13(b). LMZ, MMS1, and MMS2 generate a single pulse for their CMV. By the cancellation between the rectifier and inverter, resultant CMV is only two pulses per T_{sw}. Since there exists a small difference in the angles of voltage references between the rectifier and inverter, the polarity of one may change prior to the other. In such a condition, CMV of two stages may overlap and the magnitude of $v_{cm,rec}-v_{cm,inv}$ reaches $V_{dc}/3$ at that moment.

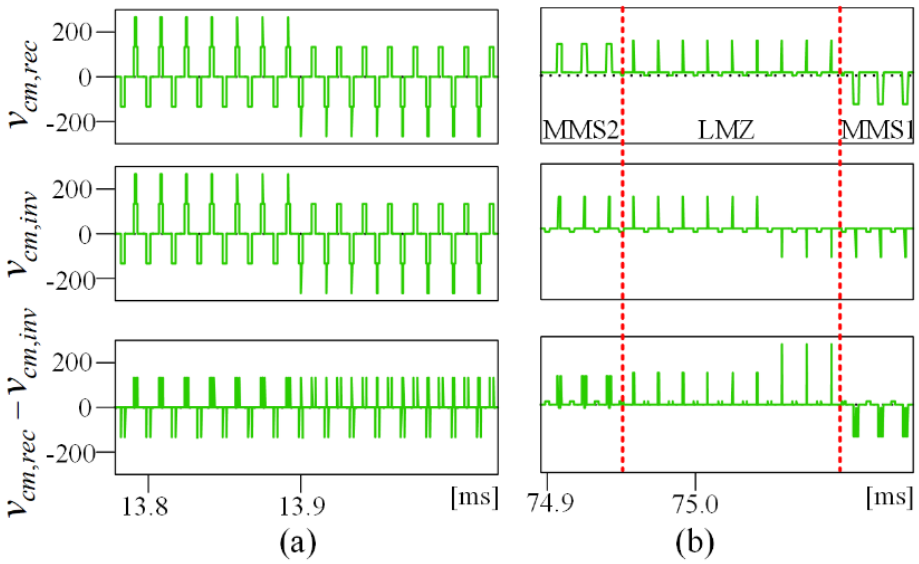


Fig. 4-13. Time domain waveforms of $v_{cm,rec}$, $v_{cm,inv}$, and $v_{cm,rec} - v_{cm,inv}$ (a) SVPWM, and (b) proposed PWM scheme.

Secondly, the NPV balancing capacity has been tested. The size of the capacitor is designed to be 150 μF. When only the rectifier or inverter operates with the dc-dc stage, 3rd harmonic ripple on NPV is limited to 5% of total dc-link at rated condition. For the NPV balancing flowchart in Fig. 4-10, the value for Δv_{dc} went through a notch filter to eliminate 3rd harmonics components and extract the average value. The simulation result is shown in Fig. 4-14. The reference for Δv_{dc} was changed from 50 V to 0 V. It can be seen that the MMS2 is used to elevate Δv_{dc} to 50 V, and, MMS1 is used to set it down to 0 V. By transitions among the LMZ and MMS, the drift of NPV can be prevented.

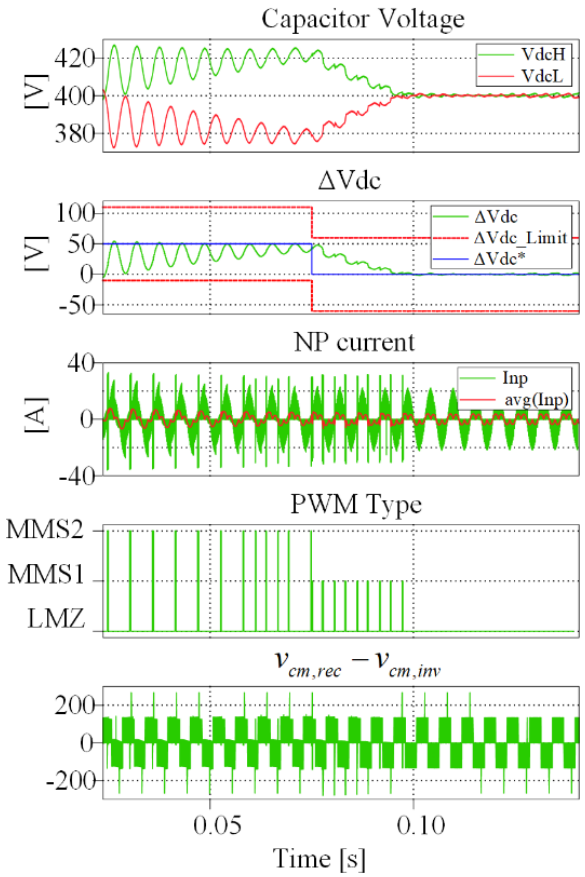


Fig. 4-14. Simulated waveforms for NPV balancing.

4.6 Experimental Results

A prototype 20 kW full-SiC UPS has been built. A picture of the prototype and experimental setup are shown in Fig. 3-2. A single low ESL film capacitor (FFVS6K0147K—from AVX Corporation) with 140 μH is used for each dc-link. The value for the capacitors is selected so that, when the rectifier operates at 20 kW, the maximum Δv_{dc} equals to 40V which is 5% of the total dc-link voltage. A water-cooled resistor bank was used for ac-loads. MX45 from California Instrument served as the ac source. The LCL filter is designed to meet THD of 4%. The

parameters for the ac-ac stage is the same as Table 3-7. Details of the hardware can be found in Chapter 5.

First, the implementation of the LMZ and MMS combination were verified. When 20 kW power is transferred from the rectifier to inverter, $v_{cm,rec}$, $v_{cm,inv}$, and $v_{cm,btb}$ are measured and the result is shown in Fig. 4-15. In Fig. 4-15(a), SVPWM is used, and the resultant CMV waveform shows 6 pulses within T_{sw}. On the other hands, the proposed LMZ and MMS combination generates a single pulse as shown in Fig. 4-15(b) and cancels each other. The small glitches in MMS1 are caused by the dead-time.

The measured CM noise spectrum when UPS operates in double-conversion mode is shown in Fig. 4-16. Note that, at the nominal condition, the voltage reference for two stages are almost identical except the voltage drop across the filter stage, and most of the CMV already are canceled. The proposed PWM scheme shows 4 dB decrease at 180 kHz and around 6 dB decrease at MHz range. The MI for inverter has been adjusted to 0.6 while the rectifier stage is at the rated condition to demonstrate the CMV reduction. In this case, CMV cannot be canceled naturally, and the proposed PWM scheme reduced the maximum 16 dB at low-frequency range, and near 10 dB at MHz range.

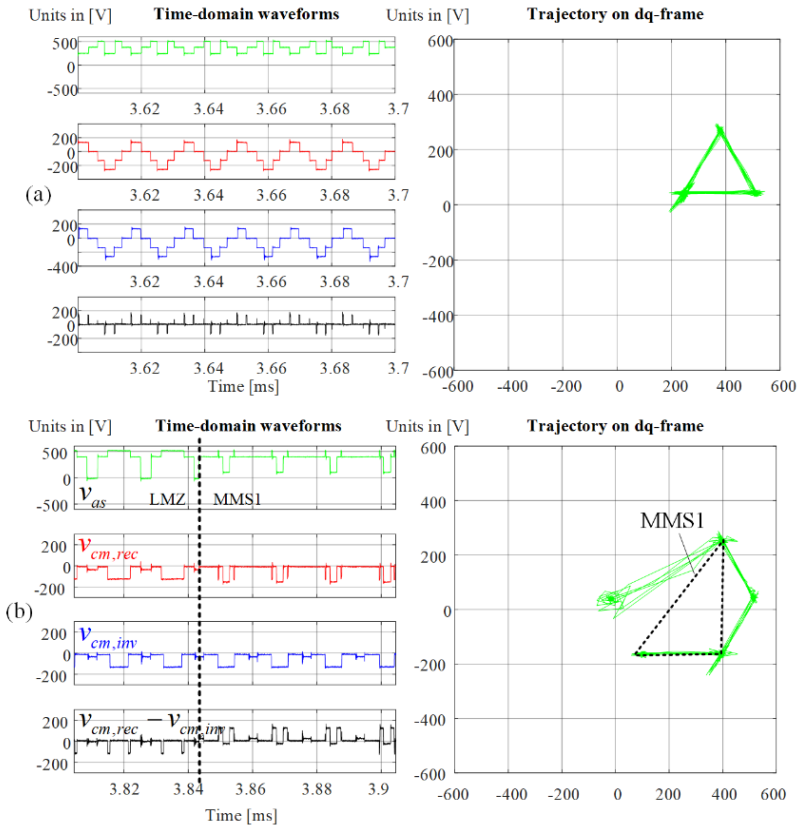


Fig. 4-15. Phase-A voltage, common-mode voltage of inverter, rectifier, and ac-ac stage for (a) SVPWM, and (b) proposed PWM scheme.

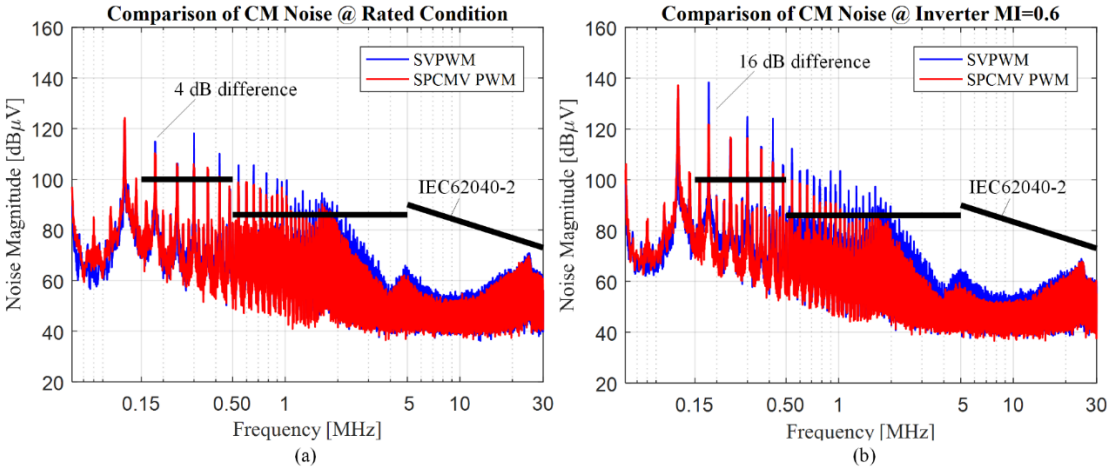


Fig. 4-16. Measured CM EMI spectrum: SVPWM vs. proposed PWM scheme. (a) At rated condition, and (b) when the inverter MI set to 0.6.

Secondly, the NPV balancing capacity has been tested. When UPS operates at the rated power, Δv_{dc} was intentionally set to 50 V and NPV balancing was done by the inverter. The result is shown in Fig. 4-17. From the three-phase pole voltage outputs, which vector combination is being used can be observed. The vector combination of inverter changed from LMZ to MMS2 and the NPV can be set back to 0. The same experiments have been performed for 3 different MIs: 0.66, 0.8, and 1.07 and the dynamics of Δv_{dc} are shown in Fig. 4-18. Since the MMS pairs only covers a part of the vector space over MI = 1, the case with MI = 1.07 settle down to 0 slower than the other two cases. Therefore, a selection of the dc-link capacitors should consider this to ensure that the NPV does not diverge at the high MI range.

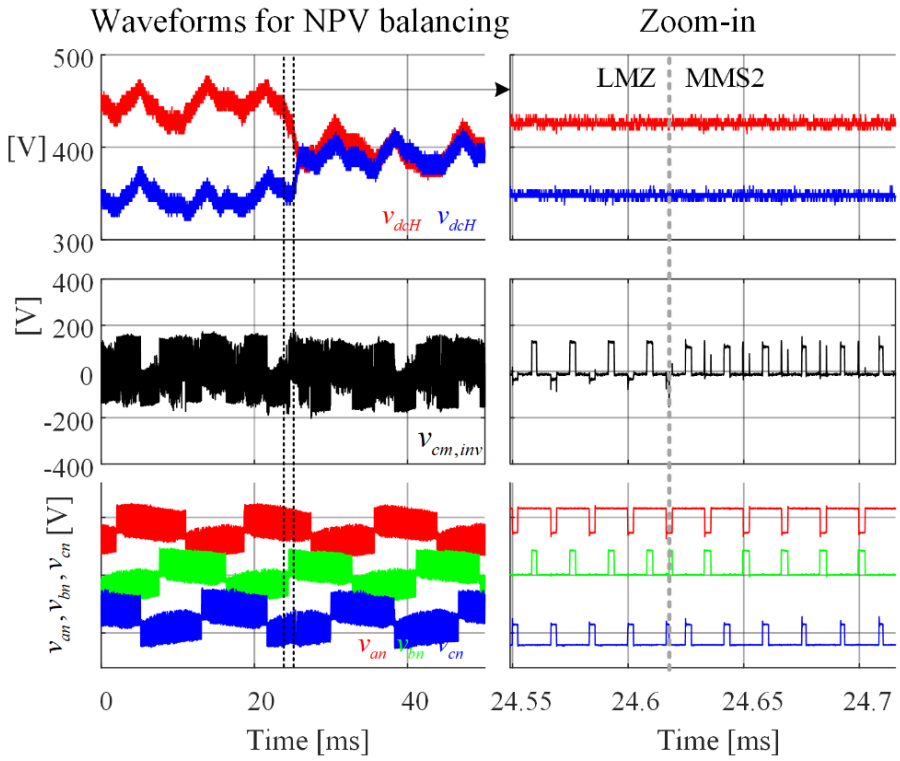


Fig. 4-17. Experimental waveforms for v_{dcH}, v_{dcL}, $v_{cm,inv}$, and three pole voltages of inverter during neutral point voltage balancing.

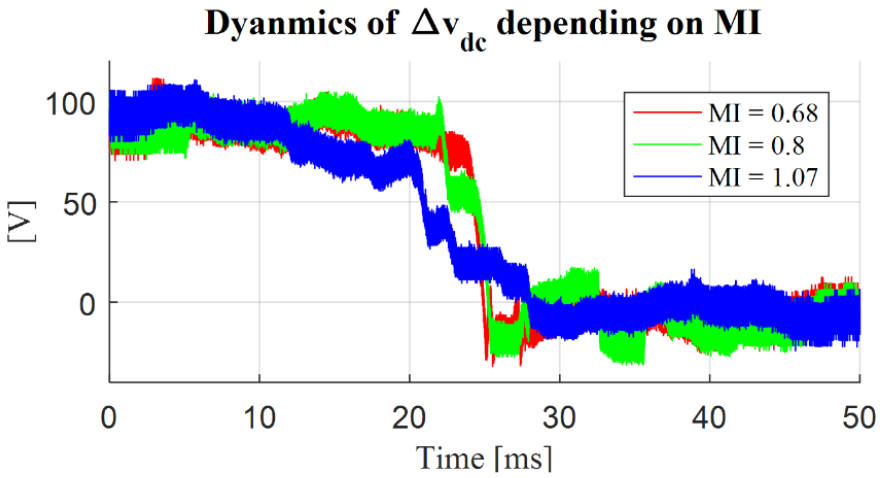


Fig. 4-18. Balancing of NPV depending on MI.

Lastly, the impact of NPV unbalance for the full-SiC 3-level inverter and their compensations have been tested. As shown in Table 3-7, the minimal inductance of 130 μH is used for 20 kW, 480 V_{ac} line. For the demonstration, Δv_{dc} is controlled to be 50 V by the inverter, and the rectifier-side currents have been measured. The cases with and without the compensation for DM voltage is shown in Fig. 4-19. With the small inductors, the output current is severely distorted and THD of output current shows 7.3%. With the compensation, the THD drops to 4.3%. From the frequency spectrum in Fig. 4-19(c), it can be seen that the low-order harmonics such as 5th harmonics are large without any compensation.

If the same ZSVs as Table 4-2 are used, the switching instants cannot be synchronized. In Fig. 4-20, misalignments of LMZ combination is shown when Δv_{dc} equals to 40 V. The impact on the frequency spectrum is shown in Fig. 4-21. Without the ZSV compensation, the CM noise increased by maximum 6 dB between 1 – 5 MHz range wherein the noise may not be easily handled by passive EMI filters. The proposed method to re-synchronize the switching

instant does not suffer from a high computational burden and could effectively suppress an additional CM noise by the misalignments.

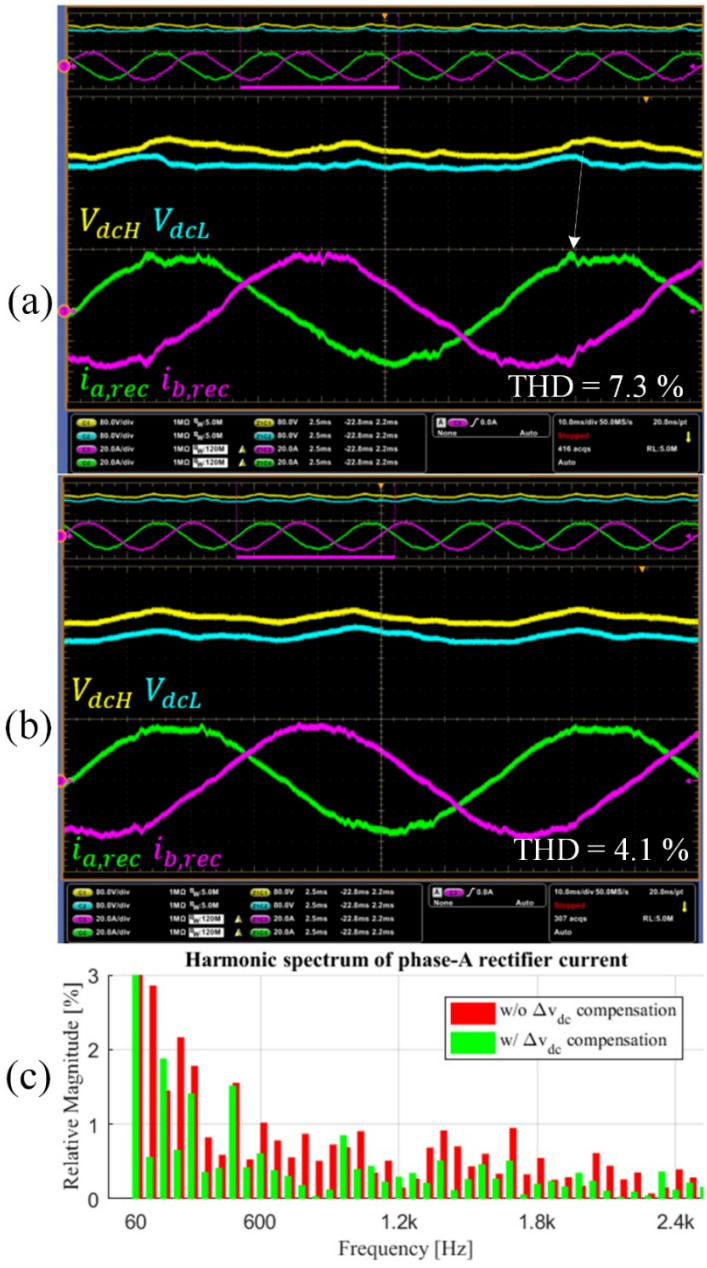


Fig. 4-19. Waveforms of rectifier phase-A and –B current [20 A/div] and v_{dcH} , v_{dcL} [80 V/div] (a) w/ carrier compensation, (b) w/o carrier, and (c) comparison on the frequency spectrum.

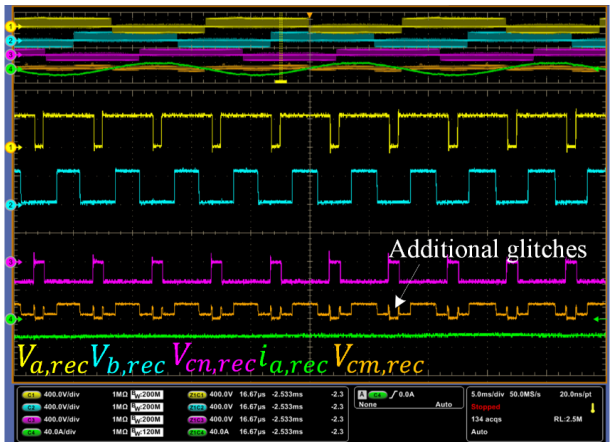


Fig. 4-20. Misalignments of switching instants by modification of carriers.

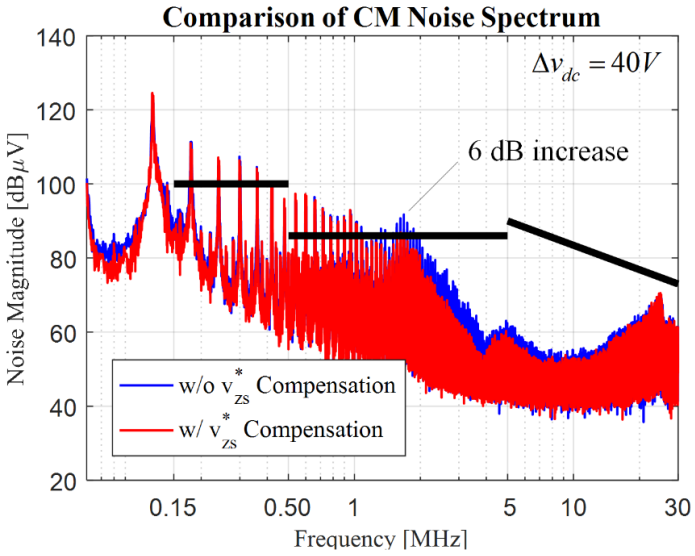


Fig. 4-21. Frequency spectrums with or without a compensation by the modified ZSV.

4.7 Chapter Conclusion

In this chapter, a reduced PWM scheme has been proposed for the full-SiC three-level UPS. MMS vector combinations together with LMZ vector combination have been proposed to fully utilize CMV cancellation of the ac-ac stage. A capability of neutral point voltage balancing has been investigated for unity power factor case. The simple carrier-based implementation has

been demonstrated to avoid complexity in the implementation. Lastly, the compensation of neutral point voltage fluctuation has been shown for both DM and CM voltage. With the proposed PWM scheme and compensations for neutral point voltage, CM noise and the size of dc-link capacitors can be reduced, thus can improve the power density of a full-SiC three-level ac-ac stage. A prototype full-SiC UPS with 60 kHz switching has been built and the proposed PWM scheme has been experimentally verified.

Chapter 5. Design of 20 kW Full-SiC, Three-level Three-Phase Uninterruptible Power Supply

5.1 Chapter Introduction

In this chapter, design, and implementation for high efficiency 20 kW, 480 V_{ac}, 800 V_{dc} full-SiC based UPS has been presented as a result of CM EMI modeling in Chapter 3 and the PWM scheme in Chapter 4. A double conversion efficiency (Ac-ac) of the state-of-the-art solutions based on Si-IGBT is limited to 96 ~ 97% range. Thanks to superior loss characteristic of SiC devices loss, the efficiency of a single stage can be up to 99% which leads to 98% double conversion efficiency. With high efficiency, the operation costs of UPS can be reduced [77]. Also, the increase in the switching frequency leads to higher power density [76].

To demonstrate and quantify the benefit of SiC devices, researches have demonstrated optimized three-phase AC-DC converter. An optimized design tool has been developed for SiC-based 2-level three-phase inverters and compared with the optimized Si-IGBT design in [123]. In [111], benefits by SiC device on 3-level T-type phase leg have been investigated, focusing on the reduction in semiconductor loss and a possible increase in the power rating of the phase leg. In [5], the performance of SiC-based 3-level photovoltaic inverters has been compared between hard- and soft-switched case in terms of power density and efficiency. In [114], [125], a design optimization for 3-level 20 kW UPS comprised Si-IGBT and SiC Schottky diode has been done. The result showed that 96.6% efficiency at 16 kHz switching

frequency. However, optimized design and power density improvement of full-SiC three-level UPS has not been demonstrated in the literature.

In this chapter, design of high-efficiency full-SiC three-phase UPS has been presented. The system specification is shown in Table 3-1. Firstly, double conversion efficiency of two-level and three-level topologies is compared based on the datasheet. Second, a gate driver has been designed and double pulse test (DPT) has been conducted to extract the switching-loss with minimal gate resistor. Third, a thermal simulation has been done to estimate a junction temperature rise and the switching frequency has been decided based on efficiency simulation. LCL filter has been designed to meet the specification. Lastly, a 20 kW full-SiC, three-level, three-phase UPS has been built and tested.

5.2 Topology and Module Selection

In this section, topologies and commercial modules are compared to achieve 98% double conversion efficiency with 20 kW output. Two-level and three-level topologies as Fig. 5-1 are considered. Selected devices and modules to implement 20 kW three-phase bridge are listed in Table 5-1. For two-level topology, a 1.2 kV half-bridge module and a 6-pack module have been selected. For three-level topology, a neutral point clamped (NPC) module and a half-bridge module with two discrete MOSFETs to realize a T-type phase leg have been chosen.

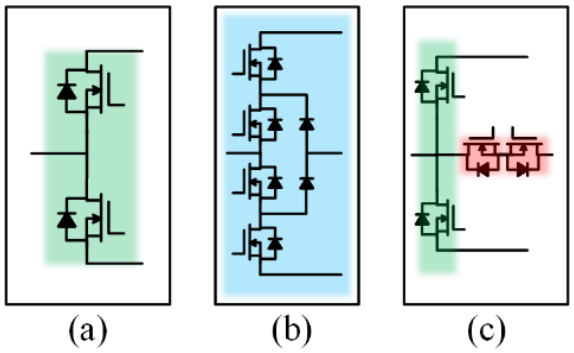


Fig. 5-1. Topology candidates (a) 2-level, (b) NPC, and (c) T-type.

Table 5-1. Module and device selection for comparison.

Topology	Circuit Configuration	Manufacturer	Model Number	Voltage Rating	Current Rating
2-level	3 x half-bridge	Microsemi	APTMC120AM55CT1AG	1.2 kV	42 A
	Six-pack	Wolfspeed	CCS050M12CM2	1.2 kV	59 A
3-level, NPC	3 x NPC	Microsemi	APTMC60TLM55CT3AG	1.2 kV	40 A
3-level, T-type	3 x half-bridge	Microsemi	APTMC120AM55CT1AG	1.2 kV	42 A
	6 x discrete	Microsemi	APT70SM70B	700 V	41 A

Based on the datasheet values, a double conversion efficiency only considering device loss has been compared. A gate resistor (R_g) largely impacts the switching dynamics and switching-loss tables with 20 ~ 25 Ω were provided in the datasheets. Contribution of conduction-loss varies depending on a junction temperature and 50°C has been selected for the comparison. The total device loss depending on switching frequency (f_{sw}) is plotted in Fig. 5-2. The two-level topology shows high efficiency in $f_{sw} < 30\ kHz$ as three-level topologies suffer from the increase in the conduction-loss. When f_{sw} goes over $30\ kHz$, three-level topologies start to have a benefit on the total loss due to smaller switching-loss. Note that, due to the large gate resistance used for a switching-loss table in the datasheet, the double-conversion efficiency was underestimated. In the actual experiment, near zero external gate resistors were connected and switching-loss was low enough to achieve high efficiency.

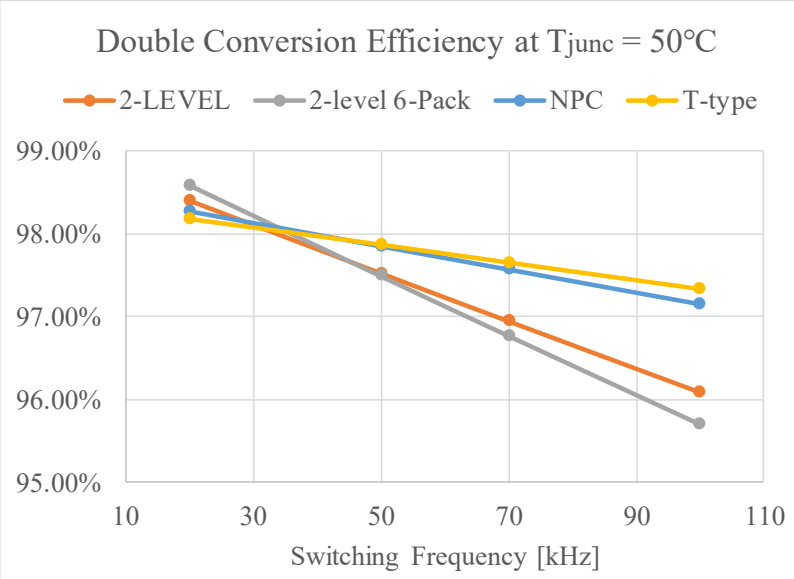


Fig. 5-2. Comparison of the double conversion efficiency based on the datasheet for different switching frequency range.

The NPC module has been selected for the final phase leg design. The three-level topology enables the operation at the higher switching frequency and the size of the passive components can be minimized. Based on the simulation result, the efficiency of NPC could be comparable to the T-type case. Also, parasitic inductances for interconnections among SiC MOSFETs can be minimized, which may bring benefit on mitigation of electromagnetic interference (EMI) and switching loss.

5.3 Gate Driver Design and Double Pulse Test

A gate driver has been designed for the NPC module. The architecture of the gate driver is shown in Fig. 5-3. More details can be found in the Appendix. A. For immunity of common-mode noise generated by fast switching of SiC devices, isolated dc-dc converters with low isolation capacitance($< 3\ pF$) are used to support the gate driving voltage for each MOSFETs.

There are 6 power planes. From the 24 V input, the isolated dc-dc chip generates 24 V bus. From this bus, 5 V plane is generated for primary-side of gate driver ICs and fiber optics. For 4 SiC-MOSFETs of a NPC phase leg, four MG2J242005SC from Murata are used to generate 20 V/ -5 V. With this structure, 5 V for control logic can be protected from noise generation by high dv/dt [126].

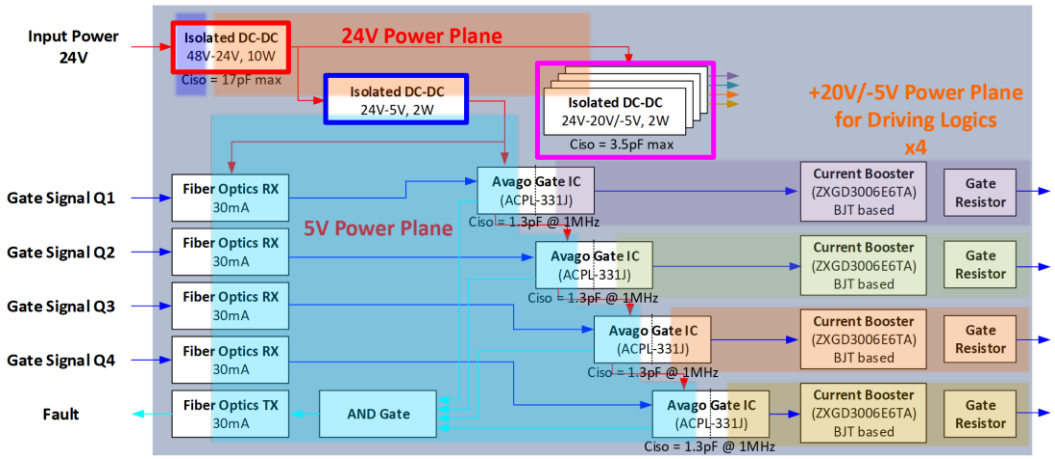
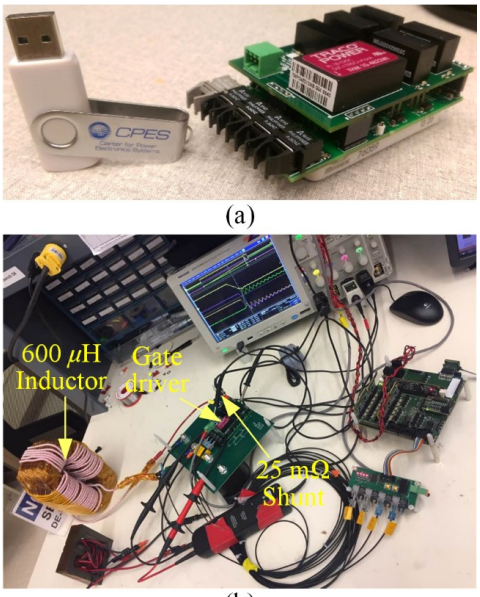


Fig. 5-3. The architecture of the prototype gate driver.

A picture of the prototype gate driver is shown in Fig. 5-4(a). 600 μH inductor is used as a load inductor. Test setup for DPT is shown in Fig. 5-4(b). Waveforms for turn-on and turn-off instant at 40 A, 400 V with different R_g values are shown in Fig. 5-5. Maximum dv/dt is 26.4 V/ns while di/dt is 4.14 A/ns when R_g equals to 0.05 Ω. The switching-loss measured is shown in Fig. 5-6(a) and compared to the datasheet value where $R_g = 25\,\Omega$. The switching loss can be significantly smaller with minimal R_g. It can be inferred that the efficiency based on the datasheet in Fig. 5-2 is underestimated.



(a)

(b)

Fig. 5-4. A picture of (a) the prototype gate driver, and (b) DPT setup.

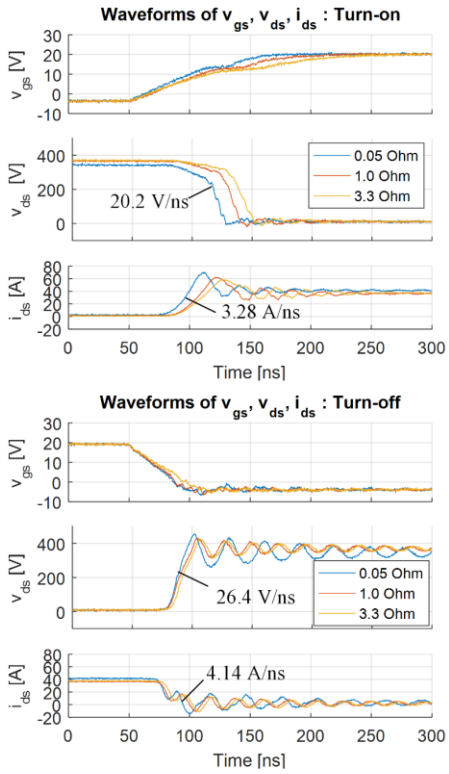


Fig. 5-5. Switching waveform with the designed gate driver.

5.4 Switching Frequency Decision and Filter Design

Based on the experimental switching-loss data, the efficiency simulation has been performed to determine the switching frequency. Since the on-drop of the MOSFETs and neutral point clamping diodes is highly dependent on the junction temperature as shown in Fig. 5-6(b), a lumped parameter thermal simulation has been performed to estimate the temperature rise. The lumped parameter thermal circuit for the simulation is shown in Fig. 5-7. $T_{j,Q1} \sim T_{j,Q4}$ refer to the junction temperature of 4 SiC MOSFETS in a single NPC phase leg. $T_{j,CR5} \sim T_{j,CR8}$ indicates the junction temperature of the diodes in APTMC60TLM55CT3AG module. T_{amb} is ambient temperature and assumed to be 25℃. $P_{sw,x}$ and $P_{cond,x}$ indicate the switching- and conduction-loss of a single power device. The thermal resistances of the module are summarized in Table 5-2. The three phase legs share a single heatsink, therefore, thermally connected. The rectifier and inverter have separate heatsinks and the two junction temperatures are not equal.

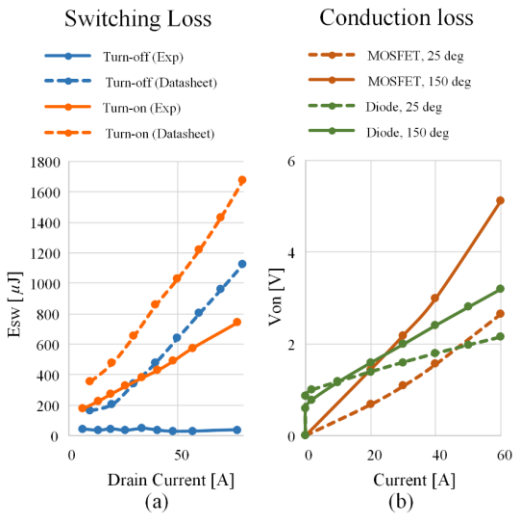


Fig. 5-6. (a) Switching-loss comparison when $R_g = 0.05\ \Omega$ (Experiment) and $R_g = 25\ \Omega$ (Datasheet), and (b) on-drop of SiC MOSFET and neutral point clamping diodes depending on the junction temperature.

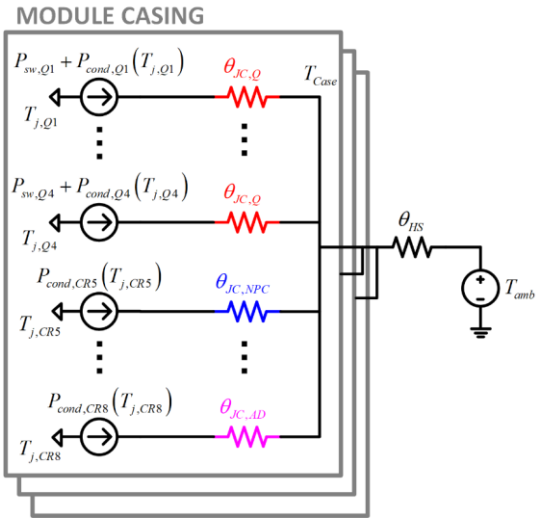


Fig. 5-7. A lumped parameter thermal circuit for a three-phase bridge.

Table 5-2. Summary of thermal circuit.

Parameter	Description	Value
$\theta_{JC,Q}$	Thermal resistance between SiC MOSFET and the module case	0.57 ℃/W
$\theta_{JC,NPD}$	Thermal resistance between the neutral point clamping diode and the module case	0.80 ℃/W
$\theta_{JC,AD}$	Thermal resistance between additional diodes in APTMC60TLM55CT3AG and the module case	0.50 ℃/W
θ_{HS}	Thermal resistance of heatsink with LFM 600	0.17 ℃/W

With given heatsink and fan design, the junction temperature of the rectifier-side heatsink reaches 65℃ while the inverter side reaches 81℃ at switching frequency of 60 kHz. Loss distributions among the power devices in one phase leg of the rectifier and inverter are shown in Fig. 5-8(a) and (b). The double conversion efficiency is 97.98% without considering the loss in the passive components.

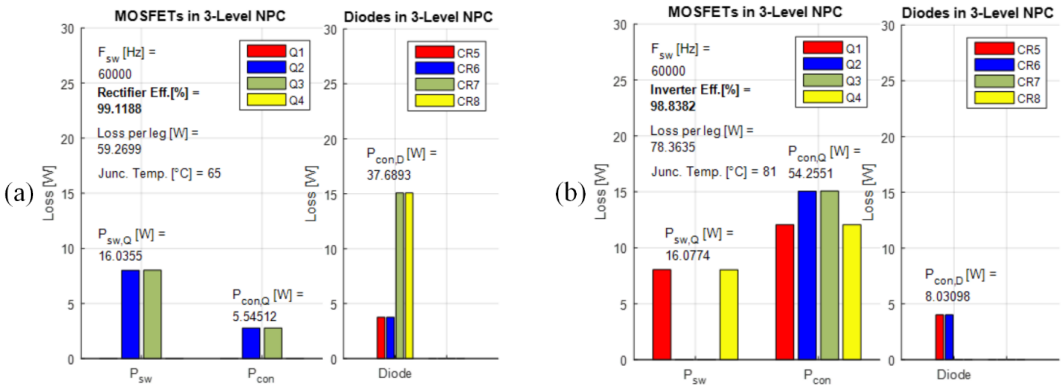


Fig. 5-8. Loss distribution within a NPC phase leg and junction temperature at switching frequency of 60 kHz (a) rectifier, and (b) inverter.

An LCL filter is designed to meet the THD requirement of UPS. The circuit diagram of the LCL filter is shown in Fig. 5-9. A RC circuit (R_d, C_d) is connected in parallel with the filter capacitor (C_f) for a passive damping. Converter-side inductors (L_{f1}) are exposed to 60 kHz

switching-ripple and require a low core-loss material. Three materials are considered to build the inductors: soft ferrite, amorphous, and nano-crystalline. Different sizes of a E-core of T and R material from Mag-inc. are considered for ferrites. For amorphous and nano-crystalline, AMCC and F3CC from Hitachi are used, respectively. A U-core structure and an E- core with 2 U-core pairs are considered for the tape wound cores. To estimate the core-loss per switching-cycle, the improved generalized Steinmetz equation (iGSE) has been used and the core-loss corresponds to the line-cycle current has been separately calculated [10].

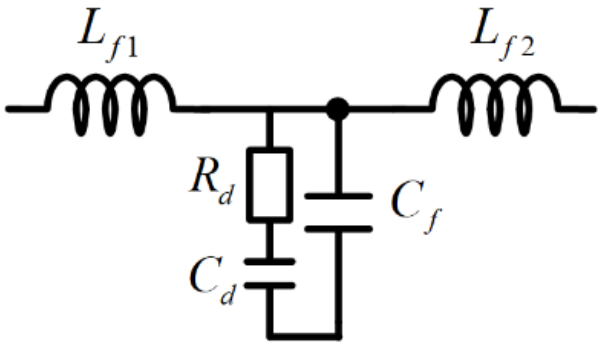


Fig. 5-9. Circuit diagram of LCL filter.

Optimization results including the conduction-loss estimation are shown in Fig. 5-10. At the switching frequency of 60 kHz, the amorphous core shows larger core-loss compared to the other materials. On the other hand, relatively small maximum flux-density (B_{max}) of ferrite material gives an increase in the size compared to the other two materials. When the size is comparable, a large air-gap had to be inserted and a large turns-number to meet the desire inductance results in high conduction-loss. Finally, the nano-crystalline material is selected for L_{f1}. For L_{f2}, no significant current ripple presents and the amorphous core is used. The parameters of the LCL filter and details of the final design are listed in Table 5-3.

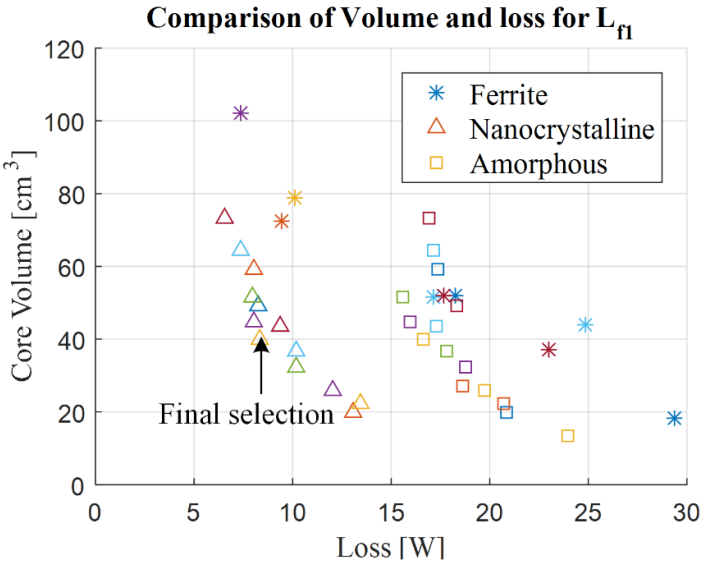


Fig. 5-10. Optimization of converter-side inductor.

Table 5-3. Details of LCL filter design.

Component	Value	Remark	Cost
L_{f1}	93 μH (0.003 p.u.)	F3CC-0063 x 2 Turn number: 16 Air gap : 1.0 mm Litz wire 37/500 (AWG 10 equivalent)	$ 654/kg
L_{f2}	40 μH (0.0013 p.u.)	AMCC-004 x 2 Turn number: 12 Air gap : 0.4 mm	$ 116/kg
C_f	3 μF	EPCOS (TDK) B32924A4155M000	$ 4.22 per each
C_d	0.68 μF	EPCOS (TDK) B32924A4684M000	$ 2.89 per each
R_d	47 Ω	Yageo FMP200JR-52-47R	$ 0.24 per each

With all designed components, estimated loss breakdown is shown in Fig. 5-11 for full-load. The conduction-loss from SiC MOSFETs and diodes takes around 64% of total-loss. The full-load efficiency has been estimated to be 97.6%.

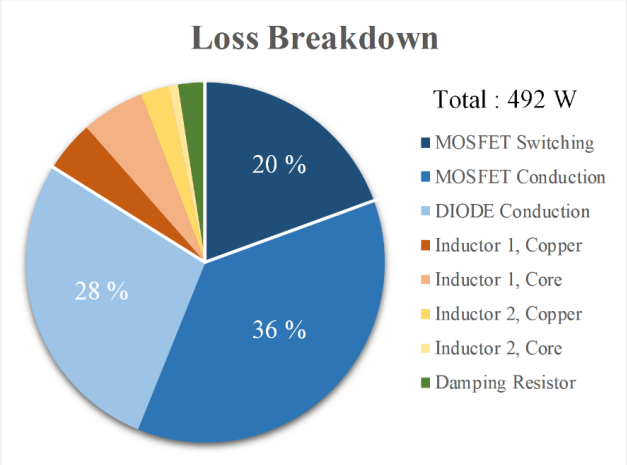


Fig. 5-11 Simulated loss breakdown at the full load.

5.5 Experimental Results

A prototype full-SiC 3-level UPS has been built. The circuit diagram of the prototype is shown in Fig. 5-12. A 3-level dc-dc converter [106] is built to interface a battery rack to the dc-link. The same NPC module is utilized for manufacturability. The picture of the prototype is shown in Fig. 3-2(a). The size of the assembly is 280 mm x 254 mm x 178 mm. For the dc-dc stage, two 247 μH inductors are built from powder cores. The efficiency of the dc-dc stage is 99.02% at full load. A detailed design process for the dc-dc stage is not covered in this work and can be found in [127]. A single 140 μF film capacitor with a low equivalent series inductance (ESL) is used per dc-link. MX45 from California Instrument is used as the input grid and three 11 Ω resistors are connected to the inverter to emulate three-phase load. Based on the DPT result, a dead-time is set to be 200 ns.

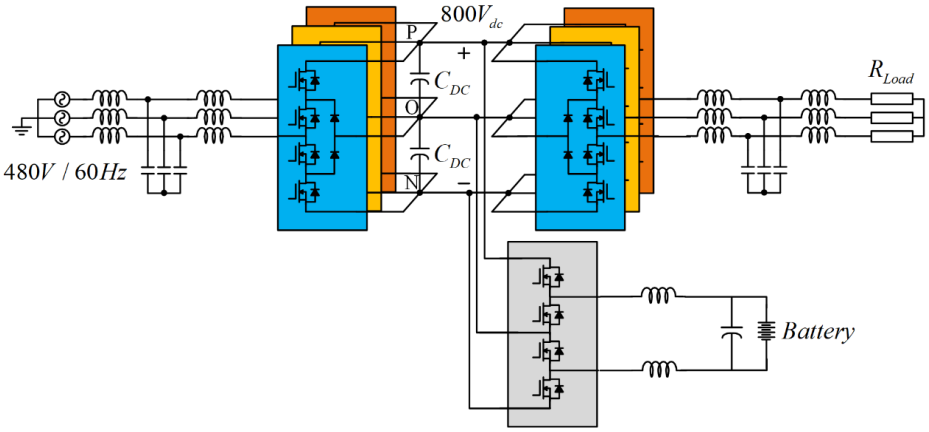


Fig. 5-12. Final circuit diagram of a full-SiC UPS.

The waveform of the inverter three-phase currents is shown in Fig. 5-13 when the rectifier and inverter operate in their 20 kW full power. Space-vector PWM is used for the modulation scheme. THD of the inverter-side currents is measured to 2.1%. The waveforms of inverter phase-A current, rectifier phase-A current, dc-link voltage, and the output capacitor voltages are shown in Fig. 5-14. THD of load-side voltage is 2.2%.

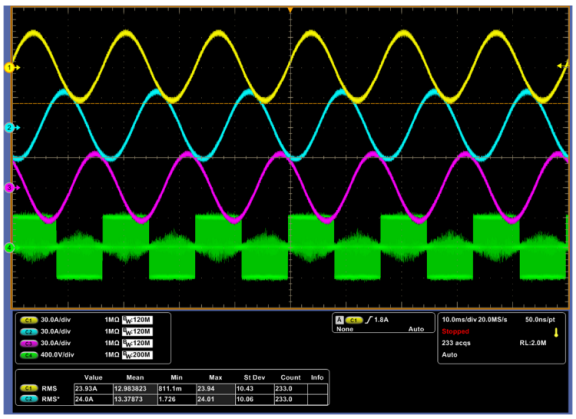


Fig. 5-13. Waveforms of inverter currents, CH1: Phase-A, CH2: Phase-B, CH3: Phase-C, CH4: Phase-A output voltage.

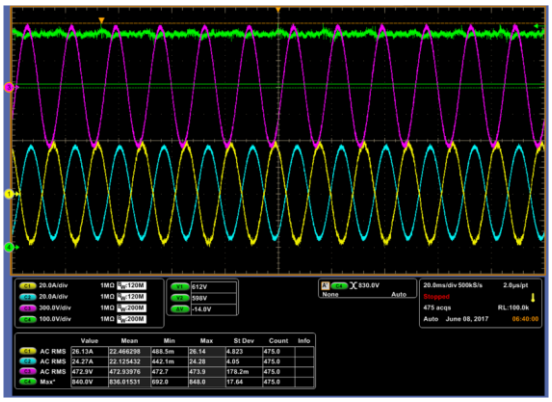


Fig. 5-14. Waveforms for double conversion CH1: Rectifier phase-A current, CH2: Inverter phase-A current, CH3: Load voltage between phase-A and -B, CH4: DC-link voltage.

A thermal rise of the heatsink is measured with a thermal camera when it reached the equilibrium. Two 24 V – 0.15 A fans provide cooling for each heatsink. The inverter-side temperature was higher in the simulation due to relatively higher conduction-loss in SiC-MOSFETs. In the experiment, the highest temperature on the inverter-side heatsink is measured to be 71℃. The simulation result shows 70℃ and both results matched well. The temperature of the LCL filter is measured and shown in Fig. 5-16. With small core-loss of nanocrystalline, the temperature of the converter-side inductor is measured to be lower than 55℃. Note that usage of nanocrystalline may give a burden on the cost as shown in Table 5-3.

However, amorphous can be too lossy at this high switching frequency, and size of ferrite core will be large compared to the other two materials.

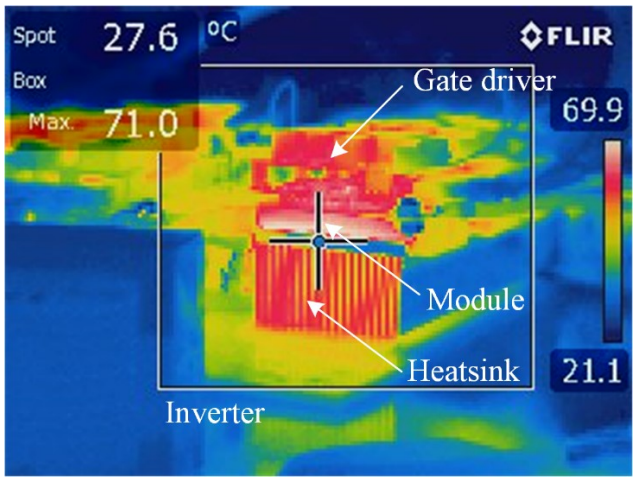


Fig. 5-15. Temperature of heatsink: Inverter-side.

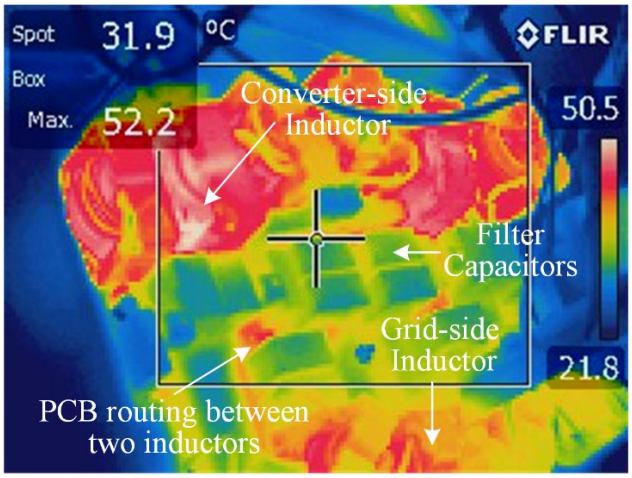


Fig. 5-16. Temperature of LCL filter.

The efficiency measurement has been done with Keysight Power Analyzer PA2203A. A capture when the UPS operates in full load is shown in Fig. 5-17. 97.57% efficiency can be achieved for the double-conversion. Several repetitive measurements have been done to ensure efficiency data. The result is in accordance with the simulation result which predicted 97.6%.

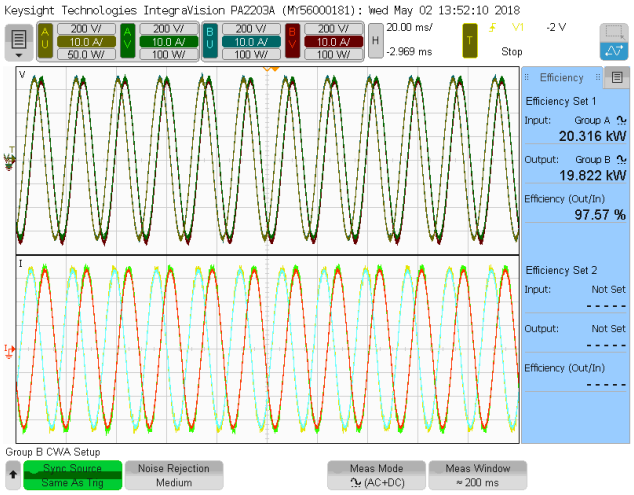


Fig. 5-17. Efficiency measurement at full load.

An efficiency curve has been extracted from 30% load to 100% load and shown in Fig. 5-18. It is compared with Si-IGBT based solution [128] and Si and SiC hybrid UPS [129] with the 3-level topology and similar power rating. It can be seen that the full-SiC prototype could achieve a 1% increase in the double conversion efficiency at the full load.

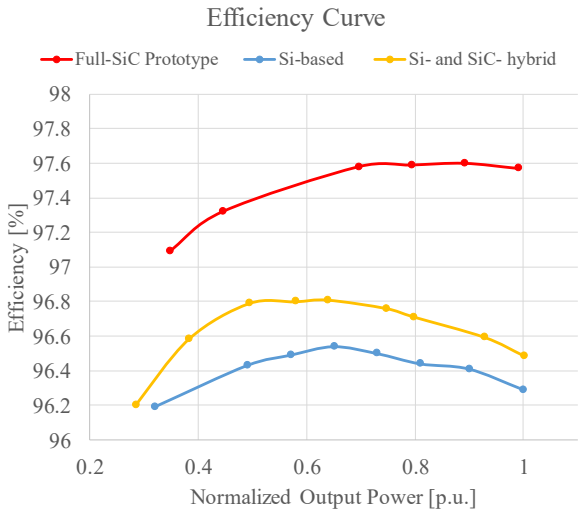


Fig. 5-18. Efficiency curve and a comparison with Si-based, and Si- and SiC- hybrid three-level UPS.

5.6 Chapter Conclusion

In this chapter, design of full-SiC, three-level, three-phase UPS has been presented for 480 V line. Different topologies are compared and NPC structure has been adopted considering the efficiency at the high switching frequency. A gate driver has been designed which achieves 26 V/ns and 4 A/ns maximum speed. To estimate the junction temperature, therefore conduction-loss, a lumped parameter simulation has been done for the thermal equivalent circuit. With 60 kHz switching frequency, LCL filter has been designed. With high switching frequency, the inductance value could be small but the material choice for the converter-side inductor was limited. Total loss breakdown shows that the conduction-loss of SiC MOSFETs and diodes dominates the overall loss. The prototype UPS has been built and tested. Thermal aspects of the heatsinks and filters are verified. THD of the output current is 2% and full load efficiency is 97.57%. Compared to Si-based UPS, or Si-IGBT and SiC diode hybrid solutions, the efficiency at full load showed 1% higher.

Chapter 6. Design Comparison on Three-level Three-phase 40 kW PV Inverter Operating in Continuous Conduction Mode and Triangular Conduction Mode

6.1 Chapter Introduction

Wide-bandgap (WBG) devices have seen high growth in power electronics markets for the past few years. With the early adoption of SiC or GaN devices into commercial products [130], [131], the reliability perspectives of such devices are expected to be verified in upcoming years. Renewable generations, such as photovoltaic (PV) generations, are applications where superior loss-characteristics of SiC devices can improve both efficiency and power density [3], [111], [132].

For tens to hundreds of kW-level PV farms, the PV inverters can be connected to the grid without any transformer to improve power density and efficiency, as shown Fig. 6-1. However, leakage current through the parasitic capacitors of the PV panels is limited to below 300 mA by standards. With conventional Si-IGBTs, three-level topologies such as neutral point clamped (NPC) or T-type are widely adopted to limit the leakage current. Owing to their multi-level voltages, the size of the filter for switching-frequency ripple can be reduced. Also, the common-mode (CM) filter for electromagnetic interference (EMI) and leakage current can be minimized. The benefit of SiC-MOSFETs three-level inverters is demonstrated in [43], [133] for these transformer-less PV inverters. The peak efficiency of a SiC-based solution can reach over 99%, while the power density shows a significant improvement, compared to Si-IGBT

inverters. However, the switching frequency (f_{sw}) of inverters in continuous conduction-mode is limited to below 70 kHz, due to the EMI concern; most EMI standards ask to limit noise starting at 150 kHz.

On the other hand, the switching loss of the SiC MOSFETs is reported to be concentrated on the turn-on instant [48], [134], [135]. An example of a full-SiC NPC module from Microchip is shown in Fig. 6-2. To further increase f_{sw}, thus power density of three-phase inverters, literature has investigated zero-voltage switching (ZVS) schemes which have been widely used in single-phase inverters [26], [136], [137] or dc-dc converters.

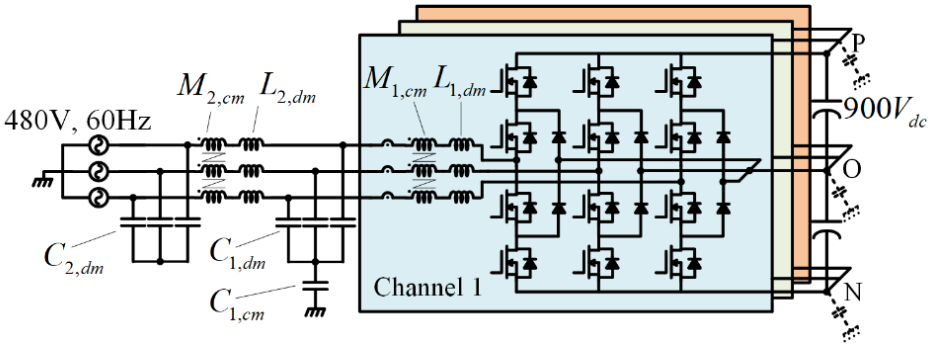


Fig. 6-1. Paralleled three-phase three-level inverters for PV panels.

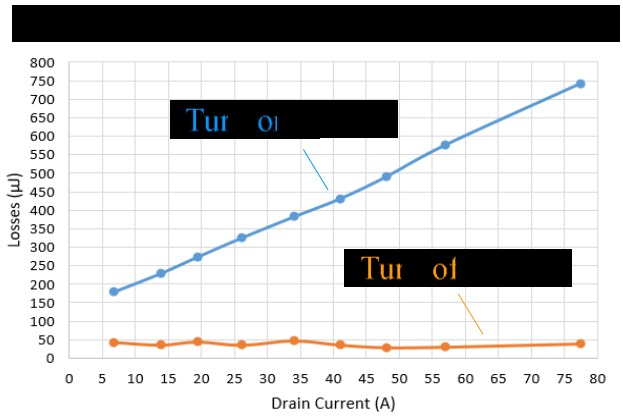


Fig. 6-2. Double pulse test result for the full-SiC NPC module: APTMC60TLM55CT3AG from Microchip.

In [48], [138], three-phases are decoupled through the additional capacitors. However, the modulation index (MI) is limited below 1, and the variation of f_{sw} along the line cycle is huge. In [139], an additional resonant circuit is added for ZVS, and 99% efficiency can be achieved even at 300 kHz. However, this scheme needs an additional passive component, and, a package for the 7-in-1 module was used as an effort to minimize the leakage inductances of the commutation path and overvoltage.

In [52], [140], the current ripple of carrier-based pulse-width modulation (PWM) has been analyzed. Without any additional components or zero-current detection (ZCD) circuitry, the ZVS can be achieved for most of the line cycle. However, the analysis presented is focused on the unity power factor (u.p.f.) case only.

In [27], [29], three conduction-modes are used to achieve ZVS of the three-phase inverters. Discontinuous conduction mode (DCM) and triangular conduction mode (TCM) are used for two-phases, and the other phase is clamped to positive or negative dc-rail. Also, its operation for non-u.p.f. has been verified [141]. However, this research works only focus on two-level topology. Furthering [27], [29], a TCM scheme for three-level topologies was proposed in [28]. The variation of f_{sw} along the line-cycle is limited to 10%. However, no detailed analysis was included to verify its benefit in the three-level inverter. A comparison with hard-switching in [124] showed the highest efficiency by the three-level TCM inverter, but the three-phases were decoupled which significantly impact f_{sw} range.

In this chapter, a detailed comparison in hardware design for a three-level inverter operating in CCM and a three-phase coupled TCM [28] is presented. With an identical full-SiC three-

level phase leg, f_{sw} was designed to achieve 99% efficiency. With the designed switching frequency, a guideline for an LCL filter design was presented. The benefit on EMI was compared with the CCM inverter case. An optimization procedure for the LCL filter and CM choke of the TCM inverter was investigated. The final filter design was compared between the CCM inverter and TCM inverter.

6.2 Switching Sequence for a Three-level Three-phase Inverter in Triangular Conduction Mode

In this section, the switching sequences for a three-level TCM inverter proposed in [28] are briefly described. Furthering [29] and [27], three different conduction-modes are utilized for three phases. Examples of time domain waveforms are shown in Fig. 6-3(a) and (b). The phase with the largest current is clamped to positive dc-rail or negative dc-rail depending on the current direction, which is similar to the discontinuous PWM (DPWM) scheme. The phase with the smallest current magnitude is operated in DCM and the other phase in TCM. The conduction modes of three-phases along the line cycle are shown in Fig. 6-4(a) for the u.p.f case. The variation of $t_{dcm,on}$, $t_{tcm,on}$, and T_{sw} within 30° is shown in Fig. 6-4(b) when the modulation index (MI) is 1. There exists only a 10% variation within 30°. As all 12 sectors in Fig. 6-4(a) are symmetric, the switching frequency is quasi-constant along the line-cycle.

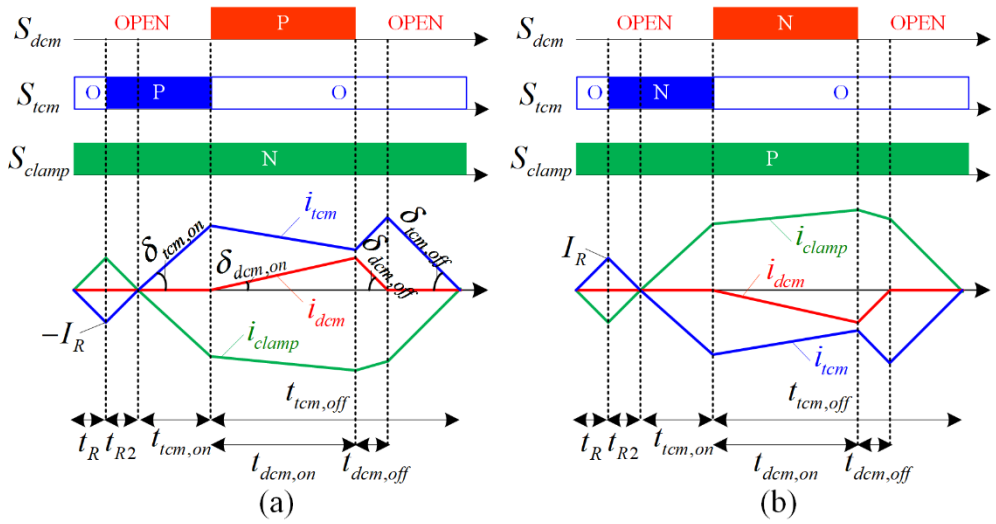


Fig. 6-3. Switching sequences for (a) clamped to negative dc-rail, and (b) clamped to positive dc-rail.

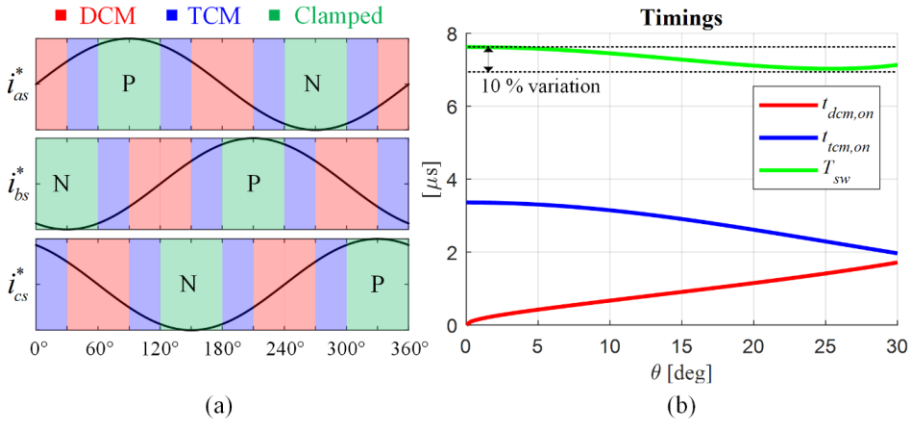


Fig. 6-4. (a) Conduction-modes of three-phases along the line-cycle, and (b) variation of $t_{dcm,on}$, $t_{tcm,on}$, and T_{sw} within 30°.

6.2.1 Operation of TCM phase

For the TCM phase, O-state time is extended after zero-current detection (ZCD) of clamped phase current $\left(i_{clamp}\right)$ by t_R to generate the reverse current $\left(I_R\right)$. Inherent signal-processing delays in the ZCD circuit and gate driver propagation delays are included in t_R [142]. Note

that the dead time where discharging of the junction capacitance occurs, is not shown in Fig. 6-3(b) and (c). The dead time has to be set long enough to ensure the discharging while the conduction-loss may increase if a duration for body diode conduction prolongs. After t_R, the P-state lasts for $t_{tcm,on}$ to build up the average current. During $t_{tcm,off}$, the current falls back to zero while the switching of the DCM phase impacts the slope during $t_{dcm,on}$ and $t_{dcm,off}$.

6.2.2 Operation of DCM phase

When the switching state of the DCM phase (S_{dcm}) is "open", all four MOSFETs on a phase leg are turned off. For the switching sequence under analysis, S_{dcm} turns on synchronously when S_{tcm} transits from O-state to P-state and generates triangular current on the DCM phase. To build up the average current, $t_{tcm,on}$ is controlled. When S_{dcm} is "open", an oscillation between the output inductor and junction capacitances of MOSFETs may exist. By this oscillation, only partial ZVS can be achieved, and a parasitic ringing is present on the DCM phase current (i_{dcm}). However, the current at turn-on instant of the DCM phase is very small.

6.3 Comparison of Device-Loss

In this section, the device loss from SiC MOSFETs is compared for the CCM and TCM inverter case. A full-SiC neutral-point-clamped (NPC) module is chosen for comparison. A 1.2 kV, 42 A full-SiC module (APTMC60TLM55CT3AG) from Microchip is used to realize the phase leg for both CCM and TCM inverters. The double pulse test result is shown in Fig. 6-2. At rated current, the turn-on loss was 12 times higher than turn-off loss.

A PLECS simulation was performed to evaluate both switching-loss and conduction-loss for a single 3-level inverter operating in CCM and TCM. With a large number of power devices in the three-level circuit, the dynamics of resonance from the DCM phase is not easy to predict, especially in the design stage. In this loss simulation, the DCM phase is assumed to switch at zero voltage without parasitic ringing. Even though the MOSFETs may switch at partial ZVS, the current flowing through the MOSFETs are near zero except for a small ringing current. Also, the ringing voltage will be divided into series-connected MOSFETs in the three-level phase leg, and the partial turn-on loss from the DCM phase may not be significant.

For both CCM and TCM cases, f_{sw} is pushed as high as possible while the efficiency remains over 99%, only considering semiconductor losses. To meet a 40 kW power rating, two inverters are paralleled for the CCM case. Three inverters are paralleled in the TCM case to mitigate the increase in conduction-loss by high current ripple. As a result, a single channel processes 20 kW in the CCM inverter and 13.3 kW in the TCM inverter.

At the junction temperature of 75°C, the loss distribution within the phase leg is shown in Fig. 6-5. The total loss from devices considering the paralleled inverters is summarized in Table 6-1. With ZVS operation, f_{sw} in the TCM case can be increased to 144 kHz from 40 kHz in the CCM case, while the efficiency of the three-phase bridges maintains 99%.

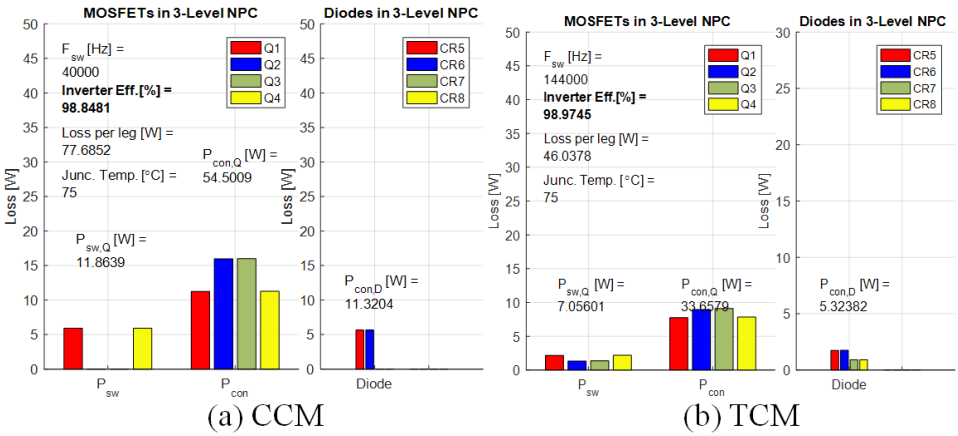


Fig. 6-5. Loss distribution within a single NPC phase leg (a) CCM, and (b) TCM.

Table 6-1. Device loss from SiC MOSFETs in two modulation method.

	CCM	TCM
Switching-loss [W]	72	77.4
Condition-loss [W]	395	311
Total loss [W]	466	388.8

6.4 Filter Designs

6.4.1 Design criteria of LCL filter

An LCL filter is selected to meet the total rated-current distortion (TRD) requirement in IEEE-1547 [143]. The 1st inductor $(L_{1,dm})$ is placed at each inverter output to limit the current ripple or provide controllability of each inverter current. The capacitor $(C_{1,dm})$ and 2nd inductor $(L_{2,dm})$ of the LCL filter are placed after the point of common coupling (PCC) to maximize benefits of the ripple cancellation by interleaving, as shown in Fig. 6-1. Zero-sequence circulating currents (ZSCC), provoked by interleaving, can be attenuated by CM chokes or coupled inductors. CM chokes are chosen in this comparison. Without the coupling

between the inverters, only one or two inverters can run at light load condition to improve the efficiency.

In the following section, the focus is on the design of the LCL filter in the TCM case. Different criteria are used for the filter design. With TCM operation, $L_{1,dm}$ determines the f_{sw} range with a given output power. A variation of f_{sw} within a line cycle is shown in Fig. 6-6, depending on the inductance and output power. For 13.3 kW per channel, 9 μH inductance is required to limit f_{sw} below 140 kHz. The CM choke to block the ZSCC will provide its leakage inductance $\left(L_{1,cm,lk}\right)$, and the summation of this leakage component and $L_{1,dm}$ has to meet 9 μH. The leakage inductance of the CM choke can be analytically estimated once the physical dimension of the toroidal core is determined [144].

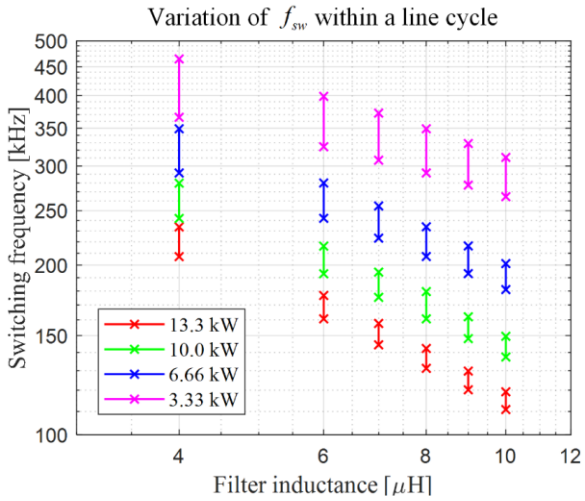


Fig. 6-6. Switching frequency range depending on filter inductor.

The dc-link voltage and the voltage across $C_{1,dm}$ determine the slope of currents on $L_{1,dm}$. Thus, the dynamics of the TCM inverter are sensitive to the variation of these voltages. To

ensure proper operation of the TCM inverters, $C_{1,dm}$ has to be large enough so that the voltage across the capacitor does not deviate from its nominal value during the transient response. Also, an oscillation at a resonant frequency of the LCL filter has to be properly damped. On the other hand, the capacitance should not be too large that reactive currents at no load condition is limited. Lastly $L_{2,dm}$ is designed to provide enough attenuation to meet TRD.

At full load, the inverter current contains a large current ripple by the TCM operation. The THD of a single channel may reach 100%. However, interleaving among three channels effectively cancels out each other, and the THD of the total current flowing toward PCC significantly reduces. The simulated waveforms with paralleled channels are shown in Fig. 6-7. The THD of the total current at PCC is 13% in the CCM case and 17% in the TCM case. As a result, high-frequency current-ripple through $C_{1,dm}$ may not be excessive.

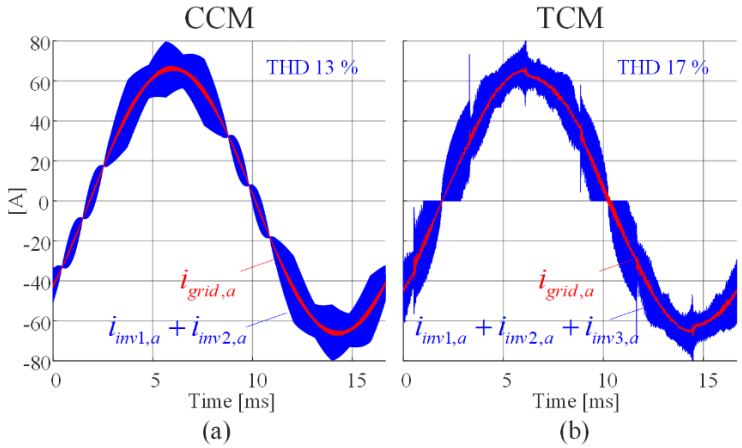


Fig. 6-7 Simulation waveform: The summation of phase-A current for paralleled inverters and grid-side current (a) CCM case, and (b) TCM case.

The design of the LCL filter for the CCM inverters followed criteria in [145]. A design criterion for $L_{1,dm}$ is to limit the current ripple of the inverter current to 20%. According to the

TRD goal and limitation on the reactive power at the rated condition, $C_{1,dm}$ and $L_{2,dm}$ are designed. The parameters for the LCL filters are summarized in Table 6-2. The main boost inductor $(L_{1,dm})$ in the TCM case shows a significant reduction in inductance value.

Table 6-2. Parameters for LCL filter design.

Parameters	CCM	TCM
$L_{1,dm}$	51 μH	9 μH
Peak current for $L_{1,dm}$	40 A	56 A
$C_{1,dm}$	1.6 μF	5 μF
RMS current for $C_{1,dm}$	6.82 A	7.7 A
$L_{2,dm}$	22 μH	5.6 μH

6.4.2 Design of CM choke for suppression of circulating current and CM EMI

The switching sequence design in [28] assumes that no ZSCC flows among the inverters. A presence of a large ZSCC will disrupt the zero-current detection (ZCD) instant. Once the ZCD signal is disrupted, the volt·sec balance on $L_{1,dm}$ may not be guaranteed. In particular, when the clamping direction changes every 60°, a step change in on the ZSCC exists [58] since the clamping directions become different among the paralleled inverters. Without a modification on the switching sequence, the passive filters such as the CM chokes have to limit the magnitude of this jump. The magnitude of the jump can be written as (6.1) where $T_{sw}|_{\theta=0^\circ}$ indicates the switching period at sector change at 0°. The size of the CM choke has to be designed to withstand a bias current during the transient.

$$\Delta i_{cir,cm1} = \frac{V_{dc}}{3}\frac{1}{2L_{1,dm}+6M_{1.cm}}T_{sw}\Big|_{\theta=0^\circ} \qquad (6.1)$$

As shown in Fig. 6-4, the change in clamping direction occurs at k*60° where k = *0, 1, ... 5*. For the UPF case, the DCM current is zero, and only the TCM and clamped phase switches. In the case of two parallel TCM inverters, the switching states at 60° are shown in Fig. 6-8 for phase-A and phase-B. Zero current flows on phase-C in DCM, and the phase-C does not switch. After $T_{sw1}[k]$, the two phases of inverter 1 change their conduction-mode. When the inverter 2 changes its clamping direction at the beginning of $T_{sw2}[k+1]$, the ZSCC jumps similar to the CCM case in [58]. As mentioned, the mutual inductance of the CM choke $(M_{1,cm})$ and the size of the magnetic core have to be large enough to suppress the jump, and to withstand a transient bias current. In this work, $M_{1,cm}$ is set to 260 μH which limits the maximum jump below 1.5 A.

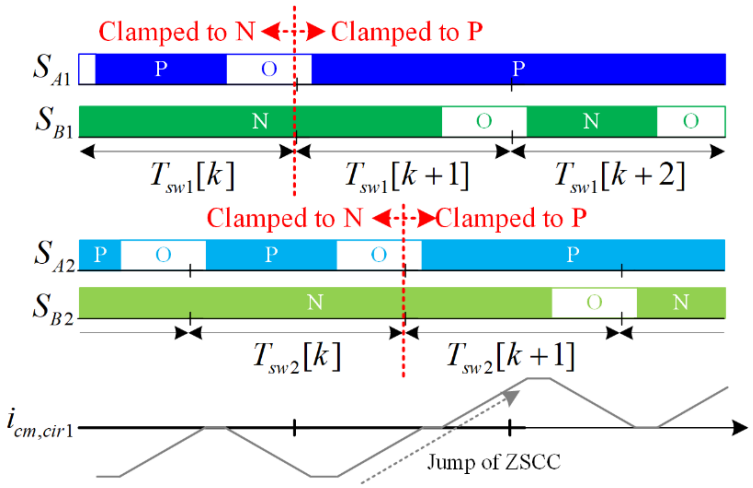


Fig. 6-8. Jump of zero-sequence circulating current at the instant of the clamping direction.

Another important consideration is the CM EMI. With the fast switching behavior of the SiC device, EMI and EMC strategy of SiC-based power electronics become more important. For the transformer-less PV inverters, the leakage current through the parasitic capacitance of

the PV panel has to be limited below 300 mA. This parasitic capacitance ranges from 50 nF ~ 150 nF / kW and reaches a few μF at tens of kW level. Also, an EMI standard such as IEC61000 has to be met. These two limitations enforce a large CM EMI filter to be added for the transformer-less PV inverters.

The frequency spectrum for the output voltage of the interleaved inverters is plotted in Fig. 6-9, and the CCM case and TCM are compared. The lowest emission frequencies between 150 kHz and 500 kHz are located at 160 kHz for the CCM case and 420 kHz for the TCM case. Dotted lines are drawn to illustrate required attenuation by the 2nd order EMI filter. With an elevated f_{sw} and interleaving, the TCM inverter benefits both on differential-mode (DM) and CM EMI. 20 dB less attenuation is required from the EMI filter. This will result in a significant reduction in the size of the magnetic core. Two observations should be noted. First, the impact of interleaving is included in the spectrum in Fig. 6-9. Without interleaving, the TCM inverter has high emission at f_{sw}. Second, a closed-loop interleaving algorithm for the three-phase TCM inverter should work properly to maximally utilize the benefit of interleaving.

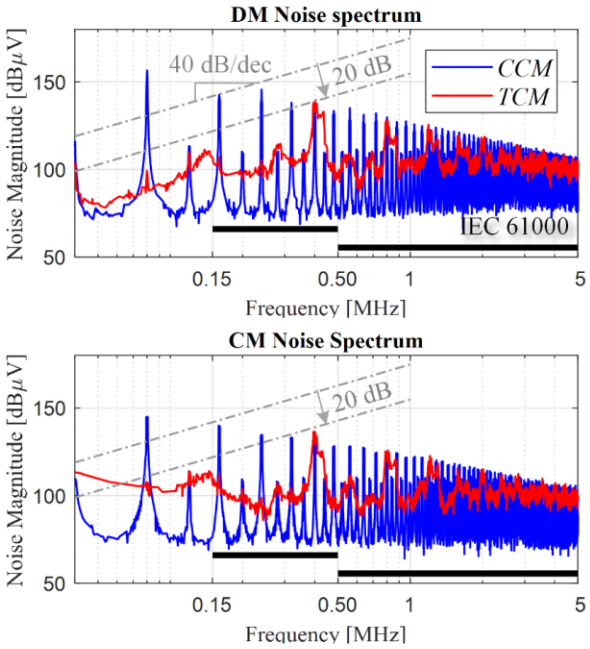


Fig. 6-9. Frequency spectrum of output DM and CM voltage for interleaved inverters.

6.5 Loss Evaluation and LCL Filter Optimization

Compared to CCM inverters, the increase in switching frequency by the ZVS operation and presence of high current-ripple brings a change to the LCL filter design. In this section, an analytic solution to calculate winding-loss and copper-loss for inductors of the TCM inverter is introduced. Also, a design guideline for sizing the CM choke is revealed. A final optimization result is compared between the CCM and TCM inverters.

6.5.1 Core-loss estimation

The waveform of the TCM current waveform is piecewise linear (PWL). For a PWL waveform, the improved Generalized Steinmetz Equation (iGSE) [146] can be used to estimate the core-loss. An example waveform is shown in Fig. 6-10. The original Steinmetz equation is

written as (6.2). For the minor-loop which is the single switching period in Fig. 6-10, the core-loss based on iGSE can be written as (6.3). According to (6.4), k_1 is calculated and ΔB is maximum peak-to-peak flux-density within the minor loop.

$$\overline{P_c} = k f^{\alpha} B^{\beta} \tag{6.2}$$

$$\overline{P_c} = \frac{k_i}{T_{sw}} (\Delta B)^{\beta-\alpha} \int_0^{T_{sw}} \left| \frac{dB}{dt} \right|^{\alpha} dt \tag{6.3}$$

$$k_1 = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta-\alpha} \, d\theta} \tag{6.4}$$

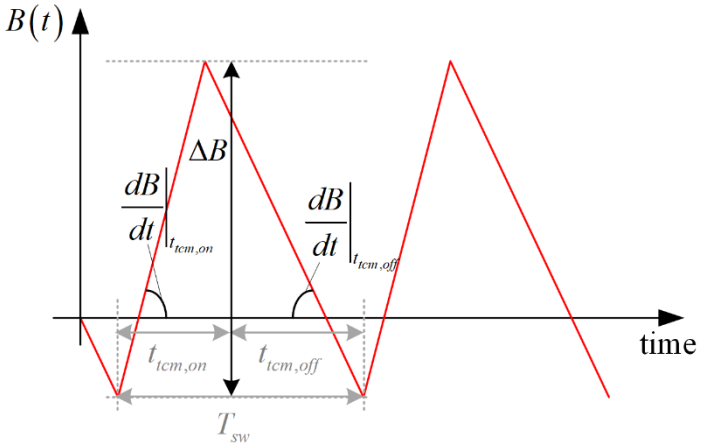


Fig. 6-10. Example waveform of flux-density to calculate the core-loss based on iGSE.

For the inverter-side inductor, the slopes of current, therefore dB/dt of the magnetic core, are determined by the capacitor voltage and dc-link voltage. In Fig. 6-3, the rising and falling slopes of the TCM phase when the DCM phase is off are defined as $\delta_{tcm,on}$ and $\delta_{tcm,off}$, respectively. On the other hand, the rising and falling slopes when the DCM phase operates are

defined as $\delta_{dcm,on}$ and $\delta_{dcm,off}$. The slopes for each time-period are summarized as Table 6-3. Capacitor voltages correspond to each conduction-mode are labeled as e_{clamp}, e_{tcm}, and e_{dcm}. For an example, e_{clamp} is phase-B capacitor voltage between 0° ~ 30°. A reverse of polarity for the clamping direction is defined as Pol, as shown in (6.5). The every slope can be generally represented by these four variables as in Table 6-3, considering the conduction-modes and clamping direction in Fig. 6-4.

$$Pol = \begin{cases} -1 & \text{if clamping to } P \\ +1 & \text{if clamping to } N \end{cases} \tag{6.5}$$

$$\begin{aligned} \delta_{tcm,on} &= \frac{Pol \cdot V_{dc} - \left(e_{tcm} - e_{clamp}\right)}{2L_{1,dm}} \\ \delta_{tcm,off} &= \frac{Pol \cdot V_{dc} / 2 - \left(e_{tcm} - e_{clamp}\right)}{2L_{1,dm}} \end{aligned} \tag{6.6}$$

$$\begin{aligned} \delta_{dcm,on} &= \frac{Pol \cdot V_{dc} / 2 - e_{dcm}}{L_{1,dm}} \\ \delta_{dcm,on} &= \frac{-Pol \cdot V_{dc} / 6 - e_{dcm}}{L_{1,dm}} \end{aligned} \tag{6.7}$$

Table 6-3. Current slopes for each time-period.

	$t_{R2} \sim t_{tcm,on}$	$t_{dcm,on}$	$t_{dcm,off}$	Rest of T_{sw}
TCM	$\delta_{tcm,on}$	$\delta_{tcm,off} - \frac{1}{2}\delta_{dcm,on}$	$\delta_{tcm,off} - \frac{1}{2}\delta_{dcm,off}$	$\delta_{tcm,off}$
DCM	0	$s_{dcm,on}$	$s_{dcm,off}$	0
Clamp	$-\delta_{tcm,on}$	$-\delta_{tcm,off} - \frac{1}{2}\delta_{dcm,on}$	$-\delta_{tcm,off} - \frac{1}{2}\delta_{dcm,off}$	$-\delta_{tcm,off}$

Based on Table 6-3 and timing information, a trajectory of the three currents can be analytically derived. The flux of the inductor is written as (6.8) where N is the turns-number and A_c is the cross-sectional area of the magnetic core. Note that required inductance for the inverter-side inductor is $L_{1,dm} - L_{1,cm,lk}$, not $L_{1,dm}$.

$$B = \frac{L_{1,dm} - L_{1,cm,lk}}{NA_c} i \tag{6.8}$$

In (6.3), ΔB can be calculated as Table 6-4. Since the current waveform is PWL, the integral term in (6.3) can be evaluated as Table 6-5. Note that the polarities of $\delta_{tcm,on}$ and $\delta_{dcm,on}$, or $\delta_{tcm,off}$ and $\delta_{dcm,off}$ are always the same, as shown in Fig. 6-3, under a given condition. From Table 6-4 and Table 6-5, the core-loss can be analytically predicted for given $L_{1,dm}$, N, and A_c.

Table 6-4. Analytic solutions for ΔB of iGSE.

	ΔB
TCM	$\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c} \lvert \delta_{tcm,on}(t_{tcm,on} + t_{R2}) \rvert$
DCM	$\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c} \lvert \delta_{tcm,on} t_{dcm,on} \rvert$
Clamp	$\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c} \left\lvert \delta_{tcm,on}(t_{tcm,on} + t_{R2}) + \left(\delta_{tcm,off} + \frac{1}{2}\delta_{dcm,on}\right) t_{dcm,on} \right\rvert$

Table 6-5. Analytic solutions for the integration term of iGSE.

	Integration term in iGSE
TCM	$\int_0^{T_{sw}} \left\lvert \frac{dB}{dt} \right\rvert^{\alpha} dt = \left(\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c}\right)^{\alpha} \left\{ \lvert \delta_{tcm,on} \rvert^{\alpha} (t_{R2} + t_{tcm,on}) + \left\lvert \delta_{tcm,off} - \frac{1}{2}\delta_{dcm,on} \right\rvert^{\alpha} t_{dcm,on} + \left\lvert \delta_{tcm,off} - \frac{1}{2}\delta_{dcm,off} \right\rvert^{\alpha} t_{dcm,off} + \lvert \delta_{tcm,off} \rvert^{\alpha} (t_{tcm,off} + t_R - t_{dcm,on} - t_{dcm,off}) \right\}$
DCM	$\int_0^{T_{sw}} \left\lvert \frac{dB}{dt} \right\rvert^{\alpha} dt = \left(\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c}\right)^{\alpha} \{ \lvert \delta_{dcm,on} \rvert^{\alpha} t_{dcm,on} + \lvert \delta_{dcm,off} \rvert^{\alpha} t_{dcm,off} \}$
Clamp	$\int_0^{T_{sw}} \left\lvert \frac{dB}{dt} \right\rvert^{\alpha} dt = \left(\frac{L_{1,dm} - L_{1,cm,lk}}{NA_c}\right)^{\alpha} \left\{ \lvert \delta_{tcm,on} \rvert^{\alpha} (t_{R2} + t_{tcm,on}) + \left\lvert \delta_{tcm,off} + \frac{1}{2}\delta_{dcm,on} \right\rvert^{\alpha} t_{dcm,on} + \left\lvert \delta_{tcm,off} + \frac{1}{2}\delta_{dcm,off} \right\rvert^{\alpha} t_{dcm,off} + \lvert \delta_{tcm,off} \rvert^{\alpha} (t_{tcm,off} + t_R - t_{dcm,on} - t_{dcm,off}) \right\}$

6.5.2 *Winding-loss estimation*

The RMS current to calculate a conduction-loss with the skin effect can be calculated based on the slope and timings shown in Table 6-3. To consider skin effect, a frequency spectrum of current harmonics has to be extracted which can be done through simulation.

6.5.3 *Optimization result*

The optimization is performed based on the design criteria in Section 6.4.1 and the loss evaluation in Section 6.5.1 and 6.5.2. The flowchart for the optimization is shown in Fig. 6-11.

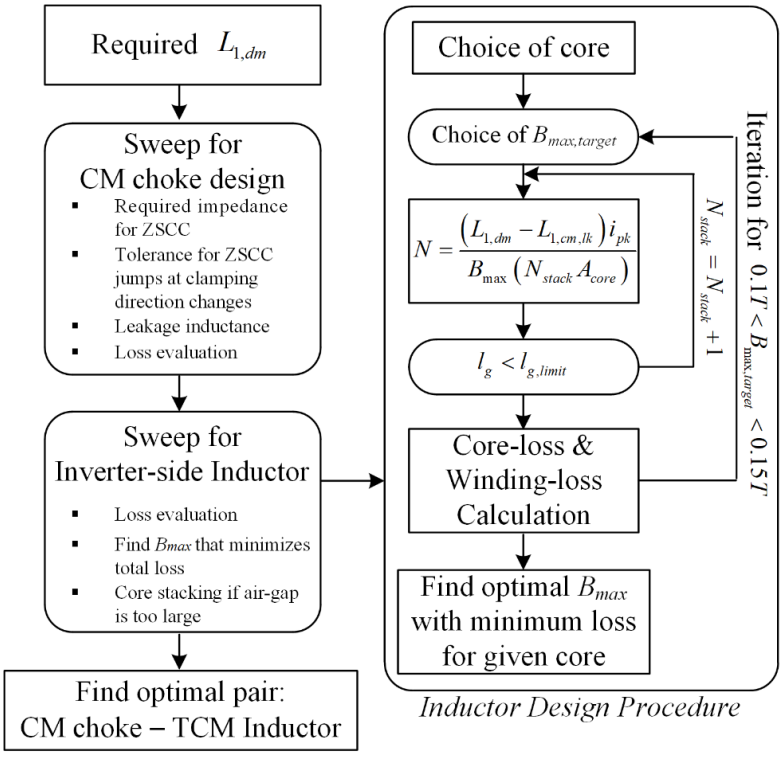


Fig. 6-11. Design procedure for a common-mode choke and inductor pair of TCM inverter.

Firstly, the required $L_{1,dm}$ is identified by the desired f_{sw} range. Then, the CM chokes are designed to guarantee that TCM operation is not interrupted by the ZSCC. From the simulation, the mutual inductance of the CM choke is designed to be 260 μH at f_{sw}. The ZSCC jumps at the change of clamping directions is calculated to be 1.5 A based on (6.1). The core is sized to tolerate bias current of 3 A. The leakage inductance of the CM choke $\left(L_{1,cm,lk}\right)$ is calculated based on the analytic solution in [144]. The value of $L_{1,cm,lk}$ should not exceed $L_{1,dm}$. With the high current peaking in inverter current waveforms, partial saturation may occur near the windings by $L_{1,cm,lk}$. The core-loss from such partial saturation is not included in this optimization result.

Secondly, the inverter-side inductor is designed. The required inductance is $L_{1,dm} - L_{1,cm,lk}$. As a first step, the magnetic core is selected, and the maximum flux-density $\left(B_{\max,target}\right)$ is chosen. The turns number and air gap are designed to meet the inductance and $B_{\max,target}$ when the number of the stacked core $\left(N_{stack}\right)$ is one. Due to the high peaking of TCM current and kW-level power, the required air-gap can be too large and may not be realizable. A maximum limit for the air gap $\left(l_{g,limit}\right)$ is set, and, if the calculated value goes over it, the additional magnetic core is stacked to reduce the air-gap. Once the parameters are determined, the winding-loss and core-loss are evaluated for a given design. To find an optimal $B_{\max}$ which gives the minimum loss, $B_{\max,target}$ is swept between 0.1 T and 0.15 T. The same procedure is done for the other sizes and shapes of the magnetic cores to compare loss and size. Even though

it is included in Fig. 6-11, an optimization for the grid-side inductors was done in a similar manner, but a powder core with high maximum flux density (> 1.2 T) is used.

The result of the optimization process for the inverter-side inductor and the CM choke is shown in Fig. 6-12. A final choice of the CM chokes and the inductors pair and the design parameters are summarized in Table 6-6 and Fig. 6-7. A nanocrystalline core is used for the CM choke and impacts total size significantly. To endure bias current of 3A and provide 260 μH at f_{sw}, the size of the CM choke was large. The value for $L_{1,cm,lk}$ is 5.6 μH. The maximum flux-density by its leakage inductance is 0.23 T. For the inverter-side inductors, a ferrite pot core is chosen for the TCM case.

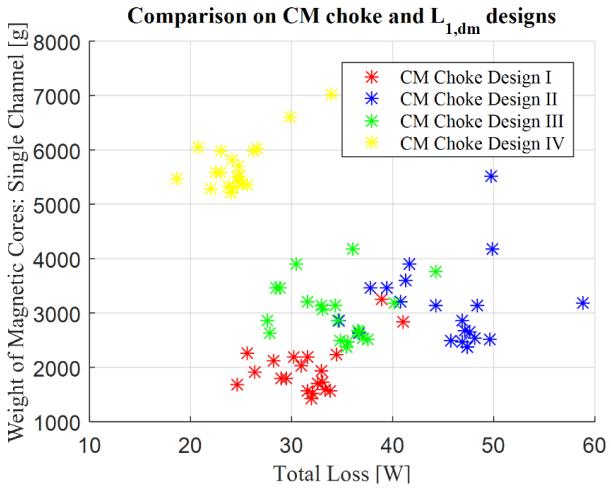


Fig. 6-12. Optimization result for common-mode choke and $L_{1,dm}$ design.

Table 6-6. Parameters for $M_{1,cm}$.

Parameter	Value
Part number	T60006-L2080-V091
$M_{1,cm}$	260 μH
$L_{1,cm,lk}$	5.6 μH
Turns number	6
Maximum bias	3 A
Total weight	459 g

Table 6-7. Comparison of inductor designs.

Parameter	CCM		TCM	
	Inverter-side Inductor	Grid-side Inductor	Inverter-side Inductor	Grid-side Inductor
Material	Amorphous	Powder core	Ferrite	Powder core
Part number	AMCC-06.3 for E-core	0078439A7	Pot core, 0T44229UG	0078586A7
Turns number	20	15	7	15
AWG	10	7	10	7
Air gap	1.624 mm	0 mm	2.5 mm	0 mm
B_{max}	0.31 T	0.55 T	0.105 T	0.58 T
Core weight	198 g	149 g	87 g	149 g
Core volume	66.7 cm^3	30.83 cm^3	41.5 cm^3	8.21 cm^3
Winding weight	97 g	87.4 g	64 g	45 g
Total weight	1770 g	709 g	1359 g	222 g

A comparison with the CCM inverter is summarized in Table 6-7. The weight of the inverter-side inductors is reduced by 24%, and the grid-side inductors by 69%, with the TCM operation. Note that the volume of the inverter-side inductor may not be significantly reduced. Available B_{max} of a ferrite material is limited compared to amorphous material, and the number of the inductors increases by the additional channel.

6.6 EMI Filter Design and Final Comparison

The high f_{sw} of the TCM inverter, along with interleaving, highly benefits EMI as shown in Fig. 6-9. The required attenuation from the DM/CM EMI filter was 20 dB less in the TCM inverter case. The equivalent circuits for DM and CM are shown in Fig. 6-13. A parasitic capacitance between the module output and the heatsink is C_s. The impedance of the LISN is

labeled as Z_{LISN}. The number of paralleled channels is defined as n which is 2 for the CCM case and 3 for the TCM case.

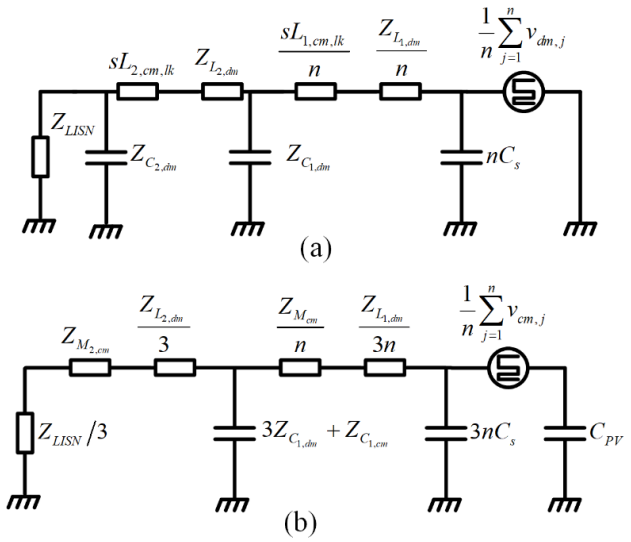


Fig. 6-13. Equivalent circuits for EMI analysis of (a) DM components, and (b) CM components.

Frequency spectra with EMI filters are shown in Fig. 6-14. In the CCM case, the resonant frequency of the LCL filter is located at low enough frequency, and the DM EMI can be met without an additional filter. However, CM noise has to be suppressed. Since an additional capacitor will induce more ground currents, a second CM choke $\left(M_{2,cm}\right)$ is added instead. On the other hand, CM noise in the TCM case is already below IEC61000 limits without any filter, with help from the CM chokes for the ZSCC. However, the relatively small inductance for the DM noise calls for additional filtering. Within a limit for reactive power, a large enough $C_{2,dm}$ can be added to shunt high-frequency DM noise. In summary, only $M_{2,cm}$ is added in the CCM case, and $C_{2,dm}$ in the TCM case.

Based on the simulation, the parameters for $M_{2,cm}$ and $C_{2,dm}$ are designed to meet IEC61000 with 6 dB margin in the CCM and TCM case, respectively. The results are shown in Fig. 6-14. The value for $M_{2,cm}$ is 115 μH and $C_{2,dm}$ is 2.5 μF.

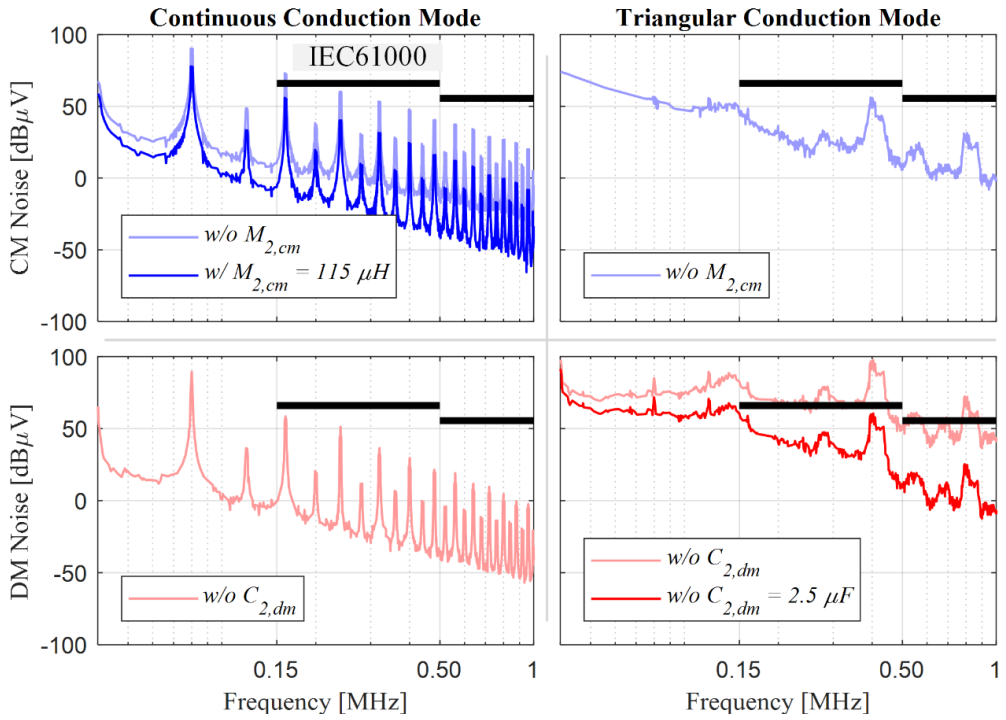


Fig. 6-14. Frequency spectra of DM, CM noise with or without EMI filter for CCM and TCM cases.

The optimization result for $M_{2,cm}$ is summarized in Table 6-8. With the designed filter components, the weight of the filter stage is summarized in Fig. 6-15. Total weight of the filter stage can be reduced by 15%. The reduction mainly comes from $L_{1,dm}$ and $L_{2,dm}$. However, the number of required $M_{1,cm}$ mitigates the benefit of weight reduction. The total loss of the filter stage is estimated and summarized in Fig. 6-16. The CCM case was 90 W and the TCM case was 50.7 W. The main reduction in the TCM inverters came from the reduction of core-

loss in $L_{1,dm}$ by the ferrite cores while the loss from the CM choke took a notable portion (43%).

The efficiency of the TCM inverter is 98.9% while the CCM inverter is 98.65%.

Table 6-8. Parameters for $M_{2,cm}$.

Parameter	Value
Part number	T60006-L2045-V118
$M_{2,cm}$	115 μH
Turns number	4
Total weight	164 g

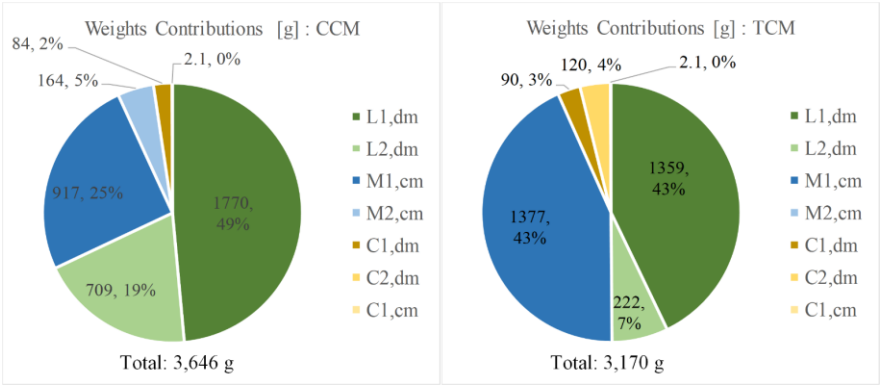


Fig. 6-15. Comparison on weight of filter components.

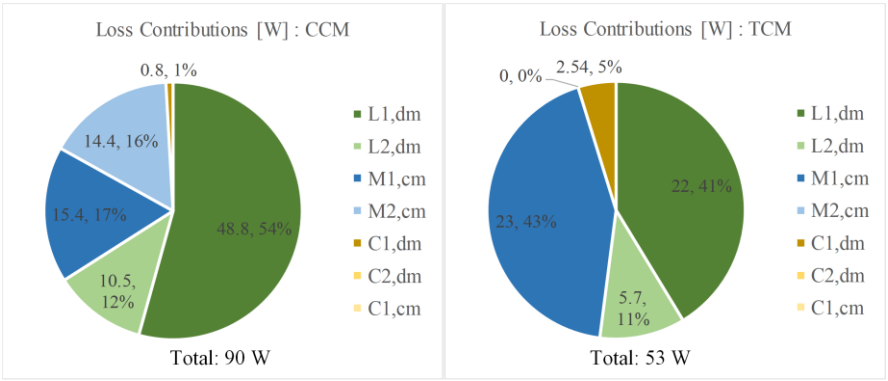


Fig. 6-16. Comparison on loss of filter components

6.7 Chapter Conclusion

In this chapter, hardware design of a 40 kW inverter operating in CCM and TCM was investigated. The switching frequency was set to achieve 99%, considering device-loss. A design guideline for an LCL filter design in the TCM inverter was presented. An analytic model for core-loss of the inductor of the TCM inverter was revealed. The optimization was done based on the analytic model. The weight of the inverter-side inductor shows a 33% reduction. However, with a limited material choice, the size does not see a significant decrease at high power and high frequency. EMI analysis shows a 20 dB reduction, compared to the CCM case. Total filter weight can be reduced by 15% while the efficiency can be maintained at 98.9%.

Chapter 7. Conclusions

After a long era of Si-IGBTs, the commercialization of SiC-based three-phase inverters is deemed to come to a close. One of the key factors to evaluate the technical progress of power electronics is power density, and the superior-loss characteristics of SiC MOSFETs have driven the power density of a grid-connected three-phase inverter to reach 3 ~ 4 kW/dm^3 or 50 ~ 66 W/in^3 level. An increase in switching frequency has brought a significant change in the contribution of each component on the total weight and size. Factors such as high EMI, limited increase in switching frequency, and the size of magnetic components, set barriers to further improvements of power density.

In this dissertation, techniques were investigated to reduce the size of the key components in full-SiC three-phase ac-dc converters. Within a general design procedure for three-phase inverters, techniques that can be used at each design step were proposed. Topology-wise, three-level topologies were investigated in most of the chapters.

This dissertation starts with a magnetic integration method for paralleled inverters. Since the current-rating of SiC devices are limited, the paralleling at device-level or converter-level is required to increase power capability. With interleaving among paralleled inverters, the size of the output boost inductor is reduced. However, coupled inductors, to suppress circulating current, mitigate the reduction in total volume and size. A systematical classification of harmonics is proposed on the frequency domain which classifies every harmonic into 4 groups; this is dependent upon circulating or flowing toward the load, or different-mode and common-mode. Extending a conventional integration method, three coupled inductors are integrated into

two: a differential-mode coupled inductor and common-mode coupled inductor. The proposed integration scheme utilizes widely-used core-shapes and can directly replace the conventionally coupled inductors with a 20% reduction in weight and size.

Techniques for three-phase full-SiC uninterruptible power supplies are shown in Chapters 3, 4, and 5. Multiple power stages within the UPS and various operation modes raise complexity in noise analysis. If the deliberate strategy is set before prototyping, the effort and cost for EMI handling can be minimized. Most notably, a noise interaction between the ac-ac stage and the dc-dc stage with a huge battery-rack was not clear. In Chapter 3, a common-mode equivalent circuit model was presented to predict the noise phenomena of the UPS in the design phase and highlights the impact from the dc-dc stage and a battery-rack. Based on the modeling, a topology and PWM scheme can be chosen as a mitigation strategy for the CM EMI, which will contribute to the optimization of the EMI filters on the ac- and dc-side, improving power density. When the dc-dc stage operates, the noise measurement showed that the CM EMI increases by 7 dB within a 150 – 500 kHz range and a maximum 40 dB over a 5 MHz range. With selected PWM schemes, the CM noise emission was reduced by a maximum of 16 dB within a wide frequency range.

Based on Chapter 3, a three-level topology was chosen for the ac-ac stage, and a PWM scheme to further improve the power density was proposed in Chapter 4. Two key components, which may take a considerable volume of a full-SiC three-level UPS, were targeted for size-reduction: a dc-link capacitor and a CM EMI filter. Through three different choices of injected zero-sequence voltage and polarity of carriers, the 4 out of 6 switching instances among the three-phases can be synchronized. The output common-mode voltage of the rectifier or inverter

stage can be shaped to a single pulse which maximizes the possible CMV cancellation between the two stages. The fluctuation of neutral point voltage can be compensated for both differential-mode and common-mode output voltage by a modification on zero-sequence voltage and carrier slopes. The experimental results showed a 4 dB reduction on CM EMI, which lead to a 30% reduction on the required CM inductance value. The compensation for neutral point voltage unbalance showed the reduction of grid-side current THD from 7.4% to 4.1% and a maximum 6 dB decrease on CM EMI over 1 MHz - 10 MHz range. When a 10% variation of neutral point voltage can be handled, the dc-link capacitance was reduced by 56%.

Chapter 5 presents an optimization procedure based on the work in Chapter 3 and Chapter 4. The double conversion efficiency of the ac-ac stage showed 97.6% which corresponds to 98.9% per stage. The dc-dc stage achieved 99.2%. The power density of the 20 kW prototype UPS was 1.53 kW/dm^3 without the EMI filter and auxiliary circuits. This is around a 50% improvement, compared to the state-of-the-art solution based on the Si-IGBT and SiC diodes.

Chapter 6 is dedicated to validating the benefits of soft-switching modulation on three-phase three-level grid-connected applications. By eliminating turn-on loss, the switching frequency of the three-level inverter can be increased from 40 kHz with hard-switching to 140 kHz with soft-switching. A change in the modulation and tripled switching frequency brings a design challenge for an LCL filter. A guideline was revealed for the three-phase soft-switching inverter. To enable an optimal filter design, an analytic solution to estimate the core-loss was shown. The reduction on the weight and volume of filters, including common-mode chokes for circulating current and EMI filters, were verified. The weight of the filter inductor was reduced by 36%; the weight of the EMI filter is reduced by 27%. The total filter weight is reduced by

15%. A large CM choke, to block the circulating current, and the components for an additional channel to mitigate conduction-loss, and impede further improvement on the power density. Projected efficiency and power density are 98.8% and 4 kW/dm^3, respectively, at a 40 kW level.

Appendix A. Gate driver for full-SiC three-level NPC module

From Chapter 3 to 6, a gate driver for full-SiC neutral point clamped (NPC) module is used. This appendix includes schematics of the gate driver. The schematic of the module (APTMC60TLM55CT3AG from Microchip) is shown in Fig. 3-18(b). The schematics of the gate driver are shown in Fig. A-1 ~ Fig. A-3. Fig. A-1 shows the overall schematic of the gate driver. 4 SiC MOSFETs (Q1 ~ Q4) in the module and a gate-source terminal of each is connected to a dedicated driving channel. There exists a separate PCB where driving voltages (+20V/-5V) are generated from the auxiliary power supply (+24V) and supplied to each of the driving channels. Three OR gates (NC7SZ08P5X) combine 4 fault signals from the 4 channels. The ORed fault signal is transferred to the digital controller by an optical fiber.

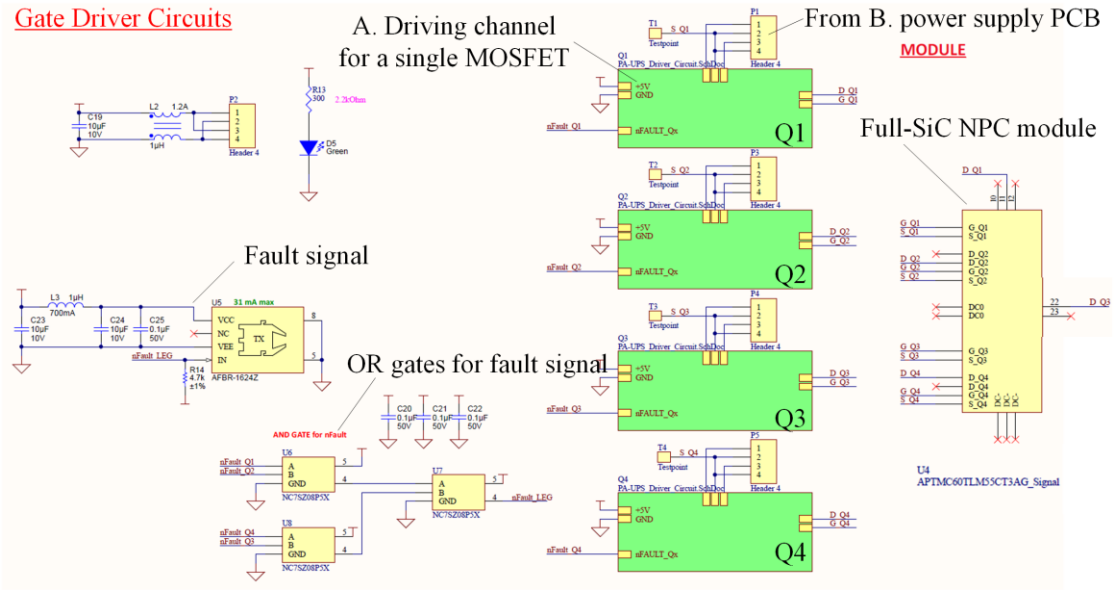


Fig. A-1. Overall schematic of gate driver for the full-SiC three-level module.

A schematic of the driving channel for a single SiC MOSFET is shown in Fig A-2. +5V for control logic and +20V/-5V for a gate driver are supplied from the power supply part in Fig. A-3. The gate signal is transmitted from the digital controller through the optical fiber, then delivered to the gate driver IC (ACPL-332J). A bipolar junction transistor (BJT) type current booster (ZXGD3006) amplifies a gate current to maximum 10 A for a fast switching dynamics.

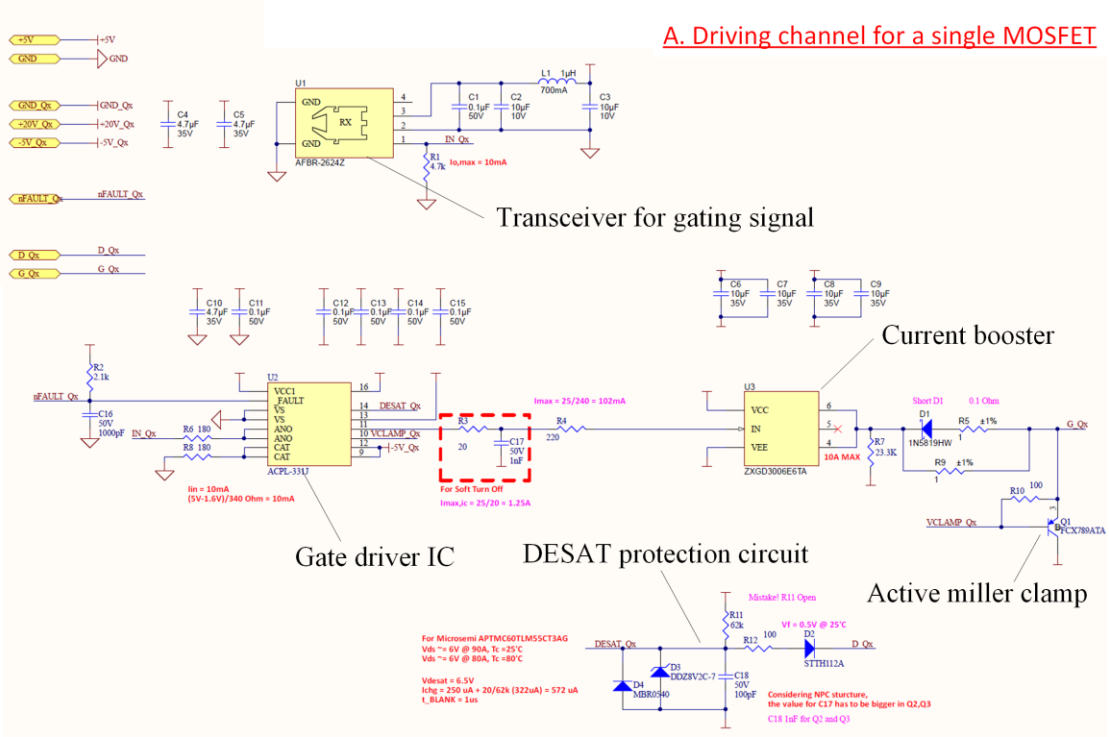


Fig. A-2. Schematic of a driving channel for a single SiC MOSFET.

An additional RC circuit between the gate driver IC and the current booster is to realize soft-turn-off (STO) functionality. When DESAT protection is activated, the value of internal resistance of the gate driver IC significantly increases. The capacitor of this RC branch is slowly discharged, and limit the amount of the magnitude of the gate current. A Schottky diode (1N5819) is added after the current booster to differentiate a gate resistance value for turn-on,

and turn-off instant. In the experiment, the same gate resistance values are used. A PNP bipolar transistor (FCX789ATA) functions as an additional current sink to realize an active miller clamp (AMC). A blanking time for a conventional DESAT protection indicates that the amount of time takes to charge the DESAT capacitor to the DESAT voltage. In the current design, the blanking time is 2.7 μs. This can be improved by connecting a resistor to the gate-source voltage, which will add a charging current when the gate signal is on.

The power supply part is shown in Fig. A-3. With the input voltage of +24 V, 24V bus is generated which feed 5 isolated power supply ICs. Due to high noise generation at the switching of SiC MOSFETs, the isolation capacitance of these power supply ICs plays a critical role for proper operation. Power supply ICs with 2 ~ 17 pF isolation capacitance is selected. A bill of material (BOM) is included at the end of Appendix. A. More details can be found from the datasheets provided by the manufacturers.

The designed gate driver comprises of two PCBs as shown in Fig. 5-4(a). The whole circuit is divided into the two PCBs to reduce the volume of the gate driver. The bottom contains the circuit for Fig. A-2. The circuit in Fig. A-3 is included in Fig. A-3. Note that the voltage potentials of the source node are floating and the connector between the top and bottom PCB may generate a radiative noise. The procedure for a double-pulse test of three-level NPC phase leg can be found in [147]. The waveforms in Fig. 3-22, and Fig. 6-2 are the results from the bottom-most MOSFETs, Q4.

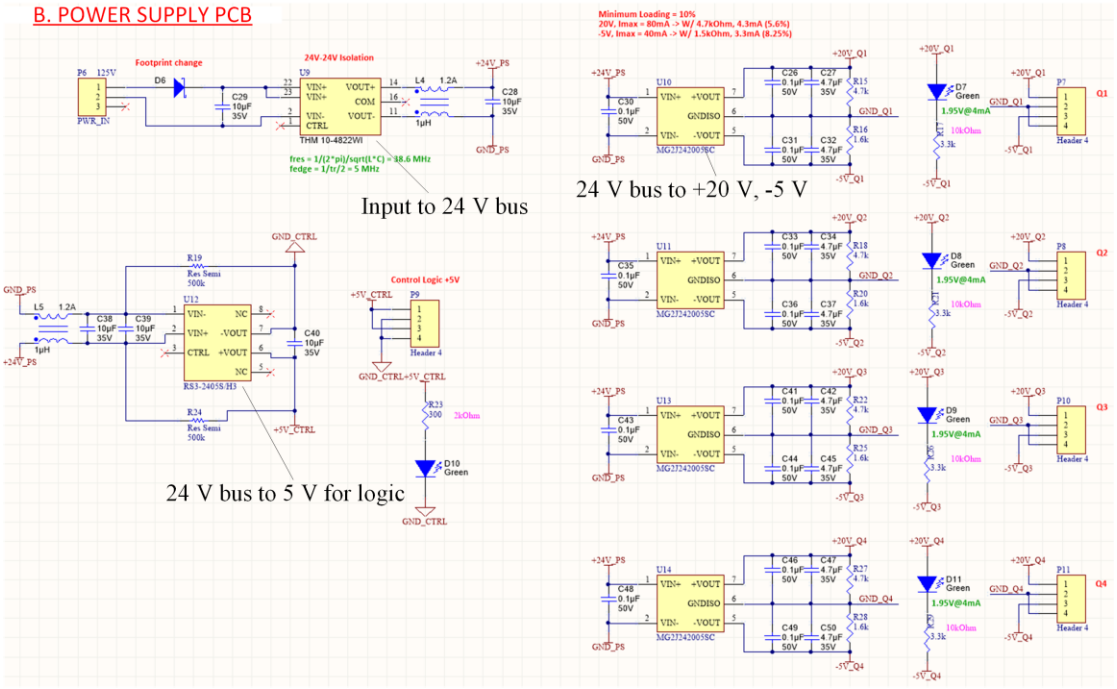


Fig. A-3. Schematic of a power supply part for the gate driver

Table A-1. Bills of Material (BOM) list for the full-SiC NPC gate driver

Comment	Description	Footprint	Quantity	Value
C1608X7R1H104K080AA	CAP CER 0.1UF 50V 10% X7R 0603	0603C	40	
C2012X7R1A106K125AC	CAP CER 10UF 10V 10% X7R 0805	0805C	11	
C2012X7R1V475K125AC	CAP CER 4.7UF 35V 10% X7R 0805	0805C	20	
C3216X7R1V106K160AC	CAP CER 10UF 35V 10% X7R 1206	1206C	21	
50V	Capacitor	0603C	12	1000pF, 1000pF, 1000pF, 1000pF, 1nF, 1nF, 1nF, 1nF, 100pF, 100pF, 100pF, 100pF
1N5819HW	DIODE SCHOTTKY 40V 1A SOD123	SOD-323F	4	
STTH112A	DIODE GEN PURP 1.2KV 1A SMA	SMA	4	
DDZ8V2C-7	Zener Diode	SOD-123	4	
MBR0540	Default Diode	SOD-123	4	
3V3 PWR	LED 555NM GREEN WTR CLR 0603 SMD	0603-LED-G	6	
MBR0580S1-7	DIODE SCHOTTKY 40V 1A SOD323	SOD-123	1	
MLZ1608N1R0LT000	FIXED IND 1UH 700MA 110 MOHM SMD	0603I	5	
744235601	CHOKE COM MODE 600 OHM 1.2A SMD	WE-1812	3	

Header 4	Header, 4-Pin	HDR1X4_MALE	5	
PWR_IN	TERM BLOCK HDR 3POS R/A 2.5MM	Phx_1881451	1	
Header 4	Header, 4-Pin	HDR1X4_Female	5	
PNP	PNP Bipolar Transistor	SOT89N	4	FCX789ATA
ERJ-3EKF4701V	Resistor	0603R	8	4.7k
RC0603FR-072K1L	Resistor	0603R	4	2.1k
RC0603JR-07100KL	Resistor	0603R	4	20
RMCF0805JT220R	Resistor	0603R	4	220
ERJ-1TRQF1R0U	RES SMD 1 OHM 1% 1W 2512	2512R	8	
Res3	Resistor	0603R	22	180, 180, 180, 180, 23.3K, 23.3K, 23.3K, 23.3K, 62k, 62k, 62k, 62k, 100, 100, 100, 100, 300, 3.3k, 3.3k, 300, 3.3k, 3.3k
RC0603JR-07180RL	Resistor	0603R	4	180
Res3	Resistor	0805R	4	100
MCR03ERTF4701	RES SMD 4.7K OHM 1% 1/10W 0603	0603R	1	
ERJ-3GEYJ162V	Resistor	0603R	4	1.6k
Res Semi	Semiconductor Resistor	AXIAL-0.5	2	500k
Testpoint		Testpoint	4	
AFBR-2624Z	RCVR OPT DC-50MBD 1MM POF	AFBR-2624Z	4	
ACPL-331J	Optocoupler	SO-16_N	4	ACPL-331J
ZXGD3006E6TA	IC GATE DRVR IGBT/MOSFET SOT26	SOT26A-6AM	4	
APTMC60TLM55CT3AG_Signal	SiC NPC MODULE W/ SP3 PKG	SP3 Package _ Signal	1	
AFBR-1624Z	TXRX OPT 650NM 1MM POF	AFBR-1624Z	1	
NC7SZ08P5X	TWO INPUT AND GATE	SC70-5	3	
THM 10-4822WI	Isolated DC/DC Converters 10W DC/DC 10kV REG 12Vin +/- 12Vout	TRACO_THM	1	
MG2J242005SC	Isolated Module DC DC	MGJ2 Sries	4	
RS3-2405S/H3	Isolated Module DC DC Converter 1 Output 5V 600mA 18V - 36V Input	SIP7	1	

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