Zero Voltage Switching (ZVS) Turn-on Triangular Current Mode (TCM) Control for AC/DC and DC/AC Converters

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ABSTRACT

One of the greatest technological challenges of the world today is reducing the size and weight of the existing products to make them portable. Specifically, in electric vehicles such as electric cars, UAVs and aero planes, the size of battery chargers and inverters needs to be reduced so as to make space for more parts in these vehicles. Electromagnetic Interference (EMI) filters take up a more than 80 % of these power converters, the size of these filters can be reduced by pushing the switching frequency higher. High frequency operation (> 300 kHz) leads to a size in reduction of EMI filters though it also leads to an increase in switching losses thus compromising on efficiency. Thus, soft switching becomes necessary to reduce the losses, adding more electrical components to the converter to achieve soft switching is a common method. However, it increases the physical complexity of the system. Hence, advanced control methods are adopted for today's power converters that enable soft switching for devices specifically ZVS turn-on as the turn-off losses of next generation WBG devices are negligible. Thus, the goal of this research is to discover novel switching algorithms for soft turn-on.

The state-of the-art control methods namely CRM and TCM achieve soft turn-on by enabling bi-directional current such that the anti-parallel body diode starts conducting before the device is turned on. CRM and TCM result in variable switching frequency which leads to asynchronous operation in multi-phase and multi-converter systems. Hence, TCM is modified in this dissertation to achieve constant switching frequency, as the goal of this research is to be able to achieve ZVS turn-on for a three-phase converter. Further, Triangular Current Mode (TCM) to achieve soft switching and phase synchronization for three-phase two-level converters is proposed. It is shown how soft switching and sinusoidal currents can be achieved by operating the phases in a combination of discontinuous conduction mode (DCM), TCM and clamped mode. The proposed scheme can achieve soft switching ZVS turn-on for all the three phases. The algorithm is tested and validated on a GaN converter, 99% efficiency is achieved at 0.7 kW with a density of 110 W/in^3.

The discussion of TCM in current literature is limited to unity power factor assumption, however this limits the algorithm's adoption in real world applications. It is shown how proposed TCM algorithm can be extended to

accommodate phase shift with all the three phases operating in a combination of DCM+TCM+Clamped modes of operation. The algorithm is tested and validated on a GaN converter, 99% efficiency is achieved at 0.7 kVA with a density of 110 W/in^3. TCM operation results in 33 % higher rms current which leads to higher conduction losses, as WBG devices have lower on-resistance, these devices are the ideal candidates for TCM operation, hence to accurately obtain the device parameters, a detailed device characterization is performed.

Further, proposed TCM+DCM+Clamped control algorithm is extended to three-level topologies, the control is modified to extract the advantage of reduced Common Mode Voltage (CMV) switching states of the three-level topology, the switching frequency can thus be pushed to 3 times higher as compared to state-of-the-art SVPWM control while maintaining close to 99 % efficiency. Two switching schemes are presented and both of them have a very small switching frequency variation (6%) as compared to state-of-the-art methods with >200% switching frequency variation.

Zero Voltage Switching (ZVS) Turn-on Triangular Current Mode (TCM) Control for AC/DC and DC/AC Converters

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GENERAL AUDIENCE ABSTRACT

Power supplies are at the heart of today's advanced technological systems like aero planes, UAVs, electrical cars, uninterruptible power supplies (UPS), smart grids etc. These performance driven systems have high requirements for the power conversion stage in terms of efficiency, density and reliability. With the growing demand of reduction in size for electromechanical and electronic systems, it is highly desirable to reduce the size of the power supplies and power converters while maintaining high efficiency. High density is achieved by pushing the switching frequency higher to reduce the size of the magnetics. High switching frequency leads to higher losses if conventional hard switching methods are used, this drives the need for soft switching methods without adding to the physical complexity of the system. This dissertation proposes novel soft switching techniques to improve the performance and density of AC/DC and DC/AC converters at high switching frequency without increasing the component count. The concept and the features of this new proposed control scheme, along with the comparison of its benefits as compared to conventional control methodologies, have been presented in detail in different chapters of this dissertation.

To my parents

My Father: Deep Haryani

My Mother: Vijaya Haryani

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With immense appreciation in my heart, I would like to express my sincerest gratitude to my advisor, Dr. Rolando Burgos, for his continued support and encouragement, since I have been at Virginia Tech. Also, I want to thank him for his critical challenges and high expectations from me during every discussion, which drove me to use a fresh mind every time to pinpoint the problem, to self-examine my research work, and then seek for further improvement, instead of stopping by the satisfaction of the existing achievement. I have learned so much from his rich knowledge, logical thought and devoted attitude towards research, it will certainly influence my future career.

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Chapter 1. Introduction

This chapter presents the motivations, objectives and overview of this dissertation. First, the latest trend and the requirements of high-density converters are discussed. The challenges and limitations of state-of-the-art hard switching continuous conduction mode (CCM) and pulse width modulation (PWM) are discussed. It is shown that soft switching is required to maintain high efficiency for power electronic converters operating at high switching frequency ranges. The need to push power converters to high switching frequencies comes from the drive to achieve higher power density as high frequency operation leads to a significant decrease in filter volume which consumes most of the space in power converter systems. It is also discussed how in wide bandgap devices soft switched turn-on is more essential than soft switched turn-off. A survey of the existing soft switching schemes is presented, followed by the dissertation outline and the scope of research.

1.1 Research Background

High performance power electronic converters are the heart of today's fascinating electrical grids, aerospace systems and servers as shown in Fig. 1.1. To understand the challenges of the converters' requirements for these high performance electrical systems, the latest trend of electrical systems and the need for high density will be discussed first.

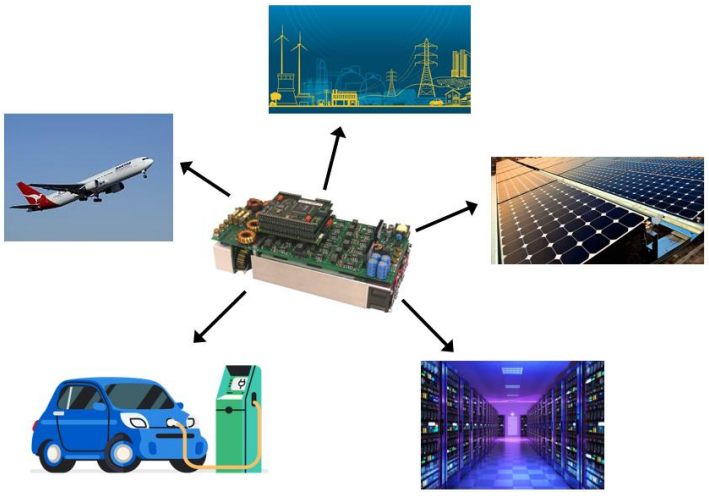


Figure 1. 1 Applications of Power Converters

These power converters can operate as power factor correctors (PFC) which are single-phase or three-phase AC/DC converters used for improving power quality or DC/AC inverters connected in grids (as shown in Fig. 1.2, 1.3, 1.4, 1.5 and 1.6), uninterruptible power supplies (UPS), motor drives or PV panels.

Figure 1. 2 Block Diagram of AC/DC Power Converter Systems

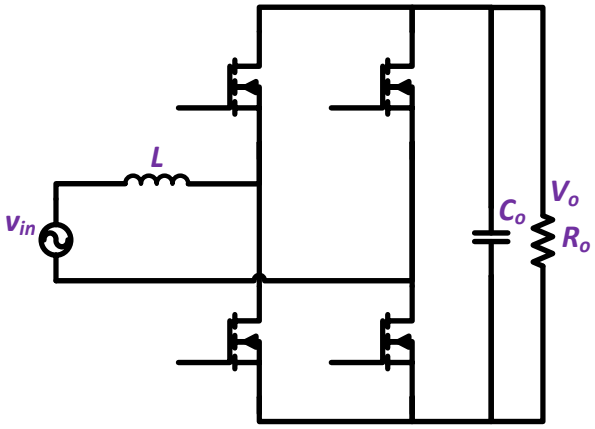


Figure 1. 3 Single phase PFC circuit schematic

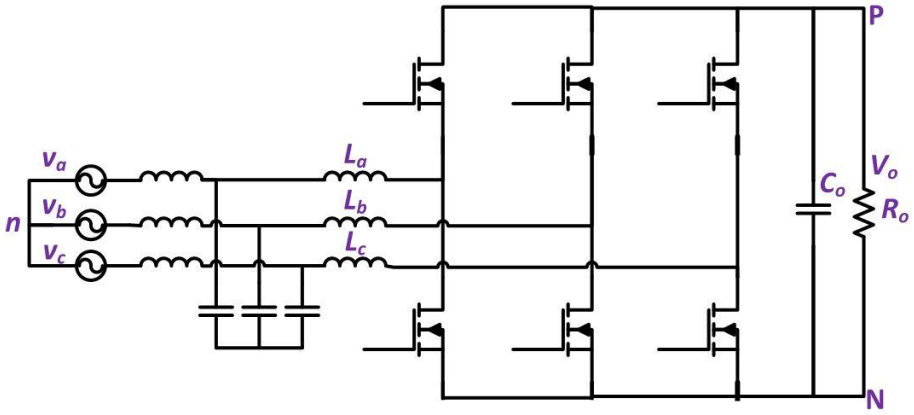


Figure 1. 4 Three-Phase PFC circuit schematic

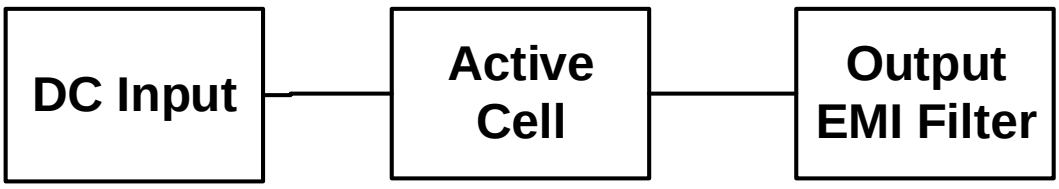


Figure 1. 5 Block Diagram of DC/AC Power Converter Systems

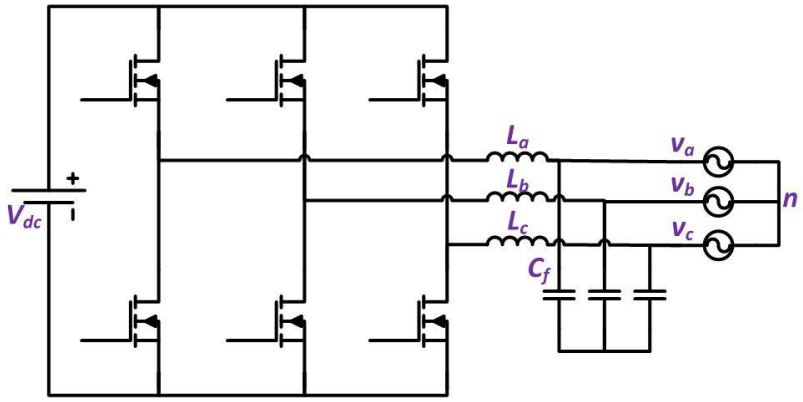


Figure 1. 6 DC/AC three-phase inverter circuit schematic

1.1.1 High Power Density Power Electronic Systems

Power electronic converters are widely used in electrical systems such as grids, servers and electric vehicles. The push until now has been for power electronic systems to achieve higher efficiency, however recently the drive has been to achieve higher power density. To achieve higher density, the size of the active bridge, dc capacitance and EMI filters has to be reduced. The active bridge size can be reduced by decreasing the number of devices, using smaller devices and packaging the devices more compactly as discussed in [A.1], [A.2], [A.8], [A.17] and [A.18].

As compared to state-of-the-art Si devices, GaN devices with similar voltage and current rating have smaller sized package as discussed in [A.12]-[A.18] and shown in Fig. 1.7. The capacitor size can also be reduced by using smaller ceramic and film capacitors and positioning them as near to the devices as possible. The third and most space consuming part in most power converters today are the EMI filters as shown in Fig. 1.8. The size of EMI filters can be reduced by operating at high frequency ranges.

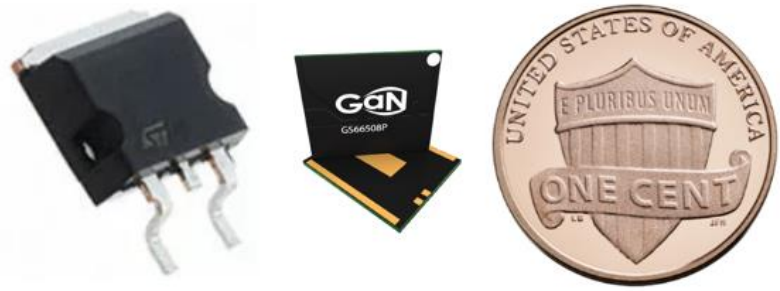


Figure 1. 7 Comparison of size of state-of-the-art Si and GaN devices at similar breakdown voltage and current ratings

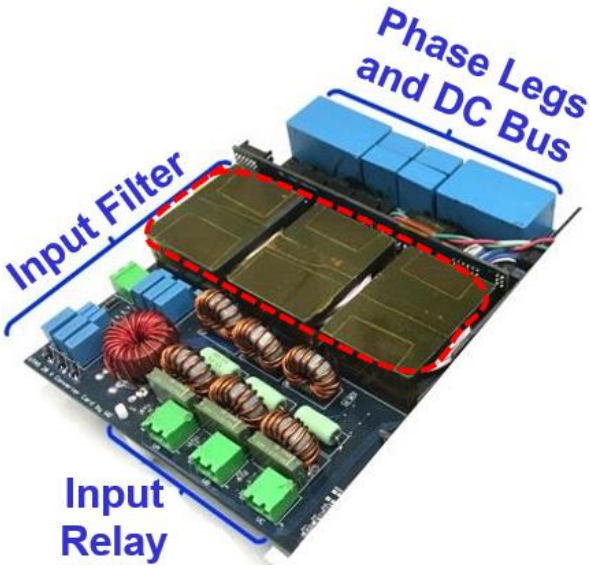


Figure 1. 8 Power Converter showing 80 % of the space being taken by input filter at f_s ~50 kHz in [A.11]

The above converter from [A.11] is designed for ~50 kHz switching frequency operation, hence the EMI filter size is large and it occupies most of the space in the converter. The three inductors shown in the red box measure 300 µH each, hence they occupy a large space in the converter. For achieving higher density, the switching frequency can be increased to > 300 kHz to reduce the size of the filter as discussed in [B.38].

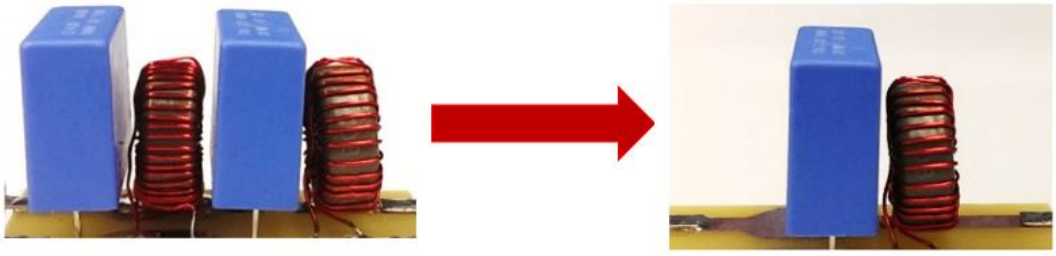


Figure 1. 9. DM filter size reduction from 50 kHz PFC DM filter to 1MHz single-phase PFC DM filter from [B.38]

1.1.2 High Frequency Operation Challenges with Hard Switching

As discussed above, pushing the switching frequency to > 300 kHz greatly reduces the size of the filter, however pushing the switching frequency higher will also lead to more switching losses in the devices.

1.1.2.1 Single-Phase PFC Hard Switched Continuous Conduction Mode (CCM)

In recent years, along with the rapid development of power electronic technology, the application of various types of power electronic devices in the power system, industry, transportation, family and many other fields has become wider. However, the harmonic pollution and reactive power issues brought by them is becoming an increasingly serious concern. The harmonic current and harmonic voltage in the grid can cause great harm to other electric equipment. Under this circumstance, power factor correction (PFC) technology has gradually become an important subject in the field of power electronic research. As for switch power supply, it is a very effective method, using active power factor correction technology in power electronic equipment, to restrain harmonic current in the power grid and to improve the power factor ([A.1] and [A.2]).

Ideally, the load of PFC should be equivalent to a resistance when looking from the input, thus enables the line side of electrical equipment a high power factor of 0.99, or even higher. Most of the PFC topologies are based on boost circuit. According to the different states of inductor current, the control methods of APFC are classified into continuous mode (CCM), critical mode (CRM)

and discontinuous mode (DCM). In order to maintain continuous current, inductor of PFC under CCM mode are usually made bigger, meanwhile higher the cost becomes. Moreover, MOSFETs do not achieve zero current conduction and zero voltage switching, making the loss bigger. The shut off current of diode is not zero, leading to a bigger reverse recovery loss ([A.2], [A.3], [A.8] and [A.10]). However, because of its continuous current, when operating under high power condition, the inductor has small ripple current. The current stress of MOSFET is small, and the EMI differential-mode noise is also small. The schematic of a single-phase PFC is shown in Fig. 1.10.

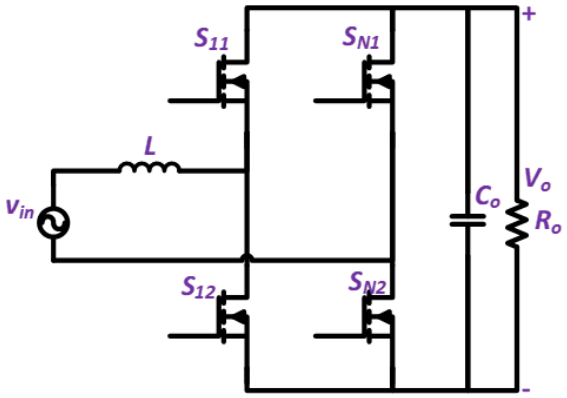


Figure 1. 10 Single-Phase PFC circuit schematic

The function of power factor correction is to ensure that the output voltage maintains constant despite the change of input voltage or load. Besides, it makes the input current track the change of input voltage, with the present state of sine wave. In this way, a single control loop will not meet the requirements of the whole system. Usually the processing method is to use double control loop. The outer loop works as the voltage control loop and the inner loop is the current control loop. The outer loop maintains the output voltage constant, while the inner one guarantees the input current of system track the shape of input voltage. The output of outer loop is sent to the inner one as input. System control structure is shown in Fig. 1.11 below ([A.37]).

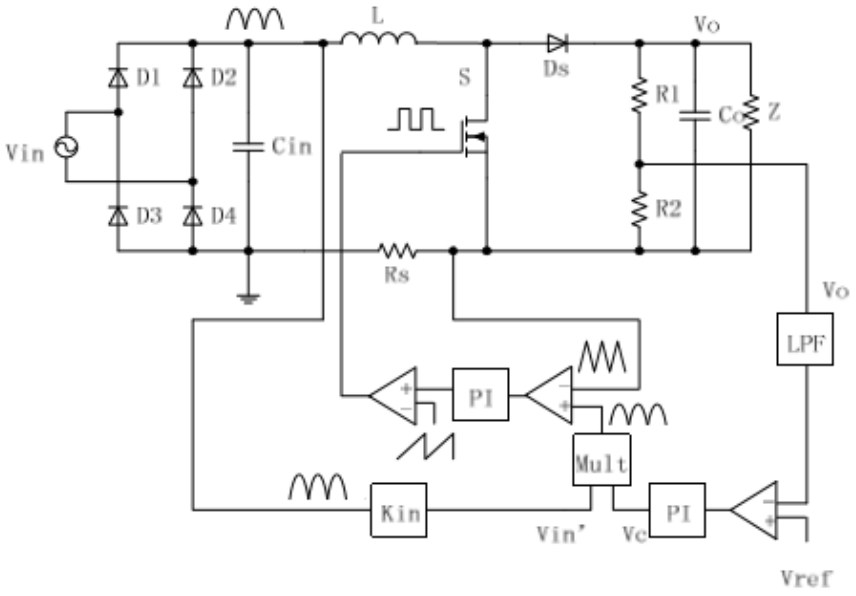


Figure 1. 11. Working principle of CCM boost PFC from [A.37]

After sampling circuit, output voltage V_o is transferred into sample value V_o' which is yhen compared with the reference voltage V_{ref}, the voltage error value is fed into the PI controller of voltage control loop, so that the output voltage V_o can maintain stable. The output value of voltage loop PI controller, V_c, is multiplied by V_{in}', which is the sample value of input voltage. Since the shape of input voltage sample value is sinusoidal, the signal of sine wave shape is obtained. This signal is the reference of inductor current, and then the current error value is sent into the current loop PI controller after comparing I_L with I_{ref}. By corresponding algorithm, I_L is designed to follow I_{ref}, so as to ensure the input current of inductor be able to track the change of I_{ref}. Thus, the input current is in phase with the input voltage and achieve the goal of power factor correction. The inductor current and reference current in CCM is shown in Fig. 1.12.

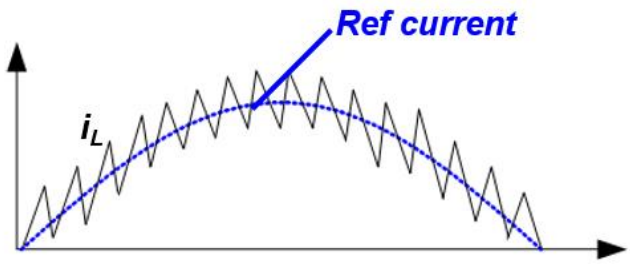


Figure 1. 12. Inductor Current and Phase Current of one phase

The loss breakdown for a single-phase PFC operating in CCM at 230 V V_{ac}, 400 V V_{dc}, 1.2 kW P_o, f_{sw} 1 MHz is shown in Fig. 1.13 based on analytical model of GaN HEMT. The converter suffers from considerable turn-on losses making soft switching turn-on a necessity for efficient high frequency operation. Also, because of the diode recovery current problem, a converter operating in CCM has higher switching loss and noise ([A.8]).

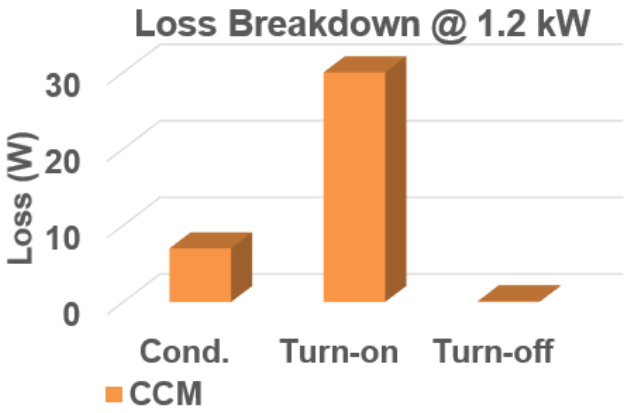


Figure 1. 13. Loss Breakdown of single-phase PFC

1.2 State-of-the-art Soft Switching Control Methods for Single-Phase PFC

As shown above, the switching losses specifically the turn-on losses become significant at high switching frequencies, hence soft turn-on is required, i.e. the voltage across the device should reach zero before the device is turned on and it starts to conduct current. There are several methods to achieve soft switching by adding resonant elements in the converter ([A.38]-[A.43]), however they do not form the scope of this research as they add complexity to the circuit and the layout. The soft switching methods which can achieve soft turn-on by making use of parasitic components, i.e. parasitic capacitors will be discussed in this section.

1.2.1 Single-Phase CRM

The mode of conduction in which the inductor conducts current continuously i.e. the inductor current increases or decreases continuously is called continuous conduction mode or CCM as

discussed above. The mode of conduction in which the inductor current remains zero for some part of the switching cycle as shown in Fig. 1.14 is called discontinuous conduction mode (DCM).

Figure 1. 14. Inductor current in DCM

The mode of conduction in which the inductor current just touches zero and then starts to increase again is called Critical Conduction Mode (CRM) or Boundary Conduction Mode (BCM) as shown in Fig. 1.15. The detailed operation of CRM and how soft switching achieved in CRM is discussed in detail. CRM for single-phase PFC has been discussed in detail in [B.2], [B.6], [B.8] and [B.22].

Figure 1. 15. Inductor current in CRM

The circuit schematic of single-phase totem pole PFC is shown in Fig. 1.10. In order to overcome the high turn-on losses, critical conduction mode (CRM) is a preferred control method. In the circuit schematic in Fig. 1.12, the two switches in the right leg operate synchronously with the mains frequency, i.e. when $v_n > 0$, S_{N2} conducts and when $v_n < 0$, S_{N1} conducts. Here the input voltage is assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency. When input voltage $v_n > 0$ the circuit will simplify to a boost converter with S_{12} as the main/low side (LS) switch and S_{11} as the auxiliary/high side (HS) switch as shown in Fig. 1.16.

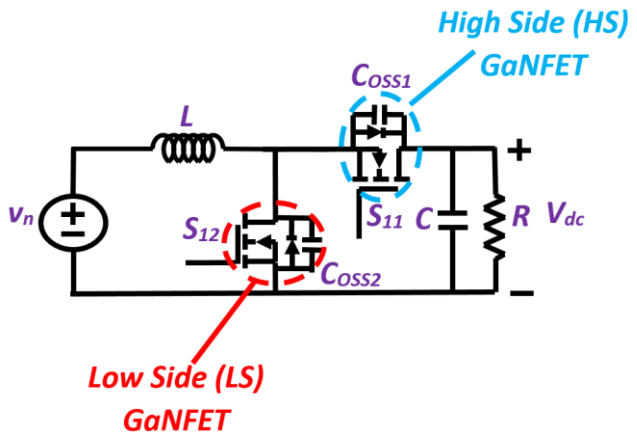


Figure 1. 16. Equivalent circuit schematic when $v_{in}>0$

The detailed switching waveform is shown in Fig. 1.17. Initially, switch S_{12} is closed and the input voltage v_n is applied across the inductor L. Thus the inductor current i_L increases linearly for a fixed on time (T_{on}) whose value depends on the converter output power P_o. S_{12} is switched off at the end of T_{on}. Immediately after the turn-off instant of S_{12} the capacitor C_{OSS2} is discharged while C_{OSS1} is charged at output voltage V_{dc} where C_{OSS2} and C_{OSS1} are the output capacitors of the switches S_{12} and S_{11} respectively. Thus, the two output capacitors and the inductor form a resonant circuit. Current i_L increases till the voltage across the switch S_{12} (v_{S12}) reaches v_n and then it starts to decrease. Finally, C_{OSS2} is charged to V_{dc} and C_{OSS1} is discharged to zero after which the body diode of S_{11} starts conducting. Hence, S_{11} can be turned on at 0 V. After a short delay, S_{11} is turned on and the inductor current i_L falls linearly. S_{11} is turned off when i_L reaches 0.

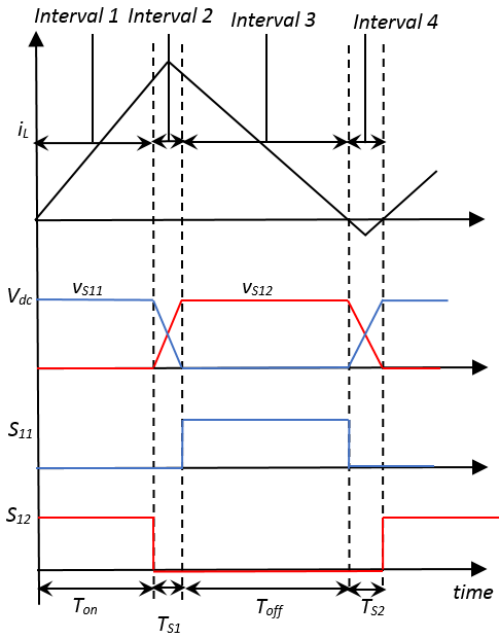
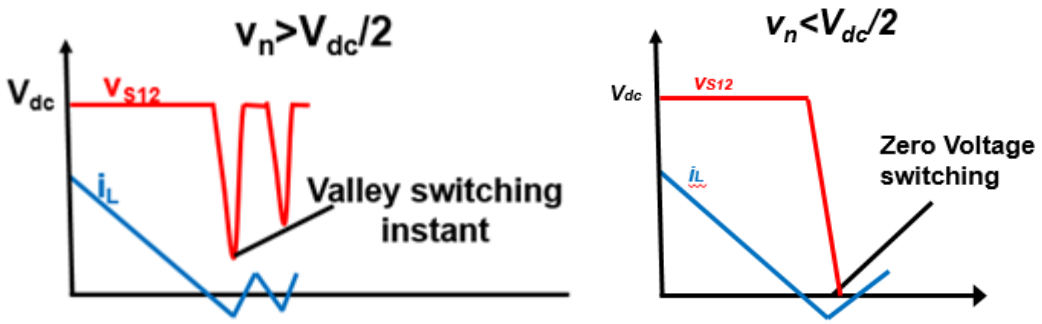


Figure 1. 17 Current and Voltage waveforms in CRM for one swithcing cycle

Immediately after the turn-off of S_{11}, resonance occurs between C_{OSS1}, C_{OSS2} and L, the nature of this resonance depends upon the input voltage v_n and output voltage V_{dc}. If $v_n < V_{dc}/2$, C_{OSS2} is completely discharged and ZVS turn on of S_{12} is achieved. If $v_n > V_{dc}/2$, C_{OSS2} is discharged to $2v_n$-V_{dc}. The turn on instant of S_{12} must coincide with the valley switching instant to ensure minimum turn-on losses as shown in Fig. 1.18. The minimum voltage achievable during the non-ZVS transition is:

$$Minimum\ Voltage = 2v_n - V_{dc} \tag{1}$$



(a) (b)

Figure 1. 18 (a). Resonant transition when input voltage is greater than half of DC voltage: Partial ZVS achieved (e) Resonant transition when input voltage is less than half of DC voltage: Complete ZVS achieved

The inductor current waveform for CRM is shown in Fig. 1.19. The losses between CCM and CRM for a single-phase PFC are compared in [B.12] for a 230 V V_{acrms}, 400 V V_{dc}, 1.2 kW P_o and 1 MHz minimum switching frequency (f_{smin}) and it is shown that CRM provides 2.5 % benefit in efficiency. The turn-on losses are < 0.1 %. In addition, CRM boost PFC converter can eliminate the reverse recovery loss of power diode with ZCS. The loss breakdown is shown in Fig. 1.20. Small turn-on losses are present due to partial ZVS. The devices used are 650 V, 30 A cascode GaN devices from Transphorm.

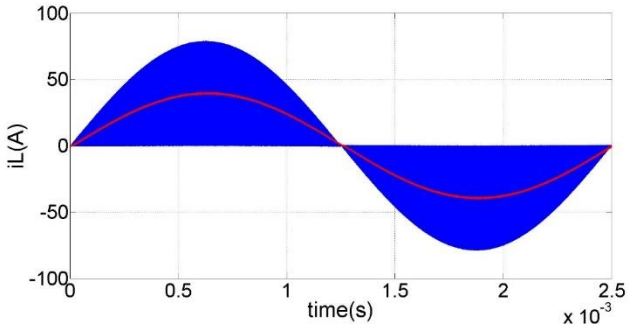


Figure 1. 19 Inductor current for one line cycle in CRM for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_{smin}: 1 MHz

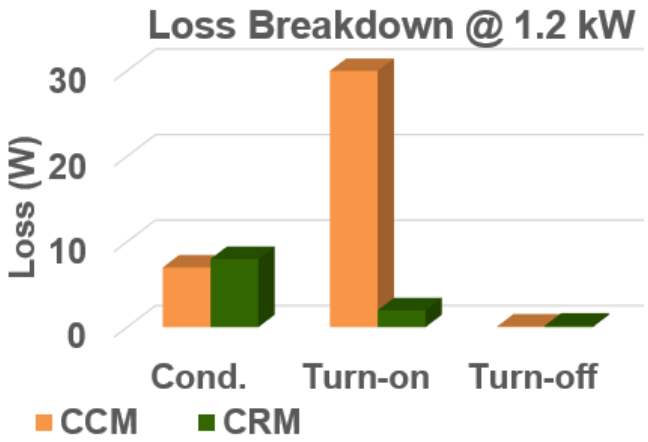


Figure 1. 20. Loss Breakdown Comparison between CCM and CRM at 230 V V_{acrms}, 400 V V_{dc}, 1.2 kW P_o at 1 MHz f_s

As can be seen above, partial ZVS losses can be significant, also since the aim of this dissertation is to be propose soft switching techniques for three-phase converters, the correct modeling of the valley switching point will be very difficult, hence a method in which complete ZVS turn-on is achieved is required. Such a modulation called Triangular Current Mode (TCM) has been proposed in [A.3].

1.2.2 Triangular Current Mode (TCM) Control

To overcome the drawback of losing ZVS over some part of the mains period, the inductor current can be allowed to go below zero (as proposed in [A.3]), i.e. S_{11} is kept on even after the zero crossing of i_L. Hence during *Interval 4*, i_L keeps decreasing linearly till it reaches a negative current I_R (as shown in Fig. 1.21). This technique is called Triangular Current Mode (TCM) control. In TCM, *Interval 1-3* are similar to CRM as shown in Fig. 1.17 and 1.21.

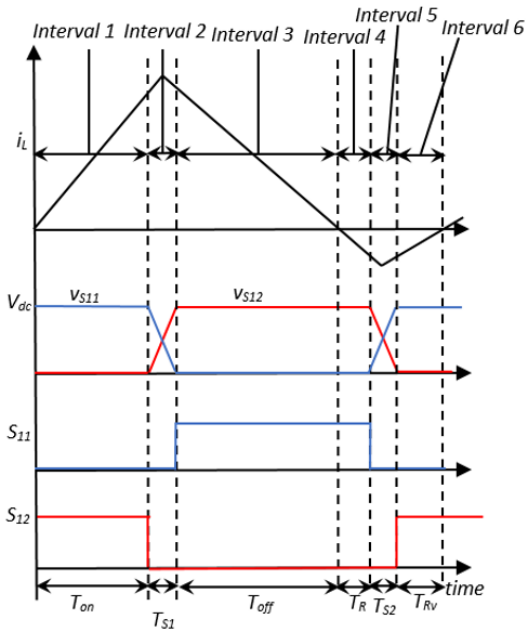


Figure 1. 21 Current and Voltage waveforms in TCM for one switching cycle

As soon as i_L reaches I_R, S_{11} is turned off and resonance occurs between C_{OSS1}, C_{OSS2} and L. During this resonance v_{S12} reaches 0V (contrary to CRM) due to negative inductor current i_L. Thus ZVS can be achieved over the entire mains cycle as shown in Fig. 1.22. When v_{S12} reaches 0 V, inductor current i_L is commutated to the body diode of S_{12} and after a short delay S_{12} can be turned on at zero voltage.

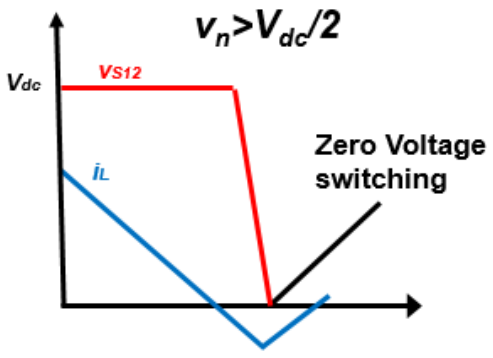


Figure 1. 22 Resonant transition in TCM when input voltage is greater than half of DC voltage: Complete ZVS achieved

I_R has to be chosen so that ZVS is achieved over the entire mains cycle. Minimum I_R, T_{off2} and T_{on2} required to achieve ZVS:

$$I_R = -(v_n \sqrt{1-(\frac{V_{dc}-v_n}{v_n})^2}) \sqrt{\frac{2C_{OSS}}{L}} \quad (2)$$

$$T_{off\,2} = \frac{L}{V_{dc}-v_n}|I_R| \quad (3)$$

$$T_{on2} = \left|\frac{L}{v_n}\right| |I_R| \quad (4)$$

where T_{off2} and T_{on2} are the off time and on time of the main switch (during negative current) respectively.

Average inductor current i_{av}

If the resonant transition times are assumed to be much smaller than T_{on1}, T_{off1}, T_{off1}, T_{off2}, the average current i_{av} in CRM and TCM is given by:

$$i_{av,CRM} = \frac{1}{2}\frac{v_n}{L}T_{on} \quad (5)$$

$$i_{av,TCM} = \frac{1}{2}\frac{v_n}{L}(T_{on1}-T_{on2}) \quad (6)$$

Inductor current waveform for TCM is shown in Fig. 1.23. Loss comparison between CCM, CRM and TCM for a 230 V V_{acrms}, 400 V V_{dc}, 1.2 kW P_o and 1 MHz minimum switching frequency (f_{smin}) is shown in Fig. 1.24. This comparison has been made based on an analytical loss model of. The loss breakdown shows complete elimination of turn-on losses and a very small (<0.05 %) increase in turn-off and conduction losses.

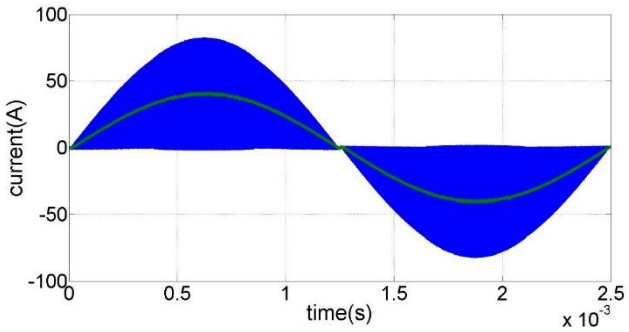


Figure 1. 23 Inductor current for one line cycle in TCM for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_{smin}: 1 MHz

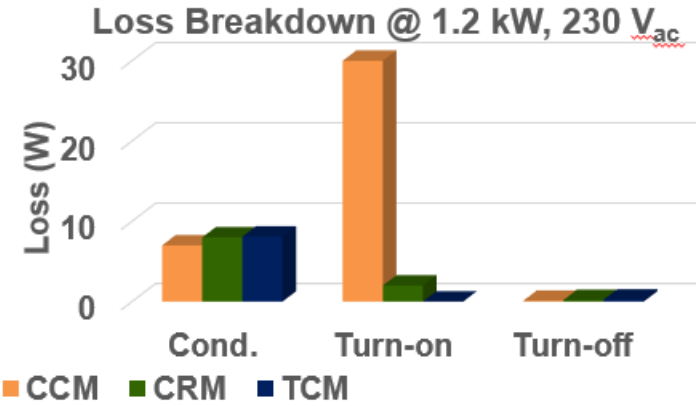


Figure 1. 24 Loss Breakdown Comparison between CCM, CRM and TCM at 230 V V_{acrms}, 400 V V_{dc}, 1.2 kW P_o at 1 MHz f_s

Variation of the switching frequency f_{sw} during one line cycle is given by:

$$f_{sw,CRM}(t) = \frac{V_{inrms}^{\ 2}(V_{dc} - |V_{in\max}\sin(\omega t)|)}{2LP_oV_o} \tag{7}$$

$$f_{sw,TCM}(t) = \frac{(V_{dc} - |V_{in\max}\sin(\omega t)|)}{V_{dc}(T_{on1} + T_{on2})} \tag{8}$$

where V_{inrms} and V_{inmax} are the rms and amplitude of input voltage respectively and P_o is the output power. The efficiency is improved in TCM but the switching frequency variation also becomes higher as shown in Fig.1.25. As variable switching frequency is not preferred in three-phase converters and multi-converter systems, TCM is modified to achieve quasi constant switching

frequency. The method proposed is discussed in Chapter 2. A review of the existing three-phase CRM schemes is discussed in the next section.

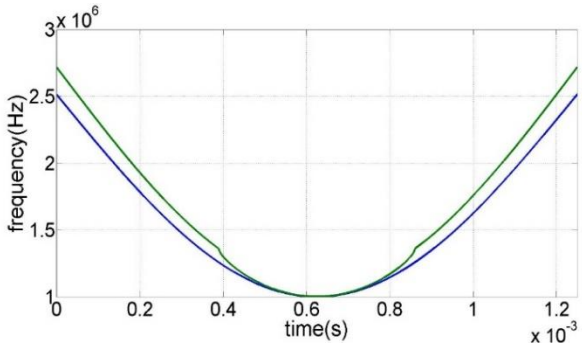


Figure 1. 25. Switching frequency variation during half line cycle in CRM and TCM

1.3 Review of Three-Phase TCM

1.3.1 Three-Phase Decoupled TCM

Three-Phase TCM has been proposed for micro-inverters (shown in Fig. 1.26) in [C.5], [C.11], [C.17] and [C.18]. This technique is similar to single-phase TCM, it makes use of body diode conduction before the device is turned on, and hence the current is bidirectional. This technique is called Boundary Conduction Mode (BCM). Since the soft-switching condition for the switches of the conventional half-bridge three-phase topology is created by this control scheme, no additional devices or magnetic components are required. This method also allows for easy implementation in a DSP and, thus, eliminates the requirement for external analog components, further decreasing the component count.

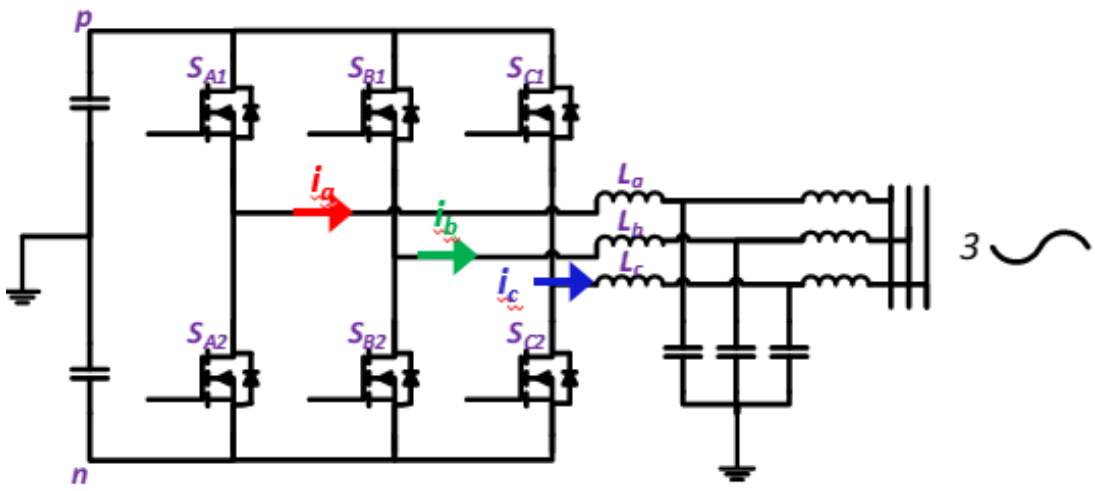


Figure 1. 26. Half bridge three-phase DC-AC Inverter

A standard half-bridge three-phase inverter is shown in Fig.1.26. In this topology, the diodes and capacitors paralleled with the MOSFETs are the body diodes and parasitic output capacitors of the MOSFETs. The ZVS boundary conduction mode (BCM) control is implemented for this topology. ZVS is achieved by allowing the bidirectional current flow that discharges MOSFET output capacitor and passes through the body diode prior to each switching transition.

1.3.1.1 Basic Operation

Since the DC mid-point is connected to AC neutral as shown in Fig. 2.1, each phase of three-phase inverter under BCM current control operates independently. Hence the whole system behaves as three single-phase converters running in parallel. Therefore, to analyze the detailed operation principle, transition from one switch to another one in one phase leg of the inverter is given. The following assumptions are made to simplify the analysis of the ZVS inverter:

1) the whole inverter system operates in steady state;

2) the output voltage (V_o) is the grid voltage.

Since the switching frequency (f_s) is much higher than the grid voltage frequency, the output voltage is assumed to be constant in one switching period (T_s). Fig. 1.27 shows the current and voltage waveforms during the transition.

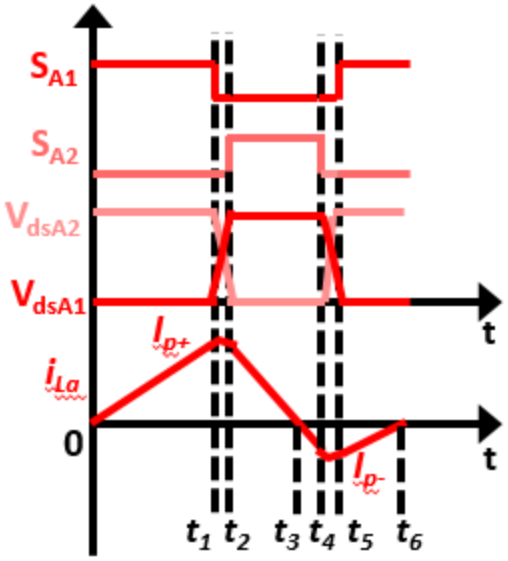


Figure 1. 27 One switching cycle in BCM control

The detailed operation stages are presented as follows:

Stage 1 (t_1–t_3): In this stage, as shown in Fig. 1.27, the switch S_{A2} is on and the switch S_{A1} is off. The equivalent circuits are shown in Fig. 1.28 and 1.29. The inductor current is linearly decreasing, after crossing the zero point (at t_2), it increases in the opposite direction. The inductor current is calculated according to the following equation:

$$i_{La}(t) = \frac{V_{ac} - V_{dc}/2}{L} t + i_{La}(t_1) \tag{9}$$

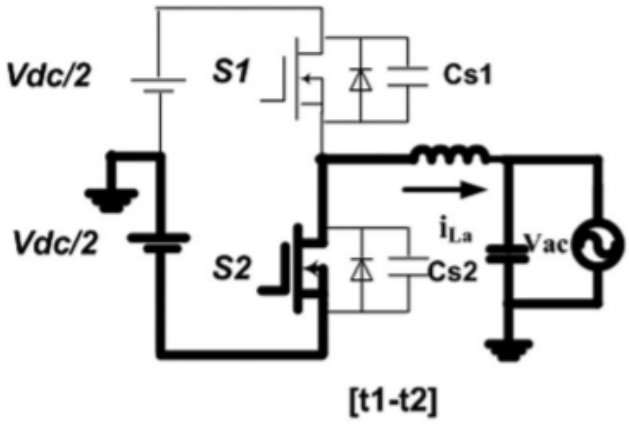


Figure 1. 28 Equivalent circuit during t_1-t_2

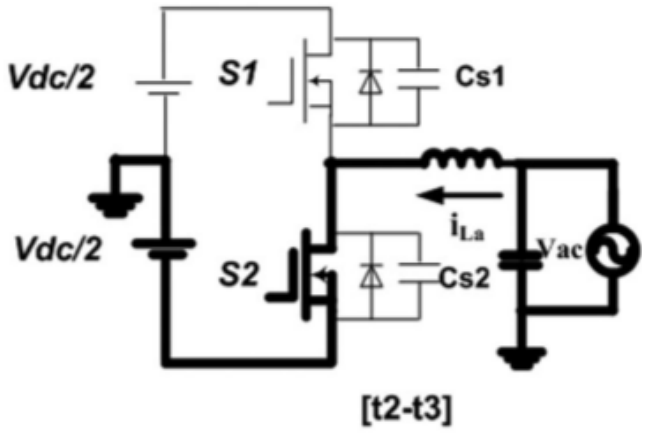


Figure 1. 29 Equivalent circuit during t_2-t_3

Stage 2 (t_3−t_4): In t_3, the inductor current has reached the expected reverse value and switch S_{A2} is turned off. As the switch S_{A2} is turned off, the resonant current of inductor L_a discharges and charges the parasitic capacitors of the MOSFETs S_{A1} and S_{A2}, respectively. The equivalent circuit is shown in Fig. 1.30. This stage ends when the capacitor of MOSFET S_{A1} is totally discharged and its voltage is zero. The status equation for the inductor current and capacitor voltage can be written as follows:

$$i_{L_a}(t) = -i_{L_a}(t_3)\cos(\omega_0 t) - \frac{V_{ac} + V_{dc}/2}{Z_0}\sin(\omega_0 t) \tag{10}$$

$$V_{CsA1}(t) = (V_{dc}/2 - V_{ac}) + (V_{dc}/2 + V_{ac})cos(\omega_0 t) - i_{L_a}(t_3) Z_0 \ sin(\omega_0 t) \tag{11}$$

The natural resonant frequency (ω_0) and the characteristic impedance (Z_0) of the resonant tank, composed by L_a, C_{sA1}, and C_{sA2}, are defined in (19) and (20), respectively

$$\omega_0 = \frac{1}{\sqrt{2CL_a}} \tag{12}$$

$$Z_0 = \sqrt{L_a / 2C} \qquad C = C_{sA1} = C_{sA2} \tag{13}$$

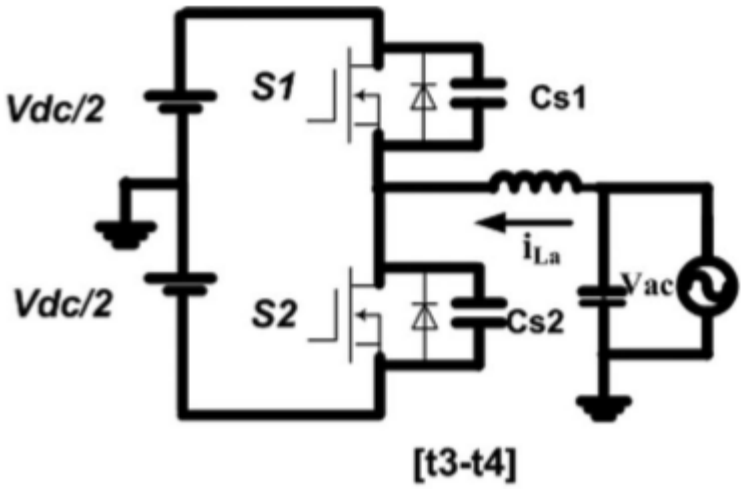


Figure 1. 30 Equivalent circuit during t_3-t_4

Stage 3 (t_4−t_5): In t_4, the voltage across S_{A1} drops to zero, and the antiparallel diode of the switch S_{A1} starts to conduct. The equivalent circuit is shown in Fig. 1.31. S_{A1} is turned ON under the ZVS condition. During this stage, the inductor current starts ramping up according to the following equation:

$$i_{La}(t) = \frac{V_{dc}/2 - V_{ac}}{L_a} t + i_{La}(t_4) \tag{14}$$

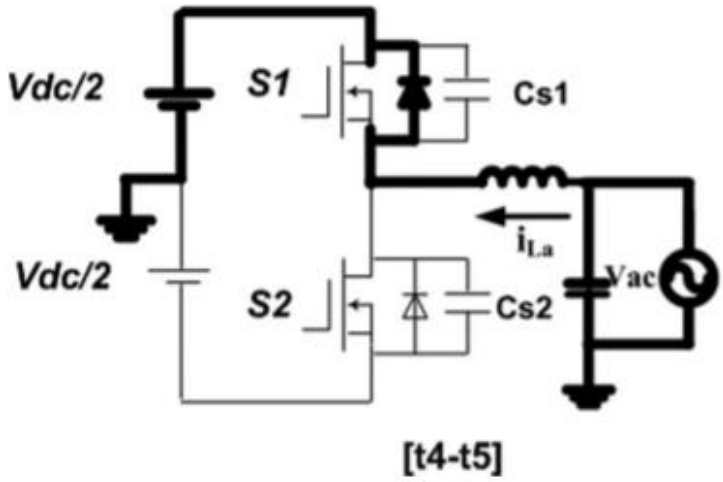


Figure 1. 31 Equivalent circuit during t_4-t_5

Stage 4 (t_5−t_7): In t_5, the switch S_{A1} turns ON at zero voltage. The equivalent circuit is shown in Fig. 1.32. Inductor current transfers from the antiparallel diode to the switch S_{A1} and keeps

decreasing linearly until it reaches a zero value and then increases in the opposite direction. Inductor current still follows (21).

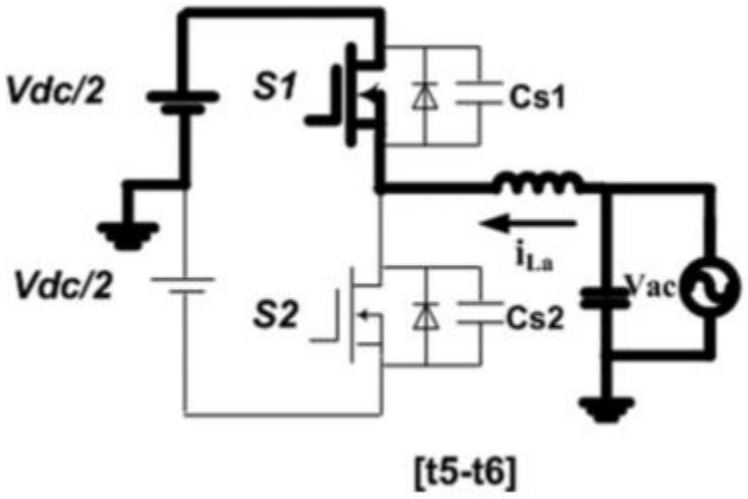


Figure 1. 32 Equivalent circuit during t_5-t_6

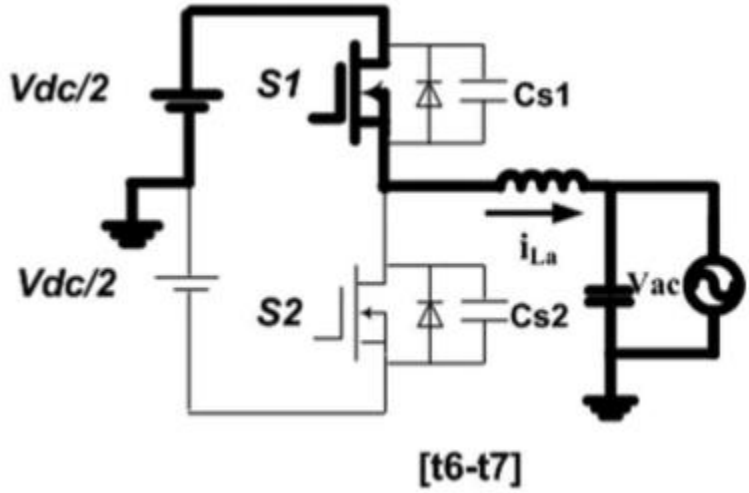


Figure 1. 33 Equivalent circuit during t_6-t_7

Implementation of the ZVS BCM control requires setting the upper and lower boundaries (limits) of the inductor current.

1.3.1.2 Issues and Limitations of Three-Phase Decoupled TCM

As discussed above, the operation of three-phase TCM is highly simnplified when DC mid-point is connected to AC neutral, the converter operation is very similar to single-phase converter operating in TCM mode. Each phase leg's operation can be viewed and understood independently. Since in TCM as the switching frequency changes during the line cycle, the biggest drawback of

the above method of achieving three-phase soft switching is the three phase legs operate at completely different switching frequencies simultaneously as shown in Fig. 1.34.

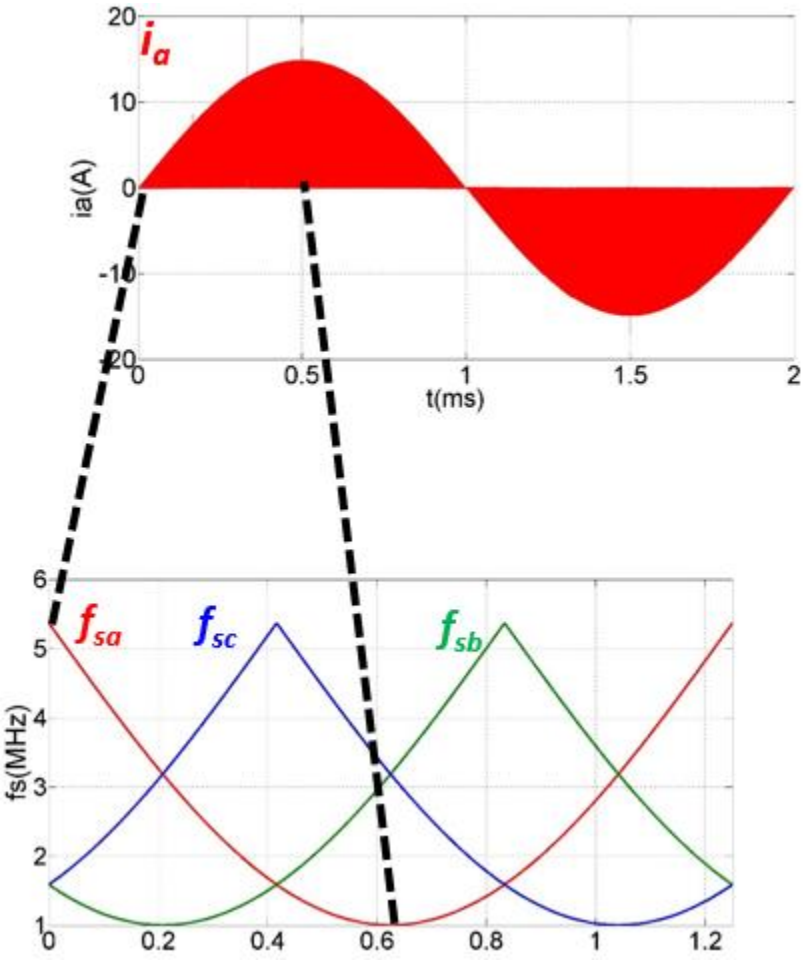


Figure 1. 34 Switching frequency variation during half line cycle showing each phase leg operating at completely different switching frequencies at the same time

The first limitation of this three-phase control scheme can be addressed by the single-phase QCFTCM control proposed in the Chapter 2. The inductor current ripple of each phase can be modified in such a way that all the phases run at the same switching frequency at the same time although it'll result in very high ripple in the current which is discussed in the next chapter. However, decoupled TCM control has a second limitation too: since during ramping up, the slope of the current is $(V_{dc}/2-|V_{ac}|)/L$ (from Eq.21), it's necessary that the ac voltage is always less than half of the DC voltage ($V_{dc}/2>|V_{ac}|$), hence limiting the modulation index to 1. To address both issues, three-phase CRM with phase synchronization from [C.7] and [C.20] is discussed below.

1.3.2 State-of-the-art Three-Phase CRM with Phase Synchronization

1.3.2.1 Three-Phase Conventional CRM

Conventional Three phase CRM has been discussed in [C.7] and [C.20] for a three-phase single switch boost PFC as shown in Fig. 1.35. The detailed operation is discussed below.

1.3.2.1.1 Theory

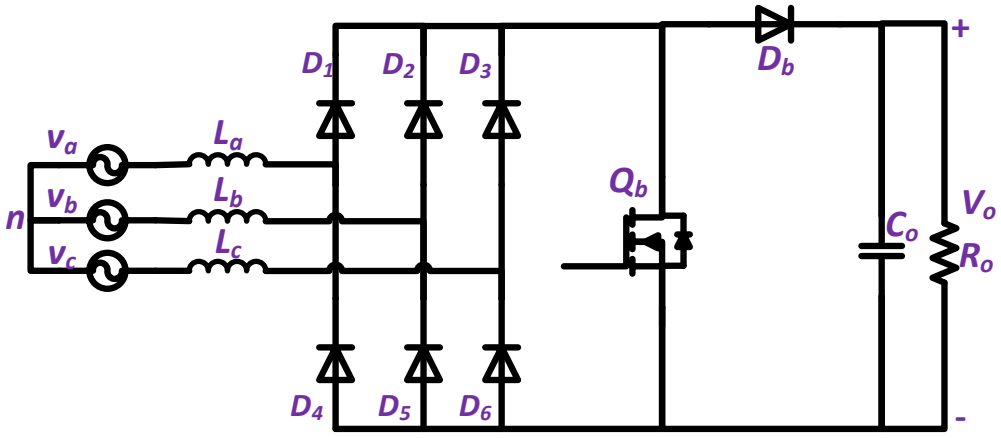


Figure 1. 35 Three-Phase single switch Boost PFC

The three-phase operation is analyzed sector wise like it is done in SVM in which the line cycle is divided into 6 sectors, a sector changes whenever a phase with the maximum absolute voltage changes. However, in this operation, the line cycle is divided into 12 sectors as shown in Fig. 1.36, where in each sector, the voltage direction and relative magnitude of the three-phase input voltage is same. The input voltages are given by:

$$v_a = V_m \sin(\omega t) \tag{15a}$$

$$v_b = V_m \sin(\omega t - 2\pi/3) \tag{15b}$$

$$v_c = V_m \sin(\omega t + 2\pi/3) \tag{15c}$$

One switching cycle waveform in sector I ($0<\omega t<\pi/6$) is shown in Fig. 1.37. Each switching cycle can be divided into 3 intervals. The input voltages are assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency.

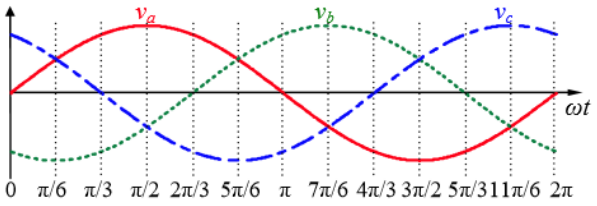


Figure 1. 36. Line cycle divided into 12 sectors

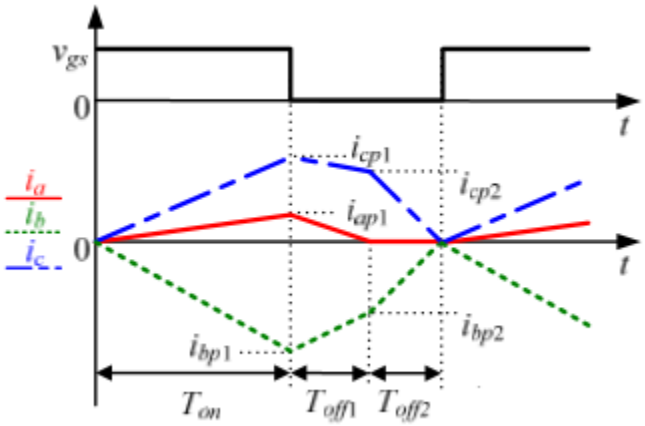


Figure 1. 37 Switching cycle waveform in Sector I

(1) *Switching Mode* 1 (0-T_1)

During switching mode 1, when Q_b is on, D_1, D_5, D_3 conduct and the phase currents increase directly proportional to respective phase voltages. The equivalent circuit is shown in Fig. 1.38(a), the phase currents' slopes are given by:

$$di_a / dt = v_a / L \tag{16a}$$

$$di_b / dt = v_b / L \tag{16b}$$

$$di_c / dt = v_c / L \tag{16c}$$

After i_b reaches peak current i_{bp1}, Q_b is turned off, the peak inductor currents are given by:

$$i_{ap1} = \frac{v_a}{L} T_1 \tag{17a}$$

$$i_{bp1} = \frac{v_b}{L} T_1 \tag{17b}$$

$$i_{cp1} = \frac{v_c}{L} T_1 \tag{17c}$$

(2) *Switching Mode* 2 (T_1-T_1+T_2)

During switching mode 2, when Q_b is off, D_b conducts and D_1, D_5, D_3 are still conducting, the equivalent circuit is shown in Fig. 1.38(b). The phase currents' slopes are given by:

$$di_a / dt = (v_a - V_o / 3) / L \tag{18a}$$

$$di_b / dt = (v_b + 2V_o / 3) / L \tag{18b}$$

$$di_c / dt = (v_c - V_o / 3) / L \tag{18c}$$

This mode ends when i_a reaches zero as v_a is minimum in magnitude in sector I, the time corresponding to this falling period is

$$T_2 = \frac{3v_a}{V_o - 3v_a} T_1 \tag{19}$$

The peak current i_{bp2} and i_{cp2} are given by:

$$i_{bp2} = i_{bp1} + \frac{di_b}{dt} T_2 \tag{20a}$$

$$i_{cp2} = -i_{bp2} \tag{20b}$$

(3) *Switching Mode* 3 (T_1+T_2-T_1+T_2+T_3)

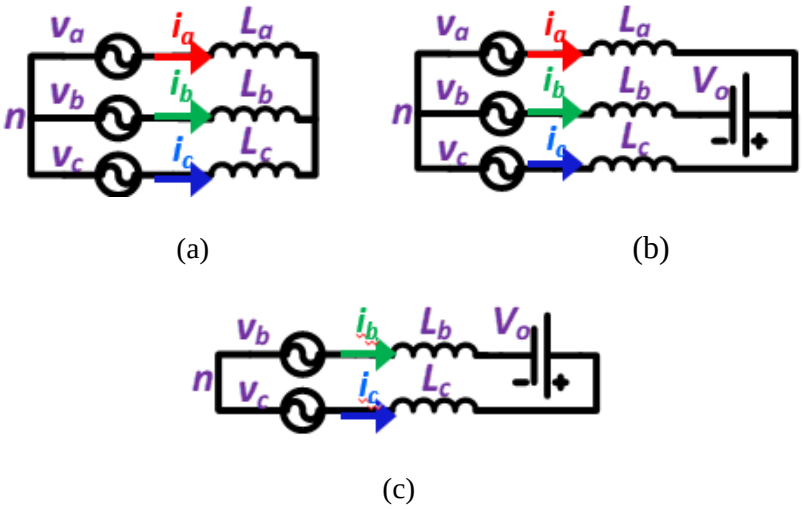
In this mode, i_b is zero while D_5 and D_3 continue to conduct, the equivalent circuit is shown in Fig. 1.38(c). The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (\mathrm{V_o} + v_b - v_c) / 2L \tag{21}$$

This mode ends when i_c and i_b reach zero. The fall time T_3 is given by:

$$T_3 = \frac{\left|i_{bp2}\right|}{\left|di_b / dt\right|} = \frac{2V_o(v_b + 2v_a)}{(V_o + v_b - v_c)(3v_a - V_o)} T_1 \tag{22}$$

After i_b reaches zero, D_B stops conducting, resonance occurs between L_B and output source capacitors of devices such that V_{dsQb} reaches 0 and Q_B is turned on at 0 V V_{ds}. This marks the beginning of a new switching cycle.



(a) (b)

(c)

Figure 1. 38 (a) Equivalent circuit in switching mode 1 (b) Equivalent circuit in switching mode 2 (c) Equivalent circuit in switching mode 3

Average phase currents can be calculated from area integral of the current waveforms and the calculated average currents are equated to the sinusoidal currents required given by:

$$i_a = I_m \sin(\omega t) = k_1 v_a \tag{23a}$$

$$i_b = I_m \sin(\omega t - 2\pi/3) = k_1 v_b \tag{23b}$$

$$i_c = I_m \sin(\omega t + 2\pi/3) = k_1 v_c \tag{23c}$$

where

$$k_1 = I_m / V_m \tag{24}$$

From (26) and (29), the switching cycle is

$$T_s = T_1 + T_2 + T_3 = \frac{V_o}{V_o + v_b - v_c} T_1 \tag{25}$$

The switching frequency can be expressed as

$$f_s = \frac{1}{T_s} = \frac{V_o + v_b - v_c}{V_o T_1} \tag{26}$$

The average currents are given by:

$$i_{a\_avg} = \frac{i_{ap1}(T_1 + T_2)}{2T_s} \tag{27a}$$

$$i_{b\_avg} = \frac{i_{bp1}T_1 + (i_{bp1} + i_{bp2})T_2 + i_{bp1}T_3}{2T_s} \tag{27b}$$

$$i_{c\_avg} = \frac{i_{cp1}T_1 + (i_{cp1} + i_{cp2})T_2 + i_{cp1}T_3}{2T_s} \tag{27c}$$

Hence, for synchronization, the phase with minimum absolute current/ voltage operates in DCM and the other two operate in CRM.

1.3.2.1.2. Issue: Non-sinusoidal Currents

As can be seen from (34), the average currents are dependent on T_1, T_2, T_3 and T_s, however, T_2, T_3 and T_s are dependent on T_1 (from eqns (26), (29) and (32)), hence this scheme has just one independent control variable which is not enough to control three average currents. Since

$$i_a + i_b + i_x = 0 \tag{28}$$

Two independent control variables are required to control two average currents and the third will be dependent on the other two. Since in this method, T_1 is the only independent control variable, this method can be used to achieve soft switching but it is not enough to achieve sinusoidal currents for all the three phases. The current for this modulation for 115 V V_{acrms}, 400 V V_{dc}, 1.2 kW P_o, 1 MHz f_{smin} is shown in Fig. 1.39. It can be seen that the average current is not sinusoidal. The average current has a distortion factor of 0.97. Also, since in the above method, switching frequency is dependent on line voltages which change during the line cycle, hence, this method also has variable switching frequency as shown in Fig. 1.40. However, since all the phases are synchronized, all the phases run at the same switching frequency.

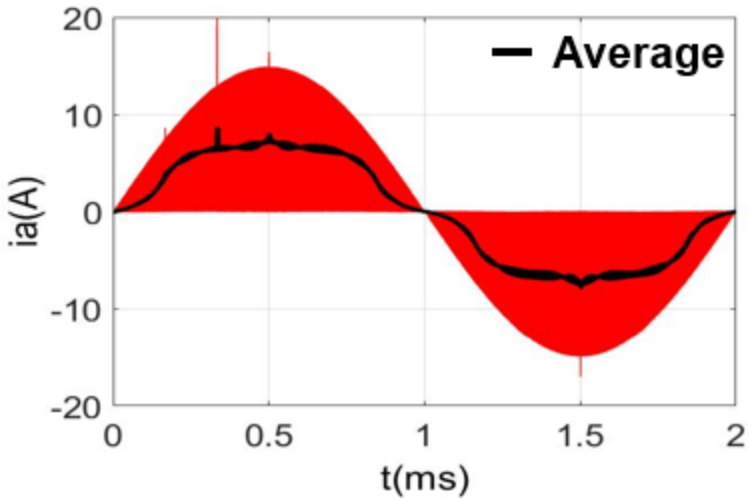


Figure 1. 39 Inductor current for conventional CRM

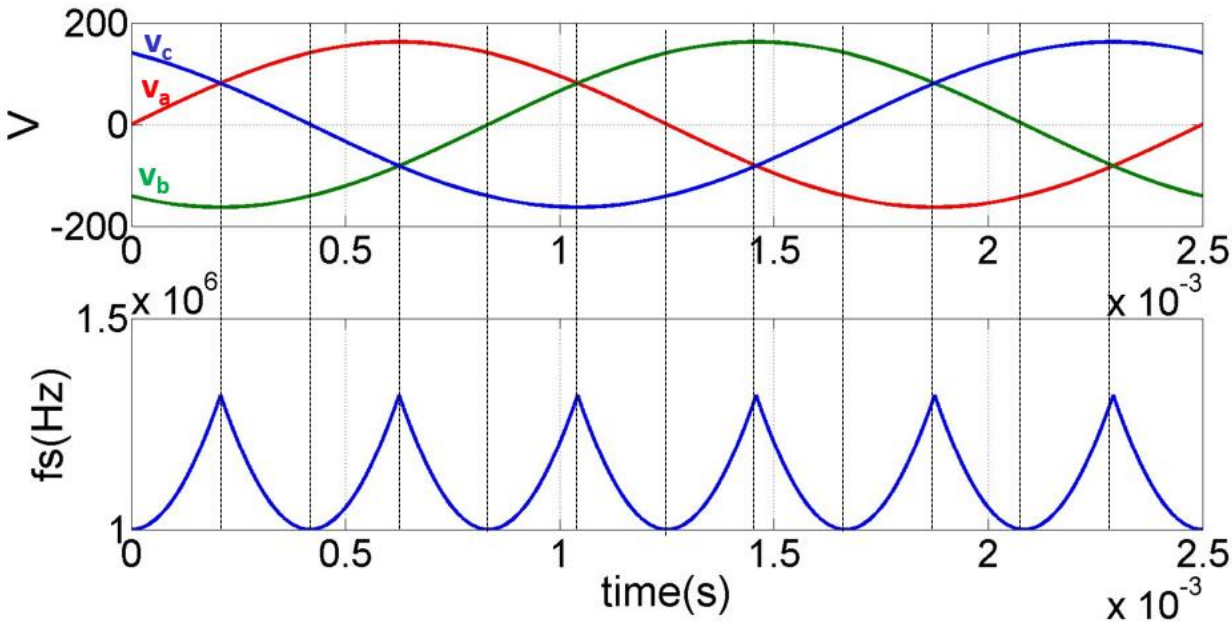


Figure 1. 40 Switching Frequency Variation of conventional CRM over one line cycle

As discussed above, just one control variable and one active device are not sufficient for achieving three sinusoidal currents. For achieving sinusoidal currents in all the three phases, at least two independent control variables and more active devices are required. The issue of non-sinusoidal currents is addressed in [C.21] for a VIENNA rectifier and it is shown how by introducing two independent control variables, sinusoidal currents can be achieved.

1.3.2.2 Boundary Mode Sinusoidal Input Current Control of the VIENNA Rectifier

Vienna Rectifier (VR) are usually operated in CCM. However, operation in DCM with sinusoidal input currents is also possible and has been applied in order to reduce the total harmonic distortion (THD) of the input currents at light load [C.21]. By operating the rectifier at the boundary of DCM and CCM, zero voltage turn-on of the power transistors can be obtained in case conventional Si freewheeling diodes with sufficient reverse recovery current are employed, i.e. switching frequencies in the 100 kHz range are possible without the need for SB SiC diodes.

In order to obtain sinusoidal input currents when operating the VR in BCM a special modulation scheme has to be used which has been outlined in detail [C.21].

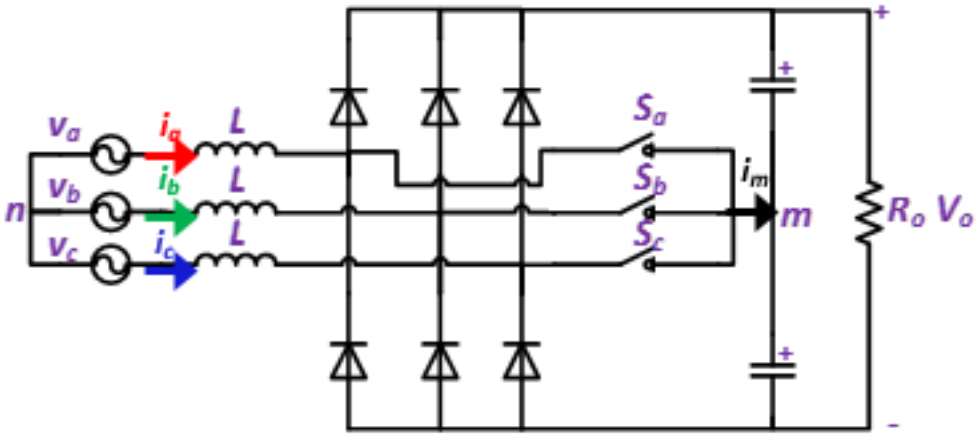


Figure 1. 41 Basic power circuit of the VR. Three bidirectional switches S_a, S_b, S_c allow to connect each phase to the DC-link midpoint, six diodes conduct the currents during the free-wheeling states to the positive or negative DC-link rail, depending on the current direction.

For the analysis of the BCM control scheme, a simplified circuit of the VR as shown in Fig. 1.41 is considered. When operating in BCM, the boost inductor currents are zero at the beginning of each switching period. The switching period always starts by turning on all the three switches S_a, S_b, S_c simultaneously. For the following considerations of the currents in the boost inductors during a single switching cycle T_s it is assumed that the values of the phase voltages show a relation $u_a >$

$0 > u_b > u_c$ and that all inductor currents are zero at the beginning of the cycle. Since the VR exhibits phase symmetry and bridge symmetry [C.21] the same considerations can be applied to any other 30° section of the mains period.

State 1: At the start of each switching cycle all switches are turned on and the currents are rising at a rate proportional to the corresponding phase voltage; the duration of the state is defined by the duty cycle D_1.

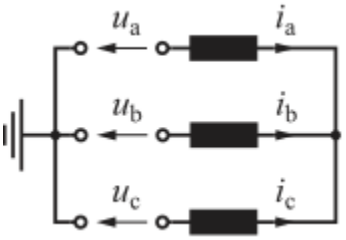


Figure 1. 42 Equivalent circuit during State 1

State 2a: If all switches were turned off at the same time, the current with the smallest absolute peak value, in this case i_b, would drop too fast and its local average would therefore be too low. In order to avoid this, the absolute value of i_b has to be increased. This can be achieved by turning-off the switch conducting the current with middle absolute peak value (in this case i_c) first, before turning off the switches conducting the currents with minimum and maximum absolute peak value, i.e. i_b and i_a (see Fig. 1.45(a)). The duration of this state 2a is given by the duty cycle D_{2a}, which has to be set such that the local average values of all currents are proportional to the corresponding phase voltages.

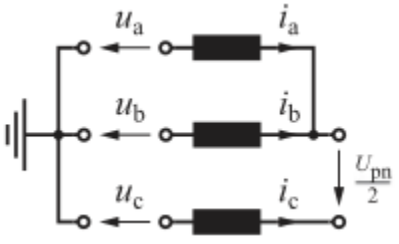


Figure 1. 43 Equivalent circuit during State 2a

State 2b : Alternatively, the absolute value of i_b could also be increased by leaving only the switch conducting the current with the smallest absolute value (S_b) turned on after state 1 (see Fig. 1.45(b)).

This state 2b can therefore also be used to achieve resistive mains behavior, concerning the relation of the boost inductor currents local average values and the mains phase voltages. In both states 2a and 2b, a current i_m is flowing into the midpoint M of the DC-link capacitors (Fig. 1.45). In state 2b the direction of that current equals the direction of the current with the lowest absolute value, in state 2a it is the opposite. Therefore, the choice between states 2a and 2b offers a degree of freedom which can be used to balance the voltage sharing between the upper and lower DC-link capacitor. The duration of state 2b is given by the duty cycle D_{2b} which has to be selected such that the local average values of the boost inductor currents are proportional to the corresponding phase voltage.

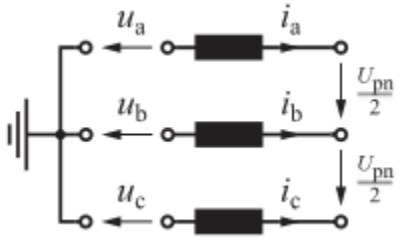
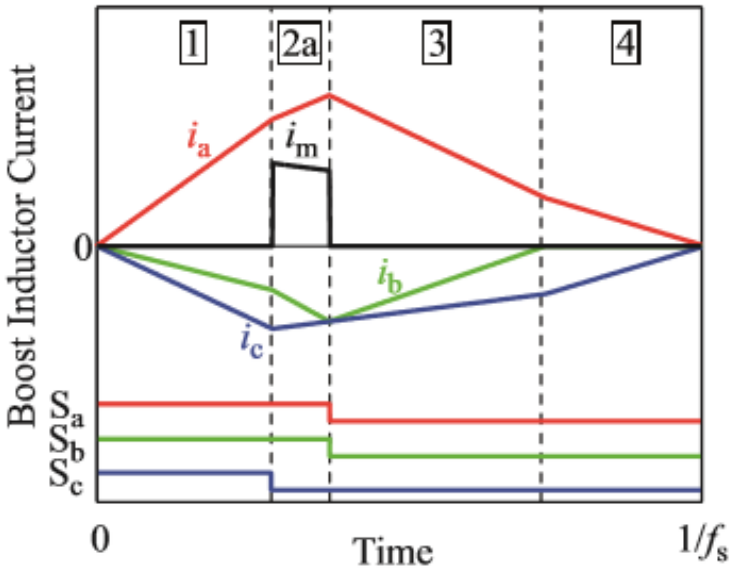
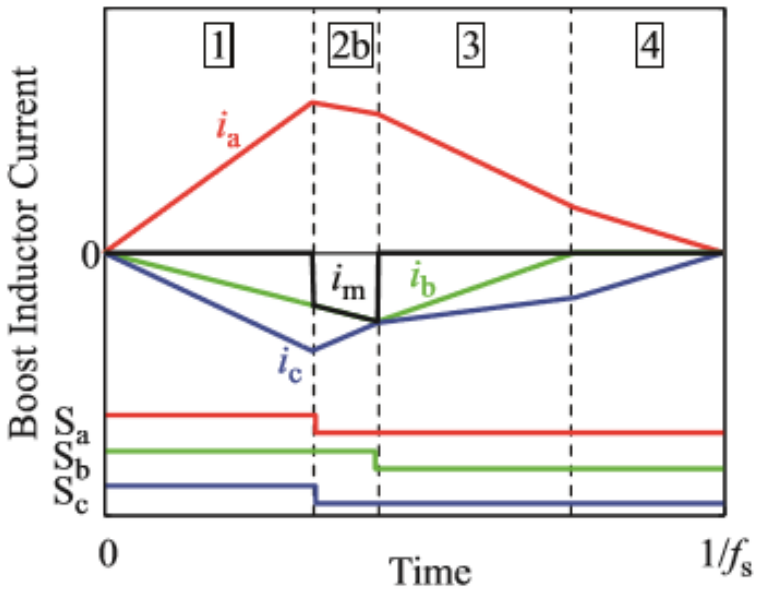


Figure 1. 44 Equivalent circuit during State 2b



(a)



(b)

Figure 1. 45 Currents i_a, i_b, i_c in the boost inductors, current into the DC-link midpoint i_m, and control signals of the four quadrant switches during a single switching cycle *Ts* using state 2a (a) and 2b (b) to achieve resistive behavior.

State 3: After state 2a or 2b is finished all currents are flowing through the free-wheeling diodes. The duration of state 3 is defined by the time the current i_b takes to reach zero.

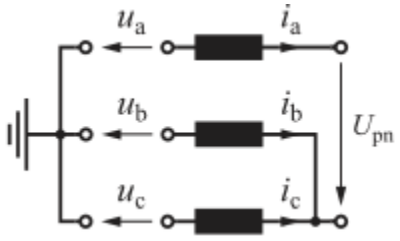


Figure 1. 46 Equivalent circuit during State 3

State 4: During state 4 only two diodes remain conducting, the duration of the state is given by the time it takes until the currents reach zero.

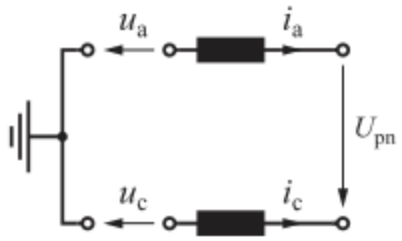


Figure 1. 47 Equivalent circuit during State 4

In order to maintain resistive mains behavior as outlined in the previous section, the necessary durations of states 1, 2a and 2b have to be calculated by the current controller, depending on the phase voltages, the DC-link voltage and the required input conductance to be emulated for the mains which is defined by the voltage controller as it determines the power delivered to the DC side. In the previous section it is assumed that $u_a > 0 > u_b > u_c$. Considering the phase symmetry, i.e. all phases feature the same circuit topology, all permutations of the phases a, b, c are also covered. In fact, if the three mains voltages are sorted by their absolute values and the subscript keywords max, mid and min are assigned to all phase quantities instead of a, b and c such that

$$|u_{max}| > |u_{mid}| > |u_{min}| \tag{29}$$

Hence, the according switch duty times T_{max}, T_{mid} and T_{min} for resistive mains behavior can be calculated. In BCM the switching frequency is varying such that the rectifier is always operating in boundary conduction mode, i.e. state 4 is immediately followed by state 1.

The simulation results from [C.21] for 400 V V_{acl}, 800 V V_{dc}, 10 kW P_o, 5 µH inductance are shown in Fig. 1.48.

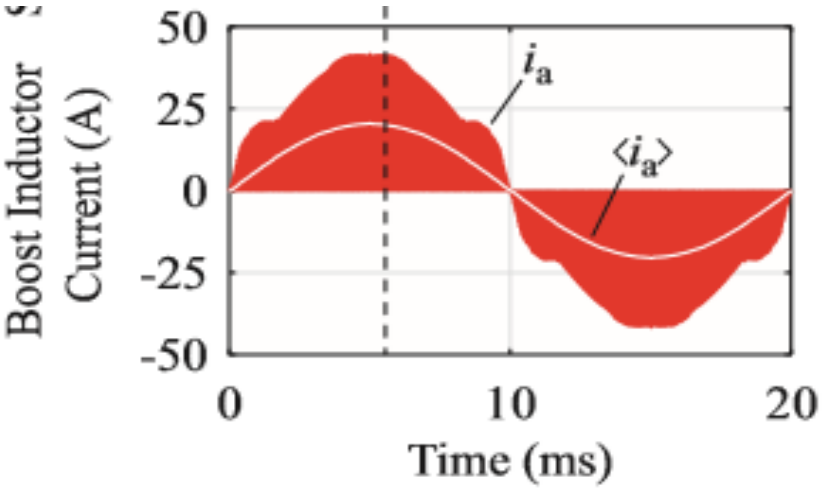


Figure 1. 48 Simulated waveform of a phase current, i_a from [C.21]

1.3.3 Issues and Limitations of State-of-the-Art Three-Phase CRM/TCM

As discussed above, three-phase decoupled TCM results in decoupled phase operation and modulation index limitation. The BCM algorithm for achieving soft switching, sinusoidal currents and phase synchronization for Vienna Rectifier is very specific to the topology and it cannot be directly extended to bi-directional topologies. Vienna Rectifier has a 3-phase diode bridge which constitutes a major chunk in the losses. Due to the diode bridge, complete ZVS turn-on is also not possible. Also, VR is a three-level topology which is more commonly used in high voltage (>1 kV) high power application. The most common topology for a three-phase converter operating < 1 kV DC bus voltage is a three-phase two-level converter.

Hence, TCM for two-level converters with phase synchronization and sinusoidal currents is proposed for in the next few chapters of this dissertation. The core idea remains that for controlling three sinusoidal phase currents, two independent control variables are required. Similar to the timeline of this research, work has been published for three-phase two-level converters in [C.23] and [C.24] with a similar fundamental of operating the converter in a combination of DCM+CRM+Clamped mode, however the discussion in these publications is limited to unity power factor. The difference between this work and the methods discussed in [C.23] and [C.24] is that the methods proposed in this dissertation achieve complete ZVS turn-on of all the three phases

(DCM, TCM and Clamped), thus minimizing the losses. [C.24] only discusses valley switching for DCM phase which leads to significant losses at high switching frequency and also creates the issue of switching time calculation which is very complex. The details are discussed in Chapter 3. Further, in Chap. 4 and 5, the scope of this dissertation is expanded to reactive power control and three-level converters.

1.4 Dissertation Outline

This dissertation is organized into six chapters.

Chapter 1 is the introduction of the research background. Today's power and energy systems have very high density (>50 W/in^3) and efficiency (>99 %) requirements. Power electronics systems were earlier driven by the target to achieve high efficiency, however with state-of-the-art Si technology and hard switched CCM control, the current AC-DC and DC-AC converter systems have already achieved ~99% efficiency at low switching frequencies (<30 kHz). Recently, the drive has shifted to achieving high power density while maintaining the same efficiency. In today's AC-DC and DC-AC converter systems, most of the space is consumed by EMI filters, hence reducing the size of filter can be instrumental in achieving high power density.

High frequency operation (> 300 kHz) leads to a size in reduction of EMI filters though it also leads to an increase in switching losses thus compromising on efficiency. Thus, better control methods are required for today's power converters that enable soft switching for devices specifically ZVS turn-on without adding to the physical complexity of the converter. The state-of the-art control methods namely CRM and TCM have been discussed as these methods achieve soft turn-on by enabling bi-directional current such that the anti-parallel body diode starts conducting before the device is turned on.

Overview of state-of–the-art Triangular Current Mode control (TCM) for three-phase converters is discussed. First, it is shown that when DC mid-point is connected to AC neutral, single-phase TCM can be directly extended to three-phase operation. However, this kind of

operation leads to decoupling of the three phases. Also, there is a limit to the maximum modulation index this topology can achieve. Further, conventional critical mode control (CRM) is discussed for a three-phase single switch boost PFC and it is shown how the issue of decouple phases can be solved by operating the converter in a combination of DCM+TCM mode of operation. Though, sinusoidal currents cannot be achieved by this method. In the last section of this chapter, sinusoidal input current Boundary Conduction Mode control (BCM) is discussed for a Vienna Rectifier which paves the way for sinusoidal line frequency currents. However, this method cannot be directly extended to three-phase two-level converters. This gives the motivation to search for a new control technique to achieve soft switching and sinusoidal currents for the common three-phase two-level topology.

In Chapter 2, a new switching scheme, constant frequency TCM is proposed for a single-phase PFC such that it achieves ZVS turn-on, sinusoidal mains current and constant switching frequency. TCM is modified to achieve constant switching frequency by shaping the current ripple envelope as the goal of this research is to be able to achieve ZVS turn-on for a three-phase converter without adding any extra resonant components to the converter.

In Chapter 3, Triangular Current Mode (TCM) to achieve soft switching and phase synchronization for three-phase two-level converters is proposed. It is shown how soft switching and sinusoidal currents or resistive mains behavior can be achieved by operating the phases in a combination of discontinuous conduction mode (DCM), TCM and clamped mode. The detailed operation in one switching cycle with mathematical models governing the circuit operation is discussed for both rectifier and inverter mode of operation. The whole line cycle is divided into 12 sectors, the voltages and currents mirrored after every thirty degrees owing to the three-phase symmetry. Variation of conduction times in one sector is shown. Further, the whole line cycle operation is discussed making use of the three-phase symmetry. A simple single core DSP implementation is also proposed with average current control and zero crossing detection of

currents. The relationship governing which phase operates in DCM, TCM or clamped mode of operation is also discussed. The proposed algorithm is validated on a GaN converter and it is shown how soft switching can be achieved for the phase operating in DCM mode resulting in zero turn-on losses and lower CM noise. System efficiency of 99% is achieved with a power density of 110 W/in^3 at 300 V DC voltage, 0.7 kW power level at ~500 kHz switching frequency.

The discussion of TCM in current literature is limited to unity power factor assumption, however this limits the algorithm's adoption in commercial rectifiers and inverters. In commercial applications, there can be reactive power requirement from the grid in case of inverters, as discussed in Chapter 4. It is proposed in Chapter 4 that TCM algorithm discussed in Chapter 3 can be extended to accommodate reactive behavior. It is proposed that the three phases can still operate in a combination of DCM+TCM+Clamped modes of operation. To compensate for reactive power, higher ripple needs to be injected in currents also resulting in higher conduction losses. Hence, beyond a certain power factor, it is recommended to switch to hard-switched CCM. The algorithm is validated on a GaN converter, final efficiency achieved is ~99% along with a power density of 110 W/in^3 at 300 V DC voltage and 0.7 kVA. ZVS turn-on is achieved for all the three phases.

In Chapter 5, proposed TCM+DCM+Clamped control algorithm is extended to three-level topologies, the switching sequence is modified to extract the advantage of reduced Common Mode Voltage (CMV) switching states of the three-level topology, the switching frequency can thus be pushed to 3 times higher as compared to state-of-the-art SVPWM control while maintaining close to 99% efficiency. Two switching schemes are proposed, both have a very small switching frequency variation of 6% as compared to state-of-the-art methods with >200% switching frequency variation. The validation of the proposed algorithm is shown on a three-level NPC inverter.

Chapter 6 provides conclusions of the work with the summary of actions taken and the directions for future work.

1.5 Contributions

A new switching scheme is proposed which achieves constant switching frequency for a single-phase converter operating in TCM mode, the envelope of the ripple is varied to maintain a constant switching frequency. This research has been published in a peer-reviewed IEEE conference paper. WBG devices are a promising candidate for high frequency operation owing to their small conduction losses, to accurately analyze the devices' parameters, detailed device characterization is carried and the results are published in two peer-reviewed IEEE conference papers.

TCM is further extended to three-phase converters such that the phases operate in a combination of DCM, TCM and Clamped modes of operation, the switching frequency variation with the proposed algorithm is just 34 % as compared to >100 % in decoupled TCM. All the phases have complete ZVS turn-on, thus pushing the efficiency higher (99 %) and the common mode noise lower. This algorithm is further extended to reactive power control which is required for motor drives and grid connected inverters. A mathematical model for the proposed schemes is also presented. This work has been awarded a patent and two peer reviewed IEEE conference papers have been published. Further, a paper is being prepared for transactions on power electronics from this research. A very simple single CPU DSP implementation of the proposed algorithm is also presented.

The proposed DCM+TCM+Clamped operation is extended to three-level converters such that it employs the benefit of lower CMV offered by the three level topologies. The maximum CMV magnitude is reduced by 33 %. This improvement also reduces the switching frequency variation to just 6%. Two switching schemes are proposed and both of them have been applied for patenting. The switching schemes lead to a huge (6x) improvement in the power density of the three-level inverter. This research has also been published in peer reviewed IEEE conference paper and a paper is being prepared for transactions on power electronics.

Chapter 2. Proposed Constant Frequency TCM for Single-Phase Converters

Power factor correction (PFC) rectifiers form a very essential part of ac/dc/ac converter systems. Efficiency close to 100% is required in PFC rectifiers. Single-phase conventional boost PFC rectifiers consist of a diode bridge followed by boost converter. However, this topology suffers from high conduction losses in the diode bridge. Basic bridgeless topology in [A.1] eliminates the diode rectifier bridge which decreases the number of semiconductor devices thereby decreasing the converter losses.

Totem Pole Bridgeless PFC rectifiers [A.2] further decrease the converter losses, however this topology has two active switches and two diodes. The conduction losses can be further minimized by using active switches instead of diodes as in H-bridge PFC [A.3]. The circuit schematic of H-bridge PFC is shown in Fig. 2.1.

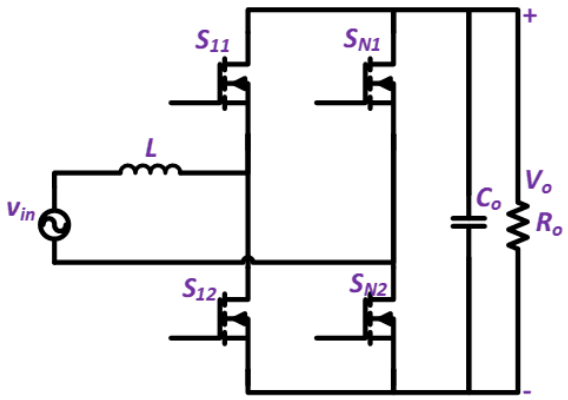


Figure 2. 1 Single-Phase PFC Circuit Schematic

As discussed in the previous chapter, the most common modulation technique hard switched CCM suffers from high turn-on losses which are reduced in CRM and completely eliminated in TCM by ZVS turn-on. The technique used in these switching schemes is passing bidirectional current in each switching cycle such that the body diode starts conducting before the device is

turned on. However, switching frequency varies in CRM and TCM such that it is maximum when the input voltage is minimum as shown in Fig. 2.2. This frequency varies with load and DC voltage also. This also poses a challenge for the scheme's extension to three-phase as all the phases will operate at completely different switching frequencies simultaneously.

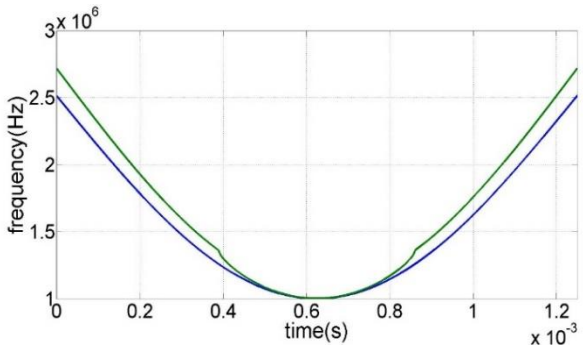


Figure 2. 2 Switching frequency variation in CRM and TCM over half line cycle

2.1 Theory

The basic idea of constant frequency TCM lies behind making the frequency v/s time constant. If we choose the minimum switching frequency of CRM and TCM as the operating switching frequency of QCFTCM, it is desirable to decrease the switching frequency where it is maximum, i.e. increase the switching period for that part of the mains cycle.

This can be achieved by increasing the reverse current to increase the time period but if the reverse current is increased, the peak current has to be increased accordingly to maintain the same average current as shown in Fig. 2.2.

2.1.1 Mathematical Model

The equations to shape the current ripple are given by:

$$T_{on1} = \frac{1}{2}\left(\frac{1}{f_{sw}} + \frac{2LP_o}{V_{inrms}^2}\right) - \frac{|v_n|}{2 f_{sw} V_{dc}} \tag{30}$$

$$T_{on2} = \frac{1}{2}\left(\frac{1}{f_{sw}} - \frac{2LP_o}{V_{inrms}^2}\right) - \frac{|v_n|}{2 f_{sw} V_{dc}} \tag{31}$$

$$T_{off1} = \frac{V_{dc} - |v_n|}{|v_n|} T_{on1} \tag{32}$$

$$T_{off2} = \frac{V_{dc} - |v_n|}{|v_n|} T_{on2} \tag{33}$$

$$I_R = -\frac{v_n}{L} T_{Rv} \tag{34}$$

$$I_{peak} = \frac{v_n}{L} T_{on} \tag{35}$$

The QCFTCM control is derived from CRM, in CRM the auxiliary switch is turned off after the current reaches zero. In QCFTCM, zero current is detected and after ZCD a variable delay of T_{off2} is given to turn off the auxiliary switch. In CRM, the main switch conducts for a constant on-time while in QCFTCM, the main switch conducts for a variable on-time equal to the sum of T_{on1} and T_{on2}.

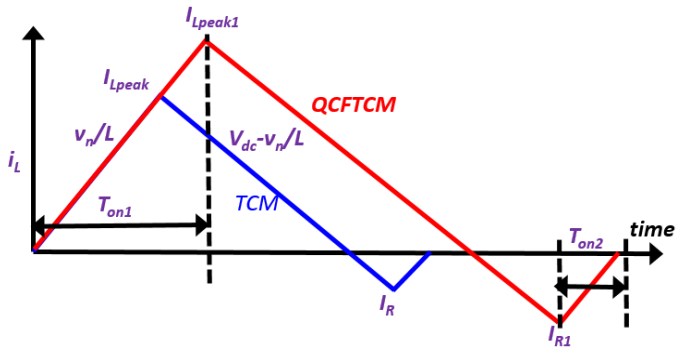
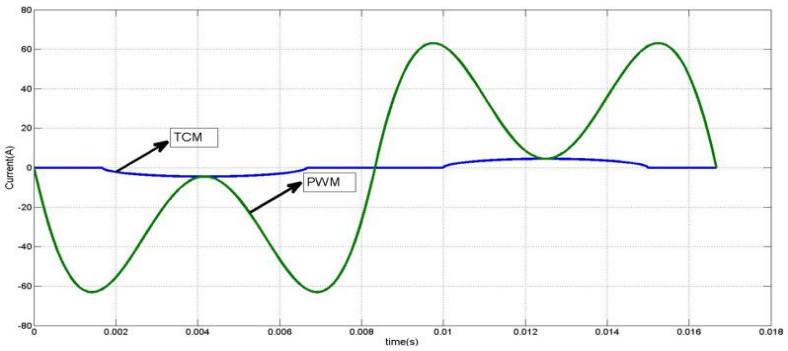


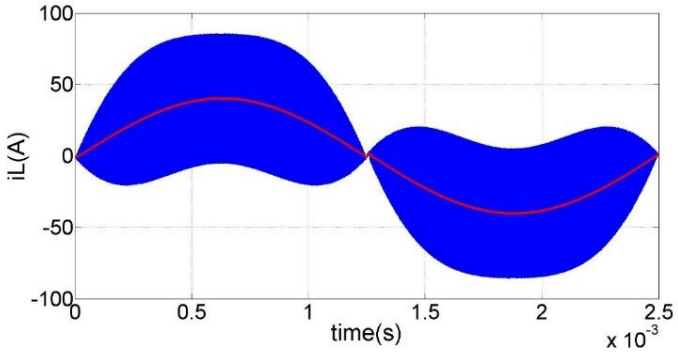
Figure 2. 3 Inductor current for one switching cycle in TCM and QCFTCM

2.1.2 Verification by Simulation

Variation of T_{on} and T_{Rv} over full line cycle is shown in Fig. 2.4(a). The simulated phase current is shown in Fig. 2.4(b).



(a)



(b)

Figure 2. 4 (a) Variation of T_{on} and T_{Rv} for full line cycle and (b) Simulated inductor current for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_s: 1 MHz

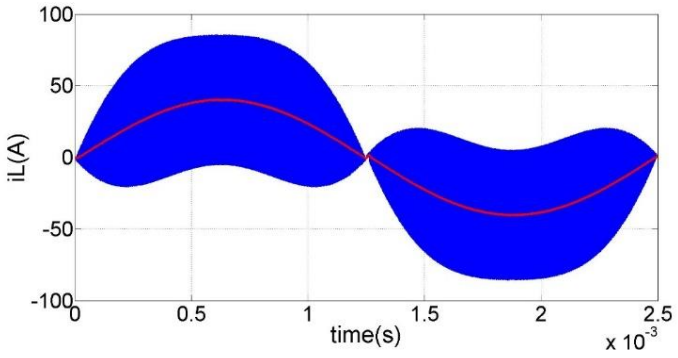
2.1.3 QCFTCM and Pulse Width Modulation (PWM)

QCFTCM is derived from CRM but since it is a quasi-constant frequency modulation it is important to find similarities and differences between QCFTCM and PWM. The duty ratio in QCFTCM is given by:

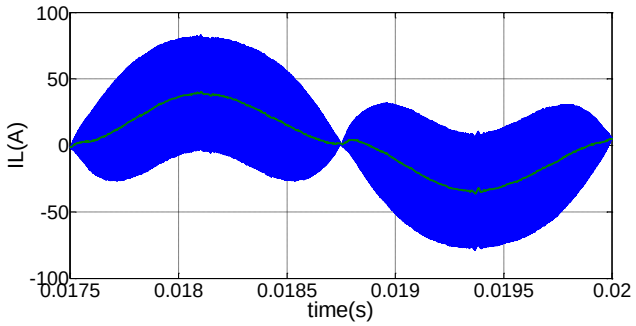
$$d = \frac{T_{on1} + T_{on2}}{T_s} = 1 - \frac{|v_n|}{V_{dc}} \tag{36}$$

When the same duty ratio is applied in left aligned constant frequency carrier based PWM, it is expected to give same results as QCFTCM. Though, on further analysis of the inductor current, it can be seen that both result in different inductor currents and different average currents as shown in Fig.2.5(a) and (b). The inductor current spectrums look similar but on viewing closely, it can be

seen that in QCFTCM the switching frequency varies in a small range around 1MHz while in PWM only the switching frequency and it's harmonics are present as shown in Fig. 2.6(a) and (b).

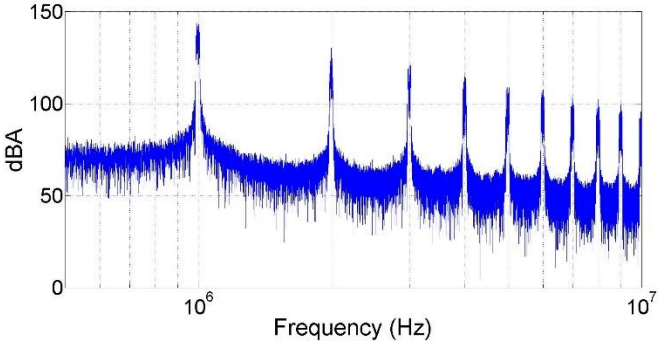


(a)

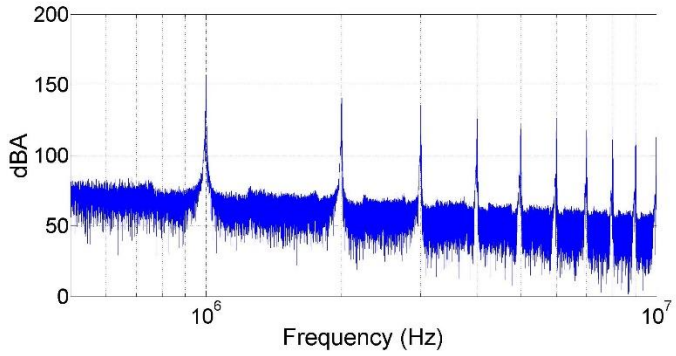


(b)

Figure 2. 5 (a) Inductor current for one line cycle in (a) QCFTCM (b) PWM for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_s: 1 MHz



(a)



(b)

Figure 2. 6 Inductor current spectrum for (a) QCFTCM (b) PWM

This is due to the presence of second order harmonics in output DC voltage V_{dc} of PFC while in caculations V_{dc} is assumed to be constant. As control methods of QCFTCM and PWM are different, this ripple has different effects on inductor current in both of them. This change in DC voltage will affect the falling slope of inductor current. In QCFTCM, since inductor current zero crossing is detected to control the current, the envelope of the current ripple cannot change and the duty ratio adjusts itself to generate sinusoidal currents. Hence, in QCFTCM there is a jitter in switching frequency around 1 MHz as shown in Fig.2.6(a).

In PWM, since there is a constant frequency carrier wave, the DC voltage ripple changes the envelope of the current ripple thereby changing the average current as shown in Fig. 2.5(b). Morover, in PWM the switching frquency harmonics are very clear and prominent while in QCFTCM they are distributed over a range of frequency around the switching frequency and a single frequency component is not that prominent.

Thus, this modulation is called Quasi-constant frequency TCM as thereotically, the switching frequency should be constant but in simulation a small jitter around the switching frequency is observed. Furthermore, PWM cannot be used for achieving sinusoidal current and soft switching operation simultaneously as it does not give the desired average inductor current while QCFTCM compensates for the DC voltage ripple by continuosuly compensating the conduction times and switching frequency. Achieveing constant switching frequency and ZVS turn-on paves the way to

the goal of this resaerch which is to propose TCM for three-phase converters with phase syncronization.

2.2 Control Implementation

A straightforward way of implementation is to start the switching cycle from Zero Crossing Detection (ZCD) of inductor current and then use pre-calculated switching times T_R and T_{Rv}+T_{on} for the turn-off of the auxiliary device and the turn-on off main device respectively. However, the use of pre-calculated times can lead to distortion due to non-idealities not considered in the model (as discussed in [A.8]) such as dead-time effect, controller-switch delay etc., hence closed loop control implementation using average current controller is proposed in [B.42] for CRM.

In CRM, T_{on} is generated using average current controller. QCFTCM can be implemented in a similar way with the only difference that a pre-programmed variable delay T_R is given after ZCD of inductor current i_L and the on-time of device S_{12} (T_{Rv}+T_{on}) is generated from the compensator as shown in Fig. 2.7. Thus, these two control variables, T_R and T_{Rv}+T_{on} are used to control the two outputs- constant switching frequency and average inductor current respectively.

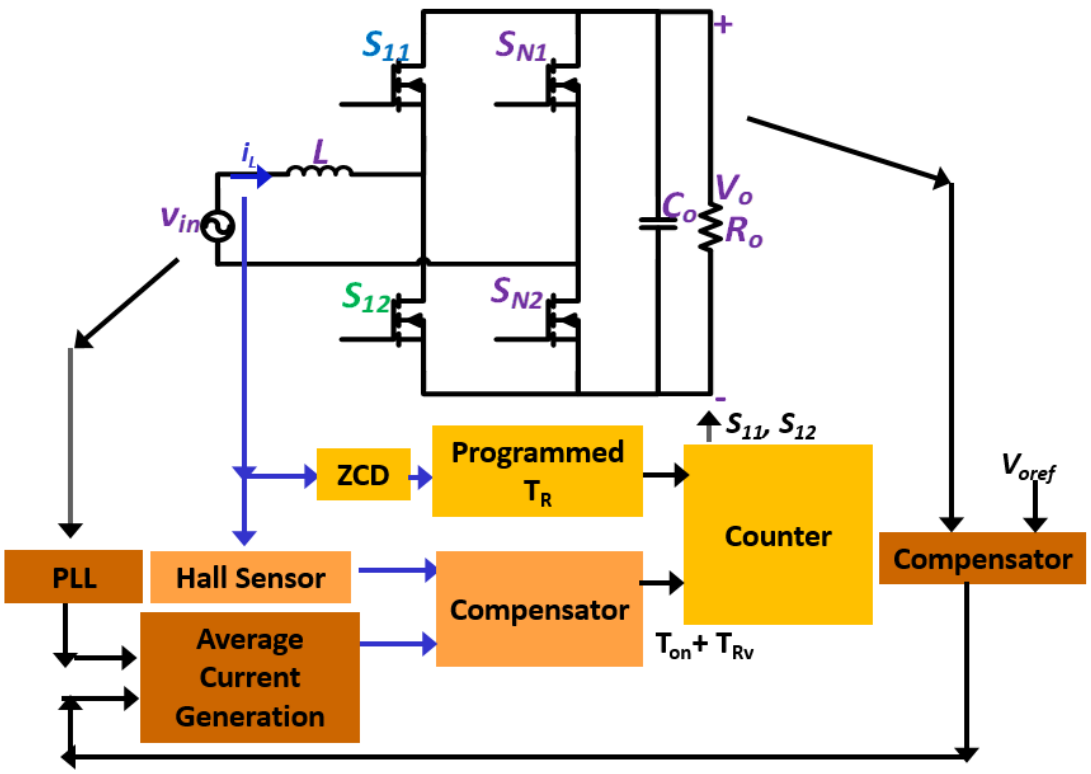


Figure 2. 7 Closed loop Implementation for QCFTCM using average current control

2.2.1 Verification by Simulation

The simulated phase current with the above implementation for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_s: 1 MHz is shown in Fig. 2.6.

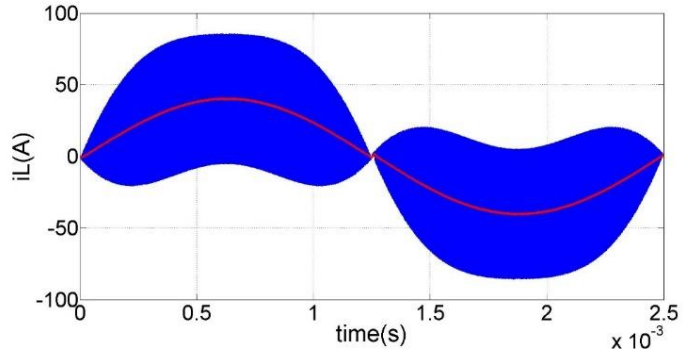


Figure 2. 8 Simulated inductor current for V_{acrms}: 115 V, V_{dc}: 270 V, P_o: 3.3 kW, f_l: 400 Hz, f_s: 1 MHz

2.3 Efficiency and EMI Noise Comparison

Based on analytical loss model and simulation, a loss comparison is shown below. The converter specifications for each modulation are shown in Table 2.1. The loss comparison is shown in Fig. 2.9. A key point to note is that in hard switching conditions in CCM, the turn-on losses are much higher (due to reverse recovery process of body diode of auxiliary switch) than turn-off losses which necessitates the need of soft switching turn on. The turn off losses are almost independent of current during the entire range of operation and very low as compared to the turn-on losses.

	CRM	TCM	CFTCM
V_{inrms}	115 V	115 V	115 V
P_o	3.3 kW	3.3 kW	3.3 kW
I_{Lrms}	28.7 A	28.7 A	28.7 A
V_{dc}	270 V	270 V	270 V
L	0.8 µH	0.74 µH	0.74 µH
f_{sw}	1-2.5 MHz	1-2.5 MHz	1 MHz

Table 2. 1 Converter Specifications

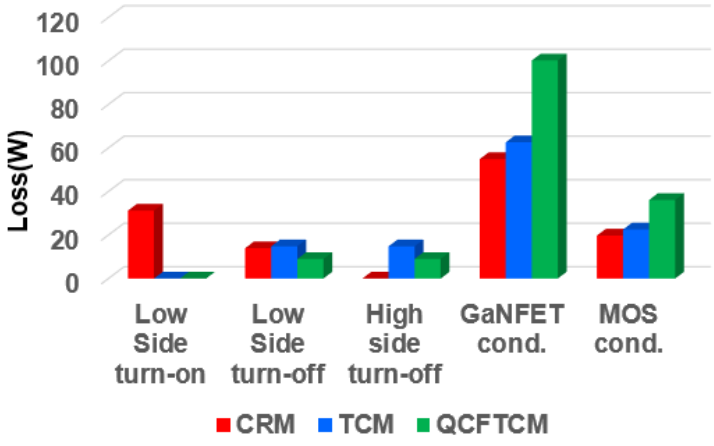


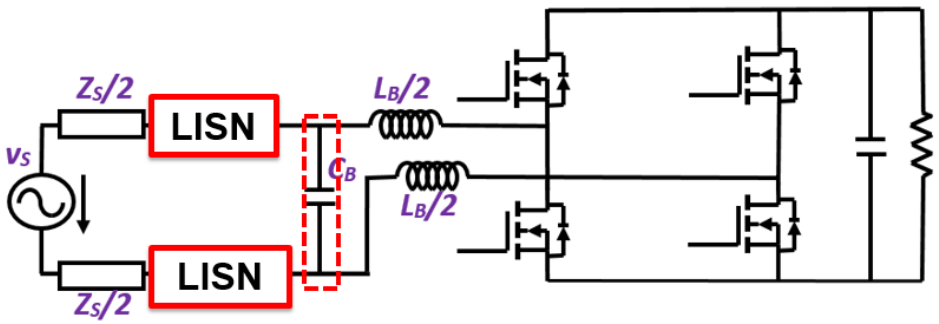
Figure 2. 9 Loss Comparison of CRM, TCM and QCFTCM

EMI noise measurement method discussed in this paper is based on the procedure discussed in [A.9]. This procedure is based on the analysis of conducted EMI problems and the use of an

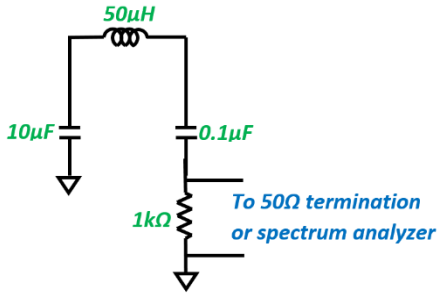
EMI diagnostic tool-noise separator. The noise separator is used to separate differential-mode (DM) and common-mode (CM) noise which greatly simplifies the filter design process. Fig. 2.10(a) shows the setup diagram of a typical conducted EMI measurement. The line impedance stabilizing network (LISN) required in the measurement contains inductors, capacitors and 50Ω resistors as shown in Fig. 2.10(b). The noise current that flows through these resistors, expressed in frequency ranging from 150 KHz to 30 MHz for DO-160E limit, is by definition the conducted EMI. The noise current, flowing through the 50Ω resistors contains both common-mode (CM) noise and differential-mode (DM) noise. The DM current (i_{DM}) and CM current (i_{CM}) are given by:

$$i_{DM} = \left|\frac{i_1 - i_2}{2}\right|, i_{CM} = \left|\frac{i_1 + i_2}{2}\right| \tag{37}$$

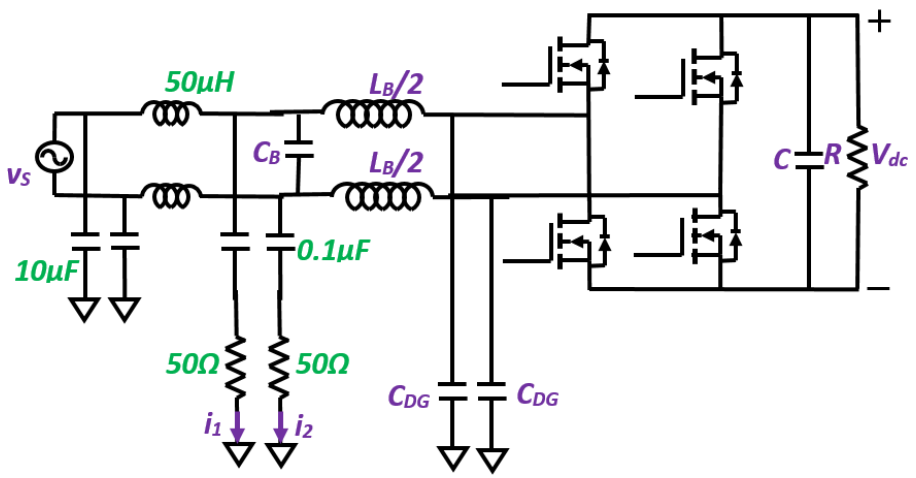
where i_1 and i_2 are the currents flowing through the 50Ω resistors as shown in Fig. 2.10(c). The CM current flows through the parasitic drain-to-gate capacitance (C_{DG}) of the GaNFETs whose value is approximately equal to 2 pF.



(a)



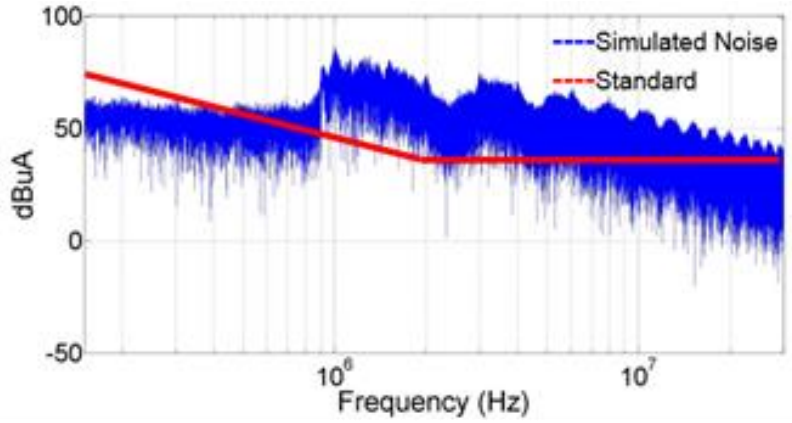
(b)



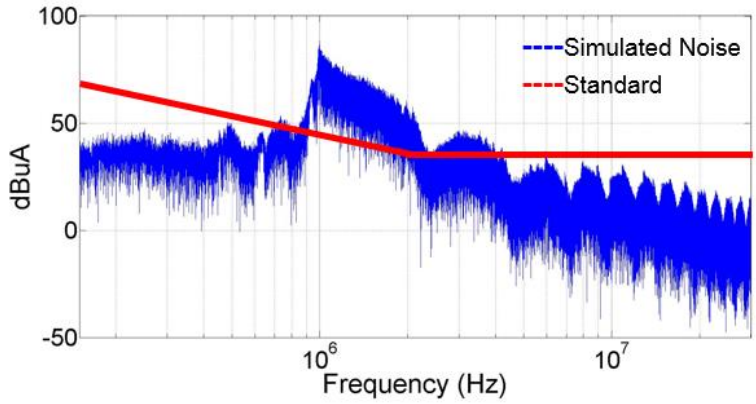
(c)

Figure 2. 10 (a) Test setup for conducted EMI measurement (b) Equivalent circuit of LISN (c) Circuit schematic for measurement setup

The simulated noise spectrum for CRM and CFTCM is shown in Figs. 2.11 and 2.12 respectively. As CRM and TCM current ripple is similar, TCM noise spectrum is not shown. As expected, the DM noise of CFTCM is larger owing to high ripple in the current.

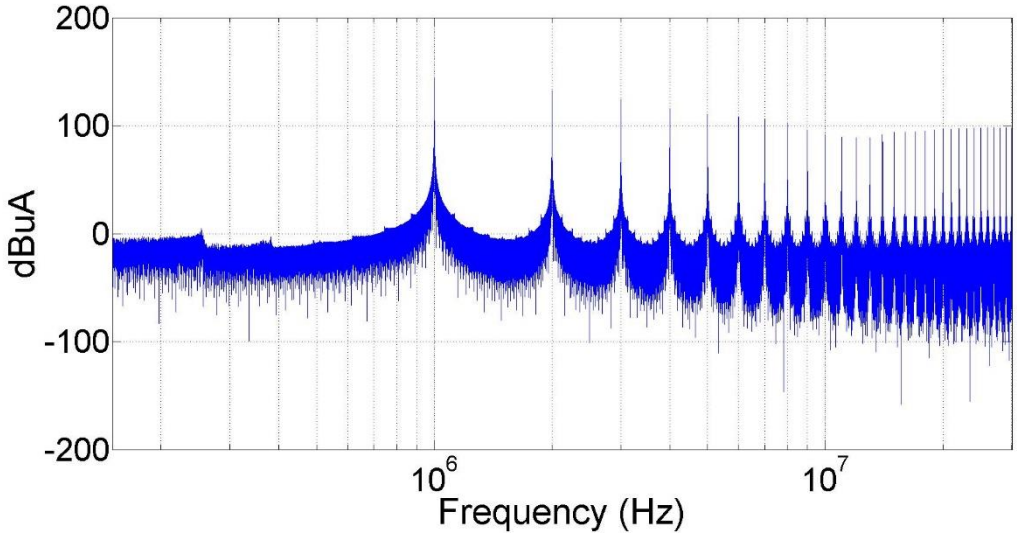


(a)

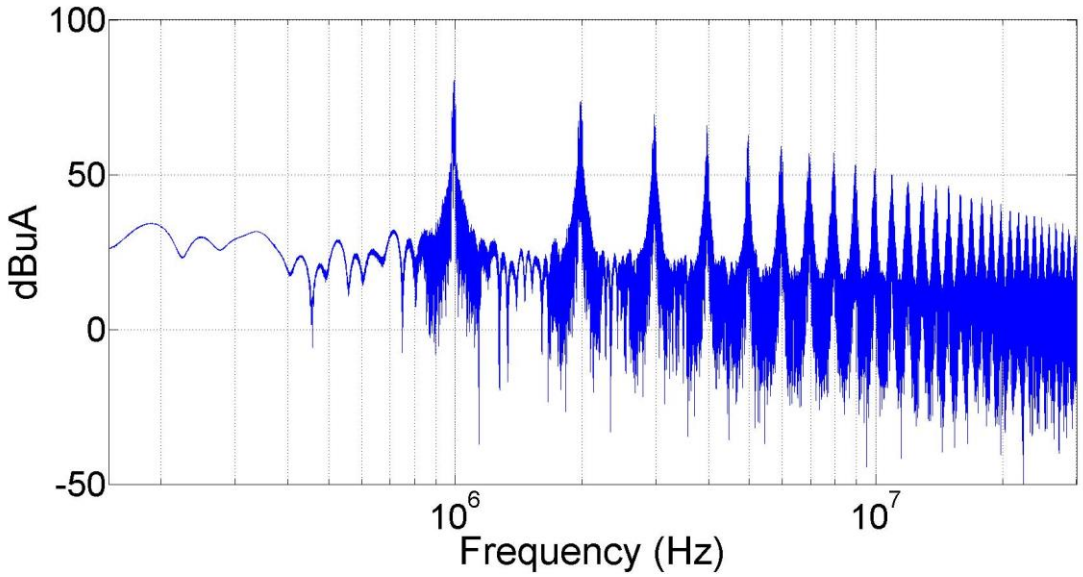


(b)

Figure 2. 11 Simulated EMI noise for CRM (a) Base line CM Noise (b) Base line DM Noise



(a)



(b)

Figure 2. 12 Simulated EMI noise for CFTCM (a) Base line CM Noise (b) Base line DM Noise

2.4 Summary

Since CRM control leads to variable switching frequency, in this chapter it is modified to achieve constant switching frequency by shaping the envelope of current ripple accordingly. The current has higher negative and positive current peaks leading to larger ripple. This technique has ZVS turn-on during the entire mains period which results in lower switching losses. However due to higher current ripple, QCFTCM has 67 % more conduction losses at 270 V DC voltage and 3.3 kW power level.

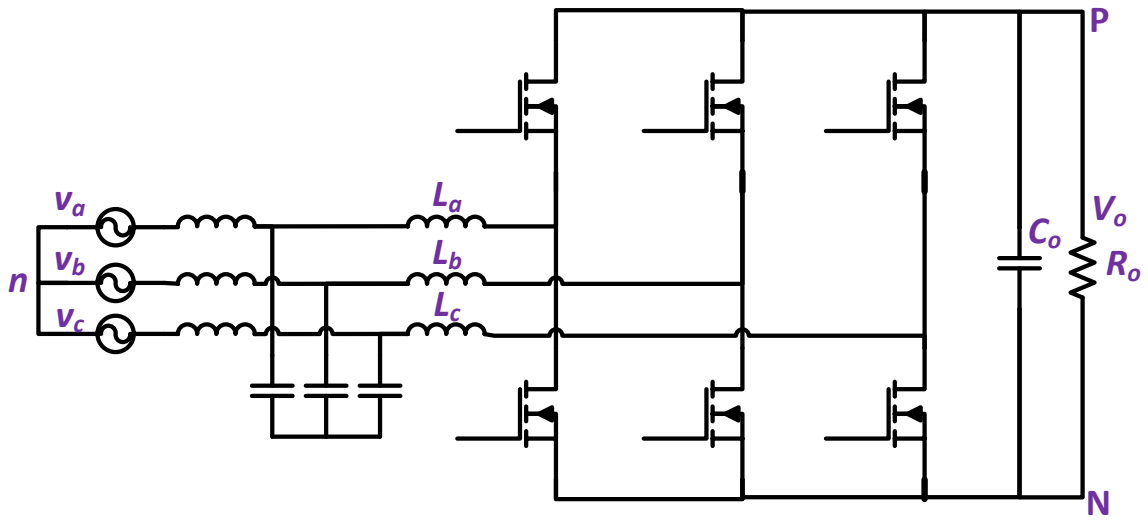
The efficiency achieved in QCFTCM is higher than that of CRM but lower than TCM for GaN 650 V/ 30 A devices. Since QCFTCM has higher current ripple, it requires a larger DM filter but interleaving can be considered to solve this issue as perfect ripple cancellation can be obtained in quasi constant frequency case. Further, QCFTCM can be extended to three-phase systems.

Chapter 3. Proposed TCM for Three-Phase Two-Level Converters: Unity Power Factor

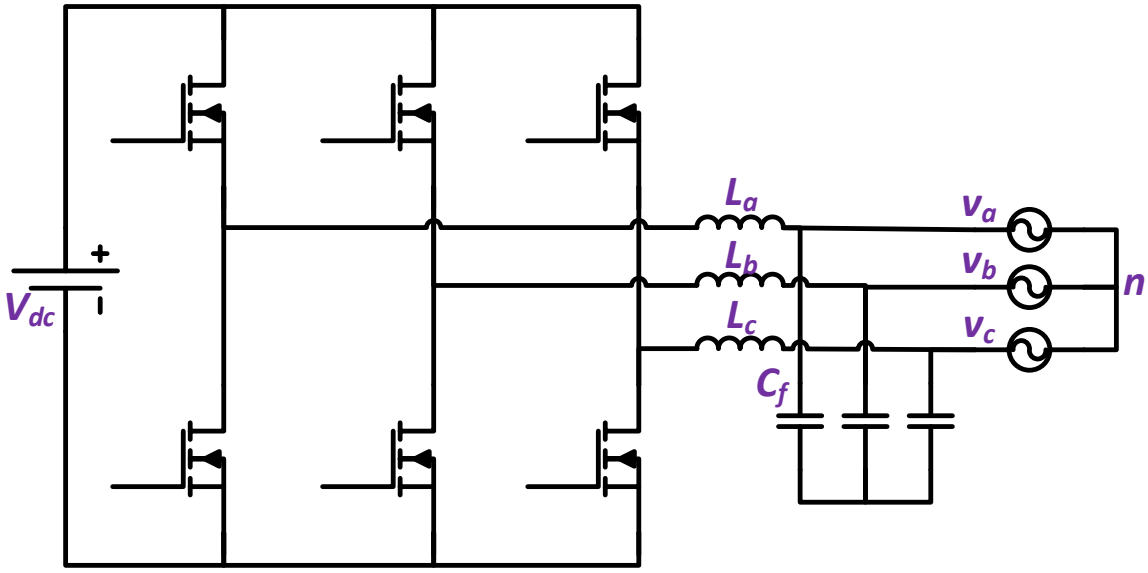
As discussed in the previous chapters, due to high turn-on losses, efficient high frequency operation necessitates soft turn-on. In earlier chapters, it was mentioned how ZVS turn-on can be achieved by pulling current in both directions such that the body diode anti parallel to the device starts conducting before the device is turned on. Thus, the current has high frequency triangular ripple, hence this control is called Triangular Current Mode (TCM) control. The ripple has to be maintained such that the average current is sinusoidal.

In state-of-the-art TCM control for three-phase two-level converters, if phase synchronized operation is maintained, the average currents are not sinusoidal as discussed in Chapter 1. In case of unity power factor, the average current has to be in phase with the voltage with a distortion factor of >0.99. However, conventional CRM with phase synchronization is unable to generate a sinusoidal waveform, it is shown in Chapter 1 how conventional CRM is modified in a VIENNA Rectifier in [C.21] by adding another switching state in the switching cycle. This switching state pulls the DCM current higher adding a required second degree of freedom to control two phase currents. Hence, TCM with phase synchronization and average sinusoidal currents is proposed in this chapter for two-level converters running in rectifier and inverter mode. The converter topology is shown in Fig. 3.1.

A combination of CRM+DCM leads to phase synchronization, in unidirectional topologies in each sector one phase operated in DCM and two operate in CRM. It is shown in this chapter how one of the phases can be clamped in bidirectional topologies saving on the turn-off losses. Thus the converter is proposed to operate in a combination of TCM+DCM+Clamped modes of operation.



(a)



(b)

Figure 3. 1 Three-phase tw- level converter operating in (a) rectifier mode (b) inverter mode

The concept of operating the converter in a combination of CRM+DCM+Clamped modes is also introduced in research published in similar timeline [C.23]. However, the discussion in these publications is limited to unity power factor. The difference between this work and the methods discussed in [C.23] and [C.24] is that the methods proposed in this dissertation achieve complete ZVS turn-on for both DCM and TCM phase, thus minimizing the losses. [C.24] only discusses valley switching for DCM phase which leads to significant losses at high switching frequency and

also creates the issues of accurate dead time calculation and modeling of the converter considering all non-idealities.

3.1 Rectifier Mode

The circuit schematic of a three-phase two-level boost PFC is shown in Fig. 3.1. The currents flowing out of the grid are considered positive, the basic theory for achieving soft switching and sinusoidal currents is discussed below. The basic principle behind achieving soft switching remains the same as in single-phase converter, to allow the body diode to conduct before the device is turned on by pulling current in negative direction. However, for achieving sinusoidal currents in all the three phases, as mentioned previously two independent control variables are required.

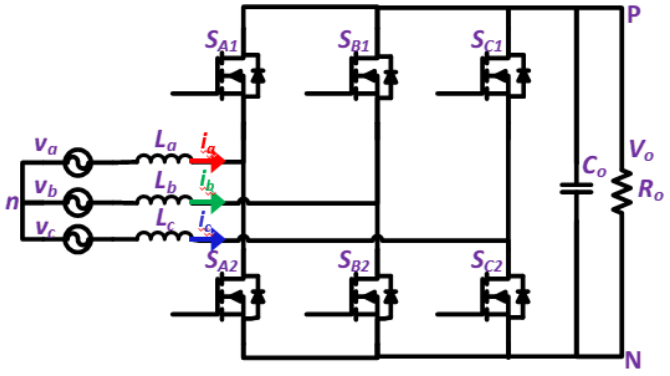


Figure 3. 2 Circuit Schematic of three-phase six-switch two-level boost PFC

3.1.1 Theory

The line cycle can be divided into twelve sectors (like in conventional CRM discussed in Chap. 1) as shown in Fig. 3.3, where in each sector, the voltage direction and relative magnitude of the three-phase input voltage is same. The input voltages are given by:

$$v_a = V_m \sin(\omega t) \tag{38a}$$

$$v_b = V_m \sin(\omega t - 2\pi/3) \tag{38b}$$

$$v_c = V_m \sin(\omega t + 2\pi/3) \tag{38c}$$

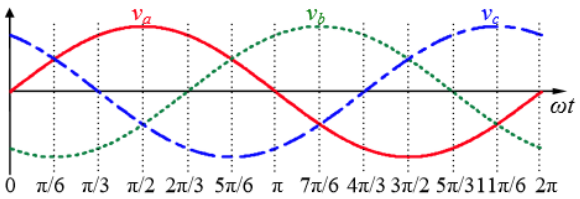


Figure 3. 3 Line cycle divided into twelve sectors

One switching cycle waveform in sector I ($0<\omega t<\pi/6$) is shown in Fig. 3.4. Each switching cycle can be divided into 9 intervals including the dead times. The input voltages are assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency (f_l). The detailed operation in each interval is discussed below.

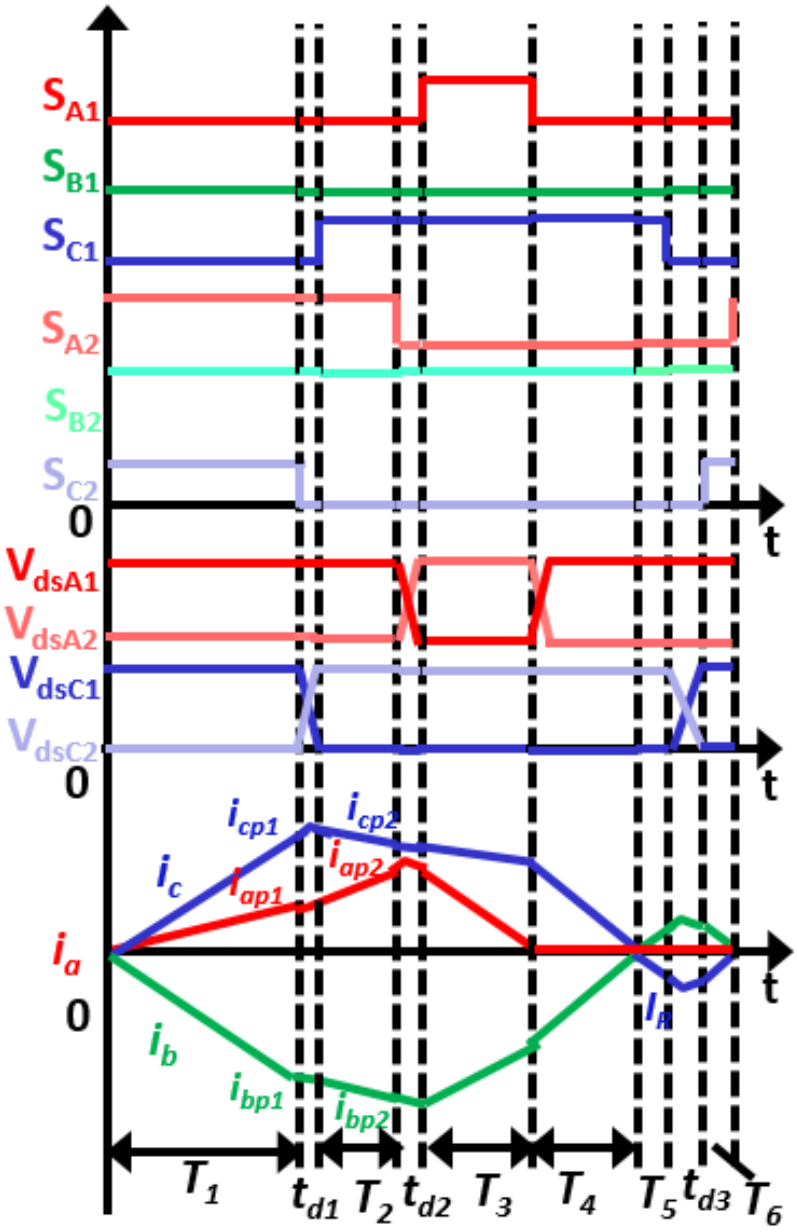


Figure 3. 4 One switching cycle waveform for proposed TCM in Sector I

Interval I (0-T_1)

During interval I, S_{A2}, S_{B2}, S_{C2} conduct, i.e. all the phases are connected to N point of the DC bus, the phase currents increase directly proportional to respective phase voltages. The equivalent circuit is shown in Fig. 3.5, the phase currents' slopes are given by:

$$di_a / dt = v_a / L \tag{39a}$$

$$di_b / dt = v_b / L \tag{39b}$$

$$di_c / dt = v_c / L \tag{39c}$$

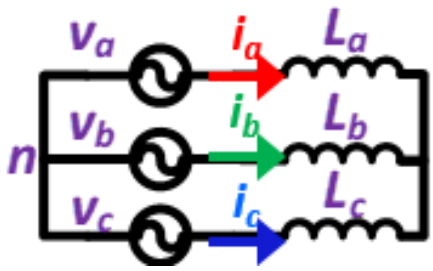


Figure 3. 5 Equivalent circuit in Interval I

The peak currents are given by:

$$i_{ap1} = v_a T_1 / L \tag{40a}$$

$$i_{bp1} = v_b T_1 / L \tag{40b}$$

$$i_{cp1} = v_b T_1 / L \tag{40c}$$

After i_c reaches i_{cp1}, S_{C2} is turned off as shown in Fig. 3.4. Since the magnitude of phase A voltage (v_a) is minimum in sector I, i_a reaches least peak value in magnitude (i_{ap1}).

Interval II (T_1-T_1+t_{d1})

After S_{C2} is turned off, resonance occurs in between phase C devices' output source capacitors (C_{oss}) and L_c as shown in Fig. 3.6. By the end of this interval, V_{dsC2} reaches V_o and V_{dsC1} reaches 0 (as shown in Fig. 3.4), the body diode of S_{C1} starts conducting and the switch can be turned on at 0 V.

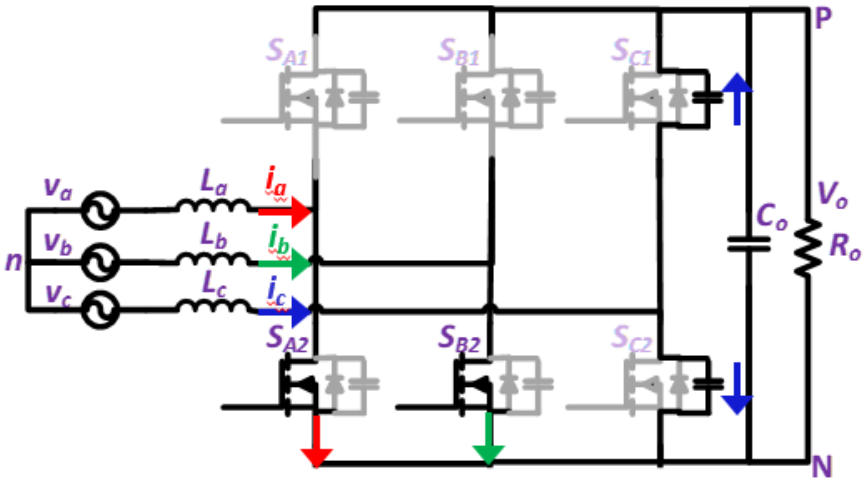


Figure 3. 6 Resonance between device output source capacitors and inductors during Interval II

Interval III (T_1+t_{d1}-T_1+t_{d1}+T_2)

At the beginning of interval III, S_{C1} is turned on, thus i_a continues to increase. The equivalent circuit is shown in Fig. 3.7. The phase currents' slopes are given by:

$$di_a / dt = (v_a + V_o / 3) / L \tag{41a}$$

$$di_b / dt = (v_b + V_o / 3) / L \tag{41b}$$

$$di_c / dt = (v_c - 2V_o / 3) / L \tag{41c}$$

The peak currents are given by:

$$i_{ap2} = i_{ap1} + \frac{1}{L}(v_a + V_o / 3)T_2 \tag{42a}$$

$$i_{bp2} = i_{bp1} + \frac{1}{L}(v_b + V_o / 3)T_2 \tag{42b}$$

$$i_{cp2} = i_{cp1} + \frac{1}{L}(v_c - 2V_o / 3)T_2 \tag{42c}$$

After i_a reaches i_{ap2}, S_{A2} is turned off as shown in Fig. 3.4.

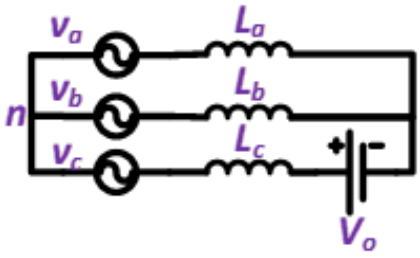


Figure 3. 7 Equivalent circuit in Interval III

Interval IV (T_1+t_{d1}+T_2- T_1+t_{d1}+T_2+t_{d2})

After S_{A2} is turned off, resonance occurs in between phase A devices' output source capacitors and L_a as shown in Fig. 3.8. By the end of this interval, V_{dsA2} reaches V_o and V_{dsA1} reaches 0 (as shown in Fig. 3.4), the body diode of S_{A1} starts conducting and the switch can be turned on at 0 V.

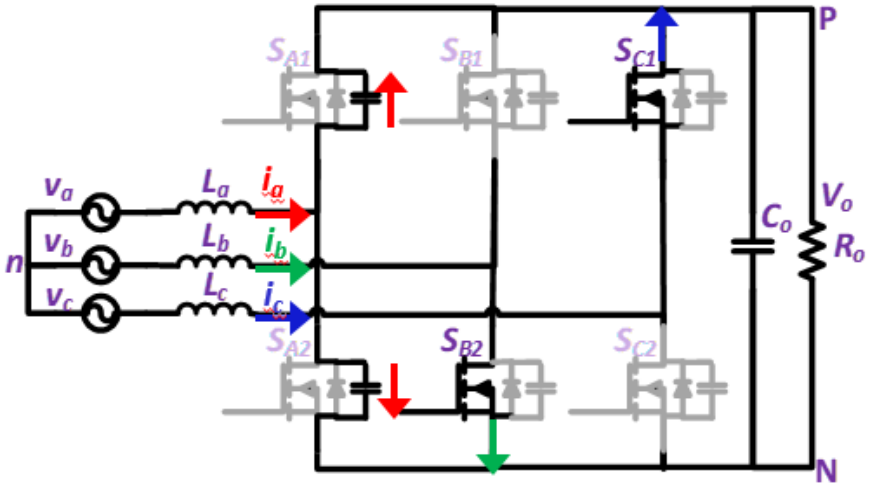


Figure 3. 8 Resonance between device output source capacitors and inductors during Interval IV

Interval V (T_1+t_{d1}+T_2+t_{d2}- T_1+t_{d1}+T_2+t_{d2}+T_3)

At the beginning of interval V, S_{A1} is turned on at 0 V. Thus i_a starts to fall, the equivalent circuit is shown in Fig. 3.9, the phase currents' slopes are given by:

$$di_a / dt = (v_a - V_o / 3) / L \tag{43a}$$

$$di_b / dt = (v_b + 2V_o / 3) / L \tag{43b}$$

$$di_c / dt = (v_c - V_o / 3) / L \tag{43c}$$

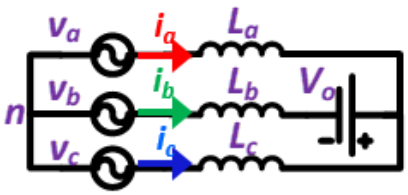


Figure 3. 9 Equivalent circuit in Interval V

The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{1}{L}(v_b + 2V_o / 3)T_3 \tag{44a}$$

$$i_{cp3} = i_{cp2} + \frac{1}{L}(v_c - V_o / 3)T_3 \tag{44b}$$

Since in sector I the magnitude of v_a is minimum, i_a reaches 0 first and this interval ends when i_a reaches zero, S_{A1} is turned off at the end of *Interval* V.

Interval VI (T_1+t_{d1}+T_2+t_{d2}+T_3- T_1+t_{d1}+T_2+t_{d2}+T_3+T_4)

In this mode, S_{B2} and S_{C1} conduct, the equivalent circuit is shown in Fig. 3.10. The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (V_o + v_b - v_c) / 2L \tag{45}$$

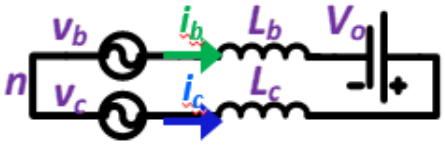


Figure 3. 10 Equivalent circuit in Interval VI

Thus i_c falls to zero during this interval, this interval ends when i_c reaches zero.

Interval VII (T_1+t_{d1}+T_2+t_{d2}+T_3+T_4- T_1+t_{d1}+T_2+t_{d2}+T_3+T_4+T_5)

In CRM, the device is turned off right after the current reaches zero, however in TCM a small negative current is allowed for full ZVS as discussed in Chapter 1. After i_c reaches 0, S_{C1} is allowed to conduct for a little more time till i_c reaches a negative value I_R which is enough to discharge the phase C devices' output source capacitors for ZVS turn-on of S_{C2}. The equivalent circuit is the same as in Interval VI. At the end of this interval, S_{C1} is turned off. The peak negative current I_R is given by:

$$I_R = -\frac{(V_o + v_b - v_c)T_5}{2L} \tag{46}$$

Interval VIII (T_1+t_{d1}+T_2+t_{d2}+T_3+T_4+T_5- T_1+t_{d1}+T_2+t_{d2}+T_3+T_4+ T_5+t_{d3})

After S_{C1} is turned off, resonance occurs in between phase C devices' output source capacitors and L_c as shown in Fig. 3.11. By the end of this interval, V_{dsC1} reaches V_o and V_{dsC2} reaches 0 (as shown in Fig. 3.4), the body diode of S_{C2} starts conducting (as i_c<0) and the switch can be turned on at 0 V.

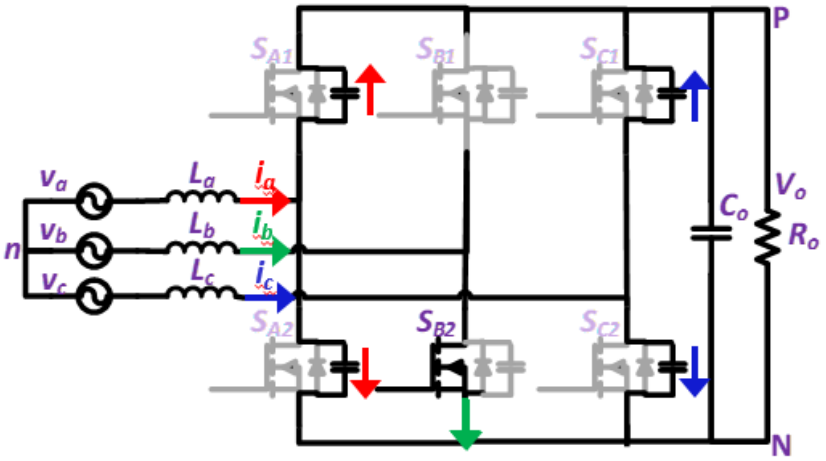


Figure 3. 11 Resonance between device output source capacitors and inductors during Interval VIII

Interval IX (T_1+t_{d1}+T_2+t_{d2}+T_3+T_4+T_5+t_{d3}- T_1+t_{d1}+T_2+t_{d2}+T_3+ T_4+T_5+t_{d3}+T_6)

At the beginning of Interval IX, S_{C2} is turned on (as shown in Fig. 3.4), the equivalent circuit is shown in Fig. 3.12. The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (v_b - v_c) / 2L \tag{47}$$

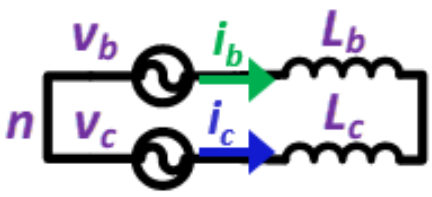


Figure 3. 12 Equivalent circuit in Interval IX

The peak negative current I_R is given by:

$$I_R = \frac{(v_b - v_c)T_6}{2L} \tag{48}$$

Thus i_c starts to increase again and this interval ends when i_c and i_b reach zero and a new switching cycle starts form here.

As the switching cycle times depend on phase voltages which vary during line cycle, the switching frequency varies in TCM.

3.1.2 Mathematical Model

While calculating the switching times, ideal devices are considered, dead times are neglected for average current calculation as they are very small (<0.01 %) as compared to the switching times. The current ripple caused by parasitic capacitors is also neglected for switching times calculation as a model including the effect of parasitic capacitors on average currents is very complex.

T_5 and T_6, calculated from (46) and (48) are given by:

$$T_5 = \frac{-2I_R L}{(V_o + v_b - v_c)} \tag{49a}$$

$$T_6 = \frac{2I_R L}{(v_b - v_c)} \tag{49b}$$

T_3 and T_4 can be derived in terms of T_1 and T_2 derived from the following equations:

$$i_{ap2} + \frac{1}{L}(v_a - V_o/3)T_3 = 0 \tag{50a}$$

$$i_{bp3} + \frac{1}{L}\frac{(V_o + \mathrm{v}_b - \mathrm{v}_c)}{2}T_4 = 0 \tag{50b}$$

Where i_{ap2} and i_{bp3} are derived using Eqns. (40), (42) and (44). Thus T_1 and T_2 can be derived from average current equations:

$$i_{aavg} = \frac{i_{ap1}\frac{T_1}{2} + (i_{ap1} + i_{ap2})\frac{T_2}{2} + i_{ap2}\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} = k_1 v_a \tag{51a}$$

$$i_{bavg} = \frac{i_{bp1}\frac{T_1}{2} + (i_{bp1} + i_{bp2})\frac{T_2}{2} + (i_{bp2} + i_{bp3})\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} + \frac{i_{bp3}\frac{T_4}{2} - I_R(\frac{\mathrm{T}_5 + \mathrm{T}_6}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_b \tag{51b}$$

Where k_1 is given by:

$$k_1 = 2P_o / 3V_m^2 \tag{51c}$$

P_o- Output Power

V_m- Peak phase input voltage

$$V_m = \sqrt{2}V_{rms} \tag{52}$$

V_{rms}- RMS of input phase voltage

From the above equations, the switching times T_1 and T_2 are calculated as:

$$T_1 = 2Lk_1 \tag{53a}$$

$$T_2 = \frac{2I_R L + 2Lk_1(v_a + 2v_b)}{v_a + 2v_b} \tag{53b}$$

The switching times for a 1.2 kW, 400 V V_o, 115 V_{inrms}, f_s~ 1MHz, L= 4 µH are shown in Fig. 3.13. The inductance is chosen to obtain the desired minimum switching frequency. Minimum I_R for ZVS turn-on is calculated as -1 A.

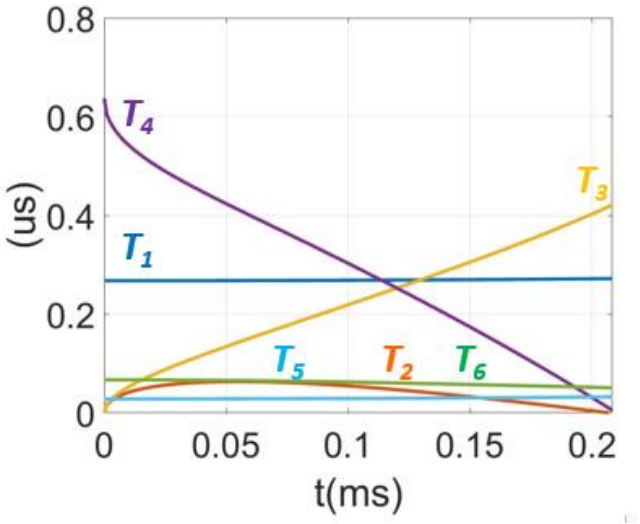


Figure 3. 13 Switching times 1.2 KW P_o, 400 V V_o, 115 V V_{inrms}, L~ 4 µH

3.1.3 Full Line Cycle Control

As mentioned above, after every 30°, the operation is repetitive, hence the same formulae can be used after every 30° by replacing the phase that operates in DCM, TCM and clamped mode. The

decision of mode of operation for each phase is based on the relative magnitude of average currents. For unity power factor, the relative magnitude of required average currents and phase voltages is the same. The average phase currents can be denoted as $|i_{av}|_{\min}$, $|i_{av}|_{\text{med}}$ and $|i_{av}|_{\max}$ where the relationship between these voltages is defined as:

$$\left|i_{av}\right|_{\max} > \left|i_{av}\right|_{\text{med}} > \left|i_{av}\right|_{\min} \tag{53}$$

The following modes of operation are assigned as per the relative absolute value of average phase current:

$|i_{av}|_{\min} \rightarrow$DCM

$|i_{av}|_{\text{med}} \rightarrow$TCM

$|i_{av}|_{\max} \rightarrow$Clamped

The phase with maximum current is clamped similar to clamped SVM technique to minimize the losses.

Since in sector I,

Phase A$\rightarrow |i_{av}|_{\min}$

Phase B$\rightarrow |i_{av}|_{\max}$

Phase C$\rightarrow |i_{av}|_{\text{med}}$

Hence, phase A operates in DCM, phase B is clamped and phase C operates in TCM. As mentioned above, this relative relationship changes after every 30^{o}, so does the phases operating in DCM, TCM or clamped mode of operation. The full line cycle control is shown in Fig. 3.14.

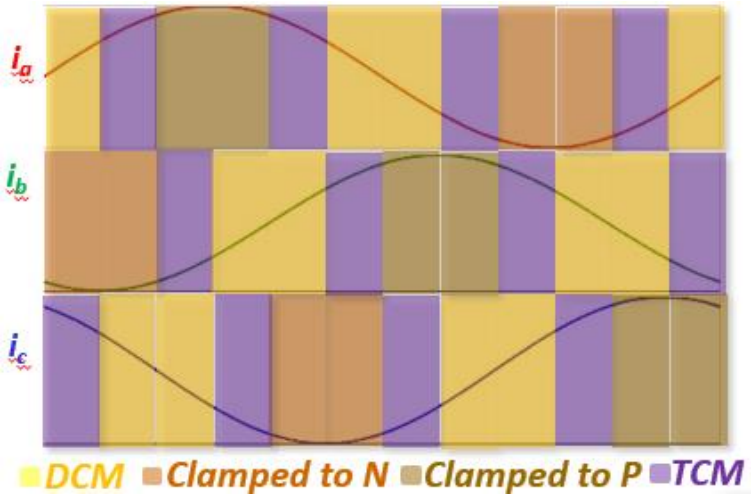


Figure 3. 14 Full line cycle control showing control symmetry after every 30°

The total switching cycle time (T_s) is given by:

$$T_s = \sum_{i \in 1-6} T_i \tag{54}$$

The switching frequency (f_s) is given by:

$$f_s = 1/T_s \tag{55}$$

The switching frequency variation for 0-60° is shown in Fig. 3.15. The graph is symmetrical after every 30°.

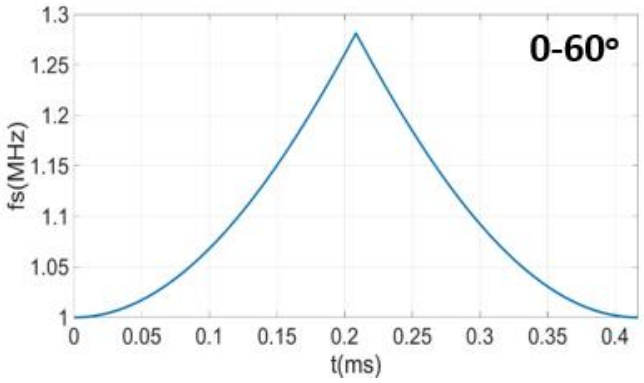


Figure 3. 15 Switching frequency variation for 1.2 KW P_o, 400 V V_o, 115 V V_{inrms}, L~ 4 µH

3.1.4 Verification by Simulation

The converter is simulated from pre-calculated switching times (T_1, T_2, T_3, T_5 and T_6). T_4 is not pre-calculated, the end of T_4 is detected by zero crossing of TCM phase. The simulated phase currents are shown in Fig. 3.16, ideal devices are considered in this simulation. The zoomed in

waveforms in sector I are shown in Fig. 3.17. It is shown how ZVS turn-on is achieved by driving the current negative.

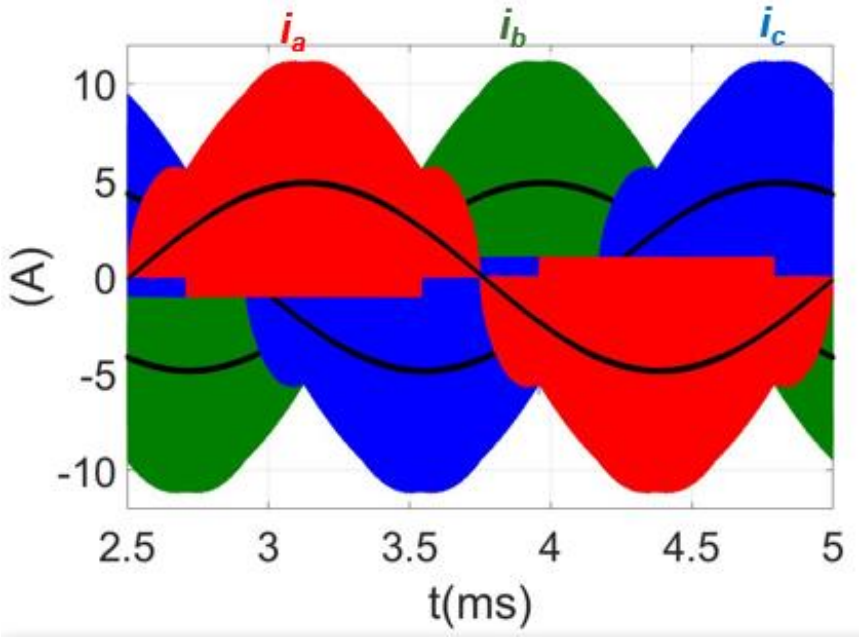
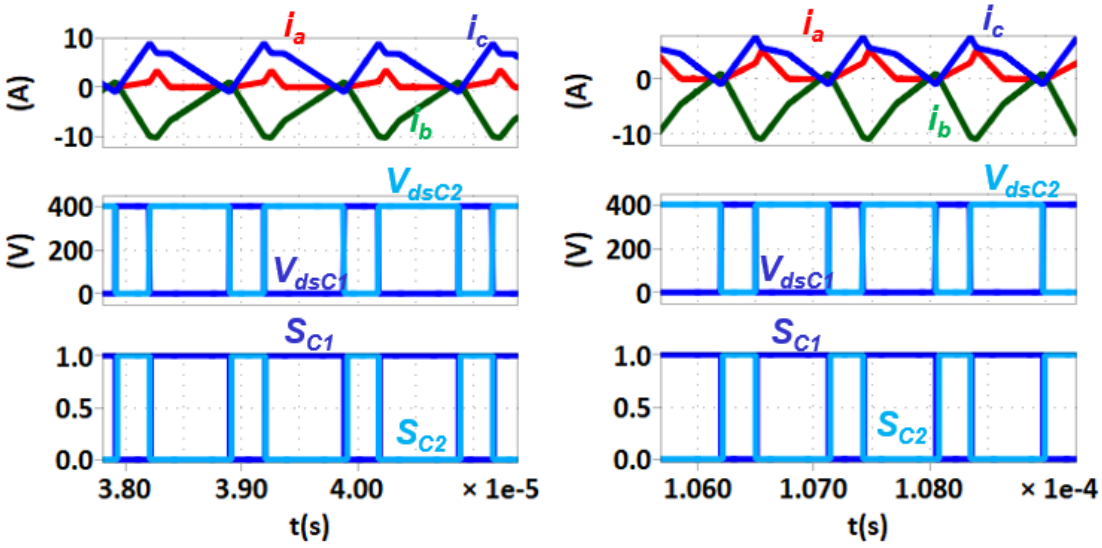
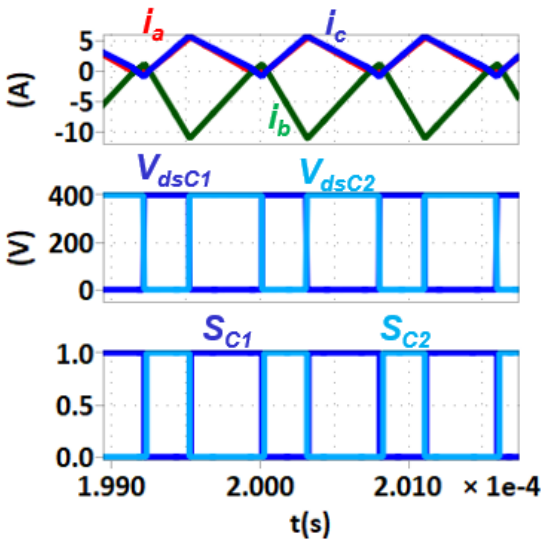


Figure 3. 16 Simulated phase currents for 1.2 KW P_o, 400 V V_o, 115 V V_{inrms}, L~ 4 µH



(a) (b)



(c)

Figure 3. 17 Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector I

The loss breakdown comparison between CCM at 68 kHz and proposed TCM+DCM+Clamped algorithm at 1 MHz is shown in Fig. 3.18. As compared to state-of-the-art Si three-phase converters operating in CCM at ~50 kHz, there is a ~2.5 times increase in power density as the filter size is reduced by 60 %. Thus TCM achieves high density while maintaining the same efficiency.

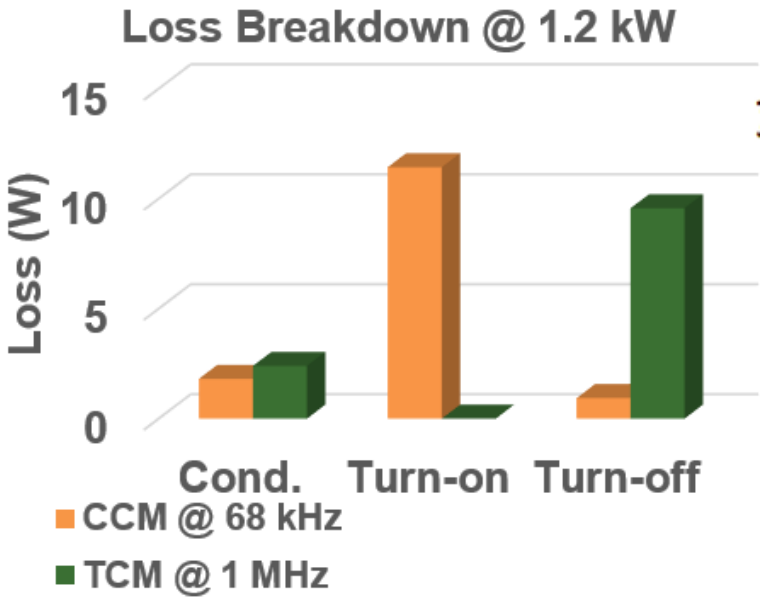


Figure 3. 18 Loss Breakdown Comparison of CCM at 50 kHz and TCM+DCM+Clamped at 1 MHz at 1.2 KW P_o, 400 V V_o, 115 V V_{inrms}

3.2 Inverter Mode

TCM for converter operating in rectifier mode is discussed above. However, a bidirectional converter operates in both inverter and rectifier mode. In inverter mode, power gets transferred from DC-AC. Solar panels connected to grid and motor drives operate converter in inverter mode for most of the time. The schematic of a three phase two level inverter is shown in Fig. 3.19. It is to be noted that here, the currents flowing into the grid are taken as positive unlike for a rectifier, the current flowing out of the grid is taken as positive.

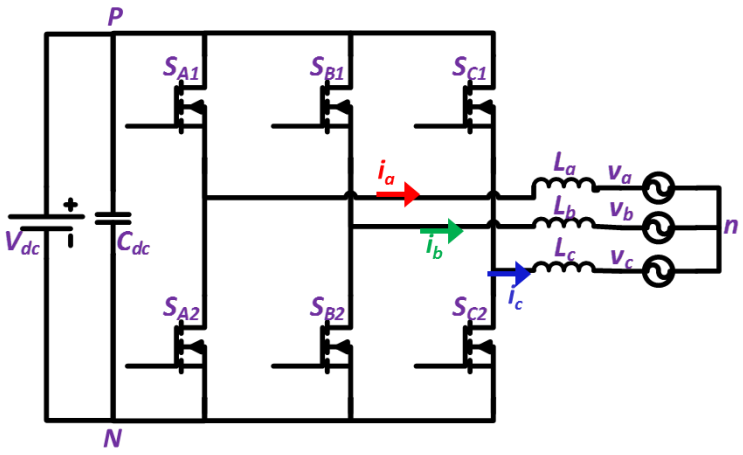


Figure 3. 19 Circuit schematic of three-phase six-switch two-level inverter

The basic theory for achieving soft switching and sinusoidal currents with TCM+DCM+Clamped algorithm is discussed below. The basic principle of achieving soft switching remains the same as in single-phase converter, to make the body diode conduct before the device is turned on by pulling current in negative direction.

3.2.1 Theory

The line cycle can still be divided into 12 sectors (similar to rectifier mode) as shown in Fig. 3.3, where in each sector, the voltage direction and relative magnitude of the three-phase input voltage is same. The input voltages are given by Eq 38.

One switching cycle waveform in sector I ($0<\omega t<\pi/6$) is shown in Fig. 3.20. Each switching cycle can be divided into 6 intervals, the detailed operation during dead time is not discussed for

the sake of brevity. The input voltages are assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency (f_l). The detailed operation in each interval is discussed below.

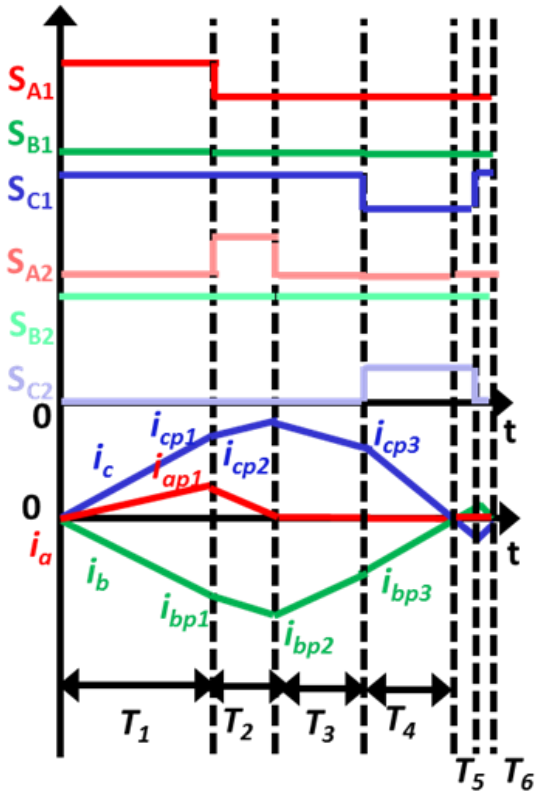


Figure 3. 20 One switching cycle waveform for TCM in inverter in Sector I for case a: when i_a reaches 0 before i_c reaches peak value i_{cp2}.

Interval I (0-T_1)

During interval I, S_{A1}, S_{B2}, S_{C1} conduct leading to increase in i_a and i_c, the equivalent circuit is shown in Fig. 3.21, the phase currents' slopes are given by:

$$di_a / dt = (V_{dc} / 3 - v_a) / L \tag{56a}$$

$$di_b / dt = (-2V_{dc} / 3 - v_b) / L \tag{56b}$$

$$di_c / dt = (V_{dc} / 3 - v_c) / L \tag{56c}$$

The peak currents are given by:

$$i_{ap1} = \frac{(V_{dc}/3 - v_a)}{L} T_1 \tag{57a}$$

$$i_{bp1} = \frac{(-2V_{dc}/3 - v_b)}{L} T_1 \tag{57b}$$

$$i_{cp1} = \frac{(V_{dc}/3 - v_c)}{L} T_1 \tag{57c}$$

After i_a reaches i_{ap1}, S_{A1} is turned off as shown in Fig. 3.20.

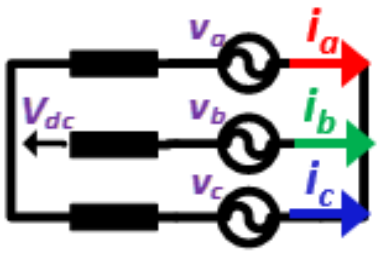


Figure 3. 21 Equivalent circuit in Interval I

Interval II (T_1-T_1+T_2)

After S_{A1} is turned off, resonance occurs in between phase A devices' output source capacitors (C_{oss}) and L_a, Because of this resonance, V_{dsA1} reaches V_{dc} and V_{dsA2} reaches 0, the body diode of S_{A2} starts conducting and the switch can be turned on at 0 V. After S_{A2} is turned on, i_a starts to drop. The equivalent circuit is shown in Fig. 3.22, the phase currents' slopes are given by:

$$di_a / dt = (-V_{dc}/3 - v_a) / L \tag{58a}$$

$$di_b / dt = (-V_{dc}/3 - v_b) / L \tag{58b}$$

$$di_c / dt = (2V_{dc}/3 - v_c) / L \tag{58c}$$

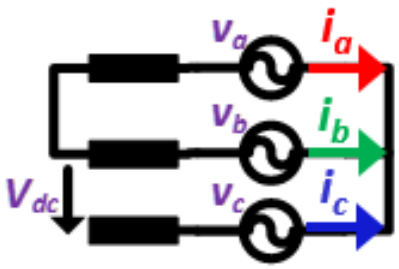


Figure 3. 22 Equivalent circuit in Interval II

Interval II can end in two cases. The first one when current i_a reaches zero (IIa), the second one when i_c when reaches peak current i_{cp2} before i_a reaches 0 (IIb). IIa happens near the beginning of sector I when v_a is relatively small and IIb happens near the end of sector I when v_a is comparable to v_c. Both the cases are discussed below.

Interval IIa

When i_a reaches 0 before i_c reaches peak value i_{cp2}, the peak currents are given by:

$$i_{bp2} = i_{bp1} + \frac{1}{L}(-V_{dc}/3 - v_b)T_2 \tag{59a}$$

$$i_{cp2} = i_{cp1} + \frac{1}{L}(2V_{dc}/3 - v_c)T_2 \tag{59b}$$

This interval ends when i_a reaches 0. After i_a reaches 0, S_{A2} is turned off as shown in Fig. 3.20.

Interval IIb

When i_c reaches peak value i_{cp2} before i_a reaches 0, the peak currents are given by:

$$i_{ap2} = i_{ap1} + \frac{1}{L}(-V_{dc}/3 - v_a)T_2 \tag{60a}$$

$$i_{bp2} = i_{bp1} + \frac{1}{L}(-V_{dc}/3 - v_b)T_2 \tag{60b}$$

$$i_{cp2} = i_{cp1} + \frac{1}{L}(2V_{dc}/3 - v_c)T_2 \tag{60c}$$

One switching cycle with currents and gating signals for this case is shown in Fig. 3.23. This interval ends when i_c reaches peak value i_{cp2}. After i_c reaches peak value i_{cp2}, S_{C1} is turned off as shown in Fig. 3.23.

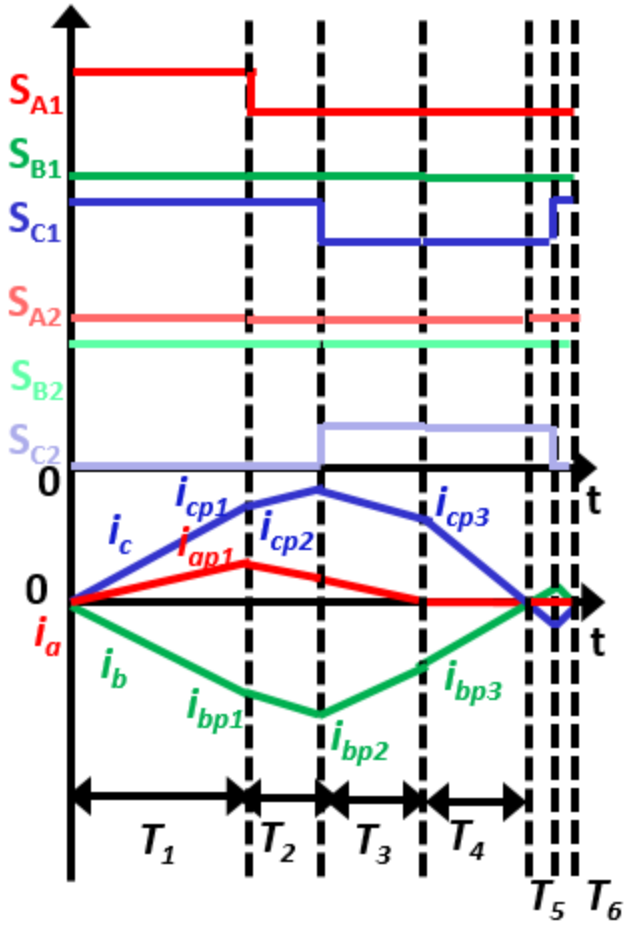


Figure 3. 23 One switching cycle waveform for TCM in inverter in Sector I for case b: when i_c reaches peak value i_{cp2} before i_a reaches 0.

Interval IIIa (T_1+T_2- T_1+T_2+T_3)

S_{A2} is turned off at the beginning of Interval IIIa as shown in Fig. 3.20, S_{B2} and S_{C1} continue to conduct. The equivalent circuit is as shown in Fig. 3.24, the phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (-V_{dc} + v_c - v_b) / 2L \tag{61}$$

When i_c reaches i_{cp3}, S_{C1} is turned off as shown in Fig. 3.20, this marks the end of Interval IIIa. The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{1}{2L}(-V_{dc} + v_c - v_b)T_3 \tag{62a}$$

$$i_{cp3} = i_{cp2} + \frac{1}{2L}(V_{dc} - v_c + v_b)T_3 \tag{62b}$$

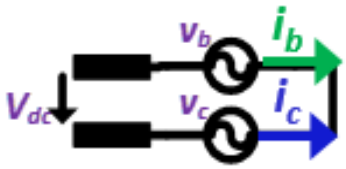


Figure 3. 24 Equivalent circuit in Interval IIIa

Interval IIIb (T_1+T_2- T_1+T_2+T_3)

After S_{C1} is turned off at the end of Interval IIb, resonance occurs in between phase C devices' output source capacitors (C_{oss}) and phase inductor L_c, Because of this resonance, V_{dsC1} reaches V_{dc} and V_{dsC2} reaches 0, the body diode of S_{C2} starts conducting and the switch is turned on at 0 V. After S_{C2} is turned on, i_c starts to drop and i_a continues to drop as shown in Fig. 3.23. The equivalent circuit is shown in Fig. 3.25, the phase currents' slopes are given by:

$$di_a / dt = (-v_a) / L \tag{63a}$$

$$di_b / dt = (-v_b) / L \tag{63b}$$

$$di_c / dt = (-v_c) / L \tag{63c}$$

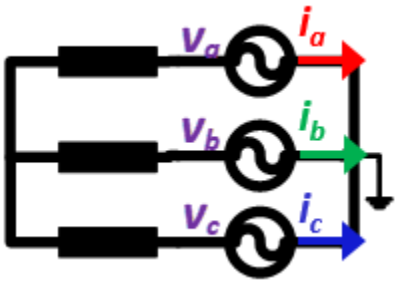


Figure 3. 25 Equivalent circuit in Interval IIIb

This interval ends when i_a reaches 0. When i_a reaches 0, S_{A2} is turned off as shown in Fig. 3.23, this marks the end of Interval IIIb. The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{1}{L}(-v_b)T_3 \tag{64a}$$

$$i_{cp3} = i_{cp2} + \frac{1}{L}(-v_c)T_3 \tag{64b}$$

Interval IV (T_1+T_2+T_3 - T_1+T_2+T_3+T_4)

After S_{C1} is turned off at the end of interval IIIa, resonance occurs in between phase C devices' output source capacitors (C_{oss}) and L_c like in the beginning of interval IIIb. Because of this resonance, V_{dsC1} reaches V_{dc} and V_{dsC2} reaches 0, the body diode of S_{C2} starts conducting and the switch is turned on at 0 V. Since S_{C2} is already on at the beginning of interval IIIb, i_c continues to drop in interval IV after interval IIIb. Hence, whether the currents follow case a or b (Fig. 3.20 or Fig. 3.23), from interval IV, the waveforms follow the same sequence. When S_{C2} and S_{B2} conduct (the equivalent circuit is shown in Fig. 3.26), i_c drops, the phase currents' slope is given by:

$$di_b / dt = -di_c / dt = (v_c - v_b) / 2L \tag{65}$$

This interval ends when i_c reaches 0.

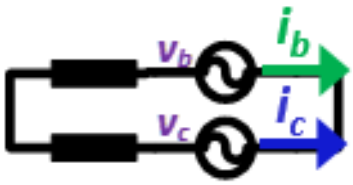


Figure 3. 26 Equivalent circuit in Interval IV

Interval V (T_1+ T_2+ T_3+T_4- T_1+ T_2+ T_3+T_4+T_5)

After i_c reaches 0, S_{C2} is allowed to conduct for a little more time till i_c reaches a negative value I_R which is enough to discharge the phase C devices' output source capacitors for ZVS turn-on of S_{C1}. The equivalent circuit is the same as in Interval IV. At the end of this interval, S_{C2} is turned off. The peak negative current I_R is given by:

$$I_R = \frac{(v_b - v_c)T_5}{2L} \tag{66}$$

Interval VI (T_1+ T_2+ T_3+T_4+ T_5 - T_1+ T_2+ T_3+T_4+ T_5+T_6)

After S_{C2} is turned off, resonance occurs in between phase C devices' output source capacitors and L_c, thus V_{dsC1} reaches V_{dc} and V_{dsC2} reaches 0, the body diode of S_{C1} starts conducting (as i_c<0) and the switch is turned on at 0 V. The equivalent circuit after is shown in Fig. 3.24. The phase currents' slopes are given by Eq. 65.

The peak negative current I_R is given by:

$$I_R = -\frac{(V_{dc} + v_b - v_c)T_6}{2L} \tag{67}$$

Thus, i_c starts to increase again and this interval ends when i_c and i_b reach zero and a new switching cycle starts form here.

3.2.2 Calculation of Conduction Times

While calculating the switching times, ideal devices are considered, dead times are neglected for average current calculation as they are very small as compared to the switching times. T_5 and T_6 are calculated from (66) and (67) for a given I_R. For a part in the beginning of sector I, case a is followed and after a certain degree depending on the relative magnitude of DC and phase voltages, case b is followed.

Case A

For case A, T_2 and T_4 can be derived in terms of T_1 and T_3 from the following equations:

$$i_{ap1} + \frac{1}{L}(-V_{dc}/3 - v_a)T_2 = 0 \tag{68a}$$

$$i_{bp3} + \frac{1}{L}\frac{(v_c - v_b)}{2}T_4 = 0 \tag{68b}$$

Where i_{ap1} and i_{bp3} can be derived using Eqns. (57), (59) and (62). Thus T_1 and T_3 can be derived from average current equations:

$$i_{aavg} = \frac{i_{ap1}(\frac{T_1 + T_2}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_a \tag{69a}$$

$$i_{bavg} = \frac{i_{bp1}\frac{T_1}{2} + (i_{bp1} + i_{bp2})\frac{T_2}{2} + (i_{bp2} + i_{bp3})\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} + \frac{i_{bp3}\frac{T_4}{2} - I_R(\frac{T_5 + T_6}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_b \tag{69b}$$

Case B

For case B when DCM phase conducts for 3 switching states, T_3 and T_4 can be derived in terms of T_1 and T_2 from the following equations:

$$i_{ap2} + \frac{1}{L}(-v_a)T_2 = 0 \tag{70a}$$

$$i_{bp3} + \frac{1}{L}\frac{(v_c - v_b)}{2}T_4 = 0 \tag{70b}$$

Where i_{ap1} and i_{bp3} can be derived using Eqns. (57), (60) and (64). Thus T_1 and T_2 can be derived from average current equations:

$$i_{aavg} = \frac{i_{ap1}\frac{T_1}{2} + (i_{ap1} + i_{ap2})\frac{T_2}{2} + i_{ap2}\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} = k_1 v_a \tag{71a}$$

$$i_{bavg} = \frac{i_{bp1}\frac{T_1}{2} + (i_{bp1} + i_{bp2})\frac{T_2}{2} + (i_{bp2} + i_{bp3})\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} + \frac{i_{bp3}\frac{T_4}{2} - I_R(\frac{T_5 + T_6}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_b \tag{71b}$$

The switching times for a 1.2 kW, 400 V V_{dc}, 115 V_{inrms}, f_s~ 1MHz, L= 4 µH are shown in Fig. 3.27. The inductance is chosen to obtain the desired minimum switching frequency. Towards the end of the sector, T_3 touches 0, that is the point where the switching sequence transitions from a to b. I_r is set as -1 A, the same as in rectifier mode, however, later it is found that a very small negative current is required for full ZVS turn-on in inverter mode.

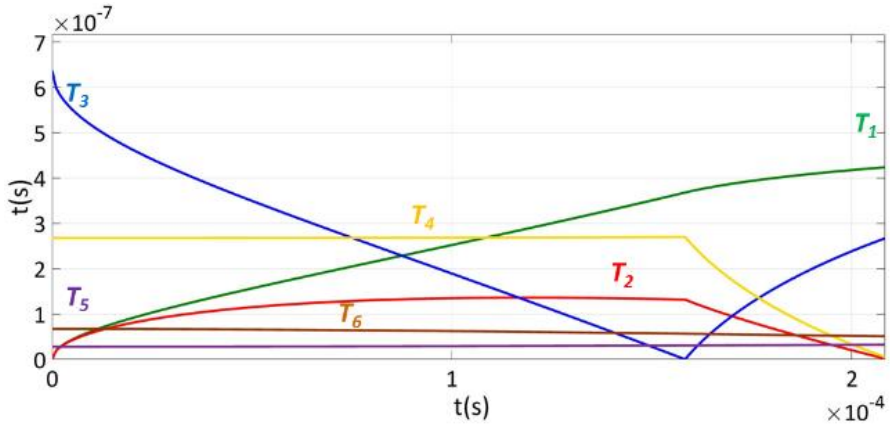


Figure 3. 27 Switching times for 1.2 KW P_o, 400 V V_{dc}, L~ 4 µH, 115 V V_{acrms}

The full line cycle control and the decision of DCM, TCM and Clamped mode of operation is the same as in rectifier mode form Fig. 3.14. The phase with the minimum absolute average current is in DCM, the phase with maximum absolute average current is clamped and the third one operates in TCM. The switching frequency variation from 0-60^{o} is shown in Fig. 3.28. The variation is symmetric after every 30^{o}.

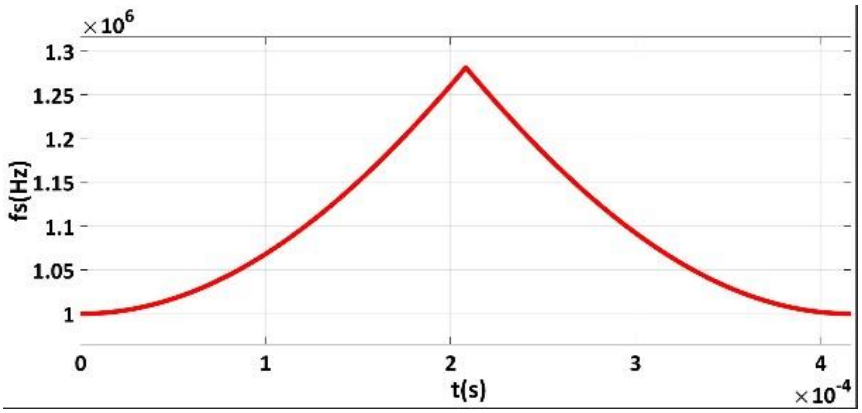


Figure 3. 28 Switching frequency variation for 1.2 KW P_o, 400 V V_{dc}, L~ 4 µH, 115 V V_{acrms}

3.2.3 Verification by Simulation

The converter is simulated from pre-calculated switching times (T_1, T_2, T_3, T_5 and T_6) and zero current detection (ZCD) of TCM phase. The simulated phase currents are shown in Fig. 3.29, ideal devices are considered in this simulation. The zoomed in waveforms in sector I are shown in Fig. 3.30. The estimated loss breakdown is similar to that of a rectifier a shown in Fig. 3.17 as the peak currents are very similar.

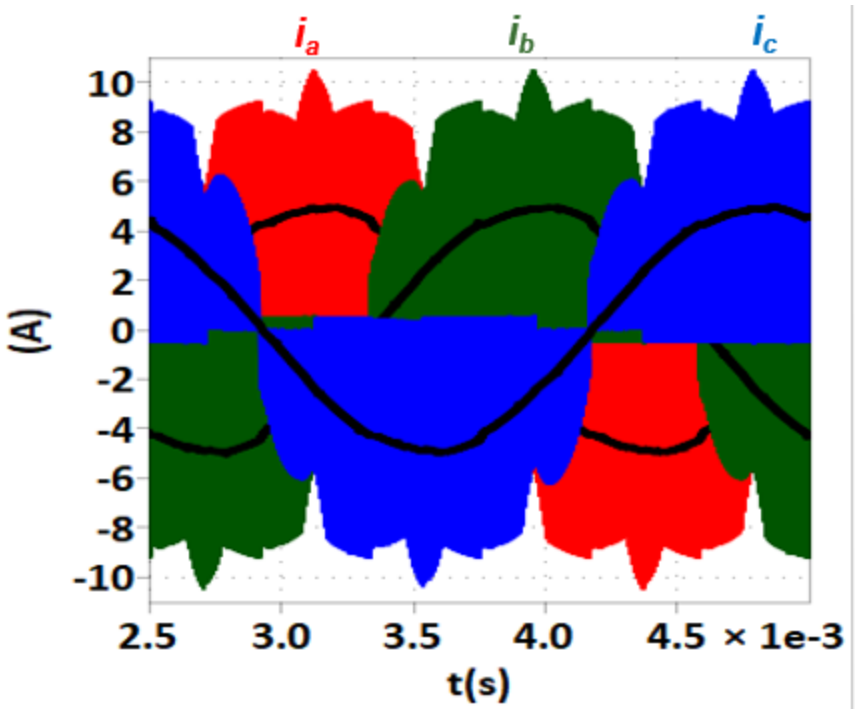
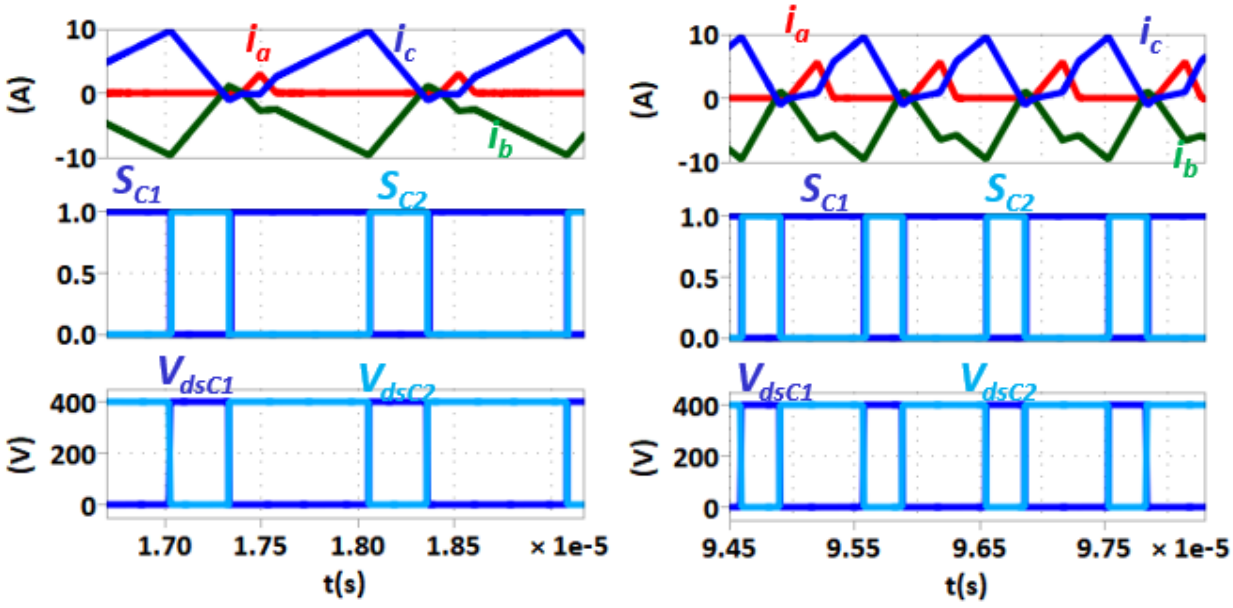
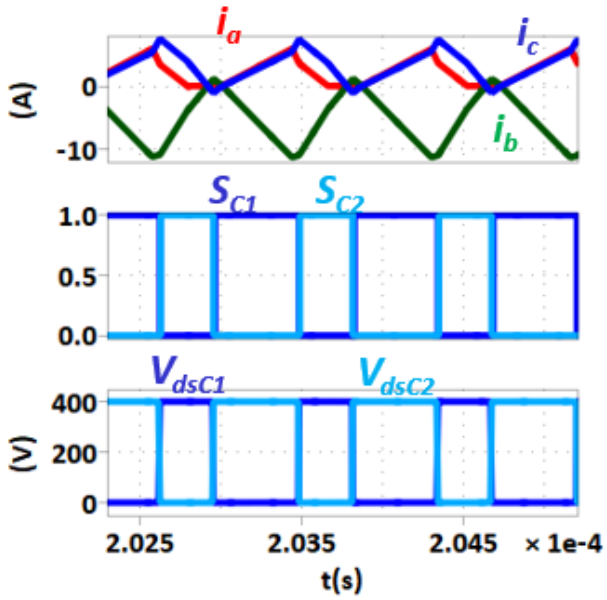


Figure 3. 29 Simulated phase currents for 1.2 KW P_o, 400 V V_{dc}, 115 V V_{inrms}, L~ 4 µH, inverter mode



(a) (b)

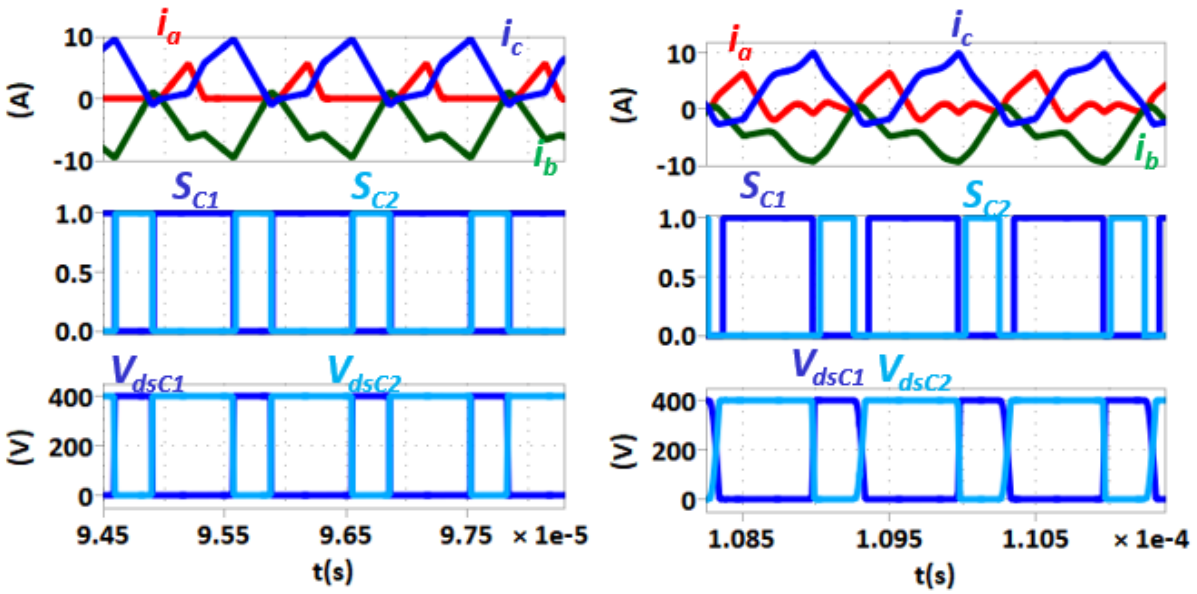


(c)

Figure 3. 30 Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector I

3.3 Control Implementation

The times shown above are calculated for ideal devices (neglecting the effect of C_{oss} and L resonance ripple on average current). This causes distortion in average current when the above switching times are used with device parasitics. The switching waveforms without and with C_{oss} are compared in Fig. 3.31. It can be seen that C_{oss} can cause significant ripple especially in DCM phase. This ripple affects the average currents such that the simulation becomes unstable in the middle of sector I. The model considering the effect of this ripple on average currents is very complex, hence to solve this issue, feedback control is required such that the average current follows the desired sinusoidal reference. Feedback controllers controlling average current can be used like in [B.42].



(a) (b)

Figure 3. 31 Phase currents i_a, i_b and i_c (a) with ideal devices and (b) considering C_{oss}

The closed loop implementation is shown in Fig. 3.32. The grid voltages' phase is measured with phase locked loop (PLL) and average sinusoidal currents are generated. Based on the relationship in Eq. 53, the controller assigns a mode of operation (DCM, TCM or clamped) to each phase. Also, if the phase with the maximum absolute value has positive current, it is clamped to P and if the current requirement is negative, the phase is clamped to N as shown in Fig. 3.32. Here, T_1 and T_3 denote the conduction times of S_{A1} and S_{C1} respectively in one switching cycle. Based on Eq. 53 and Fig. 3.33, the controller divides the i_a, i_b, i_c phase currents into i_{DCM}, i_{TCM} and i_{Cl} as shown in Fig. 3.34.

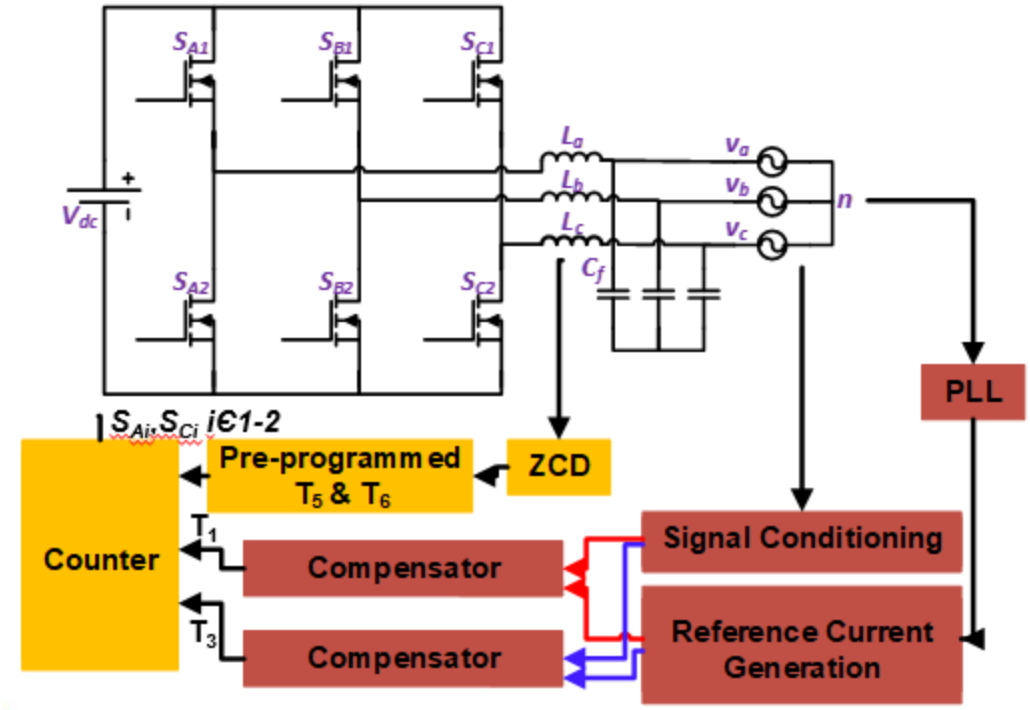


Figure 3. 32 Digital control block diagram for average current control from 0-30˚

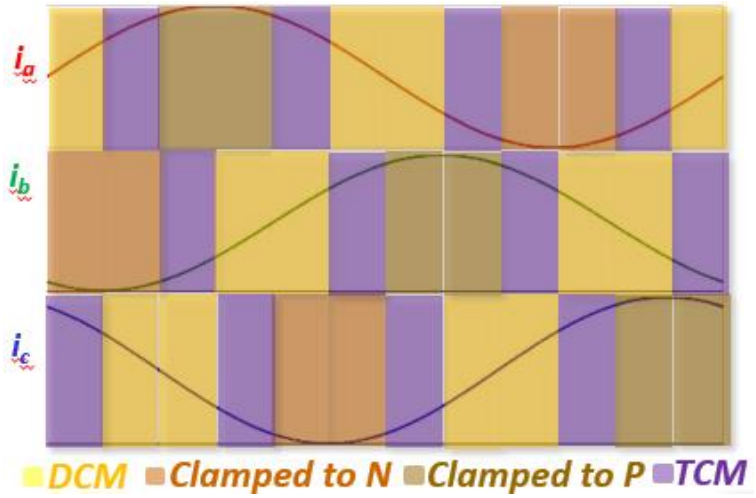


Figure 3. 33 Full line cycle operation showing assignment of DCM, TCM and Clamped mode of operation

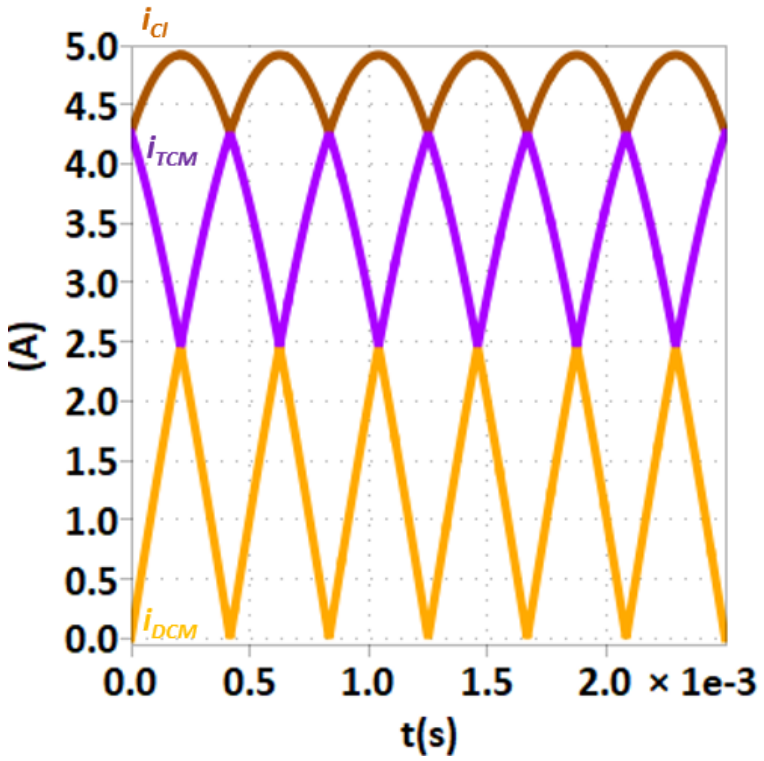


Figure 3. 34 Reference currents division into DCM, TCM and clamped operation

The controller block diagram shown in Fig. 3.32 shows phase A in DCM and phase C in TCM (sector I), however as discussed above due to symmetry, the same control block diagram is valid for the whole line cycle with just DCM and TCM phases changed depending on Eq. 53 and Fig. 3.33.

3.3.1 Verification by Simulation: Inverter Mode

As discussed above and from Fig. 3.32, the reference currents are generated from PLL, the average line frequency currents are measured by hall sensors as shown in Fig. 3.33. The hall sensor bandwidth is around 50 kHz such that it only measures the average current and filters all the high frequency noise. The error between the reference and measured currents at line frequency for DCM and TCM phases is input for the compensators. The compensators then generate the switching times T_1 and $T_1+T_2+T_3$ in the case of inverter as shown in Fig. 3.32.

The converter is simulated with the above implementation, the results are discussed below for different designs of compensators. The currents from the above implementation without

considering C_{oss} in the device model is shown in Fig. 3.35. The compensator is a PI controller with feedforward control. The bandwidth of DCM controller is higher than that of TCM controller, i.e. the DCM controller is faster than the TCM controller.

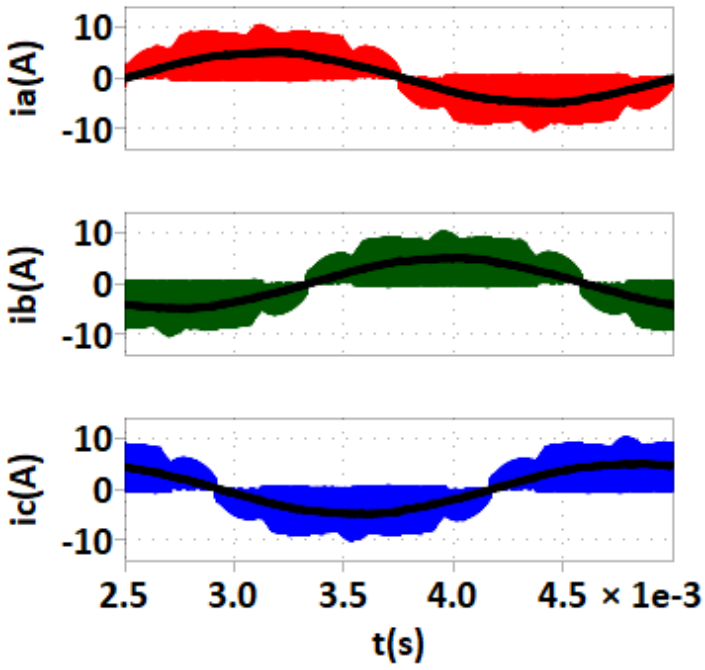


Figure 3. 35 Phase currents from proposed implementation with controller parameters:

$K_{pdcm}=1e^{-7}$, $K_{idcm}=1e^{-2}$, $K_{ptcm}=4e^{-8}$, $K_{itcm}=2e^{-2}$, $K_{ffdcm}=5e^{-9}$, $K_{fftcm}=5e^{-9}$

The simulated phase currents for the model considering C_{oss} are shown in Fig. 3.36 and the zoomed in waveforms are shown in Fig. 3.37. ZVS turn-on is achieved as shown in Fig. 3.37.

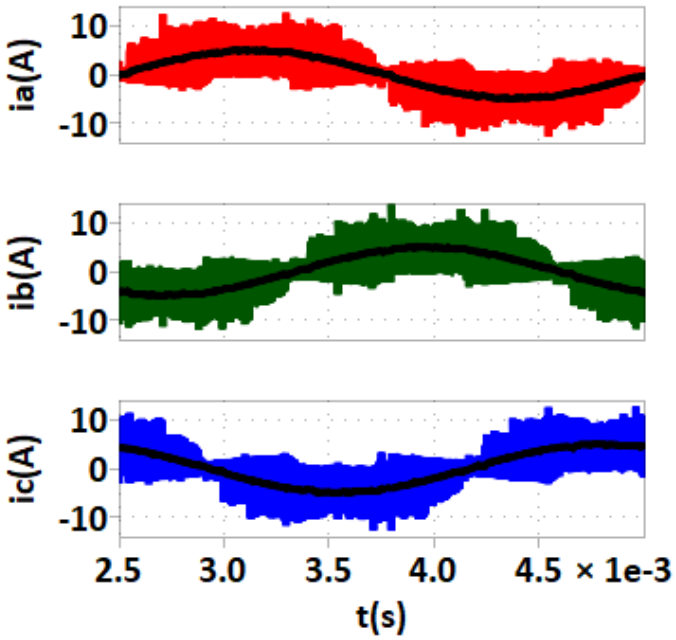
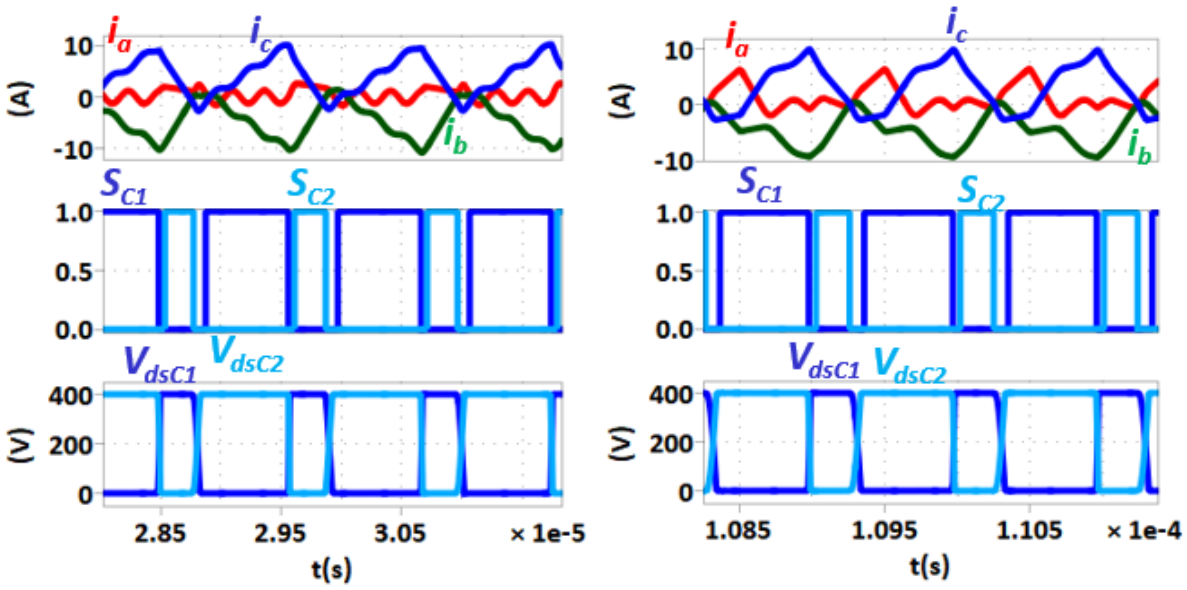
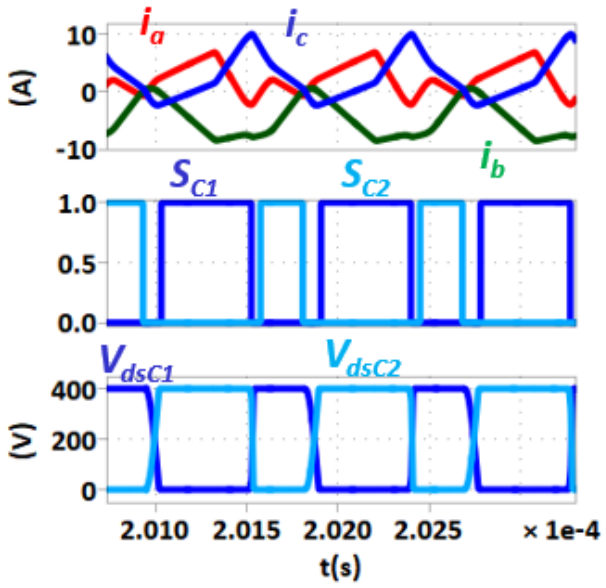


Figure 3. 36 Phase currents from proposed implementation (considering constant C_{oss}: 150 pF) with controller parameters: $K_{pdcm}=1e^{-7}$, $K_{idcm}= 5e^{-2}$, $K_{ptcm}= 3e^{-8}$, $K_{itcm}= 2e^{-2}$, $K_{ffdcm}=5e^{-11}$, $K_{fftcm}=1e^{-10}$



(a) (b)



(c)

Figure 3. 37 Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector I

3.3.2 Verification by Simulation: Rectifier Mode

The above implementation can also be employed for rectifier mode as shown in Fig. 3.38 with a low bandwidth (~5 Hz) output voltage controller which generates the magnitude of reference average currents.

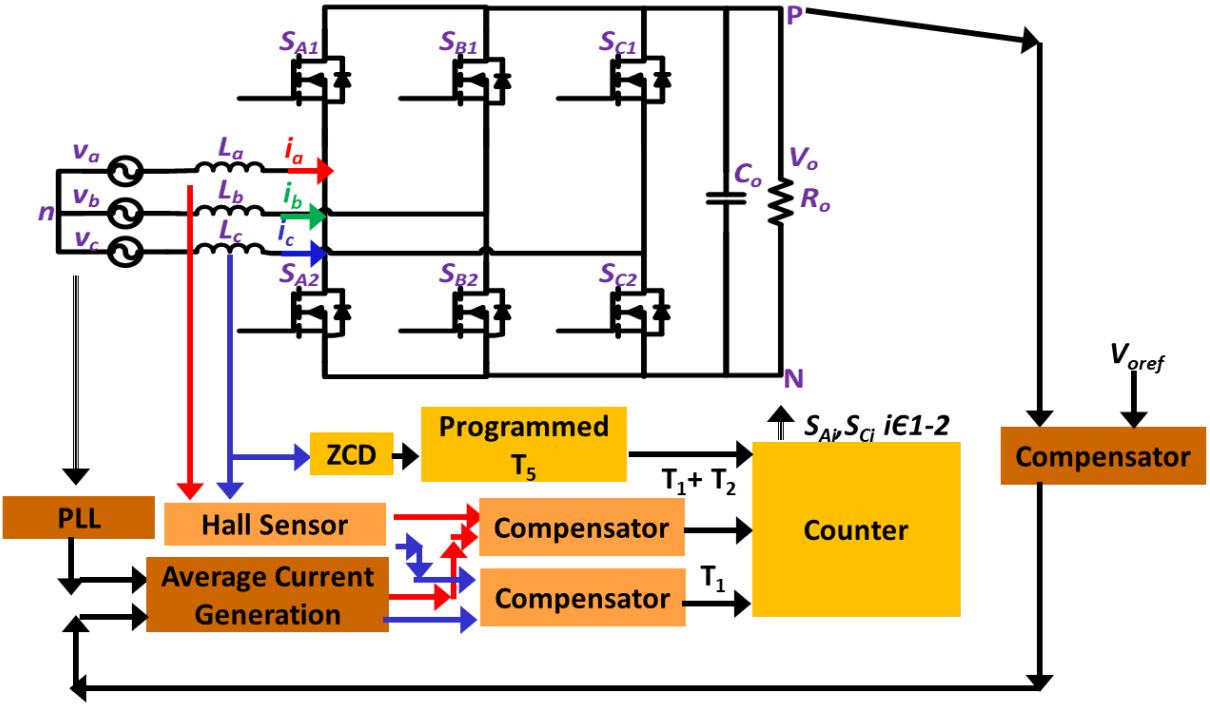
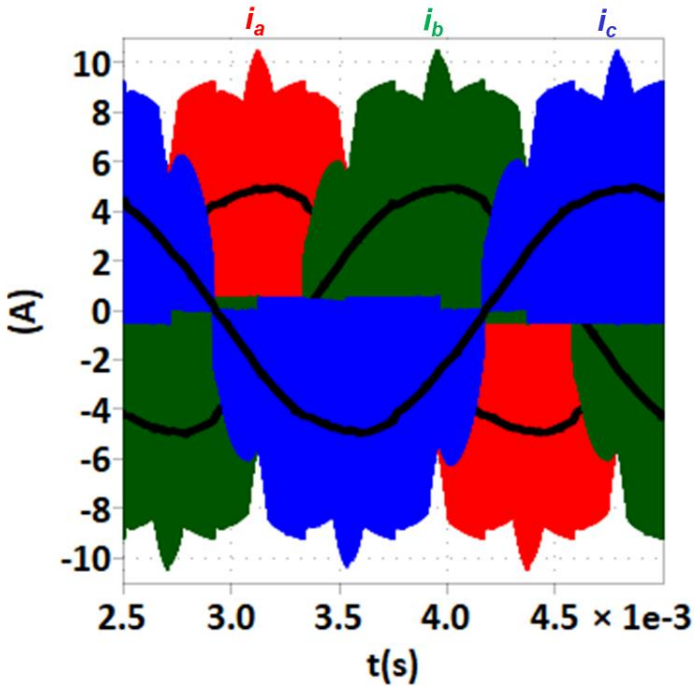
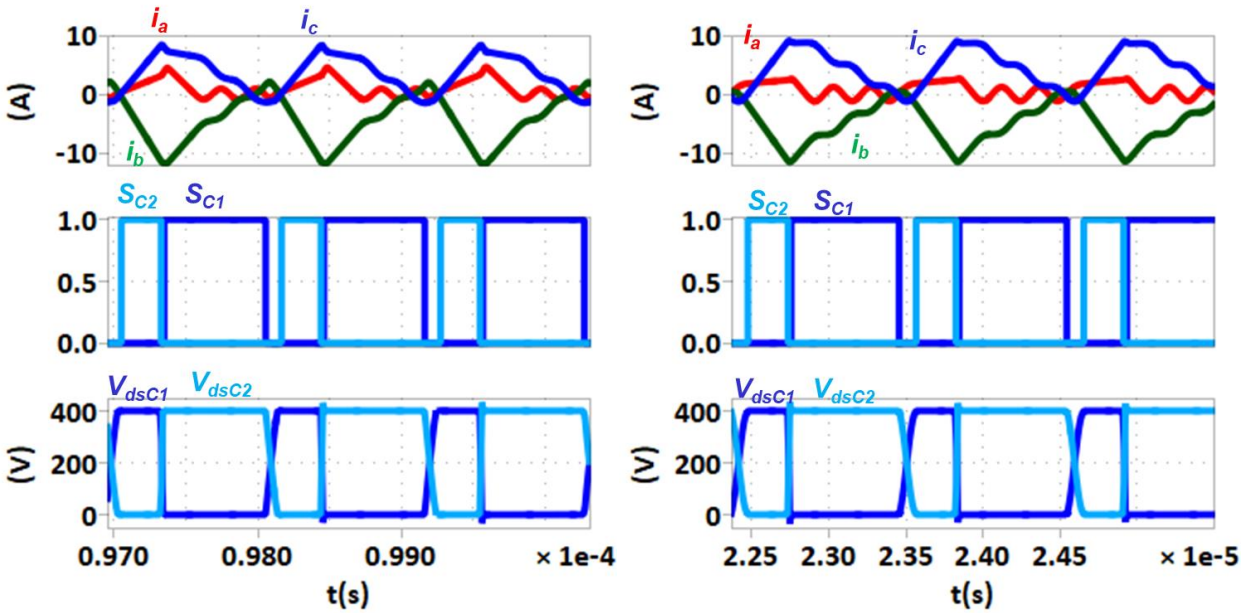


Figure 3. 38 Digital controller block diagram for rectifier mode from 0-30˚

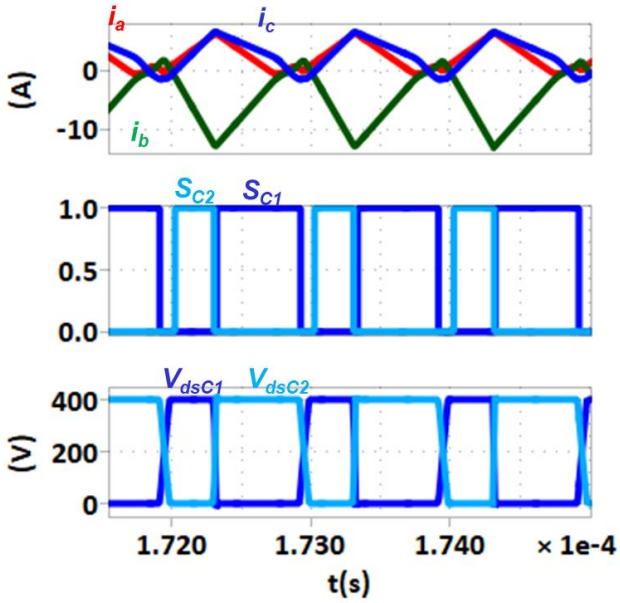
The above implementation is validated for rectifier mode, the simulation results are shown in Fig. 3.39(a). ZVS turn-on is shown in Figs. 3.39(b), (c) and (d).



(a)



(b) (c)



(d)

Figure 3. 39 (a) Phase currents from proposed implementation (b) Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in beginning (c) middle and (d) end of sector I

3.3.3 Implementation with DSP

A detailed controller architecture is shown in Fig. 3.40. According to the phase generated by PLL, the controller generates phase voltages and phase currents based on which it allocates a sector in which the 3-phase system is operating. This phase is updated in each ADC interrupt cycle. Based on the relative magnitude of phase currents, the controller segregates i_a, i_b, i_c to i_{DCM}, i_{TCM} and i_{Cl} based on the following equation:

$$|i_{Cl}| \geq |i_{TCM}| \geq |i_{DCM}| \tag{72}$$

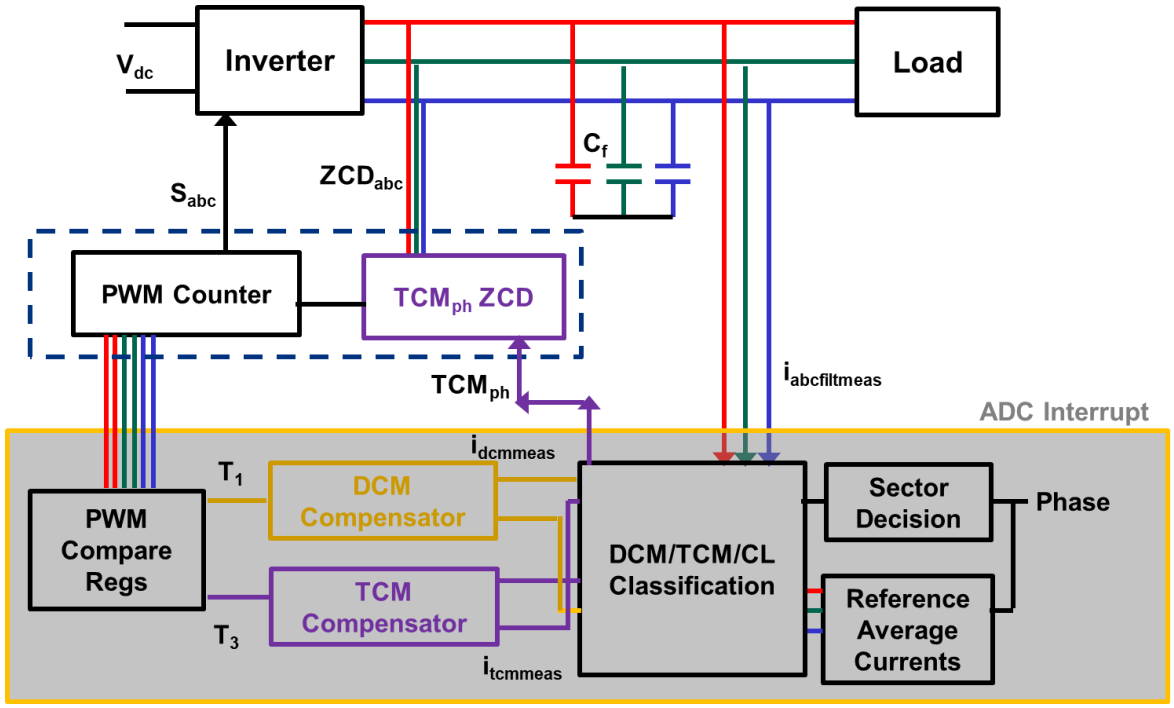


Figure 3. 40 Controller Architecture: Single core DSP implementation

The error between reference and measured currents is fed into the DCM and TCM compensators which generate switching times T_1 and T_3, T_1 and T_3 are fed to the PWM compare registers. These times are updated in every ADC interrupt cycle (16 µs) while the PWM counter is reset in synchronization with the ZCD signal. As discussed above, the ZCD signal is a variable frequency signal, hence to reset the counter at this variable frequency is a challenge which is discussed in the next section.

The biggest challenge is to generate variable frequency PWM signals, one method can be to reset the CPU counter of MCU which would make a dual core operation necessary for TCM. However, PWM modules in microcontrollers have a separate counter which is generally employed for PWM generation. Figure 3.41 shows that the PWM modules can be synchronized with an external signal (EPWMSYNCI). The counter (CTR) can be reset to a pre-programmed value TBPHS whenever the controller encounters a synchronization signal.

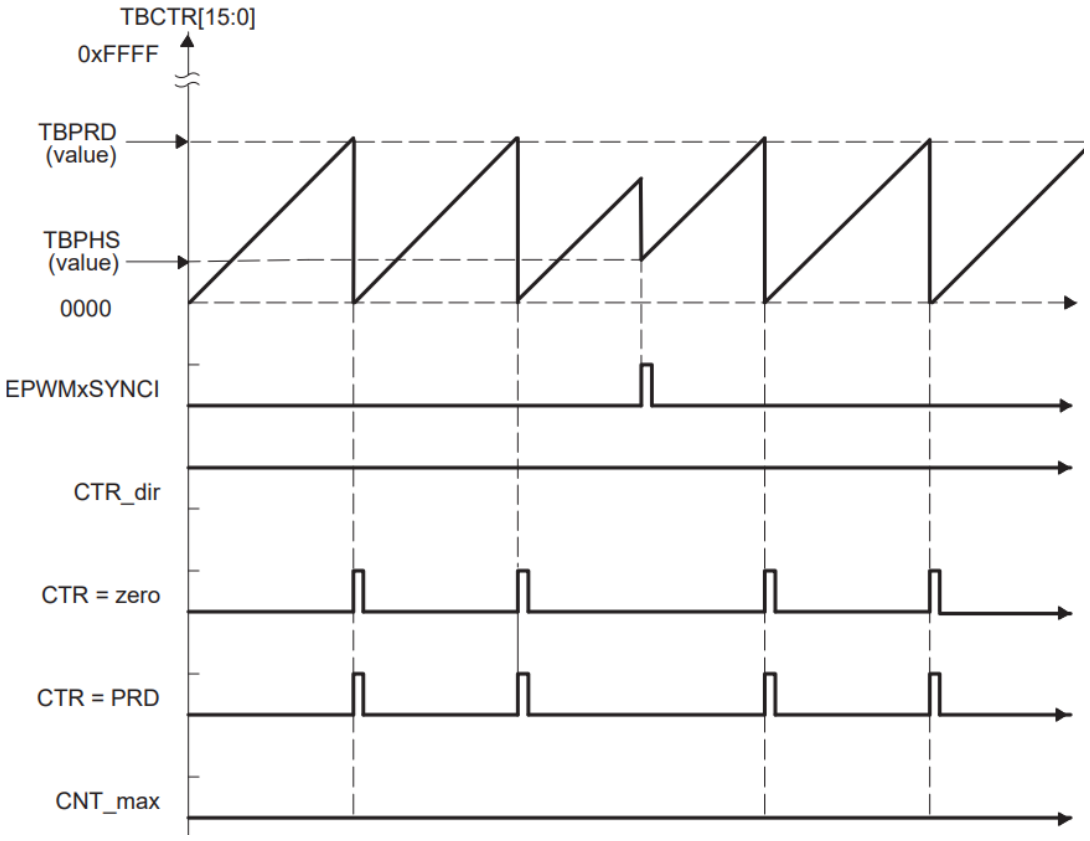


Figure 3. 41 PWM counter can be reset to a programmed value after the SYNCI signal goes high where TBPRD: PWM time period register value, TBPHS: PWM reset phase register value, EPWMSYNCI: External Synchronization Signal (ZCD_{TCM}) and CTR: PWM Counter

If the period of PWM signals (TBPRD) is programmed to be greater than the time period of external signal, a variable frequency PWM signal can be generated as shown in Fig. 3.42.

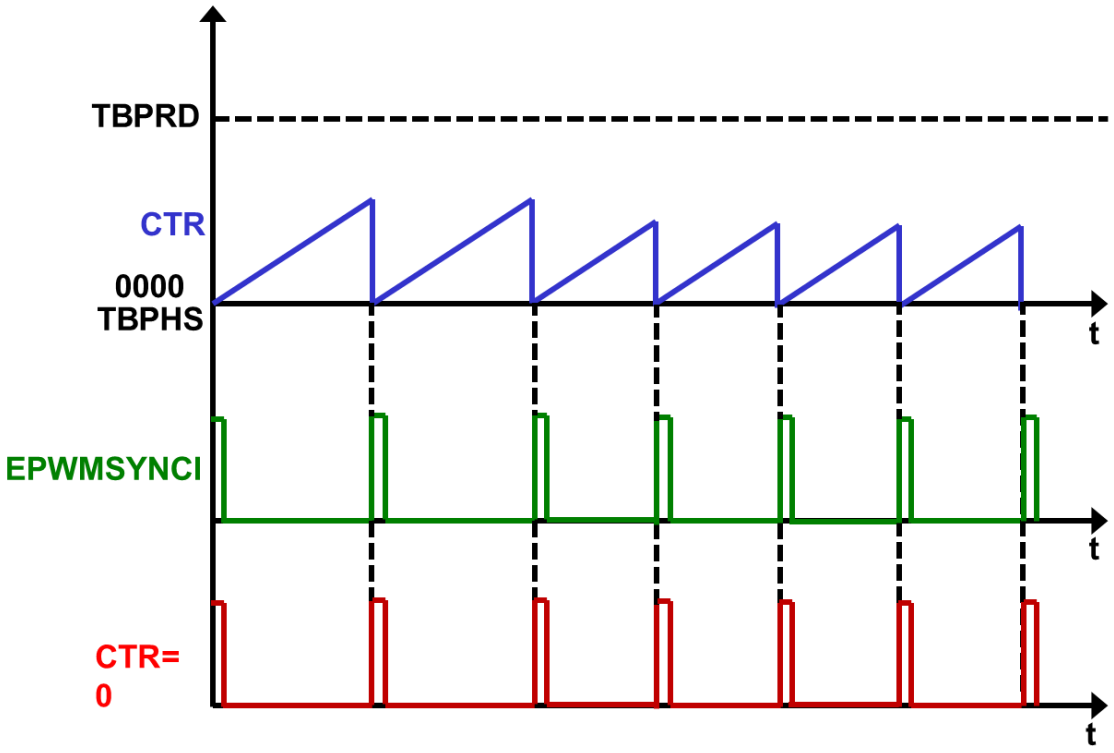


Figure 3. 42 Variable frequency PWM signals generated using EPWMSYNCI signal

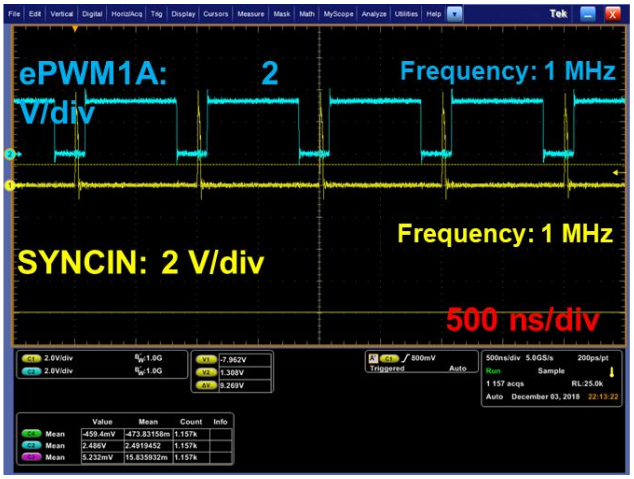
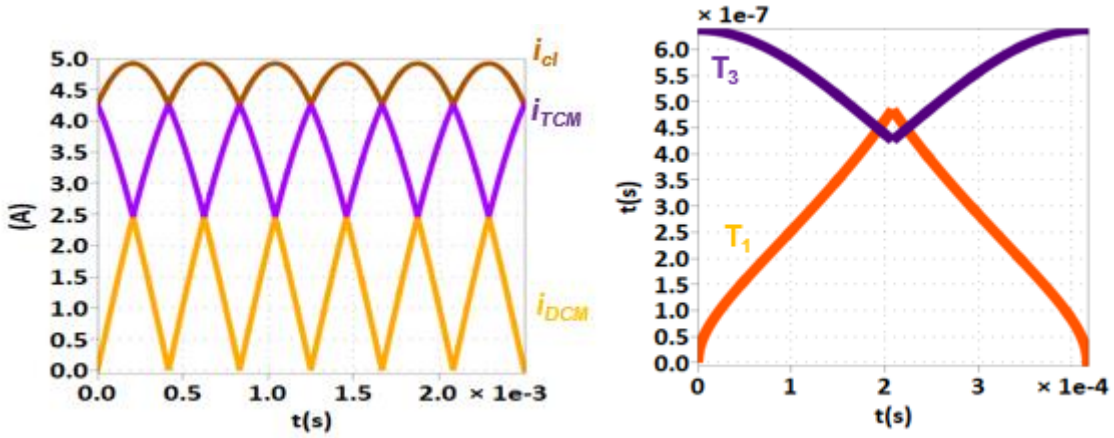


Figure 3. 43 PWM output synchronized with external signal

It can be seen from Fig. 3.43 that there is an 80 ns delay in the time which the external signal transitions from high to low and the PWM signal changes from low to high. The effect of this delay plus the delays caused by the hardware are discussed in the next section.

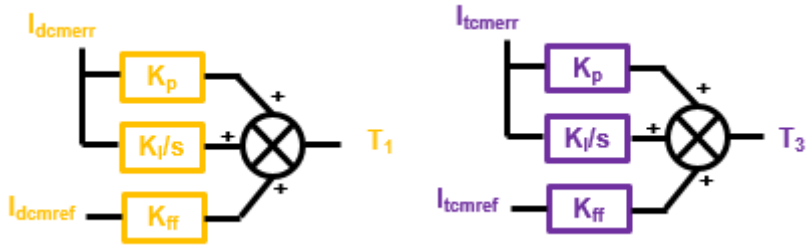
Another important aspect of the implementation is the compensator design and tuning. The compensator is a traditional PI + feedforward compensator a shown in Fig. 3.44. Fig. 3.45 shows

T_1 and T_{23} derived from the mathematical model right next to the DCM and TCM reference currents. The shape of T_1 and T_3 is similar to i_{DCM} and i_{TCM} respectively. Thus, it can be concluded that feedforward control will help in controlling the currents. Also, it can be seen that the rate of change in T_1 and i_{DCM} is greater than that of T_3 and i_{TCM}. Thus the bandwidth of DCM controller should be greater than the bandwidth of TCM controller. The values of PI and feedforward gains are shown in Table 3.1.



(a) (b)

Figure 3. 44 (a) DCM and TCM reference currents (b) T_1 and T_3 control times from mathematocal model.



(a) (b)

Figure 3. 45 (a) DCM and (b) TCM compenstaor

Parameter	DCM	TCM
K_p	$3*10^{-7}$	$2.25*10^{-8}$
K_i	0.00864	0.00253125
K_{ff}	$1*10^{-10}$	$1*10^{-10}$

Table 3. 1 Table showing compensator values

3.4 Experimental Verification

3.4.1 Hardware Setup

The above algorithm is tested on a three-phase two-level GaN converter (shown in Fig. 3.46) with 650 V/ 60 A GaN devices. The characterization and phase leg design with these devices is discussed is Appendix A. The top and bottom device are on opposite sides of the PCB making it an ultra-low inductance vertical power loop.

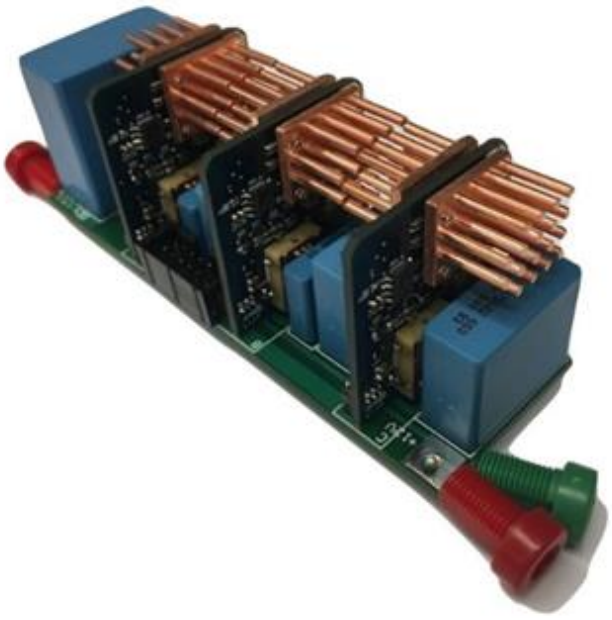


Figure 3. 46 Three-phase GaN converter with ultra-low inductance vertical power loop for 650 V/ 60 A GaN devices

The converter with filter inductors is shown in Fig. 3.47. The converter specifications are 400 V V_{dc}, 115 V V_{acrms}, 1.2 kW P_o and inductor is designed for 4 µH inductance such that the minimum switching frequency is 1 MHz.

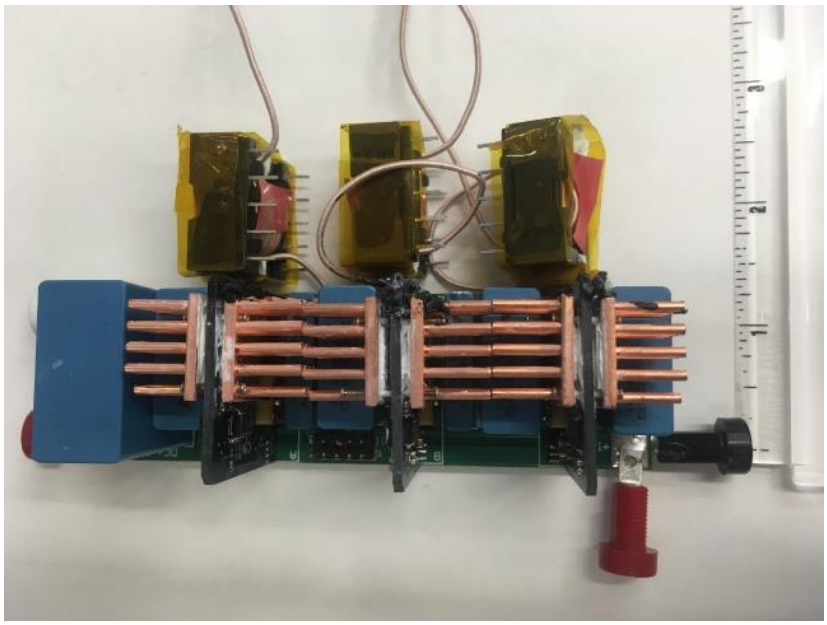


Figure 3. 47 GaN converter with filter inductors deigned to operate at ~1MHz switching frequency.

A crucial and the most important part of the control algorithm is the accurate zero crossing detection (ZCD) for instantaneous phase currents. The ZCD signal of the TCM phase triggers the start of a new switching cycle. This makes accurate zero crossing detection very important. In [B.23], ZCD is done by adding a small shunt resistor in series with the inductor as shown in Fig. 3.48. The voltage across this resistor is compared to zero with a comparator (as shown in Fig. 3.49), ZCD signal is triggered whenever this voltage changes sign. This reduces the complexity of sensing the high frequency instantaneous currents.

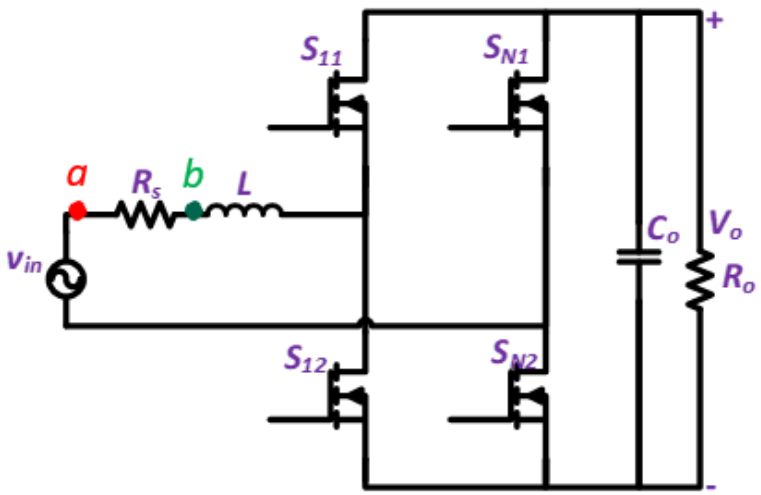


Figure 3. 48 Shunt Resistor in series with the inductor

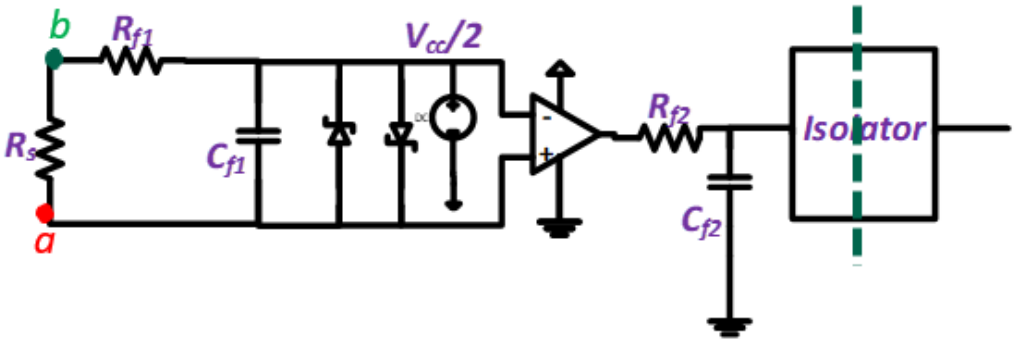


Figure 3. 49 Voltage across shunt resistor is compared to zero

The ZCD board schematic is shown in Fig. 3.50. The comparator output is fed into a digital isolator which is then transferred to the controller. The ZCD board is also very small as shown in Fig. 3.51. The ZCD board test results are shown in Fig. 3.52.

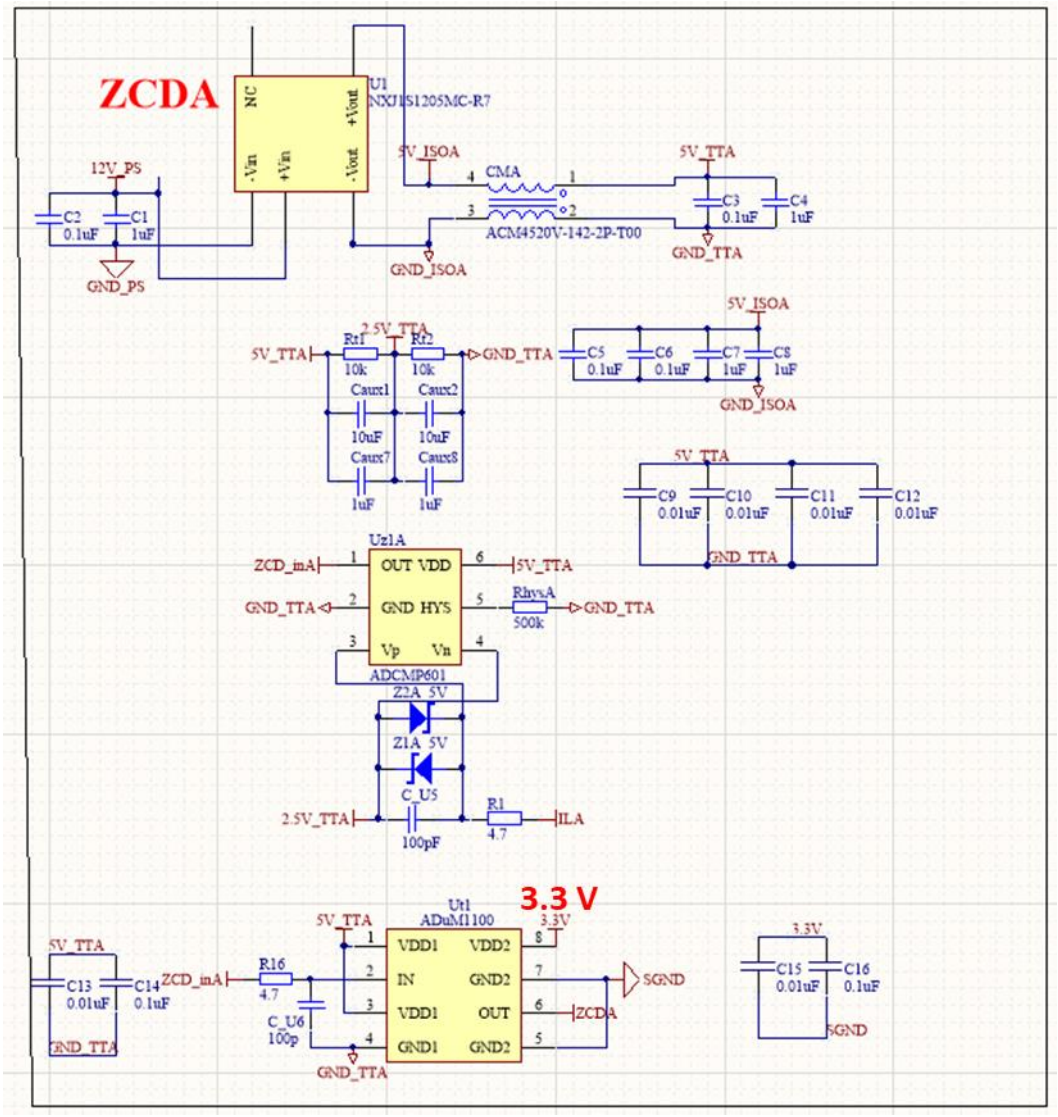
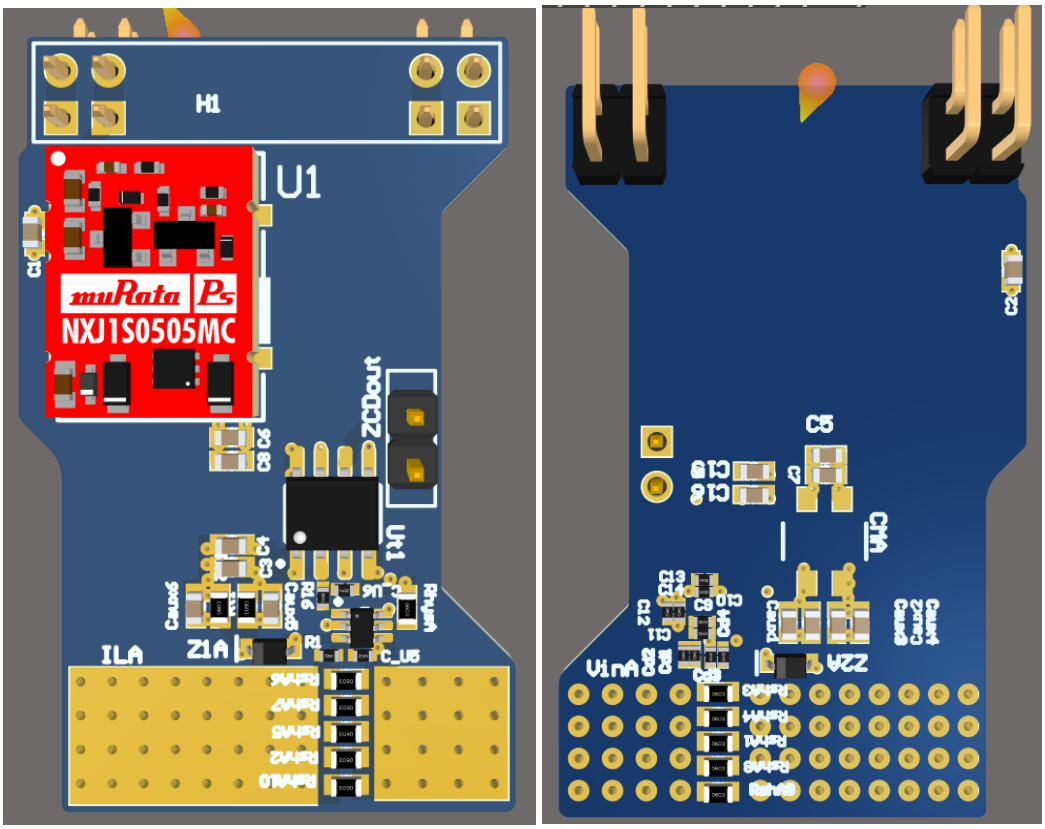


Figure 3. 50 ZCD circuit schematic



(a) (b)

Figure 3. 51 ZCD board (a) Top view and (b) Bottom view

Figure 3. 52 ZCD board testing results where V_{sh}: Voltage across shunt resistor

The filtered currents are sensed by connecting hall sensors in series with the load. The hardware setup is shown in Fig. 3.53.

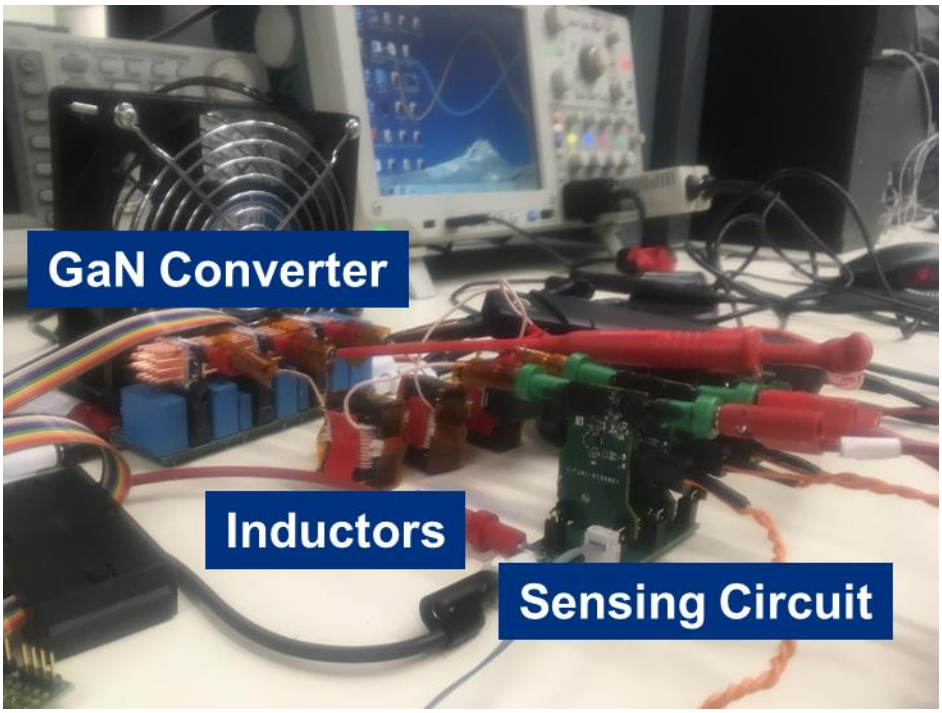


Figure 3. 53 Experimental setup showing GaN converter, inductors and sensing circuit.

3.4.2 Revised Algorithm

As shown above, the ZCD board is unable to detect exact 0 V crossing, it rather detects ±0.7 A crossing which along with hardware delays such as ZCD board to controller signal transfer delay, 80 ns controller input to output delay and PWM signal transfer delay leads to further drop of negative current as shown in Fig. 3.54. Thus the current drops to -2.8 A before S_{C2} is turned off.

Figure 3. 54 The delays in hardware, sensing circuit and controller leading to higher negative current than desired.

Hence to reduce this negative current the algorithm is revised as shown in Fig. 3.55. T_5 and T_6 are programmed to be 0, thus the switching sequence has four switching intervals now.

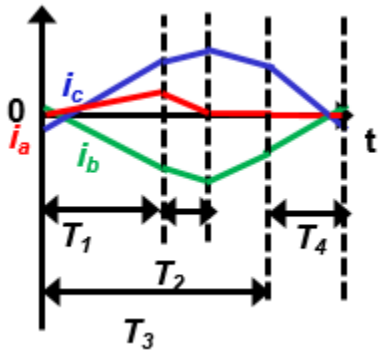


Figure 3. 55 Revised algorithm with T_5 and T_6= 0.

This causes a reduction in negative current, though it's still higher than desired. This high negative current also causes the switching ripple to go higher and switching frequency to drop. Thus, the EMI filter capacitor needs to be increased accordingly. The final values are discussed in the next section.

3.4.3 DCM Phase ZVS Turn-on

Negative current in TCM phase ensures ZVS turn-on of TCM phase, however DCM phase turn-on will still be hard switched if the algorithm is not designed for soft switching. The simulation results are shown for the same in Fig. 3.56. It is shown how the DCM phase does not turn on at 0 V if it's turned on immediately after the end of T_4, i.e. immediately after the ZCD of TCM phase.

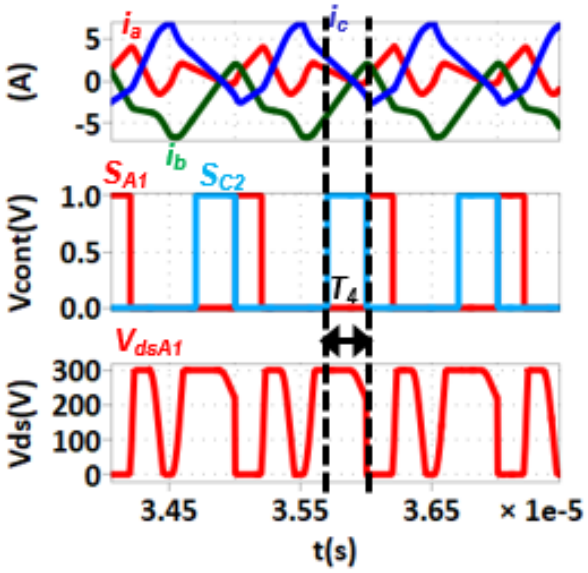


Figure 3. 56 DCM phase does not turn on at 0 V if S_{A1} is turned on immediately after turn-off of S_{C2}.

However, if the DCM phase is turned on with the TCM phase, i.e. S_{A1} is turned on with S_{C1} or after that, then the DCM phase can be turned on at 0 V as shown in Fig. 3.57.

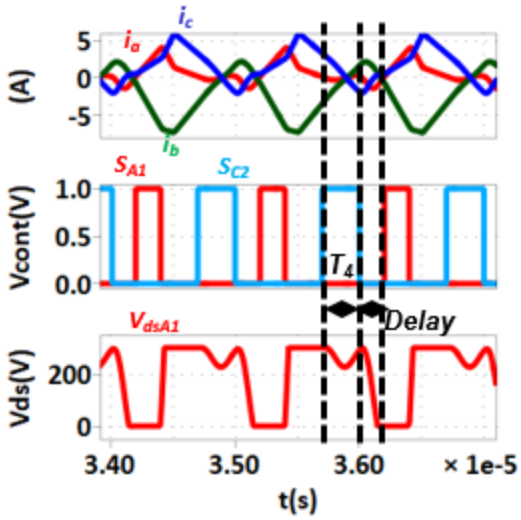


Figure 3. 57 DCM phase does is turned on at 0 V if S_{A1} is turned on after a delay after turn-off of S_{C2}.

3.4.4 Experimental Results

TCM and DCM phase ZVS turn-on is validated and shown in Fig. 3.58 and 3.59 respectively. The operating conditions are:

V_{dc}= 300 V

P_o= 675 W

V_{acrms}=86.25 V

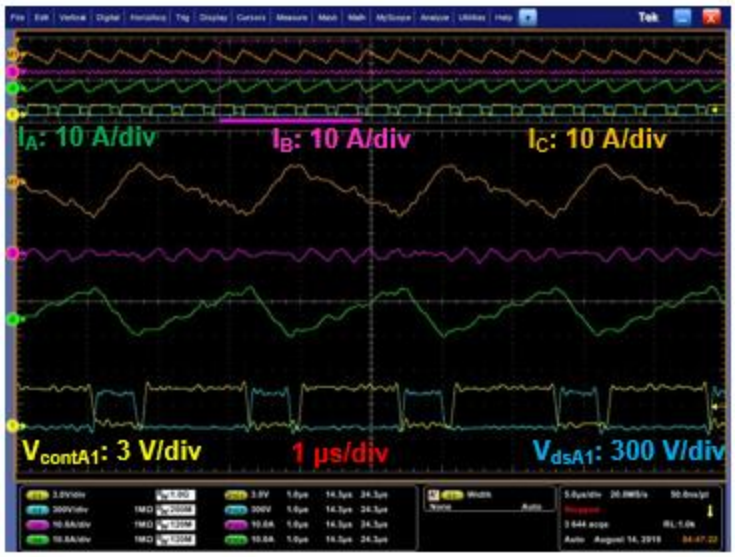


Figure 3. 58 Phase A operating in TCM mode, controller signal goes high after V_{dsA1} has reduced to 0 V.

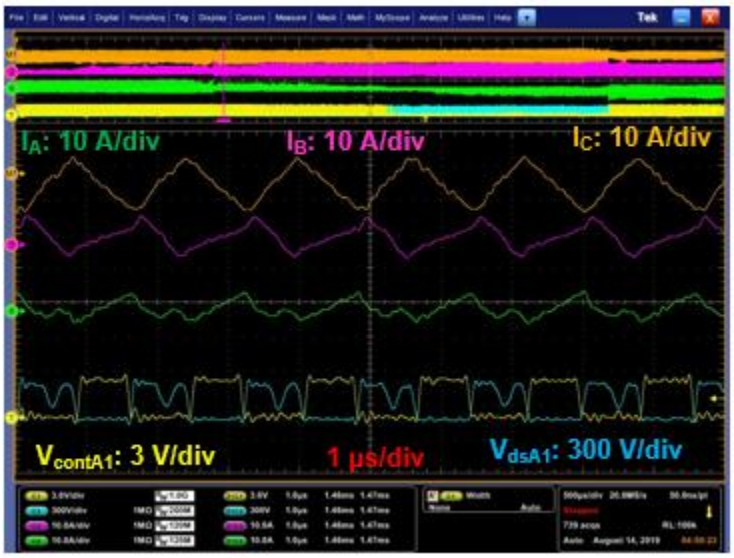


Figure 3. 59 Phase A operating in DCM mode, controller signal goes high after V_{dsA1} has reduced to 0 V.

Full line cycle currents are shown in Fig. 3.60. The measured system efficiency is 98.7 % at the above specified conditions. This result includes the inductor losses, ZCD shunt resistor losses and connector losses. Switching frequency range is 400- 530 kHz, this drop is owing to higher negative current issue. Filter capacitor had to be increased to 4 µF from 0.8 µF. The final density achieved

is 110 W/in^3 which can be improved by a more optimized assembly of the system. Measured filtered currents are shown in Fig. 3.61, the THD is 6.59 %.

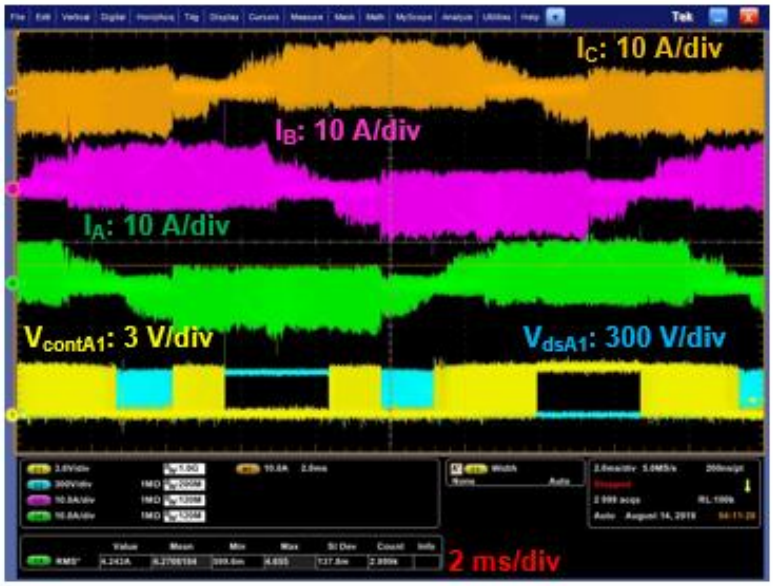


Figure 3. 60 Phase currents for V_{dc}= 300 V, P_o 675 W, V_{acrms}= 86.25 V.

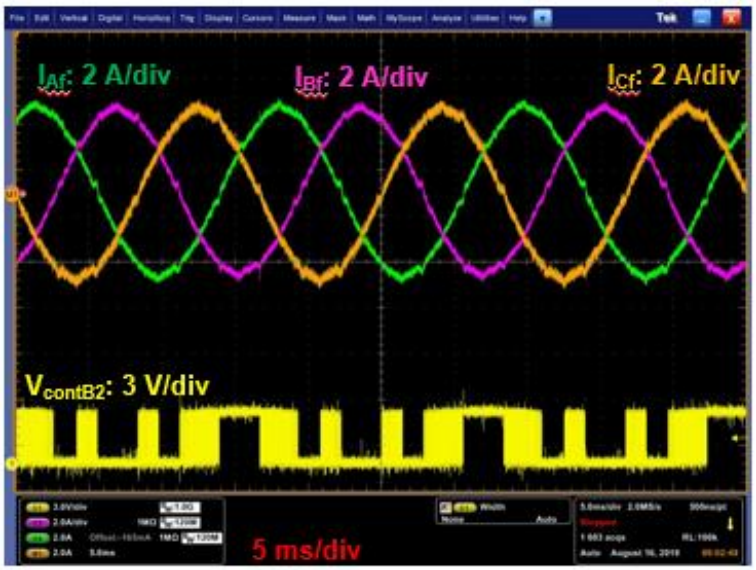


Figure 3. 61 Filtered phase currents, measured THD= 6.59 %

3.5 Summary

As shown above, TCM with phase synchronization is achieved by a combination of DCM+TCM+Clamped operation. The switching frequency variation is reduced to 34% as compared to more than 2* variation in state-of-the-art decoupled TCM. The key to achieving

sinusoidal currents is two independent switching times to control three phase currents. One of the challenges faced is calculation of switching times considering non-idealities which leads to implementation with average current control. However, high frequency ZCD is still important which indicates the start of a new switching cycle. The inability of ZCD circuit to detect close to 0 A and the hardware delays lead to a revision in algorithm with no pre-programmed negative current.

The challenges faced from implementation standpoint are synchronizing the microcontroller with a variable frequency ZCD signal without halting all the operations of the MCU. In the proposed implementation, DSP PWM module is employed like in common power converter control techniques. Thus, a single CPU implementation is shown in this chapter.

The discussion in previous literature is limited to only TCM ZVS turn-on, however in this chapter, it was discussed how DCM phase can also be turned on at 0 V by adjusting the timing of the turn-on. Thus, all the three phases turn on at 0 V reducing the losses and CM noise. The final system efficiency measured is 98.7 % at 300 V DC voltage, 0.7 kW and 400-530 kHz switching frequency. The power density achieved is 110 W/in^3.

However, the above discussion was only limited to unity power factor which is not sufficient for commercial applications. Reactive power control is also desired for commercial three-phase converters which is discussed in the next chapter.

Chapter 4. TCM for Three-Phase Two-Level Converters: Reactive Power Control

The state-of-the-art CRM/TCM control is limited to unity power factor mode of operation. However, for commercial applications, unity power factor operation is not guaranteed. There can be reactive power requirement from the grid in case of inverter (as shown in Fig. 4.1) or the EMI filter can also introduce a phase lag between ac voltages and boost inductor currents for both rectifier (as shown in Fig. 4.2) and inverter, hence TCM control needs to be extended to operation when reactive power is consumed/ delivered.

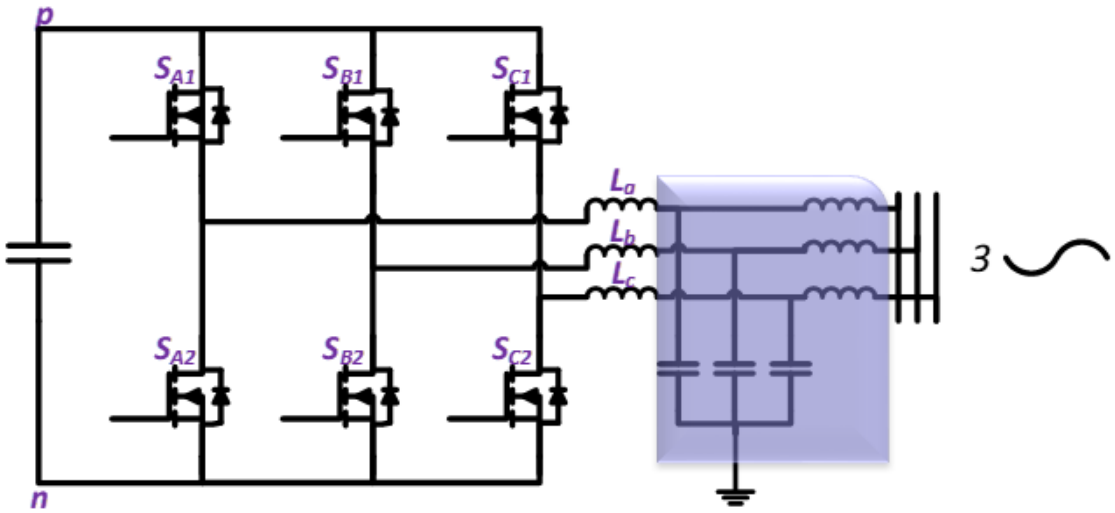


Figure 4. 1 Reactive power requirement from the grid and the EMI filter causing a phase lag between boost inductor currents and AC voltages.

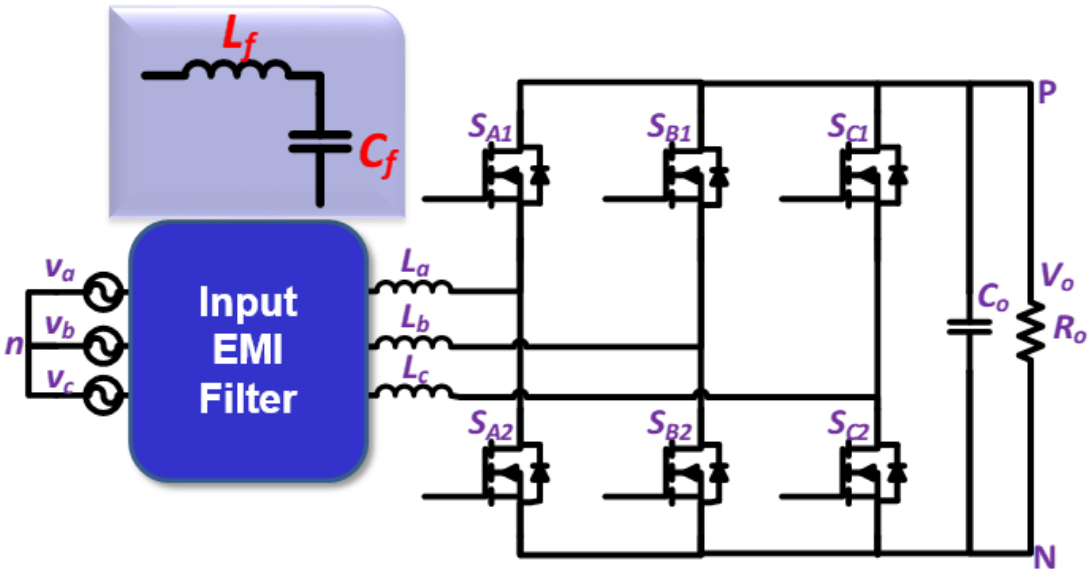


Figure 4. 2 Phase lag introduced by EMI filter between boost inductor currents and AC voltages

4.1 Theory

As discussed in chapter 3, in the case of unity power factor operation, the average phase currents can be expressed as directly proportional to respective phase voltages. For active +reactive power or purely reactive power generation, the average phase current phasor can be expressed as the vector addiction of two voltage phasors as shown in Fig. 4.3(b). The average currents are given by:

$$i_a = I_m \sin(\omega t - \phi) = k_1 v_a + k_2 v_b \tag{73a}$$

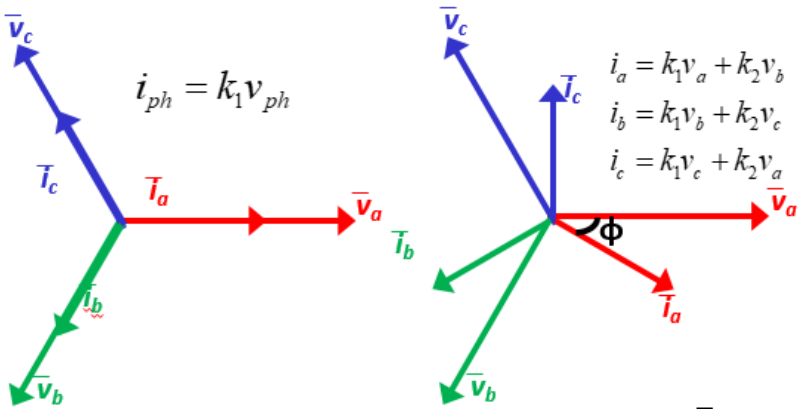
$$i_b = I_m \sin(\omega t - 2\pi/3 - \phi) = k_1 v_b + k_2 v_c \tag{73b}$$

$$i_c = I_m \sin(\omega t + 2\pi/3 - \phi) = k_1 v_c + k_2 v_a \tag{73c}$$

where

$$k_1 = (\cos\phi + \sin\phi/\sqrt{3}) I_m / V_m \tag{74a}$$

$$k_2 = (2\sin\phi/\sqrt{3}) I_m / V_m \tag{74b}$$



(a) (b)

Figure 4. 3 Average currents (a) directly proportional to phase voltages for unity power factor case (b) expressed as sum of two phase voltages for active + reactive power generation

The above mathematical expression is physically equivalent to pulling the current from two voltage sources instead of just one as there can be a non-zero current requirement when the corresponding phase voltage is zero and vice versa. This phenomenon can be clearly seen when the voltages and currents are viewed on the time axis a shown in Fig. 4.4.

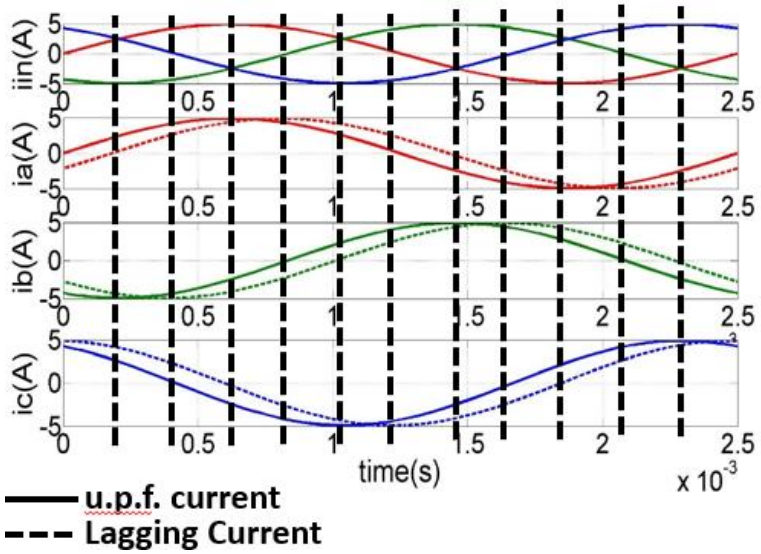


Figure 4. 4 Average currents for unity power factor and current with a phase lag

4.2 Active + Reactive Power

Similar to unity power facto operation, the phases still operate in DCM, TCM and clamped mode. Usually in standard SVM, the phase with maximum magnitude of current is clamped as

was done in the case of unity power factor in previous chapter. For example, in the case of 30° lagging power factor shown in Fig. 4.5, phase C has maximum magnitude of current in Sector I. If phase C is clamped to P and phase A is in DCM as it has minimum magnitude of current.

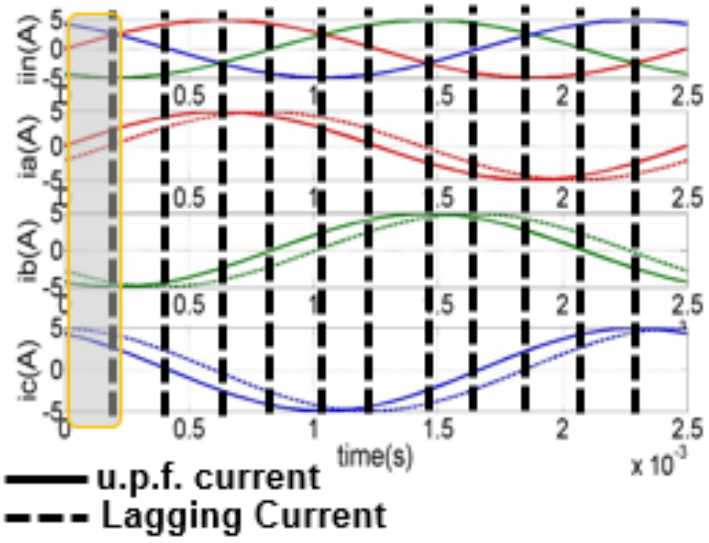


Figure 4. 5 Reference currents for unity power factor and 30° lagging power factor

The simulated currents when phase C is clamped to P, phase A is in DCM and phase B is in TCM are shown in Fig. 4.6. It can be seen that the body diode of S_{A2} starts to conduct current in the positive direction when phase A is programmed to be off. This current ripple is undesirable and cannot be compensated by the controller as shown in Fig. 4.6.

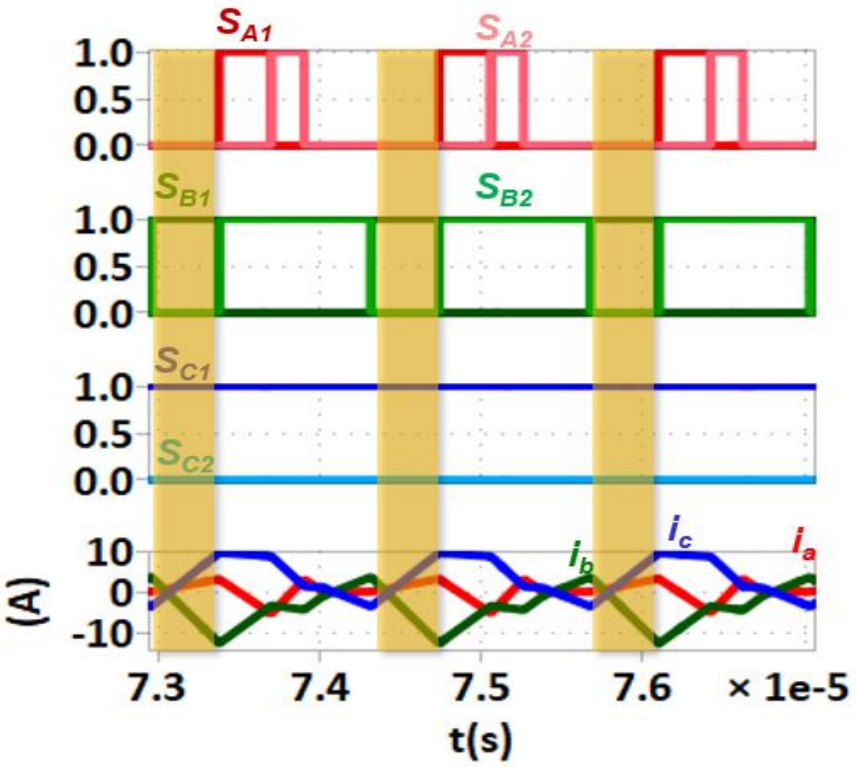


Figure 4. 6 Phase A current increasing in positive direction as body diode of S_{A2} becomes forward biased

Thus, phase with maximum voltage is clamped. Hence the phase shift for which this algorithm gives significant improvement as compared to CCM is -30º-30º as beyond 30º, when phase with maximum absolute voltage will be clamped, it will also be the phase with minimum current magnitude and the higher current phases will be switching. This is discussed in detail in section 4.5.

4.2.1 Optimal Range of Phase Shift: -30º-30º

The average currents for 30° phase lag are shown in Fig. 4.7. It can be seen that the challenge is to generate average currents that are not directly proportional to input voltages thus generating zero average current when the voltage is not zero and vice versa. Also, when there is a phase lag, it is possible that the currents and voltages do not have full circular symmetry as the voltages are symmetric about one phase angle and the currents are symmetric about a different phase angle. It can be seen in Fig. 4.7 that for 30° lag, currents and voltages are not symmetric after every 30° but

the three phase symmetry still holds after every 60°. Hence, two sectors' operation are discussed in detail for this case.

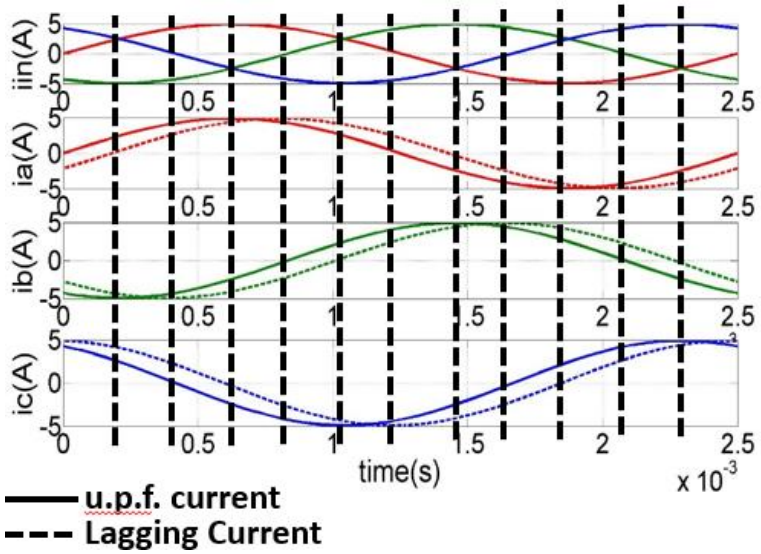


Figure 4. 7 Average currents for unity power factor and 30° lagging cases

4.2.2 Mathematical Model

Sector I (0<ωt<π/6)

Each switching cycle can be divided into 6 switching intervals (the dead times are not included as operation during dead time is very similar to unity power factor case) as shown in Fig. 4.8. The gating signals are also included to show the switching sequence. As can be seen in Fig. 4.7, average phase A current (i_{aavg}) is negative, hence i_a ripple should be negative as opposed to unity power factor, also A phase (phase in DCM) is only allowed to conduct for two switching intervals as in the end of sector I, average i_a is zero with positive phase voltage, hence times T_2 and T_3 should be zero at end of sector I, the detailed operation is discussed below.

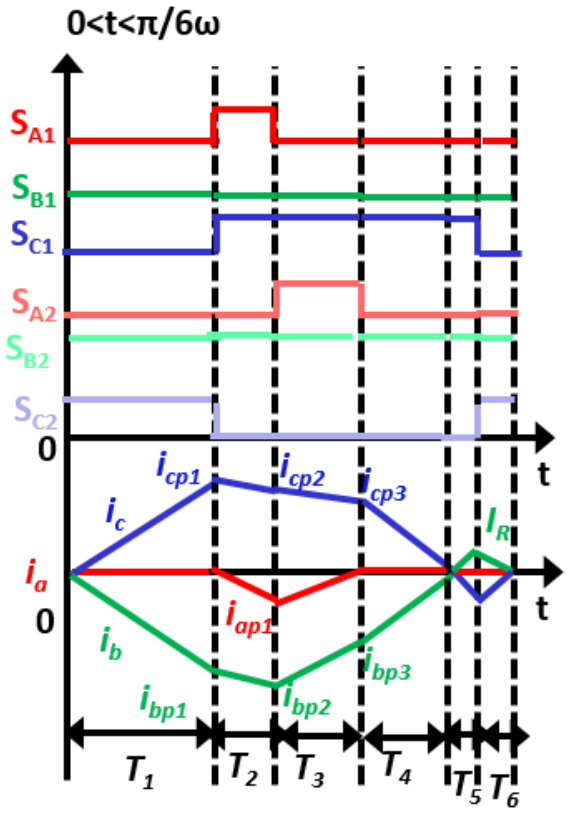


Figure 4. 8 One switching cycle waveform for 30° phase lag in sector I

Interval I (0-T_1)

During interval 1, S_{B2} and S_{C2} conduct, i_c increases proportional to phase voltage. The equivalent circuit is shown in Fig. 4.9, the phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (v_b - v_c) / 2L \tag{75}$$

The peak currents are given by:

$$i_{bp1} = -i_{cp1} = \frac{(v_b - v_c)}{2L} T_1 \tag{76}$$

After i_c reaches i_{cp1}, S_{C2} is turned off as shown in Fig. 4.8.

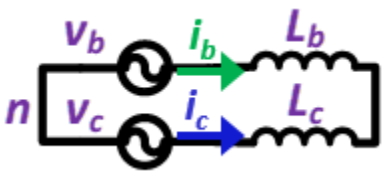


Figure 4. 9 Equivalent circuit in Interval I

Interval II (T_1-T_1+T_2)

After S_{C2} is turned off, the voltage across S_{C1} drops to zero due to resonance between devices' capacitors and inductor L_c, hence S_{C1} is turned on at 0 V. S_{A1} is also turned on and i_a begins to fall. The equivalent circuit is shown in Fig. 4.10. The phase currents' slopes are given by:

$$di_a / dt = (v_a - V_o / 3) / L \tag{77a}$$

$$di_b / dt = (v_b + 2V_o / 3) / L \tag{77b}$$

$$di_c / dt = (v_c - V_o / 3) / L \tag{77c}$$

The peak currents are given by:

$$i_{ap2} = \frac{1}{L}(v_a - V_o / 3)T_2 \tag{78a}$$

$$i_{bp2} = i_{bp1} + \frac{1}{L}(v_b + 2V_o / 3)T_2 \tag{78b}$$

$$i_{cp2} = i_{cp1} + \frac{1}{L}(v_c - V_o / 3)T_2 \tag{78c}$$

After i_a reaches i_{ap2}, S_{A1} is turned off as shown in Fig. 4.8.

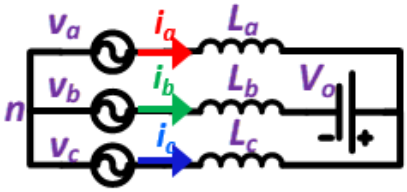


Figure 4. 10 Equivalent circuit in Interval II

Interval III (T_1+ T_2 - T_1+ T_2+ T_3)

After S_{A1} is turned off, the voltage across S_{A2} drops to zero due to resonance between devices' capacitors and inductor L_a, hence S_{A2} is turned on at 0 V. At the beginning of interval III, S_{A2} is turned on. Thus i_a starts to rise, the equivalent circuit is shown in Fig. 4.11, the phase currents' slopes are given by:

$$di_a / dt = (v_a + V_o / 3) / L \tag{79a}$$

$$di_b / dt = (v_b + V_o / 3) / L \tag{79b}$$

$$di_c / dt = (v_c - 2V_o / 3) / L \tag{79c}$$

The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{1}{L}(v_b + V_o / 3)T_3 \tag{80a}$$

$$i_{cp3} = i_{cp2} + \frac{1}{L}(v_c - 2V_o / 3)T_3 \tag{80b}$$

This interval ends when i_a reaches zero, S_{A2} is turned off at the end of *Interval* III.

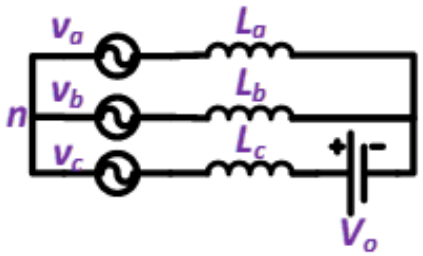


Figure 4. 11 Equivalent circuit in Interval III

Interval IV (T_1+ T_2+ T_3- T_1+ T_2+ T_3+T_4)

In this mode, S_{B2} and S_{C1} conduct, the equivalent circuit is shown in Fig. 4.12. The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (V_o + v_b - v_c) / 2L \tag{81}$$

Thus i_c falls to zero during this interval, this interval ends when i_c reaches zero.

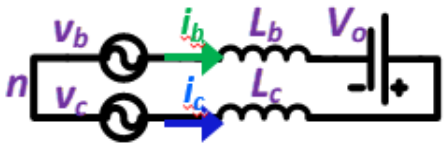


Figure 4. 12 Equivalent circuit in Interval IV

Interval V (T_1+ T_2+ T_3+T_4- T_1+ T_2+ T_3+T_4+T_5)

After i_c reaches 0, S_{C1} is allowed to conduct for a little more time till i_c reaches a negative value I_R. The equivalent circuit is the same as in Interval IV. At the end of this interval, S_{C1} is turned off. The peak negative current I_R is given by:

$$I_R = -\frac{(V_o + v_b - v_c)T_5}{2L} \tag{82}$$

Interval VI (T_1+ T_2+ T_3+T_4+T_5 - T_1+ T_2+ T_3+ T_4+T_5+ T_6)

After S_{C1} is turned off, resonance occurs in between devices' output source capacitors and inductors. Thus V_{dsC1} reaches V_o and V_{dsC2} reaches 0, S_{C2} is turned on (as shown in Fig. 4.8), the equivalent circuit is shown in Fig. 4.13. The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (v_b - v_c) / 2L \tag{83}$$

The peak negative current I_R is given by:

$$I_R = \frac{(v_b - v_c)T_6}{2L} \tag{84}$$

Thus, i_c starts to increase again and this interval ends when i_c and i_b recah zero again and a new switching cycle starts from here.

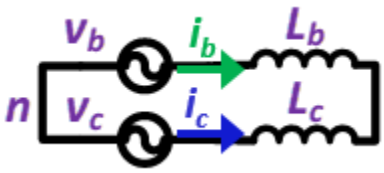


Figure 4. 13 Equivalent circuit in Interval VI

Thus, negative ripple is achieved in phase A when the phase voltage is positive and ZVS turn-on is achieved by a combination of DCM, TCM and Clamped mode of operation.

Sector II ($\pi/6<\omega t<\pi/3$)

From Fig. 4.7, it can be seen that phase currents and voltages are in the same direction now. While the magnitude of phase A average current is minimum, the corresponding phase voltage is

much higher posing a challenge for the choice of switching states. The switching waveform for one switching cycle is shown in Fig. 4.14.

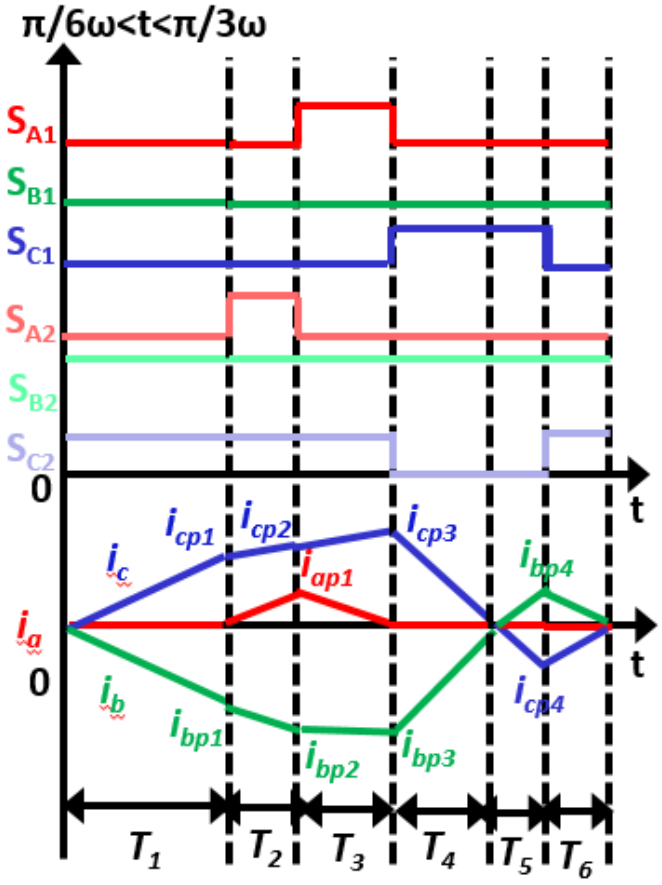


Figure 4. 14 One switching cycle waveform for 30° phase lag in sector II

Interval I (0-T_1)

During interval 1, S_{B2} and S_{C1} conduct, i_c increases proportional to phase voltage. The equivalent circuit is the same as in interval I of sector I (as shown in Fig. 4.9), the phase currents' slopes are given by Eq. 75. The peak currents are given by Eq. 76. After i_c reaches i_{cp1}, S_{A2} is turned on as shown in Fig. 4.14.

Interval II (T_1-T_1+T_2)

After S_{A2} is turned on, i_a begins to rise. The equivalent circuit is shown in Fig. 4.15. The phase currents' slopes are given by:

$$di_a / dt = v_a / L \tag{85a}$$

$$di_b / dt = v_b / L \tag{85b}$$

$$di_c / dt = v_c / L \tag{85c}$$

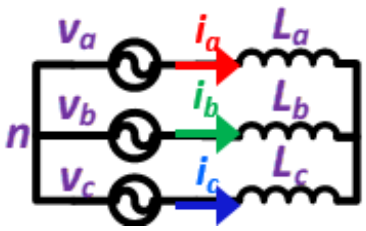


Figure 4. 15 Equivalent circuit in Interval II

The peak currents are given by:

$$i_{ap2} = \frac{v_a}{L} T_2 \tag{86a}$$

$$i_{bp2} = i_{bp1} + \frac{v_a}{L} T_2 \tag{86b}$$

$$i_{cp2} = i_{cp1} + \frac{v_c}{L} T_2 \tag{86c}$$

After i_a reaches i_{ap1}, S_{A2} is turned off as shown in Fig. 4.14.

Interval III (T_1+ T_2 - T_1+ T_2+ T_3)

After S_{A2} is turned off, the voltage across S_{A1} drops to zero due to resonance between devices' capacitors and inductor L_a, hence S_{A1} is turned on at 0 V. At the beginning of interval III, S_{A1} is turned on. Thus i_a starts to fall, the equivalent circuit is shown in Fig. 4.16, the phase currents' slopes are given by:

$$di_a / dt = (v_a - 2V_o / 3) / L \tag{87a}$$

$$di_b / dt = (v_b + V_o / 3) / L \tag{87b}$$

$$di_c / dt = (v_c + V_o / 3) / L \tag{87c}$$

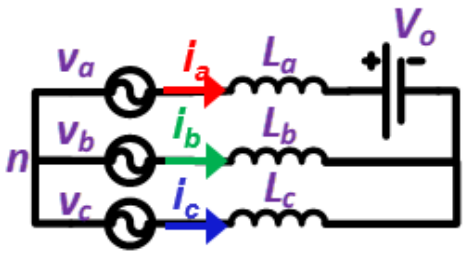


Figure 4. 16 Equivalent circuit in Interval III

The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{1}{L}(v_b + V_o / 3)T_3 \tag{88a}$$

$$i_{cp3} = i_{cp2} + \frac{1}{L}(v_c + V_o / 3)T_3 \tag{88b}$$

This interval ends when i_a reaches zero, S_{A1} is turned off at the end of *Interval* III.

Interval IV (T_1+ T_2+ T_3- T_1+ T_2+ T_3+T_4)

In this mode, S_{B2} and S_{C1} conduct, the equivalent circuit is the same as in interval IV of sector I (as shown in Fig. 4.12). The phase currents' slopes are given by Eq. 81. Thus i_c falls to zero during this interval, this interval ends when i_c reaches zero.

The operation of Interval V and VI is similar to Sector I, hence it is not discussed in detail for the sake of brevity. The switching times considering ideal devices are calculated from the following equations: T_5 and T_6 are calculated from (82) and (83) for a given I_R. T_3 and T_4 can be derived in terms of T_1 and T_2 from the following equations for sector I:

$$i_{ap1} + \frac{1}{L}(v_a + V_o / 3)T_3 = 0 \tag{89a}$$

$$i_{bp3} + \frac{1}{L}\frac{(V_o + v_b - v_c)}{2}T_4 = 0 \tag{89b}$$

Where i_{ap1} and i_{bp3} can be derived using Eqns. (76), (76) and (80). For sector II, T_3 and T_4 are derived from the following equations:

$$i_{ap1} + \frac{1}{L}(v_a - 2V_o/3)T_3 = 0 \tag{90a}$$

$$i_{bp3} + \frac{1}{L}\frac{(V_o + v_b - v_c)}{2}T_4 = 0 \tag{90b}$$

Where i_{ap1} and i_{bp3} can be derived using Eqns. (78), (88) and (90). Thus T_1 and T_2 can be derived from average current equations:

$$i_{aavg} = \frac{i_{ap1}(\frac{T_2 + T_3}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_a \tag{91a}$$

$$i_{bavg} = \frac{i_{bp1}\frac{T_1}{2} + (i_{bp1} + i_{bp2})\frac{T_2}{2} + (i_{bp2} + i_{bp3})\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} + \frac{i_{bp3}\frac{T_4}{2} - I_R(\frac{T_5 + T_6}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_b \tag{91b}$$

The switching times for a 1.2 kW, 400 V V_{dc}, 115 V_{inrms}, L= 4 µH converter are shown in Fig. 4.17. The inductance is the same as in unity power factor. Minimum I_r for positive solutions of conduction times is calculated as -3.3 A as to compensate for the reactive power, higher ripple is needed.

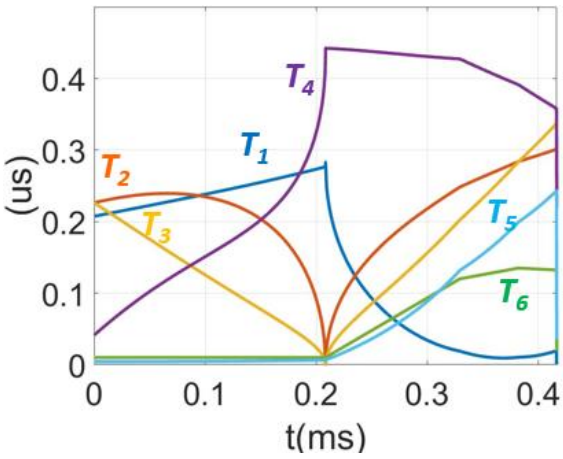


Figure 4. 17 Switching times for 1.2 KW P_o, 400 V V_{dc}, L~ 4 µH, 115 V V_{acrms}, 30° lagging power factor

The full line cycle control showing phases operating DCM, TCM and Clamped mode is shown in Fig. 4.18. The phase with the maximum absolute voltage is clamped, minimum absolute average

current is in DCM, and the third phase operates in TCM. The switching frequency variation from 0-60^{o} is shown in Fig. 4.19, it's only 12.5 % as compared to >2* variation in decoupled TCM. The variation is symmetric after every 60^{o}.

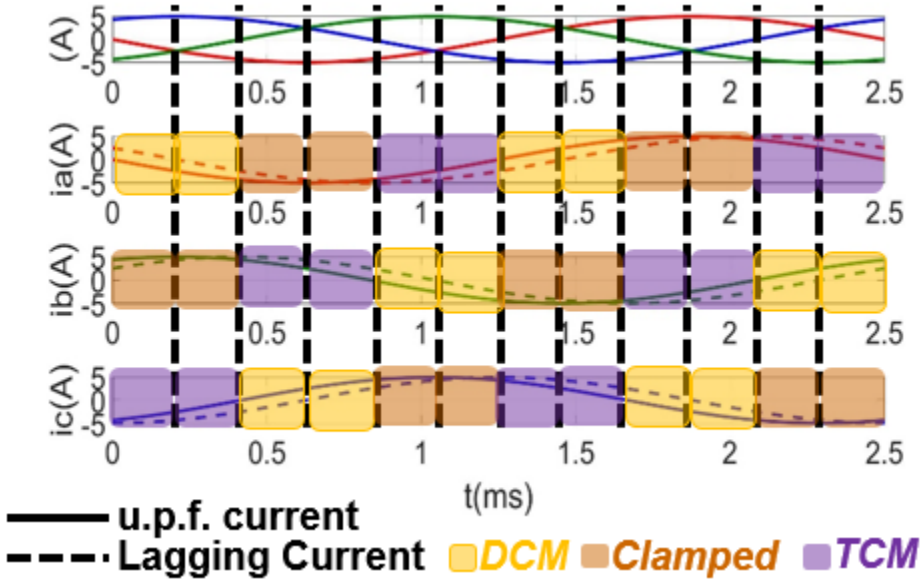


Figure 4. 18 Full line cycle control for 30^{o} lagging power factor

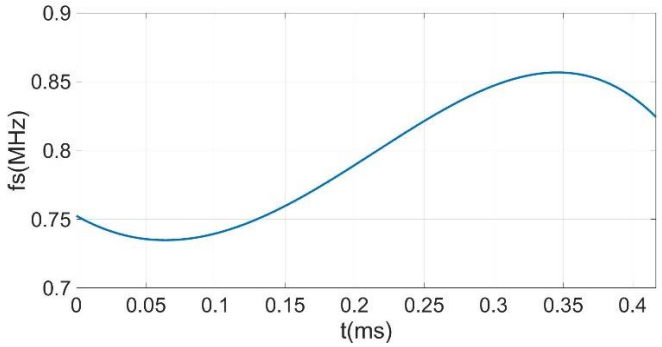


Figure 4. 19 Switching frequency variation for 1.2 KW P_o, 400 V V_o, L~ 4 µH, 115 V V_{inrms}, 30^{o} lagging power factor

4.2.3 Verification by Simulation

The converter is simulated from pre-calculated switching times (T_1, T_2, T_3, T_5 and T_6), T_4 is detected in real time by ZCD of TCM phase. The simulated phase currents are shown in Fig. 4.20, ideal devices are considered in this simulation. The zoomed in waveforms in sector I and II are shown in Figs. 4.21 and 4.22 respectively.

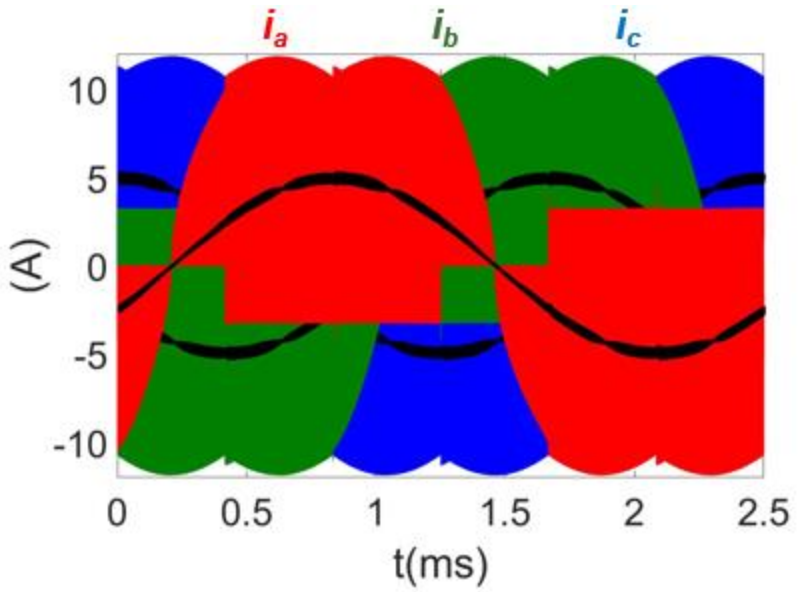
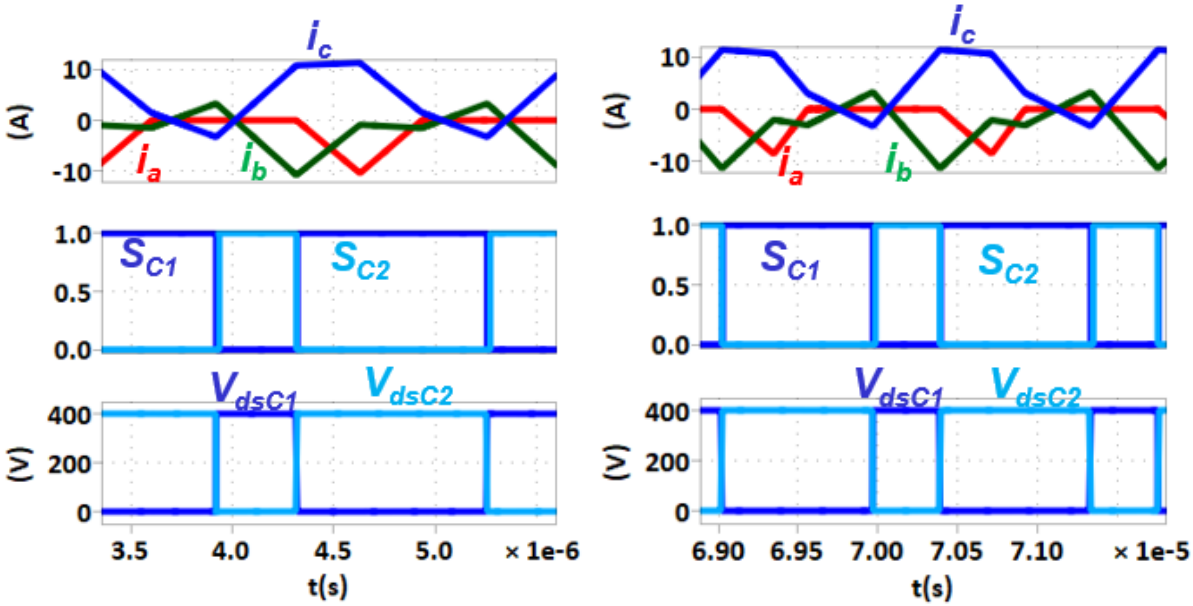
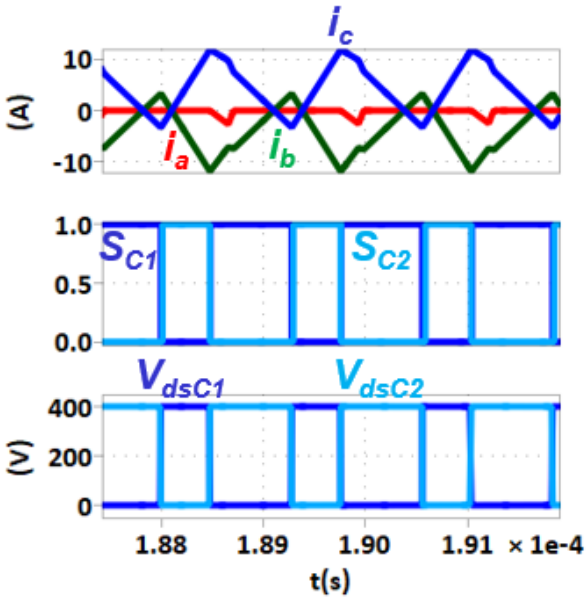


Figure 4. 20 Simulated phase currents for 1.2 kVA, 400 V V_o, 115 V V_{acrms}, L~ 4 µH, 30^o lagging power factor rectifier mode

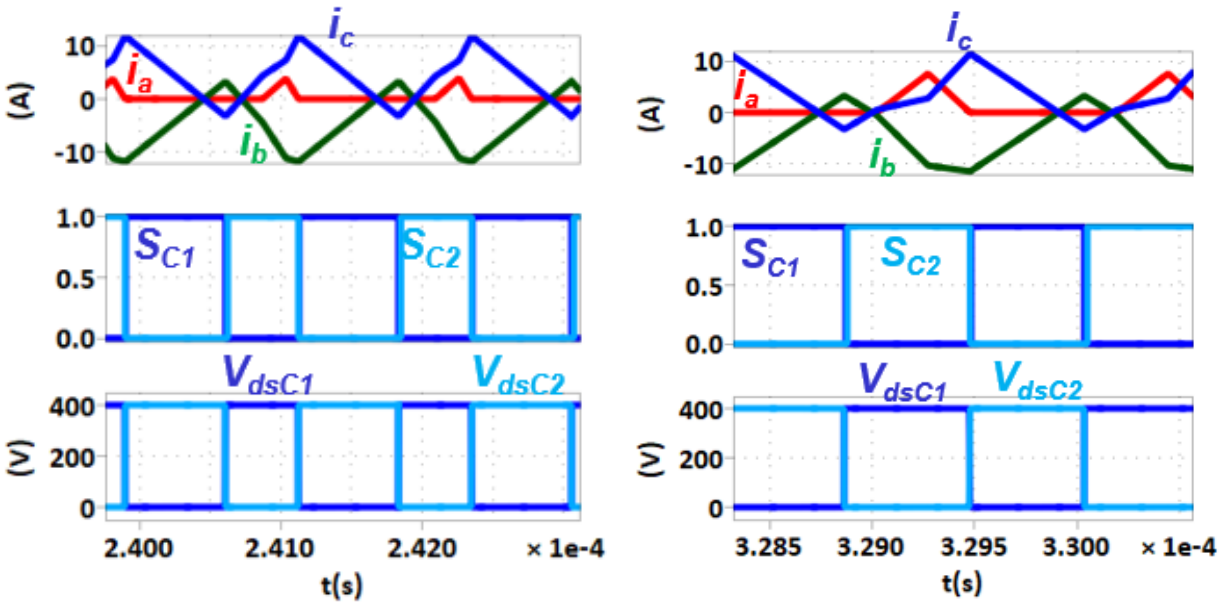


(a) (b)

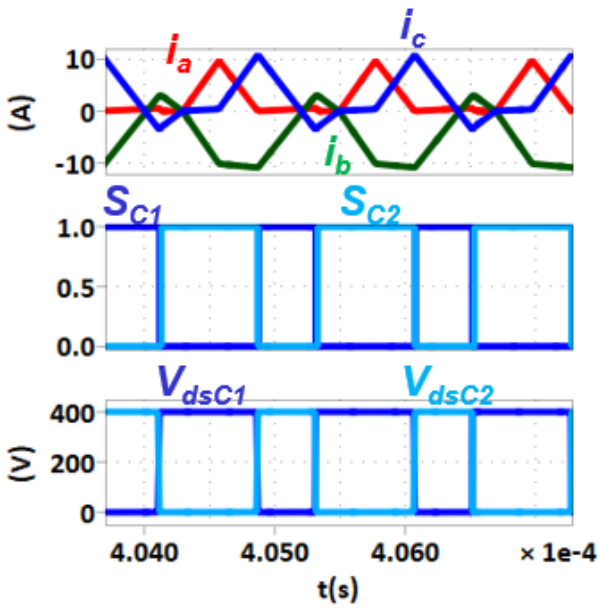


(c)

Figure 4. 21 Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector I



(a) (b)



(c)

Figure 4. 22 Zoom in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector II

The loss breakdown comparison is shown in Fig. 4.23. Despite higher conduction losses due to higher ripple, the converter can still maintain ~99 % efficiency at 0.8 MHz.

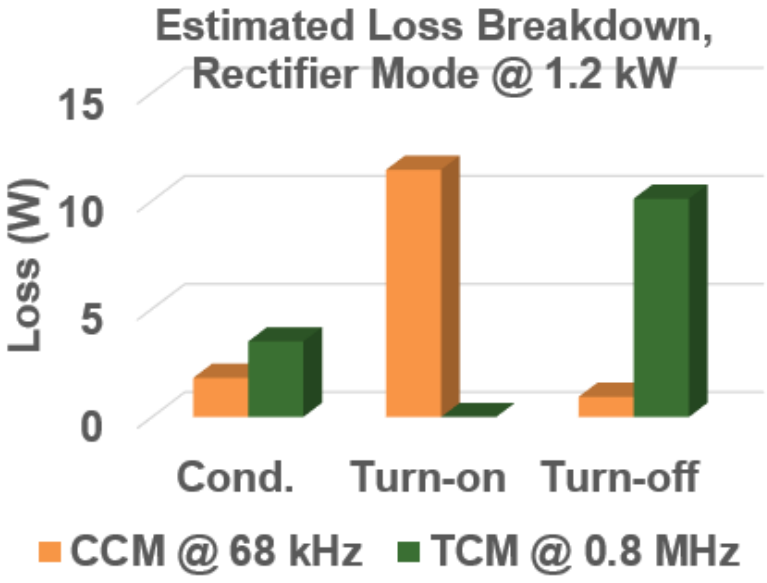
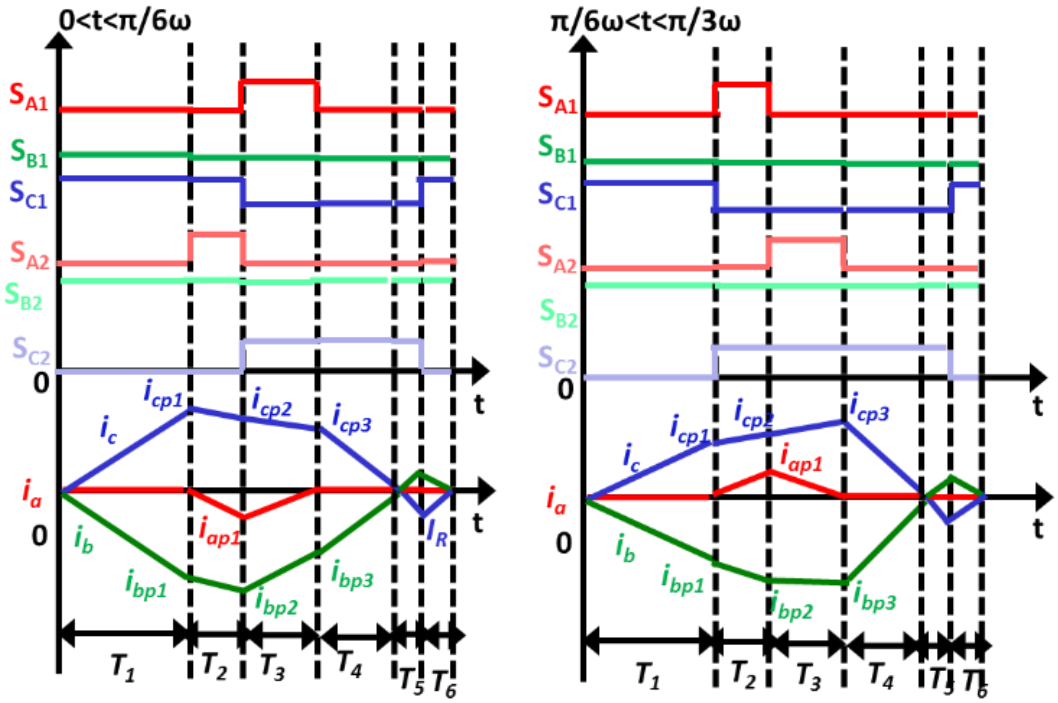


Figure 4. 23 Loss Breakdown Comparison of CCM at 50 kHz and TCM at 0.8 MHz at 1.2 KVA, 400 V V_o, 115 V V_{inrms}, 30^o lagging power factor

4.3 Control Implementation

The DSP implementation is very similar to unity power factor mode in Chapter 4, based on the relative magnitude of average currents and voltages, the controller assigns DCM, TCM or clamped mode of operation to each phase. The times T_1 and T_2 are generated by the average current compensators.

The operation for 30° lagging inverter mode is very similar to rectifier mode. The gate signals for one switching cycle in sector I and II for inverter mode are shown in Fig. 4.24 (a)and(b). Average reference currents and voltages for inverter mode are shown in Fig. 4.25.



(a) (b)

Figure 4. 24 One switching cycle waveform for 30° phase lag in (a) Sector I (b) Sector II inverter mode

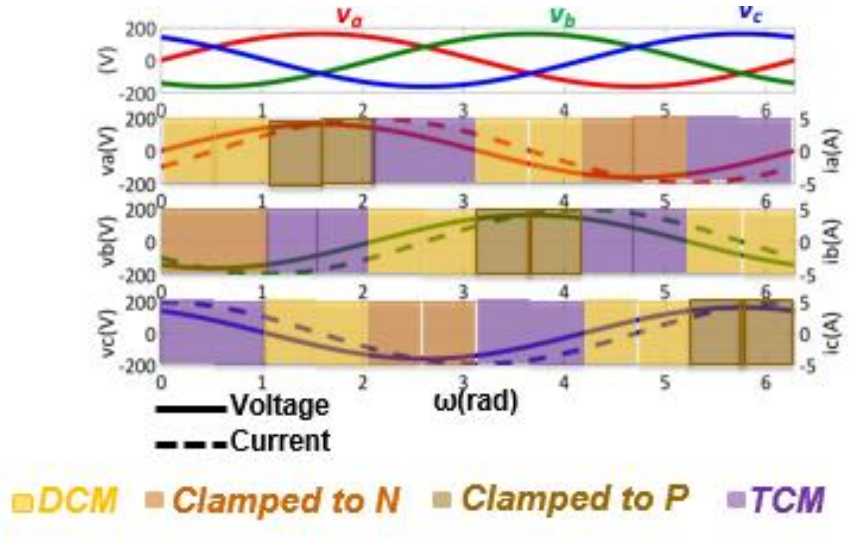


Figure 4. 25 Full line cycle control for inverter mode

The classified phase currents as DCM, TCM and clamped currents are shown in Fig. 4.26. Since after every 60^o the phase clamped is changed and the clamping decision is taken based on voltage magnitude, hence i_{TCM} has a jump after every 60^o. The closed loop implementation is shown in Fig. 4.27.

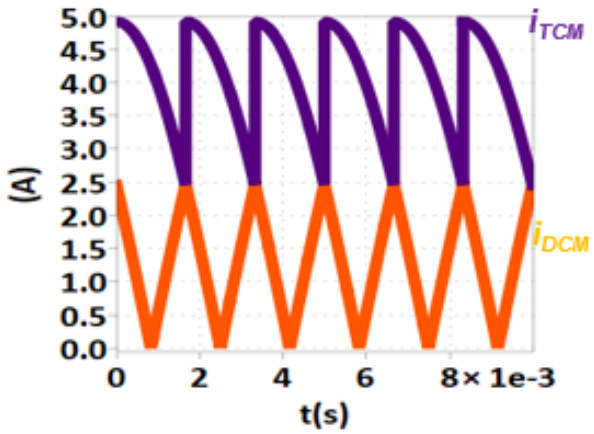


Figure 4. 26 Reference DCM and TCM currents symmetric after every 60^o

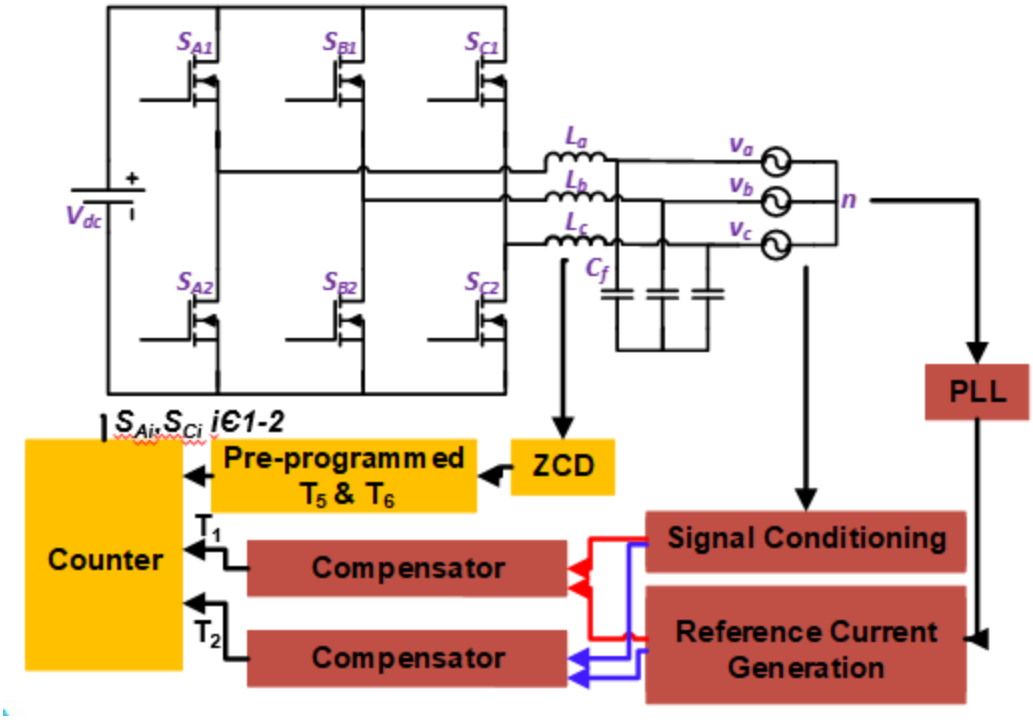


Figure 4. 27 Controller implementation for sector I

It can be seen in Fig. 4.28 that the currents are symmetric after every 60^o and the TCM reference current has a jump after every 60^o. This jump is also visible in T_1 in Fig. 4.17, hence it can be concluded that a high feedforward gain is required in the compensator for phase shifted currents.

4.3.1 Verification by Simulation

The simulation results with the closed loop implementation for 1.2 kVA, 400 V V_{dc}, 115 V V_{acrms}, L= 4 µH, 30^o lagging inverter mode are shown in Fig. 4.28. The detailed operation in inverter mode is very similar to rectifier mode. The zoom-in current waveforms are shown in Figs. 4.29 and 4.30.

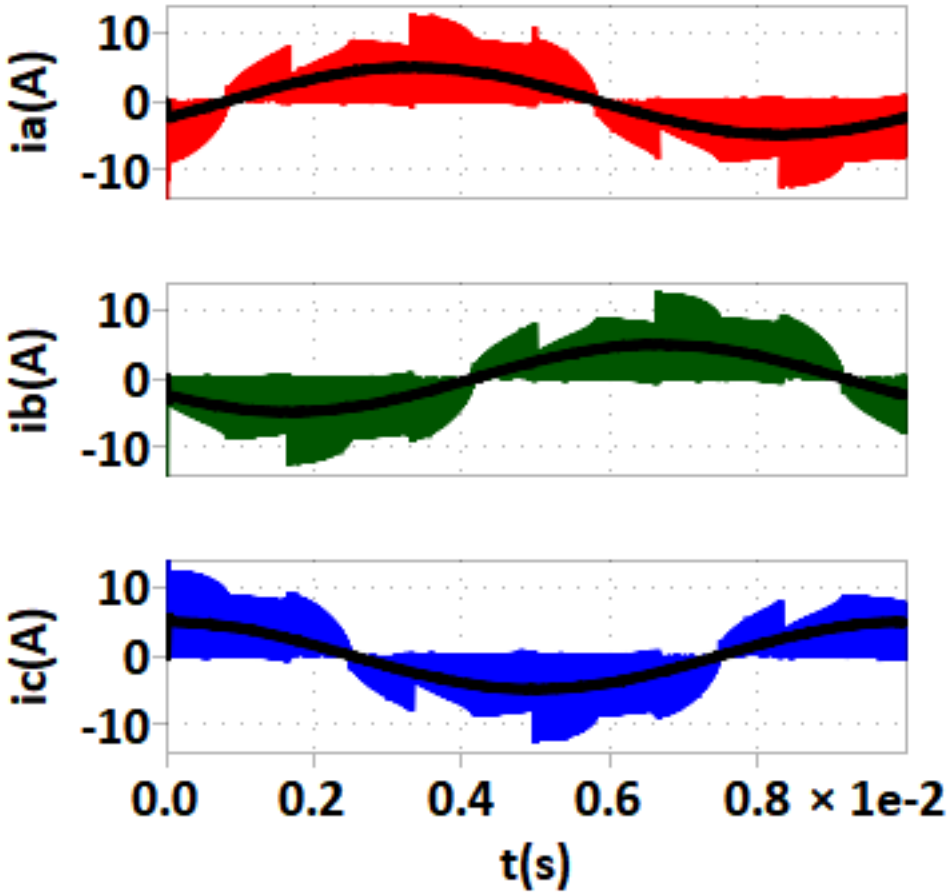
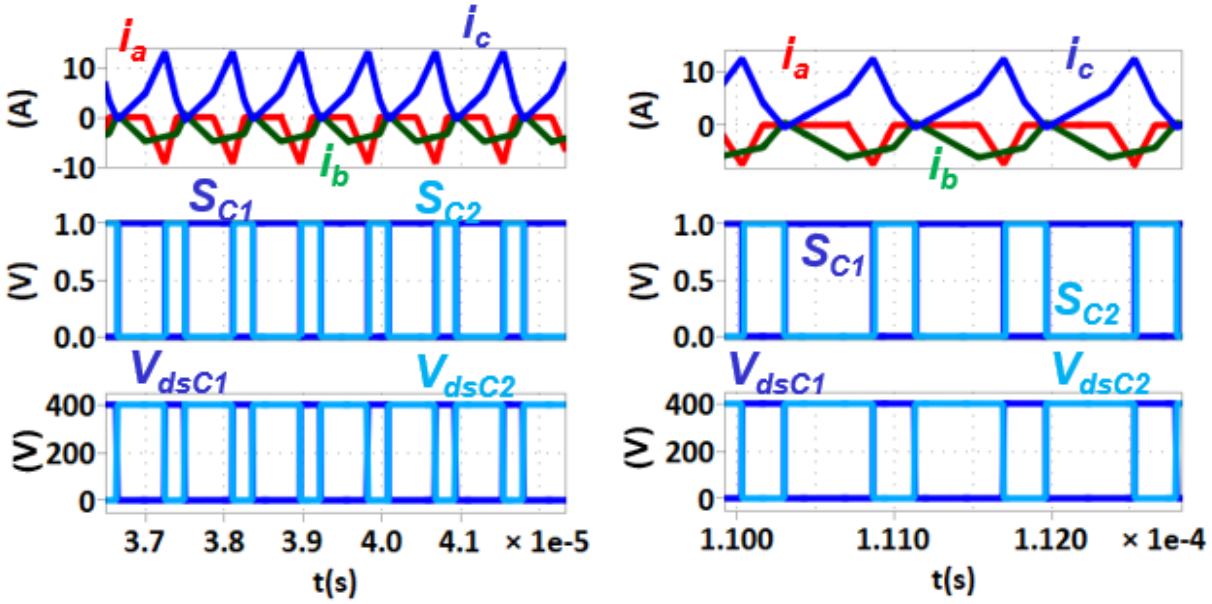
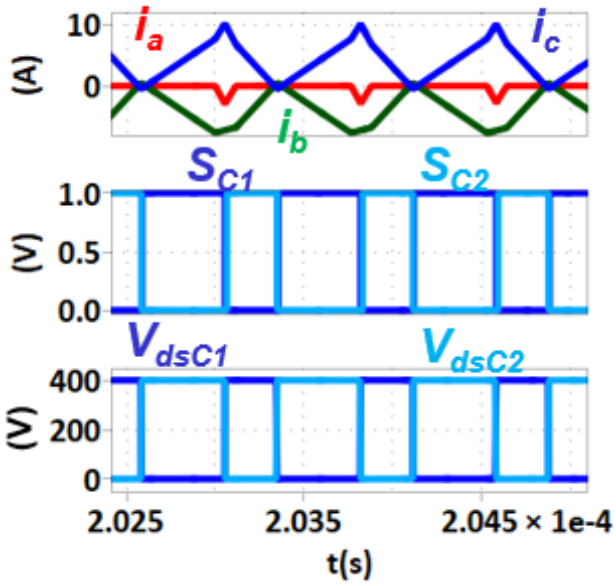


Figure 4. 28 Simulated phase currents for 1.2 kVA, 400 V V_{dc}, 115 V_{acrms}, L= 4 µH, 30° lagging inverter mode

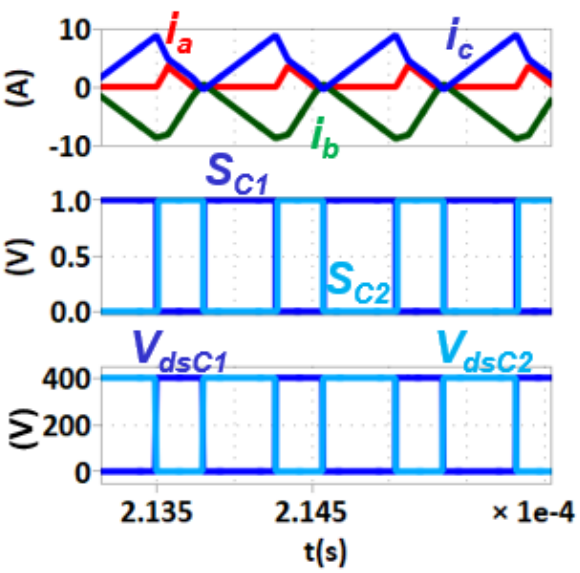


(a) (b)

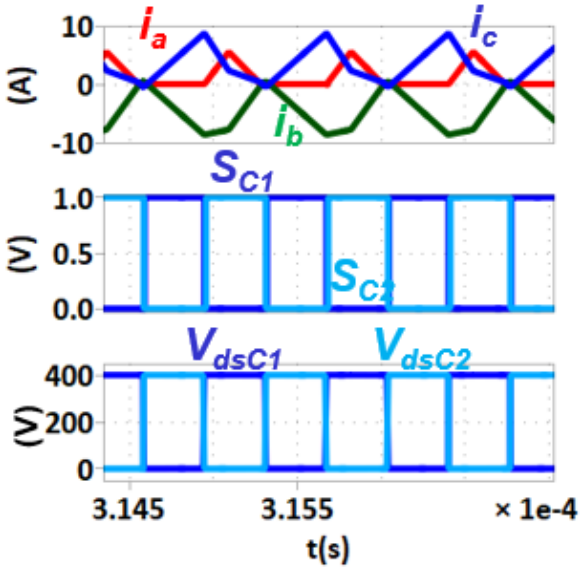


(c)

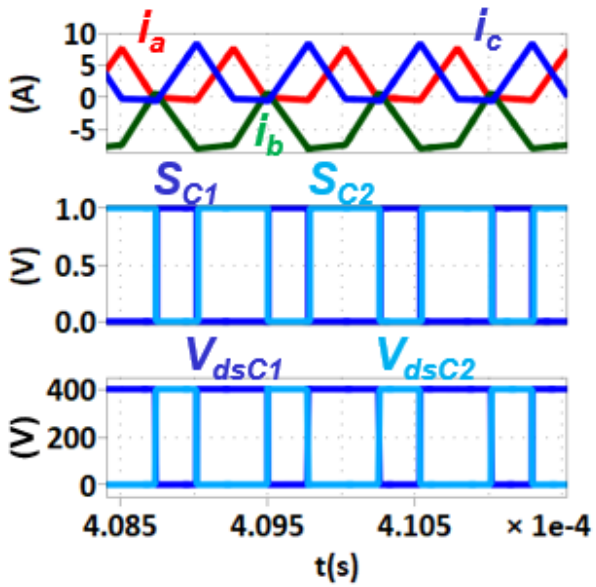
Figure 4. 29 Zoom-in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector I for inverter mode at 30^{o} lagging power factor



(a)



(b)



(c)

Figure 4. 30 Zoom-in current and gate signal waveforms showing ZVS turn-on for TCM phase in (a) beginning (b) middle and (c) end of sector II for inverter mode at 30^{o} lagging power factor

The filtered phase currents are shown in Fig. 4.31, the currents are able to follow the reference currents.

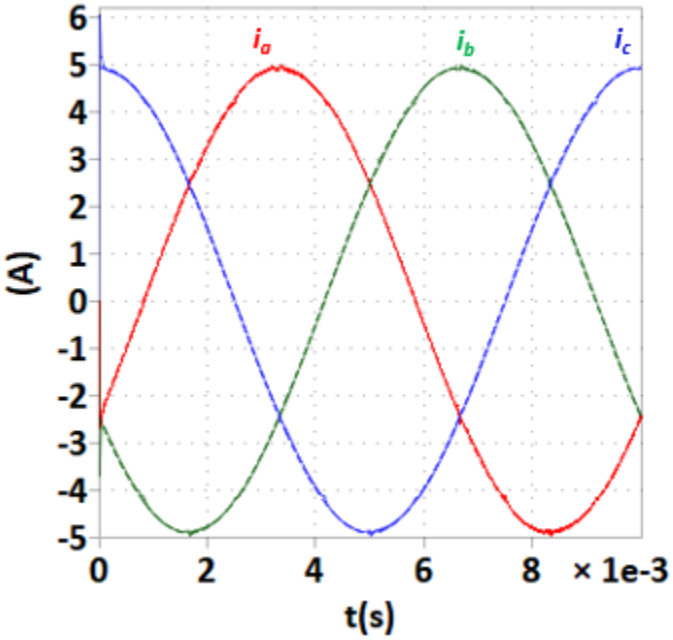


Figure 4. 31 Filtered phase currents

4.4 Experimental Verification

The proposed algorithm is validated on the GaN converter shown in Chap. 3. The initial compensator design is the same as discussed in Chap. 3 for unity power factor, however even after PI controller tuning, the filtered currents had >10 % THD. The causes for the same are investigated below.

4.4.1 Revised Compensator Design

The key challenges for phase shifted current operation are implementation with asymmetry combined with hardware delays causing higher negative current making the system more complex. Thus, to model the simulation as close as possible to the experimental setup, the delays caused by ZCD signal, controller and converter delays are integrated into the system. The values used for the TCM and DCM compensators are shown in Table 4.1.

Parameter	DCM	TCM
K_p	$4*10^{-8}$	$5*10^{-8}$
K_i	$3*10^{-8}$	$5*10^{-6}$
K_{ff}	$2*10^{-7}$	$1*10^{-8}$

Table 4. 1 Compensator gains

The simulation results with hardware and controller delays included in the model are shown in Figs. 4.32 and 4.33. The results shown in Fig. 4.31 were from a model not considering these delays. It can be seen from Fig. 4.32 that the ripple increases after delays are included, also the filtered phase currents have glitches. These glitches occur after every 60^o.

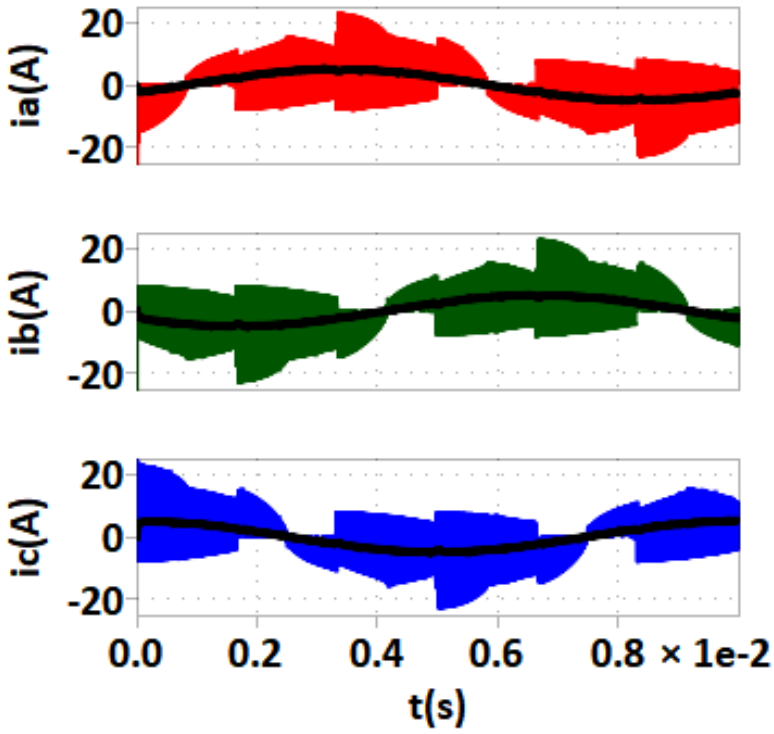


Figure 4. 32 Simulated phase currents after considering delays in the model

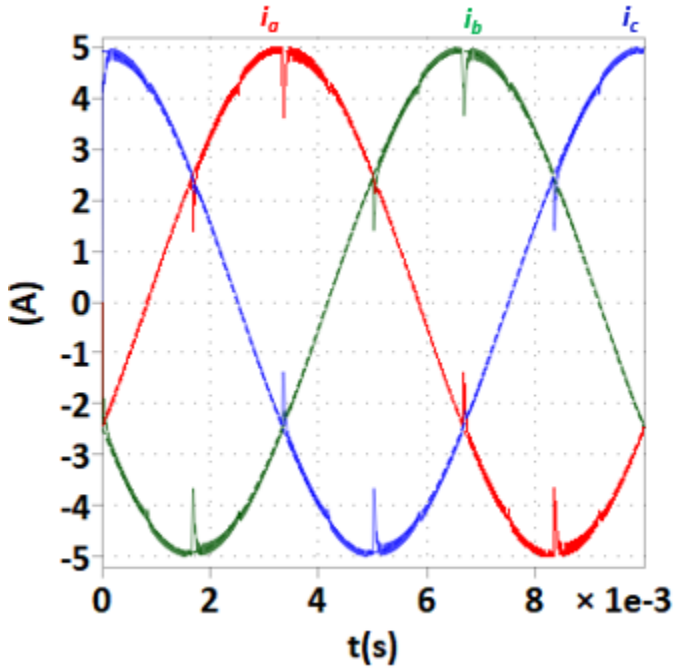


Figure 4. 33 Simulated filtered phase currents after considering hardware delays in the model.

The control times T_1 and T_2 are analyzed to get a deeper understanding of the issue. The plots for T_1 and T_2 are shown in Fig. 4.34. It is clear that like i_{TCM} (from Fig. 4.28), T_1 also requires an offset after every 60°. This offset is partly supplied by feedforward control however the feedforward gain cannot be further increased as higher K_{ff} leads to distortion in currents in the middle of sectors. One of the methods that could be employed is an offset addition in T_1 after every 60°. An offset of 100 ns is added to T_1 after every 60° and the simulated results are shown in Fig. 4.35.

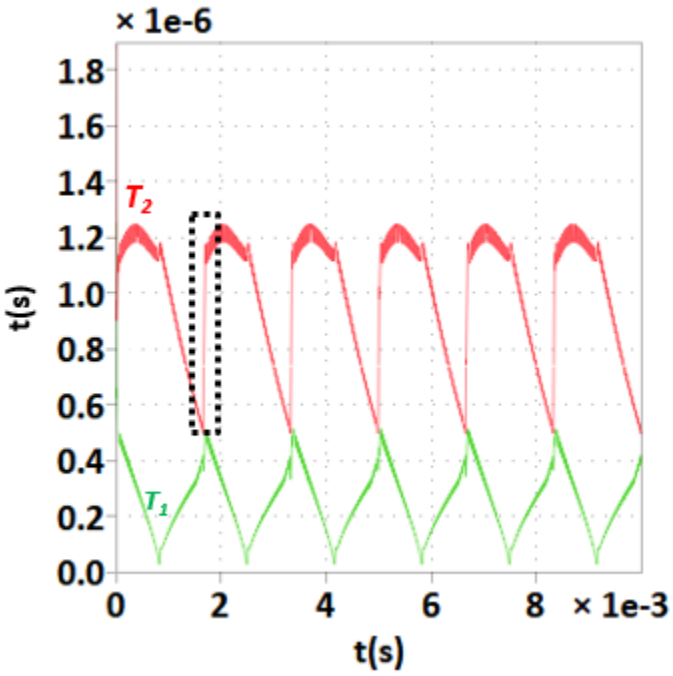


Figure 4. 34 T_1 and T_2, jumps in T_1 required

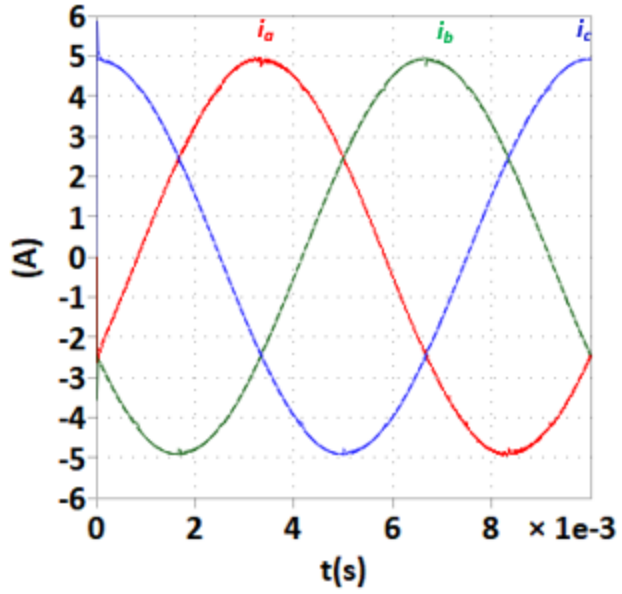
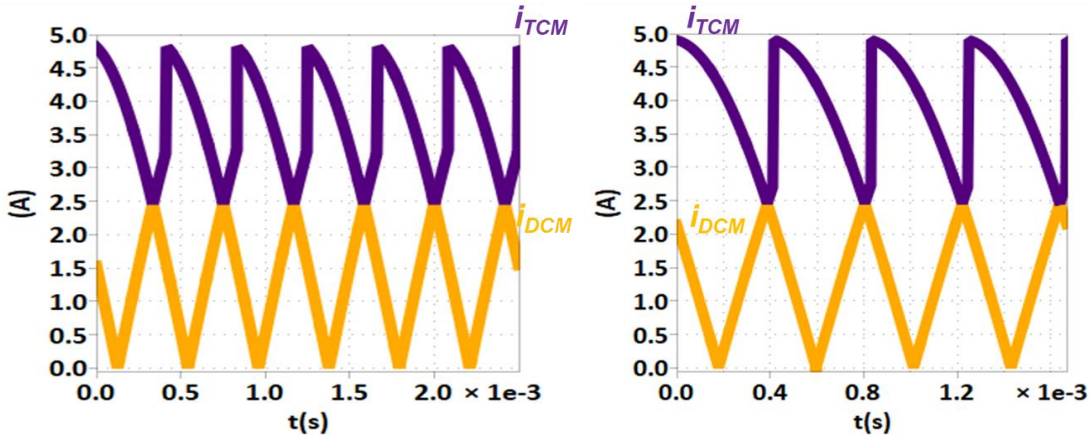


Figure 4. 35 Simulated filtered phase currents after an offset is added to T_1 after every 60°.

The position of offset is same for -30°-30° phase shift, it occurs after every 60° as shown in Fig. 4.36. The simulation results for 0.95 lag, 400 V V_{dc} and 1.2 kVA are shown in Fig. 4.37. A generic simulation model is built for the range of -30°-30° phase shift



(a) (b)

Figure 4. 36 Reference DCM and TCM currents for (a) 0.95 lag and (b) 0.9 lag

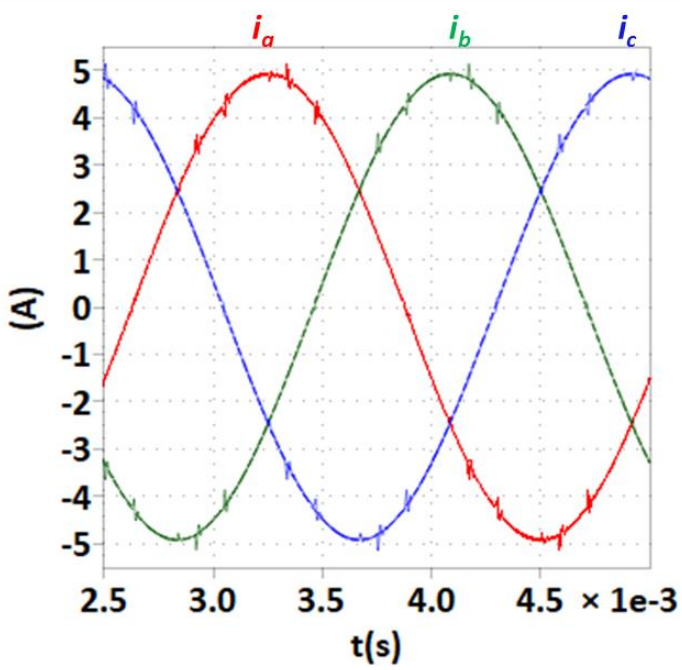


Figure 4. 37 Simulated filtered phase currents for 0.95 lagging power factor.

4.4.2 Experimental Results

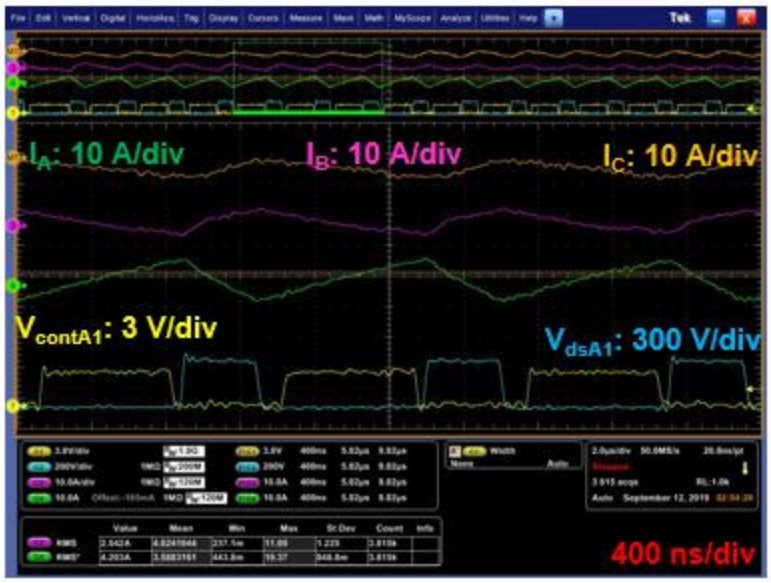
TCM and DCM phase ZVS turn-on is validated and shown in Fig. 4.38 and 4.39 respectively. The operating conditions are:

V_{dc}= 300 V

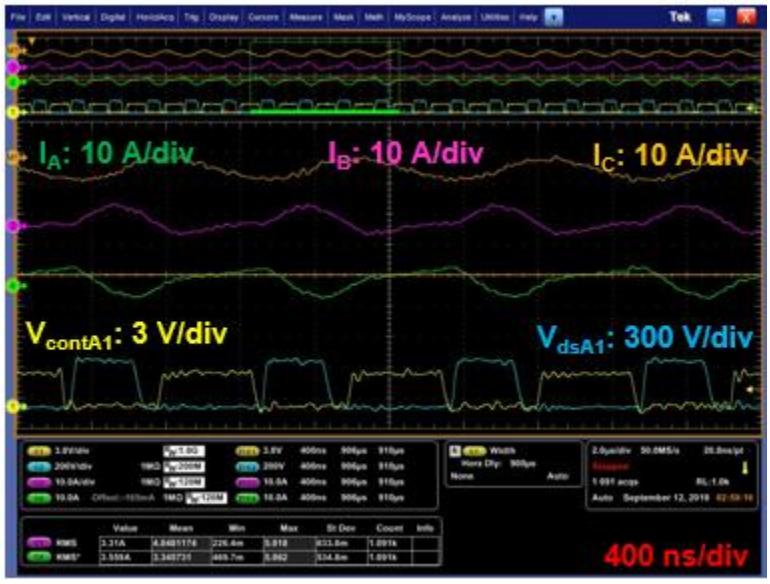
S_o= 0.675 kVA

P.f.= 0.866

V_{acrms}=86.25 V

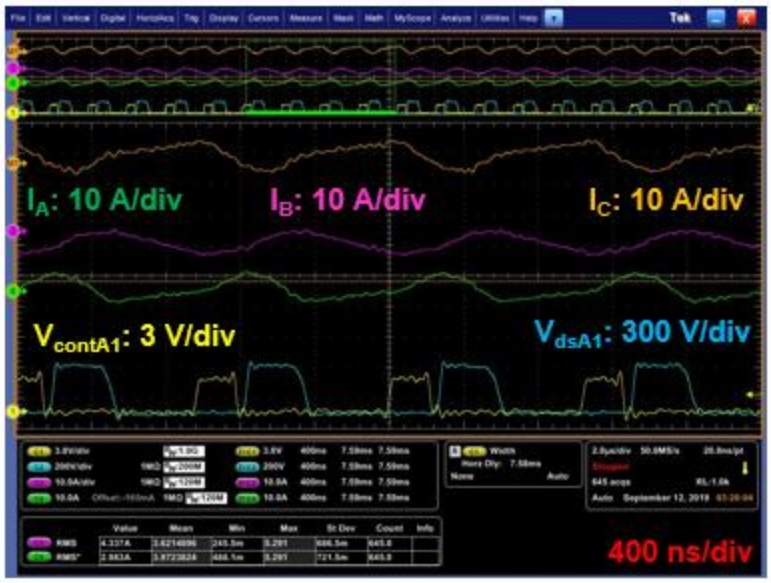


(a)

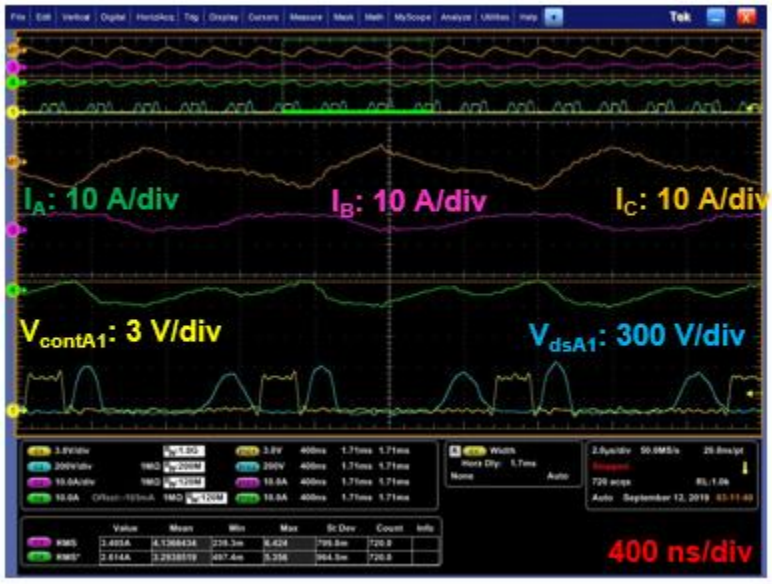


(b)

Figure 4. 38 Phase A operating in TCM mode in (a) Sector V and (b) Sector VI, controller signal goes high after V_{dsA1} has reduced to 0 V.



(a)



(b)

Figure 4. 39 Phase A operating in DCM mode in (a) Sector II and (b) Sector VII, controller signal goes high after V_{dsA1} has reduced to 0 V.

Full line cycle currents are shown in Fig. 4.40. The measured system efficiency is 98.54 % at 300 V V_{dc}, 0.675 kVA, 30^o lagging power factor and 600- 850 kHz switching frequency range. These losses includes the inductor losses, ZCD shunt resistor losses and connector losses. Switching frequency range is 600- 850 kHz, this drop is owing to higher negative current detection

issue discussed in Chap. 3. The final density achieved is 110 W/in^3 which can be improved by a more optimized assembly of the system. Measured filtered currents are shown in Fig. 4.41. The THD is 6.51 %.

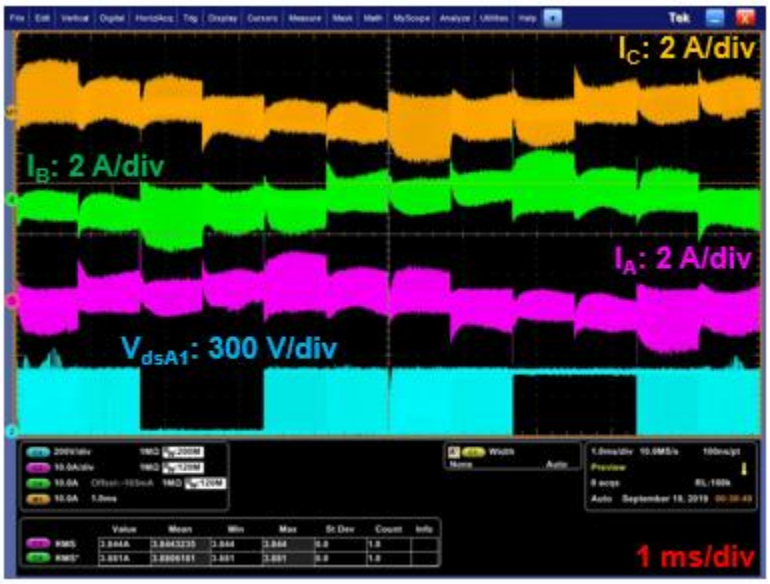


Figure 4. 40 Phase currents for V_{dc}= 300 V, S_o=675 VA, V_{acrms}= 86.25 V, p.f.= 0.866 lagging

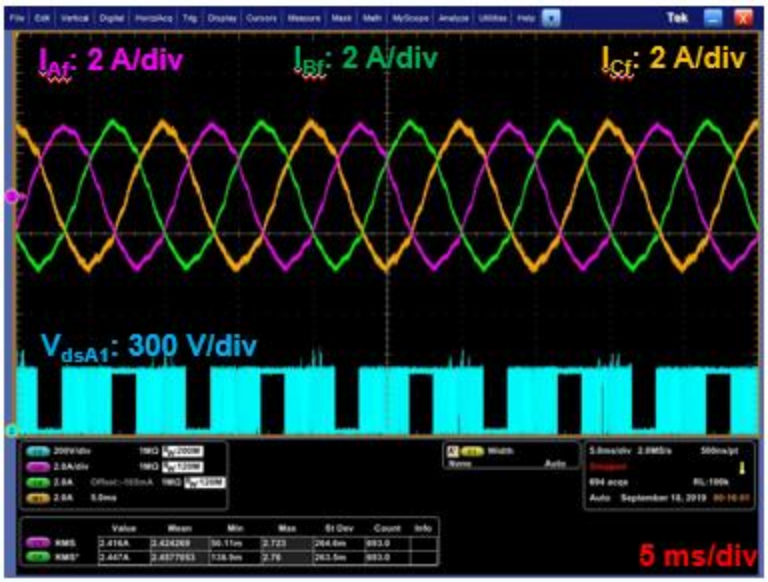


Figure 4. 41 Filtered phase currents, measured THD= 6.51 %

4.5 Extension to Purely Reactive Power

In the previous section, proposed TCM control is extended to active + reactive power, however the ripple also increases. To extend the capability of proposed control, it is discussed in this section if this control can be applied to purely reactive power cases. The average currents for 90° phase lag are shown in Fig. 4.42. It can be seen that in this case, the phase with maximum voltage has the minimum average phase current requirement. This will start happening beyond 30° phase shift. Hence, now the phase with maximum average current cannot be clamped. It instead operates in TCM with ZVS turn-on.

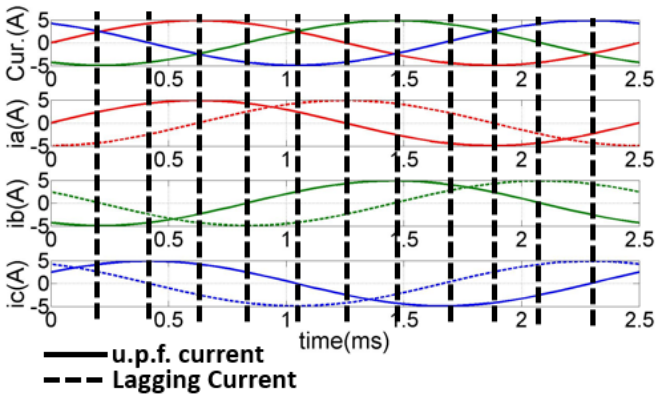


Figure 4. 42 Average currents for u.p.f. and 90° lagging cases

It can be seen in Fig. 4.42 that the case of 90° phase lag has full circular symmetry, thus operation in only one sector is discussed in detail. The switching waveform with gating signals for one switching cycle in sector I is shown in Fig. 4.43. It can be seen (from Fig. 4.42 and 4.43) that the phase with highest average and switching current operates in TCM while the phase with minimum average current but higher switching current is clamped (phase B in sector I), thus still saving on switching losses. The full line cycle control is shown in Fig. 4.44.

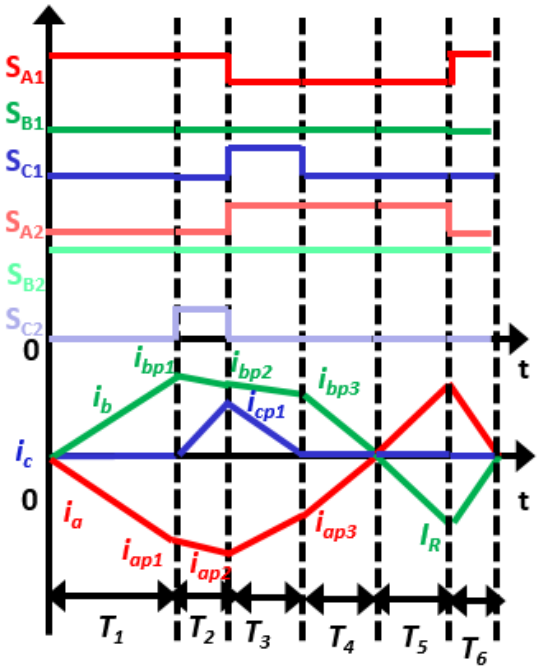


Figure 4. 43 One switching cycle waveform for 90˚ phase lag in Sector I

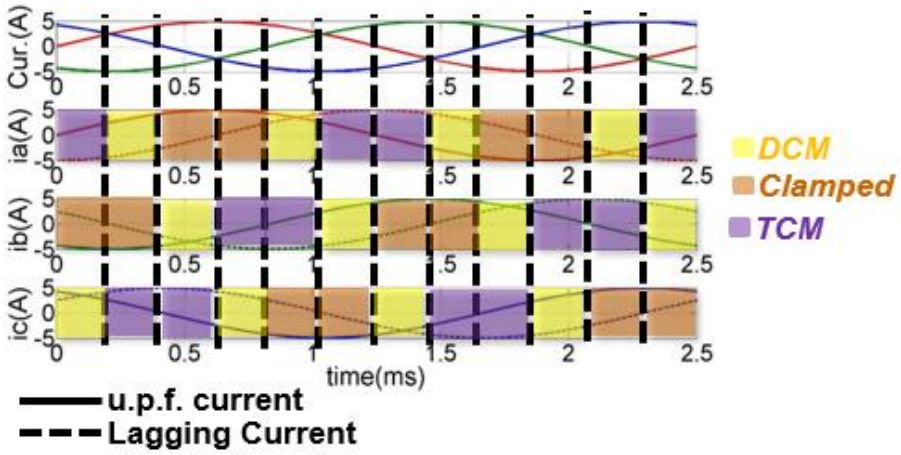
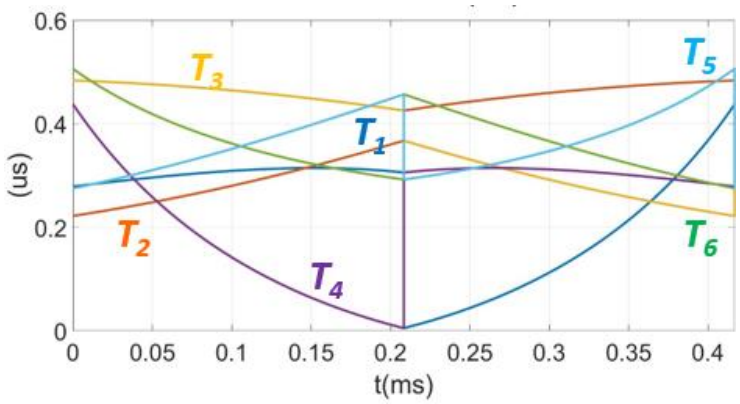


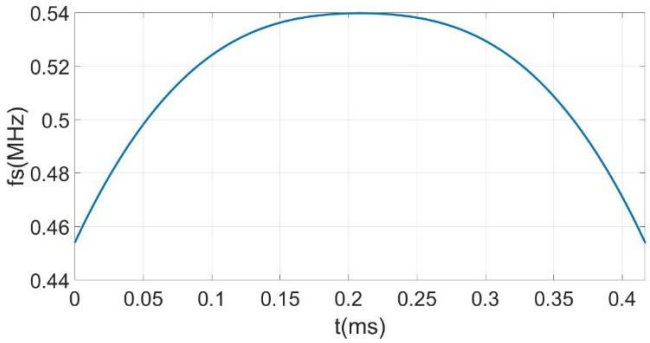
Figure 4. 44 Full line cycle control for 90º lagging current

4.5.1 Verification by Simulation

The solution for switching times (for sector I and II) for a 1.2 kVA, 400 V V_o, 115 V_{inrms}, L= 4 µH, 90˚ phase lag is shown in Fig. 4.45(a). I_R has to be increased to -9 A to obtain positive solutions for the complete range of time. The switching frequency variation is shown in Fig. 4.45(b). Simulated phase currents (for ideal devices) is shown in Fig. 4.46(a). The zoom in waveforms of currents is shown in Fig. 4.46(b).

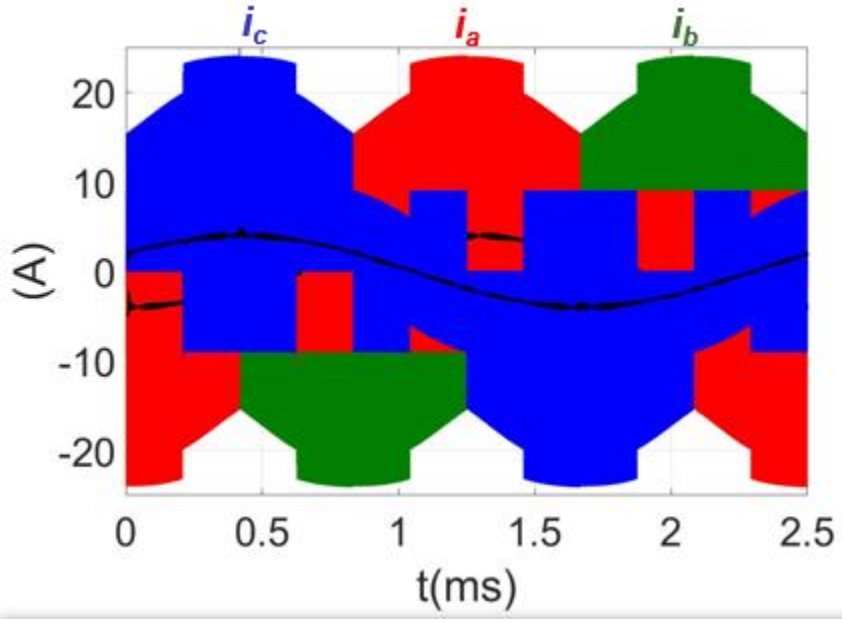


(a)

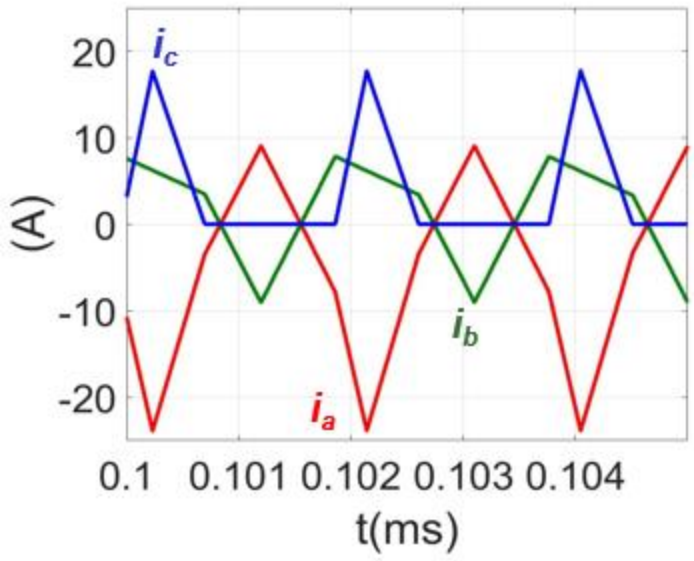


(b)

Figure 4. 45 90˚ phase lag 1.2 kVA, 400 V V_o, 115 V_{inrms}, L= 4 µH (a) Switching times solution assuming ideal devices for sector I and II (b) Switching frequency variation from 0-60˚



(a)



(b)

Figure 4. 46 90˚ phase lag 1.2 kVA, 400 V V_o, 115 V_{inrms}, L= 4 µH (a) Full line cycle phase currents (b) zoom in waveform of phase currents

Hence, TCM can be pushed for the entire range of power factor but on the cost of increase in ripple and hence conduction losses. Also, the phase with maximum average current magnitude cannot be clamped beyond 0.866 power factor.

4.6 Summary

As shown above, proposed DCM+TCM+Clamped operation can be extended to reactive power cases. The switching frequency variation is still very small (41.66%) as compared to >2* variation in decoupled TCM. TCM for meeting reactive power demands has never been discussed which limits its practical application. The biggest challenge for phase shifted current TCM is that the average phase currents ripple shape and hence magnitude are dependent on respective phase voltages. When the phase with maximum average current magnitude is clamped (like in clamped SVM and TCM unity power factor discussed in Chap. 3), it leads to instability in the system as the body diode of one of the devices in DCM phase starts conducting when the DCM phase should be off. This current is opposite in sign compared to the reference current, this leads to undesirable

ripple in all the phases which the controller is unable to compensate for. Thus, the phase with maximum magnitude of voltage is clamped.

Another key challenge is that since the phase clamping decision is taken on the bases of phase voltage while the DCM and TCM phases are classified on the basis of phase currents' magnitudes, it leads to discontinuity in the TCM reference currents. This discontinuity combined with the delays caused by converter, sensing circuit and the controller leads to glitches in the currents after every 60^o. Thus, to solve this issue an offset is added to the controller output at a frequency six times fundamental frequency. This offset addition technique is verified by simulating a model for -30^o-30^o phase shift and no glitches are observed.

The DCM and TCM phases ZVS turn on is validated on the GaN converter. Thus, all the three phases turn on at 0 V reducing the losses and CM noise. The final system efficiency measured is 98.54 % with a power density of 110 W/in^3 at 300 V V_{dc}, 0.675 kVA, 30^o lagging power factor.

It is shown that TCM can be pushed for the entire range of power factor but at the cost of increase in ripple, hence conduction and turn-off losses also increase. Also, the phase with maximum average current magnitude cannot be clamped beyond 0.866 power factor. So, the optimal range of phase shift for DCM+TCM+Clamped operation is found to be -30^o-30^o.

The proposed algorithm achieves phase synchronization, sinusoidal currents and <40 % switching frequency variation. It achieves 99 % efficiency and >100 W/in^3 power density at 300 V V_{dc}, ~0.7 kW power level and ~0.5 MHz switching frequency for the two-level GaN converter. As compared to CCM where the peak efficiency achieved by this converter is 97 % and the density is < 50 W/in^3. Thus, in the next chapter it is discussed how the proposed algorithm can be extended to the three-level converter with the added benefit of reduced CMV to explore the algorithm's benefits for other topologies.

Chapter 5. TCM for Three-Level Topologies

This chapter discusses extension of proposed TCM algorithm to three-level converter topologies. A three-level Neutral Point Clamped (NPC) inverter is shown in Fig. 5.1 and a three-level T-type inverter is shown in Fig. 5.2. The extension of TCM+DCM+Clmaped algorithm to achieve ZVS turn-on, phase synchronization, sinusoidal average currents and very small switching frequency variation is discussed. As power requirements increase, the two-level converter needs a large size filter and higher blocking voltage rated devices. To mitigate these disadvantages, three-level converters are employed in high power and high voltage applications.

As shown in Figs. 5.1 and 2, in the three-level topology each phase can be connected to *N*, *P* or *O* state in the DC bus as opposed to only *N* or *P* states in the two-level topology. Hence, the objective of proposed algorithm is also to make the best use of the *O* state as this state exhibits the property of lower common mode voltage (CMV) which is discussed in the next section.

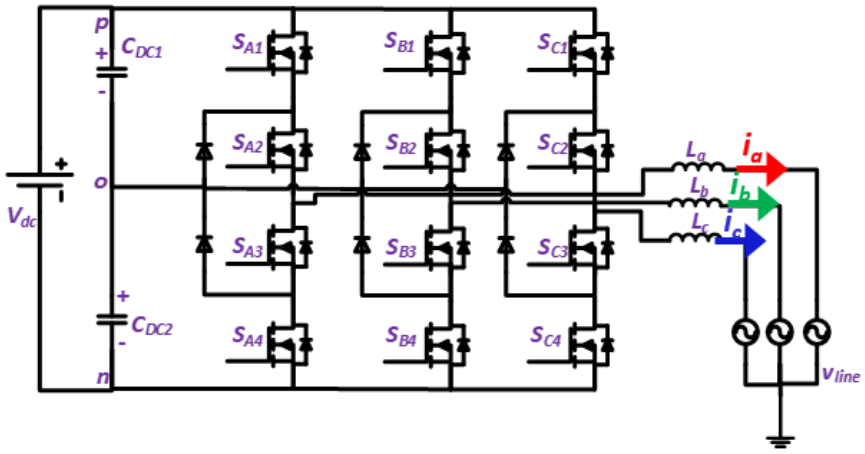


Figure 5. 1 Three-level NPC inverter

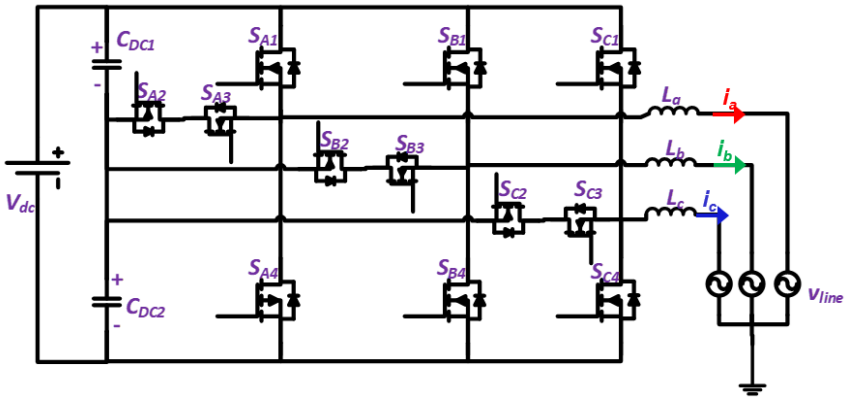


Figure 5. 2 Three-level T-type inverter

5.1 Theory

As shown in previous chapters, ZVS turn-on can be achieved for a two-level converter without adding any extra resonant components, thus the same principle is extended to a three-level inverter in this chapter. The modulation discussed for a two-level inverter can be directly implemented to a three-level inverter but one of the advantages of the three-level topology is reduced common mode voltage (CMV). This advantage of this topology is made use of in the proposed modulation schemes. CMV (v_{CM}) is defined as:

$$v_{CM} = \frac{(S_a + S_b + S_c)}{3}\frac{V_{dc}}{2} \tag{92a}$$

Where

$$S_i = \begin{bmatrix} 1 \text{ for P} \\ 0 \text{ for O} \\ -1 \text{ for N} \end{bmatrix} \tag{92b}$$

As shown in Figs. 5.1 and 5.2, P is the positive DC bus point, N is the negative DC bus point while O is the DC bus mid-point in case of a three-level inverter. S_i represents the point to which each phase is connected in a switching state, the value of which is given by Eq. 92(b). The switching states and CMV in one switching cycle of the two-level inverter unity power factor modulation are shown in Fig. 5.3. It can be seen that the first switching state (N-N-N) has the highest CMV ($-V_{dc}/2$).

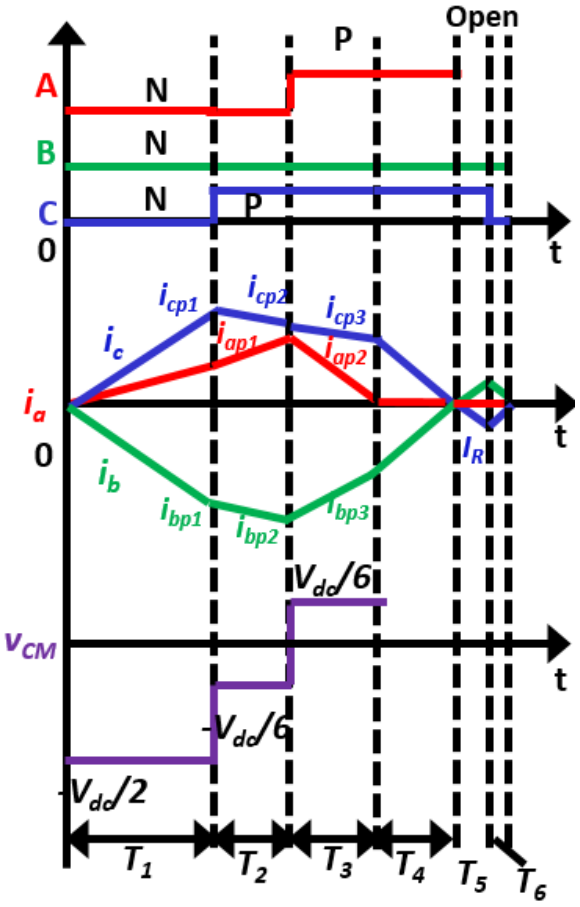


Figure 5. 3 Switching sequence and CMV in two-level TCM

5.2 Reduced CMV Switching Sequence I

The switching schemes discussed in this chapter make use of the reduced CMV states. The line cycle can still be divided into 12 sectors (like in a two-level converter) as shown in Fig. 3.3, where in each sector, the voltage direction and relative magnitude of the three-phase ac voltage is same. The ac voltages are given by Eq. 38. One switching cycle waveform in sector I ($0<\omega t<\pi/6$) is shown in Fig. 5.4. Each switching cycle can be divided into six intervals. The input voltages are assumed to be constant for one switching cycle as the switching frequency (f_{sw}) >> line cycle frequency (f_l). The detailed operation in each interval is discussed below.

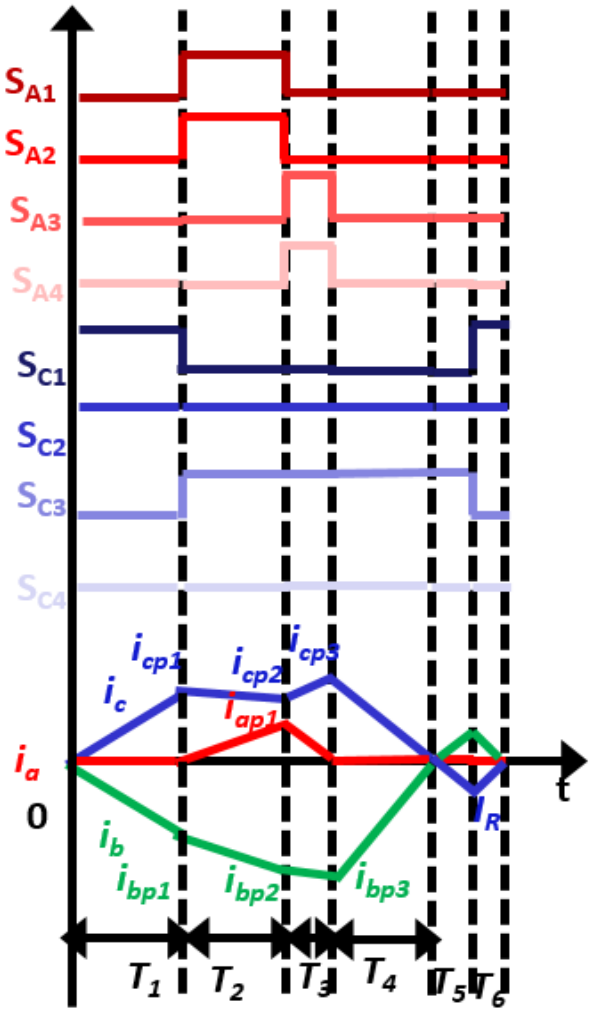


Figure 5. 4 One switching cycle waveform for TCM in inverter in Sector I for case a: when i_a reaches 0 before i_c reaches peak value i_{cp2}.

5.2.1 Mathematical Model

Interval I (0-T_1)

During interval I, S_{B3}, S_{B4}, S_{C1} and S_{C2} conduct leading to rise in i_c and fall in i_b. the equivalent circuit is shown in Fig.5.5, the phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (-V_{dc} + v_c - v_b) / 2L \tag{93}$$

The peak currents are given by:

$$i_{bp1} = -i_{cp1} = \frac{(-V_{dc} + v_c - v_b)}{2L} T_1 \tag{94}$$

After i_c reaches i_{cp1}, S_{C1} is turned off as shown in Fig. 5.4.

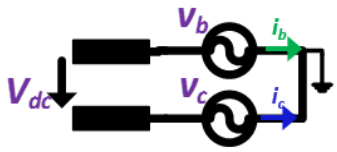


Figure 5. 5 Equivalent circuit in Interval I

Interval II (T_1-T_1+T_2)

After S_{C1} is turned off, resonance occurs in between phase C devices' output source capacitors (C_{oss}) and L_c, Because of this resonance, V_{dsC1} reaches $V_{dc}/2$ and V_{dsC3} reaches 0, the body diode of S_{C3} starts conducting and the switch can be turned on at 0 V. After S_{C3} is turned on, i_a starts to drop. The equivalent circuit is shown in Fig. 5.6, the phase currents' slopes are given by:

$$di_a / dt = (V_{dc} / 2 - v_a) / L \tag{95a}$$

$$di_b / dt = (-V_{dc} / 2 - v_b) / L \tag{95b}$$

$$di_c / dt = -v_c / L \tag{95c}$$

The peak currents are given by:

$$i_{ap2} = \frac{(V_{dc} / 2 - v_a)}{L} T_2 \tag{96a}$$

$$i_{bp2} = i_{bp1} + \frac{(-V_{dc} / 2 - v_b)}{L} T_2 \tag{96b}$$

$$i_{cp2} = i_{cp1} + \frac{-v_c}{L} T_2 \tag{96c}$$

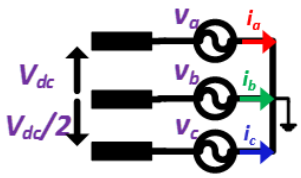


Figure 5. 6 Equivalent circuit in Interval II

Interval II ends when current i_a reaches peak current i_{ap1}, S_{A1} and S_{A2} are turned off at the end of this interval.

Interval III (T_1+T_2- T_1+T_2+T_3)

After S_{A1} and S_{A2} are turned off, resonance occurs in between phase A devices' output source capacitors (C_{oss}) and L_a, Because of this resonance, V_{dsA1} and V_{dsA2} reach $V_{dc}/2$ and V_{dsA3} and V_{dsA4} reach 0, the body diodes of S_{A3} and S_{A4} start conducting and the switches can be turned on at 0 V. After the body diodes start conducting, i_a starts to drop. The equivalent circuit is shown in Fig. 5.7, the phase currents' slopes are given by:

$$di_a / dt = (-V_{dc} / 6 - v_a) / L \tag{97a}$$

$$di_b / dt = (-V_{dc} / 6 - v_b) / L \tag{97b}$$

$$di_c / dt = (V_{dc} / 3 - v_c) / L \tag{97c}$$

The peak currents are given by:

$$i_{bp3} = i_{bp2} + \frac{(-V_{dc} / 6 - v_b)}{L} T_3 \tag{98a}$$

$$i_{cp3} = i_{cp2} + \frac{(V_{dc} / 3 - v_c)}{L} T_3 \tag{98b}$$

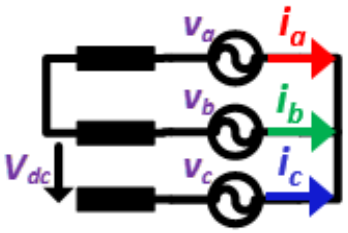


Figure 5. 7 Equivalent circuit in Interval III

Interval III ends when current i_a reaches 0, phase B and C continue to conduct current.

Interval IV (T_1+T_2+T_3 - T_1+T_2+T_3+T_4)

During interval IV, S_{B3}, S_{B4}, S_{C2} and S_{C3} continue to conduct leading to fall in i_c and rise in i_b. the equivalent circuit is shown in Fig.5.8, the phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (-V_{dc} / 2 + v_c - v_b) / 2L \tag{99}$$

This interval ends when i_c reaches 0.

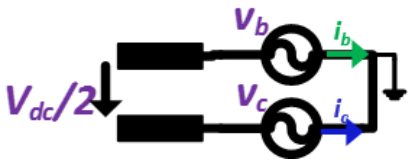


Figure 5. 8 Equivalent circuit in Interval IV

Interval V (T_1+ T_2+ T_3+T_4- T_1+ T_2+ T_3+T_4+T_5)

After i_c reaches 0, S_{C2} is allowed to conduct for a little more time till i_c reaches a negative value I_R which is enough to discharge the phase C devices' output source capacitors for ZVS turn-on of S_{C1}. The equivalent circuit is the same as in Interval IV. At the end of this interval, S_{C3} is turned off. The peak negative current I_R is given by:

$$I_R = \frac{-(-V_{dc}/2 + v_c - v_b)T_5}{2L} \tag{100}$$

Interval VI (T_1+ T_2+ T_3+T_4+ T_5 - T_1+ T_2+ T_3+T_4+ T_5+T_6)

After S_{C3} is turned off, resonance occurs in between phase C devices' output source capacitors and L_c, thus V_{dsC3} reaches V_{dc} and V_{dsC1} reaches 0, the body diode of S_{C1} starts conducting (as i_c<0) and the switch is turned on at 0 V. The equivalent circuit after is shown in Fig. 5.5. The phase currents' slopes are given by Eq. 93.

The peak negative current I_R is given by:

$$I_R = -\frac{(V_{dc} + v_b - v_c)T_6}{2L} \tag{101}$$

Thus, i_c starts to increase again and this interval ends when i_c and i_b touch zero and a new switching cycle starts from there.

The calculated switching times for ideal devices neglecting the effect of C_{oss} and dead times are shown in Fig. 5.9. T_5 and T_6 are calculated from (100) and (101) and are given by:

$$T_5 = \frac{2I_R L}{-(-V_{dc}/2 + v_c - v_b)} \tag{102a}$$

$$T_6 = \frac{-2I_R L}{(V_{dc} + v_b - v_c)} \tag{102b}$$

T_3 and T_4 can be derived in terms of T_1 and T_2 derived from the following equations:

$$i_{ap1} + \frac{1}{L}(-V_{dc}/6 - v_a)T_3 = 0 \tag{105a}$$

$$i_{bp3} + \frac{1}{L}\frac{(-V_{dc}/2 + v_c - v_b)}{2}T_4 = 0 \tag{105b}$$

Where i_{ap1} and i_{bp3} are derived using Eqns. (94), (96) and (98). Thus T_1 and T_2 can be derived from average current equations:

$$i_{aavg} = \frac{i_{ap1}\dfrac{(T_2 + T_3)}{2}}{\sum_{i\in 1-6} T_i} = k_1 v_a \tag{104a}$$

$$i_{bavg} = \frac{i_{bp1}\dfrac{T_1}{2} + (i_{bp1} + i_{bp2})\dfrac{T_2}{2} + (i_{bp2} + i_{bp3})\dfrac{T_3}{2}}{\sum_{i\in 1-6} T_i} + \frac{i_{bp3}\dfrac{T_4}{2} - I_R(\dfrac{T_5 + T_6}{2})}{\sum_{i\in 1-6} T_i} = k_1 v_b \tag{104b}$$

Where k_1 is given by Eqs. (51) and (52).

T_1 and T_2 are given by:

$$T_1 = \frac{-2Lk_1(2v_b + v_a)}{V_{dc} + 2v_b + v_a} \tag{105}$$

The switching times for a 5 kW, 900 V V_{dc}, 480 V_{llrms}, f_s~ 0.1MHz, L= 36 µH are shown in Fig. 5.9. The inductance is chosen to obtain the desired switching frequency.

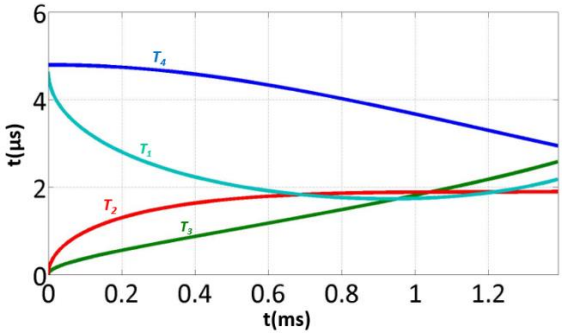


Figure 5. 9 Switching times 5 kW P_o, 900 V V_{dc}, 480 V_{llrms}, f_s~ 0.1MHz, L- 36 µH

The decision of mode of operation for each phase follows the same relationship as in unity power factor for a two-level inverter. The full line cycle control is shown in Fig. 5.10.

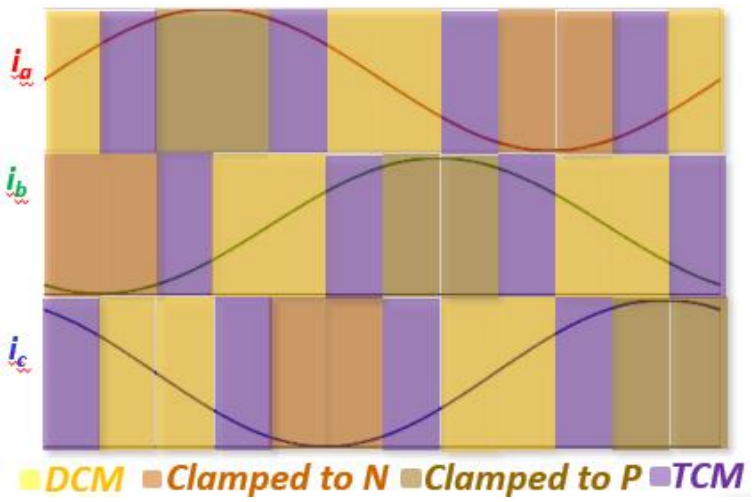


Figure 5. 10 Full line cycle control showing control symmetry after every 30^o

The switching frequency variation for 0-60^o is shown in Fig. 5.11. The graph is symmetrical after every 30^o. The switching frequency variation is just 6 % as compared to >2* variation in state-of-the-art decoupled TCM. The CMV variation for one switching cycle is shown in Fig. 5.12. The maximum CMV is $|V_{dc}/3|$ while for two-level TCM the maximum CMV is $|V_{dc}/2|$ (as shown in Fig. 5.4).

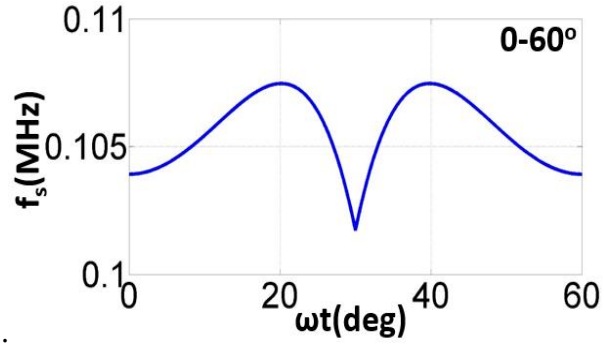


Figure 5. 11 Switching frequency variation for 5 kW P_o, 900 V V_{dc}, 480 V_{llrms}, f_s~ 0.1MHz, L- 36 µH

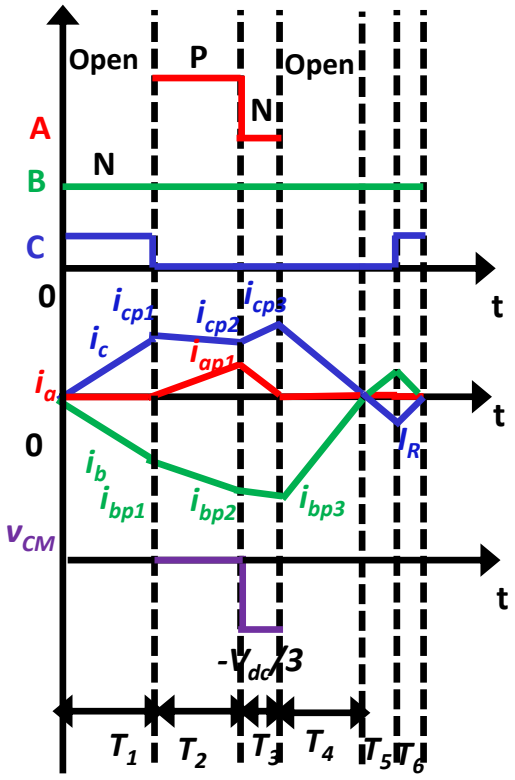


Figure 5. 12 Switching sequence and CMV in proposed 3-level TCM

5.2.2 Verification by Simulation

The converter is simulated from pre-calculated switching times (T_1, T_2, T_3, T_5 and T_6) and zero crossing detection (ZCD) of current of clamped phase. The simulated phase currents for 5 kW P_o, 900 V V_{dc}, 480 V V_{acl}, L~ 36 µH are shown in Fig. 5.13, ideal devices are considered in this simulation. The zoomed in current waveforms in sector I are shown in sector I is shown in Fig. 5.14. The closed loop implementation is very similar to the closed loop implementation for two-level TCM discussed in Chapter 3 in Fig. 3.38. The compensator for phase in TCM now generates switching time T_1 and the compensator for phase in DCM generates switching time T_2.

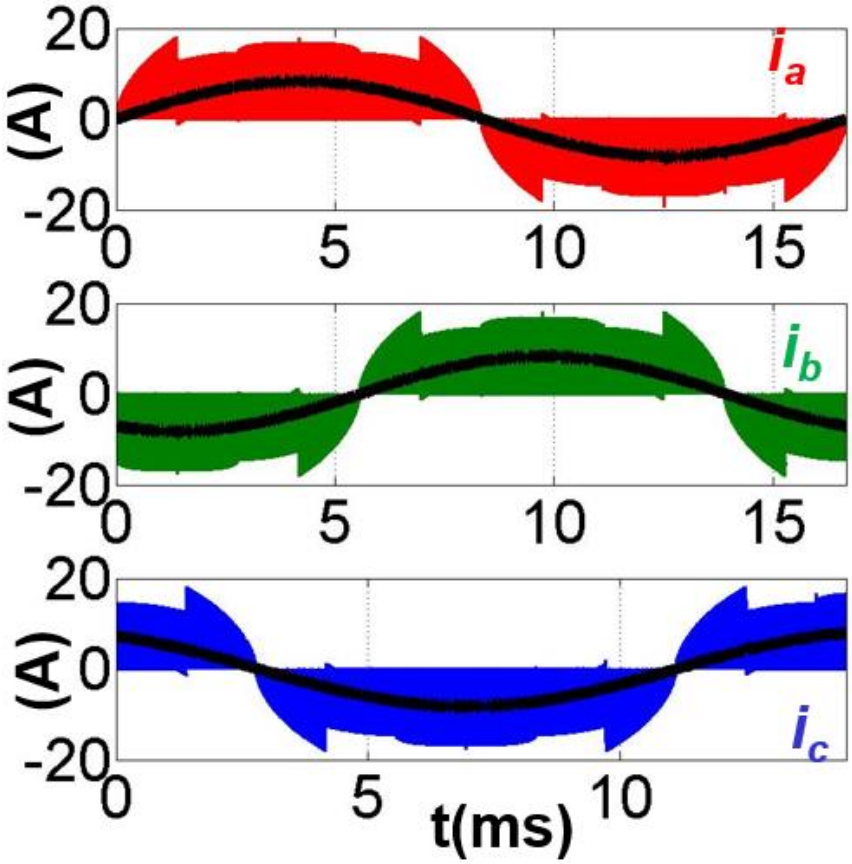


Figure 5. 13 Simulated phase currents for 5 KW P_o, 900 V V_{dc}, 480 V V_{acl}, L~ 36 µH

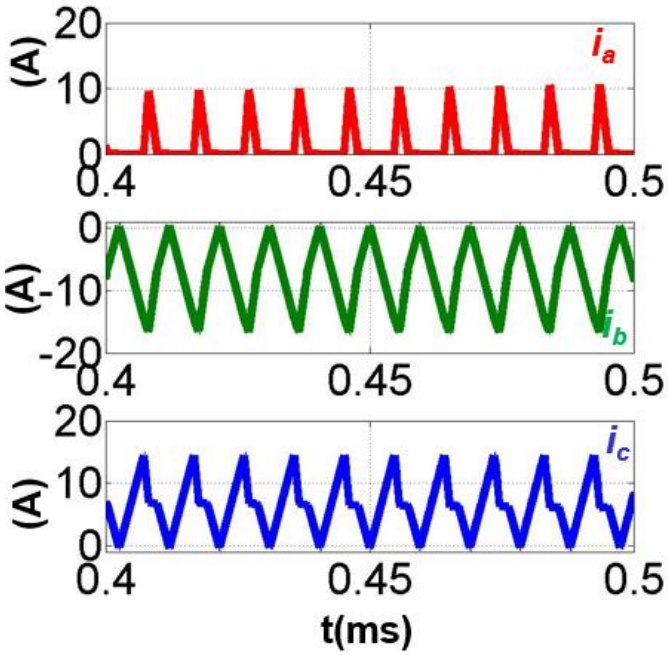
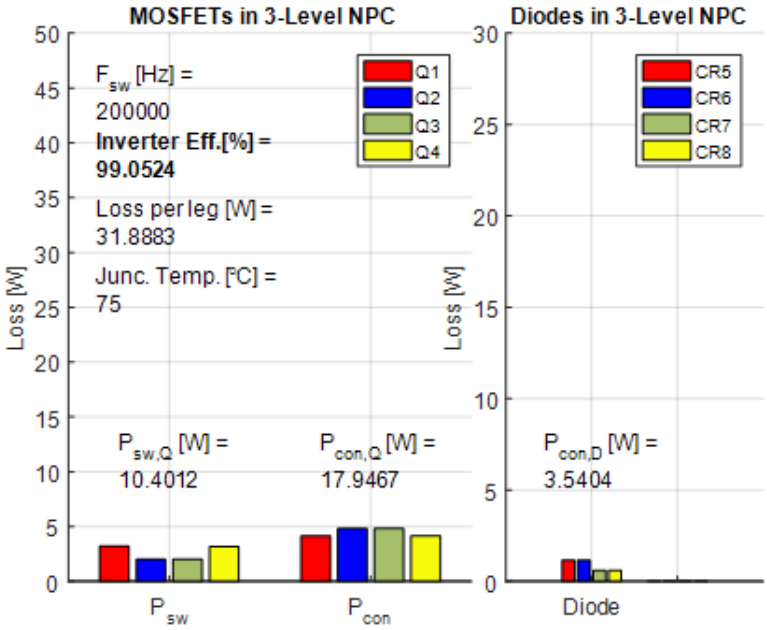


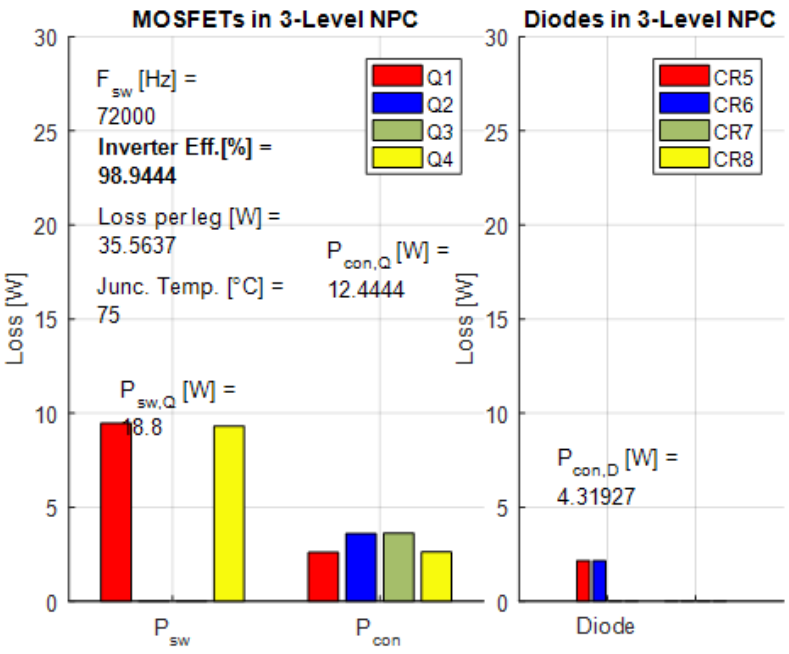
Figure 5. 14 Zoom in current waveforms in Sector I

The loss comparison between hard switched Space Vector Pulse Width Modulation (SVPWM) and proposed algorithm for 10 kW P_o, 900 V V_{dc}, 480 V V_{acl} is shown in Fig. 5.15. It

can be seen that the proposed switching sequence can achieve >99 % efficiency at 200 KHz switching frequency while with SVPWM ~99% efficiency is achieved at 72 kHz. Thus, a great reduction in filter size is achieved while maintaining same efficiency.



(a)



(b)

Figure 5. 15 Loss Comparison between (a) TCM and (b)SVPWM and TCM for 10 KW P_o, 900 V V_{dc}, 480 V V_{acl}, L~ 9 µH for TCM and L~ 140 µH for hard switched SVPWM

5.2.3 Control Implementation

The implementation is very similar to the implementation of two-level average current control, two compensators are used for controlling two average currents. The closed loop implementation from 0-30^{o} is shown in Fig. 5.16, phase A compensator generates T_2 while phase C compensator generates T_1. The phases operating in DCM and TCM modes of operation keeps rotating as shown in Fig. 5.10.

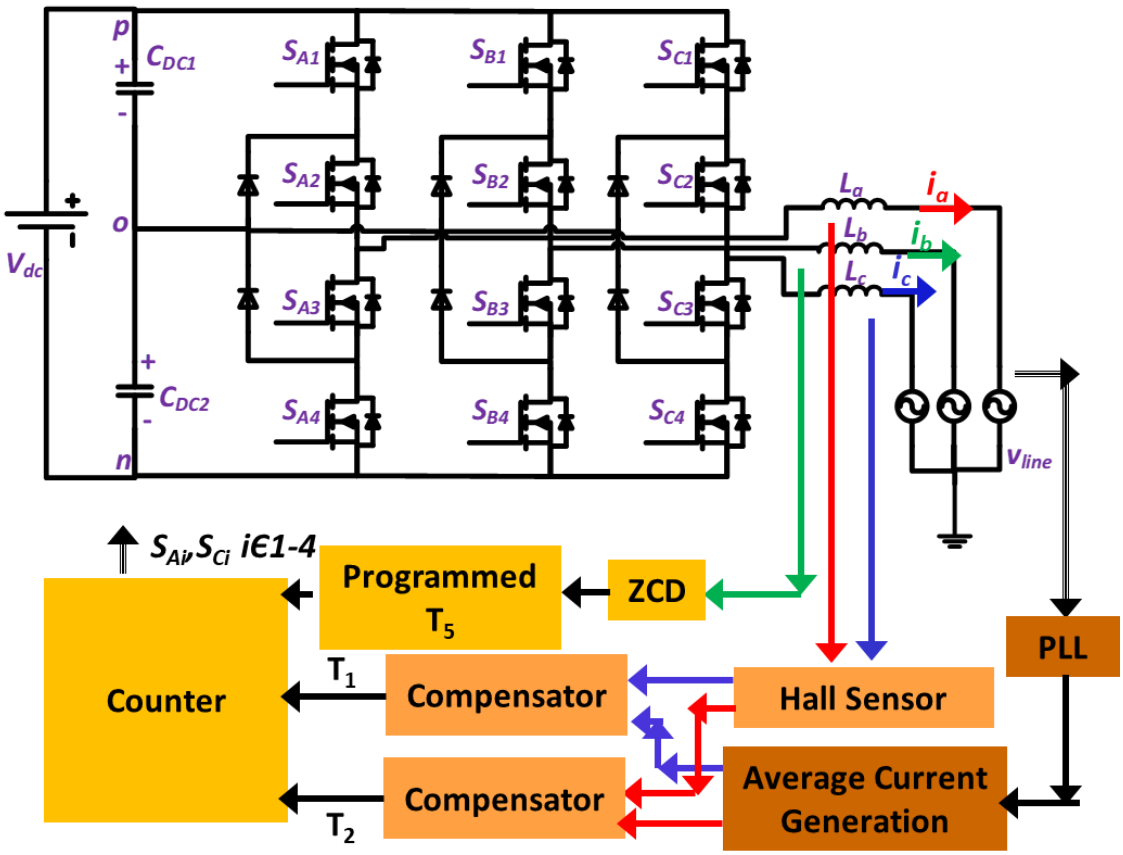


Figure 5. 16 Control Closed Loop Implementation from 0-30^o.

Proposed implementation is verified by simulation, the simulation results for 5 kW P_o, 900 V V_{dc}, 480 V_{llrms}, f_s~ 0.1MHz, L= 36 µH is shown in Fig.5.17.

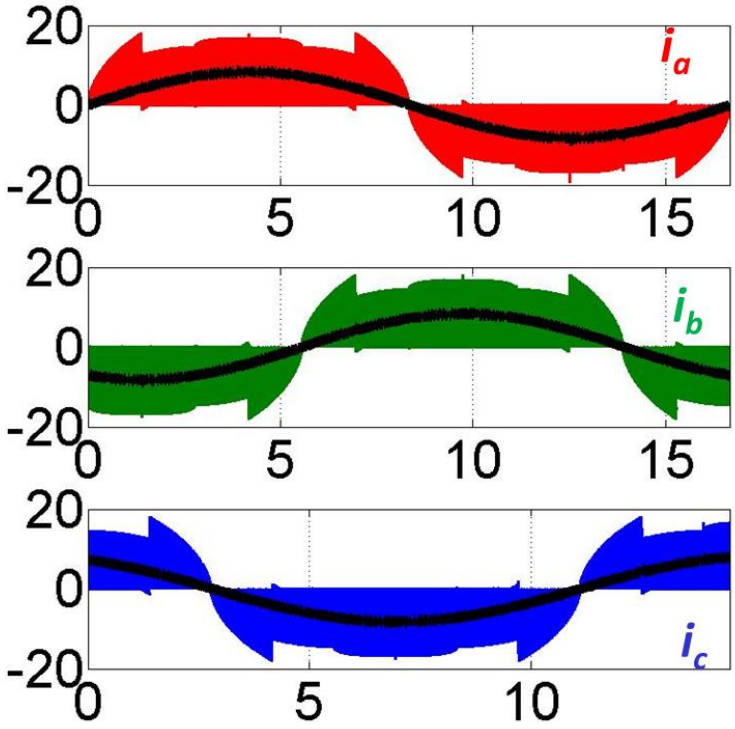
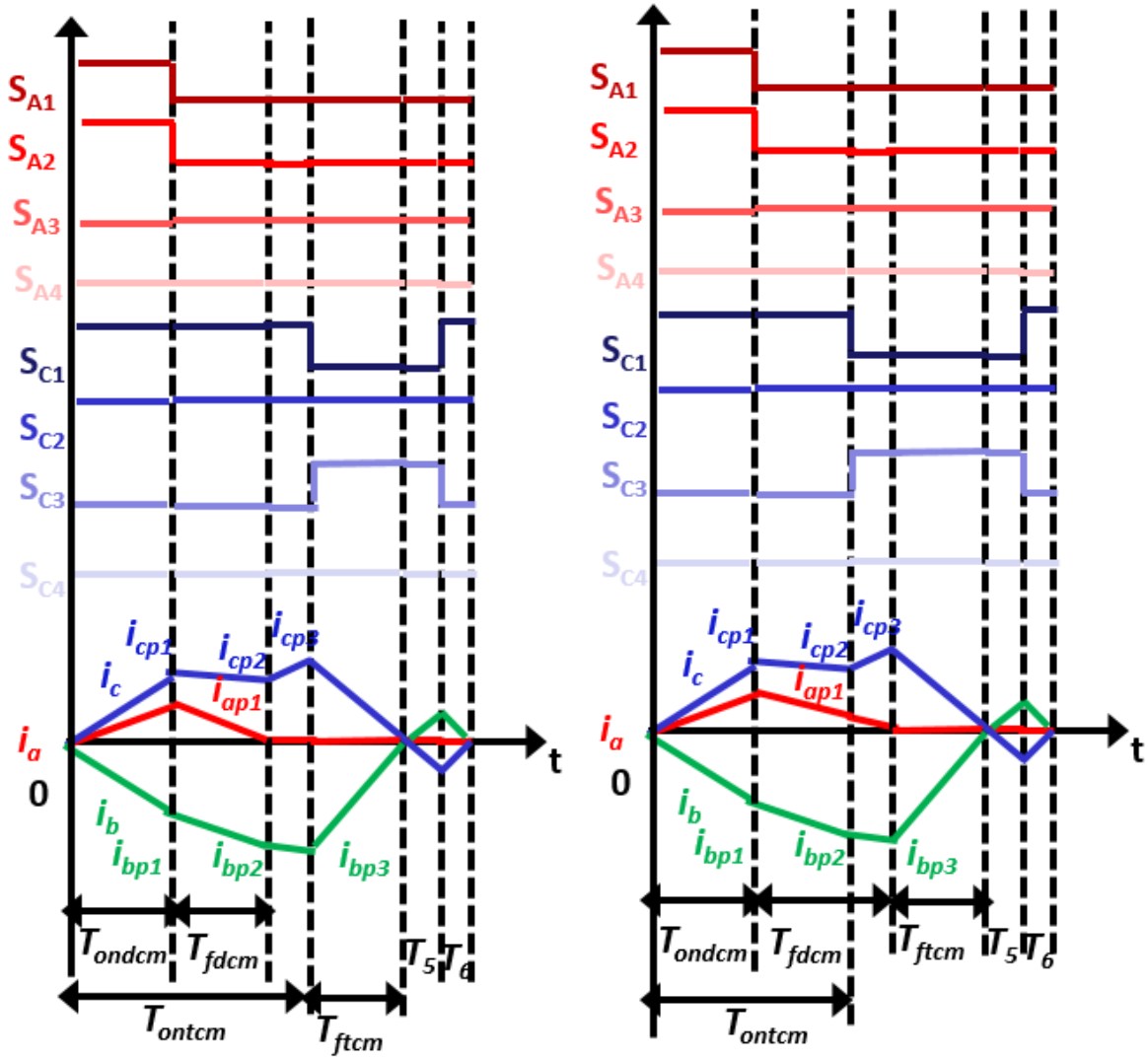


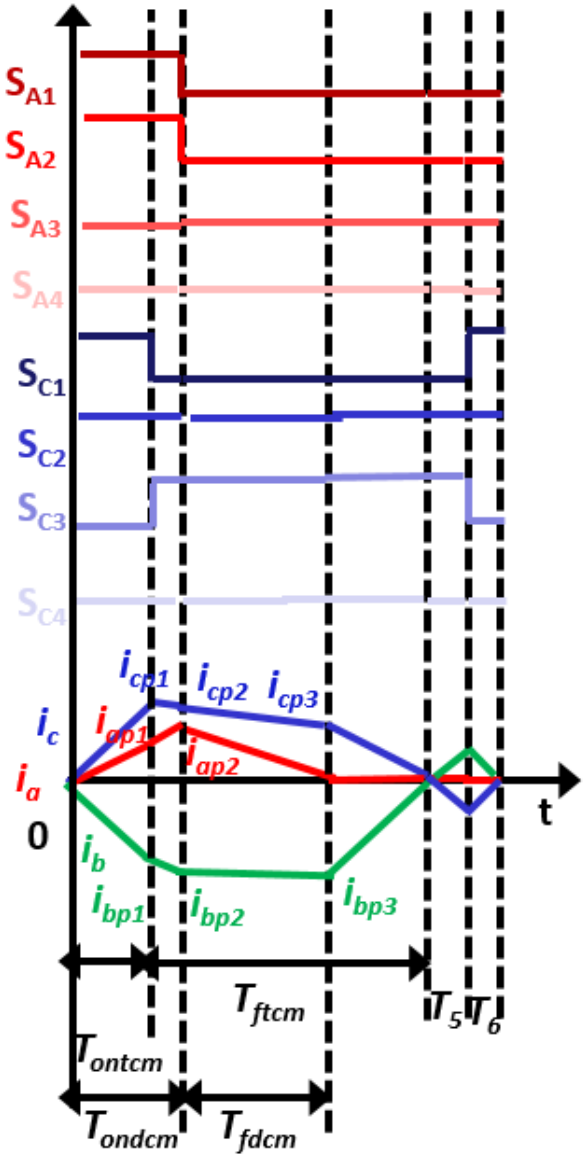
Figure 5. 17 Simulated phase currents from proposed implementation for 5 kW P_o, 900 V V_{dc}, 480 V_{aclrms}, f_s~ 0.1MHz, L- 36 µH for sequence I.

5.3 Reduced CMV Switching Sequence II

In switching sequence I, the DCM phase is turned on after the TCM phase (after time T_1). In the second switching sequence proposed, the DCM and TCM phases are turned on at the same time in the beginning of every switching cycle like for a two-level inverter or rectifier unity power factor mode of operation. As discussed for two-level inverter TCM switching sequence, it can be divided in two cases, similarly the proposed switching sequence for three level inverter can be divided into three cases. The switching cycle waveforms in sector I ($0<\omega t<\pi/6$) for case A, B and C are shown in Figs. 5.18 (a), (b) and (c) respectively.


S_A1
S_A2
S_A3
S_A4
S_C1
S_C2
S_C3
S_C4
i_cp1
i_cp2
i_cp3
i_c
i_ap1
i_a
0
t
i_b
i_bp1
i_bp2
i_bp3
T_ondcm
T_fdcm
T_ftcm
T_5
T_6
T_ontcm

(a) (b)



(c)

Figure 5. 18 One switching cycle waveform for TCM in Sector I for (a) Case A: $T_{ontcm}>T_{ondcm}+T_{fdcm}$ (b) Case B: $T_{ontcm}<T_{ondcm}+T_{fdcm}$ and (c) Case C: $T_{ontcm}<T_{ondcm}$

The time for which phase A devices S_{A1} and S_{A2} conduct is termed as on-time for phase operating in DCM (T_{ondcm}) and after these devices are turned off, the time taken by i_a to decrease to zero is called the fall time of DCM phase (T_{fdcm}) as shown in Fig. 5.18. Similarly, the time for which the phase C device S_{C1} conducts, i.e. phase C is connected to P is termed as on-time for phase operating in TCM (T_{ontcm}) and after S_{C1} is turned off, the taken by i_c to decrease to zero is called the fall time of TCM phase (T_{ftcm}) as shown in Fig. 5.18. These terms are defined for clear

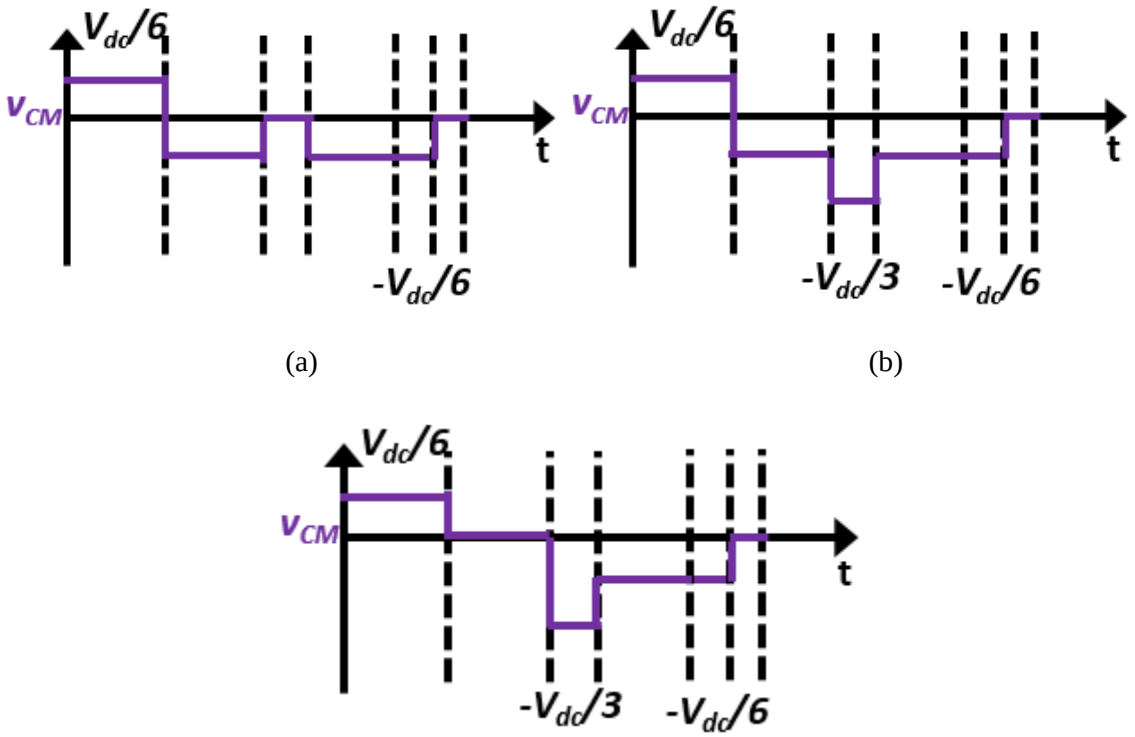
understanding of this switching sequence. B phase, i.e., the phase with the maximum magnitude of average current (as shown in Fig. 5.10) is still clamped. The switching sequences in the three cases are given by:

Case A: P-N-P|N-N-P|N-P|N-O|N-O|N-P

Case B: P-N-P|N-N-P|N-N-O|N-O|N-O|N-P

Case C: P-N-P|P-N-O|N-N-O|N-O|N-O|N-P

The CMV for all the three cases is shown in Fig. 5.19, it can be seen that the maximum magnitude of the CMV is always less than $V_{dc}/3$.



(a) (b)

(c)

Figure 5. 19 CMV variation during one switching cycle for TCM in Sector I for (a) Case A: $T_{ontcm}>T_{ondcm}+T_{fdcm}$ (b) Case B: $T_{ontcm}<T_{ondcm}+T_{fdcm}$ and (c) Case C: $T_{ontcm}<T_{ondcm}$

5.3.1 Mathematical Model

Based on the circuit equations in each time interval, the switching times are calculated, T_{ondcm} and T_{ontcm} are shown in Fig. 5.20. The switching frequency variation for 5 kW P_o, 900 V V_{dc}, 480

V_{llrms}, f_s~ 0.1MHz, L= 36 µH is shown in Fig. 5.21. It can be seen that both the on times vary similar to the two-level inverter on times. Hence the controller implementation is very similar.

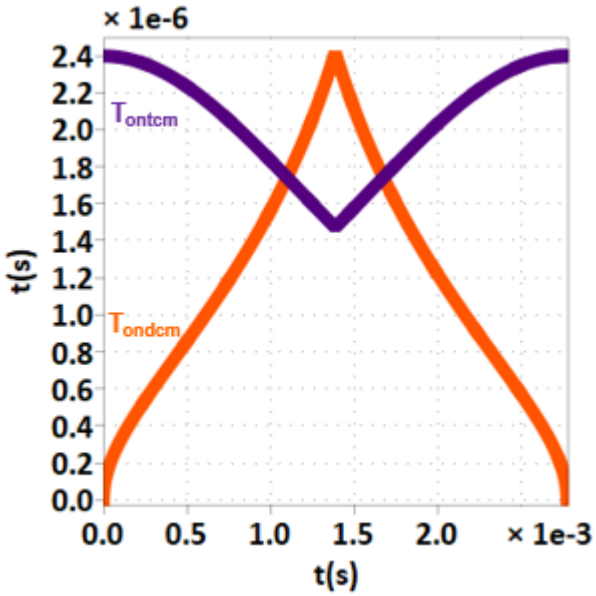


Figure 5. 20 DCM and TCM phase on times

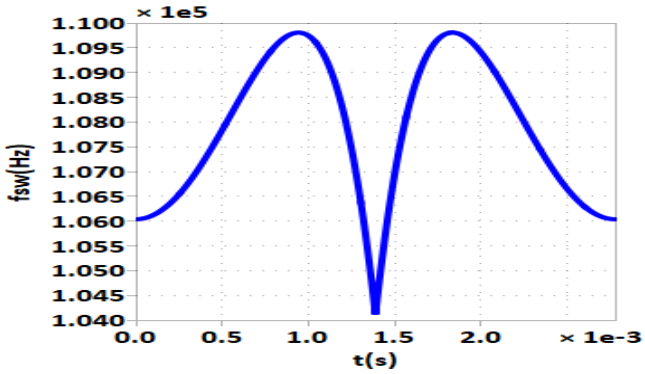


Figure 5. 21 Switching frequency variation for 5 kW P_o, 900 V V_{dc}, 480 V_{aclrms}, f_s~ 0.1MHz, L- 36 µH for sequence II

5.3.2 Control Implementation

The implementation is very similar to the implementation of previous switching sequences, average current control is employed, two compensators are used for controlling two average currents. The closed loop implementation from 0-30^o is shown in Fig. 5.22, phase A compensator generates T_{ondcm} while phase C compensator generates T_{ontcm}. The phases operating in DCM and TCM modes of operation keep rotating as shown in Fig. 5.10.

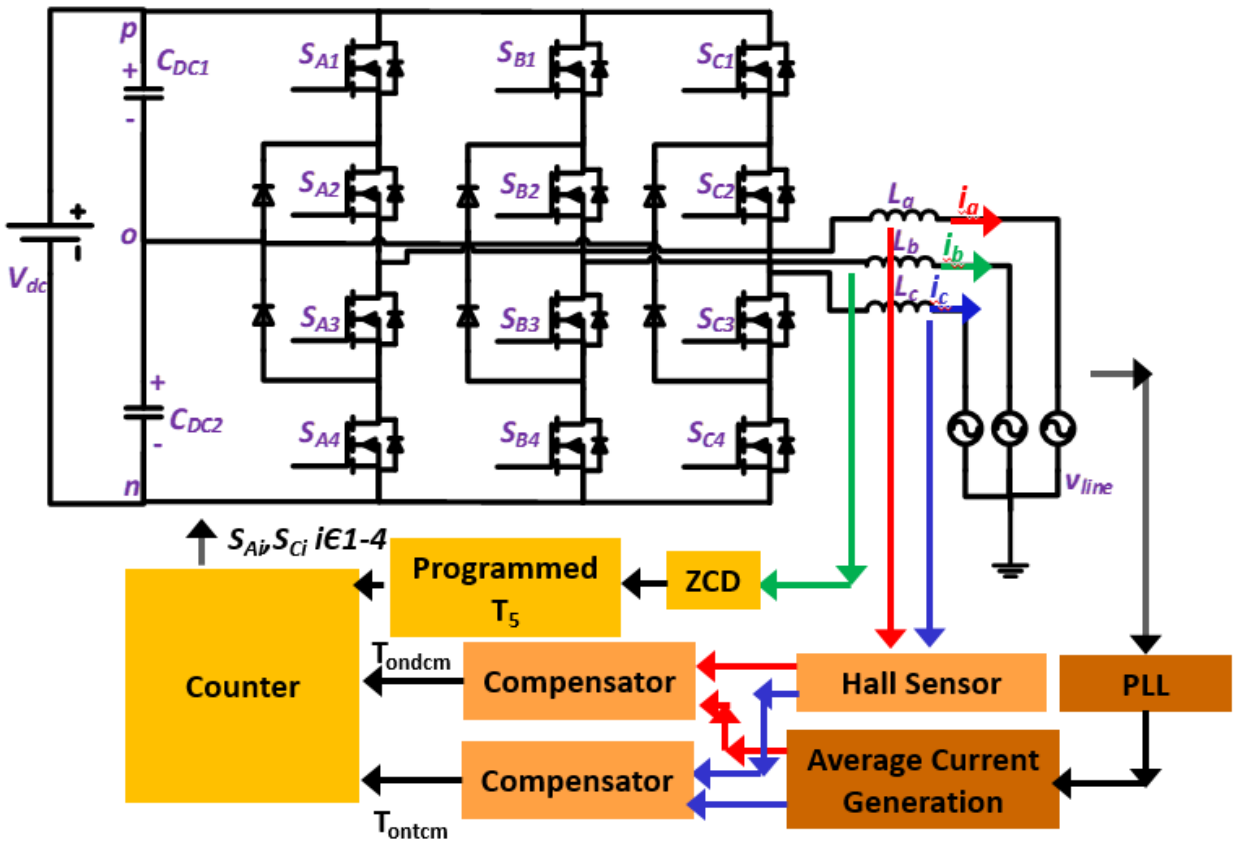


Figure 5. 22 Closed loop control implementation from 0-30° where phase A operates in DCM and phase C operates in TCM

5.3.3 Verification by Simulation

The simulated phase currents are shown in Fig. 5.23. The zoom in current waveforms in sector I are shown in Fig. 5.24. It can be seen that ZVS turn-on is achieved for the phase operating in TCM. The peak ripple is very similar to sequence I, however the current envelope is different. Also, the zoom in waveforms show difference in the two sequences.

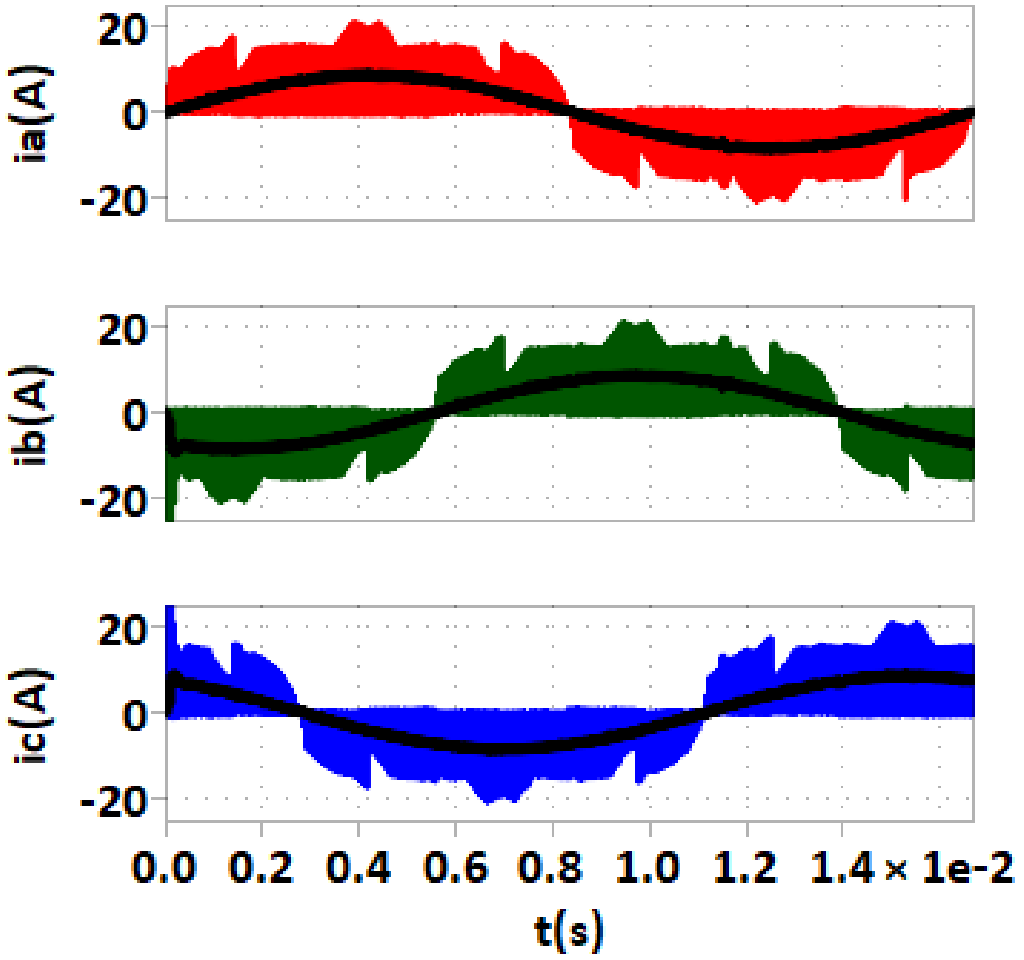
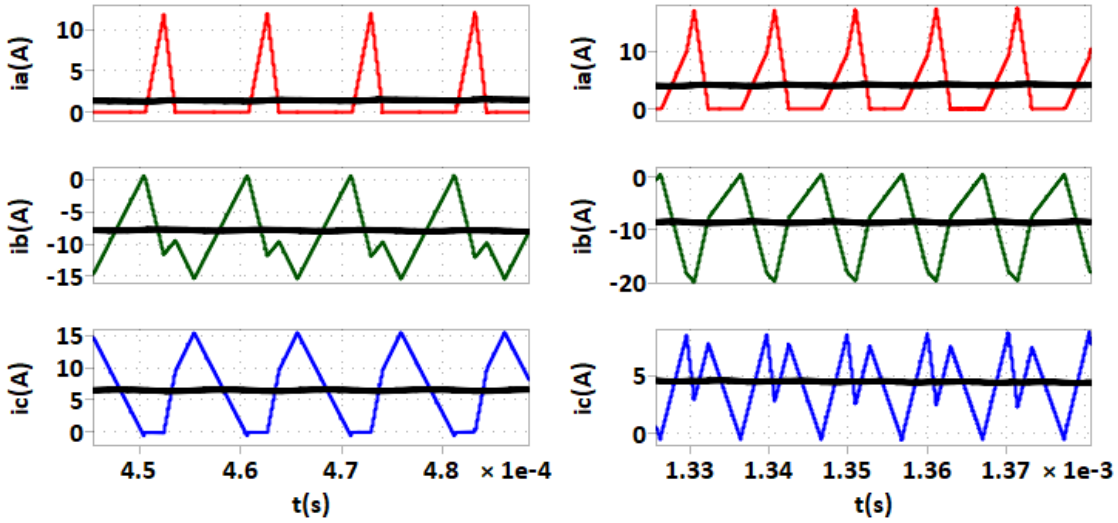


Figure 5. 23 Simulated phase currents for 5 KW P_o, 900 V V_{dc}, 480 V V_{acl}, L~ 36 µH for sequence II



(a) (b)

Figure 5. 24 Zoom in current waveforms in Sector I for sequence II

5.4 Experimental Verification

The switching sequence I is tested on an NPC inverter, the NPC module is rated for 1.2 kV, 40 A. The switching times are generated from DSP and then fed into CPLD as shown in Fig. 5.15. The CPLD resets the counter shown in Fig. 5.23 and counts the time till the end of each switching interval and resets the counter to zero after every ZCD. This implementation is different from complete DSP implementation discussed in previous chapters.

The low power testing results at 625 W P_o, 225 V V_{dc}, 120 V_{aclrms}, f_s~ 0.1MHz, L= 9 µH for sequence I are shown in Fig. 5.24. The zoom in waveforms for phase A operating in DCM and TCM are shown in Fig. 5.24 (b) and (c) respectively. It can be seen from Fig. 5.24(c) that ZVS turn-on is achieved for TCM phase. Also, the small ripple resulting from resonance between L_a and phase A device output source capacitors can be seen in Fig. 5.24 (b). The average currents are not perfectly sinusoidal as can be seen from Fig. 5.24 (a), the compensator design for DCM and TCM phase needs to be improved which is a good future research problem.

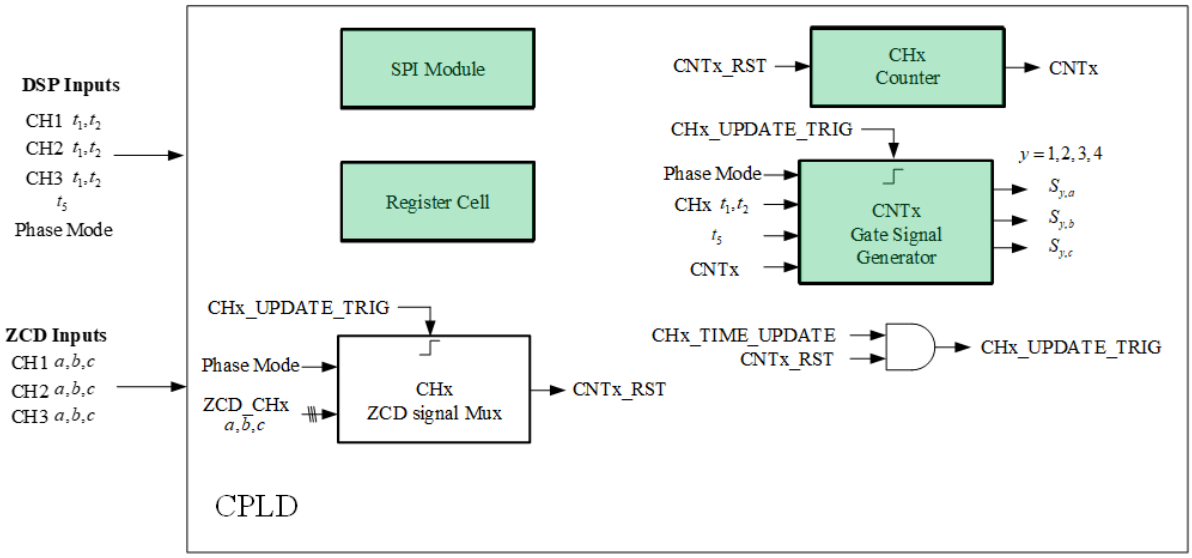
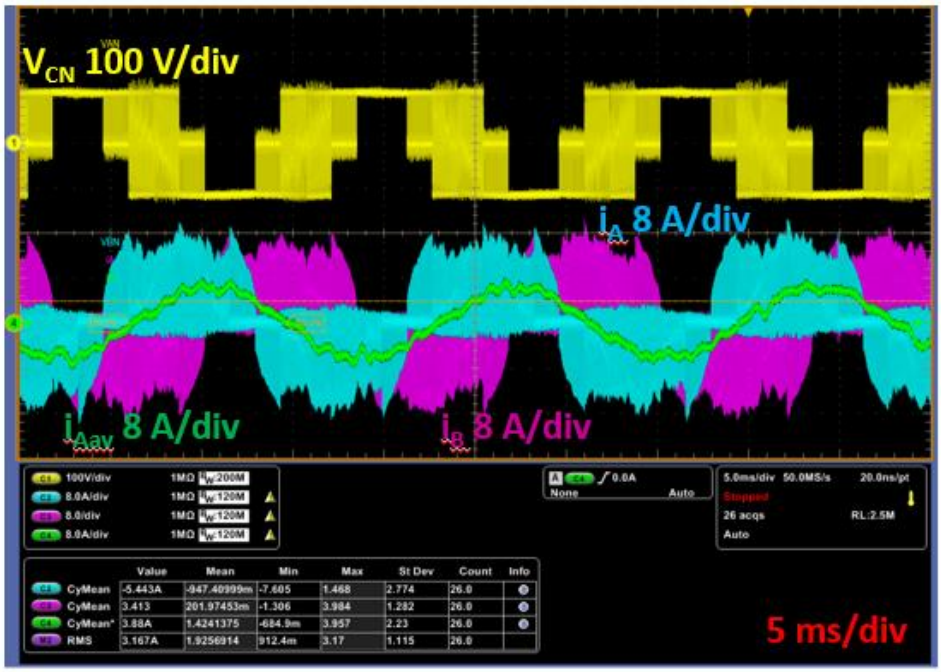
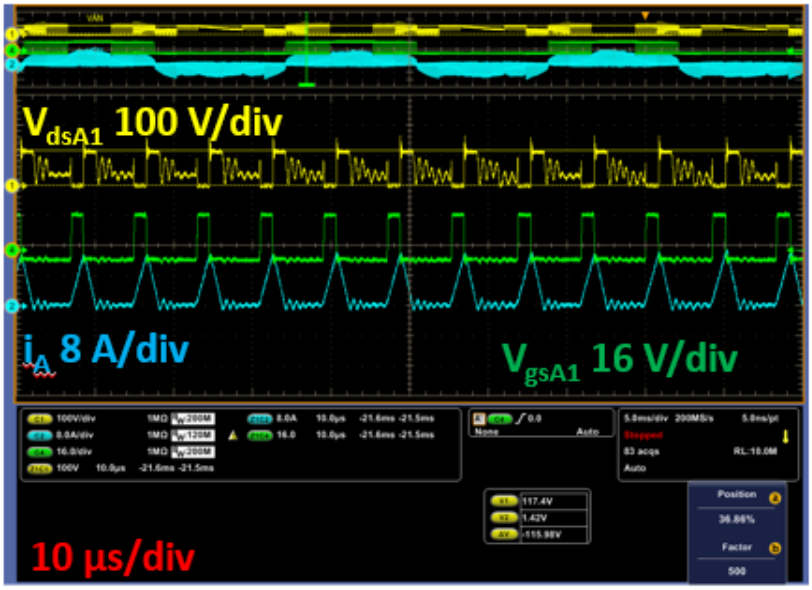


Figure 5. 25 DSP+CPLD block diagram



(a)



(b)

(c)

Figure 5. 26 Experimental Results at 625 W P_o, 225 V V_{dc}, 120 V V_{aclrms}, L= 9 µH (a) Full Line cycle currents and line-neutral voltage (b) Phase A operating in DCM (c) Phase A operating in TCM

5.5 Summary

In this chapter, DCM+TCM+Clamped algorithm is extended to three-level converters. The proposed switching sequences employ the benefit of reduced CMV switching states of three-level

topology. The switching sequences are designed such that the phase operating in TCM mode switches between P and O or N and O state. This limits the maximum CMV to $|V_{dc}/3|$, whereas, the maximum CMV in two-level TCM is $|V_{dc}/2|$. These sequences are generic to three-level topologies, i.e. the algorithm can be implemented on a T-type converter also without any modification.

The switching frequency variation is very small (6%) for both the switching sequences as compared to >2* variation in state-of-the-art decoupled TCM. The implementation is similar to the two-level algorithm, two switching times are generated by two average current controllers and the compensator design is also similar to that of the two-level algorithm. The phase with maximum magnitude of current is still clamped.

This algorithm is tested on a three-level NPC inverter and the converter density increases 6* as compared to state-of-the-art three-level NPC converter switching in hard switched CCM.

Chapter 6. Conclusion and Future Work

6.1 Summary

High switching frequency operation leads to a great reduction in the power converter size, WBG devices enable high switching frequency operation owing to their fast switching speed, small size, and low switching noise and hence, reduced switching losses. The turn-on losses are still significant (as shown in Appendix A) though for > 0.3 MHz switching frequency operation making soft turn-on necessary for efficient high frequency operation. ZVS turn-on can be achieved by adding a resonant tank to the converter but that increases the physical complexity of the converter. Hence, methods that achieve ZVS turn-on by modification of control techniques are investigated.

State-of-the-art critical conduction mode and triangular current mode control are discussed in Chapter 1. In these techniques, phase inductor and device capacitors form the resonant tank. TCM for single-phase PFC has >2* switching frequency variation, phase decoupled TCM for three-phase converters results in the three phases operating at different switching frequencies simultaneously.

Hence, TCM+DCM+Clamped algorithm is proposed to achieve ZVS turn-on with phase synchronization in Chapter 3. Each switching cycle has six switching states and two independent switching times. These switching times are controlled such that the average three-phase currents are sinusoidal. It is shown that the proposed algorithm leads to only 34% switching frequency variation. The phase with maximum current magnitude is clamped minimizing the turn-off losses. The DCM phase also operates with ZVS turn-on, the existing methods have only focused on TCM phase ZVS turn-on and valley switching turn-on for DCM phase. The implementation is highly simplified by incorporating average current control. DSP implementation with just one CPU is showed. The algorithm is validated on a GaN converter, the converter's density is pushed to 110

W/in^3 while maintaining ~99 % efficiency at 300 V V_{dc}, 0.675 kW and ~0.5 MHz switching frequency.

The discussion of CRM/TCM in existing literature is limited to unity power factor assumption which limits the algorithm's adoption in real world applications, the proposed algorithm of TCM+DCM+Clamped is thus extended to reactive power cases in Chapter 4. The algorithm is able to achieve phase shifted sinusoidal currents, each switching cycle is still divided into six switching states, two independent switching times are controlled to generate three-phase sinusoidal currents. It is discussed when phase with the maximum average current is clamped, it leads to uncontrolled current flowing in the DCM phase which ultimately leads to instability. Hence, phase with maximum voltage magnitude is clamped and it is concluded that the optimal range of phase shift for the proposed algorithm is -30^o-30^o. A general algorithm is shown for this phase shift. The algorithm is implemented with average current control. It is validated on the GaN converter and the converter's density is pushed to 110 W/in^3 while maintaining ~99 % efficiency at 300 V V_{dc}, 0.675 kVA, 30^o phase lag and 0.6-0.85 MHz switching frequency.

The proposed algorithm is also extended to three-level converters in Chapter 5 employing the benefit of reduced CMV switching states in three-level topologies. Two switching sequences are proposed, both the sequences have six switching states, and two independent switching times are controlled to generate three-phase sinusoidal currents. The TCM phase switches between N and O or P and O switching states in one switching cycle leading to a reduction of maximum CMV to $|V_{dc}/3|$ as compared to $|V_{dc}/2|$ in two-level TCM. Both the proposed switching sequences have a very small (6%) switching frequency variation as compared to >2* variation in state-of-the-art decoupled TCM. The implementation is similar to that of the two-level TCM+DCM+Clamped algorithm. The experimental verification with a three-level NPC inverter is shown, the inverter's density is pushed 3* as compared to the hard switched CCM NPC inverter.

6.2 Future Work

In the future, it would be an important research problem to conduct detailed study of controller design for the TCM+DCM+Clamped algorithm implementation. Also, the transient performance of the controller needs to be studied. Also, for reactive power generation, the compensator design needs to be studied in detail owing to asymmetry in phase shifted operation. It would be an important problem to study a general compensator design for the whole range of phase shift. For the three-level algorithm, it would be a good research problem to study TCM switching sequences that do not cause mid-point voltage imbalance. Also, a detailed controller design is required to improve the quality of phase currents.

APPENDIX A

GaN Static and Dynamic Characterization

As discussed in Chapter 1, converters operating in high frequency TCM operation do have high current ripple passing through the devices, the converter should be able to operate efficiently with such a high ripple current too. Wide Bandgap devices are a promising candidate for this design owing to their low conduction losses. Wide band-gap GaN-based devices are emerging as an attractive candidate for high-efficiency power driving systems ([A.12]-[A.15], [A.26]) owing to their high breakdown voltage, low on-resistance, fast switching, and high temperature operation.

As shown in Fig. A.1, the theoretical limit of GaN breakdown voltage is very high with very low specific on-resistance. The 600 V cascode GaN-on-Si structure has been dominant in medium power applications for a long time but the cascode structure has issues of charge imbalance between the low voltage Si and high voltage normally-on GaN, lower reliability and high common source inductance [A.19].

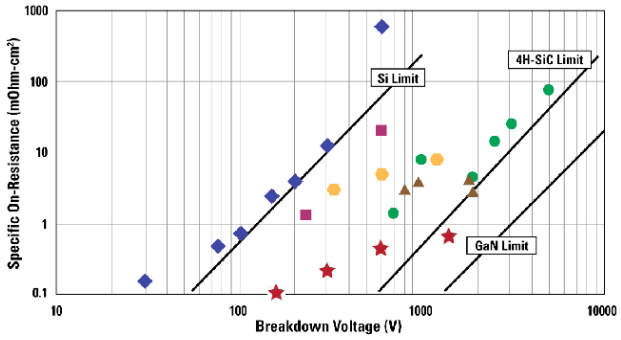


Figure A. 1 Specific on-resistance vs breakdown voltage for different semiconductor materials showing that the theoretical limit for GaN is the highest

The 650 V e-mode GaN devices are very small (as shown in Fig. A.2) and have low package inductance but to extract the full benefits of these devices, it is important to analyze the static and dynamic characteristics of the device. A detailed device characterization to study the variation of the parameters (R_{dson}, C_{oss} etc.) with junction temperature, applied voltage and current is done to

model the device's performance in TCM mode converters. First, the static characterization of the device is discussed at both low temperature and high temperatures. Later, dynamic characterization is discussed with two phase leg designs: reference lateral phase leg design and vertical phase leg design.

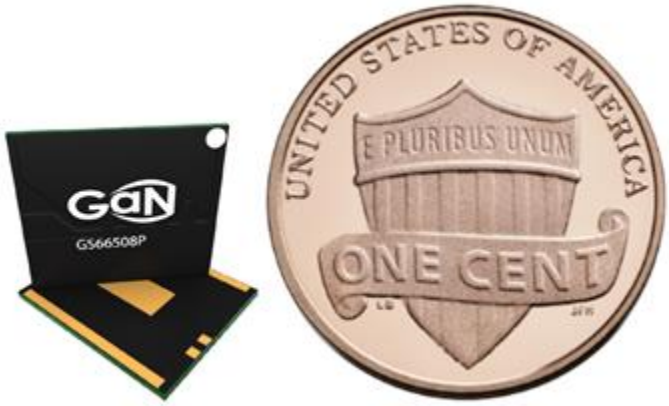


Figure A. 2 650V/ 30 A GaN device from GaN Systems with very low package inductance and small package size

A.1 Static Characterization

An ideal power device should act as short circuit when on and open circuit when the device is off but an actual power device has several parasitics as shown in Fig. A.3. The device static characteristics include the device drain-source resistance (R_{dson}) which increases with temperature and drain current. The equivalent gate circuit of a power MOSFET shown in Fig. A.3 shows device parasitic capacitors and package inductances. The device has a surface mount device (SMD) package with gate and source inductances less than 0.7 nH. The parasitic parameters are studied in detail with static characterization. In order to gain a deep insight of the device switching and thermal performance, it is important to measure each parasitic element accurately.

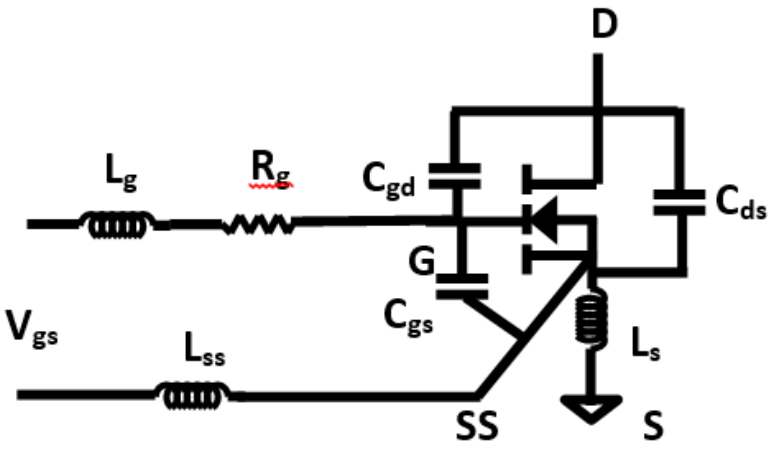


Figure A. 3 Equivalent circuit of a power MOSFET

A.1.1 Characterization Procedure

The parasitic on-resistance (R_{dson}) varies with drain current (I_d) and device junction temperature (T_j). The on-resistance also changes with the gate source voltage (V_{gs}) applied on the device as the enhancement mode operation requires a minimum positive gate-source voltage on the device. On-resistance is measured during enhancement mode of the device as in most power electronics application the MOSFET is operated in linear mode to minimize the parasitic resistance.

The parasitic capacitances namely gate-source capacitance (C_{gs}), drain source capacitance (C_{ds}) and gate-drain capacitance (C_{gd}) as shown in Fig. A.3 depend on the drain-source voltage V_{ds}. The static characterization was performed using a curve tracer (Agilent B1505A) as shown in Fig. A.4. The tests which need a high current capability (>1 A) like the output characteristics, transfer characteristics etc. were done by connecting the curve tracer to an ultrahigh current expander (Agilent N1256A). The tests which needed a higher voltage (> 60 V) such as capacitance measurement were done by connecting the curve tracer to a high voltage bias tee (Agilent N1260A). The bias tee can be used for testing up to 3 kV. The device is mounted on the socket with gate, source and drain connections as shown in Fig. A.5.

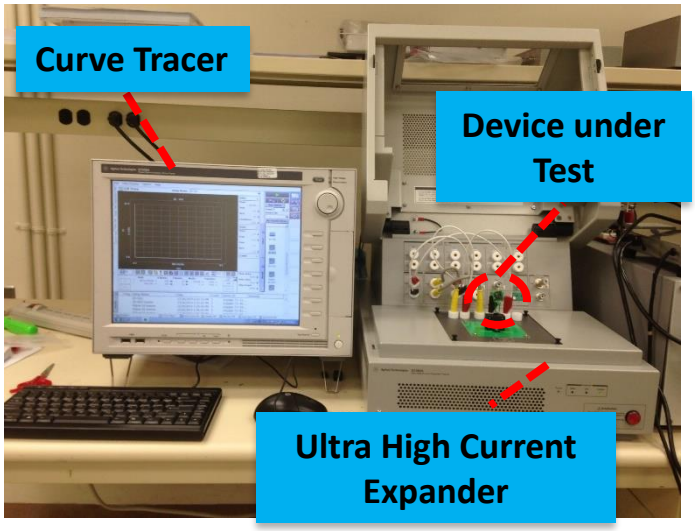


Figure A. 4 Experimental setup of static characterization

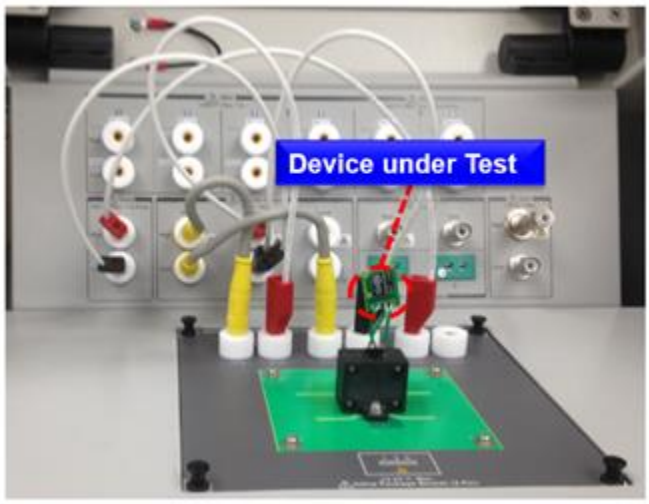


Figure A. 5 Ultra high current expander fixture showing device under test and drain, source and gate connections.

A.1.2 Experimental Results at Low Temperature

The output forward characteristics were measured by sweeping V_{ds} from 0-5 V at V_{gs} varying from 1 V- 10 V as the breakdown V_{gs} limit from is +/- 10 V. The gate-source voltage is kept constant for one V_{ds} sweep. The curve tracer has separate force and sense connections to apply voltage and current and to sense them separately. This Kelvin sense connection increases the accuracy of measurement. The pulse width of V_{gs} for measurement is kept very low (0.001 %) to avoid self-heating of the device. Also, it is assumed that the junction temperature will be similar

to case temperature because of the small duty ratio. A gate resistor of 100 Ω was selected on the curve tracer fixture to avoid any voltage and current overshoot on the device during turn-on and turn-off.

The forward output characteristics of the 650 V/ 30 A GaN HEMT at case temperature (T_c) 25 ^{O}C are shown in Fig. 3.6(a). The device starts to conduct very small current at V_{gs} 2 V and is fully enhanced at 5 V. The device saturates at I_d 44 A for V_{gs} 7 V-10 V. The reverse output characteristics as shown in Fig. 3.6(b) are measured by varying V_{ds} from -5-0 V and V_{gs} varying from -5-10 V. An important thing to note during reverse conduction is that the GaN HEMT doesn't have a body diode anti-parallel to the device but during reverse conduction, the channel starts to conduct when

$$V_{sd} > V_{sg} + V_{gsth} \quad (106)$$

where

V_{sd}- negative of applied drain-source voltage

V_{sg}- negative of applied gate-source voltage

V_{gsth}- gate-source threshold voltage

This phenomenon ensures that GaN HEMT will have very low on resistance during reverse conduction and hence lower reverse conduction losses as compared to silicon carbide (SiC) and silicon (Si) MOSFETs. Also, since enhancement mode GaN has no body diode, it has no reverse recovery losses which is a very big advantage over Silicon carbide (SiC) and cascode GaN devices. The reverse characteristics are similar to forward characteristics when applied gate source voltage is greater than 4 V. The device saturates at I_d -44 A for V_{gs} 7 V-10 V.

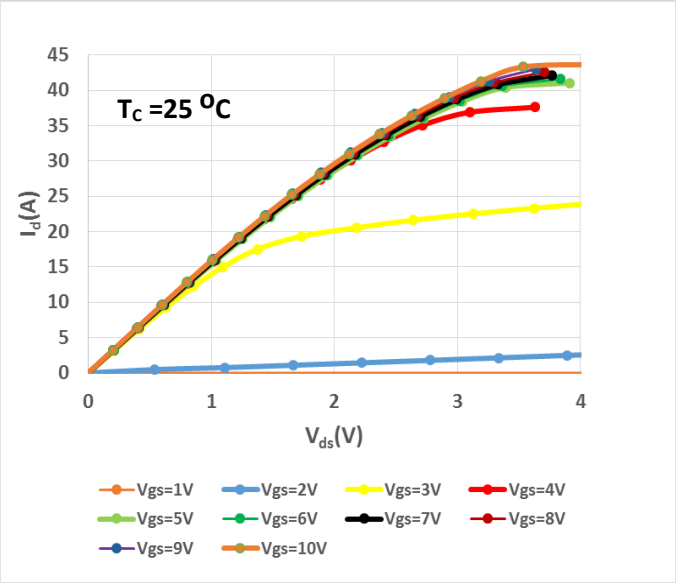


Figure A. 6 Forward characteristics of GaN HEMT at case temperature 25 °C

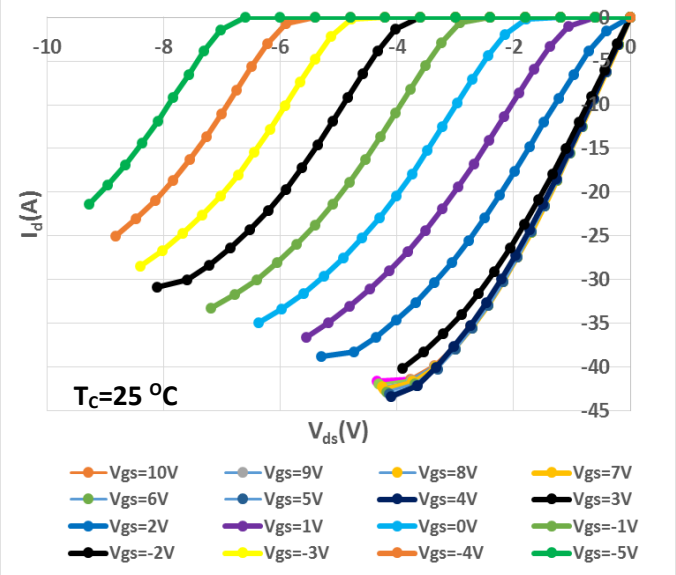
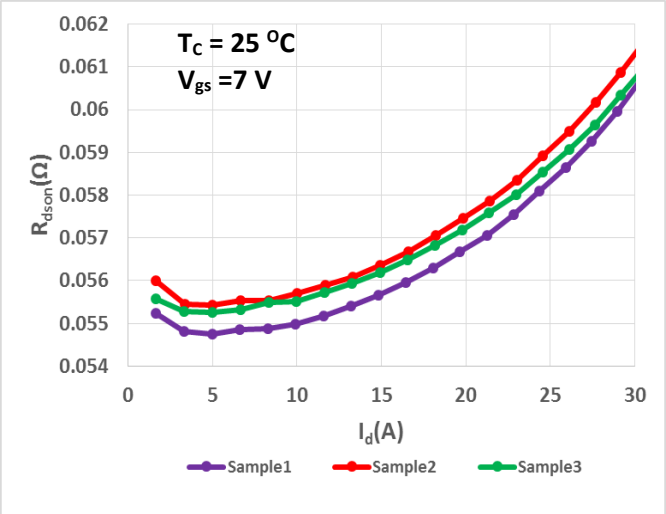


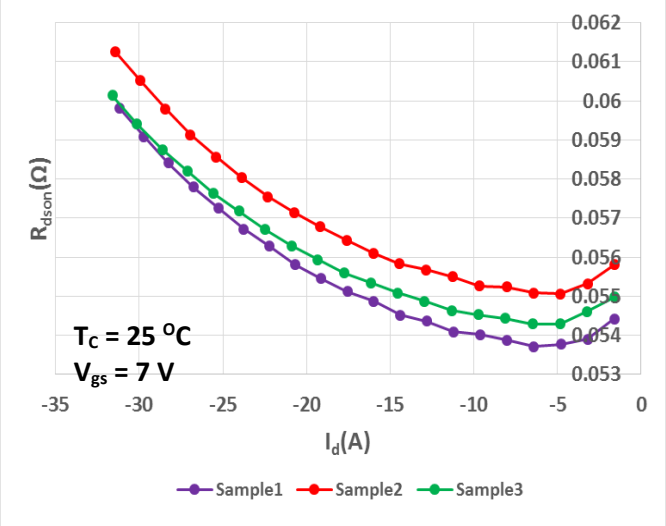
Figure A. 7 Reverse characteristics of GaN HEMT at case temperature 25 °C

The device on-resistance is measured by the curve tracer by measuring the slope of the I-V curve. The resistance of the wires and connectors is compensated by subtracting the value from the measured on resistance. The measured forward on-resistance (R_{dson}) at I_d 9 A and V_{gs} 7 V is 55 mΩ as shown in Fig. 3.8(a) while in [A.26] it is mentioned to be 52 mΩ. The measured reverse on-resistance (R_{dson}) at I_d -9 A and V_{gs} 7 V is 54.5 mΩ. This shows that this device has a very low on resistance which makes it ideal for high power applications. The cascode GaN device with similar voltage and current ratings has three times on resistance at similar current levels. Also, it

can be seen from Fig. A.8 that on resistance (both forward and reverse) is almost constant for I_d 0 - 30 A.



(a)



(b)

Figure A. 8 (a) Forward on resistance vs drain current and (b) Reverse conduction resistance vs drain current of GaN HEMT at V_{gs} 7 V and T_c 25 °C

The transfer characteristics are measured by varying V_{gs} from 0-5 V at a constant V_{ds} bias of 7 V. The device starts to conduct when $V_{gs} > V_{gsth}$ as shown in Fig. 3.9. The gate threshold voltage is 1.6 V from [A.26] and from the measurement, it is found to be 1.8 V. The threshold voltage is the applied gate-source voltage at which the drain current I_d is 7 mA under the operating conditions

of $V_{ds} = V_{gs}$. The drain current at which the threshold voltage is defined is recommended by the device manufacturers. The measured trans-conductance is 15 S while in [A.26], it's mentioned to be 13 S.

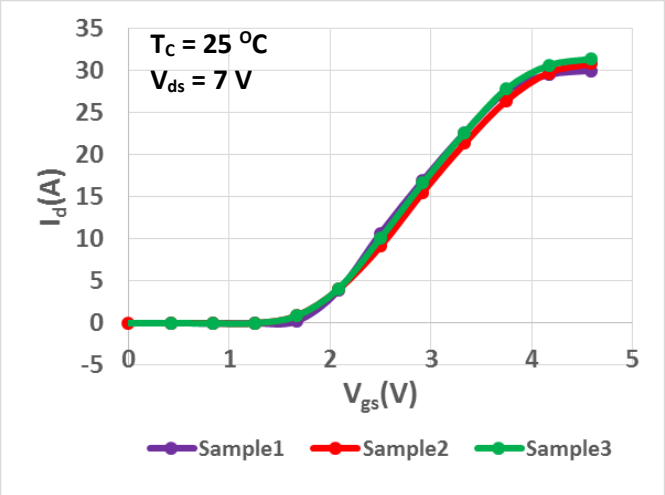


Figure A. 9 Transfer characteristics of GaN HEMT at V_{ds}7 V and T_c 25 °C

The device blocking capability can usually be evaluated by two parameters: BV_{DSS} –the drain-source breakdown voltage, and I_{DSS} – the drain leakage current at the rated voltage. For MOSFET, BV_{DSS} is usually defined as the voltage which produces 250 μA drain leakage current with the gate-source terminals shorted. Under this criterion, BV_{DSS} is usually measured to be higher than the rated voltage. However, under elevated temperatures, devices may break down even before the leakage current reaches 250 μA. For mature and rugged devices, all the single cells within the device are uniform in their blocking capability. These devices also have built-in avalanche capability that helps them survive from short-time unexpected over-voltage stress.

However, for certain prototype DUTs, some single cells are weaker than the others, which will break down first under high voltage stress, and the resultant damage is usually not recoverable. In this case, the DUT is destroyed (i.e. can no longer block voltage) even if the output characteristics still look fine. To avoid possible damages to the GaN DUTs, I_{DSS} is adopted in this work to evaluate the device blocking capability instead of BV_{DSS}, and is measured under the High Voltage Mode of the curve tracer. Measuring I_{DSS} is relatively safer because the leakage current is

obtained under rated V_{DS} voltage with the channel pinched-off. The drain leakage current is measured to be 2.4 µA at 650 V V_{ds} and T_C 25 ^{O}C as shown in Fig. A.10.

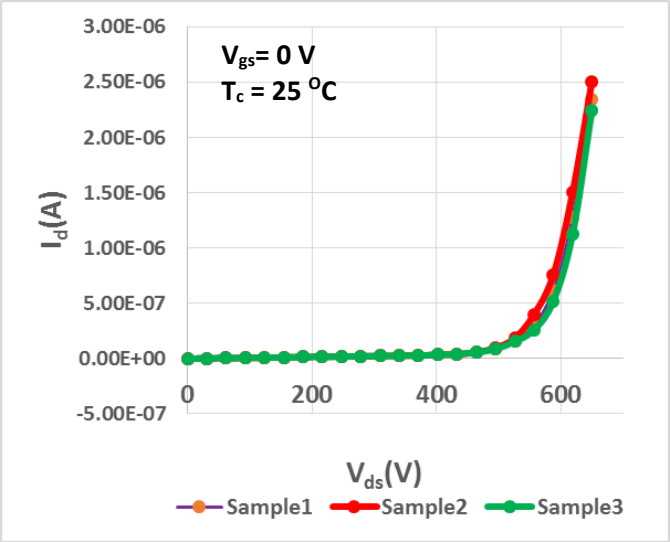


Figure A. 10 Drain leakage current vs drain source voltage with device pinched off and T_c 25 ^{O}C

As discussed above the device parasitic capacitances are termed as C_{ds} (drain-source capacitance), C_{gs} (gate-source capacitance) and C_{gd} (gate-drain capacitance). The input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) are given by:

$$C_{iss} = C_{gs} + C_{gd} \quad (107)$$

$$C_{oss} = C_{gd} + C_{ds} \quad (108)$$

$$C_{rss} = C_{gd} \quad (109)$$

The capacitances are measured by using the high voltage bias tee (Agilent N1260A) with the curve tracer. The C_{gd} measurement block diagram is shown in Fig. A.11. Only the AC measurement signal passing through C_{dg} component is measured by the Im current meter, and converted to C_{dg}. The AC current passing through C_{ds} flows in AC Guard, and it does not affect the C_{dg} component. Also the potential of L (low) input is almost GND level, and the C_{gd} current branching off to C_{gs} component can be ignored since the potential between C_{gs} is close to zero

volts. However, at high frequency the impedance of AC guard increases which may cause some signal leaks to C_{gs} affecting measurement accuracy.

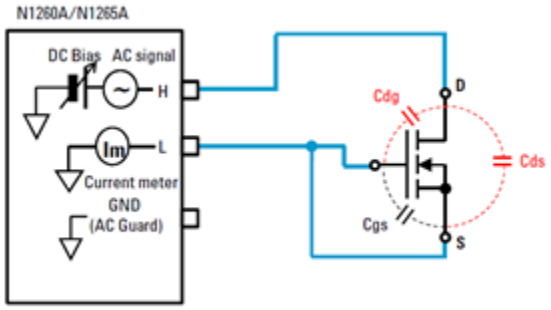


Figure A. 11 Block diagram for C_{dg} measurement

For C_{oss} measurement, the gate and source of the device are both connected to L. The measured C_{oss}, C_{rss} and C_{iss} from experiment are 62 pF, 7 pF and 182 pF respectively at V_{ds} 400 V. These measurements match well with the capacitance values in the preliminary datasheet. These capacitances are quite lower as compared to state-of-the-art Si and SiC devices. The results are shown in Fig. A.11.

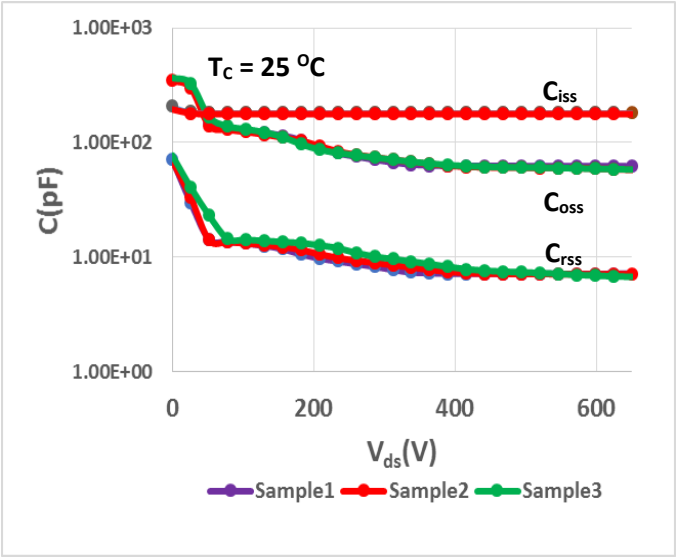


Figure A. 12 Parasitic capacitances vs drain source voltage. These capacitances are measured at a frequency of 1 MHz

A.1.3 Experimental Results at High Temperature

A lot of device parameters such as on-resistance, threshold voltage, blocking capability etc. vary with junction temperature. The device on resistance increases with temperature which leads to increase in power loss on the device and hence temperature increases further. The leakage currents also increase with increase in junction temperature. This is due to the intrinsic carrier concentration increasing exponentially with temperature. The high temperature static characterization setup is shown in Fig. A.13.

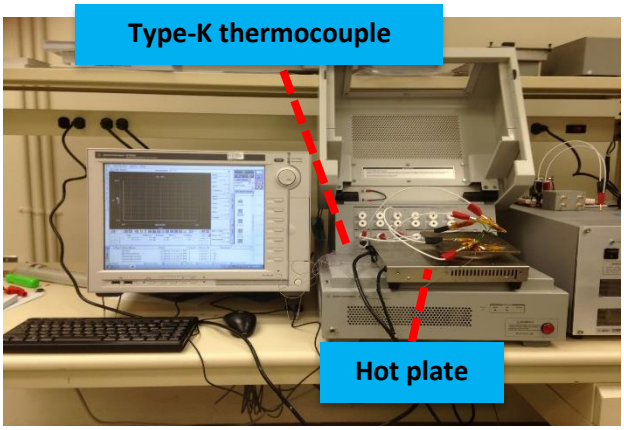
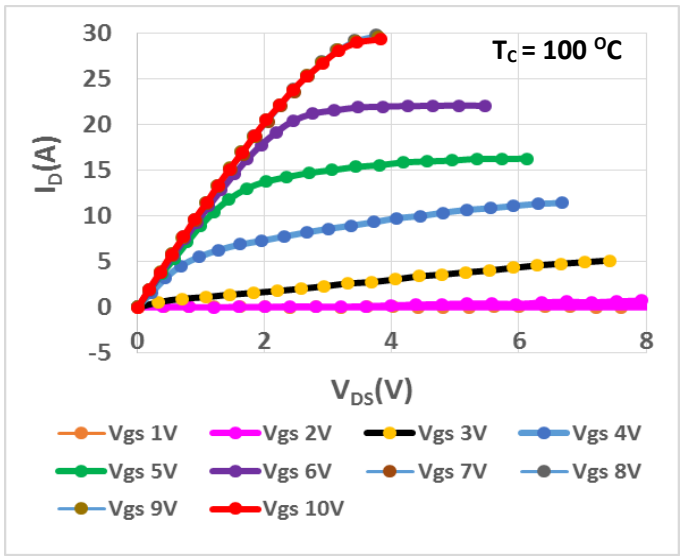
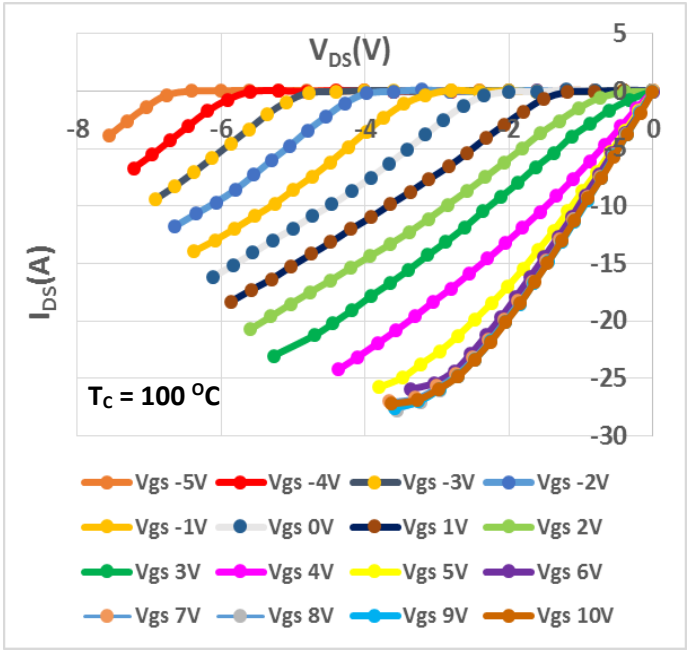


Figure A. 13 High temperature static characterization setup

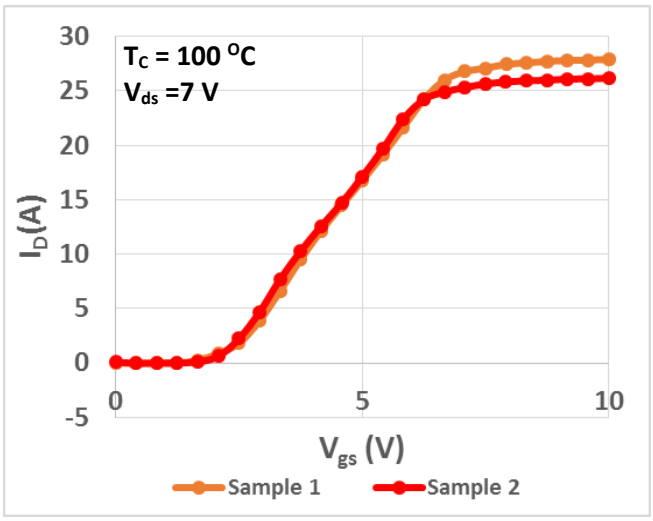
The device is heated on a hot plate, a thermocouple is used to measure the device case temperature which is connected to the curve tracer. The device begins to saturate at lower drain currents for the same gate-source voltage as shown in Fig. A.14(a), the GaN HEMT saturates at 30 A for V_{gs} 7-10 V. The device is fully enhanced at V_{gs} 7 V at T_C 100 ^{O}C as compared to 5 V at 25 ^{O}C as shown in Fig. A.14(a) and (b). Hence, the recommended gate driver voltage for this device is 7 V which is 3 V lower than the gate breakdown voltage. The trans-conductance of the device at 100 ^{O}C is half of the trans-conductance at 25 ^{O}C as shown in Fig. A.14(c).


T_C = 100 °C
I_D(A)
V_{DS}(V)
Vgs 1V
Vgs 2V
Vgs 3V
Vgs 4V
Vgs 5V
Vgs 6V
Vgs 7V
Vgs 8V
Vgs 9V
Vgs 10V

(a)


V_{DS}(V)
I_{DS}(A)
T_C = 100 °C
Vgs -5V
Vgs -4V
Vgs -3V
Vgs -2V
Vgs -1V
Vgs 0V
Vgs 1V
Vgs 2V
Vgs 3V
Vgs 4V
Vgs 5V
Vgs 6V
Vgs 7V
Vgs 8V
Vgs 9V
Vgs 10V

(b)



(c)

Figure A. 14 (a) Output forward characteristics (b) Reverse characteristics (c) Transfer characteristics at case temperature 100 ^{O}C

As can be seen from Fig. A.14 (a) and (b), the slope of I-V curve during enhancement mode has greatly reduced which signifies a large increase in R_{dson}. Forward on-resistance increases to 136 mΩ at I_d 9 A and T_C 144 ^{O}C as compared to 54.5 mΩ at T_C 25 ^{O}C. Similarly, the reverse on-resistance also increases to 129 mΩ at 144 ^{O}C case temperature and -9 A I_d. The normalized on-resistance vs temperature is shown in Fig. A.15.

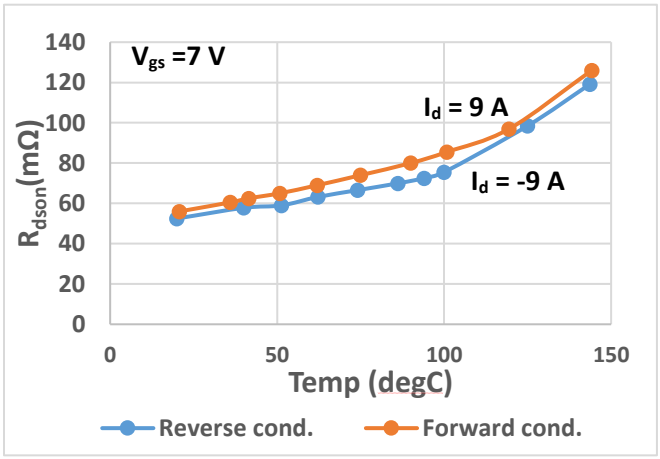


Figure A. 15 Normalized forward conduction and reverse conduction on resistance vs temperature

From the static characterization results shown above, it is clear that the parasitics play a very important role in the device switching and dynamic performance. Also, the parasitics change with

the drain current and voltage applied on drain-source or gate-source. These parameters are also temperature dependent. To understand the performance of the device in the phase leg configuration, dynamic characterization in discussed below.

A.2 Dynamic Characterization

As discussed in introduction section, for high frequency applications, it is very important to design the phase leg PCB layout with low loop inductance. GaN Systems' GS66508 has very low package inductance (drain and source inductances are each 0.2 nH from [A.26]). The gate driver block diagram to control the device is shown in Fig. A.16. It is shown that isolation is important between the control signal and the power side. This isolation ensures that the noise and high dv/dt from the power side doesn't get transferred to the control side. The primary side of the isolated gate driver is supplied from the controller and the secondary side is powered from the isolated power supply. This power supply is chosen for its very small isolation capacitance (C_{iso}: 2 pF) so that it provides good blockage to the noise from the power side.

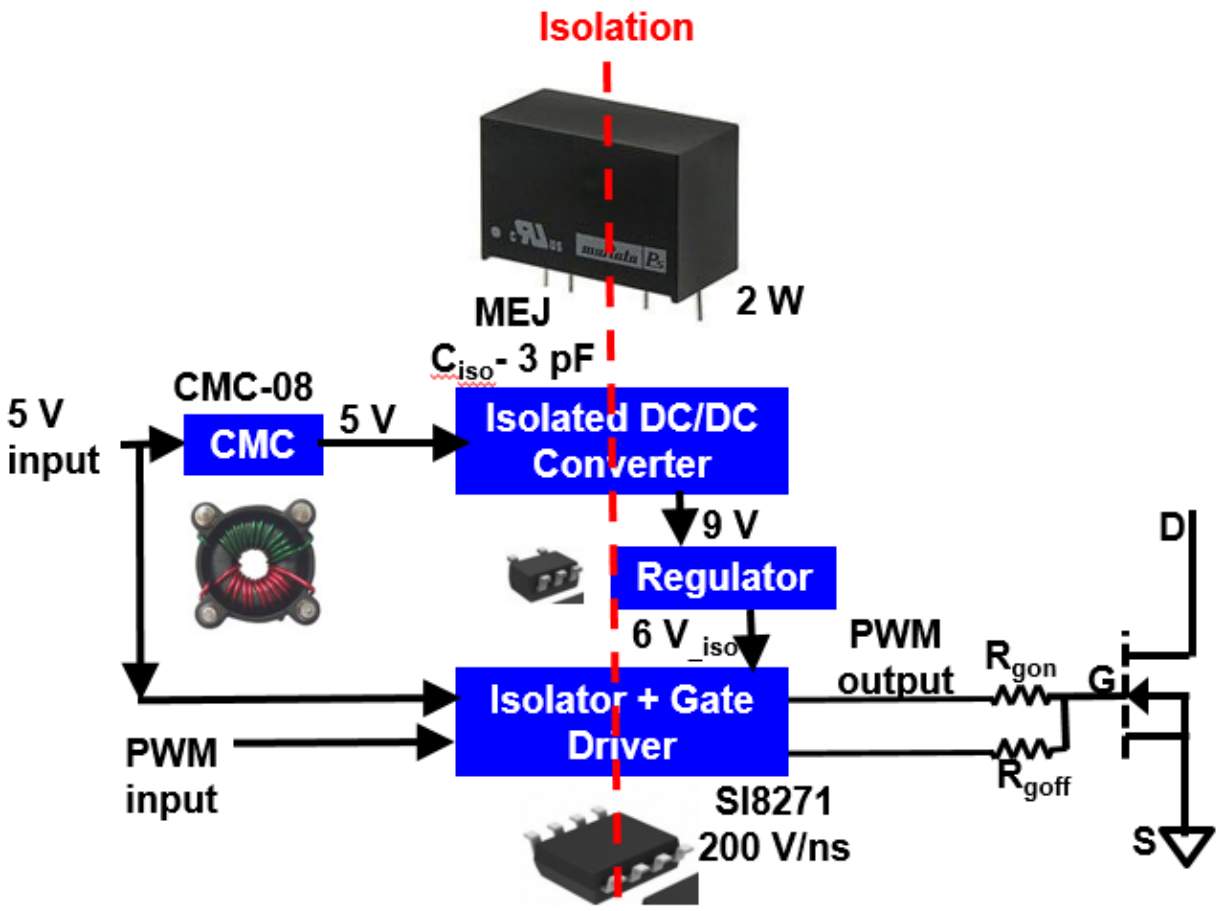


Figure A. 16 Gate driver block diagram for 650 V/ 30 A GaN device

The gate driver schematic is shown in Fig. A.17 with the specific rating of each component.

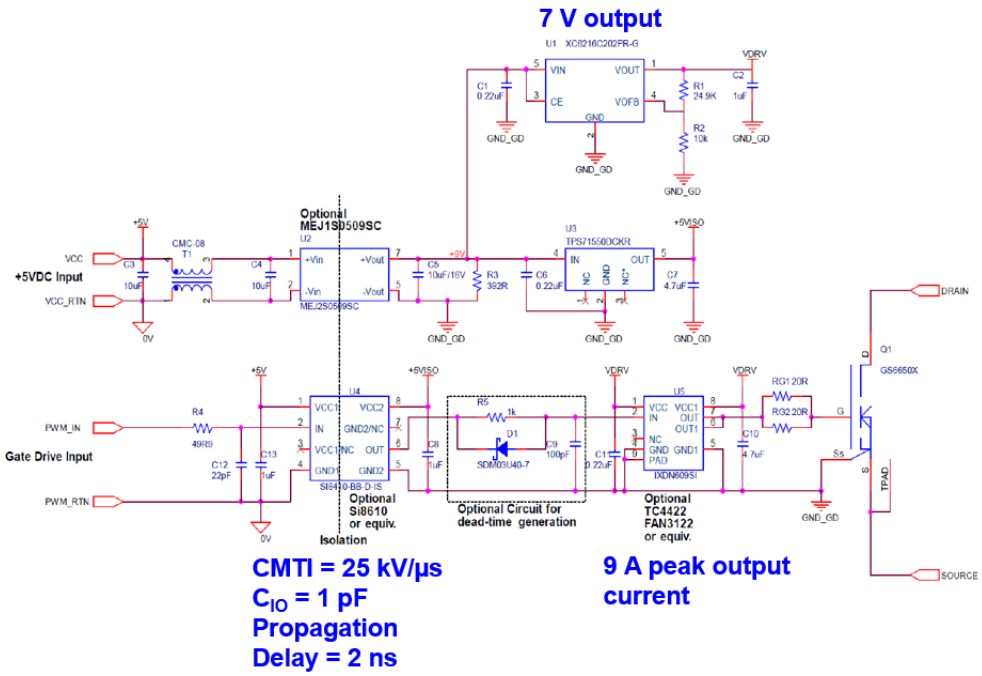


Figure A. 17 Gate driver schematic

A.2.1 Phase Leg Design

The phase leg schematic is shown in Fig. A.18. For phase-leg layout, two designs are compared in terms of electrical and thermal performance. The first one is a reference lateral phase leg design in which both the devices are placed on the top side of the board as shown in Fig. A.19(a). The second design is the vertical phase leg in which one device is on top side of the PCB and the other one is on the bottom side of the board as shown in Fig. A.19(b). The power loop inductance is thus limited only by device package inductance, dimensions of the device and the PCB. The vertical design has a lower power loop inductance (~0.6 nH) as compared to the lateral power loop (~3 nH).

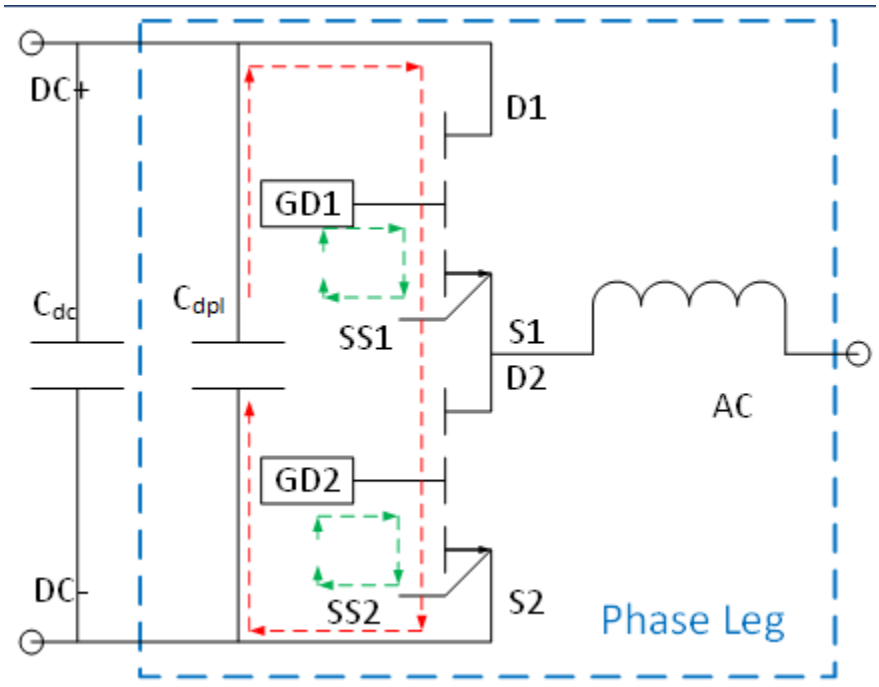
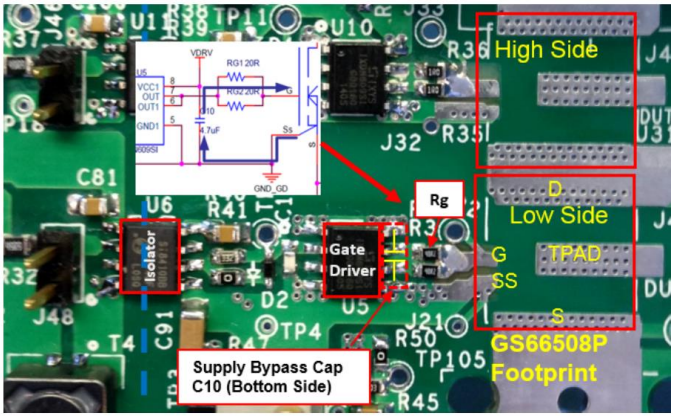
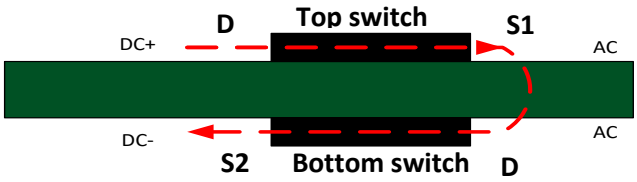


Figure A. 18 Phase Leg Schematic



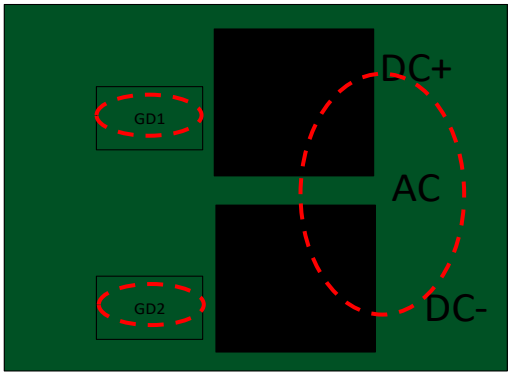
(a)



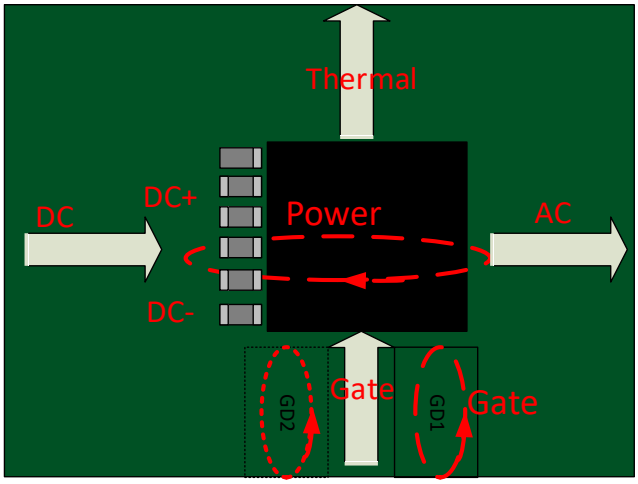
(b)

Figure A. 19 (a) Lateral Phase Leg Design (b) Vertical Phase Leg Design

The vertical design also enjoys the benefit of minimized coupling between gate loop and power loop as the gate loop is perpendicular to the power loop. Whereas in the reference design the gate loop is parallel to the power loop and the AC and DC terminals are coupled with each other as shown in Fig. A.20(a). The vertical design has minimal coupling between AC and DC terminals of the phase leg.



(a)



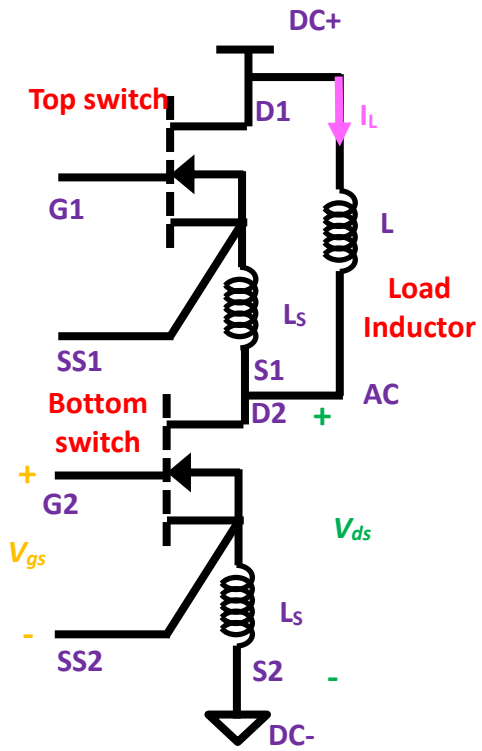
(b)

Figure A. 20 (a) Power loop and gate loop coupling in reference phase leg design (b) Minimal power loop and gate loop coupling in vertical phase leg design

A.2.2 Experimental Results

The double pulse test of the two designs is conducted with the load inductor connected across the top switch as shown in Fig. A.21(a). The experimental setup is shown in Fig. A.21(b). The bottom switch was turned on and off (with 5 µs dead time) while the top switch was kept off. The gate driver is designed for on state V_{gs} 7 V and off state V_{gs} 0 V. The results at 400V DC voltage, 30 A inductor current for lateral phase leg design are shown in Fig. A.22(a), and for vertical phase leg design are shown in Fig. A.22(b).

The V_{ds} overshoot measured for vertical design was 68.8V (17.2%) whereas from the double pulse test results in lateral design at similar conditions, the V_{ds} overshoot is 188 V (47 %). Thus the vertical design can reduce the voltage overshoot to less than half as compared to the lateral power loop design. This low overshoot paves the way for reduction of gate resistance, faster switching and hence lower energy losses. The V_{gs} rise time is less than 20 ns and peak V_{gs} measured is 9 V. The high noise in V_{gs} might also be due to absence of accurate measuring points on the board.



(a)

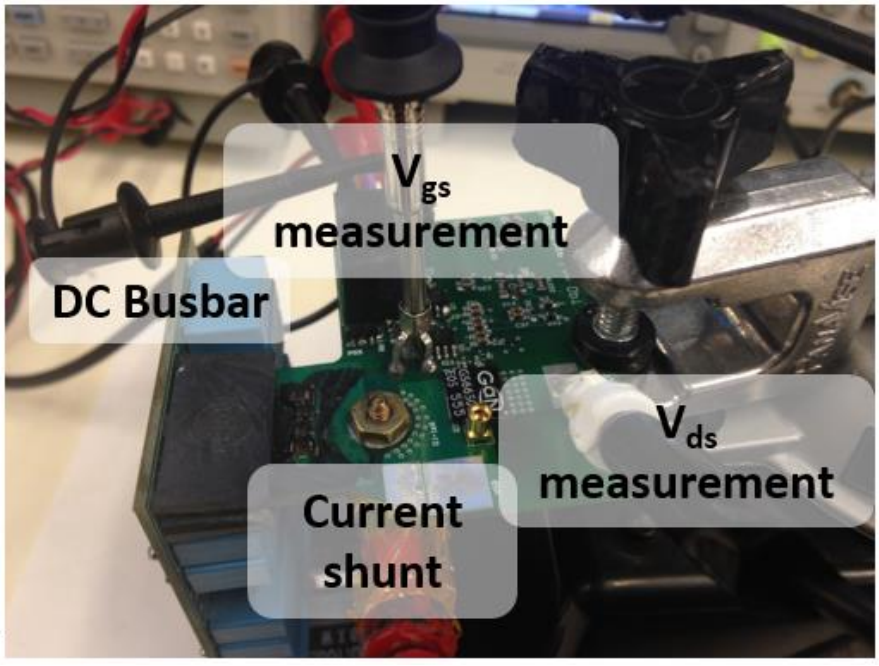
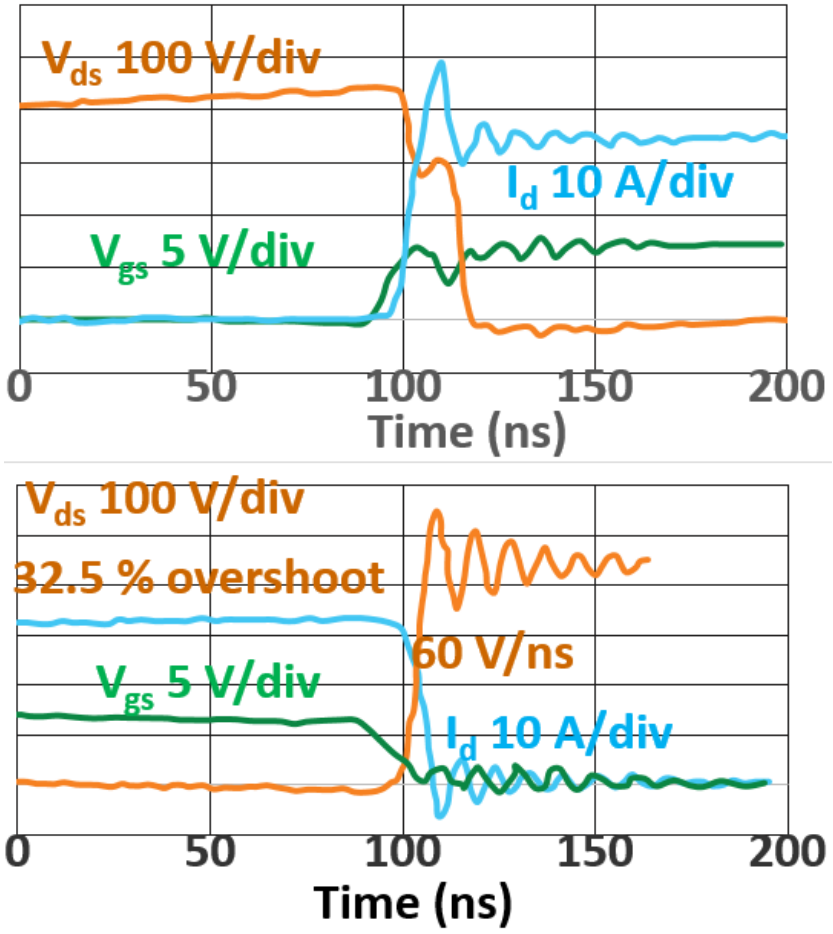
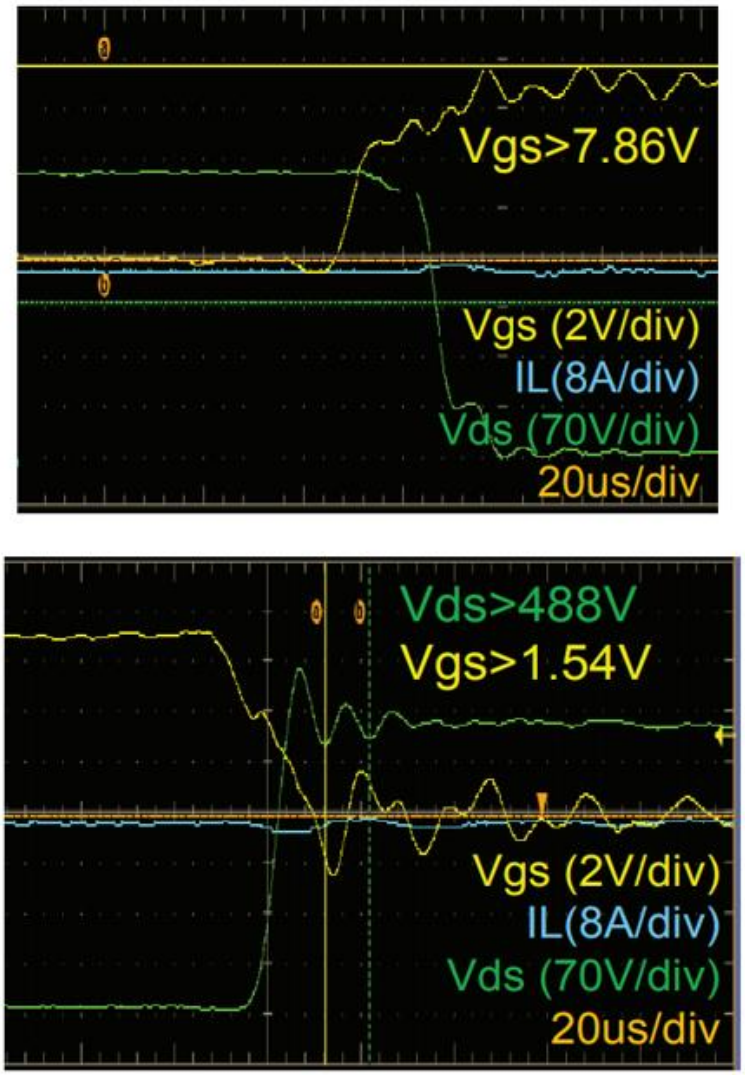


Figure A. 21 (a) Phase leg schematic for DPT with inductor across top switch (b) Experimental setup


V_{ds} 100 V/div
I_d 10 A/div
V_{gs} 5 V/div
0
50
100
150
200
Time (ns)
V_{ds} 100 V/div
32.5 % overshoot
60 V/ns
V_{gs} 5 V/div
I_d 10 A/div
0
50
100
150
200
Time (ns)

(a)



(b)

Figure A. 22 Turn-on and Turn-off transients at 400 V, 33 A for (a) Lateral Phase Leg Design

(b) Vertical Phase Leg Design

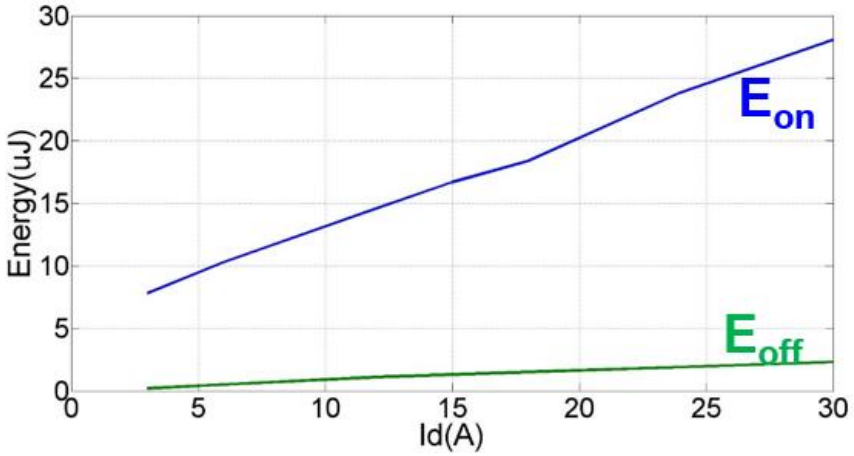


Figure A. 23 Switching losses for 650 V/ 30 A GaN HEMT

The switching losses measurement shown in Fig. A.23 shows the necessity of soft turn-on.

A.3 Summary

The detailed static characterization of the low package inductance 650 V/ 30 A and 650 V/ 60 A GaN HEMTs at room temperature and high temperature is shown in this chapter. The key conclusions from static characterization are that R_{dson} increases considerably with temperature, the device turns on fully at 6 V while the maximum transient gate voltage allowed is 10 V thus leaving a very small margin for the overshoot on gate voltage. This makes the gate loop design very critical.

The dynamic characterization of the proposed low inductance vertical layout is shown, the voltage overshoot in this case is less than half of the voltage overshoot in the lateral phase leg design from [A.33]. Hence, the devices can be turned on faster with lower switching losses. The turn-on losses are 10* the turn-off losses making soft turn-on necessary at high switching frequency.

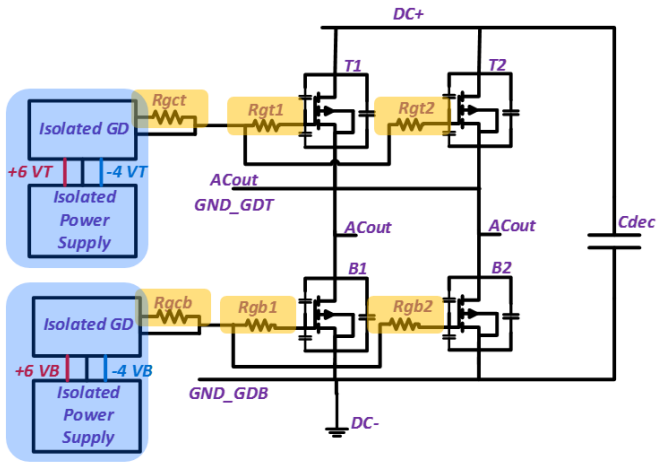
APPENDIX B

Phase Leg Design with Multiple Devices in Parallel

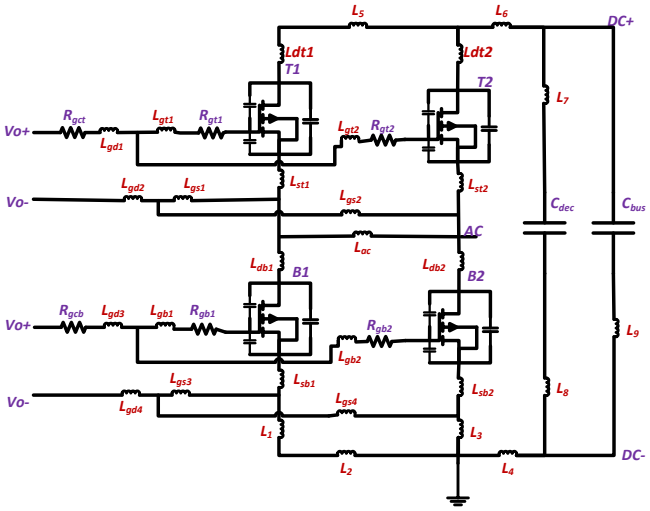
Appendix A discusses the importance of low inductance gate driver and phase leg design for high frequency operation. However, for higher power requirement, devices have to be connected in parallel. In this section, the design and operation of two 650 V/ 60 A Gallium Nitride (GaN) devices in parallel connection is discussed in detail, further, the challenges faced and the trade-offs required for paralleling high speed GaN devices are also examined. The dynamic characterization of two devices in parallel is presented in detail. The phase leg design requires both power loops and gate loops to be as small and as identical as possible for the two devices as for high speed GaN devices, even a small parasitic inductance or capacitance added due to the layout causes high overshoot in device voltage and current.

B.1 Schematic and Layout

The phase leg schematic with two devices in parallel is shown in Fig. B.1(a). The split on-state resistor (R_{gt1}, R_{gt2}, R_{gb1}, R_{gb2}) for each device is same as the off-resistor. It should be noted that it is very important to have some split gate resistors for each device after the common gate resistor as shown in Fig. B.1 to control the oscillations due to the loops formed in between the two devices and these split gate resistors have to be placed as close to the device gate as possible. The phase leg schematic including all the parasitics is shown in Fig.B.1 (b). The most important point for the layout design is that the parasitic inductances after the split of the gate path (L_{gt1}, L_{gt2}, L_{st1}, L_{st2}, L_{gs1}, L_{gs2}, L_{gb1}, L_{gb2}, L_{sb1}, L_{sb2}, L_{gs3}, L_{gs4}) should be small (<0.2 nH) and identical. The gate loop inductances from the gate driver to the device gate (L_{gdi}, $i \in$ 1-4) and the power loop inductances should also be small and identical.



(a)

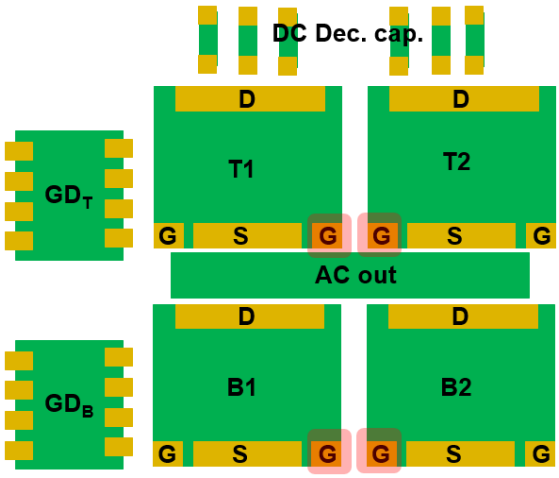


(b)

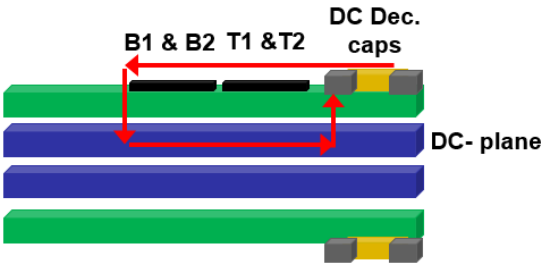
Figure B. 1 (a) Phase Leg Schematic and (b) Phase Leg Schematic with parasitics

The phase leg layout block diagram is shown in Fig. B.2(a). The gate drivers are on the bottom side of the board while all the devices are on the top side of the board. The dual gate pins of the device are made use of and only the gate pins in the middle are connected to the gate driver asshown in the figure. From [A.24], the two gate pads are internally shorted, hence, gate driver connection to only one gate pad is sufficient for driving the device. The gate loop inductances after the split are as small as 0.5 nH, the total gate-source loop inductance for all the devices is close to 3.5 nH, the gate-source loop is identical for top and bottom devices and for both the devices in parallel. The power loop inductance is also very small- 1nH. The parasitic inductances and

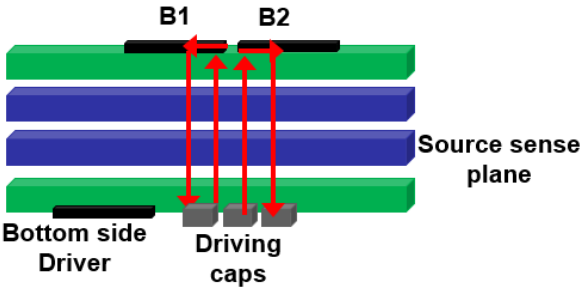
capacitances are simulated from FEA simulation. The power loop and gate loop are shown in Fig. B.2 (b) and (c) respectively. Though the device doesn't have a separate source sense pin, separate layers are used for power loop and gate loop grounds thus minimizing the mutual inductance between the two loops.



(a)



(b)



(c)

Figure B. 2 (a) Phase leg layout (b) Phase leg lateral view showing power loop (c) Phase Leg side view showing gate loop

The DPTer schematic with two current shunts is shown in Fig. B.3 (d), each shunt is in series with the device. To avoid paralleling of shunts, source resistors (R_{sb1},R_{sb2}) have to be added in between the device source and gate driver ground to measure individual device current accurately. The value of these source resistors has to be much larger than the current shunt resistance so that the drain current passes through the shunt but this resistor is also included in the gate loop, hence it cannot be too large.

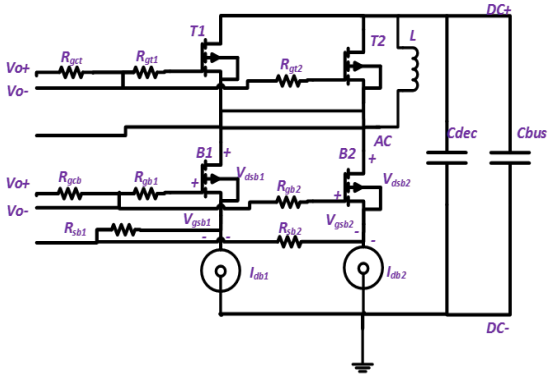


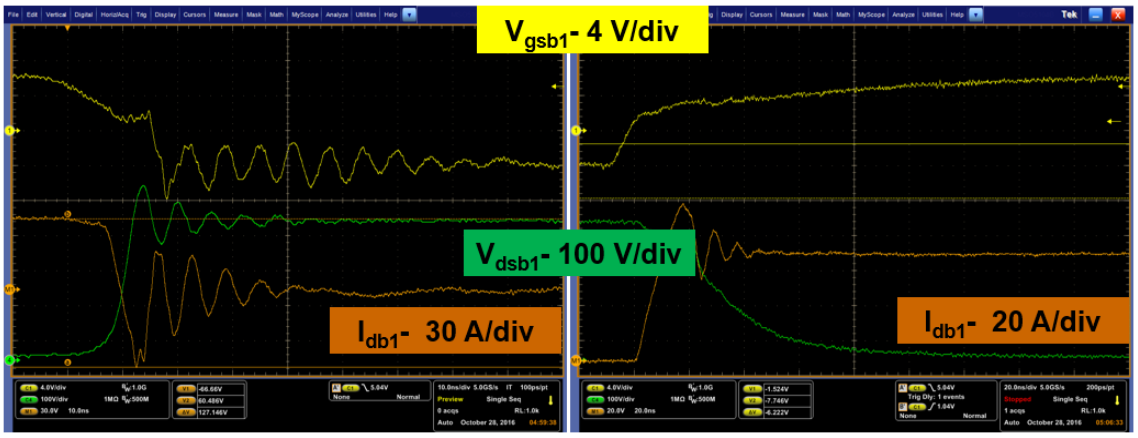
Figure B. 3 DPTer schematic with shunts and source resistors

B.2 Experimental Results

The DPTer is populated with just one phase leg initially (one top and one bottom device) and then, after the single phase leg characterization is done till 400 V, 60 A, all the four devices are populated on the board. The split gate resistor (R_{gb1} and R_{gb2} in Fig. B.2 (a)) being 4 Ω each. The source resistor is chosen as 1 Ω and the common gate resistor is 20 Ω. Thus, the total on-state resistor is 25 Ω while the off-state resistor is 5 Ω.

The single phase leg DPT results for bottom device with inductor across the top switch are shown in Fig. B.4. Gate source voltage (V_{gsb1}) of the device is measured with a single ended passive probe of bandwidth 1 GHz, drain source voltage (V_{dsb1}) is measured with a passive probe of bandwidth 500 MHz and the device current (I_{db1}) is measured with a current shunt, resistance 15 m Ω and bandwidth 1 GHz. The on-state gate voltage is 6 V while the off-state voltage is -4 V (as recommended in [A.24]). It is mentioned that for paralleling, a negative off-state voltage is

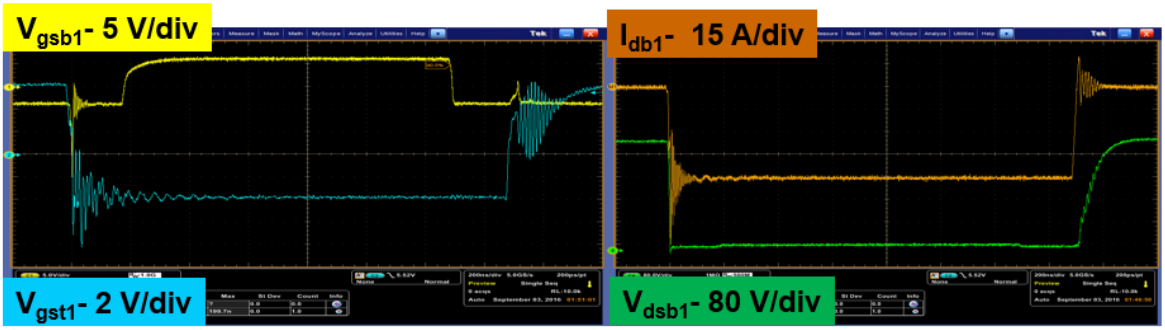
required to avoid the issue of false turn-on as the Miller capacitor (C_{gd}) is doubled. As shown in Fig. B.4, there are very small oscillations in the gate voltage, the V_{dsb1} overshoot during turn-off is also small (97 V). The overshoot without the current shunt will be smaller as the shunt adds approximately 3 nH inductance to the power loop.



(a) (b)

Figure B. 4 Single Device Phase Leg DPT at 400 V, 60 A (a) Bottom device turn-off and (b) turn-on

The top device DPT is also conducted (with inductor across the bottom switch) to measure the miller effect on bottom device. During the turn-on of top device, the bottom V_{gsb1} reaches 0.93 V, which is acceptable as the device threshold voltage is 1.3 V. The results are shown in Fig. B.5 (a) and (b). The top device gate-source voltage (V_{gst1}) is measured using a differential probe, hence it has more noise.



(a) (b)

Figure B. 5 Single Device Phase Leg DPT at 400 V, 60 A (a) Gate voltages during top device turn-off and turn-on and (b) Bottom device drain-source voltage and drain current during top device switching.

Further, the DPT with two devices in parallel was conducted. As shown in Fig B.6, the static current sharing between the two devices is accurate. The DPT results are shown at 400 V, 100 A with the two shunts shorted in Fig. B.7. The two shunts are shorted to avoid any circulating current between the two devices because of the path of circulating current created by the two shunts.

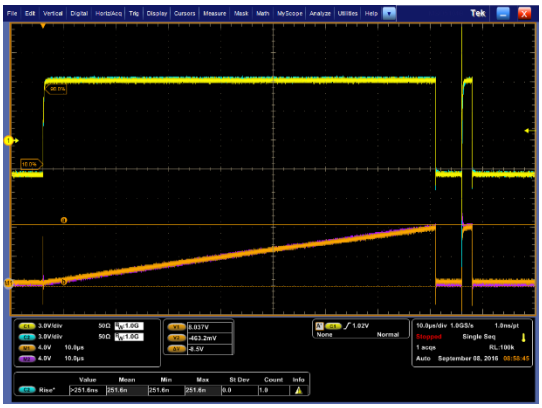
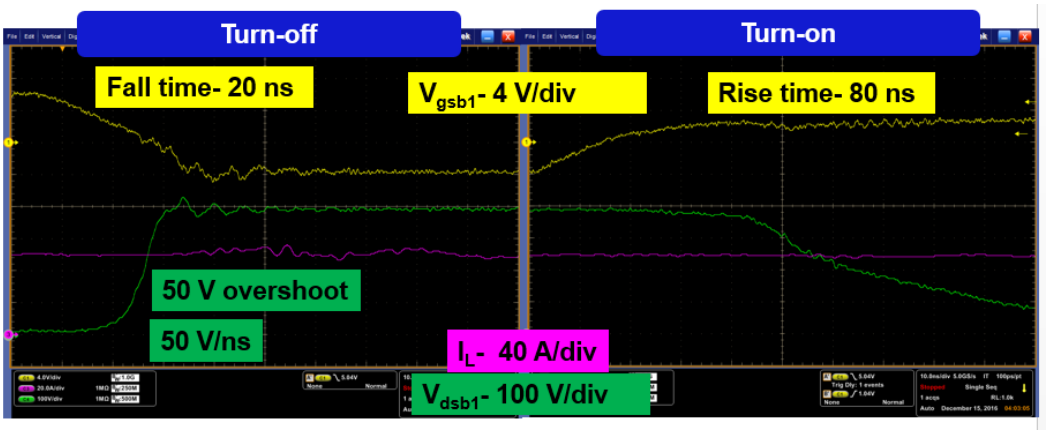


Figure B. 6 Paralleled devices' Phase Leg DPT at 200 V, 15 A



(a) (b)

Figure B. 7 Paralleled devices' DPT with the two shunts shorted at 400 V, 100 A (a) Turn-off (b) Turn-on

It can be concluded from the device characterization that fast speed WBG devices enhance the switching and thermal performance, however due to the fast speed, a good design with minimal loop inductances is necessary for minimizing the noise and losses caused by fast transients. For efficient operation in TCM mode, multiple devices are connected in parallel to reduce the conduction losses. The main challenge for paralleling high speed GaN devices is circulating current between the two devices. To minimize this current, the layout should be designed so that both the devices' gates and sources are as close to each other as possible. Secondly, using split gate resistors is recommended.

References

A. Introduction & GaN Converter Design

[A.1] Yang Xi-jun, Wang Han, Yang Xing-hua, Lei Huai-gang, Guan Hongfei, "Theoretical Analysis and Experimental Study of a Novel Bridgeless Partial Active PFC," in *Proc. IEEE-ICEMS'* 2008 Ann. Meet., pp. 1179-1184.

[A.2] Bin Su and Zhengyu Lu, "An Interleaved Totem-Pole Boost Bridgeless Rectifier with Reduced Reverse-Recovery Problems for Power Factor Correction," in *IEEE Transactions on Power Electronics,* vol. 25, no. 6, pp. 1406-1415, June 2010.

[A.3] C. Marxgut, J.Biela and J.W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifier with High Efficiency and High Power," in *Proc. IEEE-IPEC' 2010 Ann. Meet.*, pp. 1725-1732.

[A.4] Yuancheng Ren., Ming Xu., Zhou J., Lee F.C., "Analytical Loss Model of Power MOSFET," *in IEEE Transactions on Power Electronics,* vol. 25, no. 2, pp. 310-319, Mar. 2006.

[A.5] D. Jauregui, B. Wang and R. Chen, "Power Loss Calculation with Common Source Inductance Consideration for Synchronous Buck Converters," Texas Instruments Application Report, 2011.

[A.6] Zijian Wang, "DM EMI Noise Analysis for Single Channel and Interleaved Boost PFC in Critical Conduction Mode," MS dissertation, CPES, Virgina Tech., Blacksburg, 2010.

[A.7] Delaine J., Jeannin P., Frey D., Guepratte K., "High frequency DC-DC Converter using GaN device," in *Proc. IEEE-APEC' 2012 Ann. Meet.,* pp. 1754-1761.

[A.8] Xiucheng Huang, Qiang Li, Zhengyang Liu and Fred C. Lee, "Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration," in *Proc. IEEE-ECCE' 2013 Ann. Meet.*, pp. 3587-3594.

[A.9] Fu-Yuan Shih, Dan Y. Chen, Yan-Pei Wu, and Yie-Tone Chen, "A Procedure for Designing EMI Filters for AC Line Applications," in *IEEE Transactions on Power Electronics,* vol. 11, no. 1, pp. 170-181, Jan. 1996.

[A.10] C. Marxgut, "Ultra-Flat Isolated Single-Phase AC-DC Converter Systems," Ph.D. dissertation, ETH Zurich, Zurich, 2012.

[A.11] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. White and M. Kheraluwala, “Design and Optimization of a High Performance Isolated Three Phase AC/DC Converter”, *IEEE-ECCE* 2016, pp. 1-10.

[A.12]U. K. Mishra, P. Parikh, and Y. F. Wu, “AlGaN/GaN HEMTs - An overview of device operation and applications,” *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, 2002.

[A.13]N. Ikeda, S. Kaya, J. Li, Y. Sato, S. Kato, and S. Yoshida, “High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 287–290, 2008.

[A.14]International Rectifier, “GaNpowIR - An Introduction,” Www.Irf.Com, February, 2010.

[A.15]A. Brief, “Designing with GaN Transistors,” GaN Systems Applicate Note, 2014.

[A.16]J. Roberts, T. MacElwee, L. Yushyna, H. Lafontaine, I. Scott, and M. R. Ottawa, “White paper: Thermal and Electrical Performance of CMOS Driver Compatible GaN Power Transistors,” , The 2018 GaN Power Electronics Roadmap, pp. 5–8, 1996.

[A.17]A. Brief *et al.*, “GaN Systems to present paper on lateral GaN transistors in automotive applications at PCIM : new high current devices also to be announced,”May, 2014.

[A.18]W. Saito *et al.*, “A 120-W boost converter operation using a high-voltage GaN-HEMT,” *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 8–10, 2008.

[A.19]Z. Liu, X. Huang, W. Zhang, F. C. Lee, and Q. Li, “Evaluation of high-voltage cascode GaN HEMT in different packages,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 168–173, 2014.

[A.20]X. Huang, Z. Liu, Q. Li, and F. C. Lee, “Evaluation and application of 600V GaN HEMT in cascode structure Evaluation and Application of 600V GaN HEMT in Cascode Structure,”*Conf. Proc.- IEEE APEC*, pp. 2453–2461, 2013.

[A.21]“22 GaN-AlGaN HFETs (basic operation).”, Www.Irf.Com, February, 2010 .

[A.22]W. Chen, K. Y. Wong, and K. J. Chen, “Single-chip boost converter using monolithically integrated AlGaN/GaN lateral field-effect rectifier and normally off HEMT,” *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 430–432, 2009.

[A.23]Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, “A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz,” *IEEE Electron Device Lett.*, vol. 29,

no. 8, pp. 824–826, 2008.

[A.24]J. Roberts, G. Klowak, and L. Yushyne, “GaN Transistors – Drive Control, Thermal Management, Isolation,” *Power Electron. Technol.*, no. February, pp. 24–28, 2013.

[A.25]X. Huang, F. C. Lee, Z. Liu, and Q. Li, “Evaluation and Design Consideration of High Voltage Cascode GaN device,”, *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453 - 2461, 2014.

[A.26]O. J. Temperature, S. T. Range, D. Voltage, and G. Voltage, “GS66508P-E03 650V enhancement mode GaN transistor PRELIMINARY DATASHEET GS66508P-E03 650V enhancement mode GaN transistor PRELIMINARY DATASHEET,” pp. 1–4, 2014.

[A.27]Z. Liu, X. Huang, F. C. Lee, and Q. Li, “Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, 2014.

[A.28]B. Hughes, Y. Y. Yoon, D. M. Zehnder, and K. S. Boutros, “A 95% efficient normally-off GaN-on-Si HEMT hybrid-IC boost-converter with 425-W output power at 1 MHz,” *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC*, pp. 4–6, 2011.

[A.29]B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic, and K. Boutros, “GaN HFET switching characteristics at 350V/20A and synchronous boost converter performance at 1MHz,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, no. 310, pp. 2506–2508, 2012.

[A.30]J. Roberts, “Lateral GaN transistors - A replacement for IGBT devices in automotive applications,” *PCIM Eur. Conf. Proc.*, pp. 310–317, May 2014.

[A.31]X. Huang, Q. Li, Z. Liu, and F. C. Lee, “Analytical loss model of high voltage GaN HEMT in cascode configuration,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, 2014.

[A.32]D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic, “GaN-FET based dual active bridge DC-DC converter,” *2011 Twenty-Sixth Annu. IEEE Appl. Power Electron. Conf. Expo.*, pp. 1425–1432, 2011.

[A.33]A. Note, “Design considerations for driving GaN Systems power switches,” *www.GaNSystems.com*, pp. 3–5, 2013.

[A.34]B. Sun, R. Burgos, N. Haryani, S. Bala, and J. Xu, “Design, characteristics and application of pluggable low-inductance switching power cell of paralleled GaN HEMTs,” in *Proceedings IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, vol. 2017-Janua.

[A.35]J. Delaine, P. O. Jeannin, D. Frey, and K. Guepratte, “High frequency DC-DC converter using GaN device,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, no. 1, pp. 1754–1761, 2012.

[A.36]W. Saito *et al.*, “Demonstration of resonant inverter circuit for electrodeless fluorescent lamps using high voltage GaN-HEMT,” *Power Electron. Spec. Conf. 2008. PESC 2008. IEEE*, pp. 3324–3329, 2008.

[A.37]Q.Li, "Average Current Mode Control", Chapter 8, ECE 5254 Power Converter Modeling and Control, Virginie Tech., Blacksburg, 2013.

[A.38] Y. Chin and F. C. Lee, “Constant-frequency parallel-resonant converter,” *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 133–142, Jan./Feb. 1989.

[A.39] R. Redl, N. O. Sokal, and L. Balogh, “A novel soft-switching full-bridgedc/dc converter: Analysis, design considerations, at 1.5 kW, 100 kHz,” *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 408–418, Jul. 1991.

[A.40] T. Ninomiya, N. Matsumoto, M. Nakahara, and K. Harada, “Static and dynamic analysis of zero-voltage-switched half-bridge converter with PWM control,” in *IEEE Power Electron. Spec. Conf. (PESC) Rec.*, 1991, pp. 230–237.

[A.41] L. H. Mweene, D. M. Otten, and M. F. Schlecht, “A high-efficiency 1.5 kW, 390–50 V half-bridge converter operated at 100% duty-ratio,” *in Proc. IEEE Appl. Power Electron. (APEC) Conf.*, 1992, pp. 723–730.

[A.42] R. Liu and C.Q. Lee, “Series resonant converter with third-order commutation network,” *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 462–468, Jul. 1992.

[A.43] G. Hua, F. C Lee, and M. M. Jovanovic, “An improved full-bridge zero-voltage-switched PWM converter using a saturable inductor,” *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 530–534, Oct. 1993.

B. Single-Phase CRM/TCM

[B.1] Z. Liu, B. Li, F. C. Lee, and Q. Li, "Design of CRM AC / DC Converter for Very High-Bidirectional On-Board Battery Charger," in *Proc. IEEE ECCE*, 2016.

[B.2] S. H. Tang, D. Chen, C. S. Huang, C. Y. Liu, and K. H. Liu, "A new on-time adjustment scheme for the reduction of input current distortion of critical-mode power factor correction boost converters," *2010 Int. Power Electron. Conf. - ECCE Asia -, IPEC 2010*, pp. 1717–1724, 2010.

[B.3] A. Abramovitz, "Effect of the ripple current on power factor of CRM boost APFC," *Conf. Proc. - IPEMC 2006 CES/IEEE 5th Int. Power Electron. Motion Control Conf.*, vol. 2, pp. 1412–1415, 2007.

[B.4] Z. Lu and T. C. Green, "A study of soft-switched CCM boost AC/DC converter," *Seventh Int. Conf. Power Electron. Var. Speed Drives, 1998. (Conf. Publ. No. 456)*, no. 456, pp. 662–667, 1998.

[B.5] M. M. Ul Alam, W. Eberle, and F. Musavi, "A hybrid resonant bridgeless AC-DC power factor correction converter for off-road and neighborhood electric vehicle battery charging," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1641–1647, 2014.

[B.6] E. Firmansyah, S. Abe, M. Shoyama, S. Tomioka, and T. Ninomiya, "A critical-conduction-mode bridgeless interleaved boost power factor correction: Its control scheme based on commonly available controller," *Proc. Int. Conf. Power Electron. Drive Syst.*, pp. 109–114, 2009.

[B.7] F. C. Lee, and Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," *IEEE Journal of Emeriging and Selected Topics in Power Electroni*cs, vol. 4, no. 3, pp. 808–814, 2016.

[B.8] F. Yang, X. Ruan, Q. Ji, and Z. Ye, "Input DM EMI filter design of interleaved CRM boost PFC converter with coupled inductor," *IEEE Energy Convers. Congr. Expo. Energy Convers. Innov. a Clean Energy Futur. ECCE 2011, Proc.*, pp. 2614–2621, 2011.

[B.9] A. Note, "Totem pole bridgeless PFC using GaN transistors," www.GaNSystems.com, pp. 1–6, 2013.

[B.10] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM)

resonant transition, single phase PFC rectifier with high efficiency and high power density," *2010 Int. Power Electron. Conf. - ECCE Asia -, IPEC 2010*, pp. 1725–1732, 2010.

[B.11] P. Kong, S. Wang, and F. C. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, 2008.

[B.12] Z. Liu, X. Huang, M. Mu, Y. Yang, F. C. Lee, and Q. Li, "Design and Evaluation of GaN-Based Dual-Phase Interleaved MHz Critical Mode PFC Converter,", in *Proc. IEEE ECCE*, pp. 611–616, 2014.

[B.13] Z. Liu, Z. Huang, F. C. Lee, Q. Li, and Y. Yang, "Operation Analysis of Digital Control based MHz Totem-pole PFC with GaN Device," in *Proc. IEEE WiPDA*, 2015.

[B.14] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition , Single Phase PFC Rectifier with High Efficiency and High Power Density.", *IEEE ECCE Asia*, pp. 1725-1732, 2010.

[B.15] W. Zhang, S. Member, G. Feng, S. Member, Y. Liu, and S. Member, "A Digital Power Factor Correction (PFC) Control Strategy Optimized for DSP," *IEEE Trans. On Power Electronics, vol. 19*, no. 6, pp. 1474–1485, 2004.

[B.16] K. Yao, W. Hu, Q. Li, and J. Lyu, "A novel control scheme of DCM boost PFC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5605–5615, 2015.

[B.17] L. Gu, J. Sun, M. Xu, Q. Zuo, and J. Fan, "Size reduction of the inductor in critical conduction mode PFC converter," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 550–557, 2011.

[B.18] J. W. Shin, G. S. Seo, B. H. Cho, and K. C. Lee, "Digitally controlled open-loop master-slave interleaved boost PFC rectifier," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 304–309, 2012.

[B.19] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz Totem-pole PFC Rectifier," *IEEE ECCE*, pp. 682–688, 2015.

[B.20] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," *2010 Int. Power Electron. Conf. - ECCE Asia -, IPEC 2010*, pp. 1725–1732, 2010.

[B.21] C. Deng, M. Chen, P. Chen, C. Hu, W. Zhang, and D. Xu, "A PFC converter with novel

integration of both the EMI filter and boost inductor," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4485–4489, 2014.

[B.22] X. Wu, J. Yang, J. Zhang, and M. Xu, "Design considerations of soft-switched buck PFC converter with constant on-time (COT) control," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3144–3152, 2011.

[B.23] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, 2014.

[B.24] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799–807, 2016.

[B.25] C. Deng *et al.*, "Integration of both EMI filter and boost inductor for 1-kW PFC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5823–5834, 2014.

[B.26] Z. Qian and M. Chen, "Analysis and Average Modeling of Critical Mode Boost PFC Converter," in *Proc. IEEE PEDS*, pp. 138–141, 2001.

[B.27] F. Yang, X. Ruan, Q. Ji, and Z. Ye, "Input differential-mode EMI of CRM boost PFC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1177–1188, 2013.

[B.28] Y. L. Chen, Y. M. Chen, and C. N. Wu, "The time-domain analysis for constant on-time critical mode boost-type PFC converters," *2012 IEEE Energy Convers. Congr. Expo. ECCE 2012*, pp. 4643–4648, 2012.

[B.29] Z. Liu, Z. Huang, F. C. Lee, and Q. Li, "Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC," *IEEE Journal of Emeriging and Selected Topics in Power Electroni*cs, vol. no. 4, pp. 1847–1852, 2016.

[B.30] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, 2008.

[B.31] J. Kim, S. Member, and H. C. Member, "New Modulated Carrier Controlled PFC Boost Converter," *IEEE Trans. Power Electron*, vol. 33, no. 6, pp. 1–10, 2017.

[B.32] Y. Yang, Z. Liu, F. C. Lee, and Q. Li, "Multi-phase Coupled and Integrated Inductors for Critical Conduction Mode Totem-Pole PFC Converter," *IEEE APEC*, pp. 1804–1809, 2017.

[B.33] J. Zhang, J. Shao, P. Xu, F. C. Lee, and M. M. Jovanovic, "Evaluation of Input Current in the Critical Mode Boost PFC Converter for Distributed Power Systems", *IEEE APEC*, pp. 130–136, 2001.

[B.34] Q. Ji, X. Ruan, and Z. Ye, "The worst conducted EMI spectrum of critical conduction mode boost PFC Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1230–1241, 2015.

[B.35] J. Yang, J. Zhang, X. Wu, Z. Qian, and M. Xu, "Performance comparison between buck and boost CRM PFC converter," *2010 IEEE 12th Work. Control Model. Power Electron. COMPEL*, 2010.

[B.36] N. B. Nam, N. A. Dung, Y. Liu, Y.-C. Hsieh, H. Chiu, and M. Hojo, "Design and Implementation of Digital Controlled Boost PFC Converter Under Boundary Conduction Mode,", *IEEE IFEEC*, pp. 1114–1119, 2017.

[B.37] W. Zhang, G. Feng, Y. Liu, and B. Wu, "DSP Implementation of Predictive Control Strategy for Power Factor Correction (PFC)," *IEEE APEC*, pp. 67–73, 2004.

[B.38] Y. Yang, Z. Liu, F. C. Lee, and Q. Li, "Analysis and Filter Design of Differential Mode EMI Noise for GaN-based Interleaved MHz Critical Mode PFC Converter," *IEEE ECCE*, pp. 4784–4789, 2014.

[B.39] W. Zhang, G. Feng, Y. F, and S. Member, "Analysis and Implementation of a New PFC Digital Control Method.", *IEEE PESC*, pp. 335-340, 2003.

[B.40] Z. Huang, Z. Liu, Q. Li, and F. C. Lee, "Microcontroller-Based MHz Totem-Pole PFC with Critical Mode Control," *IEEE ECCE*, 2016.

[B.41] Y. Yang, M. Mu, Z. Liu, F. C. Lee, and Q. Li, "Common mode EMI reduction technique for interleaved MHz critical mode PFC converter with coupled inductor," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, vol. 2, pp. 233–239, 2015.

[B.42] Z. Liu, B. Li, F.C. Lee, and Q. Li "Design of CRM AC/DC converter for very high-frequency high-density WBG-based 6.6kW bidirectional on-board battery charger", in *Proc. IEEE-ECCE*, pp. 1030-1038, 2016.

[B.43] J. Muhlethaler, H. Uemura, and J. W. Kolar, "Optimal design of EMI filters for single-phase boost PFC circuits," *IECON Proc. (Industrial Electron. Conf.)*, pp. 632–638, 2012.

C. Overview of state-of-the-art Critical Mode Control for Three-Phase Converters

[C.1] N. Takeuchi, K. Matsui, I. Yamamoto, M. Hasegawa, F. Veda, and H. Mori, "A novel PFC circuit for three-phase utilizing a single switching device," *INTELEC, Int. Telecommun. Energy Conf.*, pp. 2–6, 2008.

[C.2] M. Hartmann, H. Ertl, and J. W. Kolar, "Current control of three-phase rectifier systems using three independent current controllers," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3988–4000, 2013.

[C.3] H. Mao D. Boroyevich, F.C. Lee, "Novel reduced-order small-signal model of three-phase PWM rectifiers and its application in control design and system analysis," *IEEE PESC 2002*, pp. 1–7, 2002.

[C.4] M. Kaufmann, A. Tüysüz, and J. W. Kolar, "New optimum modulation of three-phase ZVS triangular current mode GaN inverter ensuring limited switching frequency variation," *8th IET Int. Conf. Power Electron. Mach. Drives (PEMD 2016)*, no. Pemd, p. 6 .-6 ., 2016.

[C.5] A. Amirahmadi, U. Somani, L. Chen, N. Kutkut, and I. Batarseh, "Variable boundary dual mode current modulation scheme for three-phase micro-inverter," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 650–654, 2014.

[C.6] "Closed-Loop Control Design of Three-Phase Converters."

[C.7] K. Yao, Q. Meng, F. Yang, and S. Yang, "A Novel Control Scheme of Three-Phase Single-Switch Quasi-CRM Boost Rectifier," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6236–6244, 2017.

[C.8] S. Hilti, and D. Boroyevich, "Small-Signal Modeling of Three-Phase PWM Modulators,", in *Proc. IEEE PESC*, pp. 1–7, 1996.

[C.9] D. Leuenberger and J. Biela, "Triangular current mode operation of a three phase interleaved T-type inverter for photovoltaic systems," *PCIM Eur. Conf. Proc.*, no. May, pp. 436–443, 2012.

[C.10] D. Zhang, Q. Zhang, H. Hu, A. Grishina, J. Shen, and I. Batarseh, "High efficiency current mode control for three-phase micro-inverters," *2012 Twenty-Seventh Annu. IEEE Appl. Power Electron. Conf. Expo.*, no. 1, pp. 892–897, 2012.

[C.11] A. Amirahmadi *et al.*, "Hybrid ZVS BCM current controlled three-phase microinverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2124–2134, 2014.

[C.12] J. G. Cho, D. Y. Hu, and G. H. Cho, "Three phase sine wave voltage source inverter using

the soft switched resonant poles," *15th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 48–53 vol.1, 1989.

[C.13] L. Schrittwieser, P. Cortes, L. Fassler, D. Bortis, and J. W. Kolar, "Modulation and Control of a Three-Phase Phase-Modular Isolated Matrix-Type PFC Rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4703–4715, 2018.

[C.14] M. Schweizer, S. Member, and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, 2013.

[C.15] Q. Wang, X. Zhang, R. Burgos, D. Boroyevich, A. White, and M. Kheraluwala, "Design and optimization of a high performance isolated three phase AC/DC converter," *2016 IEEE Energy Convers. Congr. Expo.*, pp. 1–10, 2016.

[C.16] P. Cortes, J. Huber, M. Silva, and J. W. Kolar, "New modulation and control scheme for phase-modular isolated matrix-type three-phase AC/DC converter," *IECON Proc. (Industrial Electron. Conf.*, no. Iecon, pp. 4899–4906, 2013.

[C.17] A. Amirahmadi, H. Hu, A. Grishina, F. Chen, J. Shen, and I. Batarseh, "Hybrid control of BCM soft-switching three phase micro-inverter," *2012 IEEE Energy Convers. Congr. Expo. ECCE 2012*, pp. 4690–4695, 2012.

[C.18] A. Amirahmadi, L. Chen, U. Somani, H. Hu, N. Kutkut, and I. Bartarseh, "High efficiency dual-mode current modulation method for low-power DC/AC inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2638–2642, 2014.

[C.19] J. Muhle Thaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of lcl harmonic filters for three-phase pfc rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, 2013.

[C.20] K. Cai, and Z. Xu, "A novel control method of three-phase single-switch Boost power factor corrector under variable switching frequency," in *Proceedings of International Conference on Power System Technology*, 2002, pp. 565-569.

[C.21] M. Leibl, M. Darani and J. W. Kolar, J. Deuringer "New Boundary Mode Sinusoidal Input Current Control of the VIENNA Rectifier," in *IEEE 2015 Energy Conversion Congress and Exposition*, 2015, pp. 201-209.

[C.22] F. C. Lee and Q. Li, "High-frequency integrated point-of-load converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, 2013.

[C.23] Z. Huang, Z. Liu, Q. Li, F. C. Lee, and F. Xiao, "Critical-Mode-Based Soft-Switching Modulation for Three-Phase Inverters" *IEEE 2017 Energy Conversion Congress and*

Exposition, 2017.

[C.24] Z. Huang, Z. Liu, F. Lee, and Q. Li, "Critical-Mode-Based Soft-Switching Modulation for High-Frequency Three-Phase Bi-Directional AC/DC Converters," *IEEE Trans. Power Electron.*, vol. PP, no. c, p. 1, 2018.

[C.25] I. Term, "A Novel Control Method of Three-phase Single-Switch Boost Power Factor Corrector under Variable Switching Frequency," *IEEE International Conference on Power System Technology*, pp. 565–569, 2002.

[C.26] Q. Wang and R. Burgos, "A Method for Increasing Modulation Index of Three Phase Triangular Conduction Mode Converter," *2018 IEEE 19th Work. Control Model. Power Electron.*, pp. 1–5, 2018.

[C.27] "Vector Representation of Three-Phase Variables Three-Phase Circuits"