# Innovative GTO Thyristor Based Switches Through Unity Gain Turn-Off

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# Through Unity Gain Turn-Off

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## (ABSTRACT)

The Gate Turn-Off (GTO) Thyristor has the best voltage blocking and current conducting capabilities among all known high power semiconductor devices. To improve its dynamic performances to meet the increased demand in high-performance high-power applications, a special driving technique, namely unity gain turn-off, is studied. Several innovative approaches, which realize this driving requirement, are proposed, analyzed and experimentally demonstrated in this dissertation.

The Emitter Turn-Off Thyristor (ETO) is a new family of high power semiconductor devices that is suitable for megawatt power electronics application. ETOs with voltage and current ratings of 4.0~6.0 kV and 1.0~4.0 kA, have been developed and demonstrated. These power levels are the highest in silicon power devices and are comparable to those of the GTO. Compared to the conventional GTO, the ETO has a much shorter storage time, voltage controlled turn-off capability, and a much larger reverse biased safe operation area (RBSOA). These combined advantages make the ETO based power system simpler in terms of dv/dt snubber, di/dt snubber and over current protection, resulting in significant savings at the system level. Experimental and numerical simulation results that demonstrate the advantages of the ETO are presented.

A new family of snubberless turn-off GTO, the Resonant Gate Commutated Thyristor (RGCT) is proposed and investigated. By using a transient high commutation voltage, the RGCT can achieve unity turn-off gain and snubberless turn-off capability even with a relatively high gate loop stray inductance. Therefore conventional GTOs with flexible gate lead can be used to

achieve the state-of-the-art performance similar to that of the Integrated Gate Commutated Turn-Off thyristor (IGCT). Detailed current commutation analysis and experimental results are presented.

A novel equivalent circuit model for the GTO under the unity gain turn-off is proposed. This model is composed of a step current source, which represents the open-base PNP turn-off behavior, in series with a diode that represents the GTO's gate-cathode junction. This equivalent circuit can be used to analyze the turn-off transient behavior of a system employing this GTO.

A new mechanism that dominates the failure of the GTO under the unity gain turn-off condition is identified and analyzed. Innovative hybrid GTO-based devices all have significant gate lead stray inductance. During the turn-off transition, this stray inductor will interact with the turn-off voltage source, the junction capacitance of the GTO's gate-cathode, causing effective current injection into the GTO's emitter junction when the voltage on the device is already high. Design guidelines and solutions for different types of GTO-based hybrid devices are provided.

To my wife, Guoping,

who has given me my first world through her bright smile,

lovely personality,

care and concern for others and keen intelligent conversation.

To my friends,

who have taught me to appreciate the new world.

# Acknowledgements

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# Chapter 1 Introduction

## 1.1    Background

It has been more than fifty years since the first silicon power switch [A1] was developed for practical applications. With their faster switching speed and easier control, power semiconductor switches have won over their traditional mechanical counterparts. In addition, a new engineering field dedicated to the research and application of power conversions---Power Electronics---has been formed and developed based on these advanced power switches [A2].

A power semiconductor switch is a component that can either conduct a current when it is commanded ON or block a voltage when it is commanded OFF through a control. This change of conductivity is made possible in a semiconductor by specially arranged device structures that control the carrier transportation. The time that it takes to change the conductivity is also reduced to the microsecond level compared to the millisecond level of a mechanical switch. By employing this kind of switch, a properly designed electrical system can control the flow of electric energy, shaping the electricity into desired forms. Parameters describing the performance of a power conversion system include reliability, efficiency, size and cost.  The power switch plays an important role in determining these system-level performances [A3]. To facilitate the analysis, a simple buck converter shown in Figure 1-1 (a) is used as an example. There are two switches SW and $D_F$ in the circuit. The purpose of this circuit is to deliver energy from a power source with a higher voltage $V_{CC}$ to the load with a lower voltage $V_O$ requirement. When the power switch SW is on, the energy is delivered from the source $V_{CC}$ through switch SW, inductor L to the load. When the output voltage is high enough, this energy link will be shut down by turning off SW. Energies stored in L and $C_O$ will maintain the load voltage. The typical circuit waveforms are depicted in Figure 1-1 (b). The circuit has four different operating modes: (1) (t0-t1) SW on and $D_F$ off; (2) (t1-t3) SW turn-off and DF turn-on; (3) (t3-t4) SW off and $D_F$ on; (4) (t4-t6) SW turn-on and $D_F$ turn-off.

(a)



(b)
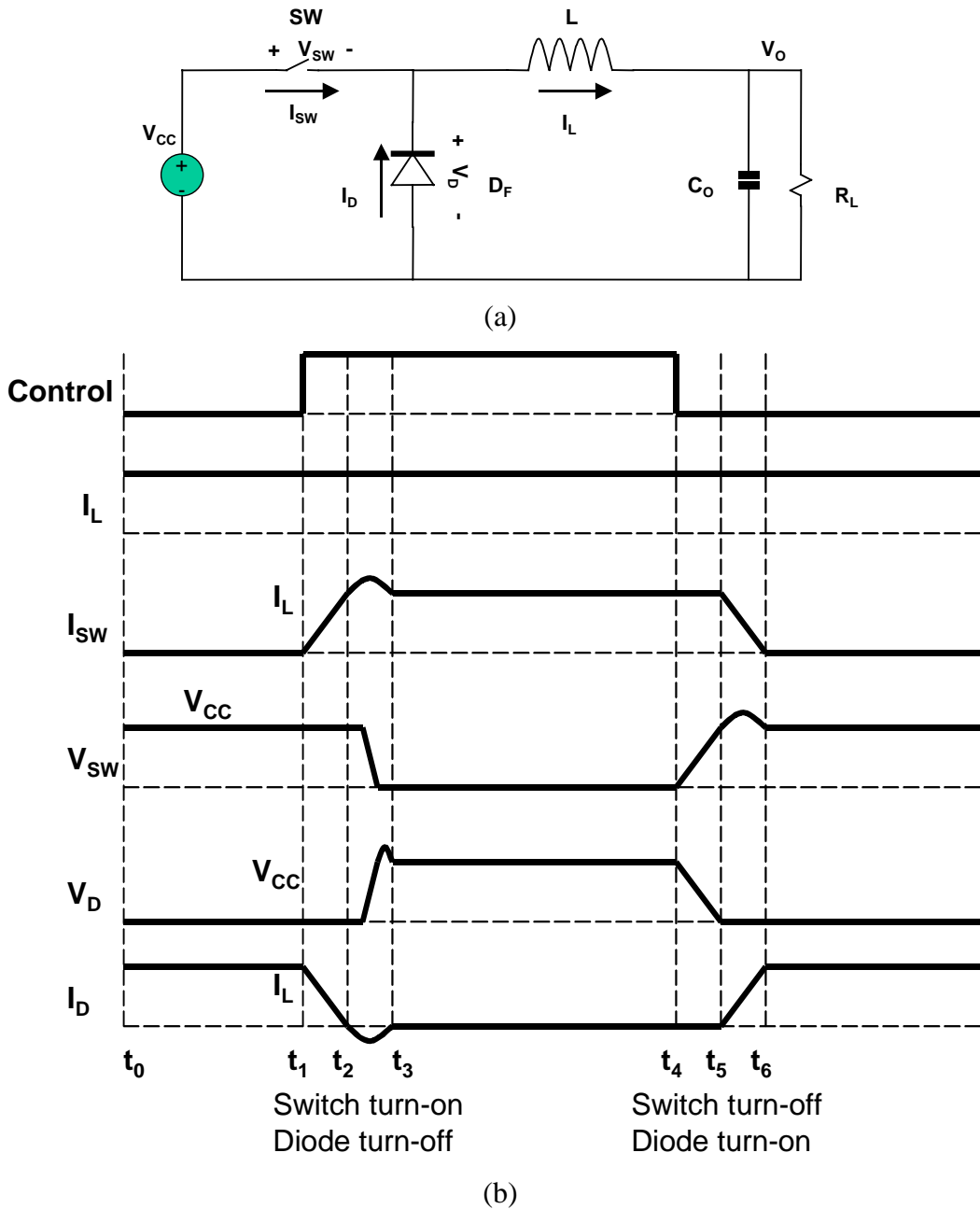
Figure 1-1 (a) Buck converter and (b) its switching waveforms.

Generally, the following parameters are important for a semiconductor switch designed for power conversion applications:

1.  Maximum current carrying capability;

2.  Maximum voltage blocking capability;

3.  Forward voltage drop during "ON" and its temperature dependency;

4.  Leakage current during "OFF";

5.  Thermal capability;

6.  Switching transition times during both turn-on and turn-off;

7.  Capability to stand dv/dt when the switch is "OFF" or during turn-off;

8.  Capability to stand di/dt when the switch is "ON" or during turn-on;

9.  Controllable di/dt or dv/dt capability during switching transition;

10. Ability to withstand both high current and voltage simultaneously;

11. Switching losses;

12. Control power requirement and control circuit complexity.

The above items can be further divided into three categories: static, dynamic and control parameters. Items 1 to 5 regard the static performance of a switch. Both current and voltage ratings describe the power handling capability of a switch. For a certain application, devices with higher current and voltage ratings are more robust to transient over current and voltage due to switching transitions or circuit faults, increasing the system level reliability. For the buck converter, the nominal current of SW when it is on is equal to the current of the output inductor. However, SW will experience higher peak current during the turn-on period between t2 and t3 due to diode $D_F$ reverse recovery. When the load $R_L$ is shorted or $D_F$ is fail shorted, SW will observe a much higher fault current.

Lower forward voltage drop and leakage current lead to a lower power loss, which is good from the energy efficiency and the thermal management point of view. Between t0 and t1, SW is on and its power dissipation is ($I_L V_F$), where $V_F$ is the forward voltage drop of SW. Between t3 and t4, SW is off and its power dissipation is ($V_{CC} I_{LKG}$), where $I_{LKG}$ is the leakage current of SW. Good thermal capability, which refers to the thermal resistance from the device to ambient and the maximum temperature the device can withstand, allows the device to operate at its full power rating instead of being limited by the thermal management.

Items 6 to 11 are related to the dynamic performance of a switch. Short transition times are required in order to increase the switching frequency and reduce the switching loss. The latter is caused by the overlap of current and voltage on the switch. For the buck converter, the turn-on

transition time of SW is (t3-t1) and the turn-off transition time is (t6-t4). The switch's current/voltage overlaps, hence its switching losses are approximately proportional to the switching times. Item 7 describes the external dv/dt immunity of the device. In a system, the switch is generally exposed to a complex electromagnetic environment. However, the state and the operation of the switch should only be controlled by its control command instead of the environment. When the switch is in the OFF state or during turn-off operation, the switch should stay OFF or continue its turn-off process no matter what the external dv/dt across its anode and cathode (or collector/emitter) is. Similarly, there is a di/dt requirement when the switch is "ON" or during the turn-on transition. Devices with a large cell size such as the Gate Turn-Off (GTO) thyristor have lower di/dt limitations because of longer time required for uniform current distribution.

While a good switch should be able to withstand severe dynamic voltage and current changes, it should also be able to provide the system with an acceptable electromagnetic noise. This requires the controllable di/dt and dv/dt capabilities from the switch [D1]. A typical *turn-on* operation of a switch in a power conversion system is associated with a *turn-off* process of another switch (or diode). The di/dt is generally determined by the *turn-on switch* and shared by the *turn-off switch*, which may not be able to withstand the high di/dt. For example, a diode has a turn-off problem and high turn-off di/dt may over-stress it. In the buck converter, the turn-off of the diode $D_F$ is accompanied with the turn-on of SW starting from t1. $D_F$'s falling di/dt is equal to that of SW's rising di/dt. After t2, $D_F$ enters its reverse recovery process, experiencing its highest instant power before its current finally goes to zero. To effectively protect these associated devices, the maximum turn-on di/dt should be limited. Similarly, a typical turn-off operation of a switch in a power conversion circuit is associated with a turn-on process of another switch (or diode). The dv/dt is generally determined by the *turn-off switch* and shared by the *turn-on switch*, which may not be able to withstand the high dv/dt. The maximum dv/dt of the active-switch should be limited to protect the associated switches. Both dv/dt and di/dt controls normally require a device to possess a Forward Biased Safe Operation Area (FBSOA) [A4]. The FBSOA defines a maximum V-I region in which the device can be commanded to operate with simultaneous high voltage and current. The device current can be controlled through its gate (or base) and the length of the operation is only limited by its thermal limitation. Devices with FBSOA normally

have an active region in which the device current is determined by the control signal level as is shown in Figure 1-2. It should be noted however, that di/dt control normally means slowing down the transient process and increasing the turn-on loss.
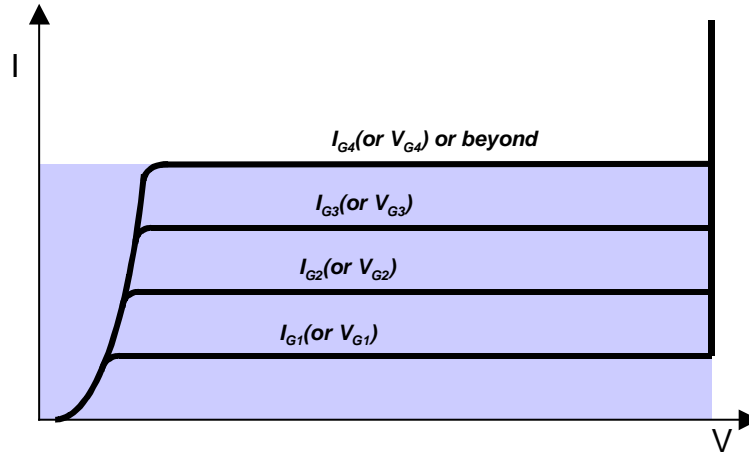


Figure 1-2 Forward I-V characteristics of a device and its FBSOA (shaded area) definition. The control of the device may be current or voltage.

During a typical inductive turn-off process, the voltage of a switch will rise and its current will decrease. During the transition, the device observes both high voltage and high current simultaneously. Figure 1-3 depicts the typical voltage-current trajectory of an inductive turn-off process as is the case in the buck circuit shown in Figure 1-1 between t4 and t6 in time domain. The device's current maintains constant while its voltage rises. Its current begins to decrease once its voltage reaches its nominal value. The voltage spike is caused by the di/dt and stray inductance in the current commutation loop. On the device's I-V plane, the curve that defines the maximum voltage and current boundary within which the device can turn-off safely, is referred to as the Reverse Biased Safe Operation Area (RBSOA) [B1] of the device. Obviously, a device's RBSOA should be larger than all its possible turn-off I-V trajectories. Devices without a large enough RBSOA need an external circuit (such as an auxiliary soft-switching circuit or a dv/dt snubber) to shape their turn-off I-V trajectories to a smaller one to ensure safe turn-off operation. Devices with turn-off snubbers can therefore survive with a much smaller RBSOA. However, a dv/dt snubber increases the system's component count, hence the system's size, cost.

The turn-off operation conducted without the help of a snubber is called snubberless turn-off or hard turn-off, while a process with the help of a snubber is called snubbered turn-off process.
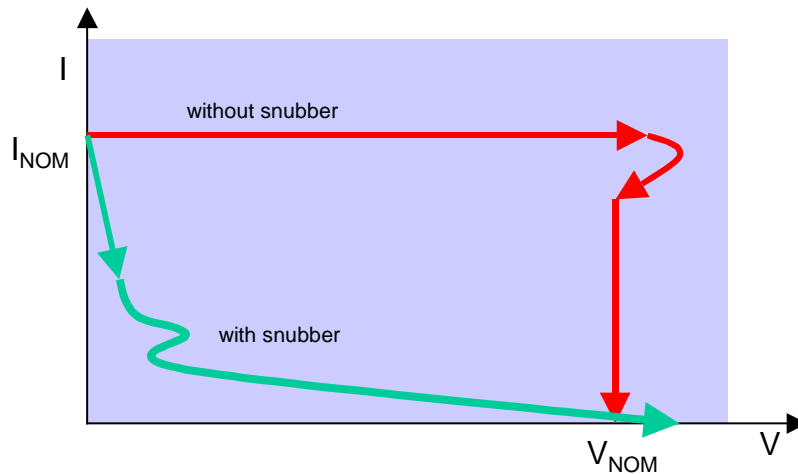


Figure 1-3 Turn-off I-V trajectories of a device under typical inductive load condition with and without a turn-off snubber.

During the turn-on transition, a switch will also observe both high voltage and high current simultaneously. Figure 1-4 depicts the typical voltage-current trajectory of an inductive turn-on process as is the case in the buck circuit shown in Figure 1-1 between t1 and t3 in time domain. The device's voltage stays constant while its current increases until it hits the device's nominal current level. The current overshoot is due to the reverse recovery of an associated diode (or a switch). A device without large enough FBSOA needs an external snubber circuit to help its I-V trajectory as is shown in Figure 1-4. The stress on the device can be significantly reduced with the turn-on snubber. However, a turn-on snubber circuit also increases a system's component count, size and cost.

Item 10 defines the capability of a switch to withstand high instant power. However, this capability during turn-on and turn-off will be different for a semiconductor device due to the difference in free carrier distribution. RBSOA is mostly used to describe a device's turn-off capability, while FBSOA is used to measure the turn-on capability of a device. FBSOA, implied by its name, is also used to measure a device's capability to withstand high voltage and high current under DC and short circuit conditions.
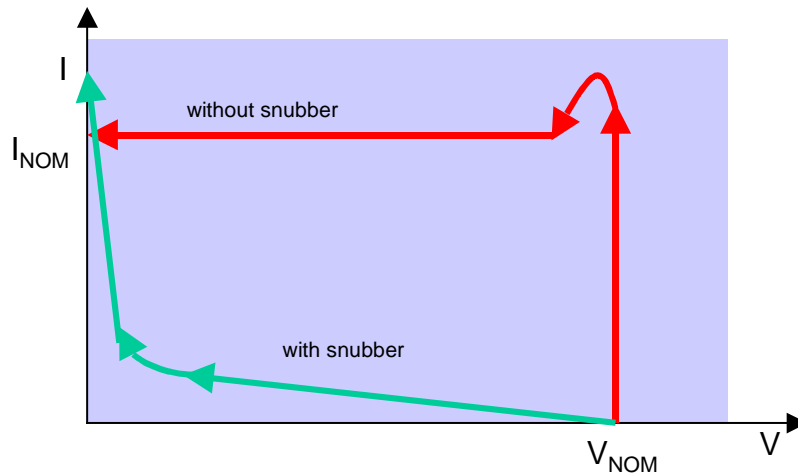
Figure 1-4 Turn-on I-V trajectories of a device under a typical inductive load condition.

A load short circuit is a threat to the device that is ON in a typical circuit. A temporary load short can introduce an extremely high current that generates high instant power dissipation, leading to the failure of the switch.  To effectively protect the switch under a "short-circuit" condition, the capability to limit its maximum current at a given DC voltage is required. In this case, the peak instant power is $(V_{CC}I_{LIM})$ while for the device without this capability is $(V_{CC}^2/r)$, where $V_{CC}$ is the DC voltage, $I_{LIM}$ is the device's maximum current limitation and $r$ is the effective resistance of a device while it is ON. Since $r$ is normally low in a practical device, the instant power of a device under a load short circuit without the maximum current limitation is much higher. Figure 1-5 shows the I-V characteristics during the ON state for devices with or without the self current limitation capability.

The ability for a switch to limit its maximum current regardless of the voltage applied is an effective method to limit its instant power. A device with FBSOA capability normally has the self current limiting capability, hence can survive a short-circuit fault for a short time determined by its thermal limitation [D2].
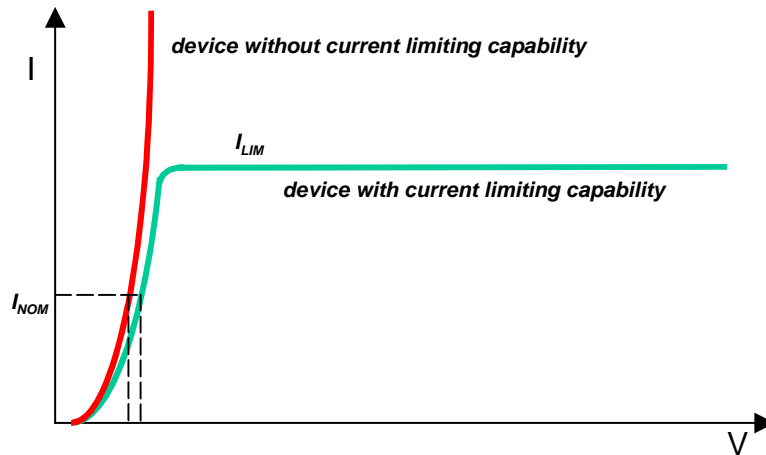
Figure 1-5 Forward I-V characteristics of two type of devices with / without self current limiting capability.

The first power semiconductor switch that was put in use was the Silicon Controllable Rectifier (SCR) [A1] invented in 1950s. The SCR is a latch-up device with only two stable states: ON and OFF. It does not have FBSOA. It can be switched from OFF to ON by issuing a command in the form of a small gate-triggering current. This will initiate a positive feedback process that will eventually turn the device on. The SCR has a good trade-off between its forward voltage drop and blocking voltage due to the strong conductivity modulation provided by the injections of both electrons and holes. Moreover, an SCR's structure is very simple from the manufacturing point of view because its gate can be placed at one small region. The size of a single SCR can therefore be easily expanded to increase the current capability of the device without too many processing problems. 8.0kA/10.0kV SCRs are commercially available utilizing a six-inch silicon wafer for current conduction. However, SCRs cannot be turned off through their gate controls.

Because of the limitation of the turn-off controllability of the SCR, the Gate Turn-Off (GTO) Thyristor [B2] was subsequently developed. As its name denotes, a GTO is a device that can be turned off through its gate control. Its basic structure is very similar to that of a SCR. However, many gate fingers are placed in the GTO surrounding its cathode. During a turn-off operation, the latch-up mechanism can be broken through the gate control.

A GTO is thus a device with full gate control and similar high current/voltage rating of an SCR. To date, the GTO has the highest power rating and the best trade-off between the blocking voltage and the conduction loss of any fully controllable switch. However, GTOs' dynamic performance is poor. A GTO is slow in both turn-on and turn-off. It lacks FBSOA and has poor RBSOA so it requires snubbers to control dv/dt during the turn-off transition and di/dt during turn-on transition.

As the earliest controllable switch, the Bipolar Junction Transistor (BJT) [B3] had been the workhorse device for power conversion applications up until a decade ago. The dynamic performance of the BJT is much better than that of the GTO. The switching speed of a BJT is also faster than the GTO; it typically does not require dv/dt and di/dt control during turn-off and turn-on. It also has a good FBSOA so its di/dt and dv/dt can be controlled at switch level without snubber circuits. However, the power BJT has several limitations in its static and dynamic characteristics. It is a current controlled device with a relatively low gain. This causes difficulty in simplifying the control circuitry. The trade-off between its blocking voltage and its forward voltage drop is poor. There are almost no power BJTs being designed beyond 1.5kV with a good forward voltage drop. The well-known second breakdown of a power BJT significantly limits its RBSOA and FBSOA [B4].

Both the BJT and the GTO are current driven so they require significant control power. This is a big issue for high-frequency applications. On the contrary, the power MOSFET [D3] is a voltage-controlled device requiring virtually no control power. It also has an excellent dynamic performance due to its ***majority-carrier current conduction*** mechanism. Although its power ratings (both current and voltage) are difficult to increase, the power MOSFET has become a nearly perfect power switch for applications below 600V. The key merits of the MOSFETs can be summarized as below:

1.  Very fast switching speed and very short switching transition time;
2.  Excellent FBSOA and RBSOA;
3.  Good di/dt and dv/dt controlability;
4.  Voltage control.

The major limitation of a power MOSFET is that its conduction loss increases as the square of its blocking voltage.

When the development of power MOSFETs encountered difficulty in increasing their current handling capability, the idea of a MOS controlled BJT was developed to overcome the problem. This effort led to today's Insulated Gate Bipolar Transistor (IGBT) [D4].  The IGBT fundamentally changes the BJT's current control into voltage control while maintaining BJT's advantages. In addition, the use of a wide-base PNP transistor in the IGBT structure results in a much better conductivity modulation effect than a conventional BJT, pushing the voltage rating of the IGBT toward the level of GTOs. The internal PNP structure also does not have the second breakdown problem as a conventional NPN structure because the high voltage is supported by the base region of the PNP transistor instead of by the collector region as is the case for a conventional NPN transistor. IGBTs also have excellent RBSOA and FRSOA. Having undergone several years' development, IGBTs have become the best device for applications in the range of 600V to 3000V.

Although there are a number of other devices that have been developed or are being developed, the workhorse power semiconductor devices today are SCRs, GTOs, MOSFETs and IGBTs. Each of these devices dominates a special power arena. The MOSFET has excellent dynamic and static performance. It rules low voltage applications below 600V. The IGBT is slower than the MOSFET but has better forward voltage drop at above 600V. It rules applications from 600V to 3000V. At an even higher voltage level, the GTO becomes the dominant device with better current carrying capability but much slower dynamic response. Without turn-off capability, the SCR has an even better current conduction capability, so it is suitable for even higher power AC applications where the gate-controlled turn-off capability is not necessary.

For a typical application, the switching frequency is an important index in determining the system performance. Generally, the higher the switching frequency, the better the system's dynamic performance, the smaller the system's size due to reduced passive components and the lower the system's cost due to savings on passive components. The practical switching frequency of an application system is a trade-off of many issues including maximum device switching

frequency, maximum magnetic switching frequency, switching losses of the power switches, overall system efficiency, etc. In the low power field where the MOSFET plays the major role, the switching frequency is normally subject to system efficiency and/or magnetic considerations instead of devices' limitation. In the medium power field where the IGBT plays the major role, the situation changes. At the lower end, the limitation of the device does not dominate since the lower rating IGBT is normally fast enough. However, when the power rating is higher, the IGBT's switching speed decreases and the switching losses increase significantly. The practical switching frequency is thus subject to the limitation of the device. When the power level moves even higher, the GTO is the only available device. Since it has several tens of microseconds switching time, significant turn-off and dv/dt snubber loss, the GTO is traditionally the limitation of the system's switching frequency.

The above trend shows that when the power level moves higher, power semiconductor devices limit the maximum system switching frequency, hence the system's performance, especially at the GTO level. To meet the increasing demand for better performance in high power systems, many efforts have been made to improve the performance of high power semiconductor devices. Among them, one effort is to push the IGBT toward higher power ratings based on the module concept. With its good dynamic performance, high power systems equipped with IGBTs can operate at a much higher switching frequency and have many benefits compared to a conventional GTO system. The state-of-the-art IGBT rating is currently 3.3kV/1.2kA [D5], which is at the low end of that of the GTO.

Another effort to pursue better high power devices is to improve the dynamic performance of the traditional high power GTO. The study to improve the dynamic performance of a GTO has been conducted since it was invented. It has been shown that the performance of a GTO thyristor significantly changes when its gate-driving condition changes. Efforts to incorporate the better drive technology at the silicon level have led to the study of MOS Controlled Thyristors (MCTs) [A5]. Monolithic integration is definitely the best solution, however, since there are too many trade-offs in the MCT design, in particular the RBSOA limitation of a large area MCT [A6], the achieved device ratings were far below what was expected. Another method to achieve this better drive is through hybrid integration. By integrating GTO and MOSFET/IGBT at die level

or even at packaged device level, new high power devices can be developed with much better performance and lower cost because each of these has been designed and optimized for their best performance.

This dissertation is dedicated to the development of innovative high power semiconductor devices through hybrid integration of high power GTOs with low voltage power MOSFETs.

## 1.2   Dissertation outline and major results

### 1.2.1   The performance of the GTO under unity gain turn-off

This chapter summarizes the fundamentals of traditional GTO operation and then systematically studies the performance of a GTO under the condition of unity gain turn-off. Prior research results and the most recent development in IGCT and MTO are also summarized.

### 1.2.2   The principle of the Emitter Turn-Off (ETO) Thyristor

Based on the unity turn-off gain theory, a new driving method that improves the performance of the GTO is investigated. Through hybrid integration, the Emitter Turn-Off (ETO) thyristor  is proposed. The operational principle of the ETO is introduced. The advantages and drawbacks of the ETO compared to the GTO are identified. Two-dimensional device-level simulation is conducted to understand the physics of the ETO.

### 1.2.3   Experimental demonstration of the ETO

Based on the ETO theory, experimental high power ETOs were developed by using commercially available GTOs and MOSFETs. The mechanical and electrical layout of the ETO is optimized to minimize the ETO gate loop stray inductance $L_G$, which is crucial to the achievement of the unity turn-off gain. Experimental results attest the predicted advantages of the ETO, which include voltage-controlled turn-off, fast switching speed, much higher maximum turn-off current capability and better turn-on performance. To simplify the analysis, a simplified GTO equivalent circuit model for the turn-off transient is proposed. The unity turn-off gain, which is crucial to the performance of the ETO, is also experimentally verified.

### 1.2.4    Snubberless turn-off capability of the ETO

The snubberless turn-off capability is a very important feature for modern power semiconductor switches. The ETO has better RBSOA that can lead to the snubberless turn-off capability. In this study, a special snubberless turn-off failure mechanism, which is related to the ETO's hybrid structure and is applicable to the IGCT and MTO, is identified and analyzed.

### 1.2.5    ETOs in parallel and series connection

By dramatically decreasing the storage time, ETOs have a much better match in storage time. Storage time dispersion of less than ±100nsec is normal for ETOs and can be further reduced through adjustment of the emitter switch gate resistance. Thus, the capacitance required for dynamic voltage balancing in an ETO series connection is significantly reduced. Uniform current sharing for parallel connected ETOs is also guaranteed at the device level by the open-base PNP turn-off mechanism. The current balancing inductance can be essentially removed. Theoretical analysis and experimental results of parallel and series connection ETOs are presented.

### 1.2.6    The Resonant Gate Commutated Thyristor (RGCT)

To realize the unity gain turn-off, the turn-off current commutation rate should be high enough. There are two factors that affect this rate: the gate loop stray inductance $L_G$ and the maximum applicable turn-off voltage $V_{OFF}$. $L_G$ is determined by the device's physical structure while $V_{OFF}$ is traditionally lower than the GTO gate-cathode breakdown voltage, which is about 20V. A novel approach that makes use of a transient high voltage for the current commutation is proposed. A family of RGCTs are derived and studied. The best topology is then identified. This RGCT also benefits the turn-on process by sharing the resonant capacitor charging current with the turn-on of the RGCT.

### 1.2.7    Snubberless turn-off of a Diode Assisted Gate Turn-Off Thyristor (DAGTO)

Realizing that the blocking voltage of the gate-cathode junction of the GTO sets the limitation of the maximum turn-off voltage that can be used for the current commutation, the DAGTO uses a discrete diode in series with the GTO cathode to increase this voltage. The maximum turn-off voltage for the DAGTO thus can be as high as the sum of the two diodes' blocking voltage.

Crucial issues including the selection of the turn-off voltage and the effect of the junction capacitance are studied. An experimental DAGTO has been implemented and demonstrated.

### 1.2.8   Conclusions

This chapter summarizes the major contributions made during the course of this study.

# Chapter 2 The Performance of the GTO Under Unity-Gain Turn-Off Condition

## 2.1    Introduction

The GTO thyristor was one of the very first power semiconductor switches with full gate control. It has served many power applications ranging from low power (below 100 watts) in its early years to high power up to hundreds of megawatts. A state-of-the-art GTO can be fabricated on a silicon wafer as big as 6 inches and can be rated up to 6.0 kA and 6.0 kV [L3]. This rating is much higher than the ratings of any other fully controllable devices.

The GTO's static parameters are excellent: low conduction loss due to double-sided minority carrier injection, high blocking voltage and low cost due to the capability of fabrication on a large single wafer. However, its dynamic performance is poor. The requirements of a dv/dt snubber during turn-off operation, a di/dt snubber during turn-on operation and minimum on and off times make the GTO difficult to use. To improve the dynamic performance of the GTO while keeping its good static performance, a better understanding of the mechanism of the GTO is necessary. In this chapter, the basic operation principle of the GTO, its advantages and disadvantages, and the mechanism that determines its performance are summarized and discussed. A new gate-driving concept, namely unity-gain turn-off, is then introduced. The advantages through this special driving method are analyzed and discussed. Finally, all known approaches that make use of this special driving technique are summarized.

## 2.2    GTO forward conduction

Figure 2-1 (a) shows the cell structure and the doping profile of a typical high power GTO. It is a three terminal, four-layer PNPN structure with a lightly doped N⁻ voltage-blocking layer in the center [B5]. The electrode on the external P+ layer is called the anode where the current is normally flowing into the device. The electrode on the external N+ layer is called the cathode from where the current is normally flowing out. The electrode on the internal P layer (p-base) is called the gate, which is used for control.

The operation principle of a GTO can be understood through its equivalent circuit model shown in Figure 2-1 (b). The PNP transistor represents the GTO's top three layers, while the NPN transistor represents the GTO's bottom three layers. Since the n⁻ layer serves as the base of the PNP and the collector of the NPN, and the internal P layer serves as the base of the NPN and the collector of the PNP, the two transistors are cross coupled. This structure has two stable states: ON and OFF, which are determined by its gate control. When a current is injected into the GTO from its gate to its cathode, the NPN structure will be turned on and its collector current will be flowing from the anode of the GTO through J1 junction. Since J1 is the emitter junction of the PNP structure, the collector current of the PNP is then the base current of the NPN. The two transistors therefore provide base currents to each other, forming a positive feedback among them until they reach a self-sustaining state commonly known as latch-up or latched. Under the latched condition, high level minority carrier injections are available from the anode to the cathode, with all three PN junctions forward biased.  A high conductivity therefore exists from anode to cathode, allowing high current to flow from the anode to the cathode. Figure 2-2 illustrates this turn-on process.

At the silicon level, the turn-on of junction J3 results in the injection of electrons into the p-base region. These electrons diffuse across the p-base and are mostly collected by the reverse biased junction J2. To maintain the continuity of the current, junction J1 will supply a current by injecting holes into the n⁻ region. Part of these holes will diffuse across the n⁻ region and are collected by junction J2, resulting in more electron injection from junction J3. When both transistors operate at sufficient current gain, a positive feedback mechanism is sufficient to result in the latch-up.

(a)



(b)



(c)
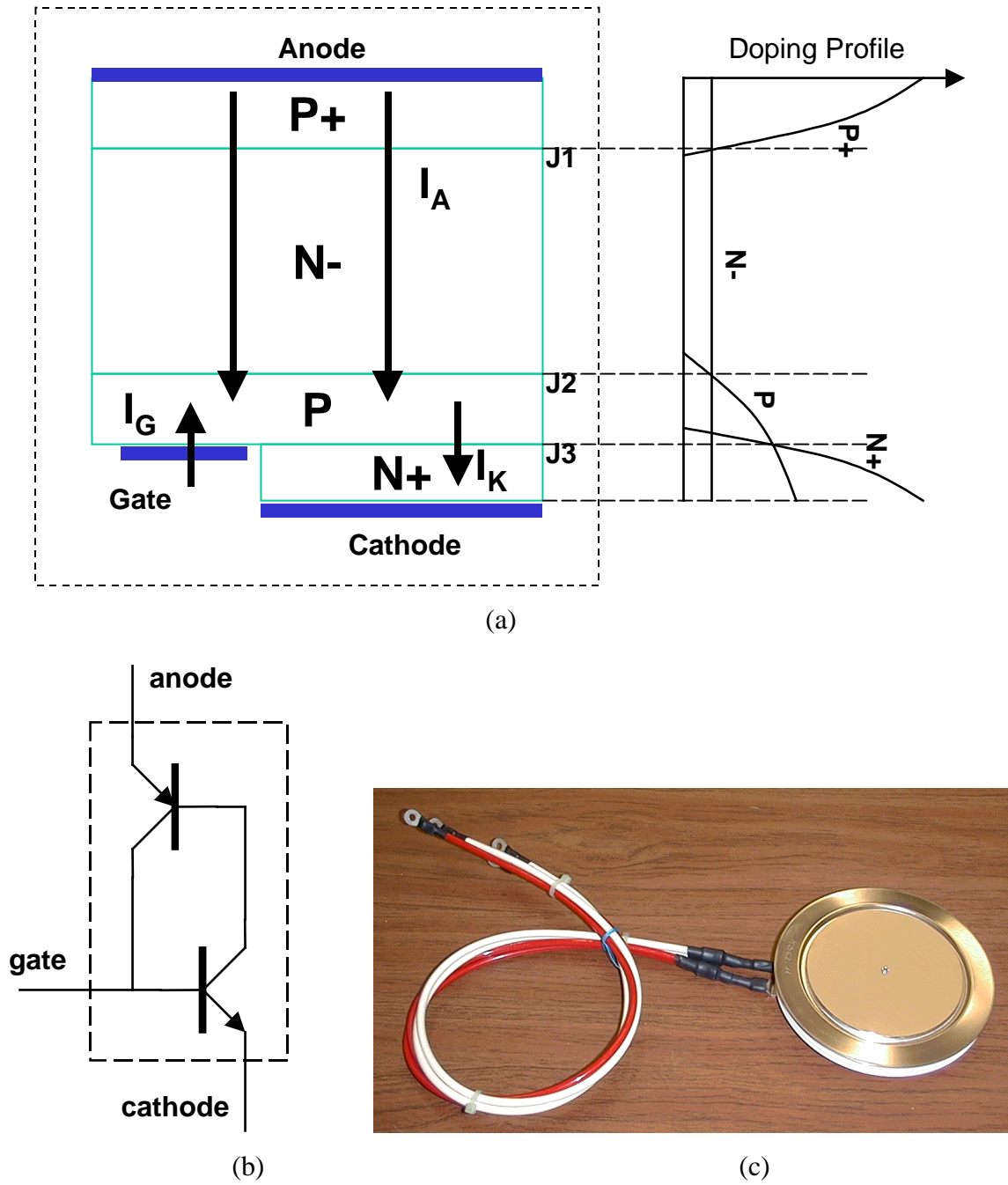
Figure 2-1 (a) GTO cell structure and its doping profile; (b) The GTO's equivalent circuit model;

(c) A photo of a four-inch GTO along with its gate lead.
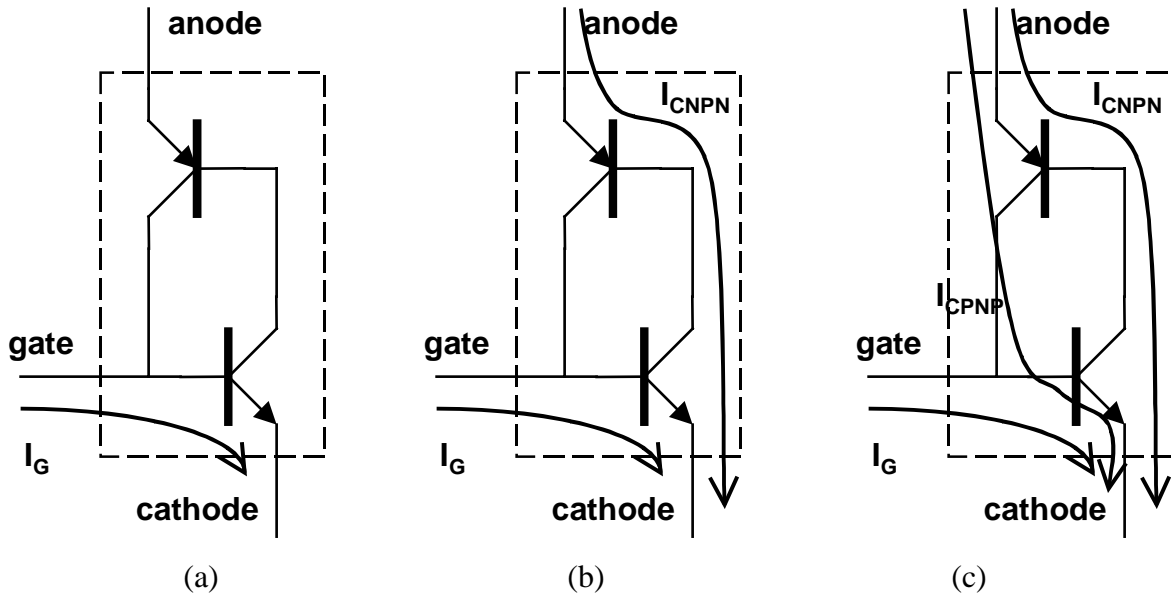
Figure 2-2 Turn-on and current sustaining process in a GTO.

Let the common base current gain of the PNP and NPN be $\alpha_{PNP}$ and $\alpha_{NPN}$ respectively. Normally $\alpha_{PNP}$ is lower than $\alpha_{NPN}$ since the PNP is a wide base structure. The current flow inside a GTO is illustrated in Figure 2-3. At junction J2, the current due to cathode side injection is $\alpha_{NPN}I_K$; the current due to anode side injection is $\alpha_{PNP}I_A$; the leakage current is $I_L$. According to Kirchhoff's law:

$$I_A = \alpha_{PNP}I_A + \alpha_{NPN}I_K + I_L \qquad (2\text{-}1),$$

and

$$I_A = I_K - I_G \qquad (2\text{-}2).$$

Combining these equations:

$$I_A = (\alpha_{PNP}I_G + I_L)/(1 - \alpha_{PNP} - \alpha_{NPN}) \qquad (2\text{-}3).$$

This equation shows that the thyristor structure can sustain its anode current by itself once the sum of both transistors' common base current gain ($\alpha_{PNP} + \alpha_{NPN}$) is approaching unity. For a GTO, $\alpha_{NPN}$ is designed low and is normally depending on $I_G$ to ensure its gate turn-off capability. This will be discussed later.
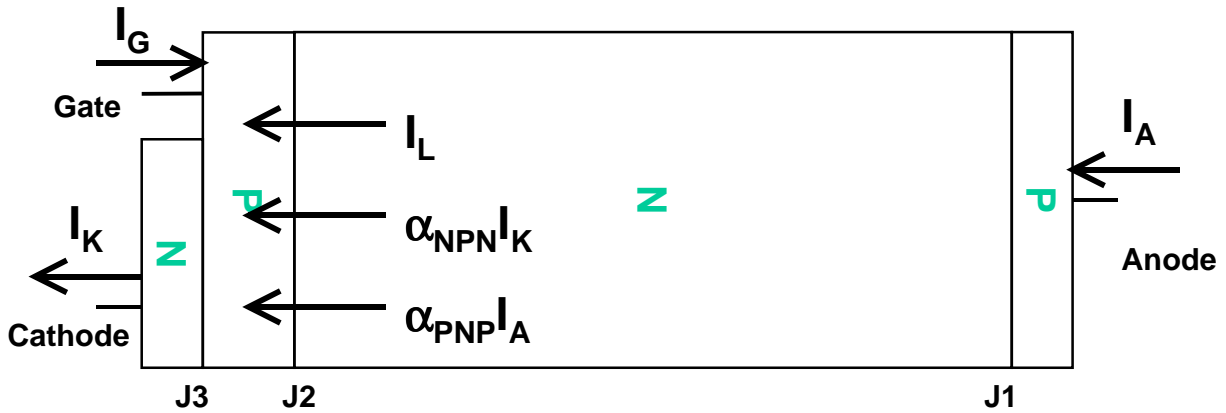
Figure 2-3 Current flow in a GTO with gate drive current.

With this self-sustaining capability, the gate of a GTO does not need to supply a lot of current and does not need to be very close to its cathode as is in a BJT design. The dimension of a typical GTO cell shown in Figure 2-1 (a) is 100~150μm wide. This is very large compared to the micron and/or even sub-micron process used for modern MOSFETs and IGBTs. The large cell size design is cost-effective and makes it possible to fabricate large single die devices to boost their current capability. A state-of-the-art GTO die is as big as 6-inch in diameter with a turn-off current capability of up to 6.0 kA [L3].

The large cell structure introduces a current spreading problem during the turn-on transition of a GTO. When a gate current is injected, the turn-on occurs first in the vicinity of the gate contact. The conduction area then spreads across the rest of the cathode area. This can be characterized by a propagation velocity called the **_spreading velocity_** [B6]. Experimental measurements [B7] have shown a typical spreading velocity of 5000cm/sec. This velocity depends upon the GTO design parameters, the gate turn-on injection current and its $dI_G/dt$.

Because of this spreading velocity, it takes time for the whole GTO cell to turn on. To avoid overstressing the part of the cell that is turned on first, the increasing rate of the anode current should be limited. This sets the maximum turn-on di/dt limitation for a GTO.

The major advantages of the GTO are its low forward voltage drop and high voltage blocking capability. These can be understood as the benefit of its double-side minority carrier injection

mechanism. For high voltage devices, the forward voltage drop is mainly determined by the resistive voltage drop in the voltage-blocking region where minority carriers play an important role. Figure 2-4 (d) shows the minority carrier distribution in the n⁻ region of an IGBT and Figure 2-4 (c) shows the case of a GTO. For the same blocking voltage design, their n⁻ regions should have similar width and doping. Since there is only one transistor in the IGBT structure, minority carriers can only be injected from one side so the conductivity modulation in the n⁻ region is weaker than that of the GTO. In the GTO, since there are two transistors, minority carriers can be injected from both ends, making a more uniform plasma distribution in the whole area. For a 4.5 kV state-of-the-art GTO, its forward voltage drop at a current density of 50 A/cm$^2$ can be as low as 2.0 V [L2] if a constant gate current injection presents. Figure 2-5 shows the on state characteristics of an state-of-the-art GTO manufactured by ABB [L2].



(a) GTO circuit model.          (b) IGBT circuit model.



(c)                              (d)
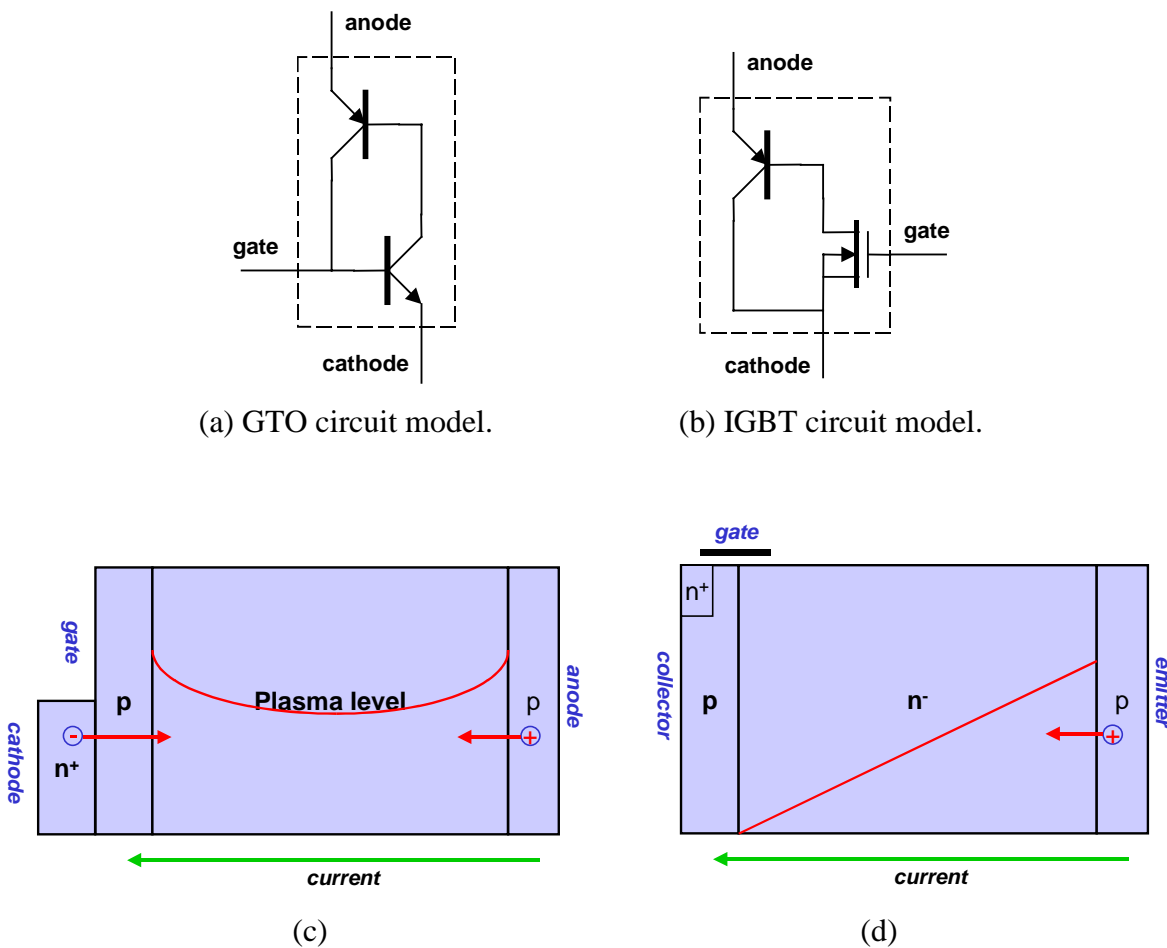
Figure 2-4 On-state minority carrier distribution in the voltage blocking region for (a) GTO and (b) IGBT.

## 2.3    GTO turn-off and forward blocking

If the gate is pulling out current from the GTO, the current injection into the NPN base will be reduced.  Once this is reduced below a certain level, the collector current of the NPN hence the base current of the PNP will also decrease, leading to the reduced PNP collector current. This will further reduce the base current of the NPN since it is the difference between the collector current of the PNP and the gate pullout current. This positive feedback process will eventually turn off the GTO.
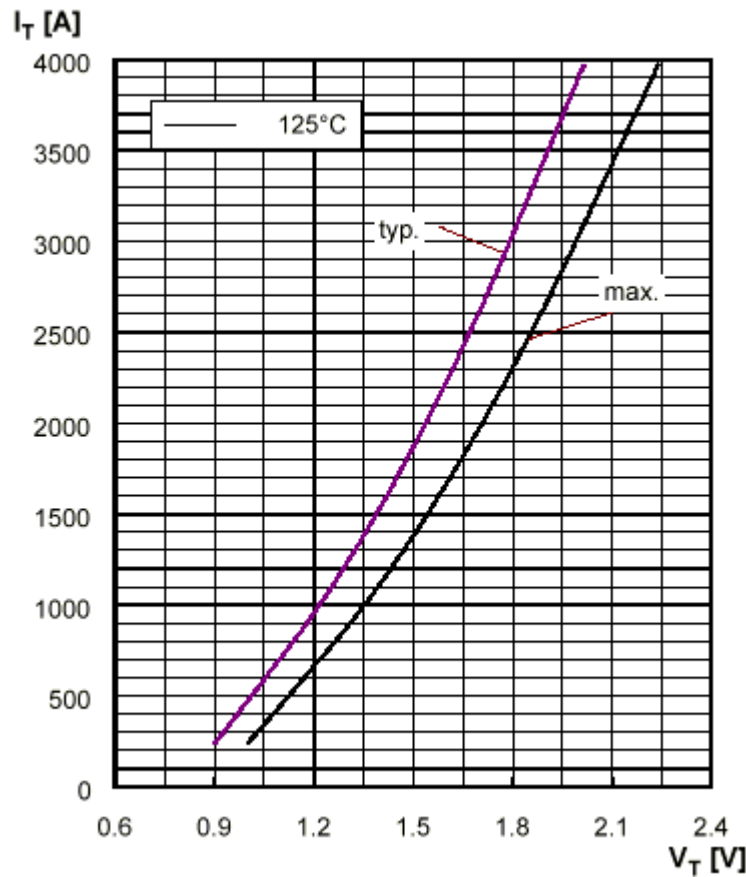
Figure 2-5 On state characteristics of 5SGT 40L4502, a 4.5kV GTO from ABB.

Figure 2-6 shows the current flow inside the GTO when its gate is pulling out current to turn off the device. The base drive current required to maintain current conduction in the NPN transistor is $(1-\alpha_{NPN})I_K$. The base drive current available to the NPN transistor in this case is $(\alpha_{PNP}I_A-I_G)$. Thus the condition to turn-off the GTO through the gate control is given by:

$$\alpha_{PNP}I_A - I_G < (1 - \alpha_{NPN})I_K \qquad\qquad (2\text{-}4).$$

Since

$$I_K = I_A - I_G \qquad\qquad (2\text{-}5),$$

so the condition to turn-off the GTO is:

$$I_G > \frac{(\alpha_{PNP} + \alpha_{NPN} - 1)}{\alpha_{NPN}} I_A \qquad\qquad (2\text{-}6).$$
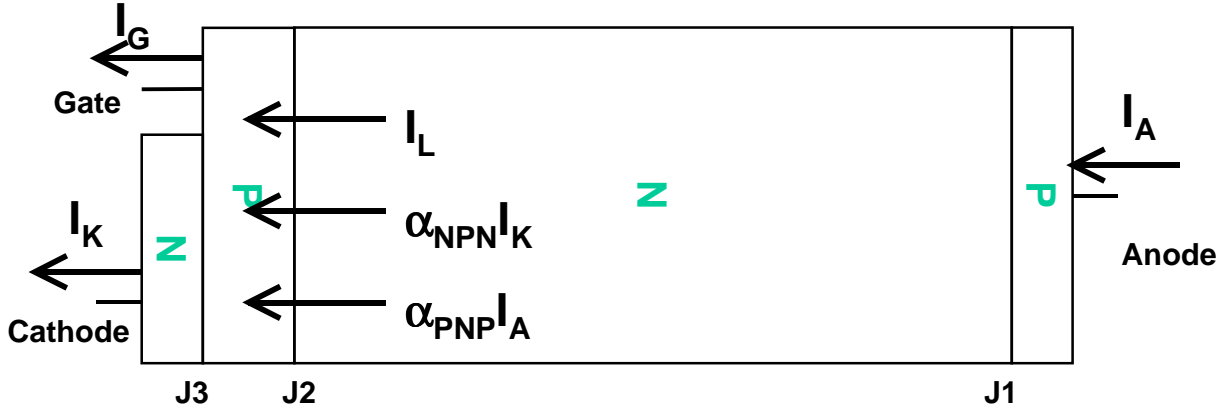


Figure 2-6 Current flow inside the GTO when its gate is pulling out current.

The ratio of the anode current to the gate current at which level a GTO is turned off is defined as the turn-off gain. From (2-6), the maximum turn-off gain [B5] an be expressed as;

$$\beta_m \equiv \frac{I_A}{I_G} = \frac{\alpha_{NPN}}{\alpha_{PNP} + \alpha_{NPN} - 1} \qquad\qquad (2\text{-}7).$$

A large turn-off gain is normally desirable to reduce the gate driver requirements. Lower $(\alpha_{PNP} + \alpha_{NPN})$ value is necessary to ensure a reasonable turn-off gain. It is also important to point out that $\alpha_{NPN}$ in (2-7) is not a constant, normally it decreases when gate current $I_G$ increases.

When a GTO is OFF, its junction J2 is reverse biased and can support a high voltage applied between its anode and cathode as is shown in Figure 2-7 (a). If the junction J3 is reverse biased or shorted by the gate driver, the GTO's maximum forward blocking voltage $BV_{AK}$ is determined by the avalanche breakdown capability of the PNP transistor under the open-base condition [B8]. This voltage can be expressed as:

$$BV_{AK} = (1 - \alpha_{PNP})^{\frac{1}{n}} BV_{J2} \qquad\qquad (2\text{-}8)$$

where $\alpha_{PNP}$ is the common base current gain of the PNP structure at low current levels; n is an empirical constant and $BV_{J2}$ is the avalanche breakdown voltage of the PN junction J2. Since this PNP has a wide base structure, its common base current gain $\alpha_{PNP}$ is low compared to a normal bipolar transistor. Thus the forward voltage blocking capability $BV_{AK}$ of a GTO is very close to the breakdown voltage of junction J2.
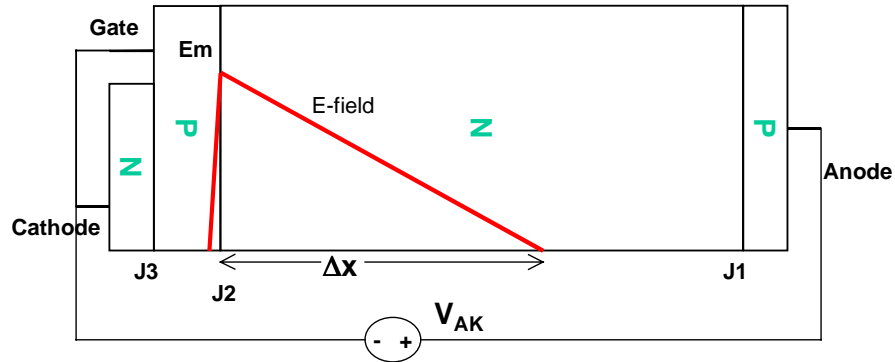


(a) The GTO is in forward blocking state.
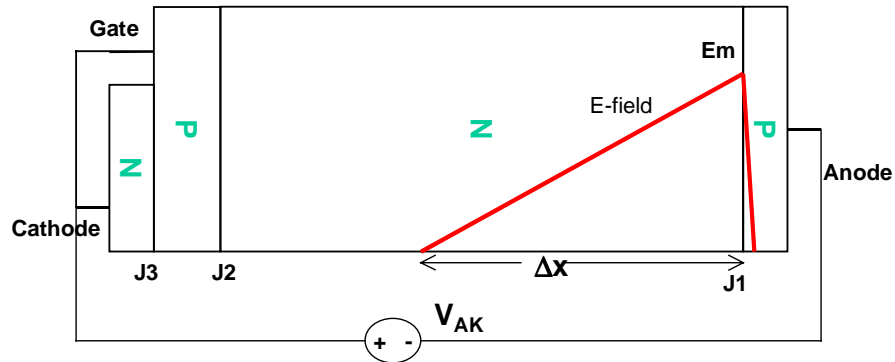


(b) The GTO is in reverse blocking state.

Figure 2-7 Electric field profile when a GTO is blocking a voltage.

A GTO can also block a reverse voltage by its junction J1 as is shown in Figure 2-7 (b). When the junction J3 is gated off, the reverse voltage blocking capability is similarly determined by the avalanche breakdown of the PNP structure under the open-base condition. A GTO with both forward and reverse blocking capability is called symmetric blocking GTO.

## 2.4    Practical GTO turn-off operation

A GTO normally requires a dv/dt snubber circuit to conduct turn-off operation. Figure 2-8 shows a practical setup in which dv/dt snubber formed by $D_S$, $R_S$ and $C_S$ is used and Figure 2-9 shows a typical GTO's turn-off characteristic  under snubbered condition.

Before t0, the GTO is ON so a current is built up in the load inductor $L_L$ and the DUT. The anode current $I_A$ is approximately equal to the cathode current $I_K$ because the gate current $I_G$ is negligible. Starting from time t0, a negative voltage $V_{OFF}$ is applied to the gate of the GTO. The gate current $I_G$ then decreases linearly at a rate determined by the applied negative turn-off gate voltage $V_{OFF}$ and the gate lead stray inductance $L_G$. At t1, the device could not maintain the latch anymore so the anode current begins to decay. The current from the load inductor will be diverted to the dv/dt snubber path. At t2, when the anode current observes its maximum di/dt, the anode voltage shows a spike due to the stray inductance $L_S$ in the dv/dt snubber path. At t3, the anode current enters its tail stage. At t4, the anode voltage reaches the DC link voltage so the freewheeling diode $D_F$ will be conducting. The energy in the stray inductance in the loop of power supply, freewheeling diode and the dv/dt snubber will be released to the snubber capacitor, causing another voltage peak. The anode voltage dip between t4 and t5 is due to the reverse recovery of the dv/dt snubber diode $D_S$. The turn-off trajectory of a GTO with a dv/dt snubber is significantly reduced as shown in Figure 1-3.
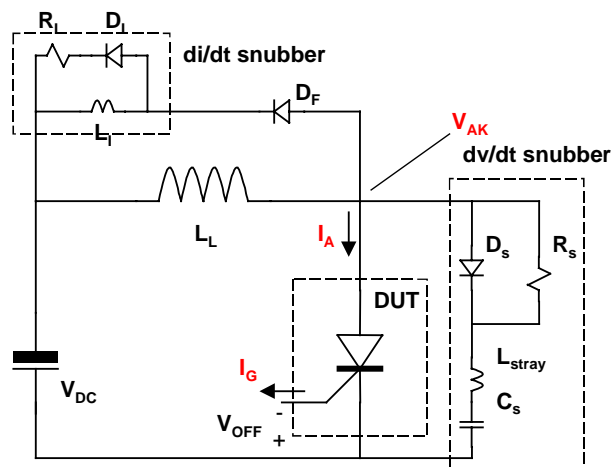


Figure 2-8 A GTO's turn-off circuit with a typical RCD dv/dt snubber.
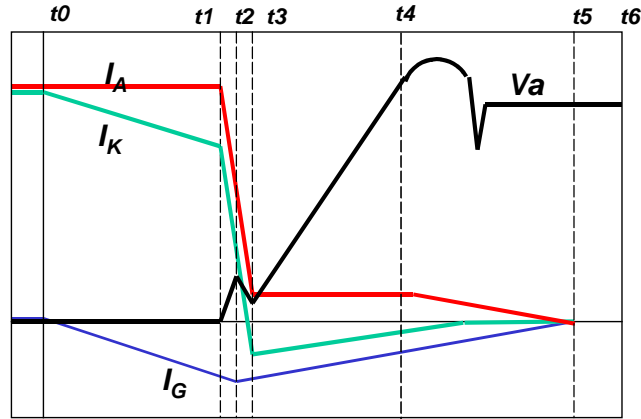
Figure 2-9 Typical GTO's turn-off characteristics under dv/dt snubber condition.

The turn-off capability of a GTO is limited by three factors: maximum cell turn-off current, dynamic avalanche and non-uniform current distribution during turn-off transient.

## 2.5    Maximum cell turn-off current limitation

Besides the turn-on current spreading problem, the large cell size of the GTO sets the maximum turn-off current for a GTO cell due to its p-base lateral resistance. Figure 2-10 shows currents in a GTO cell when it fails to turn-off. Because of the presence of the p-base lateral resistor $\mathbf{r_P}$, turn-off gate current $I_G$ produces a lateral voltage drop in the p-base. Once the anode current is high enough, the voltage drop across $r_P$ can maintain the forward bias on the part of the thyristor cell far away from the gate contact while the part close to the gate contact is reverse biased and is already turned off.  The maximum turn-off current density $J_{A,MAX}$ set by this resistive limitation can be expressed as:

$$J_{A,MAX} \le 8 \ ((V_{OFF} + 0.7) / (R_{E,P} \, W_E^2)) \qquad\qquad (2\text{-}9)$$

where $V_{OFF}$ is the turn-off voltage of the GTO's gate driver, $R_{E,P}$ is the sheet resistance of the p-base and $W_E$ is the width of the GTO cathode. This current density is basically the maximum turn-off capability of the GTO under snubberless turn-off condition, and is not normally the limitation under snubbered condition.
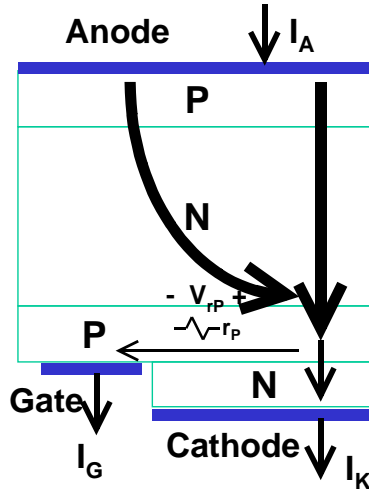
Figure 2-10 Currents in a GTO cell when it fails to turn off.

## 2.6    Dynamic avalanche

Under a high electric field, an avalanche process will happen inside the silicon. The static critical electric field is a function of doping profile. The lower the doping, the lower the critical avalanche electric field. The static avalanche voltage of a single side abrupt PN junction is determined by both the critical electric field and the depletion region width.

While the junction is conducting high current, the avalanche voltage decreases significantly due to the existence of carriers in the depletion region. This process is called dynamic avalanche [H7]. Figure 2-11 shows the cross section of a PNP transistor under both current and voltage stress. A GTO turn-off with a dv/dt snubber enters the PNP conduction mode between t2 and t3 as shown in Figure 2-8. Assuming carriers in the depletion region are moving at their saturation speed, then both the anode current density and the anode-cathode voltage can be expressed as:

$$J_A = q\, p\, v_s \qquad\qquad\qquad\qquad (2\text{-}10)$$

$$V_{AK} = E_m\, W_E/2 \qquad\qquad\qquad (2\text{-}11)$$

$$\approx (\varepsilon_s\, E_C^2) / 2\, q\, p = (\varepsilon_s\, E_C^2) / (J_A/v_s) \qquad (2\text{-}12)$$

where $p$ is hole density in the depletion region; $E_C$ is the critical electric field causing avalanche breakdown; $v_S$ is the saturation velocity of holes. In the depletion region, holes are the only carriers. In the presence of holes in the depletion region, the charge density in the depletion region is higher compared to the case without the current, so the peak electric field is also higher at the same width of the depletion region.

At the point when dynamic avalanche happens, the power density of the device, which is the product of both the current and the voltage applied on the device, can thus be expressed as:

$$J_A \, V_{AK} = \varepsilon_s \, v_s \, E_C^2 \,/\, 2 \tag{2-13}$$

which is about *200~300* kW/cm$^2$ for silicon.

The on-set of dynamic avalanche itself is not a stable condition because the generated carrier is not enough to maintain the current. However, it is not a failure condition from the device's physics point of view. The dynamic avalanche is widely regarded as the failure mechanism of the GTO because it will initiate a non-uniform current distribution among large wafer size GTOs. The current crowding or current filament formed after the on-set of dynamic avalanche is enough to destroy the device at one location in the form of a melted spot [B11].
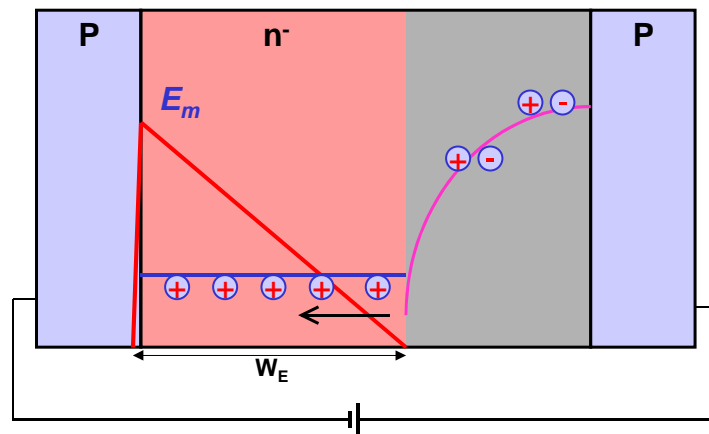


Figure 2-11 Dynamic avalanche in the blocking junction of a PNP structure.

## 2.7    Non-uniform turn-off process among GTO cells

For a high power GTO, the instant turn-off power it can withstand is far below the value set by the dynamic avalanche breakdown. So a GTO needs help from a dv/dt snubber to shape its turn-off I-V trajectory as is shown in Figure 1-3 and to lower the maximum average instant power the external circuit can apply. Non-uniform current distribution or current filament [B11] among GTO cells during the turn-off operation accounts for this limitation. The current filament can be formed at the beginning of the turn-off due to differences in storage times or caused by the on-set of the dynamic avalanche during the turn-off [B12].

The non-uniform turn-off process can be understood by considering two GTO cells in parallel as is shown in Figure 2-12. The two cells are identical except their storage time. Although only two cells are shown, GTO1 can represent a group of slower cells while GTO2 represents a group of faster cells. The turn-off process starts from t0. Since it has a shorter storage time, GTO2 turns off earlier at t1. The current originally shared by GTO2 is now transferred to GTO1. At t2, GTO1 is turned off at twice its previous current. Turn-off failure can happen if its current at t2 exceeds the maximum turn-off capability of GTO1. This can easily be the case when the number of faster cells is much larger than the number of slower cells. At t3, where both current and voltage are high, GTO1 is subject to much higher instant power stress than that of GTO2. The dynamic avalanche could happen first at GTO1 and initiate a positive feedback that will enable the re-latch of GTO1. If the number of slower cells is much smaller than that of faster cells, the current density in GTO1 can then become extremely high. The excessive energy dissipated on the stressed cells can cause permanent failure because the temperature can be very high.



(a)                                    (b)
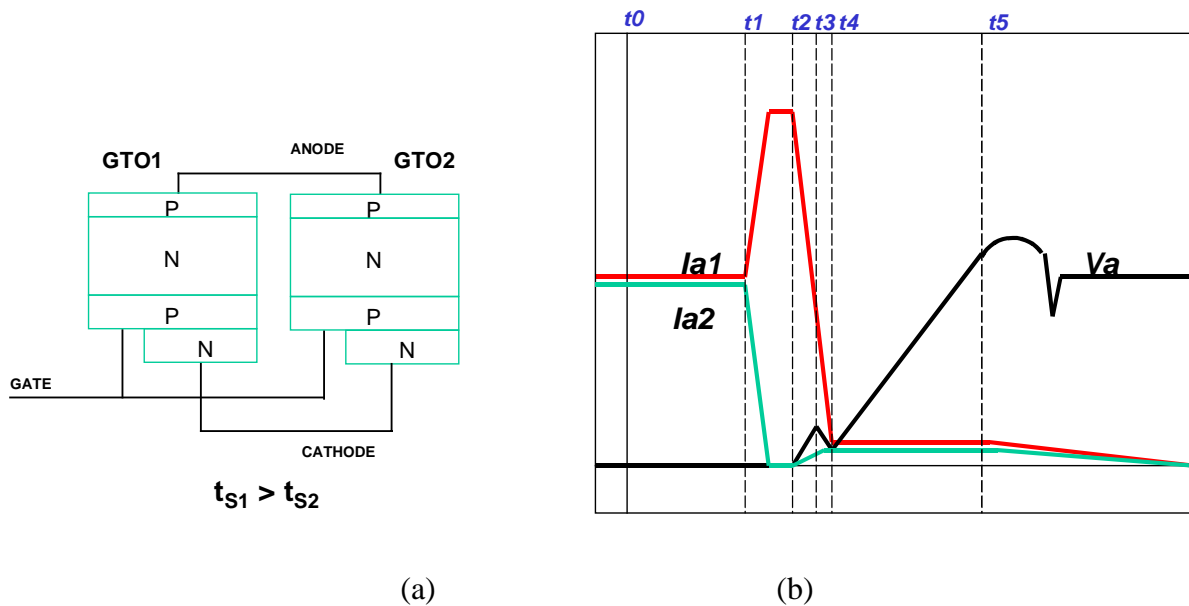
Figure 2-12 Current crowding among two GTO cells due to their storage time difference.

There is also a positive feedback mechanism that will further increase the storage time difference as is shown in Figure 2-13. At higher current density, the common-base current gains of both

transistors in GTO1 increase. Thus its turn-off gain becomes even lower according to equation (2-7), requiring more gate current for turn-off.
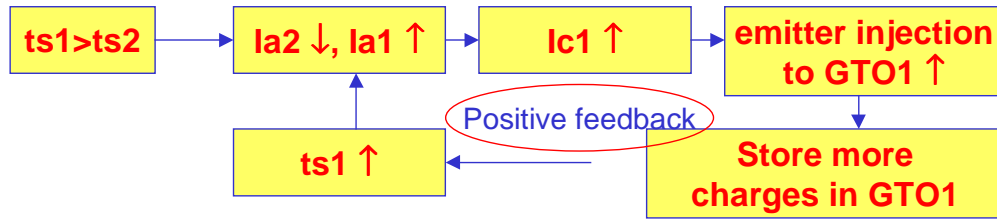


Figure 2-13 Positive feedback mechanism enhances the storage time difference and pushes the current filament into the slowest cell.
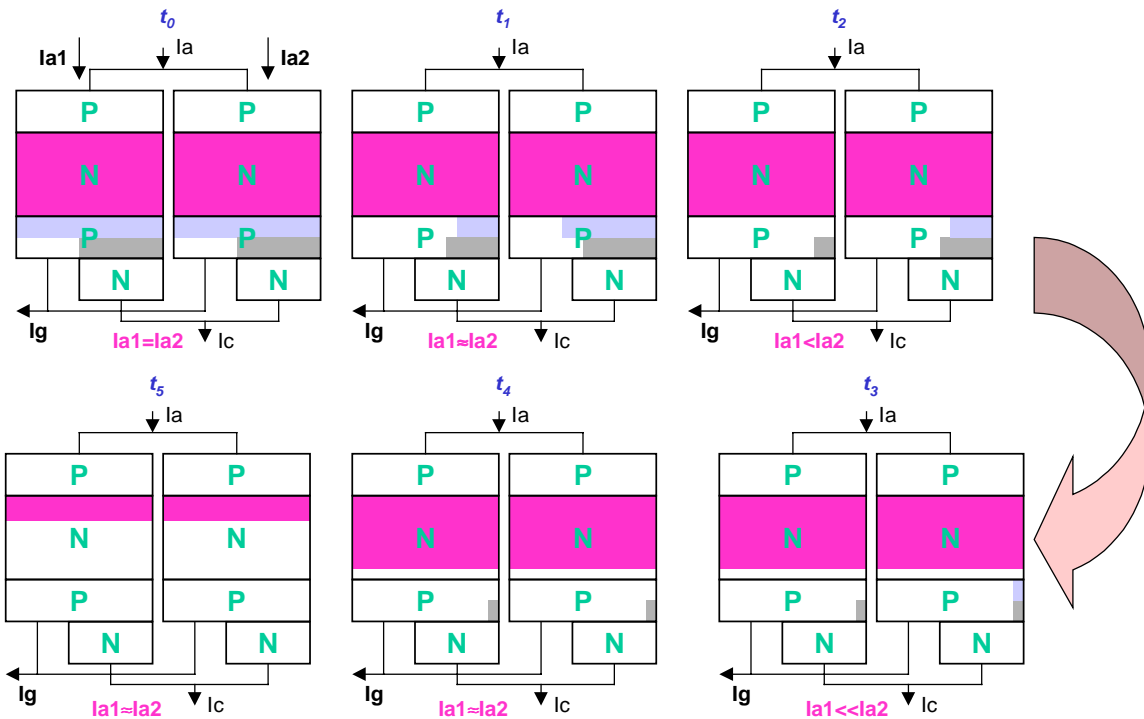


Figure 2-14 Semiconductor level analysis of the non-uniform turn-off process. The shaded region represents stored charge(plasma) in the GTO.

Figure 2-14 shows the analysis of current crowding at the semiconductor level. By t1, minority carriers in the p-base of GTO2 are drained below a critical level so its anode current begins to decay. At t2, current filament in GTO1 is formed. By t3, minority carriers in the p-base of GTO1 are also drained below its critical level so it begins to turn off. After t4, the anode voltage is

increasing and carriers in their voltage blocking region n⁻ will disappear at the same pace. If the number of faster cells is much higher than the slow cells, the latch condition in slowest cell cannot be cut off and localized current density can be thousands of times higher than the initial current density. Device failure happens when voltage increases to a certain point due to high power density stress. Combination of storage time differences and the on-set of possible localized dynamic avalanche just make the case even worse. Practical RBSOAs of high power GTOs are below the 50kW/cm$^2$ power constant line.

## 2.8    Summary of the GTO's characteristics

Advantages of the GTO include

      1     high current/voltage capability

      2     low conduction loss

      3     low cost solution

Disadvantages

      1     non-uniform turn-off---poor RBSOA

                              ---dv/dt snubber required

      2     non-uniform turn-on---di/dt snubber required

      3     current control     ---high gating power

      4     long switching time ---low speed

      5     no current limitation capability (FBSOA)

## 2.9    Unity gain turn-off operation of the GTO

### 2.9.1    Tradition GTO turn-off and RBSOA

Traditional GTOs are generally designed with a turn-off gain of three to five. This is the result of trade-offs between the GTO's performances and its gating requirement. Figure 2-15 shows the typical turn-off circuitry for a traditonal GTO. A negative turn-off voltage source $V_{OFF}$ is connected to the GTO's gate-cathode junction J3 through the turn-off control switch SW. Since both sides of the junction J3 are highly doped, its breakdown voltage $BV_{GC}$ is practically about 20 volts and can hardly be increased. The turn-off voltage $V_{OFF}$ is selected below junction J3's breakdown voltage to avoid constant breakdown of this junction when the GTO is in the off state. To turn off the GTO, switch SW is turned on so the negative turn-off voltage $V_{OFF}$ is

applied on the GTO's gate-cathode junction. The current originally flowing through the cathode will then be diverted to the gate, causing cathode current $I_K$ to decrease and the gate current to increase. Because of the existence of the GTO's gate lead stray inductance $L_G$, which is practically in the order of several hundreds of nano-Henry determined by the lead structure and length, the cathode current will decrease linearly and the gate current will increase linearly. This current commutation rate is thus given by:

$$dI_G/dt = V_{OFF} / L_G \qquad\qquad (2\text{-}14).$$

The higher the turn-off gate current slew rate, the shorter the storage time. To get the highest switching speed, the turn-off voltage is normally selected very close to $BV_{GC}$ to realize highest turn-off gate $dI_G/dt$. The typical turn-off gate $dI_G/dt$ is in the order of several tens of amperes per microsecond and the typical storage time of a high current GTO is about 20 microseconds. Figure 2-16 shows the typical current and voltage waveforms of a GTO. After the GTO is turned off, its gate current will drop back to zero slowly by breaking down the GTO's gate-cathode junction due to the energy stored in $L_G$. The energy required from the gate driver during this turn-off transition is the integration of the gate current times the turn-off voltage $V_{OFF}$. This energy is significant because the gate current lasts for a long period.
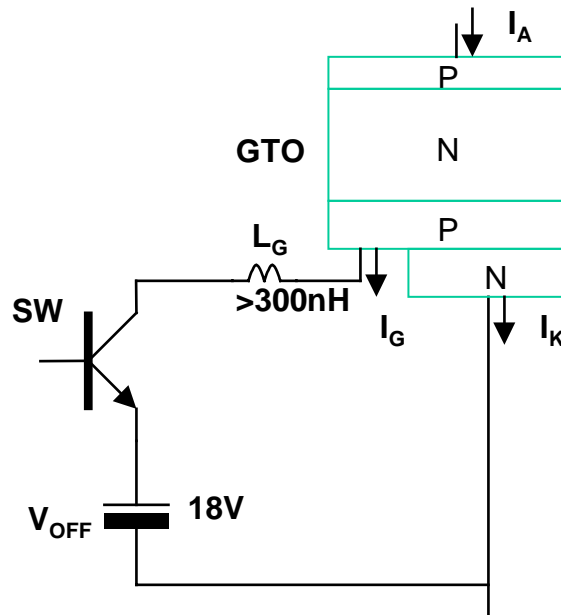


Figure 2-15 Typical turn-off circuitry for a traditional GTO.

Due to the long transient process, storage time differences among GTO cells become bigger and the non-uniform current redistribution after t1 is significant. The practical RBSOA of a GTO is normally much lower than the 200kW/cm$^2$ limit set by the dynamic avalanche because of the non-uniform current turn-off. (storage time differences and localized dynamic avalanche)

### 2.9.2    Unity Turn-off Gain and RBSOA

If the gate driver of a GTO is very fast so the gate current can increase rapidly to the anode current level and the cathode current decreases to zero before the anode current begins to decay, then the device's current and voltage waveforms are as shown in Figure 2-17. According to the definition above, the turn-off gain in this case is unity.

The internal turn-off process of the GTO changes significantly under the unity turn-off gain condition. Figure 2-18 shows minority carrier distribution during the turn-off transition. Inside the p-base, there are two functioning parts of minority carriers (electrons). The first part is the electrons related to the bias of the gate-cathode PN junction; the second part is the electrons related to the forward bias of junction J2. Before the turn-off process at point t0, minority carriers have been accumulated in the p-base and n$^-$ region. Starting from t0, the cathode current is decreasing rapidly and the gate current is increasing rapidly in the reverse direction. By t1', the cathode current comes to zero so minority carriers associated with the gate-cathode junction are removed. Zero cathode current cuts minority carrier injection from the n+ side into the p-base. From this moment, the GTO is like an open base PNP transistor instead of a PNPN latch-up structure. This difference makes the GTO more rugged during turn-off transition. Negative gate current continues the extraction of minority carriers out from the p-base until t1 when they are totally removed.
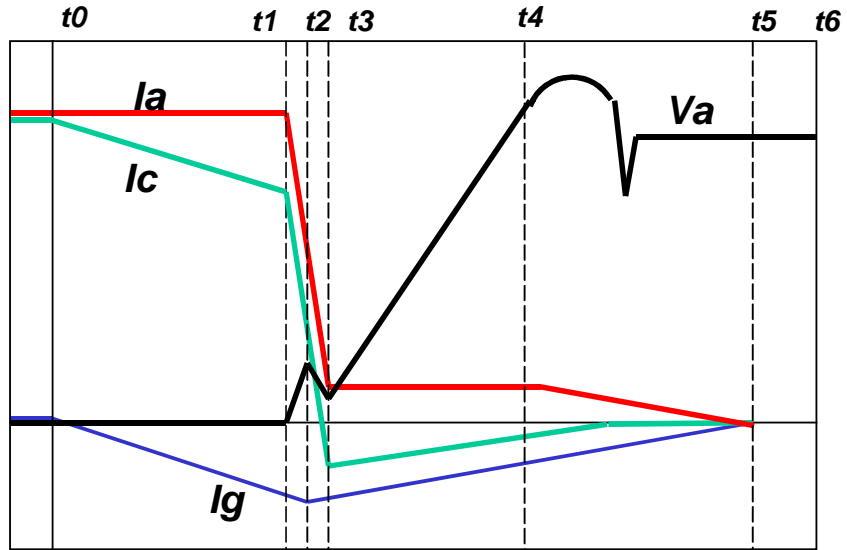
Figure 2-16 Typical turn-off characteristics of a GTO.
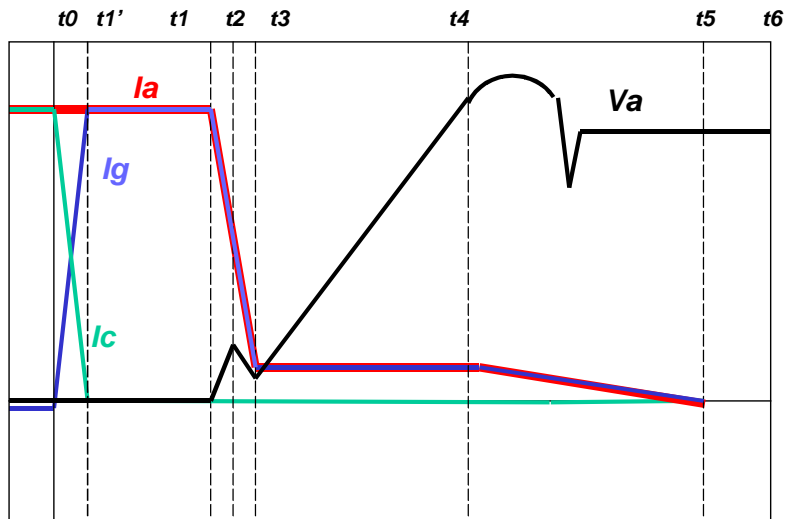
Figure 2-17 GTO turn-off waveform under unity gain.
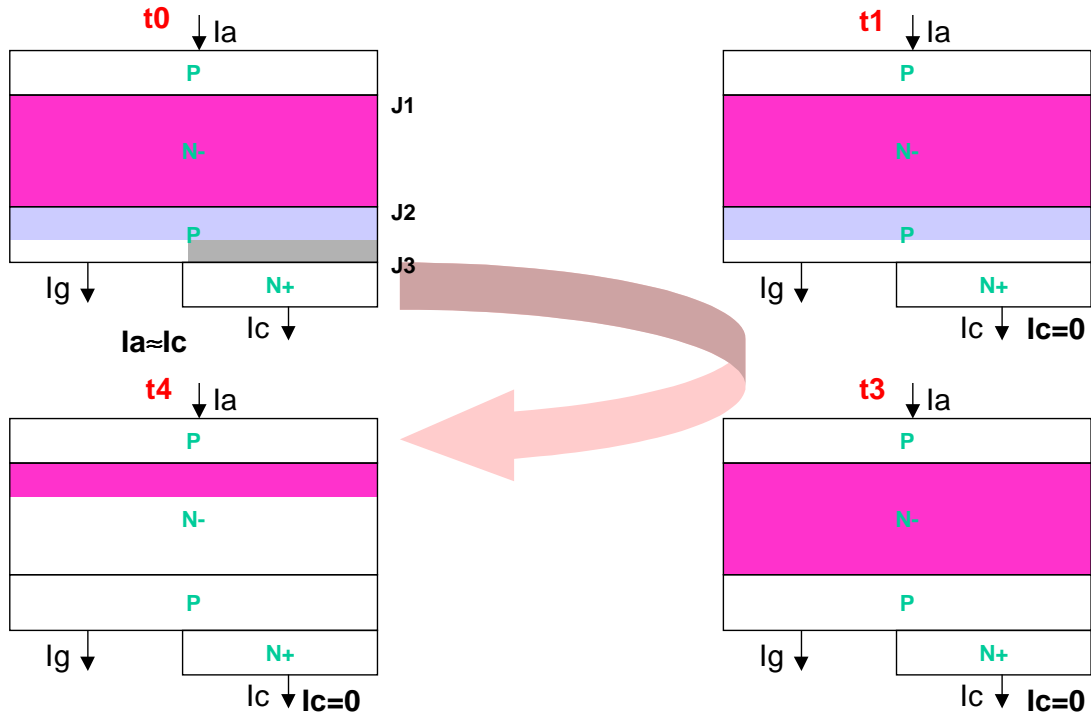
Figure 2-18 Internal process of a GTO under unity gain turn-off.

### 2.9.3    Advantages through unity gain turn-off

With unity turn-off gain, the storage time of a GTO is significantly reduced. The storage time is the time required to remove minority carriers in the p-base. In the normal GTO case, the gate current is much less than the anode current so the removal speed is slow. Furthermore, the cathode current is not cut down so minority carrier injection continues during the whole storage phase. With unity turn-off gain, the gate current is as high as the anode current, leading to a fast carrier removing speed. Also the cathode current is reduced to zero, instantly stopping the minority carrier injection into the p-base. Generally, the storage time of a GTO under unity turn-off gain is about one microsecond compared to that of about twenty microseconds in a normal GTO case with high turn-off gain.

Another important performance improvement through unity gain turn-off is in the RBSOA. As is analyzed above, the GTO current tends to crowd toward the cell with a longer storage time. This process significantly limits the average instant power a GTO can withstand so a dv/dt snubber circuitry is normally required to limit the voltage level, hence the instant power stress during turn-off transition.

GTO cells under unity gain turn-off have a tendency toward uniform current sharing. Figure 2-19 illustrates the current distribution during the turn-off transition between two GTO cells with different storage times, and Figure 2-20 shows the minority carrier distribution during the transition. Since the gate current in this case is as high as the anode current and the cathode current is zero, the absolute storage time difference is much less than that under normal GTO turn-off. At t2, GTO2 finishes its storage phase so it is turned off first and its current will be transfered to GTO1. Since the storage time difference is less, only a small portion of GTO1's current can be commutated before GTO1 turns off as well. With more anode current, the localized gate current for GTO1 is also higher, which increases the minority carrier removing speed and further shortens the storage phase of GTO1. This is therefore a negative feedback process. By t3, GTO1 is turned off, with a current higher than that of GTO2. The current difference is, however, not as significant as shown in Figure 2-12.



(a)                                               (b)
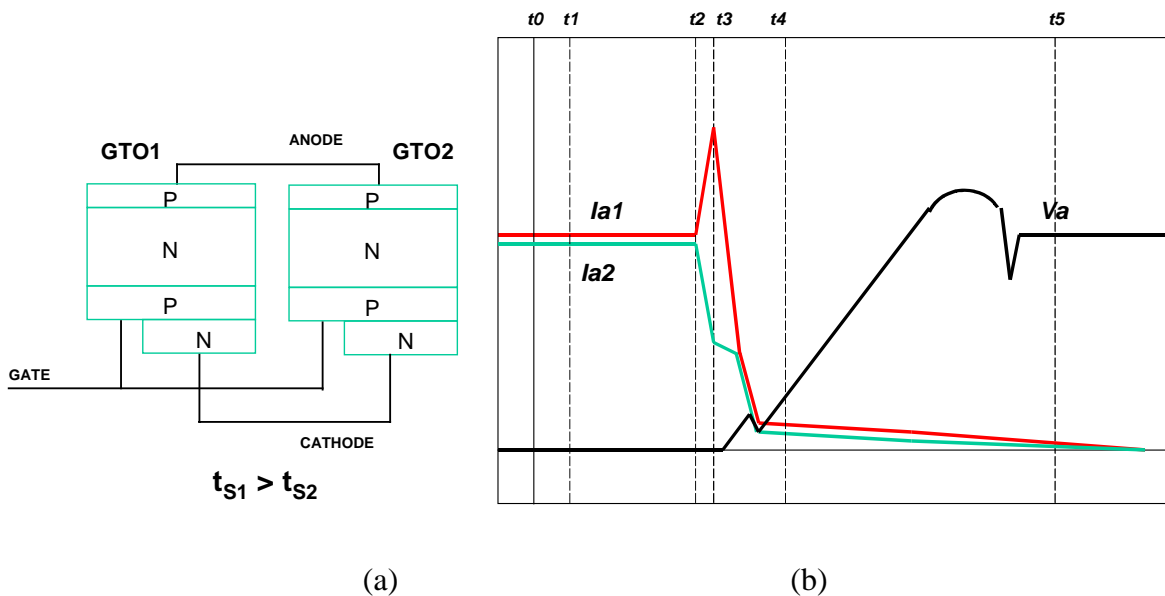
Figure 2-19 Turn-off waveforms of GTO cells under unity gain turn-off condition.

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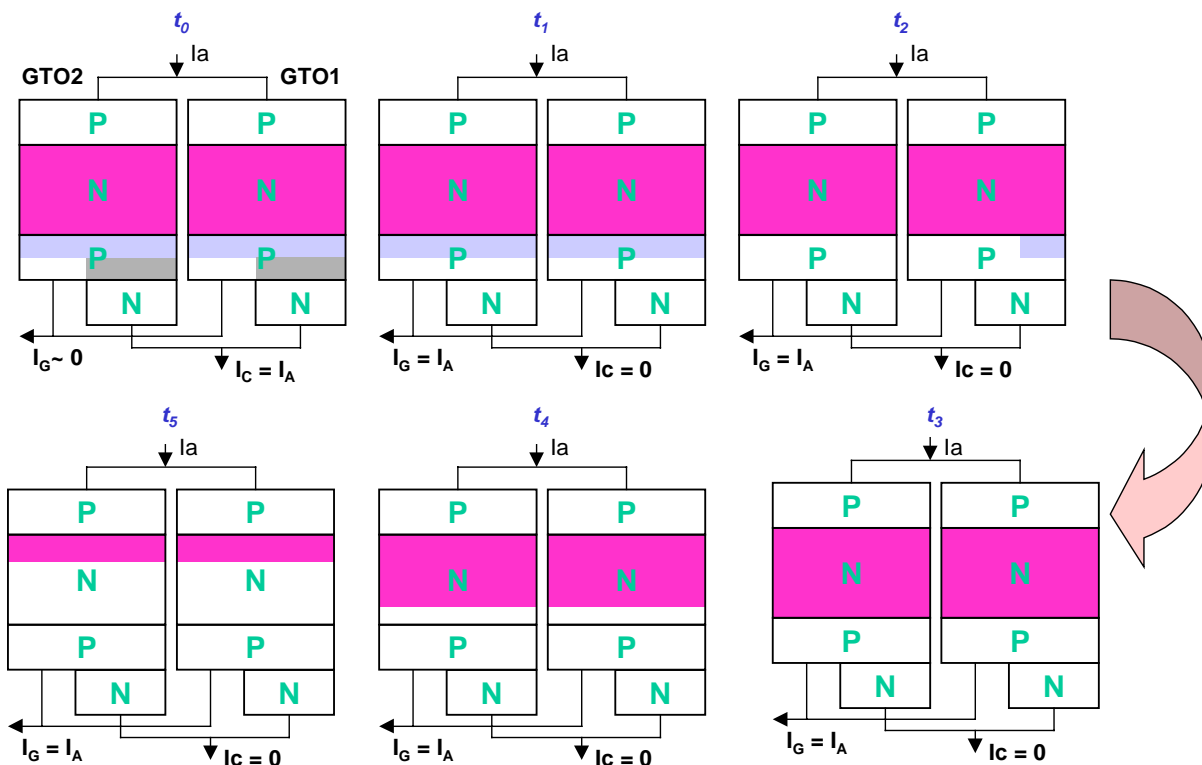
Figure 2-20 Internal process of carrier distribution during unity-gain turn-off transition for two
GTO cells with different storage time. Shaded area represents stored charges in the GTO cell.

Once minority carriers in the p-base are completely removed and the storage phase finishes, the GTO's anode current will decay and the current decay rate is determined by the minority carrier extraction process in the voltage-blocking n⁻ region as is shown in Figure 2-21. In the case where a dv/dt snubber limits the voltage rising rate, the depletion region boundary associated with J2 junction hardly moves when the current decreases. Between t2 and t3, GTO1 still has carriers in its p-base so at junction J2, electrons collected by J2 compose the major part of its anode current while the plasma profile in n⁻ region is almost unchanged. However, GTO2 has finished its storage phase and there is no more minority carrier in its p-base. The decay of its minority carrier gradient at junction J2 on its n⁻ region side forms its time dependent anode current. This current can be expressed as:

$$I_{A2} \propto d\rho_2(t)/dx \qquad\qquad (2\text{-}15)$$

where $\rho_2$ is the minority carrier profile in the n⁻ region of GTO2. After t3, when GTO1 has also finished its storage phase, the diffusion current of minority carriers at its junction J2 on its n⁻ region side also forms its anode current, which can be expressed as:

$$I_{A1} \propto d\rho_1(t) / dx \qquad\qquad\qquad (2\text{-}16)$$

where $\rho_1$ is the minority carrier profile in the n⁻ region of GTO1. At t3, diffusion currents compose both cells' anode current. Since the gradient of GTO2's minority carrier profile is already low and that of GTO2's is high, GTO2 will share more current. However, since higher current means faster carrier extraction, the gradient of GTO2's will decrease faster until their gradients or their anode currents become equal again. This means they gain current sharing again through this negative feedback mechanism.
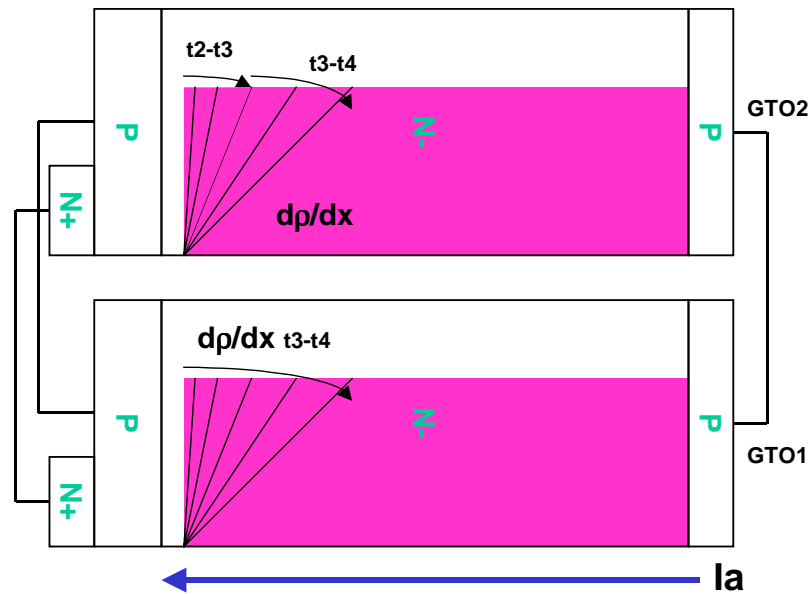


Figure 2-21 Internal process of anode current decay during turn-off transition.

In the anode voltage rising stage, both of the GTOs will have a good current sharing as well. Their current compositions are illustrated in Figure 2-23. The increase of their voltage is accompanied with the expansion of depletion region in their n⁻ region. Since the two GTO cells have the same structure, their depletion region length should be close. Their minority carrier profiles in the n⁻ region should also be close. To increase voltage on both of them, their depletion region expansion Δx is the same and the charge swept out ΔQ is the same too. This leads to the uniform current sharing for both of the cells. If one cell shares more current, it will drain more charges and expand more of its depletion area, causing voltage unbalancing between the two paralleled cells, which is impossible. This negative feedback process is depicted in Figure 2-23.
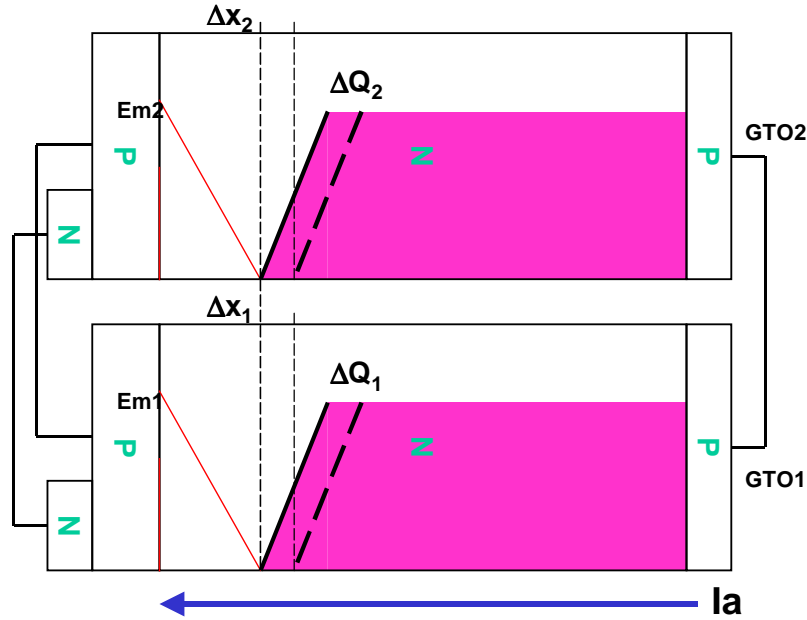
Figure 2-22 dv/dt current in the n⁻ region.

With this uniform current distribution tendency provided by the unity turn-off gain, a GTO as a whole can withstand much higher average instant power during turn-off transition. A GTO should be able to perform turn-off operation without the help of a dv/dt snubber. The snubberless RBSOA should now only be limited by the on-set of dynamic avalanche, which is about 200-$300kW/cm^2$ for silicon. It should also be pointed out again that the on-set of dynamic avalanche may not be the actual RBSOA boundary because if it does not initiate a run-away current filament, it is not a destructive one. Experimental results [H3] on IGCT turn-off, however, suggest that the dynamic avalanche is not uniform and it does lead to a device's failure. Unity gain turn-off is therefore effective in removing any current filament problem associated with storage-time differences and the dynamic avalanche soon after the current filament is formed.
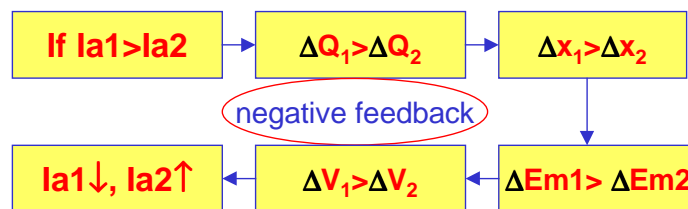


Figure 2-23 Negative feedback mechanism in the current sharing of two paralleled GTO cells during voltage increasing phase.

## 2.10  Innovative approaches to improve the performance of traditional GTO

Unity turn-off gain can significantly improve the performance of a GTO in several aspects including RBSOA and turn-off storage time. Several innovative approaches have been proposed to realize unity turn-off gain. According to their realizations, they can be classified into two different categories: hard driven type and MOS controlled type.

Hard driven type approaches use a powerful gate driver to realize unity turn-off gain. The gate driver supplies the gate current and the gating power. Falling in this category are the Resonant Gate Commutated Thyristor (RGCT) [J2]; the Diode Assisted Gate Turn-Off Thyristor (DAGTO) [J3, J4] and the Integrated Gate commutated Thyristor (IGCT) [E1].

The MOS controlled approaches use MOSFETs to help the turn-off process of the GTO. Other than the unity turn-off gain, these approaches also save control power for the turn-off process. Falling in this category are the Emitter Turn-Off (ETO) [F1] thyristor and the MOS Turn-Off (MTO) [E9] thyristor.

Figure 2-24 shows the turn-off principle of an IGCT. The major difference from that of a GTO is its reduced gate stray inductance. In the IGCT structure, the gate stray inductance is significantly reduced to allow a high enough current commutation rate to achieve unity turn-off gain. The IGCT [E1] has been developed by ABB and Mitsubishi. (IGCT is the technology initiated by ABB while it is called Gate Commutated Thyristor (GCT) by Mitsubishi)  The typical gate loop stray inductance for a four inch 4.0kA maximum turn-off current IGCT is 3nH.

Figure 2-26 shows the turn-off principle of a MTO$^{TM}$ [E9, E10]. When it is turned on, the MOS switch is acting as a short circuit to the emitter junction of the GTO. Thus the cathode current will be commutated to the MOS switch path. To assure the high current commutation rate, the voltage due to the resistance of the MOSFET and the loop stray inductance $L_G$ should be very low compared to the forward voltage drop of the emitter PN junction. The MTO is being developed by Silicon Power Corporation.
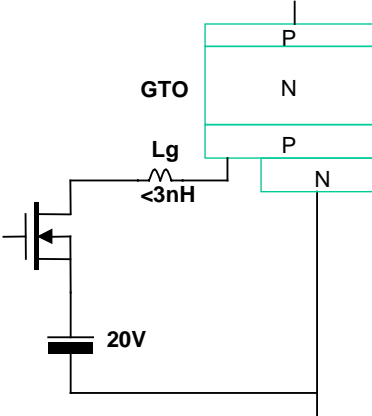
Figure 2-24 IGCT turn-off circuitry.
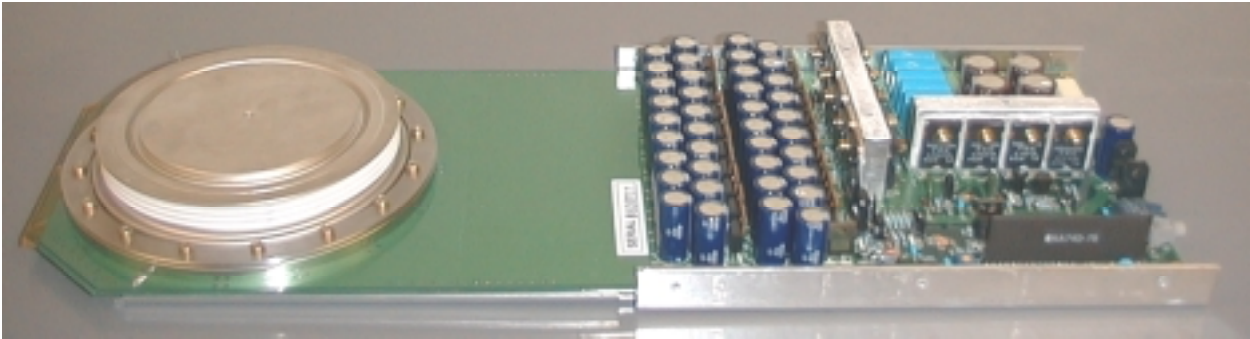


Figure 2-25 A 4.0kA/4.5kV GCT.
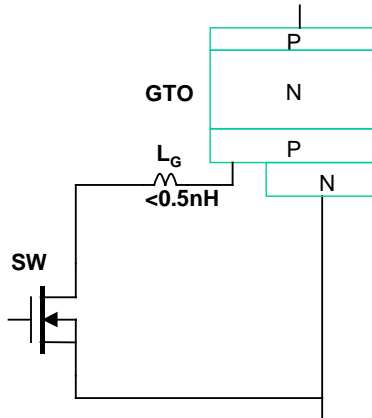


Figure 2-26 MTO turn-off circuitry.
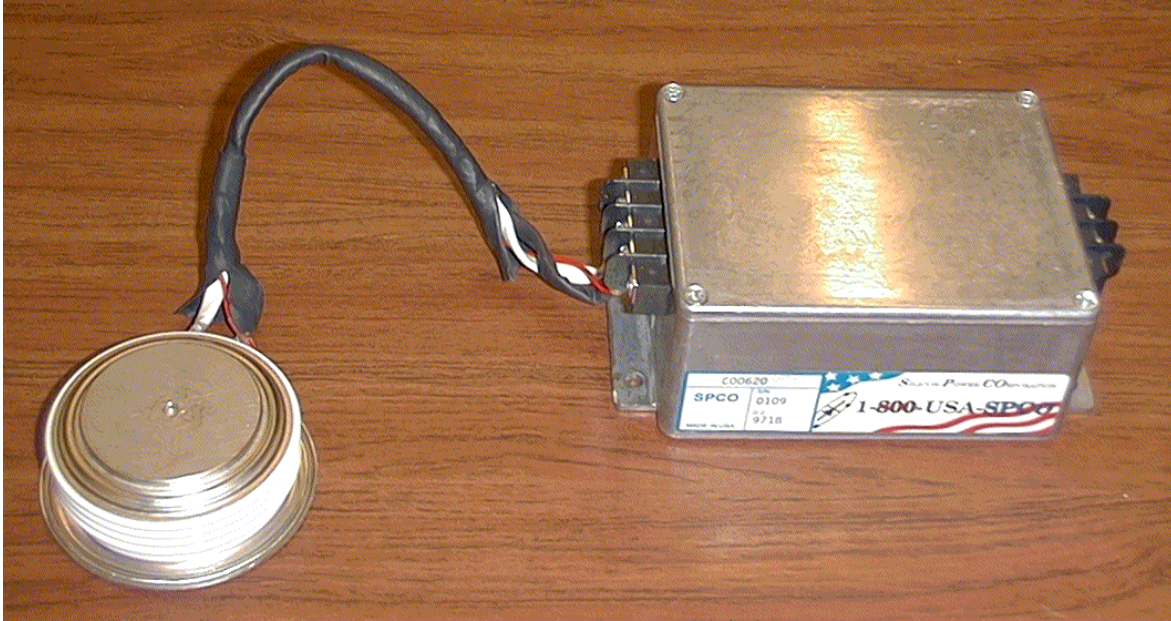
Figure 2-27 SPCO 500A/4.5kV MTO with gate driver.

The ETO is based on the GTO cascode structures [C1-13], which have been previously studied as is shown in Figure 2-28. By utilizing switches in a special connection with the GTO, the hybrid structure has advantages such as better RBSOA, fast switching speed and easy control. These studies have been focusing on the topology investigation and concept demonstration. The ETO, which has been intensively studied here, has been focusing on real scale device issues including unity gain turn-off at high currents, impact of stray parameters. The snubberless turn-off capability has also been emphasised and demonstrated.
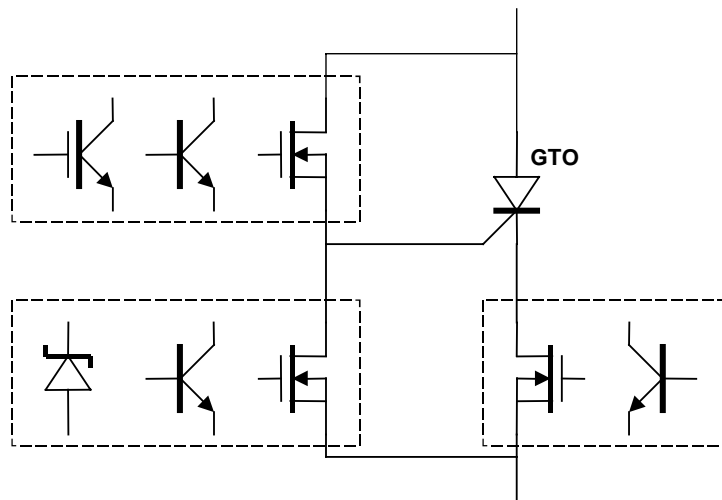


Figure 2-28 GTO cascode structure.

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A new gate driving concept, namely the Resonant Gate Commutated Thyristor (RGCT), which can achieve unity turn-off gain, is proposed, analyzed and experimentally demonstrated. The snubberless switching capability of the Diode Assisted Gate Turn-Off Thyristor (DAGTO) is fully analyzed and demonstrated.

# Chapter 3 Fundamentals of the Emitter Turn-Off Thyristor

## 3.1    Introduction

The Emitter Turn-Off (ETO) thyristor is a hybrid device based on the hybrid integration of a GTO with a series switch. Although it is similar to the cascode switches studied before, the ETO was proposed to achieve the breakthrough in GTO's turn-off performance in speed and ruggedness. Limited by the technology available at that time, the study of GTO cascode structure was mainly focusing on the demonstration of a simplified gate driving strategy. In addition, ratings of all reported cascode devices were much lower than that of the GTOs available on the market today so issues of realizing high-current switches and the effect of stray parameters are not addressed. The ETO is proposed to improve the performance of large GTO devices. This chapter will discuss the fundamentals of the high power ETO.

## 3.2    Operation principles of the ETO

Figure 3-1 shows the equivalent circuit of the ETO. An emitter switch $Q_E$ is in series with the GTO, and a gate switch $Q_G$ is connected to the GTO's gate. By turning on the emitter switch $Q_E$ and turning off the gate switch $Q_G$, a current injection into the GTO's gate (gate-1) can turn on the ETO, just like turning on a GTO. The traditional gate turn-on current is still necessary for the ETO due to the nature of the GTO. By turning off $Q_E$ and turning on $Q_G$, the GTO cathode current path is cut off and the cathode current has to commutate to the gate switch $Q_G$ via the GTO's gate, which finally turns off the GTO, hence the ETO. It is therefore obvious, by using a MOSFET as the emitter switch, that the turn-off process is a voltage-controlled one. The turn-off gate current required by the GTO is supplied by itself instead of by an external gate driver. The name "Emitter Turn-Off" emphasizes the control of the emitter junction J3, which controls the main injection of electrons. Figure 3-2 shows the turn-on and turn-off principles of the ETO.

It is very important to notice that both the emitter switch $Q_E$ and the gate switch $Q_G$ are not subjected to high voltage stress, no matter how high the voltage is on the ETO. The internal structure of the GTO's gate-cathode is a PN junction. In the ETO's off state, the high voltage is blocked by the GTO's main junction $J_2$, and the leakage current is bypassed by the gate switch

$Q_G$, which is ON. The voltage on the emitter switch $Q_E$ can be as low as the voltage on the GTO's gate, which is low because $Q_G$ is on, minus the forward voltage drop of junction J3 or as high as the voltage on the GTO's gate plus junction J3's reverse breakdown voltage $BV_{GC}$, which is about 20V. In the ETO on state, the emitter switch is ON, so the voltage on the gate switch $Q_G$ cannot exceed the voltage across the emitter switch plus the GTO's gate-cathode PN junction forward voltage drop.
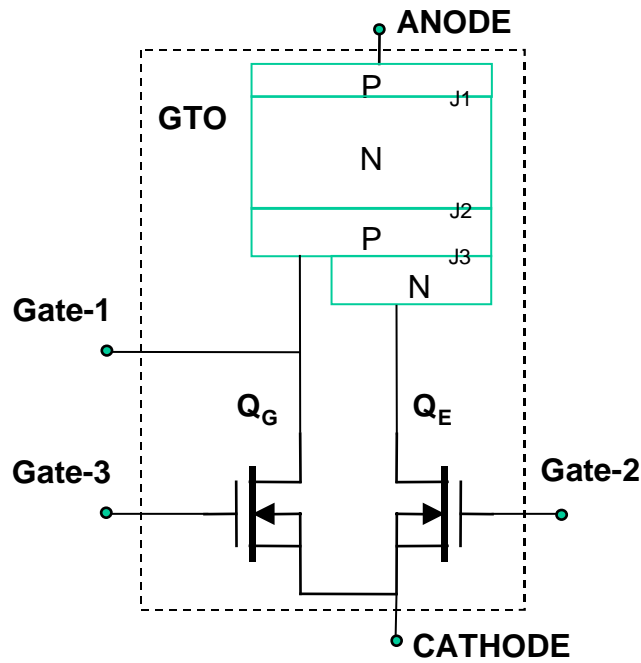
Figure 3-1 The equivalent circuit of the proposed ETO.

(a)                                    (b)
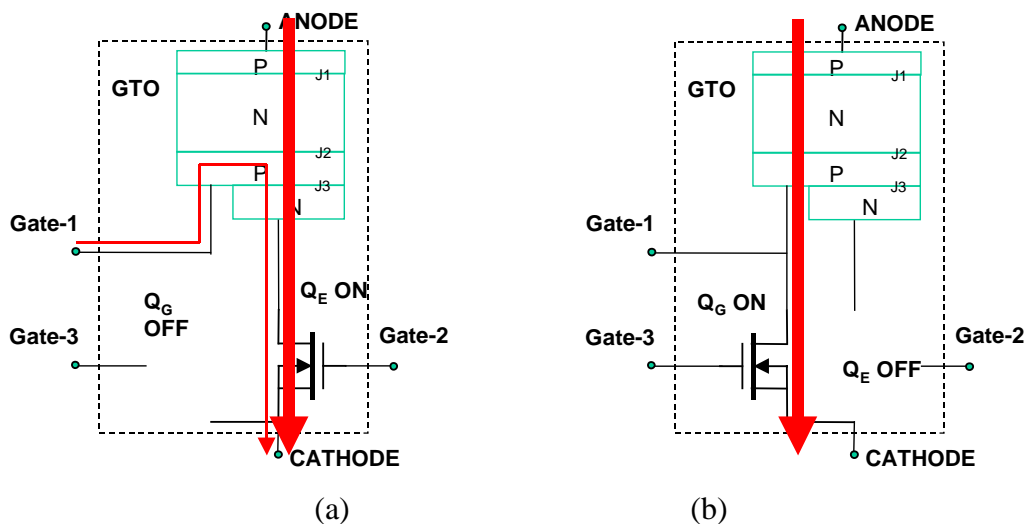
Figure 3-2 The ETO's (a) turn-on; (b) turn-off principle.

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### 3.3    Unity turn-off gain in the ETO

The turn-off gain in the ETO is theoretically unity since the emitter switch $Q_E$ is turned off, which cuts off the current path of the GTO's cathode and forces anode current flowing through its gate path during the turn-off operation of the ETO. However, due to the existence of the stray inductance $L_G$ among the loop ($Q_E$, $Q_G$ and the GTO's gate-cathode) and limited voltage capability of the emitter switch $Q_E$ thus limited voltage $V_C$ on the emitter switch, the rate of current commutation $dI_G/dt$ from the GTO's cathode to its gate is not infinite. To ensure unity turn-off gain, this current commutation rate has to be maximized. This current commutation rate can be expressed as:

$$dI_G/dt = (V_C - V_G - V_{GC}) / L_G \qquad\qquad (3\text{-}1)$$

where $V_{GC}$ is the voltage drop on the emitter junction J3. It is about one volt and does not change much with the anode current. $V_G$ is the voltage drop on the gate switch $Q_G$ when it is on and should be minimized. $L_G$ has to be minimized in the design to improve the current commutation rate. $V_C$ is the voltage on the emitter switch $Q_E$. It is built up by charging the parasitic output capacitor of $Q_E$ by the cathode current $I_K$ during turn-off transition and its maximum value is limited by the voltage rating of the emitter switch $Q_E$. A device with high voltage rating is necessary to increase the current commutation rate.

### 3.4    ETO variations

The ETO structure shown in Figure 3-1 has three control terminals. To reduce the complexity of the ETO's gate driver, the gate switch $Q_G$ can be connected in the self-driven configuration as is shown in Figure 3-3 to eliminate one control terminal. In this configuration, the gate switch becomes a two-terminal device with an I-V characteristic like a zener diode as is illustrated in Figure 3-4. The turn-on voltage of the self-driven MOEFET is its threshold voltage $V_{TH}$. When the emitter switch $Q_E$ is on, the self-driven gate switch $Q_G$ is automatically off because its turn-on voltage $V_{TH}$ is higher than the voltage at the gate of the GTO determined by the voltage across the emitter switch plus the forward voltage drop $V_{GC}$ of the GTO's gate-cathode junction. When the emitter switch $Q_E$ is off, the gate switch $Q_G$ is turned on by the current flowing through it. At high current, the voltage drop across the gate switch is the same in both cases. However, the gate-driven method exhibits significant lower voltage drop at low current levels.

Other than the saving of one gate control requirement, the ETO configuration with self-driven gate switch can improve its dv/dt capability even when its gate driver is not powered on. When the ETO is subject to a high dv/dt increase at its anode, its voltage-blocking junction J2 needs to be charged up to expand its depletion region. This will cause a dv/dt current going into its p-base. In the gate-driven configuration, the gate switch is off when its gate driver is not powered on so the dv/dt current will go through the emitter junction J3, activating the emitter injection that will probably lead to a turn-on process at some point. With the self-driven configuration, the gate switch will be turned on automatically to by-bass the dv/dt current, preventing dv/dt problem.
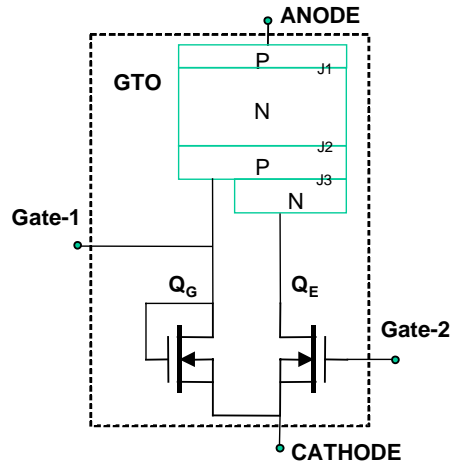
Figure 3-3 An ETO variation with a self-driven gate switch.
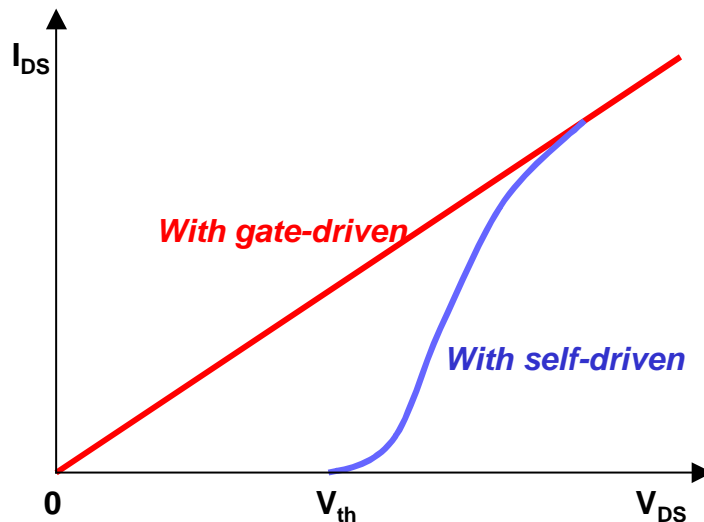
Figure 3-4 Characteristics of a MOSFET under gate-driven and self-driven.

As a compromise, another ETO variation with both self-driven and gate-driven gate switches is proposed in Figure 3-5. This configuration still has three control terminals but its dv/dt capability is improved.
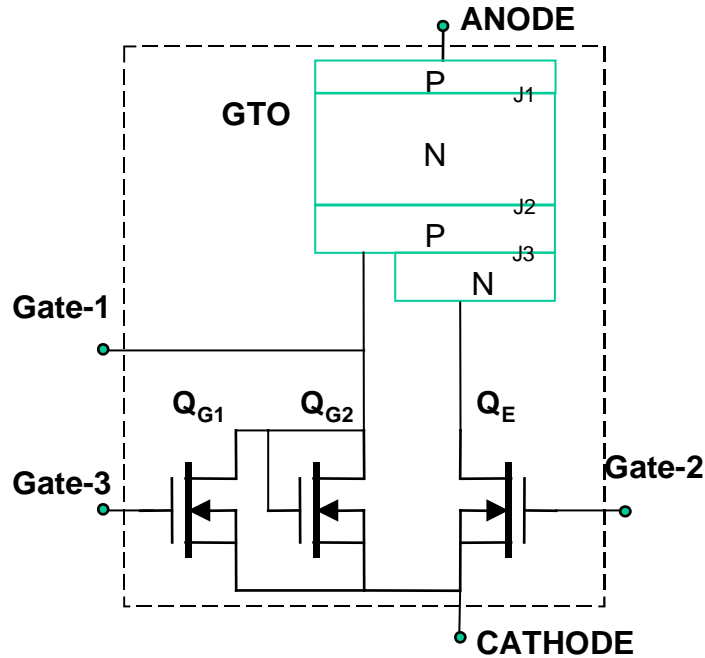


Figure 3-5 An ETO variation with both gate-driven and self-driven gate switches.

## 3.5    Numerical simulation and FBSOA

To better understand the performance and the internal process of the ETO, numerical simulations were conducted. The simulation circuit is shown in Figure 3-6. The GTO is modeled at silicon level; the gate and emitter MOSFETs are modeled as their SPICE model along with packaging parasitic inductors. The load is emulated by a current source. The GTO has a die area of about 10cm$^2$. Figure 3.4 is the simulated turn-off characteristics. The turn-off storage time is typically less than one microsecond in a unity-gain turn-off situation.
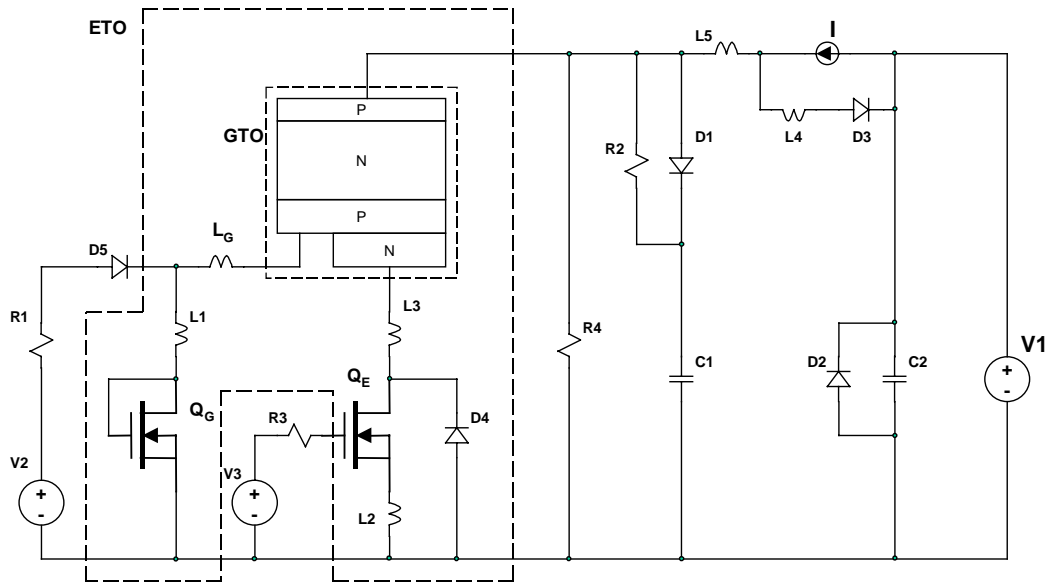
Figure 3-6 Circuit used in the mixed mode numerical analysis of the ETO.
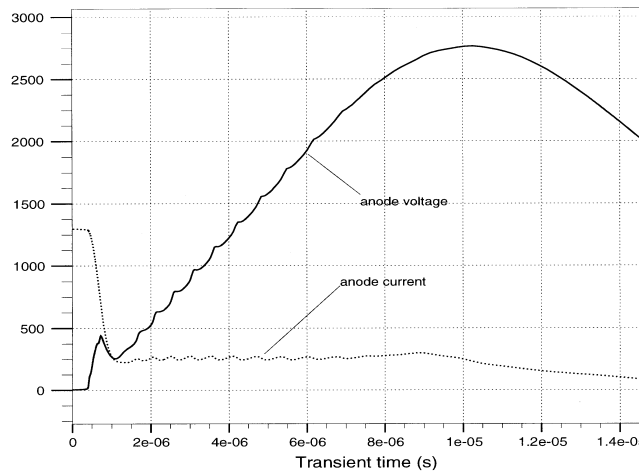


Figure 3-7 Simulated turn-off waveforms of the ETO under inductive load condition.

Besides the improvements expected in the RBSOA, speed and control, the ETO also has forward current saturation capability or FBSOA. The FBSOA results from the ballasting effect of the emitter switch $Q_E$. Assuming the ETO gate switch $Q_G$ acts like a zener diode with an equivalent turn-on voltage of $V_Z$. Under normal conduction mode, the voltage on the emitter switch $Q_E$ is always less than ($V_Z$- $V_{J1}$), where $V_{J1}$ is the forward voltage drop across the GTO emitter junction, so the gate switch $Q_G$ is off, and the ETO's forward conduction behavior is similar to

that of the GTO. However, by controlling the gate voltage, the emitter switch $Q_E$ can have a much higher voltage drop. Once this voltage is as high as ($V_Z$- $V_{J1}$), a portion of the GTO current will be diverted to the gate path. Because the current flowing out of the GTO gate has the effect of turning it off, the current conduction capability of the ETO decreases and the voltage drop across the ETO increases. This process continues until a balance is reached in which the anode current no longer increases with the increase of the ETO voltage.

Figure 3-8 illustrates the high voltage/current saturation capability of the ETO obtained by two-dimensional mixed mode device simulation. Figure 3-9 shows the current flowlines of the ETO under the high voltage current saturation condition ($V_G$=7V---voltage on the gate of the emitter switch, Vanode=2410V). It is clearly shown that part of the current flows out of the GTO's gate while another part of the current flows through the GTO's cathode. It is the current flowing out of the GTO's gate that results in the high-voltage current saturation characteristic of the ETO. Figure 3-10 shows the potential contours of the ETO in the same case. The high voltage is supported by the main blocking junction--J2, and the two transistors in the GTO are working in the linear active region instead of the saturation region.
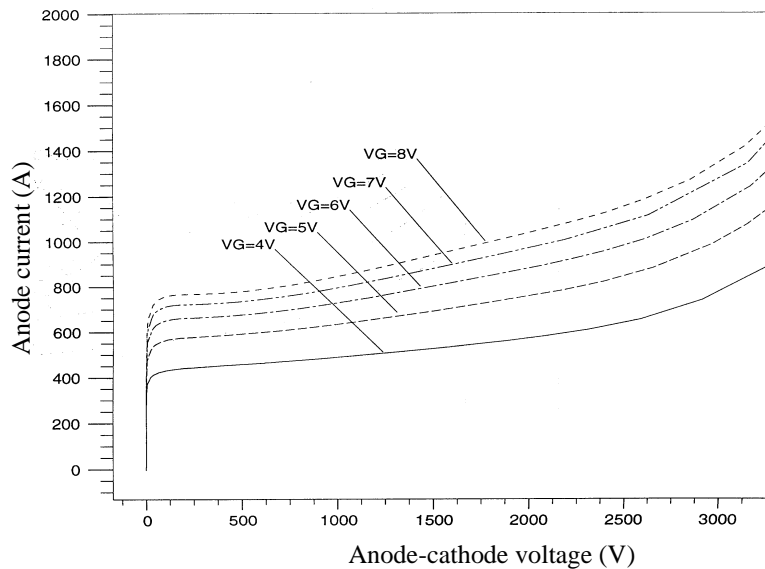


Figure 3-8 High-voltage current saturation capability of the ETO obtained by device simulation.
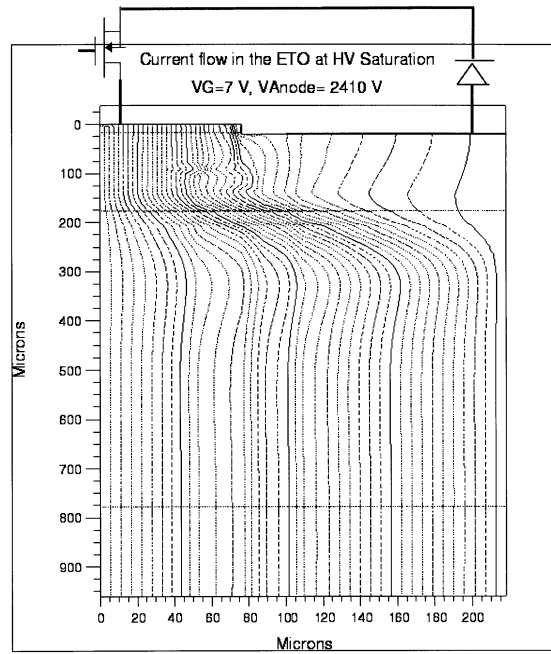
Figure 3-9 Current flowlines of the ETO under high-voltage current saturation condition. Notice the current component towards the GTO gate.
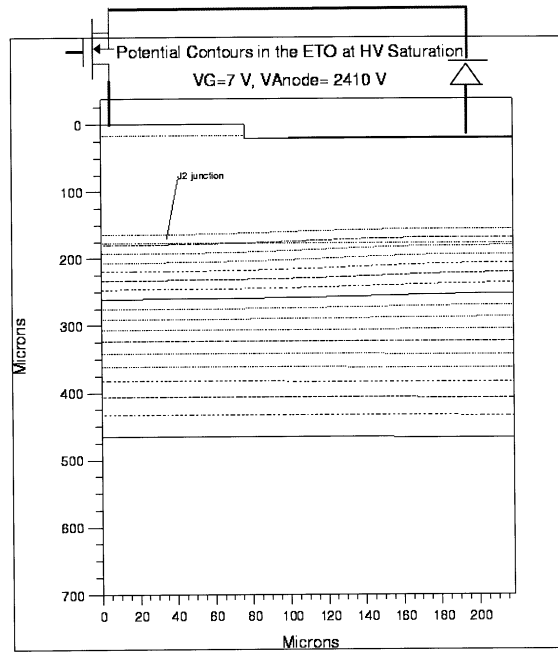


Figure 3-10 Potential contours of the ETO under high-voltage current saturation condition. High voltage is supported by the blocking junction J2.

The existence of the FBSOA in the ETO is a significant advantage over GTOs. FBSOA also exists in IGBTs and it benefits applications in two ways [D6]. First, the dynamic di/dt during the device turn-on can be controlled by the device's gate drive circuit. This will eventually eliminate the di/dt snubber in high power system. Second, devices with FBSOA have short circuit withstand capability which is very important on the reliability of the system. [H4] suggests that achieving FBSOA in large area ETO may be difficult due to non-uniform current sharing among GTO cells when they enter the current saturation region. A monolithic ETO is needed to achieve full FBSOA

## 3.6    Conclusions

It can be concluded that the ETO is a superior replacement to the tradition GTO. ETOs inherit the high current and high voltage ratings of GTOs at an expense of a slightly higher forward voltage drop due to the series emitter switch $Q_E$. With unity-gain turn-off, the ETO has significantly improved dynamic performance in terms of its turn-off speed and RBSOA. Due to the nature of MOSFET controlled turn-off process, its turn-off has been changed from current control to voltage control, which significantly reduce the control power requirement. The cost of the ETO is also low with the hybrid approach.

# Chapter 4 Experimental Demonstration of the ETO

## 4.1    Introduction

High power prototype ETOs have been experimentally developed and fully characterized by the author. This chapter presents the design considerations, improved switching performances, unity turn-off gain verification and over-current protection features of the ETO.

## 4.2    The prototype ETOs

Based on the operation principles and device simulation results, prototype ETOs, ranging from 1.0 kA to 4.0 kA, 4.0 kV to 6.0 kV, have been developed using commercial GTOs. Figure 4-1 shows the photograph of the developed ETO family along with their gate drivers. The model name of the ETO reflects the rating of the GTO used. The first two digits stand for the GTO's maximum turn-off current rating and the last two digits stand for the voltage rating. For example, ETO1045S means the GTO used for the ETO has a 1.0 kA turn-off current and a 4.5 kV voltage blocking capability. S stands for anode-shorted GTOs. The gate driver is much smaller compared to conventional GTO drivers due to the elimination of turn-off power requirement.

## 4.3    Design considerations

Several practical issues have to be addressed in the development of these prototype ETOs. First, it is difficult to realize an ideal emitter switch $Q_E$ and gate switch $Q_G$, as both of them are supposed to conduct the full anode current. Second, the stray inductance in the emitter-gate current commutating loop in practice determines whether the unity turn-off gain can be reached. That is to say, the stray inductance has to be reduced as much as possible. Many efforts have been made to optimize the design of the ETO with respect to the mechanical layout, electrical connection, thermal consideration, and current sharing.

# 1kA/4kV ETO1045S
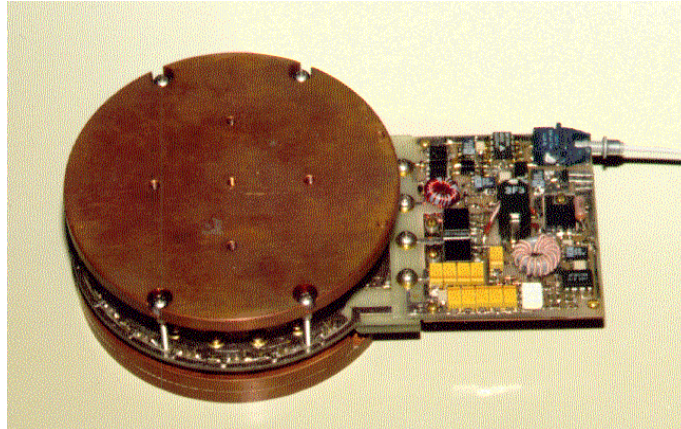
# 2kA/4.5kV ETO2045S
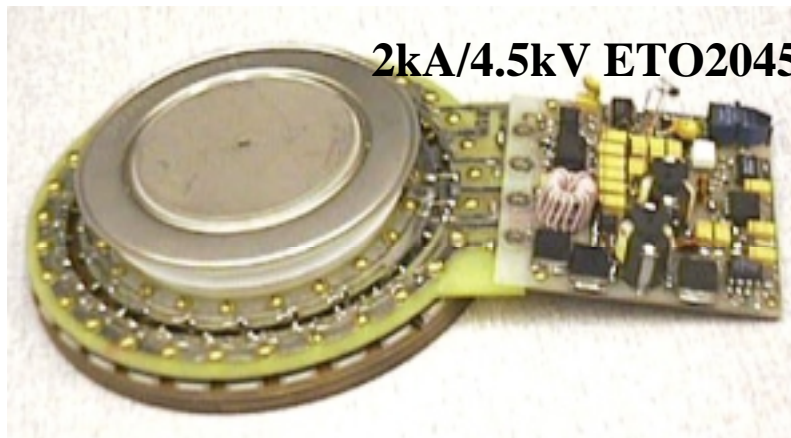
# 4kA/6kV ETO4060
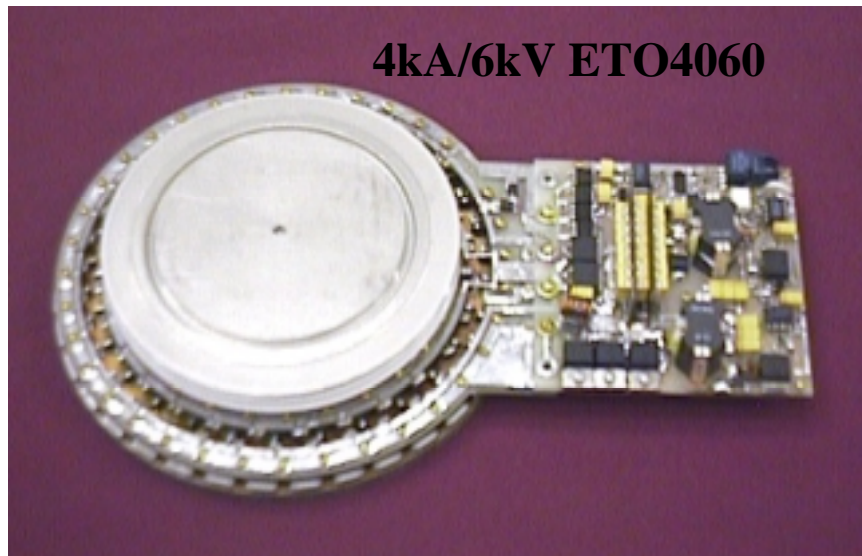
Figure 4-1 ETO family and their gate driver.

The emitter switch $Q_E$ is realized by paralleling a number of high current low voltage n-channel power MOSFETs; the gate switch $Q_G$ is realized in the same way, by paralleling several MOSFETs. There are two ways to control the gate switch $Q_G$. One is to control it through a gate driver. This method provides the lowest gate impedance current path when $Q_G$ is on. The other way is to drive the gate switch by itself. By shorting its gate with the drain, the MOSFET acts as a two-terminal zener diode. The switch is off when the voltage on it is lower than the threshold voltage of the MOSFET, and is on when the voltage is higher. With the latter configuration, the ETO can withstand high dv/dt even when its gate driver is not powered on because the gate switch $Q_G$ is turned on automatically to bypass dv/dt displace current. The positive temperature co-efficiency of the majority carrier power MOSFET also ensures uniform current sharing among MOSFETs used for $Q_E$. The use of ultra-low channel resistance power MOSFETs minimizes the added forward voltage drop to the ETO.

From the principle of the ETO, several criteria are devised for the ETO design:

a) MOSFETs are used to for the gate-switch $Q_G$ and the emitter-switch $Q_E$. Since power GTOs have very high current capability and no other single device has such a high current capability, device parallel connection is inevitable for both $Q_E$ and $Q_G$. MOSFETs are majority carrier devices with a resistive forward I-V characteristic and positive temperature co-efficiency, they are suitable for parallel connection. They also have excellent avalanche breakdown capability and its breakdown voltage has also positive temperature co-efficiency, both ensure parallel connection. Modern power MOSFETs have been optimized for low voltage / high current applications, which is what an ETO requires.

b) The voltage drop on the MOSFET in series with the GTO should be small compared to the voltage drop on the GTO. In practice, this extra voltage drop should be less than 0.5 volts at room temperature and at the rated maximum turn-off current. N channel power MOSFETs are used to construct both $Q_E$ and $Q_G$ because they have much lower channel resistance than p-channel MOSFETs at the same voltage rating level.

c) The gate MOSFET is required to sink a gate current pulse as high as the main ETO current for a very short time. In the design, the number of the gate MOSFETs is minimized by using MOSFET's repetitive surge current rating.

d) In the ETO turn-off process, the current in the emitter-switch path will be transferred to the gate path in a short time. To assure this process happens as fast as possible, the stray inductance in the gate-emitter loop should be minimized. This is very crucial to the ETO's operation.

e) Some mechanical contacts in the ETO are used for current conduction. These contacts should be designed so that the contact resistance can be neglected compared with the MOSFET resistance.

The design of a 4.0 kA ETO is briefly discussed below to show the post structure ETO---a novel package technique that integrates commercial packaged MOSFETs and GTOs.

Figure 4-2 shows the cross section of the post structure. There are two copper layers below the GTO with a thin insulation layer in between. The top copper layer is in direct contact with the GTO's cathode. The emitter MOSFETs are placed on this copper and the sources of these MOSFETs are connected to the bottom copper layer through the interconnection posts. The gate MOSFETs are placed on a separate copper layer at the same level. The source of the gate MOSFETs is again connected to the bottom copper layer through the interconnection posts.

Figure 4-3 shows the topview of the 4.0kA ETO design. The gate MOSFETs occupy a small section of the ring structure. The MOSFETs are arranged in a ring structure around the GTO to minimize the stray inductance.
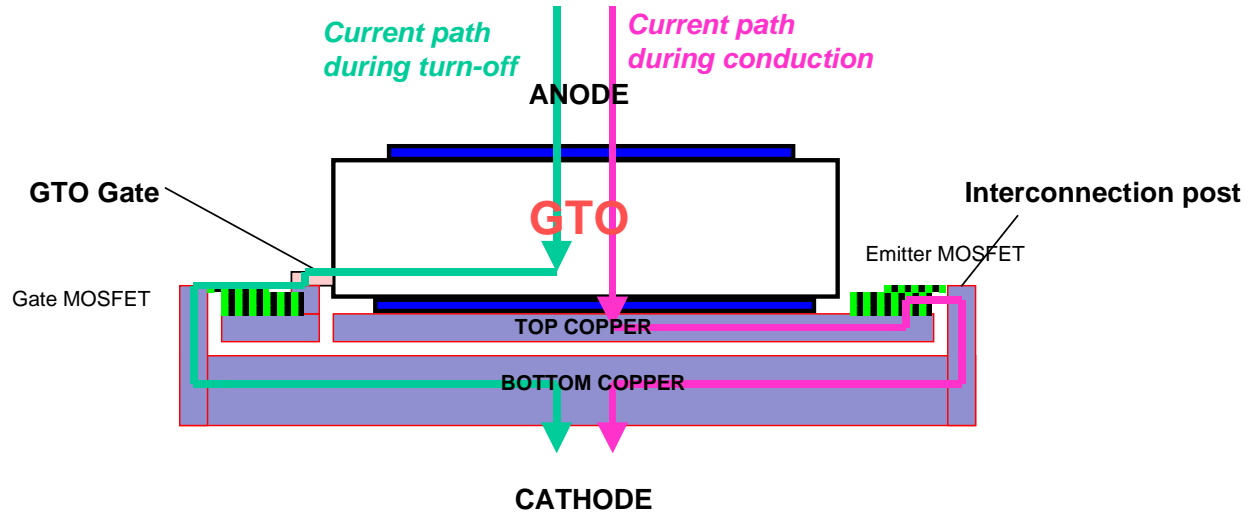
Figure 4-2 Current flow direction in the new poster structure. The current loop in the N-MOS path is reduced The current loop in the gate loop is also reduced
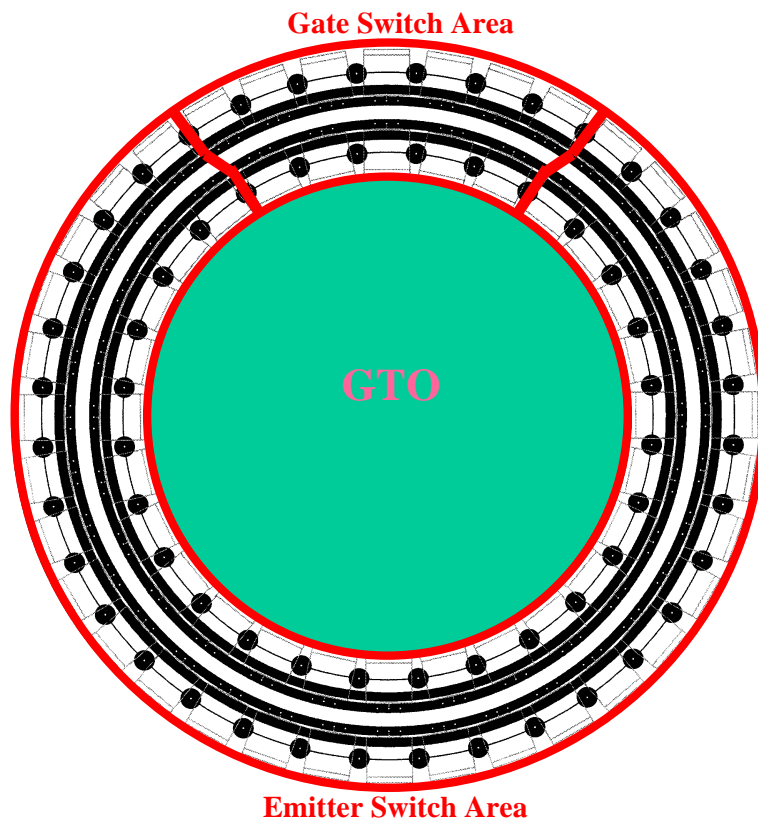


Figure 4-3 Top view of a 4.0kA ETO. The center area is for a 4-inch GTO.

## 4.4    Demonstration of faster switching speed and improved turn-off capability

Experimental results obtained from the developed ETO prototypes confirm the predicted high switching speed and short storage time. Figure 4-4 shows a typical ETO turn-off characteristic obtained on a high-power pulse tester developed by the author. Table 4-1 summarizes the measured results of several 53mm ETOs and corresponding GTOs. Table 4-2 summaries the turn-off parameters of the three different rating of ETOs. Compared with the GTO, the storage times of the ETO are dramatically reduced from typically 14µsec [L1] to 1.5µsec. On the other hand, the current tail value, which is about 10% of the anode current for the GTO, is now two times as high for the ETO1045S. This is because the significantly reduced storage phase leaves no time for the plasma profile in the n⁻ region to decrease. The overall turn-off loss of the ETO, as shown in Table 1, is about the same as that of the GTO under the same dv/dt snubber condition, while the turn-on loss is significantly reduced due to the enhanced turn-on gate current injection. Figure 4-5 shows the ETO turn-off energy for ETO1045S at 125C at different anode currents. The turn-off energy increases linearly as the anode current increases. The snubberless turn-off energy is only slightly higher than that with a dv/dt snubber. This is another indication of the high-speed capability of the ETO. The snubberless turn-off capability of the ETO will be discussed in detail in Chapter 5.

Table 4-1 53mm GTO and ETO test result comparison.

|      | $t_f$ | $t_{gq}$ | $E_{off}$ | $I_{tail}$ | $t_d$ | $t_{gt}$ | $E_{on}$ |
|------|-------|----------|-----------|------------|-------|----------|----------|
| **GTO1** | **1.2** | **14** | **1.93** | **116** | **1.1** | **3.5** | **0.416** |
| **ETO1** | **1.0** | **2.3** | **2.1** | **200** | **0.5** | **2.5** | **0.31** |
| **GTO2** | **1.3** | **14** | **1.93** | **121** | **1.0** | **3.3** | **0.366** |
| **ETO2** | **0.9** | **2.3** | **1.9** | **250** | **0.5** | **1.8** | **0.27** |
| **GTO3** | **1.2** | **14** | **1.73** | **111** | **1.0** | **3.2** | **0.349** |
| **ETO3** | **0.9** | **2.2** | **2.0** | **250** | **0.5** | **1.6** | **0.26** |
| **GTO4** | **1.4** | **13** | **1.69** | **103** | **1.1** | **3.4** | **0.370** |
| **ETO4** | **0.7** | **2.1** | **0.95** | **200** | **0.4** | **1.6** | **0.22** |
| **GTO5** | **1.1** | **13** | **1.69** | **100** | **1.1** | **3.6** | **0.397** |
| **ETO5** | **0.9** | **2.1** | **1.6** | **200** | **0.5** | **1.7** | **0.25** |
| **GTO6** | **0.7** | **12** | **1.49** | **147** | **1.1** | **3.6** | **0.425** |
| **ETO6** | **0.8** | **2.0** | **1.0** | **200** | **0.4** | **1.7** | **0.32** |

(Anode current 1.0kA, DC link voltage ~1.8kV, 2μF dv/dt snubber, 120A/μsec di/dt snubber,

125C)

| | | | |
|---|---|---|---|
| tf: | current fall time during turn-off; | tgq: | turn-off time; |
| Eoff: | turn-off energy; | tail: | maximum tail current; |
| td: | turn-on delay time; | tgt: | turn-on time; |
| Eon: | turn-on energy. | | |
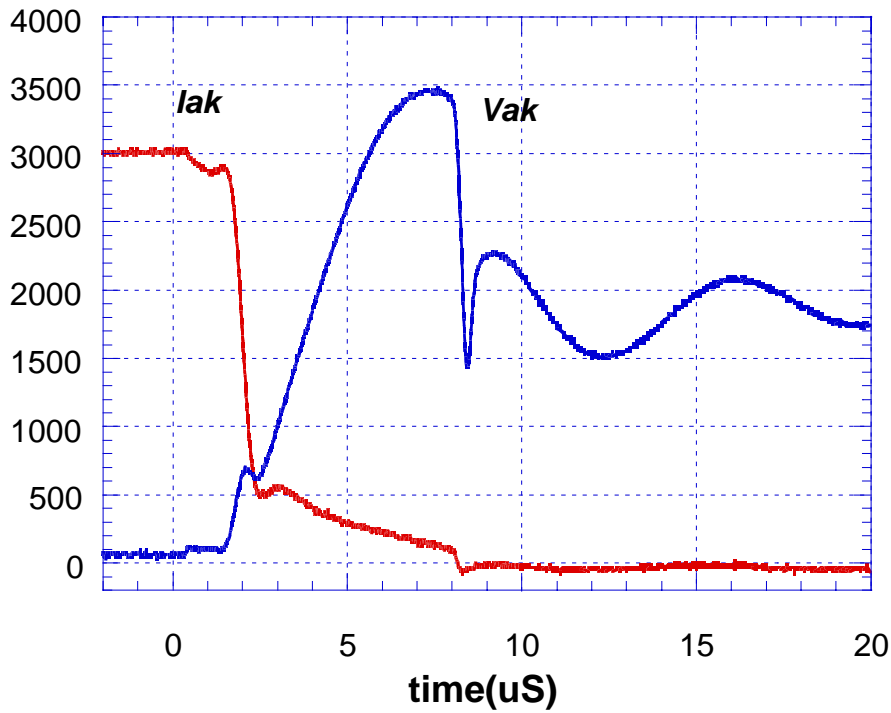
Figure 4-4 ETO4060 turn-off characteristic with a 3μF dv/dt snubber at 25C.

Table 4-2 Summary of typically ETO turn-off parameters.

|  | ETO1045S | ETO2045S | ETO4060 |
|---|---|---|---|
| Voltage rating | 4500V | 4500V | 6000V |
| Current rating | 1000A | 2000A | 4000A |
| Turn-off storage time | 1.5usec | 1.5usec | 1.8usec |
| Turn-off fall time | 0.5usec | 0.5usec | 0.7usec |
| Current tail time | ~10usec | ~10usec | ~10usec |
| Test condition | 1200A turn-off current 3500V peak turn-off voltage 3u dv/dt snubber | 2500A turn-off current 3500V peak turn-off voltage 3u dv/dt snubber | 3700A turn-off current 5000V peak turn-off voltage 3u dv/dt snubber |

* The current rating used here is the maximum turn-off current of the GTO from which the ETO

is made of.
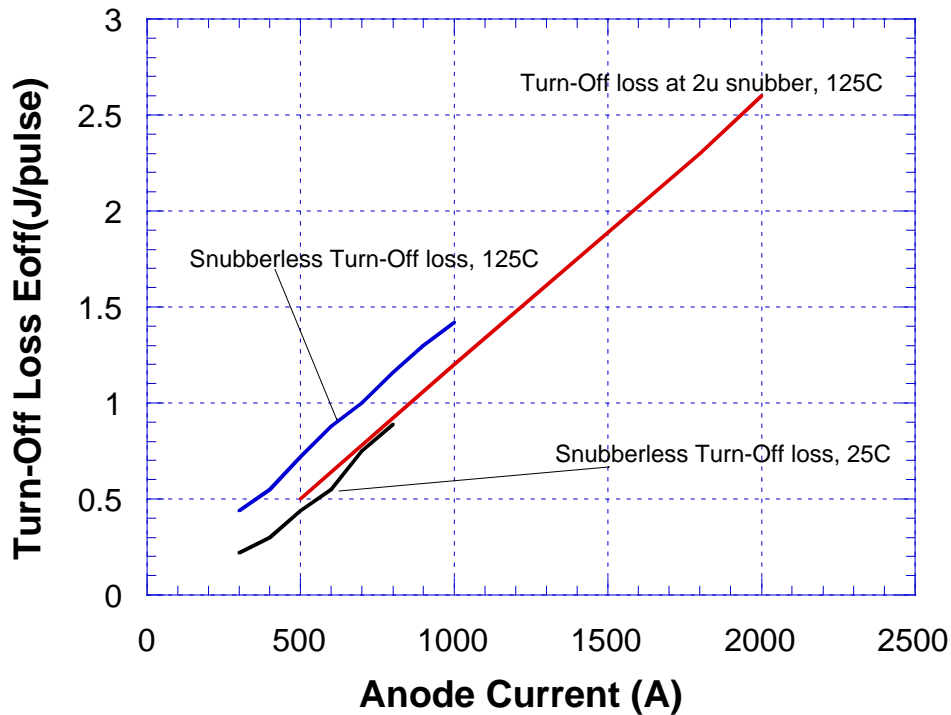
Figure 4-5 ETO1045S typical turn-off energy at 1800V DC link voltage.

The turn-on transient is accelerated significantly in the ETO and the turn-on switching loss is reduced as compared to the GTO, as shown in Table 4-1. These are due to the high turn-on current injection [E2] from the gate driver with a reduced injection loop stray inductance. In the case without dv/dt snubber, there is also no discharge current from the snubber capacitor during turn-on; thus the turn-on energy is further reduced. At 2.5 kV DC link voltage and 0.8 kA current, the turn-on loss is less than 0.15J per pulse.

From Table 4-1, the turn-off time $t_{gq}$, defined as the storage time plus the fall time, for different GTOs varies from 12 to 14μsec; while for different ETOs, it varies from 2.3 to 2.0μsec. The absolute difference among device's storage time is therefore reduced significantly. The ETO can therefore be considered to have a much more uniform turn-off transient, hence parallel and series connecting  ETOs becomes relatively easy. The operation of ETO under parallel and series connection will be discussed in Chapter 6. Figure 4-6 shows the relationship between the storage

time, the turn-off time as a function of the turn-off current for the ETO2045S. The storage time does not show significant increase when the anode current increases.
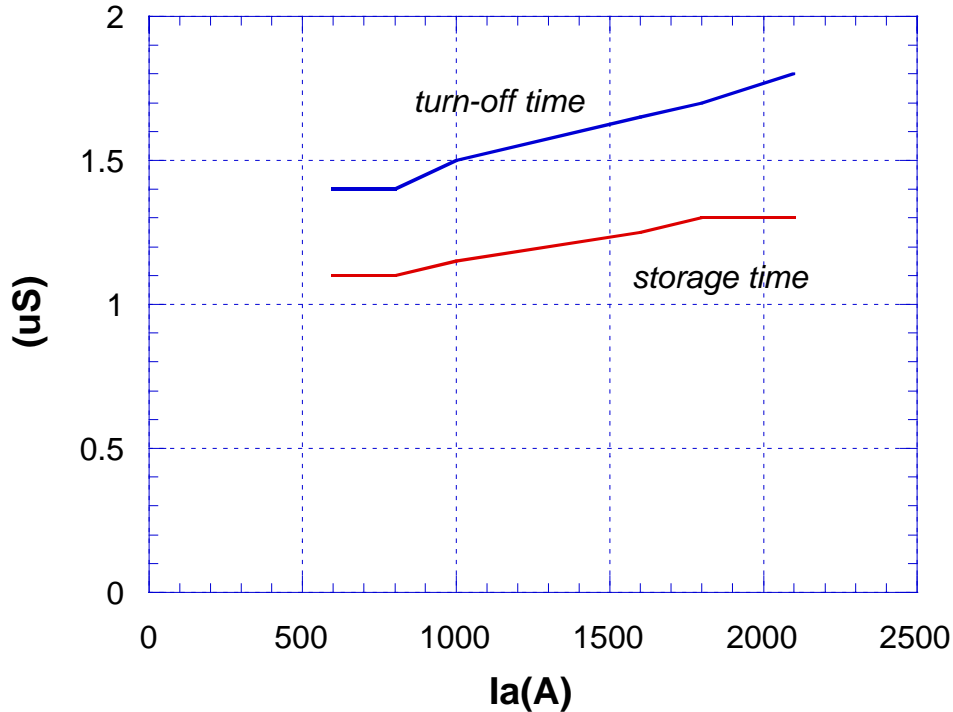


Figure 4-6 The turn-off time versus turn-off current for ETO2045S with 3μF dv/dt snubber, 25C.

As has been predicted, the gating power required for the turn-off of the ETO is only the power to control MOSFETs $Q_E$ & $Q_G$. At 1 kHz frequency, it is about 1~2Watts for the ETO1045S. The overall gating power of the ETO is therefore decreased significantly and is now mainly determined by the turn-on current injection. For the 1kA/4kV ETO1045S, the DC current injection requirement is 2A, so the total gating power required is less than 5 watts. The compact gate drivers that are shown in Figure 4-1 all have on board isolated DC-DC power supplies instead of a separate big isolated power supply box that is usually used for traditional GTOs. The control signal is provided to the gate driver through an optical fiber.

For a traditional GTO, the maximum turn-off current is generally low compared to its maximum RMS current, especially to its surge current capability. This limitation poses a heavy burden on applications to avoid a turn-off operation at higher current. With a better RBSOA, the ETO

should have a significantly higher turn-off current under the same condition. Figure 4-7 shows the ETO1045S turning off two times as much current as for the GTO under the same condition set for the GTO.
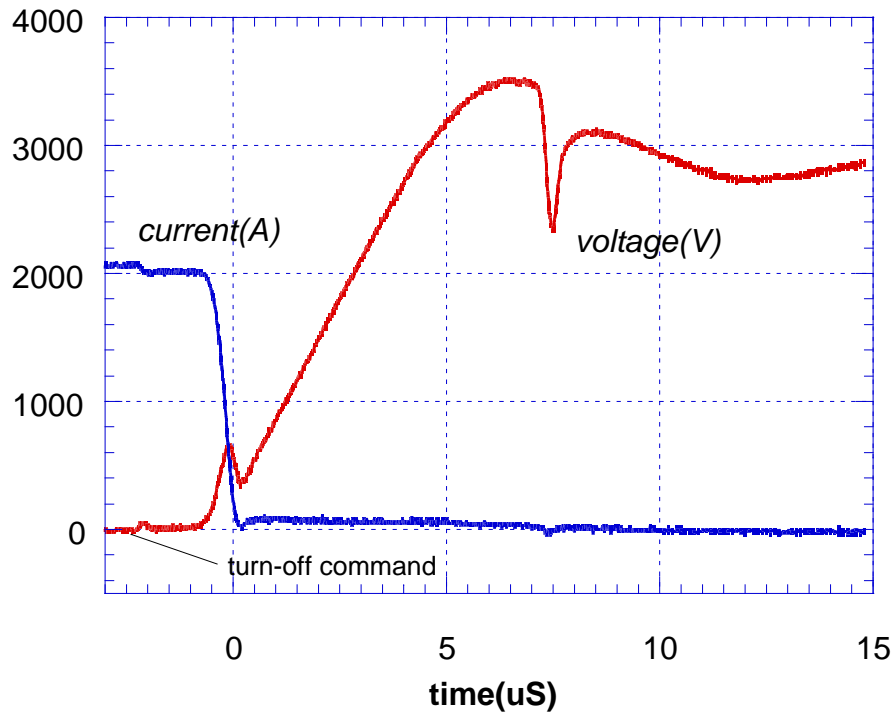


Figure 4-7 ETO1045S exhibits two times maximum turn-off current capability. 3μF dv/dt snubber, 25C.

The MOSFET has a positive temperature coefficiency on its forward voltage drop and normally the GTO has a negative temperature coefficiency. By series connecting them together, the ETO shows positive temperature coefficiency in its forward voltage drop like the MOSFET. Figure 4-8 shows the measured forward voltage drop versa temperature. For the GTO, the forward voltage temperature coefficiency turns from negative to positive at around 900A; but for the ETO, this cross over point drops down to below 500A. This feature again will enable current sharing among paralleled ETOs.
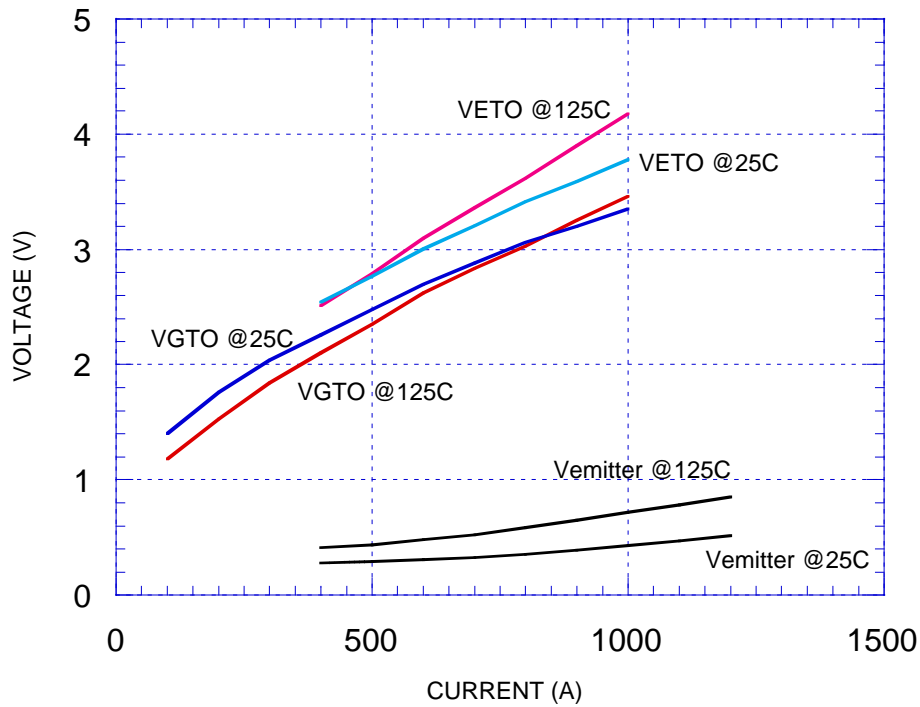
Figure 4-8 The relationship of forward voltage drop versa temperature for ETO1045S.

## 4.5    Simplified circuit model for the ETO during the turn-off transition

In actual ETO turn-off, the current commutation from the emitter to the gate is complicated because of the high di/dt involved in the process and the unavoidable stray inductance in the package. Therefore, the interaction between the emitter switch $Q_E$, gate switch $Q_G$, and any stray inductance presented in the emitter-gate loop determines the actual performance of the ETO.

To analysis the behavior of the ETO, a simplified turn-off circuit model for the GTO with unity turn-off gain is proposed and is shown in Figure 4-9. The GTO is modeled by a step current source in series with a diode. The upper PNP transistor in the GTO is modeled as a current source because, during the fast current commutation stage, the anode current $I_A$ remains almost constant and the PNP transistor still operates in the saturation region. The emitter junction of the GTO is modeled as a diode $D_{GC}$. The capacitor in parallel with the diode reflects the GTO's gate-cathode junction capacitance.

**ANODE**

**GTO**

$I_A$

**GATE**

$D_{GC}$    $C_{GC}$

**CATHODE**
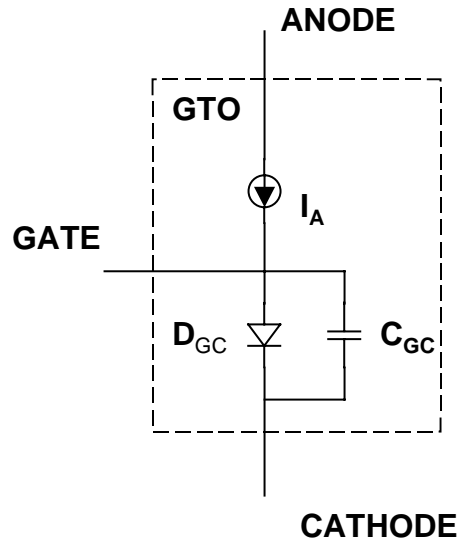
Figure 4-9  The equivalent turn-off circuit model for the GTO with unity turn-off gain.

The model can also be justified by analyzing the internal carrier distribution of the GTO right before the turn-off operation as is shown in Figure 4-10. There are two types of minorities in the p-base region. $Q_D$ represents the part associated with the emitter junction while $Q_P$ represents the part associated with the storage time of the NPN transistor. Inside the voltage-blocking region, $Q_N$ represents the part associated with the dv/dt current while $Q_T$ with current tail.

Ia

P

$Q_T$

N

$Q_N$

P

$Q_P$

$Q_D$

Ig

N

Ic
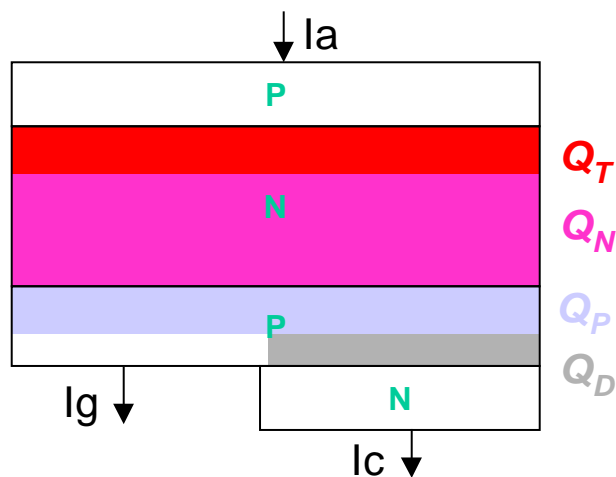
Figure 4-10 Stored charge distribution inside the GTO before turn-off.

Figure 4-11 shows the relationship between the GTO's internal charges and its external characteristics with or without a dv/dt snubber. The step current source models the sudden change of the anode current at the end of the ETO's storage phase. The storage time is different for these two cases. With the dv/dt snubber, the storage time is determined only by $Q_P$ while $Q_N$ also contributes to the storage time as well in the snubberless case. The negative $dI_A/dt$ is also different. For the snubberless turn-off case, the $dI_A/dt$ will be higher due to higher rate of charge removal resulted from high electron current density near junction J2 [F4]. This is clearly shown in Table 4-1. Positive GTO cathode current $I_K$ injects minority carriers into the p-base. Once $I_K$ becomes zero or even negative, this injection stops so the emitter junction is de-coupled from thyristor's behavior. Once the GTO's anode voltage begins to increase, the emitter junction J3 should stay inactive to let the open-base PNP alone conduct the turn-off process. Monitoring $I_K$ gives information whether the GTO is under unity-gain turn-off or not.

## 4.6   Investigation of the unity turn-off gain

The improvement in the ETO's turn-off capability is a direct result of the unity turn-off gain of the ETO. To confirm that the ETO does operate under a unity turn-off gain condition, one has to measure either the emitter or the gate current in addition to the measurement of the anode current. This is almost impossible without introducing a significant amount of inductance in the device, which, by design, has to be minimized to achieve unity turn-off gain. For this reason, numerical simulations and experimental analyses were used to confirm the unity turn-off gain in the ETO.

Based on the proposed GTO equivalent circuit model under unity-gain turn-off condition, a simplified equivalent circuit model of the ETO during the turn-off transition is shown in Figure 4-12. The gate switch $Q_G$ is modeled as a resistor since it is on during turn-off and the emitter switch $Q_E$ is modeled as its body-diode in parallel with its junction capacitor. The expected current commutation waveforms during the ETO turn-off are depicted in Figure 4-13. At the beginning of the turn-off process at t0, the emitter MOSFET $Q_E$ is turned off. The emitter switch voltage $V_C$ rises because a constant emitter current, $I_K$, charges the output capacitance of $Q_E$. $V_C$ increases almost linearly until it reaches a preset clamp voltage $V_{CP}$ ($V_{CP}$ is controlled by a

clamp circuit in the driver board and is below the breakdown voltage of switch $Q_E$). Because of the relatively small $Q_E$ output capacitance and large charging current $I_K$, this process finishes shortly.
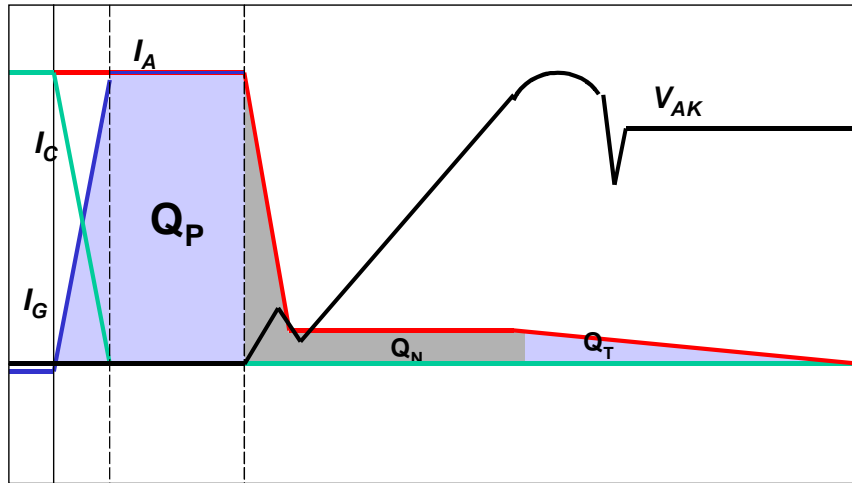


(a)
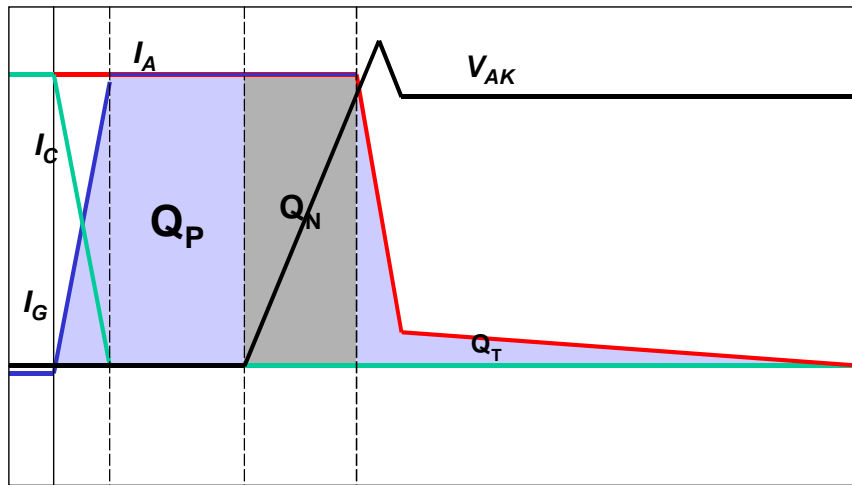


(b)

Figure 4-11 Relationship between the GTO's internal charges and its external characteristics. (a) with dv/dt snubber; (b) without dv/dt snubber.
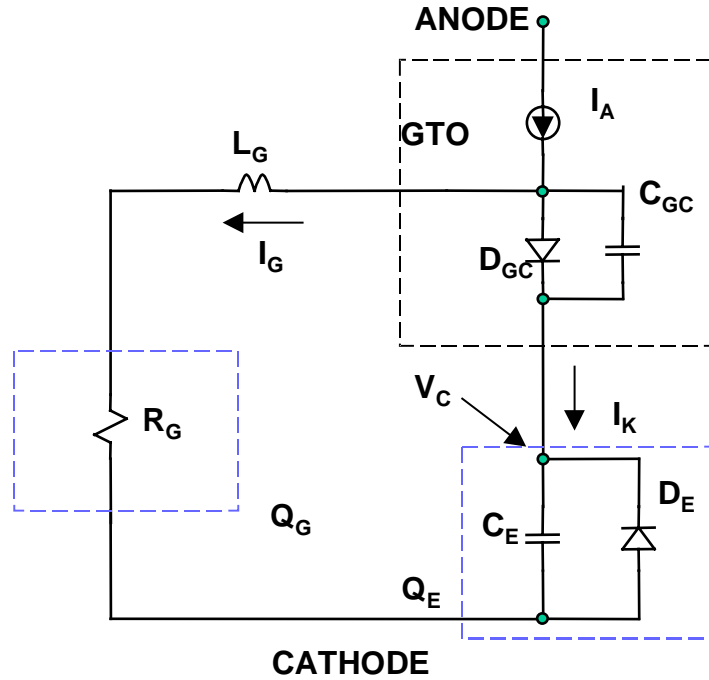
Figure 4-12 Simplified equivalent circuit model for ETO after the emitter switch $Q_E$ has been turned off.
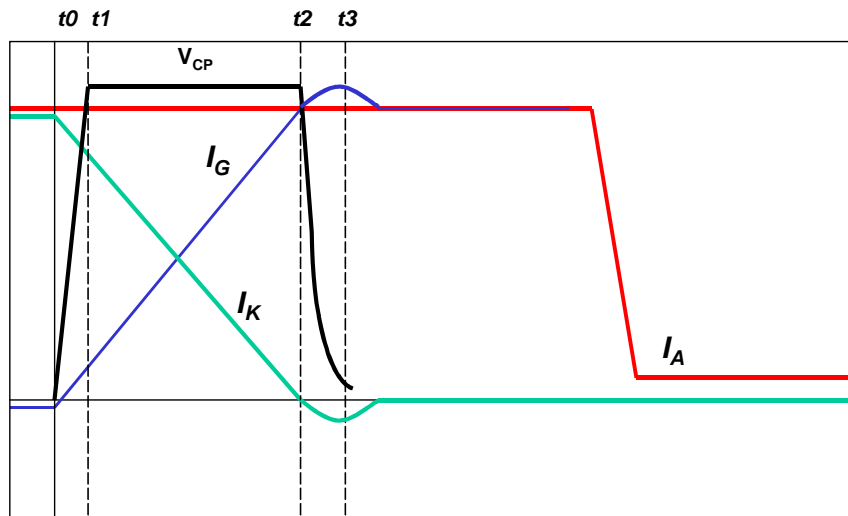


Figure 4-13 Predicted circuit waveforms during the turn-off transition of the ETO.
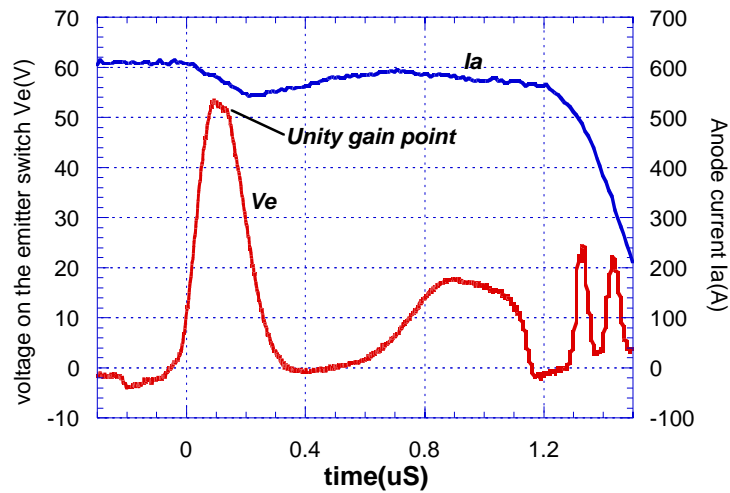
(a)
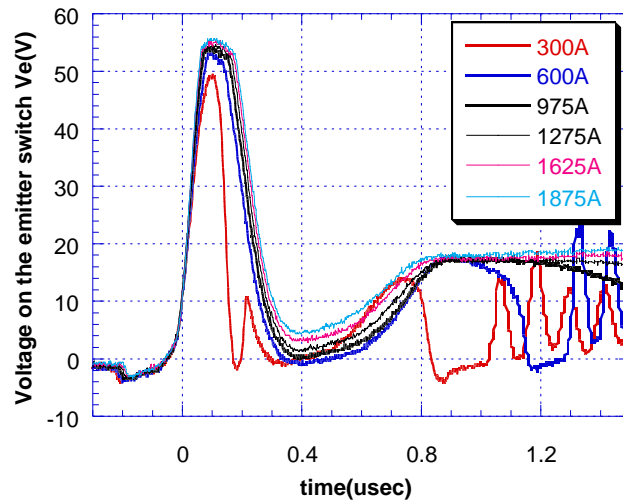


(b)

Figure 4-14 Dynamic voltage at the emitter MOSFET during ETO turn-off. (a) the emitter
MOSFET drain voltage and the ETO anode current; (b) the emitter MOSFET drain voltage at
several different turn-off currents.

Once the voltage on $Q_E$ increases, the voltage on the GTO emitter junction's positive side---the
p-base also increases. Because before the charge associated with $D_{GC}$ is removed, $D_{GC}$ can be
considered a short circuit. Thus, at the end of $V_C$ rising phase, a voltage source $V_C$ can be
considered to be applied across the gate stray inductor $L_G$ and gate switch $Q_G$, resulting in the

charging of the gate current $I_G$ and the current commutation process. During this phase, the voltage $V_C$ remains constant, and the $dI_G/dt$ in the gate loop is thus almost a constant according to (3-1).

At the moment the gate loop current $I_G$ reaches the anode current $I_A$, emitter current $I_K$ becomes zero; that is to say, the emitter diode $D_{GC}$ at this moment goes through zero current crossing point and enters a reverse recovery process. Since the emitter junction diode $D_{GC}$ in a high voltage GTO is relatively slow and has a large junction area, it will still act as a short circuit when the current starts to reverse direction. The energy stored in the output capacitor of $Q_E$ is discharged through the reverse recovery current of the $D_{GC}$, resulting in the rapid decrease of the emitter voltage $V_C$. This process also happens very quickly because of the small junction capacitance value of $D_E$. The rate of the voltage drop is very much similar to the rate of rise during the charging phase of $L_G$. The voltage will decrease to a value close to $V_G$---voltage on the gate switch, and the gate current could become larger than the anode current during this phase because of the discharge current of $Q_E$ output capacitance (or the reverse recovery current of $D_{GC}$).

Based on these analyses, it is therefore proposed that the instant (as shown in Figure 4-14 (a)) when the voltage on the emitter switch begins to decrease rapidly from the clamp voltage is the point where the unity turn-off gain is achieved. If this time instant is reached before the ETO anode voltage $V_A$ starts to rise or before the anode current starts to fall in the case with a dv/dt snubber, the device has unity turn-off gain. Another way to say this is that the recovery of the emitter junction ($D_{GC}$) happens earlier than that of the main blocking junction J2 in the GTO.

According to (3-1), the gate loop stray inductance $L_G$ can be expressed as:

$$L_G = (V_C - V_G - V_{GC}) / dI_G/dt \qquad\qquad (4\text{-}1)$$

Figure 4-14 shows experimentally observed voltage waveforms on the emitter switch $Q_E$ in ETO1045S during the turn-off at several different anode currents. The anode voltage waveforms (not shown in the figure) show that the anode voltage starts to rise at about 1.2 µs for the 600A case. Based on the above analyses, the gate loop stray inductance $L_G$ in the ETO1045S can be estimated as below. Using the 600A anode current case as an example, the time it takes for the

emitter switch voltage $V_C$ to reach the clamped voltage of 55 V is 0.12 μs. Assuming the voltage drop across the gate switch $Q_G$ is 10 V, the gate loop stray inductance $L_G$ can be calculated as 9 nH

Since the typical turn-off storage time of the ETO is about 1.5~2 μsec, it can be concluded, based on the above estimation, that the ETO technology based on traditional GTO parts has a small enough gate stray inductance and high enough commutation voltage $V_{CP}$ so that the unity turn-off gain can be fully achieved.

The unity turn-off gain theory described above is also confirmed by an extensive two-dimensional mixed mode device simulation that models the stray inductance as well as the two dimensional carrier distribution in a practical high voltage GTO structure. An inductive switching circuit that resembles the actual test condition of ETO1045S is constructed and simulated using MEDICI [K2]. The simulated circuit is shown in Figure 3-6. All elements except the GTO are modeled by their lump circuit models. The GTO is modeled by solving basic semiconductor equations. Figure 4-15(a) shows the anode voltage and current waveforms obtained from the simulation when the device turns off 1.2 kA at 1 kV. Figure 4-15(b) shows the corresponding voltage and current waveforms at the gate and the emitter. Current flowlines that correspond to different time instances during the device turn-off are shown in Figure 4-16 around the emitter junction region of the GTO.

Simulation results shown in Figure 4-15 & Figure 4-16 confirm that the unity turn-off gain theory presented herein is correct. The linear increase of the gate current during the first phase of the device turn-off is clearly shown in Figure 4-15(b). During the gate current rise phase, the GTO gate voltage is about 0.7 V higher than that of the emitter voltage because $D_{GC}$ is still conducting. Once the gate current reaches that of the anode, both gate and emitter voltage starts to decrease to about 10V corresponding to the voltage required to maintain the high gate current in switch $Q_G$. This simulation shows that the unity turn-off gain is reached within about 600 ns. It takes another 600 ns for the GTO to turn off. A slow increase of the gate current after the first fast rise is caused by the discharge of the snubber capacitor Cs (this also appears as a slow increase in the anode current in Figure 4-15(a)).

Inspection of Figure 4-16 together with Figure 4-15 provides much more needed insights into the ETO operation. During the time when the gate current is increasing, the emitter current is decreasing. This decreasing of emitter current actually happens in a non-uniform manner. Part of the emitter junction close to the gate terminal actually starts reverse recovery much earlier than the part located far away from the gate (Figure 4-16 b&c). The two different current directions in the emitter result in a net decrease of the emitter terminal current. At t = 0.65 μs, the two current components equal each other and the net terminal current is zero. This is the point when unity turn-off gain is reached. At t = 1 μs, the PNP transistor still remains in the saturation mode, but the emitter junction has been fully recovered with no current components through it. However, strong current crowding near the center of the device and near the emitter/gate boundary can still be seen. This is due to the minority carriers still stored in the upper base region of the GTO. Only after all of these charges are removed would the GTO start to turn off. This process takes another 600 ns to complete. At the end of that process, the main anode current decreases rapidly, as does the gate current. The rate of the current decrease depends on, to the first order degree, the gain of the NPN transistor. The current will decrease to a tail current value sustainable by the open base PNP transistor operation, which depends on the charges still remaining in the PNP base and the gain of the PNP transistor. Because ETOs turn off within 1.5μs, the charge in the lower PNP transistor is close to its steady state value, resulting in higher tail current value, as shown in Table 4-1. At t = 5 μs, which corresponds to the current tail stage of the device, a very uniform current conduction is seen while the voltage across the main junction reaches the bus voltage.
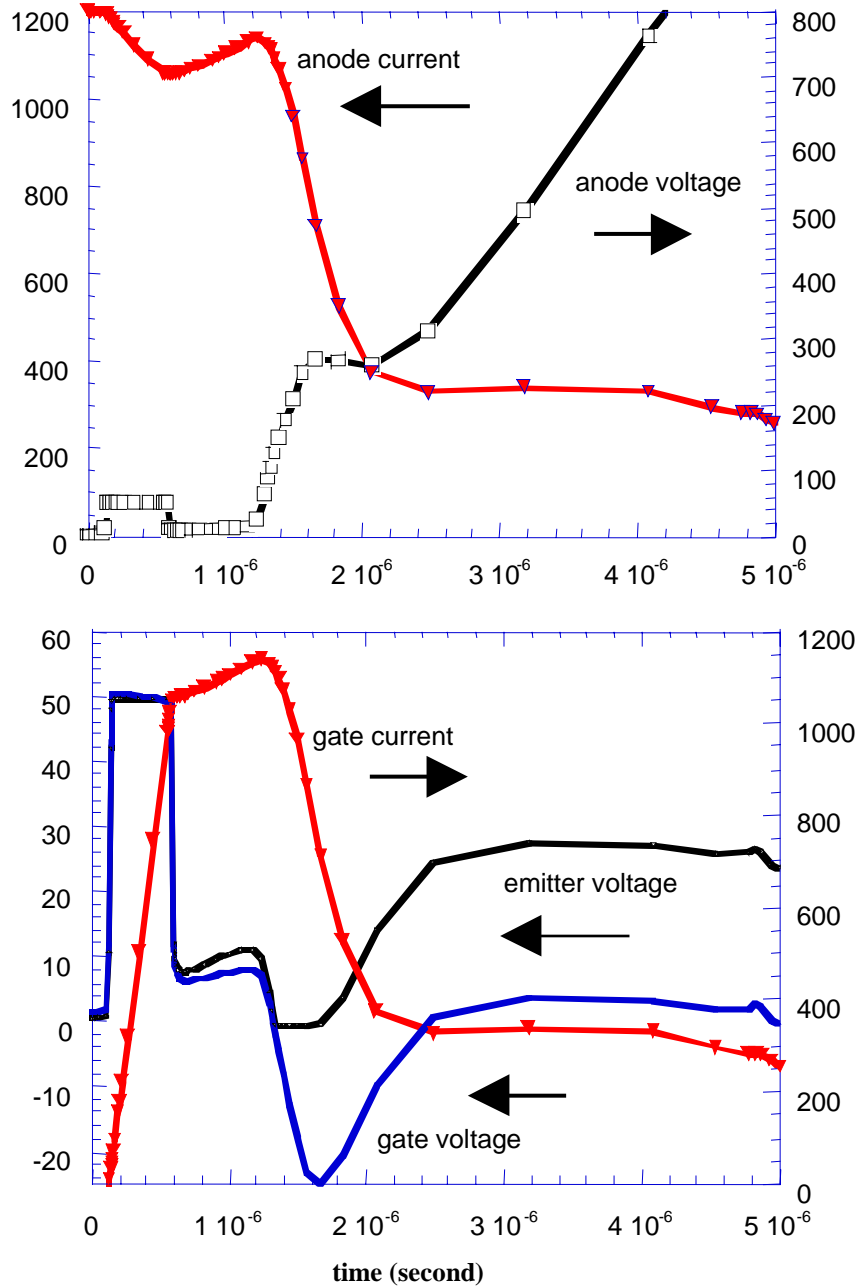
Figure 4-15 Results obtained from the mixed mode device simulation. (a) anode voltage and current; (b) gate voltage, gate current and emitter volgtage.

a) t = 0 μs

b) t = 0.55 μs

c) t = 0.65 μs

d) t = 1 μs

e) t = 5 μs
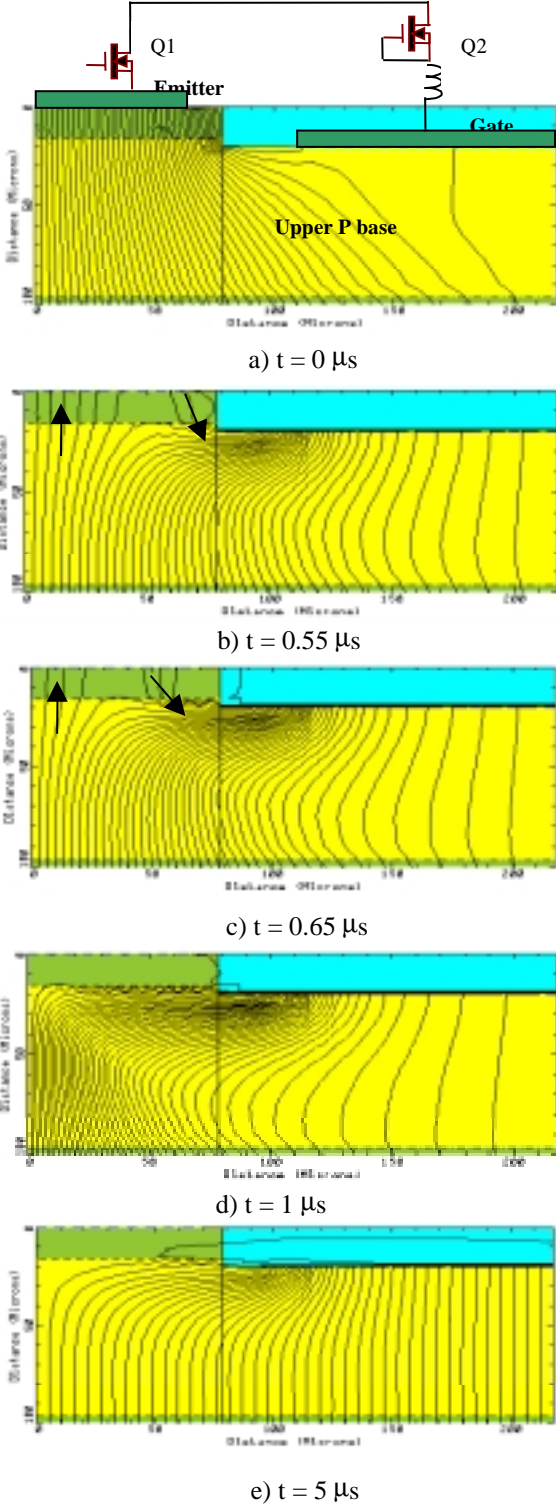
Figure 4-16 Current flowlines in the ETO at different time instances during the turn-off.

Another important phenomenon that happens in the ETO is the avalanche breakdown of the emitter gate junction J3 during the rapid fall of the main anode current. As is shown in Figure 4-15b, the rapid falling of the anode and gate current results in a negative voltage at the gate node due to the energy stored in the stray inductance $L_G$. Initially the emitter voltage follows the fall of the gate voltage. However, due to the existence of a body diode in switch $Q_E$, the voltage of the emitter terminal is clamped to about –0.6 V, forcing the emitter gate junction of the GTO to be reverse biased. This reverse biased voltage will reach the avalanche breakdown voltage of the emitter/gate junction. The avalanche process lasts until the energy stored in inductance Lg is dissipated in the emitter/gate junction and switch $Q_G$.

As a direct result of the unity turn-off gain, the ETO's RBSOA can be expanded to silicon's 200~300kW/cm$^2$ avalanche breakdown level. For the above mentioned 1kA/4kV ETO1045S, the die area is 13cm$^2$, so it should withstand 1kA snubberless turn-off at its rated voltage. Figure 4-17 shows the snubberless turn-off characteristics of ETO1045S. The peak power level is 3.0MW, or about 230kW/cm$^2$. The snubberless turn-off of the ETO will be discussed in detail in the next chapter.
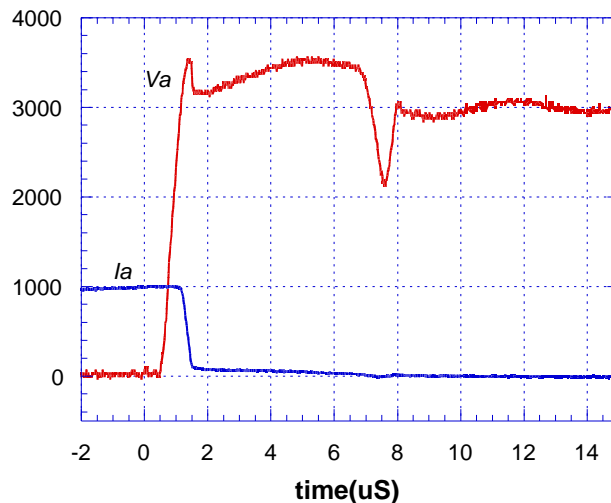


Figure 4-17 Snubberless turn-off characteristics of ETO1045S @25C.

## 4.7    Over-current protection

The ETO has an important merit that both IGBT and IGCT do not have--the on-device over-current detection capability. The emitter switch of the ETO acts as a small linear resistor in the normal conduction mode, hence the voltage drop across the emitter switch $Q_E$ reflects the current through the device and can therefore be used for feedback and protection purposes. The on-device current sensing through the emitter switch, combined with the fast turn-off speed and high maximum turn-off current, can provide the much needed over-current protection for the ETO. Figure 4-18 shows the on-device current sensing principle. In the ON state, the voltage across the emitter switch reflects the main current through the device and will be less than one volt in the normal conduction mode. Through a R/C low pass filter, any over current can generate an effective voltage output from the comparator and thus generate protection logic through the control logic unit.
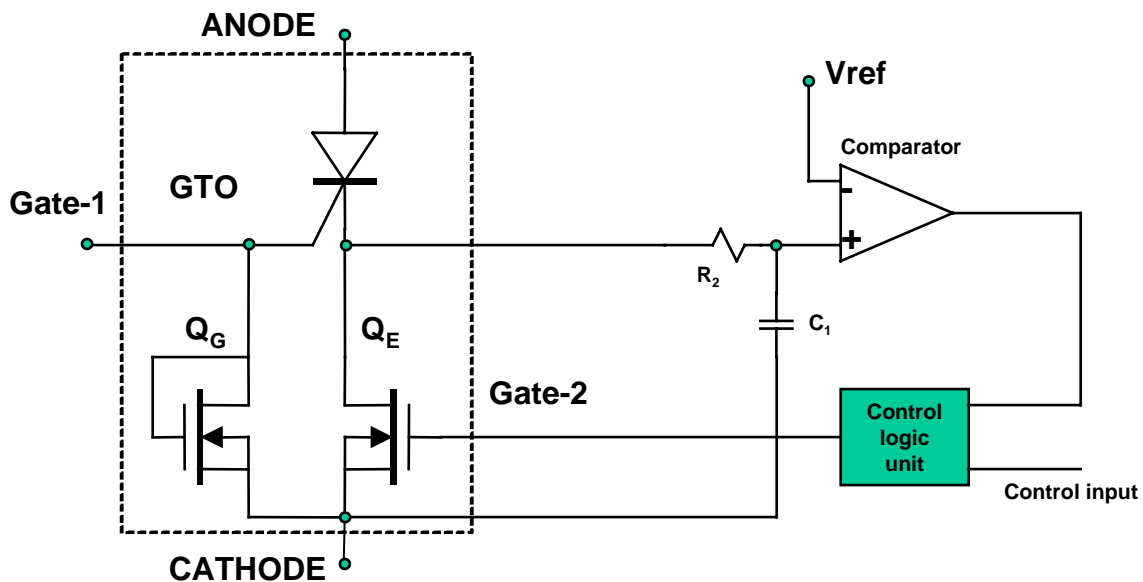


Figure 4-18 Over-current protection strategy of the ETO.

Figure 4-19 shows the experimental waveforms when an over current detection at almost 800A was detected. The time required to shut down the ETO when an over current is detected is about 1.5μsec, which is basically the storage time of the ETO.

The over-current protection for the IGBT is normally realized simply through its current de-saturation capability in the active region. This function is implemented at the gate driver board, so that fast response is guaranteed. For the IGCT, over-current protection can only be realized by an outer loop control command initiated by an external over current sensor. Deliberately designed current sensing and feedback circuits are hence required.
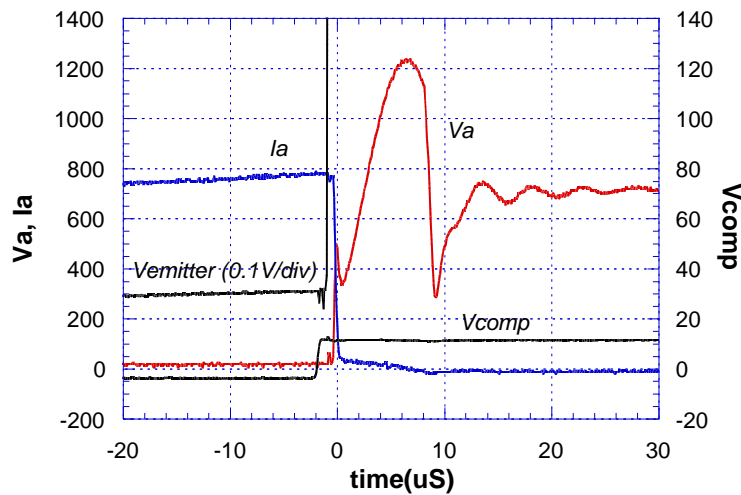


Figure 4-19 Over-current protection test waveform. The protection current level is set at 800A. The time interval between the effective output of the comparator and the main current falling edge is about 1.5μsec.

## 4.8    Conclusions

Based on its operation principles, high power ETOs have been developed ranging from 1.0~4.0 kA and 4.0~6.0 kV.  The packaging design ensures a very low gate loop stray inductance (about 10nH for different rating devices), good current sharing, and low thermal resistance. Experimental data proves that the ETO has all of its predicted merits including voltage controlled turn-off capability, high turn-on/off speed, good RBSOA that approaches silicon avalanche limitation. It is a very promising candidate for advanced power conversion in megawatt applications. The root of this new device lies in its hybrid structure, which makes use of both advantages of the GTO and the MOSFET. A comprehensive comparison study between the ETO and the IGCT and the high power IGBT [F9] has proved the competitive performance of the

ETO. A number of efforts are currently being made to demonstrate the ETO's capability at system level in CPES laboratory. A one-megawatt ETO based three-phase voltage inverter has been developed and the hardware is shown in Figure 4-20. The ETO used in the system is rated 1.0kA/4.5kV. With snubberless turn-off capability, the system component number is significantly reduced. Each phase has its di/dt snubber and local voltage clamp. The inverter can operate at a DC link up to 2.5kV. With fast switching speed, ETOs in the system are operating at a switching frequency of 1.5kHz. 3.0kHz switching is also possible at a de-rated phase current.



Figure 4-20 One megawatt three phase voltage source inverter system using ETO1045S.

# Chapter 5 Analysis of the Snubberless Operation of the ETO

## 5.1    Introduction

Snubberless switching capability is a very important feature of advanced power semiconductor switches. Traditional GTOs do not have this capability because current crowding will happen among GTO cells. They demand a bulky dv/dt snubber to shape the voltage waveform, lowering the instant power level during the turn-off transient. The failure mechanism for the traditional GTO turn-off with dv/dt snubber has been recognized as the current filamentation [H1, H2] or non-uniform current re-distribution during the turn-off transient. There are two distinct processes that can cause the current filamentation in the GTO turn-off. One happens in the turn-off storage-time stage. Due to the nature of non-uniform storage time among thousands of GTO cells, those cells with longer storage times will accumulate more current from those with shorter storage times. The failure caused by this process usually happens during the current fall when the voltage is rising due to the stray inductance of the dv/dt snubber. This failure eventually causes a physical melted hole of the size of several millimeters. At the end of the current filamentation, the current is concentrated to a very small area, and the device is destroyed due to very high power density and hence extremely high temperature at the failure location.

Another time that the non-uniform current distribution may happen is in the current tail stage. The minority carriers left in the n⁻ region are the reason for the current tail, which can last for from a few to several tens of microseconds depending on the device design. The current filamentation can be initiated when the instant power level in any of the GTO cells reaches their dynamic avalanche limitation. Strong dynamic avalanche causes positive current generation feedback, hence high power density and high temperature, which eventually leads to physical damage as in the first case.

In the two failure processes described above, the current filamentation is strongly enhanced due to the likelihood of the latch-up of the PNPN thyristor. The key to improve the GTO's turn-off capability is to establish a uniform current flow at or before the time when the voltage starts to rise.

Due to the unity-gain turn-off capability, a uniform current flow has been established (PNP current flow) in the ETO before the voltage starts to rise. Theoretical studies [H3-5] have proven that the ETO operating under unity turn-off gain has a very good RBSOA and can even conduct turn-off switching without any dv/dt snubber.

The ETO improves the RBSOA in two ways. First, due to the unity turn-off gain, the current filamentation at the storage time phase is basically eliminated because each GTO cell now has a very similar storage time. Second, the likelihood of PNPN thyristor latch-up in the ETO is greatly reduced during turn-off because the emitter switch $Q_E$ is open. This greatly reduces the chance of current filamentation caused by dynamic avalanche. Therefore, theoretically, the ETO can have a snubberless switching capability determined only by the dynamic avalanche breakdown of an open-base PNP transistor.

However, preliminary ETO snubberless turn-off tests failed at various low power levels. This chapter [H6] analyzes the new failure mechanism in the ETO snubberless operation. Possible solutions are then proposed that have expanded the ETO's snubberless turn-off capability to more than 200 kW/cm$^2$.

## 5.2    Theoretical dynamic avalanche limitation and snubberless turn-off failure of the ETO

Under the condition of unity turn-off gain, the PNPN latch mechanism is essentially eliminated and the dynamic performance of a GTO during turn-off is like an open-base PNP bipolar transistor. If uniform current conduction can be maintained, the theoretical dynamic avalanche limitation of a PNP transistor is determined by the instant power $P_{max}$ [H3] expressed in (2-13). For silicon, $P_{max}$ is in the range of 200~300 kW/cm$^2$, depending on the $E_C$ used in the calculation.

ETO1045S, a 1.0kA, 4.5kV ETO, has an effective die diameter of 4.2 cm, and a silicon area of 14 cm$^2$. Assuming a uniform current distribution during the entire turn-off transient, it should withstand 2.8 megawatts of instant peak power, or at a DC link voltage of 2.8 kV, this device should withstand snubberless turn-off at 1 kA current.

However, snubberless turn-off tests of ETO1040S failed at various lower power levels. Figure 5-1 shows an ETO1040S snubberless switching failure case. This failure is different from that of the GTO in several aspects:

- No failure in the current fall happens, even though the highest instant power appears there;

- Failure happens several(1~3) microseconds into the current tail;

- The instant power when the failure happens is very low, much lower than that during the current/voltage cross over, lower than that at the initial stage of the current tail;

- This failure is voltage dependent. When the voltage is higher, the failure point current is much lower.
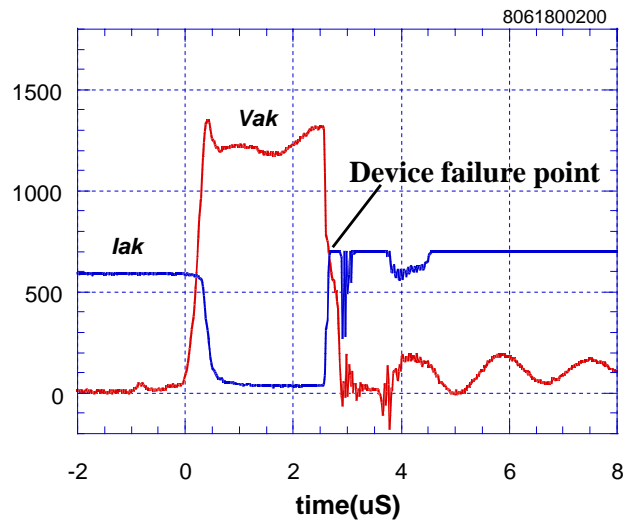


Figure 5-1 Current and voltage waveforms of ETO1040S failure during a snubberless turn-off. The flat part of the anode current after failure is due to

## 5.3    The ETO equivalent circuit model for the snubberless turn-off transient analysis

### 5.3.1    ETO snubberless turn-off process

A typical snubberless ETO turn-off characteristic is shown in Figure 5-2, which defines several important time instances during a snubberless turn-off. The turn-off operation begins from the time zero point $t_0$. Thereafter, the emitter switch $Q_E$ is turned off and the gate switch $Q_G$ is turned

on. In the period $t_0$-$t_1$, the voltage on the emitter switch rises to and stays at a clamped value (about 60 volts in the ETO1045S case). Because the internal structure of the GTO gate-cathode is a PN junction, the potential of the GTO gate will increase correspondingly, and the current from the upper PNP transistor in the GTO will be commutated to the gate switch $Q_G$ until finally the cathode current becomes zero. At $t_1$, the ETO achieves the so-called unity turn-off gain. In the time period $t_1$-$t_2$, the anode current remains constant, flowing through the PNP transistor to the GTO gate. The minority carriers in the P-base region are pulled out by this current until $t_{11}$ when the main junction $J_2$ is recovered. From $t_{11}$ to $t_2$, the minority carriers in the n⁻ region are swept out while the voltage increases to the DC link voltage value. The GTO's emitter (gate-cathode) PN junction is turned off from $t_1$ to $t_2$.
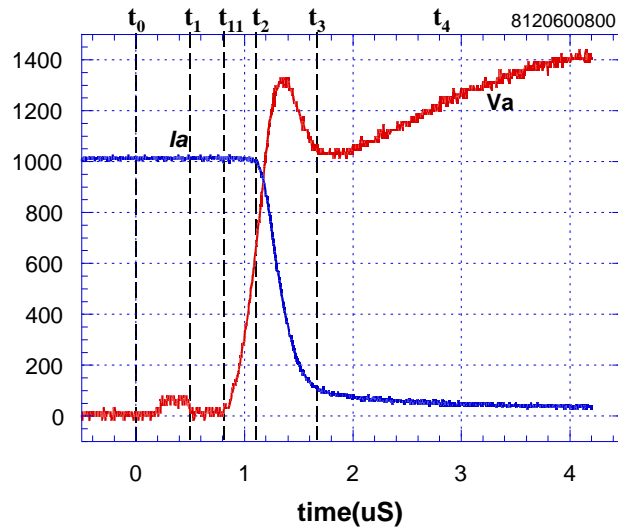


Figure 5-2 Typical ETO turn-off characteristics.

In the time period $t_2$-$t_3$, because there is no more base current injected into the base of the PNP transistor, the anode current falls to its tail value rapidly and voltage spike appears due to the di/dt applied to stray inductances. Finally in $t_3$-$t_4$ period, the anode voltage remains high while the anode current decreases slowly, determined by the minority carrier recombination in the undepleted n⁻ region.

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## 5.3.2    *Simplified circuit model for the ETO turn-off*

In order to understand the abnormal ETO snubberless turn-off failure, the simplified equivalent circuit model shown in Figure 4-12 is used for the circuit level analysis.

Major circuit parameters are listed in Table 5-1. It is worthwhile to point out that both of the capacitance effects of the emitter switch body diode $D_E$ and that of the GTO gate-cathode diode $D_{GC}$ are represented by linear capacitors. This is not accurate quantitatively but is helpful to understand the current contribution due to the charging/discharging of their capacitors and the effect of diode reverse recovery. Figure 5-3 shows the actual measured gate-cathode diode junction capacitance of the GTO used in the ETO1045S.
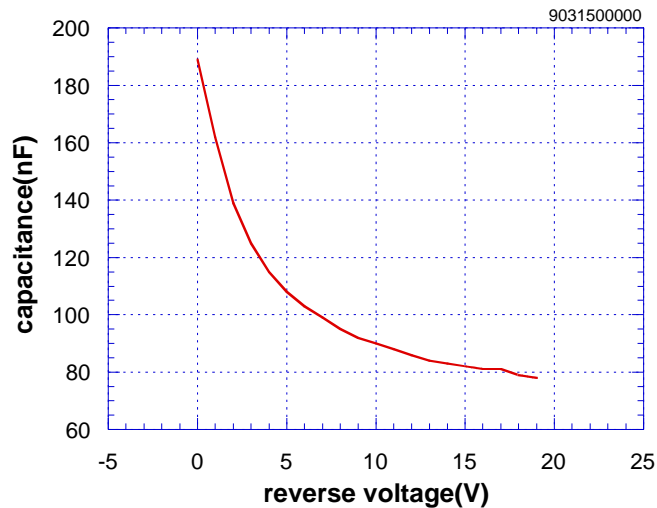


Figure 5-3 Measured junction capacitance of the gate-cathode diode in the GTO used for the ETO1045S.

To guarantee the theoretically predicated high-power snubberless turn-off capability of the ETO, it is very important to make sure that the ETO operates in open-base PNP mode and there is no positive current injection into the GTO's gate-cathode PN junction after time instant $t_1$. Any kind of injection will turn the PNPN structure back on and destroy the device.

The transient process happening in the time period $t_0$-$t_2$ has been studied in chapter 4, and no abnormal phenomenon has been found. The purpose of the circuit model here is to help analyzing the possible transient gate current injection into the emitter junction in the $t_2$-$t_4$ period.

Table 5-1 Component values used in the simulation

| $L_G$ | $R_G$ | $C_{GC}$ | $C_E$ | $V_B$ |
|-------|-------|----------|-------|-------|
| 10nH  | 0.002Ω | 60nF    | 20nF  | 20V   |

## 5.4    Simulated turn-off transient process and current injection analysis

Based on the above circuit model, PSpice simulations were carried out to understand the dynamic transient process of transferring the emitter current from the ETO's main current path to the gate path. Figure 5-4 shows the simulation result of a 1.0 kA snubberless turn-off waveform.

Before the anode current $I_A$ begins to decrease, the GTO cathode current is zero, having already been commutated to the gate path. When the anode current begins to fall, the negative $di_A/dt$ introduces a negative voltage on the stray inductor $L_G$. This voltage is applied on the GTO gate-cathode diode $D_{GC}$ through the body diode $D_E$ of the emitter switch. However, because $BV_{GC}$---the reverse breakdown voltage of $D_{GC}$, is low (20V for normal GTOs), reverse breakdown happens and reverse current flows through $D_{GC}$. The maximum negative $dI_G/dt$ through the $L_G$ loop is therefore limited approximately by ($BV_{GC}/L_G$), which is 2.0kA/μsec in the considered ETO1045S case.    Because the anode current $dI_A/dt$ is much higher than the achievable $dI_G/dt$, the reverse breakdown current through the gate-cathode diode is required to maintain current flow in $L_G$. The lower $dI_G/dt$ on the stray inductor $L_G$ and the reverse current through $D_{GC}$ are clearly shown in Figure 5-4(a).

When the current in the gate path $I_{LG}$ finally reaches the anode current tail level, the reverse current through the GTO gate-cathode diode becomes zero. If, hereafter, the anode current flows through the GTO gate completely, the cathode current can remain zero. However, effective transient current injection into the GTO gate-cathode diode is clearly shown in Figure 5-4 (b).

Detailed circuit analysis ascribes this current injection to the reverse recovery effect of the emitter switch body diode $D_E$ along with the parasitic capacitance $C_{GC}$ of the GTO gate-cathode diode. The time when the reverse breakdown current in $D_{GC}$ becomes zero, its parasitic capacitor $C_{GC}$ is fully charged and the body diode $D_E$ of the emitter switch has not been recovered. After this point, $C_{GC}$ will discharge through $D_E$, $R_G$ and $L_G$, building current in the GTO cathode and causing current to decrease in the gate path. Before $C_{GC}$ is completely discharged, the cathode current flows through the parasitic capacitance. This means there is no minority carrier injection into the GTO gate even though there is a positive gate current. However, after $C_{GC}$ is completely discharged, the diode $D_{GC}$ will take over the current---this will be an effective turn-on current injection to the GTO gate. This process continues until the emitter switch body diode $D_E$ is recovered and blocks voltage. The cathode current comes to zero finally.

In the ETO snubberless turn-off situation, the anode voltage of the device is already high in the current tail stage. The current injection into the gate of the GTO turns some GTO cells on, introducing current crowding or filamentation. With higher anode voltage, the current gain of the upper PNP transistor increases and it is easier to turn on the GTO cells. This can explains the special failure in the ETO.



(a)

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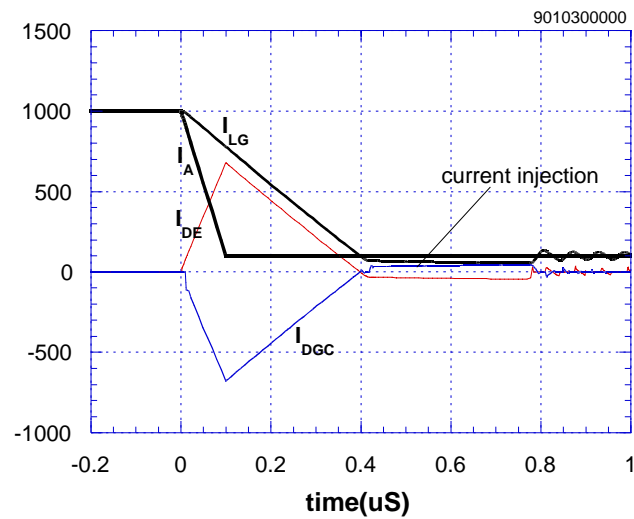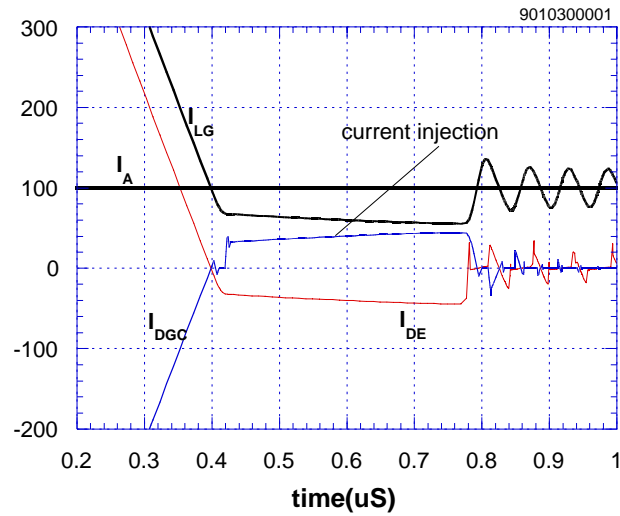
(b)

Figure 5-4 (a) Simulation results show that there is current injection due to the reverse recovery of the emitter body diode. (b) Zoom-in view of the current injection into the emitter of the GTO.

In conclusion, we believe that a new mechanism that leads to the failure of the ETO snubberless turn-off is identified. The discharging of the GTO gate-cathode junction capacitor and the reverse recovery of the emitter switch $Q_E$ body diode can introduce an effective current injection into the GTO gate-cathode junction.

## 5.5    Possible solutions to the ETO snubberless turn-off

### 5.5.1    Voltage clamp

If the emitter switch body diode $Q_E$ can be recovered before the end of the GTO gate-cathode diode reverse breakdown, the forward current injection will no longer appear. One solution therefore is to add an external circuit to the cathode point of the GTO that helps to recover $D_E$. In the circuit shown in Figure 5-5, the voltage clamp circuit has a 5V voltage output and a 400A maximum current capability.
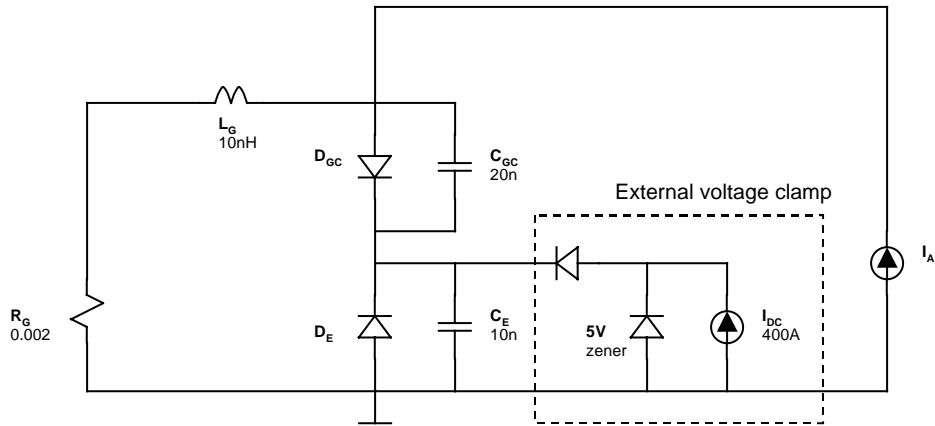
Figure 5-5 PSpice simulation circuit for the ETO with external voltage clamp.

Figure 5-6 shows the simulated waveforms for this case. It is clear that the reverse recovery of the body diode $D_E$ finishes before the end of $D_{GC}$ breakdown, and there is no forward current injection into the $D_{GC}$. A newer generation of ETO1045S has been developed with this concept. They have demonstrated snubberless turn-off at 1.0 kA/ 3.0 kV with a peak instant total power of 2.5 MW, or about 200kW/cm$^2$ average power as shown in Figure 5-7. This power constant is close to the theoretical limitation of a PNP transistor turn-off determined by the dynamic avalanche.
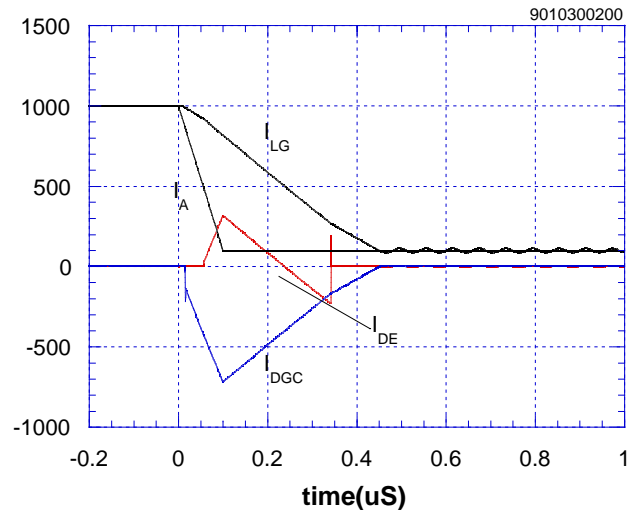
Figure 5-6 Pspice simulation results for the ETO with external voltage clamp which has a 400A maximum current capability.

The external voltage clamp's current capability is related to the reverse recovery of $D_E$. The current injection should be high enough so that during the whole $D_E$ reverse recovery period, the GTO gate-cathode diode is in breakdown state. Hereafter, $C_{GC}$ still needs to be discharged. The discharging happens among $C_E$, $R_G$ and $L_G$. Since $C_{GC}$ is bigger than $C_E$ in ETO1040S, the diode $D_{GC}$ can maintain reverse bias after all. The external current injection is only required for about half a microsecond, so the required power is very low.
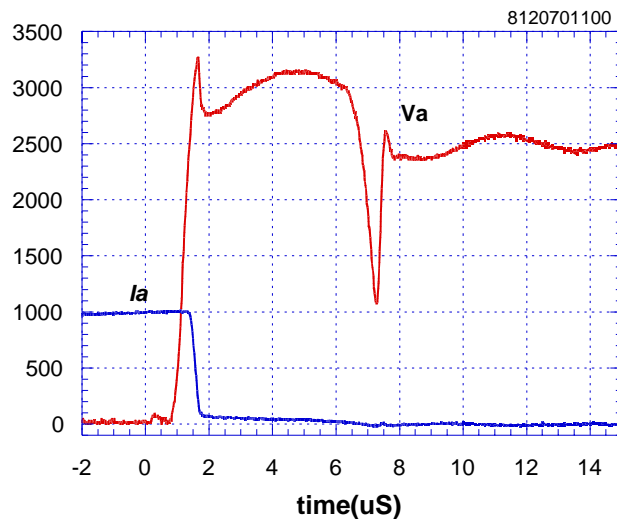


Figure 5-7  ETO1040S snubberless turn-off characteristics with external current injection solution.

### 5.5.2    *Lower gate stray inductance solution*

If the emitter switch body diode $D_E$ never conducts, there will not be any reverse recovery problem, hence there will not be any current injection to the GTO during the transient. The reason for possible current through the emitter switch body diode is the breakdown of the GTO gate-cathode diode. This breakdown is due to the high negative voltage introduced by the gate stray inductor $L_G$ and the negative $dI_A/dt$ of the anode current. The negative voltage is ($L_G dI_A/dt$). Once this value is greater than $BV_{GC}$, reverse breakdown current will appear as well as the conduction of the body diode $D_E$. So the critical condition for the ETO to avoid the GTO gate-cathode junction breakdown, hence to avoid the effective current injection into the GTO gate is:

$$L_G \frac{di_A}{dt} < BV_{GC} \qquad\qquad (5\text{-}1)$$

In the above-mentioned 1.0 kA/3.0 kV snubberless turn-off case, the maximum turn-off transient $di_A/dt$ is about 3.0 kA/μsec. To make the ($L_G dI_G/dt$) less than 20V, $L_G$ should be less than 7nH.

A new generation of ETO that features "four gate", was built to reduce the gate path stray inductance. Because there are four separate gate connections inside the GTO, the equivalent total stray inductance should be only one-fourth of a conventional ETO, i.e., about 3nH. This device survived 1.0kA/1.5kV snubberless switching without external voltage clamp.
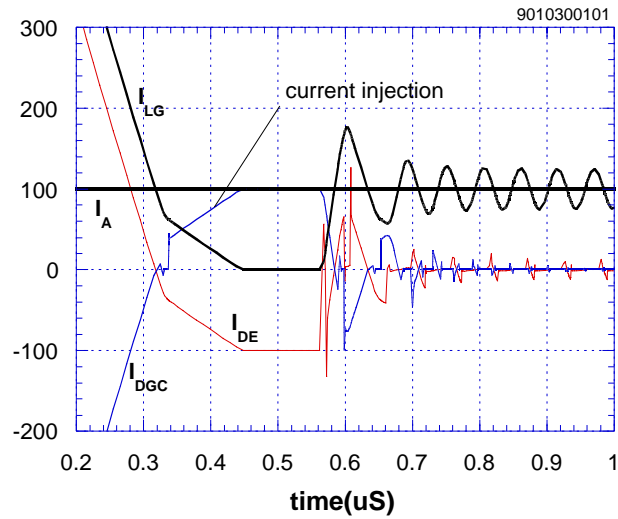


Figure 5-8 Simulated transient current injection into the GTO gate when the gate switch is driven by itself.
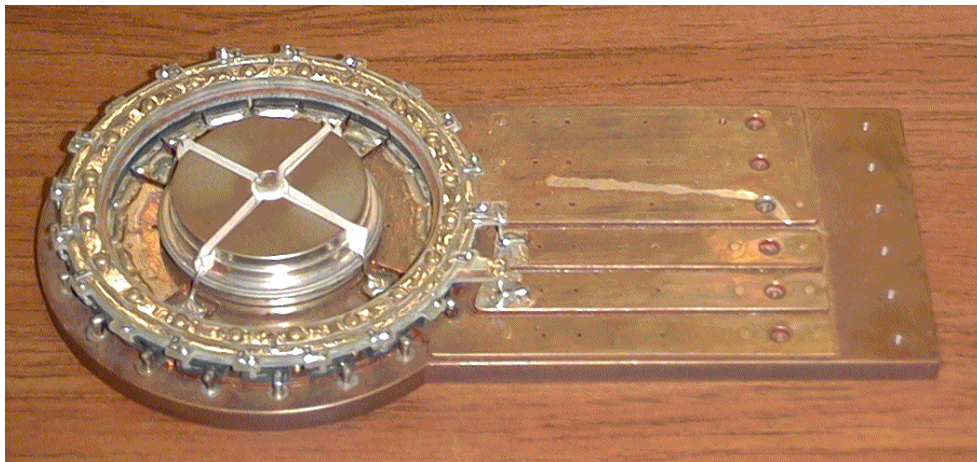


Figure 5-9 A four-gate ETO housing. The equivalent $L_G$ is about 3.5nH.

*5.5.3    Extra ETO design criteria due to snubberless turn-off requirement*

With the low gate loop stray inductance solution, the voltage ($L_G dI_A/dt$) is still there. This voltage will reverse bias the GTO's gate-cathode junction and charge its junction capacitor $C_{GC}$. Once the negative $dI_A/dt$ disappears, $C_{GC}$ will resonant with $L_G$ and $C_E$, generating voltage and current oscillation. Under certain condition, this oscillation will generate effective current injection into the GTO's gate.

Similar phenomenon exits in the solution with external voltage clamp. After the body diode of the emitter switch is recovered and the negative $dI_A/dt$ disappeared, the pre-charged $C_{GC}$ will resonant with $L_G$ and $C_E$, generating voltage and current oscillation, hence the effective current injection into the GTO's gate as well.

Figure 5-10 shows this parasitic resonance equivalent circuit. To make sure that there is no effective current injection into the GTO's gate-cathode junction, $D_{GC}$ should always be reverse biased. Considering the initial condition of $V_{DGC}>0$, $V_{DE}=0$ and $I_G=0$, the instant voltage on $D_{GC}$ can be expressed as:

$$V_{DGC}(t) = V_{DGC}\left(1 - \frac{1}{L_G\omega_0}\frac{1}{\omega_0 C_{GC}}(1-\cos\omega_0 t)\right) \tag{5-2}$$

where $\omega_0 = 1/\sqrt{L_G \dfrac{C_{GC}C_E}{C_{GC}+C_E}}$. To guarantee that $V_{DGC}(t)$ is greater than zero ($D_{GC}$ reverse bias), equation (5-2) gives the condition:

$$C_E < C_{GC} \tag{5-3}$$

If the initial condition of $V_{DE}$ is greater than zero, the oscillation amplitude will be smaller if the rest condition is the same since $V_{DE}$ tends to reverse bias $D_{GC}$. Thus equation (5-3) can be taken as the bottom line to design $C_E$.

With this limitation, the number of paralleled emitter MOSFET should be limited. This adds a limitation to reduce the added forward voltage drop due to the emitter switch.
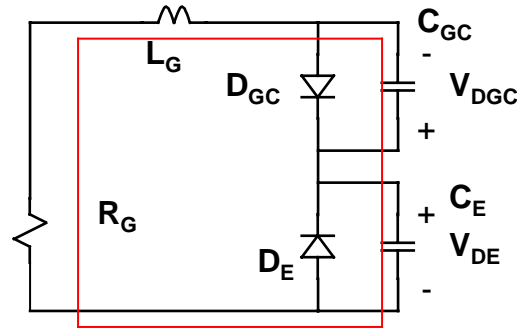
Figure 5-10 Parasitic resonance among $C_{GC}$, $C_E$ and $L_G$.

## 5.6    Discussion

### 5.6.1    When the gate switch is self-driven

The ETO gate switch can be self-driven as well as driven through a gate driver. By shorting its gate and drain together, the MOSFET $Q_G$ acts as a zener diode that can be turned on or off automatically according to the voltage applied. This feature helps the ETO to maintain its off state even when the gate driver is not active. However, this structure worsens the current injection problem during the turn-off transient. Simulation is conducted by adding a 5V zener in series with $R_G$. Figure 5-8 shows the simulation results. After the initial step, the injection current increases rapidly until the current tail. This faster $dI_G/dt$ is due to the added zener in the loop.

### 5.6.2    Experimental observation of the current injection

It is very hard to directly measure the above-mentioned current injection. Any added measurement tool will significantly change the gate loop stray inductance, therefore the basis for the unity turn-off gain will be changed. On the other hand, the current injection is considered detrimental; direct measurement will destroy the device.

A modified ETO topology shown Figure 5-11 is designed to observe the current injection indirectly. The gate switch is connected in the self-driven state, a ceramic capacitor $C_H$ is connected across the GTO's gate/cathode. The connection is made so that the $C_H$ and GTO gate-cathode loop stray inductance is less than that in the ($Q_E$ $Q_G$ GTO gate-cathode) loop.

The device turn-off transient process changes a little in this case. When $Q_E$ is turned off and $Q_G$ is turned on, $C_H$ will be charged to a high value. When finally the cathode current is completely commutated to the gate path, the reverse recovery and reverse breakdown of the GTO gate-cathode junction will bring the voltage on the $C_H$ down to a stable level. During the anode current fall stage, the reverse breakdown of the GTO gate-cathode junction happens too. Unlike the regular ETO case, the breakdown current will take the path of $C_H$ instead of the body diode of the emitter switch at the beginning. This current will in return bring the voltage on $C_H$ down. Once the reverse breakdown finishes, the GTO gate-cathode junction will discharge. This discharging process mainly takes ($C_H$ $L_G$ $C_{GC}$) loop. The effective current injection due to the discharging of $C_{GC}$ turns on some of the GTO cells, increasing anode and cathode current. The increased anode current, in return, will increase the voltage on $C_H$, which commutates the cathode current back to the gate and turns off the device again. Experimental results are shown in Figure 5-12. The current bump in the anode current tail corresponds to the current injection.
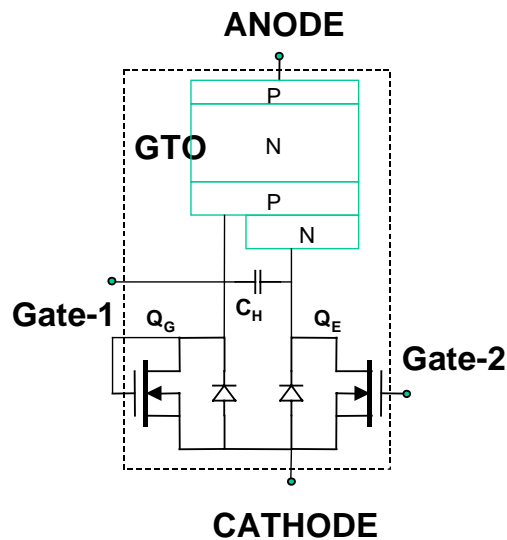
Figure 5-11 A modified ETO structure. The $C_H$ is the capacitor added externally.

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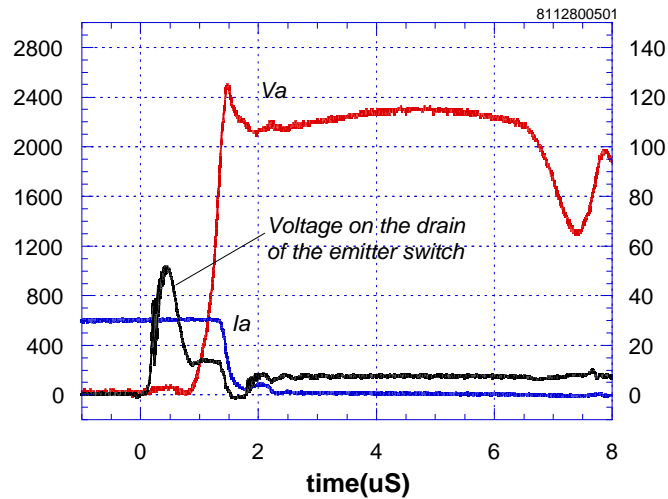
Figure 5-12 Experimental results show the current bump in the current tail due to effective current injection.

### 5.6.3    Similar mechanism in the IGCT

The effective current injection also exists in the IGCT. Figure 5-13 shows the IGCT structure. Because the gate loop stray inductance $L_G$ is very small (typically 3nH as specified [L4]), the negative voltage source $V_{OFF}$ can commutate current from the IGCT cathode to gate quickly, realizing unity turn-off gain similar to that of the ETO. During the anode current fall stage, the negative voltage introduced by $L_G$ along with the negative power supply $V_{OFF}$ will causing reverse breakdown of the IGCT gate-cathode diode. When finally the reverse current in the gate-cathode diode comes to zero, the same discharging process due to the parasitic capacitance $C_{GC}$ of the gate-cathode diode will happen. This discharging is among $V_{OFF}$, $L_G$ and $C_{GC}$. Assuming $C_{GC}$ is linear and it is charged to the breakdown voltage $BV_{GC}$ of $D_{GC}$, then the condition to avoid effective current injection is:

$$V_{OFF} > \frac{BV_{GC}}{2} \tag{5-2}$$

Normally, the turn-off voltage $V_{OFF}$ is selected as high as possible to accelerate the current commutation, so condition (5-2) is normally met and the IGCT in practice does not have the current injection problem. On the other hand, high turn-off voltage $V_{OFF}$ slows down the decreasing $dI_G/dt$ in the IGCT gate after the turn-off is complete because $dI_G/dt=(BV_{GC}-V_{OFF})/L_G$ and requires more power from its gate driver.
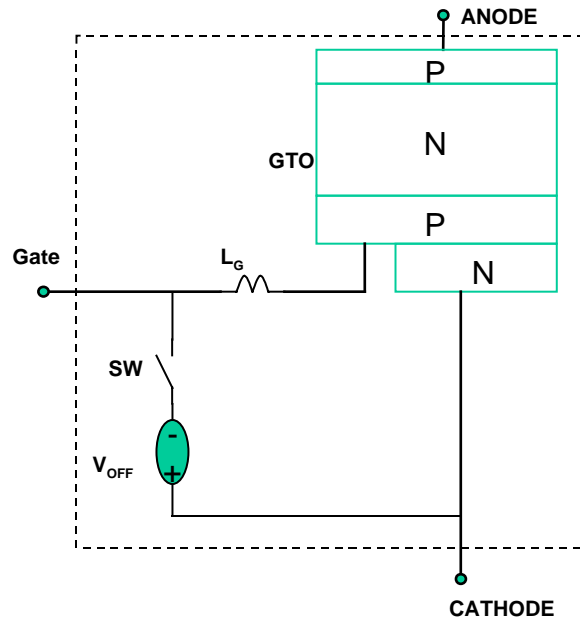
Figure 5-13 The IGCT turn-off principle.

### 5.6.4    Current injection in the MTO

The MTO thyristor is another hybrid GTO-MOSFET structure that improves the control of the GTO. Figure 5-14 shows its principle. Compared to the ETO, the MTO does not have the emitter switch, but does have a very low gate loop stray inductance $L_G$. By turning on the gate switch $Q_G$, the GTO gate-cathode diode is shorted and the cathode current can be commutated to the gate if $Q_G$ has very low ON impedance, realizing unity turn-off gain.

The same current injection mechanism exists in the MTO during the turn-off transient. When the anode current is decreasing, the gate loop stray inductance $L_G$ will introduce a negative voltage ($L_G di_A/dt$), which will be applied on the GTO reverse gate-cathode PN junction. After the anode current decrease, the parasitic capacitor $C_{GC}$ of the GTO gate-cathode diode will discharge through the $L_G$, $Q_G$ and $C_{GC}$ loop and eventually introduce forward current injection into the GTO gate-cathode junction.

To avoid an effective minority carrier injection into the GTO gate-cathode junction, the forward voltage on this junction should be below a critical value so that the junction is not conducting. So

for the MTO, the condition that can avoid effective current injection to the GTO gate-cathode junction is:

$$L_G \frac{di_A}{dt} < V_{crit} \tag{5-3}$$

where $V_{crit}$ is a critical voltage value that causes strong current injection. $V_{crit}$ can be considered equal to the turn-on voltage of the emitter junction of a GTO, which is about 0.3V. This condition is very hard to meet and requires extremely low $L_G$ design.

In the case of non-uniform transient process, even smaller ($L_G dI_A/dt$) can introduce effective current injection to one GTO cell.
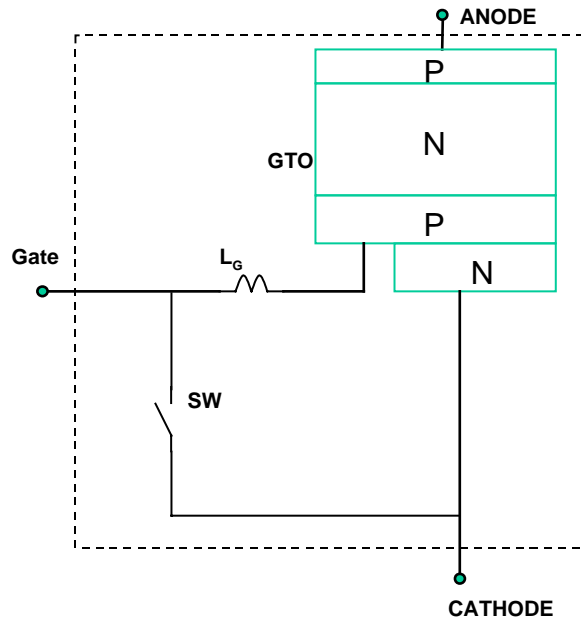


Figure 5-14 The MTO turn-off principle.

## 5.7    Conclusions

The effective current injection into the GTO gate during the turn-off transient, introduced by the discharging of the GTO emitter junction parasitic capacitor along with the reverse recovery of the emitter switch body diode, has been found and analyzed as the failure mechanism for the previous generations of ETOs. In the ETO, the gate stray inductance is significant and the high $dI_A/dt$ is harmful to the device's snubberless operation. Through a carefully designed external circuit, the above-mentioned injection can be eliminated and newer generation of the ETO can operate at snubberless condition close to the theoretical limitation determined by the PNP

transistor. Future ETOs with lower gate stray inductance will have full snubberless switching capability without any external circuit. This capability will enable the ETO to compete with devices such as IGCT and IGBT in the high power applications. For the IGCT, although similar current injection mechanism exists, it will not cause problem when the turn-off voltage is not very low. On the contrary, this could be a major issue that hurts the snubberless turn-off capability of the MTO.

# Chapter 6 Series and Parallel Operation of the ETO

## 6.1    Introduction

Device-level series connection has been the most popular practice in industry to boost system power output. For a system equipped with series connected devices, the operating voltage is increased so the current can be reduced to save connections and conduction loss. The stray inductance becomes less critical, allowing simpler system layout design.

The key issue in series connection is how to ensure uniform dynamic voltage sharing at both turn-off and turn-on transition. For IGBTs, the dynamic voltage sharing can be achieved through active gate control without additional component [I1]. However, because there is no FBSOA, series-connected GTOs have to use passive voltage-balancing capacitor $C_S$ as shown in Figure 6-1. Under inductive load turn-off condition, the voltage difference between these two GTOs due to the storage time difference $2\Delta t_S$ is given by:

$$\Delta V = 2 I_A \Delta t_S / C_S \qquad (6\text{-}1)$$

The storage time of a traditional high power GTO is about 20μsec [D3], which is determined by the gate driver and GTO's parameters such as carrier lifetimes and doping. A storage time spread of ±10% is reasonable for GTOs made from the same process [I3]. Thus to maintain a maximum voltage difference of ±10% of their rated voltage during turn-off phase for two 1kA/4.5kV GTOs, the voltage-balancing capacitance required will be 4μF. This big capacitor should be avoided for the following three reasons. First, this high voltage high-speed capacitor is very expensive. Second, a big $C_S$ increases the energy trapped every time during turn-off ($0.5C_SV^2$), leading to the increased power dissipation in the discharge resistor $R_S$. Third, a big $C_S$ requires more switching transient time and limits the applicable switching frequency of the system.

To alleviate these problems, a group of devices with much less storage time dispersion are required.
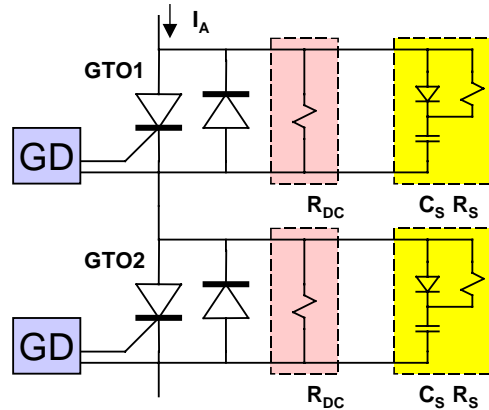
Figure 6-1 Two GTOs series connection topology.

Device paralleling is another device-level option to increase the power handling capability of a system. Parallel connection can significantly increase a device's current capability, which is required in some applications such as circuit breakers where no single device can handle the current. The GTO is by far the device with the highest current handling capability and full gate control. The state-of-the-art six-inch GTO has a maximum turn-off current capability of 6.0 kA. However, the parallel operation of traditional GTO is very hard. In the case of two GTOs in parallel, the current will try to crowd to the slower device during the turn-off transient. With more current, the carrier injection of the slower device becomes stronger so the critical gate current to turn off the device also increases, which leads to a further delayed turn-off process for the slower device. This is therefore an undesired positive feedback process. The slower GTO can easily enter a state that is beyond its turn-off capability. Traditionally, a dynamic current balancing inductor $L_B$ is required for each paralleled device to prevent current crowding as shown in Figure 6-2. Large $L_B$ increases voltage spike applied on the device and increases switching losses as well as cost and size of the system.

Issues of paralleling devices include ensuring DC current sharing and dynamic current sharing. Devices with uniform, resistive and positive temperature coefficiency I-V characteristics will give a good DC current sharing (this is the case for MOSFETs). The parameter uniformity of paralleled devices, on the other hand, determines the dynamic current sharing.

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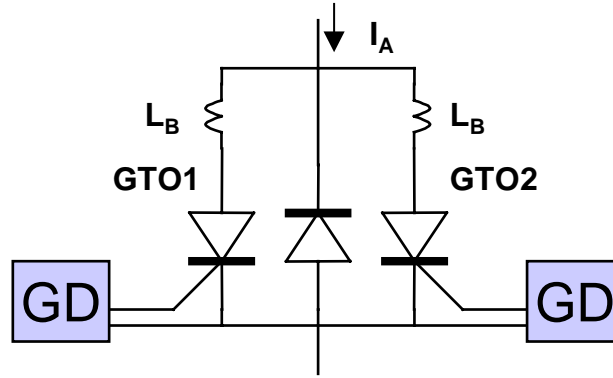
Figure 6-2 Two GTOs parallel connection topology.

Devices with less storage time spread are also required to solve current crowding for parallel connected devices.

## 6.2    ETOs in series connection

### 6.2.1    Dynamic voltage sharing during turn-on and turn-off

With significantly decreased storage time, ETOs have much better storage time dispersion than that of the GTO. A storage time survey of six ETOs made from six commerical GTOs is shown in Table 6-1. The difference is within ±10% and the absolute value of $\Delta t_{S(max)}$ is reduced to about ±100nsec.

Two 1.0kA/4.5kV ETO1045S with a storage time difference of 100nsec were used to demonstrate the improved series connection performance. The current is measured by a Rogowski coil. The dynamic voltage balancing capacitance is reduced to 0.5μF due to the reduced $\Delta t_S$. Figure 6-3 and Figure 6-4 show the dynamic voltage on these two devices during turn-off and turn-on respectively. The voltage difference during turn-off is only 0.2kV, which is less than 5% of their rated voltage, when they are turned off at their rated current (1.0kA). The observed turn-on delay time difference is essentially nothing. Considering the turn-on di/dt snubber is normally required to control the reverse recovery of the diode, turn-on is not a practical concern in series connection.

Table 6-1 ETO storage times @ 125C

|                | ETO1 | ETO2 | ETO3 | ETO4 | ETO5 | ETO6 |
|----------------|------|------|------|------|------|------|
| $t_s$ (μsec)   | 1.3  | 1.4  | 1.3  | 1.4  | 1.2  | 1.2  |
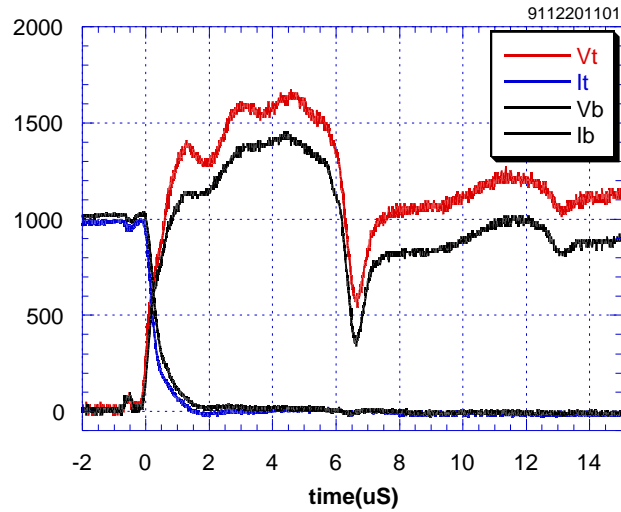


Figure 6-3 Turn-off of two series connected ETOs @ 0.5μF voltage balancing capacitance.
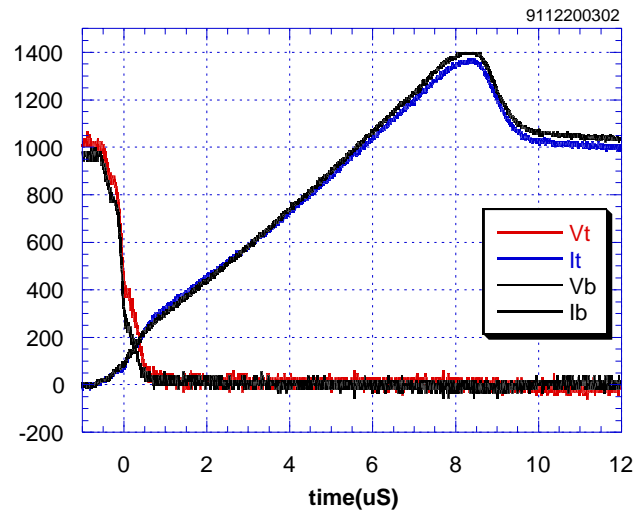


Figure 6-4 Turn-on of two series connected ETOs @ 0.5μF voltage balancing capacitance.

*6.2.2    Storage time adjustment*

The storage time of the ETO can be further adjusted by inserting a resistor in the gate of the emitter switch $Q_E$ of the ETO, similar to the case of the IGBT. This gate resistor will delay the turn-off process of the emitter switch and eventually delay the turn-off process of the ETO. Since this resistor stays with the device instead of with the gate driver, ETO's storage time can be calibrated easily. Figure 6-5 shows the experimental waveforms and Table 6-2 is a summary of the relationship between the storage time and the gate resistance for one specific ETO. With tightly matched storage time, ETOs can even do series connection without the help of dv/dt snubber with an acceptable voltage sharing performance.
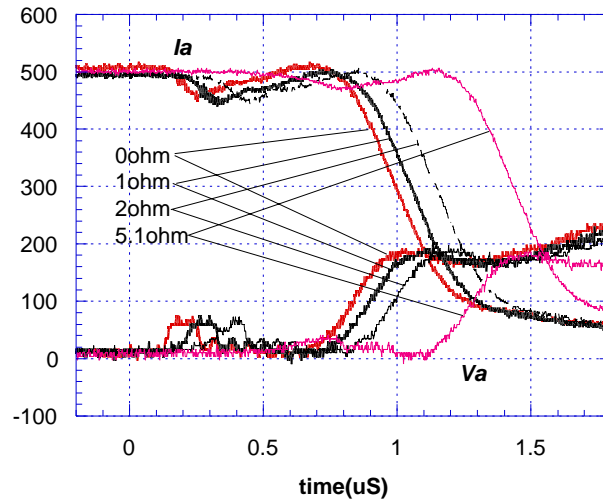
Figure 6-5 ETO's storage time dependency on the gate resistance of the emitter switch.

Table 6-2 ETO storage time increase with respect to its gate resistance

| $R_G(\Omega)$ | 0 | 1 | 2 | 5.1 |
|---|---|---|---|---|
| $\Delta t_S$ (usec) | 0 | 0.06 | 0.15 | 0.42 |

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### 6.2.3    *System savings due to the reduced $\Delta t_S$*

The dramatically reduced storage time difference $\Delta t_S$ implies big saving at system level. For a system employing series connected devices, if:

devices' storage time dispersion is $t_S \pm \Delta t_S$;

maximum designed static voltage for each device is $V_S$;

dynamic voltage balancing capacitance is $C_S$;

maximum turn-off current is $I_M$;

then the maximum voltage sharing difference is:

$$\Delta V_M = 2\, I_M\, (\Delta t_S / C_S) \tag{6-2}$$

$\Delta V_M$ can also be related to the maximum permitted static voltage $V_S$ through:

$$\Delta V_M \equiv k V_S \tag{6-3}$$

where $k$ is the voltage sharing index. From (6-2), $k$ can be expressed as:

$$k = 2\, (I_M / V_S)\, (\Delta t_S / C_S) \tag{6-4}$$

For $n$ devices in series connection, the worst case is that $(n-1)$ devices are having a longest storage time $(t_S + \Delta t_S)$ and only one device has a shortest storage time $(t_S - \Delta t_S)$. Then the total voltage $V_{DC}$ these n devices can handle is:

$$V_{DC} = V_S + (n-1)(V_S - \Delta V_M)$$

$$= n V_S - (n-1)\, \Delta V_M \tag{6-5}$$

Thus, the number of devices needed to handle $V_{DC}$ is:

$$n = (V_{DC} - \Delta V_M)/(V_S - \Delta V_M)$$

$$\approx V_{DC}/(V_S - \Delta V_M)$$

$$= (1/(1-k))\, (V_{DC}/V_S) \tag{6-6}$$

In an ideal case where all devices have the same storage time and share the same voltage during turn-off transient, $k$ is thus zero so the devices needed is minimum $(V_{DC}/V_S)$. When the sharing difference $k$ is increasing, the normalized number of devices needed is increasing according to (6-6) and is depicted in Figure 6-6.

$$K = (\Delta V_M / V_S) = 2\, I_M / V_S\, (\Delta t_S / C_S)$$
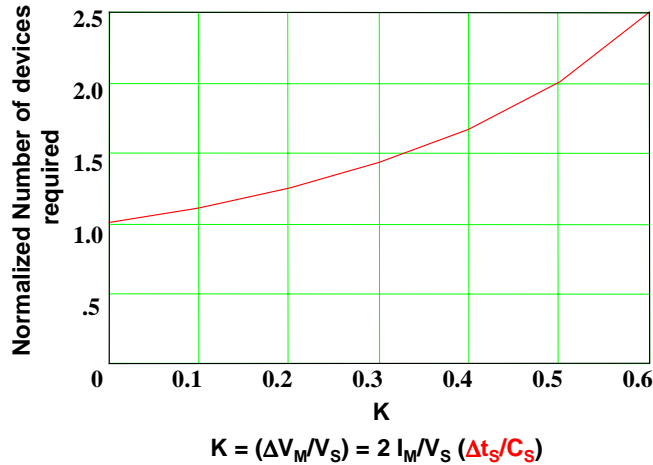
Figure 6-6 Normalized number of series-connected devices needed to handle a certain voltage.

For a system employing GTOs in series, if the voltage sharing index $k$ is selected 0.5, then twice as many as the minimum devices are needed from Figure 6-6. If the devices are replaced with the ETO, which has only one twentieth the storage time difference, then the voltage sharing index $k$ will be 0.025---essentially the ideal case, so the number of devices needed is the minimum number. If the snubber capacitance is cut to one tenth, then the voltage sharing index $k$ will be 0.25, which then requires a 1.4 times minimum device number. For high voltage applications, the snubber capacitor means cost, size and thermal management. A ten times smaller snubber capacitance has great impact on the system.

## 6.3    ETOs in parallel connection

### 6.3.1    DC current sharing

High-voltage GTOs are more likely to have a resistive I-V characteristic that is good for DC current sharing. The series connected MOSFET, which behaves like a ballast resistor, makes the ETO's I-V even more resistive.

To avoid positive feedback of current crowding, a positive temperature coefficient I-V is very important. Typical high-voltage GTOs have this feature above a critical current value. This critical current point, however, moves toward a lower current direction for the ETO because of the strong positive temperature coefficient of the series connected MOSFETs. A typical ETO's measured forward I-V characteristics are shown in Figure 4-8.

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*6.3.2    Dynamic current sharing during turn-off transient*

The current sharing is a big problem for traditional GTOs operating in parallel connection because of their PNPN latch-up mechanism. However, this mechanism is broken in the ETO turn-off operation. Due to the unity turn-off gain, the cathode injection is terminated quickly and the device functions like an open-base PNP transistor.

Under unity gain turn-off, the storage time is the time needed to remove all the minority carriers in the p-base layer. Since the cathode injection is cut off, minority carriers in the p-base will simply decrease from its initial density before turn-off. The current to remove p-base minority carriers is the device's gate current, which equals to its anode current under the unity turn-off gain condition.

The ETO's storage time is almost a constant value over a wide current range. The minority carrier quantity in the p-base is in proportion to the anode current before turn-off process, and under unity turn-off gain, the minority carrier removing speed is the anode current. Unlike the GTO, the storage time difference of parallel connected ETO will decrease. In the case of two ETOs in parallel, the current will crowd to the slower device with a longer storage time right after the faster ETO finishes its storage phase. However, more anode current means faster minority carrier removing speed, which makes the slower ETO's storage time shorter. This is a negative feedback process that alleviates current crowding problem.

Another feature of the ETOs' parallel operation is that the uniform current distribution among devices can be reestablished after the slowest device finishes its storage phase. The current sharing of two GTO cells has been analyzed in chapter 2. The same theory can be applied on the device level parallel connection as well.

Experimental results support the above theory. Two 1.0 kA/4.5 kV ETOs (ETO1 and ETO2) are used for the experiment. ETO1 has a 70nsec longer storage time than ETO2. The two ETOs are arranged 6-inch away from each other with two bus bars across them. The stray inductance in the two devices' loop is about 100nH.

Figure 6-7(a) shows these two ETOs current sharing characteristics under snubbered turn-off condition. The current transfer between time instant (0.15-0.3μsec) is due to their gate driver difference. Because ETO2's gate driver is inherently 30nsec faster, the anode voltage of ETO2 has a net increase of its turn-off voltage (about 60V) before ETO1 does. This set a voltage difference on the two devices' anode and introduces a small current commutation. However, this current crowding is harmless because this period is short and the voltage on the devices is still low.

The current crowding due to storage time difference happens after time instant t=0.55μ in Figure 6-7(a). The anode voltage on ETO2 increases to overcome the two devices' loop stray inductance. The probing point (center point between the two devices) voltage as shown is thus also increased. After ETO1 enters its turn-off phase, ETO1's anode current decreases rapidly while ETO2's anode current is almost waiting (decreases very slowly). These two devices' anode currents decrease in a similar pattern after the current sharing is restored.
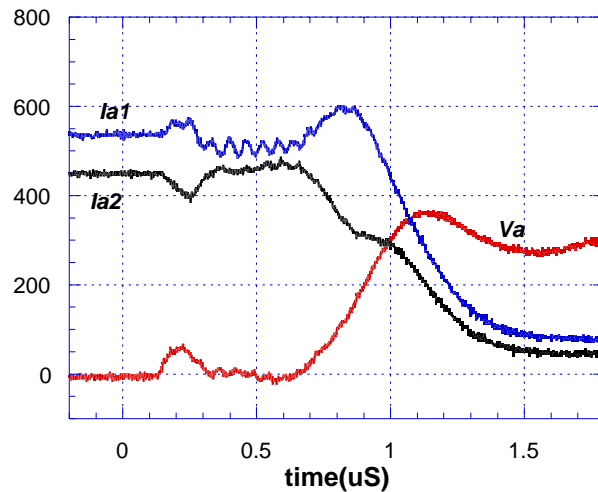


(a) ts1-ts2~70nsec
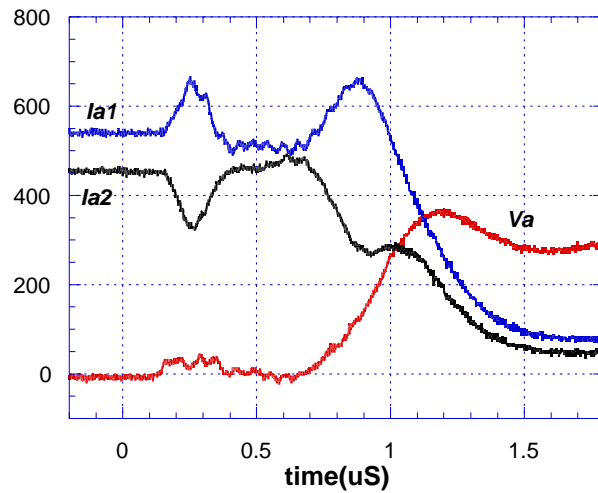
(b) ts1-ts2~130nsec
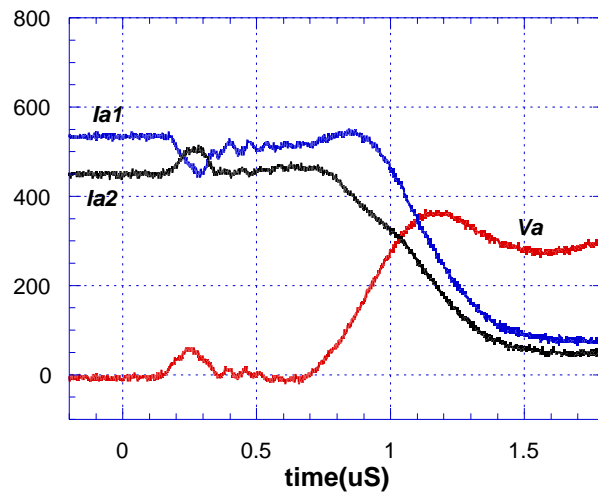


© ts1-ts2~10nsec

Figure 6-7 Current sharing between two ETOs during turn-off. $V_{DC}$=1.0kV, 3μF snubber, 25C.

As is discussed previously, ETO's storage time can be adjusted through the gate resistance of its emitter switch. By inserting a 1-Ω resistor into the gate, ETO1 will have about 60nsec more delay and the current crowding should be exaggerated. Figure 6-7(b) shows the current sharing of this case. Stronger current crowding is observed. However, uniform current distribution is eventually restored. On the contrary, the current crowding will be improved by well matched

parallel devices. Figure 6-7(c) shows the current sharing between the same two ETOs when a 1-Ω resistor is inserted into the gate of ETO2.

Current crowding during turn-off significantly increases the current stress of the slower device. However, the instant power stress is not that worse. For the case of Figure 6-7(b), even the peak current of ETO1 is more than twice as much as the current in ETO2 at that time, their peak instant power, as is shown in Figure 6-8, is only 1.5 times higher. The peak instant power of the slower device ETO1 appears at the point when the uniform current distribution is re-gained. Since ETOs can stand very high instant power ($200 \sim 300 W/cm^2$) [H6], current crowding toward the slower device does not threaten device's safe operation area.
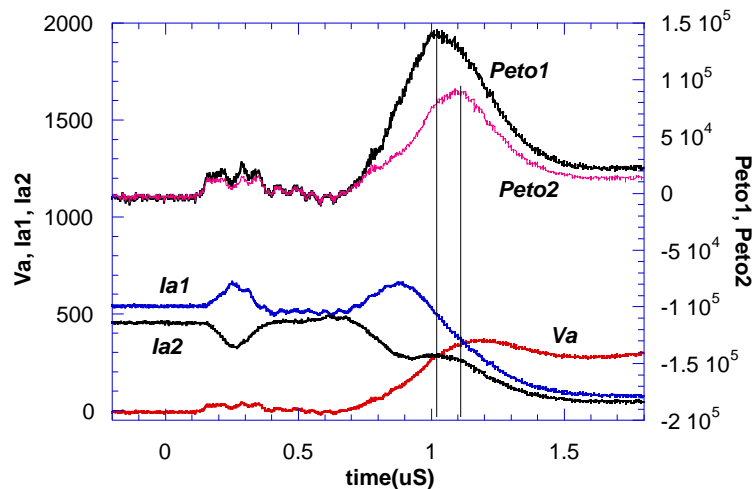


Figure 6-8 Instant power stress on the parallel-connected ETOs during turn-off transient.

Since the device level mechanism can prevent the current crowding and restore uniform current sharing after the storage phase, paralleled ETOs should also be capable of snubberless turn-off. Figure 6-9 shows the current sharing at 2kV snubberless turn-off condition. In the anode voltage rising phase, the anode currents of both the ETO are due to the expansion of their depletion region. Since the devices' initial conditions, which determine minority carrier distributions in the *n-* layer, are identical for the two ETOs, their displacement currents should also equal to each other. This guarantees uniform stress on both of the ETOs at the point of highest instant power point. The tendency of restoring uniform current sharing is also obviously shown in Figure 6-9.

It can also be observed that there is a little current crowding right before the current fall. This is because of the minor difference of the devices' doping and physical parameters. The current non-uniform distribution caused by this is very small but the di/dt of one device is significantly increased. The increased di/dt is a threat to the snubberless turn-off capability of the ETO [H6].
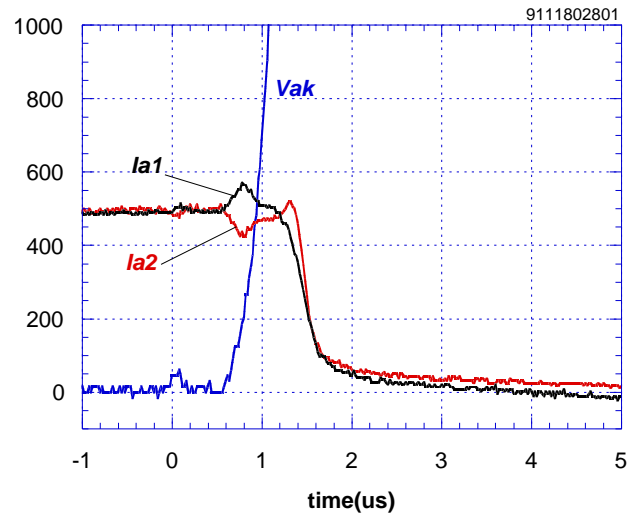


Figure 6-9 Current sharing between two ETOs during snubberless turn-off. $V_{DC}$=2kV, 25C.

## 6.4    Discussion

Most of the above-discussed theory can apply to other kind of hard-driven GTOs such as MTOs, IGCTs, etc. They all have the merit of short storage time distribution as the ETO in series connection. Although their storage times cannot be adjusted simply through a gate resistor, it can be achieved at the gate-driver level or even on the controller level.

Without the series connected MOSFET, the resistive forward I-V characteristics of the MTO and the IGCT is not as good as that of the ETO. However, this can be improved at the device level design trade-off. Both the MTO and the IGCT have the same negative feedback mechanism toward current crowding during the turn-off transient as the ETO because of the same open-base PNP turn-off nature. Compared to the ETO, the IGCT should be better to handle snubberless turn-off in parallel connection because it has no dependency on the anode falling di/dt [H6].

## 6.5    Conclusions

By dramatically decreasing the storage time, ETOs have a very good storage time agreement. Storage time dispersion of less than $\pm100$nsec is normal for ETOs and can be further reduced through adjustment of the emitter switch gate resistance. The capacitance required for dynamic voltage balancing in series connection is significantly reduced. The current sharing for paralleled ETOs is guaranteed at the device level through the open-base PNP turn-off mechanism. The required current balancing inductance can be reduced or eliminated.

# Chapter 7 Resonant Gate Commutated Thyristor (RGCT)

## 7.1    Introduction

Three kinds of advanced GTO improvements have been reported that can operate the GTO in the unity gain turn-off condition. The turn-off principles of IGCT, ETO and MTO are again shown in Figure 7-2 for comparison. The turn-off configuration of the IGCT is similar to a traditional GTO except that it has a very low gate loop stray inductance of 3nH, compared to 300nH typically for a 4-inch GTO. IGCT therefore can achieve a current commutation rate of about 6 kA/µs at a gate drive voltage of 20V. The stray inductance in the ETO gate loop is about 10nH [F1]. However, because they can make use of higher transient voltage (60V as reported [F1]), ETOs can also realize a current commutation rate up to or higher than 6kA/us. The MTO makes use of the threshold turn-on voltage of the GTO gate-cathode diode, which is typically 0.2~0.3V. The gate switch of the MTO is packaged inside the press-pack package and therefore has the lowest gate loop inductance [E9, E10].

For IGCTs, to achieve a low stray inductance, a compact structure that combines a specially designed low stray inductance GTO and its gate driver is necessary. Application systems have to be redesigned to adopt this device structure. The ETO makes use of commercially available GTO and MOSFETs. It is therefore a low cost solution, but has higher component count and higher forward voltage drop due to the series emitter switch [F1]. Compared to the IGCT, the ETO has a more uniform turn-off transient time, most of all, it needs almost no gate energy for turn-off due to the voltage-controlled turn-off process. The MTO also has a voltage controlled turn-off capability and looks just like a traditional GTO with a soft gate lead. The MTO has more components count inside the press-pack. It's main problem is the small margin to increase the current commutation rate due to limited voltage available in the gate loop[E10].
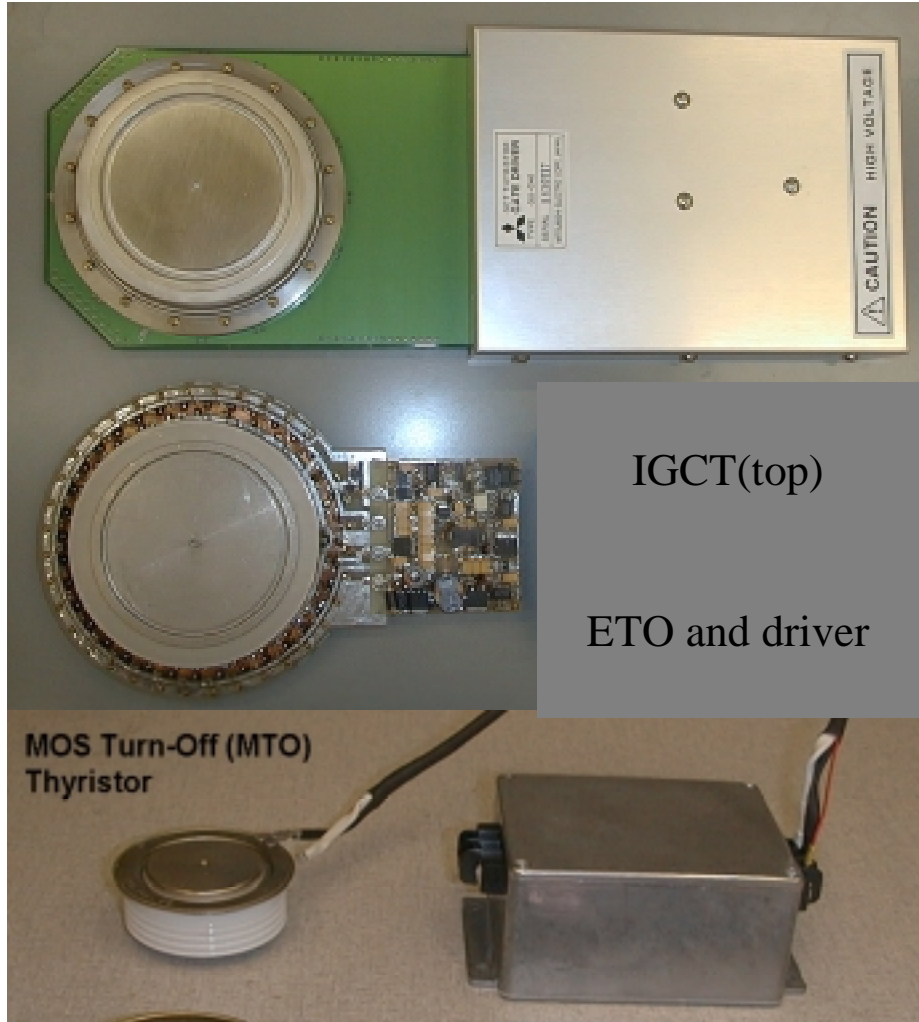
Figure 7-1 IGCT, ETO and MTO along with their gate drivers.



| (a) | (b) | (c) |
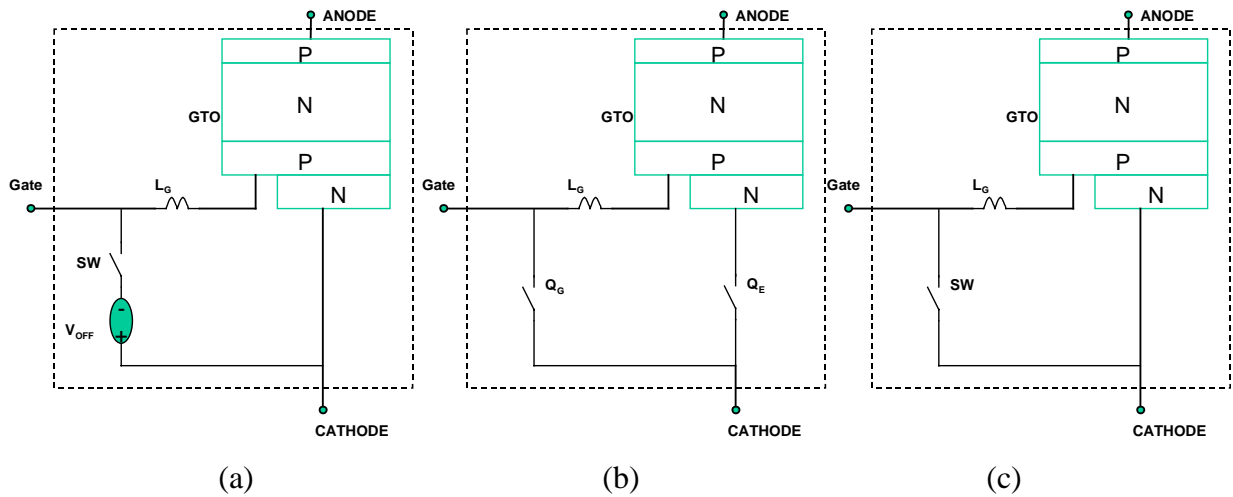
Figure 7-2 Three different types of turn-off configurations.  (a) IGCT; (b) ETO; (c) MTO

The proposed Resonant Gate Commutated Thyristor (RGCT) has the combined advantages of the above mentioned three devices. It makes use of a transient high voltage during the turn-off to speed up the current commutation rate, realizing unity gain turn-off even though the loop stray inductance is relatively high. With this capability, the connection of the RGCT between the gate-driver and the GTO can be a flexible lead. The snubberless turn-off capability is achieved at no extra component count on the main switch. Therefore, conventional GTOs can be used for the RGCT and system design can be significantly simplified because the existing GTO system can be directly upgraded by replacing GTOs with RGCTs.

## 7.2    The principle of resonant current commutation

There are two major requirements for achieving snubberless turn-off capability of a GTO. The first one is the unity turn-off gain, which means that the gate commutation rate has to be high so that all of the cathode current can be commutated to the GTO gate path before the turn-off storage stage. With a high gate loop inductance, as is the case in the proposed RGCT, this can only be achieved with a high commutation voltage. Second, the emitter junction of the GTO (gate-cathode diode) has to be fully reverse biased during the whole turn-off process. RGCTs realize these two requirements by having a high voltage resonant capacitor for current commutation and a low voltage power supply in the gate loop to maintain the reverse bias of the gate-cathode junction.

Figure 7-3 shows the principle of the proposed resonant gate current commutation [J1]. This circuit is similar to that of the IGCT, except the power supply in the IGCT is replaced by a resonant capacitor $C_R$. Typically, the breakdown voltage of the gate-cathode junction of a GTO is about 20~22V. IGCTs and conventional GTOs have to use a voltage source less than this breakdown voltage to prevent constant breakdown of this junction in the off state. This requirement sets up the maximum voltage that can be used for the IGCT.  The only way to achieve high current commutation rate is to reduce the loop stray inductance.
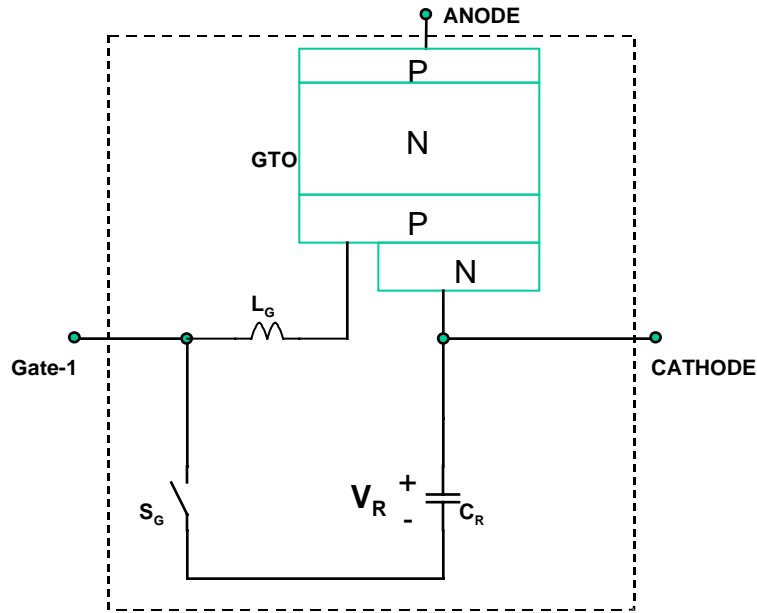
Figure 7-3 Resonant current commutating circuit principle.

By using a resonant capacitor, however, a higher voltage can be used to help the current commutation. The resonant capacitor is fully charged before the initiation of the turn-off transient. When the gate switch $S_G$ is turned on, $C_R$ will resonant with $L_G$, commutating the cathode current to the gate path. The higher the energy in the resonant capacitor, the higher the current that can be commutated. The resonant capacitor is discharged during this resonant process so that after the transition, the voltage left on $C_R$ is less than the breakdown voltage of the GTO's gate-cathode diode.

There are several ways to incorporate the constant reverse bias voltage source with the resonant circuit to make fully functioning RGCTs. Four different versions of RGCTs are analyzed in detail in the following sections.

## 7.3    RGCT-1

### 7.3.1    Operation Principle

Figure 7-4 shows the first version RGCT-1. Connected to the cathode of the GTO is a resonant capacitor $C_R$, which has a high voltage. $S_G$ is a switch. In the normal conduction mode $S_G$ is off, no current flowing through it. When it is on, it drains current from the gate of the GTO and turns off the device. $C_C$ is a lower voltage cap bank, which can maintain a reverse voltage over the

emitter junction of the GTO during the turn-off and off state. $D_C$ is a voltage blocking diode, which prevents discharging from $C_R$ to $C_C$.

The equivalent topology of RGCT-1 looks like a normal ETO without the emitter switch. The GTO's anode and cathode are still the anode and cathode of the RGCT. In the normal conduction mode, it is a normal GTO, with the same forward characteristic.

Before the turn-off, the resonant capacitor $C_R$ has been charged to a high voltage value $V_{CR}$. When the turn-off gate switch $S_G$ is turned on, $C_R$ will resonant with the gate loop stray inductor $L_G$ and the current originally in the GTO emitter junction will be fully commutated to its gate path. The time required to commutate the current is determined by the time constant of $C_R$ and $L_G$. The initial voltage on the $C_R$ determines the maximum current that can be commutated.
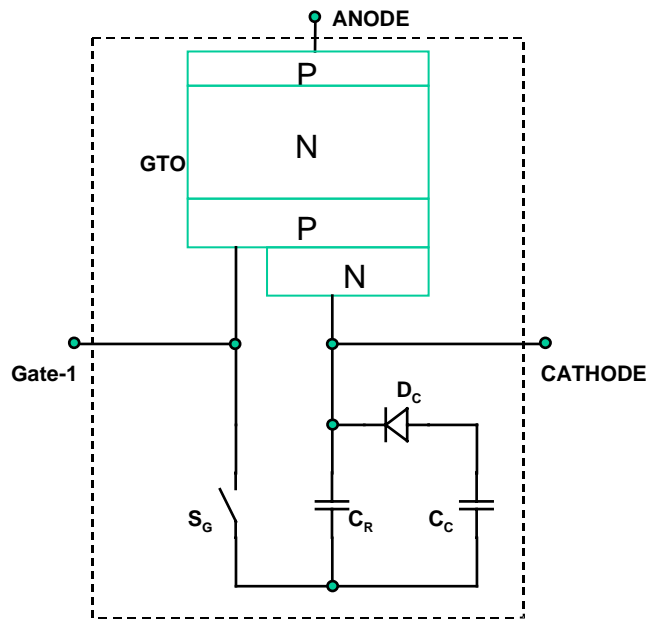


Figure 7-4 RGCT-1 topology.
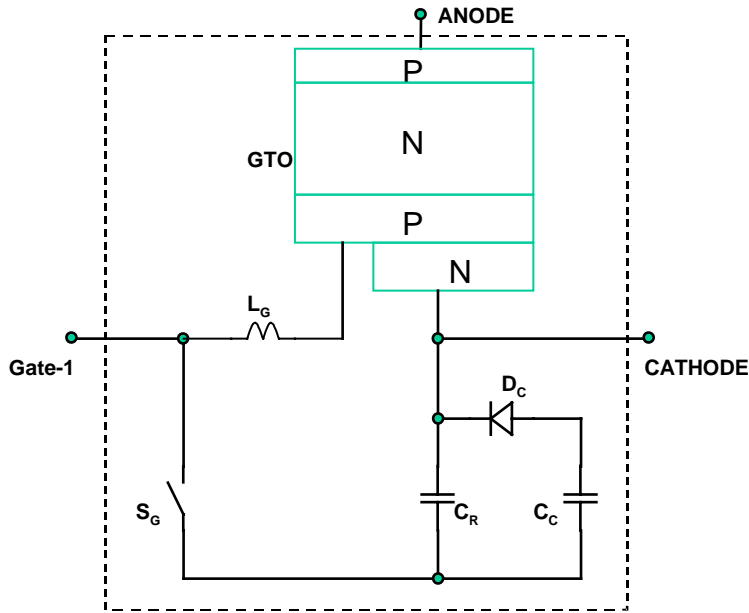
Figure 7-5 RGCT-1 equivalent circuit with the gate stray inductor.

Based on the above analysis, a PSpice equivalent circuit that can be used for simulating the RGCT unity-gain turn-off and undesirable current injection is shown in Figure 7-6. Key parameters are also listed. The $C_C$ can be understood as a voltage source.
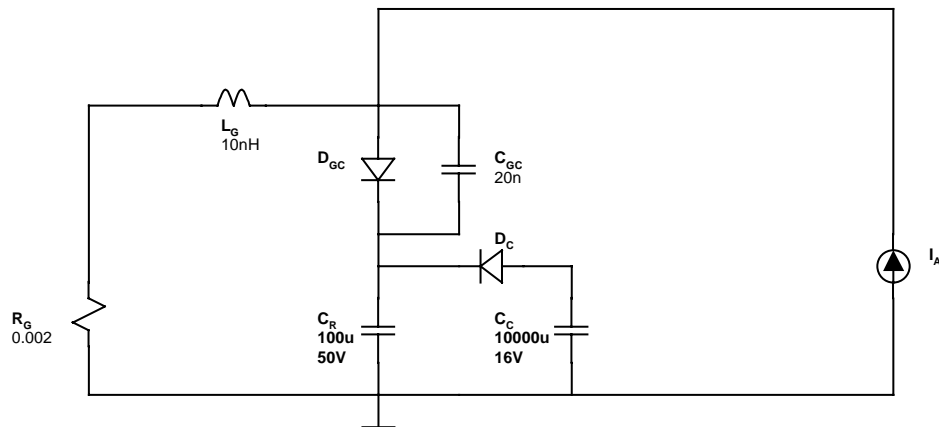


Figure 7-6 PSPICE simulation equivalent circuit for the unity turn-off gain and current injection study.

Figure 7-7 shows simulation results for the RGCT-1. At time instant 0, turn-off process begins. In about 0.3μsec, the current on the stray inductor $L_G$ reaches anode current and the GTO gate-cathode junction current becomes zero. This is the unity gain point. After that and before the

falling edge of the anode current, the current on the GTO gate-cathode junction maintains negative and the voltage over this junction is negative too. This means that the emitter junction is not active, and the whole GTO should act as an open base PNP transistor.
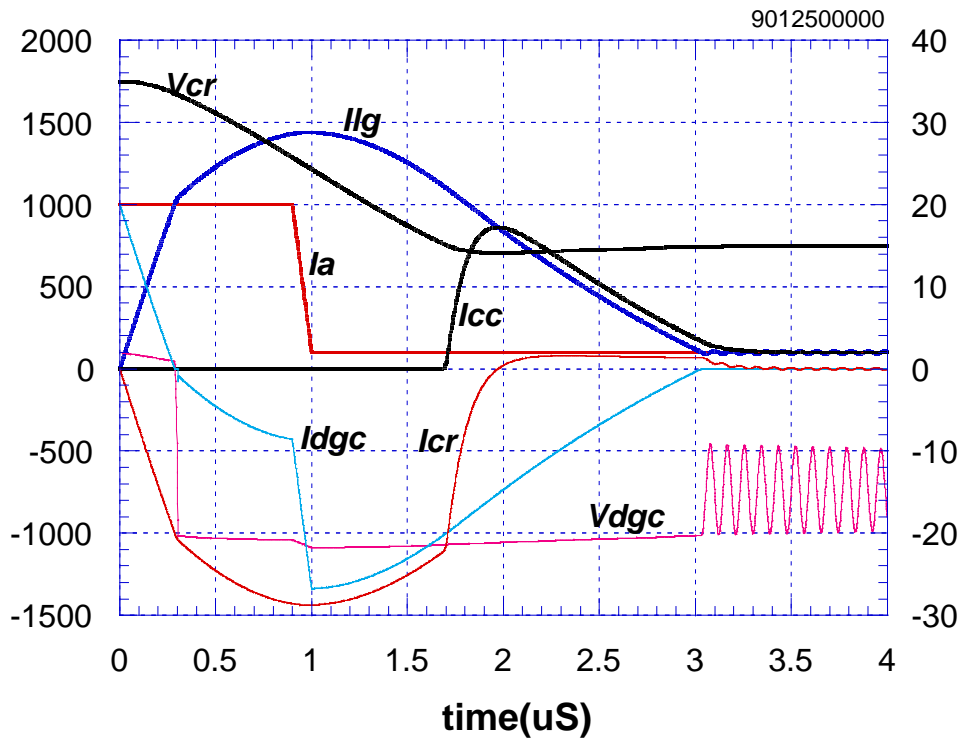


Figure 7-7 Simulated results for the RGCT-1 based on the equivalent shown in Figure 7-6.

When the voltage on the resonant capacitor $C_R$ comes below the voltage on the clamp cap bank $C_C$, $C_C$ will take over by supplying current for the current tail and charging back the voltage on the $C_R$. Because of the big $C_R$, most of the current coming from the cap bank $C_C$ goes to $C_R$.

**I$_{DGC}$**, the reverse breakdown current of the GTO gate-cathode junction finally goes to zero. This junction keeps reverse biased after all. The voltage oscillation of $V_{DGC}$ is between the stray inductor $L_G$ and the emitter junction capacitor $C_{GC}$. All the way after the turn-off, there is no current injection into the GTO emitter junction.

### 7.3.2    *Effect of stray inductance in the voltage clamp path*

In the above analysis, no stray parameters in the clamp cap bank path were taken into consideration. Without stray inductor in series with it, the $C_C$ can react very fast and take over the current in the $L_G$ instantly while the voltage on the resonant capacitor drops down. The di/dt in the $C_C$ path is as high as 10kA/μsec in the simulation as can be observed from Figure 7-7.

If there is stray inductance, the current in the $C_C$ path can not build up so fast. This can lead to some problem. The voltage over the resonant cap $C_R$ may decrease to a very low value or even to negative, generating current injection into the GTO emitter junction. Assuming a stray inductance of 30nH, the simulation results are shown in Figure 7-9. From Figure 7-10---its zoom-in diagram, the junction can be observed forward biased and the unwanted current injection occurs. This is the killer during snubberless turn-off.
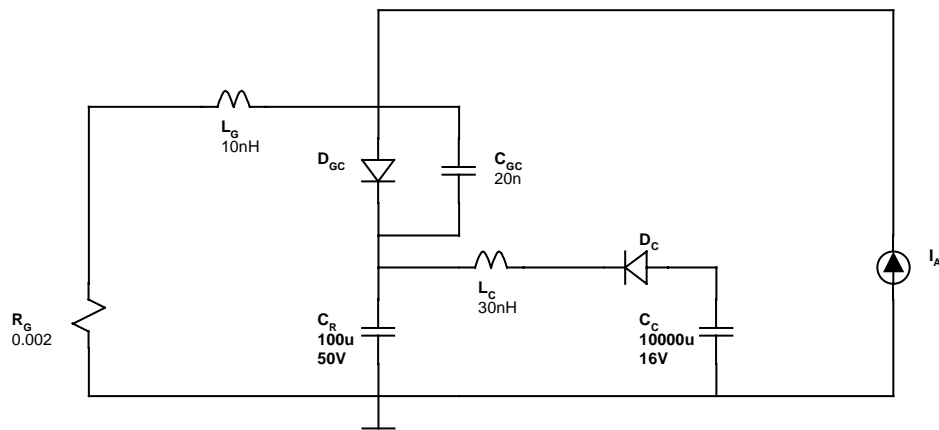


Figure 7-8 PSPICE simulation equivalent circuit for the unity turn-off gain and current injection considering the stray inductance in the voltage clamping path.
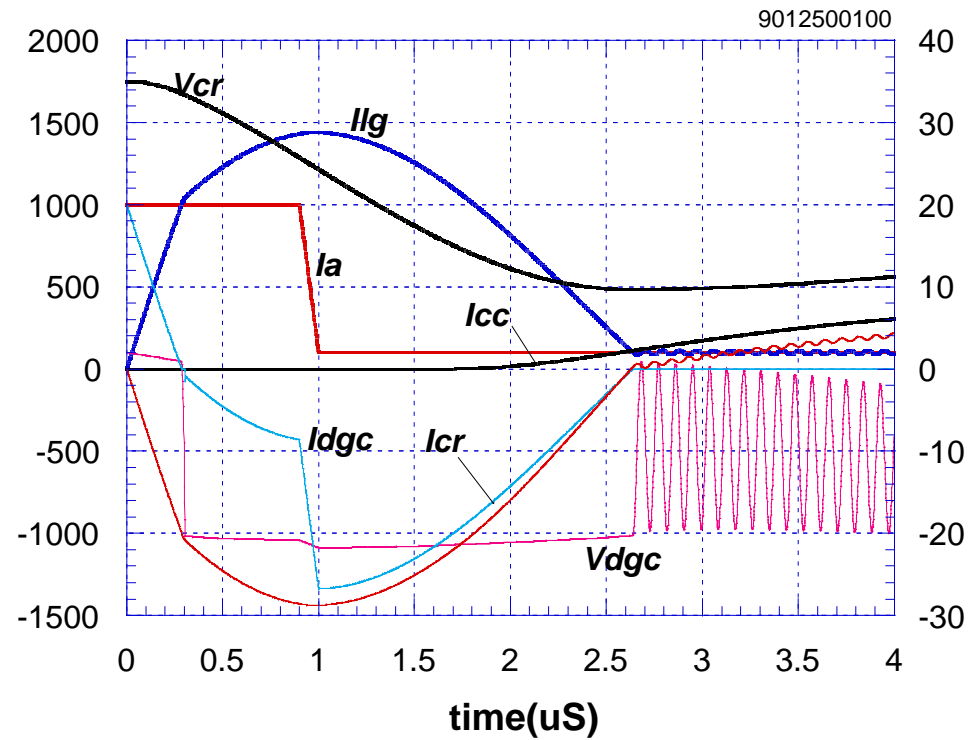
Figure 7-9 PSPICE simulation results for the RGCT-1 when the stray inductance in the voltage clamping path considered.

In practical situation, the clamp cap bank **C$_C$** in series with the diode **D$_C$** will have a significant stray inductance, which introduces the forward current injection problem to the GTO gate-cathode junction.

The voltage across the GTO gate-cathode junction oscillates when its reverse breakdown current reaches zero. This oscillation is between the GTO emitter junction parasitic capacitor C$_{GC}$ and the GTO gate stray inductor L$_G$ as shown in Figure 7-11. Because the resonant capacitor C$_R$ is in the loop, the oscillation voltage is around the voltage on C$_R$.

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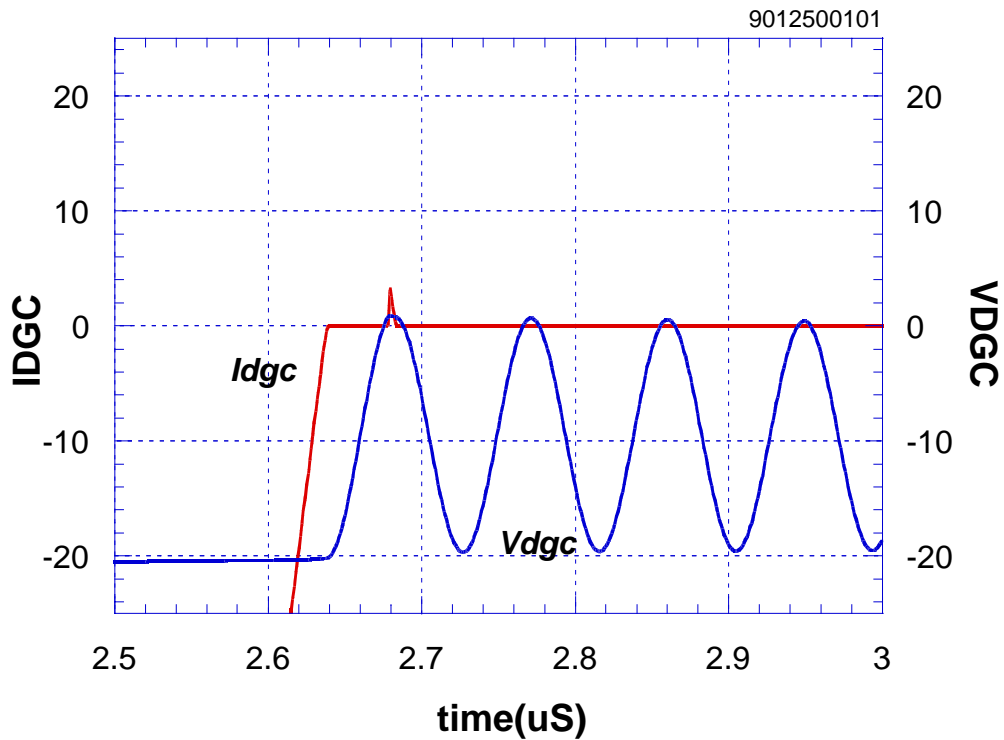


Figure 7-10 A zoom-in view of the voltage and the current on the GTO gate-cathode junction for

Figure 7-9. The junction comes to forward bias and the current injection occurs.
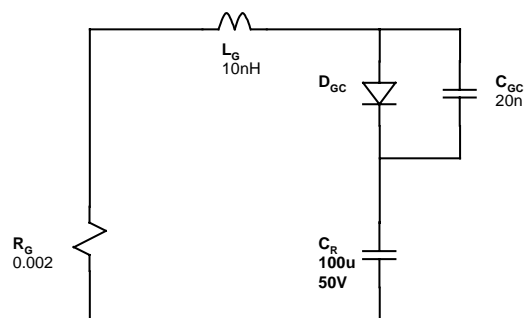


Figure 7-11 Parasitic oscillation equivalent circuit loop once the reverse breakdown of $D_{GC}$

finished. The CC acts as a voltage source.

Since $(C_R L_G)$ constant is much bigger than the $(L_G C_{GC})$ time constant, the voltage on $C_R$ can be taken as a DC value. To make sure the junction never goes to forward bias, the instant voltage on the $C_R$ should be greater than half of the breakdown voltage of the GTO emitter junction. In the

idea case shown in Figure 7-7, the voltage on $C_R$ is 14V, the lowest reverse biased voltage on the GTO emitter junction is 9V. However, in the case with stray inductance in the voltage clamp path, the voltage on the $C_R$ decreases to 9.8V, the junction becomes forward biased.

In both cases, the voltage of the clamp capacitor $C_C$ was 16V. Without stray inductance, the voltage on the $C_R$ is automatically clamped by the voltage clamp. Current in it can be built instantly once needed so the minimum voltage on the $C_R$ is equal to the voltage on $C_C$ minus one diode forward voltage drop. If stray inductance presents, situation changes. In a special case when the stray inductance is unlimited large, no current injection is availablefrom the voltage clamp path and the voltage on $C_R$ can drop below zero when the reverse current in the GTO emitter junction reaches zero. The consequence is that all the tail current will be commutated back to the GTO emitter junction and the negatively charged $C_R$ will also generate more current injection into it.

To have a higher voltage on the $C_R$ when the reverse current through the GTO emitter reaches zero, it is better to have the voltage on the clamp cap bank as high as possible. However, it can not be higher than the reverse breakdown voltage of the GTO emitter (normally 20V).

To maintain the voltage or slow down the decreasing rate of the voltage on $C_R$, the voltage clamp $C_C$ path has to be able to deliver high di/dt.

### 7.3.3    Selection of the resonant capacitor $C_R$

The $C_R$ value and the voltage on $C_R$ combined with the GTO gate stray inductance $L_G$ determine the unity turn-off gain as well as the maximum current that can be commutated.

Theoretically, in half the oscillation cycle determined by $L_G$ and $C_R$, all the energy can be commutated from $C_R$ to $L_G$ and the commutation current can reach its maximum. Typically, the storage time of the device is about 1-2μsec. To make sure the commutation current reaches its peak before the current fall stage, a $L_G$ $C_R$ cycle of 2μsec can be selected. In the case of 10μH $L_G$, a 10μF $C_R$ is reasonable.

PSPICE simulation was conducted based on the above analysis. Figure 7-12 shows the simulation results when a 10μF resonant capacitor is used. The advantage is that the resonant current overshoot is small. However, the circuit cannot maintain the unity turn-off gain firmly. After quarter cycle of the ($C_R$, $L_G$) oscillation, the resonant capacitor cannot maintain the anode current and the voltage clamp is required to supply all the current almost instantly, which is difficult in the present of the stray inductance. In Figure 7-12, serious current injection can be observed before the main current fall.

The better way to maintain the unity turn-off gain is to use a bigger resonant capacitor so that the resonant commutation current reaches its peak around the time when the main current begins to fall. Typically the current storage time is 1-2μsec. At the condition of 10μH $L_G$, a 100μF resonant capacitor is reasonable.
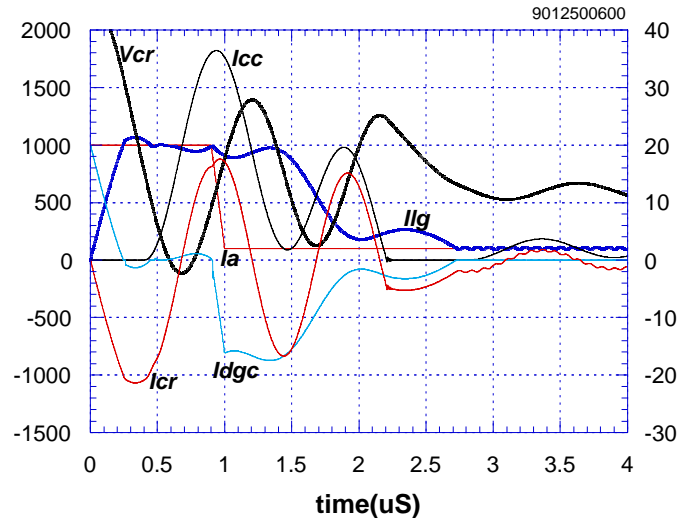


Figure 7-12 PSPICE simulation results for 10μF resonant capacitor. The voltage on the CR is 45V, the stray inductance in the clamp path is 3nH.

### 7.3.4   *Conclusion about the RGCT-1*

Based on the above discussion, following conclusions can be derived for the RGCT-1:

1. By utilizing a resonant capacitor $C_R$, the unity turn-off gain can be achieved with any kind of GTO gate stray inductance $L_G$.

2. The voltage clamp can keep the GTO gate-cathode junction reverse biased during the current tail period.

3. The voltage on the resonant capacitor $C_R$ has to be kept higher than half of the GTO emitter junction breakdown voltage to make sure no forward bias voltage be applied on the GTO emitter junction.

4. Only two components involved in the high current loop, they are GTO's gate switch $S_G$ and the resonant capacitor $C_R$. The total stray inductance in this loop can be minimized.

5. The voltage clamp path should have high current capability to charge the voltage on $C_R$ back. The loop stray inductance $L_C$ should be as low as possible.

## 7.4    RGCT-2

The RGCT-1 has two problems. Firstly, the current capability of the voltage clamp required is high. Secondly there is difficulty to achieve low stray inductance in the voltage clamp loop because there are two components ($D_C$ $C_C$) in series so the loop is hard to be minimized.

The RGCT-2 is trying to solve the second problem. Figure 7-13 shows the principle topology for the RGCT-2. The resonant capacitor $\mathbf{C_R}$ is now in series with the voltage clamp cap bank $\mathbf{C_C}$, while the voltage clamp diode is in parallel with the resonant capacitor $\mathbf{C_R}$.

Compared to the RGCT-1, one more component $C_C$ involves into the main current resonant loop. This is a drawback because it introduces extra gate loop stray inductance. However, the stray inductance in the voltage clamp path can be reduced. Only two component $D_C$ and $C_R$ accounts for the stray inductance $L_C$.

Figure 7-16 shows the PSPICE simulation results without considering the stray inductance in the voltage clamp path. The results are just like the idea case for the RGCT-1.
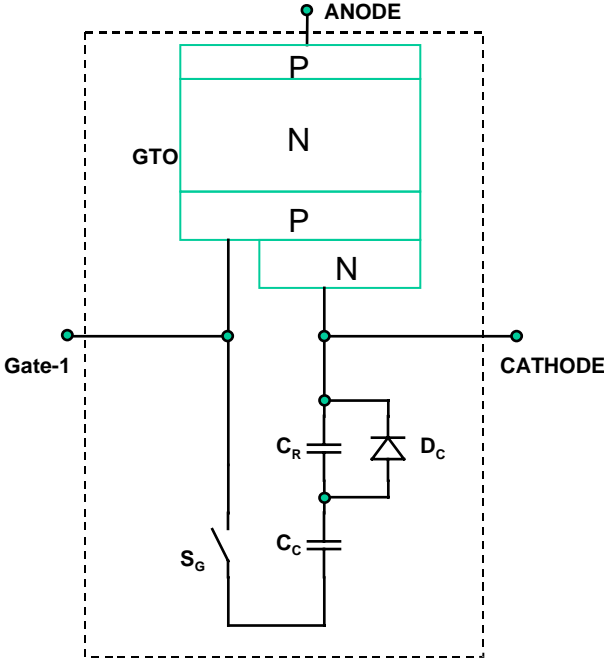
Figure 7-13 RGCT-2 principle topology.
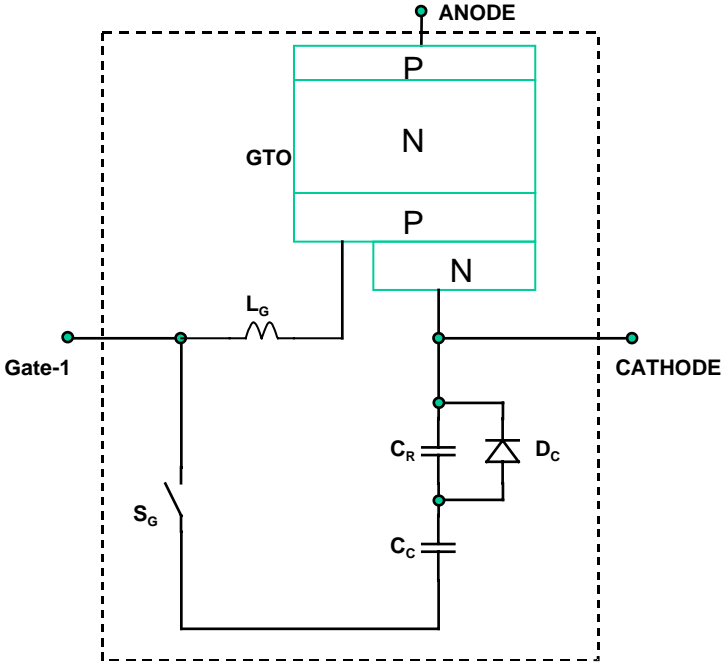


Figure 7-14 RGCT-2 equivalent circuit when the GTO gate loop stray inductor $L_G$ is considered.
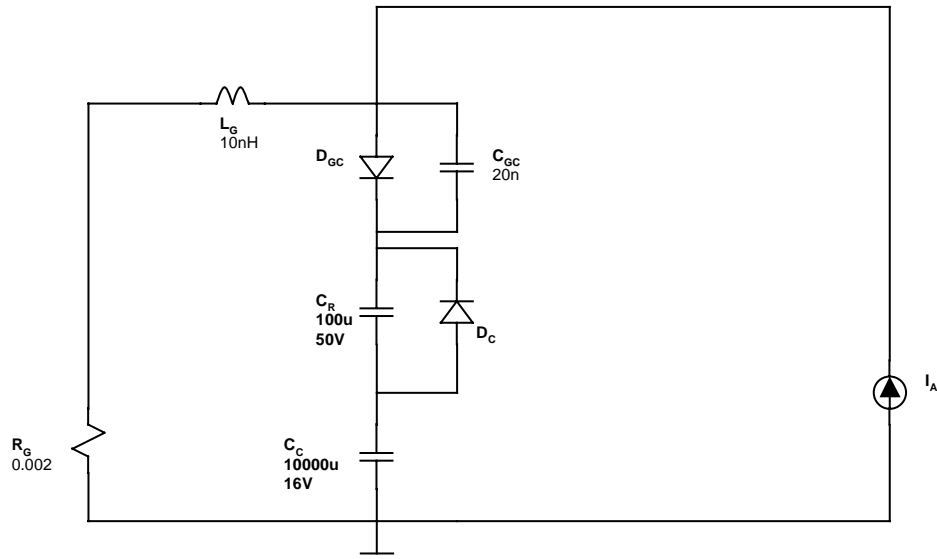
Figure 7-15 PSPICE simulation equivalent circuit for the unity turn-off gain and current injection study.
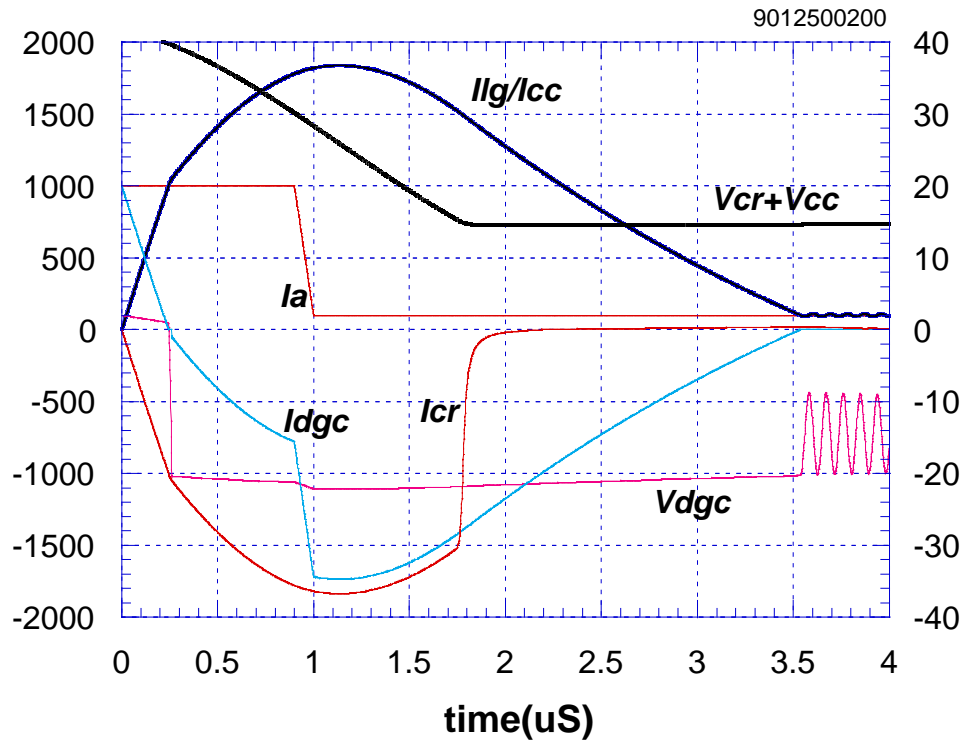


Figure 7-16 Simulated results for the RGCT-1 based on the equivalent shown in Figure 7-15.
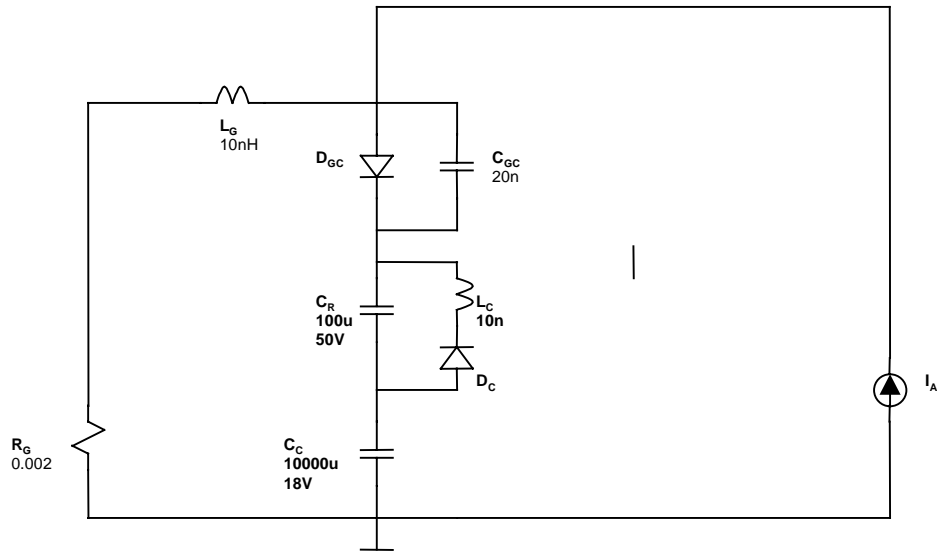
Figure 7-17 PSPICE simulation equivalent circuit for the unity turn-off gain and current injection study when the stray inductance $L_C$ in the voltage-clamping path is considered.
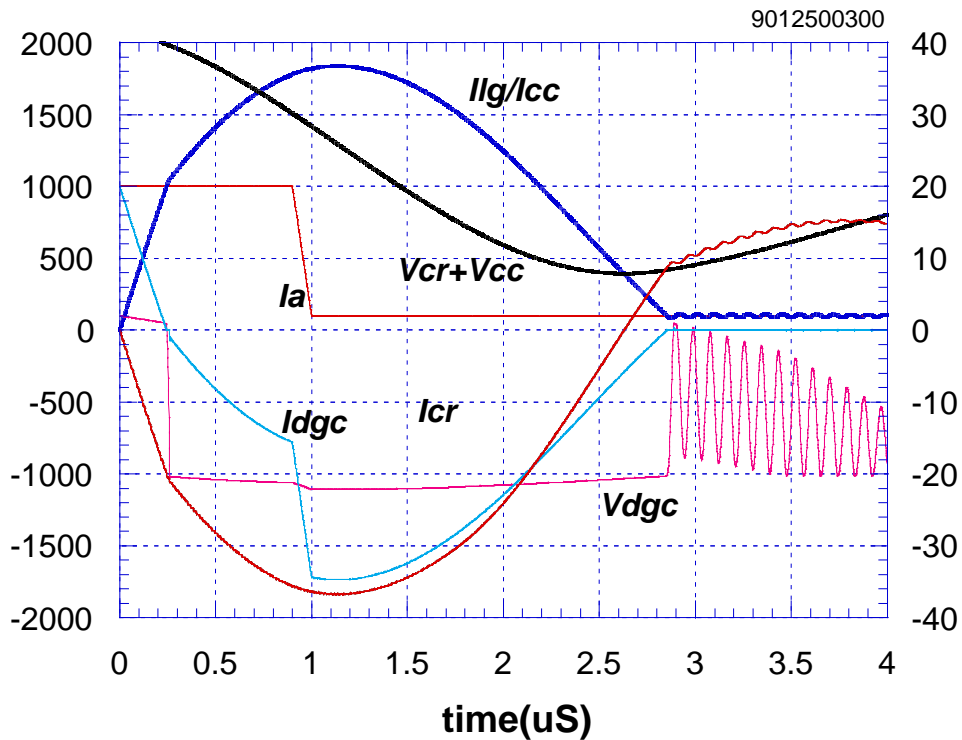


Figure 7-18 PSPICE simulation results for the RGCT-1 when the stray inductance in the voltage clamp path considered.

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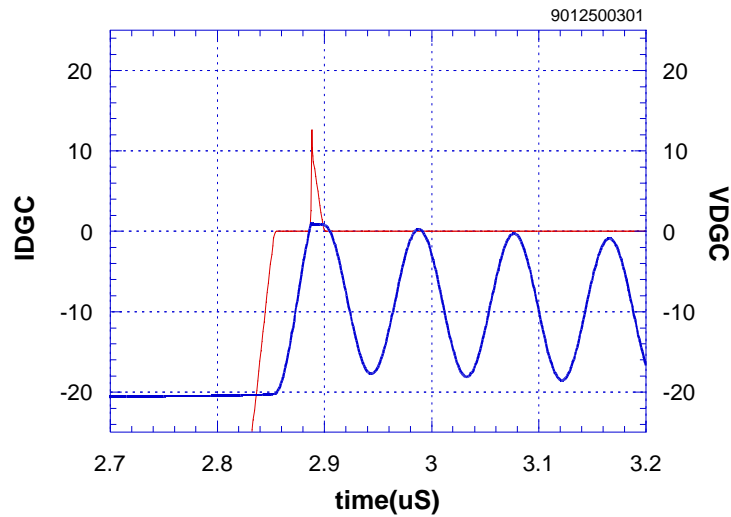
Figure 7-19 A zoom-in view of the voltage and the current on the GTO gate-cathode junction for Figure 7-18. The junction becomes forward biased and the current injection occurs.

### 7.4.1    *Effect of the stray inductance in the voltage clamp path*

Figure 7-18 shows the PSPICE simulation results for the RGCT-2 when the stray inductance $L_C$ in the voltage clamp path is considered. Even with a higher clamp voltage (18V) and a lower clamp stray inductance $L_C$ (10nH), the voltage over $C_R$ and $C_C$ drops below half of the GTO emitter junction breakdown voltage and some current injection appears during the current tail stage.

Compared with RGCT-1 case, it can be observed that the voltage over $C_R$ and $C_C$ in the RGCT-2 decreases faster considering the same clamp loop stray inductance $L_C$. This can be interpreted as following. When the voltage on the resonant capacitor drops to the level of the clamp voltage $V_C$ for RGCT-1, the voltage clamp begins to take over the resonant current. Due to the existence of $L_C$, the voltage clamp cannot take over the current instantly so the resonant capacitor $C_R$ needs to continue supplying part of the commutation current until $L_C$ is charged up. The maximum energy $C_R$ released, which is $0.5C_R(V_C{}^2\text{-}(V_C\text{-}V_{CRLOW1})^2)$, is about the energy $L_C$ required to be charged up to the commutation level. ($V_{CRLOW1}$ is the lowest voltage on $C_R$ for RGCT-1). Similar analysis applies to RGCT-2 except that the voltage clamp path begins to take over the commutation current when the resonant capacitor is discharged to zero. Thus the energy $C_R$ should release is

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$0.5C_RV_{CRLOW2}^{2}$. ($V_{CRLOW2}$ is the lowest voltage on $C_R$ for RGCT-2). To release the same energy, $V_{CRLOW1}$ is smaller than $V_{CRLOW2}$. So the minimum turn-off voltage ($V_{CRLOW1}$) in RGCT-1 is higher than the minimum turn-off voltage ($V_C$- $V_{CRLOW2}$) when $V_{CRLOW1}$ is approaching $V_C/2$.

### 7.4.2    *Conclusion about the RGCT-2*

Based on the above discussion, following conclusions can be obtained for the RGCT-2:

1. By utilizing a resonant capacitor $C_R$, the unity turn-off gain can be achieved with any kind of GTO gate stray inductance $L_G$.

2. The voltage clamp can keep the GTO gate-cathode junction reverse biased during the current tail period.

3. The voltage on the resonant capacitor $C_R$ has to be kept higher than half of the GTO emitter junction breakdown voltage to make sure no forward bias voltage be applied on the GTO emitter junction.

4. Three components are involved in the high current loop, they are GTO gate switch $S_G$, resonant capacitor $C_R$ and the voltage clamp capacitor $C_C$. The total stray inductance in the main current commutation loop is higher than that in the RGCT-1.

5. The voltage clamp path should have the same high current capability as the resonant capacitor $C_R$. The loop stray inductance $L_C$ can be reduced in this case.

6. The voltage on $C_R$ and $C_C$ is hard to remain high compared to the RGCT-1.

## 7.5    RGCT-3

For both the RGCT-1and the RGCT-2, the voltage on the resonant capacitor $C_R$ during the current tail period is crucial. To make sure no forward current injection into the GTO gate-cathode junction, voltage on the $C_R$ should be maintained higher than a value (typically half of the breakdown voltage of the GTO emitter). On the other hand, the clamp voltage could not be higher than the GTO emitter breakdown. These two factors combined together give a stringent requirement to the design.

The purpose of the clamp path is to maintain the reverse voltage on the GTO cathode. However, because of the big resonant capacitor $C_R$ and the limited current capability of the voltage clamp path, the voltage at the GTO cathode point is hard to be charged back once it is discharged.

To solve this problem, the RGCT-3 is proposed. Compared to the RGCT-1, a diode $D_R$ is added as shown in Figure 7-20. With this diode, the resonant capacitor $C_R$ can be understood as a big capacitance in one direction, but a very small capacitance (reverse junction capacitance of $D_R$) in the other direction.

There are two merits for this topology. One is that the voltage clamp path does not have to be that powerful as in the RGCT-1. Once the voltage on the $C_R$ decreases, $C_C$ supplies the device tail current. No current required from $C_C$ to charge the $C_R$ as in the RGCT-1.

In the RGCT-1, the voltage at the GTO cathode point should be maintained higher than a value to prevent forward bias by the discharge of the GTO emitter junction capacitance $C_{DGC}$. The case in the RGCT-3 has been changed. Because there is only a small capacitance (generally less than $C_{DGC}$) of the diode $D_R$ is in series with $C_{DGC}$, the GTO emitter junction will remain reverse biased all the time regardless of the discharging of $C_{DGC}$.

Considering the reverse recovery of $D_R$, $C_C$ should have the capability to recover $D_R$ before the reverse breakdown current of the GTO emitter junction comes to zero.
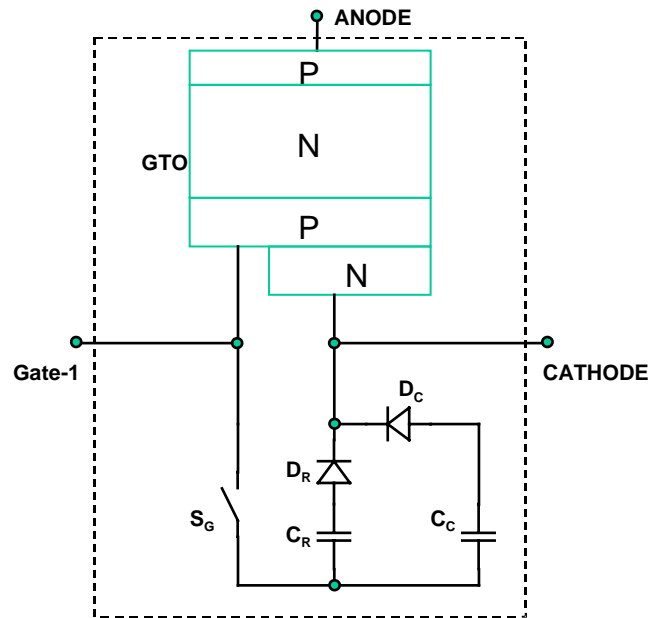


Figure 7-20 RGCT-3 concept topology.
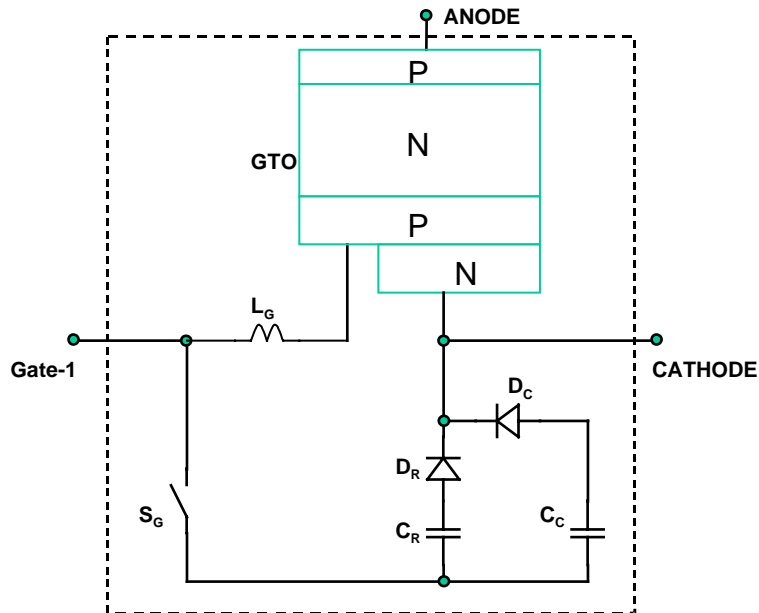
Figure 7-21 RGCT-3 principle topology when the stray inductance in the GTO gate considered.

*7.5.1    RGCT-3 performance without considering the stray inductance in the voltage clamp path*

Figure 7-22 is the RGCT-3 PSPICE simulation equivalent circuit without considering the stray inductance in the voltage clamp path. The only difference compared to RGCT-1 is that a diode $D_R$ is in series with $C_R$.

Figure 7-24 shows the simulation results for this case. Due to the existence of the reverse blocking diode $D_R$, the voltage on the $C_R$ does not need to be charged back during the current commutation period, and the voltage oscillation amplitude is lower than that for the RGCT-1.
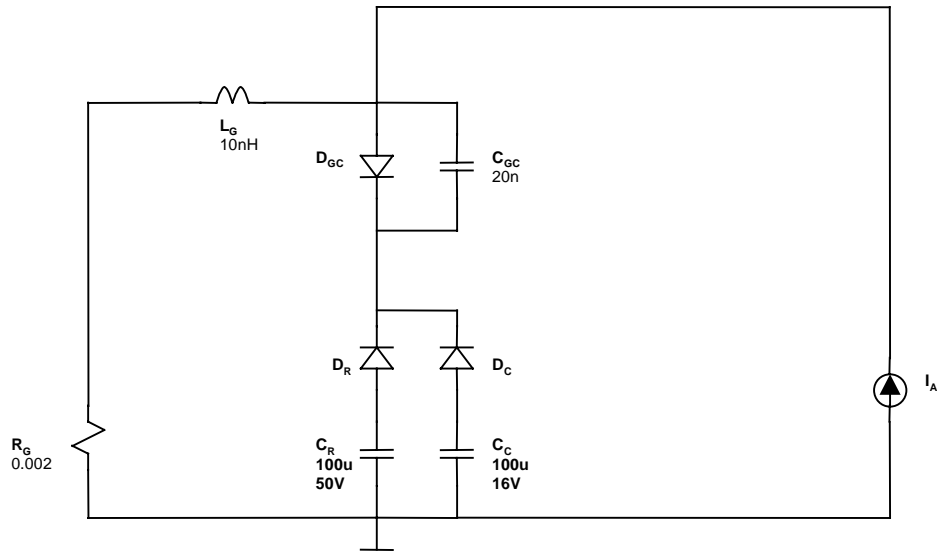
Figure 7-23 RGCT-3 PSPICE simulation equivalent circuit without considering the stray inductance in the voltage clamp path.
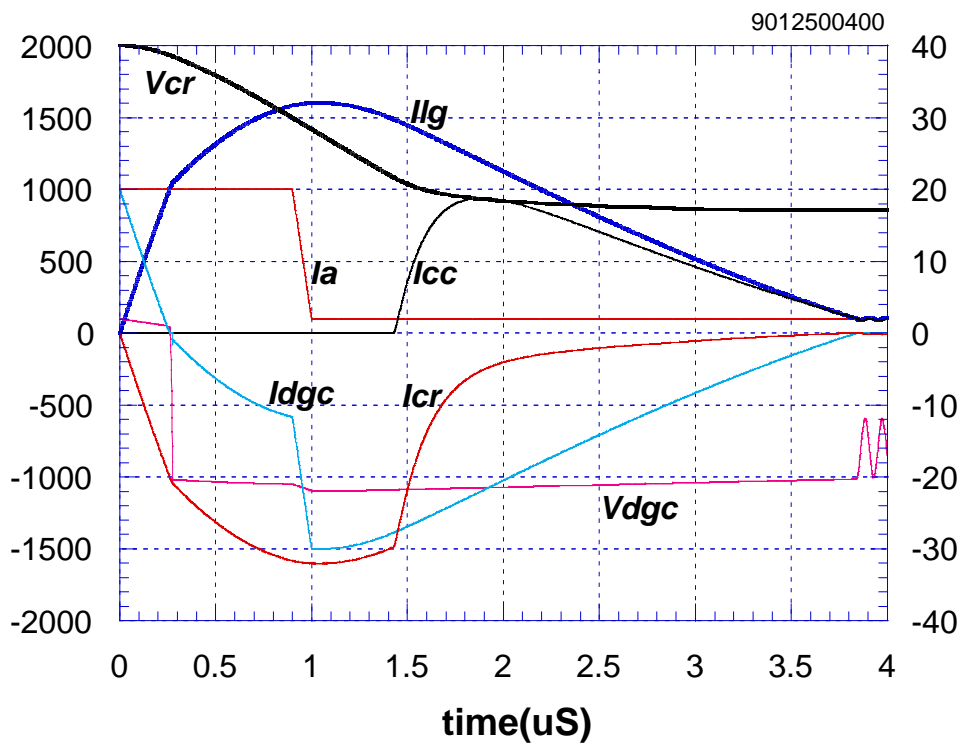


Figure 7-24 RGCT-3 PSPICE simulation results.

*7.5.2    RGCT-3 performance considering the stray inductance in the voltage clamp path*

Figure 7-25 is the RGCT-3 PSPICE simulation equivalent circuit considering a 30nH stray inductance $L_C$ and a 16V voltage in the clamp path. Figure 7-26 shows the simulation results.

With the stray inductance $L_C$, the dynamic response of the current in the voltage clamp path is significantly decreased. The di/dt from the simulation is about 500A/μsec. However, there is no unwanted current injection into the GTO emitter junction.

The minimum current from the voltage clamp path in this case can be estimated as following:
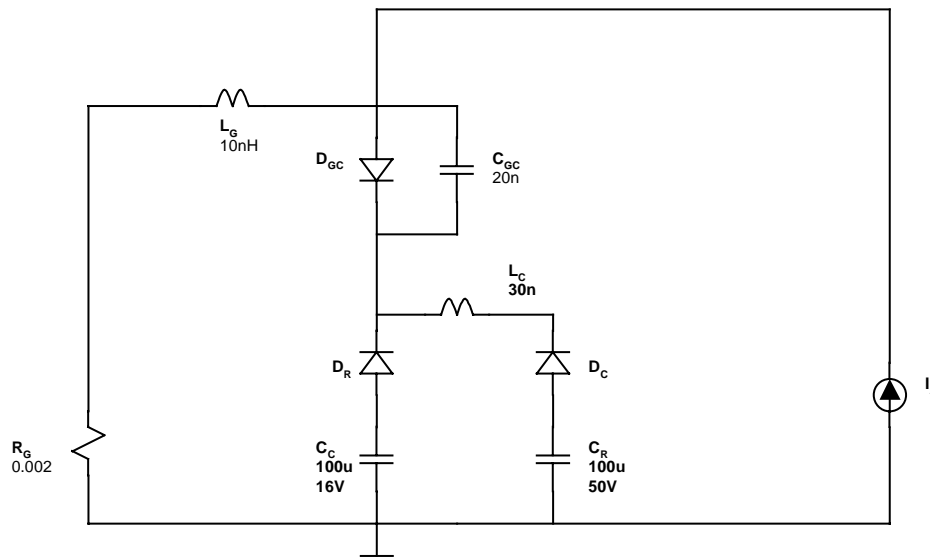


Figure 7-25 RGCT-3 PSPICE simulation equivalent circuit when the stray inductance in the voltage clamp path considered.

Assuming the reverse recovery time of $D_R$ is 100nsec. The time when the current in $D_R$ reaches zero, the reverse conducting current in the GTO emitter junction should be a certain value higher than the anode current tail so that the reverse current in $D_{GC}$ takes more time than the reverse recovery of $D_R$. The current decreasing rate in $D_{GC}$ at final stage is $(22-9)/L_G=1300$A/μsec. So the current in $D_{GC}$ at the time when the current in $D_R$ reaches zero should be at least 230A. From this time forward, all the current should come from the voltage clamp, so this is also the minimum current requirement for the voltage clamp path.
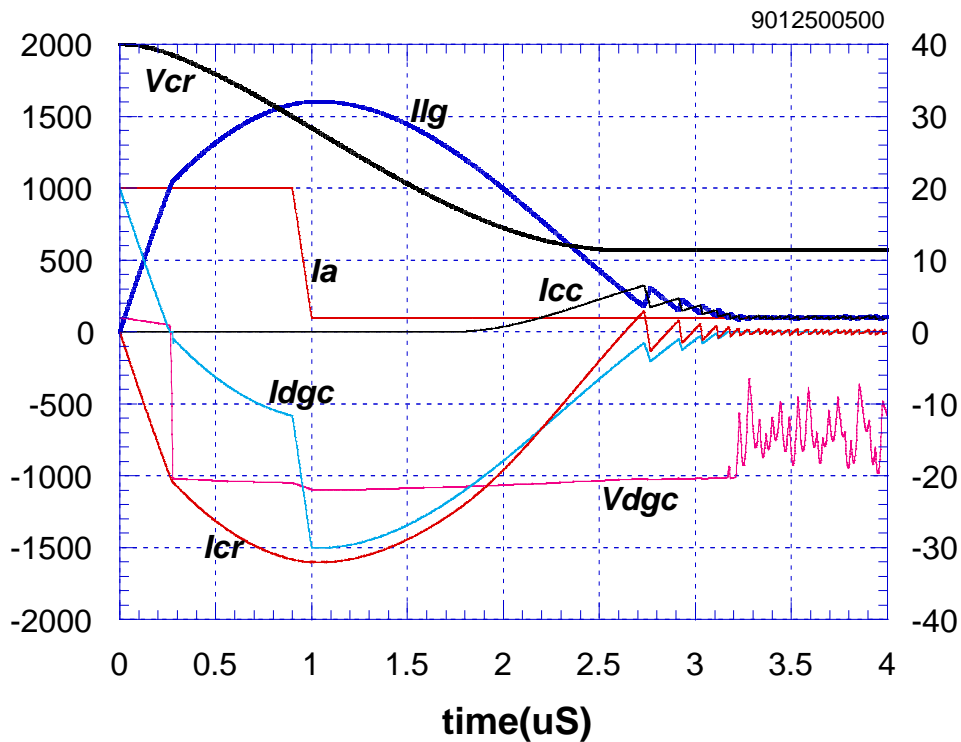
Figure 7-26 RGCT-3 PSPICE simulation results when a 30nH stray inductance in the voltage clamp path is counted.

### 7.5.3    Conclusion about RGCT-3

Based on the above discussion, following conclusions can be summarized for the RGCT-3:

1. By utilizing a resonant capacitor $C_R$, the unity turn-off gain can be achieved with any kind of GTO gate stray inductance $L_G$.

2. The voltage clamp can keep the GTO gate-cathode junction reverse biased during the current tail period.

3. The voltage on the resonant capacitor $C_R$ does not have to be kept higher than half of the GTO emitter junction breakdown voltage to make sure no forward bias voltage be applied on the GTO emitter junction.

4. Three components are involved in the high current loop, they are GTO gate switch $S_G$, resonant capacitor $C_R$ and diode $D_R$.

5. The total stray inductance in the main current commutation loop is higher than that in the RGCT-1 due to $D_R$.

6. The voltage clamp path does not require the same high current capability as the resonant capacitor $C_R$. The loop stray inductance $L_C$ can be higher while zero current injection into the GTO emitter junction is assured.

## 7.6    RGCT-4

For the above mentioned three version RGCTs, the resonant capacitor $C_R$ is discharged when the GTO is OFF.  It can only be charged when the gate switch $S_G$ is off. The higher the charging current, the faster the charging process.

The time when $S_G$ is off, the GTO should be in the on state and requires turn-on injection current. To speed up the turn-on process, high initial injection current is required.

Combining them together, it is clear that in the same time period, both the GTO emitter junction and the resonant capacitor $C_R$ need current injection and both of them need high injection current. If they can be put in a series connection, one current injection will do both jobs.

Figure 7-27 shows the proposed RGCT-4 topology. The circuit topology is similar to that for the RGCT-3 except that the resonant path and the voltage clamp path are moved from the GTO cathode side to its gate side.

With this topology, the resonant capacitor $C_R$ is in series with the GTO gate-cathode junction. The time the GTO is going to be turned on, $S_G$ will be turned off and the charger switch will be turned on. A pulse charging current will go through the resonant capacitor $C_R$ and the GTO emitter junction.

### 7.6.1    Conclusion about the RGCT-4

Besides all the merits that the RGCT-3 has, the RGCT-4 has one more merit. That is the RGCT-4 derives its turn-on pulse current from the charging the resonant capacitor $C_R$.
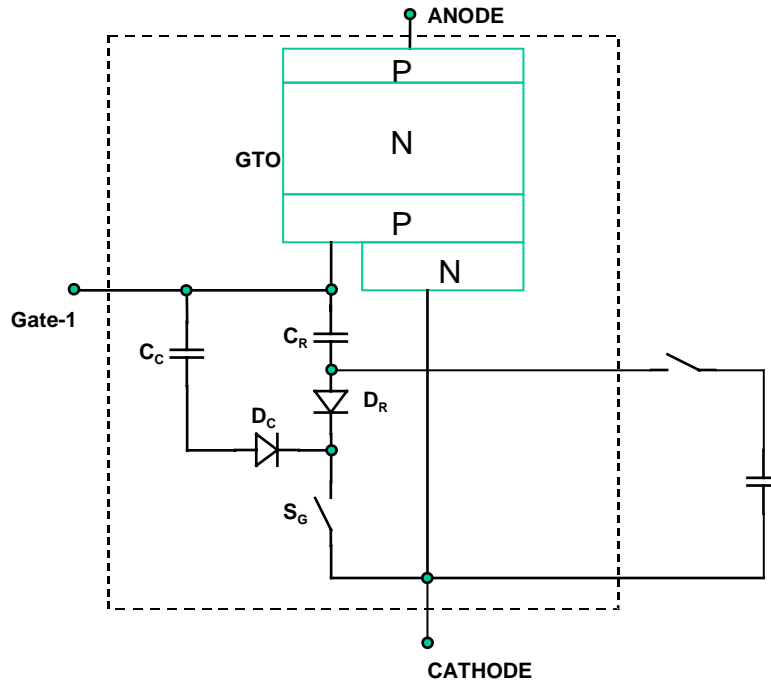
Figure 7-27 RGCT-4 principle topology.

## 7.7    The performance of the RGCT

### 7.7.1    Prototype RGCT

Figure 7-28 shows a prototype RGCT developed based on RGCT-4. The GTO is a 4.5kV device with a maximum turn-off current of 2.0kA at a 2µF dv/dt snubber. As can be seen, the connection between the GTO and the gate driver is a 20-inch flexible cable. The resonant capacitance is 144µF, the resonant voltage used is 50V and the clamp voltage is 18V unless specified. The anode current is sampled through a current shunt while the gate current is through a Rogowsky current transducer.

### 7.7.2    Current commutation during the turn-off transient

To investigate the turn-off current commutation process, snubbered turn-off experiments were first carried out. Figure 7-29 shows the transient waveforms of the RGCT turning off at 1.5kA/1.5kV. The voltage on the gate-cathode of the GTO was measured at the end near the gate-driver.

The resonant current and voltage waveforms show a very good agreement with the simulation. When the turn-off switch is on, the turn-off voltage $V_R$ is applied to the GTO's gate-cathode junction and the stray inductor $L_G$ in the gate loop. Before this junction is fully recovered, it acts as a short circuit so the gate commutation di/dt is determined by $V_{GC}/L_G$, where $V_{GC}$ is the voltage across the GTO gate-cathode terminals. The unity turn-off gain is the point where the gate current and the anode current cross over. At the unity gain point, the cathode current comes to zero. In less than 0.1 µsec after the unity gain point, an abrupt di/dt change can be observed on the gate current $I_G$. This is the point when the GTO gate-cathode junction recovers. This can also be observed from the gate-cathode voltage measured near the GTO end as shown in Figure 7-31. The step-down of $V_{GC2}$ is due to the voltage blocking of the emitter junction.
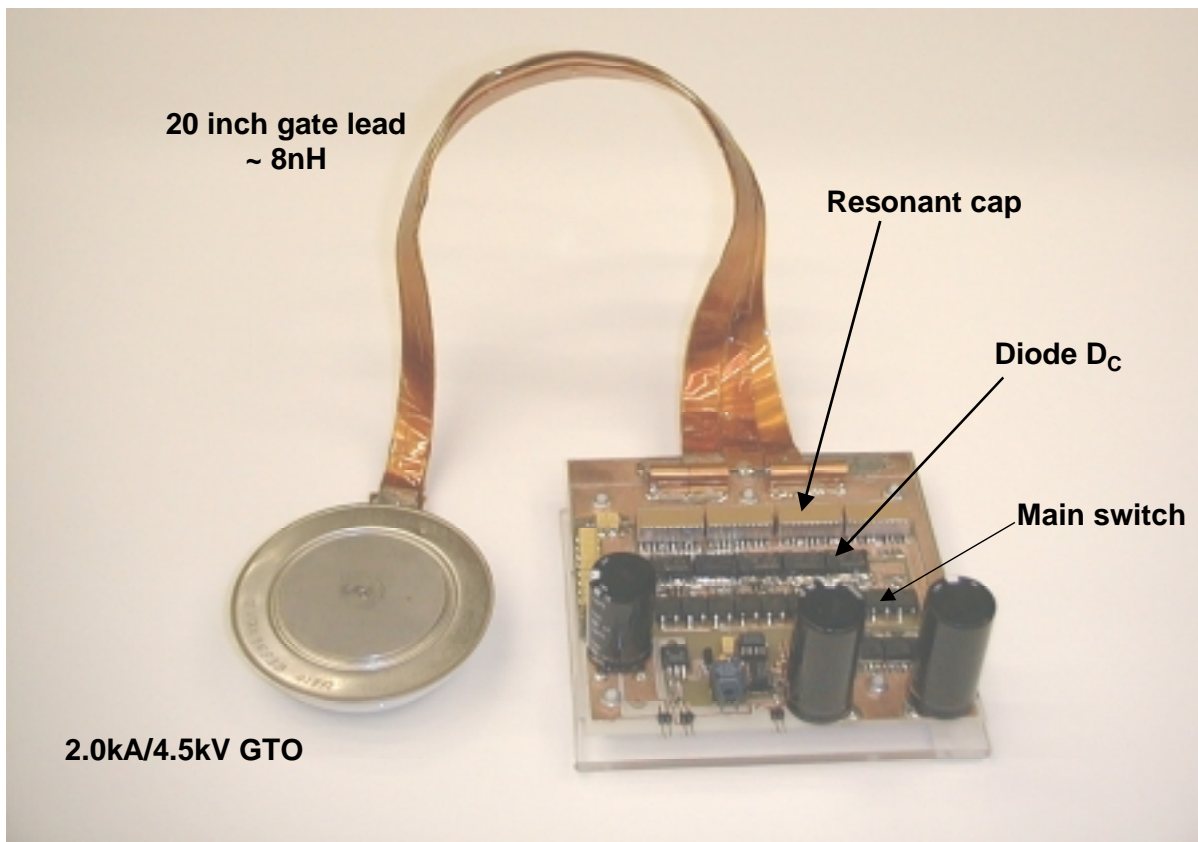


Figure 7-28 A picture of a 2.0kA/4.5kV RGCT with snubberless turn-off capability.

After this point, a new resonant process will be among the resonant capacitor $C_R$, the gate loop stray inductor $L_G$ and the gate-cathode junction, which is acting as a zener. The gate current $I_G$ resonants to its peak when $C_R$ is discharged to the level of the gate-cathode breakdown, and then

$I_G$ decreases. With the discharging of the resonant voltage, the negative $di_G/dt$ becomes lower and lower, the gate-cathode voltage $V_{GC}$ becomes lower and lower as well in this process. At about 5μsec, as is shown in Figure 7-29, the slope of $I_G$ becomes smaller and $V_{GC}$ comes back from a lower level to a higher steady value. This is the point when the voltage clamp source takes over the gate current.
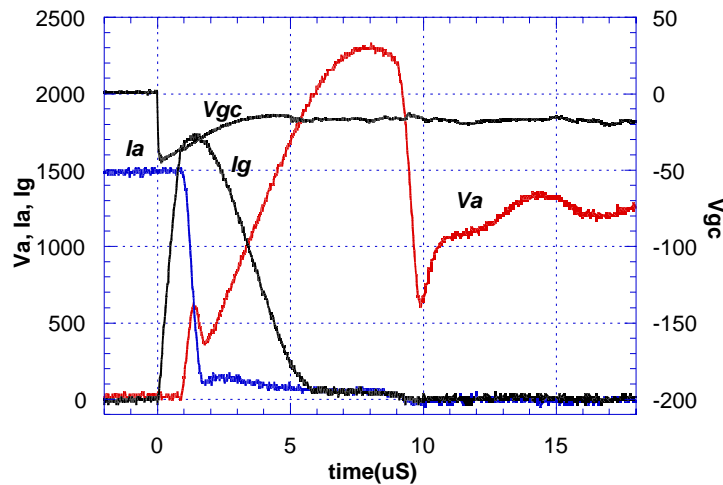


Figure 7-29 The gate current of the RGCT during snubbered turn-off.

It is therefore clear that the reverse recovery of the GTO gate-cathode junction changes the resonant condition. This recovery happens at different time when the turn-off anode current is different. Figure 7-30 shows the resonant current $I_G$ at different $I_A$. The turn-off storage time increases as the anode current increases. The resonant peak current increases slightly when the anode current is increasing because less energy is dissipated due to the breakdown of the gate-cathode junction. At all current levels, the voltage clamp source takes over the gate current before the gate current reaches the current tail value.
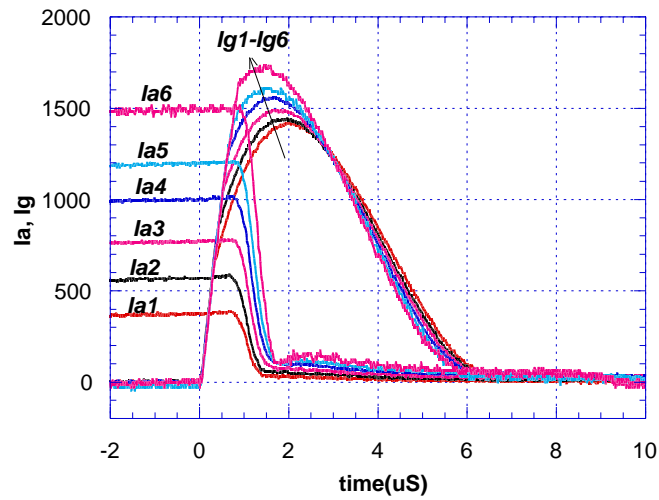
Figure 7-30 The gate current of the RGCT during snubbered turn-off.

### 7.7.3   Gate stray inductance

Figure 7-31 shows the voltage across the GTO's gate-cathode during the turn-off transient. As is analyzed above, before the reverse recovery of the gate-cathode junction, the current commutation $dI_G/dt$ is determined by:

$$dI_G/dt = V_{GC1}/L_G \qquad\qquad (7\text{-}1)$$

The $di_G/dt$, from the gate current waveform, can be read as 2.0kA/μsec, so the total gate loop stray inductance is about 20nH.

In the RGCT, $L_G$ is consisted of the stray inductance inside the GTO package and that introduced by the flexible connection. According to the voltage on the GTO gate/cathode near the GTO end, the gate loop stray inductance inside the GTO is about 12nH while that due to the flexible connection is about 8nH.

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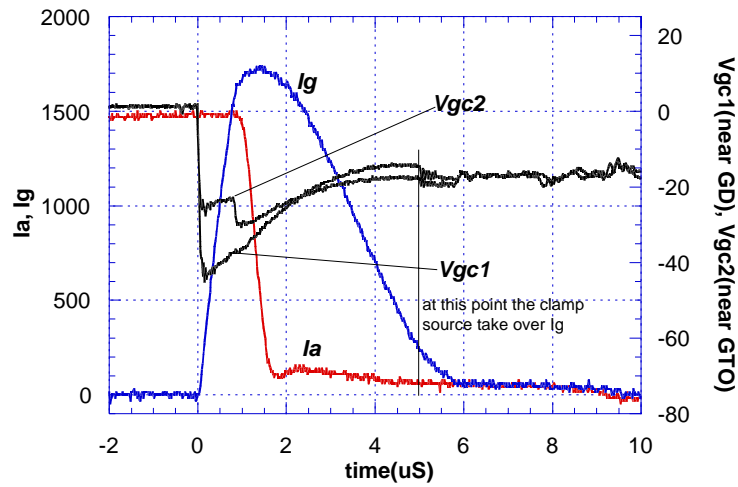
Figure 7-31 voltage on the GTO gate-cathode during the turn-off transient. $V_{GC2}$ is measured near the GTO while the $V_{GC1}$ is measured at the end of the gate connection.
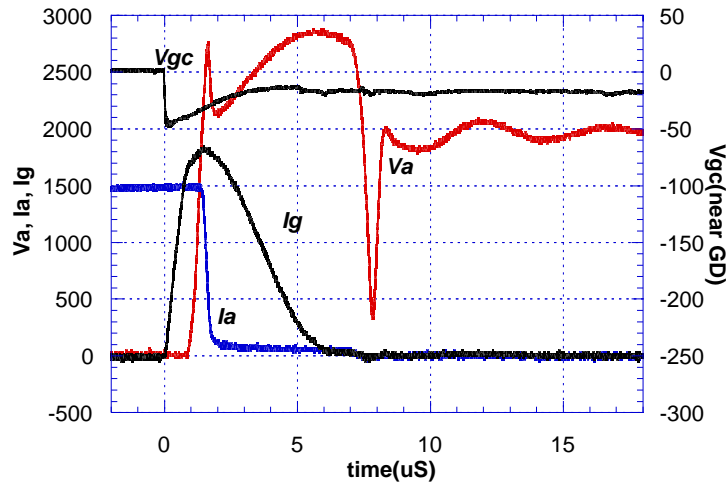


Figure 7-32 RGCT snubberless turn-off at 1.5kA/2.0kV @25C.

### 7.7.4    Snubberless turn-off demonstration

The snubberless turn-off capability of the RGCT is experimentally demonstrated as shown in Figure 7-32. The current storage time in this case is 1.4µsec and the current fall time is 0.35µsec.

### 7.7.5　Turn-on improvement

Traditional GTO has serious turn-on problem. Due to the big size of the silicon die, the turn-on process is not uniform. Those cells near the gate contact will be turned-on first and then those cells far away. This slow spreading turn-on process limits the maximum turn-on $di_A/dt$ for the GTO.

High initial turn-on gate current injection can improve the turn-on capability[E2] of the GTO. The RGCT has this improvement automatically. The resonant capacitor needs to be charged after each turn-off process. The charging can only happen when the RGCT is turned on. By arranging the charging path in series with the GTO gate-cathode junction and making an appropriate control, the charging current can be used for the GTO turn-on. The anode voltage decreases from 2.2 kV to almost zero in about 0.3 µsec.

Experiment was conducted to check the turn-on performance under different gate injection. The test circuit has a di/dt snubber and a dv/dt snubber. The purpose of the dv/dt snubber is to supply the device with a high initial turn-on di/dt. Figure 7-33 shows the measured results. The maximum turn-on injection $di_G/dt$ is more than 1.0kA/µsec.
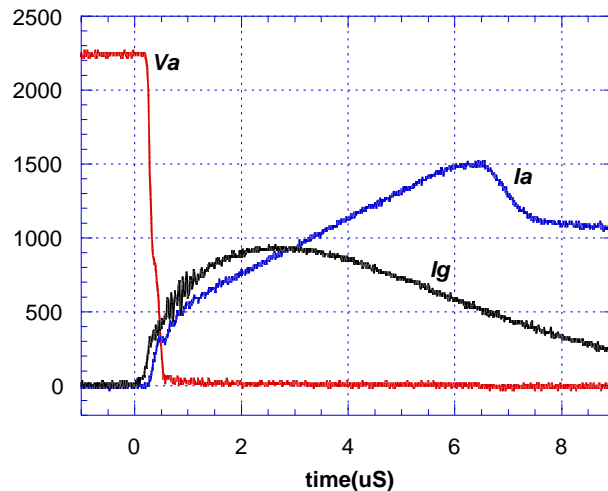


Figure 7-33 High turn-on injection current in the RGCT.

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Figure 7-34 shows the turn-on voltage waveform at different gate injection currents under the condition as for Figure 7-33. When the turn-on injection drops to about 200 amperes, the voltage shoulder becomes wider and the voltage tail becomes longer.
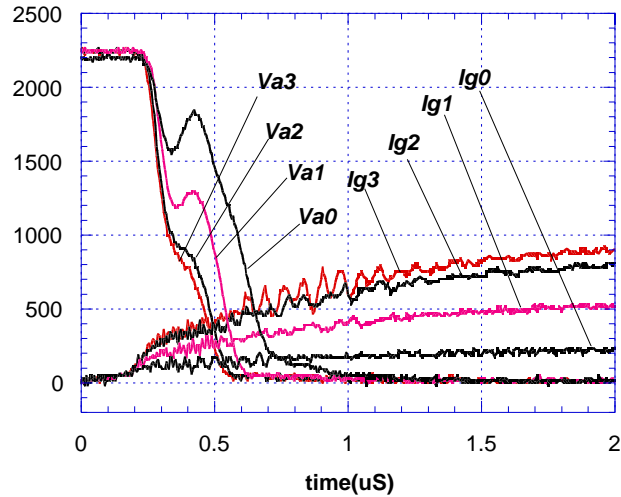


Figure 7-34 Turn-on voltage waveforms along with the gate current injection.

## 7.8    Discussion

### 7.8.1    Gating power requirement

The gating power for the RGCT is composed of three parts: the on-state DC current injection power, the OFF state holding energy and the resonant power. The pulse injection current is provided by the charging to the resonant capacitor.

The net turn-on DC injection power is relatively low. Assuming a 2-ampere injection current, the power is less that two watts. The OFF state holding power is also very low. The holding power supply needs to output the leakage current of the GTO's emitter junction.

The resonant energy can be estimated as below. The prototype RGCT has 2.0 kA turn-off capability with a 55V resonant. At a switching frequency of 500Hz, the power required for this is:

$$0.5*C_R*V^2*f=90W$$

The overall power required for a 2.0kA maximum turn-off current RGCT is thus less than 100W. This power requirement is comparable to that of a traditional GTO with the same rating. This is also reasonable compared to the requirement of the IGCT. From the gate driver heat sink point of view, the gate driver of the IGCT comes with the device, hence the additional size of the gate driver and the way to dissipate power pose a limitation. The RGCT does not have this limitation because of the flexible connection.

### 7.8.2    Gating over-drive in the RGCT

The RGCT has a gate current over-drive problem as is shown in Figure 7-30. Because the gate driver does not know the anode current, the resonant capacitor is always prepared to turn-off the maximum turn-off current.

The over-drive adds a lot more gating power and stress on the gate driver. The solution to this problem is to charge the resonant capacitor based on the anode current. One possible way to sense the anode current is through the forward voltage drop of the GTO gate-cathode junction.

## 7.9    Conclusions

A novel resonant gate comutated thyristor (RGCT) is studied. The unity turn-off gain is realized by using a high transient voltage. Snubberless switching capability is guaranteed and demonstrated experimentally. Compared to the IGCT, this technology can tolerate significantly higher gate loop stray inductance so that snubberless turn-off can be realized in a conventional GTO package along with flexible lead gate connection. Successful development of the RGCT therefore can provide a lower overall cost to advanced high power system design.

# Chapter 8 Snubberless Turn-Off of a Diode Assisted Gate Turn-Off Thyristor (DAGTO)

## 8.1    Introduction

For a traditional GTO, its turn-off voltage $V_{OFF}$ is selected below its gate-cathode junction reverse breakdown voltage $BV_{GC}$, which is normally about 20V. The maximum achievable turn-off gate current commutation rate can be expressed as:

$$dI_G/dt \leq BV_{GC}/L_G \qquad\qquad (8\text{-}1)$$

Taking 500nH gate lead stray inductance as an example, the maximum achievable turn-off current commutation rate is about 40A/μsec. This slow turn-off $dI_G/dt$ accounts for the long storage time for tradition GTOs.

Based on (8-1), there are two ways to increase the current commutation rate to achieve unity turn-off gain. Either increase the breakdown voltage $BV_{GC}$ of the GTO's gate-cathode junction or decrease the gate loop stray inductance $L_G$. The IGCT uses the latter technology. By dramatically reducing $L_G$ to about 3nH, a four-inch IGCT has achieved a $dI_G/dt$ as high as 6.0kA/μsec.

However, further decrease of $L_G$ is subject to the limitation of mechanical structure and physical size of the device. For even bigger size devices such as six-inch GTOs, which have much higher current rating and desire much higher current commutation rate to achieve unity turn-off gain, alternatives to increase $dI_G/dt$ are necessary.

Based on (8-1), another way to increase $dI_G/dt$ is to increase $BV_{GC}$---the reverse breakdown voltage of the GTO's gate-cathode junction. Normally, this breakdown voltage is hard to be increased without harming the GTO's performance. In this chapter, the design and snubberless turn-off issues of the Diode Assisted Gate Turn-Off (DAGTO) [J4] thyristor that employs a hybrid approach to improve the GTO's $BV_{GC}$, are discussed. Experimental results are presented.

## 8.2    The operational principle of the DAGTO

Figure 8-1 shows the equivalent circuit of the DAGTO. Compared to that of the IGCT, an additional diode $D_E$ is in series with the GTO. The breakdown voltage of the GTO gate-cathode diode is $BV_{GC}$; the breakdown voltage of $D_E$ is $BV_{DE}$; the turn-off voltage source is $V_{OFF}$; and the gate loop stray inductance is $L_G$. Figure 8-2 shows the expected anode current $I_A$, anode voltage $V_A$, cathode current $I_C$ and gate current $I_G$ waveforms.

During the turn-off transient t0-t1, the turn-off switch $Q_G$ is turned on, so the turn-off voltage source is applied on $L_G$ while $D_E$ and $D_{GC}$ is conducting. The turn-off current commutating rate can be expressed as:

$$dI_G/dt = V_{OFF}/L_G \qquad (8\text{-}2)$$

whereas the basic limitation for $V_{OFF}$ is:

$$V_{OFF} < BV_{GC} + V_{DE} \qquad (8\text{-}3)$$

Since $D_E$ can be implemented as a discrete diode, its breakdown voltage can be selected very high, so a very high $dI_G/dt$ can be achieved.
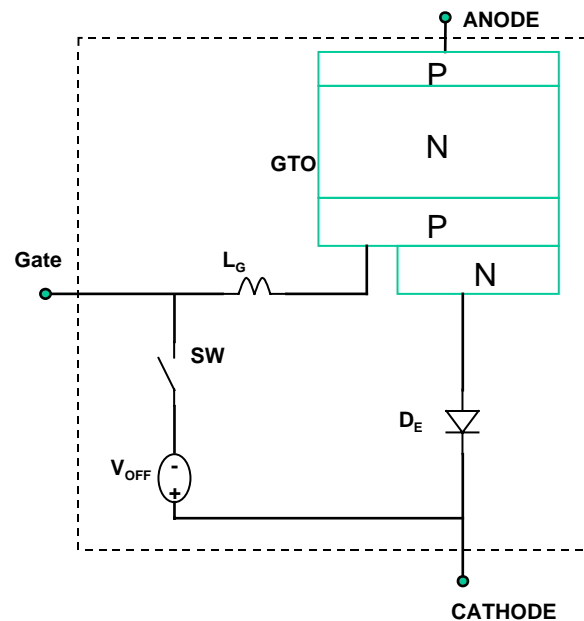


Figure 8-1 DAGTO principle circuit.
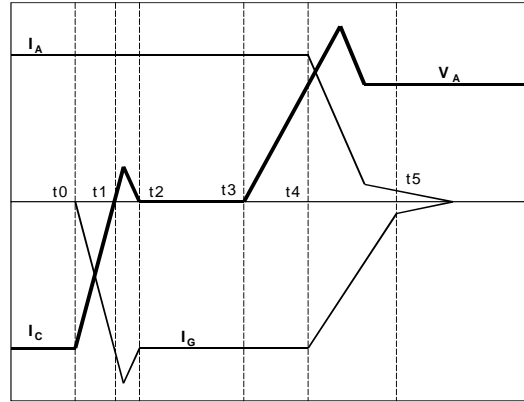
Figure 8-2 Predicted anode current, anode voltage cathode current and gate current waveforms.

Under snubberless turn-off condition.

Once the forward current in $D_E$ and $D_{GC}$ decreases to zero, the GTO enters into the unity gain turn-off condition. However, the current in $L_G$ will keep increasing after t1 until both diode $D_{GC}$ and $D_E$ finish their reverse recovery and block voltage. To limit the over current commutation, a fast reverse recovery diode should be used for $D_E$. By the end of this reverse recovery process at t2, currents through the two diodes come back and stay at zero before the end of the storage time. These two diodes will also block the turn-off voltage $V_{OFF}$.

After the end of the storage phase t3, the anode voltage begins to increase. At t4, anode voltage reaches the DC link value, and the anode current begins to decrease. The maximum gate current decay rate, which is determined by the gate loop parameters $V_{OFF}$, $BV_{GC}$, $BV_{DE}$ and $L_G$, may be slower than that of the anode current. Reverse breakdown will happen for both diodes $D_E$ and $D_{GC}$ until t5 when the gate current reaches the current tail level.

Based on the above analysis, its is clear that the DAGTO can realize higher turn-off current commutation rate by making use of the diode $D_E$. The unity turn-off gain is realized very quickly and can be maintained until the end of the turn-off transient process.

The implementation of the DAGTO can also be very simple. Making use of a single diode die in wafer form like the GTO, a DAGTO can be made by simply stacking the two dies together. The component count is therefore low compared to the ETO and the MTO. Because the press pack

diode has proven long-term reliability, the reliability of the DAGTO is expected to be high. The forward voltage drop of the DAGTO, however, will increase.

## 8.3    Design issues of the DAGTO

The design of the DAGTO is quite straightforward at the first glance. Based on the gate loop stray inductance $L_G$ and the minimum desired current commutation rate $di_G/dt$, the minimum turn-off voltage can be designed as:

$$V_{OFF}=L_G*(di_G/dt) \tag{8-4}$$

according to equation (8-2).

The design of the breakdown voltage $BV_{DE}$ of diode $D_E$ is subject to equation (8-3), which implies that $BV_{DE}$ can be from minimum ($V_{OFF}-BV_{GC}$) to infinite. However, gating power and snubberless turn-off capability induce extra constrains on $BV_{DE}$ design.

Practically, the gating power of the GTO is an important concern and should be minimized. This power is in proportional to the turn-off voltage $V_{OFF}$, switching frequency and the integration of the gate current $I_G$ as is shown in Figure 8-2.  To minimize this integration, the gate current slope in (*t4-t5*) should be increased and the over-current shoot between (*t1-t2*) should be minimized.

The gate current over shoot between (*t1-t2*) is due to the reverse recovery of diode $D_E$ and the gate-cathode diode $D_{GC}$. Therefore, a fast recovery diode should be used for $D_E$. Normally, this diode can be designed much faster than the gate-cathode diode $D_{GC}$.

The gate current decreasing rate between (*t4-t5*) is determined by two factors. First of all, this rate cannot exceed the anode current decreasing rate in this period. Secondly, this slope is also subject to the circuit loop ($V_{OFF}$-$Q_G$-$L_G$-$D_{GC}$-$D_E$), which sets a maximum:

$$(dI_G/dt)_{max}=(BV_{DE}+BV_{GC}-V_{OFF})/L_G \tag{8-5}$$

To obtain a higher gate current decreasing rate to reduce the gating power, the difference between ($BV_{DE}+BV_{GC}$) and $V_{OFF}$ should be increased.

The above analysis leads to the conclusion that an added diode with very high breakdown voltage ensures lowest gating power. However, an unwanted effective gate current injection introduced by the gate loop stray inductor $L_G$ and the parasitic capacitors of both $D_E$ and $D_{GC}$ set another limitation on the selection of $D_E$'s breakdown voltage $BV_{DE}$.

In the snubberless turn-off situation of a typical hard-driven GTO, the anode current begins to decrease after the anode voltage rises above its DC link. In the short time period hereafter inside the GTO's voltage blocking $n^-$ region, there are still a lot of minority carriers, which makes a high PNP current gain. In the presence of the high anode voltage, any positive current injection into the gate of the GTO can easily initiate a non-uniform turn-on process that will eventually destroy the device.
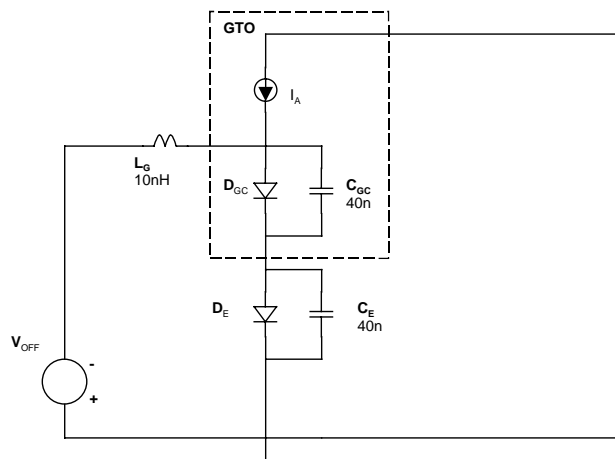


Figure 8-3 Simulation equivalent circuit for the turn-off transient of the DTO.

To investigate the possible effective gate current injection existing in the DAGTO introduced by the parasitic parameters during the turn-off transient, the simplified GTO circuit model is used for PSpice simulation. Figure 8-3 shows the simulation circuit. The GTO is modeled as a step down current source---representing the PNP transistor during turn-off---in series with a diode---representing the gate-cathode diode. The reverse parasitic capacitive effects of both the added diode and the gate-cathode diode are represented by discrete capacitors in parallel with the diodes.

Figure 8-4 shows the simulation results when the turn-off voltage $V_{OFF}$ is less than the breakdown voltage of the added diode ($BV_{DE}$=60V and $V_{OFF}$=55V). Serious current injection into the GTO gate is found both before and after the anode current fall. When all the cathode current is commutated to the GTO gate, $D_E$ and $D_{GC}$ enter into reverse recovery. During this period, the turn-off voltage source $V_{OFF}$ will build up an opposite current into the GTO cathode and extra energy in $L_G$. Because $D_E$ is designed faster than $D_{GC}$ to avoid excess reverse current being built in $D_{GC}$, $D_E$ will be recovered earlier and block $V_{OFF}$. Since $V_{OFF}$ is less than $BV_{DE}$, the extra energy in $L_G$ will now be discharged by transferring to the junction capacitance $C_{DE}$ of $D_E$ and breaking it down. The gate current begins to decrease at a rate of:

$$dI_G/dt = (BV_{DE} - V_{OFF})/L_G \qquad\qquad (8\text{-}6)$$

After a while, the GTO gate-cathode diode will also be recovered. The maximum gate current decreasing rate will be:

$$dI_G/dt = (BV_{DE} + BV_{GC} - V_{OFF})/L_G \qquad\qquad (8\text{-}7)$$

This $dI_G/dt$ is much higher than the previous one and brings the gate current to the anode current level rapidly as is shown in Figure 8-4. It is important to notice that $I_{DGC}$---net current through the gate-cathode diode---reaches zero earlier than the gate current reaches the anode current. The difference is the charging current through the parasitic capacitor $C_{GC}$ of the gate-cathode diode $D_{GC}$.


When the gate current reaches the anode current, the GTO cathode current is zero. After this point, the energy stored in the parasitic capacitor $C_{GC}$ and $C_E$ will be discharged through $L_G$, generating a positive current in the gate loop. After $C_{GC}$ is discharged to zero, this current will eventually turn on $D_{GC}$, becoming an effective gate current injection. Similar transient process will happen by the end of the turn-off current trailing edge as can be observed in Figure 8-4. This unwanted injection is dangerous for the snubberless turn-off GTO [H6].
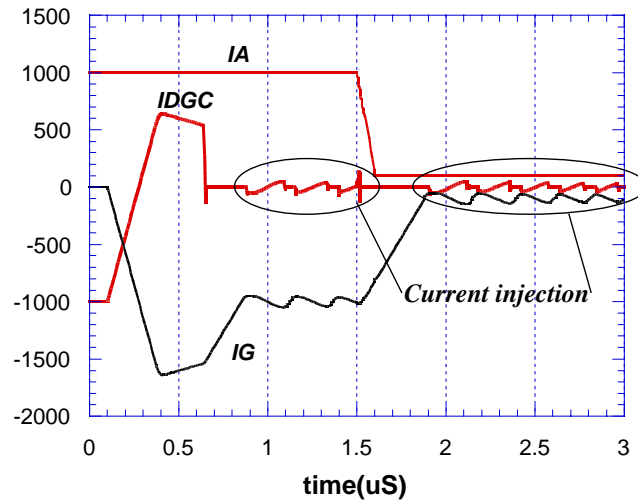
Figure 8-4 Simulation results showing the unexpected current injection during the turn-off transient.

By designing $V_{OFF}$ higher than $BV_{DE}$ with a critical margin, the effective current injection problem can be solved. Figure 8-5 shows the simulation results when the turn-off voltage $V_{OFF}$ is increased to 70V. The current in $D_{GC}$ does not flow in forward direction once it is commutated. However, the gate current overshoot is much higher and the gate current decreasing rate is slower.
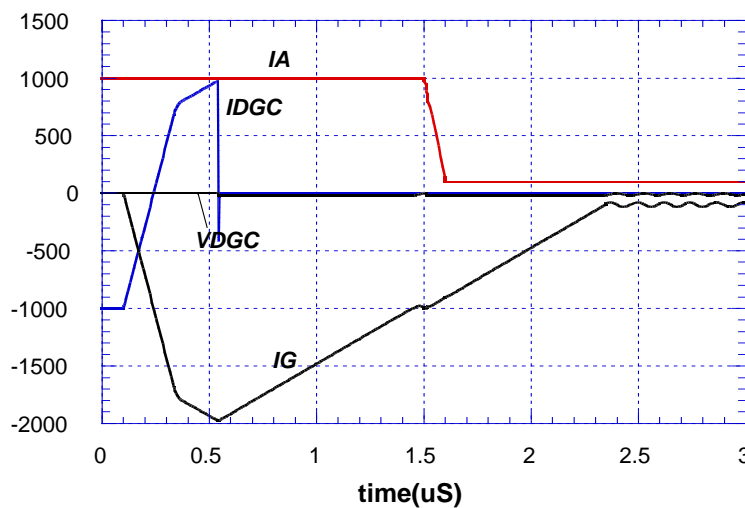


Figure 8-5 Simulation results showing that the current injection disappeared by selecting higher turn-off voltage $V_{OFF}$ than the breakdown voltage of $D_E$.

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## 8.4    Experimental demonstration

An experimental DAGTO is developed as shown in Figure 8-6 based on the above-described DAGTO principles. The diode in this model is implemented by parallelling a number of discrete diodes. The GTO used is a 53mm 1.0kA/4.5kV device manufactured by Westcode Semiconductor. The breakdown voltage of $D_E$ is 65V, and the turn-off voltage $V_{OFF}$ is 80V. Once the GTO is turned off under the unity turn-off gain condition, the uniformity of the current distribution is guaranteed. Theoretical and experimental results show that the turn-off capability of the GTO is only limited by the dynamic breakdown, which is about 200~300kW/cm$^2$ [H3]. This ensures the snubberless turn-off capability of the DAGTO. Figure 8-7 shows the tested snubberless turn-off waveform of this DAGTO at 1.0kA, 1.5kV DC link voltage.
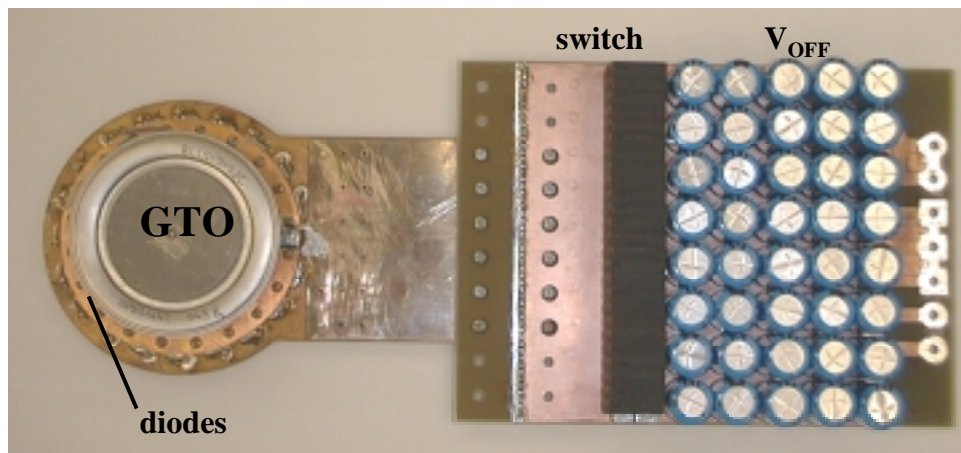


Figure 8-6 A photo of the experimental DAGTO model.

Internal voltage waveforms can be used to better understand the circuit process of the DAGTO. Figure 8-8 shows the measured voltage on the added diode ($V_{DE}$), the voltage across the turn-off switch ($V_{TOFF}$) and the depicted gate current $I_G$. By t12, the added diode $D_E$ is recovered since it blocks voltage from now on. By t2, the GTO gate-cathode diode $D_{GC}$ is also recovered. This can be identified through the voltage waveform on $D_E$. At this point, the voltage on $D_E$ is decreasing. Since the turn-off voltage $V_{OFF}$ is higher than $D_E$'s voltage blocking capability, the only reason that leads the voltage decreasing on $D_E$ is $D_{GC}$ changes to block. Starting from t4, the added diode re-enters the reverse breakdown since the circuit determined maximum *$dI_G/dt$* is lower than the anode current decreasing rate. The voltage on the added diode reaches its maximum. At t5 point, this voltage drops down a little, which means the reverse breakdown ends.
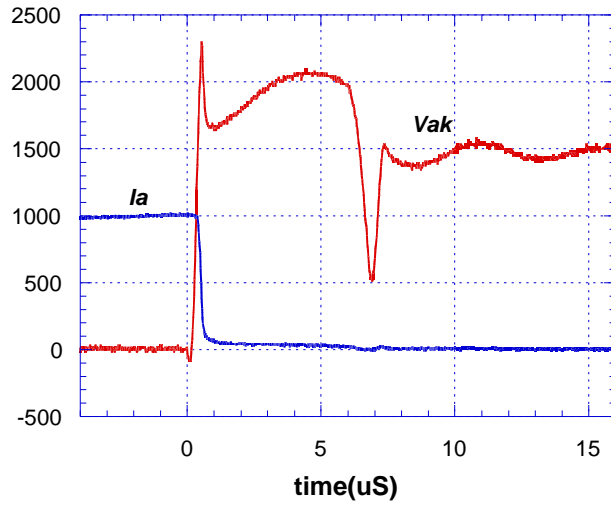
Figure 8-7 DAGTO snubberless turn-off waveforms.
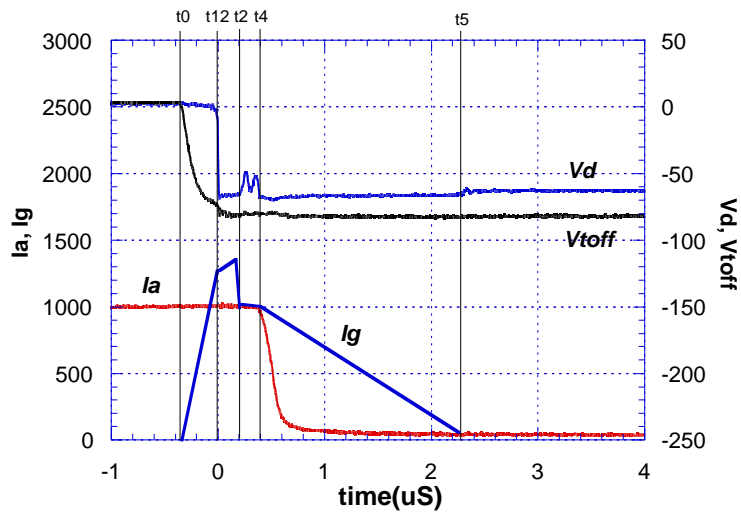


Figure 8-8 Internal voltage waveforms in the DAGTO during the turn-off transient.
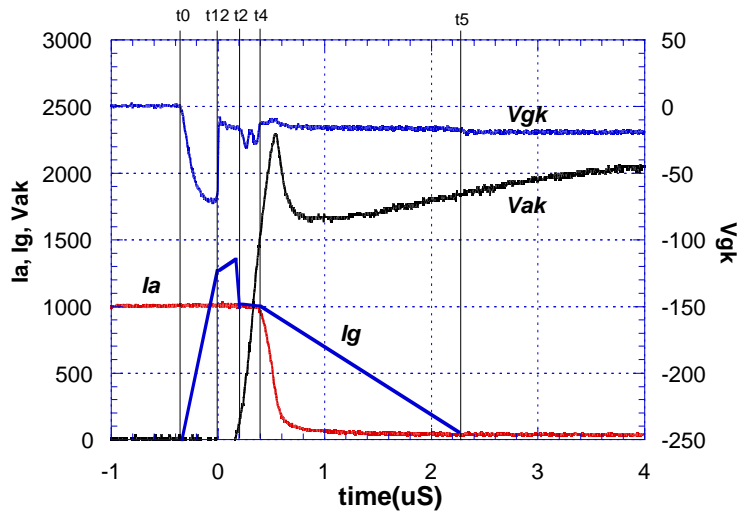
Figure 8-9 Voltages on the DAGTO during the turn-off transient.

The voltage difference between $V_{TOFF}$ and $V_{DE}$ is the voltage $V_{GK}$ across the GTO gate-cathode diode $D_{GC}$ and the gate loop stray inductor $L_G$, which is depicted in Figure 8-9. A transient high voltage is presented. After that, the voltage remains close to 20V to reverse bias the GTO's gate-cathode diode to avoid effective current injection.

The turn-off current commutation rate $di_G/dt$ and the gate loop stray inductance $L_G$ can be estimated from Figure 8-9. The time interval for the current commutation is about 0.35usec. In the meantime, about 1.2kA current is transferred from the cathode to the gate of the GTO, so the $di_G/dt$ is about 3.5kA/usec. The voltage used to overcome the GTO gate loop internal stray inductance $L_G$ is about 70V, So $L_G$ can be estimated as $70/(di_G/dt) \sim 20nH$.

### 8.5    Discussion

The prototype DAGTO has demonstrated that a much higher turn-off voltage $V_{OFF}$ can be used for the current commutation than that of the GCT. In conjunction with a reduction in the gate loop stray inductance, the current commutation rate of the DAGTO can be much higher than 6kA/μsec.

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6-inch GTOs have been commercialized for several years, having more than twice the die area of a 4-inch device. However, a 6-inch IGCT is not expected to switch twice as much current as the 4-inch IGCT. There are two reasons. One is that the gate driver cannot supply a high enough current commutation rate (12kA/μsec) to ensure the unity turn-off gain. Another reason relates to the uniformity of the turn-off transient process under unity turn-off gain. An even higher current commutation rate is needed to avoid non-uniform transient current distribution on big size silicon chip due to distributed gate path inductance and resistance [H3]. The DAGTO concept can be used to achieve this goal.

## 8.6    Conclusions

The snubberless turn-off of the DAGTO is analyzed and demonstrated. By using a discrete diode in series with the GTO, the DAGTO significantly increases the turn-off voltage that can be used for the current commutation. The unity turn-off gain and the snubberless turn-off capability are demonstrated experimentally.

# Chapter 9 Conclusions

With its high voltage blocking, large current conduction capability and low conduction loss, the high power GTO has been the dominant semiconductor device for high power applications including industry medium voltage drives, traction controls, High Voltage Direct Current (HVDCs), FACTS, StatCom, etc. However, the GTO's dynamic performances are poor. Its long switching transition times limit its practical switching frequency below 1.0 kHz. Its dv/dt snubber requirement for turn-off and di/dt snubber requirement for turn-on operations increase the complexity, size and cost of the system based on it. Higher performance and reliability applications call for better high power semiconductor devices.

This dissertation developed several new GTO based devices with fast switching speed and better RBSOA: the ETO, RGCT, and DAGTO; developed a simplified equivalent circuit model for the GTO under unity-gain turn-off for circuit level analysis; proposed a novel failure theory that is applicable for all hard-switched GTO devices.

The ETO is a hybrid integration of the high power GTO with the power MOSFET. By inserting a MOSFET in series with the cathode (emitter), the cathode current path of the GTO can be cut by turning off the series MOSFET, forcing the anode current flows through the GTO's gate. Thus the GTO in the ETO is turned off under unity-turn-off gain through a voltage control. The switching transition speed of an ETO is much faster than a traditional power GTO. Without considering the thermal capability, an ETO can operate at a switching frequency as high as 5.0 kHz. Due to the voltage controlled turn-off process, the gating power requirement of an ETO is significantly reduced to the level determined only by its turn-on operation. A typical ETO gate driver with a 5 amperes constant turn-on injection consumes about 15 watts at a switching frequency of 1.5 kHz. With the improved RBSOA capability, the ETO has successfully conducted turn-off operation with an instant power density of more than 200 kW/cm$^2$, which is about the theoretical limitation of silicon's avalanche.

The RGCT makes use of a high resonant voltage to realize the unity turn-off gain condition for the GTO. Since there is no limitation on the resonant voltage, the RGCT can be designed to realize unity turn-off gain no matter what the gate lead stray inductance of the GTO is. Since there is no inserted component, the static performance of the GTO is not affected. Also the proposed RGCT's turn-on characteristic is improved.

The DAGTO uses a discrete diode in series with a GTO to improve the reverse breakdown of its gate-cathode breakdown voltage so the turn-off voltage can be significantly increased to increase the turn-off gate current commutation rate. The design of the breakdown voltage of the added diode and the turn-off voltage are crucial to the snubberless turn-off capability of the DAGTO. The turn-off voltage should be high enough to realize the unity turn-off gain. It should also be higher than the reverse breakdown voltage of the added diode plus half of the breakdown voltage of the GTO's gate-cathode junction to avoid effective current injection during the turn-off transition.

With unity turn-off gain, the behavior of the GTO during turn-off transition is completely different from that of a traditional GTO with a higher turn-off gain. An equivalent circuit model for the GTO under this condition is proposed and analyzed.  This model is composed of a step current source in series with a diode. Since the GTO's gate-cathode junction is recovered first and the actual turn-off process is an open-base PNP process, the step current source models the turn-off behavior of the open-base PNP structure while the diode models the GTO's gate-cathode junction. This model is very useful for effective current injection analysis during the turn-off transition.

Due to the nature of hybrid integration, stray inductance is significant in all GTO-based hybrid devices. The effective current injection caused by the interaction between the GTO's gate connection stray inductance and other parameters including the turn-off voltage, the junction capacitance of the GTO's gate-cathode junction, etc. is identified as the reason that causes snubberless turn-off failure of the new GTO-based devices. Design guidelines are provided to avoid this kind of failure.

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His professional career has featured a broad scope. He worked on microwave communication systems between 1985 and 1987; designed a high power Giant Transistor (GTR) in 1989; was the director of the high frequency small signal transistor production line in 1992; led the pioneering infrared communication products development between 1992 and 1995. He also developed state-of-the-art high-power semiconductor devices between 1996 and 2000. He spent many years working on semiconductor devices. However, he found his interest on analog and digital circuits, audio amplification and radio frequency communication, microprocessor control and applications, and power conversion. He is proud of his knowledge in advanced quantum mechanics and solid state physics that always led his thought to real science.