Robustness of Gallium Nitride Power Devices

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(ABSTRACT)

Power device robustness refers to the device capability of withstanding abnormal events in power electronics applications, which is one of the key device capabilities that are desired in numerous applications. While the current robustness test methods and qualification standards are developed across the 70 years of Silicon (Si) device history, their applicability to the recent wide bandgap (WBG) power devices is questionable. While the market of WBG power devices has exceeded $1 billion and is fast growing, there are many knowledge gaps regarding their robustness, including the failure or degradation physics, testing methods, and lifetime extraction.

This dissertation work studies the robustness of Gallium Nitride (GaN) power device. The structures of many GaN power devices are fundamentally different from Si or Silicon Carbide (SiC) power devices, leading to numerous open questions on GaN power device robustness. Based on the device structure, this dissertation is divided into two parts:

The first half discusses the robustness of lateral GaN high electron mobility transistor (HEMT), which recently sees rapid adoption among wide range of applications such as the power adapter and chargers, data center, and photovoltaic panels. The absence of p-n junction between the source and drain of GaN HEMT results in the lack of avalanche mechanism. This raises a concern on the device capability of withstanding surge-energy or overvoltage stress, which hinders the penetration of GaN HEMTs in broader applications.

To address this concern, the study begins with conducting the single-event unclamped inductive switching (UIS) test on two mainstream commercial p-gate GaN HEMTs with the Ohmic- and Schottky-type gate contacts, where the GaN HEMT is found to withstand surge energy through a resonant energy transfer between the device capacitance and the

loop inductance. The failure mechanism is identified to be a pure electrical breakdown determined by device transient breakdown voltage (BV). The BV of GaN HEMT is further found to be "dynamic" from the switching tests with various pulse widths and frequencies, which is further explained by the time-dependent buffer trapping. This dynamic BV (BV_{DYN}) phenomenon indicates that the static or single-pulse test may not reveal the true BV of GaN HEMT in high frequency switching applications.

To address this gap, a novel testbed based on a zero-voltage-switching converter with an active clamping circuit is developed to enable the stable switching with kilovolt overvoltage and megahertz frequency. The overvoltage failure boundaries and failure mechanisms of four commercial p-gate GaN HEMTs from multiple vendors are explored. In addition to the frequency-dependent BV_{DYN}, two new failure mechanisms are observed in some devices, which are attributable to the serious carrier trapping in GaN HEMTs under the high-frequency overvoltage switching. At last, based on the findings in the high frequency overvoltage test (HFOT), a physics-based lifetime model for commercial GaN HEMTs utilizing the device on resistance (R_{ON}) shift is established and validated by experimental results. Overall, the switching-based test methodology and experimental results provide critical references for the overvoltage protection and qualification of GaN power HEMTs.

The second half of the dissertation discusses the robustness of the vertical GaN fin-channel junction field effect transistor (Fin-JFET), a promising pre-commercialized GaN power device with the p-n junction embedded between the gate and drain which enables the avalanche breakdown. The robustness study on GaN JFET follows similar test approaches as Si metal-oxide-semiconductor field-effect transistor (MOSFET) with two key interests: the avalanche and short circuit capabilities. The avalanche breakdown is first explored via the single-event and repetitive UIS tests and under various gate drivers, from which an interesting "avalanche-through-fin-channel" mechanism is discovered. By leveraging this avalanche path, the electro-thermal stress migrates from the main blocking p-n junction to the n-GaN fin channel, resulting in a very favorable failure-to-open-circuit signature. The single-pulse critical avalanche energy density (E_{AVA}) of vertical GaN Fin-JFET is measured to be as high as 10 J/cm^2, which is much higher than the Si MOSFET and comparable to the SiC MOSFET.

The short circuit capability is explored utilizing the hard-switching fault on the 650-V rated GaN Fin-JFET, with a gate driving circuit identical to the switching application to best mimic device operation in converters. The short circuit withstanding time is measured to be 30.5 μs at an input voltage of 400 V, 17.0 μs at 600 V, and 11.6 μs at 800 V, all among the longest reported for 600-700 V normally-off transistors. In addition, the failure-to-open-circuit signature is also shown in the single-event and repetitive short circuit tests; all devices retain the avalanche breakdown after failure, which is highly desirable for system applications. These results suggest that, while GaN HEMT is already available in market, vertical GaN Fin-JFET shows superior avalanche and short-circuit robustness and thereby can unlock great potential of GaN devices for applications like automotive powertrains, motor drives, and grids.

Robustness of Gallium Nitride Power Devices

Ruizhe Zhang

(GENERAL AUDIENCE ABSTRACT)

In recent years, many power electronics applications such as data centers and electric vehicles have witnessed a rapid increase in the adoption of wide bandgap (WBG) power devices. The Gallium Nitride (GaN) device is one of the most attractive candidates in WBG devices, owing to its good tradeoff between breakdown voltage and on resistance, as well as the small gate charge that enables high frequency switching. For power devices, their robustness against overvoltage and overcurrent stresses is as important as their performance under normal operations. However, the new material, new device structure, and new device physics in GaN power devices brought up many open knowledge gaps in their robustness study, particularly under the dynamic operation in switching circuits.

This dissertation presents the work in exploring the robustness of GaN power devices. Based on the device structure, the discussion is divided in two parts:

The first half of the dissertation focuses on the overvoltage robustness of the lateral GaN High Electron Mobility Transistor (HEMT), the commercially available device covering 30 to 900 V voltage classes. A key feature of this device is the lack of p-n junction between source and drain, leading to an absence of avalanche capability. The study is conducted on mainstream, commercial p-gate GaN HEMTs, with a combination of circuit testing, microscale failure analysis, and physics-based device simulation. The main contribution is on three aspects: identifying the single-event and high-frequency repetitive overvoltage boundaries of GaN HEMT, unveiling the failure and degradation mechanisms under transient overvoltage conditions, and providing guidelines to GaN HEMT device users with proper robustness test methodology for device qualification and screening.

The second half of the dissertation focuses on the robustness of vertical GaN fin-channel junction field effect transistor (Fin-JFET), a promising pre-commercial GaN power device with the p-n junction implemented between the source and drain. The robustness tests follow the classic approaches deployed for Silicon power devices, where both the avalanche and short circuit capabilities are investigated. From the single-event and repetitive test results, the GaN JFET shows excellent avalanche robustness with a desirable failure-to-open-circuit behavior, as well as a critical avalanche energy (E_{AVA}) of 10 J/cm^2 that is higher than the Silicon metal-oxide-semiconductor field-effect transistor (MOSFET) and comparable to the Silicon Carbide MOSFET. For a 650-V rated GaN Fin-JFET, a record high 30.5 μs short circuit time is demonstrated under the hard-switching fault condition at 400 V input voltage. Overall, the results show great potential of GaN power devices for the power electronics applications that involve more stressful operation conditions for devices.

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Chapter 1: Introduction

1.1 Introduction of Silicon and Wide Bandgap Power Devices

Power device is the key component in almost any power electronics circuit. Power devices act as solid-state switches in circuit, and they are required to block high voltage in their off-state and offer small on resistance (R_{ON}) when being turned-on to conduct the current [1]. Along with the power device history, Silicon (Si) has maintained its dominance for more than seven decades. From the first successful demonstration of the bipolar junction transistor (BJT) in 1948 [2], the structure of Si-based power devices has been renovated to achieve a faster switching speed, lower conduction forward voltage (represented by the on resistance, R_{ON}, for unipolar devices) for a specific breakdown voltage (BV) : from the invention of metal-oxide-semiconductor field-effect transistor (MOSFET) in 1959 [3], to the Insulated Gate Bipolar Transistor (IGBT) that combines the advantages of both the bipolar current conduction of BJT and fast switching of MOSFET in 1979 [4] and finally, the invention of superjunction MOSFET in 1980s [5] broke the limit of the 1D trade-off with a drastically reduced R_{ON}, and Si CoolMOS^{TM} hit the market with over 600 V voltage rating. Meanwhile, the potential of Si was almost fully exploited.

However, the quest never ends on developing new generation of power devices, researchers have always been exploring alternative materials and novel device architectures to overcome the limitations of Si devices. When judging the potential of a material for 1D unipolar power devices, a figure of merit (FOM) proposed by Baliga is usually used, which is defined in formula (1) [6]:

$$\frac{BV^2}{R_{on,sp}} = \frac{\epsilon \mu_n E_C^3}{4} \tag{1}$$

where BV is the device breakdown voltage, $R_{on,sp}$ is the specific on-resistance (the product of resistance and chip area), ϵ is material permittivity, μ_n is the carrier mobility, and E_C is the critical electric field of the material. From (1), a slight increase in the E_C would boost the FOM by a cubic power law. While a 2 (for indirect semiconductor material) or 2.5 (for direct semiconductor material) power factor relationship is unveiled between semiconductor material bandgap (E_g) and E_C [7], i.e., $E_C \propto E_g^{2.5}$, it can be clearly seen that thanks to the higher E_C, wide bandgap (WBG) power semiconductor devices offer a much smaller $R_{on,sp}$ at the same voltage rating compared to

Si devices, which enables much smaller device size, leading to lower device capacitance and enables faster switching speed. Hence, WBG devices are drawing more and more attention for next-generation power electronics applications targeting higher power density and efficiency.

The two most popular candidates in the WBG material family are Gallium Nitride (GaN, direct bandgap material with a bandgap of ~ 3.4 eV) [8] [9] and Silicon Carbide (to be more specific, 4H-SiC, indirect bandgap material with a bandgap of ~3.2 eV) [8]. Compared to Si, whose bandgap is ~ 1.1 eV, GaN and SiC are equipped with an around 10 times higher critical electric field (E_C).

Figure 1-1 plots the limits of Si, SiC and GaN for unipolar power devices. From the FOM, it can be clearly seen that a 10 times higher E_C gives a drastic decrease in $R_{on,sp}$ for the same BV: by increasing the doping or carrier concentration and reducing the thickness or length of the drift layer. Therefore, WBG devices allow for smaller die size for a specific R_{on} or current rating, as well as smaller device capacitance, as compared to Si devices, further enabling fast switching operation up to megahertz, and reducing the size of the passive components. These allow for the system miniaturization in many applications such as datacenter and portable adapter [1] [10] [11] [12][13].

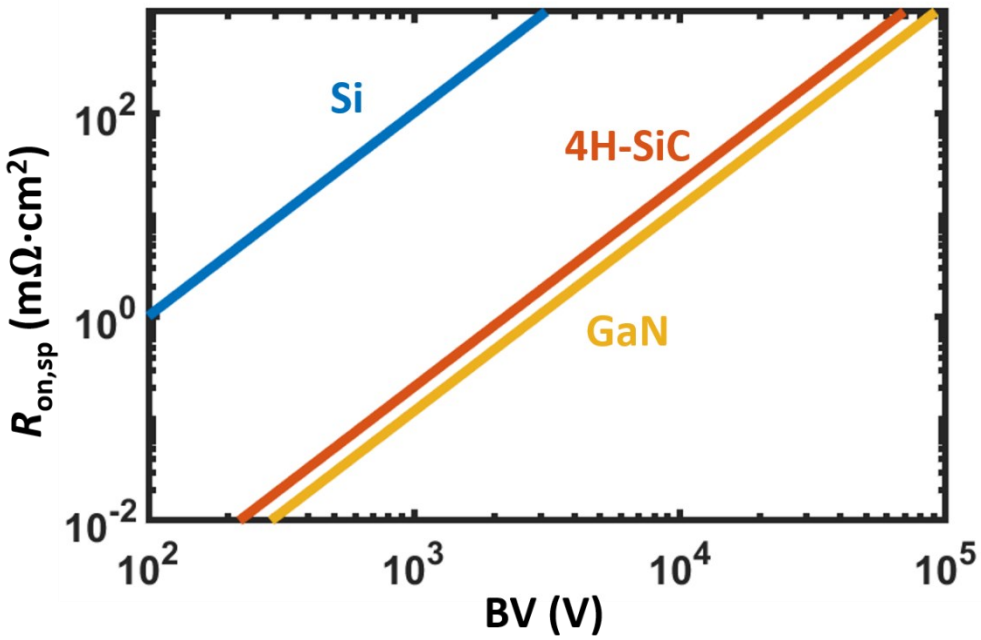


Figure 1-1. Unipolar limits of Si, 4H-SiC and GaN power devices.

Another advantage of WBG device is the high temperature operation capability. Since semiconductor material bandgap usually shrinks with increasing temperature, leading to an increase in intrinsic carrier density and off-state leakage current [14]. Wider bandgap material has much lower intrinsic carrier density compared to Si, which reduces the leakage and allows the dopant to be effective at higher temperature, hence allowing for a higher temperature tolerance in operation. GaN high electron mobility transistor (HEMT) has been reported to safely operate at 400 ºC [15] while similar result has also been reported on SiC-based power junction-gate field-effect transistor (JFET) [16], which is an unmatched capability by Si-based power devices, as the usual max temperature limit of Si devices is merely 125 ºC [13].

1.2 Knowledge Gaps in GaN Power Devices Robustness Study

Compared to SiC, the advantages of GaN include a slighter wider bandgap hence a higher breakdown electric field (E-field), and a higher mobility in either bulk GaN or the two-dimensional-electron-gas (2DEG) at the Aluminum Gallium Nitride (AlGaN) / GaN interface. The electron mobility is reported to be over 1800 cm^2/Vs in the 2DEG [17], and over 1200 cm^2/Vs in bulk GaN material [18], which is over twice or 1.5 times of the electron mobility in SiC [19]. Theoretically, GaN devices possess a better FOM over SiC devices that can enable a higher switching frequency, higher power density and efficiency in the power electronics systems. In academia, GaN devices have been demonstrated with a voltage class up to 10 kV and performance exceeding the SiC 1D limits [20]–[23]

In recent years, the industry has seen the prosperity of GaN power devices, which results from both the superior performance and processing maturity of GaN power devices, as well as the effort on solving the challenges on electromagnetic interference (EMI) [24]–[26], magnetic design [27]–[30] and circuit control [31]–[33] in high frequency operations. With the introduction of the first GaN-based cell phone charger into the market in 2018, GaN has been quickly adopted in various applications including but not limited to power adapter, motor drive, on board charger, power modules for datacenter, advanced CPU and GPU [34]–[37]. The market size of GaN power devices is projected to exceed $1.26 billion by 2027 [38].

However, apart from the superior device performance, power device robustness is another key aspect to consider when deploying new generation devices into power systems [39]. Device robustness refers to the device capability of withstanding abnormal events near or out of its safe operation area (SOA). As shown in Figure 1-2, a typical SOA is limited by current, voltage and power dissipation (thermal); the common abnormal events include the short-circuit and the overvoltage or avalanche. Short circuit events are the transients that power devices conduct current several times higher than the rated value, usually at a high blocking voltage from the power source. The overvoltage or avalanche events are usually induced by an inrush of inductive energy to the off-state devices, in such the transient device drain voltages are higher than their rated value. In recent years, some major concerns about GaN device robustness have slowed down the penetration in specific applications [39]. These concerns are primarily raised from the differences in the device architecture and physics compared to Si and SiC devices. In the rest of this section, major knowledge gaps in both lateral and vertical GaN power devices robustness study will be discussed.

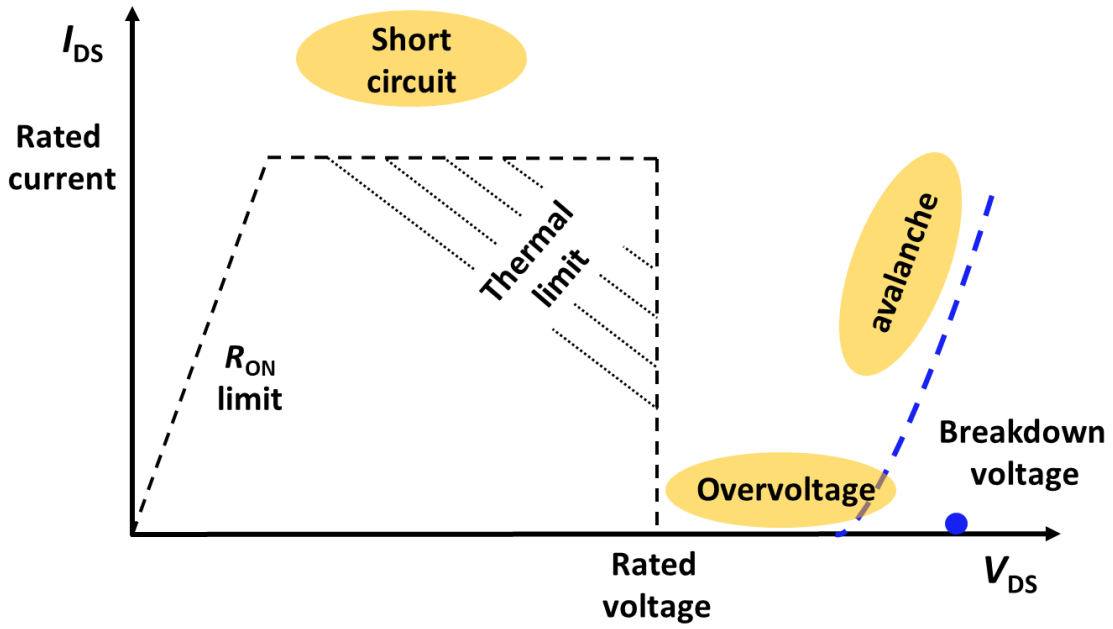


Figure 1-2 Common stressors in power device robustness studies in comparison to the device's SOA.

1.2.1 Lateral GaN High Electron Mobility Transistor (HEMT)

The most representative lateral GaN device is the GaN high electron mobility transistor (HEMT), which has been commercialized from 15 V to 900 V by multiple vendors, covering various low voltage application profiles. The GaN HEMTs leverage the 2DEG to form the conduction channel, the enhancement mode (E-mode) operation is realized by placing a piece of p-GaN gate (p-gate) on top of the AlGaN barrier to lift the conduction band and deplete the local 2DEG underneath the p-gate region. In general, there are two types of E-mode p-gate GaN HEMT available in market, namely the hybrid-drain gate injection transistor (HD-GIT) and the Schottky p-gate HEMT (SP-HEMT). As shown in Figure 1-3(a), in the HD-GIT, gate metal forms an Ohmic contact to p-GaN and the AlGaN barrier is recessed, such to facilitate the hole injection into the

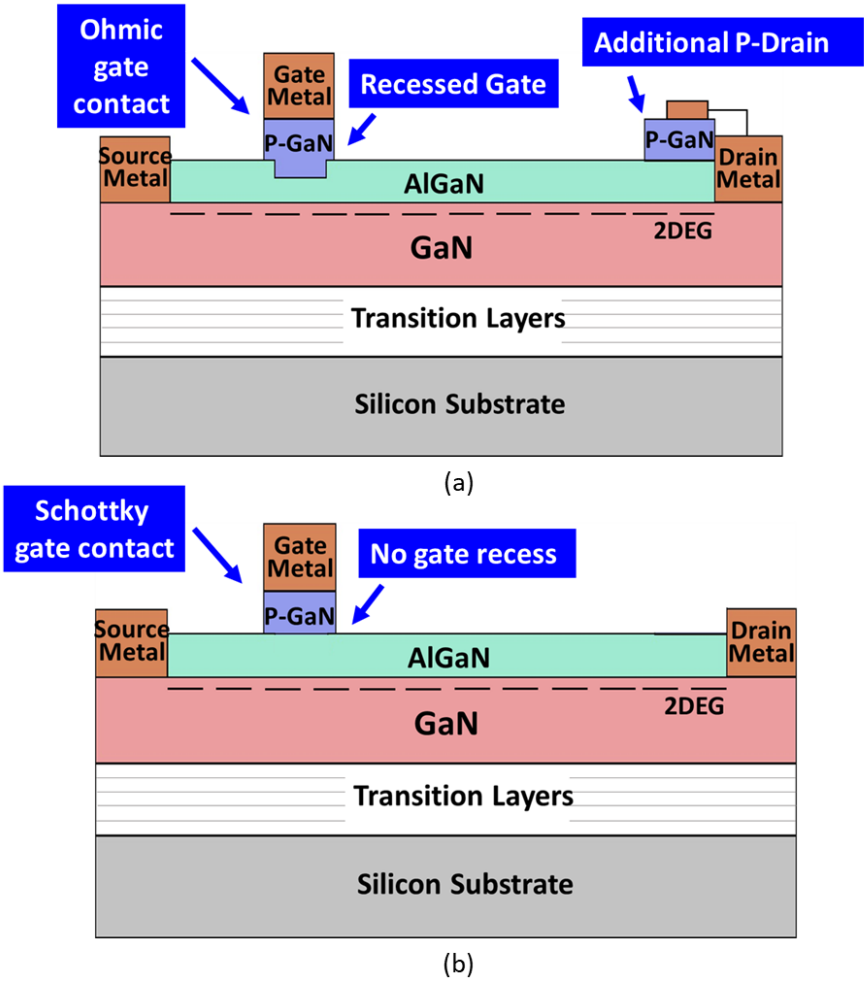


Figure 1-3. Schematic structure of the (a) HD-GI and (b) SP-HEMT.

2DEG channel for conductivity modulation. Another piece of p-GaN connects with the drain to suppress electron trapping under high drain bias, referring as the "hybrid drain" structure [40]. While in SP-HEMTs, gate metal forms a Schottky contact to p-GaN that gives a higher gate overvoltage margin (Figure 1-3(b)), and there is no gate recess or hybrid drain design.

In regards of device robustness, there are two key differences comparing GaN HEMT and power MOSFET. The first one is the lack of avalanche breakdown mechanism in GaN HEMT. Figure 1-4(a) illustrates the avalanche process in a power MOSFET. Avalanche breakdown is a carrier impact ionization (I. I.) and multiplication process: it is initiated in the semiconductor region with the peak electric field (E-field); the I. I. generated electron-hole pairs are accelerated by the local E-field and collide with lattice atoms to generate an increasing number of electron-hole pairs [41]. To maintain a sustained avalanche, the carriers produced in the I. I. and multiplication must be effectively removed via the p-n junction structure connected to the device electrodes. During the avalanche process, fast generation and effective removal of I. I. carriers prevent further rise of the peak E-field and minimize the risk of device electrical breakdown. As shown in Figure 1-4(b), when avalanche breakdown occurs in power applications, device drain bias (V_{DS}) will be clamped at its avalanche breakdown voltage (BV_{AVA}), and the inductive current (I_L) goes down with the energy is dissipated within the device. This process protects the device from surge energy events. Therefore, avalanche breakdown is highly desirable for power devices.

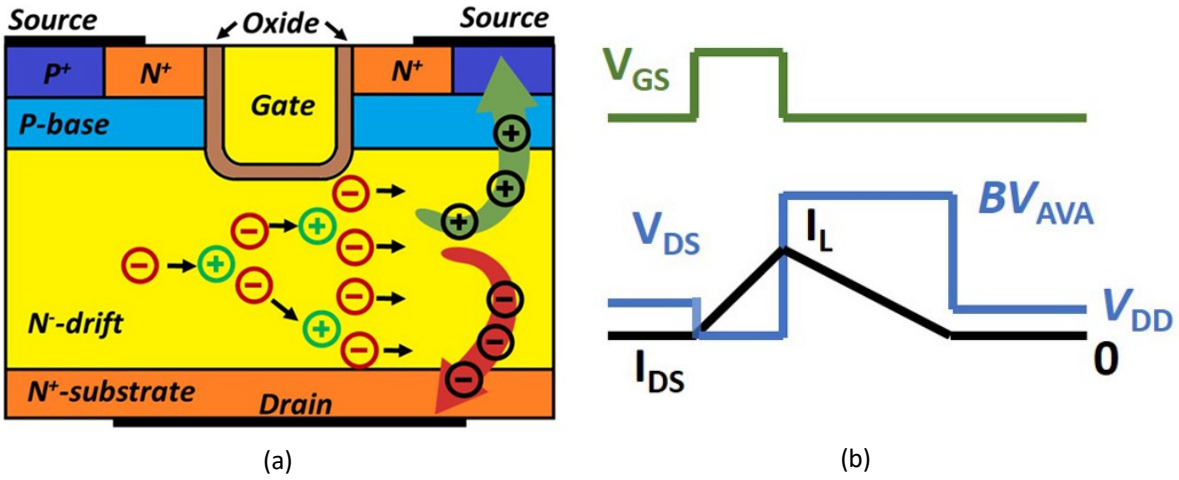


Figure 1-4. Illustration of the (a) avalanche process in a power MOSFET, (b) avalanche waveforms under surge energy stress.

However, as shown in Figure 1-3, there is no p-n junction between the source and drain of a power GaN HEMT, hence a non-avalanche breakdown is expected when the device undergoes transient surge energy or voltage spike. This inherent difference leads to the following knowledge gaps on the GaN HEMT surge energy robustness: (a) How do GaN HEMTs withstand surge energy? What are the physical dynamics in the withstanding process? (b) What determines the failure of GaN HEMTs under surge energy? (c) Do different types of GaN HEMTs fail with the same mechanisms and behaviors?

The second difference is the epitaxy layer growth: power MOSFETs are usually fabricated on homogeneous epitaxy layers, i.e., Si MOSFETs are fabricated on Si epitaxial layers grown on a Si substrate. The homogeneous epitaxy avoids the lattice mismatch thus minimizes the defect density in the epitaxy layer. However, for commercial GaN HEMTs, the GaN epitaxial layers are usually grown on Si or sapphire substrate. The lattice mismatch leads to considerable number of defects. Meanwhile, to prevent vertical leakage, dopants such as Carbon (C) and Iron (Fe) are added into the GaN epitaxy. All these defects and external dopants form the traps in the GaN layer, covering a wide activation energy from 0.089 to 3.22 eV [42], almost a full expand of GaN bandgap. From the literature, the dynamic response of trapping and de-trapping changes the charge distribution profile in GaN HEMT, which leads to various issues including the dynamic R_{ON} and threshold voltage (V_{TH}) instability. Considering the overvoltage robustness, device BV is highly dependent on the charge distribution, therefore, the non-switching static tests may not give accurate BV measurement; a switching circuit-based testbed is required. Following the aforementioned knowledge gaps, two more open questions emerge: (d) How to design proper test setup that can best correlate the experimental results to their operation in high frequency switching converters? (e) How to project the GaN HEMT lifetime in applications, when overvoltage transient occurs due to parasitic or leakage inductance? In this dissertation work, comprehensive studies are conducted to address the knowledge gaps above, the key findings are presented in the following sections.

1.2.2 Vertical GaN Fin-Channel Junction Field Effect Transistor (Fin-JFET)

Compared to lateral GaN HEMTs, vertical GaN FETs are more attractive for applications over 600-V class. In vertical devices, for a higher device BV, the drift region thickness of vertical devices increases without expanding device area. But in lateral GaN HEMTs, in order to increase device breakdown voltage, drain to gate distance needs to be expanded, which increases die size

that leads to a higher cost. The vertical structure can also allow for a superior thermal management due to more spreading current and electric field distributions [43]. Due to the reasons above, building up vertical GaN FET for high voltage, high power density applications has been a hot topic in power devices society over a decade [44]–[46].

Vertical GaN Fin-JFET is a pre-commercial WBG power device with voltage rating up to 1.2 kV [47], [48]. The cross-section structure of the GaN Fin-JFET is shown in Figure 1-5. In the Fin-JFET, an array of sub-micrometer wide n-GaN pillars forms the vertical channel, and they are surrounded by the heavily doped p-GaN, forming a gate-all-around structure. The E-mode or normally off operation is realized by the depletion at the gate p-n junction: at zero gate bias (V_{GS}), the p-GaN gate depletes the entire n-GaN channel laterally and pinches off the current conduction.

The GaN Fin-JFET has achieved a smaller $R_{on,sp}$ compared to state-of-art GaN HEMT at the voltage rating of 600 V [49], indicating the great potential of the device. However, the development of GaN Fin-JFET is still at a relatively early stage, and almost no robustness research has been conducted. With the p-n junction incorporated in the device, the avalanche breakdown and avalanche energy (E_{AVA}) are key interests for this device. Meanwhile, in MOSFET, the p-n junction is formed between drain and source, hence the avalanche current naturally flows through

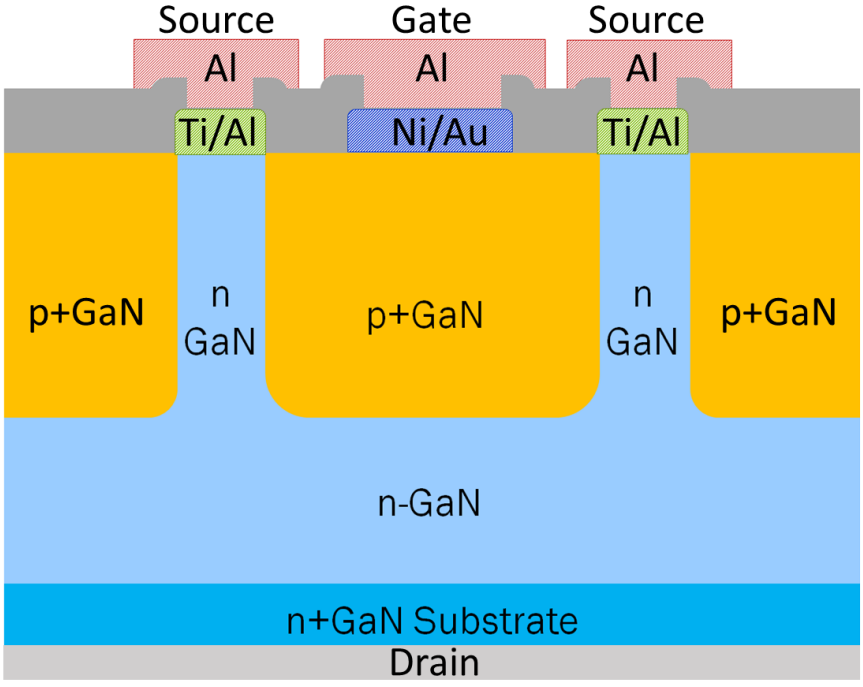


Figure 1-5. Device schematic of the vertical GaN Fin-JFET (not to scale).

the power loop in circuit. However, in GaN Fin-JFET, the p-n junction is between gate and drain, hence the avalanche current path in GaN Fin-JFET could be distinct from the MOSFET. Short circuit robustness is also a key interest when studying power device robustness, as an over 10 μs short circuit withstanding time (t_{SC}) is usually required in applications such as EV powertrains and smart grids [50]. In the investigation of avalanche and short circuit robustness, it is essential to determine the critical E_{AVA} and t_{SC} in single-event test. Additionally, exploring device degradation mechanisms in repetitive events is also preferred as it offers deeper understanding of device physics and provides key information for further improvement of device robustness.

1.3 Robustness Testing Methods for GaN HEMTs

Typical power device robustness testing methods and robustness standards were developed in the era of Si, with the interests focusing on the abnormal events such as avalanche and short circuit, as well as accelerated lifetime extraction. Those methods and standards have also been adopted in WBG devices and provide key understanding on device robustness. However, resulting from the new material and new device architecture in WBG power devices, the traditional robustness test methods cannot reflect some failure or degradation modes, for example, those induced by the carrier trapping in GaN HEMTs.

Overall, the robustness testing methods can be divided into two groups according to the device operation condition during the test, namely the static (non-switching) and switching test methods. This section briefly introduces the commonly used testing methods, discusses their outcomes and limitations, and provides insights on further optimization of robustness testing methodology for GaN power devices. A thorough discussion is presented in a recent review paper [39].

1.3.1 Static Test Methods

In static reliability testing, the device under test (DUT) is usually kept in the off-state, and a consistent bias is applied on the DUT terminals. The two widely adopted test methodologies are the high temperature reverse bias (HTRB) test and high temperature gate bias (HTGB) test.

In the HTRB test, a drain bias stress at over 80% of the DUT voltage rating is applied at drain terminal, along with a temperature of 150 °C. Up to date, multiple GaN HEMT vendors have published their HTRB test results with the focus on qualification failure mechanisms determination

and lifetime extraction. However, among the vast number of reports, only one vendor reported the HTRB test at a bias higher than the device voltage rating [51]. The complication in selecting proper voltage stress originates from the lack of avalanche breakdown in GaN HEMTs. For a bias over voltage rating, the rise in leakage current will enhance the carrier trapping, which leads to a faster failure of GaN HEMT and thereby a possibly underestimated lifetime projection. Meanwhile, the continuous high bias on drain in the HTRB test does not represent the transient overvoltage condition with a resonance nature in practical power systems.

The testing methodology in HTGB test is similar to HTRB, with the bias applied on the gate terminal. Compared to Si or SiC MOSFETs, GaN HEMTs have much smaller gate overvoltage margin and the gate robustness is a particularly important topic as well. Up to date, a time dependent dielectric breakdown (TDDB) mechanism is widely accepted in the reports from both academia and industry [52], [53], but most of the tests are still DC bias based.

1.3.2 Switching Test Methods

In switching tests, DUT turn-on and turn-off transients are involved, either in a manner of single-event or continuous switching. Some switching tests are the legacy from the Si era, such as the unclamped inductive switching (UIS) test and the short circuit test. Recently, mission profile tests based on circuit application scenarios are drawing increased attention in GaN HEMTs robustness studies [54], [55]. Meanwhile, the switching-based tests are also emerging for the gate reliability and robustness studies for GaN HEMTs [53], [56].

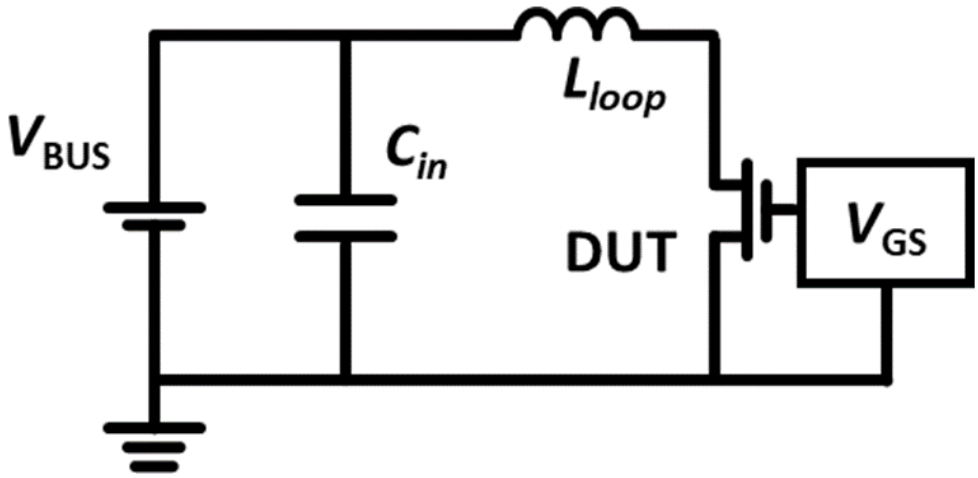


Figure 1-6. Circuit schematic of the UIS test.

The schematic of the UIS circuit is shown in Figure 1-6. The inductor stores the energy when the DUT is turned on, when the DUT is turned-off, the inductive energy surges into the off-state DUT. The UIS test is originally designed to characterize the avalanche energy for power MOSFETs. From 2016, researchers started to apply the UIS test on GaN HEMTs. However, controversial conclusions have been reported in [57]–[61]. Saito *et al*. [57]–[59] concluded that their p-gate GaN HEMTs retain some avalanche capability enabled by the hole removal through the p-GaN/AlGaN/GaN gate stack. In contrast, Kozárik *et al*. [60] and Martinez *et al*. [61] claimed that the UIS capabilities of p-gate GaN HEMTs are not due to avalanche but originates from capacitive charging. Further discussion on the UIS test is presented in Chapter 2 of the dissertation.

Another key robustness requirement for power devices is the short circuit capability. A general requirement is the short circuit withstanding time (t_{SC}) should be longer than 10 μs without failure for the protection circuit to intervene [50]. In this dissertation work, only the short circuit robustness of vertical GaN Fin-JFET is discussed because the GaN HEMT short circuit robustness has been studied extensively in the literature. GaN HEMTs are reported to be vulnerable under short circuit stress with a t_{SC} under 1 μs at 400 V bus voltage for 650 V rated GaN HEMTs [62]. It should be noted that in some literatures, the t_{SC} of GaN HEMTs is reported to be much longer, because the testing profiles adopt large R_G or parasitic inductance. In order to capture the robustness data that provide closet reference for applications, switching robustness tests that best mimic the application scenario need to be adopted.

Apart from the UIS and short circuit test, various mission profile tests have been conducted to study the GaN HEMT degradation and lifetime under switching stress. Examples of such switching stress setup include the hard-switch boost converter [63], soft-switch LLC converter [64], double pulse test setup [63]. Currently, there is no switching testing standard established for GaN HEMTs. This is partly because the GaN HEMT's degradation mechanisms under switching stress are diverse and have not been fully understood.

1.4 Motivation of the Research

The objective of power device robustness study is usually concluded into three categories: identifying, understanding, and guiding. While in the study on the surge-energy and overvoltage

robustness of GaN HEMTs and the robustness study on vertical GaN Fin-JFET, the motivation and expected outcomes are summarized below:

1. Identifying: identify device BV under various testing conditions that set the hard failure boundaries of GaN HEMTs. Identify the critical E_{AVA} and t_{sc} of vertical GaN Fin-JFET.
2. Understanding: due to the distinct structures of GaN HEMT and GaN Fin-JFET in comparison with power MOSFETs, understanding the device failure and degradation mechanisms under overvoltage, avalanche or short circuit conditions is of major interest in this dissertation work. The non-avalanche nature and the existence of high-density trap states in GaN HEMT, the formation of gate p-n junction in GaN Fin-JFET are found to impact device behaviors, failure and degradation modes under robustness test conditions.
3. Guiding: based on the understanding gained from the robustness test, guidance is expected for GaN HEMT device users on how to properly qualify device robustness, protect devices in applications, as well as project device lifetime in operations. Provide feedback to GaN HEMT and GaN Fin-JFET device designers and manufacturers for further improving the critical device and material structures that determine the device reliability and robustness.

1.5 Contribution of This Dissertation

The work presented in this dissertation addresses several important knowledge gaps on the robustness and reliability of lateral GaN HEMTs and vertical GaN Fin-JFET. The key findings include: new overvoltage failure and degradation mechanisms, new testing methodology of device reliability and robustness under the high frequency overvoltage switching, and new avalanche breakdown mode. More specifically, this dissertation establishes the following:

1.5.1 Surge-energy and Overvoltage Robustness of GaN HEMT

1. Under the single-event UIS test, the p-gate GaN HEMT is found to withstand surge energy through a resonant energy transfer between device output capacitance (C_{OSS}) and the loop inductance, rather than a resistive energy dissipation as occurred in avalanche. The device failure occurs at the transient of peak resonant voltage and is limited by the device overvoltage capability, indicating the energy is no longer the most meaningful parameter that can directly represent the intrinsic robustness of GaN HEMTs. In a surge-energy event,

almost no energy is dissipated in the resonant withstand process and the device failure is dominated by electric field rather than thermal runaway.

2. From the UIS tests with various pulse widths from 20 ns to 2 s, the BV of GaN HEMT is found to increase with the decreased pulse width, up to 500 V higher than the static BV measured on the curve tracer. This behavior is explained by the reduced buffer trapping and the resulting lower peak electric field in shorter pulses. This "dynamic BV" (BV_{DYN}) provides additional overvoltage and surge-energy margin for GaN HEMTs when being used in converters.

3. The overvoltage robustness of GaN HEMTs is found to also depend on frequency. In the high frequency overvoltage test (HFOT), a novel converter-based testbed with the active clamping circuit (ACC) is designed and prototyped, allowing for >1 kV overvoltage at switching frequency (f_{sw}) up to 1 MHz. The test results see the frequency dependent BV in some commercial p-gate GaN HEMT with two new degradation mechanism identified: a drastic, nearly unrecoverable increase in R_{ON} due to severe electron trapping in the GaN HEMT, and a degradation of the OFF-state leakage current and BV due to the trapping in the GaN buffer. Finally, the repetitive UIS test is proposed as a fast and effective method for the GaN HEMTs screening for the high-f_{sw} overvoltage ruggedness. These results reveal the necessity of running application-based robustness test beyond single-event or DC static tests for the qualification of GaN HEMTs.

4. Based on the findings in the HFOT test, a lifetime model based on the shift of GaN HEMT's dynamic R_{ON} is established. A high frequency UIS test setup with accurate in-situ R_{ON} monitoring is demonstrated. Good agreement between the measured data and the lifetime model fits are achieved under different peak switching voltages, which reveals the electron trapping in the passivation layer interface to be the main physical origin of device degradation.

1.5.2 Avalanche and Short-circuit Robustness of Vertical GaN Fin-JFET

1. A unique "avalanche through fin-channel" phenomena is observed in the vertical GaN Fin-JFET. With the implementation of an RC interface gate driving circuit, the channel can be turned on during the avalanche, which migrates the avalanche current from the gate p-n junction to the device fin-channel. In comparison with the avalanche in the p-n junction

(avalanche through gate), the avalanche through fin-channel offers higher E_{AVA}, and features a failure-to-open-circuit signature. This avalanche path also allows for the spatial separation of the high current stress and the peak E-field, resulting in a more robust avalanche capability in power devices.

2. From the single-event short circuit test, a record high t_{SC} of 30.5 µs at an input voltage of 400 V is measured for a 650-V rated Fin-JFET. All devices show the failure-to-open signature where the device maintains the avalanche breakdown voltage (BV_{AVA}) after failure. Meanwhile, the vertical GaN Fin-JFET is the first power device that demonstrates robust short circuit capability near the BV_{AVA} with t_{SC} over 10 µs. The physics behind these results is well explained by the avalanche-through-fin process.
3. Repetitive avalanche and short circuit testing show similar degradation at the lateral gate-to-source junction, providing guidance for further enhancing the robustness of GaN Fin-JFETs.

1.6 Dissertation Outline

Chapter 1introduces the background of the study, the key differences between GaN-based power devices and Si or SiC-based power devices, and the open knowledge gaps in GaN power device robustness study.

The key contents of chapter 2 to chapter 5 can be summarized in the device SOA figure (Figure 1-2) which is shown in Figure 1-7.

Chapter 2 discusses the surge energy robustness based on the single-event UIS test. This chapter presents a combination of switching circuit testing, microscopic failure analysis, and technology computer aided design (TCAD) simulation. This chapter focuses on device *BV*, i.e. the hard failure boundaries of GaN HEMTs. The findings in this chapter also set the knowledge base for Chapter 3.

Chapter 3 covers the HFOT on commercial p-gate GaN HEMTs. The dynamic *BV* of GaN HEMT presented in chapter 2 indicates the single-event test may not reveal the device's true *BV* in high frequency switching applications. This chapter introduces the test circuit design, test results, degradation analysis, and the implementation of high frequency screening test. Finally, the

lifetime projection model based on the findings in the high frequency test is validated by experimental results. The focuses in this chapter include device *BV* and the lifetime at lower switching voltage.

Chapter 4 and Chapter 5 discuss the robustness of vertical GaN Fin-JEFT. Chapter 4 covers the avalanche robustness, including the avalanche-through-fin phenomena, the single-event avalanche energy, and the degradation mechanism in repetitive testing. Chapter 5 presents the short circuit test results, including the measurement of t_{SC} at various input voltage, and the degradation mechanisms under repetitive short circuit tests.

Chapter 6 provides a summary of this dissertation and establishes a foundation for future research topics on the robustness of GaN power devices.

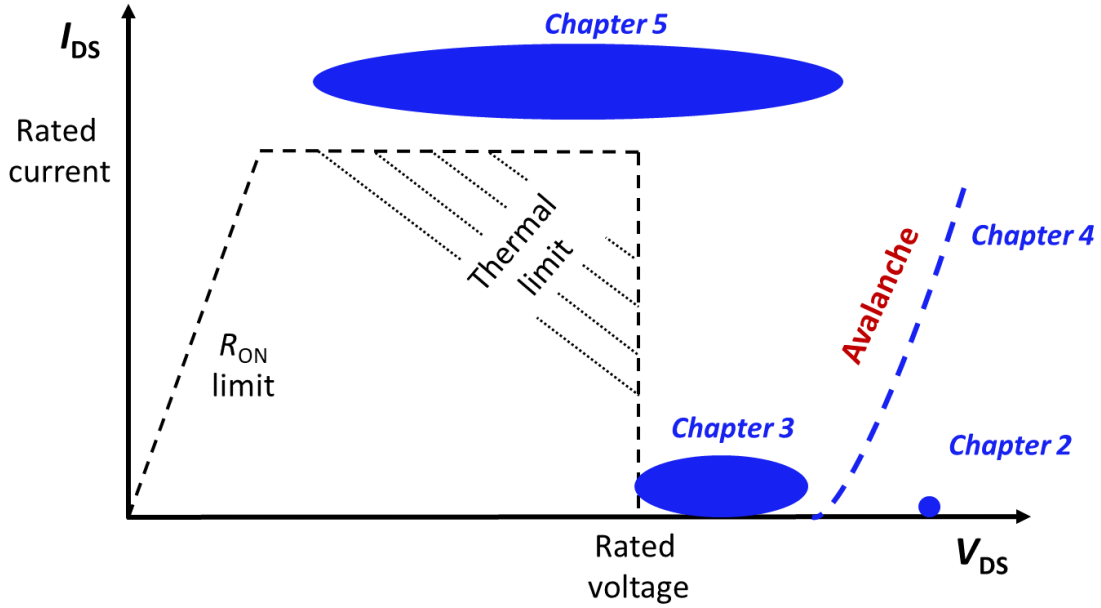


Figure 1-7. Summary of the main content of different chapters with respect to the device SOA.

Chapter 2: Surge energy and Overvoltage Robustness of GaN HEMT Under Single-event Transient

2.1 Introduction of Unclamped Inductive Switching (UIS) Test

Power device surge energy robustness is usually characterized by the UIS test. Figure 2-1illustrates the UIS circuit schematic. It consists of the device under test (DUT) and a loop inductor (L_{loop}) connected in series. The UIS test procedure is described below: the DUT is first turned on with a positive gate bias (V_{GS}) to charge the inductor. Once the inductor current reaches the desired value, the DUT is turned off and the inductor energy is forced to be withstood by the off-state DUT. Such a UIS test has been widely adopted to characterize the avalanche energy of Si/SiC MOSFETs or Si IGBTs [65]–[68], meanwhile, it is also suitable for exploring the surge energy robustness of non-avalanche devices thanks to its simple circuit topology and setup, versality in tuning the *dv/dt* and pulse width. In fact, after the publication of our work in early 2020 [69], vast efforts have been put into the GaN HEMT overvoltage robustness study [57]–[60], [70], and the UIS test has become very popular for the BV_{DYN} characterization in various non-avalanche device technologies, e.g., various types of industrial GaN HEMTs [71]–[73] emerging GaN diodes and HEMTs [74], [75], [76] as well as for different applications, e.g., high and cryogenic temperature tests [73], [77] and on-wafer breakdown test [76] [78]. In this chapter, based

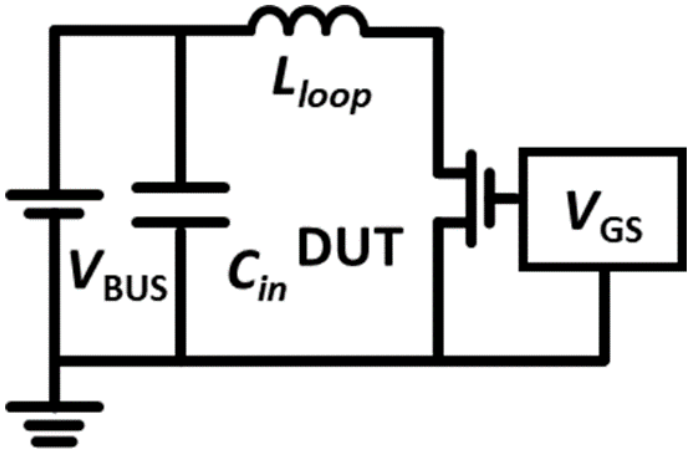


Figure 2-1. Circuit schematic of the UIS test.

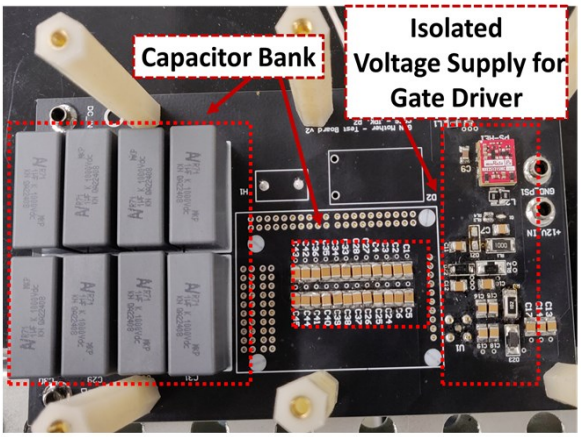
on the UIS test, the GaN HEMTs safe withstanding process, the failure boundaries, and failure mechanisms under the surge energy event are discussed.

2.2 Single-event UIS Test Results

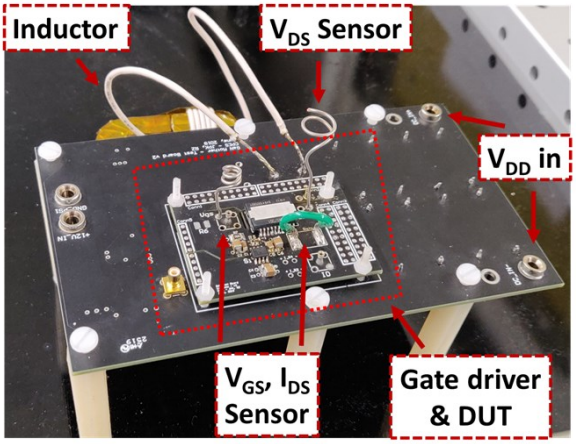
2.2.1 Device Under Test and UIS Test setup

The devices under test (DUT) in this section are the commercially available 600 V, 31 A HD-GIT from Infineon [79] and 650 V, 30 A SP-HEMTs from GaN Systems [80]. The features of these two types of p-gate GaN HEMTs have been discussed in Chapter 1.

Figure 2-2 shows the experimental UIS test hardware. The test setup comprises a motherboard with main power loops and two daughter boards each to accommodate the packaging and gate



(a)



(b)

Figure 2-2. Photos of (a) the motherboard and (b) a daughter board of the UIS test hardware.

driving circuit for each type of the DUT. The motherboard includes the primary power switching loop and isolated, auxiliary power supply for the gate driver circuitry. Because the gate-source loop layout is critical for proper GaN device operation, the daughter board includes an optimized gate loop with small parasitic inductance for each packaging type. Sensing circuitry to measure the gate bias (V_{GS}), drain bias (V_{DS}), and drain current (I_{DS}) is also implemented upon each daughter board. Regarding the gate driving circuit, the topology and components parameters follow the guidelines in the datasheet and application note of each DUT [81], a commercial Si8271GB-IS gate driver is used for both HD-GIT and SP-HEMT. During DUT switching, the on-state V_{GS} is 5 V for SP-HEMT, and around 3.5 V for HD-GIT as the hole injection through the gate p-n junction clamps the V_{GS}. The off-state V_{GS} is kept at -5 V for both DUTs. The input voltage (V_{IN}) of the UIS test in this section is set as 30 V.

2.2.2 Surge Energy Withstanding Process

Figure 2-3 show the typical UIS waveforms in the safe withstand situation for HD-GITs and SP-HEMTs. The two types of devices show very similar withstand waveforms. The peak transient overvoltage is higher than the DUT rated voltage, suggesting that a good overvoltage margin is built in both devices. Four distinct phases have been identified in the UIS safe withstanding waveforms:

(a) *Phase I*, inductor charging: the DUT is turned on, inductor is charged by V_{IN} until the current reaches the desired values.

(b) *Phase II*, turn-off transient: the DUT turns off, and V_{DS} exceeds V_{IN}. Due to the turn-off loss and gate-loop parasitic, I_{DS} drops.

(c) *Phase III*, overvoltage transient: a *LC*-like resonance is produced between the load inductor (L) and the device output capacitance (C_{OSS}). The peak positive I_{DS} at the start of resonance (e.g., ~1.5 A in Figure 2-3(a), ~2 A in Figure 2-3(b)) is almost identical to the maximum negative current after a half cycle of resonance (e.g., -1.5 A in Figure 2-3(a), -2 A in Figure 2-3(b)). This suggests the same amount of inductive energy and almost no energy dissipated within the DUT. Note that a nonideal loss of the device due to the device dynamic C_{OSS} may occur during this resonance stage, which has been analyzed in detail in . Different from the avalanche waveform in power MOSFETs as illustrated in Figure 1-4(b), in the UIS waveform of GaN HEMTs, I_{DS} is zero at the peak V_{DS} transient, and V_{DS} does not clamp at its peak value. This validates that there is no

avalanching occurred inside the DUT during the withstand process. In contrary to the positive I_{DS} in avalanche waveforms, I_{DS} show negative values in the waveforms of GaN HEMTs. These waveform features suggest a resonant transfer of energy between the device capacitance and the load inductor rather than a resistive energy dissipation as occurs in avalanche. In other words, GaN HEMTs 'withstand' the surge energy but do not 'dissipate' it. A further evidence for the resonance is that, the C_{OSS} calculated from the measured resonance period, $T = 2\pi\sqrt{LC_{OSS}}$, is very close to the DUT's energy related C_{OSS} in the datasheet.

(d) *Phase IV*, reverse conduction: when V_{DS} resonates to negative values and exceeds the DUT's reverse turn-on voltage (V_F^{3rd}), the DUT conducts in the third quadrant (3rd-quad), and the

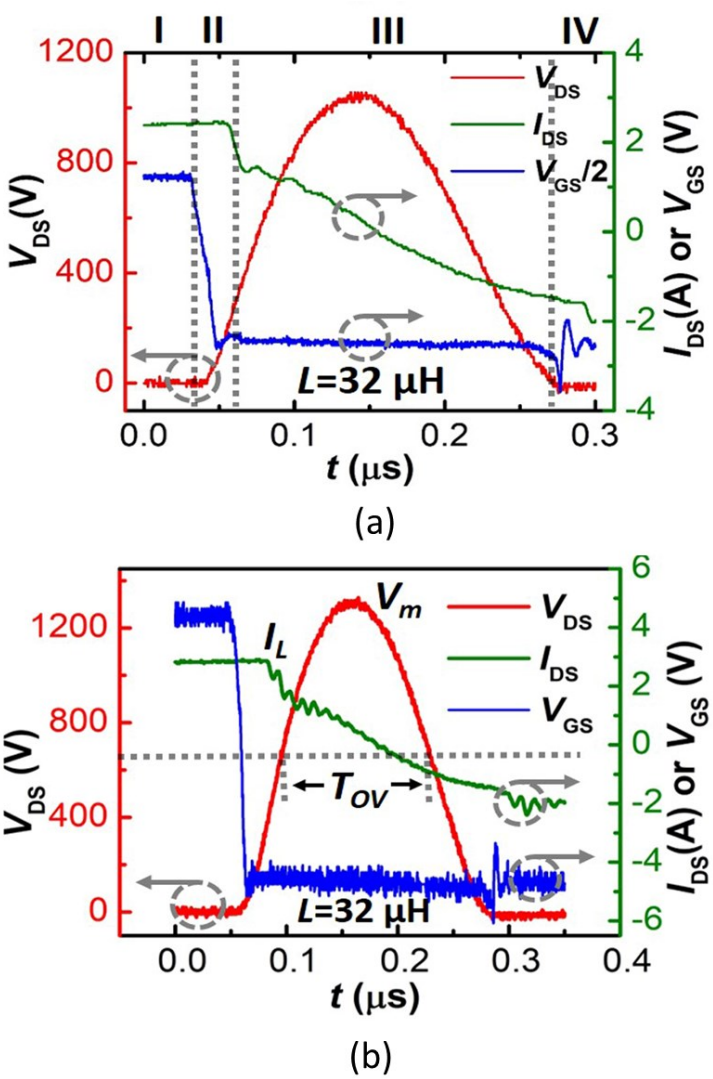


Figure 2-3. UIS safe withstand waveforms of the (a) GaN HD-GIT and (b) SP-HEMT with a loop inductor value of 32 µH

LC-resonance stops. V_{DS} is then clamped around its 3rd-quad voltage drop. The clamped voltage extracted from the UIS waveforms is about -8 V, which is consistent with the 3rd-quad voltage drop at V_{GS} of -5 V from the DUT datasheet. Once the DUT turns on reversely, the positive V_{IN} applies on inductor and the inductor is discharged by the power supply.

2.2.3 GaN HEMTs Failure Boundaries in UIS Tests

The DUT failure in the UIS tests is then studied by gradually increasing the inductor current (I_L) at the end of *Phase I* until the DUT fails in the UIS tests. As shown in Figure 2-4, the peak transient V_{DS} in the UIS waveform, which is defined as V_M, is found to be well fitted by the resonance relation $V_m = I_L\sqrt{L/C}$ for different load inductors. The slight discrepancy in the fitting at higher I_L is due to the turn-off loss in *Phase II*, the core loss from the inductor, and the parasitic impedance in the switching circuit. The DUT failures under different load inductances occurred at an almost identical V_M boundary.

Figure 2-5(a) and (b) show the typical failure waveform of the HD-GIT and the SP-HEMT, respectively. In both types of devices, the failure occurs near the transient of peak resonant voltage. The HD-GIT fails at a transient overvoltage of 1150~1200 V and the SP-HEMT fails at 1400~1450 V, showing that these devices are built with considerable overvoltage capability compared to their rated voltages. The failure modes exhibited in these two DUTs are slightly different. In the GIT, a small collapse in V_{DS} is shown after the device failure, indicating the creation of a leakage path.

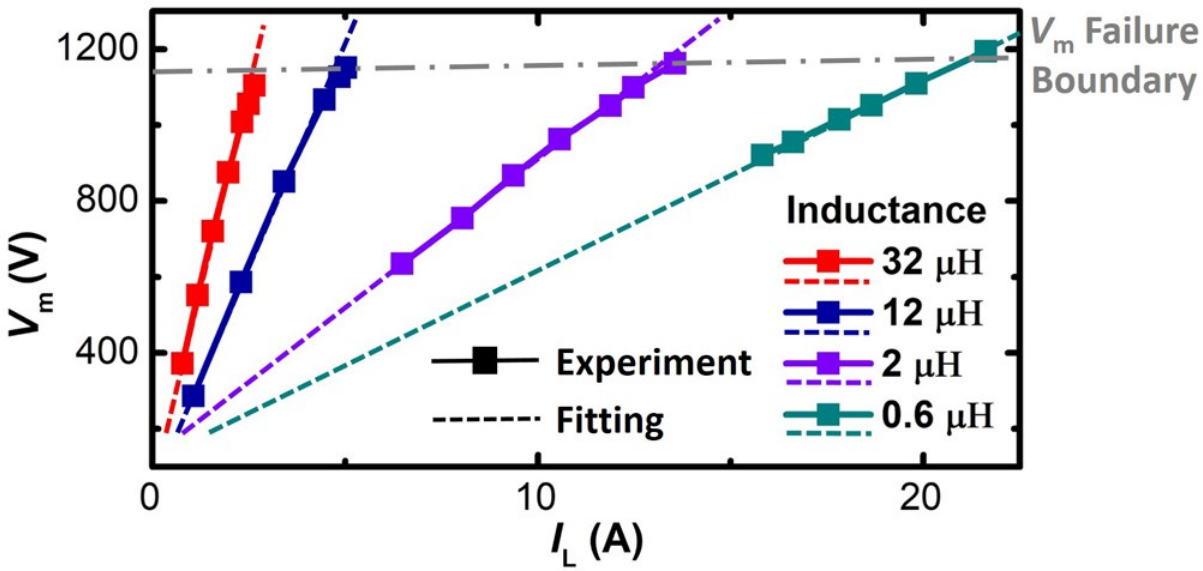


Figure 2-4. Dependence of V_m on I_L extracted from the UIS tests with various inductors.

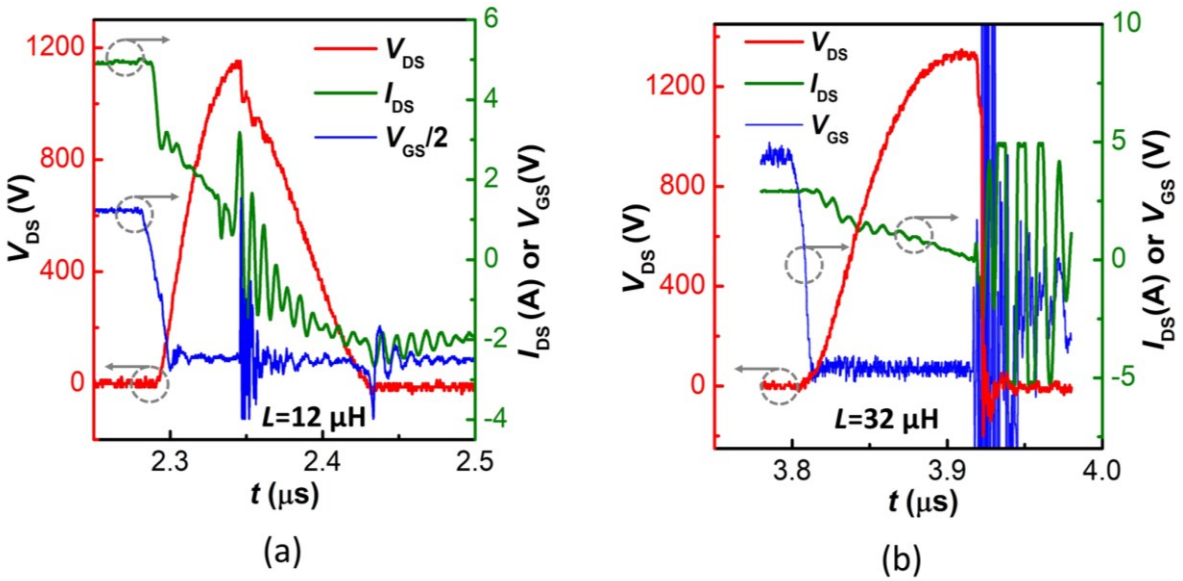


Figure 2-5. Failure waveforms of the (a) GaN HD-GIT and (b) SP-HEMT

However, the resonance continues and the V_F^{3rd} is also stable, indicating the gate control over I_{DS} retains. In the SP-HEMT, the gate control is lost right after the device failure; the source and drain are short. The different waveforms after the DUT failure implies different failure locations in the HD-GIT and SP-HEMT, which will be analyzed in detail in Section 2.2.4.

To further study if the DUT failure is dominated by the transient overvoltage, or also dependent on the voltage ramp rate (*dv/dt*) and the total duration of overvoltage, the DUT failure under different inductors is studied. From the resonance relations, a change in inductance results in different resonance periods, *dv/dt*, and overvoltage durations. Here the overvoltage duration (T_{ov}) is defined to be the time when V_{DS} is higher than the rated voltage during the *LC*-resonance, as illustrated in Figure 2-6. The smallest inductor value (600 nH) is selected to allow for a *dv/dt* of ~120 V/ns, which is comparable to the highest switching speed of GaN transistors demonstrated in the state-of-the-art converters [82]. The largest inductor value (32 μH) is selected to be over 50-fold higher than the smallest one, which produces a *dv/dt* of ~10 V/ns. For each inductor, the failure of HD-GITs and SP-HEMTs is found to consistently occur at the peak overvoltage transient. Three DUTs are tested to failure for each inductor for validation. The DUT's V_M values versus different T_{ov} are shown in Figure 2-6, when T_{ov} increases from ~ 5 ns to 60 ns, the failure boundary of V_M shows little dependence on T_{ov} for both HD-GITs and SP-HEMTs. This suggests that the GaN HEMT failure under surge energy is mainly limited by its overvoltage capability or the transient breakdown voltage (*BV*). However, a slightly decreasing trend can be found in Figure 2-6, and this

trend is more pronounced in the SP-HEMT. In section 2.3, GaN HEMTs BV dependence on T_{ov} will be studied with a further expansion of T_{ov} from nanosecond to second range.

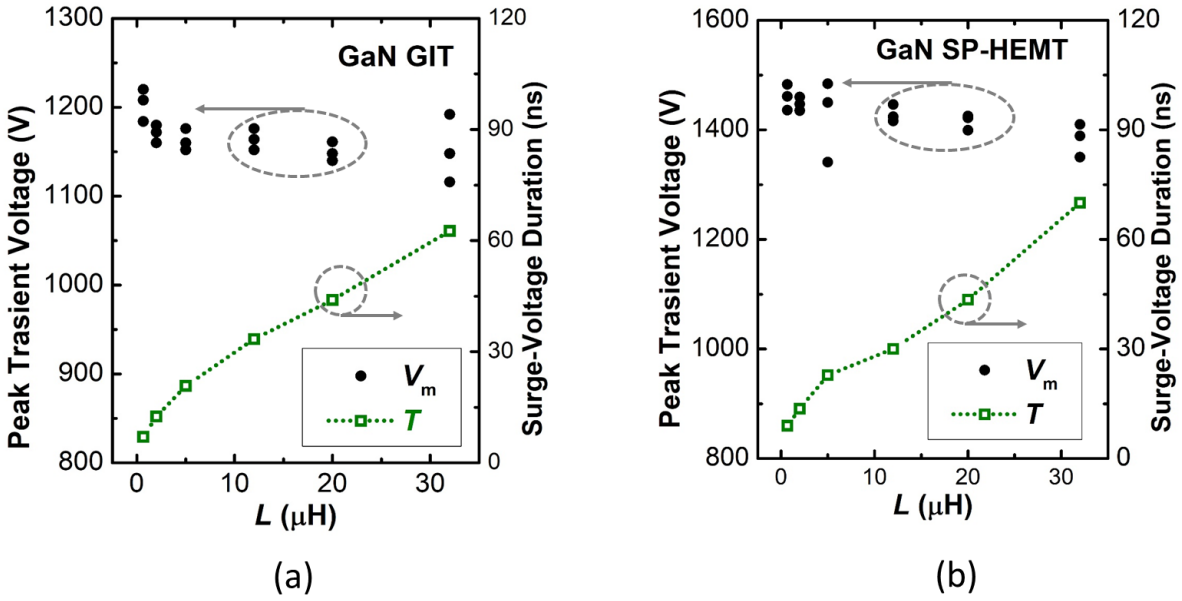


Figure 2-6. The transient peak overvoltage that leads to device failure and the overvoltage duration as a function of inductor values, for the (c) GaN HD-GIT and (d) SP-HEMT.

2.2.4 Failure Analysis and TCAD Simulations

Comprehensive failure analysis is performed to thoroughly understand the failure mechanisms of HD-GITs and SP-HEMTs in the UIS tests. Packages of the failed devices are de-capsulated. Electric measurements of the de-capped device are first performed using a probe station. Microscopic imaging tools such as scanning electron microscopy (SEM) and focused ion beam (FIB) are then used to image the failure spots. Based on the device geometry revealed in the microscopic imaging, physics-based device simulation stacks are built and then combined with a UIS circuit arrangement for mixed-mode simulation. This mixed-mode simulation enables to validate our theoretical explanations of the UIS waveforms in Section 2.2.2, and to extract the distribution of electric field (E-field) within the device structure at any switching transient.

A. HD-GITs

Figure 2-7(a) illustrates the package structure of the HD-GIT, the Si substrate of GaN HEMT is connected to the heat slug by solder and electrically connected with the source pad by a wire bond. Figure 2-7(b) shows the transfer I_{DS}-V_{GS} characteristics of a brand-new and a failed HD-GIT, illustrating the gate retains the control over the 2DEG channel in the failed device in the UIS

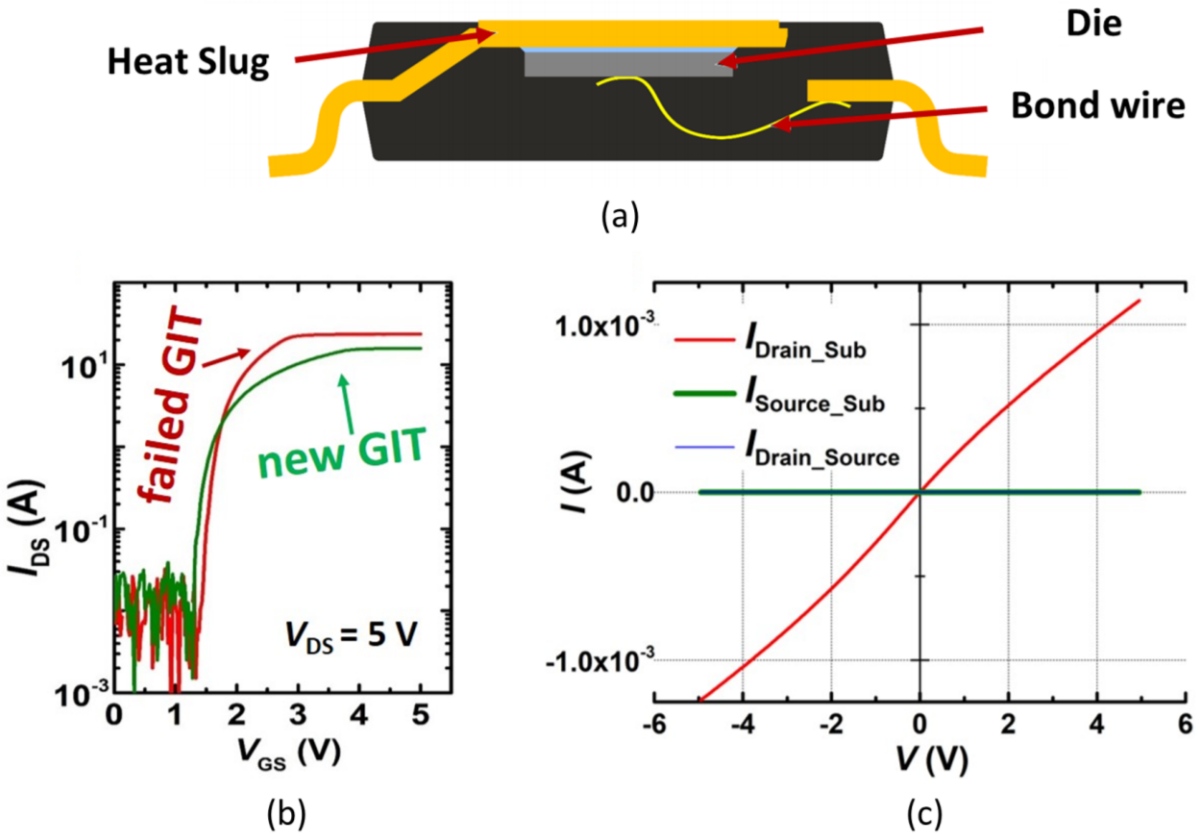


Figure 2-7. (a) Illustration of the packaging structure of the HD-GIT (b) Transfer characteristics of a failed HD-GIT and a new one. (c) Leakage current measured between the source, drain, and substrate of a failed HD-GIT after the de-capsulation and the removal of the wire between source and substrate.

test. With the gate floating, the drain-to-source resistance is measured as below 1000 Ω, indicating the creation of leakage paths between drain and source. After removing the wire bonds connecting source and substrate in the original de-capped device, the leakage current paths between lateral drain to source and vertical drain to substrate are separated. Figure 2-7(c) shows the *I-V* characteristics between source, substrate, and drain. A large drain-to-substrate leakage current is presented, the drain-to-source and source-to-substrate leakage currents are minimal, suggesting the damage possibly locates at the drain and penetrates to substrate, i.e., a vertical failure.

No burning or melting traces are observed at the optical microscopic scale on the chip surface after de-capsulation (Figure 2-8(a)), confirming that the major failure mechanism is not thermally related, and failure occurred in the semiconductor rather than the packaging. Emission microscopy (EMMI) analysis is used to locate the failure spots, the emission (failure spot) is observed at the drain finger (Figure 2-8(b)), followed by SEM inspection with FIB. Figure 2-8(c) shows the cross-sectional SEM image of the device channel region at the failure spot, revealing that failure occurred

in the drain region and the drain-connected p-GaN. The gate region maintains intact, which explains the functional gate control shown in Figure 2-7(a). A percolation leakage path through

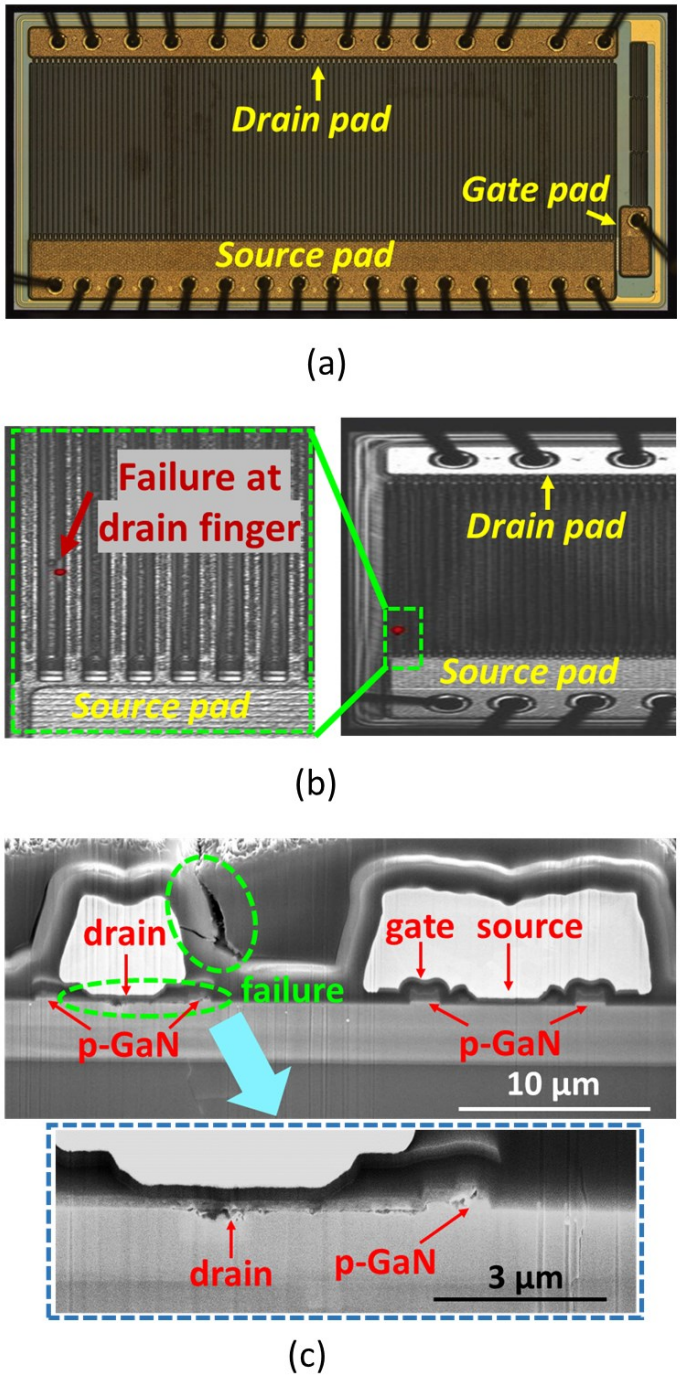


Figure 2-8. (a) Photo of the chip surface after de-capsulation under the optical microscope. (b) EMMI analysis results of the de-capsulated failed device (c) Cross-sectional SEM image of the device channel region at the failure spot, showing damages in the drain region and the drain-connected p-GaN.

defect states, which are difficult to observe under SEM, may form from the damaged drain region to the Si substrate, which accounts for the leakage path revealed from Figure 2-7(b).

A physics-based TCAD mixed-mode simulation in Silvaco Atlas is performed for the HD-GIT. The physical models for device simulation are based on the ones described in [83] and [84], and the static simulation is calibrated with the device datasheet. Acceptor-like traps are added into the GaN buffer layer in the simulation based on the experimental reports on GaN-on-Si devices [85], [86], the implementation of the traps is critical for the convergence of the simulation. The implementation of device-circuit mixed-mode TCAD simulation is similar to some previous work [87], [88]. The complete TCAD codes for the GaN HEMT mixed-mode UIS simulation can be found in Appendix A: GaN HEMT UIS Mixed-mode TCAD Simulation Script for Silvaco.

Figure 2-9(a) shows the calibration of the mixed-mode simulation. The simulated waveform with an inductor of 12 μH and a V_M of ~1 kV agrees well with the experimental test waveforms.

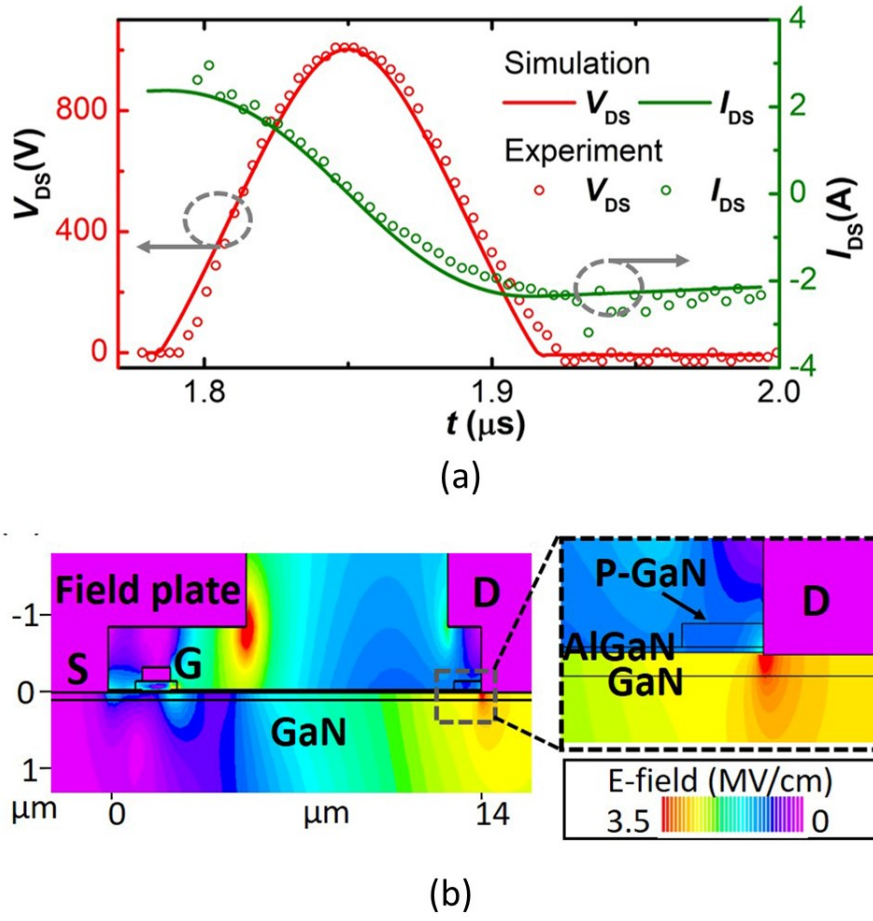


Figure 2-9. Comparison between the simulated and experimental UIS waveform. (b) Simulated electric field distribution in the HD-GIT unit-cell at the peak overvoltage (1150 V) transient and a zoom-in at the drain region.

This further validates the *LC*-resonance and 3rd-quad conduction as explained in Section 2.2.1. Figure 2-9(b) shows the simulated E-field distribution in the HD-GIT at a peak transient voltage of 1150 V. The peak E-field in GaN is found to be located at the drain edge, with a value of ~3.4 MV/cm, which is close to the critical E-field of GaN. The simulated peak E-field in dielectrics close to the edge of the source field plate (FP) is ~4.5 MV/cm, which is below the critical E-field of SiN_x or SiO_2 (~10 MV/cm [89]), the commonly-used dielectric materials for passivation of GaN devices. The agreement between the simulated peak E-field location and the failure location in the DUT suggests that the DUT failure under surge energy is induced by the high E-field at the peak overvoltage transient. This agrees well with the withstand process where almost no heat is dissipated in device, as explained in Section 2.2.2.

B. SP-HEMTs

Different from the failed HD-GITs, the SP-HEMTs are found to fail short between source, gate, and drain, as revealed from electrical measurements. The loss of gate control and a short between source and drain explain the UIS failure waveforms shown in Figure 2-5(b). No obvious burning traces are observed on the chip surface under the optical microscope, suggesting the failure is dominated by E-field rather than heat as well.

Figure 2-10(a) and (b) shows the cross-sectional SEM images of a unit-cell of the fresh SP-HEMT and the failed SP-HEMT, respectively. The SP-HEMT unit-cell includes four main FPs: a large size source connected FP, a drain connected FP, and two source connected FPs that covers the gate region (referring to the gate FP). The failure spots are found to locate at both the gate FP region and the drain region, and the failure structures are more complicated than the ones in HD-GITs. In the drain contact region, damage is observed in GaN and cracks are shown in the drain FP. In the gate floating FP region, cracks are shown around the two floating FPs. These damages and cracks can be attributed to local E-field crowding in GaN or FP dielectrics. The cracks may be generated due to the mechanical exfoliations after initial E-field failure in the FP dielectrics. In addition to cracks, the molten metal is observed at the interconnect on top of drain, producing a void in metal. This is attributed to the heat generated after the initial electrical failure at the overvoltage transient, as the SP-HEMT is failed short between source and drain at high voltage.

Figure 2-10(c) shows the simulated E-field distribution in the SP-HEMT at the transient of peak overvoltage of 1450 V. The peak E-field in GaN locates at the drain region and the peak E-

field in dielectrics at the edge of floating FPs in the gate region, the source FP, and the drain FP. The peak E-field in GaN is believed to account for the failure in the drain region while the peak E-field in dielectrics could account for the gate failure. The complex multi-layer FP structures in the gate region of SP-HEMTs may exacerbate the device vulnerability to mechanical failure in the gate FP region when compared to HD-GITs. The E-field induced dielectric fatigue or failure is

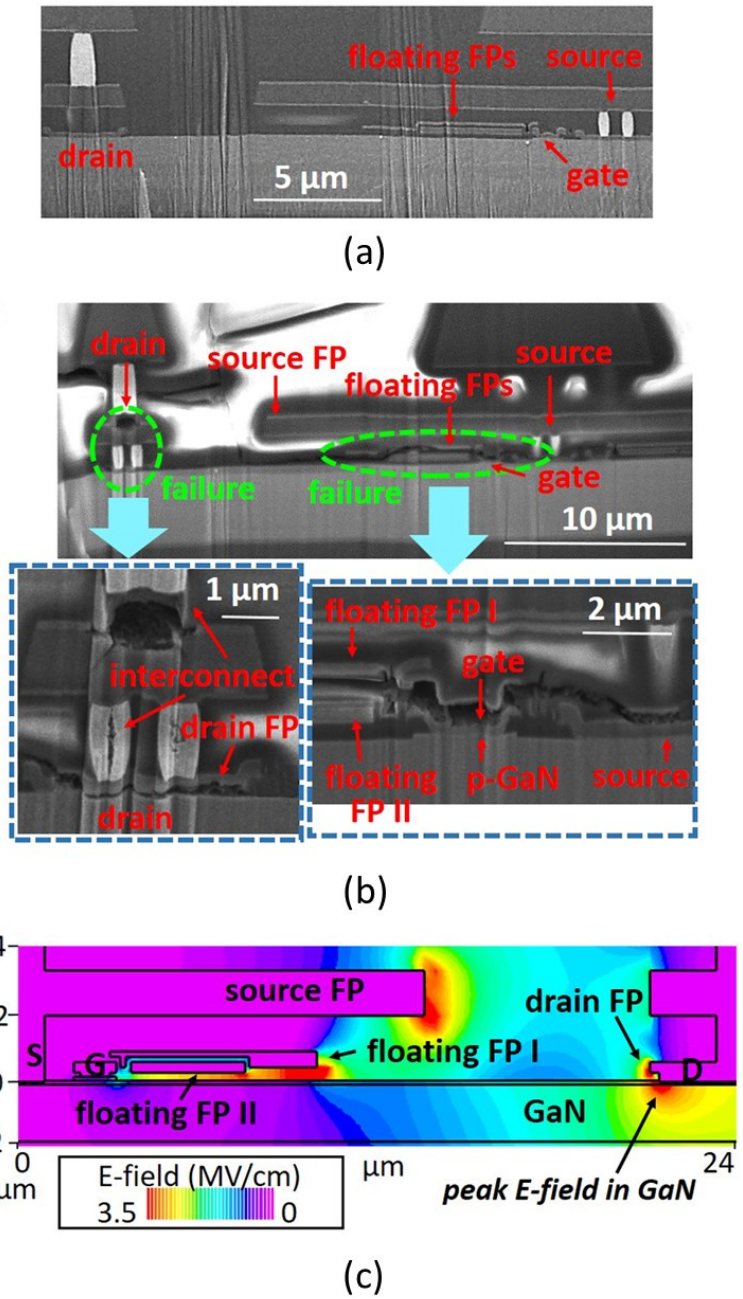


Figure 2-10. Cross-sectional SEM image of a unit-cell of (a) the fresh SP-HEMT and (b) the failed SP-HEMT, showing damages in both the drain region and the gate region of the failed device. (c) Simulated E-field distribution in the SP-HEMT at a transient overvoltage of 1450 V.

likely to further induce mechanical failures (e.g., cracks) in the complex FP structures consisting of multiple layers of thin dielectrics and metals with small patterns.

From the failure analysis and mixed-simulation presented in this section, it is clear that the initial device failure at the transient peak overvoltage is mainly induced by E-field, and the failure spots are consistent with the peak E-field locations in the device. The failure behaviors of GaN HEMTs are fundamentally different from the failure of SiC/SiC MOSFETs in avalanche, which is usually induced by thermal runaway and burning traces are shown in the failed DUT in avalanche [90].

2.2.5 Comparison with Avalanche Breakdown Devices

Figure 2-11 illustrates the typical surge-energy withstanding waveforms of the GaN HEMT and the Si/SiC MOSFET. The difference originates from the lack of avalanche capability in GaN HEMTs. Table 2-1 summarizes the key differences in withstand dynamics, failure mechanisms, and failure determining factors for GaN HEMTs compared to Si/SiC MOSFETs. The GaN HEMT withstands the surge energy without the avalanche capability to dissipate it; as a result, minimal heat is generated in the withstand process, suggesting thermal runaway is not a major mechanism

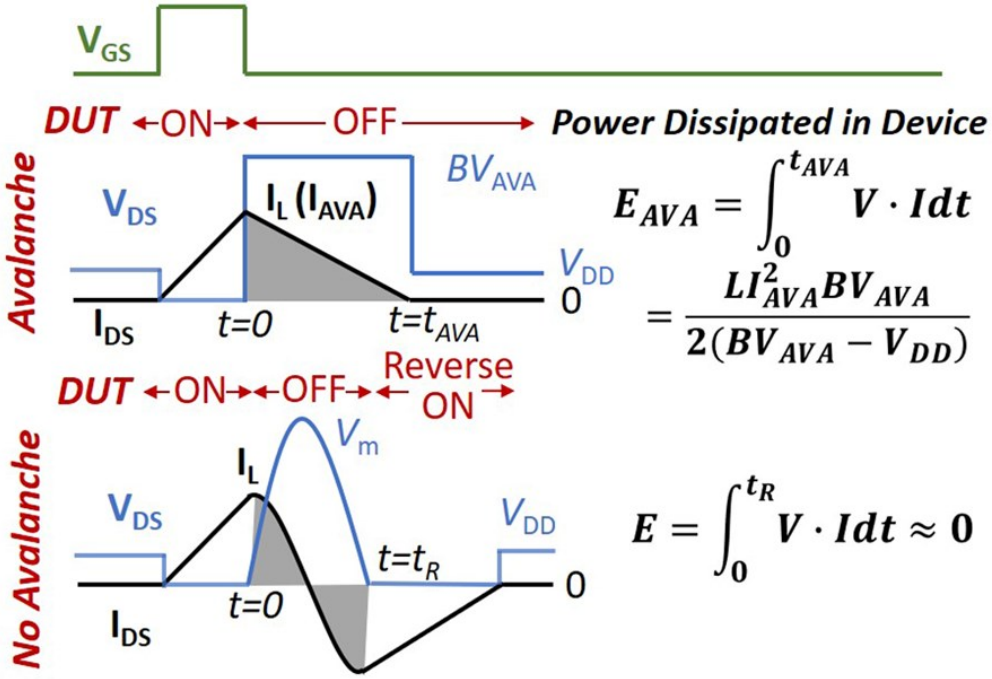


Figure 2-11. Schematic illustration of the UIS waveforms for a power transistor with and without avalanche capabilities as well as the resistive power dissipation in device during the surge-energy withstand process.

for device failure. Instead, the device failure is limited by the peak overvoltage, which can be correlated with the surge energy in inductor (E_L)

$$V_m = I_L\sqrt{L/C} = \sqrt{\frac{2E_L}{C_{OSS}}} \qquad (2-1)$$

(2-1) suggests that the surge energy (or an equivalent 'avalanche' energy) is no longer a parameter that can directly represent the intrinsic ruggedness of GaN HEMTs. While E_{AVA} represents an intrinsic and thermal-related device capability, the failure of GaN HEMTs under E_L not only depends on device capacitance and overvoltage margin, but also depends on parasitic capacitances and inductances of the switching circuit. Some prior literatures compared the surge energy that GaN HEMTs can withstand (E_{surge}^{max}) to the E_{AVA} of Si/SiC MOSFETs. However, this comparison is not physically meaningful, due to the entirely different withstand dynamics and failure mechanism of GaN HEMTs. An E_L identical to E_{AVA} does not necessarily imply the same device ruggedness.

If assuming negligible loop inductance and parasitic capacitance, E_{surge}^{max} can be correlated to the device parameters of GaN HEMTs based on (2-1):

$$E_{surge}^{max} = \frac{1}{2} C_{OSS} BV^2 \qquad (2-2)$$

Table 2-1. Comparison between the surge energy withstanding process and failure mechanisms of power Si/SiC MOSFETs and GaN HEMTs.

	Si/SiC MOSFET	GaN HEMT
Withstand process	avalanching	L-C resonance and reverse conduction
Energy path	resistive dissipation in device through avalanche	little/no dissipation in off-state withstand; dissipation in reverse conduction
Limiting factor	avalanche energy	overvoltage capability
Failure mechanism	thermal run-away	E-field induced breakdown

BV is the device transient breakdown voltage. Two implications can be deduced from (2): (a) for the same device technology (e.g., the devices from the same manufacturer with the same BV), the devices with higher current rating expect a larger E_{surge}^{max}, due to larger die size and therefore larger C_{OSS}; (b) for the devices from different manufactures, the devices with higher overvoltage margin typically expect a higher E_{surge}^{max}. This is not only due to higher BV, but also a higher C_{OSS}, as BV is usually increased by scaling up the drain-to-gate distance, which leads to an increased C_{OSS}. This implies a fundamental trade-off between the switching performance of GaN HEMTs and their surge-energy ruggedness. A higher voltage margin (and usually higher C_{OSS}) may slow down the device switching, at least for hard switching, but could enable a higher E_{surge}^{max}.

A final point worth mentioning is that for Si/SiC MOSFETs, the intrinsic E_{AVA} would generate a failure boundary comprising the avalanche current (I_{AVA}) and the total avalanche time (t_{AVA}) (I_{AVA} and t_{AVA} shown in Figure 2-11). This failure boundary is routinely measured in the industrial UIS test as it provides useful information for power electronics applications. Some of the UIS tests for GaN HEMTs plotted a 'boundary' between I_L and the resonant withstand time duration (t_R in Figure 2-11), with the aim to correlate the failure to avalanche. However, in this dissertation, it is pointed out that the plot between I_L and t_R does not reflect any intrinsic failure boundary for GaN HEMTs, as their failure is dominated only by the overvoltage. This plot would provide indirect and even misleading information to device users. The transient overvoltage margin and device capacitance are more relevant to the surge ruggedness of GaN HEMTs.

2.3 Dynamic Breakdown Voltage of GaN HEMTs

2.3.1 Introduction of UIS Test Setup with Tunable Pulse Width

While the content in the previous section has shown that the UIS test is a suitable tool to characterize GaN HEMT overvoltage robustness, and provide critical understandings for the qualifications and applications of E-mode GaN HEMTs, the UIS setup presented in section 2.2 involves a limited variation in the pulse width of the transient voltage overshoot: by only varying the inductor value from 600 nH to 32 μH in the circuit, the overvoltage duration, T_{ov} is only changing in the range of tens or hundreds of nanoseconds. In application scenario, when UIS occurs, the pulse width could vary from nanosecond range such as the voltage overshoot triggered

by parasitic or leakage inductance [91]–[93], to several milliseconds or even longer such as the UIS between device and large motor coil [65]. Therefore, a testbed with flexibility of changing resonance pulse with a wide range is needed.

Figure 2-12 shows the circuit schematic of the various pulse width UIS test. Compared to the normal UIS test, an additional capacitor C_{ADD} is put in parallel with the DUT. Compared to using a large inductor, which occupies a large volume and takes long time to build, an additional capacitor is much smaller in size and allows a further increase of the pulse width as well.

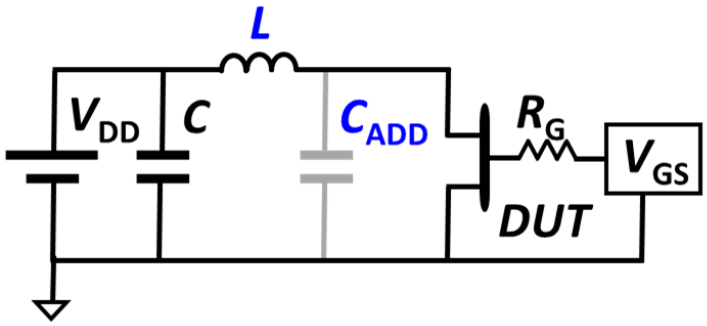
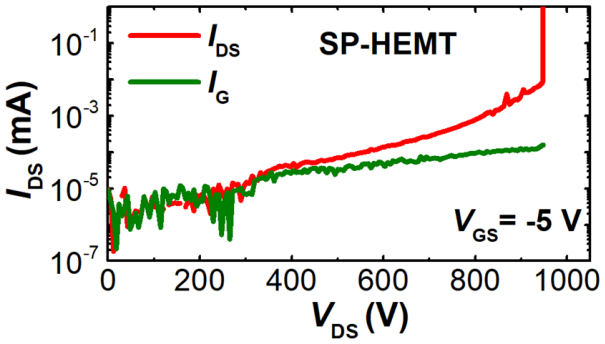


Figure 2-12. Circuit schematic of the UIS test with various pulse widths.

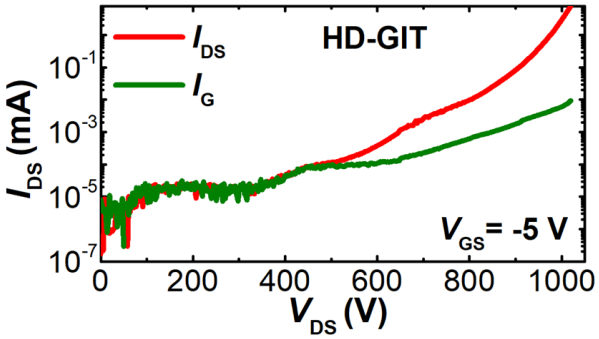
2.3.2 Dynamic Breakdown Voltage and Physical Explanations

The same commercial p-gate GaN HEMTs as the ones used in section 2.2 are tested in this section, i.e. the 650 V, 30 A rated SP-HEMT from GaN Systems [80] and the 600 V, 31 A rated HD-GIT from Infineon [79]. The DUT static *BV* is first obtained via the quasi-static I-V sweep on a curve tracer, which reveals a 950 V destructive *BV* in the SP-HEMT (Figure 2-14(a)). The HD-GIT's leakage current reaches the current compliance (8 mA) of the curve tracer at V_{DS} of 1000 V without the DUT catastrophic failure (Figure 2-14(b)).

Similar hardware configuration comprising a motherboard with the main power loops and two daughter boards to accommodate the package and gate driving circuitry for each type of the DUT is used (Figure 2-13). The voltage measurements are taken right at each terminal pad of the DUT for a better signal accuracy. A power resistor is mounted on the daughter board to enable high temperature measurements, while the temperature is raised by an external power supply and calibrated by thermal imaging and thermocouple. A Si8271GB-IS gate driver is used to provide ±5 V on/off V_{GS} (again, the V_{GS} is clamped around 3.5 V in HD-GIT). The modulation of the pulse



(a)



(b)

Figure 2-14. Quasi-static off-state I-V curves of the (a) SP-HEMT and (b) HD-GIT

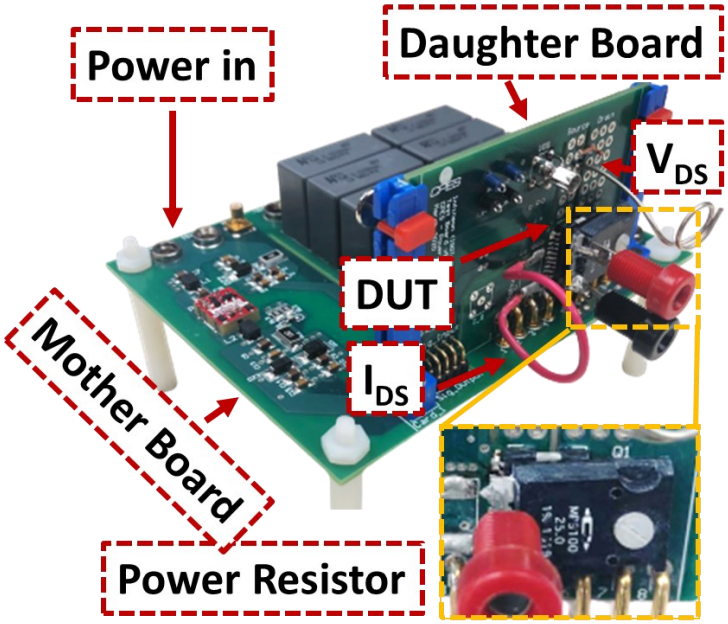


Figure 2-13. Photo of the test setup.

width is realized by using various inductors from 600 nH to 81 mH, as well as paralleling a capacitor (0 to 10 µF) across the DUT's drain and source.

To measure the transient *BV*, the inductor current is gradually increased in the UIS pulse to produce a 10 V step increase in the peak V_{DS}. After each pulse, the DUT rests for 5 minutes to allow sufficient de-trapping. Six DUTs are tested to failure under each condition to validate the statistical significance.

A. Dynamic BV of SP-HEMTs

Figure 2-15 shows the safe-withstand waveform and the failure waveform of the SP-HEMT at 600 nH *L*. The pulse width is 25 ns, producing an average *dv/dt* of 120 V/ns. I_{DS} drops from 24 A to 12 A after DUT turn-off mainly due to device switching loss, followed by a *LC*-resonance. Since an air core inductor is used in this measurement, minimal core loss is involved. The capacitive I_{DS} at the start of resonance almost equals to the negative I_{DS} (~ -12 A) after a half cycle of resonance, suggesting minimal resistive energy dissipation (and self-heating) within the DUT. The resonance suspends after a half cycle, as the negative V_{DS} turns on the DUT reversely. The DUT failure occurs at the transient of peak V_{DS}. At a pulse width of 25 ns, while increasing the temperature from 25 °C to 125 °C, the safe-withstand UIS waveforms shows no change in shape (Figure 2-17(a)) while the peak V_{DS} at the failure transients are found to be almost independent of temperature (Figure 2-17(b)), confirming that the DUT breakdown is E-field induced rather than thermal limited.

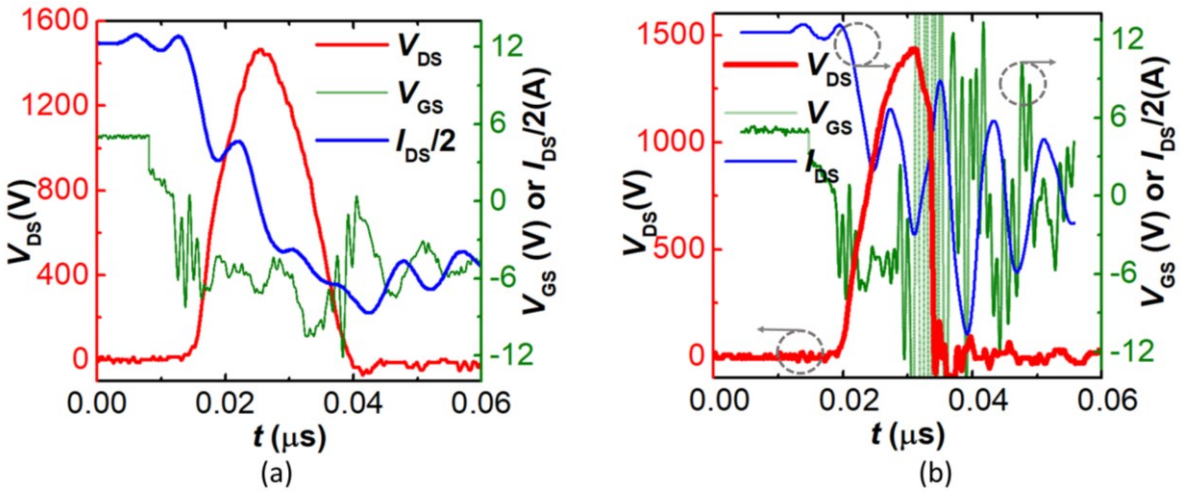


Figure 2-15. UIS (a) safe withstanding and (b) failure waveforms of the SP-HEMT with a 25 ns pulse width.

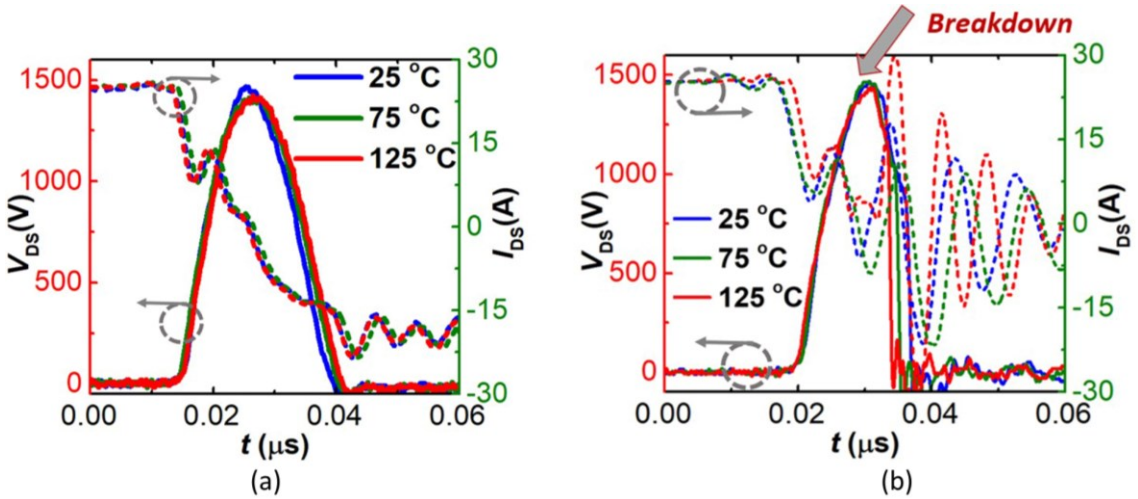


Figure 2-17. UIS (a) safe withstanding and (b) failure waveforms of the SP-HEMT with a 25 ns pulse width at three different temperatures (25 ºC, 75 ºC, 125 ºC)

Figure 2-16 shows the spectrum of the last safe-withstand waveform (10 V below destruction) for four pulse widths from 25 ns to 5 ms. A clear *BV* dependence on pulse width is identified, revealing a *BV* decrease from 1480 V to 1270 V. Finally, Figure 2-18 shows the box plots of the *BV vs.* pulse width (from 25 ns to 2 s) at 25-125 ºC. A total of 8 different pulse widths and 3 different temperatures are implemented. At each condition, 6 DUTs are tested to failure to obtain the *BV*. The *BV*s for the pulse width below 20 ms are obtained in the UIS test and above 20 ms are tested in a commercial pulse I-V system (with a 2 ms shortest pulse). The *BV* measured in these two methods are validated to be consistent under the same conditions, which is confirmed in 2 ms

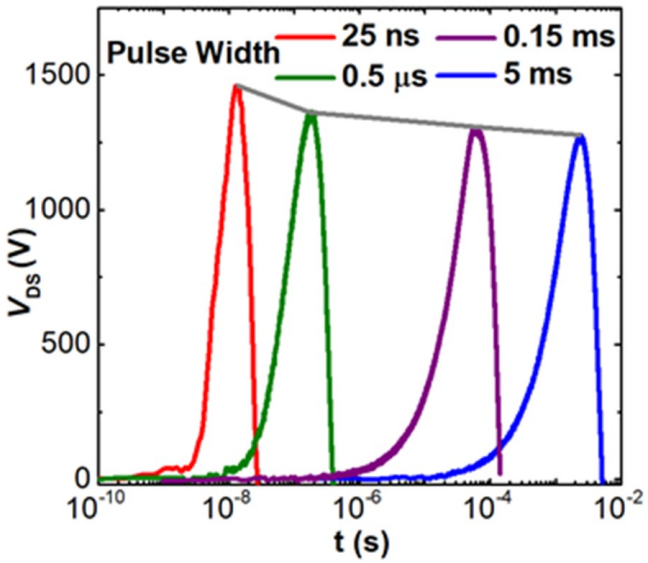


Figure 2-16. The last safe-withstand waveforms of SP-HEMTs in the UIS tests with four different pulse widths. *t* is plotted in the log scale.

to 50 ms. From the box plot, three key findings are revealed: a) a consistent BV decrease from 1480±10 V to 950±10 V across 8 orders of magnitude in the pulse width, showing a "dynamic BV (BV_{DYN})" phenomena. b) At the same pulse width, i.e., 20 ms, the transient BV decreases as temperature increases from 25 to 125 °C. c) When pulse width is longer than 200 ms, device BV converges to the static BV value: i.e., at 25 °C, the BV is measured to be 950 V at both 200 ms and 2 s pulse widths.

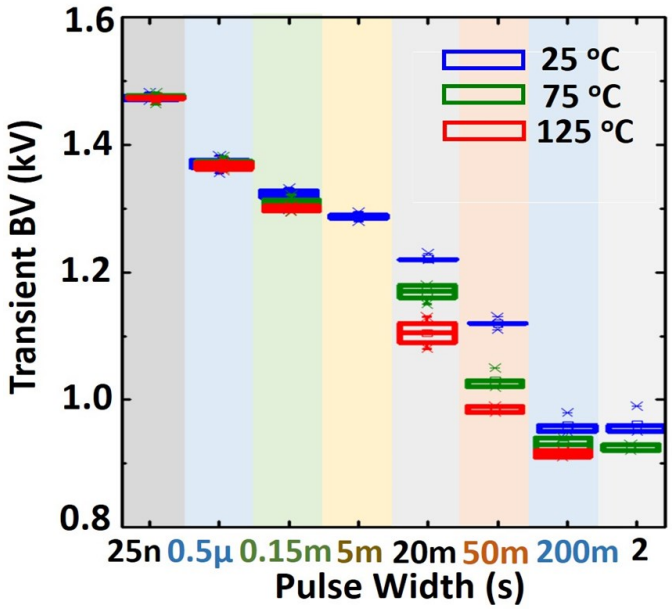
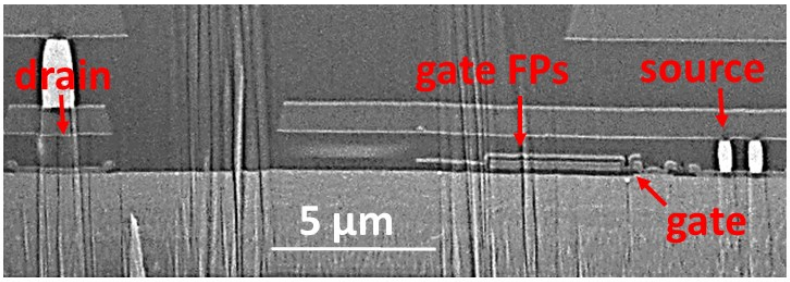


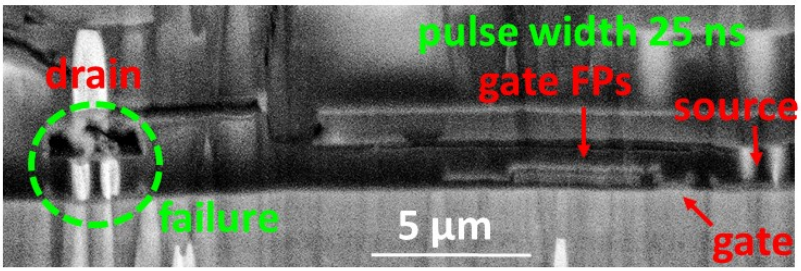
Figure 2-18. Box plots of the transient BV of GaN SP-HEMTs at 8 pulse widths and 3 temperatures.

To explain the BV_{DYN} in GaN HEMT, microscopic failure analysis is first conducted. After the de-capsulation of the failed DUTs, the failure spots are identified by EMMI, followed by the SEM inspection. Mixed-mode TCAD simulations are also performed, with the device model calibrated with the datasheet and the simulated UIS waveforms calibrated with experiment [69]. At different pulse widths of 25 ns and 5ms, the breakdown locations are found to be consistently at the drain side (Figure 2-19), which agrees with the simulated peak E-field location in GaN when the SP-HEMT is at the peak V_{DS} transient (Figure 2-10), confirming the same peak E-field induced device breakdown as illustrated in section 2.2.

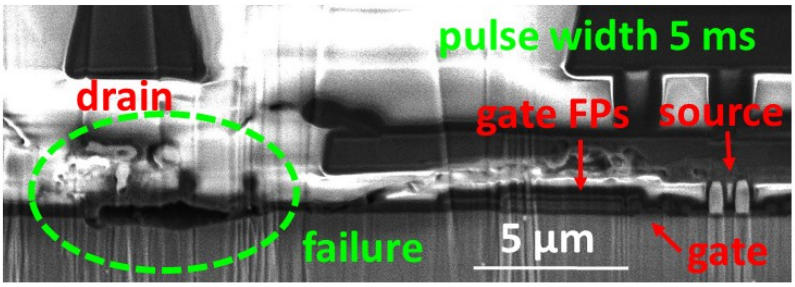
The BV_{DYN} can be explained by the dynamic filling of buffer traps. At zero drain bias, the acceptor-like buffer traps are partially filled, leaving a number of available trap states in the buffer layer [94], [95]. At high V_{DS}, electrons will be injected into the buffer from the source or from the



(a)



(b)



(c)

Figure 2-19. Cross-sectional SEM images of a SP-HEMT unit-cell in a (a) fresh device, (b) failed device in 25 ns pulses, and (c) failed device in 5 ms pulses. The breakdown locations are both at the drain side

Si-substrate/transition-layer interface, inducing the filling of acceptor traps (or hole emission) [96]. Figure 2-20 shows the simulated E-field contours with different trap filling profile. It reveals a higher E-field at the drain side with more negative buffer charges (ionized traps) (Figure 2-20(b) and (c)). Corresponding the simulation results to the UIS test, at shorter pulses, less electrons are injected and trapped in the buffer, leading to a higher *BV*. If minimal buffer traps are filled, the peak E-field reaches the critical E-field of GaN (E_C~3.4 MV/cm) at 1450 V V_{DS} (Figure 2-20(a)), which agrees with the *BV* measured in 25 ns pulses. As the pulse width increases, more traps in the buffer are ionized and *BV* decreases. When the filled buffer trap density reaches its max limit (i.e., all available traps are filled), no further decrease of *BV* will be presented. In the TCAD simulation, a maximum ionized trap density of 3.2×10^{16} cm^{-3} is used, which is similar to the

reported max ionized density of carbon-related traps [94], the peak E-field reaches E_C at 950 V (Figure 2-20(c)), which agrees with the BV in 200 ms or longer pulses and the static sweep. At higher temperatures, the electron injection and trap filling are enhanced, inducing a higher ionized trap density hence the BV drops faster with the increased pulse width (Figure 2-18). This physical explanation on the BV_{DYN} has recently been validated by experimental results of the electric field mapping from another group [97].

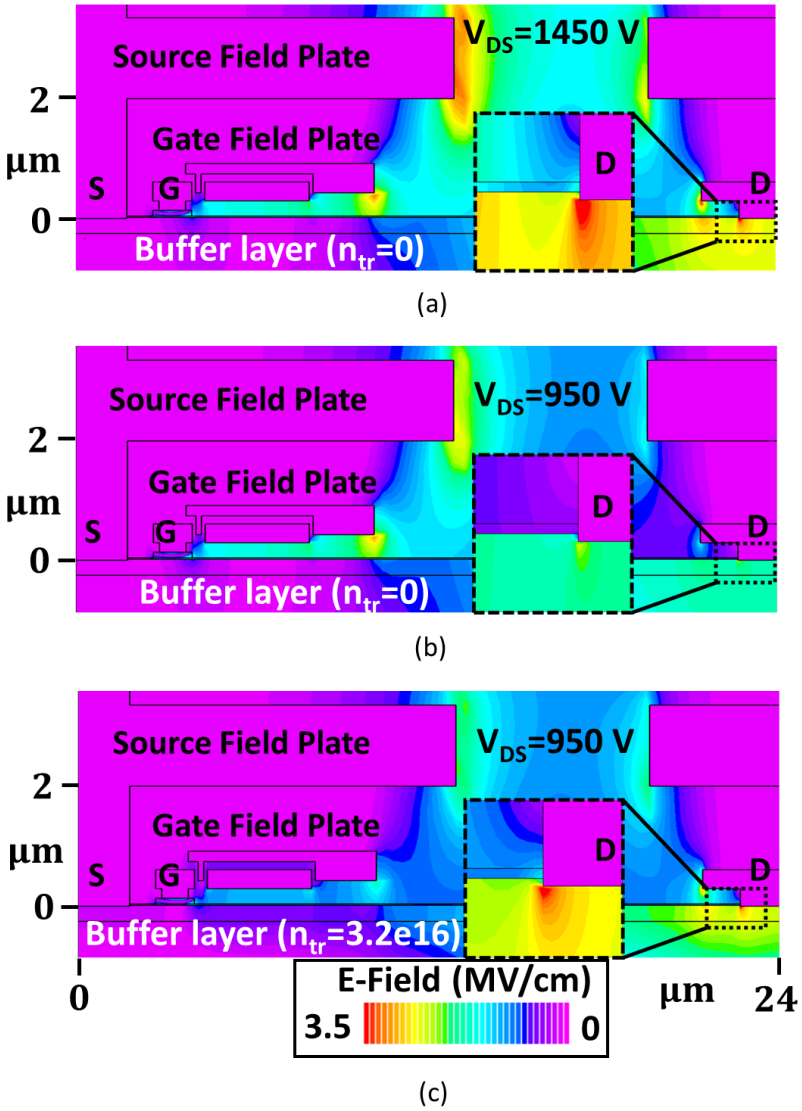


Figure 2-20. Simulated E-field in SP-HEMT at the transient peak V_{DS} for (a) 1450 V V_{DS}, no ionized buffer trap, (b) 950 V, no ionized buffer trap, and (c) 950 V, an ionized acceptor-like buffer trap density of 3.2×10^{16} cm^{-3}.

B. Dynamic BV of HD-GITs

The UIS waveforms of HD-GITs are found to be consistent with the ones of SP-HEMTs. Figure 2-21 shows the last safe-withstand waveforms at various pulse widths from 25 ns to 5 ms, and Figure 2-22 shows the box plots of the *BV vs.* pulse-width at three different temperatures. The *BV* of the HD-GIT shows a much smaller variation compared to SP-HEMTs, dropping from 1180±5 V to 1095±5 V for the pulse width of 25 ns to 5 ms, and remaining unchanged in longer pulses. The *BV* shows little temperature dependence. From the FIB microscopic inspection, the HD-GIT shows the same electric breakdown mechanism as the SP-HEMT: the breakdown location in HD-GIT is also at the drain side (Figure 2-24), agreeing with the simulated peak E-field location.

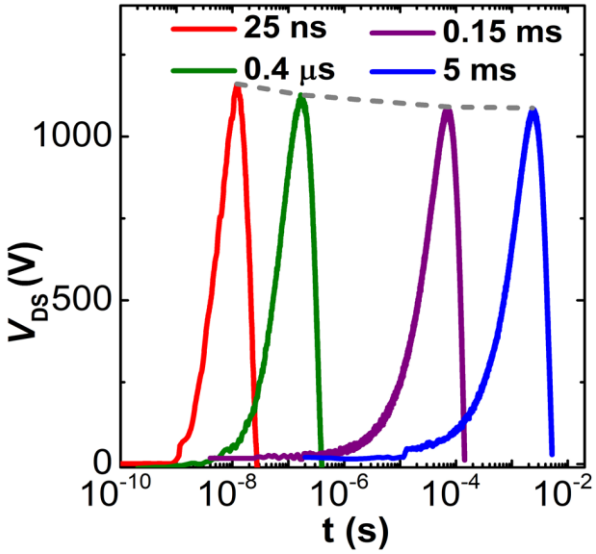


Figure 2-21. The last safe-withstand waveforms (10 V below the breakdown) of the HD-GITs with four

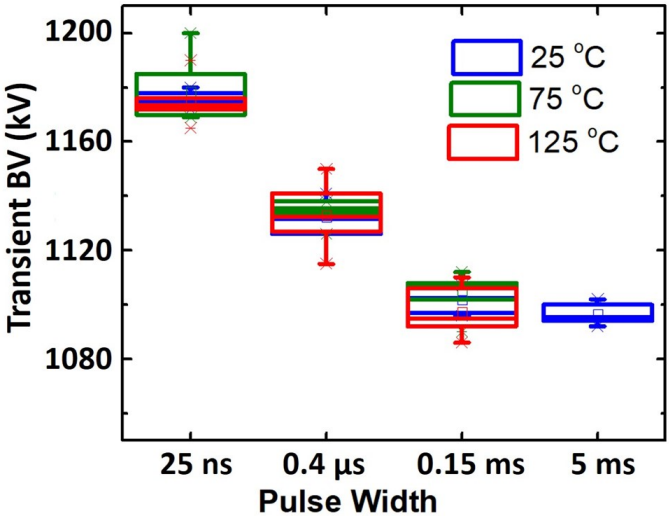


Figure 2-22. Box plots of the BV of GaN HD-GITs at 4 pulse widths and 3 temperatures. The BV reduces from ~1180 V to ~1095 V when the pulse width increases from 2 ns to 5 ms.

The smaller BV_{DYN} range in the HD-GIT suggests less buffer electron trapping, which is explained by the hole injection from the mixed drain (Figure 2-24): at high V_{DS}, the p-GaN at the drain injects holes into the GaN buffer layer, which accelerates the de-trapping process. Comparing with SP-HEMT, the HD-GIT has a smaller trapped charge density in GaN buffer under the same testing conditions; hence a smaller variance in the BV_{DYN} is exhibited.

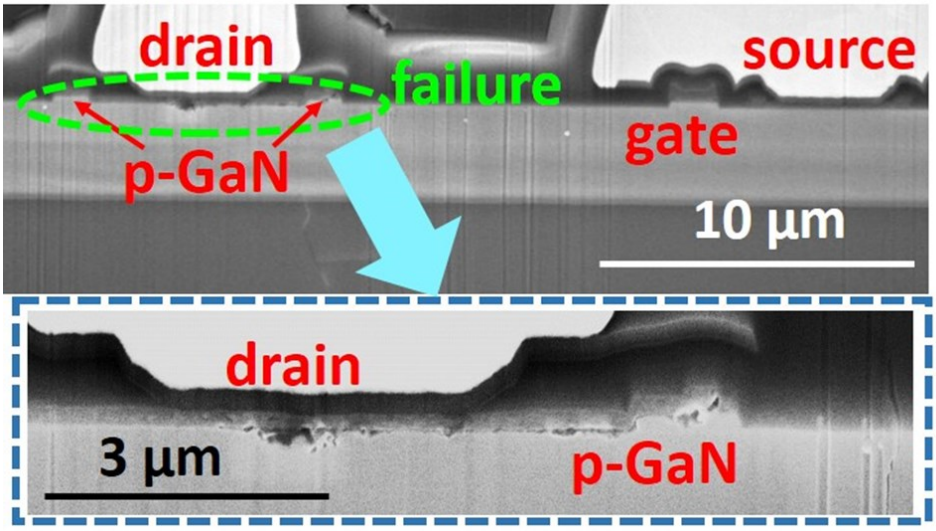


Figure 2-23. Cross-sectional SEM image of the HD-GIT failed in 25 ns pulses. The breakdown location is at the hybrid-drain.

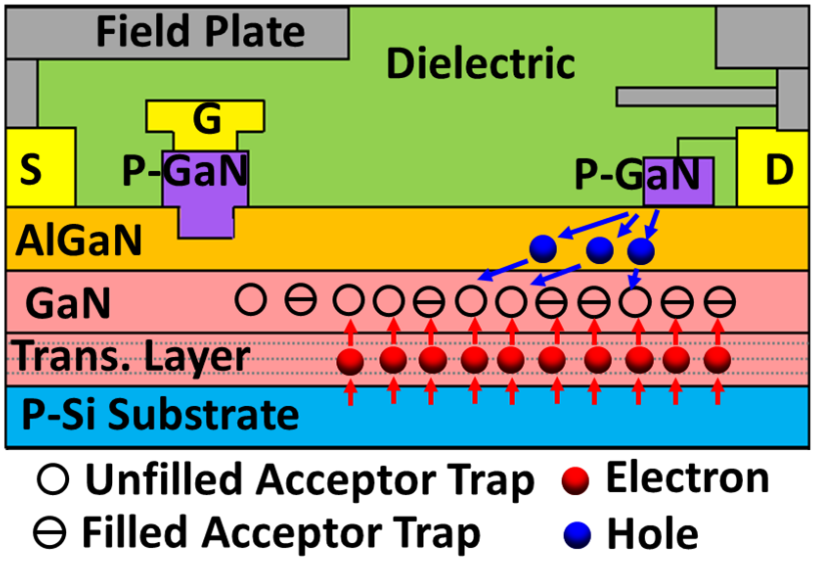


Figure 2-24. Illustration of the buffer de-trapping by hole injection in the HD-GIT.

2.3.3 Repetitive Overvoltage Test Results

The higher BV_{DYN} in shorter transients can provide GaN HEMTs additional safe margin in the power applications involving transient overvoltage, as the converter design usually relies on the device static BV. However, the buffer trapping may increase the risk of charge accumulation under repetitive overvoltage pulses, if the charges cannot be fully de-trapped within the switching period, which may gradually lower the BV at high frequency operations.

To understand this trade-off, SP-HEMTs and HD-GITs are tested under repetitive UIS pulses with two pulse widths (25 ns and 0.5 µs) and two switching period (50 µs and 1 ms; the inductive energy is clamped in both periods), for up to 10,000 pulses. From 2.3.2, it is known that the longer pulse width induces more buffer trapping. While a longer pulse period can provide longer de-trapping time between pulses, the dynamics of trapping and de-trapping are studied by different composition of the pulse widths and pulse periods. The peak V_{DS} is set to be 95% of the BV_{DYN} corresponding to each pulse width, based on the value unveiled in section 2.3.2.

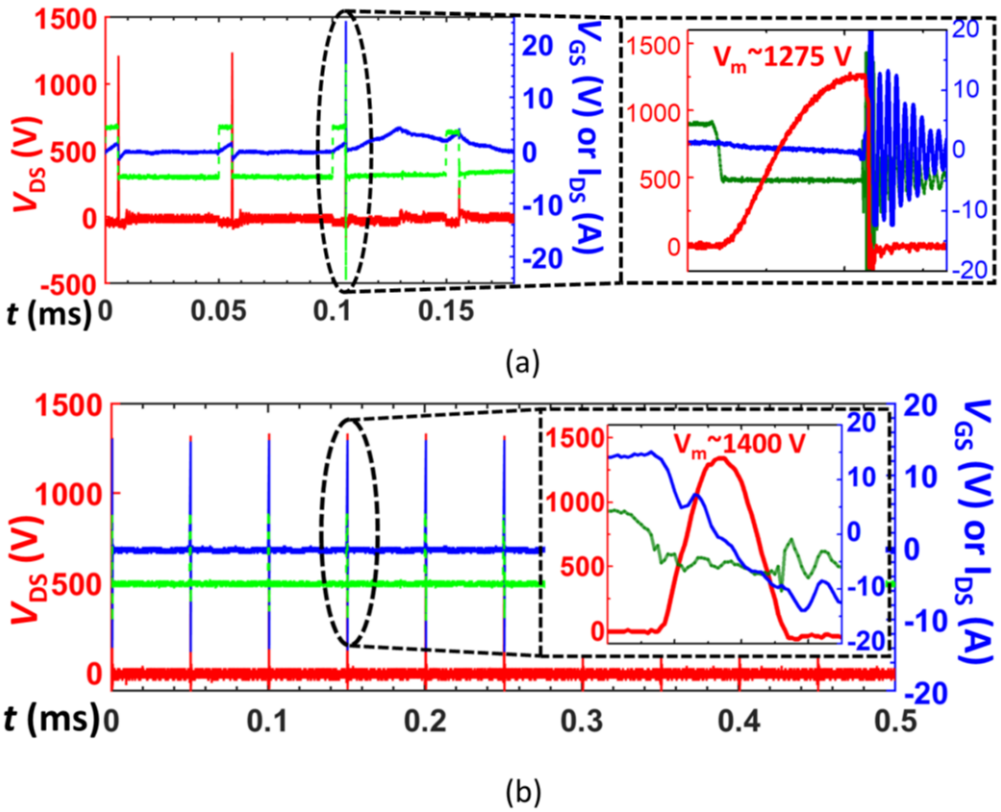


Figure 2-25. Repetitive UIS waveforms of the SP-HEMT with a pulse width of (a) 0.5 µs (failure in a few pulses) and (b) 25 ns (no failure after 10,000 pulses).

Table 2-2. Summary of Conditions and Results of the Repetitive UIS Tests.

Pulse Period	Device	Pulse Width	BV (V)	Peak Voltage (95% BV) (V)	Test Results (Device failure or degradation)
50 µs (20 kHz)	SP-HEMT	25 ns	1470	1400	No failure or degradation after 10,000 cycles, part of the test waveform shown in Fig. 2-25(b)
		0.5 µs	1340	1275	Failure in less than 10 cycles, waveforms shown in Fig. 2-25(a), failure at the peak voltage transient
	HD-GIT	25 ns	1170	1110	No failure or degradation after 10,000 cycles
		0.5 µs	1135	1080	Failure in about 100 cycles, waveforms similar to Fig. 2-25(a), failure at the peak voltage transient
1 ms (1 kHz)	SP-HEMT	25 ns	1470	1400	No failure or degradation after 10,000 cycles
		0.5 µs	1340	1275	No failure or degradation after 10,000 cycles
	HD-GIT	25 ns	1170	1110	No failure or degradation after 10,000 cycles
		0.5 µs	1135	1080	No failure or degradation after 10,000 cycles

As shown in Table 2-2 and Figure 2-25, under the 50 µs period (20 kHz), the SP-HEMT fails in only a few 0.5-µs-wide pulses but survive 10,000 25-ns-wide pulses without degradation; with the aid of hole injection, HD-GITs still fail in ~100 0.5-µs-wide pulses but survive 10,000 25-ns-wide pulses. When the switching period increases to 1 ms (1 kHz), the SP-HEMTs and HD-GITs both survive 10,000 25-ns and 0.5-µs-wide pulses. These results imply that the overvoltage margin from the "dynamic *BV*" is kept under two conditions: a) small parasitic/load inductance and b) not too high frequency to induce an accumulation of filled traps. It should be noted that the test results in Figure 2-25 only discusses the device survival, while the degradation of DUTs is not characterized. In [95], GaN HEMTs degradation and recovery under repetitive overvoltage conditions are studied by unitizing repetitive UIS test in kHz frequency range, and a recoverable negative threshold voltage shift is identified to be the major degradation due to the impact ionization induced hole trapping near the gate region.

2.4 Conclusions

This chapter covers the surge energy and overvoltage robustness of GaN HEMTs under single-event tests. Section 2.2 unveils the withstand process and failure mechanisms of commercial p-gate GaN HEMTs under the transient surge energy and overvoltage implemented by a traditional UIS test. The surge-energy withstand process and failure mechanisms of GaN HEMTs are found

to be fundamentally different from the Si and SiC MOSFETs with avalanche capability. The GaN HEMT is capable of withstanding surge energy through its intrinsic overvoltage capability, via a resonance nature, but it cannot dissipate the surge energy during the withstand process. The device failure under surge-energy is mostly related to the peak overvoltage, which is defined as device *BV*. The magnitude of surge energy is no longer a parameter that can directly reflect the device intrinsic surge ruggedness for GaN HEMTs. The failure mechanism is mostly E-field limited and the breakdown locations in device are consistent with the peak E-field locations.

Section 2.3 presents a new UIS test with tunable pulse width to measure the transient *BV* of a non-avalanche power device, from which the transient *BV* of GaN power HEMTs under a pulse width from 25 ns to 2 s is characterized. The *BV* in shorter pulses is found to be higher than the static *BV* by up to 500 V, due to reduced buffer trapping. This "dynamic BV" provides additional overvoltage margin for the GaN power converters involving voltage overshoot and surge energy, under certain restrictions in the load/parasitic inductance and switching frequency.

While these findings in this chapter provide important new insights on GaN HEMT surge energy robustness and breakdown voltage physics, it should be mentioned that the results shown in Table 2-2 indicates a frequency dependent BV_{DYN}, but the detailed discussion is not covered by the content in this chapter due to the limitation of the UIS setup. The switching frequency of GaN HEMT-based converters is usually at least hundreds of kHz [92], [98], some even in the range of MHz [99], [100]. A 20 kHz repetitive UIS performed in section 2.3.3 cannot resemble the high frequency application scenario and further improvement on the test setup can be made. The design of the high frequency overvoltage test system for GaN HEMT and the testing results with degradation and failure analysis will be presented in Chapter 3.

Chapter 3: GaN HEMTs Overvoltage Robustness Under High Frequency Switching

3.1 Introduction of the High Frequency Overvoltage Test (HFOT)

3.1.1 Limitation of Current Overvoltage Test Methods

To date, the majority of the GaN HEMT overvoltage tests are performed with the single-event UIS test. Denote the BV_{DYN} measured in such a test as the single-event BV_{DYN} ($BV_{DYN\text{-}SIN}$). The $BV_{DYN\text{-}SIN}$ has been found to be different from the static BV measured on a curve tracer and depend on the pulse width (and dv/dt) and temperature due to the time-dependent trap filling in the GaN HEMT structure [73], [97], [101], [102], which has been explained in detail in section 2.3.3.

Beyond the single-event test, the repetitive UIS results in section 2.3.3 and some recent works show that the BV_{DYN} in continuous switching ($BV_{DYN\text{-}SW}$) can be different from the $BV_{DYN\text{-}SIN}$ [73], [103], [104]. For example, the $BV_{DYN\text{-}SW}$ of 650 V cascode GaN HEMTs in 100 kHz continuous switching (1.25-1.3 kV) is found to be lower than $BV_{DYN\text{-}SIN}$ (1.4-1.7 kV) [73]. However, it is hard to further push up the switching frequency (f_{sw}) in the repetitive UIS. Figure 3-1 recaps the typical testing waveforms of the UIS test with four main phases marked: (1) L_{loop} charging by power supply with the device DUT turned-on; (2) overvoltage resonance between device C_{OSS} and loop

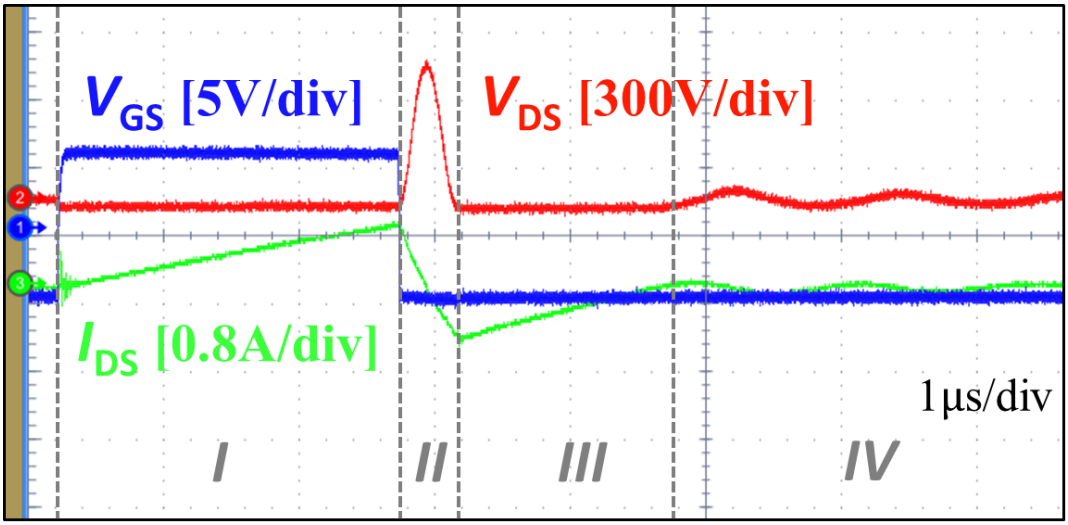


Figure 3-1. Illustration of different phases in a complete UIS process.

indctor (L_{loop}); (3) L_{loop} discharging via the DUT reverse conduction; and (4) residual resonance due to the difference between V_{BUS} and the DUT's V_F^{3rd}. In order to run a repetitive UIS test with stable V_M among switching cycles, the switching period should at least cover the time of phase *I* to phase *III* to fully damp the surge energy in L_{loop} [102], hence the f_{sw} can be limited in the UIS or the clamped inductive switching (CIS) test due to a similar reason [69], [95], [102].

On the other hand, state-of-the-art GaN converters are operating at hundreds of kilohertz or even megahertz [92], [98], [99]. The overvoltage robustness and BV_{DYN} of GaN HEMTs in such high-frequency switching remains a knowledge gap. To address this gap, new test setups for the high frequency overvoltage test (HFOT) are required.

3.1.2 Design of the HFOT with Active Clamping Circuit (ACC)

Figure 3-2 shows the circuit schematic of the buck converter based HFOT. This testbed features DUT zero-voltage turn-on realized by tuning the duty cycle and the value of the filter inductor (L_M) for a negative inductor current when the DUT is switched-on. An additional air-core inductor (L_{air}) is placed next to the drain side of the top switch (i.e., the DUT). In the DUT's hard turn-OFF transient, the energy stored in L_{air} goes through the OFF-state DUT and produces the V_{DS} overshoot in the DUT. The peak V_{DS} in the overshoot can be controlled by the V_{BUS}, value of L_{air} and the current flowing through it at the DUT turn-OFF ($I_{L\text{-}off}$). An active clamping circuit (ACC) is connected in parallel with the L_{air}, which consists of a power resistor (R_C) and two back-to-back connected power MOSFETs for bidirectional voltage blocking.

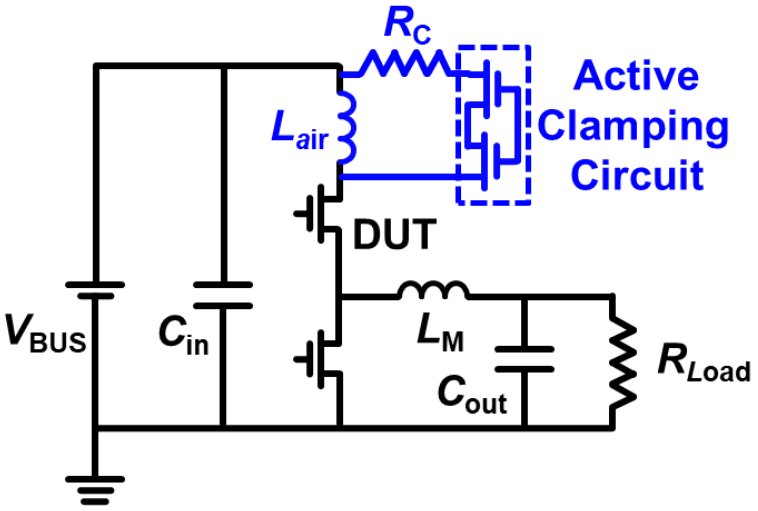


Figure 3-2. Test circuit schematic of the HFOT

The functions of this ACC are regulating waveforms and stabilizing the peak V_{DS}. To illustrates the working principles of the ACC, SPICE simulations are first performed at 400 V bus voltage (V_{BUS}), 1 MHz f_{sw} and 0.5 duty cycle. Figure 3-3(a) shows the simulated top switch V_{DS} waveforms without the ACC. As high V_{DS} overshoot is triggered, the energy in L_{air} could not be fully dissipated in the natural resonance by the end of the OFF-state period. As a result, in the next switching cycle, L_{air} is charged up from a non-zero current value, resulting in different $I_{L\text{-}off}$ and unstable peak V_{DS} from cycle to cycle. Besides, multiple high V_{DS} pulses are produced in each switching cycle, all of which could potentially stress the DUT. This complex stress makes it difficult to accurately correlate the DUT's failure or degradation induced by the overvoltage stress.

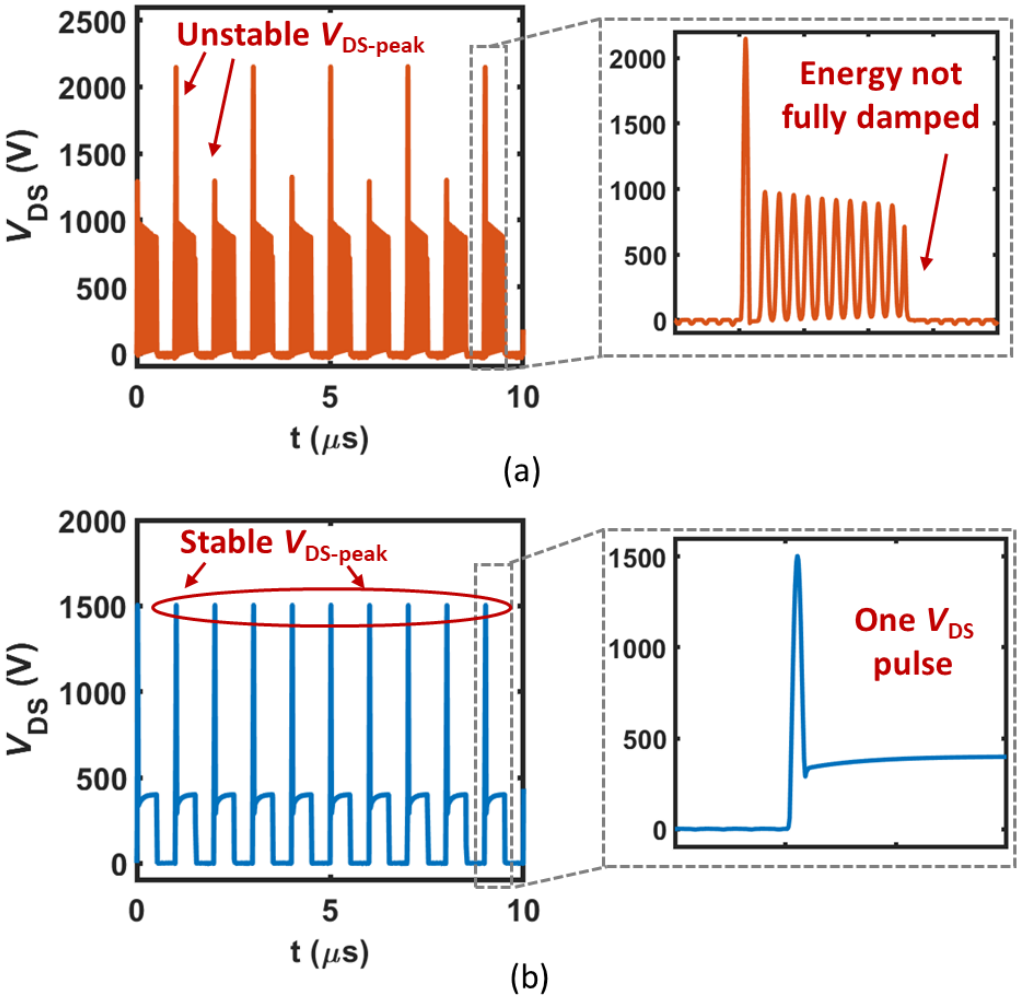


Figure 3-3. Simulated DUT V_{DS} waveforms (b) without and (c) with the ACC.

Figure 3-3(b) shows the simulated waveforms with the ACC intervention. The power MOSFETs in the ACC switch at the same f_{sw} as the main converter. In each switching cycle, the ACC turns ON right after the first pulse of the V_{DS} overshoot, which transfers the surge energy to the ACC loop; the ACC turns OFF before the top switch turns ON, which regulates the overvoltage ringing waveform to contain only one high V_{DS} overshoot pulse. In addition, the energy stored in L_{air} is fully dissipated in the ON-state power MOSFETs and R_C in each cycle, allowing for the realization of a stable peak V_{DS}. It is worth mentioning that passive clamping circuits (e.g., an *RC* snubber) across the L_{air} are not preferred in the HFOT as they drastically decrease the *dv/dt* of the hard turn-off transient and prevent the HFOT from mimicking the high frequency operations in practical power converters. In conclusion, the HFOT proposed in this dissertation best resembles the GaN HEMTs operation in converters except for a higher and tunable V_{DS} overshoot in each switching cycle.

3.1.3 Device Under Test and Their Single-event UIS Breakdown Voltage

Table 3-1 summarize the specifications of the four DUTs tested in this work, with the manufacturers listed as well. The DUTs are mainstream commercial p-gate enhancement mode GaN HEMTs from multiple vendors, covering both 100-V and 600-V rating and different gate stack designs. DUT #1 is the HD-GIT with Ohmic gate contact and an additional p-GaN connected to the drain. DUT #2-4 are the SP-HEMT with a Schottky contact formed on p-GaN. DUT #1 and #3 are 600/650 V rated, while DUT #2 and #4 are 100 V rated.

Table 3-1. Summary of key parameter of DUTs

DUT	Voltage Rating (V)	Manufacturer	Part Number	Structure	Static *BV* (V)	$BV_{DYN\text{-}SIN}$ (V)
#1	600	Infineon	IGOT60R070D1	HD-GIT	>1000	1160
#2	100	EPC	EPC2045	SP-HEMT	180	280
#3	650	GaN Systems	GS66508T	SP-HEMT	950	1365
#4	100	GaN Systems	GS61008T	SP-HEMT	180	390

The DUTs are first characterized on the Keysight B1505A curve tracer to acquire the static *BV* through the quasi-static I-V sweep [105]. Figure 3-4 shows the off-state I-V characteristics of the DUTs. DUT #1 shows no failure when the drain leakage current (I_D) reaches the 8-mA

measurement current compliance. Other DUTs fail catastrophically with the drain to source short upon failure.

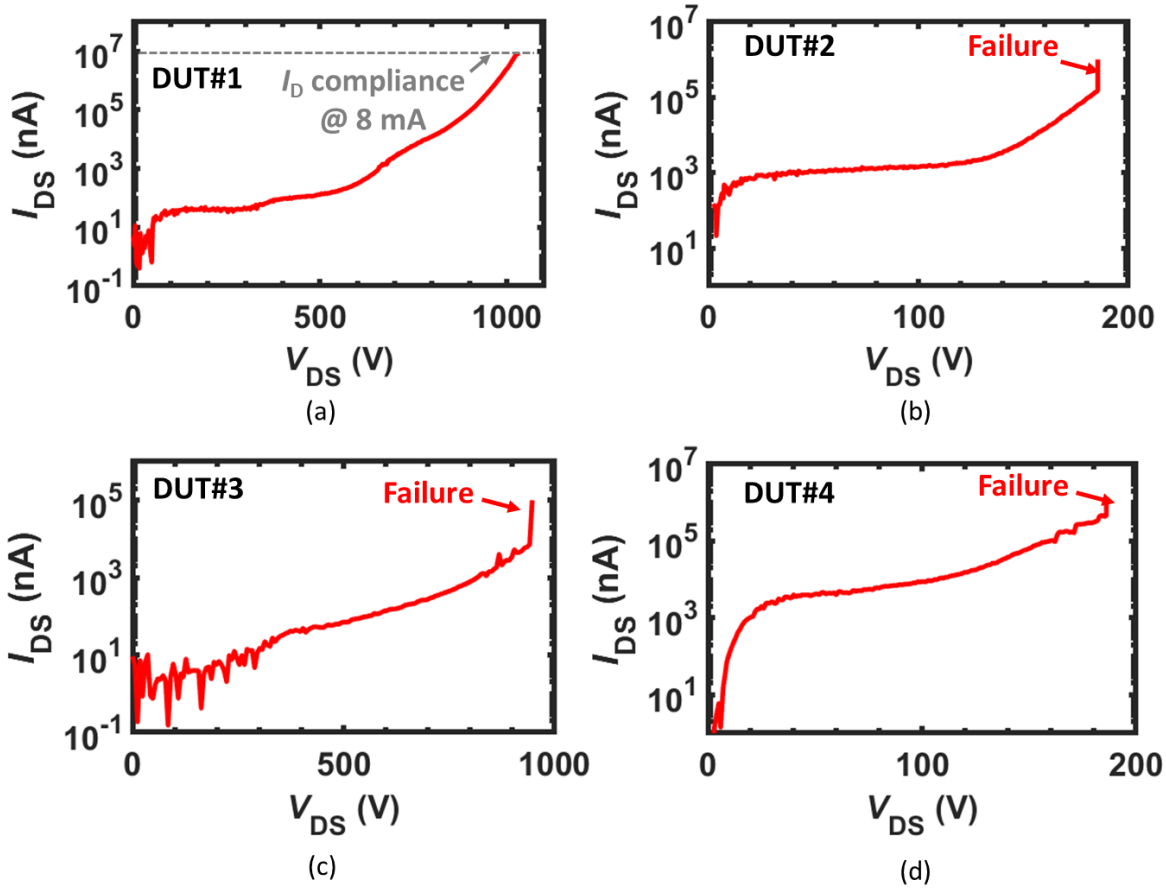


Figure 3-4. Off-state I-V characteristics of the four DUTs measured on the curve tracer with the static *BV* marked.

The $BV_{DYN\text{-}SIN}$ is extracted from UIS test with a L_{loop} of 300 nH (implemented by a commercial air core conductor, 2222SQ-301), a V_{BUS} of 30 V (for DUT #1 and #3) or 20 V (for DUT #2 and #4). Figure 3-5 shows the failure V_{DS} waveforms in the UIS tests. Upon failure, a sudden drop in V_{DS} is observed, and the peak V_{DS} (V_M) in the waveform is recorded as the $BV_{DYN\text{-}SIN}$. For each DUT, three devices are tested to failure, and their $BV_{DYN\text{-}SIN}$ show good consistency. As summarized in Table 3-1, it is clear that the $BV_{DYN\text{-}SIN}$ of all four DUTs are higher than their static *BV*. This is due to the enhanced buffer trapping in quasi-static I-V sweep on the curve tracer, which has been well explained in section 2.3.

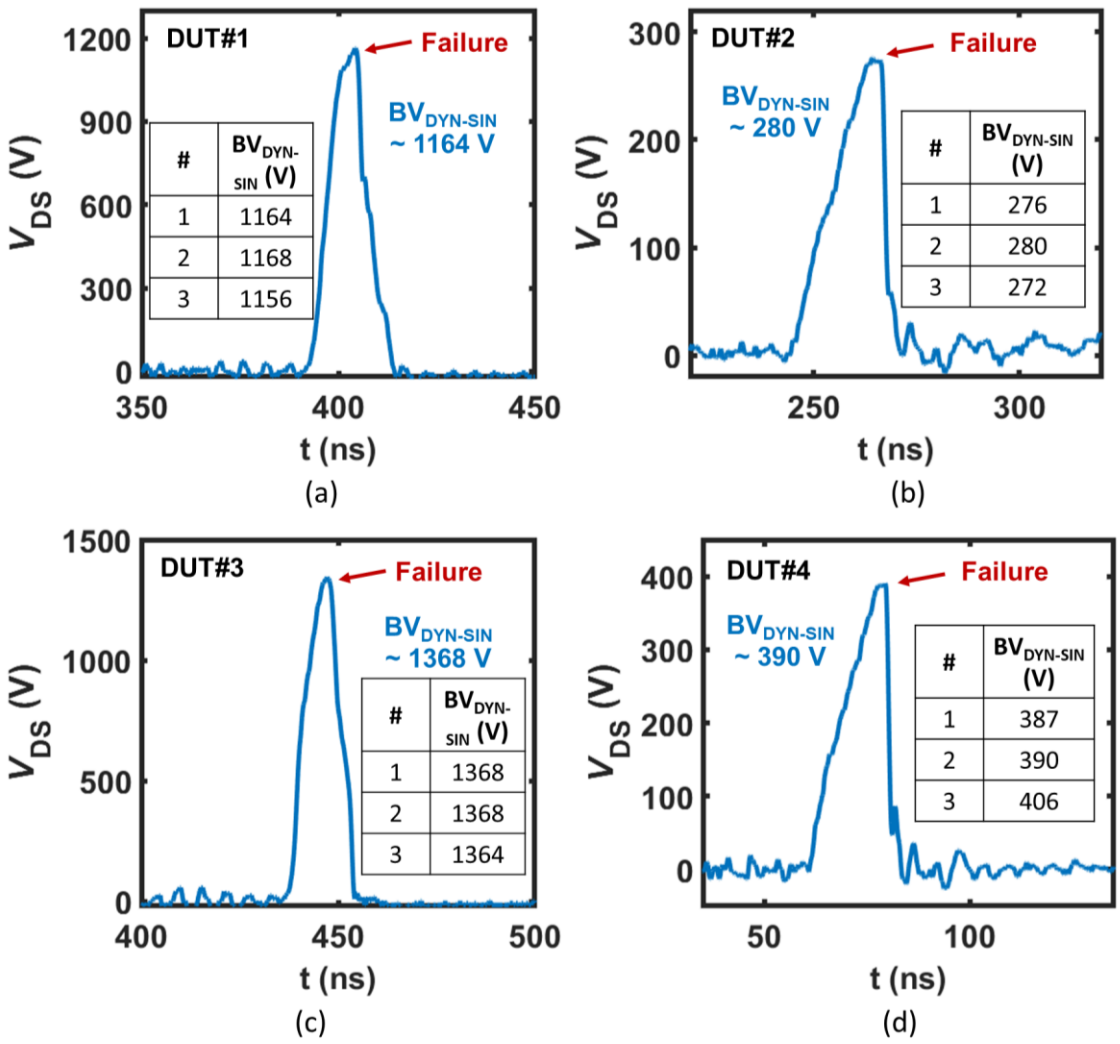


Figure 3-5. Typical UIS failure waveforms and the $BV_{\text{DYN-SIN}}$ of the four types of DUTs extracted from the single-pulse UIS tests. Three devices are tested to failure for each type of DUT, and their $BV_{\text{DYN-SIN}}$ are listed in the inset of figures.

3.1.4 HFOT Test Hardware Setup and Test Procedure

The hardware is exhibited in Figure 3-6. The setup includes a universal mother board with the converter power loop, the power supply for gate drivers, the L_{air} and ACC, and a daughter card. The daughter card comprises a half bridge to accommodate different package footprints and gate drivers for various types of commercial GaN HEMTs.

A key concern of the HFOT implementation is the DUT's heat dissipation, as some commercial GaN HEMTs have a very small cooling pad. To alleviate the thermal stress on the DUT (the top

switch), the other device with a larger cooling pad is intentionally selected as the bottom switch, as shown in Figure 3-6(b). In this way, the converter's duty cycle could be reduced (set to 0.12 in the HFOT experiments), allowing most of the conduction loss to dissipate on the bottom switch. The bottom switch is effectively cooled by an external heatsink and a strong fan blowing.

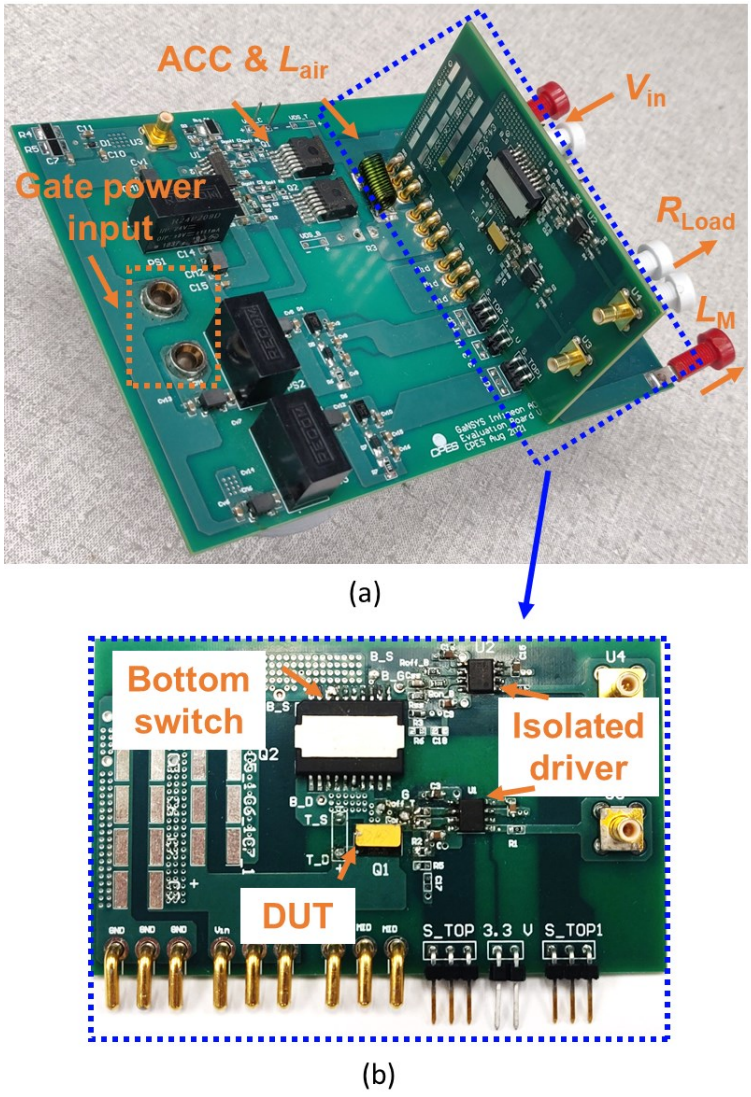


Figure 3-6. Photos of the (a) overall HFOT setup and (b) daughter card.

Another concern of the HFOT setup is the signal isolation, as the HFOT involves high V_{DS} overshoot. In a bootstrap configuration, the V_{DS} signal could couple to the gate signal of the complimentary transistor due to the limited isolation capability from the bootstrap capacitor, which may cause false turn-ON of transistors. To address this concern, two SI8271GB-IS gate drivers with 2.5 kV isolation capability are used to drive the transistors separately. The gate control signals

are given by external function generators. The driving circuitry and gate voltage follow the recommendation from the DUTs' datasheets and application notes [79]–[81], [106], [107]. For a more accurate DUT V_{DS} measurement, a Tektronix TIVH08L differential probe with optical isolation and 800 MHz bandwidth is used.

The work presented in section 2.3 has revealed that BV_{DYN} of GaN HEMTs is dependent on the pulse width (or *dv/dt*) in the overvoltage resonance. Hence, to make a fair comparison with the single-event UIS test, the same 300 nH L_{air} used in section 3.1.3 is selected for the HFOT setup. Figure 3-7(a) shows the layout of the ACC. A 2 Ω, TO-247 packaged power resistor is mounted in the vias as R_C, and two 1.7 kV SiC MOSFETs (IMBF170R450M1XTMA1) are selected to actively clamp the inductor energy. Note that the two MOSFETs are back-to-back connected (i.e., drain-source-source-drain) for bi-directional voltage blocking in its off-state. The ACC voltage

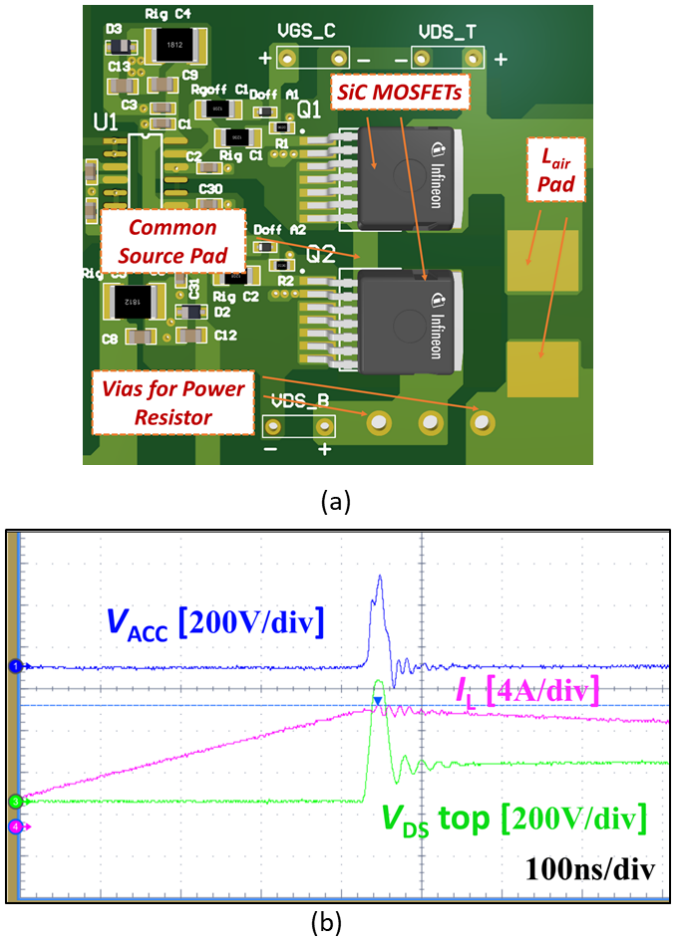


Figure 3-7. (a) PCB layout of the active clamping circuit. (b) Voltage waveform of the active clamping circuit at 200 kHz, 600 V V_{DS} peak.

waveform is shown in Figure 3-7(b), the voltage of ACC follows the contour of DUT V_{DS} with a gap of V_{BUS}. The voltage distortion in the V_{ACC} signal is from the insufficient bandwidth and isolation of THDP200 differential probe used for measurement. Upon the ACC turn-on, the voltage could be both positive or negative depends on the delay time. Bi-directional voltage blocking prevents the reverse turn-on of the SiC MOSFETs in the ACC and adds more flexibility in signal delay time control.

The load resistor R_{Load} and the filter inductor L_M values are carefully tuned based on the f_{sw} and DUT's C_{OSS} to generate negative inductor current I_L to realize the zero-voltage turn-on on the top switch (i.e., the DUT). The peak negative I_L value is kept small to reduce the voltage spike on bottom switch at its hard turn-off as well.

To compare different types of DUTs, a unified HFOT test procedure is applied. The delay of the ACC gate is first tuned at a low V_{BUS} to obtain desired waveforms. Then the peak V_{DS} of the DUT is stabilized at 600 V for 10 minutes for the DUT to reach the thermal steady state, and the case temperature (T_C) is checked by a thermal camera. Then the V_{BUS} is increased to raise the peak overvoltage magnitude on the DUT in continuous switching. The V_{BUS} increases within about 15 seconds until the DUT failure occurs. This relatively fast increase allows for the DUT's failure test in continuous switching, at the same time minimizing the risk of thermal runaway. In this process,

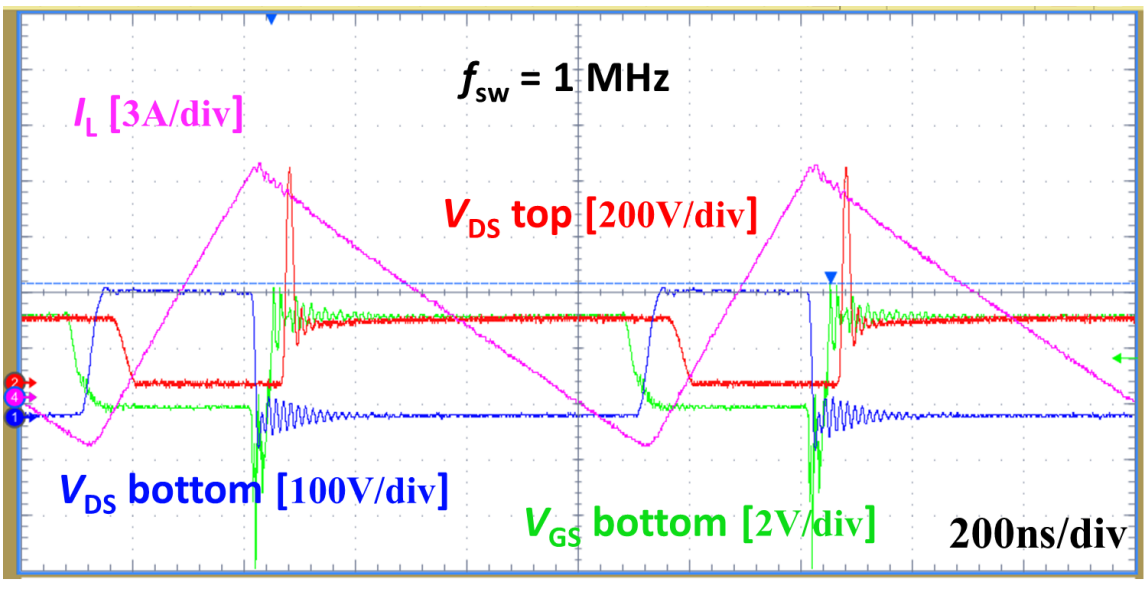


Figure 3-8. Sample test waveforms of the top switch (i.e., the DUT) and the bottom switch at f_{SW} = 1 MHz.

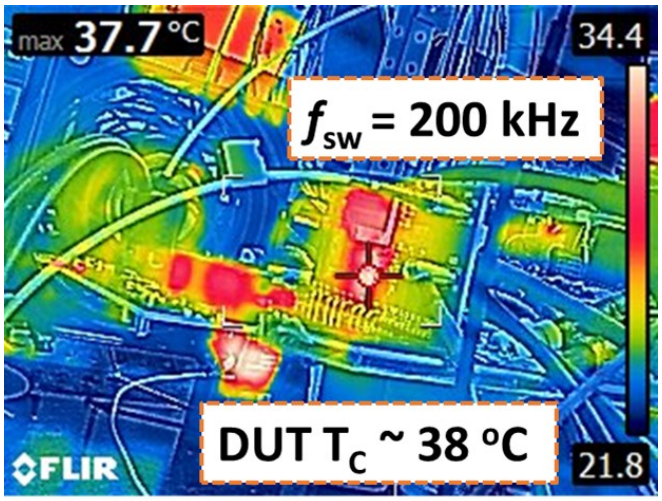


Figure 3-9. Thermal camera image of the DUT#3 operation in continuous switching with 600 V peak V_{DS} and 200 kHz f_{sw}.

all waveforms are recorded by a screen recording software, which allows for the post-processing to extract the DUT's failure waveform and $BV_{DYN\text{-}SW}$.

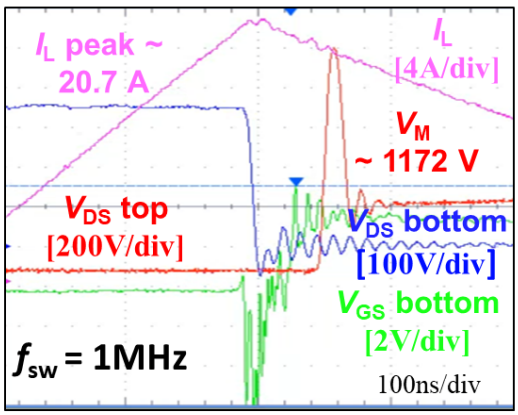
Based on the above test procedure, sample waveforms are acquired at 1 MHz f_{sw}, as shown in Figure 3-8. A 50 ns signal delay is added on top switch V_{DS} signal to have a clearer view of V_{DS} overshoot. The waveform confirms that the ZVS operation is achieved by the negative inductor current (I_L). At the hard turn-off transient, high V_{DS} overshoot is triggered by L_{air}; the ACC clamps the extra inductor energy, enabling only one high V_{DS} overshoot to be generated in each cycle with stable V_M from cycle to cycle. Among the four types of DUTs, DUT #3 has the most serious thermal concern due to its smaller package as compared to DUT #1 and its much larger R_{ON} as compared to DUT #2 and #4. Figure 3-9 shows thermal camera image, revealing a case temperature (T_C) below 40 °C for the DUT #3's operation at 200 kHz, 600 V peak continuous overvoltage switching.

3.2 HFOT Test Results on Commercial P-gate GaN HEMT

Similar to the UIS test, three devices for each type of the DUT are tested to failure in the HFOT. The recorded V_M in the failure waveform is extracted as the $BV_{DYN\text{-}SW}$ in each test.

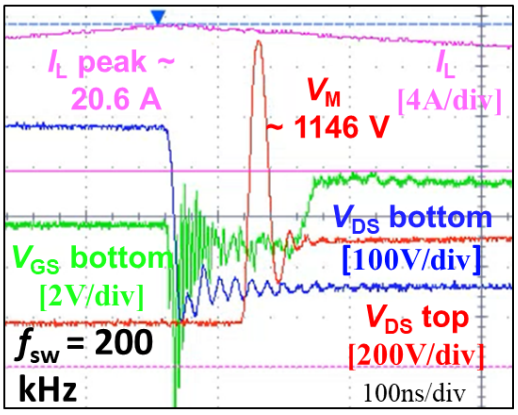
A. DUT #1

Figure 3-10 illustrates the recorded V_M waveforms showing the $BV_{DYN\text{-}SW}$ of *DUT #1* under the high-frequency HFOT with f_{sw} of 200 kHz and 1 MHz. The testing conditions for *DUT #1* are summarized in Table 3-2. Note that *DUT#1* has a large cooling pad, and there is no need to aggressively reduce the converter duty cycle for thermal management. The V_{BUS} at device failure is around 400 V. At f_{sw} of 1 MHz and 200 kHz, a consistent $BV_{DYN\text{-}SW}$ of ~1160 V is shown, which is identical to the $BV_{DYN\text{-}SIN}$ extracted from the single-pulse UIS test as shown in Fig. 3-5(a). Additional tests in the HFOT have confirmed this consistency at lower f_{sw}. This consistency suggests the nearly f_{sw}-independent BV_{DYN} of *DUT #1* and the dominance of electrical failure at the overvoltage boundary in continuous switching.



f_{sw}	#	V_M (V)
1 MHz	1	1172
	2	1156
	3	1127

(a)



f_{sw}	#	V_M (V)
200 kHz	1	1146
	2	1171
	3	1163

(b)

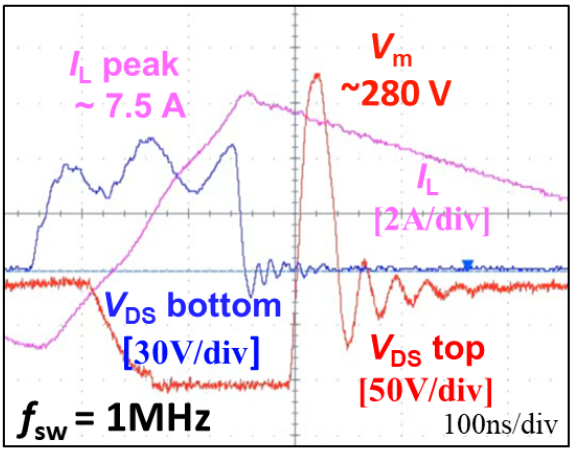
Figure 3-10. Recorded HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of DUT #1 at f_{SW} of (a) 1 MHz and (b) 200 kHz. The $BV_{DYN\text{-}SW}$ of three DUTs tested in each condition are listed below the waveform.

Table 3-2. Testing Conditions for *DUT #1*

f_{sw}	Duty Cycle	L_M (µH)	R_{Load} (Ω)	V_{BUS} at failure (V)	$BV_{DYN\text{-}SW}$ (V)
1 MHz	0.32	5.5	13.2	~400	~1160
200 kHz	0.4	22	13.2	~400	~1160

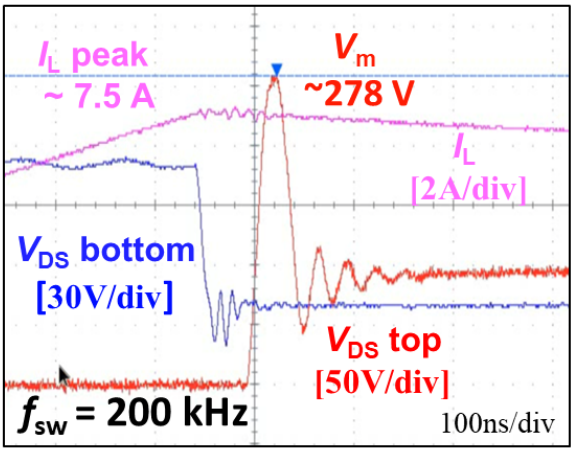
B. DUT #2

Similar to *DUT #1*, *DUT #2* also shows a f_{sw} independent $BV_{DYN\text{-}SW}$. As illustrated in Figure 3-11, a consistent $BV_{DYN\text{-}SW}$ of ~ 280 V is extracted at f_{sw} of 1 MHz and 200 kHz, which is consistent with the DUT #2's $BV_{DYN\text{-}SIN}$ shown in Figure 3-5(b). The testing conditions are summarized in Table 3-3.



f_{sw}	#	V_M (V)
1 MHz	1	280
	2	276
	3	278

(a)



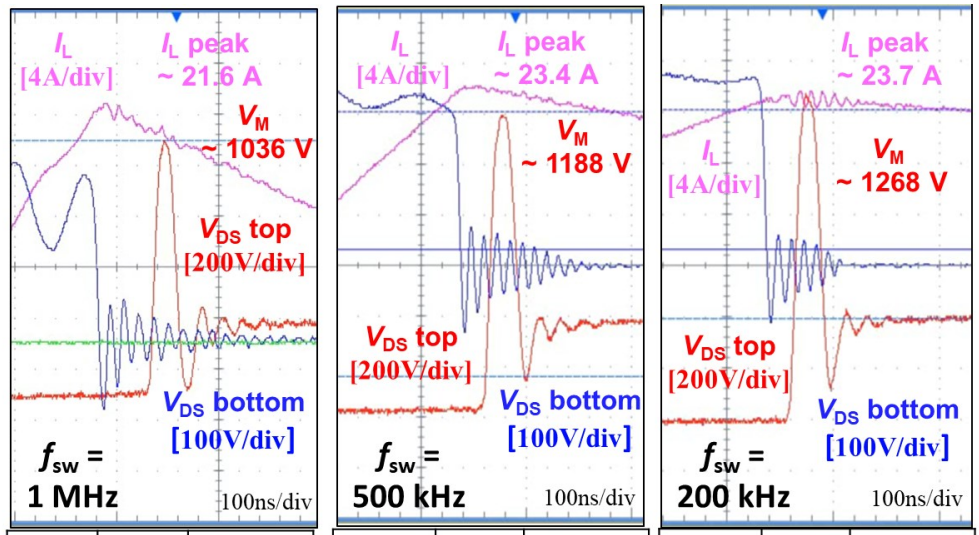
f_{sw}	#	V_M (V)
200 kHz	1	278
	2	278
	3	268

(b)

Figure 3-11. Recorded HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of DUT #2 at f_{SW} of (a) 1 MHz and (b) 200 kHz. The $BV_{DYN\text{-}SW}$ of three DUTs tested in each condition are listed below the waveform.

Table 3-3. Testing Conditions for *DUT #2*

f_{sw}	Duty Cycle	L_M (μH)	R_{Load} (Ω)	V_{BUS} at failure (V)	$BV_{DYN\text{-}SW}$ (V)
1 MHz	0.12	1.0	5	~70	~280
200 kHz	0.12	8.6	5	~70	~280



f_{sw}	#	V_M (V)
1 MHz	1	1036
	2	1060
	3	1040

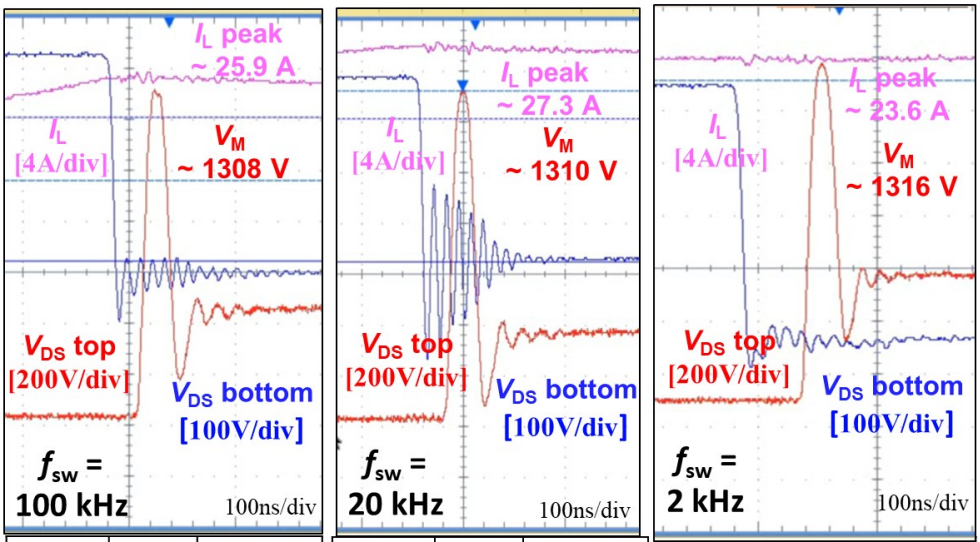
(a)

f_{sw}	#	V_M (V)
500 kHz	1	1188
	2	1188
	3	1192

(b)

f_{sw}	#	V_M (V)
200 kHz	1	1268
	2	1264
	3	1268

(c)



f_{sw}	#	V_M (V)
100 kHz	1	1308
	2	1308
	3	1306

(d)

f_{sw}	#	V_M (V)
20 kHz	1	1310
	2	1305
	3	1308

(e)

f_{sw}	#	V_M (V)
2 kHz	1	1316
	2	1316
	3	1324

(f)

Figure 3-12. Recorded HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of DUT #3 at f_{SW} of (a) 1 MHz, (b) 500 kHz, (c) 200 kHz, (d) 100 kHz, (e) 20 kHz and (f) 2 kHz. The $BV_{DYN\text{-}SW}$ of three DUTs tested in each condition are listed below the waveform. The $BV_{DYN\text{-}SW}$ shows f_{SW} dependence in (a)-(c) but not in (d)-(f).

Table 3-4. Testing Conditions for *DUT #3*

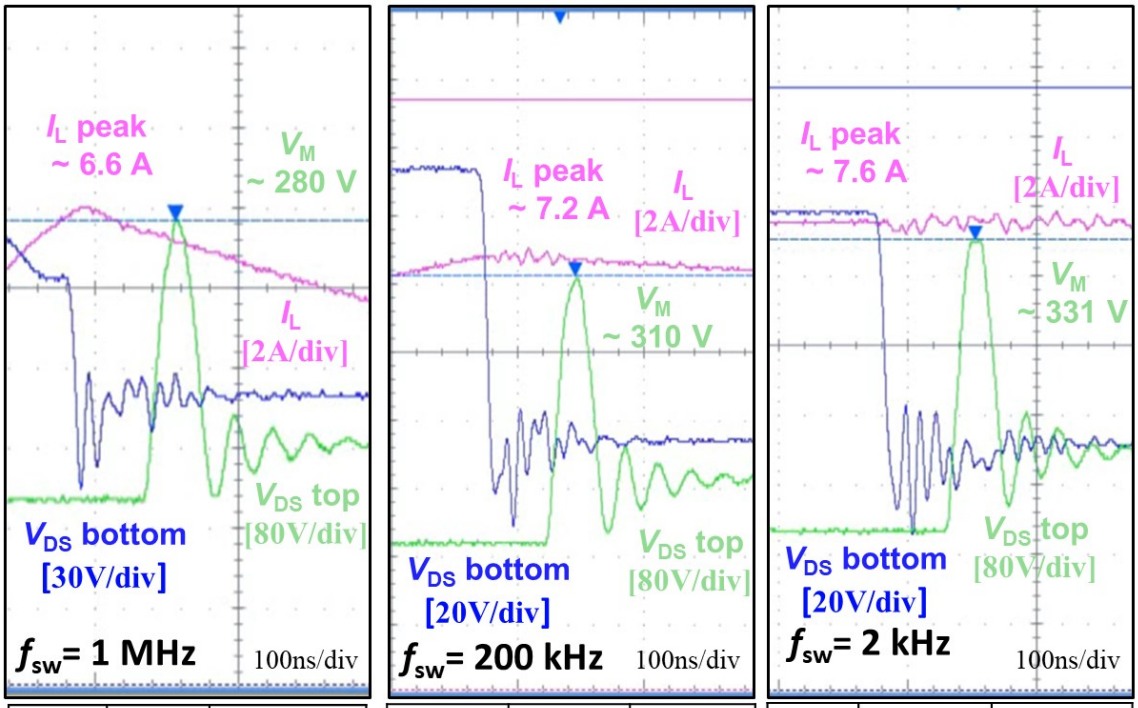
f_{sw}	Duty Cycle	L_M (μH)	R_{Load} (Ω)	V_{BUS} at failure (V)	$BV_{DYN\text{-}SW}$ (V)
1 MHz	0.12	1.0	5	~300	~1050
500 kHz	0.12	2.1	5	~330	~1190
200 kHz	0.12	8.6	5	~400	~1265
100 kHz	0.12	20.0	5	~400	~1310
20 kHz	0.12	110.0	5	~370	~1310
2 kHz	0.12	1200	5	~440	~1320

C. DUT #3

Figure 3-12 shows the HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of *DUT #3* under six different f_{sw} from 2 kHz to 1 MHz. The testing conditions are summarized in Table 3-4. The peak I_L at the DUT failure (or the amount of inductive energy) is not necessarily to be the same, as it is determined by the DUT BV and V_{BUS} when the device failure occurs. Variations in BV and V_{BUS} will influence the I_L peak value upon failure. From Figure 3-12(a)-(c), a $BV_{DYN\text{-}SW}$ drop from ~1265 V to ~1050 V is observed when f_{sw} increases from 200 kHz to 1 MHz. However, interestingly, when f_{sw} is below100 kHz, the $BV_{DYN\text{-}SW}$ becomes quite stable at ~1310 V (Figure 3-12(d)-(f)), which is close to the DUT #3's $BV_{DYN\text{-}SIN}$ extracted from the single-pulse UIS test as shown in Figure 3-5(c).

D. DUT #4

Figure 3-13 shows the HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of *DUT #4* under three f_{sw}. The testing conditions are summarized in Table 3-5. The average $BV_{DYN\text{-}SW}$ are 300 V at 1 MHz, 315 V at 200 kHz and 332 V at 2 kHz. Overall, a large variation of ~40 V is observed in the $BV_{DYN\text{-}SW}$ of three devices measured at 1 MHz and 200 kHz. Different from the f_{sw}-dependent behavior of *DUT #3*, the $BV_{DYN\text{-}SW}$ of *DUT #4* exhibits a monotonically decreasing trend with increasing f_{sw}. Besides, the $BV_{DYN\text{-}SW}$ are all much smaller than the $BV_{DYN\text{-}SIN}$ of 390 V (Figure 3-5(d)). Even at low f_{sw} of 2 kHz, the $BV_{DYN\text{-}SW}$ (332 V) is still 60 V lower.



f_{sw}	DUT	V_M (V)
1 MHz	1	280
	2	310
	3	310

(a)

f_{sw}	DUT	V_M (V)
200 kHz	1	336
	2	295
	3	310

(b)

f_{sw}	DUT	V_M (V)
2 kHz	1	335
	2	331
	3	330

(c)

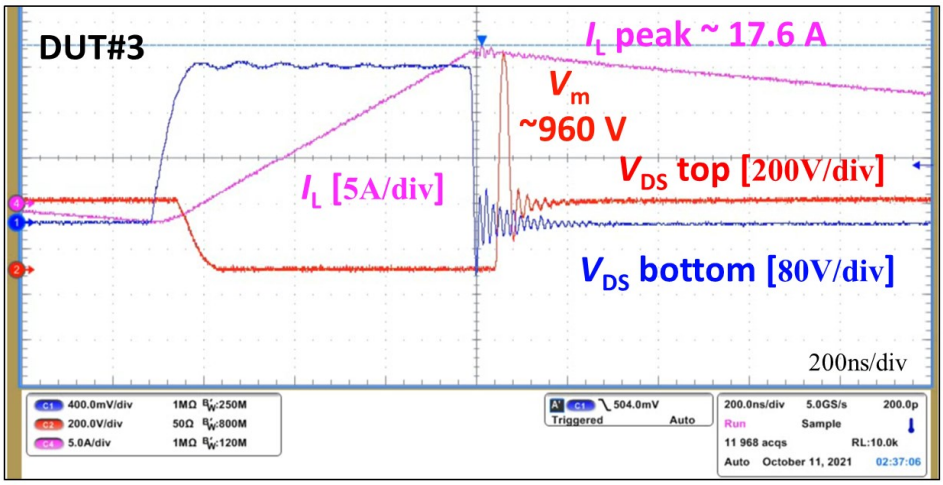
Figure 3-13. Recorded HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of DUT #4 at f_{SW} of (a) 1 MHz, (b) 200 kHz and (c) 2 kHz. The $BV_{DYN\text{-}SW}$ of three DUTs tested in each condition are listed below the waveform.

Table 3-5. Testing Conditions for *DUT #4*

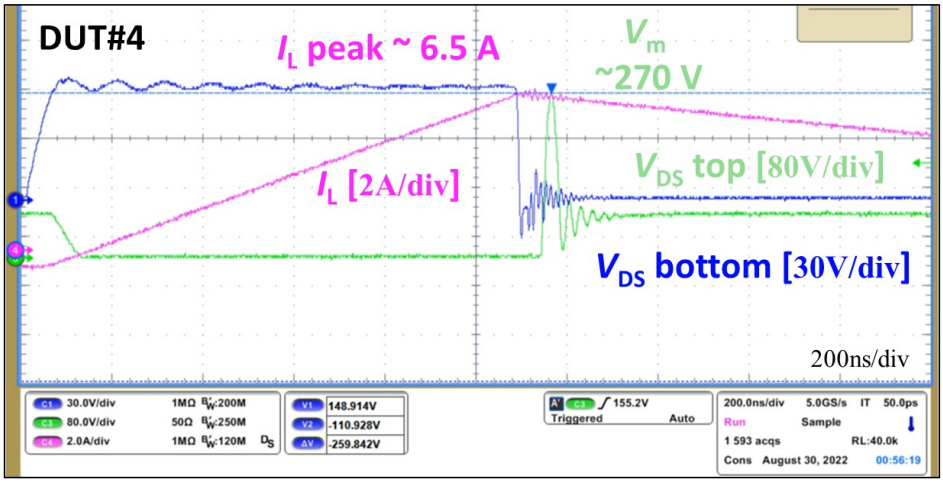
f_{sw}	Duty Cycle	L_M (μH)	R_{Load} (Ω)	V_{BUS} at failure (V)	$BV_{DYN\text{-}SW}$ (V)
1 MHz	0.12	1.0	5	70~75	~300
200 kHz	0.12	8.6	5	70~78	~315
2 kHz	0.12	920.0	5	~73	~332

3.3 Analysis of Degradation and Failure Mechanisms

In *DUT #3* and *#4*, the f_{sw} dependent $BV_{DYN\text{-}SW}$ and the considerable distinction between $BV_{DYN\text{-}SW}$ and $BV_{DYN\text{-}SIN}$ suggest additional degradation mechanisms at high f_{sw}. To identify the dominant parametric shifts and device degradations, long-term HFOT is carried out on DUT #3 and #4. In the long-term HFOT test, the peak V_{DS} is reduced so that the HFOT can be run sufficiently long (over 15 minutes) without DUT catastrophic failure, and the DUT degradation can be identified by post-stress characterization. The f_{sw} is set as 200 kHz and the peak V_{DS} is kept at ~70% of the $BV_{DYN\text{-}SIN}$ of each DUT, i.e., 960 V for DUT #3 and 270 V for *DUT #4*. Figure 3-14 shows the HFOT waveforms in the long-term stressing tests for both devices.



(a)

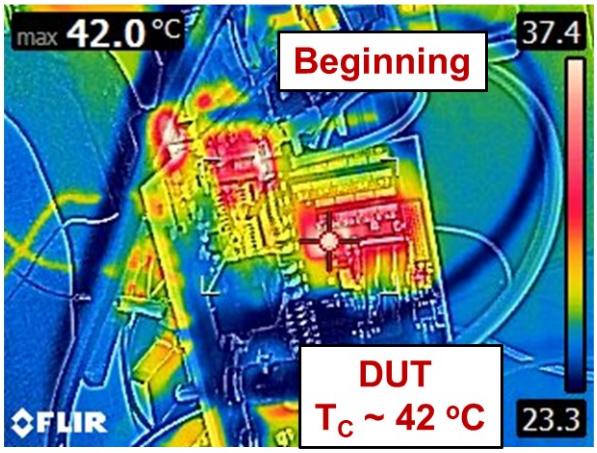


(b)

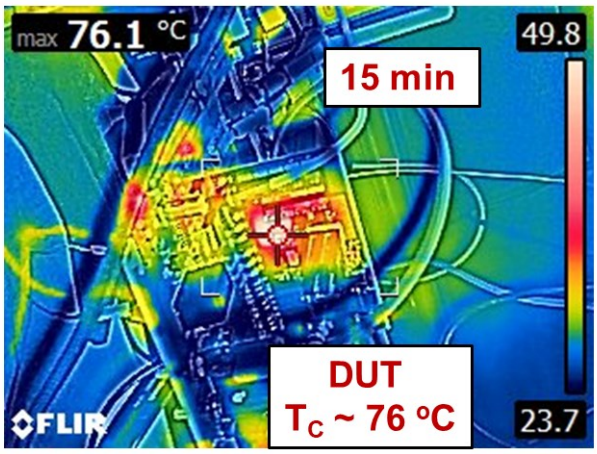
Figure 3-14. Illustration of waveforms of the long-term HFOT on (a) DUT #3 and (b) DUT #4. The f_{sw} is 200 kHz and the V_M is 70 % of $BV_{DYN\text{-}SIN}$.

3.3.1 Drastic R_{ON} Shift in DUT #3

As the long-term HFOT prolongs, the DUT's T_C is tracked by thermal camera imaging. T_C is only ~ 40 ºC (Figure 3-15(a)) at the beginning of the test but increases to > 75 ºC (Figure 3-15(b)) after 15 minutes of continuous switching. The rise in T_C indicated significant power loss elevation, which may be due to the R_{ON} drift. The DUT #3 is characterized on curve tracer right after the 15 minutes HFOT, revealing a over 30 times higher R_{ON} increase (i.e., R_{ON} over 2 Ω as compared to the initial state of < 70 mΩ) (Figure 3-16(a)). Unlike the well-known dynamic R_{ON} phenomena, which usually recovers in μs [108], the recovery of this R_{ON} degradation remains slow after days and could not recover to the initial state after 5 days of relaxation.



(a)



(b)

Figure 3-15. Recorded T_C (a) at the beginning of the HFOT and (b) after 15 minutes HFOT tests for DUT #3.

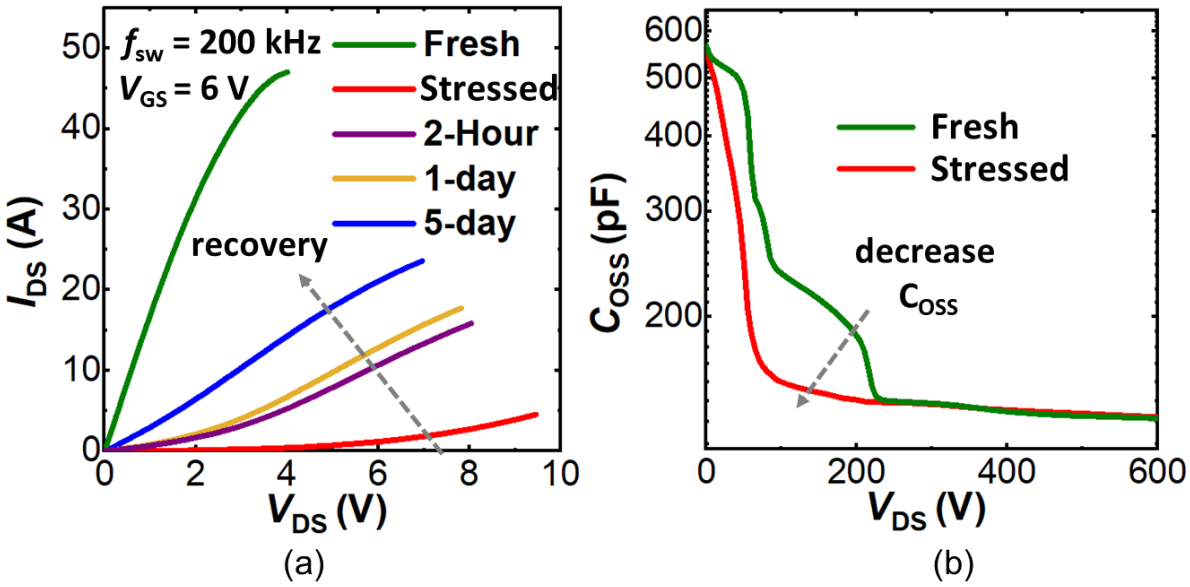


Figure 3-16. (a) R_{ON} shift in DUT #3 after 15 minutes, 200 kHz HFOT and its recovery up to 5 days. (b) C_{OSS} drift after 15 minutes, 200 kHz HFOT.

The *DUT #3*'s C_{OSS} also shows significant shifts after the 15 minutes HFOT (Figure 3-16(b)). In a fresh DUT, its C_{OSS}-V_{DS} characteristics show staircase features, which signify the successive depletion of the two-dimensional electron gas (2DEG) channel with the aid by various field plates [109]. The stressed DUT, however, show no such signatures in the C_{OSS}-V_{DS} characteristics and a quick depletion at low V_{DS}. This suggests significantly fewer 2DEG in the channel, which could be due to the severe electron trapping in the passivation, the interface between passivation and AlGaN, and/or in the buffer layer. This severe electron trapping is believed to be induced by the OFF-state overvoltage stress in the continuous HFOT [110].

The f_{sw} of the long-term HFOT is then reduced to 100 kHz and 2 kHz with the same 960 V peak V_{DS}. To make a fair comparison, the total testing time in these two tests are extended to match the total switching cycles in the 200 kHz HFOT. Testing results show a much smaller R_{ON} degradation in lower f_{sw} test (Figure 3-17(a) and (b)): ~ 4 times R_{ON} increase under 100 kHz and minimal R_{ON} drift at 2 kHz. These results agree with prior reports on the SP-HEMT parametric shifts in repetitive overvoltage stress at low f_{sw} (a few kHz), where relatively small R_{ON} shift is observed and it can recover in a short time [102], [111]. The alleviated R_{ON} shift in low-f_{sw} overvoltage switching can be explained by the prolonged time in each cycle for de-trapping, yielding less accumulation in trapped electrons.

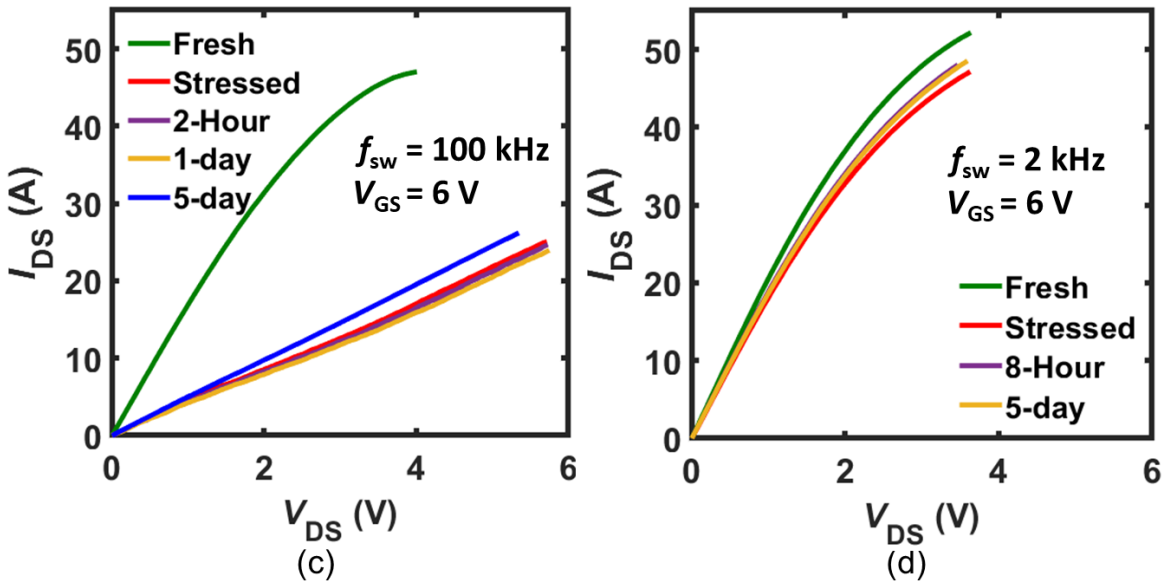


Figure 3-17. R_{ON} drift and recovery for 15 minutes, (c) 100 kHz and (d) 2 kHz HFOT on DUT #3.

As a comparison, *DUT #1* and *#2* are also stressed in the HFOT with 200 kHz and the peak V_{DS} at 70% of $BV_{DYN\text{-}SIN}$. After 30 minutes of HFOT stress, both DUTs are measured on the curve tracer and both show almost no change in R_{ON} (Figure 3-18).

The comparison between *DUT #3* and *DUT #1/#2* reveals the strong correlation between the drastic, nearly unrecoverable R_{ON} degradation and the f_{sw}-dependent $BV_{DYN\text{-}SW}$, both occurring at high f_{sw}. This relation can be understood from the electrothermal viewpoint. The drastic R_{ON} increase ramps up the conduction loss and deteriorates the thermal stress. As V_{DS} further increases, the more severe carrier trapping amplifies the increases in R_{ON} and thermal stress. This positive feedback finally leads to the premature thermal runaway before the electrical boundary ($BV_{DYN\text{-}SIN}$) is reached.

The critical role of thermal factors in the *DUT #3* failure is confirmed by the HFOT test with a lower current. By increasing the L_{air} value from 300 nH to 1 µH (two 2929SQ-501 putting in series), less current is required to produce the same peak V_{DS}, which can alleviate the thermal stress. The *DUT #3*'s failure waveform and the extracted $BV_{DYN\text{-}SW}$ are shown in Figure 3-19, revealing at least 80 V higher $BV_{DYN\text{-}SW}$ as compared to the result shown in Figure 3-12. This validates that, despite the severe R_{ON} degradation, the suppressed thermal failure allows the DUT's $BV_{DYN\text{-}SW}$ getting closer to $BV_{DYN\text{-}SIN}$. The thermal failure of *DUT #3* is also confirmed by the

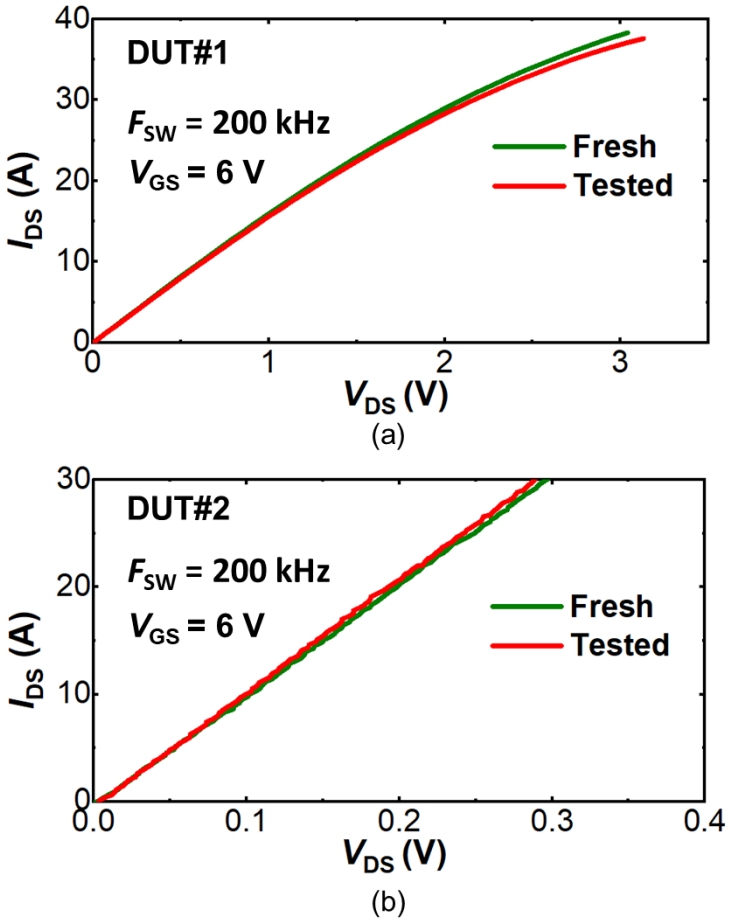


Figure 3-18. R_{ON} drift of (a) DUT#1 (b) DUT#2 after 30 minutes, 200 kHz HFOT at 80% of $BV_{DYN\text{-}sin}$, showing minimum R_{ON} increase.

$BV_{DYN\text{-}SW}$ measurement at a higher T_C of 100 ºC before the measurement starts. The $BV_{DYN\text{-}SW}$ is found to decrease from 1265 V to 1200 V, as the initial high T_C accelerates the thermal runaway. In contrast, the $BV_{DYN\text{-}SW}$ of *DUT #2* is found to be unchanged at a higher initial T_C, validating the electrical failure of *DUT #2*.

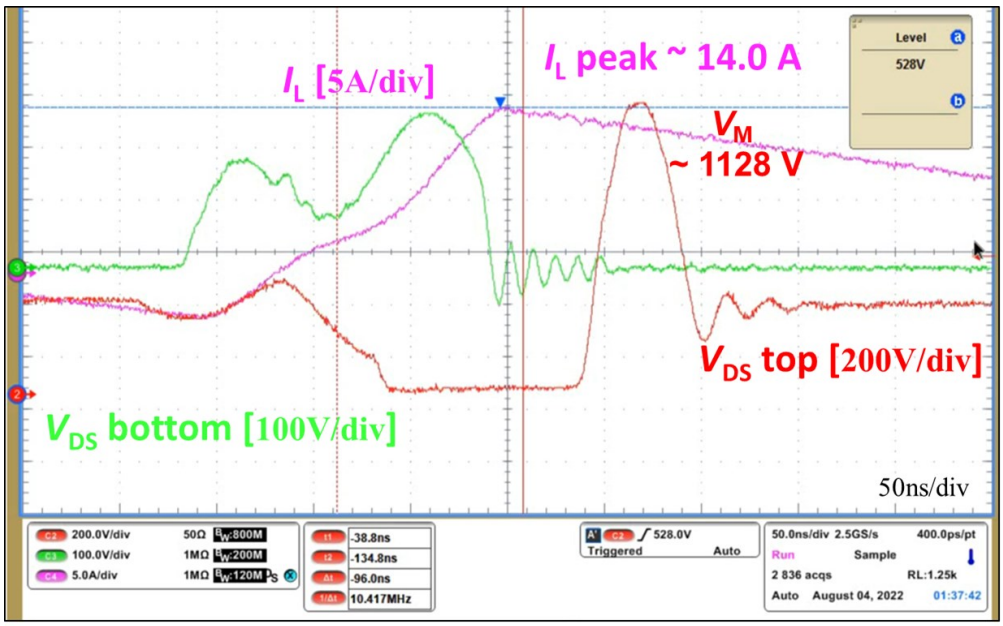


Figure 3-19. Recorded HFOT waveforms and extracted $BV_{DYN\text{-}SW}$ of DUT#3 with L_{air} = 1 µH at f_{sw} = 1 MHz. The $BV_{DYN\text{-}SW}$ is 80 V higher than that obtained with L_{air} = 300 nH.

3.3.2 Off-state Leakage Current Degradation

Along with the long-term HFOT on *DUT #4*, device characteristics are comprehensively measured on curve tracer after every 15 minutes of HFOT. Figure 3-20(a) shows the output

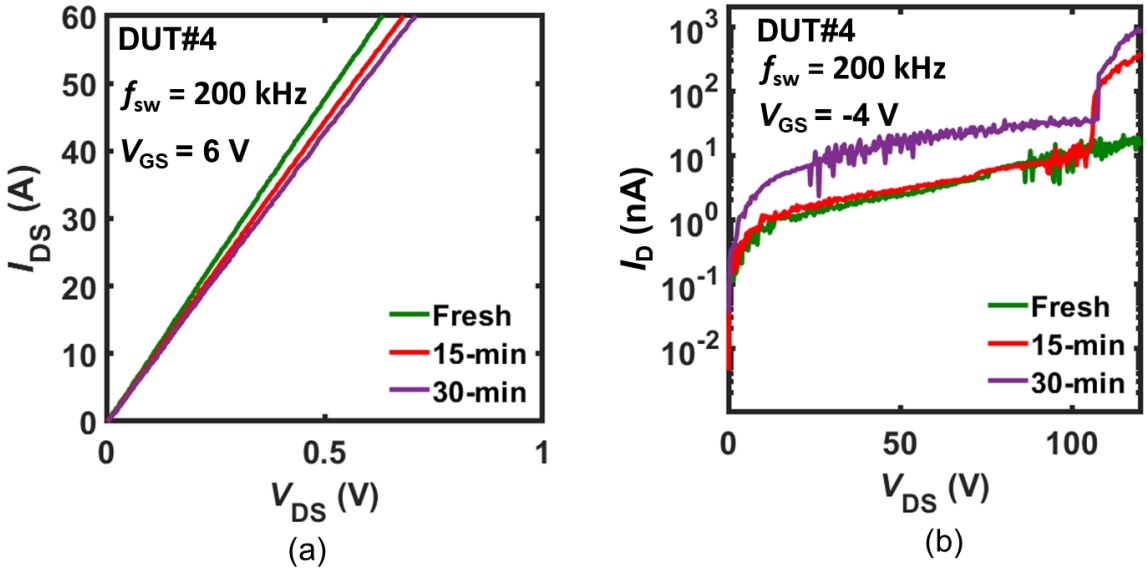


Figure 3-20. (a) Output I-V characteristic and (b) OFF-state I-V characteristics of the DUT #4 after the 15 minutes and 30 minutes of HFOT at f_{sw} of 200 kHz and the peak V_{DS} of 270 V.

characteristics, revealing an increase in R_{ON} by ~ 15% after 30 minutes of HFOT. Such a small increase is not expected to lead to thermal runaway in the HFOT. Instead, a major degradation is observed in the *DUT #4*'s OFF-state I-V characteristics. As shown in Figure 3-20(b), after 15 minutes of HFOT, while the I-V curve is almost unchanged at low V_{DS}, the leakage current shoots up at 100 V V_{DS}. Such a current hump is very similar to the I-V signature reported in [105] and can be attributed to a trap-filling mechanism.

In fact, similar trap-filling signatures in I-V characteristics have been widely reported as the trap-assisted space-charge-limited-current (SCLC) mechanism [85], [112], [113], [86]. In an OFF-state I-V sweep, trap states in the buffer layer are gradually occupied by carriers. At the V_{DS} that all trap states in a local region are filled, i.e., the trap-filled-limited voltage (V_{TFL}), a sudden increase in the leakage current occurs as the excess carriers cannot be further trapped and all contribute to leakage current. Such trap states could come from the intrinsic defects in the buffer layer or the extrinsic defects created in the HFOT stress [112]. For either origin, the observation of SCLC current suggests the severe trapping in the DUT as the HFOT prolongs.

In the devices with the SCLC leakage current, the V_{TFL} is usually regarded as their effective breakdown voltage [85], [105], as orders of magnitude higher leakage current would be present at higher V_{DS}. Hence, the *DUT #4* suffers from a large reduction of its effective *BV* during the HFOT test. After 30 minutes HFOT and the following characterization, the DUT is put back in the HFOT. Catastrophic failure occurs within 90 seconds at the peak V_{DS} of only 270 V.

Different from *DUT #3*, the f_{sw} dependent $BV_{DYN\text{-}SW}$ of *DUT #4* originates from the degradation in the drain leakage current and the effective *BV*. A degradation tracking test with 2 kHz f_{sw} and 270 V V_{DS} is then performed. Comparing to the 200 kHz test shown in Figure 3-20(b), the DUT *#4* does not see degradation until 7.5 hours of the 2 kHz test (Figure 3-21). Overall, the degradation of DUT #4 seems to depend on the pulse number. However, since the degradation mode is only present in one type of DUT, we didn't perform extensive further characterizations to convincingly verify this hypothesis.

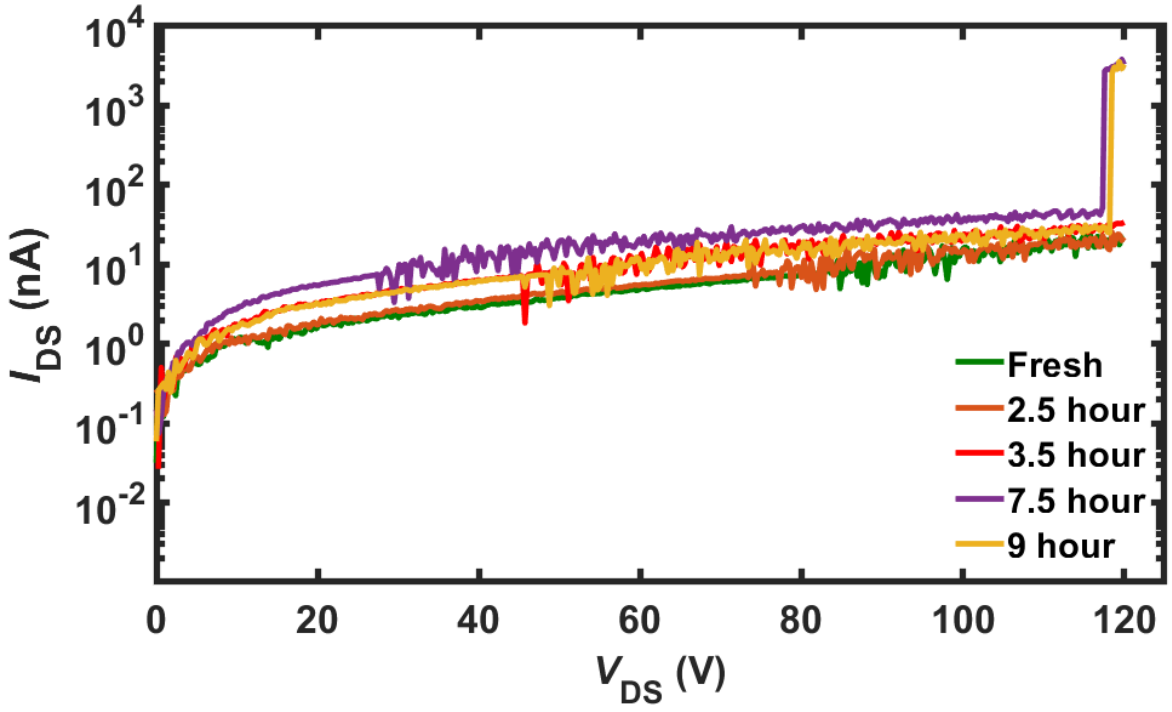


Figure 3-21. OFF-state I-V characteristics of the DUT #4 in 2 kHz overvoltage test

The higher f_{sw} HFOT causes more severe buffer trapping and degradation. which can explain the overall decreasing trend in $BV_{DYN\text{-}SW}$ in Figure 3-13. Meanwhile, the trap-filled device region becomes very unstable when it is subject to a bias higher than its effective BV ($V_{TFL} \sim 100$ V). This instability can explain the relatively large spread (over 40 V) in $BV_{DYN\text{-}SW}$ in each set of high f_{sw} tests as shown in Figure 3-13.

Note that the OFF-state I-V characteristics of *DUT #1-#3* are also examined when these DUTs are subject to the HFOT at 70% of their $BV_{DYN\text{-}SIN}$, revealing no degradations in these DUTs.

3.4 A Simple Test Method for GaN HEMT Overvoltage Robustness Qualification

From the discussions in prior sessions, DUT #1 and #2 show consistent $BV_{DYN\text{-}SW}$ at various f_{sw}, reflecting the intrinsic overvoltage boundary and margin. In addition, $BV_{DYN\text{-}SW}$ is consistent with $BV_{DYN\text{-}SIN}$ measured from the single-pulse UIS test with a similar *dv/dt*. This suggests the viability of using the simple UIS test to identify the intrinsic BV and overvoltage margin of GaN HEMTs in power switching.

DUT #3 and *#4* show nearly unrecoverable degradations in the HFOT at 70% of the $BV_{DYN-SIN}$, and these degradations are tightly correlated to their compromised BV_{DYN-SW} at high f_{sw}. In addition to the reduced overvoltage margin, the revealed degradations in R_{ON} and BV would adversely impact the DUTs' normal operations. From the application point of view, these devices show inferior ruggedness in overvoltage switching.

The degradations in *DUT #3* and *#4* are possibly due to severe trapping; further studies are desirable to unveil the trap locations and origins. However, for device users, it is more important to develop an easy-to-implement qualification tests that can filter out the devices with inferior ruggedness before deploying them into high-f_{sw} converters and systems.

The prior sessions have shown that the converter-based HFOT setup is a powerful tool for this qualification test. However, it is relatively complicated. Here we propose the use of repetitive UIS tests with the peak voltage up to ~70% of the $BV_{DYN-SIN}$ for a faster qualification test and detail the design considerations of this test. As the UIS test is essential in determining the $BV_{DYN-SIN}$, it would be very convenient if the same test setup can be used for device qualification test.

The major consideration for designing such a repetitive UIS test is to achieve high f_{sw} while maintaining stable peak V_{DS}, i.e., the V_M, in every cycle. The key parameters in the UIS test include the L_{loop}, the inductor charging time of t_{ON}, input bus voltage V_{BUS}, and V_M. The correlation between these parameters and the current constraint can be derived as

$$\frac{1}{2}C_{OSS}V_m^2 = \frac{1}{2}L_{loop}I^2 = \frac{L_{loop}}{2}\left(\frac{V_{BUS}t_{on}}{L_{loop}}\right)^2 \qquad (3-1)$$

$$0.7BV_{DYN-SIN} \approx V_m = V_{BUS}t_{on}/\sqrt{L_{loop}C_{OSS}} \qquad (3-2)$$

$$V_{BUS}t_{on}/\left(L_{loop} + R_{on}t_{on}\right) \le I_{rate} \qquad (3-3)$$

where I_{rate} is the DUT's rated current. From the discussion in section 3.1, to upscale f_{sw}, t_{on} needs to be minimized, which requires the use of relatively large V_{BUS} and small L_{loop}. Whereas, the selection of V_{BUS} and L_{loop} is constrained by the device rated current, as illustrated in (3-3). In addition, the high V_{BUS} will increase the amplitude in the residual resonance, extending the time of *phase IV* in the UIS waveform.

Note that, even with carefully selected components, the f_{sw} of the repetitive UIS tests is limited by the time needed for damping the surge energy (i.e., *phase III* and *IV*) and managing the DUT self-heating. Particularly, in the reverse conduction phase, considerable heat dissipation is expected. Our experience suggests that, for $BV_{DYN-SIN}$ > 1000 V, it is difficult to push the f_{sw} of the repetitive UIS test to exceed 200 kHz.

Considering these trade-offs, the f_{sw} in the repetitive UIS qualification test is set to 200 kHz with the L_{loop} value of 300 nH and V_{BUS} of 30 V. Figure 3-22 shows the example waveforms of the repetitive UIS qualification test on DUT #3 with the peak V_{DS} kept at 960 V in each cycle.

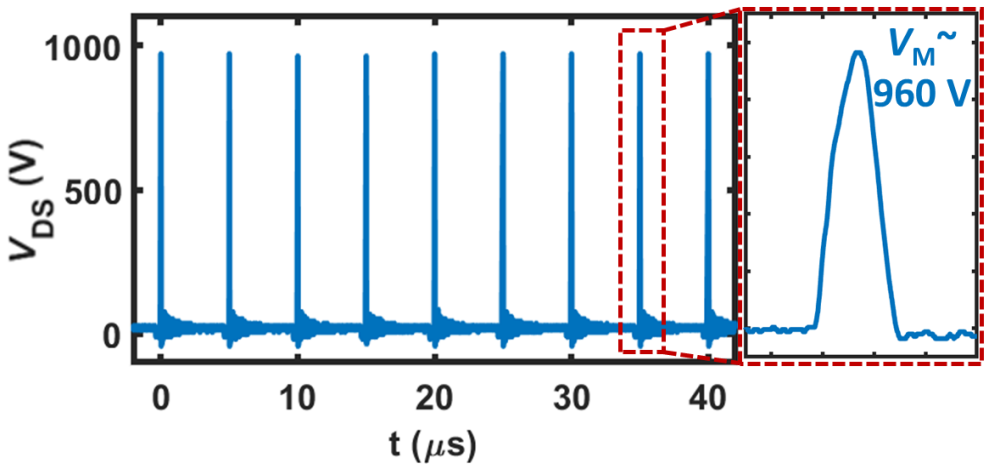


Figure 3-22. V_{DS} waveforms of the repetitive UIS screening test of DUT #3 at 200 kHz.

Figure 3-23 shows the repetitive UIS qualification test results of DUT #3 and #4. Due to the relatively high T_C (around 100 °C) on *DUT #3* in the qualification test, it only runs for 10 minutes, after which a twice R_{ON} increase is already shown (Figure 3-23(a)). Similar qualification test is performed on *DUT #4*. The leakage current and *BV* degradation are also well replicated, as shown in Figure 3-23(b). Similar repetitive UIS qualification tests on *DUT #1* and *#2* show very similar results to their HFOT at 200 kHz, without the observation of any significant and unrecoverable degradations. These results validate the viability of using the repetitive UIS test as an easy-to-implement and fast qualification method.

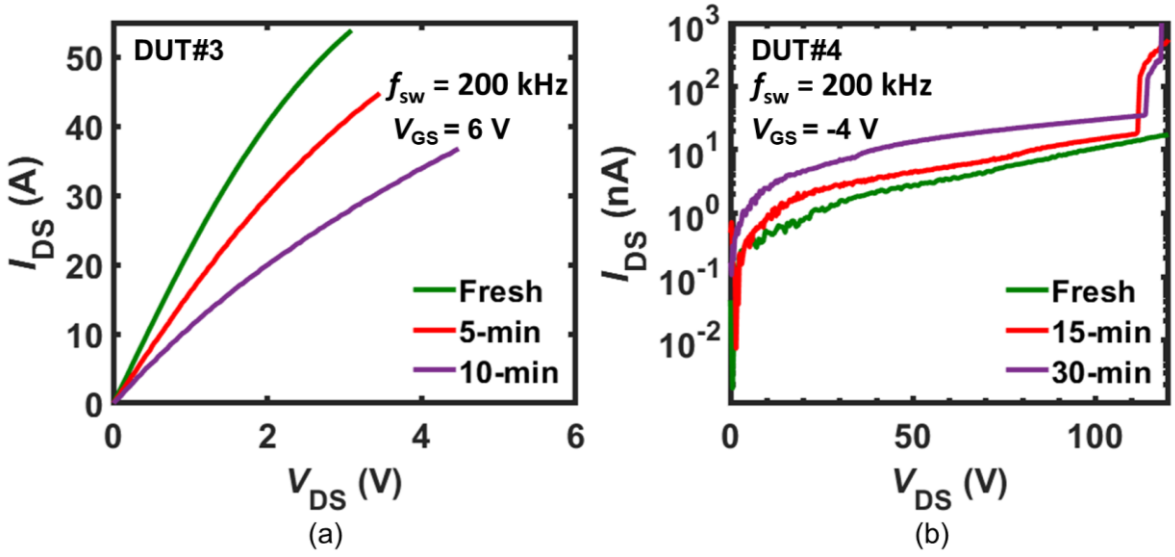


Figure 3-23. (a) The shift in the output characteristics of DUT #3 as the UIS screening test prolongs. (b) The shift in the OFF-state I-V characteristics of DUT #4 in the UIS screening test.

3.5 Discussion on GaN HEMT R_{ON} Degradation in High Frequency Switching

From the HFOT results and failure analysis presented in section 3.2 and section 3.3, the positive shift of device R_{ON} is the most common signature of GaN HEMT degradation under the transient overvoltage conditions that usually occur in application scenarios. The study on the R_{ON} shift in GaN HEMT has lasted for more than a decade, and the origin is typically related to the charge trapping which depletes the carriers in the 2DEG channel. Some behavior models of the charge trapping have been built up in [114], [115]. In these studies, charge trapping is introduced by DC bias, hence in the behavior model only two variables are included: the voltage and the temperature. However, in practical switching scenario, more parameters need to be considered in the modeling of dynamic R_{ON} evolution such as the switching frequency and voltage pulse width. This section discusses the key parameters that may impact the charge trapping in GaN HEMTs and the possible locations of the trapped electrons introduced in the HFOT.

3.5.1 R_{ON} Evolution's Dependency on Circuit Parameters

Switching frequency and peak V_{DS} value: the impact from f_{sw} has been shown in Figure 3-17, a higher f_{sw} allows less de-trapping time that brings severer accumulation of trapped charges hence

a faster R_{ON} degradation. When the peak V_{DS} in the 200 kHz HFOT reduces from 960 V to 900 V for *DUT #3*, DUT R_{ON} shows a much smaller increase (Figure 3-24) as the trapping effect is weakened at lower V_{DS}.

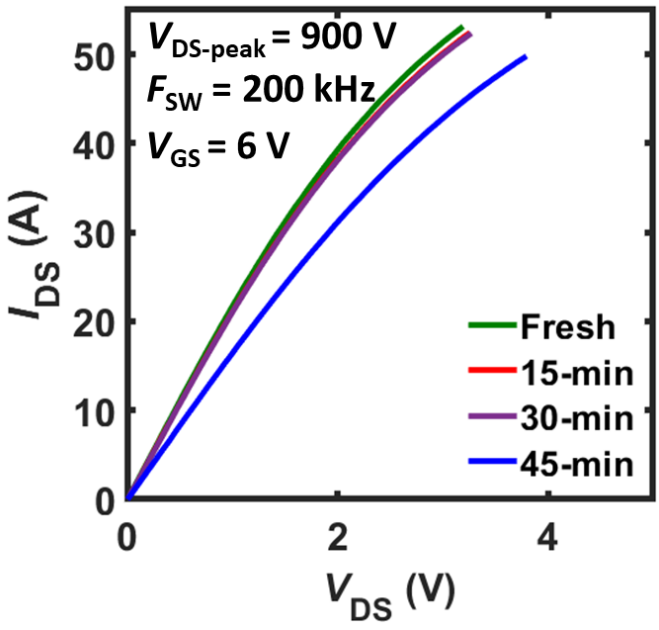


Figure 3-24. DUT #3 R_{ON} shift after 45 minutes of 900 V V_{DS} peak HFOT at 200 kHz.

Pulse width and temperature: The pulse width refers to the duration of the voltage overshoot. Theoretically, trapping effect is enhanced by longer pulse width [101], and shows a non-monotonic relationship with temperature, as higher temperature enhances the leakage [114] but provides kinetic energy that in favors of the de-trapping as well [116]. Due to the complexity of the trapping mechanics, a complete physics-based mathematic model that includes all parameters is very challenging to build. Instead, a mission profile-based test-to-fit modeling method is recommended. Section 3.6 will present the exploration on quantifying the dynamic R_{ON} evolution using the first-principle, physics-based lifetime projection modeling.

3.5.2 Location of Traps

It has been widely reported that charge trapping usually occurs at two locations in GaN HEMT: the buffer layer and interface between the passivation layer and the AlGaN barrier (Figure 3-25) [42], [110]. The primary trapping location is determined by device operation transient. According to [110], hot electron trapping in the passivation layer usually occurs during the GaN HEMT hard-switch semi-on, and buffer trapping usually occurs during the off-state DC bias.

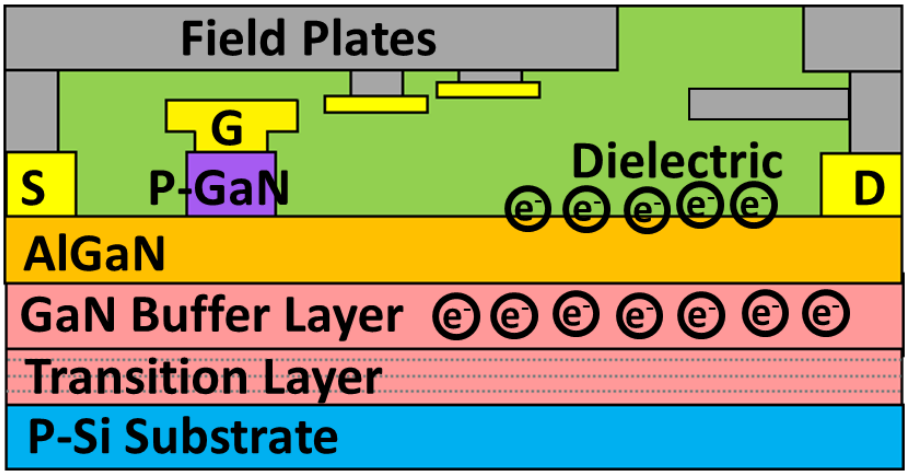
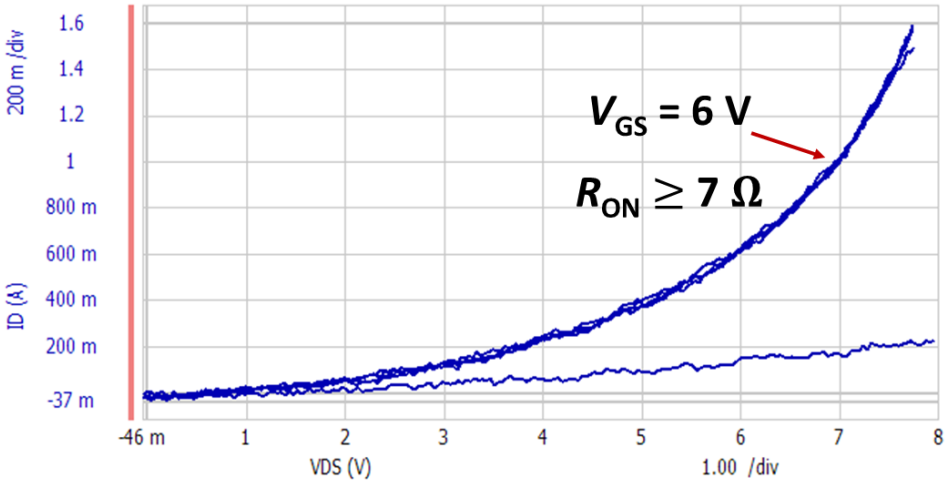


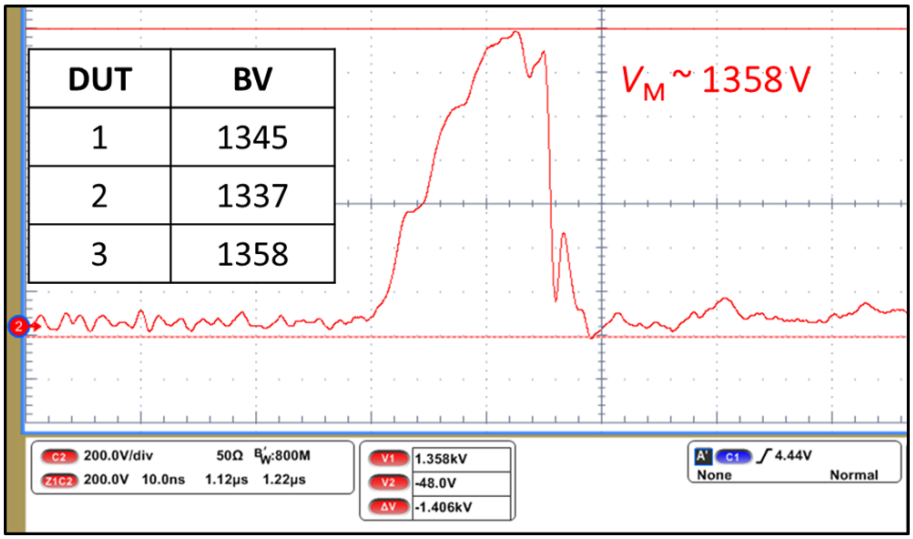
Figure 3-25. Schematic of a GaN HEMT showing the electron trapping in the GaN buffer layer and the interface between passivation layer and AlGaN barrier.

To determine the trapped charge location in the HFOT test, further investigation is conducted on *DUT #3*. The DUT is first put in the 960 V, 200 kHz HFOT test to induce an over 100 times R_{ON} increase (Figure 3-26(a)), then DUT is put back on the UIS test to measure the $BV_{DYN\text{-}SIN}$. Since the recovery is slow (Figure 3-16 and Figure 3-17), the majority of the trapped electrons remain in the DUT in the UIS test. Figure 3-26 shows the $BV_{DYN\text{-}SIN}$ of the degraded DUT. Compared to the fresh ones (Figure 3-5(c)), the $BV_{DYN\text{-}SIN}$ merely decreases by < 20 V (Figure 3-26(b)). However, based on the findings in section 2.3, a drastic decease of the $BV_{DYN\text{-}SIN}$ is expected with trapped charges in the buffer layer, hence it can be inferred that the majority of the charge trapping occurs in the interface between the passivation layer and front barrier.

Note that the GaN HEMT electron trapping locations have been reported in [110], where the authors investigate the charge trapping in off-state and semi-on state stress and concludes that the electron trapping in off-state mainly occurs in the GaN buffer layer. The off-state charge trapping location in [110] is different from the claim in this dissertation work as commercial and academic devices have distinct processing flows that can form different main leakage paths; in addition, the testing conditions in HFOT are essentially different with higher peak V_{DS} compared to the pulsed bias test in [110]. In the charge trapping modeling process in section 3.6, only the trapping effect in the passivation layer interface is considered.



(a)



(b)

Figure 3-26. (a) Output characteristics of DUT #3 showing the drastic R_{ON} increase. (b) UIS test waveforms of the degraded DUT #3. Minimal $BV_{SW\text{-}SIN}$ is shown.

3.6 Lifetime Projection of GaN HEMT Under High Frequency Overvoltage Switching

The work presented in section 3.4 can be further improved from two perspectives: a) device characterization is conducted off-line via the curve tracer for the degradation tracking, where the unavoidable delay (at a minimum of several minutes) from stopping the circuit operation to performing device characterization makes it challenging to capture the possible dynamic parametric shifts due to fast trapping effects. b) The studied overvoltage regime is over 50% higher than the device's rated voltage, which can only be accessed under rare occurrences, abnormal events in certain applications. While GaN HEMT degradation and lifetime projection in lower voltage regime are also key interests.

In this section, the above-mentioned gaps are addressed by in-situ monitoring the dynamic R_{ON} under repetitive overvoltage switching. An UIS test setup with in-situ R_{ON} measurement is developed [117]. The 100 V EPC GaN HEMTs are chosen as the *DUT #2* shows negligible R_{ON} shift in the HFOT with off-line characterization in section 3.4. Compared to the resistive hard-switching performed by EPC [118], this inductive switching system better emulates the overvoltage stress in practical applications. In this chapter, following results are highlighted: 1) zero catastrophic failure is observed in >1.5 billion switching cycles with overvoltage up to 150% of the device max rated voltage; 2) dynamic R_{ON} increase is the major device degradation under overvoltage switching with peak V_{DS} exceeding device rated value, the dynamic R_{ON} is accurately measured by the testing system; 3) a universal physics-based model is established to simulate the time evolution of dynamic R_{ON} for various V_M, which enables the lifetime projection for commercial GaN HEMTs under the continuous overvoltage switching.

3.6.1 Setup of High Frequency Repetitive UIS Test System with In-situ R_{ON} Monitoring

Figure 3-27 illustrates the circuit schematic of the UIS test with the voltage clipper. The main circuit consists of an air core inductor and the device under test (DUT) in series. During the test, the DUT is first turned on to charge the inductor. Then the DUT is turned off, during which the energy in the inductor is withstood by the DUT output capacitance (C_{OSS}) that triggers the transient drain voltage overshoot. In this work, the UIS test setup features the incorporation of an additional self-controlled voltage clipper circuit connected to the DUT for on-state V_{DS} measurement. Due to the high ratio between the maximum voltage (when DUT is turned-off) and minimum voltage (when DUT is turned-on) applied on the DUT, simply using a voltage probe to capture DUT on-state voltage drop would give inaccurate measurement results [119]. The function of the voltage clipper is that it isolates the high voltage bias from the measurement point during the DUT's off-state: the clipper MOSFET (STN3N45K3) is switched off and disconnects the Kelvin-sensed V_D from the DUT's drain. During the DUT's on-state, the clipper MOSFET is switched on, connecting the DUT drain to the measurement point. The $R_{DS(ON)}$ of the clipper MOSFET (3.3 Ω) is over 300 times smaller than the resistor (1 kΩ) connected in series. Based on the voltage divider equation, measured V_D that is used for in-situ dynamic $R_{DS(ON)}$ monitoring accounts for more than 99.7% of the DUT's on-state drain voltage. Therefore, the error due to the voltage drop across the clipper MOSFFET is minimal.

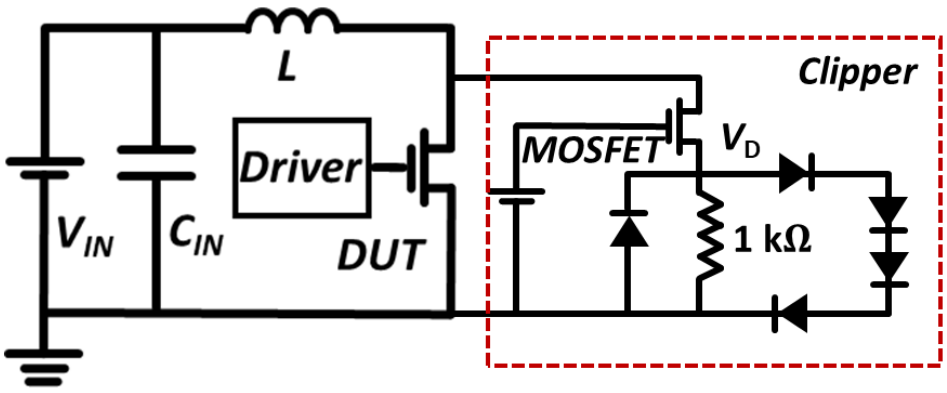


Figure 3-27. Circuit schematic of the repetitive UIS test with the voltage clipper marked in the schematic.

Figure 3-28 shows the hardware implementation of the repetitive UIS testing system. The DUT is EPC2218, a 100 V rated, 3.2 mΩ max enhancement-mode (E-mode) GaN HEMT (eGaN^{TM} FET) [120]. A prob card that accommodates the DUT footprints is plugged into the motherboard with all power loops. During the test, the DUT on-state drain voltage (V_D), source voltage (V_S), and source current (I_S) are measured via coaxial cables and current shunt, respectively. The off-state

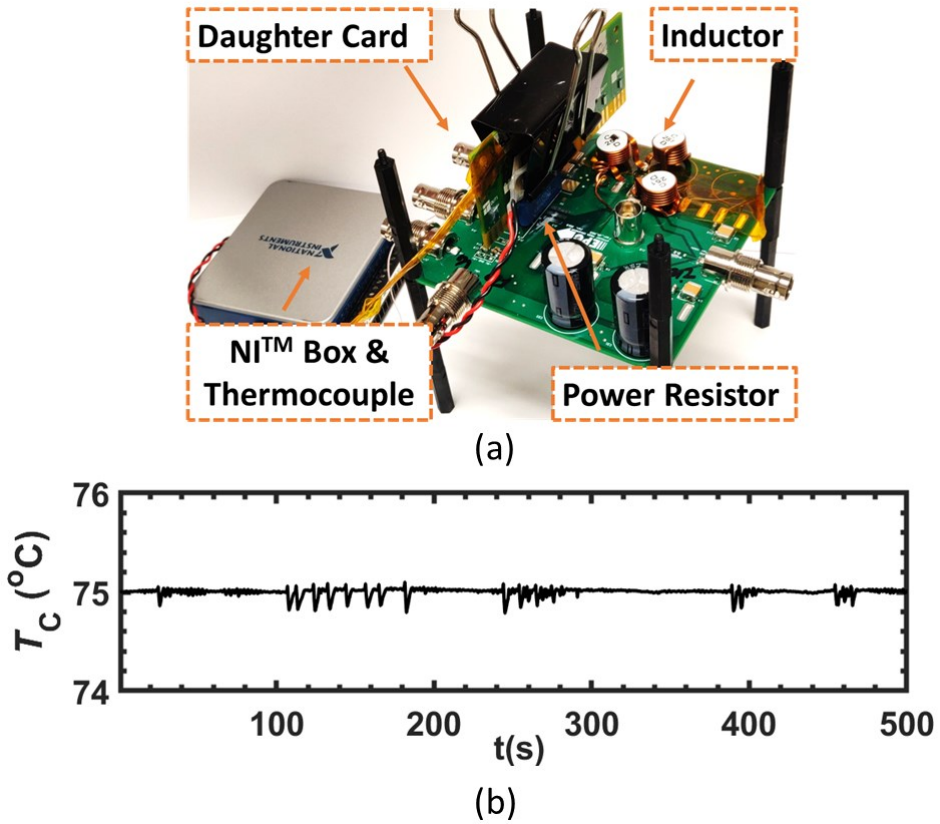


Figure 3-28. (a) Picture of the test system hardware. (b) T_C read from the thermocouple along with time.

drain-to-source voltage (V_{DS}) is measured by P6139B voltage probe. Note that from section 3.4, a switching frequency of ≥100 kHz is recommended to capture the GaN HEMT's full degradation in overvoltage switching. Hence, a small air core inductor value of 771 nH is used to push the repetitive UIS frequency to 100 kHz. The duty cycle is kept low at 6% to minimize the DUT self-heating. V_M is determined by the energy stored in inductor, and can be approximated by the formula given in section 2.2:

$$V_M = I_L\sqrt{L/C_{OSS}} = V_{IN}t\sqrt{1/LC_{OSS}} \qquad (3-4)$$

where t is the inductor charging time, L is the loop inductance, C_{OSS} is GaN DUT output capacitance, and V_{IN} is the input voltage. Since t is fixed by frequency and duty cycle, the $V_{DS,peak}$ in the UIS test is tuned by the value of V_{IN}.

To track the DUT degradation and stabilize the test condition, test automation features are added to the UIS system including an active temperature control and in-situ R_{ON} monitoring. A proportional-integral-derivative temperature control system is directly mounted on the backside of the DUT, with a TO-247 power resistor heating up the DUT and a NI™ Box to control the current flow through the power resistor. The DUT's case temperature (T_C) is calibrated by a thermocouple. When T_C appears higher than the set value, power through the resistor will be cut off to cool down the DUT. As shown in Figure 3-28(b), with this temperature controller, T_C of the DUT is maintained consistent at 75 °C throughout the entire experiment, with a maximum variation of only ~0.2 ºC. Note that the power dissipation on DUT during the test is less than 0.3 W. A 0.5 ºC/W junction-to-case thermal resistance [120] leads to less than 0.15 ºC difference between T_C and junction temperature (T_J). It should be noted that the change in T_C does not affect the accuracy of the voltage clipper, since V_D is far below the forward voltage drop of the four diodes in series (~ 2.8 V).

Figure 3-29 illustrates a cycle of UIS waveforms with a $V_{DS,peak}$ of 120 V. Each switching cycle consists of four phases: inductor charging (phase I), overvoltage resonance (phase II), DUT reverse conduction and inductor discharging (phase III), and residual resonance (phase IV). The detailed dynamics of DUT in these four phases have been explained in detail in [69]. Here we focus on the in-situ R_{ON} monitoring in phase I, as it is the newly added test component in this section.

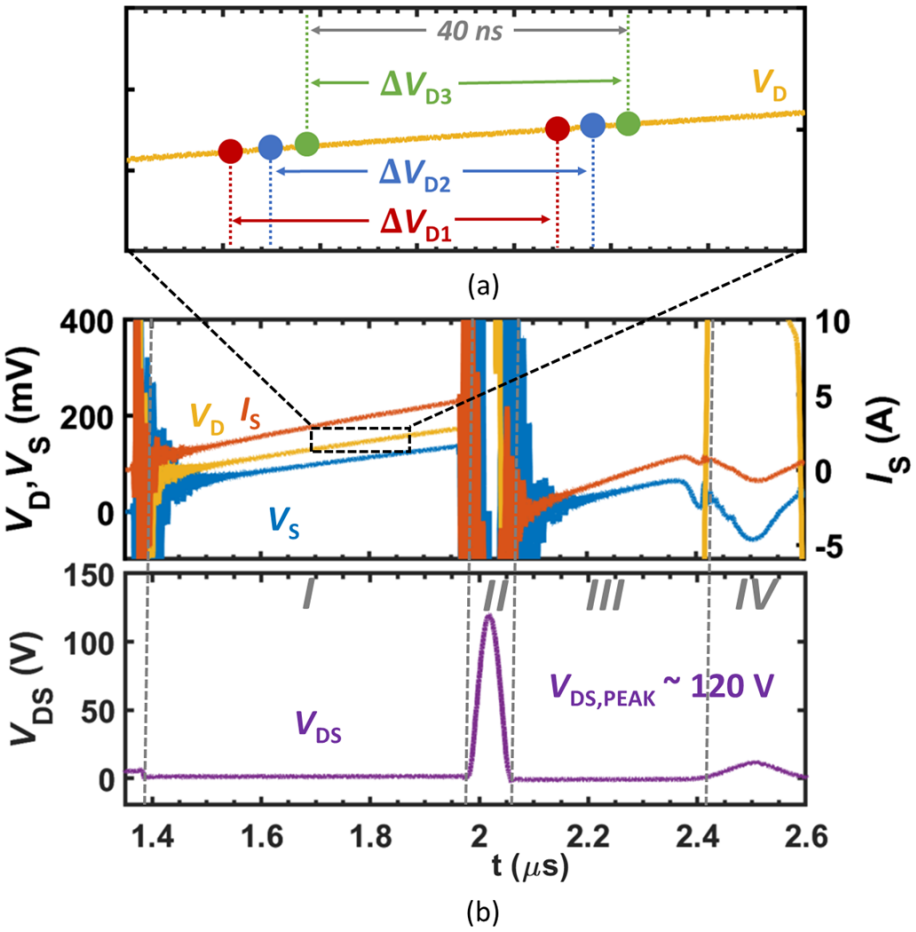


Figure 3-29. (a) Illustration of the data extraction for R_{ON} calculation. The time window between each pair of dots is 40 ns, while the interval between adjacent data point is 0.4 ns (not to scale). (b) Typical UIS test waveforms in experiments. Different phases in a UIS cycle are marked.

Theoretically speaking, the DUT's $R_{DS(ON)}$ can be calculated by the voltage and current at any time transient in phase I using the Ohm's law. However, in practical measurements, the settling effect of the voltage clipper leads to considerable background noises in the voltage measurement when running the test at higher frequencies with an inductive current [115]. To minimize the impact of such background noise, the incremental voltage and current (ΔV and ΔI) extraction approach is deployed to cancel out the background noise. The calculation process is illustrated in Figure 3-29(a). Using ΔV_D as an example. ΔV_D is extracted between pairs of data points (e.g., ΔV_{D1}, ΔV_{D2}, ΔV_{D3}) with the time difference between each pair being 40 ns. For each pair of ΔV_D, ΔV_S and ΔI_S, an $R_{DS(ON)}$ is calculated. Such paired data sampling is executed for 500 consecutive times with the interval between two adjacent sampling data being 0.4 ns, followed by an average applied to the 500 calculated R_{ON} for the final in-situ R_{ON}:

$$R_{ON} = \sum_{i=1}^{500} \left[\frac{\Delta V_{Di} - \Delta V_{Si}}{\Delta I_{Si}} \right] / 500 \qquad (3-5)$$

where ΔV_{Di}, ΔV_{Si} and ΔI_{Si} are incremental voltage or current at a selected 40 ns window. As a validation of this method, the extracted $R_{DS(ON)}$ value from a room-temperature single-event UIS test matches well with the datasheet value.

3.6.2 Testing Results of the R_{ON} Evolution

During the repetitive UIS test, all waveforms are periodically recorded every 2 minutes as controlled by a LabVIEW program. The recorded waveforms are processed by MATLAB for the dynamic $R_{DS(ON)}$ extraction based on (2). Figure 3-30 shows the extracted, in-situ monitored, dynamic $R_{DS(ON)}$ of the DUT in two UIS tests with $V_{DS,peak}$ of 120 V and 150 V, respectively. For

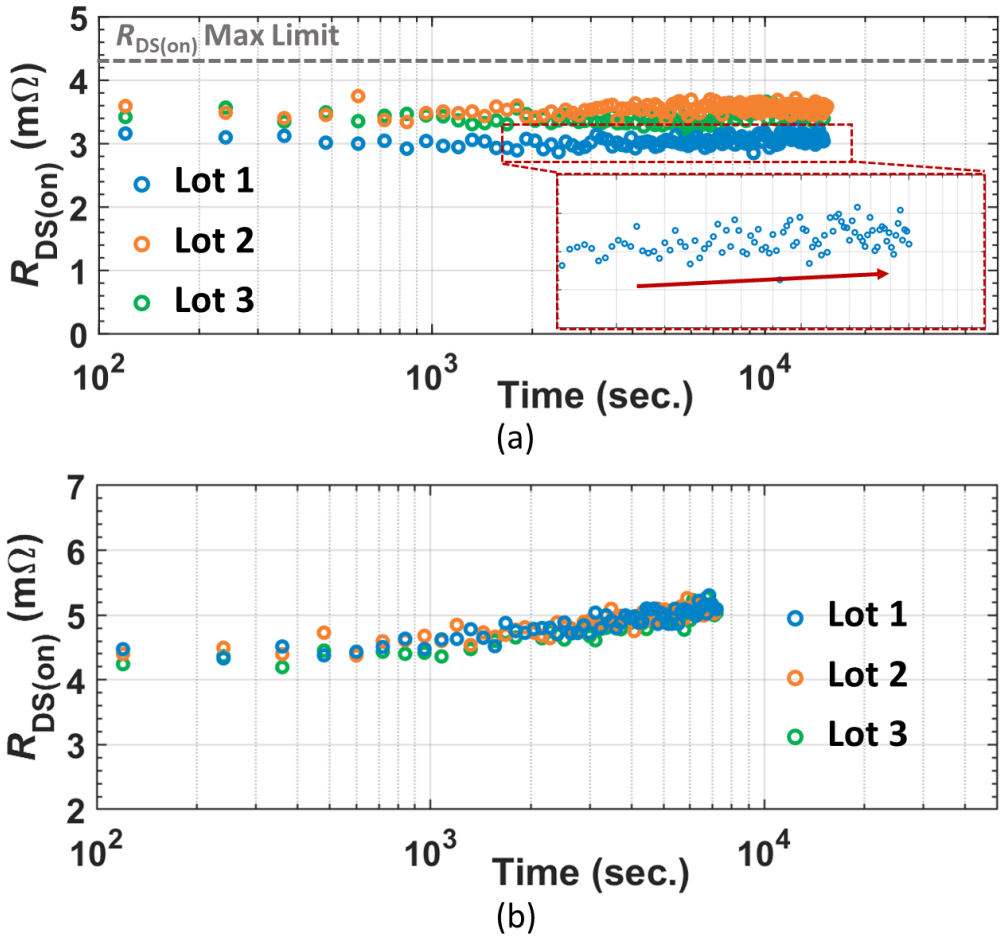


Figure 3-30. In-situ measured, dynamic R_{ON} of DUTs from three lots in the repetitive UIS test with $V_{DS,peak}$ of (a) 120 V and (b) 150 V.

each V_M, a total of 9 devices from 3 different lots (wafers) are tested. All three DUTs from each wafer behaved consistently. Hence, the testing results of one representative device from each lot are presented in the following discussions.

Figure 3-30(a) presents the dynamic R_{ON} evolutions of DUTs from three lots stressed continuously for more than 4 hours at 120 V $V_{DS,peak}$, which is equivalent of approximately 1.5 billion cycles. The initial dynamic $R_{DS(ON)}$ is around 3.2 mΩ at 75 °C. Note that the dynamic $R_{DS(ON)}$ is well below the max static $R_{DS(ON)}$ limit in datasheet (4.3 mΩ at 75 °C) by considering the temperature coefficient (1.35x) given by the datasheet [120].

From Figure 3-30(a), despite some small lot-to-lot variation, all DUTs showed a consistent small dynamic $R_{DS(ON)}$ drift well below the R_{ON} max limit. From the zoom-in view of the scatterplots, a slight increasing trend of dynamic R_{ON} is observed in the time log scale.

In the repetitive UIS tests at 150 V V_M, a more significant dynamic R_{ON} drift is observed after 2 hours of repetitive UIS stress, as shown in Figure 3-30(b). The R_{ON} of all DUTs drifted out of the datasheet max limit quickly after the test started. To understand the dynamic R_{ON} drift of GaN HEMTs under repetitive transient voltage overshoot at different V_M, a physics-based model will be discussed in detail in section 3.6.3.

In addition to the in-situ measurement, R_{ON} is also measured on curve tracer at three different timestamps: prior to (fresh), shortly after (tested), and 8 hours after (recovery) the UIS test. After being removed from the UIS test board, DUTs are cooled down to room temperature before the curve tracer measurement, which usually takes about 2 minutes. The R_{ON} of DUT is consistently measured with 5 V gate bias and 900 mA source current. Figure 3-31 shows the R_{ON} tracking results, revealing that the R_{ON} shift is not permanent and can be fully recovered. In addition, the measured R_{ON} shortly after the 150 V UIS test (Figure 3-31(b)) is significantly smaller than the in-situ monitored $R_{DS(ON)}$ values reported in Figure 3-30(b), indicating considerable recovery when transferring DUT from the testing circuit to the curve tracer. This discrepancy highlights the importance of the in-situ monitoring developed in this study because ex-situ measurements cannot accurately characterize the dynamic R_{ON} degradation.

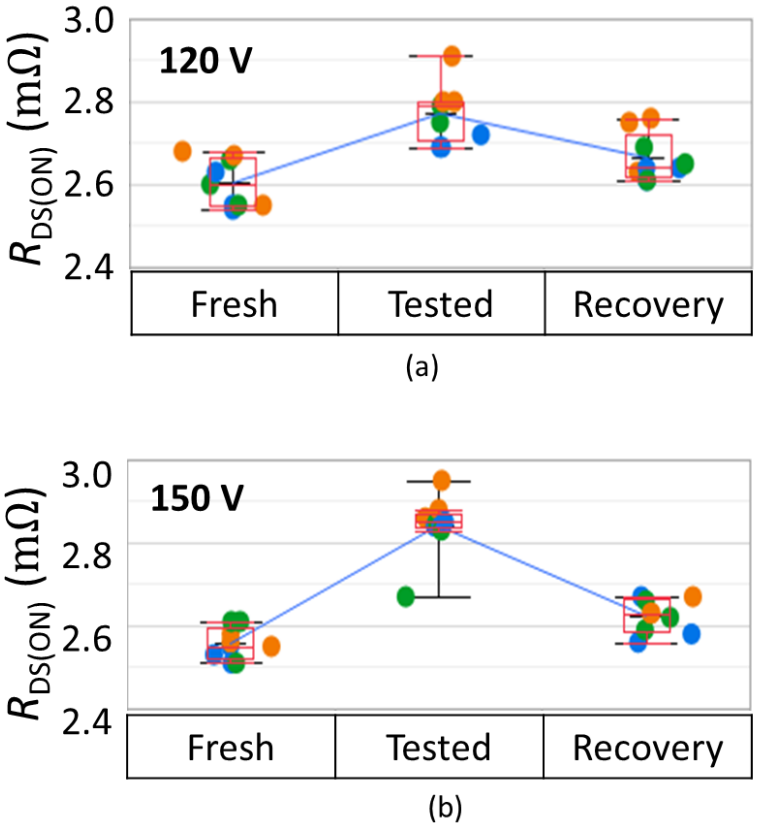


Figure 3-31. R_{ON} recovery tracking after (a) 120 V and (b) 150 V UIS tests. R_{ON} almost recovers to the initial state after 8-hour of relaxation.

3.6.3 Validation of the Physics-based Lifetime Model

A first-principles physics-based model is developed upon the theories proposed in [52], [121], accounting for the self-limiting electron trapping that occurs at the interface between AlGaN and the passivation layer (e.g., Si_3N_4). Note that this model does not apply to the buffer trapping [115]. As illustrated in Figure 3-32(a), the model considers the critical region of interest with the highest magnitudes of electric field (E-field); since the electrostatics in the vertical direction dominate the electron trapping at the interface, the model simplifies the interface trapping/de-trapping process to a 1D problem. The variation of E-field, carrier concentration, and trapping rate along the lateral direction is ignored. Each modeled parameter represents an average along the lateral direction in the critical region.

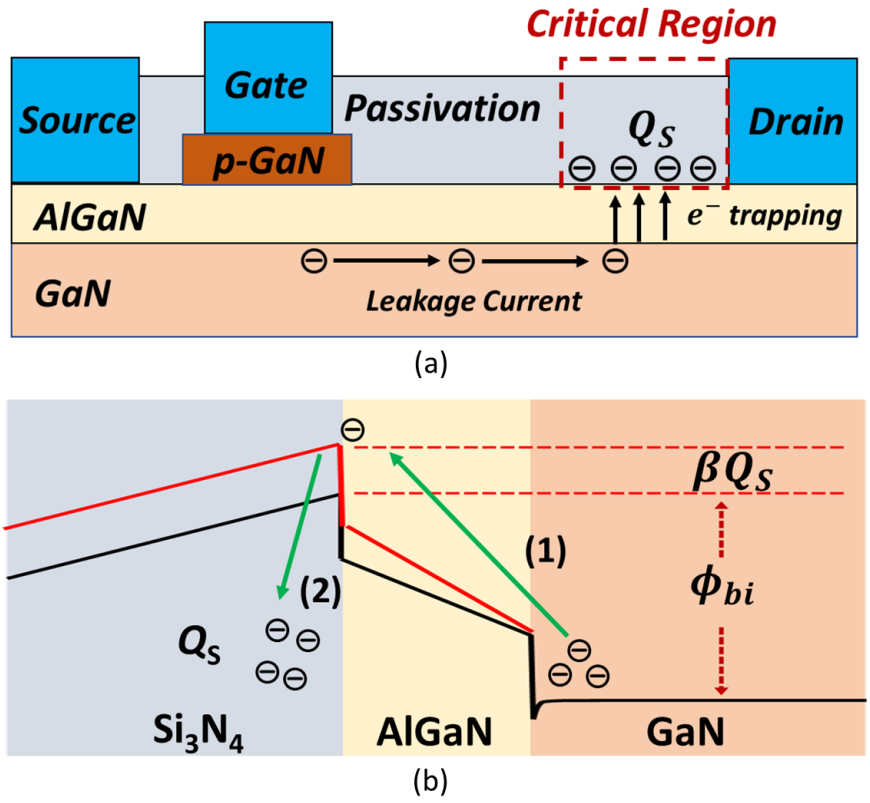


Figure 3-32. (a) Illustration of the trapping process in the DUT; the interface electron trapping occurs mainly in the critical high-field region near the drain contact. (b) Illustration of the 1-D trapping model in the vertical direction near the drain. The energy barrier is lifted up when additional electrons get trapped.

The 1-D trapping model in the vertical direction is shown in Figure 3-32(b), a surface barrier (ϕ_{bi}) exists at the AlGaN/Si_3N_4 interface. Under the influence of high electric field, a small fraction of electrons gains enough kinetic energy to overcome ϕ_{bi} and get trapped in the deep-level state within the dielectric. Denote the amount of trapped surface electrons as Qs. Qs further raises the barrier height dynamically by $\beta \times Q_S$, where β is a geometric factor relating Q_S to the barrier height change. This surface barrier rise hinders further electron trapping. Based on this 1D model, the extraction of the GaN HEMT lifetime consists of two steps: 1) calculating the trapped surface charge Q_S as a function of time; 2) converting Q_S to the R_{ON} shift.

To calculate Q_S, the electron density distribution in the energy space is first derived [81], [82]:

$$f(E)dE \propto Ee^{-\frac{E}{qF\lambda}}dE \qquad (3-6)$$

where E is electron energy, F is E-field, q is electron charge, and λ is electron mean free path. This equation suggests that the electron density drops exponentially as F decreases. Hence, in the

modeling process, we consider the critical region of electron trapping to be near the drain contact, as the peak F is usually located near the drain contact in commercial E-mode GaN HEMTs [69], [95], and such peak F governs the dynamic R_{ON} shift in the DUT.

Based on (3-6), the charge trapping rate near the drain is calculated by an integral in the energy space, since the energy barrier is $\phi_{bi} + \beta Q_s$, the integral is written as:

$$\frac{dQ_S}{dt} = A\int_{\phi_{bi}+\beta Q_s}^{\infty} f(E)dE$$

$$= A\int_{\phi_{bi}+\beta Q_s}^{\infty} Ee^{-\frac{E}{qF\lambda}}dE \approx A\phi_{bi}e^{-\frac{\phi_{bi}+\beta Q_S}{qF\lambda}} \equiv Be^{-\frac{\beta Q_S}{qF\lambda}} \quad (3-7)$$

From (3-7), the time evolution of Q_S can be solved:

$$Q_S(t) = \frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right) \quad (3-8)$$

Note that an equation similar to (3-8) is given in [121] with more parameters including the trap density, hot electron density, electron capture cross-section, etc. These parameters are hard to derive and vary significantly from vendor to vendor due to the differences in device structure, epi quality and process flow. For simplicity, in (3-8), they are all lumped into parameter B.

The next step is to model the dynamic R_{ON}. Firstly, we denote the density of electrons in the 2DEG channel as Q_P. Secondly, the total resistance of contacts and the 2DEG channel away from the drain contact, i.e., the region that is not impacted by the trapped electrons, is denoted as R_{00}, as illustrated in Figure 3-33 In a fresh DUT, as the access region resistance is inversely proportional to the 2DEG density, R_{ON} can be modeled by $R_{ON}(0) = R_{00} + C_1/Q_P$, where C_1 is a constant. As the dynamic R_{ON} is mainly caused by electron trapping in the critical region near the drain contact, the dynamic R_{ON} is modeled by $R_{ON}(t) = R_{00} + C_1/(Q_P - Q_S)$. Therefore, ΔR_{ON} is calculated by:

$$\Delta R_{ON}(t) = R_{ON}(t) - R_{ON}(0) = \frac{C_1}{Q_P - Q_S} - \frac{C_1}{Q_P}$$

$$= \frac{C_1}{Q_P}\left(\frac{1}{1-\frac{Q_S}{Q_P}}\right) - \frac{C_1}{Q_P} \quad (3-9)$$

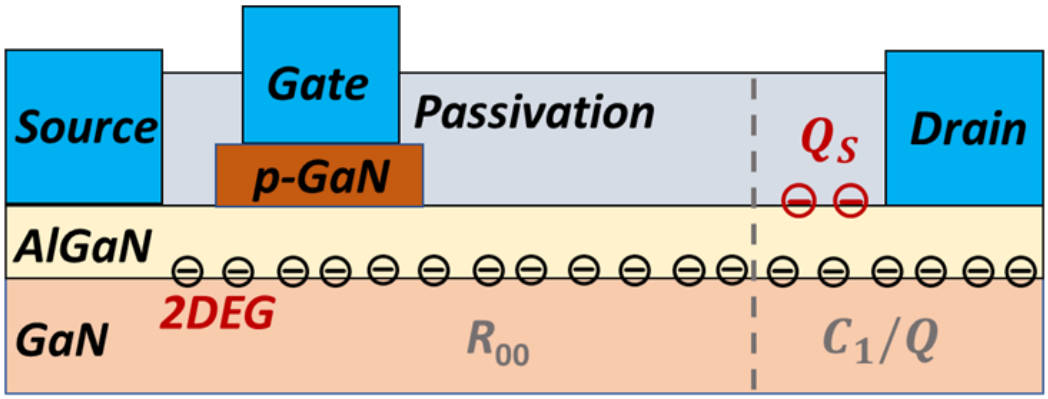


Figure 3-33. Illustration of the R_{ON} distribution in the modeled GaN HEMT.

Based on (3-9), the solution of $R_{ON}(t)$ can be further derived under two scenarios:

A. 120 V peak UIS test

When the trapped charge density is small ($Q_S << Q_P$), i.e., a mild R_{ON} drift, (3-9) is further simplified utilizing the first order Taylor expansion as:

$$\Delta R_{ON}(t) \approx \frac{C_1}{Q_P}\left(1+\frac{Q_S}{Q_P}\right)-\frac{C_1}{Q_P}$$

$$= \frac{C_1 Q_S}{Q_P^2} = \frac{C_1}{Q_P^2}\frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right) \qquad (3-10)$$

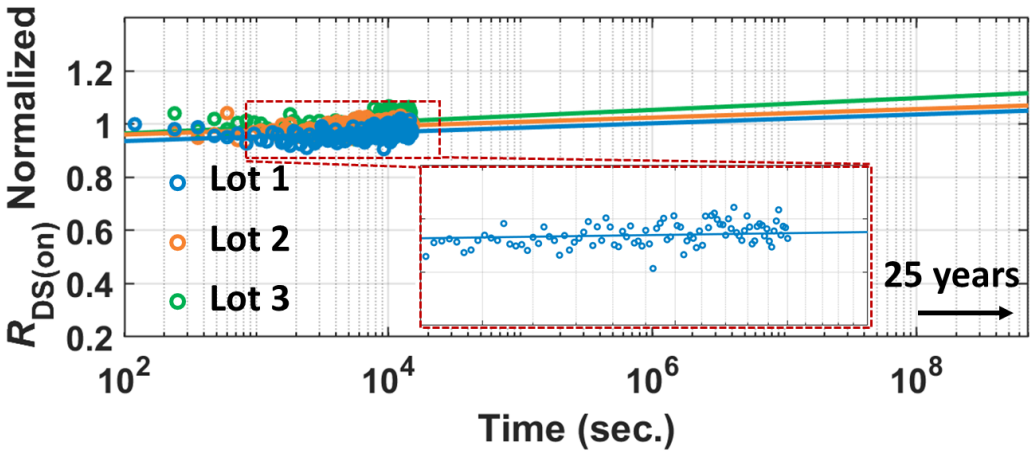


Figure 3-34. DUT lifetime projection based on the electron trapping model at 120 V.

(3-10) predicts a nearly linear dependence of $R_{DS(ON)}$ on log *t,* which is verified by the linear fitting in the semi-log plot of $R_{DS(ON)}$ as shown in Figure 3-34. For a clearer view of $R_{DS(ON)}$ drift, y axis in Figure 3-34 is normalized to the first data point. DUTs from three lots show similar projected $R_{DS(ON)}$ slope in the fit, which confirms that they all have an identical underlying trapping mechanism. More importantly, the model projects less than 10% R_{ON} increase over 25 years of continuous overvoltage switching at 100 kHz and 120 V $V_{DS,peak}$. Note 10% increase of the initial $R_{DS(ON)}$ measured in-situ is still within the datasheet max limit, revealing good overvoltage robustness of GaN HEMTs.

B. 150 V UIS test

At 150 V $V_{DS,peak}$, the density of the trapped charges Q_S can approach that of the 2DEG electrons Q_P. As revealed in Figure 3-30 , the DUTs exhibit larger $R_{DS(ON)}$ increase in 150 V UIS test. Hence, the linear approximation in (3-10) no longer holds. The projection of $R_{DS(ON)}$ drift is calculated directly by plugging (3-8) into (3-9):

$$\Delta R_{DS(ON)}(t) = \frac{C_1 Q_S(t)}{Q_P[Q_P - \frac{qF\lambda}{\beta}\log\left(1 + \frac{B\beta}{qF\lambda}t\right)]} \qquad (3-11)$$

For an accurate modeling and lifetime projection, the value of the fitting parameters needs to be extracted.

The barrier height change originated from Q_S is induced by the additional electrostatic potential change due to the trapped electrons, hence, β can be modeled by the potential change induced by an electron based on the Gauss' law:

$$\beta = V_{QS} = \frac{q}{4\pi\epsilon_r\epsilon_0 d} \qquad (3-12)$$

where q is the unit electron charge, ϵ_r is the dielectric constant of AlGaN, ϵ_0 is the permittivity of free space d is the thickness of the AlGaN, which is typically between 10-20 nm in GaN HEMTs. These values give the estimated $\beta \sim 0.0066\,V - 0.0132\,V$. In the modeling process, β is chosen to be 0.01 V based on the specific device structure of the DUT in this work.

F is the peak electrical field near the drain contact at an arbitrary time instant during the repetitive UIS test, and the value of F is determined by V_{DS}. The formula to estimate F is given in [52]:

$$F = C_2 \alpha \ln\left[1 + exp\left(\frac{V_{DS} - V_{FD}}{\alpha}\right)\right] \quad (3-13)$$

where C_2 is a constant, α is the curvature parameter representing how quickly the electric field grows after full depletion of the channel. The numerical extraction of α and C_2 is based on the TCAD simulation, where α is 10 V and C_2 is 1.6×10^4 (unitless) for the DUT. V_{FD} is the voltage at which the 2DEG is fully depleted to the drain contact; V_{FD} = 100 V for the DUT in this work [52].

Q_P is the 2DEG density in the GaN HEMT access region. For the DUT in this work, Q_P = 5.7×10^{12} cm^{-2} from the material characterizations.

$$\lambda \propto \sqrt{T} \exp\left(\frac{h\omega_0}{kT}\right) \quad (3-14)$$

where T is the temperature in Klevin, k is the Boltzmann constant, and $h\omega_0$ is 92 meV [124]. From the equation above, λ is estimated to be ~560 nm at 75 °C, and this value is used in the model.

Parameter B and C_1 are extracted by numerical fitting, whereas these two parameters are related to the physical electron trapping process, device structure and characteristics, as well as the device operating conditions. Since the normalized $R_{DS(ON)}$ is used in the lifetime projection, $C_1/R_{DS(ON)}(0)$ is denoted as C_3. For the DUT in this work, a typical value of C_3 = 0.6 is used, which has been shown to be valid for GaN HEMTs with various voltage ratings [52]. A typical value of B is 166 $K^{0.5}s^{-1}$.

As $Q_S(t)$ is also a time dependent variable, there is no analytical solution of (3-11). Instead, a set of MATLAB code is then used to obtain the numerical solution of the equation via iteration. The calculating process is illustrated in Figure 3-35. In each switching cycle, differentiation is first applied at the voltage overshoot, from which the ΔQ_S is calculated; by summing up the ΔQ_S, the total Q_S is obtained in this cycle. Since the energy barrier is influenced by the trapped charge density, the Q_S is put in the next switching cycle to calculate the new ΔQ_S and Q_S, and the numbers of iteration match the total switching cycles of the UIS test.

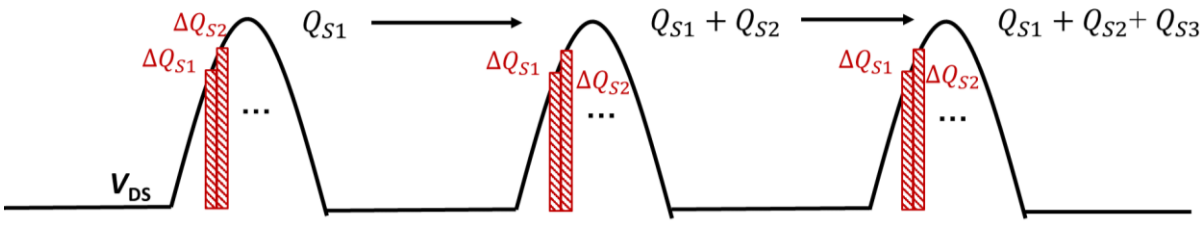


Figure 3-35. Illustration of calculating the Q_S by iteration in MATLAB.

By tuning value B, a good agreement between the measured datapoints and the solid fit lines across multiple lots is observed and shown in Figure 3-36. This validates that the electron trapping at passivation interface is the predominant intrinsic degradation mechanism. The good agreement between models and measurements at multiple $V_{DS,peak}$ and for multi-lot DUTs proved the applicability and versatility of the lifetime model.

It is worth mentioning that the value of parameter B is impacted by the intrinsic device parameters (e.g., leakage profile, trap density, trap energy levels, etc.) and device operation conditions (e.g., switching frequency, voltage overshoot duration), where both variables can significantly impact the trapping effect. Hence, the accurate determination of parameter B through a first-principle method is quite challenging. Practically, parameter B can be extracted by matching the test condition with the target mission profile, where the frequency and the pulse width of the overvoltage spikes are well defined. By utilizing this approach, the dynamic R_{ON} can be projected

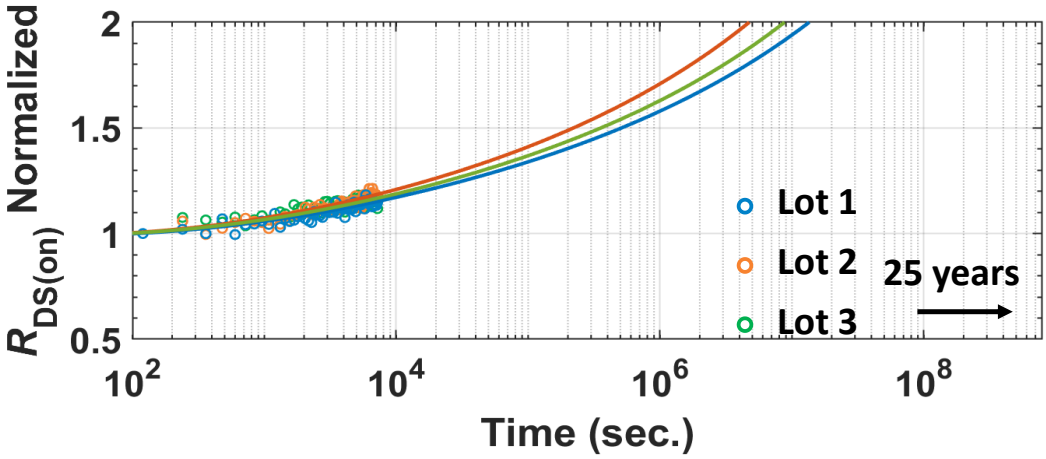


Figure 3-36. DUT lifetime projection based on the electron trapping model at 150 V.

by a simplified linear model when the shift is small. When higher overvoltage spikes are applied, the more significant $R_{DS(ON)}$ shift can be fit by (3-11).

3.7 Conclusions

This chapter introduces the high frequency repetitive testing methodology on studying the overvoltage robustness of GaN HEMTs. The HFOT test explores the overvoltage ruggedness and $BV_{DYN\text{-}SW}$ of p-gate GaN HEMTs in high-f_{sw} switching. A novel converter-based testbed with the ACC is designed and prototyped, allowing for >1 kV overvoltage at f_{sw} up to 1 MHz. This setup is used to characterize the commercially available 600/650 V and 100 V p-gate GaN HEMTs from various vendors. *DUT #1* and *#2* show a nearly f_{sw} independent $BV_{DYN\text{-}SW}$ consistent with their $BV_{DYN\text{-}SIN}$ obtained from the single-pulse UIS test. *DUT #3* and *#4* show the considerably reduced $BV_{DYN\text{-}SW}$ at high f_{sw} (>200 kHz). Two distinct root causes are identified through the HFOT stressing at 70% of the $BV_{DYN\text{-}SIN}$. DUT #3 shows a drastic, nearly unrecoverable increase in R_{ON}, while DUT #4 shows degradations in the OFF-state leakage current and BV. Finally, the repetitive UIS test is proposed as a fast and effective method for filtering out the GaN HEMTs with inferior high-f_{sw} overvoltage ruggedness. These results reveal two new degradation mechanisms in GaN HEMTs under the high-f_{sw} switching and provide critical information for the GaN HEMT overvoltage qualification and the fault protection of GaN-based converters.

The high frequency repetitive UIS test with in-situ R_{ON} monitoring enables a comprehensive understanding of the dynamic R_{ON} shift over time. The R_{ON} degradation over time is attributed to the electron trapping occurs at the AlGaN-passivation interface. A physics-based model is proposed to explain and project such evolution. Less than 10% dynamic $R_{DS(ON)}$ increase is projected for over 25 years of continuous operation under 120% of the max rated drain voltage, indicating good overvoltage robustness of GaN HEMTs. Good agreements between the measured data and model fits at various repetitive overvoltage spikes are achieved, validating the proposed electron trapping mechanism and the versatility of the lifetime projection.

The experimental results in this chapter manifest the necessity of performing switching based GaN HEMT robustness test with in-situ degradation monitoring. The testing profile should be as close to the application scenario as possible to capture all failure or degradation phenomena and understand the underlying mechanisms.

Chapter 4 Avalanche Robustness of Vertical GaN Fin-JFET

4.1 Introduction of the Vertical GaN Fin-JFET

Chapter 2 and 3 present the overvoltage robustness of lateral GaN HEMT. As the structure of GaN HEMT is inherently different from traditional Si and SiC based power devices, new device physics, degradation and failure mechanisms are unveiled. Another technical approach to exploit the superior material property of GaN is building up the vertical GaN devices. Recently, significant progress has been made on the GaN vertical Fin-channel JFET, which has achieved the E-mode operation and a smaller specific R_{ON} compared to GaN HEMT and SiC MOSFET. In addition, 1.2 kV vertical GaN Fin-JFETs have been demonstrated by the industry. The device schematic of the GaN Fin-JFET is shown in Fig. 1-5 in chapter 1. Vertical GaN Fin-JFET has similar architecture as SiC JFET except for a narrower fin-channel realized by the entirely different fabrication process, which can realize the E-mode operation without comprising the low channel resistance. Therefore, it is expected to possess an avalanche breakdown mechanism under overvoltage conditions similar to the SiC JFET. This chapter presents the studies to characterize the avalanche capability of the vertical GaN Fin-JFET.

4.1.1 Key Device Characteristics

The DUT in Chapter 4 and 5 is the 650-V class GaN Fin-JFET fabricated by NexGen Power Systems. Note that the 1200-V class GaN Fin-JFET has also been demonstrated in [47], [48]. their avalanche capability, as well as the surge current and avalanche capability of the vertical GaN p-n diodes, have been initially studied in [105], [125], [126]. In this thesis work, we characterize the 650-V rated devices mainly to allow for a direct comparison with the similarly-rated GaN HEMTs. Figure 4-1(a) and (b) show the transfer and OFF-state I-V characteristics at 25, 75 and 125 ^{o}C. The threshold voltage (V_{th}) is 0.7 V at 25 ^{o}C extracted at a drain current (I_D) of 1 mA. The BV_{AVA} is ~800 V with a positive temperature coefficient.

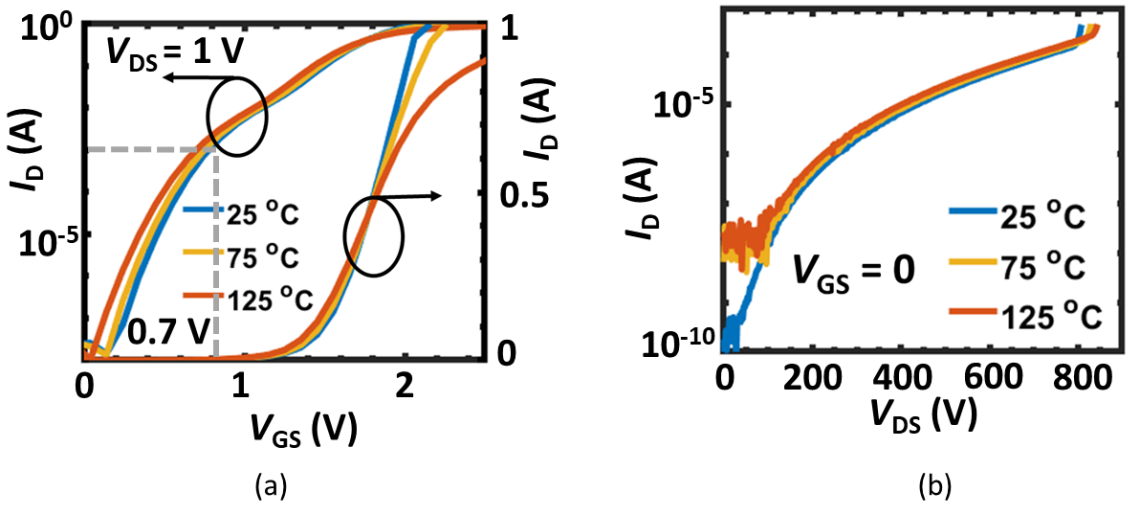


Figure 4-1. The DUT's (a) transfer, (b) OFF-state I_D-V_{DS} at 25-125 °C.

Figure 4-2 shows the gate current (I_G) versus gate-to-source bias (V_{GS}) from 25 °C to 125 °C. The turn-on voltage is ~3 V extracted at I_G = 1 mA at 25 °C, which is close to GaN's bandgap, suggesting the good quality of the lateral p-n junction with low interface states [127]. This gate stack allows an effective hole injection into the fin channel, which is validated by output characteristics at various I_G (Figure 4-3(a)). At higher I_G, the enhanced hole injection induces a stronger conductivity modulation, reducing R_{ON} and raising the saturation I_D. Figure 4-3(b) shows the output characteristics at various V_{GS}, the active area of the DUT is 0.1 mm^2, yielding a specific R_{ON} of 0.7 mΩ·cm^2.

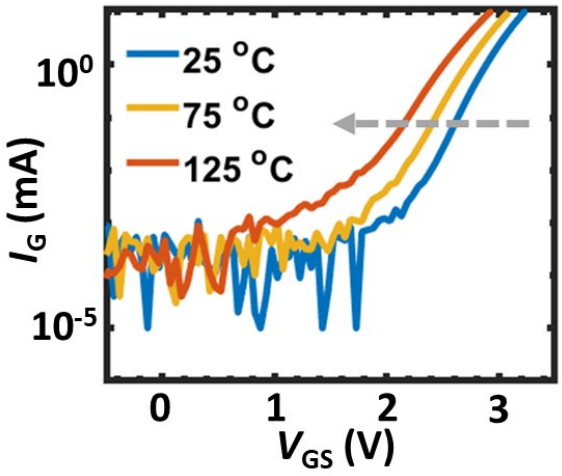


Figure 4-2. DUT's I_G-V_{GS} characteristics at 25-125 °C.

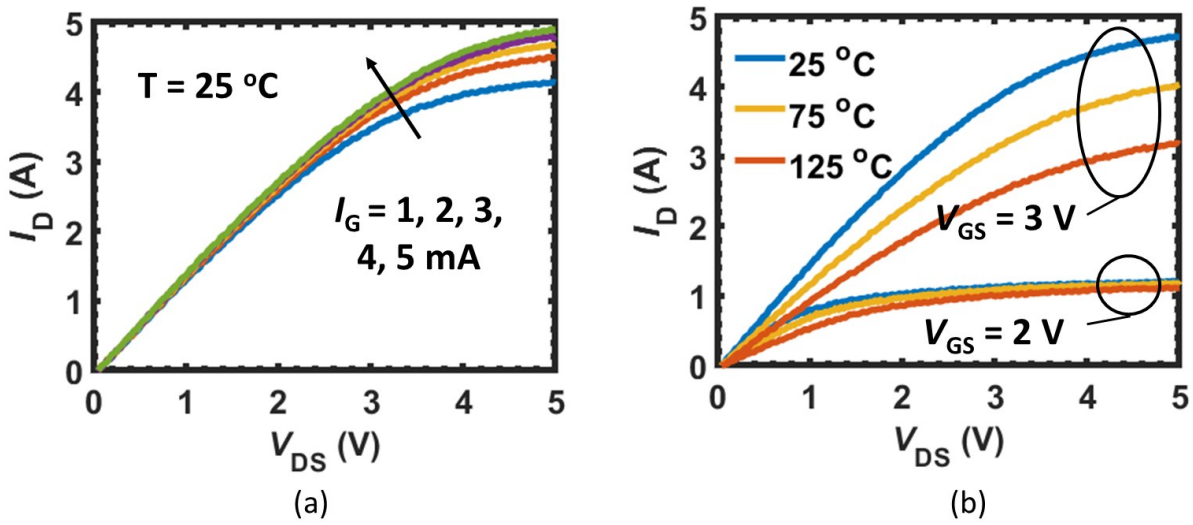


Figure 4-3. DUT's output characteristics with (e) various I_G and (f) various V_{GS} at 25-125 °C.

4.1.2 Different Avalanche Breakdown Modes in GaN Fin-JFET

The different avalanche modes in GaN Fin-JFET is first identified and explained by Dr. Liu in 2020 [47]. To be more specific, there are two avalanche paths in the Fin-JFET: a) through the p-GaN gate [47], [48], which is the typical avalanche with the avalanche current flowing through the gate-drain p-n junction, and b) through the n-GaN fin channel [128], in which the gate is turned ON during the avalanche enabled by a RC interface gate driver.

Since the p-n junction is located between the gate and drain, an RC interface current driving circuit is preferred for fast switching as well as low gate I_G during the steady on-state. Figure 4-4(a) shows the schematic of the driver circuit. C_G represents the DUT's gate capacitance. R_{ON} and R_{OFF} are used to limit the peak gate current during the switching transitions, R_{SS} is used to set the steady state on current and Css is used to provide a negative gate-source voltage during turn-off. As a general rule of thumb, the value of R_{SS} is much larger than R_{ON} of 4.7 Ω.

The gate driving circuit behavior during the turn-on transient, steady on-state, and turn-off transients are illustrated in Figure 4-4 (b)–(d). In the turn-on transient, positive bias V_G^+ is supplied at the driver. Before the device's gate p-n diode turns on, capacitive charging occurs via the loop of R_{ON} and C_{SS} (Figure 4-4 (b)). Once the gate p-n diode turns on, device enters the steady state,

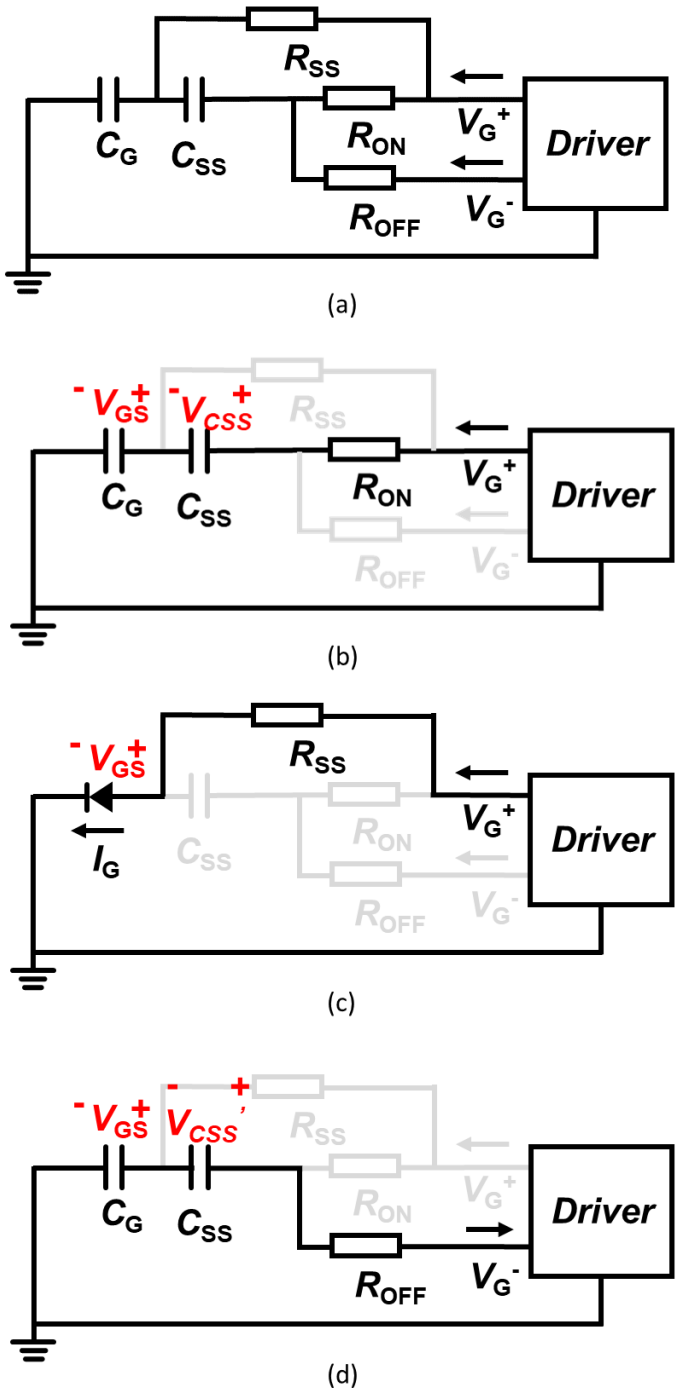


Figure 4-4. Illustration of (a) gate driving scheme. (b) Turn-on transient. (c) Steady on-state. (d) Turn-off transient of the vertical GaN Fin JFET.

the gate junction conducts current I_G determined by V_G^+ and gate diode voltage drop (Figure 4-4(c)). In the turn-off transient, as illustrated in Figure 4-4 (d), a charge balance between C_G and C_{SS} occurs, providing required negative V_{GS} for device turn-off.

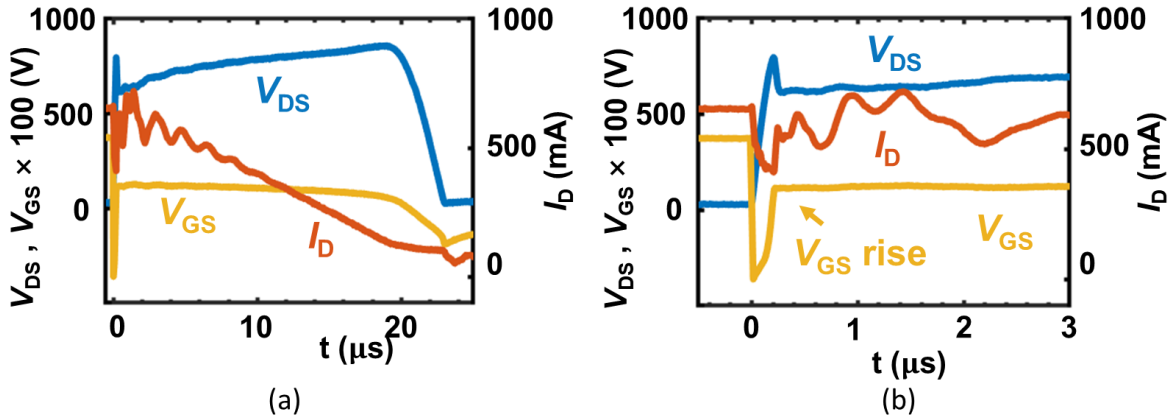


Figure 4-5. (a) GaN Fin-JFET avalanche waveform of the avalanche-through-fin process. (b) Zoom-in waveforms in the first 3 µs.

Figure 4-5 illustrates the measured waveforms of the through-fin avalanche in the UIS test [128]. As shown in Figure 4-5(a), the DUT shows textbook-avalanche behavior: V_{DS} clamps at BV_{AVA}, and I_{AVA} gradually reduces to zero. Different from the avalanche waveforms in MOSFETs [65], V_{GS} is kept above 1 V during most of the avalanche duration and I_G is much smaller than the avalanche current (I_{AVA}). Zoom-in waveforms in the first 3 µs of avalanche is shown in Figure 4-5(b), during the first 0.2 µs after the DUT turns OFF, V_{GS} first drops to negative values as the device is turned-off, then it is lifted and turns on the channel until the end of avalanche.

Figure 4-7 illustrates the physical process of the through-fin avalanche. When the avalanche is initiated, I_{AVA} first goes through the path of R_{SS}, R_{ON}, R_{OFF} to the driver (Figure 4-7(a)). The voltage drop on these resistors raises V_{GS} over the DUT's V_{th}, and then the fin channel is turned ON, migrating the majority of the I_{AVA} to the source. Only a small portion of I_G flows through the large R_{SS} to keep $V_{GS} > V_{th}$ (Figure 4-7(b)).

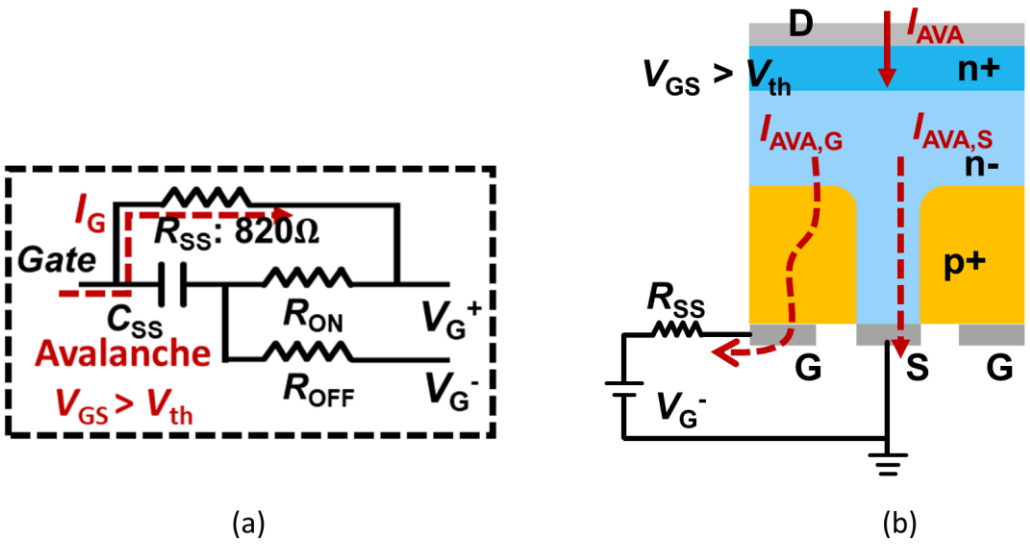


Figure 4-7. (a) Illustration of current paths in the DUT's avalanche processes. (b) Illustration of the avalanche-through-fin process in the UIS test with the *RC* gate driver.

The waveforms of the through-gate avalanche are illustrated in Figure 4-6. It is realized by replacing the RC interface driving circuit with a MOSFET gate driver with a 2 Ω gate resistor to ensure $V_{GS} < V_{th}$ in avalanche. However, smaller gate resistor value results in higher quiescent I_G therefore larger driving loss, such a driving circuit design is not recommended in applications. In Figure 4-6, it is clear that $V_{GS} < V_{th}$ and $I_G \approx I_{AVA}$, validating the through-gate avalanche.

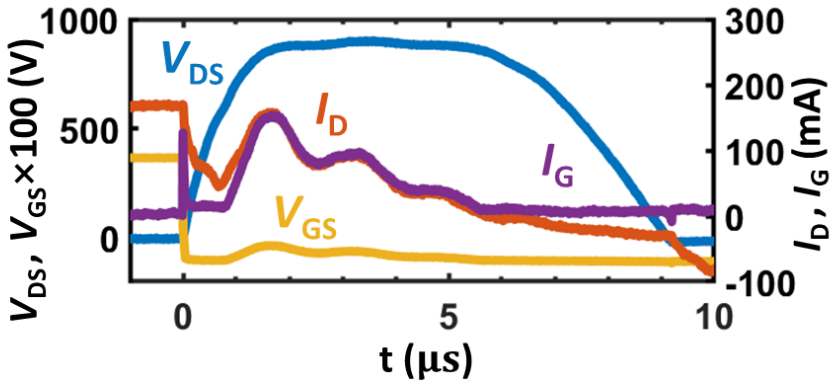


Figure 4-6. Through-gate avalanche waveforms of the DUT.

4.2 Avalanche Test Results

UIS circuit is used in this chapter to characterize GaN Fin-JFET avalanche capability. Figure 4-8(a) shows the UIS circuit schematic used in this section. A 24 mH inductor is connected with the DUT, and the input voltage (V_{IN}) is set at 30 V. Figure 4-8(b) shows our UIS test setup. V_{GS}, I_D, and drain-to-source voltage (V_{DS}) are directly measured by probes. I_G is calculated by the voltage drop on an additional gate resistor connected between the driving circuit and DUT gate. A function generator is used to control the gate signal for both single and repetitive UIS tests.

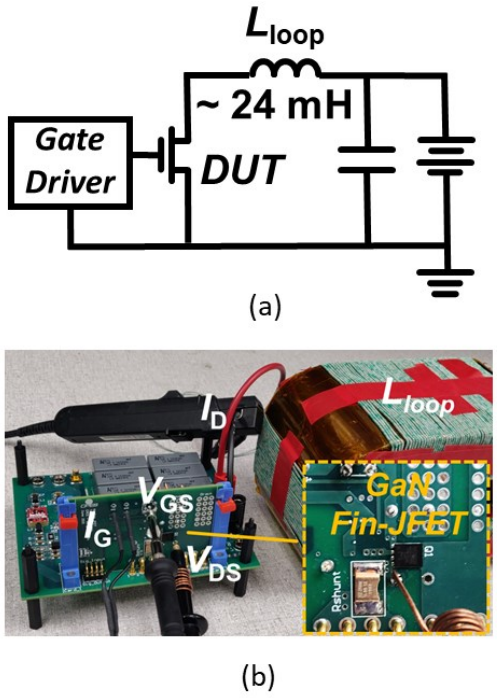


Figure 4-8. (a) Circuit schematic and (b) setup of the UIS test.

The E_{AVA} of the through-fin avalanche is first studied by increasing the load current in the UIS test. Figure 4-9 shows a typical failure waveform. A total of four DUTs are tested to failure. From the BV_{AVA}~I_{AVA} integral, E_{AVA} of three devices is calculated to be 10 J/cm^2, and 8 J/cm^2 for the last device. The device capacitance stored energy is much smaller than E_{AVA} (0.11 J/cm^2 calculated from the V_{DS}~I_D integral in the capacitive charging stage. Upon failure, V_{GS} reduces to zero, indicating a shorted gate-source (G-S) junction; the drain-source (D-S) remains open, and V_{DS} climbs to a slightly higher BV_{AVA}.

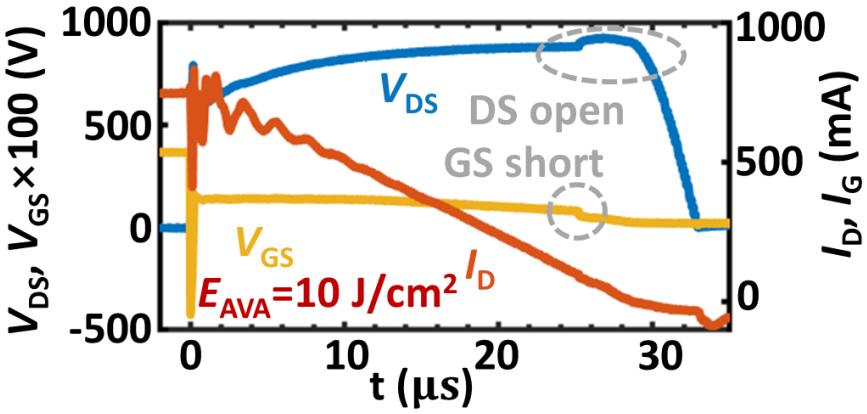


Figure 4-9. Failure waveform of a single-pulse through-fin avalanche.

To further probe the failure location, the source current (I_S), I_D and I_G of a fresh DUT and the failed DUT are measured at increased V_{DS} and zero V_{GS} on the curve tracer. For the fresh DUT (Figure 4-10(a)), $I_D \approx I_G \gg I_S$, showing that the gate-drain (G-D) junction is the main leakage path, and the G-S junction remains OFF. For the failed DUT (Figure 4-10(b))), $I_D \approx I_S \gg I_G$, proving the shorted G-S junction, which deviates the leakage current to the low-resistivity fin channel. Note that I_D is almost identical in the fresh and failed DUTs, suggesting that the G-D junction is intact in the failed DUT. The illustration of DUT failure spot is shown in Figure 4-10(c). Interestingly, from the off-state I-V curve (Figure 4-10(a) and (b)), the failed DUT shows a BV_{AVA} higher than that of the fresh DUT. This higher BV_{AVA} can be explained by the shorted G-S junction, which eliminates the depletion of lateral p-n junction in the failed DUT and thus reduces the number of charges contributing to the peak E-field at the fin bottom.

Repetitive UIS tests are then performed with a 3 s interval and 70% E_{AVA} in each cycle. No junction temperature built-up is observed, as confirmed by the thermal camera. Multiple DUTs are tested, and they all survive thousands of cycles with consistent behaviors. Here we describe a typical DUT that shows initial degradation in cycle #3701. The waveform suggests a G-S partial

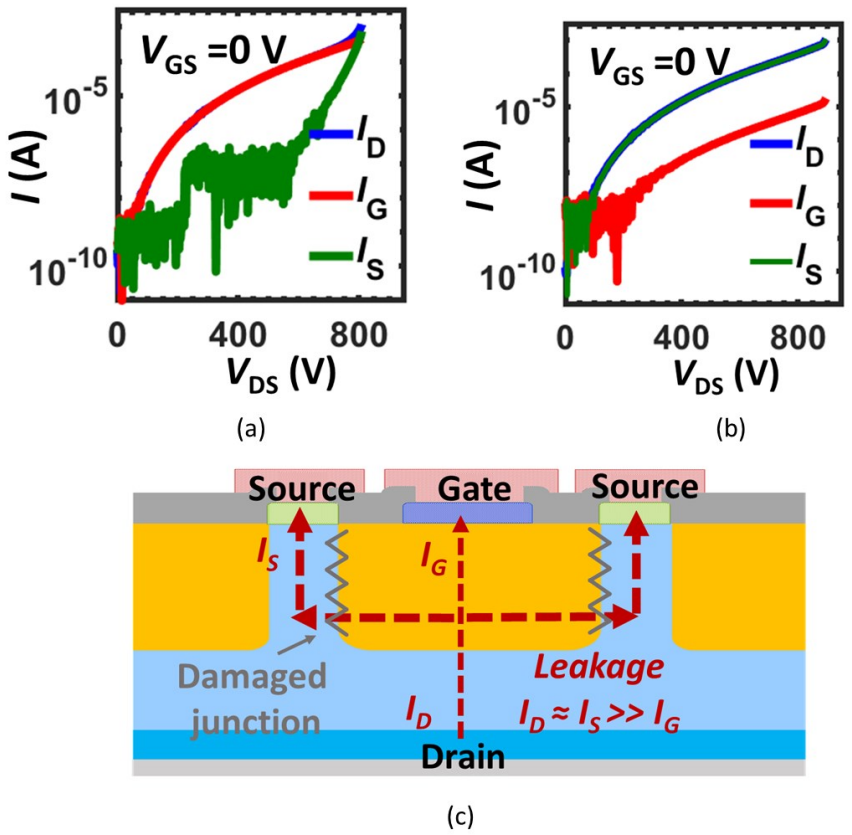


Figure 4-10. OFF-state *I-V* characteristics of (a) a fresh DUT and (b) the failed DUT. (c) Illustration of leakage current paths in the failed DUT.

short (Figure 4-11(a)). The post-cycle tests reveal an I_G increase at negative V_{GS} (Figure 4-11(b)), while the gate control is retained at forward V_{GS} (Figure 4-11(c)).

This DUT continued to withstand avalanche stress until the G-S junction is fully shorted in cycle #3705, in which the DUT cannot be turned ON. The BV_{AVA} is retained, revealing a failure-to-open-circuit (FTO) signature. This progressive FTO behavior can be explained by the increase in the number of fins that fail in the repetitive avalanche, with the G-S failed short in each fin.

By contrast, the DUTs tested in the through-gate avalanche failed with a failure-to-short-circuit (FTS) signature in single and repetitive tests. The E_{AVA} of the through-gate avalanche is measured to be ~1 J/cm^2. Figure 4-12 shows the DUT failure waveform in the repetitive tests, the destructive failure occurs at cycle # 523.

To understand the distinct failure behaviors in two avalanche modes, mixed-mode TCAD simulations are performed in Silvaco Atlas. The device model is based on [18]–[20] and the mixed-

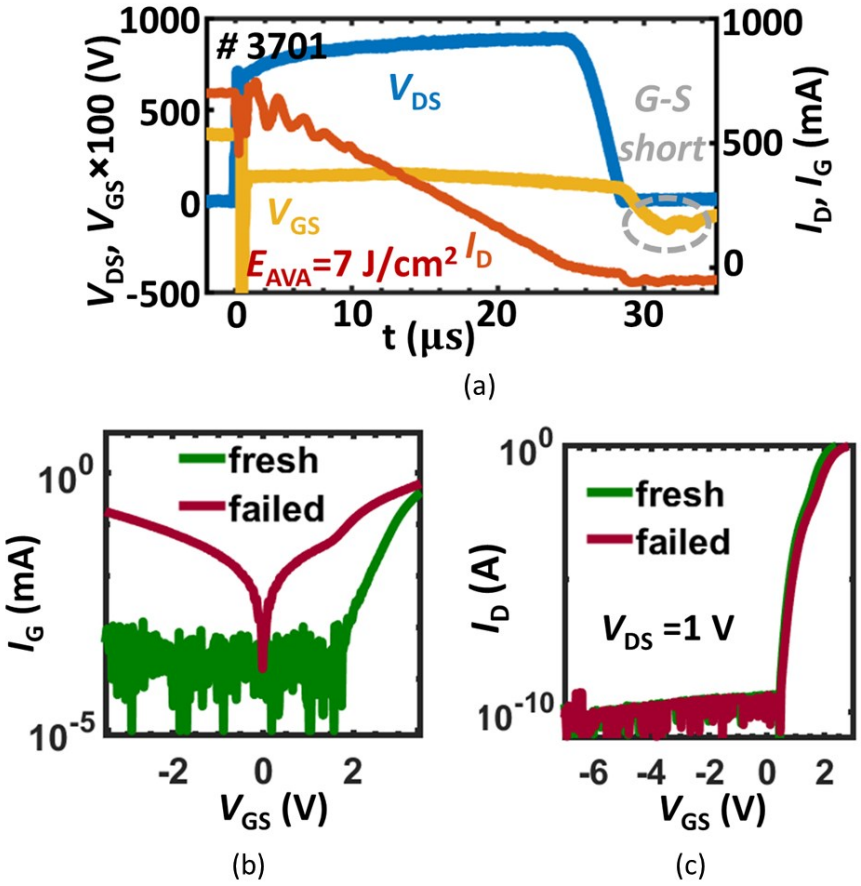


Figure 4-11. (a) Initial failure waveform in the repetitive through-fin avalanche test. (b) I_G-V_{GS} and (c) transfer characteristics of the fresh and failed DUTs after cycle #3701

mode simulation setup based on [87] using the UIS circuit. All experimental waveforms can be replicated.

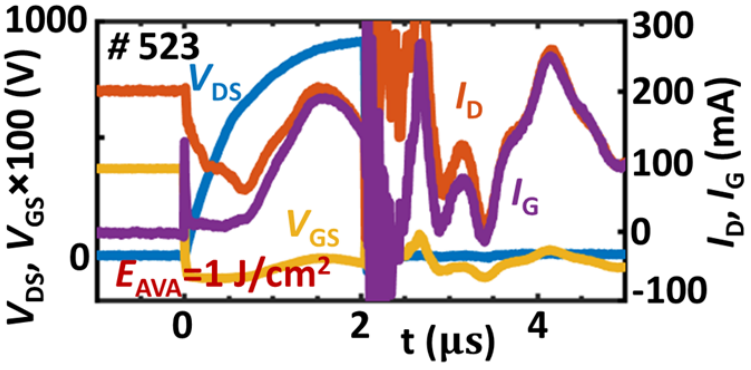


Figure 4-12. Failure waveform in the repetitive through-gate avalanche test, in which the DUT fails at cycle #523.

Figure 4-13 shows the simulated contours of I. I. generation rate, E-field and current in two avalanche modes. In the through-gate avalanche (Figure 4-13(a)-(d)), the locations of peak E-field, I. I. generation rates, and electron and hole currents are all at the G-D p-n junction. Hence, the junction damage due to high I_{AVA} and local heating leads to the device short failure.

In the through-fin avalanche (Figure 4-13(e)-(h)), while the peak E-field is still at the G-D p-n junction, the peak I. I. location moves to the foot of the n-GaN fin. Electrons are pumped from the source, travel through the fin channel, and recombine with the I. I.-generated holes. Holes are also

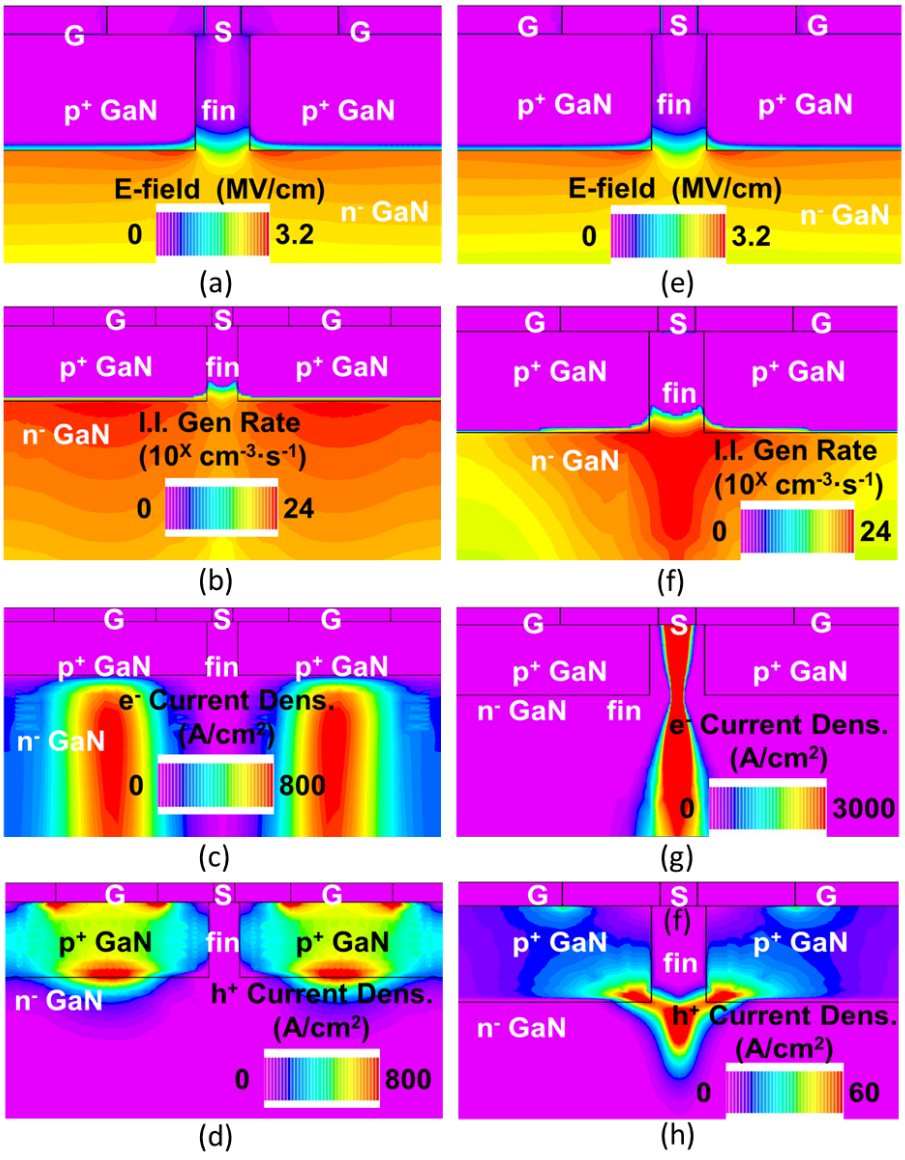


Figure 4-13. Simulated contours of (a)(e) E-field, (b)(f) I. I. generation rate, (c)(g) electron current density, and (d)(h) hole current density in the Fin JFET. (a)-(d) in the left column correspond to the through-gate avalanche, and (e)-(h) in the right column correspond to the through-fin avalanche.

partially removed via the gate to maintain the small I_G. As a result, the high I_{AVA} stress congregates in the fin, and only a small hole current density is present at the junction around the fin corner.

As this I_{AVA} stress is away from the G-D junction, and the narrow fin prevents the punch-through, BV_{AVA} retains in the failed DUT. The current density in the junction region is much lower than that in the avalanche through gate, suggesting a much smaller electrothermal stress locally. This explains the higher E_{AVA} in the avalanche through fin.

4.3 Benchmark and Conclusions

Table 4-1 compares the avalanche test results of GaN Fin-JFET with those of Si superjunction MOSFETs [129], [130], SiC JFETs [131], and SiC MOSFETs [132], [133]. The E_{AVA} of GaN Fin-JFETs is the highest reported in GaN FETs, much higher than that of Si MOSFETs and comparable to SiC FETs. Despite fewer survival cycles than Si and SiC MOSFETs, the GaN Fin-JFET shows an FTO signature in the through-fin avalanche, while all Si and SiC FETs show an FTS signature in avalanche. This shows the great promise of GaN Fin-JFETs in the applications like automotive powertrains and electric grids.

The broader implication of this work is that the I_{AVA} path can be tuned away from the major blocking p-n junction; this spatial separation of the high current stress and the peak E-field allows a new, robust avalanche mode with the desirable FTO signature.

Table 4-1. Summary of reported avalanche robustness data of GaN SiC and Si unipolar power FETs

Device	Voltage Rating (kV)	E_{AVA} (J/cm^2)	Repetitive Avalanche			Failure signature
			E_{AVA}%[a]	Period	Cycle survived	
GaN Fin JFET	**0.65**	**10.0**	**70%**	**3 s**	**>3700**	**FTO**
Si CoolMOS	0.6-0.9	1.3 [130]	62% [129]	3 s	10000	FTS
SiC JFET[b]	1.2	18 [131]	90% [131]	4 s	1000	FTS
SiC MOSFET	1.2	7.5[c] [132]	<77%[d] [133]	0.5 s	80000	FTS

[a]Percentage of E_{AVA} used in repetitive tests; [b]Normally-ON device; [c]E_{AVA} extracted at an avalanche time similar to that of GaN Fin-JFETs; [d]Estimated using the single-pulse avalanche energy provided in the datasheet, which is expected to be lower than the true E_{AVA} of the device.

Chapter 5: Short Circuit Robustness of Vertical GaN Fin-JFET

5.1 Short Circuit Robustness Requirement for Power Devices

Besides the avalanche or overvoltage robustness, short-circuit robustness is another key application requirement for power devices, particularly in automotive powertrains, motor drives, electric grids, and circuit breakers. In these systems, when short-circuit events occur, power devices must withstand an abnormally high current before protection circuits intervene, which typically takes at least ~10 μs [50], [62]. According to the U. S. Department of Energy 2025 Vehicle Drive Roadmap [134], even with ultrafast protection circuits added to gate drivers (which may increase system cost and complexity), the short-circuit withstanding time (t_{SC}) of power devices is required to exceed 2 μs. Depending on the device operation conditions, there are three types of short circuit events: type I (hard-switching fault) is a direct turn-on of the device while it withstands V_{BUS}; prior to the turn-on, there is no current flows through the off-state device. Type II (fault under load) refers to the case when device is conducting the load current, the complimentary switch on the same arm conducts or fails, and the device runs into the short circuit events. Due to a higher initial current compared to type I short circuit, the thermal stress in type II short circuit is harsher. Type III (reverse conduction) refers to the case that device undergoes short circuit event in reverse conduction [135]. For power transistors, the type I short-circuit condition is usually employed to evaluate the device robustness, where the device is required to withstand an abnormally high current while sustaining the bus voltage (V_{BUS}) in power converters [50].

The lateral GaN HEMT, a device with promising performance and low cost, however, has been found to possess a limited capability to withstand short circuit. The reported t_{SC} of all types of commercial 600/650-V GaN HEMTs is below 1 μs at the 400 V V_{BUS} in electric vehicle (EV) powertrain inverters [62], [136]. This weak ruggedness has become a roadblock for the penetration of current GaN devices into high power applications such as the EV powertrain. More fundamentally, it raises the concern if GaN devices with different designs are generically susceptible to short circuit events in power converters.

Extensive efforts are being made to improve the short-circuit robustness of GaN power devices, and almost all these efforts are still built on the HEMT device architecture. Recently, Transphorm [137] and Samsung [138] reported a t_{SC} of 3 µs and 10 µs, respectively, in their R&D GaN HEMTs. However, their ruggedness in repetitive short-circuit events is not reported. Meanwhile, t_{SC} has been found to seriously deteriorate under repetitive stresses for some GaN HEMTs [139].

This chapter presents the breakthrough short-circuit robustness in the vertical GaN Fin-JFET. The following major results of the short-circuit capability are highlighted: a) a record t_{SC} of 30.5 µs at V_{BUS} = 400 V, b) a failure-to-open signature where the device maintains the avalanche breakdown voltage (BV_{AVA}) after failure, c) a unique short-circuit capability at the device BV_{AVA} with t_{SC} > 10 µs, d) no degradation after 30,000 cycles of repetitive 10 µs short-circuit stresses at 400 V and e) the physics of device degradation and failure under repetitive 600 V 10 µs short circuit test.

5.2 Single-event Short Circuit Test

5.2.1 Test Setup

To best mimic the type I short-circuit in EV powertrains, the test setup (Figure 5-1(a)) has several design features: a) a V_{BUS} of 400-V or higher, stabilized by a 810 µF capacitor bank; b) a high slew rate (*di/dt*) enabled by the low stray inductance of the circuit board (Figure 5-1(b)), which mimics the shoot through in power systems; c) an *RC*-interface gate driving circuit (Figure 5-1(c)), which is identical to that used for the DUT's switching operations [47]. The working principles of this driver has been explained in detail in Figure 4-4. The DUT's V_{GS} and V_{DS} are measured by two high-bandwidth passive probes (1 GHz and 500 MHz). I_D is measured by a 30 A current probe (TCP0030A) or a 600 A Rogowski coil (CWTUM/3/B). I_G is calculated from the measured voltage across R_{SS}.

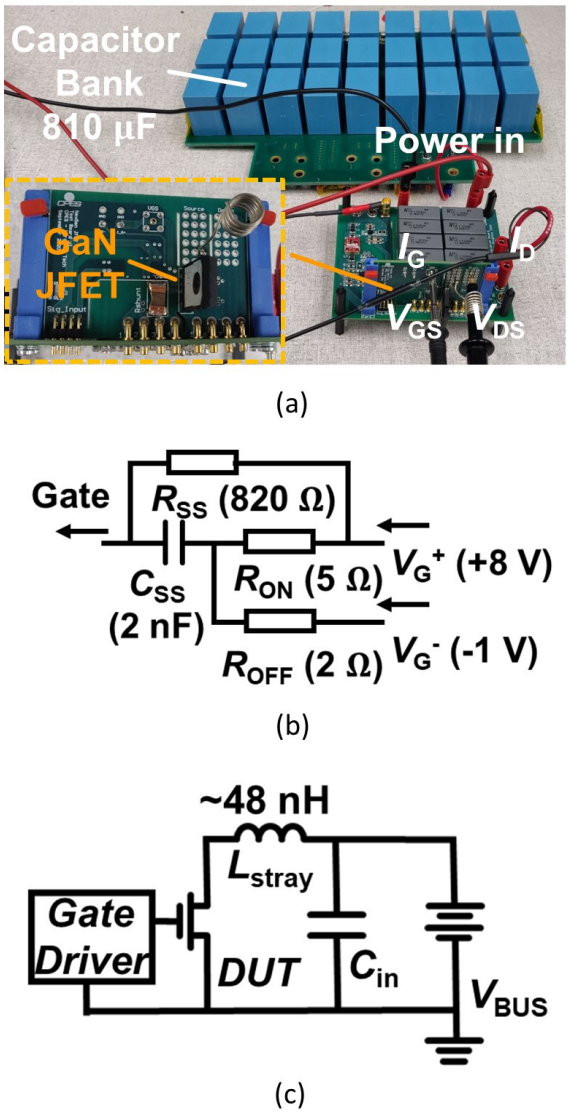


Figure 5-1. (a) Photo of the test setup. (b) Short circuit test circuit diagram (L_{stray} ~ 48 nH). (c) Circuit diagram of the *RC* gate-drive network.

5.2.2 Test Results

Single-event and repetitive short-circuit tests of GaN Fin-JFETs are performed at the V_{BUS} increased from 400 V up to the DUT's BV_{AVA} (800 V). At least three DUTs are tested for each condition, and good consistency is observed in all tests. All DUTs survived the 10 µs tests at different V_{BUS} with no degradations. Figure 5-2 shows the 10 µs test waveforms at V_{BUS} of 400 V and 800 V. A fast turn-on is enabled by the driving circuit (I_D rises to ~20 A in ~20 ns), followed by a large I_D reduction (>10X) due to elevated junction temperatures (T_j), accompanied by an I_G

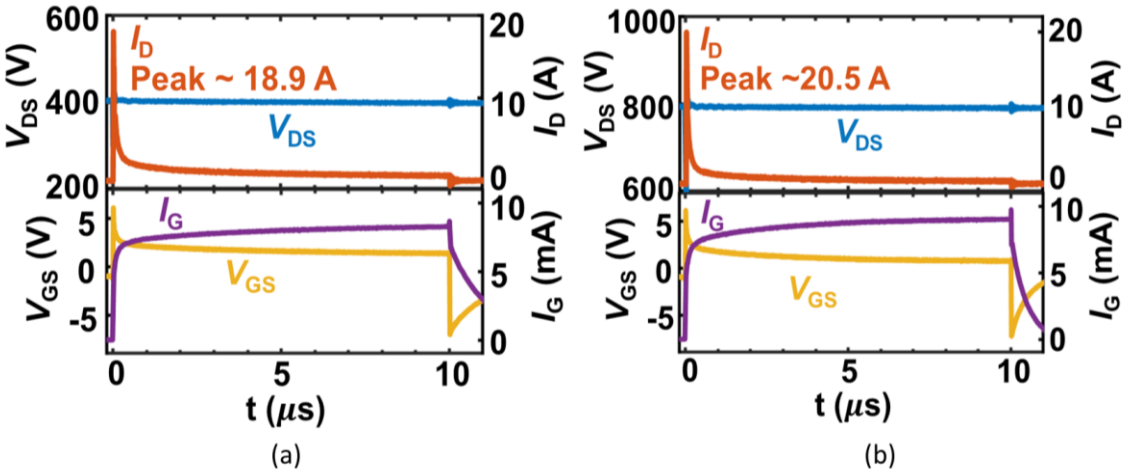


Figure 5-2. Typical 10 μs short-circuit test waveforms of GaN Fin-JFETs at a V_{BUS} of (a) 400 V and (b) 800 V. DUTs survived both tests and showed no degradation after each test. The peak I_D is around 20 A in the SC tests.

increase and V_{GS} decrease. This $I_{D,SAT}$ reduction with T_j is more pronounced than that in GaN HEMTs, which is the key enablers of the superior short-circuit capability of Fin-JFETs. This strong $I_{D,SAT}$ reduction can be attributed to:

(a) the negative temperature coefficient of bulk GaN mobility;

(b) high T_j facilitating the hole injection in the gate-to-source (G-S) p-n junction, resulting in an increase in I_G and the voltage across R_{SS}, thus reducing the device V_{GS};

(c) the reduction in the knee voltage (V_{knee}), which can be modeled by [13].

$$V_{knee} \approx \frac{qN_{Fin}W_{Fin}^2}{8\varepsilon} + V_{GS} - \frac{kT_j}{q}\ln\left(\frac{N_{Fin}N_A}{n_i^2}\right) \qquad (5-1)$$

where N_{Fin} and W_{Fin} are the doping concentration and width of the fin channel, N_A is the ionized acceptor concentration in p-GaN, and n_i is the intrinsic carrier concentration. At high T_j, V_{knee} decreases due to the reduced V_{GS} and increased N_A [as the acceptor (magnesium) energy is relatively deep in GaN]. The decreased V_{knee} leads to an early saturation and a lower $I_{D,SAT}$.

The forward voltage (V_F) of the G-S p-n junction, i.e., V_{GS} at a specific I_G, shows a good linear relation with T_j in the GaN Fin-JFET. This linear relationship is modeled in [124] for the GaN p-n junction, and the V_F is used as an electrical measure for T_j [141]. Figure 5-4 shows linear fittings for V_F versus T_j at various I_G from 6 mA to 10 mA, allowing construction of a lookup table for T_j

estimation based on any set of (I_G, V_{GS}). This lookup table is used to estimate T_j in the short-circuit process using the (I_G, V_{GS}) extracted from the waveform.

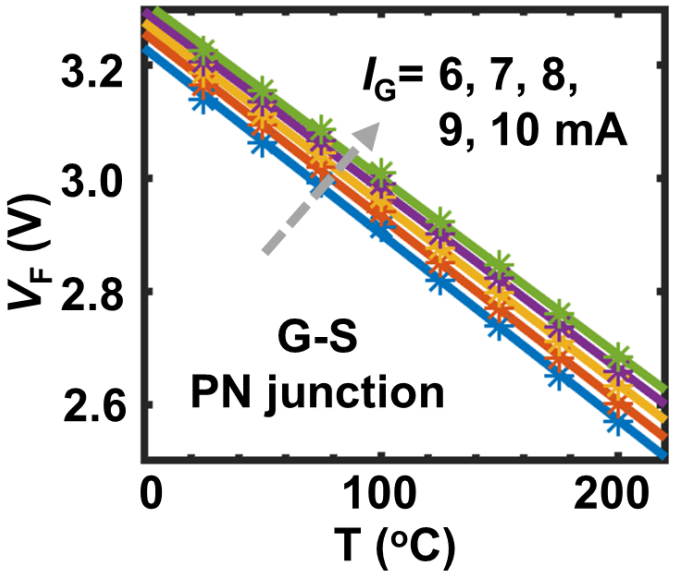


Figure 5-4. Forward voltage versus temperature of the gate-source p-n junction at I_G = 6 ~ 10 mA measured at 25 to 200 °C. A linear fit is shown for each I_G.

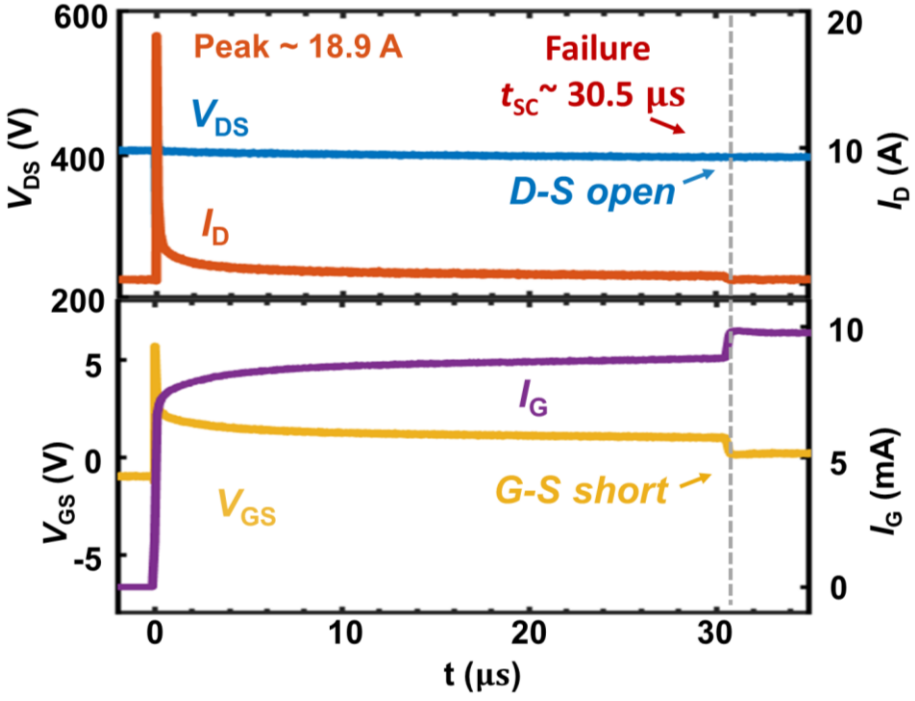


Figure 5-3. DUT's short-circuit failure waveforms measured at the V_{BUS} of 400 V

DUTs are tested to failure at different V_{BUS}, and a t_{SC} of 30.5 µs is measured at 400 V (Figure

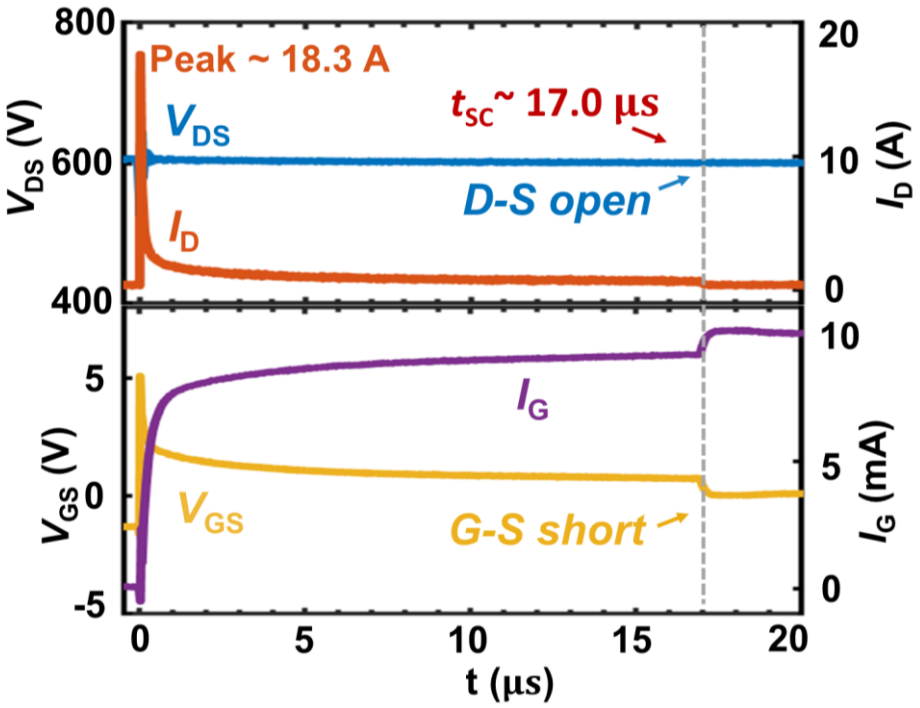


Figure 5-5. DUT's short-circuit failure waveforms measured at the V_{BUS} of 600 V

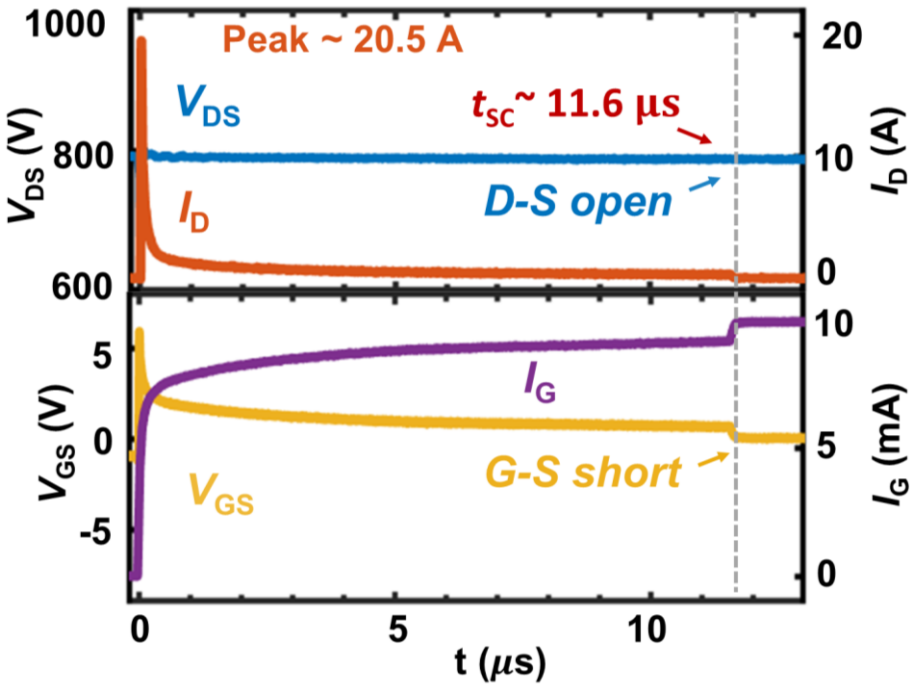


Figure 5-6. DUT's short-circuit failure waveforms measured at the V_{BUS} of 800 V

5-3), 17.0 µs at 600 V (Figure 5-5) and 11.6 µs at 800 V (i.e., the BV_{AVA} at 25 ºC) (Figure 5-6). The estimated T_j at failure is 740~845 ºC, suggesting th e good crystal quality of GaN. Upon failure, V_{DS} showed no change; I_D and V_{GS} dropped to zero; and I_G increased. These behaviors imply a drain-to-source (D-S) open and G-S partial shorting. This signature is confirmed by static characterizations of the failed DUT (Figure 5-7), in which BV_{AVA} is retained. This failure-to-open signature is highly desirable in system applications, as the failed device still blocks voltage, retaining system functionality in the case of parallel devices or multi-chip modules [142].

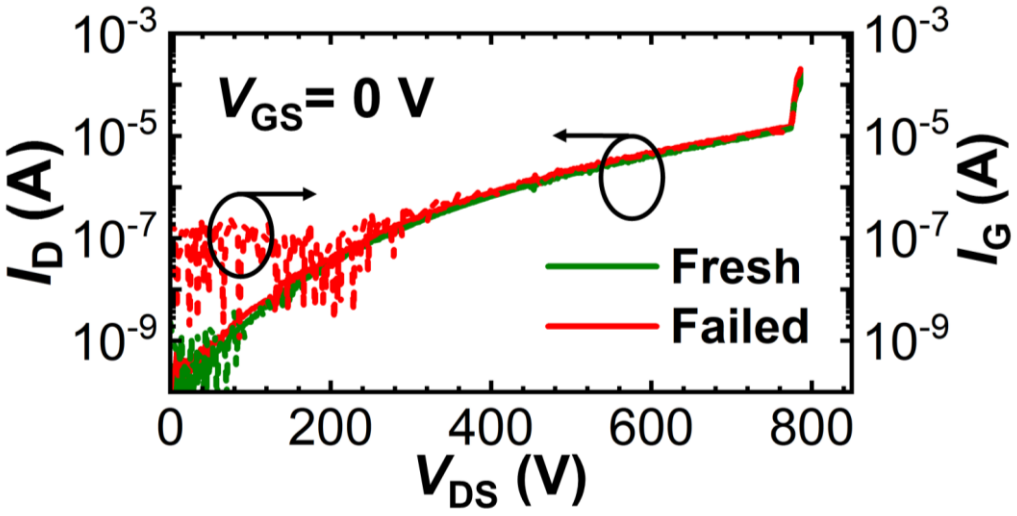


Figure 5-7. Off-state I-V characteristics of the fresh and failed DUTs. The I_D-V_{DS} and BV_{AVA} in the blocking state remain the same, and I_G at low V_{DS} is higher in the failed DUT.

5.2.3 Short Circuit Capability Near Avalanche Breakdown Voltage

The short-circuit capability at a bus voltage close to BV_{AVA} has not been reported previously. To understand this unique feature of GaN Fin-JFETs, we performed physics-based, electrothermal, mixed-mode TCAD simulations in Silvaco. The device avalanche models are similar to those described in [47] the electrothermal models are based on [83], and impact ionization coefficients are extracted from [143]. The key material models are detailed in Table 5-1. The circuit in the simulation is the same as the short circuit experiment. The simulation is able to replicate the measured experimental waveforms.

In the simulated short-circuit transient at 800 V (t = 11 µs), the impact ionization (I. I.) generation rate is found to peak at the foot of the fin channel (Figure 5-8(a)). The holes generated in the I. I. are removed via the p-GaN gate (Figure 5-8(b)), and these holes also facilitate electrons

to be pumped from the source to recombine with them (Figure 5-8(c)). This produces an "avalanche-through-fin" phenomenon that could accommodate a large I_D flowing through the fin channel into the drift region. As shown in Figure 5-8(d), the simulated peak T_j is located at the foot of the fin with a magnitude similar to our prior estimations using (I_G, V_{GS}), suggesting that the

Table 5-1. Key models in the electro-thermal simulation

Parameter	Simulation Model
GaN electron mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	Drift layer: $800 \times (T_L/300)^{-1.25}$ Substrate: $100 \times (T_L/300)^{-1.25}$
GaN k_T ($W \cdot cm^{-1} \cdot K^{-1}$)	$2 \times (T_L/300)^{-1.3}$
Thermal resistance ($W \cdot cm^{-2} \cdot K^{-1}$)	Top surface: 2 Bottom surface: 0.1
Impact ionization coefficients (cm^{-1})	Electron: $4.48 \times 10^8 \times \exp(-3.39 \times 10^7/E)$ Hole: $7.13 \times 10^8 \times \exp(-1.46 \times 10^7/E)$

T_L: lattice temperature (in Kelvin); E: electric field.

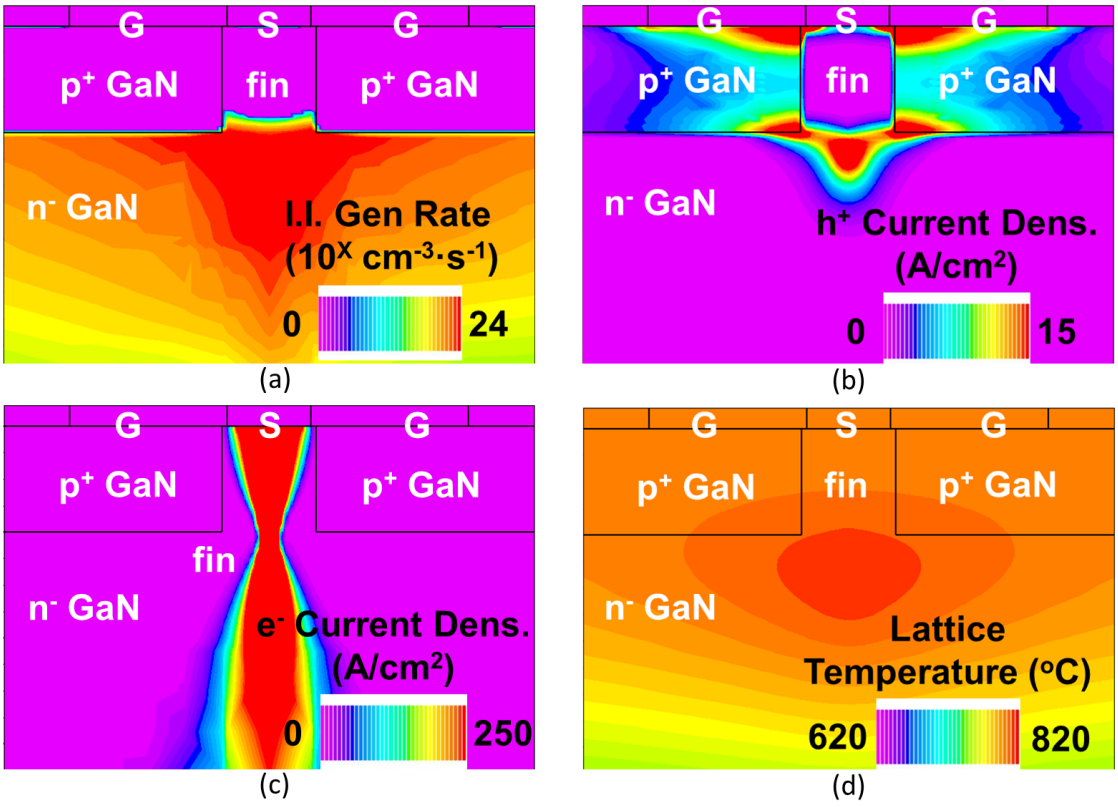


Figure 5-8. Simulated contours of (a) the impact ionization generation rate, (b) hole current density, (c) electron current density, and (d) lattice temperature at the t = 11 μs transient in the 800 V short circuit condition.

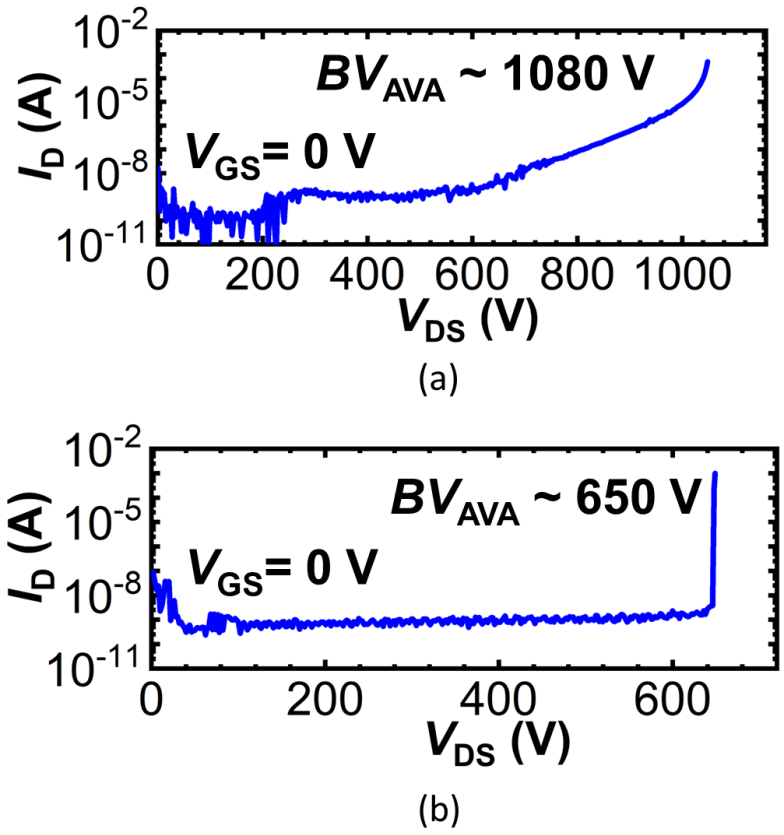


Figure 5-9. The off-state I-V characteristics of (a) SiC MOSFETs (C3M0120065K) and (b) Si CoolMOS (IPZA60R180P7).

DUT fails due to the G-S junction degradation under high electrothermal stress in the concurrent presence of avalanche and short-circuit.

The simulation results can also help understand the quick drop of $I_{D,SAT}$ in GaN Fin-JFETs under the short-circuit stress. At high V_{BUS}, the depletion region expansion results in the narrowing of the current path. The location of peak T_j coincided with that of the narrowest current path, leading to a fast decrease in carrier mobility. As a result, $I_{D,SAT}$ and the resulting thermal stress on GaN Fin-JFETs are suppressed, leading to a long t_{SC}.

Finally, as the high-V_{BUS} short-circuit test data of Si and SiC devices are lacking in the literature, the short-circuit capabilities of a 650-V SiC MOSFET (C3M0120065K) and a 600-V Si CoolMOS (IPZA60R180P7) at V_{BUS} higher than 400 V are tested. Before the short circuit test, the DUTs are put on curve tracer for the off-state I-V characteristics. The BV_{AVA} of the tested SiC MOSFET is around 1080 V and around 650 V for the Si CoolMOS (Figure 5-9).

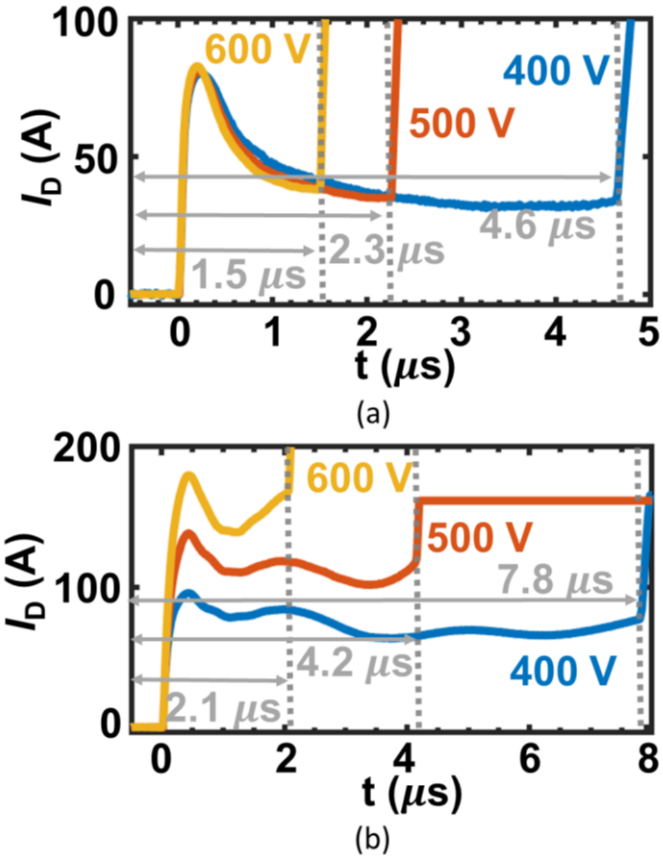


Figure 5-10. Short circuit test failure waveforms of (a) SiC MOSFETs (C3M0120065K) and (b) Si CoolMOS (IPZA60R180P7). The t_{SC} of each test is marked in the waveform.

The short circuit tests are performed on the same short-circuit test board but with a MOS-type gate driver. R_{ON} is 10 Ω and R_{OFF} is 2 Ω in the gate driver; the on-state gate drive voltage is 15 V. At 600 V (below the BV_{AVA} of SiC MOSFETs and Si CoolMOS), their t_{SC} is around 1.5~2.1 μs (Figure 5-10). At V_{BUS} higher than 600 V, the two types of DUTs almost failed immediately with a device current reaching our measurement compliance and a shorting observed between all three terminals in each DUT. These test results suggest the lack of the short-circuit capability nearing BV_{AVA} in these devices.

5.3 Repetitive Short Circuit Test

The repetitive short circuit test is first performed at 400 V and V_{BUS} is then increased to 600 V to further explore DUT's robustness. SC duration is set as 10 μs for each pulse, and period is 3 s in both the tests. Test setup is the same as the one described in Figure 5-1(a).

In the 400 V test, no failure is observed after 30,000 cycles of SC stress. Before and after the test, DUT is characterized in a 400 V, 4 A double pulse test (DPT). Figure 5-11 shows the turn-on and turn-off waveforms of the DUT and a fresh device in the DPT, showing good agreement. This suggests no degradation in the DUT's characteristics.

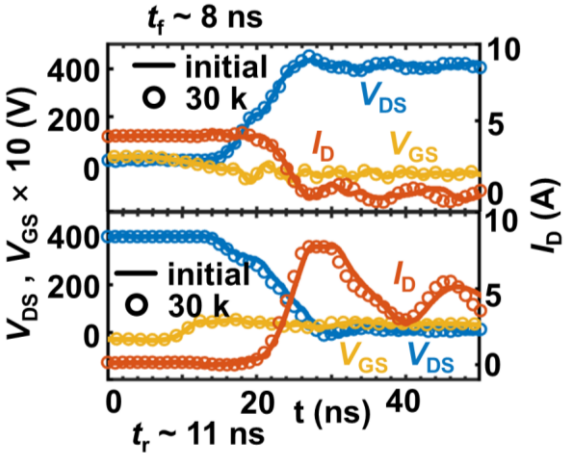


Figure 5-11. Turn-off and turn-on switching waveforms before and after 30,000 cycles of 400 V, 10 µs short circuit stress.

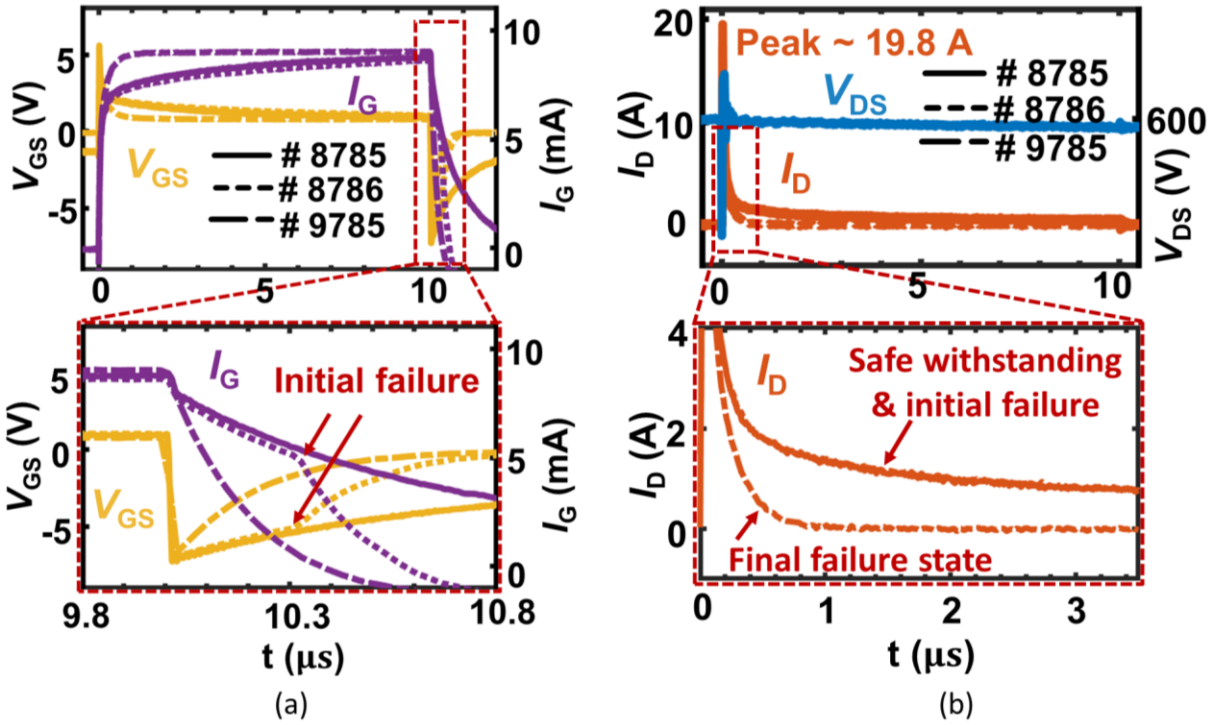


Figure 5-12. (a) V_{GS} and I_G waveforms in 600 V repetitive short-circuit tests and the zoom-in at the pulse ending phase. The failure initiates in cycle # 8786. (b) I_D waveforms in 600 V repetitive short-circuit tests, and the zoom-in at the pulse starting phase.

In the 600 V repetitive test, the DUT survived over 8,000 SC cycles. The failure initiated in cycle #8786. As shown in Figure 5-12, V_{GS} rises from negative value to zero, implying a G-S partial short while D-S remains open. The final failure state is reached in cycle #9785. In this stage, the DUT can still withstand short-circuit stress with a lower I_D: after the DUT is pulsed on, V_{GS} quickly drops to zero due to the partially shorted G-S terminals. As a result, the thermal stress in the short circuit test is reduced and the DUT would not suffer from further damage. This non-destructive and progressive failure can be understood from the output characteristics as shown in Figure 5-13: the gate functionality is retained in the failed DUT; a consistent I_D decrease is present from the initial failure (cycle #8786) to the final failure (cycle #9785). I_D quickly reduces to 0 in the final failure state due to the partial shorted G-S junction. This progressive failure process lasting for ~1000 pulses could be due to a gradual accumulation in the number of failed fins, with each fin failing with a G-S short.

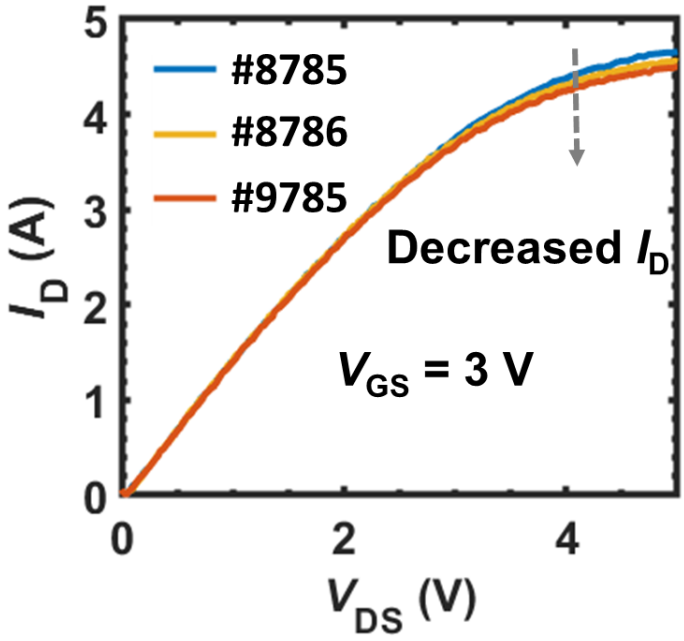


Figure 5-13. Output characteristics of the DUT in 600 V repetitive SC tests.

To further explore the device parametric shift as the SC pulse prolongs, DUTs are characterized periodically to track any possible parameter shift in 600 V SC repetitive test. Figure 5-14(a) shows the I_G drift when blocking high V_{DS}. A gradual increase in the gate leakage current is observed as the repetitive SC test prolongs, and this saturates after thousands of pulses. Meanwhile, the I_D drift (Figure 5-14(b)) is found to be much smaller than I_G shift. Therefore, I_G path is located between

gate and source. Note that the gate leakage and drain leakage current measurements are performed a few minutes after the end of repetitive stress. It is still unknown if this parametric shift is recoverable or permanent. However, as this I_G increase is consistent with the device behavior at the final failure stage, we believe that I_G could be a viable precursor to device failure and degradation, which can be therefore used for device condition monitoring.

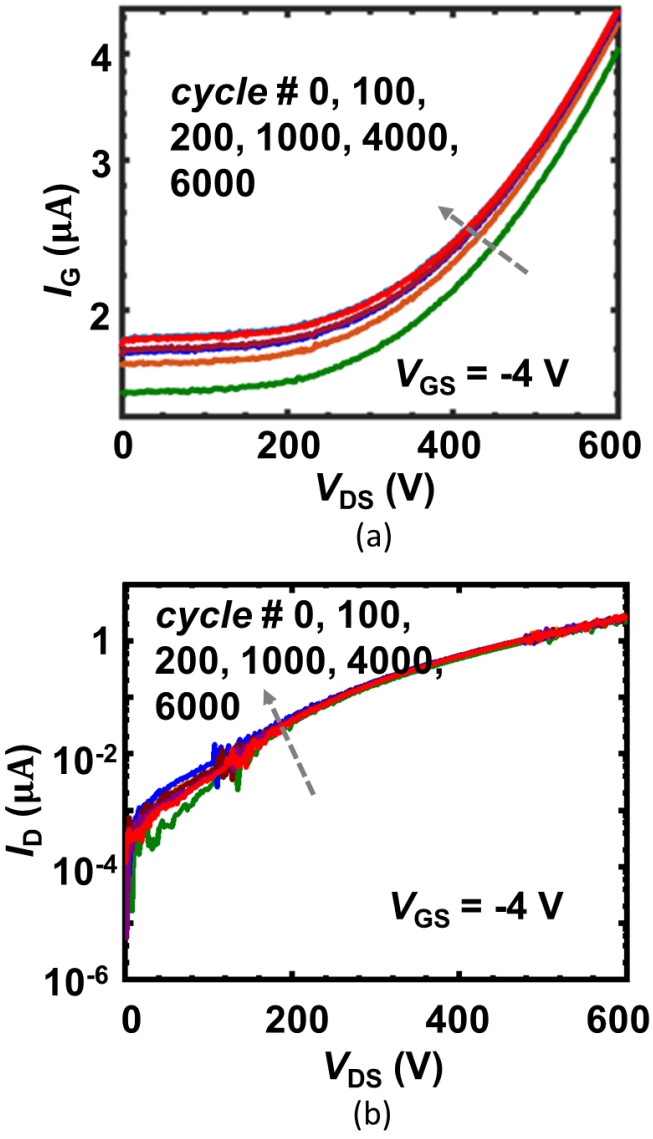


Figure 5-14. Drift in (a) gate leakage and (b) drain leakage during the 600 V repetitive short circuit test.

5.4 Benchmark and Summary

Table 5-2 summarizes this work and prior reports on single-event and repetitive short-circuit capabilities of 600~700-V GaN, SiC and Si unipolar normally-off devices [62], [136], [137], [138], [144], [145]. Figure 5-15 benchmarks their t_{SC} versus V_{BUS} capabilities. The GaN Fin-JFETs show the smallest specific R_{ON}, the highest t_{SC} and short-circuit energy density at 400 V (7.5 J/cm^2), no degradation in the repetitive 10 µs short-circuit tests at 400 V, a failure-to-open signature, and unique short-circuit capabilities at V_{BUS} close to the device BV_{AVA}. These results set a new record for the GaN power transistor short-circuit capability and illustrate that GaN devices with proper designs can achieve comparable or even superior short-circuit capability when compared to Si and SiC MOSFETs and SiC cascode JFETs. Meanwhile, in the repetitive short-circuit test, The DUT was found to withstand 30,000 cycles of 400 V, 10 µs SC stress without showing any degradation. At a higher V_{BUS} (600 V) close to the DUT rated voltage, DUTs survived over 8,000 cycles. Device degradation occurred at the lateral G-S junction, which leads to the G-S short and D-S open failure signatures. This open-circuit failure is highly desired in applications as it protects the whole system from catastrophic shorting in abnormal events.

As a further discussion, it is believed that the JFET structure is the key enabling factor for the

Table 5-2. Summary of the reported shorr-circuit test results of 600~700 V normally-off unipolar GaN, SiC and Si power transistors

Device	Type & Reference	Specific R_{on} (mΩ·cm^2)	Single Short Circuit Test				Repetitive Short Circuit Test				
			V_{bus} (V)	t_{SC} (µs)	E_{SC}[a] (J/cm^2)	Fail[b]	V_{bus} (V)	t_{SC} (µs)	Cycle period	Cycle number	Fail
Vertical GaN Fin-JFET (This work)		0.7	400 800	30.5 11.6	7.50 6.15	open	400	10	3 s	30,000	no
GaN HEMTs	Comm.[c] [62]	N/A	400	0.62	N/A	short	300	0.2	2 min	7	yes
	R&D [137]	N/A[d]	400	3	N/A	N/A			N/A		
	R&D [138]	19 Ω·mm[e]	400	4-10	N/A	N/A					
SiC/Si JFET cascode [144]		1.05	400	10	N/A	N/A	400	8	N/A	100	no
SiC MOSFET	Comm. [136]	N/A	400	13	N/A	open			N/A		
	R&D [145]	7.2	400	8.4	6.0	N/A					
Si CoolMOS	Comm. [145]	10	400	19	6.7	N/A			N/A		

Note: [a]critical short-circuit energy density. [b]failure signature. [c]commercial. [d]1.35X higher than commercial cascode HEMT. [e]~ 4.3 mΩ·cm^2 using a 20-µm source-to-drain length and 3-µm contact finger width.

high short-circuit capabilities observed in GaN Fin-JFETs. The JFET can effectively suppress

$I_{D,SAT}$ under the short-circuit stress, and high short-circuit capabilities have been reported in SiC JFETs [146]–[149]. While the short-circuit performance of industrial SiC casode JFETs has been included in Table 5-2, many other reports on normally-off and normally-on standalone SiC JFETs exist in the literature. Table 5-3 summarizes the reported short-circuit capabilities of 600 V and 1.2 kV standalone SiC JFETs, many of which show excellent t_{SC} at a bus voltage of 300-600 V. Note that of most of today's standalone SiC JFETs are normally-on, while the GaN Fin-JFET is normally-off. The viability and advantages of GaN Fin-JFET on realizing the normally-off operation have been explained in [48].

In addition to reporting GaN Fin-JFET's breakthrough short-circuit capabilities, we also unveiled the key enabling device physics. Owing to the characteristics of the junction gate stack and the *R*-*C* interface gate driver, GaN Fin-JFET can effectively suppress its $I_{D,SAT}$ during the short-circuit withstanding process, thus enabling a long t_{SC}. The avalanche-through-fin mechanism allows for a large avalanche current through the fin channel and thus enables the unique short-circuit capability at a bus voltage close to the device BV_{AVA}. Our results show the great potential of vertical GaN Fin-JFETs for applications like EV powertrains, motor drives, and grids, due to their excellent robustness under the concurrent presence of short-circuit and overvoltage stresses.

Table 5-3. Summary of the reported short circuit et results of 600-V and 1.2 kV SiC JFETs

Voltage Rating (V)	Operation Type	Temperature (°C)	Single Short Circuit Test			
			V_{bus} (V)	t_{SC} (µs)	E_{SC}[a] (J/cm^2)	Fail[b]
600	normally-on [146]	125	300	45	N/A	N/A
1200	normally-on [147]	25	600	300	N/A	N/A
1200	normally-on [148]	25	400	660	60	short
		350	400	6	N/A	N/A
1200	normally-off [149]	25	400	1440	44.6	short

Note: [a]critical short-circuit energy density. [b]failure signature.

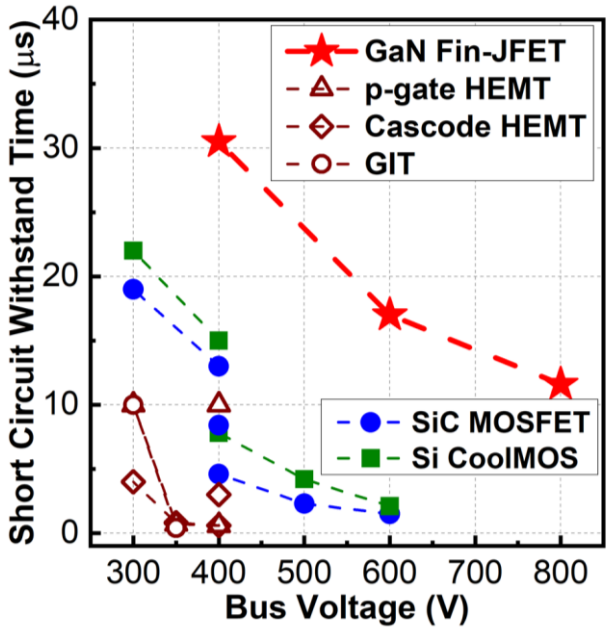


Figure 5-15. t_{SC} *vs.* V_{BUS} benchmark for GaN Fin-JFETs and other 600~700 V GaN, SiC and Si devices. Data are from the literature reports in Table 5-2 and our measurements shown in Fig. 5-10.

Chapter 6: Conclusions and Future Work

6.1 Summary of Work

6.1.1 Overvoltage Robustness of Lateral GaN HEMTs

The study begins with the single-event UIS test on commercial p-gate E-mode GaN HEMTs. The test results show that GaN HEMTs withstand the surge energy via a capacitive charging process. Once the peak V_{DS} reaches the device dynamic *BV*, catastrophic failure will occur. The failure mechanism is identified to be the electric failure induced by high E-field located at HEMT drain edge. The key takeaway from the UIS test is that, due to the lack of avalanche mechanism, GaN HEMT surge energy robustness is limited by its overvoltage robustness. Dynamic *BV* is the parameter that directly reflect the robustness instead of the amount of surge energy.

Followed by the traditional UIS test, GaN HEMT's *BV* dependency on pulse width (or the switching speed dv/dt) is studied by the UIS setup with tunable pulse widths. The test results unveil that GaN HEMT's dynamic *BV* is influenced by the dynamic charge trapping in the buffer layer, and it shows a decreasing trend with the increased pulse width (or reduced dv/dt) until the dynamic *BV* converges to the static *BV* with increasing overvoltage duration. Finally, repetitive UIS test is performed at 1 kHz and 20 kHz, the variation in device failure indicates a frequency dependent BV_{DYN} which opens up the idea of performing the high frequency overvoltage test.

In chapter 3, a novel ZVS buck converter based HFOT test setup is designed and demonstrated. It enables a f_{sw} to 1 MHz at kilovolt voltage overshoot in the GaN HEMT overvoltage test by avoiding the limitations of the UIS or CIS test: long inductive energy dissipation time is required in the natural damping, and device self-heating can be present in the reverse conduction. The HFOT test can best resemble the application scenario. New understandings on GaN HEMTs overvoltage robustness are also illustrated through testing four mainstream commercial GaN HEMTs. While *DUT#1* and *#2* show the f_{sw} independent BV_{DYN}, DUT#3 and #4 show a clear BV_{DYN} deduction when increasing the f_{sw} from 2 kHz to 1 MHz. Two new degradation mechanisms, i.e., a drastic, nearly non-recoverable R_{ON} increase and a degradation in the off-state leakage, have been identified. The results in chapter 3 highlight the necessity of adopting application-based testing methodology in GaN HEMT robustness study.

Extended studies have proved that, by optimizing circuit parameters in the UIS test, repetitive UIS test can be run at 200 kHz and is a powerful tool for GaN HEMT overvoltage robustness qualification. Finally, after understanding the failure boundary and degradation mechanisms through deploying the new testing methodologies, GaN HEMT's lifetime under overvoltage switching is studied with a high frequency UIS test setup with the accurate in-situ R_{ON} monitoring. A first-principle physical trapping model is used to project GaN HEMT lifetime under high frequency transient voltage overshoot. The accuracy is validated by experimental data under different peak V_{DS}.

Overall, the study on GaN HEMT overvoltage robustness follows a step-by-step process. It starts with the easily implemented single-event robustness test, in which all the DUTs are tested to failure with new device physics and failure mechanisms unveiled, such as the E-field dominant, dynamic breakdown voltage. The unveiled mechanisms in turn inspire the new ideas on performing the high frequency repetitive overvoltage test. While the failure mechanisms have been clearly understood, the testing conditions are tuned to be less harsh with a lower peak V_{DS}, from which frequency dependent degradation mechanisms are identified. Such tests highlight the importance of performing the application-based mission profile test on GaN HEMTs. Lastly, the study is further extended to GaN HEMT reliability study by providing a universally applicable testing methodology and device lifetime models. The findings presented in this dissertation provide key guidelines for device users and key information for GaN HEMTs manufacturers for enhancing their devices' robustness.

6.1.2 Overvoltage Robustness of Vertical GaN Fin-JFETs

The study on the emerging vertical GaN Fin-JFET follows a more traditional way with the focus on device avalanche and short circuit robustness. The vertical GaN Fin-JFETs are found to be robust under both avalanche and short circuit scenario: the recorded critical E_{AVA} in single-event avalanche is 10 J/cm^2. They withstand over 3700 repetitive avalanche pulses at 70% of E_{AVA}. It exhibits a failure-to-open-circuit signature in single and repetitive avalanche. This soft failure mode allows the device to retain its full breakdown voltage, which is highly desirable for system robustness. Such avalanche and short-circuit robustness are demonstrated in vertical GaN transistors for the first time.

The t_{SC} of GaN Fin-JFETs is measured to be 30.5 μs at a V_{BUS} of 400 V, 17.0 μs at 600 V, and 11.6 μs at 800 V, all among the longest reported for 600-700 V normally off transistors. Meanwhile, the failure-to-open-circuit signature is also shown in the short circuit test. In repetitive short circuit test, they survive 30,000 cycles of 400 V, 10 μs SC stresses without any degradation in device characteristics. At a 600 V V_{BUS}, it survived over 8,000 cycles of 10 μs SC stresses before an open-circuit failure.

Besides the robustness testing data, unique device physics are also identified in vertical GaN Fin-JFET, including the "avalanche-through-fin" mechanism and the exceptional short circuit capability near its BV_{AVA}. The repetitive testing also reveals the lateral gate-to-source junction to be the most vulnerable location in GaN Fin-JFET, providing key information for further improvement of the device robustness as well as the device online monitoring.

6.2 Future Work

Although the dissertation work covers many of the important topics in GaN device robustness study, there are still some open knowledge gaps remains to be explored regarding GaN HEMTs robustness, reliability and stability, which are included in [39], [41]. The section briefly presents the author's thoughts on some specific topics:

A. Factors that limit GaN HEMT t_{SC}

GaN HEMTs are known to be vulnerable under short circuit, but the reasons are still under debate. Since the channel pinch-off only occurs underneath the p-gate region when GaN HEMTs operate in the saturation region. The localized heat generation underneath the gate could be the bottleneck that limits GaN HEMTs t_{SC}, however, no relevant study has been published up to date.

B. Measurement of the dynamic R_{ON}

Clipper circuits are required in characterizing GaN HEMTs dynamic R_{ON}, but the RC discharging delay from the voltage clipper can mix up with the V_{DS} signal hence giving misleading dynamic R_{ON} characterization results. Therefore, it is critical to provide guidelines on clipper circuit design, as well as on proper data processing methods for the dynamic R_{ON} study.

C. Further implementation of the HFOT

With the test methodology and prototype of HFOT, further studies on GaN HEMT lifetime modeling can be conducted by combining HFOT with the in-situ R_{ON} measurement. The first advantage of the HFOT with ACC is the access to a wider range of switching frequency, from several kHz to 1 MHz, hence the R_{ON} evolution data under higher f_{sw} can be obtained. The second advantage is that the HFOT with ACC eliminates the DUT reverse conduction in comparison with the UIS test, hence the thermal stress in the HFOT is more manageable, and DUT R_{ON} evolution under different temperature can be accessed.

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Appendix A: GaN HEMT UIS Mixed-mode TCAD Simulation Script for Silvaco

```
go atlas

#simflags="-128"

set w_s=3

set w_d=3

set l_g=2

set w_sg=1

set w_gd=11

set w_recess=1.5

set w_space=0.5

set h_barrier=0.015

set h_barrier_recess=0.015

set h_ohm=0.01

set h_die=0.0

set h_metal=0.3


set h_pgan=0.04

set h_ohm_metal=0.3

set h_gate=0.5

set h_air=6

set y_gate=$"h_gate"+$"h_ohm_metal"

set y_air=$"y_gate"+$"h_air"
```

```
set w_gwing=($"l_g"-$"w_recess")/2

set y_pgan=$"h_pgan"+$"h_barrier"

set h_sub=0.1

set h_ch=1.8

set h_buffer=3.8

set w_dpl=1

set w_dpd=0.5

set w_dpr=0

set w_fps=2.2

set w_fpg=0

set w_fpd=0.2

set h_ch0=0.01

set label=hemt_mix_5


mesh

# three.d

x.mesh loc=0.00 spac=$"w_d"/3

x.mesh loc=$"w_s" spac=$"w_sg"/5

x.mesh loc=$"w_s"+$"w_sg"/2 spac=0.1

x.mesh loc=$"w_s"+$"w_sg"   spac=$"w_sg"/4

x.mesh loc=$"w_s"+$"w_sg"+$"w_gwing"  spac=$"w_recess"/4

x.mesh loc=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"  spac=$"w_gwing"/6

x.mesh loc=$"w_s"+$"w_sg"+$"l_g" spac=$"w_gwing"/6

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_fpg"  spac=$"w_gwing"/4
```

```
x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_fps"  spac=$"w_gwing"/3

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_fps"  spac=$"w_gwing"/3

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"/2 spac=$"w_gd"/20

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpl"-$"w_fpd" spac=$"w_gwing"/5

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpl" spac=$"w_gwing"/4

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpd" spac=$"w_gwing"/4

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpr" spac=0.25

x.mesh loc=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"+$"w_d"  spac=$"w_d"/2


y.mesh loc=-$"y_air" spac=1

y.mesh loc=-$"y_gate"  spac=0.15

y.mesh loc=-$"h_ohm_metal"  spac=0.1

y.mesh loc=-$"y_pgan"  spac=0.002

y.mesh loc=-$"h_barrier"-$"h_die" spac=0.005

y.mesh loc=-$"h_barrier" spac=0.005

y.mesh loc=-$"h_barrier_recess"   spac=0.003

y.mesh loc=-0.001  spac=0.0005

y.mesh loc=0  spac=0.0005

y.mesh loc=0.001  spac=0.0005

y.mesh loc=$"h_ohm"  spac=$"h_ohm"/3

y.mesh loc=$"h_ch0"  spac=$"h_ohm"

y.mesh loc=$"h_ch"   spac=$"h_ch"/8

y.mesh loc=$"h_buffer"*2/3  spac=$"h_buffer"/10

y.mesh loc=$"h_buffer"  spac=$"h_sub"/4
```

#y.mesh loc=$"h_buffer"+$"h_sub" spac=$"h_sub"/4

region num=1 material=SiN y.min=-$"y_air" y.max=-$"h_barrier"-$"h_die"

region num=2 material=GaN y.min=0 y.max=$"h_ch0"

region num=3 material=SiO2 y.min=$"h_ch0" y.max=$"h_ch"

region num=4 material=Al2O3 y.min=-$"h_barrier"-$"h_die" y.max=0

region num=5 material=GaN x.min=$"w_s"+$"w_sg" x.max=$"w_s"+$"w_sg"+$"l_g" y.min=-$"y_pgan" y.max=-$"h_barrier"

region num=6 material=AlGaN x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"+$"w_d" x.min=0 y.min=-$"h_barrier" y.max=0 x.comp=0.25

#region num=6 material=AlGaN x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd" x.min=$"w_s" y.min=-$"h_barrier_recess" y.max=0 x.comp=0.25

#region num=6 material=AlGaN x.max=$"w_s"+$"w_sg"+$"w_gwing" x.min=$"w_s" y.min=-$"h_barrier" y.max=-$"h_barrier_recess" x.comp=0.25

#region num=6 material=AlGaN x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd" x.min=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess" y.min=-$"h_barrier" y.max=-$"h_barrier_recess" x.comp=0.25

region num=7 material=Al2O3 y.min=$"h_ch" y.max=$"h_buffer" x.comp=0.1

region num=8 material=GaN x.min=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpl" x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd" y.min=-$"y_pgan" y.max=-$"h_barrier"

```
elec num=1 name=gate     x.min=$"w_s"+$"w_sg"+$"w_gwing"
x.max=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess" y.min=-$"h_ohm_metal" y.max=-
$"y_pgan"

elec num=2 name=source   x.min=0 x.max=$"w_s"  y.min=-$"y_gate" y.max=-$"h_barrier"
elec num=2 name=source   x.min=0 x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_fps"  y.min=-
$"y_air"  y.max=-$"y_gate"

elec num=3 name=drain    x.min=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"
x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"+$"w_d"  y.min=-$"y_air" y.max=-$"h_barrier"
elec num=3 name=drain    x.min=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"
x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"  y.min=-$"y_gate" y.max=-$"y_pgan"
#elec num=3 name=drain    x.min=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpd"
x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"  y.min=-$"y_gate" y.max=-$"y_pgan"
elec num=3 name=drain    x.min=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"-$"w_dpl"-$"w_fpd"
x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"   y.min=-$"y_air" y.max=-$"y_gate"
elec num=4 name=sub      bottom

doping region=5 uniform p.type conc=1.6e18

save outf=$"label"_structure.str
tonyplot $"label"_structure.str

go atlas
#
# This example demonstrates gate charge characteristics of a DMOS structure.
```

```
#
# SPISCES, MIXEDMODE was used
#
# Part 1: Steady state solution
# Circuit descriptions
#
.begin
#
vg  0  4  0
r1   4  1  2
l1   2  3  14.2uH
ainfineon  1=gate  2=drain  0=source 0=sub  infile=$"label"_structure.str width=3.85e5
#width=2.86e5
vin 3 0 0
#
# End of circuit description
#
.model ideal d()
#
.nodeset v(1)=0 v(2)=0 v(3)=0
#
.numeric lte=0.05
#
.options fulln print
```

```
#
.save outfile=$"label"_steady
#
.log outfile=$"label"_steady
#
.dc vg 0 -5 -0.1
.dc vin 0 1 0.1
.dc vin 1 30 0.2

#.save master=$"label"

.end

################################
#  material characteristics #
################################



################################
#  gate-source contact      #
################################
contact  device=ainfineon name=source  workfun=4.04
contact  device=ainfineon name=drain   workfun=4.04
#contact   name=gate    workfun=4.6
```

```
contact  device=ainfineon name=gate    workfun=5.2
##############################
#  impact models           #
##############################
impact device=ainfineon selb material=GaN

models device=ainfineon region=2 srh fldmob  print
mobility device=ainfineon region=2 FMCT.N Gansat.N  mu2n.fmct=1200

mobility device=ainfineon region=5 albrct.p bp.albrct=1e04 ap.albrct=1e04
model device=ainfineon region=5 pch.ins

trap region=2 device=ainfineon donor e.level=3.2 density=1.27e18 sign=1e-15 sigp=1e-15
degen=2
trap region=2 device=ainfineon acceptor e.level=0.36 density=7e17 sign=1e-15 sigp=1e-15
degen=4

#model device=ainfineon ten.piezo psp.scale=0.67 piezo.scale=0.67 calc.strain
interface device=ainfineon x.min=0 x.max=$"w_s"+$"w_sg"+$"w_gwing" y.min=-0.001
y.max=0.001 charge=6e12 s.s
#interface device=ainfineon x.min=5.6 x.max=6 y.min=-0.02 y.max=-0.01 charge=3e14 s.s
interface device=ainfineon x.min=$"w_s"+$"w_sg"+$"w_gwing"
x.max=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess" y.min=-0.001 y.max=0.001 charge=2e12
s.s
interface device=ainfineon x.min=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"-0.5
x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"+$"w_d" y.min=-0.001 y.max=0.001 charge=1e13 s.s
```

```
#interface  x.min=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"
x.max=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"+0.5 y.min=-0.001 y.max=0.001
charge=1e14 s.s

method block newton trap px.tol=1e-2  clim.dd=1e15 dvmax=1e12 itlim=100 nblockit=30
maxtrap=10 carriers=1 elec
#carriers=2

output con.band val.band band.param flowlines charge traps e.mob h.mob e.vel ex.vel ey.vel
h.vel hx.vel hy.vel qss polar.charge

go atlas
# Part 2: Transient Solution
# Circuit descriptions
#
.begin
#
vg  0  4  -5  pulse -5 3 1e-10 1e-9 1e-9 0.96e-6 4e-6
r1   4  1  2
l1   2  3  14.2uH
ainfineon  1=gate  2=drain  0=source 0=sub  infile=$"label"_structure.str width=3.85e5
#width=3e5
vin 3 0 30

# End of circuit description
```

```
#
.model ideal d()
#
.numeric vchange=0.01 imaxtr=50
#
.load infile=$"label"_steady
.save outfile=$"label"_tr
.save master=$"label" tsave=1e-9, 2.21e-9, 5e-9, 1e-8, 0.9e-6, 0.905e-6, 0.910e-6, 0.915e-6,
0.920e-6, 0.95e-6, 1e-6, 2e-6, 2.5e-6, 3e-6, 3.5e-6, 4e-6
#
.options fulln print
#
.log outfile=$"label"_transit
#
.tran 25ps 10e-6
#
.end
#


##############################
#  material characteristics #
##############################
```

```
##############################
#  gate-source contact      #
##############################
contact  device=ainfineon name=source  workfun=4.04
contact  device=ainfineon name=drain   workfun=4.04
#contact   name=gate    workfun=4.6
contact  device=ainfineon name=gate    workfun=5.2
##############################
#  impact models           #
##############################
impact device=ainfineon selb material=GaN

models device=ainfineon region=2 srh fldmob  print
mobility device=ainfineon region=2 FMCT.N Gansat.N  mu2n.fmct=1200

mobility device=ainfineon region=5 albrct.p bp.albrct=1e04 ap.albrct=1e04
model device=ainfineon region=5 pch.ins

trap region=2 device=ainfineon donor e.level=3.2 density=1.27e18 sign=1e-15 sigp=1e-15
degen=2
trap region=2 device=ainfineon acceptor e.level=0.36 density=7e17 sign=1e-15 sigp=1e-15
degen=4

#model device=ainfineon ten.piezo psp.scale=0.67 piezo.scale=0.67 calc.strain
```

interface device=ainfineon x.min=0 x.max=$"w_s"+$"w_sg"+$"w_gwing" y.min=-0.001 y.max=0.001 charge=6e12 s.s

#interface device=ainfineon x.min=5.6 x.max=6 y.min=-0.02 y.max=-0.01 charge=3e14 s.s

interface device=ainfineon x.min=$"w_s"+$"w_sg"+$"w_gwing" x.max=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess" y.min=-0.001 y.max=0.001 charge=2e12 s.s

interface device=ainfineon x.min=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"-0.5 x.max=$"w_s"+$"w_sg"+$"l_g"+$"w_gd"+$"w_d" y.min=-0.001 y.max=0.001 charge=1e13 s.s

#interface x.min=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess" x.max=$"w_s"+$"w_sg"+$"w_gwing"+$"w_recess"+0.5 y.min=-0.001 y.max=0.001 charge=1e14 s.s

method block newton trap px.tol=1e-2 clim.dd=1e15 dvmax=1e12 itlim=100 nblockit=30 maxtrap=10 carriers=1 elec

#carriers=2

output con.band val.band band.param flowlines charge traps e.mob h.mob e.vel ex.vel ey.vel h.vel hx.vel hy.vel qss polar.charge

quit