

Development of Chip-Scale Power Packages Using Solder Joint Interconnection

Chip scale packaging (CSP) of integrated chips is gaining acceptance widely because of its intrinsic size advantages, the promise of highly favorable cost/performance trade-offs and reliance on existing materials and assembly infrastructures. Chip Scale Packaging (CSP) is being considered as the future area array solution to satisfy the evolutionary growth in I/O densities that are demanded by ever increasing levels of silicon performance and integration in integrated circuit field. Actually, in power electronics packaging area, CSP can enable a few very important concepts and advantages. Solder joint interconnection for power chips offers a great potential of developing chip-scale power packages. We have developed two kinds of chip-scale power packages. One is called cavity down flip chip on flex; the other is termed Die Dimensional Ball Grid Array (D²BGA). Both utilize solder joint as chip-level interconnection. These CSPs make high-density packaging and module miniature possible, enable the power chip to combine excellent thermal transfer, high current handling capability, improved electrical characteristics, and ultra-low profile packaging. Electrical tests show that the $V_{CE(sat)}$ of the high speed IGBT chip-scale packages is improved by 20% to 30% by eliminating the device's wirebonds and other external interconnections, such as leadframe. In this chapter, the design concepts are presented and the package structures are introduced. We also discuss the material issues and describe the fabrication process of chip-scale packages. The electrical and reliability test results of the CSPs are reported. Finally, the application of these CSPs is discussed.

5.1 Introduction to Chip-Scale Power Packaging

JEDEC defines the chip scale package (CSP) as any package that is no more than 20% larger than the die. CSPs come as either peripherally leaded or grid-array devices, such as BGAs. CSPs can potentially meet demands for smaller components and greater electrical performance. These components reduce packaging well beyond what is possible with standard leadframe packages. CSPs can occupy less than one-fifth the area, one-half the weight, and two-thirds the mounting height of the thinnest leadframe packages. Their very short interconnects

reduce parasitics over other package styles. To achieve acceptable levels of parasitics in high-speed designs, interconnects need to be optimized.

Incremental advances in silicon and its various process technologies reduced the resistance of power semiconductors, i.e. on-resistance (R_{ds}) of MOSFETs, but the packaging resistance becomes as much as 25 to 40 percent of the total [1]. As a result, more and more of power semiconductor manufacturers are specifically paying attention to the "box" holding the chips. The efficiency demands of electronics, heat dissipation and board real estate are pushing smaller packages toward the chip-scale ideal with the same die performance and thermal characteristics be developed. However, circuit assembly and packaging technologies for power electronics [2] have not kept pace with those for microelectronics. The state-of-the-art packaged power devices (for example, IGBTs, MOSFETs) are in the forms of single-in-line package (SIP), dual-in-line package (DIP), small outline package (SO or SOP), and quad flat pack (QFP), which have large size, high resistance and parasitics, poor thermal management and high cost. Inside those power devices, chip-level interconnection is accomplished with wirebonds. Wirebonds in power devices are prone to resistance, noise, parasitic oscillations, fatigue and eventual failure. For most of the power electronics applications, like an inverter module, the power devices are switching at high di/dt and dv/dt , and they generate a high electromagnetic field, resulting in proximity effects and uneven current distribution among the bonding wires [3-5]. To mitigate the reliability problems associated with wire bonds, power device manufacturers improved the composition of the wire, the shape of the bonding tool, the bonding parameters, the metallization on leads and the protective coatings rather than exploring alternative device interconnection schemes. To improve performance and reliability of packaged power electronics, wire bonds need to be replaced.

Chip Scale Packaging (CSP) is being considered as the future area array solution to satisfy the evolutionary growth in I/O densities that are demanded by ever increasing levels of silicon performance and integration in integrated circuit field. However, the concept of chip scale packaging is yet to be put forward in power electronics packaging area. Actually CSP can enable a few concepts and advantages in power electronics packaging. First, chip scale package provides the power processing element for multichip power module in a surface mount package, just like the conventional single chip power packages, but smaller size. CSP reduces package size well beyond what is possible with standard leadframe packages. Second, CSP is a potential

low-cost known-good-die (KGD) solution for multichip power module packaging. One of the toughest issues for MCM packaging is KGD supply, and the problem has yet to be overcome. Burn-in and testing technologies that are cost competitive are still under development. Especially in power electronics, testing bare dies (such as MOSFETs, IGBTs) at levels of several hundred to thousand volts and hundreds of amps is currently impossible. Chip-scale packaged power devices can be readily handled and tested at full power ratings, thus providing a KGD solution. Third, standardization issue on power components and PWB design could be solved. Power components standardization is necessary to insure multiple source availability. Industry standard I/O pitch for area array technologies and PCB ground rules are established. Sockets in a dense full area array format for BGA package test and burn-in are available. Therefore, power electronics industry may take advantage of the standard, widely available resources. Fourth, CSP provides a vehicle for getting rid of wire bonds, which can be the bane of power electronics module reliability. Lastly, CSP offers greater electrical performance by eliminating wire bond and leadframe parasitics and reducing copper track parasitics. The reduced package size and lower package profile allows shorter and wider signal and power traces.

As introduced in Chapter I, Fairchild and IR used solder joints as MOSFET interconnection and developed their chip-scale power packages recently [6-9]. Figure 5.1 shows Fairchild's BGA MOSFET and Figure 5.2 shows IR's FlipFET structure. By allowing direct connection of the power chips to the substrate, the BGA package and FlipFET have eliminated the undesired contributions from the wirebonds and the leadframe. Therefore, these approaches have boosted the device's power-handling capability and there is a dramatic improvement in the thermal efficiency and heat-transfer ability, compared to equivalent devices in wirebonded packages. The combinations of lower voltage drop/on-resistance and superior heat-transfer characteristics at higher power levels make the transistor attractive for designing higher-efficiency power converters.

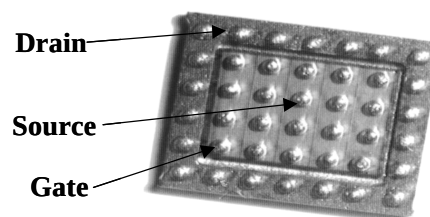


Figure 5.1. Fairchild's BGA MOSFET.



Figure 5.2. IR's FlipFET™ [10].

Harris Semiconductor developed a packaging technique for power devices such as IGBTs [11], which is basically also a chip scale power package. The design includes a metallized (Ti-Ni on Al) device on top of which a machined ceramic (Al_2O_3 or AlN) with metallized grooves is attached. The top side of the ceramic piece is patterned with conductor metallization while the bottom side of the ceramic is metallized with a Ni followed by a flash gold coating. The grooves are filled with Pb-Sn solder paste, which is reflowed to connect the contact pads of the devices to the top metallization on the ceramic. A schematic of the HTP structure is shown in Figure 5.3, where the solder contacts for different terminals of the devices are achieved on the top and bottom sides of the device.

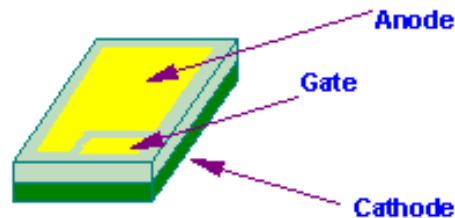


Figure 5.3. Schematic of a Harris Thin Pack with solderable contacts on both sides of the device [11]

We have developed cavity down flip chip on flex and Die Dimensional Ball Grid Array (D²BGA) chip scale power packages. Package design and process have been optimized to gain better electrical characteristics, realize compatible fabrication process to existing assembling capability, and achieve higher reliability. The two CSPs enable dense packaging of power chips and short interconnection distances, resulting in lower parasitic resistance and inductance. Besides, the top surface is covered by thick solder bumps, which promise increased power handling capability and better heat dissipation. The cavity down flip chip on flex and D²BGA CSPs are compatible with most surface-mount assembly operations and has the testability of a traditionally packaged device. In the following sections, the design concepts are presented and

the package structures are introduced; followed by a discussion of the material issues and description of the fabrication process. Finally, the electrical and reliability test results of the CSPs are reported and the application of these CSPs is briefly discussed.

5.2 Design Concepts and Package Structures

A power semiconductor package is preferred to have minimal parasitic resistance and inductance. High resistance will result in high conduction loss. Parasitic inductance affects device switching times and induces high turn-off voltage overshoot, which not only add electrical stress on the device, but also result in high switching losses and thus low overall efficiency. Since losses can not be avoided in power semiconductors, a package design should be efficient in dissipating heat. There is an ever-increasing demand to increase the power for a lot of applications such as switched mode power supply and telecom systems, and decline voltage levels (for example, for microprocessors, the voltage drops from 3.3 to 2.5 and 1.5 V), so the current is increasing. Therefore, a power semiconductor package should be able to handle high current. On the other hand, in many applications (such as portable and switched mode power supply applications), smaller package size is desired. Thus, power density is becoming increasingly important in package design. The need to supply the same or better functionality in a smaller outline is a serious challenge. Of course, a good package design also should satisfy the reliability requirement for power electronics applications. Therefore, basically electrical performance, thermal management, current handling capability, power density and reliability issues need to be addressed when considering how to design a power semiconductor package.

5.2.1 Parasitic Resistance and Inductance Reduction

Conventional power semiconductor packages use wire bonding to connect the leads of the package to the source of the die. It is difficult to design the sweep of wires from the chip to the leadframe in peripheral packaging to minimize resistance, self-inductance and mutual inductance between adjacent wires. Each wire bonds and lead frame has a finite resistance, adding to the $R_{DS(on)}$ of the device. A “wireless” chip interconnection could reduce the package resistance significantly. Also if die itself is the total package, we eliminate the lead frame resistance. One method to eliminate wire bonds is to form area arrayed solder bumps on the wafer which has been used in the IC industry to allow hundreds of connections to the IC in a

small space. Advantages of solder-bump interconnection of chips have been well documented in numerous research works [12-15]. In the power semiconductor field, the use of solder joints could reduce the resistance by allowing many parallel connections to be made from the source of the die to substrate directly or to the lead frame. Solder-bumped chips could have short pad-to-circuit connections for reduced coupled noise, low capacitance, and low self and mutual inductance, as illustrated in Figure 5.4.

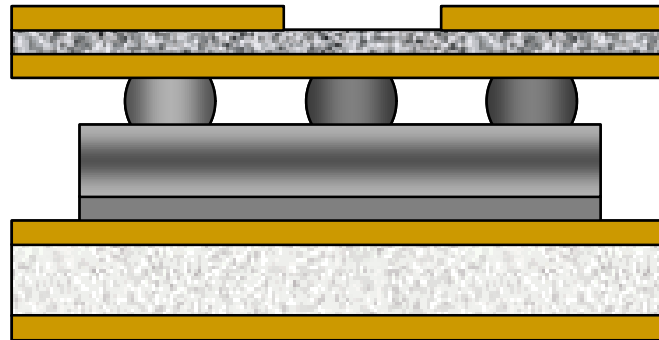


Figure 5.4. Cross-sectional view of solder joint area array interconnection of power chips.

5.2.2 Thermal Management

Thermal capability is measured with a thermal impedance known as R_{thja} , where lower is better, which is the thermal resistance from the junction of the silicon to the outer case of the device or ambient. Thermal capability can be affected by both the silicon and the package. Power semiconductor manufacturers obtained lower thermal impedance by reducing the thickness of a silicon wafer, or merely use a larger area of silicon to dissipate the heat. However, the heat generated by the power semiconductor eventually need to be dissipated out from the package. Packages can affect the thermal performance by allowing faster, more effective heat flow out of the device. Thus, the package should be designed ideally to have double-sided cooling, to have as few interfaces as possible, preferably no interface at all, and interface should be as thin as possible. On the other hand, packages can also improve the resistance of a device and hence improve the electrical performance and lower power dissipation. A preferred package design should make the chip-level interconnection as short as possible and increase the area of conducting contact from the electrode (source for MOSFET and emitter for IGBT) of a power semiconductor to the board-level connection.

A solder joint area array package is the right answer to the above two questions. As shown in Figure 5.5, a simple solder bumped chip package accomplishes both goals simultaneously by replacing the long wire-bonds with short solder joints and allowing substrate to be in direct contact with the solderable back-side of the power die. The solder joints and thermally conductive underfill material (if used) can act as heat paths because they are attached to the active surface of the silicon and are massive enough to draw heat away from the silicon. Therefore, thermal resistance of the package is improved by providing heat conduction from both the drain contact on the bottom of the package, and the source solder joints, as show in Figure 5.5. Fairchild claimed that BGA MOSFET improved heat dissipation over modified SO-8 by 175% and 250% over traditional wirebonded SO-8 package. A finite-element thermal analysis [16-17] indicated that 20-43% heat could be removed through the top solder joints.

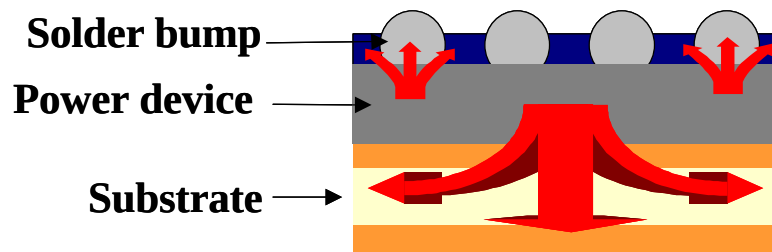


Figure 5.5. Double-sided cooling of designed CSPs.

5.2.3 Current Handling Capability

The ability of a package to handle current is inextricably linked to the thermal properties of a device as discussed earlier. A solder joint area array chip interconnection and optimal package structure could improve current handling capability of power packages. As demonstrated in Figure 5.6, solder-bump contacts provide a larger effective contact area between power semiconductor devices and outside circuitry. Obviously, thick solder bumps can carry larger currents than thin wire bonds. The larger contact area greatly reduces current crowding and eliminates the hot spots that could happen in wire bonds. In general, since power chips only have several I/O, power die pad size can be designed much larger than that of IC chips, which has much more I/Os. It is possible to use larger solder bumps or even BGA to interconnect power chips. Larger solder bumps can carry higher current, which enables those devices to be used in higher power level applications.

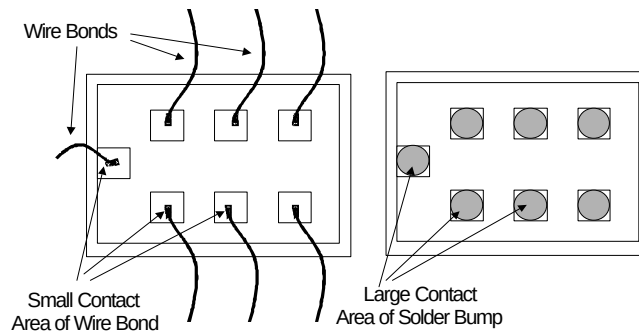


Figure 5.6. Comparison of contact geometries of wire bond and solder bump interconnection

5.2.4 Power Density

In an effort to meet the need for increased power density - power output per unit volume, it is critical to minimize footprint areas taken by power conversion devices. A good indication of power density is the silicon to footprint ratio. This is the ratio of silicon (die) in a package divided by the total footprint. Also, a performance measure of the packaged product can be expressed as a space figure of merit (FOM) which calculated as the device $R_{ds(on)}$ x Footprint Area.

Power chip packaging has been typically focused on peripheral packages with wirebonds as the chip level interconnects. The devices on the silicon die are routed from the center location on the chip to the wirebond pads on the periphery. The chip is attached to a substrate and is wirebonded to electrically connect the chip to the leadframe. The leadframe extends interconnects through a dielectric into a peripheral pattern, where it can be soldered to a printed wiring board. An alternative to peripheral interconnect packaging is to access the unused area under the chip using area-arrayed interconnects. In a solder joint area-array package, it is possible to achieve 100% silicon to footprint ratio and thus dramatically improve the power density.

5.2.5 Reliability Considerations

Thermal stresses caused by the CTE mismatch of silicon and substrate are the main reliability issues for solder bump interconnection. Fortunately, solder bump technology has the flexibility to extend the solder joint interconnections to accommodate larger and denser chips without affecting system reliability. More specifically, solder joint interconnection offers the opportunity to improve its reliability in the following areas: geometry or shape improvement;

alternate solders; use of compliant substrates and underfill encapsulant. A potential solution is to use greater standoff and hourglass-shaped solder interconnects, which have been demonstrated in Chapter III to have greater reliability. We have developed a stacked solder bumping process to control solder joint height and shape, and thus improved power chip solder joint interconnection.

Furthermore, wafer-level solder bumping and flip-chip bonding facilities are commercially available in IC industry. The solder bumping and flip chip bonding processes are compatible with most surface-mount assembly operations. Solder reflow process offers high process yield and high quality bonding. Recent cost study also shows that area array solder bump flip chip is cheaper than wire bonding [18]. Thus, solder joint area array interconnection potentially offers low cost power chip interconnection and also provides the possibility of power components standardization.

5.2.6 Package Structures

Having discussed the design considerations, it becomes clear that the most straightforward implementation of solder joint power chip interconnection in making chip scale power package is D²BGA package. D²BGA CSP is designed mainly for three-dimensional structure applications, such as 3-D MCM power modules, 3-D integrated power electronics modules (IPEMs). Figure 5.7 illustrates the structure and cross section of the D²BGA CSP. In order to achieve higher reliability, stacked solder joint structure is proposed which makes ready to form high standoff hourglass-shaped solder joint. Single solder bump can be used if the reliability requirement is not very high for some applications. The D²BGA CSP consists of a power chip, inner solder caps, high-lead solder balls, and molding resin (optional, just for the purpose of making the package easy to handle and robust). The surface of the package has an array of solder bumps that are connected to the chip source pads and one gate pad by inner solder caps and under bump metals. The backside (drain for MOSFET and collect for IGBT) is solderable and can be directly attached to substrate. This package has the same lateral dimensions as the starting power chip, thus offers 100% silicon to package footprint ratio. The very low on state resistance (on voltage drop for IGBT) $R_{DS(ON)}$ together with the minimum footprint area achieves high current density figures of merit. Figure 5.8 shows a D²BGA package with and without encapsulation. At this stage, burn-in testing on the packaged device can be carried out by soldering the package to a tester circuitry with a low melting solder.

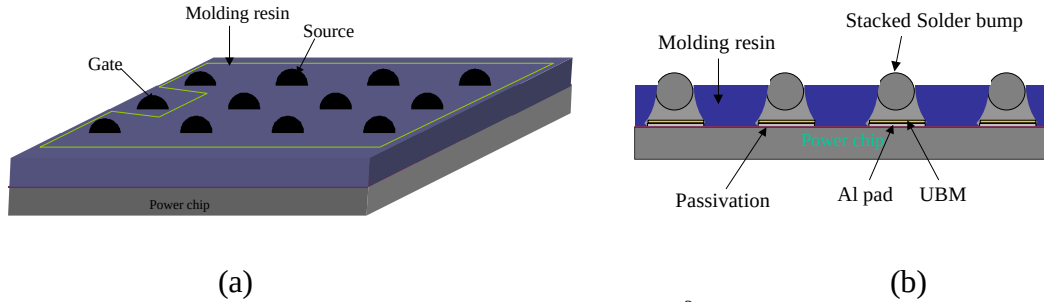


Figure 5.7. (a) The structure and (b) the cross sectional view of D²BGA chip-scale packaged power device.

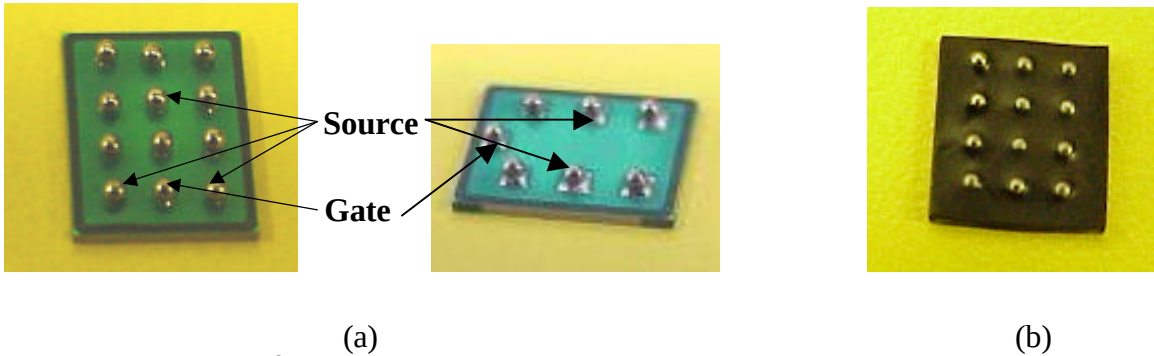


Figure 5.8. D²BGA IGBT chip-scale package (a) without and (b) with encapsulation.

Solder joint power chip interconnection also enables other wireless chip scale packages to be easily built by using the solder joints with various leadframe or connector designs. For some planary structure applications, we have designed cavity-down flip chip on flex (FCOF) chip scale package, as shown in Figure 5.9. In this structure, source and gate pads were connected to flex leadframe by solder joint with either high standoff hourglass-shaped structure or just conventional single bump structure. The inner side of the flex was etched so that gate leadframe is separated from the source leadframe. All the source pads were connected together by the flex leadframe, which is extended out from the right side. The gate leadframe is extended from the left side. The backside (drain for MOSFET and collect for IGBT) is solderable and can be directly attached to substrate. The gate and source leadframes were designed in such a way that they are coplanar backside of the device. Figure 5.10 shows a cavity-down flip chip on flex IGBT package.

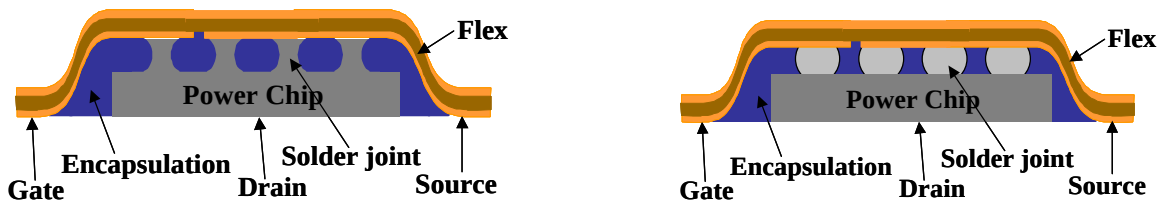


Figure 5.9. Cross section view of cavity-down flip chip on flex CSP.

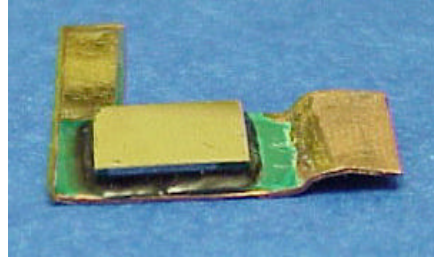


Figure 5.10. An example of cavity-down flip chip on flex CSP.

5.3 Fabrication Process

Prototypes of both D²BGA and cavity-down FCOF CSPs were fabricated. The power chip used was IXYS high speed IGBT-IXSD35N120A. The fabrication process for both D²BGA and cavity-down FCOF CSPs are similar. The core part is the solder bumping process, which has been introduced in Chapter II. In principle, before solder bump formation, under-bump metallization (UBM) need to be deposited on the aluminum pads of the power chips. However, the IGBT chips we bought from IXYS were originally solderable. So we directly form solder joint on the chip pads. The IXYS UBM is Ti/Ni/Ag.

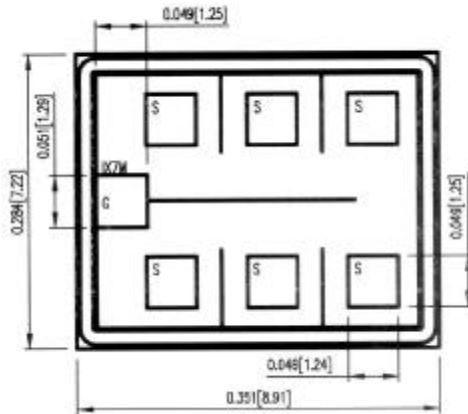


Figure 5.11. Die-map of IXSD35N120A [19]

D²BGA package fabrication has three major steps: Solder mask patterning, solder bumping and molding (this is optional, the purpose of molding is for better handling). For the solder mask patterning process, a photoimable solder mask was applied on power chips using spin coating. Photolithography allowed definition of openings in the solder mask for all the solder bump pads on power chips. Solder bumping process was described in Chapter II. For conventional single solder bump, eutectic solder was used. For stacked solder joint, the inner

solder cap is Sn96.5/Ag3.5 alloy with a melting temperature of 221°C. The middle solder ball is high-lead Sn10/Pb90 solder with a melting temperature of 268°C. In our research, the power chip pad size was 1.1 mm× 1.1 mm. According to our design of forming hourglass-shaped solder joint, 35 mil (0.9 mm) diameter solder balls were used. The height of this stacked solder bump is 40-50 mil. After solder bumping, the stacked solder bump on chip assembly is cleaned. Finally, in order to make the CSP easy to handle and robust, the chip is encapsulated by a molding compound in such a way that the surface of the package is left with an array of the high-lead solder balls.

For the cavity-down FCOF package process, the first several steps are basically same as the fabrication process of D²BGA package. After solder bumping, the devices were flip chip attached to prepared flex leadframe.

During the process, the IGBT devices were tested and characterized for their functionality and performance using low power curve tracer with probe contact. Three probes were used, one connected to collector, the other one placed on one emitter pad and another one placed on the gate pad. No emitter and collector sensors. In order to characterize packaging process influence on IGBT device, the devices were probed at the same pads for each testing after the process steps. Figure 5.12 shows the forward characteristic of a typical IGBT chip tested after the major process steps. We can see from Figure 5.12 that the forward characteristic of IGBT device is indiscernible before and after solder mask patterning process. This means that solder masking process did not degrade IGBT performance. For testing solder bumped IGBTs, the probes were placed on top of the solder bumps on the pads where the probes were placed before solder bumping. We can see that the slope of the IGBT forward curve were lower after solder bumping process. This means that the voltage drop of the IGBT were higher than that before solder bumping. This is understandable since solder bump added resistance to the IGBT from the contributions of both solder bump material resistance itself and the contact resistance between solder bump and chip pad. After the solder bumped IGBT was flip-chip attached to substrate, the slope of forward curve was lowered further slightly. For this test, probes were placed on the substrate pads that are still connected to the corresponding chip pads through solder joints. For comparison of the resistance added by solder bump and wire bond, we also tested wire bonded IGBTs. For testing wire bonded IGBTs, just like flip-chip bonded IGBTs, the probes were placed on the substrate pads that are connected to the same chip pads as solder

bumped IGBT through wire bonds. We can see from Figure 5.12 that slope of the forward curve of wire bonded IGBT is much lower than that of the flip-chip attached one. This indicates that the resistance added by wire bond is even higher. This is also a proof that the D²BGA package has lower voltage drop and on-resistance over wire bond packages.

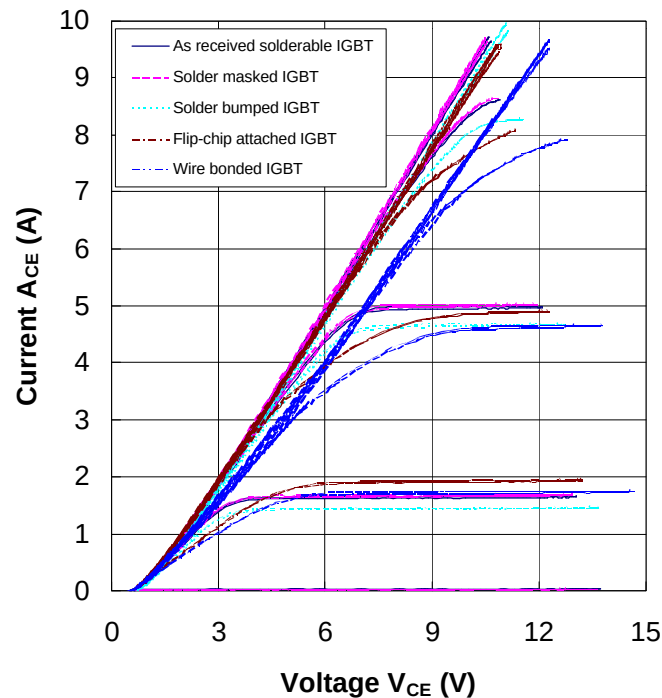


Figure 5.12. Forward characteristic of IGBT device tested by lower power curve tracer with probe contact after each major process steps and that of wire bonded IGBT.

5.4 Electrical Performance

In power electronics applications, both static and switching performances of active power devices are important. In this section, we only discuss the static performance of the IGBT CSPs since switching test is extremely difficult to be carried out at the chip scale package level and leave the switching performance evaluation in chapter VI where electrical performances of power modules made by these CSPs will be discussed.

The most important static electrical characteristics for IGBTs are: Collector-to-Emitter Breakdown Voltage (BV_{ces}); Collector-to-Emitter Saturation voltage ($V_{CE(sat)}$); Gate Threshold voltage ($V_{GE(th)}$); and Forward transconductance (g_{fs}). BV_{ces} is determined primarily by the chip itself. $V_{CE(sat)}$ is a critical parameter as it determines on-state power dissipation. A lower voltage

drop within a device means lower losses and higher efficiency. The voltage drop across the IGBT in the linear region has four components:

$$V_{CE(sat)} = V_{CE(offset)} + V_{(N-region)} + V_{(surfMOSFET)} + V_{R(packaging)}$$

Thus, the on-state voltage drop across an IGBT never goes below the offset voltage (diode threshold). The first three terms are determined by the device, while the fourth term is dependent on packaging structure. $V_{R(packaging)}$ is mainly comprised of contact resistance between emitter/collector and the interconnection medium (wirebonds or area bonds), the resistance of interconnection medium and the resistance of leads or other external connections. Traditional wire-bonds on the top (source) of the power devices have been a primary contributor to electrical and thermal losses from packaging. In essence, the wire-bonds and the top metal sheet contribute about 90% of the overall package resistance. $V_{GE(th)}$ is the range of voltage on the gate at which collector current starts to flow. Like BV_{ces} , $V_{GE(th)}$ is determined by the device itself. Transconductance g_{fs} is the amount of change in collector current by the amount of change in the gate-emitter bias voltage. If g_{fs} is large enough, high current handling capability could be gained from the low gate drive voltage and the high frequency response is possible. g_{fs} also influences the turn-on and turn-off times. The higher the g_{fs} , the higher the collector current slope. The value of g_{fs} is also related to packaging approach.

Chip-scale packaged IGBTs, commercial packaged IGBTs from vendor in the form of JEDEC TO-247 package were evaluated using static tests. For both cases, the same IGBT die was used which we bought from the same vendor. Five samples of each kind of devices were tested. SONY Tektronix 371 programmable high power curve tracer is used to conduct the static tests. The test condition is: pulse width is 250 μ s, duty cycle lower than 0.5%.

The IGBT die we used is high speed IGBT. Its I_C versus V_{CE} curve is almost linear in the active region, thus we can define the amount of change in V_{CE} by the amount of change in the collector current I_C as on-state resistance R_{on} . Figure 5.13 is the summary of the voltage drop and on-resistances of IGBT CSPs and IGBT TO-247 packages. Table 5.1 is the typical test data and Figure 5.14 show the typical saturation characteristics curves of CSP IGBT and commercial packaged IGBT. We can see that CSP IGBT has the lower voltage drop and on-state resistance, higher forward transconductance. Compared with the commercial packaged IGBT, the $V_{CE(sat)}$ and R_{on} of CSP IGBT are improved by about 20% and 30% respectively.

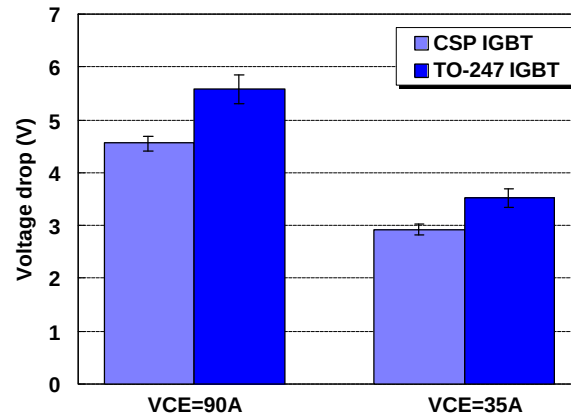
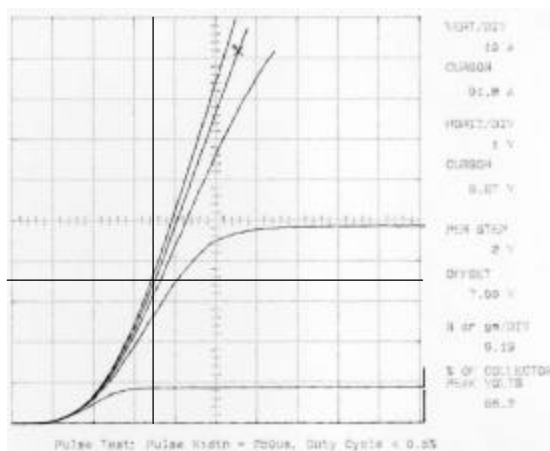


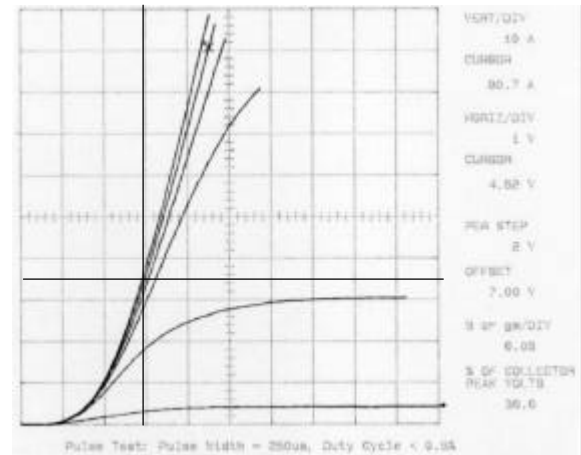
Figure 5.13. Summary of the voltage drop and on-resistance of IGBT CSP and IGBT TO-247 package.

Table 5.1. Typical static test data of IGBT CSP and IGBT TO-247 package.

	BV_{CES} (V) ($I_C \approx 2$ mA) ($V_{GE} = 0$ V)	V_{GE} (V) ($I_C \approx 2$ mA) ($V_{CE} = V_{GE}$)	$V_{CE(sat)}$ (V) ($I_C \approx 35$ A) ($V_{GE} = 15$ V)	$V_{CE(sat)}$ (V) ($I_C \approx 90$ A) ($V_{GE} = 15$ V)	R_{on} (m Ω) ($I_C \approx 90$ A) ($V_{GE} = 15$ V)	g_{fs} (S) ($I_C \approx 90$ A) ($V_{CE} \approx 10$ V)	$I_{C(on)}$ (A) ($V_{GE} = 15$) ($V_{CE} \approx 10$ V)
TO-247 IGBT (Data sheet)	>1200	6	3.1	X	X	X	170
TO-247 IGBT (test data)	>1300	6	3.5	5.6	37	30	158
CSP IGBT	>1300	6	2.9	4.5	26	34	211



(a)



(b)

Figure 5.14. Typical saturation characteristics curves of (a) Commercial packaged IGBT and (b) CSP IGBT.

Contact resistances between the interconnect bonds and power chip pads as well as interconnect bonds and substrate may have significant contribution to the total on-resistance and

thus the on-voltage drop. We measured individual resistance as well as contact resistance of in-house made wire bonds, wire bonds in commercial power modules and solder joint to chip pads and DBC substrate. We measured six bonds for each case. Our experimental tests show that wire bonds have higher electrical resistance than solder joint, as shown in Figure 5.15 (only the resistances of wire bonds in commercial power modules and solder joint are shown). The typical resistance value of wire bond itself is 2-3 m Ω , while that of the area bonds is about 0.2 m Ω . The contact resistance between bonding wire and power chip pad is significantly higher than the contact resistance between area bonds and chip pad. Figure 5.16 shows the average contact resistance of in-house made wire bond, commercial wire bond and solder joint to IGBT pads. What makes the wire bonding worse is the inconsistency of the contact resistance. In Figure 5.16, the standard deviation of the contact resistances of six bonds on IGBT pads is calculated and indicated in the figure. We can see that the contact resistance of wire bonding is widely scattered (from 9.8 to 20.3 m Ω for in-house made wire bonds and from 5.1 to 13.4 m Ω for commercial wire bonds), while that of solder joint is quite consistent. We attribute this to the fact that wire bonding is sensitive to several process parameters, while the solder bumping is a single-step reflow process, which is easily controlled. This inconsistency contact resistance causes uneven current distribution among wire bonds. The contact resistance for both the wire bonds and solder joint to the DBC substrate is quite low and consistent. Altogether, solder joint cuts down interconnect resistance by about 65% compared to commercial wire bond.

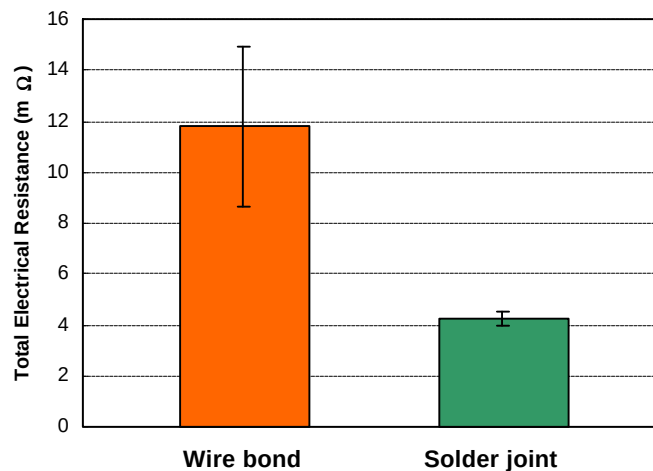


Figure 5.15. Total resistance of wire bonds and solder joints for power chip interconnection.

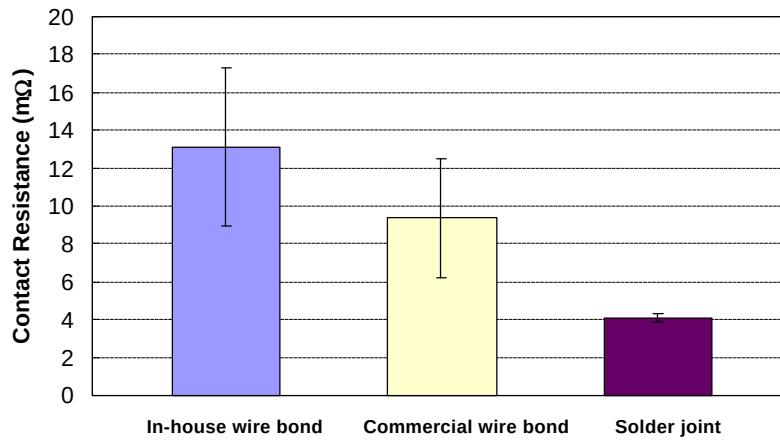


Figure 5.16. The average contact resistance of in-house made wire bond, commercial wire bond and solder joint to IGBT pads.

5.5 Reliability Evaluation

Thermal stresses in solder joints caused by CTE mismatch between top substrate and silicon are the main causes of failure in solder joint interconnections. For application, the backside of both cavity-down flip chip on flex CSP and D²BGA CSP is attached to a substrate. Thus, failure is likely to happen at two locations. One is the front chip interconnection-solder joint. The other is the back side of chip-die attach solder layer. For the die attach solder layer, fatigue failure is also caused by the CTE mismatch between the substrate and silicon. Reliability of the CSPs is evaluated by temperature cycling test. In this section, we discuss the reliability of the CSPs and wire bonded power devices.

One major failure mechanism encountered in the state-of-the-art wire-bond power devices subjected to thermal and/or power cycling is wire bond lift-off [20-26]. Bonding wires are subject to a thermal stress due to the large CTE mismatch between aluminum wires and silicon chips when there are temperature changes during thermal/power cycling. This leads to bond fatigue and eventually failure. Poor bonding, potential chip surface cracking and mechanical stress at the heel of wires [26] due to the wire bonding process are also the sources of failure. The current imbalance in bonding wires, due to the inconsistency of contact resistance, proximity effect [27-28] could cause some thermal problem, or even burn out the wire bond connection. Most of the IGBT chips of the failed modules are burned out either catastrophically

or locally [22-23]. The emitter and gate bonding wires are observed to be either fused or lifted-open, as shown in Figure 5.17.

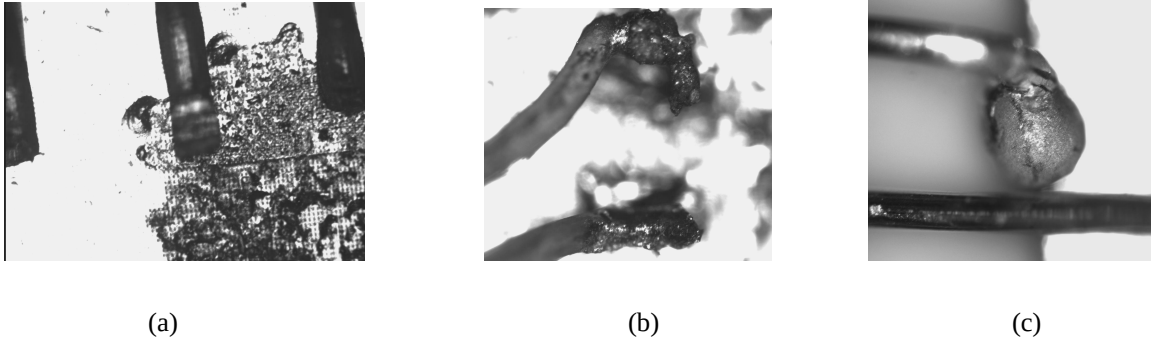


Figure 5.17. Wire bond lifted-open or fused due to current imbalance among bonding wires.

Electromigration might happen at a current density of about 10^4 A/cm² and at high temperature [22,29]. The inconsistent contact resistance, high parasitics associated with the bonding wires, and the proximity effect of the wires cause uneven current distribution among the IGBT wire bonds and cells (within one chip as well as among the paralleled chips). If the current distributes non-uniformly among the IGBT chips, or wire debonding occurs at first, then the current density in some wires will be much higher than the average value and cause severe electromigration. Besides, high temperature plays a important role in thick wire electromigration, which accelerates the migration process.

The high current in the wire bonds generates high electromagnetic field and because the wire bonds are so close to each other, strong mechanical forces are generated between wire bonds. This also affects the overall reliability of the power modules.

The CTE mismatching between silicon chip and the substrate is the most important reliability issue in solder joint assembly. The solder joint interconnection technique offers opportunities to reduce thermal stress by optimizing solder joint geometry, using compliant substrate and underfilling. Electrical modeling work also pointed out much uniform current distribution in the low-profile area array interconnects [30-31].

Numerous factors affect solder joint fatigue performance, such as chip size, chip pad size, joint geometry, interface metallurgy, underfill and substrate. Since power chip does not have many I/O, we can design large chip pad size in order to fabricate thick solder joint that can carry high current. Thick and tall solder joint offers high fatigue lifetime. In order to maximize the fatigue lifetime, we need to minimize the thermal strain. In application, a compliant substrate, an optimized solder joint geometry for device interconnection, and underfill material can reduce the

shear strain. One of the reasons of using flex substrate in the cavity-down FCOF CSP is to improve solder joint reliability by making one side of solder joint connection compliant. Solder joint geometry and shape play an important role in solder joint reliability as we have discussed in Chapter III. Furthermore, underfill can improve flip chip solder joint fatigue lifetime by several times which is proven in microelectronics packaging.

D²BGA and cavity-down FCOF CSPs with both triple stacked high standoff hourglass-shaped solder bumps and conventional barrel-shaped solder bumps as chip-level interconnection were conducted thermal cycling test. For the same interconnection structure, assemblies with both underfilled and nonunderfilled chips were tested. In order to assess the reliability of those CSPs for field application, the backside of the CSPs were soldered to an IMS (Burquist board) substrate. For the D²BGA package, actually it was first flip chip bonded to an IMS and then die attached to the bottom IMS. Thus basically, the thermal cycling test structures for both CSPs are the same, with solder bumped power chips sandwiched in between two substrates. The major difference is that for D²BGA, the top and bottom substrates were IMS, but for cavity-down FCOF, the top substrate is flex. Figure 5.18 illustrates the test configurations of the CSPs. The thermal cycling temperature range was 0°C to 100°C with the rate of 2 cycles/hour.

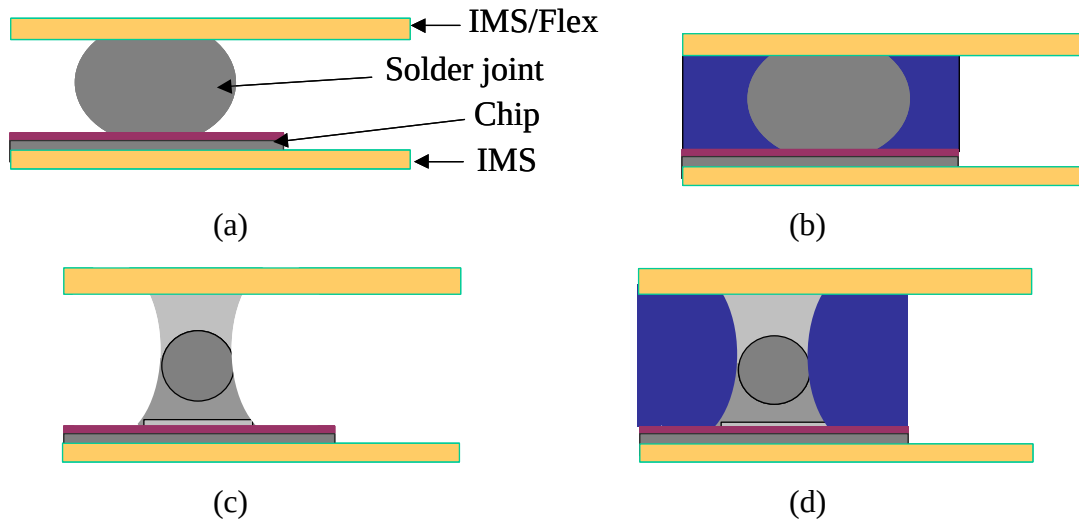
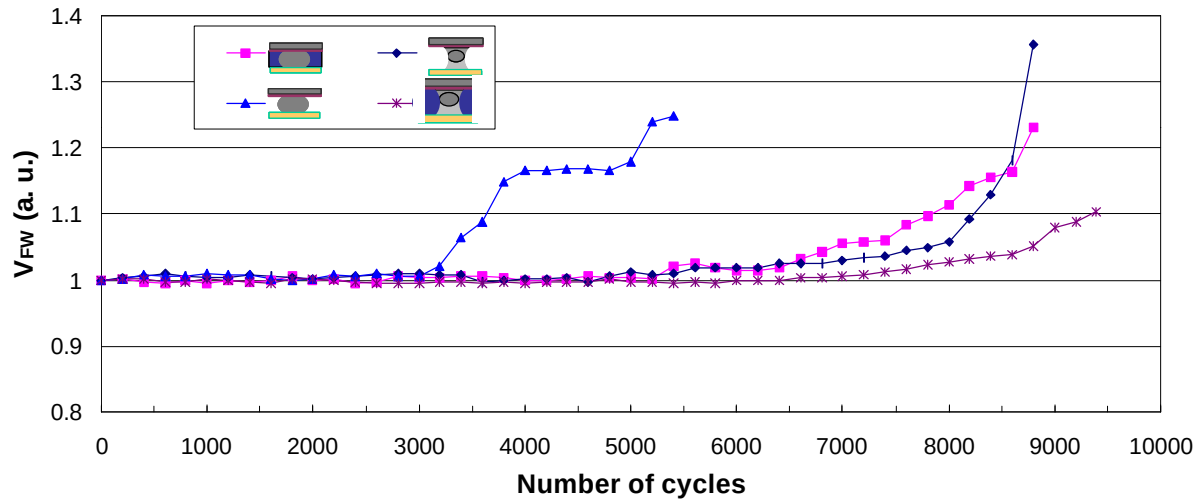


Figure 5.18. Thermal cycling test configurations of CSPs: (a) barrel-shaped; (a) barrel-shaped and underfilled; (c) high standoff hourglass-shaped; and (d) high standoff hourglass-shaped and underfilled solder joint interconnections.

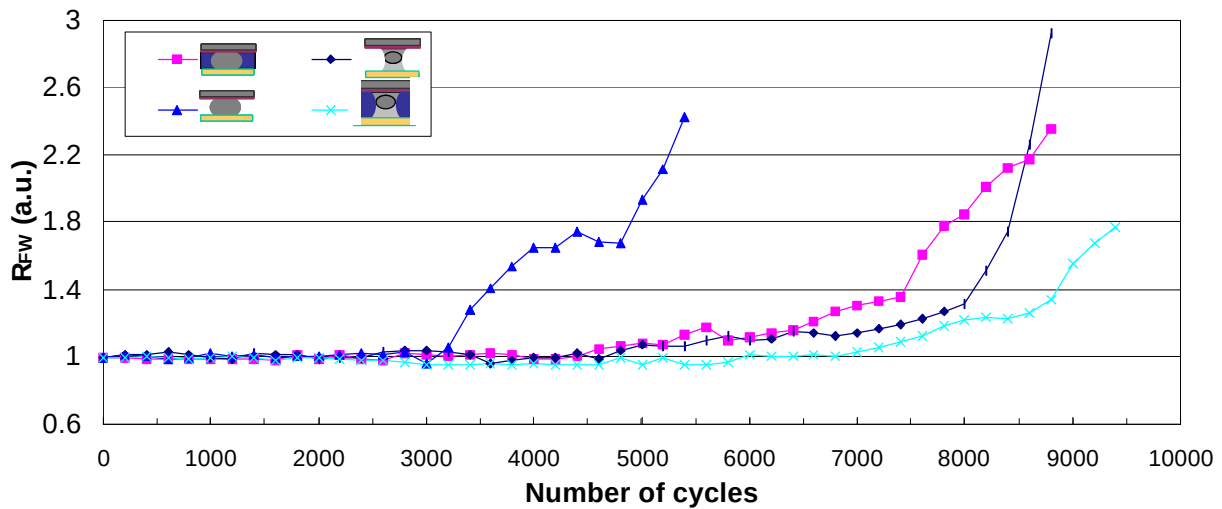
The changes of collector emitter voltage drop ($V_{CE(sat)}$) of IGBT devices and/or forward voltage (V_F) of diodes, noted as V_{FW} , as well as the slope of the forward characteristics (dV/dI),

noted as R_{FW} , were used as the evaluation criteria. When V_{FW} and R_{FW} increase 20%, we regard the test samples fail. After every 200 thermal cycles, the test assemblies were systematically tested. When there are cracks in the solder bump, V_{FW} and R_{FW} will increase. Figure 5.19 shows the typical V_{FW} and R_{FW} changes for the four different configurations of D²BGA CSP as a function of the number of cycles. The values of the forward voltage for different CSP configuration were normalized for comparison purposes. Three sets of samples were tested. Figure 5.20 summarizes the average fatigue lifetime of four different configurations of CSPs using V_{FW} and R_{FW} as criteria. The error bars in the figures are standard deviations of fatigue lifetimes of three samples. From both Figure 5.19 and Figure 5.20, we can see that fatigue lifetimes of all the configurations obtained from V_{FW} criterion are significantly different from those obtained from R_{FW} criterion, with R_{FW} criterion being more sensitive. This can be easily understood when we consider that there is an offset of IGBT (or diode) forward characteristics, as shown in Figure 5.14. However, in both cases, we can clearly see that those CSPs with high standoff hourglass-shaped solder joints have higher fatigue life than those with barrel-shaped solder joints, which is in consistent with the experimental results we discussed in Chapter 3. Figure 5.21 shows the cross section pictures of some typical failed solder joints. For barrel-shaped solder joints, failure occurred at the interface between the solder bump and the silicon chip and/or the interface between solder bump and substrate. We can see that the crack location of the hourglass-shaped solder joints could be inside the stacked solder joint, which is different from that of the barrel-shaped solder bump. However, majority of the high standoff solder joints still fail at the interface corners. Furthermore, underfill improved the reliability of both barrel and hourglass solder joints, but it seems underfill is more effective for barrel-shaped solder joint, which is very different from the results we got in Chapter 3. For the CSPs with barrel-shaped solder joints, lifetime was doubled by using underfill. For CSPs with high standoff hourglass-shaped solder joints, fatigue life is increased by less than 10% if there is any improvement from underfilling. Note that as we introduced before, there are two locations that could fail under temperature cycling, one is the front solder joints, the other is die attach layer. We can see from the SAM images in Figure 5.22 and cross-section pictures in Figure 5.23 that there is obvious cracking in die attach solder layer for both CSP test samples with high standoff hourglass-shaped non-underfilled and underfilled solder joints at 8600 temperature cycles or earlier. This explains why underfill did not improve the reliability of high standoff hourglass-shaped solder joint

significantly as it is supposed to. In the other words, high standoff hourglass-shaped solder joint is reliable enough that die attachment becomes the limit of the reliability of those CSP test samples. For barrel-shaped solder joint, its fatigue lifetime is much lower than the fatigue lifetime of die attach solder layer, thus underfill can improve the lifetime significantly.

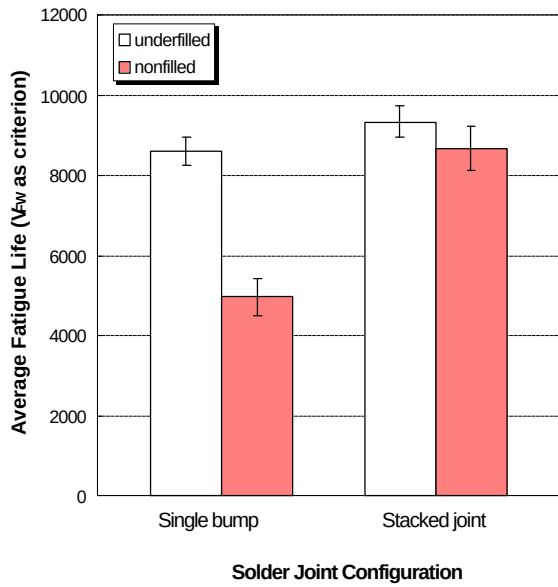


(a)

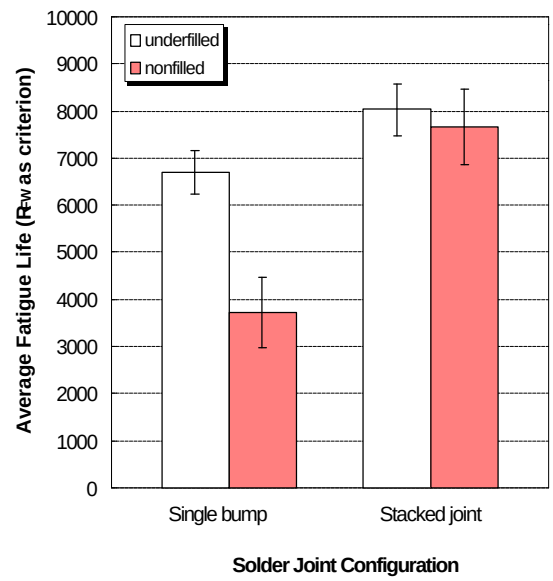


(b)

Figure 5.19. Typical (a) forward voltage and (b) resistance changes of CSP assemblies versus number of thermal cycles.

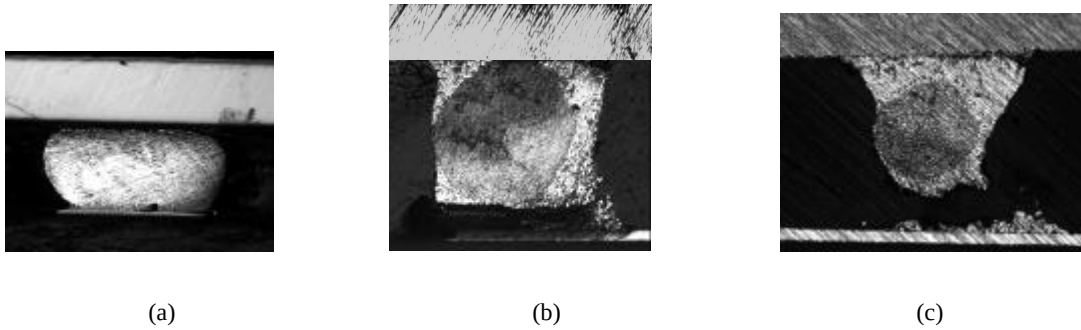


(a)



(b)

Figure 5.20. Comparison of average fatigue lifetime of four different configurations of CSPs; (a) using V_{FW} as criterion; (b) using R_{FW} as criterion.

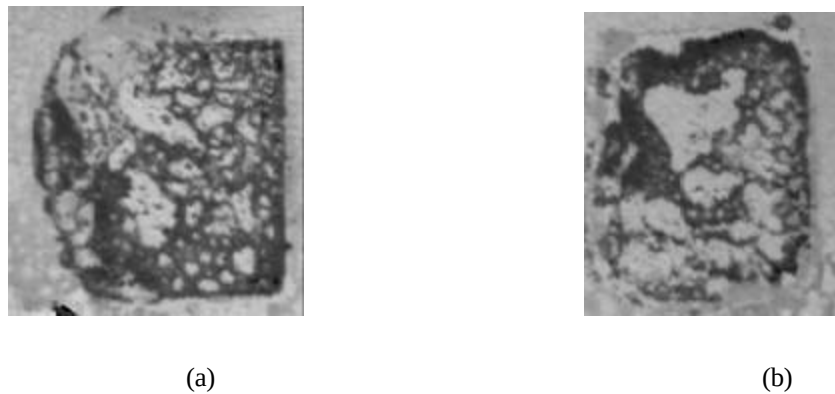


(a)

(b)

(c)

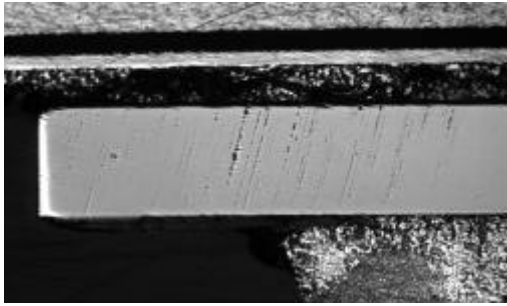
Figure 5.21. Cross section pictures of failed solder joints (a) barrel-shaped (b) and (c) hourglass/column-shaped.



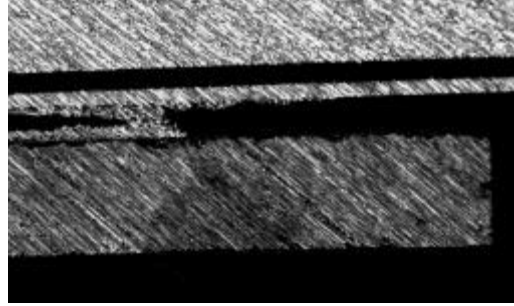
(a)

(b)

Figure 5.22. C-SAM images of CSP test samples with high standoff hourglass-shaped (a) non-underfilled; (b) underfilled solder joints after 8600 temperature cycles.



(a)



(b)

Figure 5.23. Microphotographs of die attach layers of CSP test samples with high standoff hourglass-shaped (a) non-underfilled; (b) underfilled solder joints after fatigue failure.

5.6 Applications

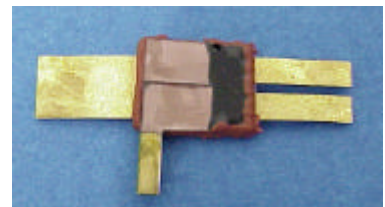
The chip scale packages could be used individually as discrete components in electronic systems where the conventional wire bonded, lead frame packages are being used. These CSPs not only offer superior electrical performance, improved thermal management, but also occupy much less board real estate. Also the CSPs can be put together to build some basic units for electronic applications. For example, an IGBT CSP and a diode CSP can be connected either in series or in parallel to form a basic unit for the most commonly used half-bridge circuit, as shown in Figure 5.24.



(a)



(b)



(c)

Figure 5.24. A basic unit for half-bridge circuit (c) can be built by an IGBT CSP and a diode CSP (a) attached to a substrate (b).

Integrated power electronics modules (IPEMs) are envisioned to have high levels of integration of power semiconductor devices, gate drive, and control circuitry for a wide range of power electronics applications. IPEMs can also be easily built using the CSPs which we will introduce in details in Chapter VI.

5.7 Summary

New single power chip packages, which are essentially chip scale packages, have been developed by using solder joint as the chip-level interconnection. The compact packages make high-density packaging and module miniature possible. By eliminating the wire-bonds and the leadframe, the IGBT chip-scale packages offer nearly a 20% and 30% improvement in voltage drop and on-resistance over a TO-247 IGBT package, respectively. These CSPs not only provide the essential elements of the IPEM in surface mount packages, offer an opportunity for getting rid of the wire bonds that can be the bane of power electronics module performance and reliability, but also allows for a relatively low cost know good die system. The stacked solder bumps are thick and they occupy a large portion of the power chip area. They help extract heat from the devices. The combinations of lower voltage drop/on-resistance and superior heat-transfer characteristics at higher power levels make the CSPs attractive for designing higher-efficiency electronic systems.

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