NOVEL MULTILEVEL CONVERTER FOR VARIABLE SPEED MEDIUM VOLTAGE SWITCHED RELUCTANCE MOTOR DRIVES

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Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

In

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February 14, 2017

Blacksburg, VA

Keywords: Switched reluctance motor, power converter, variable speed drives, multilevel converter, multi-megawatt applications, single-pulse control, brushless dc motor

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ABSTRACT

A novel multilevel converter that is especially suited for high speed multi-megawatt switched reluctance motor drives operating at the medium voltage level is presented. The drive is capable of variable speed, four-quadrant operation. Each phase leg of the converter contains an arbitrary number of cascaded cells connected in series with the phase winding. Each cell contains a half-bridge chopper connected to a capacitor. The converter is named the cascaded chopper cell converter. The modular nature of the converter with the ability to add redundant cells makes it very reliable, which is a key requirement for medium voltage drive applications. A comprehensive control algorithm that overcomes the challenges of balancing and controlling cell capacitor voltages is also proposed. A suitable startup algorithm to limit startup current and switching losses, as well as ensure that cell capacitor voltages remain controlled at startup, is suggested. Details of the drive design such as component sizing and control parameter selection are also discussed. A detailed simulation model is developed and explained, and simulation results are provided for primary validation. Operation with standard current and speed control is first simulated. Then a scheme that gives way to a controller that operates the drive in single-pulse mode is developed and presented. This single-pulse control scheme controls the turn-on and turn-off angles, as well as the energization voltage level, in order to obtain high efficiency. Practical considerations related to the drive such as reliability, efficiency, and cost considerations are also discussed. Finally, a detailed comparison of the proposed converter with another competing converter is performed. Besides its scalability to high voltages and powers, the reliability and efficiency of the proposed converter makes it also a candidate for sub-megawatt applications requiring minimum downtime, or any application where high efficiency or improved performance is required.

A small part of this work is also dedicated to brushless dc machines. Control methods for a new converter for brushless dc machines are proposed and verified via simulation. The main advantage of this converter with the proposed control is that it allows exact control of torque or speed up to twice the rated speed, without resorting to current phase advancing or other flux-weakening techniques.

NOVEL MULTILEVEL CONVERTER FOR VARIABLE SPEED MEDIUM VOLTAGE SWITCHED RELUCTANCE MOTOR DRIVES

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GENERAL AUDIENCE ABSTRACT

Electric motors are used in a very wide range of applications. They are found in power tools, in household appliances like washers and dryers, in compressors for HVAC, in fans, blowers and pumps in industry, and in electric vehicles and electric transit systems, only to name a few. An electric motor that is combined with an electronic circuit that allows precise control of the motor speed and torque is referred to as an electric drive. Very large electric drives – reaching multi-megawatt powers – are used in several applications such as in ship propulsion, in large pumps for moving water and sewage, and others. Very few electric motor drive options currently exist at that power level, and so multi-megawatt electric motor drives present an interesting research opportunity.

This work proposes a novel drive system that is best suited for high speed multi-megawatt electric drives employing the switched reluctance motor. The switched reluctance motor was chosen due to its robustness, high efficiency, and high speed capability. A novel electronic converter that is scalable to high power and voltage levels is proposed. It features high reliability which is essential in multi-megawatt applications that typically require very high uptime. It has a modular structure, thereby allowing for simple construction. A comprehensive control algorithm for the drive system consisting of the converter and motor is proposed. Also a suitable algorithm that keeps the electrical and thermal variables within the allowed limits during the startup stage is proposed. A detailed simulation model is developed and explained, and simulation results are provided for primary validation. Next, a control scheme that results in high efficiency through appropriate control of the drive's various parameters is proposed. Practical considerations related to the drive such as reliability, efficiency, and cost considerations are also discussed. Finally, a detailed comparison of the proposed converter with another competing converter is performed. Besides its scalability to high voltages and powers, the reliability and efficiency of the proposed converter makes it also a candidate for sub-megawatt applications requiring minimum downtime, or any application where high efficiency or improved performance is required.

A small part of this work is also dedicated to drives using another type of machine called the brushless dc motor. Control methods for a new converter for brushless dc machines are proposed and verified via simulation. The main advantage of this converter with the proposed control is that it allows exact control of torque or speed up to twice the rated speed, which makes it useful in traction applications.

ACKNOWLEDGEMENTS

All praise and thanks be to God Almighty for enabling me to carry out this work, and to have given me the opportunity to contribute to the enhancement of knowledge for the betterment of humanity. I thank Him for giving me the health, means, and the support of those around me in order to accomplish this task.

Most sincere gratitude and appreciation go to my advisor, Professor Krishnan Ramu. He extended to me moral and technical support to very far lengths that left me unable to express enough thanks. His kindness, concern, encouragement, and mentorship were key in allowing me to reach to this stage. To his students, he and his wife, Ms. Vijaya, are like parents in absentia.

I would also like to thank my committee members, Dr. Daniel J. Stilwell, Dr. William T. Baumann, Dr. Kathleen Meehan, and Dr. Alexander Leonessa for making themselves available, and for their direction and suggestions.

Last but not least, heartfelt thanks go to my parents, my parents-in-law, my siblings, and my loving and supporting wife, Afaf. Without their support, prayers, and encouragement it would simply not have been possible for me to undertake this endeavor.

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Chapter 1

Introduction

1.1 Motivation

Electric motors and the loads they drive account for 43-46% of all global electricity consumption. This is more than twice the consumption by lighting, the next largest end-use of electricity [1, pp. 11]. In the United States, electric motor energy consumption represents more than 50% of the total energy consumption [2]. A very large percentage of this consumption occurs in industrial fans, pumps, conveyers, and compressors in industries like chemicals, food, petroleum and coal products, primary metals, and paper [3]. Traditionally, electric motors were operated at a fixed speed. When a process required lower speeds, dampers or throttling valves were used to control fan air-flow or pump liquid-flow, respectively. While this satisfied the requirements of the process, it also wasted a large amount of energy. Then emerged variable speed drives (VSDs), aided by advancements in the fields of power semiconductor devices and digital control. VSDs are electronic devices that, when connected to a motor, can almost precisely control the amount of torque it generates as well as its operating speed. So rather than generating power then redirecting the unwanted portion, VSDs better matched the motor speed and torque to the mechanical load's requirements.

Fans and centrifugal pumps are examples where significant savings in energy can be achieved through the use of VSDs. Torque in fans and centrifugal pumps is proportional to the square of speed, and power is proportional to the cube of the speed. This means that if a process requires only half the speed, then the power needed to run that fan or pump with a VSD is only one eighth of the power needed to run it at full speed. On the other hand, with traditional damper/valve control, the motor is operated at full power in all cases. VSDs present only one example of efficient energy usage in electric motor drives. It is reported that if all efficiency improvement options were fully implemented in electric motor drive systems, the worldwide electricity demand could be reduced by as much as 7% [4, pp. 2]. Another important fact to consider is that motor energy costs represent over 90% of a motor's life-cycle cost [1, pp. 12, 2], and so even though initial buying cost of VSDs is more than that of traditional drives, the increased investment is more than made up for in the form of energy savings. Given the widespread use of electric motor drives and their critical impact on the global energy situation, work in this field has been undertaken with the goal of making a useful contribution.

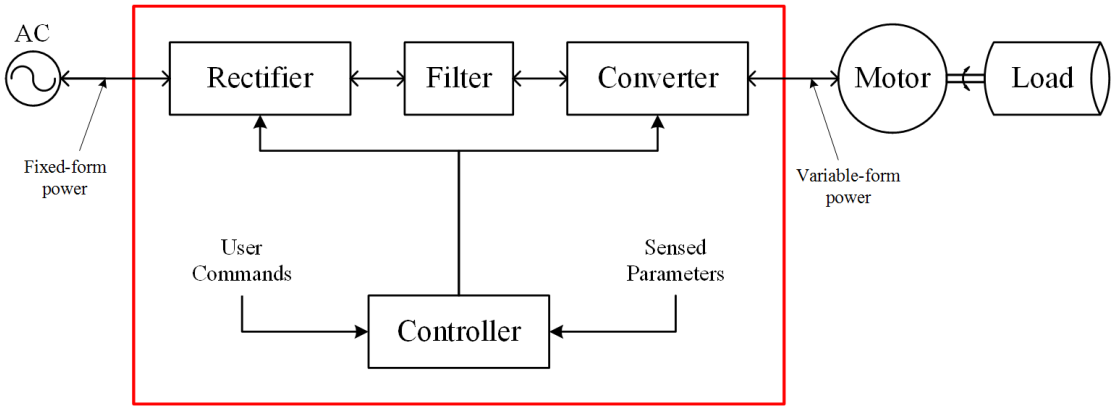


Fig. 1.1 Major components of a variable-speed electric motor drive

1.2 Background Information on Electric Motor Drives

The focus of this work is on VSDs, and so it is important to start by defining a VSD and describing its major components.

1.2.1 Variable-speed Electric Motor Drives

In a few words, a VSD converts ac power that has voltage of fixed-amplitude and fixed-frequency into an adjustable form of power that has voltage with variable-amplitude and variable-frequency. A simplified diagram of a modern, variable-speed, electric motor drive is shown in Fig. 1.1. Strictly speaking, the drive includes only the components enclosed in the red box, and not the machine or load. However, the term "motor drive" is also loosely used to refer to the system including the machine as well. Only the major components of the drive are shown in Fig. 1.1. Other components not shown include sensors, which are situated at almost every stage in the drive system. Also omitted from the figure are auxiliary systems, such as cooling systems in case of large drives. The supply is always in the from ac power, being the only available form of power from the power network or from any standalone generator – except in very small drives that are battery operated. Following is a description of the major components of an electric drive:

- *Rectifier*: The rectifier converts the ac power to dc. It is usually referred to as the front-end converter since it is what faces the supplying source. A rectifier is either made of a diode bridge or of fully-controlled switches such as MOSFETs or insulated-gate bipolar transistor (IGBTs); in the latter case it is called an active front-end or active rectifier. While the diode bridge is less expensive, it does not allow reverse current flow back to the source, and hence does not allow power to flow from the motor-end to the source. This feature is useful in drives where appreciable power may be recovered, such as elevators where gravitational energy in the downward trip can be sent back to the electric supply. Active front-ends on the other hand do support recovery of energy by allowing current to flow in the opposite direction, i.e., back to the source, in a process known as regeneration.

Other advantages of active front-end rectifiers are that they present a better power factor to the supplying source, which amounts to more efficient use of power from the network, and also reduced injection of harmonic distortion into the supplying network compared to a diode front-end rectifier.

- *Filter*: The filter section, also referred to as dc link, is made of a capacitor or inductor, or a combination of the two. When the filter or dc link is a capacitor, it presents a constant voltage source to the converter stage that follows it. Such converter is then called a voltage-source converter. If the dc link is an inductor, the converter is presented with a constant current source rather than a constant voltage source, and is hence called a current-source converter.

- *Converter*: This is the heart of an electric motor drive. Its function is to convert the dc voltage or current to ac voltage or current but with a variable average value and a variable frequency. In other words, it customizes the voltage and current waveforms according to the needs of the motor and its load. This gives great flexibility in terms of operating the motor drive at the desired speed and torque, which is the whole point of an electronic variable speed drive. Since the dominant form of variable-speed drives are the ac drives, this stage is also commonly called inverter, as it inverts dc back to ac. The term "converter" is adopted in this text, being more general, since not all variable-speed motor drives require ac power – though still they require variable amplitude and variable frequency.

- *Controller*: Controllers today mostly take the form of digital processors or field-programmable gate arrays (FPGAs). They take in the user commands as well as the sensed parameters. Their main function is to send control signals to the converter in order to synthesize the appropriate voltage or current required by the motor. When the rectifier is of the active type, the controller also sends control signals to it in order to control the dc link voltage and/or current, as well as improve power factor and harmonic distortion at the point of connection with the supply side. Controllers also perform protection functions by acting upon fault signals, as well as other functions.

1.2.2 Machines for Industrial Electric Motor Drives

Aside from the converter, at the core of every electric motor drive system is the electric machine used. The early age of industrial motor drives was dominated by dc motors, which were all but replaced in the 80's and 90's by ac motor drives using induction machines [5]. Compared to dc drives, ac motor drive systems were maintenance free, offered better performance, and were of smaller size and weight [5]. Induction ac machines are also known as asynchronous ac machines, since the rotor speed is different from that of the rotating magnetic field. But synchronous ac motors also played in a role in replacing dc motors, especially at higher powers. In fact, today's largest machines operating at tens of megawatts are most dominantly ac synchronous machines.

In the meantime, major advancements had been taking place in the field of permanent magnetic materials [6, 7], and soon enough brushless permanent magnet (PM) and PM AC synchronous motors appeared in the market. They featured better efficiencies and higher power densities compared to induction motors, but were also more expensive. Another contender, the switched reluctance motor (SRM), had also been slowly emerging in the market. Though the machine had been invented in the first half of the 19th century [8, 9], it was not until suitable power electronic switches became available that they developed into capable drive systems. SRMs feature simple brushless construction with no magnets or windings on the rotor, making it cost less to build and very reliable in operation. And unlike AC drives, it only requires unipolar current, which results in a simple power converter circuit. Penetration of the SRM in the industrial sector is still somewhat limited, mainly due to hesitance in adopting newer technologies, as that involves added cost for the manufacturer in terms of installing new manufacturing lines as well as training personnel on the new technology [8, ch. 9]. Other motor types aside from those three also exist but are less commonly used, and by far the most common industrial machine nowadays is the ac induction motor.

This work touches upon two of the major contributing drives in today's market, namely SRM drives and PM motor drives. Majority of the work is related to the SRM, but a small portion is also dedicated to the PM brushless dc motor (BLDCM).

1.3 Area of Focus

Electric motor drives exist at power levels ranging from as little as a few Watts, e.g. in electric tools, going through several hundred Watts in applications like AC compressors, washers and dryers, etc., and all the way to up to many megawatts in industries like oil and gas, marine applications, etc. Multi-megawatt drives present an interesting opportunity for research in the field electric motor drives, and have been chosen as the focus of this research. Very few electric motor drive options currently exist at that power level. One of the reasons is the slow-changing nature of the multi-megawatt drive market, due to the very high initial capital investment leading to hesitance in adapting new technologies. Of the major multi-megawatt applications of electric motor drives are compressors in natural gas production and transmission, whose sizes range from a few megawatts up to 50 MW and more [10]-[18]. Traditionally, mechanical prime movers, like gas or steam turbines, or diesel engines, have been used to drive large compressors. However, these have low efficiencies since they rely on the customary throttling valves or recirculation systems for control, rather than matching the pressure/flow to the process requirement as with VSDs. Also environmental concerns have led governments to impose regulations that limit the emission of harmful gases, like those produced by the aforementioned mechanical drives. These factors and others have contributed to the increasing adoption of electric drives in the oil and gas industry in the last 20 years.

As electric drives started to make appearance in high-power applications like the oil and gas compressors and very large fans and blowers, the ac synchronous and induction motors were some of the choices for motors. While synchronous motors are slightly more efficient [13], induction motors are capable of running at higher speeds. Also induction motors do not require field excitation (as with synchronous motors), and so they are easier to build and operate. The SRM on the other hand can provide a wider speed range than both induction and synchronous motors, has a simpler construction than both, and is inherently tolerant to short-circuit faults. It was also shown in a study comparing efficiencies of a 2-MW SRM drive and a 2-MW cage induction motor drive that the SRM was slightly more efficient due to lower rotor losses [14].

1.4 Problem Statement and Contributions

The goal of this research is to develop a converter, along with its controls, for an SRM drive that is suitable for operation at the multi-megawatt level. In order to offer drives at such high powers as required by some of today's gas pipeline compressors, it is almost unavoidable to operate at the medium voltage level, which may be defined as 1 kV to 30 kV. This is because operating at high voltage levels generally results in better efficiencies when compared to drives with lower voltage but higher current ratings. Characteristics sought in this drive are thus:

- **Scalability**: The converter should theoretically be able to operate at any voltage level.
- **Reliability**: Multi-megawatt applications are usually critical ones, and downtime cost is very high. Therefore, reliability is an essential requirement of the proposed converter.
- **Redundancy**: This is basically one of the reliability features, but is singled out for its importance as it allows for continued operation in case of minor faults. On top of redundancy, the ability to replace the faulted redundant components without the need for downtime would be a major plus as it would contribute to even higher uptime. Without this additional feature, if successive faults were to occur before a scheduled maintenance – when faulted components are replaced – the consequences would be undesirable.

Two more features, whose significance will become more apparent after the review of converters in the next chapter, are listed here for completeness.

- **Modularity**: The converter must be constructed from small building blocks or modules, which should make scalability easier, and also make manufacturing simpler. Modularity is also a way of providing more possibilities for incorporating redundancy.

- **Multilevel capability**: This will be further explained in the next chapter, but in essence drives that utilize the multilevel technology typically have higher efficiencies, especially at higher voltages. Multilevel converters also have better in several other categories, which will explained in due course in the next chapter.

Contributions from this research include:

- Development of a novel converter topology for medium-voltage variable-speed SRM drives, satisfying the requirements mentioned above.
- Development of a complete control scheme for the proposed drive, with the cell capacitor voltage balancing and control being novel.
- Development of a startup algorithm, not requiring any extra devices, that allows the proposed drive to go through the startup phase without a large increase in the cell capacitor voltages, which avoids oversizing the capacitors. The startup algorithm also limits the switching losses, which makes the startup process thermally safe.
- Verification of all of the above through simulations via a detailed switching-based model.
- Development of an algorithm for operating the drive in an efficient single-pulse mode throughout the speed range.
- Suggested simulation approach for the evaluation of various losses in the above single-pulse mode throughout the speed range.
- Development of control methods for a new converter for BLDCM drives, and their verification via simulation.

1.4 Organization of the Dissertation

Chapter 2 provides background information on the SRM to provide the reader with the fundamentals necessary to understand the work done. It covers the SRM principle of operation, its electromagnetic characteristics, its basic control, and definitions of SRM-related terminology used in dissertation. The chapter also provides a review of the major high-power multilevel converters used in ac drives and their adaptations to SRM, to set the context for the development of the proposed converter. Other multilevel SRM converters that are not based on the ac multilevel converters are also reviewed for completeness.

Chapter 3 describes the newly proposed converter and explains its principle of operation. Initialization of the converter through charging the cell capacitors is explained. Pros and cons of the drive apparent up to that point are also discussed.

Chapter 4 explains the control of the proposed converter, with focus on cell capacitor voltage balancing and control, as well as startup control. A detailed description of the simulation model used is then provided, followed by simulations results for several different operating points and other variations.

Chapter 5 describes an algorithm for achieving single-pulse operation throughout the speed range of the drive by taking advantage of the proposed converter's multilevel voltage capability. A simulation approach is used to evaluate the drive's efficiency using this scheme at several operating points through the speed range.

Chapter 6 discusses practical considerations for the drive, such as reliability, efficiency, and cost, and also sheds light on the effects of scaling the converter on efficiency and cost. The chapter also suggests suitable front-end converter options. Finally, the chapter provides a detailed comparison with a competing high-voltage SRM converter reported in earlier literature.

Chapter 7 proposes control methods for a previously published converter that is targeted to brushless DC motor (BLDCM) drives. The proposed control methods aim to extract some of the advantages of this topology in order to overcome some of the shortcomings of standard BLDCM drives at speeds above rated. Simulation results are provided for validation and comparison with the standard BLDCM drive.

Chapter 8 provides a summary of the work done and includes some suggestions about directions for related future research work.

Chapter 2

SRM Fundamentals and a Review of Multilevel Converters for SRM Drives

2.1 Introduction

The goal of this chapter is to provide the reader with the necessary background on the SRM to enable better understanding of the requirements of the converter part of an SRM drive. Also a review of relevant converters in literature is provided to better appreciate the motivation for this work, which is to develop a new SRM converter for medium-voltage multi-megawatt applications. Section 2.2 describes the basic features of an SRM, its principle of operation, its basic control, and its advantages and disadvantages compared to other machines. The standard asymmetric bridge SRM converter is also introduced to aid in the explanation of electronic control of an SRM. Section 2.3 provides the review of high-power SRM converters, with stress on those using the multilevel approach. Some of the ac multilevel converters are reviewed in the process, since the multilevel approach started with ac drives. Other high-power converters for SRM, not necessarily based on ac multilevel drives, are also reviewed for completeness.

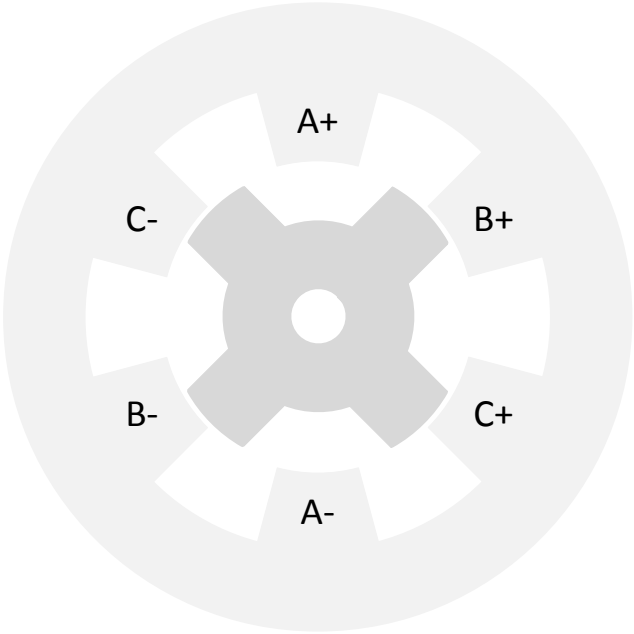


Fig. 2.1 Cross-section of a 6/4 SRM

2.2 SRM Features, Control, Operation, and Evaluation

The SRM comes in both rotary as well as linear versions. Since the focus of this work is to develop a converter for a rotary SRM, only rotary SRMs are considered in this review. Also only those with a radial magnetic field are considered – as opposed to axial-flux SRMs where the field is along the length of the machine or shaft.

2.2.1 Features of the SRM

The SRM is a doubly salient machine, meaning that both the stator and rotor poles are protruding, as shown in the example SRM configuration in Fig. 2.1. The windings are concentrated around the stator poles, with no overlap between phases; the windings are hence not distributed in slots along the perimeter of the machine as in ac machines. The coils of diametrically opposite stator poles are typically connected in series to form one phase winding. The rotor of an SRM has no windings or permanent magnets. Due to the double saliency of the SRM and the use of concentrated windings, the air gap seen by the electromagnetic flux produced by the phase windings varies based on the position of the rotor. When a phase winding is excited with current, the rotor aligns its poles with that phase in order to provide a minimum reluctance path to the electromagnetic flux produced by that phase's winding. By energizing and de-energizing the stator phase windings in sequence, the rotor is forced to rotate. This form of torque resulting from the tendency of the rotating part to align itself in the positon where reluctance to flux is minimum is known as reluctance torque.

Based on the features above, the following may be said of the SRM:

- Since the rotor does not carry current, rotor copper losses are eliminated. This is an advantage compared to motors like the induction and synchronous motors that have conducting rotors or rotor windings, as it enhances efficiency and simplifies rotor cooling requirements.

- Since the rotor does not have permanent magnets, rotor construction is simpler, making manufacturing cost potentially lower. Also the absence of attached magnets on the rotor makes for a more robust construction and avoids other related problems like demagnetization of the magnets. This is one of the reasons SRMs are capable of very high speeds.

- The fact that the SRM relies on single excitation (i.e. from stator windings only and not the rotor), along with the effects of fringing fields and magnetic saturation, makes its magnetic characteristics highly non-linear [19]. Derivation of a good analytic model is hence not possible, and control design requires measurements or finite element simulation of the SRM's electromagnetic characteristics.

- The reliance of the SRM on reluctance torque makes it insensitive to the direction of current in the windings. Therefore, it may be operated with unidirectional current only. This enables building converters with fewer components compared to ac drives, which results in reduced converter cost as well as increased reliability due to lower component count.

2.2.2 SRM Configuration and Terminology

SRM configurations are referred to by the number of poles on the stator and rotor. For example, the configuration in Fig. 2.1 with six stator poles and four rotor poles is referred to as a 6/4 SRM. As earlier mentioned, every pair of diametrically opposite stator poles have their windings connected in series. Therefore, with six rotor poles, there are three sets of windings or in other words three electrical phases. Very little mutual inductance exists between phases since there is no overlap between windings of different phases.

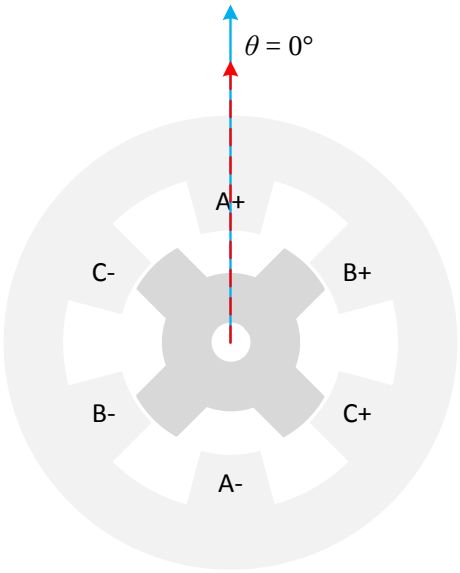
Consider the 6/4 SRM view in Fig. 2.2 (a). Since there are four rotor poles, the position of the rotor with respect to the stator repeats after every 90° of mechanical rotation. Also note that the relative stator/rotor positions are always different for each phase, and so position is always defined with respect to a given phase. Assume that the solid blue axis is attached to the stator at the position shown, i.e., at the center of the phase A stator poles. Also assume that the dashed red axis is attached to the rotor and hence rotates with it. With this stationary solid blue axis as reference, the various positions of the rotor may be defined. Let θ_a be the position of the moving dashed red axis to with respect to the stationary solid blue axis. Similarly, θ_b and θ_c may be defined for the other phases with the appropriate set of axes for each. But since the electrical and electromagnetic response of all phases is identical, albeit with a shift in time, it suffices to consider one phase only for purposes of explanation and control design. Therefore in this chapter and subsequent chapters, θ_{ph} or just θ may be used to denote rotor position with respect to a given phase.

- *Unaligned Position*: When rotor poles are farthest from alignment with the stator poles of a given phase, the SRM is said to be in the unaligned position for that phase. At this position reluctance to electromagnetic flux generated from that phase is at its maximum, due to the air gap being largest. Phase inductance, L_{ph} (or L for short), at this position is at its minimum. This position is illustrated in Fig. 2.2 (a) for phase A. From here onward this position will also be referred to as $\theta_{unalign}$ or θ = 0°; the inductance at that position will be denoted as L_{min}. The θ = 90° position is equivalent to the θ = 0° position.

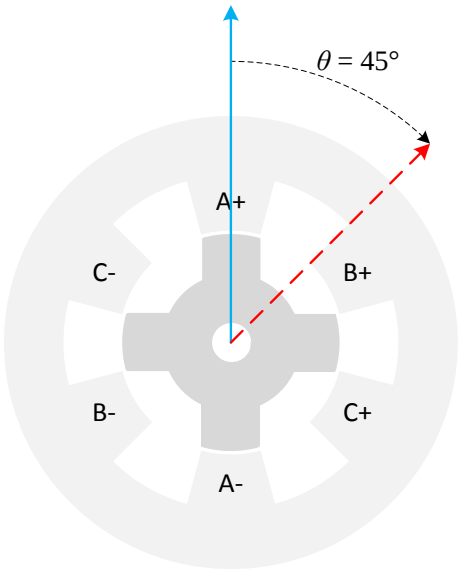
- *Aligned Position*: When rotor poles are completely aligned with the stator poles of a given phase, the SRM is said to be in the aligned position for that phase. At this position reluctance to electromagnetic flux generated from that phase is at its minimum, due to the air gap being smallest. L_{ph} at this position is at its maximum. This position is illustrated in Fig. 2.2 (b) for phase A. From

here onward this position will also be referred to as θ_{align} or $\theta = 45°$; the inductance at that position will be denoted as L_{max}.

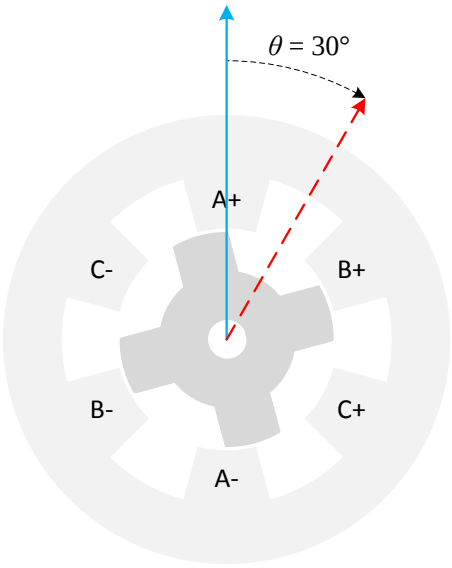
- *Misaligned Positions*: Any position besides the aligned and unaligned positions are referred to as misaligned positions [20]. Two examples of misaligned positions for phase A are shown in Fig. 2.2 (c) and Fig. 2.2 (d).



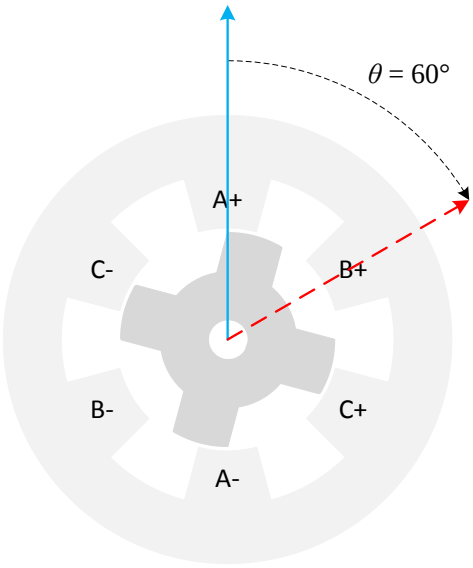
(a) Phase A in unaligned position at $\theta = 0°$



(b) Phase A in aligned position at $\theta = 45°$



(c) Phase A in misaligned position at $\theta = 30°$



(d) Phase A in misaligned position at $\theta = 60°$

Fig. 2.2 Examples of rotor positions in a 6/4 SRM

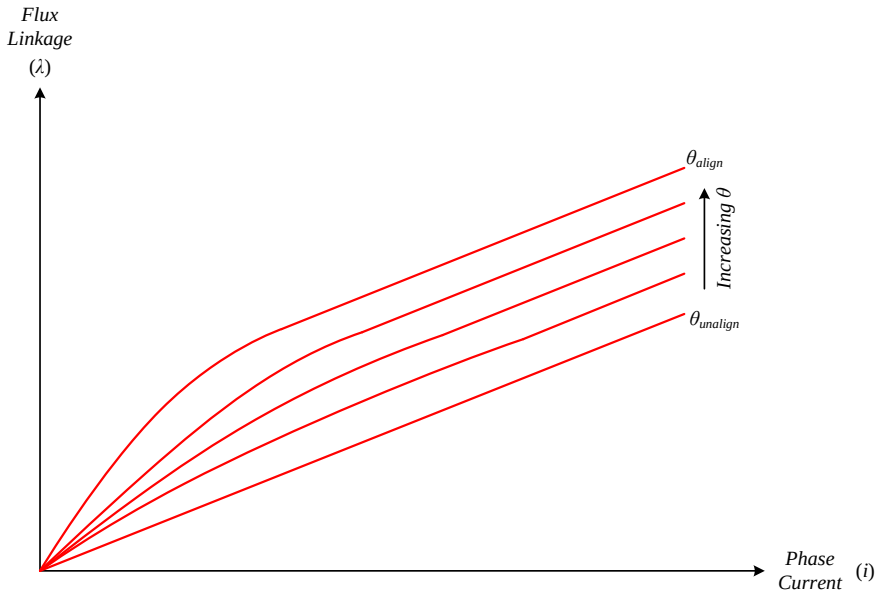


Fig. 2.3 Symbolic flux linkages vs. current characteristics for an SRM phase for different phase currents

2.2.3 Electrical and Electromagnetic Characteristics of the SRM

The flux linkages in an SRM winding, λ, are a function of θ and current, i. This variation is illustrated in Fig. 2.3, which provides a sketch of the characteristics of λ vs. i for $\theta_{unalign}$, θ_{align}, and some arbitrary positions between the two [8, 20]. At $\theta_{unalign}$ there is little or no overlap between rotor and stators poles, causing the flux to travel a significant length though air; hence, the subject phase does not experience saturation in this position. On the contrary, at θ_{align} almost all flux travels through the poles across a very small air gap, and typically saturation occurs at a fraction of the rated SRM current.

Inductance of a given phase is a function of λ, as expressed in (2.1).

$$L(\theta, i) = \frac{\lambda(\theta, i)}{i} \tag{2.1}$$

From (2.1) and Fig. 2.3, it may be deduced that in the areas where saturation does not occur, inductance is constant regardless of current. Next, Fig. 2.4 shows a typical SRM L-θ profile for various levels of current. The inductance pattern repeats every 90 mechanical degrees for a 6/4 SRM. One full repeating pattern is highlighted in solid red. Note how inductance decreases with increasing current. This is due to the fact that higher current produces more flux, but as the iron core nears saturation, reluctance to this flux increases, and hence inductance decreases. Also note how the inductance around $\theta_{unalign}$ is flat. This represents the area when there is not any partial overlap between the rotor and stator poles, and so the reluctance slightly before or after that is almost equal, meaning that inductance is also unchanged. Also around θ_{align} there tends to be flattening of L, which is more noticeable in designs with the stator pole arc larger than the rotor pole arc, making L almost constant for slight changes in rotor position around θ_{align}.

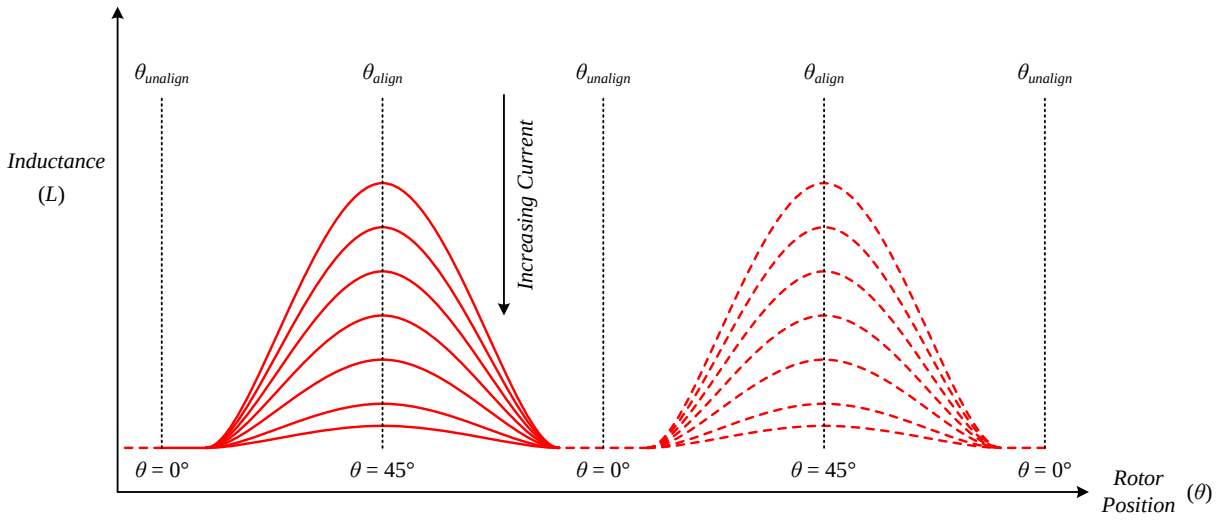


Fig. 2.4 Symbolic inductance vs. rotor position characteristics for an SRM phase for different phase currents

The length of the flat regions of L, and the change in slope of the L around the $\theta_{unalign}$ and θ_{align} positions, depend on the machine design – most prominently the stator and rotor pole arcs and also the shaping of the poles [8]. The L-θ characteristic such as the one shown in Fig. 2.4 is very important for SRM control design. To appreciate that, some more SRM model equations need to be considered. Starting from the SRM electric circuit, the following may be written:

$$v = R_s i + \frac{d\lambda(\theta,i)}{dt} \tag{2.2}$$

where v is the voltage across the phase winding, and R_s is the resistance of the phase winding.

Using (2.1) to substitute for λ, and expanding the derivative term, leads to the following:

$$\begin{aligned} v &= R_s i + L(\theta,i)\frac{di}{dt} + i\frac{dL(\theta,i)}{dt} \\ &= R_s i + L(\theta,i)\frac{di}{dt} + i\frac{dL(\theta,i)}{d\theta}\frac{d\theta}{dt} \\ &= R_s i + L(\theta,i)\frac{di}{dt} + i\frac{dL(\theta,i)}{d\theta}\omega \end{aligned} \tag{2.3}$$

where ω is the speed of the rotor. The first term represents the resistive voltage drop, the second represents the inductive voltage drop, and the third the induced electromotive force (EMF).

Multiplying (2.3) by i to get power, and after some mathematical manipulation, the following term may be derived for electromagnetic torque developed, T_e, by the SRM [8]:

$$T_e = \frac{1}{2} i^2 \frac{dL(\theta,i)}{d\theta} \tag{2.4}$$

Finally, the equation of motion describing the mechanical behavior of the SRM is given by:

$$J\frac{d\omega}{dt} + B\omega = T_e - T_{load} \tag{2.5}$$

where J is the coefficient of inertia in units of kg·m^2, and B is the friction coefficient representing frictional losses, and is in units of N.m/(rad/s).

The following may be then noted:

- From (2.4) it is seen that positive torque is produced when current is applied during the positive sloping region of L in Fig. 2.4, while negative torque is produced when current is applied during the negative sloping region of L.
- Also interesting to note from (2.4) is that T_e is a function of the square of the current, which reiterates the comment made earlier about the SRM not being sensitive to current direction and hence requiring only unipolar current to operate.
- SRMs are always operated with a power electronic converter. The converter may be easily controlled to produce current at either the upward or downward sloping inductance regions. Also by reversing the sequence in which the phases are excited, the direction of rotation may be reversed. Combining this ability to produce torque in either direction and also rotate in either direction, makes all SRM drives with a converter inherently four-quadrant drives.
- Since T_e may be adjusted through controlling the converter to provide the desired amount of current, SRM drives with converters are also inherently variable-speed drives, since speed is directly influenced by the torque T_e as per (2.5).

To further clarify how SRM control is exercised, Fig. 2.5 shows an example of how motoring torque is produced with the help of an electronic converter. The figure shows a simplified inductance profile (in solid red), and a simplified version of a typical current waveform (in dashed blue). Since current is applied during the positive slope of L, the produced torque will be positive as per (2.4), resulting in motoring operation.

Next, some important definitions for SRM-related terms that will be used throughout this dissertation are given; several of them are illustrated in Fig. 2.5. While most of these definitions are standard throughout texts and literature on SRM, there may be a slight variation in some of the definitions.

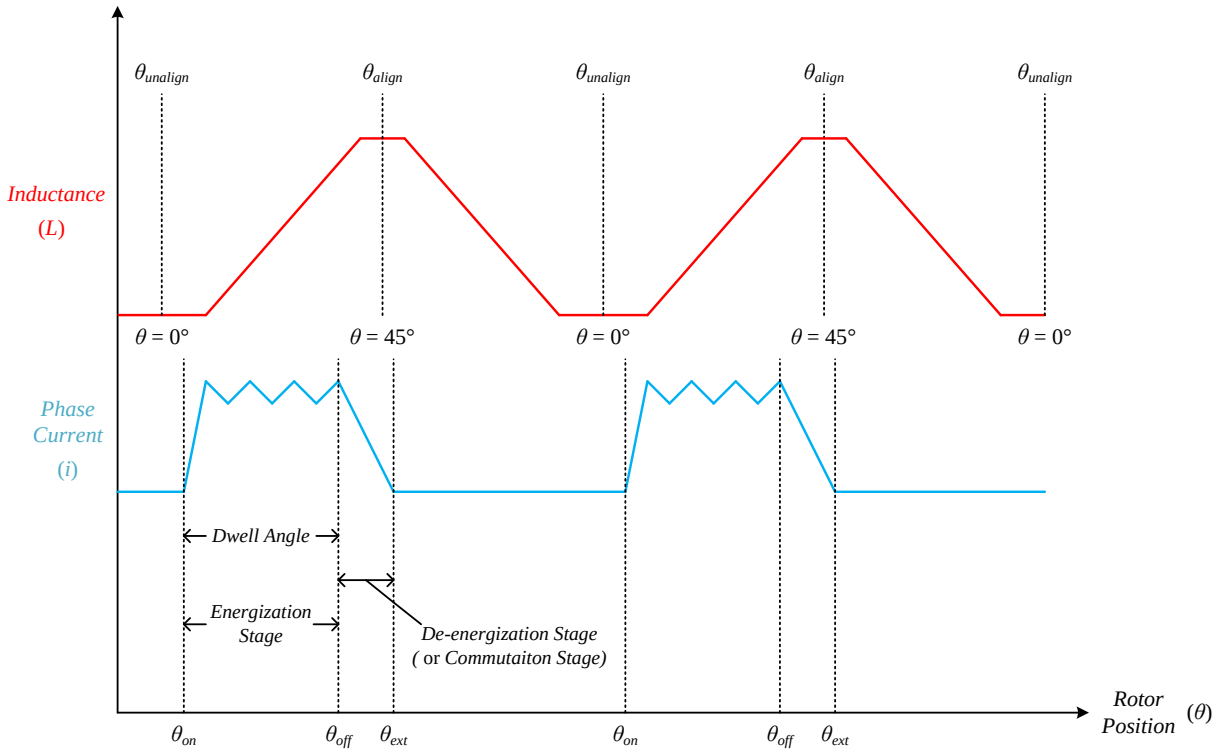


Fig. 2.5 Simplified SRM inductance and current waveforms vs. rotor position

- *Turn-on angle*: Referred to as θ_{on} from hereon, this represents the θ value (i.e. rotor position) at which the energizing voltage is applied to the phase winding, marking the beginning of the so-called energization stage.

- *Turn-off angle or commutation angle*: Referred to as θ_{off} from hereon, this represents the θ value at which the energizing voltage is removed, and substituted by either opposite or zero voltage, thus marking the beginning of the so-called de-energization stage.

- *Energization (stage)*: Also referred to as magnetization or fluxing, this is the stage at which voltage is applied to a phase winding to develop and sustain current in order to produce the flux, which in turn causes the rotor to rotate by virtue of the reluctance torque principle described earlier. Recall that the polarity of the torque developed depends on the slope of the inductance and not on the direction of the current. Therefore, the energization voltage applied to the phase may also be of any polarity – as long as it does not change within one energization cycle. In some texts the energization phase refers to only the initial rise time of the current, but here it will refer to the complete duration during which the phase remains energized (i.e. up to θ_{off}). Note that during this stage the energizing voltage is typically turned on and off to control the current. The ratio of the time the energizing

voltage is applied to the total duration of the energization stage gives the duty cycle. The initial current rise stage is typically excluded in the calculation of the duty cycle.

- *De-energization (stage)*: Also referred to as demagnetization or de-fluxing, this is the process of removing the current from the excited winding. This is usually achieved by applying voltage of opposite polarity to the one used for excitation. In cases where the converter circuit does not have the capability of applying opposite voltage, then the energization voltage is just removed (i.e. zero voltage is applied) until the current naturally dies out.

- *Dwell angle*: This is the angle given by $\theta_{off} - \theta_{on}$, and will be denoted by θ_{dwell}. This is basically the span of the energization stage explained above.

- *Dwell time or period*: This defines the time required by the rotor to travel through the dwell angle. In other words, it is from the instant θ_{on} in a given phase occurs to the instant the following θ_{off} in the same phase occurs. It will be referred to as t_{dwell}.

- *Extinction angle*: This is the rotor position at which current (and hence flux) has completely fallen to zero following de-energization of phase; it will be referred to as θ_{ext}.

- *Commutation period*: Also referred to as the fall time, this is the time duration between θ_{off} and θ_{ext}; it will be referred to as t_f.

- *Conduction period*: This is the time duration from θ_{on} to θ_{ext}. In other words, it is the combination of the dwell period and the commutation period, and represents the total time a given phase conducts current during one stroke. It will be referred to as t_{cond}.

- *Conduction angle*: This is the angle given by $\theta_{ext} - \theta_{on}$, and will be denoted by θ_{cond}.

- *Stroke*: This term is generally used to define the excitation cycle that each SRM phase goes through, consisting of the energization and de-energization stages. Therefore, in one revolution, each SRM phase goes through as many strokes as there are rotor poles. So in a 6/4, each phase goes through four strokes in a single revolution, and given it has three phases, the total number of strokes is 12. Therefore strokes per revolution is simply given by the product of the number of phases and the number of rotor poles.

2.2.4 SRM Control and the Standard Asymmetric SRM Converter

Equation (2.4) reveals that the amount of torque produced depends on the level of current and the slope of inductance. The slope of inductance is decided by the location of θ_{on} and θ_{off}. The level of current

depends on the level and duty cycle of the applied voltage. Current also depends on the inductance, which is affected by the location of θ_{on} and θ_{off}. Therefore, the SRM control variables may be summarized as:

- Energization voltage level
- Duty cycle of the voltage applied within the dwell time
- θ_{on}
- θ_{off}

At a basic level, the SRM is speed controlled. A simple PI controller computes the required torque or current based on the speed error. When the rotor reaches the θ_{on} position, the converter circuit applies an energization voltage to build current in the phase winding, as shown in Fig. 2.5. The converter circuits then maintains the current around its reference value by modulating the applied voltage – most commonly via turning it on and off – until θ_{off} arrives. At the instant when rotor position reaches θ_{off}, voltage of the opposite polarity is applied to quickly de-energize the phase. Modulation of the energization voltage may be achieved by using a second PI controller for current and directing its duty cycle output to a PWM modulator, or by using a hysteresis controller. The PWM method has the advantage of fixed switching frequency, while hysteresis has the advantage of quick response and hence high control bandwidth. Both methods fall under the category of current-chopping, in reference to the current waveform being chopped.

Many variations can be introduced to the control scheme above:

- Instead of chopping by turning on and off the applied voltage, the energization voltage itself may be continuously varied – for example by using a dc-dc converter between the front-end rectifier and motor-end converter. In effect this moves the chopping from the motor-end converter (and hence from the SRM phase) to the dc-dc converter stage. However, this solution is only feasible at very low powers. At a few kW the chopper circuit will result in high semiconductor losses, especially if the SRM is used for a high-speed application.
- As an alternative to both current-chopping and to using a continuously variable energization voltage source, only θ_{on} and θ_{off} may be varied to provide the right amount of energy needed to develop the required torque. While this seems to be an appealing alternative as it avoids chopping and hence improves efficiency, it can also have several disadvantages. In the absence of current chopping, very high peak currents can occur at low speeds. This necessitates oversizing the semiconductor devices in the driving converter circuit. Also due to this high current, a smaller dwell angle is used – as opposed to a wide dwell angle with a controlled (or chopped) current. The smaller dwell angle

results in highly pulsating torque, as there may be no overlap between the individual torque contributions from each phase.

- For high-performance drives, a combination of chopping and angle control may be applied to optimize for efficiency, low torque ripple, and other objectives.
- Various other control techniques have also been suggested. More on these may be found in specialized texts and other publications [8, 9, 19].

Going back to the basic control strategy, a commonly known converter circuit that can easily implement this current-chopping method is shown in Fig. 2.6. This circuit is known as the asymmetric converter circuit. The phase leg of each converter is identical, consisting of two switches and two diodes. The converter circuit in Fig. 2.6 is for an SRM with three phases (A, B, & C), such as a 6/4 SRM with each phase wound around two diametrically opposite stator poles. As explained in chapter 1, the dc link voltage, V_{dc}, is usually obtained from a 1ph or a 3ph ac supply using a rectifier circuit and a dc link filter capacitor.

Operation modes of the asymmetric converter circuit can be summarized as follows:

- *Energization*: When the rotor position reaches θ_{on}, the controller turns on switches S_1 and S_2, which sets $v_{ph} = V_{dc}$. This energizes the phase winding.
- *Free-wheeling*: When current in the phase winding, i_{ph}, reaches its reference level, only one of S_1 and S_2 is turned off. This forces i_{ph} to go through one switch and one diode. For example, if S_2 is turned off, i_{ph} goes through the loop formed by S_1, the phase winding, and D_1. Likewise if S_1 is turned off, i_{ph} goes through the loop formed by S_2, the phase winding, and D_2. In both cases, the dc link voltage is eliminated from the loop, making $v_{ph} = 0$. This prevents further rise in current. When the current drops to a certain level, the controller goes back to the energization mode, and so on switching between the two modes continues until the rotor reaches θ_{off}.
- *De-energization*: Once the rotor reaches θ_{off}, both S_1 and S_2 are turned off. i_{ph} is forced to go through the loop formed by D_1, V_{dc}, D_2, and the phase winding. v_{ph} is now equal to $-V_{dc}$. This negative voltage across the phase winding quickly distinguishes the current, thereby resetting the flux in that phase to zero.

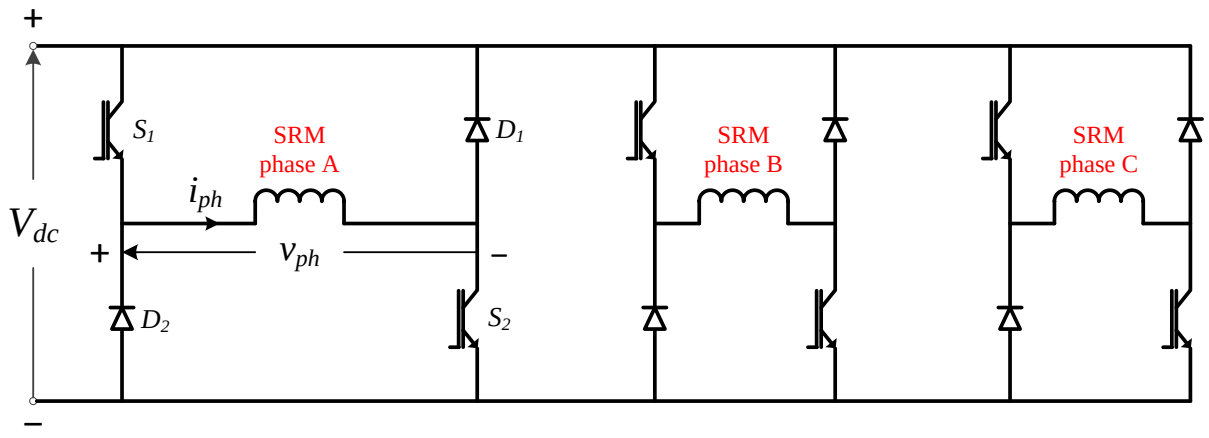


Fig. 2.6 Asymmetric converter for SRM drives

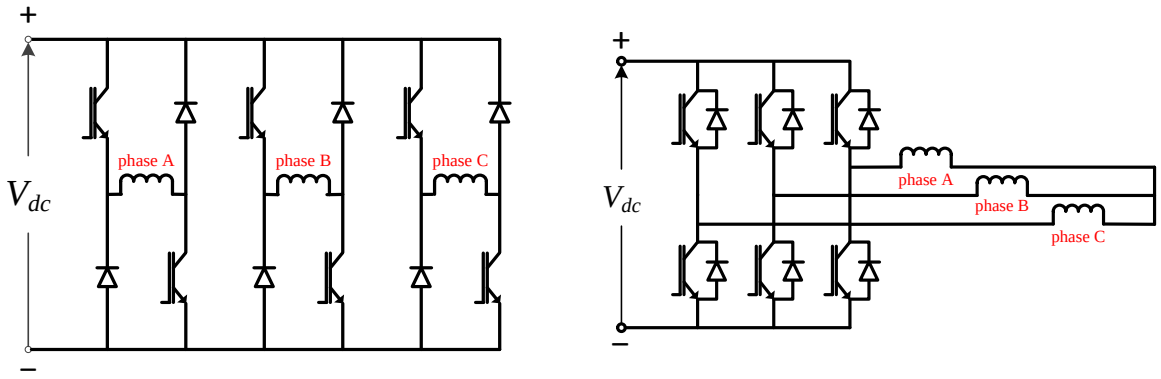
The following is noted about the operation of the asymmetric converter:

- It was noted that the free-wheeling mode can be arrived at with two different switch combinations, i.e., either S_1 on and S_2 off, or S_1 off and S_2 on. In actual operation, these two combinations are used in alternation to balance the usage among the switch pair and diode pair. This allows for choosing devices with equal ratings, and also balances semiconductor losses across the devices which puts them under the same thermal condition thereby simplifying cooling.

- Besides switching between V_{dc} and 0 to control current in the energization stage, a faster current response may be obtained by switching between $+V_{dc}$ and $-V_{dc}$ [8, ch. 4]. This reduces current ripple which consequently lowers the torque ripple. However, the machine phase windings experience twice the rate of change of voltage, putting more stress on the insulation, and also introducing more ripple into the dc link capacitor thereby potentially shortening it lifetime. Furthermore, with such strategy the switching frequency is increased, which increases semiconductor losses and reduces efficiency. Such strategy is thus usually only resorted to in high-performance drives that require fast dynamic response and low torque ripple.

- The switches and diodes need to have a minimum voltage rating equal to the dc link voltage. In practice a safety margin is kept to account for voltage spikes occurring due to the switching and other over-voltage conditions. Practical devices may thus have switches and diodes rated as much as twice the dc link voltage.

- The current rating of the switches depends on the maximum desired peak current, the duty cycle, as well as the total conduction time – since a larger conduction duration results in a larger average current in each of the diode and switch.



(a) SRM asymmetric motor-end converter (b) Standard ac motor-end converter

Fig. 2.7 Standard SRM and ac motor converters

2.2.5 Advantages and Disadvantages of SRM Drives

Having gone through the basic features and control of the SRM, it is worthwhile to summarize some of its advantages and disadvantages. To make this more meaningful, it is also important to consider these advantages in relation to its counterparts, like ac induction motors, permanent magnet motors, etc. The standard motor-end converter circuit used for both ac machines and permanent magnet motors is shown in Fig. 2.7 (b), aside the SRM asymmetric converter in Fig. 2.7 (a). One reason for the difference between the two configurations is the fact that the SRM only requires unidirectional current to operate, whereas other motors require ac current. Also since in an SRM the net torque is given by the sum of the individual phase torque contributions, an overlap between the phase torque outputs is required to provide continuity in the developed torque. This can be achieved by controlling each phase independently by carefully timing its energization and de-energization rather than depending on the state of other phases. Such operation can be obtained by using the SRM asymmetric converter circuit, and hence its difference from the standard converter circuit of most other motors, in which there is interconnection between the circuits of each phase. Advantages of an SRM include:

- *Inherent fault-tolerance*: In the converter for ac drives shown in Fig. 2.7 (b) for ac drives, if an error on part of the controller results in the two switches of the same leg being turned on simultaneously, a short-circuit loop consisting of the dc link and these two switches is formed, resulting in excessive current. This is referred to as a shoot-through fault, and usually the results in permanent damage of the switches in that phase leg. The SRM asymmetric circuit does not suffer from this problem, as there is a phase winding in series with the switch. This is not limited to the asymmetric converter circuit, but is true of almost all SRM converter circuits.

- *Independent phase operation*: It is clear from Fig. 2.7 (a) that the circuit for each SRM phase is independent of the other phases. And as mentioned earlier, the lack of overlap of phase windings

makes the mutual coupling between phases negligible. Therefore, the phases in an SRM drive are both electrically and electromagnetically independent. Therefore, in case a fault occurs in one of the phases, operation can continue with the other phases, albeit with reduced net torque and increased torque ripple.

- *High starting torque*: This follows from the fact that torque is proportional to the square of the current, as seen in equation (2.4).

- *Robustness*: As mentioned earlier in section 2.2.1, the SRM gains its robustness from its simple construction with no magnets or windings on the rotating part. This makes it capable of very high speeds, and also makes its manufacturing potentially simpler and less costly.

- *Simplified cooling requirements*: Since the rotor does not carry current, unlike the ac induction and synchronous motors, its rotor has low losses and generally does not require cooling.

- *High efficiency*: SRM drives are known to have a high efficiency over a wide speed range.

- *Inherent variable-speed and four-quadrant operation*: Though mentioned earlier, this point is reiterated for its significance. Standard SRM drives are always operated with a converter, and cannot be connected directly to and single-phase or three-phase ac supply. Through the converter control, the phase excitation sequence can be reversed, which reverses the direction of rotation. Also in either direction of rotation, any of positive or negative torque may be generated, depending on whether excitation is performed during positive sloping or negative sloping inductance. This makes any SRM drive inherently capable of operating in all four torque-speed quadrants, which are forward motoring, reverse motoring, forward generation (or braking), and reverse generation (or braking).

Disadvantages of an SRM include the following:

- *Need for converter*: The need for a converter to run an SRM stems from its high-non-linearity and the fact that stored magnetic energy needs to be dissipated or returned to the source at the end of every stroke. Therefore, for constant-speed application where ac motors like induction and synchronous motors can be used without any converter (i.e. directly connected to the line), the SRM is not cost-competitive due to the additional cost of the power-electronic converter.

- *High torque ripple*: SRMs are known to have high torque ripple due to the net torque being the sum of the individual phase torque contributions, which unless carefully managed will result in dips in torque during commutation intervals (when a phase is being de-energized and the next energized). Large torque ripple can introduce oscillations in speed and also reduce efficiency. Torque ripple

can be reduced by controlling the current during the commutation intervals such that the net torque is more or less constant. Such techniques are called current-shaping techniques. Many different methods have been proposed for the reduction torque ripple [8, ch. 5], and so this issue can be largely mitigated when required in high-performance drives.

- *High acoustic noise*: SRMs are also known for producing high audible noise, which can make it unsuitable for applications like cooling compressors that are located near the user. Again several techniques for reducing this noise have been suggested, including both machine design measures as well as control-specific measures [8, ch. 7].

- *Higher bus current ripple*: The dc link current in SRM drives tends to have higher ripple, partly for the same reason that each phase works independently and hence during commutation intervals total current drawn by all phases will experience a dip. Also if single-pulse mode is used where current is not regulated, the phase currents and hence dc link current will also experience a rise. This large ripple necessitates larger dc link capacitors. Again current shaping to improve the smoothness in the overlapping can be used to reduce the effects of this.

2.3 High Power and Multilevel SRM Converters

The advantages of SRM drives listed in the previous section makes them good candidates for high-power applications. But to be able to drive a high power motor, the power electronic converters in the drive must obviously be capable of handling that high power. Increasing a converter's operating power can be achieved by either increasing its current capacity while operating at a lower voltage, or otherwise increasing its operating voltage while operating at a lower current. Advantages and disadvantages of each approach are studied in the next section.

2.3.1 Choosing between Low-Voltage and Medium-Voltage Converters

Drives operating below the 1 kV level are usually referred to as low-voltage drives. Drives in this category are usually operated from 480 V or 600 V ac supply voltages in the United States. Low-voltage utilize standard converters such as those shown in Fig. 2.7. To reach high operating powers, each switch is replaced by several switches in parallel to share the high current. On the other hand, drives that operate in the range 1 kV to 30 kV are referred to as medium-voltage drives. Some of the advantages of using drives at the medium-voltage level over low-voltage are:

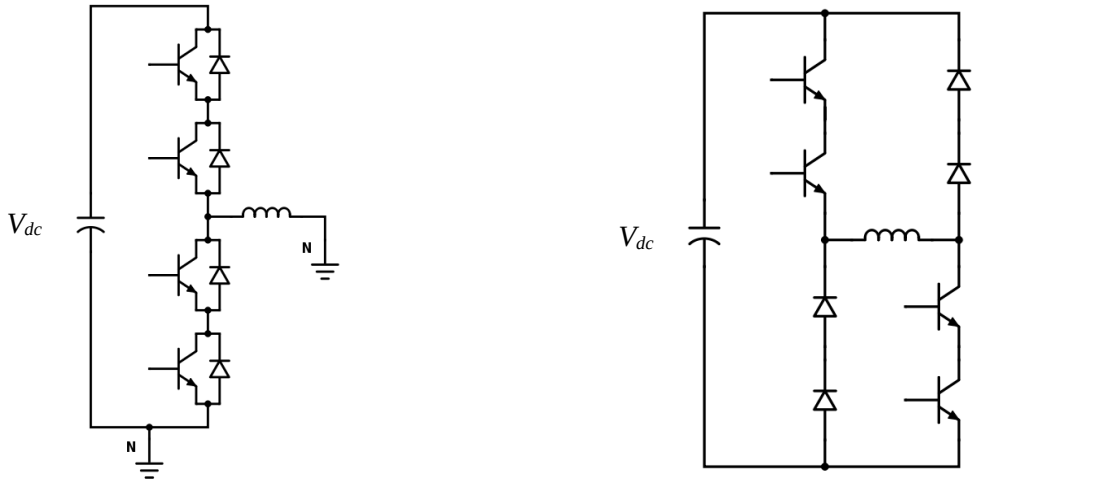
- *Higher efficiency*: Because medium-voltage drives use less current than low-voltage drives, there are less copper losses and hence higher efficiency.

- *Lower cable cost* [21]: While cables for a medium-voltage drive are expected to cost more than that of a low-voltage drive due to the increased insulation, the amount of copper saved due to lower current outweighs the insulation cost increase, making cables for medium-voltage drives less expensive overall [21]. Also since cables for low-voltage are larger, their cable tray or conduit is heavier, resulting in more expensive and more complex cable installation [21]. These two factors together mean that medium-voltage drives have a lower cost of (cable) material and have a lower installation labor cost.

- *Transformer-less operation* [21]: Use of a transformer may be avoided, since medium-voltage drives can be interfaced directly with distribution voltages like 2.3 kV, 4.16 kV, and even higher; this reduces size, weight, and cost.

On the other hand, the semiconductor cost for medium-voltage drives tends to be higher since switches in the medium-voltage category tend to cost more than low-voltage switches with higher currents. This is mainly due to higher demand for the latter, since low-voltage products are more common in the market. Also due to high demand, the manufacturing of low-voltage drives has become more of a production line-based, whereas medium-voltage drives are more custom engineered and custom manufactured. Finally, some applications require an isolation transformer anyway, which takes away the cost advantage of medium-voltage drives due to being potentially transformer-less. Therefore, it appears that medium-voltage drives have a higher first cost, but due to their higher efficiency their energy cost is expected to be lower.

Medium-voltage drives are almost exclusively used at powers above a 1000 hp (or ~ 0.75 MW), while low-voltage drives are found at powers below 500 hp (or ~ 0.37 MW) [22]. In between 500 hp and 1000 hp, the decision is based on specifics of the application and industry. Where long cables are required, medium-voltage drives are favored due to cost savings [22]. Also where there is a requirement for low harmonics at the source side, the low-voltage drives will require a filter, whereas medium-voltage drives with inherently better harmonic distortion may not [22], hence potentially favoring the medium-voltage drive due to lower cost. Examples of sectors where medium-voltage drives are used include oil and gas, mining, metals, water processing, marine, chemical, cement, pulp and paper, and others [23].



(a) One phase of ac motor converter with series switches (b) One phase of SRM converter with series switches

Fig. 2.8 Extending operating voltage with series switches

2.3.2.1 Using series switches to build medium-voltage converters

The voltage rating of a converter is limited by voltage rating of the semiconductor devices used. In today's industrial drives, perhaps the most common semiconductor switches are the IGBTs, which have a maximum voltage rating of 6.5 kV. Also integrated gate-commutated thyristor (IGCT) devices have emerged that are rated around 9.5 kV. In practice, to account for possible over-voltage transients from the supply network, the maximum operating voltage of a front-end ac-dc converter is less than half the rated voltage of the semiconductor devices used - typically 40% [24]. Therefore, standard converters such as those shown in Fig. 2.7 are only capable of operating from a 2.3 kV ac distribution-level input. To operate at the next higher ac distribution-levels, which are above 4 kV in the United States, other solutions need to be sought.

The classic way of overcoming this limitation of device voltages is to connect them in series. Taking the example of a motor-side converter, Fig. 2.8 (a) shows how series switches are utilized in an ac motor drive converter, while Fig. 2.8 (b) shows the same for an SRM drive converter. Only one phase is shown in each case, with the other phase(s) being identical. Using two switches in series instead of one as shown in these figures effectively doubles the operating voltage of the drive. However, several disadvantages accompany this solution, which include:

- Static and dynamic characteristics of semiconductor devices, though manufactured to be the same, are seldom identical. This results in an unequal distribution of blocking voltage among the devices when operated, both while they are off as well as during switching. Due to this potential imbalance, if a device is exposed to a large enough voltage that it is not capable of blocking, it could be permanently damaged. Additional snubber devices are typically used to ensure balancing of

blocking voltage, but those increase losses and result in low utilization of the power semiconductors. Overall, this increases both cost and complexity of the converter, and could result in derating the drive – i.e. operating it at a power lower than it is theoretically capable of.

- Even though each device is to block only part of the total operating voltage, the load still sees high rate of voltage change (*dv*/*dt*) during switching. This brings along issues like harmonics, electromagnetic interference (EMI), insulation stress, and motor bearing stress due to common-mode voltage.

- To provide redundancy for better fault-tolerance, duplicate or triplicate blocks may be used, but again this is costly and complex.

A more appealing solution for achieving higher operating voltages lies in what is called multilevel converters, which are taken up in the following section.

2.3.2 Multilevel Converters: Introduction, Advantages, Disadvantages, and Applications

The first concept of multilevel power electronic converters was introduced around four decades ago for ac converters, and since then work on them has been extensively published [25]-[29]. Currently multilevel converters for ac loads are commercialized in a very wide range of applications in many sectors. Generally, any multilevel converter can be equally used as either a front-end rectifier (converting ac-dc), or as a load-side converter (converting dc to ac or variable voltage).

The idea behind multilevel converters is to use smaller switches to collectively serve the higher operating voltage, with the voltage of each being fixed by some mechanism – as opposed to simply placing switches in series with possible variation of voltage across the switch. A second major goal of multilevel converters is to provide the ability to vary the voltage seen by the electric load in steps. This powerful advantage of being able to operate in smaller *dv*/*dt* steps provides several benefits, which include:

- Switching occurs at a lower *dv*/*dt* in multilevel converters, which reduces switching losses in the semiconductor devices. And even though multilevel converters tend to have more switching devices than traditional converters, their overall efficiency is usually better due to the significant reduction in switching losses per device, especially at higher operating voltages.

- Multilevel converters are better capable of producing staircase-like waveforms that are closer to a sine wave, which reduces harmonic distortion in the generated voltage and current waveforms, and also decreases the radiated EMI. When used as a front-end converter (i.e. rectifier), this reduction of distortion lowers the filtering requirements – or even dispenses with it.

- Multilevel converters produce smaller common-mode voltages, which results in less stress on motor bearings. In some cases common-mode voltages may be completely eliminated with multilevel converters.

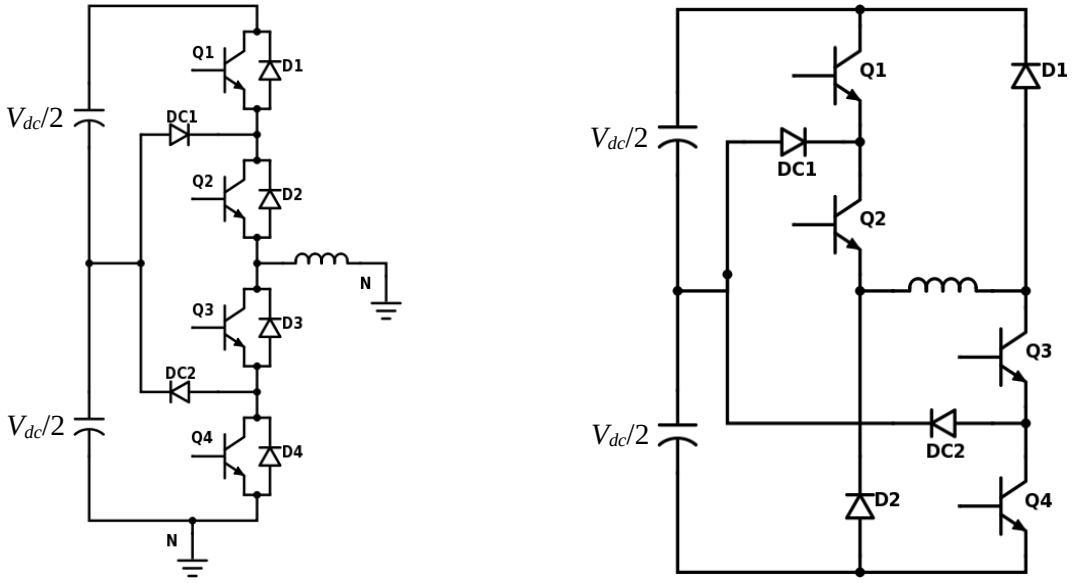
- Since multilevel converters can reach high operating voltages, the need for a step-down transformer to interface with the higher distribution-level voltages may be avoided.

A disadvantage of multilevel converters is the fact that they use more switches, which also includes more switch driving circuits, and hence tend to be more expensive. However, the benefits obtained from using multilevel converters tend to offset and/or justify this increase in initial investment. Another disadvantage is that control complexity is high in some multilevel converters, but some multilevel topologies have relatively simple control. Finally, with an increased device count, balancing usage among switches to maintain thermal uniformity becomes a challenge is some multilevel converter topologies. But again, especially in cellular structures which will be soon described, this issue is highly mitigated. Below are some examples of where multilevel converters are used today, which testifies to their success as a viable solution for medium-voltage high-power applications:

- *Variable speed drives*: One of the major areas where multilevel inverters are employed are variable-speed drives in the megawatt range. Application examples of this includes: i) pumps and compressors in oil and gas, water, and wastewater treatment, ii) high-power blowers in cement industry, iii) mining, and iv) traction, such as electric rail and naval transportation.

- *Renewable energy*: Wind energy is seeing increased penetration in energy market. Today's wind turbines can be as large as 4 MW per turbine or higher. To handle such power, either parallel low-voltage converters (with coupling transformers) are used, or else medium-voltage multilevel converters. Solar and fuel cells can also be integrated in multilevel converters with cellular structures.

- *Power quality improvement*: The voltage levels of the transmission network are always very high, and so are many of the distribution network voltage levels. Modern power quality equipment for filtering harmonic currents, voltage regulation, reactive power compensation, load balancing, flicker mitigation and others are based on power electronic converters. At such high voltage levels, multilevel converters provide a convenient solution, without the need for using transformers between the network and the power quality equipment.



(a) One phase of ac NPC converter (b) One phase of SRM NPC converter

Fig. 2.9 Neutral-point clamped multilevel configurations for ac motor and SRM converters

2.3.3 Multilevel Converter Configurations

Generally multilevel converters can be built using what are called clamping techniques, or using cellular structures. Combinations of the two also exist in so-called hybrid multilevel converters. Out of all known ac multilevel converters, four configurations have become very popular, with some of them having been applied widely in practice [28, 29]. The following review will focus on those four topologies, with mention of some of the other important ones. The interested reader may gain more information on other multilevel configurations from literature or texts and textbook chapters [25]-[30]. Since the development of multilevel converters has been primarily targeted to ac applications, this review will based on ac multilevel converters. But as many of these topologies can be adapted to work for the SRM, previously published adaptations of these converters for SRM will also be presented aside the ac multilevel converter. Unlike the ac multilevel converters which have been commercialized over a decade or two ago, it is highly unlikely that any of the SRM adaptations have found their way into commercial applications yet, being only newly introduced, and due to the slow-changing nature of technology in high power applications.

2.3.3.1 Neutral point clamped multilevel converter

Fig. 2.9 (a) shows a single phase of an ac multilevel converter called the diode clamped or neutral point clamped converter. Similar to the configuration in Fig. 2.8 with switches in series, here also double the number of switches are used to double the operating voltage. However, the dc link capacitor is split into two that equally share the dc link voltage. Two clamping diodes, DC1 and DC2, are used to “clamp” the voltage across each device to only one of these two capacitors. Switches Q1 and Q3 work in complementary fashion, and so do Q2 and Q4. This means that when Q1 is turned on for example, Q3 is off, and vice versa.

When both switches Q1 and Q2 are turned on, the voltage across the phase winding is the full V_{dc}. Current in this case could be going from the converter into the winding through switches Q1 and Q2, or it could be flowing from the converter into the winding through diodes D1 and D2. Now consider the case where Q1 is off and Q2 turned on (and hence Q3 is on and Q4 is off). When current is flowing into the motor winding, it comes through the lower capacitor, DC1, and Q2; the phase winding voltage is $V_{dc}/2$. This intermediate voltage was not possible with the standard converter of Fig. 2.7 (b). Also note that since DC1 conducts, it connects Q1 in parallel to be the upper capacitor only, thereby limiting the voltage Q1 is to block to $V_{dc}/2$ only. In this way the switches always end up blocking the equivalent of one capacitor's voltage. In the same example when current is flowing from the winding into the converter, it goes through Q3, DC2, and the lower capacitor, with the phase winding voltage still being $V_{dc}/2$. Zero voltage across the winding is obtained by turning off Q1 and Q2; current in this case goes through Q3 and Q4 (when flowing into converter) or through D3 and D4 (when flowing into winding).

The neutral point clamped converter therefore achieves both primary goals of the multilevel approach, which are the ability to use smaller switches to collectively operate at higher voltages, and synthesizing a phase voltage with more intermediate steps than the standard ac converter in Fig. 2.7 (b). An adapted version of the neutral point clamped converter for SRM drives presented in [31] is shown in Fig. 2.9 (b). Here also three different levels of phase voltage can be applied as opposed to two that are possible with the standard SRM asymmetric converter in Fig. 2.7 (a). An approach for the control of the neutral point clamped converter for SRM is provided in [32].

With regards to voltage magnitude – and regardless of the polarity of the voltage – the standard converters of Fig. 2.7 with a single dc link capacitor are called two-level converters since they can only output two distinct phase voltage levels. The neutral point-clamed configurations of Fig. 2.9 are referred to as three-level converters since they can output three different phase voltage levels. But the neutral point clamped configuration can also be theoretically extended to any voltage level. For a dc link subdivided by N-1 capacitors, N different phase voltage levels are possible, and the voltage across each device is always limited to the voltage across each capacitor. However, as this topology is extended, it becomes quite complex. In configurations beyond three-level, the clamping diodes have to block different voltages, and this applies to the SRM-adapted version as well. A consequence for this is that the diodes with the larger voltages will have large transients and higher turn-off losses. Otherwise, a series connection of diodes (with the same voltage rating each) may be used instead of one diode of high blocking voltage, but this increases cost and decreases reliability due to increased device count. Other disadvantages of this topology include:

- Successful operation of this converter assumes that all capacitors in the dc link are at the same voltage. But when intermediate voltage levels are used, some capacitor(s) are charged or discharged

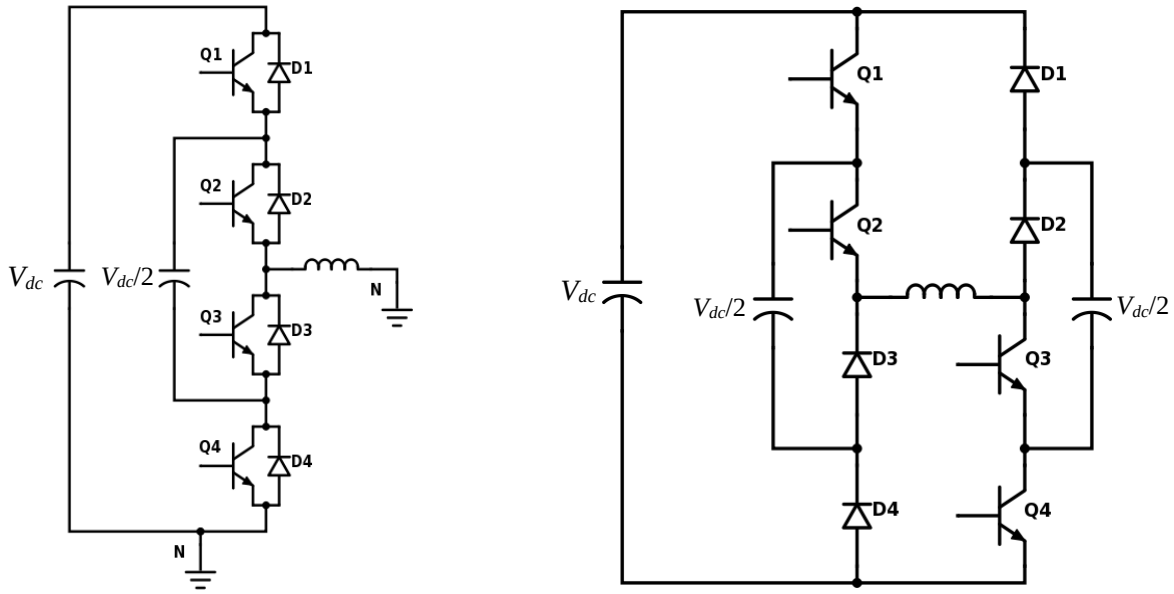
while the other(s) remain unchanged. Therefore, care has to be taken in alternating capacitor usage such that their voltage remains balanced. In ac drives, a challenge that arises here is that some switch combinations are not allowed because their output voltage is not deterministic but rather depends on current direction. This limits the flexibility in choosing the states needed to balance the dc link capacitor voltages under certain operating conditions. As a consequence, balancing the capacitor voltages in versions beyond the three-level is challenging; drives it requires extra devices or intelligent control, and may place a limit on the maximum allowable modulation index, thereby imposing operation limits on the converter. For the SRM version, the neutral point clamped converter was not studied previously in literature beyond the three-level version, but nevertheless the complexity of the circuit as it grows makes it undesirable.

- In both the ac version and SRM version, the inner devices conduct more than the outer ones, necessitating component oversizing and potentially posing thermal balancing issues.

Given the complexity of this topology beyond three-levels, it is not commonly found in versions above three-level in ac applications. With today's high-voltage IGCT devices, it has become possible to directly interface a three-level neutral-point clamped converter with the 7.2 kV distribution voltage level [33]. Its industrial applications extend to powers up to tens of megawatts [28, 29]. To overcome some of the disadvantages of the neutral point clamped topology, a modification for the ac version was suggested that replaces the clamping diodes with active switches, in the so-called active neutral point clamped converter [34]. This easily allows for capacitor voltage balancing as well as balanced switch usage under all operating conditions, with the latter leading to thermal balancing among the switches.

2.3.3.2 Capacitor clamped multilevel converter

Another clamping-based topology is the capacitor clamped multilevel converter, which uses capacitors rather than diodes for clamping. A single phase of this topology is shown in Fig. 2.10 (a) for an ac motor-side converter. Its adaptation to SRM presented in [31] is shown Fig. 2.10 (b). In this topology, different capacitors have different voltage levels; the output voltage step size is the increment from one capacitor to next. The configuration shown can output three phase voltage levels, namely 0 V, $V_{dc}/2$, and V_{dc}. As with the neutral point clamped topology, this topology can also be extended to higher voltages, where it can also output more distinct voltage steps. Also worth noting about this converter is that it may also be categorized as cellular or modular, as it is basically composed of similar blocks of two switches and a capacitor each – though the voltage of each block is different. This somewhat simplifies the layout and connections of the converter. Capacitor voltages are kept balanced by judiciously using the intermediate voltage levels such that the average energy circulating in each capacitor is zero.



(a) One phase of ac capacitor clamped converter (b) One phase of SRM capacitor clamped converter

Fig. 2.10 Capacitor clamped multilevel configurations for ac motor and SRM converters

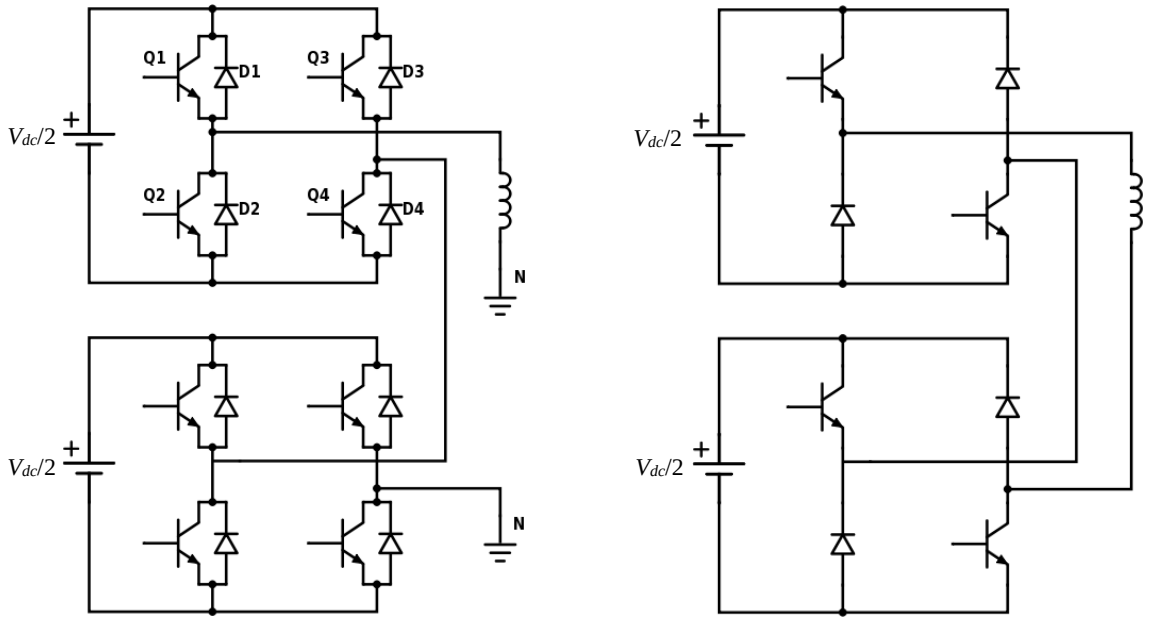
An advantage of this topology is that unlike the neutral point clamped converter, balancing the capacitor voltages is possible under all operating conditions. The reason for this is that there are no forbidden states in this converter, and all intermediate voltage levels can be obtained by several different combinations of switch states. This gives the converter the flexibility needed to ensure capacitor balancing under any operating condition. A second advantage of this converter is that the presence of many capacitors enable ride through of short-duration outages and deep voltage sags.

Some disadvantages of the capacitor clamped converter include:

- To keep the capacitors properly balanced, a relatively high switching frequency is required to help keep the capacitor voltage fluctuations low – unless large, expensive, capacitors are used. This, combined with the cost and volume of the capacitors, usually limit its use in practice to up to four or five levels [28, 29].
- Control of the different capacitor voltage levels could be complicated.
- Pre-charging the capacitors is more challenging than in the diode-clamped where all capacitors can be easily pre-charged as a group.

2.3.3.3 Cascaded H-bridge multilevel converter

The cascaded H-bridge ac multilevel converter [35] is one of the most prominent ac multilevel converters, and is the preferred choice for voltages above 7.2 kV – which is the highest ac input voltage that a three-level neutral point clamped converter using high voltage IGCT devices can be interfaced with.



(a) One phase of ac cascaded H-bridge converter (b) One phase of SRM cascaded bridge converter

Fig. 2.11 Cascaded H-bridge (for ac motors) and cascaded asymmetric bridge (for SRM) converters

One phase of the ac cascaded H-bridge converter circuit is shown in Fig. 2.11 (a), and its adaptation to SRM that is presented in [31] is shown in Fig. 2.11 (b). The converter is composed of cells; for the ac version, each cell is basically a single-phase inverter, converting dc voltage to single-phase ac voltage. Like any ac converter, the switches connected to each other work in complimentary fashion. For example, in the top cell of Fig. 2.11 (a), when Q1 is on, Q2 is off, and vice versa. The same applies to Q3 and Q4. When Q1 and Q4 are turned on, the voltage generated by the cell is $+V_{dc}/2$ – considering that the top terminal of the cell is positive. On the other hand, when the Q2 and Q3 are turned on, the voltage across the cell is $-V_{dc}/2$. Zero voltage is obtained by turning off all switches. Therefore, each cell is capable of generating a positive, negative, or zero voltage. Any number of cells can be added in series. For N separate cells of equal voltage, the number of different voltage levels obtainable across the phase winding is $2N+1$ – hence a very high number of levels is made available to the load. More levels can even be obtained by using cells with different voltage levels each – although uniformity is lost.

A drawback of this configuration is the requirement for a source for each cell. The sources are typically obtained using an input transformer with as many secondary windings as there are cells in all phases combined. Each three-phase secondary winding is then connected to a three-phase rectifier block, which then connects to the cell through a filter capacitor. Therefore, between the ac input and ac output of each cell, there is a three-phase rectifier block that has six switches, a dc link capacitor, and a single-phase inverter input. With so many switch requirements and hence the increased cost, this configuration is usually

only favorable at high voltages and high powers that are not practically obtainable with the neutral point clamped and capacitor clamped converters. But this configuration has also many advantages:

- A better waveform quality at the output side is obtainable using this converter due to the high number of voltage levels per phase.
- By phase shifting the secondary windings with respect to each other, the waveforms at the input side are also of less harmonic distortion. This high power quality improves overall efficiency and makes it easy to meet the standards for input power quality required by some regulations, almost without any need for a filter.
- The modularized layout and packaging results in easier manufacturing.
- Redundancy can be easily built in by adding spare cells, making it a very attractive option for critical applications requiring high reliability and high uptime.
- Since the dc link capacitors are directly connected to rectifiers and hence are controlled, this configuration does not suffer from the capacitor voltage balancing problem of the neutral point clamped converter, making its control simpler regardless of the number of levels of the converter.

The SRM adaptation of this converter in Fig. 2.11 (b) is very similar in both construction and operation. It has the same requirement for sources, which means that it requires a special transformer with many secondary windings, each connected to the cell shown in the figure through a three-phase rectifier block and a filter capacitor. However, the since an SRM requires only unipolar current to operate, the number of switches and diodes are less than those required for the ac version. By turning on both switches in the cell, the cell output voltage is $+V_{dc}/2$. Once current is flowing, if only one of the two switches is turned off, current will circulate through the other switch (that is on) and the diode across it on the other limb, which will result in the voltage output of the cell to be 0 V. This mode is called freewheeling, referring to the current flowing freely even after the driving voltage is withdrawn. Also while current is flowing, if both the switches are turned off, current is forced to go through the diodes, which results in $-V_{dc}/2$ appearing at the cell output terminals. Hence, though the SRM version of the cell uses less components, it is still capable of generating a positive, negative, and zero voltage, just like its ac counterpart. The difference between the two is that negative voltage cannot be forced when current is zero, but only during freewheeling – but this is sufficient for the full operation of the SRM in all four quadrants of torque and speed.

The SRM version of the converter, may be called the cascaded asymmetric bridge, or CAB SRM converter for short. This converter will be further studied in chapter 6 as part of a detailed comparison with the converter that will be proposed in this work.

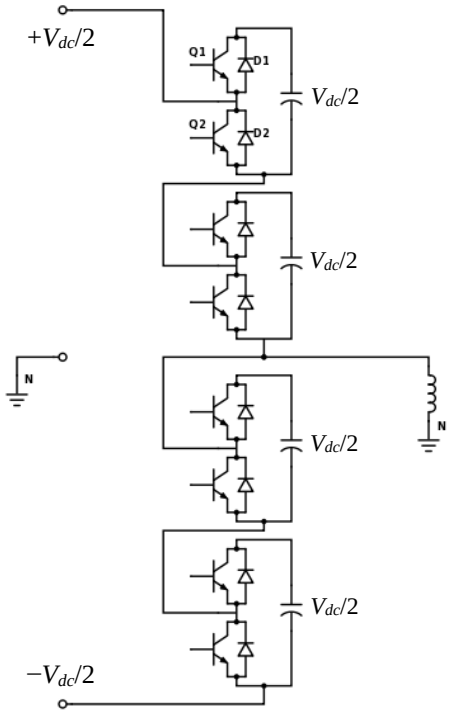


Fig. 2.12 Modular multilevel converter for ac loads

2.3.3.4 Modular Multilevel Converter

The modular multilevel converter (MMC) is a rather recent addition to the ac multilevel converters family [36]. The MMC also belongs to the cellular structure category. It is composed of a cascade of half-bridge cells, as seen in Fig. 2.12, which shows one phase leg of the converter. The state of the two switches in each cell during the operation of the converter is always complementary. When the top switch in a cell is turned on and is conducting current, the voltage at the cell terminals is equal to the capacitor voltage, which is $V_{dc}/2$ in this case. Also when current is forced to flow through the top diode the voltage at the cell terminals is equal to the capacitor voltage. On the other hand, if the bottom switch is on and conducting current, the voltage across the terminals of the cell is 0 V. The cell voltage is also 0 V when current is forced to flow through the bottom diode.

This topology is very flexible and can have any (even) number of cells in series. The total number of capacitors conducting at any time should be such that the total voltage from the top dc link rail to the bottom dc link rail is V_{dc}. In the example shown in Fig. 2.12 with four cells per phase, two out of the four cells should always have their capacitors conducting. The output ac voltage, which is the voltage across the phase winding shown in Fig. 2.12, can then be synthesized by inserting or removing capacitors to get the desired voltage. For example, when the cell voltages of the top two cells are both set to 0 V (by turning on the bottom switch of each so they conduct current and bypass the capacitor), then the output phase voltage is $+V_{dc}/2$. In this case both capacitors of the two bottom switches must be conducting to maintain V_{dc} across

the dc link. Next if one of the capacitors in the upper two cells is conducting, then the output phase voltage is 0 V. Finally, if both upper cells have their capacitors conducting, then the output phase voltage is $-V_{dc}/2$. For an MMC with $2N$ cells in one phase leg, i.e. N on the upper side and N on the lower side, the number of levels in the phase-to-neutral voltage is $N+1$.

This converter brings about a whole new concept; it combines the modularity of the cascaded H-bridge multilevel converter with the use of capacitors only as opposed to sources, like in the capacitor-clamped multilevel topology. Note that when capacitors in the MMC conduct current, they are charged or discharged – depending on the direction of the current. Several algorithms have been proposed to control the capacitor voltages. In general, when the current direction is such that it would charge the cell capacitor, then the cells having the lowest capacitor voltages are given priority to be inserted. On the other hand, if current direction is such that it would discharge the cell capacitor, cells with the highest capacitor voltages are given priority to be inserted. This method also inherently supports thermal balancing of the devices and capacitors by virtue of rotating their operation. This process can take place independent of the main operation of the converter, and at a rate that is as low as milliseconds [36].

One of the disadvantages of this converter is that a circulating current travels through legs of different phases without going through the load. This current can cause additional losses and increased capacitor ripple. Methods to control ad suppress this circulating current have also been proposed.

Only one adaptation of this converter for SRM has been reported in literature [37]. However, the proposed topology uses capacitors in series, which takes away the modularity advantage of the converter. Also, the capacitor voltage balancing is not explained.

2.3.3.5 Other SRM converter configurations

Since the focus of this work is on high-power SRM converters, cost-saving converters targeted for low-power, high-volume applications are not considered in this review. A summary of such converters may be found in [8]. Besides the standard multilevel configurations discussed above, other converters have been proposed in literature that are not designed to be scalable but can just provide one or two additional voltage levels on top of the dc link voltage – and so technically they may be considered multilevel. These converters are not necessarily targeted to high powers, but since they can provide extra voltage levels they have the potential to serve higher operating powers than the standard asymmetric converter of Fig. 2.7 (a). Therefore, it is useful to review a few such converters.

The main motivation for having an extra voltage level on top of the dc link is to allow the drive to run at higher speeds. The reasoning for this is explained in what follows. The torque developed in an SRM is mainly dependent on current, while the speed of the SRM is mainly dependent on the maximum available

energizing voltage – provided enough current capability is also available. As the speed of the SRM increases, the phase back emf also increases. Since back emf opposes the energizing voltage, its increase reduces the net voltage across the winding, thereby limiting the ability of developing current in the winding at high speeds. In fact, the rated speed of the drive is around the point where the maximum back emf reached during the energization stage is approximately equal to energization voltage. This is why the phase is typically excited before the $\theta = 0°$ position, i.e., where inductance and back emf are both lowest, so that enough current develops before these voltages rise above the energization voltage. Besides advancing the energization, some converters were proposed that provide an extra voltage boost at the initial stage of energization, which reduces current rise time thereby allowing more current to be developed at higher speeds. Both of the measures, advancing and providing a boost voltage to initially develop higher current, effectively increase the torque capability of the SRM drive, and hence its speed.

Providing an increased voltage during demagnetization as well provides for higher speeds. At high speeds when the stroke duration is very short, the current extinction angle extends into downward sloping inductance region, thereby resulting in a negative torque contribution form that phase. However, due to overlap in torque production in most SRM designs, the net torque almost always remains positive. But this negative torque contribution reduces the SRM efficiency and also prevents the drive from reaching higher speeds. Therefore, some of the circuits that were proposed provide an increased voltage during demagnetization as well. One such converter, presented in [38], is shown in Fig. 2.13. Note how besides the dc link capacitor, there is an extra capacitor per phase. Using certain switch combinations, the dc link and phase capacitor may be put in series with the extra phase capacitor, thus providing a large voltage for initial energization. Once the current has reach the desired level, the extra capacitor voltage may be removed from the loop and only the dc link can continue to provide energy for the remainder of the stroke.

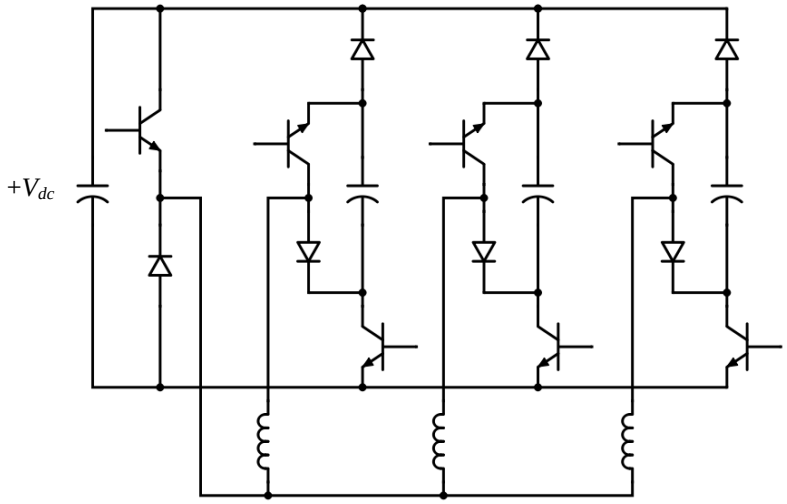


Fig. 2.13 SRM converter with extra optional voltages for energization and de-energization

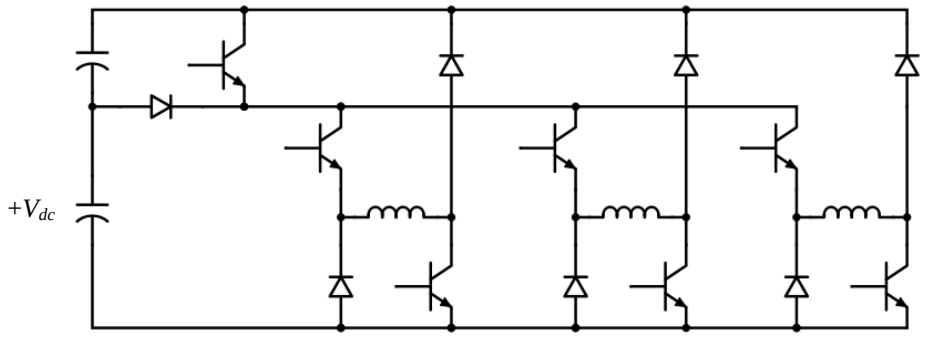


Fig. 2.14 SRM converter with an additional optional voltage for energization and de-energization

In the same circuit of Fig. 2.13, an increased voltage is also available during demagnetization. When all switches are turned off, the current is forced to enter both capacitors from their positive terminals, resulting in the sum of the two capacitor voltages appearing across the winding. This allows for faster de-energization and hence results in less of a negative torque contribution, which simply translates to higher speed capability. A modification to the circuit in Fig. 2.13 is also presented in [38], where yet another level of voltage is made available. In addition to the dc link source and the controlled phase capacitor shown in Fig. 2.13, the modified configuration provides a third source that can be inserted in series with those two. The extra source is suggested to be a battery of supercapacitors. The suggested application of this circuit as per [38] is in electric vehicles. While this circuit is useful, it is not meant for multi-megawatt powers. It also lacks the modularity and redundancy requirements set forth for the sought converter in Chapter 1.

Another converter with a voltage boosting capability, presented in [39], is shown in Fig. 2.14. This circuit is simpler than the one above, but no details are provided about the control of the extra capacitor's voltage. Therefore, the extra capacitor could have fluctuating voltage. This is not a major issue for SRM, but nevertheless this converter does not meet the modularity and redundancy criteria mentioned in chapter 1, and is not intended for multi-megawatt applications. In [40] and [41], modified versions of the ac matrix converter are suggested as converters for SRM drives. However, those are only suitable for low powers.

So in general it is seen that very little work has been done on medium-voltage converters for SRM drives. Out of the converters that were reviewed, as well as others in literature, perhaps the only converters that have the potential to scale to medium-voltage levels are the three multilevel converter adaptations described above. Out of those three, the neutral point clamped and capacitor clamped converters do not allow for easy modular replacement of a failed section, nor do they have built-in redundancy capability. They are still useful in applications not requiring modularity and redundancy, and their three-level version can serve drives up to 7.2 kV ac input as earlier mentioned.

The cascaded asymmetric bridge converter is the most attractive of the three. In fact, its ac version is also the preferred choice for high-power, medium-voltage, ac drives. This is owing to its high level of

modularity and built-in provision for redundancy. Perhaps the only major disadvantage of this configuration is the need for the large transformer with many secondary windings, whose construction and connections could become quite complex when a large number of cells are used. Besides, the fact that the sources are distributed makes it impossible to use any of the traditional single dc bus rectifiers, thus limiting its front-end choices.

In the next chapter, a novel converter is proposed that easily scales to any voltage level and does not require such transformer. It is also modular, and has built-in provision for redundancy. Chapters 3 to 6 are dedicated to the operation and control of this converter, but in chapter 6 a detailed comparison of the proposed converter with the cascaded asymmetric bridge converter is given.

Chapter 3

Novel Multilevel Converter for Variable-Speed Medium-Voltage Multi-Megawatt Switched Reluctance Motor Drives

3.1 Introduction

As explained in chapter 2, resorting to high voltage levels when operating in the multi-megawatt level is important as it results in better efficiency as well lower cost when compared to high current solutions at lower voltages. It was also argued in chapters 1 and 2 that switched reluctance motor (SRM) drives are well suited for multi-megawatt operation. Reasons for that include its simple construction and lack of permanent magnets or rotor windings. This makes it robust, and renders it suitable for high-speed operation. It also makes it potentially both easier and less costly to manufacture compared to other currently used high-power drives – like synchronous motor drives and induction motor drives. The SRM also displays a high efficiency over a wide speed range. Further advantages relevant to multi-megawatt operation include the inherent short-circuit fault tolerance of typical SRM drives, as well as the independence of phases and the ability to operate with reduced phases, if temporarily needed.

The goal of this work is to propose a converter for SRM drives suitable for the medium-voltage level which it may be generally defined as that above 1 kV, and can extend up to 35 kV. In any case, the converter should theoretically be scalable to any voltage level. Criteria sought in this converter are:

- **High Modularity**: The converter must be constructed from small building blocks or modules, and should avoid large central components as much as possible. This improves reliability, results in easy scalability and simpler manufacturing, and provides more possibilities of incorporating redundancy.

- **High Reliability**: The converter must have some level of redundancy such that certain failures may be tolerated. This improves the converter uptime, which is critical in multi-megawatt applications.

A converter that addresses the requirements above is proposed and explained in this chapter. The converter is mainly targeted to high-speed applications at the multi-megawatt level, such as compressors in natural gas production and transmission. But the converter may also be useful at sub-megawatt power levels

in critical applications where reliability and performance take priority over cost. Section 3.2 introduces the building block of the novel converter. Section 3.3 presents the novel converter topology and explains its principle of operation. Section 3.4 explains how the cell capacitors may be initially charged prior to operation. Finally, advantages and disadvantages of the converter are discussed in section 3.5.

3.2 Building-Block of the Novel Converter

The new converter is based on a simple chopper cell building block, referred to here as "cell". Fig. 3.1 (a) shows a diagram of one cell; the different states in which the cell operates are shown in Fig. 3.1 (a) - (e). The building block itself is not new and has in previous converters, the first of which was perhaps the ac MMC converter that was explained in the literature review section of chapter 2. Within a cell, the switch or diode drawn vertically are given subscript *v*, while those drawn horizontally are given subscript *h*. Note that i_{cell} is always equal to i_{ph}. Each cell has four useful states, which are described below:

State 1: Shown in Fig. 3.1 (b), S_v is turned on while S_h is off. i_{cell} is positive, and it passes through S_v, thus bypassing the cell capacitor. v_{cell} is unchanged in this state.

State 2: Shown in Fig. 3.1 (c), S_v is off while S_h is on. i_{cell} is negative, and it passes through S_h and the cell capacitor. v_{cell} decreases in this state.

State 3: Shown in Fig. 3.1 (d), both S_v and S_h are off, and i_{cell} is positive. This state naturally occurs after state 1 when S_v is turned off. i_{cell} passes through D_h and the cell capacitor. v_{cell} increases in this state.

State 4: Shown in Fig. 3.1 (e), both S_v and S_h are off, but i_{cell} is negative. This state occurs naturally after state 2 when S_h is turned off. i_{cell} passes through D_v, thus bypassing the cell capacitor. v_{cell} is unchanged in this state.

Not allowed: The state where both S_v and S_h are on is not useful and is not allowed.

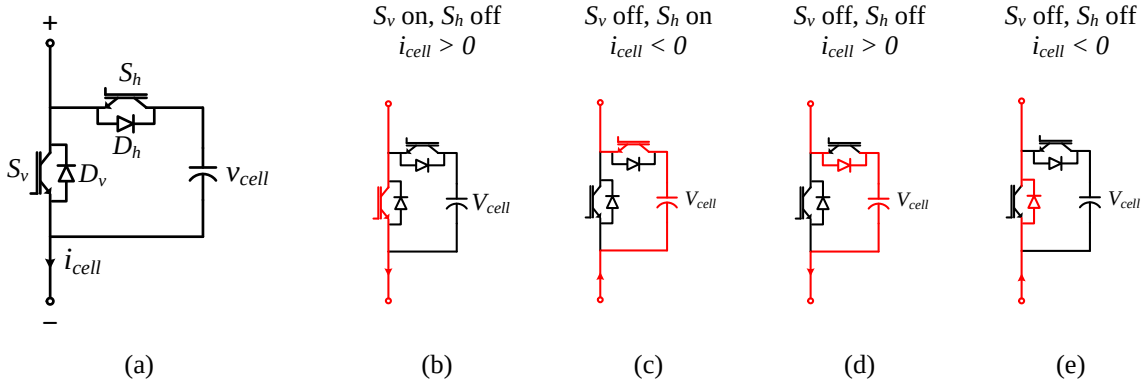


Fig. 3.1 Useful states of a cell in the proposed CCC SRM converter

3.3 The Novel Cascaded Chopper Cell Converter

Each phase leg of the converter contains an arbitrary number of cascaded chopper cells connected in series with the phase winding. The converter is hence named the cascaded chopper cell converter, or CCC converter for short. Each cell contains a capacitor that defines the voltage of the devices in that cell. All cells are identical on terms of device ratings and capacitor size and ratings. Fig. 3.2 shows a 4-cell (per phase) version of the CCC converter for a 3ph SRM drive. V_{dc} is the nominal dc bus voltage, v_{ph} is the instantaneous voltage across the SRM phase winding, and i_{ph} is the instantaneous SRM phase current.

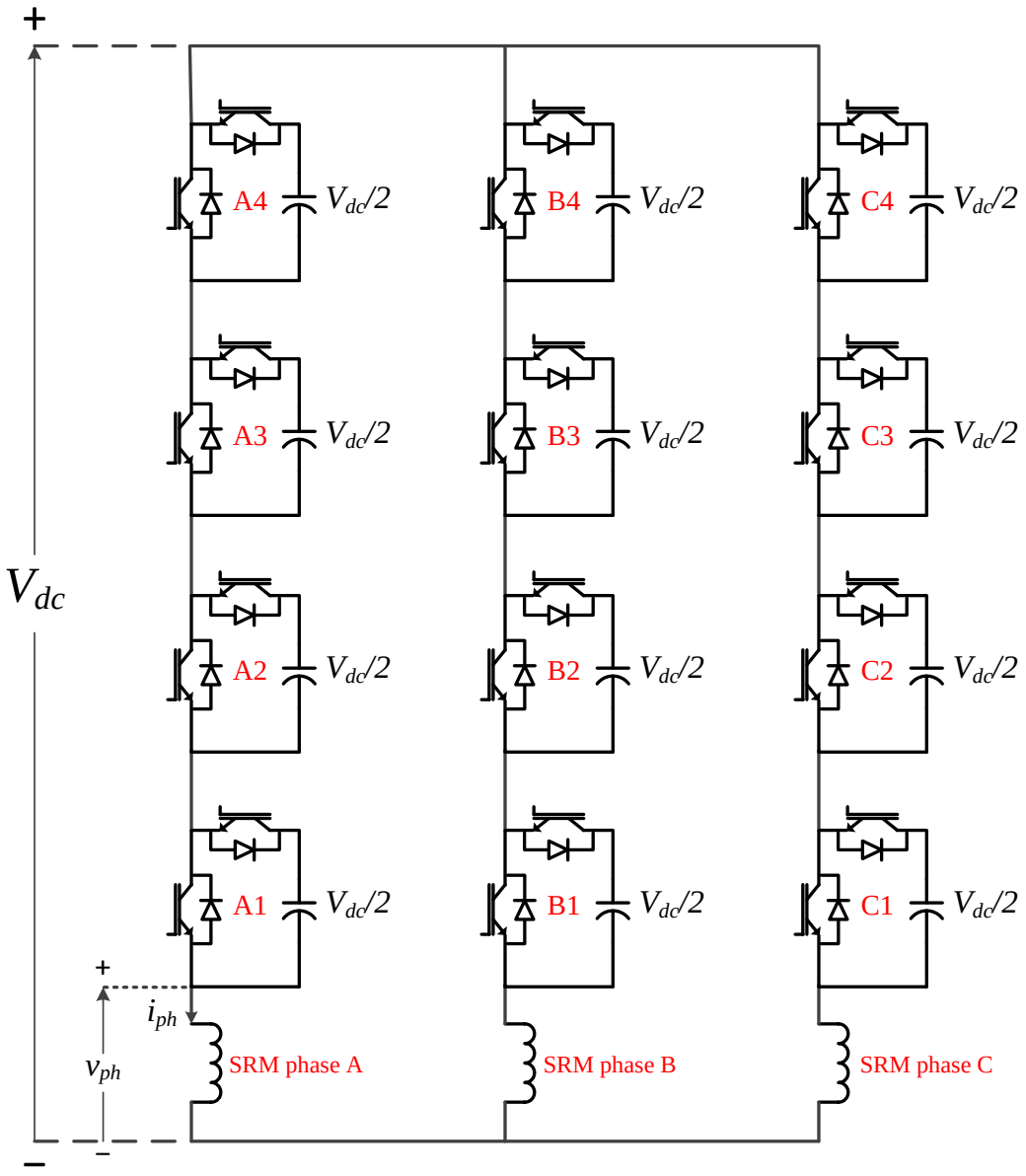


Fig. 3.2 Proposed CCC converter for a 3ph SRM drive (in 4-cell configuration)

Let $v_{cell\text{-}n}$ be the instantaneous voltage across the capacitor of cell n. Below are some basic rules regarding the converter design:

- For every phase leg, the sum of all $v_{cell\text{-}n}$ should be equal to $2V_{dc}$; this allows v_{ph} to vary from $+V_{dc}$ (when all capacitors are bypassed) to $-V_{dc}$ (when all capacitors are conducting current).
- All $v_{cell\text{-}n}$ are controlled to the same voltage, i.e., all $v_{cell\text{-}n}$ are identical (within the control accuracy limits). This largely simplifies the control of the $v_{cell\text{-}n}$, as will be explained in the next chapter.

It follows from rules 1 and 2 that for N cells, the voltage across each cell capacitor is $2V_{dc}/N$. This is evident in equations (2.1) and (2.2) below that summarize rules 1 and 2, respectively.

$$\sum_1^N v_{cell-n} = 2V_{dc} \tag{3.1}$$

$$v_{cell-1} = v_{cell-2} = \cdots = v_{cell-N} = \frac{1}{N}\sum_1^N v_{cell-n} = \frac{2V_{dc}}{N} \tag{3.2}$$

For the 4-cell configuration shown in Fig. 3.2, $N = 4$, and so the voltage across each cell capacitor is $2V_{dc}/4 = V_{dc}/2$. Based on how many capacitors are inserted and how many are bypassed, five different voltage levels for v_{ph} may be synthesized in this 4-cell CCC converter. These voltage levels are $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$. Thus, it may be easily concluded that for an N-cell CCC SRM converter, the number of different voltage levels that can be applied to the SRM phase winding are N+1.

3.3.1 Operating Modes of the CCC Converter

Based on the basic properties of the CCC converter given above, its operating modes may be divided into two categories, depending on the direction of i_{ph}. Operating modes where i_{ph} is positive will be referred to as "P-modes". Likewise, operating modes where i_{ph} is negative will be referred to as "N-modes". Fig. 3.3 illustrates how the five different v_{ph} voltages mentioned above may be synthesized in a given phase for the case when i_{ph} is positive, i.e., during P-mode operation. Fig. 3.4 illustrates the same but for negative i_{ph}, i.e., during N-mode operation. It may be easily noted upon studying Fig. 3.3 and Fig. 3.4 that intermediate voltage levels – meaning those besides $+V_{dc}$ and $-V_{dc}$ – can be produced by more than one combination of switch states. Using number subscripts to denote the cell number (e.g. S_{v1} is the vertical switch in cell 1), Table 2.1 lists all possible (useful) switch combinations for the 4-cell CCC converter. An entry of 1 signifies that a switch is on, and 0 signifies it is off. The last column gives the direction of i_{ph} – and recall from Fig. 3.2 that i_{ph} flowing downwards is considered positive. It is noted that in all P-modes, all S_h switches are always off. Likewise, in all N-modes, all S_v switches are always off. This is simply due to the fact that S_v switches are only used for positive i_{ph} (or P-mode state), while S_h switches are only used for negative i_{ph} (or N-mode state). And since the same i_{ph} flows through all cells, a given phase cannot have some cells in P-mode and others in N-mode at the same time.

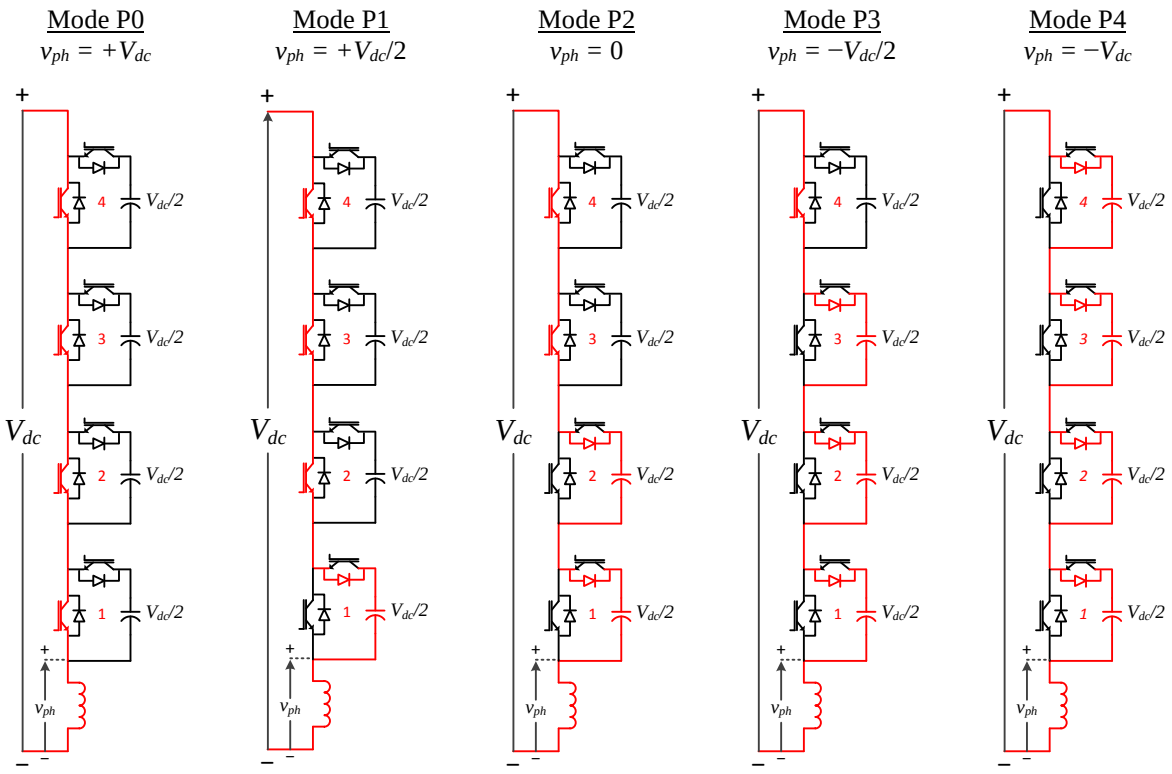


Fig. 3.3 SRM phase voltage levels for the 4-cell CCC converter for positive i_{ph} (P-mode)

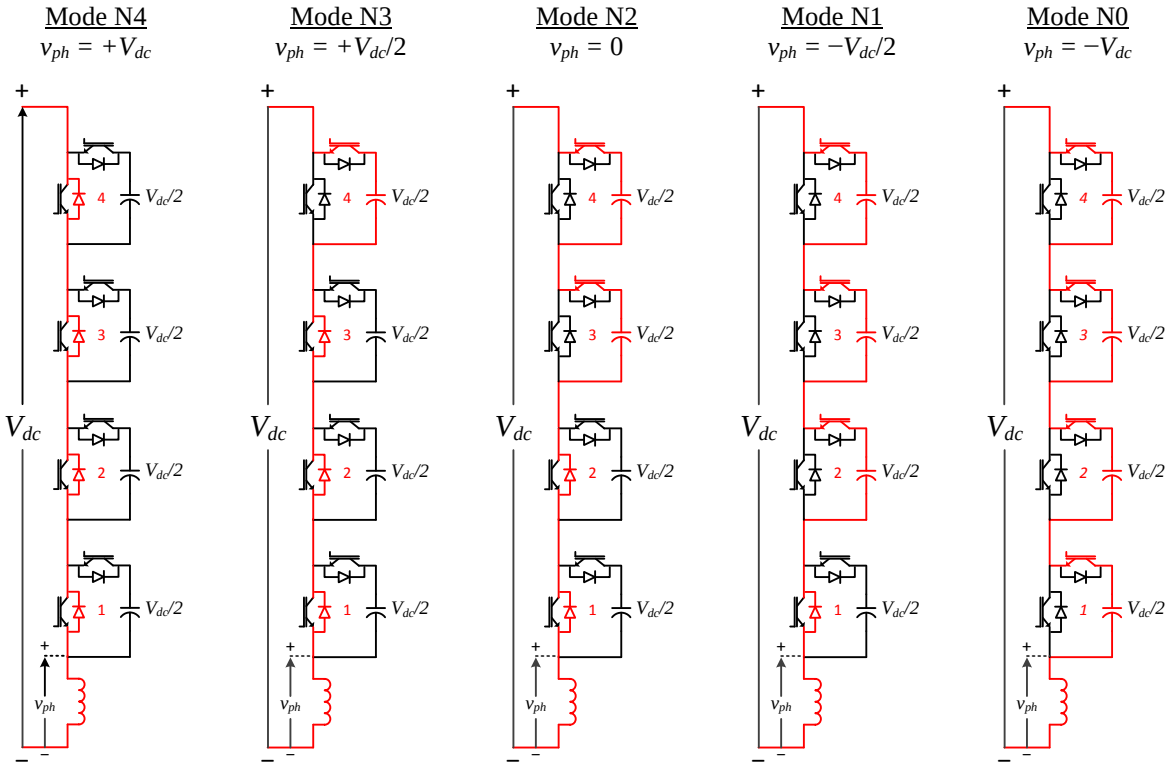


Fig. 3.4 SRM phase voltage levels for the 4-cell CCC converter for negative i_{ph} (N-mode)

TABLE 3.1
CCC CONVERTER OPERATING MODES

Mode	S_{v1}	S_{v2}	S_{v3}	S_{v4}	S_{h1}	S_{h2}	S_{h3}	S_{h4}	v_{ph}	i_{ph}
P0	1	1	1	1	0	0	0	0	$+V_{dc}$	+
P1a	1	1	1	0	0	0	0	0	$+V_{dc}/2$	+
P1b	1	1	0	1	0	0	0	0	$+V_{dc}/2$	+
P1c	1	0	1	1	0	0	0	0	$+V_{dc}/2$	+
P1d	0	1	1	1	0	0	0	0	$+V_{dc}/2$	+
P2a	1	1	0	0	0	0	0	0	0	+
P2b	1	0	1	0	0	0	0	0	0	+
P2c	0	1	1	0	0	0	0	0	0	+
P2d	1	0	0	1	0	0	0	0	0	+
P2e	0	1	0	1	0	0	0	0	0	+
P2f	0	0	1	1	0	0	0	0	0	+
P3a	1	0	0	0	0	0	0	0	$-V_{dc}/2$	+
P3b	0	1	0	0	0	0	0	0	$-V_{dc}/2$	+
P3c	0	0	1	0	0	0	0	0	$-V_{dc}/2$	+
P3d	0	0	0	1	0	0	0	0	$-V_{dc}/2$	+
P4	0	0	0	0	0	0	0	0	$-V_{dc}$	+
N0	0	0	0	0	1	1	1	1	$-V_{dc}$	−
N1a	0	0	0	0	1	1	1	0	$-V_{dc}/2$	−
N1b	0	0	0	0	1	1	0	1	$-V_{dc}/2$	−
N1c	0	0	0	0	1	0	1	1	$-V_{dc}/2$	−
N1d	0	0	0	0	0	1	1	1	$-V_{dc}/2$	−
N2a	0	0	0	0	1	1	0	0	*0*	−
N2b	0	0	0	0	1	0	1	0	*0*	−
N2c	0	0	0	0	0	1	1	0	*0*	−
N2d	0	0	0	0	1	0	0	1	*0*	−
N2e	0	0	0	0	0	1	0	1	*0*	−
N2f	0	0	0	0	0	0	1	1	*0*	−
N3a	0	0	0	0	1	0	0	0	$+V_{dc}/2$	−
N3b	0	0	0	0	0	1	0	0	$+V_{dc}/2$	−
N3c	0	0	0	0	0	0	1	0	$+V_{dc}/2$	−
N3d	0	0	0	0	0	0	0	1	$+V_{dc}/2$	−
N4	0	0	0	0	0	0	0	0	$+V_{dc}$	−

3.3.2 Operation Sequence of the CCC Converter

As explained in chapter 1, a typical stroke in any SRM drive starts with energizing a phase at a specific rotor angle by applying voltage to the phase winding until i_{ph} reaches its commanded value. The controller then switches between the available voltages levels to keep i_{ph} as close as possible to the commanded value. Then at another specified rotor position, the phase is de-energized, typically by applying voltage of polarity opposite to that of the energizing voltage. The turn-on angle, also referred to as the

conduction angle, is denoted θ_{on}. The turn-off angle, also referred to as the commutation angle, is denoted θ_{off}. The de-energization voltage and θ_{off} are chosen so that the phase is completely de-energized before the rotor crosses the stator pole. Otherwise, any current left in the phase winding after the rotor rotates away from perfect alignment with the stator will result in negative torque – effectively pulling back the rotor.

The same operating sequence is applied in the CCC SRM converter. However, it may be easily noted that in the CCC SRM converter the cell capacitors build up charge when i_{ph} is positive, i.e. P-mode. The only exception is in the P0 mode when all cell capacitors are bypassed and full dc link voltage is applied to the phase winding. This is why it is necessary to use N-mode operation as well, since in N-mode (where i_{ph} is negative) cell capacitors lose charge. The only exception in this case is in the N4 mode when all cell capacitors are also bypassed to apply full dc link voltage to the phase winding. A method for controlling and balancing the cell capacitor voltages through judicious alternation of P-modes and N-modes is proposed and explained in the next chapter. It is worth mentioning here that the SRM operation is not affected by the alternation of current polarity, since one of the unique features of reluctance machines is that they are not sensitive to the direction of the current. In other words, they produce the same torque regardless of the direction of i_{ph}. However, the direction of i_{ph} cannot change within one stroke, i.e., only P-modes or only N-modes are allowed within one stroke, and not a mix of both. This is ensured by the controller of the SRM drive.

3.4 Initial Charging of Cell Capacitors

Recall that in an N+1 level CCC converter, the voltage of each cell capacitor needs to be $2V_{dc}/N$. But to prevent overcharging of the capacitors upon startup, the capacitors are only partially charged before startup. However, the sum $\sum_1^N v_{cell-n}$ should not be below V_{dc}, or else uncontrolled flow of current from the source through the horizontal diodes and the machine will occur upon closing the circuit of CCC SRM converter. Therefore the requirement is to charge each cell capacitor to just above 50% of their nominal value, i.e., slightly above V_{dc}/N. A separate low-power source of size $(1+x)V_{dc}/N$, where x may be as low as 0.05 or even lower, may be used for that purpose. This external source should be connected to the positive dc bus terminal and bottom terminal of the last cell, as illustrated in Fig. 3.5. This way the machine windings are bypassed during the charging phase. Fig. 3.5 also shows a discharging circuit, which when connected will allow the capacitors to discharge when needed after the drive is turned off. Two switches are used to complete the charging/discharging circuits. The upper switch is a 3-position switch that puts the drive in either charging mode, discharging mode, or ON mode. The discharging position may be used as the OFF position, or a fourth open position may be used if desired. The lower switch is 2-position only that puts the drive in either charging or discharging mode. Note that the position of the lower switch is of no effect if the upper switch is connected to the dc link for the ON mode.

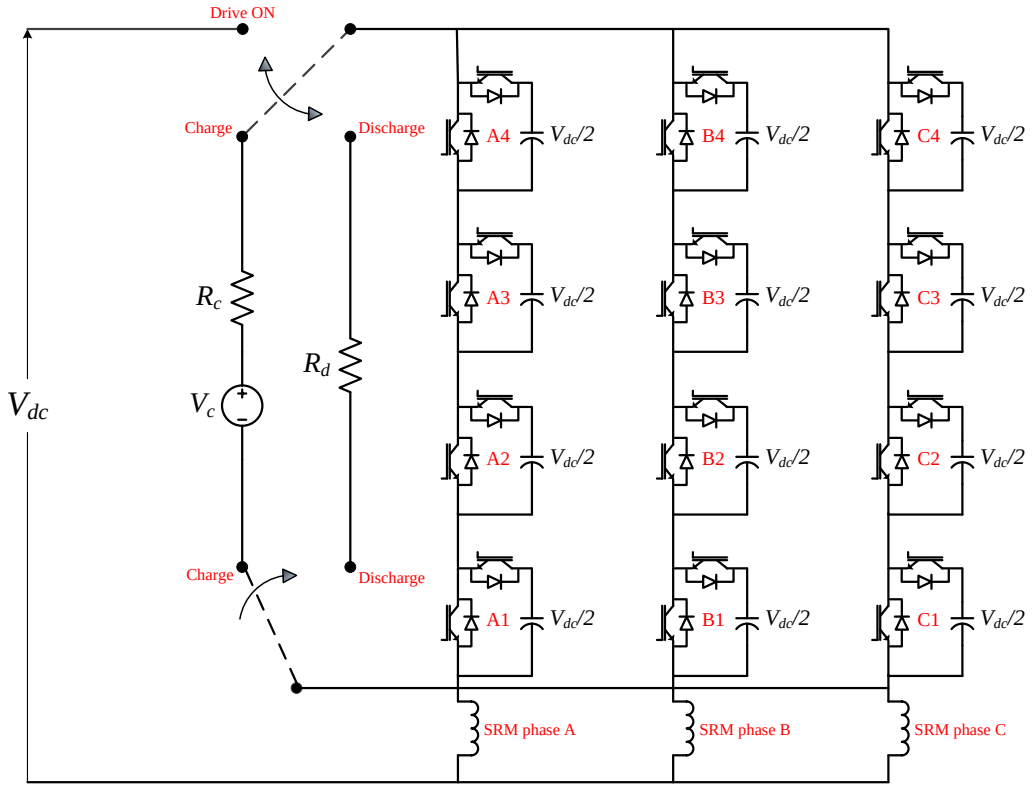


Fig. 3.5 Charging and discharging circuits for the 4-cell CCC converter

For charging, a method similar to the one used in the AC MMC is followed [36], which is to charge one cell at a time by turning on all but one of the switches S_{v1}, S_{v2}… S_{vN}. The cell to be charged should have its S_v switch off, which allows it to charge through its horizontal diode, D_h. When the voltage level of that cell naturally reaches that of the external source, V_c, its S_v switch is triggered on to bypass it, and the S_v switch of the next cell is immediately turned off to allow its capacitor to charge through its own D_h diode, and so on until all capacitors charge. This process may be applied to the three phases simultaneously, i.e., charging one cell from each phase simultaneously, then the next three cells, and so on. Otherwise the cells in one phase may be charged one by one as described above, until all cells in the phase are charged, then the next phase is taken up one cell at a time, and so on. In the latter case, it should be noted that when the charging process is started, current will flow in all three phases for a short period of time regardless of the switch states. This is may be explained as follows. Assume the scenario where it is intended to charge phase A only first. Switches in phases B and C will all be off initially, while in phase A only the cell to receive charge first will have its S_v off, with the S_v switches in the other three cells on. When the switch shown in Fig. 3.5 is put in the charging position, phase A will have current flowing through it, and only the capacitor with its switch S_v off will be charged. But for phase B and C, since all capacitors are at 0 V initially, current will flow from the charging source through the four D_h diodes and their corresponding capacitors until the

total voltage across all four capacitors combined has reached V_c. Only at that stage do the diodes turn off and do phases B and C become controlled.

The initial charging current in each phase is only dependent on V_c and the resistor in the charging circuit, R_c. Therefore, for a given V_c, the desired initial charging current is set by appropriately sizing R_c, so long as that current does not exceed the peak current capability of the charging source. For example, for the CCC SRM converter shown in Fig. 3.5 with V_{dc} = 4000 V and N = 4, let V_c = 1.02 x V_{dc}/N = 1.02 x 4000/4 = 1020 V. If 40 A initial charging current is desired in each phase, then R_c = 1020/40 = 25.5 Ω. A simulation of the charging process with cell capacitor size of 20mF is shown in Fig. 3.6, where all three phases are charged simultaneously. The switch is put in the charging position at t = 0.5 s. The dashed line marks the nominal initial cell voltage level, which is V_c = 1020 V. Also shown is the total charging current, i_c, flowing from the charging source. Each cell takes about 2.35 s to charge to 99% of the desired 1020 V, or 9.4 s for all four cells. This may be sped up by reducing R_c to increase the charging current.

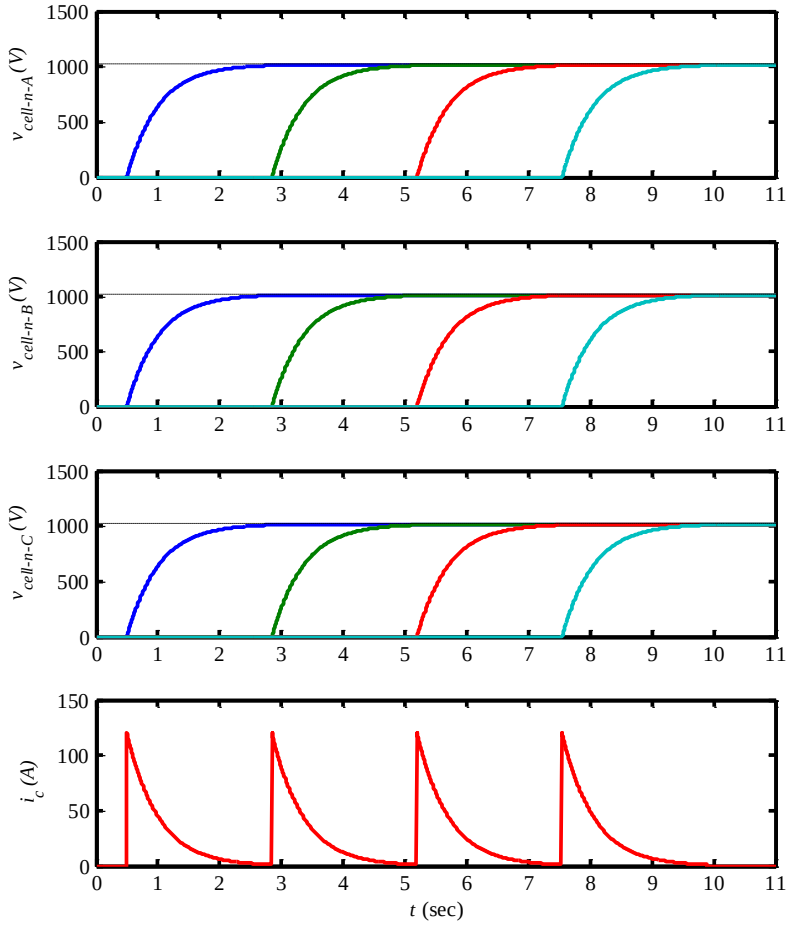


Fig. 3.6 Waveforms for the cell capacitor charging process for a 4-cell SRM CCC converter

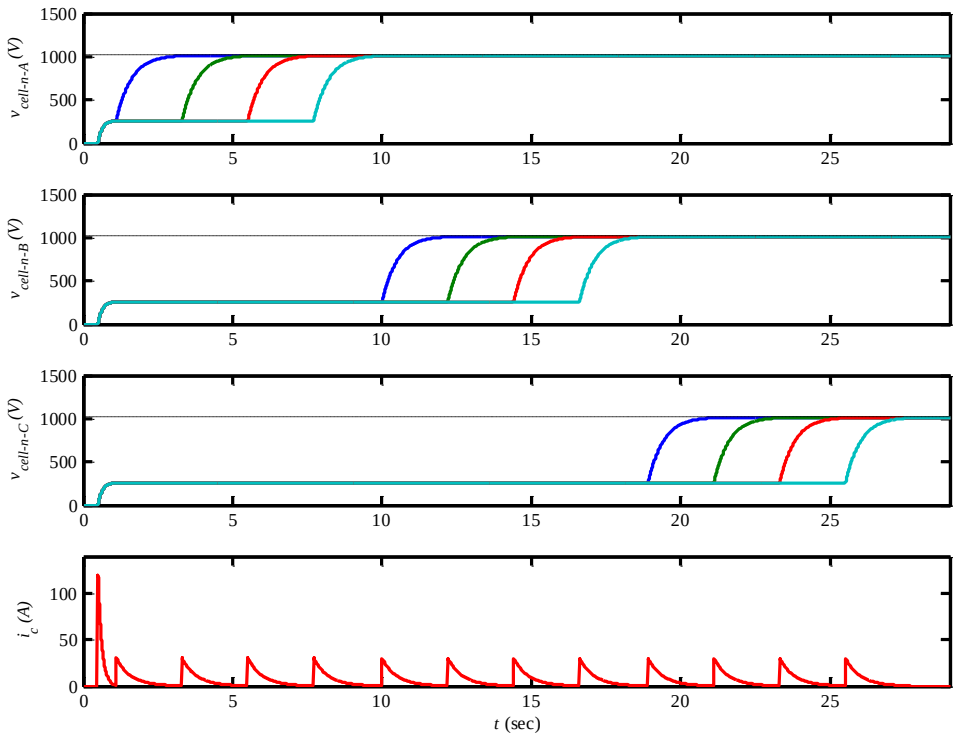


Fig. 3.7 Waveforms for an alternate cell capacitor charging process for a 4-cell SRM CCC converter

The second scenario of charging mentioned above is also simulated but with a slight modification to the sequence. First, the switch put in the charging position at $t = 0.5$ s, but with all semiconductor switches in the off state. All capacitors in all phases will charge through their D_h diodes as mentioned above, but only when the total voltage of all capacitors in each phase equals V_c. This occurs at about $t = 1.1$ s. At that point charging is started in phase A, one cell at a time. Now each cell takes about 2.2 s only to charge since it is already charged to 25% of the desired level. When all cells in phase A are charged, phase B cells are charged one at a time, and then phase C. The complete process takes about 28 s, but uses less current than in the first scenario, except at the initial peak where initial current is the same as in the first scenario. Waveforms for this scenario are shown in Fig. 3.7.

As for discharging, the cell capacitors need not be discharged one at a time. However, discharging one cell at a time limits the discharging current and hence reduces the heat generated across the discharge resistor, R_d, thus requiring a resistor of smaller power rating. Also a useful strategy that may be applied when the drive is braking in preparation to stop, is to lower the $v_{cell\text{-}n}$ from its nominal $2V_{dc}/N$ down to the initial charging voltage of $(1+x)V_{dc}/N$. This may be done at near the zero speed so as it would slow down the braking process if done too early. The $v_{cell\text{-}n}$ hysteresis controller would simply have to shift its band down to the new level. The controller would then force a few more N-mode strokes to discharge the capacitors, until the desired $v_{cell\text{-}n}$ is reached. The advantage of doing so is that about half the energy in the cell capacitors are returned to the source through regenerative braking, as opposed to wasting it in the

discharge resistor. Also, with the $v_{cell\text{-}n}$ at the initial charging level, the drive is ready to be started if it is not to be turned off for a long time. But even if it needs to be discharged, at least only half the energy is dissipated in the discharging process.

3.5 Advantages and Disadvantages of the CCC Converter for SRM

Advantages of the CCC converter that have become apparent so far are summarized below.

- *Scalability to high voltages*: The use of low voltage cells allows for constructing a v_{ph} that can theoretically extend to any voltage level, thereby achieving the main objective of being able to operate at the high voltages demanded by multi-megawatt applications.

- *Redundancy*: By adding redundant cell(s) which may be activated only in case of a fault, the reliability and uptime of the converter are highly improved. The redundant cells may also be used during normal operation, and in case of failure a reduced number of cells is used. More on redundant operation will be covered in chapter 6.

- *Less issues related to transient and dynamic voltages across switches*: The presence of a capacitor in each cell provides the important advantage of defining the voltage of the semiconductor device in that cell. This reduces problems related to voltage balancing among devices, both statically (during the off state) and dynamically (during switching).

- *Homogenous structure:* All cells in the CCC SRM converter are identical in terms of nominal capacitor ratings and semiconductor device ratings. This simplifies operation and control, and is more convenient for manufacturing and maintenance. The AC capacitor-clamped multilevel converter (or its adaptation to SRM drives described in [31]) does not have this advantage. Both switch ratings and capacitor voltage in the AC capacitor-clamped multilevel converter vary from cell to cell when the converter is scaled to more than three levels of line-to-line voltage.

- *No requirement for independent sources*: The CCC converter does not require sources for each cell like the AC cascaded H-bridge converter or its adaptation for SRM drives, the cascaded asymmetric-bridge (CAB) converter described in [31]. The CCC converter uses only capacitors in its cells, and therefore dispenses with the large transformer with many secondary windings used in the CAB converter to provide separate sources for each cell. While this reduces cost, more importantly it simplifies the overall structure hence making scaling of the converter less complex. If a transformer is needed for isolation, a standard 3ph transformer with only three primary and three secondary windings may be used at the input side.

- *Multilevel advantage*: General advantages of multilevel converters are also gained, like reduced EMI, reduced stress on motor winding insulation, and reduced requirement on (and sometimes elimination of) output filters when long cables to the motor are used. Other advantages of multilevel voltages in terms of efficient operation and improved performance are also obtained; this is further explained and verified via simulation in chapters 4 and 5.

- *Avoidance of circulating current issue*: The AC MMC converter described in chapter 1 is a potential candidate for medium-voltage drives due to its easy scalability and reliability. Its phase legs are built from series chopper cells as well, but the three-phase ac connections are tapped off the legs. One consequences of this is the circulating current phenomenon, whereby a current flows through the cells only and not the load. If not properly controlled, the circulating current could increase losses as well as capacitor ripple, thereby requiring oversized switches and capacitors. In the CCC SRM converter, the phase winding is in series with cells, or in other words it is part of the arm. Therefore, no current can bypass the windings and go through the cells only.

- *Independent phases*: The CCC SRM converter maintains the advantage common to most SRM drives, which is independent phase operation. First this allows operation with reduced phases in case of a major fault that requires one of the phases to be temporarily disconnected. Second, if a cell fails in one of the phases, it will have no effect on the other phases. But in the AC CHB or SRM CAB converters, a failed cell must be immediately replaced with a redundant cell, or else a voltage imbalance on the AC primary side of the supplying transformer will occur.

All these advantages of the CCC SRM drive do come at the expense of some undesired but necessary features. The need for capacitive energy storage elements is quite high, which adds to the cost and weight of the drive. However, the gains obtained from this structure like high reliability by virtue of redundancy, is expected to pay off in terms of avoiding failures and downtime which could be very costly. Also the modular structure would also pay dividends in terms of energy savings resulting from improved efficiency, which will be demonstrated in the simulations in chapters 4 and 5. Another disadvantage of the CCC SMR drive is that since it uses both positive and negative phase current, it often returns power to the source. In other words, while on average the power flow is from the source to the drive, the instantaneous dc link current is negative at times. This results in additional losses in the dc link and in the cell capacitors, though both of these are quite small compared to other losses. The constant change in power flow direction may also slightly lower the input-side power factor if not filtered at the dc link.

The next chapter explains the control of the CCC SRM drive and provides simulation results for validation.

Chapter 4

Control and Simulation of the Novel CCC Multilevel Converter for SRM Drives

4.1 Introduction

The previous chapter introduced the concept of the novel cascaded chopper-cell (CCC) converter for SRM drives, and explained its modes of operation. It also covered the initialization of the converter through charging the cell capacitors. Finally, some advantages and disadvantages of the drive were listed. This chapter mainly focuses on the control of the CCC SRM drive, including startup, transient, and steady-state operation. Section 4.2 describes the complete control scheme, with focus on capacitor balancing and control. Section 4.3 proposes a startup algorithm for the safe starting of the drive without the need for additional hardware. Section 4.4 gives a detailed description of the simulation model used. Some design aspects of the drive are also discussed in this section. Section 4.5 provides simulation results, and finally a summary of the chapter is given in section 4.6.

4.2 Control of the CCC Converter for SRM Drives

Fig. 4.1 provides a simplified diagram of the CCC SRM drive control system. It represents the controls for one phase, which is replicated for other phases since each phase is independent.

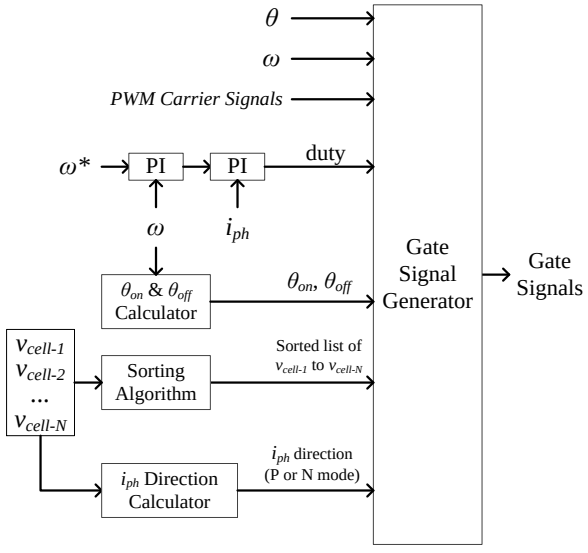


Fig. 4.1 CCC SRM drive control system

As with any high-performance SRM drive, measurement of i_{ph} is required. Also rotor position (θ) and speed (ω) feedback are essential since sensorless operation for the CCC converter has not yet been investigated. Measurement of V_{dc} is not required for control of the motor-side converter but is important for protection purposes, which is especially true in larger drives like the medium-voltage drives that this converter is meant for. The only additional measurement requirement compared to conventional SRM drives is for the cell capacitor voltages, $v_{cell\text{-}n}$. Measurements of the $v_{cell\text{-}n}$ are required both for control as well as fault detection. The following subsections describe the components of the control system.

4.2.1 Cell Capacitor Voltage Balancing and Control

Consider the operation of a single phase and assume steady state operation. Also recall that in a P-mode stroke (where i_{ph} is positive) the $v_{cell\text{-}n}$ increase, while during an N-mode stroke (where i_{ph} is negative) the $v_{cell\text{-}n}$ decrease. In order to keep the $v_{cell\text{-}n}$ from increasing or decreasing indefinitely, it would be intuitive to alternate between P-mode and N-mode strokes. However, it is not difficult to note that due to the nature of the converter's operation, the energy lost by the capacitors during an N-mode stroke is more than the energy gained by the capacitors during a P-mode stroke. This will be explained in more detail with the aid of simulation results in section 4.5. But this means that even with alternating between P-mode and N-mode strokes, over time the $v_{cell\text{-}n}$ will steadily decrease, which is a challenge that has to be overcome. Yet another challenge is to balance the use of different cells in order to avoid a particular cell from being overused which would result in overheating of its devices. Therefore, a comprehensive control scheme that addresses both the balancing and control of the $v_{cell\text{-}n}$, without hindering the operation of the SRM drive, is a requirement for the successful operation of the CCC converter SRM drive. A two-step control method is proposed that satisfies these requirements:

1. *Balancing through sorting*: The $v_{cell\text{-}n}$ are continuously measured, and the measurements are sent to the controller. The controller sorts the cells according to their v_{cell} level. When the direction of i_{ph} is positive (i.e. P-mode stroke, where capacitor charging occurs), capacitors with the lowest voltages are used most. If the direction of i_{ph} is negative (i.e. N-mode stroke, where capacitor discharging occurs), capacitors with the highest voltages are used most. This concept is not new and has been used in the ac MMC converter [36] and perhaps in others. The sorting can be synchronous, where the capacitor sorting order is updated at a fixed frequency. This frequency will be referred to as the sorting frequency, or f_{sort}. f_{sort} is independent of the PWM frequency, f_{pwm}, though it is recommended that f_{sort} does not exceed f_{pwm} so that it remains deterministic as to what the highest switching frequency is. Alternatively the sorting may be asynchronous, where the sorting order is updated at the beginning of each stroke, or more often at lower speeds. A comparison between the two approaches is given in section 4.5 along with other simulation results.

2. *Controlling capacitor voltage through using more P-mode strokes than N-mode*: This simple yet novel algorithm for controlling the $v_{cell\text{-}n}$ is represented by the "i_{ph} Direction Calculator" block shown in Fig. 4.1. First the $v_{cell\text{-}n}$ for each phase are summed, and the sum is fed to a hysteresis controller. Recall that the sum $\sum_1^N v_{cell-n}$ for a given phase needs to be $2V_{dc}$. The hysteresis band is hence centered around $2V_{dc}$, and its limits are set by the user based on acceptable cell capacitor voltage ripple. The output of the hysteresis controller decides the direction of i_{ph}, i.e., whether P-mode or N-mode stroke. To avoid mixing between P-modes and N modes within one stroke, the controller for each phase holds the value of the i_{ph} direction throughout the stroke duration, and updates it only a few degrees ahead of θ_{on} of the next stroke.

4.2.2 Speed and Current Control

At a basic level, speed and current control may be achieved with standard PI controllers. For applications operating primarily at one speed, the PI current controller may be just tuned for acceptable performance at that speed. But for drives that operate often at multiple speeds, adaptive or scheduled gains can be used to enhance performance. Alternatively, multiband hysteresis methods similar to those proposed for ac multilevel converters [42] may be adapted and used. Going back to the PI method, the duty cycle output from the PI current controller is compared against stacked PWM carrier signals, much like in many AC multilevel converters. Example PWM carriers suitable for the 4-cell converter discussed in the previous chapter are shown in Fig. 4.2. The corresponding controller action for different duty values is given in Table 4.1.

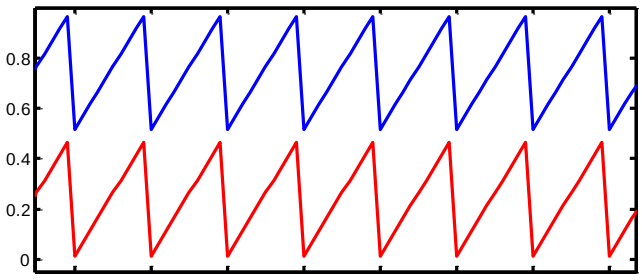


Fig. 4.2 PWM Carriers for 4-level CCC converter

TABLE 4.1
OPERATING MODE CHOICE DURING PWM MODULATION

Duty	**P-mode Stroke**		**N-mode Stroke**	
0	$v_{ph} = 0$	Any P2 mode	$v_{ph} = 0$	Any N2 mode
(0,0.5]	$v_{ph} = +V_{dc}/2$	Any P1 mode	$v_{ph} = -V_{dc}/2$	Any N1 mode
(0.5,1]	$v_{ph} = +V_{dc}$	P0 mode	$v_{ph} = -V_{dc}$	N0 mode

The following simple rules are followed in constructing the PWM signals, and they apply to a CCC converter of any size:

1. The number of PWM carriers is equal to the number of levels that are to be used during current chopping (excluding the zero voltage level).

2. If chopping uses v_{ph} of only one polarity, the PWM carriers are limited between 0 and 1, and so would be the duty output from the current controller. But if it is desired that some or all voltage levels of the opposite polarity be used during chopping, then more PWM carriers may be added in the 0 to −1 range. For example, if chopping only uses $+V_{dc}$, $+V_{dc}/2$, and 0 in P-mode, and only $-V_{dc}$, $-V_{dc}/2$, and 0 in N-mode, then only two stacked carriers in the range 0 to 1 suffice as shown in Fig. 4.2. But if for instance chopping uses $+V_{dc}$, $+V_{dc}/2$, 0, and $-V_{dc}/2$ in P-mode, and uses $-V_{dc}$, $-V_{dc}/2$, 0, and $+V_{dc}/2$ in N-mode, then an additional carrier should be added with limits −0.5 to 0.

4.2.3 Startup Scheme for the CCC SRM Drive

It is common for startup currents in low power machines to reach several times the rated current. However, in large machines that may not be tolerated or desired, and hence safe startup techniques are required. The startup scheme must limit both peak current as well as the switching frequency. A high instantaneous current can damage the switches, and so can the high device temperatures that result from a high switching frequency. The individual $v_{cell\text{-}n}$ must also be prevented from rising significantly during startup, or else the cell capacitors would need to be significantly oversized, thereby unduly increasing system cost. A startup scheme is proposed here that limits both current and switching frequency to a sufficiently low level, while keeping the individual $v_{cell\text{-}n}$ within acceptable limits. The scheme is based on the following:

- A hard limit is put on the maximum current by using a hysteresis current controller during startup rather than PWM modulation.

- A wide band is used for the current hysteresis controller in order to reduce the switching frequency. But a too wide a band should be avoided, as it will result in a large increase in the cell capacitor voltage, as well as an unnecessarily large torque ripple.

- Only the current controller is activated on startup, and a low reference current is commanded that is just enough to overcome inertia and friction and start the drive. A low initial current will produce low torque and hence slow acceleration initially, but this is seldom an issue for large drives, including those for the target applications like large compressor drives or large fans and blowers. But if desired, the initial current may be increased as long as the three constraints

mentioned earlier are not breached, which are: device peak current limit, device thermal limit, and capacitor voltage limit. Of course a safe margin must be maintained in all of these.

- Since the switching frequency is not controlled, it needs to be limited to its minimum possible. This is achieved through minimizing the magnitude of the energization and de-energization voltages used during the current chopping phase, which allows i_{ph} to rise and decay slowly, thereby limiting the switching frequency. But since the $v_{cell\text{-}n}$ are continuously changing during startup, the controller needs to choose the appropriate ON and OFF chopping voltages at different times.

- Cell capacitors are only partially charged prior to startup, to allow for some rise in the individual $v_{cell\text{-}n}$ without going much over their nominal value of $2V_{dc}/N$.

A list of the practical steps for the startup scheme follows:

1. The CCC converter is started with a P-mode rather than an N-mode stroke, meaning that i_{ph} is positive. Thus, the cell capacitors will charge during the current chopping phase of the first stroke.

2. Since the cell capacitors are initially charged to slightly above 50% of their nominal voltage and that their voltages will be continuously changing, the v_{ph} voltage levels will not be as listed in Table 3.1 in the previous chapter. v_{ph} is rather synthesized according to the following criteria (only temporarily for the duration of the startup process):

   - *For a P-mode stroke*: When i_{ph} is below the lower hysteresis band limit, v_{ph} is set to the lowest available positive voltage (though above a specified minimum, e.g. $+0.25V_{dc}$) to energize the phase. And when i_{ph} is above the upper hysteresis band limit, v_{ph} is set to the smallest available negative voltage (i.e. closest to zero). In the latter case, even v_{ph} = 0 V would work since the cell capacitors charge up during P-mode, and so as they're inserted against the V_{dc} bus voltage they will only make v_{ph} more negative rather than make it rise above 0 V.

   - *For an N-mode stroke*: When the (magnitude of) i_{ph} is below the lower hysteresis band limit, v_{ph} is set to the negative voltage with the smallest available magnitude above a specified minimum (e.g. $-0.25V_{dc}$). And when (the magnitude of) i_{ph} is above the upper hysteresis band limit, v_{ph} is set to the smallest positive voltage. Even if that v_{ph} was 0 V initially, as the capacitors only discharge during N-mode, and hence v_{ph} would only become more positive rather than fall below 0 V.

3. Once the machine reaches a few percent of its rated speed and the $v_{cell\text{-}n}$ are within the commanded limits and remain controlled, regular speed and current control may be applied.

TABLE 4.2
CRITERIA FOR SYNTHESIZING v_{ph} DURING CHOPPING STAGE OF FIRST (P-MODE) STROKE

i_{ph}	Action Required	$\sum_1^N v_{cell-n}$ (V)	$\min_t(v_{cell})$ (V)	$\max_t(v_{cell})$ (V)	# of caps to insert	$\min_t\lvert v_{ph}\rvert$ (V)	$\max_t\lvert v_{ph}\rvert$ (V)
Less than lower hysteresis band limit	Apply +ve v_{ph} to increase i_{ph}	[4200, 6000)	1050	1500	2	+1000	+1900
Less than lower hysteresis band limit	Apply +ve v_{ph} to increase i_{ph}	[6000,12000)	1500	3000	1	+1000	+2500
Less than lower hysteresis band limit	Apply +ve v_{ph} to increase i_{ph}	>=12000	3000	unlikely and undesirable to reach >3000	0	+4000	+4000
Higher than upper hysteresis band limit	Apply −ve v_{ph} to decrease i_{ph}	[4200, 5336)	1050	1334	4	−200	−1336
Higher than upper hysteresis band limit	Apply −ve v_{ph} to decrease i_{ph}	[5336, 8000)	1334	2000	3	−2	−2000
Higher than upper hysteresis band limit	Apply −ve v_{ph} to decrease i_{ph}	[8000, 16000)	2000	4000	2	0	−4000
Higher than upper hysteresis band limit	Apply −ve v_{ph} to decrease i_{ph}	>=16000	4000		1	0	

Taking the example of the 4-cell CCC converter described in the previous chapter, and assuming V_{dc} is 4000 V and that the initial $v_{cell\text{-}n}$ are 1050 V (i.e. 52.5% of their nominal value), Table 4.2 provides an example of voltage choices during the first stroke – which as mentioned earlier is chosen to be a P-mode stroke. $\sum_1^N v_{cell-n}$ is the sum of all cell capacitor voltages, while $\min_t(v_{cell})$ and $\max_t(v_{cell})$ are the minimum and maximum average individual cell capacitor voltage. $\min_t\lvert v_{ph}\rvert$ and $\max_t\lvert v_{ph}\rvert$ are the minimum and maximum phase voltages resulting from the insertion of the suggested number of capacitors.

The first three rows are for the case where i_{ph} falls below the lower hysteresis band limit, while the last four rows are for the case when i_{ph} rises above the upper hysteresis band limit. The decision on which voltage to apply is based on the sum $\sum_1^N v_{cell-n}$ rather than the individual $v_{cell\text{-}n}$, since the latter tend to vary from each other, but they're close enough to assume that they are identical. Below is a detailed description of each row of Table 4.2. It should be kept in mind that throughout this process the sorting algorithm alternates between the cell capacitors, at a rate given by the sorting frequency, to keep the $v_{cell\text{-}n}$ balanced.

Row 1: Starting from zero speed and with each $v_{cell\text{-}n}$ at 1050 V, two capacitors are inserted against the dc bus voltage of 4000 V. This results in an initial v_{ph} of 1900 V. But as the $v_{cell\text{-}n}$ become more positive, v_{ph} drops, and as mentioned above the controller will only allow v_{ph} to drop to a certain level. Consider that this level is $0.25V_{dc}$ = 1000 V. When v_{ph} = 1000 V the controller changes the number of inserted capacitors.

Row 2: When each cell capacitor has charged from the initial 1050 V to 1500 V, meaning that v_{ph} has become 1000 V, the controller switches to inserting only one capacitor to prevent the energization voltage from being too low to meet the current demand. This takes v_{ph} back up to 2500 V, but again as the $v_{cell\text{-}n}$ increase v_{ph} continues to drop.

Row 3: In the unlikely case that each $v_{cell\text{-}n}$ exceeds 3000 V each, for example due to very high current demand, then no capacitor is inserted, taking v_{ph} from 1000 V back up to 4000 V. This prevents further increase in the $v_{cell\text{-}n}$, and also ensures a high enough energization voltage. However, the switching frequency may increase at this stage, but the design should be such that this stage does not last long before the first stroke has ended. It is highly preferable that the $v_{cell\text{-}n}$ do not increase to more than 3000 V, which is150% of their nominal value of 2000 V. Otherwise the capacitors may have to be oversized. Choosing the appropriate capacitance and voltage rating is a design decision that depends on many factors including cost, size, and available voltage ratings of the capacitors, all of which depend on the capacitor technology used. More on this will be discussed in chapter 4 on practical considerations.

Row 4: Every time i_{ph} rises above the upper hysteresis band limit, a zero or negative v_{ph} is commanded to control it. With the $v_{cell\text{-}n}$ at 1050 V initially, all four capacitors are inserted against the 4000 V dc bus voltage. Since the sum $\sum_1^N v_{cell-n}$ is 4200 V initially, the resultant v_{ph} is −200 V, which is the closest possible to zero that can be obtained at that stage. When each $v_{cell\text{-}n}$ has risen to about 1334 V, which is the minimum that enables three capacitors to be inserted and generate a zero or negative v_{ph}, the controller switches to inserting only three capacitors as opposed to four.

Row 5: With three capacitor inserted, each at 1334 V, the initial de-energization v_{ph} is −2 V. This becomes more negative though as the $v_{cell\text{-}n}$ increase, until each of the cell $v_{cell\text{-}n}$ is about 2000 V.

Rows 6 and 7: When each $v_{cell\text{-}n}$ is about 2000 V, two capacitors only are inserted to set v_{ph} to 0 V. It is highly unlikely that the $v_{cell\text{-}n}$ would rise above 4000 V each, but if they do then only one capacitor is inserted.

It should be noted that the "i_{ph} direction calculator" block is enabled right from the startup. Given the expected rise in the $v_{cell\text{-}n}$ in the first P-mode stroke, it is almost sure that the second stroke will be N-mode. In N-mode energization happens with a negative voltage, and capacitors only discharge rather than charge. Table 4.3 provides an example of voltage choices for the second stroke assuming that it is N-mode.

Row 1: In N-mode, and with reference to Table 4.3, initially only a single capacitor is used if each $v_{cell\text{-}n}$ has risen above 5000 V in the P-mode stroke. Of course it is highly undesirable for the $v_{cell\text{-}n}$ to rise to this value, and typically the control design should aim for a value of 1.5 to two times the nominal. In any

case this scenario is included for completeness. Using one cell capacitor initially against the dc bus voltage of 4000 V will result in an initial energization voltage is v_{ph} = −1000 V.

TABLE 4.3
CRITERIA FOR SYNTHESIZING v_{ph} DURING CHOPPING STAGE OF SECOND (N-MODE) STROKE

$\lvert i_{ph}\rvert$	Action Required	$\sum_1^N v_{cell-n}$	$\min_t(v_{cell})$	$\max_t(v_{cell})$	# of caps to insert	$\min_t\lvert v_{ph}\rvert$	$\max_t\lvert v_{ph}\rvert$
Less than lower hysteresis band limit	Apply −ve v_{ph} to increase $\lvert i_{ph}\rvert$	>=20000	5000		1	-1000	
Less than lower hysteresis band limit	Apply −ve v_{ph} to increase $\lvert i_{ph}\rvert$	(20000,10000]	2500	5000	2	−1000	−6000
Less than lower hysteresis band limit	Apply −ve v_{ph} to increase $\lvert i_{ph}\rvert$	(10000,6668]	1667	2500	3	−1001	−3500
Less than lower hysteresis band limit	Apply −ve v_{ph} to increase $\lvert i_{ph}\rvert$	(6668,5000]	1250	1667	4	−1000	−2668
Higher than upper hysteresis band limit	Apply +ve v_{ph} to decrease $\lvert i_{ph}\rvert$	>=16000	4000		0	+4000	+4000
Higher than upper hysteresis band limit	Apply +ve v_{ph} to decrease $\lvert i_{ph}\rvert$	(16000, 8000]	2000	4000	1	0	+2000
Higher than upper hysteresis band limit	Apply +ve v_{ph} to decrease $\lvert i_{ph}\rvert$	(8000, 5332]	1333	2000	2	0	+1334
Higher than upper hysteresis band limit	Apply +ve v_{ph} to decrease $\lvert i_{ph}\rvert$	(5332, 5000]	1250	1333	3	+1	+250

Row 2: Below 5000 V per v_{cell-n} down to 2500 V per v_{cell-n}, two capacitors are used. This will provide a maximum energization voltage of v_{ph} = −6000 V for 5000 V per v_{cell-n}, and a minimum energization voltage of v_{ph} = −1000 V for 2500 V per v_{cell-n}. When each v_{cell-n} has fallen below 2500 V, three cell capacitors are used for energization, as given in row 3.

Row 3: Assuming each v_{cell-n} is 2500 initially, the energization voltage is v_{ph} = −3500 V with three cell capacitors inserted. When each v_{cell-n} has discharged down to 1667 V, the energization voltage decreases (in magnitude) to become v_{ph} = −1001 V. At that point all four capacitors are inserted as in row 4.

Row 4: When the v_{cell-n} have dropped to 1667 V each, v_{ph} becomes −1001 V. At that point the fourth capacitor is inserted to make v_{ph} = −2668 V. Then when the v_{cell-n} have dropped to 1250 V each, v_{ph} would be −1000 V. It is not expected that the v_{cell-n} would drop below 1250 V each in the second stroke, but even if it does, no further action is required as there are no more than four capacitors to insert. The v_{cell-n} may continue to decrease until their sum is 4000 V. The control and converter design stage should ensure that the individual v_{cell-n} do not come too close to this minimum of 1000 V per cell.

Row 5: When $|i_{ph}|$ rises above the upper hysteresis band limit in an N-mode stroke, a zero or positive v_{ph} is commanded to control it. The goal is to synthesize a v_{ph} that is as close to 0 V as possible in order to reduce the switching frequency. Again for completeness an unlikely worst-case $v_{cell\text{-}n}$ of more than 4000 V per cell is assumed at the start of the N-mode stroke. At that stage no capacitors should be inserted, since inserting any capacitor would only contribute to increasing the current. With no capacitors inserted, the demagnetization voltage is v_{ph} = +4000 V.

Row 6: For anywhere between 4000 V and 2000 V per cell, one capacitor may be inserted. This translates to a v_{ph} of 0 V for 4000 V per $v_{cell\text{-}n}$, up to a v_{ph} of +2000 V for 2000 V per $v_{cell\text{-}n}$. v_{ph} = +2000 V is in fact quite high and will result in a higher switching rate. However, a second capacitors may not be inserted until each $v_{cell\text{-}n}$ is around 2000 V, or else a negative v_{ph} would be produced which would make the current increase rather than decrease.

Row 7: When each $v_{cell\text{-}n}$ discharges to around 2000 V, two capacitors may be inserted. This immediately reduces v_{ph} to 0 V, and that can continue until each $v_{cell\text{-}n}$ have fallen to around 1333 V. At that point it is possible to insert three capacitors and yet obtain a positive v_{ph}.

Row 8: Three capacitors are inserted when each $v_{cell\text{-}n}$ is about 1333 V, which sets the de-energization voltage v_{ph} to +1 V. But v_{ph} would increase to +250 V as the cell capacitors further discharge to 1250 V each.

Though it is unlikely that the $v_{cell\text{-}n}$ would drop below 1250 V each in the second stroke, there is no harm if they do; four capacitors can then be inserted to set v_{ph} to +1000 V which would approach 0 V when each $v_{cell\text{-}n}$ approach 1000 V – which is even more unlikely. Again it should be kept in mind that through this process the sorting algorithm is active and it alternates between the cell capacitors (at a rate given by the sorting frequency) to keep the $v_{cell\text{-}n}$ balanced. Also as mentioned above the control design should limit the chances of the $v_{cell\text{-}n}$ dropping too low or rising too high. Waveforms from simulation using the tables above will be provided in section 4.5 on simulation results.

4.3 CCC SRM Drive Design and Specifications

An SRM model based on the 2-MW SRM design in [14] is used for simulation. This 2-MW SRM has a 6/4 configuration, as depicted in Fig. 4.3; its electrical/mechanical ratings are given in Table 4.4. The SRM is driven with a 4-cell per phase CCC converter described in chapter 3. And since N = 4 cells, the nominal cell capacitor voltage, $v_{cell\text{-}n}$, is 2000 V. A stiff dc link of V_{dc} = 4000 V is assumed for the simulations. Options for the front-end converter are not discussed in this chapter, but are covered in chapter 6 along with other practical considerations.

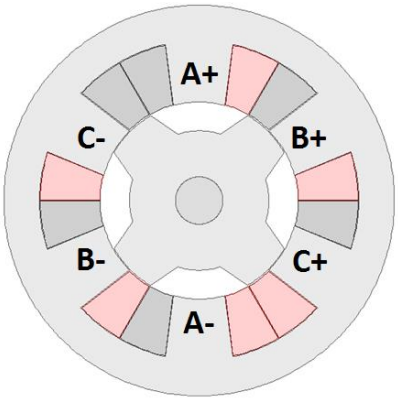


Fig. 4.3 Cross-sectional view of the 6/4 SRM used in the simulations

TABLE 4.4
RATINGS OF THE 2-MW SRM USED IN THE SIMULATIONS

Rated Power	1880 kW	Approx. Stator Resistance @ 115°C	20 mΩ
Rated Voltage	4000 V	Unaligned Inductance	0.936 mH
Rated Current	487 A	Aligned Inductance at rated current	4.4 mH
Rated Speed	16790 r/min	Inertia Coefficient (including load)	30 kg·m^2
Rated Torque	1069 N·m	Friction Coefficient (including load)	0.0061 N·m·rad^{-1}·s^{-1}

4.3.1 Sizing of Cell Capacitors

Since the CCC converter uses several capacitors that are switched in and out at a rate dictated by the frequency of the $v_{cell\text{-}n}$ sorting algorithm, and since the P-mode and N-mode strokes are judiciously used to keep the $v_{cell\text{-}n}$ within the user-specified range, deviation of the $v_{cell\text{-}n}$ form their nominal value is kept to a minimum. In fact, most fluctuation is experienced at startup, and specifically during the first stroke which has the longest duration of all strokes. The cell capacitors are therefore sized to withstand this initial voltage rise. But the steady-state ripple will also be discussed in section 4.5 on simulations.

An analytic expression for the change in $v_{cell\text{-}n}$ is the starting point in sizing the cell capacitance, C, which is identical for all cells. Let the initial voltage of cell n be $v_{cell\text{-}n\text{-}init}$, and its voltage at the end of the first stroke $v_{cell\text{-}n\text{-}max}$ – and note that the latter is given the subscript *max* since as mentioned above it is expected to be the highest value any $v_{cell\text{-}n}$ would reach up until rated speed. And let $i_{cell\text{-}n}$ be the current passing through the cell capacitor. Also let T_{cond} be the duration of current conduction in the first excited phase – i.e. from the time i_{ph} rises from zero up until it drops to zero again. Considering only the first stroke through the first phase that is energized, the following general expression may be written:

$$v_{cell-n-max} = v_{cell-n-init} + \frac{1}{C}\int_0^{T_{cond}} i_{cell}\,dt \tag{4.1}$$

Let the average of i_{cell} over the period T_{cond} be denoted by I_{cell}. Defining $\Delta v_{cell\text{-}n} = v_{cell\text{-}n\text{-}max} - v_{cell\text{-}n\text{-}init}$, (4.1) can be rearranged as follows:

$$C = \frac{T_{cond}\overline{i_{ph}}}{\Delta v_{cell-n}} \tag{4.2}$$

$\Delta v_{cell\text{-}n}$, which is a direct measure of the rise in the cell capacitor voltage during startup, is specified by the user and is the main criteria for sizing C. But is it is not easy to determine analytic expressions for I_{cell} and T_{cond} because of the high non-linearity of the SRM. In general though, I_{cell} is inversely proportional to T_{cond}; increasing I_{cell} increases the drive's acceleration by producing more torque thereby shortening T_{cond}, while decreasing I_{cell} has the opposite effect. However, the product $T_{cond}.I_{cell}$ is difficult to quantify without the aid of a simulation tool, and so an initial sizing of C is best obtained with the help of simulation. A suggested procedure for sizing C as well as for choosing an appropriate current command, i_{ph}^*, is given below:

1. Initial values for i_{ph}^* and C are chosen, and recall that during the startup procedure i_{ph}^* is fixed rather than being computed by the speed controller. A simulation from startup using these initial i_{ph}^* and C is performed, with all the measures mentioned above applied. These the measures briefly are: 1) start with a P-mode stroke, 2) use a small i_{ph}^* during startup (for example no more than half the rated current), 3) use a wide hysteresis band for the current controller (at least 50% on either side), 4) have the $v_{cell\text{-}n}$ at 52.5% of their nominal value, and 5) use Tables 4.2 and 4.3 to synthesize the appropriate v_{ph}.

2. Next, based on the simulation results from step 1, the i_{ph} command is tuned to achieve the minimum desired acceleration (measured over the first few strokes). Note that the acceleration can be increased gradually after the startup stage.

3. With i_{ph}^* set, the value of C is then adjusted to obtain the desired $v_{cell\text{-}n\text{-}max}$, the maximum cell capacitor voltage at the end of the first stroke. Modifying C is not expected to affect the acceleration – this is investigated later in section 4.4.

4. A final tuning step involving the i_{ph} hysteresis band may be performed. The advantages of using a smaller hysteresis band are reduced torque ripple and a slightly increased acceleration. The disadvantages are increased switching frequency and a slight increase in $v_{cell\text{-}n\text{-}max}$. Therefore, care should be taken not to use too small a band, as maintaining acceptable switching losses and limiting $v_{cell\text{-}n\text{-}max}$ are critical goals during the startup phase, whereas the low torque ripple and fast acceleration are not essential during startup for most multi-megawatt applications.

The procedure above was implemented in simulation. The details of the simulation model used for all simulations in this work is explained in section 4.4. For now only brief results for startup are provided for the purpose of sizing *C*. Even though it is expected that this startup procedure will result in highly reduced semiconductor losses, a thermal component should nevertheless be included in simulation to estimate semiconductor device temperatures and make sure they remain well below their safe maximum. The turn on or conduction angle (θ_{on}) was set to 11° for startup, while the commutation angle (θ_{off}) was set to 41°. This results in a dwell angle of $\theta_{off} - \theta_{on} = 30°$ for each phase. For a three-phase SRM, a 30° dwell angle ensures continuity of torque, which is important at startup since the machine has less inertia. It is also assumed in the startup simulation that the first phase happens to be right at 11°, and so the first P-mode stroke will last the full 30°. This represents the worst case for $v_{cell\text{-}n\text{-}max}$.

TABLE 4.5
SIMULATION RESULTS FOR THE STARTUP PHASE OF THE CCC SRM DRIVE

	C (mF)	i_{ph}^* (A)	Hysteresis band (A)	$v_{cell\text{-}n\text{-}max}$ (V)	T_{cond} (s)	ω at 1s (r/min)	Conduction losses in W (1st stroke)	Switching losses in W (1st stroke)	Max. $T_{junction}$ in °C up to 1% ω_{rated}
Varying i_{ph} command	20	150	±100	2669	0.442	59.61	821	1443	33.94
	20	200	±100	2742	0.345	98.21	1232	2195	35.20
	20	300	±100	2877	0.244	201.60	2206	4216	43.95
Varying C	11	150	±100	3471	0.442	60.20	836	2046	34.58
	8.2	150	±100	3973	0.440	60.17	846	3269	38.71
Varying i_{ph} hysteresis band	20	150	±50	2751	0.440	65.75	904	2752	39.04

Table 4.5 provides a summary of the startup simulation results, showing the effect of varying each of *C*, i_{ph}^*, and the hysteresis band. ω is the instantaneous speed of the drive, while ω_{rated} is the rated speed. The conduction and switching losses given in the table are the average of the losses taken over the period of T_{cond} only.

In all cases the temperature is well controlled. A common heat sink was assumed for both devices in one cell. The thermal resistance from the device case to ambient, which is the sum of the thermal resistance from device case to heat sink, then heat sink to ambient, was set to 0.1 K/W. The thermal capacitance on the other hand was set to 1 J/K. The ambient temperature was assumed 25°C. The most sensitive figure in Table 4.5 is the $v_{cell\text{-}n\text{-}max}$. The lowest obtained $v_{cell\text{-}n\text{-}max}$ was 2669 V, which is 669 V above the nominal cell capacitor voltage. It will be shown later in section 4.5 on simulations how shifting θ_{on} and

θ_{off}, as well as starting the machine from the fully aligned position, can further reduce the $v_{cell\text{-}n\text{-}max}$ by an appreciable amount. Trends noted form the results in Table 4.5 are explained below:

- *Varying i_{ph} command:* It is seen from Table 4.5 that increasing i_{ph}^* increases acceleration and also results in a slight increase in $v_{cell\text{-}n\text{-}max}$. However, more importantly, it increases conduction and switching losses. This should be carefully considered when choosing i_{ph}^* command for startup.

- *Varying cell capacitor size:* Using an 11 μF cell capacitor as opposed to 20 μF significantly increases $v_{cell\text{-}n\text{-}max}$. This will necessitate increasing the cell capacitor voltage rating, and so there is a tradeoff between capacitance and voltage rating. A discussion on this is included in chapter 4 on practical considerations. Also faster fluctuations of the $v_{cell\text{-}n}$ occur with smaller capacitance, which results in more frequent sorting (up to the sorting frequency limit) and hence increases switching losses. The increase in switching losses is only slight going from 20 mF to 11 mF, but going below that results in a noticeable increase in switching losses and hence higher device temperatures. Finally, note that as expected the acceleration is barely affected by changing *C*. This is because acceleration is mainly dependent on torque which is mainly dependent on i_{ph}, and that in turn follows i_{ph}^*.

- *Varying i_{ph} hysteresis band:* As mentioned in section 4.2.3, a large hysteresis band is recommended, mainly to reduce switching losses and thus keep the device temperatures from rising too high. Comparing the results for a ±100 A i_{ph} hysteresis band (first row in Table 4.5) and a ±50 A i_{ph} hysteresis band (last row in Table 4.5) show that the latter results in a slightly increase in $v_{cell\text{-}n\text{-}max}$, as well as slightly higher acceleration. Also not shown in the table, the torque ripple will be significantly lower, since torque is proportional to the square of the current in an SRM. But the semiconductor losses and hence temperature rise somewhat noticeably. Therefore it is highly recommended that the drive starts with maximum acceptable torque ripple such that a wide enough hysteresis band may be accommodated, thereby resulting in less losses.

4.3.2 Cell Capacitor Voltage Balancing and Control Parameters

For the control of the $v_{cell\text{-}n}$, the hysteresis controller of the "i_{ph} Direction Calculator" block of Fig. 4.1 is set to control the sum $\sum_1^N v_{cell-n}$ to ±1% ripple. Therefore, each cell capacitor will also have ±1% ripple, i.e. each $v_{cell\text{-}n}$ will fluctuate between 1980V and 2020V (at steady state). The hysteresis band may also be replaced with a single line; more on this will be covered in section 4.5 in light of the simulation results.

As for balancing the $v_{cell\text{-}n}$, the sorting frequency explained in section 4.2.1 is set to 500 Hz. This is a very realistic and rather conservative choice for today's devices. A commercial medium-voltage high-

current IGBT module from Infineon [43] reportedly has optimized switching losses at 500 Hz – and is definitely capable of operating at higher frequencies. Also as mentioned earlier, instead of specifying a certain frequency, an asynchronous alternative based on rotor position may be used where the sorting order is updated at specified rotor positions. A comparison of the two will is given in section 4.5.5.

4.3.3 Speed and Current Controllers

As earlier mentioned, a PI controller is suitable for speed control. Given that large machines have relatively slow dynamics, high sampling rates are not required. A sampling rate of 500 Hz is chosen for speed. Also recall that speed control is disabled during the startup phase since a specific current is commanded in that phase.

As for current control, and as mentioned earlier, options include PI control with multi-carrier modulation, or multi-band hysteresis control. The latter was chosen in all simulations for simplicity and for the ease of comparing switching frequencies and losses for different schemes – e.g. half-voltage vs full-voltage energization. Again this does not apply for startup, where just a single-band hysteresis current controller is used with a special algorithm for deciding the number cell capacitors to be inserted – as described in detail in section 4.2.4.

4.3.4 Switching Frequency

Besides some very short, intermittent, periods of high switching frequencies at startup, each lasting ~0.1 s, the highest switching frequency is encountered at high speed operation. For the rated speed of 16790 r/min and assuming single-pulse operation at that speed, the switching frequency is (16790/60 x 4) = 1119 Hz, where 4 is the number of rotor poles. Therefore the highest switching frequency is around 1200 Hz. Again, modern-day high-power devices are easily capable of operating at such frequency.

4.3.5 Firing Angles

For a drive with a very wide speed range like the one considered here, the firing angles at different speeds must not be the same. A simple scheme of linearly varying firing angles are used in these simulations. The turn on or conduction angle (θ_{on}) was set to 11° for startup, which then decreases linearly to −8.5° at rated speed. The turn off or commutation angle (θ_{off}) was set to 41° at startup, which then decreases linearly to 33° at rated speed. While these values were found to be reasonable from simulation trials, they are not optimized. Efficient operation of the CCC SRM drive is the focus of the next chapter.

4.4 CCC SRM Drive Simulation Model

The simulation model for the CCC SRM drive is built using a combination of MathWorks MATLAB/Simulink and PLECS from Plexim. The simulation model spans the following domains:

- *Electrical domain* – to model the CCC converter power stage
- *Electromagnetic domain* – to model the SRM electromagnetic response
- *Mechanical domain* – to model the SRM dynamics
- *Thermal domain* – to model the semiconductor device losses.

The controls are programmed in Simulink, with embedded MATLAB code blocks to simplify coding of the algorithms for synthesizing v_{ph} under different conditions. The following sections provide a description of each of the simulation model's components.

4.4.1 Power Stage Model

The CCC converter power stage is modelled in the PLECS blockset for Simulink. Reasons for choosing PLECS include the fact that it is geared for power electronic systems, its ease of use, and its fast and reliable calculations. Its integration with Simulink enables the versatile power electronic modeling with PLECS in combination with the well-established control programming of MATLAB/Simulink. Another major advantage of PLECs is the ease of thermal modeling. It contains a framework for thermal calculations were the user only supplies the thermal properties of the device module and heat sink, then the conduction and switching losses, as well as junction temperatures, are easily obtained from simulation. Finally, PLECs-based thermal models of some commercial devices are available online on the manufacturer. As an example, the ABB website provides PLECs thermal models for many of its semiconductor modules.

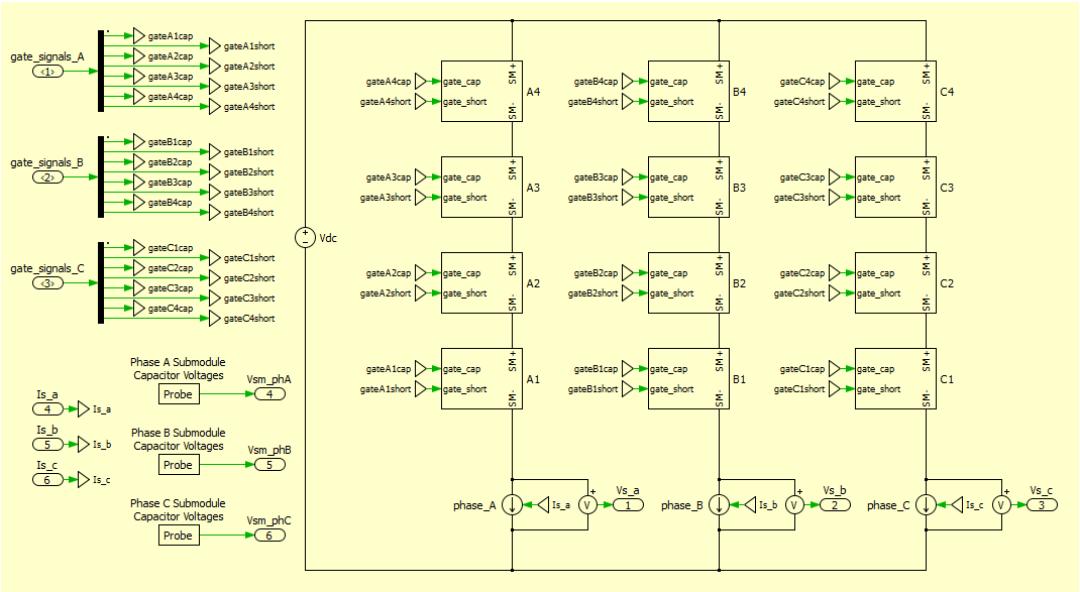


Fig. 4.4 Power Stage of the 4-cell CCC converter modeled in PLECS

A switching model rather than an average model is used for the switches/diodes. Voltage drops across the switches/diodes are ignored in the electrical model since they are very small compared to the large operating voltage – note however that they *are* included in thermal model. Also the rise/fall times are currently ignored – after verifying that the turn-on and turn-off time required by the switches available today are sufficiently low in comparison to the minimum switching time period of the simulated drive. Fig. 4.4 shows a screenshot of the power stage model in PLECS. The phase winding is modeled as a current source whose value is obtained from the SRM model. Therefore, one set of inputs to the power stage are the phase currents. The other set of inputs are the gate signals from the controller block. The outputs are the three phase voltages (measured across the respective current sources) and the cell capacitor voltages. The resistive drop of the phase winding is modeled in the SRM model block and so it is omitted here.

4.4.2 Models for SRM and Load

This part includes the electromagnetic and mechanical models of the SRM and load. The load has a quadratic torque-speed characteristic, typical of fans and compressors in the targeted applications. Let the load torque be referred to as T_{load}, and let ω denote speed. Equation (4.3) describes the behavior of the load.

$$T_{load} = k_{load}\omega^2 \tag{4.3}$$

The constant k_{load} is chosen such that at rated speed the total load torque plus the torque to overcome friction equals the rated electromagnetic torque, $T_{e\text{-}rated}$. This is mathematically expressed in (4.4), where B is the friction coefficient whose value is given in Table 4.4. The value of B was chosen such that the frictional losses are 1% of the rated power. The calculated value for k_{load} is 0.000342 N·m/(rad^2/s^2).

$$T_{e-rated} = k_{load}{\omega_{rated}}^2 + B\omega_{rated} \tag{4.4}$$

The electrical behavior of the SRM is described in (4.5), where R_s is the resistance of the phase winding, λ is the flux linkage for the corresponding phase, and θ is the rotor position.

$$v_{ph} = R_s i_{ph} + \frac{d\lambda(\theta, i_{ph})}{dt} \tag{4.5}$$

Rearranging (4.6) results in the following:

$$\lambda(\theta, i_{ph}) = \int \left(v_{ph} - R_s i_{ph}\right) dt \tag{4.6}$$

Equation (4.6) is very convenient for simulation and is in fact quite commonly used in modeling SRMs. A voltage is applied to the phase, and the resistive drop based on the current value of i_{ph} is subtracted from it. The result is then integrated to obtain λ. The next step is to obtain the i_{ph} value corresponding to that λ value so it can be used in the next simulation step. For this purpose, pre-calculated data relating i_{ph} to λ for different values of θ is used. This so-called magnetization data is obtained through FEA analysis – in

this case using Maxwell ANSYS. Therefore, a non-linear model for the flux linkage based on FEA magnetization data is the core of this SRM model. This data is stored in the form of a lookup table in Simulink. The lookup table block in Simulink then allows for interpolation/extrapolation of the data for values not explicitly included in the tables. Fig. 4.5 shows a graphical representation of the SRM inductance data for the subject 2MW motor – and recall that the inductance, L, is equal to the product $\lambda \cdot i_{ph}$. $\theta = 0°$ represents the unaligned position, i.e., when the stator pole of the subject phase is exactly between two rotor poles. $\theta = 45°$ represents the aligned position, i.e., when the subject phase stator pole is in complete alignment with a rotor pole. The different traces are for different values of i_{ph}, in steps of 50 A, starting from 50 A (uppermost trace) to 1000 A (lowermost trace).

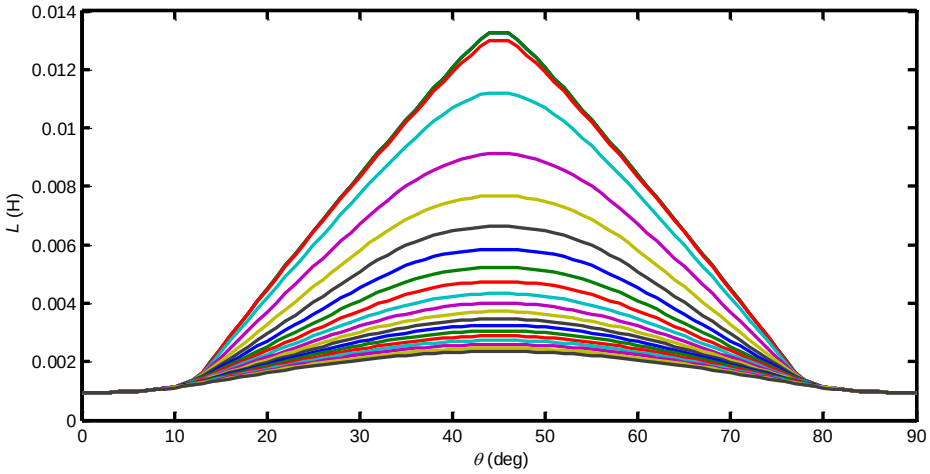


Fig. 4.5 SRM inductance data for various magnetization currents: lowermost trace 1000 A, uppermost trace 50 A

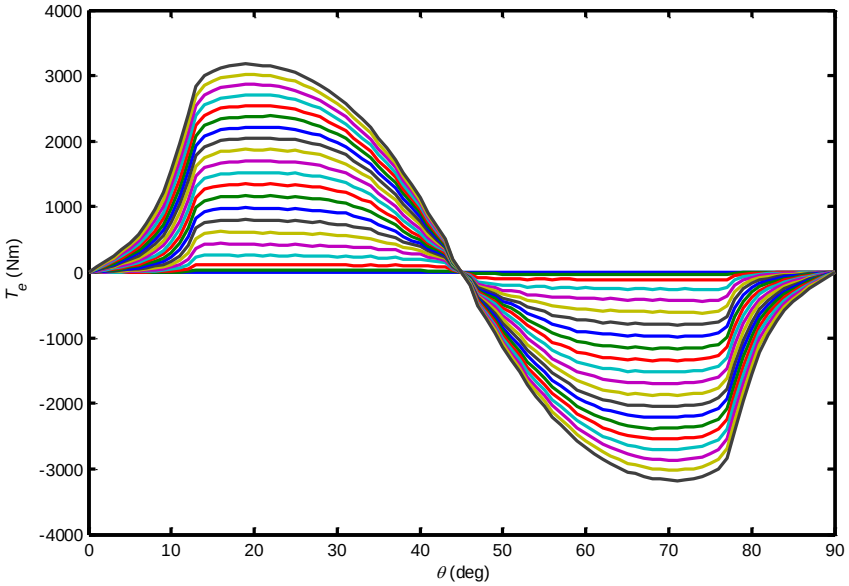


Fig. 4.6 SRM torque data for various magnetization currents: uppermost trace 1000 A, lowermost trace 50 A

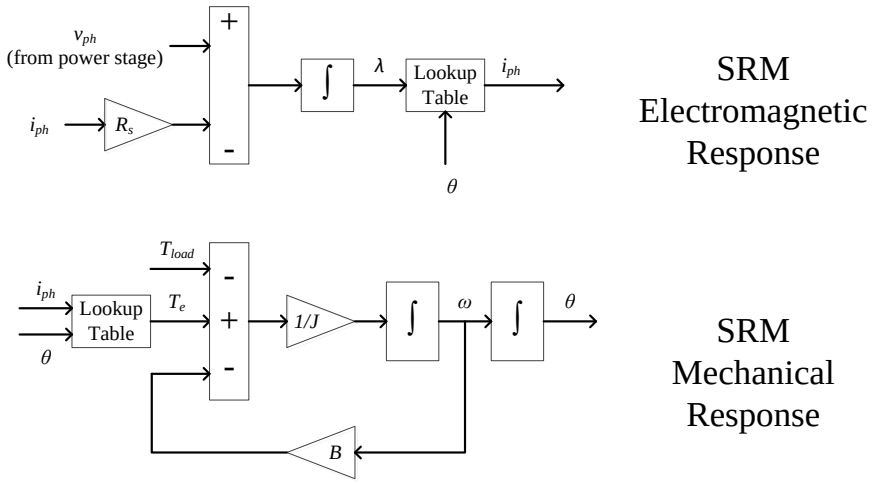


Fig. 4.7 Complete electromagnetic/mechanical SRM and load model used in simulation

A similar non-linear model is used to simulate the mechanical behavior of the SRM. The equation describing the motor dynamics is given in (4.7), where J is the coefficient of inertia in units of kg·m^2 and T_e is the developed electromagnetic torque in N·m.

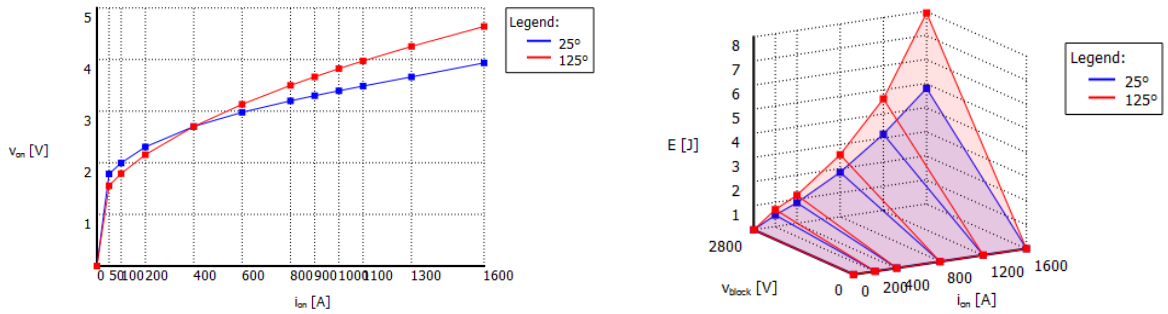
$$J\frac{d\omega}{dt} = T_e - T_{load} - B\omega \tag{4.7}$$

With T_{load} calculated from (4), and B and J as given in Table 4.4, only T_e is required to calculate the value of acceleration and hence obtain the updated speed value (through integration) as well as the updated rotor position (through a second integration). T_e is obtained from another Simulink lookup table based on data obtained through FEA analysis as well.

Fig. 4.6 provides a graphical representation of the stored FEA data for T_e as a function of θ and i_{ph}. Again the different traces represent different i_{ph}, ranging from 50 A (lowermost trace) to 1000 A (uppermost trace), in steps of 50 A. Fig. 4.7 summarizes the complete electromagnetic/mechanical SRM and load model used in the simulations.

4.4.3 Thermal Model for Semiconductor Losses

It is necessary to model semiconductor losses in order to ensure safe operation of the drive at all stages, including transients (like startup and acceleration) and steady state. A thermal model is implemented with the aid of the PLECS blockset for Simulink, and is used to calculate the conduction and switching losses, as well as device junction temperatures. Blocking state losses due to leakage currents are neglected as they are typically small. The data used to calculate losses are based on ABB IGBT modules.

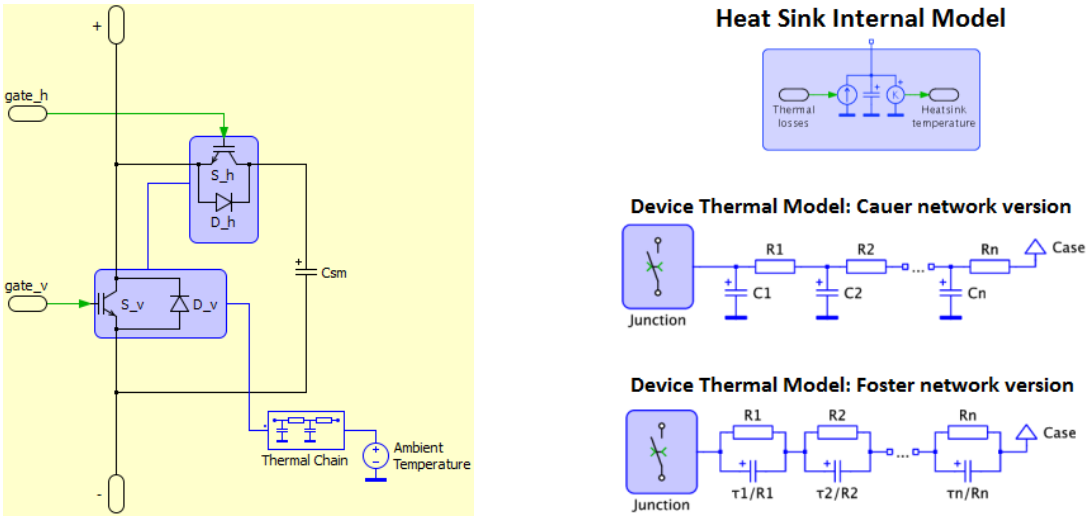


(a) (b)

Fig. 4.8 Semiconductor loss data as viewed in PLECS: (a) Diode on-sate voltage, (b) IGBT turn-on losses

The PLECs thermal models for IGBT modules used in simulations was downloaded from the ABB website. The model contains all relevant thermal information, including switching loss data, conduction loss data, and values of the module thermal resistance and capacitance used to calculate the device junction temperatures. All of this is conveniently included in a single XML file for each IGBT + diode module. Otherwise, such data may be obtained from the device datasheets and entered manually into PLECs. However, manually entering information may be time consuming and prone to error, and also not all information is readily available in the datasheets, and the manufacturer may need to be contacted for some information. Calculation of losses and device temperatures by PLECS is explained below.

Conduction Losses: This is simply calculated as the product of device current and on-state voltage. On-state voltage data as a function of device temperature and current is stored as a lookup table in PLECS. Graphical representation of an example of on-state voltage data for a diode is shown in Fig. 4.8 (a).



(a) (b)

Fig. 4.9 (a) Single CCC converter cell with heat sink as modeled in PLECS, (b) PLECS thermal models of the heat sink and devices as given in the PLECS documentation

Switching Losses: Again switching losses are stored in the form of lookup tables in PLECS. These tables store values for switching energies as a function of current. But typically switching losses are available at several operating temperatures as well as one or two blocking voltages. Therefore, switching loss data is stored as a 3-D lookup table – with one table for turn-on losses and another for turn-off losses. Graphical representation of turn-on loss data for an example module is shown in Fig. 4.8 (b). During simulation, PLECS uses linear interpolation and extrapolation to calculate the actual losses from the lookup tables.

Heat Sink: In modeling of the CCC converter, each cell was assigned a separate heat sink. Fig. 4.9 (a) shows a screenshot of a cell in PLECS; the heat sink appears as a semitransparent block covering switches to which it is to be connected in practice. The thin blue line connecting the two heat sinks signifies that the two heat sinks are in fact one but shown separate for visual clarity. In PLECS the heat sink is modeled by a capacitance, as shown in Fig. 4.9 (b); it absorbs all thermal losses dissipated by the components it encloses then propagates its temperature back to these components. The heat sink thermal capacitance is given by the product of it mass (in kg) and its specific thermal capacitance (in J/K.kg); this information is obtained from the manufacturer. The value chosen for the specific thermal capacitance in the simulations was based on other practical drive designs of similar power capability. Note that thermal capacitance does not have important implications at steady state, but is important during transients.

Device Thermal Model: The device thermal equivalent circuit is modeled in PLECS as a network of thermal transitions from junction to case. Each transition consists of a thermal resistor and a thermal capacitor. One of two forms for the thermal network may be used, the *Cauer* network or the *Foster* network. Both are made of series transitions, with each transition containing a thermal resistance and a thermal capacitance, as shown in Fig. 4.9 (b). The R_i are units of K/W; the C_i in the *Cauer* network are in units of J/K, while the τ_i in the *Foster* network are in units of seconds. The PLECs thermal models downloaded from the ABB website already contains these values; otherwise, they may be obtained from the device datasheets. A thermal chain component, also shown in Fig. 4.9 (b), is used to model the thermal transitions from device case to heat sink, and then heat sink to ambient. The former depends on factors like the thermal interface material, thermal interface area, and others, while the latter depends on heat sink material, size, design, and system airflow. Again, typical values are used.

Calculating Heat Sink and Device Junction Temperatures: The semiconductor device junction temperature is the maximum temperature at the die surface (i.e. device circuit itself), and is the most important to be monitored. Device datasheets provide the maximum safe values of junction temperatures, and it is recommended that operation be well below those limits. With knowledge of the thermal losses as well as the thermal transition values, device junction temperatures are easily obtained through the general

equation given in (4.8), where R_{12} is the thermal resistance (in K/W) between point 1 and point 2, T_1 and T_2 are the temperatures at points 1 and 2, respectively, and P_{12} is the power loss from point 1 to point 2.

$$T_2 = T_1 + R_{12}P_{12} \tag{4.8}$$

Note that the conduction and switching losses described above are calculated in unites of energy, i.e. Joules. At steady state, these are converted to power losses by averaging them over a large time period.

4.5 Simulation Results

The simulation is run in discrete-time mode with a fixed step size of 1μs. The plotting resolution is 10μs. With regards to the choice of the device voltage rating, guidelines provided by ABB for load-side converter device selection are followed [24]. These guidelines explain that the safety margin in motor-side device voltage rating need not be as high as that in the front-end converter devices, especially when a dc link capacitor is used as it filters out random transients from the AC source. It is suggested that a 10-20% safety margin be added on top of the peak line-line AC input voltage to account for normal line tolerances, plus another 50-60% of the result to account for switching conditions and stray inductances on the load side. In the 4-cell CCC SRM converter considered for simulations, each switch is rated V_{dc}/2, or 2000 V. Therefore, the minimum and maximum recommended device voltage ratings as per the ABB guidelines are 1.1x1.5x2000 = 3.3 kV and 1.2x1.6x2000 = 3.84 kV, respectively. For the conducted simulations it will be assumed that the 3.3 kV devices are safe enough, though in practice the next higher voltage rating may be preferred, or the nominal cell voltage may be designed to be lower. Therefore, the 3.3 kV/800 A single IGBT module (with anti-parallel diode) is chosen for the 4-cell CCC SRM converter simulations; its ABB IGBT module number is 5SNA 0800N330100. Details pertaining to the choice of device current rating are not included in this chapter but are covered in chapter 4 along with other practical considerations.

4.5.1 Simulation Results for Operation at Startup

Recall that the cell capacitors are initially charged to below their nominal voltage to avoid their voltages from rising too high upon startup. But also recall that the sum $\sum_1^N v_{cell-n}$ in one phase needs to be greater than V_{dc} in order to avoid uncontrolled flow of current in all phases through the D_h diodes upon closing the circuit of the CCC SRM drive (i.e. at startup). The initial $v_{cell\text{-}n}$ are therefore set to 52.5% of the nominal, i.e., $v_{cell\text{-}n}$ = 1050 V. This makes the initial sum $\sum_1^N v_{cell-n}$ equal 4200 V, i.e. 200 V above V_{dc}, hence putting the D_h diodes in reverse bias.

For this startup simulation an i_{ph} of 150 A is commanded along with a ±100 A hysteresis band, as in the first row of Table 4.2. All other values are as mentioned in section 4.4, including C = 20 mF. Fig. 4.10 (a) shows waveforms for the first stroke only, which is commanded P-mode by the controller – i.e. i_{ph} is positive. As earlier mentioned, θ_{on} and θ_{off} for startup are 11° and 41°, respectively, and the initial rotor

position for the first energized phase was also set at 11° to simulate the worst-case rise in the $v_{cell\text{-}n}$. Given this initial position and a dwell angle of $\theta_{off} - \theta_{on} = 30°$, the other two phases will only start conducting after the first stroke is over. Therefore only the waveforms of the first phase energized are shown in Fig. 4.10 (a). Waveforms for ω and T_e, the total developed electromagnetic torque, are given in Fig. 4.10 (b). The role of the startup modulation strategy in reducing the switching frequency is clearly noted from Fig. 4.10 (a). All four $v_{cell\text{-}n}$ traces appear identical in Fig. 4.10 (a), but upon zooming in, a small difference may be noticed, and this is shown in Fig. 4.11.

Bursts of high switching frequency, with a maximum of about 10 kHz, occur for very short periods of time of less than 0.1 s. The IGBT device chosen is in fact capable of higher switching frequencies, as long the thermal condition of the devices is maintained below critical temperatures.

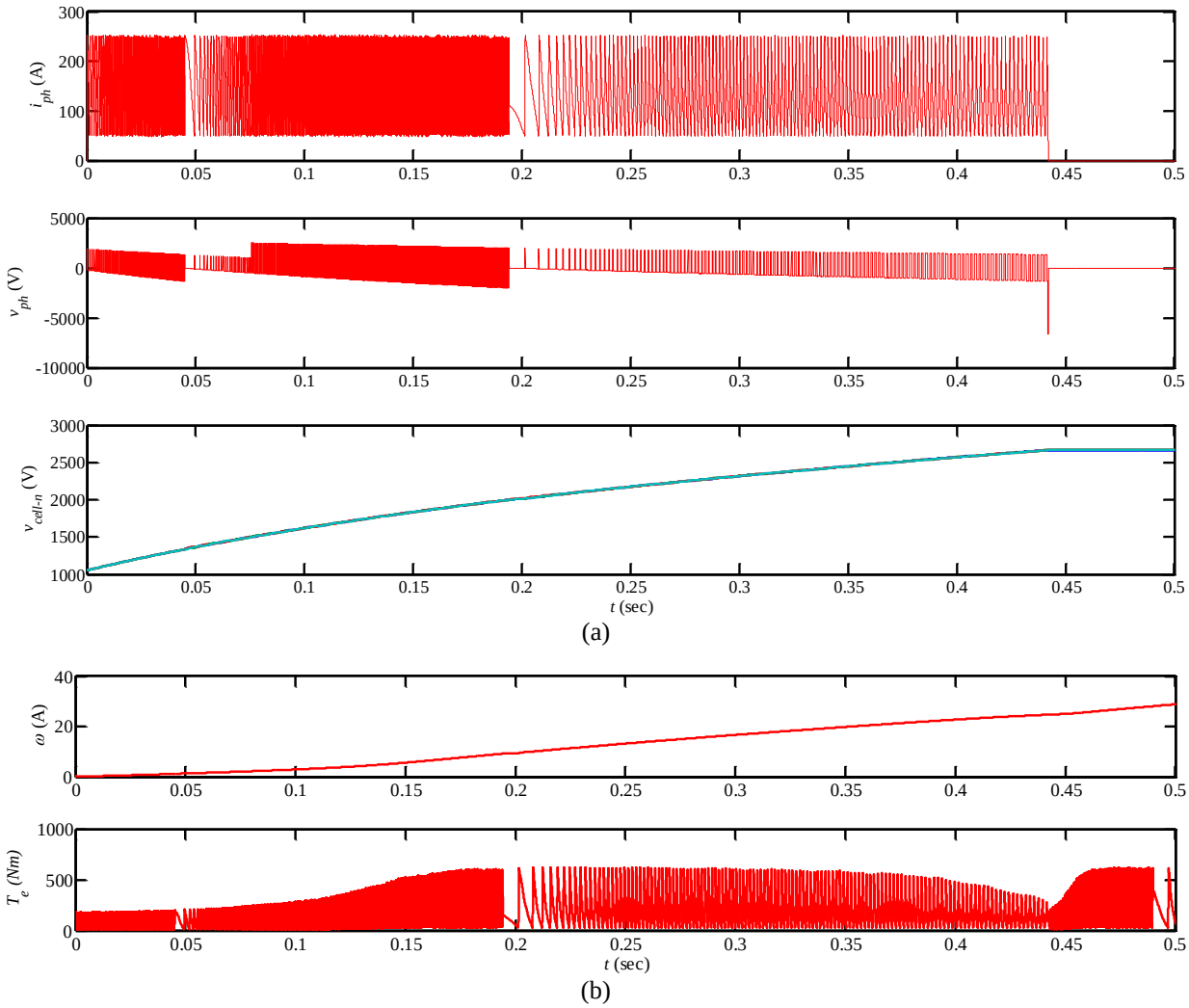


Fig. 4.10 Startup operation: Waveforms during the first stroke for the first phase to be energized

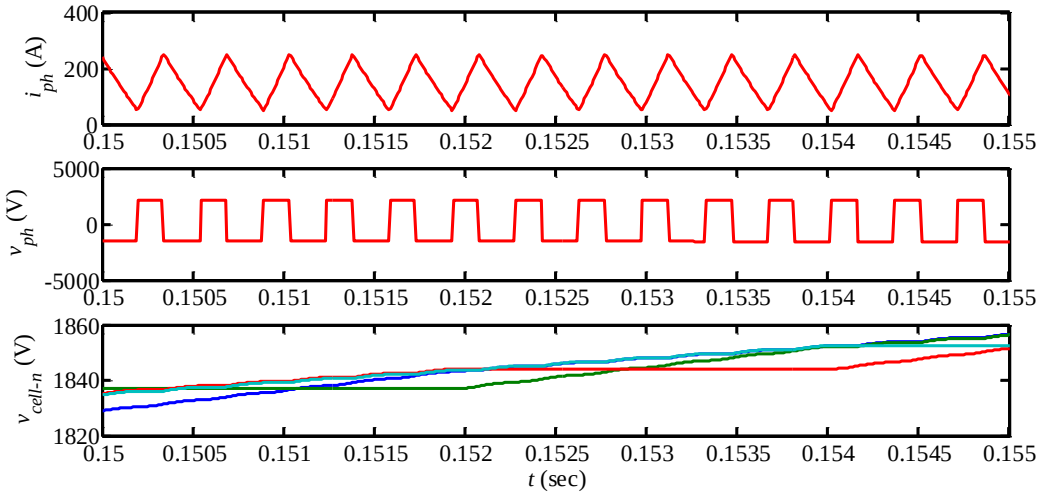


Fig. 4.11 Startup operation: Close-up waveforms for startup operation showing minor variation in $v_{cell\text{-}n}$

Next, the $v_{cell\text{-}n}$ in all phases are shown up to 1% of the rated speed are shown in Fig. 4.12. Note how the cell capacitor voltages are quickly controlled close to their nominal value of 2000 V – marked by the horizontal red line in Fig. 4.12.

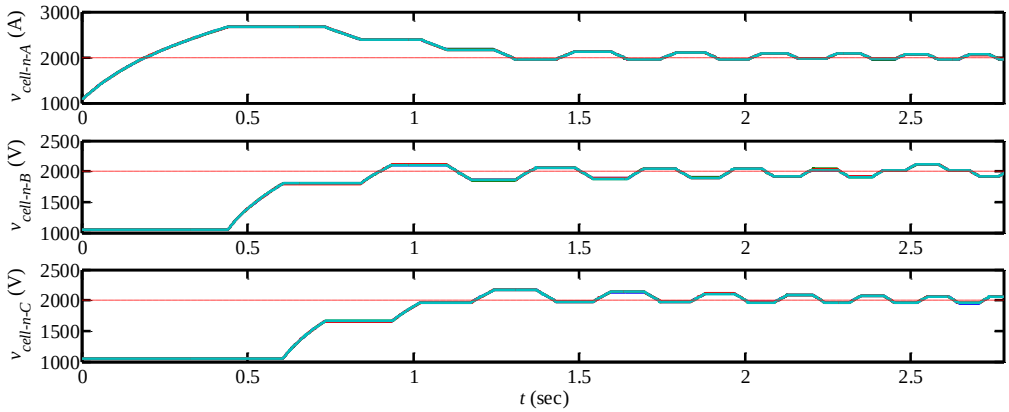


Fig. 4.12 Startup operation: Waveforms of $v_{cell\text{-}n}$ for all three phases up to 1% of rated speed

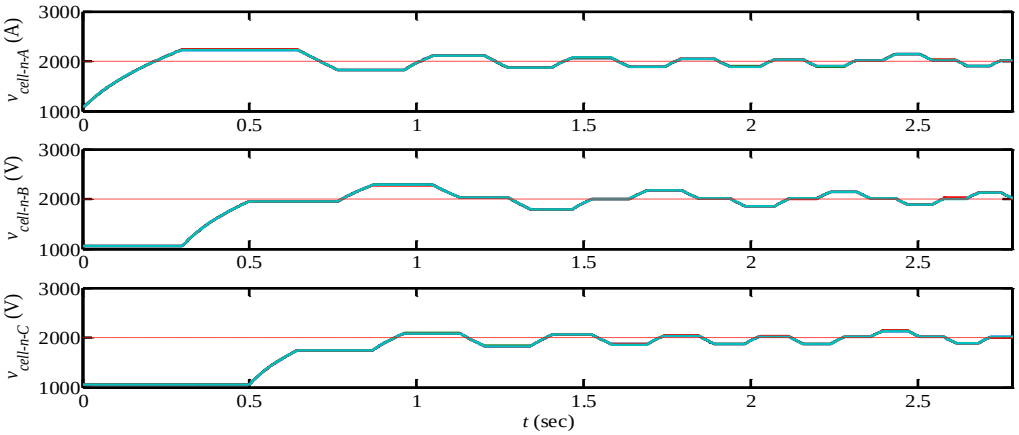


Fig. 4.13 Startup operation: $v_{cell\text{-}n}$ waveforms for all phases up to 1% of rated speed – improved scheme

The maximum voltage reached by a cell capacitor, $v_{cell\text{-}n\text{-}max}$, was 2669 V. This happens in the phase that is first energized, since in the first stroke the speed is lowest. The second phase to be energized had a $v_{cell\text{-}n\text{-}max}$ of 2175 V, and the last phase to be energized had a $v_{cell\text{-}n\text{-}max}$ of 2120 V. Noting this trend, some measures may be taken to reduce $v_{cell\text{-}n\text{-}max}$ in the first stroke. First, if one of the phases is initially placed in the aligned position, which is equivalent to 45° rotor position in this context, then the other two phases will be at 15° and 75°. This could be achieved by applying current pulses in one phase only prior to startup until the rotor poles are aligned with that phase.

Assuming that the direction of rotation is consistent with an increasing rotor position, then the first phase to be energized will be the one at 15°. Second, if the initial firing angles are set at θ_{on} = 5° and θ_{off} = 35°, then the first energized phase will conduct for only 20° during its first stroke, as opposed to the worst case of 30°. This scenario was tested in simulation and the resulting $v_{cell\text{-}n\text{-}max}$ waveforms are shown in Fig. 4.13. The first energized phase had a $v_{cell\text{-}n\text{-}max}$ of 2237 V only. The second energized phase had a $v_{cell\text{-}n\text{-}max}$ of 2283 V after two strokes, and the phase last energized had a $v_{cell\text{-}n\text{-}max}$ of 2091 V after two strokes as well. This represents a significant improvement over the previous scenario where the first energized phase had $v_{cell\text{-}n\text{-}max}$ = 2669 V. Also the $v_{cell\text{-}n\text{-}max}$ of the second and third energized phases in this second scenario may be further reduced by widening the $v_{cell\text{-}n}$ control band, which will most likely force the second stroke to be N-mode. The second scheme resulted in a reduction of acceleration by ~9% only measured over the first 1% of the speed range.

Finally, to verify that the thermal limits are also satisfied, the temperatures of all four devices in a cell are plotted, as shown in Fig. 4.14. This is done for a representative cell in the first phase to be energized, with the worst-case scenario assumed where the phase undergoes a complete 30° conduction in its first stroke.

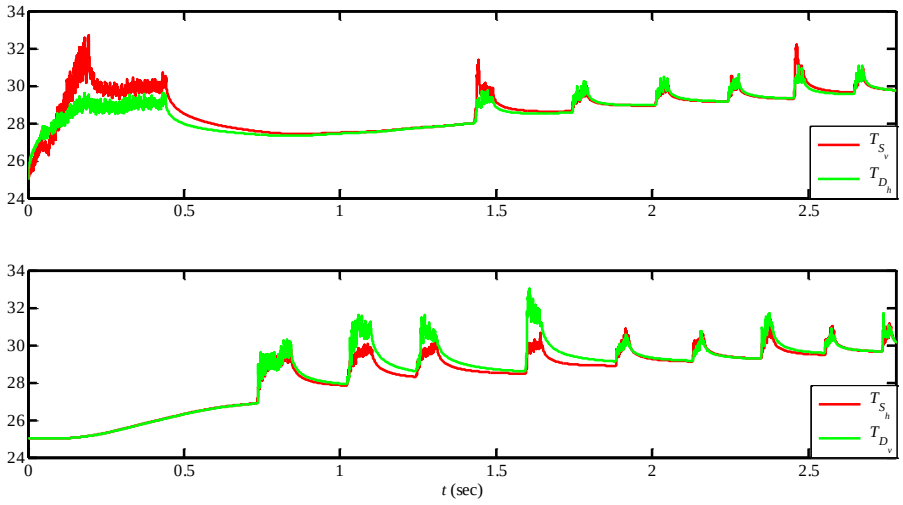


Fig. 4.14 Startup operation: Temperature profile in °C of semiconductors in a cell up to 1% of rated speed

The other cells are expected have to behave almost identically, both in thermal and electric terms, by virtue of the rotation among the cells. But in practical applications monitoring of all cells is necessary for the purpose of fault detection. The same thermal capacitance of 1 J/K used earlier in the section on sizing C was assumed for this simulation. Also the same thermal resistance from the device case to ambient of 0.1 K/W is used, along with an ambient temperature of 25°C.

In summary, the two main goals of the startup scheme, which are to limit the rise in $v_{cell\text{-}n}$, as well as limit the switching frequency in order to allow safe thermal operation, have been achieved. This is attained by continuously adjusting v_{ph} while the $v_{cell\text{-}n}$ change during startup, in order to choose the smallest voltage steps.

Once the drive has reached a few percent of the rated speed, regular speed and current control described in section 4.2.2, along with the regular $v_{cell\text{-}n}$ control described in section 4.2.1, may be used. The firing angles should be adjusted at that stage, since a large conduction window may result in a very high rise in the $v_{cell\text{-}n}$. The choice of firing angles for the complete speed range, for both transient and steady state operation, is discussed in detail in chapter 3. For now an example of the acceleration in the very low speed region is provided to demonstrate that the standard $v_{cell\text{-}n}$ control may be safely used at a very low speed – after the drive has been started with the special startup scheme. For this purpose, a simulation for the drive accelerating from 200 r/min to 250 r/min (roughly 1.2% to 1.5% speed) is performed; the resulting $v_{cell\text{-}n}$ waveforms are given in Fig. 4.15. It is clearly seen form the figure that the $v_{cell\text{-}n}$ are very well controlled, with the ripple being only ±13% at such low speed. Chopping was done using only $V_{dc}/2$ and 0 V.

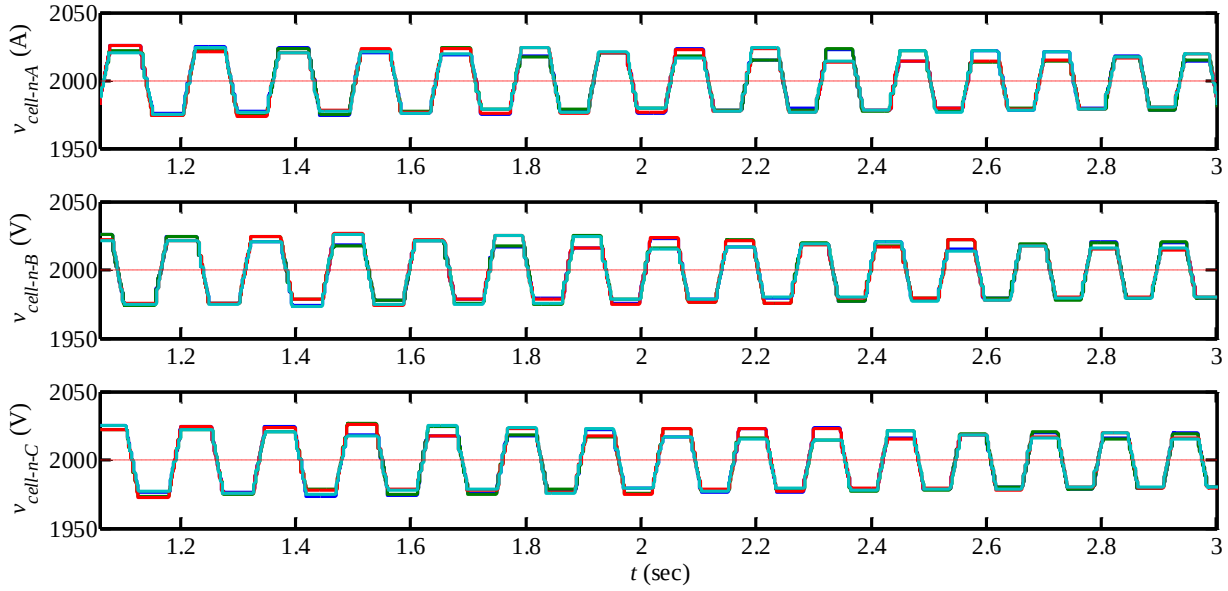


Fig. 4.15 $v_{cell\text{-}n}$ waveforms for all phases during acceleration from 1.2% to 1.5% speed – demonstrating successful control of the $v_{cell\text{-}n}$ at very low speeds

4.5.2 Simulation Results for Operation at Rated Speed

Fig. 4.16 shows voltage and current waveforms for operation at rated speed and rated torque. Fig. 4.17 shows a close-up of the waveforms, also including torque, where Fig. 4.17 (a) shows only two P-mode strokes and Fig. 4.17 (b) shows only two N-mode strokes. At this speed and torque only full dc link energization is feasible, as intermediate energization voltage levels will not sustain the high current requirement. Therefore only full voltage pulses, i.e., $+V_{dc}$ or $-V_{dc}$, are seen in the waveforms. θ_{on} and θ_{off} are chosen so that the drive works in single-pulse mode at this operating point – again chapter 3 will provide details on how the appropriate θ_{on} and θ_{off} are chosen for the complete speed range. It is noted from Fig. 4.16 that more P-mode strokes are used than N-mode in order to control the $v_{cell\text{-}n}$, which is expected since as earlier mentioned cell capacitors lose more charge in N-mode strokes than they gain in P-mode strokes. Semiconductor losses were 0.011 pu based on base power of 1.88 MW, with ambient temperature being 50°C and thermal resistance of the heat sink set at 0.02 K/W. Later in this section efficiency of the CCC SRM drive will be compared to that of the standard asymmetric converter driving the same 2 MW SRM.

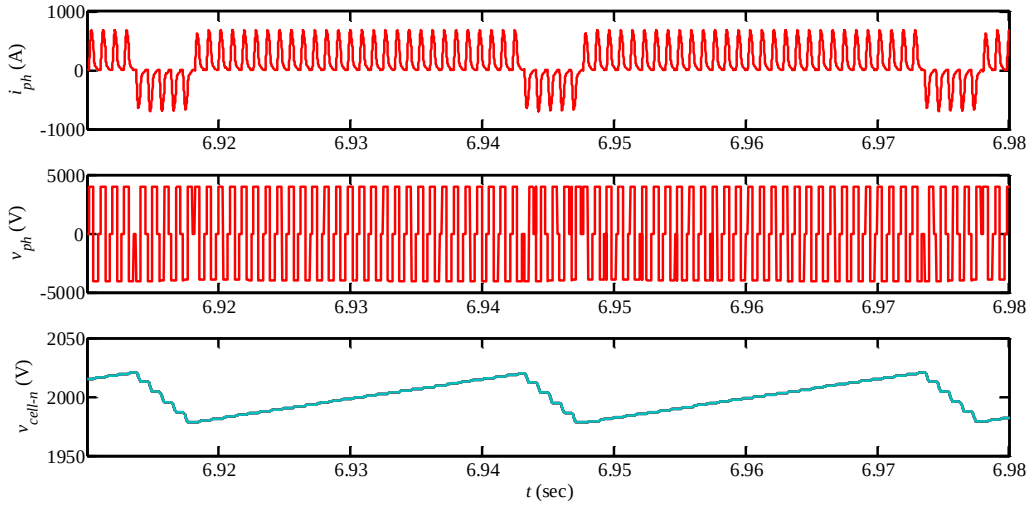


Fig. 4.16 Rated Operation: Waveforms for operation at rated speed and rated torque

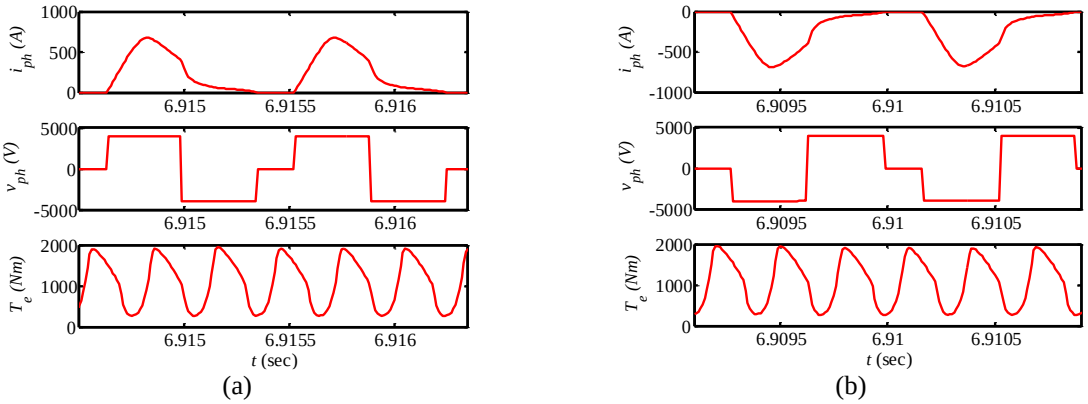


Fig. 4.17 Rated Operation: Close-up of waveforms for operation at rated speed and rated torque

Next, waveforms for all three phase currents ($i_{ph\text{-}a}$, $i_{ph\text{-}b}$, & $i_{ph\text{-}c}$), as well as the dc link current (i_{dc}), are given in Fig. 4.18. Note how i_{dc} is negative for short periods of time, which means energy is being returned from the converter back to the source. Such behavior may very slightly reduce efficiency due to additional losses in the dc link as well as in the cell capacitors. But note that the relative location of the N-mode conduction durations among the three phases is not constant and shifts over time. An intelligent scheme may be used to reduce the negative component of i_{dc} by shifting the N-mode strokes so that, as much as possible, only one phase is going using N-mode strokes at a time, with the other two phases using P-mode strokes. For instance, an on-coming N-mode stroke in one phase could be delayed if any other phase is using an N-mode stroke. In other words, a phase towards the end of its P-mode operation could prolong its P-mode operation in favor of another phase that is still in N-mode. The first phase would have to temporarily override its hysteresis $v_{cell\text{-}n}$ controller in that case, until the N-mode strokes in the other phase are completed. Doing this should set the N-mode strokes of the different phases apart for some time. But since the duration of P-mode and N-mode stroke spells are not uniform, it is likely that after some time N-mode strokes would start to overlap again. While the goal of this is to reduce the duration and magnitude of the negative portions in i_{dc}, in order to enhance efficiency, the dc link and capacitor losses are usually small and thus the little gain efficiency may not be worth the complication of having such intelligent algorithm. Also as will be shortly seen, when lower energization voltage levels are used, the duration of operation in P-mode decreases and that in N-mode increases, and so it becomes impossible to avoid any overlap. Therefore, as long as the front-end is able to exchange power in both directions, this should not be a major issue. Options for the front-end converter are discussed in chapter 4.

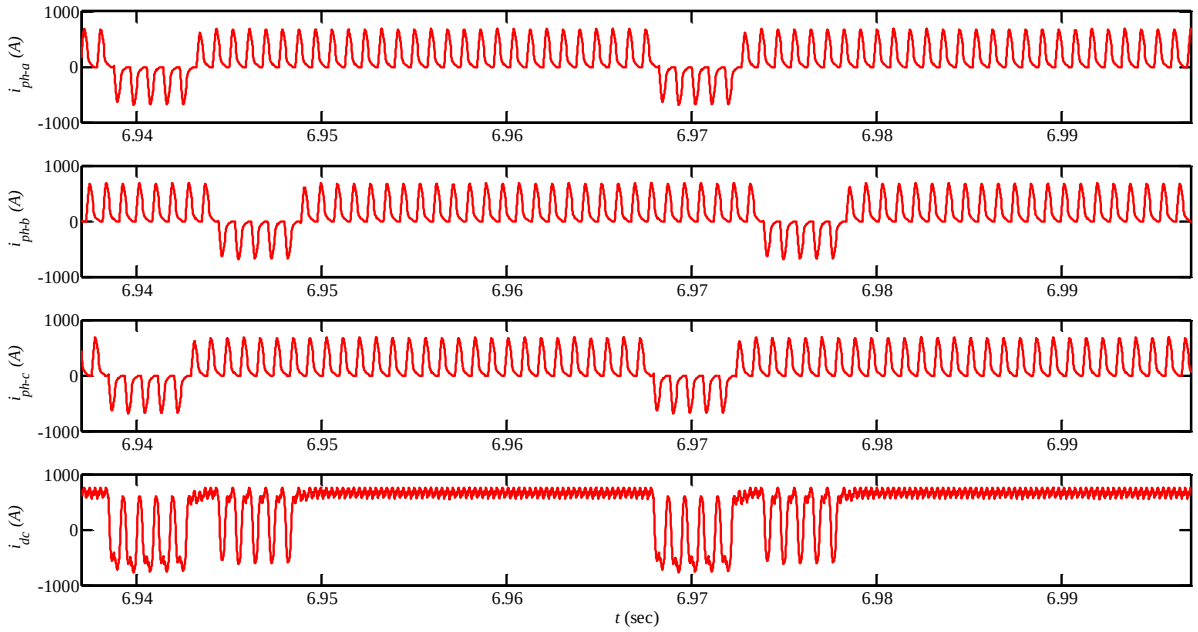


Fig. 4.18 Rated Operation: Waveforms of all three phase currents and dc link current at rated speed and rated torque

4.5.3 Effect of varying the $v_{cell\text{-}n}$ controller hysteresis band

It was seen from Fig. 4.16 that the number of P-mode strokes is much higher than that of N-mode strokes. For example, it may be counted from Fig. 4.16 that there are 5 N-mode strokes, followed by 28 P-mode, then 5 N-mode, then 29 P-mode. The exact number of strokes in one streak of the same type is decided by the size of the hysteresis band. For the past simulations the band size was set to ±1%. Decreasing this band size is expected to decrease both the number of successive strokes of the same type, i.e. P-mode or N-mode, while maintaining a similar ratio between the two. Fig. 4.19 compares the effect of using different hysteresis band sizes. Fig. 4.19 (a) shows i_{ph} and $v_{cell\text{-}n}$ for the same ±1% band, while Fig. 4.19 (b) shows the same waveforms but for a ±0.5% band, and finally Fig. 4.19 (c) shows the waveforms for a single line instead of a band. In the last case, the $v_{cell\text{-}n}$ switches to N-mode when the nominal 2000 V level is exceeded. The last scenario results in the minimum cell capacitor voltage ripple at an operating point, for a given capacitor size.

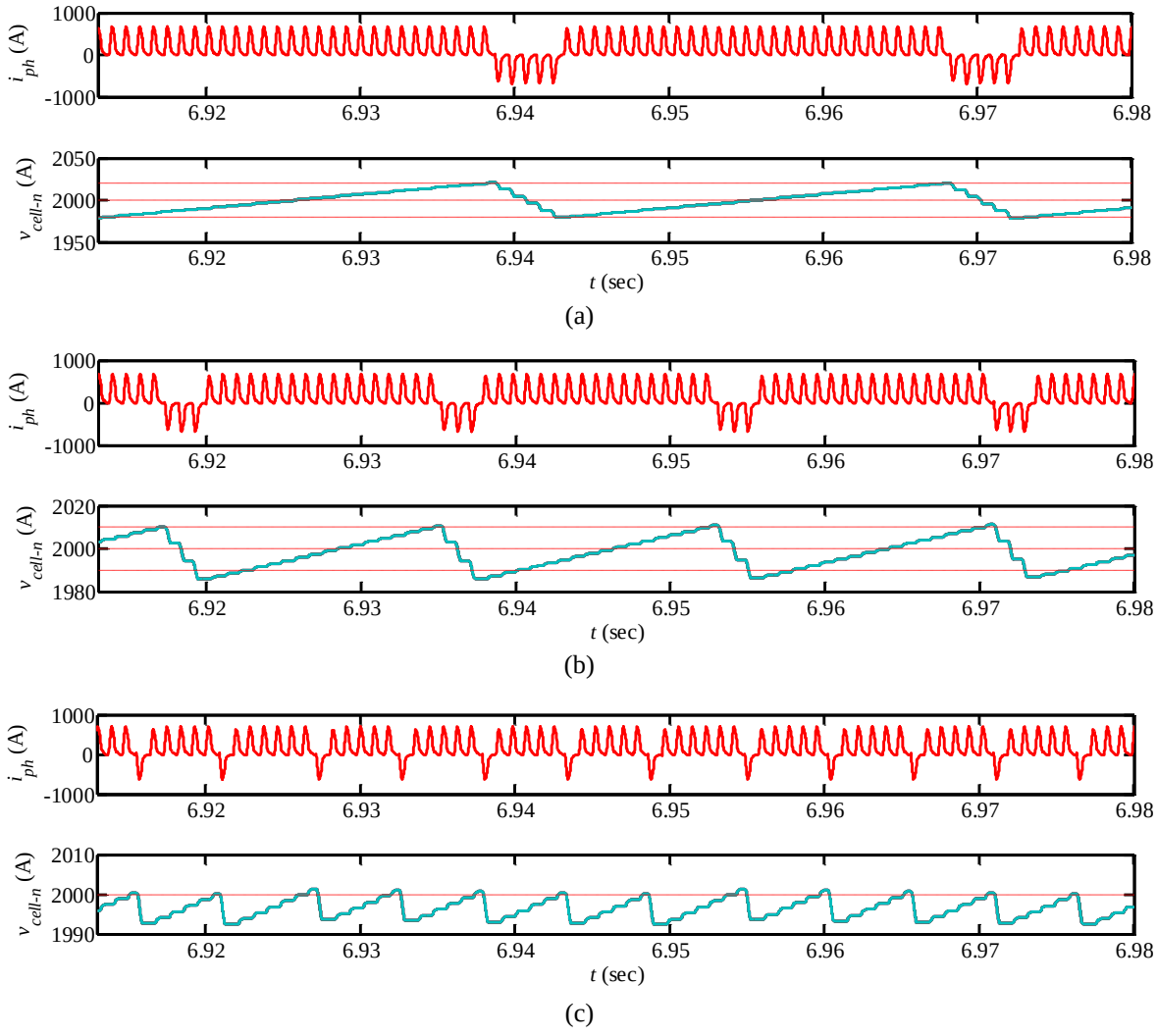


Fig. 4.19 Rated Operation: Effect of decreasing the $v_{cell\text{-}n}$ controller cell hysteresis band

Another point to be noted from Fig. 4.19 is that the smaller the band, the better the thermal balancing across the devices. Recall that in P-mode only the S_v and D_h devices conduct (in complementary fashion), whereas in N-mode only the S_h and D_v devices conduct (also in complementary fashion). Therefore, when there are many successive P-mode and many successive N-mode strokes, the devices tend to heat up more, which increases losses and thermal stress. The average current should not be much different going from one band size to another, but having the conduction rotate more regularly results in a better thermal response. In fact, the last scenario shows a very slight improvement in semiconductor losses over the first and second scenarios. Therefore, the single line band will be used in all subsequent simulations in this chapter.

4.5.4 Simulation results for operation at low speed

Further advantages of the multilevel capability may be demonstrated at medium and low speeds. The current control techniques describe earlier, namely PI current control with multiple carriers for modulation, and multi-band hysteresis, both take advantage of this capability by trying to use lower voltages when possible. In the following simulations, which are conducted at 7200 r/min (0.429 pu), multi-band hysteresis is demonstrated. But also two other energization schemes are explored, in order to show the flexibility offered by multilevel converters. First, the conventional full-voltage scheme, where only $\pm V_{dc}$ and 0 are used, is shown. Next, a half-voltage scheme, where only $\pm V_{dc}/2$ and 0 are used, is demonstrated. Finally, the multiband hysteresis case is demonstrated. In all three cases demagnetization is done with full $\pm V_{dc}$. This is because it is almost always desired to de-energize an SRM phase as quickly as possible, once θ_{off} has arrived, to avoid the development of negative torque from that phase. The fan/compressor type load described earlier was used, resulting in the load torque at this point being 0.184 pu only. Finally, the firing angles were chosen to be $\theta_{on} = -2°$ and $\theta_{off} = 33°$. This puts the drive in chopping mode in all three cases, which is done purposefully to demonstrate the reduction in switching with lower voltage levels.

Fig. 4.20 shows waveforms for the conventional full-voltage scheme. Fig. 4.20 (a) is a close-up, showing only three strokes, where the first two are P-mode and the third is N-mode. Fig. 4.20 (b) covers a larger time scale in order to properly show trends in $v_{cell\text{-}n}$ and i_{dc}. Some glitches are noted in the i_{ph} waveform, occurring at the beginning of some strokes; these are due to numerical issues in the simulation and are of very little or no consequence to the results.

In this full-voltage scheme, only $\pm V_{dc}$ and 0 are used during the energization phase. To implement that, a single hysteresis band was used. The hysteresis band was set at ±35 A. The default speed control using a PI controller that outputs a reference current command, i_{ph}^*, was used.

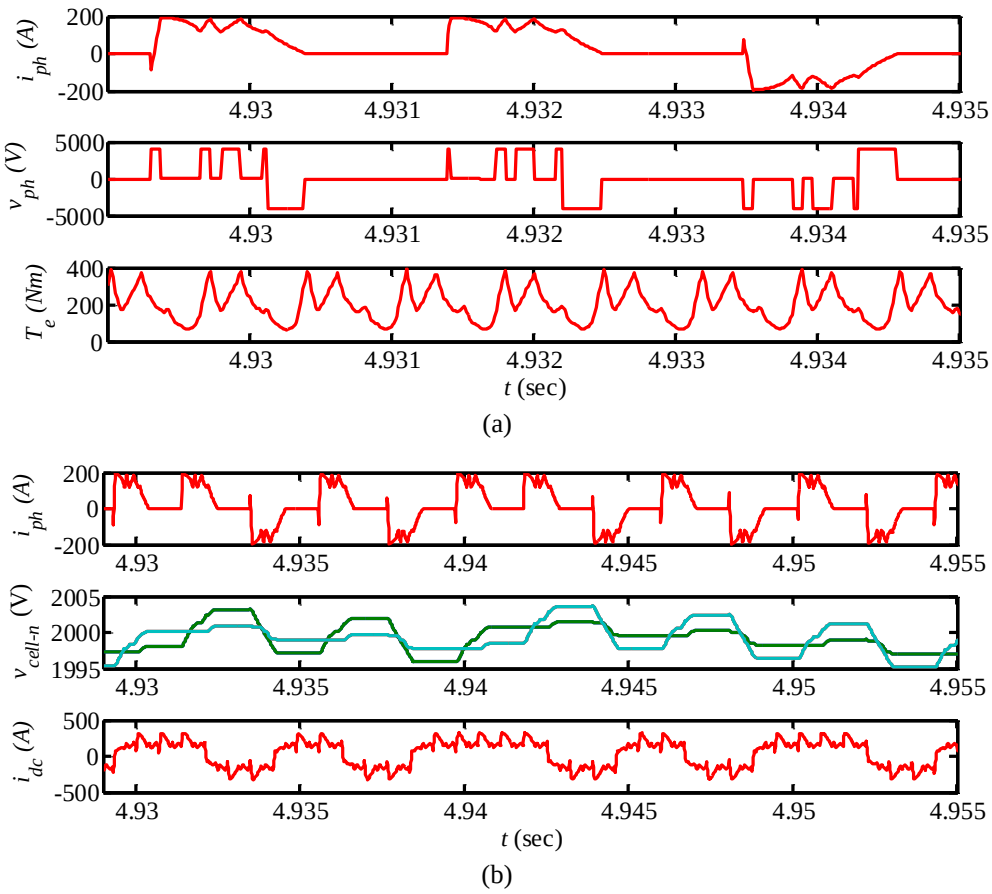


Fig. 4.20 Low-speed Operation: Waveforms for operation at 7200 r/min using full-voltage scheme

From simulation, i_{ph}^* came out to be 151.7 A for this scheme. Switching losses were 8.44 kW, while conduction losses were 1.23 kW. Together they represent about 0.005 pu (based on the rated power of 1.88 MW), or 6.44% of the operating output mechanical power, which was 150.19 kW. This is a high percentage of losses. However, this scheme is only illustrated for the sake of comparing to the other schemes; it is indeed highly preferable not to switch such levels of current at a high rate. High torque pulsations are also noted from Fig. 4.20 (a), which is also a result of the strong energization voltage that causes large variation in i_{ph} as it is controlled.

It is interesting to note from Fig. 4.20 (b) that the ratio of the P-mode strokes to N-mode strokes is only 2:1 or 1:1. This is contrasted to the P-mode to N-mode ratio at rated speed and torque, which was almost 6:1. The explanation for this is as follows. At rated speed and torque, the drive only used $\pm V_{dc}$, and not 0 or any other intermediate voltage level. For a P-mode stroke, this means only mode P0 is applied during energization, then only mode P4 is applied for demagnetization. Recall from Fig. 3.3 and Table 3.1 in the previous chapter that in mode P0 no capacitor conducts current, and so in this scenario the v_{cell-n} are unaltered throughout the energization phase. Also recall that in mode P4 all capacitors conduct positive current, i.e., they are charged. Therefore, to summarize, in the P-mode strokes of single-pulse mode

operation with only $+V_{dc}$ energization and only $-V_{dc}$ demagnetization, cell capacitors receive energy throughout the commutation period – which is from θ_{off} until i_{ph} drops to zero – but are unaltered during the conduction period. In the same token, in N-mode strokes of single-pulse mode operation with only $-V_{dc}$ energization and only $+V_{dc}$ demagnetization, it may be easily concluded that cell capacitors lose energy throughout the conduction period, but are unaltered during the commutation period. Now since the commutation energy represents only a small percentage of the total energy processed in one stroke, while conduction energy represents most, the rise of the $v_{cell\text{-}n}$ in a P-mode stroke in this scenario is much less than the drop in $v_{cell\text{-}n}$ in an N-mode stroke. This is why, to balance the $v_{cell\text{-}n}$, an N-mode stroke is required for every five or six P-mode strokes.

However, whenever any intermediate voltage level is used, the situation described above changes. In P-mode strokes, some of the cell capacitors do receive some energy, which is in addition to the energy that all cell capacitors receive when de-magnetization with $-V_{dc}$ takes place. This may be easily understood by inspecting intermediate modes, like P1, P2, and P3, in Fig. 3.3. On the other hand, the N-mode stroke behavior with intermediate voltage levels also changes, but in an opposing manner to P-mode. During energization with an intermediate voltage level, only some of the capacitors lose energy. But still during demagnetization with $+V_{dc}$, all $v_{cell\text{-}n}$ are unchanged. Again this is easily seen upon inspecting intermediate modes, like N1, N2, and N3, in Fig. 3.4 from the previous chapter. To summarize, the more intermediate voltages are used within a stroke, the less the difference is between the rise in $v_{cell\text{-}n}$ in P-mode and the drop in $v_{cell\text{-}n}$ in N-mode. In this current simulation set, the intermediate voltage level that was used was the 0 V level, whereas in the simulated operation at rated speed and torque, neither 0 V nor any other intermediate voltage level was used.

Next, consider the $v_{cell\text{-}n}$ waveforms in Fig. 4.20 (b). All $v_{cell\text{-}n}$ are plotted in the figure, but only two traces are visible since the other two exactly overlap them. This is expected since the drive uses only $\pm V_{dc}$ and 0, i.e. modes 0, 2, and 4 in Table 3.1. All of these mode either charge/discharge a pair of capacitors together, or all four at the same time, which results in every pair of cell capacitors always having the same voltage.

Finally, for the sake of comparison with other schemes, a calculation is performed to estimate the average switching frequency per IGBT. First, it is noted from Fig. 4.20 (a) that there are four pulses per stroke. Four IGBTs are turned on in the beginning of the first pulse, and four IGBTs are turned off only at the end of the last pulse. In between, three times it happens that two IGBTs are turned off (to get 0 phase voltage) then turned back on. Therefore, for this specific simulation case, there are 4+2+2+2 = 10 turn on events and 10 turn off events per stroke. With 4 strokes per rotation for a 6/4 SRM, there are 40 turn on and 40 turn off events per rotation in each phase. At a speed of 7200 r/min, or 7200/60 = 120 Hz, the duration

of each rotation is 0.0083 s. Therefore, the effective switching frequency is 40/0.0083 = 4.8 kHz. This is shared by four cells, and so the average switching frequency per cell is 4.8 kHz/4 = 1.2 kHz. Within one cell, the ratio of P-mode to N-mode strokes may be estimated as 3:2 from Fig. 4.20 (b). Also recall that in P-mode strokes only S_v and D_h conduct, while in N-mode strokes only S_h and D_v conduct. Therefore, it may be estimated that the switching frequency for the S_v IGBT in this scenario is 3/5 of 1.2 kHz, or 720 Hz. Likewise, the estimated switching frequency for the S_h IGBT in this scenario is 2/5 of 1.2 kHz, or 480 Hz. While the estimated switching frequencies are acceptable given today's commercial high-current devices, this can be further improved as will be seen in what follows.

The next scenario as mentioned uses only $\pm V_{dc}/2$ and 0, except during demagnetization where full V_{dc} is used. Again a ±35A single-band hysteresis is used, and with the same $\theta_{on} = -2°$ and $\theta_{off} = 33°$. Resulting waveforms are shown in Fig. 4.21; again some numerical glitches occur at the beginning of some strokes, but can be safely ignored.

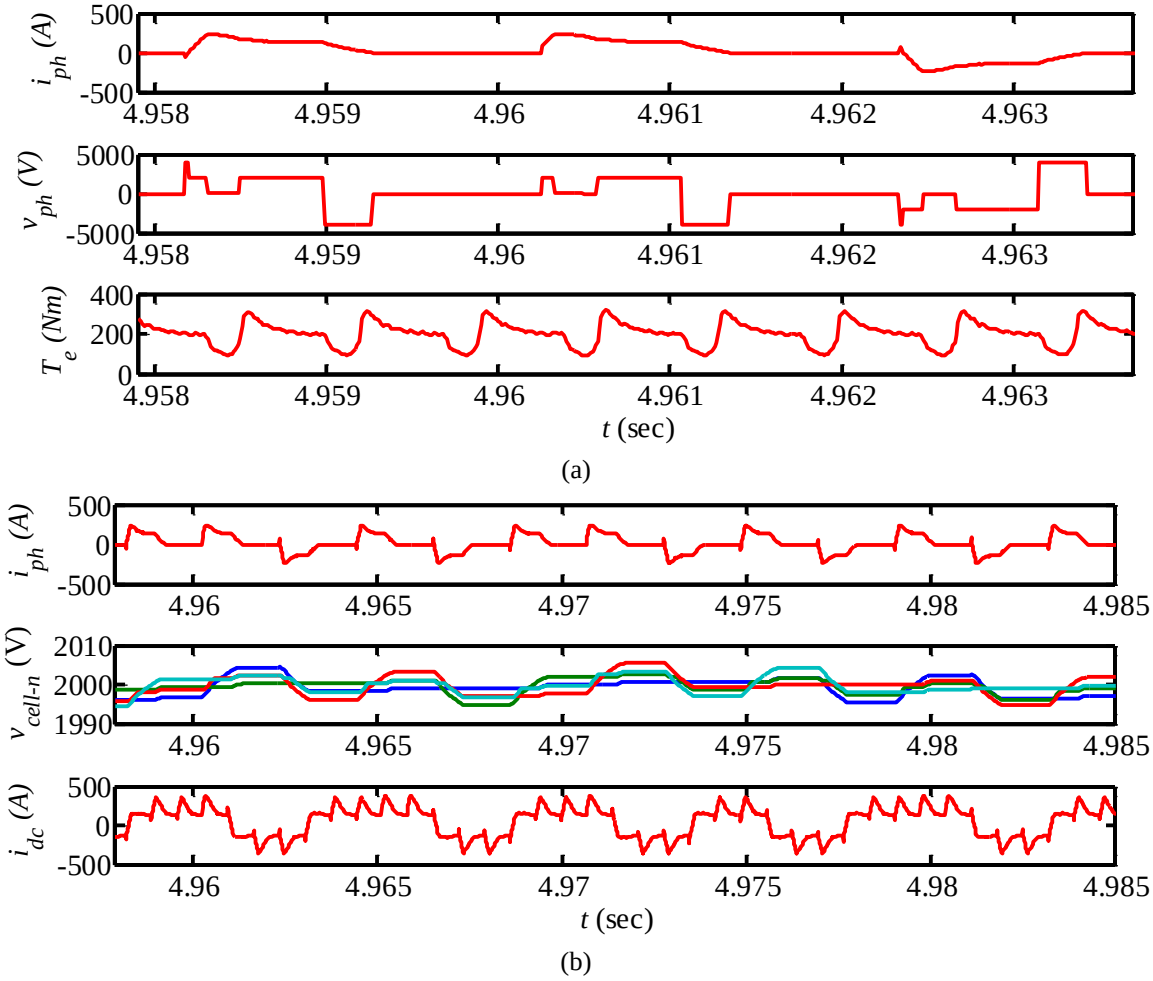


Fig. 4.21 Low-speed Operation: Waveforms for operation at 7200 r/min using half-voltage scheme

From simulation, i_{ph}^* came out to be 201.5 A for this scheme, compared to 151.7 A for the full-voltage scheme. This increase is expected since now the energization voltage is lower, yet the required power is the same, and so a higher current is commanded to compensate for the reduction in voltage. Switching losses were 2.70 kW, while conduction losses were 1.29 kW. Together they represent about 0.002 pu based on the rated power, or 2.65% of the operating output mechanical power of 150.19 kW. This is a vast improvement over the full-voltage case where semiconductor losses are about 2.5 times higher. This demonstrates one advantage that multilevel converters have to offer.

With regards to switching frequency, only two pulses per stroke occur in this scenario, as seen from Fig. 4.21 (a). Three IGBTs turn on in the first pulse, and also three turn off in the last pulse. In between, only one IGBT is turned off to get to 0 V, then one IGBT is turned on again to return to $+V_{dc}/2$. Therefore, there are (3 + 1) x 4 = 16 IGBT turn on and turn off events per revolution. The average switching frequency per cell is (16/0.0083)/4 = 480 Hz only. Fig. 4.21 (b), the estimated ratio of P-mode to N-mode strokes is again 3:2, and so estimated switching frequency for the S_v IGBT in this scenario is 3/5 of 480 Hz, or 288 Hz, and the estimated switching frequency for the S_h IGBT in this scenario is 2/5 of 480 Hz, or 192 Hz. The switching frequencies of 288 Hz and 192 Hz are almost three times lower and the 720 Hz and 480 Hz with the full-voltage case. This is why the switching losses are considerably lower in the half-voltage scheme. As for conduction losses, since less devices conduct on average in the half-voltage case, but at a higher current, conduction losses are similar in both cases. Torque ripple is also improved in comparison to the full-voltage scheme.

Next, the multi-band hysteresis scheme is considered, which allows the converter to use all voltage levels during chopping as opposed to only two. An inner band of ±20A is used to switch between $V_{dc}/2$ and 0, while an outer band of ±35A is used to switch between V_{dc} of one polarity and $V_{dc}/2$ of the opposite polarity. For example, for a P-mode stroke, if i_{ph} is more than 35A below i_{ph}^*, $+V_{dc}$ is used to increase the current. This is most commonly encountered at the start of a phase energization when current is rising from zero. Using full dc link voltage initially for energization allows for a quick current buildup, which is especially important at medium to high speeds due to the shortness of the stroke duration. Then when i_{ph} is within a certain threshold from i_{ph}^*, set here at 30 A, the inner ±20A band takes effect, and $+V_{dc}/2$ is used to further increase i_{ph}. Within this ±30A threshold, the inner band tries to maintain i_{ph} using $+V_{dc}/2$ and 0. If i_{ph} goes 30 A above i_{ph}^*, control is switched to the outer band again, and $-V_{dc}/2$ is used to reduce it until it is again within 30 A of the current. Then again the inner band takes control, and so on until the stroke is finished.

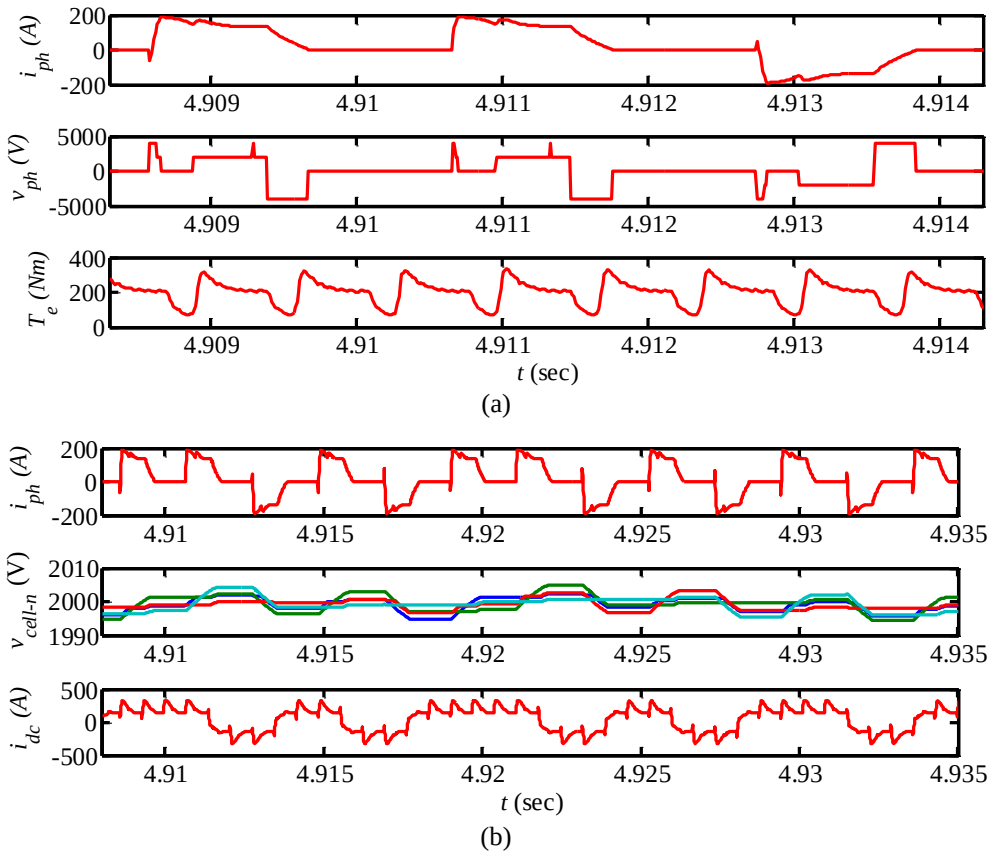


Fig. 4.22 Low-speed Operation: Waveforms for operation at 7200 r/min using mixed-voltage scheme

Waveforms for this mode of operation are given in Fig. 4.22. i_{ph}^* in this scheme came out to be 166.1 A, compared to 151.7 A for the full-voltage scheme and 201.5 A for the half-voltage scheme. The result that i_{ph}^* in this case lies between i_{ph}^* in the other two cases is expected, since the average energization voltage in this case also lies between those in the other two simulated. Switching losses were 7.57 kW, while conduction losses were 1.23 kW. Together they represent about 0.0047 pu based on the rated power, or 5.86% of the operating output mechanical power of 150.19 kW. These results represent only a slight improvement over the full-voltage scheme, but losses in the half-voltage scheme are much lower. In fact at this low speed (<50%), the full dc link energization pulses are not really required, and so using them increasing losses with little or no performance gains. As for average switching frequency, based on Fig. 4.22 (a) it is estimated to be {(4 + 1 + 1) x 4}/0.0083/4 = 720 Hz per cell. And again with the estimated ratio of P-mode to N-mode strokes being 3:2 from Fig. 4.22 (b), the estimated switching frequency for the S_v IGBT in this scenario is 3/5 of 720 Hz, or 432 Hz, and the estimated switching frequency for the S_h IGBT in this scenario is 2/5 of 720 Hz, or 288 Hz. The results for all three methods are summarized in Table 4.6.

Several conclusions are made from this set of simulations at the low speed of 7200 r/min:

TABLE 4.6
COMPARISON OF DIFFERENT ENERGIZATION SCHEMES FOR THE 4-CELL CCC SRM CONVERTER AT 7200 R/MIN

Energization Scheme	Switching Frequency		Switching Losses (kW)	Conduction Losses (kW)	Reference Current (A)
	S_v/D_h	S_h/D_v			
Full-voltage pulses	720 Hz	480 Hz	8.44	1.23	151.7
Half-voltage pulses	288 Hz	192 Hz	2.70	1.29	201.5
Mixed-voltage pulses	432 Hz	288 Hz	7.57	1.23	166.1

- The ability to use lower energization voltages, offered by multilevel converters, is highly advantageous in terms of efficiency improvement. Chapter 3 focuses on how to make the most of this flexibility in order to obtain pseudo-optimal efficiency.

- Device usage within one cell is more balanced at lower speeds when intermediate voltage levels are used. It was seen at rated speed that the S_v and D_h devices were used almost six times as much as the S_h and D_v devices, when no intermediate voltages (including 0 V) were used. But at 7200 r/min this ratio dropped to about 3:2. While this has no consequence on operation, it is important to note for the purpose of sizing the devices.

4.5.5 Synchronous vs. Asynchronous Cell Capacitor Sorting and Balancing

Recall form section 4.2.1 that the $v_{cell\text{-}n}$ are balanced by judiciously choosing which cell capacitors are inserted/bypassed during the charge/discharge operations that are part of the normal operation of the drive. To enable this, the $v_{cell\text{-}n}$ are continuously sorted by the controller. However, the $v_{cell\text{-}n}$ sorting order should not be updated at a high frequency, or else the capacitors will be switched in and out at a high rate, causing their associated switches to produce large switching losses and significantly overheat. It was also mentioned that the capacitor sorting order can either be updated at fixed time intervals, or at a fixed, repeating, rotor position. This section compares the two approaches using a simulation at the same 7200 r/min speed like in the previous section. The same half-voltage scheme (with a ±35 A hysteresis band) is also used here, with the same firing angles of $\theta_{on} = -2°$ and $\theta_{off} = 33°$.

Fig. 4.23 shows waveforms for the synchronous case, where the sorting frequency, f_{sort}, is set to 500 Hz. The vertical blue dashed lines mark the instants at which the sorting order is updated. Again the 4000 V spikes at the beginning of some strokes are to be ignored, as they are due to numerical glitches. Since f_{sort} is not related to the operating speed of the drive, the position of the sorting order update instant continuously shifts with respect to the rotor position, θ. As a result, sorting order update instants sometimes occur during the active period of the stroke, while current is flowing, and sometimes during the inactive period. This is easily noticed from Fig. 4.23. The cell capacitors are hence sometimes switched in or out while current is being conducted, which increases semiconductor switching losses.

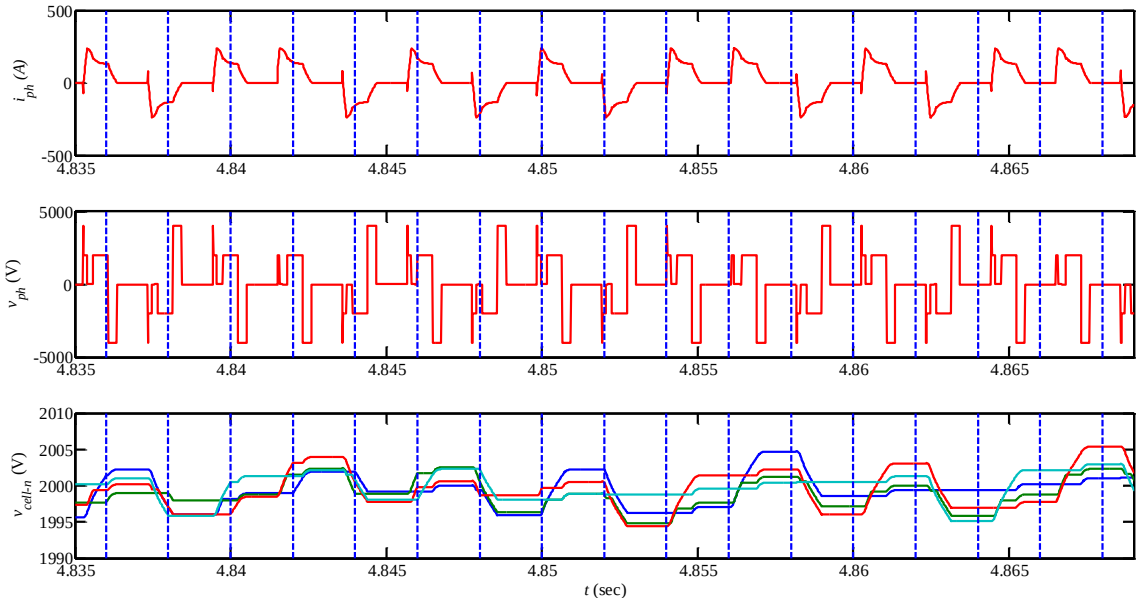


Fig. 4.23 Synchronous capacitor sorting: Operation at 7200 r/min with f_{sort} = 500 Hz

A small section from Fig. 4.23 that illustrates a case of such extra switching is magnified and shown in Fig. 4.24. In Fig. 4.24, the drive is going through a P-mode stroke, where capacitors are charged up – and so the cell capacitors with lowest voltage are used most. Note how the cell capacitor with lowest voltage (red trace) is inserted in favor of the cell capacitor with highest (cyan trace). This is in addition to the switching related to the current control that occurs later in the stroke. If the sorting order was updated outside the active part of the stroke, balancing would still be achieved without having to go through this extra switching. Therefore, another scheme is evaluated, where the sorting order is updated at a fixed rotor position, which will be referred to as θ_{sort}. Waveforms for this scheme, using $\theta_{sort} = -12°$, are illustrated in Fig. 4.25 for the same time period in Fig. 4.23. Recall that $\theta_{on} = -2°$, and so capacitor sorting order is updated 10° ahead of the start of a stroke, thus ensuring no unnecessary switching occurs during the stroke.

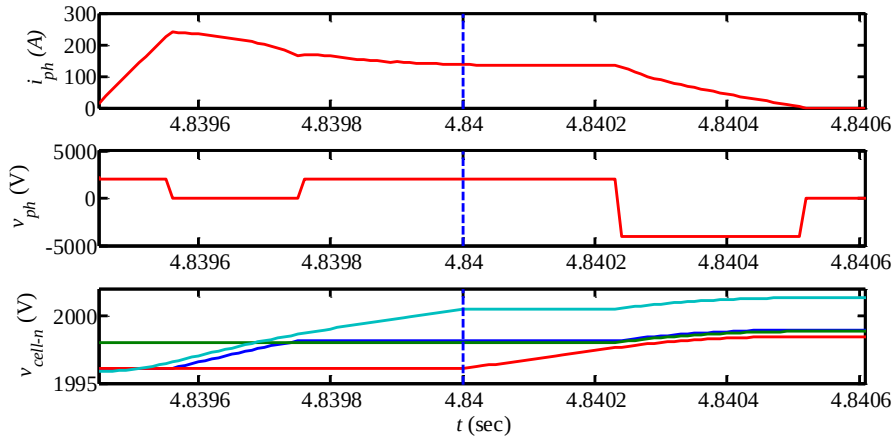


Fig. 4.24 Synchronous capacitor sorting: Sorting-related switching event occurring during active period of the stroke

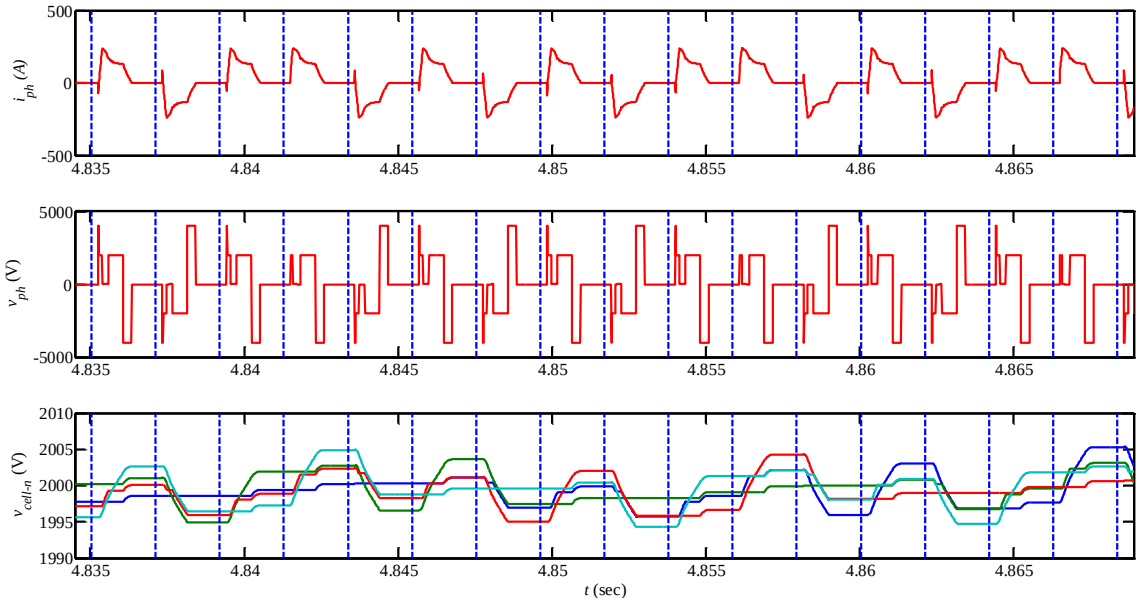


Fig. 4.25 Asynchronous capacitor sorting: Operation at 7200 r/min with $\theta_{sort} = -12°$

It is noted that the i_{ph} and v_{ph} waveforms are almost identical in both the synchronous and asynchronous cases, with only the $v_{cell\text{-}n}$ being slightly different. The parallel of Fig. 4.24, for the same time duration, is shown in Fig. 4.26. The capacitor sorting order is not updated during the active period of the stroke, and so no switching takes place except that related to the current control. Therefore, the asynchronous scheme is generally superior. However, when the speed is very low, if sorting order is only updated outside the stroke, then certain cell capacitor(s) may undergo a large increase or decrease within the stroke. Therefore, the synchronous scheme is recommended at low speeds, while the asynchronous is recommended at high speeds. The speed at which the scheme is switched depends on the maximum acceptable cell capacitor voltage ripple, which is decided by the user, and is affected by the capacitance value as well as the load torque profile.

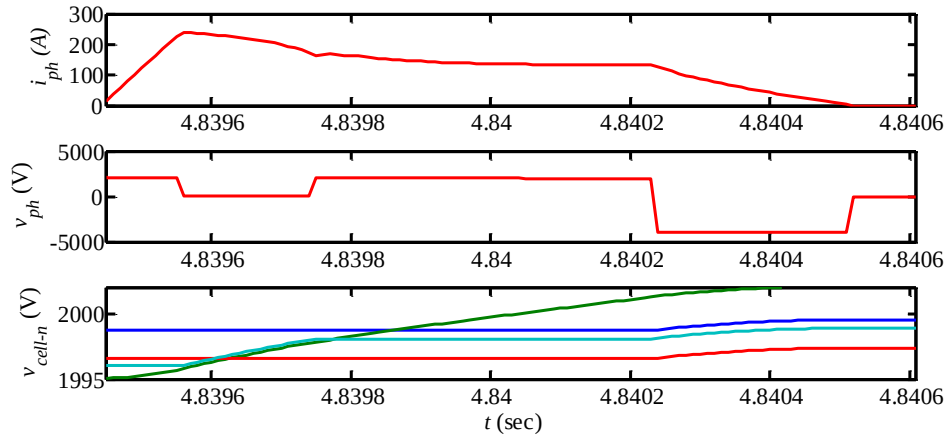


Fig. 4.26 Asynchronous capacitor sorting: No sorting-related switching events during active period of the stroke

4.5.6 Comparison with the Standard Asymmetric SRM Converter

In this final set of simulations, efficiency of the 4-cell CCC SRM converter is compared to that of the standard asymmetric converter described in chapter 1. For the loss calculations, the thermal model of the devices in the asymmetric converter are based on the ABB single-IGBT module (with anti-parallel diode) rated 6.5 kV/750 A; its ABB IGBT module number is 5SNA 0750G650300. In practice it may be desired that the device has a higher rated voltage than 6.5 kV since it will block the full 4000 V dc link voltage, but for the purpose of simulation it is deemed acceptable being the highest available IGBT choice. This is why multilevel converters are preferred above say 3.5 kV dc link voltage, or alternatively two IGBT switches may be used in series to support up to say 7 kV dc link voltage.

Performance of the two converters is compared for two scenarios. First, operation is compared at rated speed and torque, in which case both converters use only full dc link energization, and both operate exclusively in single-pulse mode. Second, operation `at 50% speed and 25% torque, reflecting a fan/compressor type load. Both converters are operated in chopping mode with the same firing angles which were chosen as $\theta_{on} = -2°$ and $\theta_{off} = 33°$. The asymmetric converter uses voltage levels V_{dc} and 0 for chopping. The 4-cell CCC converter is evaluated in two modes, first using only $\pm V_{dc}$ and 0 for chopping (full-voltage scheme), then using only $\pm V_{dc}/2$ and 0 for chopping. To maintain a fair comparison, the heat sinks were similar for both converters, and ambient temperature was the same in all simulations. Table 4.7 summarizes the results.

TABLE 4.7
COMPARING PERFORMANCE OF 4-CELL CCC SRM CONVERTER TO STANDARD ASYMMETRIC SRM CONVERTER

Converter	Operating Point	Voltage levels used during Energization	Switching Losses (kW)	Conduction Losses (kW)
Asymmetric	16790 r/min at 1069 N.m	$\pm V_{dc}$, 0	25,124	3,971
4-cell CCC	16790 r/min at 1069 N.m	$\pm V_{dc}$, 0	10,006	6,525
Asymmetric	7200 r/min at 199.2 N.m	$\pm V_{dc}$, 0	31,291	823
4-cell CCC	7200 r/min at 199.2 N.m	$\pm V_{dc}$, 0	5,859	1,473
4-cell CCC	7200 r/min at 199.2 N.m	$\pm V_{dc}/2$, 0	2,580	1,582

In the first case, both converters switch use the same voltages for chopping, yet the asymmetric converter shows significantly more switching losses than the 4-cell CCC, but less conduction losses. The reason behind this is easily understood upon inspecting the loss characteristics of the devices from the datasheets. For the 6.5kV/750A ABB IGBT, the turn-on and turn-off energy per pulse at 125°C for a blocking voltage of 4000 V and an instantaneous current of 200 A, are both estimated as 2 J. For the

3.3kV/750A ABB IGBT, the turn-on and turn-off energy per pulse at 125°C for a blocking voltage of 2000 V and an instantaneous current of 200 A are about 0.35 J and 0.6 J, respectively. The 200 A is only used here for illustration, and the trend is similar for other currents. So even though the 4-cell converter switches twice as many IGBTs as the asymmetric converter, the fact that switching energies per event are about four times higher in the asymmetric converter is what makes the difference in the switching losses large. Conduction losses on the other hand depend more on current than the voltage rating of the device or the voltage at which it is switching. This is why conduction losses are higher in the 4-cell CCC converter, since it has more devices with almost the same conduction loss per each as with the asymmetric converter. Another factor that widens the difference between the two is that the higher losses in the asymmetric converter push the temperature to a much higher level than in the 4-cell CCC (for the same ambient), which makes the losses rise even more – so it is a positive feedback process. However, in all cases the operating temperature was still below the 125°C recommended in the datasheets.

In the second case, even though the current demand is lower, the asymmetric switching losses were even higher. This is because the converter switches more. Of course the firing angles as well as switching frequency may be better optimized to limit the switching losses, and so this scenario is only used for comparison. For the same firing angles and same ambient temperature, the 4-cell CCC converter has much lower switching losses as expected, even with the full-voltage scheme. With the half-voltage scheme, the switching losses are even lower. The conduction losses are also expectedly higher in the 4-cell CCC converter due to it using more devices. The half-voltage scheme has slightly higher conduction losses than the full-voltage scheme since the phase current is slightly higher.

4.6 Summary

This chapter explained the controls of the proposed CCC converter for SRM drives, including the novel cell capacitor balancing and control algorithm, as well as standard current and speed control. Further, a novel startup algorithm was proposed that limits rise of cell capacitor voltages as well as the switching frequency in order to ensure a safe startup. A detailed simulation model was used to demonstrate operation startup and very low speed, at a medium speed, and at a high speed for a 2 MW SRM rated 16,790 r/min. Performance for several different energization schemes were simulated and compared. The following points summarize the advantages of the CCC SRM converter as well as other conclusions from this chapter:

- The availability of multiple energization voltage levels and the use of devices of lower voltage result in high efficiency and better current command tracking capability
- In comparison to the asymmetric converter driving a motor of the same size, the CCC SRM converter has significantly less switching losses, but a little higher conduction losses.

- Given its high efficiency, good performance, and high reliability, the CCC converter may also find use in sub-megawatt applications that require high performance and maximum uptime. Also at these relatively lower powers where somewhat higher frequencies switching are permitted, a lot of possibilities in terms of improving torque ripple and reducing acoustic noise are opened up.

- Key contributions in this chapter include:

    - Development of a technique for controlling and balancing the cell capacitor voltages, and suggestion and comparison of two different approaches to sorting the capacitor voltages. This is control technique is scalable to any number of cells without any modification.

    - Introduction of a suitable startup technique that both keeps the cell capacitor voltages form rising too high as well as maintains a low switching frequency

Current control using PWM with multiple carriers, or multi-band hysteresis, explained in this provides most flexibility in that they work for the complete speed range without the need for modification. However, they do not necessarily provide the best performance or best efficiency. They are well-suited for transient operation, or at low powers when high switching frequencies are possible. For multi-megawatt drives, a combination of using the lowest possible voltage levels along with adjusting the firing angles to reduce switching and hence improve efficiency may give best results. This is investigated in the next chapter, which focuses on achieving high efficiency with the CCC SRM drive.

Chapter 5

Single-Pulse Control Scheme for Efficient Operation of the Cascaded Chopper-Cell SRM Drive

5.1 Introduction

In the previous two chapters, the novel cascaded chopper-cell (CCC) converter for SRM drives and its control were developed and presented. Emphasis was placed on the control and balancing of the cell capacitor voltages at steady state and in transients, and also during startup. A brief description of speed and current control options was given, and simulation results were provided to demonstrate operation of the drive using the proposed control method. Basic design criteria for the various drive components and parameters were also discussed, along with few other relevant topics. But since work on multi-megawatt converters for SRM in general is still in its infancy, little can be found in literature about topics like efficient operation of multi-megawatt SRM converters. In an effort to contribute to that area, this chapter suggests a control scheme for achieving higher efficiencies in light of the power levels and applications targeted by the proposed CCC SRM drive. The control scheme is based on the single-pulse mode of operation, which will be explained below. The scheme features control of the turn-on angle (θ_{on}) and turn-off angle (θ_{off}), as well as energization voltage levels (EVLs), in order to achieve and maintain single-pulse operation at any speed. Furthermore, this control algorithm applies to any multilevel converter for SRM, including the cascaded asymmetric bridge multilevel SRM converter [31] that was described in chapter 2.

The simulation results provided in chapter 2 showcased the flexibility that the CCC multilevel converter for SRM provides. The availability of multiple voltage levels that allow for switching in smaller steps of dv/dt enables better tracking of the current command, while resulting in lower switching frequency per device and hence lower switching losses. This ability to closely follow the current command makes it easier to achieve various objectives like torque ripple reduction, as well as the reduction of acoustic noise that is characteristic of switched reluctance machines. However, instead of utilizing the possibility of including extra switching to reduce torque ripple and acoustic, the multilevel advantage may be used in a different way to enhance efficiency. At medium and low speeds, instead of using a high energization voltage

level (EVL) and having to chop the current in order to control torque and hence speed, if a lower EVL is used along while increasing the dwell angle ($\theta_{on} - \theta_{off}$), then higher efficiency is obtained.

5.1.1 Operation in single-pulse mode

For high-speed multi-megawatt applications which the CCC SRM converter is best suited for, such as compressors/pumps in oil and gas or water/chemicals industry, operating speeds are usually very high. The converter is forced to switch at high frequencies, and if switching is not limited, the semiconductor devices heat up quickly. This will necessitate increasing the cooling capacity as well as using switches with higher current ratings, thereby increasing the system cost. And even if the devices are thermally controlled, losses may reach very high levels and result in unacceptable efficiency levels. Also increasing the capacity of auxiliary systems, such as the cooling system, increases the overall power consumption of the drive and hence results in lower overall system efficiency.

Consider the example of the 6/4 SRM used for simulation studies in the previous chapter. The rated speed of the SRM is 16790 r/min, which is equivalent to ~ 280 revolutions per second. The rotor passes the stator four times every revolution, meaning that each phase of the three phases will be excited four times every revolution since there are four rotor poles. Assuming that the switches are turned on only at θ_{on} and then off at θ_{off}, with no switching in between, then each switch will be turned on and off at a rate of ~1120 Hz. This is already a high switching frequency current in the order of several hundred Amperes, and therefore any extra switching should be avoided. This mode in which only a single pulse of voltage is applied during every stroke is referred to as the single-pulse mode. The current and inductance waveforms in single-pulse mode are illustrated in Fig. 5.1. But with a single pulse, no chopping of current occurs, and hence no regulation of torque takes place. Therefore, another form of control needs to be used to control torque and hence speed. This is achieved through the control of θ_{on} and θ_{off}.

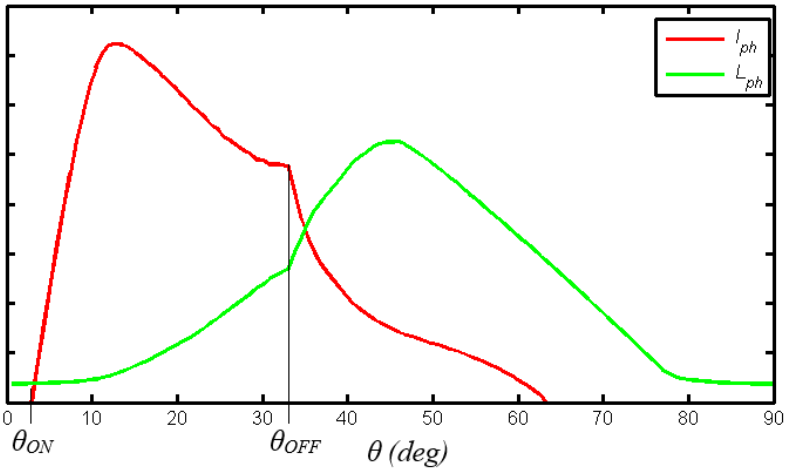
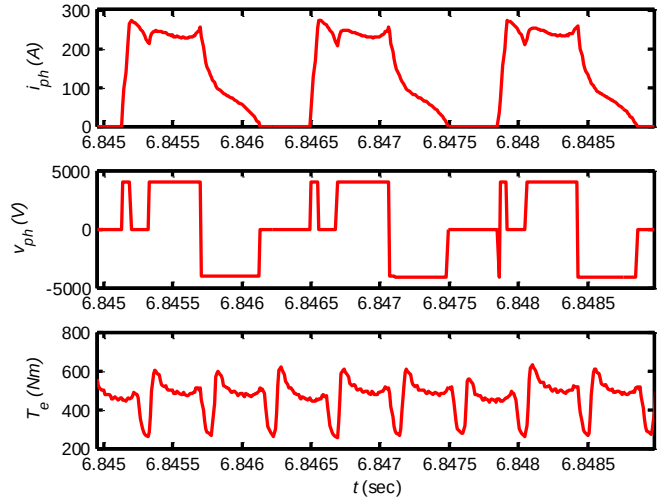
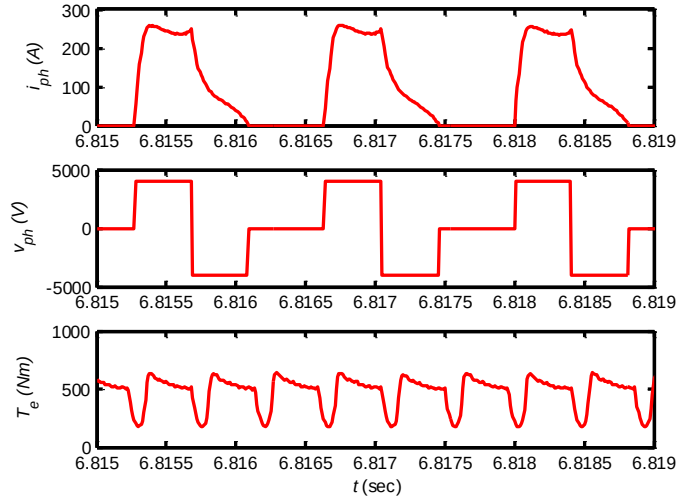


Fig. 5.1 Typical i_{ph} and L_{ph} waveforms in single pulse mode

Example simulation waveforms for both chopping mode and single-pulse mode are provided in Fig. 5.2 for the CCC SRM drive described in the previous chapter, operating at 11000 r/min. Semiconductor losses in single-pulse operation were estimated in simulation as 2.25% of the output power, whereas in chopping-mode operation they were 4.02% of the output power, and that too with only one extra pulse. This amount to ~42 kW losses in single-pulse mode as opposed to ~75 kW in chopping-mode. Torque ripple may be slightly higher in single pulse operation, and in fact adding more pulses can provide better flexibility to control torque ripple (as well as reduce acoustic noise) [8, ch. 5]. However, as earlier mentioned, if high-speed multi-megawatt applications like compressors and centrifugal pumps are the target, then low torque ripple or low acoustic noise are seldom a strict requirement.



(a)



(b)

Fig. 5.2 Waveforms for operation at 11000 r/min: (a) Chopping mode (b) Single-pulse mode

The objective of this chapter is to demonstrate efficient operation of the CCC SRM converter through the use of a methodology giving way to a controller that operates the drive in single-pulse mode, while also taking advantage of the multi-level capability using the EVL that results in best efficiency. The drive is still operated in the standard current-chopping mode during transients, but once in steady state the single-pulse mode controller smoothly transitions the drive from chopping mode to single-pulse mode. The suggested controller is adaptive in nature and hence is able to adjust to variations in the load or other changes in the characteristics of the drive. This is an important aspect of the controller, since often the θ_{on} and θ_{off} angles that produce single-pulse operation at different operating points are found by simulation or even based on experimental trials. But while this is useful as an initial step, in actual operation, the drive may operate at a slightly different speed than expected due to several factors. Such factors include load variation, tolerances in machine design, and friction and windage introduced by wear and tear. Therefore, a form of online speed control is still important even in single-pulse operation. The controller even goes beyond that, where an optional step is suggested in which after steady-state single-pulse operation is achieved, the controller slowly moves θ_{on} and θ_{off} angles while maintaining speed in search for the highest efficiency.

Section 5.2 explains the complete control methodology, and also covers other details not covered in the previous chapter like the choice of appropriate initial θ_{on} and θ_{off} angles for different operating points. Proper choice of the EVLs for different operating points is also discussed. Section 5.3 provides simulation results at various operating points, with the results covering a range of θ_{on} and θ_{off} for each operating point. Section 5.4 provides summary and analyses of results, while section 5.5 summarizes the key points of the chapter and draws some conclusions.

5.2 Control Scheme for Efficient Single-Pulse Operation of the Cascaded Chopper-Cell SRM Drive

5.2.1 Introduction

Having decided to operate in single-pulse mode, the next step is to design a controller that can ensure this through the entire speed range. In SRMs, single-pulse operation can be forced by choosing θ_{on} and θ_{off} so that the desired speed is met, without having to apply any current control. But several concerns arise in single-pulse operation:

- First, at low speeds a very large instantaneous current develops if the full dc link voltage is used for energization, which could exceed the peak current limitation of the device. Exceeding this rating could lead to device turn-off failures, and possible over-heating of the device. The CCC multilevel SRM converter, and in fact any other similar multilevel converter, has the advantage of being able to energize the phase using lower EVLs, which overcomes this problem.

- Second, even though the single-pulse mode is more efficient than the chopping mode, applying single-pulse mode with a lower EVL in the CCC converter results in lower switching losses than applying it with a higher EVL. This is because the former uses less devices. Also while average current is expected to increase with the lower EVL, again the fact that less devices are engaged is likely to result in less device conduction losses as well.

- Third, even with single-pulse mode, the higher the EVL the larger the current is likely to be at the instant of turn-off or commutation. Using its multilevel capability, the CCC SRM converter can operate in single-pulse mode with a lower EVL at lower speeds and/or lower torque. The resulting phase current is then expected to be lower at commutation, which further contributes to the reduction of the switching losses.

- Another lesser concern is that even with using low EVLs, at very low speeds if the torque demand is low, the pulses are so narrow that there exist short periods when the total developed torque of the drive is zero. This occurs due to the lack of overlap of phase torque contributions from the different phases. This makes the speed response more oscillatory, though for large drives these oscillations are less pronounced and are filtered out quickly. This can be reduced to some extent by using a de-energization voltage of smaller magnitude, which elongates the tail of the current, and hence provides a more continuous torque profile. Traditional drives can only demagnetize with 0 V or full negative dc link voltage. If the 0 V level is used, then the tail current may extend too far and enter the negative torque region for that phase, but the CCC SRM converter can demagnetize at various levels between 0 V and the full negative dc link voltage. An examples where low torque occurs at low speed is in fan/compressor loads where the torque is a proportional to the square of the speed.

Finally, an important point to note is that while lower EVL in single-pulse mode is expected to result in lower semiconductor losses than a higher EVL in single-pulse mode, not always does the former result in higher overall efficiency. If too low an EVL is used, the dwell angle ($\theta_{on} - \theta_{off}$) needs to be very wide. If θ_{on} has to be advanced a few degrees ahead of the $\theta = 0°$ position, a negative torque contribution from this phase will be initially produced. To meet the average torque requirement per stroke, more current is developed in the later part of the stroke to overcome the reduction due to this negative initial component. The increased current results in higher copper losses and hence a reduction in overall efficiency. Therefore, the control scheme should also take into account this factor and choose the best EVL accordingly.

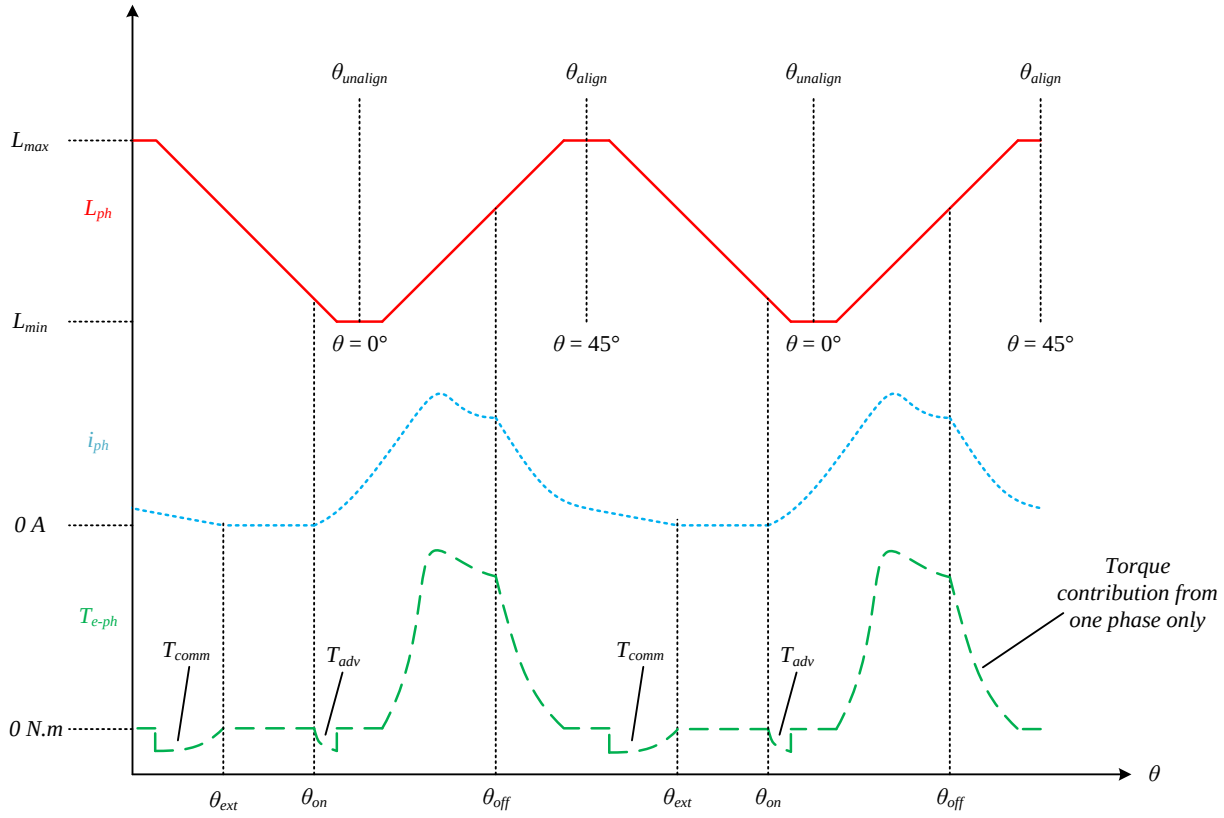


Fig. 5.3 Typical waveforms for i_{ph}, L_{ph}, and individual phase torque ($T_{e\text{-}ph}$) in single pulse mode

5.2.2 Criteria for choosing best EVL

Before discussing the controls that lead to operation in single-pulse, first the EVL to be used at the different operation points need to be predetermined. Since the goal of this control scheme is to achieve high efficiency, various losses in the drive need to be estimated to come up with an efficiency figure. The EVL producing the best efficiency at an operating point is then adopted. Peak phase current must also be monitored to ensure that it does not exceed the rated current of the chosen device, is a possibility at a combination of low speed and torque and a high EVL in single-pulse mode. But with SRM drives, information like losses, current levels, etc. is difficult to obtain by analytical means due to the highly non-linear nature of the SRM. Simulation or experimental analysis is therefore needed. In this work, simulation is adopted. In the later part of this chapter, after the control has been described, simulation results will be provided for various operating points. The same 2 MW three-phase 6/4 SRM used in chapter 4 will be considered for these simulations. For each operating point, the following is calculated and reported:

- $\boldsymbol{I_{avg}}$ (average absolute phase current): This is an important figure and gives a direct indication of device conduction losses as well as machine copper losses. Absolute current is used since current can be either positive or negative in the CCC SRM converter.

- $\boldsymbol{I_{pk}}$ (peak absolute phase current): This is an important figure to watch, especially at low speeds where in single-pulse mode large current may develop with large energization voltages. Absolute current is used since current can be either positive or negative in the CCC SRM converter.

- $\boldsymbol{P_{sw}}$ (CCC converter device switching losses): Total switching losses of all devices, including IGBTs and diodes, in all three phases.

- $\boldsymbol{P_{cond}}$ (CCC converter device conduction losses): Total conduction losses of all devices, including IGBTs and diodes, in all three phases.

- $\boldsymbol{P_{cu}}$ (SRM copper losses): Total copper losses in all three phases.

- $\boldsymbol{P_{adv}}$: This represents the power that is unnecessarily expended due to advancing θ_{on} before $\theta = 0°$. This power is not lost, but rather circulates between the dc-link/front-end and the motor-end converter. This concept is illustrated in Fig. 5.3. A negative torque contribution from the subject phase is generated when θ_{on} is advanced before $\theta = 0°$; it is labeled T_{adv} in Fig. 5.3. The area between the T_{adv} portion and the $T_e = 0$ N.m line gives the (magnitude) of the energy sent back to the dc-link/front-end. An equal amount of energy is generated by the SRM in the same stroke to compensate for this negative torque. P_{adv} is the time average of both of these energies. P_{adv} may be easily calculated in simulation as follows. First the product of the operating speed and the average the torque due to this negative portion over a long period of time, e.g. 1 s, is computed. The result is multiplied by 2, since the same amount of energy needs to be generated to compensate for the negative torque. Finally, the answer is multiplied by 3 to account for the three phases, to give P_{adv}.

- $\boldsymbol{P_{comm}}$: This represents another form of losses related to negative torque. Often at high speeds the current phase current does not decay to zero before the rotor pole has started moving away from alignment with the stator pole. The energized stator tries to effectively pull back the rotor, thereby resulting in a negative torque contribution from that phase. This is also illustrated in Fig. 5.3, where this portion of negative torque due to late current extinction is labeled as T_{comm}. P_{comm} is calculated in simulation in the same way as P_{adv}. The torque due to this negative portion is averaged over a long period of time (e.g. 1 s), then multiplied by the operating speed. The result is then multiplied by 2 since the same amount of energy needs to be generated to compensate for this negative torque. Finally, the answer is multiplied by 3 to account for the three phases, which gives P_{comm}.

- $\boldsymbol{\eta_c}$ (converter efficiency): This is the efficiency of the converter alone. Let P_{mech} be the mechanical power developed. Also let P_{fric} represent the frictional losses, given by $B\omega^2$. η_c is given by $(P_{mech} + P_{cu} + P_{fric})/(P_{mech} + P_{cu} + P_{fric} + P_{cond} + P_{sw})$ x 100%.

- η' (converter efficiency): This is the overall efficiency calculated based on the losses above. It is given by $P_{mech}/(P_{mech} + P_{cu} + P_{fric} + P_{cond} + P_{sw})$ x 100%. The prime sign is used to indicate that some losses are not accounted for in this figure. These include machine stator and rotor iron losses, also referred to as core losses. These losses represent about 1.5% of the total power at rated operating conditions [14]. Such losses are difficult to estimate analytically, and typically require finite element simulations, which are time consuming. However, core losses in general increase with current, but are also reduced when lower *dv*/*dt* steps are used, i.e., by using a lower EVL. Therefore, since the goal of these simulations is to compare different EVLs at a given operating point, the fact that going from a higher EVL to a lower EVL increases current but decreases the *dv*/*dt* step, the core losses are not expected to vary by much.

5.2.3 CCC converter used in the design example

To best explain the control strategy, it is illustrated with the aid of an example system. The same 2MW 6/4 SRM described in chapter 4 is considered, but driven by an 8-cell CCC converter as opposed to the 4-cell version used in the chapter 4. This is done to better demonstrate the flexibility that the multilevel CCC converter offers, as the 8-cell version produces more EVLs than a 4-cell. With the 8-cell CCC converter, possible voltage levels are $\pm V_{dc}$, $\pm 0.75V_{dc}$, $\pm 0.5V_{dc}$, $\pm 0.25V_{dc}$, and 0. On the other hand, a 4-cell CCC converter can only provide $\pm V_{dc}$, $\pm 0.5V_{dc}$, and 0. Also, in the 8-cell CCC converter, each cell capacitor is controlled to only $0.25V_{dc}$, while in the 4-cell CCC converter the nominal cell capacitor voltage was $0.5V_{dc}$. A few example operating points are simulated, and the EVL producing the best efficiency is chosen for implementation in the control algorithm. Hence the simulation stage is one of the steps of the control design. Simulated speeds, in percentage of rated speed, are 25%, 50%, 75%, 100%, 110%, and 120%. At 100% speed, only rated power operation is simulated. At speeds above rated, i.e. 110% and 120%, the simulated load torque is proportionately reduced in order to maintain the maximum output power at the rated value. For the lower speeds, two different operating points are considered, namely a constant 100% torque load, and a fan/compressor type load. The same quadratic torque-speed profile for the fan/compressor type load that was described in the previous chapter is used here.

5.2.4 Overview of control strategy

A quick overview of the control algorithm is first provided before each step is explained in detail:

1. Simulations using the single-pulse mode are first performed to evaluate efficiency at various operating points. For each operating point, all feasible EVLs are simulated to judge which one produces the best efficiency. But also for each EVL at every operating point, several combinations of θ_{on} and θ_{off} are used, and the ones that result in the best efficiency are also recorded. The best EVL for each operating point,

along with the θ_{on}/θ_{off} pair that gives the best efficiency in simulation is stored in the controller. These will be the settings applied by the controller when it switches to single-pulse mode.

2. Next, the θ_{on} and θ_{off} values that the drive should use as it accelerates through the entire speed range should be determined. In the previous step, the θ_{on} and θ_{off} for single-pulse mode were determined. Using the same EVL, any lower θ_{on} value while keeping θ_{off} the same will allow the drive to accelerate beyond that speed. A set of θ_{on} values that are comfortably lower than the single-pulse mode θ_{on} is formed and stored in the controller. Let this set be called the "acceleration θ_{on}" set.

3. The 3 steps above complete the offline control design stage. The drive is initially operated in current-chopping mode based controlled mode based on the θ_{on}/θ_{off} choices from step 2. The milt-carrier PWM or multi-band hysteresis current control described in chapter 4 could be used. This current-controlled mode is also defaulted to whenever a step change in speed or torque is required, or for example when a disturbance occurs that alters the drive speed significantly for more than a minimum pre-set time. Once in steady state at the commanded speed, the drive is switched to the desired EVL stored from step 1. Current is still controlled through chopping, but the drive is forced to only use the desired EVL.

4. Next, with θ_{off} held constant, θ_{on} is incremented in a systematic way. At the right moment, which will be explained later, the speed control mode is switched form current reference output to θ_{on} reference output, while simultaneously increasing the reference current command to a high but safe level. This guarantees single-pulse operation, as will be demonstrated in the explanation of this step.

5. By step 3, majority of the performance gains will have been achieved. An extra step may be performed where θ_{off} is slowly varied in predefined increments, each time allowing the speed controller to settle on the new θ_{on}. Efficiency is evaluated online, and the drive is settled on the θ_{on}/θ_{off} pair that gives the best efficiency. This step may take from one minute to several minutes in large drives, and so is not feasible in drives that operate for short intervals, or drives that go through transients very frequently. However, it may be feasible in high power compressors, pumps, fans, etc. that may be run continuously at the same operating point for many hours.

5.2.5 Explanation of steps

A detailed explanation of each step now follows. Simulation results and their analyses are postponed to the two sections that follow.

***Step 1:** Choosing the best EVLs and corresponding θ_{on}/θ_{off} pairs (offline step)*

While only full dc link voltage, V_{dc}, will sustain operation at high speeds, at lower speeds lower EVLs may alternatively be used in single-pulse operation, sometimes resulting in better efficiencies. Simulations are performed for various operating points, considering the load profiles mentioned earlier. At

each operating point, all feasible energization voltage levels are simulated. The EVLs that were determined as feasible from simulation are listed in Table 3.1.

Further, for a given operating point with a given EVL, several combinations of θ_{on} and θ_{off} are used. Post-simulation analysis of the results to calculate efficiency in every case is performed. The procedure followed for varying θ_{on}/θ_{off} is to vary θ_{off} in 1° increments and allow the control to find the θ_{on} that produces single-pulse mode. For every operating point, the combination of EVL and the corresponding θ_{on}/θ_{off} that give the best efficiency are stored in the controller. If two EVLs give the same efficiency, the one with a lower $P_{adv} + P_{comm}$ is chosen. The set of θ_{on}/θ_{off} for single-pulse operation will be referred to from hereon as the "single-pulse θ_{on}/θ_{off} set". Note that while the single-pulse θ_{on}/θ_{off} set attains single-pulse mode in simulation, due to discrepancy between simulation and practice it may not be assumed that such set will always result in single-pulse operation in practice. But as will be explained later, these values are not depended on but rather only used for initial guidance. The control algorithm is designed to find the θ_{on} that produces single-pulse operation, and is also able to adapt to disturbances and or changes in the system parameters over time such as due to friction/windage introduced by wear and tear.

TABLE 3.1
POSSIBLE ENERGIZATION VOLTAGES AT DIFFERENT OPERATING POINTS FOR THE 8-CELL CCC SRM DRIVE

Speed (% of rated)	**Fan/Compressor Load** (torque prop. to ω^2)	**Constant-Torque Load** (fixed at 100% torque)
25%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$
50%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$
75%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$	V_{dc}, $0.75V_{dc}$
100%	V_{dc}	V_{dc}

It is noted that the voltage levels in Table 3.1 are only given for a few speeds. This works if the drive is known to operate at and around a few discrete speeds, as then any neighboring speed can use the same EVL and θ_{on}/θ_{off} of the nearest stored speed. But if the operation speeds are not discrete and are unknown, ranges of speeds may be entered into the controller along with the appropriate voltage levels.

Step 2: *Choosing θ_{on}/θ_{off} pairs for acceleration (offline step)*

The θ_{on} and θ_{off}, chosen in step 1 for single-pulse mode represent the smallest dwell angle that the drive can have to stay at a given operating speed and a given EVL. To increase the speed, either a higher EVL is to be applied, or the dwell angle must be increased. Since in some case the highest EVL is already the choice at that speed, the only other option is to increase the dwell angle. Therefore, to guarantee that drive is able to accelerate through the entire speed range, a set of θ_{on} and θ_{off} must be defined throughout the range that is comfortable wider than the θ_{on}/θ_{off} that produce single-pulse at every speed. Since it is

enough to change one of the two angles, it is chosen to lower θ_{on} while keeping the same θ_{off} as that from the single-pulse set. This set is called "θ_{on} acceleration set". The sketch in Fig. 5.4 shows how such set may be obtained. First the single-pulse θ_{on} set obtained from simulation is plotted. In Fig. 5.4, red diamond markers are for the single-pulse θ_{on} set for the 100% load torque profile, while the blue diamond markers are for the single-pulse θ_{on} set for the fan/compressor load torque profile. The points at 110% and 120% speed are shown differently in green diamond markers because they do not follow either torque profile; rather, they operate at a reduced torque in order not to exceed the rated operating power of the drive. These plotted values are based on values obtained from simulation for the EVLs that produced the best efficiencies.

Next, a line is drawn in each a case that is a few degrees below the single-pulse θ_{on} set. The red dashed line marks the θ_{on} acceleration set for the 100% load torque profile, while the dashed blue line marks the θ_{on} acceleration set for the fan/compressor load torque profile. Accuracy is not at all required in this step. The idea is to only provide a θ_{on} set that allows the drive to accelerate through the speed range, and to also serve as initial values at steady state before the drive is transitioned into the single-pulse mode. It is important to choose a θ_{on} set that provides a wide enough dwell angle, not only to account for possible difference between simulation and practice, but also to allow for faster acceleration when needed. If this criteria is followed, then at any steady state speed the drive will be in chopping mode, initially. As for the θ_{off} values, the same ones from step 1 that make up the single-pulse θ_{on}/θ_{off} set are used.

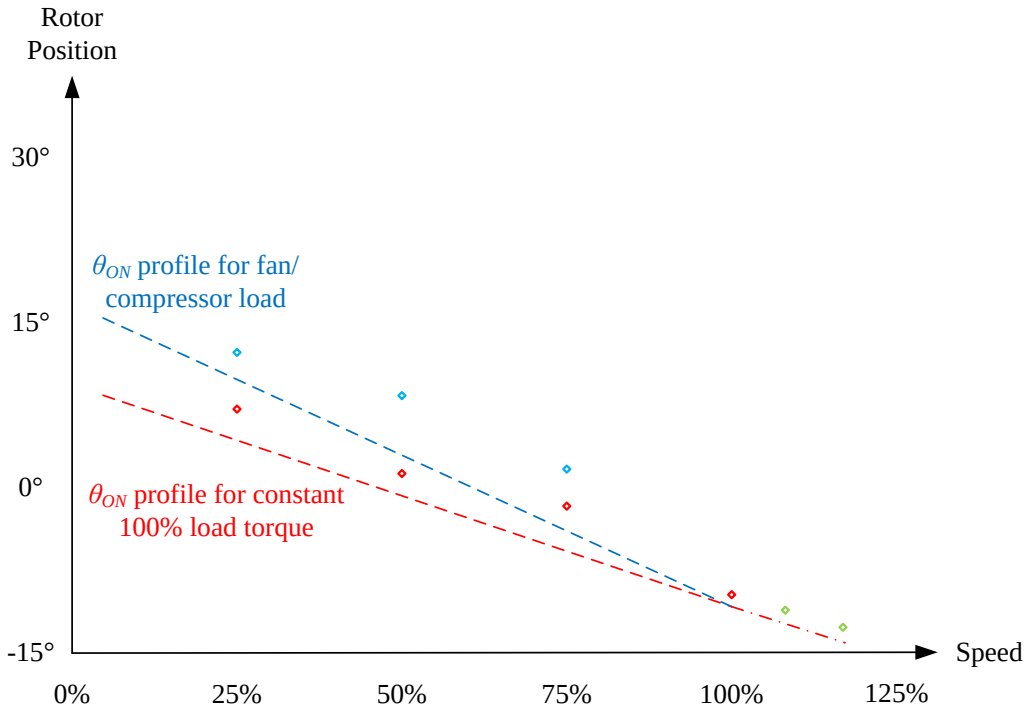


Fig. 5.4 Obtaining the θ_{on} acceleration set for the two different load torque profiles

Next, the derived θ_{on} acceleration sets should be tested in simulation to see if they provide the desired acceleration rate. For example, for the considered drive with a rated speed of 16790 r/min, if the drive is to reach the rated speed in no more than three minutes or 180 seconds, which is equivalent to an average acceleration of rate of 16790/180 or 93.3 r/min/s, then in simulation an acceleration rate of say 100 r/min/s should be achieved. If the drive produces less than the desired acceleration, the θ_{on} acceleration set is further lowered and then tested again in simulation, and so on until the desired acceleration rate is achieved.

Finally, a note is worth making about why it was chosen to vary θ_{on} and keep θ_{off} constant and not the opposite. While the reverse would work, there tends to be less flexibility in how much θ_{off} can be varied. The reason is that if θ_{off} is pushed too far then a large component of negative torque per phase will be generated. On the other hand, it θ_{off} is advanced by much, a large period of motoring torque generation will be missed. Therefore θ_{off} for best efficiency usually comes out to be in the range from 25° to 30° for a 6/4 machine with three phases – except at very low speeds where it could be pushed further.

Step 3: *Starting drive and switching to the desired EVL (online step)*

The previous steps covered the offline part of the controller design. With all the necessary information available and stored in the controller, the drive is now operated. The startup phase was explained in detail in chapter 4, and may be used up to around 1% to 3% of the drive speed, or whenever the capacitor cell voltages are within their nominal control range. Then the drive is switched to regular PI speed control with a current reference output enforced through chipping. Any of the current controllers discussed in chapter 4, namely PI + PWM or multi-band hysteresis, can be used. As the drive accelerates, the θ_{on} values are obtained from the stored θ_{on} acceleration set. The θ_{off} values, as mentioned above, are taken as the same θ_{off} are from the single-pulse set.

Once the drive has reached the commanded speed, it is time to switch to the desired EVL. When the speed has spent a pre-defined amount of time around the steady-state speed, the stored EVL for that gives the best efficiency is applied. The speed may be considered steady as long as it remains within a certain pre-defined percentage of the target speed, referred to as *sss band* from hereon. If the applied EVL is different from the EVL or EVL combination applied by the current controller, the drive will experience a transient as the PI speed controller takes time to correct its reference current output to match the new EVL.

Step 4: *Gradually switching to single pulse mode after reaching steady state (online step)*

After successfully switching to the desired EVL, the final step is to switch to single-pulse operation. A counter for steady state speed, which will be referred to as *sss counter*, is used by the controller for this purpose. The settling period for the speed, set by the user, will be referred to as *sss period*. The controller

also needs to signal every time a pulse occurs in any phase, i.e., every time there is chopping of current. A simple way of detecting this is to activate a flag or variable (digital 1) whenever current exceeds the upper hysteresis limit, or equivalently when the carrier signal rises above the duty cycle. Then the steps to achieving single-pulse operation are as follows:

1. While still controlling speed via setting a reference current, the *sss counter* starts counting as soon as the speed is within the *sss band*. When one *sss period* has elapsed, and as soon as the first pulse is detected, θ_{on} is increased by a predefined increment. The PI speed controller will adjust to the reduction of the dwell angle, (θ_{off}–θ_{on}), by changing its reference current output to maintain the commanded speed. It may be thought that the reference current would increase since the dwell time has been shortened, but often times it will increase. This is because with a smaller dwell angle, chopping does not happen too early, thereby allowing more torque to develop before the first chopping instant.

2. After every θ_{on} increment, the *sss counter* is reset and will not start counting until the speed returns to the *sss band*. This allows the drive to settle once again at the commanded speed. When the *sss counter* completes a second *sss period* at steady state, it waits for the next pulse form the pulse detector. Upon receiving the pulse, a second increment to θ_{on} is applied, and so on. Note that chopping of current is only happening because there is too much current in one stroke, so naturally as the dwell time is reduced, a point will come where chopping will cease.

3. Depending on the size of the increment, at some point after one of the increment cycles, the speed will very likely drop a few r/min below the commanded speed and settle there. This signals that the drive has surely entered into single-pulse mode, as otherwise the drive would not settle at the lower speed. This is because the conduction window has become so small that the phase current is not even reaching the current commanded by the speed controller – in fact the speed controller's output will saturate at its limit after some time.

4. After some time has elapsed with the drive's speed not returning to the commanded speed, the current reference is increased to a high but safe value. This could be the, for example, 125% of the saturation limit of the PI speed controller output reference. This ensures that chopping does not occur again. At the same instant, the PI speed controller is switched from outputting a reference current to outputting a reference θ_{on}, i.e., another PI controller is used. This controller will automatically advance θ_{on} until the commanded speed is achieved again. Note that even with the PI speed control switched to output a θ_{on} reference, in the unlikely event that current rises to the new high reference current, a chopping should still occur, for example by using a single-band hysteresis controller that switches between the chosen EVL and 0 V.

It should be noted that if the size of the θ_{on} increment is very small, there is a minor possibility that drive would enter single-pulse mode at some point after several increments. However, it is nevertheless always better to switch speed control through θ_{on}. First, this allows the drive to adapt to any disturbance, second it allows θ_{on} to be continuously adjusted, though within a very small radius, to cater to minor fluctuations in the cell capacitor voltages or the dc link.

With regards to the size of the θ_{on} increment, larger increments result in a faster transition to single-pulse operation, but too large an increment will result in a larger transient at the moment when speed control is switched to command a reference θ_{on}, as will be demonstrated below. On the other hand, very small increments may take the drive too long to switch to single-pulse mode, e.g. one minute in the considered drive, though this may not be an issue if the drive is to operate for many hours at a given speed. Also it was found that often several successive small increments were required to push the speed out of the *sss band*, which amounts to the same as applying one larger increment. Therefore, there is no particular advantage for using a very small increment. It was found from simulation that a θ_{on} increment between 0.05° to 0.15° is suitable for the considered drive.

Fig. 5.5 shows a simulation of the complete process of step 5, again for a 75% speed command with 100% load torque. The drive's speed (ω), reference current (i_{ref}), θ_{on}, and *sss counter* are all plotted. The *sss counter* starts counting from $t = 0$ since the simulation is started at the commanded speed that is shown in blue – and which is 75% of the 16790 r/min rated speed, or 12592.5 r/min. The *sss band* was defined as 0.5 r/min, while the *sss period* was set as 0.5 s. The speed response does not experience much transients for the initial θ_{on} increments, but as the conduction window gets narrower the transients become more pronounced. Note that for some short intervals the *sss counter* stops counting. This happens when the speed has risen above the *sss band*; the *sss counter* only resumes after the speed returns to within the *sss band*. Also note how speed starts dropping below the commanded speed after the last increment, and how it is brought back to the commanded speed through action of the PI speed controller through adjusting θ_{on}. Finally, note how the current reference is increased to a large value, which is not shown in the figure but is 125% of the saturation limit given by 800 A. Keeping this current limit enforced is done to ensure safe operation of the drive, though it is kept quite high to ensure single-pulse operation under normal circumstances.

The θ_{on} increment used in this example was 0.2°, and the initial of θ_{on} was −10°. The controller finally settles on a θ_{on} of −7.92°. The whole process took about 10 seconds only, which is almost unnoticeable for a drive that is to operate for hours at the same speed. As mentioned above, the transient at the point where speed control through θ_{on} is applied may be reduced by reducing the size of the θ_{on} increment. Fig. 5.6 shows the same process at the same conditions but with a θ_{on} increment size of 0.1°.

Since the overall process is expected to be slower with the smaller increment size, the *sss band* was reduced to 0.35 r/min, and the *sss period* was also reduced to 0.35 s. Reduction in the speed transient at the point where speed control through θ_{on} is applied is noted.

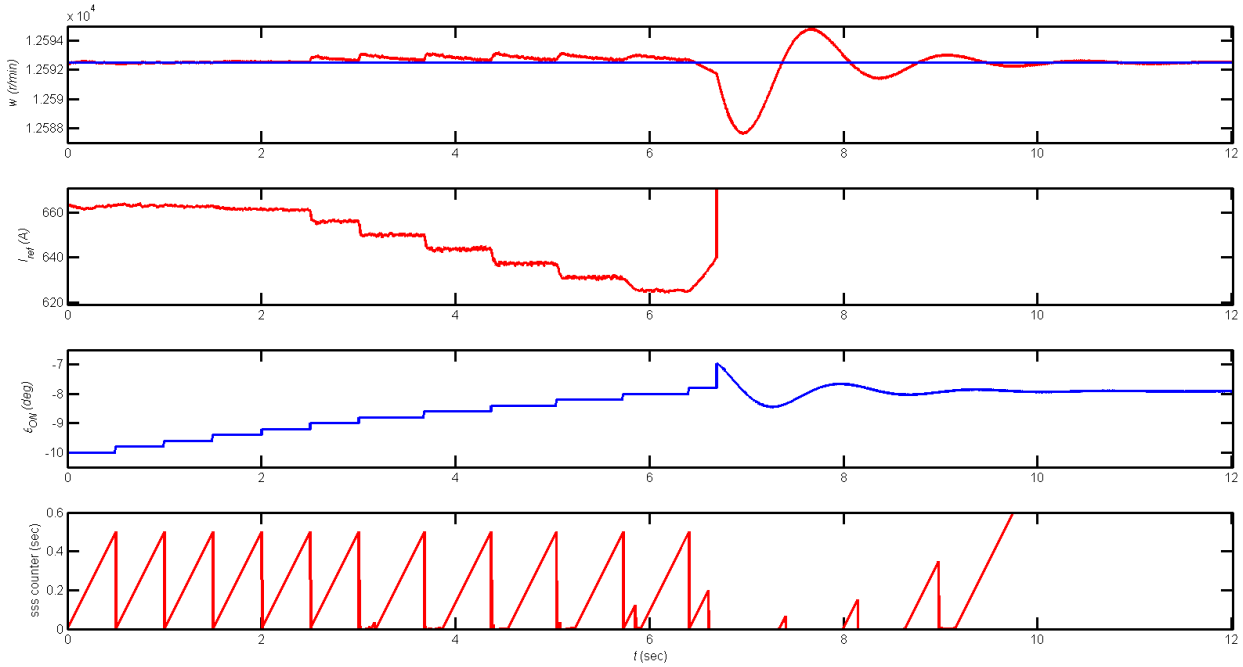


Fig. 5.5 Transitioning 8-cell CCC SRM Drive from chopping mode to single-pulse mode

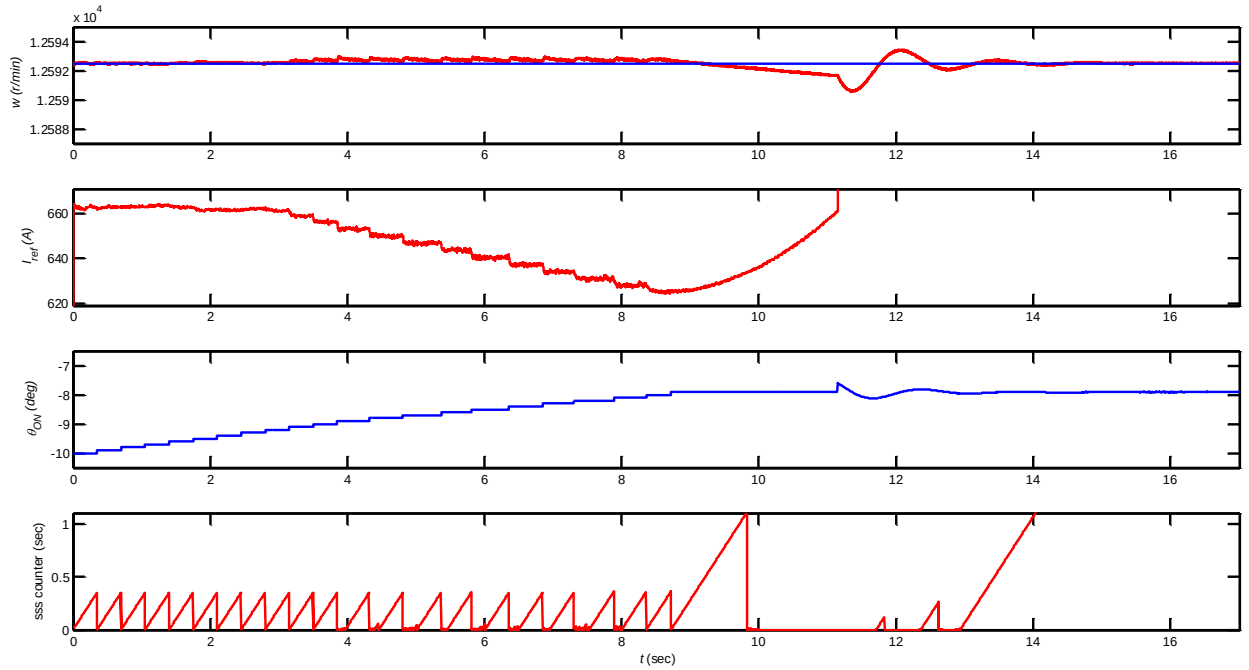
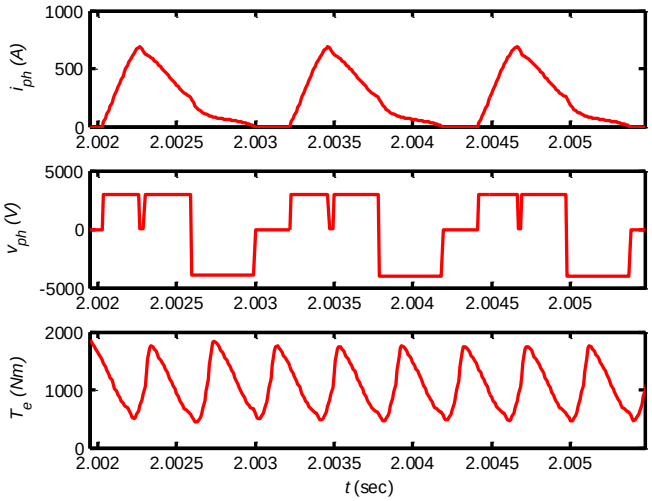
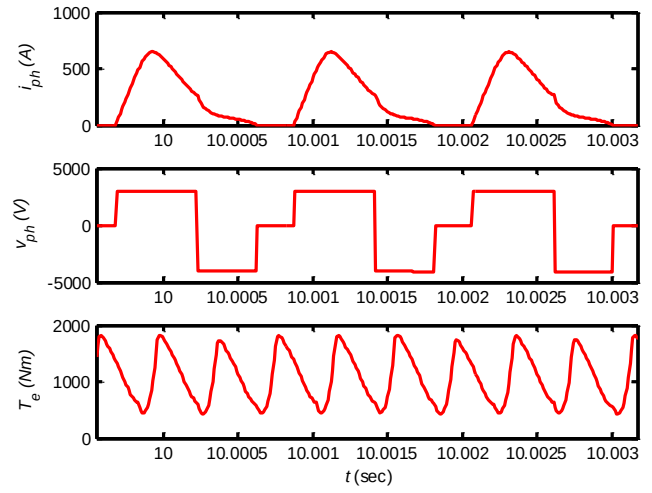


Fig. 5.6 Transitioning from chopping mode to single-pulse mode with a reduced θ_{ON} increment size



(a)



(b)

Fig. 5.7 8-cell CCC SRM Drive at 75% speed and 100% torque: (a) Chopping mode, (b) Single-pulse mode

TABLE 3.2
COMPARING PERFORMANCE AT DIFFERENT POINTS FOR WAVEFORMS IN FIG. 5.6

75% RATED SPEED, FULL RATED TORQUE, 0.75V_{DC} ENERGIZATION VOLTAGE, θ_{OFF} = 33°

Time Interval (s)	θ_{on} (°)	Total # of current chops in all phases (excluding those occurring at θ_{OFF}) for specified time interval	$P_{cond} + P_{sw}$ (kW)	I_{avg} (A)	I_{pk} (A)
[0.50, 0.95]	-9.80	88542	26931	234.92	696.43
[3.75, 4.20]	-8.60	35829	21996	225.49	674.73
[5.80, 6.25]	-8.00	5373	17484	220.98	656.06
[9.75, 10.00]	-7.93	0	16638	220.77	654.64

Next, Fig. 5.7 shows screenshots of the phase current and voltage, as well as total torque at two different times; Fig. 5.7 (a) is while the drive is still in chopping-mode, while Fig. 5.7 (b) is when the drive has entered into single-pulse mode. Table 3.2 provides performance figures for several different time intervals, where the last interval represents single-pulse mode operation. It can be seen how the total semiconductor losses, $P_{cond} + P_{sw}$, improve as the dwell angle is reduced and the number switching events are consequently reduced. In fact, when single-pulse operation has almost arrived, switching events will only occur when the energization voltage, which naturally fluctuates due to cell capacitor voltage fluctuation, is closer to its peak.

An alternative approach to transitioning gradually approaching to single-pulse mode is to switch to the PI controller with θ_{on} output as soon as the drive has reached the commanded speed. While this approach is valid, the transient may be large at the time of switching controllers. With multi-megawatt drives being a potential application, limiting over-current transients as much as possible is highly preferred. Also in some cases, during the transient in switching controllers, the drive may settle at a θ_{on} where operation is not in single-pulse! This would happen if that over-current transient is large that it reaches the new high current limit. This will force the safety single-band hysteresis controller to chop the current. If commanded speed is encountered while chopping at that high current is still taking place, the controller will lock into this state, even though it is not single-pulse.

Step 5: *Slowly shifting conduction window to find best* θ_{on}/θ_{off} pair *(online step)*

Having achieved single-pulse operation at the voltage level that was found to achieve the best performance in simulation, a further step of varying θ_{off} while allowing the speed controller to adjust θ_{on} may be performed. After every increment, efficiency may be calculated online. A certain pre-defined range may be spanned, and after it is completely swept, the controller is gradually returned to the θ_{on}/θ_{off} that was found to give best efficiency. Simulations in the next section show results for several different θ_{off} choices at every operating point for every EVL, which can be used to guide the range of θ_{off} to span in this process.

While this step is optional, it helps to further optimize the drive's efficiency. As mentioned earlier, while such step is not feasible in drives that do not operate continuously for long periods of time and/or that change speed and/or torque often, it is feasible and rather beneficial in high power drives that do meet that criteria, such as compressors, pumps, and fans in some applications. However, even if this step is not performed, the majority of the performance gains will have been achieved anyway.

So in summary, the procedure outlined above provides a complete system on how to manage all the control variables available in a CCC SRM, namely the θ_{on}/θ_{off} as well EVL, through all stages of the drive's operation. The goal of this procedure is not only to control the drive's speed, but also ensure high efficiency, while having the ability to adapt to disturbance such as load variances, or to changes in the

drive's parameters over time such as change in friction/windage. The complete procedure is summarized in the flowchart in Fig. 5.8. The control diagram is shown in Fig. 5.9; it shows the three major components of the control system, namely the cell capacitor balancing and control, speed and current control through current-chopping with PI + PWM current control, and speed and current control through single-pulse mode angle control. The diagram also indicates which signals are to be measured, and which are the rotor position and speed, phase current, and the cell capacitor voltages. The transitioning algorithm that switches the drive from chopping mode is not shown for simplicity. The gate signal generator block produces the appropriate gate signals based on the measured θ and i_{ph}, and also based on whether the drive is operating in chopping mode where the EVL depends on the duty and PWM, or in single-pulse mode where the EVL is fixed for a given operating point.

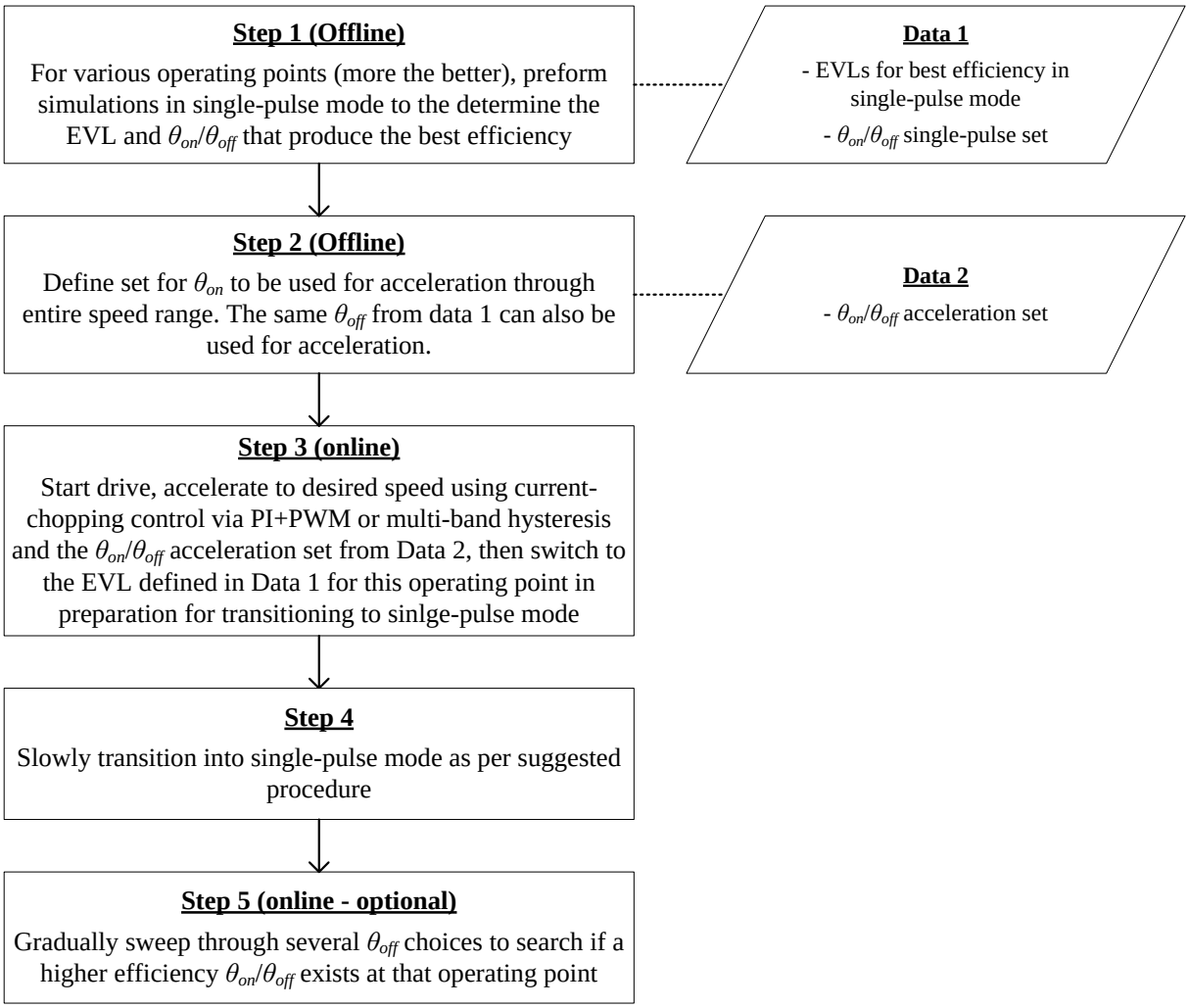


Fig. 5.8 Summary of control procedure for single-pulse operation of CCC SRM drive (or any similar multilevel SRM drive)

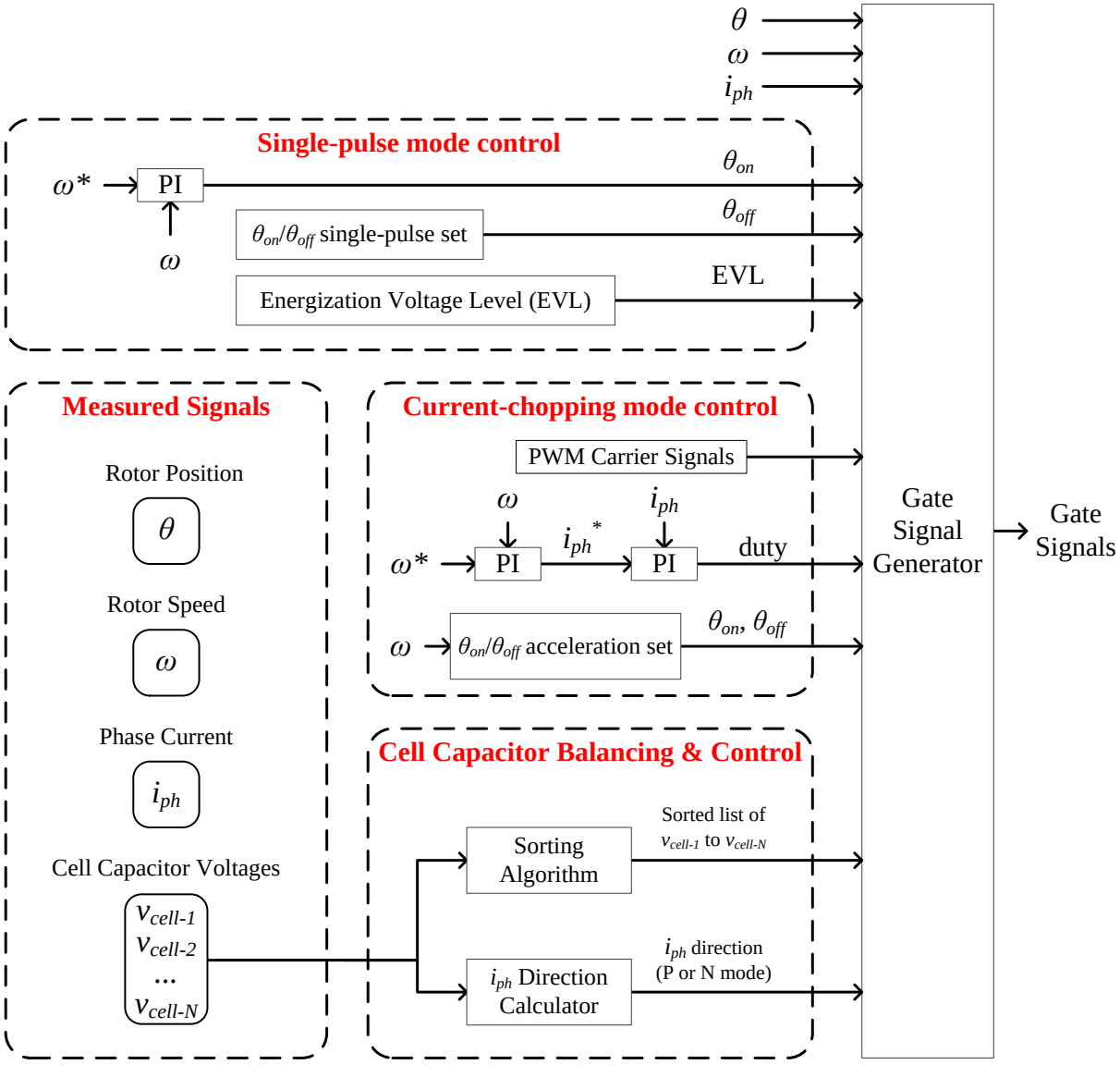


Fig. 5.9 Control system of the CCC SRM converter drive system including single-pulse controller

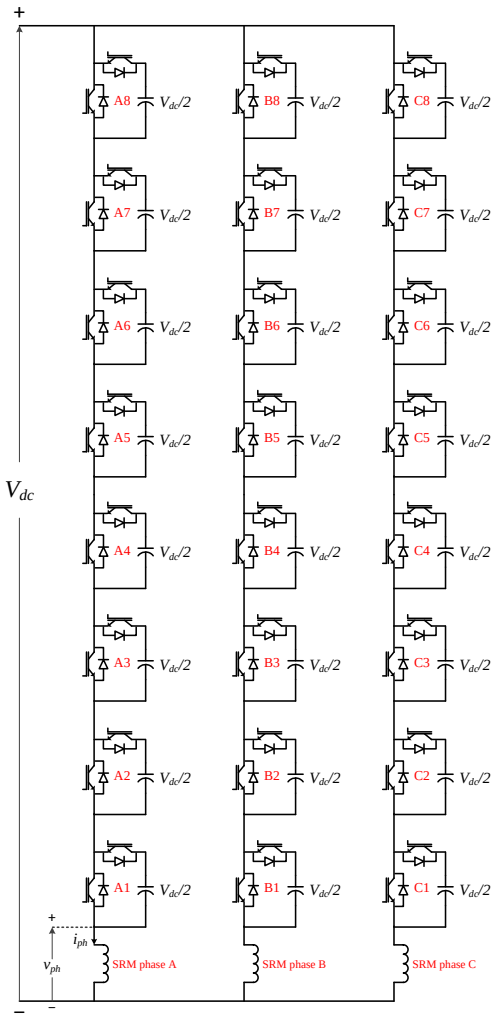


Fig. 5.10 8-cell CCC converter for a three-phase SRM

5.3 Simulation Results for Single-Pulse Operation of the 8-cell CCC SRM Drive

This section provides simulation results for operation of the CCC SRM drive in single-pulse mode. As earlier mentioned, simulations are based on the 2MW 6/4 SRM described in detail in chapter 4, and using the same simulation model, only with the difference that an 8-cell CCC converter is used in place of the 4-cell version. The 8-cell CCC converter is shown in Fig. 5.10. Table 3.3 summarizes all the cases for which results are presented. Each case represents one operating point at a certain EVL. For example 50% speed at 100% load torque, using an EVL = V_{dc}, represents one set or one case. For each case, plots of i_{ph}, v_{ph}, T_e, and $v_{cell\text{-}n}$ are be provided, along with a table showing performance figures for different choices of θ_{on}/θ_{off}. For the case of 25% speed at ~6% torque, only the $0.25V_{dc}$ EVL case is reported, and the other three EVLs are omitted for the sake of brevity.

TABLE 3.3
SUMMARY OF SIMULATED OPERATION SCENARIOS OF THE 8-CELL CCC SRM DRIVE IN SINGLE-PULSE MODE

Speed	Torque	Energization Voltage (s)
120%	~83%	V_{dc}
110%	~91%	V_{dc}
100%	100%	V_{dc}
75%	100%	V_{dc}, $0.75V_{dc}$
75%	~56%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$
50%	100%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$
50%	~25%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$
25%	100%	V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, $0.25V_{dc}$
25%	~6%	$0.25V_{dc}$

In all simulations, the same thermal settings for the semiconductor device heat sinks were used to provide a fair comparison. The thermal resistance from the device case to ambient, which is the sum of the thermal resistance from device case to heat sink, then heat sink to ambient, was set to 0.1 K/W. The ambient temperature was assumed 25°C, which is a good compromise between machine-room cooled environment or an outdoor unit in hot temperature. The results reported were calculated when the drive was at or close to steady state temperature, which is different from one operating point to another, being obviously higher for more demanding operating points where absolute thermal losses are higher.

Simulation results are given below, and their analyses are provided in the section that follows. To obtain single-pulse operation for different values of θ_{off}, a PI speed controller with θ_{on} reference output, such as described above, was used.

Case 1: *100% speed at 100% torque*

TABLE 3.4
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 100% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
22	−10.52	231.57	784.70	7475	11020	7789	27167	7853	99.05	97.66
23	−10.06	228.07	763.27	6880	10659	7418	22159	11252	99.09	97.73
24	−9.65	225.17	744.46	6329	10345	7094	18283	15183	99.14	97.79
25	−9.31	223.11	726.56	5824	10091	6824	15391	19852	99.17	97.84
26	−9.03	221.85	713.04	5356	9883	6595	13202	25695	99.21	97.89
27	−8.80	221.32	701.03	4948	9722	6407	11535	32834	99.24	97.92
28	−8.63	221.66	690.35	4278	9509	6261	10283	42740	99.26	97.96

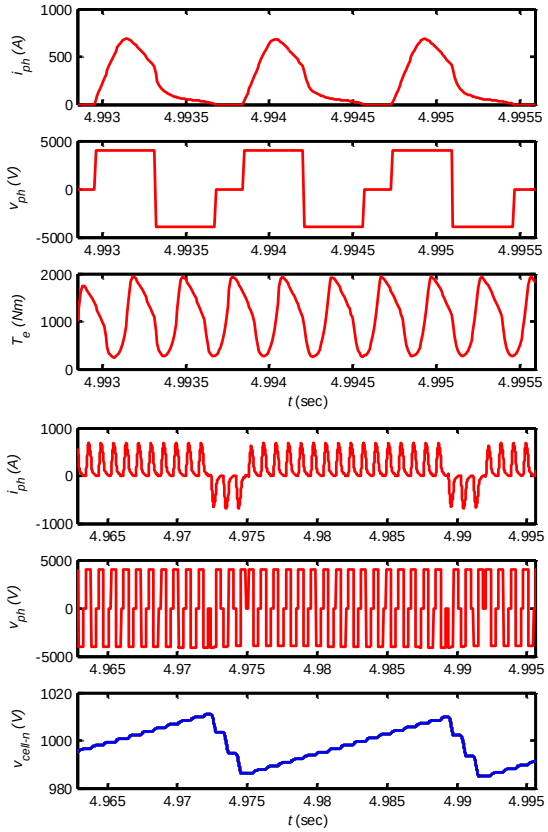


Fig. 5.11 Sample waveforms for single-pulse operation at 100% speed & 100% torque, EVL = V_{dc}

Case 2: *110% speed at ~91% torque (operating at rated power – i.e. in constant power mode)*

TABLE 3.5
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 110% SPEED AND 91% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
21	−12.46	231.10	783.39	8041	10965	7647	51146	8028	99.02	97.44
22	−11.95	226.93	761.05	7405	10573	7263	41647	10997	99.07	97.52
23	−11.52	223.73	742.55	6789	10250	6941	34792	14771	99.12	97.58
24	−11.15	221.34	727.07	6209	9980	6666	29651	19401	99.16	97.64
25	−10.85	219.69	712.37	5698	9760	6435	25710	24909	99.20	97.68
26	−10.63	218.86	699.50	5275	9588	6247	22799	31727	99.23	97.72
27	−10.45	218.76	689.98	4878	9458	6095	20571	40076	99.25	97.76

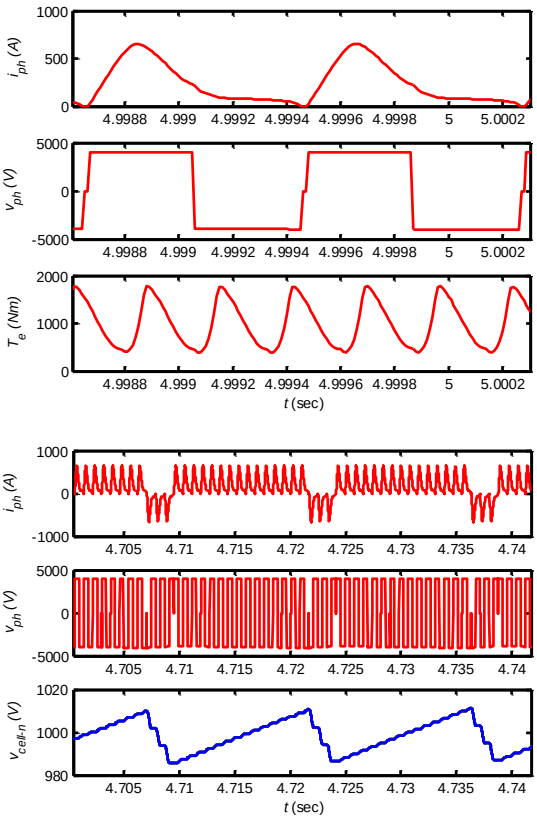


Fig. 5.12 Sample waveforms for single-pulse operation at 110% speed & 91% torque, EVL = V_{dc}

Case 3: *120% speed at ~83% torque (operating at rated power – i.e. in constant power mode)*

TABLE 3.6
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 120% SPEED AND 83% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
21	−13.83	226.87	760.80	7763	10538	7192	72786	13104	99.06	97.29
22	−13.36	223.12	740.68	7099	10188	6849	61467	15491	99.11	97.35
23	−12.97	220.50	724.43	6487	9913	6572	52969	19323	99.15	97.41
24	−12.66	218.63	710.60	5972	9687	6340	46097	24860	99.19	97.46
25	−12.42	217.62	700.79	5521	9512	6154	41019	31540	99.22	97.50
26	−12.23	217.26	690.67	5094	9373	6001	37152	39523	99.25	97.54
27	−12.12	217.71	682.36	4711	9280	5887	34386	49459	99.27	97.57

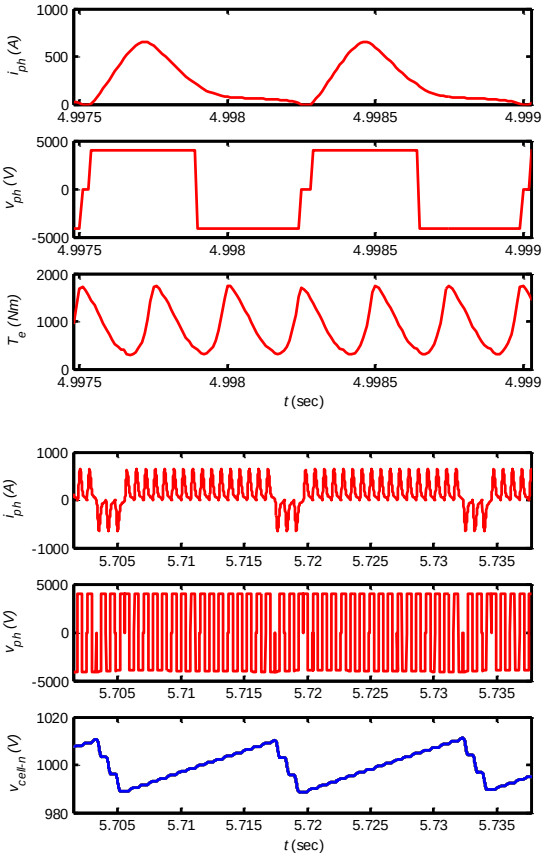


Fig. 5.13 Sample waveforms for single-pulse operation at 120% speed & 83% torque, EVL = V_{dc}

Case 4: *75% speed at 100% torque (Energization Voltage Level = V_{dc})*

TABLE 3.7
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 75% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
21	−3.99	193.33	757.63	6834	9100	6619	1387	49	98.90	97.71
22	−3.45	189.00	730.69	6369	8719	6215	828	333	98.96	97.79
23	−2.99	185.56	701.94	5912	8399	5865	488	1047	99.01	97.86
24	−2.57	182.83	673.37	5503	8124	5561	282	2265	99.05	97.93
25	−2.19	180.69	649.60	5144	7892	5299	160	3993	99.09	97.99
26	−1.85	179.20	627.62	4830	7698	5073	89	6346	99.13	98.04
27	−1.55	178.41	611.26	4535	7541	4882	49	9571	99.16	98.08

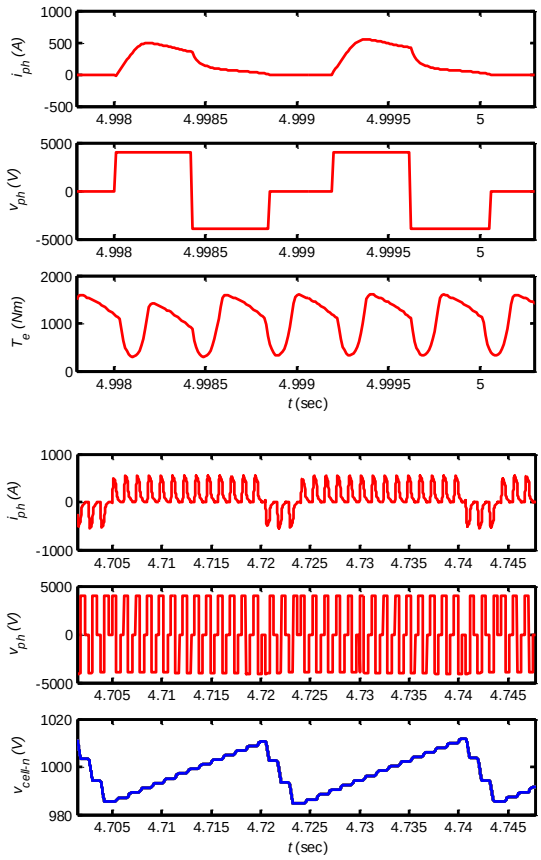


Fig. 5.14 Sample waveforms for single-pulse operation at 75% speed & 100% torque, EVL = V_{dc}

Case 5: *75% speed at 100% torque (Energization Voltage Level =* $0.75V_{dc}$*)*

TABLE 3.8
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 75% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = $\mathbf{0.75V_{DC}}$

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
24	−9.35	221.48	762.00	4400	10063	7235	14972	1068	98.99	97.76
25	−8.99	218.54	744.34	4054	9775	6919	12352	2152	99.04	97.82
26	−8.69	216.44	724.52	3736	9539	6656	10439	3780	99.07	97.88
27	−8.42	214.89	710.24	3454	9345	6430	8949	5910	99.11	97.92
28	−8.20	213.98	699.63	3215	9185	6241	7809	8683	99.13	97.96
29	−8.03	213.73	686.23	3007	9067	6090	6944	12126	99.16	97.99
30	−7.89	213.94	679.60	2831	8979	5963	6278	16488	99.17	98.02

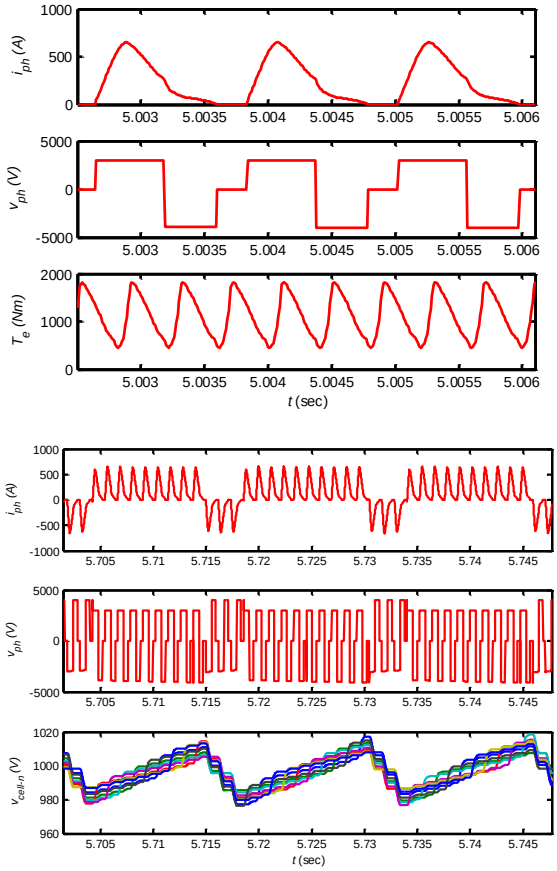


Fig. 5.15 Sample waveforms for single-pulse operation at 75% speed & 100% torque, EVL = $0.75V_{dc}$

Case 6: *75% speed at ~56% torque (Energization Voltage Level = V_{dc})*

TABLE 3.9
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 75% SPEED AND 56% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
19	−0.43	115.50	568.01	4519	4628	2922	3	0	98.89	97.24
20	0.25	112.54	537.00	4296	4427	2712	0	0	98.93	97.31
21	0.88	110.12	513.03	4109	4254	2533	0	0	98.98	97.37
22	1.47	108.26	493.79	3963	4113	2381	0	0	99.01	97.42
23	2.01	106.95	474.49	3854	3997	2256	0	0	99.04	97.47
24	2.40	106.05	458.35	3702	3902	2146	0	25	99.07	97.51
25	2.62	105.76	449.62	3468	3831	2057	0	348	99.11	97.56

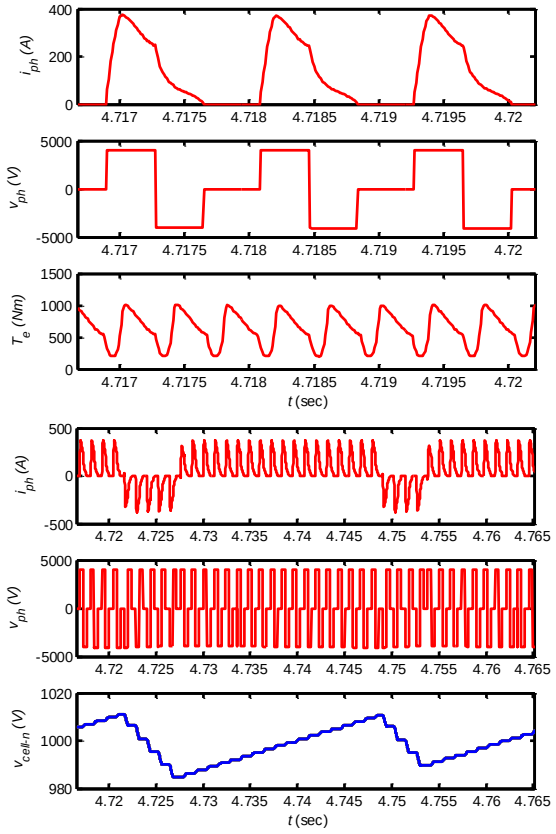


Fig. 5.16 Sample waveforms for single-pulse operation at 75% speed & ~56% torque, EVL = V_{dc}

Case 7: *75% speed at ~56% torque (Energization Voltage Level = 0.75V_{dc})*

TABLE 3.10
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 75% SPEED AND 56% TORQUE

ENERGIZATION VOLTAGE = 0.75V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
23	−3.21	128.40	537.99	2949	4886	2926	523	0	99.04	97.38
24	−2.73	127.13	526.08	2866	4779	2806	368	0	99.06	97.42
25	−2.40	126.31	519.18	2741	4691	2704	267	22	99.09	97.46
26	−2.26	126.05	514.31	2546	4625	2620	210	282	99.12	97.50
27	−2.23	126.20	505.99	2369	4576	2552	173	1048	99.15	97.54
28	−2.18	126.50	497.38	2222	4541	2492	144	2354	99.17	97.57
29	−2.13	127.11	490.51	2097	4515	2445	120	4266	99.19	97.59

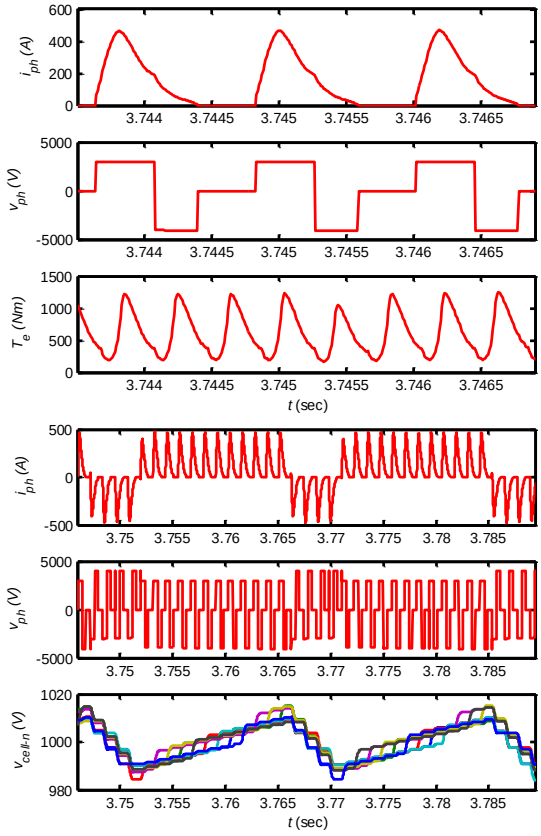


Fig. 5.17 Sample waveforms for single-pulse operation at 75% speed & ~56% torque, EVL = 0.75V_{dc}

Case 8: *75% speed at ~56% torque (Energization Voltage Level = 0.5V_{dc})*

TABLE 3.11
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 75% SPEED AND 56% TORQUE

ENERGIZATION VOLTAGE = 0.5V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
27	−12.11	171.50	610.90	1705	6550	4135	25959	139	98.99	97.19
28	−12.13	171.27	606.71	1582	6492	4058	24458	593	99.01	97.22
29	−12.17	171.26	599.43	1477	6443	3991	23152	1475	99.03	97.25
30	−12.19	171.59	594.50	1391	6409	3941	22136	2791	99.05	97.28
31	−12.20	171.98	590.02	1316	6384	3894	21227	4566	99.06	97.29
32	−12.21	172.61	585.53	1264	6368	3857	20470	6833	99.06	97.30
33	−12.23	173.32	583.41	1210	6355	3823	19801	9614	99.07	97.31

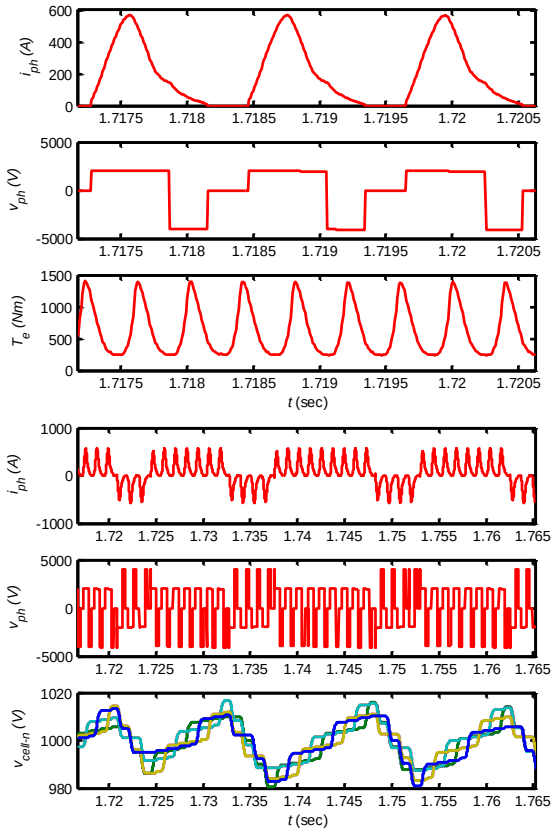


Fig. 5.18 Sample waveforms for single-pulse operation at 75% speed & 56% torque, EVL = 0.5V_{dc}

Case 9: *50% speed at 100% torque (Energization Voltage Level = V_{dc})*

TABLE 3.12
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
24	4.35	146.08	802.27	4486	6437	4605	0	0	98.85	97.88
25	4.91	144.31	794.11	4517	6282	4391	0	3	98.87	97.92
26	5.36	143.15	785.76	4369	6131	4203	0	110	98.90	97.97
27	5.74	142.64	775.70	4242	6020	4056	0	568	98.92	98.00
28	6.11	142.53	772.09	4120	5932	3933	0	1509	98.94	98.04
29	6.44	142.95	765.79	4050	5874	3840	0	3013	98.96	98.06
30	6.76	144.10	766.33	4000	5855	3784	0	5173	98.97	98.08

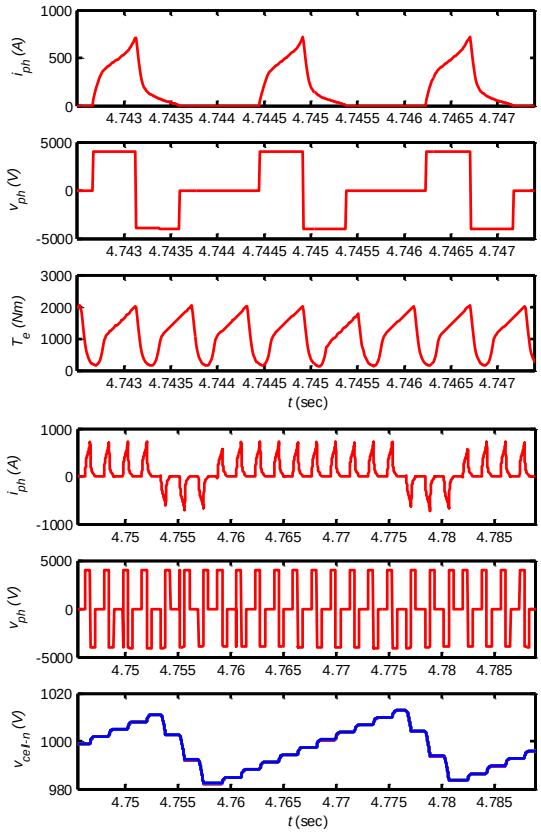


Fig. 5.19 Sample waveforms for single-pulse operation at 50% speed & 100% torque, EVL = V_{dc}

Case 10: *50% speed at 100% torque (Energization Voltage Level = 0.75V_{dc})*

TABLE 3.13
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = 0.75V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
24	−0.46	168.28	677.96	3386	7380	5326	3	0	98.87	97.82
25	0.13	165.59	651.98	3272	7141	5045	0	0	98.91	97.89
26	0.64	163.58	631.05	3166	6943	4806	0	4	98.94	97.95
27	1.03	161.98	608.65	3019	6766	4587	0	92	98.97	98.00
28	1.31	160.96	589.43	2858	6620	4400	0	480	99.00	98.05
29	1.57	160.41	567.12	2716	6501	4238	0	1302	99.03	98.10
30	1.81	160.47	552.21	2611	6417	4110	0	2606	99.05	98.12

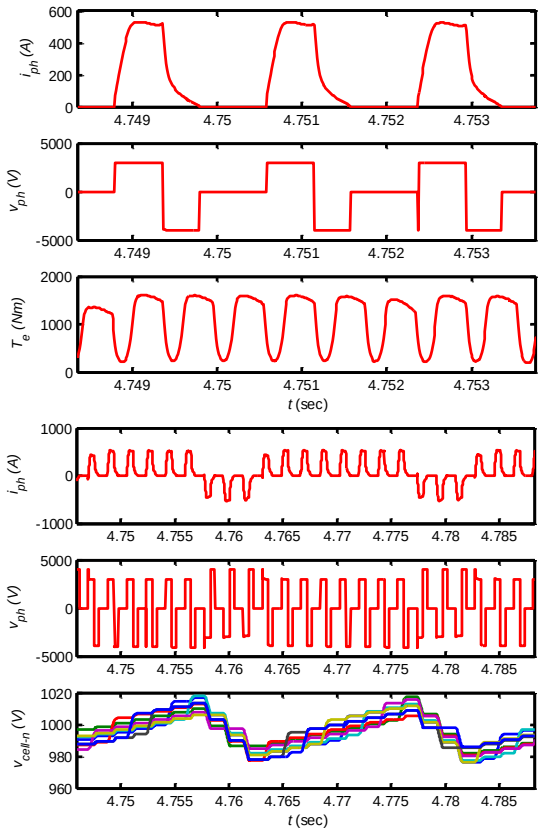


Fig. 5.20 Sample waveforms for single-pulse operation at 50% speed & 100% torque, EVL = 0.75V_{dc}

Case 11: *50% speed at 100% torque (Energization Voltage Level = $0.5V_{dc}$)*

TABLE 3.14
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = $0.5V_{DC}$

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
26	−8.58	213.76	740.56	2117	9285	6861	7756	0	98.81	97.60
27	−8.10	211.35	729.26	2012	9058	6598	6565	0	98.85	97.67
28	−7.75	209.47	716.30	1909	8874	6368	5637	23	98.87	97.71
29	−7.57	208.40	704.31	1786	8733	6180	4955	215	98.89	97.76
30	−7.46	207.70	695.58	1660	8607	6017	4390	742	98.94	97.82
31	−7.34	207.51	686.62	1552	8517	5886	3951	1647	98.94	97.83
32	−7.25	207.61	677.16	1473	8445	5774	3601	2981	98.96	97.86

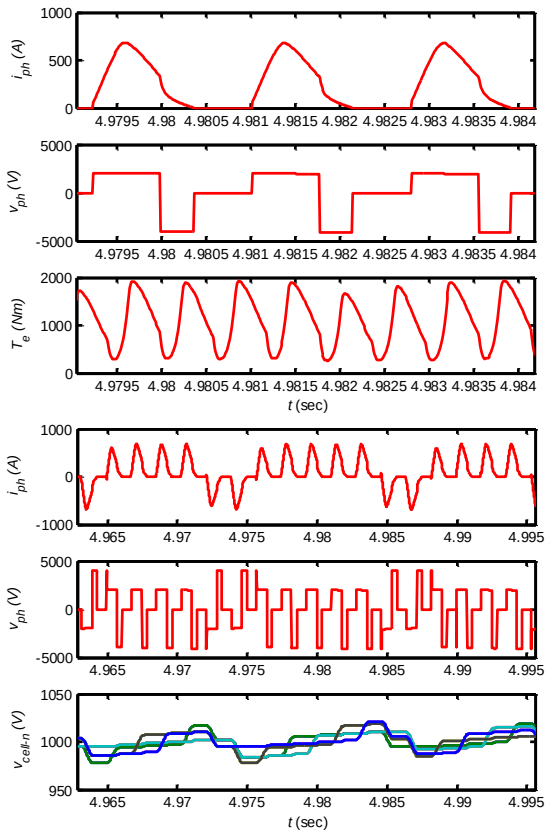


Fig. 5.21 Sample waveforms for single-pulse operation at 50% speed & 100% torque, EVL = $0.5V_{dc}$

Case 12: *50% speed at 25% torque (Energization Voltage Level = V_{dc})*

TABLE 3.15
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 25% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
24	10.29	45.25	328.81	1708	1358	551	0	0	98.75	96.61
25	10.66	45.96	319.88	1697	1364	540	0	0	98.76	96.61
26	11.04	46.75	313.57	1745	1371	533	0	0	98.73	96.60
27	11.42	47.62	308.96	1701	1385	528	0	0	98.75	96.63
28	11.80	48.52	304.42	1710	1399	526	0	0	98.73	96.61
29	12.09	49.55	307.94	1674	1416	525	0	31	98.75	96.61
30	12.28	50.80	306.08	1616	1440	528	0	392	98.75	96.61

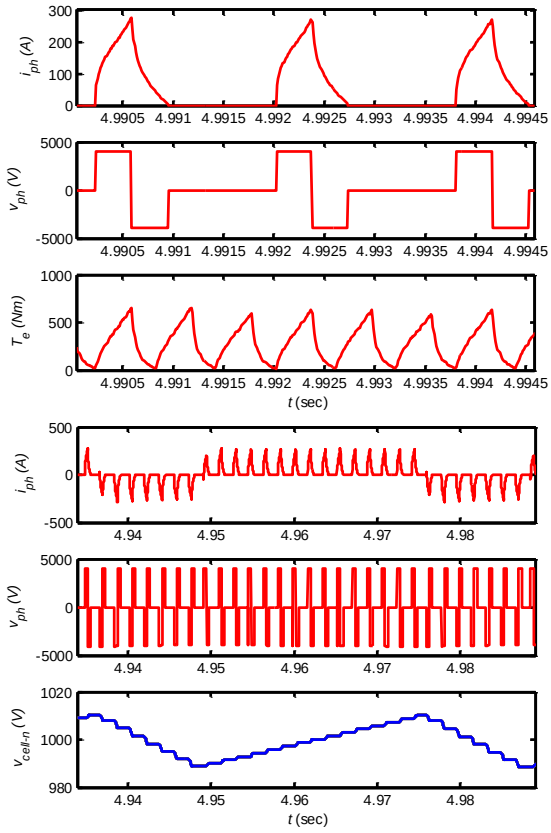


Fig. 5.22 Sample waveforms for single-pulse operation at 50% speed & 25% torque, EVL = V_{dc}

Case 13: *50% speed at 25% torque (Energization Voltage Level = 0.75V_{dc})*

TABLE 3.16
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 25% TORQUE

ENERGIZATION VOLTAGE = 0.75V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
24	7.45	49.89	262.31	1259	1503	606	0	0	98.87	96.70
25	7.78	50.31	252.34	1250	1497	587	0	0	98.88	96.72
26	8.09	50.85	241.68	1241	1496	571	0	0	98.88	96.72
27	8.40	51.38	232.27	1251	1495	557	0	0	98.88	96.73
28	8.72	52.05	224.25	1267	1500	547	0	0	98.87	96.74
29	9.05	52.68	213.71	1281	1504	538	0	0	98.87	96.72
30	9.28	53.44	212.82	1273	1509	530	0	13	98.86	96.72

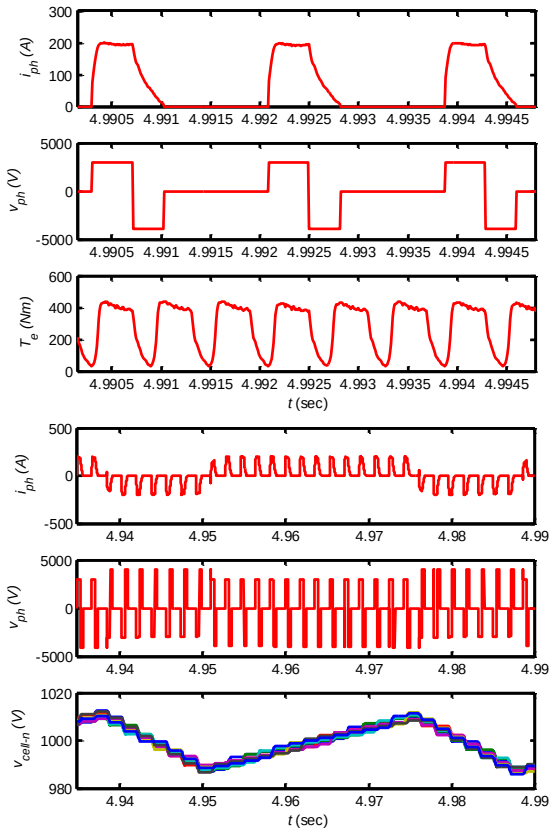


Fig. 5.23 Sample waveforms for single-pulse operation at 50% speed & 25% torque, EVL = 0.75V_{dc}

Case 14: *50% speed at 25% torque (Energization Voltage Level = 0.5V_{dc})*

TABLE 3.17
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 25% TORQUE

ENERGIZATION VOLTAGE = 0.5V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
27	3.30	62.30	313.73	862	1877	769	0	0	98.88	96.65
28	3.59	62.50	307.76	873	1864	749	0	0	98.88	96.65
29	3.90	62.77	301.95	888	1855	731	0	0	98.87	96.65
30	4.21	63.05	296.10	908	1846	715	0	0	98.88	96.65
31	4.51	63.34	293.14	927	1839	700	0	0	98.87	96.67
32	4.68	63.85	286.03	922	1837	688	0	18	98.88	96.68
33	4.70	64.54	284.15	888	1839	677	0	218	98.89	96.69

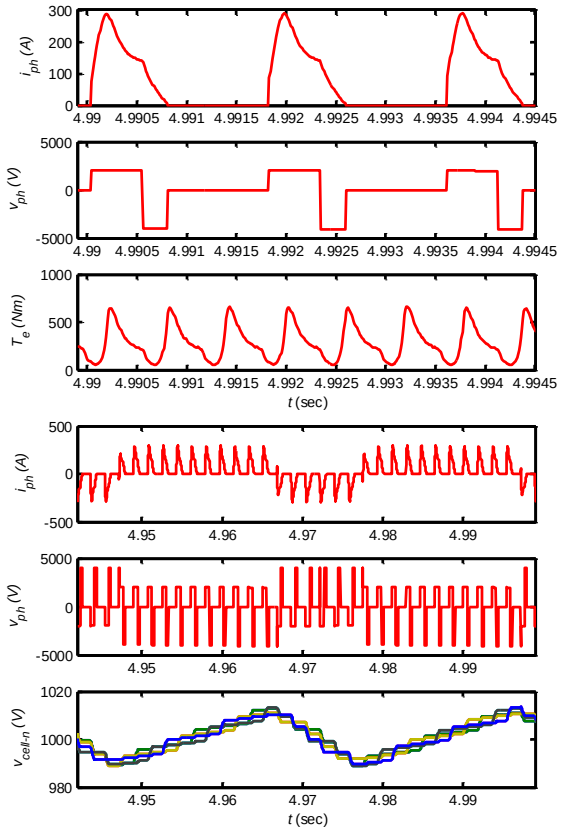


Fig. 5.24 Sample waveforms for single-pulse operation at 50% speed & 25% torque, EVL = 0.5V_{dc}

Case 15: *50% speed at 25% torque (Energization Voltage Level = 0.25V_{dc})*

TABLE 3.18
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 50% SPEED AND 25% TORQUE

ENERGIZATION VOLTAGE = 0.25V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
31	−8.83	100.96	412.89	576	3202	1549	3612	0	98.47	95.93
32	−8.44	100.67	410.33	593	3175	1523	3337	0	98.48	95.94
33	−8.02	100.38	406.94	614	3149	1497	3071	0	98.47	95.94
34	−7.64	99.87	403.83	630	3113	1465	2790	0	98.46	95.93
35	−7.66	101.13	403.12	620	3140	1476	2813	22	98.49	96.00
36	−7.75	101.69	401.75	599	3138	1464	2755	172	98.49	96.01
37	−7.96	102.40	399.60	568	3140	1455	2727	581	98.50	96.03

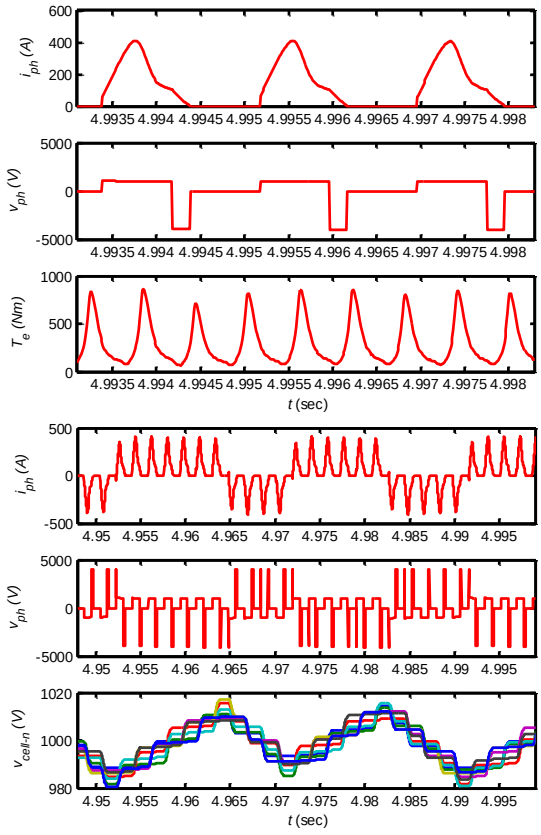


Fig. 5.25 Sample waveforms for single-pulse operation at 50% speed & 25% torque, EVL = 0.25V_{dc}

Case 16: *25% speed at 100% torque (Energization Voltage Level = V_{dc})*

TABLE 3.19
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 25% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
21	9.30	124.15	1310.38	3463	6273	5778	0	0	97.98	96.54
22	10.05	122.94	1318.37	3465	6165	5643	0	0	98.01	96.60
23	10.77	122.50	1329.77	3502	6113	5580	0	0	98.01	96.62
24	11.46	122.68	1355.19	3563	6113	5585	0	0	97.99	96.59
25	12.13	123.71	1404.25	3666	6180	5678	0	0	97.95	96.52
26	12.78	125.50	1427.28	3721	6261	5851	0	0	97.93	96.47
27	13.43	127.74	1496.24	3901	6424	6086	0	0	97.88	96.38

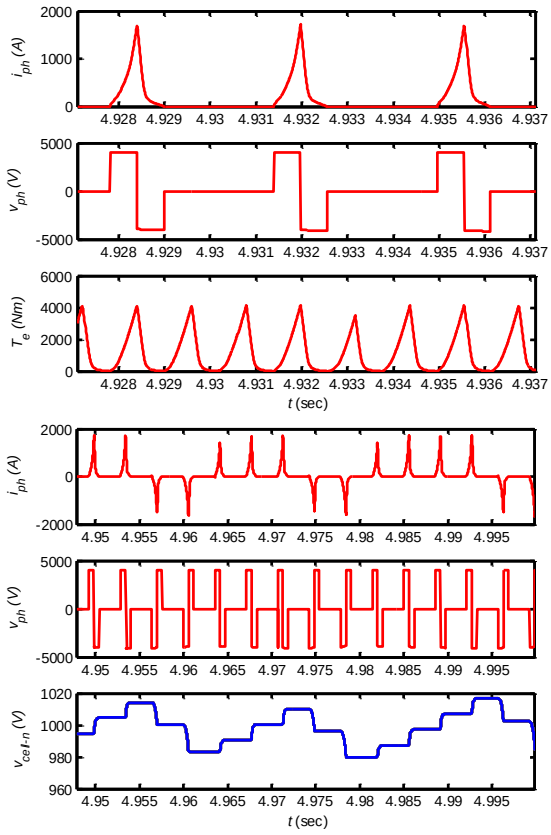


Fig. 5.26 Sample waveforms for single-pulse operation at 25% speed & 100% torque, EVL = V_{dc}

Case 17: *25% speed at 100% torque (Energization Voltage Level = 0.75V_{dc})*

TABLE 3.20
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 25% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = 0.75V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
23	7.95	127.53	1129.42	2528	6026	5118	0	0	98.24	96.93
24	8.62	126.25	1122.35	2513	5904	4959	0	0	98.24	96.96
25	9.25	125.55	1123.17	2535	5823	4848	0	0	98.24	96.98
26	9.86	125.63	1146.06	2561	5788	4806	0	0	98.25	97.00
27	10.45	126.50	1175.79	2621	5799	4829	0	0	98.27	97.02
28	11.02	127.81	1214.14	2721	5868	4912	0	0	98.24	96.98
29	11.57	129.78	1288.04	2852	5988	5064	0	0	98.16	96.88

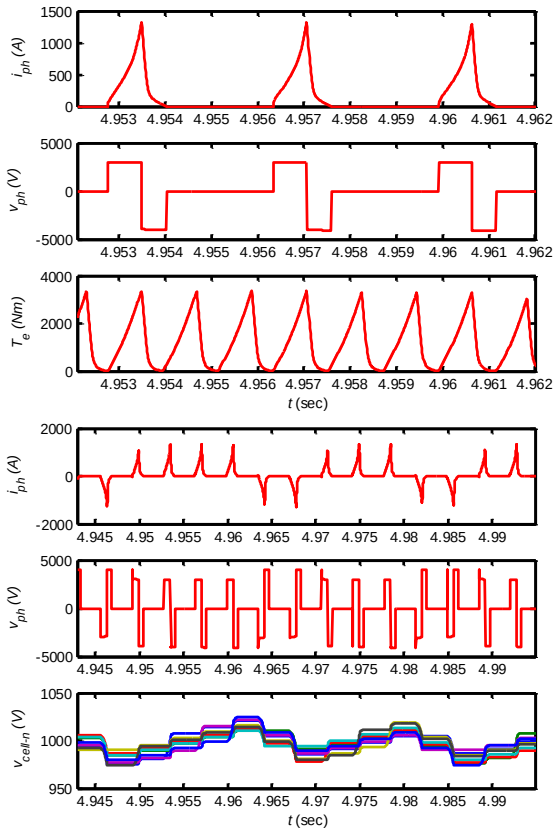


Fig. 5.27 Sample waveforms for single-pulse operation at 25% speed & 100% torque, EVL = 0.75V_{dc}

Case 18: *25% speed at 100% torque (Energization Voltage Level = 0.5V_{dc})*

TABLE 3.21
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 25% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = 0.5V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
27	5.19	138.28	825.31	1480	5828	4331	0	0	98.48	97.33
28	5.70	137.35	813.32	1459	5710	4170	0	0	98.51	97.39
29	6.18	136.81	810.64	1462	5625	4043	0	0	98.52	97.44
30	6.63	136.95	825.30	1483	5580	3959	0	0	98.52	97.44
31	7.07	137.44	843.33	1508	5546	3899	0	0	98.52	97.46
32	7.47	138.45	883.66	1546	5557	3880	0	0	98.52	97.47
33	7.81	140.16	910.09	1596	5603	3906	0	7	98.49	97.43

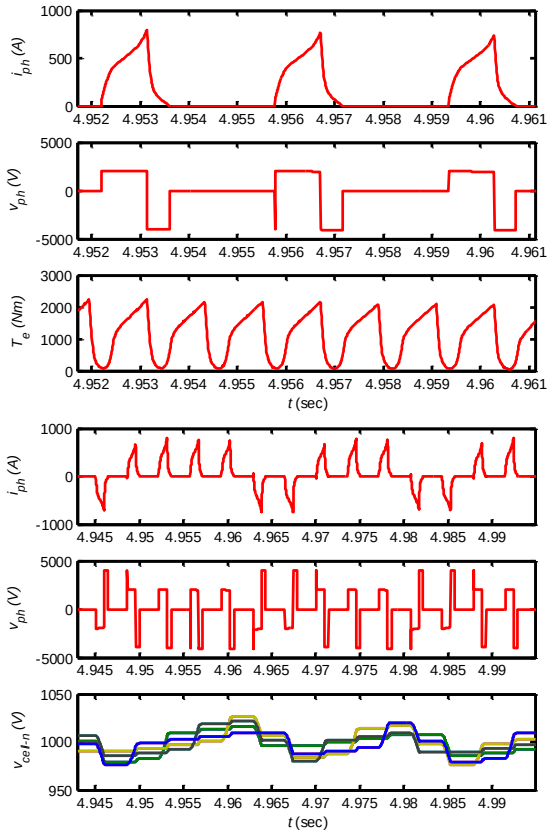


Fig. 5.28 Sample waveforms for single-pulse operation at 25% speed & 100% torque, EVL = 0.5V_{dc}

Case 19: *25% speed at 100% torque (Energization Voltage Level = 0.25V_{dc})*

TABLE 3.22
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 25% SPEED AND 100% TORQUE

ENERGIZATION VOLTAGE = 0.25V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
32	−7.09	202.79	712.80	590	8245	5976	1863	0	98.17	96.68
33	−6.79	202.32	705.54	585	8161	5851	1688	0	98.18	96.73
34	−6.55	202.07	699.29	577	8089	5739	1540	0	98.21	96.77
35	−6.39	202.21	693.14	570	8037	5647	1420	6	98.22	96.81
36	−6.31	202.59	686.28	559	8003	5565	1317	75	98.23	96.83
37	−6.28	203.34	678.17	546	7983	5502	1226	311	98.23	96.84
38	−6.25	204.40	673.37	533	7978	5456	1149	798	98.23	96.86

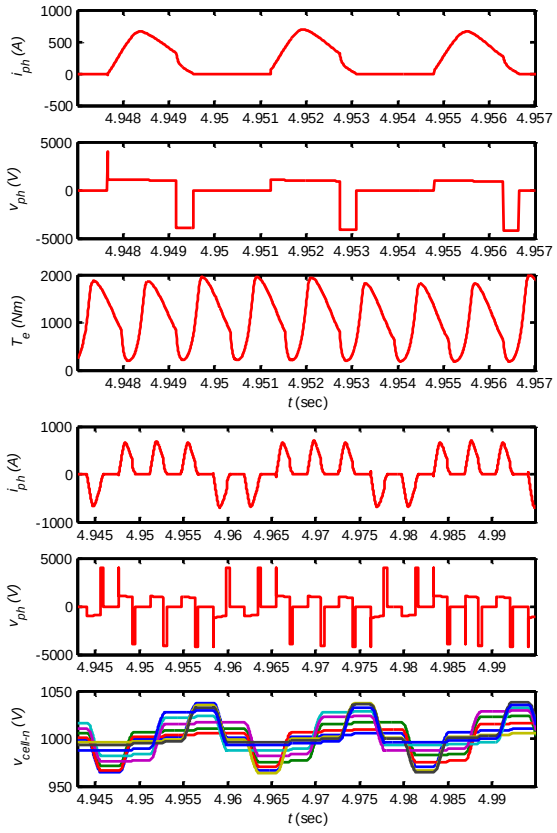


Fig. 5.29 Sample waveforms for single-pulse operation at 25% speed & 100% torque, EVL = 0.25V_{dc}

Case 20: *25% speed at ~6% torque (Energization Voltage Level = 0.25V_{dc})*

TABLE 3.23
PERFORMANCE FOR SINGLE-PULSE OPERATION AT 25% SPEED AND 6% TORQUE

ENERGIZATION VOLTAGE = 0.25V_{DC}

θ_{off} (°)	θ_{on} (°)	I_{avg} (A)	I_{pk} (A)	P_{sw} (W)	P_{cond} (W)	P_{cu} (W)	P_{adv} (W)	P_{comm} (W)	η_c (%)	η' (%)
32	11.30	22.64	106.06	222	449	116	0	0	97.92	93.93
33	11.66	22.92	105.40	223	445	115	0	0	97.93	93.93
34	12.02	23.20	103.72	225	444	114	0	0	97.91	93.92
35	12.40	23.53	103.62	224	444	114	0	0	97.96	93.97
36	12.78	23.85	103.50	224	444	115	0	0	97.96	93.95
37	13.10	24.42	102.49	224	453	117	0	0	97.91	93.90
38	13.49	24.77	102.35	221	454	117	0	0	97.95	94.00

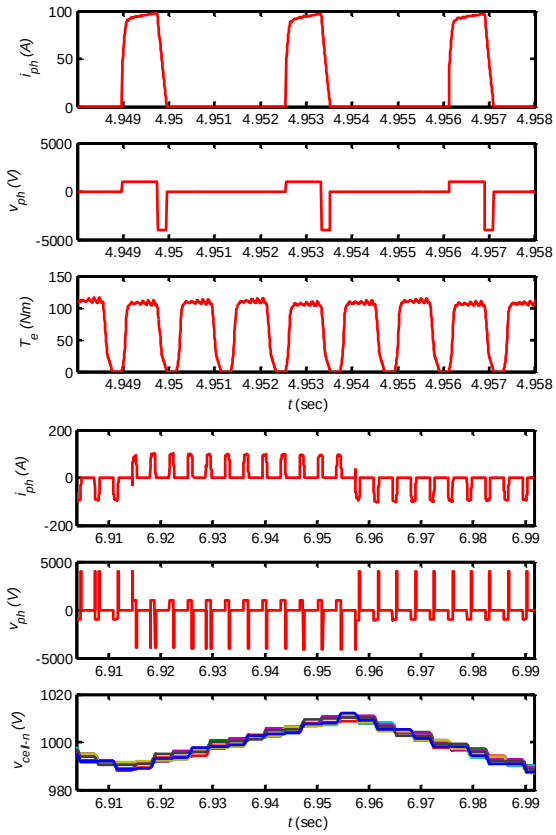


Fig. 5.30 Sample waveforms for single-pulse operation at 25% speed & 6% torque, EVL = 0.25V_{dc}

5.4 Analysis of Simulation Results

5.4.1 Semiconductor Losses

Semiconductor losses are composed of conduction losses, P_{cond}, and switching losses, P_{sw}. P_{cond} is mainly dependent on the average current going through the switch or diode. P_{sw} depends on the voltage that the device is blocking or is to block, as well as the current at the switching instant. Device temperature also affects both forms of losses, though to a lesser extent. The following trends are noted from the simulations above regarding semiconductor losses.

5.4.1.1 Effect of energization voltage level on semiconductor losses

To analyze this trend, loss data for different EVLs at 50% speed are plotted in Fig. 5.31 (a) for the 100% load torque case, and in Fig. 5.31 (b) for fan-type load. Opposing trends are noted for P_{cond} and P_{sw}. P_{cond} increase when a lower EVL is used. The same amount of energy must be generated per stroke regardless of the EVL used. Energy is the product of current, voltage, and time. The voltage pulse for lower EVLs is wider, though not wide enough to keep the current demand the same as that for the higher EVL. Therefore, a slight increase in current occurs when using lower EVL. This is the reason for the increased P_{cond} at lower EVLs. However, it is noted that a sharp rise in P_{cond} occurs for the lowest feasible EVL. This happens when the EVL is too low that it requires advancing θ_{on} before 0°. As a consequence, negative torque components, T_{adv}, are generated as explained earlier in section 5.2.2. Since extra current needs to be developed to compensate for these negative torque contributions, the resulting current demand is noticeably higher than with the other EVLs, which is what causes the exaggerated conduction losses. This is why operation at this EVL results in low efficiency, as will be later seen in the section on efficiency trends.

(a) (b)

Fig. 5.31 Variation of semiconductor losses with EVL at 50% speed

TABLE 3.23
OF DEVICES SWITCHING AT θ_{OFF} FOR DIFFERENT ENERGIZATION VOLTAGE LEVELS IN 8-CELL IN AN 8-CELL CCC SRM CONVERTER

Energization Voltage Level	IGBTs turning OFF
V_{dc}	8
$0.75V_{dc}$	7
$0.5V_{dc}$	6
$0.25V_{dc}$	5

On the other hand, P_{sw} always decreases when a lower EVL is used. The main reason behind this is that less devices are being switched per stroke when lower energization voltages are used. Table 3.24 compares the number of IGBT switching events per stroke that contribute significantly to P_{sw} for different EVLs. Recall that in single-pulse mode switching happens only at θ_{on} and θ_{off}. But at θ_{on} the current is typically zero, so there are no switching losses at that instant. Therefore switching losses occur only at θ_{off}, and so only IGBT turn-off events are considered in Table 3.24. Also immediately following an IGBT turn-off, the corresponding diode in the cell is turned on. However, diode turn-on losses are very low and are usually neglected in calculation, and so they are also omitted in Table 3.24. Since the applied de-energization voltage in all simulations was of magnitude V_{dc}, all active IGBTs are turned off at θ_{off}. This is achieved by setting all gate signals to zero at θ_{off}, which produces $-V_{dc}$ across the winding to de-energize after a P-mode stroke, or a $+V_{dc}$ across the winding to de-energize after an N-mode stroke. It is clear how lower EVLs have fewer switching events that contribute to P_{sw}. Another factor that contributes to the reduction of P_{sw} is that the current at the turn-off instant is usually lower at lower EVLs.

5.4.2 Efficiency

The converter efficiency and overall efficiency are compared across the speed range in Fig. 5.32 for the constant 100% load torque case, and in Fig. 5.33 for the fan-type load. The efficiencies are calculated as explained earlier in section 5.2.2. The efficiency pair reported for each operating point is based on the EVL and θ_{on}/θ_{off} that produced the best overall efficiency. Note how the CCC SRM converter efficiency in single-pulse mode maintains high efficiency across the complete speed range. But at low speed and torque, such as 25% speed for a fan-type load, the semiconductor losses, even though lower, represent a bigger percentage of the operating power when compared to higher speeds and torques. Thus, at low speed and torque the efficiency is expectedly lower.

With regards to overall efficiency, slightly lower values are obtained at higher speeds for the 100% load profile due to the increased current demand, which results in higher semiconductor losses as well as increased copper losses – except at 25% speed due to the reason explained above. Also this trend is not true in the fan-type load since current demand is lower. Rather, the same argument that losses, though lower in magnitude, represent a bigger percentage of the operating power when compared to higher speed/torque.

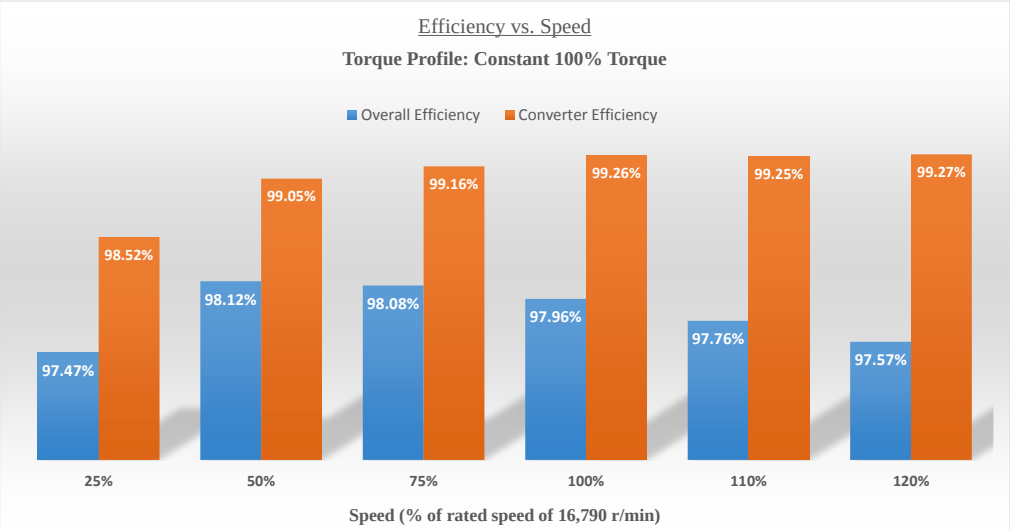


Fig. 5.32 Best efficiency for various points across speed range for 100% load torque

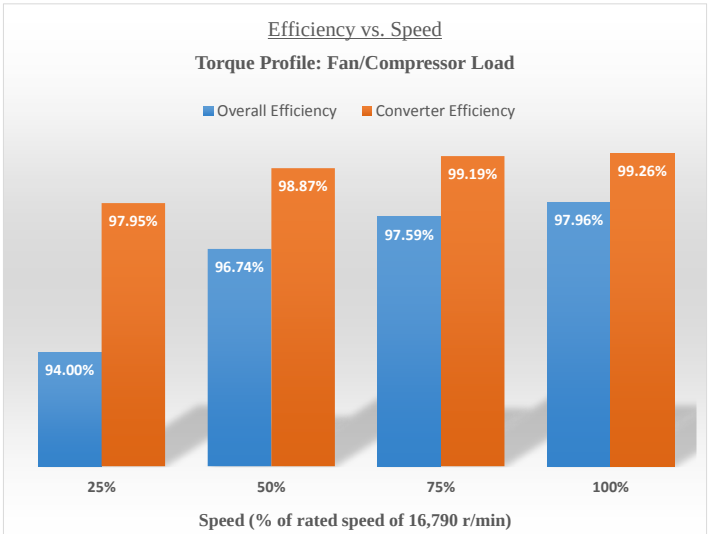
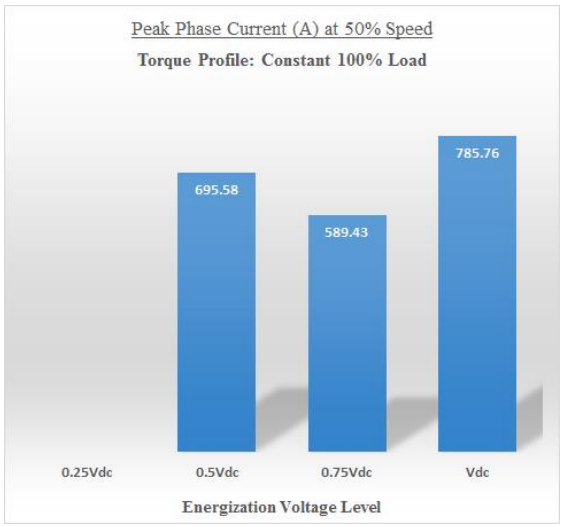


Fig. 5.33 Best efficiency for various points across speed range for fan-type load

5.4.3 Peak Phase Current

As earlier mentioned, the peak phase current, I_{pk}, is an important performance figure as it cannot exceed a certain value for a given device. For the SRM under consideration at 100% speed and 100% torque, $i_{ph\text{-}peak}$ = 744.46 A for the EVL and θ_{on}/θ_{off} that produced the best overall efficiency. Datasheets for high current IGBTs quote both a maximum average current and a maximum peak current for each of the IGBT and the anti-parallel diode. The peak current rating is most of the time two times the average current rating. However, in most cases a limitation is placed on the duration of the occurrence of that peak current. Since an SRM can have a long peak duration at high speeds, it is safest if the device is chosen such that its rated (average) current is equal or close to the maximum peak current found from simulations.

(a)



(b)

Fig. 5.34 I_{pk} for different EVLs at 25% and 50% speed with 100% torque

5.4.3.1 Variation of peak phase current with energization voltage level

The highest peak currents occur at the combination of low speed and high torque demand. Therefore the 25% and 50% speeds at 100% load will be considered here. Fig. 5.34 (a) shows the trend in the variation I_{pk} with EVL at 25% speed and 100% load torque, while Fig. 5.34 (a) shows the same at 50% speed and 100% load torque. While I_{pk} is acceptable for all energization voltage levels at the 50% speed, it is excessively high at the 25% speed except at the $0.25V_{dc}$ EVL. This demonstrates another advantage of the CCC multilevel converter for SRM in that it can combine both low semiconductor losses with low peak current by allowing energization with lower voltage levels. At other speeds I_{pk} was 673.37 A at 75% speed & 100% torque, 744.46 A at 100% speed, 727.07 A at 110% speed, and 710.60 A at 120% speed.

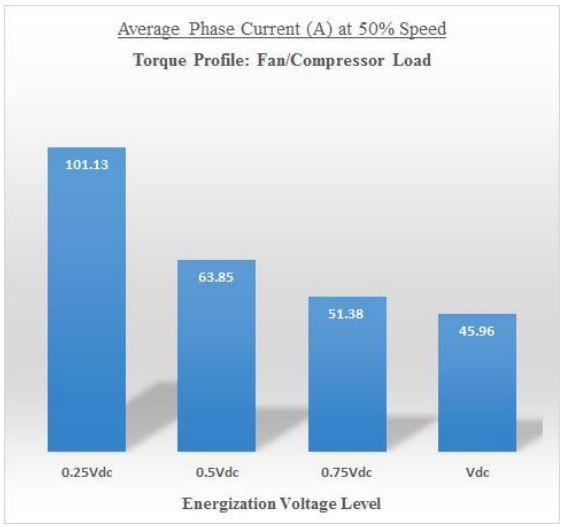
5.4.4 Average Phase Current

In any machine a lower average current, I_{avg}, is desired, as it results in lower device conduction losses as well as lower copper losses.

5.4.4.1 Variation of average phase current with energization voltage level

The different I_{avg} obtained for all feasible EVLs at 50% speed are shown in Fig. 5.35 (a) for 100% load torque and in Fig. 5.35 (b) for a fan-type load. As explained earlier, I_{avg} is expected to increase as the EVL used is lowered, and shows a sharp rise at very low EVLs when θ_{on} is advanced before 0° which results in negative torque contribution that is compensated by increasing the current. This is why the lowest feasible EVL is not typically the most efficient. Rather, the most efficient EVL is likely to be that lowest feasible EVL that does not require θ_{on} to be advanced before 0°, since in such EVL P_{sw} is lower without the penalty of additional P_{adv}.

(a)



(b)

Fig. 5.35 I_{avg} for different EVLs at 50% speed for two different load profiles

5.4.4 Using Lower De-energization Voltage Levels

In all simulated cases, the highest available voltage was used for de-energization to commutate the current at the end of a stroke. For a P-mode stroke this was $-V_{dc}$ and for an N-mode stroke it was $+V_{dc}$. This is almost always desirable as it provides the fastest commutation before the current extends into the negative torque generation region. However, at low speeds and very low torque demands, like in fan/compressor loads with a quadratic torque-speed relationship, there may be regions of zero torque production in single-pulse mode due to the pulse being narrow. This is most noticeable with high EVLs. But even when using the lowest available EVL, sometimes this cannot be avoided. The use of a lower de-energization voltage level may help reduce this.

Considering case 20, with 25% speed and ~6% torque, a simulation with $0.5V_{dc}$ de-energization voltage was also carried out. Current and torque waveforms are given in Fig. 5.36 (a) for full V_{dc} de-energization, and in Fig. 5.36 (a) for $0.5V_{dc}$ de-energization. First, it is noticed that the zero torque regions are reduced with lowering the energization voltage. Another advantage noted was that semiconductor losses decreased by roughly 0.1% going from full V_{dc} de-energization to $0.5V_{dc}$. The reasoning behind this may be explained as follows: When the current tail is extended, more torque is being produced during the commutation period, which is form θ_{off} until current falls to zero. The PI speed controller, which outputs a θ_{on} reference in single-pulse mode, reacts to this change by slightly pushing forward θ_{on} to decrease the dwell time in order to reduce the torque production during the dwell period, which is form θ_{on} to θ_{off}. This has the effect of reducing the peak current at this particular speed and hence reducing the current at which the IGBTs are turned-off at the onset of commutation. This results in reduced IGBT turn-off losses. This opens the door for further performance optimization with the use of multilevel converters for SRM.

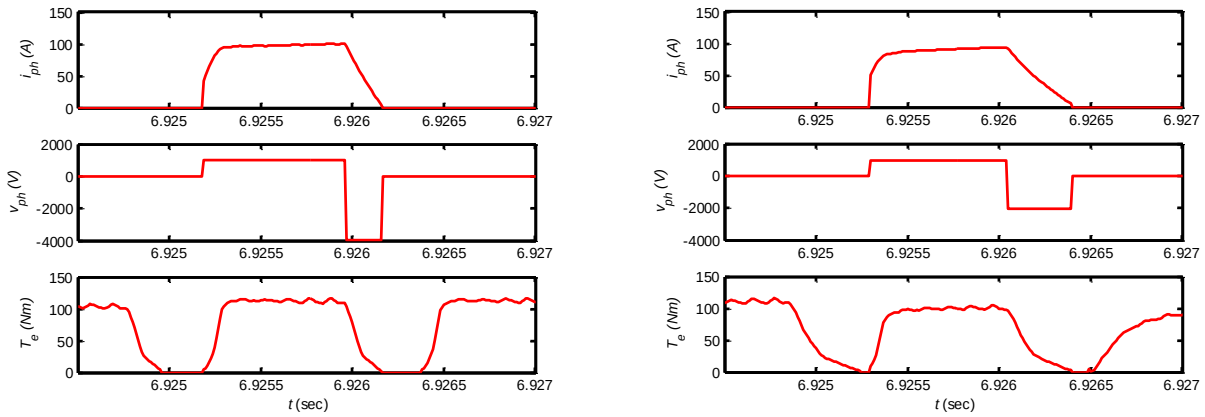


Fig. 5.36 Single-pulse mode waveforms at 25% speed and ~6% torque for (a) V_{dc} de-energization, (b) $0.5V_{dc}$ de-energization

5.4.5 Trends in Cell Capacitor Voltages

Though not of any significant consequence on the drive operation, it is interesting to note how the amount of time spent in P-mode strokes versus that spent in N-mode strokes varies with a change in the EVL. Fig. 5.37 shows waveforms of the submodule capacitor voltages, $v_{cell\text{-}n}$, for operation at 50% speed and 25% torque, where all four available energization voltages levels are feasible. Two things are noted. First, only with full V_{dc} energization are all the $v_{cell\text{-}N}$ identical. This is simply due to the fact that all cell capacitors are either switched in or out in this mode, so their charge/discharge patterns are identical throughout this mode operation. Second, the amount of time spent in P-mode strokes, which is identified by the cell capacitors charging, decreases when the EVL is lowered, while that for N-mode increases. Recall from chapter 4 that the amount of charge gained in a P-mode strokes is less than that lost in an N-mode stroke. The explanation for this is simple. Consider the case of full V_{dc} energization; for a P-mode stroke, no capacitors are charged during the dwell period, while all are charged during the commutation period. For an N-mode stroke all capacitors are discharged in the dwell period, whereas none are discharged in the commutation period. But the dwell period energy is far greater than commutation energy, and hence the $v_{cell\text{-}n}$ controller lets more P-mode strokes occur than N-mode to keep their voltages controlled at the required level. However, with lower EVLs, the difference between the dwell period and commutation energies is reduced due to the fact that in P-mode more capacitors are being exposed to charging current during the dwell period, while in N-mode strokes less capacitors are being exposed to discharging current during the dwell period. This results in almost equal number of P-mode and N-mode strokes, thus making the $v_{cell\text{-}n}$ variation waveform look more symmetrical.

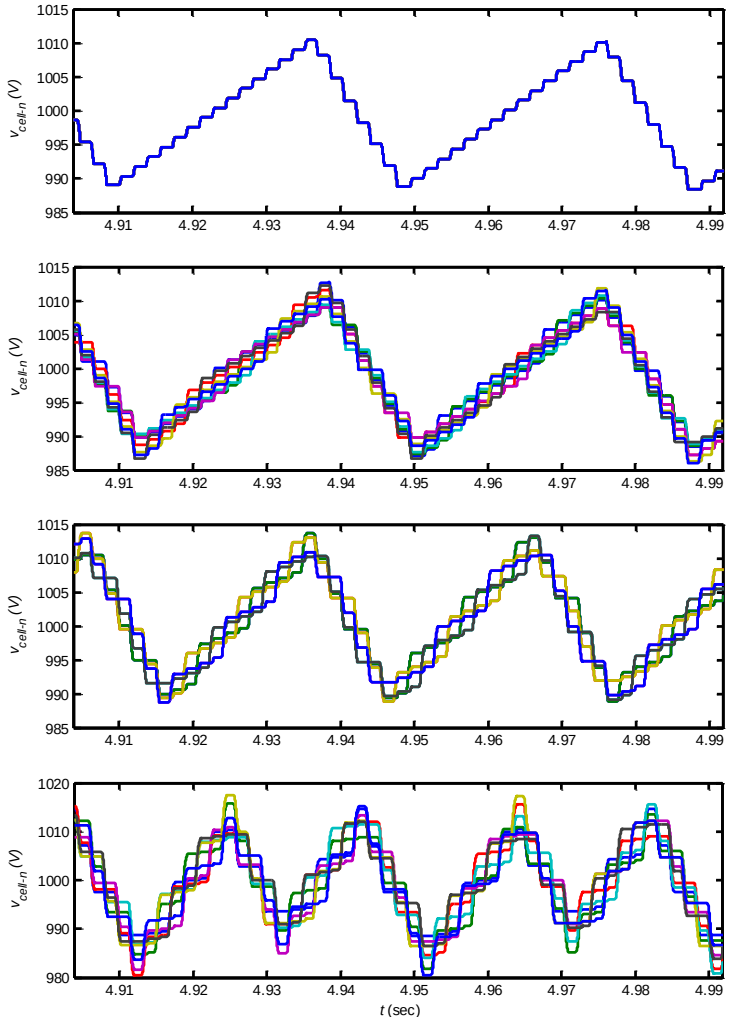


Fig. 5.37 Cell capacitor voltages for various EVLs - From top to bottom: V_{dc}, $0.75V_{dc}$, $0.5V_{dc}$, & $0.25V_{dc}$

5.5 Conclusion

In this chapter a comprehensive control algorithm was proposed for efficient operation through the use of single-pulse operation aided by the multi-level capability of the CCC SRM converter. A detailed explanation of the algorithm was given based on an 8-cell CCC SRM multilevel converter, though easy adaptation to any number of cells is possible. Relevant simulation results to both demonstrate performance as well as provide an example on how to select the appropriate EVLs for different torque-speed profiles were provided. Analysis of the results was also presented. Following is a summary of the conclusions from the work in this chapter:

- The proposed speed and current control algorithm for efficient operation in single-pulse mode, combined with the cell capacitor balancing and control algorithm explained in chapter 4, make up a comprehensive control scheme that is very useful for practical applications at the medium-voltage, multi-megawatt level, especially those that operate at high speeds.

- The proposed controller makes use of simulation data for initial settings only, but does not depend on it as it utilizes a PI controller that actively adapts to any variation to keep the drive in single-pulse mode.
- The availability of a selection of multiple EVLs not only provides flexibility, but also practicality that cannot be substituted. For example, by giving way to obtaining low peak phase current at low speeds, it enables operation in single-pulse mode that is otherwise not possible at low speeds with standard non-multilevel converters. In high-speed multi-megawatt drives, low speeds are themselves high, and so the ability to use the efficient single-pulse mode is a major advantage.
- It was clearly seen from simulations that in all cases lower EVLs resulted in lower switching losses.
- The availability of a multiple voltage levels even for the commutation (or de-energization) stage also opens the door for more possibilities that could be further investigated. One scenario was demonstrated where a lower demagnetization voltage significantly reduced the zero torque at low speed and low torque, which is typical of fan/compressor loads that have a quadratic torque-speed relationship.
- The simulation results presented thus help both in sizing the converter devices as well as making the appropriate choices for the controller.

Finally, it is worthy of mention that the extensive simulation that needs to be carried out is not considered overhead work, since most of the time it is required for SRM drive control design anyway in order to size the devices as well as predict settings that result in best performance. In case of the CCC SRM converter case, these same simulations could be used to make the appropriate choices for the EVLs that is required for the single-pulse controller design.

Chapter 6

Practical Considerations for the CCC SRM Converter and its Comparison to the CAB SRM Converter

6.1 Introduction

The three previous chapters covered the CCC multilevel converter concept, its principle of operation, control, basic design, and finally efficient operation in single-pulse mode. It was concluded that the CCC multilevel SRM converter was suitable for medium-voltage multi-megawatt applications, or for sub-megawatt applications that are either critical and hence require maximum uptime, or those that require high efficiency or improved performance. For such applications, especially the first two cases, reliability is the most important requirement, with efficiency coming second. Third in order of importance is perhaps the cost. Unless cost is prohibitively high, the choice of a drive for applications such as those targeted by the CCC SRM converter will not typically favor low cost options if the other criteria, like reliability and efficiency, are not fully met.

This chapter discuss practical considerations related to the CCC SRM drive, such as those listed above, and others. Section 6.2 sheds light on the reliability of the CCC SRM drive in light of different fault scenarios. Section 6.3 provides short notes on the efficiency of the CCC SRM drive, while section 6.4 offers a brief discussion on the cost of the CCC SRM drive. Other considerations like performance, volume, and weight of the drive are then briefly touched upon in section 6.5. In section 6.6, the choice of front-end converters (or rectifiers) for the CCC converter is discussed. Then, in section 6.7, the complete drive system consisting of one of the rectifier options and the CCC SRM converter will be used for a detailed qualitative comparison with the cascaded asymmetric bridge multilevel SRM converter, which is perhaps the only other SRM converter in literature that has the scaling capability of the CCC SRM converter, as well as modularity and redundancy features.

6.2 Reliability considerations for the CCC SRM converter

Semiconductor devices have a specified failure rate due to the effect of cosmic radiation [44]. No matter what the level of testing and design is, possibility of sporadic device failure cannot be eliminated. In general, it is considered that the more devices a converter has, the less reliable it is, due to the increased probability of any failure occurring. However, the inclusion of some level of redundancy can enhance the reliability of a converter. Finally, another factor that affects reliability of a converter is its usage profile, since this has a direct impact on the lifetime of its constituent devices. Therefore, the criteria upon which the reliability of a converter depends may be summarized as follows:

- Device count
- Redundancy
- Device lifetime based on power cycling and thermal cycling capabilities

6.2.1 Single Cell Failure

A significant advantage of cellular or modular converters is that in many of them failed cells may be eliminated while the converter is running, with little or no effect on operation. This is made possible by the use of spare or redundant cells, and having the capability of automatically deactivating a failed cell and activating a spare cell to replace it during operation. Besides avoiding downtime, an added benefit of using redundant cell is that other cell are protected from increased voltage in the event of a cell failure. This is true since the number of active cells before and after a single cell failure remains that same. Another feature in modular converters that can further enhance reliability and uptime is to have the capability of replacing a failed, deactivated, cell with a healthy one while the drive is running. This should not be difficult to implement since a deactivated cell does not carry any current and connections should be such that the cell can be taken out during operation following some appropriate procedure.

The deactivation of a failed cell without affecting operation may be implemented by the simple addition of a high-speed bypass switch or contactor in parallel to each cell, as shown in Fig. 6.1. This has been reported for practical applications of similar converters such as the ac cascaded H-bridge converter [45] as well as the ac modular multilevel converter [46], and it applies equally well to the proposed CCC SRM converter. When a failure occurs in a cell, all active switches in the cell are automatically turned off by the controller, and the high-speed bypass switch is simultaneously activated to maintain the flow of current and hence prevent interruption to operation. The high-speed bypass switch should be capable of handling the full load current. Also note that the illustration in Fig. 6.1 is rather simplistic, but in actual implementation the faulted cell should be electrically isolated, such as is illustrated in [45].

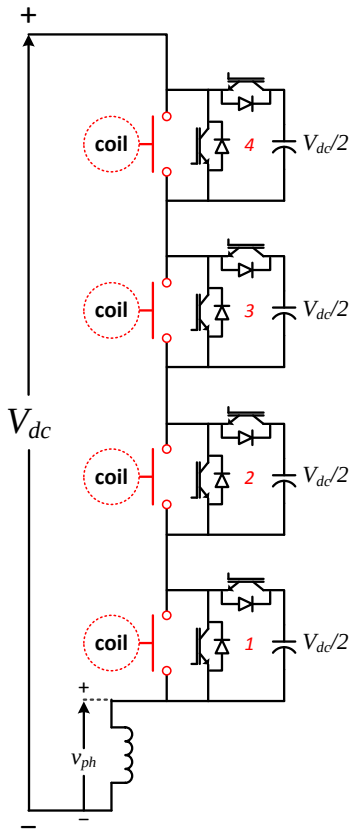


Fig. 6.1 4-cell CCC SRM converter with a bypass contactor for each cell

6.2.2 Jammed rotor

Next consider the failure scenario where the SRM rotor is suddenly jammed. Depending on the rotor position, unless the controller signals react to the fault, current in one or two phases will continue to flow since every SRM phase is programmed to conduct current as long as the rotor is situated between θ_{on} and θ_{off} with respect to that phase. And since the back emf drops to zero when the SRM is not rotating, a large net voltage develops across the active phase windings, with the potential of developing an excessively large current. The SRM has a unique advantage when compared to other machines in that the phase winding is always in series with the switches. This slows down the rate of rise of the current, thereby limiting the current in the switches and diodes until the circuit breaker is tripped or some other safety mechanism is activated. But in high-power machines, the stator resistance is low, which leads to a small RL time constant. Thus, there is still potential for developing very large currents before the circuit breaker is opened. Therefore, other protective measures must be taken in order to protect the converter from damage in case of such fault.

Considering the 2 MW SRM studied in chapters 4 and 5, a simple calculation may be performed to evaluate the current in this case. Let the phase current be positive (i.e. flowing downwards in Fig. 6.1), and

assume the worst case phase voltage given by the full dc link voltage, V_{dc} = 4000 V. The worst case inductance is the lowest inductance occurring at the unaligned position, given by L_{min} = 1 mH approximately. In the absence of back emf due to lack of motion, and also in the absence of variation in inductance due to the arrangement of the stator/rotor and hence magnetic circuit being steady, the circuit is reduced to a simple RL circuit. The instantaneous current for this circuit is given by $\frac{V_{dc}}{R_s}\left(1 - e^{-(R_s/L_{min})t}\right)$, where R_s is the stator winding resistance, given by 20 mΩ for this SRM. The steady state current is given by $\frac{V_{dc}}{R_s}$, which evaluates to 200 kA. Only a few percent of this current is enough to damage the switches and diodes. The surge current limit of high current diodes are in the order of several hundred kA, with a typical maximum duration of about half-cycle at line frequency, i.e., 10 ms for 50 Hz line frequency. For example, for the ABB 3300 V device [47] used for simulation in the 4-cell CCC SRM converter in chapter 4, the maximum diode surge current is 8 kA for a duration of 10 ms. For the 1700 V device [48] used in the 8-cell CCC SRM converter in chapter 5, the maximum diode surge current is 6.6 kA for a duration of 10 ms.

One protective measure that could be applied is for the controller to turn off all switches as soon as current in any of the phases rises beyond a given limit. This action can take place within a few microseconds since the current sampling rate can be very high. In the case of positive current (i.e. P-mode), turning off all switches forces the current to go against a negative voltage given by $-V_{dc}$, as it has to flow through all capacitors. As a consequence, the current starts to decay rather than rise, though at the expense of some rise in the cell capacitor voltages. However, usually switches are chosen such that they can tolerate twice the nominal cell capacitor voltage. The capacitors should also be undamaged through the process, since high-current film capacitors have very high impulse current capability [49].

On the other hand, if the current is negative, then again turning off all switches forces the current to go against a negative voltage given by $-V_{dc}$, where it will flow against a dc-link capacitor and a front-end until it dies out. In any case, an extra protective feature could be implemented where a press-pack thyristor could be placed in parallel to each cell, i.e., in addition to the high-speed bypass switch used for shorting out a failed cell. Press-pack thyristors have even higher surge-current ratings, which are in the order of few tens of kA [50]. These could be activated if, before the breaker is opened, current in the diodes approaches their surge current limit, or the allowed duration for carrying the surge current by the diodes is about to be exceeded. But when the thyristors are activated, current will not be flowing against a negative voltage, and so could rise quickly. However, by the time this suggested sequence of steps have taken place, the delay time of the circuit breaker should have elapsed. This addition of an extra thyristor to each cell has been reported in [46] for the ac modular multilevel converter, and is similarly applicable in the CCC SRM converter. The presence of such thyristor is also very useful in the case of a short-circuit fault between the

dc terminals in a high voltage system, where it performs a function similar to crowbar circuits used for the protection of traditional ac converter circuits.

6.3 Efficiency considerations for the CCC SRM converter

Next to reliability, efficiency is of much importance, especially for multi-megawatt applications where a significant amount of energy could be lost if efficiency is poor. The CCC SRM drive is able to maintain a high efficiency throughout the speed range. The following situations highlight how this is achieved. But first it should be noted that while the CCC SRM converter will be compared to the standard asymmetric SRM converter in the explanations below, the latter does not scale to higher voltages such as the CCC converter, and so would not be an option at that level. So whenever such comparison is performed, it should be understood that it applies to voltages levels where standard asymmetric SRM converter is feasible. This applies to the current section as well as the following ones. It is also noted that the advantages of the CCC SRM converter that will become apparent in fact hold at potentially any voltage level.

6.3.1 Efficiency at rated speed

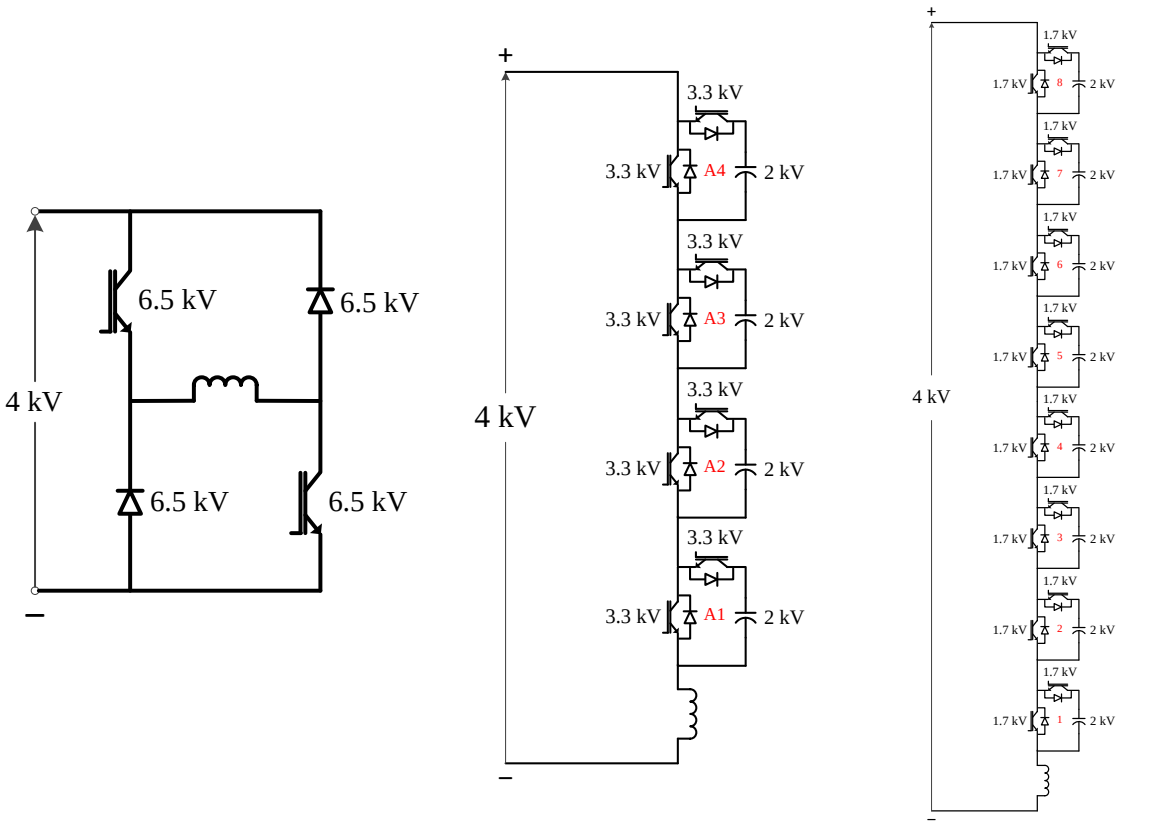
Near the rated speed in high-speed machines, the converter switches are forced to switch at a very high rate, and so switching losses are expected to be at their highest. In the CCC SRM converter, since the full dc link voltage must be used for energization to meet the high current demand, in every stroke all vertical switches cells (in P-mode) or all horizontal switches (in N-mode) will be engaged at every stroke.

Comparing the standard asymmetric converter to a CCC SRM converter, the former has less switches per phase, though each switch in the standard asymmetric converter has to switch a higher voltage compared to the CCC SRM converter. On the hand, while the CCC SRM converter, has more switches turning on and off per phase every stroke, each of them switch a lower voltage compared to the switches in the asymmetric converter. In both cases, the amount of conducted current and the duration of conduction is the same at rated speed since both use the same energization voltage at that speed, i.e., the full dc link voltage. It was shown in chapter 4 that more but smaller switches result in lower overall semiconductor losses and hence better efficiency. The reasoning behind this may be explained as follows.

The two major forms of semiconductor losses in a converter are switching and conduction losses. To illustrate the difference in losses, consider again the 2 MW SRM used in simulation in chapters 4 and 5. Three different converter arrangements will be considered for this comparison. The first arrangement consists of the standard asymmetric converter driving the 2 MW SRM. To withstand the 4 kV dc link voltage, the converter uses 6.5 kV IGBTs and diodes. As explained in chapter 4, in practical applications a slightly higher safety margin between the dc link voltage and the rated device voltage is desired, but for the purpose of comparison the 6.5 kV are considered to be sufficient. The second arrangement consists of a 4-

cell CCC converter driving the 2 MW SRM, where each cell capacitor holds 2 kV and so 3.3 kV IGBTS with anti-parallel diodes are used. Finally, the third arrangement consists of an 8-cell CCC converter driving the 2 MW SRM, where each cell capacitor holds 1 kV and so 1.7 kV IGBTS with anti-parallel diodes are used. One phase of each of the three arrangements are shown in Fig. 6.2.

Table 6.1 shows the relevant loss information from the datasheets of the three devices. Conduction losses are given by the current through the device times this voltage drop across it, known as the collector-emitter saturation voltage, or $V_{ce\text{-}sat}$. Hence, $V_{ce\text{-}sat}$ is a direct indication of a device's conduction losses. This information is readily found in datasheets of IGBT modules. Switching losses on the other hand are usually expressed in datasheets as energy losses per switching event, with E_{on} for turn-on losses and E_{off} for turn-off losses.



(a) SRM asymmetric converter (b) 4-cell CCC converter (c) 8-cell CCC converter

Fig. 6.2 Ratings of IGBTs in different SRM converter arrangements

TABLE 6.1
CONDUCTION AND SWITCHING LOSS DATA FOR DIFFERENT SRM CONVERTER ARRANGEMENTS

Converter	IGBT rating	$V_{ce\text{-}sat}$ @ 125 °C	E_{on} @ 125 °C	E_{off} @ 125 °C
Asymmetric	6500 V/750 A	3.9 V @ 750 A	6400 mJ @ 3600 V/750 A	5300 mJ @ 3600 V/750 A
4-cell CCC	3300 V/800 A	3.8 V @ 800 A	1380 mJ @ 1800 V/800 A	1250 mJ @ 1800 V/800 A
8-cell CCC	1700 V/800 A	2.6 V @ 800 A	250 mJ @ 900 V/800 A	300 mJ @ 900 V/800 A

Considering conduction losses first, it can be seen from Table 6.1 that $V_{ce\text{-}sat}$ only slightly increases with an increase in the IGBT module voltage rating. Going from a 3300 V used in the 4-cell CCC converter to a 6500 V IGBT module used in the asymmetric converter, the increase in $V_{ce\text{-}sat}$ is less than 3%. With devices conducting the same current in both converters at rated speed, and for the same duration per stroke, the conduction losses are then obviously higher with the 4-cell CCC converter – in fact it is almost double. Next, comparing the 8-cell CCC converter to the 4-cell CCC, the 3300 V IGBT modules in the latter have about 30% higher $V_{ce\text{-}sat}$, but the former has twice the number of IGBTs conducting every stroke at rated speed. Also since again both converters conduct the same current and for the same duration per stroke, the conduction losses are higher with the 8-cell CCC converter compared to the 4-cell CCC converter. Note that the SRM current varies in every stroke from 0 A to some maximum and then back to 0 A. The $V_{ce\text{-}sat}$ varies of each IGBT varies with the current. While the listed values for $V_{ce\text{-}sat}$ are only for the full rated current of each device, $V_{ce\text{-}sat}$ scales linearly with current, and so the comparison based on full load current $V_{ce\text{-}sat}$ is valid. Finally, note that the discussion omitted the diode losses. The trend in the diode voltage drop going from one voltage rating to another is similar to that in IGBTs, and so for brevity IGBT voltage drops alone were considered sufficient for this comparison.

Next, consider the switching losses, again only for IGBTs. The switching voltages at which E_{on} and E_{off} are given are different from what the converters for the 2 MW SRM with a 4 kV dc link voltage switch. However, they are close enough. Also the listed E_{on} and E_{off} are for full rated current, but they serve as an indication and so are sufficient for the purpose of this comparison. Based on the values in Table 6.1, for a 6500 V/750 A IGBT used in the asymmetric converter, a turn-on and turn-off event at 3600 V and 750 A results in 6400 + 5300 = 11700 mJ energy losses. Since the converter has two switches per phase, the losses per phase are 2 x 11700 = 23400 mJ. For the 4-cell, energy losses per phase for a turn-on and turn-off event are 4(1380 + 1250) = 10520 mJ. For the 8-cell, energy losses per phase for a turn-on and turn-off event are 8(250 + 300) = 4400 mJ. Thus, it is clearly seen that switching losses are significantly decreased going from the asymmetric converter to the 4-cell CCC converter, and then again significantly decreased going from the 4-cell CCC converter to the 8-cell CCC converter. This significant difference outweighs the reverse trend in losses, making the CCC SRM converter more efficient than an asymmetric converter

driving the same SRM at rated speed. The comparison also shows that using more cells comprised of devices with smaller voltage ratings results in further reduction in semiconductor losses.

6.3.2 Efficiency at medium and low speeds

At speeds below rated where the average applied voltage is controlled through chopping in the standard asymmetric converter, the CCC SRM converter displays even more advantages with regards to efficiency. First, the multilevel capability of the CCC SRM converter may be used to apply a lower voltage in single-pulse mode, as shown in chapter 5. In this mode each switch is only turned on and off once per stroke. Also since in this mode current diodes are not forcefully switched off while conducting current, but rather the current dies out naturally in them, the diode turn-off losses are completely eliminated. The diode turn-off losses are in fact the major loss in a diode, with diode turn-on losses being much smaller and often neglected in calculation. Therefore, by reducing the number of times the switches turn on and off to a minimum, and by eliminating the diode turn-off losses, the converter efficiency is well improved going from the standard asymmetric to the CCC SRM converter. Of course operation in single-pulse mode may not always be possible, but even if chopping occurs, the fact that the CCC SRM converter undergoes chopping at lower voltages still reduces the number of times switching takes place as well as the energy loss per switching event.

Further to this, efficiency improvement in the CCC SRM converter is also displayed in the machine core losses. The core losses are expected to be lower when the voltage switched is lower, since the lower dv/dt results in a lower rate of change of flux, and hence lower core losses. This is true whenever a lower energization voltage level is used, i.e., when any voltage level below the full dc link voltage is used by the CCC SRM converter. But operating points where the full dc link voltage is required, machine core losses are expected to be the same in both CCC SRM converter and the standard asymmetric converter.

Finally, the cell capacitor losses, which are present in the CCC SRM converter but not in the standard asymmetric converter, should also be considered. These losses are typically small, since the equivalent series resistance (ESR) of capacitors can be at least an order smaller than the stator winding resistance. For example, consider again the 2 MW SRM considered for simulation in chapters 4 and 5. While the phase resistance for this SRM is 20 mΩ, the ESR of a typical high-current film capacitor is less than 1 mΩ. Therefore, even an 8-cell version will have total ESR losses per phase that are about ten times smaller than the stator winding resistive losses in that phase. Also the capacitors do not conduct full load current. Only some of the operating modes, as explained in chapter 3, have the phase current going through the capacitors. And with the ESR losses being proportional to the square of the rms current going through the capacitor, cell capacitor ESR losses are hence expected to be much lower than stator winding losses (known as copper losses). Thus, ESR losses may be neglected in efficiency calculations.

6.4 Cost considerations for the CCC SRM converter

While low cost is always desired, cost carries less weight in the applications targeted by the CCC SRM drive. It is obvious that the CCC SRM converter, and in fact any multilevel converter with a cellular structure, requires a high number of semiconductor devices. Consider the example arrangements in the previous section, a phase leg of an asymmetric SRM converter had two 6.6 kV IGBTs and two 6.6 kV diodes per phase, whereas an equivalent CCC SRM converter had eight 3.3 kV IGBTs with anti-parallel diodes. Nevertheless, in the following it will be shown that the cost increase in adopting the CCC SRM converter is not excessively high, and that this increase is justified given the benefits of this new converter.

6.4.1 Semiconductor cost

Considering high-voltage IGBT modules, the cost of a module for a given voltage/current rating could be more than twice that of module with the same current rating but half the voltage. However, such relationship cannot be generalized since it depends on many factors like the volume sold, the type of internal isolation, package size, and others. However, it is also true that the 1200 kV and 1700 kV IGBT modules are highly demanded, which makes them the subject of steady improvement in chip design [38], and also potentially contributing to their cost-competitiveness. Also the lower the voltage of an IGBT module, the more likely it is to be available in combined packages. For example, modules consisting of two IGBTs (each with an anti-parallel diode) are usually available for IGBTs rated 3300 V, 1700 V, and below, but not available for 4500 V and 6500 V IGBTs. Such modules are either already connected as half-bridge cells or left unconnected. Such modules could be used directly in the chopper cells of the CCC converter, which simplifies design and potentially reduces cost. For the 6500 V level an IGBT in series with a diode may be found that can be used to make up half the phase leg of the asymmetric converter, but the device current ratings tend to be low at that voltage level.

Given this advantage of the availability of high-current multiple-device modules at lower voltages, as well as the fact that the semiconductor module cost could be less than half when voltage rating is halved, the increase in semiconductor cost going from the asymmetric converter to the CCC converter is rather acceptable and less than it may seem to be. However, it should also be remembered that more switches require more gate drivers. As for heat sinks and other cooling arrangements, no changes are expected between the asymmetric and CCC converters, since the overall heat dissipation is similar – in fact it is less with the CCC SRM converter given its lower semiconductor losses.

Next, comparing the semiconductor cost of a 4-cell CCC SRM converter to that of the 8-cell version, the latter may in fact cost less. An 8-cell requires twice as many semiconductor modules as the 4-cell version. But if the less-than-half cost trend for semiconductor modules with half the voltage rating holds true, then the total cost of the 8-cell using converter should be slightly less, given that it uses devices

with half the voltage rating. But with twice the number of gate drivers, the overall cost should be more or less the same.

6.4.2 Capacitor cost

The comparison of semiconductor cost above showed that the increased semiconductor cost going from an asymmetric SRM converter to a CCC SRM converter may not be significant, especially for multi-megawatt applications or highly critical applications. Also it was pointed out the scaling an SRM converter almost has no effect on the semiconductor cost. However, the majority of the cost increase comes in the capacitor category. A unique feature of most cellular multi-level converter structures is the use of a capacitor in every cell, since this is what holds the voltage of the semiconductors in that cell to a specified voltage, thus protecting them from over-voltages. So while the cell capacitor cost is considered extra, the benefits it brings about in terms of enabling modularity and most advantages that have been explained earlier, like improved reliability, improved efficiency, multilevel capability, easier manufacturability, justifies this cost. Also, such cellular structures are the easiest to scale amongst all multilevel converters proposed in so far. Finally, it should be remembered that as mentioned in chapter 1, the first cost of the converter could represent as little as less than 5% of the motor's life-cycle cost, with the motor energy costs being 90% or more.

6.5 Other practical considerations

The CCC SRM converter tends to be slightly larger and heavier than the standard asymmetric SRM converter described, mainly due to the increased number of capacitors. Therefore, the CCC SRM converter is not suitable for applications requiring particularly low volume or low weight. Multi-megawatt converters are usually not of that category, such as high-speed compressors in the oil and gas industry. But some sub-megawatt may have some size and/or weight restrictions.

With regards to other performance criteria like acoustic noise and torque ripple, it was mentioned earlier that the multilevel capability of the CCC SRM converter could lend itself useful in better applying techniques proposed to control the two. For torque ripple, techniques involving current shaping have been proposed to reduce it [8, ch. 5]; the different energization voltage levels in the CCC SRM converter provide more flexibility in terms of attaining a certain current profile. Acoustic noise may be reduced by a combination of appropriate machine design as well as certain current shaping techniques [8, ch. 7], which again can benefit from the multilevel advantage of the CCC SRM. The multilevel advantage manifests itself in the fact that adding extra pulses at high speeds becomes more of a possibility with the availability of the lower energization voltages – since at high speeds extra pulses with full dc link voltage switching leads to excessive switching losses. It is such advantages performance advantages, along with the improved

efficiency, that makes the CCC SRM converter also a good candidate for high-performance applications even below the medium voltage level in the sub-megawatt range.

6.6 Choice of front-end converters for the CCC SRM converter

Two main criteria are required for the front-end rectifier of the CCC SRM converter. First, it should be able to provide a controlled dc link voltage to the CCC SRM converter, since the latter is basically a voltage source converter. Second, the rectifier should have regeneration capability, or in other words be able to conduct current in both directions, i.e., from the source to the dc link, and vice versa. This second criteria is due to the CCC SRM converter returning dc current to the dc link whenever one or more phases are in N-mode, i.e., using negative phase current. The use of bi-directional current phase current in the CCC converter is necessary to control the cell capacitor voltages. Choice of the appropriate front-end depends on the operating voltage of the drive.

6.6.1 Front-end Options at Lower Operating Voltages

For an SRM operating from 2.6 kV dc link, a standard three-phase PWM rectifier consisting of six high power 6.5 kV IGBT devices may be used for front-end converter or rectifier. This converter is designed to maintain a constant dc link voltage. It can also operate in the two modes or quadrants required by the CCC SRM converter; the first mode is where current flows out of the converter into the dc link capacitor and the CCC SRM converter, while the second is where current flows back from the CCC SRM converter back into the dc link and the front-end rectifier. An input ac voltage of 1800 V would be appropriate for such rectifier. This limitation on voltage is due to the safety margin required for IGBT devices in a rectifier being larger than that of motor-side converter or inverter. The reason for this is that the former is connected to the network and so is exposed to over-voltage transients of larger magnitude. Example guidelines for sizing rectifiers made of high power semiconductors may be found in [24]. The three-phase PWM voltage-source rectifier is well established in industry. Besides its simplicity and ease of control, the standard three-phase PWM voltage-source rectifier has the following advantages as rectifier:

- Near sinusoidal currents may be obtained by operating at a sufficiently high PWM frequency, aided by an input filter inductor
- Ability to operate at unity power displacement factor in both motoring and regenerative operating modes [51]

The standard three-phase PWM rectifier using six IGBTs is categorized as a two-level converter, since its ac line-line voltages consist of pulses of either $+V_{dc}$ or $-V_{dc}$ only, where V_{dc} is the dc link voltage. A three-level converter on the other hand can additionally provide 0 V line-line voltage. A three-level converter based also 6.5 kV IGBTs can operate at roughly twice the 2.6 kV dc link voltage possible with

the two-level converter. Examples of three-level AC converters include the neutral-point clamped or diode clamped converter, active neutral point clamped converter, and capacitor-clamped converter, but there are also others. Operation of the diode-clamped converter as rectifier has been reported in literature. Even higher dc link voltages may be achieved if the high-voltage 9.5 kV IGCTs are used. For example, a neutral-point rectifier using 9.5 kV IGCTs can be interfaced directly with the 7.2 kV ac distribution voltage. The dc link voltage in such configuration could be as high as 13 kV to 14 kV.

The two-level and three-level rectifier options mentioned above satisfy the basic criteria for a front-end to the CCC SRM converter, but they lack the modularity and built-in redundancy capabilities that may be desired in multi-megawatt or critical sub-megawatt applications. Also beyond the 13 kV to 14 kV dc link voltage, four-level or five-level configurations must be used, where both topology and control are complex. In fact in practice the four-level or five-level configurations of the above-mentioned converters are very uncommon, with mainly the three-level version finding way in applications. A more appealing option lies in the ac modular-multilevel converter (MMC) that was described in the literature review in chapter 1.

6.6.2 Front-end for the Medium-Voltage Range

The ac MMC maybe the most suitable front-end converter for the CCC SRM converter. It naturally meets both criteria of providing a controlled dc link voltage and having the ability to operate with both positive and negative dc link currents. In fact the main intended application of the ac MMC was high-voltage dc (HVDC) transmission applications, where one ac MMC would be at the sending end (as rectifier) and another at the receiving end (as inverter). The ac MMC was also suggested as an inverter for ac drives in numerous publications, and also shown to operate as rectifier as well as in the back-to-back configuration. The ac MMC is also easily extendable to high voltages, making the whole system with the ac MMC front-end and CCC converter motor-end easily scalable to potentially any voltage level. Another important advantage of the ac MMC is that it dispenses with the large dc link capacitor, thereby making the complete drive system fully modular and thus more reliable. Fig. 6.3 depicts the complete SRM drive system with the ac MMC as front-end rectifier and the CCC converter as motor-side converter.

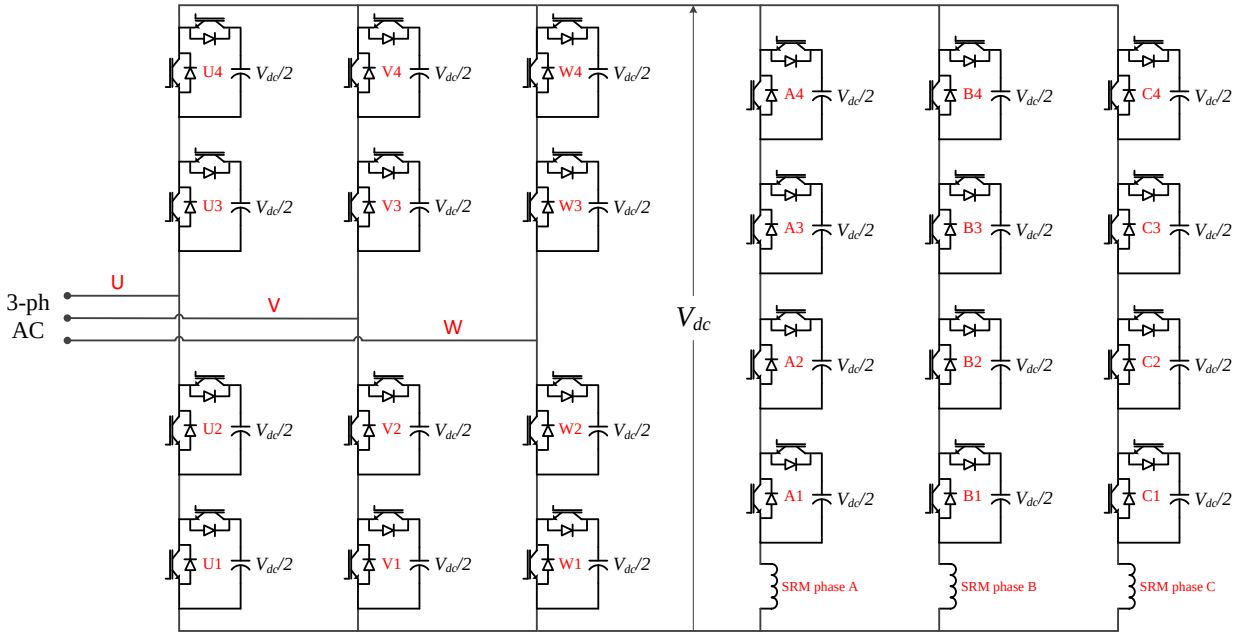


Fig. 6.3 Complete SRM drive system with ac MMC as front-end rectifier and CCC converter motor-side converter

6.6.2.1 Configuration of the ac MMC

Each phase leg of the ac MMC consists of two sets of series chopper cells, where each set is referred to as an *arm*. The two arms are separated by the connection point of the ac terminal. Due to the instantaneous difference in voltage between the different phase legs, a current circulates through the phase legs, without passing through the load. This so called circulating current is controlled by means of an inductor and an appropriate control strategy. The chopper cell operates in the same way as the CCC SRM converter, i.e. it either inserts the capacitor or bypasses it, with each occurring in either current direction. When a cell capacitor is conducting the cell is said to be on, otherwise it is in the off position.

6.6.2.2 Operation and voltage ratings in the ac MMC

The basic operation of the ac MMC was explained in chapter 1. One of the fundamentals of ac MMC is that at any instant the total number of cells that are on must be such that the total voltage across the whole leg must equal the dc link voltage, V_{dc}, within some control tolerance. Let N be the total number of chopper cells per phase leg. Since each of the two arms in a phase leg has an equal number of cells, it follows that each arm will have $N/2$ cells. If each cell capacitor is controlled to a voltage of $2V_{dc}/N$, then exactly half (or $N/2$) of the cells in a phase leg need to be on at any given time. For example, in an MMC with $N = 10$, if 3 out of the 5 upper arm cells are on, with a 4th upper arm cell in PWM mode, then at the lower arm should have 1 cell on and a 2nd in PWM mode. The two cells in PWM will be complementary to each other such that the total voltage from the positive terminal of the top-most cell to the negative terminal of the bottom-most cell is always maintained at V_{dc}.

It is interesting to note that the nominal cell voltage in the ac MMC converter with N cells per phase leg is equal to the nominal cell voltage in the CCC converter with also N cells per phase leg. But recall from chapters 3 and 4 that while each cell capacitor in the CCC SRM converter needs to be controlled to $2V_{dc}/N$, the capacitors are initially charged to slightly above 50% of this nominal voltage, i.e., around V_{dc}/N. The same external source of voltage $2V_{dc}/N$ may be used to charge the cell capacitors of both the CCC converter as well as ac MMC, if two cells of the CCC converter are charged at once. Since the cells are in the CCC converter are in series, each cell capacitor will be then charged to V_{dc}/N only as desired. Alternatively, if the ac MMC has twice as many cells as the CCC converter, such that the nominal voltage of each cell in the ac MMC is equal to the initialization voltage of the CCC SRM converter cells, then the same charging source may be used with charging one cell at a time in both converters. The use of more cells at the ac MMC front-end may be desirable anyway as it results in better input power quality. As an example, for the 4-cell CCC SRM converter considered in chapter 3, the nominal voltage per cell was $2V_{dc}/N$ = (2 x 4000)/4 = 2000 V. The initial charging voltage is about half of that, or 1000 V. If the ac MMC with the same dc link voltage has eight cells per phase leg, or equivalently four cells per arm, then also the nominal cell voltage will be 1000 V, with four cells required to be on at any time. The same charging source of slightly above 1000 V could then be used for initial charging.

Finally, with regards to the voltage ratings of the devices, if the number of cells per phase leg is the same in both the ac MMC and the CCC converter, then the voltage rating of the cell IGBTs is the same in both converters. Also since the power processed by each phase in both converters is roughly the same, the current ratings of IGBTs in both cases is expected to be similar. Therefore, the same IGBT module packages may be used for both converters, which is more convenient for construction as well as for maintenance.

In the following section, the complete system consisting of the AC MMC front-end with the CCC converter at the motor-end is carried over for a comparison with another converter that is also suitable for medium-voltage, multi-megawatt SRM applications. This converter was reported in [31], and will be referred to as the cascaded asymmetric bridge SRM converter. A detailed comparison will be provided which covers many aspects ranging from operation and performance to scalability, reliability, complexity, cost, and input-side power quality, among others.

6.7 Comparison of proposed CCC SRM converter to CAB SRM converter

The ac cascaded H-bridge (CHB) converter described in the literature review in chapter 1 is the most popular choice for high-voltage ac drive applications, being modular and scalable. It also has built-in provision for redundancy. An adapted version suitable for SRM drives, the cascaded asymmetric bridge converter or CAB converter, was presented in [31].

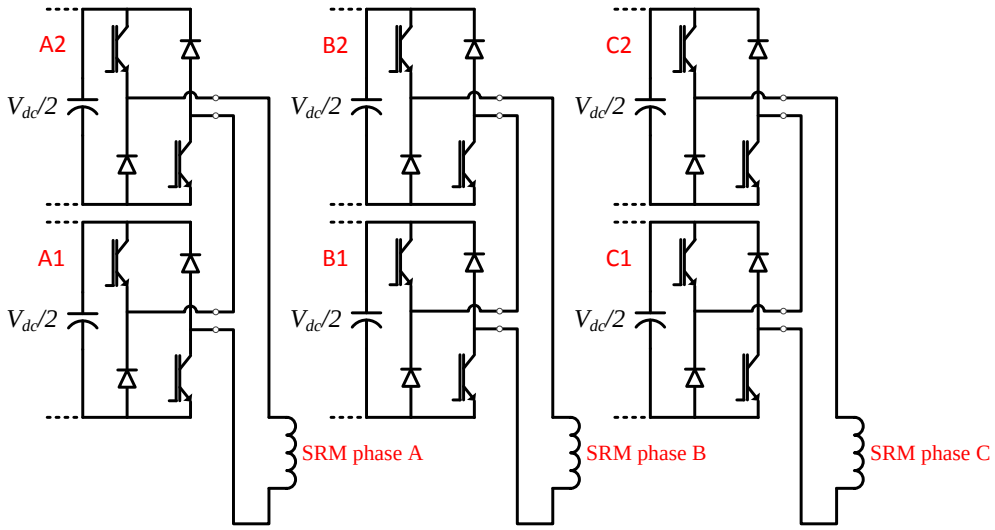
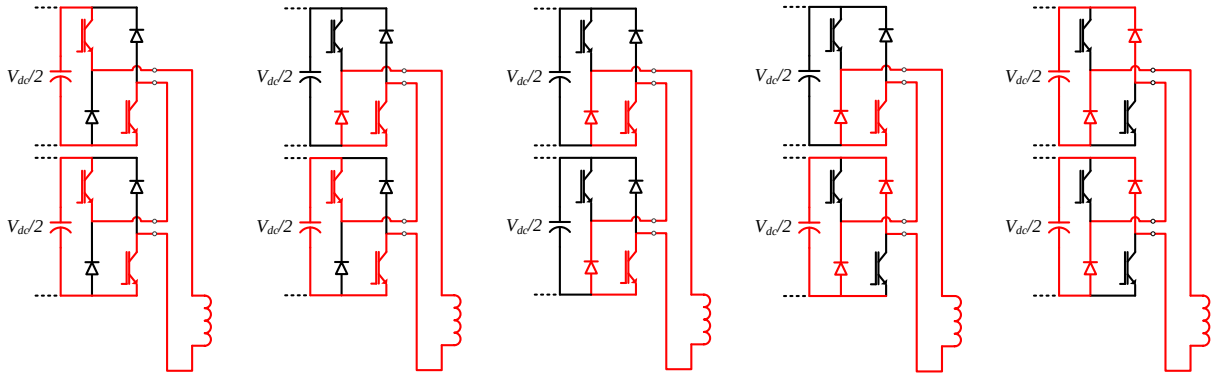


Fig. 6.4 Cascaded Asymmetric Bridge (CAB) converter for a 3ph SRM drive



(a) $v_{ph} = +V_{dc}$ (b) $v_{ph} = +V_{dc}/2$ (c) $v_{ph} = 0$ (d) $v_{ph} = -V_{dc}/2$ (e) $v_{ph} = -V_{dc}$

Fig. 6.5 Possible voltage levels in the 2-cell CAB SRM converter

The topology of the CAB SRM converter is redrawn in Fig. 6.4 for a 3ph SRM drive. Each phase is composed of an arbitrary number of asymmetric-bridge cells, each one similar having being identical to one phase leg of the standard asymmetric SRM converter. Operation of the CAB is rather straightforward. Each cell can force a voltage of $+V_{dc}/2$ by turning on both switches. Then, once current is flowing in the phase and through the cell, if one of the switches in a cell is turned off, the current circulates through the switch and the diode opposite to it, and leaves the cell without flowing through the capacitor. In this mode, the voltage contribution form this cell is 0 V. Finally, when current is flowing, if both switches in a cell are turned off, current is forced to flow through the capacitor in reverse direction, thereby making the voltage contribution of that cell $-V_{dc}/2$. In this manner, the CAB SRM converter is able to produce the same five different voltages using only two cells. Fig. 6.5 illustrates how the five different phase voltages, v_{ph}, are obtained with the two-cell CAB SRM converter. It may be easily noted that intermediate voltages, other than $v_{ph} = +V_{dc}$ and $v_{ph} = -V_{dc}$, may be produced by more than one combination of cell states.

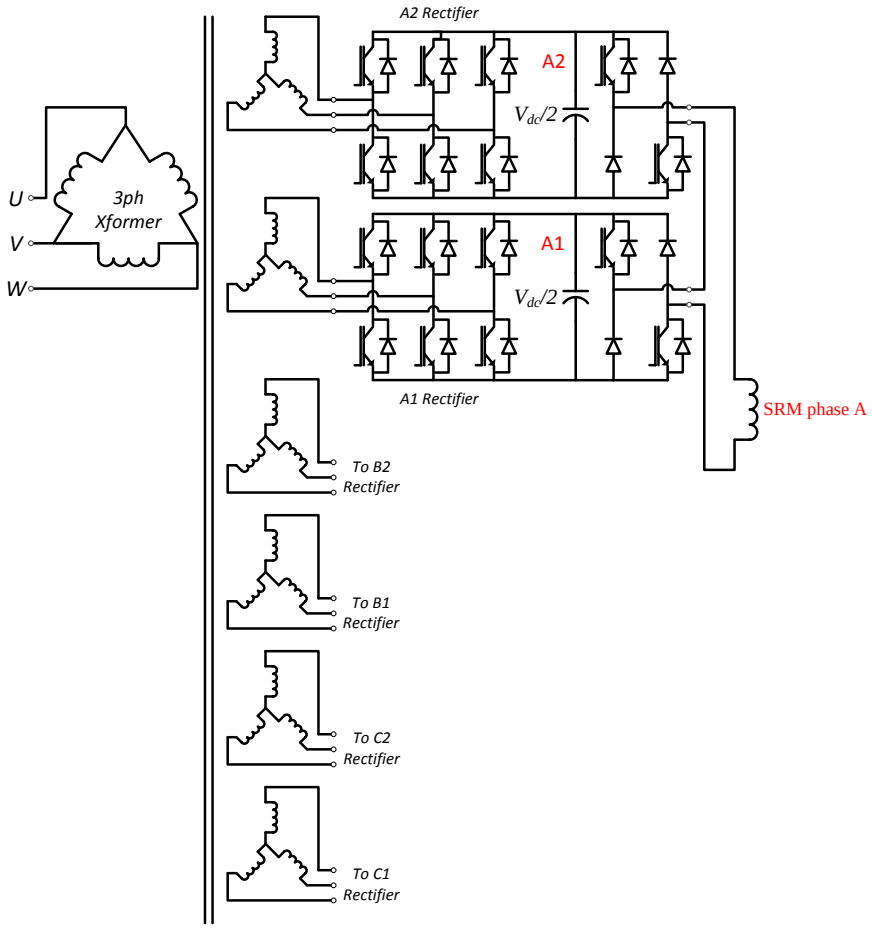


Fig. 6.6 Cascaded Asymmetric Bridge (CAB) converter for a 3ph SRM drive, including front-end

The CAB converter is not supplied from a large dc bus; rather each cell needs to have its own dc source. These sources are typically obtained from a large secondary transformer with as many secondary windings as there are cells in all phases of the converter. Each secondary winding feeds a rectifier module that connects to the filter capacitor in each cell, as shown in Fig. 6.6. The secondary windings are usually phase shifted to cancel out harmonics on the AC supply side and hence limit injection of harmonics into the network or source. The comparison will be carried out between the following two systems:

- System 1 (MMC + CCC converter) – as shown in Fig. 6.3: The first drive system is composed of a three-phase ac MMC front-end converter, with four cells per phase leg (or two cells per arm). The motor-end converter is a CCC SRM converter with four cells per phase leg.

- System 2 (CAB with special input transformer) – as shown in Fig. 6.6.: The second drive system consists of the CAB SRM converter, with its sources supplied by a transformer with six sets of three-phase secondary windings, each supplying a three-phase rectifier cell, as shown in Fig. 6.6.

6.7.1 Motor-end converter device count and device blocking voltage

Each phase leg of the CCC SRM converter uses eight IGBTs, each with an anti-parallel diode. The CAB converter uses also eight devices, but those are four single IGBTs (with no anti-parallel diode) and four single diodes. The voltage ratings of all devices in both converters are the same, since they all are required to withstand a voltage of $V_{dc}/2$. In this category the CAB converter is considered superior due to the lower device count though it produces the same number of voltage levels as the CCC converter.

6.7.2 Motor-end converter device current ratings

Since conduction of current alternates between the IGBTs and the diodes throughout operation, each device carries only a certain percentage of the phase current and hence needs to be rated accordingly. Also different operating modes that produce the same voltage but with different switch state combinations are alternated between to keep thermal balancing among devices. This alternation should also be taken into consideration when evaluating how much of the full phase current each device carries.

Considering only rated speed operation at rated power since phase current is highest at this operating point, full dc link voltage needs to be applied in every stroke. In this case only one combination of switch states in both converters will work. In the CCC converter, if it is a P-mode stroke, all four S_v IGBTs conduct from θ_{on} to θ_{off}, while all four D_h diodes conduct from θ_{off} up to the extinction angle, θ_c. These angles are defined in chapter 2. For an N-mode stroke, all four S_h IGBTs conduct from θ_{on} to θ_{off}, while all four D_v diodes conduct from θ_{off} up to the extinction angle, θ_c. For the CAB converter, all four IGBTs conduct from θ_{on} to θ_{off}, while all four diodes conduct from θ_{off} up to the extinction angle, θ_c.

By inspection of the simulated waveforms at rated conditions in chapter 4, it may be approximated that roughly 80% of the current occurs between θ_{on} to θ_{off}, while the remaining occurs between θ_{off} to θ_c. Therefore, for the CAB converter, the IGBTs must be able to handle 80% of the phase current, while the diodes must be able to handle 20%. For the CCC converter, the current is further split due to alternation between P-mode and N-mode strokes. At rated conditions, about 84% of the strokes are P-mode, based on the simulations in chapter 2. Therefore, the S_v IGBTs must be able to handle 80% of their 84% share, which is about 67.1% of the phase current. The D_h diodes should then be capable of handling 20% of their 84% share, which is about 16.8%. Using similar calculations for the N-mode, it is estimated that the S_h IGBTs must be able to carry 12.9% of the phase current, while the D_v need only to be rated for 3.2% of the phase current.

However, it is important to note that while the above calculations assume that ratings are based on average current carrying capability, the peak current should also be taken in to consideration. Typical peak current ratings for high-power IGBTs are usually twice that of their average current ratings. However, a condition is that this peak does not occur for longer than a specified duration, which is typically 10 ms for

the high-power IGBTs. This condition may be violated at low speeds in the order of 1000 r/min. Therefore, for low-speed machines, the peak current rating should be used, but for high-speed machines the average current rating may be used, as long as the module is thermally capable of handle that current given the thermal management system used for the drive system.

In this category, the CAB has a slight advantage due to the more uniform distribution of current among the devices. The CCC converter hence requires more kVA capacity to deliver the same power.

6.7.3 Front-end converter device count and device blocking voltage

Each phase leg of the MMC uses eight IGBTs, each with an anti-parallel diode. The CAB converter uses two rectifier cells each with six IGBTs with anti-parallel diodes, for a total of 12 IGBTs per phase on the front-end. The voltage ratings of all devices in the front-end are gain the same, given by $V_{dc}/2$. In this category the MMC + CCC converter system may be considered superior due to the lower device count.

6.7.4 Front-end converter device current ratings

The MMC front-end has a total of six arms, while the CAB front-end has a total of six rectifier cells. Therefore, it may be estimated that each arm processes one sixth of the power flow, and likewise for each rectifier cell. In the MMC, each arm has four IGBTs with an anti-parallel diodes. On the other hand, each rectifier cell has six IGBTs with an anti-parallel diodes. Therefore, the current rating of each IGBT in the MMC is expected to be higher than that of the IGBTs in the CAB rectifier cells. Also, current distribution among the devices within an MMC cell is not even. Therefore, oversizing is a possibility in the case of MMC cells, since often a cell is made of a dual-IGBT module, where one is forced to have the cell rated to the worst-case current occurring in any of its devices. Therefore, in this category, the CAB front-end may be preferred since it features more even power distribution among its front-end devices.

6.7.5 Installed kVA Capacity

Commercial devices come in discrete steps of current and voltage ratings. If for simplicity it is assumed that the current ratings are all uniform, the kVA capacity is easier to estimate. This may be done in practice anyway, since some oversizing for some of the components in multi-megawatt applications or critical sub-megawatt applications is more of a possibility since the semiconductor cost does not represent a dominant percentage of the total system cost and therefore reliability and uniformity may be preferred over cost. Therefore, if for example a dual IGBT module is used in case of the CCC and MMC converters, as well as the rectifier cells, and if the CA converter uses modules consisting of an IGBT in series with a diode, then the module current rating will be according to the device that carries the highest load.

For the motor-end, the CCC converter device count is eight per phase, with each device including an IGBT and anti-parallel diode, which makes 16 total semiconductor devices. For the CAB converter, if

IGBTs with no anti-parallel diodes then the total semiconductor device count per phase is only 8. However, if due to market availability or other reasons the modules that include the anti-parallel diodes are used in the CAB converter, its total semiconductor device count per phase is 12.

Therefore, the CCC converter will have 1.5 to 2 times the kVA capacity of the CAB converter, depending on the IGBT type used in the CAB converter. Therefore, the CAB converter has the edge in this regard.

6.7.6 Capacitor count

The first system uses a total of 12 capacitors in the front-end MMC and 12 in the motor-end CCC converter. On the other hand, the CAB system uses only six capacitors in the whole system. However, each capacitor in the second system is expected to be of larger size than those used in the first system. But with the capacitor count in the second system being much higher, the total installed energy storage capacity in the second system is also expected to be higher. Therefore, the CAB system also has an advantage in this category.

6.7.7 Transformer requirement

The CAB system requires a large expensive transformer with multiple secondary windings that could make the connections increasingly complex as the converter is scaled with more cells to accommodate higher voltages. On the other hand, the first system is transformer-less. And even in situations where a transformer is required for isolation between the drive and the network, a standard three-phase transformer with only three windings on each side would be installed. Also with such transformer arrangement for the CAB system, the upgrading of a system more difficult than in the MMC + CCC converter system. Therefore, the MMC + CCC converter system has the advantage in this category.

6.7.8 Motor-end converter efficiency

It is noted form the operating modes of the CCC converter explained in chapter 3, and those of the CAB converter explained earlier in this section, that for any given synthesized voltage always the same number and same type of devices conduct in both cases. For example, to energize full dc link voltage, four IGBTs conduct. To de-energize with full dc link voltage, also four IGBTs conduct. To apply 0 V in any of the converters, two IGBTs and two diodes conduct. And given that it is expected for the chosen device modules to be almost identical in both cases, the efficiency at the two different motor-end converters is also expected to be almost identical. Capacitor losses occur within the cell capacitors of the CCC converter, and they also occur in the capacitors of the CAB converter cells. While the capacitor losses may not be identical, as earlier explained they are much lower than the other losses and so may be neglected. Therefore, neither converter has the edge in this category.

6.7.9 Front-end converter efficiency

If no transformer is used in the MMC + CCC converter system, then it will have the advantage in terms of front-end efficiency, since the CAB converter suffers from transformer losses, which are typically 1% of the system power. Besides that, both front-end converters are highly efficient, and little difference is expected in this regard. In this category the MMC + CCC converter system has the advantage due to its ability to operate without a transformer and hence having better efficiency in such cases.

6.7.10 Control complexity

The control of the motor-end converters is very similar, and follows standard SRM control but with multi-level capability. The only difference is that the CCC converter has the additional cell capacitor control and balancing, but which is quite simple. In both cases control complexity does not increase significantly with scaling the converter.

Front-end control is standard and straightforward for the rectifier cells in the CAM system. For the MMC extra control for balancing and controlling cell capacitor voltage is required. However, this is also not complex and has been applied in practice.

The CAB system has a slight advantage in this aspect as it does not require any capacitor control or balancing. But since capacitor control in the MMC + CCC converter system is not complex, the advantage for the CAB system is only minor.

6.7.11 Redundancy

Both systems have the capability of including redundant cells and shorting out any failed cell and replacing it with one of the redundant cells so as not to interrupt operation. However, if a cell fails in the CAB converter system then both the front-end and motor-end side of the cell become unusable. For example, if the motor-end part of the cell fails, its rectifier cell is also prevented from conducting current. If a redundant cell is available to replace it, then operation is not affected. However, if no redundant cell is available, then besides the reduced capability on the motor-end, the front-end ac system experiences and unbalance. Some algorithms have been proposed to deal with that unbalance [45]. However, if a module fails in the MMC + CCC converter system, then only the side on which the failure occurred is affected. This is because the front-end and motor-end modules are independent.

Another point to note in this regard is that including redundant cells in the CAB converter system means also adding extra secondary windings, which makes adding redundant cells more complex and more costly. In the MMC + CCC converter system, only the cells are added, which is less complex and less expensive. Therefore, the MMC + CCC converter system has a slight advantage in this category due to the

simplicity of including redundancy as well as the independence of front-end and motor-end in the event of a failure.

6.7.12 Input power quality

The front-end converters in both systems have the capability if drawing power form the network with very low distortion. In the MMC this is achieved due to the multilevel effect and the smaller switching steps as more cells are added. In the CAB converter system front-end, the combined effect of PWM in the rectifier cells along with the cancellation of harmonics due to phase shifting the transformer secondary windings with respect to each other, results in very high input power quality. Also both systems are capable of producing near unity power factors. Therefore, neither system has an edge in this category.

6.7.13 Ease of upgrading system

Assuming both systems use a transformer, and assuming that the transformers are oversized to accommodate future scaling of the system to a higher voltage, then the scaling of the MMC + CCC converter system is simpler and costs less as explained above.

6.7.14 Gate drive and heat sink requirements

Given that the total number of IGBTs is the same in both systems (including motor-end and front-end), the same number of gate drives are required. As for sinks, again a similar volume of heat sinks is expected for both systems since losses are expected to very similar on both ends – even though the heat sinks would be arranged different in each system due to their different configurations.

6.7.15 Other considerations

Below are few other considerations related to the comparison between the two systems:

- The CAB converter system is not compatible with standard rectifiers and is limited to the transformer arrangement or something very similar. The CCC SRM converter on the other hand can be interfaced to any rectifier that provides a controlled dc link voltage and that supports bidirectional power flow through reversal of current direction.

- The CCC converter can force a negative current from the beginning of the stroke in the SRM, whereas the CAB converter cannot. However, this is not a requirement for the SRM as it only requires unipolar current.

- Due to the high number of secondary windings in the CAB converter system transformer, it tends to be more complex to manufacture and perhaps even more complex to maintain.

- Current in the dc link of the CCC SRM converter reverses direction. This limits the choices of the front-end converters to those that can accept bidirectional current, and eliminates choices like diode

bridge rectifier front-end converters. However this is seldom an issue in high-power systems where cost is not the most important factor and so bidirectional rectifiers using active switches or the MMC can be used.

6.7.16 Summary of comparison

A summary of the comparison is provided in Table 6.2. It may be seen that most of the advantages of the CAB converter system relate to the device count (and hence kVA capacity) and consequently cost. However, unless prohibitive, cost is not of high priority for multi-megawatt applications or critical sub-megawatt applications. At such applications device oversizing is more likely anyway. That cost advantage may come into play in high-performance sub-megawatt applications that could benefit from the multilevel capability of this converter. However, at this power level the fact that MMC + CCC converter system does not require a transformer whereas the CAB system does takes away the cost advantage – except if an isolation transformer is required by the application or due to regulation.

On the other hand, the MMC + CCC converter is easier to scale and has better fault tolerance due to the independence of the front-end and motor-end. These criteria weigh heavily in multi-megawatt applications or critical sub-megawatt applications.

TABLE 6.2
CONDUCTION AND SWITCHING LOSS DATA FOR DIFFERENT SRM CONVERTER ARRANGEMENTS

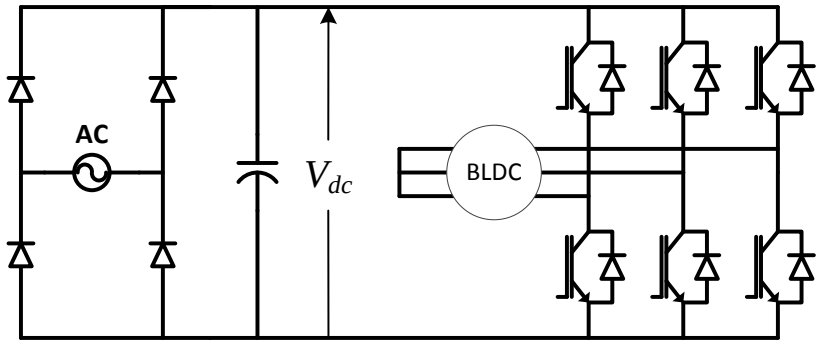
Criteria	MMC + 4-cell CCC converter system	2-cell CAB converter system	Remarks
Motor-end device count per phase leg	8 IGBTs with antiparallel diode	4 IGBTs + 4 diodes	CAB ✓
Motor-end device blocking voltage	$V_{dc}/2$	$V_{dc}/2$	equal
Motor-end device current ratings	Max. IGBT current ~ 67% of phase current, unequal current distribution	Max. IGBT current 80%, but more uniform device current distribution	CAB ✓
Front-end device count per phase leg	8 IGBTs with antiparallel diode	12 IGBTs with antiparallel diode	CCC ✓
Front-end device blocking voltage	$V_{dc}/2$	$V_{dc}/2$	equal
Front-end device current ratings	similar	similar, but more uniform device current distribution	CAB ✓
Installed kVA Capacity	200%	100% or 150%	CAB ✓
Total capacitor count	12 front-end + 12 motor-end	6	CAB ✓
Transformer requirement	Only if required for isolation	required in all cases	CCC ✓
Motor-end efficiency	same	same	equal
Front-end efficiency	similar	similar	equal
Control complexity	similar	similar	equal
Redundancy	motor and front ends independent	motor and front ends connected	CCC ✓
Input power quality	excellent	excellent	equal
Scalability	easy	Number of transformer secondary connections increase complexity	CCC ✓
Gate drive requirements	same	same	equal
Heat sink requirements	similar	similar	equal

Chapter 7

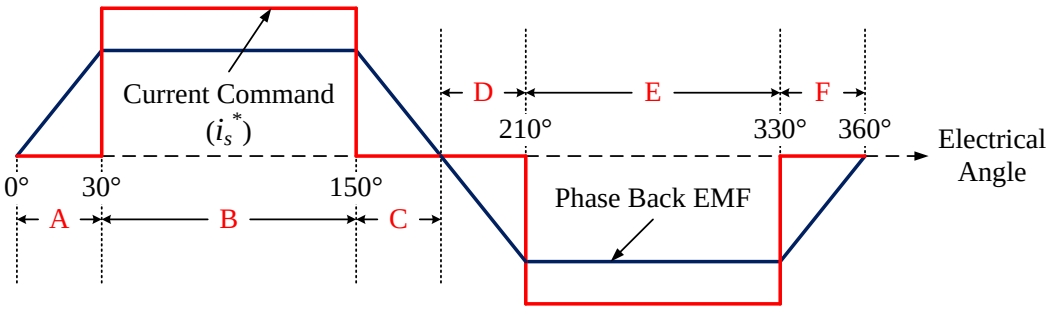
Control Methods for a Brushless DC Motor Drive with a New Converter Topology

7.1 Introduction

Permanent-magnet brushless motor drives are utilized in a wide variety of applications. Their applications include electric and hybrid vehicles, fans in HVAC and refrigeration, machine tool drives, motion control and actuation systems in manufacturing, and more. Their attractive features include light weight, small size, simplicity of control, high efficiency, lack of maintenance, and low acoustic noise. Permanent magnet brushless dc motors with a trapezoidal back electromotive force (EMF) profile are commonly known as BLDCMs for short, while those with a sinusoidal back EMF profile are known as PMSMs (for permanent-magnet synchronous motors).



(a)



(b)

Fig. 7.1 (a) Conventional BLDCM Drive (b) Typical BLDCM Waveforms

BLDCMs also have a greater power density than PMSMs [6], and have simpler position sensing requirements that are much less expensive than those required by PMSMs. Also BLDCM control is simpler than that of PMSM, can be implemented with analog electronics as opposed to a digital controller. However, torque ripple is much higher in BLDCMs compared to PMSMs, and so BLDCMs tend to be the favored choice in applications with lower performance requirements.

The standard configuration of a 3-ph BLDCM drive is shown in Fig. 7.1 (a). The back EMF profile for one phase is shown in Fig. 7.1 (b). The total electromagnetic torque of the machine, T_e, is related to the phase back EMFs e_a, e_b, and e_c, and phase currents i_a, i_b, and i_c, according to (7.1), where ω_r is the angular velocity of the rotor.

$$T_e = (e_a i_a + e_a i_a + e_a i_a)/\omega_r \tag{7.1}$$

Thus for a given motor speed, torque is maximized by producing phase currents that track the shape of their respective phase back EMF waveforms as closely as possible. One of the most commonly used excitation schemes is the 120 degree square wave excitation, illustrated in Fig. 7.1 (b) and explained below.

In the 120 degree square wave excitation, the current magnitude to produce the commanded torque or speed is computed by a controller and commanded for the complete flat portion of the back EMF waveform, i.e., where back EMF is maximum. Zero current is commanded in the sloping regions of the back EMF. BLDCM drives using this excitation scheme and other schemes have been successfully used in many applications. However, the speed of the machine is limited by its dc bus voltage, which is usually a standard value for a given application. Designing the machine with a smaller back EMF to allow for a higher speed rating will result in reduced torque and hence reduced power capabilities. This is undesired in applications requiring high startup torque or high rated torque. Using higher currents may compensate for that (at low speeds only), but that requires higher rated switches and may reduce efficiency.

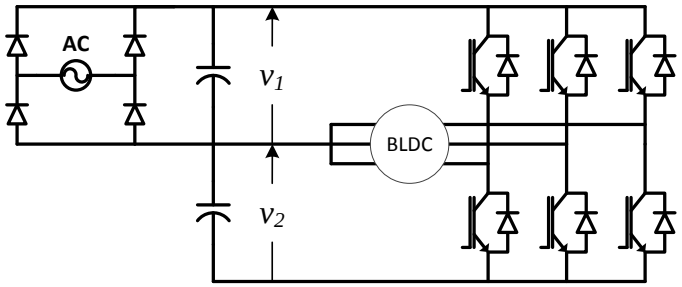
For applications such as in traction, which require low torque at high speeds, operation at speeds above rated has been typically achieved through current phase advancing [52]-[55]. In this method, each phase is excited before the phase back EMF reaches its peak, and sometimes even while it is still negative. This allows enough current to develop before the back EMF rises above the dc link voltage. However, several limitations to this method exist. First, BLDCs with rare earth magnets are known for their low inductance, and hence very large currents tend to develop when the net voltage applied to the winding is high [55]. This requires additional cooling and/or an increase in the semiconductor ratings. Second, exact control of speed or torque becomes difficult since current is usually uncontrolled in that mode. Third, for large advance angles, the bypass diodes are likely to conduct for a short period of time just before the phase

commutates. During that time the phase current and phase back EMF will have opposite signs, thus resulting in a negative torque contribution from that phase. This reduces the efficiency of the motor. Alternate topologies with twice the number of switches have been suggested to mitigate some of the issues mentioned above [56]-[57]. However, the additional components increase the converter cost and decrease its reliability due to increased device count.

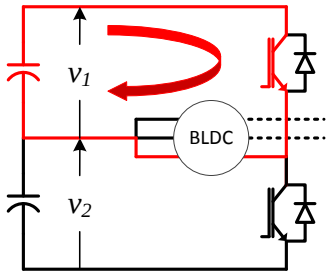
7.1.1 Alternate Converter Topology

A new converter topology [8], requiring an additional capacitor or a battery and the neutral connection, is considered for study in this work. Fig. 7.2 (a) depicts this topology, with a capacitor used for the additional source. Let v_1 and v_2 be the voltages across the upper and lower capacitors, respectively, as labeled in Fig. 7.2 (a). Assuming v_1 and v_2 are constant, several advantages are noted about this topology:

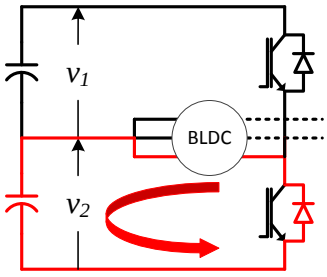
1. Voltage available for excitation is increased from v_1 to v_1+v_2. This can be used to operate the drive at higher speeds without phase advancing, or operate the drive at only half the dc link voltage.
2. If chosen as battery, the additional source may be potentially used to temporarily drive the motor in case of ac power loss. This is useful in electric vehicle applications and other critical applications.
3. Since each phase leg controls only one phase of the motor, if a fault occurs in one phase and it is excluded, the drive may be potentially operated with two phases.



(a)



(b)



(c)

Fig. 7.2 (a) Considered BLDCM drive, (b) Phase energization during positive half-cycle of current, (c) Freewheeling during positive half-cycle of current

This work focuses on exploring the operation of the drive in light of the first listed advantage. Potential fault tolerant operation mentioned in advantages 2 and 3 are left for future research and verification.

7.1.2 Principle of Operation of Considered Converter

Consider the converter in Fig. 7.2 (a), and consider the commanded current waveform, i_s^*, shown in Fig. 7.1 (b). For a given phase, positive half-cycle current is provided by turning on the upper switch in the phase leg to energize the phase through the upper capacitor, as illustrated in Fig. 7.2 (b). To control the current, the upper switch is turned off, thereby allowing current to freewheel through the bypass diode of the lower switch, as illustrated in Fig. 7.2 (c), but also charging the lower capacitor. The opposite takes place in the negative half-cycle; the lower switch is used to energize the phase through the lower capacitor, while current is controlled by freewheeling through the upper bypass diode. Thus, energy is lost from the lower capacitor in the negative half-cycle, partially to generate torque, and then for partial return of its stored energy to the source.

If the voltage of the lower capacitor is not actively controlled, its level cannot be maintained, and so advantage 1 listed above cannot be capitalized on. The main objectives of this work are to propose a control strategy for the considered converter, verify it through simulation, and compare the drive's performance to that of a conventional BLDCM drive [59]. In section 7.2, a control strategy with three variations is proposed for controlling v_2. In section 7.3, simulation results using the proposed control strategy are presented for the case $v_1=v_2=V_{dc}$, where V_{dc} is the nominal dc link voltage of a conventional BLDCM drive using the same motor and delivering equal power. Simulation results for a conventional BLDCM drive are also given for comparison. In section 7.4, high speed operation of the considered drive with exact control of torque at a given speed is demonstrated through simulation. In section 7.5 it is shown that the drive may be operated at rated torque and speed with only half the dc link voltage. Some notes about initial charging of the lower capacitor are provided in section 7.6. Conclusions and suggestions for further work are provided in section 7.7.

7.2 Proposed Control Strategy

To maintain v_2 at a desired level, it is proposed that an asymmetry in the form of positive dc shift be introduced in the phase currents [59]. The idea is to increase the magnitude of the positive half-cycle current until free-wheeling energy during the positive half-cycle is just enough to charge the lower capacitor to the desired level, while maintaining desired speed or torque. Fig. 7.3 shows how such strategy may be implemented.

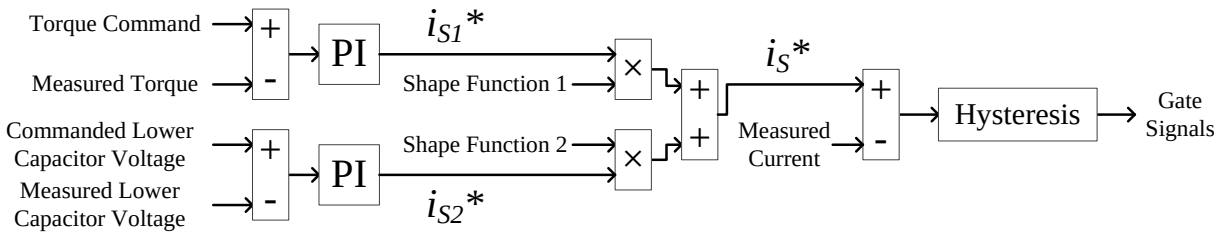


Fig. 7.3 Proposed control strategy for the considered BLDCM drive

Let the output of the usual speed or torque controller be called i_{s1}^*. This component is responsible for maintaining the commanded torque or speed. Another faster controller is used to compute a second reference, i_{s2}^*, based on the error between v_2 and its desired level. This represents the dc current component required to maintain v_2 at the desired level. i_{s1}^* and i_{s2}^* are then used to make up the total phase current command, i_s^*. Three methods of forming i_s^* from i_{s1}^* and i_{s2}^* are presented in this work; they are explained in the following.

Method 1

i_{s2}^* is added to i_{s1}^* only during the interval labeled B in Fig. 7.2 (b). Current during interval E is still $-i_{s1}^*$, and current during intervals A, C, D, and F is still zero. Note that i_{s1}^* in this case would be smaller than it would be in a standard BLDCM converter with the same output power.

Method 2

Phase currents are controlled to i_{s2}^* during the intervals labeled A and C in Fig. 7.2 (b). Current during intervals B and E is still i_{s1}^* and $-i_{s1}^*$, respectively, and current during intervals D and F is still zero. i_{s2}^* in this method is typically larger than i_{s2}^* in method 1, since it spans only 60° (30°+30°), whereas i_{s2}^* in method 1 spans 120°.

Method 3

Phase currents are controlled to i_{s2}^* during intervals A and C. However, i_{s2}^* is also added to i_{s1}^* during the interval B. Current during interval E is still $-i_{s1}^*$, and is still zero during intervals D and F. i_{s2}^* in this method is smaller than i_{s2}^* in methods 1 and 2, since it has a larger span of 180° (30° + 120° + 30°).

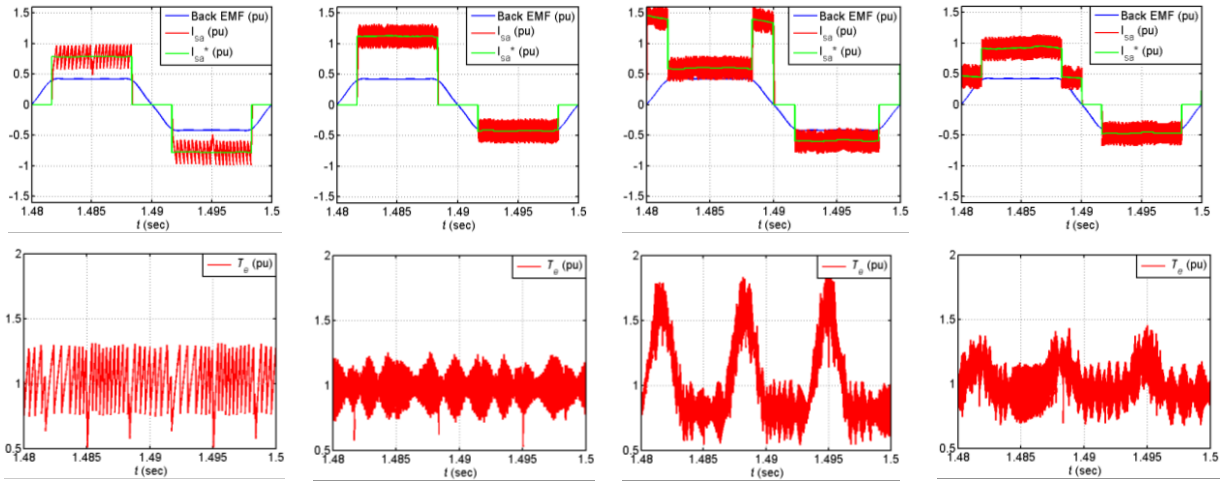
7.3 Simulation Results

A simulation model using Simulink and the PLECs blockset is developed to evaluate the performance of the proposed control strategy. The BLDCM used in simulation is a modification of a model provided by PLECs. It is 3-phase with 2 rotor poles, rated 942 W @ 3000 r/min, 300V. Motor back EMF is modeled as a sum of a fundamental component and the 3rd, 5th, 7th, 9th, and 11th harmonics. Mutual inductance between stator phases, M, is assumed constant. Stator winding inductance, $L_s - M$, is 2.84 mH,

and stator winding resistance, R_s, is 0.388 Ω. Capacitors are assumed initially charged. Notes on the initial charging of the lower capacitor are provided in section 7.7. The dc link capacitor in both converters is 1000 uF, which was found to keep capacitor voltage ripple below 10% pk-pk at rated speed and torque. The lower capacitor is only 100 uF, and that gave less than 6% pk-pk ripple at rated speed and torque. A thermal model is also incorporated in the simulation to better evaluate conduction and switching losses. The torque controller sampling rate is 1 kHz, while the sampling rate for the controller for voltage v_2 is 10 kHz. The hysteresis band for the phase current controllers is 2 A. In this first set of simulations, v_1 is set to V_{dc}, and v_2 is controlled to V_{dc}. Drive operation is simulated for rated speed and torque. Results are summarized in Table 7.1 and plots given in Fig. 7.4.

TABLE 7.1
COMPARISON OF CONVENTIONAL BLDCM DRIVE WITH STUDIED DRIVE IN ALL 3 CONTROL METHODS

	$I_{s\text{-}rms}$ (A)	$T_e/I_{s\text{-}rms}$ (Nm/A)	T_e/P_{cu} (Nm/W)	Av. IGBT Currents (A)		Capacitor Currents (A)		Conduction Losses (% of P_{out})		Switching Losses (% of P_{out})		Efficiency (%)
				Top	*Bottom*	*Top*	*Bottom*	*IGBTs*	*Diodes*	*IGBTs*	*Diodes*	
Conventional Drive	3.11	0.966	0.264	1.18	1.18	9.01	N/A	0.90	0.08	0.24	0.03	96.70
Studied Drive (Control Method 1)	3.39	0.885	0.219	1.33	0.49	9.10	2.63	1.12	0.19	5.31	0.18	91.54
Studied Drive (Control Method 2)	3.67	0.819	0.188	1.41	0.68	9.40	3.26	1.15	0.28	6.74	0.32	89.68
Studied Drive (Control Method 3)	3.16	0.951	0.258	1.34	0.55	9.11	2.55	1.06	0.22	6.21	0.22	90.38



(a) (b) (c) (d)

Fig. 7.4 Waveforms for steady state operation at rated speed (3000 r/min) and rated torque (~3 Nm)

(a) Conventional BLDCM drive; (b) Studied drive - Method 1; (c) Studied drive - Method 2; (d) Studied drive - Method 3

$I_{s\text{-}rms}$ is the rms stator current for one phase. P_{cu} is the total copper losses per unit rms current for all 3 phases. The efficiency calculation includes resistive, inverter, and some parasitic losses such as capacitor ESRs. However, frictional and core losses are not calculated and hence are not included in the efficiency calculation. Note that the back EMF in the plots is the per-phase back EMF. Base value for per-unit (p.u.) back EMF in the plots is peak ac supply voltage, and for p.u. currents it is 5 A.

Simulations results show that the main objective of this work, which is to provide a working control strategy for the drive with the studied converter, has been achieved. The studied drive using control method 3 and the conventional drive had the best overall performance, with the conventional drive having the edge in efficiency. This is contributed to its lower switching frequency, owing to the fact that the conventional drive uses half the voltage per phase that the studied drive uses. Method 1 had slightly lower performance ratios than method 3, since unlike method 3 it does not utilize sloping regions of the back emf for torque production. However, since the current in method 3 spans 30° more per cycle, it tends to have higher losses and hence has lower efficiency than method 1. Method 2 had the lowest performance, as a large portion of the current is applied during the sloping back EMF regions, in which torque generation is least productive.

Considering method 3 only, it is seen that the current requirement of the top three switches is close to that of the conventional drive, and that the lower three switches need only half the current capacity. Therefore it can be said that the extra cost of the new converter lies only in doubling the switch voltage ratings, and in the additional capacitor that is only a tenth of the dc link capacitor size. Stator winding design must accommodate twice the voltage per phase (only in terms of wire insulation), and requires a slightly increased core saturation capability since peak current in the new converter using method 3 was about 0.78A higher than the peak current in the standard converter.

7.4 High-Speed Operation with New Converter

For this set of simulations, both v_1 and v_2 are still at V_{dc}. However, the drive is simulated at twice the rated speed but with reduced torque, typical of traction applications. Torque is controlled to half the rated value to maintain rated power and to demonstrate that the drive allows exact control of torque at speeds above rated. Simulation results for methods 1 and 3 are given in Table 7.2, and corresponding plots are given in Fig. 7.5. The hysteresis band was reduced from 2 A to 1 A to avoid phase current going negative at some instances during the negative half-cycle, which is slightly noticed in in Fig. 7.5(a). This may result in slight negative torque contribution from the phase – though the overall developed torque will be positive due to larger overlapping torque contributions from other phases.

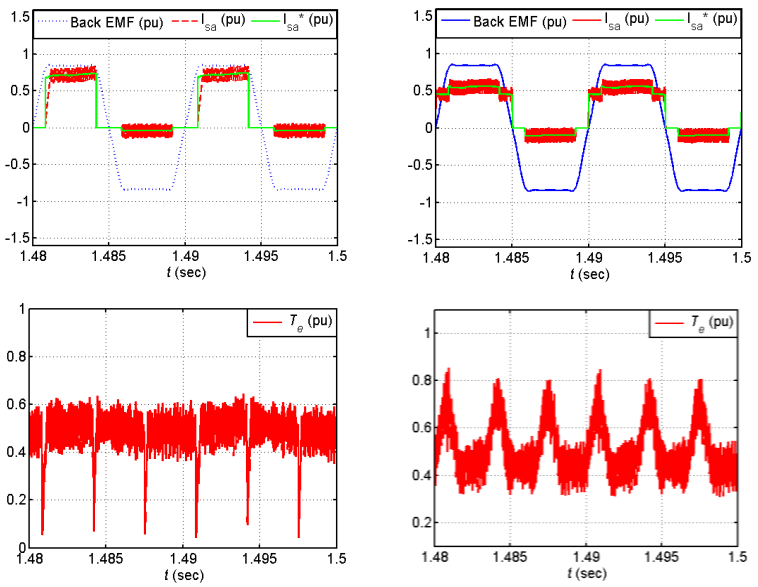


Fig. 7.5 Studied drive at twice rated speed (6000 r/min) and half rated torque: (a) Control method 1; (b) Control method 3

TABLE 7.2
COMPARISON OF CONTROL METHODS 1 AND 3 OF STUDIED DRIVE AT TWICE RATED SPEED (6000 R/MIN) AND HALF RATED TORQUE

	$I_{s\text{-}rms}$ (A)	$T_e/I_{s\text{-}rms}$ (Nm/A)	T_e/P_{cu} (Nm/W)	Av. IGBT Currents (A)		Capacitor Currents (A)		Conduction Losses (% of P_{out})		Switching Losses (% of P_{out})		Efficiency (%)
				Top	*Bottom*	*Top*	*Bottom*	*IGBTs*	*Diodes*	*IGBTs*	*Diodes*	
Studied Drive (Control Method 1)	2.12	0.708	0.291	1.15	0.08	8.83	0.89	0.87	0.00	1.53	0.00	96.26
Studied Drive (Control Method 3)	1.84	0.816	0.374	1.12	0.15	8.54	1.06	0.79	0.01	3.29	0.00	95.03

Results show that the considered converter with the proposed control strategy presents a strong alternative to other methods of achieving high-speed operation, such as current phase advancing in conventional BLDCM drives [2]-[5], or modified topologies that use as many as twice the number of switches [6]-[7].

7.5 Operation with Half DC Link Voltage

In this set of simulations, v_1 and v_2 are both at $0.5V_{dc}$. Note that this results in the same voltage per phase as with the conventional drive. Simulation results for methods 1 and 3 are given in Table 7.3, and corresponding plots in Fig. 7.6. A smaller hysteresis band of 1 A was again used to avoid or minimize negative current and hence negative torque components in the negative half-cycle of the current.

TABLE 7.3

COMPARISON OF CONTROL METHODS 1 AND 3 OF STUDIED DRIVE OPERATING WITH HALF THE DC LINK VOLTAGE ($v_1 = v_2 = 0.5V_{DC}$)

	$I_{s\text{-}rms}$ (A)	$T_e/I_{s\text{-}rms}$ (Nm/A)	T_e/P_{cu} (Nm/W)	Av. IGBT Currents (A)		Capacitor Currents (A)		Conduction Losses (% of P_{out})		Switching Losses (% of P_{out})		Efficiency (%)
				Top	*Bottom*	*Top*	*Bottom*	*IGBTs*	*Diodes*	*IGBTs*	*Diodes*	
Studied Drive (Control Method 1)	4.13	0.726	0.153	2.17	0.12	15.93	1.62	2.00	0.01	0.74	0.00	92.89
Studied Drive (Control Method 3)	3.68	0.816	0.192	2.27	0.29	15.78	1.96	1.87	0.02	1.56	0.01	92.70

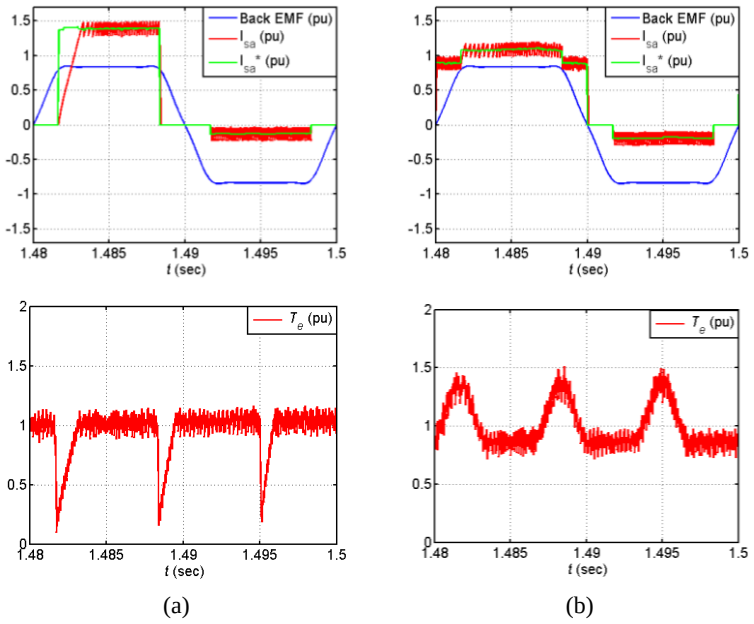


Fig. 7.6 Studied drive with $v_1=v_2=0.5V_{dc}$: (a) Control method 1; (b) Control method 3

It is also important to note that the size of the capacitors was increased in order to improve stability. 5100 uF was used for the upper capacitor, and 3000 uF for the lower. Stability analysis for this drive is another topic that is worthy of exploration, but is beyond the scope of this work, as the focus here is on proof of concept. The studied drive with $v_1=v_2=V_{dc}$ is fairly stable, and that is the main intended mode of operation for this drive. Nevertheless stability analysis is for this drive is strongly suggested as future work.

From Table 7.3, it is noted that a larger rms current is required to produce the same power than required by the full dc link voltage case, as seen in Table 7.1. This results in lower performance ratios of torque per unit rms current and torque per unit copper loss, given respectively as $T_e/I_{s\text{-}rms}$ and T_e/P_{cu}. But since the excitation voltage is lower, the switching frequency is also lower, leading to a slightly higher efficiency – although use of a smaller hysteresis band again increased the switching frequency. Note also that devices in this mode will have the same voltage rating as in a conventional BLDCM drive, i.e., only V_{dc}, whereas the devices in the case where $v_1=v_2=V_{dc}$ have a rating of $2V_{dc}$.

7.6 Charging Lower Capacitor on Startup

As earlier explained, the lower capacitor is charged from the freewheeling energy during the positive-half cycle of any phase current. Therefore, the lower capacitor may be initially charged by sending short current pulses to one or more phases until the desired voltage level is reached. Enough time should be given between pulses to ensure the excited phases are completely de-energized after every pulse, to avoid build-up of current in the windings leading to their saturation.

7.7 Conclusion and Future Work

In this chapter, a control strategy with three variations for a BLDCM drive with a new converter topology is proposed. The new topology is based on a conventional voltage-fed inverter plus an additional source like a capacitor or battery, and requires access to the neutral of the BLDCM. Contributions and findings are summarized below:

- Performance of the studied drive using the proposed control strategy was verified through detailed simulations
- Performance of the studied drive using the suggested control strategy (in its three variations) was compared in simulation to a conventional BLDCM drive using the same motor and operating with the same dc link voltage, and delivering equal power
- Results show that the studied drive using control method 3 had almost equal performance ratios of torque per unit rms current and torque per unit copper loss as the conventional BLDCM drive, but had a slightly lower efficiency
- The studied drive with the proposed control strategy has other advantages, such as:
    - Ability to provide exact control of torque and speed at up to twice rated speed without resorting to current phase advancing or other flux-weakening techniques
    - Ability to deliver rated power at only half the dc link voltage with $v_1=v_2=0.5V_{dc}$, if needed for some applications. If the additional source is a capacitor, it was found that large capacitors were required to improve stability. Stability analysis could help define clear stability margins for the capacitor values and controller parameters. But since the main intended mode of operation of this is drive is $v_1=v_2=V_{dc}$, which is quite stable with lower capacitor values, stability analysis is not pursued further in this work. However, stability analysis is strongly suggested as future work.

- The studied drive potentially has some fault-tolerant operation modes due to its inherent independent phase operation. The drive may be operated with only two phases if a phase fails and is excluded, and also it may operate temporarily with only the additional source in case of loss of ac power. However, this fault-tolerant potential is not studied in this work, and is suggested as future work.

- Simulations showed that if the additional source is a capacitor, it could be as small as one tenth the size of the dc link capacitor, and must handle only about a third of the current handled by the dc link capacitor.

- While all switches require twice the voltage rating when compared to the conventional drive switches, and while the upper switches required roughly the same current capability as with the conventional converter's switches, the lower switches in the studied drive required only about half the current capability.

Therefore, given its multiple uses and benefits, the studied drive with the proposed control strategy is quite versatile and can prove useful in many areas of application. Future work includes studying the effect of the proposed control methods on core losses to get a more complete picture of the losses, establishing criteria for sizing the additional capacitor (via analytical modeling and assessing stability limits), exploring fault-tolerant operation, and experimental validation of the proposed control methods.

Finally, an important point to mention is that while the simulations given in this chapter were based on a machine designed for a standard BLDCM converter, for the new converter with the proposed control the machine design could be altered to further enhance the efficiency and other performance figures. For example, while keeping the air gap power of the machine the same, the number of turns as well as the conductor area could be adjusted to increase the back EMF and thus reduce switching losses. The drawback of such approach is the speed of the drive with the new converter is then lowered due to the increase in emf.

Chapter 8

Conclusion and Future Work

In this work, a novel multilevel converter for switched reluctance motor drives that is scalable to high voltage levels has been proposed. The proposed converter is called the chopper cell (CCC) converter. The converter is naturally capable of variable speed, four-quadrant operation. The CCC converter has a modular construction and offers high reliability; it also has provision for including redundant modules. The CCC converter mainly targets high speed multi-megawatt that typically operate at the medium voltage level which extends from 1 kV all the way up to 30 or 35 kV. Examples pf potential applications are very high power pumps and compressors in the oil and gas industry. However, due to its multilevel capability and use of low voltage cells, the CCC converter also offers high efficiency and improved performance. Therefore, the proposed converter may also find use in sub-megawatt SRM drive applications that require high efficiency and or high performance. And by virtue of its reliability, the converter may also be used in critical sub-megawatt SRM drive applications that require very high uptime.

Several control algorithms have also been proposed for the CCC converter. Most important is the novel cell capacitor voltage balancing and control, without which the drive cannot operate. A startup algorithm that limits startup current and switching losses, and that ensure cell capacitor voltages remain controlled at startup, has also been proposed. Finally, a complete scheme that operates the CCC SRM converter drive at a high efficiency is also proposed.

A detailed simulation model was developed and used to validate the converter's operation and all of the above-mentioned control techniques. The suggested algorithms act on all the control variables in the drive, those being the energization voltage level, as well as the turn-on and turn-off angles, and finally the current. Practical considerations related to the drive such as reliability, efficiency, and cost considerations are also discussed. Also a detailed comparison of the CCC converter with another multilevel SRM converter is performed.

Finally, a small part of this work is also dedicated to brushless dc machines (BLDCMs). A control strategy with three variations for a BLDCM drive with a new converter topology has been proposed and verified via simulation. The new topology is based on a conventional voltage-fed inverter plus an additional source like a capacitor or battery, and requires access to the neutral of the BLDCM. One of the most important advantages of the new converter with the proposed control methods is the ability to achieve exact

control of torque and speed at up to twice rated speed without resorting to current phase advancing or other flux-weakening techniques.

The contributions from this research are thus summarized below:

- Development of a novel converter topology for medium-voltage variable-speed SRM drives that satisfies the requirements of this category, most significantly easy scalability and high reliability.
- Development of a complete control scheme for the proposed drive, with the cell capacitor voltage balancing and control being novel.
- Development of a startup algorithm, not requiring any extra devices, that allows the proposed drive to go through the startup phase without a large increase in the cell capacitor voltages, which avoids oversizing the capacitors. The startup algorithm also limits the switching losses, which makes the startup process thermally safe.
- Verification of all of the above through simulations via a detailed switching-based model.
- Development of an algorithm for operating the drive in an efficient single-pulse mode throughout the speed range.
- Suggested simulation approach for the evaluation of various losses in the above single-pulse mode throughout the speed range.
- Development of control methods for a new converter for BLDCM drives, and their verification via simulation.

Besides the suggested future in chapter 7 on the BLDCM drive, following are suggested future works related to the CCC SRM converter part:

- Experimental validation on a down-scaled laboratory prototype
- Explore the possibility of altering startup algorithm, or proposing a new one, that further minimizes the capacitance requirement of the cell capacitors
- Further investigation of the complete system including the ac MMC front-end converter and the motor-end CCC SRM converter, with and without dc link capacitance.

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