Design and Control of Charge-Pumped Reboost Converter for PV Applications

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Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical and Computer Engineering

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April 29, 2010
Blacksburg, Virginia

Keywords: DC-DC Converter, PV

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ABSTRACT

Photovoltaic (PV) systems are renewable, DC sources which provide non-linear output power with respect to PV panel operating voltage or current. The majority of PV sources yield poor conversion efficiencies between available solar radiation and electrical output. Additionally, they are expensive compared to other conventional power sources. Power electronic converters are capable of harvesting the most energy from these resources due to their configurability and high-efficiency. These converters form a power conditioning stage which allows for numerous control methods and energy management options.

Traditional systems group PV sources into arrays in order to increase operating voltage and power to levels where it is practical to connect them to the utility grid. Grid-tied PV has the potential to increase the acceptance of PV energy by reducing end-user complexity – there are no batteries to manage and additional wiring can be kept to a minimum. However, these arrays of PV panels have significant drawbacks when they are subjected to non-ideal conditions. If a single panel is shaded, or covered in some way, then it will have greatly reduced output current. As a result, any other panel which is connected in series with the affected panel is also subject to the same output current reduction. This series grouping of panels may then indirectly affect other series-sets of panels which are connected in parallel to it by tricking the power electronics unit into operating at a point which is not the true maximum-power-point (MPP).

By connecting a single PV panel to a single DC-DC converter, these array-effects can be avoided. Reliability and power output of the whole system should increase at the expense of additional hardware. The outputs of several PV-connected DC-DC converters can be connected either in series or in parallel. If they are connected in parallel, the converters must be able to boost the PV panel voltage up to a level greater than the desired utility-grid voltage.

This thesis focuses on the design and control of a high-boost-ratio DC-DC converter suitable for use in a parallel-connected, grid-tied PV system. It demonstrates the feasibility of boost-ratios of up to 10 times while still achieving high efficiency. The design avoids the use of electrolytic capacitors in favor of smaller ceramic capacitors and a few large film-capacitors. A simplified model is proposed which is still suitable for use in the design of high-bandwidth control loops. Testing is done with a PV source showing preliminary results with a maximum-power-point-tracker (MPPT) which achieves very good steady-state performance.

Dedication

I would like to dedicate this thesis to my family – their love and support is the motivation for everything that I do.

I would like to thank my advisor, Dr. Jih-Sheng Lai, for giving me this opportunity to work on such a practical and fun research project. I would also like to thank Dr. Wensong Yu for teaching me how to think about power electronics and for giving me the chance to work with him and learn from him. I also thank all of my fellow co-workers and friends for showing me all of the little things that one cannot learn from a textbook.

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1 Introduction

Photovoltaic (PV) power is an emerging technology strictly because power electronics are allowing it to be used in practical ways. With PV panel prices dropping and the desire to 'go green' increasing, demand for PV power is improving. Most traditional PV installations are stand-alone systems relying on large battery banks to supply power when the sun goes down. Modern PV systems eliminate the battery banks in favor of utility-grid connections, where the energy from the PV panels is pushed back onto the grid to offset energy produced at the power plant.

Arrangements of the PV panels in these grid-connected or grid-tied configurations vary widely. Some commercial inverters, such as those produced by Siemens, Xantrex, SMA – famous for the Sunny Boy inverter – and Solectria use large arrays of PV panels to generate high enough voltages to be able to send power to the utility grid with a single conversion stage (Figure 1). Single-phase grid-tied inverters frequently use large decoupling capacitors to smooth the energy flow between the dc PV array and the ac utility-grid. These capacitors are typically large, expensive, electrolytic capacitors which have a short lifespan compared to other capacitor compositions such as film or ceramic.

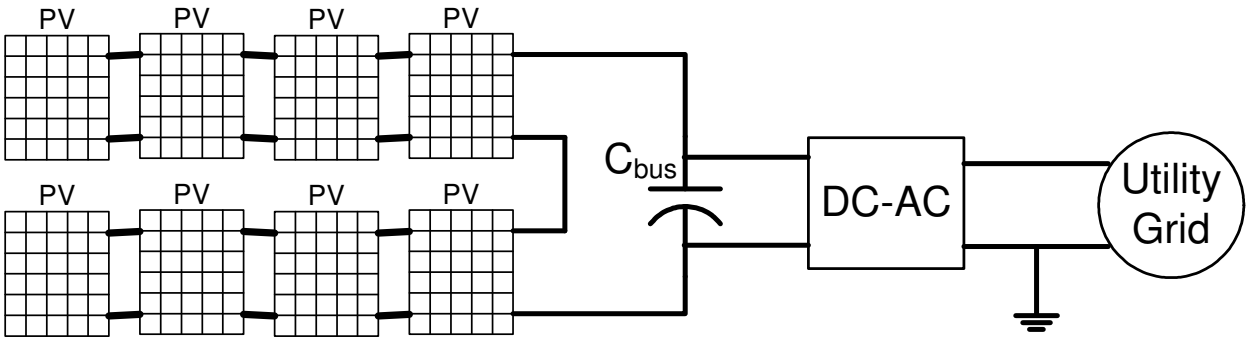


Figure 1. Conventional Grid-Tied System

Increasingly, companies are changing to distributed inverters, or micro-inverters (Figure 2), which have PV panels and inverters at a 1:1 ratio [1]. The hope is that by making the systems modular, they can be made more productive and reliable. PV panels have a dc current output which is proportional to the amount of solar radiation received by the solar cells of the panel. If there is less sunlight, there is less current. The problems arise when these cells are connected to form panels, and the panels are connected to form arrays. If one cell in the panel sees less light due to shading or some obscuration, it can drastically reduce the current output of the panel – subsequently, if the current output of one panel is reduced, the current output of the whole array can be significantly lower. By separating the panels with microinverters, the localized conditions of one panel no longer affect the rest of the system.

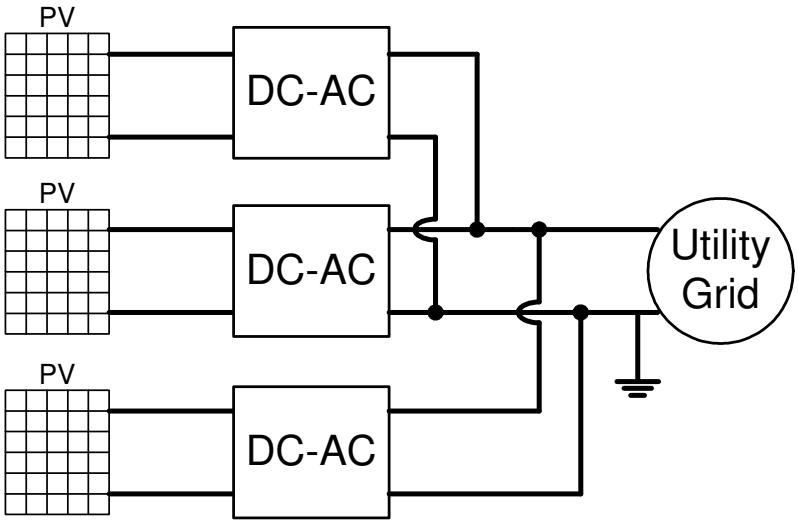


Figure 2. Microinverter Grid-Tied System

Many companies have begun to develop or manufacture micro-inverter systems –Direct Grid, EnPhase Energy, Exeltech, Petra Solar, and SolarBridge are but a few.

Enphase uses an active clamp flyback to create a rectified single-phase current waveform, which is then connected to the utility grid through a polarity-selection stage made up of thyristors [2]. Since there is a single PWM stage, there is low-frequency current ripple which must be passively decoupled – the EnPhase microinverter accomplishes this by using 5, 1.8 mF electrolytic capacitors in parallel at the low-voltage input. These electrolytic capacitors have a low maximum temperature rating and can fail over time from evaporation or leakage of the liquid electrolyte. Measured peak efficiency of the EnPhase microinverter at 25 V_{dc}, 240 V_{ac} is 94.7% at 150W.

If a two-stage microinverter is adopted like in (Figure 3), then the low-frequency ripple can be decoupled between the dc-dc and dc-ac stages. This can eliminate the need for electrolytic capacitors by replacing them with higher-voltage rated film capacitors.

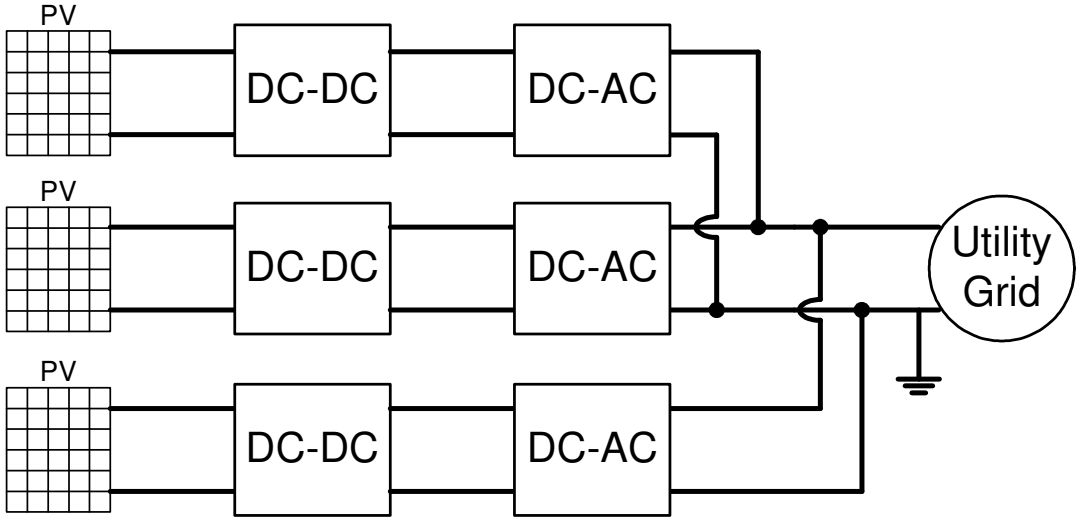


Figure 3. Two-Stage Grid-Tied System

Exeltech uses a two-stage system to do grid-tied PV [3]. The peak quoted efficiency for the Exeltech ac-module is 93.5% [4]. They probably use a high-boost ratio dc-dc stage like the boost-converter or full-bridge converter with a buck-type dc-ac stage. By using a more advanced boost topology, they should be able to improve the overall efficiency.

Solarbridge, formerly Smartspark, uses a H-bridge to act as an ac-ripple port to do active power filtering for a push-pull PV inverter [5]. This allows very high ripple across the capacitor of the active-filter so that electrolytic capacitors can be eliminated from the system. The ac-ripple port requires bi-direction switches – switches that can block in either direction – at high frequency. With modern devices this requires back-to-back IGBT's or MOSFET's. The downside of this is in control of the switches and conduction losses. Typically, an isolated gate drive is required to operate the back-to-back switches. Current flowing through the ac-ripple port goes through 4 switches at a minimum, and once the push-pull stage switches are included, the current is flowing through 5 switches. Additionally, the conduction losses of the thyristor are larger than for a similar mosfet at low power levels. By using a simple two-stage design, the conduction losses can be reduced while still achieving good ripple-rejection at the output of the PV panel.

This thesis proposes that the charge-pumped reboost converter can yield superior efficiency in a two-stage, grid-tied PV inverter compared to state-of-the-art systems while simultaneously eliminating the need for electrolytic capacitors. This thesis will cover the basic design methodology for components of the dc-dc stage and will show steady-state efficiency testing. This thesis will describe the need for an approximate model in order to develop control loops and will then propose a suitable approximate model. Closed-loop testing of the dc-dc stage will be shown with fast transient responses to step-voltage changes of a thevenin source, MPPT tracking with real PV panels, and simulated shading transients with PV panels.

1.1 Topology Review

This topology review will be punctuated by design examples showing the merits and disadvantages of each topology. The nominal specifications are:

Input Voltage	20 V_{dc} to Max Achievable
Output Voltage	200 V_{dc}
Output Power	200 W
Acceptable Duty Cycle	10 to 90%
Maximum Peak Voltage Rating of any Component	600 V

Table 1

1.12 Boost Topology

The standard boost topology (Figure 4) is usually very good for boost ratios of less than 5. In practical applications, the series resistance of the inductor – along with finite switching times of the active devices – act to limit the maximum achievable boost ratio. This topology should have very low input-current ripple since the inductor guarantees continuous input current. In the real system, there will be an input capacitor

which would further smooth the source-current ripple when used with a higher-impedance source like PV.

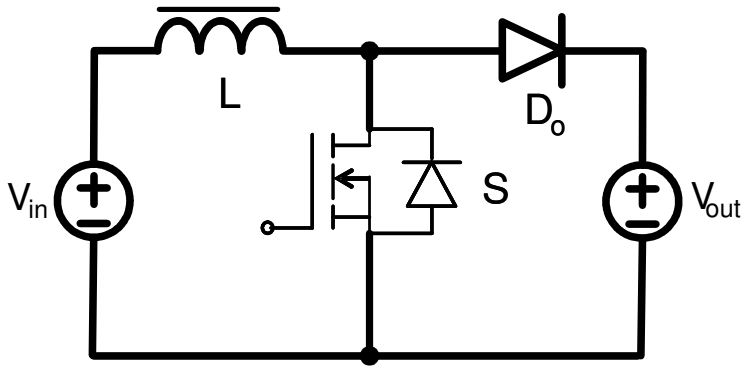


Figure 4. Boost Topology

Of major importance is the extreme duty cycle which is required for high conversion ratios. For the specifications given in Table 1, a conversion ratio of 10 is required for the boost converter. A duty cycle of 90% is calculated according to Eqn. 3.

$$V_{out} = \frac{V_{in}}{1-D} \tag{3}$$

While this is in the acceptable range, it may be impossible to achieve in real applications due to parasitics in the circuit which can reduce the maximum achievable duty cycle. Assuming an ideal system, the operating input voltage range would be 20-180 Volts.

The main reason that this topology is unsuitable for use in a two-stage, grid-tied PV inverter is because it requires the use of a higher voltage rated device for the main switch – the switch sees voltage stress equal to the output voltage (200 Volts). This results in higher conduction and switching losses for the device which lowers the overall system efficiency. Real world efficiency at high input voltages can be very good, 98% or greater, but at low line can suffer, where efficiency might drop to 80% or so. Variations of this topology like the tapped-inductor boost converter or Wide-Input Wide-Output (WIWO) topology [6] can reduce the voltage stress of the main device. These modified topologies do not always account for leakage inductances which could cause additional voltage stresses.

1.13 Flyback Topology

The Flyback converter shown in (Figure 5) is more suitable than the boost converters for PV applications. It is easier to design for operation across a given duty cycle range. With a turns ratio of 4 and maximum output diode voltage stress of 500, the input voltage range is from 20-75 Volts over a duty cycle of 40-71%. The main switch sees a voltage stress of 125 Volts.

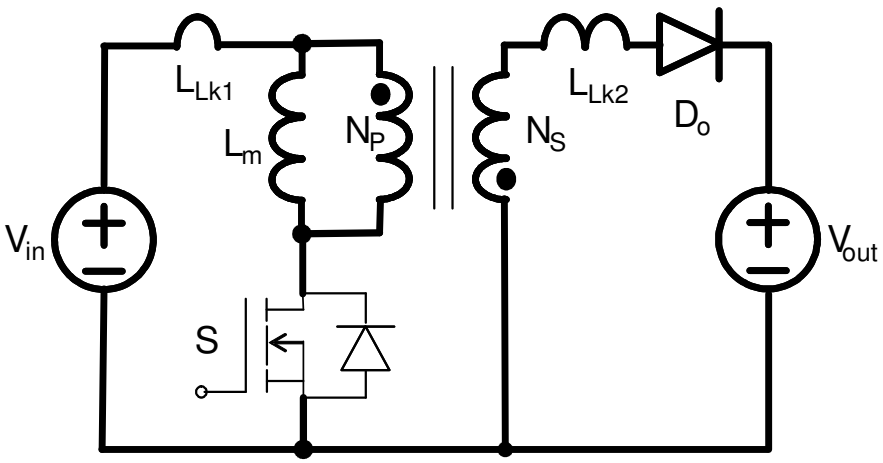


Figure 5. Flyback Topology

The duty cycle is given by Eqn. 4, and the voltage stresses are given by Eqn. 5.

$$V_{out} = V_{in} \frac{N_s}{N_p} \frac{D}{1-D} \tag{4}$$

$$V_{switch} = V_{in} + \frac{V_{out}}{\left(N_s / N_p \right)} \qquad \& \qquad V_{diode} = V_{out} + V_{in} \frac{N_s}{N_p} \tag{5}$$

The main disadvantage of this circuit comes from how it deals with the leakage inductor L_{LK1} shown in the circuit topology. This inductor comes from parasitics of the interconnects and from the flyback transformer itself – in practice it causes a high-voltage spike across the switch and must be dealt with by either a RCD (resistor, capacitor, diode) clamp or RC snubber. The voltage rating of the switch must also be higher than the maximum expected voltage stress to ensure sufficient safety margin, for example, 125 Volt stress is expected, but a 200 Volt or 250 Volt rated device might be used. This causes a large drop in efficiency.

Another disadvantage is the pulsating flow of energy from the input source. Large-amplitude, high-frequency current ripple increases the amount of decoupling capacitance needed at the input of the converter. Additionally, all of the energy must transfer through the flyback inductor, instead of allowing a direct conduction path from the source to the output. This causes another drop in efficiency. Typical efficiency for the flyback converter is less than 80%.

1.11 Active-Clamp Flyback Topology

Shown in (Figure 6), the active-clamp flyback converter can achieve a high boost ratio and low switching loss due to zero-voltage turn-on of the MOSFET devices [7]. The two switches operate synchronously with some dead-time between the turn-off of one switch and the turn-on of the other. It is more efficient than the traditional flyback converter because there is no turn-on switching loss for either switch, and it does not need to dissipate the energy stored in the leakage inductor each switching cycle. This

active-clamp topology has the same issue with pulsating energy from the source and inefficiency due to the fact that all energy must flow through the flyback transformer.

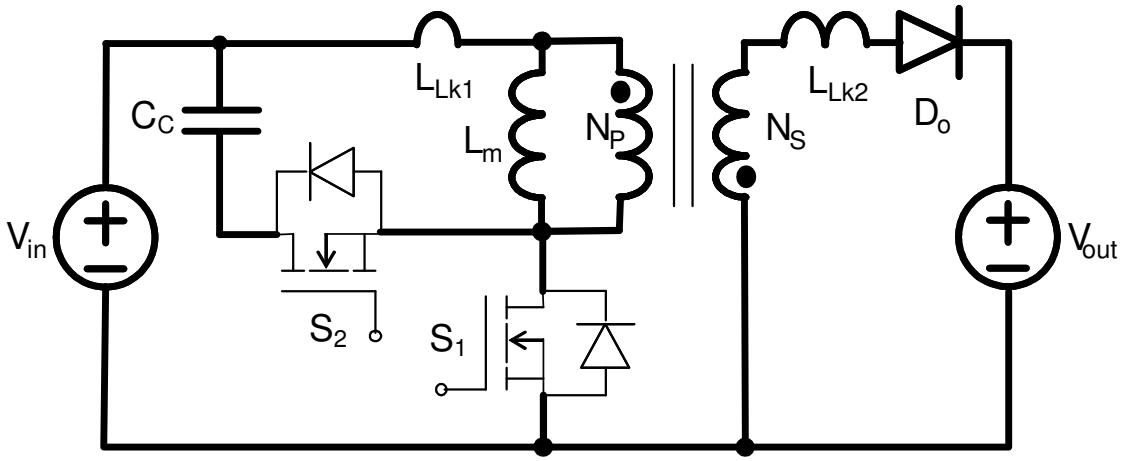


Figure 6. Active-Clamp Flyback Topology

The duty cycle is given by Eqn. 6, and the voltage stresses are given by Eqn. 7.

$$V_{out} = V_{in}\frac{N_s}{N_p}\frac{D_{eff}}{1-D_{eff}}, \qquad D_{eff} = D - \frac{1}{D}\frac{2L_{Lk1}P_o f_{sw}}{\left(V_{in} + \frac{N_p}{N_s}V_{out}\right)V_{in}} \tag{6}$$

$$V_{switch} = V_{in} + \frac{N_p}{N_s}V_{out} + \frac{2L_{Lk1}f_{sw}P_o^{\max}}{\eta V_{in}D(1-D)} \tag{7}$$

From [7], the last term of Eqn. 7 represents the voltage across the resonant inductor, L_{LK1}. If the resonant inductor is extremely small, then the resulting equations should be identical to the traditional flyback equations. Typical efficiencies of the active-clamp flyback range from 80% up to 92% [8-10], but 94.7% has been measured experimentally with the EnPhase microinverter at 25 Volt input, 150 Watt output. The improved efficiency is due to a complicated control scheme which switches operating modes (e.g., PWM, quasi-resonant, and boundary-mode) dependent on output voltage level, since the active-clamp flyback circuit in the EnPhase microinverter is generating a rectified sine-wave output.

1.15 Push-Pull Topology with AC-Ripple Port

The push-pull converter shown in (Figure 7) is an isolated, current-fed converter [5]. The output thyristors are used as low-frequency, polarity-selection switches to send power to the grid, whereas conventional single-stage converters might use a PWM-controlled cycloconverter output stage [11]. By adding a tertiary winding to the transformer and a small H-bridge composed of bi-directional switches, an ac-ripple port can be formed which acts to cancel low frequency ripple at the input of the push-pull converter. There is a large-amplitude, low frequency ripple across the auxiliary capacitor. The auxiliary inductor acts to smooth the high-frequency current. The output inductor further reduces the high-frequency switching ripple.

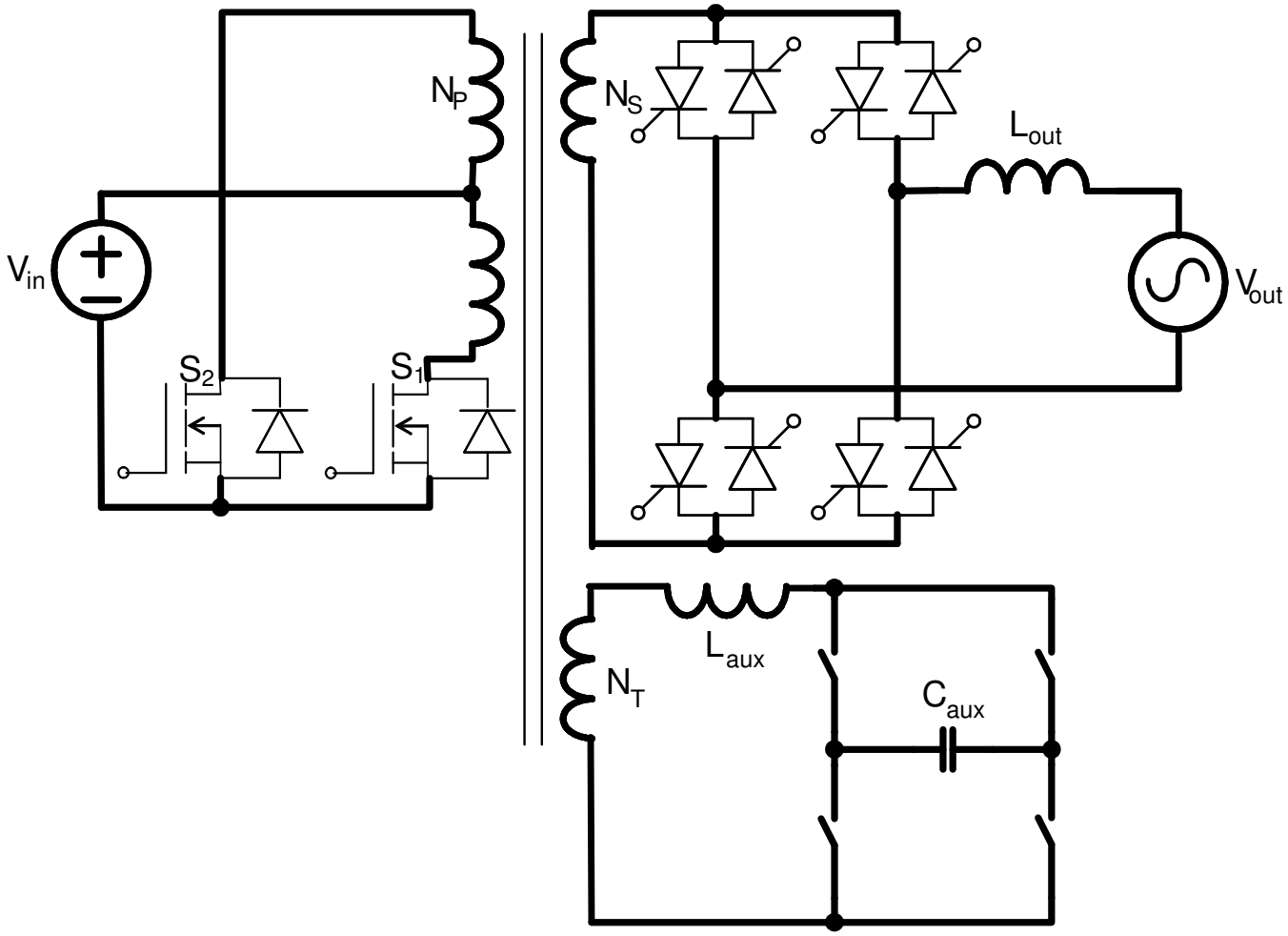


Figure 7. Push-Pull with Ac-ripple port Topology

There are numerous problems with this topology – the most significant issue is the huge number of switches that must be controlled. Since each bi-directional switch of the ac-ripple-port H-bridge must actually be two IGBT's or MOSFET's connected back-to-back, the total switch count of this circuit is 18. 10 of these switches must be run at PWM-frequency; the other 8 of the thyristor output bridge are run at line-frequency. This large switch-count causes huge conduction loss and there is also potential for significant switching losses.

The other major issue is control complexity, since the ac-ripple-port has bi-directional power flow. There is significant interaction between the push-pull stage and the ac-ripple port since they are connected through the high-frequency transformer.

For a typical push-pull dc-dc converter, the voltage stress of the switches is twice the input voltage – in this case it is harder to estimate since the schematic of (Figure 7) omits leakage inductances on the primary side. These leakage inductances, combined with the current-fed nature of the ac-ripple port, could create significant voltage stresses

for the devices. The voltage stress originates from trying to abruptly stop the current through the inductor.

1.16 Reboost Topology

The Reboost topology (Figure 8), patented by [12] and also called the clamp-mode coupled-inductor boost converter by [13], includes a diode-capacitor clamp. This allows the energy stored in the leakage inductor to be transferred to the output, and provides a direct conduction path from the input to the output. The switch, transformer, and output diode form a flyback converter. The switch, leakage inductor, and clamp diode form a boost converter.

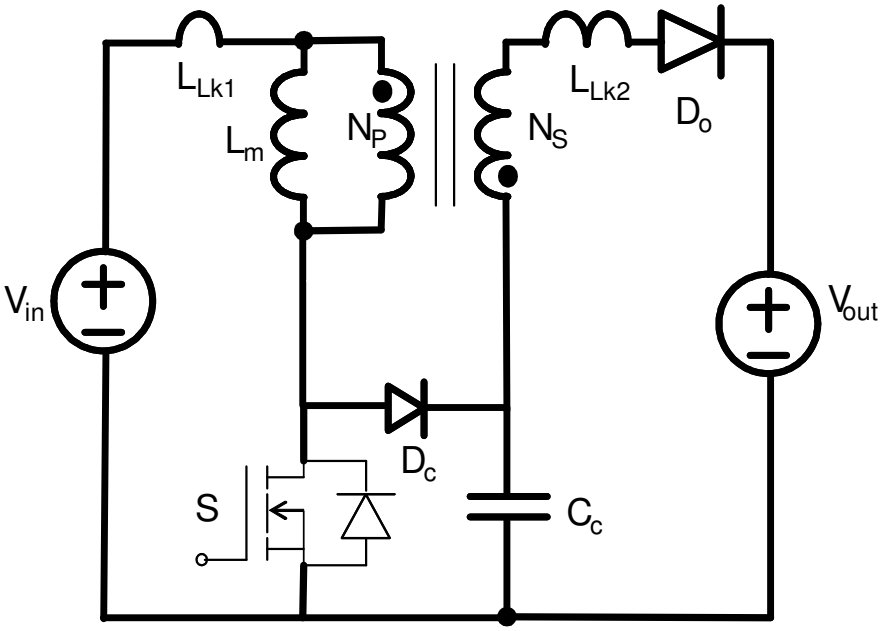


Figure 8. Reboost Topology

The Duty cycle is given by Eqn. 8, and the voltage stresses are given by Eqn. 9.

$$V_{out} = V_{in} \frac{1 + \frac{N_s}{N_p} D}{1 - D} \tag{8}$$

$$V_{switch} = \frac{\frac{N_s}{N_p} V_{in} + V_{out}}{\frac{N_s}{N_p} + 1} \qquad \& \qquad V_{diode} = \frac{\left(\frac{N_s}{N_p} V_{in} + V_{out}\right)\left(\frac{N_s}{N_p}\right)}{\frac{N_s}{N_p} + 1} \tag{9}$$

This topology is a major improvement over the standard flyback because the peak voltage stress of the main device can be limited in an efficient manner. It still suffers from the same disadvantage of pulsating energy from the input source – its behavior is like a flyback, not like a boost converter. The operating modes are most clearly defined in [14]. Efficiency optimization and loss calculations are derived in [15], with calculated efficiencies up to 97%.

2 Charge-Pumped Reboost Topology

The Charge-pumped Reboost topology is two-component modification to the Reboost topology [16]. It is different than the integrated boost-flyback converter based on the connection point of the pump diode [17, 18]. By adding an additional charge-pump circuit in series with the output, the converter achieves continuous input-current and higher voltage gain while reducing the voltage stress for the main device and output diode (Figure 9).

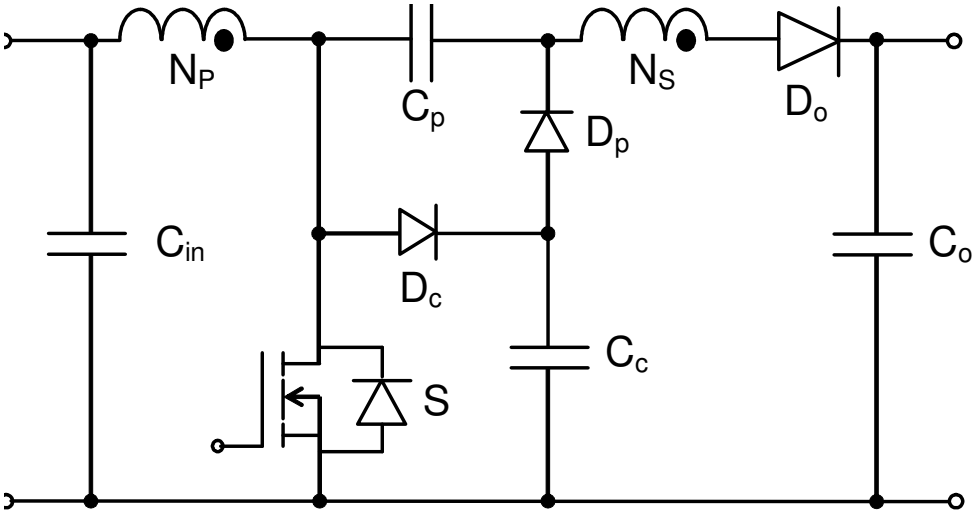


Figure 9. Charge-Pumped Reboost Topology

The common-name of each component in (Figure 9) is given below:

C_{in}	Input Capacitor
C_P	Pump Capacitor
C_C	Clamp Capacitor
C_{out}	Output Capacitor
D_C	Clamp Diode
D_P	Pump Diode
D_o	Output Diode
S	Switch, Mosfet
N_P	Primary Winding
N_S	Secondary Winding

Table 2

This topology has the advantages of continuous input current and even lower voltage stresses as compared to the Reboost converter. Its main disadvantage arises from the charge-pump loop. When the switch turns on, the current flowing from the clamp capacitor into the pump capacitor is limited only by parasitic inductances. Thus the peak

current in the charge-pump loop can be extremely high at startup and during very small duty cycles. During normal operation, the voltage difference between the clamp capacitor and pump capacitor is small, so the peak current between them is also fairly small.

2.1 Operating Modes

At t_0, during the first operating mode (Figure 10) the main switch is already on. Current is flowing from the source and energy is being stored in the main inductor.

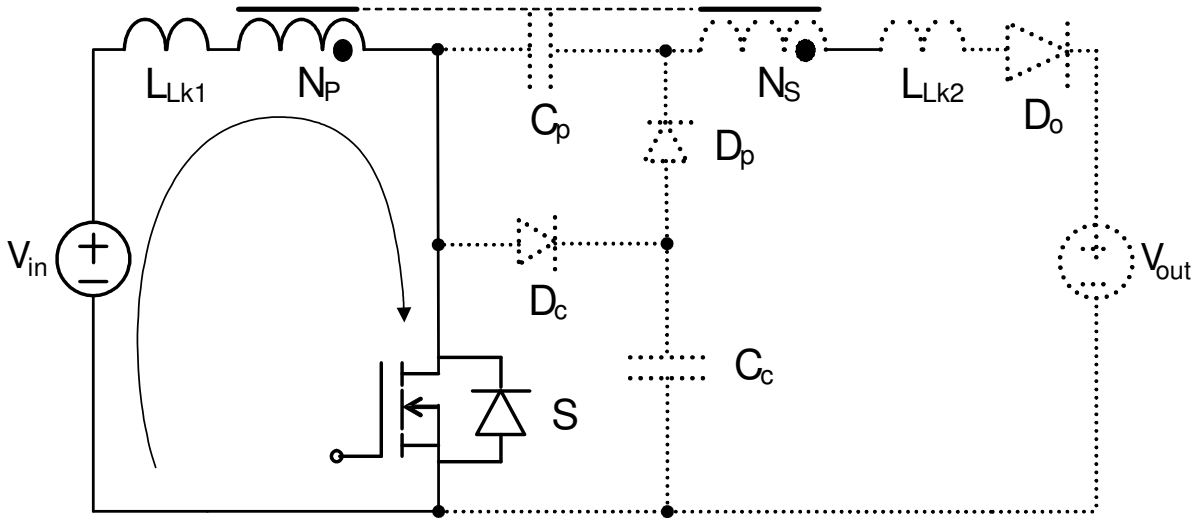


Figure 10. Charge-Pumped Reboost Operating mode 1

At t_1, during the second operating mode (Figure 11) the main switch turns off. Current from the leakage inductor L_{Lk1} flows through the clamp diode into the clamp capacitor. This clamp circuit limits the peak voltage of the main switch. Current also begins to flow through the pump capacitor and the secondary winding. The output leakage inductor L_{Lk2} limits the dI/dT of this current.

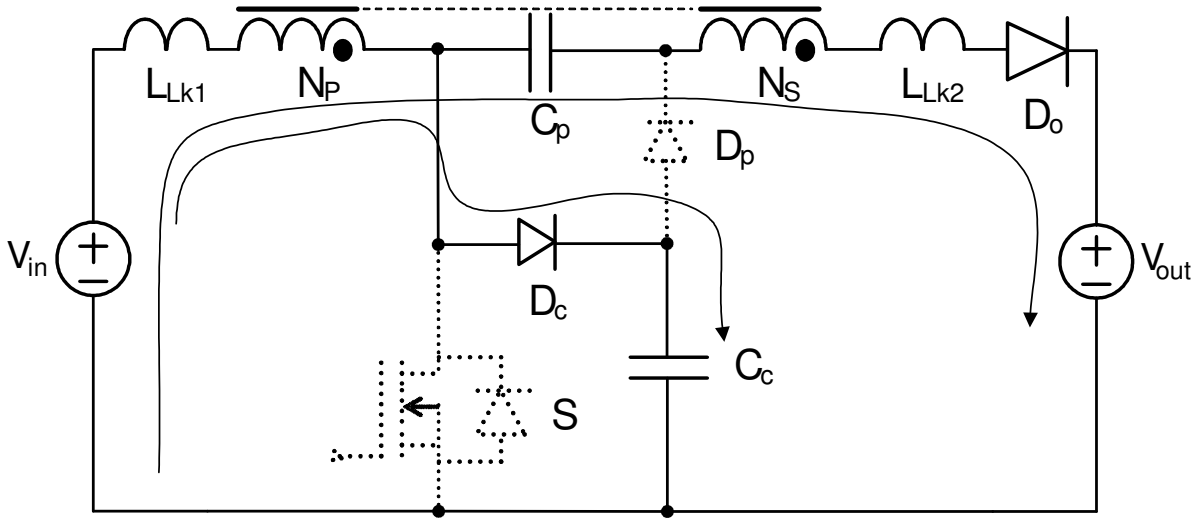


Figure 11. Charge-Pumped Reboost Operating Mode 2

At t_2, during the third operating mode (Figure 12) the energy in the leakage inductor L_{Lk1} has been transferred to the clamp capacitor, so the clamp circuit turns off. Current continues to flow from the input to the output through the inductor and pump capacitor.

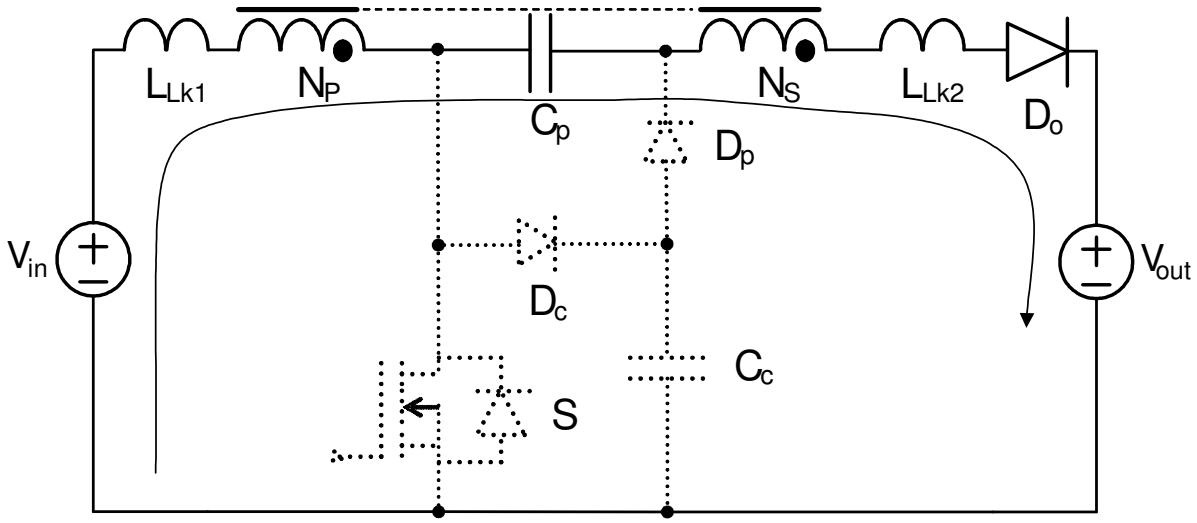


Figure 12. Charge-Pumped Reboost Operating Mode 3

At t_3, during the fourth operating mode (Figure 13) the main switch turns on again. Current still flows through the secondary winding due to the leakage inductor L_{Lk2} which slows down the turn-off speed of the output diode. Current flows from the source through the inductor and through the main switch. Current through the pump capacitor reverses as energy is transferred in a charge-pump action between the clamp capacitor and the pump capacitor.

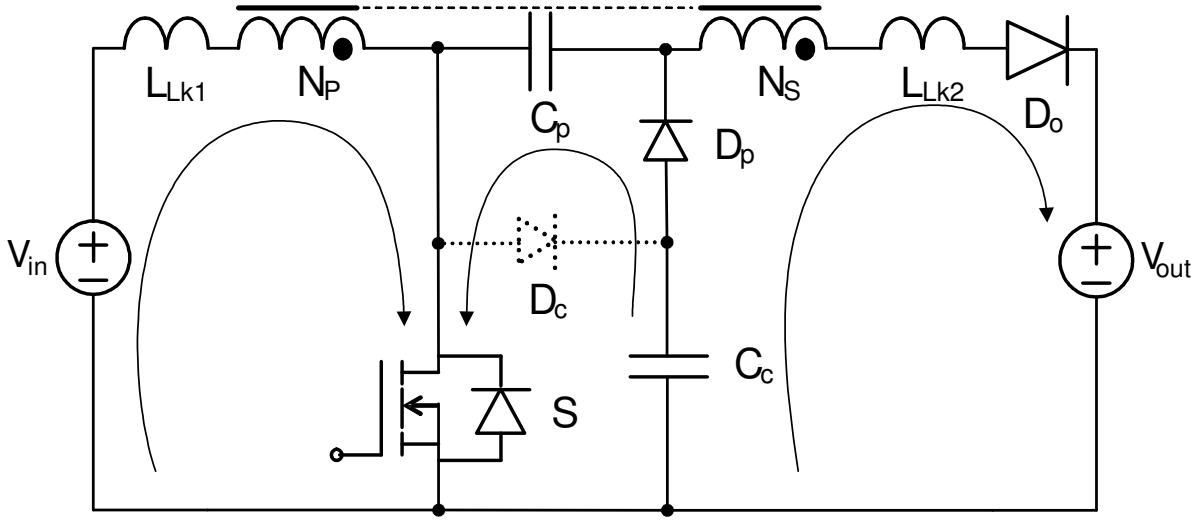


Figure 13. Charge-Pumped Reboost Operating Mode 4

At t_4, during the fifth operating mode (Figure 14) the output diode turns off. Current in the charge-pump loop flows until the voltage equalizes between the clamp capacitor and pump, or until the switch turns off. The first operating mode resumes at t_5.

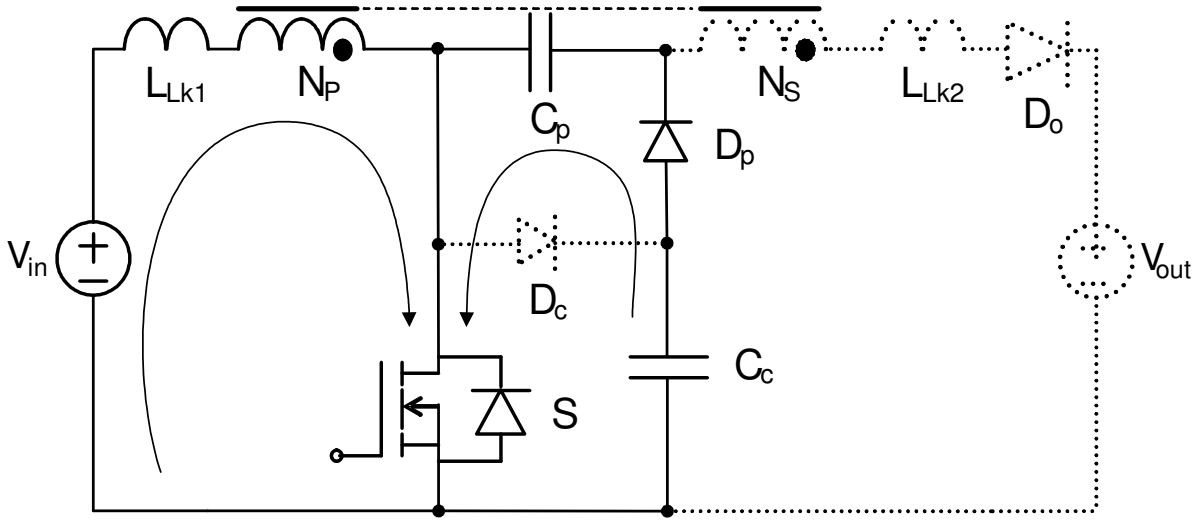


Figure 14. Charge-Pumped Reboost Operating Mode 5

The timing diagram for these operating modes is shown below in (Figure 15).

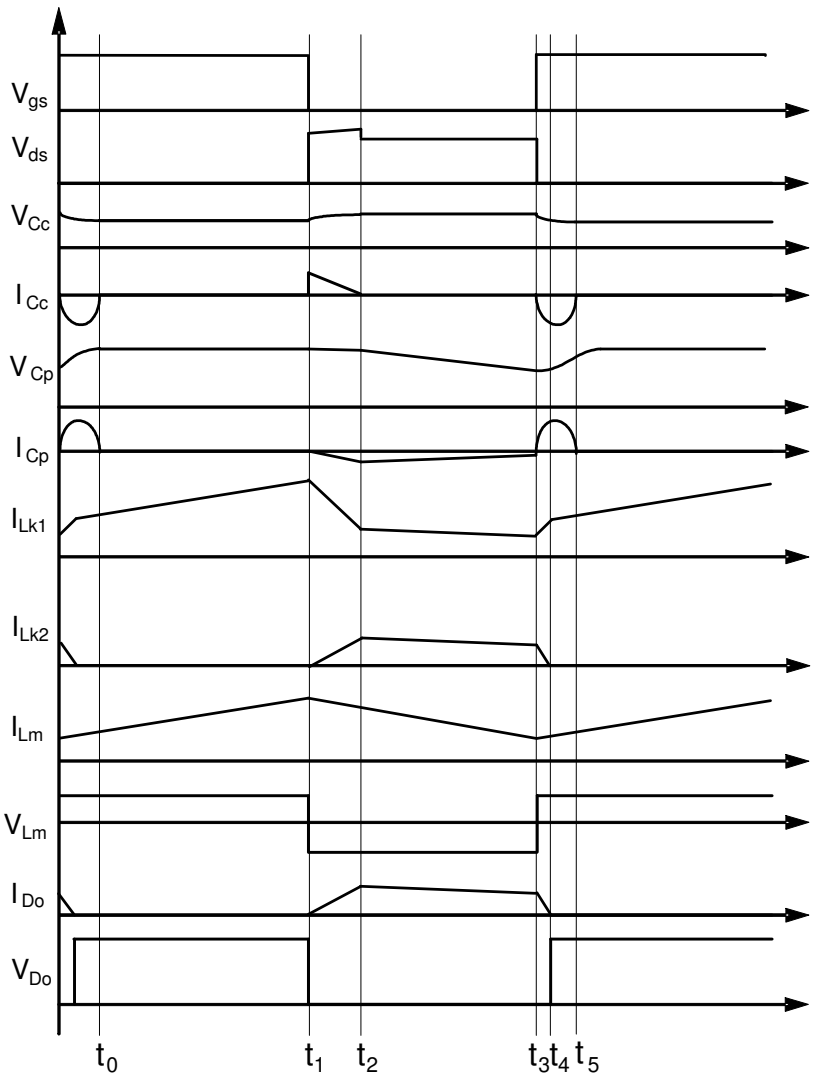


Figure 15. Charge-Pumped Reboost Timing Diagram

Some of the measured operating waveforms are shown below in (Figure 16) for comparison.

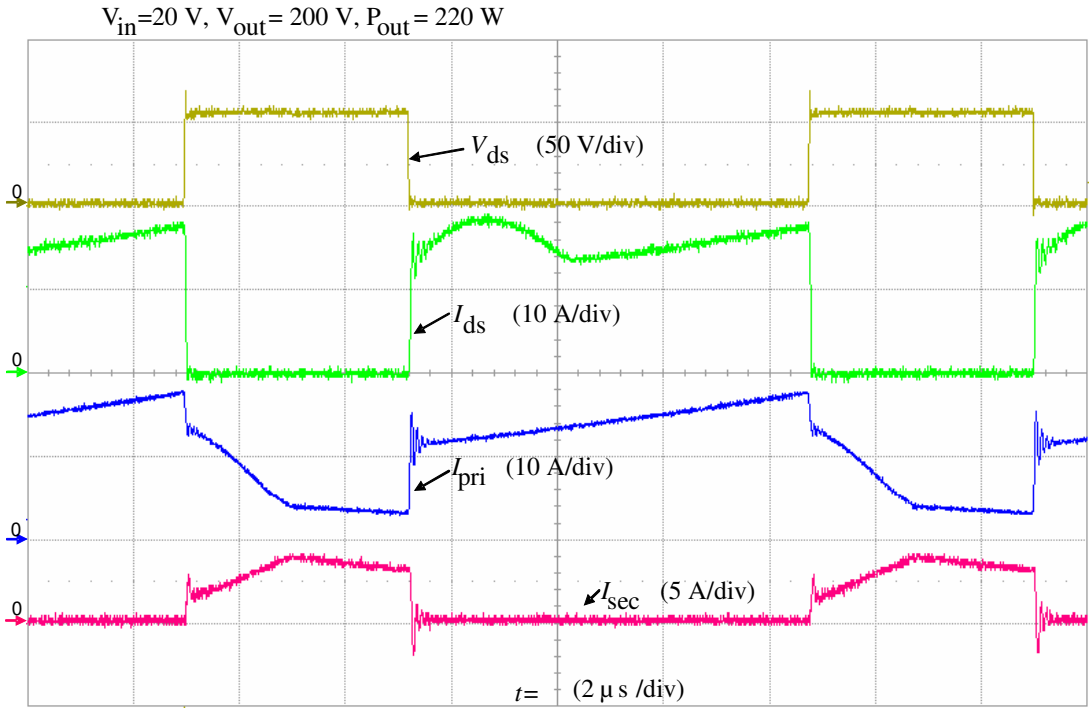


Figure 16. Measured Operating Waveforms

2.2 Voltage Stresses

The voltage stresses for the various components of the converter are given in the following equations.

$$V_{ds} = V_{Dp} = V_{Dc} = V_{Cp} = V_{Cc} = \frac{\left(\frac{N_s}{N_p} V_{in} + V_{out}\right)}{\left(\frac{N_s}{N_p} + 2\right)} \tag{10}$$

The voltage stress of Eqn. 10 shows that there is equal voltage stress for the main switch, pump diode, clamp diode, pump capacitor, and clamp capacitor. In practice, the voltage stress of the main switch can be a little higher due to voltage-spikes at turn-off caused by inductance in the clamp loop.

$$V_{Do} = \frac{\left(\frac{N_s}{N_p} V_{in} + V_{out}\right)\left(\frac{N_s}{N_p} + 1\right)}{\left(\frac{N_s}{N_p} + 2\right)} \tag{11}$$

The voltage stress for the output diode is given by Eqn. 11, and is the highest stress of any component in the circuit. Again, the peak voltage stress of this component can be significantly higher (on the order of 50%) due to reverse recovery effects and parasitic capacitance of the output diode.

$$V_{pri\_charge} = V_{in} \qquad V_{pri\_discharge} = V_{ds} - V_{in} \tag{12}$$

The voltage stresses for the primary winding is given by Eqn. 12.

$$V_{sec\_charge} = \frac{N_s}{N_p} V_{in} \qquad V_{sec\_discharge} = V_{out} - 2V_{ds} \tag{13}$$

The voltage stress for the secondary winding is given by Eqn. 13.

2.3 Voltage Gains

The overall voltage gain is given by Eqn. 14, and is identical to Eqn. 15 which is re-arranged for convenience.

$$\frac{V_{out}}{V_{in}} = \frac{\left(2 + \frac{N_s}{N_p} D\right)}{1 - D} \tag{14}$$

$$D = \frac{V_{out} - 2V_{in}}{\left(\frac{N_s}{N_p} V_{in} + V_{out}\right)} \tag{15}$$

3 Design for PV Applications

In this section, suggestions will be made for design methodology and rules. For this specific topology, in this specific application, it is assumed that the input voltage is variable, and the output voltage is fixed. It is also assumed that the maximum power is applicable at any voltage level. The design specifications are given in the following table.

Input Voltage	20 V_{dc} to 70 V_{dc}
Output Voltage	200 V_{dc}
Output Power	200 W
Acceptable Duty Cycle	10 to 90%
Output Diode Voltage Rating	600 V
Switch Voltage Rating	150 V
Switching Frequency	100 kHz

Table 3

3.1 Design for wide-input range

One desirable characteristic for a front-end converter for PV applications is that it be able to handle a wide input-voltage range to permit use with a large assortment of PV panels. In order to be practical, the selected topology must have reasonable duty cycles and voltage stresses across the entire operating range.

In order to properly design the power stage, it is necessary to determine the limiting factor of the design. A good place to start is with the output diode, since it experiences the highest voltage stress during operation. Typically the desired input voltage range is specified, and a maximum voltage rating for the output diode is known, so these two factors can be used to get an initial value for the turns-ratio of the flyback transformer.

At this point, the voltage rating requirements of the main switch and other associated components can be used to modify the turns-ratio into a more agreeable value. Since these components are usually chosen with high-efficiency in mind, they tend to be oversized in terms of current-handling capabilities. This is also useful for long-term reliability and survivability during transient-conditions, where peak-transient currents can be an order of magnitude higher than peak-operating currents.

If we plot the normalized voltage stress of the output diode and the main switch versus the turns ratio (Figure 17) at the highest input voltage, we can find the intersection point which represents the highest margin of safety for both devices. In the figure, the numbers are normalized by dividing the calculated voltage stress by the voltage rating of the component. The intersection occurs at a turns ratio of about 3. Using this value and the input voltages listed above, the duty cycle ranges from 14.6% to 69.4%.

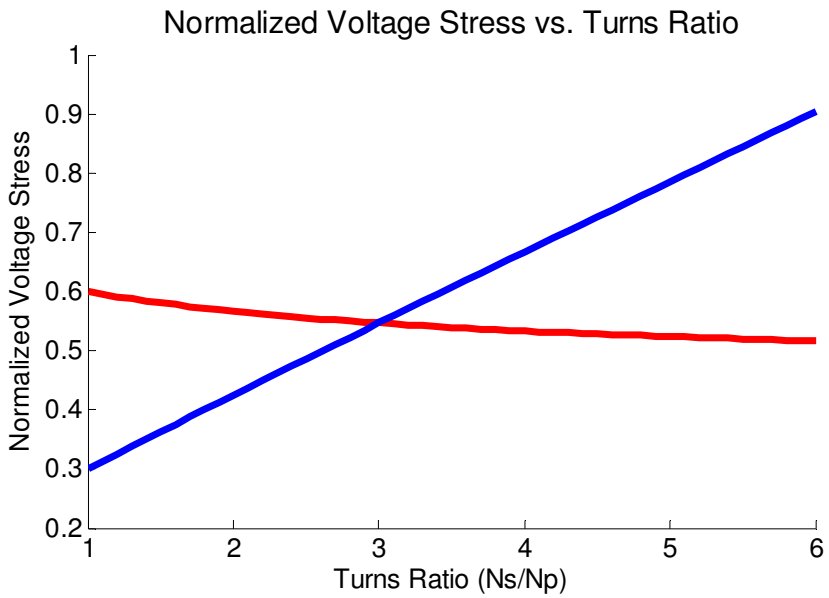


Figure 17. Normalized Voltage Stress vs. Turns Ratio.

It is important to note that this method is biased heavily by the normalizing values. If a smaller value were used to normalize the switch stress (e.g. use a lower voltage-rated switch), then this technique would favor a higher turns ratio.

3.2 Minimizing Low-Frequency Input Ripple

Line frequency ripple will be present in the system since this converter is intended to serve as part of a two-stage, single-phase PV micro-inverter. 60 Hz ac-current at the output of the inverter translates to 120 Hz voltage-ripple at the bus capacitor between the dc-dc stage and the dc-ac stage. Since, for a fixed duty-cycle, there is a voltage conversion relationship between the input and output of the dc-dc converter, this ripple will naturally propagate back to the input capacitor, which affects the performance of the PV source by moving it away from the maximum power point. This structure will be further explained in section 4.4.

We can reduce the low-frequency input ripple by several means – design topology, passives, and active compensation.

One example of solving the low-frequency ripple propagation by the design topology would be the use of a discontinuous-conduction-mode flyback converter. With this DCM topology, the load should not affect the source at all. The disadvantage of this approach is that the discontinuous flyback converter is very inefficient.

The problem may also be solved through passive means, using inductors and capacitors to filter out the low-frequency ripple. The disadvantage here is that very large component sizes must be used – which usually involves electrolytic capacitors. Electrolytic capacitors are unsuitable for high ambient-temperatures, and may eventually fail due to evaporation or leakage of the liquid electrolyte.

Active compensation means either designing the compensator for high gain at the frequency of interest or injecting some equal-and-opposite signal to cause the controller to cancel out the ripple [19]. With a traditional PID compensator, this translates into

designing for the highest bandwidth possible. These compensation techniques will be covered in more detail in section 4.

3.3 Power Stage Component Selection

3.31 Main Switch

The main switch should be MOSFET-based instead of IGBT since this design favors high switching frequency and smaller size. CoolMOS is unnecessary since there is low voltage stress for this part of the circuit, although it would be acceptable to use given that there is no body-diode conduction in this topology.

The Infineon IPD200N15N3G MOSFET was chosen for its low $R_{DS\text{-}on}$ and fast switching speeds relative to its 150 V_{ds} rating. This particular design could use a 100 V_{ds} rated part such as the Fairchild FDB3632 with some additional modification, but it's useful to have extra safety margin during testing.

3.32 Output Diode

The output diode should be an ultra-fast type high-voltage power diode with low junction capacitance. For this design, the Vishay 15ETH06S was selected. It is a 600 Volt, 15 Amp rated diode with a typical reverse-recovery time of 22 nanoseconds. The ampere-rating is overkill for this design, but the reverse-recovery characteristic is highly favorable.

3.33 Clamp and Pump Diodes

The diodes used for the clamp and pump circuits should be schottky diodes in order to avoid reverse-recovery and forward-recovery losses. The Central-Semi CMSH5-100 was used since it is rated for 100 Volts blocking and peak surge currents up to 125 Amps. In testing, the peak current through the charge-pump circuit was nearly 100 Amps under startup conditions. (Figure 18) shows this peak-current characteristic.

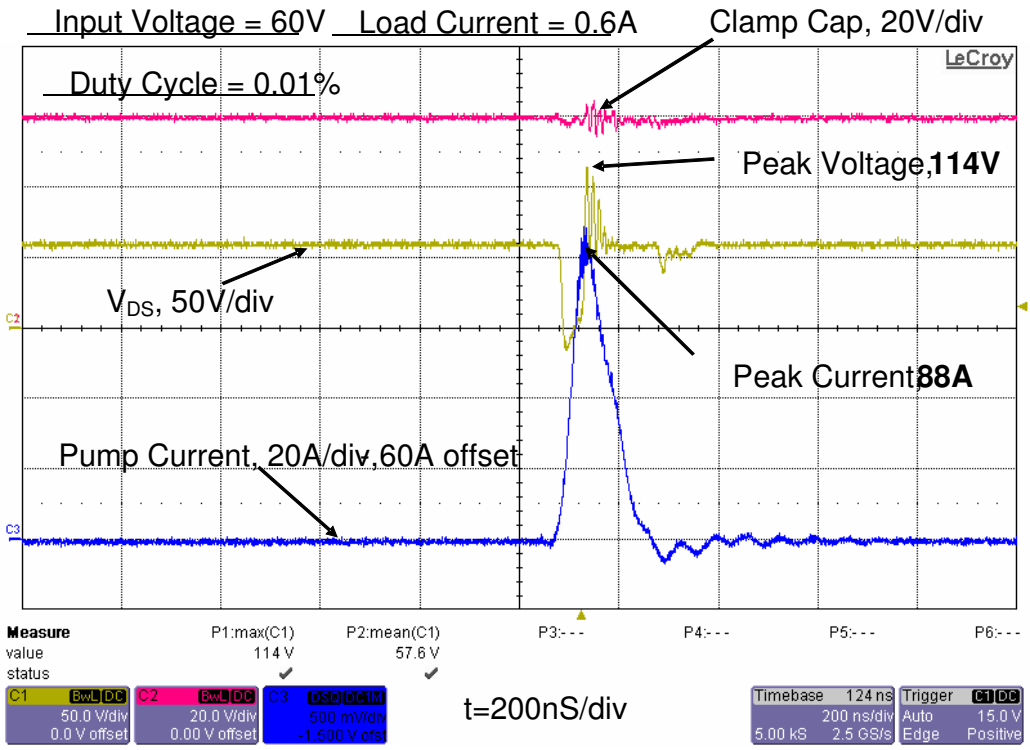


Figure 18. Peak Current Problem During Startup

The clamp circuit is shown below in (Figure 19). This is a low-inductance loop – most of the inductance is caused by device packaging. This extra inductance causes the measured voltage spike across the switch.

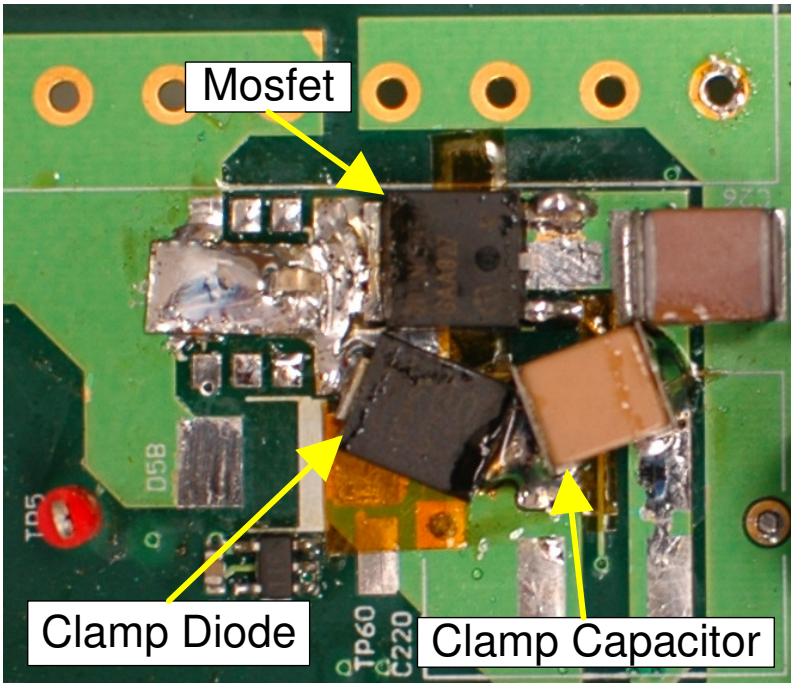


Figure 19. Clamp Circuit

3.34 Clamp and Pump Capacitors

A quality X7R or X5R capacitor should be used for the clamp capacitor. This design utilized the TDK "Mega-cap" CKG57NX7R2A106M. Film capacitors should not be used for the clamp due to their higher parasitic inductance. The effect of this higher inductance is shown in (Figure 20). For the pump capacitor either film or ceramic may be used, but it is generally useful to have both parts be identical.

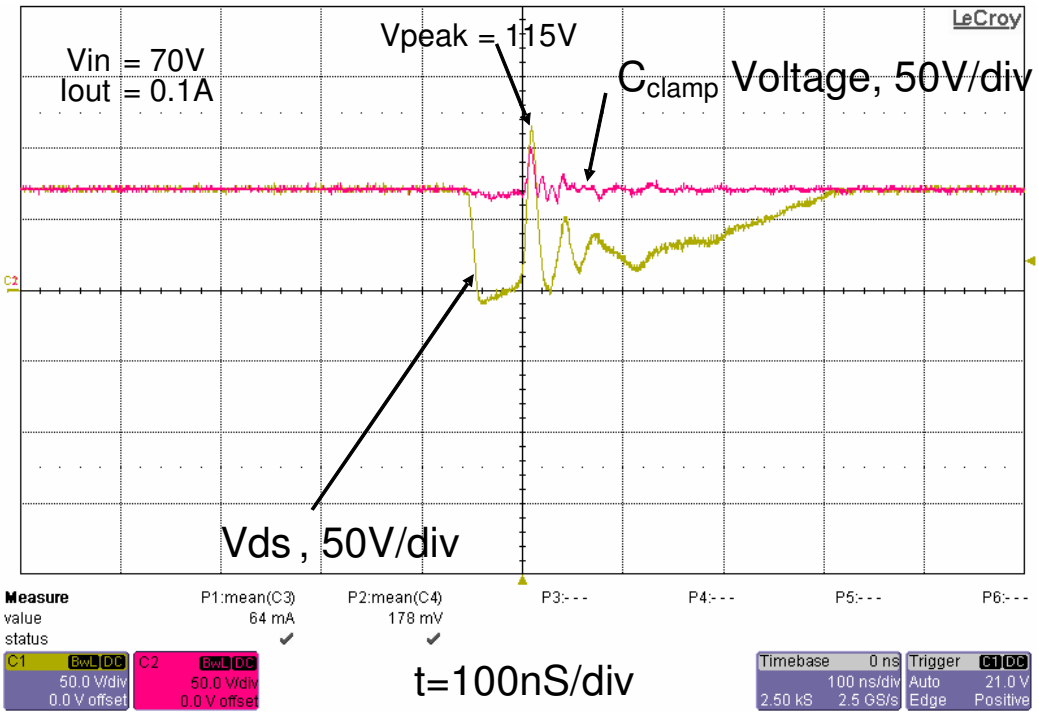


Figure 20. Clamp Circuit Performance with Film Capacitor

As can be seen in (Figure 21), if a ceramic capacitor is used, the peak voltage stress of the main switch can be reduced significantly.

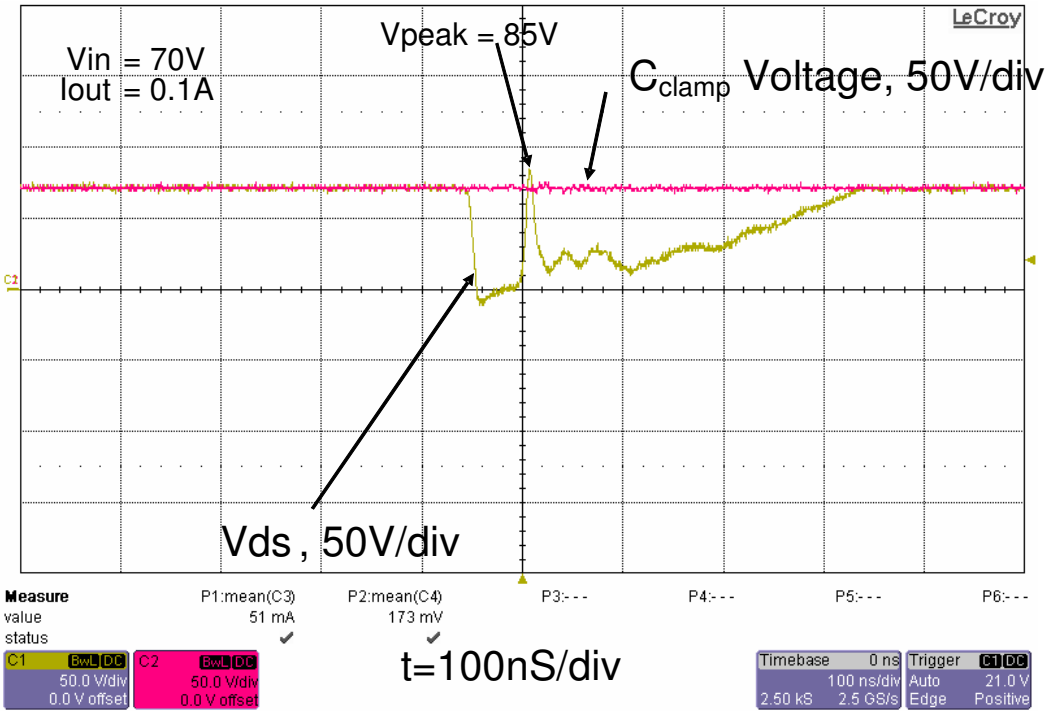


Figure 21. Clamp Circuit Performance with Ceramic Capacitor

3.35 Input and Output Capacitors

The input and output capacitors can be nearly any composition, but should be bypassed with ceramic capacitors. For the bulk output capacitance this design used 5 polypropylene EPCOS B32774D4226K capacitors in parallel. For the input capacitance this design used 3 ceramic TDK "Mega-cap" CKG57NX7R2A106M in parallel.

3.36 Flyback Inductance Design

The flyback magnetizing inductance value can be chosen to give peak efficiency at a certain operating point by designing it to transition from discontinuous-conduction to continuous-conduction mode at that point. By trial-and-error we found that a value of 24µH gave peak efficiency at half-load, 60V input. This value is measured across the primary winding of the flyback inductor with the secondary winding disconnected.

3.37 Parts Summary

C_{in} (Input Capacitor)	3x TDK CKG57NX7R2A106M	100V, 10uF, X7R Cap
S (Main Switch)	Infineon IPD200N15N3G	150V, 50A, 20mΩ
D_c (Clamp Diode)	Central-Semi CMSH5-100	100V, $5A_{avg}$, $125A_{peak}$
C_c (Clamp Capacitor)	TDK CKG57NX7R2A106M	100V, 10uF, X7R Cap
D_p (Pump Diode)	Central-Semi CMSH5-100	100V, $5A_{avg}$, $125A_{peak}$
C_p (Pump Capacitor)	TDK CKG57NX7R2A106M	100V, 10uF, X7R Cap
D_o (Output Diode)	Vishay 15ETH06S	600V, 15A, $22ns_{rev\_recovery}$
C_o (Output Capacitor)	5x EPCOS B32774D4226K	450V, 22uF, Metallized Polypropylene Film
L_m (Inductance)	------	24uH, 10:27 Turns Ratio

Table 4

3.4 Efficiency Results

The measured efficiency curves of the converter are shown below in (Figure 22). The peaks of the curves are regions where the drain-source voltage of the main switch resonates down to zero and the device achieves a zero-voltage turn-on transition. The valleys in the efficiency curves at lower power are where the converter is running in discontinuous-current mode, but the main switch still turns on at full drain-source voltage.

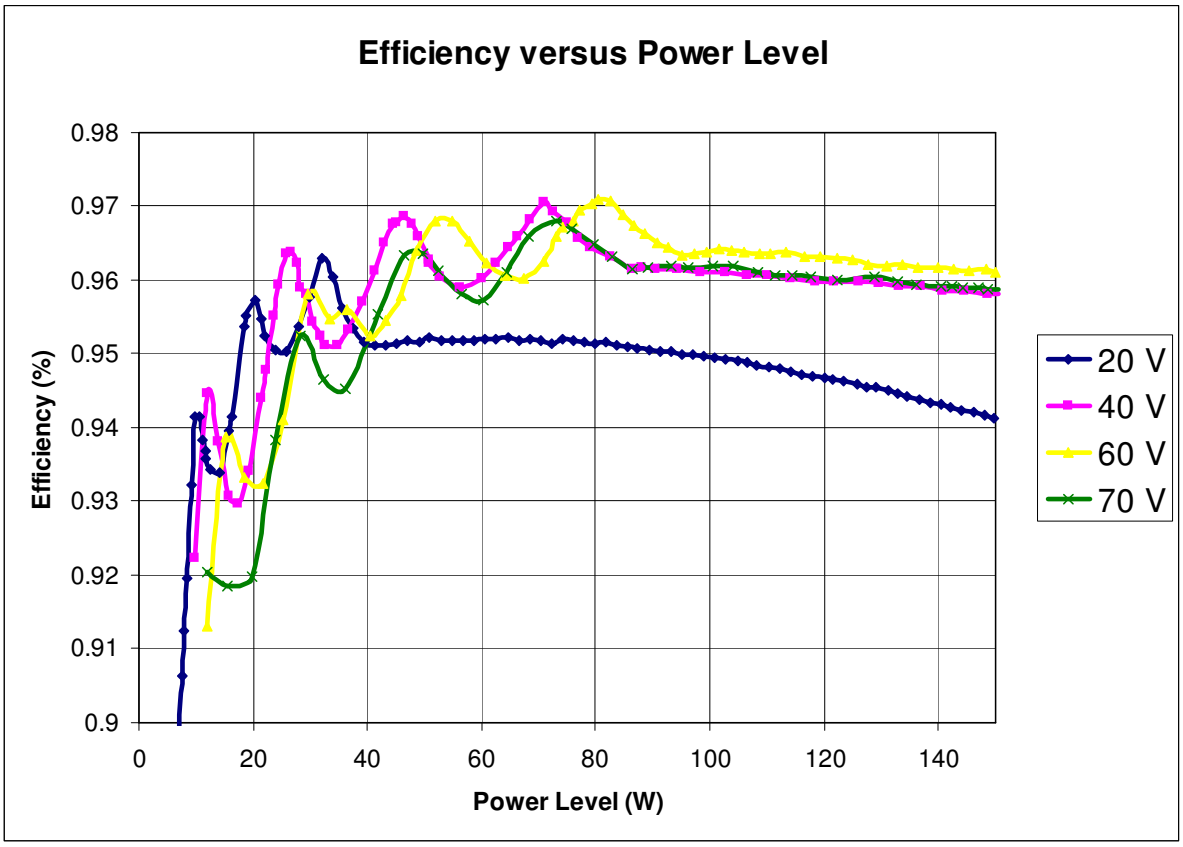


Figure 22. DC-DC Efficiency

The peak efficiency results at the boundary between the discontinuous inductor-current and continuous inductor-current modes. This boundary-mode operation is shown in (Figure 23). The current in the inductor decreases to zero, and as soon as the drain-source voltage decreases to zero, the MOSFET turns on.

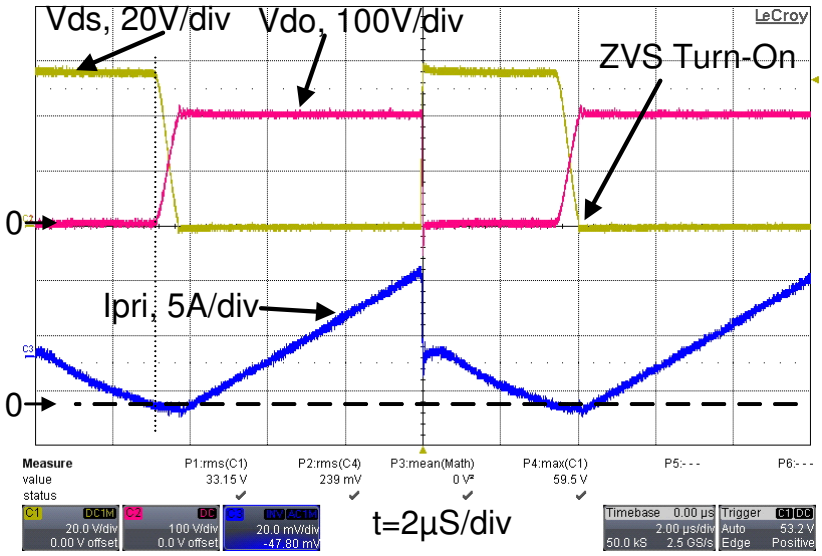


Figure 23. Boundary-mode ZVS Transition

For a compare and contrast, another DCM zero-voltage-switching transition is shown in (Figure 24), and a worst-case DCM hard-switching transition is shown in (Figure 25). Note that in (Figure 25) the peak voltage stress of the output diode is significantly higher – about 130V higher.

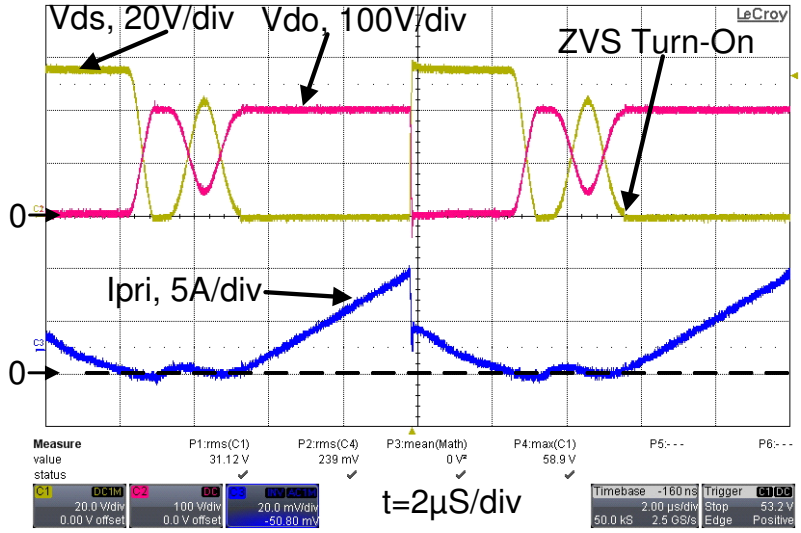


Figure 24. DCM ZVS Transition

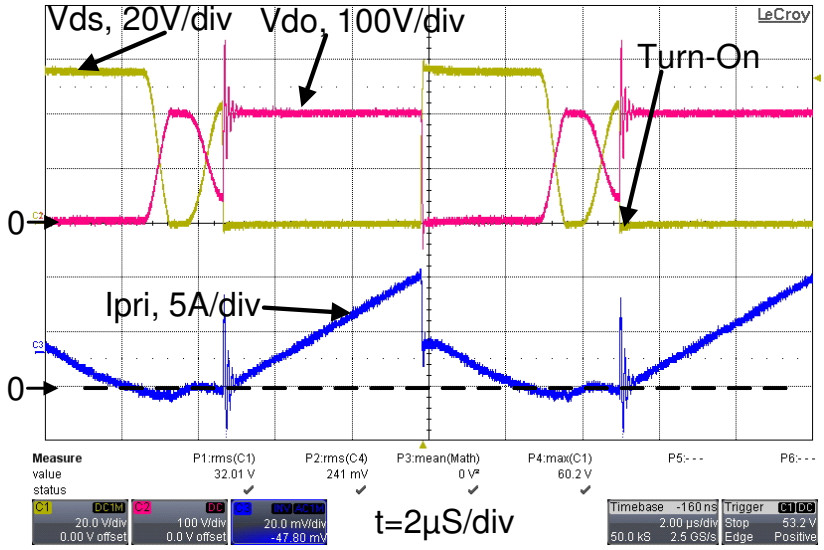


Figure 25. DCM Hard-Switching

If oversized components are used for the transformer core and main switch, the efficiency can be increased by several percentage points, as shown below in (Figure 26). The main differences are use of a lower voltage-rated switch (100 V vs. 150 V), larger transformer core (E55 vs. ETD-44), and lower switching frequency (85 kHz vs. 100 kHz). Rippling in the efficiency curve from DCM operation is not visible due to the small quantity of measurement points. Average efficiency is improved by approximately 1%.

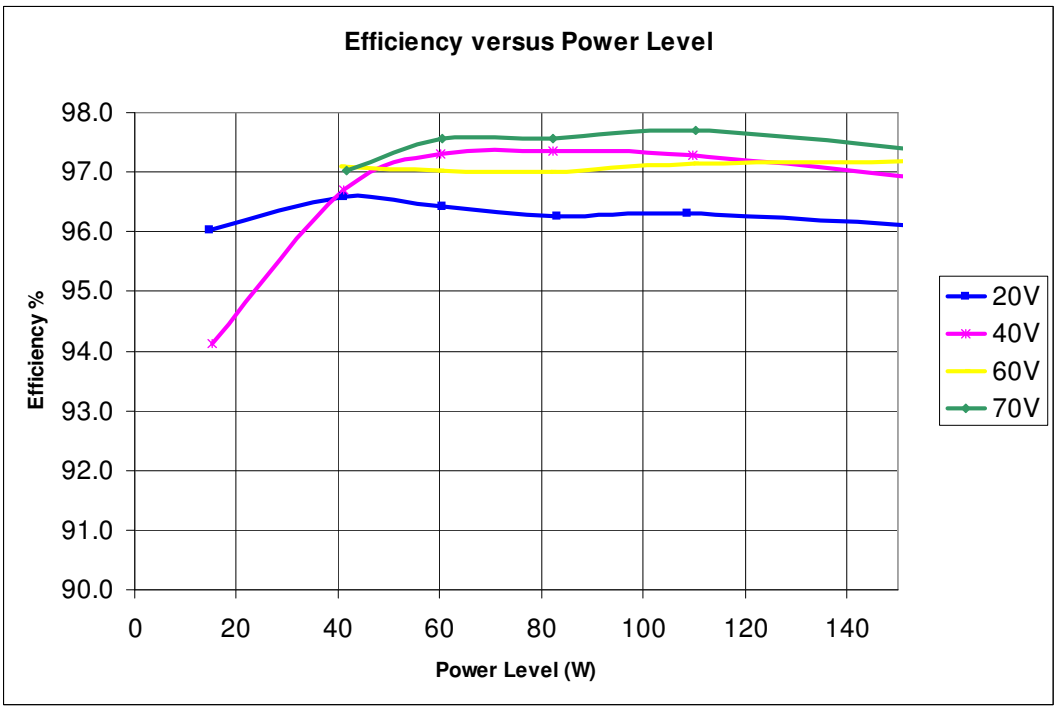


Figure 26. DC-DC Efficiency with Oversized Components

3.5 Thermal Imaging Analysis

A thermal image capture of the entire micro-inverter board running at a power level of 160 W is shown below in (Figure 27). (Figure 28) is provided as a reference picture of the dc-dc stage. The left side is the dc-dc stage, and the right side is the dc-ac stage. A close-up of the flyback transformer can be seen in (Figure 29). A close-up of the main device and clamp circuit can be seen in (Figure 30). Ambient air temperature was approximately 15 degrees centigrade.

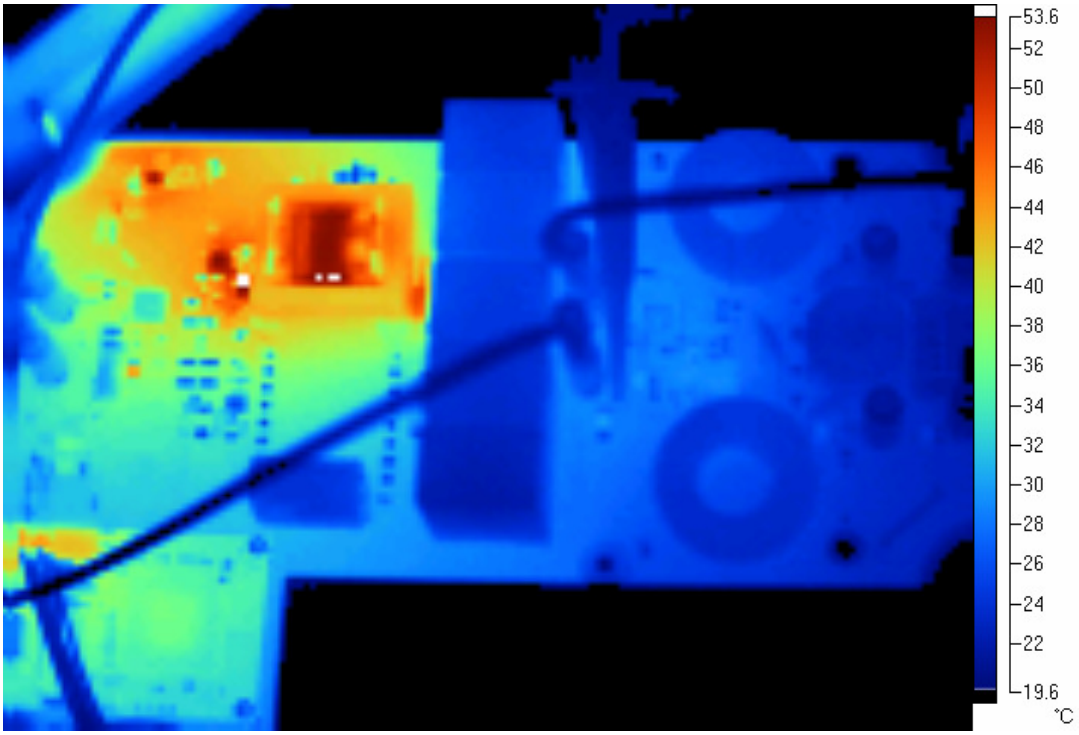


Figure 27. Thermal Image of Entire Microinverter

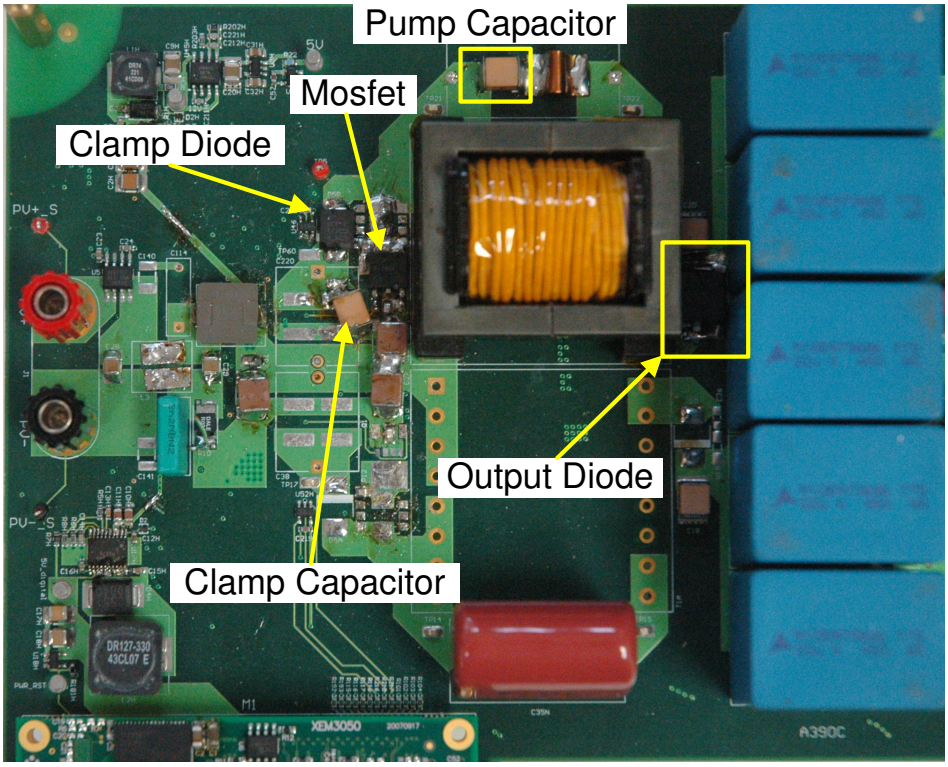


Figure 28. DC-DC picture

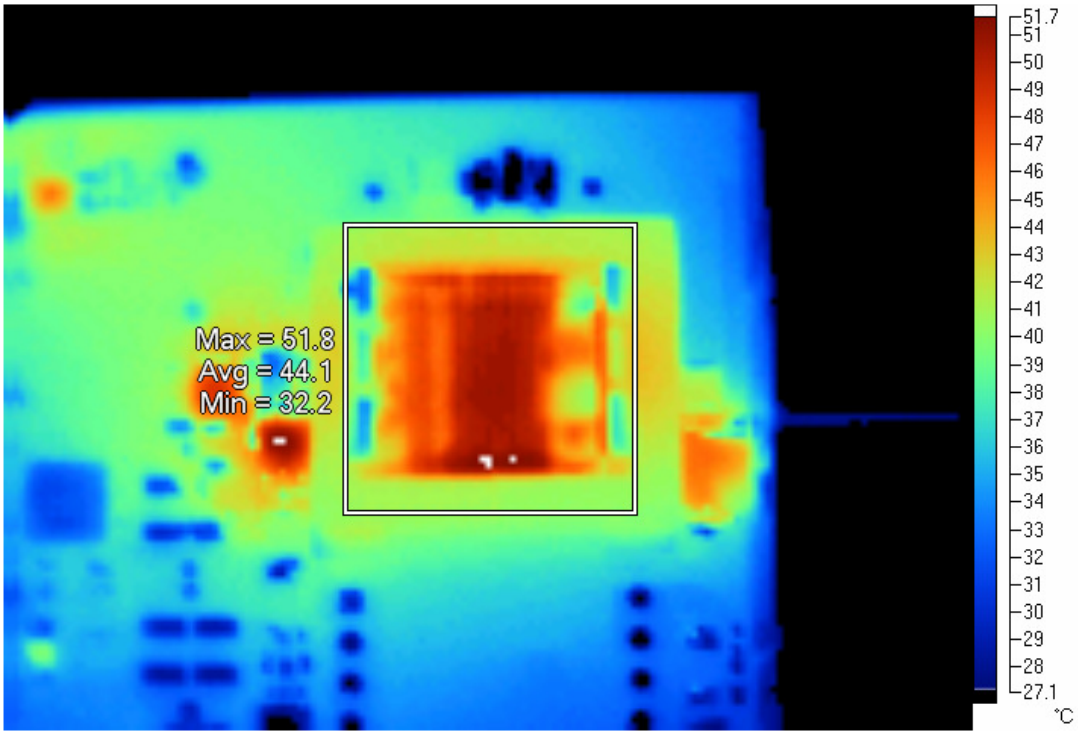


Figure 29. Thermal Image of Flyback Transformer

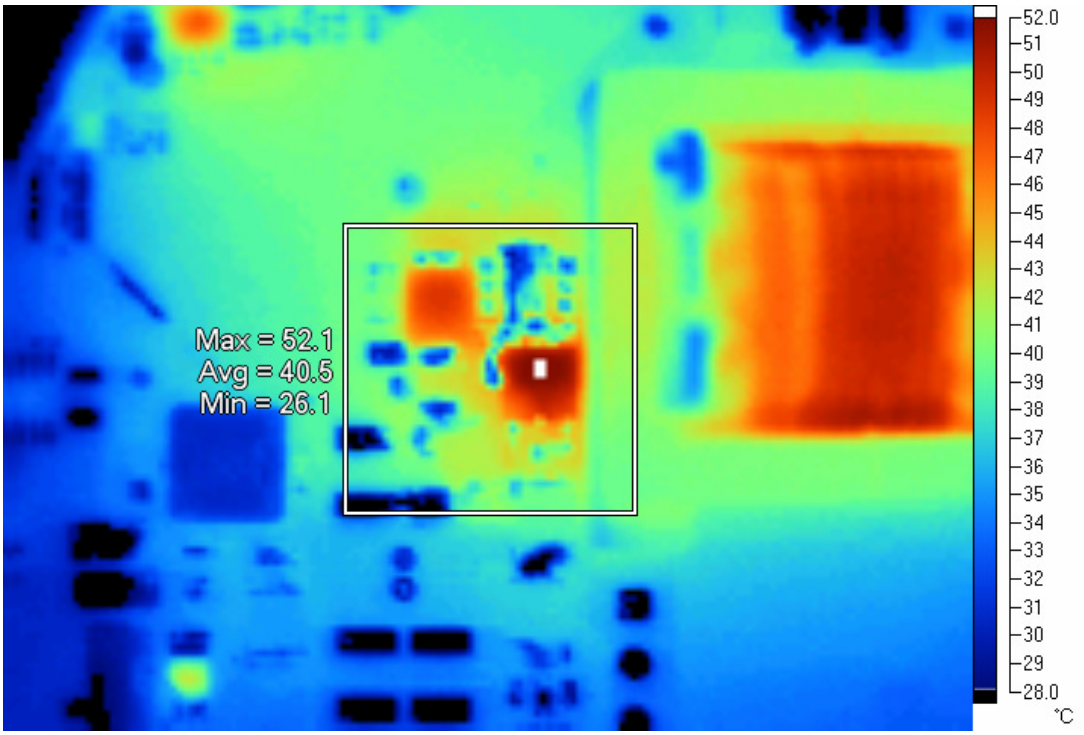


Figure 30. Thermal Image of Main Switch and Clamp

This thermal imaging shows that the two components with the highest loss in the circuit are the main switch and the inductor. It may be possible to reduce the loss in the switch by going to a lower voltage-rated device or paralleling an additional MOSFET.

4 Control

4.1 Need for Approximate Model

The charge-pumped reboost converter has many state variables for its transfer function:

- Input Leakage Inductor
- Output Leakage Inductor
- Magnetizing Inductor
- Pump Capacitor
- Clamp Capacitor
- Input Capacitor
- Output Capacitor

Each component theoretically adds another order to the transfer function. Despite this, the measured transfer function only shows a 2^{nd} order characteristic. It can be assumed that the leakage inductors are very small, so their effects occur at a frequency much higher than the switching frequency, and may be neglected. The pump and clamp capacitors may also be neglected in the frequency domain, their contribution is mostly as a dc-gain factor. The output capacitor should be large enough to be able to be replaced with a voltage-source for the frequency analysis. This leaves the magnetizing inductor and input capacitor as the key components of the model.

4.11 Inspiration for Model

The inspiration for the model comes from looking at the inductor current-waveform (Figure 31). The charge-pumped reboost (CPR) is almost identical to the tapped-boost waveform. The only difference is immediately after switch transitions.

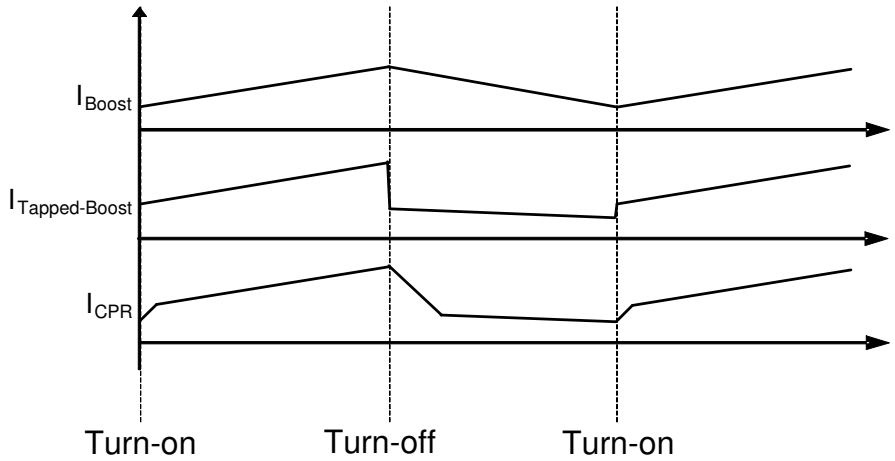


Figure 31. Input Current Ripple of Various Boost Topologies

This transient is caused by the leakage inductances, which are already assumed to be small enough to be negligible. Based on this fact, reducing the circuit to the tapped-

inductor boost equivalent and solving for the small-signal model should give a reasonably accurate solution.

4.2 Plant Model

Due to the presence of the charge-pump circuit, it is difficult to generate an averaged state-space model which is accurate over the full operating range. The transfer function can be approximated by a simpler tapped-boost converter of (Figure 32). This control-to-input model is determined in the same way as the control-to-output model of [20] by using modeling methods described in [21]. This approach neglects using a more advanced PV model from [22] since the real-world operating conditions are usually non-ideal and widely varied. A worst-case approximation can still be determined from the Thevenin-source model.

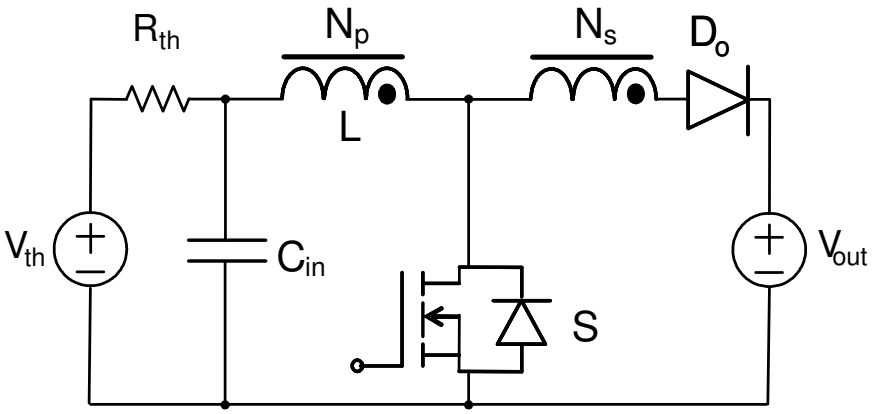


Figure 32. Tapped-Boost model for state-space transfer function derivation

This model represents the PV source as a Thevenin-equivalent circuit. There are two sub-cycles during operation, the first sub-cycle D is when the switch S is turned on, and the second sub-cycle D' is when the switch S is turned off.

D sub-cycle

$$C\frac{dv_c}{dt} = \frac{v_{in} - v_c}{R} - i_1$$

$$L\frac{di_1}{dt} = v_c$$

D' sub-cycle

$$C\frac{dv_c}{dt} = \frac{v_{in} - v_c}{R} - i_2$$

$$L_{eq}\frac{di_2}{dt} = v_c - v_{out}$$

$$i_1\frac{1}{(N+1)} = i_2$$

$$L_{eq} = (N+1)^2 L$$

By averaging these equations, we get:

$$C\frac{dv_c}{dt}=\frac{v_{in}-v_c}{R}-i_1 D-\left(i_1\frac{1}{(N+1)}\right)D'$$

$$D\,sub-cycle \Rightarrow \frac{di_1}{dt}=\frac{v_c}{L}$$
$$D'\,sub-cycle \Rightarrow \frac{di_1}{dt}=\frac{v_c(N+1)}{(N+1)^2 L}-\frac{v_{out}(N+1)}{(N+1)^2 L}=\frac{v_c}{(N+1)L}-\frac{v_{out}}{(N+1)L}$$
$$Averaged \Rightarrow \frac{di_1}{dt}=\frac{v_c}{L}D+\frac{v_c}{(N+1)L}D'-\frac{v_{out}}{(N+1)L}D'$$

After differentiating, the result is:

$$\frac{d\hat{v}_c}{dt}=\hat{v}_{in}\left(\frac{1}{RC}\right)-\hat{v}_c\left(\frac{1}{RC}\right)+\hat{d}\left(\frac{I_1}{(N+1)C}-\frac{I_1}{C}\right)-\hat{i}_1\left(\frac{D}{C}+\frac{1-D}{(N+1)C}\right)$$
$$\frac{d\hat{i}_1}{dt}=\left[\hat{v}_c\left(\frac{D}{L}+\frac{1-D}{(N+1)L}\right)+\hat{d}\left(\frac{V_c}{L}-\frac{V_c}{(N+1)L}+\frac{V_{out}}{(N+1)L}\right)-\hat{v}_{out}\left(\frac{1-D}{(N+1)L}\right)\right]$$

Then take the Laplace transform:

$$s\hat{v}_c=\hat{v}_{in}\left(\frac{1}{RC}\right)-\hat{v}_c\left(\frac{1}{RC}\right)+\hat{d}\left(\frac{I_1}{(N+1)C}-\frac{I_1}{C}\right)-\hat{i}_1\left(\frac{D}{C}+\frac{1-D}{(N+1)C}\right)$$
$$s\hat{i}_1=\left[\hat{v}_c\left(\frac{D}{L}+\frac{1-D}{(N+1)L}\right)+\hat{d}\left(\frac{V_c}{L}-\frac{V_c}{(N+1)L}+\frac{V_{out}}{(N+1)L}\right)-\hat{v}_{out}\left(\frac{1-D}{(N+1)L}\right)\right]$$

And then approximate:

$$\hat{v}_{out}=0$$
$$\hat{v}_{in}=0$$
$$s\hat{v}_c=-\hat{v}_c\left(\frac{1}{RC}\right)+\hat{d}\left(\frac{I_1}{(N+1)C}-\frac{I_1}{C}\right)-\hat{i}_1\left(\frac{D}{C}+\frac{1-D}{(N+1)C}\right)$$
$$s\hat{i}_1=\hat{v}_c\left(\frac{D}{L}+\frac{1-D}{(N+1)L}\right)+\hat{d}\left(\frac{V_c}{L}-\frac{V_c}{(N+1)L}+\frac{V_{out}}{(N+1)L}\right)$$

Then solve for the transfer-function of interest:

$$\frac{\hat{v}_c}{\hat{d}}=\frac{\left(s\left(\frac{-NI_1}{(N+1)C}\right)-\left(\frac{(V_cN+V_{out})(ND+1)}{(N+1)^2 LC}\right)\right)}{\left(s^2+s\left(\frac{1}{RC}\right)+\left(\frac{(ND+1)^2}{(N+1)^2 LC}\right)\right)}$$

Then modify this equation to account for the gain of the charge-pump circuit:

$$\frac{\hat{v}_c}{\hat{d}} = \frac{\left(s\left(\frac{-NI_1}{(N+1)C} \right) - \left(\frac{\left(V_c N + \left(V_{out} - \frac{V_c}{1-D} \right) \right)(ND+1)}{(N+1)^2 LC} \right) \right)}{\left(s^2 + s\left(\frac{1}{RC} \right) + \left(\frac{(ND+1)^2}{(N+1)^2 LC} \right) \right)}$$

4.3 Verification of Transfer Function

The transfer function can be measured with both the physical board and with simulation. The experimental data, simulated data, and mathematical model for three different source impedances are shown in (Figure 33), (Figure 34), and (Figure 35). This data shows that as the source impedance goes up, the quality-factor of the plant also increases. The quality-factor, or gain-peaking at the double pole, of the circuit should achieve its maximum theoretical value at the boundary between continuous-conduction mode and discontinuous-conduction mode of the inductor.

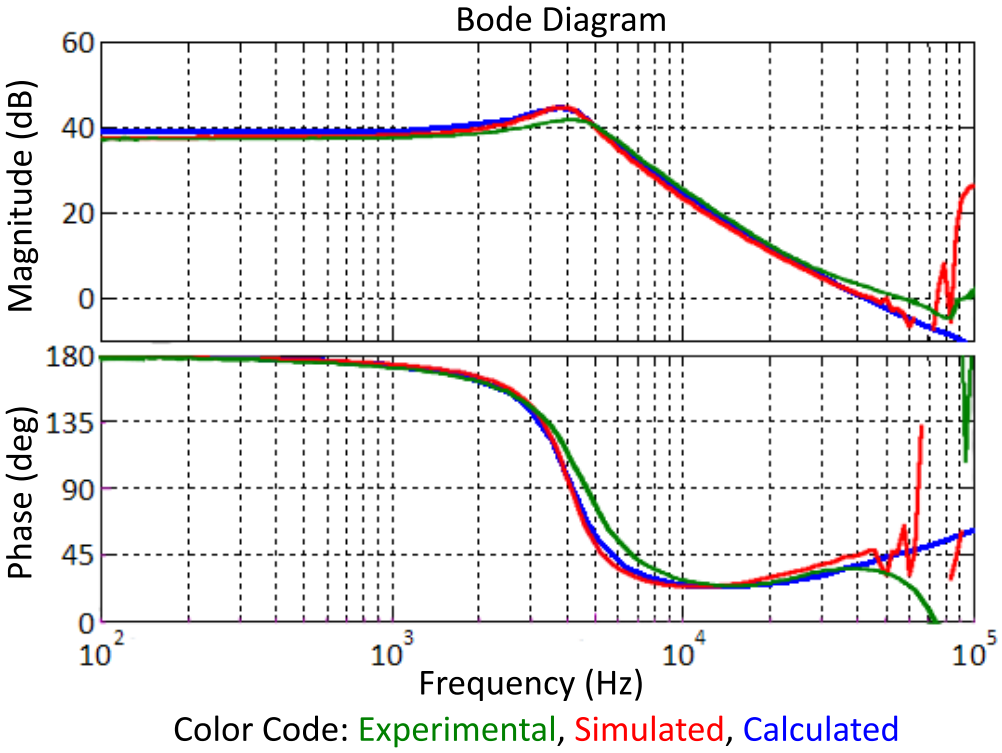


Figure 33. Frequency Response at 25 Vdc with Thevenin Resistance of 2.4Ω

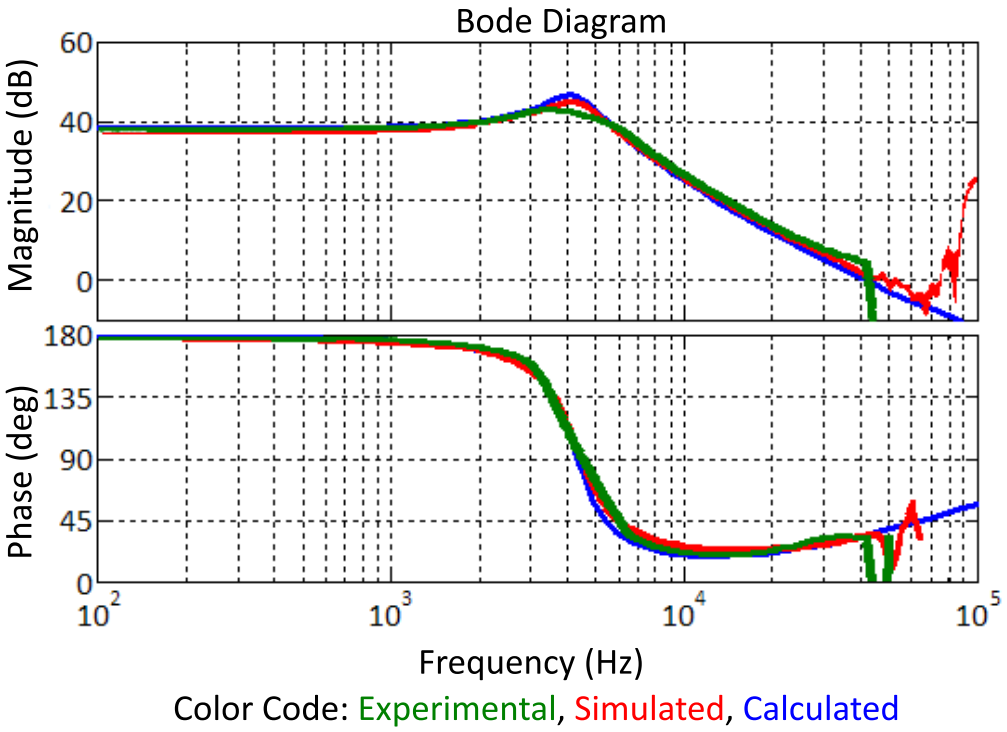


Figure 34. Frequency Response at 22 Vdc with Thevenin Resistance of 3.2Ω

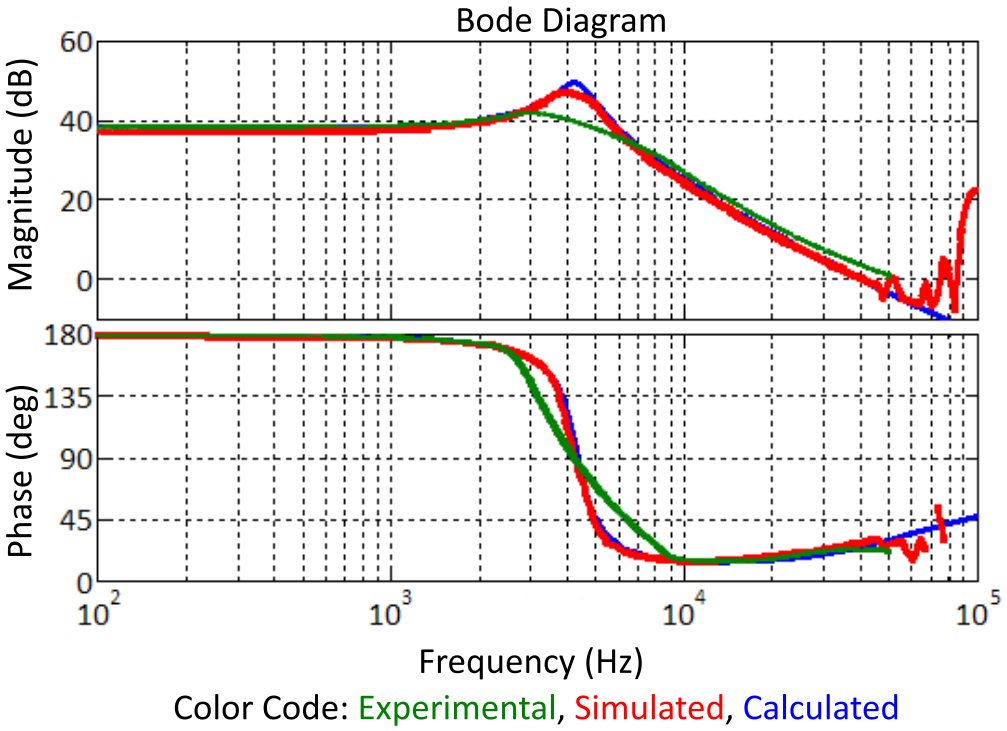


Figure 35. Frequency Response at 21.5Vdc with Thevenin Resistance of 4.5Ω

The model does not match as well as the operating point shifts to higher input voltages and the duty cycle decreases. The simulated data and mathematical model are shown for two higher operating points in (Figure 36) and (Figure 37).

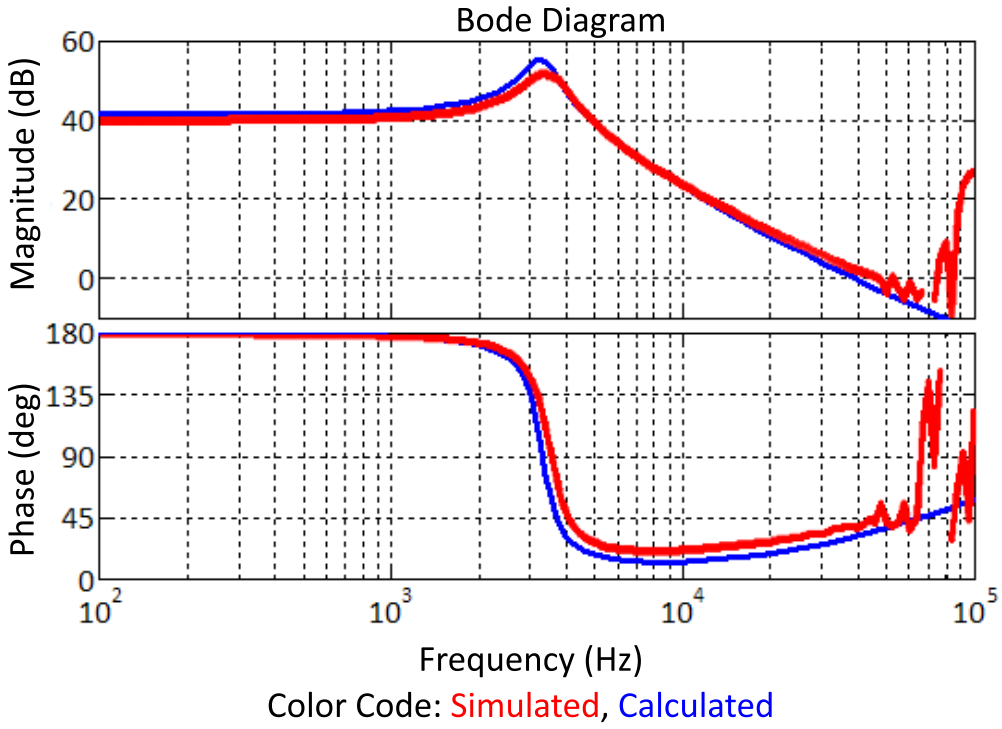


Figure 36. Frequency Response at 40 Vdc with Thevenin Resistance of 8Ω

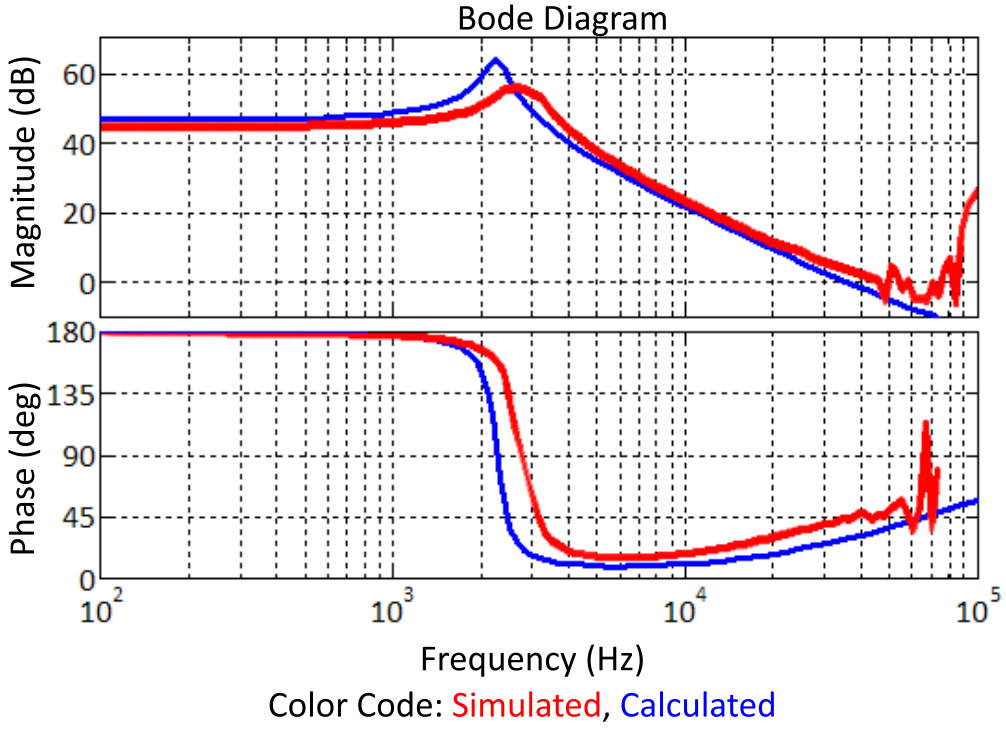


Figure 37. Frequency Response at 70 Vdc with Thevenin Resistance of 16.3Ω

4.4 Control Strategy

The proposed control structure is shown in (Figure 38). This includes a DC-AC stage as a load instead of a fixed voltage source. This control structure places emphasis on the operating voltage of the PV source in order to guarantee maximum power capture. The PV voltage is controlled because it is typically bounded over a smaller range than the PV current [23]. It eases the constraints on the MPPT loop by not requiring it to regulate the input current which can change abruptly during solar transients. By controlling the bus voltage, we guarantee power balance between the DC-DC stage and the DC-AC stage. This structure – omitting the voltage loop on the DC-DC stage – has been verified experimentally by [24]. The advantages of the voltage loop for reducing the ripple components at the output of the PV panel is shown in [25] which implements a system very similar to (Figure 38).

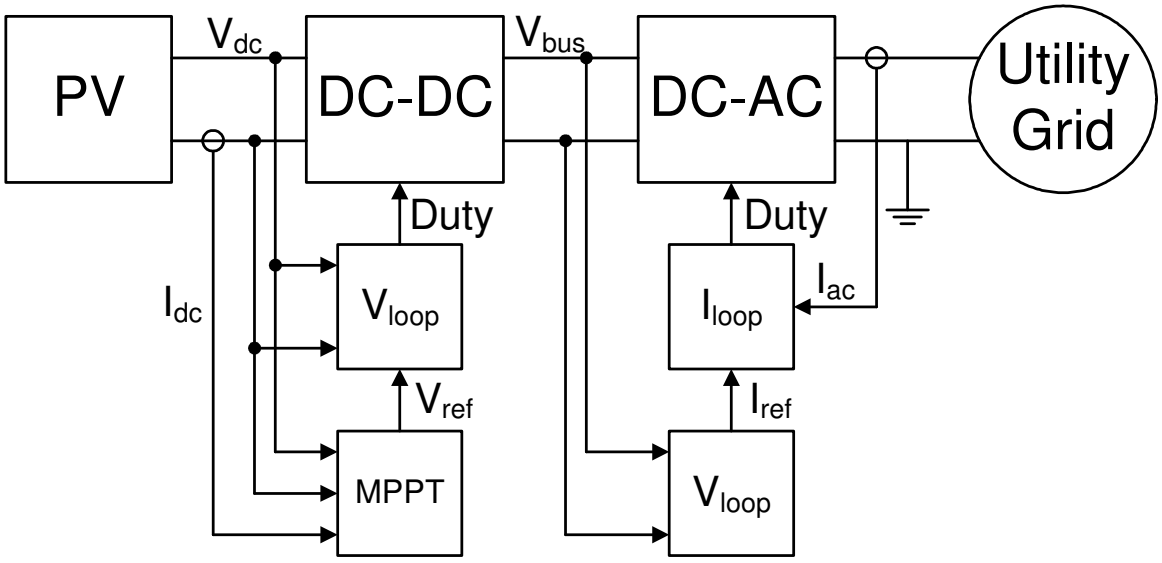


Figure 38. PV System Control Structure

This control structure is suitable for paralleling of any number of PV-connected DC-DC stages and connecting to any number of parallel DC-AC stages without affecting individual MPPT performance. This control structure is the best as it decouples the two stages and allows them to be designed individually.

An alternate configuration proposed in [26] does not sense the DC bus voltage at all. Instead, it assumes that the modulation index of the inverter can be sensed for free since it is internal to some digital controller. The outer voltage loop is then replaced by a peak-modulation-index controlling loop – this loop provides a current reference by regulating the peak duty cycle of the active devices of the inverter. This method has significant merit since it may improve the efficiency of a buck-type inverter by lowering the bus voltage slightly during periods where there is reduced power from the PV source.

4.41 DC-DC Voltage Loop

The transfer function in 4.2 shows that DC-DC plant is fairly easy to control. For testing, the analog compensator shown in (Figure 39) was used. The intent during testing was to have high-performance at a single operating point of 20 V_{dc} in, 200 V_{dc} out in order to test various MPPT algorithms. A digital controller implemented in an FPGA was not used due to problems encountered with limit-cycling due to insufficient PWM resolution. [27] was important in discovering these effects and finding ways to mitigate them, although ultimately an analog compensator yielded better performance. These digital effects could be reduced by using a method to achieve higher PWM resolution such as in [28]. The method given in the paper uses four high-frequency, phase-shifted clocks to generate an additional two-bits of PWM resolution.

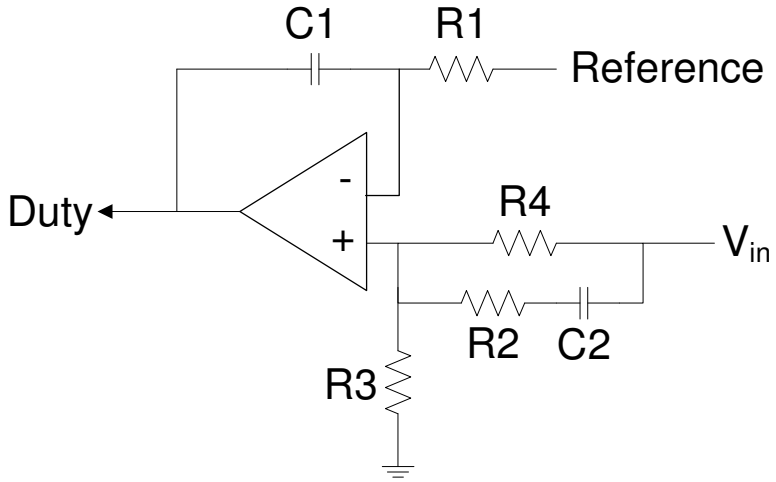


Figure 39. DC-DC Compensator

R1 = 818 R2 = 1 k R3 = 270 R4 = 51 k C1 = 0.1 uF C2 = 1 nF

$$TF = \left(\frac{1+sR_1C_1}{sR_1C_1}\right)\left(\frac{R_3}{R_3 + R_4 \parallel \left(R_2 + \frac{1}{sC_2}\right)}\right) \quad \Rightarrow \quad TF = K\left(\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s\left(1+\frac{s}{\omega_{p2}}\right)}\right)$$

$$K = \frac{R_3}{R_4 + R_3}\frac{1}{R_1C_1}$$

$$\omega_{z1} = \frac{1}{R_1C_1} \qquad \omega_{z2} = \frac{1}{C_2(R2+R4)}$$

$$\omega_{p1} = origin \qquad \omega_{p2} = \frac{R_3 + R_4}{C_2(R_2R_3 + R_3R_4 + R_2R_4)}$$

This compensator provides 2 poles and 2 zeros. At low frequency, C1 acts as an integrator, providing high DC gain to eliminate steady-state error. At high frequency, the compensator provides fixed gain since C1 acts as a short, and the op-amp operates as a voltage-follower. When the 2 pole, 2 zero compensator is combined with the 2 pole, 1 zero plant-model, this configuration provides a very large phase margin from 0 Hz up to half of the switching frequency.

The plant transfer function at low input voltage and full load is shown in (Figure 40); the compensator transfer function is shown in (Figure 41); the combined compensator and plant transfer function is shown in (Figure 42). The final loop has a cross-over frequency of 7.15 kHz with a phase margin of 70 degrees and infinite gain margin. The compensator transfer function includes the modulator gain of the analog PWM chip. As can be seen in (Figure 42), the gain at 120 Hz is roughly 20 dB, which can help attenuate any low-frequency ripple created by the inverter-load at the dc-bus.

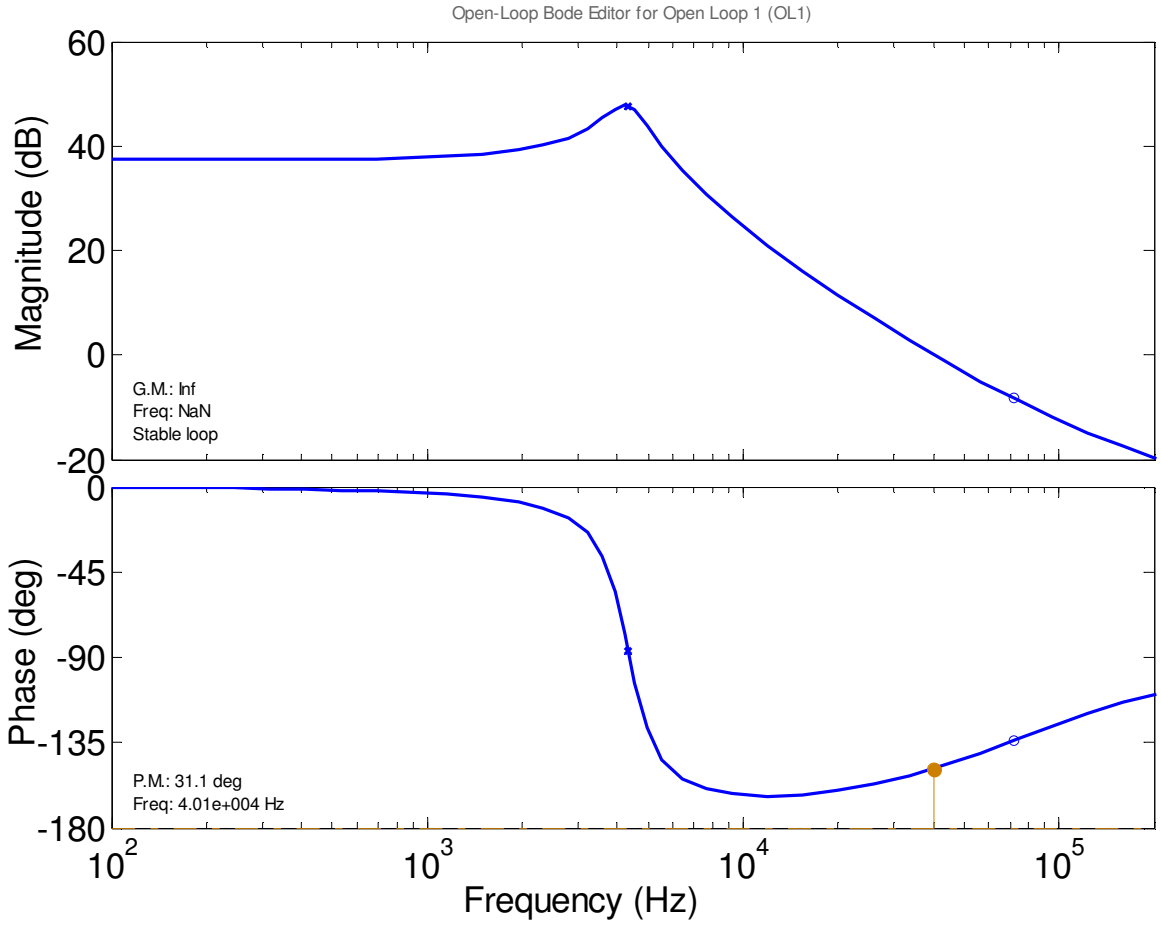


Figure 40. Plant Transfer Function

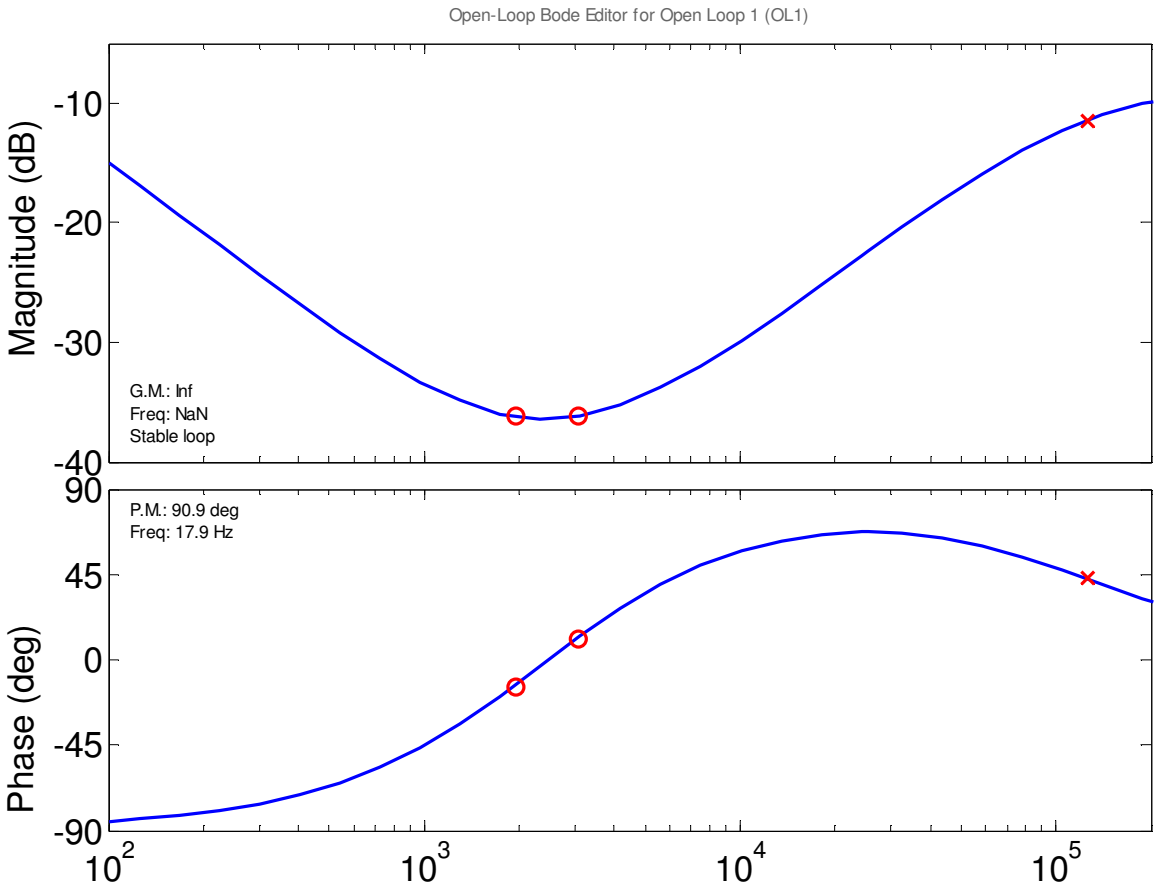


Figure 41. Compensator Transfer Function

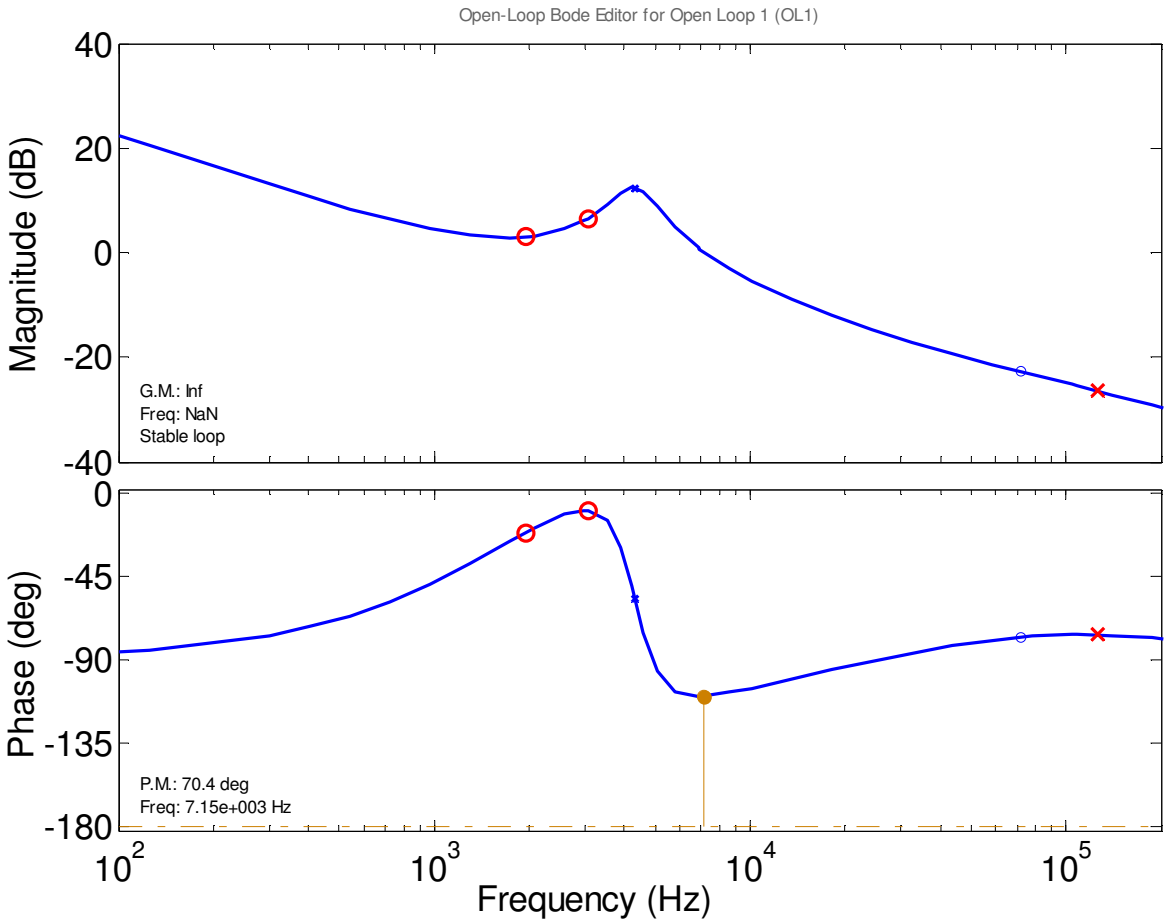
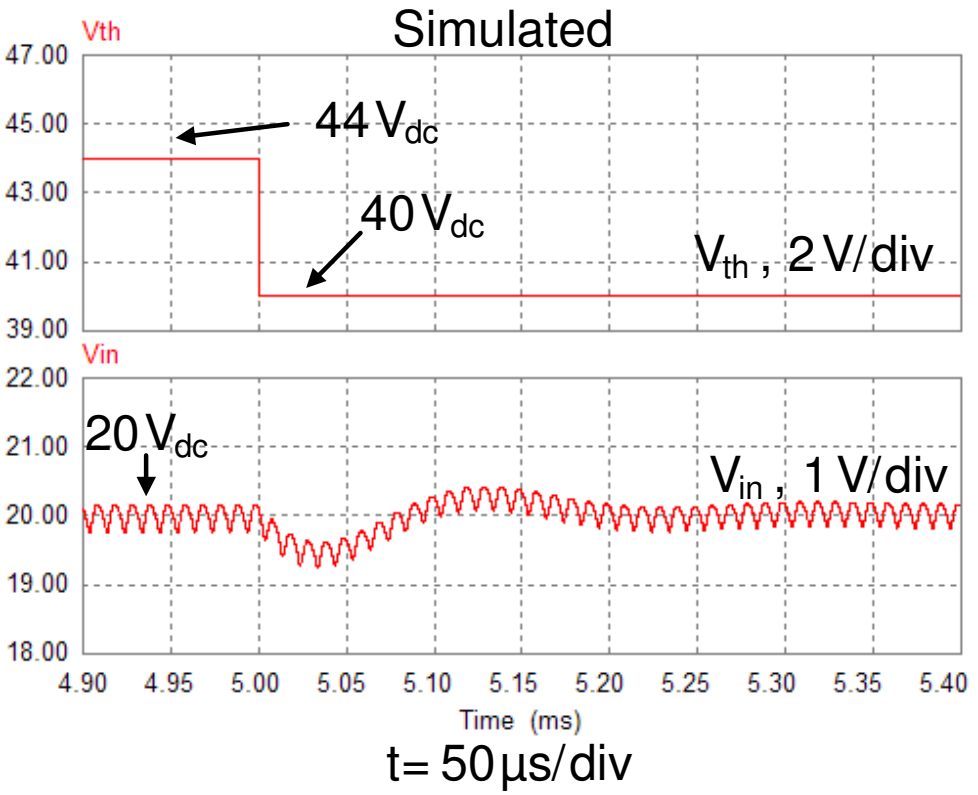


Figure 42. Combined Plant and Compensator Transfer Function

The compensator provides about 45 degrees of phase-boost at the cross-over frequency near 7 kHz. Transient response showing a thevenin-source voltage step is shown in (Figure 43). Transient response showing a 5 Volt reference step is shown in (Figure 44).



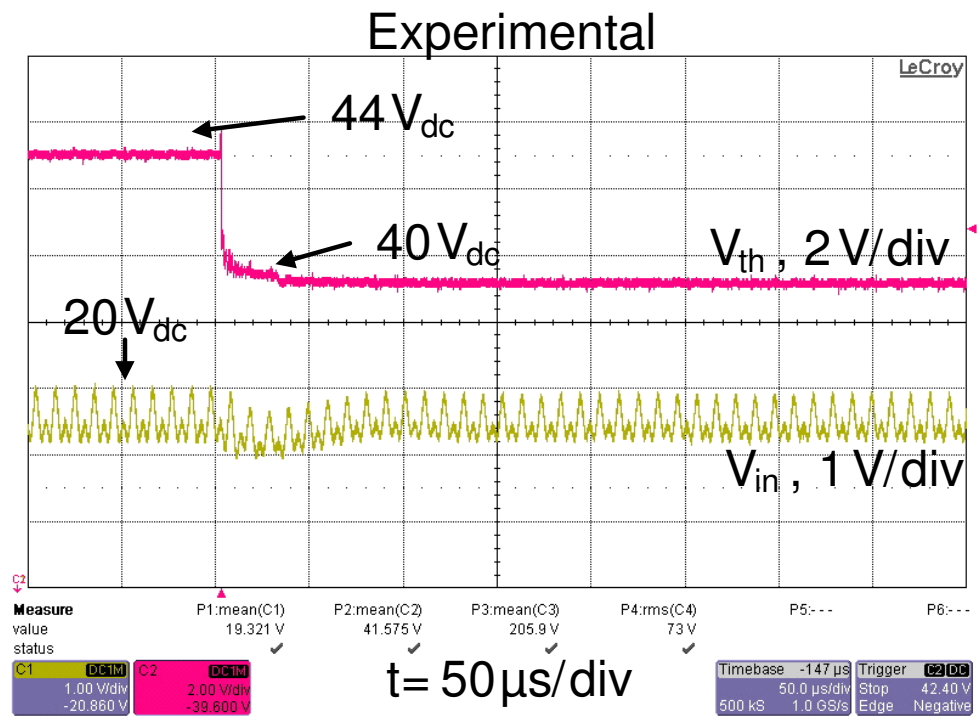


Figure 43. Source Voltage Step Response

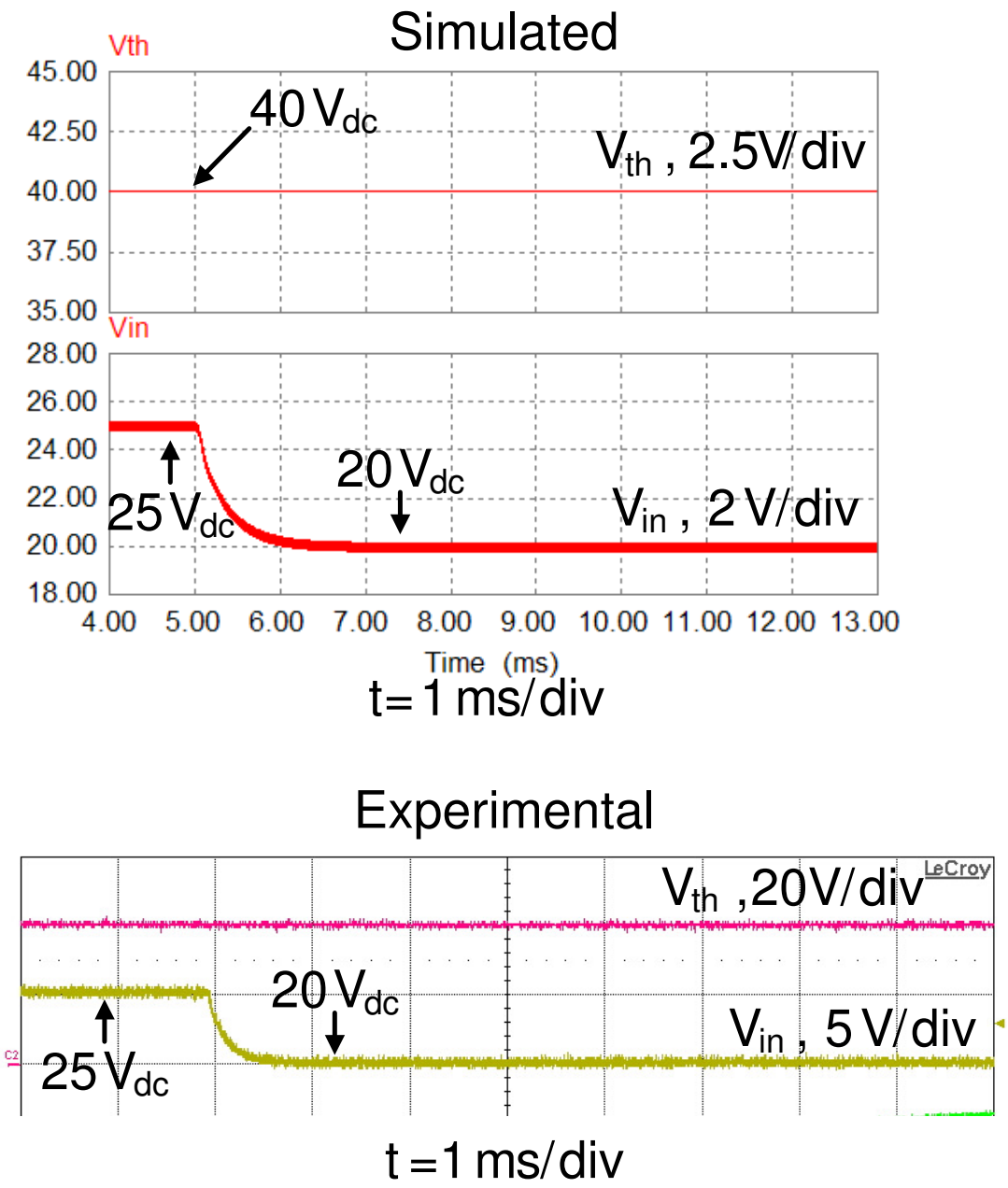


Figure 44. Reference Voltage Step Response

4.42 DC-DC MPPT Loop

The MPPT algorithm is shown in (Figure 45). It is similar to the Perturb & Observe (P&O) or the Hill-Climb methods. It is not guaranteed to track ideally in shaded conditions, as it may become stuck on a local maximum power point instead of the true global maximum power point.

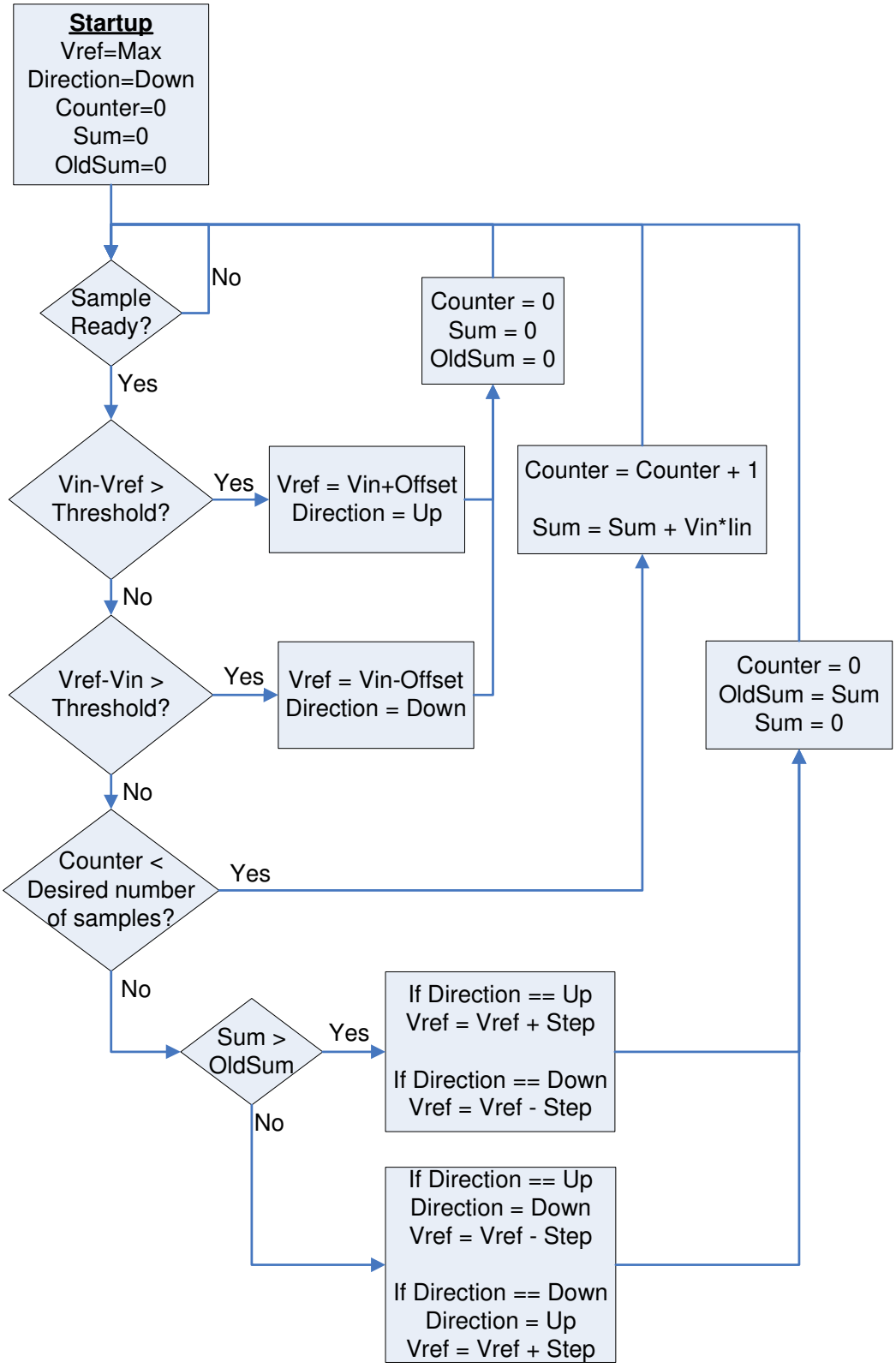


Figure 45. MPPT Algorithm

The PV panel used for testing, a Kyocera KD180GX-LP has specifications given in table 5 [29]. A single panel is used for all of the tests unless otherwise specified.

Maximum Power (Pmax)	180W
Maximum Power Voltage (Vmpp)	23.6V
Maximum Power Current (Impp)	7.63A
Open Circuit Voltage (Voc)	29.5V
Short Circuit Current (Isc)	8.35A
Number of Cells	48

Table 5

This implementation uses an over-sampling technique to improve the signal-to-noise ratio, and updates the reference on a period equivalent to 60Hz. There are approximately 8300 samples taken over a 16.7ms time period, about 5 samples per switching cycle. The reference step size is typically much smaller than the peak-to-peak voltage ripple across the input capacitor (Figure 46). The voltage ripple across the input capacitor is shown in detail in (Figure 47). Compared to [25], the MPPT step size with the algorithm of (Figure 45) is significantly smaller – 0.075V versus 1.3V, although the overall ripple is still similar at 1.15V versus 1.3V.

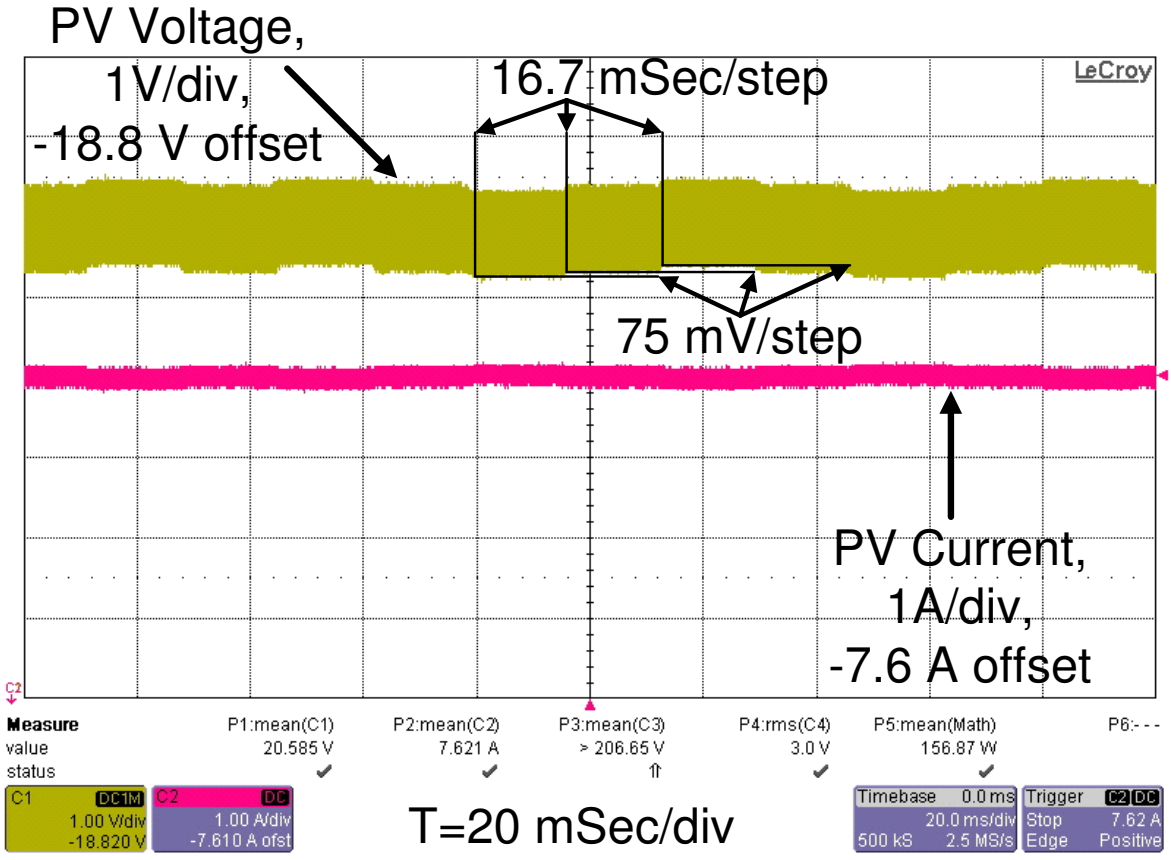


Figure 46. MPPT Limit-Cycling

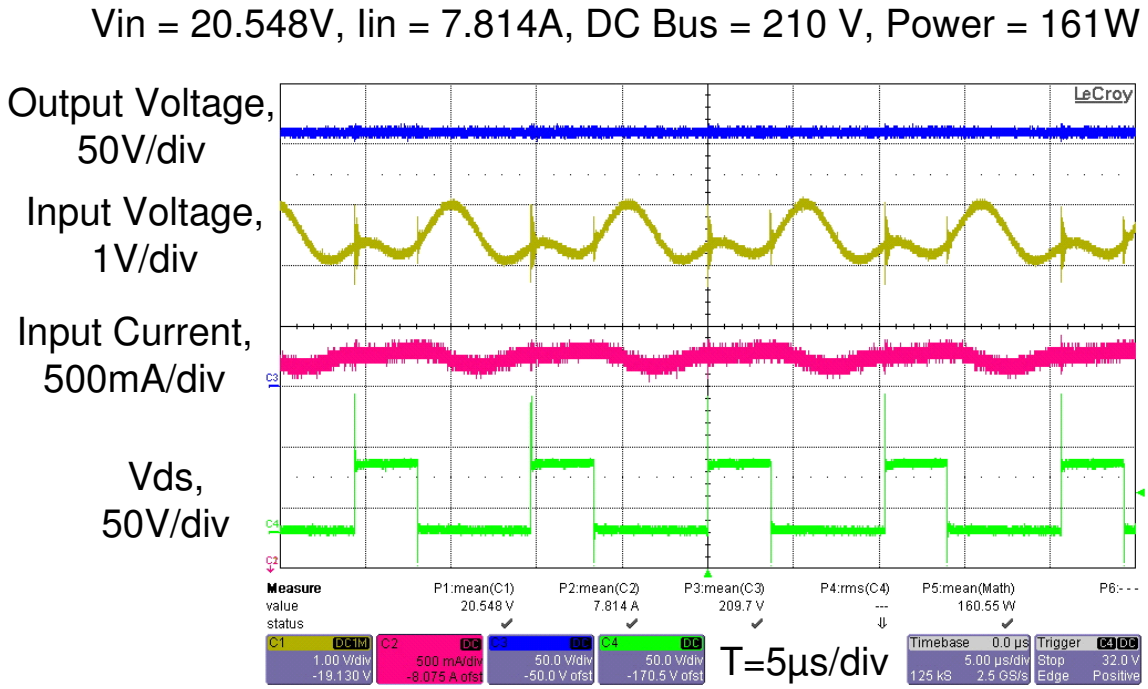


Figure 47. Input Voltage and Current Ripple

Since this is a guess-and-check algorithm and there may be fault conditions where the voltage-loop is disabled, the MPPT algorithm should be able to re-sync itself. This is accomplished through the threshold comparison, which determines if the reference and the sensed value are far out of synchronization. If they are out of sync, then the MPPT sets the reference equal to the measured value (plus some offset). This offset helps to guarantee PWM operation.

At startup or after a fault, if we set the reference equal to the open circuit voltage, the PWM duty cycle will be extremely small and the MPPT loop may not be able to track properly. By “offsetting” the reference slightly below the open-circuit voltage, we ensure that the duty cycle is of a significant value and that any change in the reference will be measurable. This is shown in the smooth start-up waveforms of (Figure 48). Similarly, if the converter begins to operate below the under-voltage lockout level and a fault occurs which turns off the PWM, the MPPT loop will sync to a level somewhere above the under-voltage lockout level.

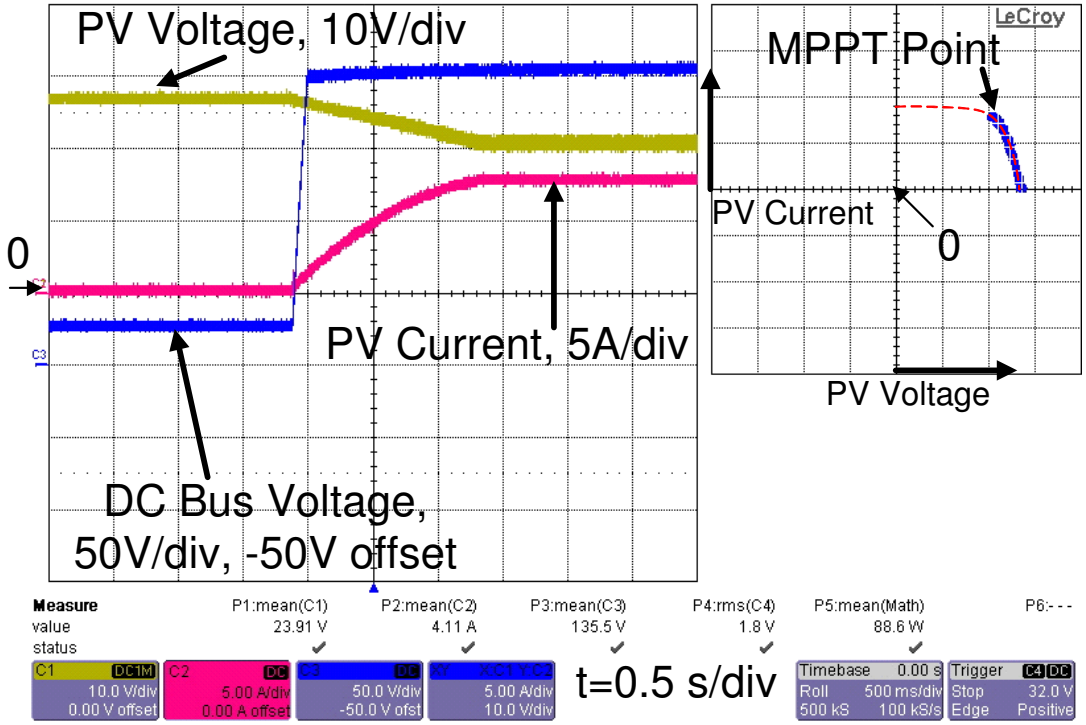


Figure 48. MPPT Startup

4.43 Considerations for use as part of a 2-stage Grid-Tied PV system

There are alternate ways to control this system. One of these is shown in (Figure 49). This configuration has been tested with hardware at the 300 W level where the instability at the MPP was discovered. It is not recommended to use this configuration. The droop-control method mentioned in [30] would be best to use in this arrangement, but its disadvantage is that the system cannot operate at the true maximum power point.

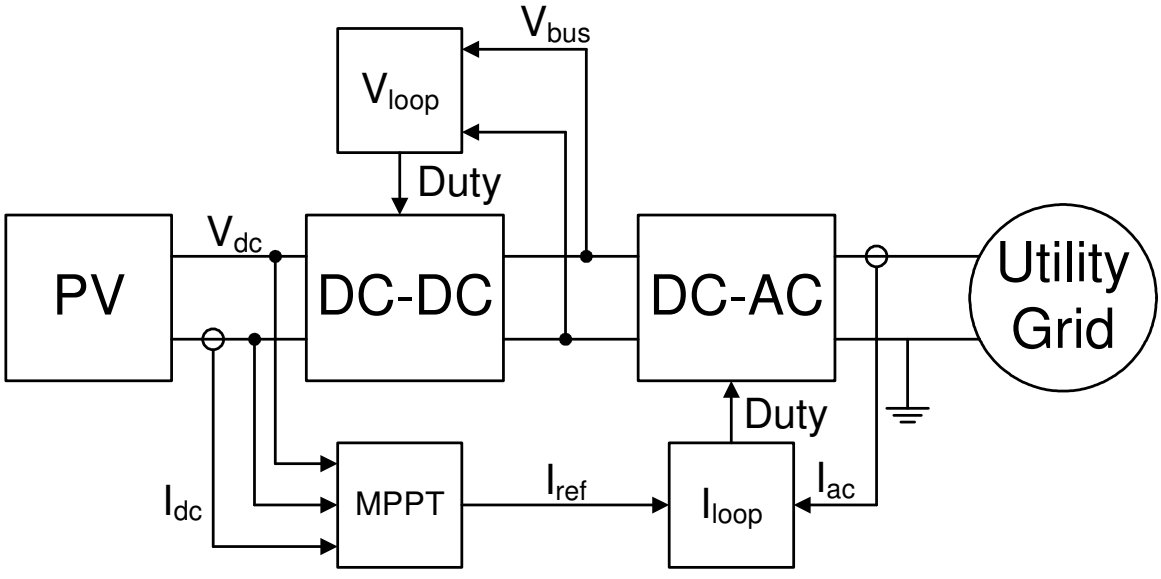


Figure 49. Unstable PV Control Structure

The problem arises in how the reference is commanded to the inverter. By giving a grid-current reference (assuming the grid-voltage is fixed) then the MPPT commands fixed power to the inverter. If that power command exceeds the maximum power available from the DC-DC converter and the PV source, then the DC-DC converter will run at the highest duty-cycle possible, which may act to latch the PV source into short-circuit operation if the duty-cycle is not limited. The voltage loop for the DC-DC stage will actually go into positive feedback once the input voltage is lower than the voltage of the maximum power point. This region is shown in (Figure 50).

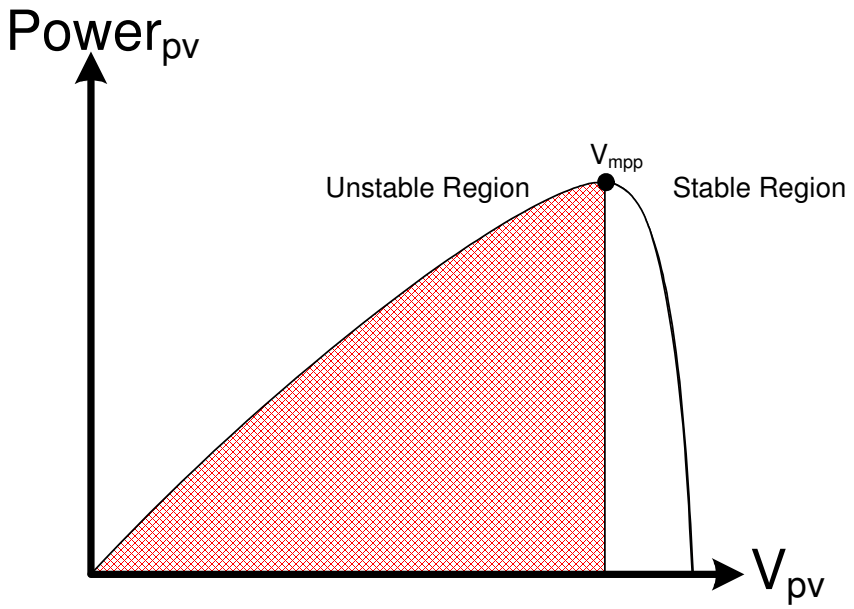


Figure 50. Unstable Control Structure Region

The only way for the system to recover is for the DC-AC to command zero power while the DC bus voltage recovers to the controlled value. This control structure is suitable for paralleling multiple DC-AC inverters, but not for paralleling multiple DC-DC stages. Regardless, this control structure should be avoided since it does not allow for operation at the true MPP. This instability is shown in (Figure 51). This test was done with two PV panels connected in series.

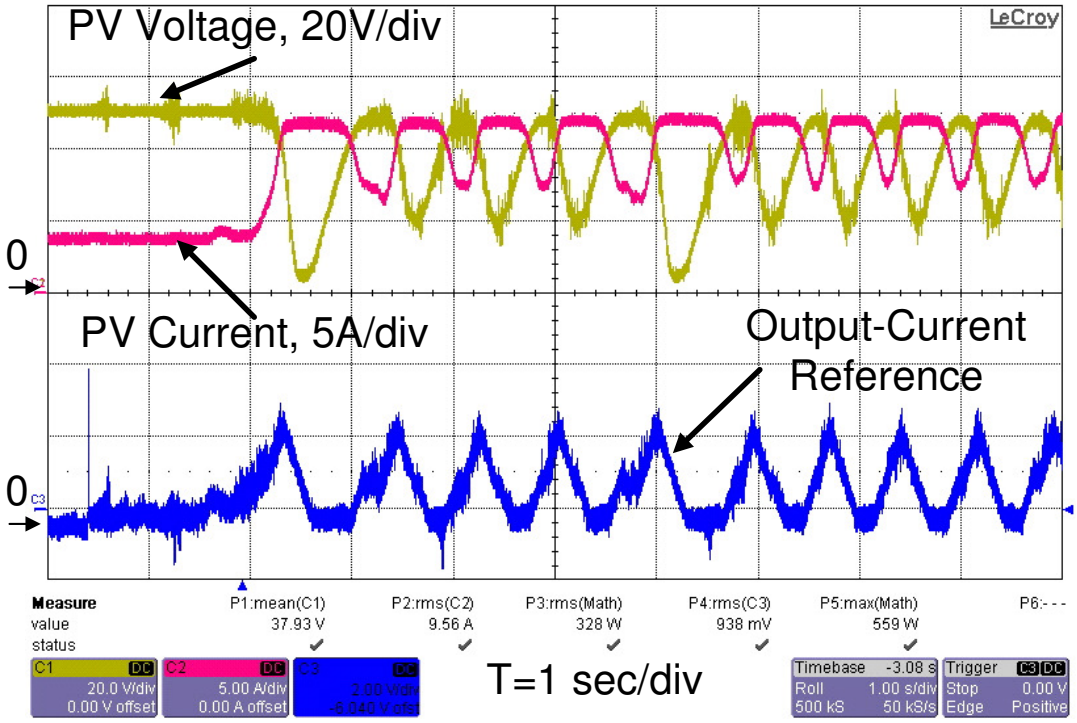


Figure 51. MPPT Instability

The result of this test showed that the array did not latch itself into a short-circuit state, but instead wound up oscillating around the maximum power point at an extremely low frequency – approximately 1.2 Hz.

Another control structure is shown in (Figure 52). This control structure has the DC-DC acting as a dc-transformer, stepping the PV voltage up or down as required. It avoids the instability of (Figure 49) since the addition of the bus-voltage loop results in power-balance between the DC-DC and DC-AC stages.

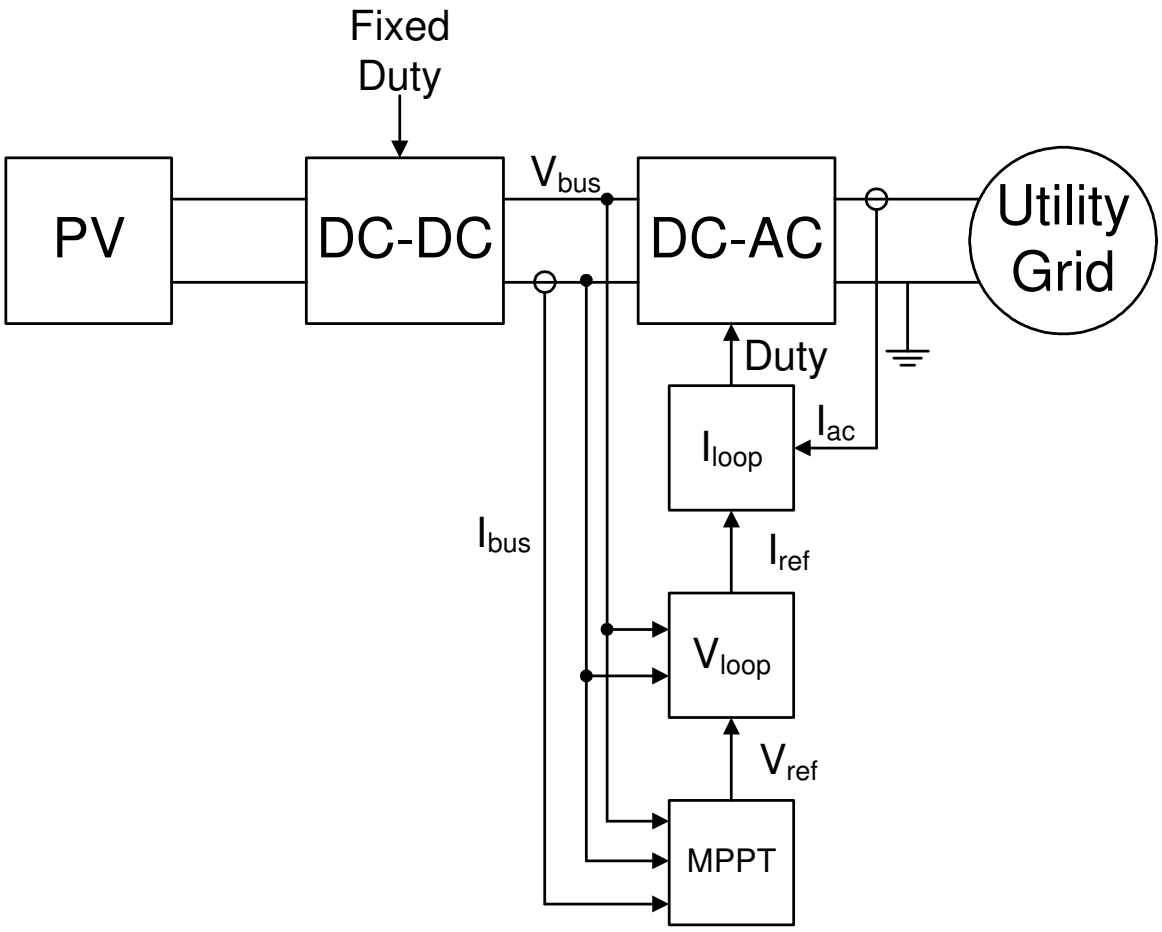


Figure 52. Simple Control Structure

If multiple DC-DC stages are used in parallel, it is impossible to guarantee maximum power capture from the PV sources since they are not being managed individually. In practice with the control structure of (Figure 52) it may be better to omit the DC-DC stage and use series- or parallel-connected PV sources tied directly to the DC bus.

4.5 Interaction with PV source

The PV source can have transients which are not always tracked properly by the MPPT algorithm due to their speed. For a very slow transient that shades a single cell as in (Figure 53), the MPPT algorithm has time to adjust to the new local maximum power point.

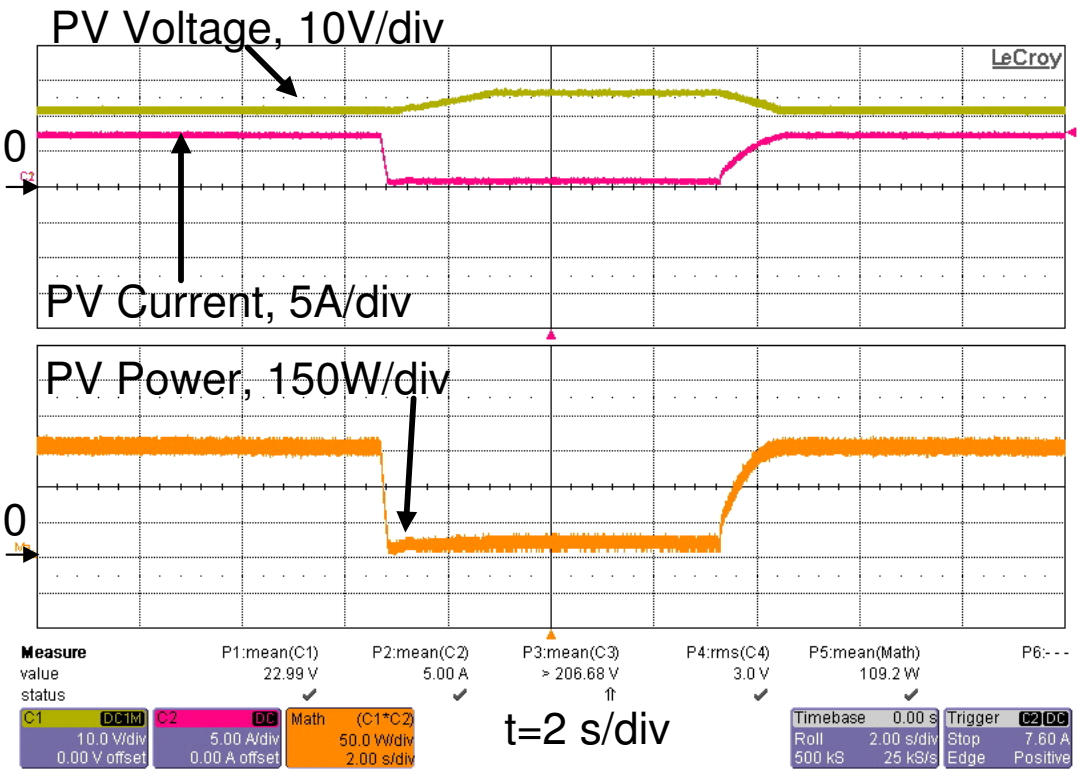


Figure 53. MPPT Single Cell Shadowing

Other transients which may not track properly include a moving shadow across a row of cells. This is shown in (Figure 54). The peaks in the current-waveform are from the shade moving from cell to cell. There are 8 cells in each row on the test PV panel, so subsequently there are 7 possible transitions – 7 peaks. Another way to look at it is that there are 8 valleys in the current-waveform. Since the input voltage cannot change very fast, there is insufficient time for the tracker to settle to the correct value. The same result occurs when the shadow accelerates across the cells as shown in (Figure 55). These transients could be improved by using a more advanced algorithm such as ripple-correlation control, which is proposed in [31]. Ripple-correlation control uses the switching ripple as the perturbation source, which allows for very fast determination of MPP direction and subsequently rapid approach towards local maxima.

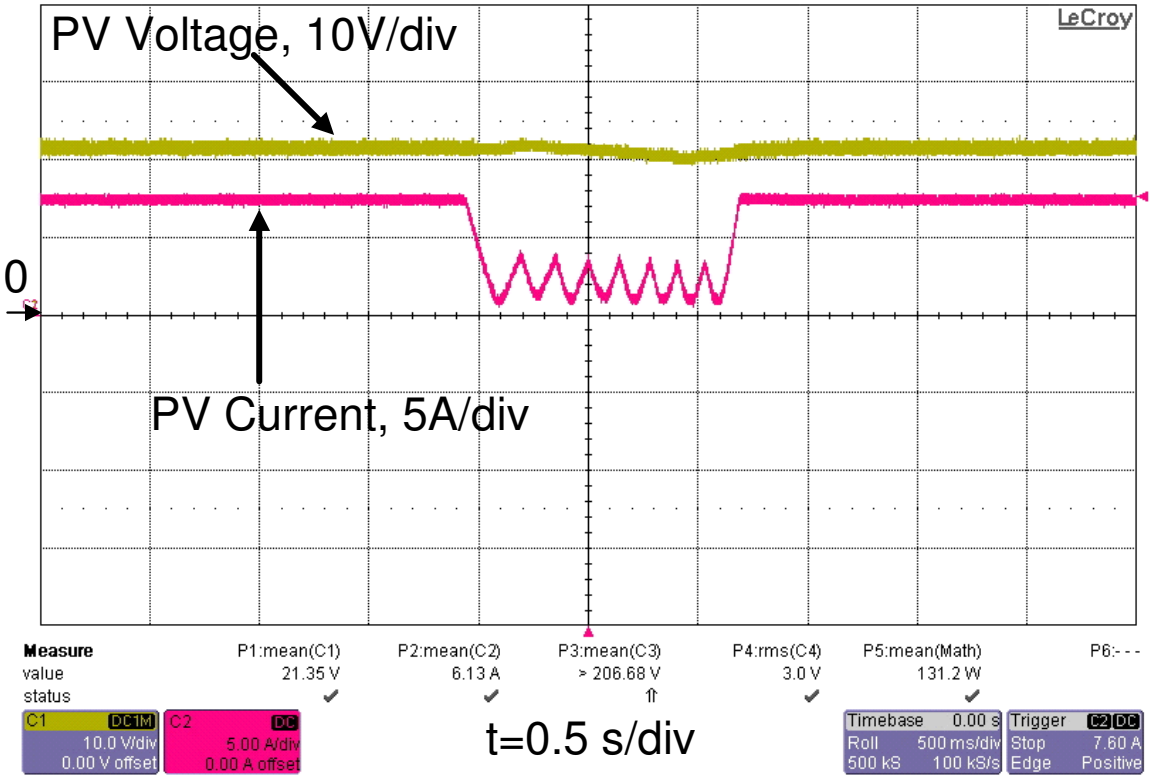


Figure 54. MPPT with Moving Shadow

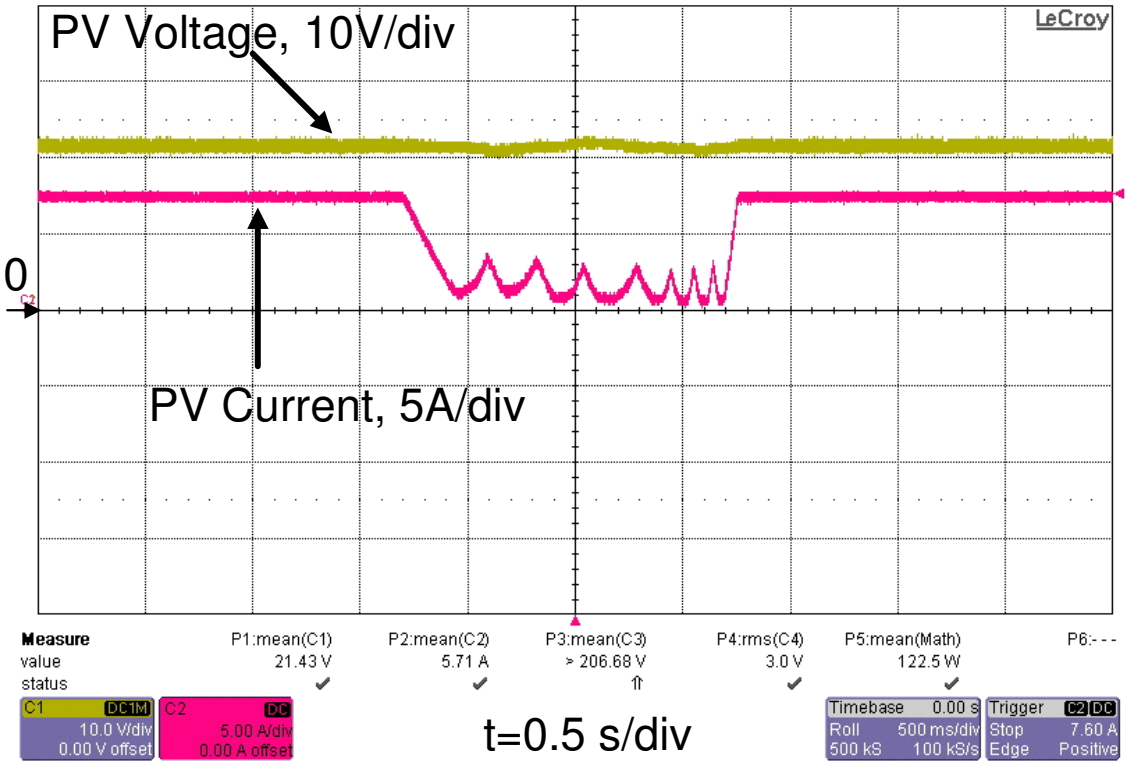


Figure 55. MPPT with Accelerating Shadow

If the shading event is slow enough, or has some sort of pause, then the MPPT algorithm can settle to the correct local maximum after some time. This is shown in (Figure 56).

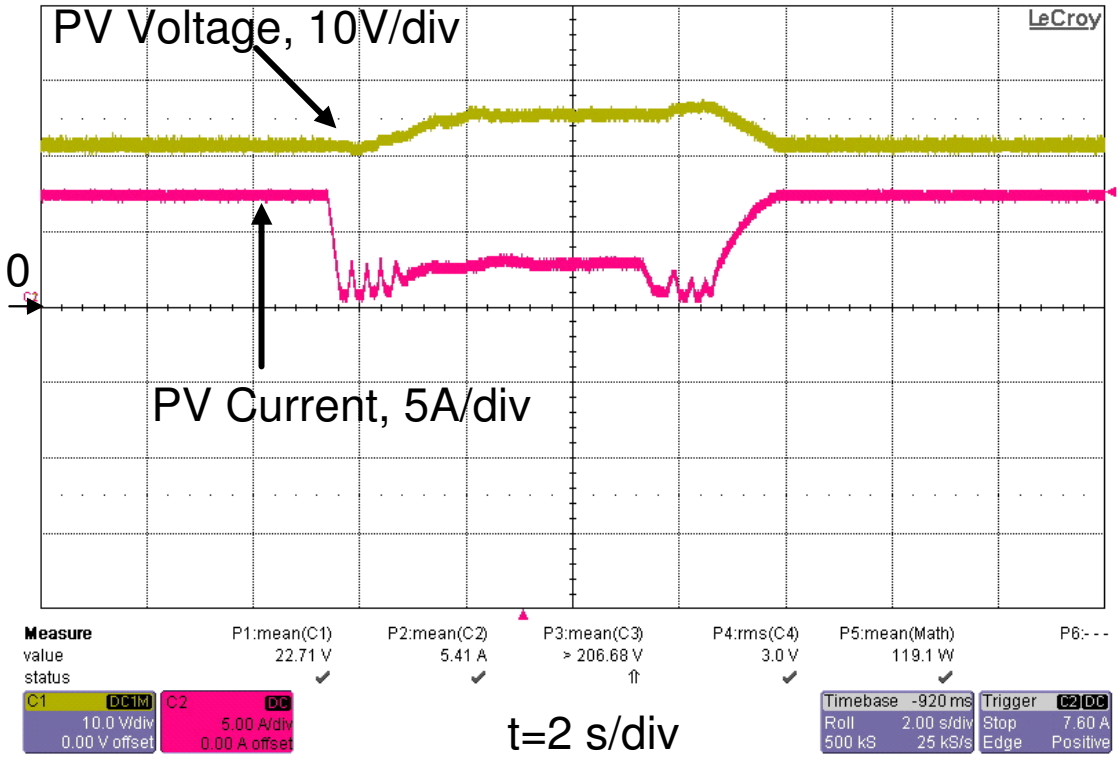


Figure 56. MPPT with Moving Shadow including pause

4.6 Effects of large dc bus ripple

By having the dc-dc converter control the PV operating point it is possible to reduce the effects of any rippling at its output. (Figure 57) shows how the converter can prevent the 20 $V_{pk\text{-}pk}$ ripple at the dc-bus from propagating back to the input. Even the small amount of low-frequency ripple which does reach the input of the converter has no effect on the MPPT performance. The majority of the ripple at the input is caused by the voltage-ripple across the small input-capacitor.

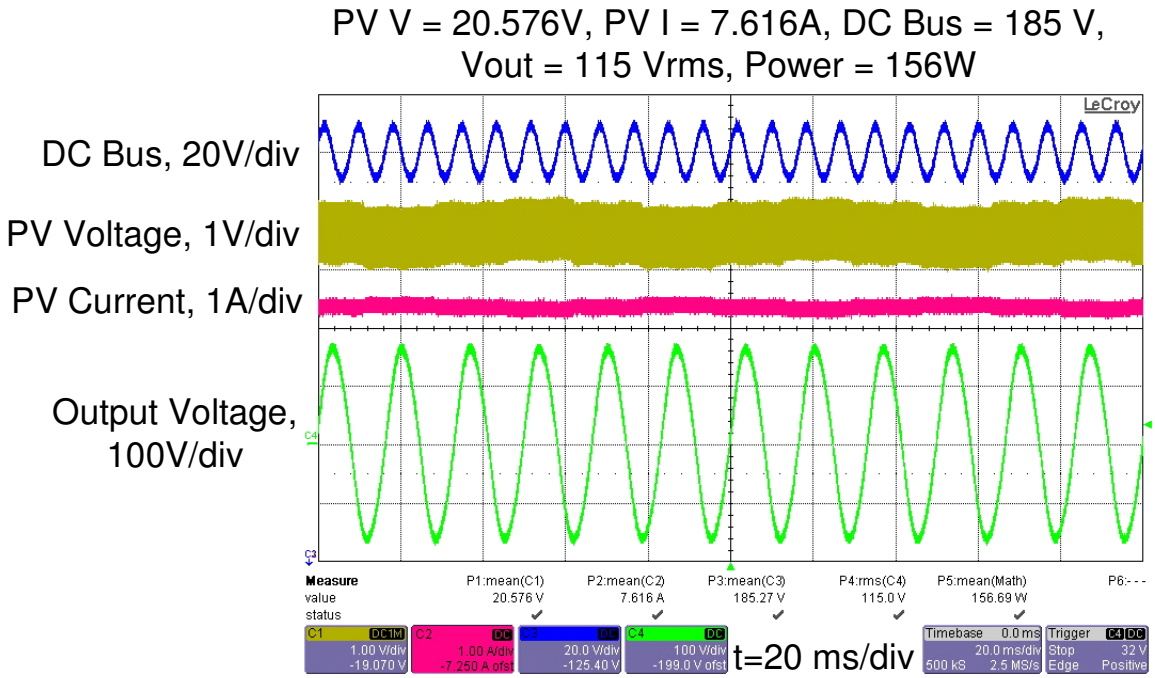


Figure 57. MPPT with DC Bus Ripple

Assuming a 27 dB gain at 120 Hz – this test used a more aggressive voltage-loop than shown in (Figure 42) – the ratio of low-frequency voltage ripple at the input of the converter due to ripple present at the bus is $\frac{V_{in-ripple}}{V_{out-ripple}} = \frac{V_{in-dc}}{V_{out-dc}} \frac{1}{10^{\left(\frac{Gain_{120Hz}}{20}\right)}} = \frac{20.5V_{dc}}{185V_{dc}} \frac{1}{22.38} = 0.00495$. With the peak-to-peak bus ripple voltage of 22 volts, we can expect the low-frequency ripple at the input to be 0.109 volts, which is about 0.5% of the input voltage.

In the above figure, there should be peak-to-peak 12 Hz ripple of 75mV * 2 = 0.15 volts due to the MPPT, peak-to-peak 120 Hz ripple of 0.109 volts due to the dc-bus ripple propagating back to the input, and peak-to-peak 100 kHz ripple of about 1 volt due to switching of the converter and the small input capacitor.

5 Photographs of DC-DC Board, PV Test Building, PV Test Configuration

The test board is shown in (Figure 58). The large blue capacitors in the middle are the dc-bus capacitors. The section to the left is the dc-dc stage; the section to the right is the dc-ac stage. The small board in the bottom left is the FPGA control board. The small adapter with the wireless antenna is a Bluetooth dongle used to provide isolation while commanding the board wirelessly via MATLAB – because sometimes power supplies do strange things. Originally, it was intended to have the dc-dc stage be two interleaved converter stages, but for this testing only one of them was used.

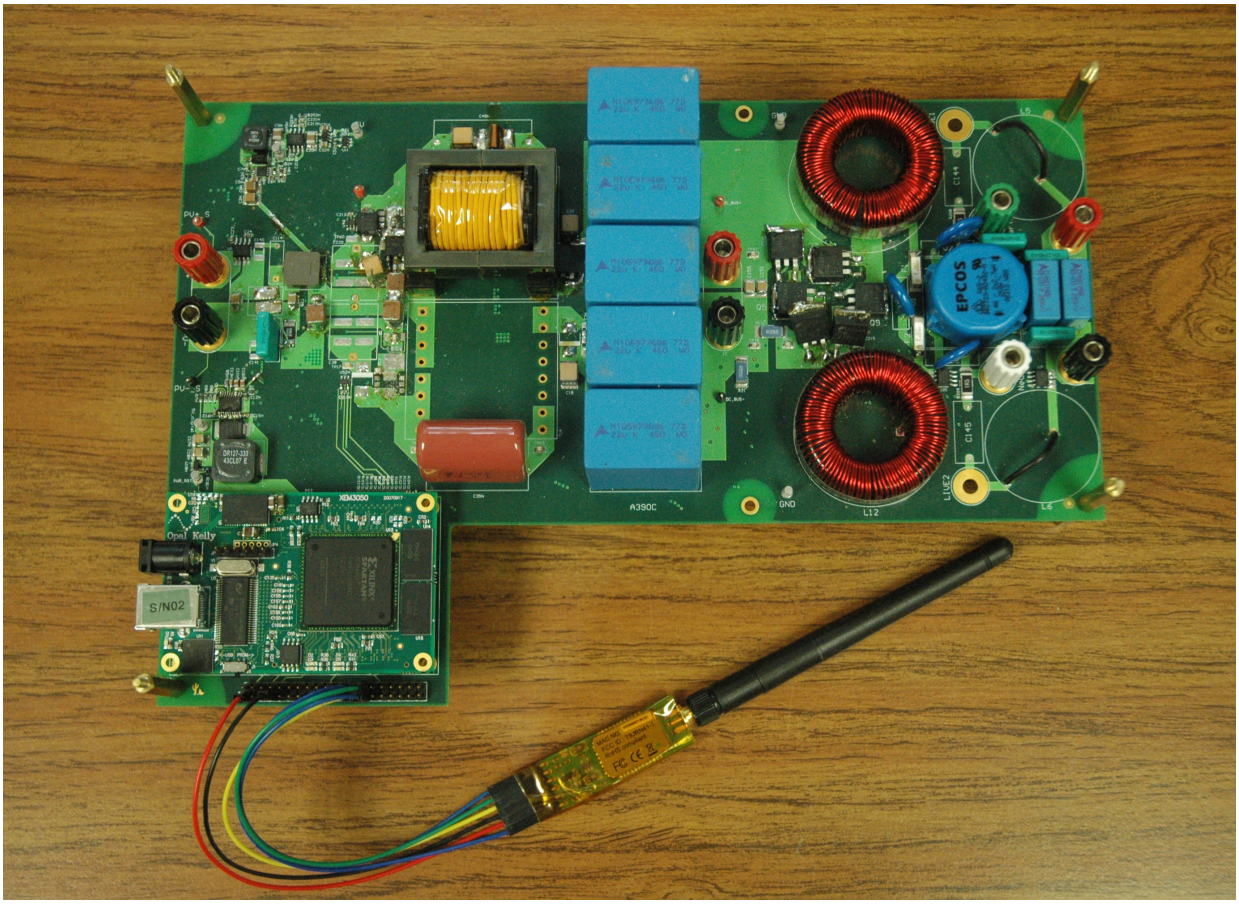


Figure 58. Microinverter picture

The test building is shown in (Figure 59). The array includes 6 panels, but only the bottom left panel was used for testing, since it's the easiest one to throw things on to in order to cause shading.

Figure 59. PV Test Building

The test setup is shown in (Figure 60). The input of the board was connected directly to a single PV panel, no auxiliary power supply was used. The DC-bus was connected through an additional diode to a 200V stack of lead-acid batteries. These batteries clamped the bus voltage and made things more convenient. The output of the inverter was connected to a resistor load bank in order to run stand-alone for testing.

Figure 60. PV Test Setup

6 Conclusions and Future Research Direction

This thesis shows the basic design and control of a high boost-ratio DC-DC converter. The disadvantages of several existing topologies have been shown as a motivation for the use of the charge-pumped reboost topology. The operating modes of the charge-pumped reboost converter have been detailed, along with guidelines for component selection. Certain transient-effects of the charge-pump and clamp circuit have been documented in order to make sure that the chosen devices can survive. High-peak efficiency of over 97% has been shown, which is greater than that of other state-of-the-art topologies. Thermal imaging shows that the majority of power-stage losses occur in the main switch and the flyback transformer when used in conjunction with a low-voltage PV panel. Finally, no electrolytic capacitors were used in the construction of the circuit.

The control methodology, although simple, achieves good power-capture from the PV source while mostly eliminating low-frequency ripple. The proposed small-signal model is very accurate for low input-voltages, but it has accuracy error as the input-voltage increases. A high-bandwidth voltage loop can be easily implemented in analog which allows fast transient response and good low-frequency ripple rejection. By including this voltage loop, almost any MPPT algorithm can be used. Over-sampling of the input voltage and current allow accurate hill-climb MPPT operation even with significant high-frequency ripple. Although there are certain dynamic performance issues with a slow hill-climb MPPT algorithm, it still gives very good steady-state performance.

Future Research:

- A detailed loss analysis of the charge-pumped reboost topology in order to reach higher efficiency,
- Investigating alternate PWM control methods to reduce switching stress on active devices,
- Modifying the topology to permit higher output voltage,
- Implementing more advanced MPPT controllers to improve dynamic response to changing weather conditions,
- Modeling of the interaction between the DC-DC stage and the DC-AC stage of a grid-tied system,
- And design and control of a suitable DC-AC stage for use in this grid-tied system.

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