

PCB-Based Heterogeneous Integration of PFC/Inverter

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Abstract

State-of-the-art silicon-based power supplies have reached a point of maturity in performance. Efficiency, power density, and cost are major trade-offs involved in further improvements. Most products are custom designed with significant non-recurrent engineering and manufacturing processes that are labor intensive. In particular, conventional magnetic components, including transformers and inductors, have largely remained the same for the past five decades. Those large and bulky magnetic components are major roadblocks toward an automated manufacturing process. In addition, there is no specific approach to reduce electromagnetic interference (EMI) in conventional practices. In certain cases, EMI filter design even requires a trial-and-error process.

With recent advances in wide-bandgap (WBG) power semiconductor devices, namely, SiC and GaN, we have witnessed significant improvements in efficiency and power density, compared to their silicon counterparts. In a power factor correction (PFC) rectifier/inverter, the totem-pole configuration with critical conduction mode (CRM) operation to realize zero-voltage switching (ZVS) is deemed most desirable for a switching frequency 10 times higher than current practice. With a significantly higher operating frequency, the integration of inductors with embedded windings in the printed circuit board (PCB) is feasible.

However, a PCB winding-based inductor has a fundamental limitation in terms of its power handling capability. The winding loss is proportional to the magnetomotive force (MMF), which

is Ni . That is to say, with the number of layers (turns) and currents increased, winding loss is increased nonlinearly. Furthermore, for a large-size planar inductor, flux distribution is usually non-uniform, resulting in dramatically increased hysteresis loss and eddy loss in a magnetic core. Thus, current designs are challenged by the capability of extending to a higher power range. To address those issues, a modular building block approach is proposed in this dissertation. A planar PCB inductor is formed by an array of pillars that are integrated into one magnetic core, where each pillar handles roughly 750 W of power. The winding loss is reduced by limiting the number of turns for each pillar. The core loss is minimized with a proposed planar magnetic structure where rather uniformly distributed fluxes were observed in the plates. The proposed approach has a similar loss to a conventional litz wire-based design but features a higher power density and can be easily assembled in automation. A 3 kW high frequency PFC converter with 99% efficiency is demonstrated as an example. Furthermore, PCB-based designs up to 6 kW are provided.

Another challenge in a WBG-based PFC/inverter is the high common-mode (CM) noises associated with the high dv/dt of the WBG devices. Symmetry and cancellation techniques are often employed to suppress CM noises in switching power converters. Meanwhile, shielding technique has been demonstrated to effectively suppress CM noises in an isolated converter with PCB-based transformer design. However, for non-isolated converters, such as PFC circuits, none of the techniques mentioned above are deemed applicable or justifiable. Recently, the balance technique has been demonstrated to effectively suppress CM noises up to a point where the parasitic ringing between the inductor and its winding capacitor is observed. This dissertation presents an improved balance technique in a PCB-based coupled inductor design that compensates for the detrimental effect of the interwinding capacitors. A CM noise model is established to simplify the convoluted couplings into a decoupled representation so as to illustrate the necessary

conditions for realizing a balanced network. In the given 1 kW PFC example, CM noise suppression is effective in the frequency range of interest up to 30 MHz. The parasitic oscillation of inductors, known to be detrimental for CM noise reduction, is circumvented with the improved magnetic structure.

By applying the balance technique to a PFC converter and the shielding technique to an LLC DC/DC converter, significant noise reductions were realized. This provides the opportunity to use a simple one-stage EMI filter to achieve the required EMI noise attenuation for a server power supply. This dissertation further offers an in-depth study on reducing the unwanted near-field couplings between the CM/DM inductors and DM filter capacitors, as well as unwanted self-parasitics such as the ESL of the DM capacitors. An exhaustive finite element analysis (FEA) and near field measurements are conducted to better understand the effect of frequency on the polarization of the near field due to the displacement current. The knowledge gained in this study enables one to minimize unwanted mutual coupling effects by means of physical placement of these filter components. Thus, for the first time, a single-stage EMI filter is demonstrated to meet the EMI standard in an off-line 1 kW, 12 V server power supply.

With the academic contributions in this dissertation, a PCB winding-based inductor can be successfully applied to a high-frequency PFC/inverter to achieve high efficiency, high power density, automation in manufacturing, lower EMI, and lower cost. Suffice it to say, the proposed approach enables a paradigm shift in the designing and manufacturing of a PFC/inverter for the next generation of power supplies.

PCB-Based Heterogeneous Integration of PFC/Inverter

Shuo Wang

General Audience Abstract

The current switching power supplies with silicon devices have reached a point of maturity in performance. Efficiency, power density, and cost are major trade-offs involved in performance improvements. Most products are custom designed, requiring significant non-recurrent engineering and labor-intensive manufacturing processes. In particular, conventional magnetic components, including transformers and inductors, have largely remained the same for the past five decades. Those large and bulky magnetic components are one of the major roadblocks toward an automated manufacturing. In addition, switching power converters can generate electromagnetic interference (EMI) noises, which could potentially impact the normal operations of other equipment and devices if not properly addressed. The conventional approach to mitigating EMI noises is to adopt a multi-stage EMI filter at the front-end. The filter, however, occupies 1/4-1/3 of the total converter volume in general and significantly increases the size of the converter.

With recent advances in wide-bandgap (WBG) power semiconductor devices, namely, SiC and GaN, we have witnessed significant improvements in efficiency and remarkable reductions in size, compared to their silicon counterparts. With GaN devices, the switching frequency of a PFC converter is able to be increased by 10 times without compromising efficiency. With a significantly higher operating frequency, the integration of inductors with embedded windings in printed circuit board (PCB) is feasible. The challenges and opportunities in facilitating automated manufacturing and minimizing EMI noises by using PCB-based magnetics are discussed in this dissertation.

The first challenge is the dramatically increased winding and core losses at high powers for a PCB winding-based inductor. To address this issue, a modular building block approach is proposed. A planar PCB inductor is formed by an array of pillars that are integrated into one magnetic core, where each pillar handles roughly 750 W of power. The winding loss is reduced by limiting the number of turns for each pillar. The core loss is minimized with a proposed planar magnetic structure where rather uniformly distributed fluxes have been observed in the magnetic core plates. A 3 kW high-frequency PFC converter with a 99% peak efficiency is demonstrated as an example. Furthermore, PCB-based designs up to 6 kW are provided.

Another challenge in a WBG-based PFC/inverter is the high common-mode (CM) noises caused by the high switching speed of the WBG devices. The balance technique has been demonstrated to effectively suppress CM noises up to several MHz. However, the CM noise reduction is not effective beyond that. This dissertation presents an improved balance technique in a PCB-based coupled inductor to circumvent the limits. In the given 1 kW PFC example, CM noise suppression is effective in the frequency range of interest up to 30 MHz.

With the above-mentioned efforts in minimizing EMI noises, significant noise reductions were realized. This provides the opportunity to use a simple one-stage EMI filter to achieve the required EMI noise attenuation for a server power supply. It features a smaller volume compared to a conventional multi-stage filter. To further enhance the filter's performance at high frequencies, an exhaustive finite element analysis and near field measurements are conducted to better understand the effect of frequency on the polarization of the near field due to the displacement current. The knowledge gained in this study enables one to minimize unwanted mutual coupling effects through physical placement of these filter components. Several approaches for improving the filter performance at high frequency are conducted. With these approaches applied, a single-stage filter

is demonstrated in an off-line 1 kW, 12 V server power supply. Thus, for the first time, a single-stage EMI filter can be contemplated to meet the EMI standard in server power supplies.

With the academic contributions in this dissertation, a PCB-winding based inductor can be successfully applied to a high-frequency PFC/inverter to achieve high efficiency, high power density, automation in manufacturing, lower EMI, and lower cost. Suffice it to say, the proposed approach in this work enables a paradigm shift in the designing and manufacturing of a PFC/inverter for the next generation of power supplies.

To my Family

My parents: Shizhong Wang and Jianlan Zhuang

My sister: Hongmei Wang

My fiancée: Ruixuan Wang

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Chapter 1 Introduction

1.1 State-of-the-Art Power Supply and Challenges

With the advancement of information and transportation technologies, the energy consumption in electric vehicles (EVs), data centers, networks, and consumer devices continues increasing in the decades of 2010s and 2020s, as illustrated in Fig. 1.1. Particularly, in 2030, the total energy consumption in data centers and networks alone is projected to reach 6300 TWh, which is equivalent to the power generation of 900 nuclear power plants, with a capacity of 7 TWh per plant. It should be noted that Fig. 1.1 is a reproduction of the data provided in [1]-[2].

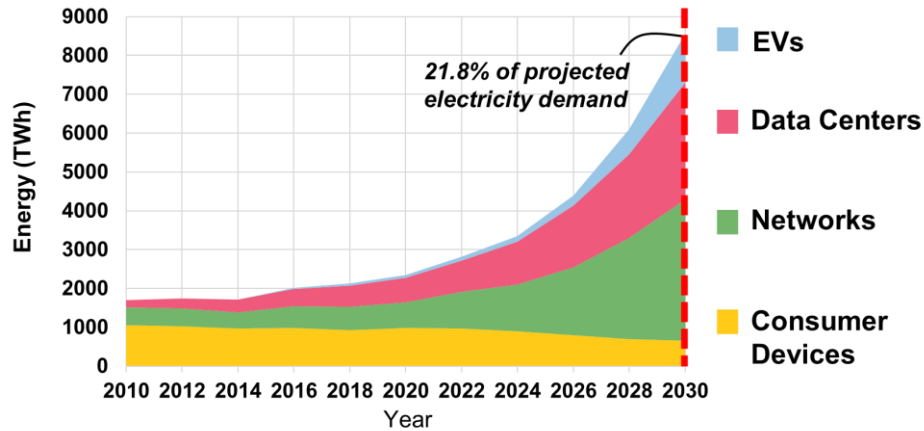


Fig. 1.1. Energy consumption of EVs, data centers, networks and consumer devices in 2010-2030 [1]-[2].

The high-performance multi-core processor is one reason for this rapid growth in energy consumption. The number of transistors per CPU doubles every two years in accordance with Moore's law, as indicated in Fig. 1.2. Shifting from a single core to a multi-core CPU enabled this expansion, resulting in a more power-hungry processor with demanded current >350 A. The development in GPU is even more aggressive and goes beyond the prediction of Moore's law where over 600 cores are implemented in a single GPU chip [3]. The large number of cores dramatically

increases power consumption (>600 A) and represents a significant challenge in powering data centers.

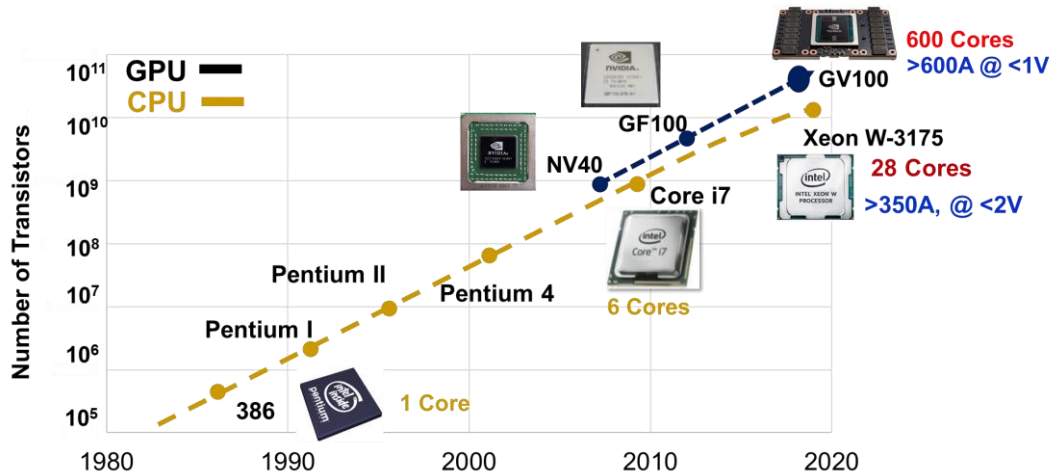


Fig. 1.2. Trend in increasing number of transistors in CPU and GPU.

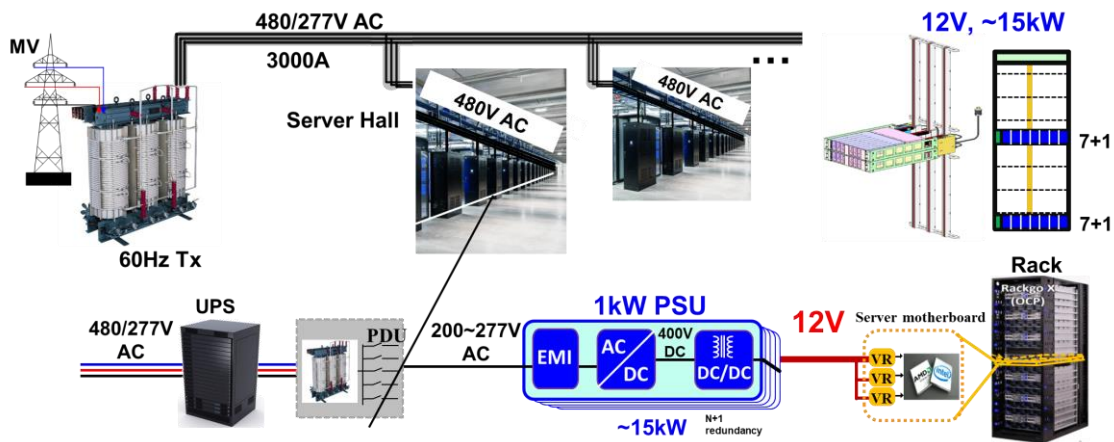
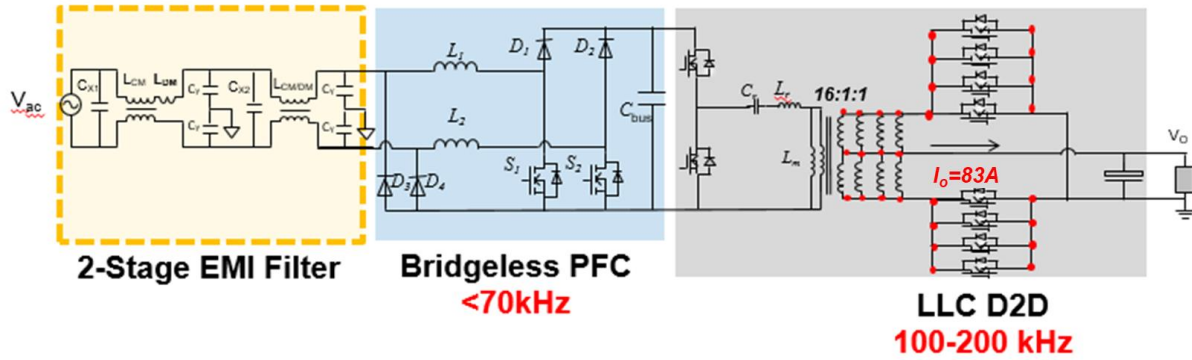


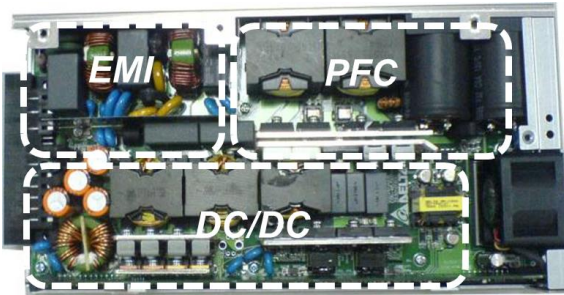
Fig. 1.3. Conventional power distribution system in a data center with 12 V rack voltage.

The conventional power architecture of a data center is shown in Fig. 1.3. The medium voltage is step down and converted to single-phase AC voltage to feed into server racks. Inside each server rack, the power shelves, formed by N+1 redundancy of 1 kW power supply units (PSU), rectify the AC line to 12-V DC voltage to power the server mother board [4]. With the expansion of

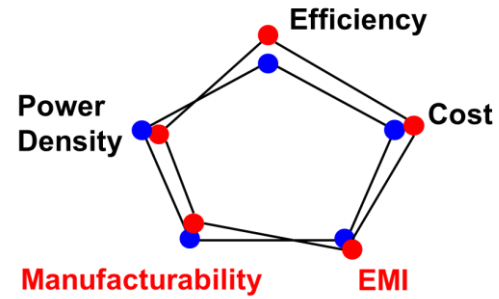
microprocessors and memory devices, power consumption in the server rack is increasing geometrically, but the space for power supplies is limited in a rack. Therefore, advanced server power supplies with higher efficiency and power density are in great demand.



(a)



(b)



(c)

Fig. 1.4. State-of-the-art industry practice for a 1 kW data center server power supply. (a) Topology. (b) A matured product. (c) Trade-offs in performance optimization.

Silicon MOSFET-based power supplies have been used for the past five decades. The state-of-the-art industry practice for a 1 kW data center server power supply is illustrated in Fig. 1.4 (a). A typical two-stage input filter is followed with a bridgeless power factor correction (PFC) rectifier which has an efficiency around 98-99%. The switching frequency of a PFC rectifier is usually limited to equal or below 70 kHz due to hard switching in continuous conduction mode (CCM)

operation. Following that, the LLC resonant converter is deemed most desirable in terms of efficiency and power density for a 400- to 12-V conversion. When operating at 100-200 kHz range, the LLC resonant converter can achieve an efficiency of around 98% and a density of around 100 W/in³. However, with an output current of 83 A, paralleled connections in synchronous rectifiers (SRs) and transformer secondary windings are deemed necessary, resulting in large termination losses and poor current sharing issues.

A typical 1 kW commercial server power supply is illustrated in Fig. 1.4 (b). The state-of-the-art solution has reached a point of maturity in performance where efficiency, power density and cost are major trade-offs involved in any performance improvements, as presented in Fig. 1.4 (c). The remaining challenges are summarized as follows:

1) Magnetic components are bulky, and they lack integration. Conventional magnetic components, including inductors and transformers, have remained largely the same for the past five decades. Typical magnetic components for a 1 kW server power supply are illustrated in Fig. 1.5 (a) and (b). The inductor is usually wound with dozens of turns of litz-wire or copper wire. It has a bulky structure with a manufacturing process that is labor-intensive. The transformer winding structure is even more complex. Its primary and secondary windings are implemented with multi-turn litz-wires and copper-foils, respectively. This complex structure results in a poor winding interleaving between primary and secondary windings. Those bulky and discrete magnetic components are major roadblocks toward a more integrated design.

2) Lack of effective approaches to mitigate EMI noises. In conventional practice, there are no specific approaches to reduce EMI noises. In general, a two-stage or even a multi-stage EMI filter is needed to meet the EMI standards. Fig. 1.6 (a) and (b) show a typical two-stage EMI filter, where

the differential-mode (DM) inductor and common-mode (CM) inductor were not able to be integrated into one magnetic core. Usually, an EMI filter occupies one-fourth to one-third of the total volume of a power supply. In certain cases, EMI filter design even requires a trial-and-error process.

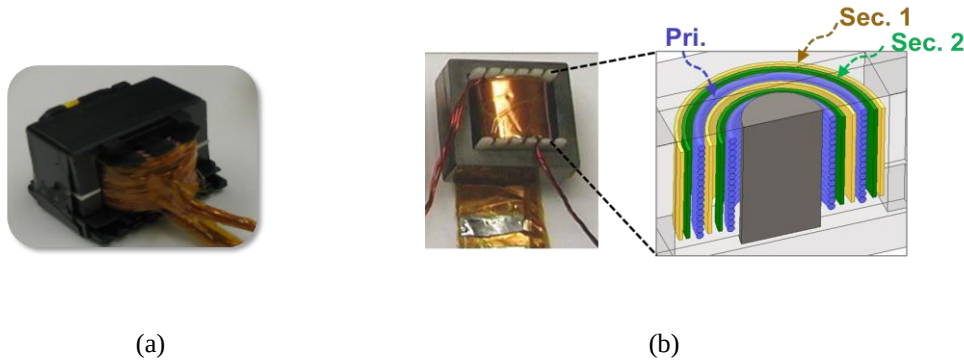


Fig. 1.5. Conventional bulky magnetic components. (a) Inductor. (b) Transformer [5].

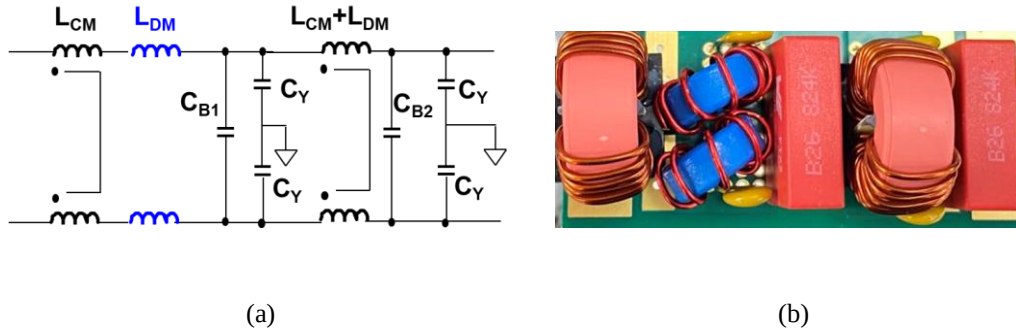


Fig. 1.6. A typical two-stage EMI filter. (a) Topology circuit. (b) Hardware implementation.

3) The manufacturing process is labor intensive. A typical assembly line for power supplies is illustrated in Fig. 1.7. To date, most products are custom designed with a manufacturing process that is labor intensive. The major roadblocks for widespread applications using these more integrated solutions hinge on the ability to integrate large and bulky passive components with power semiconductors in a form suitable for automation.



Fig. 1.7. Labor intensive system assembly.

1.2 Opportunities with Wide-Bandgap (WBG) Devices on Off-Line Power Supplies

With recent advances made in gallium nitride (GaN) and silicon carbide (SiC) power devices, it has been demonstrated that increasing switching frequency by a factor of 10-20 is possible without compromising efficiency [6]-[13]. Contrary to the large variety of possible converter topologies available for silicon-based design, it is interesting to note that converter topologies for GaN-based design are rather limited. For example, the bridgeless totem-pole configuration for the PFC rectifier is deemed the most desirable among a number of possible PFC circuits. However, this topology is deemed unsuitable for silicon devices due to its slow parasitic body diode. The LLC resonant topology for DC/DC conversion is an obvious choice at a switching frequency 5-10 times higher than the current practice. The ability of wide-bandgaps to establish a standard converter topology will have a significant impact on further development of standardized modular building blocks toward the system-level integration for broader range applications.

Fig. 1.8 illustrates the comparison of associated energy dissipation during a switching event between a 600 V rating GaN device and a comparable silicon MOSFET [7]. From Fig. 1.8, it is

obvious that the GaN device is capable of operating at a frequency 2-3 times above its silicon counterpart without incurring additional switching losses. Furthermore, if zero-voltage switching (ZVS) [6]-[7] is realized, a GaN device is able to operate at a switching frequency 10-20 times above its silicon counterparts. With the ability to increase switching frequency by one order of magnitude, the values of magnetic components are significantly reduced. Thus, the often-complicated magnetic structure can be broken down into basic elemental pieces. These elemental pieces can be further integrated into a form of matrix structure with embedded PCB windings, suitable for automation. The end result is a product with significant improvements in efficiency, density, and manufacturability.

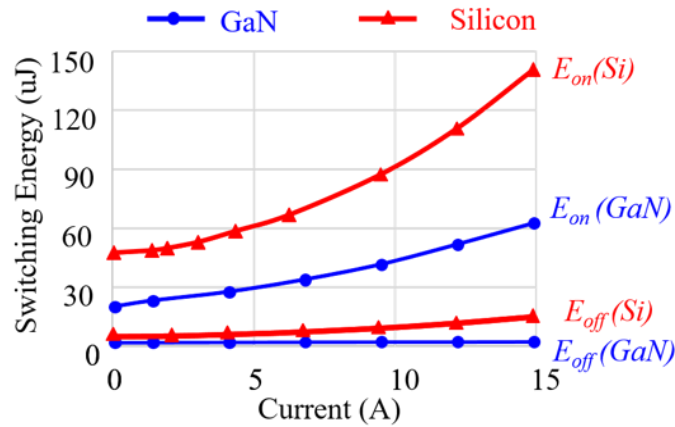


Fig. 1.8. Switching energy comparison for a 600 V GaN device and a Silicon MOSFET. The studied GaN device and Silicon device are TPH3206 and FCP13N60, respectively [7].

1.2.1 State-of-the-Art WBG-Based Resonant Converters

LLC resonant converters are deemed most suitable for the purpose of high-efficiency and high-power-density [14]-[22]. LLC converters can achieve ZVS from no load to full load. The turn-off current for the primary switches is relatively low, and the SRs can achieve ZVS/ZCS. These features are critical for switching at high frequencies [6]-[7], [23]. Furthermore, soft-switching

also leads to the reduction of electromagnetic interference [18].

For applications that require low-voltage and high-current outputs, several important design considerations are highlighted:

1) The SR devices have limited current capability, due to packaging and thermal constraint. For 1 kW server power supplies, one should consider paralleling four to eight SRs to reduce conduction losses, as illustrated in Fig. 1.9(a). When paralleling a large number of SRs, both static and dynamic current sharing are difficult to achieve, especially at high frequencies.

2) The large high frequency AC current with high di/dt must flow through common termination points among the paralleling transformer secondary winding layers and among the paralleling SRs. The termination points are highlighted with red dots in Fig. 1.9(a). The losses associated with terminations are significant and should not be overlooked.

3) It is difficult to place the large number of SRs physically close together, resulting in large leakage inductances at the transformer's secondary windings.

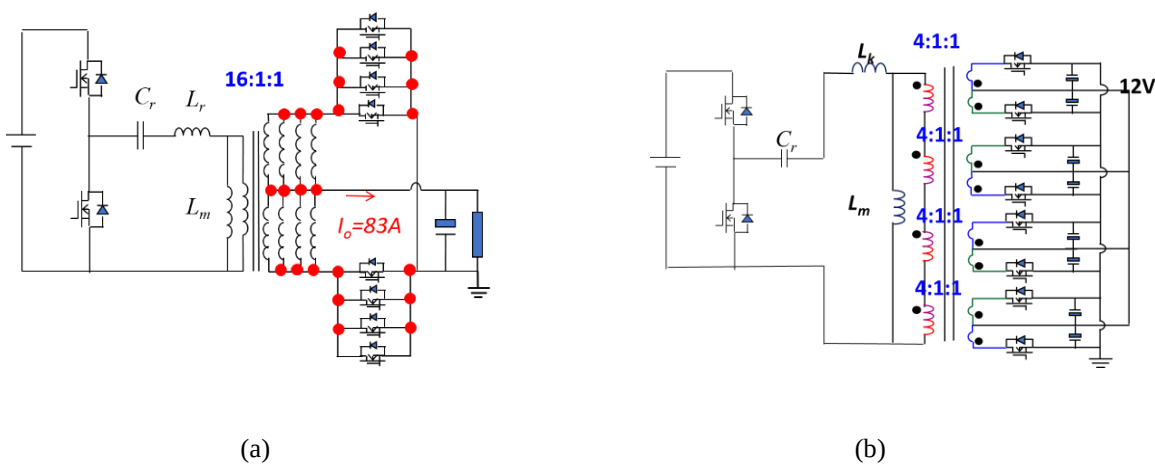


Fig. 1.9. Conventional vs. GaN-based LLC converters. (a) Conventional low voltage high current LLC topology. (b) GaN-based LLC topology with matrix transformer.

To date, transformers are implemented using litz wires or copper wires as the primary windings and copper foils as the secondary windings. They are very bulky, labor-intensive to manufacture, and have poor yield. With the prospect of operating at a significantly higher switching frequency, a very different design and manufacturing practice is contemplated as shown in sections 1.2.1-A - 1.2.1-C.

A. PCB-Based Planar Matrix Transformer for a 1 kW LLC converter

With a switching frequency up to the MHz range, a planar transformer structure with a PCB winding is feasible. An LLC converter with four transformers is shown in Fig. 1.9(b). The traditional single core structure is divided into a four-core structure [9]. Each core is implemented with a simple 4:1:1 winding ratio that can be easily realized with a 4-layer PCB. Because the primary current for the four elemental transformers is in series, the secondary current is perfectly balanced. The termination losses are completely eliminated for the SRs, thus there is no current sharing issue associated with the SRs, as well as among the transformer secondary windings.

The concept of flux cancellation is proposed to further reduce core size and loss [24]. The matrix transformer structure begins with four sets of identical UI-cores where the primary windings are wrapped around one pillar of each core, as shown in Fig. 1.10(a). If the primary winding is modified, where windings between two adjacent core legs are carrying current in opposite directions, as shown in Fig. 1.10(b), flux cancellation is achieved. In this manner, the number of cores can be reduced from four to two, as shown in Fig. 1.10(b) [9].

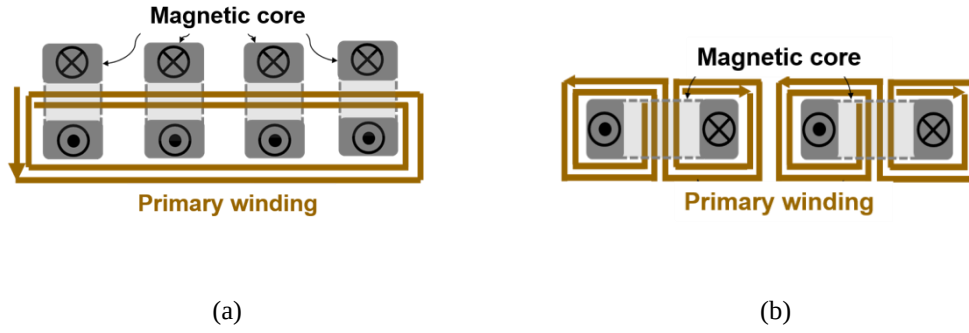


Fig. 1.10. Matrix transformer structures. (a) Matrix transformer with shared primary windings. (b) Improved matrix transformer with flux cancellation.

The structure can be rearranged in the form shown in Fig. 1.11(a) to facilitate further integration into one compact core structure. Although the flux pattern and core loss remain the same as in the original two-core structure, the flux distribution is shown to be concentrated in the area between four poles, as shown in Fig. 1.11(b).

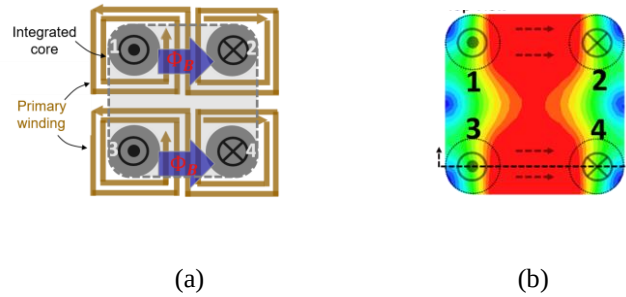


Fig. 1.11. Matrix transformer structure 1. (a) Winding and core structure. (b) Flux distribution in the core.

Further improvement is evident simply by interchanging pole 3 and pole 4 in Fig. 1.12. The magnetic flux can travel both up and down and left and right, resulting in a 50% reduction of the flux density in the magnetic plates. Subsequently, the core loss is reduced by 40%, and the proposed structure is more compact.

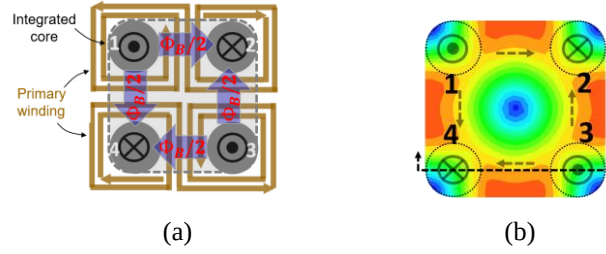


Fig. 1.12. Matrix transformer structure 2. (a) Winding and core structure. (b) Flux distribution in the core.

The matrix transformer windings can be easily integrated with a four-layer PCB, as illustrated in Fig. 1.13 (a). The top and bottom layers are secondary windings, and the two middle layers are primary windings. Fig. 1.13 (b) illustrates a prototype of a 1 MHz 800 W 400 V/12 V LLC converter. It shares the same footprint as a quarter-brick, with about half of its height. A power density of 900 W/in³ was reported [9]. The measured peak efficiency is 97.7 %. A transformer loss breakdown is presented in Table 1.1. It is observed that at 800 W power level, the PCB winding-based transformer has a lower loss compared to the conventional litz wire-based design.

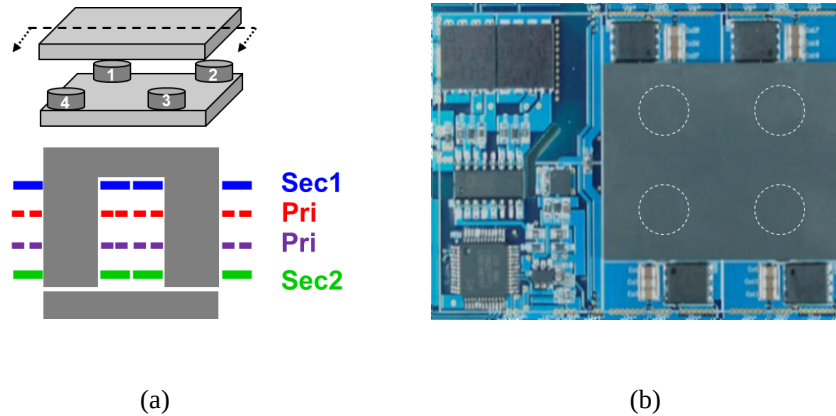


Fig. 1.13. Matrix transformer and a 1-MHz 800-W 400-V/12-V LLC converter prototype. (a) Schematic of PCB windings. (b) Converter prototype. [9]

TABLE 1.1 TRANSFORMER LOSS BREAKDOWN [9]

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB Transformer	8.6	1.4	10.0
Litz-wire Transformer	13.3	3.3	16.6

B. Shielding Techniques for Common Mode (CM) Noise Suppression

As illustrated in Fig. 1.13 (a), the PCB windings are interleaved, thus leading to a large distributed interwinding capacitance. This winding structure will invariably lead to large CM noise current. The problem is further aggravated with high dv/dt using GaN devices. Passive cancellation approaches or balance techniques can be employed to reduce the CM noise [25]-[32], but they require additional components and are sensitive to component tolerance. For PCB winding structure, suppressing CM noise can be easily achieved using the shielding technique [33]-[38]. For a 4-layer PCB winding structure, this is achieved by simply placing two shielding layers in between the primary and secondary windings, as shown in Fig. 1.14. Each shielding layer is connected to the primary ground. Therefore, the CM noise current induced by the primary winding will flow to the shielding layer and return to the primary ground. The shielding layers are made identically to the secondary windings, in a manner that they share the same voltage potential distribution; thus, no CM current can flow between the shielding layer and secondary layer. Fig. 1.15 illustrates the measured CM noises. With the proposed PCB-based shielding technique, a 20-dB μ V CM noise reduction is realized up to 30 MHz.

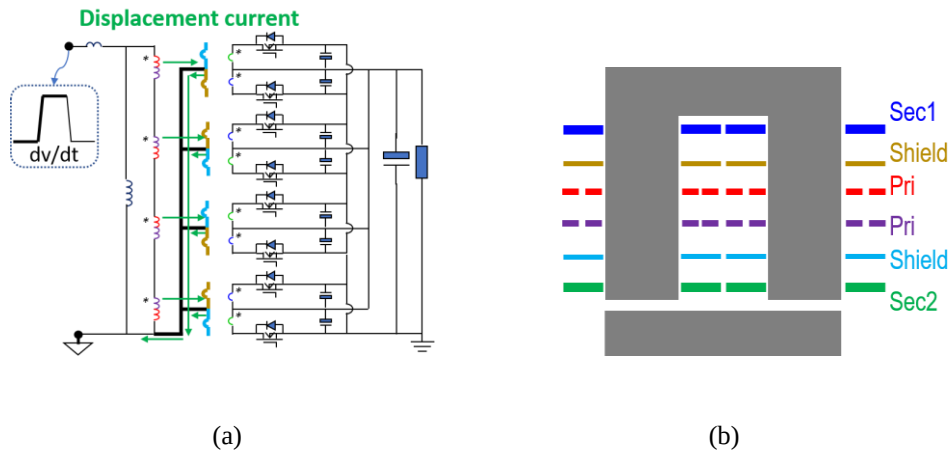


Fig. 1.14. PCB based matrix transformer with shielding layers. (a) Schematics with transformer shielding layers. (b) Cross-sectional view.

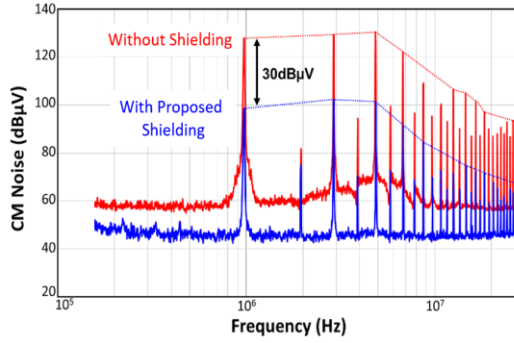


Fig. 1.15. Measurement of CM noise spectrums.

C. Extending to 3 kW Power and Beyond

The similar planar transformer structure was extended to a 1 MHz 3 kW 48 V LLC converter for generation 2 data center server power supplies[40]. Fig. 1.16 (a) and (b) illustrate the flux density in 1 kW and 3 kW designs respectively. It is noticed that for a larger size core, flux distribution in the plate tends to be non-uniform. In particular, the flux concentration at joints between magnetic plates and legs was stronger than that in the 1 kW design. As a result, core loss was dramatically increased from 1.1 W to 14 W, where the eddy current loss alone shares 8.5 W [41].

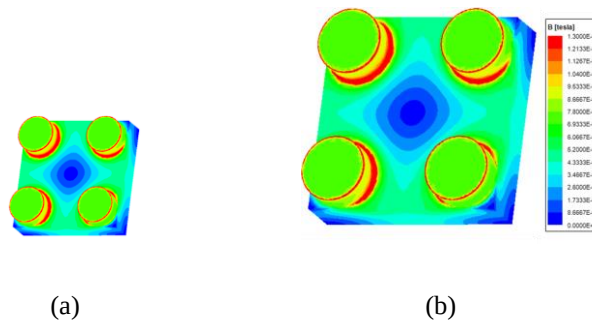


Fig. 1.16. Flux density in planar matrix transformers. (a) 1 kW transformer. (b) 3 kW transformer[41].

In order to have a more uniform flux distribution and minimize the core loss, a low-profile planar transformer structure, shown in Fig. 1.17 (a), was proposed in [42]. The improved structure has a

sides-by-side pillar layout where the flux is alternating in adjacent pillars, as illustrated in Fig. 1.17 (b). Moreover, adding two side walls with zero airgap offers the benefits of reducing flux in plates to half of that in pillars, thus resulting in a low-profile design with more uniform flux distribution, as illustrated in Fig. 1.17 (c). The end result is a design with approximately 60% lower eddy losses and 40% lower profile compared to the conventional planar transformer [41]-[42].

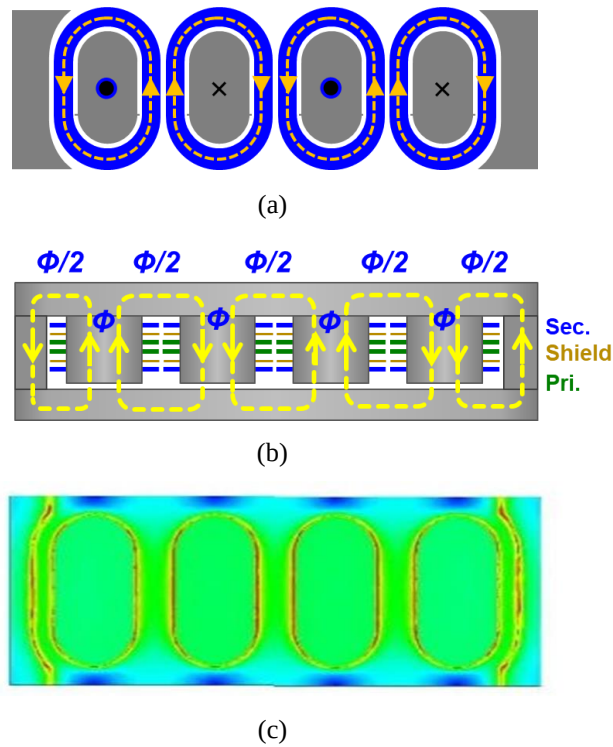


Fig. 1.17. Proposed matrix transformer structure with more uniform flux distribution in [42]. (a) Top-view. (b) Front-view and flux distribution. (c) Flux density in legs and plates.

Furthermore, the proposed structure offers the opportunity of integrating resonant inductors with transformers by adding four more smaller pillars, as delineated in Fig. 1.18. The primary windings of the transformer are extended to encircle those small pillars to form distributed inductors. Fig. 1.19 illustrates the flux distribution in plates. It is observed that both at the time instant of t_1 (peak inductor current) and t_2 (peak magnetizing current), the integration is proved to be beneficial in minimizing flux density in the plate[42].

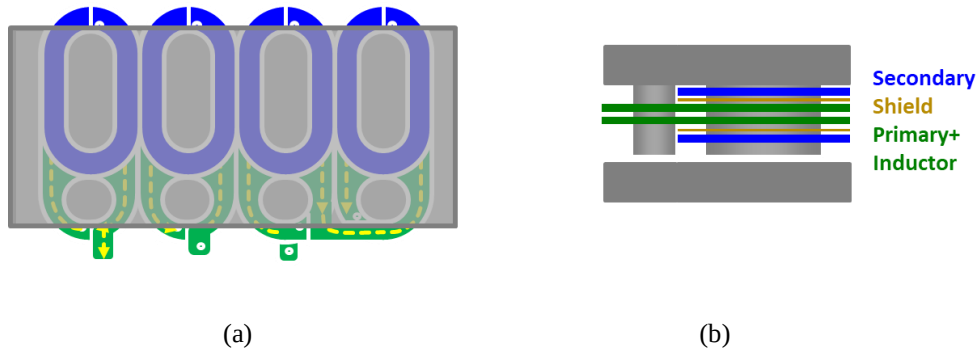


Fig. 1.18. Integration of inductors with transformers by adding additional four pillars. (a) Top-view. (b) Side-view.[42]

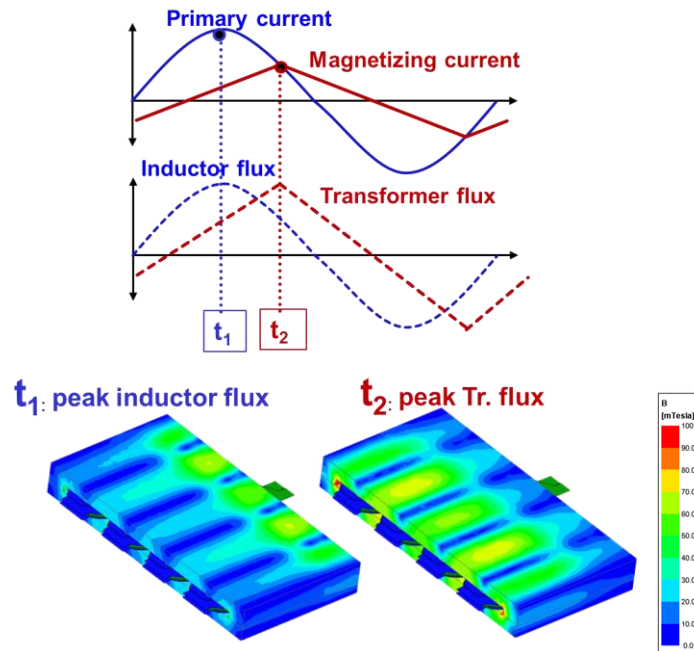


Fig. 1.19. Flux density of integrated inductor and transformer. [42]

With the proposed inductor and transformer integration approach, a 3 kW 400/48V LLC D2D converter operating at 300 kHz was built, as shown in Fig. 1.20. The converter realized a peak efficiency of 98.8% and a power density of 600 W/in³[42].

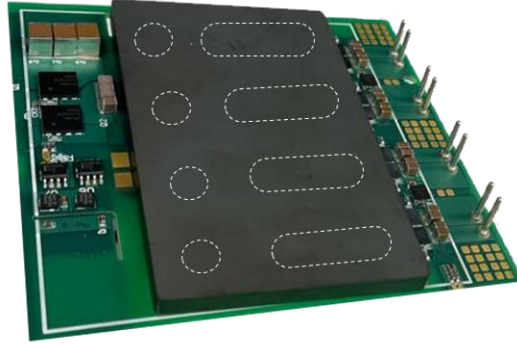
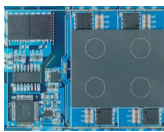
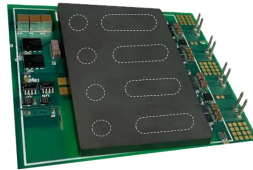


Fig. 1.20. A 3 kW 400/48V LLC D2D converter prototype with PCB integrated inductors and transformers. [42]

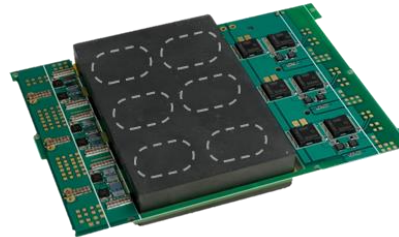
With a similar concept, PCB winding-based planar transformers in the power range of 1 kW to 9 kW have been reported in [9], [41]-[42], as shown in Fig. 1.21 (a)-(c). Their transformer losses are summarized in Fig. 1.22. It is noticed that a resonant converter with PCB winding-based transformer is able to realize a similar efficiency compared to a conventional design, but with a much lower profile and higher power density.



(a)



(b)



(c)

Fig. 1.21. Resonant converters of 1-9 kW with PCB winding-based planar transformers developed in CPES. (a) 1 kW, efficiency: 97.7%, power density: 900 W/in³[9]. (b) 3 kW, efficiency: 98.8%, power density: 600 W/in³ [42]. (c) 6-9 kW, efficiency: 99.2%, power density: 900 W/in³.

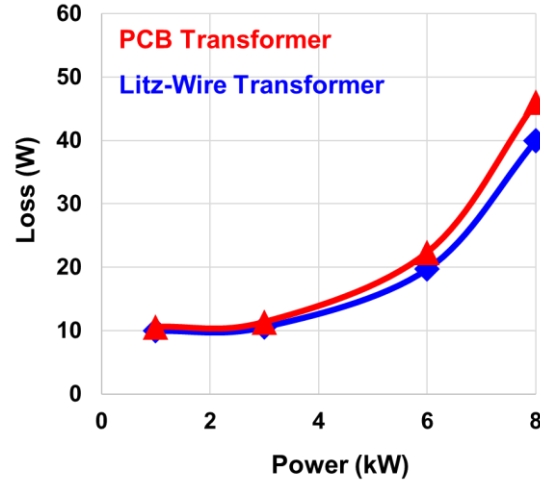


Fig. 1.22. Losses of PCB winding-based transformers and litz-wire transformers in a power range up to 8 kW.

1.2.2 State-of-the-Art WBG-Based PFC/Inverters

In the previous section 1.2.1, significant improvements are evident in resonant converters with WBG devices and PCB winding-based transformers. This section presents the state-of-the-art PFC/inverters to illustrate the opportunities and challenges with WBG devices and PCB winding-based inductors.

To date, the bridgeless PFC [43], as shown in Fig. 1.23(a), is one of the most popular PFC topologies for AC/DC conversion in off-line power supplies. With silicon MOSFETs, a PFC converter usually operates in CCM at a switching frequency equal or below 70 kHz. With recent advances in GaN devices, a PFC rectifier is capable of operating at a frequency 2-3 times above their silicon counterparts without incurring additional switching related losses, as illustrated in Fig. 1.8. However, if the PFC rectifier operates at the critical conduction mode (CRM) to achieve ZVS, the switching related loss is significantly reduced, since the turn off loss is much smaller than its silicon counterparts and the driver loss is negligible. In addition, GaN devices have no reverse recovery loss. Thus, the bridgeless totem-pole configuration, as shown in Fig. 1.23(b), is an

obvious choice for the PFC rectifier.

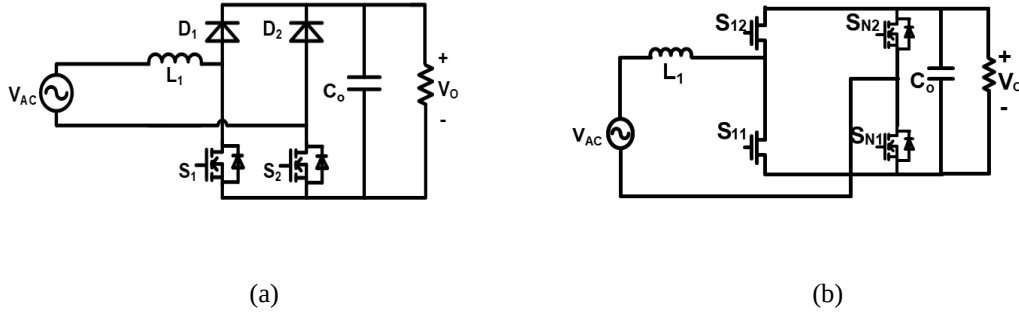


Fig. 1.23. PFC topologies. (a) Basic bridgeless PFC. (b) Totem-pole PFC.

Fig. 1.24 illustrates a loss compare between a silicon MOSFET-based bridgeless PFC and a GaN device-based totem-pole PFC. It is observed that with CRM operation, the 1 kW totem-pole PFC is capable of operating at 1-2 MHz while still maintaining a lower device loss compared to the silicon-based PFC operating in CCM with a switching frequency of 70 kHz. The ability for WBG devices to operate at a frequency 10-20 times higher than current practices will have a significant impact on magnetic design.

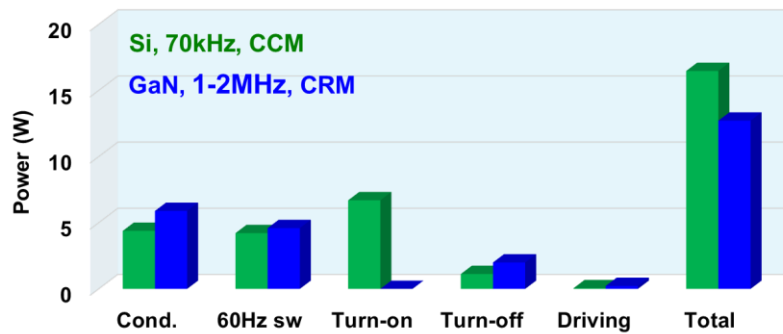


Fig. 1.24. Device loss breakdown for silicon-based PFC and GaN-based PFC at 1 kW output power. Silicon MOSFET-based bridgeless PFC operates in CCM with a switching frequency 70 kHz. GaN device-based totem-pole PFC operates in CRM with a switching frequency 1-2 MHz.

A. PCB Winding Planar Inductor for a 1 kW PFC

By increasing the switching frequency from 70 kHz to 1-2 MHz, the number of turns for a 1 kW PFC inductor is dramatically reduced from 64 to 10 [44]-[46]. This inductor can be easily implemented in a 5-layer PCB, as shown in Fig. 1.25. However, due to the accumulation of magnetomotive force (MMF), winding loss increases dramatically. The inductor loss breakdown based on ANSYS Maxwell finite element analysis (FEA) is summarized in Table 1.2. The winding loss is calculated by a 2-D FEA simulation in Ansys Maxwell, and core loss is calculated by a 3-D FEA simulation in Ansys Maxwell. It is observed that PCB winding inductor has a winding loss of 4.5 W, which is almost two times higher compared to a conventional litz-wire based design.

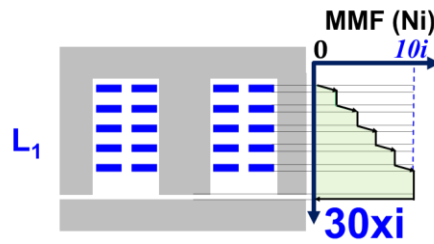


Fig. 1.25. PCB winding-based inductor for a 1kW PFC and its MMF.

TABLE 1.2 INDUCTOR LOSS BREAKDOWN

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	4.5	2.3	6.8
Litz-wire inductor	2.3	2.3	4.6

In order to reduce winding loss, the two-phase interleaving structure, as shown in Fig. 1.26, was adopted [46]. The two inductors were integrated into a single EI-shaped core in the form of inverse coupling, as shown in Fig. 1.27. Instead of placing the windings of L_1 only on the left leg, and L_2 only on the right leg, windings for L_1 and L_2 on the third layer are interchanged to provide MMF

cancellation to some extent. In this way, winding loss is reduced by approximately 40% (from 4.5 W to 2.6 W), as exhibited in Table 1.3. With the proposed structure, the total inductor loss is about the same as a conventional design using litz wire, with a slightly larger winding loss and smaller core loss [46].

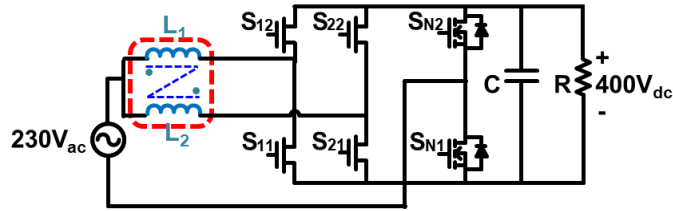


Fig. 1.26. Two-phase interleaved totem-pole PFC converter for a 1 kW server power supply.

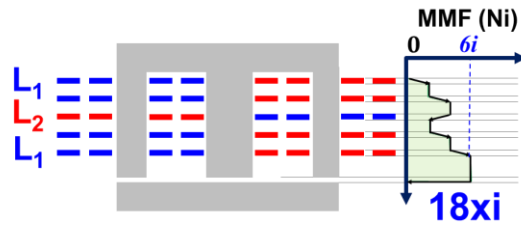


Fig. 1.27. Interleaved PCB winding structure and its MMF.

TABLE 1.3 INDUCTOR LOSS BREAKDOWN FOR INTERLEAVED STRUCTURE

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB inductor w/ interleaving	2.6	1.9	4.5
Litz-wire inductor	2.3	2.3	4.6

B. Balance Technique for CM Noise Suppression

One drawback of the CRM PFC rectifier is the high current ripple. This leads to not only a higher conduction loss but also a higher DM noise, compared to the CCM PFC rectifier. By virtue of two-phase interleaving, DM noise and filter size are effectively reduced by 3 times[47], as illustrated in Fig. 1.28.

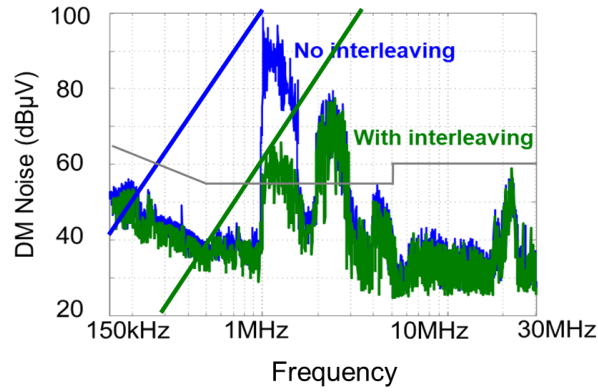


Fig. 1.28. Measured DM noises on a 1 kW CRM PFC converter.

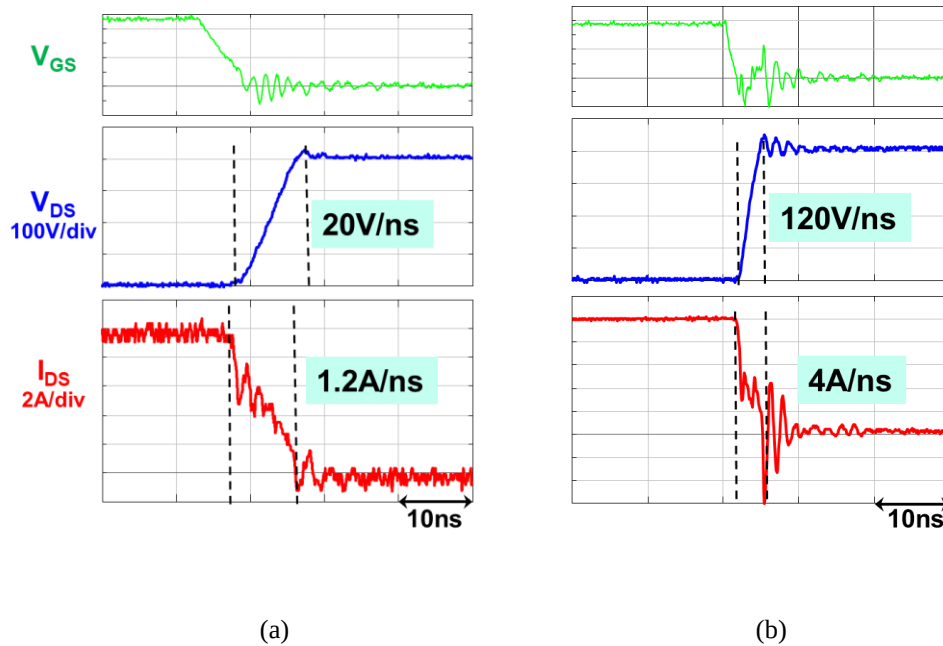


Fig. 1.29. Measured dv/dt and di/dt in switching events. (a) Silicon MOSFET: IPB60R165CP, $R_{on}=0.15\ \Omega$, $C_{oss}=220\ \text{pF}$. (b) GaN device: PGA26E19BV, $R_{on}=0.15\ \Omega$, $C_{oss}=34\ \text{pF}$ [48].

However, when GaN devices are used, the high di/dt and dv/dt during switching events lead to a concern in CM noise. Fig. 1.29 (a) and (b) present the gate signal V_{GS} , drain-source voltage V_{DS} , and current I_{DS} during a turn-off event for a typical 600 V silicon-MOSFET and a GaN device [48]. It is observed that a GaN device has 6 times higher dv/dt and 3 times higher di/dt compared to its silicon counterpart. In consequence, the CM noise measured in a GaN device-based PFC is

approximately 30 dB μ V higher than that in a silicon MOSFET-based PFC, as illustrated in Fig. 1.30.

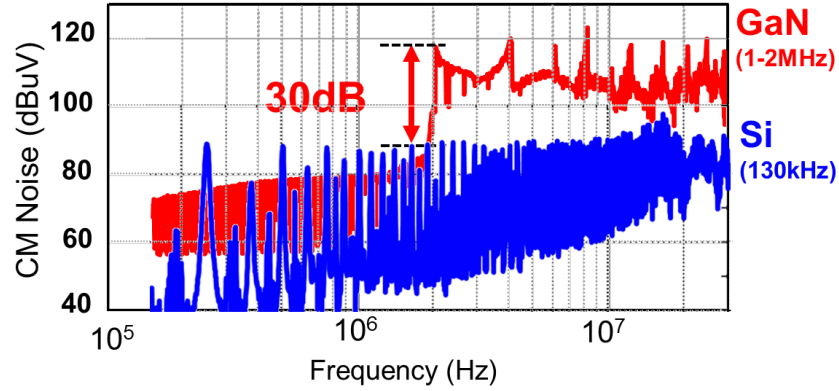


Fig. 1.30. Measured CM noises for a silicon MOSFET-based dual-phase boost PFC operating at 130 kHz [49], and a GaN device-based dual-phase totem-pole PFC operating at 1-2 MHz at 1 kW power rating.

The use of PCB-integrated magnetics offers an opportunity for significant reduction of CM noise. This is achieved by incorporating a proposed balancing technique [25], [50], which can be implemented in the PCB winding structure. The concept of the balance technique is to form a circuit topology that can be characterized by a Wheatstone bridge like structure, as shown in Fig. 1.31. In this Wheatstone bridge circuit, if $Z_1/Z_2 = Z_3/Z_4$, the voltage potential at point A is equal to that of point B. Therefore, there should be no CM current flow between point A and point B.

In order to use the balance principle for CM noise reduction, two additional inductors, L_3 and L_4 , are employed and coupled with L_1 and L_2 , respectively, as shown in Fig. 1.32(a). The equivalent CM circuit model is shown in Fig. 1.32(b), where V_{s1} and V_{s2} represent the two noise sources. The number of turns of L_1 and L_2 is N_1 . The number of turns of L_3 and L_4 is N_2 . Thus, the balance condition for source V_{s1} is $N_1/N_2 = (C_b + C_{add})/C_d$ [46].

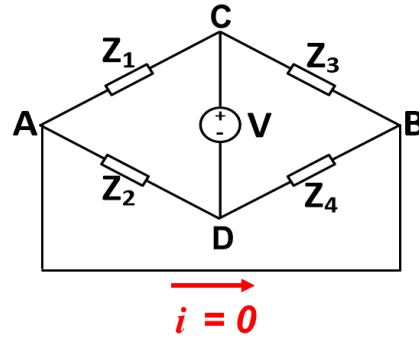


Fig. 1.31. Wheatstone bridge circuit.

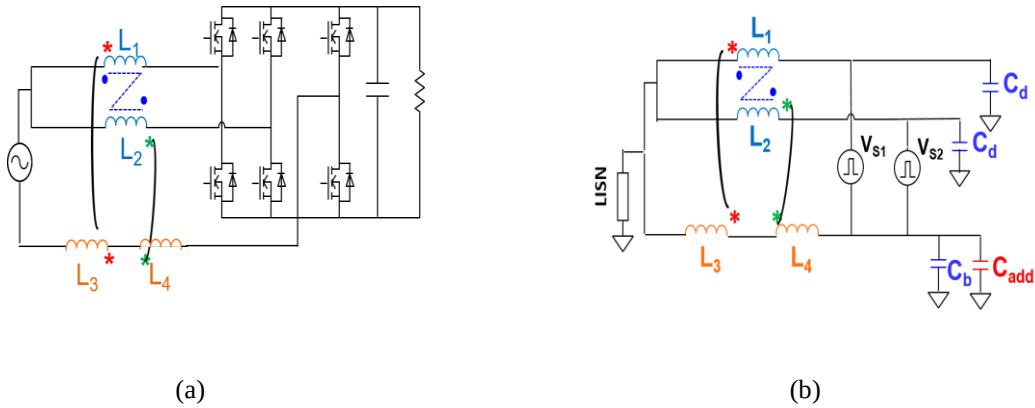
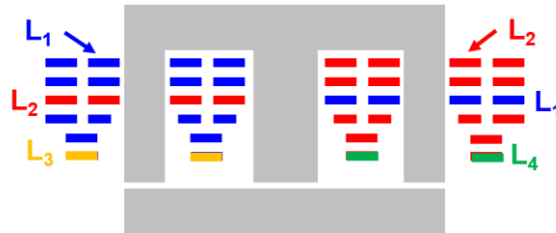


Fig. 1.32. Balance technique for interleaved totem-pole PFC converter with coupled inductors. (a) Circuit structure. (b) Equivalent circuit model of CM noise.

Fig. 1.33. PCB implementation of balance technique in a 1 kW PFC [45]-[46]. The coupling coefficients between inductor L_1 and L_2 , and L_1 and L_3 , are $\alpha_{12} = -0.6$ and $\alpha_{13} \approx 0.96$ respectively.

With PCB-based magnetics, the balance winding was implemented by replacing the one-turn balance inductor L_3 and L_4 , as the bottom layer of the PCB winding as shown in Fig. 1.33. Fig. 1.34 shows that with the balance technique, CM noise can realize 20 dB μ V reduction inside 7

MHz in a 1 kW PFC converter. However, balance technique is ineffective between 7-30 MHz.

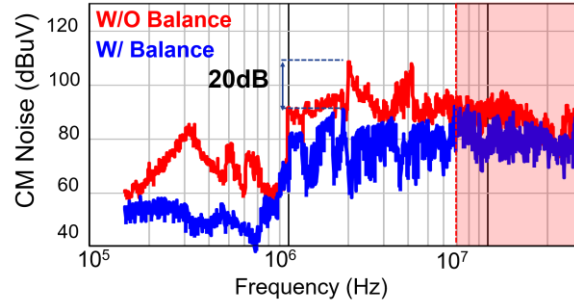


Fig. 1.34. CM noise reduction by balance technique in the prior art [45]-[46].

C. Extending to 3 kW Power and Beyond

The PCB-integrated inductor was extended to a 3 kW PFC with a switching frequency of 300-800 kHz. The PCB winding-based inductor and the interleaved winding structure are illustrated in Fig. 1.35 (a) and (b). With a wider winding width compared to the 1 kW inductor, a single turn per layer structure is selected to minimize the winding length. The two-phase interleaved structure offers the opportunity of realizing a PCB-based winding design using eight-layer PCBs. The loss breakdown is summarized in Table 1.4. It is observed that interleaving effectively reduces winding loss by 30% (from 13.7 W to 9.3 W). However, the total inductor loss is approximately 1.5 times larger than a conventional litz wire-based design. Thus, as power increases, the PCB inductor incurs extra losses.

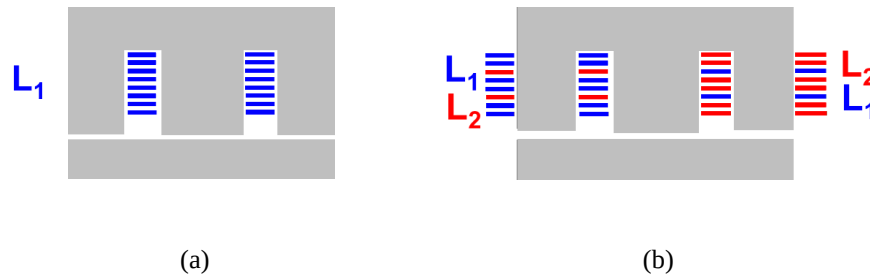


Fig. 1.35. PCB Inductors for a 3 kW PFC. (a) PCB winding inductor. (b) PCB inductor with winding interleaving.

TABLE 1.4 LOSS BREAKDOWN FOR A 3 kW PCB INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	13.7	8.0	21.7
PCB inductor w/ interleaving	9.1	7.9	17.0
Litz-wire inductor	5.8	6.2	12.0

The PCB-based inductor was further extended to a 6.8 kW EV on-board battery charger in [45], as shown in Fig. 1.36, where a variable DC-link voltage of 500-840 V was adopted to improve the charging cycle efficiency. A positive coupling approach was selected to minimize switching frequency range [45]. The PCB winding inductor structures are illustrated in Fig. 1.37 (a) and (b). Since the center leg air gap is smaller than that in the outer leg, a double-PQ core structure, as delineated in Fig. 1.37(b), was proposed to improve mechanical stability and minimize core loss. The inductor loss breakdown is summarized in Table 1.5. It is noticed that, at a 6.8 kW power level, the PCB inductor has 2-3 times higher loss compared to a litz wire-based design.

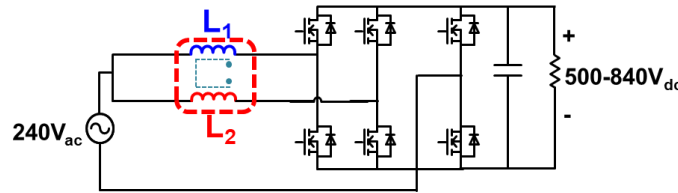


Fig. 1.36. Two-phase interleaved totem-pole PFC converter for a 6.8 kW EV on-board battery charger[45].

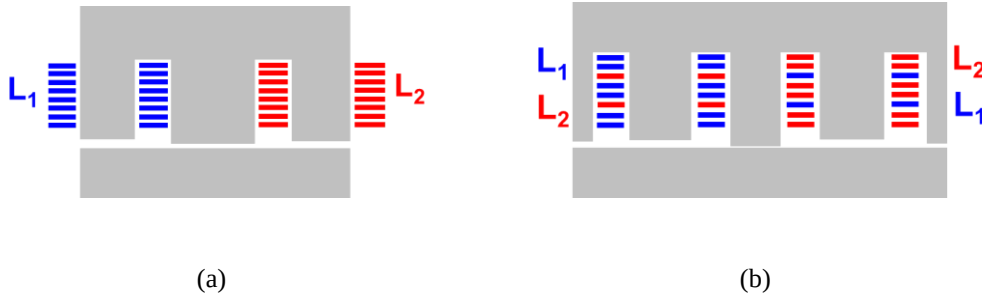


Fig. 1.37. PCB Inductors for a 6.8 kW PFC. (a) PCB winding inductor integrated in an EI-shaped core. (b) PCB integrated inductor with winding interleaving and a double-PQ core structure.

TABLE 1.5 LOSS BREAKDOWN FOR A 6.8 kW PCB INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB inductor w/o interleaving	47.0	35.0	82.0
PCB inductor w/ interleaving	36.0	30.0	66.0
Litz-wire inductor	14.0	13.0	27.0

PCB inductor losses for 1 kW, 3 kW and 6.8 kW PFC converters are summarized in Fig. 1.38. It is noticed that by increasing power from 1 kW to 6.8 kW, core losses are dramatically increased by 16 times. The unexpected higher core losses were not only observed in hysteresis losses, but also in DC bias-related losses and eddy losses. The increase in winding losses is even more severe than those in core losses. The winding loss for the 6.8 kW PCB inductor is 18 times higher than that in the 1 kW inductor. Those drastically increased inductor losses lead to a significant challenge for the implementation of PCB inductors in a high-power level.

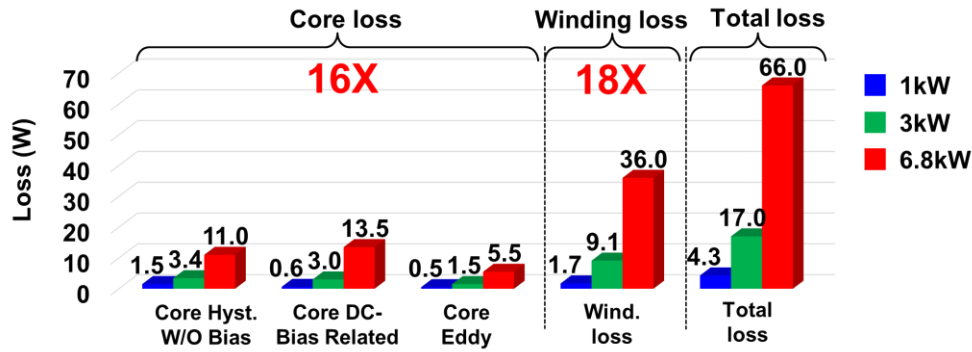


Fig. 1.38. PCB inductor losses for 1 kW, 3 kW and 6.8 kW PFC converters.

1.2.3 Challenges and Opportunities

A. Challenges and Opportunities of a PCB-Based Inductor

A PCB winding-based inductor has a fundamental limitation in power range. The PCB

inductor winding loss is proportional to magnetomotive force (MMF), which is Ni . That is to say, with the number of turns (N) and currents (i) increased, winding loss is increased nonlinearly. In order to minimize winding loss, it is desirable to create some levels of interleaving among layers for a multilayer winding structure ($N>3$). Meanwhile, a multiple core inductor structure with a limited number of turns for each elemental inductor is preferred to minimize winding loss.

The high core loss in high-power applications is another concern. For a large size inductor core, uniform flux is difficult to achieve with planar structure, thus resulting in higher core loss. In addition to the hysteresis loss, there are even high DC-bias related loss and eddy current loss. In order to minimize core loss, an improved magnetic core structure with more uniform flux distribution is desirable.

B. Challenges and opportunities in EMI

The CRM PFC rectifier inherently has a higher current ripple, which leads to higher DM noises, compared to the CCM PFC rectifier. By virtue of two-phase interleaving, DM noises can be effectively reduced. However, compared to a silicon-MOSFET based PFC converter, a GaN device-based PFC converter has significantly increased CM noises ($\sim 30\text{dB}$ higher) due to the high dv/dt and di/dt , and the increased interwinding capacitors in PCB structures. Balance technique has been demonstrated effectively to suppress CM noises up to several mega-hertz with diminishing effect beyond that. Further improvements in balance technique hinge on identifying the root cause of the failure to achieve the expected outcome and improving the magnetic design to circumvent those detrimental effects.

Furthermore, those special efforts in minimizing EMI noises in PFC and DC/DC converters offer an opportunity of minimizing the EMI filter size and improve the power density for a server power

supply.

1.3 Dissertation Outline

Several design considerations for WBG and PCB-based PFC/inverters will be addressed in this dissertation.

Chapter 1 introduces the state-of-the-art power supplies and the challenges. The magnetic integrations in a wide range of power are reviewed. The main challenges in magnetic integration and EMI noise suppression are elaborated upon.

Chapter 2 presents analysis of a PCB-based coupled inductor for a PFC/inverter. The power limitation of a PCB inductor is identified based on the analysis of winding and core losses. Furthermore, a modular inductor approach for extending a PCB inductor to a higher power range is proposed. Design considerations for minimizing PCB inductor winding loss and core loss, as well as a detailed inductor optimization process, are provided.

Chapter 3 proposes an improved balance technique for CM noise reduction. A decoupled CM noise equivalent circuit is derived to illustrate the essential conditions of achieving uniform CM noise suppression. Furthermore, an integrated PCB winding coupled inductor structure that achieves uniform CM noise suppression is proposed. Its effectiveness in mitigating CM noise is further verified based on a 1 kW server power supply.

Chapter 4 illustrates the EMI filter design considerations to mitigate near-field effects. An exhaustive finite element analysis and near-field measurements are conducted to better understand the effect of frequency on the polarization of near-field due to the displacement current. Moreover, the unwanted self and mutual parasitics are reduced with proposed approaches. A single-stage filter is demonstrated in an off-line 1 kW, 12 V server power supply.

Chapter 5 concludes the dissertation and gives the research topics that will be worked on in the future.

Chapter 2 PCB-Based Inductor for PFC

In an isolated DC/DC converter, PCB windings have been implemented in the transformer design. With interleaved primary and secondary windings, the AC winding loss can be greatly reduced. However, inductors with PCB windings are seldom seen due to the large winding loss. This chapter offers an analysis of the fundamental limitations of PCB-based inductors in terms of winding and core losses. Those studies conclude the power limit of a PCB-based inductor and lead to a modular building block approach for extending the power range. The improved structure features a lower loss and a smaller volume compared to the state-of-the-art design and can be easily extended to a higher power range without compromising efficiency. In the given example, a 3 kW PFC converter with the proposed PCB winding-based inductor realizes a peak efficiency of 99%. Furthermore, PCB inductor structures in an extended power range up to 6 kW are provided.

2.1 Fundamental Limitations of a PCB-Based Inductor

2.1.1 Analysis of Winding and Core Losses

Since the GaN device has high turn-on loss and extremely small turn-off loss, the totem-pole PFC converter with CRM operation is very desirable for a GaN-based high frequency AC/DC conversion [6]–[8], [51], [52]. The topology of a totem-pole PFC circuit is shown in Fig. 2.1.

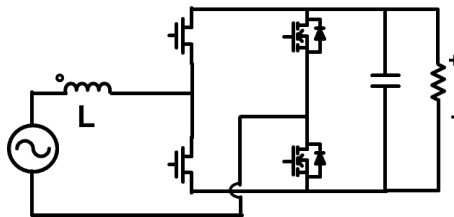


Fig. 2.1. A PFC converter with the totem-pole configuration.

Given switching frequency of 1 MHz at 1/4 of a line-cycle ($T/4$), the inductance value of L is determined by

$$L = \frac{v_{in}(T/4)}{i_{peak}(T/4)} \cdot T_{on}\left(\frac{T}{4}\right) = 5.4 \text{ (}\mu\text{H)}, \quad (2-1)$$

where $T_{on}(T/4) = D(T/4)/f_s(T/4)$, $D(T/4) = 1 - V_{in}(T/4)/V_{on}(T/4)$. With that, the switching frequency for a 1 kW PFC converter in a half line-cycle is plotted in Fig. 2.2. The frequency range is 1-2 MHz.

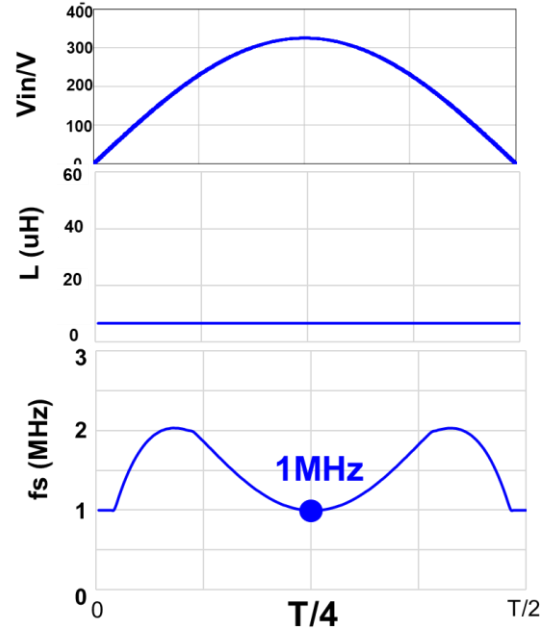


Fig. 2.2. Input voltage V_{in} , inductance value L , and switching frequency f_s in a half line-cycle for a 1 kW PFC in CRM operation.

The CRM inductor current waveforms are illustrated in Fig. 2.3 (a), where the switching cycle inductor current waveform at 1/4 line-cycle is zoomed in, and the instant at peak inductor current is marked as t_l . This current excitation was applied to a PCB winding-based inductor with a 5-layer 10-turn winding structure in ANSYS Maxwell 2-D FEA simulation, as shown in Fig. 2.3 (b).

In here, l_g represents the inductor airgap and d represents the distance between the bottom winding to the airgap. The same airgap applies to both middle and outer legs. For a PCB winding-based inductor, the ratio of d/l_g impacts the fringing effect, and thus the winding loss. Fig. 2.4 illustrates the fringing flux of three cases by varying the ratio of d/l_g from one to five. It is observed that the layers close to the airgap directly face the strong fringing flux for $d=1 \times l_g$ (Fig. 2.4 (a)), while the impact of fringing flux is minor for $d=3 \times l_g$ and $d=5 \times l_g$ (Fig. 2.4 (b) and (c)). Therefore, in the case of a 1 kW PCB inductor, $d \geq 3 \times l_g$ is preferred to minimize the fringing effect.

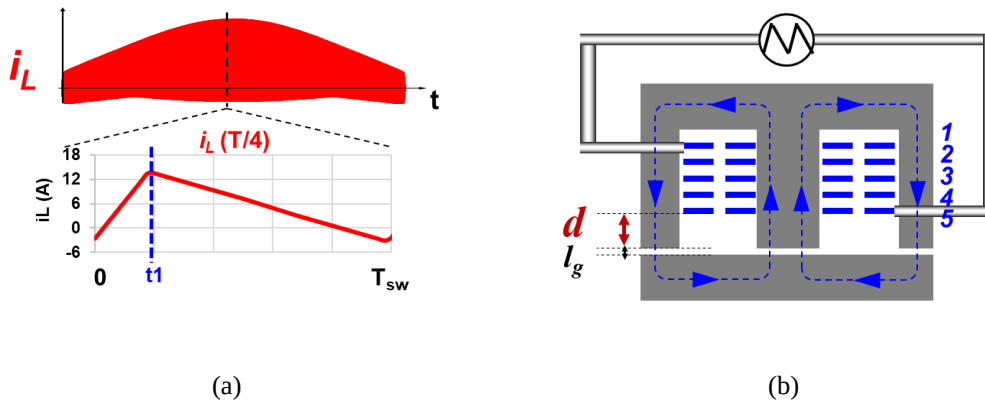


Fig. 2.3. CRM inductor current waveforms and the configuration in FEA simulation for a 1 kW PFC. (a) Waveforms. (b) Applying current excitation to a PCB inductor.

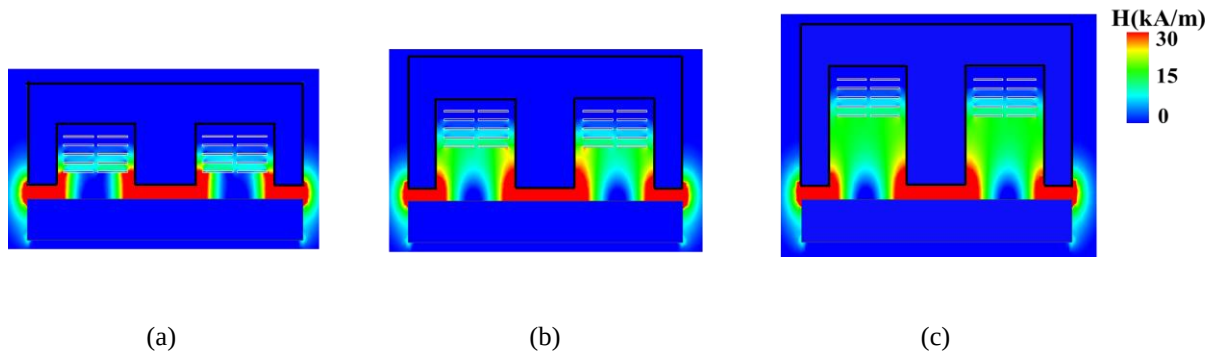


Fig. 2.4. Fringing flux (magnetic field) of a PCB inductor at the instant of t_1 . (a) $d=1 \times l_g$. (b) $d=3 \times l_g$. (c) $d=5 \times l_g$.

Despite the difference in fringing effect, one might be curious about the non-symmetrical flux distribution in the middle and outer legs observed in all three cases. This phenomenon can be best explained by the flux distribution in Fig. 2.5, where the flux density of the case (b) is illustrated as

an example. It is noticed that although major fluxes are flowing in the magnetic core, a small portion of fluxes directly flow from the outer legs to the middle leg through air. Those leakage fluxes weaken the effective fluxes in the outer legs, resulting in a lower fringing flux compared to that in the middle leg.

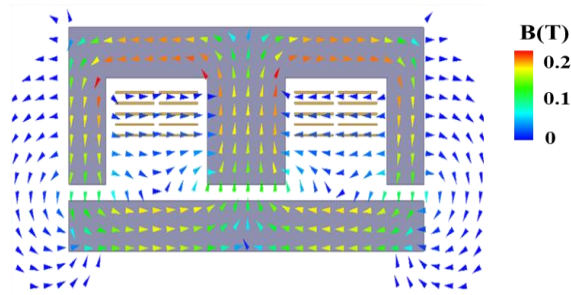


Fig. 2.5. Magnetic flux for the PCB inductor.

The method of calculating winding loss for a CRM PFC is described in Fig. 2.6. The inductor current in 1/4 of a line-cycle is evenly divided into five piecewise linear segments. Inside each segment, the peak-peak current and the switching frequency are assumed to be constant, and the middle point of each segment is chosen as the sampling point. Thus, winding loss is calculated by averaging losses of those 5 points in a quarter of a line-cycle.

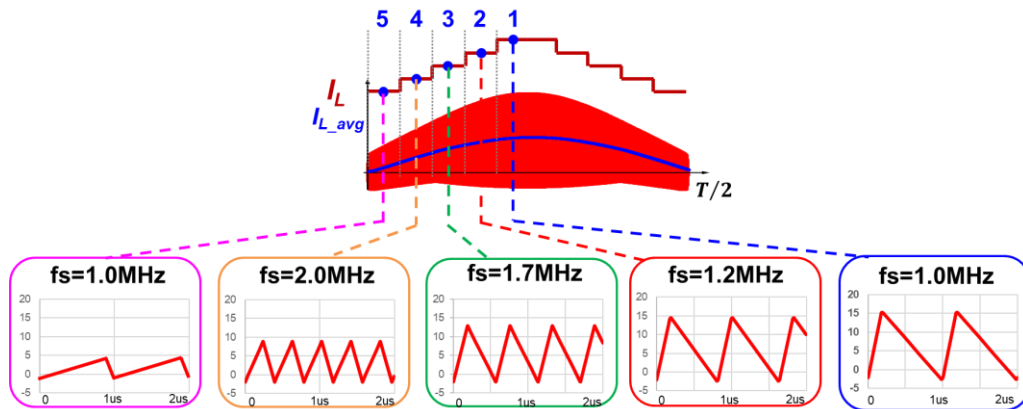


Fig. 2.6. Method of calculating winding loss for a CRM PFC by averaging losses of 5 points in 1/4 of a line-cycle.

By sweeping copper thickness from 0.5-4 oz, the calculated winding loss of each layer, as well as the total winding loss are delineated in Fig. 2.7. It is observed that winding loss is a function of copper thickness. Taking the first layer as an example, when copper thickness is smaller than 1 oz, its winding loss is essentially dominated by the DC winding loss, which can be easily calculated by $P_{dc}=I_{rms}^2\rho l/A_e$, where ρ is the conductivity of copper, l is the winding length for one layer, and A_e is the cross-section area of a winding. Further increasing copper thickness enlarges the difference between the first layer winding loss and the DC winding loss, which is attributed to the increased AC winding loss associated with stronger eddy currents. Moreover, as the number of layers increases, winding loss increases geometrically. Summing up the losses of those five layers leads to the total winding loss, which is represented by the thick blue curve. Based on that, the 1 oz copper is selected because the winding loss is minimized most with this copper thickness.

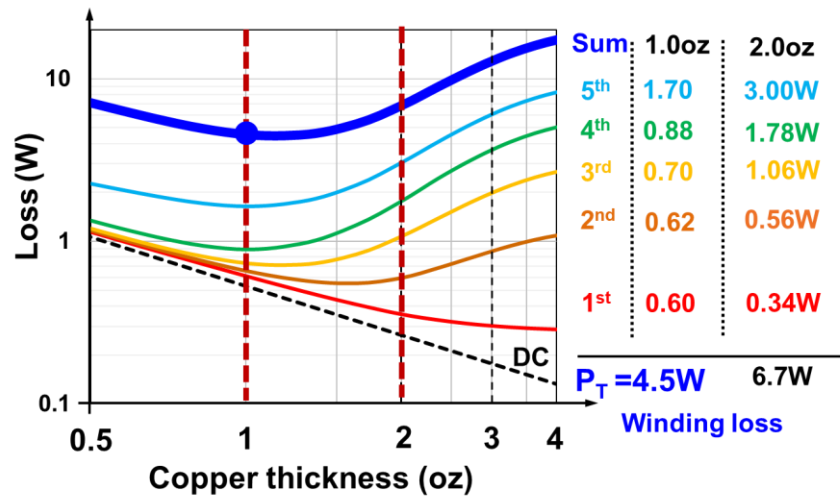


Fig. 2.7. Winding loss for layers 1-5, and the total winding loss of a PCB winding-based inductor by sweeping copper thickness from 0.5-4 oz.

The non-linear increase of winding loss as a function of layer is related to the accumulation of

MMF, as delineated in Fig. 2.8. It is observed that for an increased number of layers, the MMF increases geometrically. In consequent, the current density observed in winding cross-sections is increased. The stronger current concentration in windings indicates a larger winding loss associated with certain layers.

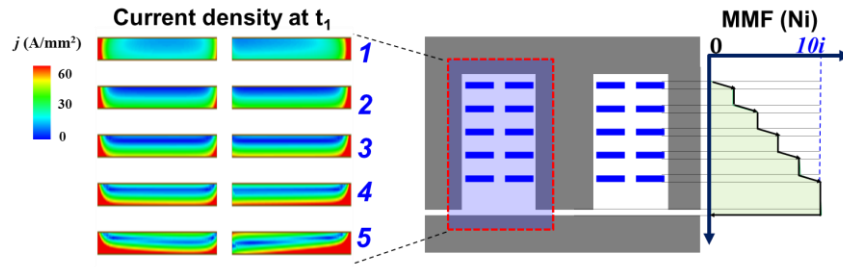


Fig. 2.8. Current density and MMF for a PCB winding-based inductor.

The inductor loss breakdown is summarized in Table 2.1. It is observed that the PCB winding inductor has a winding loss of 4.5 W, which is almost two times higher compared to that in a conventional litz wire-based design. Thus, it is unpractical to use such a PCB inductor for a 1 kW PFC.

TABLE 2.1 INDUCTOR LOSS BREAKDOWN

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	4.5	2.3	6.8
Litz-wire inductor	2.3	2.3	4.6

The two-phase interleaving structure, as shown in Fig. 2.9, offers an opportunity to minimize winding loss. The two inductors were integrated into an EI-shaped core in the form of inverse coupling, as shown in Fig. 2.10. Instead of placing the windings of L_1 only on the left leg, and L_2 only on the right leg, windings for L_1 and L_2 on the third layer are interchanged to provide MMF cancellation to some extent. It is observed that the interleaved winding structure mitigates the

current concentrations to some extent compared to the original, particularly in layers 3-5.

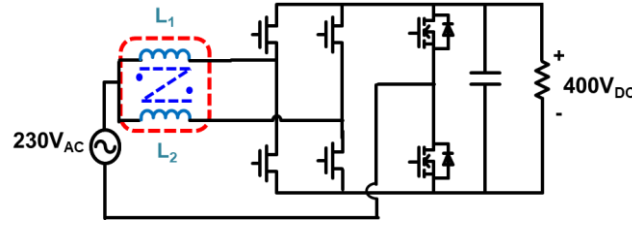


Fig. 2.9. Two-phase interleaved totem-pole PFC converter.

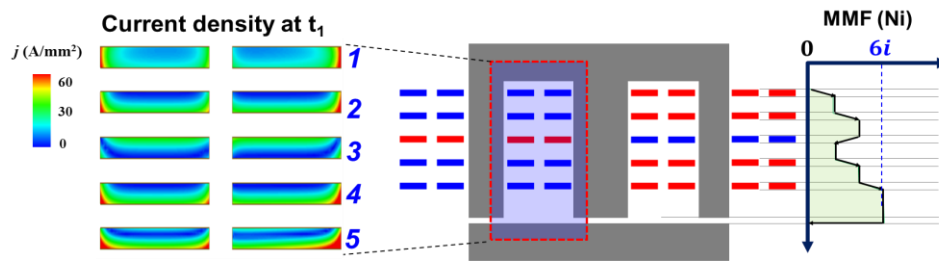


Fig. 2.10. Interleaved PCB winding structure and its MMF.

The effectiveness of the interleaved structure in winding loss reduction is illustrated in Fig. 2.11. Compared to the single-phase inductor, winding interleaving successfully alleviates the geometric increase in winding loss, particularly in layers 3-5. With a more uniform current distribution, a thicker copper with 2 oz thickness is preferred for minimizing winding loss. The end result is a PCB inductor with a winding loss of 2.6 W, which is close to the winding loss of a conventional litz wire-based design (2.3 W).

With winding interleaving, those two inductors are inversely coupled. In the center leg, DC fluxes are observed to add, as delineated in Fig. 2.12. However, as the coupling reduces, more fluxes flow to the center leg, indicating that DC bias increases as α reduces. AC fluxes in the center leg are interleaved and partially cancelled. In the outer legs, DC fluxes subtract from each other,

meaning a reduced DC bias as α increases. AC fluxes are interleaved and inversely coupled. The effects of interleaving and coupling on fluxes will be further discussed in the following works.

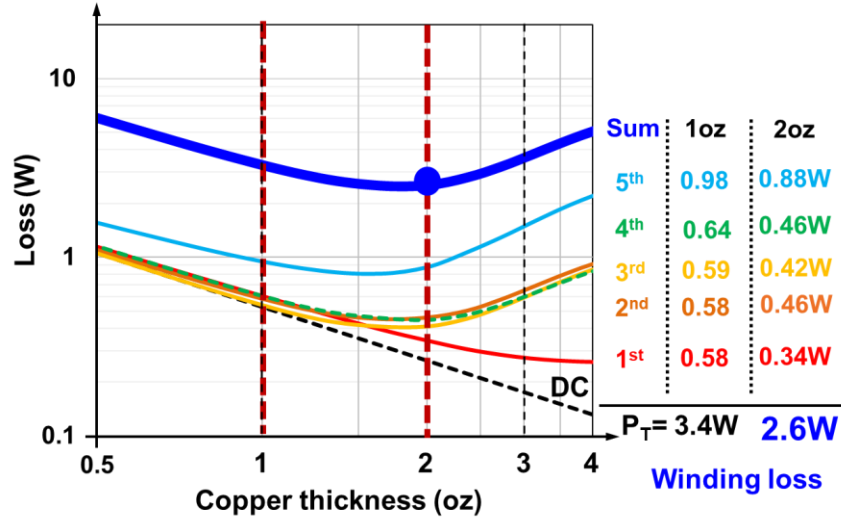


Fig. 2.11. Winding loss of the interleaved PCB winding inductor by sweeping copper thickness from 0.5 to 4 oz.

The coupling coefficient α is expressed as $\alpha = M/L$, where L is the self-inductance for L_1 and L_2 , and M is their mutual inductance. The value of α can be controlled by adjusting the center leg airgap l_{g2} .

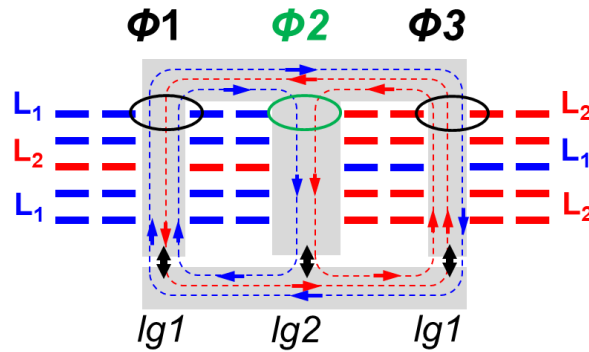


Fig. 2.12. An inversely coupled inductor. Φ_1 and Φ_3 are the fluxes on the outer legs, Φ_2 is the flux on the center leg.

The negative coupling creates non-linear inductors that are functions of the duty cycle D . This is best illustrated in Fig. 2.13 (a) and (b), with the 50% duty cycle serving as the division line where the different behaviors are exhibited. For $D < 0.5$, L_{eq1} is called the steady-state inductance [53] since it determines the current ripple, and thus the switching frequency. For $D > 0.5$, L_{eq3} is the steady-state inductance. The equivalent inductance corresponding to each interval are summarized in Table 2.2.

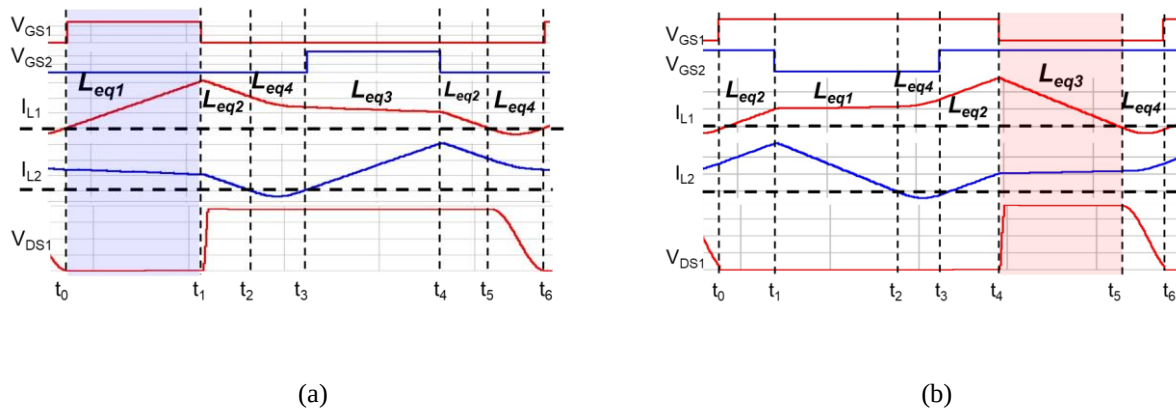


Fig. 2.13. Key waveforms of CRM operation with coupled inductor. (a) V_{GS1} , V_{GS2} , I_{L1} , I_{L2} , V_{DS1} at $D < 0.5$. (b) V_{GS1} , V_{GS2} , I_{L1} , I_{L2} , V_{DS1} at $D > 0.5$.

TABLE 2.2 COUPLED INDUCTOR EQUIVALENT INDUCTANCE[53]

L_{eq1}	L_{eq2}	L_{eq3}	L_{eq4}
$\frac{L^2 - M^2}{L + \frac{D}{D'}M}$	$L + M$	$\frac{L^2 - M^2}{L + \frac{D'}{D}M}$	$L - \frac{M^2}{L}$

One of the benefits of applying an inversely coupled inductor to a CRM PFC converter is that the variance of the switching frequency over a line cycle will decrease by taking advantage of the non-linear inductances, as shown in Fig. 2.14. The net benefit is a reduction of switching losses by 20-30%.

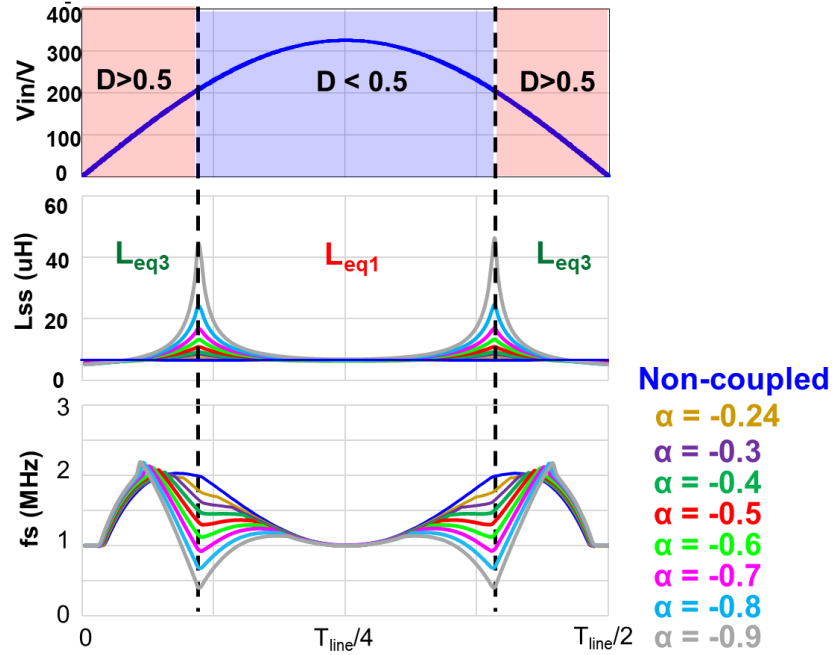


Fig. 2.14. Switching frequency variance during half line cycle for two phase interleaved totem-pole PFC.

Coupling also has impacts on flux and core loss. The benefit of an inversely coupled inductor on DC flux cancellation in the outer legs, as observed in Fig. 2.12, is well understood. However, the effect of inverse coupling and interleaving on AC fluxes is unclear. Moreover, in a PFC converter, the variance of duty ratio in a line-cycle further aggravates the difficulties in understanding the effect of coupling on fluxes. To illustrate the effect of inverse coupling and interleaving on fluxes for a PFC converter, the fluxes in a line-cycle is analyzed based on the piecewise linear approach. As illustrated in Fig. 2.15, a $1/4$ line-cycle is evenly divided into 7 piecewise linear segments. The fluxes at the middle point of each segment, i.e., the point A ~ G, are studied.

Taking point D as an example, Fig. 2.16 (a) and (b) exhibit the inductor currents for two cases with $\alpha = -0.3$ and -0.7 , respectively. The fluxes created by i_{L1} and i_{L2} on the left-side leg, and their

summed flux Φ_1 for the above two cases are illustrated in Fig. 2.16 (c) and (d). It is observed that for the case of $\alpha=-0.3$, only a small portion of the fluxes generated by i_{L2} flow to the left-side leg, as shown with the red waveform in Fig. 2.16 (c). This is different compared to the case of $\alpha=-0.7$ (Fig. 2.16(d)), where a large portion of the fluxes generated by i_{L2} were observed on the left-side leg. Since L_1 and L_2 are inversely coupled, the fluxes created by i_{L2} on the left-side leg are reversed in reference to the i_{L2} current. The summation of fluxes created by i_{L1} and i_{L2} results in the total flux Φ_1 on the left-side leg, as delineated by the black dotted line in Fig. 2.16 (c) and (d). It is observed that the AC flux of Φ_1 at $\alpha=-0.7$ is stronger compared to that at $\alpha=-0.3$. Therefore, interleaving and negative coupling increase AC fluxes in the outer leg at point D.

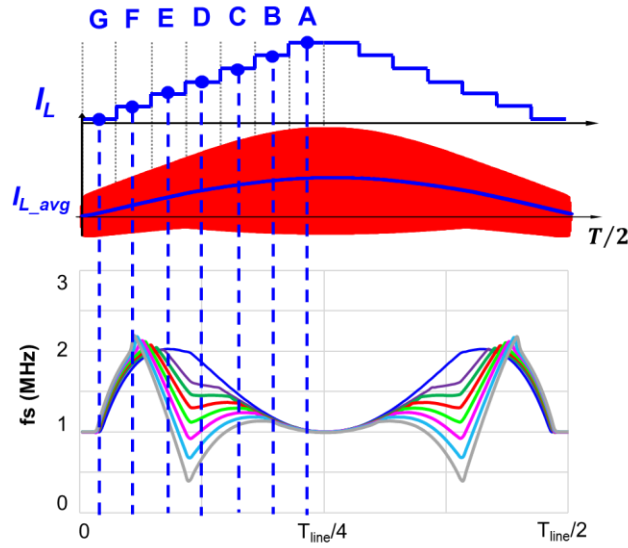
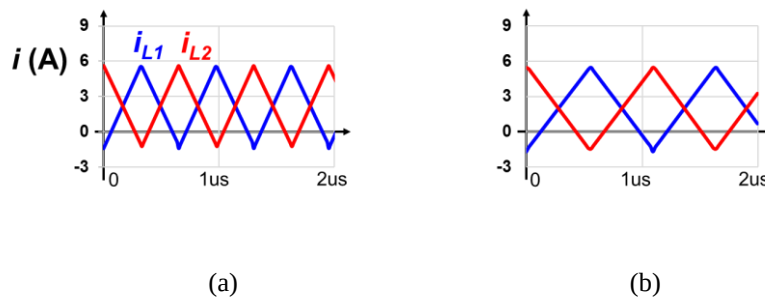


Fig. 2.15. Identifying the flux observation points of A~G in 1/4 line-cycle.



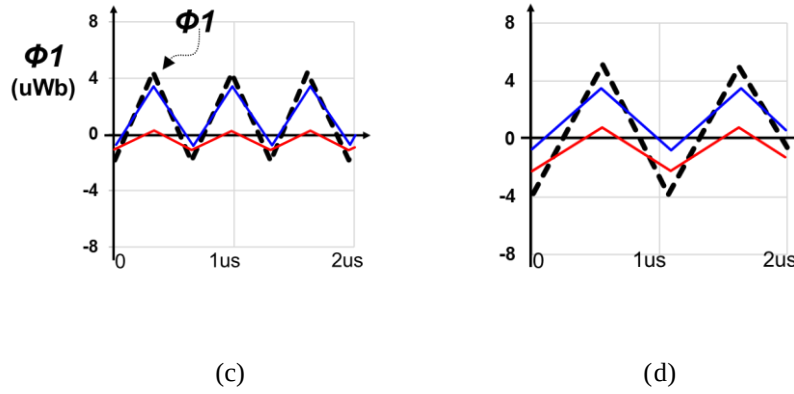


Fig. 2.16. Currents (i_{L1} and i_{L2}) and fluxes (Φ_1) for an inversely coupled inductor at point D. (a) i_{L1} and i_{L2} at $\alpha = -0.3$. (b) i_{L1} and i_{L2} at $\alpha = -0.7$. (c) Fluxes on the left-side leg at $\alpha = -0.3$. (d) Fluxes on the left-side leg at $\alpha = -0.7$.

Further investigations on fluxes of Φ_1 , Φ_2 and Φ_3 at points A-G are summarized in Fig. 2.17 to Fig. 2.23. Point A shows that the DC-biases in both legs are reduced by increasing α , while the AC fluxes almost have no change, as illustrated in Fig. 2.17. The fluxes at point B, as shown in Fig. 2.18, are similar to those at point A. Thus, the couplings of $\alpha = -0.3$ and -0.4 are eliminated because a strong DC-bias is undesirable.

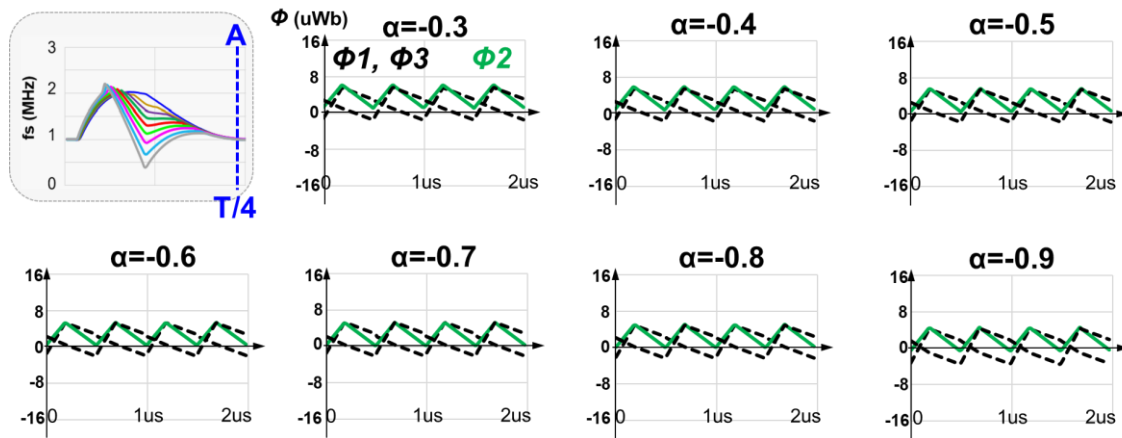


Fig. 2.17. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point A.

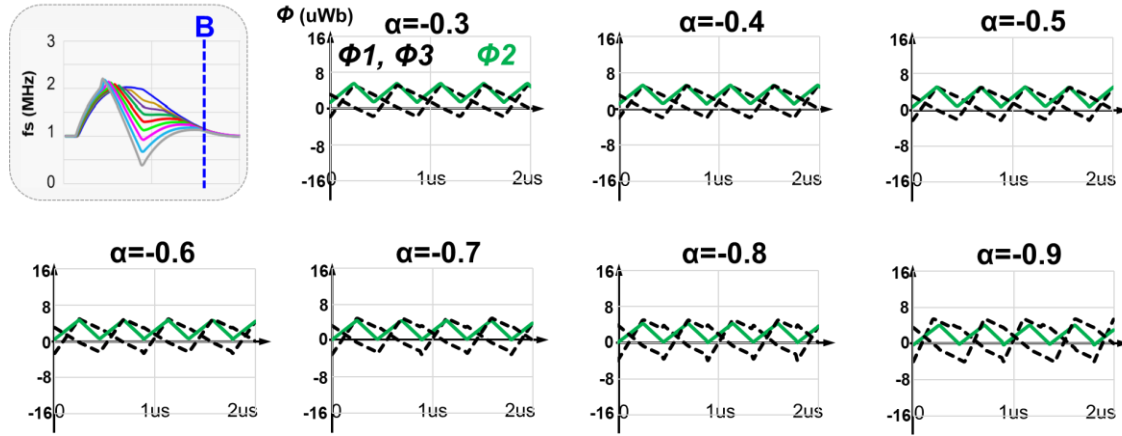


Fig. 2.18. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point B.

At point C, unwanted strong AC fluxes were observed in Φ_1 and Φ_3 for a coupling equal to and beyond -0.8, as illustrated in Fig. 2.19. Similar issues were also observed at points D and E, as shown in Fig. 2.20 and Fig. 2.21. The stronger AC flux was caused by the larger volt-sec associated with the reduced switching frequency. Based on the above analysis, the couplings of $\alpha=-0.8$ and -0.9 are undesirable.

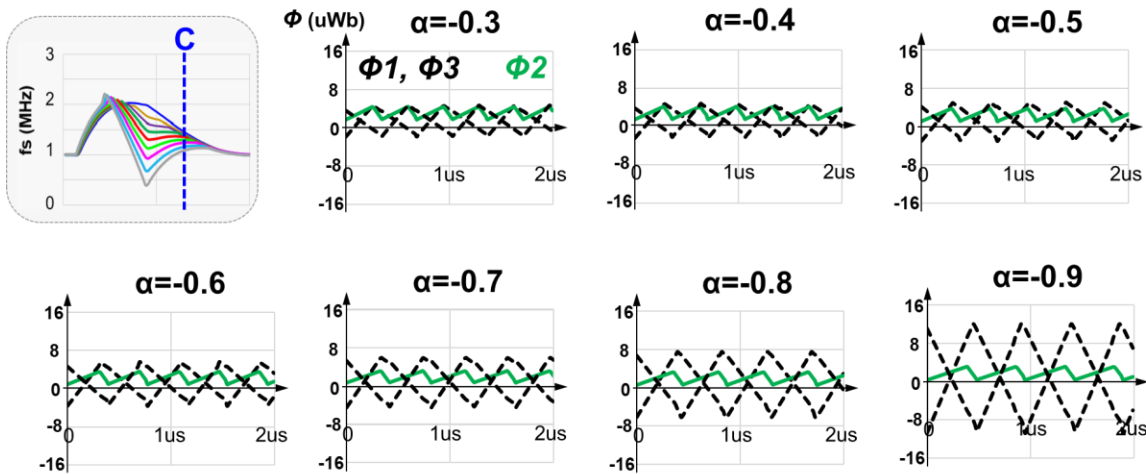


Fig. 2.19. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point C.

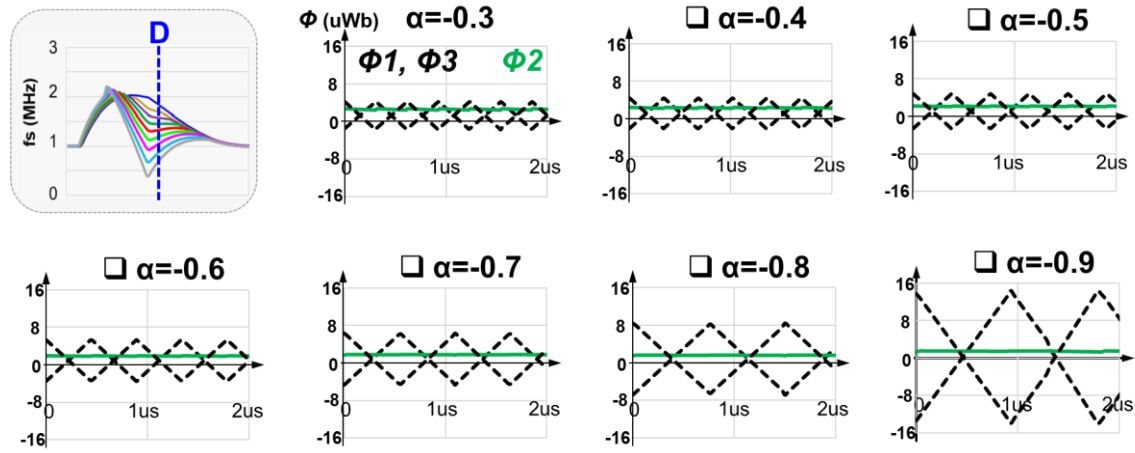


Fig. 2.20. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point D.

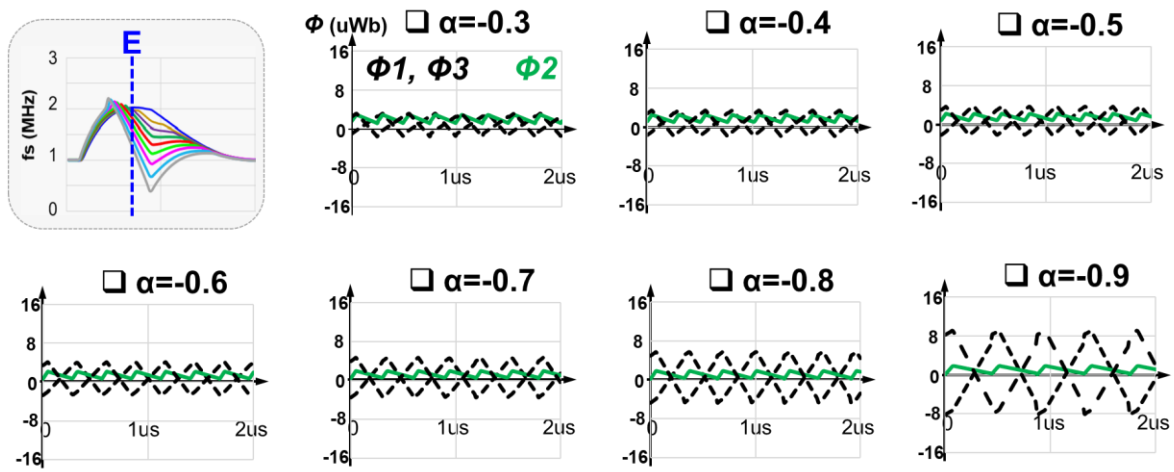


Fig. 2.21. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point E.

The fluxes at points F and G , as delineated in Fig. 2.22 and Fig. 2.23, are relatively small and have no impact on the coupling selection.

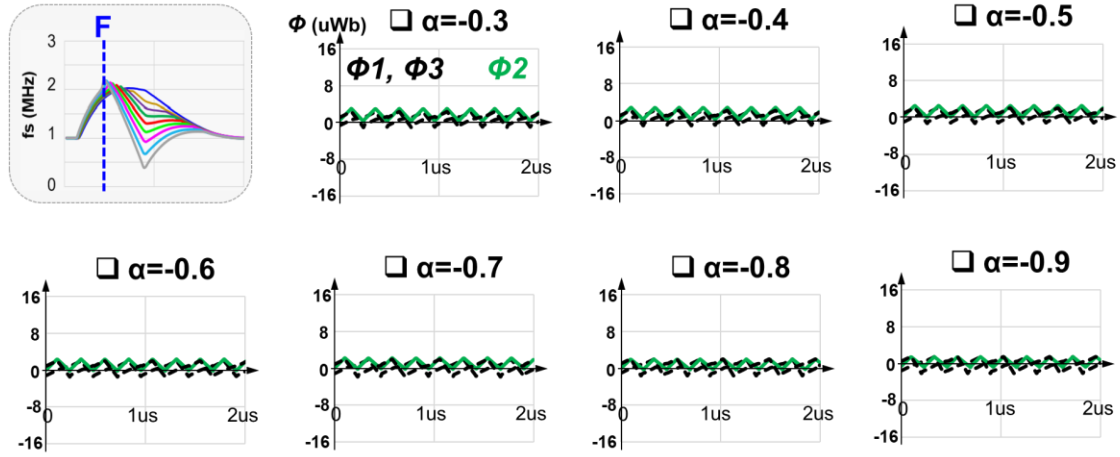


Fig. 2.22. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point F.

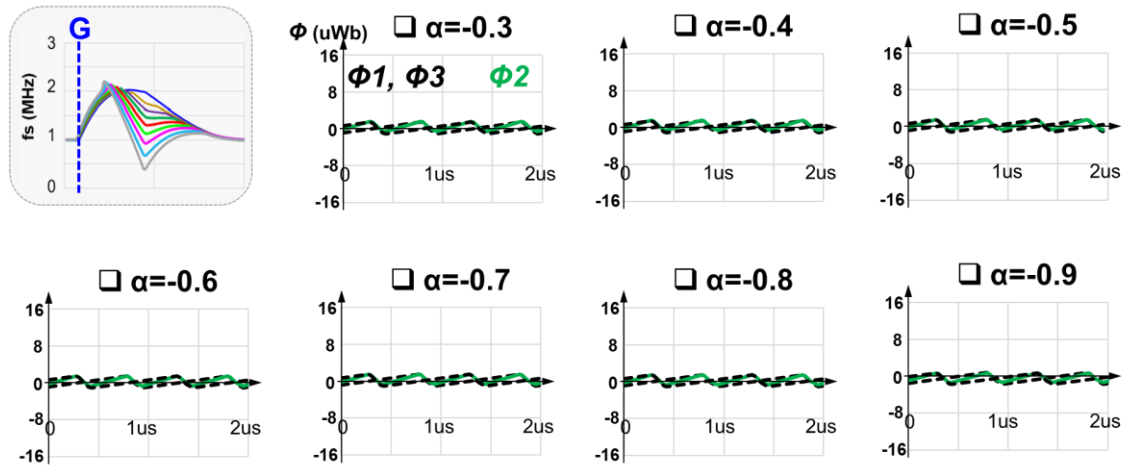


Fig. 2.23. Fluxes on the outer legs (Φ_1 , Φ_3) and the center leg (Φ_2) by varying α at point G.

Based on the above analysis, a coupling range of $-0.5 \sim -0.7$ is preferred to minimize fluxes, and thus core loss.

Coupling also has a minor effect on input ripple cancellation. This is presented in Appendix A.

A quantitative analysis of the effect of couplings on inductor losses is further performed by sweeping α . The objective is to find the optimum design with the best trade-off of inductor losses

and footprint. Given a switching frequency of 1 MHz at $T/4$, and the number of turns for each leg $N=10$, six design variables, i.e., the power loss density P_v , the coupling coefficient α , the length of the outer leg a , the width of the center leg b , the width of the outer leg d , and the width of the winding c , are identified, as shown in Fig. 2.24 (a) and (b). With those variables, the cross-section areas for outer and center legs are expressed as

$$A_{e1} = \pi \left(\frac{d}{2} \right)^2 + (a - d)d, \text{ and} \quad (2-2)$$

$$A_{e2} = ab.$$

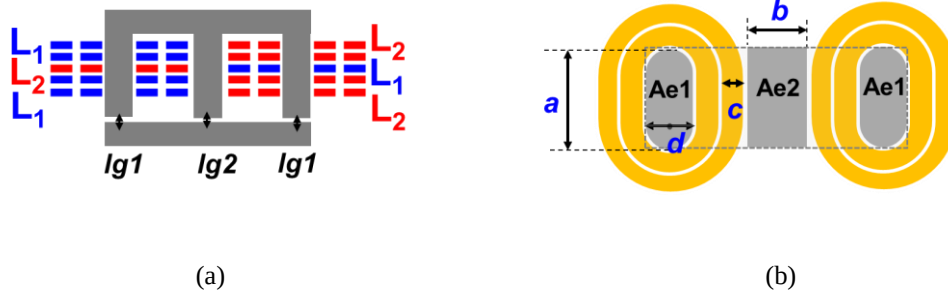


Fig. 2.24. The PCB winding-based inductor and its design variables. (a) Front view. (b) Top view.

Given $\alpha=-0.7$, the airgaps l_{g1} and l_{g2} are no longer treated as independent variables. They are functions of the self-inductance L , the coupling coefficient α , and the cross-section areas A_{e1} and A_{e2} , as

$$l_{g1} = \frac{100\mu_0}{L(1 - \alpha)} \cdot A_{e1}, \text{ and} \quad (2-3)$$

$$l_{g2} = \frac{\mu_0(68\alpha + 32)}{L(\alpha^2 - 1)} \cdot A_{e2}.$$

The derivation of l_{g1} and l_{g2} based on the reluctance model is presented in Appendix B.

Given $P_v = 500 \text{ kW/m}^3$ for both the center and outer legs, values of A_{e1} and A_{e2} are calculated in a numerical iterative process, as $A_{e1} = 51.6 \text{ mm}^2$, $A_{e2} = 68.6 \text{ mm}^2$. Thus, the variables b and d are expressed as functions of a , as shown in (2-4).

$$b = \frac{A_{e2}}{a}, \text{ and} \quad (2-4)$$

$$d = \frac{\sqrt{a^2 + (\pi - 8)A_{e1}} - a}{\frac{\pi}{2} - 4}.$$

By sweeping a and c , winding loss is calculated in a ANSYS Maxwell-based 2-D FEA simulation, and core loss is calculated in a 3-D FEA simulation. The total inductor loss, which is a summation of winding loss and core loss, and the footprint of the inductor are plotted in Fig. 2.25 (a). Over the entire range, the area around the tangential points between loss and footprint, marked in green, is the preferred design area because the inductor loss is minimized for a given footprint. The selected area is further projected to a 2-D curve with footprint as the horizontal axis and loss as the vertical axis, as shown in Fig. 2.25 (b). The shaded area is selected for a better trade-off between loss and footprint.

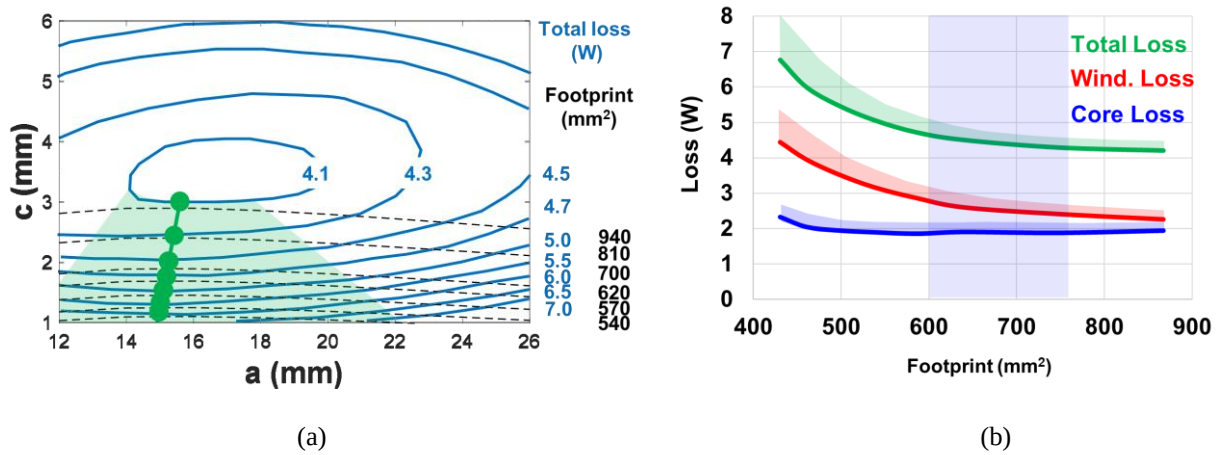


Fig. 2.25. Selecting the design area by a trade-off between loss and footprint at $\alpha = -0.7$, $P_v = 500 \text{ kW/m}^3$. (a) The PCB inductor total loss and footprint by sweeping a and c . (b) Selecting the optimal design area.

By sweeping P_v in the range of 100-900 kW/m³, a series of optimal design areas are plotted, as shown in Fig. 2.26. With a trade-off of loss and footprint, the design point with a 700 mm² footprint and a 4.5 W inductor loss is selected.

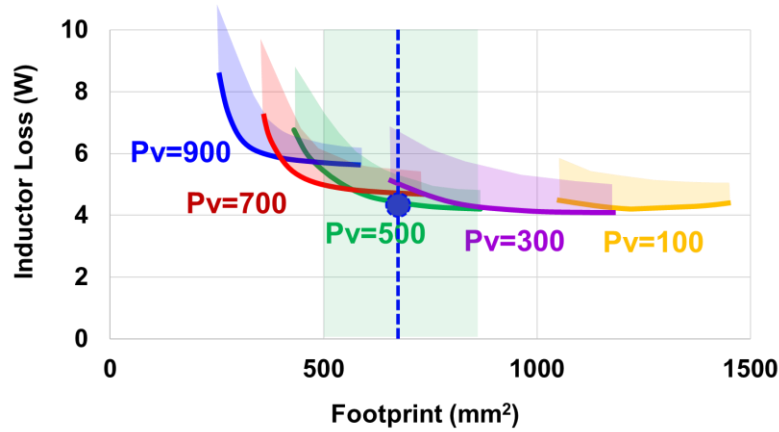


Fig. 2.26. Inductor loss versus footprint by sweeping P_v from 100-900 kW/m³ at $\alpha=-0.7$.

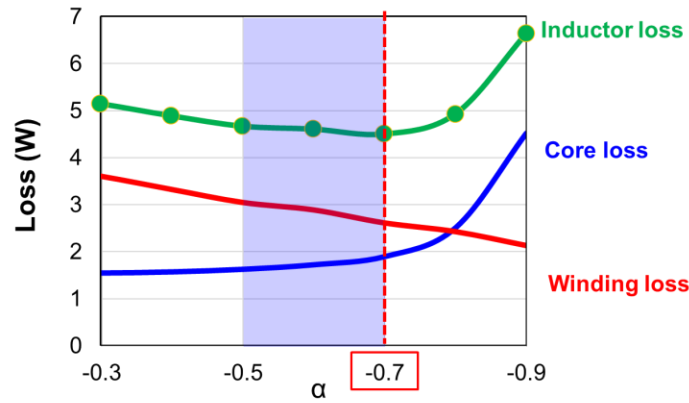


Fig. 2.27. Inductor loss by sweeping α from -0.3 to -0.9.

By repeating this process, the winding and core losses for each α from -0.3 to -0.9 were calculated. Their optimal design points are summarized in Fig. 2.27. It is noticed that, for a stronger coupling, core loss is increased while winding loss is reduced. The valley point in total inductor loss with $\alpha=-0.7$ was selected as the final design point. At this point, the selected coupling offers

a PCB winding-based inductor that has a similar loss to a conventional litz wire-based design, as shown in Table 2.3.

TABLE 2.3 INDUCTOR LOSS BREAKDOWN FOR A 1 kW PFC

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	2.6	1.9	4.5
Litz-wire inductor	2.3	2.3	4.6

2.1.2 Power Limit of a PCB-Based Inductor

The similar PCB inductor structure was further extended to 3 kW power. Given switching frequency of 300 kHz at $T/4$, the switching frequency of a 3 kW CRM PFC converter varies in a range of 300-900 kHz, as illustrated in Fig. 2.28. Similar to what was observed in the 1 kW PFC converter, a negative coupled inductor reduces switching loss by roughly 20-30%.

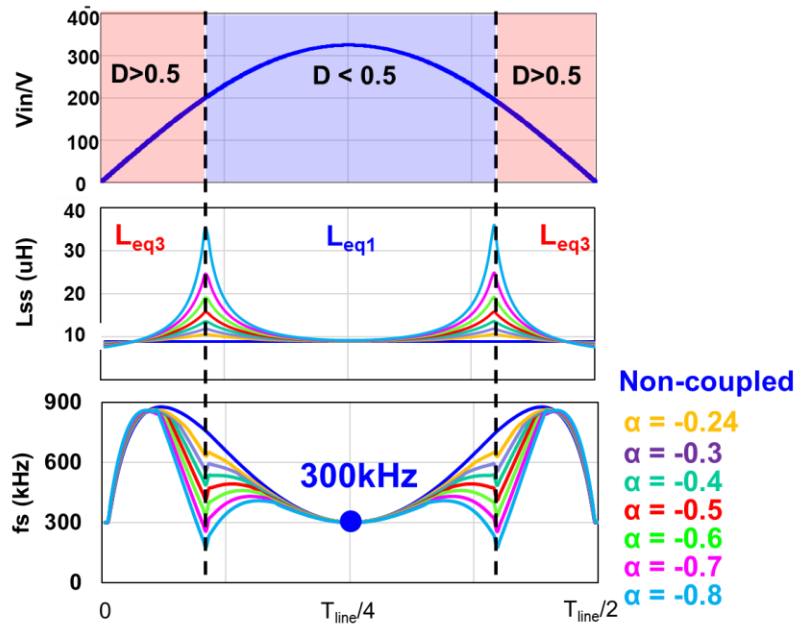


Fig. 2.28. Switching frequency in a half line-cycle for a 3 kW two phase interleaved totem-pole PFC.

Several ferrite materials from different vendors are considered as possible candidates for

building the magnetic core. Following the core loss measurement approach in [54], their power loss densities were characterized, as illustrated in Fig. 2.29. Among them, the ML95s from Hitachi Metals was selected because it has a lower P_v value compared to other materials.

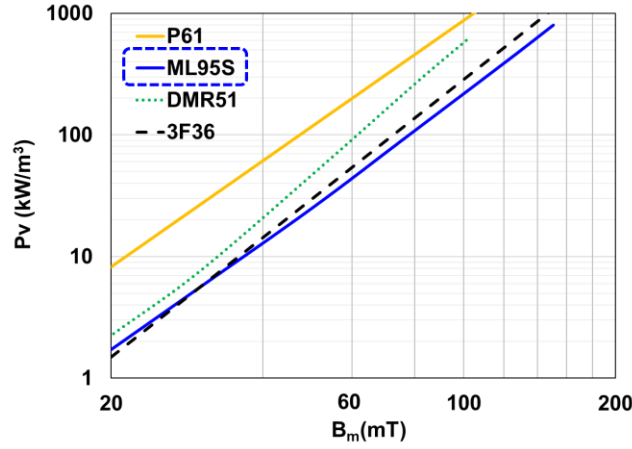


Fig. 2.29. Core loss density (P_v) at 300 kHz for several ferrite materials.

Furthermore, the effect of DC-bias on core loss is characterized following the approach in [55]. The measured P_v value as a function of H_{DC} is shown in Fig. 2.30. The DC-bias factor $k(H_{DC})$ is derived by curve fitting as

$$k(H_{DC}) = \frac{P_{v_{bias}}(H_{DC})}{P_{v_{nobias}}} = -0.0001H_{DC}^2 + 0.0475H_{DC} + 0.9769. \quad (2-5)$$

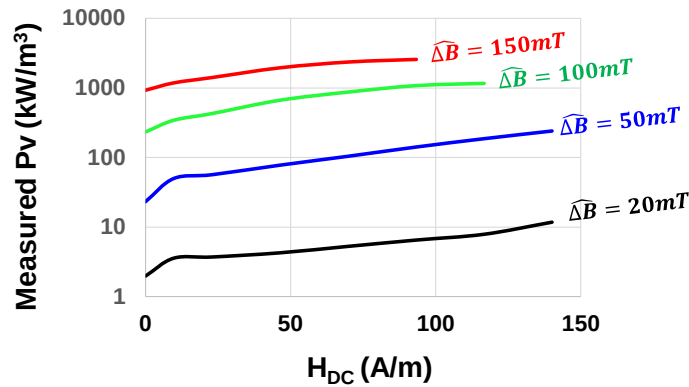


Fig. 2.30. Effect of DC-bias on P_v for ML95s ferrite material from Hitachi Metals.

With those, the core hysteresis loss density Pv_{hys} for the inductor is calculated by the equivalent elliptical loop (EEL) method [56], as

$$Pv_{hys} = k(H_{DC}) \cdot \left\{ \left| \frac{1}{C_{\alpha\beta}} \right| \cdot k \cdot \left| B_m \sqrt{1 - \left(\frac{B(t)}{B_m} \right)^2} \right|^{\beta-\alpha} \cdot \left| \frac{dB(t)}{dt} \right|^\alpha \right\} \quad (2-6)$$

where k , α , β are the Steinmetz coefficients [57] that are usually provided in datasheets. B_m is the AC flux density, and $B(t)$ is the flux density at any instant of time. $C_{\alpha\beta}$ is a constant value for given Steinmetz coefficients, as

$$C_{\alpha\beta} = (2\pi)^\alpha \cdot \frac{2}{\pi} \int_0^{\frac{\pi}{2}} \cos^\beta \theta d\theta.$$

The core eddy loss density Pv_{eddy} is calculated by

$$Pv_{eddy} = \int_{vol} \frac{J \cdot J^*}{2\sigma} dVol, \quad (2-7)$$

where σ is the conductivity of the core material, and J is the current density. Adding the hysteresis loss density and the eddy loss density yields the total core loss density Pv , as

$$Pv = Pv_{hys} + Pv_{eddy}. \quad (2-8)$$

The design objective is to find the optimum design with the best trade-off of inductor losses and footprint. Given a switching frequency of 300 kHz at T/4, and the number of turns for each leg $N=10$, six design variables, i.e., the power loss density Pv , the coupling coefficient α , the length of the outer leg a , the width of the center leg b , the width of the outer leg d , and the width of the

winding c , are identified, as shown in Fig. 2.31 (a) and (b). With those variables, the cross-section areas for outer and center legs are expressed as

$$A_{e1} = \pi \left(\frac{d}{2} \right)^2 + (a - d)d, \text{ and} \quad (2-9)$$

$$A_{e2} = ab.$$

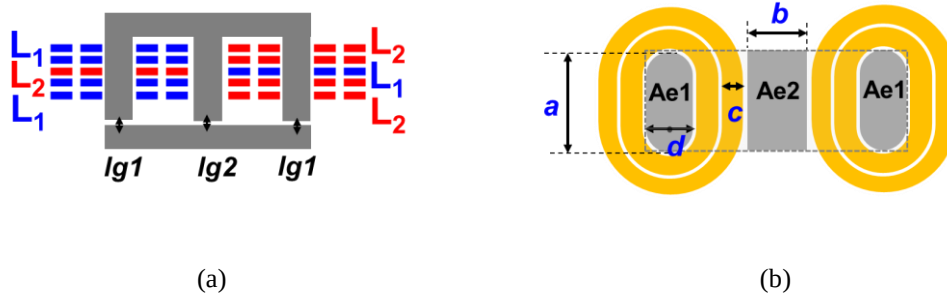


Fig. 2.31. The PCB winding-based inductor and its design variables. (a) Front view. (b) Top view.

Given $\alpha = -0.7$, the airgaps l_{g1} and l_{g2} are no longer treated as independent variables. They are functions of the self-inductance L , the coupling coefficient α , and the cross-section areas A_{e1} and A_{e2} , as

$$l_{g1} = \frac{100\mu_0}{L(1 - \alpha)} \cdot A_{e1}, \text{ and} \quad (2-10)$$

$$l_{g2} = \frac{\mu_0(68\alpha + 32)}{L(\alpha^2 - 1)} \cdot A_{e2}.$$

The derivation of l_{g1} and l_{g2} based on the reluctance model is similar to the process for the 1 kW design.

Given $P_v = 500 \text{ kW/m}^3$ for both the center and outer legs, values of A_{e1} and A_{e2} are calculated in a numerical iterative process, as $A_{e1} = 322 \text{ mm}^2$, $A_{e2} = 413 \text{ mm}^2$. Thus, the variables b and d are expressed as functions of a , as shown in (2-11).

$$b = \frac{A_{e2}}{a}, \text{ and}$$

$$d = \frac{\sqrt{a^2 + (\pi - 8)A_{e1}} - a}{\frac{\pi}{2} - 4}. \quad (2-11)$$

By sweeping a and c , winding loss is calculated in a ANSYS Maxwell-based 2-D FEA simulation, and core loss is calculated in a 3-D FEA simulation. The total inductor loss, which is a summation of winding loss and core loss, and the footprint of the inductor are plotted in Fig. 2.32 (a). Over the entire range, the area around the tangential points between loss and footprint, marked in green, is the preferred design area because the inductor loss is minimized for a given footprint. The selected area is further projected to a 2-D curve with footprint as the horizontal axis and loss as the vertical axis, as shown in Fig. 2.32 (b). The shaded area around the reflection point is selected for a better trade-off between loss and footprint.

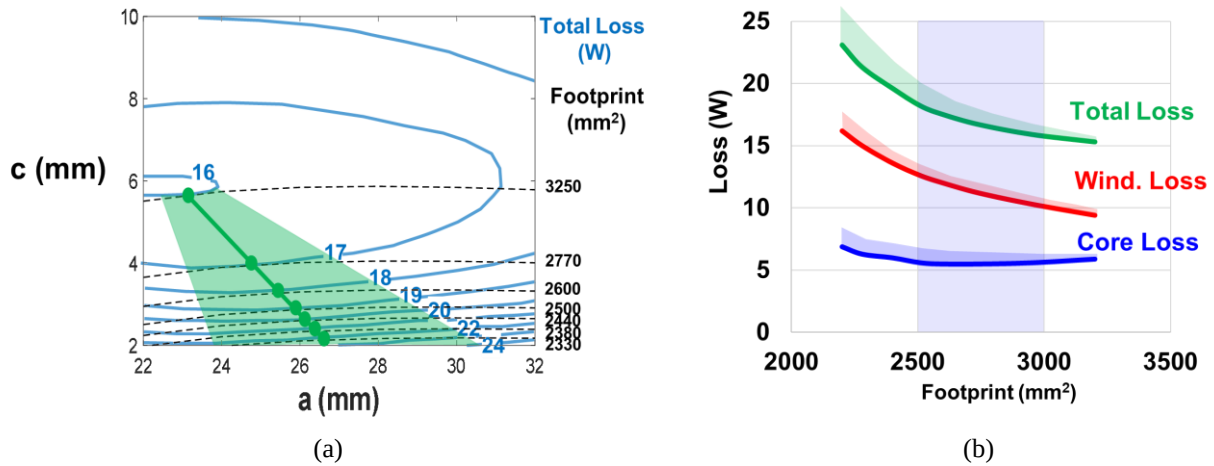


Fig. 2.32. Selecting the design area by a trade-off between loss and footprint at $\alpha=-0.7$, $P_v=500 \text{ kW/m}^3$. (a) The PCB inductor total loss and footprint by sweeping a and c . (b) Selecting the optimal design area.

By sweeping P_v in the range of 100-900 kW/m^3 , a series of optimal design areas are plotted, as delineated in Fig. 2.33. With a trade-off of loss and footprint, the design point with a 2700 mm^2

footprint and 17.3 W inductor loss is selected.

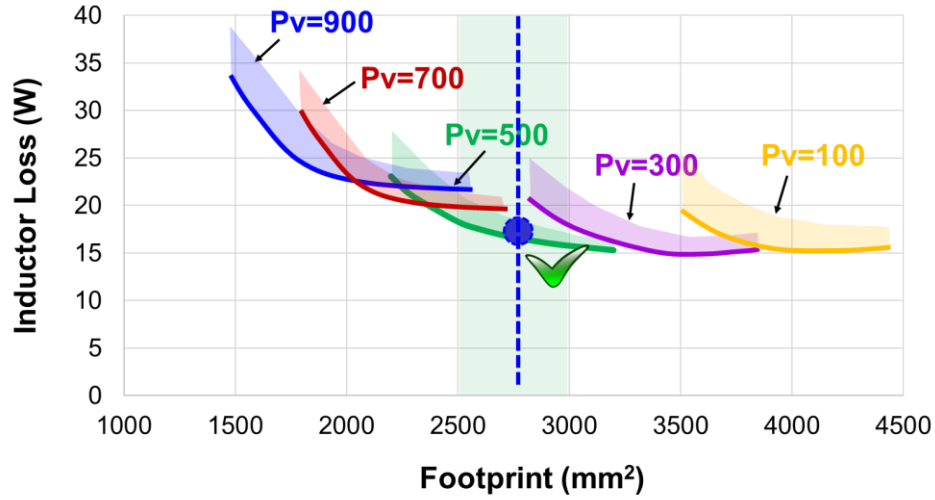


Fig. 2.33. Inductor loss versus footprint by sweeping P_v from 100- 900 kW/m³ at $\alpha = -0.7$.

By repeating this process, the winding and core losses at each α from -0.3 to -0.9 were calculated. Their optimal points were summarized in Fig. 2.34. It is noticed that, for a stronger coupling, core loss is increased while winding loss is reduced. The valley point in total inductor loss at $\alpha = -0.7$ was selected as the final design point. At this point, the inductor has a dimension of $a = 23.6$ mm, $b = 17.5$ mm, $c = 3.6$ mm, $d = 16.0$ mm, and $l_{g1} = l_{g2} = 0.5$ mm.

However, at the selected design point, the PCB winding-based inductor has a nearly 50% higher inductor loss compared to a conventional litz wire-based design, as shown in Table 2.4. In particular, the winding loss of the PCB inductor is more than 2 times higher compared to that in the litz wire windings. Thus, the high winding loss is one of the major concerns for a PCB inductor at high power.

In the following discussions, a detailed winding loss analysis by virtue of FEA simulation will be provided.

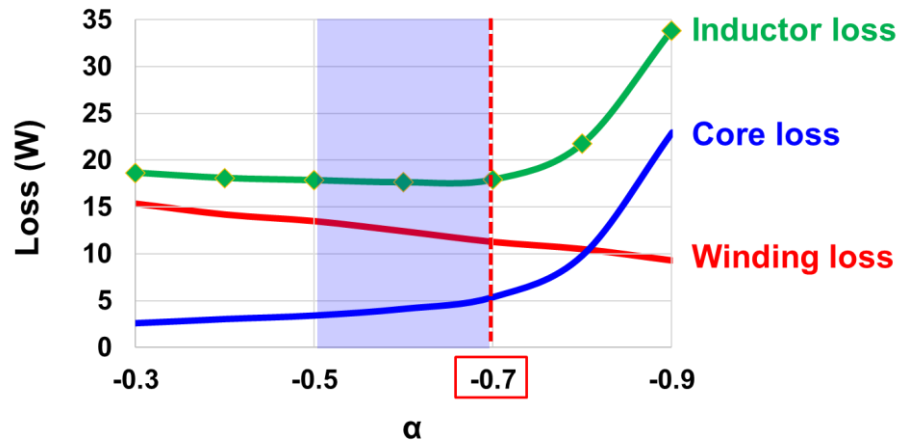


Fig. 2.34. Inductor loss by sweeping α from -0.3 to -0.9.

TABLE 2.4 INDUCTOR LOSS BREAKDOWN FOR A 3 kW PFC

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	11.8	5.5	17.3
Litz-wire inductor	5.8	6.2	12.0

By sweeping copper thickness from 0.5 to 4 oz, the winding loss of each layer, as well as the total winding loss, for the 3 kW PCB winding-based inductor were calculated, as shown in Fig. 2.35. Compared to the 1 kW PCB inductor, the winding loss of the 3 kW design increases dramatically. The large winding loss not only worsens efficiency but also potentially presents a challenge in thermal management because the PCB insulation material usually has a low thermal conductivity. Therefore, an improved design with reduced winding loss is desirable.

Fig. 2.36 shows an improved inductor structure, where the number of turns in each leg is reduced from 10 to 7, with 6 turns of L_1 and 1 turn of L_3 (two layers connected in parallel) on one leg, and likewise, L_2 and L_4 on the other leg. Since L_3 carries both currents of L_1 and L_2 , the interleaving effect remains strong. Moreover, by adding one more layer for interleaving, an enhanced MMF

cancellation effect was realized. The improved inductor structure leads to a winding loss of 9.3 W, which is 20% lower than the original, as shown in Fig. 2.37. However, a higher core loss was observed, as indicated in Table 2.5, due to the stronger flux in the magnetic core associated with the reduced number of turns. In consequence, the reduction in total inductor loss is negligible.

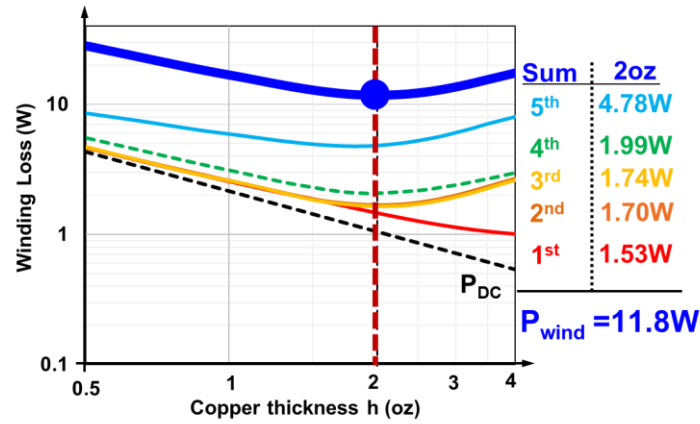


Fig. 2.35. Winding loss by sweeping copper thickness from 0.5 to 4 oz for the 3 kW PCB inductor.

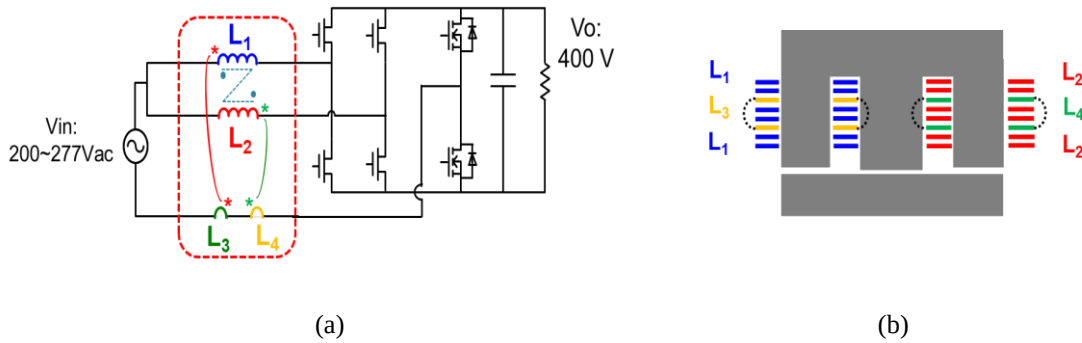


Fig. 2.36. The 3 kW PFC and its improved PCB winding-based inductor. (a) Circuit topology. (b) The improved PCB inductor structure.

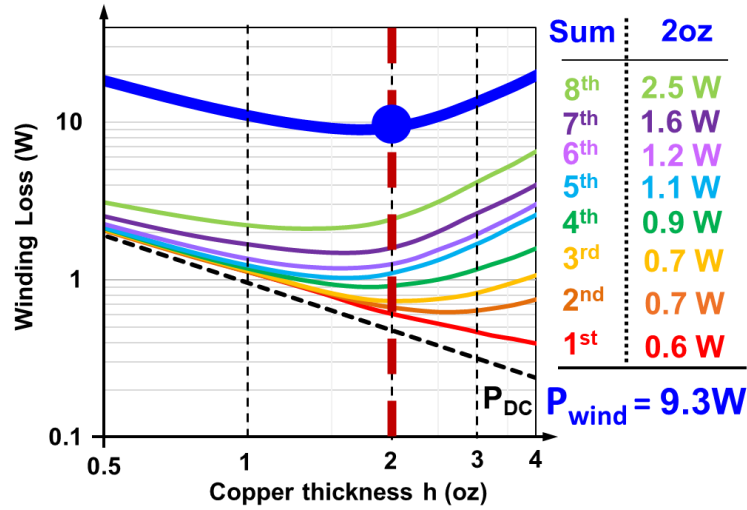


Fig. 2.37. Winding loss by sweeping copper thickness from 0.5 to 4 oz for the improved 3 kW PCB inductor.

TABLE 2.5 LOSS BREAKDOWN FOR THE IMPROVED 3 kW PCB INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	9.3	7.7	17.0
Litz-wire inductor	5.8	6.2	12.0

From the above analysis, it is observed that reducing number of turns reduces inductor winding loss but increases the core loss. Even a more balanced loss distribution between winding and core could be realized, the improvement in efficiency by reducing number of turns is negligible.

Fig. 2.38 summarizes the inductor losses in the power range of 1-3 kW. It is observed that the PCB winding-based inductor with an EI-shaped core is capable of operating below 1.5 kW, where its loss is essentially similar to a conventional litz wire-based design. Beyond that, dramatically increased loss was observed. Thus, the power limit of an EI-shaped core is roughly 1.5 kW. When extending to higher power, an improved magnetic configuration with reduced winding and core losses is desirable.

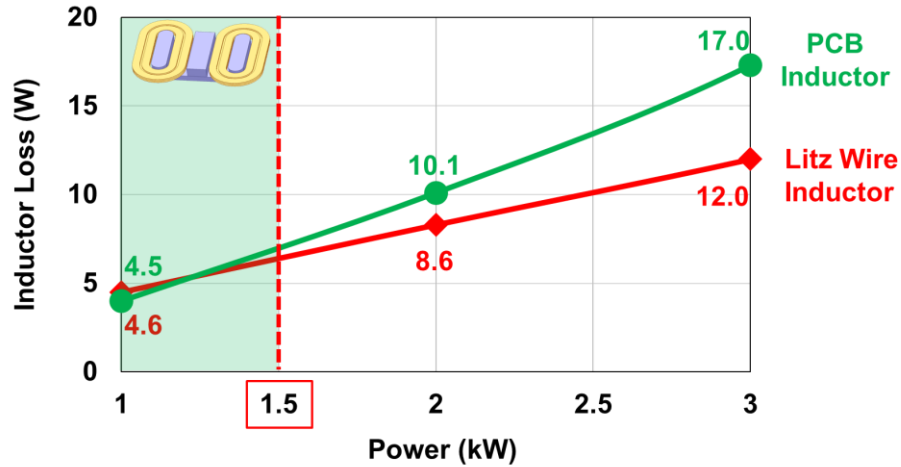


Fig. 2.38. Losses of PCB winding-based inductors in a power range of 1-3 kW.

2.2 Improved PCB-Based Inductor for Higher Power

In this section, an improved PCB inductor integration approach is proposed to circumvent the power limit of a PCB winding-based inductor. The improved structure features lower losses and a smaller volume compared to the state-of-the-art PCB inductor. Moreover, it has a good scalability and can be easily extended to a higher power range without compromising efficiency. A 3 kW PFC converter with 99% peak efficiency is built as a demonstration.

2.2.1 Modular Building Block Approach for Minimizing Winding and Core Losses

Since winding loss dominates the PCB inductor loss in the given example, as illustrated in Table 2.5, reducing winding loss is a priority for improving the design. The winding loss of a PCB-embedded inductor is proportional to MMF, which is $\Sigma(Ni)$. Thus, reducing the number of turns and inductor currents are essential for reducing winding loss. Following this idea, several approaches for minimizing winding loss are proposed.

The first approach is to reduce the current in each inductor by increasing the number of phases. When the 3 kW PFC converter is formed by four phases, as illustrated in Fig. 2.39, two sets of EI-

shaped cores are created, as shown in Fig. 2.40. In this way, the current in each winding reduces to half compared to that in the two-phase interleaving structure. As a result, the winding loss is reduced to 5.6 W based on FEA simulation, and the total inductor loss is reduced to 15.5 W, as shown in Table 2.6. However, this approach inevitably leads to a larger footprint and a more complex circuit compared to the original.

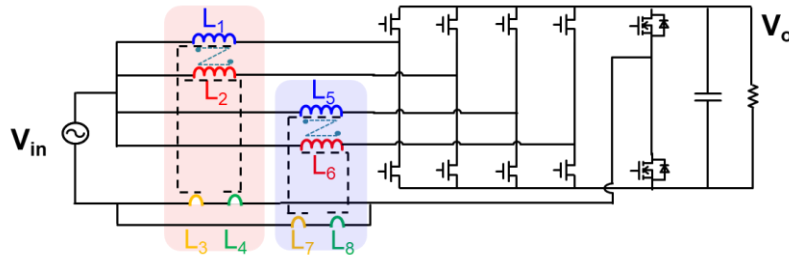


Fig. 2.39. The 3 kW PFC circuit with four phases interleaving.

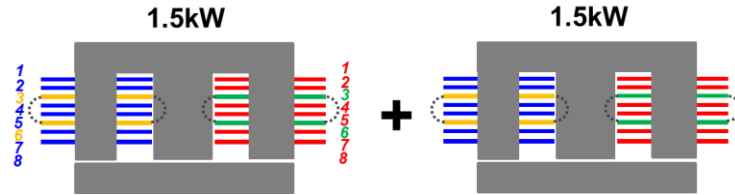


Fig. 2.40. Approach I of the PCB winding-based modular inductor.

TABLE 2.6 LOSS BREAKDOWN FOR THE APPROACH I PCB MODULAR INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	5.6	9.9	15.5
Litz-wire inductor	5.8	6.2	12.0

Another approach to minimizing the winding loss is to reduce the number of turns in each core. This was realized by dividing the single inductor in each phase into multiple inductors. One example is illustrated in Fig. 2.41, where the inductor L_1 was divided into two inductors, L_{11} and L_{12} , that are connected in series, and likewise, L_{21} and L_{22} for phase 2. In the PCB implementation,

the original EI-shaped core with an eight-layer PCB is divided into two EI-shaped cores with a four-layer PCB for each, as illustrated in Fig. 2.42. Thus, the large winding loss associated with layers 5-8 was eliminated, as illustrated in Fig. 2.43. By selecting the 3 oz copper thickness, the total winding loss was reduced from 9.3 W to 6.2 W. This value is already very close to the winding loss of a litz wire-based inductor, which is 5.8 W. The 2X here stands for the effect of two groups of cores.

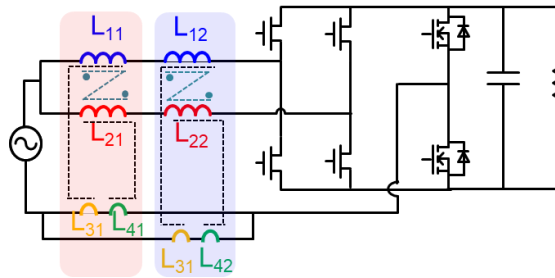


Fig. 2.41. The 3 kW PFC circuit with multi-inductor in each phase.

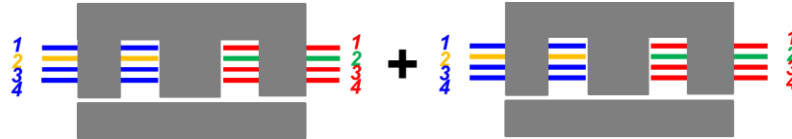


Fig. 2.42. Approach II of the PCB winding-based modular inductor.

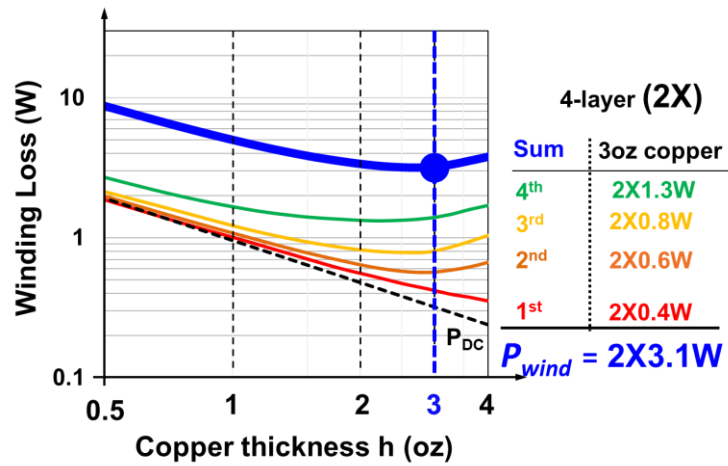


Fig. 2.43. Winding loss for Approach II of the PCB winding-based modular inductor.

However, due to the increase in core volume, the core loss is increased, and the total inductor loss is still higher than the conventional litz wire-based design, as shown in Table 2.7.

TABLE 2.7 LOSS BREAKDOWN FOR THE APPROACH II PCB MODULAR INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	6.2	9.7	15.9
Litz-wire inductor	5.8	6.2	12.0

In order to reduce the inductor core loss while still maintaining the benefits of a lower winding loss, an improved PCB inductor configuration with the modular building block concept is proposed. The first step is to break the integrated structure into multiple cores, where each elemental core has a limited number of turns. To do that, the 8-layer PCB structure for L_1 and L_3 could be divided into two elemental inductors, with a 4-layer PCB structure for each, as shown in Fig. 2.44, and likewise, another two elemental inductors for L_2 and L_4 . Those elemental inductors have a low winding loss that is similar to the value in approach II.

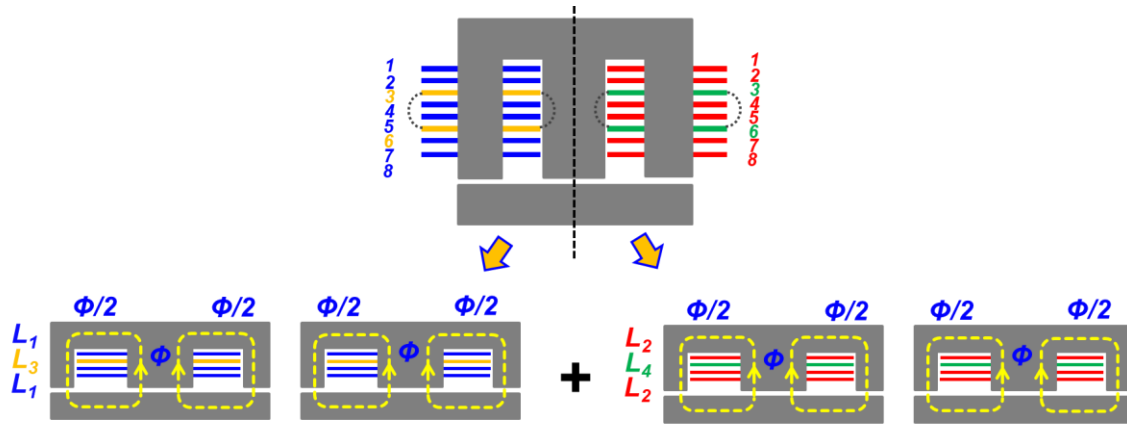
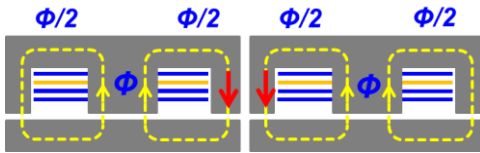
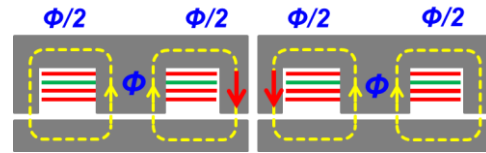
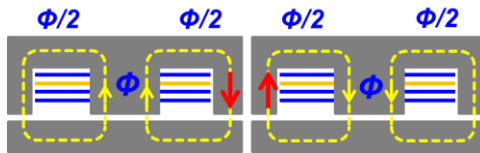
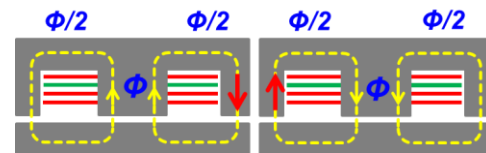


Fig. 2.44. Breaking one integrated inductor into four elemental PCB winding-based inductors.

Furthermore, those elemental inductors were integrated to reduce core size and loss by borrowing the flux cancellation concept in [58]. Taking inductors L_1 and L_3 as an example, the

integration begins with two sets of EI-cores where the magnetic fluxes in the center leg are Φ , and fluxes in outer legs and plates are $\Phi/2$, as shown in Fig. 2.45(a). If the current in one EI core is reversed, the fluxes in adjacent legs of the two EI-cores have opposite directions, as illustrated in Fig. 2.45(c). Those adjacent legs can be merged and removed due to the flux cancellation effect. In this manner, the two discrete EI-cores are integrated into one compact core structure, as shown in Fig. 2.45(e). However, by removing the adjacent legs, fluxes in the plates are doubled, resulting in thicker plates with magnetic flux concentrations occurring in the middle areas. Further improvement is evident simply by setting the airgaps in the side walls to zero in Fig. 2.45 (g). In this way, the magnetic fluxes in plates are reduced to half and are evenly distributed, and thus the plate thickness is reduced to half. Similarly, the integration of L_2 and L_4 are illustrated in Fig. 2.45 (b), (d), (f) and (h). The basic principle of choosing zero airgap in the side walls for a uniform flux distribution in plates is explained in the following discussions.

(a) Two sets of EI-cores for L_1 & L_3 .(b) Two sets of EI-cores for L_2 & L_4 .(c) Reversing fluxes in adjacent legs for L_1 & L_3 .(d) Reversing fluxes in adjacent legs for L_2 & L_4 .

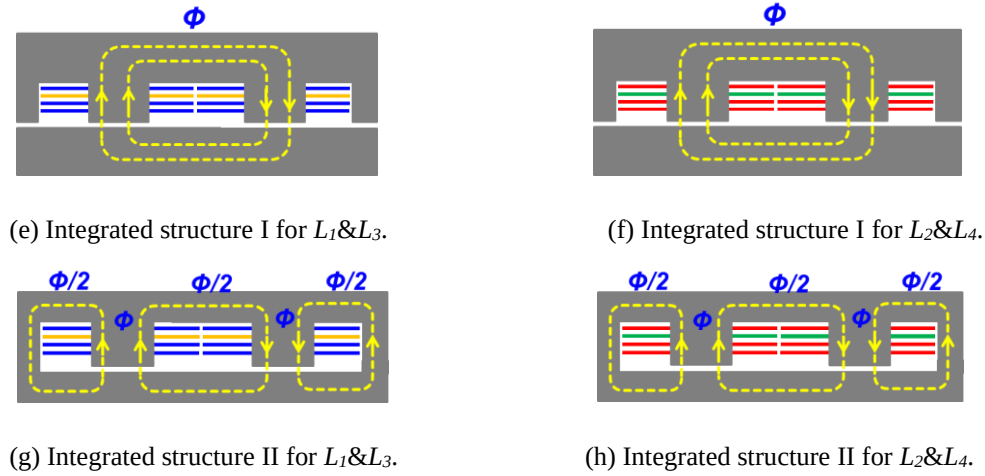


Fig. 2.45. Approach III of the PCB winding-based modular inductor.

Taking the integrated magnetics for L_1 and L_3 as an example, the core structure is redrawn in Fig. 2.46 (a), where d is the space between two middle legs, l is the distance between a middle leg and an outer wall, t is the plate thickness, h is the leg height, and l_{g1} and l_{g2} are airgaps for the middle legs and outer walls. The conditions for realizing uniform flux distribution in plates are derived based on the reluctance model, as shown in Fig. 2.46 (b), where Φ_1 , Φ_2 , and Φ_3 are fluxes in the middle legs, the outer legs (similar to outer plates), and the middle plates, respectively; Ni is the MMF for a middle leg; R_{g1} and R_{g2} are reluctances associated with airgaps in the middle legs and outer walls, respectively; R_l is the reluctance associated with the core in a middle leg; R_2 is the reluctance of the core for an outer leg and its adjacent outer plates; R_3 is the reluctance of the middle plate. The expressions for those reluctances are presented in (2-12).

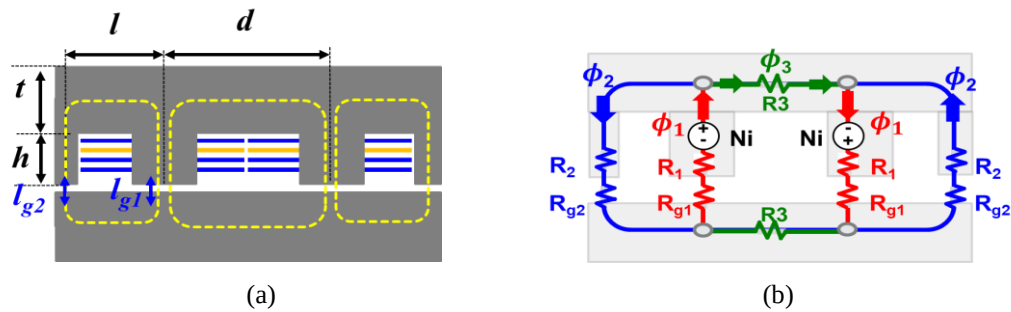


Fig. 2.46. Reluctance model for the proposed integrated PCB inductor. (a) Dimension of the magnetic core. (b) Reluctance model.

$$\begin{aligned}
R_{g1} &= \frac{l_{g1}}{u_0 A_{e1}}, \\
R_{g2} &= \frac{l_{g2}}{u_0 A_{e2}}, \\
R_1 &= \frac{h}{u_0 u_r A_{e1}}, \\
R_2 &= \frac{h + t + 2l}{u_0 u_r A_{e2}}, \text{ and} \\
R_3 &= \frac{d}{u_0 u_r A_{e2}}.
\end{aligned} \tag{2-12}$$

By solving the reluctance model, expressions of Φ_2 and Φ_3 are derived as

$$\begin{aligned}
\Phi_2 &= \frac{NI \cdot R_3}{(R_1 + R_{g1})(R_2 + R_{g2}) + (R_1 + R_{g1})R_3 + (R_2 + R_{g2})R_3}, \text{ and} \\
\Phi_3 &= \frac{NI \cdot (R_2 + R_{g2})}{(R_1 + R_{g1})(R_2 + R_{g2}) + (R_1 + R_{g1})R_3 + (R_2 + R_{g2})R_3}.
\end{aligned} \tag{2-13}$$

In addition,

$$\Phi_1 = \Phi_2 + \Phi_3. \tag{2-14}$$

Fig. 2.47 shows the normalized fluxes in plates, i.e., Φ_{2N} and Φ_{3N} , versus the ratio of $R_3/(R_2+R_{g2})$. The normalization factor is the flux Φ_1 . For a uniform flux distribution in plates, the fluxes Φ_{2N} and Φ_{3N} are expected to be the same, namely $\Phi_{2N}=\Phi_{3N}$. This is realized when $R_3=R_2+R_{g2}$. Substituting (2-12) into this condition yields

$$h + t + 2l + l_{g2}u_r = d. \tag{2-15}$$

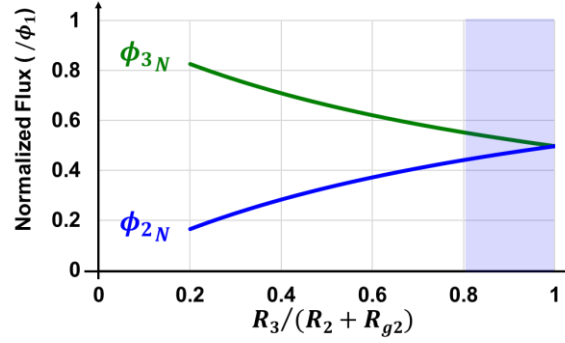


Fig. 2.47. Normalized fluxes in plates.

In (2-15), parameters h , t , l , d , and l_{g2} are dimensions of the magnetic core. They are several orders of magnitude smaller than the value of magnetic core relative permeability μ_r , which is usually close to 1000. Thus, zero airgap for the outer walls, that is $l_{g2}=0$, is essential for realizing uniform flux distributions. Furthermore, since the value of $2l$ is nearly equal to that of d , an oblong-shaped middle leg is preferred to reduce the plate thickness t . The plate length d could also be slightly extended to realize the condition in (2-15). Those values can be fine-tuned by checking the flux distribution in a 3-D FEA simulation. Knowing that realizing a ratio of $R_3/(R_2+R_{g2})$ exactly equal to 1 is not an easy task; nonetheless, it is desirable to realize a ratio in a range of 0.8-1 if at all possible, for a more uniform flux distribution, as identified in Fig. 2.47.

The final design of the proposed PCB winding-based inductors is shown in Fig. 2.48 (a), where L_1 and L_3 are integrated in one magnetic core, and L_2 and L_4 are integrated in another magnetic core. Each inductor only needs a 4-layer PCB and can be easily assembled by automation in manufacturing. The two turns for L_3 are connected in parallel to reduce the conduction loss, so as that for L_4 . Fig. 2.48 (b) illustrates the 3-D view and magnetic flux density for one magnetic core based on an FEA simulation. Since both inductors share the same structure, only the simulation result for L_1 and L_3 is presented. It is observed that the proposed integration approach

exhibits a fairly uniform flux distribution along the plate. Compared to the structure in Fig. 2.45 (e), the improved integration approach effectively reduces the profile by 40%, and the core loss by 15%.

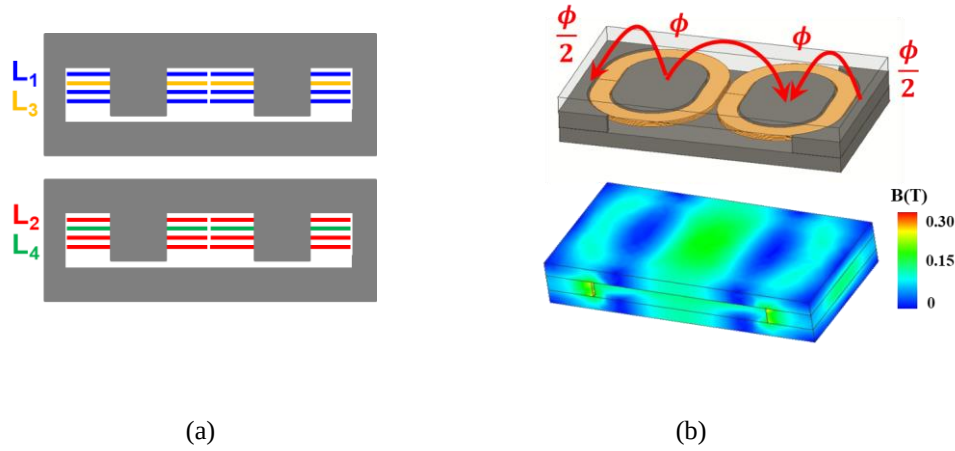


Fig. 2.48. Proposed PCB winding-based inductors for a 3 kW PFC. (a) Winding structure. (b) Magnetic flux distribution for one magnetic core (L_1 and L_3) based on FEA simulation.

A performance comparison between the approach II and III is illustrated in Fig. 2.49. At the instant of t_1 , where the current of i_{L2} reaches its peak value in a line-cycle, as shown in Fig. 2.49 (a), the flux density of approach II is plotted based on a 3-D FEA simulation, as shown in Fig. 2.49 (b). It is observed that the approach II exhibits extremely non-uniform flux distribution in the magnetic core. In particular, flux crowding has been observed at the interface between plates and legs. Those non-uniform distributed fluxes significantly increase the core loss. On the other hand, however, the approach III has a relatively uniform flux distribution, as delineated in Fig. 2.49 (c). Similarly, the flux density at the instant of t_2 , where the current of i_{L1} reaches its peak value in a line-cycle, is illustrated in Fig. 2.49 (d) and (e). The net benefit of the approach III compared to the approach II is nearly 30% core loss reduction.

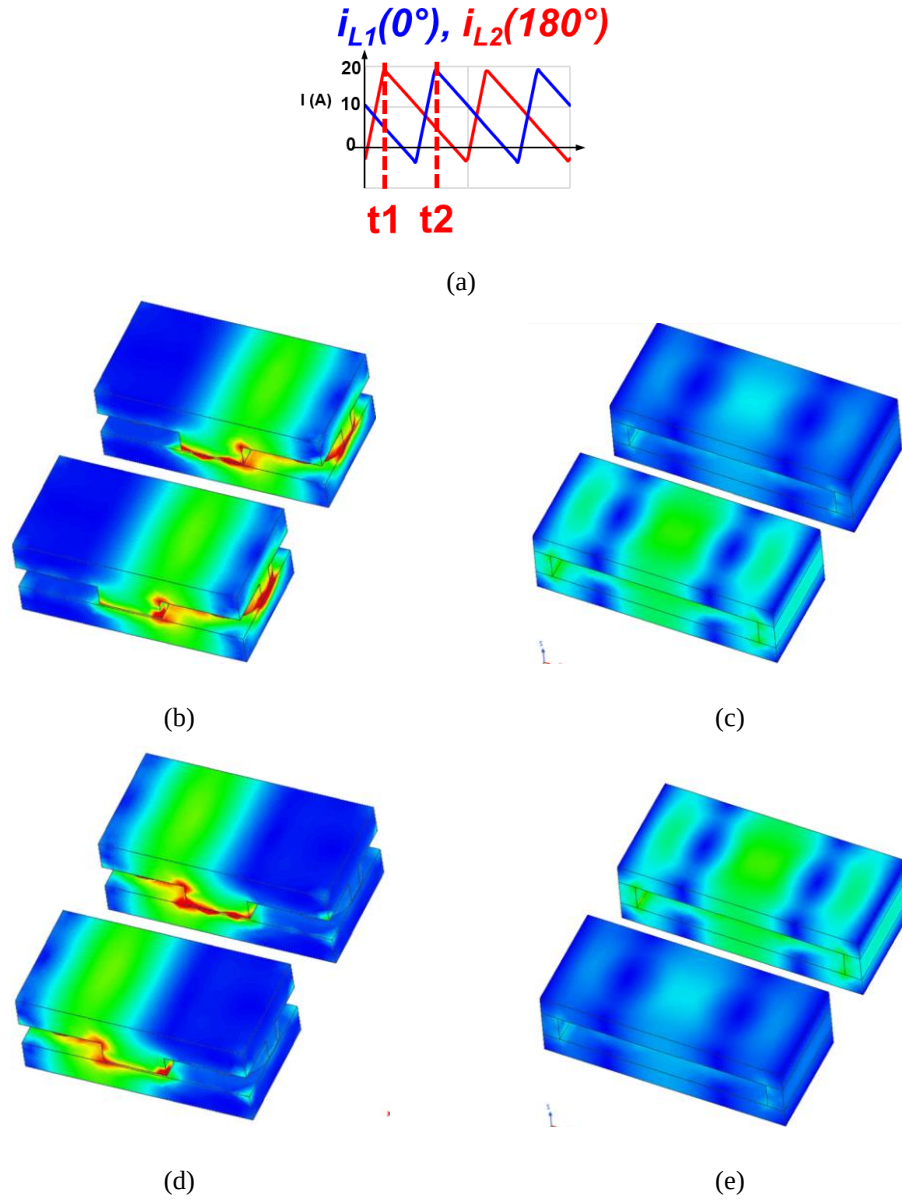


Fig. 2.49. Flux density at the instant of t_1 (i_{L2} peak current) and t_2 (i_{L1} peak current). (a) Current excitation at 1/4 of a line-cycle. (b) Flux density of approach II at t_1 . (c) Flux density of approach III at t_1 . (d) Flux density of approach II at t_2 . (e) Flux density of approach III at t_2 .

An optimal design of the proposed modular building block PCB inductor is performed. The design objective is to find the optimum dimension with the best trade-off of inductor losses and footprint. Given a switching frequency of 300 kHz at T/4, and the number of turns for each leg $N=4$, four design variables, i.e., the power loss density P_v , the length of the outer leg a , the width

of the outer leg d , and the width of the winding c , are identified, as shown in Fig. 2.50 (a) and (b).

With those variables, the cross-section area and air gap for the middle leg are expressed as

$$A_e = \pi \left(\frac{d}{2} \right)^2 + (a - d)d, \text{ and} \quad (2-16)$$

$$l_g = \frac{18\mu_0}{L_1} \left[\pi \left(\frac{d}{2} \right)^2 + (a - d)d \right].$$

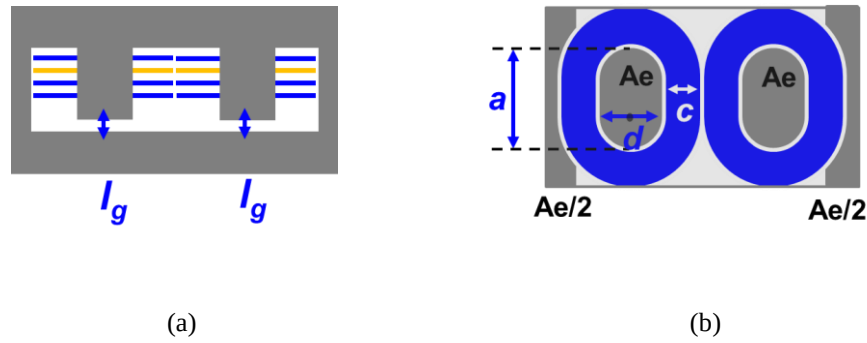


Fig. 2.50. The proposed PCB winding-based inductor and its design variables. (a) Front view. (b) Top view.

Given $P_v = 500 \text{ kW/m}^3$ for both the center and outer legs, the value of A_e is calculated in a numerical iterative process, as $A_e = 282 \text{ mm}^2$. Thus, the variable d can be expressed as a function of a , as shown in (2-17).

$$d = \frac{\sqrt{a^2 + (\pi - 8)A_e} - a}{\frac{\pi}{2} - 4}. \quad (2-17)$$

By sweeping a and c , the total inductor loss of two magnetic cores and their footprint are plotted in Fig. 2.51 (a). Over the entire range, the area around the tangential points between loss and footprint, marked in green, is the preferred design area because the inductor loss is minimized for a given footprint. The selected area is further projected to a 2-D curve with footprint as the horizontal axis and loss as the vertical axis, as shown in Fig. 2.51 (b). The shaded area around the

reflection point is selected for a better trade-off between loss and footprint.

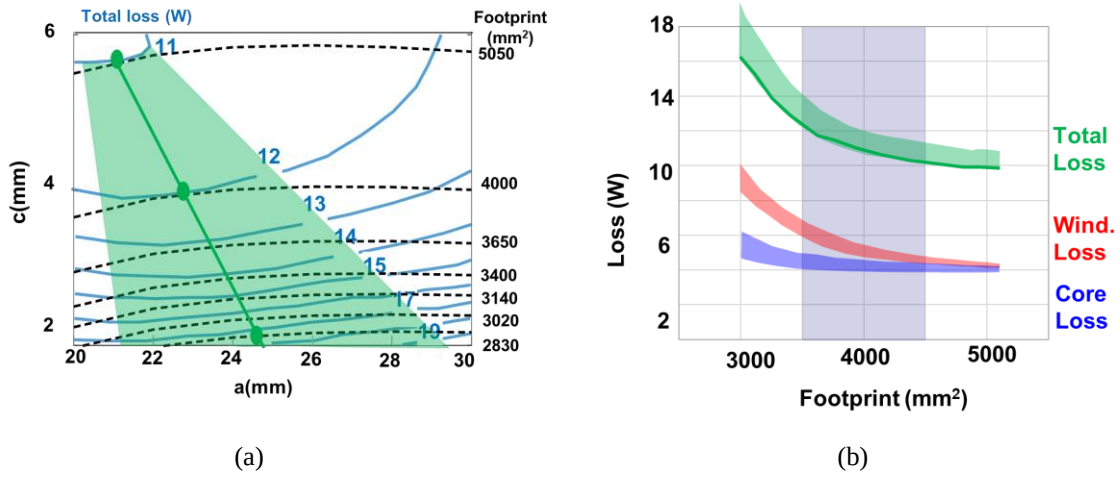


Fig. 2.51. Selecting the design area by a trade-off between loss and footprint at $P_v=500 \text{ kW/m}^3$. (a) The PCB inductor total loss and footprint by sweeping a and c . (b) Selecting the optimal design area.

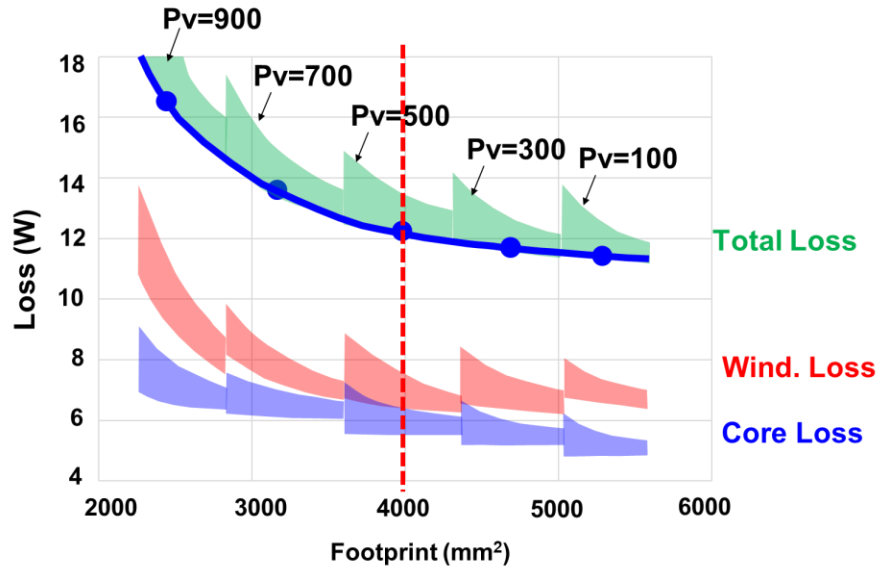


Fig. 2.52. Inductor loss versus footprint by sweeping P_v from 100- 900 kW/m^3 .

By sweeping P_v in the range of 100-900 kW/m^3 , a series of optimal design areas are plotted, as delineated in Fig. 2.52. With a trade-off of loss and footprint, the design point with a footprint of 4000 mm^2 and a total inductor loss of 12.2 W is selected. At this point, the inductor has a dimension

of $a=32.0$ mm, $c=4.0$ mm, $d=15.6$ mm, and $l_g = 1.09$ mm. The selected design offers a PCB winding-based inductor that has similar losses as those in a conventional litz wire-based design, as shown in Table 2.8.

TABLE 2.8 LOSS BREAKDOWN FOR THE PROPOSED 3 kW PCB MODULAR BUILDING BLOCK INDUCTOR

	Winding loss (W)	Core loss (W)	Total loss (W)
PCB winding inductor	6.2	6.0	12.2
Litz-wire inductor	5.8	6.2	12.0

2.2.2 Extending to Higher Power

The proposed PCB modular building block inductor has a good scalability and can be easily extended to higher power. Fig. 2.53 illustrates the proposed modular inductor designs in an extended power range up to 6 kW. The red curve represents the inductor loss of litz wire-based designs, and the blue curve exhibits the PCB inductor loss with the modular building block approach.

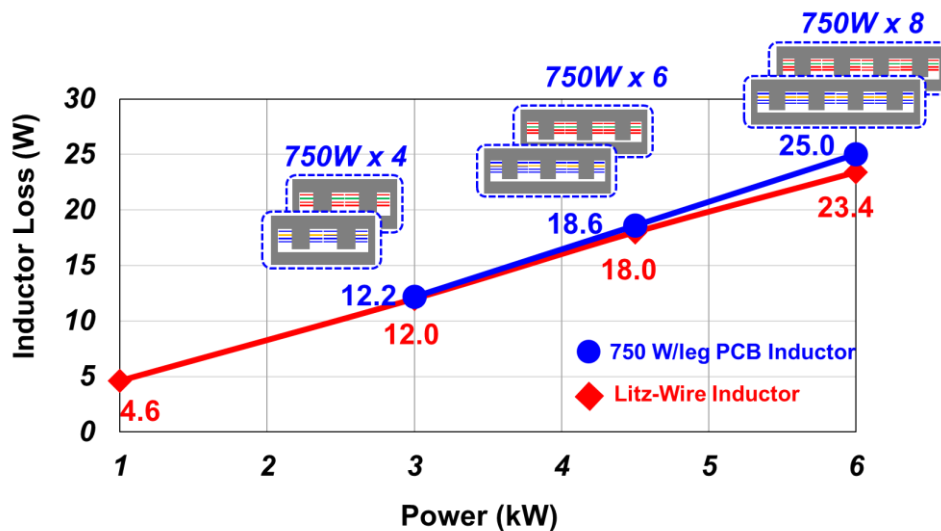
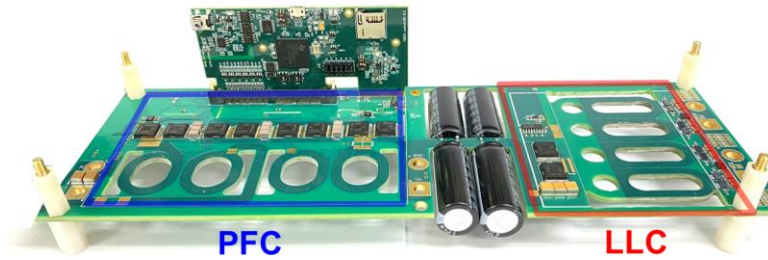


Fig. 2.53. Proposed roadmap for high-efficiency modular PCB winding-based inductors in an extended power range up to 6 kW.

The basic idea is to limit the power in each core pillar to approximately 750 W while extending the power range in the manner of adding more pillars. Thus, the 4.5 kW PCB-based inductor is built by six pillars, and the 6.0 kW inductor is built by eight pillars. In this way, the loss of a PCB inductor is close to that in a conventional litz wire-based design, based on FEA simulations. Therefore, with the proposed modular building block approach, the implementation of PCB winding-based inductors in an extended power range is feasible.

2.3 Experiment Results

With the proposed PCB-embedded inductor, a 3-kW dual-phase interleaved totem-pole PFC converter for the generation 2 data center server power supply was built, as shown in Fig. 2.54. The PFC converter features an input voltage of 200-277 V_{ac}, an output voltage of 400 V_{dc}, and a switching frequency of 300-900 kHz with CRM operation. The inductor windings were implemented in a four-layer PCB, with 3 oz copper thickness. Specific circuit parameters of the PFC converter are summarized in Table 2.9. The 400/48 V LLC converter in the following stage was introduced in [42]. The 3-kW power supply has a dimension of 28(L)× 9(W)× 1.8(H) in cm. It features an extremely low profile and realizes a power density of 110 W/in³ without the controller. The power density for the PFC converter alone reaches 300 W/in³.



(a)

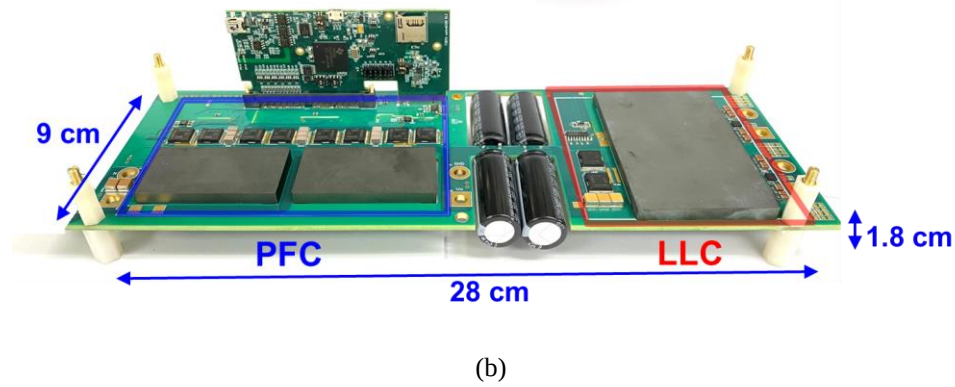


Fig. 2.54. Hardware prototype of the 3-kW data center server power supply. (a) Without magnetic cores. (b) With magnetic cores.

TABLE 2.9 SPECIFICATIONS OF THE PFC PROTOTYPE

Component	Parameter
Switching frequency	300-900 kHz
L_1 and L_2	7.3 μ H
L_3 and L_4	0.2 μ H
GaN device	IGT60R042D1
GaN device driver	Si8273
60 Hz switch	IPT60R028G7
Controller	TMS320F28379

The key experiment waveforms for the PFC converter at $V_{in}=230$ V_{ac}, $V_o=400$ V_{dc} are shown in Fig. 2.55. From top to bottom are the drain-source voltage for the main switch V_{DS} , the input voltage V_{in} , and the inductor currents i_{L1} and i_{L2} . It is observed that a good current sharing between the two phases was realized. The thermal measurement result under full load, 25 °C ambient temperature, and air-cooling conditions is shown in Fig. 2.56. A fan was placed close to the right side of the hardware to provide an air velocity of approximately 6 m/s. Three hotspots on the picture are identified, where the highest temperature of 55.1 °C appears on the GaN devices in one phase at hotspot 1. The GaN devices in the other phase, as marked by hotspot 2, have a slightly lower temperature of 52.1°C because they are closer to the fan. It should be noticed that those measurements were conducted under the condition without heatsink. Thus, devices in both phases

operated within the safe temperature range. The surface of the magnetic core, as labeled by hotspot 3, had a temperature of only 31.1 °C. It proves that the proposed PCB inductor design has a high efficiency and a good thermal performance. Moreover, the high surface area to volume ratio achieved by using planar magnetic cores results in more efficient thermal conduction and leads to a lower temperature rise compared to conventional wire-wound components.

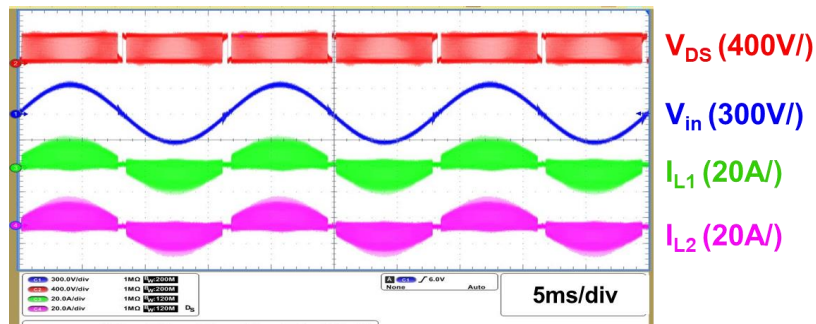


Fig. 2.55. Key experiment waveforms of V_{DS} , V_{in} , I_{L1} , and I_{L2} for the 3 kW PFC converter at $V_{in}=230$ V_{ac}, $V_o=400$ V_{dc}.

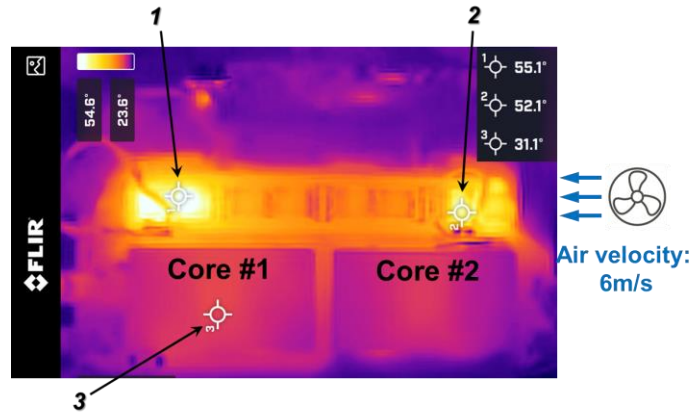


Fig. 2.56. Thermal measurement results at full load for the PFC converter. The hotspots 1 and 2 mark the surface temperature of GaN devices. The hotspot 3 marks the temperature on the surface of the magnetic core for one inductor.

The measured efficiency of the PFC converter is shown in Fig. 2.57 (a). A peak efficiency of 99% was realized at 75% load, and an efficiency of 98.8% was realized at full load. The converter loss breakdown at full load, as shown in Fig. 2.57 (b), indicates that the device loss dominates the converter loss with a value of 23.1 W. In addition, inductor contributes a loss of 12.2 W.

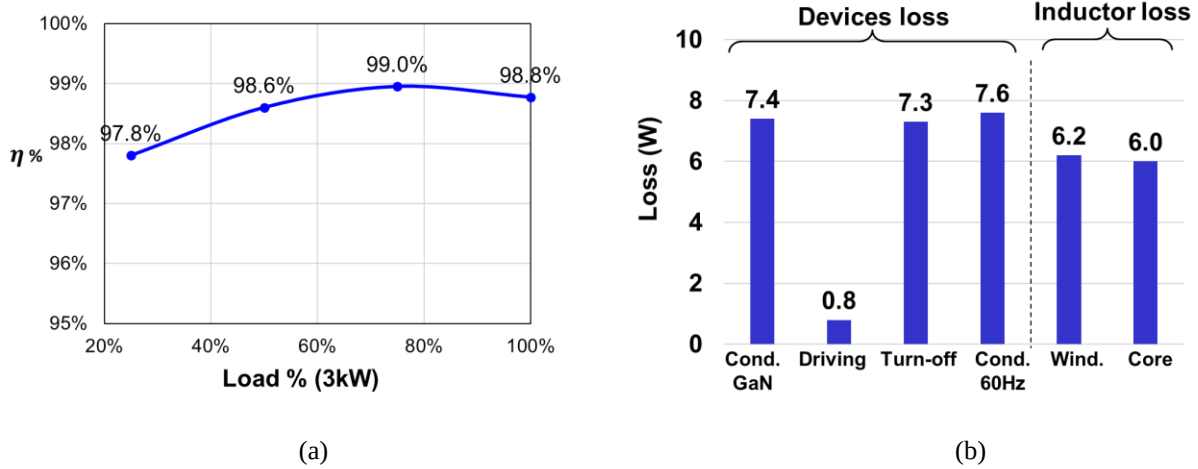


Fig. 2.57. Efficiency and loss breakdown for the 3 kW PFC converter. (a) Measured efficiency. (b) Loss breakdown at full load.

2.4 Summary and Conclusions

The PCB winding-based inductor has fundamental limitations in terms of the power handling capability. The winding loss is proportional to MMF, which is Ni . That is to say, with the number of layers (turns) and currents increased, winding loss is increased nonlinearly. Furthermore, for a large size core, uniform flux is difficult to achieve using planar structure. In addition to the hysteresis loss, there are even high DC bias related loss and eddy current loss. Those factors cause dramatically increased winding and core losses, and limit the implementation of PCB winding-based inductors in high power range.

To circumvent the limits, a PCB winding-based modular building block approach is proposed, where the integrated PCB inductor is formed by an array of pillars. Each pillar handles roughly 750 W of power. The winding loss is minimized by limiting the number of turns for each pillar. The core loss is minimized with a proposed planar magnetic structure where rather uniformly distributed fluxes were observed in the magnetic core. The proposed inductor was demonstrated on a 3 kW PFC converter for generation 2 data center server power supplies. The PFC converter

realizes a peak efficiency of 99% and a power density of 300 W/in³. Meanwhile, the proposed design can be easily assembled with automation in manufacturing, leading to much reduced labor and costs.

The proposed design also features a good scalability and can be easily extended to a higher power range without compromising efficiency. Design examples up to 6 kW are provided. Their effectiveness in improving performances for high power converters will be verified in future works.

Chapter 3 Improved Balance Technique for CM Noise Reduction

Symmetry and cancellation techniques are often employed to suppress CM noises in switching power converters. In addition, a shielding technique [38] has been demonstrated effectively to suppress CM noises for an isolated converter with a PCB-based transformer design. However, for non-isolated converters, such as PFC circuits, none of the techniques mentioned above are deemed applicable or justifiable. Recently, the balance technique has been demonstrated to effectively suppress CM noises up to the point where the parasitic ringing between the inductor and its winding capacitor is observed [25], [45]. This chapter presents an improved balance technique in a PCB-based coupled inductor design that compensates the detrimental effect of the interwinding capacitors. In the given example, CM noise suppression is effective in the frequency range of interest, up to 30 MHz. A CM noise model is established to substantiate the measurement results.

3.1 Review of CM Noise Reduction Techniques

For an off-line power supply, in general the DM noises are dominated by the PFC rectifier. Interleaving technique [59] is often used to suppress DM noises. CM noises are generally caused by high dv/dt noise sources coupled with distributed parasitic capacitances between converters and the earth ground. In this case, both PFC and DC/DC converters contribute to the unwanted CM noises.

For CM noise suppression, the choice of converters with symmetrical topologies is preferred [60]. By virtue of symmetry, a CM noise current is cancelled by a complimentary noise source. The commonly used PFC topologies are asymmetrical in nature. For asymmetrical topologies,

other means are required to suppress CM noises. To create a symmetrical structure for a PFC, additional components are required [44], [61]. An example is shown in Fig. 3.1(a) [44], where C_a , C_b , C_c and C_d are parasitic capacitors between the converter and the earth ground, and C_{add} is an extra capacitor for impedance finetuning. The CM noises were effectively suppressed, as shown in Fig. 3.1(b). However, the additional circuitry introduces higher loss and cost, and is therefore deemed not justifiable.

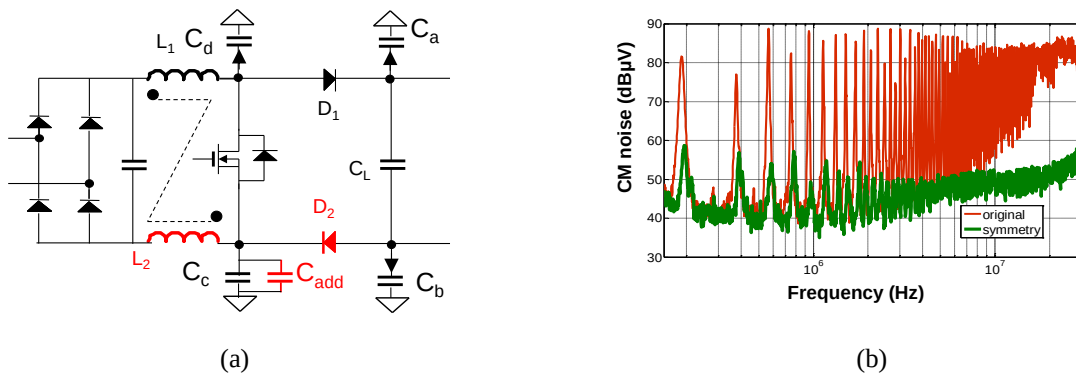


Fig. 3.1. Symmetry technique in a boost PFC. (a) Adding L_2 , D_2 and C_{add} . (b) CM noise measurement with and without symmetry technique.

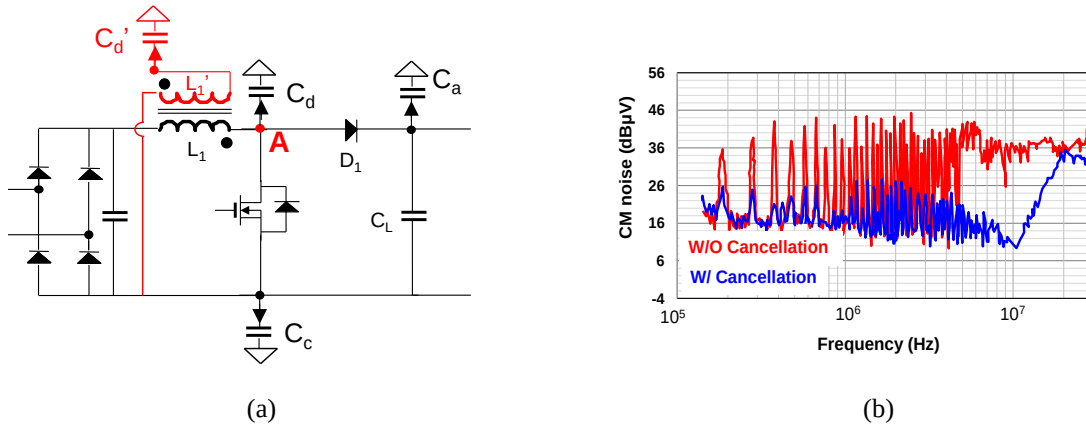


Fig. 3.2. Cancellation technique in a boost PFC. (a) Adding L_1' and C_d' . (b) CM noise measurement without and with cancellation technique.

Cancellation technique is also a frequently used technique for CM noise suppression [62]-[63]. The concept of cancellation is to create another CM noise source in such a manner to cancel the

original CM noise. One example of the cancellation technique is shown in Fig. 3.2 (a) [62]. In this technique, node A is identified as a main source of CM noises. A coupled winding to inductor L_1 is employed to create a counter CM noise current. As shown in Fig. 3.2 (b), this technique was demonstrated effectively up to the point where parasitic ringing took over. It should be noted that Fig. 3.2 (b) is a reproduction of the original Fig. 4 (a) and Fig. 7 in reference [62].

The third approach to reduce CM noises is the balance technique introduced by Wang [25]. When applying the balance technique to PFC, the boost inductor was split into two, L_1 and L_2 , as shown in Fig. 3.3 (a). The CM equivalent circuit of Fig. 3.3 (a) is shown in Fig. 3.3 (b), which resembles that of the Wheatstone bridge.

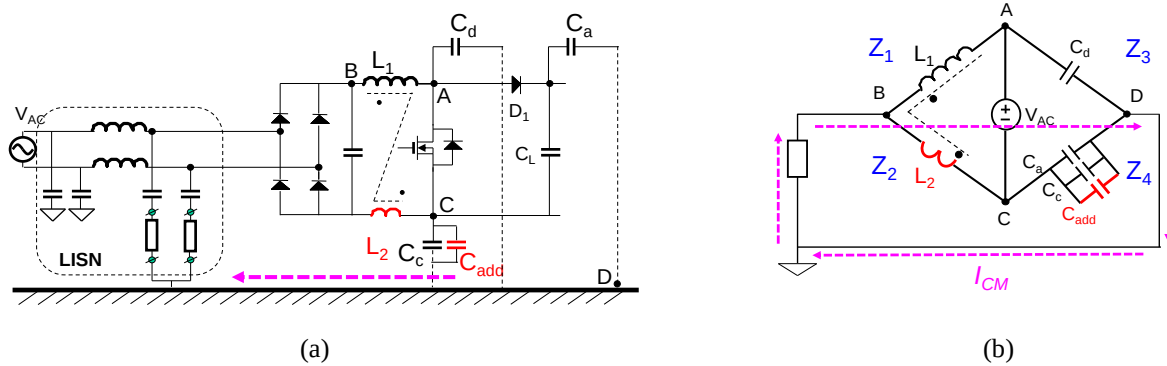


Fig. 3.3. (a) Applying balance technique to a boost converter operating at 100 kHz. (b) CM noise equivalent circuit.

When the balance condition $Z_1/Z_2 = Z_3/Z_4$ is satisfied, the voltage potential at point B is equal to that of point D. In this case, the CM noise current I_{CM} is zero.

When applying balance technique, it is important to note that the impedance of the ground loop, as shown in Fig. 3.3 (b), formed by the power return path and earth ground, is increased by the introduction of L_2 . Potential parasitic oscillation in the ground loop could occur well within 30 MHz frequency range. For this reason, L_2 was implemented using a single turn inductor, as shown in Fig. 3.4 (a) [44]. Fig. 3.4 (b) shows the experimental result in a 600 W boost PFC converter

[44]. In this case, the CM noise was effectively suppressed up to 4-5 MHz, prior to resonant frequency of the ground loop which occurred around 5-6 MHz. In this example, the resonant frequency appeared to be relatively low because a large capacitor C_{add} (417 pF) was added to Z_4 to satisfy the balance condition. Furthermore, it should be noted that the coupling coefficient of L_1 and L_2 is not strong (around 0.7) in this conventional litz wire-based inductor design. Thus, the parasitic ringing frequency of L_1 is not truthfully reflected to Z_2 . Therefore, the ratio of Z_1/Z_2 failed to remain constant at and beyond the parasitic ringing frequency. While Z_3 and Z_4 are impedances associated with the parasitic capacitors. The ratio Z_3/Z_4 essentially remains constant in the frequency range of interest.

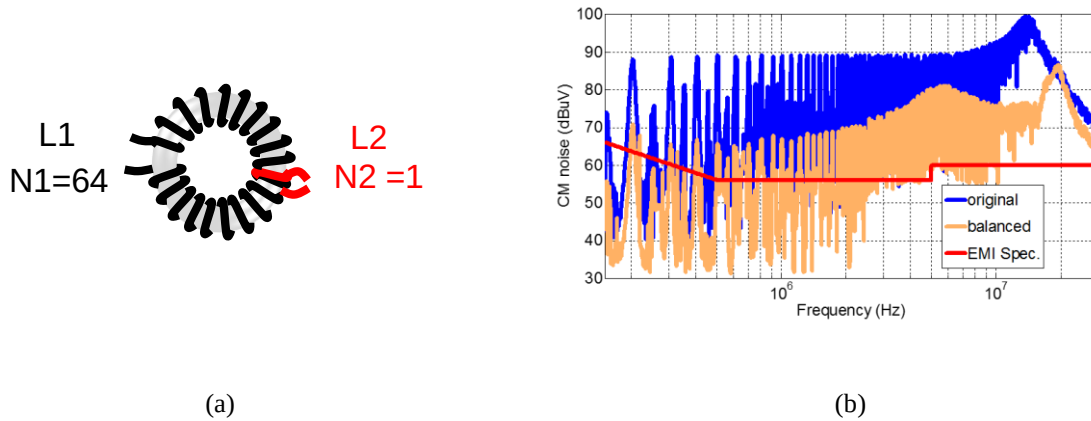


Fig. 3.4. Balance technique in a boost PFC. (a) Implementation of L_1 and L_2 . (b) CM noise measurement.

It suffices to note that the coupling between L_1 and L_2 should be as strong as possible. If L_2 is strongly coupled to L_1 , Z_2 would be merely an image of Z_1 in a reduced scale by the turns ratio. In the conventional design, a large number of turns are used in L_1 while a single turn is used in L_2 , the coupling between L_1 and L_2 is weak and is inadequate to satisfy the balance condition. However, when the inductors are implemented in the form of PCB, the above-mentioned limitations can be addressed. This will be further discussed in Section 3.2.

3.2 Balance Technique Applied to PCB-Based Inductors

In this section, the balance technique is applied to the PCB-based inductors design of a PFC circuit using GaN power devices. Prior art [45] related to the PCB-based design is reviewed, and the effectiveness of the CM noises suppression using balance technique is analyzed. Furthermore, the root cause for the failure to achieve the expected outcome is identified.

3.2.1 Prior Art: Implementation of Balance Principle in PCB-based Inductors

A GaN device-based PFC converter with PCB-based balance technique was introduced in [45]. Inductors L_3 and L_4 were added to the return path to build a balanced circuit, as shown in Fig. 3.5. In PCB implementation, one turn of L_1 and L_2 each was replaced with L_3 and L_4 respectively, as illustrated in Fig. 3.6. These four inductors were integrated into a single EI-shaped core.

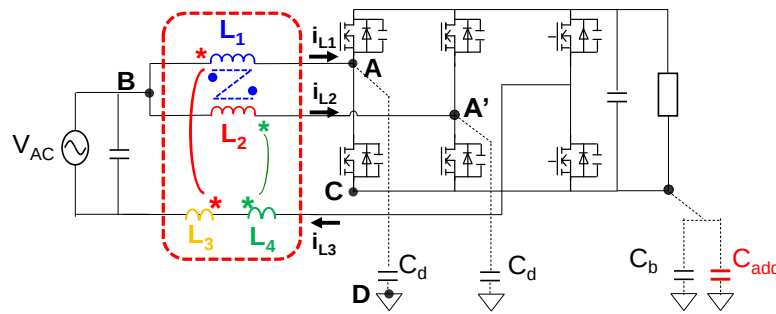


Fig. 3.5. The GaN-based dual-phase interleaved totem-pole PFC rectifier operating at 1-2 MHz with balance technique.

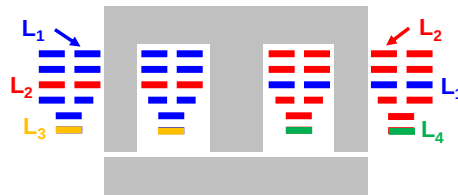


Fig. 3.6. The coupled inductor structure proposed in [45]. The coupling coefficients between inductor L_1 and L_2 , and L_1 and L_3 , are $\alpha_{12} = -0.7$ and $\alpha_{13} \approx 0.96$ respectively.

The CM noise equivalent circuit for the dual-phase PFC is shown in Fig. 3.7 (a), where two

noise sources, V_{s1} and V_{s2} , were identified. By applying superposition theory, the CM noise model for V_{s1} and its equivalent circuit in the Wheatstone form were generated, as shown in Fig. 3.7 (b) and (c). The dotted line represents couplings among various inductors.

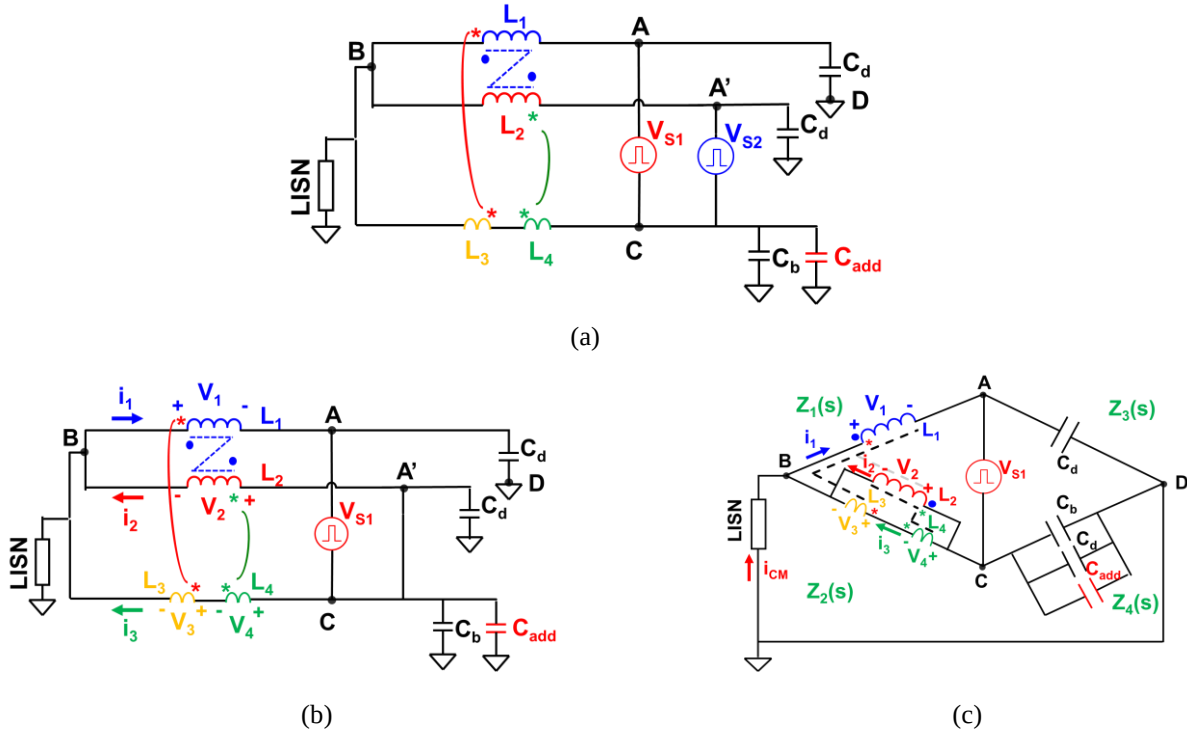


Fig. 3.7. CM noise equivalent circuit for the dual-phase PFC. (a) CM noise equivalent circuit. (b) Equivalent circuit when applying superposition to voltage source V_{s1} . (c) Equivalent circuit for V_{s1} in a Wheatstone bridge form.

The balance condition was derived based on two assumptions [45]: Assumption 1 stated that all interwinding capacitors associated with PCB windings are neglected; Assumption 2 stated that the coupling between L_1 and L_3 , as well as the coupling between L_2 and L_4 , is unity. With those, the following relationships were derived based on Fig. 3.7 (b) and (c).

$$\frac{V_1}{V_3} = \frac{N_1}{N_2} \quad (3-1)$$

$$\frac{V_2}{V_4} = -\frac{N_1}{N_2}, \text{ and} \quad (3-2)$$

$$V_3 + V_4 = V_2, \quad (3-3)$$

where V_1 , V_2 , V_3 and V_4 are the voltages of inductors L_1 , L_2 , L_3 and L_4 , and N_1 and N_2 are the number of turns for L_1 (L_2) and L_3 (L_4).

Substituting (3-1)-(3-2) into (3-3), the ratio between V_1 and V_2 is calculated as

$$\frac{V_1}{V_2} = \frac{N_1 + N_2}{N_2}. \quad (3-4)$$

Assuming in a balance condition, CM current $I_{CM} = 0$ in Fig. 3.7 (c), the following relationship is established

$$I_1 = I_2 + I_3(s). \quad (3-5)$$

$$\frac{Z_1}{Z_2} = \frac{V_1}{V_2} = \frac{N_1 + N_2}{N_2}. \quad (3-6)$$

The ratio of Z_3/Z_4 is

$$\frac{Z_3}{Z_4} = \frac{C_b + C_d + C_{add}}{C_d}. \quad (3-7)$$

To satisfy the balance principle, i.e., $Z_1/Z_2 = Z_3/Z_4$, the following condition should be realized by adjusting the external capacitor.

$$\frac{N_1}{N_2} = \frac{C_b + C_{add}}{C_d} \quad (3-8)$$

Fig. 3.8 shows the measurement of CM noise. CM noise suppression was effective only up to around 7 MHz, with diminishing effect beyond that [45].

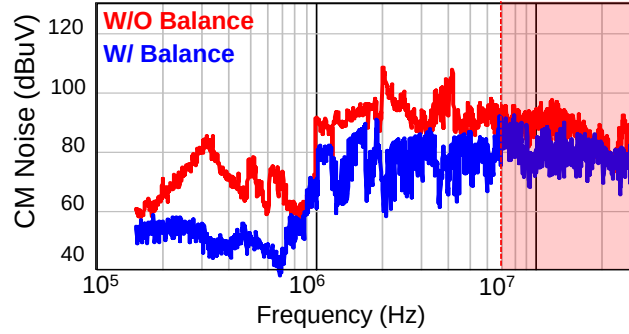


Fig. 3.8. CM noise measurement with and without balance technique[45].

In the following section, a detailed analysis is provided. The root cause for the failure to achieve the expected outcome is identified.

3.2.2 Characterization and Measurement of Z_1 and Z_2

To gain a better understanding of the inability of fulfilling the expected CM noise suppression beyond 7 MHz, impedances Z_1 and Z_2 for the coupled inductor structure are measured. As shown in Fig. 3.9 (a), Z_1 is measured from the two terminals of L_1 , with L_2 connected in parallel with L_3 and L_4 , and likewise, for Z_2 in Fig. 3.9 (b). It should be noted that the Z_1 and Z_2 measurement here only represents the impedances with respect to Fig. 3.7 (b), when V_{s1} noise source is considered.

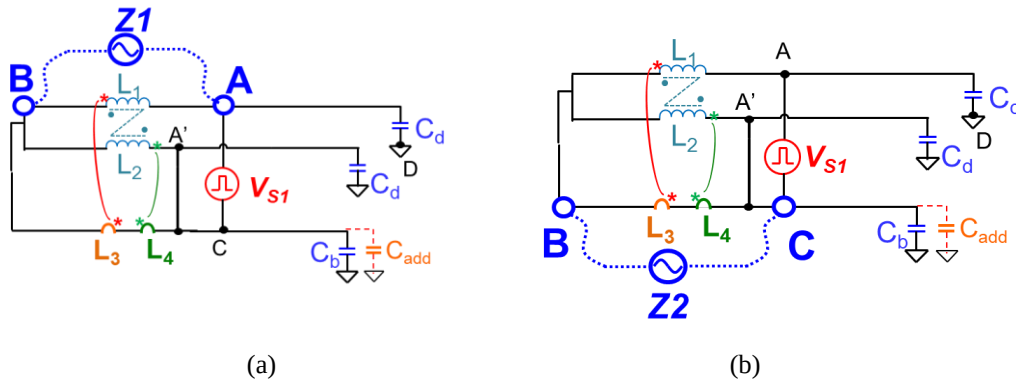


Fig. 3.9. (a) Measurement setup of Z_1 . (b) Measurement setup of Z_2 .

The measured impedance of Z_1 and Z_2 are illustrated in Fig. 3.10. It is noticed that the resonance between inductors and their associated interwinding capacitors was observed in both Z_1 and Z_2 between 10-20 MHz. Thus, it is improper to assume that all interwinding capacitors associated with PCB windings are negligible in the frequency range of interest. Furthermore, the measured impedance of Z_1 indicates that the resonant frequency of L_1 occurs at around 13 MHz. The resonant frequency of Z_2 , however, is somewhat less than 13 MHz because of the inadequate coupling between L_1 and L_3 . Subsequently, the ratio Z_1/Z_2 deviates from a constant value starting around 7 MHz. This observation further substantiates the lack of effectiveness observed in the measurement in Fig. 3.8.

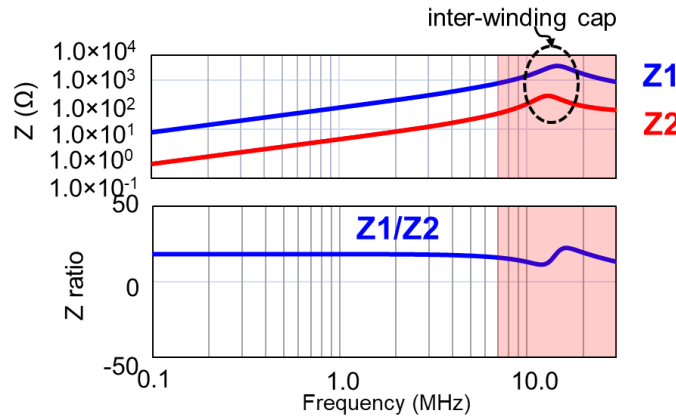


Fig. 3.10. Measured Z_1 and Z_2 based on the coupled inductor structure in Fig. 3.6.

In fact, the PCB winding structure in Fig. 3.6 has extremely complex interwinding capacitors. By taking a closer look into the winding layout, Fig. 3.11 delineates the interwinding capacitors associated with adjacent layers. In this figure, C_1 and C_2 represent the interwinding capacitors within the windings of L_1 and L_2 , respectively, while C_{12} , C_{13} and C_{24} are the interwinding capacitors between associated inductors. A more complete CM noise equivalent circuit by considering effects of those interwinding capacitors is illustrated in Fig. 3.12 (a). By applying superposition theory, the equivalent circuit for noise source V_{s1} in a Wheatstone bridge format is

shown in Fig. 3.12 (b). It is observed that those capacitors are intertwined in a rather convoluted manner. In particular, the exist of C_{12} is detrimental to the Wheatstone bridge circuit. Therefore, it is difficult to realize the balance condition with the PCB winding structure in Fig. 3.6.

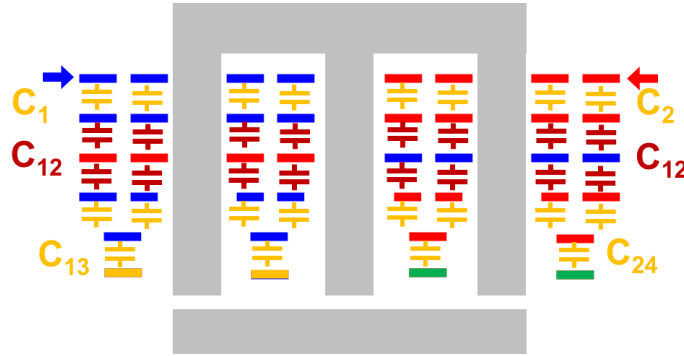


Fig. 3.11. PCB winding inductor with interwinding capacitors.

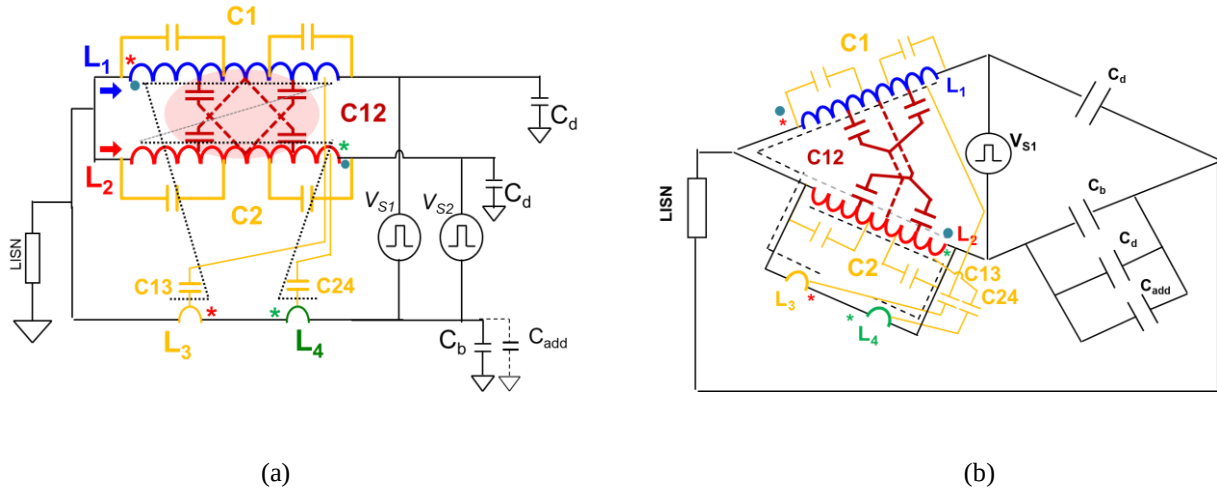


Fig. 3.12. CM noise equivalent circuit for the dual-phase PFC with interwinding capacitors. (a) CM noise equivalent circuit. (b) Equivalent circuit in a Wheatstone bridge form when applying superposition to voltage source V_{s1} .

Moreover, these four inductors were cross coupled in such a convoluted manner that the desired coupling coefficients could not be realized due to conflicting factors. Referring to the coupled inductor structure in Fig. 3.6, coupling between L_1 and L_2 , with $\alpha_{12}=-0.7$, was chosen for the purpose of reducing the frequency range[45]. Coupling between L_1 and L_3 , with $\alpha_{13}\approx 0.96$, as well

as L_2 and L_4 with $\alpha_{24} \approx 0.96$, are essential for the purpose of CM noise suppression. α_{13} and α_{24} are intended to be as strong as possible. However, the coupling between L_1 and L_4 (α_{14}), L_2 and L_3 (α_{23}), and L_3 and L_4 (α_{34}) exist as byproducts. This presents a rather convoluted coupling relationship among all four inductors. Therefore, the balance condition cannot be easily identified. A simplified PCB winding structure with less convoluted interwinding capacitors and improved coupling relationships is desirable.

3.3 Improved Balance Technique to Address Effects of Parasitics

To remove the interwinding capacitors between L_1 and L_2 , the winding configuration must change. As shown in Fig. 3.6, a layer of L_2 is placed in the midst of L_1 to reduce the winding loss. This function can simply be replaced with L_3 , since L_3 also carries the L_2 current, and likewise, L_1 is replaced by L_4 on the other leg. The proposed structure is shown in Fig. 3.13. Since L_1 and L_2 are arranged in different legs, the interwinding capacitors between L_1 and L_2 are eliminated. In addition, the coupling between L_1 and L_2 can be simply controlled by adjusting the air gap of the center leg. In this configuration, the coupling coefficient between inductor L_1 and L_2 , and L_1 and L_3 , are $\alpha_{12} = -0.7$ and $\alpha_{13} \approx 0.99$ respectively.

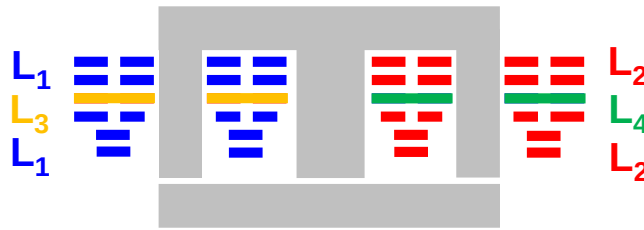


Fig. 3.13. The proposed coupled inductor structure. The coupling coefficient between inductor L_1 and L_2 , and L_1 and L_3 , are $\alpha_{12} = -0.7$ and $\alpha_{13} \approx 0.99$ respectively.

Since L_3 is part of L_1 , all parasitic capacitors associated with L_1 , as illustrated in Fig. 3.14, can

be represented by a lumped capacitor C_1 , and likewise, C_2 for L_2 and L_4 . Therefore, the improved winding configuration leads to a much-simplified equivalent circuit, as shown in Fig. 3.15 (a) and (b). However, it is still not easy to directly tell the conditions for satisfying the balance principle, due to the convoluted coupling relationship among all four inductors. A modeling is further preformed to derive the necessary conditions for realizing the balance principle.

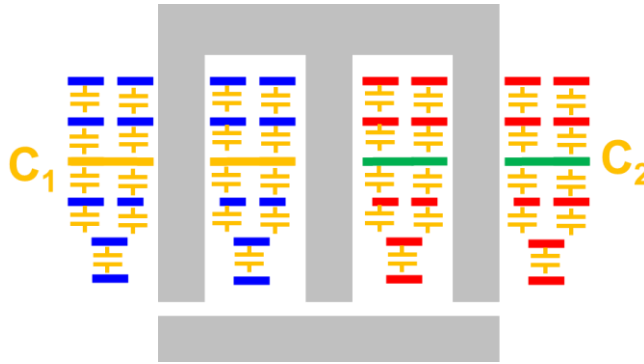


Fig. 3.14. Interwinding capacitors of the improved PCB winding inductor.

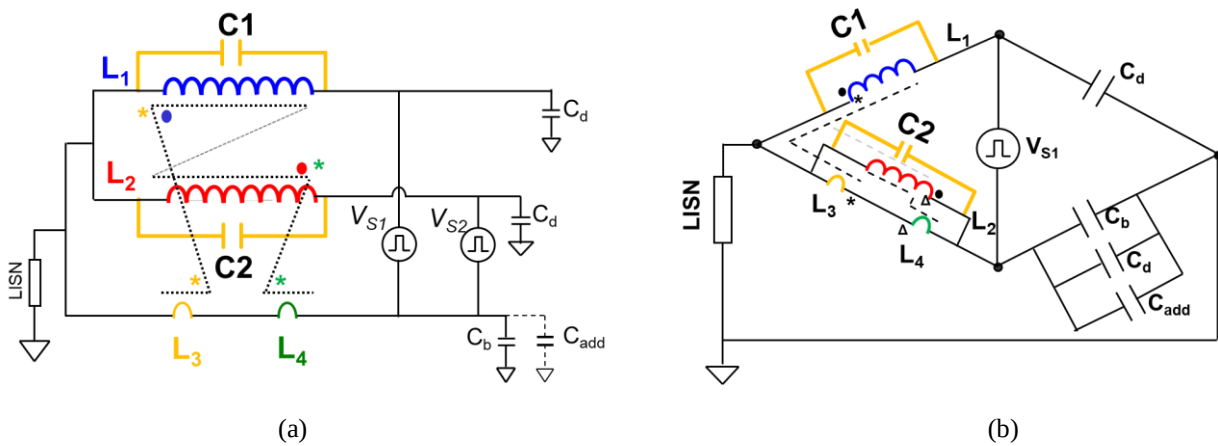


Fig. 3.15. CM noise equivalent circuit for the dual-phase PFC with improved PCB inductors. (a) CM noise equivalent circuit. (b) Equivalent circuit in a Wheatstone bridge form when applying superposition to voltage source V_{S1} .

The objective of the modeling is to simplify the convoluted coupling shown in Fig. 3.16 (a) into a decoupled representation, as shown in Fig. 3.16 (b). From the modeling point of view, one can assume a perfect coupling between L_1 and L_3 , as well as L_2 and L_4 . Then we get

$$\alpha_{13} = \alpha_{24} = 1,$$

$$\alpha_{12} = \alpha_{14} = \alpha_{23} = \alpha_{34} = \alpha = -0.7.$$

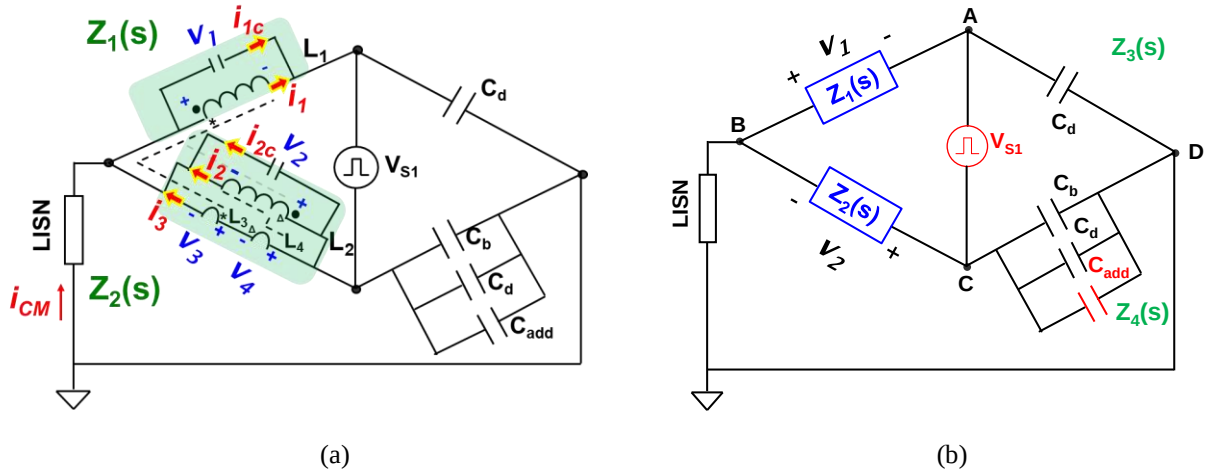


Fig. 3.16. CM noise equivalent circuit model for noise source V_{s1} by taking into account of interwinding capacitors. (a) Equivalent circuit. (b) Decoupled representation.

Since the winding structure is symmetrical, the following relation is true: $L_2 = L_1 = L$, $L_4 = L_3 = L/n^2$, where n is the turns ratio between L_1 and L_3 , and $C_1 = C_2 = C$.

From Fig. 3.16 (a),

$$v_1(t) = L \frac{di_1(t)}{dt} - M_{12} \frac{di_2(t)}{dt} + M_{13} \frac{di_3(t)}{dt} + M_{14} \frac{di_4(t)}{dt}, \quad (3-9)$$

where $M_{12} = \alpha L$, $M_{13} = M_{24} = L/n$, $M_{14} = M_{23} = \alpha L/n$, $M_{34} = \alpha L/n^2$.

Equation (3-9) can be rewritten in frequency domain as

$$V_1(s) = sLI_1(s) - s\alpha LI_2(s) + s(\alpha + 1) \frac{L}{n} I_3(s), \quad (3-10)$$

Similarly,

$$V_2(s) = -s\alpha LI_1(s) + sLI_2(s) - s(\alpha + 1)\frac{L}{n}I_3(s), \quad (3-11)$$

$$V_3(s) = s\frac{L}{n}I_1(s) - s\alpha\frac{L}{n}I_2(s) + s(1 + \alpha)\frac{L}{n^2}I_3(s), \text{ and} \quad (3-12)$$

$$V_4(s) = s\alpha\frac{L}{n}I_1(s) - s\frac{L}{n}I_2(s) + s\frac{L}{n^2}(\alpha + 1)I_3(s). \quad (3-13)$$

and

$$V_2(s) = V_3(s) + V_4(s). \quad (3-14)$$

From (3-10) - (3-14), $V_2(s)$, $V_3(s)$, and $V_4(s)$ are expressed as functions of $V_1(s)$

$$V_2(s) = \frac{V_1(s)}{n + 1}, \quad (3-15)$$

$$V_3(s) = \frac{V_1(s)}{n}, \text{ and} \quad (3-16)$$

$$V_4(s) = -\frac{V_1(s)}{n(n + 1)}. \quad (3-17)$$

Assuming in a balance condition, CM current $I_{CM} = 0$ in Fig. 3.16(a), the following relationship is established

$$I_1(s) + I_{1C}(s) = I_2(s) + I_{2C}(s) + I_3(s), \quad (3-18)$$

where $I_{1C}(s) = sCV_1(s)$, $I_{2C}(s) = sCV_1(s)/(n + 1)$. Substituting (3-15)-(3-18) into (3-10)-(3-12), the current $I_1(s)$, $I_2(s)$ and $I_3(s)$ can be expressed as a function of $V_1(s)$

$$I_1(s) = -\frac{n^2 + LCs^2n(\alpha^2 - 1) + (2n + 2)(\alpha + 1)}{sL(n + 2)(n + 1)(\alpha^2 - 1)}V_1(s), \quad (3-19)$$

$$I_2(s) = -\frac{n^2\alpha + LCs^2n(1 - \alpha^2) + (2n + 2)(\alpha + 1)}{sL(n + 2)(n + 1)(\alpha^2 - 1)}V_1(s), \text{ and} \quad (3-20)$$

$$I_3(s) = \frac{n^2 + n^2LCs^2(\alpha + 1)}{sL(n + 2)(\alpha + 1)}V_1(s). \quad (3-21)$$

$Z_1(s)$ and $Z_2(s)$ can be defined as

$$Z_1(s) = \frac{V_1(s)}{I_1(s) + I_{1c}(s)}, \text{ and} \quad (3-22)$$

$$Z_2(s) = \frac{V_2(s)}{I_2(s) + I_{2c}(s) + I_3(s)}. \quad (3-23)$$

Substituting (3-15), (3-19)-(3-21) into (3-22)-(3-23), $Z_1(s)$ and $Z_2(s)$ are expressed as

$$Z_1(s) = \frac{sL_{eq1}}{s^2L_{eq1}C_{eq1} + 1}, \quad (3-24)$$

where,

$$L_{eq1} = \frac{L(1 - \alpha^2)(n + 2)(n + 1)}{2n + 2\alpha + n^2 + 2n\alpha + 2},$$

$$C_{eq1} = \frac{C \cdot (n^2 + 2n + 2)}{(n + 1)(n + 2)}, \text{ and}$$

$$Z_2(s) = \frac{sL_{eq2}}{s^2L_{eq2}C_{eq2} + 1}, \quad (3-25)$$

where,

$$L_{eq2} = \frac{L(1 - \alpha^2)(n + 2)}{2n + 2\alpha + n^2 + 2n\alpha + 2},$$

$$C_{eq2} = \frac{C \cdot (n^2 + 2n + 2)}{(n + 2)}.$$

In reference to Fig. 3.15(b), it should be noted that $Z_1(s)$ and $Z_2(s)$ are totally decoupled. The final equivalent circuit is shown in Fig. 3.17.

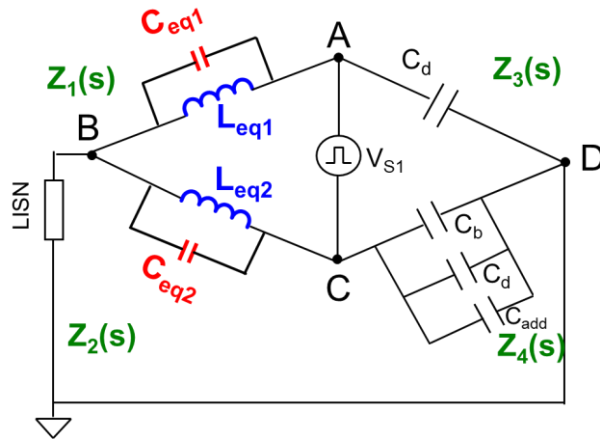


Fig. 3.17. Simplified decoupled CM noise equivalent circuit under the assumption of unity coupling ($\alpha_{13} = \alpha_{24} = 1$).

It is important to note from (3-24)-(3-25) that

$$L_{eq1}C_{eq1} = L_{eq2}C_{eq2}. \quad (3-26)$$

This means the resonant frequencies of $Z_1(s)$ and $Z_2(s)$ are matched.

In addition, the ratio of $Z_1(s)/Z_2(s)$ is greatly simplified

$$\frac{Z_1(s)}{Z_2(s)} = n + 1. \quad (3-27)$$

This ratio is simply a function of n and is independent of frequency. This is a much-welcome

result, meaning the CM noise suppression can be realized in the frequency range of interest. Of course, the previous statement is under the assumption that the ground loop resonant occurs at a frequency beyond 30 MHz.

Furthermore, it is noticed from (3-26)-(3-27) that the balance condition is independent to the coupling between L_1 and L_2 , i.e., α . Therefore, the new structure maintains the freedom of choosing proper coupling between L_1 and L_2 .

To satisfy the balance principle, the ratio of $Z_3(s)/Z_4(s)$ can be tailored to the ratio of $Z_1(s)/Z_2(s)$ by adjusting the external capacitor of C_{add} , as shown in Fig. 3.5.

$$\frac{Z_3(s)}{Z_4(s)} = \frac{C_b + C_d + C_{add}}{C_d} = n + 1. \quad (3-28)$$

Measured impedance of $Z_1(s)$ and $Z_2(s)$ are shown in Fig. 3.18. It is observed that the self-resonant frequencies of $Z_1(s)$ and $Z_2(s)$ are aligned around 12 MHz. In fact, since L_1 and L_3 are tightly coupled, the impedance $Z_2(s)$ is simply the mirror image of $Z_1(s)$ in a reduced scale, due to the turns ratio between L_1 and L_3 . Meanwhile, the ratio of $Z_1(s)/Z_2(s)$ remains constant from 150 kHz to 30 MHz.

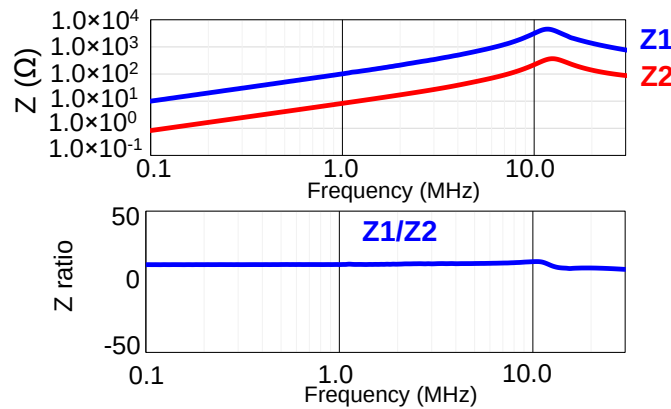
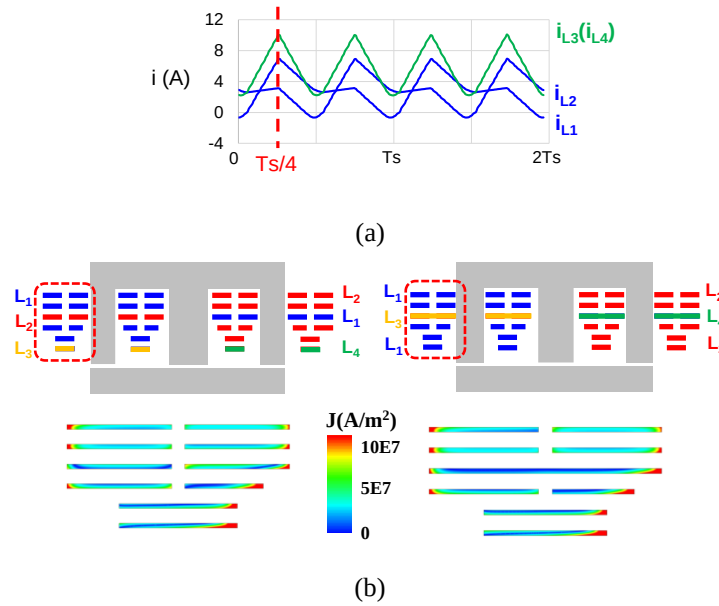


Fig. 3.18. Impedance measurements of Z_1 and Z_2 for the proposed coupled inductor structure.

Beside the significant improvement in CM noise, the impact of the improved design to core loss and winding loss are also evaluated using Ansys Maxwell FEA. The results are summarized in Table 3.1. In the simulation model, the excitation currents of the proposed inductor structure are shown in Fig. 3.19(a). Fig. 3.19(b) shows the reduction of current density in the third layer (L_3), that carries both i_{L1} and i_{L2} current. Thus, winding loss is reduced by 25%. However, the number of turns is reduced from 10 to 9 in the improved version, which causes an increase in core loss from 1.9 W to 3.1 W. Nonetheless, this amount of increase is higher than expected. ML91s is a relatively new high frequency core material. This material shows a highly non-linear increasing in power loss density when operating at a flux level beyond 70 mT. In Fig. 3.19(c), it is observed that the flux density in this planner structure is not distributed uniformly, especially at the interface between the plate and legs. It is suspected that the flux density is significantly higher than 70 mT. This problem can be circumvented with a more careful winding design and core layout in the future research.



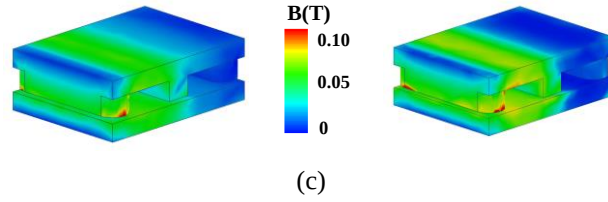


Fig. 3.19. (a) Inductor current. (b) Current distribution at $T_s/4$ for windings in the dotted box. (c) Flux density at $T_s/4$.

TABLE 3.1 PFC INDUCTOR LOSS BREAKDOWN

Inductors	Previous[45]	Improved
Winding loss	2.7 W	2.0 W
Core loss	1.9 W	3.1 W
Total inductor loss	4.6 W	5.1 W

3.4 Experiment Results

The effectiveness of the proposed balance technique in CM noise suppression is verified using a 1.2 kW dual-phase interleaved MHz totem-pole PFC rectifier, as shown in Fig. 3.20. Two prototypes were built in order to provide a fair comparison and to quantify the level of improvement. Version I used the same inductor design as the previous author Yang [45]. Version II was built using the improved design. In both prototypes, inductor windings were implemented in a six-layer PCB. The specific circuit parameters used in those two prototypes are summarized in Table II.

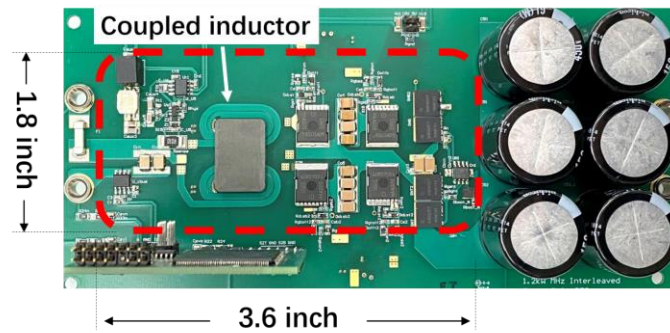
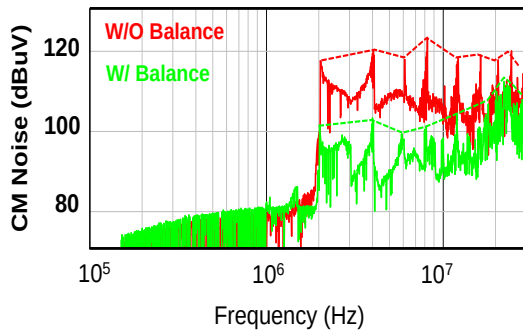


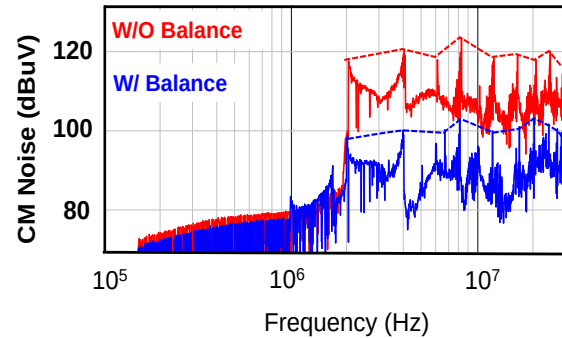
Fig. 3.20. Hardware prototype of the improved version. The other prototype using the original inductor design [45] has the same footprint with slightly different winding structure.

TABLE 3.2 SPECIFICATIONS OF THE BUILT TWO PFC PROTOTYPES[45], [64]

Component	Ver. I	Ver. II
Switching frequency	1-2 MHz	1-2 MHz
L_1 and L_2	5.2 μ H	5.0 μ H
L_3 and L_4	65.3 nH	78.0 nH
n	9	8
α_{13}, α_{24}	0.96	0.99
α_{12}	-0.7	-0.7
$\alpha_{14}, \alpha_{23},$	-0.55	-0.7
α_{34}	-0.15	-0.7
C_b	112.9 pF	107.3 pF
C_d	13.7 pF	15.3 pF
C_{add}	150 pF	15.3 pF
C_{in}	0.16 μ F	0.16 μ F
GaN device	IGT60R070D1	IGT60R070D1
GaN device Driver	Si8273	Si8273
60 Hz switch	IPL60R065C7	IPL60R065C7
Magnetic material	ML91s	ML91s



(a)



(b)

Fig. 3.21. Comparison of CM noise reduction between the two prototypes. (a) CM noise measurement in Version I prototype. (b) CM noise measurement in improved Version II prototype.

Fig. 3.21(a) shows the measured CM noise from the Version I prototype, where the inductor structure is the same as in Yang's design [45]. It is observed that CM noise suppression is effective up to around 10 MHz, with diminishing effect beyond that. Fig. 3.21(b) shows the measured CM noise with the improved prototype Version II. It is observed that CM noise can be reduced by

approximately 20 dB μ V up to 30 MHz. The reduction of CM noise by the amount of 20 dB μ V can be roughly estimated based on the CM noise model explained in the Appendix C. Furthermore, in this case, the balance inductors (L_3 and L_4) are rather small (78 nH). Thus, the ground loop resonant frequency is pushed beyond the frequency range of interest.

3.5 Conclusion

This chapter offers an improved balance technique for CM noise suppression in a PCB-based PFC circuit. The GaN-based PFC, operating beyond 1 MHz, was implemented with a two-phase interleaved boost operating at CRM for ZVS. The interleaving offered a significant DM noise reduction for CRM operation. It was also critical for PCB based inductor design for much reduced winding loss. Furthermore, balance technique was employed with two additional inductors L_3 and L_4 placed in the return path in order to reduce CM noises. With four inductors interleaved and coupled in one magnetic core, the state-of-the-art PCB winding inductor offered a rather convoluted structure in the manner that all interwinding capacitors are intertwined. Moreover, while L_1 and L_2 were coupled with certain coupling coefficient (-0.7) to minimize the frequency range variation due to CRM operation, L_1 and L_3 were expected to be strongly coupled to achieve the best effect of CM noise reduction. However, these four inductors were cross coupled in such a convoluted manner that the desired coupling coefficients could not be realized due to conflicting factors. Consequently, the effectiveness of CM noise reduction was limited up to a frequency where the parasitic ringing of L_1 and L_2 took over, roughly 7 MHz.

To eliminate the unwanted interwinding capacitors, a modified PCB winding structure with a simple physical implementation is proposed. The improved structure decouples the interwinding capacitors of L_1 and L_2 , leading to a much-simplified equivalent circuit. Meanwhile, the new

structure maintains the freedom of choosing proper coupling between L_1 and L_2 while strengthening the coupling between L_1 and L_3 , to facilitate the desired impedance matching, ie. $Z_1/Z_2 = Z_3/Z_4$. CM noise modeling and analysis of the structure were performed to derive the necessary conditions for realizing the balance principle. The proposed method offers drastic improvements in EMI/EMC. The proposed balance technique for CM noise reduction is effective for PCB-based integrated magnetic design. The parasitic oscillation of inductors known to be detrimental for CM noise reduction is circumvented with the improved magnetic structure and coupling.

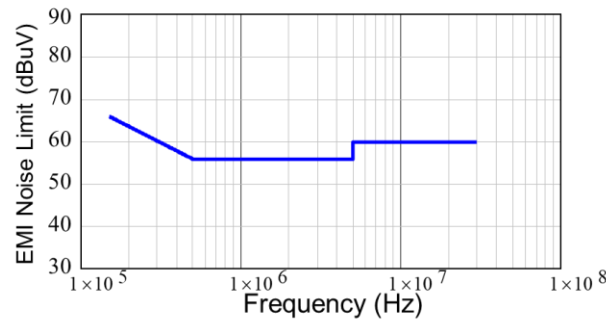
Chapter 4 EMI Filter Design Considerations to Mitigate Near Field Effect

By applying the PCB-based balance technique to a PFC converter and the shielding technique to an LLC DC/DC converter, significant noise reductions were realized. This provides the opportunity to employ a simple one-stage EMI filter to achieve the required EMI noise attenuation for a server power supply. However, the presence of self-parasitics, such as the equivalent series inductor (ESL) of capacitors and the equivalent parallel capacitor (EPC) of inductors, as well as near-field mutual couplings between the inductor and capacitors, are detrimental and render the filter ineffective in frequencies beyond a few hundred kHz.

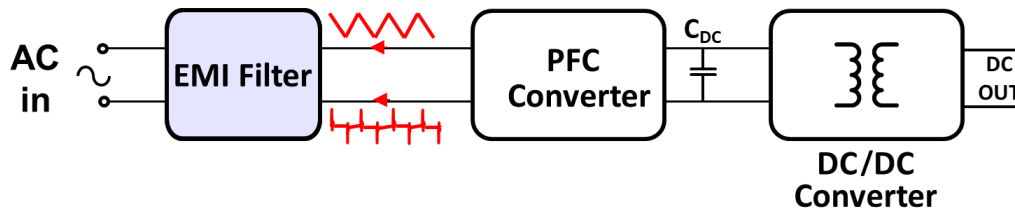
This chapter offers an in-depth study on reducing the unwanted near-field couplings between the CM/DM inductors and DM filter capacitors, as well as unwanted self-parasitics such as the ESL of the DM capacitors. An exhaustive finite element analysis (FEA) and near field measurements are conducted to better understand the effect of frequency on the polarization of the near field due to the displacement current. The knowledge gained in this study enables one to minimize unwanted mutual coupling effects by means of physical placement of these filter components. Moreover, the unwanted ESL of a DM capacitor is reduced using an X-cap structure. The mutual coupling between capacitors is also minimized by a flux cancellation loop. With these approaches applied, for the first time, a single-stage filter is demonstrated in an offline 1 kW, 12 V server power supply.

4.1 Effects of Self-Parasitics and Mutual Couplings

Switching power converters can generate conducted EMI noises, including CM and DM noises, that flow in both power lines and the earth ground. Those EMI noises could potentially impact the normal operations of other equipment and devices if not properly addressed. The EN55022 class A is one of the widely used standards for a conducted EMI for most of the AC/DC converters in the United States. It specifies the conducted EMI limits in the frequency range of 150 kHz to 30 MHz, as illustrated in Fig. 4.1 (a). The limit value is 66 dB μ V at 150 kHz, 56 dB μ V from 500 kHz to 5 MHz, and 60 dB μ V from 5-30 MHz. In order to suppress EMI noises, an EMI filter is usually adopted between the power converter and the grid, as shown in Fig. 4.1 (b).



(a)



(b)

Fig. 4.1. (a) EN55022 class A standard for conducted EMI noises. (b) Schematic of a typical AC/DC converter.

Usually, the EMI filter will occupy one-fourth to one-third of the total volume of power supply. Fig. 4.2 shows a conventional two-stage EMI filter, where the DM and CM inductors can be

integrated into one core. In some cases, it may be difficult to implement and more magnetic components must be added.

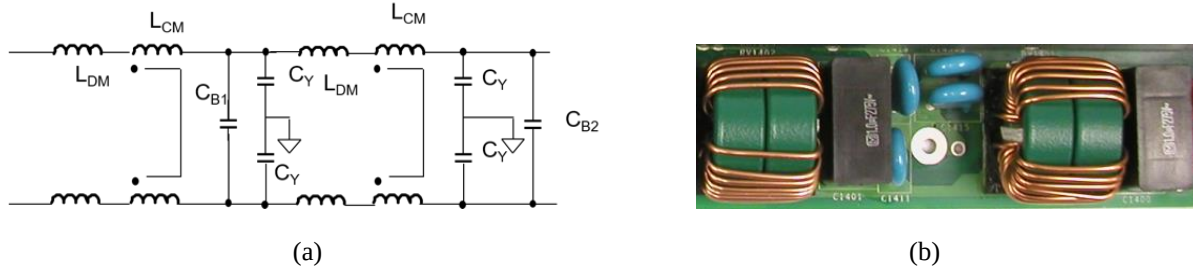


Fig. 4.2. Conventional two-stage EMI filter. (a) Filter topology. (b) Conventional two-stage filter hardware with integrated CM/DM inductor.

The 1 kW GaN-based DC-DC converter illustrated in Chapter 1 and the PFC converter illustrated in Chapter 3 require special efforts to achieve significant DM/CM noise reduction. This provides the opportunity, for the first time, to use a simple one-stage EMI filter to achieve the required EMI noise attenuation for a server power supply.

Based on the raw noise test results shown in Fig. 4.3, a single-stage EMI filter was designed. Fig. 4.4 shows the intended filter configurations for CM and DM noises, respectively. The filter parameters designed for the 1 kW server power supply are shown in Table 4.1.

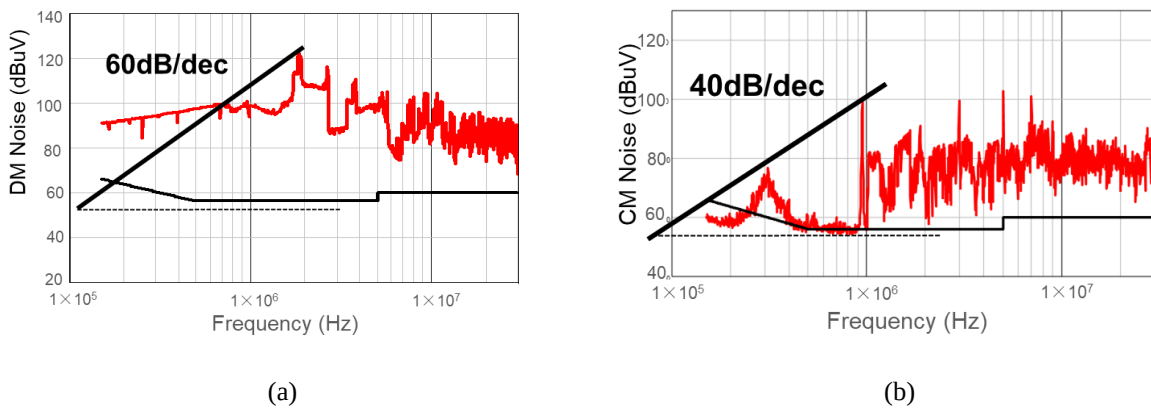


Fig. 4.3. Conducted raw noise measurement based on the previously discussed 1 kW PFC and DCX design. (a) DM noise. (b) CM noise.

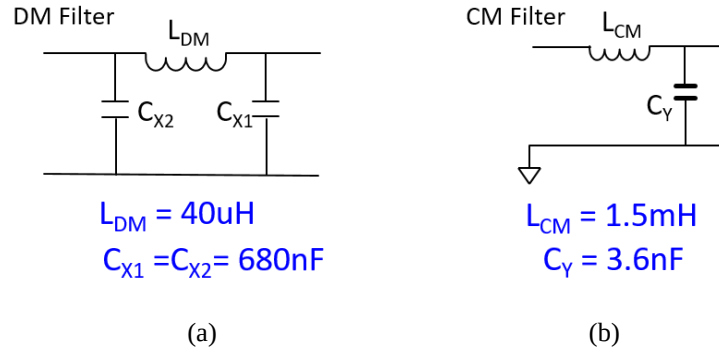


Fig. 4.4. Single-stage filter diagram. (a) DM filter. (b) CM filter.

TABLE 4.1 PARAMETERS OF THE SINGLE-STAGE EMI FILTER

Component	Parameters
L_{CM}	1.5 mH
L_{DM}	40 μH
C_{X1}, C_{X2}	680 nF
C_{Y1}, C_{Y2}	1.8 nF

Fig. 4.5 shows the combined DM/CM filter configuration, where the leakage inductance of the CM choke is used as the DM inductance.

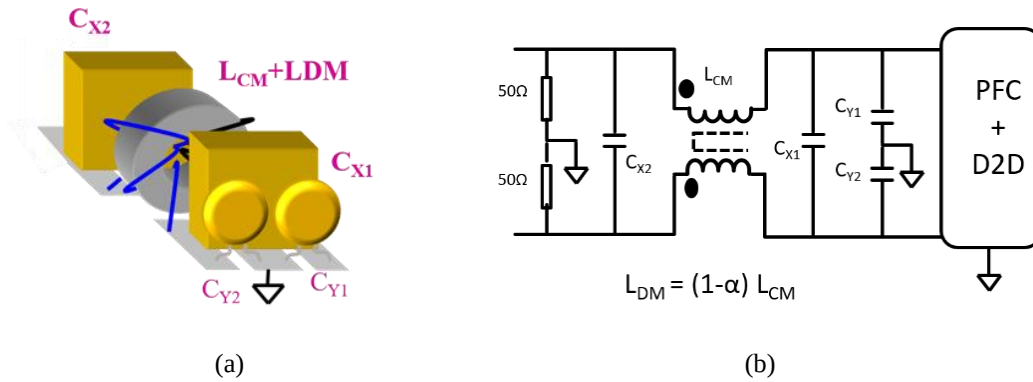


Fig. 4.5. Single-stage EMI filter with integrated CM/DM inductor. (a) Physical layout. (b) Circuit diagram.

CM and DM noise measurements are shown in Fig. 4.6 and Fig. 4.7. The CM noises have been attenuated marginally below the EN55022 class A standard, from 150 kHz to 30 MHz. However,

the DM noises amplitude exceeds the standard beyond the expectation, in the frequency range of 3 MHz to 30 MHz.

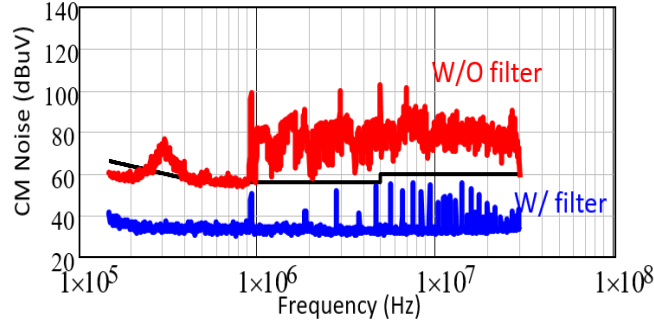


Fig. 4.6. CM noise measurement result for server power supply.

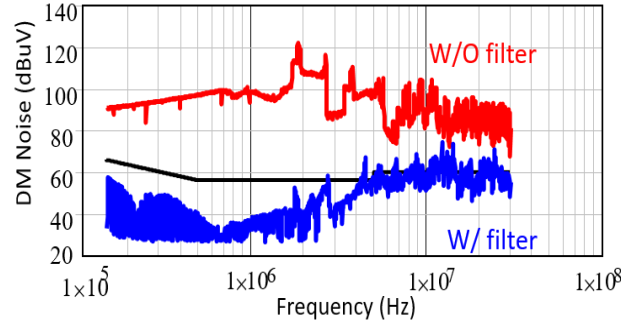


Fig. 4.7. DM noise measurement result for server power supply.

The reason for the poor performance of the DM filter at high frequencies was described in detail in [65]. It is summarized below. The equivalent circuit for the single-stage DM filter is shown in Fig. 4.8. Due to the presence of self-parasitics, such as the ESL of the DM capacitors and EPC of the CM/DM inductors, the filter has lost its ability to attenuate noises beyond 2 MHz. This is shown as Case II in Fig. 4.9. To make matters worse, the mutual couplings M_1 & M_2 between the filter inductor and DM capacitors cause additional detrimental effects that begin at an even lower frequency, around 300 kHz, as shown in Case III. The effect of the mutual coupling M_3 between DM capacitors is more pronounced at high frequency. With these unwanted parasitic effects, the

insertion gain of the single-stage DM filter is rendered ineffective beyond a few hundred kHz, as shown in Fig. 4.9, case III.

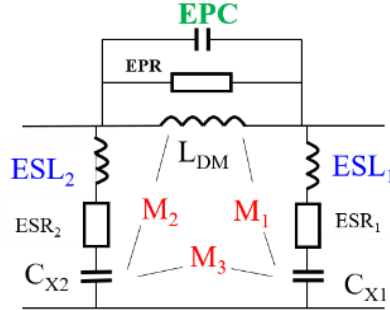


Fig. 4.8. Equivalent circuit for a single-stage DM filter, including self-parasitics and mutual couplings.

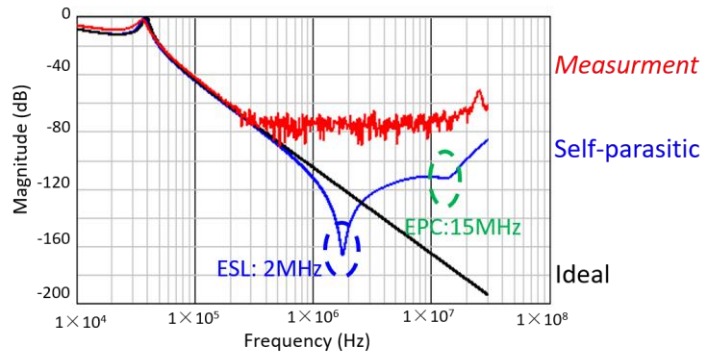


Fig. 4.9. The major factors affecting the insertion gain of the single-stage DM filter. Case I: Ideal insertion gain without parasitics. Case II: Adding the effects of self-parasitics ESL and EPC. Case III: Measured insertion gain, including both self-parasitics and mutual couplings.

It is evident that the unwanted mutual couplings between L and the two DM capacitors are related to the physical placement of these filter components [65]. Fig. 4.10 (a) illustrates a commonly used filter layout that provides the most compact footprint. With the inductor standing vertically in close proximity to two DM capacitors, it inadvertently provides the maximum coupling between L and C_{x1} and C_{x2} . However, if the inductor is positioned in the manner shown in Fig. 4.10 (b), the effects of the coupling between L and C_{x1} and C_{x2} will reduce significantly. Although this statement is

intuitively correct, the matter is far more complex than it appears, and it will be elaborated in the following sections.

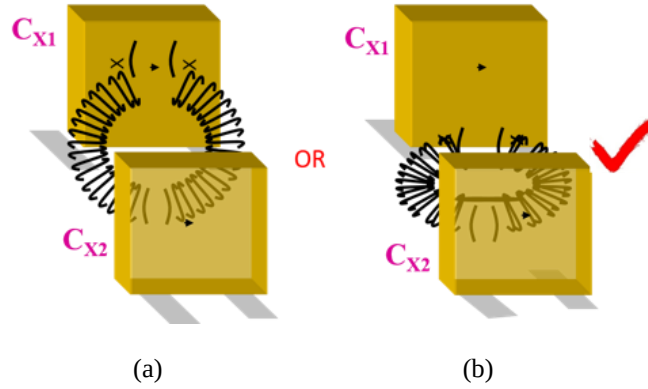


Fig. 4.10. Effect of physical layout to unwanted mutual couplings. (a) Significant mutual couplings (M_1 & M_2) between inductor and DM capacitors. (b) Reduced mutual coupling (M_1 & M_2) between L & C .

4.2 Displacement Currents and Its Near Field Effects

The simple observation given in section 4.1 can be quantified by analyzing the near field effect between the inductors and capacitors, and graphically depicting the leakage flux distribution around them.

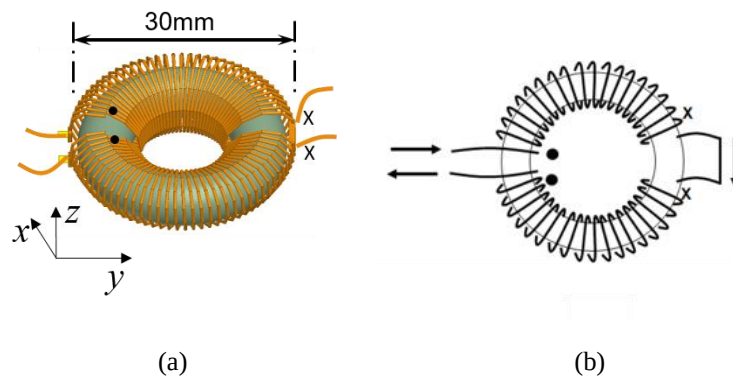


Fig. 4.11. Integrated DM/CM inductor.

An integrated DM/CM filter is shown in Fig. 4.11. The CM inductor is represented by an 80 turns inductor, wound in a sectionalized manner with 40 turns on the forward path and 40 turns on the

reverse path, as shown in Fig. 4.11 (a). The DM inductor is represented by the leakage flux, measured with one end of the CM choke shorted, and the AC excitation is applied from another end, as shown in Fig. 4.11 (b). In this design $L_{CM} = 1.5$ mH and $L_{DM} = 40$ μ H.

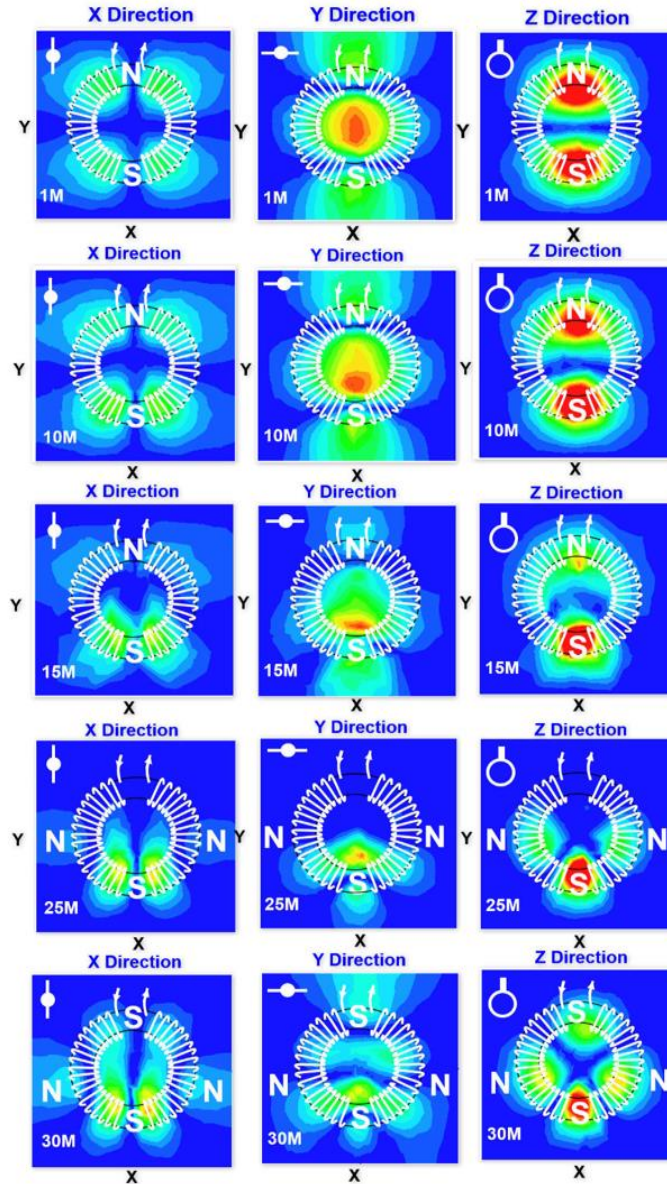


Fig. 4.12. Simulated X, Y, and Z components of the magnetic field at different frequencies (1-30 MHz) on the plane 5 mm above the horizontal inductor.

A 3D model for the CM choke is built in Ansys HFSS software for FEA analysis. The X, Y, and Z components of the magnetic field, as reference in Fig. 4.11 (a), on a plane 5 mm above the

inductor top surface are recorded. Fig. 4.12 shows the recorded near field when the AC excitation frequency varies from 1 MHz to 30 MHz. The flux patterns along the X, Y, and Z direction of the plane, 5 mm above the inductor, vary dramatically with the change of AC excitation frequency. Based on these phenomena, one can easily observe that the coupling between the inductor and capacitor varies significantly with excitation frequency. These phenomena are rather enlightening. In essence, the variation of the flux pattern is caused by the displacement current, which varies with the excitation frequency.

To further elaborate on these phenomena, one can take a simple DM inductor with six turns as an example, shown in Fig. 4.13. There are two kinds of currents shown in the inductor windings. One component of current is the conductive current i_L , i.e. the current flowing inside the copper windings. The other current component is the displacement current i_{EPC} , i.e. the current that flows through the stray capacitors between windings, as shown in Fig. 4.13 (a). The displacement current is in the opposite phase of the conductive current. The sum of i_L and i_{EPC} represents the total current, i_s .

The studied DM inductor has a self-resonant frequency of roughly 10 MHz. At 1 MHz, most of the current flowing inside the windings is conductive current. Thus, the total current is uniform among all 6 turns. However, at 25 MHz, the interwinding capacitors provide a lower impedance path, thus resulting in the displacement current i_{EPC} , which flows in the opposite direction of the conductive current [66]. The maximum AC excitation voltage is applied between turn 1 and turn 6; thus, it carries the largest displacement current. Therefore, the current in each turn is highly non-uniform, specifically at high frequencies.

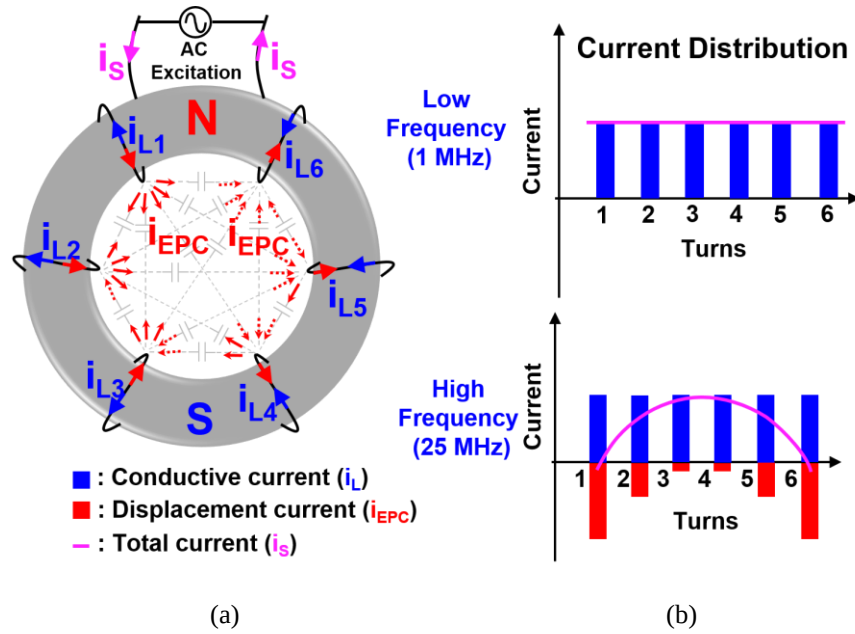


Fig. 4.13. Simple DM inductor with six turns to illustrate effect of displacement current in high frequency. (a) Inductor structure. (b) Current distribution.

The change of current distribution at different frequencies indicates the variation of flux distribution. The flux of the real CM/DM inductor in the 1 kW server power supply is shown in Fig. 4.14. At 1 MHz, the flux of conductive current flows out of the South pole and into the North pole on the plane 5 mm above the horizontal inductor's top surface. The flux of the displacement current is negligible. The total flux, which is the summation of flux by the conductive and displacement current, is symmetrical distributed, as shown in Fig. 4.12. Only one North pole and one South pole is observed in the Z-component. However, by increasing the excitation to 25 MHz, the flux of the displacement current has been comparable to the flux of the conductive current. Therefore, the original North pole by conductive current at low frequency in Fig. 4.12 disappears, and another two North poles, which are induced by the displacement current, are created on the Northeast and Northwest, alternatively.

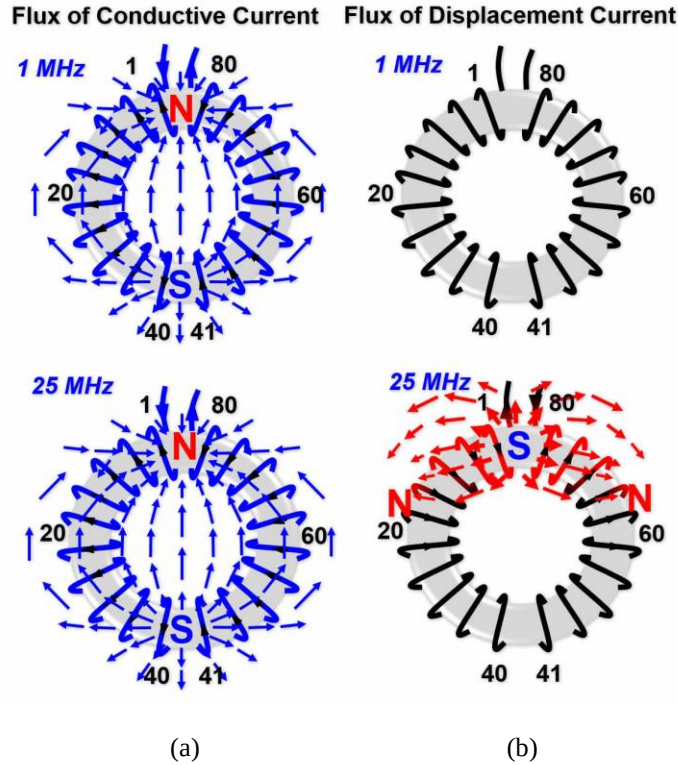


Fig. 4.14. Flux of the designed 80-turn DM inductor at low frequency (1 MHz) and high frequency (25 MHz). (a) Flux induced by conductive current. (b) Flux induced by displacement current.

4.3 Physical Placement of L and C to Minimize Near Field Couplings

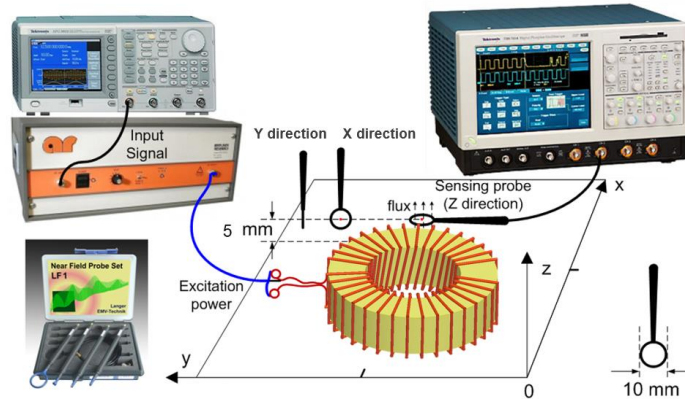


Fig. 4.15. Near field measurement setup for DM inductor [66].

The flux pattern variation is further verified with near field measurement in the experiment, as shown in Fig. 4.15. The AC excitation is provided by a function generator combined with a power

amplifier. Then the X , Y , and Z components of the magnetic field on the plane 5 mm above the inductor top surface is measured by the near field probe LANGER LF series, as delineated in Fig. 4.16. The North pole splitting phenomenon is observed and matches well with FEA simulation.

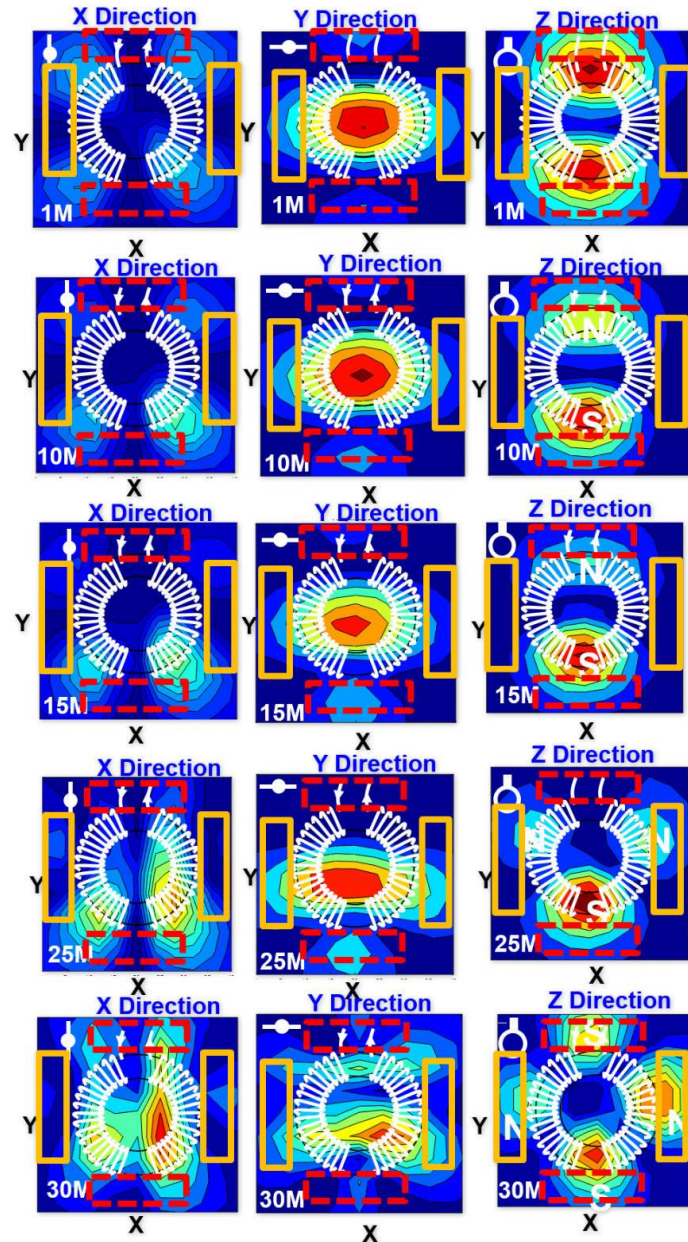


Fig. 4.16. Measured X , Y , and Z components of the magnetic field on the plane 5 mm above the horizontal inductor at different frequencies from 1-30 MHz. The red dotted line rectangles and orange solid line rectangles represent two possible candidate positions for DM capacitors.

The plotted magnetic field provides a hint that if we can find a position with weak flux at both low frequency and high frequency, then that would be an optimal position for DM capacitors in order to minimize the M_1 and M_2 coupling.

Based on this idea, if the DM capacitors are placed in the North-South location in Fig. 4.16, then the Y-direction flux is perpendicular to the capacitor surface. In this case, the Y-direction flux is considered the most influential flux that impacts the mutual coupling M_1 and M_2 . Likewise, if the capacitors are placed in East-West direction, then the X-direction flux is dominant. As can be observed in Fig. 4.16, the Y-component is quite strong at 25 MHz. If an excessive amount of noise is observed in the neighborhood of 25 MHz, it is not advisable to place the DM capacitors in the North-South direction. Instead, the DM capacitors should be placed at the East-West location. Furthermore, it is observed in Fig. 4.16 that X-direction flux is small in the places where DM capacitors are placed, in the entire frequency spectrum up to 30 MHz.

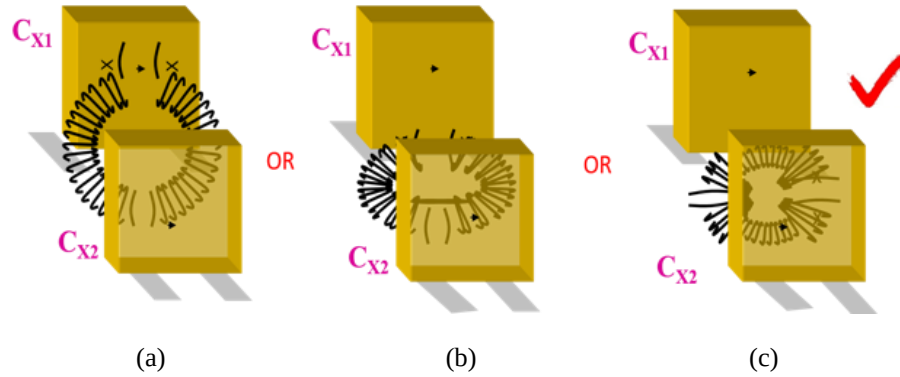


Fig. 4.17. Physical placement of input filter components. (a) Case 1: L is sandwiched by two DM capacitors with L standing vertically to minimize filter footprint. (b) Case 2: Filter L is laying down between two C_x . (c) Case 3: Coil rotating 90° with opening facing left and right.

Fig. 4.17 shows three possible layouts of the filter components. Based on the above discussions, the preferable physical layout of the filter components is Case 3 in Fig. 4.17 (c). The DM noise for different layouts of the inductor and capacitor is further verified experimentally, as shown in Fig.

4.18, for all three cases. The physical layout corresponding to Case 3 clearly renders the best attenuation of DM noises.

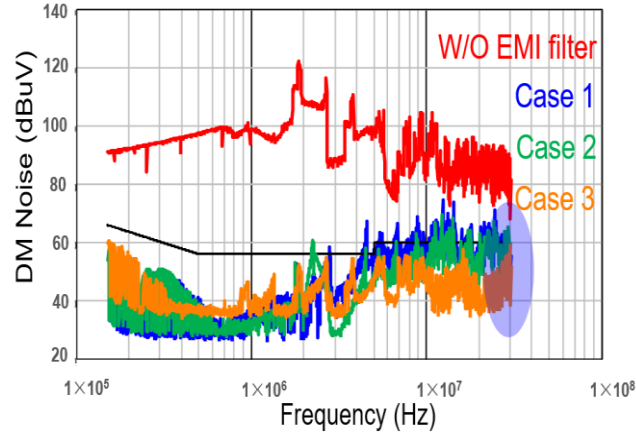


Fig. 4.18. Measured DM noise under different inductor and capacitor layouts.

The knowledge gain from Fig. 4.16 can be used as an invaluable design tool for mitigating unwanted mutual coupling between the filter inductor and capacitors. A strategy for the placement of CM capacitors, with respect to CM/DM inductors, can be developed to suppress the unwanted noises at a specific frequency band as desired.

Up to this point we have made some progress in improving the EMI signature. However, DM noise is still marginal at several isolated high frequencies in the spectrum. In the next section, we will pursue further improvement by reducing the unwanted self-parasitics.

If one works for a large corporation that can afford an in-house “EMI expert”, you may observe an exercise similar to the one mentioned above, namely, the reputed expert moves the physical placements of components in a matter of trial and error, with no particular reason behind this “fix”, then it is a matter of science rather than an art. This is what I am inspired to do and am not quite there yet.

4.4 Demonstration of a Single-Stage Filter for a 1 kW PFC

The impact of ESL takes place at around 2-3 MHz, as shown in Fig. 4.9. The ESL cancellation method proposed in [68] is demonstrated in this single-stage EMI filter, as shown in Fig. 4.19 (a). The basic idea is that if one connects two DM capacitors in an “X” structure and introduces two inductors with each inductance equals to the ESL of the DM capacitors, then the ESL in the capacitor branch is effectively cancelled. The remaining two inductors no longer behave like a capacitor ESL; rather, it is a small parasitic inductance in series with the filter inductors, as shown in Fig. 4.19 (a). The detrimental effect due to the presence of ESL of DM capacitors is nullified.

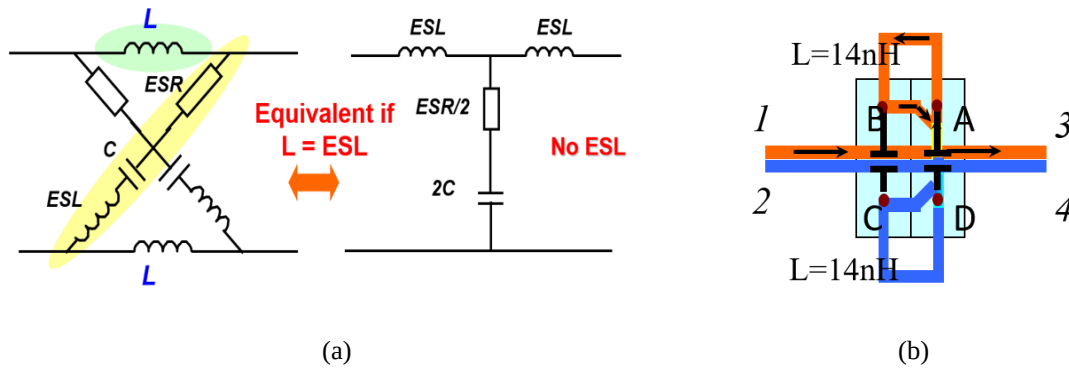


Fig. 4.19. Introducing two L to cancel ESL. (a) Circuit diagram. (b) PCB implementation.

These two small inductors are implemented by means of PCB trace, as shown in Fig. 4.19 (b) together with two “X” caps. The DM noise testing result is shown in Fig. 4.20. As can be seen, the DM noise at high frequency has been further reduced with ESL cancellation. However, a couple of spikes occur at 10 MHz and 4.5 MHz and remain anomalies.

Coupling between two DM capacitors, M_3 , also has a negative impact on the insertion gain in high frequencies. This idea may sound implausible at first, however, it can be verified in the following experiment.

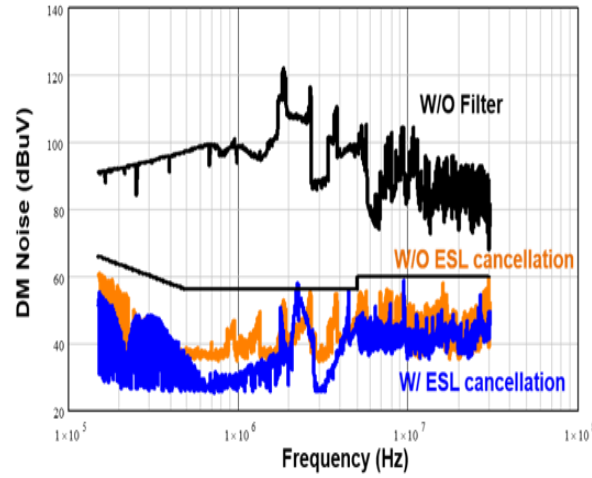


Fig. 4.20. Measured DM noise with ESL cancellation.

In order to mitigate the effect of M_3 , a flux cancellation loop L_M is introduced, as shown in Fig. 4.21 [68]. The cancellation loop is attached to the surface of C_1 . The current in the cancellation loop is the same current that flows through C_1 , but in the opposite direction. Therefore, the flux Φ_{MA} , generated by the cancellation loop, cancels the flux Φ_{M3} that flows through C_1 . Fig. 4.22 shows the measurement result with the proposed M_3 cancellation technique. The high frequency noises are noticeably reduced beyond 5 MHz [69].

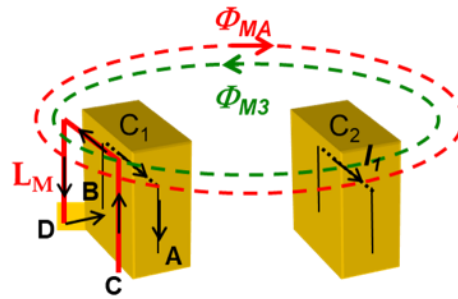


Fig. 4.21. Introducing a cancellation loop L_M to cancel the magnetic flux Φ_{M3} .

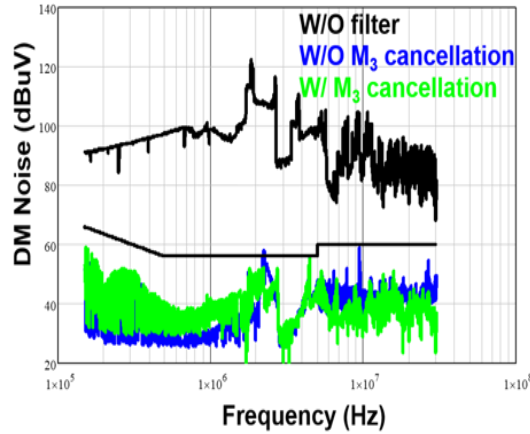


Fig. 4.22. DM noise for the proposed EMI filter without and with M_3 cancellation.

4.5 Conclusions

This chapter focuses on the design of a single-stage EMI filter for an off-line server power supply operating at a switching frequency above 1 MHz using GaN devices. By applying balance technique to the totem-pole PFC and shielding technique to LLC resonant converter, significant noise reductions are achieved. Thus, for the first time, a single-stage EMI filter can be contemplated to meet the EMI standard in server power supplies.

The chapter further offers an in-depth study on reducing the unwanted near field couplings between the CM/DM inductors and DM filter capacitors, as well as unwanted self-parasitics, such as the ESL of the DM capacitors. Based on FEA simulations, this paper clearly demonstrates the adverse effect of displacement current to the polarization of the near field, in a manner that renders the EMI filter ineffective if not properly addressed. The polarization of the near field as a function of frequency is further verified experimentally. The study leads to a better understanding of the nature of the EMI and helps to develop the means to improve filter performance and mitigate the effect of the unwanted mutual couplings.

The author does not wish to mislead the readers that the complex interactions between the unwanted parasitics among filter components are well understood at this point. At best, this work merely provides a framework that can lead to a better understanding of EMI and begin to treat it as a matter of science, rather than an art.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

The current designing and manufacturing practices for silicon-based switch-mode power supplies have reached a level of maturity that further advances will be closely linked to improvements in power devices, materials, and fabrication techniques. One of the major roadblocks for further improvement hinges on the ability to integrate large and bulky passive components in a form suitable for automation. With recent advances in wide-bandgap (WBG) power semiconductor devices, namely, SiC and GaN, we have witnessed significant improvements in efficiency and power density compared to the current practice of using silicon counterparts. Current designs are challenged by the capability to increase their operating frequency by an order of magnitude or more.

The integration of magnetic components with embedded windings in a PCB is practical and cost-effective. In a GaN-based 1 kW PFC converter, the PCB winding-based inductor was demonstrated to be beneficial since it improved the power density and EMI performance, minimized the labor and cost in assembly, while still maintaining a similar efficiency compared to a conventional litz wire-based design. However, when extending the similar structure to 6.8 kW power, a PCB winding-based inductor suffered dramatically increased winding losses due to the strong MMF associated with the multi-layer PCB structure, as well as high core losses caused by the non-uniform flux distribution in the large-size core. To address those issues, a modular building block approach is proposed in this dissertation. A PCB inductor is formed by an array of pillars in a manner that each elemental pillar handles roughly 750 W of power. The winding loss is reduced by limiting the number of turns for each pillar. The core loss is minimized with a proposed planar

magnetic structure where rather uniformly distributed fluxes were observed in the magnetic core plates. A 3 kW high frequency PFC converter with a 99% peak efficiency is demonstrated as an example. Furthermore, PCB-based designs up to 6 kW are provided.

Moreover, a PCB winding-based inductor offers the opportunity to integrate the balance concept with PCB windings for mitigating CM noises. In a two-phase interleaved PFC converter, the balance technique was employed by adding two additional inductors, L_3 and L_4 , in the return path. With four inductors interleaved and coupled in one magnetic core, the state-of-the-art PCB winding inductor had a rather convoluted structure in such a manner that all interwinding capacitors were intertwined. Consequently, the effectiveness of CM noise mitigation was limited up to a frequency where the parasitic ringing of L_1 and L_2 took over, roughly 7 MHz. To eliminate the unwanted interwinding capacitors, a modified PCB winding structure with a simple physical implementation is proposed. The improved structure decouples the interwinding capacitors of L_1 and L_2 , leading to a much-simplified equivalent circuit. Meanwhile, the new structure maintains the freedom of choosing the proper coupling between L_1 and L_2 while strengthening the coupling between L_1 and L_3 , to facilitate the desired impedance matching, ie., $Z_1/Z_2 = Z_3/Z_4$. In the given example of a 1 kW PFC converter, CM noise suppression is effective in the frequency range of interest up to 30 MHz. The parasitic oscillation of inductors, known to be detrimental for CM noise reduction, is circumvented with the improved magnetic structure.

By applying the PCB-based balance technique to a PFC converter and the shielding technique to an LLC DC/DC converter, significant noise reductions were realized. Thus, for the first time, a single-stage EMI filter could be contemplated to meet the EMI standard in a 1 kW server power supply. The dissertation further offers an in-depth study on reducing the unwanted near-field couplings between the CM/DM inductors and DM filter capacitors as well as unwanted self-

parasitics, such as the ESL of the DM capacitors. Based on FEA simulations, this dissertation clearly demonstrates the adverse effect of displacement current on the polarization of the near field, in a manner that renders the EMI filter ineffective if not properly addressed. The polarization of the near field as a function of frequency was further verified experimentally. A single-stage EMI filter was demonstrated in a GaN-based 1 kW server power supply. The study leads to a better understanding of the nature of the EMI and helps to develop the means to improve filter performance and mitigate the effect of the unwanted mutual couplings.

This dissertation provides a framework for designing a high-frequency PFC/inverter with PCB winding-based magnetics. With the academic contributions in this dissertation, a PCB winding-based inductor can be adopted in a PFC/inverter to improve the power density by 3-5 times, reduce EMI noises by roughly 20 dB μ V, minimize labor and costs in manufacturing, and get incremental improvements in efficiency in an extended power range compared to the current practices. Suffice it to say, the proposed approach in this work enables a paradigm shift in the designing and manufacturing of a PFC/inverter towards the next generation of power supplies.

5.2 Future Work

The proposed PCB winding-based modular building block inductor was demonstrated in a 3 kW PFC converter with 99% peak efficiency in this dissertation. It would be interesting to further verify its performance at a higher power level and investigate the limitations of the proposed approach.

The proposed balance technique exhibited uniform CM noise reduction in the entire frequency range up to 30 MHz in the laboratory test where the position of components was fixed. However,

in a mass production, the variations in the placement of certain components have an impact on the values of parasitic capacitors between the converter and the earth ground. This would potentially renders the balance ineffective. Further efforts are needed to investigate the tolerance of the balance condition in terms of the variations in parasitics.

This dissertation performs a detailed study of the near-field effects inside an EMI filter. However, in a compact switching power supply, there are certain possibilities that the inductors and transformers in the power stage would also impact the filter performance through mutual couplings. The concern might be a more genuine one for a PCB winding-based power supply, where the planar magnetics usually feature a larger surface area compared to a conventional litz wire-based design. Thus, it is valuable to investigate the near-field effects at a system level by taking into account of the effects of those passive components in the power stage.

Appendix A. Effect of α on Input Current Ripple

A minor effect of the coupling for a PFC converter is that it impacts the input current ripple cancellation. Figure A1 illustrates the current of each phase, i.e., i_1 and i_2 , as well as the input current i_{in} for a 1 kW dual-phase interleaved PFC converter. The effect of coupling on input current ripple at point-A (duty cycle=0.2) in Fig. 2.15 is illustrated in Fig. A2. It is observed that coupling has a negative effect on interleaving and input current ripple cancellation. Therefore, at point-A, a weak coupling is preferred for minimizing input current ripple, as well as the DM noise.

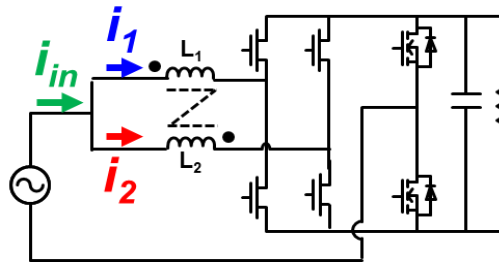


Fig. A1. A dual-phase interleaved totem-pole PFC, and its phase currents (i_1 and i_2) and input current (i_{in}).

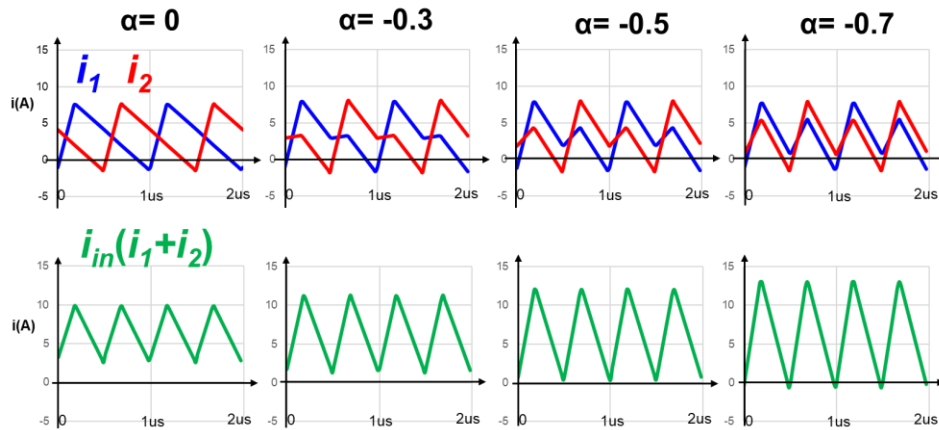


Fig. A2. Currents at point-A (duty cycle = 0.2) in Fig. 2.15 by varying α .

Further observations were conducted at point-D (duty cycle ≈ 0.5) and point-F (duty cycle = 0.7) in Fig. 2.15, as delineated in Fig. A3 and Fig. A4, respectively. At point-D, the input ripple is

almost cancelled since duty cycle is approximately equal to 0.5. Thus, the effect of coupling is negligible. At point-F, the conclusion is similar to that of point-A. Suffice it to say, a weak coupling benefits input ripple cancellation.

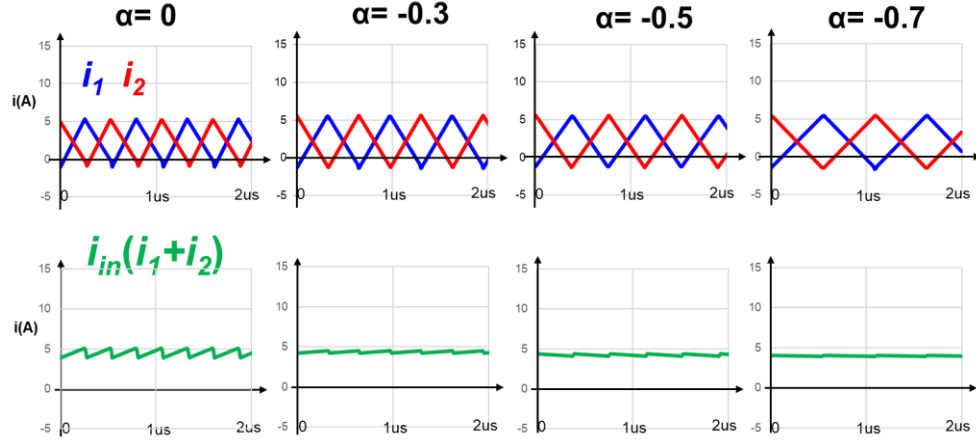


Fig. A3. Currents at point-D (duty cycle ≈ 0.5) in Fig. 2.15 by varying α .

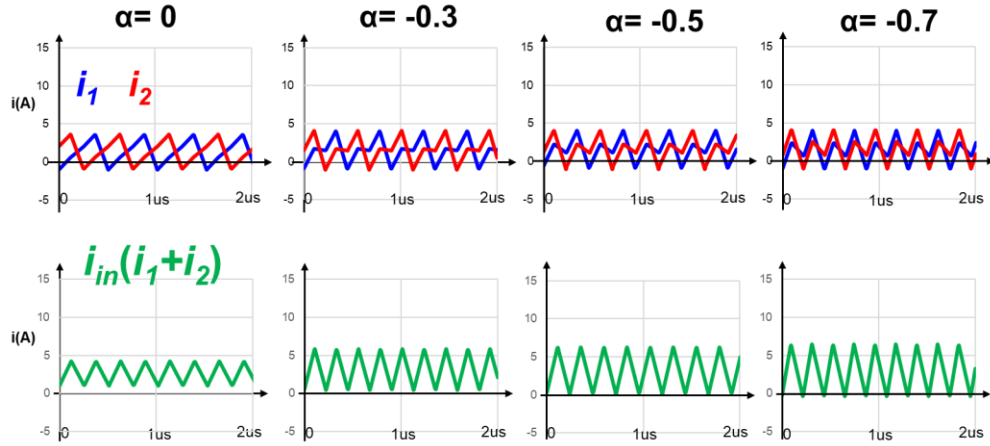


Fig. A4. Currents at point-F (duty cycle = 0.7) in Fig. 2.15 by varying α .

Appendix B. Reluctance Model for Calculating Airgap

$$l_{gi} = f(L, \alpha, A_{ei})$$

The given inductor structure for a 1 kW PFC converter and its reluctance model are illustrated in Fig. B1 (a) and (b).

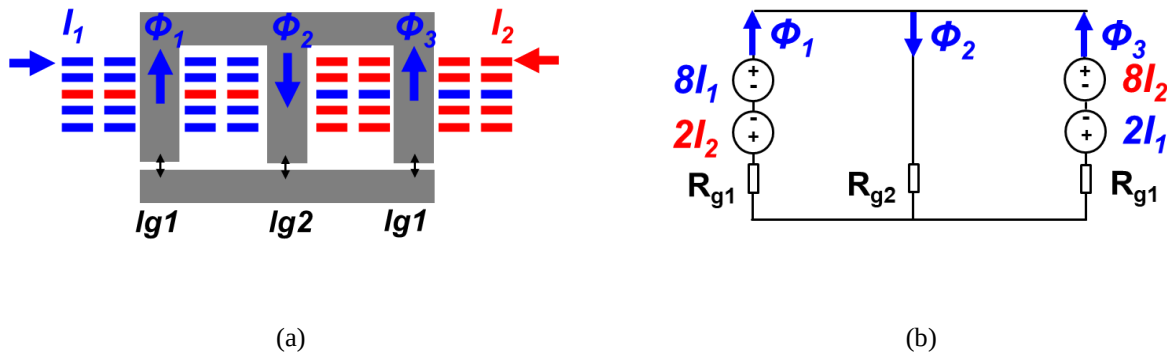


Fig. B1. (a) The PCB winding-based inductor. (b) Reluctance model.

The AC fluxes of $\Delta\Phi_1$, $\Delta\Phi_2$ and $\Delta\Phi_3$ are calculated as

$$\Delta\Phi_1 = \frac{8\Delta i_1 - 2\Delta i_2}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} + \frac{2\Delta i_1 - 8\Delta i_2}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}} \quad (B.1)$$

$$\Delta\Phi_2 = \frac{6(\Delta i_1 + \Delta i_2)}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g1}}{R_{g1} + R_{g2}}, \text{ and} \quad (B.2)$$

$$\Delta\Phi_3 = \frac{8\Delta i_2 - 2\Delta i_1}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} + \frac{2\Delta i_2 - 8\Delta i_1}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}}, \quad (B.3)$$

where the reluctance R_{gi} is a function of airgaps and cross-section areas, as $R_{g1}=l_{g1}/(\mu_0 A_{e1})$, $R_{g2}=l_{g2}/(\mu_0 A_{e2})$.

Based on Faraday's law and the inductor voltage/current relationships, when $i_2=0$, the self-

inductance L can be expressed in terms of $\Delta\Phi_1$ and $\Delta\Phi_3$, as shown in (B.4).

$$L = \frac{8\Delta\Phi_1(i_2 = 0) - 2\Delta\Phi_3(i_2 = 0)}{\Delta i_1} \quad (\text{B.4})$$

Similarly, when $i_1=0$, the mutual inductance M can be expressed in terms of $\Delta\Phi_1$ and $\Delta\Phi_3$, as

$$M = \frac{8\Delta\Phi_1(i_1 = 0) - 2\Delta\Phi_3(i_1 = 0)}{\Delta i_2} \quad (\text{B.5})$$

From (B.4)-(B.5),

$$\alpha = \frac{M}{L} = \frac{8\Delta\Phi_1(i_1 = 0) - 2\Delta\Phi_3(i_1 = 0)}{8\Delta\Phi_1(i_2 = 0) - 2\Delta\Phi_3(i_2 = 0)} \cdot \frac{\Delta i_1}{\Delta i_2} \quad (\text{B.6})$$

Substitute (B.1)-(B.3) into (B.4)-(B.6), airgaps l_{g1} and l_{g2} are calculated as

$$l_{g1} = \frac{100\mu_0}{L(1 - \alpha)} \cdot A_{e1}, \text{ and} \quad (\text{B.7})$$

$$l_{g2} = \frac{\mu_0(68\alpha + 32)}{L(\alpha^2 - 1)} \cdot A_{e2}.$$

Appendix C. CM Noise Model

A general CM noise modeling for boost converter based on the substitution theorem was proposed in [25]. The substitution theorem states that “if the voltage and current associated with any branch of a bilateral network are identified, this branch can be replaced by any combination of elements that will maintain the same voltage across and current through the chosen branches [70].” Figure C1 shows the equivalent circuit model of a totem-pole PFC. The bottom switches of Fig. 3.5 are replaced with the drain-source voltage V_{S1} and V_{S2} waveforms shown in Fig. C2. The top switches are replaced with I_{D1} and I_{D2} . The input and output capacitors are replaced with the voltage waveforms for V_{in} and V_o , respectively. It should be noted that this model is a simplified low frequency model with accuracy only up to a few megahertz. Furthermore, the effectiveness of CM noise source V_o is ignored due to the very large output capacitor in comparison with the input capacitor.

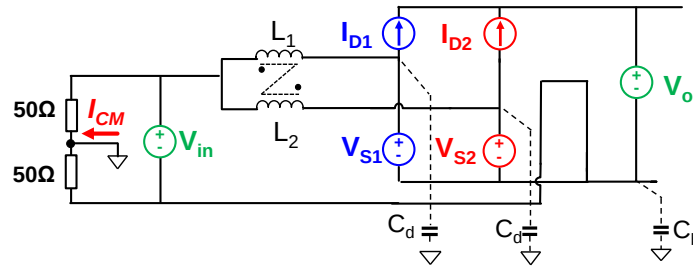


Fig. C1. CM noise equivalent circuit model for a dual-phase totem-pole PFC without balance technique.

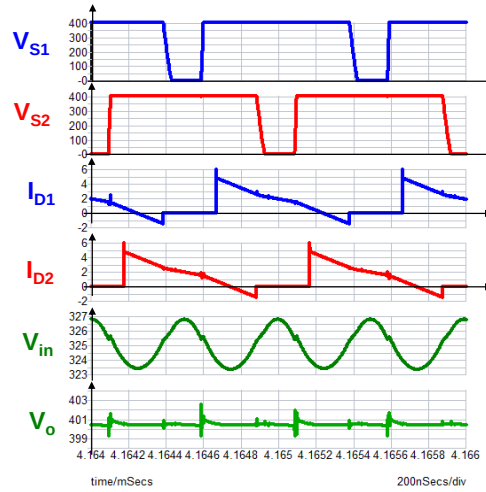


Fig. C2. Voltage and current waveforms.

By applying superposition theorem to noise source V_{S1} , the equivalent circuit can be simplified as shown in Fig. C3 (a). It can be further simplified to Fig. C3 (b) by its Thevenin equivalent circuit.

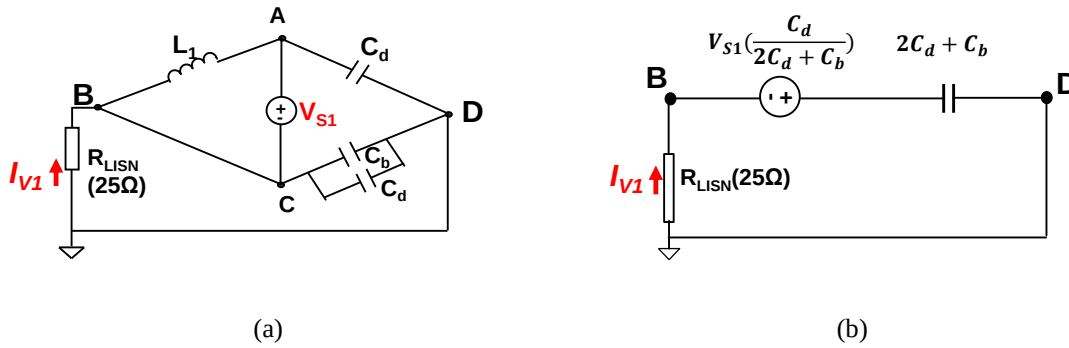


Fig. C3. CM noise equivalent circuit for V_{S1} . (a) Applying superposition to voltage source V_{S1} . (b) Equivalent circuit by applying Thevenin's theorem.

The resistance of LISN (R_{LISN}) can be neglected since it is much smaller than the impedance of $2C_d + C_b$ at the frequency range of interest. This yields the common-mode current $I_{V1}(s)$,

$$I_{V1}(s) \approx sC_d V_{S1}(s). \quad (C.1)$$

Similarly,

$$I_{V2}(s) \approx sC_d V_{s2}(s). \quad (\text{C.2})$$

Applying superposition to noise source V_{in} ,

$$I_{Vin}(s) \approx -\frac{s(2C_d + C_b)V_{in}(s)}{2}. \quad (\text{C.3})$$

From Fig. C1, $V_{in}(s)$ can be expressed as

$$V_{in}(s) \approx \frac{1}{2 - L_1(1 + \alpha_{12})C_{in}\omega^2} [V_{s1}(s) + V_{s2}(s)]. \quad (\text{C.4})$$

The current source I_{D1} and I_{D2} have no contribution to CM noises since they are short circuited from superposition point of view.

Finally, the total CM current under unbalanced condition, $I_{CM}(s)$, can be expressed as follows:

$$I_{CM}(s) = I_{V1}(s) + I_{V2}(s) + I_{Vin}(s). \quad (\text{C.5})$$

For the balanced network, the CM noise equivalent circuit model is shown in Fig. C4.

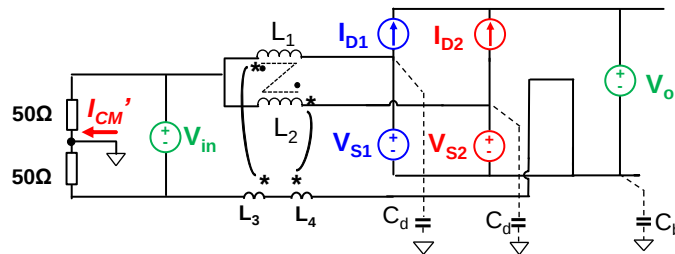


Fig. C4. CM noise equivalent circuit model for a dual-phase totem-pole PFC with balance technique

The CM noise contributed by V_{s1} and V_{s2} are nullified by balance principle. Therefore, the only remaining noise source is V_{in} . Following the same procedure, the total CM current under balanced condition, $I'_{CM}(s)$ is

$$I'_{CM}(s) = I_{vin}'(s) \approx -\frac{s(2C_d + C_b + C_{add})(n-2)n^2}{2(n+2)[2n^2 - L_1(1 + \alpha_{12})(n+2)^2 C_{in}\omega^2]} \cdot [V_{s1}(s) + V_{s2}(s)]. \quad (C.6)$$

The CM noise attenuation by balance technique is expressed as:

$$20\log\left(\frac{I_{CM}(s)}{I'_{CM}(s)}\right). \quad (C.7)$$

Substituting parameters in Table 3.2 into (C.5)-(C.7), the attenuation is calculated as 16 dBuV CM noise reduction at $f_s = 1$ MHz, and 26 dBuV at $f_s = 2$ MHz. The measurement data of 20 dBuV is within the realm of prediction.

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