Chapter 4. High Temperature Barrier Layers

The concept of hybrid electrode-barrier layers is introduced in the first section. The experimental process and ferroelectric properties of PZT films on the electrode-barrier layers are explained in detail in the second section. The fatigue problem and minimization of the fatigue are reviewed, and the improvement of the fatigue properties using the high temperature multi-layer substrates are discussed in the last section.

4.1 INTRODUCTION

In the previous two chapters, high density destructive readout (DRO) FRAM were investigated by primarily focusing on materials processing temperature. The low temperature processing was successfully achieved for the high density DRO FRAM applications by using a modified sol-gel processing. The other approach we have taken for integrating PZT films into high density CMOS devices is to develop novel electrode-barrier layers for high temperature processing. Since the currently used diffusion barrier layers such as TiN and $TiSi_2$ maintain their electrical conductivity only up to 550 °C, high temperature barrier layers are desirable for the integration of PZT films into high density CMOS devices. Ideal electrode materials for the DRO FRAM devices should possesses good electrical conductivity, outstanding thermal and chemical stability, and amenability to dry etching. In particular, the electrode-barrier should be a good diffusion barrier without reacting the ferroelectric materials or the underlying substrate (poly-Si) during high temperature processing. In this research, we propose $Pt/IrO_2/Ir$ hybrid electrode-

barrier layer as high temperature electrode for high density DRO FRAM devices. The fundamental criterion for the selection of Ir metal on poly-Si substrate is the fact that Ir deposited on poly-Si shows excellent thermal stability up to 700 °C and completely prevents oxygen diffusion into polysilicon [1]. Therefore, Ir can serve as both electrode and diffusion barrier layer for high temperature processing. It is also well-established that the interface between the ferroelectric and electrode has strong influence on several degradation properties of PZT films such as fatigue, leakage current, imprint, etc. [2-5] Since Pt/PZT/Pt capacitors show very severe degradation problem, there have been attempts to minimize the fatigue problem by employing oxide electrodes such as RuO_x, Pt/RhO_x, and $La_{1-x}Sr_xCoO_3$ (LSCO), which reduce the accumulation of oxygen vacancies at the electrode/ferroelectric interfaces [6-8]. The fatigue properties have been improved by using the oxide electrodes for PZT-based capacitors. However, the PZT films prepared on these metal oxide electrodes exhibited high leakage currents. It has been observed that relatively good leakage current properties are obtained for the PZT films on metal electrode possibly due to the high Schottkey barrier at the interface [9-10]. Therefore, metal/metal oxide multi-layer electrodes are employed to reduce both fatigue problem and leakage current. In this research, Pt/IrO_2 hybrid multi-layers are prepared as the metal/oxide layer on Ir/poly-Si substrates. IrO_2, conductive metal oxide, has a simple composition and shows very attractive electrical properties such as excellent electrical conductivity. Pt is also widely known electrode to show good electrical conductivity, and outstanding chemical and thermal stability. It is reasonable to believe that the thickness of the conducting oxide layer may play important role in determining the electrical properties of the ferroelectric films. It has been reported that the change in the thickness of metal oxide generates the variation of the Schottkey barrier height at the interfaces, which results in good leakage current of the PZT films prepared on the metal/metal oxide multi-layers [9-10]. Therefore, the IrO_2 thickness are primarily investigated as the important variable in this research. Figure 4.1 illustrates schematic view of the proposed multi-

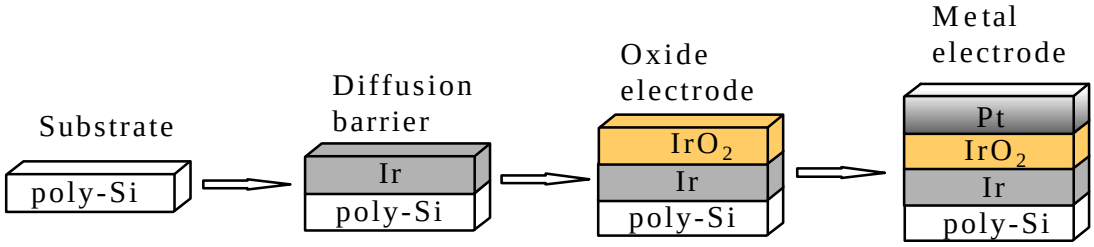

Figure 4.1 Schematic of the proposed electrode-barrier multi-layer structure for high temperature processing.

layer electrode-barrier layer structure for high temperature processing. Thin Ir layer was first deposited on poly-Si substrate for preventing oxygen diffusion, and then Pt/IrO2 layer was prepared on Ir/poly-Si substrate for reducing the fatigue problem and leakage current simultaneously.

4.2. EXPERIMENTAL PROCEDURES

The electrode-barrier, Pt/IrO_2/Ir, was prepared by rf-magnetron sputtering of Pt and Ir targets (2" diameter and 1/8" thick). The sputtering process was carried out at room temperature in a reactive atmosphere of Ar or Ar and O_2 using a Denton rf sputterer. The poly-Si substrates were precleaned using a dilute HF solution to remove a native SiO_2 oxide layer. 80-nm thick Ir-layer was first deposited onto n+ poly-Si/SiO_2/Si wafer using a rf-sputtering process in a reactive atmosphere of Ar. The gas pressure during deposition was maintained at 2.0×10^{-3} torr, and the deposition rate was 10 nm/min. IrO_2 films were then deposited to various thickness from 30 nm to 90 nm onto newly formed Ir/poly-Si substrates using an in-situ rf-sputtering process in a mixture atmosphere of Ar and O_2. The partial pressures of Ar and O_2 were 2.0×10^{-3} torr and 3.0×10^{-3} torr respectively. The deposition rates of IrO_2 were 5 nm/min. Surface compositional analysis of the IrO_2/Ir thin films was performed using electron spectroscopy for compositional analysis (ESCA). The atomic ratio of Ir/O in as-deposited IrO_2 was found to be 29/71, which corresponds to IrO_2^{+04}, but the as-deposited IrO_2 films contained some excess oxygen. These as-deposited IrO_2 and Ir thin films were annealed at 500 °C in O_2 atmosphere to enhance the crystallinity of IrO_2 and Ir films. After the heat-treatment, 80-nm-thick Pt films were deposited on the IrO_2/Ir/poly-Si substrates. All the depositions were carried out at room temperature. The $Pb_{1.1}(Zr_{0.53}Ti_{0.47})O_3$ (PZT53/47) films were prepared on Pt/IrO_2/Ir/poly-Si substrate by the modified sol-gel processing, mentioned earlier, and were finally annealed at 600 °C for 1 hr in O_2 atmosphere. The

thickness of PZT53/47 films was maintained constant at 250 nm throughout the study. The deposition conditions of Ir/IrO_2 top electrode were the same as those of bottom electrode-barriers, and the thickness of top electrodes Ir and IrO_2 were prepared as 80 nm and 30 nm, respectively.

Both the electrodes and PZT films were characterized for their phase formation and orientation by using X-ray diffraction patterns. The ferroelectric properties such as P-E hysteresis loop, fatigue, and leakage current were investigated using a standardized RT66A ferroelectric tester (Radiant Technologies). The composition variation through the depth was characterized by using Auger electron spectroscopy (AES).

4.3. RESULTS AND DISCUSSION

Figures 4.2 shows the X-ray diffraction (XRD) patterns of Pt/IrO_2/Ir/poly-Si electrode-barrier structures with various IrO_2 thickness ranging from 30 nm to 90 nm. It was observed that (110) peak was dominant in the crystalline IrO_2 films, and its relative intensity was enhanced as the thickness of IrO_2 increased. The Pt films grown on the IrO_2 were found to exhibit strong (111) orientation, which was not affected by the thickness of IrO_2 films. Since the grain orientation and crystallization of perovskite PZT films strongly depend on the substrates, the crystallinity of the substrate is very critical in determining the structure of the PZT films. Figure 4.3 shows the XRD patterns of PZT thin films prepared on these electrode-barrier substrates with different IrO_2 thickness. Polycrystalline PZT films prepared on these substrates show (110) major peak, and (100) and (200) peaks, indicating the random grain orientation. It was found that the crystallinity of PZT films were not affected by the thickness of IrO_2 layer. The structural properties of PZT films on the Pt/IrO_2/Ir electrode-barrier layers were not influenced by the

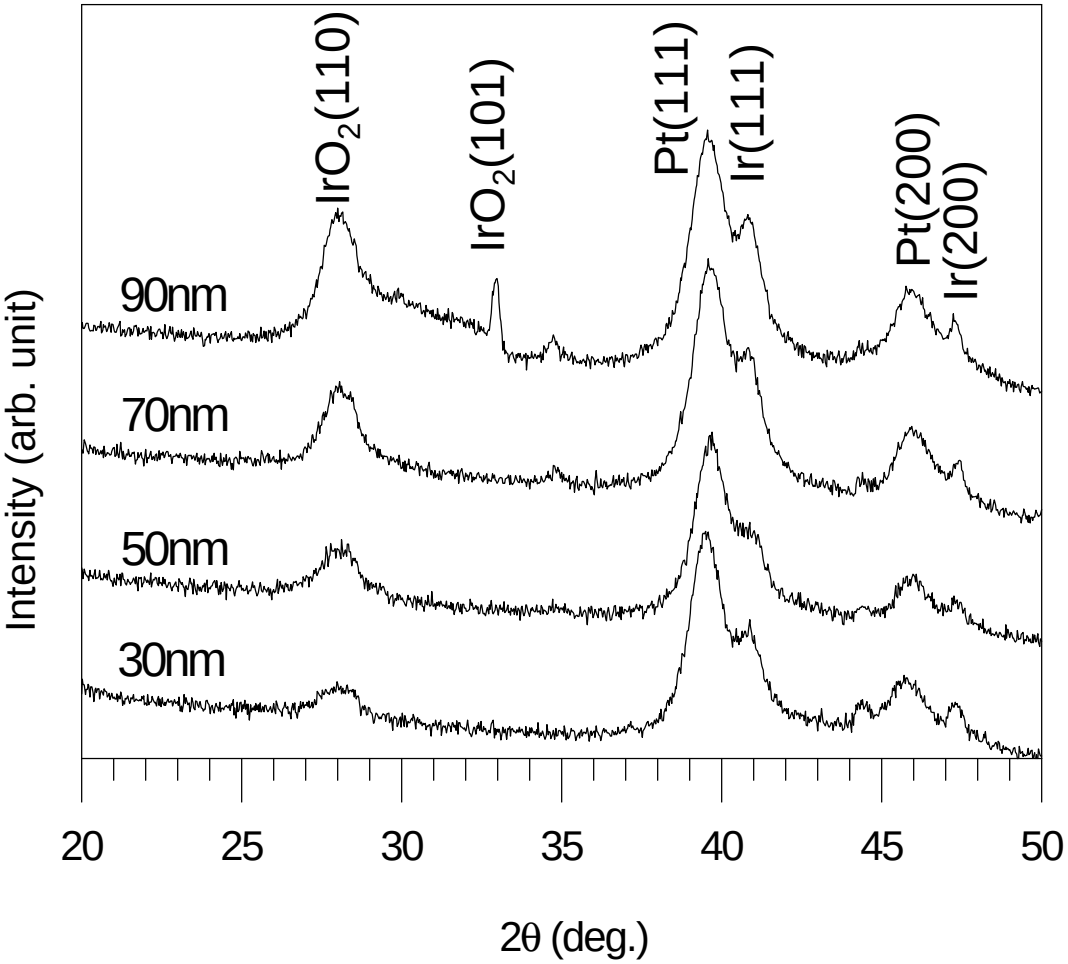

Figure 4.2 XRD patterns of Pt/IrO_2/Ir/poly-Si substrates with different IrO_2 thickness.

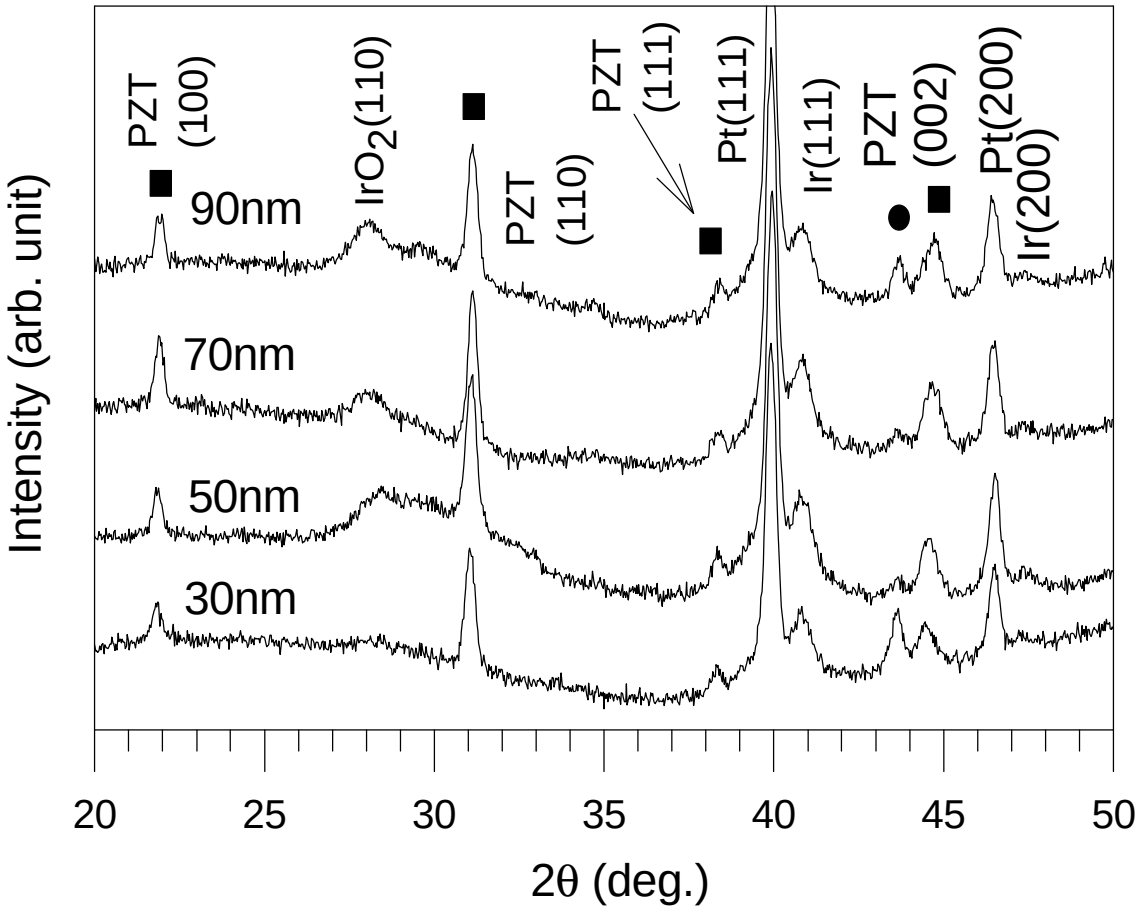

Figure 4.3 XRD patterns of PZT53/47 films at 600 °C on Pt/IrO_2/Ir/poly-Si substrates with different IrO_2 thickness.

thickness of IrO_2 layer. However, the ferroelectric properties of PZT thin film capacitors was strongly dependent upon the thickness of IrO_2 interlayer, as discussed below.

Figure 4.4 shows the P-E hysteresis loops of PZT films on Pt/IrO_2/Ir/poly-Si electrode-barrier substrates with various IrO_2 thickness. The measurement of P-E hysteresis loops was carried out by contacting between the top Pt electrode and the conductive n+poly-Si bottom electrode. Well-defined hysteresis loops were observed for the PZT films on Pt/IrO_2/Ir/poly-Si substrates, indicating that the multi-layer electrode barrier layers could be used as high temperature processing. The same well-saturated hysteresis loop was observed when the Pt underlayer was used as the bottom electrode instead of the n+poly-Si. It implied that undesired insulating SiO_2 layer was not formed on the poly-Si, because Ir layer on the poly-Si works as an excellent oxygen diffusion barrier. The values of both P_r and E_c were plotted as a function of the thickness of IrO_2 interlayer in Figure 4.5. P_r decreased rapidly from 26 to 2 $\mu C/cm^2$ with the increase in IrO_2 thickness from 30 nm to 90 nm. E_c is nearly constant at 45 kV/cm for IrO_2 thickness below 70 nm. The PZT films on Pt/IrO_2/Ir/poly-Si substrate exhibited the maximum P_r value of 26 $\mu C/cm^2$, which is comparable to the P_r value of 28 $\mu C/cm^2$ obtained for the PZT films on conventional Pt/Ti/SiO_2/Si substrate. Since the P_r increased as the IrO_2 thickness decreased, the PZT films were deposited on Pt/IrO_2/Ir/poly-Si substrate with IrO_2 interlayer of about 20 nm in thickness. However, the PZT film peeled off completely during the post annealing process at 600 °C or created large craters of about 10 μm in diameter at the surface of PZT during the post annealing process. The reason of such failures is not clearly understood at this point, but it is presumed that such failures may be due to the large stress developed between Pt and Ir in the bottom electrode during processing at a high temperature of 600 °C or due to the inhomogeneous oxygen diffusion from IrO_2 interlayer through Pt layer. Therefore, there is a minimum thickness of IrO_2 interlayer required for preparing PZT thin films onto Pt/IrO_2/Ir bottom electrodes.

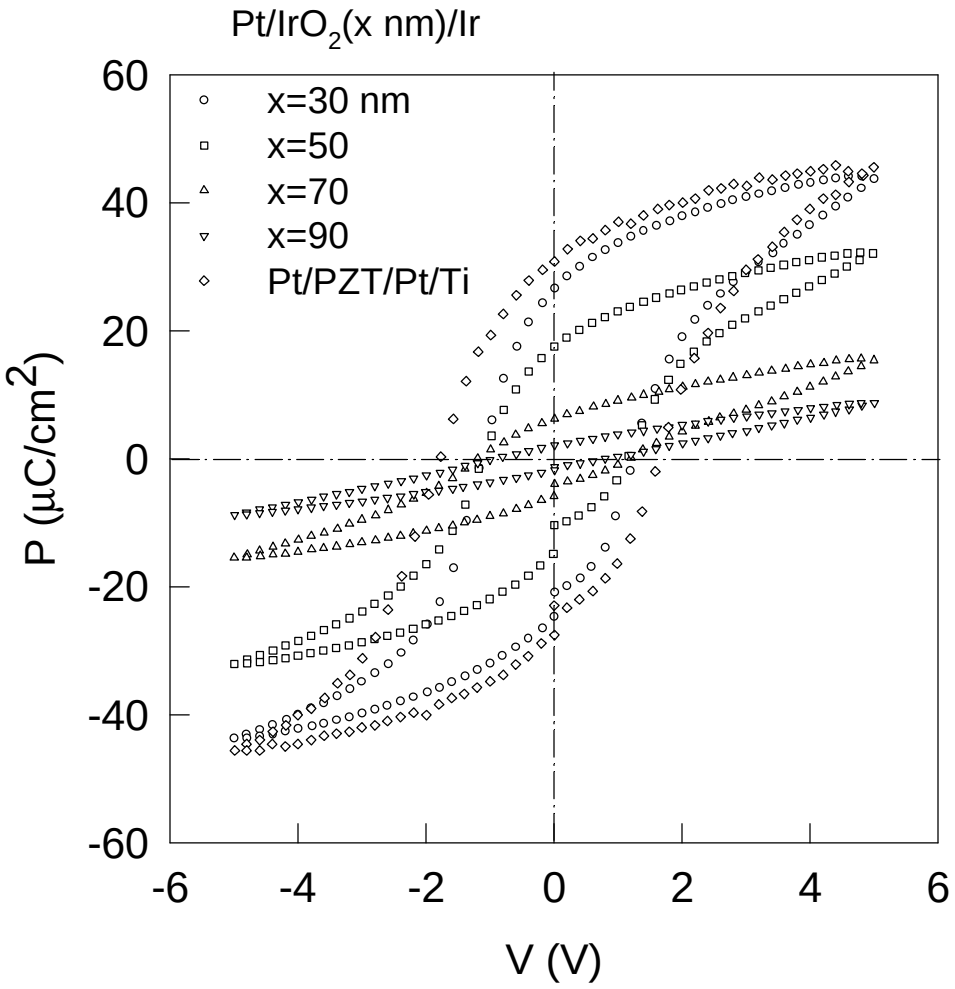

Figure 4.4 Hysteresis loops of PZT53/47 films at 600 °C on Pt/IrO_2/Ir/poly-Si with various IrO_2 thickness.

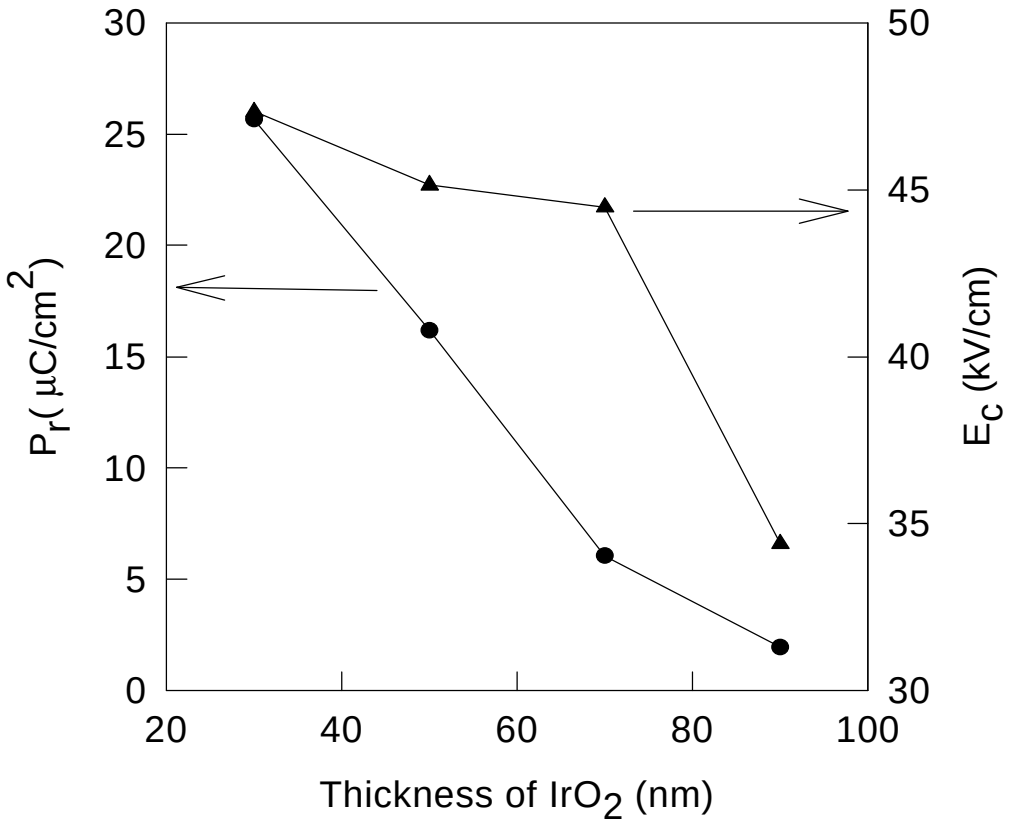

Figure 4.5 The dependence of P_r and E_c of PZT53/47 films on the IrO_2 thickness.

4.4. FATIGUE PROPERTIES

One of major problems in the PZT-based capacitors is the polarization degradation. After a large number of read/write operations, the switchable polarization decreases to a value that is too low to distinguish between two different polarization states. This degradation phenomenon is known as fatigue and is one of the profound problems restricting the development of commercial DRO FRAM devices. In this section, the main source for fatigue problem and minimization of the fatigue are discussed. In addition, the improvements in the polarization degradation by using the $Pt/IrO_2/Ir$ hybrid multi-layers are presented.

4.4.1 Literature Review

Fatigue behavior of ferroelectric materials has been investigated for several years, and various mechanisms and models have been proposed to explain the undesired degradation phenomena. In particular, the accumulation of space charge has been considered as the major source of fatigue [11-16]. Karan [15] developed a theoretical expression for fatigue induced by space charge entrapment in ferroelectric material, which results in an increase in the interfacial resistance and decrease in the interfacial capacitance. Zheludev [16] suggested a planar model in which an inactive surface is formed at the electrode-ferroelectric interfaces due to space charge, and thus reduces an amount of switched charge. Kudzin et al [12] explained fatigue based on the accumulation and resorption of space charge at the grain boundaries, which loses the capacity of domain wall to move, and the resultant value of switched charge diminishes. Duiker et al [4] proposed dendritic growth of oxygen-deficient filaments as the source of fatigue. It was postulated that during the domain switching, impact ionization (Ti^{+4} to Ti^{+3} conversion in PZT) of the ferroelectric material occurs near the electrodes, which is followed by O^- diffusion away from

the ion. This resulted in oxygen deficient regions near the electrode-ferroelectric interface, giving rise to a decrease in the switched charge. In Yoo et al [2-3] proposed a quantitative fatigue model for Pt/PZT/Pt capacitors in which defect movement under alternating pulses and defect entrapments such as grain boundaries, domain boundaries, and electrode-ferroelectric interfaces are assumed as the source for fatigue. The point defects could be either intrinsic or extrinsic. Extrinsic defects are impurities that are incorporated into the ferroelectric films during processing and can be prevented by controlling the processing conditions. The intrinsic defects could have two different types. One is defects that maintain the stoichiometry (Schottky), and the other is defects that change the stoichiometry in the ferroelectric materials.

Schottky defects in ABO_3 films can be expressed by a quasi-chemical reaction (in Kroger-Vink notation) as :

$$A_A + B_B + 3O_O \Rightarrow V_A'' + V_B'' + 3V_O'' + A_s + B_s + 3O_s$$

where A_A, B_B, $3O_O$ represent occupied A, B, and O sites, respectively; V_A'', V_B'', and $3V_O''$ represent vacancies of A, B, and O atoms; and A_s, B_s, and $3O_s$ represent the Schottky defects. A typical example of defects that alter the stoichiometry are vacancies that are generated by the vaporization of one or more volatile components in the multi-component system. In the case of PZT, the PbO component volatilizes at temperature as low as 550 °C, producing oxygen and lead vacancies as described below :

$$Pb_{Pb} + Ti_{Ti} + Zr_{Zr} + 3O_O \Rightarrow xPbO + xV_{Pb}'' + xV_O^{oo} + (1-x)Pb_{Pb} + Ti_{Ti} + Zr_{Zr} + (1-x)O_O$$

Since the net local field is not symmetric due to the internal field in the ferroelectric materials, the mobile defects (mainly oxygen vacancies) tend to move towards the electrode-ferroelectric

interfaces. Additionally, these interfaces have the large interfacial energy, which provides low potential energy sites for the defects and thus generates the defect entrapments around the ferroelectric/electrode interfaces.

Several experimental evidences indicate that the accumulation of oxygen vacancies at the electrode/ferroelectric interfaces has direct influence on the fatigue properties of the ferroelectric films. Kanzig first discussed the role of oxygen vacancies at the surfaces of ferroelectric materials [17]. The presence of surface space charge in very small ferroelectric $BaTiO_3$ particles was experimentally verified by using X-ray and electron diffraction experiments. Different symmetry was observed between a surface layer of about 10 nm thick and the bulk. A tetragonal surface layer was found above the Curie temperature, while the bulk showed cubic structure. In the case of PZT thin films capacitors, Scott et al [18] have investigated the oxygen concentration through the Pt/PZT/Au capacitors before and after fatigue by using Auger electron spectroscopy (AES). Using this AES technique, it was possible to determine the composition profile through the depth of the capacitors. Figure 4.6 shows the AES depth profile for Pt/PZT/Au capacitors they investigated. It was observed that after measuring fatigue properties, the oxygen concentration at the interface decreased to almost 50 % of its value in the bulk, indicating the presence of oxygen vacancies at the interface. Since the symmetric data are obtained at the top and bottom of the film, knock-in or related artifacts generated by the sputtering process in AES did not seem to affect the obtained data. It is postulated that most of these oxygen vacancies are compensated for by the Pb vacancies and only small amount of oxygen vacancies trap electrons and generate space charge regions.

The development of interface space charge layers has been studied by measuring capacitance of Pt/PZT/Pt capacitors [19]. The measured capacitance (C_m) is composed of three capacitors in series: a capacitor representing the bulk (C_B) of the ferroelectric film and two representing the interfaces (C_i). The total capacitance of the sample can be expressed as

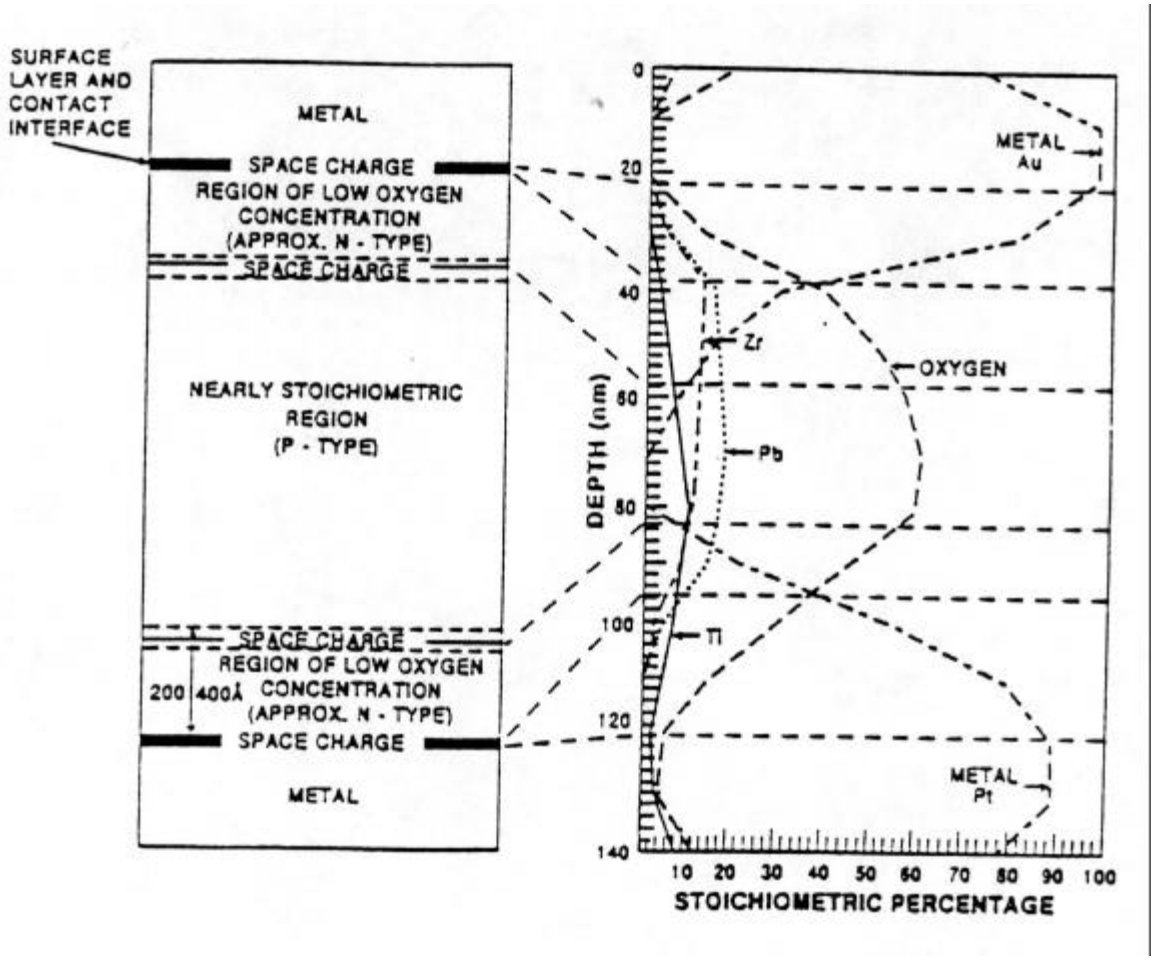

Figure 4.6 Auger microprobe data for fatigued PZT films with Pt and Au electrodes [18].

$$1/C_m = 1/C_B + 2/C_i$$

$$d_m/\varepsilon_r\varepsilon_o A = d_B/\varepsilon_B\varepsilon_o A + 2d_i/\varepsilon_i\varepsilon_o A$$

where d_m and ε_r are the total sample thickness and dielectric constant respectively; d_B and ε_B express the bulk thickness and dielectric constant respectively; represent the interfacial layer thickness and dielectric constant respectively; ε_o is the permittivity of free space and A is the sample area. Since $d_i << d_B$ and $d_B \approx d_m$, the equation can be approximated as:

$$1/C_m = d_m/\varepsilon_B\varepsilon_o A + 2/C_i$$

Therefore, by plotting $1/C_m$ as a function of d_m, $1/C_i$ is obtained from the y-axis intercept and ε_B from the slope. Lee and Desu [19] have calculated the interfacial capacitance and the bulk permittivity after each period of cycling by measuring the capacitance of the samples as a function of thickness and number of fatigue cycles for Pt/PZT/Pt capacitors. It is observed that the bulk dielectric permittivity remains constant while the interfacial capacitance increases with increasing in the switching cycles. These results indicate that a depletion region is increased due to the accumulation of oxygen vacancies at the interface with fatigue in progress.

4.4.2 Minimization of the fatigue

Based on the understanding of fatigue model discussed in previous section, there have been several attempts to overcome the fatigue problem. In general, two reasonable approaches have been taken for solving the degradation problem: (1) reducing the possibility of defect entrapment by controlling the interface state and (2) restricting the defect density. To control the defect density can be pursued by doping donor to compensate for the oxygen vacancies [20] or

developing a novel ferroelectric materials which have a low intrinsic defect concentration. La, Nb, Mn, and Mg have been used as the donor dopants [20]. It has been shown that Nb donor dopant addition to PZT film can reduce both the fatigue and leakage current on Pt and RuO_2 electrode. The alternative ferroelectric materials with low intrinsic defect concentration have been investigated, and several ferroelectric oxides belonging to the pyrochlore, layered structure and tungsten bronze families are considered for possible memory applications. In particular, $SrBi_2(Ta_xNb_{1-x})_2O_9$ family of layered structure are very strong candidate for fatigue free ferroelectric thin films applications [21]. The fatigue-free properties of the Bi-layered structure family might be attributed to the lack of any volatile component which could cause the formation of intrinsic vacancies such as oxygen vacancies in the PZT-based capacitors. However, it is very complicated task to process new ferroelectric materials which replaces PZT films for memory application. The alternative materials should compete against other factors favoring PZT films such as low processing temperature and outstanding ferroelectric properties. Therefore, relatively feasible approach for overcoming the fatigue problem is to improve interface state by stabilizing the electrode/ferroelectric interface. The stability of electrode/ferroelectric interface could be obtained by using an oxide electrode for the ferroelectric capacitors. Transition metal oxides such as RuO_2, IrO_2, OsO_2, RhO_2 etc show high electrical conductivity and good thermal stability up to high temperatures. It has been suggested that oxide electrodes work as a sink for oxygen vacancies during the films processing and fatigue measurement [22]. It is postulated that when the oxygen vacancies accumulate on the electrode/ferroelectric interfaces, the oxygen vacancies are compensated for by the oxygen atom supplied by the metal oxide electrode. This capability of providing the oxygen atoms is dependent upon the electrode. Thus, if the electrode can tolerate the oxygen vacancies well, the degradation problem will be minimized. The Pt electrode has poor affinity to oxygen, and thus possesses very low tolerance limit for oxygen vacancies, which results in very severe degradation problem of Pt/PZT/Pt capacitor. On the other hand, LSCO, RuO_2, and

IrO_2 electrodes have good tolerance limit for oxygen vacancies, and thus yield excellent fatigue properties. In this research, IrO_2 is selected over other metal oxides due to the good compatibility with Ir and easy in-situ processing. We also put Pt metal layer on the IrO_2/Ir layer for enhancing a leakage current and strengthening the fragile IrO_2 oxide electrode.

4.4.3. Results and Discussion

Figure 4.7 shows the polarization fatigue behavior of Ir/IrO_2/PZT/Pt/IrO_2(x(nm))/Ir/poly-Si capacitors with different IrO_2 interlayer thickness. The normalized difference between the switched and non-switched polarization, that is, P*-P^, was plotted as a function of switching cycles applied to the capacitors. It was observed that the fatigue properties of PZT capacitors were considerably improved as the IrO_2 thickness decreased. The PZT capacitor with 30 nm in thick IrO_2 interlayer showed polarization fatigue of less than 10% even after 10^{11} switching cycles. It was found that the replacement of Pt/Ti electrode structure with Pt/IrO_2/Ir structure generated the good fatigue resistance. Although the mechanism of polarization fatigue is not completely understood, it has been well-established that the loss of switchable polarization with repeated polarization reversal is due to pinning of domain walls which inhibits switching of the domains. It was suggested that trapping of oxygen vacancies at the interfaces play an important role in the domain pinning, as discussed earlier. In this experiment, our results of fatigue testing as well as P-E hysteresis measuring, as shown in Figure 4.4 and 4.6, are believed to be related with the oxygen vacancies in the bulk of PZT or near the interface between PZT and bottom Pt. In order to confirm these assumptions, we investigated the depth profiles of PZT thin films prepared on Pt/IrO_2/Ir/poly-Si as well as on Pt/Ti/SiO_2/Si using Auger electron spectroscopy (AES). Figure 4.8 (a), (b), and (C) show the AES depth profile of PZT/Pt/IrO_2(30nm)/Ir/poly-Si, PZT/Pt/IrO_2(90nm)/Ir/poly-Si, and PZT/Pt/Ti/SiO_2/Si, respectively. The measurements of AES

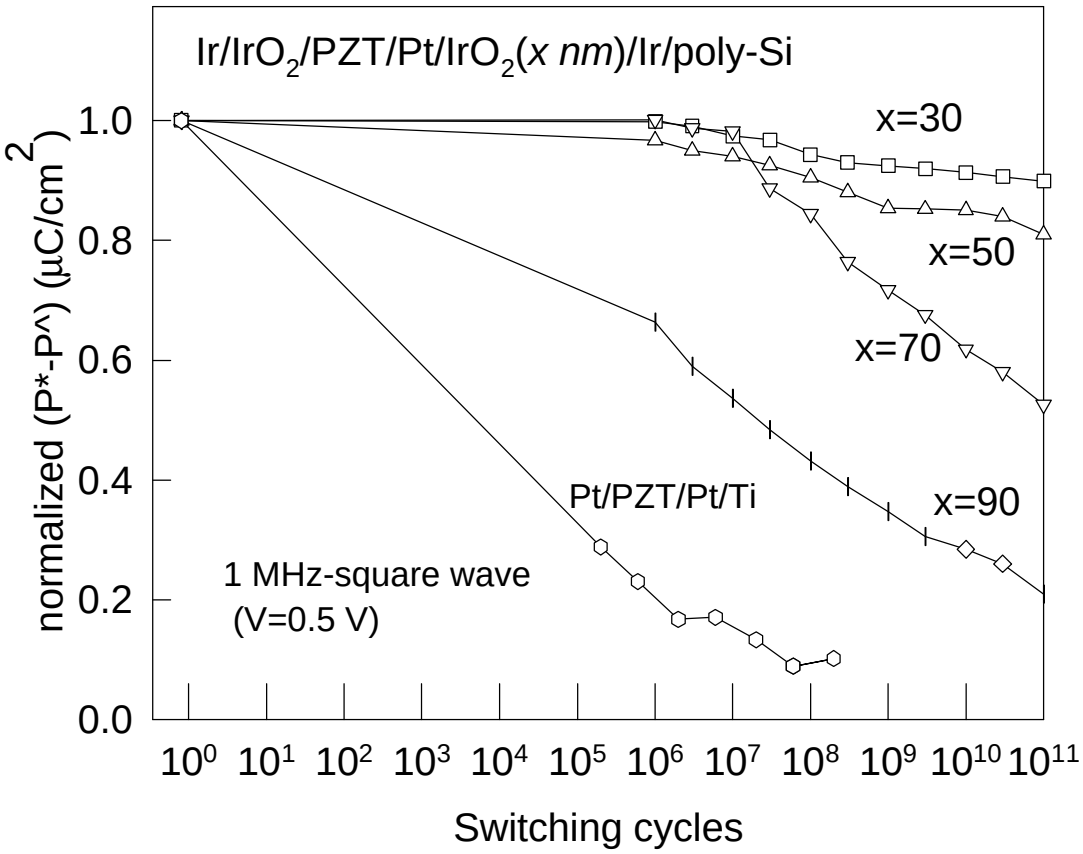

Figure 4.7 Polarization fatigue behaviors of PZT53/47 films on Pt/IrO_2/Ir/poly-Si substrates with various IrO_2 thickness.

depth profile were performed at a sputtering rate of about 2.5 nm/min, and during AES depth profile measurement, more emphasis was put on the oxygen profiles in PZT bulk and near the interface between PZT and Pt than on the profiles of the other elements, such as Pb, Ti, Zr, since Zr interfered with Pt or Ir in AES analysis. Oxygen depth profiles were found to be quite different in PZT thin films prepared on different substrates. It was observed that the PZT films on Pt/IrO_2(30nm)/Ir/poly-Si substrates maintained nearly constant oxygen concentration with depth, especially toward Pt surface (Fig. 4.8 (a)). On the other hand, the PZT films on Pt/Ti/SiO_2/Si and Pt/IrO_2(90nm)/Ir/poly-Si substrates possessed an apparently decreasing oxygen concentration as the interface of PZT and Pt was approached (Fig. 4.8 (b) and (c)). Scott et al [18] noticed a loss of polarization after fatigue cycling as the oxygen concentration decreased near the electrodes, resulting in the accumulation of oxygen vacancies. Additionally, a quantitative fatigue model proposed by Desu [5] predicted that fatigue could be minimized by preventing space charge formation arising out of oxygen vacancies at the interface. This hypothesis explained our results that the PZT films on Pt/Ti/SiO_2/Si substrate, which contained higher oxygen vacancies at the PZT/Pt interface, exhibited very poor fatigue properties, as compared to that of PZT films on Pt/IrO_2/Ir/poly-Si substrate, which contained lower oxygen vacancies at the PZT/Pt interface. It was observed that the PZT films on Pt/IrO_2(30nm)/Ir/poly-Si substrate exhibited only 10% polarization loss even after 10^{11} cycles. The PZT capacitor with optimum IrO_2 thickness of 30 nm exhibited excellent insulating properties such as leakage current density of $1x10^{-7}$ A/cm^2 at an applied electric field of 150 kV/cm. We have also investigated the effect of the top electrode on the ferroelectric properties of PZT films on Pt/IrO_2/Ir/poly-Si. Ferroelectric properties of PZT capacitor, however, did not largely depend either on the structure of the top electrode (such as Ir, IrO_2, Pt/IrO_2 and Ir/IrO_2) or on the thickness of IrO_2.

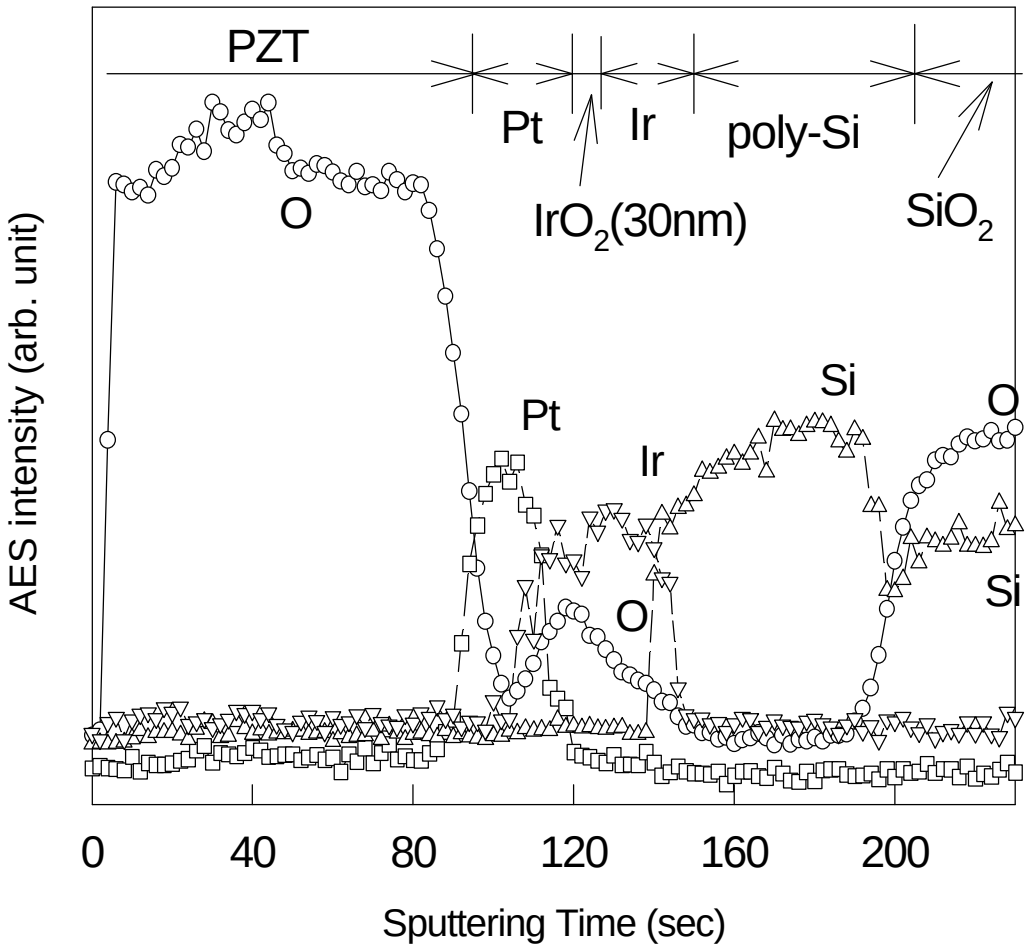

Figure 4.8 (a) Auger depth profile of PZT53/47 films on Pt/IrO_2(30 nm)/Ir/poly-Si substrates.

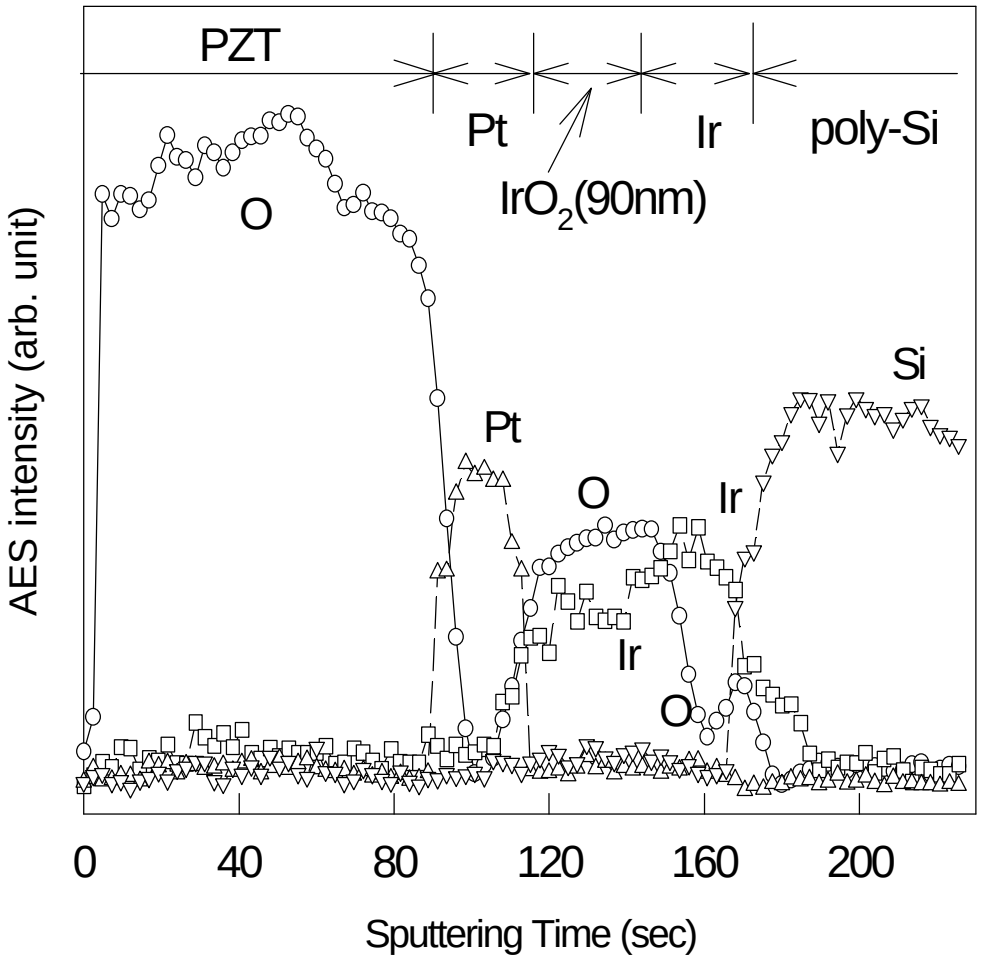

Figure 4.8 (b) Auger depth profile of PZT53/47 films on Pt/IrO_2(90 nm)/Ir/poly-Si substrates.

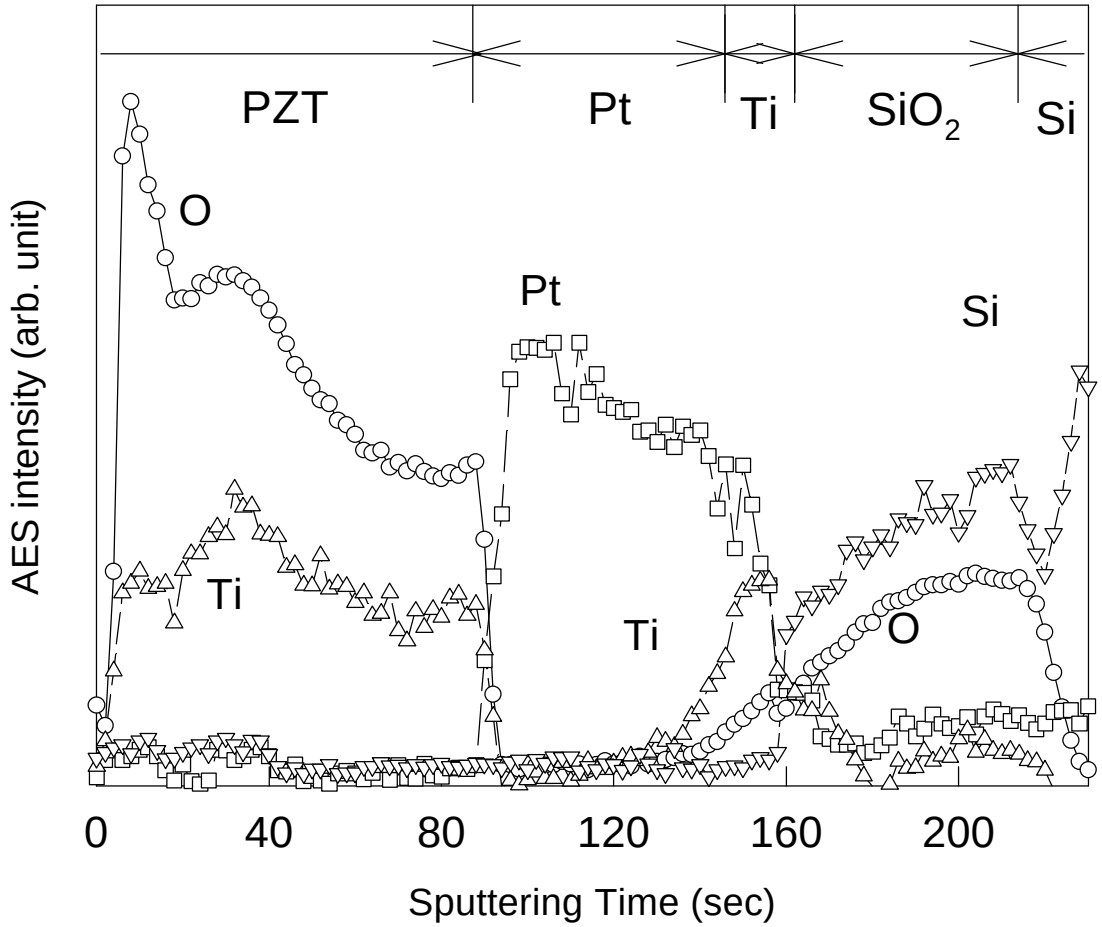

Figure 4.8 (c) Auger depth profile of PZT53/47 films on Pt/Ti/SiO_2/Si substrates

4.5. SUMMARY

Novel diffusion barrier layers (Ir and IrO_2) were developed for high temperature processing, and randomly oriented PZT53/47 films were successfully prepared on Pt/IrO_2/Ir/poly-Si substrate at 600 °C by a modified sol-gel processing. The PZT films on Pt/IrO_2/Ir/poly-Si substrate exhibited good ferroelectric properties such as remanent polarization of 26 $\mu C/cm^2$ and coercive electric field of 47 kV/cm, showed minor polarization fatigue of 10% after 10^{11} cycle, and displayed low leakage current density of $1x10^{-7}$ A/cm^2 at an applied voltage of 150 kV/cm. It was found that the thickness of IrO_2 interlayer between Pt and Ir has a significant influence on the fatigue properties of PZT capacitors. A 30 nm thick IrO_2 interlayer was found to exhibit the best fatigue properties. The excellent fatigue resistance was attributed to lower oxygen vacancies near the PZT/Pt interface. The low temperature processing and high temperature electrode/barrier layers promise to overcome major problems of PZT integration into high density memory devices.

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