Design Optimizations of LLC Resonant Converters with Planar Matrix Transformers

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(Abstract)

LLC resonant converters have been a popular choice for DC-DC converters due to their high efficiency, high power density, and hold-up capability in power supplies for communication systems, datacenters, consumer electronics, and automobiles. With the rapid development of wide-bandgap devices and novel magnetic materials, the push for higher switching frequencies to achieve higher power densities at lower costs is gaining traction.

To demonstrate high efficiency and high power density, the Center for Power Electronics Systems (CPES) at Virginia Tech designed an 800W, 1MHz 400V/12V LLC converter for future datacenters, which could achieve a peak efficiency of 97.6% and a power density of 900 W/in^3. However, with the ever-increasing demand for online services, the performance of power delivery must also be simultaneously improved to keep pace with the demand.

The focus of this thesis is improving the performance of CPES' previous 400V/12V LLC converter by investigating different aspects of its design and operation. Ultimately, design guidelines are proposed, and improvements are demonstrated to effectively achieve higher efficiency and higher power density than the previous CPES converter.

Multiple aspects of the LLC converter's design and structure are investigated to further improve its performance, and three main areas are the focus of this thesis. The output-side termination design of the planar transformer is investigated and modeled, and design guidelines

for filter capacitor selection are provided for optimal efficiency. Next, the existing shielding technique for matrix transformers, which helps reduce common-mode (CM) noise without compromising on efficiency, is investigated for asymmetry and current-sharing issues, and modifications have been proposed to improve its efficiency. Thirdly, the LLC converter's switching frequency is optimized to improve its performance over the previous CPES converter. Finally, the hardware results with the proposed improvements are demonstrated, and the converter's performance is compared with the previous CPES converter as well as other recent proposed solutions.

Design Optimizations of LLC Resonant Converters with Planar Matrix Transformers

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(General Audience Abstract)

The electricity demand by datacenters has been growing exponentially over the past few decades, especially due to the boom of artificial intelligence in addition to other internet services. This has resulted in a requirement to continually improve the efficiencies of the power delivery from the grid, through the datacenter power architecture, and finally to the loads on the server racks. The overall datacenter power architecture has been improved over time to improve the total efficiency. However, the performance of each stage along the power architecture must be improved to keep in pace with the energy demand.

The focus of this thesis is to improve the performance of the 400V/12V DC-DC stage for future datacenters. Previously, the Center for Power Electronics Systems (CPES) at Virginia Tech developed a 1MHz 800W 400V/12V LLC converter with 97.6% peak efficiency and 900W/in^3 power density. However, the performance of the converter must be further improved to stay ahead of the competition and keep in pace with the increasing energy demand.

Multiple aspects of the LLC converter's design and structure are investigated to further improve its performance, and three main areas are the focus of this thesis. Firstly, the high-frequency termination design, or how different components are interconnected and arranged, is studied, and a capacitance selection guideline is proposed to maximize the efficiency. Next, the

existing shielding technique for matrix transformers, which helps reduce common-mode (CM) noise without compromising on efficiency, is investigated for asymmetry and current-sharing issues, and modifications have been proposed to improve its efficiency. Thirdly, the LLC converter's switching frequency is optimized to improve its performance over the previous CPES converter. Finally, the hardware results with the proposed improvements are demonstrated, and the converter's performance is compared with the previous CPES converter as well as other recent proposed solutions.

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Chapter 1. Introduction

1.1 Datacenter Power Architectures

Since the turn of the century, the internet has become an integral part of almost everyone's life, with it being used for increasingly widespread tasks, ranging from launching space shuttles to purchasing groceries. Moreover, with the advent of artificial intelligence, the internet traffic to and from datacenters has exploded exponentially [1], as Fig. 1.1 shows.

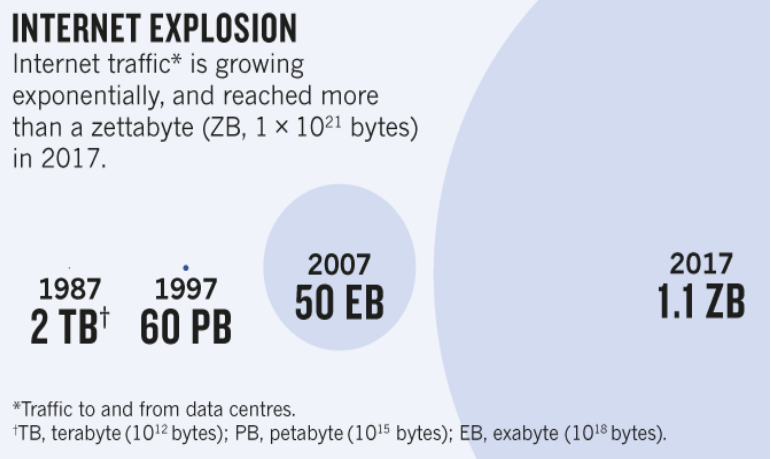


Fig. 1.1. Internet traffic growth since 1987.

Internet traffic increased 30,000 times from 1987 to 1997, further increasing by over a thousand times in the next 10 years. In the past decade, with the advent of data-hungry artificial intelligence in addition to other online services like banking, e-commerce, social media, and cloud storage, internet traffic has boomed to a mammoth 1.1 ZB.

This trend is expected to continue into the future, as forecasts suggest that the total electricity demand of information and communication technology (ICT) will accelerate in the 2020s to up to

20% of the total electricity demand, and that datacenters will take up almost around 40% of that, as shown in Fig. 1.2.

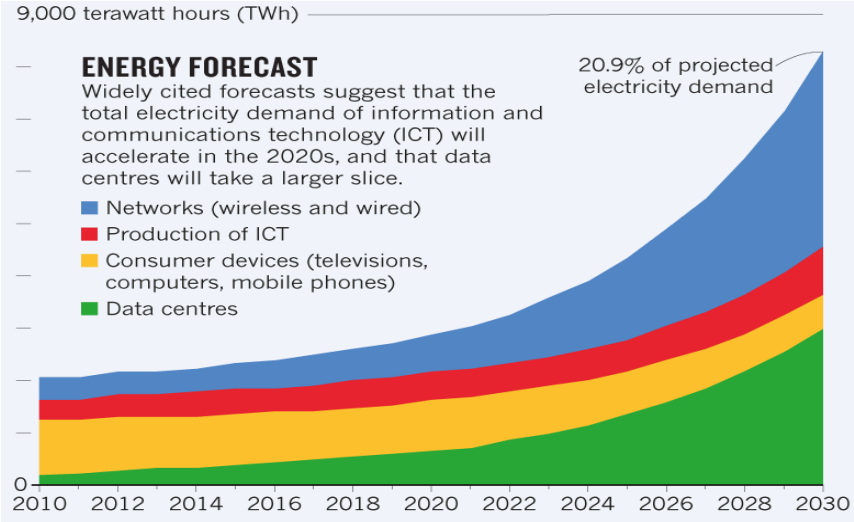


Fig. 1.2. Energy consumption forecast for ICT.

Because of the increased energy demand by datacenters, big tech companies such as Google, Amazon, Facebook, and Microsoft are building massive datacenter farms called hyperscale datacenters to serve small- and medium-sized enterprises, which can consume up to 200 MW per datacenter. The estimated annual spending on datacenter systems worldwide is almost $200 billion, out of which around 40% is estimated to be spent on the power and cooling infrastructure. Given the rising demand for online services, efficiency gains at every stage are essential to maintaining a sustainable level of global energy consumption, particularly for countries seeking to reduce their carbon footprint.

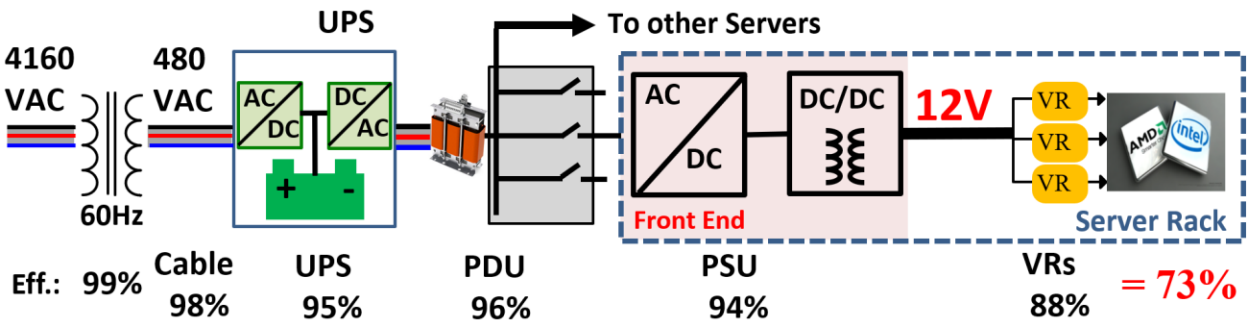


Fig. 1.3. Traditional 12V-bus architecture for datacenters.

The datacenter power architecture is one significant area where efficiency could be improved. Fig. 1.3 shows the conventional 12V bus architecture for datacenters, with the approximate efficiencies of each stage. The 60Hz transformer is followed by the AC/DC and the DC/AC stages necessary to connect the uninterruptible power supply (UPS). This is followed by the power distribution unit (PDU), which includes another 60Hz transformer, as well as switches and relays to distribute the AC voltage to different server cabinets. Within each server cabinet, there are power supply units (PSUs) consisting of the AC/DC and isolated DC/DC stages, which are front-end converters, finally followed by the voltage regulators (VRs) that supply various loads. Adding up the efficiencies of these numerous stages results in a net efficiency of only 73% [3][4].

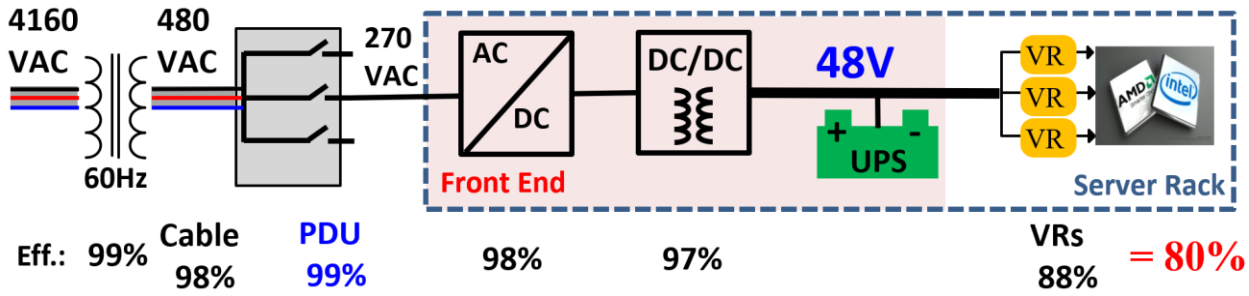
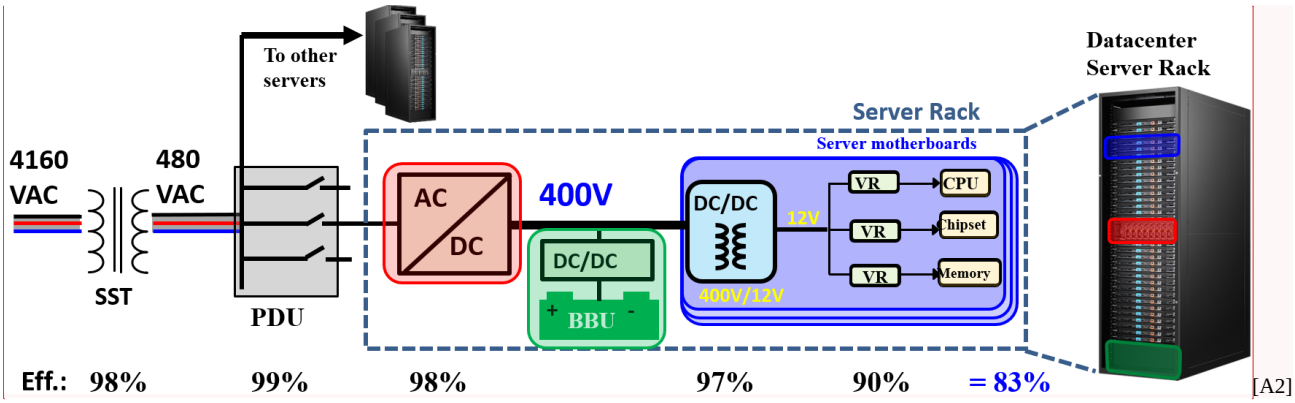


Fig. 1.4. Current 48V-bus architecture for datacenters.

Due to the low bus voltage and multiple conversion stages in the traditional 12V-bus architecture, Google came up with an improved architecture with a higher bus voltage of 48V

[5][6]. The PDU now has only switches and relays to distribute the power to different cabinets, and hence has higher efficiency. Moreover, the UPS is now moved to the 48V DC bus inside the server racks, thereby eliminating the AC/DC and DC/AC stages required to connect the UPS to the AC side, and hence reducing the number of power-conversion stages. This fact, coupled with the higher bus voltage having lower i^2R losses, results in a much higher net efficiency of 80%, 7% higher than the traditional 12V bus architectures; this is approximately equal to the energy produced by 33 nuclear power plants every month [7].



[A2]

Fig. 1.5. 400V-bus architecture for future datacenters.

Recently, the 400V DC bus architecture has gained traction due to its much lower i2R losses, and subsequently lower cost due to fewer transmission cables as compared to the 48V bus architecture [8][9]. This results in a higher overall power architecture efficiency of 83%, 10% higher than the traditional 12V architecture; this amount is approximately equal to the energy produced by 47 nuclear power plants every month. This architecture requires a DC/DC converter that can directly step-down the 400V bus voltage to 12V to supply the VRs. Industry standards for this on-board converter were proposed by the International Electronics Manufacturing Initiative (iNEMI) [10], as summarized in Table 1.1.

Table 1.1. iNEMI specifications for the DC/DC converter.

ITEM	Minimum	Nominal	Maximum
Input Voltage	360Vdc	380Vdc	400Vdc
Efficiency	92%@10% Load	96%@Full Load	97%@50% Load
Output Voltage	11.60Vdc	12.00Vdc	12.60Vdc
Output Current	0A		62.5A
Packaging	DOSA Quarter Brick Form Factor		

1.2 Review of Previous CPES 400V/12V LLC Converter

The iNEMI specifications for the DC-DC converter require a high voltage step-down ratio, high output-current capability, high efficiency, and high power density, which is challenging. Hard-switching pulse-width modulation (PWM) converters cannot achieve the required efficiency and power density due to their high switching losses at higher frequencies. Among soft-switching PWM converters, different candidates, such as asymmetrical half-bridge converters and phase-shifting full-bridge PWM converters, have been implemented as DC/DC converters [11][12]. However, they must sacrifice their normal operation efficiency to accommodate the large input voltage range for hold-up requirements in such applications.

Resonant converters are great choices for DC/DC converters due to their ability to achieve soft-switching over the entire load range and the lower turn-off losses incurred for their primary devices (as compared to their hard-switching counterparts), resulting in high efficiencies and high power densities. Among them, LLC converters have been demonstrated to be promising candidates for DC/DC converters, due to their ability to achieve high gains for hold-up, while maintaining high

efficiencies during normal operations, while also reducing the electromagnetic interference due to their soft-switching capability [13][14][15].

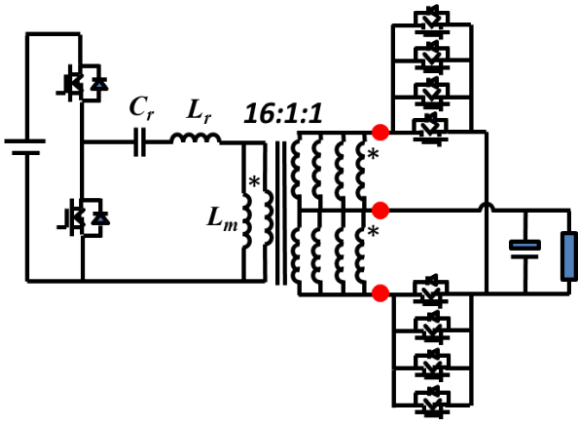


Fig. 1.6. The conventional half-bridge LLC resonant converter.

However, for a high output current of 67A (12V, 800W), the transformer's secondary winding loss and the secondary-rectifier (SR) conduction loss are too high to achieve the required efficiencies. Hence, multiple SRs and secondary windings must be effectively paralleled to reduce the conduction losses, as shown in Fig. 1.6. However, at the locations denoted by the red dots in Fig. 1.6, the termination loss is too high when connecting multiple SRs to the secondary windings.

To address these issues, CPES proposed a novel structure, termed a matrix transformer, wherein the transformer is broken down into multiple smaller transformers that are then connected such that the primary windings are in series and the secondary windings are in parallel [16][17]. Most recently, [18] proposed a matrix transformer consisting of four smaller transformers, each with a 4:1 turns ratio, as shown in Fig. 1.7. This way, as the secondary current is distributed equally among the paralleled secondary windings, it correspondingly reduces the net secondary winding loss. In addition, the SR termination loss can be minimized as the SRs don't have to be paralleled

on a single secondary winding, but instead can be placed individually on the paralleled secondary windings, thereby also mitigating the secondary winding leakage inductances.

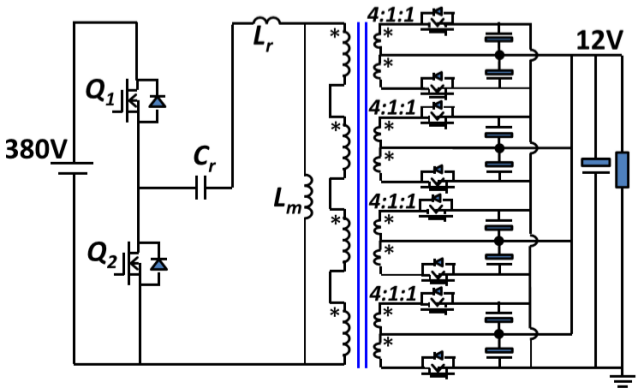
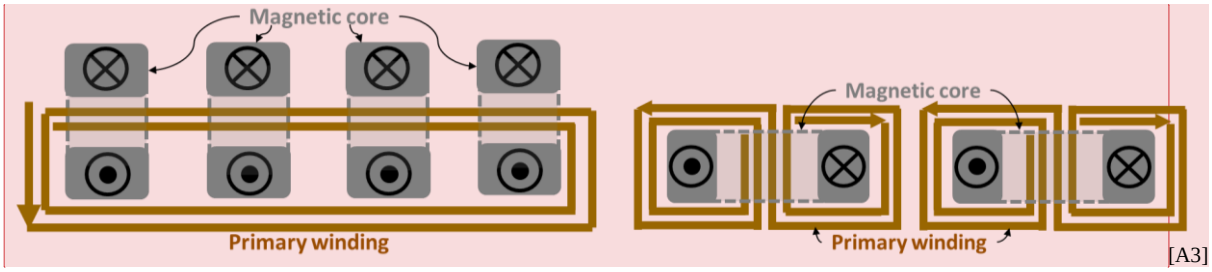
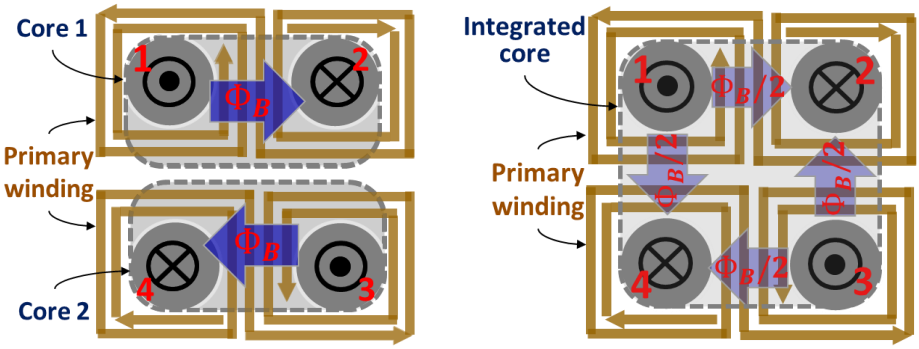


Fig. 1.7. LLC converter with four-leg matrix transformer.



(a) (b)

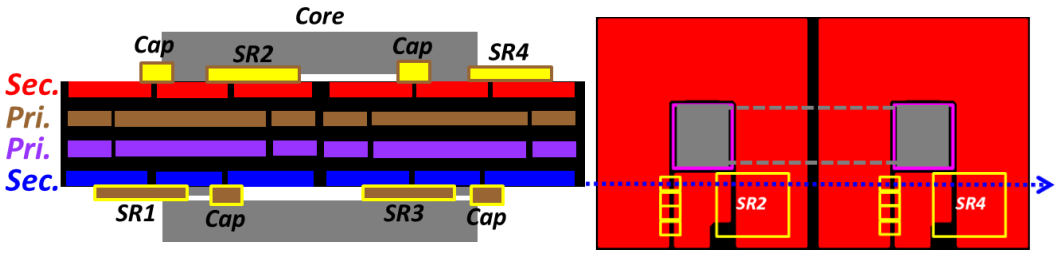


(c) (d)

Fig. 1.8. Integration process for the four-leg matrix transformer with reduced flux density: (a) original matrix transformer, (b) matrix transformer with flux cancelation, (c) before core integration, and (d) after core integration.

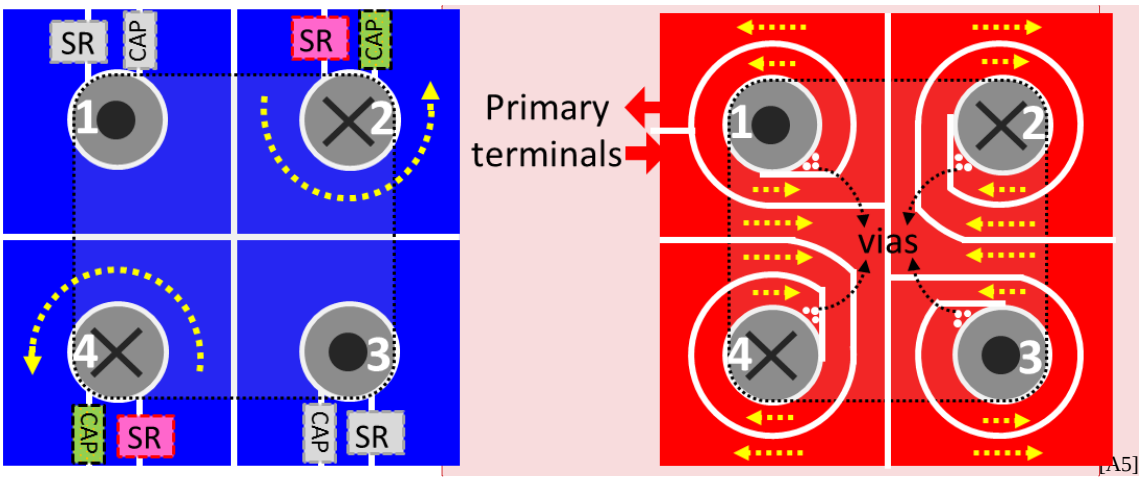
The process of integrating the four elementary transformers into one matrix transformer is shown in Fig. 1.8. The original matrix transformer with four sets of UI[A4] cores has excessive core loss due to the redundant core legs, as shown in Fig. 1.8 (a). However, two UI cores can be combined if the primary turns are wound in opposite directions, and hence the vacant legs can be removed since they have equal and opposite magnetic fluxes; this results in two sets of UI cores, as shown in Fig. 1.8 (b). Furthermore, core 2 can be rotated by $180^{0,}$ as shown in Fig. 1.8 (c), such that upon integration of all four elemental transformers under one core, the magnetic flux in the plate is evenly distributed. This way, only half the flux from each leg flows to the two adjacent legs, resulting in low core loss in the plates.

Using traditional litz-wires for the transformer windings is difficult for manufacturing and mass production, and hence printed circuit board (PCB) -based windings have been used in recent works, due to the ease with which they can be designed and manufactured [16][17][19]. Fig. 1.9 (a) shows the four-layer PCB layer stack for the matrix transformer in [18]. The two primary layers are sandwiched in between the two secondary layers on the top and bottom layers. This way, the SRs and output filter capacitors can be placed directly on the secondary windings to minimize the termination losses and secondary winding leakage inductance, as shown in Fig. 1.9 (b).

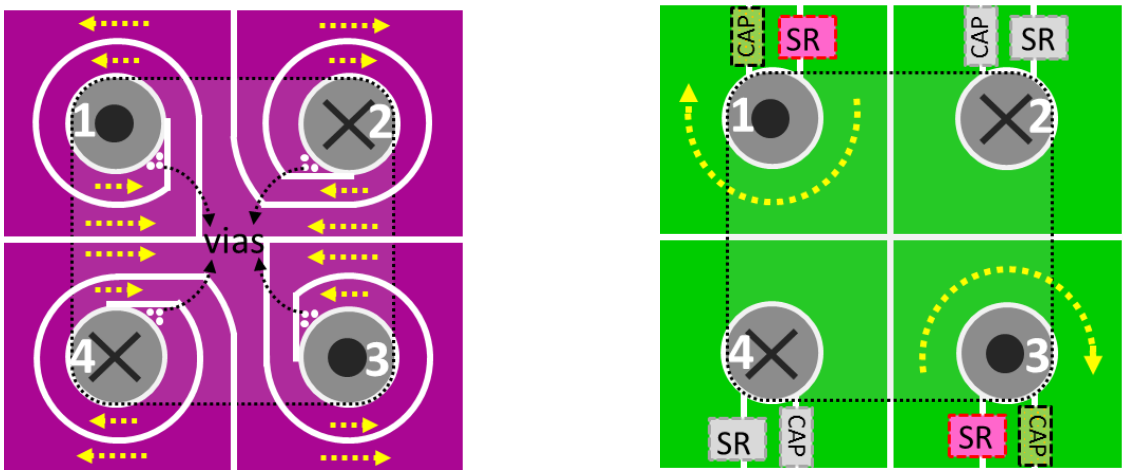


(a) (b)

Fig. 1.9. Four-layer PCB winding transformer stack-up: (a) cross-sectional view, and (b) top view.



(a) (b)



(c) (d)

Fig. 1.10. PCB winding arrangement for matrix transformer: (a) Layer 1: Secondary, (b) Layer 2: Primary, (c) Layer 3: Primary, and (d) Layer 4: Secondary.

Fig. 1.10 shows the PCB winding arrangement for the matrix transformer; the yellow arrows show the current direction in the windings. The 16 primary turns are wound among the four elemental transformers between the two primary layers. Each elemental transformer has two primary turns per layer, with vias being employed to connect the two layers between each elemental transformer. The primary terminals are right next to each other to minimize the leakage

inductance and termination loss. The secondary side employs center-tapped rectification, and hence only one set of SRs are active in each half-cycle of operation. The SRs and output filter capacitors are placed directly on the winding, which allows the secondary current to perfectly interleave with the primary, resulting in minimum leakage inductance and AC termination loss. Moreover, the SRs conducting in one half-cycle are alternatively placed on the two secondary layers to have symmetrical interleaving between the primary and secondary currents.

A hardware prototype for the 800W 380V/12V LLC DC-DC converter running at a fixed frequency of 1 MHz was developed as shown in Fig. 1.11, and the specifications for the proposed converter are shown in Table 1.2.

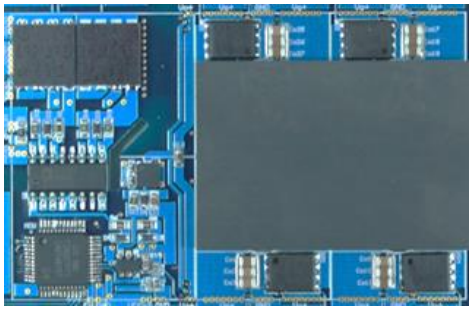


Fig. 1.11. Hardware prototype of the proposed LLC converter.

Table 1.2. Specifications of the proposed LLC converter.

Component	Parameters
Resonant Frequency	1MHz
Dead Time	90ns
Transformer Turns Ratio	16:1
Primary Devices	PGA26E08
Secondary Devices	BSC0500NSI
Primary Driver	Si8273
Secondary Drivers	FAN3122
Resonant Capacitor	71nF
Resonant Inductance	312nH
Magnetizing Inductance	25uH

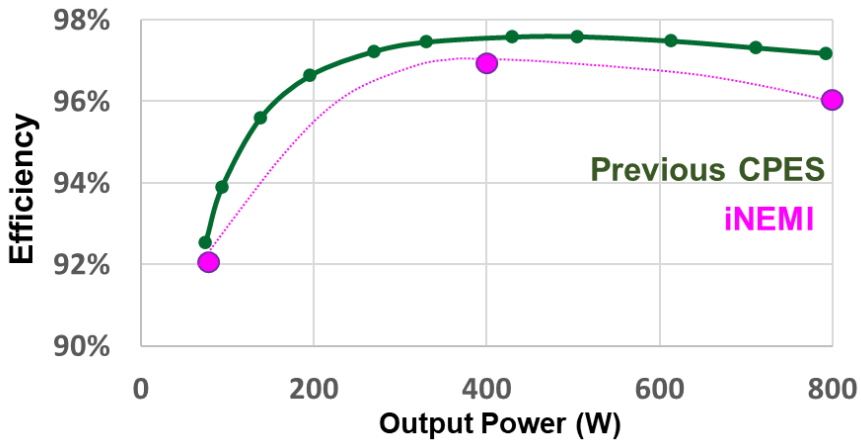


Fig. 1.12. Measured efficiency curve for previous CPES LLC converter.

The power density of the 800W converter is 930 W/in^3, and the measured efficiency curve is shown in Fig. 1.12. It can achieve 92.5% at light load (10% load), 97.6% peak, and 97.2% at full load, all of which satisfies the iNEMI requirements, as shown by the pink curve in Fig. 1.12.

1.3 Motivation and Outline for Thesis

As discussed in Section 1.1, the energy demand of datacenters is increasing exponentially, which has resulted in significant interest to realize the 400V-bus architecture for datacenters. Hence, the 400V/12V DC-DC converter has been the recent research focus of many groups [20][21][22][23][24]; a summary comparison of performance levels including the previous CPES converter [18] are listed in Table 1.3. Some research [20],[21] and [24] has demonstrated different ways the partial-turn transformer concept can be implemented effectively for the 380V/12V LLC converter, resulting in high power densities and efficiencies. One research work [22] uses series-connected low-voltage primary Si MOSFETs to reduce the device losses. Another example [23] is ViCOR's 800W bus converter module that offers high power density.

Table 1.3. Performance summary of other recent 400V/12V unregulated DC-DC converters.

ITEM	[18]	[20]	[21]	[22]	[23]	[24]
Rated Power	800W	1kW	800W	1.8KW	800W	1kW
Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz	1MHz
Peak Efficiency	97.6%	97% *	96.5% *	98.3% *	97.4%	97.3%
Power Density	900W/in^3	640W/in^3**	900W/in^3**	810W/in^3	1177W/in3	-

* Without Driving Loss ** Without Controller

The efficiency values with a * denote that they do not include the device's driving losses. For example, [22] reports 98.3% peak efficiency, which is higher than that of the previous CPES work due to lower device losses. However, it has significantly higher device driving losses (~9W) from switching 16 Si MOSFETs, and this results in an estimated 97% peak efficiency. The power density values with a ** denote that they do not include the controller circuit as part of the power density.

To summarize, new developments in magnetic and converter designs are pushing the efficiencies and power densities higher, which leads to the motivation to attempt to further improve the performance of the CPES 400V/12V LLC converter such that it can compete with state-of-the-art performance levels. This is the primary objective of this thesis. Three major areas of potential performance improvement have been identified – matrix transformer termination design analysis, the shielding technique used to suppress common-mode (CM) noise in matrix transformers and optimizing the switching frequency of the LLC converter to improve efficiency and power density.

In Chapter 1, the current trends in datacenter energy requirements are discussed, and how improvements in datacenter power architecture, achieved by pushing the bus voltage from the traditional 12V up to 400V, can help improve the overall power architecture efficiency. The 400V

bus requires a 400V/12V DC-DC converter with high efficiency and high power density. CPES has developed a 400V/12V LLC converter rated at 800W, which is briefly reviewed. Moreover, the current technology landscape of the 400V/12V DC-DC converters for future datacenters is surveyed, leading to the motivation to further improve the performance of the CPES 400V/12V LLC converter to (a) keep the performance improvement at pace with ever-increasing energy demands, and (b) outperform other recent works.

In Chapter 2, different termination techniques for the high-frequency matrix transformers with center-tapped rectifiers are discussed. The termination design must be carefully considered, especially at high-frequency operations, where the transformer leakage inductances can result in high AC termination losses. In this chapter, the termination design in the previous CPES 400V/12V LLC converter is analyzed. Due to the presence of output filter capacitors on both secondary layers (top and bottom layers), there is a parasitic path between the two filter capacitor sets that has some parasitic loop inductance, which resonates with the capacitors to result in parallel LC resonance peaks. This behavior is analyzed, and design guidelines are provided to move the parallel LC resonant frequency away from the converter resonant frequency in order to minimize this impact, and hence lessen transformer impedance, at the resonant frequency. The complete transformer including the termination is modeled and verified with hardware measurements.

In Chapter 3, the shielding technique in matrix transformers is studied. Due to the large overlapping surface area between the primary and secondary windings in planar transformers, the inter-winding capacitance is high. The high dV/dt in the primary side causes CM noise to flow through the inter-winding capacitance then into the secondary side, resulting in high CM noise at the load. To attenuate this, shield layers are placed between the primary and secondary layers and are connected back to the primary ground, such that the induced CM noise flows back into the

primary side. CPES previously designed a shielding technique with conducting shield layers, which, in addition to suppressing the CM noise, also increases the effective turns number of the transformer, thereby reducing the primary-side loss, and improving efficiency. However, there are inherent current-sharing issues in the converter due to asymmetrical leakage inductances in the two half-cycles of operation, resulting in a reduction in efficiency. This phenomenon is studied in detail, and solutions are proposed; these are verified with hardware testing. In addition, the impact the position of the transformer airgap relative to the PCB windings has on its leakage inductance is also briefly discussed.

In Chapter 4, the switching frequency of the LLC converter is optimized. The LLC converter operates at a fixed switching frequency, which equals the resonant frequency, when it operates as a DC-DC transformer. Most of the losses in the converter are dependent on the switching frequency, and hence its optimization is vital for achieving the greatest performance from the converter. To optimize the switching frequency, the best ferrite material for the transformer core must be selected for each switching frequency. To make this selection, the core loss densities of various materials are measured, and their performance factors are compared to determine the best materials at different frequency ranges. Next, the converter efficiencies and power densities are compared at different switching frequencies, and the optimal switching frequency is selected. Finally, the performance improvement is verified with hardware experiments carried out on the converter operating at the optimal switching frequency.

Chapter 5 presents a summary of the work done in this thesis and explores options for future work.

Chapter 2. Termination Analysis of High-Frequency PCB-Winding Planar Transformers

2.1 Introduction

The benefits of switching to PCB winding-based transformers from the traditional litz wire-based transformers are multifold, and include easier manufacturability, strong repeatability, and a larger surface area resulting in low-profile cores and better thermal capabilities. Moreover, the planar magnetic windings can be pushed to higher frequencies, as compared to the traditional litz-wire windings, hence reducing the magnetic core size [25]. However, in high-current applications, multiple PCB layers must be paralleled in order to achieve low DC resistance. This results in an increase in the number of termination connections to be made.

In high-frequency, high-current planar transformers, in addition to the core loss and winding loss, the total transformer loss also includes termination loss. The termination loss has two main components – (a) loss from the vias, which interconnect the multiple parallel layers, and (b) loss from the winding segments that extend outside the core for termination in the external circuitry, which includes the SRs and the output filter capacitors.

Significant work has been done to study the termination in planar transformers; multiple aspects, such as the optimal number of PCB layers, interleaving and relative positioning of the primary and secondary layers, and optimally connecting the secondary winding terminals to the SRs and output filter capacitors have been studied [25][26][27]. For the four-layer planar transformer employed for 400V/12V LLC converters, the termination for the center-tapped

rectifiers has been studied and optimized in the previous converters developed by CPES, as summarized in Fig. 2.1 and Fig. 2.2 [16][17][18].

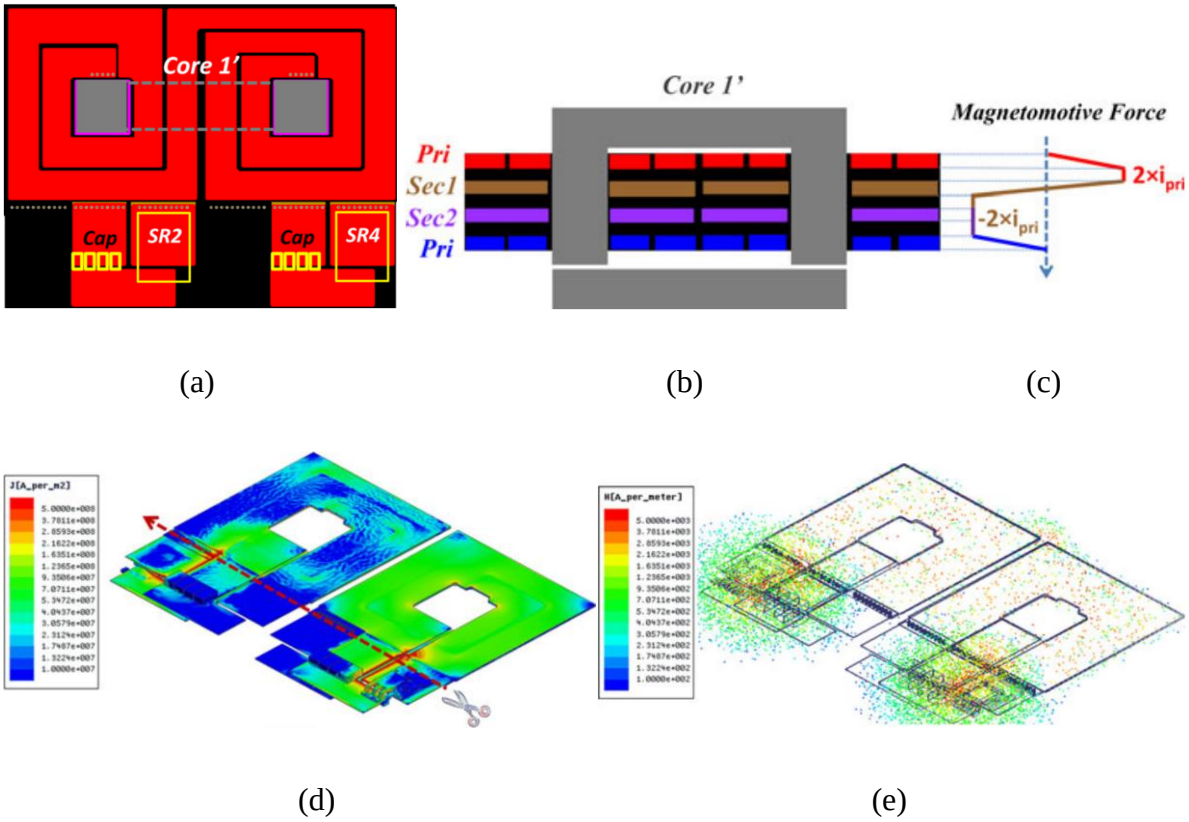


Fig. 2.1. Winding arrangement with good interleaving but high termination loss: (a) top view, (b) cross-section view, (c) MMF distribution, (d) FEA simulation of current density distribution, and (e) magnetic field intensity plot.

Fig 2.1 shows a winding arrangement in which the top and bottom layers contain the primary windings and the middle layers are for the secondary windings. This arrangement has very good interleaving due to the low peak magneto-motive force (MMF) in the transformer, as shown in Fig. 2.1 (c). However, the termination design becomes challenging in this arrangement, as the secondary winding terminals in the middle layers must be connected to the SRs and output filter capacitors on the top and bottom layers using vias, resulting in high via loss. Moreover, the SRs and filter capacitors must be placed outside the transformer area, resulting in poor interleaving in

the non-overlapping area outside the transformer, as seen by the high magnetic field intensity in Fig. 2.1 (d). The 3D finite element analysis (FEA) simulation of the secondary windings with this termination at 1 MHz results in AC resistance $R_{sec} = 6.81\ m\Omega$ and leakage inductance $L_k = 176.4nH$.

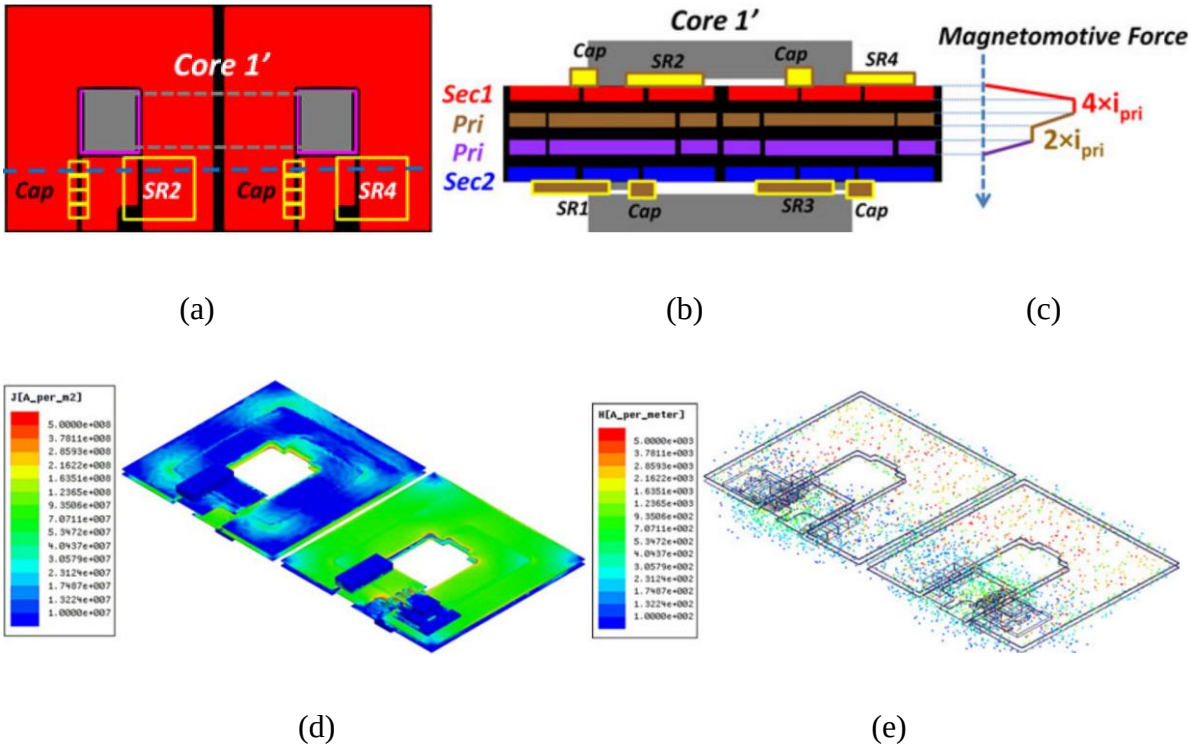
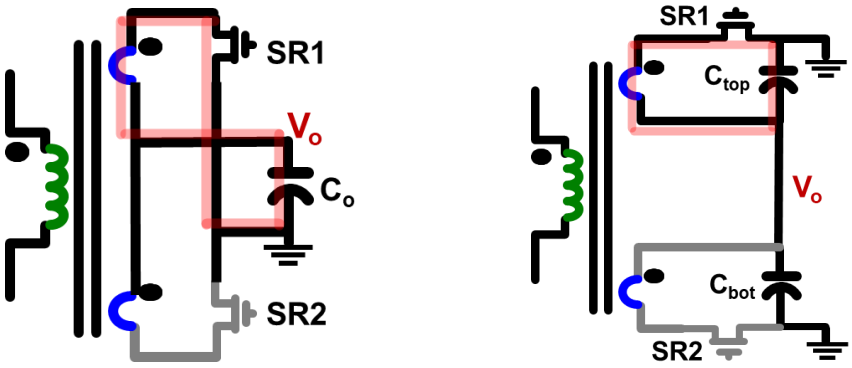


Fig. 2.2. Winding arrangement with worse interleaving but low termination loss: (a) top view, (b) cross-section view, (c) MMF distribution, (d) FEA simulation of current density distribution, and (e) magnetic field intensity plot.

Fig 2.2 shows a winding arrangement in which the top and bottom layers contain the secondary windings and the middle layers are for the primary windings. This arrangement allows the SRs and output filter capacitors to be on the same layers as the secondary windings, which eliminates the requirement of vias for connection. Moreover, the SRs and output capacitors can now be placed directly on the windings themselves, as shown in Fig. 2.2 (a), resulting in much

better overlapping between the primary and secondary current, and hence improving both components of the termination design. The 3D FEA simulation for the secondary windings of this improved termination at 1 MHz results in AC resistance $R_{sec} = 1.37\ m\Omega$ and leakage inductance $L_k = 36.6nH$. These values are almost one-third the values obtained from the previous termination, highlighting the fact that even with worse inherent interleaving, drastic improvements in termination lead to much lower AC resistances and leakage inductances of the transformer.

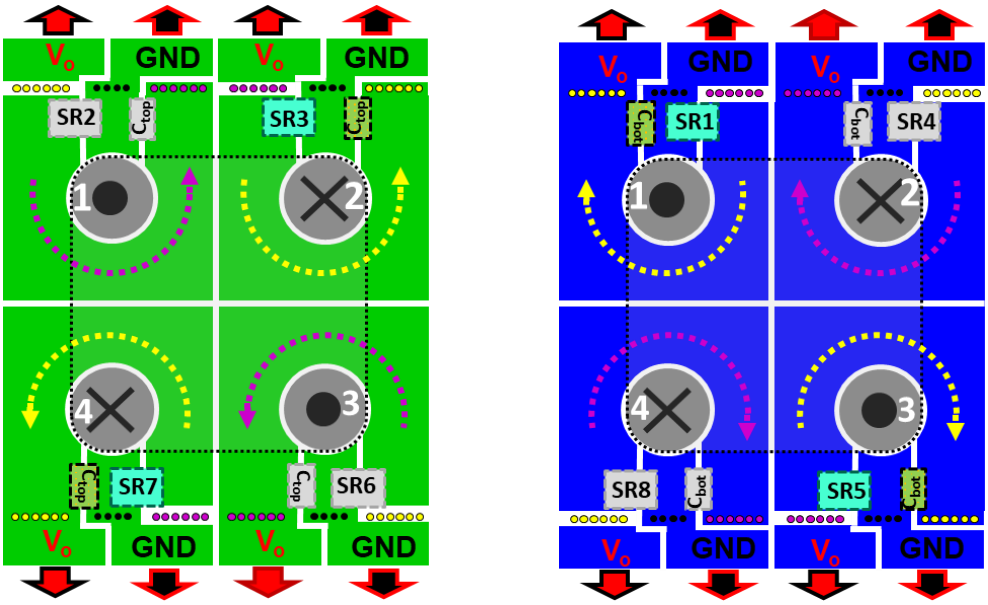
As evident from the previous designs, the center-tapped rectifier circuit is split between the top and bottom secondary layers, such that only one layer is required to conduct in each half-cycle. However, this also means that the output filter capacitors must be split into two and placed on each secondary layer to achieve an optimal termination loop. Hence, the center-tapped rectification schematic can be redrawn with split output filter capacitors, as shown in Fig. 2.3, for one elemental transformer, with the two sets of split output filter capacitors being named C_{top} and C_{bot}. The red loop shows the termination loop in one half-cycle.



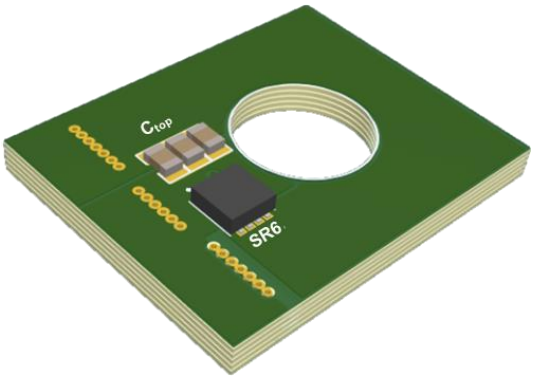
(a) (b)

Fig. 2.3. Modified schematic of center-tapped rectifier with split output filter capacitors: (a) common output filter capacitors, and (b) split output filter capacitors.

Based on this, the secondary-side termination for the four-leg matrix transformer in the previous CPES 400V/12V LLC converter with center-tapped rectifiers was designed as shown in Fig. 2.4 [17].



(a) (b)



(c)

Fig. 2.4. Secondary-side termination in the previous CPES 400V/12V LLC converter: (a) top layer, (b) bottom layer, and (c) 3D view of component and via layout in one elemental transformer.

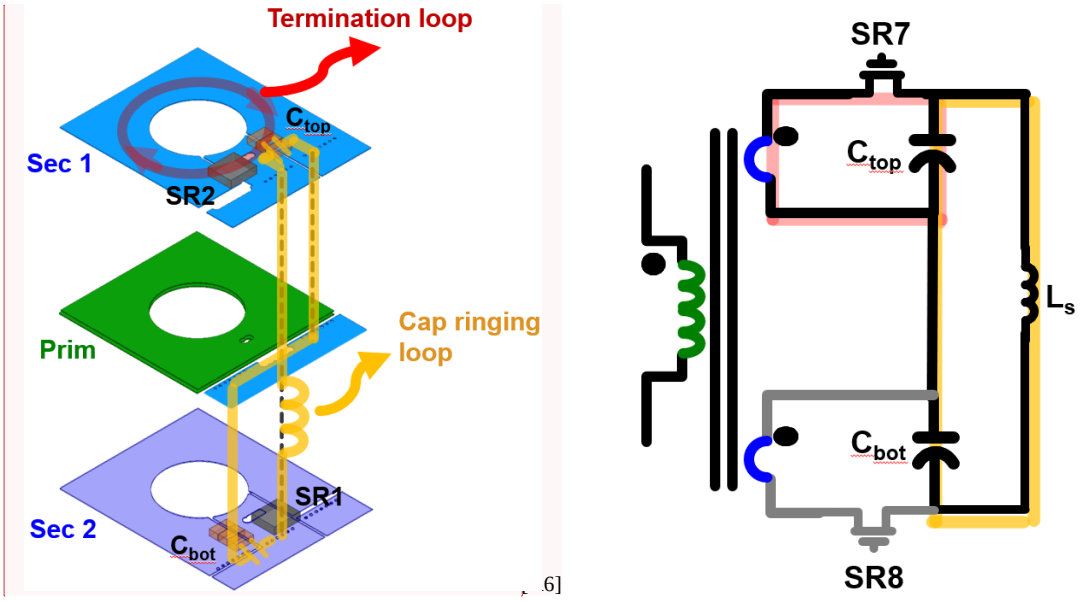
The four elemental transformers are separately connected to the load, as shown by the red and black arrows pointing outward from the transformer terminals. The output filter capacitors on the top secondary layer are labeled C_{top} and those on the bottom secondary layer are labeled C_{bot}. SR1, SR3, SR5, and SR7 conduct in the first half-cycle, and, along with their corresponding filter capacitors, are colored in. SR2, SR4, SR6, and SR8 conduct in the second half-cycle, and, along with their corresponding filter capacitors, are greyed out. Since the output currents from both half-cycles must be merged to be sent to the load, vias are needed outside the transformer to combine the output currents using the middle layers. The current flow arrows and the termination vias used by the secondary current in the first half-cycle are shown in yellow, and those used in the second half-cycle are purple.

Ideally, all AC components of the output current will be filtered out by the output capacitors, resulting in only the DC current merging through the vias and going to the load. However, as will be studied in this chapter, there is an alternative path from C_{top} to C_{bot} that results in circulating current, which has its own parasitic loop inductance and resistance. This inductance is shown to resonate with the capacitors, resulting in parallel resonance at a certain frequency, which if within the vicinity of the switching frequency, can result in increased transformer termination losses, and hence, lower efficiencies. This phenomenon is investigated, and capacitor selection guidelines are proposed for optimal design.

2.2 Parallel Resonance between Split Output Filter Capacitors

The split output capacitors, which are on the top and bottom layers, must be paralleled and connected to the load. However, since the secondary current flows in opposite directions in the two half-cycles, the positions of the SR and the filter capacitors are interchanged on the two

secondary layers. This results in a long path from C_{top} to C_{bot}, as shown in Fig. 2.5 (a), which shows the transformer layers of elemental transformer #4. The red loop indicates the secondary current termination loop, and the yellow loop shows the path from C_{top} to C_{bot} through the middle layers. A simplified equivalent schematic can then be drawn as shown in Fig. 2.5 (b), in which the parasitic loop connects C_{top} and C_{bot} through L_s.

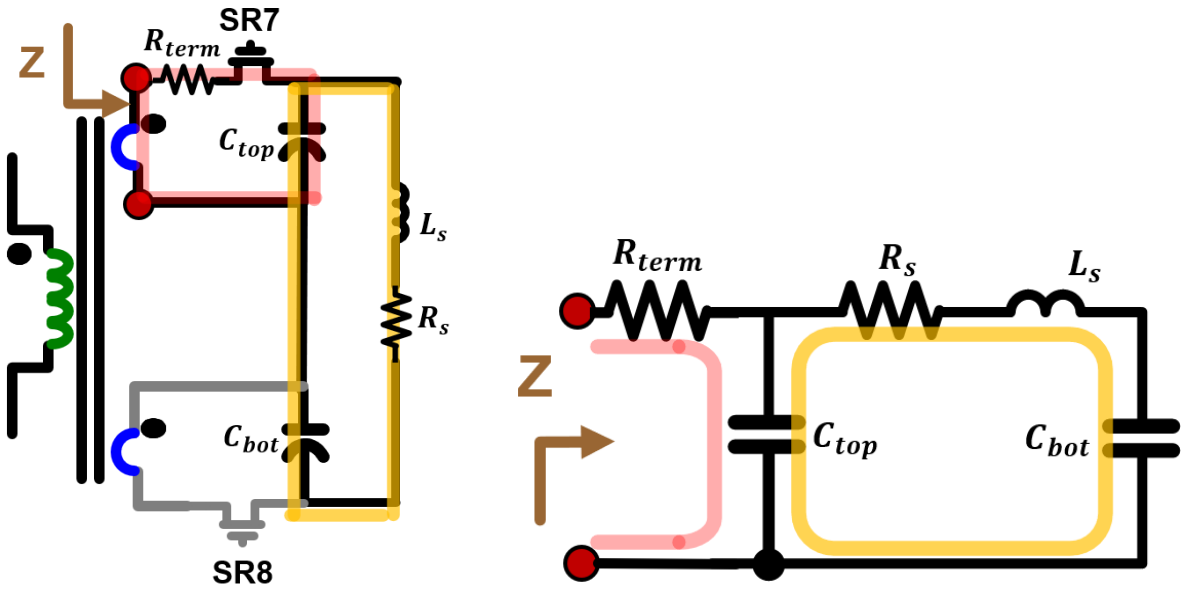


(a) (b)

Fig. 2.5. (a) Parasitic loop connecting C_{top} to C_{bot}, and (b) equivalent schematic with parasitic loop inductance L_s.

The equivalent impedance model of the termination circuit must be studied to understand the behavior of the parasitic loop. Fig. 2.6 (a) shows the modified schematic of the termination including termination resistance R_{term} and parasitic loop resistance R_s. Fig 2.6 (b) shows the equivalent impedance network of the secondary-side termination during the first half-cycle across the two red dots in Fig. 2.6 (a) and includes the capacitor ringing loop.

It can be observed that there is a parallel resonant loop in the circuit, represented by the yellow loop, which can result in high impedance if the loop's resonant frequency is around the converter's switching frequency. This loop needs to be carefully analyzed and optimized.



(a) (b)

Fig. 2.6. (a) Secondary-side termination schematic with parallel ringing loop, and (b) equivalent impedance model.

It can be realistically and reasonably assumed that $C_{top} = C_{bot}$. Therefore, the net impedance Z of the termination network can be expressed as:

$$Z = R_{term} + \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_2}}, \tag{2.1}$$

where Z_1 and Z_2 are the impedances of the two parallel branches, given by:

$$Z_1 = \frac{1}{sC_{top}} \; and \; Z_2 = sL_s + \frac{1}{sC_{top}} + R_s. \tag{2.2}$$

where $s = j\omega$, and ω is the angular frequency, given by $\omega = 2\pi f$. Therefore, (2.2) can be substituted into (2.1) to result in:

$$Z = R_{term} + \frac{1}{sC_{top} + \frac{sC_{top}}{1 + s^2 L_s C_{top} + sR_s C_{top}}}, \tag{2.3}$$

which can be further expanded to get:

$$Z = R_{term} + \frac{1 + s^2 L_s C_{top} + sR_s C_{top}}{s^3 L_s C_{top}^2 + +s^2 R_s C_{top}^2 + 2sC_{top}}. \tag{2.4}$$

This results in a third-order transfer function due to the presence of the three energy-storage elements C_{top}, C_{bot} and L_s.

To study the impact of this termination impedance on the transformer loss, the equivalent resistance, or the real part, of the impedance network must be evaluated. To achieve this, $s = j\omega$ is substituted into (2.4), and the complex conjugate of the denominator is multiplied and divided to result in:

$$Z = R_{term} + \frac{(1 - \omega^2 L_s C_{top} + j\omega R_s C_{top})[-\omega^2 R_s C_{top}^2 - j\left(2\omega C_{top} - \omega^3 L_s C_{top}^2\right)]}{\left(\omega^2 R_s C_{top}^2\right)^2 + \left(2\omega C_{top} - \omega^3 L_s C_{top}^2\right)^2}. \tag{2.5}$$

The total impedance can now be separated into the real and imaginary parts as:

$$Z = R_e + jX_e, \tag{2.6}$$

where [PPR7] R_e is the equivalent resistance of the impedance network, X_e is the equivalent reactance of the impedance network. Upon further simplifying (2.5), the following expressions for R_e and X_e are obtained:

$$R_e = R_{term} + \frac{R_s}{C_{top}^2 L_s^2 \omega^4 + C_{top}^2 R_s^2 \omega^2 - 4C_{top} L_s \omega^2 + 4}, and \tag{2.7}$$

$$X_e = \frac{L_s \omega - \frac{C_{top}(L_s^2 \omega^4 + R_s^2 \omega^2)}{2\omega}}{C_{top}^2 L_s^2 \omega^4 + C_{top}^2 R_s^2 \omega^2 - 4C_{top} L_s \omega^2 + 4} - \frac{1}{2C_{top}\omega}, \tag{2.8}$$

Clearly, $|Z|, R_e$ and X_e are a function of the frequency and can be plotted as shown in Fig. 2.7.

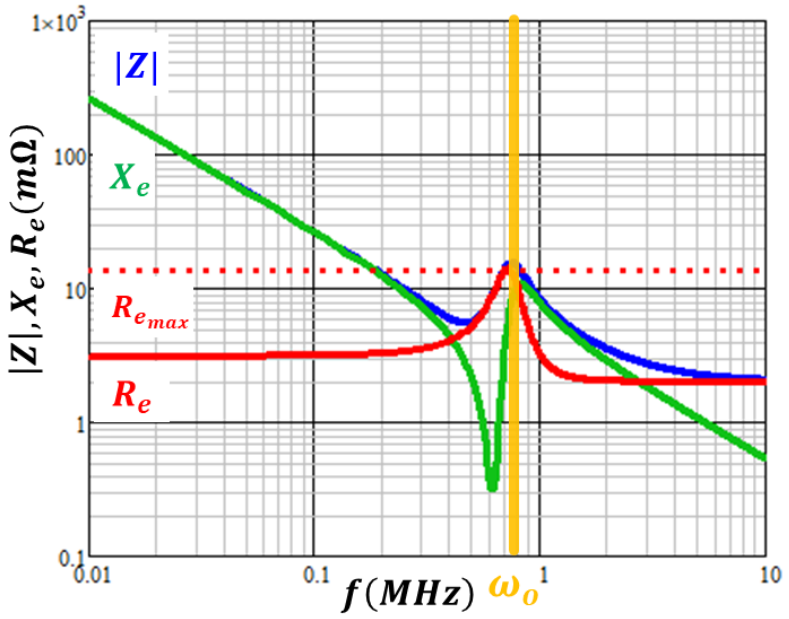


Fig. 2.7. Magnitude, real and imaginary parts of Z against frequency.

The above graph was plotted with the following parameters:

$C_{top} = C_{bot} = 3 \times 10\ \mu F, L_s = 3.1\ nH, R_s = 4.4\ m\Omega, R_{term} = 2\ m\Omega.$

The blue, green, and red curves show $|Z|, X_e$ and R_e respectively. It can be observed that at low frequencies, the impedance network is predominantly capacitive, with infinitely high reactance, and hence impedance at $\omega = 0$. However, at a particular frequency ω_0 where there is parallel resonance between C_{top}, C_{bot} and L_s, there is a large circulating energy between the energy storage elements, resulting in high impedance in the network at the parallel resonant

frequency. However, the high circulating current also passes through R_s, which is in series with L_s. This results in an increase in the termination resistance at parallel resonant frequency too. Hence, R_e dominates the network impedance around the parallel resonant frequency, and since it represents the real loss in the network, its analysis is essential to study the gather information about the transformer's termination loss.

The parallel resonant frequency can be calculated simply by setting $X_e = 0$ for the parallel resonant circuit, resulting in the following expression for the parallel resonant frequency, ω_0:

$$\omega_0 = \frac{1}{\sqrt{0.5 C_{top} L_s}}. \tag{2.9}$$

(2.4) can be rearranged to give:

$$C_{top} L_s = \frac{2}{\omega_0^2}. \tag{2.10}$$

(2.5) can be substituted in (2.2) to give:

$$R_e = \frac{R_s}{4\left(\frac{\omega}{\omega_0}\right)^4 - 8\left(\frac{\omega}{\omega_0}\right)^2 + \omega^2 C_{top}^2 R_s^2 + 4} + R_{term}. \tag{2.11}$$

At low frequencies, $\omega \ll \omega_0$, and hence R_e can be approximated as R_{lowf} given by:

$$R_{lowf} \approx \frac{R_s}{4} + R_{term}. \tag{2.12}$$

At high frequencies, $\omega \gg \omega_0$, and hence R_e can be approximated as R_{highf} given by:

$$R_{highf} \approx R_{term}. \tag{2.13}$$

At the resonant frequency, $\omega = \omega_0$, and hence the peak resistance R_{emax}, as shown by the dotted red line in Fig. 2.7, can be expressed as:

$$R_{emax} = \frac{L_s}{2C_{top}R_s} + R_{term}. \tag{2.14}$$

Given that the operating frequencies of resonant converters are easily pushed to over 500 kHz, the presence of the parallel loop resonant peak around the typical frequency range of operation is a reason to pay attention to this behavior. For example, the equivalent termination resistance is more than four times higher at 700 kHz than at 1 MHz, which (a) is counterintuitive as the termination resistance increases with switching frequency, and (b) can result in much steeper conduction losses and lower efficiencies than expected at 700 kHz. Therefore, this phenomenon needs to be studied in detail so that its impact on the converter efficiency can be minimized.

2.3 Impact of Filter Capacitance on the Transformer's Termination Loss

The model assumes the capacitor to be purely reactive. However, real capacitors have parasitic equivalent series resistances (ESRs), which could contribute to significant losses in high-output-current applications and must also be considered in the model. Fig. 2.8 shows the modified equivalent impedance model including the capacitor ESRs.

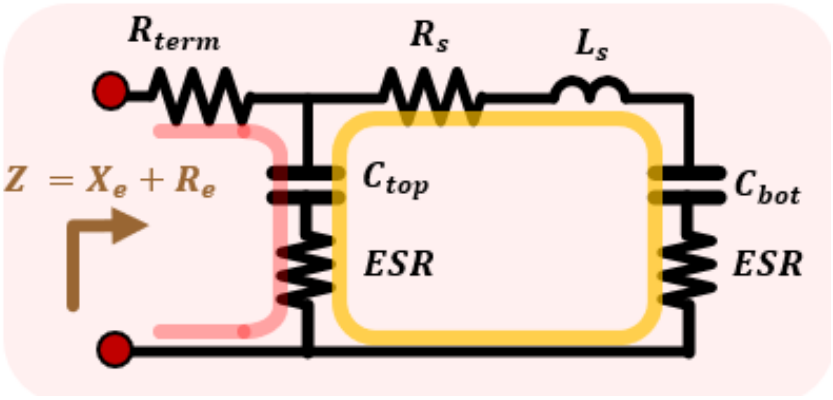


Fig. 2.8. Modified equivalent circuit model including capacitor ESR.

Adding the resistances will not impact the resonant frequency value. However, it will affect the equivalent resistance R_e as illustrated by the comparison curves in Fig. 2.9. Each 10 µF capacitor has an ESR of 2 mΩ, and hence paralleling three of them results in a net ESR of 0.67 mΩ, which is considered in this example.

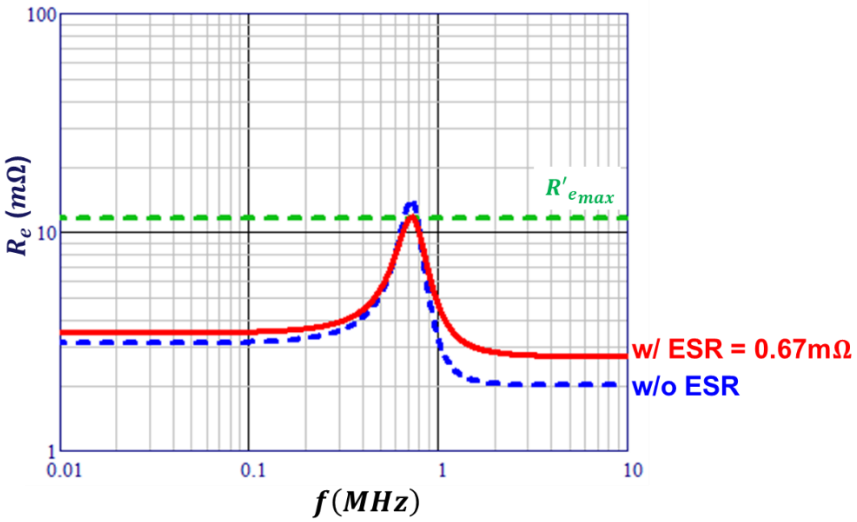


Fig. 2.9. Impact of capacitor ESR on equivalent termination resistance.

Upon considering the capacitor's ESR, the R_{lowf}, R_{emax} and R_{highf} have straightforward modifications, resulting in R'_{lowf}, R'_{emax} and R'_{highf} as shown:

$$R'_{lowf} \approx \frac{R_s + ESR}{4} + R_{term}. \tag{2.15}$$

$$R'_{highf} \approx R_{term} + ESR, and \tag{2.16}$$

$$R'_{emax} = \frac{L_s}{2C_{top}(R_s + ESR)} + R_{term}. \tag{2.17}$$

It can be observed from Fig. 2.9 that for a realistic ESR value, its impact on the equivalent termination resistance is negligible up to the resonant frequency and has a slight impact thereafter.

Therefore, for studies focusing on frequencies at or below the resonant frequency, and where the $ESR \ll R_s$, the ESR can be neglected in order to simplify the model and calculations.

The capacitance value selection is typically governed by the output voltage overshoot/undershoot during load transients, and the peak-to-peak output voltage requirements at steady state. However, from equation (2.4), the parallel resonant frequency for the parasitic termination loop depends on the output filter capacitance C_{top} and the loop inductance L_s. For instance, if a capacitance value is selected that satisfies both the transient and steady-state requirements, but results in the parallel resonant frequency being in the vicinity of the switching frequency, this will result in high termination resistance, resulting in high conduction losses, and hence low efficiency.

Fig. 2.10 shows the equivalent termination resistance R_e as a function of frequency for three capacitance values. The transformer has sufficient winding width to accommodate three 0805-sized capacitors each for C_{top} and C_{bot}, and this parameter is fixed for this study.

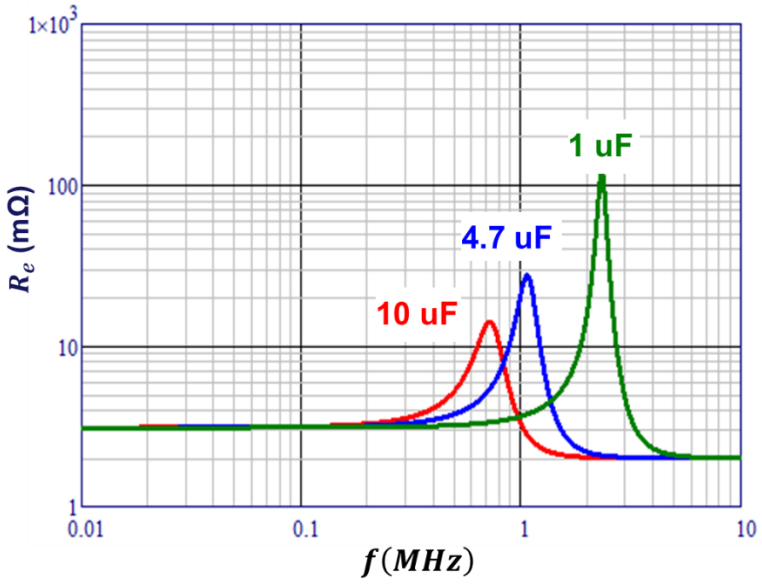


Fig. 2.10. R_e vs. frequency for different capacitors.

From Fig. 2.10, it can be observed that by increasing the capacitance, the parallel resonant frequency decreases. This result indicates that, although a higher capacitance is better for the load transient and steady-state output voltage peak-to-peak requirements, it may result in high termination resistance as the parallel resonant frequency moves much closer to the switching frequency.

2.4 Experimental Verification of Parallel Resonance

To experimentally verify the parallel resonance phenomenon in the terminations of center-tapped rectifiers in planar transformers, as discussed in Section 2.3, the transformer impedance must be measured and verified with the proposed model. However, it is practically impossible to directly measure the secondary-winding impedance. Moreover, its magnitude is usually very low ($\leq 1m\Omega$) and it is difficult to measure accurately and consistently for meaningful results. Therefore, the transformer's impedance is measured from the primary side for a two-fold benefit – (a) the impedance can easily be measured across the two distinct primary winding terminals, and (b) it is easier to capture any small differences in secondary impedance, because the high turns ratio will reflect the small resistances of the secondary to the primary with a large gain.

However, to validate the measurement, the entire transformer must be modeled, which would include the magnetizing inductance and the winding leakage inductances. Fig. 2.11 shows the complete schematic for one elemental transformer, and Fig. 2.12 shows the equivalent circuit model reflected to the primary side, where n is the turns ratio.

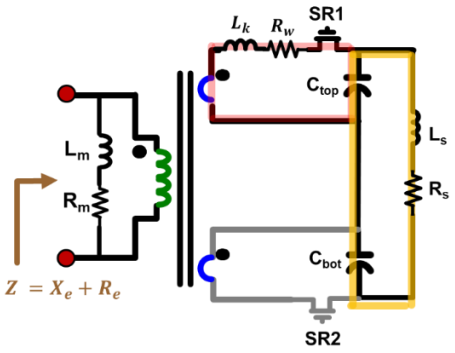


Fig. 2.11. Schematic of one elemental transformer with CT rectifiers and loop parasitics.

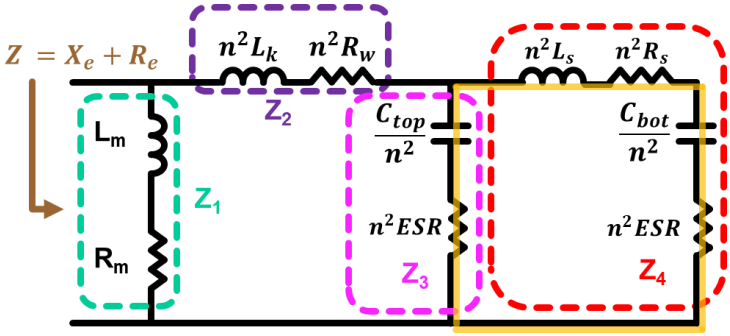


Fig. 2.12. Equivalent circuit model of transformer reflected to primary side.

The equivalent impedance of the transformer, Z is given by:

$$Z = Z_1||[Z_2 + (Z_3||Z_4)], \tag{2.18}$$

where Z_1, Z_2, Z_3 and Z_4 are the branch impedances shown in Fig. 2.12 and are defined as:

$$Z_1 = R_m + j\omega\, L_m, \tag{2.19}$$

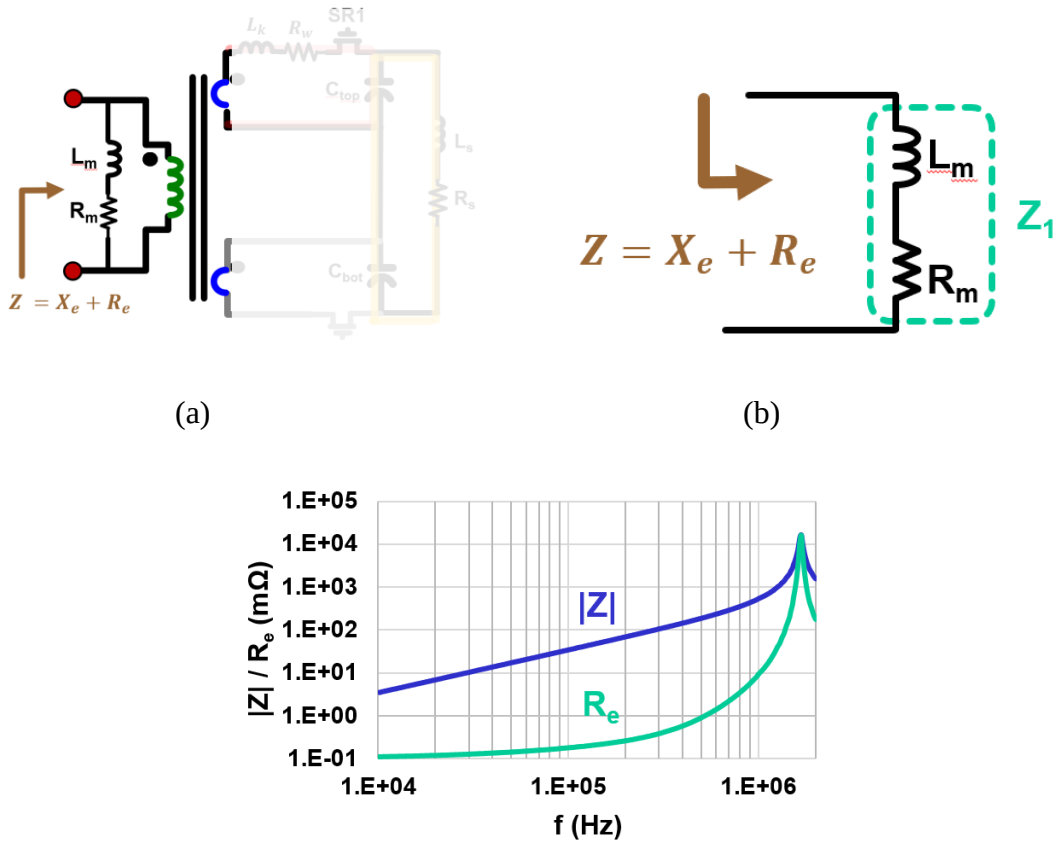
$$Z_2 = n^2(R_w + j\omega\, L_w), \tag{2.20}$$

$$Z_3 = n^2\left(ESR + \frac{1}{j\omega\, C_{top}}\right), and \tag{2.21}$$

$$Z_4 = n^2\left(ESR + R_s + j\omega L_s + \frac{1}{j\omega\, C_{bot}}\right). \tag{2.22}$$

Modeling the transformer also introduces magnetizing and leakage inductance branches into the model, and these must be accounted for to fully validate the measurement. A list of different tests to accurately measure or model the different elements in Fig. 2.12 is provided below. The transformer impedance is measured using a Keysight 4990A impedance analyzer with the Keysight 42941A high-bandwidth in-circuit impedance probe.

3.1 [A8][A9]L_m and R_m: The magnetizing impedance branch Z_1 can be measured by setting the secondary side to be an open circuit (OC), as shown in Fig. 2.13 (a), resulting in the equivalent circuit model shown in Fig. 2.13 (b).



(a) (b)

(c)

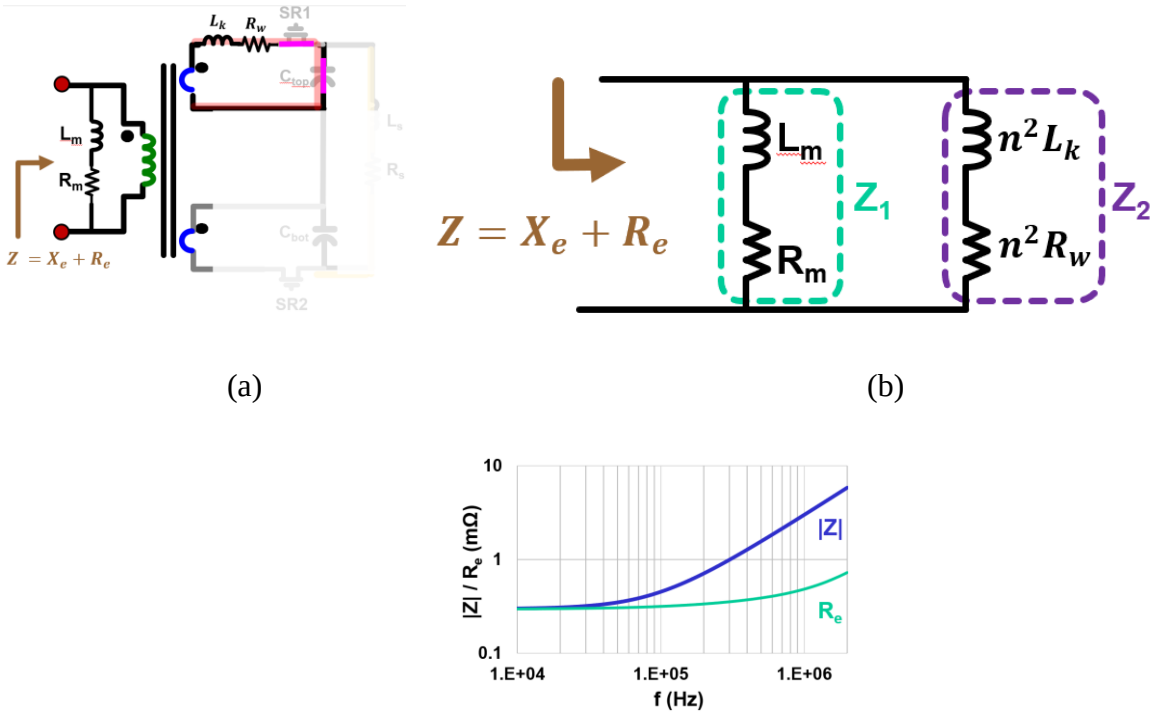
Fig. 2.13. Magnetizing inductance measurement: (a) open-circuit secondary, (b) equivalent circuit model, and (c) impedance and resistance measurement results.

The equivalent circuit model is modified as shown in Fig. 2.13 (b), resulting in the Z being measured as:

$$Z = Z_1. \tag{2.23}$$

From the measurement curves in Fig. 2.13 (c), the impedance curve is purely inductive up to 1 MHz, and the magnetizing inductance can be calculated from the slope. The magnetizing resistance is a representation of the core loss and is obtained directly from the measurement (green curve in Fig. 2.13 (c)).

3.2 [A10]L_k and R_w: The leakage impedance branch Z_2 can be measured by setting one half of the secondary side to be a short circuit (SC) as shown in Fig. 2.14 (a), resulting in the equivalent circuit model shown in Fig. 2.14 (b).



(a) (b)

(c)

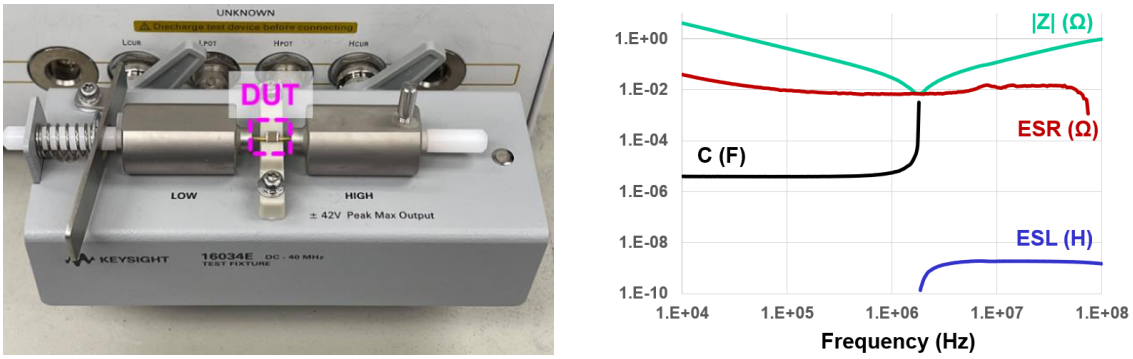
Fig. 2.14. Leakage inductance measurement: (a) short-circuit secondary, (b) equivalent circuit model, and (c) impedance and resistance measurement results.

The equivalent circuit model is modified as shown in Fig. 2.14 (b), resulting in the Z being measured as:

$$Z = Z_1 || Z_2 \approx Z_2 \; as \; Z_1 \gg Z_2. \tag{2.24}$$

From the measurement curves in Fig. 2.13 (c), the leakage inductance can be calculated from the slope of the impedance curve. The magnetizing resistance is a representation of the winding loss and is obtained directly from the measurement (green curve in Fig. 2.14(c)).

3.3 Capacitance[A11] measurement: The capacitance and the ESR of the ceramic capacitors are measured using the 16034E test fixture for surface-mounted devices (SMDs) attached to the Keysight 4990A, as shown in Fig. 2.15 (a). The impedance measurement results for one sample, a 25V 4.7µF X8L 0805, is shown in Fig. 2.15 (b).



(a) (b)

Fig. 2.15. (a) 16034E probe with device under test (DUT), and (b) capacitor parameter measurement.

Three capacitors with low ESRs were tested for this study, and their results are summarized in Table 2.1.

Table 2.1. Summary of selected capacitors.

Rated Capacitance (µF)	Package	Voltage Rating (V)	Measured Capacitance (µF)	ESR (mΩ)	Temperature Coefficient
10.0	0805	25	8.6	2.0	X7S
4.7	0805	25	4.1	6.5	X8L
1.0	0805	100	0.95	4.7	X7R

3.4 [A12]L_s and R_s: It is impractical to accurately take a physical measurement of the leakage inductance and resistance of the termination due to their small magnitudes. Therefore, FEA Q3D simulations are performed to simulate the termination-loop inductance L_s and resistance R_s. The simulated AC L_s and R_s values at different frequencies are shown in Fig. 2.16.

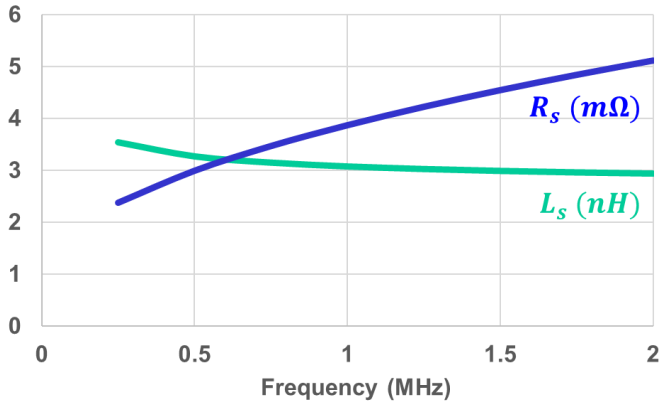


Fig. 2.16. Simulated AC L_s and R_s as a function of frequency.

The AC L_k and R_k vary with frequency, and since the exact parallel resonant frequency is not known beforehand, the exact values for the AC L_k and R_k cannot be selected. Therefore, an average over a realistic frequency range is taken, which in this case is selected as 0.5 MHz – 1.5 MHz, and results in the following values:

$$L_{s,avg} = 3.1\,nH, R_{s,avg} = 4.4\,m\Omega. \tag{2.25}$$

Once all the parameters are accounted for, the hardware measurement can be successfully validated by the transformer model. Instead of the impedance, the transformer resistance is studied because it provides a direct relationship with the transformer loss, which ultimately determines the converter's efficiency.

The transformer resistance was measured with the three capacitors listed in Table 2.1 mounted as the output filter capacitors. Fig. 2.17 shows the measured transformer resistances with the three capacitors as solid lines, and the modeled curves as the dashed lines.

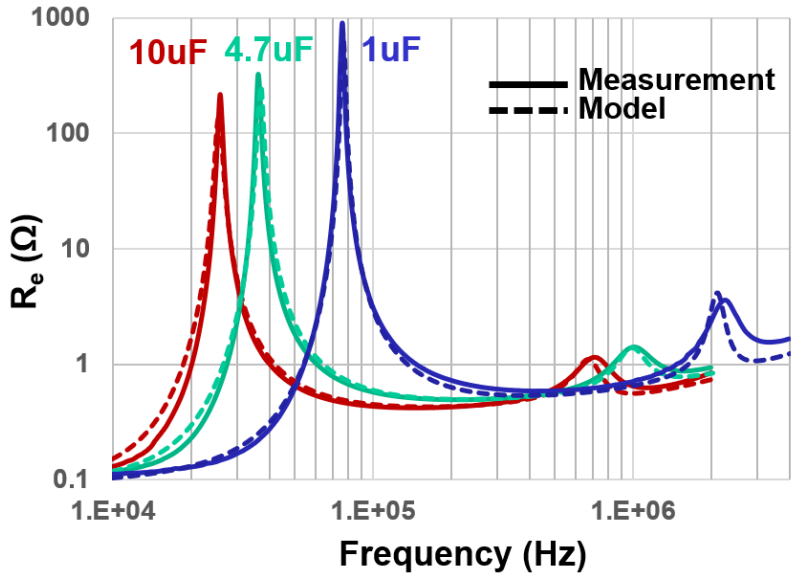


Fig. 2.17. Measured and modeled equivalent transformer resistance versus frequency.

Several conclusions can be drawn from the curves:

- The model agrees well with the measurements within reasonable margin of measurement error.
- The resistance curves can be seen to have two peaks: one at a low frequency corresponding to the parallel resonance involving the magnetizing inductance branch, and the other at a higher frequency corresponding to that involving the parasitic-loop inductance branch.

- As the capacitance increases, the parallel resonant frequency and the peak resistance at the parallel resonant frequency decrease.
- The parallel resonant frequency of the parasitic loop should be kept far away from the converter's switching frequency to minimize the transformer resistance, and hence transformer loss increase. For example, when operating at 1 MHz, the measured transformer resistances for the 10μF, 4.7μF and 1μF capacitors are 642 mΩ, 1.41 Ω and 714 mΩ, respectively. This shows that at 1 MHz, simply by changing the output capacitance from 10 μF to 4.7 μF, the transformer resistance, and hence the winding loss, will increase by almost 100%, which is significant.

  These results provide a general design guideline for output filter capacitor selection for planar transformers with center-tapped rectifiers, so as to minimize the impact of the parasitic parallel resonant peak on the transformer's resistance at the switching frequency.

2.5 Conclusions

In this chapter, the termination design in planar matrix transformers with center-tapped rectifiers have been studied. Advances in termination design have been reviewed, including minimization of the termination loss by moving the secondary layers to the top and bottom PCB layers such that the SRs and output filter capacitors can be placed directly on them.

However, this solution involves splitting the output filter capacitance between the top and bottom layers, which results in a long parasitic path between them with significant parasitic inductance. This inductance resonates with the parallel branch containing the filter capacitors, resulting in resistance peaking at the parallel resonant frequency.

The parallel resonant frequency is dependent on the parasitic inductance and the filter capacitance. In this study, the impact of filter capacitance on the parallel resonant frequency is studied. With higher capacitance, the parallel resonant frequency reduces.

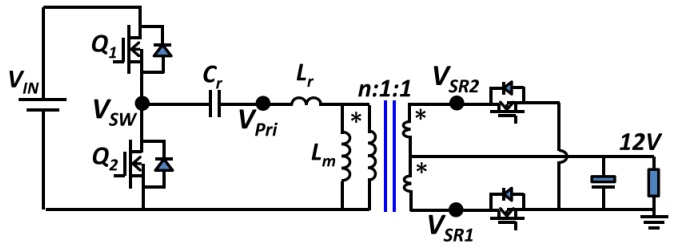
This concept is experimentally verified by measuring the transformer impedance and resistance with different output capacitors. However, the entire transformer is modeled since the impedance must be measured from the primary side. The model verifies the measurement within experimental tolerance, and verifies the hypothesis that the transformer resistance, and hence transformer conduction losses, are highest if the switching frequency is at the parallel resonant frequency; hence the latter must be moved far away from the former for optimal efficiency. For example, at 1MHz operation, either the 10µF or the 1µF capacitor may be used, but the parallel resonant peak with the 4.7µF capacitors is right around 1 MHz, resulting in almost double the transformer resistance.

The future scope for this work includes investigating the termination parasitic loop in detail and attempting to minimize the loop inductance in order to push the parallel resonant frequency further up the frequency, thereby reducing the impact of the capacitance selection on the converter’s performance.

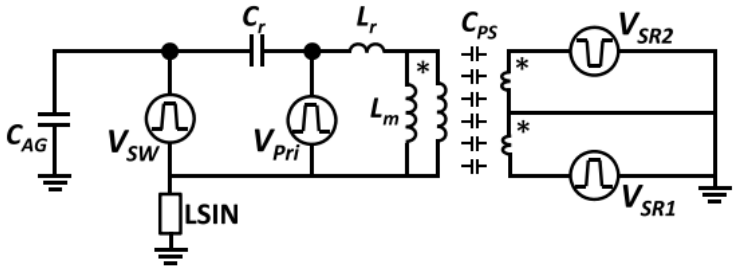
Chapter 3. Improved Symmetrical Shielding Technique for Planar Matrix Transformers

3.1 Introduction

The planar matrix transformer with PCB windings for resonant converters has been demonstrated to exhibit high efficiencies and high power densities, while realizing high reproducibility and the ability to be mass-produced. However, the large cross-sectional area of the transformer results in significant overlapping and limited distance between the primary and secondary windings, resulting in large inter-winding parasitic capacitances between the primary and secondary sides, as shown in Fig. 3.1[28].



(a)



(b)

Fig. 3.1. (a) Schematic of LLC converter with switching nodes, and (b) CM noise sources and coupling paths.

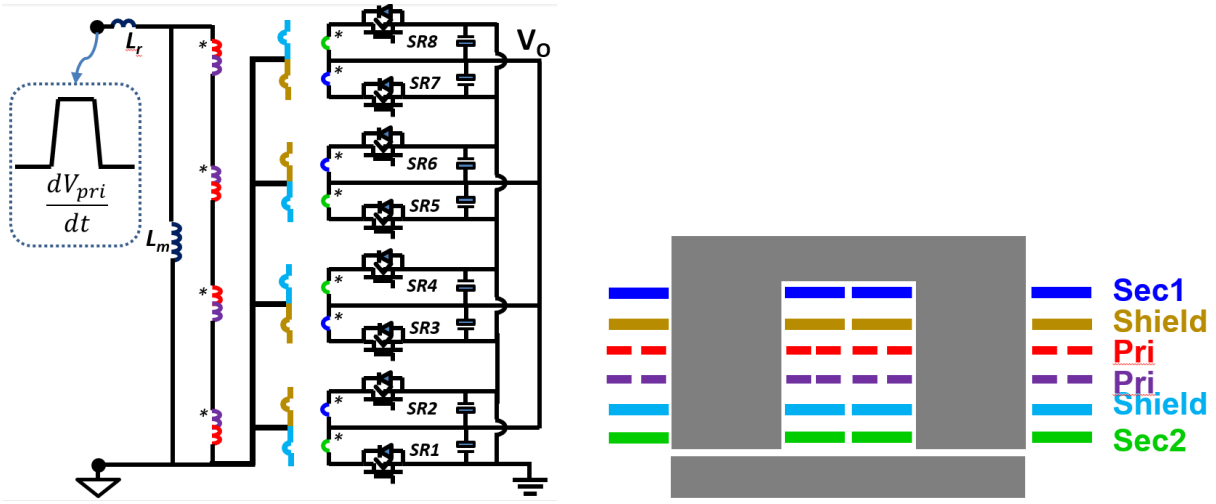
There are four voltage pulsation nodes in the converter with high dv/dt – the half-bridge switching node V_{SW}, the voltage applied to the transformer primary winding V_{pri} and the drain-source voltages of the two SRs, V_{SR1} and V_{SR2}, as shown in Fig. 3.1 (a). Fig. 3.1 (b) shows the simplified CM noise coupling path with the lumped switching voltages. V_{SR1} and V_{SR2} are equal in magnitude and opposite in phase, and hence cancel out each other's CM noise. Another path for the CM noise coupling is from V_{SW} to the primary ground through another parasitic capacitance C_{AG}. However, C_{AG} is generally much lower in magnitude than C_{PS} and hence V_{pri} dominates the CM noise going through the transformer, since it has a path through the large inter-winding capacitors.

The inter-winding current can be expressed as:

$$i = C_{PS}\frac{dV_{Pri}}{dt}. \tag{3.1}$$

To mitigate the CM noise through C_{PS}, either the dV_{Pri}/dt can be reduced, or the propagation path capacitance C_{PS} can be minimized or eliminated. To achieve this, the shielding technique is commonly employed [29][30]. The idea is to introduce additional PCB layers to the transformer between the primary and secondary layers, which can conduct the CM noise current back to the primary side.

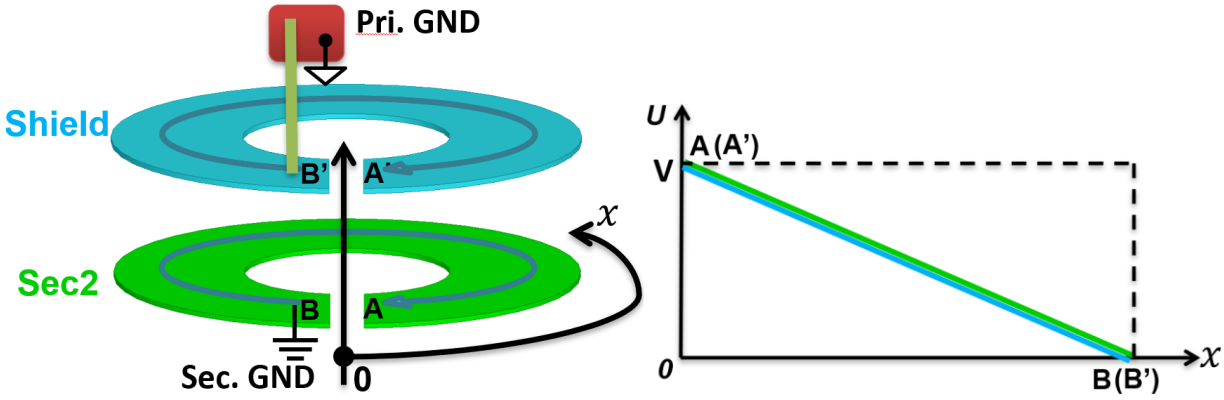
Fig. 3.2 shows the schematic and the modified PCB layer stack-up of the previously four-layer PCB planar matrix transformer with shielding. One shield layer is added between each set of primary and secondary layers, resulting in a six-layer PCB.



(a) (b)

Fig. 3.2. (a) LLC converter schematic, and (b) six-layer PCB stack-up.

The shield layers are placed between the primary and secondary layers and are connected to the primary ground such that the induced CM noise from the primary is blocked by the shield and conducted back into the primary ground, thereby isolating the secondary side. However, the induced voltage in the shield windings act as another voltage pulse source, and hence can further conduct current to the secondary side if not carefully designed.



(a) (b)

Fig. 3.3. Equipotential shield windings: (a) shield and secondary windings, and (b) potential mapping across the windings.

The shield winding must be designed identical to the secondary winding, such that there is no potential difference between the two, and hence no current flow. Fig. 3.3 illustrates this concept, as the one-turn shield layer is identical to the one-turn secondary layer. The winding can be expanded along the x-axis, along which the voltage potential can be mapped. Terminal B of the secondary winding is connected to the secondary ground. Hence, the potential from A to B reduces from an arbitrary V to 0. To make the shield winding identical, the B' terminal of the shield is connected to the primary ground, since the induced CM noise current must be sent back to the primary side. Due to the identical structures of the two windings, the potential at terminal A' is also V. Since the voltage potential at each point on the two layers is identical, there is no CM noise current going from the shield to the secondary. Moreover, the two windings remain at equipotential even if the shield winding is rotated about its center by an arbitrary angle [29].

However, there are now two additional layers that conduct current in the planar transformer, leading to additional losses, and hence lower efficiency. Since the induced current is low in magnitude, typically low-weight copper is used to design the shield layers to minimize the induced eddy currents that increase with copper weight. However, CPES recently proposed a modified shielding technique that utilizes part of the shield windings as part of the primary windings to improve the overall converter efficiency [31].

Fig. 3.4 shows the proposed shielding technique as part of the primary. Half the shield windings are connected in parallel, as they have the same voltage potential at the terminals. Next, the primary windings' terminal connected to the primary ground is disconnected and is instead connected to one end of the paralleled shield windings.

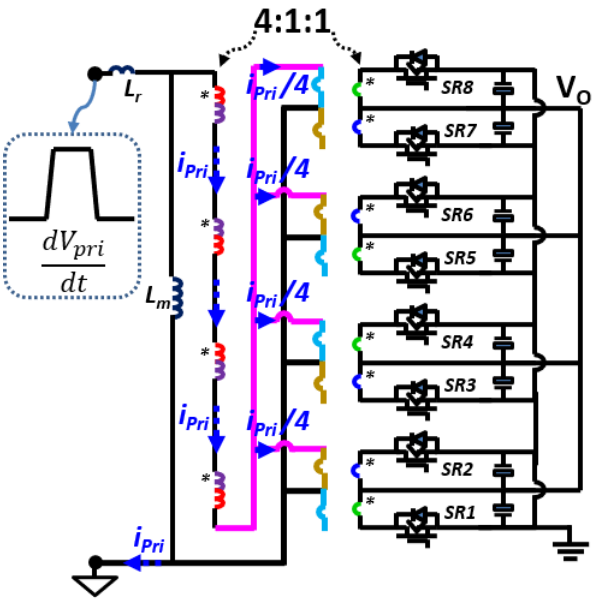


Fig. 3.4. Modified shielding technique with shielding as part of the primary.

It can be observed that, in addition to the 16 primary turns, four shield windings also carry one-fourth of the primary current, which is equivalent to an additional primary turn. This results in a net turns ratio of 17:1, which results in a lower primary current – and hence lower primary device conduction loss – by around 10%. Therefore, the increase in transformer loss due to the addition of the shield layers can be offset by the reduction in primary device conduction loss, resulting in a negligible reduction, if not an increase, in converter efficiency.

The winding structure for the proposed shielding is shown in Fig. 3.5. The primary current exits the primary layers and enters the Layer 2 shield, upon which it splits into the four matrix transformers and conducts on windings alternating between the two shield layers for better interleaving and current sharing. Finally, the primary current merges in the Layer 5 shield and drains into the primary ground.

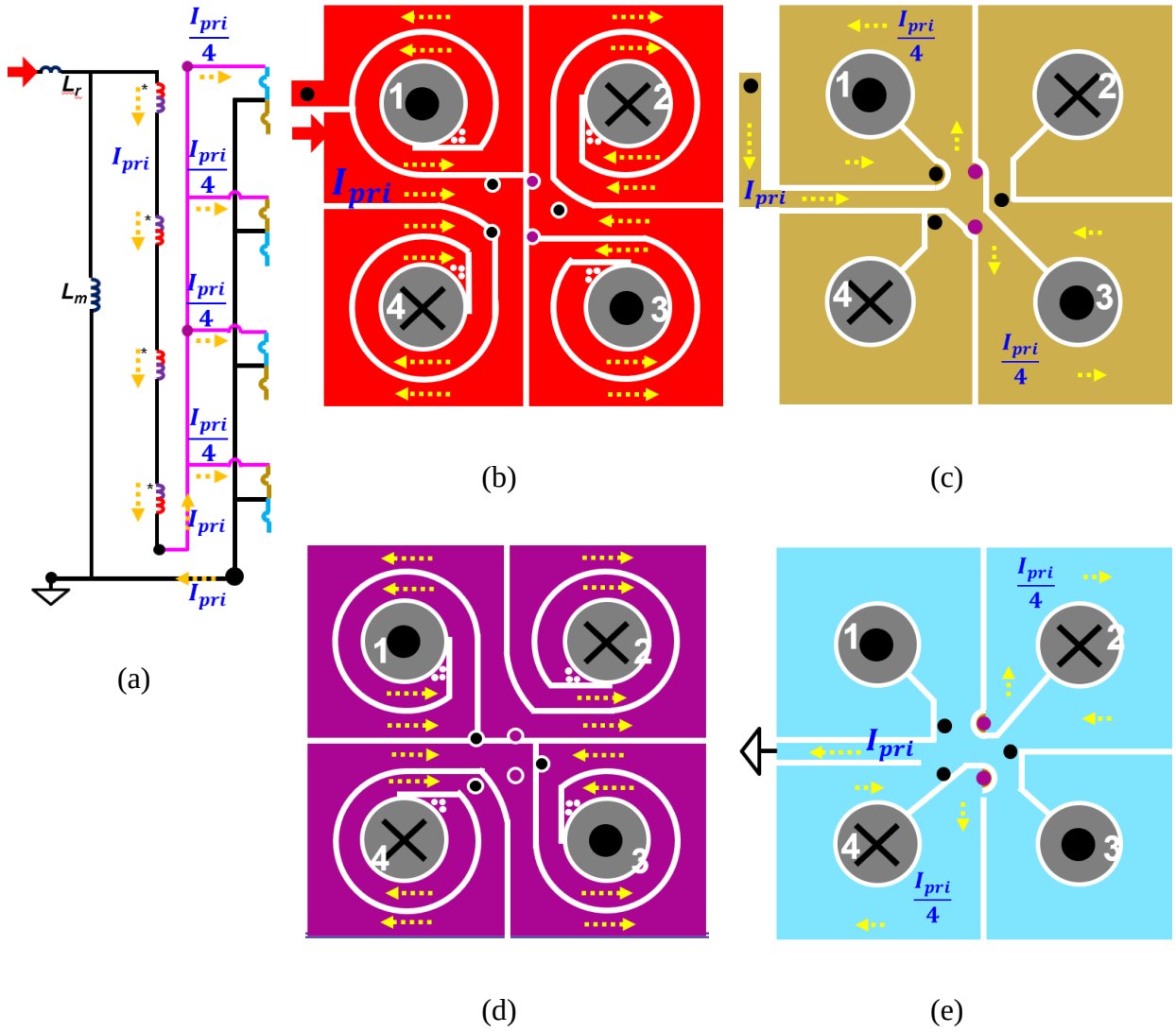
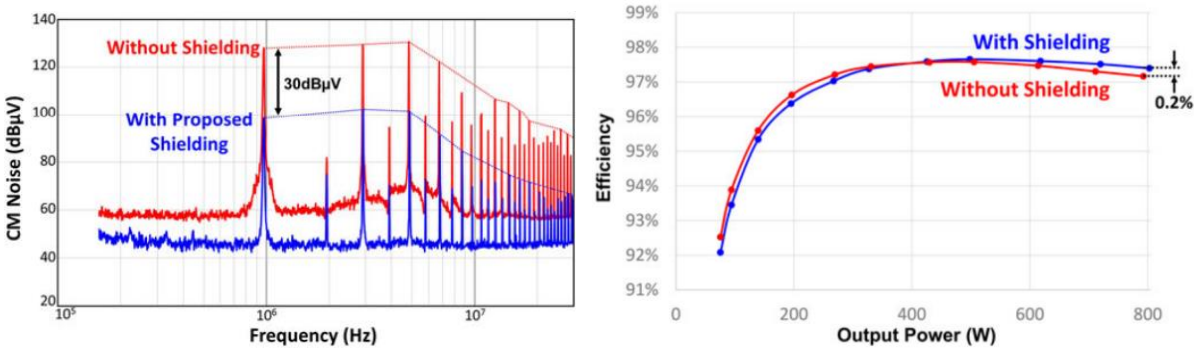


Fig. 3.5. PCB winding arrangement for proposed shielding: (a) transformer schematic with proposed shielding, (b) Layer 3: primary, (c) Layer 2: shielding, (d) Layer 4: primary, and (e) Layer 5: shielding.

This technique was incorporated into the existing 800W 400V/12V LLC converter running at 1 MHz. The hardware prototype is shown in Fig. 3.6. The measured CM noise and the converter's efficiency compared with that of the converter without shielding is shown in Fig. 3.7 (a) and Fig. 3.7 (b), respectively.

Fig. 3.6. Hardware prototype of 400V/12V LLC with proposed shielding.



(a) (b)

Fig. 3.7. Hardware testing results of 400V/12V LLC with proposed shielding: (a) CM noise comparison, and (b) converter efficiency comparison.

The CM noise was reduced significantly – by up to 30 dBµV – with the proposed shielding. Moreover, instead of sacrificing efficiency, it improved the peak efficiency from 97.6% to 97.7% and the full-load efficiency from 97.2% to 97.4% due to the lower primary device conduction losses because of the higher turns number.

While this work has substantial significance, a few aspects of the modified shield structure were not studied. This chapter will investigate the impact the modified shielding has on other aspects of the converter performance, such as current sharing and leakage-inductance symmetry, and propose solutions to further improve the performance of the converter.

3.2 Current-Sharing Study in Matrix Transformers

Due to the presence of multiple output sets in parallel in the matrix transformer, it is crucial to maintain good current sharing among them, failing which can result in lower efficiencies, especially at heavier loads. Therefore, improving current sharing between the parallel output sets is essential to maximizing converter efficiency. In addition to ensuring equivalent paths (connecting wires) from the output of the transformer to the load for all output sets, the internal transformer structure should also be investigated for any potential impedance imbalances, which could lead to current-sharing issues.

One way to study current sharing in the matrix transformer is to study the thermal performance of the different elemental transformers, as an output carrying higher current would be hotter. However, this would be a suitable method only in ideal conditions, such as with no external cooling and a perfectly symmetrical thermal camera or thermocouple positioning. Moreover, each elemental transformer in the converter has different components in its vicinity, which means the heat dissipated from neighboring components could affect the temperatures of the elemental transformers. This requires a comprehensive study of the thermal resistance network for each elemental transformer and calibration of their temperatures, which is beyond the scope of this work.

A more accurate method of studying the current sharing is to directly measure the secondary current flowing out of each elemental transformer, but this is not a practical approach. Alternatively, the drain-source voltages (V_{DS}) of the SRs can be measured to get an accurate representation of the current flowing through them. Fig. 3.8 shows waveforms of interest on the secondary side at the resonant frequency during one-half of a switching period.

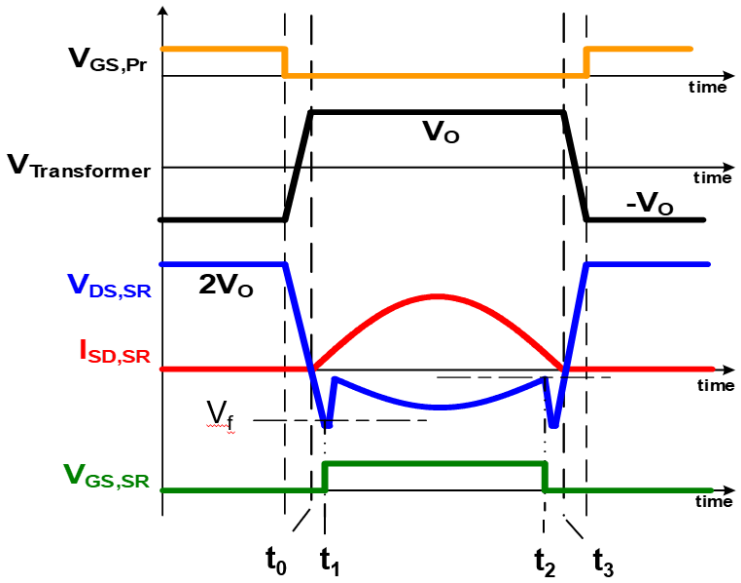


Fig. 3.8. Waveforms of interest on the secondary side during one-half of a cycle of operation.

Fig. 3.8 plots the primary gate-source voltage (V_{GS}), the transformer secondary-side voltage (V_{trans}), the SR drain-source voltage ($V_{DS,SR}$), the SR source-drain current ($I_{SD,SR}$), and the SR gate-source voltage ($V_{GS,SR}$) from top to bottom. The state of the converter at different times after the primary switch is turned off are explained in the following.

t_0: The V_{DS} of the SR reaches 0 and it starts conducting through its body diode to reduce the V_{DS} to the negative of the body diode's forward voltage ($-V_f$).

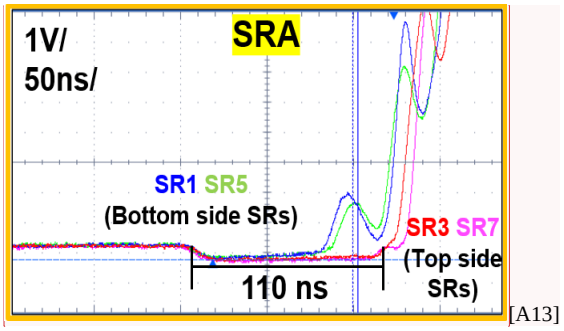
t_1: The SR channel is turned on, and $V_{DS,SR} = -I_{SD,SR} \cdot R_{DS,on,SR}$.

t_2: The SR channel is turned off just before the current's zero-crossing. The remaining current conducts through the body diode, again reducing the V_{DS} of the SR to $-V_f$.

t_3: The SR current goes to 0 and the body diode of the SR stops conducting. The C_{oss} of the SR starts charging.

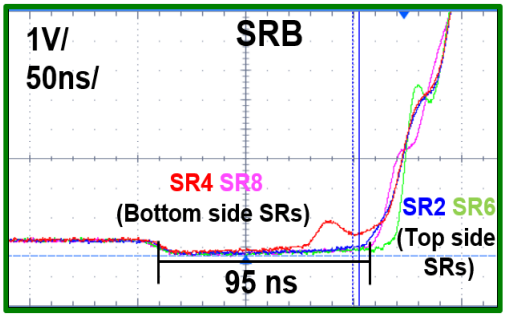
By sufficiently delaying the SRs' turn-off instants, their drain-source voltages can be measured, and the period between t_2 and t_3 can be analyzed to obtain the relative quantity of current flowing through each elemental transformer.

Fig, 3.9 (a) and Fig. 3.9 (b) show the measured drain-source voltages of the SRs during the turn-off instances of the two half-cycles of operation at full loads. Fig. 3.9 (c) shows the positions of the SRs in the two secondary layers. On the top secondary layer, SR3 and SR7 operate in the first half-cycle SRA, whereas SR2 and SR6 operate in the second half-cycle SRB. On the bottom secondary layer, SR1 and SR5 operate in the first half-cycle SRA, whereas SR4 and SR8 operate in the second half-cycle SRB.

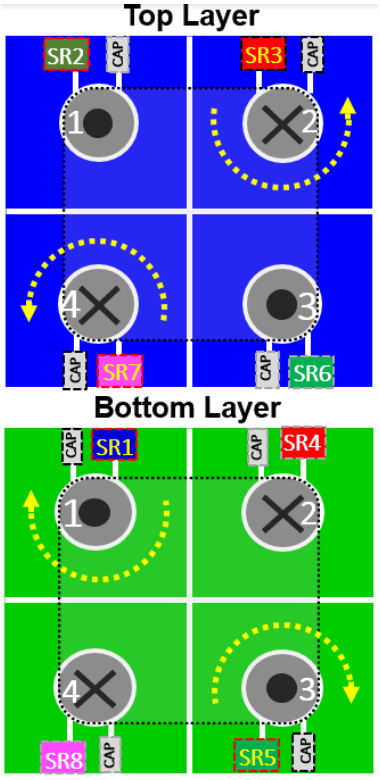


[A13]

(a)



(b)



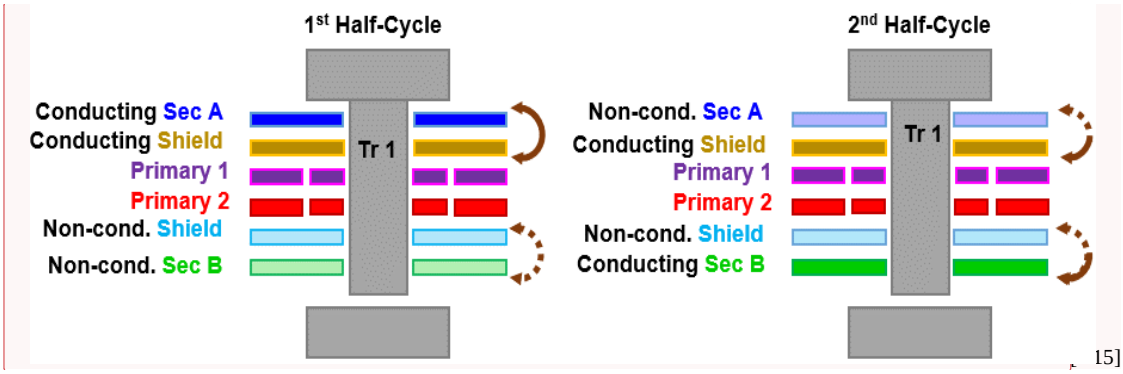
(c)

Fig. 3.9. V_{DS} waveforms of SRs during the turn-off instant: (a) first half-cycle, (b) second half-cycle, and (c) SR positions on the transformer.

Two observations can be made from Fig. 3.9 – (a) the body diode conduction periods in the two half-cycles are asymmetrical, with ~110 ns and ~95 ns for the first and second half-cycle, respectively, for the top-side SRs, and (b) the body diodes of the SRs in the bottom layer (closer to the air gap) stop conducting before those in the top layer (away from the air gap). These issues are critical and are studied in the subsequent sections.

3.3 Improved Current Sharing with Symmetrical Shielding

The explanation for the asymmetrical body-diode conduction periods in the two half-cycles can be traced to the shielding design. From Fig. 3.5 (c), Fig. 3.5 (e) and Fig. 3.9 (c), it can be observed that only one shielding layer in each leg conducts during both half-cycles[A14]. However, the conducting SR, and hence the conducting secondary layer, alternates between the top and bottom layers during one switching cycle. This leads to different proximities of the conducting shield layer to the conducting secondary layer, as shown in Fig. 3.10 (a).



(a) (b)

Fig. 3.10. Conducting layer proximities with the original shielding technique: (a) first half-cycle, and (b) second half-cycle.

The arrows indicate the proximities between the shield and secondary layers. The dotted lines represent the non-conducting layers, and the solid lines represent the conducting layers. To verify

this, 3D FEA simulations were performed, and the leakage inductances of the conducting secondary winding in the two half-cycles are potted in Fig. 3.11.

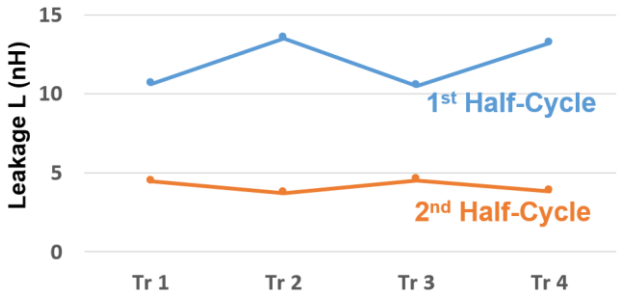
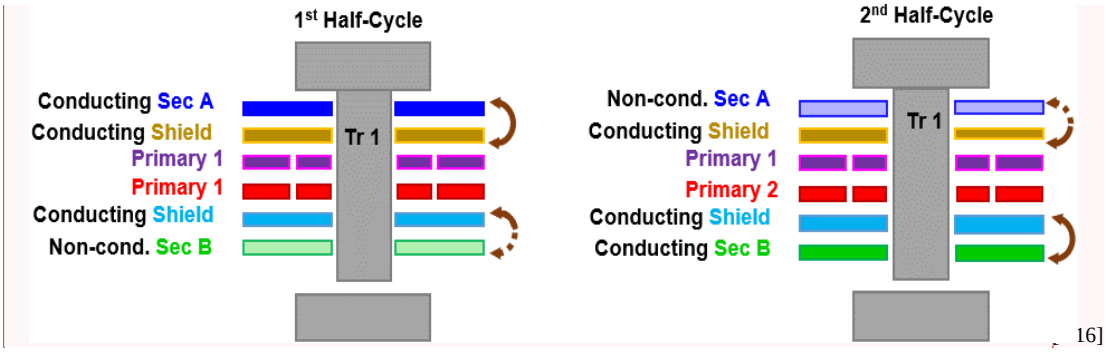


Fig. 3.11. 3D FEA simulated leakage inductances of secondary windings with original shielding.

It can be clearly observed that the leakage inductances are asymmetrical in the two half-cycles. This leads to different resonant periods in the two half-cycles, resulting in different secondary currents, which was reflected by the different body-diode conduction periods in the two half-cycles shown in Fig. 3.9.

The intuitive solution for this issue is to parallel the two shield windings in each elemental transformer, such that the proximities between the conducting shield layer and the conducting secondary layer are the same in both half-cycles, as shown in Fig. 3.12.



(a) (b)

Fig. 3.12. Conducting layer proximities with the modified shielding technique: (a) first half-cycle, and (b) second half-cycle.

It can be observed that when both shield windings conduct, the proximities are symmetrical in the two half-cycles. This is verified by the 3D FEA simulations performed on the modified transformer to calculate the leakage inductances of the conducting secondary windings in the two half-cycles, as shown in Fig. 3.13.

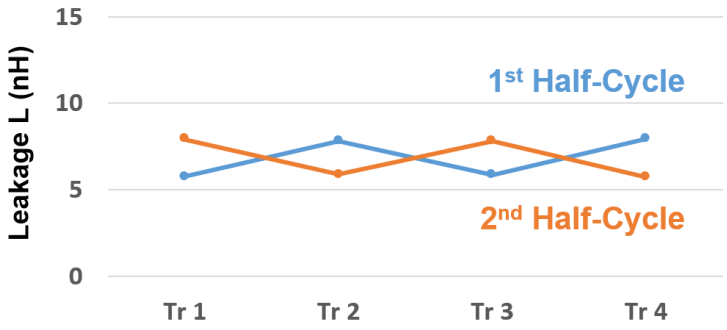


Fig. 3.13. 3D FEA simulated leakage inductances of secondary windings with modified shielding.

Fig. 3.14 shows the modified shield-winding PCB design with all the shield windings paralleled. The primary current exits the primary windings through the black spot and enters the Layer 2 shield winding, after which it symmetrically splits into all eight shield windings (four on Layer 2 and four on Layer 5 through the blue vias). Finally, the split currents converge back through the black vias in Layer 5 and drain into the primary ground.

However, when the shield windings of this improved design are simulated on FEA 3D, the current densities are much higher than the original shield windings, as shown in the comparison in Fig. 3.15. Moreover, the current directions in the paralleled shield windings are anti-parallel, indicating circulating current in the shield windings. This results in a 190% increase in the shield winding loss (1.9 W versus 0.65 W with the original shielding).

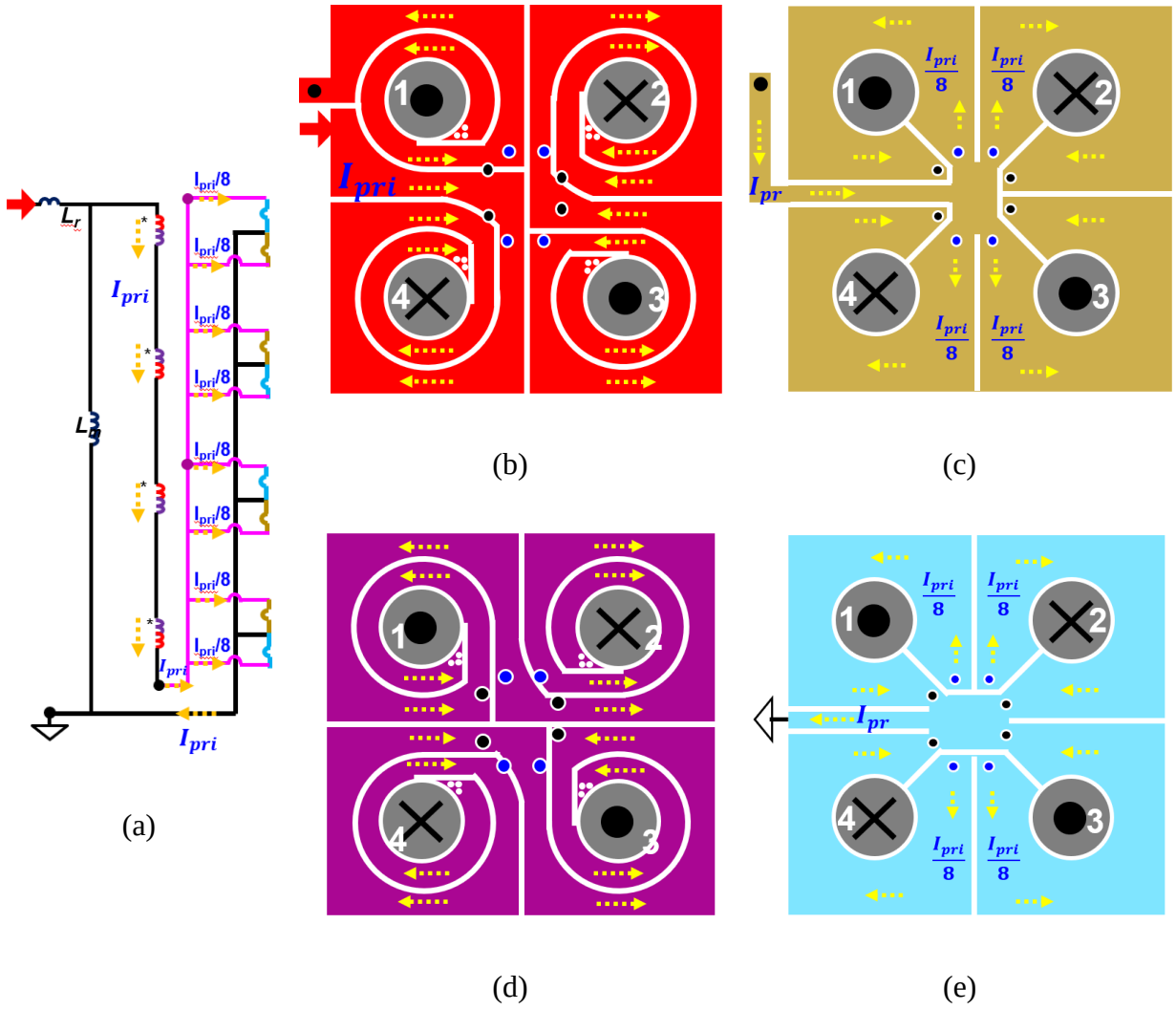


Fig. 3.14. PCB winding arrangement for improved shielding: (a) transformer schematic with improved shielding, (b) Layer 2: shielding, (d) Layer 4: primary, and (e) Layer 5: shielding.

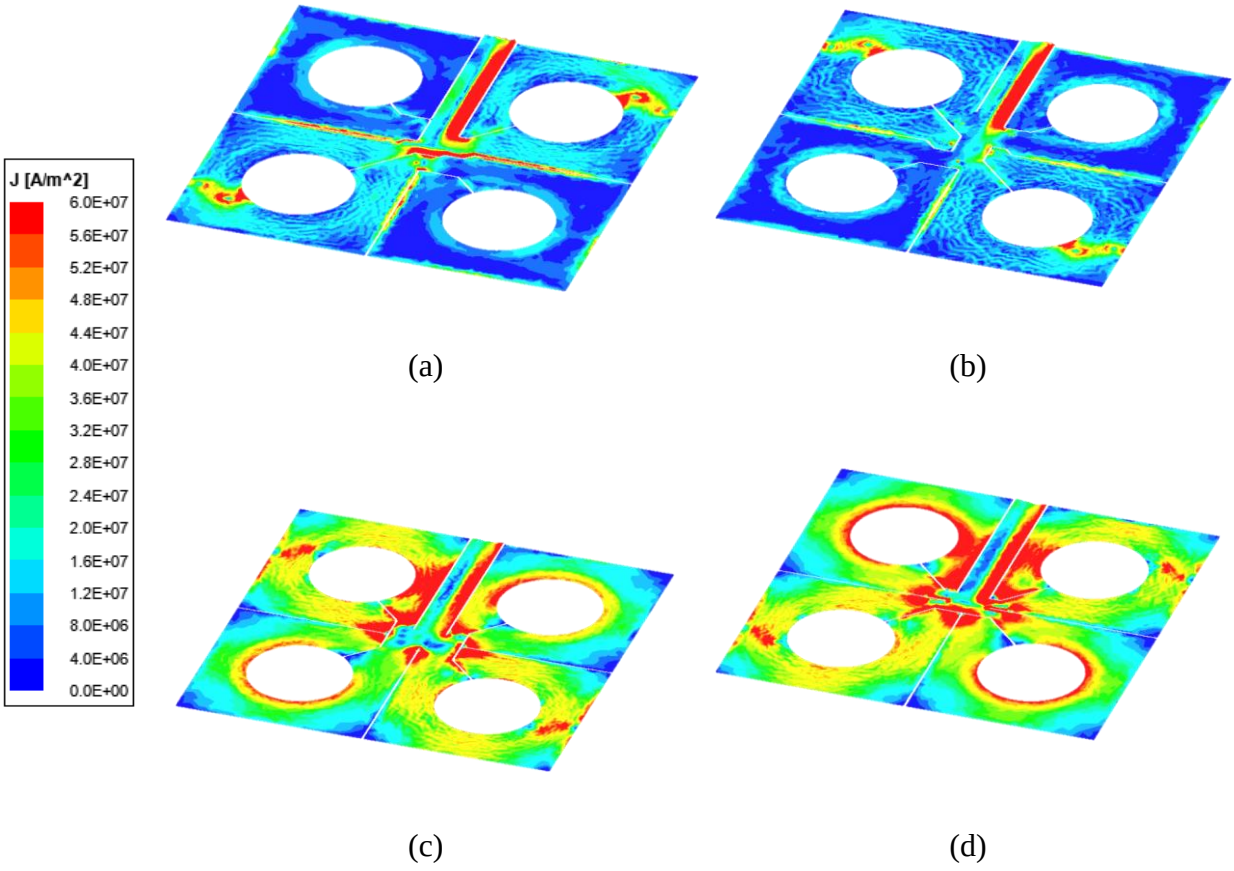


Fig. 3.15. 3D FEA simulated current density comparison between original and improved shield: (a) Layer 2 shield in original shielding, (b) Layer 5 shield in original shielding, (c) Layer 2 shield in improved shielding, and (d) Layer 5 shield in improved shielding.

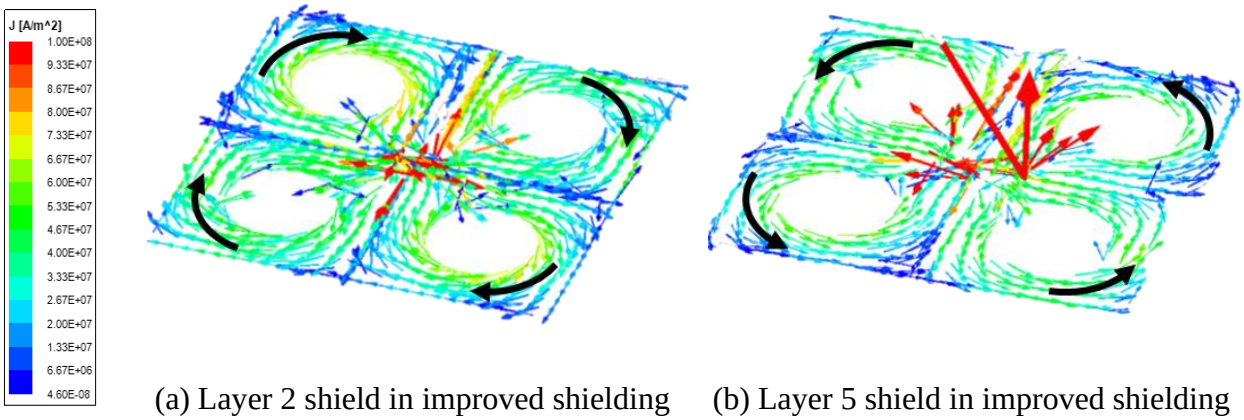


Fig. 3.16. Current directions in the paralleled shield windings in the improved shielding: (a) Layer 2 shield, and (b) Layer 5 shield.

To understand the reason for the circulating current, the electric field distribution within the six-layer planar transformer must be studied, as shown in Fig. 3.17.

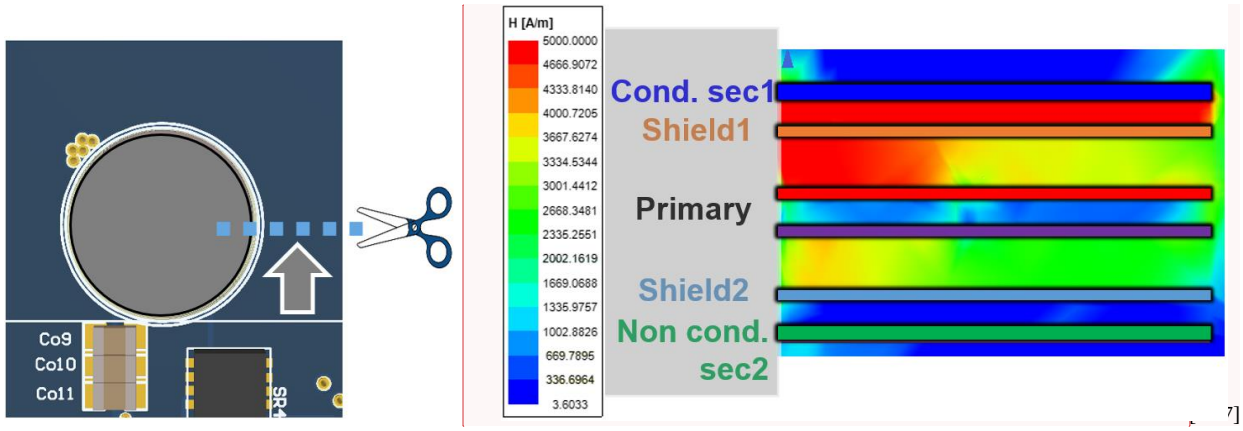
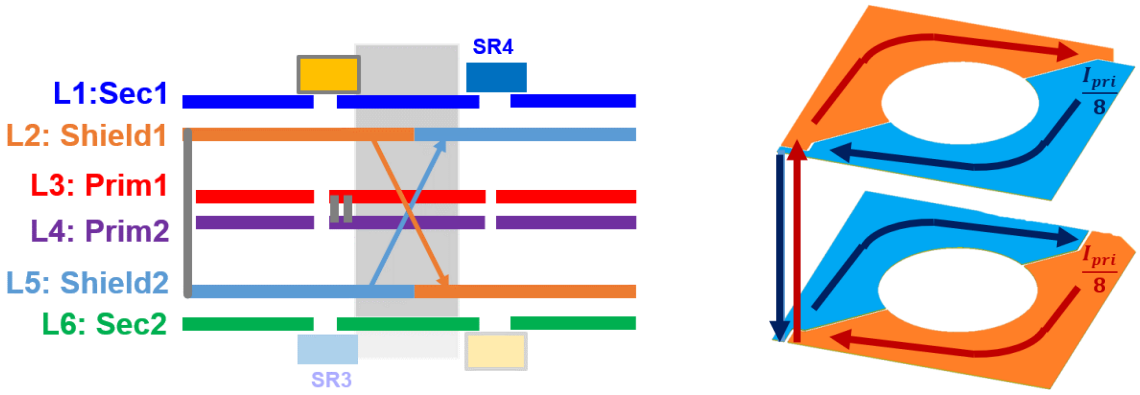


Fig. 3.17. Electric field distribution within the layers of a PCB transformer with CT rectifiers.

As discussed in Section 2.1, for transformers with CT rectifiers on the secondary side, the planar transformer design that has the secondary windings on the top and bottom layers is better in terms of termination loss. However, it has worse interleaving with the primary windings, as can be seen from the 2D FEA simulated electric field distribution in between the PCB windings of the planar transformer during one half-cycle. Since only one secondary layer conducts in each half-cycle, the electric field distribution is asymmetrical within the transformer. The shield layer closer to the conducting secondary generates eddy currents to cancel the magnetic fields from both secondary and primary windings between which it is placed. However, the other shield layer, which is placed between the primary windings and the non-conducting secondary winding, only induces eddy currents from the magnetic field of the primary windings. Thus, circulating current is induced to reduce the leakage energy difference between the two shield layers, resulting in the high current-density and shield winding losses, as observed in Fig. 3.15.

The solution for this is to expose both shield windings to equal electric fields within the transformer. To achieve this, the litz-wire concept of interleaving is implemented in the PCB windings. Fig. 3.18 shows the modified shield-winding arrangement, where the two parallel shield windings are interwound such that the equivalent electric field is homogeneous around both shield layers, resulting in no circulating current.



(a) (b)

Fig. 3.18. Interwound parallel shield layers to homogenize the electric field around them: (a) cross-section view, and (b) current flow in 3D view.

As can be observed, by employing vias, the two shield windings can be interleaved such that the equivalent electric fields around both shield layers are symmetrical. After this modification, the 3D FEA simulation yields normal current densities in the shield windings, as shown in Fig. 3.19. The shield winding loss is 0.6 W, which is 8% lower than the original shield winding due to better primary current distribution across both shield windings.

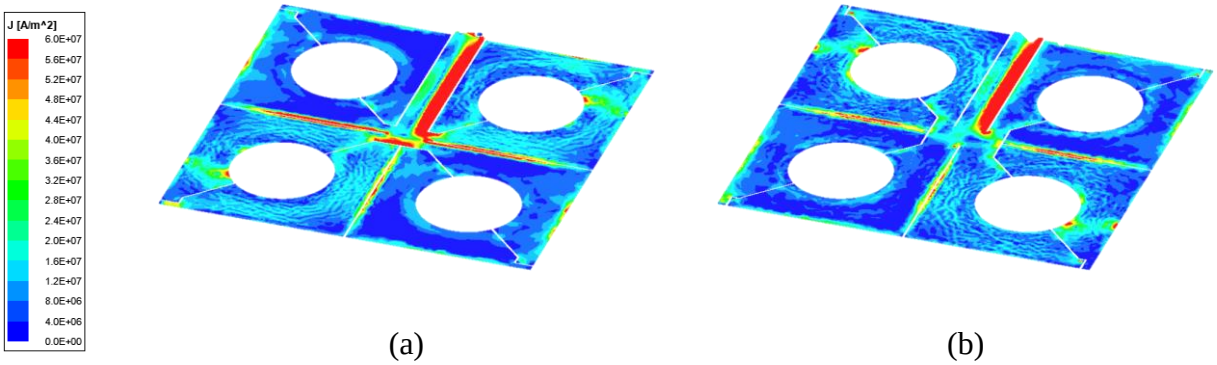


Fig. 3.19. Current density in the paralleled shield windings with interleaved shielding: (a) Layer 2 shield, and (b) Layer 5 shield.

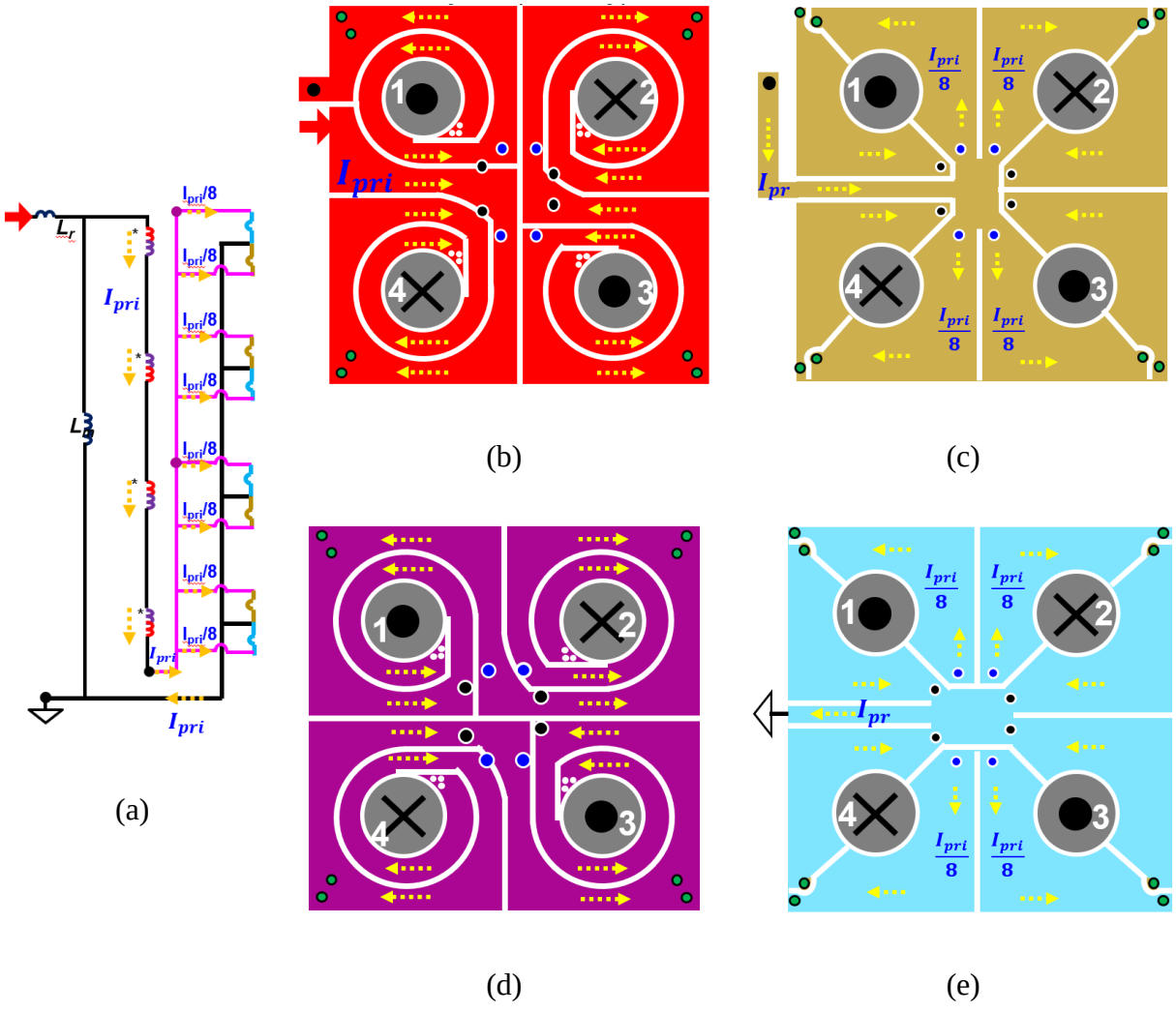


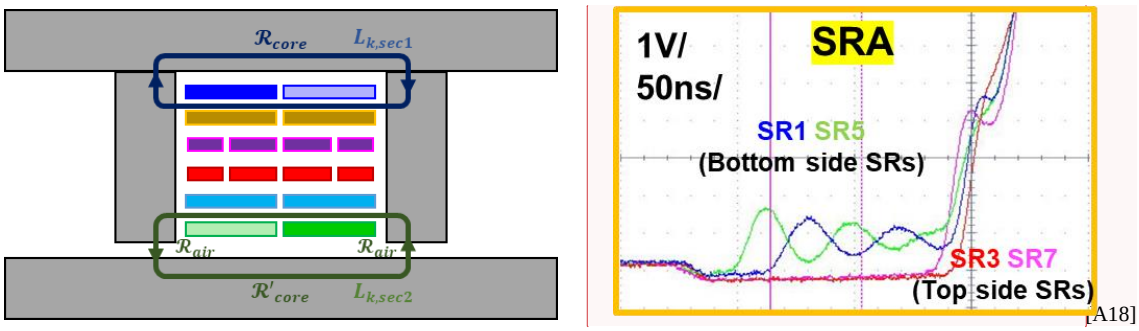
Fig. 3.20. PCB winding arrangement for improved and interleaved shielding: (a) transformer schematic with improved shielding, (b) Layer 3: primary, (c) Layer 2: shielding, (d) Layer 4: primary, and (e) Layer 5: shielding.

Fig. 3.20 shows the final PCB winding arrangement of the improved and interleaved shield windings. The green vias on the four corners of the matrix transformer are used to interleave the two shield windings. Although they make holes to pass through the primary windings, which are sandwiched between the two shield windings, the current densities on the winding corners are negligible as far as causing a significant increase in winding loss.

3.4 Impact of Transformer Airgap on Leakage Inductance

From Fig. 3.9, it can be observed that the body-diode conduction periods of SRs that are placed on the bottom layer are lower than those placed on the top layer. This is because of the different proximities of the two secondary layers to the transformer's airgap. Fig. 3.21 (a) shows the cross-section of the construction of a typical planar transformer; as shown, the airgap is situated just outside the PCB, hence making it closer to one of the secondary layers.

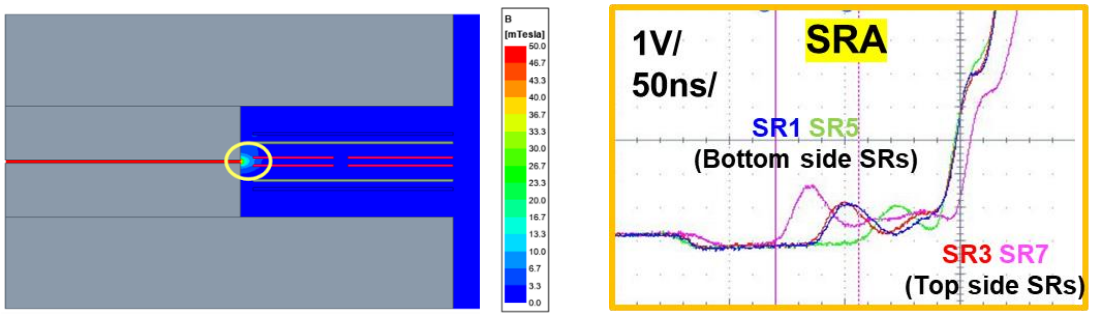
The leakage inductance paths for the two secondary layers on the top and bottom layers are shown in the transformer cross-sectional view in Fig. 3.21 (a) [32]. For the secondary winding in the top layer, the reluctance of the leakage path is $\mathcal{R}_{core}$, whereas that for the secondary winding in the bottom layer is $\mathcal{R}'_{core} + 2\mathcal{R}_{air}$. Since air has a much high reluctance than the ferrite core, the leakage path for the secondary layer close to the airgap has higher reluctance, and lower leakage inductance than the secondary layer away from the airgap.- Therefore, as can be seen in Fig. 3.21 (b), the higher leakage inductances of the secondary (also seen in the 3D FEA simulations in Fig. 3.11) result in a lower body-diode conduction period as compared to the SRs on the top secondary layer (Fig. 3.9), and this causes some current-sharing issues.



(a) (b)

Fig. 3.21. Asymmetrical leakage inductance and current sharing with airgap on one end of transformer: (a) leakage inductance path for secondary, and (b) V_{DS} of SRs during turn-off.

To achieve better symmetry, the airgap can be moved to the middle of the transformer leg, as shown in Fig. 3.22 (a). By doing so, the reluctance of the leakage paths – and hence the leakage inductance – will be more symmetrical for the top and bottom secondary layers. This results in a significantly lower difference in the body-diode conduction periods between the SRs on the top and bottom secondary layers, as shown in Fig. 3.22 (b).

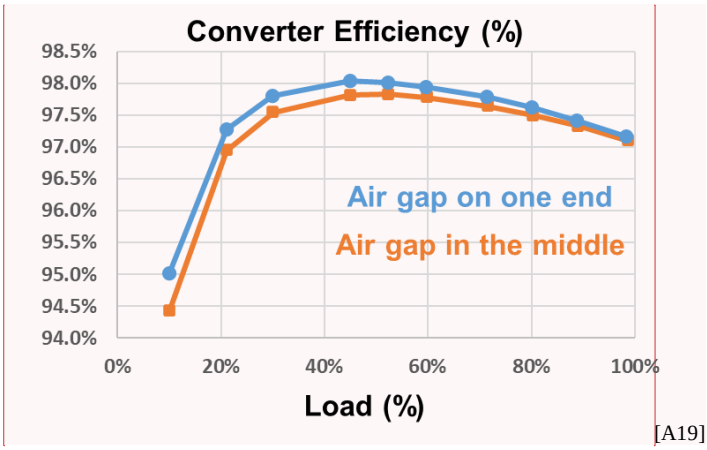


(a) (b)

Fig. 3.22. Symmetrical fringing flux and current sharing with airgap in the middle of transformer: (a) fringing flux with airgap in the middle, and (b) V_{DS} of SRs during turn-off.

However, moving the airgap to the middle also exposes the other PCB layers to the fringing flux of the airgap, thereby inducing eddy currents in them, too [33]. Since the eddy current loss is independent of load, this results in a reduction in the light-load efficiencies when a hardware

prototype of the 800W 400V/12V LLC converter running at 600 kHz was tested with the airgap on one side and in the middle, as shown in Fig. 3.23.



[A19]

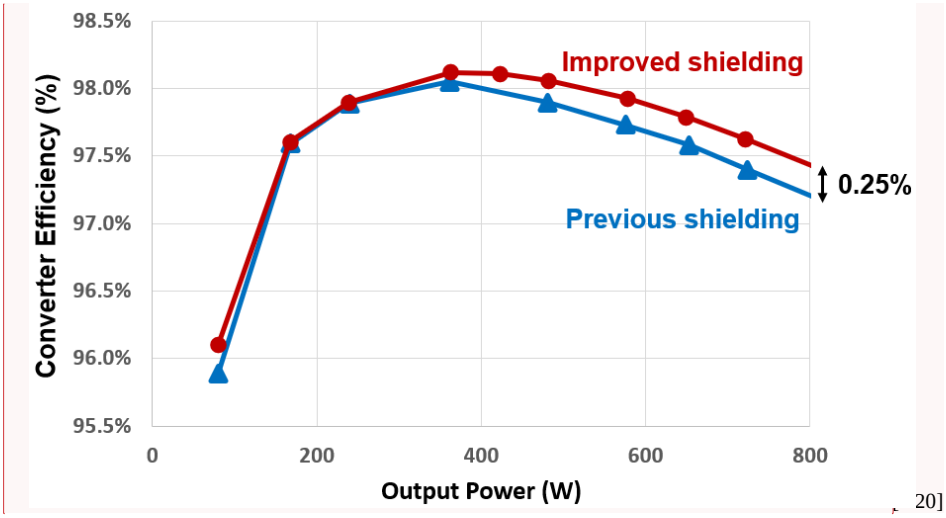
Fig. 3.23. Efficiency reduction when moving the airgap to the middle.

One solution for mitigating the eddy current induction in the PCB layers that occurs due to the fringing flux of the airgap is to increase the clearance between the transformer core and the PCB windings. However, while maintaining the same transformer footprint, doing so will reduce the winding width correspondingly. At light and medium loads, the eddy current losses contribute a significant percentage of the transformer loss, and hence the clearance between the transformer core and PCB windings can be optimized to minimize the transformer loss. However, at higher loads, the percentage of the winding losses are so high that any reduction in fringing losses from increasing the clearance is overshadowed by the increase in winding loss due to lower winding widths.

3.5 Hardware Verification of Efficiency Improvement

To verify the current-sharing improvement with the symmetrical shielding structure over the previous asymmetrical shielding, a 400V/12V LLC converter was built with the improved

shielding technique, and the converter efficiency was compared with the previous shielding technique, as shown in Fig. 3.24. The converters were operated at 600 kHz.



20]

Fig. 3.24. Efficiency improvement with improved shielding.

It can be observed that, with the better current sharing that happens with improved symmetrical shielding, the conduction losses are lower, resulting in an improvement in full-load efficiency by up to 0.25%, which represents a converter loss that is around 2W lower. This result exhibits the importance of having good current sharing between the different elemental transformers in the matrix transformer in high-current applications.

Fig. 3.25 shows the measured CM noise spectrum of the LLC converter with improved shielding, as compared to that with previous shielding and no shielding. As the fundamental shielding concept remains the same in the two shielding techniques, a CM noise reduction of around 25 dBµV over most of the frequency spectrum up to 20 MHz can be achieved over the converter with no shielding. This exhibits that, with similar shielding performance, the symmetrical shielding can achieve higher converter efficiencies over the previous asymmetrical counterpart.

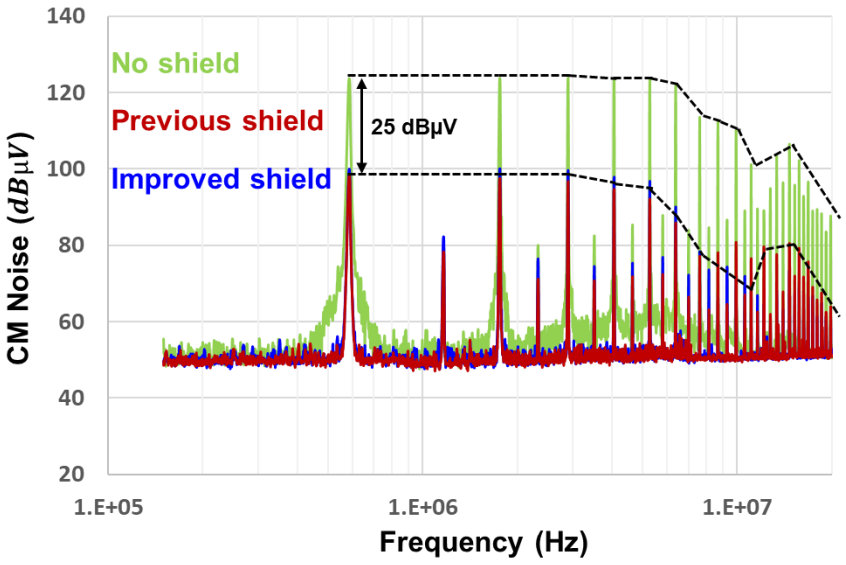


Fig. 3.25. CM Noise measurement spectra.

3.6 Conclusions

This chapter has discussed the requirement for shielding in planar matrix transformers, and reviewed the existing techniques of shielding, the most effective being one where half the shield windings double as primary windings to increase the effective turns ratio by 1, thereby improving efficiency.

Next, the current sharing in the matrix transformer was studied by examining the V_{DS} of the SRs during the turn-off period. Different leakage inductances of the secondary windings in the two half-cycles lead to different body-diode conduction periods, resulting in current-sharing issues. This challenge was traced to the asymmetrical shielding structure, where the same shield layer conducts in both half-cycles, which results in different proximities to the conducting secondary windings.

This issue was addressed by paralleling the two shield windings. However, due to imperfect interleaving in the center-tapped rectifiers, the two shield layers are exposed to different electric

fields in the transformer, resulting in current circulating among them. To overcome this, the litz-wire concept was implemented on PCB windings; in this approach, the two shield layers are interleaved and paralleled, resulting in them being exposed to the same electric field. The modified shielding structure was shown to have symmetrical leakage inductances in the two half-cycles of operation, resulting in much better current sharing.

Moreover, the location of the transformer airgap also affects current sharing in planar transformers. Typically, the airgap is placed on one end of the PCB windings. However, this approach results in an induction of eddy currents in the secondary layer closer to the airgap, in which causes a higher leakage inductance to occur than on the secondary layer away from the airgap. To address this, the airgap can be moved to the middle of the PCB such that both secondary layers are exposed to equal fringing flux, resulting in symmetrical leakage inductances. However, this also means eddy currents will be induced in the other PCB layers due to their proximity to the airgap. This affect can be reduced by increasing the clearance between the windings and the core leg, at a cost of lower heavy-load efficiencies due to lower winding widths at the same transformer footprint.

Finally, to verify the improvement in current-sharing, an 800W 400V/12V LLC converter prototype was developed, which could achieve up to 0.25% higher efficiency at full-load as compared to the converter with the previous asymmetrical shielding. Moreover, both shielding techniques achieve similar reduction in CM noise as compared to the converter with no shielding.

Chapter 4. Resonant Frequency Optimization of LLC Converters

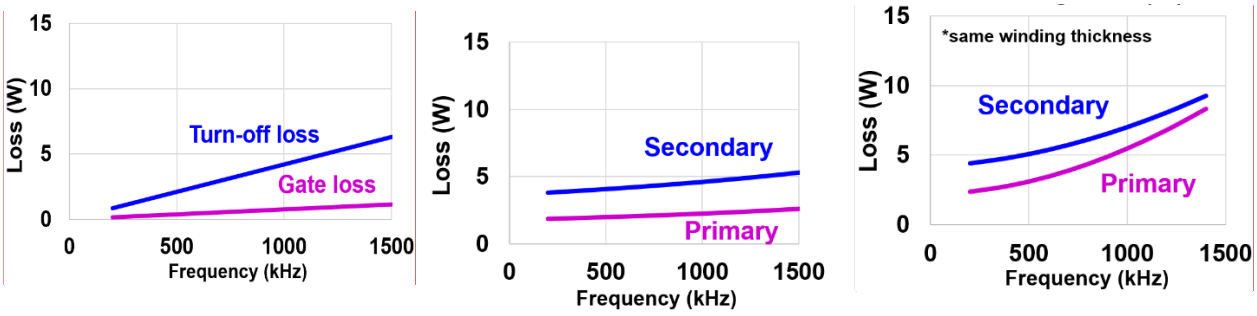
4.1 Introduction

As discussed in the introduction, the motivation for this thesis is to further improve the performance of the previous CPES 400V/12V LLC converter in order to keep pace with the performance levels of the latest technologies and with the ever-increasing demand for datacenters. In the previous chapters, different aspects of converter performance were studied to improve the converter's efficiency, including termination design optimization and a design that achieves improved current-sharing with symmetrical shielding. This chapter will address another aspect of converter performance optimization – the switching frequency.

For LLC converters, such as this one, operating as unregulated DC-DC transformers, the converter switches exclusively at the resonant frequency, at which point the converter efficiency is at its maximum. In all the previous work that CPES did on the 400V/12V LLC converter, the switching frequency was fixed to 1 MHz in order to exhibit the high-frequency operability and high power densities of the converter.

However, the various losses in the converter, such as the device losses and the transformer losses, are highly dependent on the switching frequency. As shown in Fig. 4.1, the device turn-off loss, the gate driving loss and the conduction losses all increase with frequency. Moreover, the transformer's winding losses also increase with frequency, since the winding AC resistance and the winding currents increase with frequency [34]. However, the transformer's core loss decreases with increasing frequency, as Fig. 4.1 shows in the core loss of the ML-91s material at fixed

voltage excitation. Lower core losses at higher frequencies allow the transformer size to be shrunk, which is the main motivation behind pushing for higher frequencies.



[A21] [A22]

(a) (b) (c)

Fig. 4.1. Converter losses that increase with switching frequency: (a) device switching loss, (b) device conduction loss, and (c) transformer winding loss.

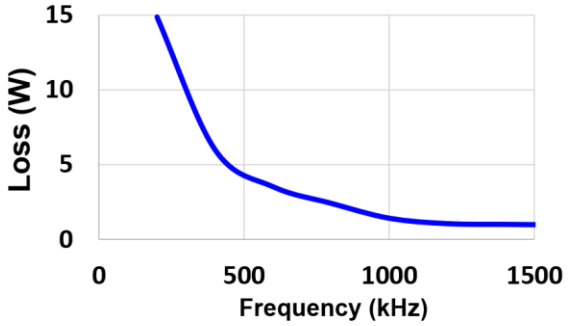
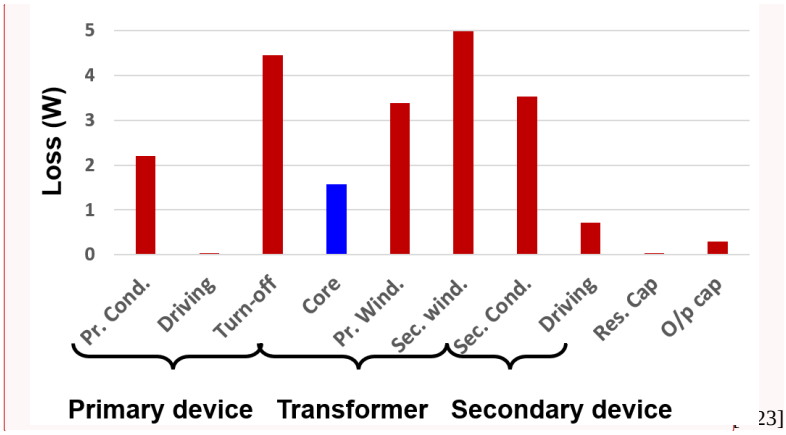


Fig. 4.2. Transformer core loss decreases with switching frequency.

There is clearly a tradeoff between the different losses in the converter with changes in frequency. Moreover, for low-voltage, high-current applications such as this one, the losses that increase with frequency (conduction losses) outweigh the one that decreases with frequency (core loss), as seen in the converter loss breakdown at 1 MHz in Fig. 4.3. The red bars show the losses that increase with switching frequency and the blue bar shows the loss that decreases with switching frequency. Clearly, for such applications, the switching frequency must be optimized to maximize the efficiency, while also studying the impact on power density.



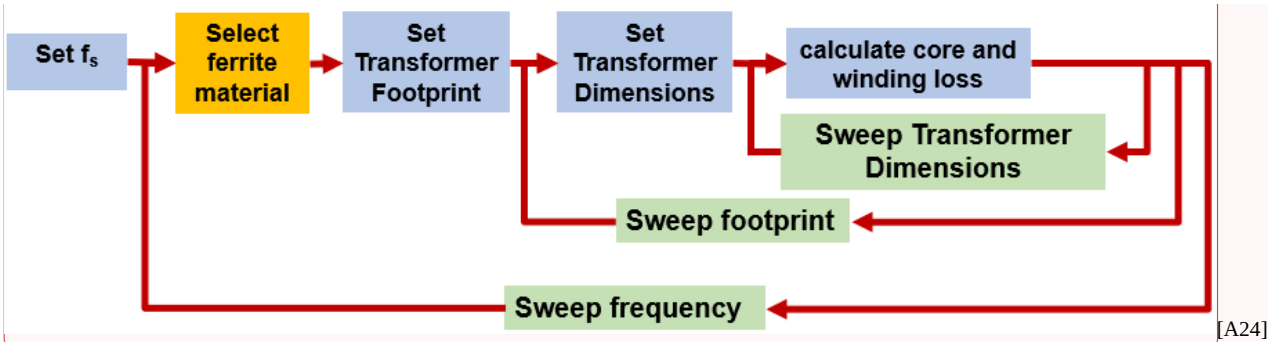
23]

Fig. 4.3. Loss breakdown of 400V/12V LLC converter at 1 MHz.

In this chapter, the switching frequency for the 400V/12V LLC converter is optimized. Core loss densities of different ferrite materials are evaluated, and a material selection guideline is provided. Finally, the converter's loss and power density are evaluated at different frequencies, and the optimal frequency is selected. The performance improvement is showcased with hardware results at the optimized frequency.

4.2 Optimal Ferrite Material Selection at Different Frequencies

Fig. 4.4 shows the flowchart for optimizing the switching frequency of the LLC converter.



[A24]

Fig. 4.4. Flowchart showing switching-frequency optimization process.

The first step is to select the best ferrite material at the selected switching frequency. Typically, Mn-Zn ferrite materials are used to design the transformer cores in high-frequency applications [35]. Companies design using different materials, which are then recommended to be operated at a specific frequency range for optimal performance. Among those, the ferrite material with the lowest core loss density is typically selected for the transformer design. The core loss density P_v is given by the popular Steinmetz equation:

$$P_v = k \cdot B_{max}^{\beta} \cdot f_s^{\alpha}, \tag{4.1}$$

where B_{max} is the peak magnetic flux density in the core, f_s is the switching frequency, and α, β, and k are the Steinmetz coefficients that are uniquely defined for each material. Moreover, B_{max} can be defined as:

$$B_{max} = \frac{\int_0^{\frac{T_s}{2}} v_0 \, dt}{2 \, n \, A_e} = \frac{V_o}{4 \, A_e \, f_s}, \tag{4.2}$$

where v_0 is the instantaneous output voltage, n is the turns ratio, A_e is the cross-sectional area of the core, and T_s is the switching period.

Combining (4.1) and (4.2), P_v can be written as a function of f_s, as follows:

$$P_v = k \cdot \left(\frac{V_o}{4A_e}\right)^{\beta} \cdot f_s^{\alpha-\beta}. \tag{4.3}$$

Generally, $\beta > \alpha$ for ferrite materials, which results in a reduction in core loss density with increases in frequency. Also, $\alpha - \beta$ determines the degree to which the core loss density decreases with increases in frequency.

The materials datasheets typically provide average Steinmetz coefficients for different frequency ranges, but this results in some unanswered questions, leading to the motivation to experimentally measure the core loss densities.

To demonstrate this, the 3F3 material from Ferroxcube can be used as an example. Table 4.1 shows the Steinmetz coefficients provided in its datasheet, where different coefficients are provided for different frequency ranges.

Table 4.1. Steinmetz coefficients for 3F3 from datasheet.

Switching Frequency (kHz)	K	β	α
200 – 400	2.2×10^{-6}	2.6	2
400 – 700	6.5×10^{-9}	2.45	2.42

It can be observed that from 200 kHz – 400 kHz, $P_v \propto f_s^{-0.6}$, which means increasing the frequency within this range will be beneficial toward reducing the core loss density. Moreover, from 400 kHz – 700 kHz, $P_v \propto f_s^{-0.03}$, which means that in this frequency range, increasing the frequency has negligible impact on the core loss density, hence negating any benefits of doing so. However, from the average Steinmetz coefficients provided in the datasheets, it is impossible to pinpoint the exact frequency at which frequency will stop impacting core loss density.

Another discrepancy can be observed from the Steinmetz coefficients provided in the datasheet for ML-91s from Hitachi metals. Table 4.2 shows different coefficients provided for different frequency ranges.

Table 4.2. Steinmetz coefficients for ML-91s from datasheet.

Switching Frequency (MHz)	K	β	α
0.5 – 1	2.02×10^{-7}	3.553	2.241
1 – 3	2.067×10^{-11}	3.077	2.784

The P_v calculated at 1 MHz (and $B_{max} = 80mT$, a typical design point) using the first and second sets of coefficients results in $P_v = 714\ kW/m^3$ and $P_v = 441\ kW/m^3$, respectively, a significantly large 62% difference. Therefore, it is difficult to determine the exact core loss density at the boundary frequencies defined by the datasheets.

These reasons led to the requirement to experimentally measure the core loss densities of various materials to accurately characterize them at different frequencies. Different Mn-Zn ferrite materials with low core loss densities (according to their datasheets) are selected for testing, as summarized in Table 4.3.

Table 4.3. Mn-Zn ferrite materials selected for core loss testing.

Recommended Range	Material	Manufacturer
Low Frequency ($f_s < 400kHz$)	3C98	Ferroxcube
	ML27D	Hitachi
Medium Frequency ($400kHz < f_s < 800kHz$)	ML95s	Hitachi
	3F36	Ferroxcube
	P53	ACME
High Frequency ($f_s > 800kHz$)	ML91s	Hitachi
	DMR-51W	DMEGC
	P63	ACME

The core loss densities are measured using toroidal cores, such that there is uniform magnetic flux throughout the core. The two-winding method with capacitive cancelation and partial cancelation concept is used to measure the core loss densities [36][37].

The core loss densities of all the materials are measured at room temperature at different B_{max} and at different f_s, resulting in numerous curves. To make the characterization and comparison significantly simpler and more straightforward, the performance factors of different materials are evaluated [38][39]. The physical significance of this parameter can be understood from the following equations:

$$P_v = \frac{Core\ loss}{Volume} = \frac{Core\ loss}{A_e \cdot l}, \tag{4.4}$$

where l is the mean path length for the magnetic flux. A_e can then be expressed as:

$$A_e = \frac{Core\ loss}{P_v \cdot l}. \tag{4.5}$$

Rearranging (4.2) to move f_s to the left-hand side (LHS),

$$B_{max} \cdot f_s = \frac{V_o}{4\,A_e}. \tag{4.6}$$

Substituting A_e from (4.5) into (4.6) yields

$$B_{max} \cdot f_s = \frac{V_o \cdot P_v \cdot l}{4} \frac{1}{Core\ loss}. \tag{4.7}$$

The term on the LHS can be defined as the performance factor, $\mathcal{F}$, as:

$$\mathcal{F} = B_{max} \cdot f_s. \tag{4.8}$$

It can be observed from (4.7) that for a fixed core loss density and effective path length (core size), a material with higher performance factor will result in a lower core loss while achieving the same output voltage.

Based on this, the performance factors of the different materials were calculated and plotted against the switching frequency at a fixed $P_v = 0.5 W/cm^3$, which is the typically observed value for this application, as shown in Fig. 4.5.

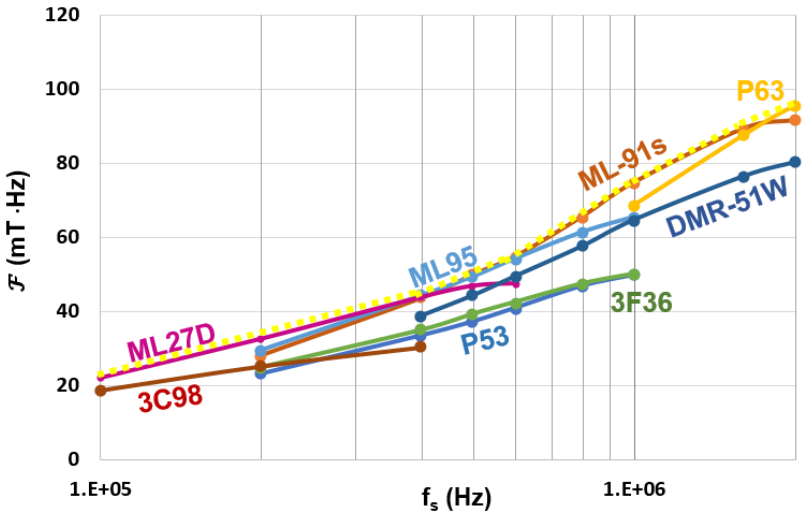


Fig. 4.5. Performance factors of ferrite materials at $P_v = 0.5W/cm^3$.

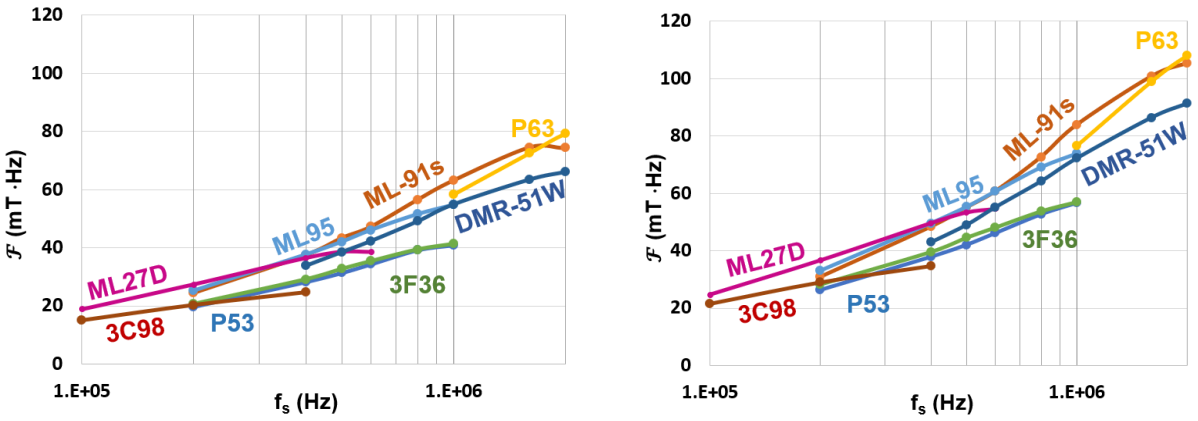
The frequencies for the different materials were pushed until the performance factor curves started plateauing, as can be seen in the curves for ML27D and ML91s in Fig. 4.5. The frequency was swept from 100 kHz – 2 MHz and the eight listed materials were tested in the relevant frequency ranges. Based on the performance factor curves, the materials with the highest performance factors at each frequency can be traced as shown by the yellow dotted line in Fig. 4.5 and as summarized in Table 4.4.

Table 4.4. Summary of materials with highest performance factors.

Frequency Range (kHz)	Material with Highest Performance Factor	Company
100 – 300	ML27D	Hitachi
400 – 600	ML95s	Hitachi
700 – 1500	ML91s	Hitachi
>1500	P63	ACME

It may be noted that the ferrite materials from Hitachi Metals perform significantly better than those from other companies.

To generalize this study to other applications with different core loss densities, the performance factors at $P_v = 0.3W/cm^3$ and $P_v = 0.7W/cm^3$ were also calculated and plotted against frequency, as shown in Fig. 4.6.



(a) (b)

Fig. 4.6. Performance factor comparison at different core loss densities: (a) $P_v = \frac{0.3W}{cm^3}$, and (b) $P_v = 0.7W/cm^3$.

It can be observed that, even within a wide range of core loss densities, the relative performance factors of the materials are largely similar. This means that for other applications with different core loss densities, the results from this study can be used as a design guideline for transformer core material selection.

4.3 Resonant Converter Performance Evaluation

Once the best-performing ferrite materials have been chosen, the converter loss is calculated at different frequencies. The switching frequency is swept from 200 kHz – 1.6 MHz. The loss of the matrix transformer shown in Fig. 4.7 is calculated using the same method as used in [18], as summarized below.

Since the transformer voltage is rectangular, the core loss expression is modified as given in [40]:

$$P_v = \frac{8}{\pi^2} \cdot k \cdot B_{max}^{\beta} \cdot f_s^{\alpha}, and \tag{4.9}$$

$$P_{core} = P_v \cdot Vol_{core}, \tag{4.10}$$

where the $8/\pi^2$ term is included to account for the rectangular transformer voltage, P_{core} is the core loss, and Vol_{core} is the core volume.

The transformer winding DC resistance is given by:

$$R_{DC} = \frac{\rho \cdot 2\pi}{h} \cdot \frac{n^2}{ln(c+r) - ln\, r}, \tag{4.11}$$

where h is the PCB layer thickness (copper weight), ρ is the resistivity of copper, n is the turns ratio, c is the winding width, and r is the core radius.

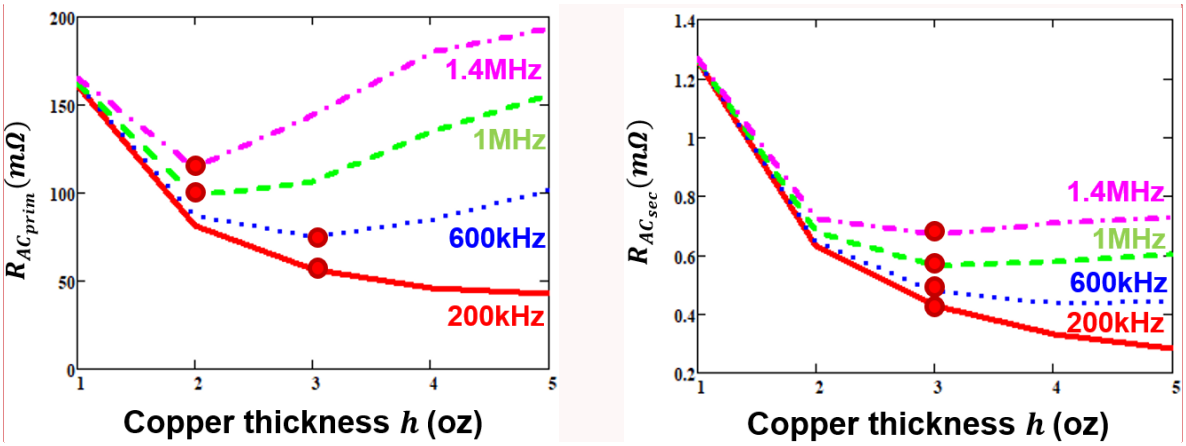
The AC resistance coefficient F_R is defined by the eddy current model described in [34] as:

$$F_R = M' + \frac{(m^2 - 1)}{3} D', \tag{4.12}$$

where M' and D' are the real parts of M and D, respectively; and $M = \alpha h \coth(\alpha h)$, $D = 2\alpha h \tanh(\alpha h/2)$, $\alpha = \sqrt{j\omega\mu_0\eta/\rho}$, $\eta = N_l a/b$, m is number of layers in a winding porting, ω is angular frequency, h is winding copper thickness, N_l is the number of turns per layer a is the total winding area width, and b is the winding width for each turn. The winding AC resistance can then be defined as:

$$R_{AC} = F_R \cdot R_{DC}. \tag{4.13}$$

From (4.12), it can be noted that the AC resistance is dependent on copper thickness h and switching frequency $\omega/2\pi$. The optimal copper thickness is where the winding AC resistance is at its minimum. Hence, the AC resistances are calculated and plotted as a function of h at different frequencies, as shown in Fig. 4.7.



[A25]

Fig. 4.7. Copper thickness optimization at different frequencies.

Fabricating PCBs with greater than 3oz Cu is very expensive, and given the diminishing returns with higher copper weights, 3oz Cu is set as the maximum thickness. For the primary windings, for $f_s < 1MHz$, 3oz Cu is selected as the optimal thickness, and for $f_s \geq 1MHz$, 2oz Cu is selected as the optimal thickness. For the secondary windings, 3oz Cu is selected as the optimal thickness at all frequencies.

The winding loss can then be simply calculated as:

$$P_{winding} = R_{AC} \cdot I_{rms}^2, \tag{4.14}$$

where I_{rms} is the transformer rms current.

The total transformer loss is the sum of the core and winding losses:

$$P_{transformer} = P_{core} + P_{winding}. \tag{4.15}$$

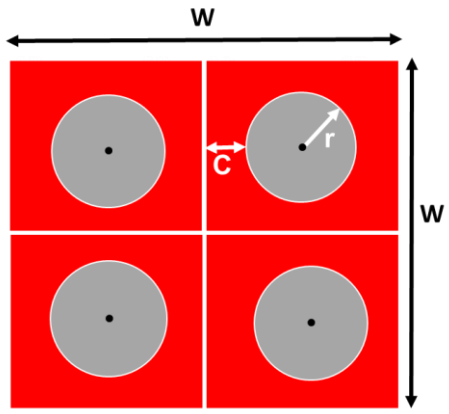
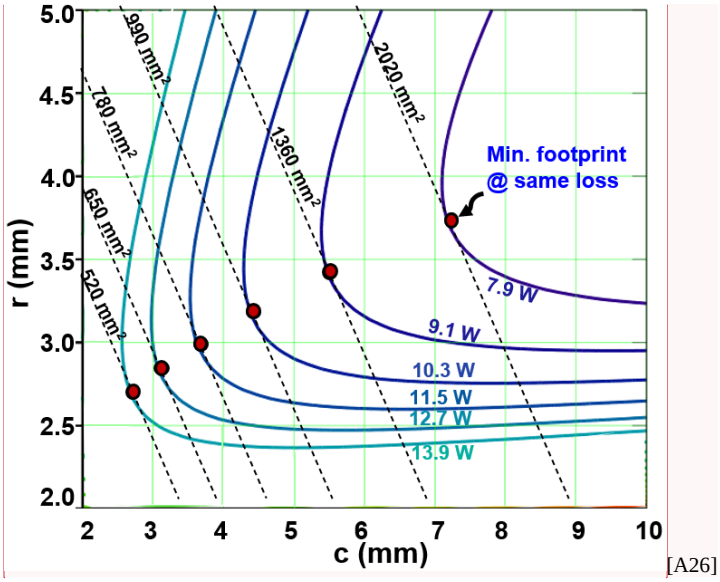


Fig. 4.8. Matrix transformer dimensions.

From Fig. 4.8, the transformer footprint can be calculated as:

$$FP = W^2 = (4r + 4c)^2. \tag{4.16}$$



[A26]

Fig. 4.9. Transformer loss optimization.

Fig. 4.9 shows transformer loss contours plotted at different core radii and winding widths at a frequency of 1 MHz. The dotted lines are the transformer's footprint contours. The knee-point in each loss contour, shown by the red dot, corresponds to a footprint contour, which is the minimum footprint required to realize that loss. Hence, at each transformer footprint, the minimum transformer loss can be achieved solely with a unique r and c combination (red dot). This also demonstrates the tradeoff between the core loss and the winding loss, where a higher r results in a lower core loss, but a higher c results in a lower winding loss.

This process is repeated for different frequencies and the minimum transformer losses can then be traced out and plotted against the transformer footprint, as shown in Fig. 4.10.

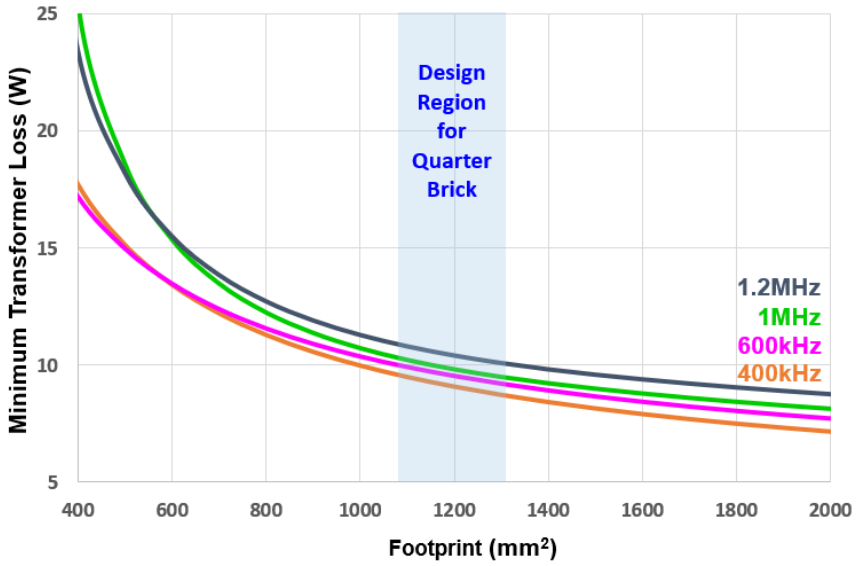


Fig. 4.10. Minimum transformer loss vs. transformer footprint.

It can be intuitively observed that the transformer loss reduces with as the transformer footprint grows. However, there are diminishing returns upon increasing the footprint, and the footprint design point must be chosen at the knee point of the curve for optimal performance.

However, since this application is restricted by the quarter-brick form factor, the design region is chosen around the 1200 mm^2 footprint region, which is also around the knee points of the curves.

The optimal r and c values at 1200 mm^2 footprint at various switching frequencies are listed in Table 4.5.

Table 4.5. Optimal transformer dimensions.

Frequency (kHz)	Core Radius, r (mm)	Winding Width, c (mm)	r/c
200	4.9	3.4	1.45
600	3.75	4.6	0.8
1000	3.45	4.9	0.7
1400	2.9	5.4	0.55

The core radius to winding width ratio indicates the ratio of the core loss to winding loss in the transformer. As the frequency increases, the winding loss increases and the core loss decreases, hence resulting in a decrease in the r/c ratio.

Finally, the total converter loss for the 1kW 400V/12V LLC converter at different switching frequencies needs to be evaluated. Fig. 4.11 shows the transformer loss at a footprint of 1200 mm^2, with device loss and total converter loss plotted against the switching frequency of the converter.

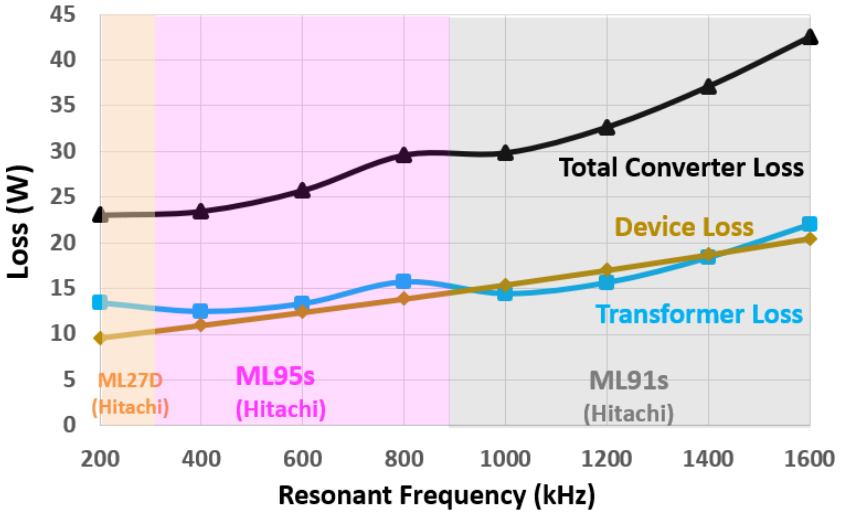
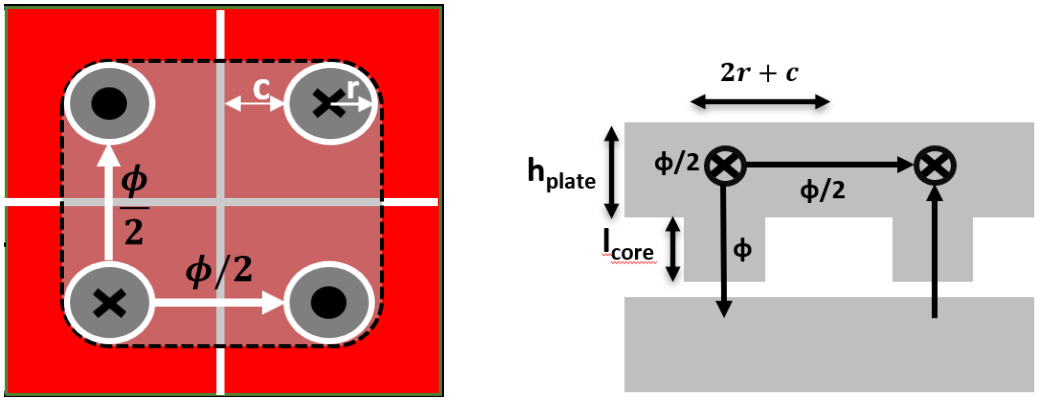


Fig. 4.11. Different converter losses as a function of resonant frequency.

The different regions show the different ferrite materials used at different frequencies. It must be noted that the maximum magnetic flux density B_{max} for the ML91s material was restricted to 80 mT based on its material requirements. The transformer loss increases with frequency with the same material, as the increase in winding loss is higher than the reduction in core loss. However, the transformer loss reduces at the frequencies when the core material changes, as switching to a better material results in lower core loss.

In addition to the converter loss, the converter power density must also be studied to completely analyze the impact switching frequency has on the converter's performance. Since the transformer, and hence, converter footprint, are fixed at all frequencies, the power density is dependent on the transformer's core profile. The plate thickness is calculated such that there is uniform magnetic field distribution throughout the transformer. Fig. 4.12 shows the magnetic flux density in the core legs and plates.



(a) (b)

Fig. 4.12. Magnetic flux density in the transformer: (a) top view, and (b) cross-sectional view.

The magnetic flux density in the plates is half of that in the core legs. Therefore, for uniform magnetic field in the transformer,

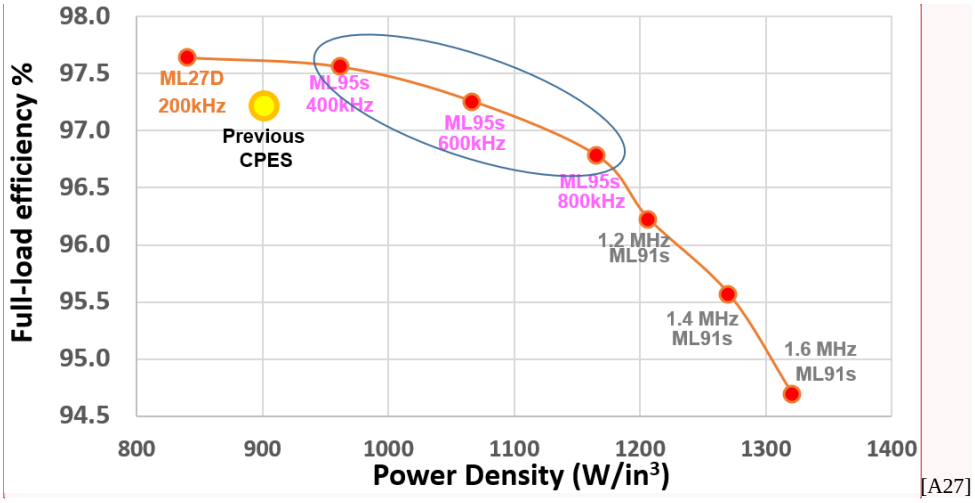
$$\frac{\phi}{A_{leg_{core}}} = \frac{\phi/2}{A_{plate_{eff}}}, \tag{4.17}$$

where ϕ is the magnetic flux density in the core legs, c is the cross-section area of the core leg, and $A_{plate_{eff}}$ is the effective cross-section area of the plate. Solving (4.17), the required plate thickness h_{plate} is given by:

$$h_{plate} = \frac{\pi r^2}{2r + c}. \tag{4.18}$$

From Table 4.5, r decreases and c increases with increases in frequency. This results in a decrease in plate thickness with increases in frequency, resulting in higher power density with increases in frequency.

Fig. 4.13 shows the converter's full-load efficiency versus power density at different switching frequencies.



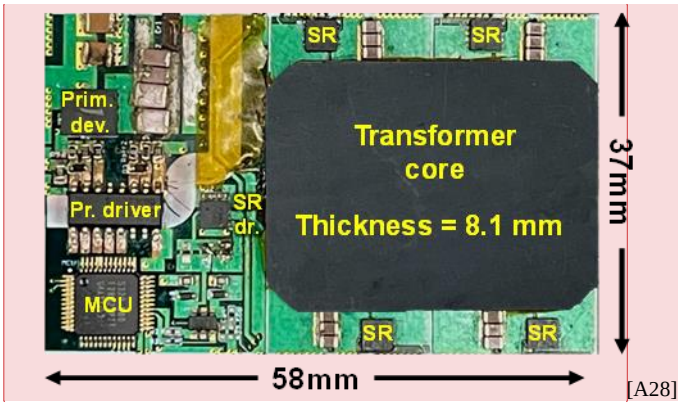
[A27]

Fig. 4.13. Full-load efficiency versus power density at different frequencies.

The previous CPES converter's performance is shown by the yellow dot. The curve behaves as expected – there is a tradeoff between converter efficiency and power density with changes in switching frequency. When the frequency is reduced from 400 kHz, there is a diminishing return in efficiency improvement. Moreover, when the frequency increases from 800 kHz, the efficiency drops very quickly owing to the high conduction and winding losses at higher frequencies. Hence, a sweet spot for converter design can be set between 400 kHz and 800 kHz. Based on the design requirements, either the converter efficiency or the power density can be prioritized, and the corresponding switching frequency can be selected to optimize converter design.

4.4 Hardware Verification of Proposed Performance Improvement

To demonstrate the increase in efficiency compared to the previous CPES converter, a 1kW 400V/12V LLC converter running at 400 kHz was designed. Fig. 4.14 shows the hardware prototype of the LLC converter.



[A28]

Fig. 4.14. Hardware prototype of proposed converter.

The converter dimensions are 58 mm x 37 mm x 8.1 mm, resulting in a power density of 940 W/in^3. This is higher than the previous CPES converter even after operating at lower frequencies due to the higher rated power. Thermally, it is difficult to push more than 800 W (with air cooling

and no heat sinks) at 1 MHz operation due to the high device and transformer temperatures that occur because of high conduction losses. However, at a lower frequency of 400 kHz, the device's conduction losses are much lower, which allows the rated power to be increased, while being thermally sound.

Table 4.6 shows the specifications of the proposed converter, compared with that of the previous CPES converter.

Table 4.6. Specifications of the proposed LLC converter.

Component	Previous CPES	This Work
Rated Power	800 W	1 kW
Resonant Frequency	1 MHz	400 kHz
Dead Time	90ns	125 ns
Transformer Turns Ratio	16:1	16:1
Primary Devices	PGA26E08	80 mΩ GaN
Secondary Devices	BSC0500NSI	BSZ0500NSI
Primary Driver	Si8273	Si8273
Secondary Drivers	FAN3122	FAN3122
Shielding Technique	Asymmetrical	Symmetrical
Output Filter Capacitance Per Leg	6 x 10 µF	6 x 10 µF
Resonant Capacitor	71 nF	287 nF
Resonant Inductance	312 nH	478 nH
Magnetizing Inductance	25 uH	80 µH
Transformer Footprint	1200 mm^2	1200 mm^2
Core Radius	3.5 mm	4.5 mm
Winding Width	4.9 mm	3.9 mm
Power Density	900 W/in^3	940 W/in^3

The resonant frequency is reduced to 400 kHz as optimized in the previous section. The leakage inductance, which is used as the resonant inductance, is 478 nH. The resonant capacitance is then accordingly set such that the resonant frequency equals the switching frequency. The magnetizing inductance and the dead time are optimized according to the methodology in [15] to result in 80 µH and 125 ns, respectively. The primary device is replaced with a new GaN device with lower turn-off energy. Due to lower winding width, the SR is replaced with a BSZ0500NSI,

as it has a smaller package that can fit on the winding. Based on the output filter capacitor selection guideline proposed in Chapter 1, the 10µF capacitors are still the best choice for operation at 400 kHz, and hence are used in this converter. Moreover, based on the study in Chapter 2, the symmetrical shielding technique is employed in this woek.

Fig, 4.15 shows the operating waveforms at light load (10%) and at full load (1kW).

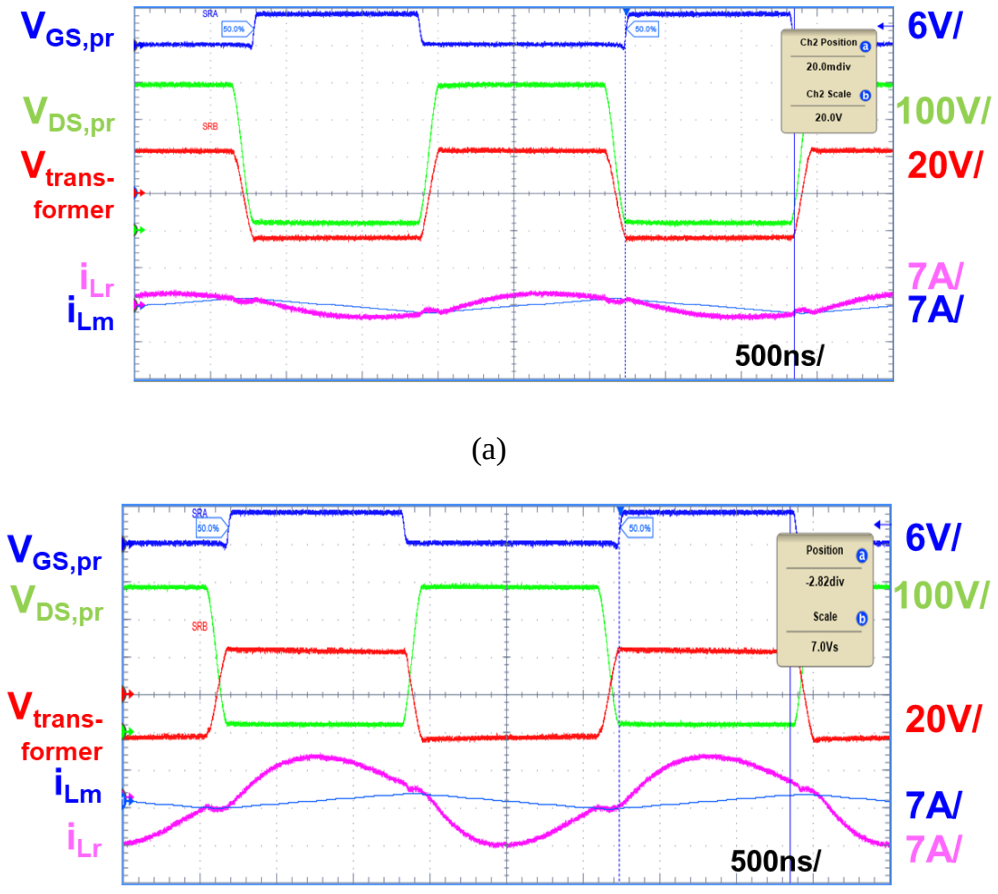


Fig. 4.15. 400V/12V LLC converter operating waveforms: (a) light load (10%, 100 W), and (b) full load (100%, 1 kW).

It can be observed that zero-voltage switching (ZVS) is achieved at both light load and full load. Moreover, there is no ringing in the secondary V_{DS} voltage due to minimum secondary leakage.

The thermal performance of the LLC converter running at full load (1kW) for around 2 minutes until thermal steady state is shown in Fig. 4.16. The converter is air-cooled with 400 linear feet per minute (LFM) from left to right. The maximum temperature on the converter is around 94 ^{0}C at the primary devices, with the SRs and transformer core showing maximum temperatures of 91 ^{0}C and 53 ^{0}C respectively.

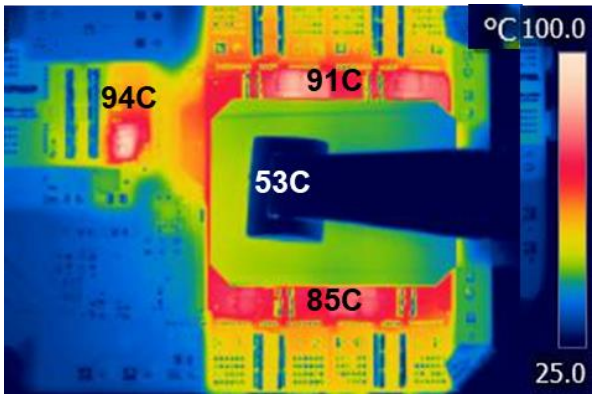
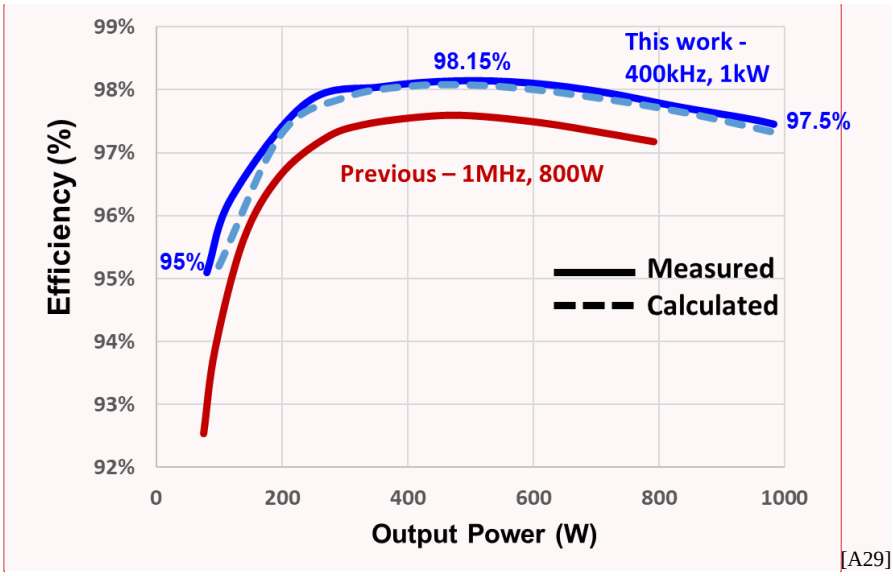


Fig. 4.16. Thermal performance of LLC converter.

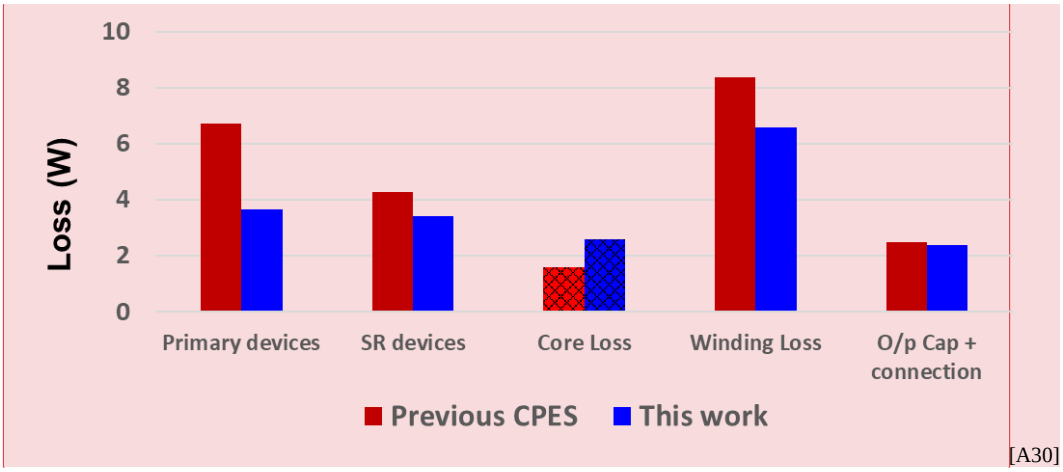
Fig. 4.17 shows the measured efficiencies of the converter, compared with that of the previous CPES converter. Moreover, the dashed efficiency curve shows the calculated efficiency, which follows the actual measurement closely, hence validating the accuracy of the frequency optimization model.



[A29]

Fig. 4.17. 400V/12V LLC converter efficiency.

The converter can achieve 95% light-load efficiency (10% load), 98.15% peak efficiency (at around 500W), and 97.5% at full load (1 kW). Due to better devices and lower switching losses at lower frequencies, the light-load efficiency increases by 2.4% despite an increase in the core loss. The peak- and full-load efficiencies also increase by 0.6% and 0.2%, respectively, due to the lower device conduction and transformer winding losses. This can be quantitatively observed from the converter loss breakdown comparison in Fig. 4.18.



[A30]

Fig. 4.18. Comparison of the converter loss breakdown at full load.

Therefore, the hardware results verify the performance improvement of the 1kW 400V/12V LLC converter operating at 400 kHz by illustrating that its efficiency and power density are higher than the previous CPES 800W 400V/12V LLC converter operating at 1 MHz.

4.5 Conclusions

In this chapter, the resonant frequency, at which the 400V/12V LLC converter switches exclusively, is optimized to improve the performance over the previous CPES 400V/12V LLC converter. The different components of the converter loss depend heavily on the switching frequency, and hence it is vital to optimize it to maximize the performance of the converter.

The selection of the best ferrite material for the transformer core at different frequencies is vital for minimizing the transformer loss. To achieve this, the core loss densities of different materials were measured, their performance factors were evaluated at a fixed core loss density as a function of frequency, and the materials with the highest performance factors were selected. To generalize the study to other applications with different core loss density values, the relative performance factors were shown to be similar at different core loss densities, too.

After selecting the core materials, the transformer loss was evaluated at different switching frequencies. The optimal copper weights for the primary and secondary PCB layers were calculated. For the primary layers, 3oz Cu is recommended for $f_s < 1MHz$ and 2oz Cu is recommended for $f_s \geq 1MHz$. For the secondary layers, 3oz Cu is recommended for all frequencies. The optimal transformer dimensions are selected based on the tradeoff between core loss and winding loss, and the minimum transformer loss at different transformer footprints are evaluated, where 1200 mm^2 is selected as the design region. Finally, the converter efficiency and the power densities at different frequencies are evaluated, where there is a tradeoff between the

two with changes in frequency. Upon studying the curve, 400 kHz – 800 kHz is recommended as the switching frequency design region.

To demonstrate the efficiency improvement, a 1kW 400V/12V LLC converter running at 400 kHz was built and tested. It is able to achieve 95% and 97.5% efficiencies at a light load and at a full load, respectively, while achieving a peak efficiency of 98.15%, all of which are higher than those of the previous CPES converter. Moreover, the power density was 940 W/in^3, also higher than the previous CPES power density, due to the higher-rated power, despite its higher transformer profile.

Chapter 5. Summary and Future Work

With the ever-increasing demand for internet services, the energy demand from datacenters is also rising exponentially. This is leading to improvements in datacenter power architectures, with the 400V-bus architecture showing the greatest promise for the future. This, however, requires stepping down 400 V directly to 12 V on the server motherboard, requiring high efficiency and power density from the 400V/12V DC-DC converter. CPES has done considerable work in this field, with the latest converter achieving 97.6% peak efficiency and 900 W/in^3. However, extensive research by other groups is closing the performance gap to the CPES converter, leading to the motivation of this thesis, which is improving the performance of the previous CPES 400V/12V LLC converter.

The second chapter studies the termination design of planar matrix transformers with center-tapped rectifiers. The SRs and output filter capacitors are placed on the secondary windings to minimize the termination inductance. However, the output filter capacitors are split between the top and bottom secondary layers, resulting in a long parallel path between the two. This parallel

loop has a parasitic inductance that resonates with the capacitance to cause a parallel resonance peak in the transformer's impedance curve. This parallel resonant frequency must be kept far away from the converter resonant frequency to minimize its impact on the transformer's AC resistance, and hence, converter efficiency. The chapter proposed a capacitance selection guideline to achieve this goal.

In addition to selecting a suitable capacitance, the loop inductance value itself can be minimized by optimizing the termination loop. If the loop inductance is sufficiently small, the parallel resonant frequency should be high enough to not impact the impedance at the switching frequency, irrespective of the capacitance. This will be investigated in the future.

Chapter 3 investigates the shielding technique in planar matrix transformers, which is crucial for minimizing the high CM noise. CPES previously proposed a shielding technique that uses half of the shielding turns as part of the primary windings in order to increase the turns ratio by 1, thereby reducing the primary-device conduction losses to offset the loss increase from adding two extra layers. However, upon studying the drain-source voltages of the SRs, current-sharing issues were detected, which were traced to the asymmetrical design of the shield and the position of the transformer airgap. The shield windings were made symmetrical by conducting all the shield windings in parallel, and by interleaving the two layers on the same elemental transformer. This resulted in a 0.25% converter efficiency improvement due to better current sharing in the two half-cycles of operation.

The transformer airgap location also affects leakage inductance, and hence the current sharing between the two secondary layers. The airgap can be moved to the center to make the leakage inductances symmetrical, but this induces eddy currents in the other windings due to their

proximity with the airgap, resulting in reduction in light-load efficiency. In the future, other possible solutions may be investigated to tackle this issue with minimum tradeoffs.

Chapter 4 discusses the switching frequency optimization for the LLC converter. First, the core loss densities of different materials were measured, their performance factors were evaluated at a fixed core loss density as a function of frequency, and the materials with the highest performance factors were selected. Based on this, the converter loss and the power densities were calculated at different frequencies, where there is a tradeoff between the two with changes in frequency. Upon studying the curve, 400 kHz – 800 kHz is recommended as the switching frequency design region.

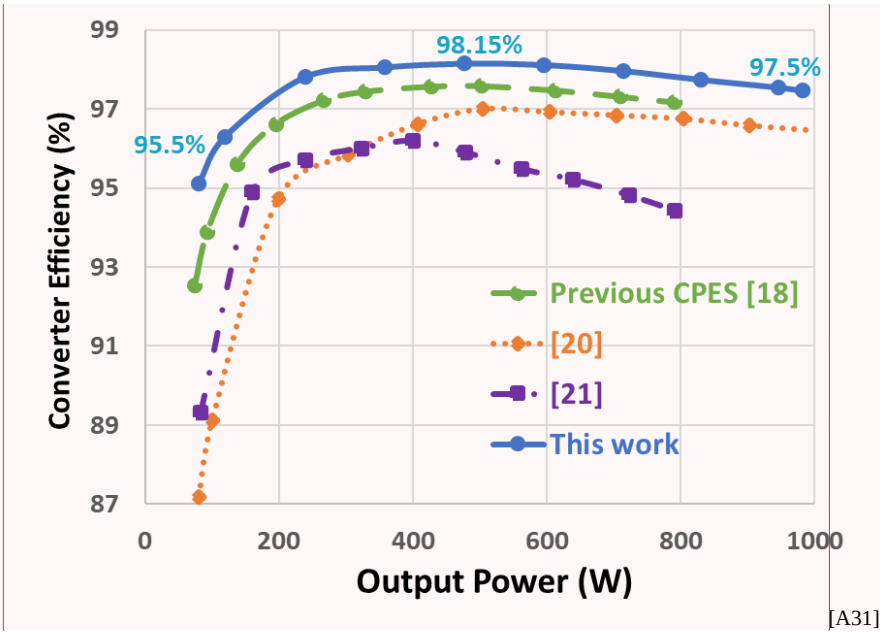
Combining the results from all the chapters, a 1 kW 400V/12V LLC converter operating at 400 kHz with symmetrical shielding and 10 µF output filter capacitors was developed. The performance of this converter can be updated from Table 1.3, resulting in Table 5.1.

Table 5.1. Updated performance summary of recent 400V/12V unregulated DC-DC converters.

ITEM	[18]	[20]	[21]	[22]	[23]	[24]	This Work
Rated Power (W)	800	1000	800	1800	800	1000	1000
Frequency (MHz)	1	1	1	1	1	1	0.4
Peak Efficiency (%)	97.6	97*	96.5*	98.3*	97.4	97.3	98.15
Power Density (W/in^3)	900	640**	900**	810	1177	-	940

* Without Driving Loss ** Without Controller

It can be observed that the performance of this work is exemplary as compared to the others described in this study. The efficiency comparisons with the previous CPES work and other works of similar power levels are shown in Fig. 5.1.



[A31]

Fig. 5.1. Converter efficiency comparison with other works.

The converter's power density can be further pushed if the rate power can be further pushed, while maintaining the same converter dimensions. However, the thermal performance needs to be further improved to achieve this end, as simply air-cooling is not sufficient to safely run the converter at higher loads. This is an interesting topic for future work.

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