


Radio Frequency Power Amplifiers for
Portable Communication Systems

by

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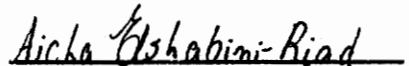
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ABSTRACT

Portable communication systems require, in part, high-efficiency radio frequency power amplifiers (RF PA) if battery lifetime is to be conserved. Conventional amplifier classifications and definitions are presented in a unified and concise format. The Bipolar Junction Transistor (BJT) and Metal-Semiconductor Field Effect Transistor (MESFET) are evaluated as active devices in high-efficiency RF PA designs. Two amplifier classes (class CE and class F) meet the system requirements of an 850 MHz operating frequency, a power output of 3 W, a battery supply voltage of 9 Vdc, and a sinusoidal-type signal to be amplified. Both classes are evaluated through recent research literature and simulated using the PSpice[®] computer simulation program. Class CE and class F are found to provide efficiencies exceeding 80 percent under the given system constraints.

ACKNOWLEDGMENT

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CHAPTER 1

1.0 INTRODUCTION

The current number of subscribers to cellular telephone services in the U.S. exceeds 3.5 million and is expected to double by the end of 1994. In addition, demands for increased capacity of portable communication systems are expected to grow substantially over the next several years. The Advanced Mobile Phone Service (AMPS) has been available since 1983 and offers analog FM for voice communications and, as of 1991, a newly adopted dual-mode cellular system known as IS-54 offers digital services in addition to AMPS capabilities [Schneiderman, 1991; Lee, 1991].

Even though services and capabilities are expanding, users of portable units continue to face a limitation of battery lifetime, which ultimately determines the amount of time the unit can be operated, or "talk time". Users generally cannot control the output power of their unit; the cellular system (or cell site) automatically and continuously adjusts the output power of each subscriber's unit in order to minimize interference between users. A simple means of increasing battery lifetime is to increase its ampere-hour capacity. Unfortunately, apart from research aimed at developing improved battery designs, the increased ampere-hour capacity brings about an undesirable increase in the weight of the unit. Since users prefer portable units that are small in size and light in weight, an alternative must be found. Clearly, if "talk time" is to be increased for a given battery capacity, then an obvious alternative is to reduce the power required by the electronics of the unit. A particular group of these electronic circuits, radio frequency power amplifiers (RF PA), is the topic of interest for this study.

The majority of power consumption within a transmitter is usually assigned to the RF power amplifier. The PA is the circuit that typically contains the higher voltages and currents necessary to produce sufficient output power for reliable transmission. Thus, if the efficiency of an amplifier can be increased, power consumption will decrease and battery lifetime will increase. A working definition of efficiency is the ratio of signal power output to the dc input power required to produce that output. An added benefit of increasing amplifier efficiency is a reduction of device power dissipation and corresponding heat generation. Therefore, a smaller heat sink may be used, which reduces unit size and weight even further. Also, lower device temperatures translate directly into improved device reliability. For these reasons, high-efficiency power amplifiers are an important part of portable unit design [Sokal and Sokal, 1975].

1.1 PURPOSE OF PROJECT

The intent of the research to be reported in this thesis is three-fold: to present a unified collection of present-day ideal amplifier classifications and their definitions, to examine practical considerations that affect ideal amplifier operation, and to evaluate high-efficiency power amplifier designs for possible use in portable cellular telephone units.

Both bipolar junction transistors (BJT) and field effect transistors (FET) will be considered for use as the active device. For the specific application of portable telephone units, the system constraints placed on the amplifier design are:

1. an operating frequency of 850 MHz,
2. a voltage supply obtained from a 9 Vdc battery,
3. a peak power output of 3 W (approximately 35 dBm), and
4. a sinusoidal signal to be amplified, using either frequency modulation (FM) or pi/4 differential quadrature phase shift keying (DQPSK).

1.2 OVERVIEW

Amplifiers are classified according to the operating regions of the device and/or associated input and output networks. Chapter 2 contains general definitions of ideal amplifier classes along with qualitative discussion of circuit operation. The role of the active device (as a current source, switch, or a combination of the two) is discussed for each class.

Practical considerations that affect amplifier operation will be examined in Chapter 3. Actual operation of an amplifier differs from the ideal operation due to the effects of device limitations (e.g., saturation voltage and resistance, transition time, drive requirements, etc.) and non-ideal circuit components (stray inductance and/or capacitance, resistance, and leakage current). Each class will be revisited in light of these limitations, with an emphasis on amplifier efficiency.

Chapter 4 contains a more detailed description of the BJT and FET devices used as the active device in power amplifier designs. The system constraints mentioned previously in this chapter will be used to aid in the selection of the device(s) and amplifier class(es) for this particular application.

Chapter 5 will discuss design considerations related to the selected device(s) and amplifier class(es). Each selected class will be examined in greater detail through the use of design examples found in literature and computer simulations.

Finally, concluding remarks will be offered in Chapter 6. Topics for future work related to this research will be briefly discussed.

CHAPTER 2

2.0 CONVENTIONAL AMPLIFIER CLASSIFICATIONS

The following paragraphs contain general and ideal definitions of various classes of amplifiers. The majority of this information is available in *Solid State Engineering* by Krauss, Bostian, and Raab [1980]; additional sources are cited where applicable. Discussion of device or circuit operation is carried out from a qualitative standpoint only. Ideal characteristics are mentioned without detailed explanations; these characteristics will be dealt with in a subsequent chapter on practical considerations. The types of signals that are commonly amplified by each class will also be stated.

Table 2.1 shows a convenient, if somewhat arbitrary, listing of amplifier classes by category. In practice, some of these categories may overlap to some degree, i.e., a linear amplifier may be designed with a tuned output for narrowband operation. This table is provided to assist the reader in formulating a general distinction between the different types of amplifiers.

Table 2.1 Types of Amplifiers by Category

Linear	Classes A, B, and AB
Tuned Output	Class C, Saturating Class C
Switch-mode	Classes D, E, and S
Waveshaping	Class F
Multiple Power Supply	Classes G and H

2.1 CLASS A

The class A amplifier (Figure 2.1) is used whenever a faithful reproduction of the input signal is required. Of all amplifier designs to be discussed in this study, class A provides the greatest degree of linearity but the lowest level of efficiency. The active device is typically employed as a current source, and the bias operating point is chosen such that output RF current flows continuously, even under quiescent (no input signal) conditions¹. A variation on this theme adapts the bias to the drive level, using base charge storage in a BJT above the β -cutoff frequency, while maintaining nearly class A operation [Overstreet, 1986]. As shown in Figure 2.2, the device never reaches saturation or cutoff. Maximum theoretical efficiency is 50 percent at maximum power output. Efficiency is reduced at power levels less than the designed maximum. The source (input) and load (output) networks are not considered part of the amplifier design. Harmonic generation and intermodulation distortion (IMD) are usually considered negligible, but filter networks at the output may be used to lower harmonic content even further. Types of signals usually requiring class A amplifiers are analog amplitude-modulated signals such as amplitude modulation (AM) and single-sideband (SSB) and digital signals that are amplitude-modulated such as quadrature amplitude modulation (QAM). Due to its low efficiency, class A amplifiers are typically used as low-level drivers [Hardy, 1979; Hakim and Barret, 1964].

¹This amplifier is said to be operating with a conduction angle of $\gamma = 360^\circ$. Conduction angle is defined to be that portion of a cycle for which the output current flows due to an input signal.

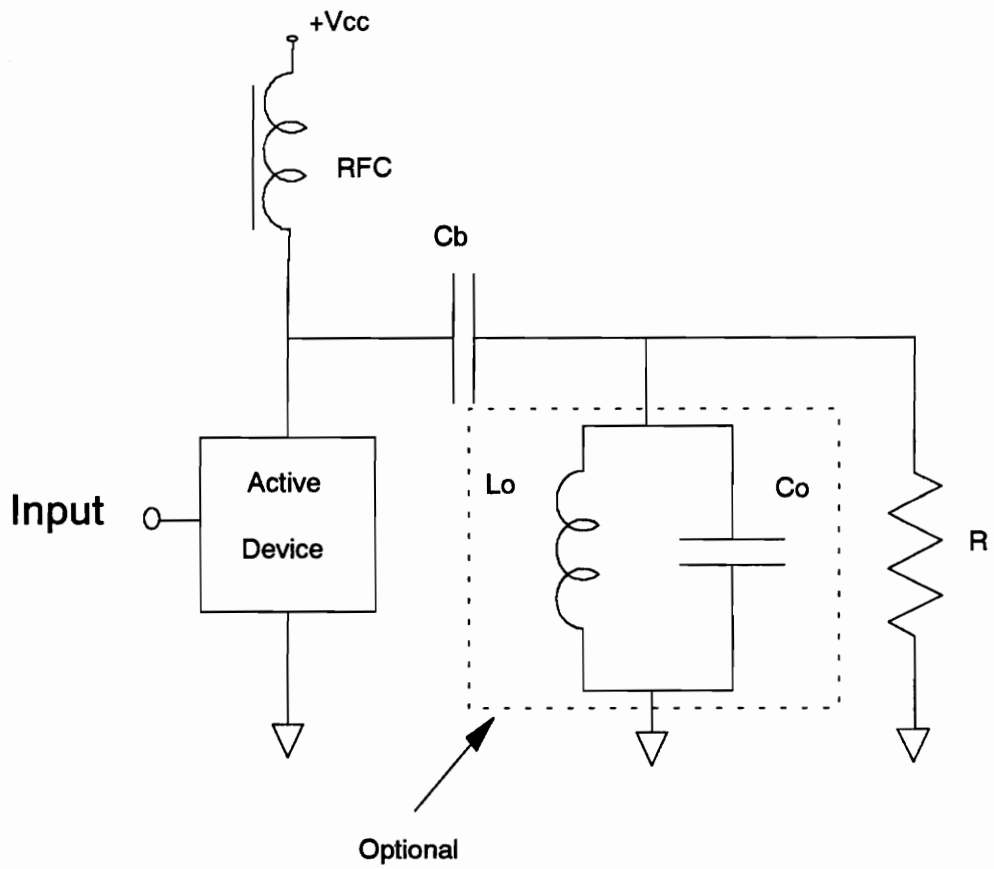


Figure 2.1 Circuit Configuration for classes A, B, and AB

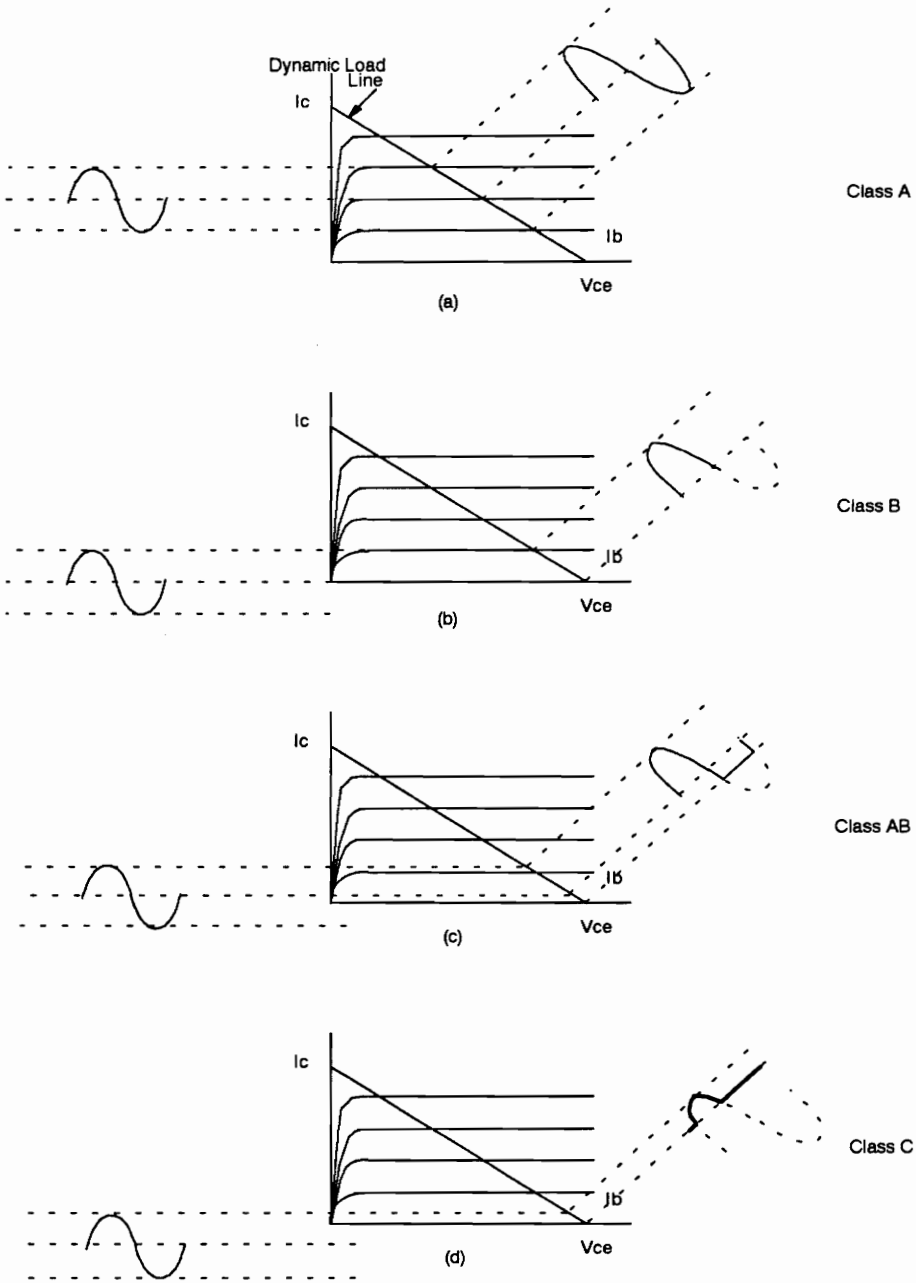


Figure 2.2 Input/Output Characteristics of Classes A, B, AB, and C

2.2 CLASS B

The class B amplifier (Figure 2.1) differs from the class A in the choice of the operating bias point. In practice, the class B amplifier is often configured in a push-pull arrangement and thus will contain two active devices instead of a single device which is typically found in a single-ended class A amplifier. Device operation is still that of a current source, but the bias is such that the output current flows for only half of the input signal; thus, the conduction angle $\gamma = 180^\circ$ (see Figure 2.2). Subsequently, linearity is reduced and harmonic generation and intermodulation distortion levels are increased. Even though output filters are typically used to reduce harmonic content, the input and output networks are still not considered part of the basic amplifier design. As with class A, the amplifier is designed to prevent the active device from entering the nonlinear region of operation. Maximum theoretical efficiency is increased to 78.5 percent at maximum power output. Increased efficiency over class A is due to operating the device at cutoff, thus reducing DC power dissipation over half of the input cycle. If device current does not flow for a certain period of time, then the current-voltage product, or power dissipated, is essentially zero; thus, efficiency is increased. However, power delivered to the load must necessarily decrease. The power output at the fundamental frequency decreases because more power is assigned to the generated harmonic frequencies. AM and SSB signals can still be amplified with class B if increased distortion (due to harmonic generation) can be tolerated; amplification is still considered linear. Near linear performance may be obtained by using the push-pull configuration.

2.3 CLASS AB

The class AB amplifier (again as Figure 2.1) is a compromise between class A and class B in terms of efficiency and linearity. The bias point is chosen slightly above cutoff such that output current flows for more than half a cycle but less than a full cycle of the input signal ($180^\circ < \gamma < 360^\circ$) as shown in Figure 2.2. A small amount of output current flows under quiescent conditions to compensate for the turn-on process of the device, resulting in a reduction of linear distortion often found in practical class B amplifiers. Thus, linearity is slightly increased compared to class B, but efficiency must necessarily decrease. Maximum efficiency and distortion (due to harmonic generation) lies between that of class A and class B depending upon the operating bias point [Hardy, 1979; Hakim and Barret, 1964].

2.4 TRUE CLASS C

The class C amplifier (Figure 2.3) differs from class A and class B in terms of operating bias and the output network. Note that the tuned output network is now required instead of being optional as with classes A, B, and AB. The device is employed as a current source as in class A and B, but the bias is chosen such that typically much less than half of the input signal brings the device into conduction, and thus output current would flow for less than 180 degrees ($0^\circ < \gamma < 180^\circ$) as shown in Figure 2.2. The output waveform suffers from a high level of nonlinearity and subsequent harmonic and intermodulation distortion. A parallel output network tuned to the fundamental frequency is used to shunt all harmonics to ground while forcing the fundamental frequency to the load.

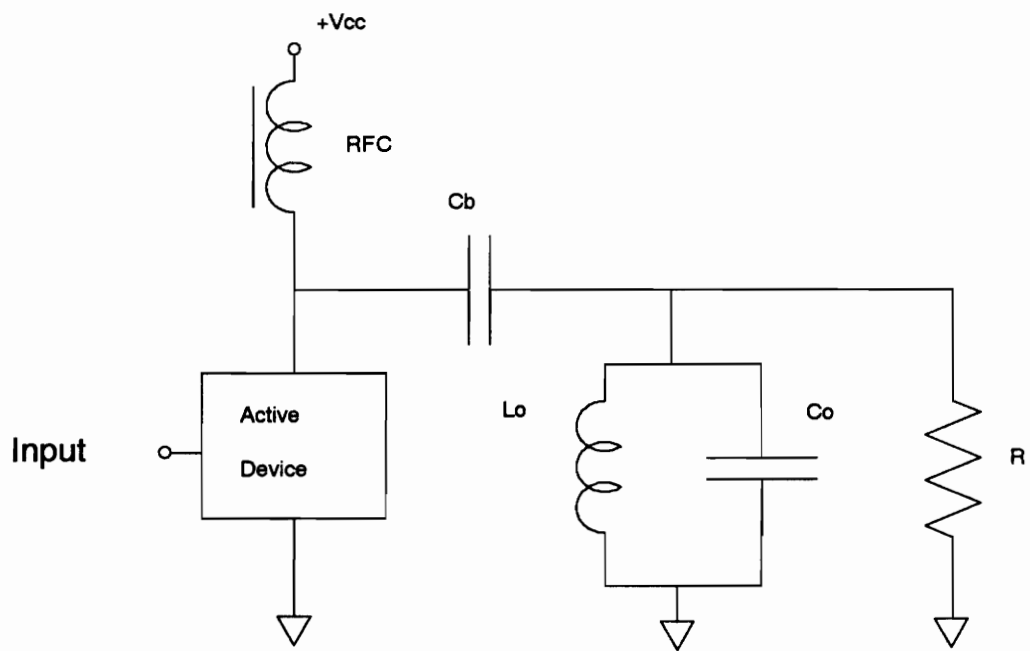


Figure 2.3 Circuit Configuration for Class C

Maximum theoretical efficiency of this amplifier can approach 100 percent by limiting device conduction, although as the conduction angle approaches zero, so does the output power. A very narrow input pulse of high amplitude could be used to increase power output, but since amplitude must necessarily be limited by power supply capabilities, so must the output power. Class C amplifiers with efficiencies on the order of 90 percent are not uncommon. While the frequency of the input signal is preserved at the output, the amplitude information is not. Continuous wave (CW) modulation and FM are two types of signals that utilize class C amplifiers because it is the presence and frequency, respectively, that carry the information and not the amplitude [Hardy, 1979].

2.5 SATURATING CLASS C

If a class C amplifier is driven hard enough so that it just enters saturation, the output RF voltage amplitude will depend largely upon the supply voltage and will be relatively insensitive to variations in the input drive level. For this reason, a saturating class C amplifier is often used as a modulator for AM by varying the supply voltage². Slight increases in efficiency and power output over a non-saturating class C are possible, but both efficiency and power output decrease once the saturation point is exceeded. Thus, maintaining the proper drive level is important if efficiency and power output are a concern. More harmonics are generated due to the nonlinearity inherent in a saturated device, but a parallel output network that is tuned to the fundamental frequency shunts much of the harmonic content to ground and forces the fundamental to the load. Due to

²It should be noted that when an amplifier is used as an amplitude modulator, the efficiency limitations are transferred to the modulation driver which is required to vary the supply voltage level. This is true of all modulators [Davis, 1992].

the minimal increase in efficiency and power over a true class C amplifier, saturating class C is typically used only when a modulator is desired.

2.6 CLASS D

As mentioned in the discussion on class B amplifiers, whenever the product of voltage across the device and current through the device can be minimized, power dissipated by the device is also minimized. The Sokals [1975] offer a concise summary of the conditions for minimal power dissipation by an active device:

1. minimize the voltage across the device when current flows through it,
2. minimize the current through the device when voltage exists across it,
and
3. minimize the duration of any unavoidable condition in which appreciable current and voltage exist simultaneously.

Class C has been shown to use conditions 1 and 2. Amplifiers using devices as switches are designed to include the third condition as well. The class D approach is one such amplifier.

The class D amplifier (Figure 2.4) uses a switch-mode technique in which at least two devices are arranged in a push-pull configuration, with an input signal forcing each device alternately between saturation and cutoff with a 50 percent duty cycle [Sokal and Sokal, 1975]. A tuned output network (i.e., bandpass filter) forces the fundamental sinewave signal to the load. Since the devices are acting as switches, the amplitude of the RF output voltage varies directly with the supply voltage, allowing the class D amplifier to

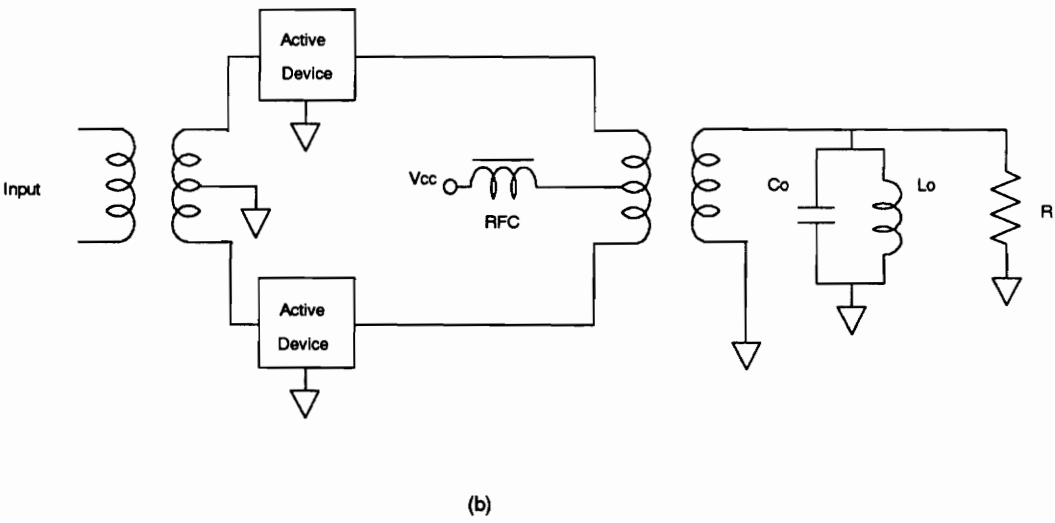
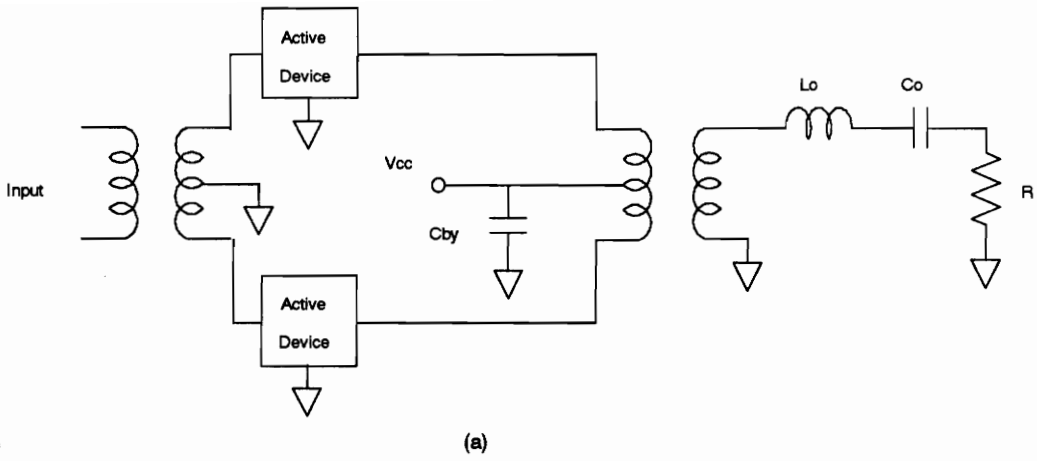


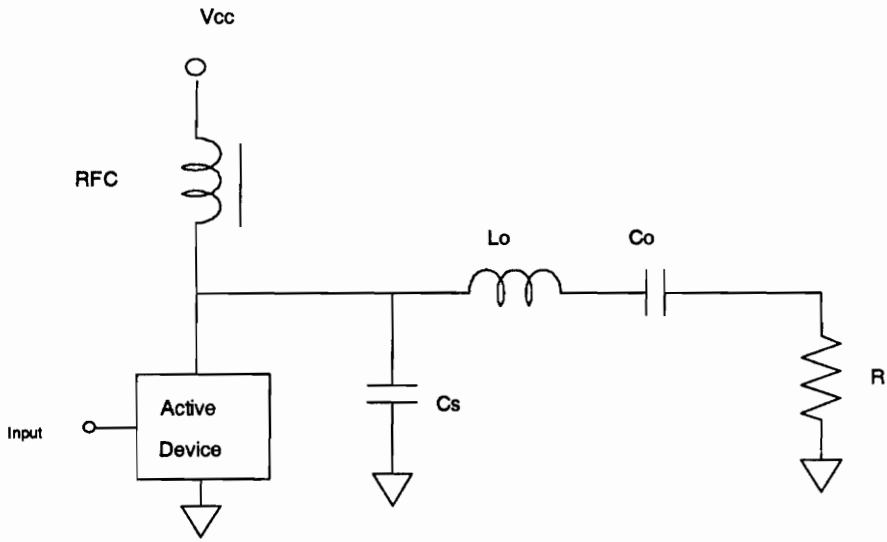
Figure 2.4 Circuit Configuration for Class D: Voltage-Switching (a) and Current-Switching (b)

be operated as an AM modulator. Maximum theoretical efficiency is 100 percent. (Recall, efficiency limitations are transferred to the modulation circuitry).

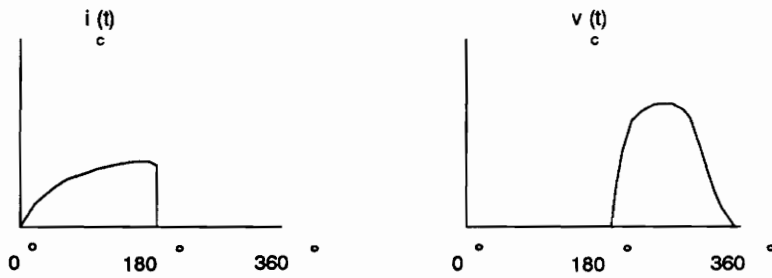
The advantages of class D over class C are lower harmonic distortion (due to a push-pull device arrangement with inherent second-order harmonic cancellation), wider bandwidth (since the first generated harmonic is third-order), and increased efficiency without decreased output power. As the frequency of operation increases, however, switching losses begin to reduce both efficiency and power output [Chudobiak and Page, 1969]. These and other losses will be reviewed in Chapter 4.

2.7 CLASS E

The class E amplifier (Figure 2.5) is a single-ended amplifier where the device acts as a single-pole switch. The load network becomes an important part of the basic design, and it provides the major difference between class E and other switch-mode amplifiers. The load network of the class D amplifier simply chooses the fundamental frequency component of the output signal. The load network of the class E amplifier is designed to accomplish three objectives: 1) delay the rise of the voltage across the device at turn-off until the device is fully off, 2) bring the collector voltage to zero when the device turns on, and 3) ensure that the slope of the collector voltage is zero at device turn-on. These objectives are achieved via the transient response of the network [Sokal and Sokal, 1975; Raab, 1978]. An example of the device output waveforms is shown in Figure 2.5. Objectives 1 and 2 are the basis for the high efficiency -- the voltage-current product is minimized. The third objective is provided in order to allow for slight timing errors (overlap of current and voltage waveforms) [Herman and Zulinski, 1990]. Thus, class E operation is defined by a combination of the active device when it is on and the transient



(a)



(b)

Figure 2.5 Circuit Configuration for Class E (a) and Device Current and Voltage Output Waveforms (b)

response of the output network when the device is off [Raab, 1977]. The output network is designed such that even if the transistor switching time is a large fraction of the input cycle time, the transient response, due to the objectives mentioned above, will maximize the power efficiency. Maximum theoretical efficiency is 100 percent, though obviously limited in practice by the loading circuit.

Although this amplifier can be used for AM modulation by varying the collector supply voltage, the class E PA is often used with FM and CW modulation because the frequency and phase track well with the input signal. With proper filtering, the class E amplifier can be operated over an octave bandwidth with greater than 95% efficiency. The Sokals [1975] state that the advantages of class E are: 1) high efficiency, 2) the ability to design the amplifier without having to "cut-and-try", 3) large reduction of second-breakdown stress³, 4) low sensitivity to the active device characteristics, and 5) potential for higher frequency of operation than conventional class D operation. Like the class D amplifier, however, class E is subject to device switching limitations which ultimately limit the maximum operating frequency.

2.8 CLASS F

From the study of Fourier series, it is well known that any periodic function, such as a square wave, may be represented as a sum of sinewaves. Therefore, by adding specific sinusoidal harmonics to the fundamental frequency sinusoid, that fundamental waveform at the collector would begin to resemble a rectangular waveshape. The

³Second breakdown is a device condition that exists when high collector currents (for a BJT) create a local "hot spot" within the device, giving rise to a thermally-induced current generation known as avalanche breakdown. This condition is potentially destructive to the device [Kovacs, 1981].

required harmonics are present in the device output waveforms, and they are reflected back into the device by resonator circuits contained within the load network. In effect, the device output waveform has been shaped by the external load network. This is the essence of a class F amplifier.

The class F amplifier (Figure 2.6) is essentially a dc-biased class B or class C amplifier with an output network resonant at one or more harmonics in addition to the fundamental frequency. The active device functions as a current source which may or may not enter saturation. The role of the resonator is to add harmonics (theoretically sinewaves) to the collector voltage waveform in such a way as to cause a flattening, or "squaring-up", of the waveform. This action serves to minimize the voltage-current product and thus reduce power dissipation [Raab, 1976; Raab, 1977]. The resonator is designed to pass only the carrier frequency to the output load. Maximum theoretical efficiency depends upon the type of output network used. If even harmonics are shorted to ground and odd harmonics are forced back into the collector waveform, a perfect rectangular waveshape is formed, the device acts as a switch, and theoretical efficiency is 100 percent. In theory, this can be accomplished by using a 1/4 wave transmission line structure as the resonant circuit. In practice, usually only the second and third harmonics are considered. The reason for this practice is the primary drawback to designing class F amplifiers: the resonator network must be designed to match device impedances at the fundamental frequency and each harmonic frequency being considered. As the frequency of operation increases, accurate knowledge of the device impedances at the harmonic frequencies becomes increasingly difficult to obtain. Nonetheless, class F designs are being used at high frequencies, and efficiencies for designs using only second-harmonic resonators are on the order of 88 percent [Raab, 1976; Krauss et al., 1980; Kopp and Pritchett, 1989; Khatibzadeh and Tserng, 1990; Hall and Trew, 1991].

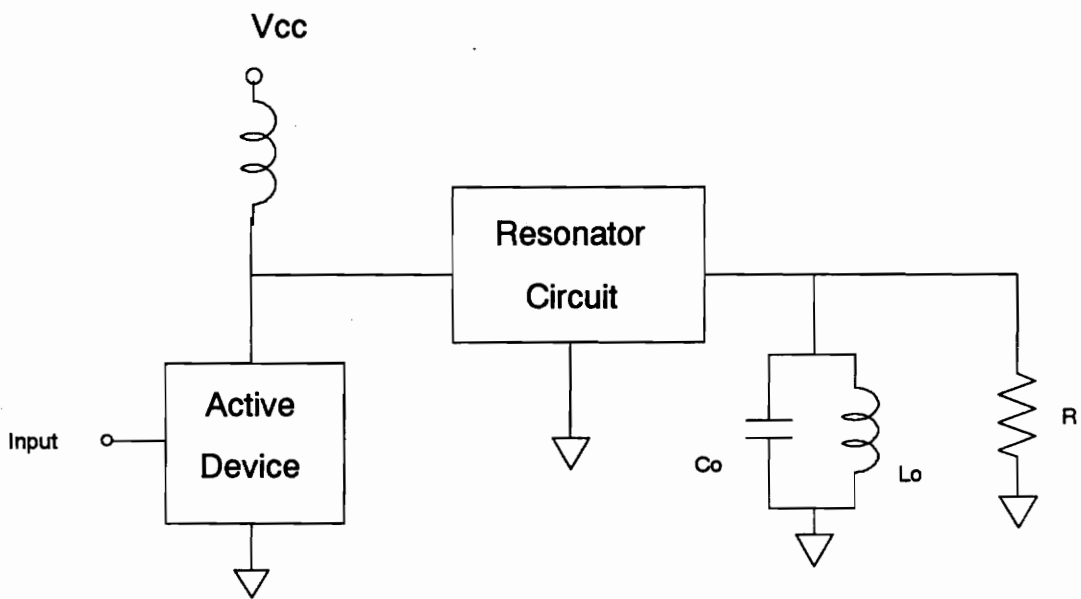


Figure 2.6 Circuit Configuration for Class F

2.9 CLASS G

The class G amplifier (Figure 2.7) is the first of two PA's to be discussed which uses multiple power supplies. The premise behind increased efficiency is that power dissipation is reduced for lower supply voltages (i.e., low voltage-current product). Therefore, if the input signal is low-level, there is no need to have a high supply voltage and thus high power dissipation and low efficiency. Developed by Hitachi for audio applications, the class G amplifier is designed to operate efficiently over the lower power levels where the majority of music power exists (this is true of speech as well). In practice, using the class G amplifier in a portable transmitter would require the use of multiple batteries in order to obtain the multiple power supply voltage levels. Otherwise, losses would occur in the circuitry to provide the multiple supplies, and overall system efficiency would be reduced.

As mentioned previously in this chapter, the conventional class B amplifier is most efficient when operated at its maximum rated power. When operated at lower power levels, the class B amplifier may be less than 20 percent efficient. The class G PA overcomes this problem by using a two-level power supply system, one for each of the two devices (biased near class B). A low level input causes active device #1 to conduct as a current source using the lower voltage supply, while device #2 remains off. Assuming no losses in the power supply, efficiency is two times higher than if both devices were on. A higher level input signal brings the second device into conduction and the higher voltage supply into use. The two devices are chosen to work over their most efficient power output range. The ratio of the two supplies affects both efficiency and device power dissipation. Although no theoretical efficiencies were found in the literature, measured efficiencies average better than 60 percent, compared to approximately 40 percent for class B at the same output level [Feldman, 1976]. A primary limitation is that the

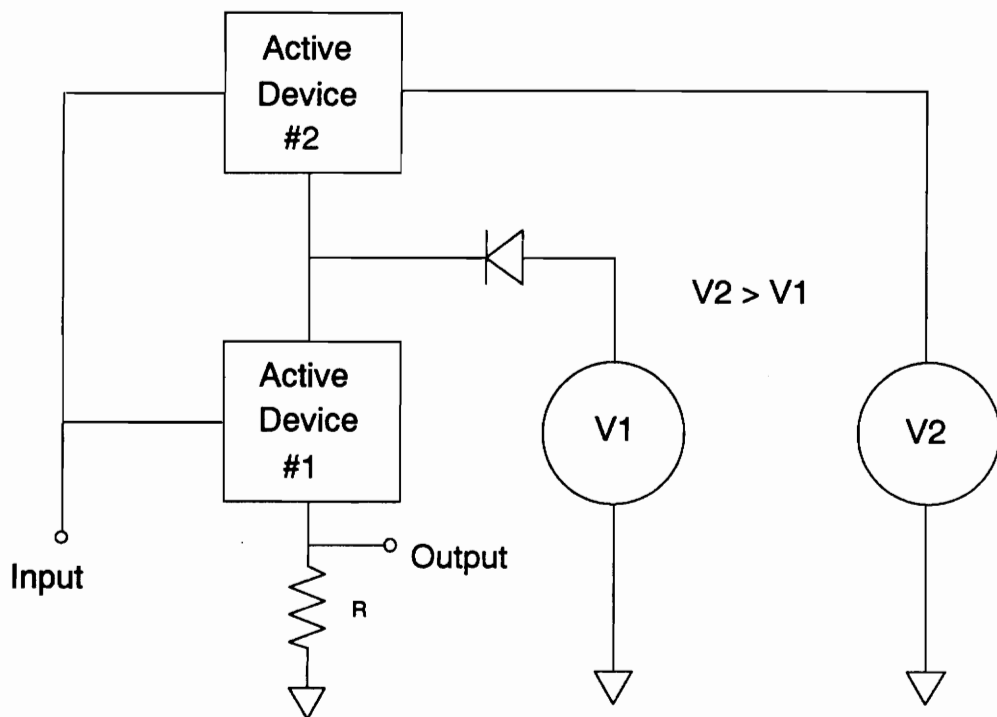


Figure 2.7 Circuit Configuration for Class G

transition of switching from one device to the next occurs when the current through the device is non zero. Thus, as the signal frequency becomes an appreciable portion of the transistor switching frequency, losses associated with this transition also increase [Feldman, 1976; Raab, 1986].

2.10 CLASS H

The second multiple supply design is the class H amplifier (Figure 2.8), requiring positive and negative voltage supply levels. Whereas the class G amplifier uses two supply levels that are fixed, the upper supply voltage level of the class H amplifier is made variable by the use of a *vari-proportional logic control*. The role of this control is to vary the supply voltage at the collector such that its level stays just above that of the collector voltage waveform. In this way, the supply level (and thus device dissipation) is kept low until more voltage is required at the collector due to an increased input signal level. An example of this action is shown in Figure 2.8. At low signal levels, the class H works like a class AB amplifier. As the signal level increases, the vari-proportional logic control anticipates the change in the output due to the increasing input signal. It then changes (at a rate faster than the input) to increase the voltage supply in order to add headroom and prevent distortion.

The predominant advantage of the class H technique over other switching schemes is that distortion of the signal is not increased by the changing supply level. Effectively, the signal never "sees" the changing supply level; all changes that are required come from within the power supply, outside of the amplifier signal path. An inherent limitation,

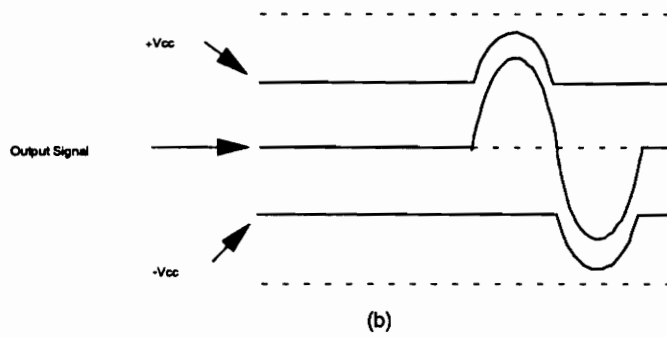
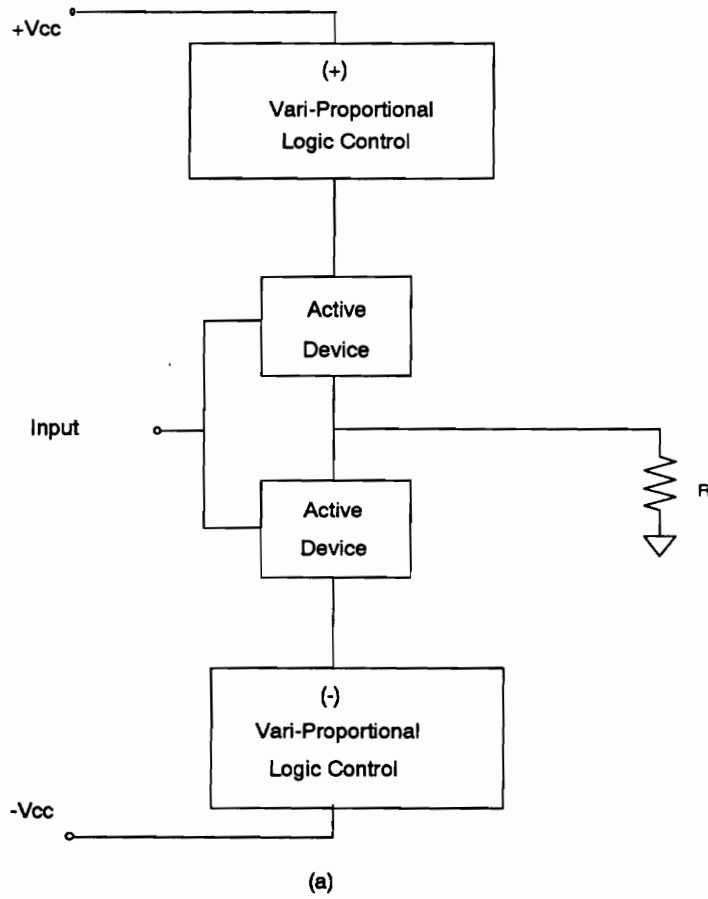


Figure 2.8 Circuit Configuration for Class H (a) and Power Supply Tracking (b)

however, is the ability of the power supply to change the voltage level faster than the signal rate. As the operating frequency increases, the power supply may not be able to maintain its ability to follow the signal [Feldman, 1977]. The inherent efficiency gains are traded to the power supply losses. This limitation will be addressed in the next chapter.

2.11 CLASS S

The class S amplifier (Figure 2.9) is the last of the amplifiers to be discussed which uses the switch-mode technique. Class S is similar to class D in that two switching devices are arranged in a push-pull configuration with an output network designed to choose the fundamental frequency [Raab, 1977]. Instead of a bandpass filter, however, class S uses a low-pass filter containing a series inductor to attenuate the switching frequencies and associated harmonics at the output while enhancing harmonics at the collector. Therefore, the load sees only the average value of the switched device output pulse. The desired output signal can be obtained by controlling the pulse width (duty cycle) of the input signal, and for this reason, class S amplifiers require pulse-width modulation (PWM) circuitry to drive the amplifier.

The class S power amplifier can be used as an amplifier if two devices are used, or as a modulator if one device is used. With two devices, the output voltage may be positive or negative. When used as a modulator, the output voltage can only be positive (assuming a positive V_{CC}). As with the class D amplifier, maximum theoretical efficiency is 100 percent. Recall once more that a modulator requires a modulation driver, and as such, overall system efficiency will be reduced by requiring this driver circuitry in addition to the PWM circuitry. Also, switching limitations serve to reduce power output and efficiency, as well as limit the maximum frequency of operation.

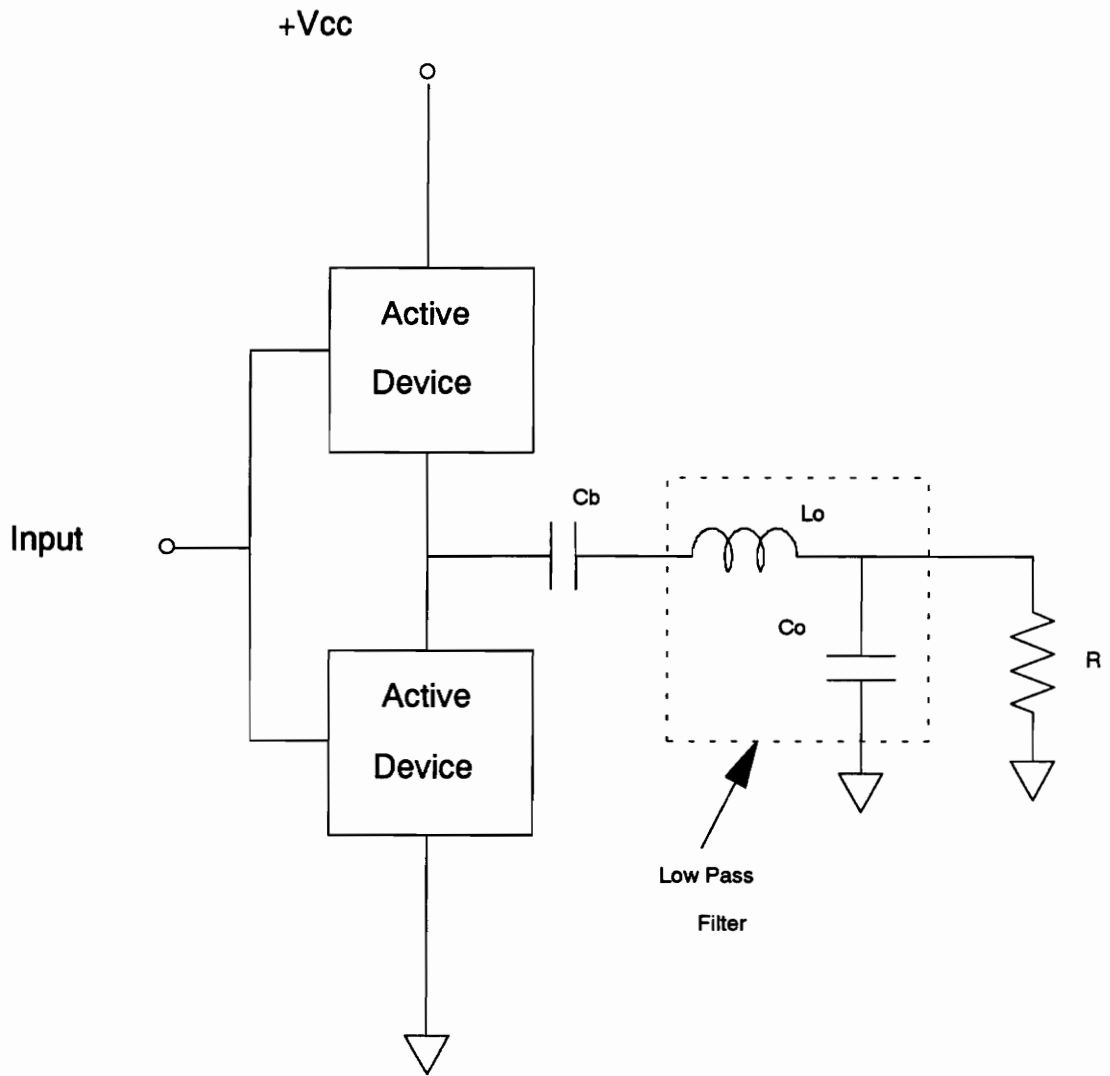


Figure 2.9 Circuit Configuration for Class S

CHAPTER 3

3.0 PRACTICAL CONSIDERATIONS

The description of amplifiers discussed thus far has dealt with ideal devices and components. Actual devices, however, suffer from a number of limitations that influence amplifier operation and ultimately reduce amplifier efficiency. The limiting factors that will be examined in this chapter include saturation voltage, saturation resistance, transition time, drive requirements, shunt capacitance and series inductance, reactive loads, output circuit Q , and intermodulation distortion. Some factors predominantly affect switch-mode amplifiers (e.g., transition time) while other factors are common to both switching and non-switching amplifiers. Also, a distinction will be made between BJTs and FETs when the factors affect the devices differently.

In addition to device-related limitations, other circuit components (resistors, capacitors, inductors, packaging, etc.) suffer from the effects of stray inductance and/or capacitance, resistance, and leakage current. These effects have an influence on transition time, drive requirements, circuit resonances, and output circuit Q .

This chapter will close with the examination of the ideal classes of amplifiers as they are affected by the limiting factors mentioned above. Pertinent compromises of the ideal classes will be addressed. As a result of these compromises, a mixed class will be introduced.

3.1 LIMITING FACTORS

Since amplifier efficiency is the primary focus of this study, it is necessary to define the ways in which efficiency is reduced by each of the limitations. As defined in Chapter 1, efficiency is the ratio of output signal power to dc input power required to produce that output. Therefore, efficiency can be reduced by having a reduction in output power for a given dc input power from the battery or supply modulator, or requiring an increase in dc input power to produce a given output power, or some combination of the two. Since power is the product of current and voltage, a reduction of current and/or voltage at the output results in a reduction of output power and efficiency.

As with the ideal amplifier descriptions in Chapter 2, the majority of the information found in these sections can be obtained in *Solid State Radio Engineering* by Krauss, Bostian, and Raab [1980]. Additional sources are cited where applicable.

3.1.1 SATURATION VOLTAGE

Saturation voltage (V_{sat}) for a BJT is defined as the collector-to-emitter voltage during device saturation. When operated at relatively low frequencies and currents, BJTs exhibit a saturation voltage with a magnitude of 50 mV to 300 mV. V_{sat} is dependent upon frequency and current, however, and may increase to 1 or 2 V at higher frequencies and currents. The frequency dependence is related to the time required to discharge the device capacitance, and is thus a function of device geometry. The current dependence is related to the resistance caused by a heavily conducting device. This resistance is sometimes referred to as the saturation resistance for a BJT. For amplifiers designed as non-saturating current sources, saturation voltage affects the operation by limiting the maximum collector output voltage swing to an effective voltage $V_{\text{eff}} = V_{\text{cc}} - V_{\text{sat}}$. Since

collector voltage swing is reduced, the output power and amplifier efficiency are also reduced. For saturating or switch-mode amplifiers, saturation voltage does not allow the voltage across the device to go to zero during current conduction. The resultant voltage-current product causes an increase in power dissipation and a reduction in efficiency [Kovacs, 1981; Horowitz and Hill, 1989].

3.1.2 SATURATION RESISTANCE

Saturation resistance for FETs is sometimes referred to as the "on" resistance (R_{ON}). Saturation occurs when the minimum drain voltage V_{dm} is equal to the product of drain current and saturation resistance. Since R_{ON} is usually in series with the load, any voltage dropped across the device is unavailable to the load. Thus, the output power is reduced, accompanied by a corresponding reduction in efficiency. Similar to the case with BJTs, saturation resistance of FETs in switch-mode amplifiers causes a simultaneous voltage-current product to exist, and both output power and efficiency decrease.

3.1.3 TRANSITION TIME

Unlike an ideal switching device, real devices cannot switch between cutoff and saturation instantaneously. Transition losses reduce efficiency of switch-mode amplifiers by allowing a simultaneous voltage-current product to exist, with subsequent power dissipation within the device. Transition time is determined by the time delay experienced while device input and output capacitances are being charged (rise and fall times), and by the time delay associated with the device conduction area being swept clean of excess charge carriers due to saturation (charge storage). In between the cutoff and saturation states of a switching device, the device is in the active state and may dissipate considerable power. Therefore, for switch-mode amplifiers, devices with fast rise/fall times are

desirable in order to reduce this loss. The type and shape of the drive signal used also affects the transition time, and is often optimized to reduce the charge storage effect [Chudobiak and Page, 1969].

3.1.4 DRIVE REQUIREMENTS

In addition to any necessary impedance matching, design of an amplifier input network requires knowledge of the drive signal required (voltage or current) and its waveshape. Because the input of an FET is largely capacitive, and therefore does not draw appreciable current, voltage drive is used and drive requirements are not usually a primary concern. On the other hand, BJTs will draw current at the input and may use either voltage or current drive, although current drive is often used for linear amplifiers. The reason for the use of current drive may be seen by the voltage and current relationships at the input and output of the BJT. The relationship between the collector current and base-emitter voltage is exponential, and the relationship between input base current and base-emitter voltage is logarithmic; thus, current drive nearly cancels these two effects, resulting in a relatively linear relationship between input current and output current. The amount of current required is inversely proportional to input impedance.

Sinewave, square wave, or complex drive waveforms may be used, depending upon whether the device is acting as a current source, switch, or some combination thereof. One example of a complex drive waveform (Figure 3.1) is a rectangular waveform with a large magnitude pulse on the leading edge of the positive and negative portions of the drive signal. The purpose of this pulse is to force carriers quickly into or out of the conduction region in order to reduce transition times. In a practical drive waveform, the pulse could not have perfectly "squared" edges; the pulse on the leading

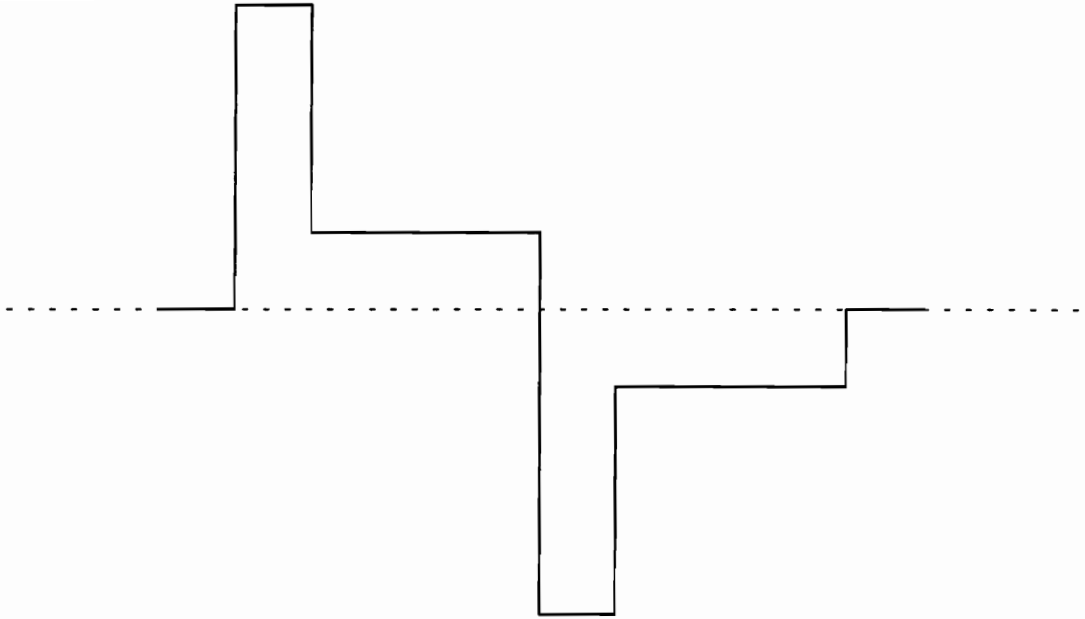
edge would be sinusoidal in nature and might be obtained by a reactive network that allows for "ringing" (i.e., overshoot) on the leading edge of the pulse [Chudobiak and Page, 1969].

3.1.5 SHUNT CAPACITANCE AND SERIES INDUCTANCE

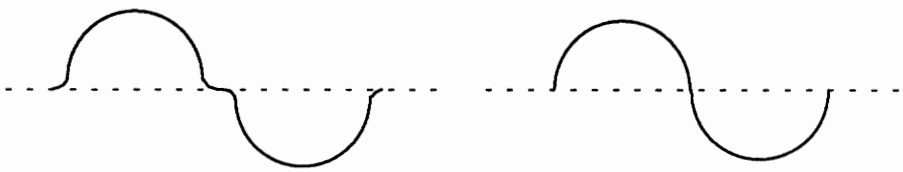
Efficiency reduction due to shunt capacitance or series inductance can be understood by considering their energy storage characteristics. Any shunt capacitance would be charged and discharged each RF cycle. Since a small amount of power is required to charge and discharge this capacitance, that portion of power cannot be delivered to the load, and overall efficiency is reduced. Similarly, any series inductance (e.g., impedance-matching transformers or lead inductance) requires power in order to quickly change current through the inductance each RF cycle. Once again, this is power that would otherwise be available for the load, and overall efficiency is reduced further [Chudobiak and Page, 1969].

3.1.6 REACTIVE LOADS

Most discussions of ideal PA's include the assumption of a purely resistive load. In actuality, many loads contain inductors and/or capacitors for tuning, impedance matching, or filtering, and the reactance of these loads is clearly a function of frequency. Therefore, any deviation from the design frequency (as well as any unaccounted-for parasitic reactance) will produce a reactive load. Reactance causes a phase difference to exist between the voltage and current, and the concern is that an unwanted simultaneous voltage-current product may be created, and power dissipation will be increased. Recalling the added losses associated with shunt capacitance and series inductance, one can see why reactive loads typically result in reduced efficiencies.



(a)



(b)

Figure 3.1 Complex Drive Waveform (a) and Crossover Distortion (b)

Reactive loads may present a danger to the device in the form of increased second breakdown stresses due to a higher instantaneous collector voltage. Also, if the energy storage in the reactance is such that a negative collector current were produced, a large voltage spike of the proper polarity could heavily forward bias the base-collector junction and damage a BJT. (FETs have no such semiconductor junction and are usually able to handle reverse currents without any device damage.) Although the proper use of diodes may alleviate the negative current concern with BJTs, losses associated with these non-ideal diodes serve to reduce efficiency further.

3.1.7 OUTPUT CIRCUIT Q

Most literature makes the assumption that an output load network with a very high quality factor Q allows the effects of harmonic output currents to be neglected⁴. This argument follows from the observation that high Q circuits typically behave as narrow frequency bandpass filters. In a broad sense, however, the quality factor Q should be considered as controlling the bandwidth of a circuit and not so much the out-of-band harmonic suppression.

The value of Q is very dependent upon the topology of the network (i.e., arrangement of inductors, capacitors and resistors), and the same Q can be obtained from different networks that provide different amounts of harmonic rejection. Actual networks possess Q values typically ranging from 3 to 10. Harmonic currents that will then be

⁴A general definition of quality factor Q is:

$$Q = \frac{2 \pi * \text{max instantaneous energy stored in the circuit}}{\text{energy dissipated per cycle}}$$

for a circuit at resonance.

present can alter circuit performance by changing the shape of the output waveform. If the amplifier is designed with a specific output waveform (as is the case with class E), any change from the optimum waveshape can result in increased power dissipation. Another consequence is that additional filtering may be required, resulting in increased losses due to signal attenuation.

3.1.8 INTERMODULATION DISTORTION

Nonlinearity causes undesired distortion to the magnitude and/or phase of the amplified signal. Intermodulation distortion (IMD) is noise that exists near the carrier frequency and is caused by a device nonlinearity which mixes harmonics of the signal spectrum and introduces spurious in-band spectral components. Sources of this nonlinearity include:

1. **crossover distortion.** This occurs when a device moves from the cutoff region to the active region and vice versa. Low level signals are most affected by crossover distortion;
2. **device saturation.** Distortion occurs when a device moves from the active to saturation region, as well as when a device is operated in the saturation region;
3. **variation of device capacitance with voltage (varactor effect).** For BJTs, the base-collector junction and base-emitter junction poses an effective nonlinear capacitance related to the junction "diode". As the instantaneous voltage across the junction varies, the accompanying change in the junction width produces a varying capacitance which is another source of nonlinearity; and

4. **gain reduction at high current levels.** It is well established that the beta (β) of a BJT is not constant, but rather a function of collector current and frequency. Thus, effects of nonlinearity are most noticeable at high current levels and high frequencies where the gain changes most with collector current.

Nonlinearity and subsequent distortion is not always a burden. In fact, amplifiers that depend upon harmonic generation for their operation (e.g., class F) require nonlinear operating conditions. Intermodulation distortion, however, is generally considered unwanted noise and therefore undesirable. Efficiency reductions can be seen by noting that, if signal power exists in distortion products, then that same power cannot be delivered to the load at the desired fundamental frequency.

3.2 ACTUAL AMPLIFIER OPERATION

In this section, each of the ideal amplifier classes will be reexamined in light of the previously discussed limitations. For the sake of clarity, this study will refer to the following set of limitations as standard limitations: saturation voltage, saturation resistance, drive requirements, shunt capacitance and series inductance, reactive loads, and output circuit Q.

All amplifier designs will be affected to some extent by the standard limitations. Intermodulation distortion (IMD) is a primary concern for linear amplifiers emphasizing amplitude control. Switch-mode amplifiers are affected most by transition losses and overdriving, a situation resulting in considerable efficiency reduction. With this in mind, discussion of actual amplifier operation will consist of those items that are significant to that particular class. The discussion will also point out possible compromises.

3.2.1 CLASS A

Both BJTs and FETs are commonly used in class A designs, and they may be implemented as single-ended designs or in push-pull configurations. Because the device operates without entering saturation or cutoff (highly nonlinear regions), intermodulation distortion in class A is the lowest of the three conventional linear classes (A, AB, and B). IMD may be reduced even further, however, by using a push-pull circuit configuration which effectively cancels even-order harmonics. In this arrangement, each transistor is dc-biased class A and amplifies the entire input signal. The lowest level of distortion occurs when matched transistors are used. Class A is subject to the standard limitations and, as mentioned before, the efficiency is lowest of all the classes covered in this study.

3.2.2 CLASSES B AND AB

In addition to the standard limitations, class B linear amplifiers suffer from increased IMD. Consequently, the amplifiers are usually configured in a push-pull arrangement for even-order harmonic cancellation. In this case, each transistor amplifies alternate halves of the input signal, and a transformer network is used to combine the two output signal halves for a complete output RF cycle. Single-ended designs are not used except in cases where narrowband output control is desired, or where severe distortion is not a concern (e.g., inductive RF heating). Most class B designs specify that the dc bias be set just above cutoff in order to reduce crossover distortion (see Figure 3.1). This arrangement is technically classified AB but is often still considered class B.

The line of distinction between classes A, B, and AB is blurred further by a phenomenon known as the self-biasing effect that occurs with BJTs [Overstreet, 1986]. Due to a charge storage effect in the base region, the BJT operating at radio frequencies

never actually reaches cutoff. Thus, harmonic generation (due to device nonlinearity) is lower than if the device had entered cutoff. Even though the device may be dc-biased class B, the self-biasing effect produces operation that closely resembles class A with its lower harmonic generation. The efficiency, however, remains near that expected of a class B amplifier. FETs do not appear to be subject to the self-biasing phenomenon.

3.2.3 TRUE CLASS C

As will be discussed in Section 3.2.5, true class C operation is rarely achieved with BJTs; FETs, however, can be found in the class C designs. Since the device output signal is usually only a small fraction of the input, intermodulation distortion and harmonic generation is substantial. This distortion must be taken into account when considering additional filtering.

3.2.4 SATURATING CLASS C

As may be expected, the saturation resistance R_{ON} of FETs and the saturation voltage V_{sat} of BJTs will affect the operation of the saturating class C amplifier. Each of these limit the maximum output voltage swing (and thus output power) and therefore efficiency is lower than the ideal case.

3.2.5 CLASS C MIXED MODE (OR CLASS CE)

As mentioned previously, the conventional (true) class C design cannot be implemented with BJTs as the active device. Krauss et al. [1980] provide three primary reasons related to BJT device physics that are responsible for this limitation: varactor capacitance, low saturation resistance, and drive and bias difficulties. The relatively high

varactor capacitance of the transistor (due to the semiconductor junctions) and the low saturation resistance contribute to difficulty in maintaining a sinusoidal collector voltage waveform. The varactor capacitance is non-linear and affects the resonant circuit such that the output waveform contains harmonics that it would not otherwise have. Also, the saturation resistance of BJTs tends to load the output network. The end result is a collector voltage waveform that becomes flattened instead of sinusoidal. Finally, if a parallel-tuned output network is not used, any current driven into or out of the base will tend to force the BJT immediately into an active/saturated state, or into a cutoff state. This condition clearly affects the collector current waveform. In order to deal with these limitations, certain compromises must be made in circuit operation and configuration. A new "class" of amplifier must be introduced to describe the altered operation. This class is referred to as class C mixed-mode or class CE [Kazimierczuk and Tabisz, 1989].

The class CE amplifier (Figure 3.2) is so named because its operation lies between that of a class C current source amplifier and a class E switch-mode amplifier. A series-tuned output network is used instead of the parallel-tuned network in order to reduce the problem of low saturation resistance. The varactor capacitance remains, but maintaining sinusoidal waveforms is no longer a concern since the BJT may behave as a switch as well as a current source. Drive and bias requirements are also eased as a result of allowing this switching action. Numerical analysis is commonly used to predict circuit performance during the BJT cutoff, active, and saturation states. An analytical solution is difficult to obtain due to the interdependence of circuit operation on instantaneous circuit conditions [Kazimierczuk and Tabisz, 1989]. More discussion of the class CE amplifier is included in Chapter 5.

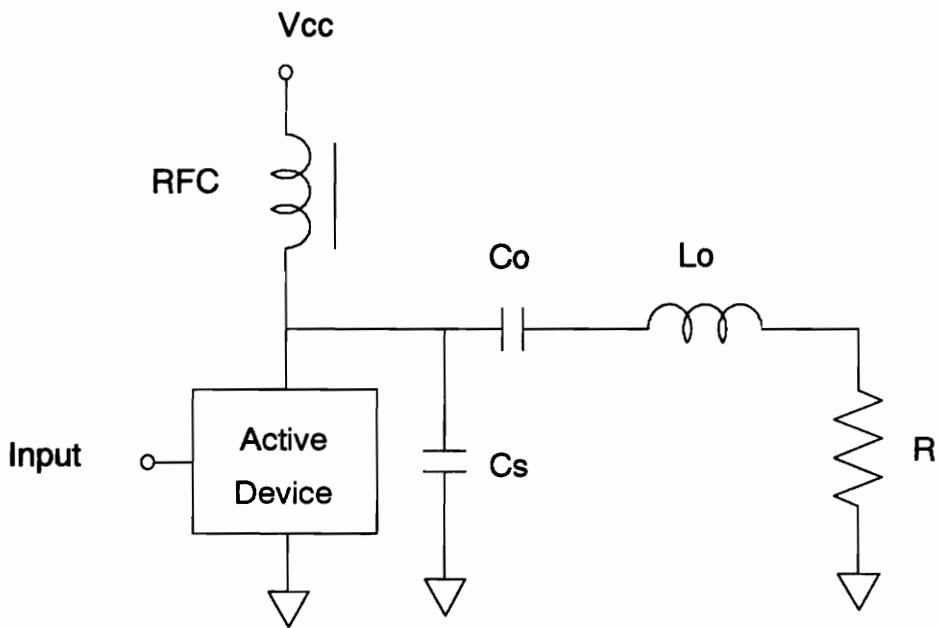


Figure 3.2 Circuit Configuration for Class CE

3.2.6 CLASS D

Losses for the class D amplifier can be divided into two basic categories: transition losses occurring between the cutoff and saturation states, and saturation losses occurring while the device is in a saturated state. Transition losses can be minimized and efficiency maximized by operating the device below $0.1f_T$ for devices rated below 10 W, and $0.01f_T$ for devices rated above 10 W. This high-efficiency design includes the assumption that charge storage times have been minimized by optimizing the drive waveform. Saturation losses are obviously a function of device saturation voltage (or resistance) and, as with any switch-mode amplifier, they serve to limit the maximum output voltage swing, with a resulting reduction of output power and efficiency [Chudobiak and Page, 1969].

3.2.7 CLASS E

Even though the class E amplifier uses the switch-mode technique, the effects of transition losses are not exactly the same as with the class D amplifier mentioned above. The primary difference between the two is that the output load network is designed to keep the voltage or current low while the device is in transition, thus minimizing power dissipation. Even when component values vary reasonably from optimum values, efficiency remains relatively high [Raab, 1978]. The maximum operating frequency of the class E amplifier, however, is inherently limited by the minimum transistor shunt capacitance [Kazimierczuk and Tabisz, 1989]. Thus, device capacitance plays a major role in this design.

3.2.8 CLASS F

Waveshaping via controlling harmonic loads is one of the oldest techniques used to improve efficiency [Snider, 1967]. While the concept is fairly easy to understand, practical implementation can be tedious, especially at higher frequencies. The most difficulty in implementing a class F design at high frequencies appears to be designing the proper source and load impedance at the fundamental and harmonic frequencies. Modeling the nonlinearities at high frequencies is the primary challenge. Depending upon the amount of waveshaping involved, the class F device may behave as a switch. If so, transition and saturation losses would have to be considered as well. Despite these limitations, class F designs have been implemented at frequencies as high as 10 GHz [Hall and Trew, 1991; Kopp and Pritchett, 1990; Raab, 1976; Khatibzadeh and Tserng, 1990].

Most of the class F designs found in literature use FETs as the active device. In order to examine some reasons why this might be so, Chapter 4 and Chapter 5 will include discussion of specific device considerations and their impact on amplifier capabilities.

3.2.9 CLASS G

Because the class G amplifier is acting as a current source, it is subject to the same limitations as classes A, AB, and B. Frequency of operation is limited not only by the device characteristics but by such necessary components as in-line inductors. These inductors are used to minimize distortion due to transient effects caused by the device coming in and out of conduction. Recall from Chapter 2 that the device operating at the lower supply voltage is in the active state as the second device begins to come into

conduction. The distortion associated with switching from one transistor to the next could be severe if it were not limited by in-line inductors.

3.2.10 CLASS H

The class H amplifier could be a very high-efficiency design if the supply voltage level could be made to instantaneously follow the output voltage level. However, the slow rate of the vari-proportional voltage supply would have to be on the order of ten times the maximum operating frequency to accomplish this. Clearly, this is no trivial task for a voltage supply. Additionally, the supply voltage level always remains above zero volts, and thus voltage always exists across the device. This is a condition of continual power dissipation (and thus reduced efficiency) since the class H amplifier is dc-biased class AB. The designer must also be concerned with the possible transient effects on the circuitry caused by rapidly changing the voltage supply level. Isolation techniques would undoubtedly be required. Losses in the power supply control network must also be considered.

3.2.11 CLASS S

In addition to the transition losses and charge storage effects mentioned previously, the class S amplifier requires both pulse width modulation circuitry and a pulse driver amplifier as part of the input network. This additional circuitry not only complicates the design but offers increased power dissipation as well.

CHAPTER 4

4.0 DEVICE AND AMPLIFIER SELECTION

The intent of this chapter is two-fold: to present an overview comparison of BJTs and FETs in order to select a suitable type of device for the desired application, and to briefly evaluate each of the amplifier classes with respect to the system constraints given in Chapter 1. The type of device selected will be determined by factors such as device performance when used as a switch or current source, maximum frequency of operation, and commercial availability.

From the information obtained about device limitations, each class of amplifier will then be re-examined. For the sake of convenience, the system constraints given in Chapter 1 are repeated here:

1. an operating frequency of 850 MHz,
2. a voltage supply obtained from a 9 Vdc battery,
3. a peak power output of 3 W (approximately 35 dBm), and
4. a sinusoidal signal to be amplified, using either frequency modulation (FM) or $\pi/4$ differential quadrature phase shift keying (DQPSK).

Each of these constraints will be used to evaluate the classes of amplifiers to determine suitability for the intended application.

System constraints 1, 2, and 3 are self-explanatory; constraint 4 requires some clarification. Both FM and DQPSK are sinusoidal signals whose peak amplitude is constant, i.e., the information is contained in the frequency or phase variations, and not the

amplitude. Therefore, amplifier characteristics such as linearity or increased average efficiency are not necessarily considered beneficial for this particular application. Frequency or phase information does not require linear amplification, and average efficiency will be the same as peak efficiency for these two signals.

4.1 DEVICE SELECTION - BJT VERSUS FET

At some point in the design process, the designer must decide upon the type of active device to be used in the amplifier. The purpose of this section is to present the information necessary to aid in this selection. Given the system constraints, the device(s) most appropriate for the desired application will be selected. To begin the discussion, an overview of high-frequency power BJTs and FETs will be presented.

4.1.1 BJT

As the frequency of operation increases, BJTs generally offer higher output power than FETs. As power output increases, however, BJTs are prone to a condition known as thermal runaway. BJT current gain (h_{FE}) has a positive temperature coefficient which causes output current to increase as the device temperature increases. The increased output current required for higher output power usually results in increased device temperature, which in turn causes output current to increase even further, repeating the cycle. This process is called thermal runaway and will continue until the device destroys itself due to excessive power dissipation. The threat of thermal runaway can be reduced by a type of negative feedback known as ballasting. Small values of resistance (ballast) are placed in series with the emitter-base junction of the BJT. These resistors are typically a built-in feature of BJT power devices since balance must be maintained between the

multiple devices on a chip that comprise a power BJT [Krauss et al., 1980; Browne, 1987]. As the output current attempts to increase, due to an increase in temperature, the voltage drop across the ballast resistor also increases, causing a corresponding reduction in base-emitter voltage (V_{BE}). A decrease in V_{BE} results in a decreased output current and enhanced temperature stability. It must be noted, however, that this form of feedback causes a reduction in device gain.

Another consequence of the current gain's positive temperature coefficient is the effect on BJT biasing. If ballasting is not used (or is insufficient), the bias supply must be able to automatically adjust the input current required to keep the output quiescent current relatively constant. Thus, simple bias supply designs are usually not possible when using BJTs [Krauss et al., 1980; Manz, 1988].

BJTs must also be protected from excessive voltage that may result from an improper impedance match to a reactive load since they are often run close to breakdown. Care must be taken not to exceed the breakdown voltage of the device, which in turn requires consideration of the output load network. For example, an optimum class E design may subject the BJT to a collector voltage that is 3.8 times greater than the supply voltage. The device must be able to withstand a peak voltage of this magnitude [Manz, 1988; Kazimierczuk and Tabisz, 1989].

Complicated impedance-matching networks are often required with BJTs, primarily as the result of a typically very low input impedance at high frequencies. If the output impedance of the previous stage is relatively high, an impedance transformer with a high ratio is required for a proper impedance match. Practical construction of this transformer can be a non-trivial task [Browne, 1987].

BJTs occasionally suffer from a phenomenon known as sub-harmonic oscillation. As the name suggests, sub-harmonic oscillation is typically a steady spurious signal at half

the operating frequency due to nonlinear effects of the junction "diodes". Among these nonlinear effects is the junction capacitance. As the voltage changes across the junction, its capacitance also changes. This capacitance is essentially a function of time, and its magnitude will determine how much effect it will have on device stability [Granberg, 1989]. The oscillation can occur when this capacitance combines with other circuit elements, discrete and parasitic, and forms a resonant circuit. Such a condition was noted by Overstreet [1986] in which a VHF power amplifier exhibited an oscillation at half the signal frequency. The oscillation was eliminated by placing a lossy⁵ choke in the resonance path, thereby loading down the resonance.

Harmonic generation is an area where BJT performance often exceeds that of FETs. Because the transfer characteristic (collector current versus base-emitter voltage) is inherently nonlinear, BJTs are ideal for harmonic generation. Thus, amplifier classes that rely on the generation of harmonics (e.g., switch-mode classes and class F) may perform better with BJTs than FETs. For sufficient power gain at the desired harmonic frequency, the device should have an f_t at least twice the harmonic frequency [Granberg, 1989].

Perhaps the greatest advantage offered by BJTs is that much experience in processing and application has been acquired⁶. In addition, design engineers have

⁵In this instance, lossy refers to an RF choke with a fairly significant resistance. The resistance serves to lower the quality factor (Q) of the circuit and to "swamp" or load down the circuit resonance.

⁶The use of vacuum tubes as active devices has not been mentioned in this study until now. The development and use of vacuum tubes precede that of BJTs and FETs. Actual operation of a vacuum tube, however, closely resembles that of an FET. In this sense, the design philosophy associated with FETs has been in existence longer than that of the BJT. For the purpose of discussion, the term "experience" refers

developed methods of dealing with the limitations and difficulties, and many of the high-frequency, high-power PAs presently in use contain BJTs.

To conclude this discussion on BJTs, two basic questions must be considered when attempting to choose a device for a particular application:

1. Is the device commercially available (a proven technology)?
2. Does the device operate properly within the given system constraints?

For the BJT, the answer to the first question is a resounding "yes". The second question can be answered by considering the following: device data books contain many RF bipolar transistors that can operate in excess of 850 MHz with 3 W output, provided the device is used as a current source. When used as a switch, the operating frequency is limited by the device output capacitance. Kazimierczuk and Tabisz [1989] examined a class E switch-mode amplifier and determined its maximum operating frequency to be

$$(4.1) \quad f_{\max(E)} = \frac{0.057 P_o}{V_{CC}^2 C_{\min}}$$

where P_o is the power output and C_{\min} is the minimum output capacitance⁷. Thus, for a maximum operating frequency of 850 MHz, power output of 3 W, and a V_{CC}

to the processing and actual implementation of BJTs. BJTs are commonly used because they are readily available and easily manufactured.

⁷The expression for the maximum operating frequency of the class E amplifier is a function of the normalized shunt capacitance (C_s), output load resistance (R), and the device minimum output capacitance (C_{\min}). The assumptions that are made include a zero collector-to-emitter saturation voltage, a 50 percent duty cycle, and a loaded quality factor (Q_L) value of 10. Please refer to the paper by Kazimierczuk and Tabisz [1989] for details.

of 9 Vdc, the minimum output capacitance of a transistor would have to be on the order of 2.5 pF. A typical RF BJT (e.g., Motorola's TP303) has an output capacitance on the order of 18 pF, and thus is capable of switching only at lower frequencies. (The TP303 can operate with a 5 Vdc to 10 Vdc supply at 3 W output power and, in fact, was designed specifically for cellular radio applications using FM in a class C design.)

Therefore, both questions concerning device selection can be answered positively for BJTs if the switching limitations are carefully considered.

4.1.2 FET

High-frequency power FETs consist of several types of devices which can be classified according to their topologies. This study will focus on two of the more familiar topologies. In one group are the insulated-gate FET (IGFET) structures which include devices such as metal-oxide-semiconductor FET (MOSFET), vertical MOS (VMOS), double-diffused MOS (DMOS), and TMOS FET (where the gate structure is T-shaped). Of the IGFET structures, only VMOS, DMOS, and TMOS are designed for high-frequency use. The other group of FETs include topologies with physical junctions, or JFETs. Among these devices are the static-induction FET (SITFET), power silicon FET (PSIFET), and GaAs metal-semiconductor FET (MESFET or GASFET).

The same two questions that were asked of the BJT must also be asked of the FET. For example, although the MOS structures are commercially available, the MOSFET cannot operate at high enough frequencies, and VMOS, DMOS, and TMOS usually require at least a 28 Vdc supply. Additionally, the latter three devices are not designed to operate above 500 MHz. SITFET and PSIFET are still laboratory technologies and thus cannot presently be considered for this application.

The type of FET that remains to be considered, then, is the MESFET which uses gallium arsenide as the semiconductor material. An attractive property of GaAs is its high electron mobility (up to six times greater than that of silicon). The high mobility results in a FET with increased transconductance and decreased electron transit time. When the device active layer is grown on top of semi-insulating (high resistivity) GaAs substrate material, the results include lower parasitic resistance and capacitance. For the purpose of this study, the resulting benefit of increased electron mobility and resistivity is a higher frequency of operation [Pengelly, 1982; Higgins, 1991]. MESFETs are readily available and possess operating frequencies well into the GHz region. Their cost remains high compared to BJTs, but the current trend points to decreasing costs in order to compete with silicon technologies.

Recalling the characteristics of power BJTs given in the previous section, FETs offer the following benefits [Evans, 1981; Manz, 1988; Granberg, 1989]:

1. The temperature stability of the FET is enhanced since the low frequency voltage gain (g_{FS}) has a negative temperature coefficient. As temperature attempts to increase, device gain decreases, causing a corresponding decrease in device current and temperature. Therefore, ballast resistors are not required.
2. Biasing is often simpler due to FETs being voltage driven (versus current driven for BJTs). FETs reach a steady-state operating condition in which they self-limit current drawn from the bias supply (due to the negative temperature coefficient).

3. The chance of second breakdown stress is reduced as the result of the negative temperature coefficient. This fact allows FETs to withstand reactive loads more favorably than BJTs.
4. Impedance matching may be easier with FETs due to the higher impedances involved. Impedance transformers are generally simpler to construct.
5. Sub-harmonic oscillation is inhibited and device stability is enhanced due to the absence of semiconductor diode junctions.
6. FETs possess the ability to conduct current in either direction, a condition which is occasionally encountered with reactive loads.

The primary limitation of high-frequency power FETs is their inability to quickly switch large currents. The main contributors to this limitation are gate length and device input capacitance. Short gate lengths are required for high-frequency operation since they result in decreased carrier transit time, but power dissipation limits the amount of length reduction possible. Providing the FET with a wider gate can increase current carrying capacity (and thus higher output power), but the gate-to-channel capacitance must necessarily increase, causing a decrease in the maximum allowable frequency [Evans, 1981]. For this reason, power FETs used as switching devices are not commonly found above 100 MHz. MESFET amplifiers used as current sources, however, will operate beyond 10 GHz, aided by the material properties of gallium arsenide.

While FETs offer several advantages over the BJT, the FET is still a relatively recent technology (with respect to cost-effective manufacturing), and research into processes and applications continues. On the other hand, silicon technology remains

entrenched and fairly inexpensive, a combination of facts that continue to encourage additional silicon research as well. If one asks the question of what technology a manufacturer will provide, perhaps the answer is the same technology provided in the past. In this case, experience and capital costs heavily influence the decision. (The semiconductor business is competitive, and profit margins are usually low; a manufacturer must minimize capital outlay to maximize profits.)

In summary, assuming that the device is able to operate correctly, the efficiency of an amplifier circuit will generally not be dependent upon which active device is used (BJT versus FET). An exception may be encountered, however, when considering the saturation voltage of the device. FETs typically possess a saturation voltage that is two to three times greater than BJTs. This condition may reduce amplifier efficiency at low voltage supply levels (below 12 Vdc) [Granberg, 1989]. Given that the system constraints for this application include a 9 Vdc supply voltage, the higher saturation voltage of the FET must be taken into account.

4.2 AMPLIFIER SELECTION

In the search for a high-efficiency RF power amplifier, it is necessary to return to the system constraints (mentioned in Chapter 1 and again in the beginning of this chapter) in order to evaluate whether an amplifier operates correctly within these constraints. What follows is a brief discussion of how each amplifier meets (or fails to meet) the criteria. This section will conclude with the selection of class(es) most appropriate for the desired application.

4.2.1 CLASSES A, B, AND AB

Amplifier classes A, B, and AB are used in applications where linearity is a priority consideration. Linearity is achieved at the expense of efficiency and, as discussed in earlier chapters, these three classes exhibit the lowest efficiency of all the classes covered in this study. Also, as mentioned in the beginning of this chapter, FM and $\pi/4$ DQPSK signals have a constant peak amplitude; the information is carried in the frequency or phase modulation, and not in any amplitude modulation. Therefore, the linear amplification provided by classes A, B, and AB is not required for FM or $\pi/4$ DQPSK signals, and the lower inherent efficiency makes these classes undesirable for this particular application.

4.2.2 CLASS C AND SATURATING CLASS C

The efficiency of the class C amplifier (including saturating class C) can approach 90 percent or more by decreasing the conduction angle. However, at this level of efficiency, the power output will be greatly reduced. Recall from the discussion of class C in Chapter 3 that the only means of increasing the power output for a given conduction angle is to increase the amplitude of the input signal. Given battery supply voltage constraints and the desire for high efficiency, the input signal amplitude must necessarily be limited, and consequently so must the output signal amplitude and output power. Due to the inability of the class C PA to provide the required output power, class C and saturating class C will be eliminated from further consideration.

4.2.3 CLASS D AND CLASS S

As mentioned in Chapter 3, the class D amplifier is typically used as a modulator where the collector voltage is varied (under the control of additional circuitry) to produce amplitude modulation. Once again, amplitude modulation is not required for this application. Also, both classes are limited in their frequency of operation due to device switching limitations. Typical switching frequencies will be less than 100 MHz. (Even if these efficient amplifiers could be used, the system efficiency would be reduced by the addition of circuitry required to modulate the collector voltage.)

The class S amplifier also suffers from device-imposed frequency limitations, as well as reduced system efficiency related to the necessary additional circuitry (e.g., pulse-width modulation (PWM) circuitry and a pulse driver amplifier). Based upon the device switching limitations and the requirements for additional circuitry, classes D and S will not be considered further.

4.2.4 CLASS G

Class G obtains its high efficiency by an increase in the average efficiency. Considering that the modulated signals for the desired application possess a constant peak amplitude, the average efficiency is the same as the peak efficiency, and therefore the advantage of operating class G is nullified. Additionally, the class G design requires the device to be turned on and off when the device output current is non-zero. As such, class G is better suited for audio frequencies instead of RF frequencies [Raab, 1986]. The requirement for multiple power supplies may imply additional weight and size concerns. Thus, efficiency and device limitations, as well as possible physical constraints, prevent the consideration of class G for this application.

4.2.5 CLASS H

Class H amplification gains its high efficiency by using two supply voltage levels and requiring the greater of the two to track the output signal level. The limitation of this amplifier is revealed in the inability of the vari-proportional logic control to successfully track the high-frequency sinusoidal signal. To be able to follow the high-frequency signal, the vari-proportional logic control would have to vary the collector supply level at a rate much greater than the signal transition rate (typically 5 to 10 times). Because it is not yet physically possible to switch a large amount of high-frequency power quickly (within the given system constraints), class H will also not be considered further. In practice, the vari-proportional logic control would be difficult to implement in a portable unit without sacrificing efficiency.

4.2.6 CLASS E

The maximum operating frequency of classes D and S amplifiers was said to be bounded by device switching limitations. Class E also suffers from this limitation, but unlike classes D and S, the output load network of the class E amplifier is designed to assist the device in switching. You may recall from Section 2.7 that the transient response of the load network is such the device switching time can be an appreciable portion of the ac cycle time without sacrificing efficiency. Thus, the maximum operating frequency of class E exceeds that of classes D and S. As mentioned in Section 4.1.1, the maximum operating frequency is limited by the device output capacitance. Since commercially available devices have an output capacitance greater than the minimum required ($\cong 2.5$ pF), the class E amplifier cannot operate effectively at the desired frequency, and therefore will not be considered further.

4.2.7 CLASS CE (CLASS C MIXED-MODE)

Class CE power amplifiers are capable of higher operating frequencies than class E. This feature is made possible by using the device as both a switch and a current source. (A non-saturating class C device is used as a current source, and a class E device is used as a switch; class CE device operation lies between these two.) Reduced efficiency is the price that is paid for the increased frequency of operation. Assuming for the moment that the operating frequency can be sufficiently increased without a substantial reduction in efficiency, the class CE amplifier will be considered a candidate for the desired application. Further analysis of this amplifier will be carried out in Chapter 5.

4.2.8 CLASS F

Proper design of a class F amplifier requires that the input and output networks provide an impedance match for the device at the fundamental and harmonic frequencies. For example, it has been found that changes in the input 2nd harmonic impedance can cause the amplifier efficiency to vary between 30 and 80 percent [Hall and Trew, 1991]. The task of designing these networks and simulating circuit performance becomes more difficult as the frequency of operation increases.

Device switching limitations may need to be considered for class F. Depending upon the order of harmonics contained in the output, the device may act as a current source, switch, or a combination of the two. With this potential limitation in mind, the class F amplifier will also be evaluated further in Chapter 5.

4.3 SUMMARY

Based upon this chapter's discussion of devices and amplifier classes, a choice of PA designs are available for further evaluation. Both BJTs and MESFETs can operate as current sources at the desired frequency. The question of partial switching operation will be examined in the following chapter. Classes CE and F meet the system constraints and offer potentially high efficiencies using either device.

In the next chapter, classes CE and F will be evaluated on the basis of research in current literature. Representative BJTs and MESFETs will be used where computer simulation is found to be necessary.

CHAPTER 5

5.0 INTRODUCTION

This chapter will seek to examine both the class CE and class F amplifiers in greater detail than was performed previously in this study. The class CE amplifier will be shown to be a suboptimum case of an ideal class E amplifier. Assumptions concerning class CE design are given and explained. An 850 MHz class CE amplifier will be designed according to the design process provided in the literature, and a simulation will be performed with the PSpice[®] circuit simulation program. This section will conclude with comments on the simulation results and device considerations.

Class F amplifier designs are currently found in mobile radio systems [Nishiki et al., 1987]. An examination of current research literature will provide additional support for its use in the desired application. A recent modification of the class F design will also be highlighted. Finally, the chapter will conclude with a brief discussion of amplifier and device considerations in light of the frequency and power output data which is given in the cited literature.

5.1 CLASS CE ANALYSIS

In order to gain insight into the class CE amplifier, the class C and class E amplifiers will be reviewed in greater detail. The intent of this section is to establish the basis for certain assumptions that are made in the design of the class CE amplifier.

Classes C, CE, and E may be represented by the same circuit configuration as shown in Figure 5.1⁸. The difference in operation is a result of the values chosen for the load network, and the operation of the active device as a current source, a switch, or a combination of the two. Class C efficiency is derived by minimizing the time that collector current and collector voltage exist simultaneously. This is accomplished by reducing the conduction angle. To see how this is achieved, consider a conduction angle of 180 degrees. For half of an RF cycle, a non-saturating class C output would exhibit a simultaneous non-zero voltage and current. This product represents a finite amount of power dissipation for the device. If the conduction angle is decreased, the length of time that this voltage-current product exists would also be decreased. Power dissipation is therefore reduced and the efficiency is increased.

Class E also minimizes the simultaneous existence of current and voltage, but it does so by altering the shape and occurrence of the collector and voltage waveforms. The conditions for optimum performance of a class E amplifier are summarized by Raab [1977] and restated here for convenience: 1) the collector voltage does not begin to rise until the device is fully off (i.e., no collector current), 2) the collector voltage returns to

⁸You may recall from Figure 2.3 that the class C amplifier was configured with a parallel LC tuned circuit at the output. Figure 5.1 shows the class C (as well as classes CE and E) amplifier configuration with a series LC tuned circuit. The two configurations result in the same fundamental frequency output at the load. The difference between the parallel and series arrangements is that the parallel LC circuits shunt the harmonic components to ground while forcing the fundamental components to the load, and the series LC circuits pass the fundamental frequency component to the load while prohibiting passage of the harmonic components. The effect of having the harmonics shunted or reflected back into the device output will determine the extent to which the device behaves as a switch and/or current source.

zero before the device turns on and, 3) the first derivative (slope) of the collector voltage should be zero as the device begins to turn on. If these conditions are met, then the shunt capacitance across the device output will not have any associated voltage to be removed when the transistor turns on. Any losses associated with discharging this capacitance through the device will then be minimized.

Based upon the conditions of optimum performance, a class CE amplifier may be viewed as a suboptimum class E amplifier. During each RF cycle the device will behave as a current source in certain regions and as a switch in other regions of the cycle. Viewed as a suboptimum class E amplifier, a finite amount of collector voltage will exist across the shunt capacitance, power will be dissipated by subsequent discharge of this voltage, and efficiency will be reduced. As was stated in Section 4.2.7, the disadvantage of lower efficiency is offset by an increase in the maximum operating frequency. This condition is due to the device behaving less as a switch and more as a current source.

To begin the analysis of the class CE amplifier, extensive reference is made to the introductory article by Kazimierczuk and Tabisz [1989]. Several assumptions concerning the class CE design are made by these authors. Taken from their paper, these assumptions are:

1. The inductance L_{RFC} of the RF choke is sufficiently large so that the ac ripple in the supply current i_{CC} will be neglected; the parasitic series resistance of the choke is zero. (In practice, a bypass capacitor at the dc supply point is used to shunt high-frequency signal components to ground, again ensuring that the supply current is essentially ripple-free.)
2. The load-network elements C_1 , C_0 , L_0 , and R are ideal, i.e., they are passive, linear, time-invariant and their parasitic components are zero.

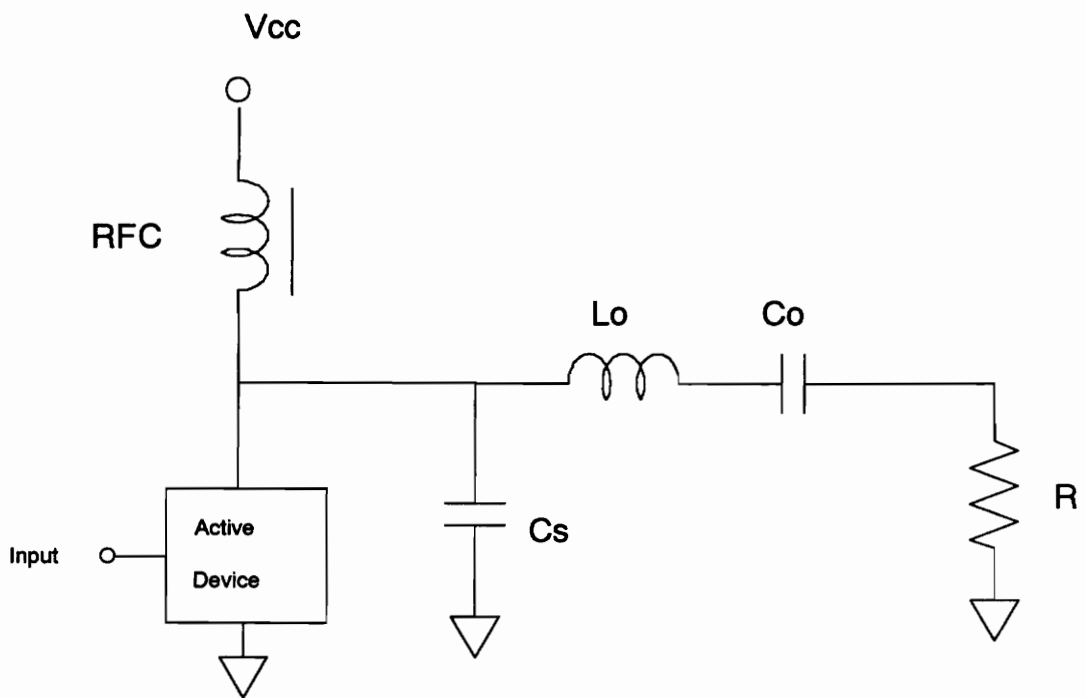


Figure 5.1 Circuit Configurations for Classes C, CE, and E

3. Dynamic effects in the transistor are neglected.
4. The conduction angle of the collector current for the Class C and CE amplifiers is 180 degrees and the switch duty cycle⁹ for the Class E amplifier is 50 percent. This provides the maximum output-power capability.
5. The loaded quality factor (Q_L) of the RLC series-resonant circuit is assumed to have a value of 10. In addition, the network component values are related to the quality factor by $Q_L = \omega_0 L/R = 1/\omega_0 CR = (L/C)^{1/2}/R$ at the series RLC circuit resonant frequency of $\omega_0 = 1/(LC)^{1/2}$.

Assumptions 1 and 2 are commonly used in many circuit analysis techniques where ideal conditions are presented. The dynamic effects mentioned in the third assumption would include such phenomena as hot carrier effects, base-width modulation, and the varactor effect. These conditions may well exist, but their effects will (hopefully) be of secondary importance. Making the assumption that these effects can be neglected also serves to simplify the analysis and computer simulation without resulting in any serious discrepancies with experimental results.

It has already been stated in Chapter 2 that the conduction angle for a class C amplifier is less than 180 degrees. Yet, the fourth assumption above states that the conduction angle for classes C and CE will be 180 degrees. For the purposes of this discussion, the conduction angle for an amplifier biased at class C may be considered as arbitrarily close to 180 degrees.

⁹Switch duty cycle is usually expressed as a percentage and may be defined as the ratio of device "on" time per cycle to the total cycle time.

With respect to the statement associated with the maximum output-power capability, Kazimierczuk and Puczko [1987] studied the class E tuned power amplifier and found that, with a 50 percent duty cycle and loaded quality factor (Q_L) greater than five, the power contained in the output signal harmonics was less than 1 percent (.01) of the total output power. In other words, the output power is maximized at the fundamental frequency when the power contained in the harmonic frequencies is minimized. Thus, a 50 percent duty cycle (and apparently a 180 degree conduction angle) provides maximum power output capability.

The last assumption, concerning the loaded quality factor, was mentioned briefly in Section 3.1.7 on practical considerations. A sufficiently high value of Q_L ($Q_L = 10$ in this example) is made in order to assume a negligible harmonic current content at the load R . Neglecting these harmonic currents will allow for a relatively distortion-free sinewave output signal. By assuming the output signal is sinusoidal, calculations of power delivered to the load can be simplified.

5.1.1 CLASS CE DESIGN

Kazimierczuk and Tabisz [1989] employ a BJT as the active device in their design of the class CE amplifier. Because the transistor behaves as both a switch and a current source, at least three regions of operation must be taken into account: the cutoff, active, and saturated regions. Additionally, provision must be made for the possibility of positive or negative switching current¹⁰. A FORTRAN program written by these two authors was used to perform a numerical analysis of the amplifier operation. This program was also used to vary the component values and the drive current levels to optimize the amplifier

¹⁰As mentioned in Section 3.1.6, negative currents may result from reactive loads.

efficiency. They then fabricated a 2 MHz class CE BJT amplifier using their design procedure in conjunction with the optimized circuit values. The measured results of the amplifier compared favorably with a SPICE® simulation. In addition to providing design equations, the authors show that the sensitivity of the class CE amplifier to the load network components is low, and the region of high efficiency (greater than 90 percent) is large. The design equations that follow are a direct result of their findings. It is assumed that the power supply voltage (V_{CC}), desired power output (P_O), and minimum device output capacitance (C_{min}) are known. A quality factor (Q_L) value of ten is also assumed.

The class CE amplifier has been shown to be a sub-optimum class E amplifier. Therefore, it is helpful to provide a relationship between these two classes. The maximum operating frequency of an ideal class E amplifier, given in Section 4.1.1 and repeated here for convenience, is:

$$(5.1) \quad f_{max(E)} = \frac{0.057 P_{o(E)}}{V_{cc}^2 C_{min}}$$

An index (k_f) is used to provide the relationship between classes E and CE:

$$(5.2) \quad k_f = \frac{f_{max}}{f_{max(E)}}, \quad \text{where}$$

f_{max} is the desired operating frequency for the class CE amplifier. Referring to Table II in the article by Kazimierczuk and Tabisz [1989], the value of k_f is used to obtain the next three parameters: the normalized reactance (x) of the series $RL_O C_O$ circuit, the normalized susceptance (b) of the shunt capacitance C_S , and the normalized output power (a).

Finally, the circuit component values can then be calculated given the three parameters (x , b , and a).

The resonant frequency (ω_0) of the series RL_0C_0 circuit is

$$(5.3) \quad \omega_0 = \frac{2 \omega Q_L}{x + \sqrt{x^2 + 4 Q_L^2}}$$

The components values for the series load network are given by:

$$(5.4) \quad R = \frac{a V_{CC}^2}{P_o}$$

$$(5.5) \quad L_0 = \frac{Q_L R}{\omega_0}$$

$$(5.6) \quad C = \frac{1}{\omega_0 Q_L R}$$

Finally, the collector efficiency of the circuit can be obtained with the following relationships:

$$(5.7) \quad \eta_c = \frac{P_o}{P_{CC}}, \quad \text{where}$$

$$(5.8) \quad P_o = I_{o,rms} V_{o,rms}, \quad \text{and}$$

$$(5.9) \quad P_{CC} = I_{CC} V_{CC}$$

5.2 CLASS CE DESIGN EXAMPLE

Using design equations (5.1) to (5.9), the component values are calculated for a class CE amplifier operating with the design constraints shown in Table 5.1. The shunt

capacitance value was chosen because it is representative of a typical device output capacitance for a device operating under the given frequency and power conditions. The results of the component calculations are shown in Table 5.2.

Table 5.1 Design Constraints

Operating frequency, f_{\max}	850 MHz
Peak power output, P_O	3 W
Supply voltage, V_{CC}	9 Vdc
Shunt capacitance, C_S	15 pF
Quality factor, Q_L	10

Table 5.2 Parameter and Component Values for the Class CE Amplifier

Parameter or Component	Value
$f_{\max}(E)$	$\cong 141$ MHz
k_f	$\cong 6$
x	$\cong 1.8$
b	$\cong 0.352$
a	$\cong 0.195$
C_S	15 pF
C_O	3.89 pF
L_O	10.78 nF
R	5.265 Ω

Given the amplifier component values, PSpice[®] analysis files are created for both a BJT and a MESFET device. The file listings are provided in Section A.2 of the Appendix. The active device parameters are representative of relatively ideal devices. For example, the input and output capacitance for both the BJT and MESFET are assigned the default value of zero Farads. The device capacitance values are fixed by adding a discrete capacitor where desired. This is done to eliminate the concern of how a PSpice[®] device model interprets an assigned parameter value. The transition times for the BJT are initially set to the default value of zero seconds. The assumption behind this action is that devices which currently exist are capable of switching at the system frequency, and therefore, the transition times need not be a major concern for this simulation.

In each amplifier design, an initial simulation was performed using the calculated component values. The efficiency calculations were performed using the average (AVG) and RMS functions provided in PROBE[®] (the post-processor graphics package associated with PSpice[®]). Since PSpice[®] performs a transient analysis, and not a steady-state analysis, the simulation was run over a 50 ns time period (roughly 40 RF cycles at the given frequency) to reach an approximate steady-state condition. For the BJT, the collector efficiency was approximately 66 percent; the MESFET simulation provided an efficiency of 57 percent. By extending the time period of the transient analysis (approximately 300 ns), the efficiencies were determined to be 73 percent and 61 percent for the BJT and MESFET, respectively¹¹. Table 5.3 summarizes the results of each simulation.

¹¹Clearly, performing steady-state analysis using PSpice[®] can be a time-consuming procedure for RF circuits. An alternative technique is the Harmonic Balance method as described in Section A.3 of the Appendix. Harmonic Balance can be a much more time-efficient technique for performing steady-state

Table 5.3 BJT and MESFET Simulation Results

BJT Amplifier	Result
P_o	1.33 W
P_{CC}	2.0 W
η	66%

MESFET Amplifier	Result
P_o	1.14 W
P_{CC}	2.0 W
η	57%

5.3 CLASS CE SUMMARY

Several points can be made about the results of the class CE amplifier analysis. First, the design process is relatively straightforward and all of the component values can be calculated using the given design parameters (i.e., x , b , and a)¹². Second, although the power output and efficiency results from the initial simulation are lower than the calculated values, the circuits were not optimized for maximum efficiency and/or maximum power output. Kazimierczuk and Tabisz [1989] point out that in the case of the BJT amplifier, the efficiency was strongly dependent upon the value of driving base

analysis, especially if optimization of the circuit components is desired. In this study, circuit optimization is not a priority and therefore PSpice[®] is sufficient for the purpose of analysis.

¹²Although these parameters are provided in tabular form by Kazimierczuk and Tabisz [1989], the same results would be obtained by using any program similar to the one used by the authors which accounts for the same transistor operation characteristics.

current. It is expected that both the power output and efficiency would improve if the circuits were optimized¹³.

Finally, the issue of practical considerations must be addressed. It is reasonable to assume that the efficiency (and thus power output) would be reduced as the device input capacitance increases. This results from an additional capacitance which would require charging and discharging for each RF cycle. In addition, the calculated value of the load resistance ($R = 5.265 \Omega$) is far from a typical load (e.g., $R = 50 \Omega$ of an antenna). By recognizing that the output of this amplifier would require additional filtering to reduce the harmonic content at the transmitter output, then the filter would have to ultimately be designed to consider impedance matching as well. Use of the filter network would undoubtedly result in a finite loss of power output and a reduction of overall system efficiency.

5.4 CLASS F ANALYSIS

In Section 4.3, it was stated that class F power amplifier designs using either BJT or MESFET devices should be able to operate correctly within the given system constraints. Figure 5.2 illustrates a typical class F circuit configuration. Although a class F amplifier is usually dc-biased at a class B level, as mentioned in Section 2.8, its efficiency is higher than that of a class B. The higher efficiency is achieved by "squaring up" the collector voltage waveform and minimizing the time during which current and

¹³Although this study does not seek to examine circuit optimization, a preliminary simulation was performed in which the load network component values were varied one at a time, and the values chosen were those that resulted in maximum efficiency. In both the BJT and MESFET simulations, the maximum efficiency was determined to be nearly 80 percent at a power output exceeding 2 W.

voltage exist simultaneously. This waveshaping is accomplished by causing certain harmonics of the output signal to be reflected back into the device. Thus, obtaining proper impedance matches at the fundamental and harmonic frequencies is a crucial design requirement for high-efficiency class F amplifiers. The impedance matching must take into account the correct order and amplitude of the harmonic components.

Many examples of high-frequency class F amplifiers exist in recent literature. Operating at frequencies in excess of 1 GHz, the class F concept (sometimes referred to as harmonic impedance matching or waveshaping) is becoming more common in GaAs monolithic microwave integrated circuits (MMICs). Examination of recent literature will show that class F amplifier technology exists not only in the laboratory, but in practical circuits as well. Finally, a PSpice[®] analysis of a class F amplifier design is performed to provide additional justification for the use of class F designs in portable communication systems.

5.4.1 CLASS F AMPLIFIER DESIGNS IN LITERATURE

You may recall from Section 4.2.8 that varying the impedance of the second harmonic termination can result in an amplifier efficiency ranging from 30 to 80 percent. The following examples describe several class F amplifiers in which the second harmonic frequency components are reactively terminated with a short:

- At an operating frequency of 5 GHz, a computer simulation of a 1200 μm MESFET¹⁴ power amplifier resulted in a power output of 691 mW with an efficiency of 80.5 percent. In addition, it was shown that both the input and output impedances should be shorted at the second harmonic for maximum efficiency [Hall and Trew, 1991].

¹⁴The dimension of 1200 μm refers to the MESFET gate periphery.

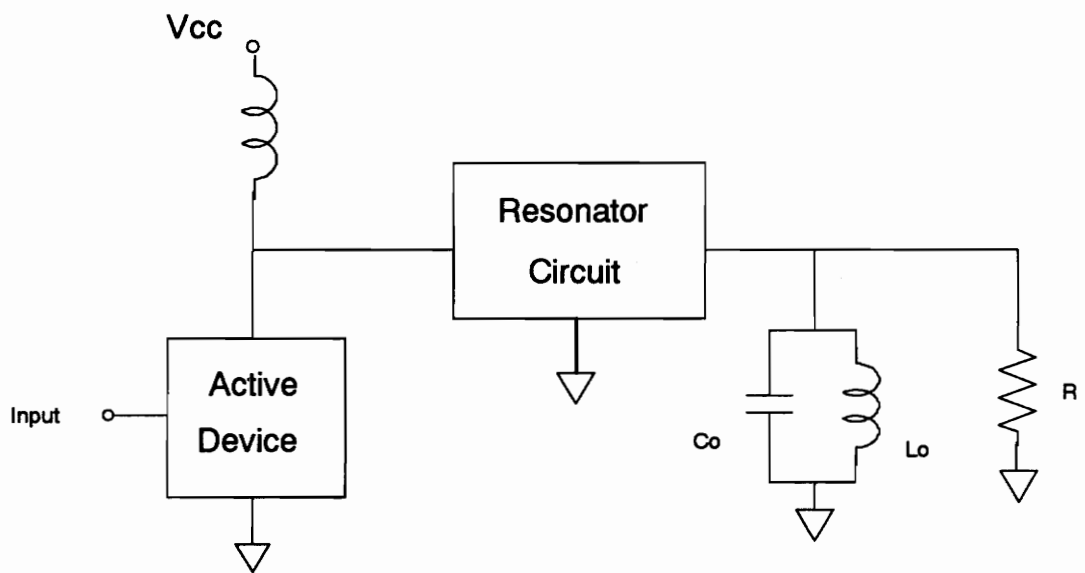


Figure 5.2 Circuit Configuration for Class F

- A simulation using the harmonic-balance method (see the Appendix, Section A.3) revealed an efficiency increase from 54 percent to 65 percent by terminating the amplifier *input* with a short at the second harmonic. Based upon these simulation results, a 10 GHz MESFET amplifier was fabricated and tested. The measured results show an efficiency of 61 percent at a power output of 450 mW [Khatibzadeh and Tserng, 1990].
- Fabricated as part of a multistage amplifier for satellite communications, a 1 W GaAs FET amplifier achieved a 65 percent efficiency at 4 GHz [Geller and Goettle, 1988].
- Bahl et al. [1989] fabricated a power MMIC amplifier. The measured results included an efficiency of 70 percent and 1.7 W power output at 5 GHz.

It is worth noting a recent publication referring to a modified class F amplifier as the Harmonic Reaction Amplifier, or HRA [Nishiki and Nojima, 1987]. The HRA is composed of two FETs configured in a push-pull arrangement. The drains of the two FETs are connected together via a second harmonic signal path which has an adjustable length in order to vary the second harmonic resonance (see Figure 5.3). (The mechanism for the length adjustment was not mentioned specifically, but is most likely a type of transmission delay-line structure.) When this length is properly adjusted, each FET injects a second harmonic current into the other in such a way as to create a second harmonic standing wave whose amplitude is zero at the FET drains. The result is an amplifier with a 75 percent efficiency and 2.7 W power output at 1.7 GHz. A conventional class F amplifier at the same frequency yielded an efficiency of 65 percent with 1.5 W power output. An updated version of the Harmonic Reaction Amplifier produced a 2 GHz, 5 W power output with a 70 percent efficiency [Nishiki and Nojima, 1988]. Both of these amplifiers used a class B dc-bias arrangement. Also, it should be noted that the updated

version of the HRA exceeds both the power output and frequency requirements for our application. An added benefit of this particular design is a lower dc supply voltage (i.e., $V_{dd} = 7 \text{ Vdc}$). Based upon the data found in these citations, the Harmonic Reaction Amplifier (modified class F) supports the decision to include discussion of class F amplifiers for the application of portable communication systems.

As was mentioned in Section 2.8, class F amplifiers may also be designed by including the third harmonic frequency components in addition to the second order harmonic components. Instead of providing a short, however, the third harmonic components must see an open circuit in order to be reflected back into the device output. The third order reflection serves to "square up" the output waveform even further, resulting in an additional increase in efficiency. This is sometimes referred to as third harmonic peaking.

One example of a third harmonic peaking class F amplifier is reported by Kopp and Pritchett [1989]. A nonlinear simulator employing the harmonic balance technique was used to examine a MESFET amplifier which provided a short for the second harmonic frequency component and an open for the third harmonic. The result was an efficiency of 61.3 percent at 10 GHz and a power output of 270 mW. This efficiency represents an 8 percent increase over a comparable class B amplifier at this frequency. High-frequency class F designs employing third harmonic peaking are not abundant in the literature. One reason for this, as mentioned in Section 2.8, is as the frequency of operation increases, accurate knowledge of the device impedances becomes increasingly difficult to obtain. However, Hall and Trew [1991] point out that the amplifier efficiency is relatively insensitive to impedance matching at the third harmonic

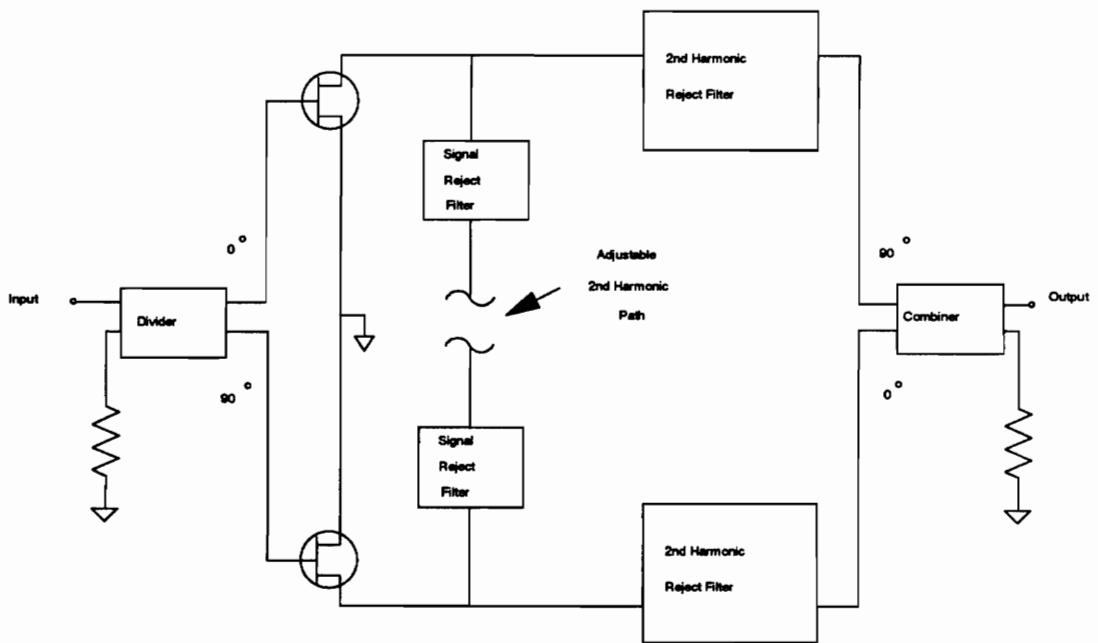


Figure 5.3 Circuit Configuration for the Harmonic Reaction Amplifier

as long as the input and output impedances presented to the third harmonic components are large in comparison with other circuit impedances. Thus, if second harmonic class F designs provide the necessary increase in efficiency, design of the third harmonic impedance matches may not be necessary. Any increase in efficiency is desirable, but the value of the increase must be weighed against the cost of obtaining that increase.

In an effort to further examine the third harmonic peaking class F amplifier, a PSpice[®] simulation was performed. Using the device parameters provided by Kopp and Pritchett [1989], a class F amplifier was simulated at an operating frequency of 10 GHz. The results are shown in Table 5.4. The PSpice[®] files are provided in the appendix, Section A.4. Although the output power and efficiency of the PSpice[®] simulation is higher than that given by Kopp and Pritchett, the results are not unrealistic. Considering that the device parameters were taken from an actual device, the simulation results are encouraging.

Table 5.4 Simulation Results for the Class F Amplifier

MESFET Amplifier at 10 GHz	Result
P_o	2.45 W
P_{CC}	2.95 W
η	83%

5.4.2 MESFETs AND BJTs IN A CLASS F DESIGN

There are two points to note concerning each of the previous citations. First, each of these amplifiers operated at frequencies much higher than 850 MHz. This has significance when considering the efficiencies and output powers provided in these citations. With the exception of the modified class F Harmonic Reaction Amplifier [Nishiki and Nojima, 1988], the output power for each of the cited designs was less than the 3 W peak power desired. It is a well established fact that power gain tends to increase as the frequency of operation is decreased¹⁵. Thus, if the operating frequency of these amplifiers were decreased to 850 MHz, it is reasonable to assume that, for a given input power, the efficiency would increase due to an increase in the output power. This can be seen in the literature just cited: a 61 percent efficiency at 10 GHz versus an 80.5 percent efficiency at 5 GHz; likewise, the output power was doubled for a decrease in the operating frequency from 10 GHz to 4 GHz.

It is also worth mentioning that higher output powers are possible through the use of multi-device amplifiers. Such is the case of a 5 W GaAs FET amplifier with an efficiency of 35 percent at 10 GHz [Kopp and Heston, 1988]. Here again, a decrease in the operating frequency would be accompanied by an increase in efficiency. There is no reason to doubt that high-efficiency class F amplifiers using FET technology cannot be used for the desired application, by proper design, taking into account the trade-offs between power output and efficiency.

The other point to consider about these citations is the exclusive use of FETs. Although it was not stated why BJTs were not used, the fact that many of the citations

¹⁵This is why high frequency devices can become unstable when used at low frequencies: the gain is very large.

involved amplifiers for MMIC (high-frequency) applications points to one possible reason. Since GaAs is usually the material of choice for microwave applications, it is reasonable to find FET technology being used in these amplifiers. Additionally, GaAs fabrication processes are geared to FET production; fabrication of GaAs BJTs is complex due to the difficulty of performing diffusion processes in GaAs material.

As was already mentioned in Section 4.1.2 on FET devices, GaAs possesses the attractive properties of fewer parasitics, and therefore higher operating frequencies, and a higher electron mobility [Pengelly, 1982; Higgins, 1991]. Also, the slightly higher impedances inherent in FET structures provide the FET with a slight advantage over BJTs in areas such as biasing and impedance matching. Finally, GaAs devices were the first to be used successfully at the high frequencies cited in the literature. At a (relatively) low frequency of 850 MHz, the designer's choice to use a MESFET instead a BJT might well be regulated by the same reasoning that a designer familiar with silicon devices might use a BJT.

The question that remains is not whether BJTs can operate at 850 MHz, but can they operate in a class F design at 850 MHz¹⁶. Perhaps the answer to this question may be found in an observation concerning class F operation [Krauss et al., 1980]. A statement was made that actual class F operation exhibits characteristics of a saturating class C amplifier and a suboptimum class E (i.e., class CE) amplifier. In addition, considerable device saturation is usually noted with actual class F amplifiers. Since this condition is typically associated with devices behaving as switches, class F designs using BJTs must take into account any switching losses.

¹⁶The fact that silicon BJTs can operate in the GHz region is proven and accepted. For example, see Basset and McCombs [1981] and Wang [1985].

Referring to Section 3.1.3, recall that switching losses are caused by the time delay experienced while the device input and output capacitances are being charged¹⁷ (rise and fall times), and by the time delay associated with the device conduction area being swept clean of excess charge carriers as a result of saturation (charge storage). Assuming that the input/output device capacitance is equivalent for the BJT and MESFET, then the difference between the two devices will be due to the charge storage.

Consider that the BJT has two semiconductor junctions in the current conduction path: the base-emitter and the base-collector junction¹⁸. For a BJT in a saturated state, a large amount of excess charge carriers exist in the base and collector regions. The saturated state results in the base-emitter and base-collector junctions being forward-biased. When the driving force is removed, the excess carriers must be removed before the collector current can begin to decrease and the BJT can enter an active or cutoff state. You may recall from the theory of BJT operation that the large electric field created by the reverse-biased base-collector junction is responsible for sweeping the charge carriers out of the base region. When the junction is forward-biased (e.g., during a state of device saturation), this electric field is greatly reduced and the charges tend to move more slowly. It is only when the excess charges are removed that the base-collector junction can return to its normal reverse-biased condition. A finite amount of time is required to remove

¹⁷In this chapter's analysis of the class CE amplifier, the input and output capacitance values were assumed to be zero.

¹⁸Here, "junction" refers to adjacent semiconductor materials of two different types (i.e. n-type and p-type material). The channel of a MESFET has no such junctions; the ohmic contact regions for the source and drain will typically have a much higher doping concentration than the channel, but these regions are of the same type semiconductor material.

these excess charge carriers and to cause the transistor to enter an active or cutoff state. If the frequency of the drive signal is greater than the time required to remove the excess charge carriers, the device cannot switch to a cutoff state [Neamen, 1992]. Thus, depending upon the degree of device saturation that occurs in a class F design, a given BJT may not be able to operate correctly.

These comments on BJT operation are not meant to imply that BJTs cannot be used in class F amplifier designs. Rather, the purpose of the discussion is to examine why a BJT might not function as well in a class F design. There is no reason to believe that a BJT could not be a suitable device, and as fabrication methods and capabilities continue to improve, switching losses at the system frequency of 850 MHz will not even be a concern.

In summary, the feasibility of class F amplifier designs for the intended application has been demonstrated through the examination of research literature. Most current designs use some form of second harmonic reactive terminations to increase the amplifier efficiency. The required high efficiency and the output power can be obtained with current technology. Although all of the cited designs use FETs as the active device, it is reasonable to assume that properly designed BJTs could be used as well.

CHAPTER 6

6.0 SUMMARY OF WORK COMPLETED

The work which was completed in the course of this study includes the compilation of ideal amplifier classifications and their definitions, the discussion of limiting factors which cause the amplifier operation to deviate from the ideal operation, the selection of amplifier classes and active devices which fulfill the given system constraints¹⁹, and the evaluation of two classes (class CE and class F) and two active devices (BJT and MESFET) which were deemed appropriate for use in high-efficiency RF power amplifier designs.

The amplifier classifications and definitions presented in Chapter 2 provide a valuable summary in a unified and concise manner that is not commonly found in the literature. The discussion of amplifier circuits and their operation will be of use to those persons desiring a succinct explanation of the different amplifier classes.

The limitations that prohibit ideal operation of the amplifiers were discussed in Chapter 3. The primary limitation for linear amplifiers (classes A, B, and AB) was determined to be intermodulation distortion. Saturation voltage (or saturation resistance) and transition losses were considered to have the most effect on switch-mode amplifiers (classes D, E, and S). Amplifiers which are used as amplitude modulators (saturating class C, class D, and class S modulator) were said to transfer any efficiency benefits to the

¹⁹The system constraints are repeated here for the sake of convenience: an operating frequency of 850 MHz, a voltage supply obtained from a 9 Vdc battery, a peak power output of 3 W, and a sinusoidal signal to be amplified.

modulation driver circuitry. Of the multiple power supply designs (classes G and H), class H was also said to transfer its efficiency to the circuitry required to modulate the power supply voltage. Class G was found to be limited to audio applications due to the transient effects caused by turning on the active device during significant current conduction. Finally, the class CE amplifier was introduced in Chapter 3 as a mixed mode class in which the active device behaved as a switch and a current source over different parts of the RF cycle. Depending upon the type of load network used, the active device of the class F amplifier may behave in a similar fashion.

In Chapter 4, the active devices and amplifier classes were examined with respect to the given system constraints. A practical discussion of high-frequency power BJTs and FETs was presented. The primary conclusion concerning the active devices is that, despite the complexity associated with some BJT designs, BJTs are readily available and widely used due to the significant amount of acquired process experience. MESFETs, however, will continue to be used at higher frequencies primarily because GaAs is the material of choice in microwave designs. Chapter 4 concludes with a re-evaluation of the amplifier classes. Based upon the system constraints, class CE and class F were chosen for their potential to operate at high frequencies with a high efficiency. It was also determined that BJTs and MESFETs would be considered for the active devices used in these designs.

The class CE amplifier design process was explained in Chapter 5. Using specific design guidelines, two versions of a class CE amplifier (using a BJT and a MESFET as the active device) were simulated on a computer using the PSpice® circuit analysis program. At an operating frequency of 850 MHz, the initial simulations show amplifier efficiencies of 66 percent and 57 percent for the BJT and MESFET design, respectively. Because the

circuits were not optimized (with respect to component values and drive levels), efficiencies and output power levels were lower than expected.

The class F amplifier design was evaluated by the research results found in literature. The majority of the designs employed some form of second harmonic reactive termination to improve the efficiency of an otherwise conventional class B amplifier. The ideal termination for the second harmonic component is a reactive short. It was established that the class F amplifier is capable of operating at the desired frequency with efficiencies greater than 70 percent. The Harmonic Reaction Amplifier (HRA) was introduced as a modified class F amplifier using two active devices in a push-pull arrangement. The HRA was found to offer a power output and efficiency that exceeds the system requirements. A high-frequency (10 GHz) MESFET design was also examined through the use of a computer simulation. The result was an efficiency of 83 percent at an output power of 2.45 W. The MESFET is the active device predominantly used in class F designs, but this appears to be due to the high frequencies encountered in the literature (greater than several GHz). BJTs designed for high-frequency use should also be considered for the active device in a class F amplifier.

6.1 TOPICS FOR FUTURE RESEARCH

There are several areas related to this study in which additional research could provide substantial benefits. This section will briefly mention these areas and discuss some practical considerations.

First, as mentioned in Chapter 1, the users of the cellular telephone system do not control the power output of their unit; the cell site automatically and continually adjusts each unit's output power. In this study, it has been assumed that the power output is relatively constant. A practical power amplifier design would have to account for a

varying output power while maintaining a high efficiency. For example, it has been established that the efficiency of a class CE amplifier is dependent upon the amount of drive current (for a BJT design). If the output power were to be reduced by using a lower drive current, then the efficiency would certainly be affected. Therefore, methods of controlling output power should be examined for this particular class, as well as other classes that may suffer from this limitation.

Secondly, there are many different types of devices that are currently being developed which could be investigated for use as the active device in high-efficiency designs. Chapter 4 mentions several of these, including the static-induction FET (SITFET) and the power silicon FET (PSIFET). Another device which was not mentioned in this study is the heterojunction bipolar transistor (HBT). The HBT offers the potential of higher output powers than the MESFET, with the added benefit of operating speeds approaching that of MESFET devices [Higgins, 1991]. As the fabrication methods and operating capabilities of the HBT and other devices improve, some of the other classes of switch-mode amplifiers (e.g., class D or class E) should be reconsidered.

Finally, areas of practical design such as impedance matching, driving the amplifier, and biasing should be investigated. For example, impedance matching networks that take advantage of existing parasitic reactances (i.e., device or circuit parasitics) could result in lower insertion losses and thus higher amplifier efficiency. By taking advantage of the operating characteristics of a device, research aimed at developing specific drive waveforms may also increase the efficiency of an amplifier. As development of active devices continues, different techniques may be required to meet special biasing or impedance matching requirements. Research into these areas should be considered.

APPENDIX

A.1 PSpice®

Circuit analysis is often performed by writing a set of linear or differential equations that describe a circuit, and then solving those equations. Computers can be used to solve many such simultaneous equations using a variety of numerical techniques. PSpice® is a personal computer-based circuit-analysis program which originated from the mainframe-based SPICE® (Simulation Program with Integrated-Circuit Emphasis), which itself originated at the University of California, Berkeley, California, in the late 1960's.

With this program, components and devices (e.g., resistors, capacitors, transistors, etc.) are described mathematically by finite difference equations (which resulted from the initial differential equations). Each set of nonlinear algebraic equations are then solved iteratively at each time step [Gilmore and Steer, 1991]. In this way, a transient analysis is performed. As will be discussed in section A.3, PSpice® is not able to perform steady-state analysis. Rather, it approximates steady-state analysis if the transient analysis is run for an extended period of time.

To perform a given type of analysis (e.g., transient, temperature, Fourier), a circuit is described in a file listing called a netlist. Components are described by stating its type (e.g., R for a resistor, C for a capacitor, etc.), the circuit nodes to which it is connected, and its value. For example, a 10 K Ω resistor connected between nodes 7 and 8 would be described as:

```
R1 7 8 10k.
```

Following the listing of circuit components, the type of analysis is then specified. PSpice® uses this completed file and solves the finite difference equations associated with the circuit components with respect to the stated circuit conditions.

In the case of this study, the "solution" is the result of a transient analysis. A post-processing graphics package called Probe® may be used as an "electronic oscilloscope" to view the transient response at different places within the circuit. PSpice® is made available by the MicroSim Corporation.

A.2 PSpice® NETLISTS FOR THE CLASS CE AMPLIFIER

The component values for the following netlists are obtained by using the class CE design procedure provided by Kazimierczuk and Tabisz [1989]. Computer simulations using these netlists can be performed with PSpice® versions 5.0 and later.

```

*      Class CE Amplifier using an Ideal BJT

*      Voltage Supply
Vcc      1      0      9V
Cbypass  1      0      100nF

*      Component Values
L(RFC)   1      2      74.7nH
C1       2      0      15pF
Co       2      5      3.7pF
Lo       5      6      11nH
R        6      0      4

*      Active Device - BJT
Q1       2      3      0      CE-BJT
.model   CE-BJT      npn

*      Drive Circuitry
Vdrive   4      0      sin(0 1.5 850e6 0 0 0)
Rdrive1  4      0      10k

```

```
G1          3      0      table {v(4,0)} [(-1.5,-15m) (0,0)]
Rdrive2     3      0      10k
```

```
*      Analysis Commands
```

```
.tran 1ps 300ns
```

```
.probe
```

```
.end
```

```
*      Class CE Amplifier using an Ideal MESFET
```

```
*      Voltage Supply
```

```
Vcc         1      0      9V
```

```
Cbypass     1      0      100nF
```

```
*      Component Values
```

```
L(RFC)     1      2      74.7nH
```

```
C1         2      0      15pF
```

```
Co        2      5      3.7pF
```

```
Lo        5      6      11nH
```

```
R         6      0      4
```

```
*      Active Device - MESFET
```

```
B1         2      3      0      CE-MESFET
```

```
.model CE-MESFET gasfet(level=3)
```

```
*      Drive Circuitry
```

```
Vdrive     4      0      sin(-2.5 2.5 850e6 0 0 0)
```

```
Rdrive1    4      0      10k
```

```
E1         3      0      table {v(4,0)} [(-2.5,-2.5) (0,0)]
```

```
*      Analysis Commands
```

```
.tran 1ps 300ns
```

```
.probe
```

```
.end
```

A.3 HARMONIC BALANCE

The quote and information that follow is taken from a tutorial on nonlinear circuit analysis by Gilmore and Steer [1991]. "The harmonic balance method is a technique for the numerical solution of nonlinear analog circuits operating in a periodic, or quasi-periodic, steady-state regime. The method can be used to efficiently derive the continuous-wave response of numerous nonlinear microwave components including amplifiers, mixers, and oscillators. Its efficiency derives from imposing a predetermined steady-state form for the circuit response onto the nonlinear equations representing the network, and solving for the set of unknown coefficients in the response equation. Its attractiveness for nonlinear microwave applications results from its speed and ability to simply represent the dispersive, distributed elements that are common at high frequencies."

According to the Gilmore and Steer, the harmonic balance method offers several benefits over a SPICE[®] analysis. Among these are the capability to optimize circuits without lengthy repetitive analysis and the ability to accommodate large circuits without a substantial increase in the length of analysis. The harmonic balance method is both practical and efficient for performing steady-state analysis of circuits using a sinusoidal excitation, but transient analysis of amplitude modulation cannot be easily performed. A time-domain tool such as SPICE[®] would be required for transient analysis.

A.4 PSpice® NETLIST FOR THE CLASS F AMPLIFIER

The component values and device parameters for the following netlist are obtained from the article by Kopp and Pritchett [1989]. The active device parameters are taken from the measurements of a 1200 μm ion-implanted FET. A computer simulation using this netlist can be performed with PSpice® versions 5.0 and later.

```
*      Class F amplifier using an non-ideal MESFET at 10 GHz

*      Voltage Supply
Vcc      1      0      9V
Cbypass  1      0      10nF

*      Component Values
L(RFC)   1      2      16nH
Co       2      7      0.413pF
Lo       7      0      0.154nH
R        6      0      50

*      Active Device - MESFET
B1       2      3      0      F-MESFET
.model F-MESFET  gasfet(level=3 vto=-4.2V cgs=1.2pF
                  +cgd=0.55pF cds=0.33pF rs=0.87
                  + rg=1 rd=1)

*      Drive Circuitry
Vdrive   4      0      sin(-4.2 4.2 10e9 0 0 0)
Rdrive1  4      0      10k
E1       3      0      table {v(4,0)} [(-4.2,-4.2) (0,0)]

*      Analysis Commands
.tran    0.1ps 5ns
.probe
.end
```

LITERATURE CITED

- Bahl, I. J., E. L. Griffin, A. E. Geissberger, C. Andricos, and T. F. Brukiewa, (1989), Class-B Power MMIC Amplifiers with 70% Power-Added Efficiency, *IEEE Transactions on Microwave Theory and Techniques*, 37(9), 1315-1320.
- Basset, R. and M. D. McCombs, (1981), Production Bipolars Edge Out FETs at 4 GHz, *Microwaves*, 20(2), 43-46, 49.
- Browne, J., Senior Editor, (1987), RF Devices Gain Higher Power Levels, *Microwaves and RF*, 26(11), 148-153.
- Chudobiak, W. J., and D. F. Page, (1969), Frequency and Power Limitations of Class D Transistor Amplifiers, *IEEE Journal of Solid State Circuits*, SC-4(1), 25-37.
- Davis, W. A., (1992), private communication.
- Evans, A. D., Editor, (1981), *Designing With Field-Effect Transistors*, chapters 4, 5, and 7, McGraw-Hill, New York.
- Feldman, L., (1976), Class G High Efficiency HI-FI Amplifier, *Radio-Electronics*, 47(8), 47-49, 87.
- Feldman, L., (1977), Class-H Variproportional Amplifier, *Radio-Electronics*, 48(10), 53-55, 106.
- Geller, B. D., and P. E. Goettle, (1988), Quasi-Monolithic 4-GHz Power Amplifiers with 65-Percent Power-Added Efficiency, *IEEE MTT-S International Microwave Symposium Digest*, 835-838.

- Gilmore, R. J., and M. B. Steer, (1991), Nonlinear Circuit Analysis Using the Method of Harmonic Balance-A Review of the Art. Part I. Introductory Concepts, *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*, 1(1), 22-37.
- Granberg, H. O., (1989), FETs Versus BJTs: Making the Proper Choice for RF Power, *Microwaves and RF*, 28(8), 125-126, 128, 130, 132, 134, 135.
- Hakim, S. S., and R. Barrett, (1964), *Transistor Circuits in Electronics*, chapter 4, Hayden Books, New York, 105-144.
- Hall, L. C., and R. J. Trew, (1991), Maximum Efficiency Tuning of Microwave Amplifiers, *IEEE MTT-S International Microwave Symposium Digest*, 123-126.
- Hardy, J. K., (1979), *High Frequency Circuit Design*, Reston Publishing, Reston, VA, 279-306.
- Herman, K. J., and R. E. Zulinski, (1990), The Infeasibility of Zero-Current Switching Class E Amplifier, *IEEE Transactions on Circuits and Systems*, 37(1), 152-53.
- Higgins, J. A., (1991), GaAs Heterojunction Bipolar Transistors: A Second Generation Microwave Power Amplifier Transistor, *Microwave Journal*, 34(5), 176, 181, 183, 184, 186, 189, 191, 193, 194.
- Horowitz, P., and W. Hill, (1991), *The Art of Electronics*, Appendix G, Cambridge University Press, Cambridge.
- Kazimierczuk, M., and K. Puczek, (1987), Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cycle, *IEEE Transactions on Circuits and Systems*, CAS-34(2), 149-159.
- Kazimierczuk, M., and W. A. Tabisz, (1989), Class C-E High-Efficiency Tuned Power Amplifier, *IEEE Transactions on Circuits and Systems*, 36(3), 421-428.

- Khatibzadeh, M. A., and H. Q. Tserng, (1990), Harmonic Tuning of Power FETs at X-Band, *IEEE MTT-S International Microwave Symposium Digest*, 989-992.
- Kopp, W., and D. D. Heston, (1988), High-Efficiency 5-Watt Power Amplifier with Harmonic Tuning, *IEEE MTT-S International Microwave Symposium Digest*, 839-842.
- Kopp, W., and S. D. Pritchett, (1989), High Efficiency Power Amplification for Microwave and Millimeter Wave Frequencies, *IEEE MTT-S International Microwave Symposium Digest*, 857-858.
- Kovacs, F., (1981), High Frequency Application of Semiconductor Devices, chapters 2 and 19, Elsevier Scientific, Amsterdam.
- Krauss, H. L., C. W. Bostian, and F. H. Raab, (1980), *Solid State Radio Engineering*, chapters 12, 13 and 14, John Wiley & Sons, New York.
- Lee, W. C. Y., (1991), In Cellular Telephone, Complexity Works, *Circuits and Devices*, 26-32.
- Manz, B. (1988), Devices and Amps Raise Standards for Solid-State Power, *Microwaves & RF*, 27(10), 133-146.
- Neamen, D. A., (1992), *Semiconductor Physics and Devices*, chapter 10, Richard D. Irwin, Boston.
- Nishiki, S., and T. Nojima, (1987), Harmonic Reaction Amplifier-A Novel High-Efficiency and High-Power Microwave Amplifier, *IEEE MTT-S International Microwave Symposium Digest*, 963-966.
- Nishiki, S., and T. Nojima, (1988), High Efficiency Microwave Harmonic Reaction Amplifier, *IEEE MTT-S International Microwave Symposium Digest*, 1007-1010.

Nishiki, S., T. Nojima, and K. Chiba, (1987), High-Efficiency Quasimicrowave GaAs FET Power Amplifier, *Electronic Letters*, 23(10), 512-513.

Overstreet, W. P., (1986), *VHF Bipolar Transistor Power Amplifiers: Measurement, Modeling, and Design*, Virginia Polytechnic Institute and State University, Ph.D dissertation.

Pengelly, R. S., (1982), *Microwave Field-Effect Transistors-Theory, Designs, and Applications*, chapter 2, John Wiley & Sons, Great Britain.

Raab, F. H., (1976), FET Power Amplifier Boosts Transmitter Efficiency, *Electronics*, 49(12), 122-126.

Raab, F. H., (1977), Idealized Operation of the Class E Tuned Power Amplifier, *IEEE Transactions on Circuits and Systems*, CAS-24(12), 725-735.

Raab, F. H., (1978), Effects of Circuit Variations on the Class E Tuned Power Amplifier, *IEEE Journal of Solid State Circuits*, SC-13(2), 239-247.

Raab, F. H., (1986), Average Efficiency of Class-G Power Amplifiers, *IEEE Transactions on Consumer Electronics*, CE-32(2), 145-150.

Schneiderman, R., Senior Ed., (1991), In Search of a New Market, *Microwaves and RF*, 30(8), 33-42.

Snider, D. M., (1967), A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier, *IEEE Transactions on Electronic Devices*, ED-14(12), 851-857.

Sokal, N. O., and A. D. Sokal, (1975), Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers, *IEEE Journal of Solid State Circuits*, SC-10(3), 168-176.

Wang, Y. C., (1985), Comparison of MESFET, Bipolar Transistor, and Static Induction Transistor Class C Amplifiers, *International Journal of Electronics*, 59(1), 1-17.

ADDITIONAL READING

- Aleksanyan, A. A., V. A. Galakhov, and V. G. Moiseyev, (1989), Effect of Quasisaturation on the Switching of Bipolar Power Transistors, *Telecommunications and Radio Engineering*, 44(8), 81-83.
- Avratoglov, C. P. and N. C. Voulgaris, (1987), A New Method for the Analysis and Design of the Class E Power Amplifier Taking into Account the Q_L Factor, *IEEE Transactions on Circuits and Systems*, CAS-34(6), 687-691.
- Avratoglov, C. P. N. C. Voularis and F. I. Ioannidou, (1989), Analysis and Design of a Generalized Class E Tuned Power Amplifier, *IEEE Transactions on Circuits and Systems*, 36(8), 1068-1079.
- Chiba, K. and N. Kanmuri, (1983), GaAs FET Power Amplifier Module with High Efficiency, *Electronic Letters*, 19(24), 1025-1026.
- Geller, B. D., F. T. Assal, R. K. Gupta, and P. K. Cline, (1989), A Technique for the Maintenance of FET Power Amplifier Efficiency Under Backoff, *IEEE MTT-S International Microwave Symposium Digest*, 949-952.
- Kazimierczuk, M., (1981), Class E Tuned Power Amplifier with Shunt Inductor, *IEEE Journal of Solid-State Circuits*, SC-16(2), 2-7.
- Kazimierczuk, M., (1983), Effects of the Collector Current Fall Time on the Class E Tuned Power Amplifier, *IEEE Journal of Solid-State Circuits*, SC-18(2), 181-193.
- Kazimierczuk, M., and K. Puczko, (1989), Power-Output Capability of Class E Amplifier at Any Loaded Q and Switch Duty Cycle, *IEEE Transactions on Circuits and Systems*, 36(8), 1142-43.

- Kazimierczuk, M., and K. Puczko, (1989), Class E Tuned Power Amplifier with Antiparallel Diode or Series Diode at Switch, with Any Loaded Q and Switch Duty Cycle, *IEEE Transactions on Circuits and Systems*, 36(9), 1201-1209.
- Kazimierczuk, M., and X. T. Bui, (1990), Class E Amplifier with an Inductive Impedance Inverter, *IEEE Transactions on Industrial Electronics*, 37(2), 160-166.
- Raab, F. H., (1977), The Class BD High-Efficiency RF Power Amplifier, *IEEE Journal of Solid State Circuits*, SC-12(3), 291-298.
- Raab, F. H., (1986), Efficiency of Envelope-Tracking RF Power Amplifier System, *Proceedings RF Expo East, Nov. 10-12*, Boston, Mass., 303-311.
- Rogers, J. D., and J. J. Wormser, (1966), Solid-State High-Power Low-Frequency Telemetry Transmitters, *Proceedings of the National Electronics Conference*, 22, 171-176.
- Sampei, T., S. Ohashi, Y. Ohta, and S. Inoue, (1978), Highest Efficiency and Super Quality Audio Amplifier Using MOS Power FETs in Class G Operation, *IEEE Transactions on Consumer Electronics*, CE-24(3), 300-307.
- Smith, G. H., and R. E. Zulinski, (1990), An Exact Analysis of Class E Amplifiers with Finite DC-Feed Inductance at Any Output Q, *IEEE Transactions on Circuits and Systems*, 37(4), 530-534.
- Yngvesson, S., (1991), *Microwave Semiconductor Devices*, chapters 10 and 12, Kluwer Academic, Boston.
- Zulinski, R. E., and J. W. Steadman, (1987), Class E Power Amplifiers and Frequency Multipliers with Finite DC-Feed Inductance, *IEEE Transactions on Circuits and Systems*, CAS-34(9), 1074-1087.

VITA

Gary L. Kunselman was born in Natrona Heights, Pennsylvania. The first twenty-one years of his life were spent in nearby Ivywood where he gained much appreciation for mowing grass, splitting firewood, and playing music. For the latter, he owes unlimited gratitude to his father for teaching him how to play guitar and sing harmony. His father is also responsible for nurturing an interest in amateur radio and electronics.

Upon completing an associates degree in electronics at Penn Technical Institute, Mr. Kunselman accepted employment with the IBM Corporation in Manassas, Virginia. An educational leave of absence was used to pursue the Bachelor of Science (1991) and Master of Science (1993) degrees in Electrical Engineering at Virginia Tech. Mr. Kunselman will return to IBM in Burlington, Vermont at the conclusion of his studies.

Learning has been and will continue to be a priority in his life. The formal education he has received is greatly appreciated, but he is well aware that the practical education continues indefinitely. By the grace of God, he'll survive that too.

Gary L. Kunselman