Novel DC/DC Converters For High-Power Distributed Power Systems

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Novel DC/DC Converter for High-Power Distributed Power Systems

By

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Electrical and Computer Engineering

(Abstract)

One of the requirements for the next generation of power supplies for distributed power systems (DPSs) is to achieve high power density with high efficiency.

In the traditional front-end converter based on the two-stage approach for high-power three-phase DPSs, the DC-link voltage coming from the power factor correction (PFC) stage penalizes the second-stage DC/DC converter. This DC/DC converter not only has to meet the characteristics demanded by the load, but also must process energy with high efficiency, high reliability, high power density and low cost. To meet these requirements, approaches such as the series connection of converters and converters that reduce the voltage stress across the main devices have been proposed.

In order to improve the characteristics of these solutions, this dissertation proposes high-efficiency, high-density DC/DC converters for high-power high-voltage applications.

In the first part of the dissertation, a DC/DC converter based on a three-level structure and operated with pulse width modulation (PWM) phase-shift control is proposed. This new way to operate the three-level DC/DC converter allows soft-switching operation for the main devices. Zero-voltage switching (ZVS) and zero-voltage and zero-current switching (ZVZCS) soft-

switching techniques are studied, analyzed and compared in order to improve the characteristics of the proposed converter. This results in a series of ZVS and ZVZCS three-level DC/DC converters for high-power high-voltage applications. In all cases, results from 6kW prototypes operating at 100 kHz are presented.

In addition, with the ultimate goal of improving the power density of the DC/DC converter, a study of several resonant DC/DC converters that can operate at higher switching frequencies is presented. From this study, a three-element ZVS three-level resonant converter for applications with wide input voltage and load variations is proposed. Experimental results at 745 kHz obtained without penalizing the efficiency of the PWM approaches are presented.

The second part of the dissertation proposes a quasi-integrated AC/DC three-phase converter that aims to reduce the complexity and cost of the traditional two-stage front-end converter. This converter improves the complexity/low-efficiency tradeoff characteristics evident in the two-stage approach and previous integrated converters. The principle of operation for the converter is analyzed and verified on a 3kW experimental prototype.

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Dear father, you are going to be in my heart all my life, this dissertation is your accomplishment as much as it is mine.

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To God, for all blessings that He has given me.

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1. Introduction

Due to the IEC61000-3-2 Class A standard, the new generation of three-phase distributed power systems (DPSs) for high-power applications must provide power factor correction (PFC) in order to reduce the total harmonic distortion (THD) injected into the utility line [1]-[3].

Nowadays, the common approach used by industry to meet this requirement consists of a two-stage approach. The first stage, the power factor corrector, is implemented by three single-phase power factor correctors [4]. Each PFC converter is followed by an isolated DC/DC converter (Fig. 1-1), which provides the necessary requirements for the load. The use of isolated DC/DC converters feeding the same load not only eliminates the possibility of interaction between modules but also allows the converter to work under unbalanced and distorted input-phase voltages. Despite its good performance, this approach turns out to be complex and expensive due to the high number of components.

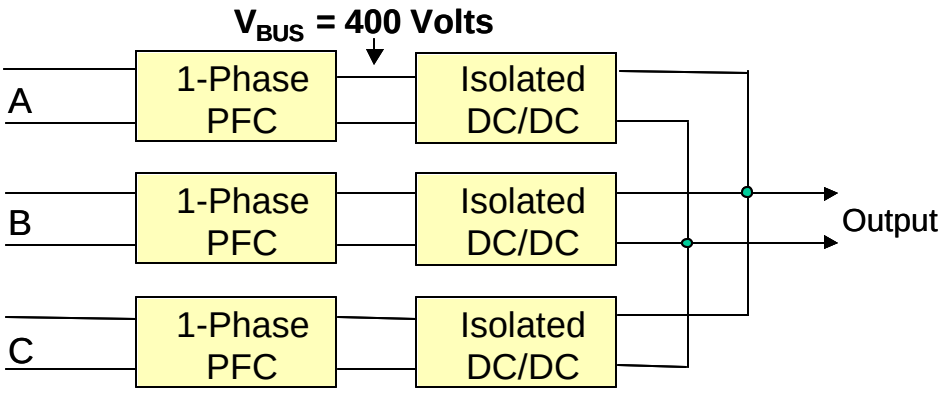


Fig. 1-1. DPS approach for high-power applications using three single-phase PFC converters.

Fig. 1-2 presents another two-stage DPS approach based on the use of three single-phase PFC converters [5]. In this approach, the outputs of the PFC converters are connected, reducing the low-frequency input power fluctuation in the high-voltage DC link. Therefore, the requirements

for the value of the bulk capacitor are minimized. In addition, the second stage can be implemented with only one isolated DC/DC converter. It is important to mention that the simplification in this approach is penalized by interaction between the stages. In order to minimize this interaction, the boost inductor in each stage is split in two, and an additional freewheeling diode is added. In addition, the DC-link voltage should be at least twice the peak input voltage, which increases not only the voltage stress across the devices in the PFC stages, but also that in the devices of the isolated DC/DC second-stage converter.

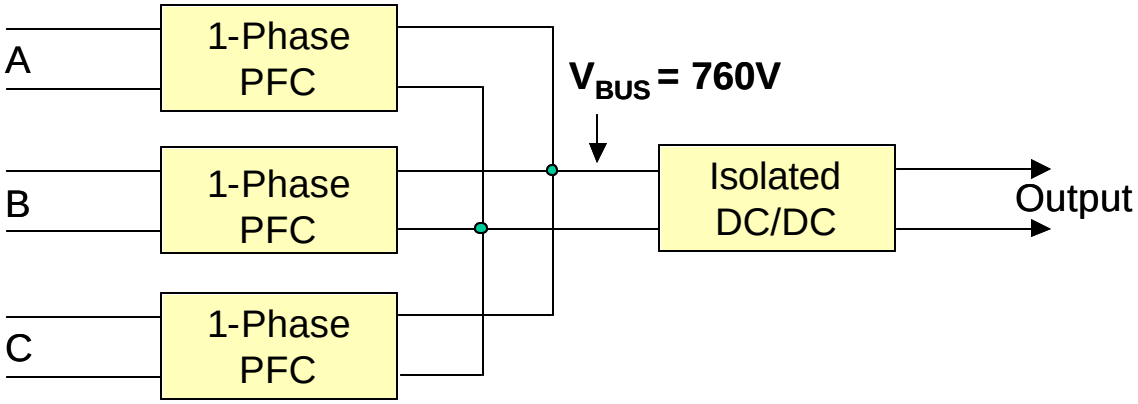


Fig. 1-2. Simplified DPS approach for high-power application.

Another alternative for implementing the front-end converter in high-power DPS systems is achieved by using a three-phase rectifier as a PFC stage [6]. Among the three-phase rectifiers, the six-switch boost topology is able to achieve the best performance in terms of shaping the input currents and presenting bi-directional power flow capability [6]-[10]. In addition, this converter presents low input and output filter requirements, which reduces the weight and volume of the overall system. However, due to the high bus voltage related to the boost-type rectifier, it is necessary to use IGBT devices, as shown in Fig. 1-3. Due to their turn-off losses, the use of IGBT devices limits the switching frequency to well below 40 kHz. To improve the efficiency of the six-switch boost rectifiers, several soft-switching schemes and lossless snubbers

have been presented [10]-[12]. The increase of the circuit and control complexity has made this structure expensive and difficult to accept in some industry applications. In addition, similar to the previous approach, the DC-link voltage imposes a high-voltage stress on the DC/DC converter.

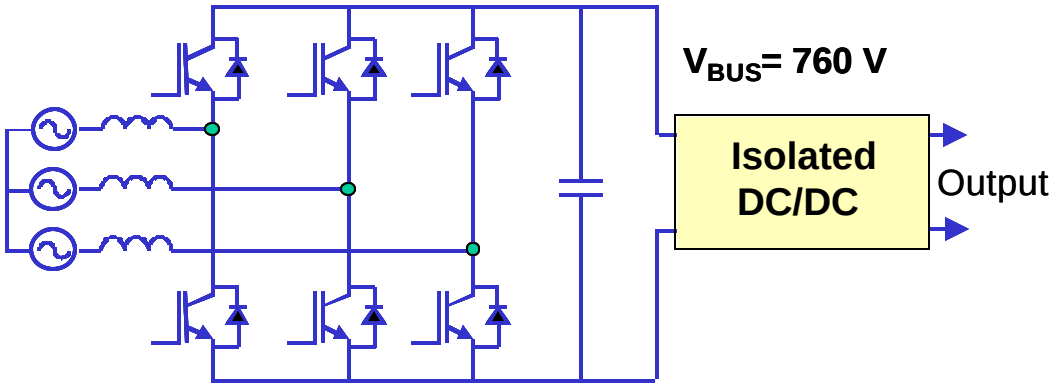


Fig. 1-3. DPS approach for high-power application using the three-phase six-switches boost rectifier as a PFC converter.

In DPS for telecom applications, the bi-directionality of the PFC converter is not necessary. Therefore, the six-switch three-phase boost rectifier can be simplified. Taking this into account, another converter recently getting a lot of attention for the implementation of the PFC converter, also in a two-stage DPS approach, is presented in [13]. The VIENNA rectifier, as it is called, presents low harmonic distortion and high efficiency in addition to simplification in the PFC stage. In addition, the three-level operation results in a lower RMS value for the mains current, which results in a reduction of the value of the input inductance when compared with the six-switch boost rectifier [13]. However, for proper operation, the DC-link voltage still needs to be twice the level of the line-to-neutral input voltage. Different from the previously mentioned DPS approach, the voltage stress across the devices in the PFC converter is minimized by the connection in the middle point of the split bus capacitors, as shown in Fig. 1-4. However, the devices in the DC/DC second-stage converter still suffer high voltage stress.

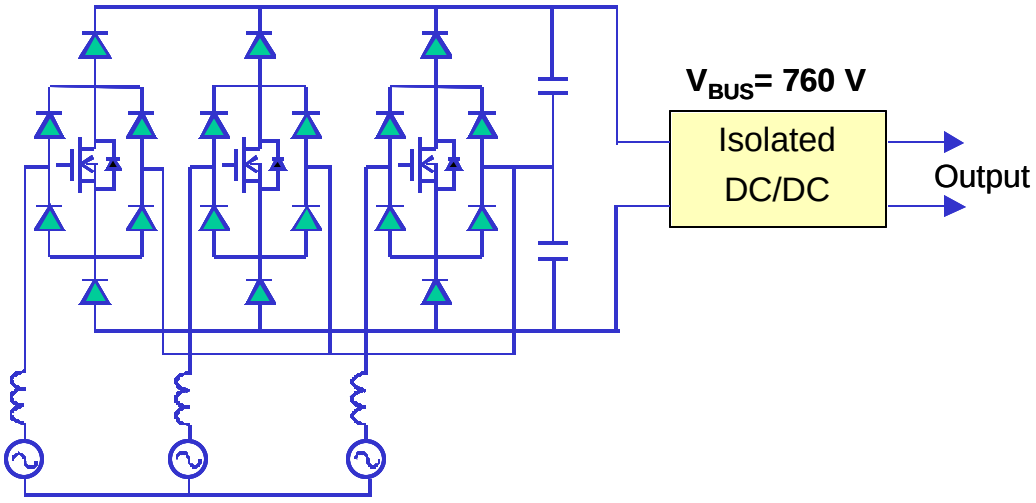


Fig. 1-4. Simplification of the DPS for high-power application by using the VIENNA rectifier as a PFC converter.

The three-phase single-switch boost rectifier is another interesting option for the implementation of the PFC stage, since it can comply with the aforementioned standard with simplicity, efficiency, reliability and low cost [14]. However, in order to reduce the harmonic distortion in the three-phase boost rectifier, its output voltage must be significantly increased with respect to the input voltage [15]-[19]. This increase in the output voltage also increases the voltage stress across the devices in the DC/DC step-down second-stage converter.

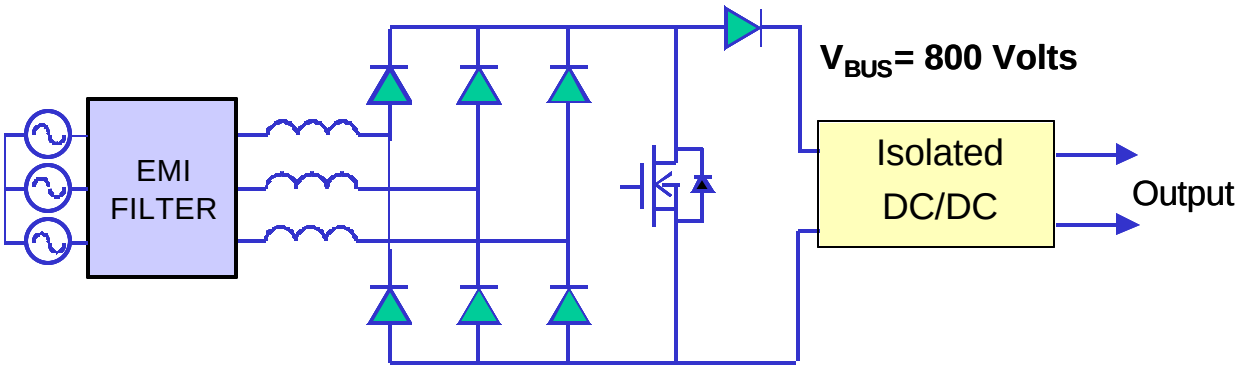


Fig. 1-5. DPS approach for high-power application using the three-phase single-switch boost rectifier as a PFC converter.

1.1. Benefits of Three-Level DC/DC Converters in High-Power DPSs

As can be seen, the increased voltage stress in the DC link is one of the problems commonly associated with the reduction of the complexity and cost of the DPS for high-power applications.

At this power level (6 kW), the second-stage DC/DC converter is usually implemented with a full-bridge topology, as shown in Fig. 1-6. The operation of this converter with phase-shift control allows the use of the leakage inductance of the transformer to achieve zero-voltage switching (ZVS) operation for the main devices [35]-[38].

One of the drawbacks that these converters present is that to maintain ZVS for a wide load range, an additional resonant inductance must be included. This in turn increases the circulating energy, which increases the conduction losses in the converter. In addition, both a reduction in the effective duty cycle and a severe secondary parasitic ringing occur.

The problem of the circulating energy in the ZVS full-bridge DC/DC converter becomes even worse when hold-up time is a requirement. For this kind of application and at this power level, the front-end converter should be able to operate for at least 10 ms with an absence of the utility lines. The usual approach to meet this requirement without increasing the cost and the volume in the front-end converter consists of designing the output capacitor of the PFC converter in such a way that it can store more energy. In addition, the DC/DC converter should be designed to operate with a wide input-voltage range. This requirement penalizes the DC/DC converter with an even higher circulating energy, since the converter should be able to handle wide input-voltage variations, thus minimizing the duty cycle at nominal input voltage.

A lot of research has been done to improve the characteristics and performance of the full-bridge DC/DC converter with phase-shift control, and this topology has become quite popular for use in high-power applications where isolation is a requirement [39]-[60]. This research has resulted in improvements of the original ZVS operation [39]-[46] and zero-voltage and zero-current switching (ZVZCS) techniques [47]-[60], which intend to eliminate this major limitation presented by the ZVS techniques.

Despite its improvements related to soft-switching operation, one of the disadvantages that this topology presents in high-voltage applications is that each switch in the full-bridge DC/DC converter is subjected to the full bus voltage. In this voltage range, MOSFET devices with a high r_{dson} may be used. This approach increases the conduction losses of the DC/DC converter. Another option for this power range is to use IGBT devices; however, the switching frequency, and consequently the power density of the converter, must be reduced.

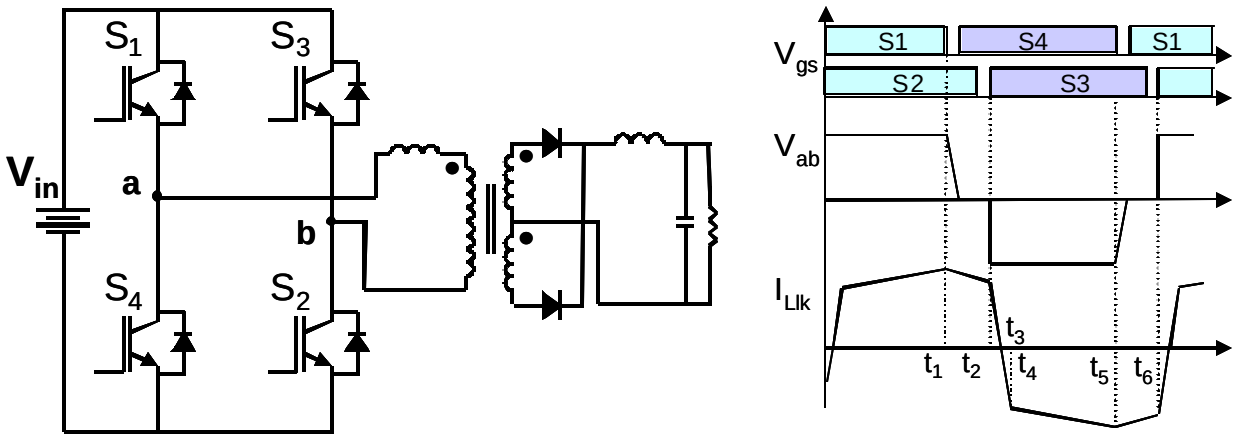


Fig. 1-6. Traditional ZVS full-bridge DC/DC converter with phase-shift control.

The series connection of converters has been proposed to solve the voltage stress across the main devices in high-voltage applications [30]-[34]. Fig. 1-7 shows this scheme using two full-bridge DC/DC converters in which the input sides of the converters are connected in series to

reduce the voltage stress across the main devices to half the level of the input voltage [32], [33]. By doing this, low-voltage-rating devices can be used, and also the soft-switching characteristic of the converters is maintained. However, an additional control strategy to balance the input voltage across the input capacitors should be used to compensate for any mismatch in the operation of the converters. Besides the complexity in the control, this approach turns out to be an expensive solution due to the high number of components.

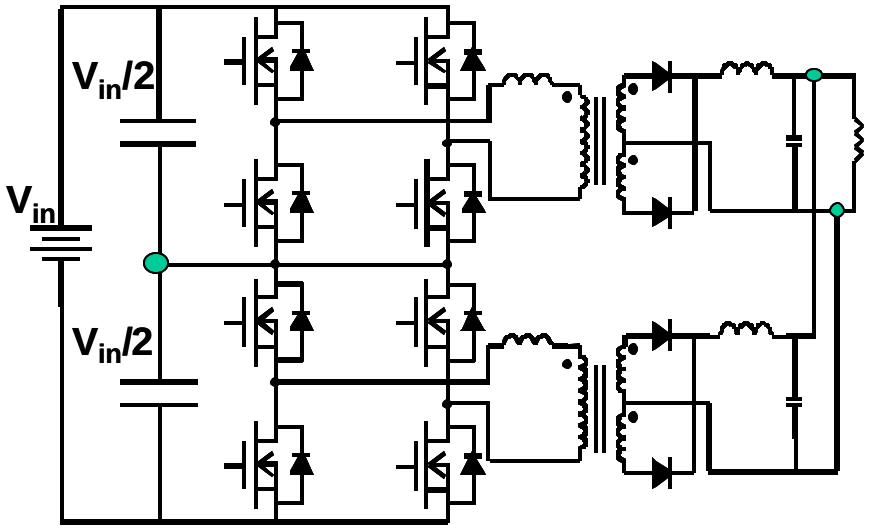


Fig. 1-7. Series connection of DC/DC converters for reduction of the voltage stress across the main devices.

In order to minimize the complexity of the previous approach, it has been proposed converters base on structures that reduce the voltage stress across the main devices [21]. The series of ZVS three-level DC/DC converters [21]-[25] and the dual-bridge DC/DC converter [26]-[29] shown in Fig. 1-8 are some examples. These DC/DC converters reduce the voltage stress across the power switch to half the level of the input voltage. Also, these converters achieve ZVS for the primary switches, which is a condition necessary for increasing the efficiency of the converter. The problem of the input-voltage imbalance presented by the series-connection of converters is minimized since the operation of these converters is based on just one control.

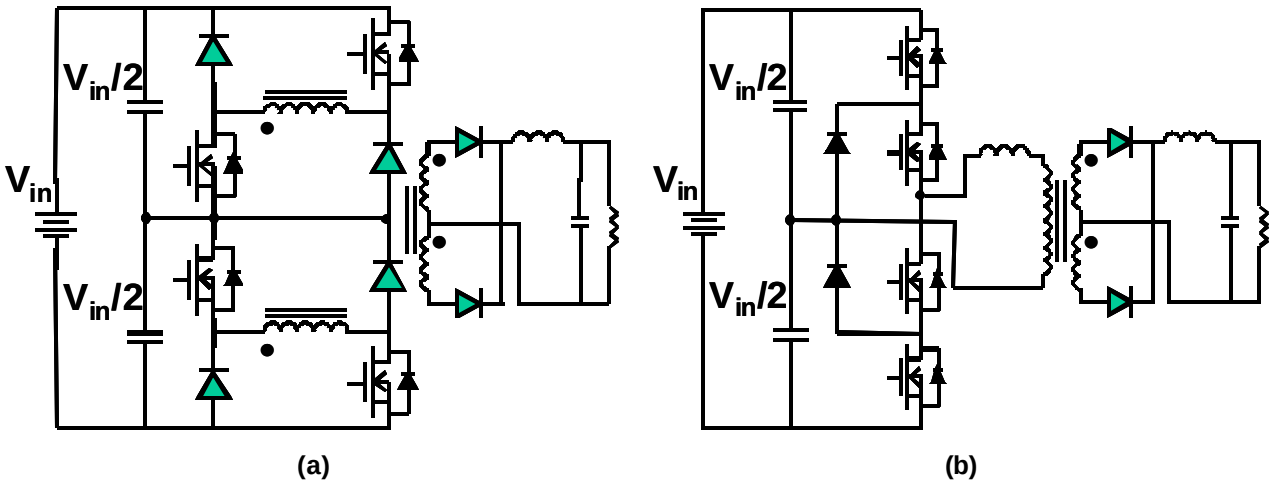


Fig. 1-8. DC/DC converters that allow reduction of the voltage stress across the main devices: (a) dual-bridge DC/DC converter and (b) three-level DC/DC converter.

In order to see the benefits of using low-voltage devices, Fig. 1-9 presentsa theoretical efficiency comparison between a full-bridge DC/DC converter and a three-level DC/DC converter used as the second stage of a DPS for high-power applications. For this comparison, the input voltage of the DC/DC converter is set to be 800 V. In addition, both converters were designed to operate at 100KHz switching frequency and to provide an output voltage of 50 V. These efficiency curves were calculated considering just the switching and conduction losses for the primary devices and the conduction losses in the secondary devices. For the full-bridge converter, the efficiency was calculated using MOSFET and IGBT devices. In the first case, a 1200V, 26A MOSFET (APT12040JVR) was selected as the primary-side device. In the second case, 1200V, 24A IGBT (IRG4PH50U) devices were selected. And for the three-level DC/DC converter, a 600V, 62A MOSFET (APT60M75JVR) was selected. It is important to mention that all devices allow a 50% voltage margin and are the best in their respective voltage ratings. In addition, a soft-switching technique was implemented in order to reduce the switching losses in the primary-side devices.

Although the new generation of IGBT devices allows higher-switching-frequency operation with reduced switching losses, their benefit is still limited for applications below 40 kHz. At 100 kHz, the switching losses are still dominant despite the use of soft-switching techniques, and therefore this converter has the lowest efficiency in this comparison. For the rest of the comparison, the use of low-voltage-rating devices in the three-level DC/DC converter allows a 1% efficiency improvement at full-load condition. This improvement occurs because the 600V device presents better electrical characteristics (conduction and switching losses) when compared with the 1200V devices.

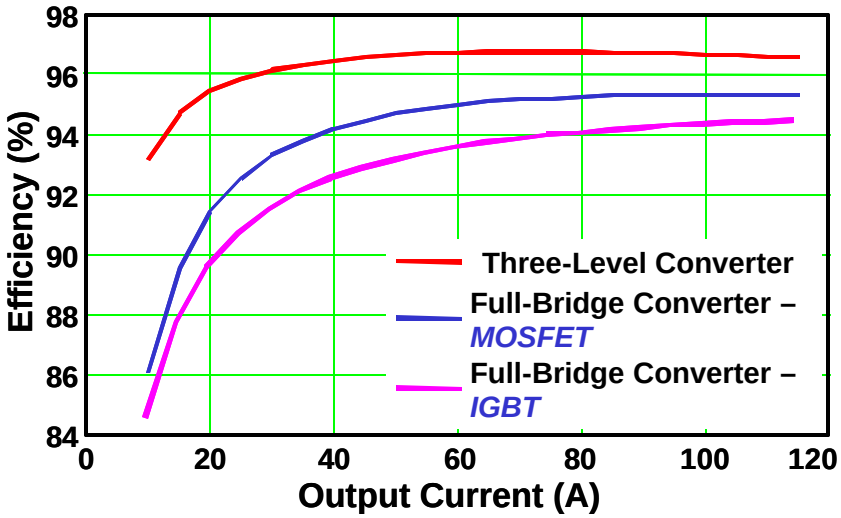


Fig. 1-9. Theoretical efficiency comparison between the three-level DC/DC converter and the full-bridge DC/DC converter for an 800V DC-link voltage using the load current as a running parameter.

1.2. Benefits of Three-Level DC/DC Converter for Power Density Requirements in the High-Power DPS

The next generation of power supplies not only has to meet the characteristics demanded by the load, but also must process energy with high efficiency, high reliability, high power density and low cost. In order to achieve converters with high power densities, it is usually required that they operate at higher switching frequencies.

As switching frequencies increase, the switching losses associated with the turn-on and turn-off of the devices also increase. In switch-mode PWM power supplies, the switching losses can be high enough to prohibit the operation of the power supply at very high frequencies, even when soft-switching techniques are used. In resonant-mode power supplies, however, the switching losses can be lower, allowing the resonant converter to operate at higher frequencies [67]. Therefore, the use of resonant converters remains an interesting option for some applications requiring the previous specifications.

In resonant converters, MOSFET devices are appropriate for high switching frequencies, and ZVS is especially recommended. The conventional series resonant converter operates with ZVS for the active devices when the switching frequency is above the resonant frequency. However, for wide input-voltage and output-load variations, the converter has to operate with wide switching frequency variations, which complicates optimization of the converter.

Some fixed-frequency control strategies have been proposed for resonant converters [61]-[75]; these permit the optimization of the converter's magnetics, as well as its input and output filters. However, in order to achieve ZVS for a wide load variation, the converter must operate with a switching frequency much higher than the resonant frequency of the tank [75], which results in large circulating energy, reduces the efficiency, and requires high-power-rating devices.

In addition, for high-input voltage, as exists in high-power DPSs for three-phase applications, the necessity of high-voltage-rating devices makes the problem even worse. It has been shown in the previous section that three-level structures can alleviate this problem by reducing the voltage stress across the power switches to half the level of the input voltage. Therefore, MOSFET devices with better characteristics can be used.

Fig. 1-10 shows again the efficiency comparison between the full-bridge and the three-level DC/DC converters at different switching frequencies. These efficiency curves were calculated considering just the switching and conduction losses for the primary devices and the conduction losses in the secondary devices. For this comparison, the input-output specifications for the second-stage DC/DC converter are as follows: 800V input voltage, 50V output voltage and 115A output current. For the primary devices, a new generation of MOSFET devices was selected, which combines lower conduction and switching with exceptionally fast switching speed. This reduction of the losses is achieved by reducing the R_{dson} and Q_g. For the full-bridge DC/DC converter, a 1,000V, 30A MOSFET device (APT10026JLL) was selected. This device was selected (instead of one with a 1,200V rating) because it presents better electrical characteristics. For the three-level DC/DC converter, a 600V, 58A MOSFET (APT60M75JLL) was selected.

As can be seen, the three-level DC/DC converter provides a significant improvement in efficiency at higher switching frequencies. This improvement is achieved because the device used in the three-level DC/DC converter offers better switching characteristics, meaning lower gate-drain ("Miller") charge Q_{gd}, reverse transfer capacitance C_{rss}, and fall time t_f (98 nC, 108 pf and 8 ns, respectively) when compared with the device used in the full-bridge DC/DC converter (196 nC, 252 pf and 9 ns). Taking into account these results, the three-level DC/DC converter also becomes an interesting option when higher switching frequencies are required to increase the power density of the DPS.

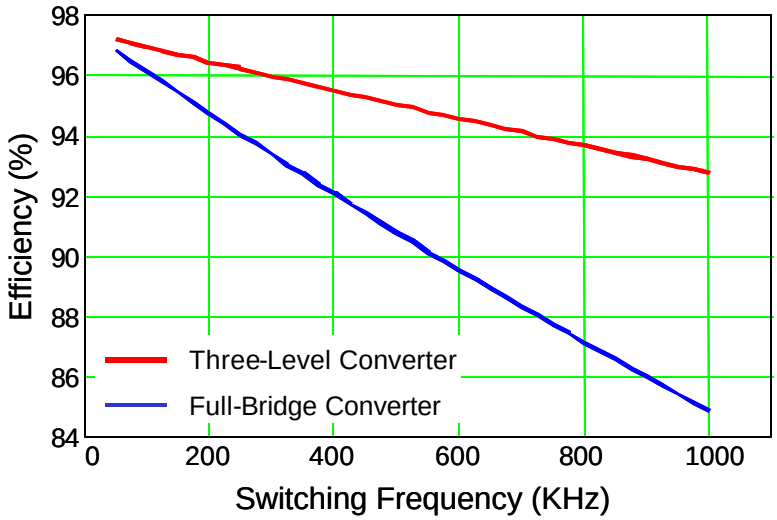


Fig. 1-10. Theoretical efficiency comparison between the three-level DC/DC converter and the full-bridge DC/DC converter for an 800V DC-link voltage using the switching frequency as a running parameter.

1.3. Benefits of the Three-Level DC/DC Converter in the Simplification of the High-Power DPS

Integrated converters have also been proposed to further reduce the complexity and cost of the high-power DPS without reducing the performance of the system. In these integrated converters, the PFC and DC voltage regulation are provided in a single structure of power conversion. A single-switch integrated converter based on a flyback structure has been proposed [86]-[87]. This converter is composed of three independent flyback converters working in discontinuous conduction mode (DCM) and sharing one power switch. Due to this configuration, the converter becomes an interesting option for three-phase applications, as it provides low harmonic distortion as well as isolation. However, its applicability is reduced to very-low-power applications.

Other single-switch integrated converters have been proposed [87]-[90], as derived from quasi-resonant and multi-resonant buck topologies. In these cases, the resonant elements are used not only to provide soft-switching commutation for the main devices but also to achieve input

currents with low harmonic distortion. Despite their good performance at higher-power levels, these topologies could have restrictions for use in high-power DPS applications due to their lack of galvanic isolation.

Fig. 1-11 shows an integrated converter based on the phase-shift full-bridge converter [92]. Similar to the single-switch three-phase boost converter, this converter achieves low harmonic distortion in the input current by working in DCM operation. In addition, the use of four switches allows the applicability of the converter at higher power levels. Also, the phase-shift control maintains simplicity in the operation of this converter as well as ZVS operation for all its main devices. One of its disadvantages is that in order to balance the input and output power, the voltage in the intermediate bus capacitor fluctuates according to the input-voltage and output-load variations, imposing additional high-voltage stress on the power devices. Therefore, in 220V line-to-neutral applications, high-voltage-rating devices with bad electrical characteristics must be used, which reduces the efficiency of the converter.

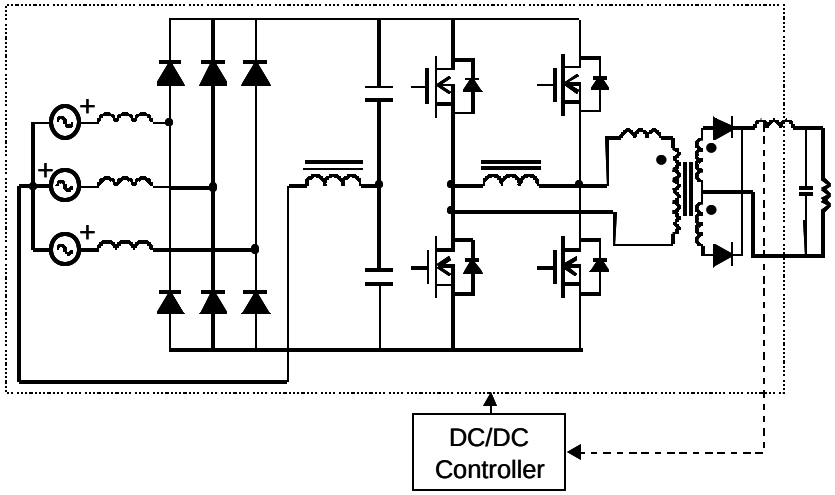


Fig. 1-11. Integrated converter based on a full-bridge structure.

The problem of high-voltage stress across the main devices can be minimized by using a three-level structure in the integrated converter [96]-[97], as can be seen in Fig. 1-12. In this way, low-voltage-rating MOSFET devices with better electrical characteristics can be used, improving the efficiency of the converter. Similar to the previous approach, the simplicity in the operation of the converter and the ZVS operation for the main devices are achieved by using phase-shift control. It is important to mention that the low harmonic distortion in the input current is also achieved by operating the input inductors in DCM. However, the THD is lower than that of the single-switch three-phase boost rectifier.

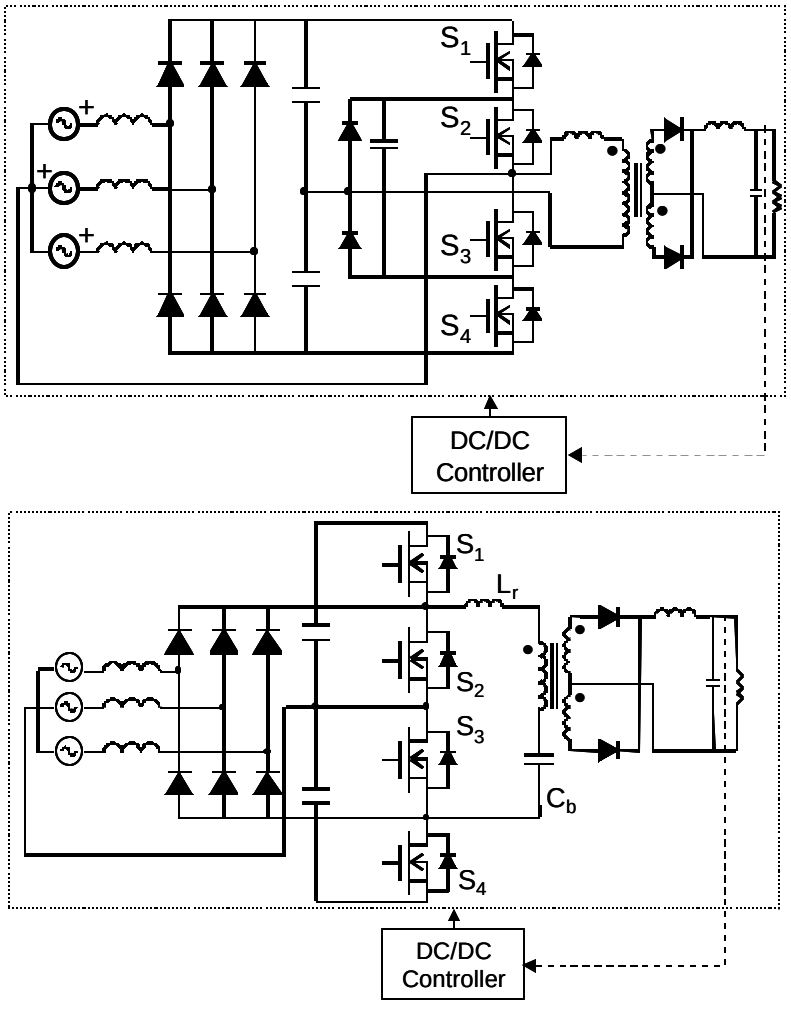


Fig. 1-12. Integrated converters based on a three-level structure.

1.4. Dissertation Proposal and Objectives

The main objective of this dissertation is to develop high-efficiency, high-density DC/DC converters for high-power DPSs. Toward this end, the dissertation proposes the following approach:

- Study of the use of low-voltage devices in high-voltage DC/DC applications by using a three-level structure;
- Study and proposal of soft-switching techniques for three-level DC/DC converters;
- Study and proposal of a DC/DC converter that operates in the megahertz range in order to increase the power density of the DPSs;
- Proposal of integrated converters to reduce the cost and complexity of the DPS.

In order to meet the outlined goal, the dissertation addresses these issues as follows. Section 1 presents a novel approach for implementing soft-switching techniques in the three-level DC/DC converter. By adding an auxiliary capacitor in the primary side [94], [99], the proposed three-level DC/DC converter operates with phase-shift control and achieves ZVS operation for all the switches. It is important to mention that by operating the converter with a phase-shift control, the control and the gate drivers are simplified. Furthermore, the operation with phase-shift control allows the implementation of soft-switching techniques, previously proposed for the full-bridge converter, to be used in the proposed three-level DC/DC converter. Based on this characteristic, this section also presents the study, implementation and comparison of improvements to the proposed ZVS three-level DC/DC converter. These improvements overcome the drawbacks that exist in conventional ZVS three-level converters, such as high circulating energy, severe

parasitic ringing on the rectifier diodes, and limited ZVS load range for the inner switches. These improvements are based on ZVS operation [99] and ZVZCS operation for the primary switches [94] [95] [100] [107] [113].

With the ultimate aim of increasing the power density of the DPS, Section 2 presents the study of resonant DC/DC converters that are able to operate at high switching frequencies. From this study, a ZVS three-level DC/DC resonant converter for high input voltage and wide load variations is proposed. The operation of the converter at both fixed and variable frequencies is discussed. In both operating modes, the proposed converter can operate with a wide ZVS range by using the magnetizing inductance of the transformer. For the fixed-frequency operating mode, the control takes place in the secondary side of the transformer, which helps to increase the ZVS range and also reduces the circulating energy in the converter. In addition, an alternative is presented to reduce the effect of wide input-voltage variations in the performance of the converter [110] [112], [114]. The principle of operation of the converter is analyzed and verified on a 2.75kW, 745kHz experimental prototype.

In order to reduce the cost of the DPS, Section 3 of this dissertation presents a quasi-integrated AC/DC three-phase converter, which improves the complexity / low-efficiency tradeoff characteristics as compared with the previously discussed DPS approaches. The proposed converter presents a low number of components, low THD, as compared with the single-switch boost rectifier, fast regulation, and improvement in efficiency with a simple control. The proposed converter also offers the advantage of reducing the voltage stress across the switches. In addition, it is demonstrated that a soft-switching technique can be implemented in the proposed converter without adding complexity [106].

2. Soft-Switching Techniques for the PWM Three-Level DC/DC Converter

2.1. Introduction

One of the problems commonly associated with the reduction of the complexity and cost of the DPS for high-power applications is the high voltage stress in the second-stage DC/DC converter. As discussed before, the use of structures that allow a reduction of the voltage stress across the main devices minimizes this problem. This section of the dissertation discusses the implementation of soft-switching techniques in the three-level DC/DC converter using the well-known phase-shift control. In this way, a simplification of the control and gate drivers is achieved. In addition, this new soft-switching implementation for three-level DC/DC converters helps to balance the voltage across the DC input capacitors under an abnormal operation of gate-signal mismatch.

2.2. ZVS Three-Level DC/DC Converter with PWM Control

Fig. 2-1 shows the ZVS three-level DC/DC operated with PWM control [22]. As can be seen, the primary side of the converter is based on a neutral-point clamped (NPC) structure, which has been widely used in inverter circuit topologies for high-power applications [20]. This is also known as a three-level diode-clamped structure, since the voltage generated in the terminals a and b, V_{ab} has three levels: $V_{in}/2$, 0 and $-V_{in}/2$. To generate this voltage, the input voltage is split into three levels by the input capacitors C_{in1} and C_{in2}. In addition, the diodes D_{c1} and D_{c2} clamp the voltage across the switches to half the level of the input voltage. To provide isolation, which

is a necessary requirement for DC/DC converters, the load is connected through the transformer that is located in terminals a and b.

In this modulation scheme, the inner switches S_2 and S_3 operate with a fixed duty cycle of nearly 50 %. To regulate the output voltage, the pulse width for the outer switches S_1 and S_2 varies. In this way, when S_1 and S_2 are on, half of the input voltage is applied to the transformer and the input power is delivered to the output.

Similar to the full-bridge converter operated with phase-shift control, this converter uses either the leakage inductance of the transformer or an external inductance to achieve ZVS for the primary switches. In order to improve the ZVS characteristics of the converter for a wide load range, several modifications of the converter have been proposed [23]-[25].

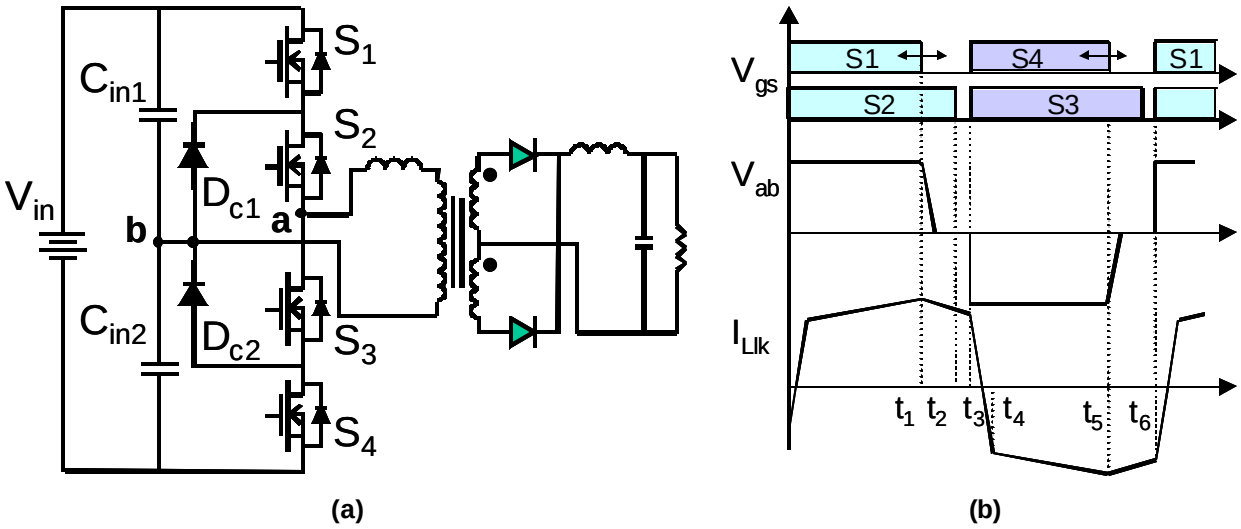


Fig. 2-1. (a) ZVS three-level DC/DC converter with PWM control and (b) its main waveforms.

As can be seen, this modulation scheme imposes additional complexity in order to generate the control signals and implement the gate drivers. In addition, it is difficult to improve the

characteristics of the converter by using other soft-switching technique such as the ZVZCS operation previously proposed for full-bridge converter with phase-shift control.

The next section proposes the operation of the converter with a phase-shift control in order to minimize the main disadvantages presented by this ZVS three-level DC/DC converter with PWM control. As will be shown in the next chapter, the phase-shift operation in this converter improves the soft-switching characteristic of the converter by using not only ZVS techniques but also ZVZCS.

2.3. Proposed ZVS Three-Level DC/DC Converter with Phase-Shift Control

A novel ZVS three-level DC/DC converter is presented in this part of the dissertation. The proposed converter and the timing diagram are shown in Fig. 2-2. It can be seen that the basic structure is very similar to that of the ZVS three-level converter proposed in other work [22]. The main difference is the inclusion of the flying capacitor C_{ss}, which uses phase-shift control to allow true ZVS operation for all switches.

In order to simplify the analysis of the converter, it is assumed that the circuit operates in steady state, the output filter inductor is large enough to be considered as a current source, all the devices are ideal, and the transformer magnetizing current is ignored.

The proposed converter has six stages of operation during each half of a switching cycle. As was mentioned before, the circuit uses the well-known phase-shift control in which all switches operate with nearly 50% duty cycles. The phase shift between S_1 and S_2 or S_3 and S_4 determines the operating duty cycle of the converter. The equivalent circuit for each stage of operation is shown in Fig. 2-3. These stages are described as follows.

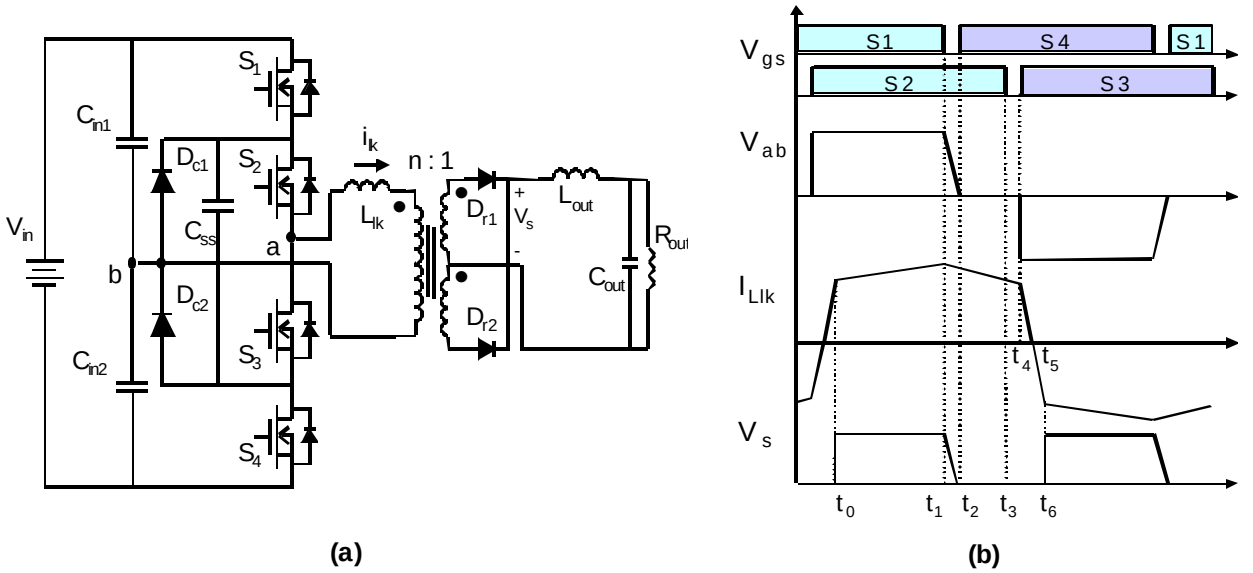


Fig. 2-2. (a) The proposed ZVS Three–Level DC/DC converter and (b) its main waveforms.

[t_0-t_1]: During this stage, switches S_1 and S_2 conduct, and the input power is delivered to the output.

[t_1-t_2]: At t_1, switch S_1 is turned off, and the load current charges and discharges the parasitic capacitance of S_1 and S_4 through flying capacitor C_{ss}. This stage ends when the voltage across the parasitic capacitance of S_1 reaches $V_{in}/2$ and clamping diode D_{c1} begins to conduct. At the same time, the voltage across the parasitic capacitance of S_4 reaches zero, and the anti-parallel diode D_4 begins to conduct.

[t_2-t_3]: After D_4 starts conducting, switch S_4 can be turned on with ZVS. The primary current freewheels through clamping diode D_{c1} and switch S_2. In the secondary side, the output current freewheels through diode rectifiers D_{r1} and D_{r2}.

[t_3-t_4]: At t_3, switch S_2 is turned off, and leakage inductance L_{lk} resonates with parasitic capacitances C_2 and C_3. The voltage across C_2 rises up to half the level of input voltage V_{in}, and the voltage across C_3 decreases to zero to turn on the anti-parallel diode D_3.

[t_4-t_5]: During this interval, half of the input voltage is applied to the primary side of the transformer, and the current in the leakage inductance starts to decrease. The anti-parallel diodes of S_3 and S_4 conduct the current of the primary side. Therefore, switch S_3 can be turned on with ZVS.

[t_5-t_6]: At t_5, the primary current reverses its polarity and starts to flow through switches S_3 and S_4. The primary current increases with a slope equal to $V_{in}/(2L_{lk})$. At the end of this stage, the primary current reaches the reflected output current, and a new half of a switching cycle begins.

2.3.1. Design Consideration

This section of the dissertation presents some important considerations for the design of the proposed ZVS three-level DC/DC converter.

As previously mentioned, the inclusion of flying capacitor C_{ss} in the primary side allows the proposed converter to operate with phase-shift control. In this way, the design considerations are very similar to those of the full-bridge converter with ZVS operation [38].

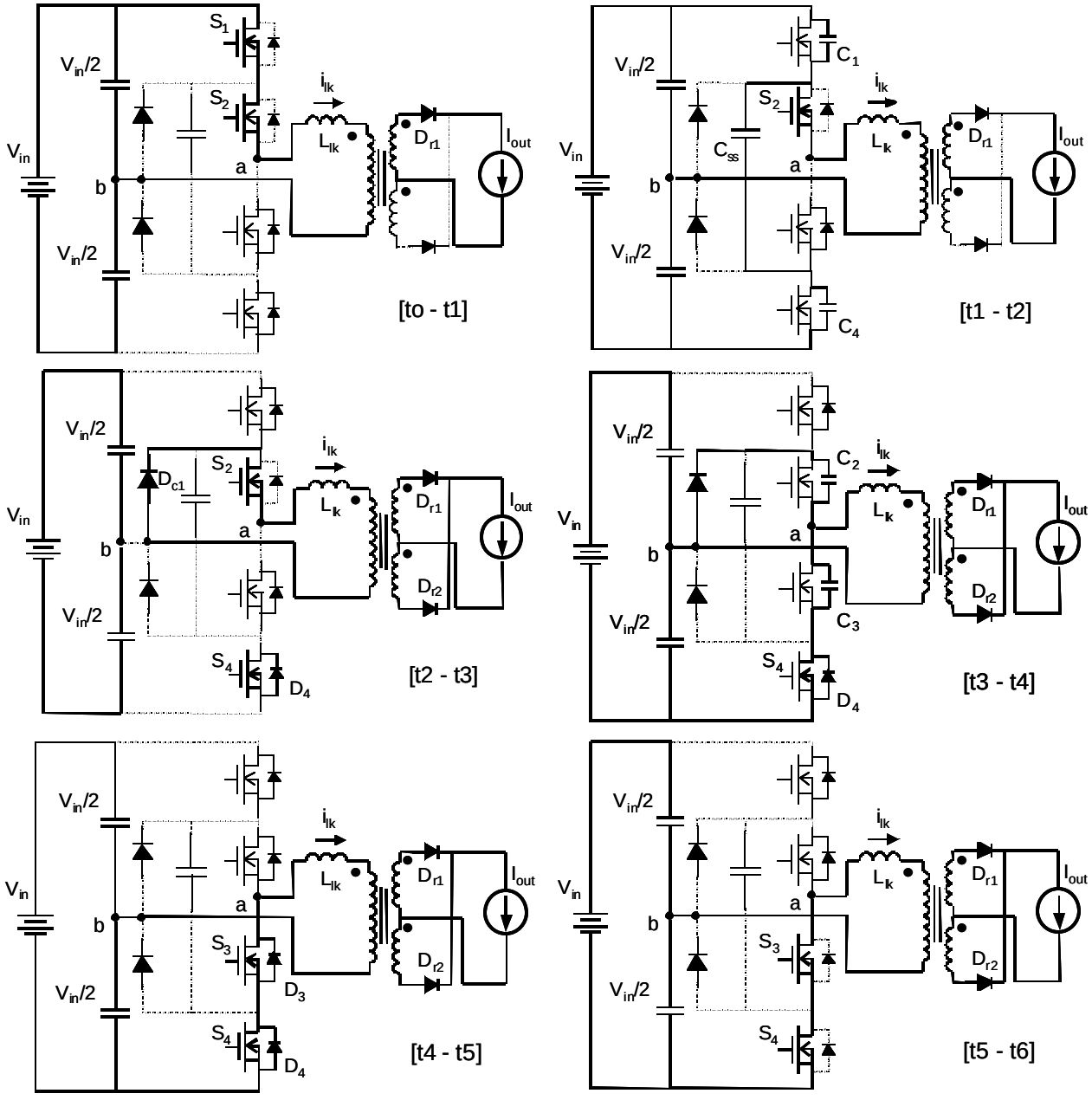


Fig. 2-3. Equivalent circuit for each stage.

A. ZVS Range

In order to achieve ZVS operation for the inner switches S_2 and S_3, the proposed converter uses the stored energy in the leakage inductance of the transformer to charge and discharge parasitic capacitances C_2 and C_3 at the instant when switch S_2 is turned off. The parasitic capacitance of the transformer also must be considered in this process. This stored energy depends on primary current i_{lk} at time t_3. For true ZVS operation, the stored energy in L_{lk} must satisfy the inequality

$$\frac{1}{2}L_{lk}i_{lk}^{2} > \frac{4}{3}C_{mos}\left(\frac{V_{in}}{2}\right)^{2} + \frac{1}{2}C_{tr}\left(\frac{V_{in}}{2}\right)^{2}, \qquad (2\text{-}1)$$

where the term $4/3C_{mos}$ is twice the typical non-linear parasitic capacitance [41] of the switch, and C_{tr} is the transformer winding capacitance.

When the ZVS condition for switches S_2 and S_3 must be achieved for a wide output-load range, L_{lk} has to be increased in order to meet the requirements in (2-1). This in turn results in a loss of duty cycle and circulating energy in the primary side as mentioned in other work [38]. Therefore, there is a tradeoff between the ZVS range and the efficiency of the converter. In practice, it is recommended that the ZVS condition for S_2 and S_3 be lost at certain load conditions. Thus, the critical primary current needed to achieve ZVS operation can be obtained from (2-1) as

$$i_{crit} = \frac{V_{in}}{2}\sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}C_{mos} + \frac{1}{2}C_{tr}\right)}. \qquad (2\text{-}2)$$

Therefore, the ZVS condition is obtained when the load current I_{out} reflected to the primary side is higher than the critical current; that is:

$$\frac{I_{out}}{n} > i_{crit}, \tag{2-3}$$

where n is the turns ratio of the transformer.

B. Dead-Time Requirements

In order to assure that the parasitic capacitances of switches S_2 and S_3 are fully discharged, it is necessary to include a dead time between the turn-off of S_2 and the turn-on of S_3, and vice versa. It is possible to determine the maximum dead-time requirement after defining the necessary leakage inductance to achieve ZVS operation under certain load conditions. This dead time can be defined as one-fourth of the resonant period that exists between C_{mos}, C_{tr} and L_{lk}; that is:

$$\Delta_{\max} = \frac{T}{4} = \frac{p}{2}\sqrt{L_{lk}\left(C_{mos} + C_{tr}\right)}. \tag{2-4}$$

C. Output-Voltage Regulation

Another important parameter to consider in the design of the proposed ZVS three-level DC/DC converter is the output-voltage regulation. The converter must be designed to achieve the maximum output voltage at the minimum input-voltage condition and full load. Therefore, the design of the converter must take into consideration the duty-cycle loss that occurs due to leakage inductance, which is selected in order to achieve the ZVS condition within a certain load range. Considering this duty-cycle loss, the output voltage of the converter can be defined as follows:

$$V_o = \frac{D}{2n}V_{in} - \frac{4}{n^2}I_{out}L_{lk}\,f_s. \tag{2-5}$$

The second term in (2-5) can be defined as the duty-cycle loss. This term is common to all converters that rely on the energy stored in the resonant inductor to achieve ZVS operation for the lagging switches [38].

2.3.2. Experimental Results

An experimental prototype was built in order to verify the operation of the proposed ZVS three-level DC/DC converter. The specifications of the prototype are as follows: V_{out} = 42 - 58 V, I_{out} = 115 A, V_{in} = 660 - 800 V, and f_s = 100 kHz.

The power stage shown in Fig. 2-2 consists of the following components.

$S_1 – S_4$: APT60M90JN

$D_{r1} – D_{r2}$: HFA140MD60C

$D_{c1} – D_{c2}$: BYV34-500

C_{in1}, C_{in2}, C_{ss}: 4x1 µF/600 V – polypropylene

T_r: E65 - 3F3

L_{lk}: 5 µH

L_{out}: 2xEC55-3C85, 16 µH

C_{out}: 220 µF/250 V – electrolytic

In order to reduce the circulating energy of the converter and to avoid an excessive duty-cycle loss, the converter is designed to lose ZVS operation at 55% of the full load at 800V input voltage. Therefore, the necessary resonant inductance is achieved by adding an additional inductance of 2.7 µH to the leakage inductance of the transformer.

The turns ratio of the transformer is designed to achieve high output voltage at low input-voltage conditions. In this way, the transformer is selected to be a center-tapped transformer with a turns ratio equal to 4, and with 12/3/3 turns in the primary and secondary sides.

Experimental waveforms for the proposed converter at full-load condition, with nominal output voltage (52V) and a high input-voltage condition are shown in Figs. 2-4 and 2-5.

Fig. 2-4 shows the voltage and current in the primary side of the transformer (upper and lower trace), and the secondary rectified voltage (middle trace). It can be seen that just half the input voltage is applied to the transformer. In addition, a ringing can be seen to occur in the secondary rectifiers. As was explained, this ringing is due to the resonance between the leakage inductance of the transformer and the parasitic capacitance of the output rectifiers.

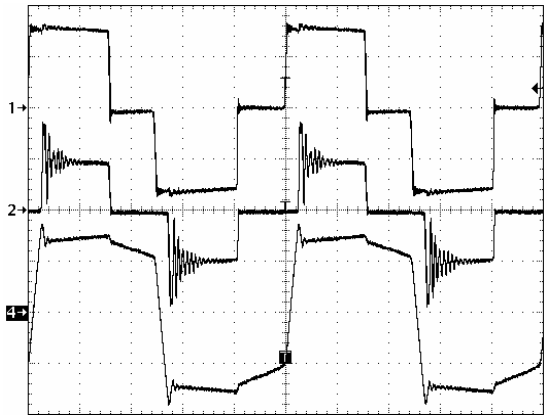


Fig. 2-4. Voltage (upper trace) and current (lower trace) waveforms of the transformer primary side, and rectifier voltage (middle trace) waveforms (250 V/div, 200 V/div, 20 A/div, 2 µs/div).

Fig. 2-5 shows the ZVS operation of the proposed converter. Figs. 2-5(a) and (b) show the drain-to-source voltage, V_{DS}, and its gate-signal voltages across switches S_1 and S_2, respectively. It can be seen that in both cases, the maximum voltage for switches S_1 and S_2 is 400 V, just half of the input voltage. Also, it can be observed that the voltage falls to zero prior to the turn-on of the gate signal, which means that a ZVS transition is achieved.

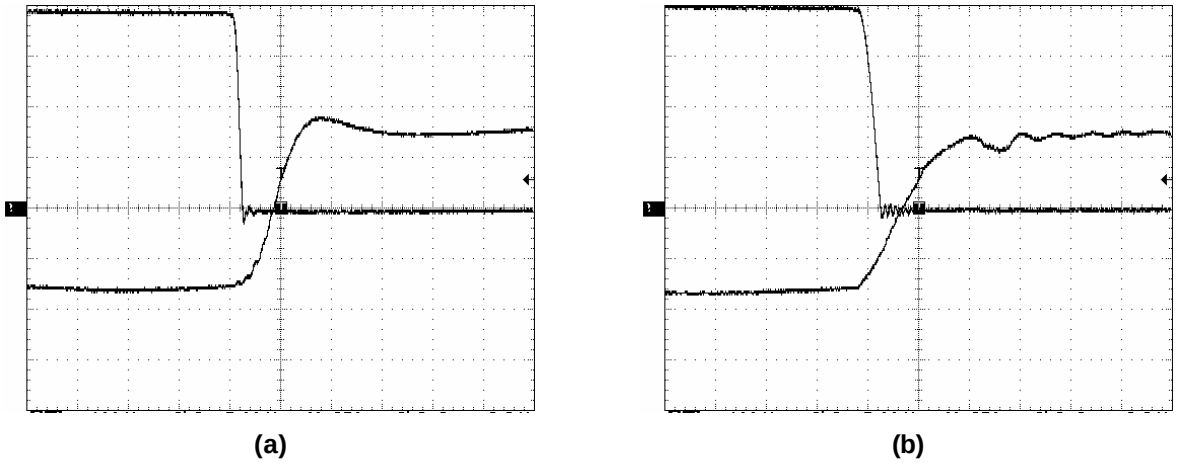


Fig. 2-5. Drain-to-source (upper trace) and gate voltage (lower trace) waveforms of (a) S1 and (b) S2 (both at 100 V/div, 5 V/div, 250 ns/div).

The experimental measured efficiency as a function of the output power at nominal input voltage (800 V) and nominal output voltage (52 V) is shown in Fig. 2-6. The efficiency at full-load condition is 91.3%, and the maximum efficiency of the converter, which occurs around 2,300 W, is 94.2%.

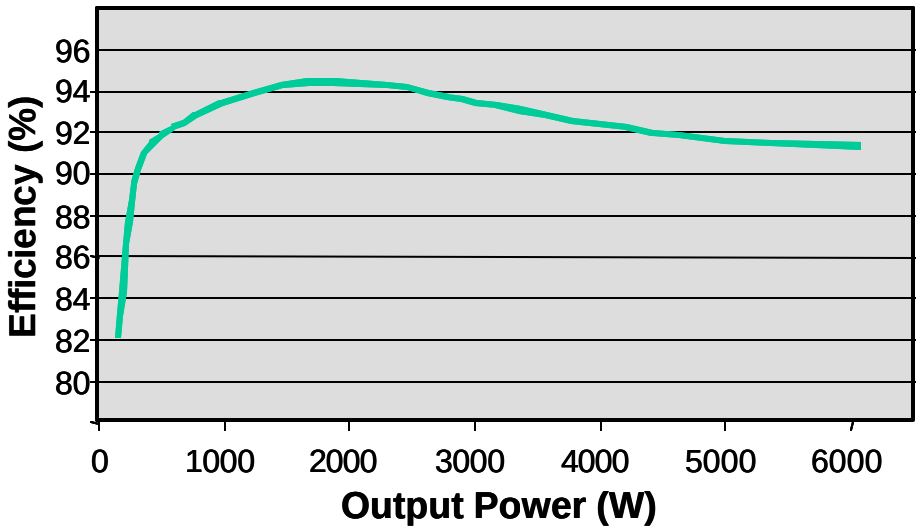


Fig. 2-6. Measured efficiency of the ZVS three-level DC/DC converter.

2.4. Self-Voltage-Balance Capability of the Input Capacitances

This section evaluates the capability of the proposed ZVS three-level DC/DC converter operated with phase-shift control to balance the voltage across the input capacitors under abnormal operation. To see this benefit, a comparison is made between the proposed converter and one using PWM control under similar abnormal operation conditions.

Besides the complexity in generating the control signals and implementing the gate drivers, one of the potential problems in the ZVS three-level DC/DC converter with PWM control is the imbalance of the input capacitor under abnormal operation conditions, such as when there is a mismatch of the gate signals. In this situation, the input capacitors work in the same way as the typical DC blocking capacitor used in traditional full-bridge DC/DC converters, in that they absorb any net voltage across the transformer. This eliminates the problem of transformer saturation under similar conditions. However, the main advantage of reducing the voltage across the main devices to half the level of the input voltage is lost.

Fig. 2-7 illustrates the main waveforms and voltage imbalance for the input capacitors under this condition. In this figure, ? T is defined as the variation of the conduction time for the outer switches S_1 and S_2. This variation results in a duty-cycle-variation parameter that gives the relationship D_2/D_1 between the dutt cycles applied to the transformer during each half of a switching cycle. Fig. 2-7(b) shows the voltage imbalance in the input capacitors using this relationship as a running parameter. The result shown in this figure uses the same specifications given in the previous section: input voltage of 800 V, 6kW output power, and switching frequency of 100 kHz. As can be seen, a ratio of 1.15 that corresponds to a ?T of 250 ns results

in a 30V deviation in each input capacitor. This deviation results also in voltage stress across the primary devices.

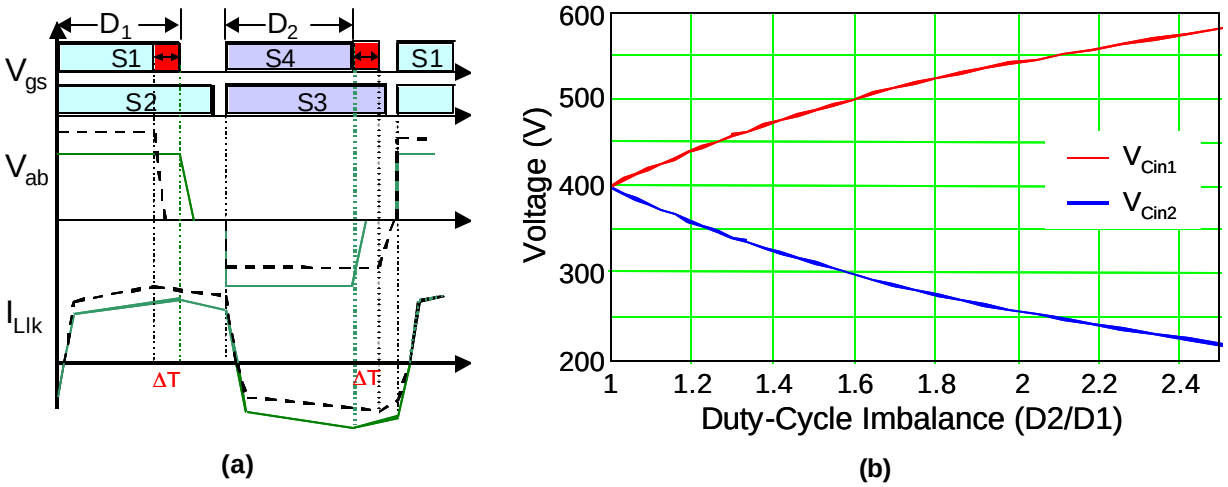


Fig. 2-7. Operation of the ZVS three-level DC/DC converter under abnormal operation: (a) typical waveforms and (b) voltage evolution across the input capacitance.

In the proposed converter, the use of the C_{ss} capacitor not only simplifies the control and gate drivers by using phase-shift control, but also helps to minimize the voltage imbalance under similar abnormal operating conditions. The C_{ss} capacitor is connected in parallel to the input capacitors during the freewheeling stage of the converter, as shown in Fig. 2-8. Therefore, the input capacitors have the opportunity to balance their charge through C_{ss} in every half of a switching cycle.

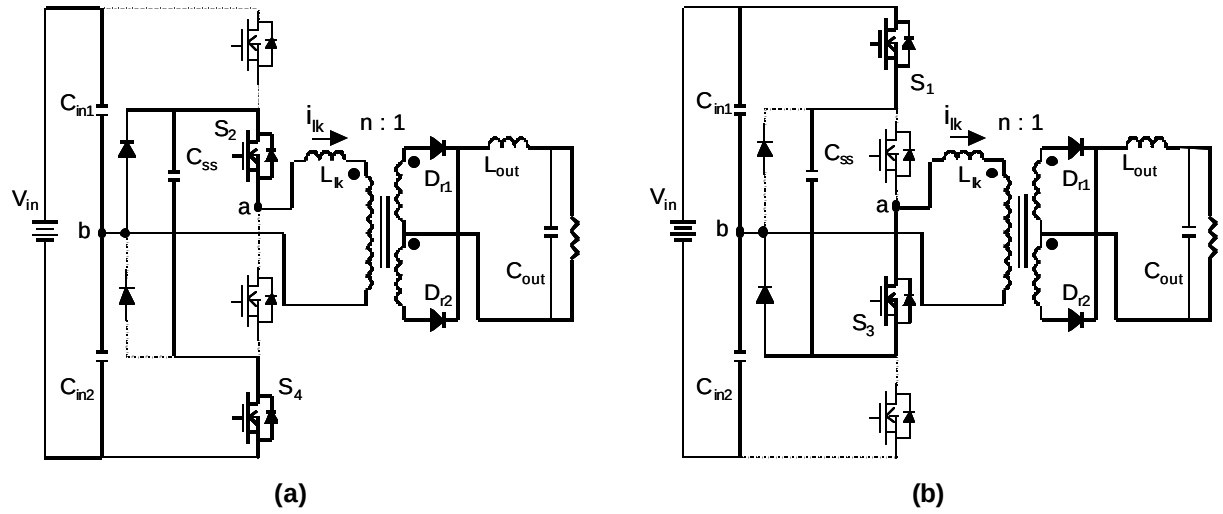
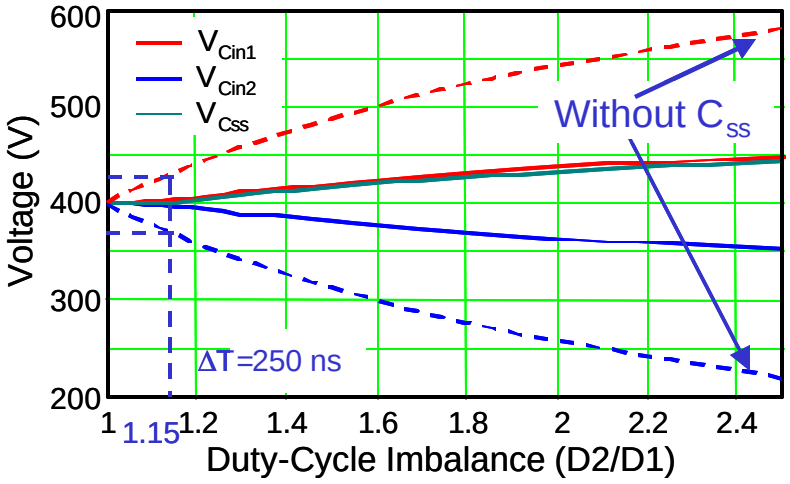


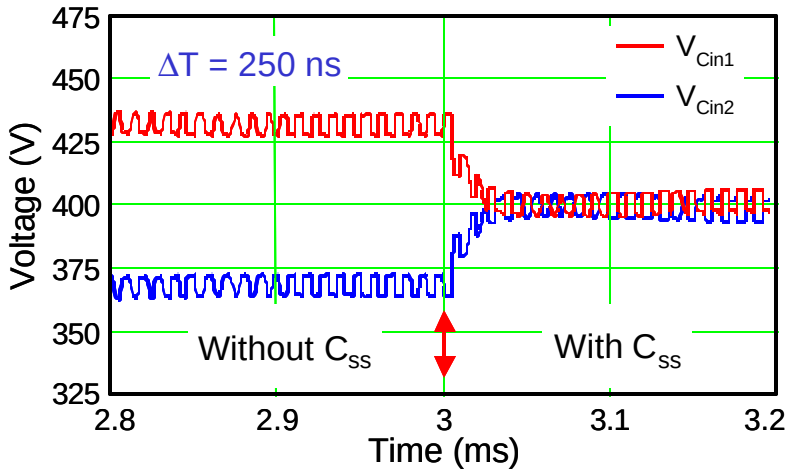
Fig. 2-8. Mechanism to balance the voltage across the input capacitors. Freewheeling stages for (a) the positive half of a switching cycle and (b) the negative half of a switching cycle.

In order to illustrate the self-voltage-balance capability of the proposed converter, Fig. 2-9 shows a comparison between the three-level DC/DC converter using PWM control and the proposed three-level DC/DC converter using phase-shitt control. Fig. 2-9(a) shows again the input-voltage imbalance of the input capacitors for both cases using the relationship D_2/D_1 as a running parameter. For the same ?T of 250 ns, it can be seen that the voltage deviation in the input capacitors is almost negligible for the proposed converter using phase-shift control. As mentioned before, C_{ss} provides the mechanism to balance the charge of both input capacitors during the freewheeling time.

It is important to mention that the self-balance capability can be extended to the three-level DC/DC converter under PWM operation by again using the auxiliary capacitor C_{ss}. Fig. 2-9(b) shows time simulations of the converter using PWM control with a ? T of 250 ns. At time 3 ms, the capacitor C_{ss} is included in the operation of the converter, providing a mechanism to minimize the deviation of the voltage across the input capacitors.



(a)



(b)

Fig. 2-9. Self-balance capability of the proposed converter: (a) comparison of the voltage deviation of the input capacitor voltage under abnormal operation and (b) effect of the auxiliary capacitor C_{ss} in balancing the voltage across the input capacitors.

It is important to mention that the self-balance capability of the proposed converter becomes an important parameter in higher-switching-frequency operation in which small ?T variations result in a big ratio between D_1 and D_2.

2.5. Conclusion

A novel ZVS three-level DC/DC converter was introduced in this chapter. The operation stages and characteristics of the proposed converter were presented. Experimental results from a 6 kW prototype were given in order to demonstrate the operation of the converter.

It was shown that this converter reduces the voltage stresses across the main switches to half the level of the input voltage. Therefore, devices with lower voltage ratings, which present better characteristics, can be used. Besides, the addition of a flying capacitor in the primary side allows ZVS operation for all switches with phase-shift control.

It was also shown that this new control scheme not only simplifies the modulation scheme for the three-level DC/DC converter, but also helps to balance the voltage across the DC input capacitor under abnormal operating conditions, such as when there is a gate-signal mismatch.

In addition, it will be shown in the next chapter that the operation with phase-shift control allows ZVS and ZVZCS techniques that were previously developed for full-bridge converters to be implemented without modifications in the proposed topology. In the case of the ZVS techniques, the ZVS range increases in the converter while minimizing the circulating energy, the duty cycle loss and the secondary parasitic ringing. It is important to mention that these problems are common in all DC/DC converters in which the ZVS operation relies on the energy stored in either an external resonant inductance or the leakage inductance of the transformer.

These characteristics make the proposed converter an interesting option for high-voltage, high-power applications that require high efficiency.

3. Improvements for the PWM Three-Level DC/DC Converter

3.1. Introduction

One of the drawbacks the proposed converter presents is the use of the energy stored in the transformer leakage inductance to achieve ZVS for inner switches S_2 and S_3. In this case, an additional resonant inductance must be included in order to assure ZVS for a wide load range. This in turn increases the circulating energy, which increases the conduction losses in the converter. In addition, both a reduction in the effective duty cycle and a severe secondary parasitic ringing occur.

As mentioned in the previous chapter, the operation with phase-shift control allows the implementation of soft-switching techniques previously proposed for the full-bridge converter to be used in the three-level DC/DC converter. This characteristic in the proposed converter allows ZVS techniques [41]-[46] and ZVZCS techniques, previously presented for full-bridge DC/DC converters [47]-[60], to become another option for overcoming the main drawbacks presented by the conventional ZVS three-level DC/DC converter.

This chapter discusses the operation of the proposed converter with different soft-switching techniques to improve its main characteristics and performance. This chapter will first address possible improvements by using other ZVS techniques, which increases the ZVS range without penalizing the circulating energy in the converter. Later, these improvements will be based on ZVZCS techniques.

Taking into account the tradeoff between simplicity and performance presented in the auxiliary circuits to realize ZVZCS in the DC/DC converter, the main contribution of this chapter is the evaluation of the benefits of ZVZCS operation in the proposed three-level DC/DC converter. This is done by analysis, implementation and comparison of several ZVZCS approaches. In all cases, this results in novel ZVZCS three-level DC/DC converters for high-voltage applications, which combine the advantages of reduced voltage stress across the main switches, presented by the use of three-level structures, with the advantages of reduced circulating energy, as offered by ZVZCS soft-switching operation.

3.2. Improvements of the Proposed Converter by Using Other ZVS Techniques

The implementations of the proposed ZVS three-level DC/DC converter with other ZVS techniques are presented in this section of the dissertation.

Figs. 3-1, 3-2 and 3-3 show some possible extensions of the proposed ZVS three-level DC/DC converter using different ZVS techniques to overcome its associated problems. In Fig. 3-1, the variation of the proposed converter uses a saturable inductor as an element to store the energy needed to achieve ZVS for the inner switches [42]. In this way, the leakage inductance can be reduced, and both the duty-cycle loss and the secondary parasitic ringing are minimized.

Another possible solution to overcome the problems of the proposed converter is shown in Fig. 3-2. In this approach, the variation of the proposed converter uses the magnetizing energy of the transformer, which is more independent of the load, to achieve ZVS for the inner switches. Thus, the load dependence of the ZVS range is minimized; since the leakage inductance is also reduced, the duty-cycle loss is negligible, and the secondary parasitic ringing is small. In order to

have control over the magnetizing energy, magnetic switches and an extra freewheeling diode are placed in the secondary side [44]-[46].

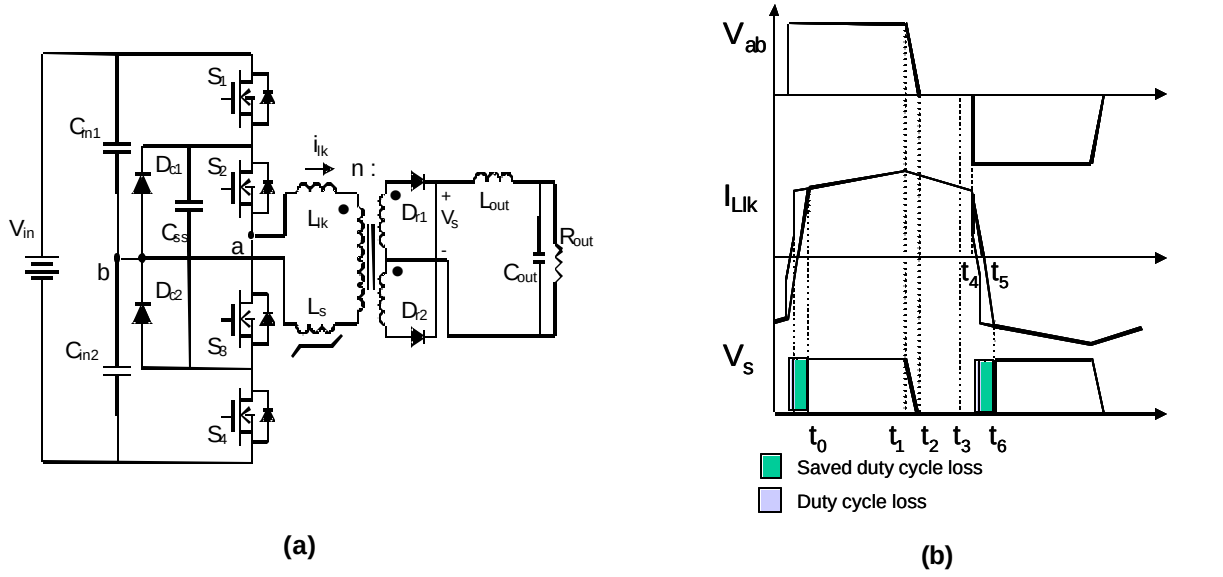


Fig. 3-1. (a) The ZVS three–level DC/DC converter using a saturable resonant inductor, and (b) its main waveforms.

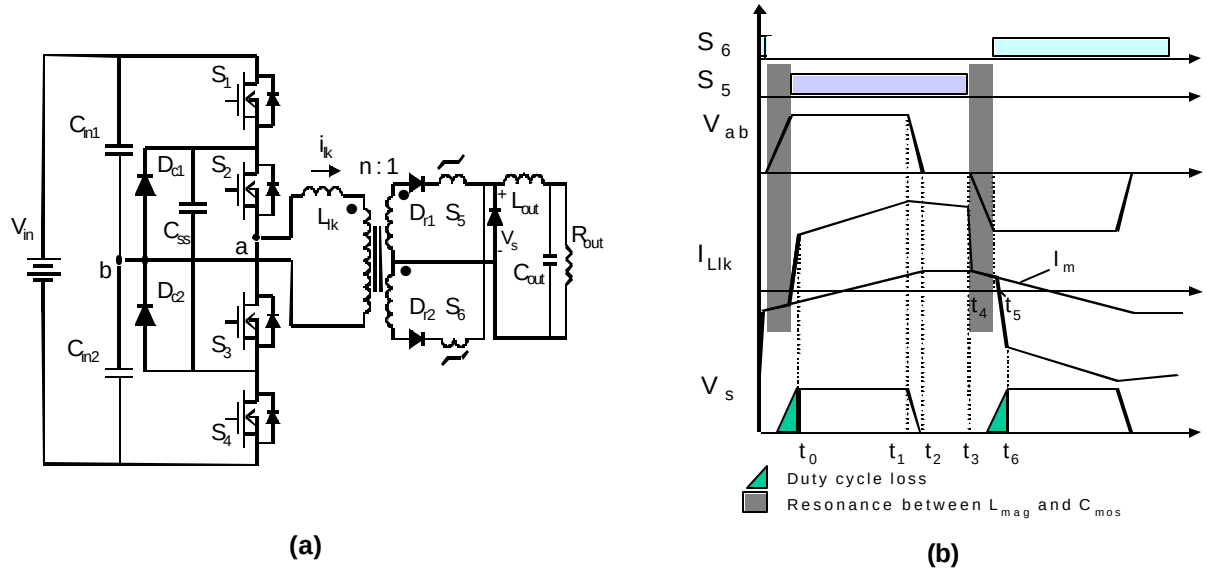


Fig. 3-2. (a) The ZVS three–level DC/DC converter using the magnetizing inductance, and (b) its main waveforms.

Fig. 3-3 shows another possible solution for eliminating the drawbacks of the proposed converter. In this case, the variation of the proposed converter uses saturable inductors as complementary switches in the secondary side to allow the stored energy in the output inductor to be used to achieve ZVS for the inner switches [40]. Since the amount of this stored energy is always greater than that of the leakage inductance, the ZVS range is widely extended. In addition, since the leakage inductance is no longer necessary to achieve ZVS for the inner switches, it can be reduced as much as possible. In this way, the duty-cycle loss and the secondary parasitic ringing are reduced.

The proposed topology lends itself to the implementation of other ZVS techniques; however, due to space constraints, these variations are not presented in this document.

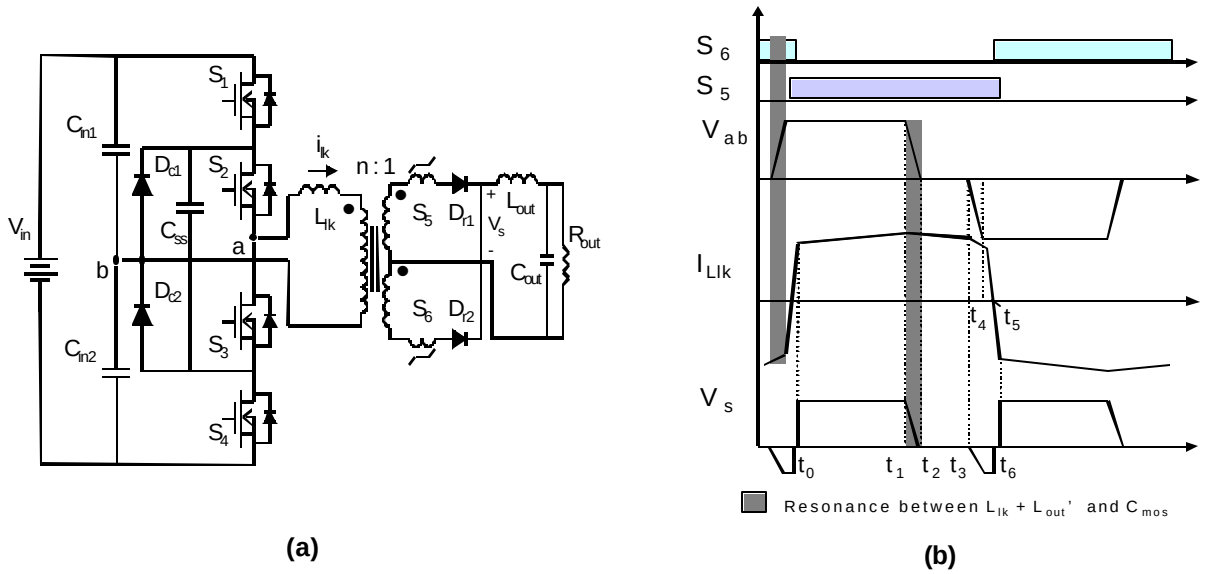


Fig. 3-3. (a) The ZVS three–level DC/DC converter using the output inductor energy, and (b) its main waveforms.

The previous ZVS techniques increase the ZVS range in the converter while minimizing the circulating energy. The next section presents a different approach to improve the soft-switching

characteristic of the converter. This approach resets the energy in the leakage inductance of the transformer, resulting in a ZCS instead of ZVS operation for the inner switches.

3.3. ZVZCS Concept in the Three-Level DC/DC Converter

In previous work [53], it is shown that the ZVZCS concept can be easily implemented in a full-bridge converter if a voltage source with polarity opposite to the primary current direction is available to reset the primary leakage current during the freewheeling time. In this way, switches S_2 and S_3 operate with ZCS instead of ZVS. This concept is illustrated in Fig. 3-4. The same concept is applicable to the three-level DC/DC converter using a phase-shift control proposed in this dissertation.

Not only can this auxiliary voltage source be implemented in different ways, but it can also be placed in the primary or secondary side of the transformer, resulting in a tradeoff between simplicity and performance in the operation of the converter. Fig. 3-5 shows two different approaches for the implementation of the auxiliary voltage source in the secondary side of the converter. In Fig. 3-5(b), an auxiliary active circuit in the secondary side provides the necessary voltage source to reset the primary current during the freewheeling stage when S_{aux} is turned on. In this way, both the ZVZCS condition for the primary switches and the active clamping of the voltage across the secondary diodes are achieved.

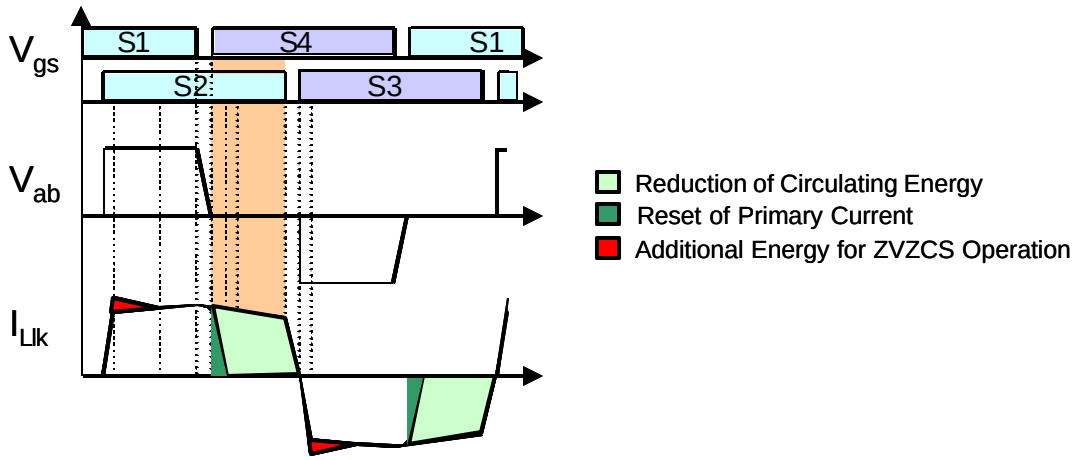


Fig. 3-4. Main waveforms for the proposed three-level DC/DC converter with phase-shift control under ZVZCS operation.

In Fig. 3-5(c), the auxiliary voltage source is implemented by also using a passive auxiliary circuit in the secondary side [50]. Its operating principle is similar to that of the converter with an active auxiliary circuit. That is, when the outer switch S_1 or S_4 is turned off, the snubber capacitor C_{aux} works as a temporary voltage source to reset the primary freewheeling current. This temporary voltage source is not controllable, which means that in every half period the snubber capacitor energy is discharged completely. Moreover, during the transition from the freewheeling stage to the active stage, this voltage source is reestablished in a resonant fashion. Therefore, the voltage stress in the rectifiers can increase to up to two times and there is an increase in the circulating energy. These drawbacks can be minimized with a better design of the turns ratio of the transformer, since the voltage stress depends on the duty cycle of the converter [50]. In addition, taking into account that the ZVS action for the outer switches is achieved using the reflected output current, the leakage inductance can be reduced as much as possible. In this way, the primary current is brought to zero in a short time, reducing the duty-cycle loss. Also, the secondary-side parasitic ringing across the output rectifier diodes is reduced.

Fig. 3-6 shows possible extensions of ZVZCS operation for the proposed three-level DC/DC converter following the concept of the voltage source introduced in previous work [53]. Fig. 3-6(a) shows the proposed converter using an auxiliary voltage source in the primary side. As in other work [49], this voltage source is implemented with a capacitor and a saturable inductor. If the capacitance is very low, the voltage level across it can be high enough to reset the primary current. Meanwhile, the saturable inductor is used to keep the current at zero during the freewheeling stage. In this case, the use of a saturable inductor can limit both the power level and the switching frequency of the converter due to thermal problems.

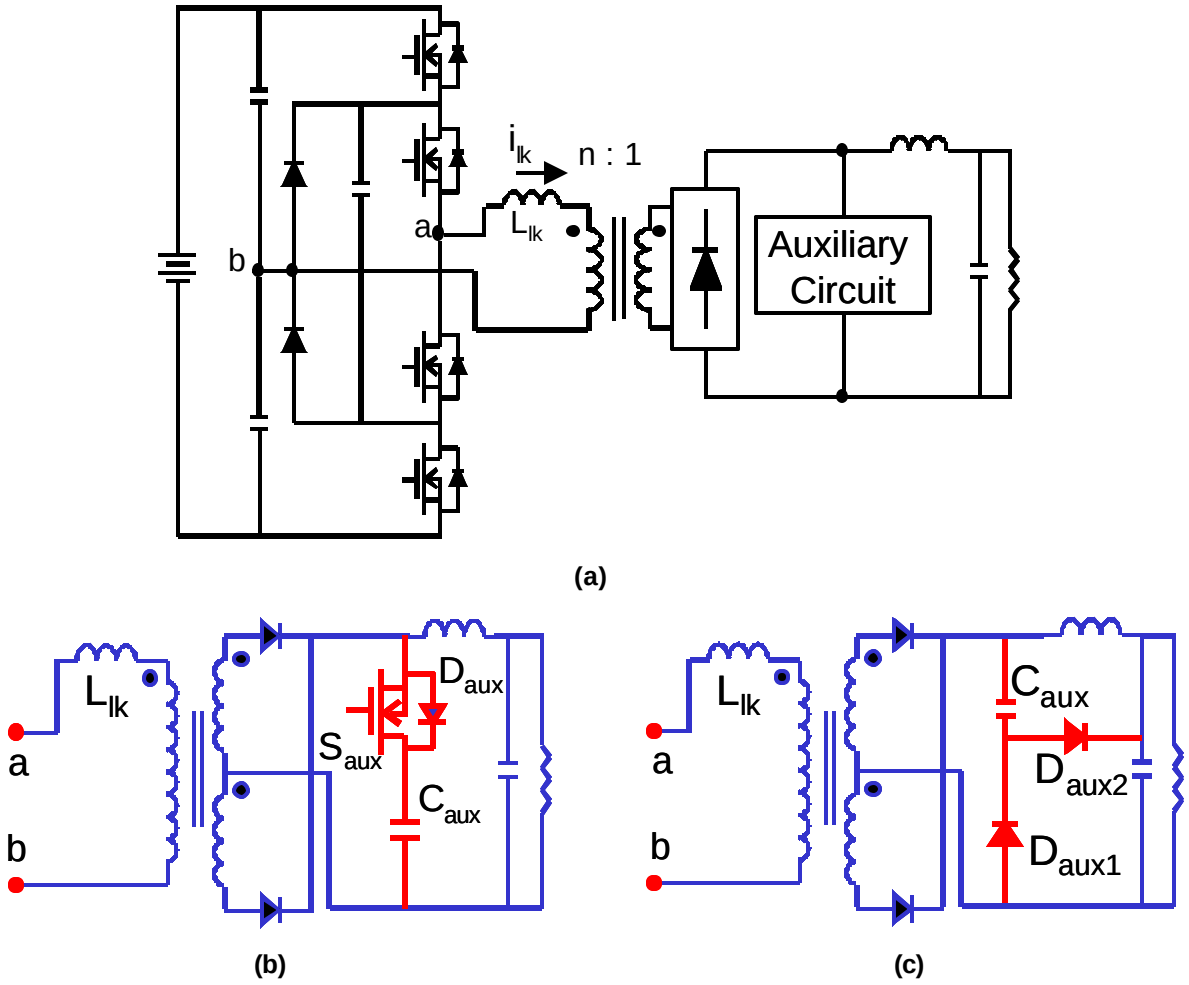


Fig. 3-5. (a) Auxiliary circuits in the secondary side for ZVZCS operation, (b) active auxiliary circuit and (c) passive auxiliary circuit.

Fig. 3-6(b) shows another way to achieve the ZVZCS condition for the proposed converter by placing an auxiliary circuit in the primary side. The auxiliary circuit is implemented with the three-winding transformer T_A and the two diodes D_{A1} and D_{A2}. In this way, the inner switches operate under ZCS condition with the assistance of the auxiliary circuit, which provides reset voltage and absorbs the reactive stored energy in leakage inductance L_{lk}. One of the characteristics that the proposed converter presents is the capability to maintain soft-switching operation even in short-circuit conditions or at start-up.

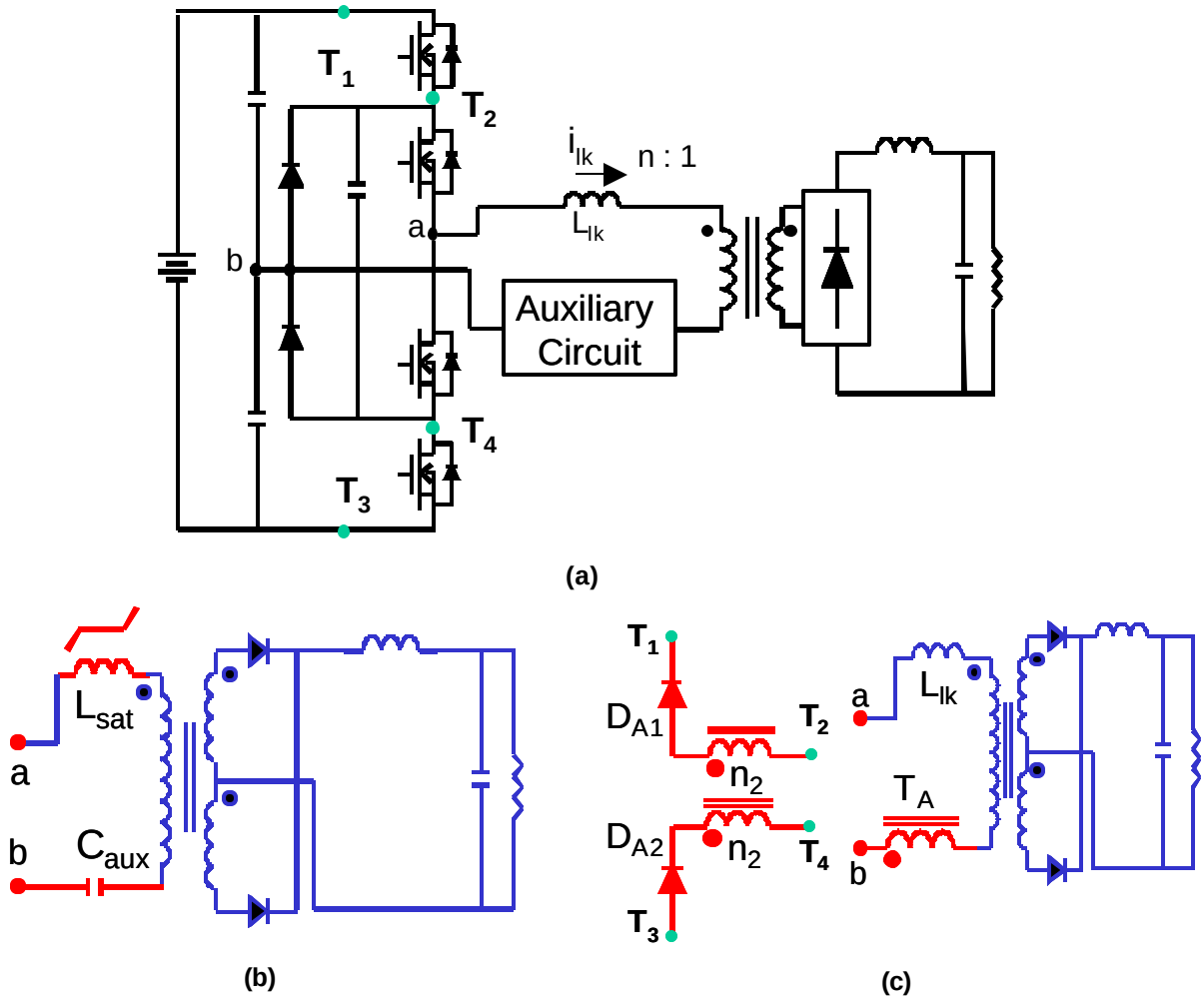


Fig. 3-6. (a) Auxiliary circuits in the primary side for ZVZCS operation, (b) saturable inductor approach and (c) auxiliary transformer approach.

The next sections present the analysis, implementation and comparison of these ZVZCS techniques in the proposed three-level DC/DC converter operating with phase-shift control.

3.4. ZVZCS Three-Level DC/DC Converter Using an Active Auxiliary Circuit in the Secondary Side

In this section, the operating principle of the ZVZCS three-level DC/DC converter using an active auxiliary circuit in the secondary side is presented. The proposed ZVZCS three-level DC/DC converter and its timing diagram are shown in Fig. 3-7. It can be seen that the basic structure is very similar to that of the ZVS three-level converter proposed in other work [22]. The main difference is the inclusion of the flying capacitor, C_{ss}, to allow the converter to operate with phase-shift control and with ZVS for outer switches S_1 and S_4. Also, an auxiliary active circuit is added in the secondary side to both reset the primary current in the transformer and to achieve ZCS operation for inner switches S_2 and S_3.

3.4.1. ZVZCS Operating Mode Using an Active Auxiliary Circuit in the Secondary Side

The proposed converter has eight stages of operation during each half of a switching cycle. Similar to the ZVS three-level DC/DC converter discussed in this dissertation, the circuit uses the well-known phase-shift control in which all switches operate with duty cycles of nearly 50%. The phase shift between S_1 and S_2 or S_3 and S_4 determines the operating duty cycle of the converter. The equivalent circuit for each stage of operation is shown in Fig. 3-8. These stages are described as follows.

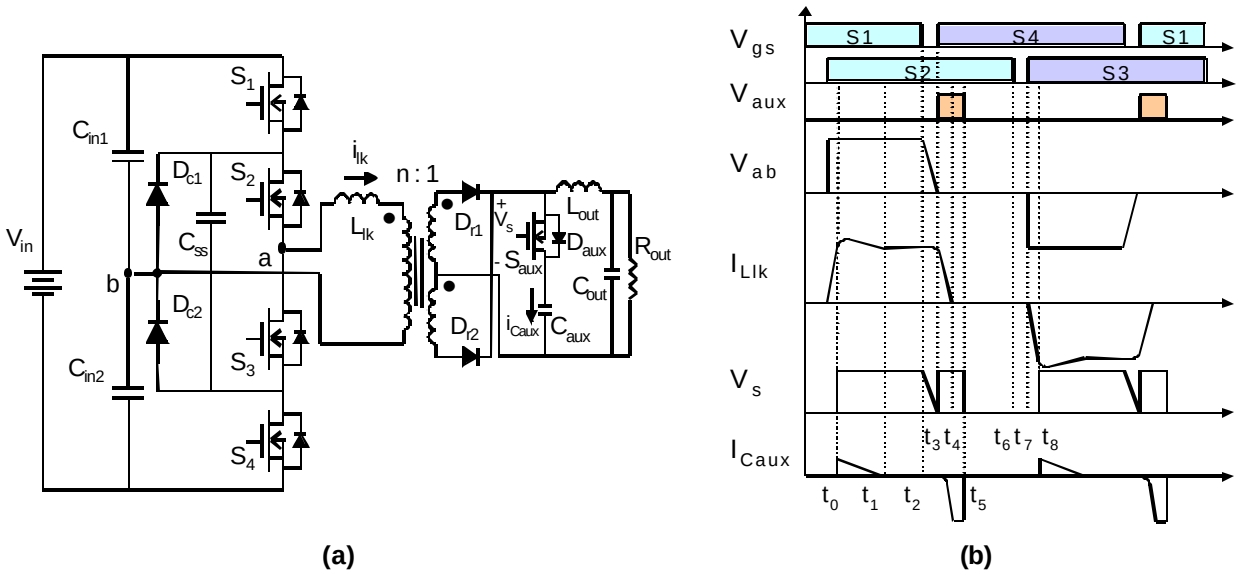


Fig. 3-7. (a) The ZVZCS three–level DC/DC and (b) its main waveforms.

[t_0-t_1]: During this stage, S_1 and S_2 are conducting, and the input power is delivered to the output. At the beginning of this stage, leakage inductance L_{lk} resonates with the junction capacitance of diode rectifier D_{r2}. This resonance takes places until voltage V_s reaches the voltage of clamping capacitor C_{aux}. After that, the extra current in the leakage inductance starts to circulate through the clamping capacitor. The discharge of the extra current is considered linear, since the voltage across the clamping capacitor is assumed to be constant. This stage ends at t_1, when the current through clamping capacitor I_{Caux} reaches zero. The duration of this stage depends on the leakage inductance, junction capacitance and reverse-recovery time of the rectifier diodes.

[t_1-t_2]: In this stage, the input continues delivering power to the output. At t_1, the current in the clamping capacitor tends to reverse its polarity, but the anti-parallel diode of auxiliary switch S_{aux} turns off, and the reverse voltage across the secondary rectifier D_{r2} becomes

$$V_{rec} = \frac{V_{in}}{n}. \tag{3-1}$$

[t_2-t_3]: At t_2, S_1 is turned off, and the load current charges and discharges the parasitic capacitance of S_1 and S_4, respectively, through flying capacitor C_{ss}. This stage ends when the voltage across the parasitic capacitance of S_1 reaches $V_{in}/2$ and clamping diode D_{c1} begins to conduct. At the same time, the voltage across the parasitic capacitance of S_4 reaches zero, and anti-parallel diode D_4 begins to conduct.

[t_3-t_4]: After D_4 starts conducting, S_4 can be turned on with ZVS. The primary current freewheels through S_2 and clamping diode D_{c1}. Meanwhile, the auxiliary switch is turned on, and the voltage across clamping capacitor C_{aux} is reflected to the primary side of the transformer and is applied across the leakage inductance. In this way, the primary current is reduced linearly to zero with a slope equal to nV_{Caux}/L_{lk}. In addition, the clamping capacitor supplies energy to the output. This stage ends when the primary current is reset to zero.

[t_4-t_5]: The rectifier diodes are turned off, since the primary current is zero and S_{aux} is still on. During this stage, the output current is still supplied by clamping capacitor C_{aux}. As a result, the effective duty cycle of the secondary side may be larger than that of the primary side.

[t_5-t_6]: At t_5, S_{aux} is turned off, the voltage applied across the output rectifiers immediately drops to zero, and the conventional freewheeling stage in the PWM converter begins. During this period, there is no current freewheeling in the primary side. Therefore, the circulating energy in the primary side is reduced due to the ZVZCS operation.

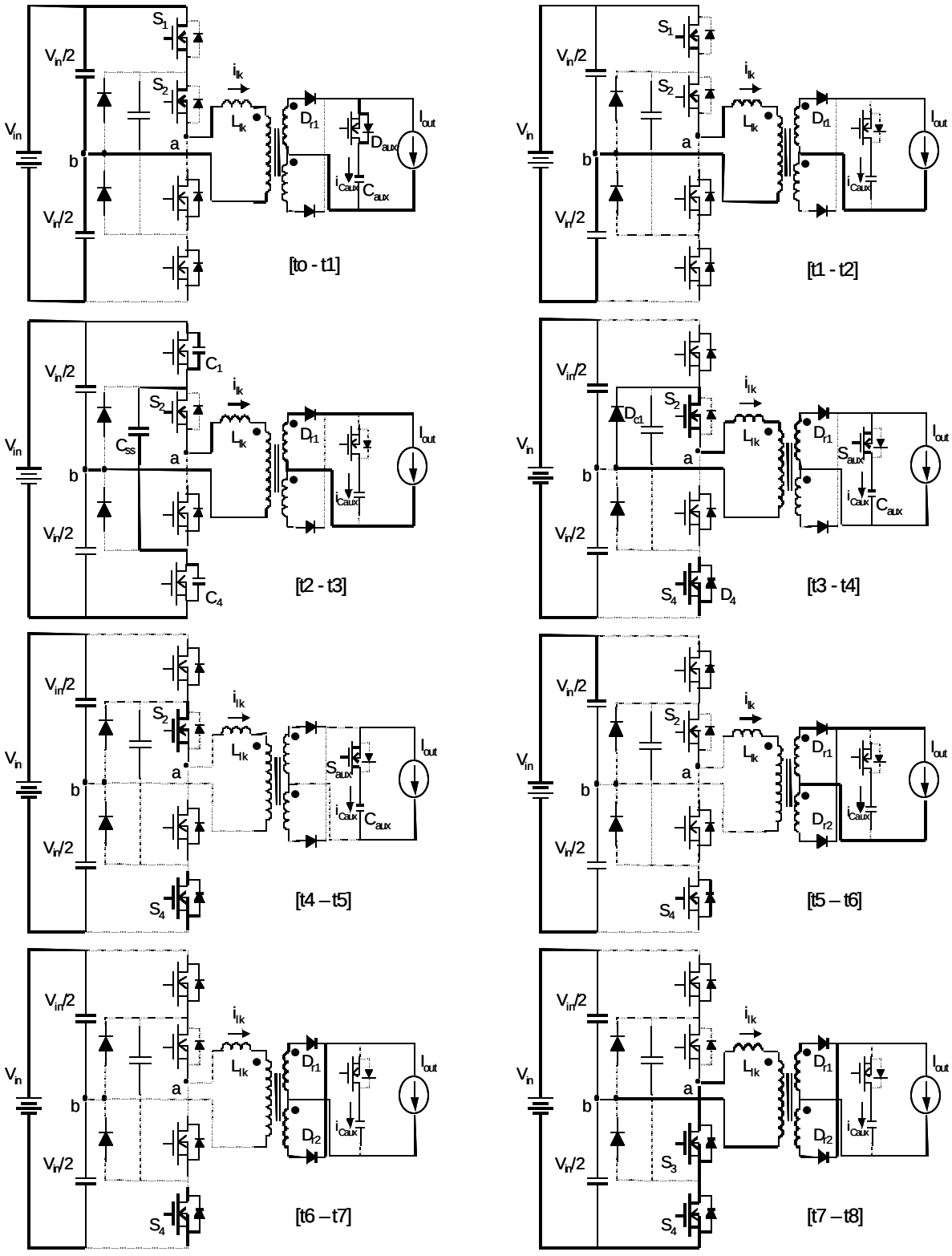


Fig. 3-8. Equivalent circuit for each stage of the ZVZCS three–level DC/DC converter using an active auxiliary circuit in the secondary side.

[t_6-t_7]: Since the leakage current has been completely reset at t_4, switch S_2 is turned off under ZCS at t_6. As a consequence, IGBTs can be used for S_2 and S_3.

[t_7-t_8]: At t_8, S_3 is turned on, and half of the input voltage is applied to the primary side of the transformer. The primary current flows through S_3, and S_4 and begins to increase with a slope equal to $V_{in}/(2L_{lk})$. At the end of this stage, the primary current reaches the reflected output current, starting a new half of a switching cycle.

3.4.2. DC Characteristics of the Proposed ZVZCS Three-Level DC/DC Converter

In this section, the DC characteristics of the proposed three-level DC/DC converter are analyzed. It will be shown that these characteristics depend on leakage inductance L_{lk}, voltage V_{Caux} in the auxiliary capacitor, and the duration of the turn-on of auxiliary switch S_{aux}.

The effective duty cycle in the converter can be expressed as

$$D_{eff} = D - D_{ch} + D_{zvs} + D_{aux} \tag{3-2}$$

where

$$D = \frac{2t_{on}}{T_s} \tag{3-3}$$

$$D_{ch} = \frac{2(t_8 - t_7)}{T_s} \tag{3-4}$$

$$D_{zvs} = \frac{2(t_3 - t_2)}{T_s} \tag{3-5}$$

$$D_{aux} = \frac{2(t_5 - t_3)}{T_s}. \tag{3-6}$$

In (3-2), D is the duty cycle applied to the primary side of the transformer, D_{ch} is the duty-cycle loss that occurs due to the charge of the leakage inductance from zero to the load current reflected to the primary, D_{ZVS} is the duty cycle that exists due to the ZVS action of the outer switches, and D_{aux} is the duty cycle that exists due to the conduction time of the auxiliary switch. D_{aux} is also known as the duty-cycle boost effect.

The time interval t_{on} in (3-3) is the simultaneous conduction time of S_1 and S_2 or S_3 and S_4, and T_s is the switching period of the converter.

The time intervals (t_8-t_7) and (t_3-t_2) are obtained from the respective equivalent circuits. These time intervals are given by:

$$(t_8 - t_7) = \frac{2 L_{lk} I_{out}}{n V_{in}} \tag{3-7}$$

$$(t_3 - t_2) = \frac{n V_{in} C}{I_{out}}. \tag{3-8}$$

Here, n is the turns ratio of the transformer, C is the parasitic capacitance of the MOSFET, and I_{out} is the output current of the converter.

The time interval (t_5 – t_3) depends on the time necessary to reset to zero the current in the leakage inductance. This time has to satisfy the following condition:

$$(t_5 - t_3) \geq \frac{I_{out} L_{lk}}{n^2 V_{Caux}} \tag{3-9}$$

where V_{Caux} is the voltage across the auxiliary capacitor. This voltage can be determined by applying the charge balance in the current through the auxiliary capacitor shown in Fig. 3-7. It

can be shown that V_{Caux} is given by

$$V_{Caux} = \frac{V_{in}}{2n}. \tag{3-10}$$

The following relationship expresses the output voltage:

$$V_{out} = D_{eff}\,\frac{V_{in}}{2n}. \tag{3-11}$$

The output voltage can be obtained by combining (3-2) with (3-11), as follows:

$$V_{out} = D\left(\frac{V_{in}}{2n}\right) - \frac{2L_{lk}\,I_{out}\,fs}{n^2} + \frac{f_s V_{in}{}^2 C}{2I_{out}} + \frac{V_{in}\left(t_5 - t_3\right) f_s}{n}. \tag{3-12}$$

As can be seen, the output voltage depends on the leakage inductance, the turns ratio of the transformer, the parasitic capacitance of the main switches, the switching frequency and the output current.

Fig. 3-9 shows the dependence of the output voltage on the output current for different duty cycles. The parameters used to plot the curves are V_{in}=660 V, fs=100 kHz, n=5, L_{lk}=600 nH, C=2.53 nF, and ($t_5 - t_3$) = 250 ns. For a given duty cycle, the output current has minimal effect on the reduction of the output voltage, because the commutations of the inner switches in this ZVZCS converter no longer rely on the energy stored in the leakage inductance. This means that the leakage inductance can be as low as possible in order to reduce the duty-cycle loss.

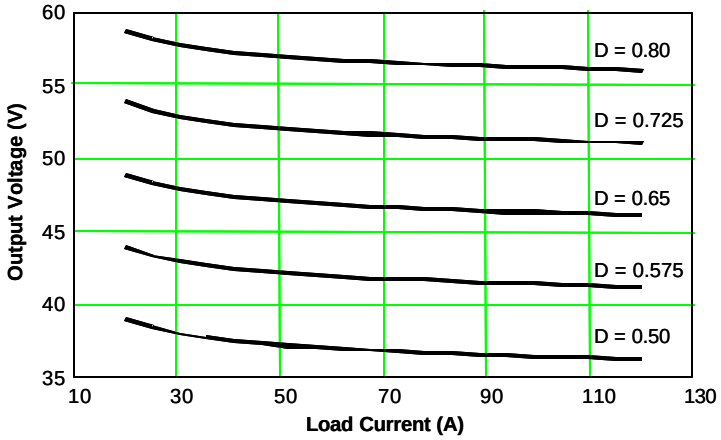


Fig. 3-9. DC characteristics of the proposed converter.

3.4.3. Experimental Results

An experimental prototype was built in order to verify the operation of the proposed ZVZCS three-level DC/DC converter. The specifications of the prototype are as follows: V_{out} = 42-58 V, I_{out} = 100 A, V_{in} = 660 – 800 V, and f_s = 100 kHz.

The power stage shown in Fig. 3-7 consists of the following components.

$S_1 – S_4$: APT60M90JN

$D_{r1} – D_{r2}$: HFA140MD60C

$D_{c1} – D_{c2}$: BYV34-500

C_{in1}, C_{in2}, C_{ss}: 4x1µF/600V – polypropylene

T_r: E65 – 3F3

L_{lk}: 1.2µH

S_{aux}: IXTH50N20

C_{aux}: 6x3.3µF/600V – polypropylene

L_{out}: 2xEC55-3C85, 16µH

C_{out}: 220µF/250V – electrolytic

The auxiliary diode D_{aux} for the auxiliary active circuit is implemented with the MOSFET's body diode of the auxiliary switch S_{aux}.

The turns ratio of the transformer is designed to achieve high output voltage at low input-voltage conditions. In this way, the transformer is selected to be a center-tapped transformer with a turns ratio equal to 5, and with 15/3/3 turns in the primary and secondary sides.

Taking into account that the ZVS action for outer switches S_1 and S_4 is achieved with the reflected output current, the leakage inductance can be reduced as much as possible. Thus, the auxiliary switch needs to be turned on for a short time in order to reset the primary current. An interleaved technique is used to reduce the leakage inductance of the transformer.

Experimental waveforms of the proposed converter at full load, nominal output voltage (52 V) and low input-voltage conditions are shown in Figs. 3-10, 3-11, 3-12 and 3-13.

Fig. 3-10 shows the voltage (upper trace) and current (lower trace) in the primary side of the transformer. It can be seen that the primary current is reset to zero after the end of the stage in which power is transferred to the output. Therefore, S_2 and S_3 are turned off with ZCS.

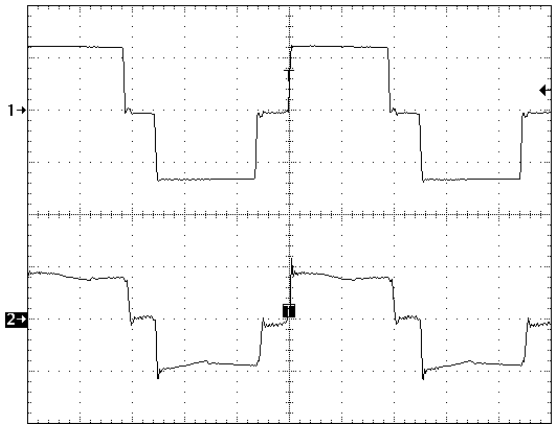


Fig. 3-10. Voltage (upper trace) and current waveforms in the primary side of the transformer (250 V/div, 20 A/div, 2µs/div).

Fig. 3-11 shows the drain-to-source voltage (V_{DS}, upper trace) and the gate-signal voltage (lower trace) of S_1. It can be seen that the maximum voltage for S_1 is 330 V, just half the levels of the total input voltage. Also, it can be appreciated that the voltage falls to zero prior to the turn-on of the gate signal. Therefore, a true ZVS action is achieved.

The voltage V_s across the secondary side (upper trace) and the current in the clamping capacitor (lower trace) are shown in Fig. 3-12. It can be seen that during the turn-on of the auxiliary switch, the clamping capacitor provides all the current to the load. Therefore, a boost duty-cycle effect occurs.

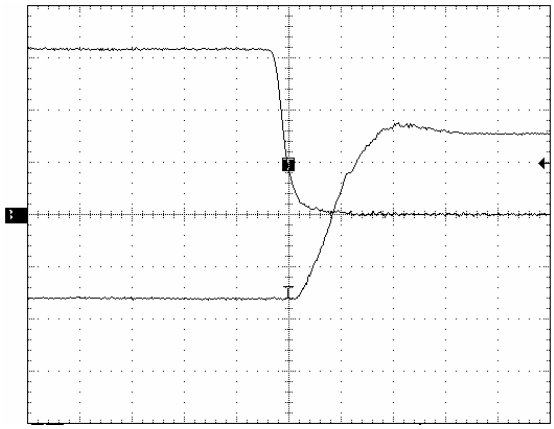


Fig. 3-11. Drain-to-source (upper trace) and gate voltage waveforms of S_1 (100 V/div, 5 V/div, 0.2µs/div).

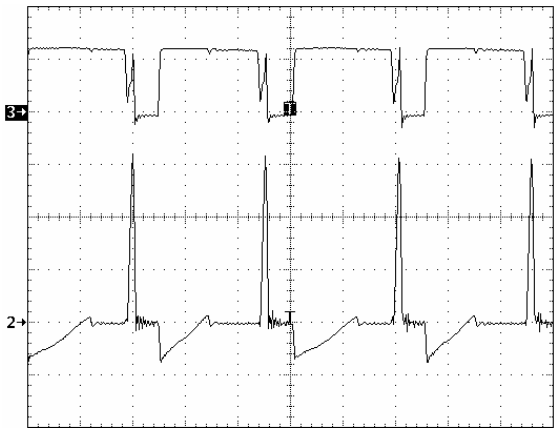


Fig. 3-12. Voltage V_s across the secondary side (upper trace) and current in the clamping capacitor (100 V/div, 30 A/div, 2µs/div).

The experimental measured efficiency as a function of the output power at nominal input voltage and maximum output voltage is shown in Fig. 3-13. The efficiency at full-load condition is 93.5%, and the maximum efficiency of the converter, which occurs around 2,100 W, is 94%.

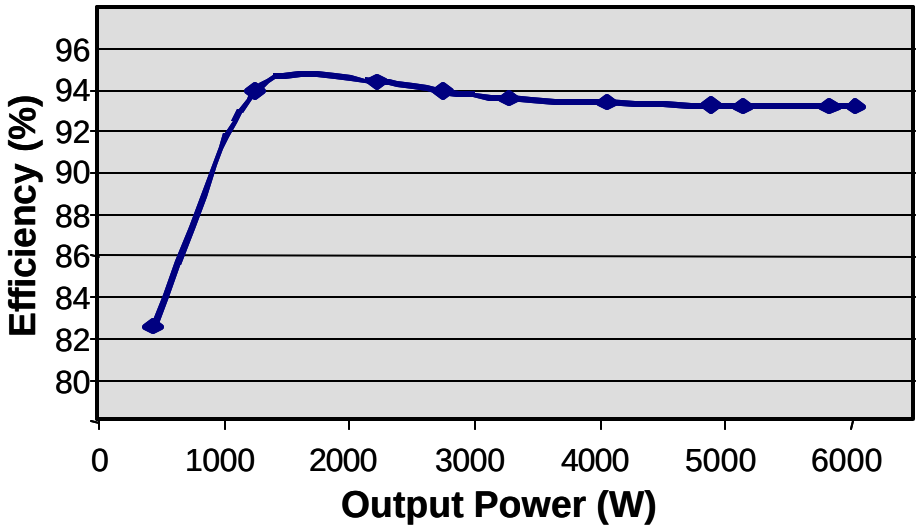


Fig. 3-13. Measured efficiency of the ZVZCS three-level DC/DC converter.

3.5. ZVZCS Three-Level DC/DC Converter Using a Passive Auxiliary Circuit in the Secondary Side

The previous section proposes a novel ZVZCS three-level DC/DC converter using an active clamp as an auxiliary circuit to allow ZCS operation for two of the switches. As can be seen, this converter combines the main advantage of the ZVS three-level DC/DC converter presented in Chapter 2, which is to reduce the voltage stress across the main switches, with the advantages offered by the ZVZCS techniques. One of the disadvantages that this converter presents is the necessity of adding an active switch to reduce the circulating energy during the freewheeling stages. This active switch increases the cost of the converter, and also reduces the overall efficiency of the converter since this active switch is turned off hard at twice the switching frequency.

This section proposes a novel ZVZCS three-level DC/DC converter with a simple auxiliary circuit also in the secondary side, which improves the performance of the converter presented in the previous section.

3.5.1. ZVZCS Operating Mode Using a Passive Auxiliary Circuit in the Secondary Side

In this section, the principle of operation of the ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the secondary side is analyzed. The proposed converter and the timing diagram are shown in Fig. 3-14. It can be seen that the basic structure is similar to that of the ZVS three-level converter proposed in other work [22]. The main difference is the inclusion of the flying capacitor, C_{ss}, to allow the converter to operate with a phase-shift control and ZVS for the outer switches (S_1 and S_4). Also, a passive auxiliary circuit in the secondary side is added to reset the primary current in the transformer and to achieve ZCS operation for the inner switches (S_2 and S_3).

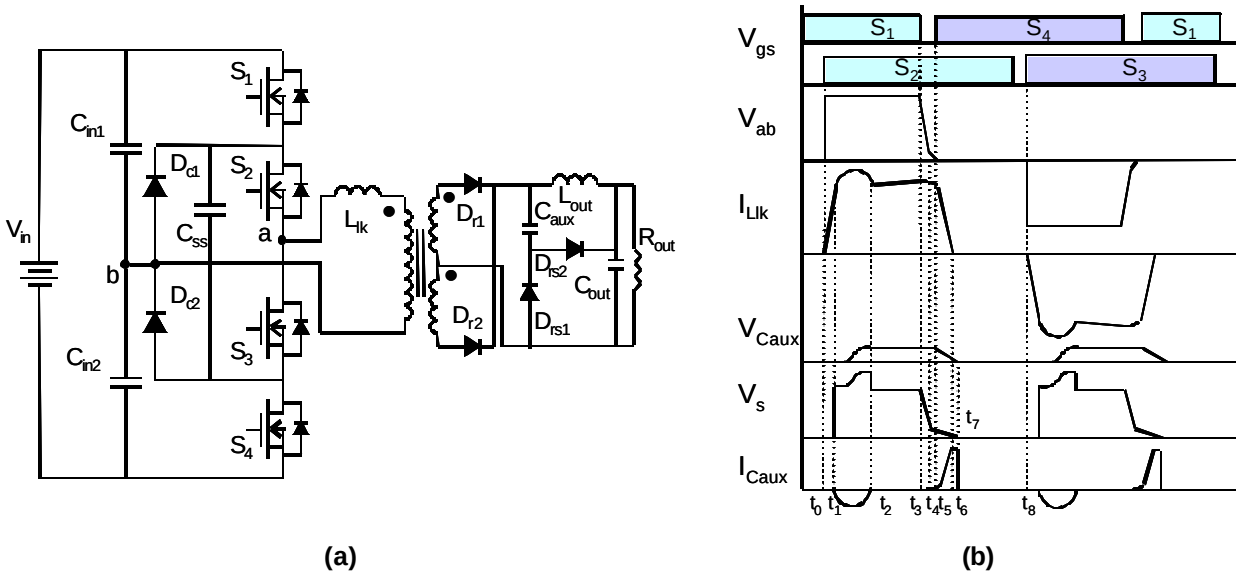


Fig. 3-14. (a) The ZVZCS three-level DC/DC converter using a passive auxiliary circuit and (b) its main waveforms.

The proposed converter has eight stages of operation during a half switching cycle. Similar to the ZVS three-level DC/DC converter discussed in this dissertation, the circuit uses the well-known phase-shift control in which all switches operate with duty cycles of nearly 50%. The phase shift between S_1 and S_2 or S_3 and S_4 determines the operating duty cycle of the converter.

In order to simplify the analysis of the converter, it is assumed that the circuit operation is in steady state, the output voltage and filter inductor current are assumed constant, all the devices are ideal, and the transformer magnetizing current is ignored. The equivalent circuit for each stage of operation is shown in Fig. 3-15. These stages are described below.

[t_0-t_1]: At t_0, S_2 is turned on, and the primary voltage is applied to the primary side of the transformer. The primary current flows through S_1, and S_2 and begins to increase with a slope equal to $V_{in}/(2*L_{lk})$. In the secondary side, the transformer is short-circuited by the rectifiers D_{r1} and D_{r2}, through which the output inductor current is freewheeling. This stage ends when the primary current equals the reflected output filter inductor current.

[t_1-t_2]: At t1, D_{r2} turns off, and the transformer transfers power to the secondary side. The auxiliary diode D_{aux1}, conducts the resonant current between the reflected leakage inductance and the auxiliary capacitor C_{aux}. The latter gets charged up to $2*(V_{in}/(2*n) - V_{out})$.

[t_2-t_3]: In this stage, power continues to be delivered to the output. At the beginning of this stage, D_{aux1} is turned off and the voltage across the rectifier returns to V_{in}/n.

[t_3-t_4]: At t_3, S_1 is turned off, and the reflected filter inductor current charges the parasitic capacitance of S_1 and discharges the parasitic capacitance of S_4 through the auxiliary flying

capacitor C_{ss}. This action continues until the rectifier voltage V_s equals the auxiliary capacitor voltage V_{Caux}, and then D_{aux1} is turned on.

[t_4-t_5]: At the beginning of this stage, a resonance between the leakage inductance and the parasitic capacitances of S_1 and S_4 takes place until the clamp diode Dc1 and the anti-parallel diode D_4 are turned on. During this time, the difference between the filter inductor current and the reflected leakage inductance current discharges $C_{aux.}$

[t_5-t_6]: Once D_4 starts conducting, S_4 can be turned on at t_5 with zero voltage. The primary current freewheels through both clamp diode D_{c1} and S_2. The voltage across the auxiliary capacitor is reflected to the primary and is applied to the leakage inductance. In this way, the primary current is reduced to zero. Also, the auxiliary clamp capacitor supplies energy to the output. This stage ends when the primary current is reset to zero.

[t_6-t_7]: At the beginning of this stage, the primary current has been completely reset and no current flows through the primary side. In the secondary side, the filter inductor current discharges the clamp capacitor C_{aux} to zero, which turns on both rectifier diodes D_{r1} and D_{r2}.

[t_7-t_8]: The conventional freewheeling stage in the PWM converter takes place with the rectifiers short-circuiting the secondary until the end of the cycle. Primary-side conditions remain unchanged, and S_2 can be turned off with zero current in the interval (t_6, t_8). Therefore, IGBT devices are a good choice for S_2 and S_3. At the end of this stage, S_3 is turned on and a new half of a switching cycle begins.

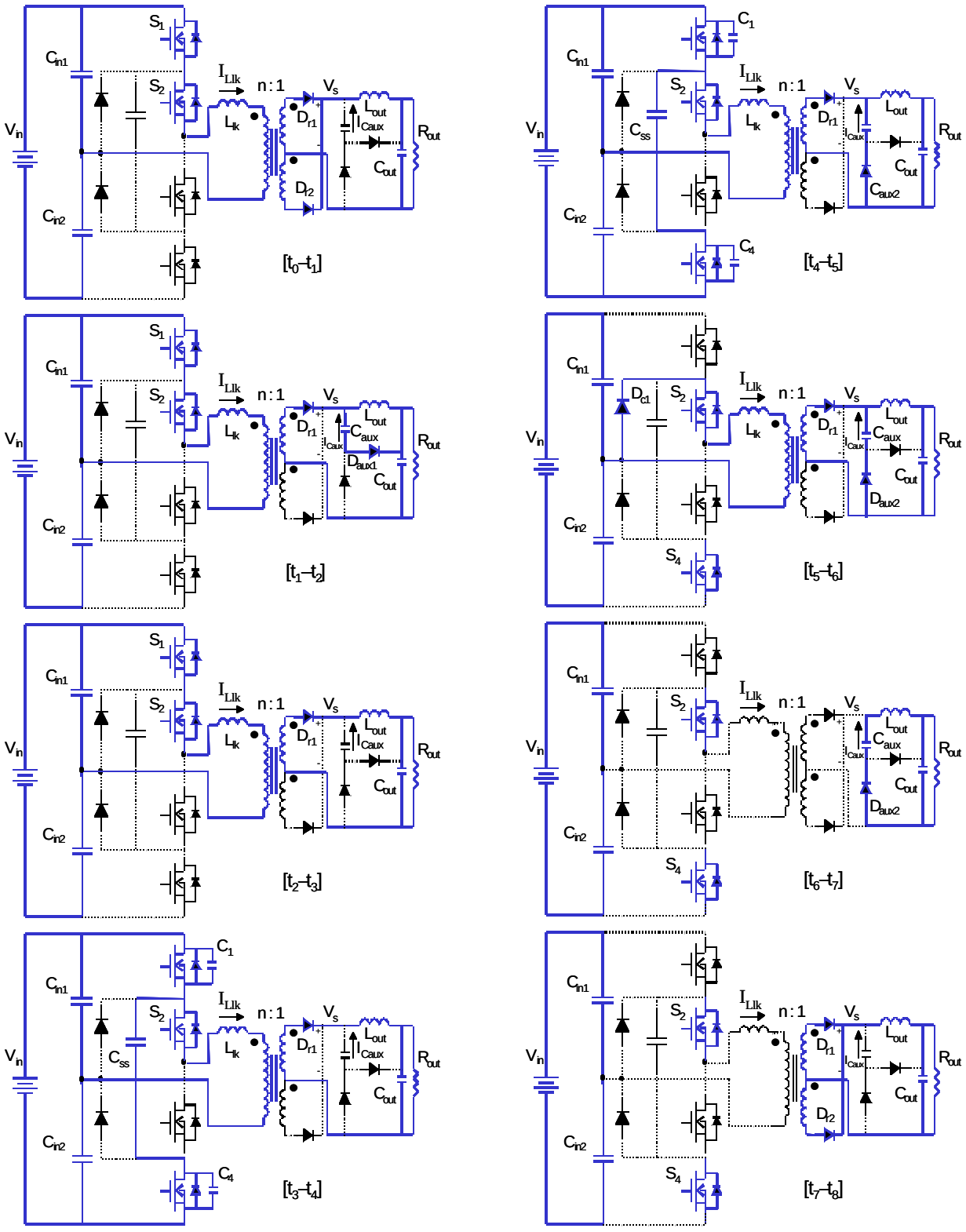


Fig. 3-15. Equivalent circuit for each stage of the ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the secondary side.

3.5.2. Design Guidelines

In the proposed ZVZCS three-level DC/DC converter using an auxiliary active circuit, the turn-on of the auxiliary active switch is synchronized with the turn-off of outer switch S_1 or S_4. In this way, the ZVS operation for these switches is not affected by the reset of the leakage inductance by auxiliary capacitor C_{aux}. In the ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the secondary side, this synchronization cannot be carried out in a simple way. When S_1 is turned off, the reflected filter inductor current charges and discharges the parasitic capacitance of S_1 and S_4, respectively. The evolution of the voltage across the parasitic capacitance during this stage is given as:

$$v_{C_1} = \frac{I_0}{n(C_1 + C_4)} t \tag{3-13}$$

and

$$v_{C_4} = \frac{1}{2} V_{in} - \frac{I_0}{n(C_1 + C_4)} t \,. \tag{3-14}$$

This stage ends when the rectifier voltage V_s equals the voltage in the auxiliary capacitor C_{aux}. Therefore, at the end of this stage, the voltage across C_4 is given by:

$$V_{C_4}(t_4) = 2n\left(\frac{V_{in}}{2n} - V_{out}\right). \tag{3-15}$$

The duration of this interval is given by:

$$\Delta_{t_3 - t_4} = \frac{1}{2}(V_b - 2nV_x) n \left(\frac{C_1 + C_4}{I_0}\right). \tag{3-16}$$

At the beginning of the stage (t_4-t_5), a new resonance begins between L_{lk} and the parasitic capacitance of the switches S_1 and S_4. On the secondary side of the transformer, the difference between the filter inductor current and reflected leakage inductance current discharges the auxiliary capacitor C_{aux}. In order to complete the ZVS operation for S_1 and S_4, the energy in the leakage inductance must be sufficient to continue discharging the parasitic capacitance of the switch. In addition, it has to be considered in this process that the current in the leakage inductance has also been reset by the reflected voltage in the auxiliary capacitor C_{aux}.

The evolution of the voltage across the parasitic capacitor of S_4 and S_1 in this stage is given by

$$v_{C_1} = \frac{-1}{n}[n^2 V_x - V_{in} n - \frac{I_o t}{(C_a + C_{eq})} - \frac{C_a^2 L_{lk} I_o w_{r_2}}{(C_a + C_{eq})^2} \sin(w_{r_2} t)] \quad (3\text{-}17)$$

and

$$v_{C_4} = \frac{1}{n}\left[n^2 V_x - \frac{I_o t}{(C_a + C_{eq})} - \frac{C_a^2 L_{lk} I_o w_{r_2}}{(C_a + C_{eq})^2} \sin(w_{r_2} t) \right], \quad (3\text{-}18)$$

where V_x is the voltage across the parasitic capacitor at time t_4, and C_a is the auxiliary capacitor reflected to the primary side. The equivalent capacitance, the C_{eq} and the resonant frequency ω_{r2} are expressed as:

$$C_{eq} = C_1 + C_4 \quad (3\text{-}19)$$

and

$$w_{r_2} = \sqrt{\frac{C_a + C_{eq}}{L_{lk} C_a C_{eq}}}. \quad (3\text{-}22)$$

At the end of this stage, the voltage across the parasitic capacitances C_1 and C_4 should be $V_{in}/2$ and zero, respectively, to satisfy ZVS operation. Combining the previous assumptions with (3-18), we can obtain the minimum leakage inductance needed to achieve ZVS operation under a certain load condition and with different turns ratios, as shown in Fig. 3-16. It can be seen that one way to increase the ZVS range is by increasing the L_{lk} inductance of the transformer. This idea is not recommended, since more energy is needed to reset the primary current of the transformer. Therefore, this circulating energy will decrease the efficiency of the converter. As can also be seen in Fig. 3-16, increasing the turns ratio of the transformer can reduce the converter's dependence on L_{lk} to achieve ZVS operation for the outer switches. Maximizing the turns ratio of the transformer is an approach commonly used to reduce the conduction losses in the primary side.

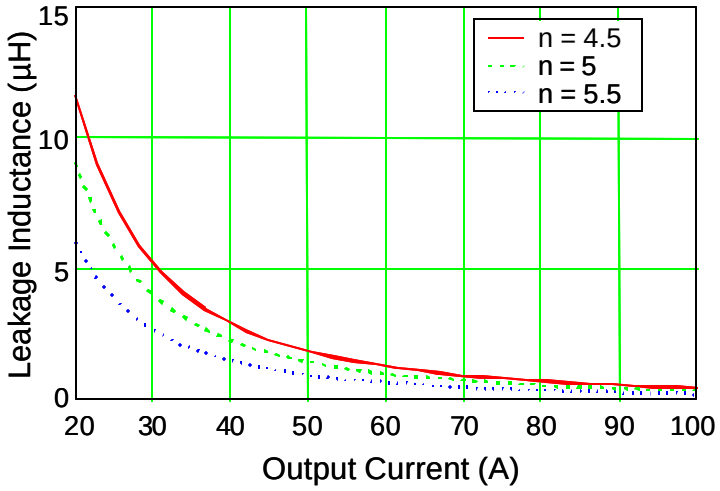


Fig. 3-16. Minimum leakage inductance for ZVS operation in the proposed ZVZCS three-level converter with a passive auxiliary circuit.

3.5.3. Experimental Results

An experimental prototype was built in order to verify the operation of the ZVZCS three-level DC/DC converter with a passive circuit. The specifications of the prototype are as follows: V_{out} = 42-58 V, I_{out} = 115 A, V_{in} = 660 – 800 V, and F_s = 100 kHz.

The power stage shown in Fig. 3-14 consists of the following components.

S_1 - S_4: APT60M75JVR

D_{r1} – D_{r2}: HFA140MD60C

D_{c1} – D_{c2}: BYV34-500

C_{in1}, C_{in2}, C_{ss}: 4*1 µF/600V – polypropylene

T_r: E65-3F3

L_{lk}: 2.2 µH

D_{aux1}, D_{aux2}: IXYSDSE160-05A

C_{aux}: 0.22 µF

L_{out}: EC55-3C85*2, 16 µH

C_{out}: 220 µF/250V – electrolytic

The turns ratio of the transformer is designed to achieve high output voltage at low-line input-voltage conditions. Then, the transformer is selected to be a center-tapped transformer with a turns ratio equal to 5, and with 10/2/2 turns in the primary and secondary sides.

Taking into account that the ZVS action for outer switches S_1 and S_4 is achieved using the reflected output current, the leakage inductance can be reduced as much as possible. In this way, the primary current is brought to zero in a short time, thus reducing the duty-cycle loss. An interleaved technique is used to build the transformer, facilitating a drastic reduction in the leakage inductance.

Experimental waveforms of the proposed converter at full load and high-input voltage, and the experimental measured efficiency as a function of the output load at low input-voltage conditions, are shown in Figs. 3-17, 3-18, 3-19 and 3-20.

Fig. 3-17 shows the primary voltage in the transformer (upper trace), the voltage across the output rectifier (middle trace), and the primary current in the transformer (lower trace). It is important to notice that, due to the reduction of L_{lk}, the secondary rectifier voltage does not present ringing. Fig. 3-18 shows the detail of the primary current. It can be seen that the freewheeling primary current is quickly reset to zero after the end of the power-transfer stage. Therefore, S_2 and S_3 are turned off with ZCS.

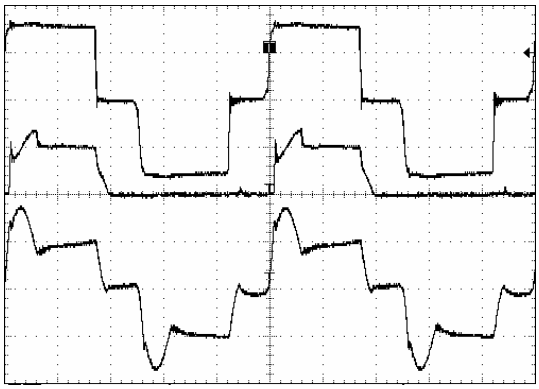


Fig. 3-17. Voltage (upper trace) and current (lower trace) waveforms of the transformer primary side and rectifier secondary voltage (middle trace) waveforms (250 V/div, 100 V/div, 20 A/div, 2μs/div).

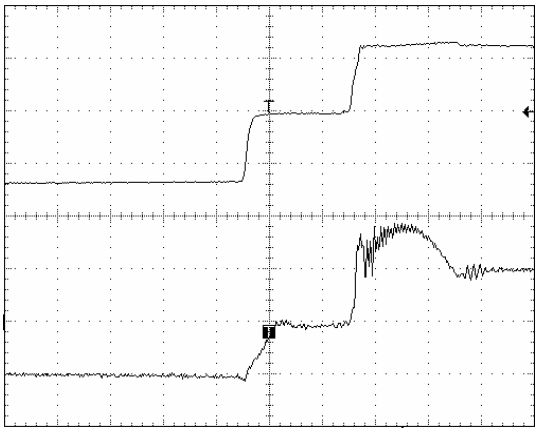


Fig. 3-18. Details of the voltage and current in the primary side (250 V/div, 20 A/div, 500 ns/div).

The drain-to-source voltage across the power switch V_{DS}, (upper trace) and its gate signal voltage (lower trace), are shown in Fig. 3-19. It can be seen that V_{DS} is 400 V, which is half of

the level of the input voltage. Also, it can be appreciated that the voltage falls to zero prior to the turn-on of the gate signal. Therefore, true ZVS action is achieved.

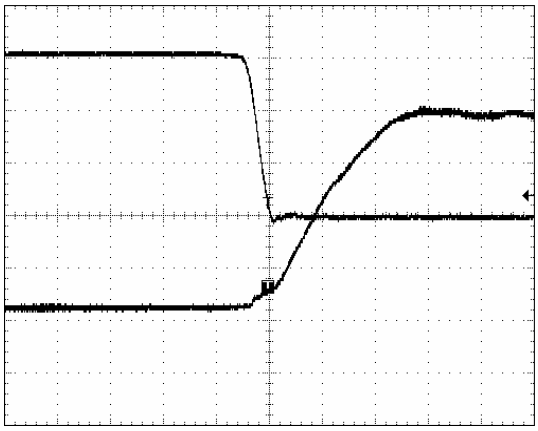


Fig. 3-19. Drain-to-source and gate voltage waveforms of S_1 (125 V/div, 5V/div, 100ns/div).

Fig. 3-20 shows the experimental measured efficiency as a function of the load at nominal input voltage (800 V) and nominal output voltage (52 V). The efficiency at full-load condition is 95.1%, and the maximum efficiency of the converter, which occurs around 2,400 W, is 96.2%. It is important to mention that the efficiency at full-load condition is higher than those achieved by the ZVS and the ZVZCS three-level converters presented in the previous sections. These improvements are due to the diodes in the auxiliary circuit that operate with almost zero switching losses.

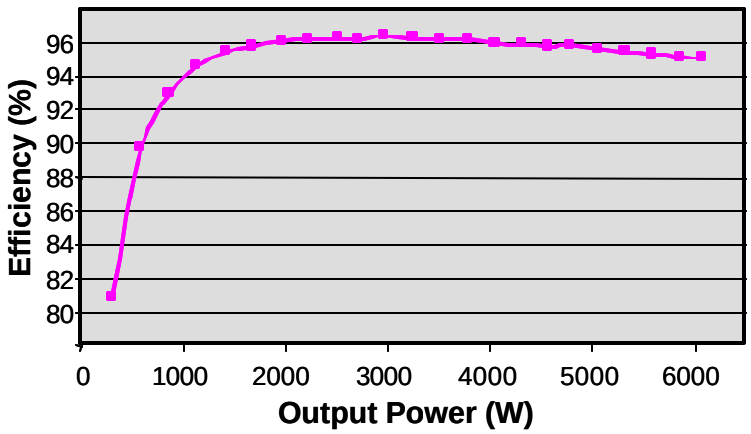


Fig. 3-20. Measured efficiency of the ZVZCS three-level DC/DC converter using a passive auxiliary circuit.

3.6. ZVZCS Three-Level DC/DC Converter Using a Passive Auxiliary Circuit in the Primary Side

This section of the dissertation presents a ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the primary side. The proposed converter and its timing diagram are shown in Fig. 3-21.

As can be seen, the primary side of the converter remains similar to the three-level structure presented in this dissertation. The only difference is the inclusion of an auxiliary circuit in the primary side, which is added in order to achieve ZVZCS operation. The auxiliary circuit consists of only two diodes and a small three-winding auxiliary transformer. The primary winding of the auxiliary transformer is connected in series with the primary winding of the main transformer. The two secondary windings of the auxiliary transformer are connected between the auxiliary diodes and the outer leg switches. Similar to the previous three-level converters presented in this dissertation, the inclusion of the flying capacitor C_{ss} allows phase shift operation and ZVS conditions for the outer switches S_1 and S_4. ZVS operation is achieved by using the output current reflected to the primary side. The inner switches S_2 and S_3 operate under ZCS conditions with the assistance of the auxiliary circuit, which provides reset voltage and absorbs the stored energy in the leakage inductance L_{lk}. In this case, L_{lk} is the sum of the leakage inductances of the main transformer and the auxiliary transformer. The auxiliary circuit operates according to the primary current. Diode D_{A1} is turned on when the primary current i_{lk} is positive, and diode D_{A2} is turned on when I_{lk} is negative.

3.6.1. ZVZCS Operating Mode Using a Passive Auxiliary Circuit in the Primary Side

In this section, the operating principle of the ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the primary side is presented.

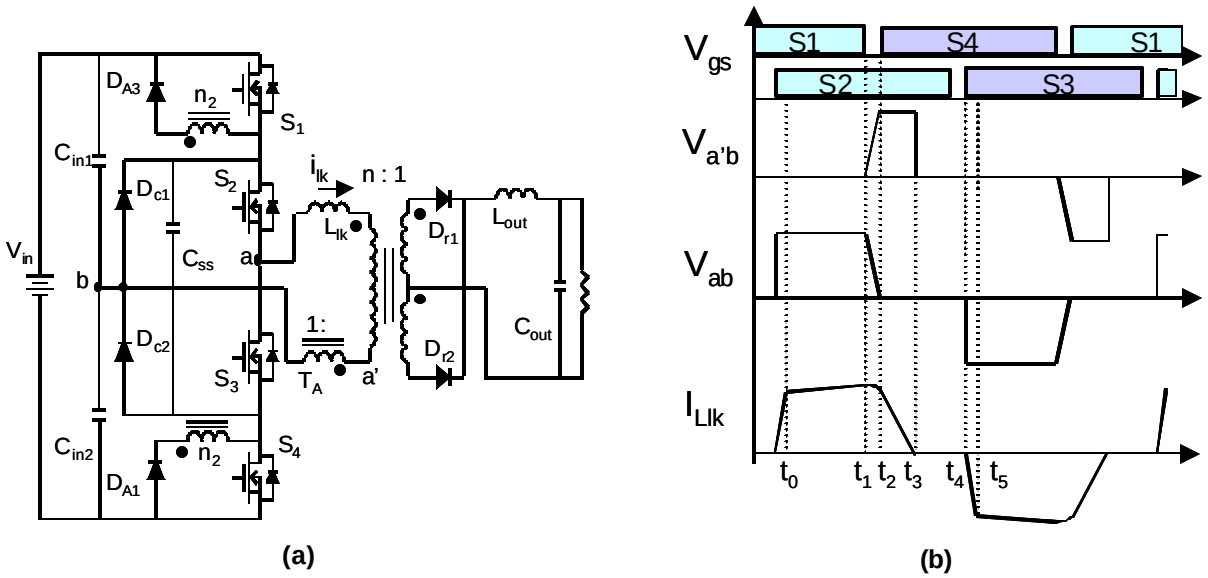


Fig. 3-21. (a) ZVZCS three-level DC/DC converter using an auxiliary circuit in the primary side and (b) its main waveforms.

The proposed converter has five stages of operation during each half of a switching cycle. In order to simplify the analysis of the converter, it is assumed that the circuit operation is in steady state, all the devices are ideal, the magnetizing inductances of the main and auxiliary transformer are ignored, and the initial voltage across C_{ss} is assumed to be half the level of the input voltage. The equivalent circuit for each stage of operation is shown in Fig. 3-22. These stages are described as follows.

[t_o-t_1]: During this stage, S_1 and S_2 are conducting, and the input power is delivered to the output through both the main transformer and D_{r1}. The secondary sides of the auxiliary transformer are short-circuited by D_{A1} and S_1. Therefore, the voltage across the auxiliary transformer is zero. The current flowing through S_1 is given by

$$i_{S_4} = \left(1 + \frac{1}{n_2}\right) i_{lk} . \tag{3-23}$$

[t_1-t_2]: At t_1, S_1 is turned off, and a resonance begins between C_1, C_2, C_{ss}, L_{lk} and L_{out}. C_{ss} couples C_1 and C_4 and assists with the zero-voltage turn-on of S_4. The equivalent circuit is shown in Fig. 3-22. The evolution of the voltage across the parasitic capacitance of S_1 is given by

$$V_{C_1} = \frac{n_2}{1+n_2}\left(\left(\frac{1}{2}V_{in} - n V_{out}\right)(1 - \cos(t - t_1)) + I_{lk}(t_1) Z_o \sin w_o (t - t_1)\right), \tag{3-24}$$

and the primary current i_{lk} is given by

$$i_{lk} = \frac{\frac{1}{2}V_{in} - n V_{out}}{Z_o} \sin(t - t_1)) + I_{lk}(t_1) \cos w_o (t - t_1)), \tag{3-25}$$

where

$$w_o = \sqrt{\frac{1}{L_{eq} C_{eq}}}, \tag{3-26}$$

$$Z_o = \sqrt{\frac{L_{eq}}{C_{eq}}}, \tag{3-27}$$

$$L_{eq} = L_{lk} + n L_{out}, \tag{3-28}$$

$$C_{eq} = \left(C + \frac{C C_{ss}}{C + C_{ss}}\right)\left(\frac{n_2}{1+n_2}\right)^2, \tag{3.29}$$

and

$$C = C_1 = C_4 . \tag{3-30}$$

The voltage across the parasitic capacitance of S_4 is given by

$$V_{C_4} = \frac{1}{2}V_{in} - \frac{C_{ss}}{C + C_{ss}}V_{C_2}. \tag{3-31}$$

Since the duration of this stage is long and that n^2L_{lk} is large, the primary current i_{lk} is considered nearly constant during this interval. This stage ends when the voltage across the parasitic capacitance of S_1 reaches $V_{in}/2$ and clamping diode D_{c1} begins to conduct. At the same time, assuming $C<<C_{ss}$ in (3-31), the voltage across the parasitic capacitance of S_4 reaches zero, and anti-parallel diode D_4 begins to conduct. Hence, S_4 can be turned on with ZVS, which leads to the conclusion that C_{ss} should be sufficiently large to ensure ZVS. In addition, the voltage across S_1 increases smoothly to $V_{in}/2$, which results in zero-voltage turn-off for S_1.

[t_2-t_3]: This stage starts when the primary current freewheels through both S_2 and clamping diode D_{c1}. Half of the input voltage is applied across the secondary winding of the auxiliary transformer and is reflected to the primary one, as shown in Fig. 3-22. In this way, the primary current is reduced to zero as

$$i_{lk} = I_{lk}(t_2) - \frac{V_{aux}}{L_{lk}}(t - t_2), \tag{3-32}$$

where V_{aux} is the reflected voltage of the input DC side through the auxiliary transformer, acting to reset the primary current, and which is given by

$$V_{aux} = \frac{1}{2}\frac{V_{in}}{n}. \tag{3-33}$$

[t_3-t_4]: This stage starts after the primary current becomes zero. During this stage, the primary current remains at zero. Therefore, the circulating energy in the primary side is reduced due to

ZVZCS operation. In the secondary, the load current freewheels evenly through the diode rectifiers D_{r1} and D_{r2}, as shown in Fig. 3-22. Also during this stage, S_2 is turned off with ZCS condition.

[t_4-t_5]: At t_4, S_3 is turned on, and half of the input voltage is applied to the primary side of the transformer. The secondary terminals of the auxiliary transformer are short-circuited by D_{A1} and S_4. In addition, the primary current flows through S_3 and S_4 and begins to increase with a slope equal to $V_{in}/(2L_{lk})$. Meanwhile, the load current flowing through D_{r1} is diverted to D_{r2} as i_{lk} increases. At the end of this stage, the primary current reaches the reflected output current, starting a new a half of a switching cycle.

3.6.2. Design Considerations

A. Conditions for ZVZCS Operation

The zero-voltage turn-off of switch S_1 is natural, as C_{eq} is connected in parallel with S_1. In a full-bridge DC/DC converter, if v_{c1} reaches the level of the DC-link voltage, a safe zero-voltage turn-on of S_4 can be attained. In this three-level DC/DC converter, however, one more condition is needed, because although v_{c1} reaches $V_{in}/2$ at the end of the time interval (t_1-t_2), v_{c4} is not exactly zero. Its final voltage depends on the ratio of C_{ss} to C. To achieve safe ZVS turn-on for S_4, the final voltage of v_{c4} must be less than the on-voltage of the switch. The extra condition is given by

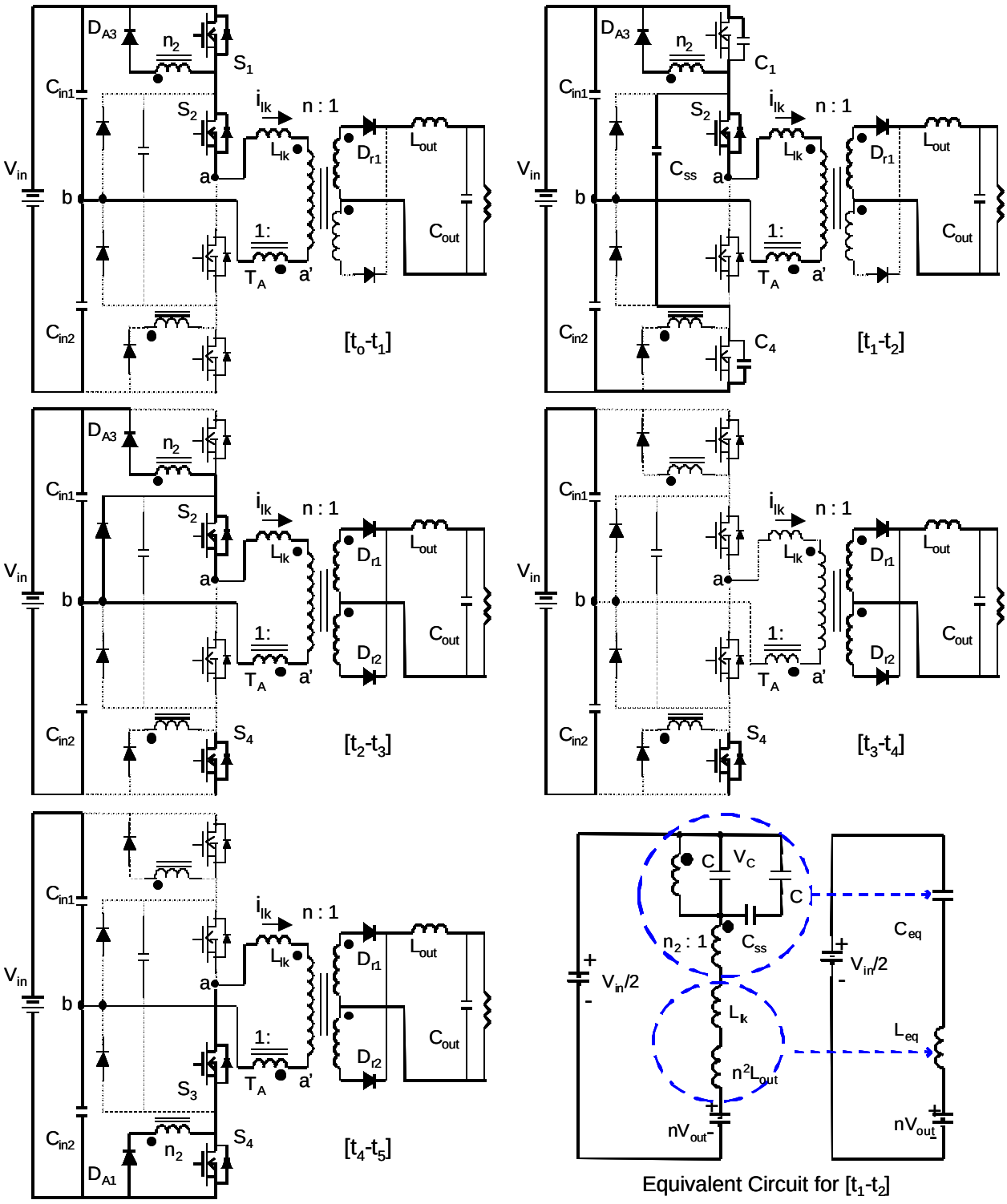


Fig. 3-22. Equivalent circuit for each stage.

$$C_{ss} > C\left(\frac{V_{in}/2}{V_s} - 1\right), \tag{3-34}$$

where V_s is the on-voltage of the switch.

As mentioned during the description of the operating stages, the primary current i_{lk} is nearly constant during time interval (t_1-t_2), since n^2L_{out} is large and the time interval is short. The time interval given to switches S_1 and S_4 for ZVS operation is expressed in given by (3-35), and it is easily designed by selecting the appropriate C_{eq}. Accordingly, the rate of change of the voltage across the outgoing switch is adjustable, as follows:

$$T_{ZVS} = t_2 - t_1 = C_{eq}\frac{V_{in}/2}{I_{lk}}. \tag{3-35}$$

During stage (t_2-t_3), zero-current turn-off operation in the inner switches is accomplished by eliminating the primary current prior to removing the gate pulse of S_2. The approximate time interval required to eliminate the primary current is given by

$$T_{ZCS} = t_3 - t_2 = \frac{L_{lk}\, I_{lk}}{V_{aux}}. \tag{3-36}$$

This ZCS operation does not depend on the output voltage, and can be achieved regardless of the output voltage if the DC-link voltage is established. The T_{ZCS} is at its maximum when the current is at its maximum, and the maximum T_{ZCS} is given by

$$T_{ZCS} = \frac{L_{lk}\, I_{lk_{\max}}}{V_{aux}}, \tag{3-37}$$

where I_{lkmax} is the maximum current allowed.

The condition for safe ZCS operation is given by

$$T_{ZCS_{\max}} < (1 - D_{\max})T_s, \tag{3-38}$$

where D_{max} is the maximum duty cycle, and T_s is the switching period.

B. Conduction Loss and Limitation of the Proposed Circuit

The additional loss in the proposed circuit and the reduction of freewheeling loss depend on n_2, so it can be optimized the loss by an appropriate n_2. Combining (3-33), (3-37) and (3-38) determines the range of n_2 such that the reset voltage ensures ZCS operation, as follows:

$$n_2 < \frac{2p(1 - D_{\max})}{\%Z_{lk}}, \tag{3-39}$$

where ω_s is the switching angular frequency, and

$$\%Z_{lk} = \frac{w_s L_{lk} I_{lk}}{V_{in}/2}. \tag{3-40}$$

In a case of low duty cycle, the ratio of turns for the auxiliary transformer is decided within the range given in (3-39) such that the conduction loss may be minimized. Assuming that the primary-side switches have the same on-voltage, the respective conduction losses of the ZVS and ZVZCS DC/DC converters can be obtained as follows:

$$P_{loss_{ZVS}} = 2V_s I_{lk}, \tag{3-41}$$

and

$$P_{loss_{ZVZCS}} = 2V_s I_{lk}\left(1+\frac{1}{n_2}\right)D + V_s I_{lk}(1+n_2)\frac{\%Z_{lk}}{2p}, \quad (3\text{-}42)$$

where V_s is the on-voltage of the switches, and D is the duty cycle.

In (3-42), the power loss in the ZVZCS converter is minimized when n_2 is set as follows:

$$n_2 = 2\sqrt{\frac{pD}{\%Z_{lk}}}. \quad (3\text{-}43)$$

From (3-38) and (3-43), the range of maximum for D can be obtained such that the conduction loss in the ZVZCS converter does not become higher than that of the ZVS converter, as given by

$$D < \left(1-\frac{1}{2}\sqrt{\frac{\%Z_{lk}}{p}}\right)^2. \quad (3\text{-}42)$$

3.6.3. Experimental Results

A 6KW experimental prototype was built and tested in order to verify the operation of the ZVZCS three-level DC/DC converter with a passive auxiliary circuit in the primary side. Similar to the previous ZVZVS approaches, it was designed for use in communication applications. The normal operating voltage is 800 V, and the final voltage at hold-up time is 660 V. The operating frequency is 100 kHz, and the switching frequency is 200 kHz.

The power stage shown in Fig. 3-21 consists of the following components.

$S_1 – S_4$: APT60M75JVR

$D_{r1} – D_{r2}$: HFA140MD60C

T_r: E65 – 3F3

L_{lk}: 1.2μH

$D_{c1} - D_{c2}$: BYV34-500 T_A: EI30- PC40

$D_{A1} - D_{A2}$: RHRP860CC L_{out}: 2xEC55-3C85, 16µH

C_{in1}, C_{in2}, C_{ss}: 4x1µF/600V – polypropylene C_{out}: 220µF/250V – electrolytic

The turns ratio of the transformer and the winding technique for reducing the leakage inductance are similar to those given for the previous ZVZCS converters.

Experimental waveforms of the proposed converter at full load and the experimental measured efficiency as a function of the output loads at nominal input voltage condition are shown in Figs. 3-23, 3-24, 3-25 and 3-26.

Fig. 3-23 shows the main waveforms for the proposed ZVZCS converter using an auxiliary circuit in the primary side. In this case, the upper trace is the primary voltage in the transformer, the middle trace is the voltage of the secondary winding of the auxiliary transformer T_A, and the bottom trace is the primary current of the main transformer. Similar to the previous ZVZCS approaches, it can be seen that the primary current is reset during the freewheeling time, which reduces the circulating energy and allows ZCS operation for the inner switches. Also, it can be seen that the reset voltage is introduced during the interval $[t_2 - t_3]$, after the primary voltage drops to zero and disappears when the primary current is reduced to zero.

Fig. 3-24 shows the drain-to-source voltage and the gate signal for the switch S_1 that operates under ZVS. It can be seen that the voltage falls to zero prior to the turn-on of the gate signal, which means ZVS operation is achieved.

Fig. 3-23. Voltage (upper trace) and current (lower trace) waveforms of the transformer primary-side and secondary voltage (middle trace) of the auxiliary transformer (500V/div, 500V/div, 20A/div, 2µs/div).

One of the advantages offered by the proposed converter is that under short-circuit operation, the soft-switching capability is maintained as shown in Fig. 3-25. For this operating condition, the output terminal is shorted with 0.022 ohms of wire, resulting in an output current of 90 A. From this figure, it can be seen that ZCS operation is guaranteed even when the output terminal of the converter are shorted.

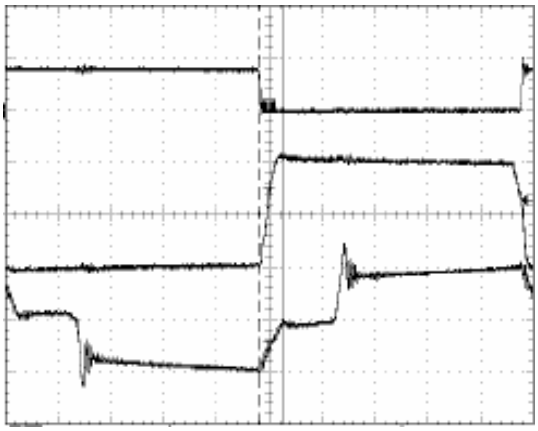


Fig. 3-24. Drain-to-source (upper trace) and gate voltage (lower trace) waveforms of S_1 and primary current (middle trace) (500V/div, 10V/div, 20A/div, 1µs/div).

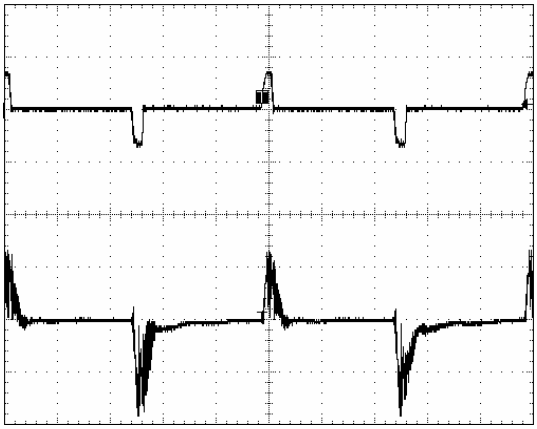


Fig. 3-25. Voltage (upper trace) and current (lower trace) waveforms of the transformer primary side under short-circuit condition (500V/div, 20A/div, 2µs/div).

Fig. 3-26 shows the experimental efficiency as a function of the load at nominal input voltage and nominal output (52 V) voltage. The efficiency at full-load condition is 94.5%, and the maximum efficiency of the converter, which occurs around 3500 W, is 96.2%.

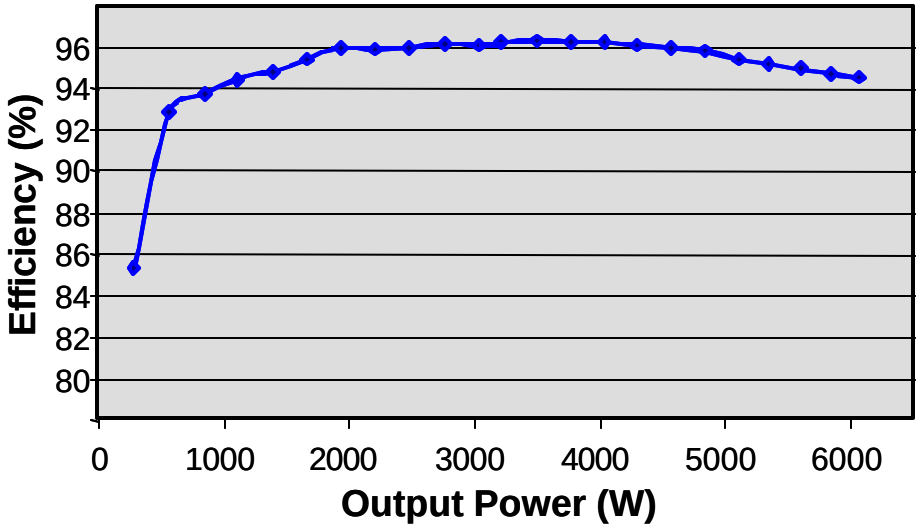


Fig. 3-26. Measured efficiency of the ZVZCS three-level DC/DC converter using an auxiliary circuit in the primary side.

Fig. 3-27 shows the measured efficiency comparison at 800V input voltage for the ZVS and ZVZCS three-level DC/DC converters presented in this dissertation. As can be seen, the efficiencies for all ZVZCS converters are higher than that achieved by the ZVS three-level converter. This improvement in the efficiency is due to the reduction of the circulating energy in

the converter and its higher effective duty cycle, which allows it to be designed with a higher turns ratio. The highest efficiency at full-load condition is slightly better for the ZVZCS three-level converter using a passive circuit in the secondary side. Its auxiliary circuit presents fewer losses and provides snubbing for the secondary rectifiers.

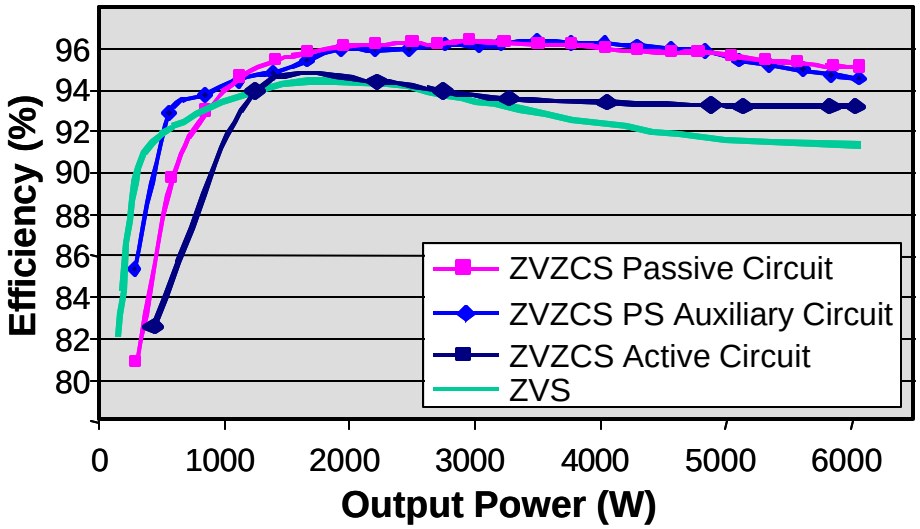


Fig. 3-27. Measured efficiency comparison of the proposed ZVS and ZVZCS three-level DC/DC converters

3.7. Conclusion

This chapter presented the benefits obtained by implementing ZVZCS techniques in the proposed three-level DC/DC converter with phase-shift control operation. The chapter presented the analysis, implementation and comparison of three ZVZCS approaches using an active and passive auxiliary circuit in the secondary side and a passive circuit in the primary side. This approach resulted in novel ZVZCS three-level DC/DC converters for high-voltage applications, and combined the advantages of reduced voltage stress across the main switches, achieved by the use of three-level structures, with the advantages of reduced circulating energy, as offered by ZVZCS soft-switching operation. In all cases, experimental results from 6kW prototypes operating at 100 kHz were shown in order to demonstrate the operation of the converters.

A ZVZCS three-level DC/DC converter using an active auxiliary circuit was first presented in this chapter. The use of an active device allows an easy synchronization with the operation of the primary devices. In this way, the inner switches S_2 and S_3 operate with ZCS operation without interfering with the ZVS operation of the outer switches. In addition, the auxiliary circuit in the secondary side clamps the voltage across the diode rectifiers, which offers a good opportunity to use 200V diodes, thus reducing the conduction losses in the secondary side. One disadvantage of this converter is the necessity of adding an active switch to reduce the circulating energy that exists during the freewheeling stages. This active switch increases the cost of the converter, and also reduces the overall efficiency of the converter, since this active switch is turned off hard at twice the switching frequency.

In order to improve the previous approach, a ZVZCS three-level DC/DC converter using an auxiliary passive circuit in the secondary side was presented. The auxiliary circuit was implemented with just two diodes and one capacitor, reducing the complexity and cost of the previous approach. In addition, this auxiliary circuit improves the efficiency of the converter, since it achieves lower conduction and switching losses. Taking into account that by using a passive circuit the ZVS operation of the switches S_1 and S_4 is affected by the ZCS operation, the design guidelines were given in order to guarantee ZVS operation of the outer switches. In this way, the leakage inductance of the transformer can be reduced as much as possible. As a result, both the circulating energy in the primary side of the three-level converter and the secondary-side ringing across the output rectifiers are drastically reduced.

The ZVZCS three-level DC/DC converter using a passive auxiliary circuit in the primary side was the last converter presented in this chapter. One of the main characteristics of this converter

is its ability to maintain soft-switching operation even in short-circuited conditions or at start-up. Because of the ZVZCS mechanism, it was shown that this soft-switching technique presents a better performance in applications that require low-duty-cycle operation. Since the duty cycle of the DC/DC converter for DPSs should be maximized, this analysis included the operating condition at which this converter achieves its minimum losses.

The characteristics presented by the three approaches make the proposed converters an interesting option for high-voltage, high-power applications that require high efficiency.

It is important to mention that because of the relevance of the results presented in this work, other authors have adopted the idea of combining three-level structures with ZVZCS operation in front-end converters for high-power three-phase DPS applications [115]-[119].

4. Resonant Three-Level DC/DC Converters for High-Power Distributed Power Systems

4.1. Introduction

One of the requirements for the next generation of power supplies for high-power DPSs is that they achieve high power density with high efficiency. In order to meet this requirement, it is usually necessary for them to operate at higher switching frequencies. As switching frequencies increase, the switching losses associated with the turn-on and turn-off of the devices also increase. Previous chapters proposed a PWM converter based on a three-level structure. The operation with phase-shift control allows the implementation of ZVS and ZVZCS soft-switching techniques in the converter. It was shown that ZVZCS techniques are advantageous in applications in which the wide input-voltage variations result in high circulating energy in the converter. As a result, the proposed converter offers advantages in high-voltage, high-power applications that require high efficiency.

Despite the good performance of the proposed PWM converter, the switching losses can be high enough to prohibit operation at very high frequencies, even when soft-switching techniques are used. In addition, the reverse-recovery problem in the secondary diode rectifiers becomes a big concern. In order to minimize these problems, it is required that soft-switching techniques not only minimize the turn-on and turn-off losses for the primary devices, but also that they solve the reverse-recovery problem in the diode rectifiers [67],[68].

This chapter presents a study of several resonant DC/DC converters that can operate at higher switching frequencies with the ultimate aim of increasing the power density in the DPS. From

this study, a novel ZVS resonant DC/DC converter, which overcomes some problems presented in the traditional PWM and resonant converters, is proposed.

4.2. Effect of Wide Input-Voltage Variations in the Performance of Resonant Converters

This section of the dissertation presents the effect of the wide input-voltage variations on the performance of the resonant converter. The series resonant converter shown in Fig. 4-1 is used as an example to illustrate this problem. Since the main interest in this dissertation is high-voltage applications, the converter is also implemented by using a three-level structure. Similar to the traditional full-bridge series resonant converter with variable-frequency control, the switches operate in pairs, S_1-S_2 or S_3-S_4 with duty cycles of nearly 50% to regulate the output voltage.

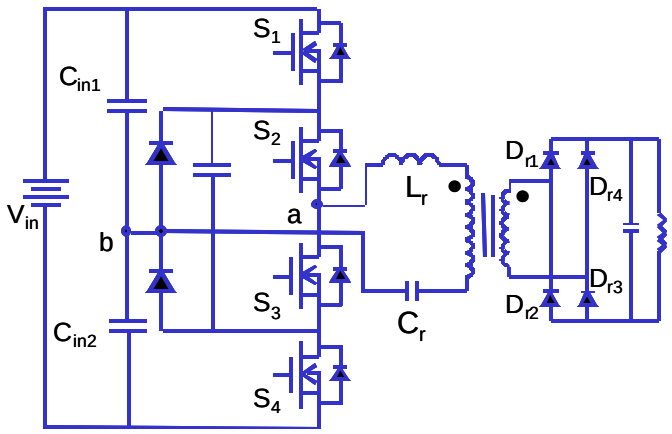


Fig. 4-1. ZVS three-level series resonant converter.

Fig. 4-2 shows the DC gain characteristic for the series resonant converter. For ZVS operation, the converter must be operated with a switching frequency higher than the resonant frequency of the tank. For an optimal design in which the circulating energy in the converter and the turn-off losses for the primary devices are minimal, the converter should work close to both the resonant frequency and close to the peak where the gain in the converter is higher. In this way, the turns

ratio of the transformer is maximized, which reduces the conduction losses for the primary devices. However, for wide input-voltage and output-load variations, such as those existing in high-power DPSs, the desired operation point is difficult to attain. Fig. 4-2 also shows the operating region of the converter for the typical application addressed in this dissertation, where hold-up time is a requirement. As can be seen, the converter operates far away from the optimal operating point during normal operating conditions. In addition, the converter operates with a wide frequency variation to provide output regulation, which complicates the optimization of the transformer as well as its input and output filters.

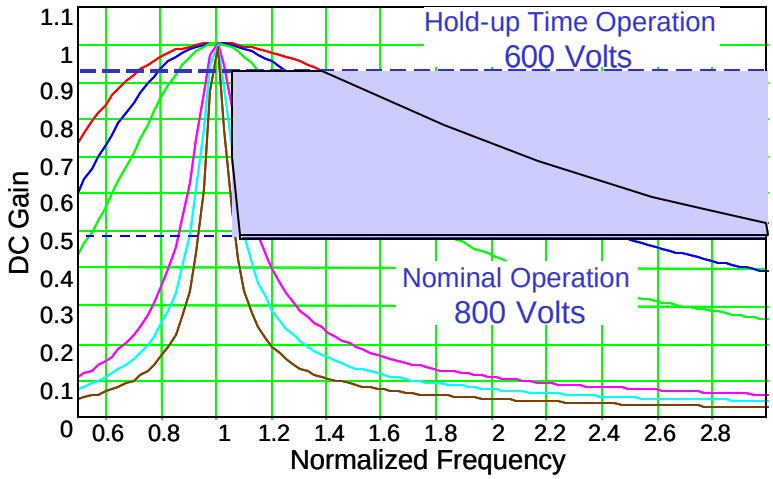


Fig. 4-2. Operating trajectory for the ZVS three-level series resonant converter under wide input-voltage variations.

Fig. 4-3 shows the projected efficiency for the ZVS three-level resonant converter under wide-input voltage variations. At 800V input voltage, the converter presents higher circulating energy and high turn-off losses, resulting in a low efficiency at the nominal operating point. It is important to mention that the thermal design must be designed at this point, which penalizes the weight and power density of the converter.

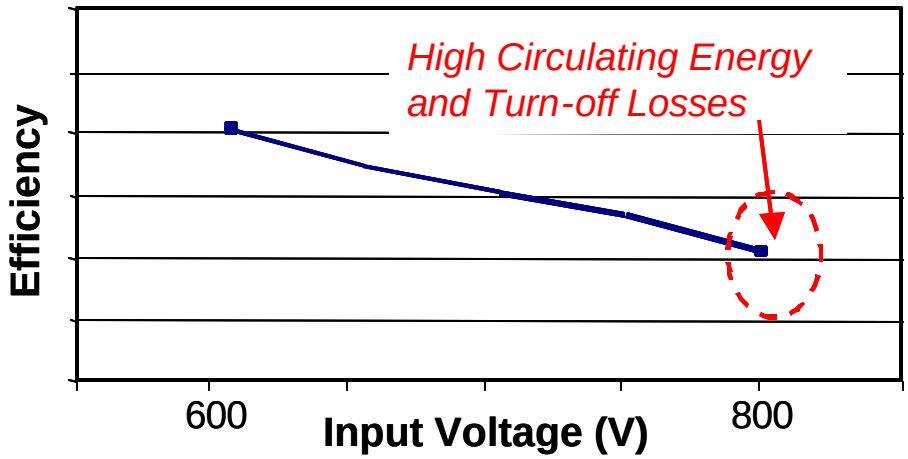


Fig. 4-3. Projected efficiency for the series resonant converter under wide input-voltage variations.

The next section presents a three-level resonant converter that overcomes the low-efficiency characteristic at the nominal operating point by using a higher-order resonant tank.

4.3. ZVS Three-Level LLC Resonant Converter

As discussed in the previous section, one of the problems presented by the resonant converters is the converter's low efficiency when it is designed to meet specifications that include wide input-voltage and load-range variations. For applications in which the converter must achieve ZVS operation for the main devices under wide load variations, the resonant tank must be designed with high Q factors, and the switching/resonant frequency ratio must be increased. As a result, the input-output voltage gain characteristic of the converter is reduced. This reduction is compensated for by the turns ratio in the isolated transformer. In addition, the turns ratio of the transformer must also meet the output-voltage regulation for the minimum input voltage. These two design specifications result in high circulating energy in the converter.

Recently, resonant converters with three and four elements have been proposed to minimize the effect of the wide input-voltage and load-range variations in the performance of the converter [68], [69]. Among them, the LLC resonant converter has shown that not only can it reduce the

circulating energy under extreme operating conditions, but it can also minimize the switching losses in the converter [70]-[72].

This section proposes a three-level DC/DC resonant converter for high-voltage applications that improves the performance of traditional resonant converters by combining low-voltage-rating devices with the advantages offered by the three-element LLC resonant tank.

The proposed converter and its main waveforms are shown in Fig. 4-4. The primary side of the converter is based on a three-level structure in order to reduce the voltage stress across the primary devices. As mentioned before, this allows the use of low-voltage-rating devices, which present better electrical characteristics. In addition, an LLC resonant tank is placed in the primary side to provide zero-voltage operation for the primary switches. One of the advantages that the proposed converter offers over the traditional series resonant converter is that it can work above or below the resonant frequency determined by the series resonant tank formed by resonant inductance L_r and resonant capacitor C_r, and still achieves ZVS operation for the primary switches. The ZVS operation is achieved by using the stored energy in the magnetizing inductance of the transformer. This energy also allows the converter to operate with soft switching under a wide load range, without requiring an increase in either the quality factor Q of the resonant tank or the ratio between switching and resonant frequencies. Consequently, the circulating energy in the converter is also reduced.

For simplification in the explanation of the converter operation, it is considered that switches S_1 and S_2 or S_3 and S_4 are turned on and off simultaneously. However, it is required that a small delay be introduced into the operation between them. In this way, auxiliary diodes D_{c1} and D_{c2}

conduct, clamping the voltage across the primary switches to half the level of the input voltage. In this case, flying capacitor C_{ss} is required for ZVS operation of switches S_1 and S_4.

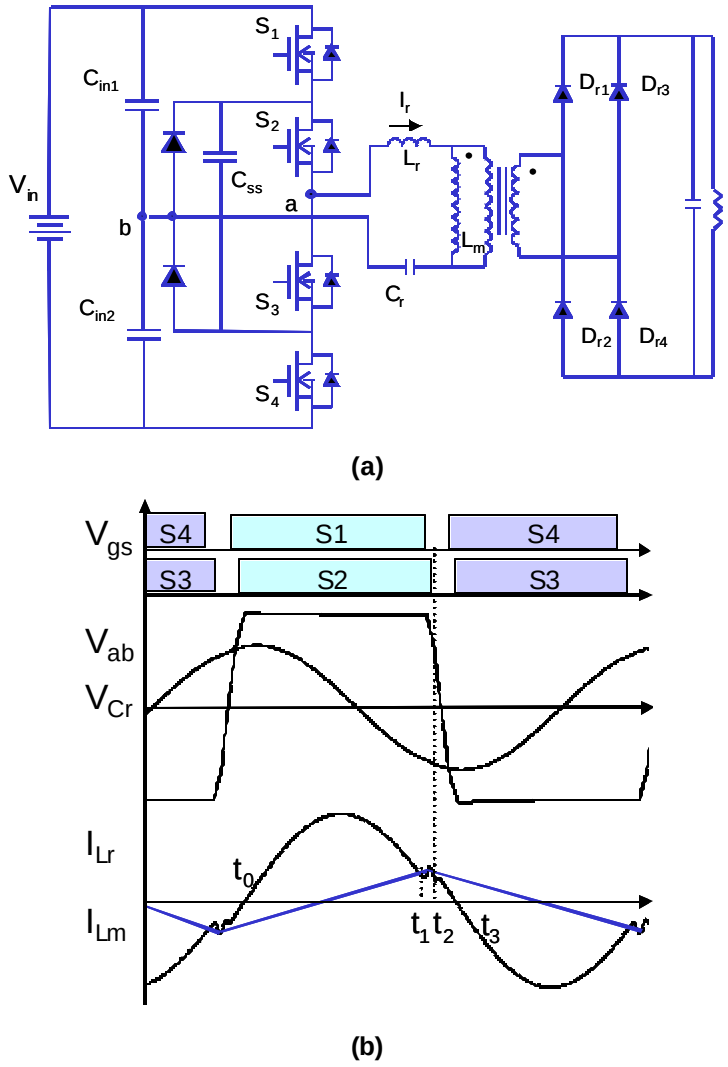


Fig. 4-4. (a) Proposed ZVS three-level LLC resonant DC/DC converter and (b) its main waveforms.

4.3.1. Modes of operation for the proposed converter

This section of the dissertation details the modes of operation for the proposed converter. Depending on the operating conditions, this converter has two modes of operation. Each operating mode consists of three stages during each half of a switching cycle. The first one

occurs when the converter operates with a switching frequency higher than the resonant frequency determined by the resonant elements L_r and C_r. In this case, the natural resonant period of the tank is interrupted. This operating mode is similar to that of the series resonant converter.

The second mode of operation occurs when the switching frequency is smaller than the resonant frequency. This section will just address this operating mode, since the converter's operation in this mode presents several advantages, as will be discussed later.

The equivalent circuit for each stage of this operating mode is shown in Fig. 4-5. These stages are described below.

[t_0–t_1]: Before this stage begins, switches S_1 and S_2 are on, and the resonant inductor current flows through their anti-parallel diodes. At t_0, the primary current reverses direction, and the difference between half the input voltage and the reflected output voltage is applied across the resonant tank. Therefore, a resonance begins between series resonant capacitor C_r and series resonant inductor L_r. During this stage, the input power is delivered to the output.

[t_1-t_2]: At t_1, the resonant inductor current reaches the magnetizing current, causing the secondary side of the transformer to be disconnected from the primary side. During this time, a new resonance is carried out between magnetizing inductance L_m, resonant inductance L_r and resonant capacitor C_r.

[t_2-t_3]: At t_2, primary switches S_1 and S_2 are turned off just with the magnetizing inductance, which reduces the turn-off losses. Also, this magnetizing inductance discharges the parasitic capacitance of S_3 and S_4 to zero to turn on their anti-parallel diode, applying a negative voltage

across the transformer. Since the anti-parallel diodes of S_3 and S_4 conduct the primary current, S_3 and S_4 can be turned on with ZVS. During this stage, the secondary side remains disconnected from the primary side of the converter. In addition, the resonance continues between L_r, L_m and C_r. At the end of this stage, the primary current reverses, thus beginning a new half of a switching cycle.

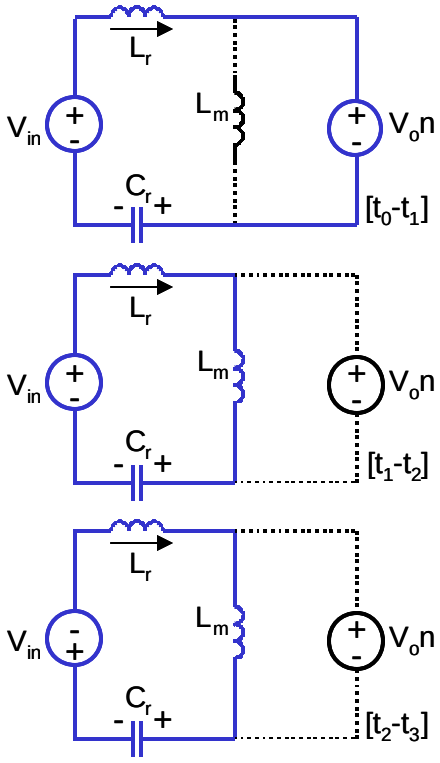


Fig. 4-5. Operating mode II: equivalent circuits for each stage.

4.3.2. Main Characteristics for the Proposed Converter

Figs. 4-6, 4-7, 4-8 and 4-9 illustrate the important steady-state characteristics and soft-switching operation regions for the converter. Fig. 4-6 shows the normalized DC gain of the converter for different Q factors, using the normalized frequency as a running parameter. For these curves, a ratio of 0.25 between inductances L_r/L_m was used.

As can be seen, the converter has the ability to boost the input voltage when it operates with low Q factors and below the normalized resonant frequency. The operation with low Q factors is one of the main advantages for this converter, since it allows reduction of the circulating energy. For this operating mode, ZVS operation is achieved using the energy in the magnetizing inductance. However, it is important to mention that the ZVS characteristic can be lost if the converter operates near the second resonant frequency, which is determined by L_r, L_m and C_r. In this case, the magnetizing current reverses its polarity before the turn-off of the switch. As a result, the converter will operate with ZCS instead of ZVS.

In this group of figures, it is noticed that for a proper selection of the parameters and for adequate design, the converter shows a no-load dependence characteristic. This allows a better optimization of the converter, since small variations in the frequency are necessary for wide load variations.

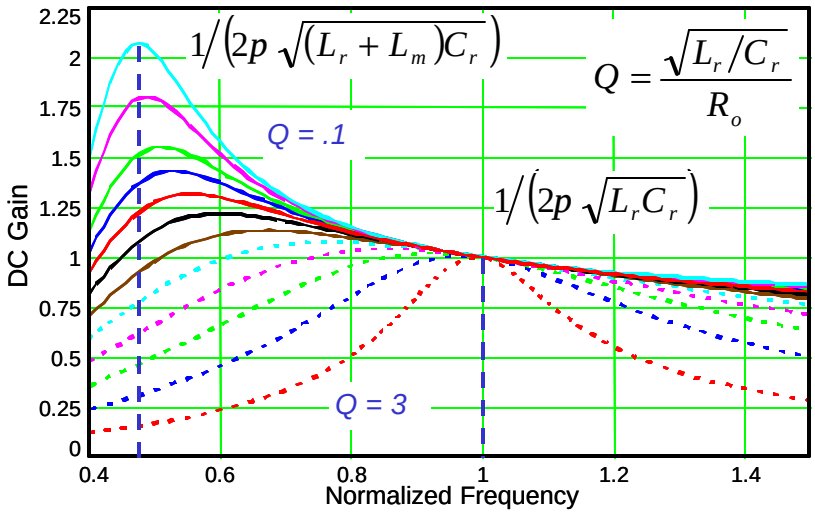


Fig. 4-6. Normalized DC gain characteristics versus normalized frequency for different Q factors.

Fig. 4-7 shows the boundary between ZVS and ZCS operation regions. This boundary is determined by tracing a line joining the peak for all the curves. It is important to mention that the

relationship between the magnetizing and resonant inductances determines the ZVS operation limit.

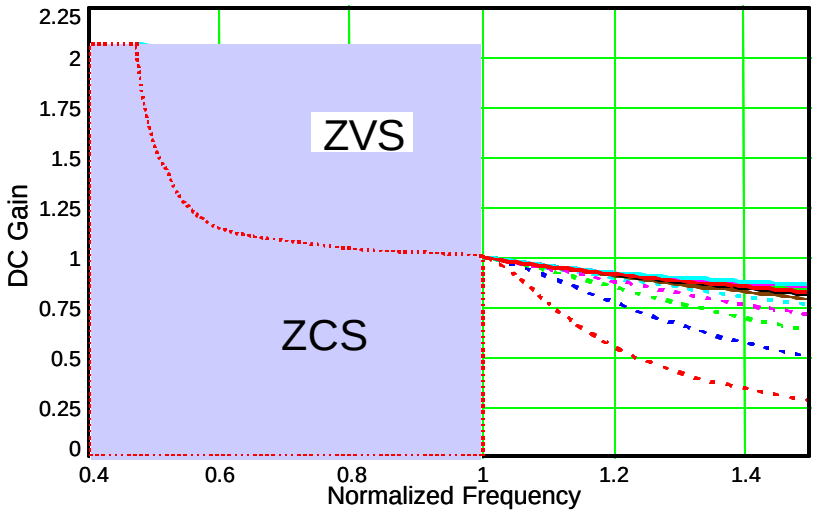


Fig. 4-7. Soft-switching operation regions for the proposed converter.

Fig. 4-8 shows the normalized voltage across the resonant capacitor C_r versus normalized frequency for different Q factors. As can be seen in this figure, another characteristic found when the converter operates close to the second resonant frequency is that the resonant capacitor is subjected to high voltage stress. In this operating region, the resonant inductance is also penalized with higher current stress, as shown in Fig. 4-9. This results in higher conduction losses for the primary devices. Therefore, it is recommended that the converter be operated around the resonant frequency, which is determined by the series resonant elements L_r and C_r.

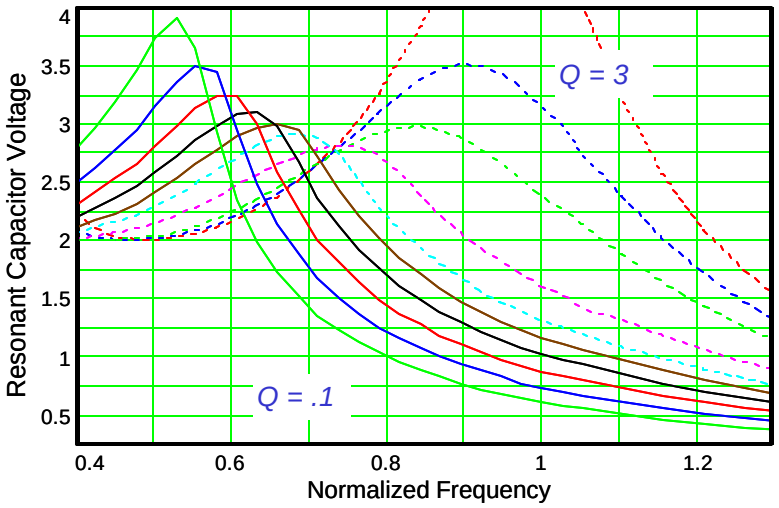


Fig. 4-8. Normalized capacitor voltage versus normalized frequency for different Q factors.

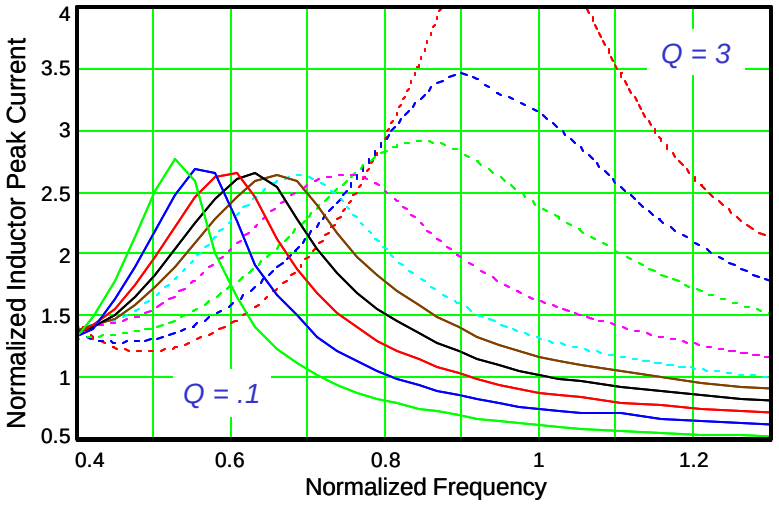


Fig. 4-9. Normalized inductor current versus normalized frequency for different Q factors.

4.4. Experimental Results

This section discusses the design and experimental results for the proposed converter. In order to illustrate the benefits of this converter, it was designed to meet wide input-voltage (600 V-800 V) and load-range variations (4.4 A-44.5 A at 60V output voltage).

4.4.1. Design of the Converter

Fig. 4-10 shows the normalized DC gain for the proposed converter. As explained before, these data were obtained from simulation. From this figure, it is possible to determine the operating trajectory for the proposed converter under input voltage and load conditions.

In order to meet the requirement of high-power density, the converter was first designed to operate at a switching frequency of 1 MHz. After completing a study that determined the optimum switching frequency for the LCT component [83] (integration of the passive components; i.e., inductor, capacitor and transformer), it was decided that the converter should operate at a maximum switching frequency of 745 kHz. Also, the converter was designed in such a way that at 800V input voltage, the converter operates close to the resonant frequency determined by L_r and C_r, thus minimizing the circulating energy at the nominal operating point. These considerations set the minimum operating frequency at 550 kHz for 600V input voltage.

Table 4-1 shows the principal parameters obtained from the design of the converter.

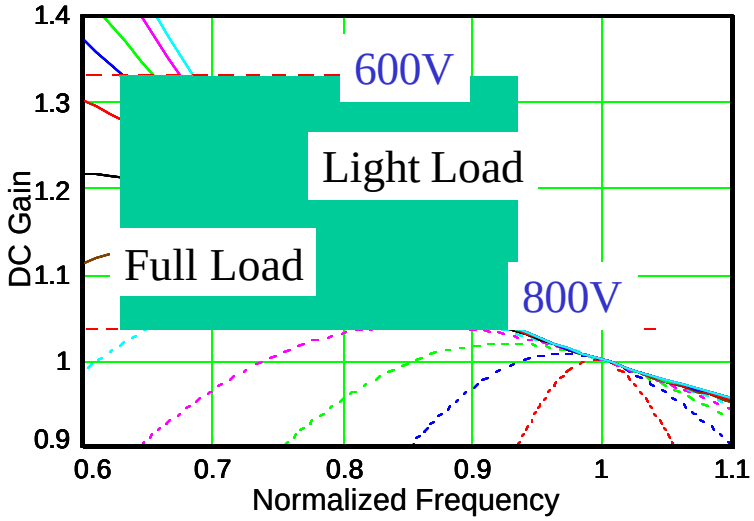


Fig. 4-10. Operating trajectory for the proposed ZVS three-level DC/DC resonant converter.

Table 4-1. Principal parameters obtained from the design of the ZVS three-level LLC resonant converter.

Q	F_n	F_s	N_p	N_s	L_r (μH)	C_r (nF)	L_m (μH)
.35	0.925	745 KHz	7	1	4.569	8.546	20

4.4.2. Implementation of the Converter

An experimental prototype was built to verify the operation of the proposed converter. The power stage shown in Fig. 4-4 is comprised of the following components.

S_1 - S_4: APT5015BLC

D_{r1} - D_{r4}: 30CPQ150

D_{c1} - D_{c2}: HFA15TB60

C_{in1} - C_{in2}: 2x330nf/400V polypropylene

C_{ss}: 470nF/400V- polypropylene

C_r: 8.36nf – 2x16.5nf/800V ceramic

T_r: E55 – 3F3 8/1

L_r: 4.948uH

L_{lk} – 2.788uH

L_r - 2.16uH 6 turns 783E – 3F3

Considering a frequency operating range of 550 - 745 KHz, and taking into account the eventual integration of the passive elements in the converter (the transformer, resonant capacitor and resonant inductor) into an LCT structure, it was decided that too much effort was required for the construction of a planar transformer. Therefore, a normal E55 core was used. In this case, Litz wire was used for the primary and secondary windings, and they were placed side by side in order to reduce the interwinding capacitance of the transformer. It is important to mention that this format causes the leakage inductance of the transformer to increase to 2.78 μH. However, this leakage inductance is absorbed by the resonant inductance. In addition, a small gap was introduced in order to adjust the magnetizing inductance of the transformer to the calculated value (20 μH).

4.4.3. Experimental Results

Experimental results for the proposed ZVS three-level LLC resonant DC/DC converter are shown in Fig. 4-11,Fig. 4-12 andFig. 4-13. Fig. 4-11 shows the voltage across the resonant tank (V_{ab}) and the primary resonant current. These waveforms were taken at 800V input voltage, 60V output voltage and 42.55A output current. The switching frequency for this operating condition is 745 kHz. As can be seen, by operating the converter below the resonant frequency, the primary current completes the entire resonant period, which reduces the switching losses in the primary devices.

Fig. 4-12 shows again the voltage across the resonant tank and the primary resonant current during hold-up time. In order to regulate the output voltage for this operating condition, the switching frequency is set to 550 kHz.

Fig. 4-13 shows the resonant current at different load conditions and at nominal input voltage. As can be seen, using an LLC resonant tank not only guarantees ZVS operation for any load condition, but also minimizes the circulating energy in the converter.

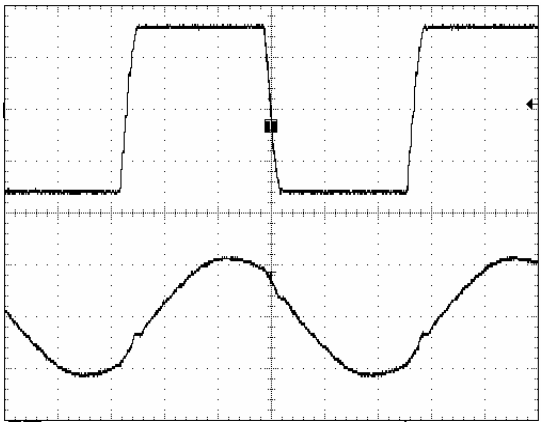


Fig. 4-11. Results at nominal input voltage: voltage across the resonant tank (V_{ab}) and primary resonant current (250V/div, 10 A/div, 250ns/div).

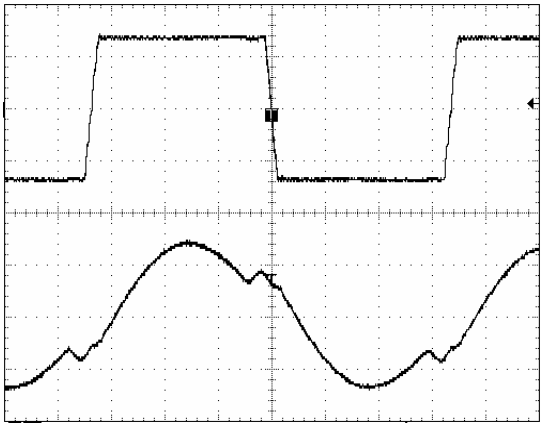


Fig. 4-12 Results during hold-up time: voltage across the resonant tank (V_{ab}) and primary resonant current (250V/div, 10 A/div, 250ns/div).

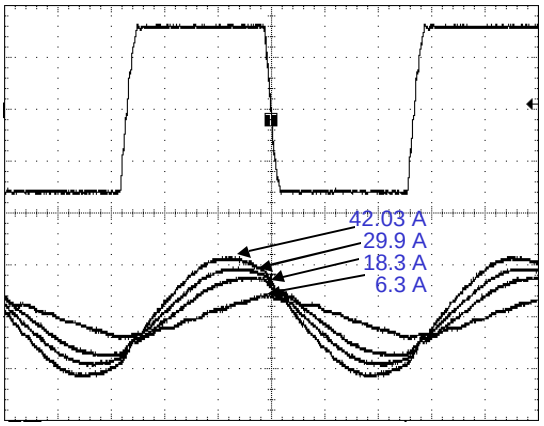


Fig. 4-13. Results for different load conditions and at nominal input voltage: voltage across the resonant tank (V_{ab}) and primary resonant current (250V/div, 10 A/div, 250ns/div).

The experimental efficiency as a function of the output power at nominal input voltage 800 V is shown in Fig. 4-14. The efficiency at full-load condition is 94.5%, and the maximum efficiency of the converter, which occurs at 1,750 W, is 95.2%. Fig. 4-15 shows the measured efficiency of the converter as a function of the input voltage at full-load condition. It can be seen that the efficiency decreases as the input voltage decreases. As was explained before, the characteristics presented by this converter allow the optimization at the nominal input-voltage condition. When the input voltage decreases, the converter operates close to the second resonant tank to compensate for this variation. In this region, the circulating energy is higher, resulting in higher conduction losses. It is important to mention that this reduction of the input voltage occurs

only during hold-up time, loss of the mains; therefore, this does not represent a thermal issue for the converter.

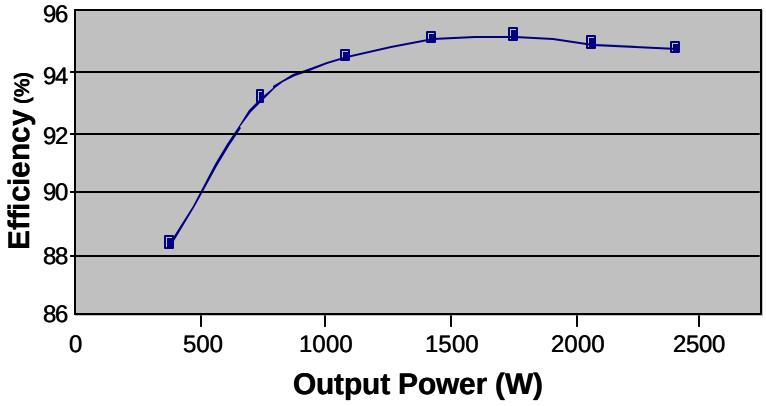


Fig. 4-14. Efficiency for the proposed converters at nominal input voltage.

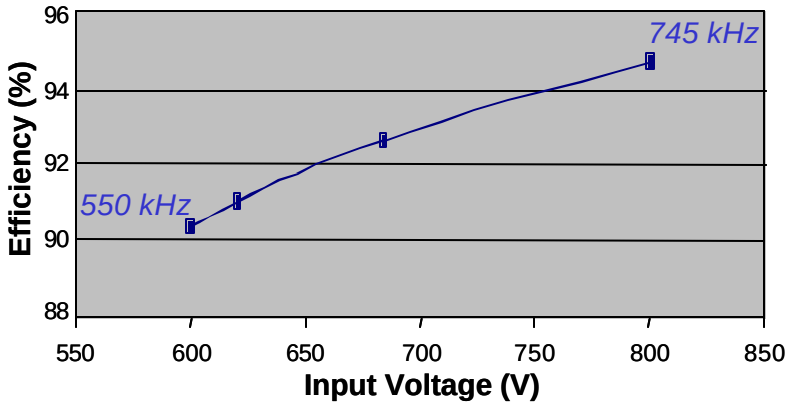


Fig. 4-15. Efficiency for the proposed converter at nominal output power and using the input voltage as a running parameter.

This section of the dissertation proposed a novel ZVS three-level LLC resonant DC/DC converter for high-power applications. Among the main characteristics offered by the converter is the reduction of the voltage stress across the main devices by using a three-level structure, its wide ZVS range, its minimal turn-off losses for primary devices, and its minimal circulating energy under wide input-voltage variations. As was shown, these characteristics make the proposed converter an interesting option for high-voltage, high-power applications that require high power density.

Knowledge of these characteristics was obtained by operating the converter with a variable switching frequency. In some military applications, it is desirable to maintain these characteristics with the restriction of fixed-frequency operation. To meet this requirement, the following sections evaluate the performance of the ZVS LLC three-level resonant converter under fixed-frequency operation. In addition, the next section presents the analysis, design of and comparison with, the traditional clamped-mode series resonant DC/DC converter in order to highlight the main advantages of the proposed converter under fixed-frequency operation.

4.5. Clamped-Mode ZVS Three-Level DC/DC Resonant Converter

This section of the dissertation analyses and evaluates different modulation strategies to improve the ZVS characteristics of the traditional clamped-mode series resonant DC/DC converter. The ZVS three-level DC/DC series resonant converter is shown in Fig. 4-16. As a first approach for the analysis, an evaluation is made of the different modulation strategies proposed for this resonant converter. The purpose is to determine which strategy achieves the best performance from the standpoint of the least conduction and turn-off losses. The analysis of the converter is done with the usual assumption that filtering provided by the resonant tank permits all high-frequency harmonics to be ignored [67]. Consequently, only the first (fundamental) harmonic of the tank current is considered in the analysis. This method provides an accurate model of the converter when it operates at frequencies close to the resonant frequency of the tank, as is the case assumed here.

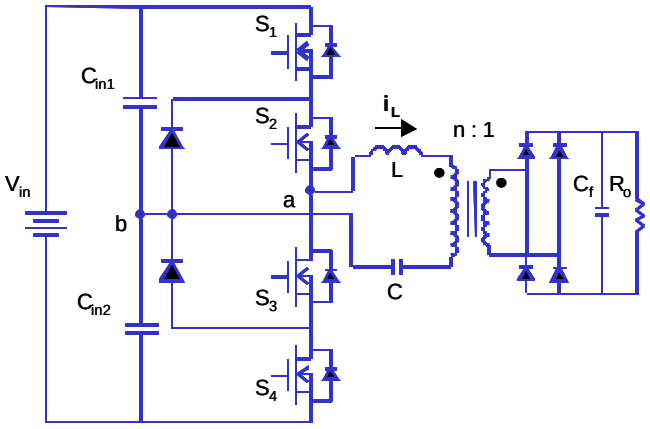


Fig. 4-16. The three-level DC/DC series resonant converter.

For the converter in Fig. 4-16, the Q factor is defined as [67]:

$$Q = \frac{Z_0}{R_{eq}}, \tag{4-1}$$

where the characteristic impedance Z_0 and the equivalent resistance R_{eq} are respectively

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4-2}$$

and

$$R_{eq} = \frac{8}{p^2} n^2 R_0. \tag{4-3}$$

The normalized switching frequency is defined as

$$w_n = \frac{w_s}{w_0}, \tag{4-4}$$

where w_s is the angular switching frequency, and w_0 is the angular resonant frequency

$$w_0 = \frac{1}{\sqrt{LC}}. \tag{4-5}$$

The previously proposed fixed-frequency control techniques [61]-[66] have different names, but they can be divided into three different strategies.

a) The traditional phase-shift or clamped-mode (CM) control [61],[62], [73]-[77].

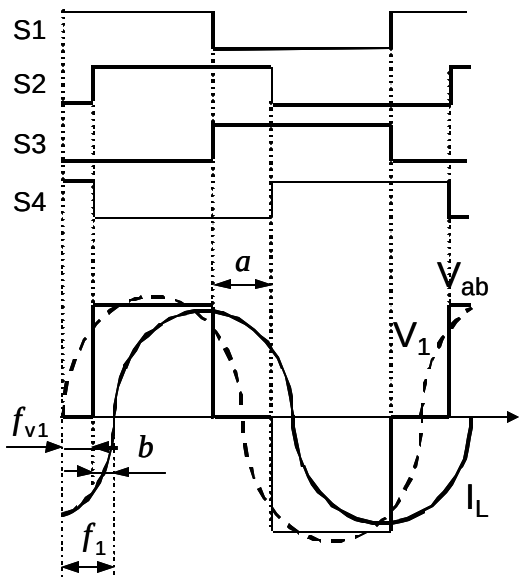
b) The asymmetrical PWM or asymmetrical-duty-cycle (ADC) control [63], [64]. This technique has been proposed for different kinds of converters by several authors. In this case, the voltage is not clamped to zero, and it can also be used in half-bridge converters.

c) The unipolar voltage cancellation or asymmetrical-clamped-mode (ACM) control [65],[66]. In this strategy, originally proposed for resonant inverters, the voltage is only clamped to zero on one size, and is thus asymmetrical.

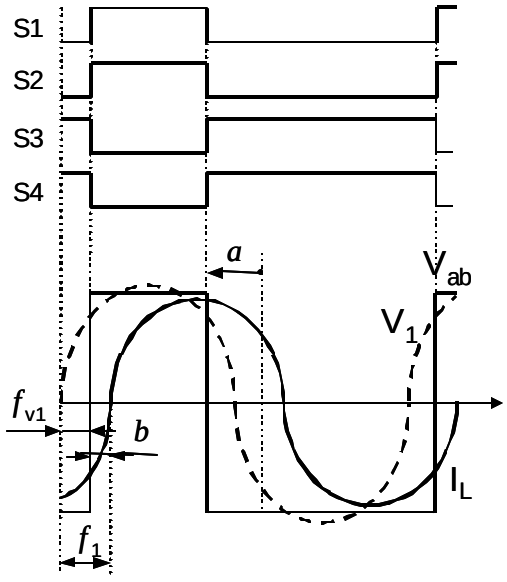
Fig. 4-17 shows some typical waveforms for the three fixed-control strategies. The sequence of conduction for switches S_1 –S_4, the quasi-square voltage V_{ab} applied to the resonant tank, and the primary current i_L through the resonant tank (this current is assumed to be practically sinusoidal, as stated before) are presented in this figure. The dotted waveform V_{ab1} is the first harmonic of V_{ab}. For each control strategy, the control angle is a.

Taking into account the previous expressions, in any case the phase lag f_1 between the voltage V_{ab1} and the current i_L through the resonant tank can be obtained as

$$f_1 = \tan^{-1} \frac{(w_n^2 - 1)\, Q}{w_n}. \qquad (4\text{-}6)$$



(a)



(b)

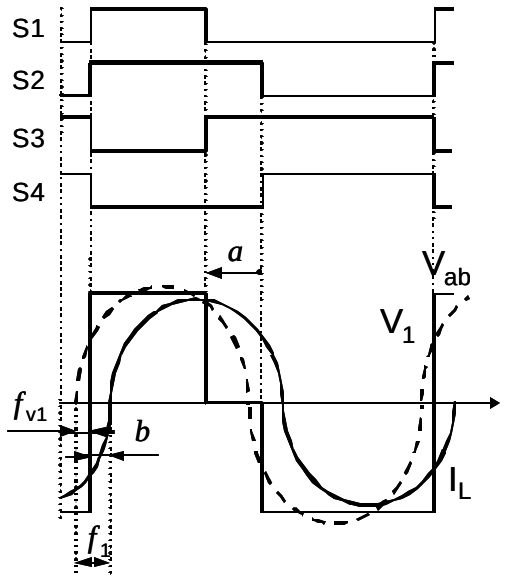


Fig. 4-17. Typical waveforms for fixed-frequency control strategies: (a) CM control, (b) ADC control, and (c) ACM control.

The amplitude and phase of voltage V_{ab1} are denoted as $\hat{V}_{ab1}$ and f_{v1}, respectively. The calculation of both variables depends on the control strategy, and these are defined as follows.

A. CM Control

The amplitude and phase of the voltage v_{ab1} are respectively (see Fig. 4-17(a))

$$\hat{V}_{ab1} = \frac{4V_i}{p}\cos\frac{a}{2} \tag{4-7}$$

and

$$f_{v1} = \frac{a}{2}, \tag{4-8}$$

where V_i is the DC input voltage.

B. ADC Control

The amplitude and phase of the voltage v_{ab1} are respectively (see Fig. 4-17(b))

$$\hat{V}_{ab1} = \frac{4\,V_i}{p}\cos\frac{a}{2} \tag{4-9}$$

and

$$f_{v1} = \frac{a}{2}. \tag{4-10}$$

Equations (4-9) and (4-10) are the same as (4-7) and (4-8), respectively. This is true for the first-harmonic expressions, but not for the rest of the harmonics in general.

C. ACM Control

The amplitude and phase of the voltage v_{ab1} are respectively (see Fig. 4-17(c))

$$\hat{V}_{ab1} = \frac{V_i}{p}\sqrt{10 + 6\cos a} \tag{4-11}$$

and

$$f_{v1} = \tan^{-1}\frac{\sin a}{3 + \cos a}. \tag{4-12}$$

For any control strategy, if V_0 is the averaged DC output voltage, I_0 is the averaged output current, and $\hat{I}_L$ is the amplitude of the inductor current, the expression for the transferred power is

$$V_0\,I_0 = \frac{1}{2}\hat{V}_{ab1}\,\hat{I}_L\cos f_1, \tag{4-13}$$

and consequently the output voltage V_0 can be obtained as

$$V_0 = \frac{1}{2}\hat{V}_{ab1}\frac{\hat{I}_L}{I_0}\cos f_1 = \frac{p}{4n}\hat{V}_{ab1}\cos f_1 = \frac{p}{4n}\frac{\hat{V}_{ab1}}{\sqrt{1+Q^2\left(w_n - \frac{1}{w_n}\right)^2}}, \tag{4-14}$$

taking into account (4-6) and

$$\frac{\hat{I}_L}{I_0} = \frac{p}{2n}. \tag{4-15}$$

For ZVS operation of the active devices, the angle b in the waveforms of Fig. 4-17 must always be greater than zero, in order to assure that there is enough energy in the inductor L to charge or discharge the corresponding parasitic output capacitance of the MOSFET [75], [76]. From the waveforms in Fig. 4-17,

$$b = f_1 - f_{v1}. \tag{4-16}$$

So the condition for a ZVS operation is

$$b > 0 \quad \Rightarrow \quad f_1 - f_{v1} > 0. \tag{4-17}$$

The value of b needed to guarantee ZVS operation for the switches actually depends on the values of the parasitic output capacitors of the devices [76]. In order to compare the control strategies, this work considers the minimum requirements to achieve ZVS as expressed in (4-17).

In order to satisfy the ZVS condition, f_1 can be increased, as is done in traditional approaches, by increasing the switching frequency (see (4-6)). At the same time, there will be greater conduction and turn-off losses, since the current should be increased in order to transfer the same

power, and the switching frequency is also higher. As a result, if the losses are supposed to be minimized, the converter should be operated at the minimum switching frequency above the resonant frequency, with $b > 0$ in order to maintain ZVS.

Another approach to satisfy (4-17) is to reduce f_{v1}, which is a function of the control angle a for each control strategy, according to (4-8), (4-10) or (4-12). As can be seen, (4-8) and (4-10) are the same, but (4-12) is different. So not all the control strategies have the same ability to maintain ZVS operation for the devices.

Substituting (4-6), (4-8), (4-10), and (4-12) into the condition (4-17) produces

$$\frac{w_n^2 - 1}{w_n} > \frac{\tan\frac{a}{2}}{Q} \tag{4-18}$$

for CM and ADC controls, and

$$\frac{w_n^2 - 1}{w_n} > \frac{\frac{\sin a}{3 + \cos a}}{Q} \tag{4-19}$$

for ACM control.

Fig. 4-18 shows a comparison between the control strategies. For each of the three strategies in Fig. 4-18 the minimum normalized switching frequency w_n required for ZVS (that is, with $b = 0$) is shown as a function of the control angle a and the Q factor. As pointed out in (4-1), the Q factor represents the load variations: The larger the Q, the larger the load I_0, assuming L and C are constant.

As shown in Fig. 4-18, ACM control requires a lower switching frequency to attain ZVS for each Q and a. That means that the total losses in the devices will be lower in every operating condition.

A usual specification is to maintain a constant level of output voltage, considering input-voltage and load variations. According to (4-14), this means that $\hat{V}_{ab1}\cos f_1$ must be constant. If $V_{i\min}$ is the minimum input voltage, corresponding to the minimum control angle a = 0, and assuming b = 0 (that is, $f_1 = f_{v1}$), then for any control strategy

$$\hat{V}_{ab1}\cos f_{v1} = \frac{4V_{i\min}}{p} \quad \Rightarrow \quad \hat{V}_{ab1} = \frac{4V_{i\min}}{p\,\cos f_{v1}}. \tag{4-20}$$

Substituting (4-7)-(4-12) into (4-20) produces

$$\frac{V_i}{V_{i\min}} = \frac{1}{\cos^2\frac{a}{2}} \tag{4-21}$$

for CM and ADC controls, and

$$\frac{V_i}{V_{i\min}} = \frac{4}{\sqrt{10+6\cos a}\,\cos\tan^{-1}\frac{\sin a}{3+\cos a}} \tag{4-22}$$

for ACM control.

The normalized input voltage V_{in} is defined as

$$V_{in} = \frac{V_i}{V_{i\min}}, \tag{4-23}$$

Equations (4-21) and (4-22) allow a to be obtained as a function of the normalized input voltage, as represented in Fig. 4-19, in order to be substituted into (4-18) and (4-19). In this way, Fig. 4-20 shows a second comparison between the control strategies. In this case, the minimum normalized switching frequency w_n required for ZVS (that is, with b = 0) is represented as a function of the normalized input voltage V_{in} (from 100 to 200%) and the Q factor.

As shown in Fig. 4-19, the maximum variation of the input voltage in ACM control is restricted to around 100% of the minimum input voltage, which is lower than in CM and ADC controls. However, it can be seen again in Fig. 4-20 that ACM control requires a lower switching frequency to achieve ZVS for each Q and V_{in}, which means the total losses in the devices should be lower.

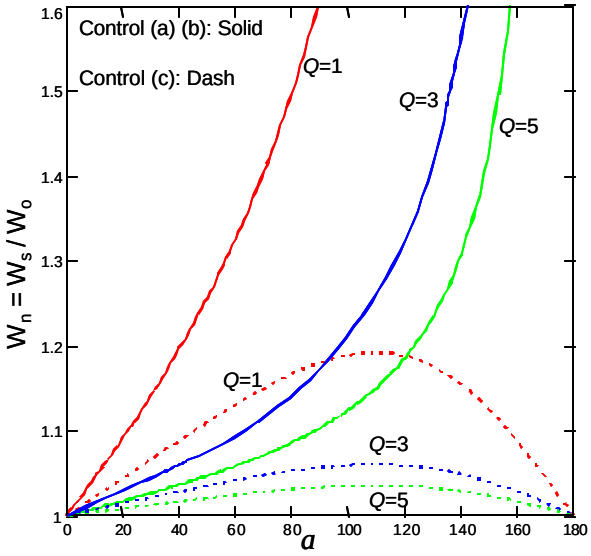


Fig. 4-18. Minimum normalized switching frequency ? $_n$ required for ZVS (ß=0) as a function of (a) the control angle a and the Q factor. Solid lines (? $_{n1}$) represent CM and ADC controls, and dashed lines (? $_{n2}$) represent ACM control.

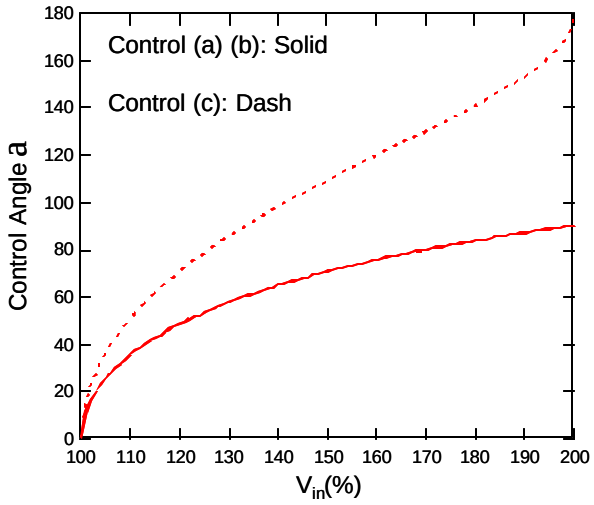


Fig. 4-19. Control angle a as a function of the normalized input voltage V_{in}. Solid lines (a_1) represent CM and ADC controls, and dashed lines (a_2) represent ACM control.

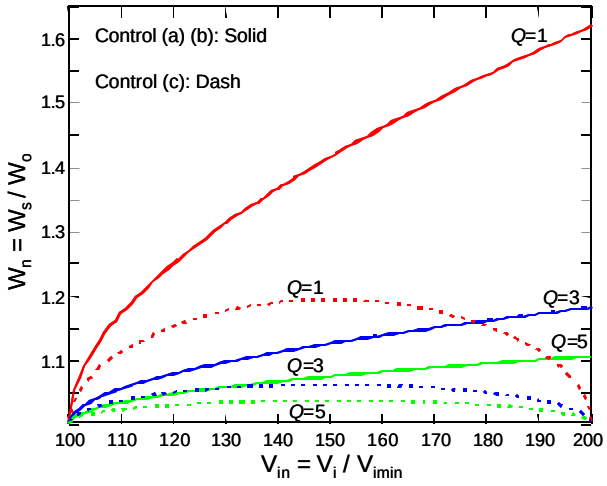


Fig. 4-20. Minimum normalized switching frequency $?_n$ required for ZVS (ß=0) as a function of the normalized input voltage V_{in} and the Q factor. Solid lines ($?_{n1}$) represent CM and ADC controls, and dashed lines ($?_{n2}$) represent ACM control.

From the previous comparison, it can be seen that the three-level series resonant DC/DC converter with ACM control could provide the best performance. In order to evaluate this converter, a 2.7kW prototype that meets wide input-voltage variations (600 V – 800 V) at 60V output voltage was designed: The design considers a wide-load-range operation; however, in order to not penalize the efficiency in the converter, ZVS for the primary devices is lost at 60% of the load. The main parameters from the design are listed in Table 4-2.

Table 4-2. Principal parameters obtained from the design of the ZVS series resonant converter with ACM control.

Q	F_n	F_s	N	L_r (µH)	C_r (nF)
3.5	1.5	750kHz	1.5	2.7	37

Fig. 4-21 shows the estimated efficiency for the proposed ZVS three-level series resonant converter with ACM. For this estimation, only the switching and conduction losses in the primary devices and the conduction losses in the secondary devices were taken in account. The devices used for this calculation are listed as follows. These devices meet their respective current and voltage requirements. Two different devices were selected as primary switches: Device A (500 V/ 58 A) presents better conduction characteristics, and device B presents better switching characteristics.

S_{1A}- S_{4A}: APT50M80B2FLC – 500V/58A D_7 - D_8: 63CPQ100 100V/63A

S_{1B} - S_{4B}: APT50M17BLC – 500V/30A

Despite the improvements in the ZVS characteristics presented by the ACM control and the design with limited ZVS range, it can be seen that the converter presents a low efficiency under all voltage ranges, as shown in Fig. 4-21. Furthermore, the worst efficiency characteristic occurs at nominal input voltage. It is important to mention that an increase in the ZVS range would penalize even more the efficiency in the converter. This result shows that the traditional clamped-mode series resonant converter even with an improved control strategy cannot be used in applications in which wide input-voltage and load-range variations are required.

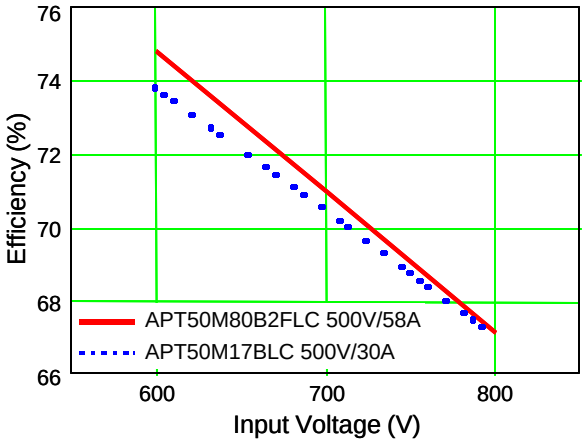


Fig. 4-21. Theoretical efficiency for the ZVS three-level DC/DC converter using ACM control.

4.6. Fixed-Frequency ZVS Three-Level LLC Resonant DC/DC Converter

The previous analysis shows that although improvements in the traditional resonant converter are achieved by modifying the modulation strategy to achieve ZVS operation under a wide load range, the converter is still penalized with low efficiency. Similar to the resonant converter operated at variable switching frequency, the resonant tank must also be designed with high quality factor Q, and the switching/resonant frequency ratio must be increased, both of which result in a reduction of the gain characteristic of the converter. This design specification also results in high circulating energy in the converter. The circulating-energy problem becomes even worse when the converter needs to meet specifications that include wide input-voltage variations.

One way to minimize the effect of the wide load condition in the performance of the converter is by using the magnetizing inductance of the transformer, as proposed for PWM converters [43]-[46]. However, in high-frequency operation it is not advisable to depend solely on the magnetizing inductance to achieve ZVS operation, since the duration of the ZVS process could greatly decrease the DC gain characteristic of the PWM converter [43].

Based on the ZVS three-level LLC resonant converter operated with variable frequency, this section proposes a resonant converter that can improve the efficiency by reducing the circulating energy. The basic idea is to maintain as much as possible the main characteristics of the converter, such as low circulating energy and wide ZVS range, while operating at fixed-frequency operation. In order to explore the characteristics presented for the proposed ZVS three-level LLC resonant converter with fixed-frequency operation, this section presents the circuit description, operating mode and characteristics. From these characteristics, design guidelines are given. Later, a possible solution is given for reducing the effect of the wide input-voltage variations in the performance of the converter.

4.6.1. Circuit Description

In this section, the operating principle of the fixed-frequency ZVS three-level LLC resonant converter is presented. The proposed converter and its main waveforms are shown in Fig. 4-22. In the primary side the structure remains the same, maintaining the main characteristic of variable-frequency operation. The use of an LLC series resonant tank allows the converter to operate above or below the resonant frequency determined by the series resonant tank, while still achieving ZVS for the primary switches. In addition, the ZVS operation occurs because of the stored energy in the magnetizing inductance of the transformer. This energy also allows the converter to operate with soft switching under a wide load range without the necessity for increasing either the quality factor Q of the resonant tank or the ratio between switching and resonant frequencies. Consequently, the circulating energy in the converter is also reduced.

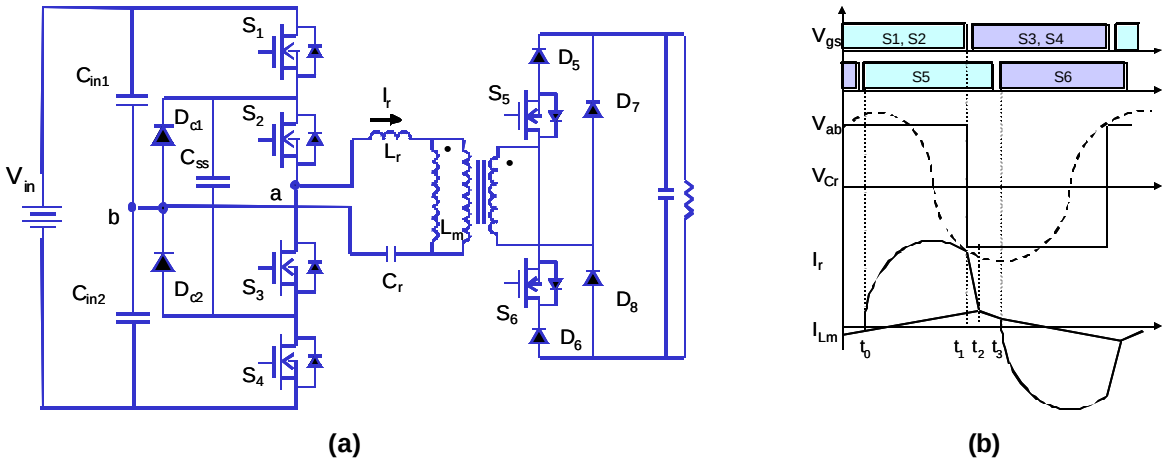


Fig. 4-22. (a) The proposed fixed-frequency ZVS three-level LLC resonant DC/DC converter and (b) its main waveforms.

In order to achieve fixed-frequency operation, switches S_5 and S_6 are placed in the secondary side of the converter. It is important to mention that by placing the devices in the secondary side, the converter operates with a wide ZVS range, thus avoiding the problems presented by the previously discussed clamp mode techniques.

The converter operates with phase-shift control in which all switches operate with duty cycles of nearly 50%. In the primary side, switches S_1 and S_2 are turned on and off simultaneously. Similarly, switches S_3 and S_4 are also operated simultaneously but with a 180° phase shift from S_1 and S_2. The phase shift of S_5 with respect to S_1 and S_2 or S_6 with respect to S_3 and S_4 determines the operating duty cycle of the converter.

For simplification in the explanation of the converter operation, it is considered that switches S_1 and S_2 or S_3 and S_4 are turned on and off simultaneously. However, it is required that a small delay be introduced into the operation between them. In this way, auxiliary diodes D_{c1} and D_{c2} conduct, clamping the voltage across the primary switches to half the level of input voltage. In this case, flying capacitor C_{ss} is required for ZVS operation of switches S_1 and S_4.

As explained in the next sections, the converter is designed in such a way that the current in the secondary side reaches zero before the turn-off of S_5 or S_6. This allows ZCS operation for these switches. In addition, the reverse-recovery problem of the diodes in the secondary side is minimized.

4.6.2. Modes of Operation and Main Characteristics for the Proposed Converter

This section of the dissertation details the main characteristics of the proposed converter. Depending on the operating conditions, this converter presents two modes of operation. Each operating mode has three stages during each half of a switching cycle.

A. Operating Mode I

The first mode of operation occurs when the time for half the resonant period is smaller than the duty cycle applied to the converter. The equivalent circuit for each stage of this operating mode and waveforms are shown in Figs. 4-23(a) and (b), respectively. These stages are described below.

[t_0–t_1]: Before this stage begins, switches S_1 and S_2 are on. At t_0, the secondary switch S_5 is turned on, and the difference between half the input voltage and the reflected output voltage is applied across the resonant tank. Therefore, a resonance starts between series resonant capacitor C_r and series resonant inductor L_r. During this stage, the input power is delivered to the output.

[t_1-t_2]: At t_1, the resonant inductor current reaches the magnetizing current, causing the secondary side of the transformer to be disconnected from the primary side. During this time, a new

resonance is carried out between magnetizing inductance L_m, resonant inductance L_r and resonant capacitor C_r.

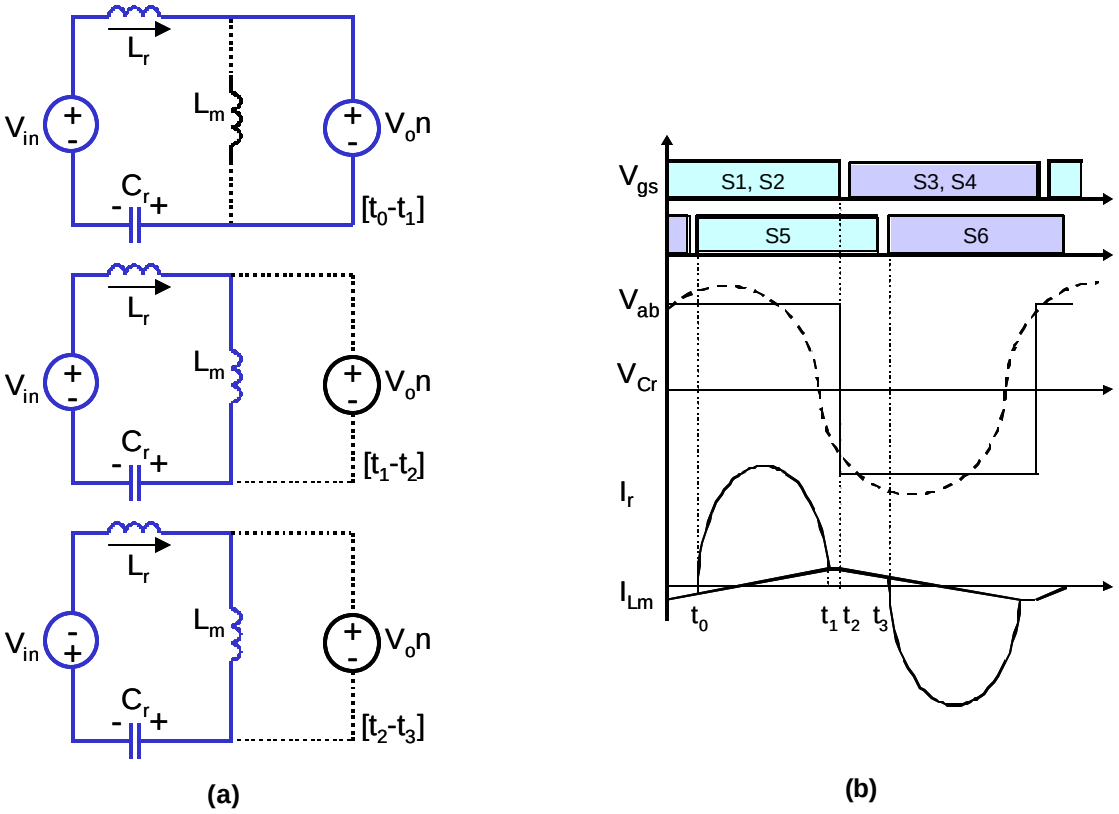


Fig. 4-23. Operating Mode I: (a) equivalent circuits for each stage and (b) its main waveforms.

[t_2-t_3]: At t_2, primary switches S_1 and S_2 are turned off and S_3 and S_4 are turned on, applying a negative voltage across the transformer. During this stage, the secondary side remains disconnected from the primary side of the converter. In addition, the resonance continues between L_r, L_m and C_r. At the end of this stage, the secondary switch S_5 is turned off under a zero-current condition, and S_6 is turned on, starting a new half of a switching cycle.

B. Operating Mode II

The second mode of operation occurs when the natural resonant period of the tank is interrupted; that is, when the duty cycle is smaller than half the resonant period. The equivalent

circuits for this mode and its main waveforms are shown in Figs. 4-24(a) and (b), respectively. A brief description of this mode is given below.

[t_0-t_1]: At t_0, the secondary switch S_5 is turned on. In the primary side, switches S_1 and S_2 are already on, so the difference between half the input voltage and the reflected output voltage is applied across the resonant tank. Therefore, a resonance starts between series resonant capacitor C_r and series resonant inductor L_r. During this stage, the input power is delivered to the output. This stage ends when switches S_1 and S_2 are turned off.

[t_1-t_2]: At t_1, switches S_3 and S_4 are turned on, changing the polarity of the input voltage. The resonance between L_r and C_r continues. This stage ends at t_2, when the primary current reaches the level of the magnetizing current.

[t_2-t_3]: During this stage, the secondary side of the transformer is disconnected from the primary side. In this way, a resonance is carried out between L_r, L_m and C_r.

At the end of this stage, the secondary switch S_5 is turned off with zero current, and S_6 is turned on, which starts a new half of a switching cycle.

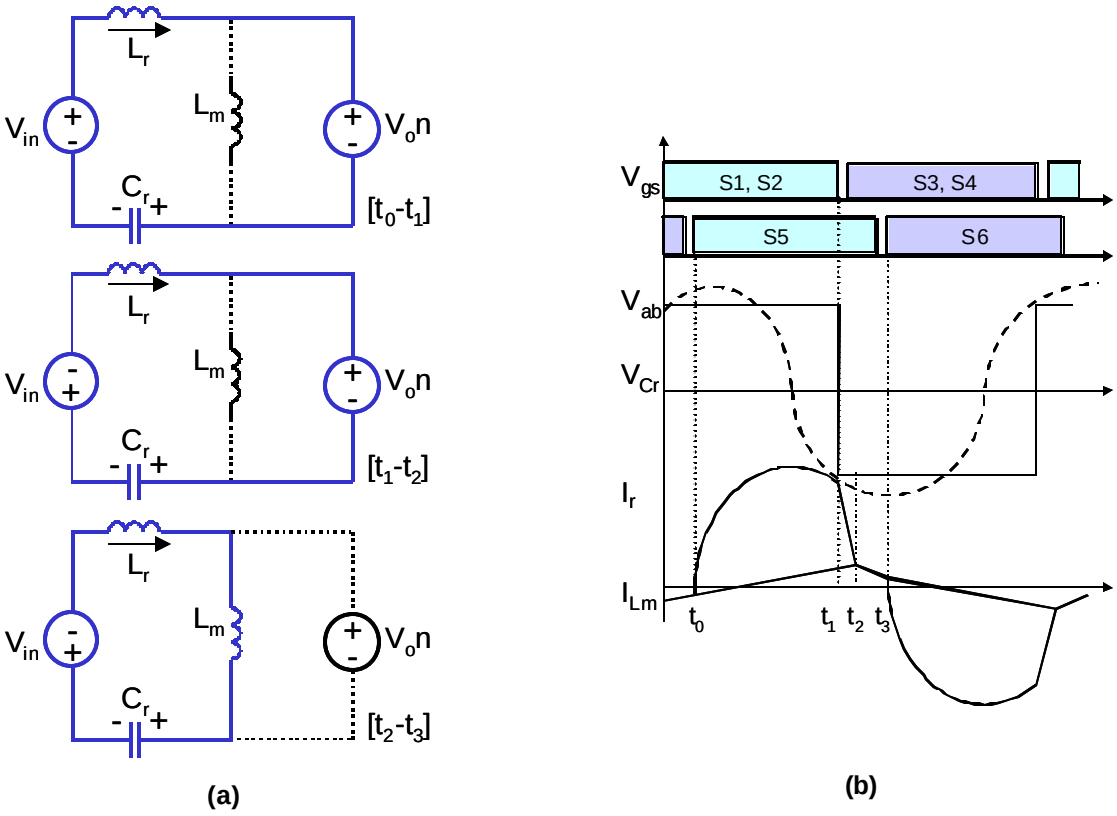


Fig. 4-24. Operating Mode II: (a) equivalent circuits for each stage and (b) its main waveforms.

C. Characteristics of the Proposed Converter

From the operating modes of the converter, one can see that the solution of the system depends on the initial conditions of the resonant inductor current and resonant capacitor voltage. As a result, it is difficult to obtain a closed-form solution for analyzing the converter. To obtain the steady-state operation, numerical methods can be used. A program implemented in Matlab was used to determine the main characteristics of the converter.

Figs. 4-25, 4-26 and 4-27 illustrate some steady-state characteristics of the converter. Fig. 4-25 shows the normalized DC gain of the converter at different normalized switching frequencies, using the duty cycle as a running parameter. It is important to mention that the solid line represents the DC gain obtained by using the program implemented in Matlab, and the dotted

lines represent the normalized DC gain obtained by simulation. There is close agreement between the calculated and simulated data.

Fig. 4-26 shows the normalized voltage across the resonant capacitor C_r for different normalized switching frequencies and using the duty cycle as a running parameter. Fig. 4-26 shows again the DC gain characteristic of the converter for different normalized switching frequencies, but now using the normalized load as a running parameter. Again, it can be seen that the simulated normalized gain (dotted line) is in accordance with the gain obtained with the Matlab program (solid line).

These graphs show that the converter maintains the main characteristics presented under variable-frequency operation: the capability to boost the input voltage when the converter operates below the normalized resonant frequency and it is designed with low Q factor, the no-load dependence, and the wide ZVS range that is achieved by using the energy in the magnetizing inductance. The last condition is always maintained if the converter operates with a normalized frequency higher than the second resonant frequency, which is determined by L_r, L_m and C_r. In addition, the operation near this point results in high-voltage stress for the resonant capacitor. Therefore, it is also recommended that the converter be operated around the resonant frequency, which is determined by the series resonant elements L_r and C_r.

The ZVS range presented for the proposed converter is an important characteristic when compared with the traditional series resonant converter with clamp mode control. As shown in the analysis presented in this chapter, the traditional series resonant converter should be designed with high Q factors and a high switching/resonant frequency ratio to maintain ZVS operation for low duty cycles.

It is important to mention that the relationship between the magnetizing and resonant inductances also determines the ZVS operation limit.

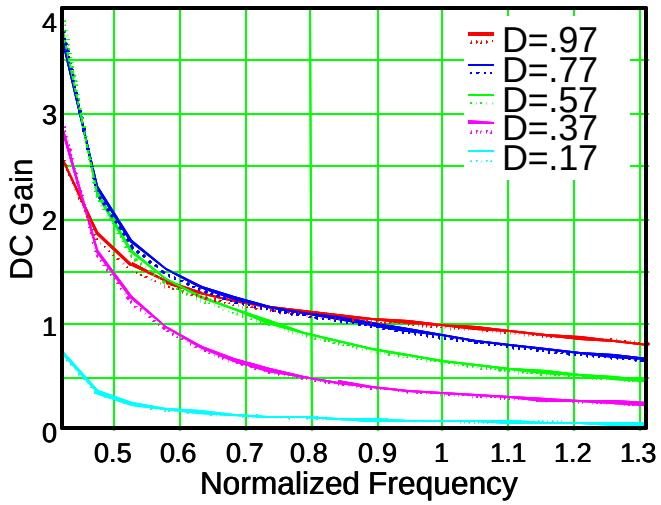


Fig. 4-25. Normalized DC gain characteristics versus normalized frequency, using the duty cycle as a running parameter.

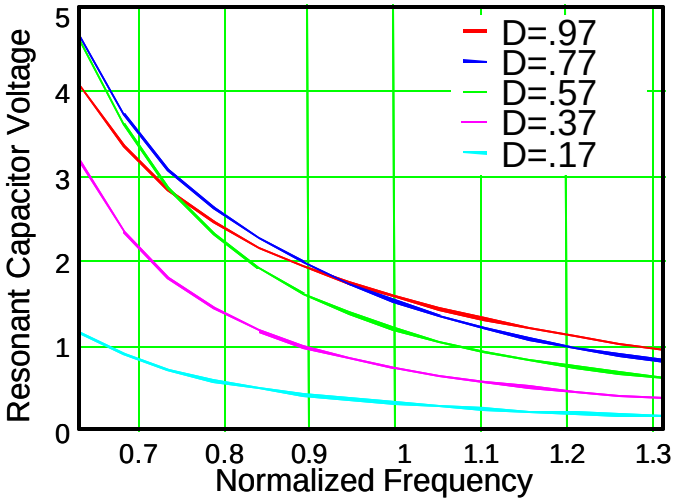


Fig. 4-26. Normalized resonant capacitor voltage versus normalized frequency, using the duty cycle as a running parameter.

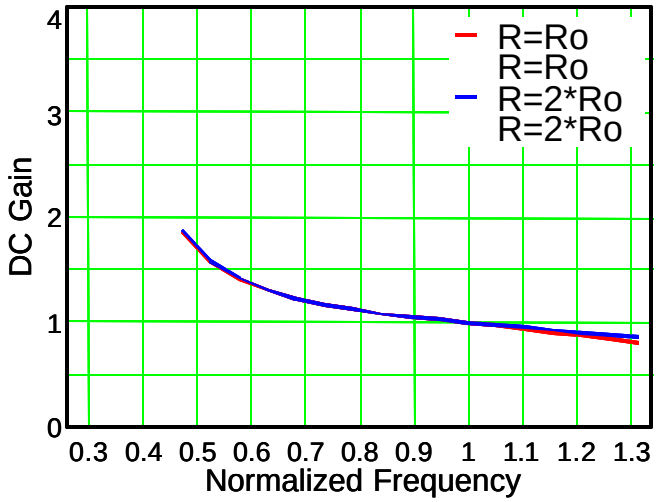


Fig. 4-27. Normalized DC gain characteristics versus normalized frequency using normalized load as a running parameter.

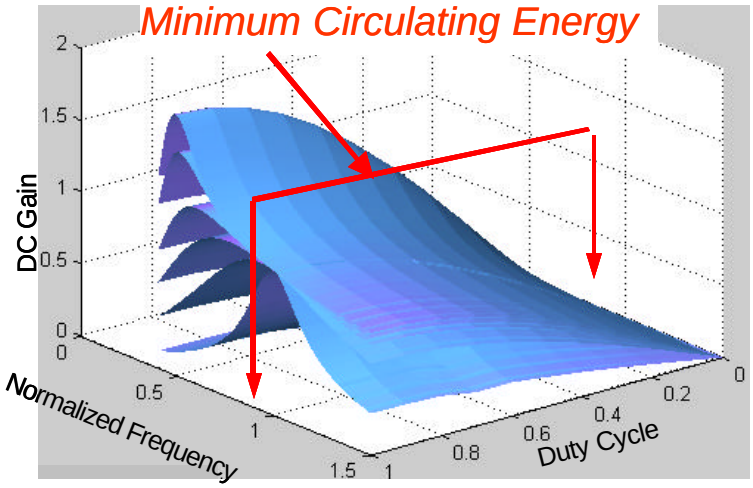
D. Evaluation of the Proposed Converter

Fig. 4-28(a) shows the DC gain characteristic of the converter using the switching frequency and the duty-cycle control as running parameters. Controlling the phase shift between the primary and secondary devices gives a second control variable for regulation of the output voltage. In this way, the selection of the switching frequency determines the maximum DC gain provided by the converter. As mentioned before, it is recommended that the switching frequency be selected to be close to the resonant frequency determined by series resonant elements L_r and C_r, which guarantees less circulating energy and stress in the resonant components for a low Q factor design. Fig. 4-28(b) shows the DC gain of the converter after selecting a switching and resonant frequencies ratio equal to 0.95. This graph is important for the selection of the turns ratio of the transformer.

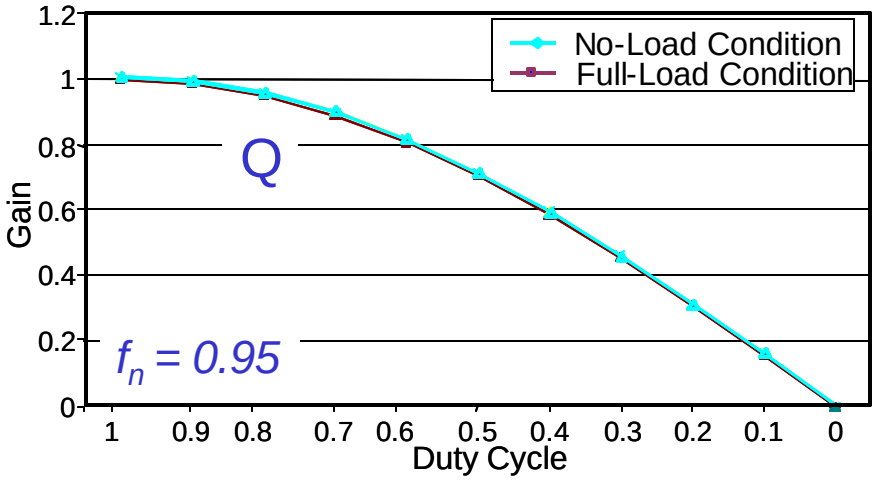
With the goal of evaluating the performance of the converter and determining the possibility that it could be used in applications in which high frequency operation with high efficiency is a

requirement, an attempt was made to design a 2.7kW converter that could meet the following specifications: V_{in} = 600 – 800 V and V_{out} = 60 V.

The converter was designed to achieve ZVS operation for the primary switches for up to 10% of the load. In addition, an operating switching frequency of 750 kHz is considered in the design of the converter in order to meet the specification regarding power density. Table 4-3 shows the principal parameters obtained from this design.



(a)



(b)

Fig. 4-28. DC gain for the ZVS three-level DC/DC resonant converter under (a) variable and fixed-frequency operation and (b) fixed-frequency.

Table 4-3. Parameters from the design of the three-level LLC resonant DC/DC converter with secondary control.

Q	F_n	F_s	N	L_r (µH)	C_r (nF)	L_m (µH)
.4	.95	750 kHz	4	1.74	23.36	18

Fig. 4-29 shows theoretical efficiency curves for the proposed converter. These efficiency curves were calculated considering only the switching and conduction losses for the primary devices and the conduction losses for the secondary devices. The devices considered for this calculation are listed as follows.

S_{1A}- S_{4A}: APT50M80B2FLC – 500V/58A D_7 - D_8: 63CPQ100 100V/63A

S_{1B} - S_{4B}: APT50M17BLC – 500V/30A D_5 - D_6: STTH3003CW

S_5 - S_6: APT20M18B2VR – 200V/ 70A

It is important to mention that these devices were chosen to meet the respective current and voltage stresses in the converter. Two different devices for the primary side were also considered in the efficiency calculation in order to evaluate the effects of the conduction and switching losses in the performance of the converter. Fig. 4-29(a) shows the theoretical efficiency curve of the converter at full-load condition using the input voltage as a running parameter. As can be seen, the proposed converter presents low efficiency at high-line input. At this operating condition, the switching losses of the converter are dominant, since the primary switches are turned off almost at the peak of the resonant current. At low-line input, the primary current is allowed to almost complete the entire resonant period, thus reducing the turn-off losses. This evolution of the current can be seen in Fig. 4-30. Fig. 4-29(b) shows the theoretical efficiency curve of the converter at nominal input voltage and using the load as a running

parameter. It can be seen that the device (B) presents less sensitivity to switching losses at low-load conditions.

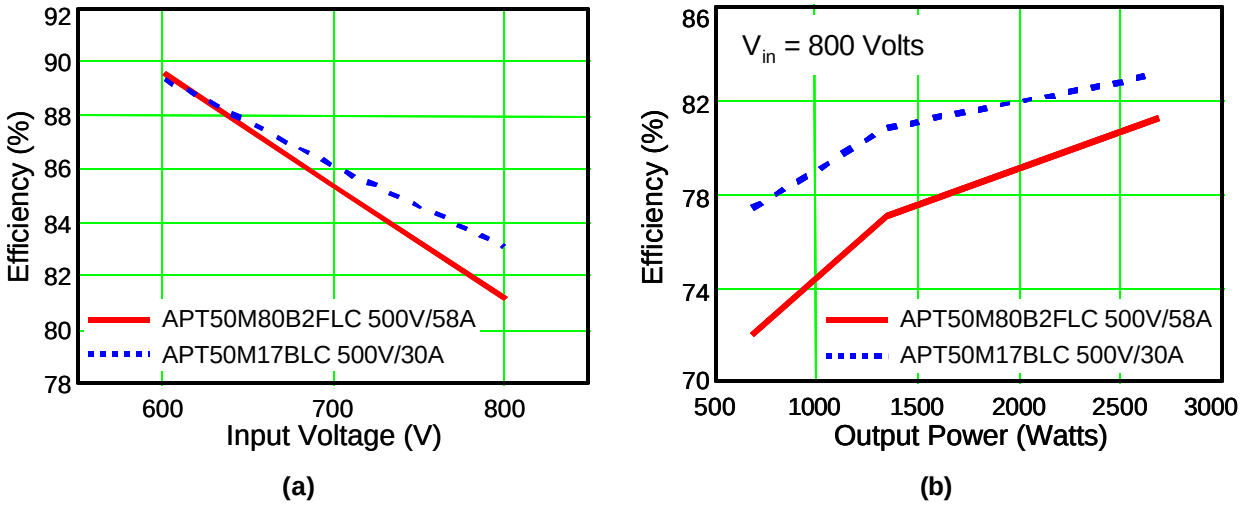


Fig. 4-29. Efficiency curves for the ZVS three-level DC/DC resonant converter with control in the secondary side. (a) Efficiency at full load, and using input voltage as a running parameter, and (b) efficiency at nominal input voltage and using load as a running parameter.

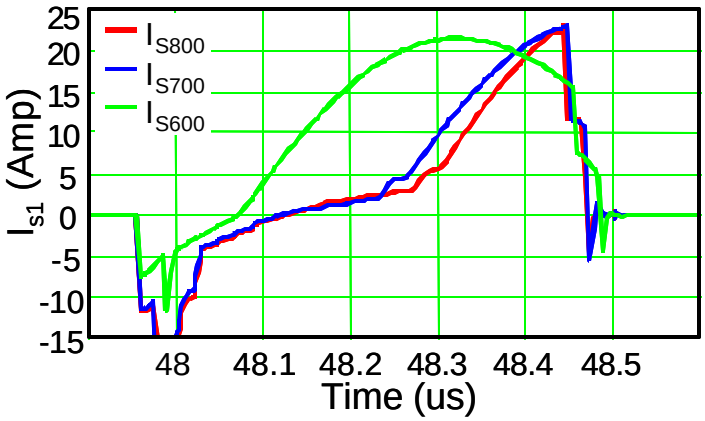


Fig. 4-30. Current through the switch S_1 at full load and different input-voltage conditions.

From these results, it can be seen that although improvements in the efficiency are achieved by designing the converter with low quality factor Q and a low switching/resonant frequency ratio, which results in a reduction of the circulating energy in the converter, the wide input-voltage variation is still an issue. The next section discusses improvements to this topology in order to reduce the effect of the wide input-voltage variation in the performance of the converter.

4.7. Solution For Wide Input-Voltage Variations

One of the problems associated with the resonant converters is their poor performance when they are subjected to wide input-voltage variations. In this kind of application, the input-voltage variation imposes both a reduction in the turns ratio of the transformer and wide variations in the duty cycle. Therefore, optimization of the converter is difficult to achieve, resulting not only in an incremental increase of the stresses in the power semiconductors and circulating energy in the converter, but also in a reduction in efficiency. A solution for reducing the output filter requirements for a PWM converter has been proposed [46]. A similar approach can be followed to reduce the duty-cycle variations for a wide input-voltage application.

Figs. 4-31 and 4-32 show this alternative approach, which would reduce the effect of the wide input-voltage variations on the performance of the converter. The basic idea with this approach is to add an additional winding in the secondary side of the transformer. Thus, the operation of the converter can be optimized by changing the turns ratio of the transformer according to the input voltage.

Fig. 4-31 shows this approach using full control in the secondary side. This idea can be implemented in a center-tapped or full-bridge structure, as shown in Figs. 4-31(a) and (b), respectively. As can be seen in Fig. 4-31(c), during a high-line condition, the converter regulates the output voltage by phase-shifting S_6 and S_7 with respect to the primary switches. Under low-line conditions, switches S_5 and S_8 carry out the regulation. By using this strategy, the secondary windings are connected in series to reduce the turns ratio of the transformer at low line. Therefore, a better optimization in the design of the converter can be achieved by reducing the variation in duty cycle.

Fig. 4-32 shows a simplified version of this approach, also using a center-tapped or full-bridge structure. In this approach, partial control of the output voltage is achieved by removing two of the secondary switches. Both secondary windings are always connected in series for any input-voltage condition. Adding more or less voltage to the main secondary controls the output voltage. Therefore, the turns ratio of the transformer must be designed in such a way that for high-line input voltage and no load, the converter is still able to regulate the output voltage. Due to this condition, the optimization of the converter is slightly more difficult to achieve than with the solution offered in Fig. 4-31.

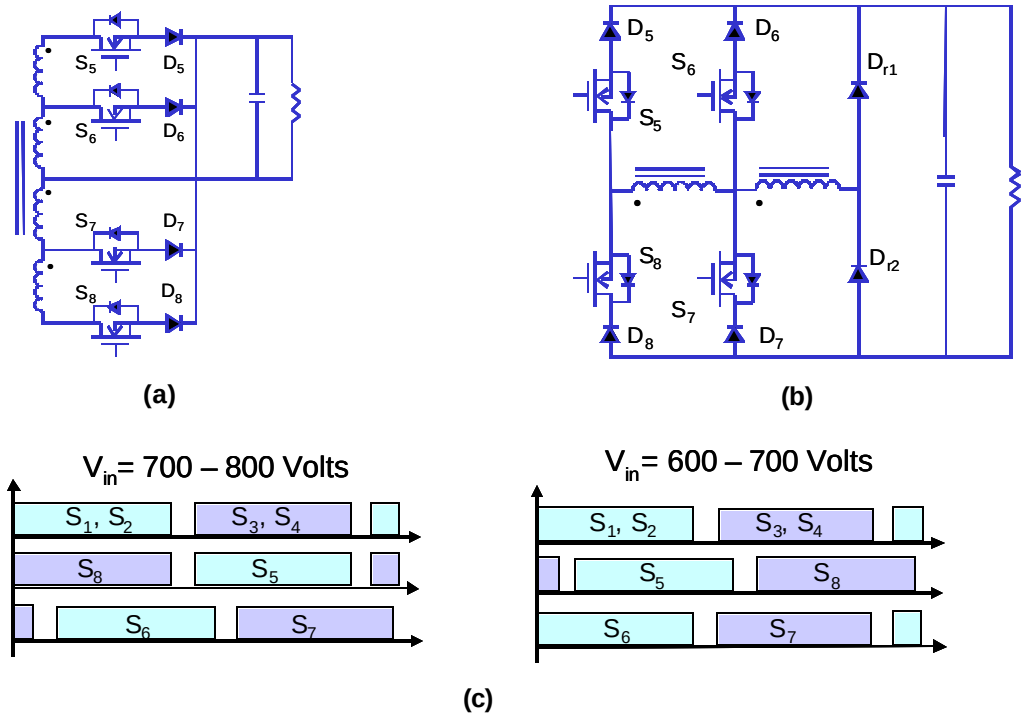


Fig. 4-31. Solutions for wide input-voltage variation: full control of the output voltage in: (a) a center-tapped configuration, (b) a full-bridge configuration, and (c) the control signals.

As can be seen in Figs. 4-31(b) and 4-32(b), using a full-bridge configuration in the secondary side enables a reduction in the complexity of constructing the transformer. However, this solution increases the conduction losses in the secondary side due to the addition of extra diodes

D_{r1} and D_{r2}. In order to have a better idea of which kind of secondary arrangement provides a better solution, it is necessary to perform an analysis using simulation tools such as Maxwell to predict the current distribution in the windings of the transformer.

Although improvements in the performance of the converter can be obtained by using the previous approaches, there is a tradeoff between simplification and optimization of the converter.

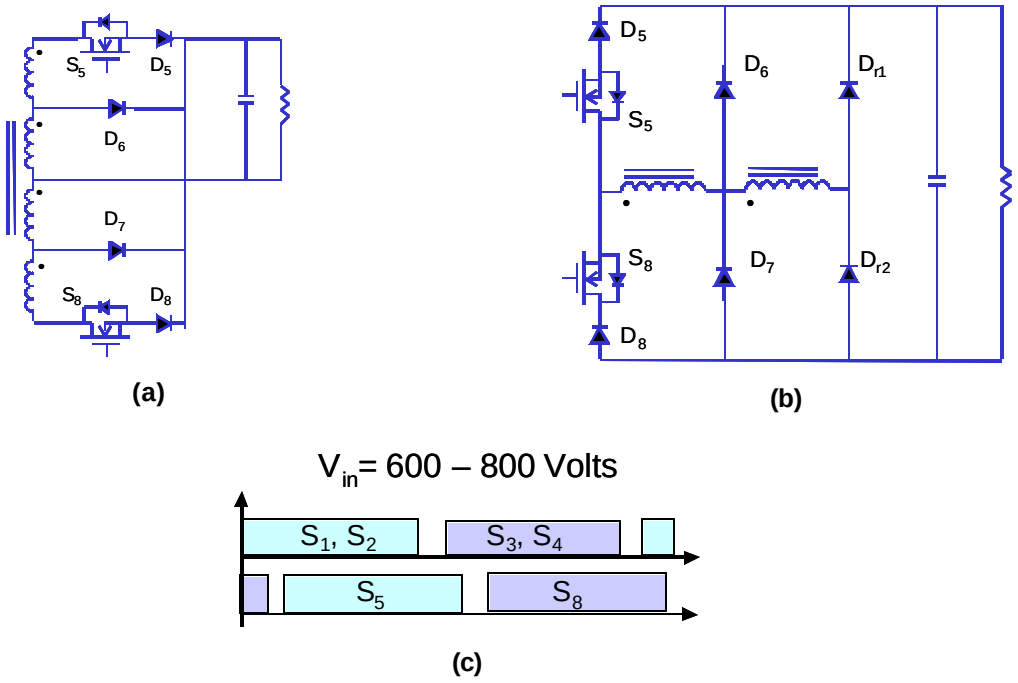


Fig. 4-32. Simplified solutions for wide input-voltage variation in (a) a center-tapped configuration, (b) a full-bridge configuration, and (c) control signals.

4.7.1. Evaluation and Comparison

This section presents a theoretical comparison between the proposed converter that uses a single winding in the secondary side, as shown in Fig. 4-22(a), and the solutions proposed for wide input-voltage variations. Among the solutions for wide input-voltage variations, the center-tapped approaches with full and partial control in the secondary side are considered. This comparison takes into account the conduction and switching losses of all power semiconductors

(active switches and diode rectifiers). The specifications for this comparison are as follows: V_{out} = 60 V, I_{out} = 44.5 A, V_{in} = 600 – 800 V, and f_s = 750 kHz.

It is important to mention that the efficiency was also calculated for each converter using two different MOSFET devices as the primary switches. MOSFET (A) is a 500V, 58A device. MOSFET (B) is a 500V, 32A device that presents higher R_{dson} resistance but better switching characteristics. All converters were designed to work at 0.95 times the resonant frequency and Q=.4. In addition, this design allows the converter to achieve ZVS operation from full load to 10% of full load.

As can be seen in Fig. 4-33, the proposed converter presents low efficiency at high-line input voltage. At this operating condition, the switching losses of the converter are dominant, since the primary switches are turned off almost at the peak of the resonant current. At low-line input, the primary current is allowed to almost complete the entire resonant period, which reduces the turn-off losses. As previously mentioned, the switching losses can be almost eliminated if the converter operates in Mode I. That means that at the turn-off instant, only the magnetizing current circulates through the primary switches. However, the benefits of this could be penalized with higher conduction loss and voltage stress in C_r.

An improvement in the efficiency at high-line conditions can be achieved by placing an auxiliary winding in the secondary side of the transformer. With the auxiliary winding and full-control approach, better optimization of the converter can be achieved, and therefore, the efficiency improvement is more significant. The converter was designed in such a way that at 700V input voltage, the primary current is allowed to almost complete the entire resonant period;

in this way, the turn-off losses are reduced, which improves the efficiency at this operating condition.

Although an improvement in the efficiency of the proposed converter at high-line condition is achieved using the auxiliary winding and partial control approach, it is penalized with an incremental increase in the conduction losses at low line. It is important to mention that the proposed converter, which uses this approach, must be designed in such a way that the converter still regulates the output voltage at high-line and no-load condition. Therefore, optimization of the converter is more difficult to obtain.

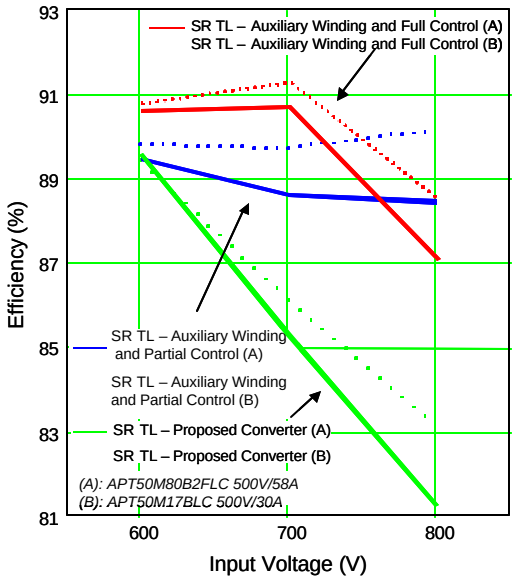


Fig. 4-33. Theoretical efficiency comparison between the proposed converter and the solutions for wide input-voltage variation.

4.8. Experimental Results

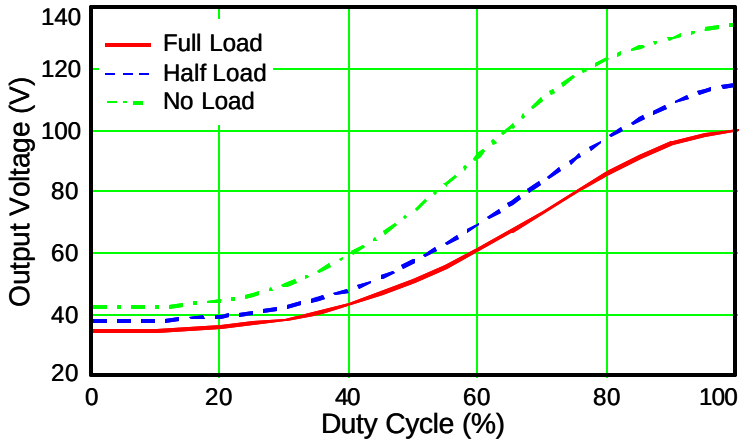
This section presents the design and experimental results for the proposed converter. In order to see the benefits in the converter, it was designed to meet wide input-voltage (600 V-800 V) and load-range variations (4.4 A-44.5 A at 60V output voltage).

4.8.1. Design of the Converter

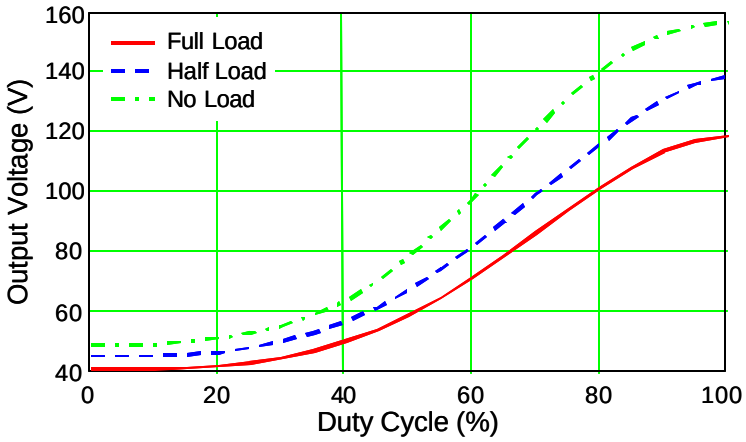
In order to meet the requirement of high power density, the converter was designed to operate with high switching frequency. From a study that determined the optimum switching frequency for the LCT component (integration of the passive components; i.e., inductor, capacitor and transformer), it was decided to operate the converter with a fixed switching frequency of between 700 and 800 KHz. In addition, in an attempt to improve the efficiency shown in Fig. 4-33, the converter was designed with a resonant frequency higher than the switching frequency. In this way, the primary resonant current has more time to resonate, which reduces the turn-off losses for the primary-side switches. In addition, the turns ratio of the transformer was selected in order to provide output-voltage regulation at critical operation conditions. These conditions occur at both full load and 600V input voltage and at no load and 800V input voltage. Fig. 4-34(a) shows the output-voltage variation at 600V input voltage and different load conditions using the duty cycle as a running parameter. As can be seen, for the critical operation condition, the duty cycle is approximately 60%, which means that more than 40% of the duty cycle is available to compensate a loss in the DC-gain characteristic of the converter. On the other hand, Fig. 4-34(b) shows the output-voltage variation for 800 V input voltage and different load conditions. This graph shows that at a no-load condition, the duty cycle can still be reduced such that it compensates for any over-gain characteristic not considered during the design. Table 4-4 shows the principal parameters obtained from the design of the converter.

Table 4-4. Principal parameters obtained from the design of the fixed-frequency ZVS three-level LLC resonant converter with auxiliary winding.

Q	F_n	F_s	N_p	N_{aux}	N_s	Q_t	L_r (µH)	C_r (nF)	L_m (µH)
.37	0.95	745 KHz	7	2	1	4	4.961	8.31	60



(a)



(b)

Fig. 4-34. Output-voltage characteristics for different load conditions for, (a) 600V input voltage and (b) 800V input voltage.

4.8.2. Implementation of the Converter

An experimental prototype was built to verify the operation of the proposed converter. In order to reduce the effect of the wide input-voltage variation, the solution with partial control in the secondary side and full rectification was implemented in the converter. The power stage shown in Fig. 4-35 is comprised of the following components.

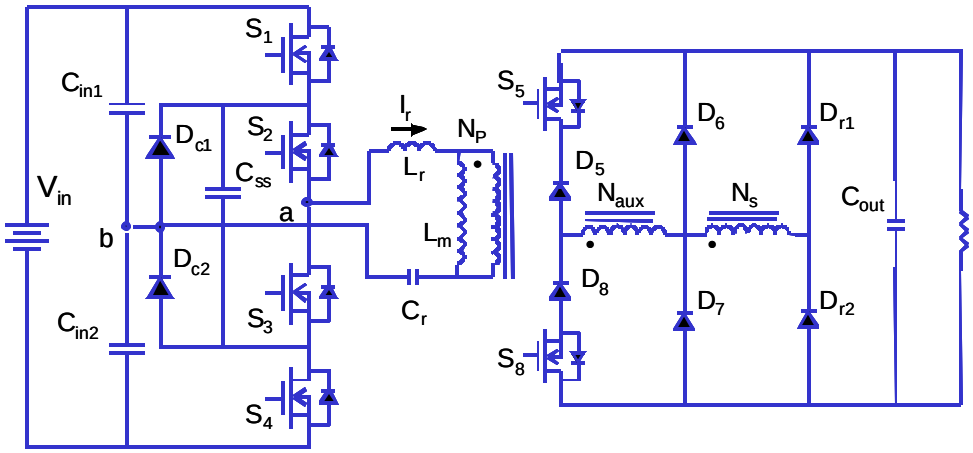


Fig. 4-35. Implementation of the proposed converter.

S_1 - S_4: APT5015BLC

S_5 - S_8: APT20M22LLCX

D_{r1} - D_{r2}: 30CPQ150

D_6 - D_7: 30CPQ150

D_5 - D_8: DSEI60 05A

D_{c1} - D_{c2}: HFA15TB60

C_{in1} - C_{in2}: 2x330nf/400V polypropylene

C_{ss}: 470nF/400V- polypropylene

C_r: 8.36nf – 2x16.5nf/800V ceramic

T_r: E55 – 3F3 7/2/1

L_r: 4.948uH

L_{lk} – 2.788uH

L_r - 2.16uH 6 turns 783E – 3F3

For this design, the transformer was also implemented using a normal E55 core. In this case, Litz wire was used for the primary and secondary windings, and they were placed side by side in

order to reduce the interwinding capacitance of the transformer. It is important to mention that this format causes the leakage inductance of the transformer to increase to 2.78 μH. However, this leakage inductance is absorbed by the resonant inductance. In addition, a small gap was introduced in order to adjust the magnetizing inductance of the transformer to the calculated value (60 μH).

Similar to the variable-frequency operation, the future implementation of the passive elements in the converter (the transformer, resonant capacitor and resonant inductor) into an LCT structure should be considered in order to improve the power density in the converter.

4.8.3. Experimental Results

Fig. 4-36(a) shows the voltage across the primary side of the transformer, the primary resonant current, and the voltage across the secondary switches. These waveforms were taken at 350V input voltage, 33.5V output voltage and 17.1A output current. As shown, there is a voltage spike across the secondary switches. This spike occurs due to the resonance among the reflected leakage inductance to the secondary side, the stray inductance in the secondary side, and the parasitic capacitance of the secondary switches. Since the goal is to continue using 200V switches in the secondary side, an RCD snubber was placed across each secondary switch. Fig. 4-36(b) shows the same waveforms presented in the previous figure but with the RCD snubbers in the secondary switches. These waveforms were taken at 500V input voltage, 49.8V output voltage and 24.4A output current.

Although a reduction in the voltage spike across the secondary switches can be achieved by using an RCD snubber, this is not a viable solution to the voltage spike problem due to power

dissipation and space constraints. Fig. 4-37 shows a possible solution for reducing this problem. Here, a flying capacitor is placed across secondary switches S_5 and S_8. This capacitor should clamp the voltage across the switches during the instant of turn-on and turn-off. In this case, the resonance across the switches depends on both the parasitic capacitance of the secondary switch and the parasitic stray inductance that occurs due to the layout. Therefore, the stray inductance of the layout should be minimized. Fig. 4-37(b) shows the bottom layer of the new layout for the secondary side. Nine decoupling capacitors, each with a value of 5uF, were placed between the positive and negative rails in order to minimize the stray inductance of the layout. In addition, C_{sec} is placed close to the secondary switches.

The next experimental results were obtained using the capacitor C_{sec} and the new layout. Fig. 4-38 shows the voltage across the primary side of the transformer and the primary resonant current. These waveforms were taken at full-load conditions and nominal input voltage; that is, 800V input voltage, 60V output voltage and 42.55A output current. The primary-side layout of the converter was modified in order to measure the current through one of the primary switches. This modification resulted in a resonance across the primary-side voltage.

Fig. 4-39 shows the drain-to-source voltages V_{DS} and the drain current through S_3, also obtained at nominal input voltage and full-load condition. It can be seen that the maximum voltage for S_3 is 400 V, just half of the level of the input voltage. Also, it can be observed that the voltage falls to zero prior to the turn-on of the switch. Therefore, a ZVS transition is achieved.

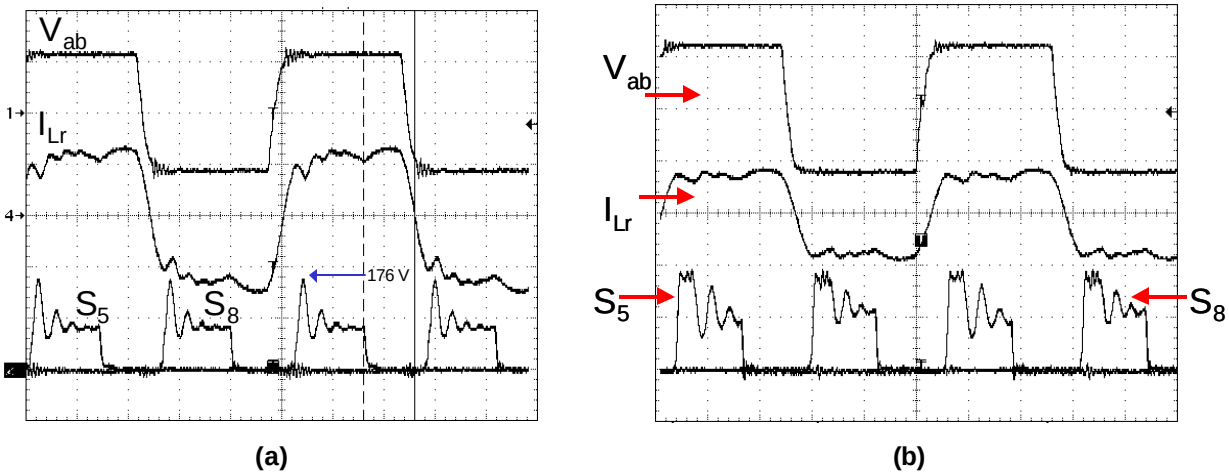


Fig. 4-36. (a) Voltage across the primary side of the transformer (upper trace), primary resonant current (middle trace) and voltage across the secondary switches (lower traces) (150 V/div, 2 A/div, 100 V/div, 100V/div, 250ns/div); and (b) the same waveforms, but with an RCD across the secondary switches (200 V/div, 5 A/div, 100 V/div, 100V/div, 250ns/div).

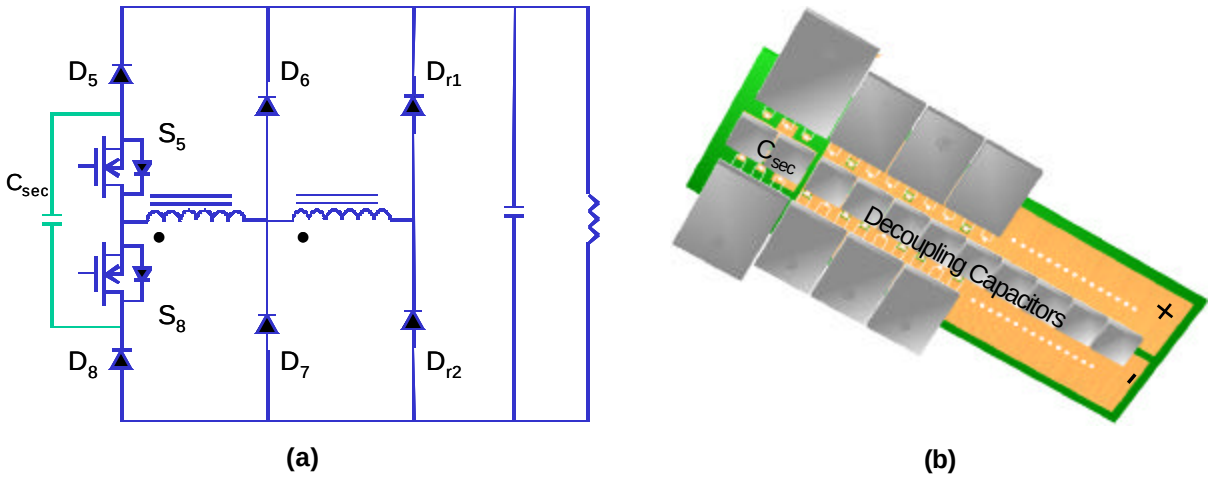


Fig. 4-37. Solution to the voltage spike across the secondary switches: (a) adding a flying capacitor C_{ss} across secondary switches S_5 and S_8 and (b) reduction of the stray inductance.

Fig. 4-40 shows the voltage across the secondary devices at full-load condition. Fig. 4-40(a) shows the voltage across diode rectifiers D_{r2} and D_8, and the drain-to-source voltage across switch S_8. In addition, Fig. 4-40(b) shows the voltage across diode rectifier D_7. The new layout for the secondary side and the flying capacitor C_{sec} both help to reduce the voltage spike across the devices. It is important to mention that no snubber circuit is used for the secondary devices.

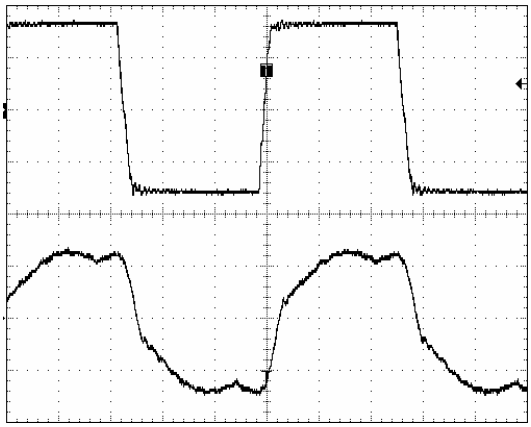


Fig. 4-38. Experimental results. Voltage across the primary side of the transformer and primary resonant current (200 V/div, 10 A/div, 250 ns/div).

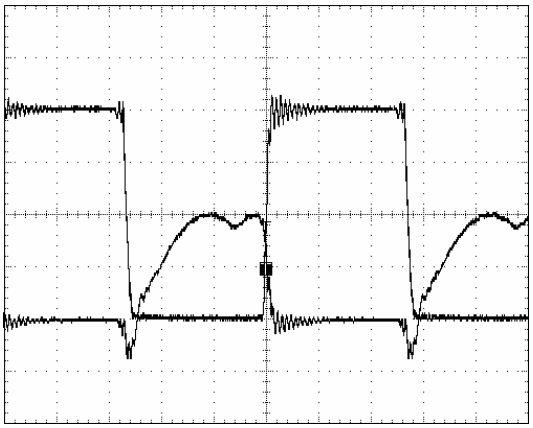
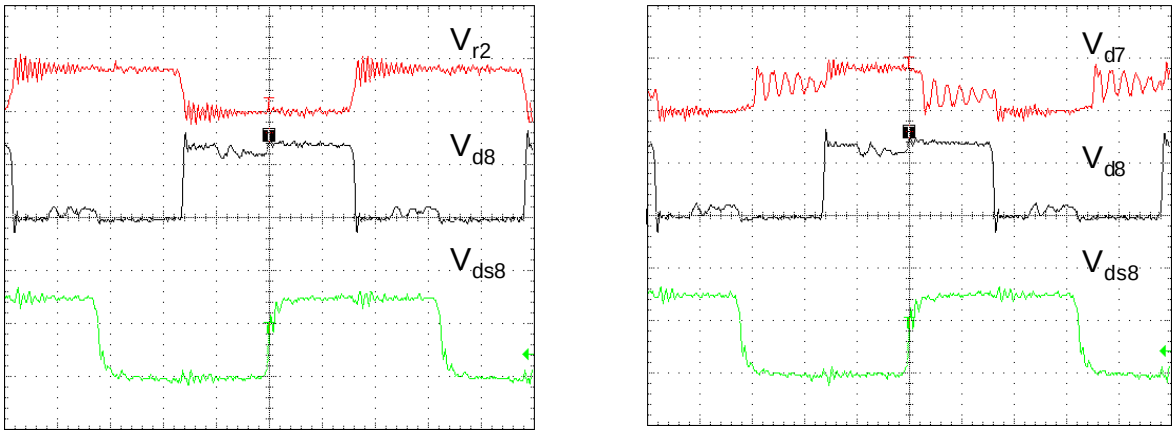


Fig. 4-39. Drain-to-source voltage and drain current through S_3 at high-load condition (100 V/div, 5 A/div, 250 ns/div).



(a) **(b)**

Fig. 4-40. Main waveforms in the secondary side: (a) voltage across D_{r2}, voltage across D_8, and drain-to-source voltage across S_3 (75 V/div, 150 V/div, 100 V/div 200 ns/div), and (d) voltage across D_7, voltage across D_8, and drain-to-source voltage across S_3 (75 V/div, 150 V/div, 100 V/div, 200 ns/div).

Fig. 4-41 shows again the drain-to-source voltages, V_{DS}, and the drain current through S_3, but at nominal input voltage and low-load condition. It can be observed that ZVS operation is still achieved despite the low-load condition. As was explained before, placing the control in the secondary side allows ZVS operation for a wide load range without penalizing the circulating energy, as shown in Fig. 4-42. This figure shows the drain current through switch S_3 for different load conditions. Fig. 4-43 shows again the primary resonant current at full-load condition and at several input voltages. The circulating energy is almost fixed for any load and input-voltage conditions.

Fig. 4-41. Drain-to-source voltage and drain current through S_3 at low-load condition (100 V/div, 5 A/div, 250 ns/div).

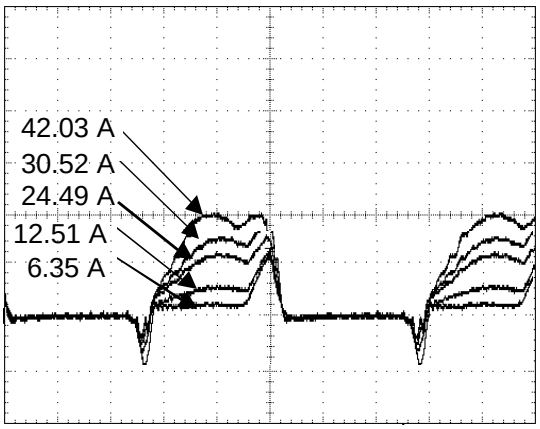


Fig. 4-42. Drain current through S_3 for different load conditions (5 A/div, 250 ns/div).

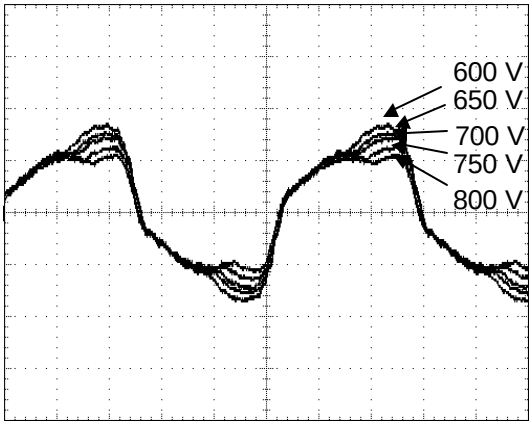


Fig. 4-43. Primary resonant current at full load and different input voltage conditions, (5 A/div, 250 ns/div).

The experimental measured efficiency as a function of the output power at nominal input voltage 800 V is shown in Fig. 4-44. The efficiency at full-load condition is 90.8%, and the maximum efficiency of the converter, which occurs around 1820 W, is 91.2%. As can be seen, the operation at fixed-frequency is penalized by almost 3% as compared to the variable-frequency operation. Despite the proposed solution for minimizing the effect of wide input-voltage and load variations, the converter still presents higher turn-off losses for the primary devices and conduction losses in the secondary side when compared to the variable-frequency operation.

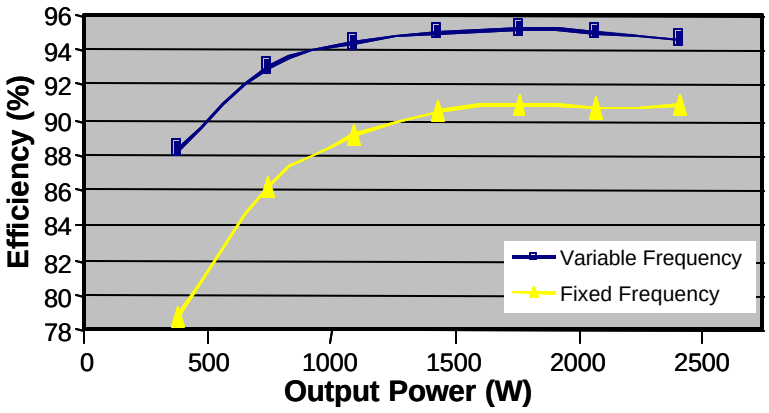


Fig. 4-44. Efficiency comparison for the proposed converter at nominal input voltage using the output power as a running parameter.

Fig. 4-45 shows a measured efficiency comparison for the proposed converter under fixed and variable frequencies as a function of the input voltage at full-load condition. It can be seen that for fixed-frequency operation, the efficiency also decreases as the input voltage decreases. Although the primary losses are maintained at an almost constant level for different input-voltage conditions, as shown in Fig. 4-43, the conduction losses in the secondary increase as the input voltage decreases. As the input voltage decreases, the auxiliary secondary needs to conduct for a longer time to compensate the loss of gain in the converter. It is important to mention that this reduction of the input voltage occurs only during hold-up time; therefore, this does not represent a thermal issue for the converter.

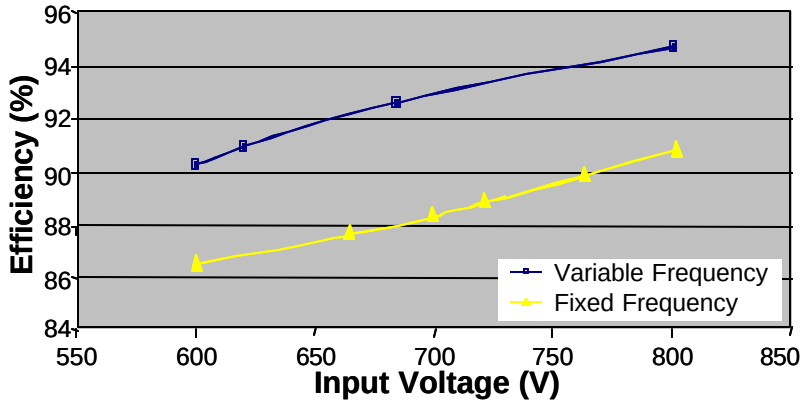


Fig. 4-45. Efficiency comparison for the proposed converter at full-load condition using the input voltage as a running parameter.

4.9. Conclusion

This chapter explores the benefits obtained by operating three-level structures at high-switching frequencies. Soft-switching techniques and modulation strategies for resonant converters were analyzed in a systematic way in order to determine the best soft-switching technique that fulfills specifications related to future telecommunications power supplies, such as high efficiency and high power density.

From this analysis, a novel ZVS three-level LLC resonant DC/DC converter was proposed. The operating stages and characteristics of the proposed converter under fixed and variable switching frequencies were presented. Experimental results for a 2.75KW prototype were shown in order to verify the operation of the converter.

It was shown that in both operating modes, the proposed converter could operate with a wide ZVS range by using the magnetizing inductance of the transformer. For the fixed-frequency operating mode, the control was performed in the secondary side of the transformer, which helped to increase the ZVS range and also reduced the circulating energy in the converter.

In addition, this chapter presented some solutions for reducing the impact of the wide input-voltage variations, which also help to reduce the circulating energy in the converter and improve the efficiency at nominal operating condition. These characteristics make the proposed converter an interesting option for high-voltage, high-power applications that require high power density and high efficiency.

5. Integrated Converters

5.1. Introduction

Previous chapters proposed high-voltage DC/DC converters based on a three-level structure. The main characteristics for these converters are the reduction of the voltage stress across the main devices, allowing the use of low-voltage-rating devices, which have better electrical characteristics, and soft-switching capability without introducing complexity in the operation of the converter. As it was shown, these characteristics not only improve the efficiency of the converter, but also offer the opportunity for higher-switching-frequency operation.

The combination of the proposed DC/DC converters with three-phase PFC converters, such as the VIENNA rectifiers or even more simple approaches such as the single-switch or two-switches boost rectifiers working in DCM, helps to reduce the complexity and cost of the DPS for high-power applications.

As mentioned before, integrated converters have also been proposed to further reduce the complexity and cost of the DPS without reducing the performance of the system. However, this simplification is usually penalized with high voltage stress across the main devices.

In order to minimize this problem, an integrated converter based on a three-level structure has been proposed [96]. One of the disadvantages that this integrated converter presents is that the discontinuous current from the AC side and the current from the DC/DC side must always flow through two switches simultaneously. Moreover, these currents result in a high peak current

during the turn-off of the switches, which produces high turn-off losses. The resulting efficiency is considered low for this power level.

To reduce these problems, this chapter presents a quasi-integrated AC/DC three-phase converter, which improves the complexity / low-efficiency tradeoff characteristics over the previously discussed DPS approaches. This converter achieves both PFC and output voltage regulation in a single stage of power conversion. Some of the main characteristics of the converter are low number of components, lower THD when compared with the single-switch boost rectifier, fast regulation, and improvement in the efficiency with a simple control. The proposed converter also offers the advantage of reducing the voltage stress across the switches. In addition, a soft-switching technique can be implemented in the proposed converter without adding complexity.

5.2. Development of Integrated Converter Based on Structures that Reduced the Voltage Stress Across the Main Devices

Fig. 5-1 shows a three-phase DPS for high-power applications that is based on a two-stage approach. The PFC is implemented with the three-phase two-switch three-level boost rectifier [105]. In this approach, the boost inductors operate in DCM to achieve high power factor. One of the advantages of this rectifier is that by using a three-level structure, the voltage stress across each switch is reduced. Therefore, 600V MOSFET devices can be used, even though the total bus voltage is regulated to 800 V. The second stage is implemented with the ZVS three-level DC/DC converter proposed in Chapter 2. The advantage of a two-stage approach is that both converters can be optimized, which improves the overall performance of the front-end converter.

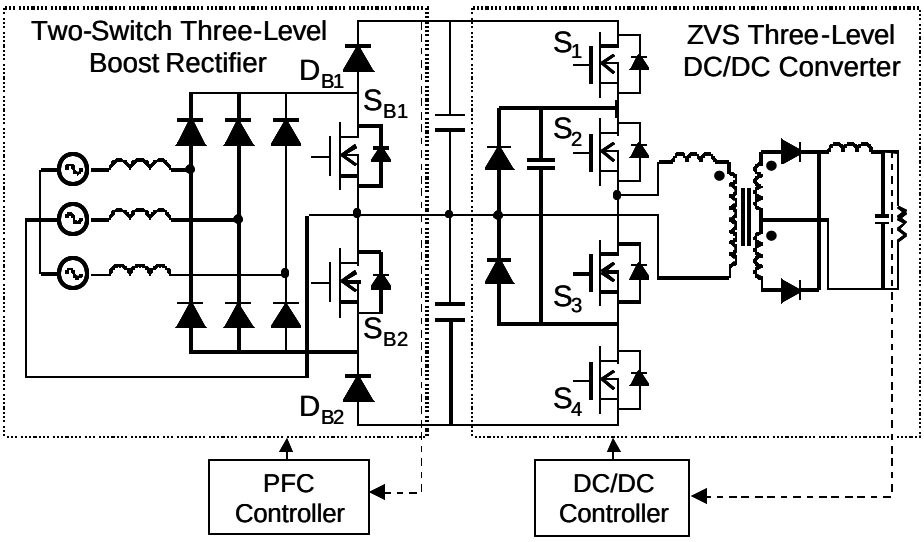
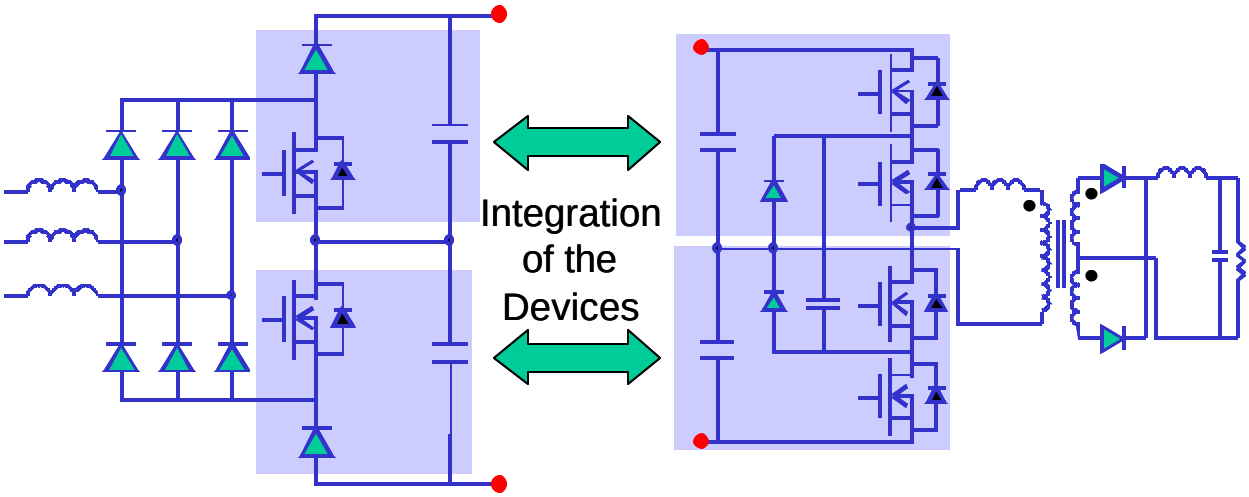


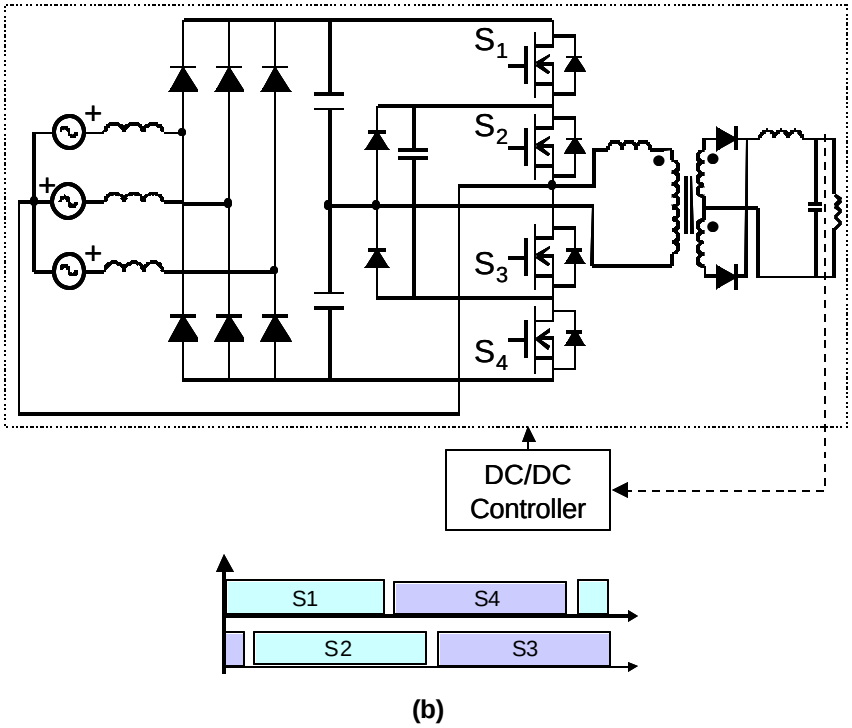
Fig. 5-1. Two-stage three-phase DPS for high-power applications, based on three-level topologies.

Fig. 5-2 shows the integration of these two topologies; the result is the single-stage ZVS three-level AC/DC three-phase converter [96]. This converter is based on the ZVS three-level DC/DC converter and maintains its main characteristics: ZVS operation for all the switches, phase-shift control, and reduced voltage stress across the main devices. The input inductors of the converter also operate in DCM to obtain PFC.

To realize the integration, common cells are identified that can be shared without penalizing the main characteristics in the performance of the converter. As shown in Fig. 5-2(a), the function of the boost switch S_{B1} was replaced with the devices S_1 and S_2 of the DC/DC converter. As a result, just one control is needed to perform both the PFC and the DC/DC task, as shown in Fig. 5-2(b). That means that when these two switches are on, not only is power delivered to the output, but also, energy is stored in the input inductors. One of the main drawbacks of sharing the devices in this way is that the AC current always circulates through two devices. This increases the conduction losses as compared to the PFC converter in the two-stage approach. Fig. 5-3 shows the trajectory of the AC and DC current in the integrated converter.



(a)



(b)

Fig. 5-2. Integration of the power stages: (a) sharing the main devices and (b) the single-stage ZVS three-level AC/DC three-phase converter.

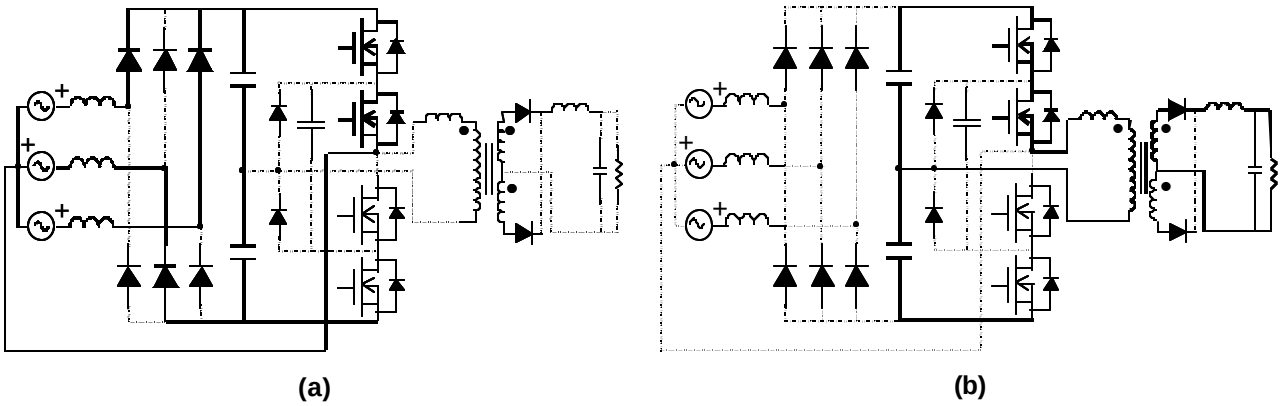


Fig. 5-3. Main characteristics for the proposed ZVS three-level AC/DC three-phase converter. (a) AC current trajectory and (b) DC current trajectory.

Fig. 5-4 shows the main results for a 3kW converter. Since there is only one controller, the intermediate bus voltage fluctuates to balance the input and output power according to the input-voltage and output-load variations, as shown in Fig. 5-4(a). As can be observed, the intermediate bus voltage increases as the power decreases, until the output inductor reaches DCM operation. At this point, the variation in the bus voltage is maintained at an almost constant level. The operating point at which the output inductor reaches DCM can be selected in such a way that the bus voltage is limited to a desired level; however, it is also penalized with high RMS current and high peak current during the turn-off. Therefore, a tradeoff between the voltage stress and the losses in the devices should be considered. Because of the level in the intermediate bus voltage during critical operation (before the output inductor reaches DCM operation), it is necessary to use 800V MOSFETs. The combination of high RMS current with devices that present high R_{dson} is penalized with lowered efficiency in the converter, as shown in Fig. 5-6(a).

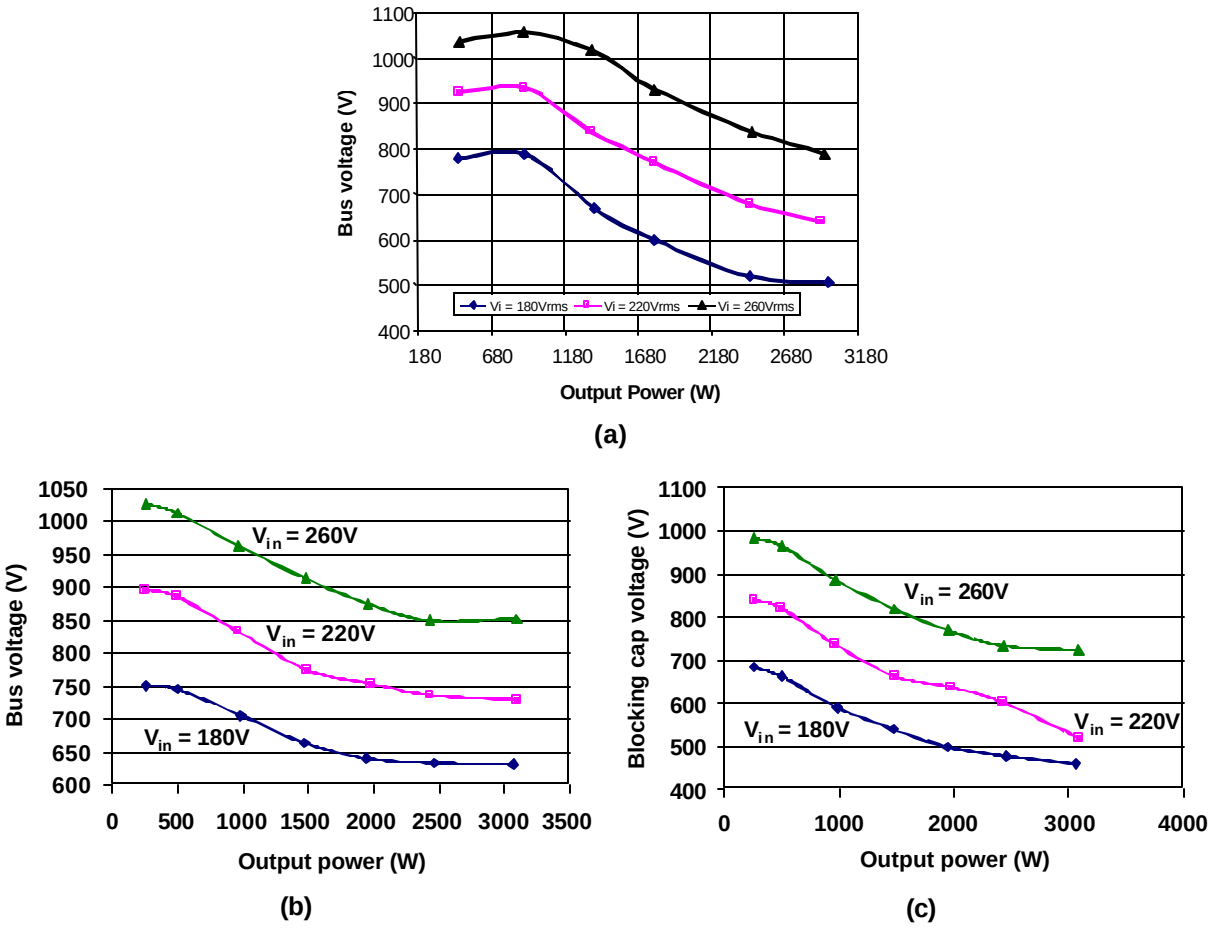


Fig. 5-4. Problematic voltage stress in integrated converters. Intermediate bus voltage stress for (a) single-stage three-level converter and (b) single-stage with asymmetrical control and (c) voltage stress in the DC blocking capacitance for single-stage with asymmetrical control.

The idea of an integrated converter based on topologies that reduce the voltage stress across the main devices can be extended, as shown in Fig. 5-5. This integrated converter [97] is based on a two-stage front-end converter using the two-switch boost rectifier working in DCM and the ZVS three-level DC/DC converter using asymmetrical control [25]. In this case, the boost switches are eliminated, and the switch S_2 is shared to realize the PFC and DC/DC functions. In addition, the anti-parallel diode of the switch S_2 is used as the boost diode. Thus, the ZVS characteristic and the reduction of the voltage stress across the primary switches is maintained

with operation in asymmetrical control. In addition, the reduction of the number of switches in series during each operating stage reduces the conduction losses.

Fig. 5-6 shows experimental results for a 3kW converter. As can be seen, this new integration results in improvement in the efficiency as compared to the former integrated converter. However, in this integrated converter, the simplification of the control strategy also results in a fluctuation in the bus voltage, as shown in Fig. 5-3(b). This problem becomes even worse in this approach, since the bus-voltage variation penalizes the voltage stress across the DC blocking capacitance that allows asymmetrical operation [97]. As can be seen in Fig. 5-3(c), this voltage can reach 1000 V at high-line input voltage and light-load condition. Therefore, special characteristics for this blocking capacitor are needed, which increases the cost of the converter. In addition, the transformer should be designed to handle the DC current that occurs due to asymmetrical operation. Fig. 5-6(b) shows the THD produced by this integrated approach. As can be seen, the converter presents a THD higher than 10 % for all input-voltage conditions. In addition, the THD produced by this converter is higher than that presented by the former integrated converter.

Fig. 5-6(a) also shows the measured efficiency for a two-stage approach. In this case, the PFC is implemented with the three-phase two-switch three-level boost rectifier operating at 40 kHz, and the DC/DC converter is implemented with a ZVZCS three-level converter with an auxiliary circuit in the secondary side, also proposed in this dissertation. The DC/DC converter operates at 100 kHz. It can be seen that by using a two-stage approach, the front-end converter can be optimized from the efficiency standpoint. However, this is penalized with complexity and cost.

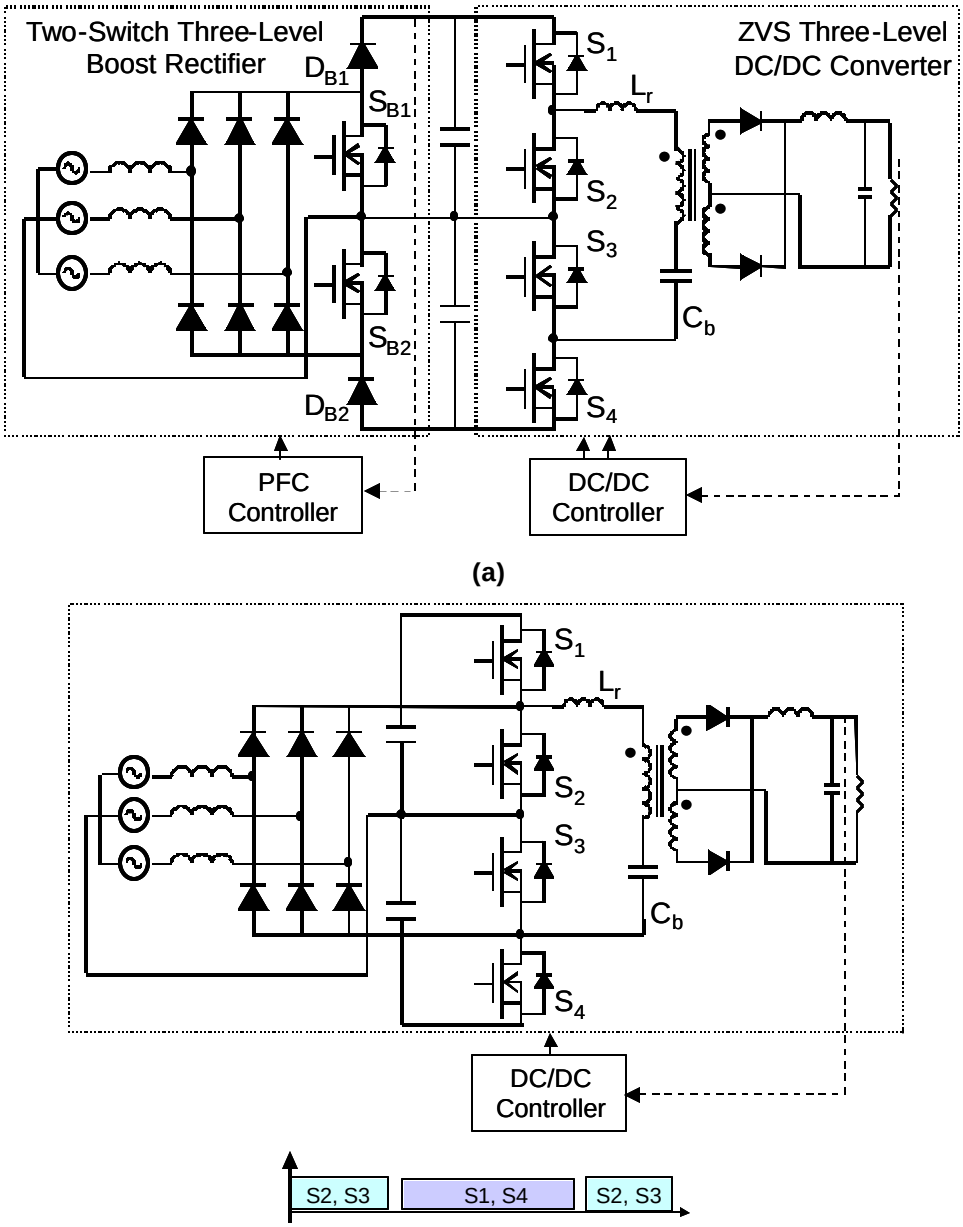


Fig. 5-5. Integration of the power stages. (a) Two-stage approach front-end converter and (b) the single-stage ZVS three-level AC/DC three-phase converter with asymmetrical control.

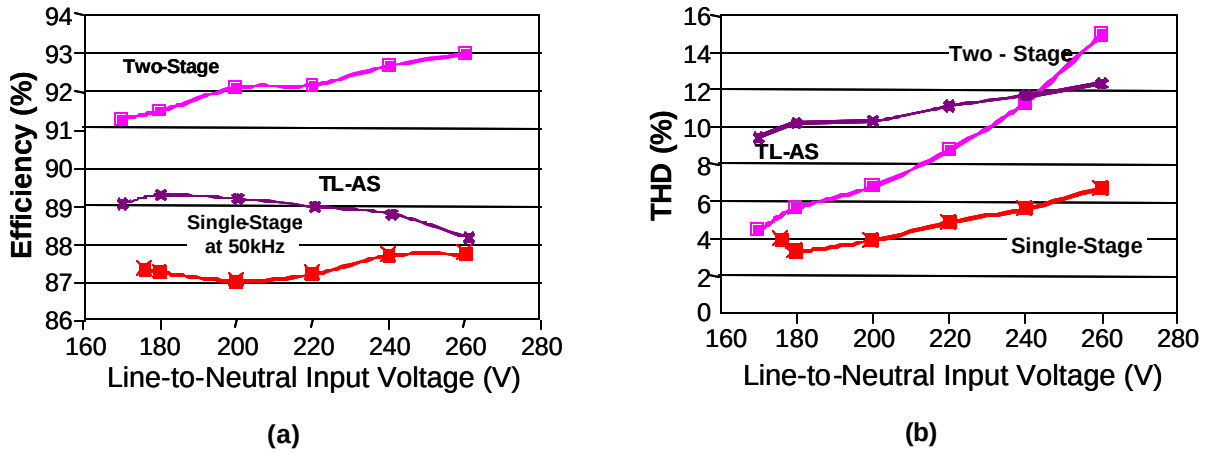


Fig. 5-6. Results and comparison for the integrated converters: (a) efficiency comparison and (b) THD comparison.

In order to improve the characteristics of the previous integrated converter, it is interesting to search for topologies that present similarities in the cells that could be integrated. Fig. 5-7(a) shows another two-stage approach for three-phase high-power applications. As can be seen, the PFC converter is also implemented with the two-switch three-level boost rectifier. However, the DC/DC converter is implemented with a dual-bridge converter [26], [27]. Similar to the three-level DC/DC converter proposed in this dissertation, this topology also allows a reduction of the voltage stress across the main devices, thus becoming another interesting approach for high-voltage applications. The converter operates with phase-shift control in which all switches operate with duty cycles of nearly 50%. The phase shift between S_1 and S_2 or S_3 and S_4 determines the operating duty cycle of the converter. ZVS operation for all the switches is achieved by using the leakage inductance of the transformer or an external resonant inductance.

As shown in Fig. 5-7(b), it is possible to identify similar cells in both converters. By integrating these converters, the function of the boost switch S_{B1} or S_{B2} is shared with the switch S_2 or S_3 of the DC/DC converter. In this case, just S_2 should be able to handle the AC input current and the DC current. Therefore, the conduction losses of the converter are reduced, when

compared with the previous approach. Another benefit that could be achieved by considering the independence of the switches S_1 and S_4 is to create another control variable in the operation of the converter, which helps to control the intermediate bus voltage. The result from this integration is shown in Fig. 5-8

The next section shows the main characteristics that result from integrating the two-switch three-level boost three-phase rectifier with the ZVS dual-bridge DC/DC converter.

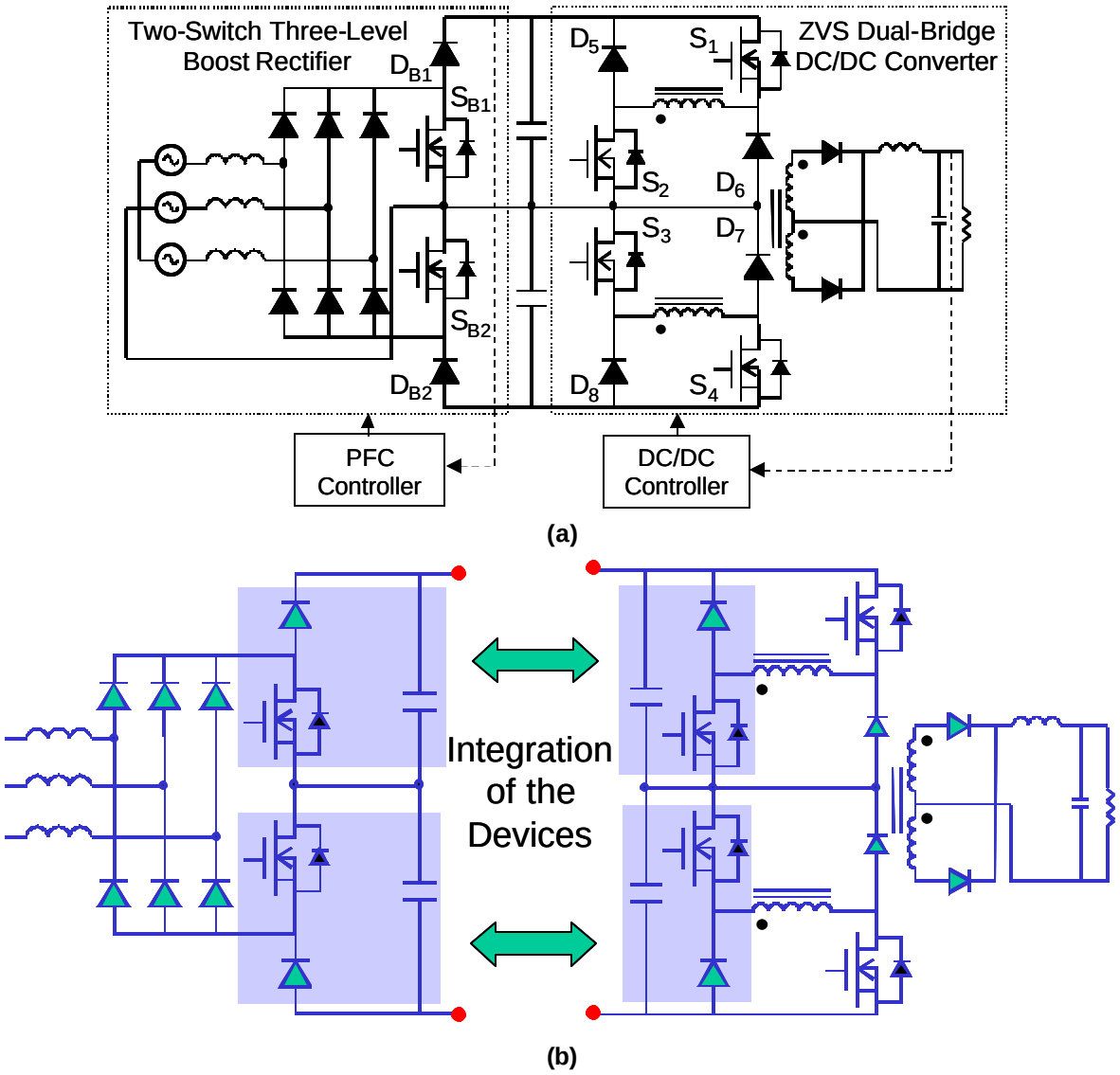


Fig. 5-7. Two-stage three-phase DPS for high-power applications using a dual-bridge topology as a DC/DC converter and (b) identification of similar cells to share the main devices.

5.3. A Quasi-Integrated AC/DC Three-Phase Dual-Bridge Converter

The proposed converter and its timing diagram are shown in Fig. 5-8. It can be seen that the basic structure is similar to that of the dual-bridge DC/DC converter previously presented [27]. The main difference is the inclusion of the three-phase bridge rectifier connected between points a and b. Thus, a three-phase two-switch boost rectifier working in DCM is formed by the three-phase bridge rectifier, inductors L_1, L_2 and L_3, switches S_2 and S_3, diodes D_5 and D_8, and capacitors C_{in1} and C_{in2}. This two-switch boost rectifier performs the PFC function with low THD in the integrated converter by running the input inductors L_1, L_2 and L_3 in DCM. In addition, it regulates the intermediate bus voltage (the voltage across capacitors C_{in1} and C_{in2}) by changing the pulse width applied to switches S_2 and S_3. The function of the isolated DC/DC converter in the quasi-integrated approach is achieved with a dual-bridge structure. The dual-bridge converter is implemented with switches S_1, S_2, S_3 and S_4, diodes D_5, D_6, D_7 and D_8, the power transformer, output rectifiers D_{r1} and D_{r2}, and the output filter. Switches S_1 and S_4 operate with nearly 50% duty cycle, and in order to regulate the output voltage, a phase shift is introduced between switches S_1 and S_2 or S_3 and S_4; it is thus possible to achieve ZVS operation for switches S_1 and S_4.

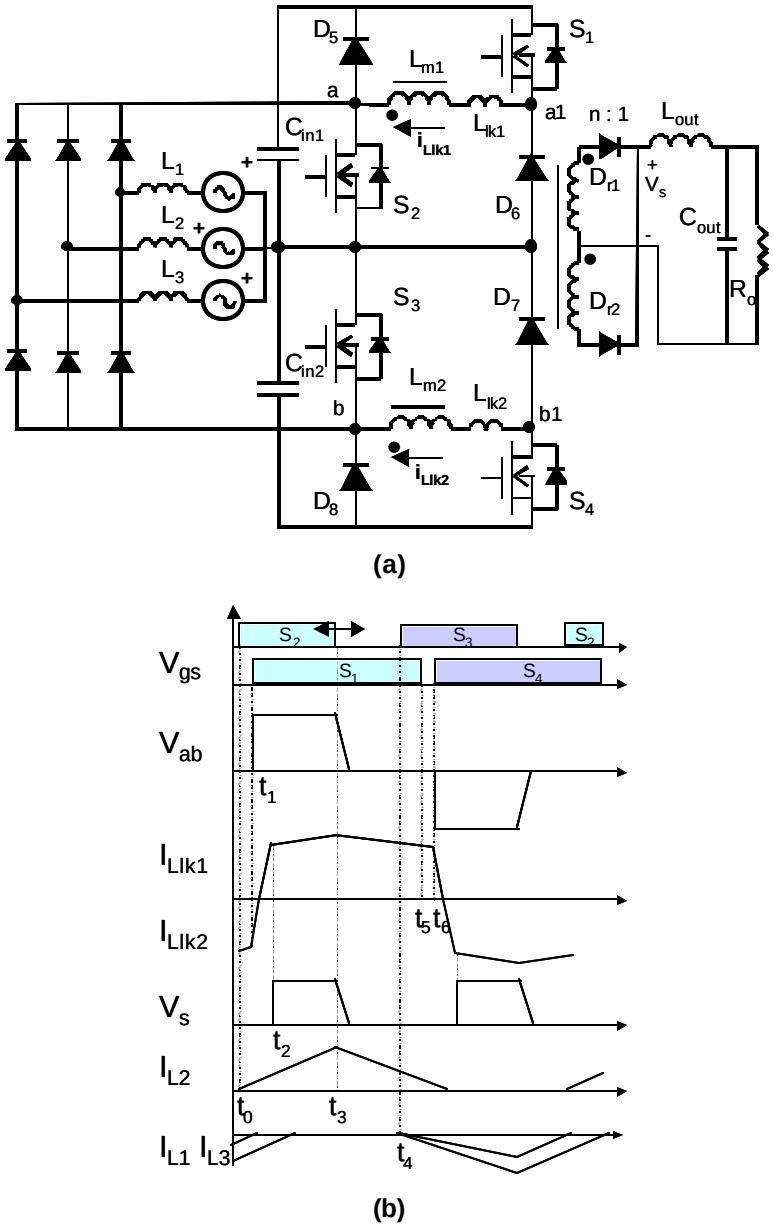


Fig. 5-8. (a) The proposed quasi-integrated three-phase AC/DC dual-bridge converter and (b) its main waveforms.

The proposed converter has six operating stages during a half-switching cycle. For the polarity of the input voltages shown in Fig. 5-8, the following operating stages will occur within one half of a switching cycle. The equivalent circuit for each stage of operation is shown in Fig. 5-9, and the stages are described as follows.

[t_o-t_1]: At t_0, S_2 is turned on, and the current in L_2 increases linearly, while the currents in L_1 and L_3 decrease. The primary current in the DC/DC converter freewheels mainly through S_4 and D_8 in the bottom part of the converter, and a small current flows through S_2 and D_6 in the top part of the converter due to the coupling of the primary windings. In the secondary side, the output current freewheels through diode rectifiers D_{r1} and D_{r2}.

[t_1-t_2]: During this stage, the current in L_2 and the currents in L_1 and L_3 continue increasing and decreasing, respectively. At the beginning of this stage, S_2 is turned on, half of the intermediate bus voltage is applied across the transformer, and the primary current I_{Lk2} starts to decrease. At the instant at which the primary current I_{Lk2} reaches zero, the primary current I_{Lk1} starts to flow through S_1 and S_2. This current increases with a slope equal to $V_{bus}/(2L_{lk1})$. This stage ends when I_{lk1} reaches the level of the reflected output current.

[t_2-t_3]: During this stage, the input power is delivered to the output. The current in L_2 continues to increase.

[t_3-t_4]: At t_3, S_2 is turned off, and the current in L_2 starts to decrease. At the end of this stage, the currents in L_1 and L_3 must be completely reset. In the DC/DC converter, the primary current freewheels through S_1 and D_5. In the secondary side, the output current freewheels through diode rectifiers D_{r1} and D_{r2}.

[t_4-t_5]: At t_4, S_3 is turned on, and the current in L_1 and L_3 increases. The current in L_2 continues to decrease. In the primary and secondary sides, the currents continue to freewheel.

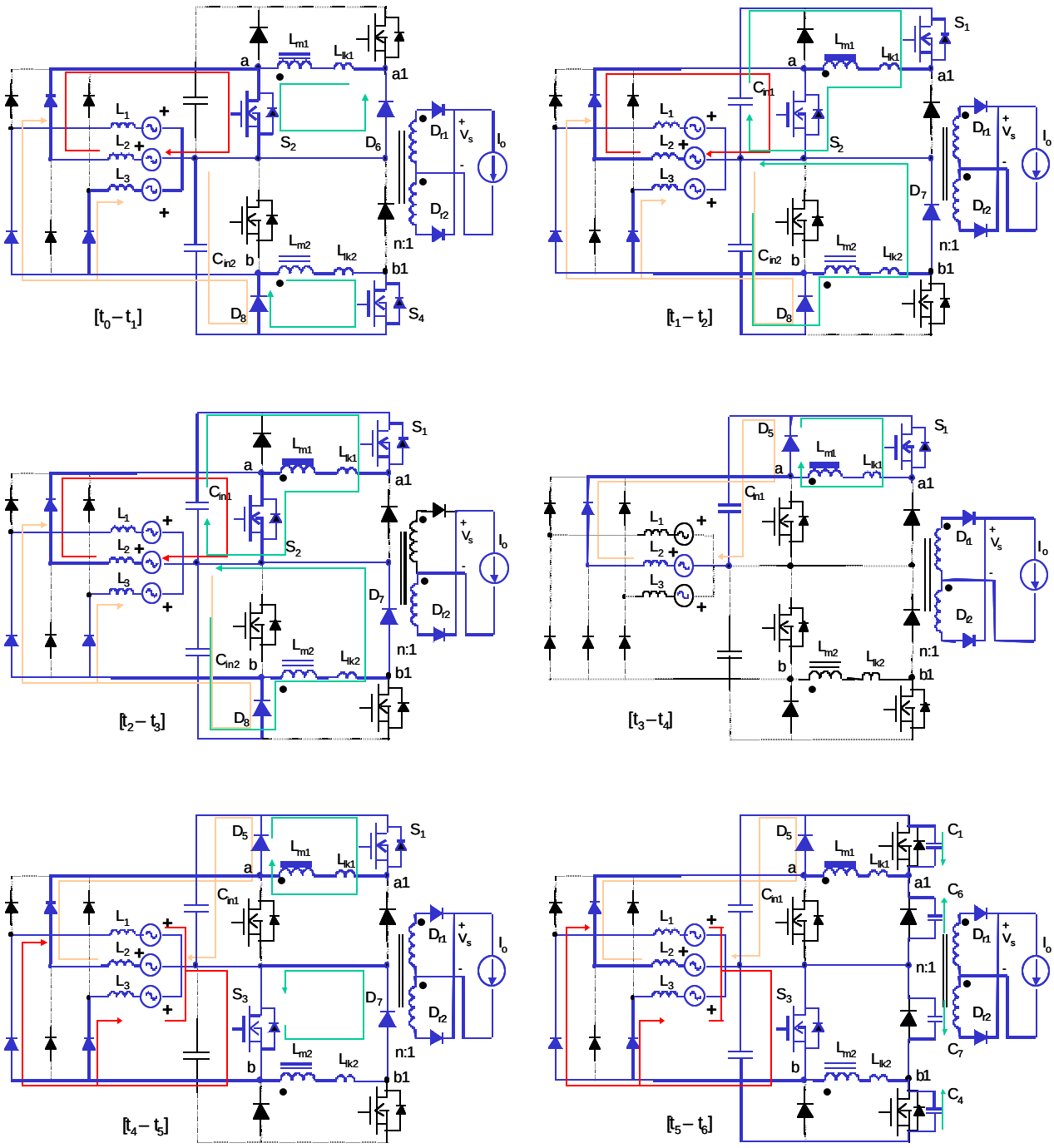


Fig. 5-9. Equivalent circuit for each stage.

[t_5-t_6]: At t_5, S_1 is turned off, and the leakage inductances of the transformer, L_{lk1} and L_{lk2}, resonate with the parasitic capacitances of switch S_1 and diode D_6, and S_4 and D_7, respectively. The voltage across S_2 increases to half the intermediate bus, and the voltage across S_4 decreases to zero to turn on the anti-parallel diode of S_4. At the end of this stage, a new switching cycle starts when S_4 is turned on with ZVS and half of the intermediate bus voltage is applied across the transformer.

5.3.1. Analysis of the Proposed Converter

This section presents the analysis of the proposed converter. A simplification in the analysis of the converter can be achieved by considering the proposed converter as two separate stages; that is, the PFC stage and the DC/DC converter. In this way, the only relationship that exists between the two stages is the limitation of the duty cycle in the DC/DC converter imposed by the PFC stage, as explained in the previous section. Therefore, the discussion in this section is divided into AC- and DC-side analyses.

A. AC-Side Analysis

As explained in other work [88], the connection between the middle point of the converter and the AC sources allows third and odd multiple harmonics to flow through the neutral of the power system, thus increasing the harmonic distortion in the line currents. To eliminate the undesirable circulation of these harmonics in the AC line, an artificial neutral connection can be provided by AC capacitors [105]. Fig. 5-10 shows the proposed converter with the inclusion of the AC capacitors.

With this approach, the line currents will be free of any third and odd multiple harmonics. However, the inclusion of the AC capacitors modifies the rectifier voltage gain characteristic in the converter and makes it difficult to obtain closed-form solutions for the rectifier equation. One way to simplify the problem is to use simulation tools to obtain the main characteristics of the converter, such as voltage gain and variations in the PFC duty cycle that occur due to input-line and load-output variations. These characteristics are important to the design of the proposed converter.

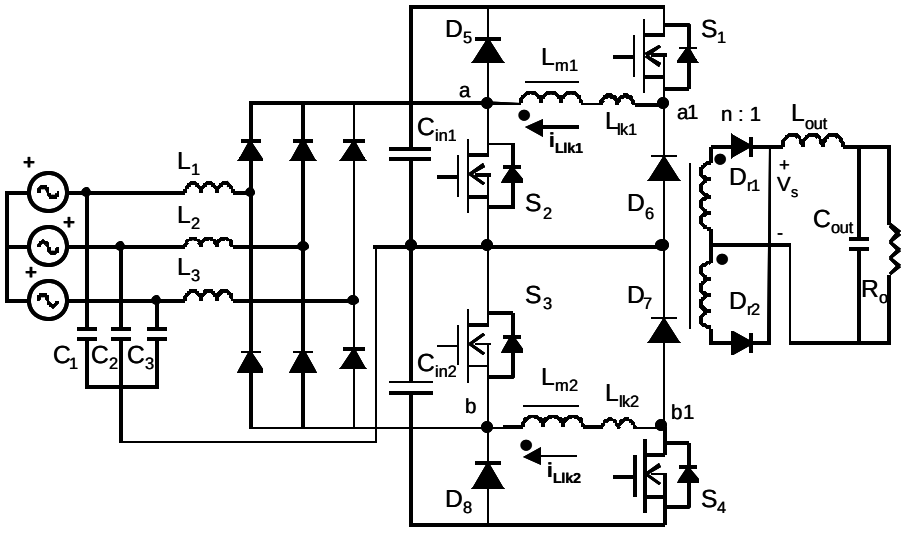


Fig. 5-10. Proposed converter with artificial neutral connection to eliminate the third and odd multiple harmonics from the line currents.

Fig. 5-11 shows the simulated voltage gain at heavy load versus the normalized output current. The simulation is performed in such a way that the input inductance value is selected to provide critical conduction at high line and full load. The voltage gain (M) and the normalized output current (I_{norm}) shown in Fig. 5-11 are defined by

$$M = \frac{V_{bus}}{V_{pk}}$$
$$I_{norm} = \frac{I\,L\,f_s}{V_{pk}} \qquad (4\text{-}1)$$

where V_{bus} is the intermediate bus voltage, V_{pk} is the line-to-neutral peak input voltage, I is the intermediate average bus current, L is the boost inductance, and f_s is the switching frequency.

It is important to mention that in order to obtain the results given in Fig. 5-11, the AC capacitors must be incorporated by the differential mode (DM) input filter, in which typical values for the AC capacitances will range from 1 μF to 3 μF.

A more detailed explanation of the method for obtaining this graph is given in other work [105].

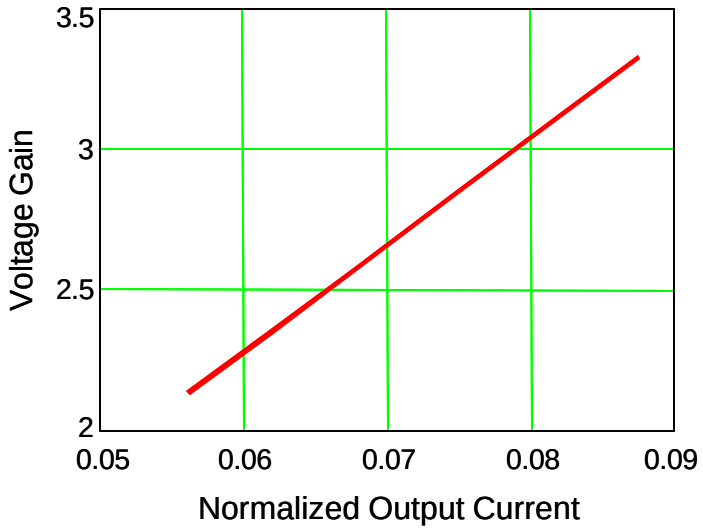


Fig. 5-11. Voltage gain versus normalized output current at heavy load.

B. DC-Side Analysis

One of the potential disadvantages of the proposed converter is the limitation of the maximum duty cycle for the DC/DC converter that is imposed by the PFC stage. This limitation becomes critical at high-line AC-input voltage and low output-load conditions. In order to minimize this problem, the converter can be designed to operate in DCM during these conditions. For this case, the DC output voltage in the converter is given by

$$V_o = \frac{(D_{dc} V_{bus})^2}{2n(2n I_o L_{out} f_s + V_{bus} D_{dc}^2)}, \tag{4-2}$$

where I_o is the load average current, n is the transformer turns ratio, L_{out} is the output filter inductance, and D_{dc} is the duty cycle for the dual-bridge DC/DC converter.

For the condition in which the DC/DC converter works in CCM, the output voltage is given by

$$V_o = \frac{D_{dc}}{n} V_{bus} - \frac{4}{n^2} I_o L_{Lk} f_s, \tag{4-3}$$

where L_{lk} is either the parasitic inductance of the transformer or an external inductance placed in series with the transformer in order to obtain ZVS operation for S_1 and S_4. The second term in (4-3) can be defined as the duty-cycle loss. This term is common to all converters that rely on the energy stored in the resonant inductor to achieve ZVS operation for the lagging switches [38].

Fig. 5-12 shows the normalized output voltage gain as a function of the normalized output current, using the DC duty cycle as a running parameter. In this graph it is possible to determine the boundary between DCM and CCM operation of the output inductor L_{out}. The normalized variables used to plot the curves in Fig. 5-12 are defined as follows:

$$\begin{aligned} M_{out} &= \frac{n V_o}{V_{bus}} \\ I_{on} &= I_o \frac{n L_{out} f_s}{V_{bus}}. \end{aligned} \tag{4-4}$$

The effect of the duty-cycle loss can be observed in this graph during CCM operation. As can be seen, the gain of the converter decreases as the normalized output current increases. It is important to mention that for this graph, the ratio between output and leakage inductances is

defined as n^2L_{out}/L_{lk} and is equal to 10. By changing this parameter, the boundary between DCM and CCM can be controlled.

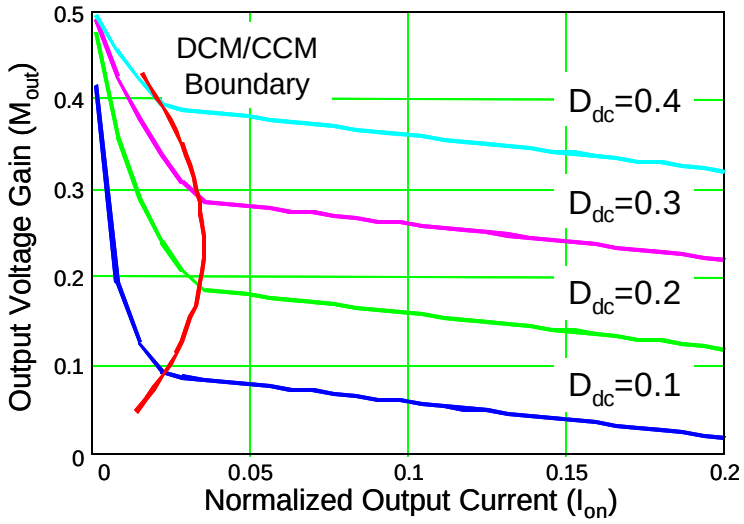


Fig. 5-12. Normalized output voltage gain as a function of the normalized output current, using the duty cycle as a running parameter.

5.3.2. Soft-Switching Implementation

In order to improve the efficiency in the quasi-integrated AC/DC dual-bridge converter, it is necessary that the power switches in the converter operate with some kind of soft-switching technique. This section describes the possibilities for and the benefits of the implementation of these soft-switching techniques.

A. Soft-Switching Operation for S_2 and S_3:

Zero-Current Transition (ZCT): As previously mentioned, switches S_2 and S_3 suffer higher current stress, since they must conduct the discontinuous currents of the input side as well as the current from the DC/DC converter. In addition, these switches have high turn-off losses because of the high peak current at the instant of the commutation. In order to minimize this problem, a modification to the previously proposed ZCT circuit [93] is implemented in this converter. The

main difference between this and the other proposed technique [93] is that because of the discontinuity of the input current during the turn-on of S_2 or S_3, it is not necessary to turn on the auxiliary switch before S_2 or S_3 is turned on. Therefore, a simplification of the control is achieved. Figs. 5-13 and 5-14 show the proposed converter with the auxiliary ZCT circuit.

B. Soft-Switching Operation for S_1 and S_4:

ZVS: In the proposed converter, ZVS operation for switches S_1 and S_4 is achieved during the intervals $[t_1^- - t_2]$ and $[t_5^- - t_6]$ without adding an auxiliary circuit. This can be explained as follows. When S_4 is turned off, the energy stored in the leakage inductances of the transformer charges the parasitic capacitance of S_4 and D_6 and discharges the parasitic capacitance of S_1 and D_7. When the parasitic capacitance of S_1 is completely discharged, the anti-parallel diode of S_1 starts to conduct. At this instant, S_1 can be turned on with ZVS. Fig. 5-13 also shows the proposed converter with ZVS operation for S_1 and S_4.

ZCS: As mentioned before, the duty cycle of the DC/DC converter is restricted by the duty cycle of the PFC stage. In addition, the ZVS range for switches S_1 and S_4 relies on the energy stored in the leakage inductance of the transformer. Therefore, these constraints penalize the converter with circulating energy in the primary side and duty-cycle loss. In order to overcome this problem, the possibility of using a ZCS technique instead of ZVS operation for switches S_1 and S_4 is evaluated. In this way, the circulating energy during the freewheeling stage is reduced. Fig. 5-14 shows the proposed converter with a passive auxiliary circuit in the secondary side [50], also discussed in this dissertation, to achieve ZCS operation for S_1 and S_4.

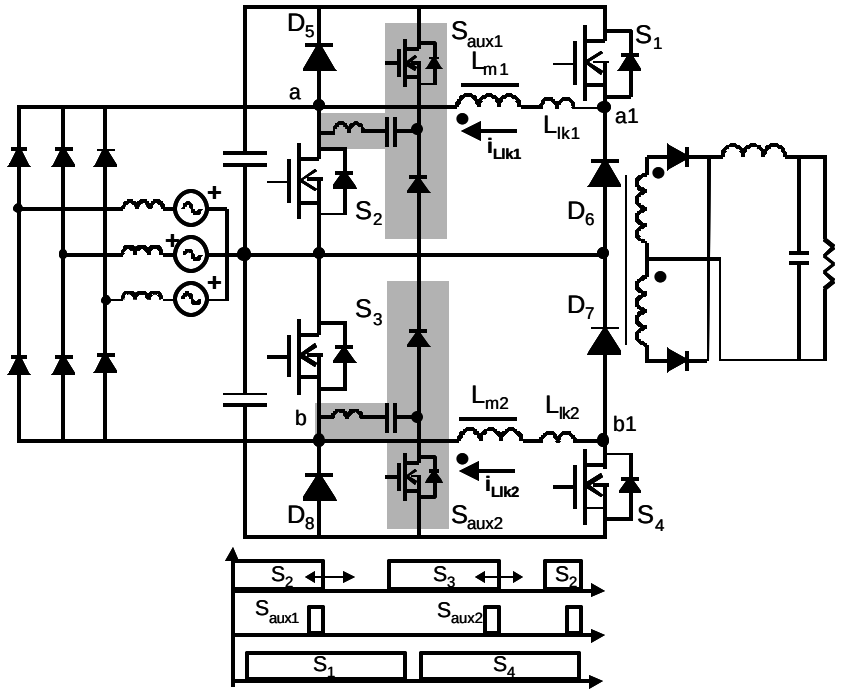


Fig. 5-13. Implementation of the quasi-integrated AC/DC three-phase dual-bridge converter with a soft-switching scheme: ZCT for S_2 and S_3 and ZVS for S_1 and S_4

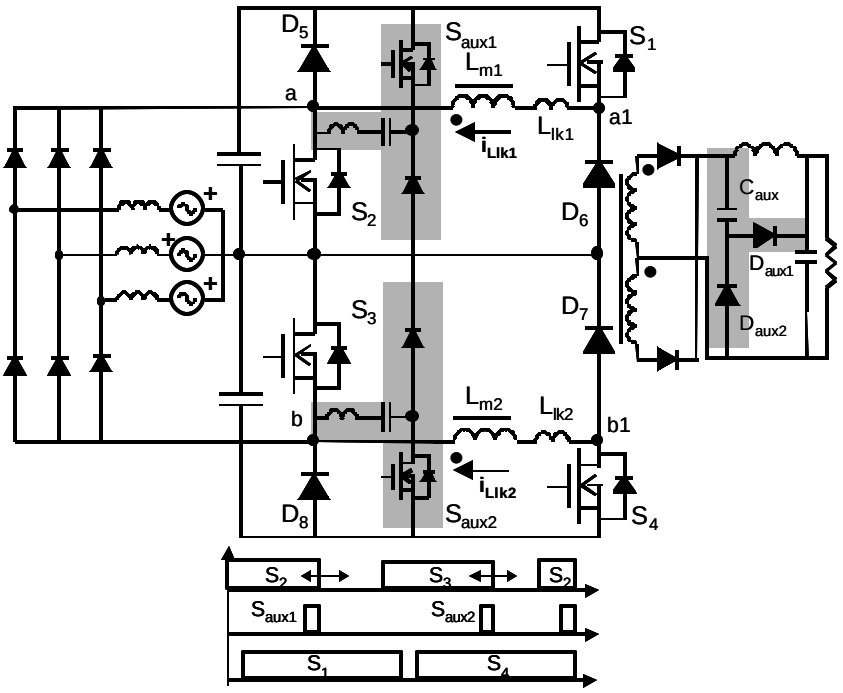


Fig. 5-14. Implementation of the quasi-integrated AC/DC three-phase dual-bridge converter with a soft-switching scheme: ZCT for S_2 and S_3 and ZCS for S_1 and S_4.

5.3.3. Experimental Results

An experimental prototype was built in order to verify the operation of the proposed quasi-integrated AC/DC three-phase dual-bridge converter. In order to both reduce the circulating energy during the freewheeling stage and to reduce the turn-off losses for switches S_1 and S_4, an auxiliary lossless passive circuit was placed in the secondary side. The specifications for the prototype are as follows: V_{out} = 42-57 V, P_{out} = 3 kW, V_{ac} = 170 – 260V, and f_s = 50 kHz.

The power stage shown in Fig. 5-8 consists of the following components.

$S_1 – S_4$: APT60M75JVR

$D_{r1} – D_{r2}$: HFA140MD60C

$D_5 – D_8$: DSEP 30-12A

C_{in1}, C_{in2}: 3x1000µF/250V connected in series

C_1-C_3: 2µF- polypropylene

T_r: E65 – 3C85 12/3/3

L_{out}: EC55-3C85, 6µH

C_{out}: 2x4700µF/100V – electrolytic

D_{aux1}-D_{aux2}: IXYSDSE160-05A

C_{aux}: 4x.068µF/400-polypropylene

The value for the boost inductance was obtained from Fig. 5-11. For this design, the intermediate bus voltage was chosen to be 800 V, which results in a boost inductance of 108 µH.

Experimental results for the proposed converter at 3 kW are shown in Figs. 5-15, 5-16, 5-17 and 5-18. Fig. 5-15 shows the measured filtered input current and the input phase voltage at 220 V and full-load condition. Fig. 5-16 presents the THD of the input currents as a function of the input phase voltage variations. As can be seen, THD for all cases is always lower than 12%. In order to reduce the distortion at 260V input voltage, either the intermediate bus voltage must be increased or harmonic injection techniques can be used. These approaches could be applied in

the future to the proposed converter in order to reduce the THD. This figure also shows the THD for the ZVS three-level AC/DC three-phase converter, which in the figure is called a single-stage, and the two-stage approach, which was also presented in the beginning of this chapter. As can be seen, the single-stage approach achieves the lowest THD among all compared topologies.

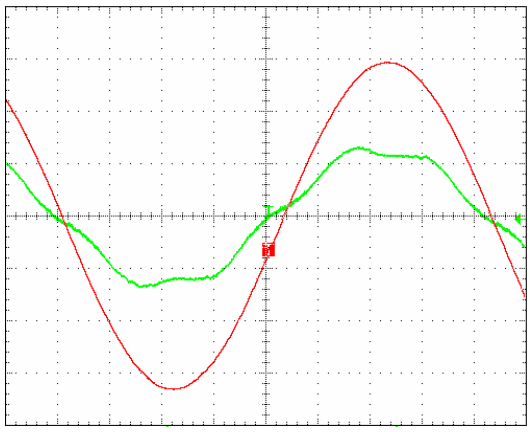


Fig. 5-15. Input voltage and filtered input current (100 V/div, 5 A/div 2ms/div).

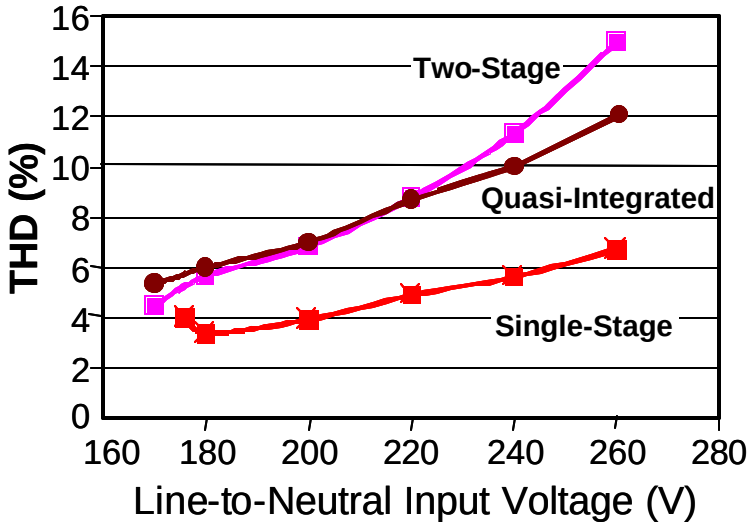


Fig. 5-16. THD generated by the proposed quasi-integrated AC/DC three-phase dual-bridge converter.

Fig. 5-17 shows the voltage (upper trace) and the current (lower trace) in one of the primary sides of the transformer, and the voltage V_s (middle trace) in the secondary side. It can be seen that the primary current is reset to zero after the end of the stage that transfers power to the

output. Therefore, a reduction of the circulating energy and ZCS operation for S_1 and S_4 are achieved. In addition, due to ZCS instead of ZVS operation for S_1 and S_4, the leakage inductance of the transformer does not have to be increased. Therefore, the parasitic ringing in the secondary side can be reduced.

Fig. 5-17. Voltage (upper trace) and current (lower trace) waveforms in the primary side of the transformer, and voltage across the secondary side (middle trace) (250 V/div, 100 V/div, 10 A/div, 5μs/div).

Fig. 5-18 shows the efficiency of the converter as a function of the variations of the input phase voltage at full-load conditions. It is important to mention that this efficiency measurement also considered the losses in the input filter. Although the efficiency of the proposed converter can be considered good for a quasi-integrated converter, it could be improved if IGBT devices were used for S_2 and S_3; in that case, a ZCT auxiliary circuit would have to be added to the converter to reduce the turn-off losses for these switches, as shown in Fig. 5-13(b). In addition, a further analysis of the design of the transformer must be carried out in order to reduce the circulating energy that exists between the two primary windings during the freewheeling stage. In this figure, the efficiency is also compared with the two-stage and the single-approach. As can be seen, the quasi-integrated converter presents a good tradeoff between simplicity and performance.

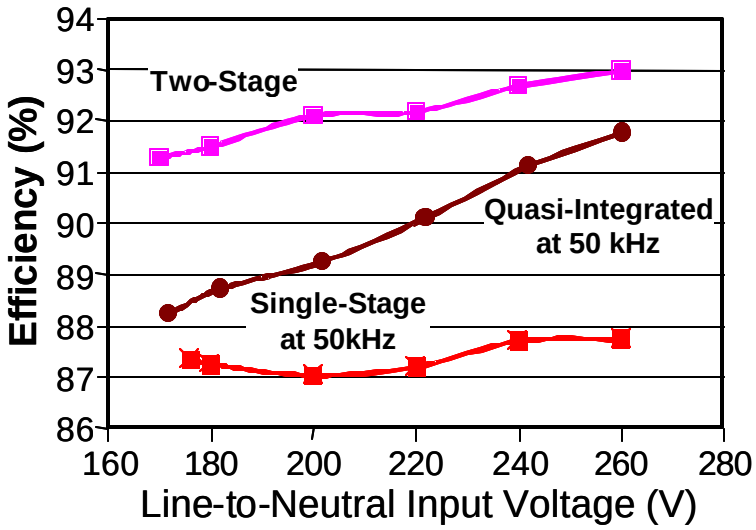


Fig. 5-18. Measured efficiency of the quasi-integrated AC/DC three-phase dual-bridge converter.

5.4. Conclusion

A novel quasi-integrated AC/DC three-phase dual-bridge converter was presented in this chapter. The operating stages and characteristics of the proposed converter were presented. Experimental results from a 3kW prototype were shown in order to demonstrate the operation of the converter.

From the results presented in this chapter, it is possible to determine that the proposed converter improves the complexity / low-efficiency tradeoff characteristics over both the two-stage approach and the integrated ZVS three-level AC/DC three-phase converter.

It was shown that by integrating two three-level converters with similar cells, the conduction losses in the devices could be reduced. In addition, the voltage stress across the main switches is reduced to half the level of the intermediate bus voltage. This allows the use of low-voltage-rating devices, which offer better electrical characteristics.

Although the proposed quasi-integrated converter presents a low THD, it is advisable to use harmonic injection techniques to maintain the THD at a level below 10% over the entire input-voltage range.

In addition, it was shown that soft-switching techniques are easy to implement for the main switches. From these techniques, ZCS instead of ZVS operation for the switches S_1 and S_4 is highly recommended. By using a passive auxiliary circuit in the secondary side, it is possible to reduce the circulating energy that exists during the freewheeling stage. Therefore, the limitation for the duty cycle in the DC/DC stage imposed by the PFC stage is minimized. For this case, it is important to study the effect of the coupling between the primary windings in order to further reduce the circulating energy that exists between them during the freewheeling stage. Furthermore, in order to further improve efficiency, it is recommended that switches S_1 and S_2, which handle the AC and DC current, be replaced by IGBT devices, and that the ZCT technique proposed in this chapter be used to alleviate the turn-off losses in these devices.

6. General Conclusion

In the traditional front-end converter based on the two-stage approach for high-power three-phase DPSs, the DC-link voltage coming from the PFC converter imposes an extra requirement for the second stage, i.e., for the DC/DC converter.

As was shown in Chapter 1, the high voltage in the DC link penalizes (in terms of efficiency and power density) the use of the traditional full-bridge DC/DC converter as a second stage. To minimize this problem, approaches such as the series connection of converters and converters that use structures that reduce the voltage stress across the main devices were discussed.

In order to improve the characteristics of these solutions, this dissertation proposed the development of high-efficiency, high-density DC/DC converters for high-power high-voltage applications.

Chapter 2, a novel ZVS DC/DC converter, based on a three-level structure, was introduced. This converter reduces the voltage stresses across the main switches to half the level of the input voltage. Therefore, devices with lower voltage ratings, which present better characteristics, can be used. Besides, the addition of a flying capacitor in the primary side allows ZVS operation for all switches with phase-shift control. It was shown that this new control scheme not only simplifies the modulation scheme for the three-level DC/DC converter, but also helps to balance the voltage across the DC input capacitor under an abnormal operation, such as when there is a gate-signal mismatch. Experimental results from a 6kW prototype were shown in order to demonstrate the operation of the converter.

Chapter 3 discussed improvements of the proposed ZVS three-level DC/DC converter. The operation with phase-shift control allows ZVS and ZVZCS techniques, previously developed for full-bridge converters, to be implemented in the proposed topology without modifications. In the case of the ZVS techniques, the converter's ZVS range increases while minimizing the circulating energy, the duty cycle loss and the secondary parasitic ringing. It is important to mention that these problems are common to all DC/DC converters in which the ZVS operation relies on the energy stored in either an external resonant inductance or the leakage inductance of the transformer.

A main contribution of this chapter is the evaluation of the benefits obtained by implementing ZVZCS techniques in the proposed three-level DC/DC converter. The chapter presented the analysis, implementation and comparison of three ZVZCS approaches using an active and passive auxiliary circuit in the secondary side and a passive circuit in the primary side. This resulted in novel ZVZCS three-level DC/DC converters for high-voltage applications. In all cases, experimental results from 6kW prototypes operating at 100 kHz were shown in order to demonstrate the operation of the converters. One of the main advantages of these converters is the reduction of the circulating energy that is common in PWM converters for applications in which hold-up time is a requirement. For these applications the traditional PWM converter should be designed with wide input voltage, thus penalizing the efficiency at normal operating conditions.

In the introduction of this dissertation, it was shown that the use of three-level structures offers an opportunity for operation at higher switching frequencies in high-power DPS applications. This is supported by the fact that the new generation of devices of up to 600 V presents a great

improvement in terms of switching characteristics. In order to take advantage of these new devices, Chapter 4 systematically explores soft-switching techniques and modulation strategies for resonant converters in order to determine the approach that best fulfills specifications related to future telecommunications power supplies, such as high efficiency and high power density.

From this analysis, it was concluded that the performance of the traditional series resonant DC/DC converter is highly penalized in applications in which wide input-voltage and load variations are required. To minimize the drawbacks of the resonant converter under these design specifications, a novel ZVS three-level LLC resonant DC/DC converter was proposed. The operating stages and characteristics of the proposed converter under fixed and variable switching frequencies were presented. It was shown that in both operating modes, the proposed converter could operate with a wide ZVS range by using the magnetizing inductance of the transformer. For the fixed-frequency operating mode, the control was performed in the secondary side of the transformer, which helped to increase the ZVS range and also reduced the circulating energy in the converter. In addition, this chapter presented some solutions for reducing the impact of the wide input-voltage variations, which also help to reduce the circulating energy in the converter and improves the efficiency at nominal operating conditions. These characteristics make the proposed converter an interesting option for high-voltage, high-power applications that require high power density and high efficiency. Experimental results for a 2.75kW prototype switching at 745 kHz were shown in order to verify the operation of the converter.

The main contribution from previous chapters was the proposal of three-level converters that can be used as a second stage in the front-end converter for high-power DPS applications. As discussed, the combination of this converter with a three-phase PFC converter such as the

VIENNA rectifier, or even simpler approaches such as the single-switch or two-switch boost rectifier working in DCM, helps to reduce the complexity and cost. With the goal to further simplify the overall system, Chapter 5 proposed a novel quasi-integrated AC/DC three-phase dual-bridge converter. This chapter started with a brief discussion of the previous integrated converter based on structures that reduce the voltage stress across the main devices. It was highlighted that the fluctuation in the intermediate DC-link voltage still penalizes the performance of these integrated converters. From the results presented in this chapter, it is possible to determine that the proposed converter improves the complexity / low-efficiency tradeoff characteristics over both the two-stage approach and the integrated ZVS three-level AC/DC three-phase converter. It was shown that by integrating two three-level converters that present similar cells, the conduction losses in the devices could be reduced. In addition, the voltage stress across the main switches is reduced to half the level of the intermediate bus voltage. This allows the use of low-voltage-rating devices, which present better electrical characteristics.

The operating stages and characteristics of the proposed converter were presented. Experimental results from a 3kW prototype were shown in order to demonstrate the operation of the converter. Although the proposed quasi-integrated converter achieves a low THD, it is recommended that harmonic injection techniques be used to maintain the THD at level below 10% over the entire input-voltage range. In addition, it was shown that soft-switching techniques are easy to implement for the main switches, and that ZCS operation for the DC/DC switches is highly recommended. By using a passive auxiliary circuit in the secondary side, it is possible to reduce the circulating energy that exists during the freewheeling stage. Therefore, the limitation for the duty cycle in the DC/DC stage imposed by the PFC stage is minimized. Furthermore, in

order to further improve efficiency, it is recommended that switches S_1 and S_2, which handle the AC and DC current, be replaced by IGBT devices, and that the ZCT technique proposed in this chapter be used to alleviate the turn-off losses in these devices.

It is important to mention that the research developed in this dissertation has resulted in one U. S. Patent [94] and one invention disclosure [110].

In addition, the results presented in this work have been used as a clear method for improving the characteristics of DC/DC converters in high-voltage applications. As an example, several authors have adopted the idea of combining three-level structures with phase-shift control and ZVS and ZVZCS soft-switching techniques for front-end converters for high-power three-phase DPS applications [115]-[123].

References

DPS – PFC

[1] IEC 61000-3-2, "Electromagnetic Compatibility (EMC) – Part 3-2: Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16A per Phase)," Edition 1.2, 1998.

[2] IEC 61000-3-4, "Electromagnetic Compatibility (EMC) – Part 3-4: Limitation of Emission of Harmonic Current in Low-Voltage Power Supply Systems for Equipment with Rated Current Greater Than 16A," First Edition, 1998.

[3] T. Key and J. Lay, "IEEE and International Harmonic Standard Impact on Power Electronic Equipment Design," in *IEEE IECON Rec.*, 1998, pp. 430-436.

[4] D. Chapman, D. James and C. J. Tuck, "A High Density 48V 200A Rectifier with Power Factor Correction," in *IEEE INTELEC,* 1993, pp. 188-125.

[5] G. Spiazzi and F. C. Lee, "Implementation of Single-Phase Boost Power-Factor-Correction Circuits in Three-Phase Applications," in *IEEE Transactions on Industrial Electronics*, Vol. 44, No. 3, pp. 365-371, June 1997.

[6] J. W. Kolar and H. Ertl, "Status of the Techniques of Three-Phase Rectifier Systems with Low Effect on the Mains," in IEEE INTELEC Rec., 1999, pp. 14-1.

[7] L. Malesani and P. Tomasin, "PWM Current Control Techniques of Voltage Source Converters – A Survey," in *IEEE IECON Rec.*, 1993, pp. 670-675.

[8] S. Chattopadhyay and V. Ramanarayanan, "Digital Implementation of a Line Current Shaping Algorithm for Three-Phase High Power Factor Boost Rectifier Without Input Voltage Sensing," in *IEEE APEC Rec.*, 2001, pp. 592-598.

[9] S. Fukuda and K. Koizumi, "Optimal Control of a Three Phase Boost Rectifier for Unity Power Factor and Reduced Harmonics," in *PEVD Rec.*, 1995, pp. 34-39.

[10] H. Mao, D. Boroyevich, A. Ravindra and F. C. Lee, "Analysis and Design of High Frequency Three-Phase Bosst Rectifier, in *IEEE APEC Rec.*, 1996, pp. 538-544.

[11] C. Cuadros, D. Boroyevich, S. Gataric, V. Vlatkovic, H. Mao and F. C. Lee, "Space Vector Modulated, Zero-Voltage Transition Three-Phase to DC Bidirectional Converter," in *IEEE PESC Rec.*, 1994, pp. 16-23.

[12] C. T. Cruz and I. Barbi, "A Passive Lossless Snubber for High Power Factor Unidirectional Three-Phase Three-Level Rectifier," in *IEEE IECON Rec.*, 1999, pp. 909-914.

[13] J.W. Kolar, H. Ertl and F.C. Zach, "Design and Experimental Investigation of a Three-Phase High-Power Density High Efficiency Unity Power Factor PWM (VIENNA) Rectifier Employing a Novel Integrated Power Semiconductor Module," in *IEEE APEC Rec.*, 1996, pp. 514-523.

[14] A. R. Prasad, P. Ziogas and S. Manias, "An Active Power Factor Correction Technique for Three-Phase Diode Rectifiers," in *IEEE PESC Rec.*, 1989, pp. 58-66.

[15] J.W. Kolar, H. Ertl and F.C. Zach, "Space Vector-Based Analytical Analysis of the Input Current Distortion of a Three-Phase Discontinuous-Mode Boost Rectifier System," in *IEEE PESC Rec.*, 1993, pp. 696-703.

[16] L. Simonetti, J. Sebastian and J. Uceda, "Single-Switch Three-Phase Power Factor Under Variable Switching Frequency and Discontinuous Input Current," in *IEEE PESC Rec.*, 1993, pp. 657-662.

[17] S. Gataric, D. Boroyevich and F. C. Lee, "Soft-Switched Single-Switch Three-Phase Rectifier with Power Factor Correction," in *IEEE APEC Rec.*, 1994, pp. 738-744.

[18] J.W. Kolar, H. Ertl and F.C. Zach, "A Comprehensive Design Approach for a Three-Phase High-Frequency Single-Switch Discontinuous-Mode Boost Power Factor Corrector Based on Analytically Derived Normalized Converter Component Ratings," in *IEEE Transactions on Industry Applications*, Vol. 31, No. 3, pp. 569-582, May/June 1995.

[19] P. M. Barbosa and F. C. Lee, "Design Aspects of Parallel Three-Phase DCM Boost Rectifiers," in *IEEE PESC Rec.*, 1999, pp. 331-336.

Three-Level DC/DC Converters

[20] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point Clamped PWM Inverter," *in IEEE Transactions on Industrial Applications*, Vol. IA-17, pp. 518-523, September/October 1981.

[21] T. Meynard and H. Foch, "Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters," in *IEEE PESC Rec.*, 1992, pp. 397-403.

[22] J. R. Pinheiro and I. Barbi, "The Three-Level ZVS PWM Converter: A New Concept in High-Voltage DC-to-DC Conversion," in *IEEE IECON Rec.*, 1992, pp. 173-178.

[23] J. R. Pinheiro and I. Barbi, "Wide Load Range Three-Level ZVS-PWM DC-to-DC Converter," in *IEEE PESC Rec.*, 1993, pp. 171-177.

[24] E. Deschamps and I. Barbi, "A Flying-Capacitor ZVS PWM 1.5 kW DC-to-DC Converter with Half of the Input Voltage Across the Switches," in *IEEE Transactions on Power Electronics*, Vol. 15, No. 5, pp. 855-860, September 2000.

[25] I. Barbi, R. Gules, R. Redl and N. O. Sokal, "DC/DC Converter For High Input Voltage: Four Switches with Peak Voltage of Vin/2, Capacitive Turn-Off Snubbing, and Zero-Voltage Turn–On," in *IEEE PESC Rec.*, 1998, pp. 1-7.

[26] G. Baggione, G. Caramazza, G. Guglielmo, F. Monasteri and R. Scibilia, "Two New High-Power-Density Power Plants for Telecommunication Systems," in *IEEE Rec.*, 1997, pp. 25-31.

[27] N. H. Kutkut, G. Luckjiff and D. M. Divan, "A Dual Bridge High Current DC-to-DC Converter With Soft Switching Capability," in *IEEE IAS Meet. Conf. Rec.*, 1997, pp. 1398-1405.

[28] N. Kutkut, "A New Dual-Bridge Soft Switching DC-to-DC Power Converter for High Power Applications," in *IEEE IECON Rec.*, 1999, pp. 474-479.

[29] R. Torrico and I. Barbi, "Dual-Bridge DC-DC Converter with Soft Switching Features," in *IEEE APEC Rec.*, 2001, pp.

[30] P. Maranesi, "The Switch in-Line Converter," in *IEEE PESC Rec.*, 1993, pp. 185-188.

[31] M. Legnani, P. Maranesi and G. Naummi, "SILC: A Novel Phase-Shifted PWM Converter," in *IEEE EPE Rec.*, 1993, pp. 1-4.

[32] M. Miller and A. Buffin, "A Versatile 48 V/60 V 100 A Rectifier for All Mains Inputs," in *IEEE INTELEC Rec.*, 1995, pp. 466-470.

[33] P. Prestifilippo, R. Scibilia, G. Baggione and G. Caramazza, "A Switched-Mode Three-Phase 200A/48V Rectifier with Input Unity Power Factor," in *IEEE INTELEC*, 1996, pp. 543-547.

[34] Y. S. Sun, S. H. Woo, C. H. Kang, J. S. Yoo, J.J. Lee and H. J. Kim "A Development of the Large Capacity Telecommunications Rectifier System using Series-Resonant Technology and Half-Bridge Topology," in *IEEE INTELEC* 1999, pp. 13-2.

ZVS Techniques

[35] Z.D. Fang, D. Y. Chen and F. C. Lee, "Designing a High Frequency Snubberless FET Power Inverter," *in Proc. Of Powercom 11*, 1984, pp. 829-834.

[36] O. D. Patterson and D. M. Divan, "Pseudo-Resonant Full Bridge DC/DC Converter," *in IEEE PESC Rec*., 1987, pp. 424-430.

[37] L. H. Mweene, C. A. Wright and M. S. Schlecht, "A 1 kW, 500 kHz Front-End Converter for Distributed Power Supply System," *in IEEE APEC Rec.*, 1989, pp. 423-432.

[38] J. A. Sabaté, V. Vlatkovic, R. B. Ridley, F. C. Lee and B. H. Cho, "Design Consideration for High-Voltage, High-Power, Full-Bridge, Zero-Voltage-Switched PWM Converter," in *IEEE APEC Rec.*, 1990, pp. 275-284.

[39] R. Redl, N. O. Sokal and L. Balogh, "A Novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Consideration, and Experimental Results at 1.5 kW, 100 kHz," in IEEE PESC Rec., 1990, pp. 162-172.

[40] Hitchcock, et al., "Resonant Transition DC-to-DC Converter," U.S. Patent No. 5,132,899, July 1992.

[41] W. Chen, J. A. Sabate, M.M. Jovanoic and F. C. Lee, "A Comparative Study of Zero-Voltage-Switching Full Bridge PWM Converters," in *VPEC Seminar*, 1994, pp. 217-226.

[42] G. Hua, F. C. Lee and M.M. Jovanovic, "An Improved Full-Bridge Zero-Voltage-Switched PWM Converter Using a Saturable Inductor," *IEEE Transactions on Power Electronics*, Vol. 8, No. 4, pp. 530-534 October 1993.

[43] R. Watson and F. C. Lee, "Analysis, Design, and Experimental Results of a 1 KW ZVS-FB-PWM Converter Employing Magamp Secondary Side Control," in *IEEE Transactions*

on Industrial Electronics, Vol. 45, No. 5, pp. 806-814, October 1998. (Also presented in *IEEE APEC Rec.*, 1994, pp. 166-172.)

[44] M. Michihira, T. Funaki, K. Matsu-ura and M. Nakaoka, "A Novel Quasi-Resonant DC/DC Converter Using Phase-Shift in the Secondary Side of High-Frequency Transformer," in *IEEE PESC Rec.*, 1996, pp. 670-675.

[45] B. Kwon, J. Kim and G. Jeong, "Full-Bridge Soft Switching PWM Converter with Saturable Inductors at the Secondary Side," in *IEE Proceedings – Electronics Power Applications*, Vol. 146, No. 1 pp. 117-122, January 1999.

[46] R. Ayyanar and N. Mohan, "A Novel Full-Bridge DC-DC Converter for Battery Charging Using Secondary-Side Control Combines Soft Switching Over the Full Load Range and Low Magnetics Requirement," in *IEEE Transactions on Industry Applications*, Vol. 37, No. 2, pp. 559-565, March/April 2001.

ZVZCS Techniques

[47] S. Hamada, M. Michihira and M. Nakaoka, "Using a Tapped Inductor for Reducing Conduction Losses in a Soft-Switching PWM DC-DC Converter," in *EPE Conf. Rec.*, 1993, Vol. 3, pp. 130–134.

[48] J. G. Cho, J. A. Sabate, G. Hua and F. C. Lee, "Zero-Voltage and Zero-Current-Switching Full-Bridge PWM Converter for High Power Applications," in *IEEE PESC Rec.*, 1994, pp. 102-108.

[49] J. G. Cho, C. Y. Jeong and F. C. Lee, "Zero-Voltage and Zero-Current-Switching Full-Bridge Converter Using Secondary Active Clamp," *IEEE Transactions on Power Electronics*, Vol. 13, No. 4, pp. 601-607, July 1998.

[50] J. G. Cho, J. W. Baek, C. Y. Jeong and G. H. Rim, "Novel Zero-Voltage and Zero-Current-Switching Full-Bridge PWM Converter Using a Simple Auxiliary Circuit," *IEEE Transactions on Industry Applications*, Vol. 35, No. 1, pp. 15-20, January/February 1999.

[51] E. Kim, K. Joe, M. Kye, Y. Kim and B. Yoon, "An Improved Soft-Switching PWM FB DC/DC Converter for Reducing Conduction Losses," *IEEE Transactions on Power Electronics*, Vol. 14, No. 2, pp. 258-264, March 1999.

[52] J.G. Cho, J.W. Baek, D.W. Yoo, C.Y. Jeong, H.S. Lee and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching Full Bridge PWM Converter Using Transformer Auxiliary Winding," in *IEEE PESC Rec.*, 1997, pp. 227-232.

[53] K. Wang, F. C. Lee and D. Boroyevich, "A Family of Quasi-Single-Stage Isolated Three-Phase ZVZCS Buck PWM Rectifiers," *VPEC Seminar*, 1997, pp. 83-88.

[54] J.W. Baek, C.Y. Jeong, J.G. Cho, D.W. Yoo, H.S. Lee and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching Full Bridge PWM Converter with Low Output Current Ripple," in *IEEE INTELLEC*, 1997, pp. 257-262.

[55] J.G. Cho, J.W. Baek, C.Y. Jeong, D.W. Yoo, H.S. Lee and G.H. Rim, "Novel Zero-Voltage and Zero-Current Switching Full Bridge PWM Converter Using A Simple Auxiliary Circuit," in *IEEE APEC Conf.*, 1998, pp. 834-839.

[56] E.S. Kim, K.Y. Joe and S.G. Park, "An Improved Soft Switching PWM FB DC/DC Converter Using the Modified Energy Recovery Snubber," in *IEEE APEC Conf.*, 2000, pp. 119-124.

[57] H. Choi, J. Kim, J. Lee and B. Cho, "Modeling, Analysis and Design of 10kW Parallel Module Zero-Voltage Zero-Current-Switched Full-Bridge PWM Converter," in *IEEE APEC Conf.*, 2000, pp.

[58] H. Choi, J. Kim and B. Cho, "Novel Zero-Voltage and Zero-Current-Switching (ZVZCS) Full-Bridge PWM Converter Using Coupled Output Inductor," in *IEEE APEC Conf.*, 2001, pp. 967-973.

[59] S.J. Jeon and G.H. Cho, "Zero-Voltage and Zero-Current Switching Full Bridge DC-DC Converter for Arc Welding Machines," in *IEE Electronics Letters*, Vol. 35, No. 13, pp. 1043-1044, 1999.

[60] S.J. Jeon and G.H. Cho, "Zero-Voltage and Zero-Current Switching Full Bridge DC-DC Converter with Transformer Isolation," in *IEEE Trans. on Power Electronics*, Vol. 16, No. 5, pp. 573-580, September 2001.

High-Density DC/DC Converter

[61] I. Pitel, "Phase-Modulated Resonant Conversion Techniques for High-Frequency Link Inverters," in *IEEE IAS Rec.*, 1985, pp. 1163-1172.

[62] F. S. Tsai, P. Materu and F. C. Lee, "Constant-Frequency Clamped-Mode Resonant Converters," in *IEEE Trans. on Power Electronics*, Vol. 3, pp. 460-473, Oct. 1988.

[63] P. K. Jain, A. St-Martin and G. Edwards, "Asymmetrical Pulse-Width-Modulated Resonant DC/DC Converter Topologies," in *IEEE Trans. on Power Electronics*, Vol. 11, pp. 413-422, May 1996.

[64] R. Oruganti, P. C. Heng, J. T. K. Guan and L. A. Choy, "Soft-Switched DC/DC Converter with PWM Control," in *IEEE Trans. on Power Electronics*, Vol. 13, pp. 102-114, Jan. 1998.

[65] F. Monterde, J. M. Burdío P. Hernández and J. R. García, "Unipolar Voltage-Cancellation Control of Resonant Inverters for Induction Cooking Appliances," in *IEEE IECON Rec.*, 1998, pp. 820-824.

[66] F. Monterde, P. Hernández, J. M. Burdío, J. R. García and A. Martínez, "Comparison of Control Strategies for Series Resonant Full-Bridge Inverter for Induction Cookers," in *EPE Rec.*, 1999.

[67] R. Steigerwald, "A Comparison of Half-Bridge Resonant Converter Topologies," in *IEEE Trans. on Power Electronics*, Vol. 3, No. 2, April 1988, pp. 174- 182.

[68] R. Severns, "Topologies for Three Element Resonant Converters," *in IEEE APEC Rec*., 1990, pp. 712-722.

[69] I. Bataresh, "Resonant Converter Topologies with Three and Four Energy Storage Elements," *in IEEE Trans. on Power Electronics*, Vol. 9, No. 1, pp. 64-73, January 1994.

[70] T. Duerbaum and G. Sauerlaender, "Analysis of the Series-Parallel Multiresonant LLC Converter – Comparison Between First Harmonic Approximation and Measurement," *in EPE Rec.*, 1997, pp. 2.174-2.179.

[71] J. F. Lazar and R. Martimelli, "Steady-State Analysis of LLC Series Resonant Converter," *in IEEE APEC Rec.*, 2001, pp. 728-735.

[72] B. Yang, F. C. Lee R. Chen, A. J. Zhang and G. Huang, "LLC Resonant Converter for Front-End DC/DC Converter," *in CPES Seminar Rec.*, 2001, pp. 44-48.

[73] B. S. Jacobson and R. A. DiPerna, "Series Resonant Converter with Clamped Tank Capacitor Voltage," in *IEEE APEC Rec*., 1990, pp. 137-146.

[74] R. Steigerwald, W. Roshen and C. Saj, "A High-Density 1 kW Resonant Power Converter with Transient Boost Function," in *IEEE Trans. on Power Electronics*, Vol. 8, No. 4, pp. 431-438, October 1993.

[75] J. Sabaté and F. Lee, "Off-Line Applications of the Fixed-Frequency Clamped-Mode Series Resonant Converter," in *IEEE Trans. on Power Electronics*, Vol. 6, No. 1, pp. 39-47, January 1991.

[76] J. Sabaté, R. Farrington, M. Jovanovic and F. Lee, "Effect of Switch Capacitance on Zero-Voltage Switching of Resonant Converters," in *IEEE PESC Rec.*, 1993, pp. 213-220.

[77] A. K. S Bhat, "Analysis and Design of LCL-Type Series Resonant Converter," in *IEEE Trans. on Industrial Electronics*, Vol. 41, No. 1, pp. 118 – 124, February 1994.

[78] J. Burdio, F. Canales, P. Barbosa and F. Lee, "Comparison of Fixed-Frequency Control Strategies for ZVS DC/DC Series Resonant Converters," in *CPES Seminar*, 2000, pp. 182-187.

[79] W. Tabiz and F. Lee, "Zero-Voltage Switching Multi-Resonant Technique – A Novel Approach to Improve Performance of High-Frequency Quasi-Resonant Converters," in *IEEE PESC Rec.*, 1988, pp. 9-17.

[80] M. Jovanovic, C. Leu and F. Lee, "A Full-Bridge Zero-Voltage-Switched Multi-Resonant Converter for Pulse-Load Applications," in *IEEE APEC Rec.*, 1990, pp. 109-118.

[81] M. Jovanovic, R. Farrington and F. Lee, "Constant-Frequency Multi-Resonant Converters," in *VPEC Seminar*, 1989, pp. 56-65.

[82] R. Farrington, M. Jovanovic and F. Lee, "Constant-Frequency Zero-Voltage-Switched Multi-Resonant Converters: Analysis, Design, and Experimental Results," in *IEEE PESC Rec.*, 1990, pp. 197-205.

[83] M. A. de Rooij, J. D. van Wyk, "Design Procedure for a Minimum Volume Low-Loss Integrated LCT Structure for 2.7 kW Series Load Resonant DC to DC Converter," CPES, Internal Report, July 2001.

[84] P. Wong, B. Yang, P. Xu and F. Lee, "Quasi-Square-Wave Rectification for Front-End DC/DC Converters," in *IEEE PESC Rec.*, 2000, pp. 1053-1057.

[85] P. Xu, Q. Wu, P. Wong and F. Lee, "A Novel Integrated Current Doubler Rectifier," in *IEEE APEC Rec.*, 2000, pp. 735-740.

Integrated Converters

[86] R. Itoh and K. Ishizaka, "Three-Phase Flyback AC/DC Converter with Sinusoidal Supply Currents," in *IEE Proceedings Part B*, Vol. 138, No. 3, pp. 143-151, May 1991.

[87] O. Apeldoorn and P. Schmidt, "Single Transistor Three Phase Power Conditioner with High Power Factor and Isolated Output," in *IEEE APEC Rec.*, 1994, pp. 731-737.

[88] E. Ismail and R. Erickson, "A Single Transistor Three Phase Resonant Switch for High Quality Rectification," in *IEEE PESC Rec.*, 1992, pp. 1341-1351.

[89] Y. Yang and R. Erickson, "New Single-Switch Three-Phase High-Power Factor Rectifier Using Multi-Resonant Zero Current Switching," in *IEEE APEC Rec.*, 1994, pp. 711-717.

[90] Y. Yang and R. Erickson, "Design and Experimental Results of a 6 KW Single-Switch Three-Phase High Power Factor Rectifier Using Multi-Resonant Zero Current Switching," in *IEEE APEC Rec.*, 1996, pp. 524-530.

[91] K. Schenk and S. Cuk, "A Simple Three-Phase Power Factor Corrector with Improved Harmonic Distortion," in *IEEE PESC Rec.*, 1997, pp. 399-405.

[92] J. Contreras and I. Barbi, "A Three-Phase High Power Factor PWM ZVS Power Supply with a Single Power Stage," in *IEEE PESC Rec*., 1994, pp. 356-362.

[93] H. Mao, F. Lee, X. Zhou and D. Boroyevich, "Improved Zero-Current-Transition PWM Converters for High Power Applications," in *IEEE IAS Rec., 1996*, pp. 1145-1152.

Publications Related to the Dissertation

[94] F. Canales, P. Barbosa and F. C. Lee, "A Zero Voltage and Zero Current Switching Three-Level DC/DC Converter," U. S. Patent No. 6, 344,044, February 19, 2002. Also, VTIP No 99.042.

[95] F. Canales, P. Barbosa and F. C. Lee **"**A Zero Voltage and Zero Current Switching Three-Level DC/DC Converter,**"** in *IEEE APEC Rec., 2000*, pp. 314-320.

[96] P. Barbosa, F. Canales, J. Burdio and F. C. Lee, **"**A Three-Level Isolated Power Factor Correction Circuit with Zero Voltage Switching," in *IEEE PESC Rec.*, 2000, pp. 347-352.

[97] P. Barbosa, F. Canales, L. Serpa and F. C. Lee, "Single-Stage Three-Phase AC-to-DC Front-End Converter for Distributed Power Systems," in *CPES Seminar Rec.*, 2002, pp. 16-24.

[98] J.C. Crebier, P. Barbosa, F. Canales, F. C. Lee and J. P. Ferrieux, "Frequency Domain Analysis and Evaluation of Differential Mode Input Current for Three-Phase DCM Boost Rectifiers with Different Control Strategies," in *IEEE PESC Rec.*, 2000, pp. 482-487.

[99] F. Canales, P. Barbosa and F. C. Lee, **"**A Zero Voltage Switching Three-Level DC/DC Converter,**"** in *IEEE INTELEC Rec.*, 2000, pp. 512-517.

[100] F. Canales, P. Barbosa and F. C. Lee "A Zero Voltage and Zero Current Switching Three-Level DC/DC Converter Using a Lossless Passive Circuit," in *CPES Seminar*, 2000, pp. 372-377.

[101] P. Barbosa, F. Canales and F. C. Lee, **"**A Front-End Distributed Power System for High-Power Applications,**"** in *IEEE IAS Rec.*, 2000, pp.

[102] F. Canales, P. Barbosa, C. Aguilar, F. C. Lee and B. Jacobson "A Fixed-Frequency Zero-Voltage-Switching Three-Level DC/DC Resonant Converter," in *CPES Seminar*, 2001, pp. 155-160.

[103] J. Burdio, F. Canales, P. Barbosa and F. C. Lee, **"**A Comparison Study of Fixed-Frequency Control Strategies for ZVS DC/DC Series Resonant Converters**,"** in *IEEE PESC Rec.*, 2001, pp. 427-432.

[104] P. Barbosa, F. Canales and F. C. Lee, **"**Passive Input Ripple Cancellation in Three-Phase Discontinuous Conduction Mode Rectifiers,**"** in *IEEE PESC Rec.*, 2001, pp. 1019-1024.

[105] P. Barbosa, F. Canales and F. C. Lee, **"**Analysis and Evaluation of the Two-Switch Three-Level Boost Rectifier," in *IEEE PESC Rec.*, 2001, pp. 1659-1664.

[106] F. Canales, P. Barbosa, C. Aguilar and F. C. Lee, "A Quasi-Integrated AC/DC Three-Phase Dual-Bridge Converter," in *IEEE PESC Rec.*, 2001 pp. 1893-1898.

[107] F. Lee, P. Barbosa, P. Xu, Z. Zhang, B. Yang and F. Canales, "Topologies and Design Considerations for Distributed Power System Applications," in *Proceedings of the IEEE*, Vol. 89, No. 6, pp. 939-950 June 2001.

[108] P. Barbosa, F. Canales, J. Crebier and F. C. Lee, "Interleaved Three-Phase Boost Rectifiers Operated in the Discontinuous Conduction Mode: Analysis, Design Considerations and Experimentation," in *IEEE Trans. on Power Electronics*, Vol. 16, No. 5, pp 724-734, September 2001.

[109] S. J. Jeon, F. Canales, P. Barbosa and F. C. Lee, "A Primary-Side-Assisted Zero-Voltage and Zero-Current Switching Three-Level DC/DC Converter," in *IEEE ICPE Rec.*, 2001, pp. 227-231.

[110] F. Canales, P. Barbosa and F. C. Lee, "A Fixed-Frequency Zero-Voltage-Switching Three-Level DC/DC Resonant Converter," VTIP No. 01.112.

[111] P. Barbosa, F. Canales, S-J. Jeon and F. C. Lee, "Three-Level Front-End Converter for Distributed Power Systems," *in EPE-PEMC Rec.*, 2002.

[112] F. Canales, P. Barbosa and F.C. Lee, "A Wide Input Voltage and Load Output Variations Fixed-Frequency ZVS DC/DC LLC Resonant Converter for High –Power Applications," in *IEEE IAS Rec.*, 2002, pp. 2306-2313.

[113] F. Canales, P. Barbosa and F. C. Lee, "A Zero-Voltage and Zero-Current Switching Three-Level DC/DC Converter," in *IEEE Trans. on Power Electronics*, Vol. 17, No. 6, pp. 898-904, November 2002.

[114] F. Canales, P. Barbosa, C. Aguilar and F.C. Lee, "A High-Power-Density DC/DC Converter for High-Power Distributed Power System," in *IEEE PESC Rec.*, 2003, pp. 11-18.

Papers Using the Publications Related to the Dissertation as a Reference

[115] Y. Cho, Y. Kim and E. Kim, "Three Level DC/DC Converter Using Energy Recovery Snubber," in *The Transactions of the Korean Institute of Power Electronics*, Vol. 6, No. 1, pp. 64-73, February 2001.

[116] N. Fröhleke and M. Schniedermann, "Enhanced Analysis and Design Issues of a 3-Level DC/DC Converter with Zero Voltage and Zero Current Switching," in *IEEE EPE*, 2001.

[117] X. Ruan, L. Zhou and Y. Yan, "A Novel Zero-Voltage and Zero-Current-Switching PWM Three-Level Converter," in *IEEE PESC Rec.*, 2001, pp. 1075-1079.

[118] X. Ruan, L. Zhou and Y. Yan, "Soft-Switching PWM Three-Level Converters," in *Transactions on Power Electronics*, Vol. 16, No. 5, pp. 612-622, September 2001. Also published in *IEEE IPEMC Rec.*, 2000, pp. 417-423.

[119] E. Kim, Y. Byun, Y. Kim and Y. Hong, "A Three Level ZVZCS Phase-Shifted DC/DC Converter Using a Tapped Inductor and A Snubber Capacitor," in *IEEE APEC Rec.*, 2001, pp. 980-985. Also published in *IEEE PCC Rec.*, 2002, pp. 115-121.

[120] X. Ruan, D. Xu and Y. Yan, "Zero-Voltage-Switching PWM Three-Level Converter with Two Clamp Diodes," in *IEEE PESC Rec.*, 2001, pp. 445-450.

[121] J. Rodriguez, J. Lai and F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls and Applications,' in IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, pp. 724-738, August 2002.

[122] Y. Jang and M. M. Jovanovic, "A New Three-Level Soft-Switched Converter," in *IEEE APEC Rec.*, 2003, pp.1059-1065.

[123] M. Chen, D. Xu, J. Lou and M. Luo, "Transformer Secondary Leakage Inductance Based ZVS Dual Bridge DC/DC Converter," in *IEEE APEC Rec.*, 2003, pp. 1082-1087.

[124] Y. Zhu and B. Lehman, "Three-Level Switch Cell for Low Voltage/High-Current DC-DC Converters," in *IEEE APEC Rec.*, 2003, pp. 121-125.

V i t a

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