CHAPTER I

Introduction

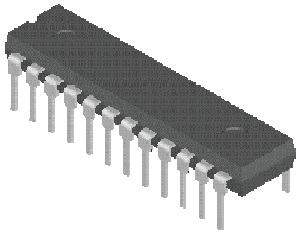
1.1 Overview of Power Electronics Packaging

Basically, power electronics packages provide mechanical support, device protection, cooling and electrical connection and isolation for power electronic components that make up a circuit. The overall performance of single chip power package, a multichip power module as well as a whole power system is not only determined by power devices and power electronics circuit, but also affected by packaging technology. Until recently, power-semiconductor suppliers have been concentrating on improving cell structures, cell densities, and process technologies to improve power device performances. This route has yielded substantial results, but further efforts in this area will provide diminishing returns, as the contribution by the package is roughly the same as that of the silicon. Monolithic integration of power electronics devices in the form of power ICs has not demonstrated its cost-effectiveness in general and is limited to very low-power applications. Over the last twenty years, industrial and research efforts on electronic power conversion are making the move toward high-frequency synthesis, which results in great improvement in converter performance, miniaturization in physical size and reduction of mass weight and cost. This is pushing the limits of existing packaging technology and thus it is packaging that is the dominant technology barrier currently limiting the rapid growth of power conversion applications.

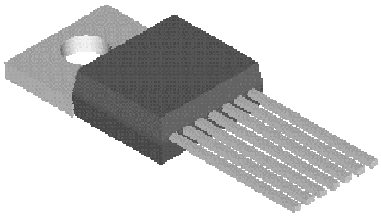
1.1.1 Evolution of Power Semiconductor Packaging

Power semiconductor device packages can basically be divided into two categories: through hole and surface mounted packages. For through-hole packages, Dual-In-Line Package (DIP), Transistor Outline Package (TO), and Pin Grid Array (PGA) are the most common available ones, while Small Outline Package (SO or SOP), Quad Flat pack (QFP), Small Outline Transistor (SOT), and Plastic Leaded Chip Carrier (PLCC) are the typical surface mount packages. Figure 1.1 and Figure 1.2 show the most common through-hole power packages and surface mount power packages, respectively. For each package type, there are still some variations, such as lead numbers, size, thickness, though the basic configuration is the same. For

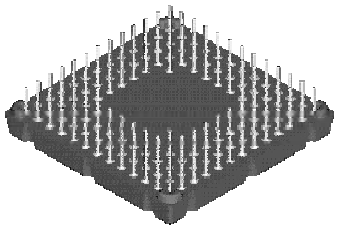
example, for TO package, there are TO-92, TO-202, TO-220, TO-226, TO-237; for SO package, there are SO-8, SO-6, SSOP, TSOP, TSSOP (Thin Shrink Small Outline Packages). The majority of those packages are JEDEC (Joint Electron Device Engineering Council) standard packages.



Dual-In-Line Package (DIP)

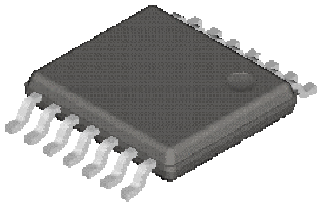


TO Packages

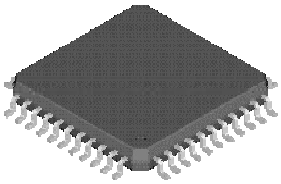


Pin Grid Array (PGA)

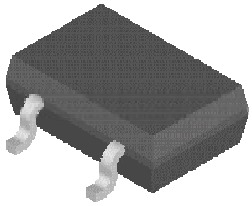
Figure 1.1. The most common through-hole power packages.



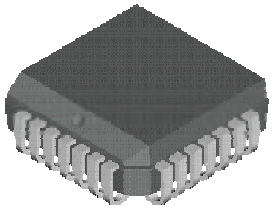
Small Outline Package (SO)



Quad Flat pack (QFP)



Small Outline Transistor (SOT)



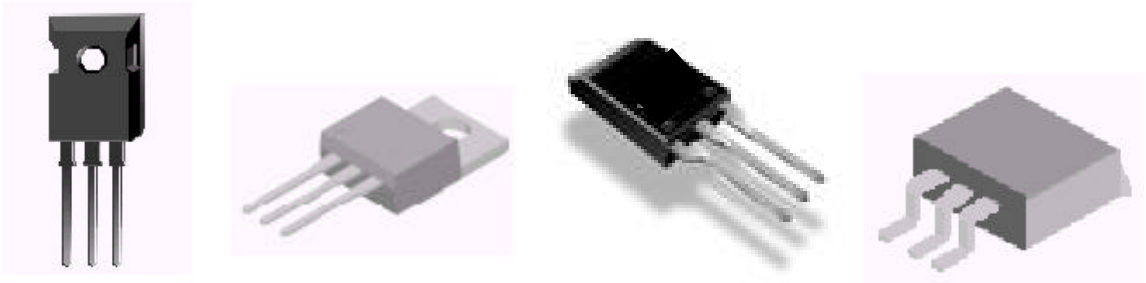
Plastic Leaded Chip Carrier (PLCC)

Figure 1.2. Typical surface mount power packages.

The trends towards miniaturization, resistance reduction and improved thermal performance are the main drivers for power semiconductor development. A good indication of power density is the silicon to footprint ratio. This is the ratio of silicon (die) in a package divided by the total footprint. Also, a performance measure of the power package can be expressed as a space figure of merit (FOM) which calculated as the device on-resistance ($R_{ds(on)}$ for MOSFET) x Footprint Area.

TO packages are the most widely used through-hole type packages. Figure 1.3 shows the TO package evolution. The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. It has isolated mounting hole. The size of TO-247 package is quite large. The TO-220 package is universally preferred for all

commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance, fairly small size and low package cost of the TO-220 contribute to its wide acceptance throughout the industry. Born from the need to accommodate ever increasing amounts of silicon in smaller, space saving packages, the SuperTO-247/SuperTO-220 allows the same die sizes that used to be put in a much larger package, such as TO-264. SuperTO-247/SuperTO-220 type package removes the traditional mounting hole and essentially extend the plastic up the tab of the device to allow for up to double the amount of silicon to be place in the same footprint area, essentially increasing the silicon to footprint ratio to figures around 30 percent from the midteens. This not only improves thermals due to the larger die capability, but also allows for a much higher power component to be used in the same footprint area. This type of package has increased current handling capability over the TO-247/TO-220 and even much larger packages. This package uses efficient and reliable clip mounting methods to attach to heatsinks. The industry effort for high current conversion over the past two decades has been the TO-263 or D^2Pak. This package, essentially a TO-220 modified for surface mount, is capable of accommodating large die sizes and is effective at transferring heat to substrate. It provides very high power capability and very low on-resistance. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. Unfortunately, the package is fairly large (155 sq. mm outline), and costly.



TO-247 TO-220 SuperTO-220/SuperTO-247 TO-263/ D^2Pak

Figure 1.3. TO power package evolution.

For surface mount packages, there have been several advances in the marketplace recently, and the traditional small outline integrated circuit (SOIC) SO-8 outline is probably where most of the development has taken place. SO-8 packages became a popular power MOSFET package about a decade ago. New silicon technology has enabled the SO-8 package to

deliver up to about 10 A in a typical application. It's widely available, space efficient and easy to handle. Unfortunately this package is not very thermally efficient, since most of its heat has to flow through the cross-sectional area of its drain leads to the substrate heat sink. Due to the demand of smaller device footprint, TSSOP (Thin Shrink Small Outline Package) was developed. The TSSOP-8 package has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the TSSOP-8 will allow it to fit easily into extremely thin application environments such as portable electronics. For better heat transfer, SOT-223 has been developed. The SOT-223 package is designed for surface mount. It has the advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25W is possible in a typical surface mount application. For lower power portable applications, the TSOP-6 and SOT-23 have provided the best power density solution for packaging power MOSFETs to date. Unfortunately, as plastic injected molded packages, most of them sacrifice size and can be up to three times the footprint of wafer level packaging solutions for the same electrical performance. Typical silicon to footprint values for these packages is in the high teens (~18 percent) for SOT-23 and low twenties (~22 percent) for TSOP-6.

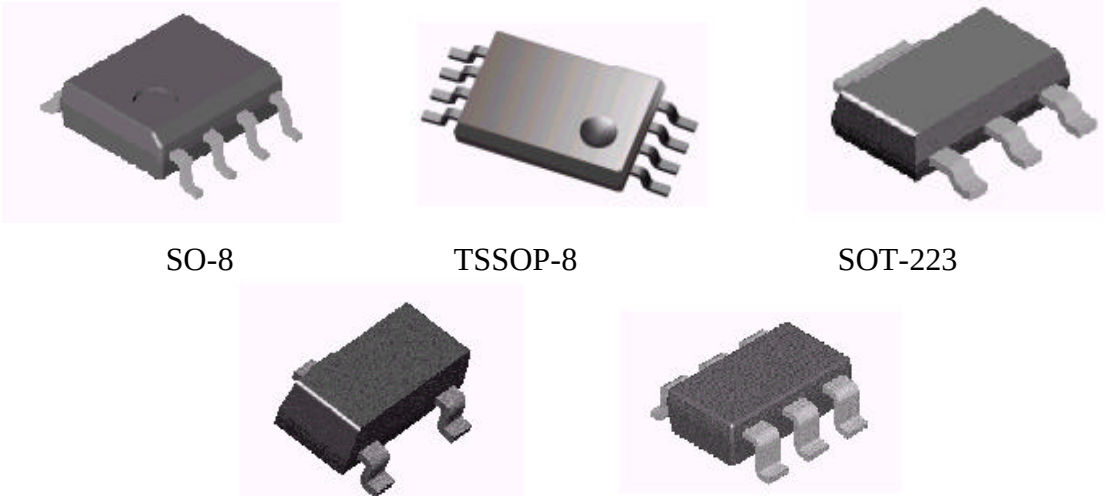


Figure 1.4. SO power package evolution.

Leadless packaging is a recent technology for power MOSFETs. This packaging approach occupies about half the board space required by a TSOP-6 for the same performance. Removing the leads from the sides of the package reduces the overall package footprint. Due to

the improved drain contact connection, this device improves the space figure of merit by approximately 44 percent versus the TSOP-6. The silicon to footprint for these devices is in the mid-50 percent range.

Area array packaging, such as ball grid array and solder bumped flip chip, is another step towards footprint reduction since the interconnections are located on the bottom of the package. Thus, with area array packages, the footprint is reduced to the outline of the package or even the silicon chip itself. The smallest footprint can be achieved is to have the solder balls placed, or bumped, directly onto the die. Flip chip packages have been introduced recently by several power semiconductor manufacturers. For example, as we will introduce in details later in this chapter, Fairchild took the flip chip route and developed BGA MOSFET package by encasing low-voltage MOSFET in a fine-pitch ball-grid array; a flip chip die device, introduced by International Rectifier, called FlipFET^{TM}, utilizes true chip scale packaging - the die is passivated and "bumped" to create the interconnections. FlipFET^{TM} achieved the ultimate goal of 100 percent silicon-to-footprint ratio. Power electronics packaging lab at CPES, Virginia Tech has developed metal post chip scale power package [1] and in this research we will introduce solder joint area array power packages which achieve 100 percent or near 100 percent silicon-to-footprint ratio. Figure 1.5 is a chart for the evolution of surface mount packages with respect to silicon to footprint ratio and their approximate time of introduction and Figure 1.6 shows figure of merit for different packages [2].

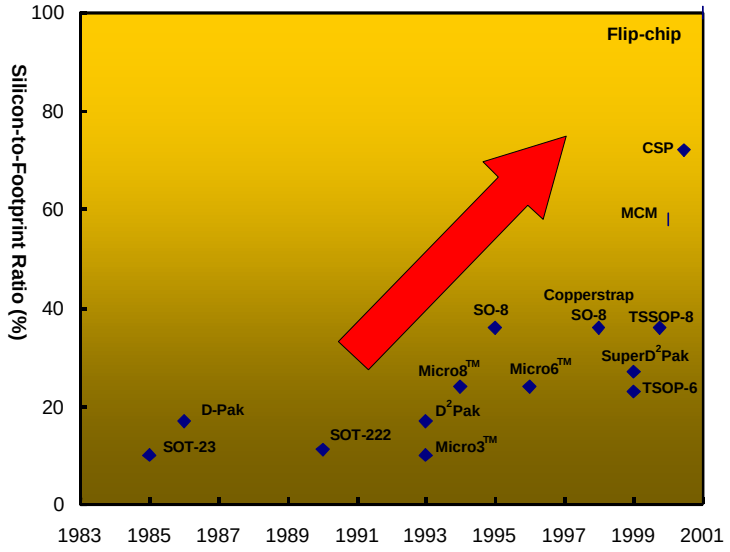


Figure 1.5. Evolution of power packages.

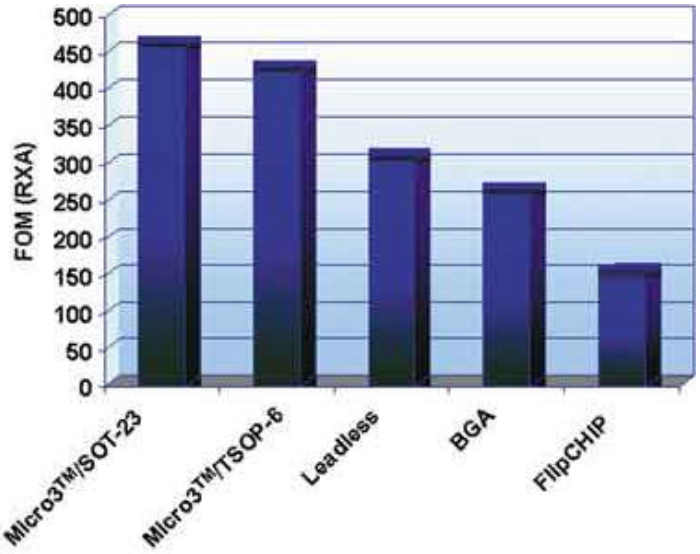


Figure 1.6. Figure of merit for different packages [2].

Conventional SO and TO packages are constructed using wire-bond technology. Wireless versions of the SO packages which reduce the package resistance and have increased power handling capability were introduced by several power device manufacturer. IR has replaced the wirebonds connecting the source to the leadframe with a solid copper strap that covers the surface of the die. Vishay Siliconix has developed a PowerConnect technology to eliminate the traditional wirebonds found in power MOSFETs by directly connecting the die and the copper leadframe. Fairchild later on developed what is called "SO-8 wireless package" which used solder bumps to connect the leads of the package to the source of the die instead of wire bonds to reduce package resistance. This trend has eliminated the use of traditional wirebonding in efforts to significantly improve the low-voltage MOSFET's on-resistance and thermal performance. However, the package leads continue to haunt the power transistor. Besides contributing to the overall on-resistance and power loss, the package leads also limit the MOSFET's heat dissipation and current-carrying ability. Furthermore, the leads may degrade the overall reliability of the package. In an effort to further reduce package resistance, recently Fairchild and IR announced their new power packages "BGA MOSFET" and "FlipFET™", respectively. These packages took the flip chip concept in IC package and completely eliminated both wire bond and leadframe by directly flip chip attach those solder bumped power device to substrate. These approaches reduce the package resistance to the minimal and also boosted thermal performance since those solder bumps can conduct more heat than the above mentioned leadframe.

Wireless versions of the SO package reduce the package resistance but do not significantly improve thermal performance. Most recently Fairchild went back to the SO-8 package format and developed the "Bottomless package" which accomplishes both resistance reduction and improved thermal performance goals simultaneously by eliminating the wire-bonds and allowing the substrate heat-sink to be in direct contact with the solderable back-side of the MOSFET die. Table 1.1 compares package current density and thermal performance of several Fairchild packages [3]. The bottomless package can handle 60% more current than the same die packaged in a conventional SO-8, allowing increased current output without increasing PCB space or component count.

Table 1.1: Package Current Density and Thermal Performance [3].

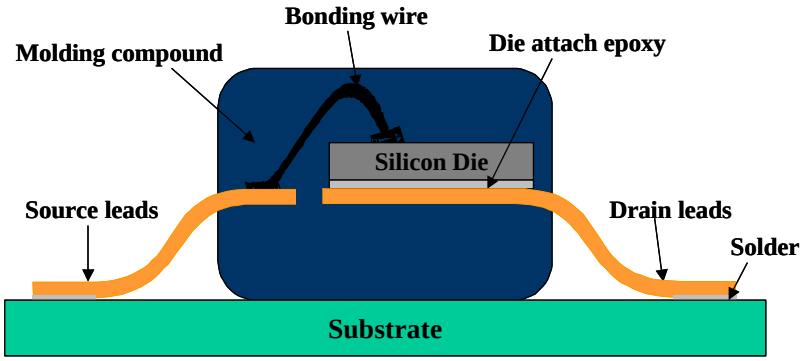
Package	Package Outline (mm^2)	Max $R_{DS(ON)}$ @ V_{GS} =4.5V (mΩ)	I_{OUT}*	θ_{J-A} (°C/W)
Bottomless	**30**	**6.0**	**20.9**	**38**
D-PAK	**57**	**9.5**	**15.3**	**45**
SO-8 Wireless	**30**	**7.5**	**14.9**	**60**
SO-8	**30**	**9.5**	**13.0**	**62.5**

*Steady-State current is calculated for T_A = 25°C, T_J = 150°C. Device mounted on 1 in^2 of 2oz copper on FR-4.

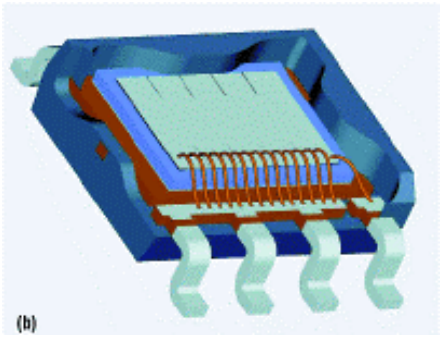
1.1.2 Recent Development in Single Power Chip Packaging

Traditional single power chip packages use wirebonds to connect the die to the source lead and the substrate, as shown Figure 1.7. Wirebonding on the top (source) of the MOSFET has been a primary contributor to electrical and thermal losses from packaging. The wirebonds and top-metal-sheet resistance contribute about 90% of package resistance [4]. The wire bonds have significant parasitic inductance at high frequencies. Also, wire bonds are one of the causes of failure in these devices [5]. Several new technologies have been developed to replace wire bonds in power packages. In this section, we review the advanced single power chip packaging approaches. The most significant concept has been developed is chip-scale packaging (CSP), an emerging technology originally developed for IC chips. CSP offers a promising solution for packaging power electronics due to its intrinsic size advantage, highly favorable cost/performance trade-off, and reliance on existing materials and assembly infrastructure. CSP

provides an area-bonding alternative to wire-bonding for interconnecting power devices. It has the potential to offer a low-cost KGD solution since chip-scale packaged power devices can be readily handled and tested at full power ratings. It also enables the power-processing elements of a power module to be in the form of low-profile surface-mount packages. Fairchild BGA MOSFET, Harris Thin pack and IR FlipFET^{TM} we are going to introduce are chip scale packages.



(a)



(b)

Figure 1.7. Traditional wire bond interconnected single power chip package. (a) Cross section; (b) Outline [4].

1.1.2.1 Vishay Siliconix PowerConnect technology

Vishay Siliconix has developed a PowerConnect technology to replace the traditional wirebonds found in power MOSFETs with direct connection between the die and the copper leadframe, as shown in Figure 1.8 [4, 6]. the PowerConnect maximizes thermal performance. To accomplish this direct connection, the top surface of the MOSFET die was made solderable by developing a nickel-based metallization process on top of the aluminum. The result is that the leadframe can be attached to both the bottom and the top surface of the die. The result is a twofold improvement in a miniaturized package over previous generations.

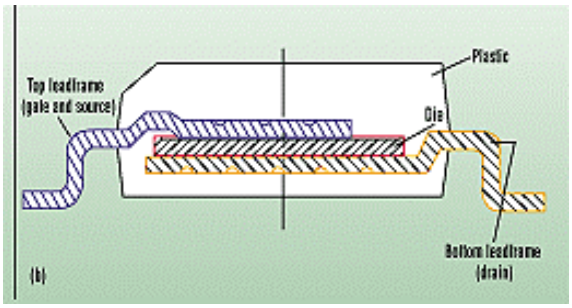


Figure 1.8. Vishay Siliconix's PowerConnect technology [4].

It was reported [4] that the interconnect contribution has been cut down to less than 1 mΩ by eliminating the bonding wires, thereby doubling the current capability of the low-voltage MOSFET in an SO-8 package. Also power dissipation was enhanced.

Reliability is a big concern in this PowerConnect strcture considering that the coefficient of thermal expansion (CET) of the leadfram is very different from that of silicon. There would have huge thermal stress at the interfaces.

1.1.2.2 IR's CopperStrap Technology

International Rectifier Corp. (IR) has replaced the wirebonds connecting the source to the leadframe with a solid copper strap that covers the surface of the die. Figure 1.9 illustrates IR's CopperStrap structure. CopperStrap provides a highly conductive path, thermally and electrically, from the die to the leadframe and pc board. According to IR, this has resulted in a 10 to 20% reduction in thermal resistance and a 61% reduction in package contribution to electrical resistance for source connections [7]. Specifically, it was reported that by replacing the fourteen 2-mil gold wirebonds (the maximum number for an SO-8 package can handle) with the CopperStrap, the die-source resistance was reduced from 1.1 mΩ to 0.11 mΩ [7].

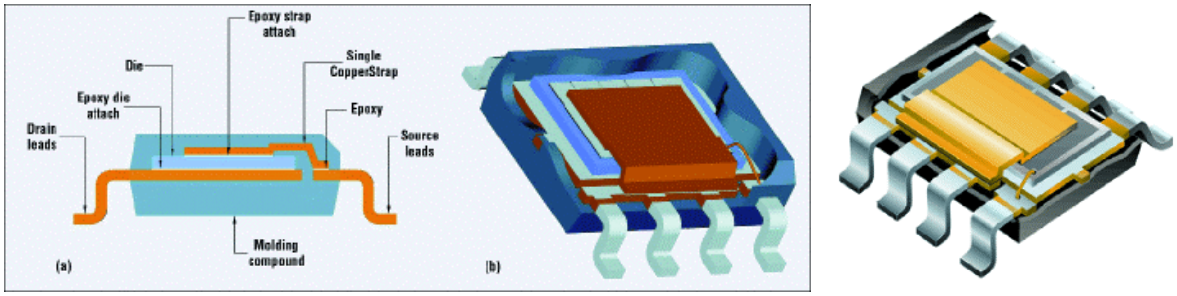


Figure 1.9. IR's CopperStrap technology [7].

Like the Vishay Siliconix PowerConnect structure, there is reliability concern in this CopperStrap structure. In order to release the thermal stress caused by the CTE mismatch of the

copper strap and silicon, silver-filled epoxy is used to attach the copper strap to aluminum top metal. The shape and features of the strap also play a key role in how well stresses are distributed under thermal cycling conditions.

1.1.2.3 Fairchild's SO-8 Wireless package

Figure 1.10 illustrates Fairchild's SO-8 wireless package. Conventional MOSFET packages use wire bonding to connect the leads of the package to the source of the die. In this wireless package, solder bumps are used to replace the wire bonds in order to reduce resistance and improve heat transfer. This package outline is same as conventional SO-8 package. Majority of the heat is still conducted through the bottom drain leadframes. Since solder bumps can also transfer some heat, the source leadframes can also be a heat path.

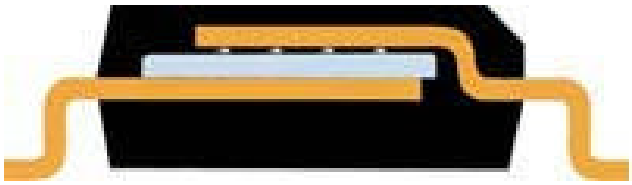


Figure 1.10. Fairchild's SO-8 wireless package [8].

1.1.2.4 Fairchild's BGA MOSFET

In December1999, Fairchild Semiconductor introduced new, low $R_{DS(on)}$ power MOSFETs in the form of ball grid array (BGA) package [9-10]. To overcome the drawbacks of traditional packages, including those modified recently, Fairchild Semiconductor has taken the flip-chip route. By encasing the low-voltage MOSFET in a fine-pitch ball-grid array (BGA), the company has eradicated the unwanted effects of wirebonds and packaging leads. Figure 1.11 shows the structure of the BGA MOSFET package. By allowing direct connection of the low-voltage MOSFET die to the printed-circuit board, the ball-grid array (BGA) package has eliminated the undesired contributions from the wirebonds and the leadframe. All solder balls on the edges of the BGA are for the drain connection. Meanwhile, the remaining balls are for the source except for one, which is for the gate. The BGA MOSFET is only 0.7-mm high [9]. BGA MOSFETs consume less than half the PC board area of MOSFETs with similar $R_{DS(on)}$ in conventional packages. BGA MOSFETs has delivered a dramatic improvement in on-resistance and has boosted the device's current-carrying and power-handling capability. Its unique design and construction disperses heat directly from the face of the die to the pc board through the solder balls, as well as from the back side of the die to the board via the drain solder balls. The

result is a dramatic improvement in the thermal efficiency and heat-transfer ability, compared to equivalent devices in both wirebonded and wireless surface-mount SO packages.

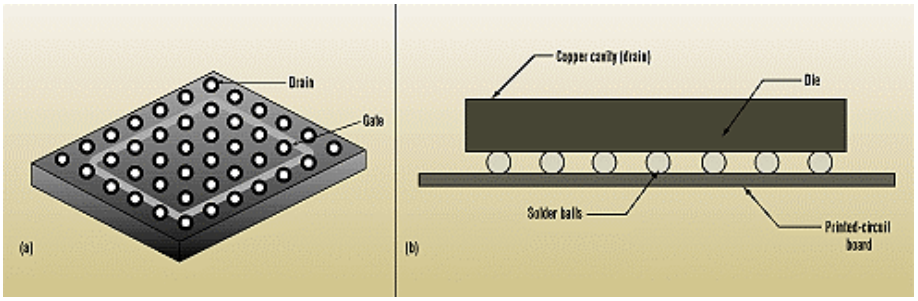


Figure 1.11. Schematic structure of BGA MOSFET [9].

Fairchild claimed the BGA MOSFET offered nearly a 35% improvement in on-resistance over a wireless SO-8 package, since the wirebonds and the leadframe are eliminated. Fairchild stated that the BGA MOSFET improves heat dissipation over modified SO-8 by 175%. By comparison to a traditional wirebonded SO-8, BGA MOSFET displays a 250% improvement [9].

1.1.2.5 Fairchild's Bottomless package

Fairchild announced their new bottomless MOSFET package in May 2000 [11]. Conventional SO and TO packages are constructed using wire-bond technology. Wireless versions of the SO packages reduce the package resistance but do not significantly improve thermal performance. The Bottomless package accomplishes both goals simultaneously by eliminating the wire-bonds and allowing the PCB heat sink to be in direct contact with the solderable backside of the MOSFET die. Figure 1.12 shows the schematic structure of Fairchild bottomless package and the outline of the package. In this structure, the continuous leadframe is attached to the source of the die, which has been bumped with solder balls at the wafer level. The bottom drain leads normally found in conventional SO packages are eliminated and hence it is termed "bottomless." Therefore, package resistance is much reduced, resulting in a very low $R_{DS(on)}$. As a result, it can handle 60% more current than the same die housed in a conventional SO-8 package. It was reported that this new package reduces the junction-to-case thermal resistance below 1°C/W, a dramatic improvement from 25°C/W found in conventional SO packages [11]. Thermal resistance is further improved by providing heat conduction from both the drain contact on the bottom of the package, and the source leads which are thermally well coupled to the MOSFET source.

(a) (b)

Figure 1.12. Schematic structure of Fairchild bottomless package (a) and the outline of the package (b) [3].

1.1.2.6 Harris Thin Pack (HTP) Technology

Harris Semiconductor developed a packaging technique for power devices such as IGBTs and MCTs as a part of Navy's Power Electronic Building Block project [12]. The design includes a metallized (Ti-Ni on Al) device on top of which a machined ceramic (Al_2O_3 or AlN) with metallized grooves is attached. The top side of the ceramic piece is patterned with conductor metallization while the bottom side of the ceramic is metallized with a Ni followed by a flash gold coating. The grooves are filled with Pb-Sn solder paste, which is reflowed to connect the contact pads of the devices to the top metallization on the ceramic. A schematic of the HTP structure is shown in Figure 2.1.8, where the solder contacts for different terminals of the devices are achieved on the top and bottom sides of the device.

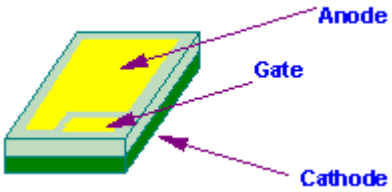


Figure 1.13. Schematic of a Harris Thin Pack with solderable contacts on both sides of the device [12].

1.1.2.7 IR's FlipFET™

In June 2000, International Rectifier (IR) introduced new power MOSFETs package, called FlipFET™, in which all of the terminals are on a single side of the die in the form of solder bump [13-14]. Figure 1.14 shows FlipFET™ power MOSFET package. The FlipFET™, a true chip scale package (CSP), combines the latest die design and wafer level packaging

technology to give the smallest package footprint possible. The FlipFET™ devices feature 0.25mm diameter eutectic solder (63Sn37Pb) bumps with 0.8mm pitch for standard SMT assembly, and are designed to require no underfill. FlipFET™ allows the use of existing SMT assembly processes with standard reflow profiles. The FlipFET™ power MOSFETs was reported would enable a new generation of super-compact power architectures with better power density for advanced portable applications, such as digital cameras, MP3 players, cell phones.

The FlipFET™ devices have a 100% silicon-to-footprint ratio. Compared to TSOP-6 and SO-8 packages, the FlipFET footprints are reduced by more than 70 percent. Since the die is the package, stray inductance and other losses associated with device packaging are minimized or eliminated. FlipFET™ packaging also improved on-resistance and thermal performance.

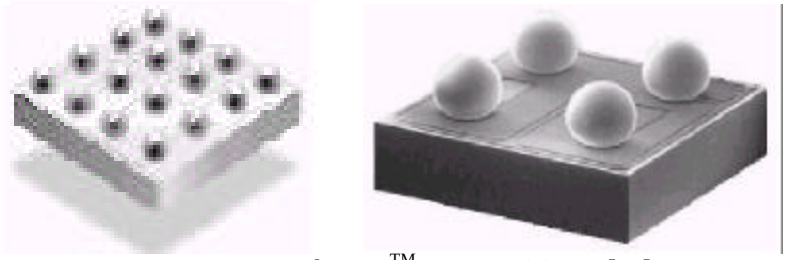
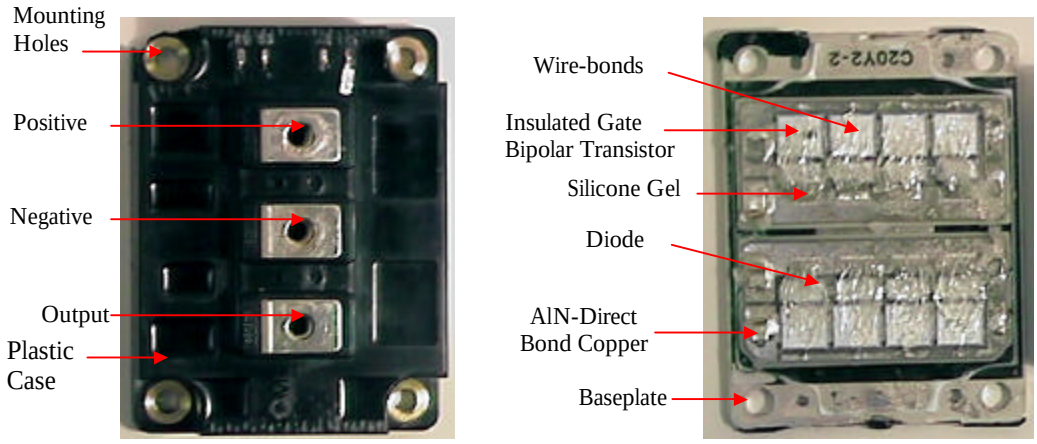


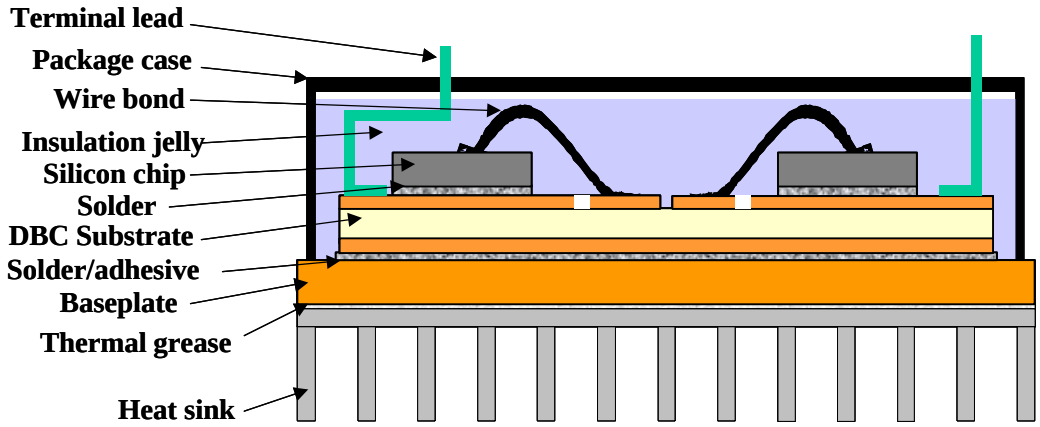
Figure 1.14. IR's FlipFET™ power MOSFET [15].

1.1.3 Power Electronics Module and System Packaging

Power modules have been widely used in applications such as motor drives and power conversion. They are normally in the form of plastic packages. Figure 1.15 shows the cut-away of a commercial IGBT module [16]. This module is a phase leg frequently used as a switching cell in a power electronics circuit. The emitter and the gate of the IGBT and the anode of the diode are located on the top of the die. The back is the IGBT collector and diode cathode, respectively. The cross-sectional structure of such a module together with the heat-sink is illustrated in Figure 1.15 (b). The direct-bond-copper (DBC) substrate is etched with the desired pattern such that the attachment of the IGBT and diode chips will make the collector-to-cathode connection in the bottom. Bonding wires are used to connect the IGBT and the diode chips to a conductor pad on the DBC substrate so that the emitter and anode connections can be made. The terminal leads, including power leads and gate control leads, are soldered on the required pad and introduced to the outside screw-mounting holes and the gate control connectors.



(a)



(b)

Figure 1.15. (a) Outside and inside of a commercial wire-bond module [16]; (b) the cross-sectional view of the IGBT module on a heatsink.

Inside the state-of-the-art power modules, interconnection of power devices is accomplished with wire bonds. In order to achieve high current capability, sometimes several silicon chips are connected in parallel by aluminum bonding wires in commercial power modules. As a result, there are tens or even hundreds of wire bonds in a high power module, as shown in Figure 1.15. Wire bonds have high parasitic resistance, inductance and moreover are prone to noise, parasitic oscillations, fatigue and eventual failure.

For a typical power electronics system, individual power devices are mounted on the heat sink, and the driver, sensor, and protection circuit are implemented on a printed circuit board and mounted on top of the power devices. In addition, a control circuitry and a microprocessor board are mounted on top of the driver board. The manufacturing process for such equipment is labor-intensive, the cost is high, and the reliability is low. In recent years, a higher level of integration

approach has been developed, where power semiconductors in die form are mounted on a common substrate with wire bond. The associated drivers, protection, and sensors are still realized in the form of a high-density printed circuit board, using surface-mount components and then packaged inside the plastic enclosure together with the power devices. There are fundamental limitations to this packaging approach. As we discussed above, the wire bond is known to be unreliable. The thermal management in this type of packaging is poor. The heat generated in a semiconductor die is transferred through its substrate onto the heat sink. Therefore, this form of packaging is primarily limited to low-power applications. In addition, the parasitic inductance associated with bonding wires and terminations are excessive, which severely limit the electrical performances of the module.

In power electronics, it is generally believed that advancement can be achieved only through a systems-level approach by developing intelligent, integrated power electronics modules (IPEMs) that enable greater integration within power electronics systems and their end-use applications [17-19]. Several manufacturers made a further step toward integration than what we introduced above and offer hybrid packaging, with switching devices assembled in planar structures [20-23] and the gate drivers and controls and protection circuits being put together in a subassembly and incorporated in a single module. This in turn increases the size and cost of the module, introduces undesirable degrading parasitics, and is prone to failure. Also heat dissipation is still limited by the planar structure and the problems with wire bond still exist in this kind of packages. Hence, innovative three-dimensional integration technologies which eliminate wire bonds are desired to be developed. It has been envisioned that the packaging of three-dimensional high-density multichip modules (MCMs) can meet the requirement for future power electronics systems [24]. The wirebond interconnected power devices are excluded from three-dimensional MCMs because of their large size, poor thermal management, high cost, and incompatible processing techniques. There are several MCM-based IPEM packaging technologies under development to eliminate wire bonds [24-30]. In the following section, we introduce some of those new packaging technologies.

1.1.4 Three-Dimensional Packaging Technologies of Power Modules

New technologies are under development to eliminate wire bonds. Basically these technologies can be classified into two categories: solder approaches and thin film approaches.

Solder approaches include using metal post, solder bump, metal strap and other ways to interconnect power device. Thin film approaches normally employ spin-coating or tape-casting for laying down dielectric, dry or wet etching for opening up the contact pads and thin film deposition or plating for interconnecting devices. Another approach outside these two categories is pressure contact assembly on the device pad [29]. Ferreira et al.[24] also proposed a packaging concept involving multiple layers of electromagnetic materials and switching function layers. Linden et al. [30] developed a power circuit substrate and packaging technology combining MCM-L technology with insulated metal substrate technology. However, some of these technologies have yet to prove their manufacturability, reliability, and cost-effectiveness. Some others are only limited to a few applications.

1.1.4.1 MPIPPS Packaging Approach

At the Center for Power Electronics Systems (CPES) at Virginia Tech, a low-cost integrated power electronics module structure called Metal Post Interconnect Parallel Plate Structure (MPIPPS) has been developed [25, 27]. In this low-cost approach, metal posts are used for interconnecting devices as well as joining the different circuit planes together. Figure 1.16 shows the MPIPPS structure. The power module has two layers of metallization with the devices sandwiched between the metallic layers. The bottom layer is an AlN-DBC with copper thickness of 10 mil. The copper layer is etched to a desired pattern where the IGBTs and diodes are attached by soldering. The copper posts, which have different sizes and heights for IGBT, diode, and top and bottom DBC plate connections, are soldered on top of devices and Cu metallization on AlN substrate. The top DBC plate is etched to a desired pattern and attached on to the copper posts of the bottom DBC plate to complete the electrical layout. The design concept is based on the use of direct bonding of copper posts, thus eliminating the use of wire bonds for power device interconnections.

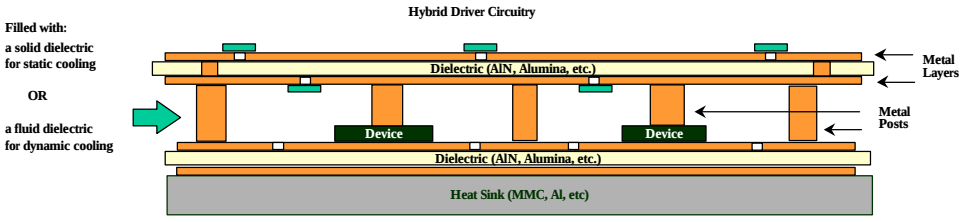


Figure 1.16. MPIPPS cross-section structure [27].

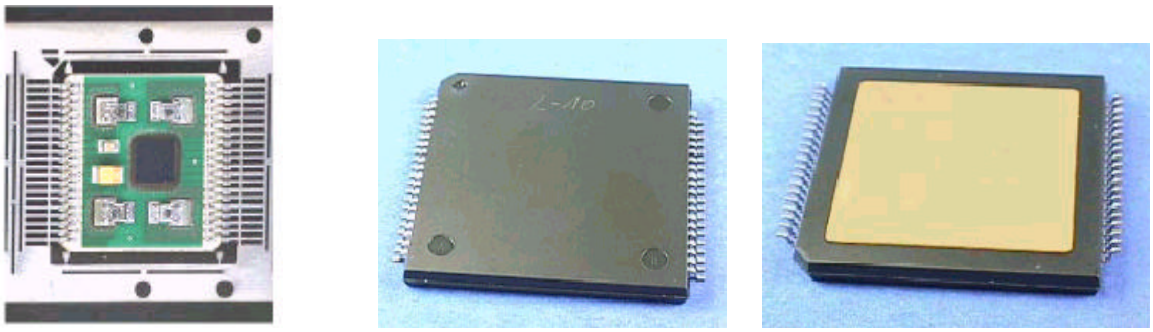
This packaging approach offers several advantages:

- Ability to carry large currents with negligible parasitic inductance and capacitance because of short and thick metal posts that are used for the interconnections in the module;
- Better thermal management due to additional thermal paths offered by the posts and the option of dynamic cooling with the use of a dielectric fluid flowing directly through the devices in-between the plates;
- Ease of integration of passive components since multiple plates can be readily stacked on top of one another through metal posts; and
- Better reliability because of low thermal stresses with the use of identical plates for the circuit planes.

1.1.4.2 Flip Chip Die Attach For Multichip Power package

Motorola's Advanced Interconnection Systems Laboratory has developed a new packaging concept for packaging multichip mechatronics power package utilizing flip chip die attach technology [31-32]. The multichip mechatronics power package is intended to provide a platform for automotive applications. In the multichip package, all power and control devices are flip chip attached directly on a common thermal conductive substrate. The general features of the multichip power package are shown in Figure 1.17. Figure 1.18 shows a prototype of the multichip power package. The components are mounted on a patterned substrate, which composes from bottom to top of a Cu heatsink layer, a dielectric layer and a Cu conductor layer. The leadframe is solder attached onto the substrate, the active devices are flip chip attached and the passive components are soldered on the substrate. The assembly is molded into an epoxy, such that the heatsink is exposed on the bottom of the package. The package outline can be variable industry standards that are utilized with surface mount packages, such as SOP and QFP. For lateral power devices, they are attached to the substrate according to the flip chip on board (FCOB) process using fully automated equipment set with fluxing unit, die placement, reflow and underfill dispense. For vertical power devices, an additional backside metal clip was solder attached to the backside of the dies, as shown in Figure 1.19. The generated heat was dissipated through the flip chip connections and down to the substrate. It was reported that this power package showed excellent heat dissipation performance and consistently passes automotive reliability criteria [32].

Figure 1.17. Multichip Power Package Concept, 1 Cu Heatsink, 2 Dielectric Layer, 3 Cu Conductor Layer [32].



(a) (b) (c)

Figure 1.18. A prototype of Multichip Power Package; (a) before molding; (b) Top view; (c) Bottom view [32].

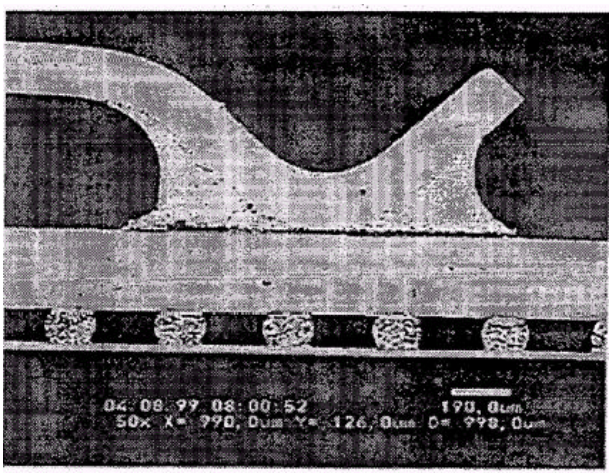


Figure 1.19. The crosssection of vertical power device assembly in Multichip Mechatronics Power package [31].

1.1.4.3 Power Multichip Module using Flip Chip as Interconnection

Another new packaging technique for power multichip modules has been developed which replace wire bond with flip chip [33]. Figure 1.18 shows the structure of the power multichip module. All power components are sandwiched between two DBC substrates which ensure thermal dissipation and electric isolation between components and heat sinks. The copper surface of the top DBC is overlaid with a 20 μm thick polyimide film, which is used to confine solder bumps and ensure electrical insulation between both DBCs. Vias are formed through the

polyimide film by standard photolithography and wet etching to solder the power device pads. The drain contact of IGBTs and cathode contact of diodes are brazed onto the bottom DBC with solder. The source and gate contact pads of IGBTs and the anode contact of diodes are brazed onto the top DBC with solder bumps using flip chip solder bump technology. Microchannel heatsinks were attached to both top and bottom DBC substrate in order to realize double-sided cooling considering solder bump is an additional heat path. It was reported that heat dissipation capability is much improved for this structure [33]. The complete module can dissipate as much as 323 W/cm^2 for a temperature rise of 40 °C. The top heat sink can dissipate up to 43% of the total heat.

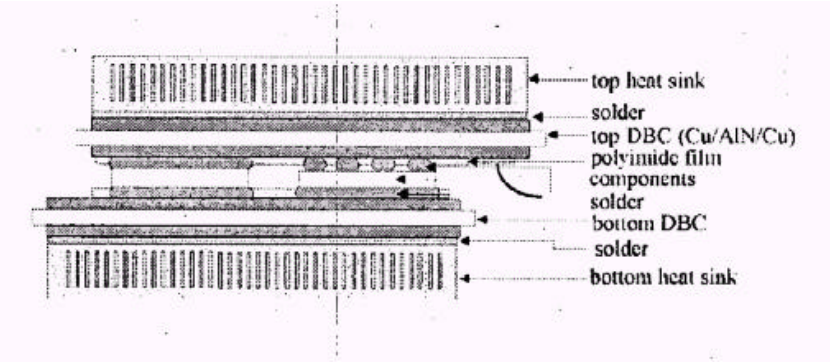


Figure 1.20. Structure of the power multichip module [33].

1.1.4.4 GE's Power Overlay Technology

The Power Overlay (POL) Technology developed at General Electric Company is a high density interconnect (HDI) process for the interconnection of Multichip modules [26, 34]. This technology has an interconnect layer built on top of the semiconductor devices and baseplates. The schematic shown in Figure 1.21 illustrates the section view of the POL design concept.

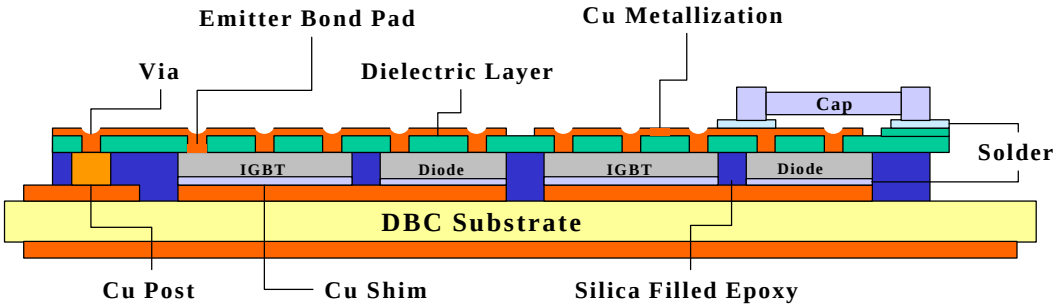


Figure 1.21. A cross-section schematic of a GE-POL structure [34].

Some of the anticipated advantages of the POL structure are described as follows:

- elimination of wire bonds with metallurgical interconnections improving electrical performance;
- improved thermal performance via reduced numbers of thermal interfaces and two-sided heat removal;
- reduced profile and more flexible packaging options for stacking additional circuits;

The POL process utilizes power semiconductor devices (IGBT, MOSFET, and diode) that are mounted to the backside of a Kapton™ tape using adhesive. The Kapton™ tape has pre-formed vias with specific pitch and size. These vias serve as electrical paths for circuit functioning. Metallization on the vias (making contact to the devices) and the polymer dielectric is achieved through a combination of sputtering and plating process [35-36]. First, a barrier and adhesion layer of Ti (typically 1000Å) is sputtered followed by a seed layer of copper (1000Å). On top of the seed copper layer, a five mil thick copper layer is deposited by electroplating. This thick copper layer provides a low-loss interconnection of the power devices. Finally, a thick photoresist is applied on the thick copper to pattern etch conductor pads on the electroplated metallization. DBC substrates are attached on the backside of devices through soldering. More layers can be built up repeatedly to realize a multilayered interconnect structure. Low profile passive components can also be embedded into the overlay. The inherent multilayer nature of POL will facilitate the integration of gate drive and other circuits into a three-dimensional package.

However, GE-POL structure has not been successfully tested for high-power applications; furthermore, plated thick copper layers as well as the Kapton layer would most likely generate a significant amount of thermo-mechanical stress on the device interconnection joint, thus reducing reliability of the structure. Also rework on the module would be almost impossible since the entire structure is built on an additive process.

1.1.4.5 Pressure Contact Technology

Semikron's SKiiPPack module includes pressure contact design with a snap-on mounting configuration. Snap-on mounting contacts the PC board and mounts the heat spreader in a single manufacturing step [28-29]. As shown in Figure 1.22, a special spring with a C-shape in the middle provides the required pressure loading and also provides the electrical contact between the pc board and the internal contact to the DBC. The matrix of 40 to 60 spring-loaded contacts

also provides distributed vertical pressure to press down the DBC evenly to the heat spreader. The spring contact material is a copper alloy with chromium, silicon and titanium, which provides good electrical conductivity, defined spring characteristics even after long-term temperature exposure and good manufacturability of the springs. Internal bus bar construction is supported by the plastic pressure spreader, which eliminates the need for additional mechanical support.

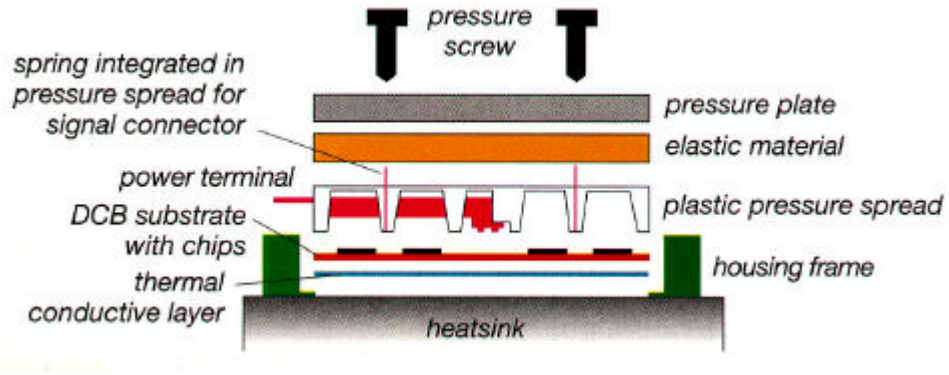


Figure 1.22. A cross-section view of Semikron's SkiiPPack with pressure contacts [28].

Despite the merits, the biggest disadvantage of pressure contact technology is its expensive manufacturing cost involved with precise machining and planarization, which may limit its application. Also, the reliability of these modules is a concern.

1.2 Motivation of using Solder Joint as Power Chip Interconnection

1.2.1 Introduction to Solder Joint Interconnection

Solder joint interconnection technology (or flip chip technology) is considered to be an advanced form of surface mount technology, where a bare semiconductor chip processed with solder bumps on its surface is turned upside down and bonded directly to the substrate without requiring any intermediate chip packaging or lead frame mounting. Figure 1.23 (a) shows schematically a solder bump termination on a chip and (b) shows a flip chip assembly. The technology is applicable to either single-chip packages or multiple-chip modules. The flip chip technology was originally invented by IBM in 1962 focused on solid logic technology with silicon transistors mounted on thick-film substrate. Several years later, the concept of limiting the solder-wettable area on the mating pads of the components was introduced, that is, controlled collapse chip connection (C-4) technology. C4 solder interconnects of devices have provided

enhanced chip input/output density, uniform chip power distribution, improved cooling capability. Solder interconnects have also resulted in increased packaging density, data bandwidths and operating frequencies while reducing system-level noise and other parasitics. In recent years, the electronic packaging industry has experienced a tremendous boost by adopting flip-chip technology in all areas of packaging applications. Flip chip technology has also allowed the packaging industry to develop new technologies such as Ball Grid Array (BGA) and Direct Chip Attach (DCA). Continuous improvements, though, are sought in the areas of cost reduction, increased package density, and enhanced reliability for these area array technologies.

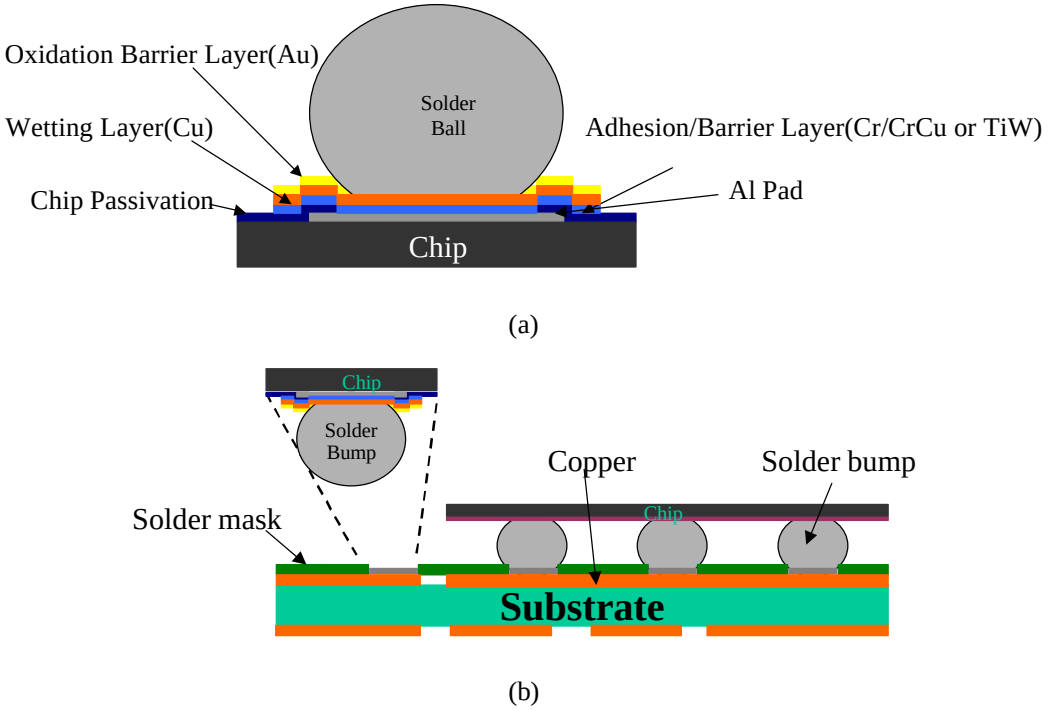


Figure 1.23. (a) Schematic of solder bump for flip chip joining; (b) flip chip assembly.

The three most commonly used device interconnection methods are face-up wire bonding, face-up tape-automated bonding (TAB), and flip chip. Among these three methods, flip-chip technology provides the highest packaging density, greatest number of I/Os, shortest possible leads, lowest inductance, highest frequency, best noise control, smallest device footprints, and lowest packaging profile [37-40]. The advantages of solder-bump interconnections of flip-chip packaging have been well-documented in numerous research works [41-43]. Table 1.2 compares a few parameters, including the reliability [40] of the three common interconnection methods and Table 1.3 lists a few critical features of the most common interconnect technologies [44].

Table 1.2. Parameters of the three different interconnections [40]

Parameters for Comparison	*Wirebonding*		*TAB*	*Flip Chip*
Connection Metallurgy	Al	Au	Cu	Pb/Sn
Resistance (Ω)	0.035	0.03	0.02	0.002
Inductance (nH)	0.65	0.65	2.10	0.200
Capacitance (pF)	0.006	0.006	0.04	0.001
I/O density (cm^{-2})	400	400	400	1600
Rework	Poor	Poor	Poor	Good
Failure rate (%/1000 h)	1×10^{-5}	1×10^{-5}	N/A	$<1\times10^{-3}$

Table 1.3. Comparison of common interconnection technologies (Ref. 44)

Feature	**Wirebond**	**TAB**	**Flip TAB**	**Flipchip Solder**	**Flipchip Adhesive**
Maturity	Very Good	Good	Limited	Very Good	Improving
Die Availability	Very Good	Fair	Fair	Poor	Very Good
Edge Bond Pitch	4-7 mils	3-4 mils	3-4 mils	8-10 mils	8-10 mils
Max I/O	400-500	800-1000	800-1000	>1000	>1000
Footprint	20-100 mils	80-800 mils	80-100 mils	<20 mils	<30 mils
Assembly Rate	Slow	Good	Good	Good	Good
Repairability	Poor	Poor	Poor	Moderate	Moderate-Poor
Chip Bi/Test	Difficult	Good	Good	Improving	Improved
Cost	$0.001	$0.003-0.01	>$0.003	$0.002	$0.0001

1.2.2 Motivations of Solder Joint Interconnection for Power Chips

In today's IC packaging industry, solder interconnections via solder bumping is a well-established technique. Compared to IC packaging, power electronics packaging is still at its infancy in terms of adopting novel interconnection schemes, which are considered state-of-the-art in the IC packaging industry. Microelectronics packages basically deal with signal processing, however, power electronics packages handle and control electromagnetic energy conversion and transportation. Thus, solder joint for power chip interconnection has to fulfill at least these requirements: (1) current handling capability; (2) power loss reduction; (3) improved thermal management. Considering the nature of solder joint interconnection, there are some

unique advantages in general of solder interconnects over the wire-bond interconnections [44-45]:

- Solder interconnects design allows placement of solder joints in an area array on the whole die surface rather than placing them on the peripherals, as in a wire-bond design, thus reducing footprint meanwhile improving current handling capability.
- Increased wafer utilization. Integrated circuits specifically designed in area array for bump can result in smaller die size and consequently, more die per wafer.
- Wider pitches over the entire area of a die would offer cost and routing relief.
- Solder interconnects allow a uniform and low inductance/resistance power feed across the face of the die, minimizes on-chip variation, which is a critical factor in wire-bonded device operation.
- The cost of solder interconnection method is effectively the same with any change of patterns. However, in a wire-bond scheme, with reduced pitch size, the cost associated with assembly, yield and reliability would increase.
- Potentially offers improved reliability of chip interconnection as well as the whole system.
- Solder interconnects allow thermal management from both faces of a die, providing bi-directional heat dissipation paths.
- Creation of standardized footprints of the same die type from various suppliers.
- Enhanced machine utilization and throughput since wafer-level solder bumping is realized in a fully automated manner and batch process.

In the following, we discuss the detailed advantages that solder joint technology could offer for power chip interconnection and these advantages are the origins of our motivation of using solder joint as power chip interconnection.

1.2.2.1 Size Reduction and Power Density Improvement

There is an ever-increasing demand for miniaturization of overall electronic components and systems, and in particular miniaturization of power conversion circuits and their associated power components. Also in an effort to meet the need for increased power density - power output per unit volume, it is critical to minimize footprint areas taken by power conversion

devices. Power chip packaging has been typically focused on peripheral packages with wirebonds as the chip level interconnects. The devices on the silicon die are routed from the center location on the chip to the wirebond pads on the periphery. The chip is attached to a substrate and is wirebonded to electrically connect the chip to the leadframe. The leadframe extends interconnects through a dielectric into a peripheral pattern, where it can be soldered to a printed wiring board. In this kind of standard power package, a large part of the internal area is used for the wire bond pads on the leads and these pads are necessary since they provide an attachment point for the bond wires as they connect the leads to the silicon device in the package. An alternative to peripheral interconnect packaging is to access the unused area under the chip using area-arrayed interconnects, as shown in Figure 1.24. In a solder joint area-array package, the surface of the chip has an array of solder joints that are joined to a substrate when the chip is flipped over and it is possible to achieve 100% silicon to footprint ratio and thus dramatically improve the power density.

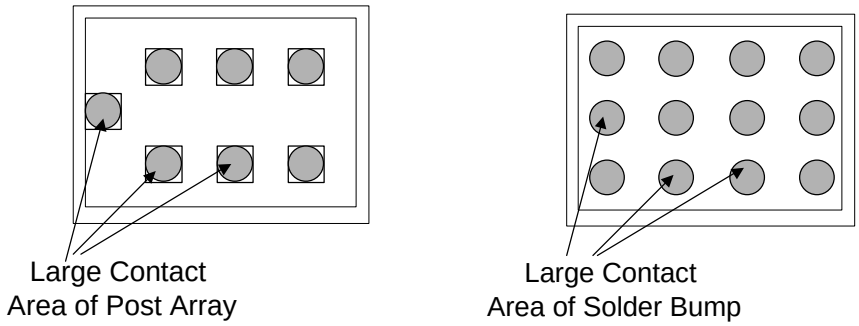


Figure 1.24. Top view of solder joint area array interconnection.

1.2.2.2 Parasitic Resistance and Inductance Reduction

Advances in power semiconductor technology have increased the proportion of electrical resistance contributed by the package, as shown in Figure 1.25. The top-metal resistance of the die isn't normally taken into account when calculating package resistance, as it isn't considered to be part of the package. But it is reported that depending on the location of the wirebonds on the top metal, thin aluminum top metal could contribute significant amount of resistance and it can be reduced by more than 60% if most of the die's top surface is covered by a kind of area interconnection [4]. In this aspect, packaging actually contributes more of the resistance. This leads to the strategies of focusing on the packaging structure and layout which can secure more usable die area.

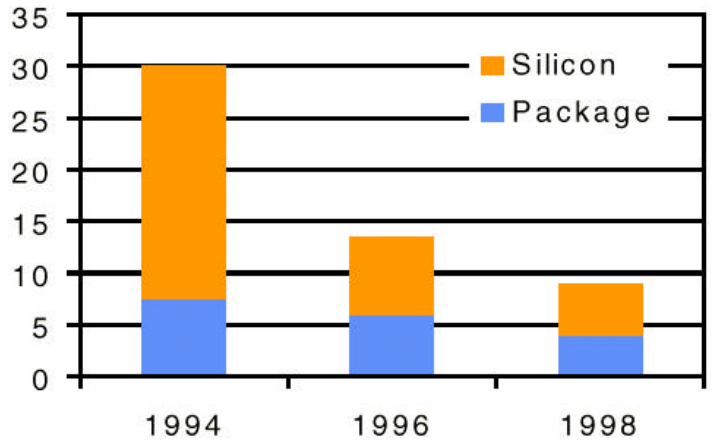


Figure 1.25. The evolution of electrical resistance contribution from silicon and package for power MOSFET [6].

For a wire bond interconnection, it is difficult to design the sweep of wires from the chip to the leadframe in peripheral packaging to minimize resistance, self-inductance and mutual inductance between adjacent wires. Each wire bonds and lead frame has a finite resistance, adding to the RDS(ON) of the device. An area arrayed solder joint chip interconnection could reduce the package resistance significantly by allowing many parallel connections to be made from the source of the die to substrate directly or to the lead frame. Also if die itself is the total package, we eliminate the lead frame resistance. Advantages of solder-bump interconnection of chips have been discussed in section 1.2.1. Solder-bumped chips have short pad-to-circuit connections for reduced coupled noise, low capacitance, and low self and mutual inductance, as illustrated in Figure 1.26.

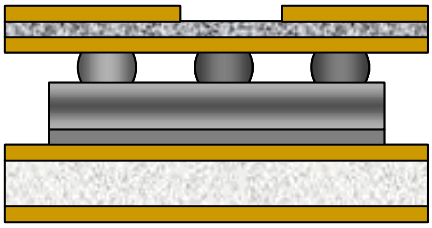


Figure 1.26. Cross-sectional view of solder joint area array interconnection of power chips.

1.2.2.3 Thermal Management

Thermal capability is measured with a thermal impedance known as R_{thja}, where lower is better, which is the thermal resistance from the junction of the silicon to the outer case of the device or ambient. Thermal capability can be affected by both the silicon and the package. Power semiconductor manufacturers obtained lower thermal impedance by reducing the thickness of a silicon wafer, or merely use a larger area of silicon to dissipate the heat. However,

the heat generated by the power semiconductor eventually need to be dissipated out from the package. Packages can affect the thermal performance by allowing faster, more effective heat flow out of the device. Thus, the package should be designed ideally to have double-sided cooling, to have as few interfaces as possible, preferably no interface at all, and interface should be as thin as possible. On the other hand, packages can also improve the resistance of a device and hence improve the electrical performance and lower power dissipation. A preferred package design should make the chip-level interconnection as short as possible and increase the area of conducting contact from the electrode (source for MOSFET and emitter for IGBT) of a power semiconductor to the board-level connection.

A solder joint area array package is the right answer to the above two questions. A solder bumped chip package accomplishes both goals simultaneously by replacing the long wire-bonds with short solder joints and allowing substrate to be in direct contact with the solderable back-side of the power die. The solder joints and thermally conductive underfill material (if used) can act as heat paths because they are attached to the active surface of the silicon and are massive enough to draw heat away from the silicon. Therefore, thermal resistance of the package is improved by providing heat conduction from both the drain contact on the bottom of the package, and the source solder joints. A finite-element thermal analysis [46-47] indicated that 20-43% heat could be removed through the top solder joints.

1.2.2.4 Current Handling Capability

The ability of a package to handle current is inextricably linked to the thermal properties of a device as discussed earlier. A solder joint area array chip interconnection and optimal package structure could improve current handling capability of power packages. As demonstrated in Figure 1.27, solder-bump contacts provide a larger effective contact area between power semiconductor devices and outside circuitry. Obviously, thick solder bumps can carry larger currents than thin wire bonds. The larger contact area greatly reduces current crowding and eliminates the hot spots that could happen in wire bonds. In general, since power chips only have several I/O, power die pad size can be designed much larger than that of IC chips, which has much more I/Os. It is possible to use larger solder bumps or even BGA to interconnect power chips. Larger solder bumps can carry higher current, which enables those devices to be used in higher power level applications.

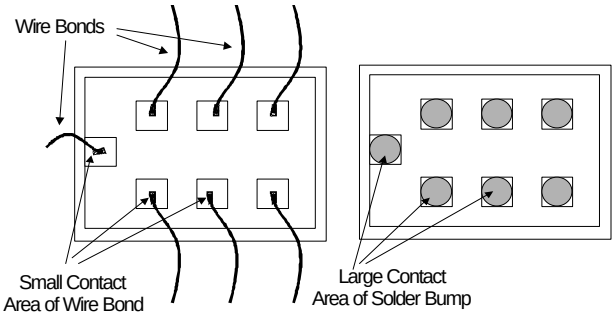


Figure 1.27. Comparison of contact geometries of wire bond and solder bump interconnection

1.2.2.5 Reliability Considerations

Inside the state-of-the-art power devices and modules, interconnection of power chips is accomplished with wire bonds. In order to achieve high current capability, sometimes several silicon chips are connected in parallel by aluminum bonding wires in commercial power modules. As a result, there are tens or even hundreds of wire bonds in a high power module, as shown in Figure 1.28. Wire bonds not only have high parasitic resistance, inductance and but also are prone to noise, parasitic oscillations, fatigue and eventual failure. Currently, the commercially available, state-of-the-art wire bond module has reliability problems with a lifetime of only a few years [48]. Wire detachment due to heel cracks, bond lift-offs, wire fusing, and reconstruction of aluminum metallization on the chips and corrosion of wires are the major reliability limiting points of wirebond interconnection. Some of the more specific reliability problems associated with the wire-bond technology are listed below [16, 49].

- The proximity effect resulting from bonding wires coupling affects the current distribution among the power chip (especially Insulated Gate Bipolar Transistor) cells within one chip as well as among the paralleled chips. This imbalance will unevenly load the paralleled IGBTs with different fatigue mechanism, even though they are designed for identical operations.
- Magnetic field induced by the close-coupled bonding wires causes the problem of the device stress and bonding wire fatigue. The lateral mechanical force has a tendency to peel the aluminum coating off the silicon chip. In most cases, the IGBT chip surface tends to crack or the bonding wire opens after power cycling test and thermal cycling.
- Commercially available, state-of-the-art wire-bond module has large parasitic inductance associated mainly with the packaging of terminal leads, which is related to the planar packaging techniques. Since the bottom conductor pads have to accommodate both wire-bonds and terminal leads carrying a high current density, they occupy a large area of the

module substrate (non-silicon area) contributing to parasitic inductance. As more IGBTs are paralleled, the inductance of the conductor pads becomes more dominant.

- Aluminum bonding wires have large thermal expansion coefficient mismatch with silicon chips. Wire bond lift-off, caused by thermal stresses, is one of the main failure mechanisms encounter in high power IGBT modules subjected to power and/or thermal cycling.
- Wirebond cratering. It occurs when silicon fractures as a result of unoptimized wirebond parameters—the bonding force, as well as the intensity and duration of ultrasonic power. Cratering can't be detected reliably at final test. Therefore, it usually appears during reliability testing or in the field.
- Wire fusing or lift-open due to hot spot. The current imbalance in bonding wires, due to the inconsistency of contact resistance, proximity effect could cause some thermal problem, or even burn out the wire bond connection. The emitter and gate bonding wires are frequently observed to be either fused or lifted-open.

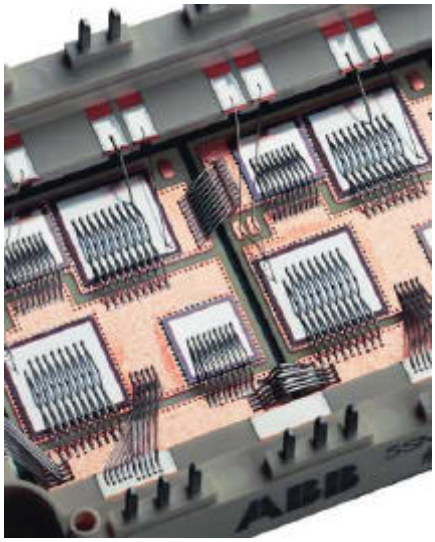


Figure 1.28. Wire bonds in power modules (Courtesy of ABB).

To mitigate the reliability problems associated with wire bonds, power module manufacturers improved the composition of the wire, the shape of the bonding tool, the bonding parameters, the metallization on leads and the protective coatings rather than exploring alternative device interconnection schemes. To improve performance and reliability of packaged power electronics, wire bonds need to be replaced. The larger contact area of solder joints greatly reduces current crowding and eliminates mechanical forces generated between wire bonds. Solder joint also allows mechanical and thermo-mechanical forces to be distributed over

a larger area, thus reducing equivalent mechanical stresses at the device connections. However, thermal stress caused by the CTE mismatch of silicon and substrate is a serious concern for solder bump interconnection. Fortunately, solder bump technology has the flexibility to extend the solder joint interconnections to accommodate larger and denser chips without affecting system reliability. More specifically, solder joint interconnection offers the opportunity to improve its reliability in the following areas: geometry or shape improvement; alternate solders; use of compliant substrates and underfill encapsulant. We will discuss these issues in Chapter III.

1.2.2.6 Manufacturability

Wafer-level solder bumping and flip-chip bonding facilities are commercially available in IC industry. The solder bumping and flip chip bonding processes are compatible with most surface-mount assembly operations and now it is fully automated. Solder reflow process offers high process yield and high quality bonding as it is batch process. Recent cost studies also show that area array solder bump flip chip is cheaper than wire bonding [45, 50]. Thus, solder joint area array interconnection potentially offers low cost power chip interconnection and also provides the possibility of power components standardization.

1.3 Objectives and Significance of this Study

A major challenge in today's power electronics packaging is the interconnection at the chip level. Chip-level interconnection is the vehicle that connects a silicon chip's input/output (I/O) terminals to a substrate or carrier and provides communication (signal and /or power) between the chip and outside world. The interconnection must meet certain performance requirements in electrical, mechanical, and thermal characteristics. Inside the state-of-the-art power devices and modules, interconnection of power chips is accomplished with wire bonds. Bonding wires are the major contributors to the parasitic resistance and inductance of a power device or module either directly or indirectly. One of the major failure modes found in wire bonded power devices or modules is bonding wire failure since bonding wires are prone to noise, parasitic oscillations, and fatigue. Furthermore, wire bond is the inherent limit for power device and module size reduction, power density improvement and implementation of multilayer multichip power modules. Therefore, a primary objective of this study is to design and develop solder joint interconnection technique for power chips replacing wire bonds. The ultimate goal

of developing solder joint interconnection for power chips is to apply this technology in building advanced power packages. Naturally, the second objective of this study is to develop chip-scale power packages and a three-dimensional integrated power electronics module structure using solder joint as chip-level interconnection. However, solder joint reliability is a major concern for power chip interconnection. Thus, the other objective of this study is to improve solder joint reliability by developing new solder bumping process for optimal solder joint structure, underfilling solder joint with encapsulant and using flexible substrate, and investigate the failure behavior of solder joints. In summary, the three objectives of this study are:

1. **Design and develop solder joint interconnection technique for power chips;**
2. **Evaluate solder joint reliability and investigate the failure behavior of solder joints.**
3. **Process and develop chip-scale power packages and a three-dimensional multichip packaging approach for integrated power electronics modules;**

Solder joint interconnects will provide the high packaging density, low resistance and inductance, small device footprints, and low packaging profile - all of which are highly desired for power semiconductor applications and are fundamental towards the implementation of a three-dimensional power module structure. The use of solder joint interconnection can improve package structure layout and thus reduce the conductor trace inductance. Solder joint interconnects are capable of carrying larger currents than wire bonds. Furthermore, solder bumping technology is quite mature in integrated circuit (IC) industry and the equipments are commercially available. Thus, we can built on IC experience and develop solder joint technology for power electronics application.

The second objective of this study is to develop chip-scale power packages and implement the chip-scale packaged power devices in building three-dimensional power modules that can potentially have the following features:

- Ability to carry large currents with negligible parasitic inductance and capacitance and low resistance;
- An alternative to known-good-die solution for power devices;
- Better thermal management, preferably three-dimensional heat dispassion;
- Easy integration of drive, control and other circuits;
- Ready for standardization of power electronics product;
- Improved reliability;

- Low profiled package and easy of fabrication;
- Robust packaging;

In recent years, an integrated systems approach to standardizing power electronics components and packaging techniques in the form of power electronics building blocks has emerged as a new concept in the area of power electronics [51]. As a result, it has been envisioned that the packaging of three-dimensional high-density multichip modules (MCMs) can meet the requirement for future power electronics systems [52]. The wirebond interconnected power devices are excluded from three-dimensional MCMs because of their large size, poor thermal management, high cost, and incompatible processing techniques. Chip-scale power packaging is a new concept in power packaging area. It offers high silicon to package footprint ratio, provides a known good die solution to power chips, and creates an opportunity for power component standardization. More importantly, chip-scale power packages are the basic units that can be readily used to implement multichip power modules and other power systems. In this study, two chip-scale power packages have been designed and developed and a three-dimensional high-density multichip power module structure has been implemented using the chip-scale power packages. These chip-scale power package structure as well as the power module structure can be used to a variety of applications.

Solder joints must maintain mechanical as well as electrical performance in both power and thermal cycling of the power electronic systems. The third objective of this study is to improve solder joint reliability and investigate failure behavior of solder joint. Solder joint failure is a very important issue in the solder area array technologies even for microelectronics application. For power electronics components and equipments, the reliability requirement is more demanding. Thermal stress caused by the coefficient of thermal expansion (CTE) mismatch between silicon chip and substrate is the source of solder joint fatigue failure. As a result, there must come about an extension of the conventional solder joint interconnection technology to accommodate larger chips and denser solder joint without affecting system reliability. In this study, solder joint reliability is improved through three ways. One is to develop a new solder bumping process that can fabricate high standoff hourglass/column shaped solder joint. The second way is to underfill the solder bumped chips, which has been proven in IC area to improve solder joint reliability. The third way is to use compliant substrate that could reduce the strain and thus stress in the solder bump interconnection. Accelerated temperature

cycling test has been conducted to verify the above three ways of improving solder joint reliability. This research is mainly focused on the investigation of solder joint geometry and flex substrate effect on reliability since underfill effect has already been proven in IC industry. These ways of improving solder joint reliability not only has their applications in power packaging, but also have guidance and significance in IC flip chip technology and ball grid array technology.

1.4 Organization of this Dissertation

This study is divided into seven chapters. Chapter 1 includes an overview of the power electronics packaging and the objectives and significance of this study, motivations of using solder joint as power chip interconnection. The overview of power electronics packaging is divided into two parts, one dealing with single power chip packaging and the other covering power electronics module and system packaging and assembling. Inside each category, the state of the art technologies are reviewed and the advanced or alternative technologies recently developed or under development are introduced. Chapters 2 through 6 are the core parts of this study which cover the experimental procedures (design and process of solder joints), results and discussions, and the applications of the developed solder joint interconnection in chip-scale power packaging as well as integrated power electronics packaging. These chapters are essentially written as technical papers dealing with the above aspects. Chapter 7 titled "Summary and Conclusions" summarizes the key achievements and findings of chapters 2 through 6, and suggests some possibilities and directions for future work in this area.

Chapter 2 is entitled "Process Development for Solder Joints on Power Chips". This chapter deals with the design and processing of different solder joints: conventional single bump solder joint, stacked high standoff solder joints with hourglass, column and barrel shape. Also in this chapter, commonly used solder bumping process is reviewed and alternative solder joint structures for improving solder interconnection reliability are introduced. The subject matter of this chapter is the basis for one journal paper entitled "Stacked Solder Bumping Technology for Improved Solder Joint Reliability" which has been accepted to appear in the Microelectronics Reliability journal.

Chapter 3 is entitled "Solder Joint Reliability Assessment". This chapter deals with the investigation of solder joint microstructure, testing of solder join adhesion strength under different conditions and evaluation of solder joint reliability. The techniques used in this chapter

for characterizing solder joint interfaces and detecting solder joint cracks are optical microscopy, scanning electron microscopy and energy dispersive X-Ray analysis, and scanning acoustic microscopy. The testing of solder joint adhesion strength required shear and tensile tests. Accelerated temperature cycling test was used to evaluate solder joint reliability with the electrical resistance change as the evaluation criterion. Reliability data for both single bump solder joint and stack solder joints is presented in this chapter and the failure modes of these solder joints are discussed.

Chapter 4 is entitled "Effect of Substrate Flexibility on Solder Joint Reliability". This chapter discusses the influence of flex substrate on the reliability. Accelerated temperature cycling test showed that solder joint reliability is improved by using flex substrate. Thermal mechanical analysis technique is used to investigate the flex substrate behavior under temperature cycling. Test results shows that flex substrate buckles during temperature cycling, which is considered to reduce solder joint thermal strain and thus improve reliability.

Chapter 5 is entitled "Development of Chip-Scale Power Packages Using Solder Joint Interconnection". Chip-scale power packaging concept is put forward in this chapter and two chip-scale power package structures are proposed and developed. The design, fabrication process of the chip-scale packages are introduced and their electrical performance, reliability are evaluated. Results from this chapter are the basis for two papers. One is entitled "Chip-Scale Packaging of Power Devices and its Application in Integrated Power Electronics Modules," which has been accepted to appear in the IEEE transactions on Advanced Packaging and was presented and published in the proceedings of the IEEE Electronic Components and Technology Conference, 2000. The second paper is entitled "Power Chip Interconnection: From Wire bonding to Area Bonding," which appeared in the International Journal of Microcircuits and Electronic Packaging and was presented and published (best paper of the session) in the proceedings of the 33rd International Symposium on Microelectronics –IMAPS 2000.

Chapter 6 is entitled "Development of Flip Chip on Flex Structure for Packaging Integrated Power Electronics Modules". A flip chip on flex structure is proposed in this chapter. The design, material selection issues and fabrication process of the flip chip on flex module are discussed. The electrical performance and reliability of the flip chip on flex module are reported. Results from this chapter are the basis for three papers. One is entitled "Three-dimensional Flip-Chip on Flex Packaging for Power Electronics Applications," which appeared in the IEEE

transactions on Advanced Packaging. The second paper is entitled “Packaging of Integrated Power Electronics Modules Using Flip-chip Technology,” which has been accepted to appear in the IEEE Industry Application Magazine and was presented and published in the proceedings of the IEEE Applied Power Electronics Conference and Exposition, 2000. The other paper is entitled “Application of Solderable Devices for Assembling Three-Dimensional Power Electronics Modules.” This paper was presented and published in the proceedings of the 31st IEEE Power Electronics Specialists Conference, 2000.

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