A Compact Three-Phase Multi-stage EMI Filter with Compensated Parasitic-Component Effects

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ABSTRACT

With the advent of wide bandgap (WBG) semiconductor devices, the electromagnetic interference (EMI) emissions are more pronounced due to high slew rates in the form of high dv/dt and high di/dt at higher switching frequencies compared to the traditional silicon technology. To comply with the stringent conducted emission requirements, EMI filters are adopted to attenuate the high frequency common mode (CM) and differential mode (DM) noise through the propagation path. However, self and mutual parasitic components are known to degrade the EMI filter performance. While parasitic cancellation techniques have been discussed at length in prior literature, most of them have focused mainly on single phase applications. As such this work focuses on extending the preexisting concepts to three-phase systems. Novel component placement, winding strategy as well as shielding and grounding techniques were developed to desensitize the influence of the parasitic effects on a three-phase multi-stage filter. The effectiveness of the three-phase filter structure employing the proposed methodologies has been validated via noise measurements at the line impedance stabilization network (LISN) in a 15kW rated motor drive system. Consequently, general design guidelines have been formulated for filter topologies with different inductor and capacitor form-factors.

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GENERAL AUDIENCE ABSTRACT

The adoption of wide bandgap (WBG) semiconductor devices, such as Silicon Carbide (SiC) or Gallium Nitride (GaN) transistors, improves the power density with higher slew rates and switching frequencies compared to the traditional Silicon technology. However, the high switching speeds and high frequencies have generated higher electromagnetic interference (EMI) noise in the surroundings. To comply with the conducted emission requirements at the grid terminal, EMI filter is mandatory to attenuate the high frequency EMI noise that flows into grid. However, near field and the effect of parasitic components are known to degrade the filter performance at the higher end of frequency spectrum where the limit lines are typically stringent. While parasitic cancellation techniques have been discussed at length in prior literature, most of them has focused mainly on single phase applications. Therefore, this thesis aims to extend the pre-existing concepts to compensate the mutual and self-parasitic coupling components in a three-phase multi-stage filter. In this regard, novel component placement, winding strategy as well as shielding and grounding techniques were developed to compensate for the parasitic effects in a three-phase multi-stage filter. The effectiveness of the three-phase filter structure employing the proposed methodologies has been validated in a 15kW rated motor drive system. Consequently, general design guidelines have been formulated for filter design with minimal parasitic effects.

Dedicated to my family

My Father: Yang-Min Chen

My Mother: Ya-Ling Wu

My sister: Ting-Yu Chen

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Table of Contents

Acknowledgements v

Table of Contents vii

List of Figures ix

Chapter 1 Introduction 1

1.1 Background 1
1.1.1 Effects of Parasitic Components 2
1.1.2 Prior Art: Self and Mutual Parasitic Cancellation Techniques 3
1.2 Research Objective 8
1.3 Thesis Organization 8

Chapter 2 Impact of Filter Parasitic Components 9

2.1 Introduction 9
2.1.1 Overview of the Three-Phase Three-Level Back-To-Back (B2B) Motor Drive 9
2.1.2 Overview of the System Simulation Model 12
2.2 Impact of the Individual Filter Components 17
2.2.1 Impact of the DM LCL Stage 17
2.2.2 Impact of the CM LCL Stage 21
2.3 Impact of Filter Interconnections 25
2.3.1 Impact of inductive couplings within the filter structure 25
2.3.2 Impact of capacitive couplings within the filter structure 30
2.3 Summary 37

Chapter 3 Design of B2B Converter Filter 39

3.1 Introduction 39
3.2 Design of Boost Inductor 39
3.2.1 Introduction 39
3.2.2 Proposed Winding Configurations 42
3.2.3 Experimental Verification 48
3.3 Design of the Full Filter Structure 51

3.3.1 Design of CM LCL Filter Stage 51
3.3.2 Design of Ground Connections and PCB Layout 57
3.4 Summary 63
Chapter 4 Experimental Evaluation of Improved Filter Design 65
4.1 Introduction 65
4.2 Experimental Results 67
4.2.1 Inductive Coupling Validation 67
4.2.2 Capacitive Coupling Validation 71
4.2.3 Self-Parasitic Components Validation 73
4.3 Filter Performance Comparison 78
4.4 Summary 81
Chapter 5 Summary, Conclusion and Future Work 83
5.1 Summary 83
5.2 Conclusion 84
5.2 Future Work 86
Appendix A. Parasitic Capacitance Extraction Procedure for a 3L-NPC converter modules 87
Bibliography 93

List of Figures

Fig. 1.1 EMI noise propagation path in a motor drive system 1

Fig. 1.2 IEC–61800-3-12 class A standard for conducted emissions at the grid terminal . 2

Fig. 1.3 (a) Typical one-stage DM EMI filter (b) DM EMI equivalent model including parasitic components 3

Fig. 1.4 DM insertion gain of the filter 3

Fig. 1.5 ESL cancellation schemes (a) X capacitor network (b) Coupled magnetic windings 4

Fig. 1.6 PCB implementation of ESL cancellation schemes (a) X capacitor network (b) Coupled magnetic windings 5

Fig. 1.7 EPC cancellation schemes (a) Seperate DM inductors (b) CM inductors............ 6

Fig. 1.8 Magnetic Coupling Cancellation Scheme (a) Rotate Inductor Windings (b) Add cancellation inductor turn. 7

Fig. 1.9 Electric coupling cancellation scheme (a) Create PCB slits (b) Insert electric shield 7

Fig. 2.1 State of the art B2B system under consideration 10

Fig. 2.2 Filter topology under study 11

Fig. 2.3 Schematic of the three-phase B2B motor drive system with high-frequency parasitic models for converter, filter, long cable, and motor. 12

Fig. 2.4 (a) Schematic of the 3L-NPC phase leg module (b) Top and lateral cross-section view inside the module. 13

Fig. 2.5 Measured and analytical impedance response of filter subcomponents: (a) $L_{cm1/2,grid}$, (b) Boost inductor $L_{dm1,grid}$, and (c) 15 m long unshielded cable. 15

Fig. 2.6 Simplified equivalent circuit for frequency-domain simulations (a) DM circuit (b) CM circuit 17

Fig. 2.7 Schematic of the DM LCL filter stage with three-phase grid-tied rectifier. 18

Fig. 2.8 Transfer Gain for DM L and DM LCL Filter (a) CM transfer gain (b) DM transfer gain 19

Fig. 2.9 Effect of f_{res4} corresponding to C_{tim} 20

Fig. 2.10 Simulated DM and CM noise voltage spectrum at the LISN terminal............. 20

Fig. 2.11 Schematic of the full filter stage with three-phase grid-tied rectifier. 21
Fig. 2.12 CM Transfer Gain for CM LCL Stage 22
Fig. 2.13 Impact of the parasitic inductance on the CM capacitor branch (a) Impact of ESL_{Cdm2} (b) Impact of ESL_{Ccm} (c) Impact of L_{gnd} (d) Parasitic components on the shunt capacitor branch 23
Fig. 2.14 Simulated CM noise voltage spectrum at the LISN terminal 24
Fig. 2.15 Impact of the ground impedance with full filter 25
Fig. 2.16 (a) Schematic of the full filter labeling the critical inductive couplings. (b) Baseline filter prototype. 26
Fig. 2.17 Equivalent circuit for inductive coupling (a) M_1 (b) M_2 28
Fig. 2.18 Impact of the mutual inductive coupling (a) Impact of M_1 (b) Impact of M_2 ... 29
Fig. 2.19 (a) Schematic of the full filter labeling critical capacitive coupling. (b) Baseline filter prototype. 31
Fig. 2.20 Impact of the mutual capacitive coupling (a) C_{coup1} (b) C_{coup2} 32
Fig. 2.21 Equivalent circuit for T-type capacitive coupling 33
Fig. 2.22 Impact of electric coupling with full filter 34
Fig. 2.23 PCB layout of the baseline grid-side filter. 35
Fig. 2.24 Schematic of the full filter with capacitive coupling from PCB traces to PCB ground plane 35
Fig. 2.25 Impact of the capacitive coupling from PCB traces to PCB ground plane 36
Fig. 2.26 Simulated CM noise at the LISN terminal with full filter 36
Fig. 3.1 Generalized FEA based Modeling Technique for Boost Inductor 41
Fig. 3.2 Traditional two-layered boost inductor with sequential winding (a) Prototype (b) Energy and capacitance distribution 42
Fig. 3.3 Proposed single-layered edgewise wound boost inductor (a) Prototype (b) Energy and capacitance distribution 43
Fig. 3.4 Hardware construction of the proposed single-layered edgewise wound boost inductor 44
Fig. 3.5 Proposed two-layered zig-zag PCB wound boost inductor (a) Prototype (b) Energy and capacitance distribution 45
Fig. 3.6 Proposed two-layered zig-zag winding configuration using planar PCB 46

Fig. 3.7 PCB stackup of the proposed two-layered 'zig-zag' winding configuration 47
Fig. 3.8 Simulated impedances for the proposed boost inductor solutions 47
Fig. 3.9 Constructed prototype of the proposed boost inductor solutions 48
Fig. 3.10 Three phase 3L PFC rectifier test bed 48
Fig. 3.11 Impedance measurements for the proposed boost inductor solutions 49
Fig. 3.12 Noise Spectrum Comparison 50
Fig. 3.13 Capacitor paralleling configurations 52
Fig. 3.14 LC test setup and test cases under study.. 53
Fig. 3.15 Voltage gain comparison 53
Fig. 3.16 Simulation of the LC setup 54
Fig. 3.17 LCL test setup and test cases under study 55
Fig. 3.18 (a) Voltage gain comparison (b) Geometry of the CM choke 55
Fig. 3.19 Voltage gain comparison 56
Fig. 3.20 (a) Split wound structure (b) Voltage gain comparison 57
Fig. 3.21 Simulation of the magnetic field distribution 57
Fig. 3.22 Schematic and structure of the full-scale grid-side filter.................................. 58
Fig. 3.23 Structure of daughter board 1 (DB1) 59
Fig. 3.24 Daughter board 1 PCB layout (a) Top Layer (red) (b) Second Layer (purple) (c) Third Layer (sky blue) (d) Fourth Layer (brown) (e) Bottom Layer (blue) (f) Layer stack-up 60
Fig. 3.25 (a) Structure of Daughter board 2 (DB2) (b) DB2 Top Layer (red) (c) DB2 Bottom Layer (blue) (d) Layer stack-up 61
Fig. 3.26 Mother board PCB layout (a) Top Layer (red) (b) Second Layer (brown) (c) Third Layer (sky blue) (d) Fourth Layer (blue) (e) Layer stack-up.......................... 62
Fig. 3.27 Filter grounding structure 63
Fig. 4.1 Schematic of the three-phase motor drive test bed... 65
Fig. 4.2 System test setup with grid-side CM LCL filter... 67
Fig. 4.3 Orientation under investigation (a) Side by side (b) Perpendicular (c) Vertical. 68
Fig. 4.4 DM noise comparison for CM choke orientations (phA).................................. 68
Fig. 4.5 DM noise comparison for CM choke orientations (a) phase B (c) phase C 69

Fig. 4.6 (a) DM noise comparison for introducing magnetic shield between the CM chokes (b) Structure of the CM chokes with shielding sheet.................................. 70
Fig. 4.7 (a) Structure of the shielding sheet in the full-scale grid-side filter (b) CM noise comparison for introducing electric shield between the boost inductor and the CM LCL filter stage.. 72
Fig. 4.8 System test setup with full grid-side filter.. 72
Fig. 4.9 CM noise comparison for PCB layouts with the full-scale grid-side filter using multi-layered traditional wound boost inductor.. 73
Fig. 4.10 EMI noise comparison for the winding configurations of the boost inductor with the full grid-side filter... 75
Fig. 4.11 Boost inductor impedance measurement... 75
Fig. 4.12 Film capacitor impedance measurements.. 76
Fig. 4.13 System test setup with grid-side DM LCL filter 76
Fig. 4.14 EMI noise comparison for paralleling multiple film capacitors with DM LCL filter.. 78
Fig. 4.15 (a) Baseline Filter (C_{dm2}/ C_{cm} placed on bottom side) (b) Redesigned Filter (C_{dm1} placed on bottom side). 79
Fig. 4.16 EMI emission comparison... 80
Fig. A.1. Proposed extended DPT (eDPT) circuit 87
Fig. A.2. Extended DPT Circuit under different switching cases. 89
Fig. A.3. Additional eDPT configurations for parasitic extraction............................. 91

Chapter 1 Introduction

1.1 Background

With the advent of wide band gap devices, the electromagnetic interference (EMI) emissions are more pronounced due to high slew rates in the form of high dv/dt and high di/dt at higher switching frequencies [1-3]. Fig. 1.1 shows the EMI propagation path in a motor drive system with a three-level (3L) back-to-back (B2B) neutral-point-clamped (NPC) converter topology. The differential mode (DM) noise flows between the power lines while the common mode (CM) noise flows between the power lines and the ground via the parasitic capacitances at the converter switching nodes.

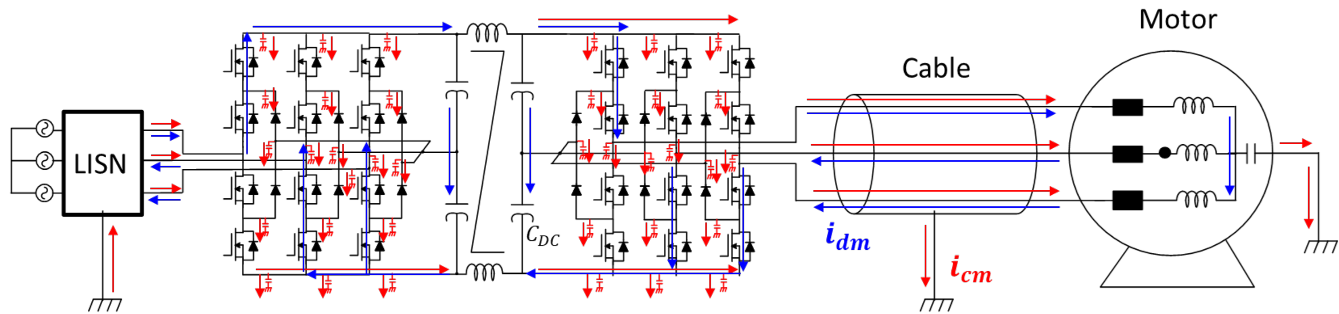


Fig. 1.1 EMI noise propagation path in a motor drive system

The IEC-61800-3 standard specifies the electromagnetic compatibility (EMC) requirements for industrial variable speed drives (VSDs). This work follows the C2 (industrial) emission levels for the grid interface per CISPR-11 regulations, as shown in Fig. 1.2. To comply with the conducted emission requirements at the grid terminal, EMI filter is mandatory to attenuate the high frequency CM and DM noise that flows into grid [4, 5]. However, near field and the effect of parasitic components are known to create issues with the high frequency performance of filters [6-8].

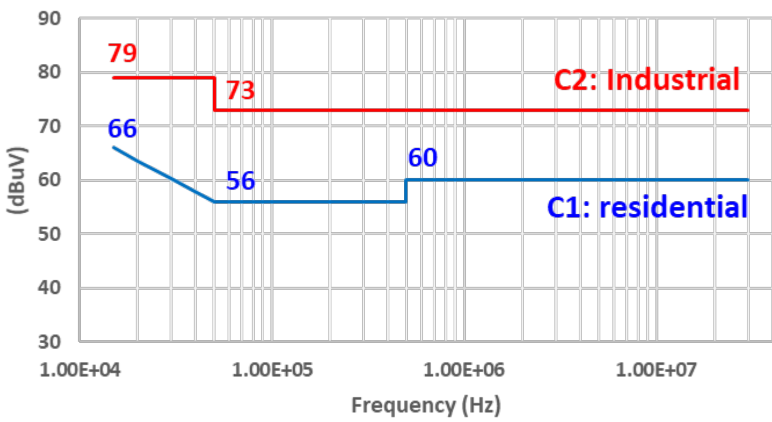


Fig. 1.2 IEC–61800-3-12 class A standard for conducted emissions at the grid terminal

1.1.1 Effects of Parasitic Components

Ref. [6-8] demonstrates the impact of the self and mutual parasitic components on the degradation of a typical one-stage DM EMI filter shown in Fig. 1.3 (a). The filter equivalent model considering the parasitic components is shown in Fig. 1.3 (b). Fig. 1.4 shows the insertion voltage gain of the filter, where the insertion gain is defined as the voltage at the load terminal (V_2) with the filter over the voltage at the load terminal without the filter. Both the load and source impedance are 50 Ω in simulation and measurement of the insertion gain. The DM EMI filter provides a 60 dB/decade attenuation after the corner frequency when ideal filter components are considered. However, the insertion gain starts to increase at high frequency when the equivalent series inductance (ESL) of the DM capacitors and the equivalent parallel capacitance (EPC) of the DM inductor are included in the simulation. In other words, the DM filter provides a weaker attenuation at high frequency when the self-parasitic components are considered. Furthermore, the insertion gain is getting even higher at lower frequency in the real measurement when the mutual parasitic coupling components are included, meaning more high frequency DM noise will directly flow through the power grid instead of being attenuated by the DM filter. Therefore, techniques to reduce or even eliminate the

self and mutual parasitic components should be introduced to improve the filter high frequency performance.

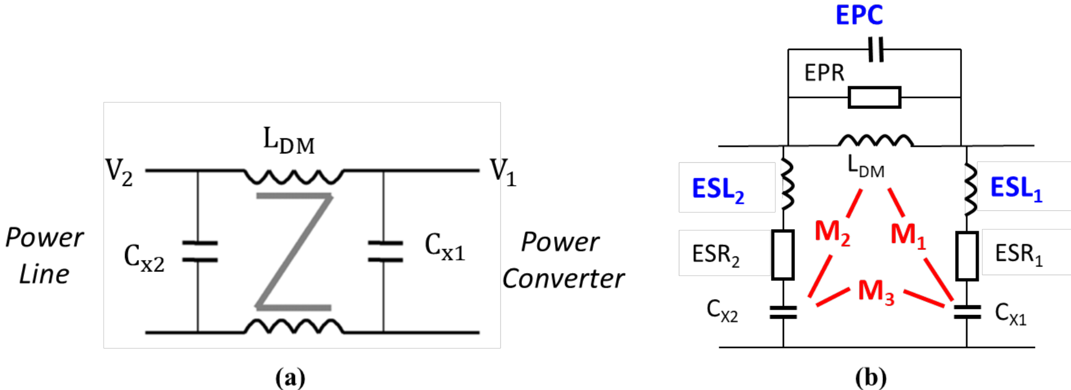


Fig. 1.3 (a) Typical one-stage DM EMI filter (b) DM EMI equivalent model including parasitic components

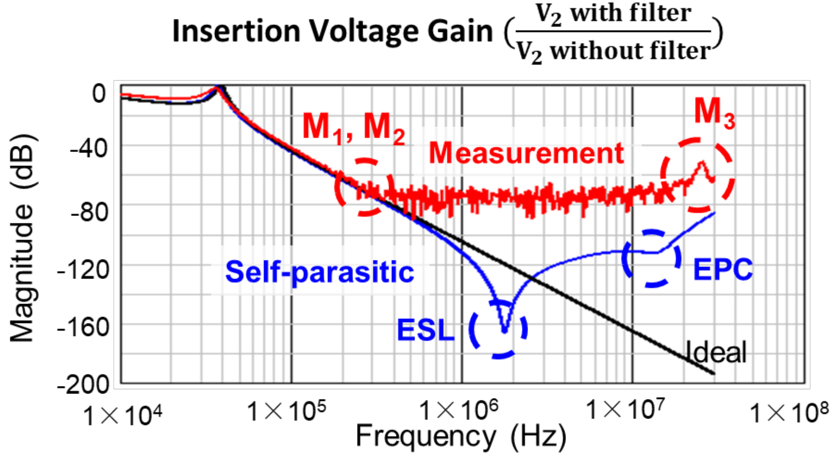


Fig. 1.4 DM insertion gain of the filter

1.1.2 Prior Art: Self and Mutual Parasitic Cancellation Techniques

In prior literature, cancellation techniques for both self and mutual parasitic parameters are discussed at length to improve the performance of EMI filters. For example, [8, 9] connects two DM capacitor in an 'x' configuration and introduces two inductors in between the two capacitor branches to cancel the ESL of the DM capacitor, as shown in Fig. 1.5 (a). The ESL of the DM

capacitor is effectively cancelled out when the introduced inductance equals to the ESL of the DM capacitor. Ref. [10-12] introduces a three-terminal coupled magnetic windings where the coupling between the coils on two terminals generates a negative inductance on the third terminal to compensate the ESL of the capacitor at that terminal, as shown in Fig. 1.5 (b). Both the cancellation inductors and the coupled windings could be implemented as a part of the filter printed circuit board (PCB) under the capacitors, as shown in Fig. 1.6.

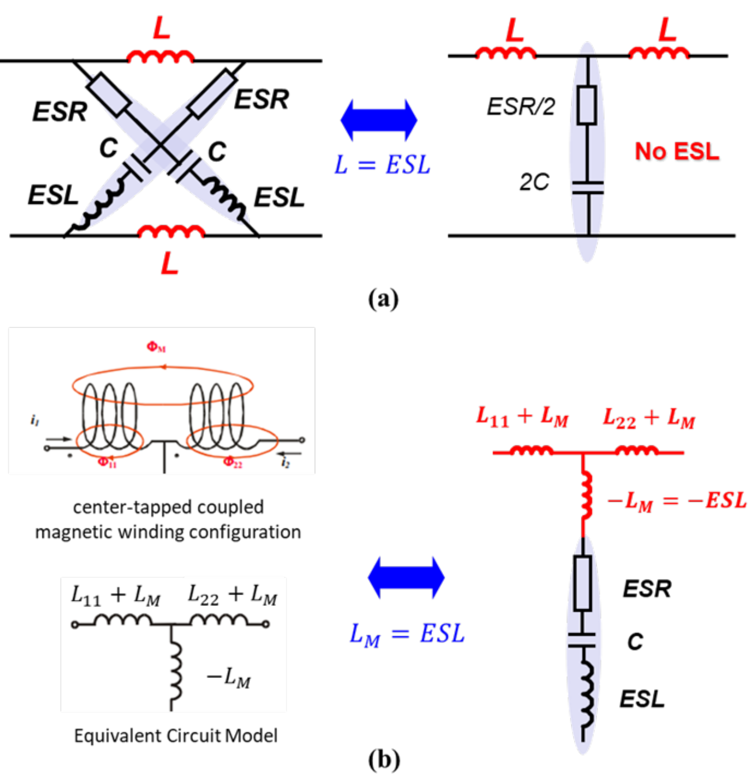


Fig. 1.5 ESL cancellation schemes (a) X capacitor network (b) Coupled magnetic windings

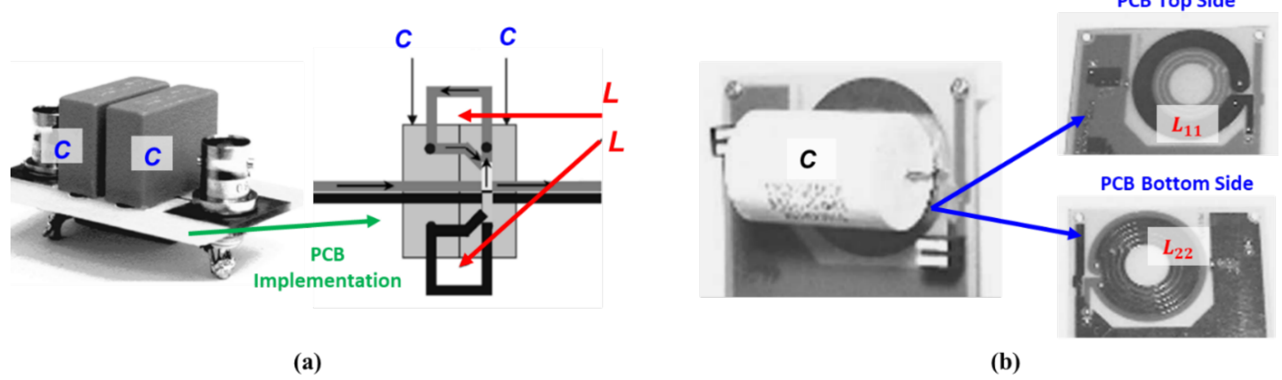


Fig. 1.6 PCB implementation of ESL cancellation schemes (a) X capacitor network (b) Coupled magnetic windings

Ref. [8, 13] discusses the EPC cancellation technique for both CM and DM inductors. Two discrete capacitors are introduced in a crisscross fashion between the input and output of the separate DM inductors, as shown in Fig. 1.7 (a). The EPC of the DM inductor is effectively cancelled out when the introduced capacitance equals to the EPC of the DM inductor. The EPC of the CM inductors are cancelled by introducing discrete capacitors from the center taps of windings to ground, as shown in Fig. 1.7 (b). Similarly, the EPC of the CM inductor is effectively cancelled out when the introduced capacitance equals to the 4 × EPC of the CM inductor.

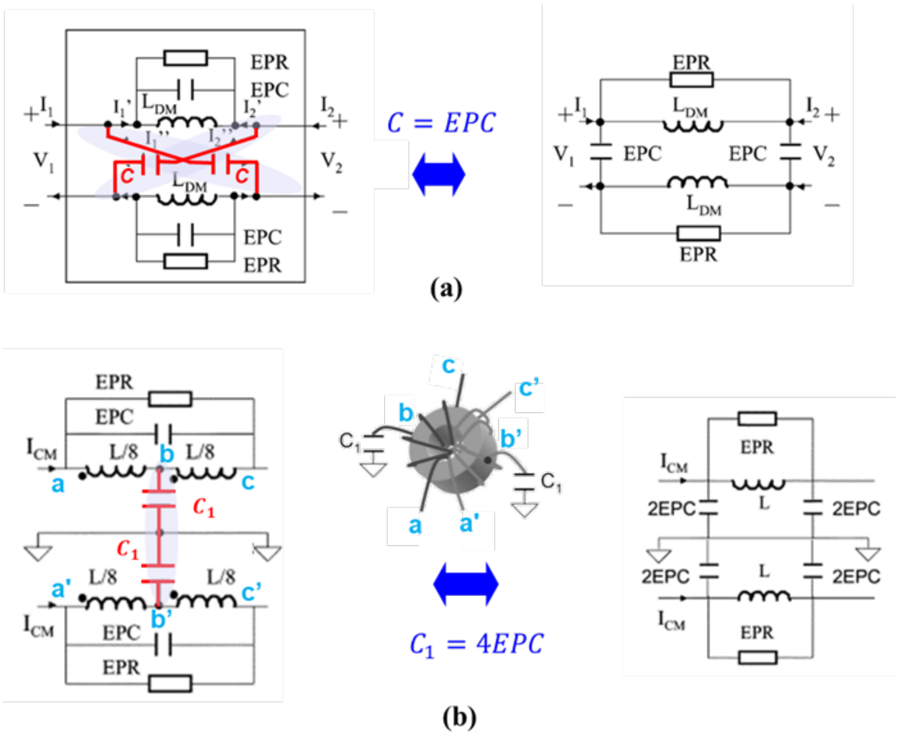
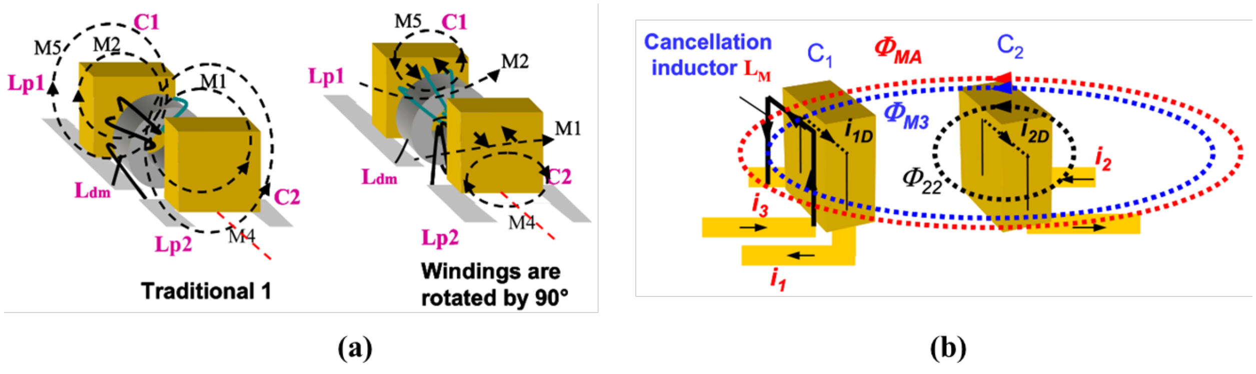


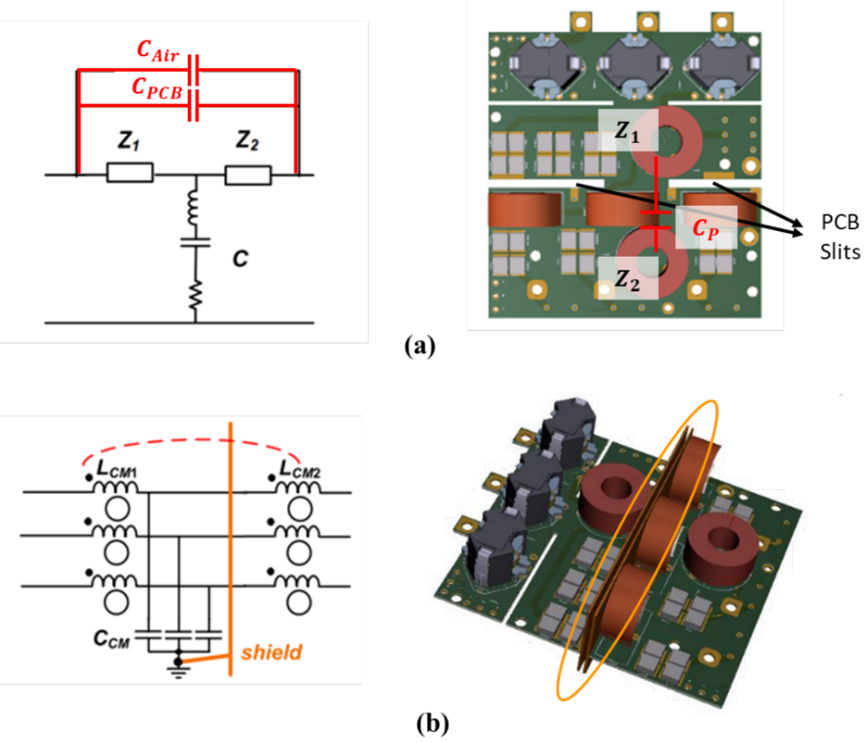
Fig. 1.7 EPC cancellation schemes (a) Seperate DM inductors (b) CM inductors

Ref. [6-8] demonstrates the impact of component placement and orientation to cancel the mutual inductive coupling in the DM EMI filter, as shown in Fig. 1.8. In Fig. 1.8 (a), the inductor winding is rotated by 90° to reduce the magnetic coupling between the inductor and the capacitor. In Fig. 1.8 (b), a cancellation turn (L_M) is integrated in series with one of the capacitors with an opposite current direction to cancel the mutual inductance between the two capacitors (Φ_{M3}). Ref. [14, 15] discusses the detrimental mutual capacitive coupling in a T-shaped filter network. PCB slits are created between the two inductors to reduce the mutual capacitance through the FR4 medium (C_{PCB}), as shown in Fig. 1.9 (a). Electric shield is also inserted in between the two inductors and tied to ground to reduce the electric field penetrating from one inductor to the other, as shown in Fig. 1.9 (b).



(a) (b)

Fig. 1.8 Magnetic Coupling Cancellation Scheme (a) Rotate Inductor Windings (b) Add cancellation inductor turn.



(a)

(b)

Fig. 1.9 Electric coupling cancellation scheme (a) Create PCB slits (b) Insert electric shield

The effectiveness of the aforementioned cancellation schemes is validated through experiments, where improved high frequency performance of the filter is observed. However, so far literature has focused mainly on low power, single-phase applications. For three-phase high-power systems, several limitations should be considered when applying the above techniques. For instance, the thermal issue arises due to the high winding losses contributed by the introduced PCB windings or cancellation turns for high current applications. The physical layout is limited by

creepage and clearance requirements for enough isolation in high voltage applications. In addition, instead of the complexity to implement the cancellation network for three-phase applications, the cross-coupling between phases could results in a much severe CM to DM mode conversion during cancellation compared to single-phase systems. As such, this thesis focuses on extending the pre-existing concepts to three-phase high-power systems. Novel placement and winding techniques are developed to compensate for parasitic components in these systems.

1.2 Research Objective

The goal of this work is to develop an optimized filter structure with compensated parasitic effects for a 15 kW three-phase motor drive system. The key aspect is to identify the impact of the parasitic parameters on the degradation of the filter performance and seek to minimize the self and mutual parasitic resistances, inductances, and capacitances, both at the component and filter levels. The filter should meet the power quality as well as the electromagnetic compatibility (EMC) requirements specified by the IEC-61800-3 guideline.

1.3 Thesis Organization

The work is organized as follows. Chapter 2 investigates the impact of the parasitic parameters on the filter performance using the high-frequency passive component models in Matlab Simulink environment. Chapter 3 carries out a detailed design procedure of the critical parameters identified from the conducted emissions simulations. Finally, a full-scale filter structure employing the proposed methodologies in the redesign process is constructed and tested for validation in the Chapter 4. Chapter 5 concludes the thesis and highlights the potential topics that could be worked on in the future.

Chapter 2 Impact of Filter Parasitic Components

2.1 Introduction

This chapter investigates the impact of the various parasitic components of the three-phase multi-stage filter. Time domain simulations are conducted using the high-frequency passive component models developed per [16] to evaluate the filter performance. Frequency domain simulations are also carried out for a further understanding of the filter behavior. Based on the simulation results, the main physical components having a significant impact on the high-frequency emissions are identified. These critical passive components will be optimized as a part of the filter design process in Chapter 3.

2.1.1 Overview of the Three-Phase Three-Level Back-To-Back (B2B) Motor Drive

The three-phase B2B ac-to-ac motor drive system under study is shown in Fig. 2.1. The system specification is listed in Table 2-1. Two three-phase converter units are arranged in a B2B configuration to form the bidirectional ac-ac converter stage that feeds the electric motor through a 15 m unshielded three-phase cable. Three-level (3L) SiC NPC module [17] has been selected to build the converter unit due to relatively lower filter volume compared to the two-level structures. State of the art filter structures [17-41] have demonstrated the use of the 3L-NPC module to develop enhanced and alternative filter building block architectures. Active front-end control (using outer voltage loop and inner current control loops) and V/f control are adopted as the control strategy for the rectifier stage and the inverter stage respectively. The carrier based sinusoidal PWM with third harmonic injection is implemented as the modulation scheme for both the inverter

and rectifier. The modulation index is defined in Table 2-1, where $V_{(1)}^{ref}$ represents the peak value of the fundamental modulating waveform.

Table 2-1 System Parameters

Parameters	***Value***
Power Rating	15 kW
Line Voltage	400 *VAC*
DC-Bus Voltage	650 V
Line Frequency	60 Hz
Switching Frequency	48 kHz
MI_{grid} ($2V_{grid(1)}^{ref}/V_{dc}$)	0.87
MI_{inv} ($2V_{inv(1)}^{ref}/V_{dc}$)	0.99 at rated speed

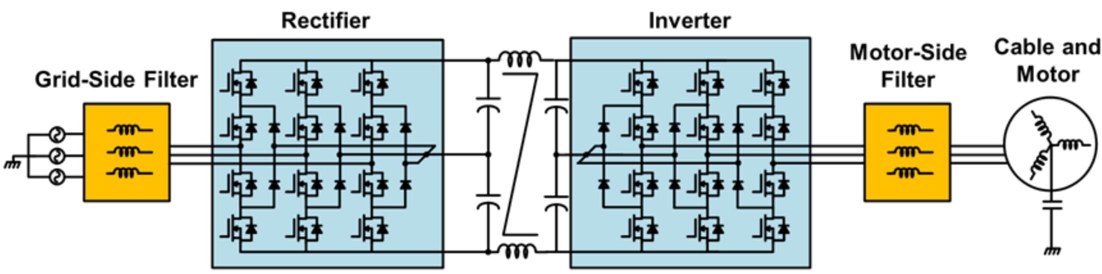


Fig. 2.1 State of the art B2B system under consideration

Fig. 2.2 shows the filter topology under study. A bridge interconnection is established between the star point of the grid-side filter and the motor-side filter to circulate and attenuate the low-frequency CM components within the B2B converter. Additional DC CM inductor ($L_{cm, dc}$) is introduced between the rectifier and the inverter to further suppress the low frequency CM components within the loop during start-up. Since the bridge interconnection only shows improvement for low-frequency attenuation [16], the grid side CM LCL stage ($L_{cm1, grid}$, $L_{cm2, grid}$, and $C_{cm, grid}$) is added to suppress the high-frequency CM components. The grid side DM LCL filter components ($L_{dm1, grid}$, $L_{dm2, grid}$, and $C_{dm1, grid}$) are designed for power quality requirement, reactive power compensation and DM EMI compliance purposes respectively. The motor side DM LC filter is added to mitigate the reflected wave from the long cable. The filter parameters are selected based on the design flow per [16] to meet the IEC-61800-3 conducted emission standard.

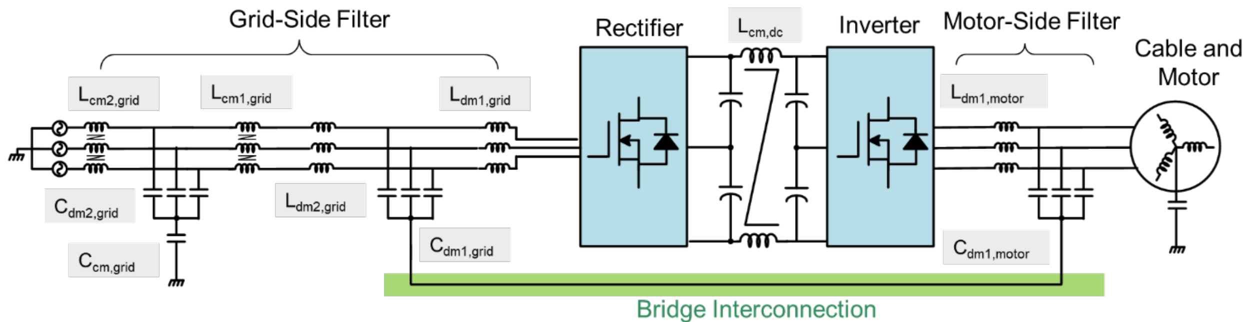


Fig. 2.2 Filter topology under study

Powder cores are used for inner loop magnetics {$L_{dm1,\ grid}$ and $L_{dm1,\ motor}$} to attenuate the high-frequency switching ripple and bridge current at the converter output due to their superior core loss characteristics and lower fringing field effects while iron-amorphous core is selected for outer loop DM inductors {$L_{dm2,\ grid}$} due to its high saturation flux density limit. Nanocrystalline toroidal cores are adopted for CM inductors {$L_{cm1,\ grid}$, $L_{cm2,\ grid}$ and $L_{cm,\ dc}$} due to their high inductance characteristics per unit volume. The physical parameters of the prototype are summarized in **Error! Not a valid bookmark self-reference.**. This work focuses on minimizing the parasitic effects on the grid side filter.

Table 2-2 3L-NPC Prototype and B2B Components

Component	***Value***	***Details***
Semiconductors	f_{sw} = 48 kHz	Microchip, SiC 3L-NPC Phase Leg, APTMC603LCT3AG, 1.2 kV, 48 A
Grid-Side Components	$L_{dm1,\ grid}$ = 100 µH	Powder Core, EMS-0432115-040 (2X), n = 25, A_e = 366 mm^2 , AL = 216 nH/T^2
	$L_{dm2,\ grid}$ = 50 µH	Amorphous, 2xE cores clamped l_g = 1 mm, n = 4, A_e = 450 mm^2
	$L_{cm1,\ grid}$ = 300 µH	Nanocrystalline, FT-3KM F4535G (2X), A_L = 4.1 µH/T^2 , n = 3, A_e = 300 mm^2
	$L_{cm2,\ grid}$ = 300 µH	Nanocrystalline, FT-3KM F4535G (2X), A_L = 4.1 µH/T^2 , n = 3, A_e = 300 mm^2

	$C_{dm1, grid}$ = 2 μH	Film capacitor, B32754C8205K000, 350 VAC, 2 μF (Same spec for $C_{dm2, grid}$)
Inverter Side Components	$L_{dm1, motor}$ = 50 μH	Powder Core, EMS-0432115-040, n = 25, A_e = 183 mm^2 , A_L = 108 nH/T^2
	$C_{dm1, motor}$ = 2 μH	Film capacitor, B32754C8205K000, 350 VAC, 2 μF
DC Side Components	$L_{cm1, dc}$ = 300 μH	Nanocrystalline, FT-8K50D F4535G, n = 6, A_L = 21 μH/T^2

2.1.2 Overview of the System Simulation Model

To study the impact of the filter parasitic components on the high-frequency emissions, wide-band frequency models for the filter components [42-45], three-level B2B converter [46, 47], unshielded long cable [48-52], and the electrical motor [49, 51] are incorporated in the system simulation model to predict the CM and DM noise. Fig. 2.3 shows the schematic of the motor drive system with the high-frequency lumped parasitic models derived in [16].

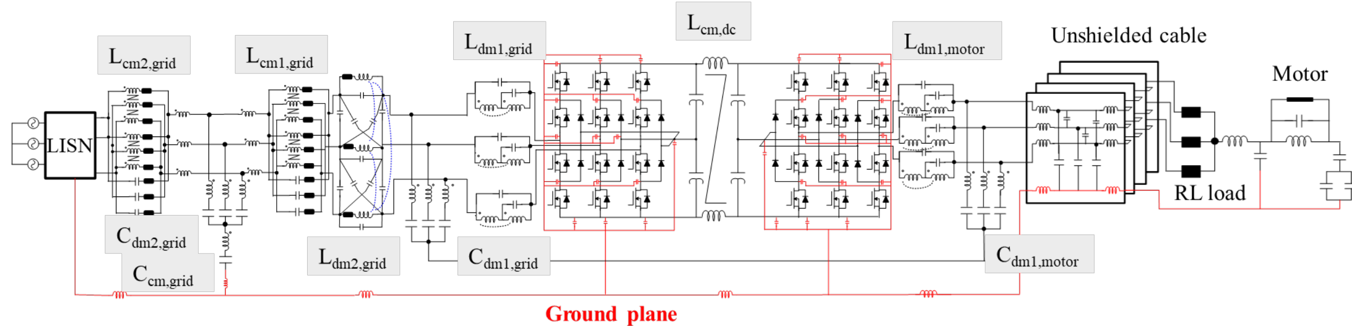


Fig. 2.3 Schematic of the three-phase B2B motor drive system with high-frequency parasitic models for converter, filter, long cable, and motor.

The high frequency lumped model for the 3L-NPC phase-leg module with parasitic elements under consideration is shown in Fig. 2.4 (a). Fig. 2.4 (b) shows the internal structure of the module. C_{px} ($x \in$ 1-6) represents the parasitic capacitance between module terminals to module baseplate while C_{tim} represents the external thermal interface material (TIM). The nodal parasitic

capacitances are extracted via the methodology discussed in Appendix A. The stray inductances of the bond wires are estimated according to their geometry while the bus-bar stray inductances are extracted by quasi-static models using finite element analysis (FEA) simulation tool.

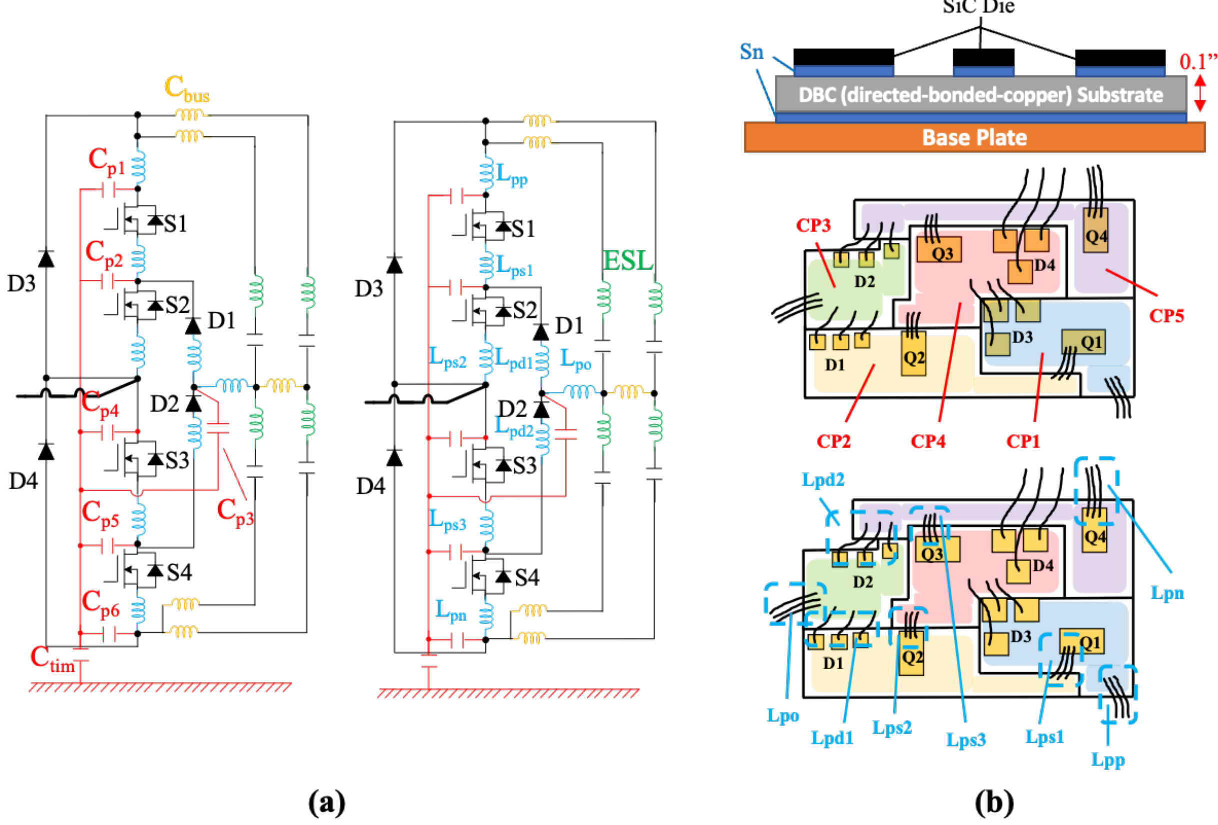


Fig. 2.4 (a) Schematic of the 3L-NPC phase leg module (b) Top and lateral cross-section view inside the module.

The parasitic parameters in the lumped models for the selected passive components are listed in Table 2-3. For three phase AC CM inductors $\{L_{cm1, grid}$ and $L_{cm2, grid}\}$, multiple RL segments in parallel (L_1, L_2, R_1, R_2) are used to represent the frequency dependent effect of permeability in time-domain while C_3 are used to represent the equivalent lumped capacitance including the static inter-turn and turn-core capacitances.

The two-layered boost inductor model are selected based on the analogy with the multi-winding transformer models [42, 53, 54]. L_3 and L_4 represents the inductance split between the

two layers considering a coupling coefficient k_1 between them. C_1 and C_2 are used to represent the equivalent lumped capacitance corresponding to the inner and outer layer respectively.

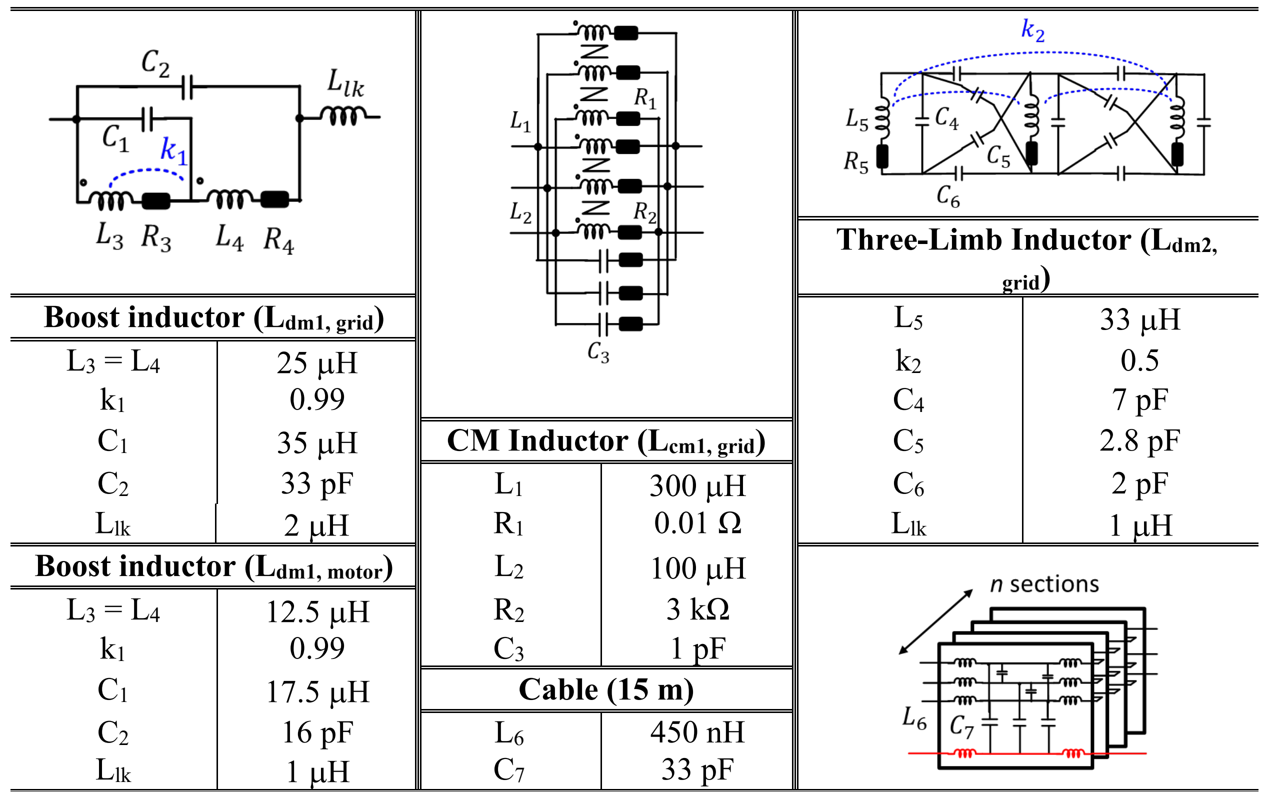
The three-limb DM inductor $\{L_{dm2, grid}\}$ model is inspired from the two winding capacitor model [42, 53, 54] where C_4, C_5 and C_6 is used to represent the cross coupled capacitances between the two adjacent phases while L_5 represents the inductance per phase considering a coupling coefficient k_2 between any two phases.

The cable model is extracted using cable modeling toolkit in ANSYS simulation environment and translated into a sectionalized lumped transmission line model [55]. This model can be scaled according to cable length, by tuning sectional (L_6, C_7) and the number of distributed section n. The motor model is derived from the existing induction motor impedance characteristic using the method proposed in previous work [49, 56].

The derivation of the passive components is discussed in detail in [16] and is therefore not covered in this thesis. The lumped models are verified through impedance measurements using Keysight impedance analyzer 4990A, as shown in Fig. 2.5.

Based on the full system model, time-domain simulations are performed to investigate the degradation of the filter performance according to the parasitic parameters in the Matlab Simulink environment. A virtual EMI test receiver with a 9 kHz resolution bandwidth is implemented to compute the LISN noise spectrum in the frequency range of interest (150 kHz – 30MHz).

Table 2-3 Passive lumped models and their parasitic values for the filters



Boost inductor ($L_{dm1, grid}$)	
$L_3 = L_4$	25 µH
k_1	0.99
C_1	35 µH
C_2	33 pF
L_{lk}	2 µH

Boost inductor ($L_{dm1, motor}$)	
$L_3 = L_4$	12.5 µH
k_1	0.99
C_1	17.5 µH
C_2	16 pF
L_{lk}	1 µH

CM Inductor ($L_{cm1, grid}$)	
L_1	300 µH
R_1	0.01 Ω
L_2	100 µH
R_2	3 kΩ
C_3	1 pF

Cable (15 m)	
L_6	450 nH
C_7	33 pF

Three-Limb Inductor ($L_{dm2, grid}$)	
L_5	33 µH
k_2	0.5
C_4	7 pF
C_5	2.8 pF
C_6	2 pF
L_{lk}	1 µH

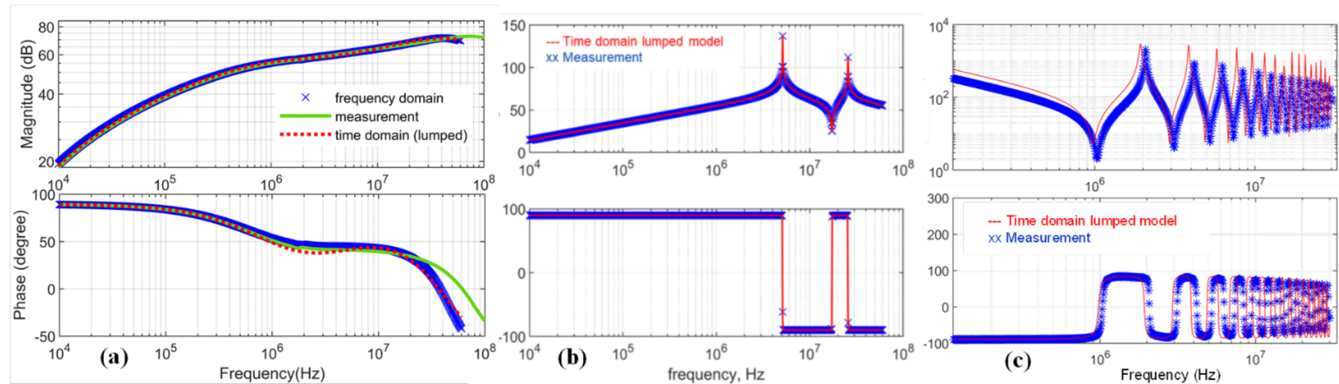


Fig. 2.5 Measured and analytical impedance response of filter subcomponents: (a) $L_{cm1/2,grid}$, (b) Boost inductor $L_{dm1,grid}$, and (c) 15 m long unshielded cable.

However, since the full system time domain simulations are time-consuming and require large computational resources [23, 57], frequency domain transfer gain analysis with only the rectifier and grid-side filter are conducted to have a general understanding on the sensitivity of the grid-

side filter components. Equation (2.1) shows the correlation between transfer gain and the noise spectrum at the LISN.

$$v_{lisn} = \frac{v_{lisn}(s)}{v_{rec}(s)} \otimes v_{rec}(s) \tag{2.1}$$

where the v_{rec} represents the Fast Fourier Transform (FFT) of the raw noise generated from the rectifier operation while v_{lisn} represents the voltage at the LISN terminal. In this case, v_{rec} and v_{lisn} are also the voltage at the input and output terminal of the grid-side filter. Clearly, the conducted EMI noise source is shaped by the transfer gain of the the grid-side filter.

Fig. 2.6 shows the DM equivalent model and CM equivalent model for frequency domain simulations. In the CM equivalent model, $C_{p,ac}$ and $C_{p,dc}$ represents the parasitic capacitances of the equivalent ac node and dc node to ground for the 3L-NPC module, which are extracted using the method discussed in [58, 59]. The noise generated by the rectifier is represented by small ac signal. The transfer gain is usually defined as the ratio of the voltage across the LISN to the small ac input signal as per (2.2)

$$\begin{cases} TF_{cm} = \frac{v_{lisn,cm}}{v_{cm}} = (\frac{1}{3} z_{lisn})(\frac{i_{lisn,cm}}{v_{cm}}) \\ TF_{dm} = \frac{v_{lisn,dm}}{v_{dm}} = (\frac{3}{2} z_{lisn})(\frac{i_{lisn,dm}}{v_{dm}}) \end{cases} \tag{2.2}$$

However, since the impedance of the LISN, namely Z_{lisn}, is constant within the frequency range of interest, the voltage across the LISN, v_{lisn}, is proportional to the current flowing through the LISN, i_{lisn}. Therefore, the ratio of the current flowing through the LISN over the small ac input signal is used to represent the transfer gain of equivalent filter circuit under study in this work. The transfer gain analysis is performed under LTSpice environment.

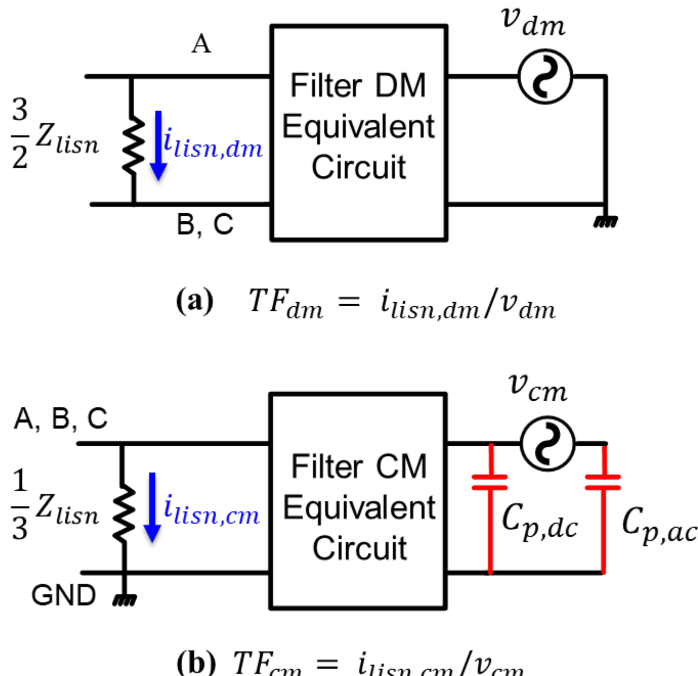


Fig. 2.6 Simplified equivalent circuit for frequency-domain simulations (a) DM circuit (b) CM circuit

2.2 Impact of the Individual Filter Components

In this section, the self-parasitic effect of the individual filter components is investigated based on the time-domain conducted emissions simulations as well as the frequency-domain transfer gain analysis.

2.2.1 Impact of the DM LCL Stage

The first stage DM-LCL filter is designed to meet the power quality and the conducted EMI standard at the LISN terminal. Fig. 2.7 shows the schematic of the DM LCL filter stage with three-phase grid-tied rectifier.

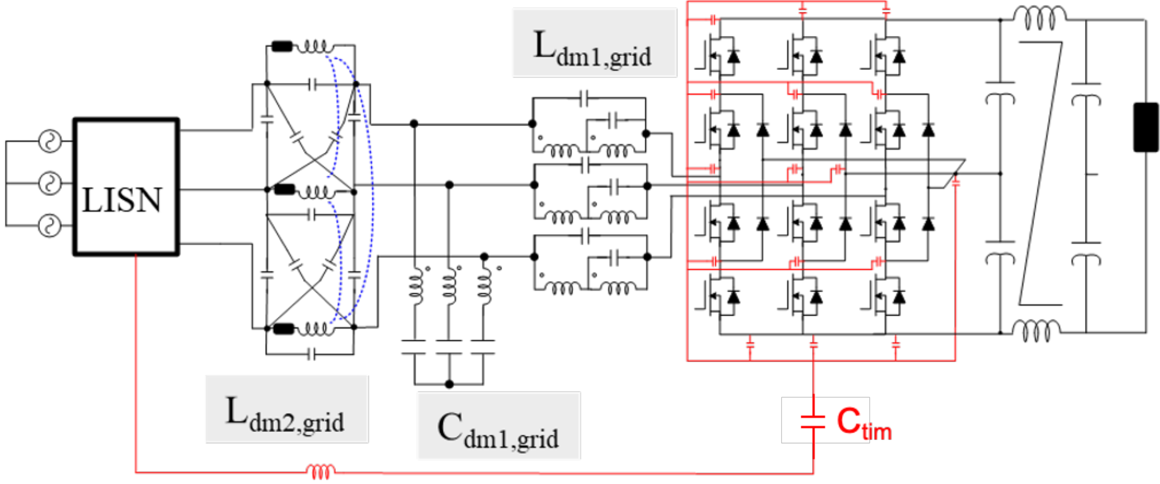


Fig. 2.7 Schematic of the DM LCL filter stage with three-phase grid-tied rectifier.

Fig. 2.8 shows the transfer gain of the DM L {L_{dm1}} and LCL filter {L_{dm1}, C_{dm1} and L_{dm2}}. The trend of the curve follows the inverted impedance profile of the L_{dm1} (also called the boost inductor), where the resonance f_{res1}, f_{res2} and f_{res3} can be correlated with the impedance peaks and valleys in Fig. 2.5. Clearly, the DM filter loses the ability to attenuate both CM and DM noise at high frequency due to the self-resonances of the boost inductor. It should be noted that the CM trace for DM L and DM LCL filter are overlapped. This is because the three-limb DM inductor {$L_{dm2,\ grid}$} does not produce impedance for CM current while the DM capacitor {$C_{dm1,\ grid}$} only circulates high frequency DM components. The propagation path for high frequency CM currents is thus identical for DM L filter and DM LCL filter. The resonance f_{res4} in the CM noise spectrum stems from the interaction between the boost inductor and the parasitic capacitance from the converter to ground. A larger parasitic capacitance from the base plate of the converter module to the system ground plane, C_{tim}, shifts the resonance f_{res4} to a lower frequency, as show in Fig. 2.9.

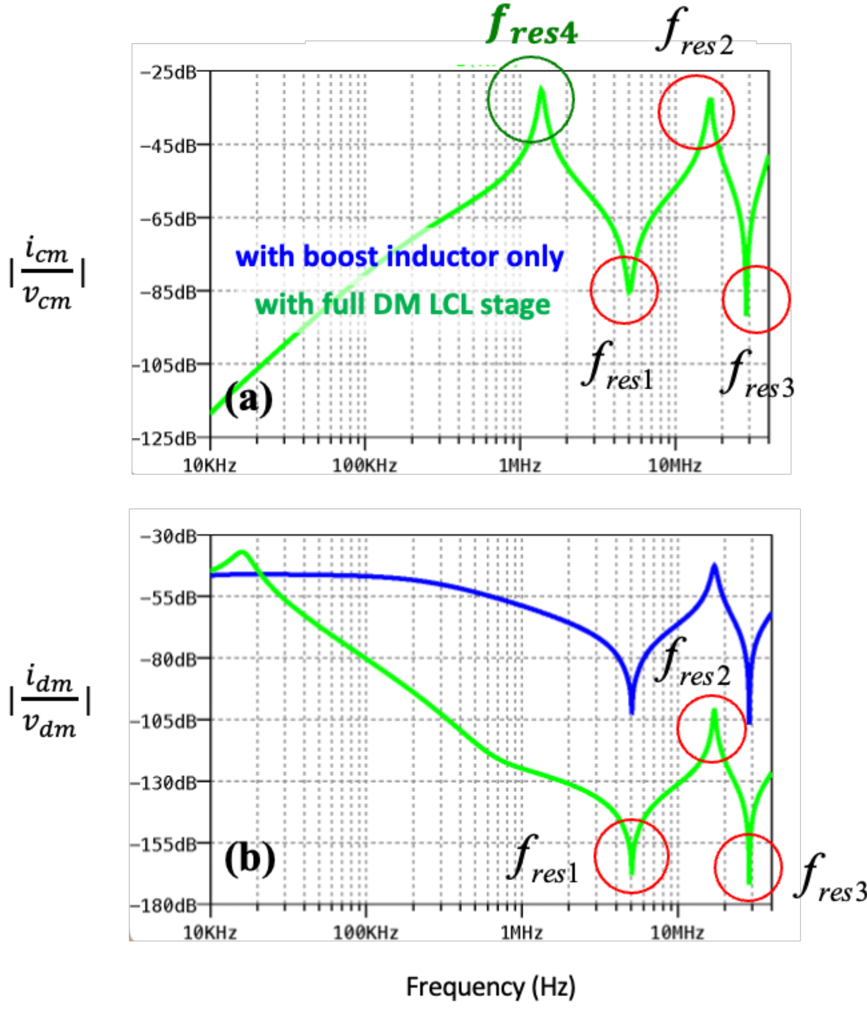


Fig. 2.8 Transfer Gain for DM L and DM LCL Filter

(a) CM transfer gain (the two curves are overlapped) (b) DM transfer gain

Fig. 2.10 shows the simulated conducted emissions at the LISN terminal. The valleys and peak in the simulated noise spectrum correlate well with the dominant resonances (f_{res1} – f_{res4}) in the transfer gain plots. In order to meet the emission standard at high frequency, the peaking of the noise emission at f_{res2}, which is correlated to the anti-resonance of the boost inductor, should be eliminated.

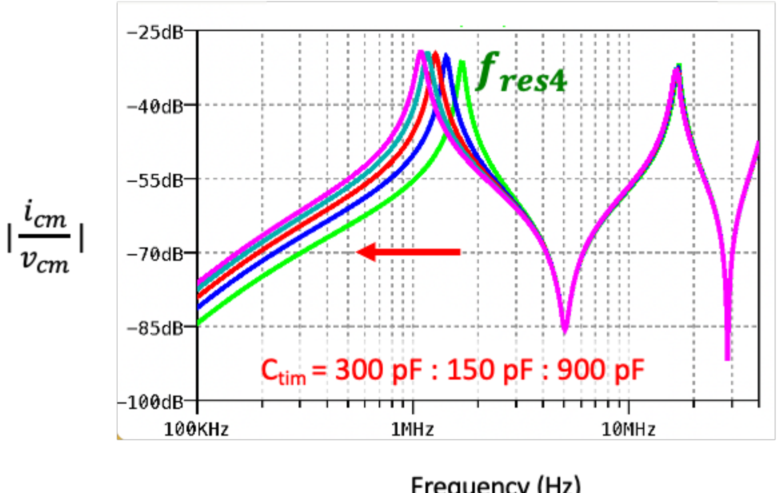


Fig. 2.9 Effect of f_{res4} corresponding to C_{tim}

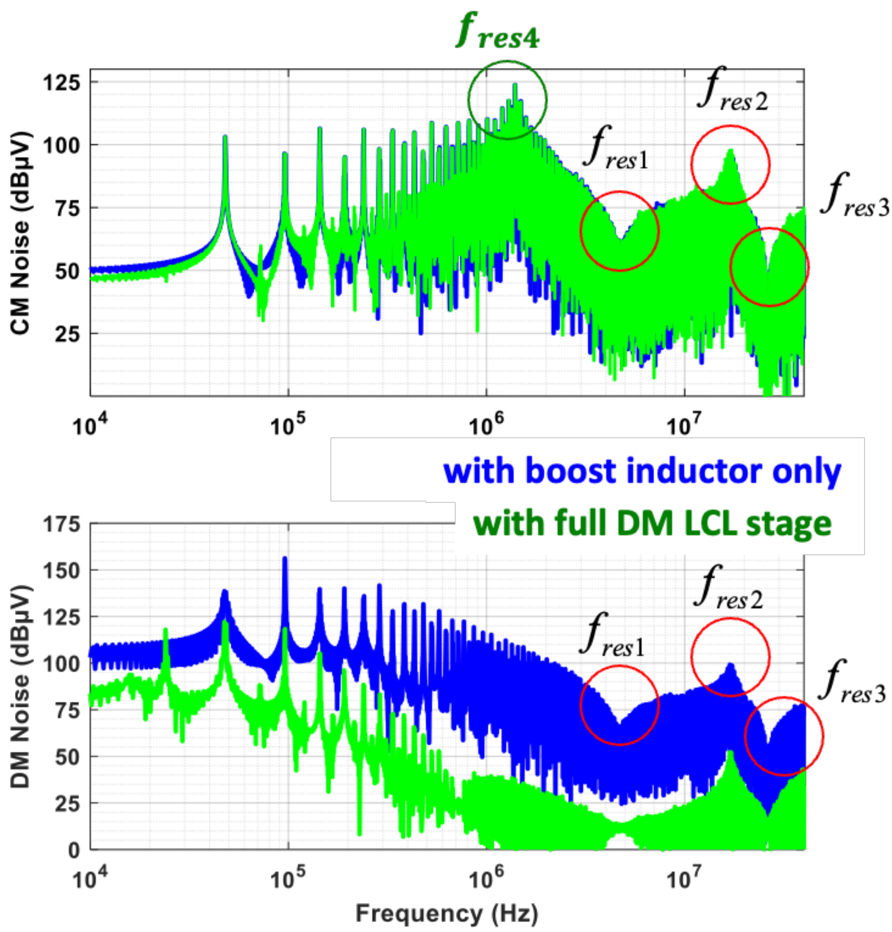


Fig. 2.10 Simulated DM and CM noise voltage spectrum at the LISN terminal

In summary, the anti-resonance of the boost inductor leads to the high conducted emission peak around the same frequency in both CM and DM spectrum. Therefore, the EPC of the boost inductor should be minimized to eliminate the anti-resonance effect up to 30 MHz.

2.2.2 Impact of the CM LCL Stage

The second stage CM-LCL filter is designed to meet the conducted EMI standard at high frequency. Fig. 2.11 shows the schematic of the full filter stage with three-phase grid-tied rectifier.

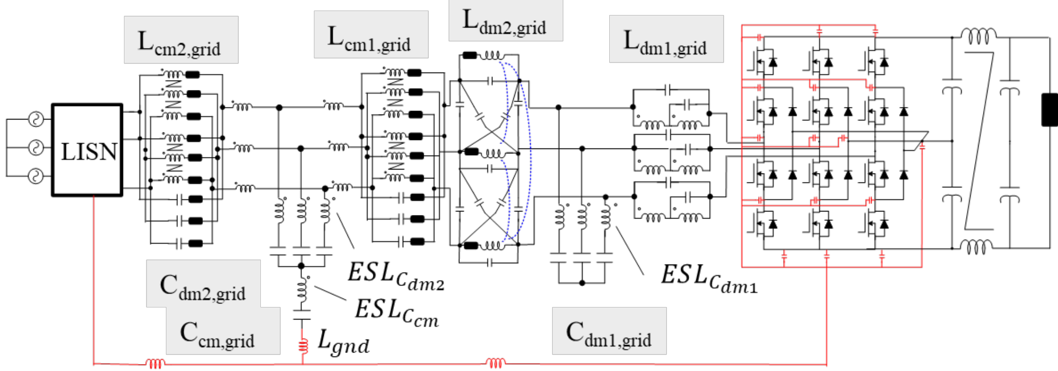


Fig. 2.11 Schematic of the full filter stage with three-phase grid-tied rectifier.

Fig. 2.12 shows the CM transfer gain at the LISN when the CM LL $\{L_{cm1}$ and $L_{cm2}\}$ and LCL $\{L_{cm1}, C_{dm2}, C_{cm}$ and $L_{cm2}\}$ filter stage are added to circuit. The red curve represents the CM transfer gain with only the DM LCL filter stage in the circuit while the green curve indicates the CM transfer gain when the CM chokes $\{L_{cm1}$ and $L_{cm2}\}$ are added in addition to the DM LCL filter stage. The resonance peaks f_{res2} and f_{res4} in the DM LCL filter stage has been damped when the CM chokes are introduced in the circuit. The blue curve shows the CM transfer gain with the full filter (CM LCL and DM LCL). The overall CM transfer gain has been decreased with an additional anti-resonance, namely f_{ESL}, showing up at 47 kHz. This frequency stems from the resonance of the net stray inductance and the equivalent capacitance on the shunt capacitor branch.

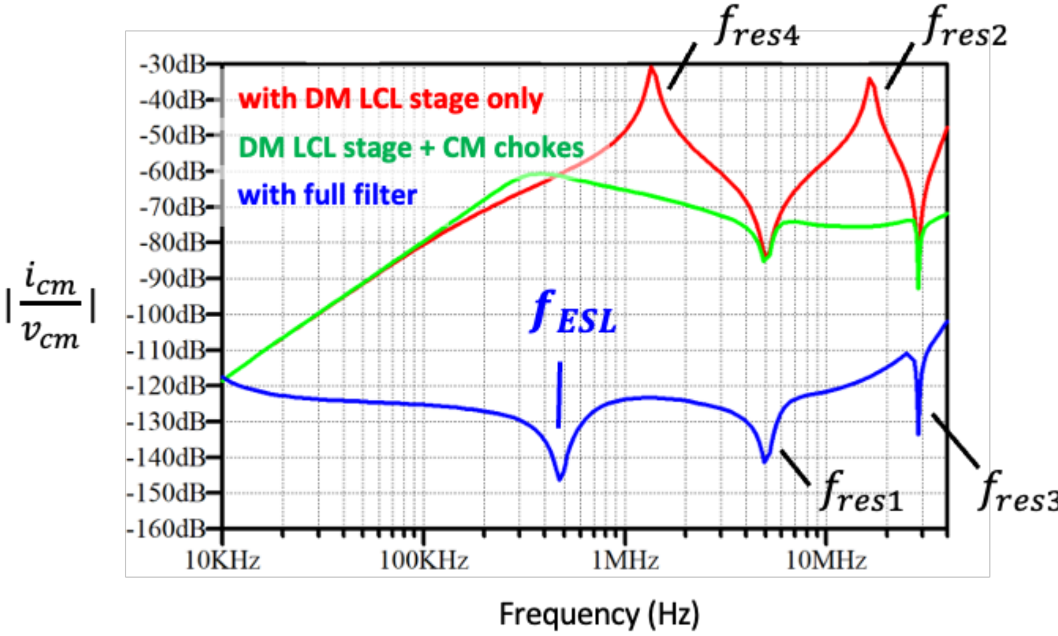


Fig. 2.12 CM Transfer Gain for CM LCL Stage

The net stray inductance of the on the shunt capacitor branch is contributed by the ESL of the C_{dm2}, the ESL of the C_{cm} as well as the stray inductance from the CM capacitor to the system ground plane (L_{gnd}), as shown in Fig. 2.13 (d). This anti-resonance f_{ESL} is given by the expression in (2.3).

$$f_{ESL} = 1 \Big/ 2\pi\sqrt{\left(\frac{ESL_{C_{dm2}}}{3} + ESL_{C_{cm}} + L_g\right)\left(\frac{C_{dm2}}{3} + C_{cm}\right)} \tag{2.3}$$

In the simulation, the ESL of capacitors C_{dm2} and C_{cm} are 25 μH while the ground inductance L_{gnd} is assigned to be 20 μH. Fig. 2.13 shows the impact of the stray inductance on the shunt capacitor branch. With a higher parasitic inductance, the anti-resonance f_{ESL} is shifting to a lower frequency and thus results in a higher gain after the resonant point. Therefore, the net ESL of the CM capacitor branch should be minimized to obtain a reduce the CM transfer gain at high frequency.

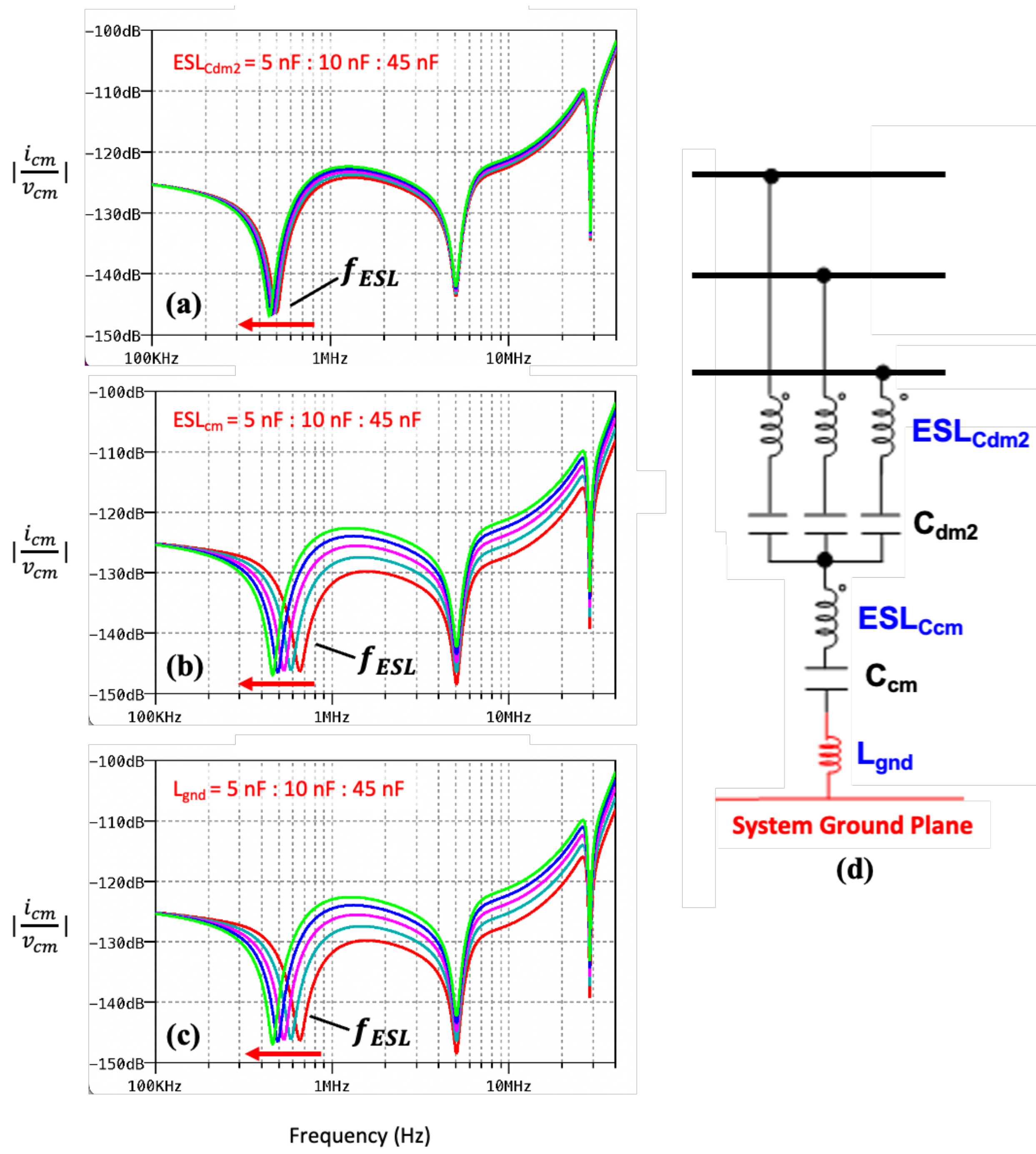


Fig. 2.13 Impact of the parasitic inductance on the CM capacitor branch (a) Impact of ESL_{Cdm2} (b) Impact of ESL_{Ccm} (c) Impact of L_{gnd} (d) Parasitic components on the shunt capacitor branch

Fig. 2.14 shows the simulated conducted emissions at the LISN terminal. The trend of the CM emission at the LISN matches well with the CM transfer curve in Fig. 2.13. The high conducted emission peaks f_{res2} and f_{res4} have been attenuated by the CM chokes and the overall CM noise has

been suppressed when the whole CM LCL filter is included in the circuit. The impact of the net parasitic inductance on the shunt capacitor branch is demonstrated by increasing the ground inductance L_{gnd} as illustrated in Fig. 2.15. Although the shifting of the anti-resonance f_{ESL} is not obvious due to the high switching harmonics around hundreds of kHz, the overall increase in the CM noise spectrum is observed after 500 kHz.

In summary, the equivalent capacitance and the net parasitic inductance on the shunt capacitor branch {ESL_{Cdm2}, ESL_{Ccm} and L_{gnd}} create an anti-resonance frequency (f_{ESL}) at hundreds of kHz. A higher net parasitic inductance results in a higher overall CM noise emission after the anti-resonance frequency. Therefore, ESL cancellation schemes as well as low impedance grounding techniques could be considered to reduce the CM emission from mid to high frequency.

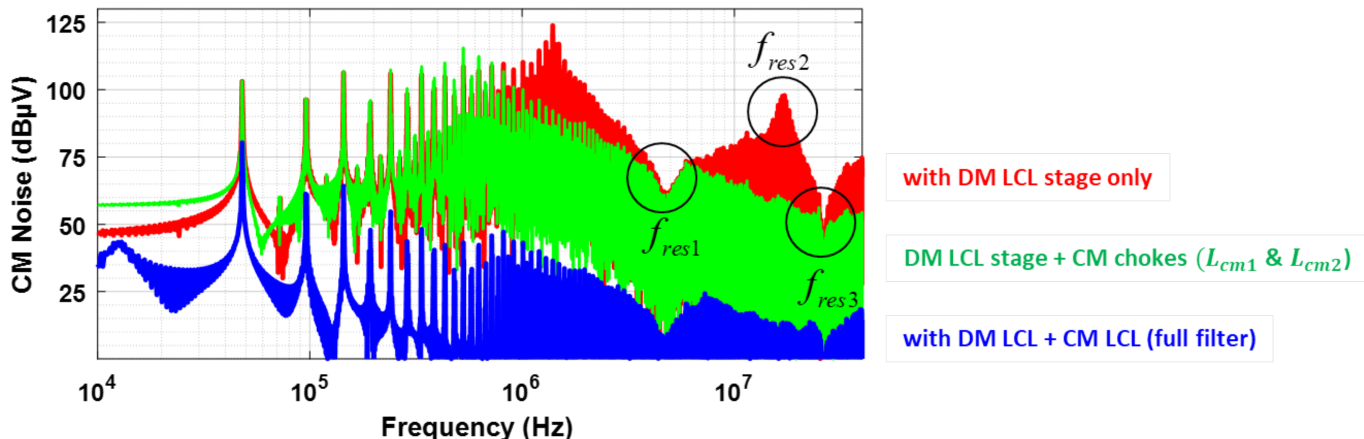


Fig. 2.14 Simulated CM noise voltage spectrum at the LISN terminal

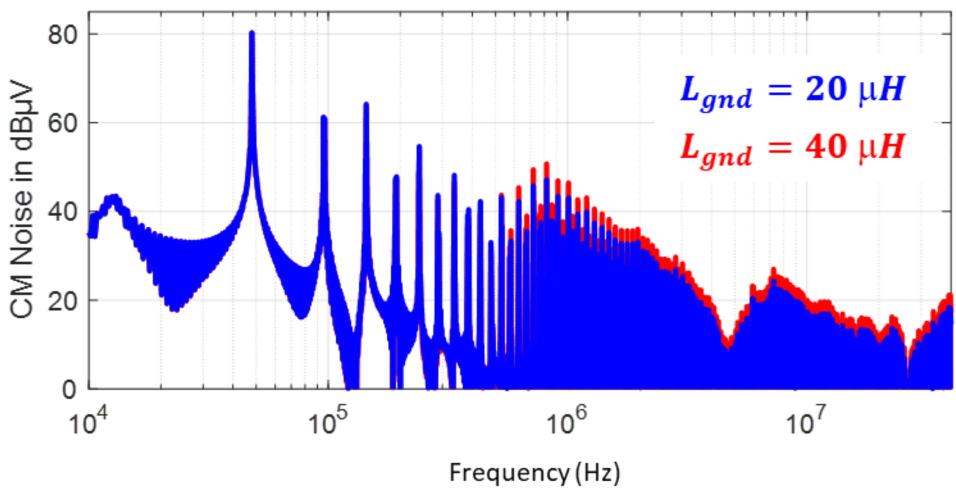


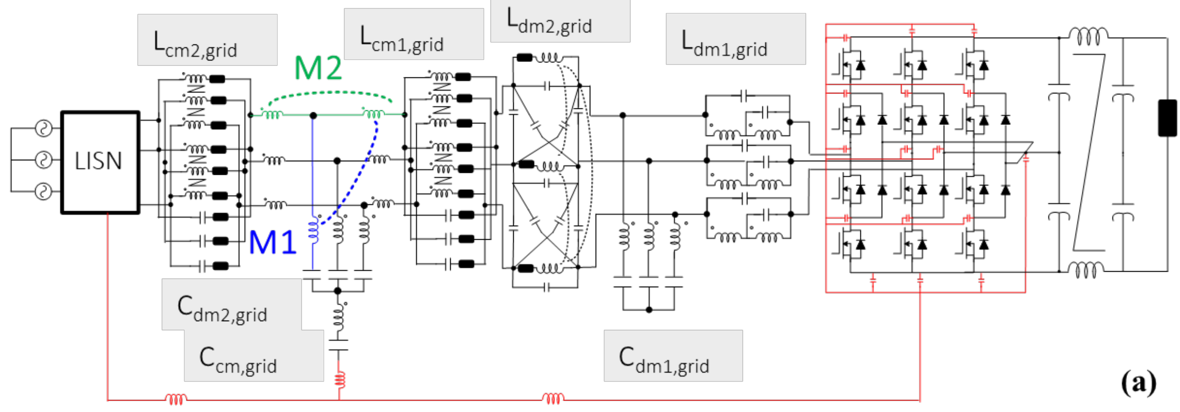
Fig. 2.15 Impact of the ground impedance with full filter

2.3 Impact of Filter Interconnections

In this section, the mutual coupling effect corresponding to the filter interconnection is investigated based on the conducted emissions simulations as well as the frequency-domain transfer gain analysis.

2.3.1 Impact of inductive couplings within the filter structure

The mutual inductive coupling is discussed in this section. Fig. 2.16 shows schematic of the full filter and 3D model of the baseline grid-side filter prototype with the critical mutual inductive couplings marked. M_1 represents the inductive coupling between the leakage inductance of the first stage CM choke (L_{cm1}) and the ESL of the second stage DM capacitor (C_{dm2}) while M_2 represents the inductive coupling between the leakage inductance of the two CM chokes.



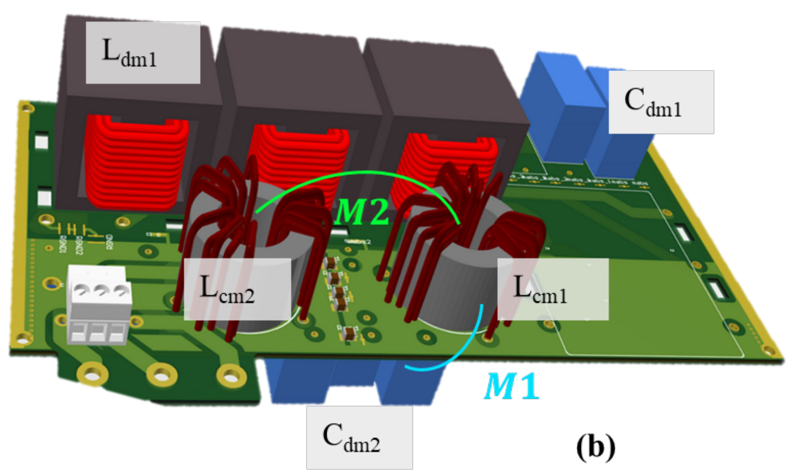


Fig. 2.16 (a) Schematic of the full filter labeling the critical inductive couplings. (b) Baseline filter prototype.

Fig. 2.17 shows the equivalent circuit for the inductive coupling. The coupling polarity is determined by the dot convention. The ESL of the DM capacitor branch will be directly affected by the mutual inductance M_1. The expression of M_1 is shown in (2.4), where k represents the coupling coefficient.

$$M_1 = k\sqrt{(L_{cm1,lk})(\, ESL_{C_{dm2}})} \tag{2.4}$$

When there is no coupling on the C_{dm2} branch, the self-resonance of C_{dm2} is seen on the DM transfer gain. The resonance can be expressed as

$$f_0 = \frac{1}{2\pi\sqrt{(ESL_{Cdm2})(C_{dm2})}} \tag{2.5}$$

For a positive coupling, the impedance of the C_{dm2} branch can be expressed as

$$Z_{pos} = ESR + j[\omega(ESL_{Cdm2} + |M_1|) + \frac{1}{\omega C}] \tag{2.6}$$

The resonant frequency of the DM capacitor branch can thus be expressed as

$$f_{pos} = \frac{1}{2\pi\sqrt{(ESL_{Cdm2} + |M_1|)(C_{dm2})}} \tag{2.7}$$

It is obvious that the resonant frequency will be shift to a lower frequency with a positive inductive coupling due to a larger net inductance on the C_{dm2} branch.

For a negative coupling, the impedance of the C_{dm2} branch can be expressed as (**2.8**)when the mutual inductance is smaller than the ESL of C_{dm2}

$$Z_{neg1} = ESR + j[\omega(ESL_{Cdm2} - |M_1|) + \frac{1}{\omega C}] \tag{2.8}$$

Similarly, the resonant frequency of the DM capacitor branch can thus be expressed as

$$f_{neg1} = \frac{1}{2\pi\sqrt{(ESL_{Cdm2} - |M_1|)(C_{dm2})}} \tag{2.9}$$

In this case, the resonant frequency will be shift to a higher frequency. However, when the mutual inductance is larger than the net ESL of the shunt capacitor branch, the resonant point does not exist anymore as discussed in [60]. Fig. 2.18 (a) shows the transfer gain at the LISN terminal for

different coupling coefficient. The ESL of the DM capacitor is 25 nH and the leakage inductance of the CM choke is 2 μH. Clearly, a positive coupling increases the net ESL of the DM capacitor branch, resulting in a higher gain at the LISN terminal. For negative coupling, only a coupling coefficient less than 0.09 will improve the performance at the LISN.

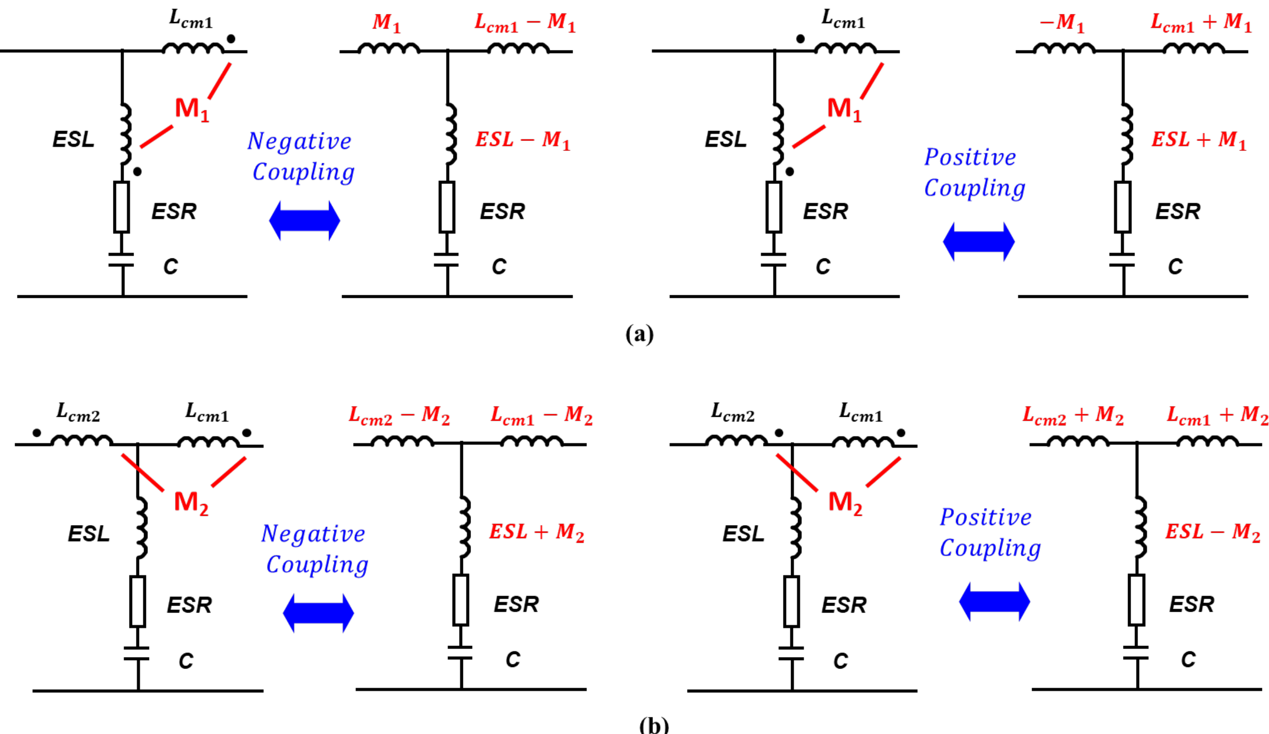


Fig. 2.17 Equivalent circuit for inductive coupling (a) M_1 (b) M_2

Similarly, the mutual coupling inductances M_2 is given by the expression in (2.10), where k represents the coupling coefficient.

$$M_2 = k\sqrt{L_{cm1,lk}\, L_{Cm2,lk}} \tag{2.10}$$

A positive coupling between the two CM chokes will generate a negative mutual inductance at the DM capacitor branch, as shown in Fig. 2.17 (b). The expression of the resonance frequency is similar as (2.7) and (2.9). Fig. 2.18 (b) shows the transfer gain at the LISN terminal for different coupling coefficient. Due to the large leakage inductance of the CM choke compared to the ESL

of the DM capacitor, only a negative coupling coefficient less than 0.01 improves the performance at the LISN. The gain at the LISN shows a 30 dB increase when a 0.2 positive and negative coupling coefficient is presented.

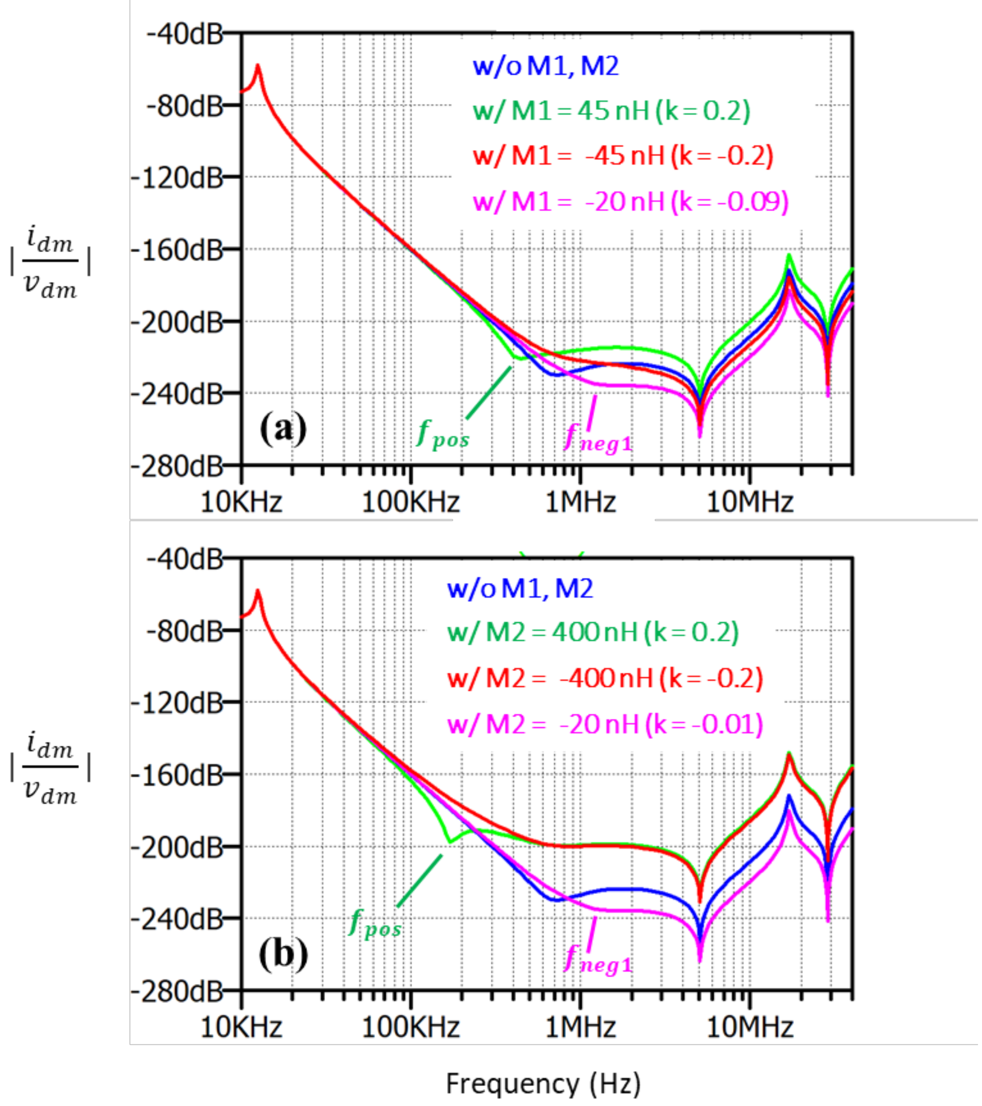


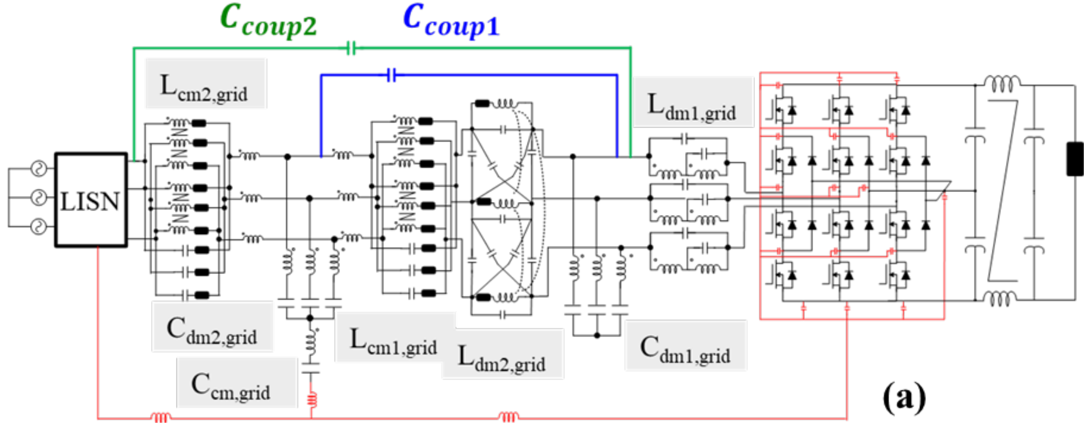
Fig. 2.18 Impact of the mutual inductive coupling (a) Impact of M_1 (b) Impact of M_2

In summary, the mutual inductive coupling M_1 and M_2 lead to the increase of the DM transfer gain after hundreds of kHz due to the mutual inductance introduced on the shunt capacitor branch of the CM LCL filter stage. Since the leakage inductance of the CM choke is much higher compared to the net parasitic inductances on the shunt capacitor branch, a small coupling

coefficient for M_1 or M_2 could generate a high mutual inductance. Therefore, the winding direction and arrangement should be considered carefully when constructing the CM choke to achieve the minimum inductive coupling within the CM LCL stage.

2.3.2 Impact of capacitive couplings within the filter structure

The electric coupling between stages of EMI filter should be considered for a compact filter design due to the proximity of filter components. Fig. 2.19 (b) shows the initial prototype of the baseline grid-side filter block. In this prototype, the mutual capacitive coupling between the boost inductor (L_{dm1}) and the first stage CM inductor (L_{cm1}) and the coupling between the boost inductor (L_{dm1}) and the second stage CM inductor (L_{cm2}) are considered due to the adjacency of the two components. The capacitive coupling effects are represented as C_{coup1} and C_{coup2} in the schematic of the full filter, as shown in Fig. 2.19 (a).



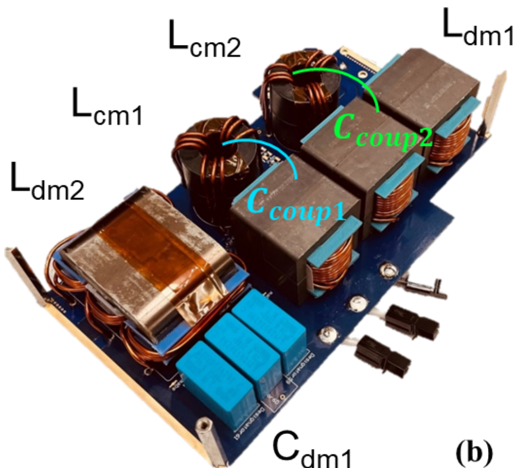


Fig. 2.19 (a) Schematic of the full filter labeling critical capacitive coupling. (b) Baseline filter prototype.

Fig. 2.20 shows the impact of the electric coupling between the two stages at the LISN terminal. A higher gain occurs after 10 MHz when a capacitive coupling path (C_{coup1}) between the boost inductor and the first stage CM choke is introduced in the circuit. This is because the C_{coup1} provides a lower impedance path compared to the impedance of the second stage DM inductor (L_{dm2}) and the first stage CM choke (L_{cm1}) after 10 MHz. Therefore, most of the CM current is flowing through the capacitive coupling path, resulting in a loss of attenuation from L_{dm2} and C_{cm1}.

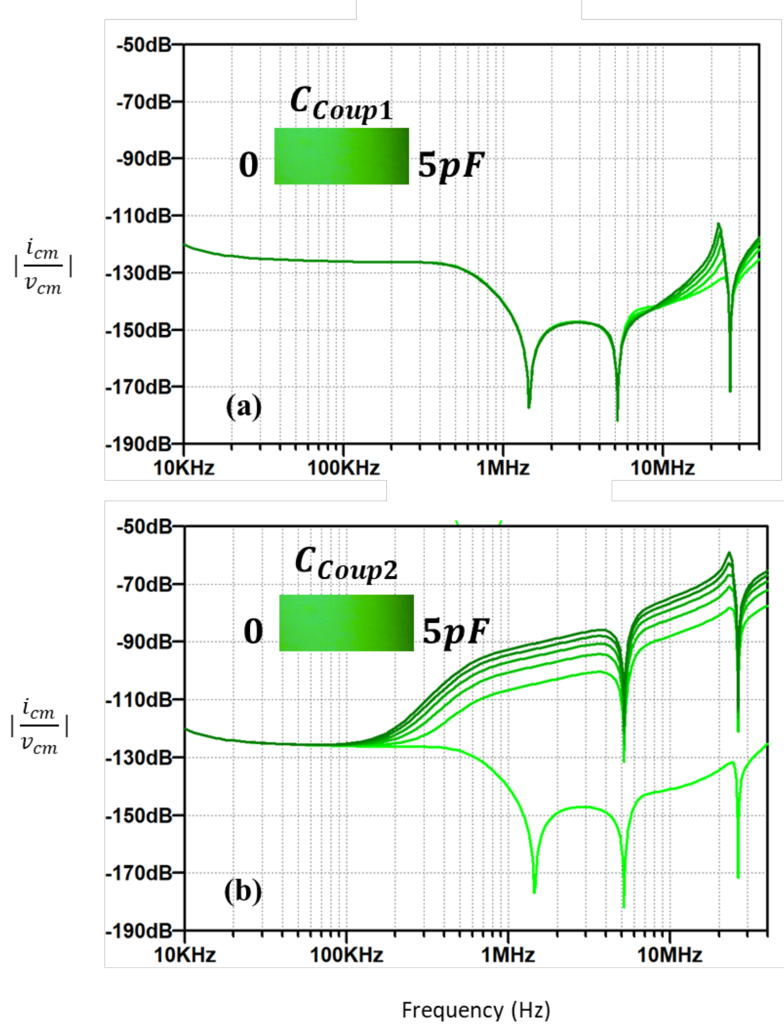


Fig. 2.20 Impact of the mutual capacitive coupling (a) C_{coup1} (b) C_{coup2}

The capacitive coupling path (C_{coup2}) between the boost inductor and the second stage CM choke results in a much higher gain at the LISN from lower frequency (100 kHz). This is due to the mutual electric coupling in the filter with a T junction. Fig. 2.21 shows the equivalent circuit for the mutual electric coupling in a T-shaped joint [14].

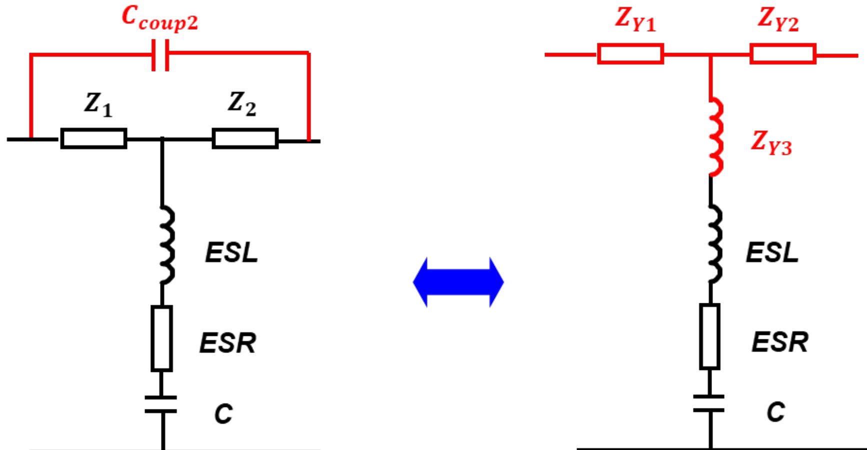


Fig. 2.21 Equivalent circuit for T-type capacitive coupling

The equivalent circuit can be derived using Δ→Y transformation. Assuming Z_{coup2}, the impedance of the parasitic capacitor C_{coup2}, is much larger than Z_1 and Z_2, the impedance of the equivalent circuit can be expressed in (2.11).

$$\begin{cases} Z_{Y1} = \dfrac{Z_{Y1}Z_{coup2}}{Z_{Y1}+Z_{Y2}+Z_{coup2}} \approx Z_1 \\ Z_{Y2} = \dfrac{Z_{Y2}Z_{coup2}}{Z_{Y1}+Z_{Y2}+Z_{coup2}} \approx Z_2 \\ Z_{Y3} = \dfrac{Z_{Y1}Z_{Y2}}{Z_{Y1}+Z_{Y2}+Z_{coup2}} \approx sC_{coup2}Z_1Z_2 \end{cases} \tag{2.11}$$

Obviously, the electric coupling in the T type filter contributes to the net ESL of the shunt capacitor branch. Considering ideal inductor for Z_1 and Z_2, Z_{Y3} can be expressed as

$$Z_{Y3} = s^3C_{coup2}(L_{cm2})(L_{cm1}+L_{dm2}) \tag{2.12}$$

The introduced impedance at the shunt capacitor branch is proportional to the cube of the frequency. Therefore, the net impedance of the shunt capacitor branch becomes much higher compared to the impedance of L_{dm2}, L_{cm1} and L_{cm2} from mid frequency. In other words, the majority of the CM currents are bypassed from the boost inductor to the LISN via the C_{coup2}, making the CM capacitor path ineffective to circulate the CM currents after 100 kHz. The impact

of the capacitive coupling is also evident in the conducted emissions simulation, as shown in Fig. 2.22.

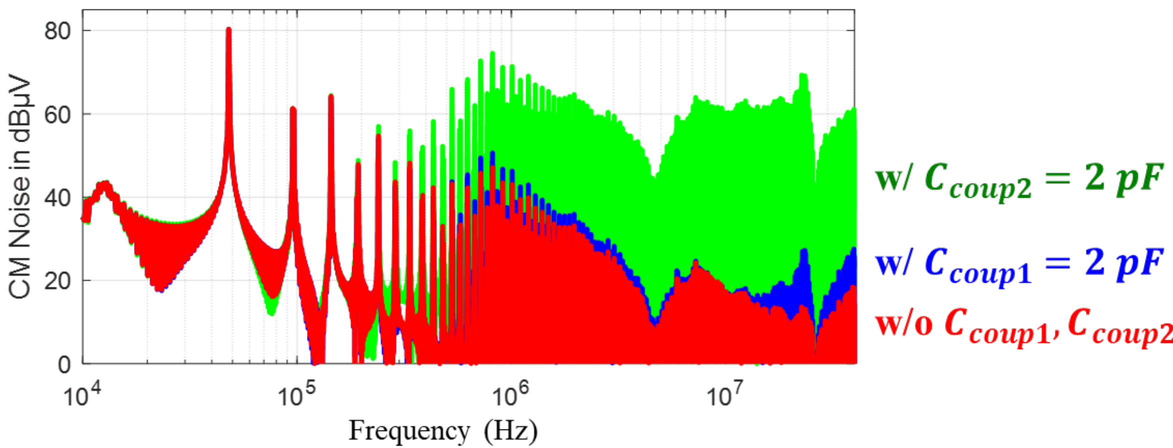


Fig. 2.22 Impact of electric coupling with full filter

In summary, the mutual capacitive coupling C_{coup1} and C_{coup2} provide feed-forward paths for high frequency CM currents, resulting in a loss of CM attenuation from the filter components being bypassed. Efforts to avoid the feed-forward coupling effect should be taken especially when a T-shape junction is included in the circuit being bypassed. In this filter topology, the coupling from the boost inductor to the second stage CM choke, C_{coup2}, should be minimized to avoid the significant increase in CM emission after mid frequency.

The PCB layout could also play an important role in the filter performance. Fig. 2.23 shows the initial PCB layout for the grid-side filter. Due to the large ground planes on the top and bottom layer, the power traces to ground parasitic C_{PCB} should be considered in the simulation model, as shown in Fig. 2.24.

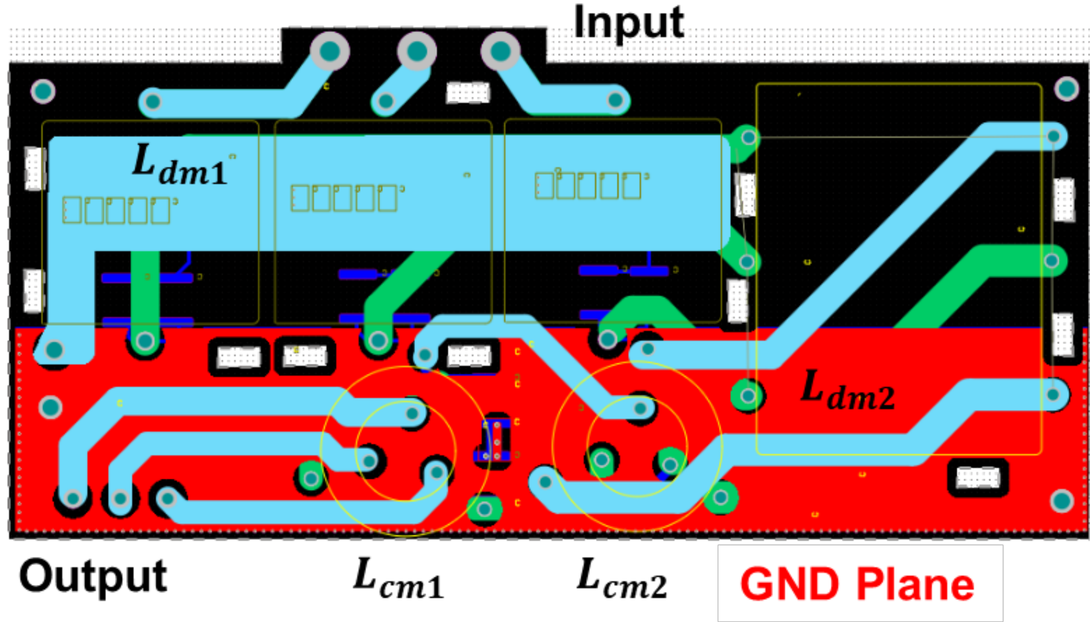


Fig. 2.23 PCB layout of the baseline grid-side filter.

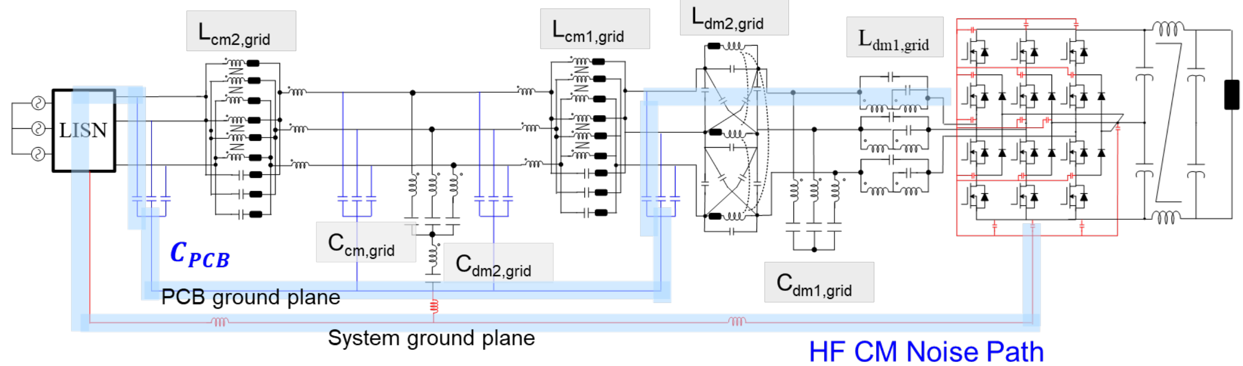


Fig. 2.24 Schematic of the full filter with capacitive coupling from PCB traces to PCB ground plane.

Fig. 2.25 shows the CM gain at the LISN when all the trace to ground parasitic is included. Since the trace to ground parasitic is much smaller compared to the CM LCL path, most of the CM currents flows through the trace to ground parasitic to the LISN and circulate back to the converter through the system ground. In this case, the CM LCL filter is ineffective in the circuit and the anti-resonance from the boost inductor can be observed at the LISN terminal. This phenomenon can also be observed in the conducted emissions, as shown in Fig. 2.26. In summary, the high frequency CM currents propagate through the PCB ground plane via the mutual capacitive

coupling corresponding to the PCB ground, making the CM LCL filter ineffective in attenuating the CM emissions at high frequency. In this filter topology, a single ground point should be enough to ground the CM capacitor. A revised host PCB was later designed to minimize the mutual parasitic coupling within the board.

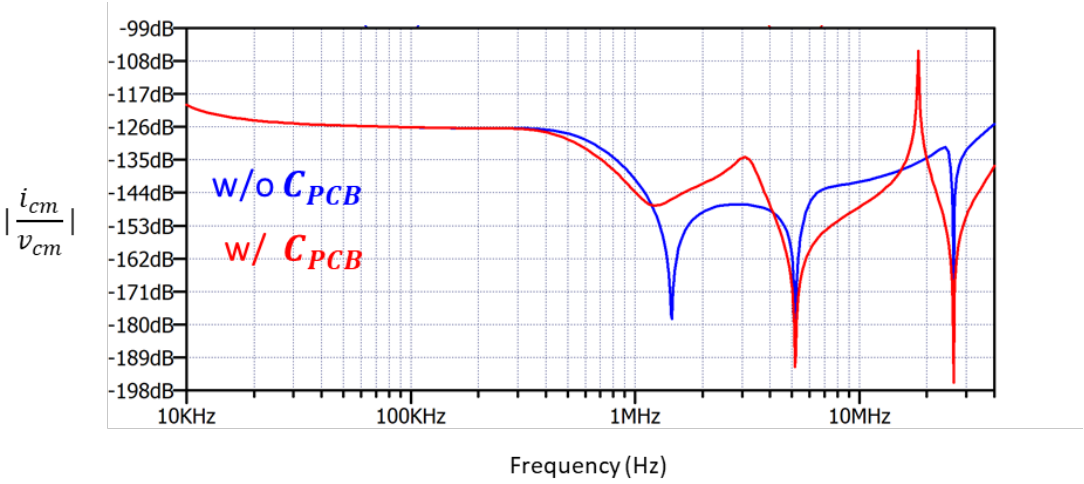


Fig. 2.25 Impact of the capacitive coupling from PCB traces to PCB ground plane

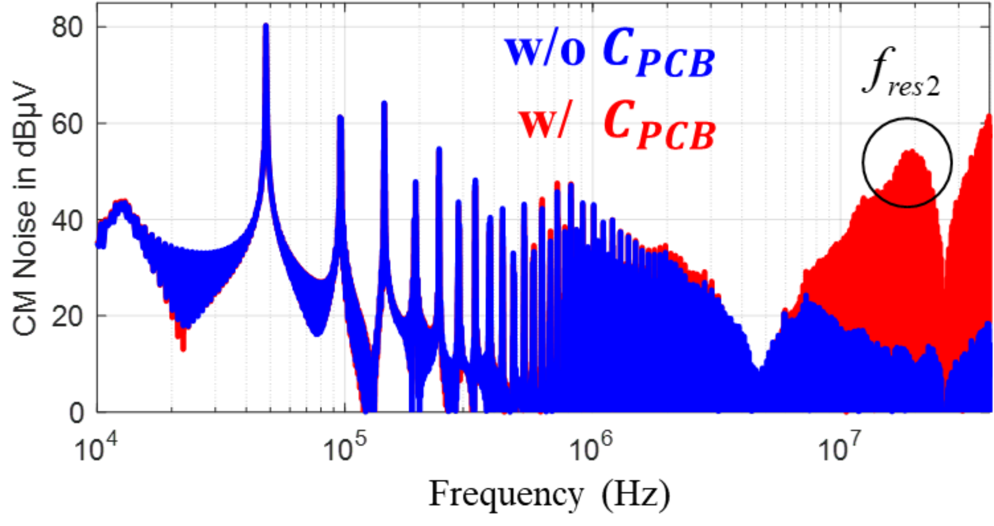


Fig. 2.26 Simulated CM noise at the LISN terminal with full filter

2.3 Summary

This chapter presents an in-depth study on the effects of the parasitic parameters on the grid-side filter performance. The critical components which have a significant impact on the high-frequency emissions are identified and summarized below.

1. The winding capacitances of the boost inductor create a high conducted emission peak around the anti-resonance frequency (f_{res2}). Better winding configurations could be adopted to minimize the EPC of the boost inductor.

2. The net parasitic inductance on the shunt capacitor branch of the CM LCL filter stage {ESL_{Cdm2}, ESL_{Ccm} and L_{gnd}} increases the overall CM noise emission beyond hundreds of kHz. Better filter grounding techniques could be adopted to reduce the L_{gnd} while paralleling multiple small capacitors could reduce the effective ESL.

3. The mutual inductive couplings M_1 and M_2 introduce mutual inductances on the shunt capacitor branch of the CM LCL filter stage, increasing the overall DM noise emission after hundreds of kHz. Better winding configurations of the CM chokes, physical placement of the CM LCL filter components could be introduced to minimize the inductive coupling effect. Magnetic shields could also be introduced in between components to absorb the flux leakage.

4. The mutual capacitive couplings C_{coup1} and C_{coup2} bypass filter components by providing a low impedance feed-forward path for high frequency CM current. Electric shields could be introduced between the filter stages to redirect the displacement currents to ground.

5. The mutual capacitive coupling C_{PCB} bypasses the CM filter stage after several MHz, making the CM LCL filter ineffective in attenuating the high frequency CM emissions. A

better layout with minimal overlapping of power traces and ground plane could be designed to reduce the detrimental feed-forward effects.

These critical parasitic components will be optimized as part of the filter design process in the next chapter.

Chapter 3 Design of B2B Converter Filter

3.1 Introduction

This chapter carries out the multi-objective design of the critical passive components identified in Chapter 2. The first part of this section addresses the high conducted emissions peak corresponding to the winding capacitances of the multi-layered traditionally wound boost inductor. Single-layered and two-layered solutions are then proposed to solve the anti-resonance issue. A Finite Element Analysis (FEA) based modeling technique is conducted to study the impedance characteristic of different winding configurations. Finally, the effectiveness of the proposed solutions is verified with a three-phase three-level rectifier setup.

The second part of this section addresses the self-parasitic and mutual couplings associated with the filter parasitic components. FEA based simulations as well as transfer gain measurements are studied to better understand impact of such parasitic components. An optimal interconnection of the filter structure, including the part-placement of filter components, as well as the PCB layout and the grounding of the filter is then proposed. Finally, a full-scale filter structure employing the proposed methodologies is constructed to desensitize the influence of self-parasitic and near field couplings. The filter performance will be evaluated in the next chapter.

3.2 Design of Boost Inductor

3.2.1 Introduction

Three-phase power factor correction (PFC) circuits are common in rectifier applications, where the most used topology is the voltage-source boost converter. This type of converter acts as

a voltage-source inverter that is connected to the grid on its ac terminals, for which it requires boost inductors to decouple its operation from the grid voltages. These inductors also serve as temporary energy storage, charging and discharging on a switching cycle basis, to pump current into the dc terminal capacitor in order to regulate the dc output voltage of the converter. This inductor hence plays a fundamental role both in the differential-mode and common-mode operation of the boost rectifier, providing it with an inherent 20 dB attenuation capacity.

However, the impedance characteristics of the boost inductor is observed to change the noise profile significantly. The anti-resonance contributed by the parasitic capacitances within the multi-layered windings of the boost inductor is observed to induce high conducted emission peak around the anti-resonance point, as seen in Section 2.2.1. To study the anti-resonance phenomenon of the traditional multi-layered boost inductor as well as the impedance characteristic of different winding configurations, a detailed Finite Element Analysis (FEA) based modeling technique is conducted.

The FEA based modeling flowchart is provided in Fig. 3.1. The elements of the boost inductor, including the magnetic cores, bobbins, insulator, and winding types are first defined in the ANSYS PEMAG software. The 3D boost inductor model is then generated and exported from ANSYS PEMAG to ANSYS Q3D software to extract the distributed RLGC parameters for different winding configurations. Finally, the circuit model is exported from Q3D to LTSpice software to obtain the impedance characteristics for different boost inductor solutions.

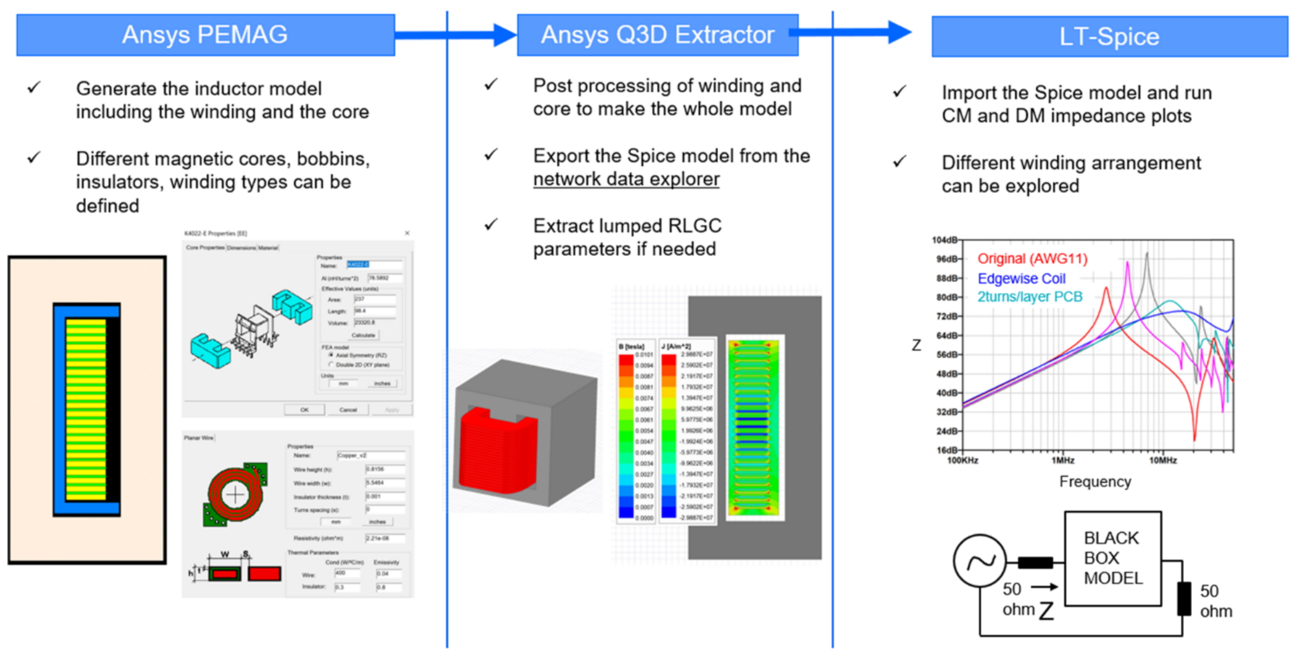


Fig. 3.1 Generalized FEA based Modeling Technique for Boost Inductor

Fig. 3.2 (a) shows the prototype of the traditionally wound boost inductor using KOOLMU® powder core 00K4022E026 from Magnetics Inc. A total of 22 turns are split into two layers with a sequential winding pattern where the inner layer (Layer 1) is wounded from top to bottom while the outer layer (Layer 2) is wounded from bottom to top with AWG 11 enameled wire. This kind of multi-layered round/foil conductor-based winding solutions have been widely adopted for boost inductors in the past due to their low cost, simplicity, and ease of manufacturing.

Fig. 3.2 (b) shows the energy and capacitance distribution of the traditionally wound boost inductor. It can be seen that the voltage difference between the top two turns (turn 1 and turn 22) is the highest while the turns at the bottom have negligible voltage drop. This high discontinuity in voltage drop/ distributed energy within the windings leads to high displacement current, resulting in the anti-resonance phenomenon.

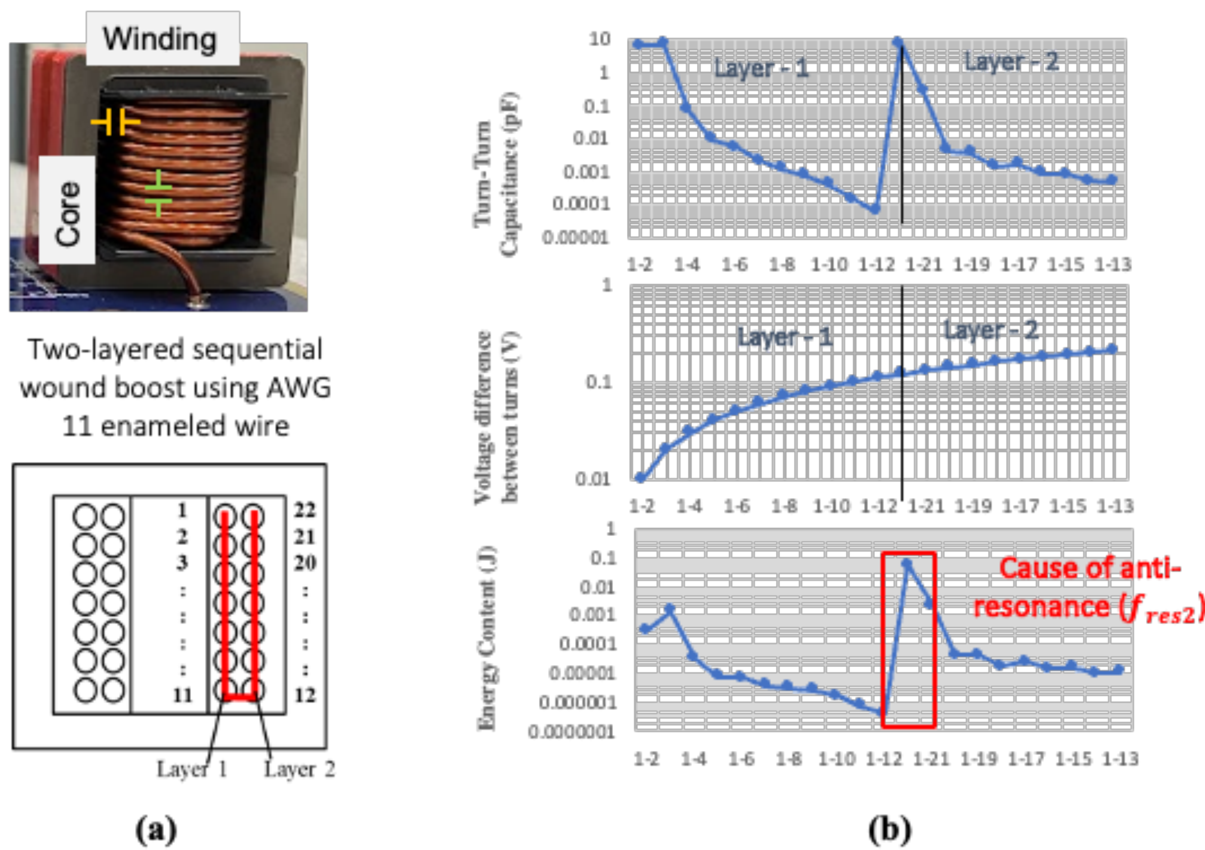


Fig. 3.2 Traditional two-layered boost inductor with sequential winding

(a) Prototype (b) Energy and capacitance distribution

3.2.2 Proposed Winding Configurations

To reduce the voltage difference between any two adjacent turns, single-layered edgewise winding solution and two-layered PCB based zig-zag winding solution are proposed.

A. Single layer solution using edge-wound coil

The edgewise coil is commonly used in electric motor applications due to their better heat dissipation compared to traditional round wires. Fig. 3.3 (a) shows the prototype of the edgewise wound boost inductor using the same KOOLMU® powder core 00K4022E026 from Magnetics Inc. The dimension of the edgewise coil is customized to accommodate all 22 turns in a single layer within the window of the core. Fig. 3.4 shows the construction of the single-layered edge wound

solution. A 1mm thick bobbin is first customized and inserted at the middle leg of the E core. Next, the customized edgewise coil is inserted with additional 0.1' FR4 sheet between turns to keep a uniform turn-turn separation and capacitance.

Fig. 3.3 (b) shows the capacitance and energy distribution of the proposed single-layered edgewise wound solution using FEA simulations; as illustrated, the discontinuity in the distributed energy within the windings has been eliminated compared to the traditional wound boost inductor.

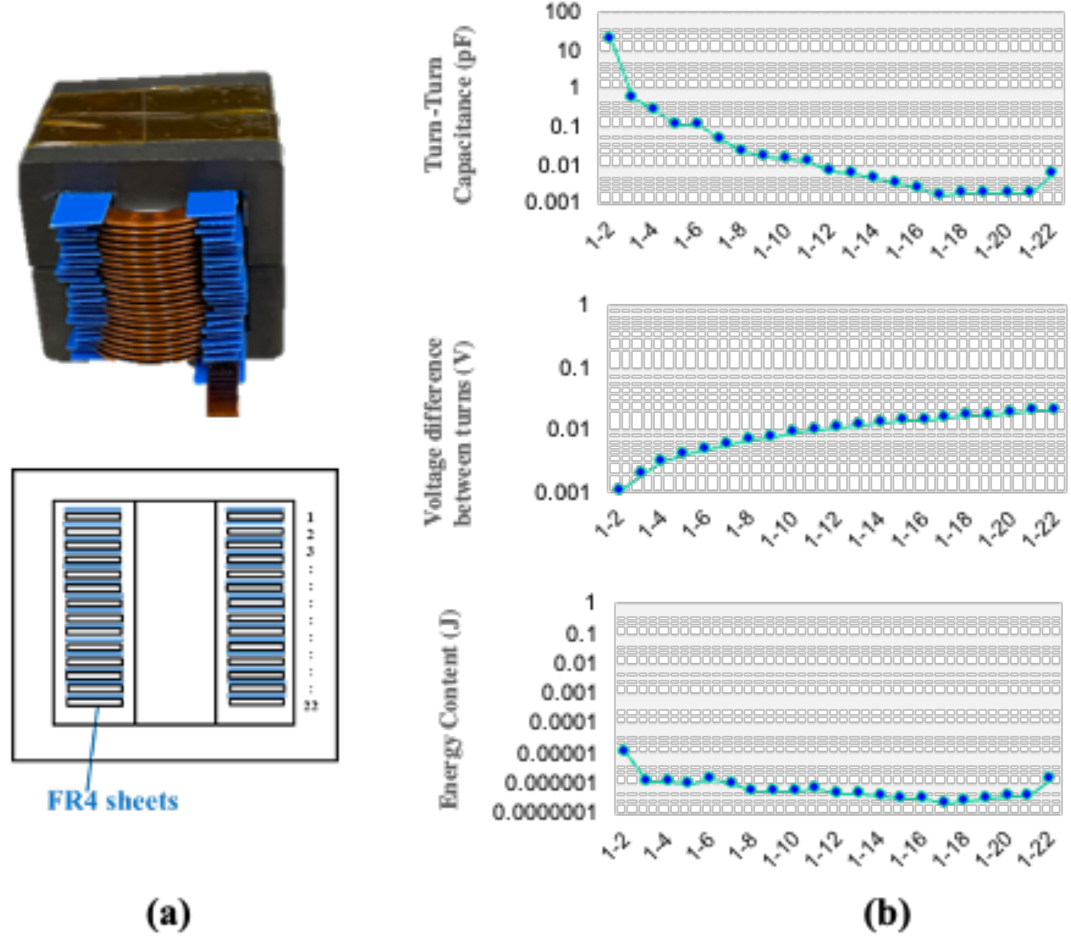


Fig. 3.3 Proposed single-layered edgewise wound boost inductor

(a) Prototype (b) Energy and capacitance distribution

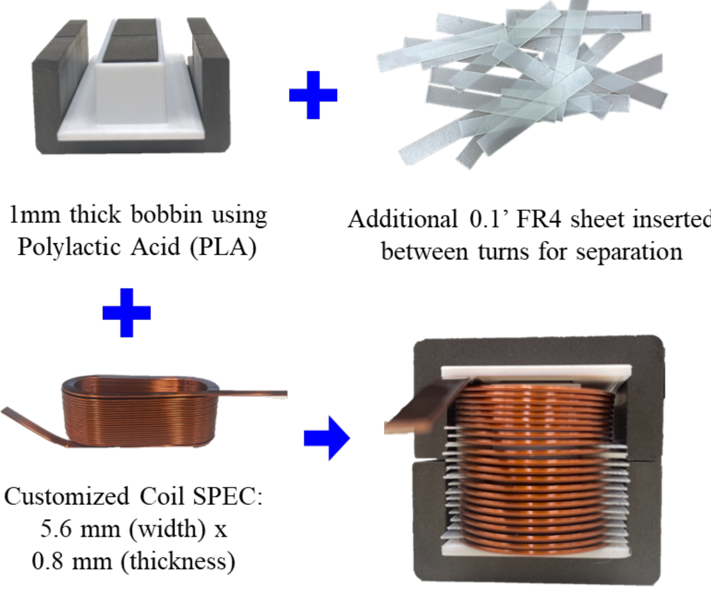


Fig. 3.4 Hardware construction of the proposed single-layered edgewise wound boost inductor

B. Two-layered zig-zag winding configuration using planar PCB

Multi-layered winding structures are usually adopted for a better window utilization compared to single-layered solutions when designing inductors. To eliminate the high voltage difference between the top or bottom turns within the multi-layered sequential winding structures, 'zigzag (zz)' winding configuration has been proposed. Fig. 3.5 (a) shows the structure of a two-layered 'zz' winding configuration, where the voltage drop between the top two turns (turn 1 and turn 10) as well as the voltage drop between the bottom two turns (turn 9 and turn 19) are negligible. This is also evident in the capacitance and energy distribution of the proposed two-layered zig-zag solution using FEA simulations, as shown in Fig. 3.5. Similarly, the discontinuity in the distributed energy within the windings has also been eliminated compared to the traditional wound boost inductor.

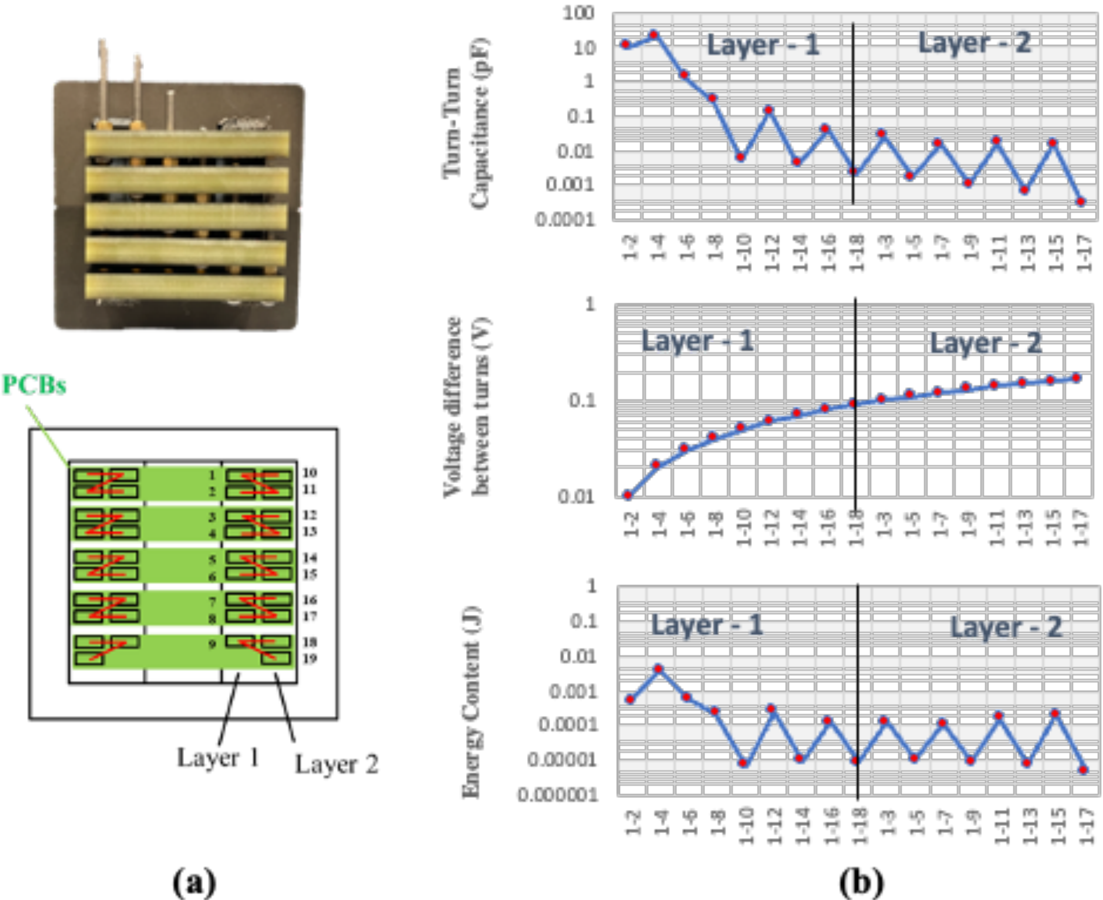


Fig. 3.5 Proposed two-layered zig-zag PCB wound boost inductor
(a) Prototype (b) Energy and capacitance distribution

To realize the two-layered 'zz' winding pattern, where each turn within the inner layer (Layer 1) is connected to the turn within the outer turn (Layer 2) below, planar PCB windings is selected due to its flexibility for winding connections compared to the traditional round conductors. The realization of the two-layered 'zz' winding configuration is visualized in the PCB layout as per Fig. 3.6. The odd layers of the PCB board contain the windings while the even layers of them connect the inner turn of the winding layer above to outer turn of the winding layer below through buried vias for the 'zz' connection. The total boards needed is dependent on the maximum thickness that a vendor can fabricate. It is possible to build entirely one PCB structure instead of stacking multiple PCBs depending on vendor capability. When multiple PCB boards are adopted,

each PCB can interface with the adjoining PCBs underneath through threaded rods. These rods ensure proper mechanical assembly besides providing electrical connections between PCBs.

In this work, a larger KOOLMU® powder core 00K5530E026 from Magnetics Inc. is selected to accommodate the multiple boards and nuts. A total of 19 turns is first divided into five 4-layer boards. Each board is comprised of two winding layers and two ‘zz’ connection layers as shown in the layout per Fig. 3.6. Fig. 3.7 shows the board stack-up, where each layer has a customized 1.1 mm copper thickness to handle the 30 Arms current. The five boards are then connected through threaded rods and nuts to form the whole zig-zag winding configuration, as shown in Fig. 3.6.

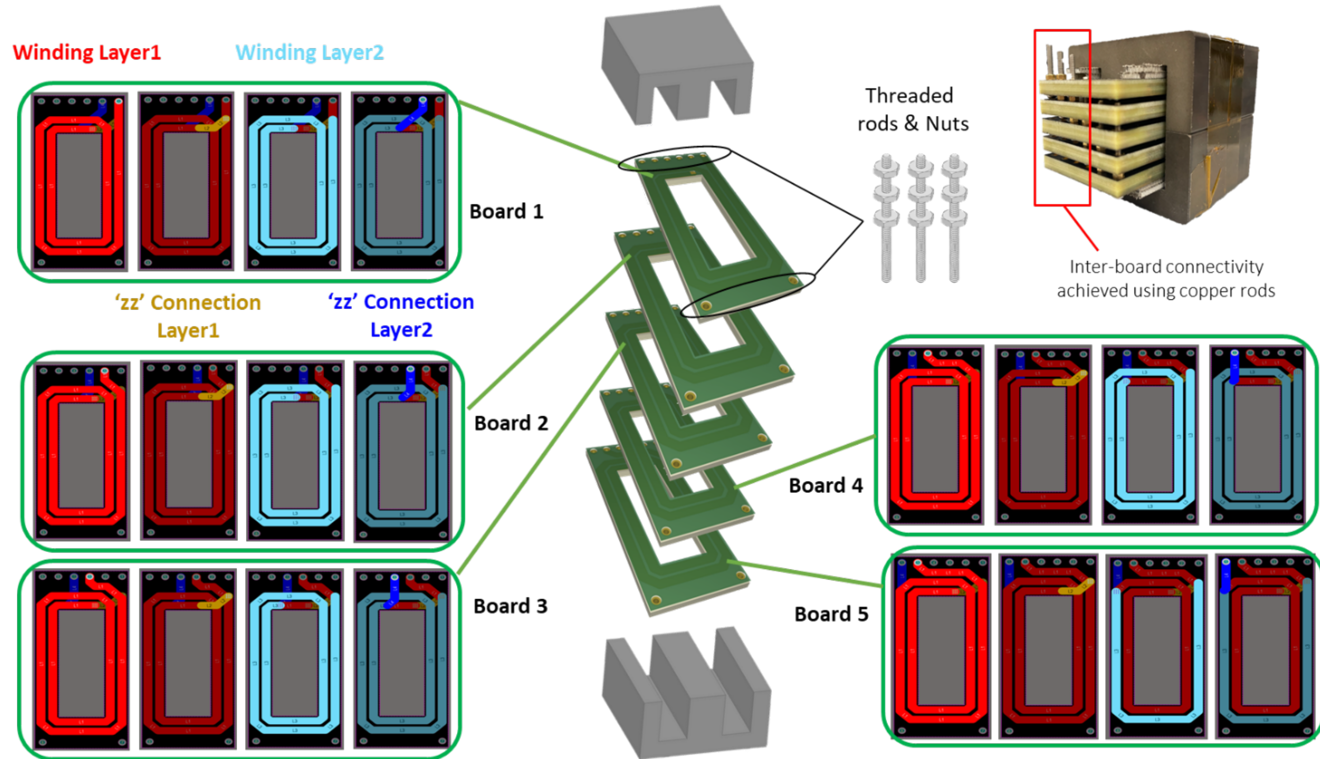


Fig. 3.6 Proposed two-layered zig-zag winding configuration using planar PCB

	Top Overlay		Overlay	
	Top Solder	Solder Resist	Solder Mask	0.01016mm
1	Top Layer		Signal	1.1mm
	Dielectric 1	FR-4	Dielectric	0.2mm
2	Mid-Layer 1		Signal	1.1mm
	Dielectric2	FR-4	Dielectric	0.2mm
3	Mid-Layer 2		Signal	1.1mm
	Dielectric3	FR-4	Dielectric	0.2mm
4	Bottom Layer		Signal	1.1mm
	Bottom Solder	Solder Resist	Solder Mask	0.01016mm
	Bottom Overlay		Overlay	

Per Board Thickness: 5 mm
Nut Height: 1.6 mm

Per Turn Dimension:
3.5mm (width)
x 1.1mm (thickness)

Fig. 3.7 PCB stackup of the proposed two-layered 'zig-zag' winding configuration

Fig. 3.8 shows the measured impedance with the distributed model extracted from ANSYS Q3D. The anti-resonant is not seen from the impedance measurements due to the low displacement currents within the windings for the two proposed solutions. The constructed prototype of the proposed solutions is shown in Fig. 3.9. It should be noted that the zig-zag wound solution is 50% larger than the edge-wound counterpart and its window utilization is poor. This is due to the lack of available powder core alternatives to meet the 'zz' form factor requirement.

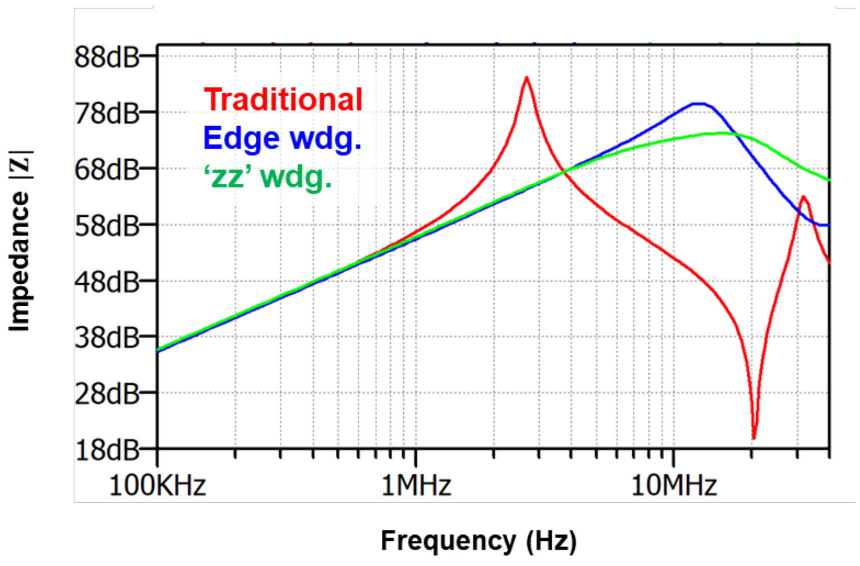


Fig. 3.8 Simulated impedances for the proposed boost inductor solutions

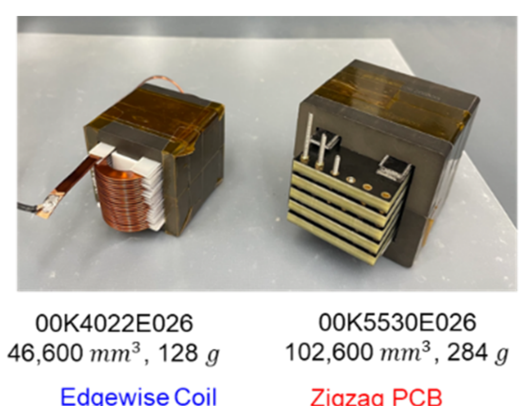


Fig. 3.9 Constructed prototype of the proposed boost inductor solutions

3.2.3 Experimental Verification

The proposed inductors are verified with the three-phase three-level PFC rectifier test bed, as shown in Fig. 3.10. The physical impedance measurements, taken using Keysight impedance analyzer 4990A, of the proposed inductors are shown in Fig. 3.11. Compared to the two-layered traditional wound inductor, the resonance points of the proposed inductors are shifted to higher frequencies and the anti-resonance points do not occur up to 30 MHz. Fig. 3.12 shows the measured EMI noise voltage spectrum at the LISN terminal. Clearly, the resonance and anti-resonance points of inductors are correlated to the valleys and peaks of the noise emissions. The absence of the anti-resonance phenomenon for the two proposed solutions result in a 20 dB improvement for both CM and DM emissions around the anti-resonance frequency of the traditional wound inductor.

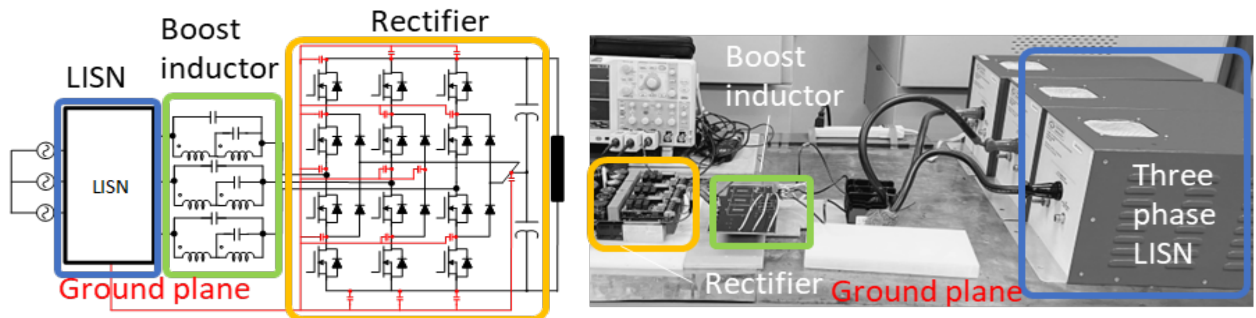


Fig. 3.10 Three phase 3L PFC rectifier test bed

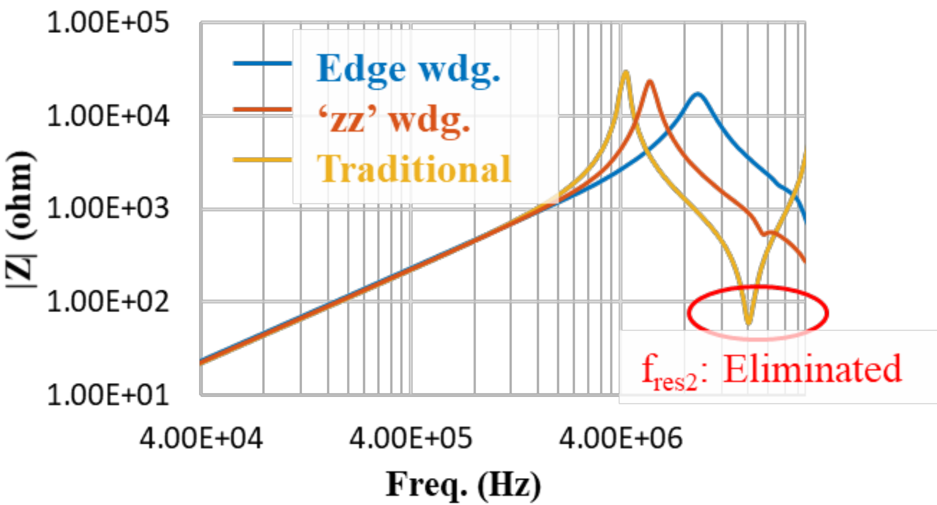


Fig. 3.11 Impedance measurements for the proposed boost inductor solutions

Compare the two proposed solutions, the edge-wound technique seems better due to a higher resonance point compared to the PCB based 'zz' winding technique. In addition, the magnitude of the converter commutation loop resonance at 27 MHz for the edge-wound technique are 10 dB lower compared to the 'zz' winding counterpart. The comparison between the traditional and the two proposed inductors for a 15-kW three-level three-phase back-to-back converter system is listed in Table 3-1. It should be noted that the zig-zag wound configuration was not fully optimized for high power density. The table is just to provide a more quantitative understanding. Besides, the flexibility in PCB based inductor design makes it possible to integrate external compensating circuits with the PCBs to further damp the resonance points.

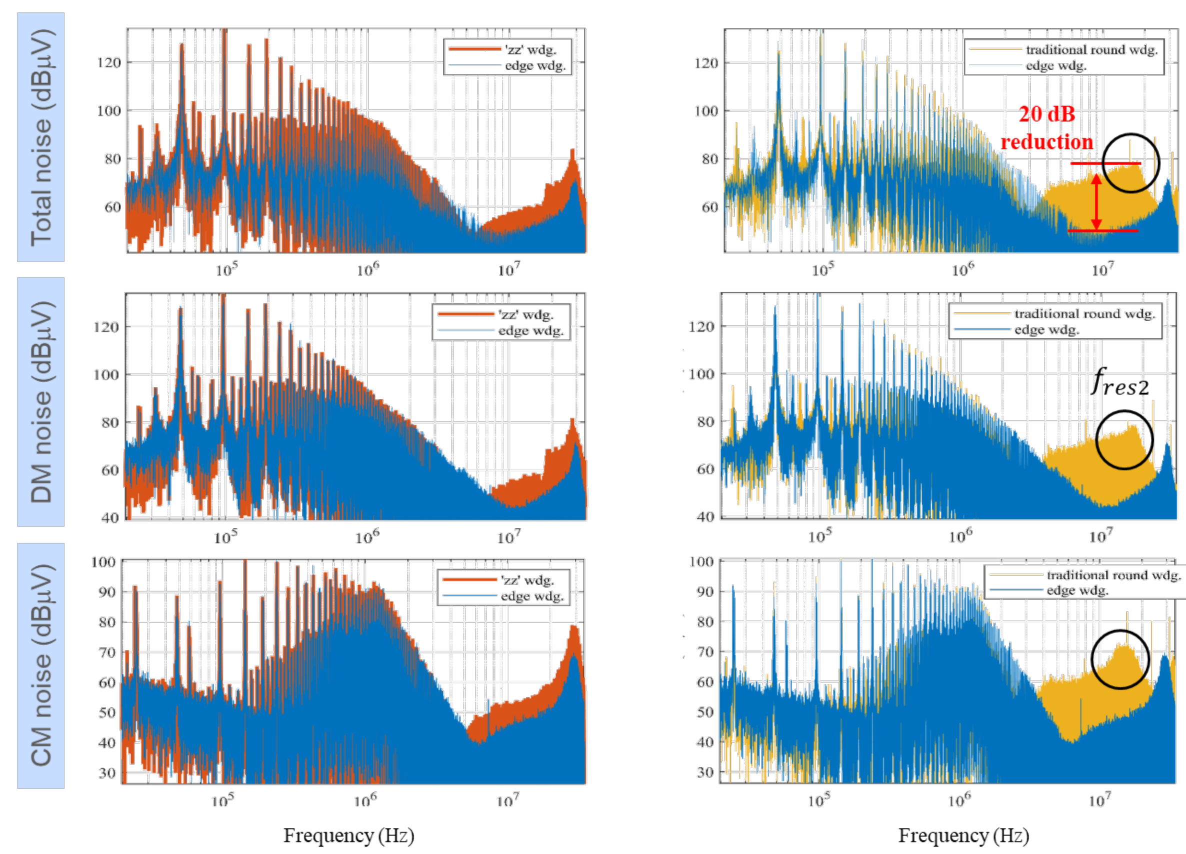


Fig. 3.12 Noise Spectrum Comparison

Table 3-1 Comparison between the proposed solution for a 15 kW prototype

Parameter	***Traditional Sequential wdg.***	***Single-layer Edge Wound***	***Multi-layer 'Zig-zag' wdg.***
Cost	Lowest	Medium	High (depends on the availability of heavy copper and PCB manufacturing costs)
f_{res2} (anti-resonance)	17 MHz	none	None
Complexity	Easy	Easy	Hard (Threads and nuts needed for construction)
Core Weight (g)	128	128	284 (lack of available core alternatives to meet the form-factor requirement)
AC Losses (W)	5.51	6.84	4.03 (benefit from low proximity loss)
Scalability	yes	yes	Yes (Heavy copper version can be made)
Compensation	NA	NA	External circuits to compensate can be integrated with the PCB

3.3 Design of the Full Filter Structure

This section addresses the self-parasitic and mutual couplings associated with the filter parasitic components. The first part of this section mainly focuses on the near field effects corresponding to the placement of the passive components in the CM LCL filter stage while the second part of this section addresses the PCB layout and the grounding configuration of the full filter structure. FEA based simulations as well as transfer gain measurements are studied to better understand impact of such parasitic components. Optimal component placement, winding strategy as well as grounding and shielding techniques are proposed to desensitize the influence of the near field coupling on the filter performance. Consequently, a full-scale filter structure employing the proposed methodologies is constructed and tested for validation. The experimental evaluation will be covered in the next Chapter.

3.3.1 Design of CM LCL Filter Stage

The ESL of the CM/ DM capacitor is first investigated in the optimization process with FEA simulation using ANSYS Q3D software. In this study, the film capacitor is modeled as a rectangular sheet based on the PEEC model per [61]. Multiple capacitors are added in parallel to reduce the net ESL of the capacitor branch. Fig. 3.13 shows different capacitor paralleling configurations and their effective ESL. It can be seen that the interleaved zig-zag pattern and the vertical interleaved pattern yields the lowest ESL due to the opposite polarity of the mutual coupling between any two adjacent capacitors.

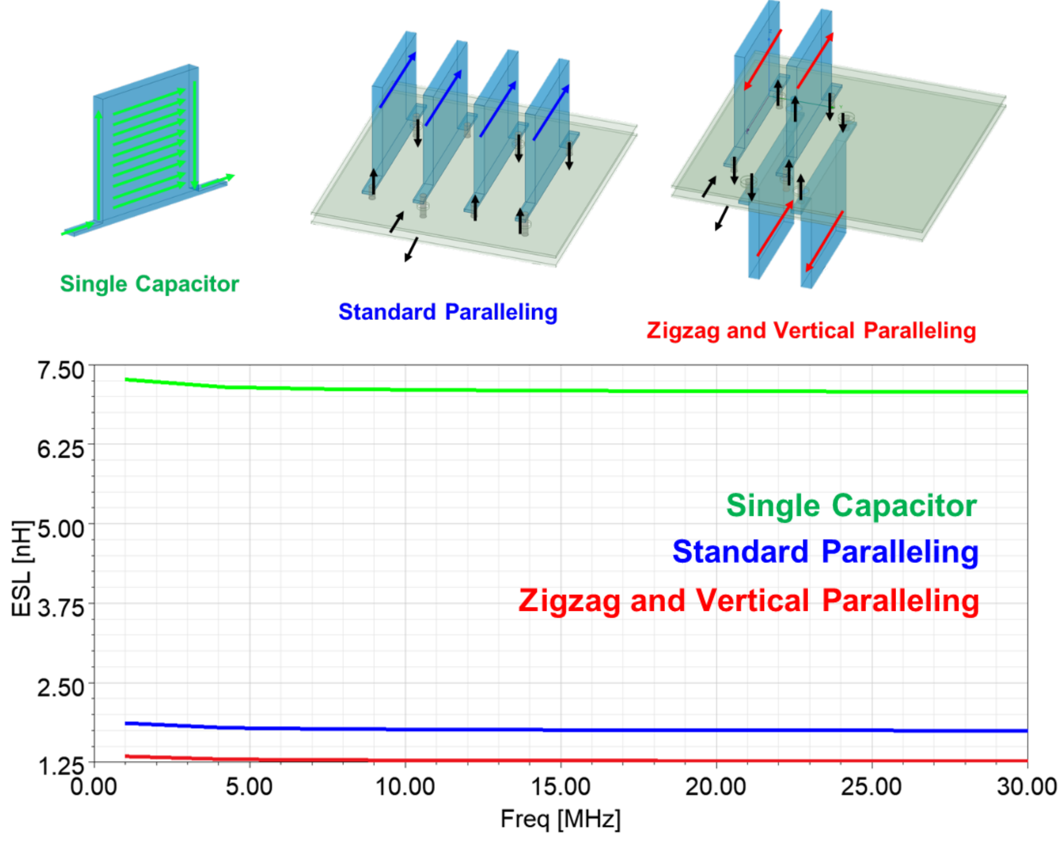


Fig. 3.13 Capacitor paralleling configurations

The mutual inductive coupling between the CM choke leakage and the ESL of the DM capacitor is then investigated through voltage gain measurements using Agilent 4395A Network Analyzer. To study the inductive coupling corresponding to the relative orientation between the capacitor and the inductor, the capacitor is oriented to be perpendicular or parallel to the inductor winding. Fig. 3.14 shows the schematic of the LC test setup and the two physical placements under study.

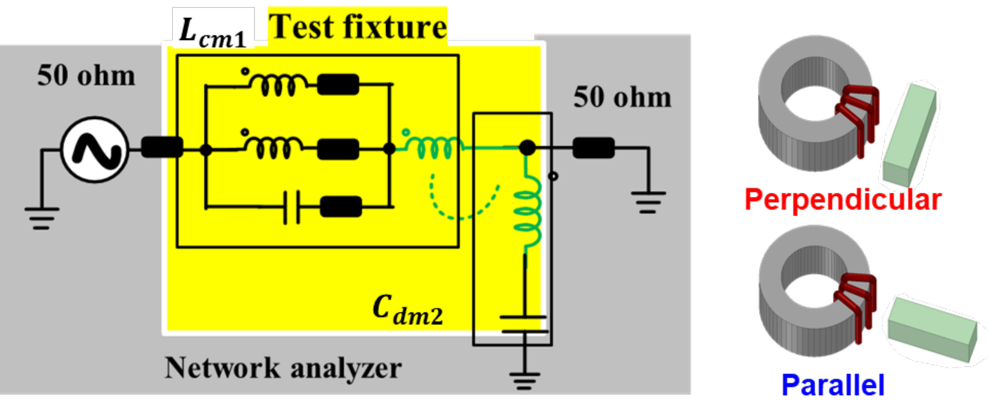


Fig. 3.14 LC test setup and test cases under study

The measured voltage gain for the two placement is compared in Fig. 3.15. The perpendicular placement shows a 3dB improvement after 650 kHz compared to the parallel placement. This is due to the minimal inductive coupling when the capacitor is placed perpendicular to the inductor windings, where the magnetic flux lines for the two are mutually perpendicular to each other. Fig. 3.16 shows the simulation model of the LC test setup and the voltage gain corresponding to different coupling coefficient. With a higher coupling coefficient between the inductor leakage and the ESL of the capacitor, the resonance point f_0 is shifting to a lower frequency and thus results in a higher voltage gain after the resonant point. This demonstrates a good agreement with the measurement results.

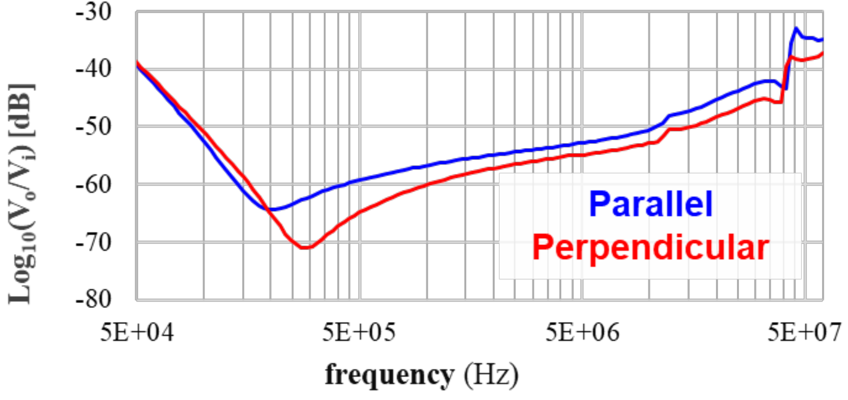


Fig. 3.15 Voltage gain comparison

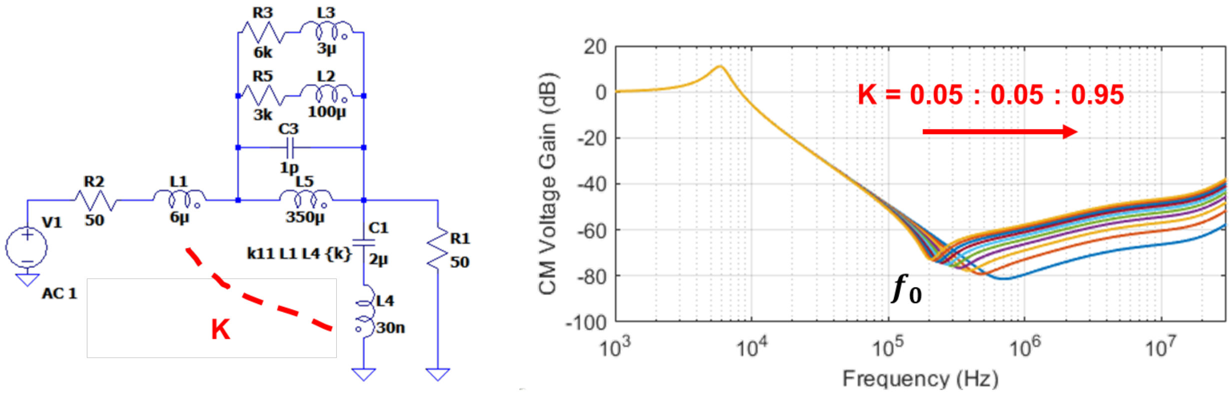


Fig. 3.16 Simulation of the LC setup

Finally, the second CM choke is added to form the LCL filter stage. The T-type coupling is investigated through voltage gain measurements with different relative orientations of the CM chokes. The two chokes are oriented along 'x' axis (namely 'side by side'), 'z' axis (namely 'vertical') or placed to be perpendicular to each other. **Error! Reference source not found.** shows the schematic of the LCL test setup and the three physical placements under study. It should be noted that same length of interconnections is used to maintain the same stray inductances for all test cases. Besides, the location of the capacitor and the distance between the CM chokes are fixed. In this way, only the relative orientation of the chokes is altered. The voltage gain measurements are compared in Fig. 3.18 (a). The lowest coupling was found when the CM chokes are stacked vertically along 'z' axis. This is due to the geometry of the core where the winding along the side of the core contributes to the magnetic flux along 'x' and 'y' axes while the winding along the outer radius to the inner radius (namely 'width') contributes to the magnetic flux along the 'z' axis. Fig. 3.18 (b) shows the prototype of the selected nanocrystalline toroidal core FT-3KM F4535G from Proterial Ltd. Since the depth of the core (50 mm) is relatively higher compared to the width of the core (18 mm), the majority of the flux lines are coupled along the 'x' and 'y' axes. Therefore,

the lowest T-type coupling could be achieved by arranging the selected CM chokes in a 'vertical' arrangement.

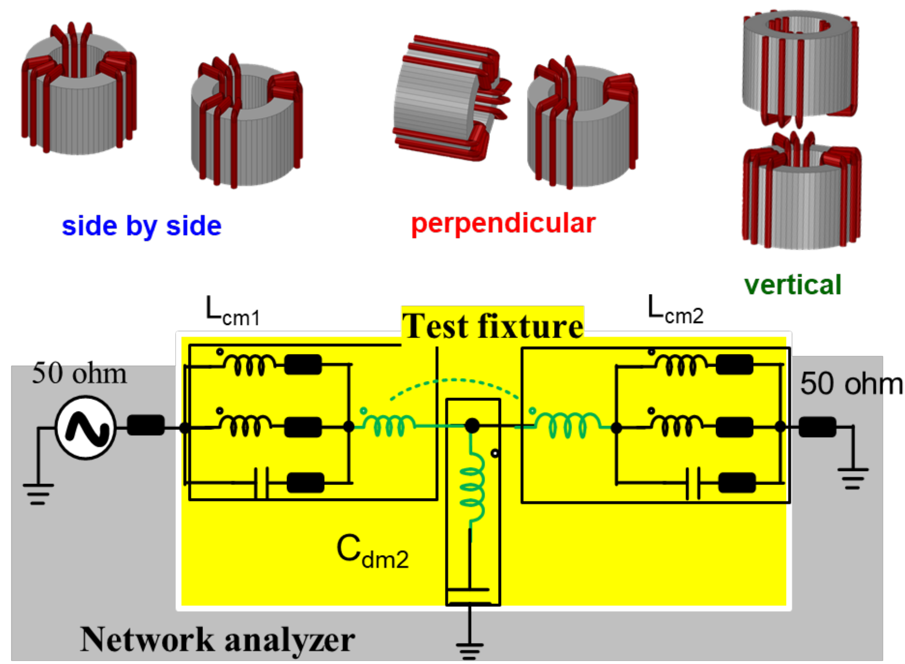


Fig. 3.17 LCL test setup and test cases under study

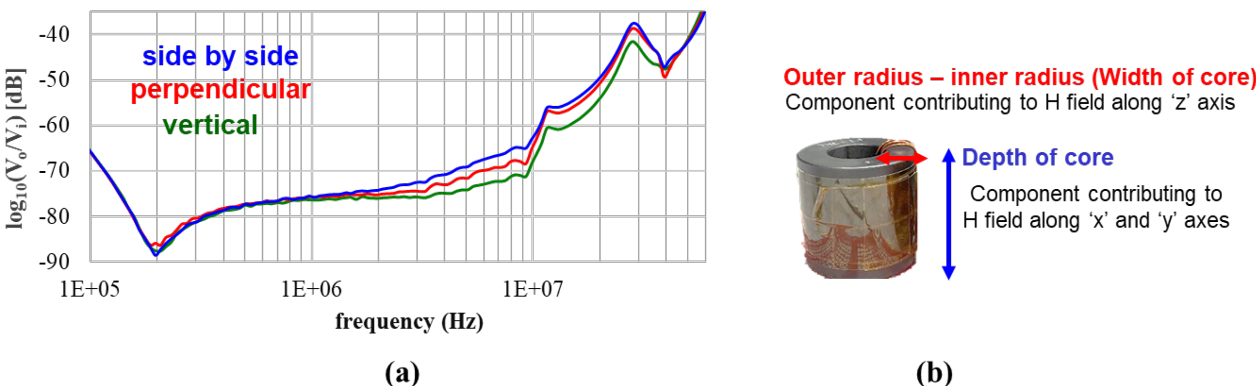
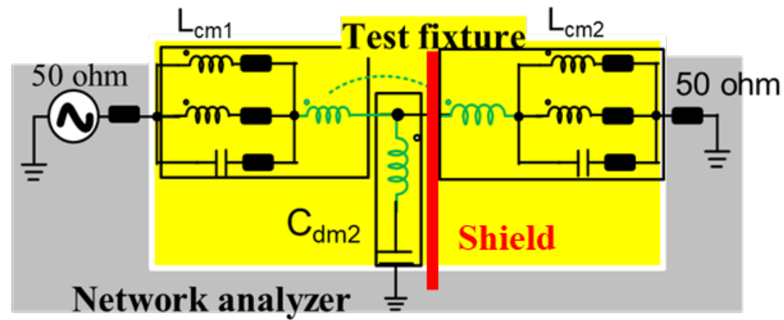


Fig. 3.18 (a) Voltage gain comparison (b) Geometry of the CM choke

To further reduce the inductive coupling along the 'z' axis, a floating 0.016" copper sheet is introduced between the CM chokes to draw the magnetic flux. Almost 10 dB improvement is

achieved after 3 MHz when a magnetic shield is added in between the chokes for the vertical configuration as per Fig. 3.19.



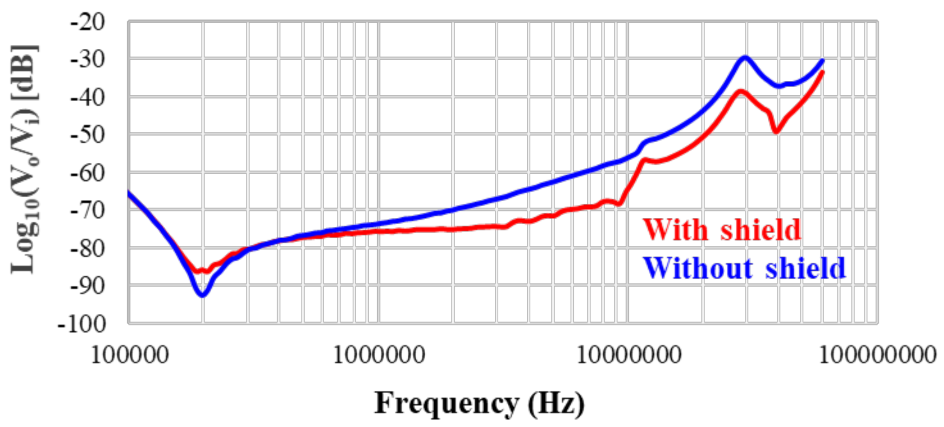


Fig. 3.19 Voltage gain comparison

The winding configuration of the three-phase CM choke is also investigated to reduce the 'z' axis coupling. The split-wound solution is introduced with the winding structure visualized in Fig. 3.20 (a). The winding for each phase is split into two and interleaved between the other two phases. The flux components generated along the 'z' axis from one side of the winding is cancelled by the flux components generated from the split winding in the opposite sides. Fig. 3.21 shows the simulated magnetic field distribution between the CM chokes in Ansys Maxwell 3D. The two chokes are stacked vertically with a 22 mm separation. A 1.15 A CM current is excited for each phase at 10 MHz. Clearly, the split-wound solution has a much lower magnetic flux density than

the traditional-wound solution. This is also verified through voltage gain measurement in Fig. 3.20 (b) with the LCL setup per Fig. 3.17.

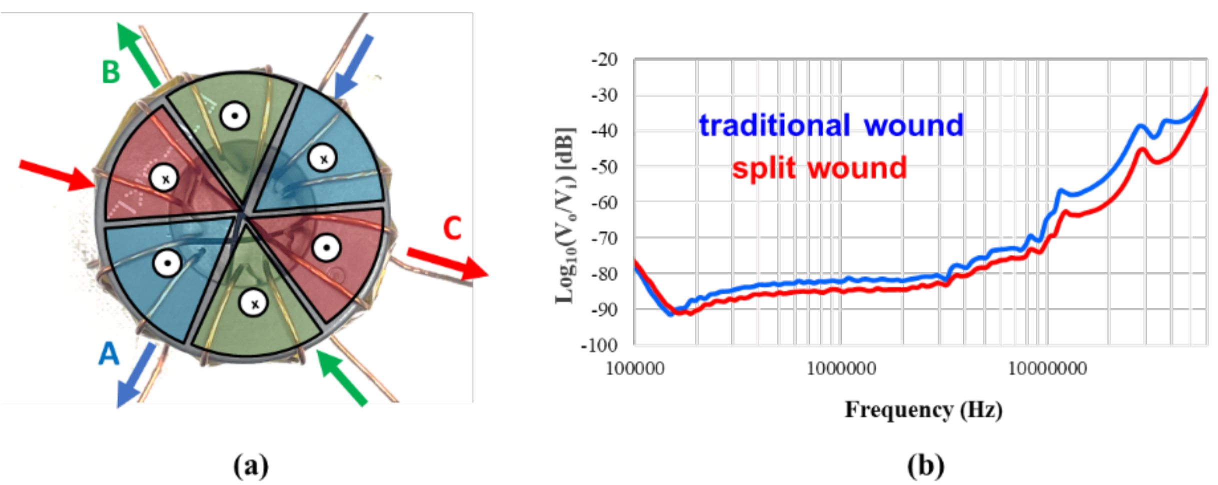


Fig. 3.20 (a) Split wound structure (b) Voltage gain comparison

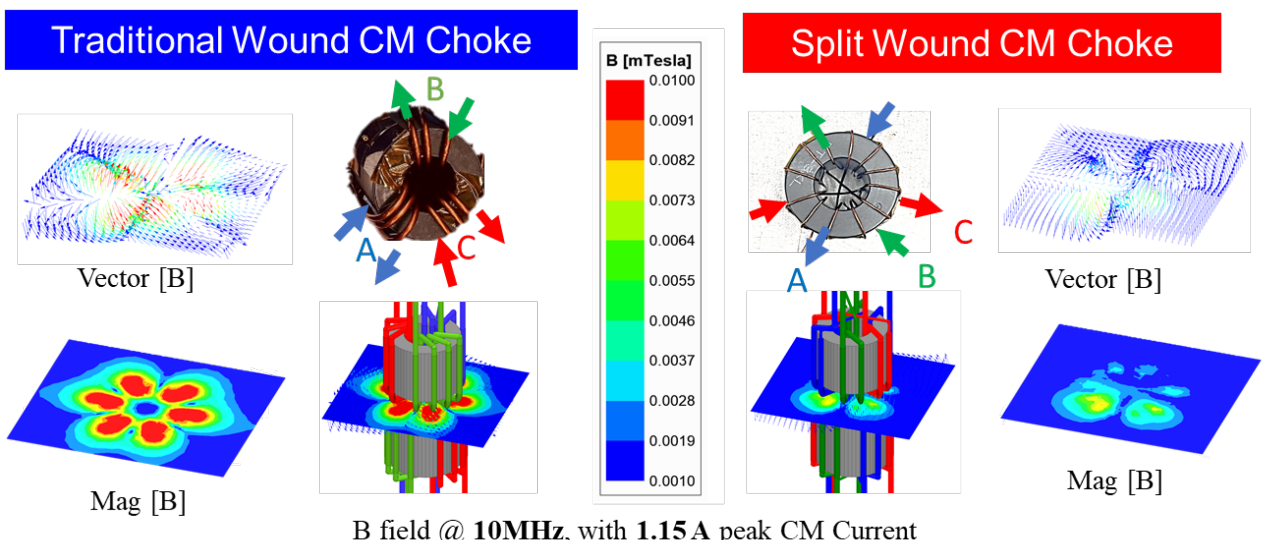


Fig. 3.21 Simulation of the magnetic field distribution

3.3.2 Design of Ground Connections and PCB Layout

The prototype of the full-scale filter employing the proposed methodologies is developed in this section. Fig. 3.22 shows the schematic and structure of the full-scale grid-side filter. Two

daughter boards are designed and inserted on the mother board to implement the ‘vertical’ orientation of the CM chokes.

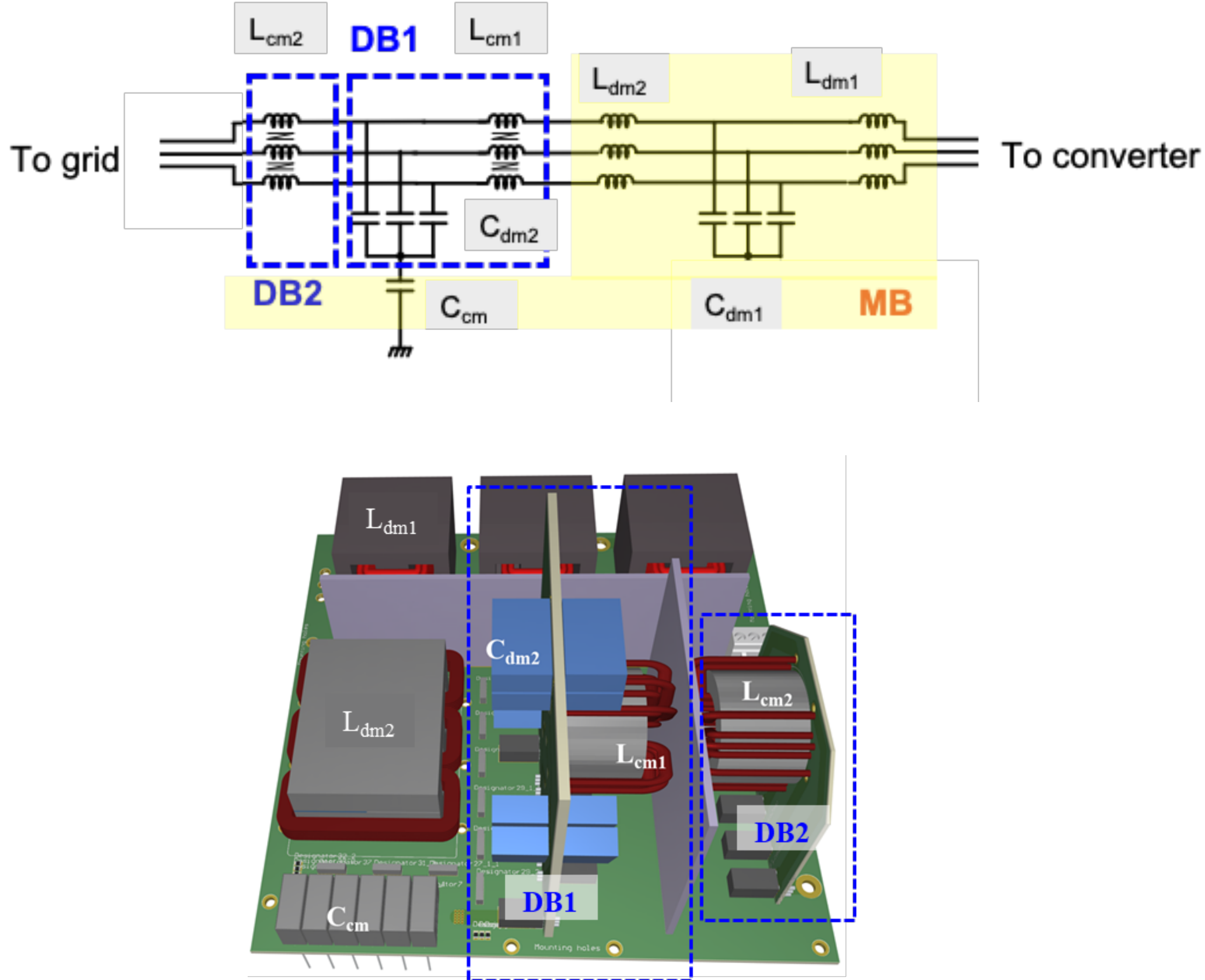


Fig. 3.22 Schematic and structure of the full-scale grid-side filter

Daughter board 1 (DB1) accommodates L_{cm1} and C_{dm2} as shown in Fig. 3.23. C_{dm2} each phase is composed of four film capacitors paralleling in ‘zig-zag’ and ‘vertical interleaved’ arrangement to achieve a lower ESL compared to a single capacitor. Besides, the film capacitors and the windings of the CM choke are placed ‘perpendicular’ to each other in order to reduce the inductive coupling between the two.

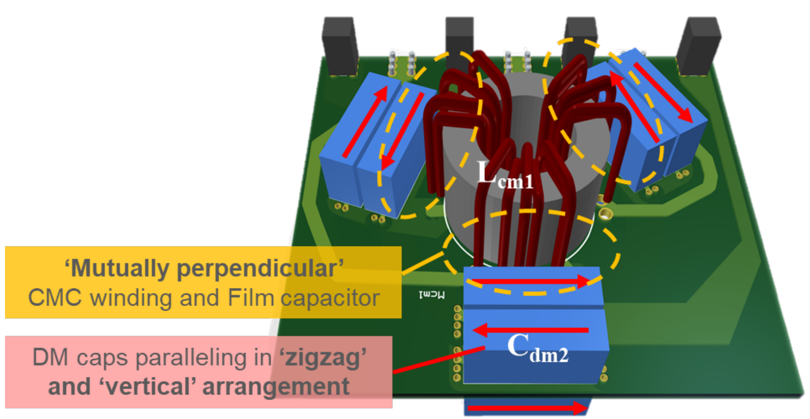
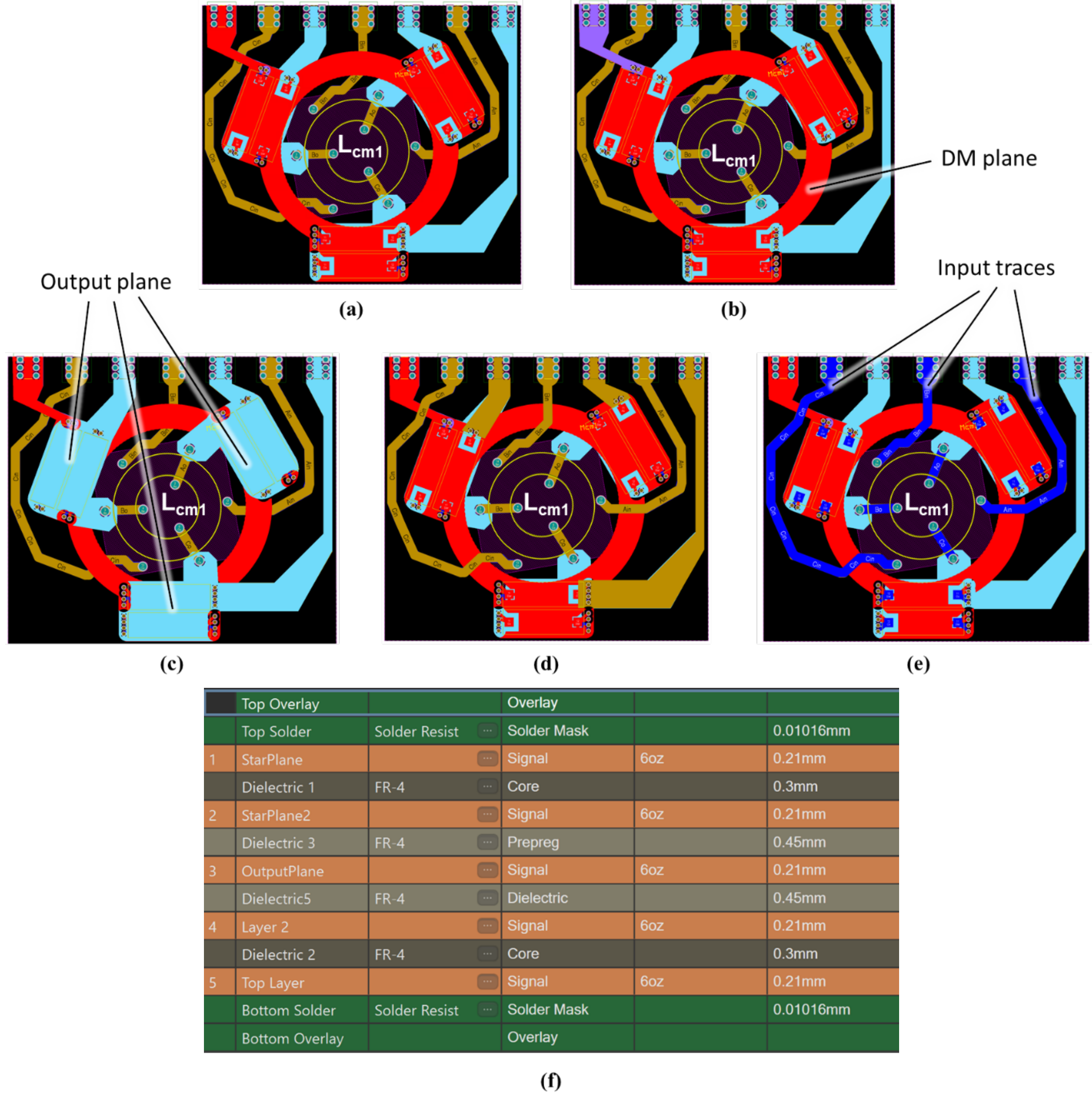


Fig. 3.23 Structure of daughter board 1 (DB1)

The 5-layer PCB layout and board stack-up for daughter board 1 is shown in Fig. 3.24. The DM plane is assigned at the top two layers while the power traces are assigned at the bottom three layers. The separation between the second and the third layer is 0.45 mm. This layer arrangement reduces the capacitive coupling between the power traces and the DM plane. A paralleling of two 6 oz copper layer is applied to all power traces to handle a 30 Arms current as well as the output of the DM plane to reduce the parasitic inductance between C_{dm2} and C_{cm} on the mother board (MB). It should be noted that the overlap of the input and output traces of the CM choke is avoided to minimize the feed-forward coupling.

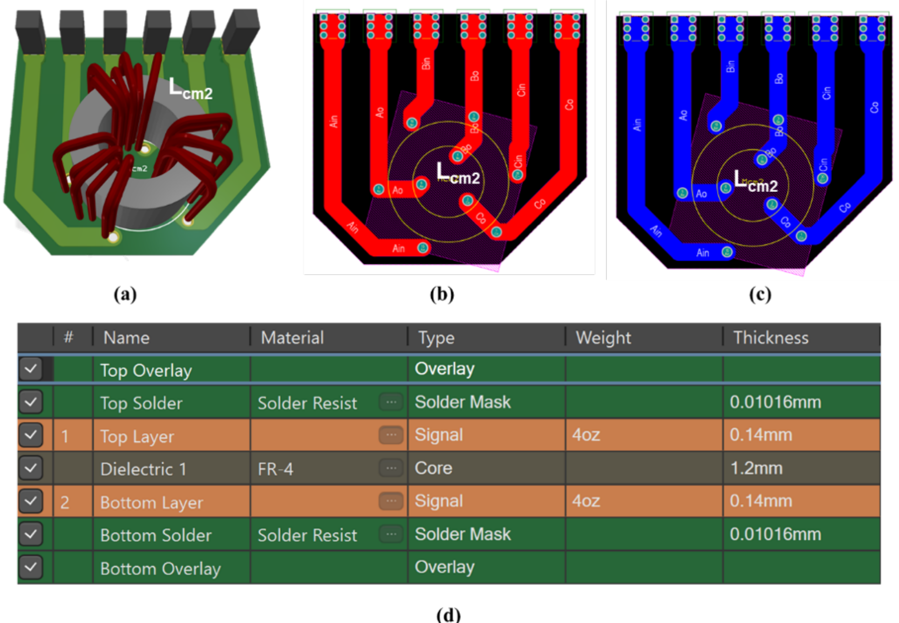


#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	StarPlane		Signal	6oz	0.21mm
	Dielectric 1	FR-4	Core		0.3mm
2	StarPlane2		Signal	6oz	0.21mm
	Dielectric 3	FR-4	Prepreg		0.45mm
3	OutputPlane		Signal	6oz	0.21mm
	Dielectric5	FR-4	Dielectric		0.45mm
4	Layer 2		Signal	6oz	0.21mm
	Dielectric 2	FR-4	Core		0.3mm
5	Top Layer		Signal	6oz	0.21mm
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm
	Bottom Overlay		Overlay		

Fig. 3.24 Daughter board 1 PCB layout (a) Top Layer (red) (b) Second Layer (purple) (c) Third Layer (sky blue) (d) Fourth Layer (brown) (e) Bottom Layer (blue) (f) Layer stack-up

Daughter board 2 (DB2) only accommodates Lcm2 as shown in Fig. 3.25 (a). By splitting the CM LCL filter into two daughter boards in this configuration, the input and output traces at the T-junction is avoided. In addition, the inductive coupling between C_{dm1} and L_{cm2} can be minimized when an inductive shield is inserted between the two daughter boards. The 2-layer PCB layout and board stack-up for daughter board 2 is shown in Fig. 3.25 (b)(c)(d). Since the trace width in DB2

(5 mm) is wider compared to the traces in DB1 (3 mm), a paralleling for the two 4oz copper layer is enough to handle the 30 Arms current for all traces in DB2.

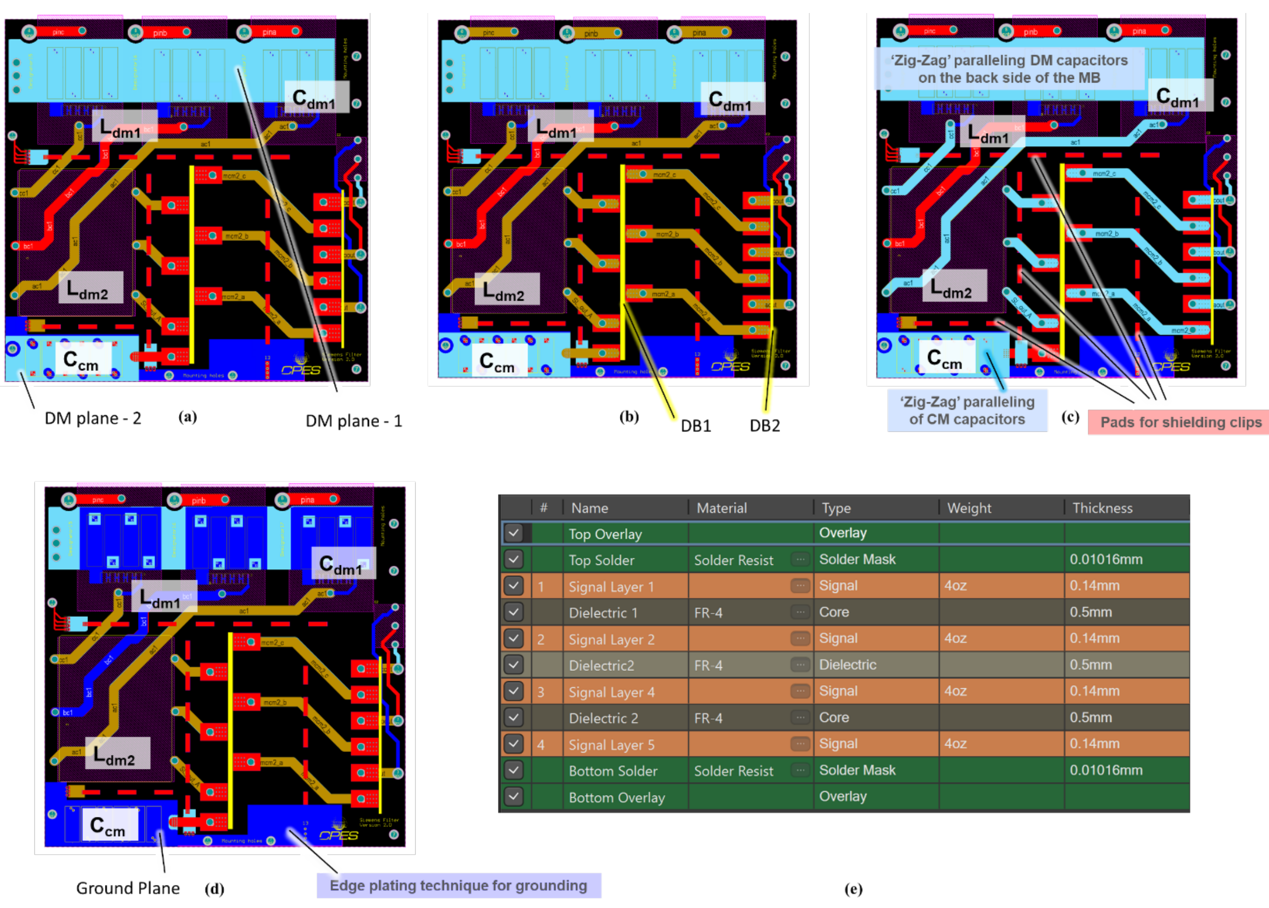


#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	Top Layer		Signal	4oz	0.14mm
	Dielectric 1	FR-4	Core		1.2mm
2	Bottom Layer		Signal	4oz	0.14mm
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm
	Bottom Overlay		Overlay		

Fig. 3.25 (a) Structure of Daughter board 2 (DB2) (b) DB2 Top Layer (red) (c) DB2 Bottom Layer (blue) (d) Layer stack-up

The mother board accommodates the full DM LCL stage and the CM capacitor (C_{cm}) from the CM LCL stage, as shown in Fig. 3.22. The edge-wound boost inductors are implemented to eliminate the anti-resonance below 30 MHz. The C_{dm1} each phase is composed of four film capacitors paralleling in ‘zig-zag’ arrangement on the back side of the board right below the boost inductor. The C_{cm} is composed of six film capacitors paralleling in ‘zigzag’ arrangement at the edge of the mother board. The 4-layer PCB layout and board stack-up for mother board is shown in Fig. 3.26. Pads for shielding clips between two different components has been assigned to facilitate the validation of the mutual coupling effects in the experiments. The pads could be removed at the areas where the coupling is verified to be insignificant. The large ground plane underneath the power traces in the baseline filter has been eliminated to avoid the feed-forward coupling effects at high frequency. Instead, a smaller ground plane has been assigned at the edge

of the board without overlapping any power traces. This ground plane location also allows the implementation of the edge plating technique [35, 62], where a low impedance from the CM capacitor to the system ground can be achieved. The edge-plating technique is visualized in Fig. 3.27, where the PCB ground plane is exposed with conductive solder mask on the back side of the board and stacked on the aluminum enclosure through brass screws and nuts. These screws and nuts ensure good electric conductivity and mechanical support between the PCB and the enclosure. A paralleling of two 4 oz copper layer is applied to all power traces to handle the 30 Arms current in the mother board.



#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	Signal Layer 1		Signal	4oz	0.14mm
	Dielectric 1	FR-4	Core		0.5mm
2	Signal Layer 2		Signal	4oz	0.14mm
	Dielectric2	FR-4	Dielectric		0.5mm
3	Signal Layer 4		Signal	4oz	0.14mm
	Dielectric 2	FR-4	Core		0.5mm
4	Signal Layer 5		Signal	4oz	0.14mm
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm
	Bottom Overlay		Overlay		

Fig. 3.26 Mother board PCB layout (a) Top Layer (red) (b) Second Layer (brown) (c) Third Layer (sky blue) (d) Fourth Layer (blue) (e) Layer stack-up

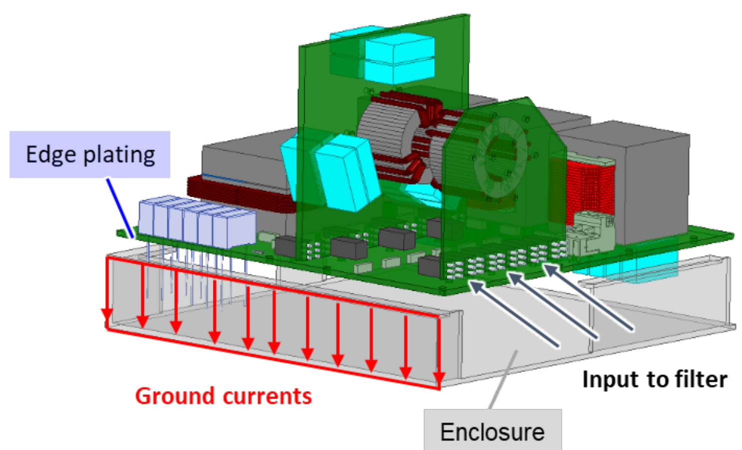


Fig. 3.27 Filter grounding structure

3.4 Summary

This chapter presents the multi-objective design of the critical passive components identified in Chapter 2. The key findings throughout the design process as well as the methods proposed to compensate the self and mutual parasitic effects are summarized below.

1. The sequential winding sequence of the traditional two-layered boost inductor is observed to have a high discontinuity in parasitic capacitance within the windings, which in turn leads to the anti-resonance phenomenon.

2. Single-layered edgewise winding as well as two-layered 'zigzag' winding using planar PCB have been proposed to minimize the parasitic capacitance between any two adjacent turns, which eliminate the antiresonance effect up to 30 MHz.

3. Paralleling multiple film capacitors using 'vertical interleaved' arrangement to achieve a lower net ESL compared to a single capacitor.

4. Placing the DM capacitor ($C_{dm2,\ grid}$) and windings of the CM choke in a 'perpendicular' arrangement to reduce the inductive coupling M_1.

5. Orienting the two CM chokes along the ‘z’ axis to reduce the inductive coupling M_2. Magnetic shield could be introduced in between the CM chokes absorb the flux leakage.
6. Using ‘split-wound’ winding configuration for the CM chokes to further reduce the magnetic flux along ‘z’ axis.
7. Grounding the filter using ‘edge-plating’ technique to reduce the ground impedance L_{gnd}.
8. Assigning a ground plane without overlapping power traces to reduce the mutual capacitive coupling C_{PCB}.

The prototype of the full filter structure is developed based on the proposed methodologies and will be constructed and tested for validation in the next chapter.

Chapter 4 Experimental Evaluation of Improved Filter

4.1 Introduction

The effectiveness of the proposed grid-side filter structure is validated through emission characterization using the three-phase motor drive system shown in Fig. 4.1. The grid- and inverter-side filters are constructed and assembled with 15 kW rated 3L-NPC units arranged in the B2B fashion. The cable, load bank and motor impedance board are added externally. A benchtop oscilloscope is used to measure the LISN phase voltages, which are then post-processed to compute the DM and CM frequency spectra. The system specification is listed in Table 4-1 while the physical parameters of the prototype are summarized in Table 4-2.

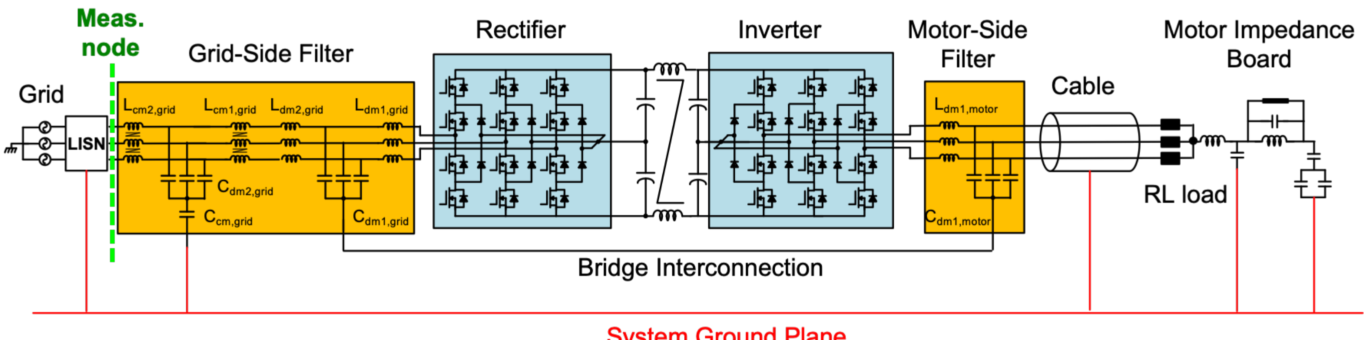


Fig. 4.1 Schematic of the three-phase motor drive test bed

Table 4-1 System Parameters

Parameters	***Value***
Power Rating	15 kW
Line Voltage	400 *VAC*
DC-Bus Voltage	650 V
Line Frequency	60 Hz
Switching Frequency	48 kHz
MI_{grid} ($2V_{grid(1)}^{ref}/V_{dc}$)	0.87
MI_{inv} ($2V_{inv(1)}^{ref}/V_{dc}$)	0.99 at rated speed

Table 4-2 3L-NPC Prototype and B2B Components

Component	***Value***	***Details***
Semiconductors	f_{sw} = 48 kHz	Microchip, SiC 3L-NPC Phase Leg, APTMC603LCT3AG, 1.2 kV, 48 A
Grid-Side Components	$L_{dm1,\ grid}$ = 100 μH	Powder Core, EMS-0432115-040 (2X), n = 25, A_e = 366 mm^2 , AL = 216 nH/T^2
	$L_{dm2,\ grid}$ = 50 μH	Amorphous, 2xE cores clamped l_g = 1 mm, n = 4, A_e = 450 mm^2
	$L_{cm1,\ grid}$ = 300 μH	Nanocrystalline, FT-3KM F4535G (2X), A_L = 4.1 $\mu H/T^2$, n = 3, A_e = 300 mm^2
	$L_{cm2,\ grid}$ = 300 μH	Nanocrystalline, FT-3KM F4535G (2X), A_L = 4.1 $\mu H/T^2$, n = 3, A_e = 300 mm^2
	$C_{dm1,\ grid}$ = 2 μH	Film capacitor, B32754C8205K000, 350 VAC, 2 μF (Same spec for $C_{dm2,\ grid}$)
Inverter Side Components	$L_{dm1,\ motor}$ = 50 μH	Powder Core, EMS-0432115-040, n = 25, A_e = 183 mm^2 , A_L = 108 nH/T^2
	$C_{dm1,\ motor}$ = 2 μH	Film capacitor, B32754C8205K000, 350 VAC, 2 μF
DC Side Components	$L_{cm1,\ dc}$ = 300 μH	Nanocrystalline, FT-8K50D F4535G, n = 6, A_L = 21 $\mu H/T^2$

4.2 Experimental Results

4.2.1 Inductive Coupling Validation

The T-type inductive coupling in the CM LCL filter stage is known to have a significant degradation on the DM noise suppression with a small coupling coefficient as discussed in Section 2.3.1. Section 3.3.1 proposed the 'vertical' arrangement of two CM chokes and a shield in between to reduce the inductive coupling between the leakage of the chokes. The different arrangement is verified with the full B2B system with the CM LCL stage on the grid-side filter. Fig. 4.2 shows the schematic of the system test setup. In this test, the boost inductor from the DM-LCL stage is also added to provide sufficient line impedance for the converter output at the grid side.

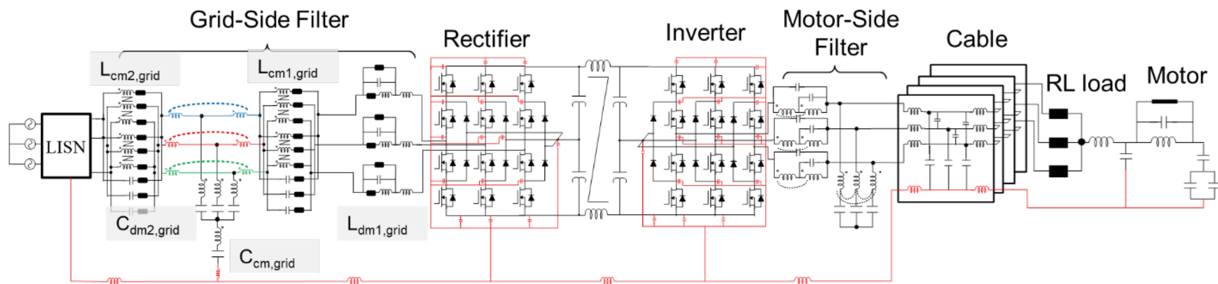


Fig. 4.2 System test setup with grid-side CM LCL filter

Fig. 4.3 shows the hardware for the three different orientations under study. Since the mother board and daughter boards are only designed to accommodate the CM chokes in a 'vertical' arrangement, the orientation tests are conducted by rotating the daughter boards outside the motherboard. Fixtures are customized to hold the daughter boards in different relative orientations. It should be noted that same length of interconnections between the mother board and the daughter boards are used to maintain the same stray inductances for all test cases. Besides, the distance between the CM chokes is fixed.

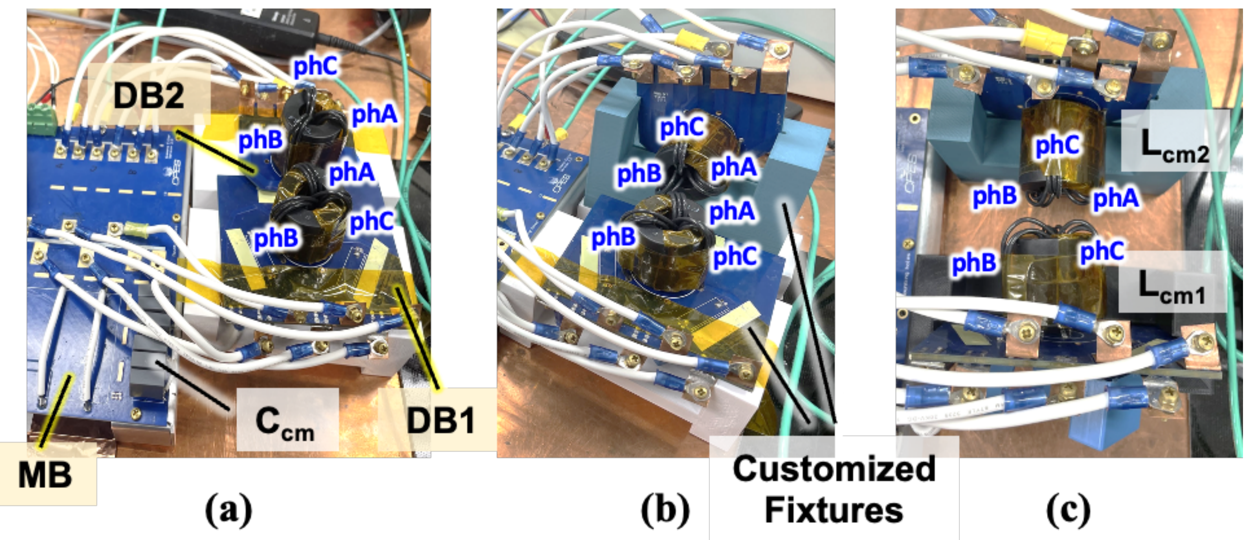


Fig. 4.3 Orientation under investigation (a) Side by side (b) Perpendicular (c) Vertical

The impact of the CM choke placement is verified in Fig. 4.4. The red trace indicates the 'side by side' arrangement of the CM chokes while the blue and green traces represent the 'perpendicular' and 'vertical' arrangement of the chokes. Clearly, the 'vertical' arrangement shows the lowest DM emission around 600 kHz to 3MHz compared to the other two configurations.

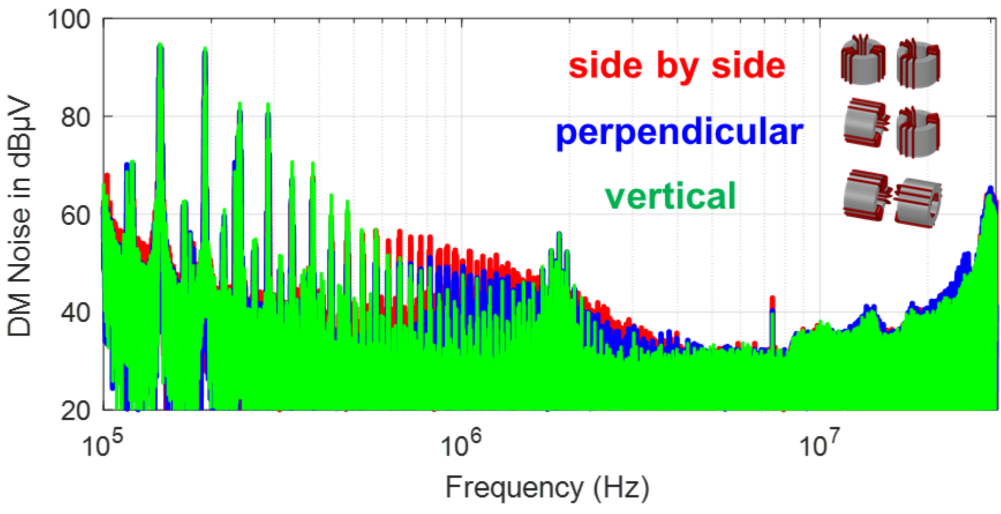


Fig. 4.4 DM noise comparison for CM choke orientations (phA)

The inductive coupling is highly related to the distance between the phase winding on one CM choke to another. Since the relative position of the different phase windings is dependent on

the relative orientation of the two CM chokes and may not be identical, as shown in Fig. 4.3, the DM emission for other two phases should also be considered to validate the effectiveness of the proposed CM chokes placement. Fig. 4.5 shows the DM emission for the other two phases. Obviously, the 'side by side' arrangement has a lower DM emission compared to the 'perpendicular' arrangement for phase C. This is because the windings for phase C in L_{cm1} is far away from all the windings in L_{cm2} for the 'side by side' arrangement. However, the 'vertical' arrangement still provides the best result for all three phases due to the lowest mutual coupling between the chokes as investigated in Section 3.3.1.

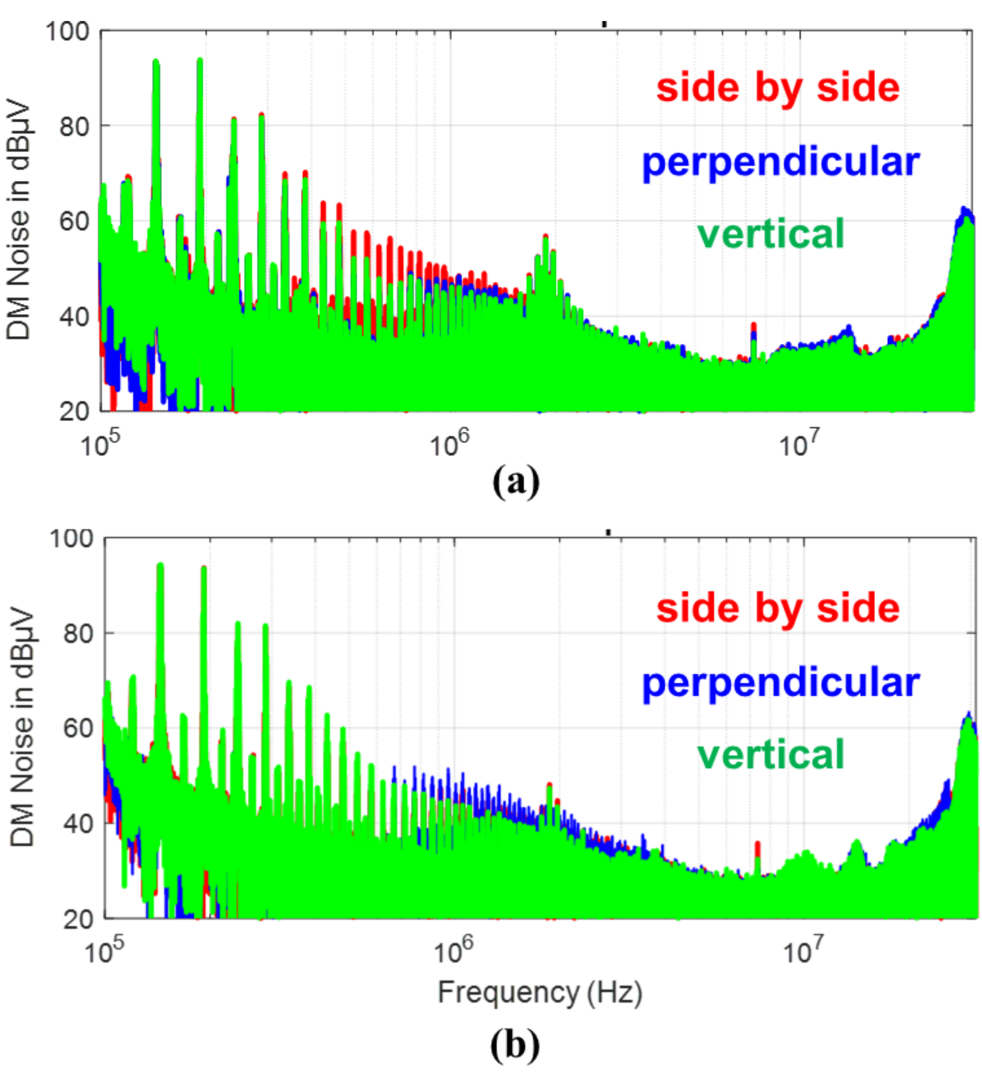


Fig. 4.5 DM noise comparison for CM choke orientations (a) phase B (c) phase C

The effectiveness of introducing a magnetic shield in between the CM chokes is demonstrated in Fig. 4.6 (a), where the CM chokes are mounted on the mother board in a 'vertical' arrangement, as shown in Fig. 4.6 (b). The blue trace corresponds to the case where a magnetic shield is inserted between the chokes, while the red trace corresponds to the case without shield. The magnetic shield is implemented by a floating 0.03" steel sheet. The DM noise is further suppressed within the same frequency range (600 kHz to 3MHz) when the magnetic shield is adopted.

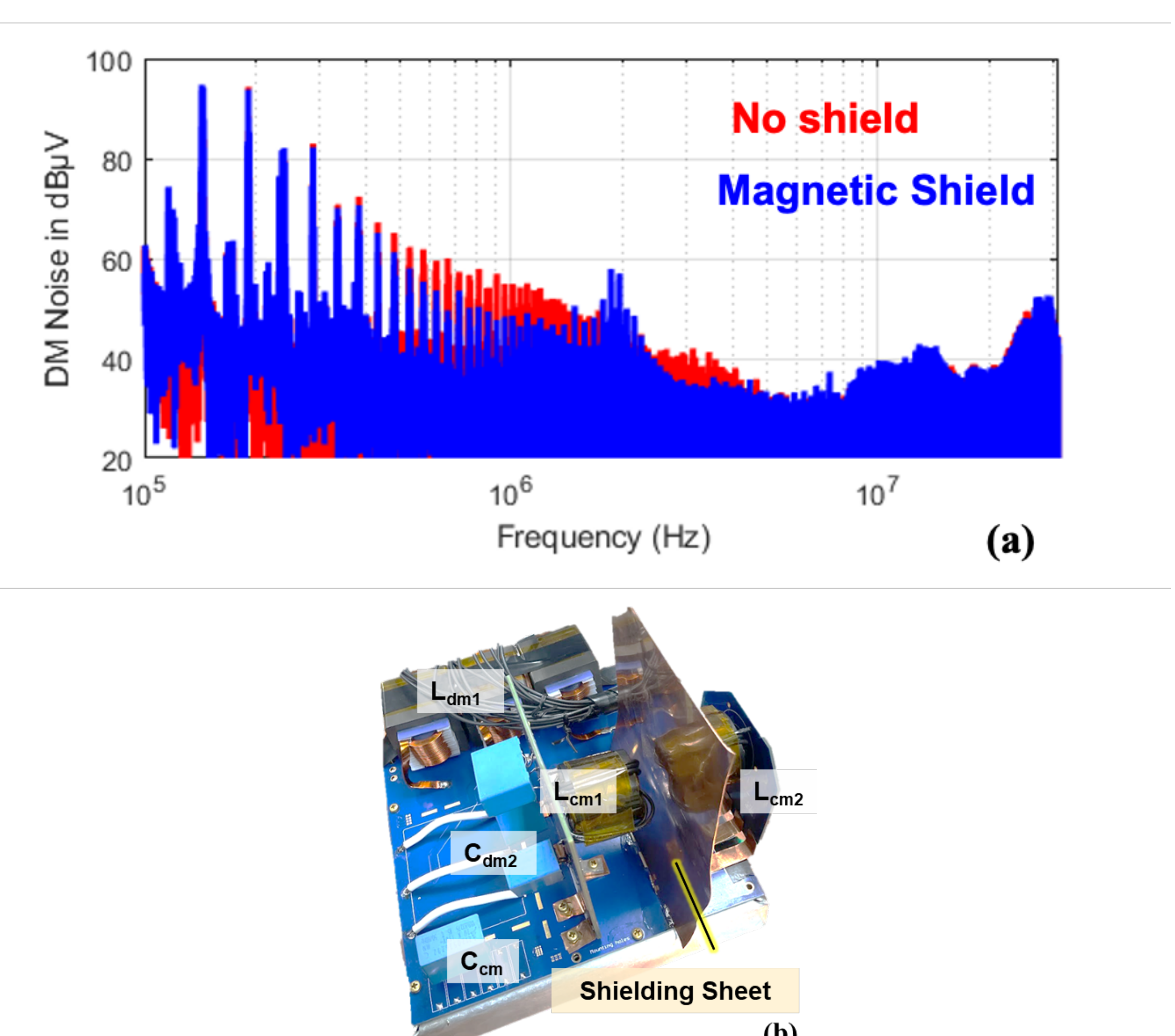
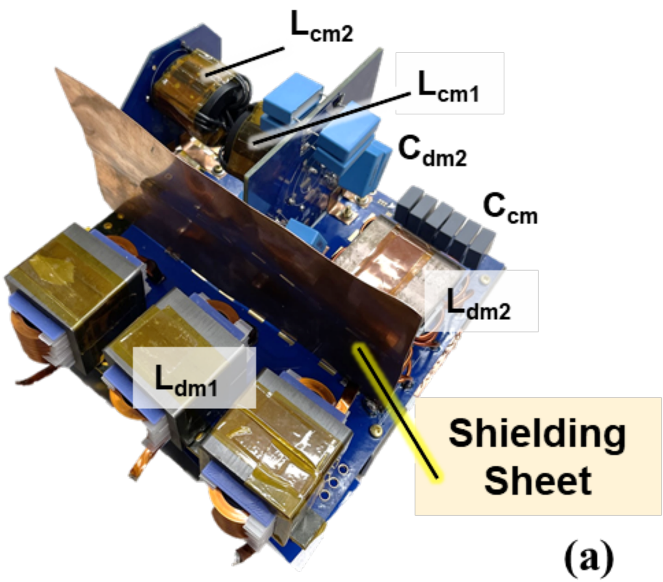


Fig. 4.6 (a) DM noise comparison for introducing magnetic shield between the CM chokes (b) Structure of the CM chokes with shielding sheet

4.2.2 Capacitive Coupling Validation

The capacitive coupling between stages of the EMI filter degrades the filter performance significantly, especially when a T-junction is included within the path of the two coupled components, as discussed in Section 2.3.2. To reduce the electric coupling between the boost inductor (L_{dm1}) from the DM filter stage and the CM chokes (L_{cm1}, L_{cm2}) from the CM filter stage, an electric shield is inserted at the interface as shown in Fig. 4.7 (a). The electric shield is implemented by a grounded 0.016" copper sheet. The effectiveness of the electric shield is verified with the full grid-side filter in the full B2B system, as shown in Fig. 4.8. Fig. 4.7 (b) shows the CM noise at the LISN terminal, where the blue trace corresponds to the use of an electric shield. A 5 dB CM noise suppression is observed after 3 MHz when the electric shield is added. In other words, the displacement current flowing from the DM stage to the CM stage has been bypassed to ground through the small capacitance induced between the filter component and the electric shield.



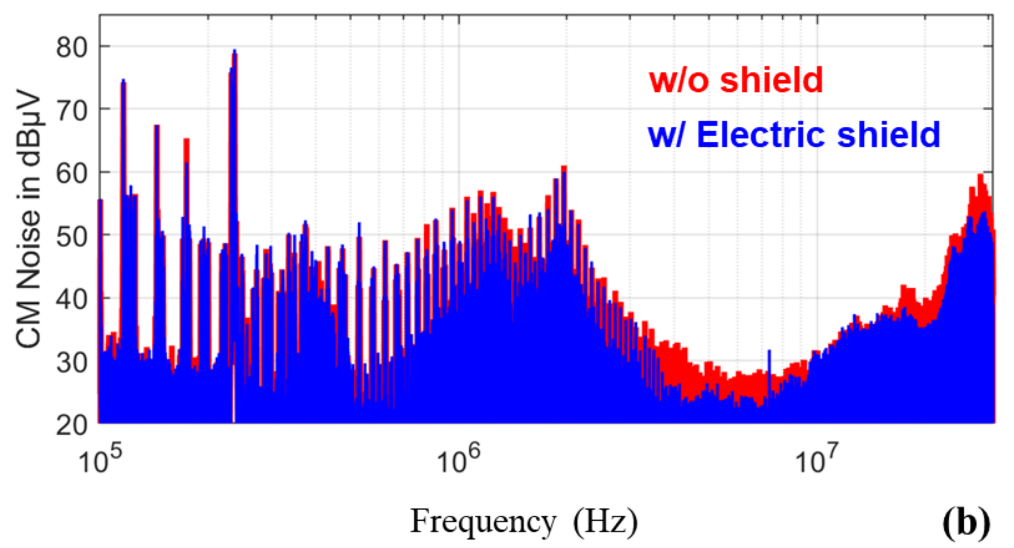


Fig. 4.7 (a) Structure of the shielding sheet in the full-scale grid-side filter (b) CM noise comparison for introducing electric shield between the boost inductor and the CM LCL filter stage

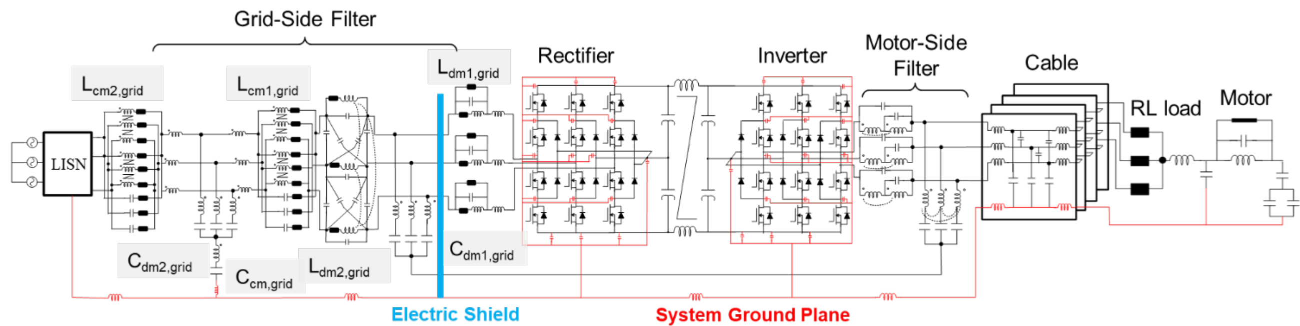


Fig. 4.8 System test setup with full grid-side filter

Another critical capacitive coupling occurs between the power traces and the large PCB ground plane in the baseline grid-side filter structure. The coupling is observed to bypass the CM LCL filter stage after tens of MHz, making the high conducted emission around the anti-resonance frequency (17 MHz) of the traditional wound boost inductor unattenuated, as discussed in Section 2.3.2. Section 3.3.2 proposed optimal PCB layout for filter interconnections as well as the ground connection for the CM capacitor (C_{cm}). Instead of having a large ground plane underneath CM filter stage, a small ground plane at the edge of the PCB board is designed to keep away from all the power traces. The effectiveness of the layout is demonstrated with the baseline and the

redesigned full grid-side filter in the full B2B system, as shown in Fig. 4.8. The two-layered traditional wound boost inductor is used in this test and all the filter components are maintained the same for the baseline and the redesigned filter.

Fig. 4.9 shows the impact of the PCB layout. Clearly, the high conducted emissions peak around the anti-resonant frequency (f_{res2}) has been greatly attenuated by the filter components instead of being bypassed to the LISN via large parasitic capacitances to ground in the baseline filter. It should be noted that a slightly larger distance (< 3 cm) between boost inductor and the CM choke within the redesigned filter also leads to a small improvement of the CM noise emission at tens of MHz due to a smaller electric coupling effect within the filter stages. Therefore, the attenuation of the anti-resonant frequency is still dominated by the improved PCB layout.

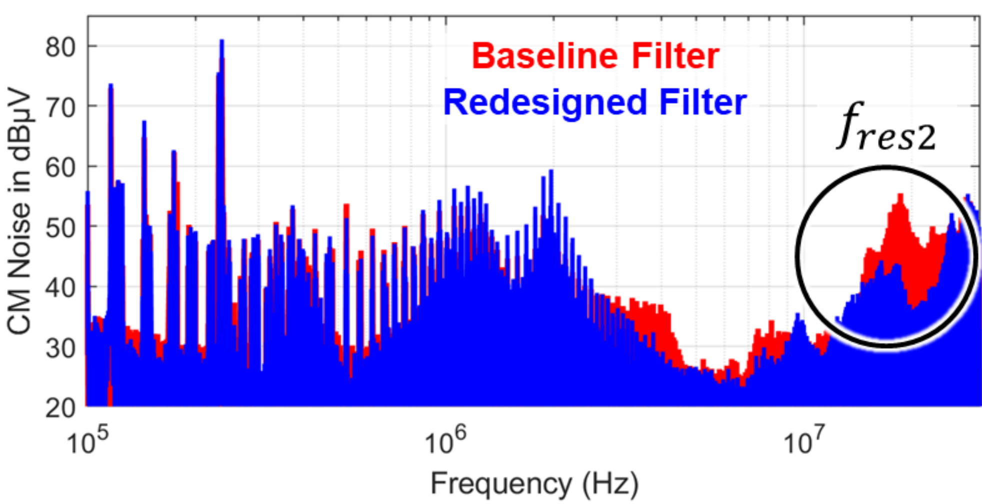


Fig. 4.9 CM noise comparison for PCB layouts with the full-scale grid-side filter using multi-layered traditional wound boost inductor

4.2.3 Self-Parasitic Components Validation

The effectiveness of the proposed edgewise wound boost inductor in Section 3.2 is verified with the full grid-side filter in the full B2B system, as shown in Fig. 4.8. Fig. 4.10 shows the voltage spectrum at the LISN terminal. The red trace indicates the baseline filter with traditional

wound boost inductor while the blue and green emission represents the redesigned filter with traditional wound and edgewise wound boost inductor respectively. The high conducted emissions peak around the anti-resonant frequency (f_{res2}) for the traditional wound boost inductor has been effectively attenuated due to minimal capacitive coupling between the power traces and the PCB ground plane in the redesigned filter as discussed in Section 4.2.1. However, with the edgewise wound boost inductor in the redesigned filter, the CM and DM emissions around the anti-resonance frequency could be suppressed further. This is due to a much larger impedance around f_{res2} for the edgewise solution compared to the traditional wound solution, as shown in Fig. 4.11. This in case results in a lower noise emission around f_{res2} as the noise emissions follows the inverted profile of the impedance curve.

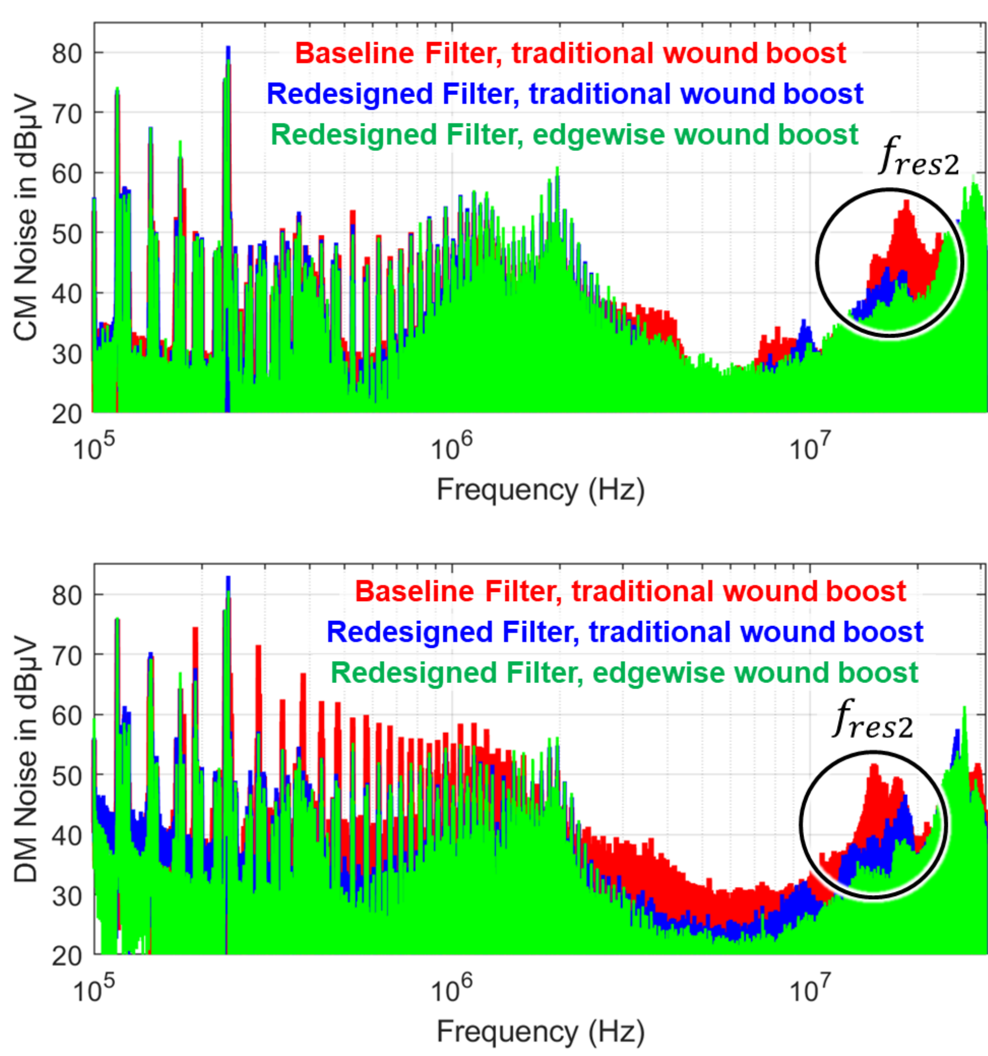


Fig. 4.10 EMI noise comparison for the winding configurations of the boost inductor with the full grid-side filter

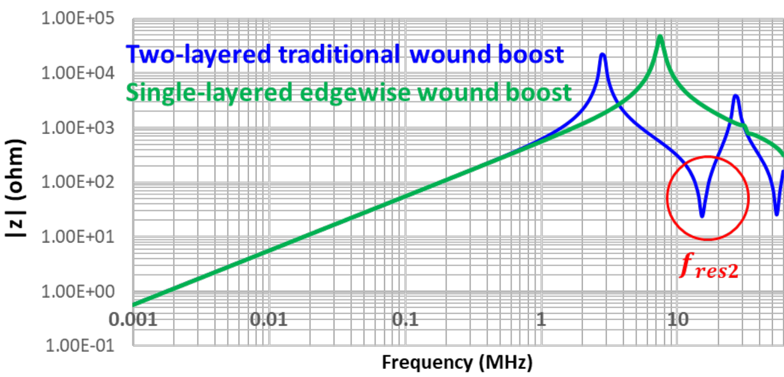


Fig. 4.11 Boost inductor impedance measurement

In the redesigned filter, multiple film capacitors are paralleled in a ‘zigzag’ configuration to reduce the effective ESL of the capacitor branch. However, the effect is usually being masked by the mutual coupling related to the capacitor branch. A single 2 μF DM capacitor and four 0.47 μF DM capacitors paralleling in a ‘zigzag’ configuration per phase is adopted to demonstrate the effect of paralleling multiple film capacitors. The ESL of the 2 μF capacitor and the 0.47 μF capacitor are 25 nH and 13 nH respectively, as shown in the impedance measurements in Fig. 4.12. The impact of the ESL for C_{dm1} is demonstrated with the DM LCL stage on the grid-side filter in the full B2B system. Fig. 4.13 shows the schematic of the test setup.

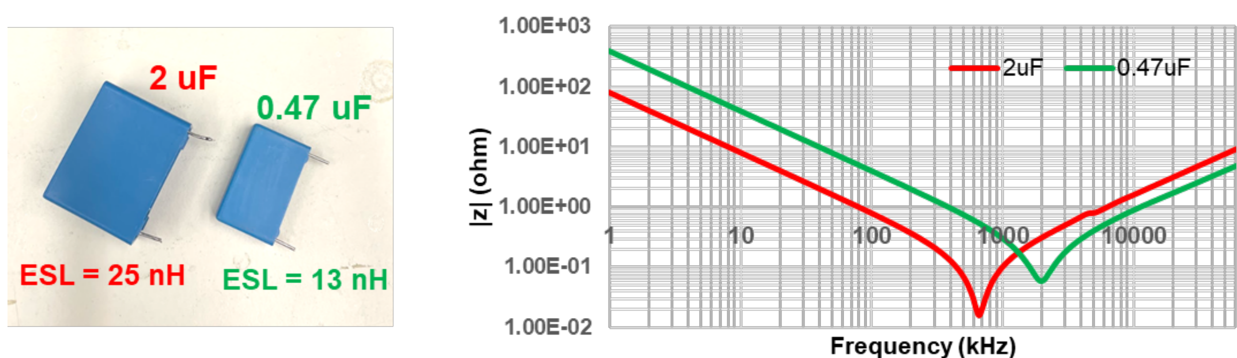


Fig. 4.12 Film capacitor impedance measurements

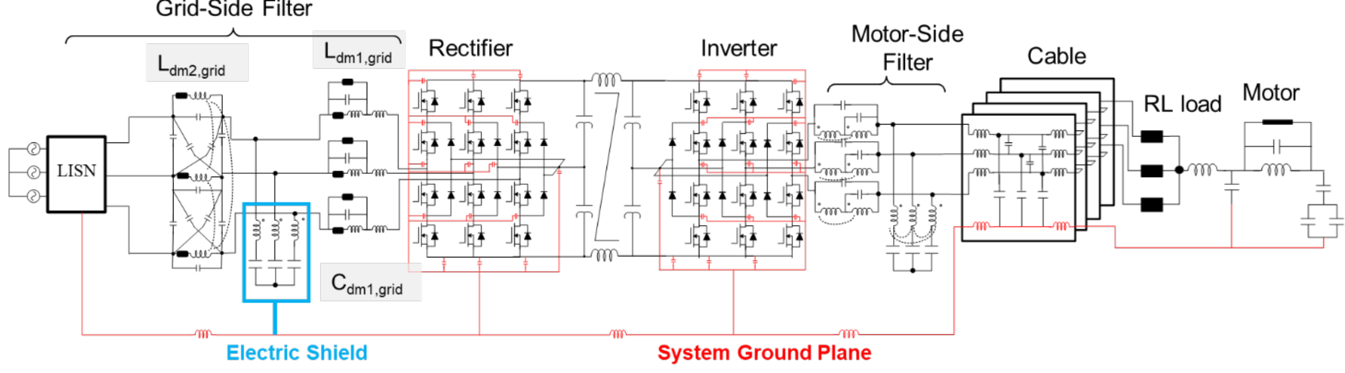


Fig. 4.13 System test setup with grid-side DM LCL filter

Fig. 4.14 shows the voltage spectrum at the LISN terminal. The red emission represents the DM LCL filter with a single capacitor or four capacitors in parallel for C_{dm1} since there is no difference between the noise emission for the two cases. However, when the DM capacitor is electrically

shielded, a 3 dB improvement can be observed in both CM and DM noise spectra when multiple film capacitors are connected in parallel. In other words, a strong electric coupling on the C_{dm1} branch is masking the effect of the capacitor ESL. This electric coupling occurs between the boost inductor (L_{dm1}) and the DM capacitor (C_{dm1}) as the two filter components are placed nearby on the motherboard. The electric shield is implemented by wrapping the copper foil tape around the film capacitor case and connecting the taped case to the system ground. Similarly, for the CM LCL filter stage, the effect of the ESL on the shunt capacitor branch, including the ESL of C_{dm2}, C_{cm} and the ground inductance L_{gnd}, due to the strong magnetic coupling between the first stage CM choke (L_{cm1}) and the second stage DM capacitor (C_{dm2}). The strong magnetic coupling between the choke and capacitor introduces a large mutual inductance on the shunt capacitor branch, making the self inductance contributed by the capacitors and the PCB traces on the path insensitive to the noise emission. Therefore, it is vital to minimize the mutual parasitic components before making attempts to reduce the self parasitic components as the mutual couplings dominate the high frequency performance of the EMI filter.

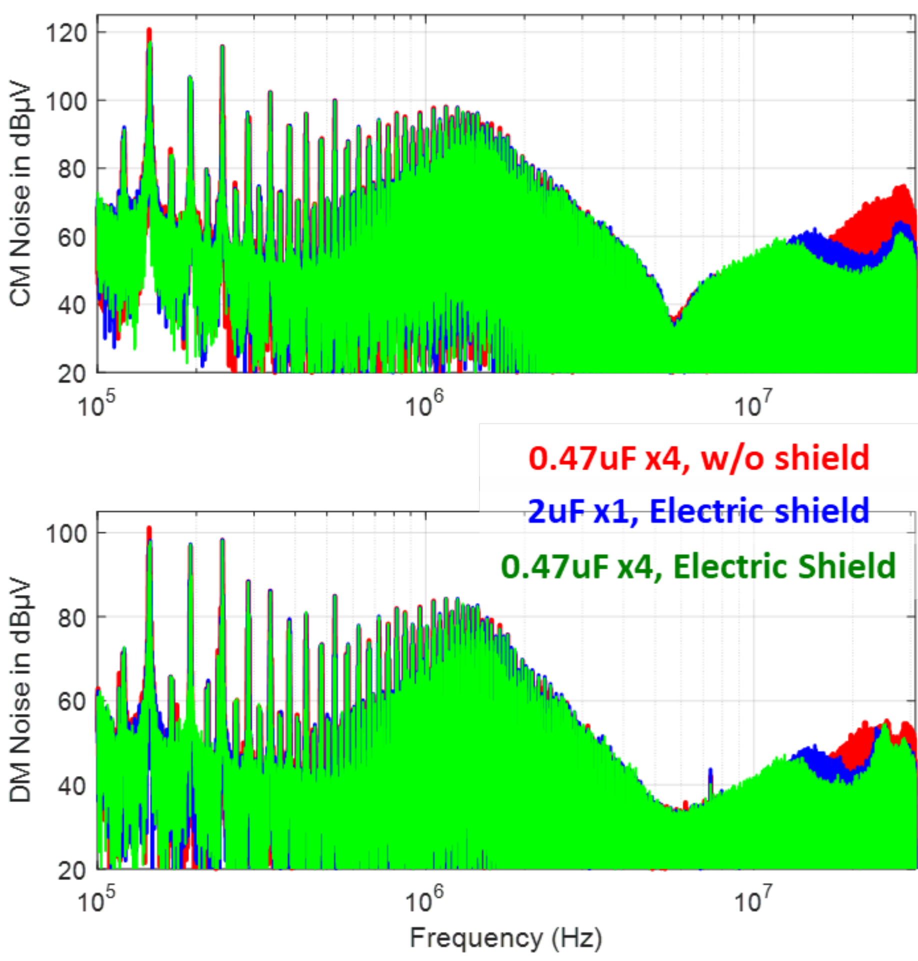


Fig. 4.14 EMI noise comparison for paralleling multiple film capacitors with DM LCL filter

4.3 Filter Performance Comparison

Finally, the performance of the redesigned filter and the baseline filter is compared in Fig. 4.16. A few observations from the EMC tests are highlighted. First, the high conducted emission peak around the anti-resonance frequency (f_{res2}) of the traditional wound boost inductor has been greatly attenuated (> 20 dBμV CM and DM noise suppression) in the redesigned filter due to minimized feedforward coupling capacitances (C_{PCB}) between the power traces and the ground plane in the redesigned PCB layout. Additional 5 dBμV DM noise attenuation is achieved around

f_{res2} by adopting the 'single-layered edgewise wound boost inductor' due to the lack of anti-resonance in the impedance characteristics of the edgewise wound solution.

The 'vertical' arrangement of the CM chokes reduces the mutual inductive coupling (M_2) in the T-junction, where a 10 dBμV DM noise improvement is observed compared to the baseline 'side by side' arrangement from 500 kHz – 5 MHz. Additional 5 dBμV DM noise attenuation is achieved at the same frequency range when a 'magnetic shield' is inserted between the chokes to absorb the magnetic flux. The introduction of the 'electric shield' between the boost inductor and the CM LCL stage reduces the capacitive coupling between the stages (C_{coup1} and C_{coup2}) with a 5 dBμV CM noise suppression above 3 MHz.

Fig. 4.15 shows the constructed hardware structure for the baseline grid-side filter and the redesigned grid-side filter. Since the proposed filter structure was only designed for minimal parasitic components instead of high power density, the volume of the redesigned filter is almost 50% larger than the baseline filter.

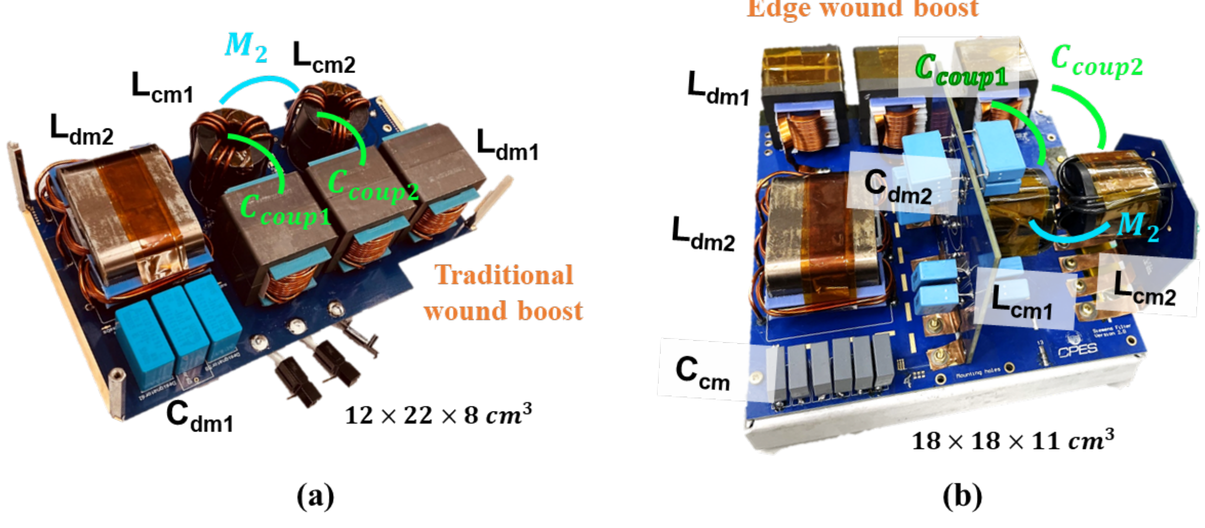


Fig. 4.15 (a) Baseline Filter (C_{dm2}/ C_{cm} placed on bottom side) (b) Redesigned Filter (C_{dm1} placed on bottom side).

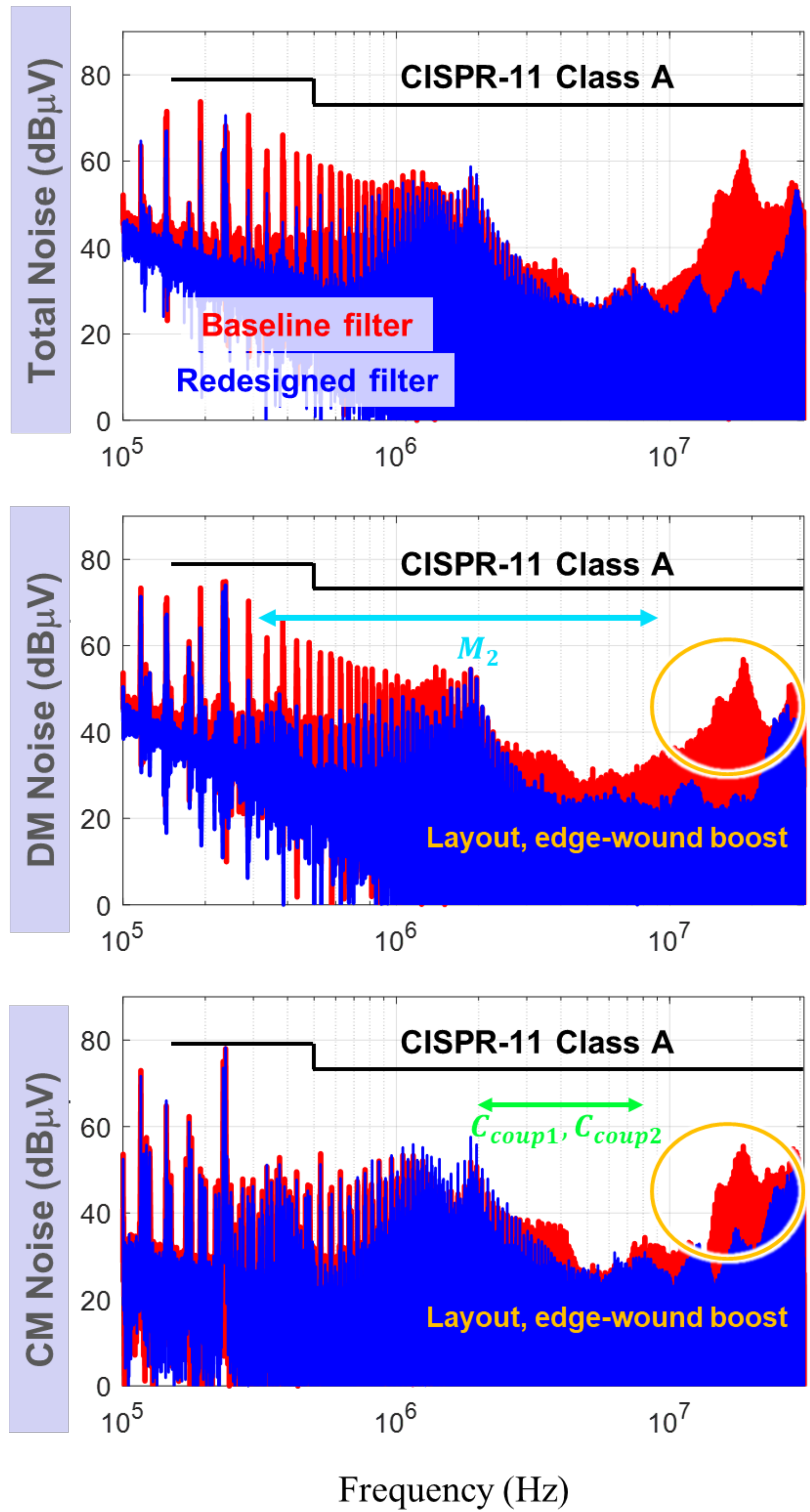


Fig. 4.16 EMI emission comparison

4.4 Summary

This chapter validates the performance of the proposed grid-side filter structure using the three-phase motor drive system. EMC tests are conducted with the individual DM LCL filter stage, the CM LCL filter stage as well as the full filter stage respectively to evaluate the effectiveness of the methodologies proposed in Chapter 3. The emission characterization results are summarized below.

1. The lowest T-junction inductive coupling M_2 is achieved when the selected CM chokes are placed in a 'vertical' arrangement. The 'vertical' arrangement is observed to reduce the DM emission by 10 dBμV compared to the baseline 'side by side' configuration within 500 kHz – 5 MHz.

2. The inductive coupling is further reduced when a magnetic shield is introduced between the CM chokes arranging in the 'vertical' arrangement. An additional 5 dBμV DM noise reduction within 500 kHz – 5 MHz is observed with the adoption of the magnetic shield.

3. The capacitive coupling C_{coup1} and C_{coup2} is reduced when electric shield is introduced between the boost inductor and the CM LCL filter stage. The electric shield between stages of the filter is observed to reduce the CM emission by 5 dBμV above 3 MHz.

4. The capacitive coupling C_{PCB} is minimized within the redesigned filter board due to the attenuation of the high conducted emission peak around the anti-resonance frequency (f_{res2}) when using the traditional wound boost inductor. A 20 dBμV reduction in both CM and DM noise is observed around f_{res2} with the use of the redesigned filter board.

5. The edgewise wound boost inductor further reduces the DM noise emission due to the lack of anti-resonance of its impedance characteristic. The edgewise wound boost inductor is observed to reduce the DM emission by 5 dBμV compared to the traditional two-layer wound boost inductor around f_{res2}.

6. The strong capacitive coupling between the boost inductor and C_{dm1} masks the effect of paralleling multiple DM capacitors. The paralleling of multiple capacitors is only observed to reduce both CM and DM noise emission by 5-10 dBμV above 10 MHz compared to a single capacitor when the case of the capacitors are electrically shielded.

7. The mutual inductances introduced by the inductive coupling M_1 and M_2 dominate the net ESL on the shunt capacitor branch of the CM LCL filter stage, making the paralleling of multiple film capacitors for C_{dm2} and C_{cm} as well as the adoption of the edge-plating grounding technique ineffective.

Chapter 5 Summary, Conclusion and Future Work

5.1 Summary

Three-phase multi-stage filters are widely adopted in modern power electronics due to their superior attenuation characteristics. However, the self and mutual parasitic effects are known to degrade the filter performance significantly at high frequency. In this work, comprehensive studies have been conducted to study the impact of the parasitic components on the multi-stage filter topology for a 15 kW three phase motor drive system. Time domain simulations using high-frequency passive component models as well as frequency domain simulations using the CM and DM equivalent models are carried out to evaluate the sensitivity of the filter parasitic components to EMI noise emissions. Critical components including the parasitic capacitance within the multi-layered sequential wound boost inductor, the net ESL of the shunt capacitor branch, T-junction inductive coupling in the CM LCL stage, the capacitive coupling between EMI filter stages, and the feedforward coupling effect on the PCB are identified.

Multi-objective redesign process has been carried out to desensitize the identified critical components. A PCB based boost inductor integrated with zig-zag planar winding for low conducted emissions is proposed to minimize the turn-to-turn parasitic capacitances with a feature of high design flexibility and higher resonance frequency. Single layer edgewise wound inductors are found to reduce the winding capacitances as well. Almost 20 dB improvement is observed for the two inductor solutions compared to the traditional boost structure based on EMC tests.

Several solutions were proposed to compensate the parasitic effect on the multi-stage filter. These included optimal component placement, winding strategy, and shielding techniques to

desensitize the influence of near field coupling on the multi-stage filter as well as the optimal film capacitor paralleling and edge-plating technique to minimize the net parasitic inductance on the shunt capacitor branch. Based on the proposed methodologies, an optimal PCB layout with minimized feedforward coupling effect is developed.

Finally, the full-scale filter solution is evaluated in the 15-kW motor drive system. The effectiveness in suppressing both CM and DM noise has been demonstrated through emissions characterization. Consequently, generalized design guidelines have been formulated for different inductor and capacitor form-factors.

5.2 Conclusion

In conclusion, this work determined the crucial parasitic components of the muti-stage filter that have a significant impact on the high frequency emission in a 15-kW motor drive system. Methods to desensitize the influence of these critical self-parasitic components and near field coupling on the muti-stage filter have been proposed. A prototype of the muti-stage filter structure applying the proposed methodologies has been developed and tested for validation using the 15 kW rated 3L-NPC converter in a B2B configuration.

Key observations from the experiments in this work are highlighted. A high conducted emission peak corresponding to the anti-resonance has been observed with the use of multi-layered traditional wound boost inductor. Single-layered edgewise winding and two-layered zigzag winding using planar PCB have been selected and developed for the boost inductor respectively to minimize the high winding capacitance contributing to the anti-resonance.

The T-junction inductive coupling of the CM LCL filter stage has been observed to increase the DM emission within the mid-frequency range due to the mutual inductance introduced on the shunt capacitor branch. The CM chokes have been oriented along the axis that contains the least flux lines, which is determined by the geometry of the selected cores. A magnetic shield has been introduced between the chokes to further absorb the flux leakage in between them.

The capacitive coupling between the stages of the EMI filter has been observed to increase the CM emission from mid to high frequency due to the feed-forward path provided by the parasitic capacitances between the stages. A electric shield has been introduced between the boost inductor and the CM LCL stage to divert the displacement current flowing between the filter stages to ground.

The capacitive coupling between the large PCB ground plane and the power traces has been observed to increase the CM emission at high frequency due to the bypassing of the whole CM LCL filter stage. A smaller PCB ground plane without the overlapping of any power traces has been introduced to achieve minimal capacitive coupling within the PCB.

Based on the key findings, the following design guidelines are formulated to compensate the high conducted emission peaks corresponding to the filter parasitic parameters at high frequency.

1. Large ground plane under power traces should be avoided to prevent the feedforward coupling effect.
2. Pay attention to the relative orientation of the two CM chokes in the CM LCL stage to minimize the inductive coupling effect on the shunt capacitor branch.

3. The single-layered edgewise wound boost inductor could be adopted to minimize the turn-to-turn capacitance, which in turn eliminates the anti-resonance effect.
4. Capacitive couplings between stages of the EMI filter should be minimized to avoid the bypass of filter components.

5.2 Future Work

This work determines the critical parasitic components which have a significant impact on high-frequency emission. A detailed study on the impact of near field coupling between two individual filter components as well as the coupling between the PCB traces are conducted. However, the mutual coupling between the individual filter components and the PCB traces should also be investigated to ensure the insensitivity towards the high-frequency emission.

Moreover, the traditional winding for the three-phase CM choke is adopted in the full-scale filter structure in terms of the manufacturability. It would be interesting to incorporate the split-winding CM chokes into the grid side filter to validate the effectiveness in reducing the magnetic field in between two CM chokes.

Future work could focus on increasing the power density of the filter structure, where the single stage boost inductor could be replaced with three-limb DM inductor for weight and volume reduction. However, it should be noted that the three limb cores can generate mixed mode component due to asymmetric capacitance distribution. Besides, the amorphous based three limb cores exhibits a higher core loss compared to the single-phase powder cores. Therefore, a comprehensive study on the three-limb DM inductor should be conducted before implementation.

Appendix A. Parasitic Capacitance Extraction Procedure for a 3L-NPC converter modules

The proposed double pulse test circuit to estimate the parasitic capacitance in a 3L-NPC module is shown in Fig. A.1. An additional large inductor (L_{add}) and capacitor (C_{add}) are introduced between the output and load of the traditional DPT circuit [63] for the 3L-NPC converter. The large inductor is introduced to mask the impact of the module stray inductance and the large capacitor to ground is added to shunt and circulate the high frequency CM current (i_{cm}). C_{P1}-C_{P6} are the major CM parasitic capacitances to be extracted from the phase leg module to ground/heatsink.

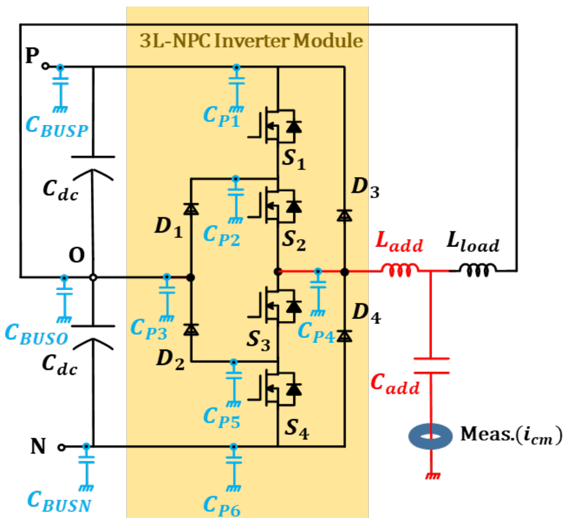


Fig. A.1.Proposed extended DPT (eDPT) circuit

Since the ringing frequency of the CM current is mainly determined by the passive oscillation of the equivalent circuit when any device is switching, multivariate equations can be derived to present the ringing frequencies under different switching states [64]. Fig. A.2 shows the equivalent passive circuits under different switching states where one of the MOSFETs (S_1-S_4) is turning on.

In the equivalent ringing circuits, DC link capacitors (C_{dc}) are considered short due to its low ac impedance compared to the module parasitic capacitance. The MOSFET is considered short when the device is on and replaced with the output capacitance (C_{oss}) when the device is off. The neutral clamped diode (D_1, D_2) is considered short when it is forward-biased and replaced with the junction capacitance (C_j) when it is reverse-biased. The ringing frequency for the four switching states are derived as (1)-(3).

$$f_1 = f_4 = 1 \Bigg/ \left(2\pi \sqrt{L_{add} \frac{C_{add}(C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{P5} + C_{P6} + \sum C_{BUS})}{C_{add} + (C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{P5} + C_{P6} + \sum C_{BUS})}} \right) \quad (1)$$

$$\begin{cases} f_2 = 1 \Bigg/ \left(2\pi \sqrt{L_{add} \frac{C_{add}(C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{\Delta 1} + C_{\Delta 2} + C_{P6} + \sum C_{BUS})}{C_{add} + (C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{\Delta 1} + C_{\Delta 2} + C_{P6} + \sum C_{BUS})}} \right) \\ \quad where\ C_{\Delta 1} = \frac{(C_{oss} + C_j)C_{P5}}{2C_{oss} + C_j + C_{P5}}, C_{\Delta 2} = \frac{C_{oss}C_{P5}}{2C_{oss} + C_j + C_{P5}} \end{cases} \quad (2)$$

$$\begin{cases} f_3 = 1 \Bigg/ \left(2\pi \sqrt{L_{add} \frac{C_{add}(C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{\Delta 3} + C_{\Delta 4} + C_{P6} + \sum C_{BUS})}{C_{add} + (C_{P1} + C_{P2} + C_{P3} + C_{P4} + C_{\Delta 3} + C_{\Delta 4} + C_{P6} + \sum C_{BUS})}} \right) \\ \quad where\ C_{\Delta 3} = \frac{(C_{oss} + C_j)C_{P2}}{2C_{oss} + C_j + C_{P2}}, C_{\Delta 4} = \frac{C_{oss}C_{P2}}{2C_{oss} + C_j + C_{P2}} \end{cases} \quad (3)$$

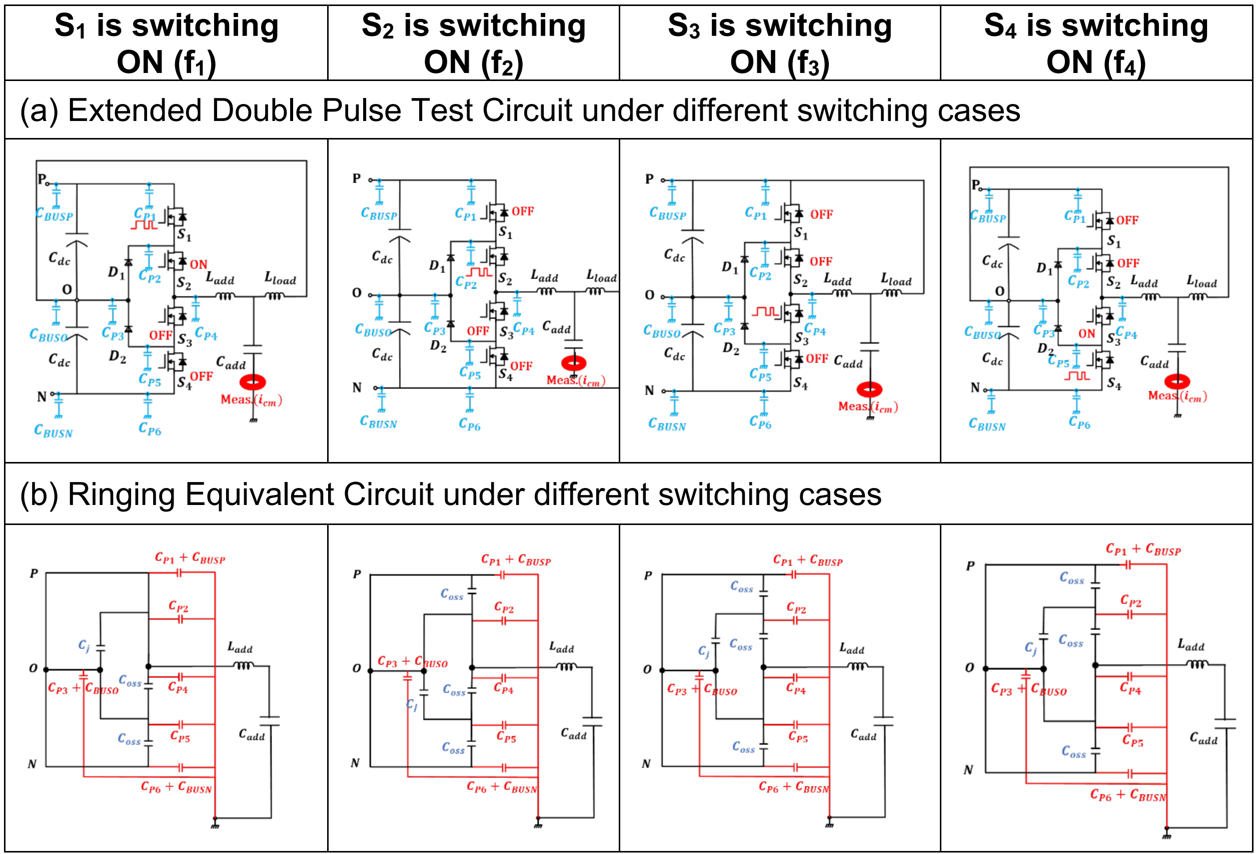


Fig. A.2.Extended DPT Circuit under different switching cases.

To further reduce the variables in (1)-(3), same die area per device is considered in the phase leg module. In this assumption, C_{pm} is the drain to ground/heatsink parasitic capacitance of the MOSFET, C_{pd1} and C_{pd2} are anode to ground/heatsink parasitic capacitance of the neutral clamped diode (D_1, D_2) and the additional diode (D_3, D_4 in Fig. 1) respectively. The emitter and anode to ground/heatsink parasitic capacitances are neglected. Substituting C_{P1}-C_{P6} with C_{pm}, C_{pd1} and C_{pd2} as shown in Table I, equation (1)-(3) can be transformed to (4)-(6).

TABLE I. Simplified expression for C_{P1}-C_{P6}

Parameter	*Simplified Expression*
C_{P1}	$C_{pm}+C_{pd2}$
C_{P2}	$C_{pm}+C_{pd1}$
C_{P3}	C_{pd1}
C_{P4}	$C_{pm}+C_{pd2}$
C_{P5}	C_{pm}
C_{P6}	*neglected*

$$f_1 = f_4 = 1\Bigg/\left(2\pi\sqrt{L_{add}\frac{C_{add}(4C_{pm} + 2C_{pd1} + 2C_{pd2} + \sum C_{BUS})}{C_{add} + (4C_{pm} + 2C_{pd1} + 2C_{pd2} + \sum C_{BUS})}}\right) \tag{4}$$

$$\begin{cases} f_2 = 1\Bigg/\left(2\pi\sqrt{L_{add}\frac{C_{add}(3C_{pm} + 2C_{pd1} + 2C_{pd2} + C'_{\Delta 1} + C'_{\Delta 2} + \sum C_{BUS})}{C_{add} + (3C_{pm} + 2C_{pd1} + 2C_{pd2} + C'_{\Delta 1} + C'_{\Delta 2} + \sum C_{BUS})}}\right) \\ \quad where\ C'_{\Delta 1} = \frac{(C_{oss} + C_j)C_{pm}}{2C_{oss} + C_j + C_{pm}}, C_{\Delta 2} = \frac{C_{oss}C_{pm}}{2C_{oss} + C_j + C_{pm}} \end{cases} \tag{5}$$

$$\begin{cases} f_3 = 1\Bigg/\left(2\pi\sqrt{L_{add}\frac{C_{add}(3C_{pm} + 1C_{pd1} + 2C_{pd2} + C'_{\Delta 3} + C'_{\Delta 4} + \sum C_{BUS})}{C_{add} + (3C_{pm} + 1C_{pd1} + 2C_{pd2} + C'_{\Delta 3} + C'_{\Delta 4} + \sum C_{BUS})}}\right) \\ C'_{\Delta 3} = \frac{(C_{oss} + C_j)(C_{pm} + C_{pd1})}{2C_{oss} + C_j + C_{pm} + C_{pd1}}, C'_{\Delta 4} = \frac{C_{oss}(C_{pm} + C_{pd1})}{2C_{oss} + C_j + C_{pm} + C_{pd1}} \end{cases} \tag{6}$$

In order to simplify and solve the equations (4)-(6) for C_{pm}, C_{pd1} and C_{pd2}, the capacitance of C_{add} is considered much larger than the sum of the module stray capacitances and the busbar capacitances, the value of ($2C_{oss}$+C_j) is assumed to be much larger than the module stray capacitance. From these assumptions, the parasitic capacitances can be calculated as (7).

$$\begin{cases} C_{pm} = \left(1\Bigg/\sqrt{\frac{1}{4\pi^2}\left(\frac{1}{f_1{}^2} - \frac{1}{f_2{}^2}\right)(2C_{oss} + C_j)/L_{add}}\right) \\ C_{pd1} = \left(1\Bigg/\sqrt{\frac{1}{4\pi^2}\left(\frac{1}{f_1{}^2} - \frac{1}{f_3{}^2}\right)(2C_{oss} + C_j)/L_{add}}\right) - C_{pm} \\ C_{pd2} = \frac{1}{2}\left(\left(\frac{1}{4\pi^2 f_1{}^2 L_{add}}\right) - 4C_{pm} - 2C_{pd1} - \sum C_{BUS}\right) \end{cases} \tag{7}$$

Equation set (7) is sufficient to determine C_{P1}-C_{P6} if the sum of the busbar parasitic capacitances is already known from FEA model extraction or direct measurement. However, if the $\sum C_{BUS}$ is unknown, this method can also estimate the value by considering additional testing configuration as shown in Fig. A.3. The output point of the converter is connected in between the

upper two switches and the lower two switches when performing DPT to S_1 and S_4 respectively. S_2 and S_3 is always OFF in this testing configuration and the 3L-NPC inverter acts like a 2L inverter. The additional equation derived from this configuration can be obtained as (8). Combining equations (4)-(6) and (8), $\sum C_{BUS}$, C_{pm}, C_{pd1}, and C_{pd2} and can be calculated as (9).

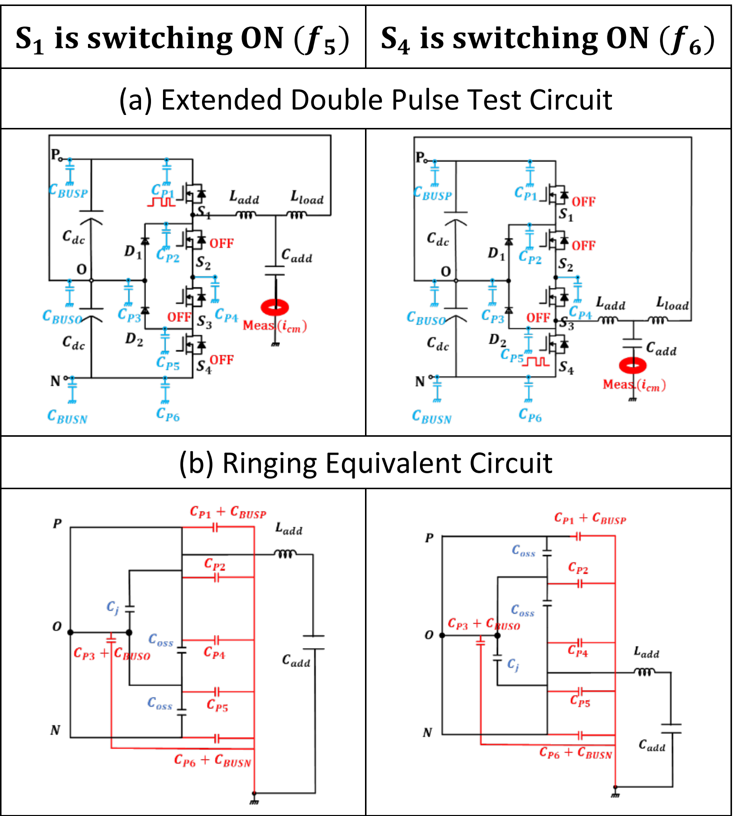


Fig. A.3.Additional eDPT configurations for parasitic extraction

$$\begin{cases} f_5 = f_6 = 1\Big/\left(2\pi\sqrt{L_{add}\dfrac{C_{add}(3C_{pm}+2C_{pd1}+1C_{pd2}+C'_{\Delta5}+C'_{\Delta6}+\sum C_{BUS})}{C_{add}+(3C_{pm}+2C_{pd1}+1C_{pd2}+C'_{\Delta5}+C'_{\Delta6}+\sum C_{BUS})}}\right) \\ \qquad where\ C'_{\Delta5} = C'_{\Delta6} = \dfrac{C_{oss}(C_{pm}+C_{pd2})}{2C_{oss}+C_{pm}+C_{pd2}} \end{cases} \tag{8}$$

$$\begin{cases} C_{pm} = \left(1\Big/\sqrt{\dfrac{1}{4\pi^2}\left(\dfrac{1}{f_1{}^2}-\dfrac{1}{f_2{}^2}\right)(2C_{oss}+C_j)/L_{add}}\right) \\ C_{pd1} = \left(1\Big/\sqrt{\dfrac{1}{4\pi^2}\left(\dfrac{1}{f_1{}^2}-\dfrac{1}{f_3{}^2}\right)(2C_{oss}+C_j)/L_{add}}\right) - C_{pm} \\ C_{pd2} = \left(1\Big/\sqrt{\dfrac{1}{4\pi^2}\left(\dfrac{1}{f_1{}^2}-\dfrac{1}{f_5{}^2}\right)(2C_{oss})/L_{add}}\right) - C_{pm} \\ \sum C_{BUS} = \left(\dfrac{1}{4\pi^2 f_1{}^2 L_{add}}\right) - \left(2\Big/\sqrt{\dfrac{1}{4\pi^2}\left(\dfrac{1}{f_1{}^2}-\dfrac{1}{f_5{}^2}\right)(2C_{oss})/L_{add}}\right) - 2C_{pm} - 2C_{pd1} \end{cases} \tag{9}$$

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