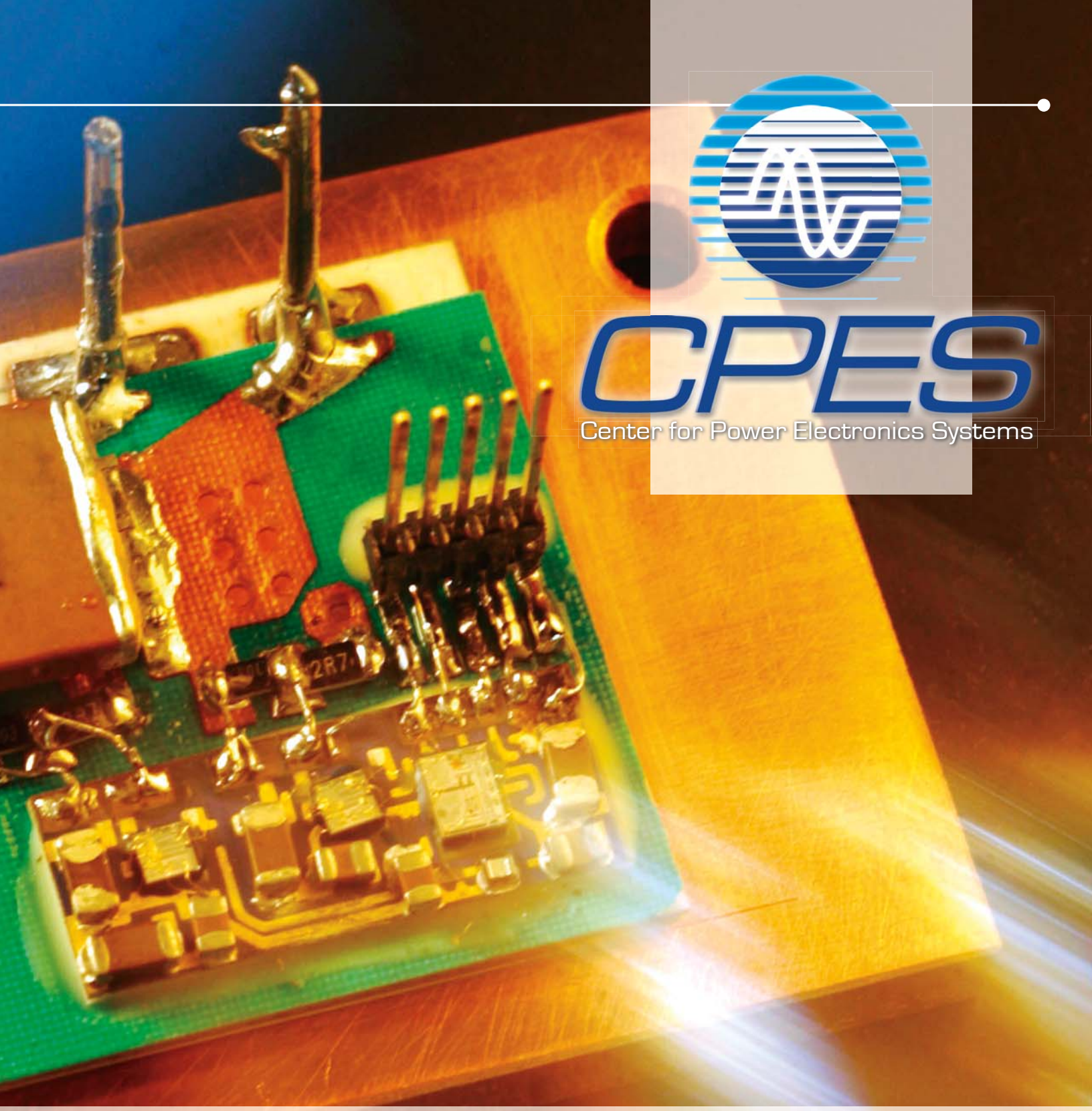

CPES

Center for Power Electronics Systems

APRIL 2009

CENTER PROGRAM SNAPSHOT

FRED C. LEE DIRECTOR DUSHAN BOROYEVICH CO-DIRECTOR

Cover: An early IPEM for high-efficiency distributed power systems from the Convergence Generation. This IPEM was used to evaluate advances in semiconductor devices and high-density integration.
Photo by Michael Kiernan

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CHAPTER 1
A SYSTEMS VISION

Electricity is used at an average rate of 40 billion kilowatt-hours worldwide every day of every year. With few exceptions, the electricity is not used its raw form. Instead, the machines, motors and electronics equipment convert electricity into the specific form they need. The conversion of electrical power from one form to another increasingly uses the technology – and the engineering discipline – of power electronics.

An enabling infrastructure technology

Power electronics and related power-processing techniques constitute an "enabling infrastructure technology." Worldwide sales of power electronics equipment top $60 billion each year and support another $2 trillion in hardware/software electronics. Advances in power electronics technology can reduce losses in power conversion and more precisely control electrical power for manufacturing operations. These, in turn, can increase energy efficiency of equipment and processes using electrical power, raise industrial productivity and improve product quality. Such advances could have a huge impact on U.S. industrial competitiveness.

Environmental benefits

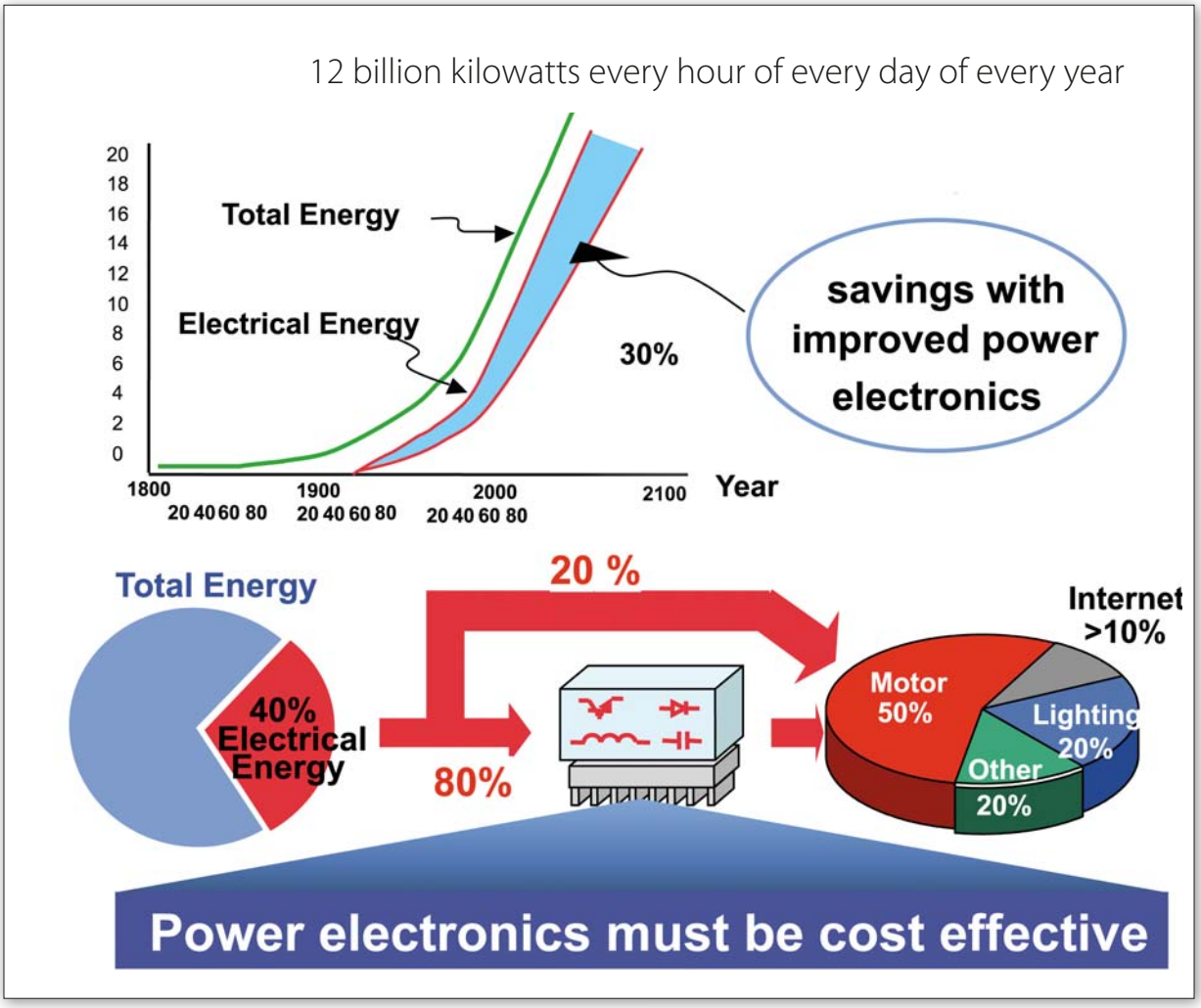
Power electronics can also yield environmental benefits. For example, the 2003 EPRI Electricity Technology Roadmap identified high-efficiency end-uses of electricity as one of the key challenges to achieving its vision of an extremely reliable power delivery system that increases economic growth rates with minimal environmental impact. High-efficiency lighting systems, motor drives and power supplies were listed among the highest priority capability gaps. The efficiency of all of those applications can be greatly improved with advanced power electronics.

Reducing energy consumption

With the widespread use of power electronics technology, the United States would be able to cut electrical energy consumption by 33 percent. The energy savings, by today's measure, is equivalent to the total output of 840 fossil fuel-based generating plants. This would result in enormous economic, environmental and social benefits.

The engineers of the Center for Power Electronics Systems (CPES) are working to make electric power processing more efficient and more exact in order to achieve these benefits. The effort requires close collaboration with industry and with researchers across universities and fields of endeavor. Electrification is considered the greatest engineering feat of the 20th century by the National Academy of Engineering. The dream of CPES engineers is to take electricity to the next step and develop power processing systems of the highest value to society.

12 billion kilowatts every hour of every day of every year



Creating CPES

State of the industry – 1998

In 1998, U.S. power electronics systems were typically custom-designed, non-standard units containing 300-400 electronic components, with little integration and fairly low reliability. Long design cycles and labor-intensive manufacturing processes created excessive costs and a weakened U.S. power electronics industry. In the 1980s, power electronics had been considered a core enabling technology for major corporations in the U.S. However, in the 1990s, the major corporations adopted outsourcing strategies and spun off their power electronics divisions. What had been a captive market was transformed into a merchant market, with fewer resources devoted to technical advancement in the technology. Consequently, innovative solutions grew scarce. Power electronics products became commoditized and cost-driven and manufacturing migrated to countries with low labor costs. U.S. industry had become bottom-line focused and spent little on development —even less on research.

Research challenges

Meanwhile, university research efforts advanced component and process technology for power electronics, but did not yield the overall improvement needed for the next generation of motors and electronics. Funding for research in the field was very competitive and research groups had little incentive to collaborate, especially across universities and fields. With fragmented academic research efforts and decreasing industrial innovation, power electronics needed a new research paradigm if the technology was going to deliver its promised efficiencies. It was a challenging engineering problem, both operationally and technologically.

ERC mission

In 1998, the National Science Foundation (NSF) established the Center for Power Electronics Systems as an Engineering Research Center (ERC) to develop advanced electronic power conversion technologies for efficient electric energy utilization through multidisciplinary engineering research and education.

The initial research vision was based on the concept of developing standardized, modularized integrated power electronics modules (IPEM) "to enable dramatic improvements in the performance, reliability and cost-effectiveness of electric energy processing systems."

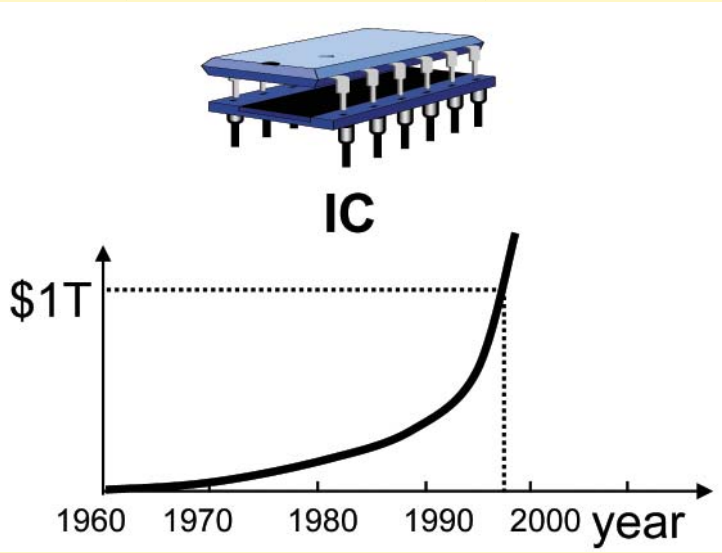
IPEM Vision

The envisioned integrated power electronics solution is based on advanced packaging of a new generation of devices and innovative circuits and functions in the form of building blocks with integrated functionality, standardized interfaces, suitability for automated manufacturing and mass production, and application versatility, namely IPEMs, and the integration of these building blocks into application-specific systems solutions. The impact of this paradigm shift can be compared to the impact realized via the improvements in very-large-scale integrated (VLSI) circuit technology that has enabled significant advancement in computer and telecommunications equipment.

SIGNAL PROCESSING - IC

Moore's Law Prevails

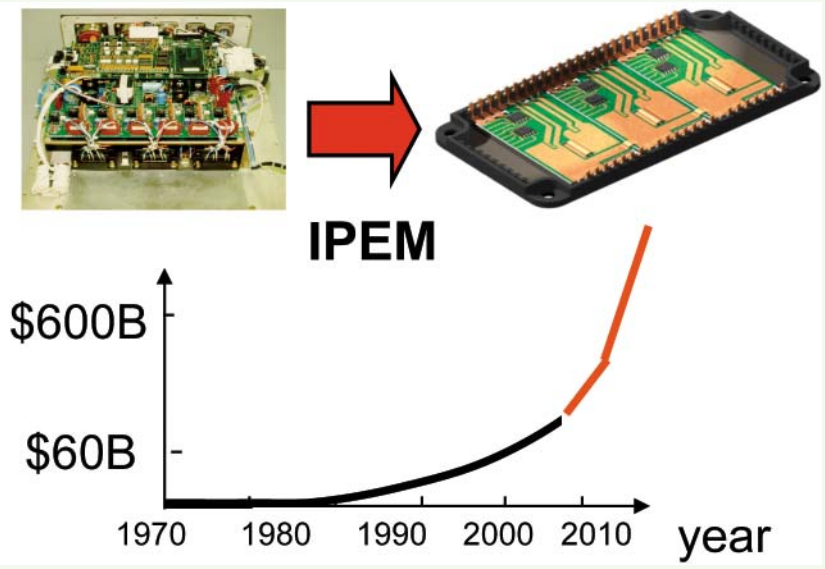
through
- Standardization
- Manufacturability
- Volume production
- Cost reduction



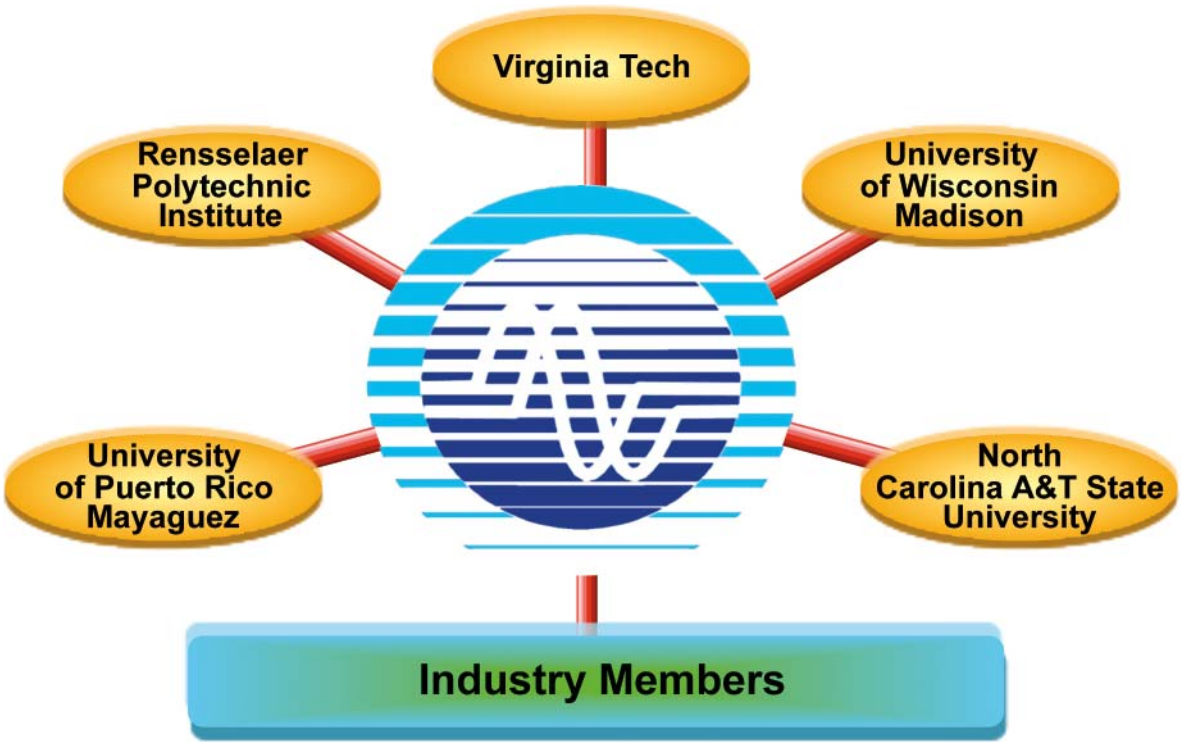
POWER PROCESSING - IPEM

IPEM Expected Impact

through
- Building blocks
- Reduced labor
- Low cost



Building The Team



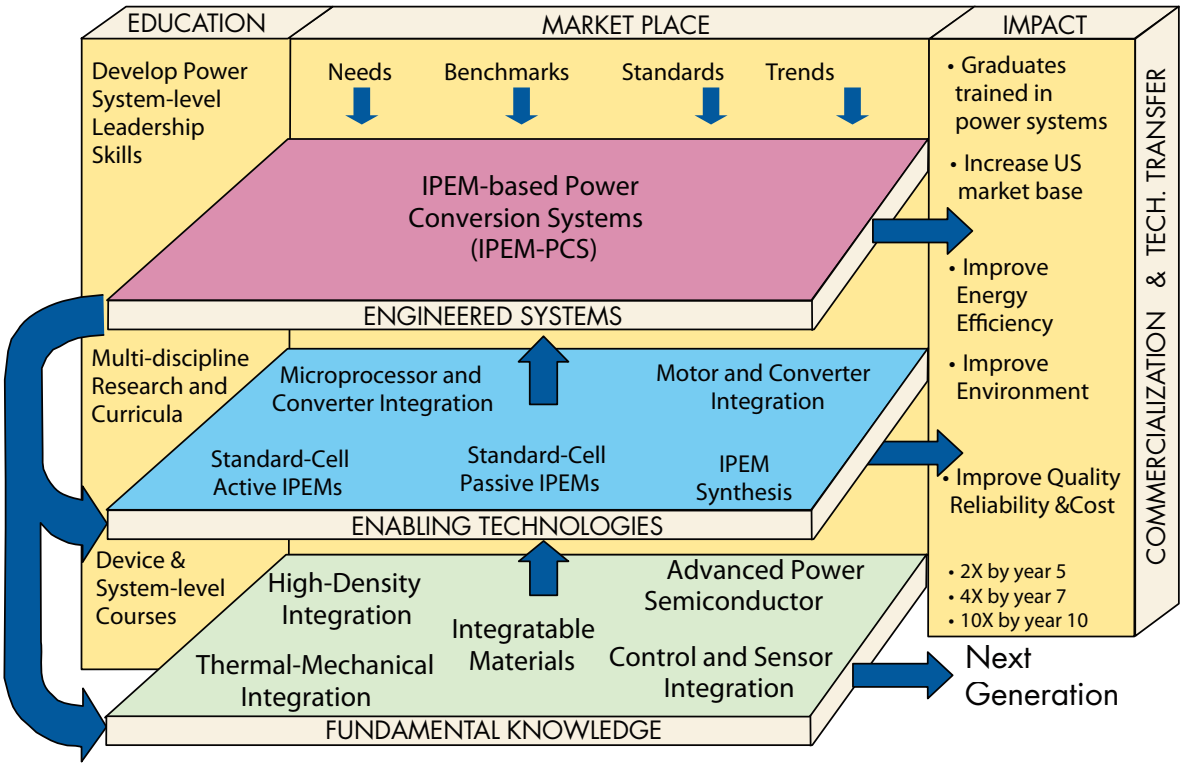
The research goal could not be accomplished by any single group and CPES was established as a consortium of five universities, with more than 80 industry members. Industrial collaboration and technology transfer were critical goals, as the power electronics solutions would need to be integrated quickly into commercial products. Because of the lack of experts in U.S. firms, CPES also was tasked with developing enough trained engineers and scientists to carry the technology forward.

Since 1998, CPES research goals have evolved and the collaborations with industry and university researchers have strengthened. CPES succeeded in changing the technology of power electronics, while increasing knowledge and participation in the field. As we graduate from the NSF ERC program, we look forward to building on our global collaboration and changing the way electricity is used.

CHAPTER 2

CENTER PROGRAM OVERVIEW

With a multi-university team such as CPES, a well defined and comprehensive strategic plan and roadmap are essential to realize the Center's vision and goals. Although the CPES research programs and organizations have always been based on the Center's IPEM-focused research vision, they have been continually evolving since the inception of the Center in response to advances in CPES research and the SWOT (Strengths, Weaknesses, Opportunities, Threats) analyses by NSF, industry, and students.



FOUR GENERATIONS OF CPES RESEARCH

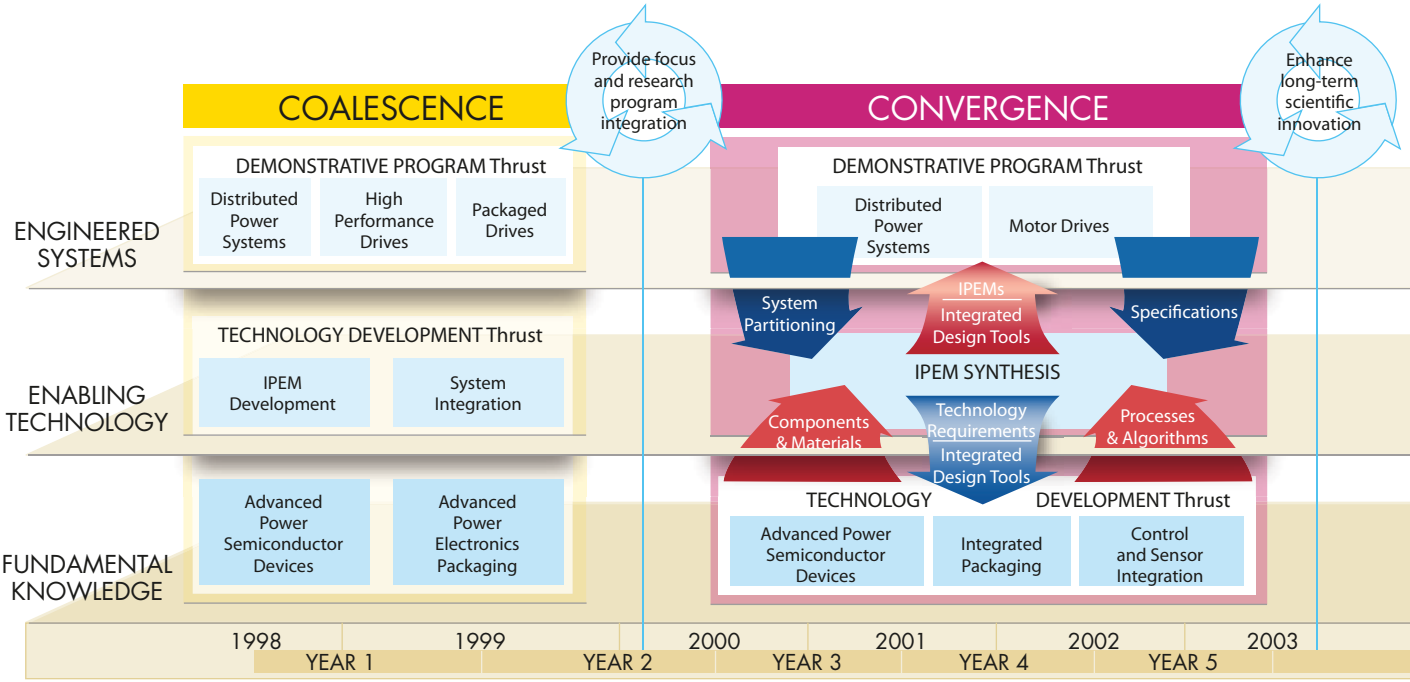
Evolution of the research strategic program

CPES was built to improve the efficiency of electricity use through developments in power electronics, improved technology transfer, and strengthened education in the field. We aimed to increase the efficiency of electrical processes by standardizing, modularizing, and integrating power electronics technology. We sought to simplify a complicated process, but our challenges were not simple. Before we could achieve modular integration through IPEMs, we first had to break the problem into discrete parts and tackle problems on multiple levels simultaneously.

We tapped the expertise from five different universities. As we developed answers and as our teams gained experience working across former boundaries of institutions and disciplines, we restructured the problem and our attack to meet the new challenges. In the past 10 years, CPES has evolved through four major configurations and phases: the early coalescence phase, in which we gathered and defined our challenges; the convergence phase, in which our solutions fed into each other and we made great strides in IPEM development; the expanded creativity phase, in which we identified and investigated more discrete tasks; and the graduation phase, in which we restructured for a renewed effort outside of the ERC program.

A 3-plane structure

CPES research can be viewed easily through the NSF three-plane strategy, as shown in the diagram below. The fundamental knowledge plane encompasses basic scientific research and engineering theory and



practices. Enabling technology incudes the engineering developments that are critical for new technology; and the engineered systems are the systems, applications, and testbeds developed to test and demonstrate advances in enabling technology and fundamental knowledge. The separate planes, although distinct, cannot exist without advances and direction from each other.

In the diagram below, the evolution of CPES research efforts are mapped across each of the strategy planes for the 10 years of the ERC.

Enabling technology

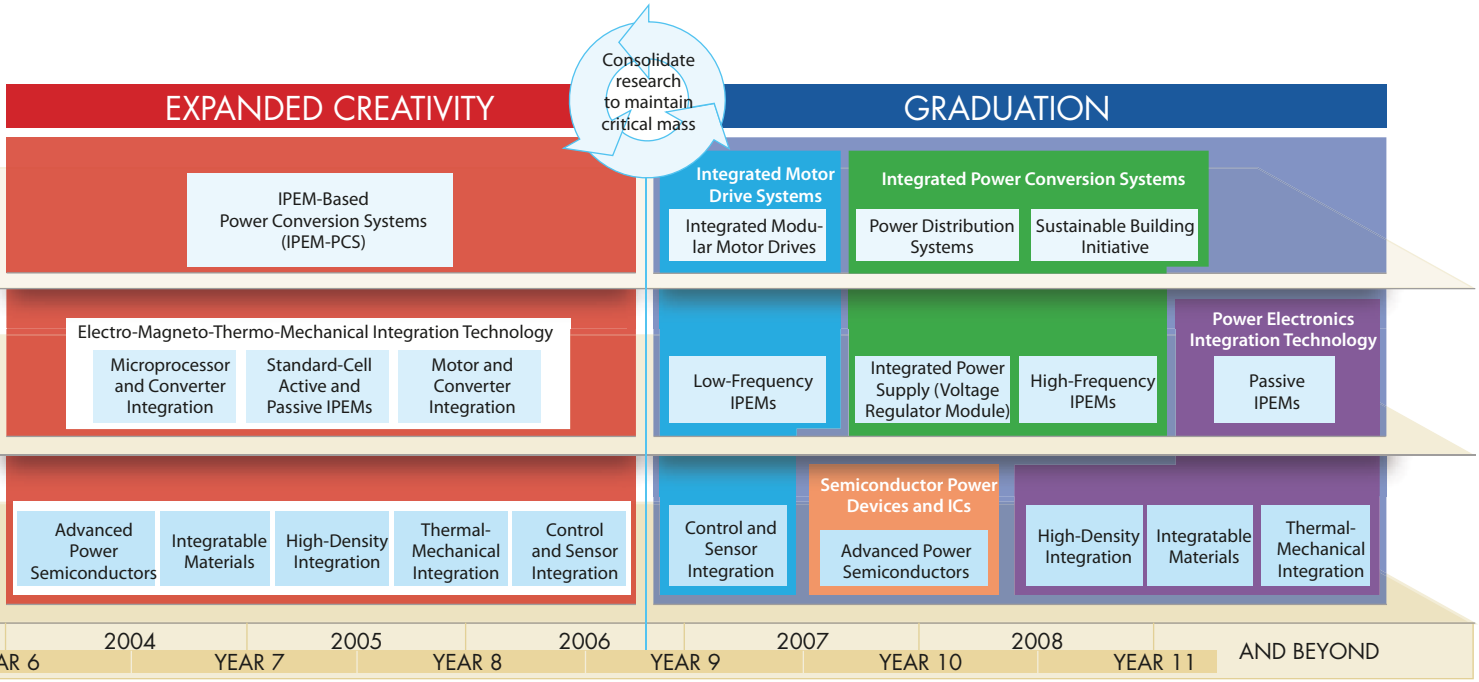
CPES was founded to advance an enabling technology: the IPEM and integrated power electronics systems. Initially, enabling technology efforts were focused on the development of the IPEM and the integration technology needed for IPEM-based systems. As the IPEMs were developed and commercialized, the focus on this plane evolved to synthesis, then integration technology. More recently, the focus has shifted to advancing specific IPEM technology – including low-frequency, high frequency, and passive IPEMs, as well as integrated power supplies.

Fundamental knowledge

The enabling technology of IPEMs could not have moved forward without significant advances in fundamental knowledge. Early on, the supporting fundamental knowledge included semiconductor devices and packaging. As the technology progressed, questions in control and sensor integration were addressed. Once the initial IPEMs were demonstrated, the fundamental knowledge research branched into a number of efforts, with the addition of materials and thermal/mechanical integration issues. These were the fundamental knowledge directions as we moved toward graduation.

Engineered Systems

Throughout the 10 years of the ERC the CPES testbeds and applications remained concentrated in applications in distributed power systems and motor drives: the two areas of expertise at Virginia Tech and the University of Wisconsin. Once the IPEMs were demonstrated, engineered systems research concentrated on power conversion systems. Post-ERC efforts continue with those two areas of expertise, but also expand to include sustainable building technology and high-power applications.



4 generations of research

In the diagram on the previous pages, the four generations of CPES research are depicted as the vertical colored blocks, with each generation lasting two-three years. The different generations provide another dimension to the CPES research story.

Coalescence

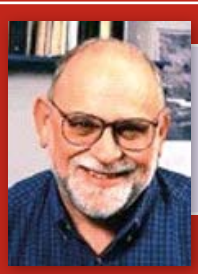
Originally, the Center's research program was structured with seven subthrusts and grouped into two thrust areas. One was technology development and the other was demonstrative programs. Within the technology development, there were four subthrusts: advanced power semiconductor devices; advanced power electronics packaging; system integration; and integrated power electronic module (IPEM) development. Within the demonstrative program, we had three testbed areas: distributed power systems; packaged drives; and high-performance drives.

The first two years of CPES were highlighted by the major effort involved in forming strong teams across universities and disciplines. During this Coalescence Phase, we identified major technology and application barriers and established the state-of-the-art benchmarks. However, by the end of this initial period, our industry members became concerned that the research program was too spread-out and without sufficient focus, while the NSF was worried about lack of

RESEARCH ORGANIZATION

CENTER DIRECTOR
F.C. Lee, VT

IPEM-based power conversion systems
D. Boroyevich, VT



T.A. Lipo, UWM

T.M. Jahns, UWM

Electro-magento-thermo-mechanical integration technology

Microprocessor and converter integration | Standard-cell active IPEMs | Standard-cell passive IPEMs | Motor and converter integration | IPEM synthesis

Advanced power semiconductors
T.P. Chow, RPI

Integratable materials
G.Q. Lu, VT

PEIT Thrust
K. Ngo, VT

High-density integration
J.D. van Wyk, VT

Thermal-mechanical integration
E.P. Scott, VT

Control and Sensor integration
R.D. Lorenz, UWM

"CPES has world class research activities in drives and converters and other research programs that build on those strengths."

—2004 NSF Site Visit Report

integration between the research teams. Consequently, the research program was strategically reorganized to facilitate the convergence of the ideas and activities.

Convergence

The modified research structure for the next four years was organized according to the NSF three-plane strategy. In the engineered systems plane, we reduced the number of testbeds to two, distributed power systems, and motor drives, in order to better tap existing strengths. In the enabling technology plane, we developed an IPEM synthesis thrust, and expanded the fundamental knowledge efforts.

We increased emphasis on IPEM synthesis as the core technology, to provide clear focus between the system-level pull and fundamental technology push. This was pursued by developing an integrated design methodology along with CAD tools that could be used both at the system- and component-level, and by designing, implementing and evaluating experimental IPEMs for the application testbeds. The resulting convergence of research produced numerous technological advances and initiated a paradigm shift in the research and design of power electronics systems.

Expanded creativity

In 2004, in order to address the issue of lack of balance between basic research and applied research as raised by NSF site visit team, CPES research programs were restructured with a much-expanded IPEM vision and a significant increase of the basic research content in all research thrusts.

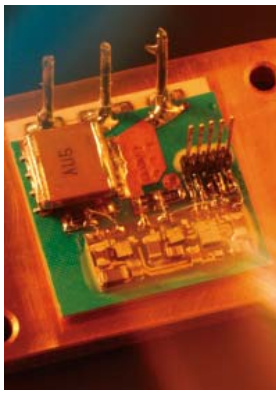
In enabling technology, a new thrust, electro-magneto-thermo-mechanical integration, was established to replace the IPEM synthesis thrust. There were three focused areas within this thrust: standard-cell IPEM technologies for high-frequency applications (based on our distributed power systems testbed) and low-frequency applications (based on our motor drives testbed); integrated power supplies; and integrated modular motor drives. In the engineered systems plane, we consolidated our testbed programs to form one IPEM-based power conversion systems thrust.

The reorganization did enable numerous new contributions in all areas of CPES research, although their connectivity and aggregate impact on the power electronics systems grew more obscure.

Preparation for graduation

During the last two years, the research strategy was reorganized again in preparation for graduation from NSF ERC funding. The plan was a result of numerous meetings and discussions of the whole CPES leadership team, the Industry Advisory Board, and the outreach to the global power electronics community. We concluded that CPES must maintain the core competence essential for our multidisciplinary research, and at the same time open up to enable future energy-related system applications. This resulted in consolidation of the research into four core thrusts: integrated power conversion systems, integrated motor drive systems, power electronics integration technology, and semiconductor power devices and ICs, and simultaneous expansion of the research sponsored by industry and other government agencies. At the same time, a broad-based research was initiated in the area of power electronics impact on the future sustainable buildings.

Although CPES IPEM technology is commercialized in many applications, we still face challenges with the concept. However, in order to make the greatest impact on future energy efficiency, we are moving toward tackling energy processing at a larger, systems level.



A Convergence Generation IPEM for high-efficiency distributed power systems, used to evaluate advances in semiconductor devices and high-density integration.

ENGINEERED SYSTEMS

OVERVIEW
Engineered Systems

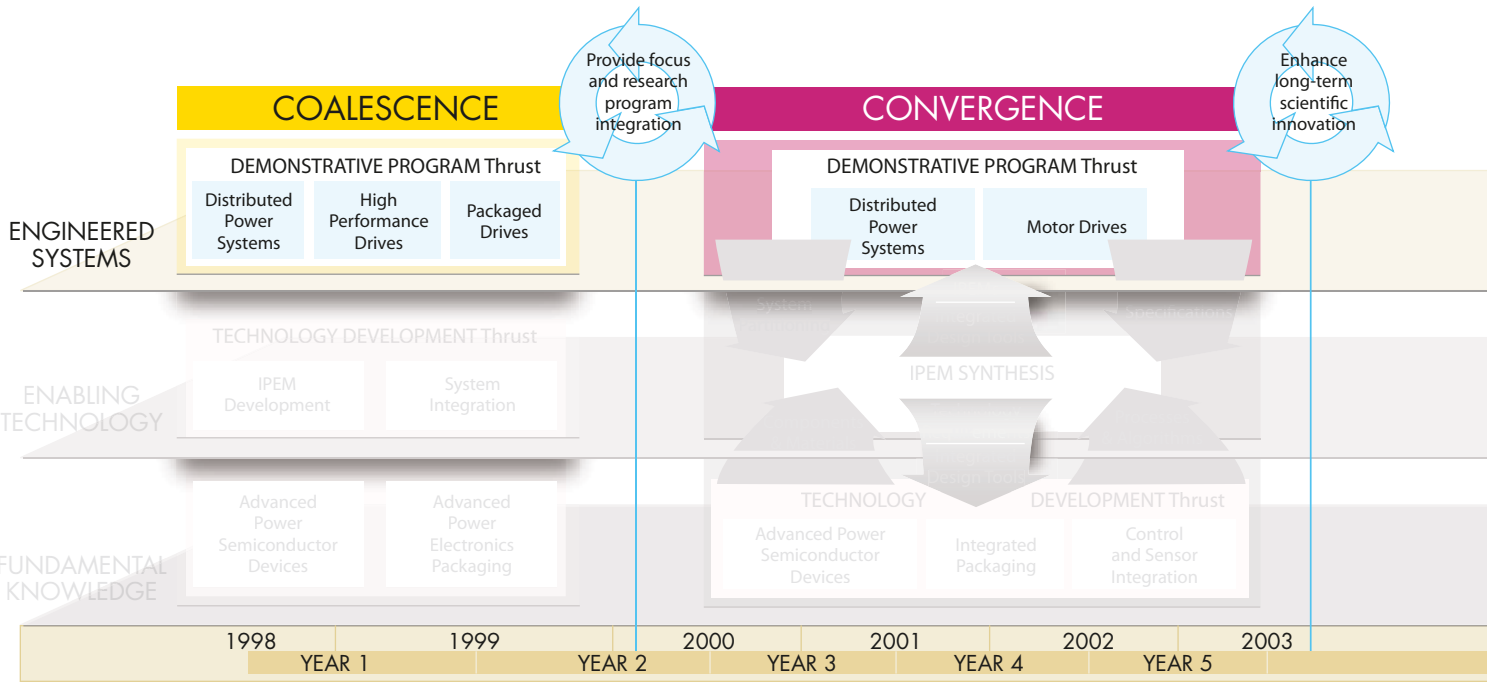
CPES has targeted systems and applications that would conserve the most energy based on the state of power electronics technology at the time. Moving the technology quickly into industrial use has been a driving force behind the Center, with the hope that the country could begin to realize energy savings almost from the start.

CPES was built around two peaks of excellence: Virginia Tech in power supplies and the University of Wisconsin in motor drives. These two technologies have played major roles throughout CPES history.

Evolution of engineered systems

In 1998, when IPEMs were just a concept, demonstrative programs were one of two major thrusts at CPES, with subthrusts in distributed power systems, high-performance drives and low-cost packaged drives. Applications and testbeds — chosen for their market potential and predicted energy savings — ranged from telecommunications to heating, ventilation and air conditioning (HVAC) to hybrid electric vehicles.

In 2000, CPES consolidated the high performance drives and packaged drive into one motor drive effort to encourage greater collaboration and integration. The two applications, distributed power systems and motor drives, reflected CPES strengths and expertise. As IPEM technology developed and the concept of system integration was formulated, it became apparent that the fundamental integration technologies for power supplies and motor drives are the same. What



set them apart was the specific requirement for IPEMs in each application. We again restructured our engineered systems efforts, blending the two applications into a general IPEM-based power conversion systems thrust.

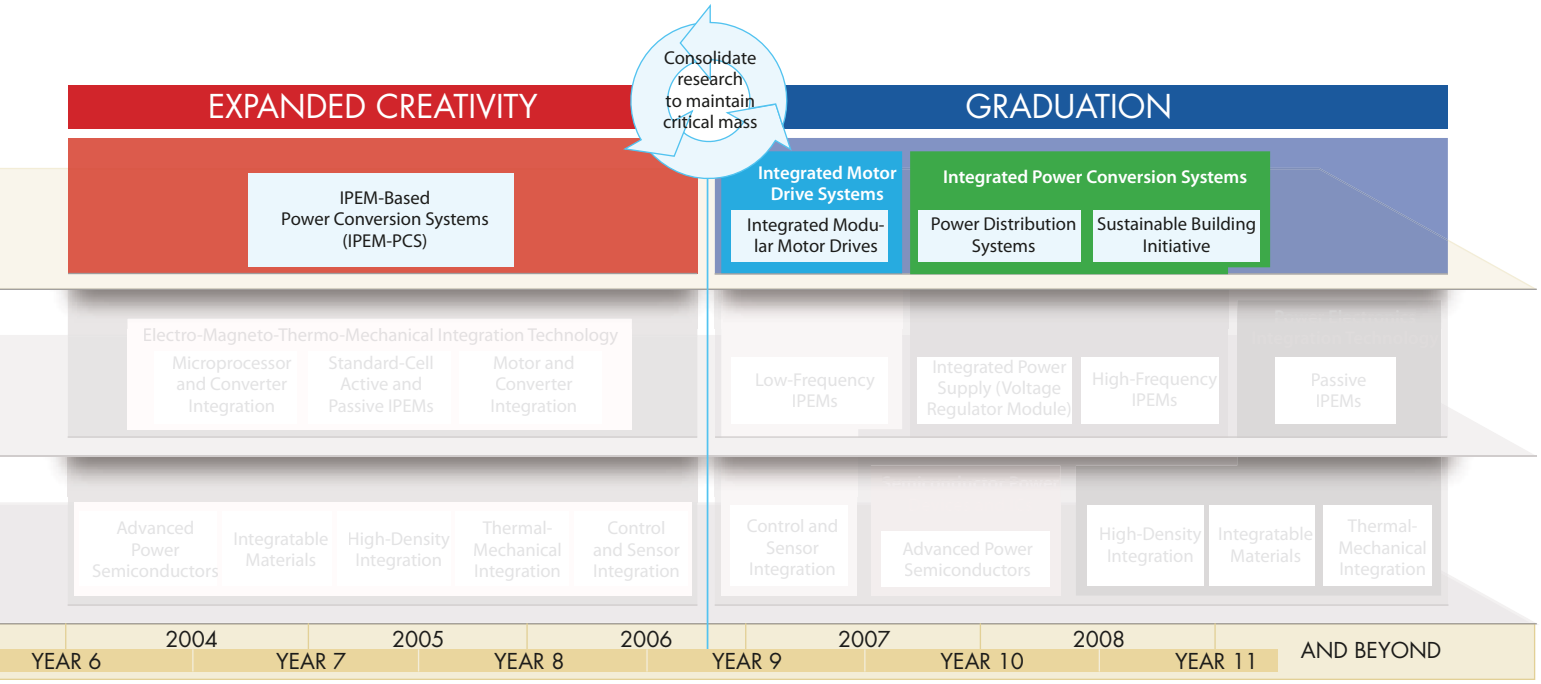
This restructuring triggered the expanded creativity phase of CPES efforts as researchers investigated many innovations of IPEMs based on different applications. As we moved toward graduation from the NSF ERC program, the ongoing engineered systems efforts in IPEM-based power conversion systems expanded beyond traditional low power high-volume power supplies and motor drives to lower power electronics for portable battery operated systems and higher power distributed power generation and processing systems.

Three major systems themes

Three major themes have been woven throughout our engineered systems work during our 10 years as an NSF ERC. The higher power, higher voltage power supply applications and the autonomous power/motor drive applications derive from our two peaks of excellence. In parallel with those efforts, research in the lowest power, microprocessor power supplies has been a significant effort. Most recently, we have added another initiative that integrates all the themes: power electronics for sustainable buildings.

Sustainable building initiative

The newest systems initiative targets saving energy in the home and other buildings. All CPES campuses are developing integrated power electronics technology for future buildings. Investigations include a high voltage (380V) dc-power distribution system and testbeds using renewable energy sources; a higher-frequency (higher than 60Hz) ac power distribution system, and power supply and management systems for portable appliances that can use multiple sources of energy.



Integrated Motor Drive Systems

Electric motors consume more than 50 percent of all electricity, much of which could be saved if motor drives are more widely adopted. Cost and reliability are primary hurdles to the integration of motor drives into applications from white goods to automobiles to aircraft — making these drives natural targets for CPES technology.

When CPES was founded in 1998, motor drive research was split into two demonstrative programs; high performance drives and packaged drives. The high performance drive thrust focused on applications such as spindle drives using new sensor and estimation techniques. Research in packaged drives focused on fractional-horsepower motor drives intended for home appliance heating, ventilation, and air conditioning (HVAC) applications.

The aim was to simplify the power converter topologies to reduce the number of active switches, thus reducing power electronics costs. Our ultimate goal was to develop integrated motor drive configurations that combined the motor and power electronics into a single physical structure.

Coalescence phase

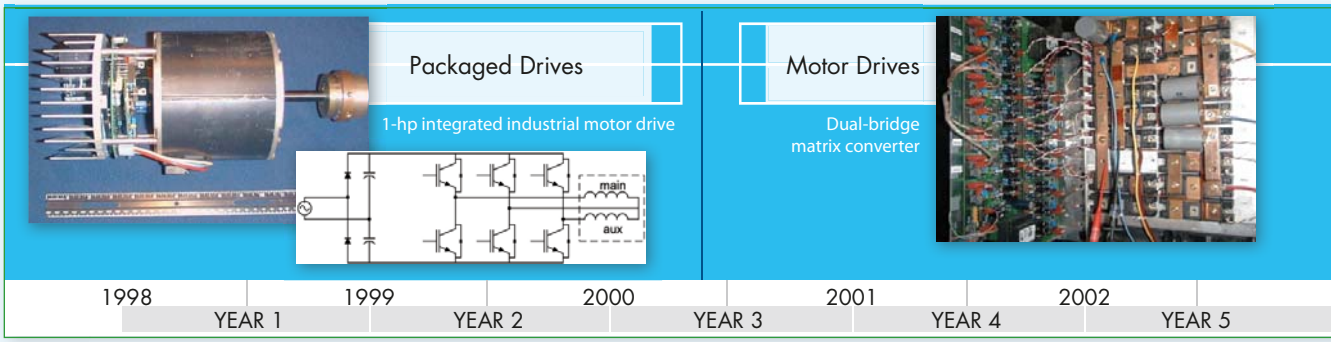
In Year 3, the two demonstrative projects were merged into a single motor drives thrust focusing on low-horsepower motor drives (1-3 hp) for HVAC applications. The goal was to reduce motor drive cost and size and to improve reliability by eliminating the electrolytic capacitors typically required for the dc link.

Automotive power electronics

In Year 3, we also launched a special "Low-Cost Automotive Power Electronics" project with additional researchers from MIT to apply IPEM technology in an integrated electric water pump for an advanced automotive architecture with 42 V of dc-electric accessories. The new integrated water pump assembly included a permanent magnet machine, a shaft mounted pump impeller, and a power electronics controller combined into a single housing, using flip-chip-on-flex planar interconnect technology for the IPEM at the heart of the motor drive.

Birth of the IMMD

In 2003, CPES defined the basic concept of the integrated modular motor drive (IMMD), which was based on a modular stator architecture that consists of basic building blocks that combine each stator pole and its concentrated winding with a single-phase in-



verter module dedicated to exciting that winding. We launched parallel efforts to develop the modular permanent magnet machine and the modular power electronics needed to implement the IMMD concept.

While this IMMD machine was under development, we worked on design features and characteristics for the phase-leg inverters needed to excite each pole winding. The expected high-temperature environment (greater than 100°C) for the IPEM led to the adoption of a film capacitor in place of the lower-temperature electrolytic capacitors used in conventional motor drives.

In order to minimize parasitic inductance and the associated transient voltage ringing, we paid special attention to interconnections between each inverter phase-leg and the front-end rectifier as well as its connections to the neighboring inverter units.

Prototype machines

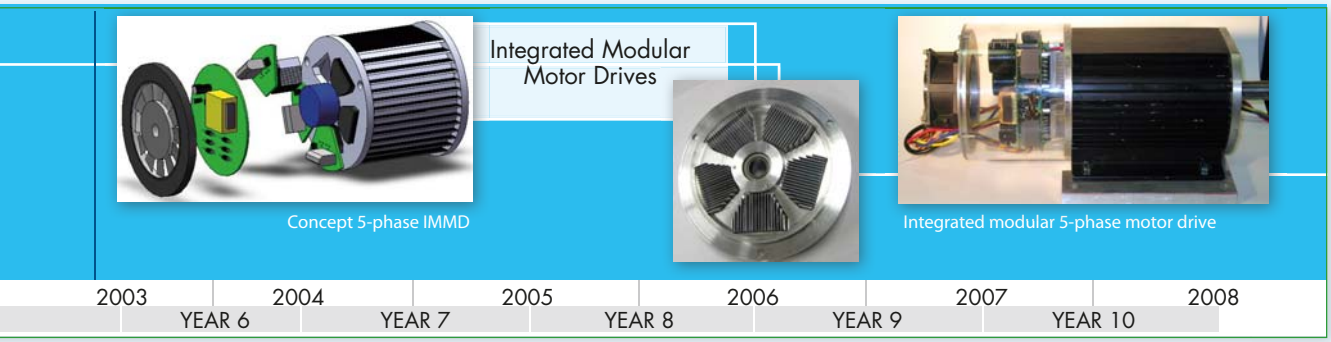
The prototype five-phase permanent magnet machine was successfully tested using a breadboard five-phase inverter during 2007. Separately, a demonstrator version of the five-phase IMMD inverter was tested in a benchtop configuration that was intended to focus on the physical dimensions of the inverter phase-drive units and their electrical performance characteristics.

Integration in one housing

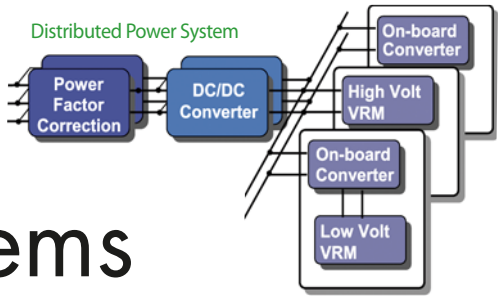
In Year 10, we redesigned the inverter phase-drive units together with a compatible motor housing so that the five-phase inverter and machine can be assembled in the same structure. Although this Year 10 IMMD assembly is a demonstrator unit rather than a production prototype, it includes many of the key physical and electrical features needed by motor drive manufacturers to evaluate the viability and readiness of IMMD technology.

Cooperative success

The success of the motor drives systems research has been possible because of cooperative efforts throughout the organization, including advances made in advanced power semiconductor development, sensor integration, standard-cell active IPEMs and IPEM packaging. Promising concepts developed through CPES in the motor drive systems area are already having an impact on new generations of commercial motor drives that are moving inexorably towards higher levels of integration.



Power Distribution Systems



Ten years ago, the distributed power systems (DPS) concept became widely used in computer and telecommunications products. The front-end power processing and interfacing with utility lines was performed at a system level: a power factor correction (PFC) converter followed by an isolated dc-dc converter, and a number of small, point-of-load converters that were placed on the circuit board for their intended loads.

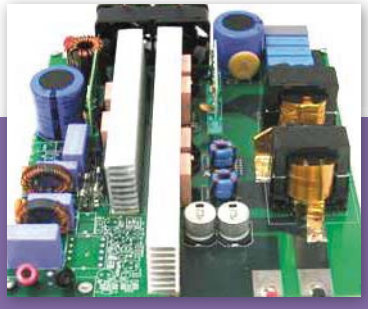
This opened the opportunity in the power supply industry to develop a standardized modular approach to power processing — an ideal application for IPEMs. From the start, CPES researchers believed that applying the IPEM building block approach would greatly reduce the product cycle time and improve power density, performance, reliability, and cost.

Telecom, server testbeds

During the first five years, research focused on testbed demonstrations of IPEM technology for telecom and servers. For the dc-dc converter, we chose an asymmetrical soft-switching half-bridge topology for its high efficiency and simplicity. For the power factor correction converter, we used the then newly developed SiC diode and CoolMOS® devices, which cut power loss by more than 35 percent.

This enabled us to successfully demonstrate a low-profile (1U) design with a 30 percent improvement of power density. This design became the baseline converter from which we replaced discrete components with integrated active and passive IPEMs in the next generation.

In 1998, the best commercial converters supplying 1 kW, 48 V, dc power for internet servers from a 120 V, 60 Hz, ac outlet had a 2.6-in. height and a 5.8 W/in^3 power density.



In 2000, the first CPES baseline converter sported discrete devices and a power density of 7.5 W/in^3.

The 2003 testbed IPEM prototype of the same converter had 1/6 the number of component and was half the size, with a power density of 11.7 W/in^3.

PERFORMANCE, EFFICIENCY ADVANCES

• The first active IPEM based on embedded power packaging technologies was demonstrated in 2000.

• Passive IPEMs were demonstrated for the first time in 2001. The IPEM significantly improved performance and power density and integrated the energy storage elements, including two capacitors and a resonant inductor together with three winding power transformers.

• Improved active IPEMs were demonstrated by successively integrating all the active devices of the PFC and dc-dc converters in 2003.

• The first prototype of the integrated EMI filter was developed in 2003.

• In 2003, an integrated front-end converter using active and passive IPEMs with improved efficiency, power density, and performance, was exhibited.

Shift to broader impacts

With the initial IPEM successes for data servers, CPES shifted research in the second 5 years to explore broader impacts on society's electrical energy usage. Advanced electronic power distribution system architectures have been investigated for reliable supply of electrical energy in internet infrastructure, defense applications, ships, and airplanes, as well as in the emerging distributed generation from alternative and renewable energy sources. In order to improve the understanding of complex multidisciplinary interactions and tradeoffs in such systems, a novel modular-terminal-behavioral approach to modeling of power system components has been developed.

As an example, over the past three years, we developed a flexible, autonomous hybrid power system testbed for future self-sustained applications that can demonstrate how power electronics can help save energy, protect the environment and improve people's lives. The testbed incorporates renewable sources, power converter-based loads, and a grid-interfaced, controllable distribution network.

The testbed is a self-contained, 3 kW, autonomous hybrid power system for data communications in remote locations. It is designed to provide uninterrupted energy supply to the data servers and air-conditioning as electrical loads. It is also a scaled-down, generic electronic power distribution system that can demonstrate applications such as future homes, hybrid electric cars, aircraft, and ships.

The testbed includes a solar photovoltaic source simulator, a wind turbine, and an ac grid connection as energy sources. Lead-acid batteries, a battery charger, ac transfer switch, dc-ac inverter, and mixed ac-dc power distribution with computer-controlled measurement and supervision comprise the energy management system.

In addition to its initial application demonstrating integrated power electronics converters, the new testbed inspired new research projects on system architectures and control, power/energy management, and system integration.

CPES has targeted systems and applications in which the technology at the time could achieve the greatest impact on energy efficiency.

The experimental electric power system testbed is a 3 kW autonomous hybrid power system for studying emerging electric systems in data centers, sustainable homes, ships, aircraft and hybrid electric cars.

Sustainable Building Initiative

Energy and sustainability have become key issues across the country and around the world. Renewable and alternative energy sources and energy conservation are receiving unprecedented attention. Power electronics, more than ever, can play a significant role in society's transition to sustainable development.

While our integrated power electronics technology has been shown to reduce energy use in several high-energy-consumption applications, the next step is improving energy efficiency in the home. Homes provide one of the largest opportunities for both improving energy-efficient utilization and for distributed energy generation.

CPES is developing a sustainable building initiative and has launched several projects during Years 9 and 10 to jump-start research in this area:

- A dc-based electric power system as a future home testbed at Virginia Tech. The goal is to design and construct a future home testbed by renovating part of a CPES laboratory into a dc-based system with nominal home loads, renewable sources (wind and solar), advanced energy storage, a grid interface, plug-in hybrid, and an energy management system.
- High-frequency power distribution system at the UW-Madison campus. Major activities include an initiative to study and build a high-frequency (400 Hz or higher) ac distribution system testbed, combined with efforts to integrate plug-in hybrid vehicles into the system, and an investigation of the suitability of sustainable buildings as microgrids.
- Integrated energy systems for portable information and entertainment appliances. This research at RPI is focused on developing an integrated energy system architecture that can provide and optimize the energy supply to portable entertainment and information appliances. These devices are expected to grow in number and significance in future sustainable buildings, making the availability of such integrated energy systems increasingly important.


Electric energy management center
HVAC
Grid connection

OVERVIEW
Enabling Technology: IPEM

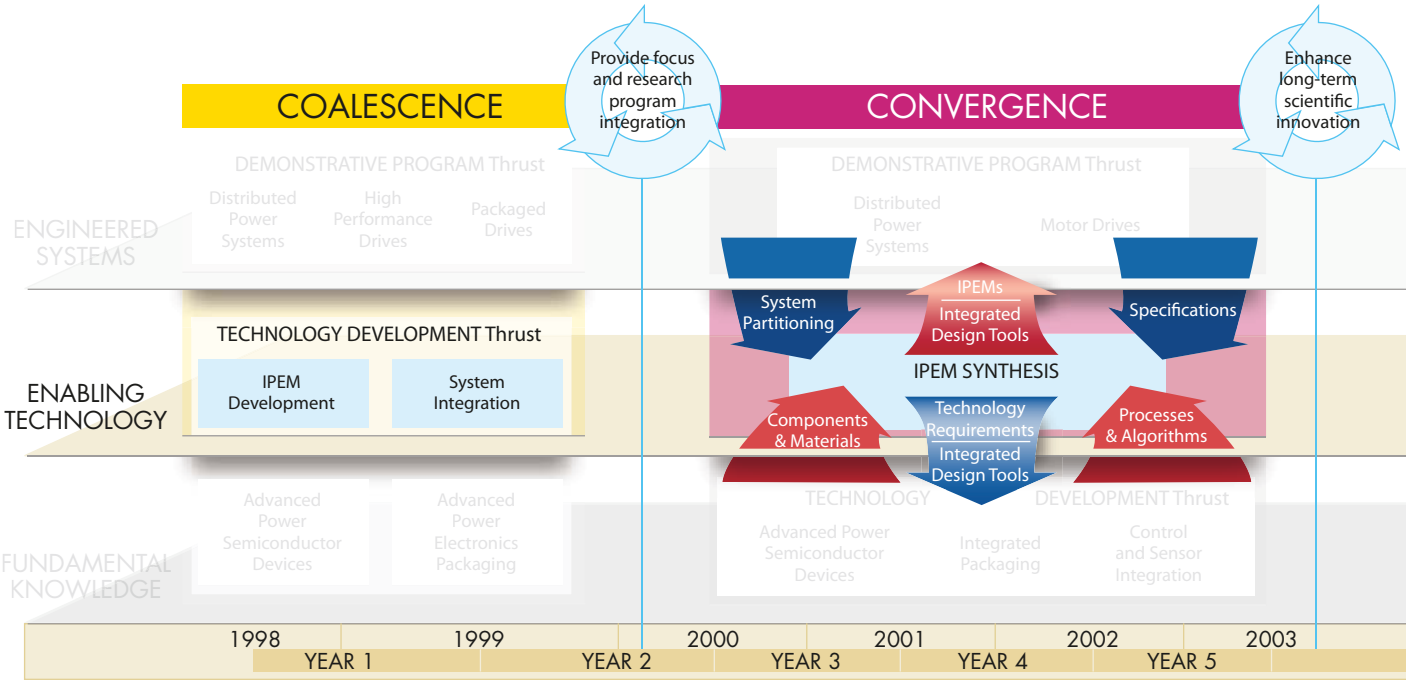
When CPES was formed, IPEMs were just a concept. We were convinced by standardizing, modularizing, and integrating power electronics technology, we could dramatically improve the performance, reliability, and cost-effectiveness of electric energy processing systems.

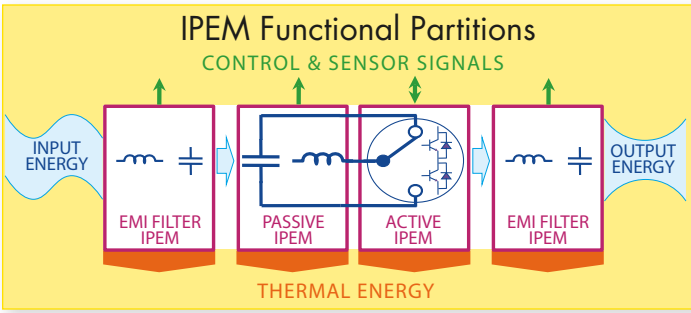
Central plane of ERC strategy

The IPEM, whether concept, design, or modules, has served as the enabling technology — the central plane of the ERC strategy — throughout the past 10 years. In this central plane, IPEM technology has provided the components, processes, packaging, and design tools for the engineered systems described in the preceding pages. At the same time, this enabling technology set the direction for the specifications and objectives of the fundamental knowledge research. Conversely, the goals and capabilities in the other planes also directed IPEM development.

Initial goals

The initial plan was to establish state-of-the-art benchmarks, stretching the boundaries of silicon-based technology. We planned to then pursue IPEM developments, such as integrating passive components, that would double performance, cost and reliability in five years. Generation three was aimed at improving performance, cost, and reliability by four times, while generation four – a fully integrated, three-dimensional multichip power module – would realize a cumulative 10-fold improvement over 1998 technology.





Basic functions of a power electronics system:

1. Switching elements to regulate energy flow
2. Electromagnetic energy storage and transformation for proper functioning of switching, control, and filtering
3. Spatial and temporal operations control
4. Thermal management
5. Mechanical/structural stability of components, modules, and total assembly

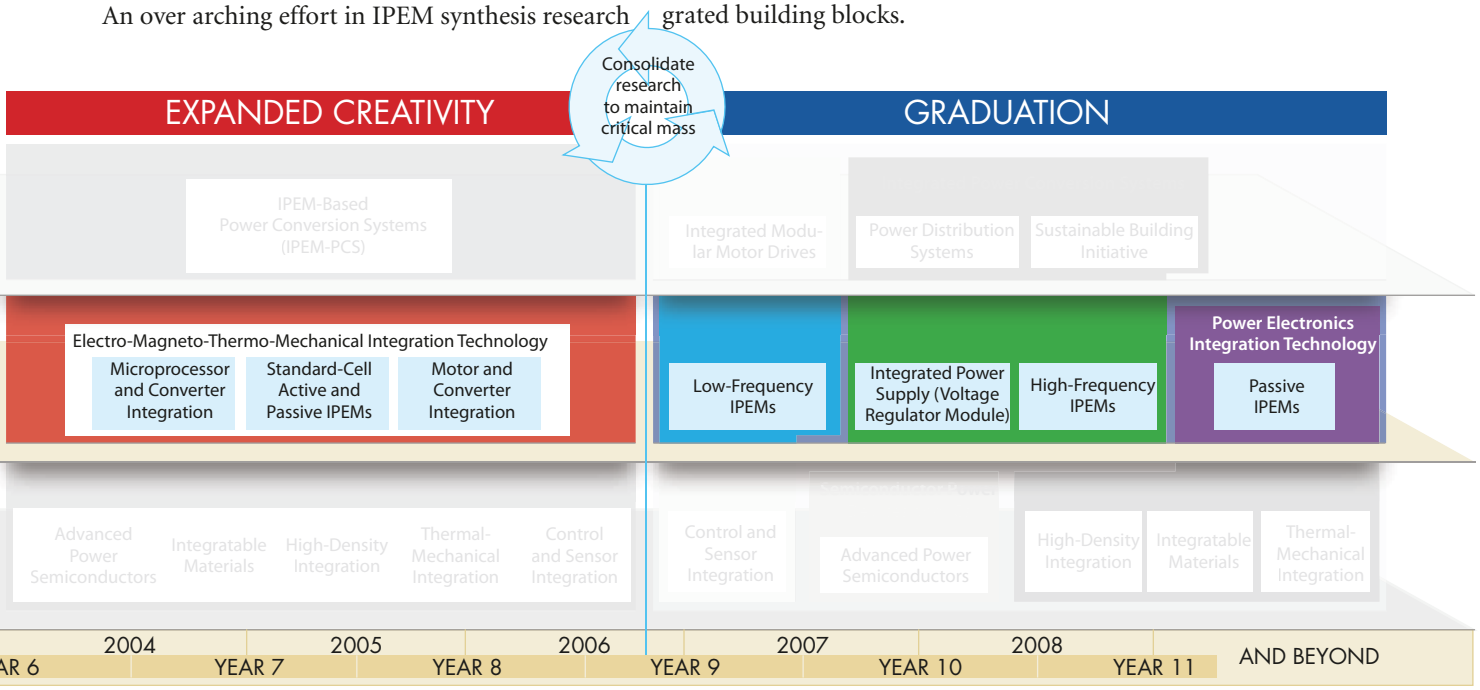
IPEM development

In the first five years, we made remarkable progress in IPEM development as we pursued development of integrated modules for motor drives and for power supplies. We demonstrated the first IPEM in 2000 using a CPES-developed embedded power packaging technique that included an active MOSFET device for power supplies that integrated the active components within the module. It was quickly followed by an active IPEM using IGBT devices for low-frequency higher-power applications; a passive IPEM; then a filter IPEM. A passive IPEM integrates the energy storage capacitors, inductors, and transformers. A filter IPEM also physically integrates inductors and capacitors, but is used specifically to attenuate high- and low-frequency switching noises.

An over arching effort in IPEM synthesis research progressed from the analysis of the multi-disciplinary design process to developing an integrated design methodology. The CPES software integration enabled commercially available models from many different segments of power electronics to be used for an overall IPEM system design.

Three continuing thrusts

With advances from CPES fundamental knowledge efforts, including a nano-silver die attach and silicon carbide diode, we proceeded with IPEM technology on two levels: high-frequency IPEMs for power supplies and low-frequency IPEMs for motor drives. In support of both thrusts, power electronics integration technology continues to translate engineering basics into the necessary technology and materials for integrated building blocks.



Integrated Voltage Regulator Modules

For new generations of microprocessors

Over a period of 10 years, the Intel processor has evolved from relatively low power consumption of 2 volts (V) and 10 amps (A) to still lower power consumption of less than 1 V and more than 100 A of current. This has been possible because of CPES technology that powers every Intel processor today.

The multi-phase voltage regulator module (VRM) technology at the heart of this success story is a specialized distributed power system. It has been a direct-commercialization effort, with a testbed including all the computers worldwide.

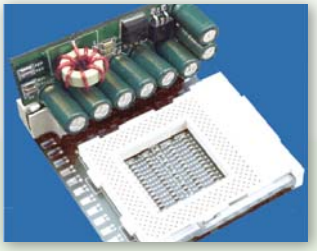
The new generation of Intel's microprocessor operates at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This mode is necessary to conserve energy and extend operation time for battery-powered equipment. A VRM is used to provide precisely regulated output with fast dynamic response so that energy can be transferred as fast as possible to the microprocessor.

The first generation VRM was too slow to respond to the microprocessor's transient energy demand. The initial solution was to use a large number of capacitors, which increased the volume and cost.

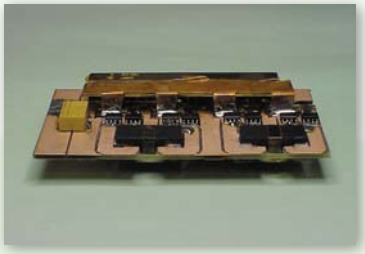
At the request of Intel, CPES established a mini-consortium that consisted of Intel, International Rectifier, National Semiconductor, Texas Instruments, STMicroelectronics and Delta. The goal of the consortium was to address the power management issue, with a target of supplying the power to microprocessors at 1.2 V and 60-100 A.

Breaking away from that era's conventional method of paralleling power semiconductor devices in order to meet the increasing current demand and efficiency requirements, CPES proposed a system that paralleled

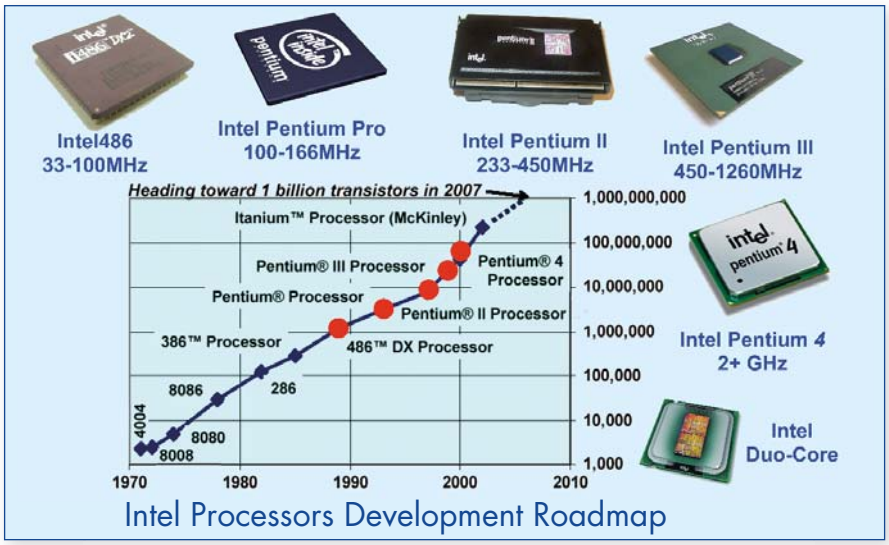
Prior to the Pentium Pro processor, Intel's 486 microprocessor used a "silver box" power supply with 5 V output.



The Pentium Pro employed lower voltage and more than doubled the clock frequency. This required a dedicated power module — a VRM, which was adjacent to the processor. This was not scalable.



In 1997, CPES proposed a multi-phase buck converter. The prototype showed a 600% improvement in power density, 1/3 the profile, a 1000% reduction of energy storage inductors and a 600% reduction of input/output capacitors.



Intel Processors Development Roadmap

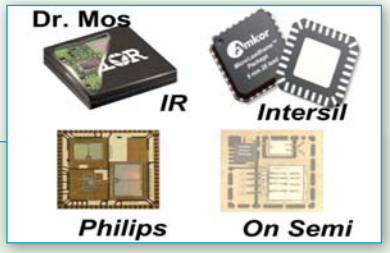
Although the Intel microprocessor followed Moore's Law in its early decades, the past 10 years show the processor outpacing the predicted 18-month doubling of transistor density. The sharp upward curve coincides with the use of CPES multi-phase VRM technology. CPES researchers are currently working on novel developments for microprocessors.

a number of mini-converters. By also phase-shifting the clock signal, not only were we able to cancel most of the output current ripple, but also increase the ripple frequency. Industry adopted the multi-phase VRM approach almost immediately.

Power management consortium

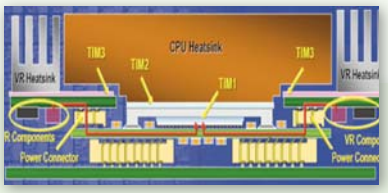
Today, CPES researchers continue to investigate this issue due to continuous reduction in voltage as well as continuous increase in load current. We are exploring new topologies and power architecture, new power semiconductor devices and power ICs, integrated magnetics, fast control and integrated packaging concepts to improve the transient response and minimize the I^2R loss due to continuous reduction in voltage as well as continuous increase in load current.

The mini-consortium has been renamed the Power Management Consortium (PMC) with an expanded scope to continue pursuing power efficiency in microprocessor-based computer and telecommunication applications through novel developments in power electronics topologies and system architecture. Membership totals 20 members at year 10, with much of the growth in the past year.



Within a year, every Intel processor was powered with the CPES-developed multi-phase VRM. By 2002, many companies offered IPEM products, referred to as "Dr. MOS" for point-of-load and VR applications.

Among other innovations, CPES promoted the idea of replacing conventional wirebond with direct bonding and introduced techniques such as flip-chip-on-flex and "embedded power." In 2002, firms introduced products without using wirebond.



As clock frequencies and power requirements continue to rise, CPES is developing novel architectures to push the technology to meet these future demands. A two-stage solution provided one step along the way.

The testbed for these systems is the most popular commercial microprocessor in the world.

High-Frequency IPEMs

For integrated power supplies

The IPEM concept was conceived when researchers at Virginia Tech first developed the multi-phase voltage regulator module for power processing of the Intel Pentium II chip. Power supplies have been an ongoing CPES theme in one form or another ever since. As electronic equipment shrinks in size, power supplies must minimize accordingly. Therefore, IPEMs for power supplies are typically high frequency in nature (up to MHz range) in order to reduce the size and weight of the passive components.

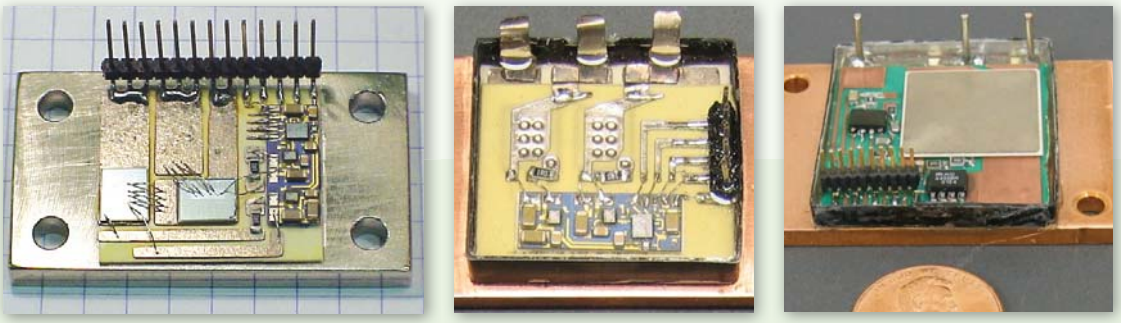
Challenges

Improving integration and reducing the packaging size are ongoing challenges for high-frequency IPEMs. Continued development depends on concurrent advances in materials, packaging, and power devices. Another challenge is parasitic capacitance. As more components occupy a smaller space, their proximity to each other encourages unwanted parasitic capacitance to arise.

High-frequency IPEM developments

The first IPEM was an active high-frequency device for server power supplies. It was based on a wire-bond approach and used for benchmarking. Each succeeding generation showed improvement in reducing interconnect parasitics and in cutting the common mode noise current that arises from parasitic capacitance inherent with the multi-layer structure.

The first passive IPEM was also for high-frequency power supplies. The passive IPEM replaced the functions of discrete capacitors, inductors, and power transformers. The integration was built upon multi-



1991 2001 2002

Three generations of IPEM development for server power supplies. All of these early IPEMs were based on the wire-bond approach for benchmarking purposes. The next generation shows improvement in reducing the interconnect parasitics and in reducing the common mode noise current due to parasitic capacitance inherent with the multi-layer structure. The third generation shows an embedded IGBT and SiC device with double-sided cooling.

layer, three-dimensional structures that used materials with different properties. This technology was quickly integrated into commercial products seeking improved thermal management.

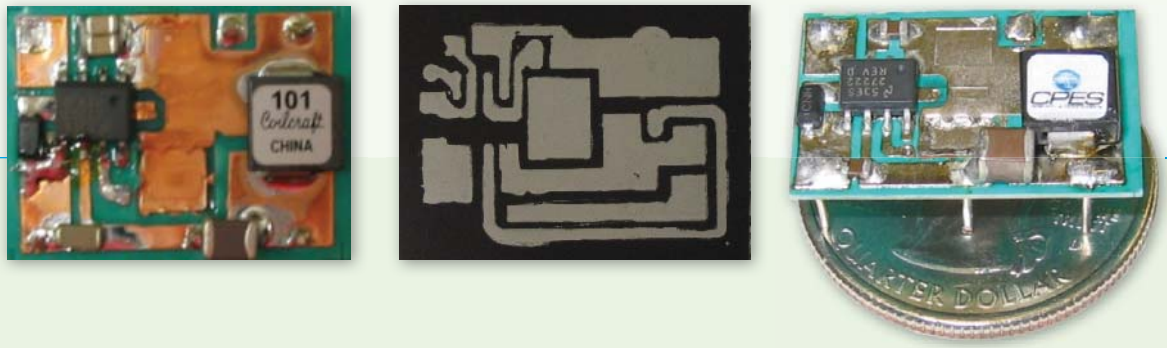
CPES later developed filter IPEMs for electromagnetic interference (EMI) and radio frequency (RF) interference. The EMI-filter IPEMs integrated magnetics and dielectrics for frequencies between 100kHz and 10MHz and was developed for use in a ballast in a 20W high-intensity-discharge (HID) lamp.

Integrated power supplies

As IPEMs and their supporting technology developed, CPES pushed to develop a three-dimensional integration of a complete power supply, combining active, passive, and filter IPEMs in a common structure. The goal is a complete physical integration in a three-dimensional multi-chip module so that power supplies can be even better integrated with microprocessors.

CPES has developed a demonstration integrated power unit, using a "stacked power" architecture. Active components are embedded inside ceramic layers that have high thermal conductivity. With moderate air flow, a heat sink can then be eliminated. The passive components are integrated with the active components using low-temperature co-fired ceramics. During testing, the single-phase module achieved 83 percent efficiency at 18A output current and 91 percent efficiency at a light load of 4.5A. The light-load efficiency shows promise in computer-related applications.

Integrated Power Supply technology is still in its infancy and CPES researchers are tackling the issues with a multi-disciplinary team of experts in materials, packaging, semiconductor devices and circuits, and system-level expertise.



CPES 3-D integrated power supply converter module, showing the first physical integration of all active and passive components in a single package.

Low-Frequency IPEMs

For integrated modular motor drives

Throughout its history, CPES has aggressively pursued the development of active IPEMs for motor drives and other applications with switching frequencies of 20 kHz or less. The common theme of this research has been to develop new features and new packaging technologies that combine to advance the state of the art of integrated power module technology. The development of motor drives with integrated power electronics is a major success for the CPES integration concept that is already achieving energy savings in many commercial applications worldwide.

Early years

One of the first motor drive power modules was the high-performance drive IPEM consisting of an IGBT-based inverter phase-leg capable of delivering 75 A to a motor phase winding from a 600 V dc bus. Although this early benchmark IPEM used conventional chip-and-wire interconnect technology, it already embodied the philosophy of integrating gate drives and higher-level features inside the power module.

Research effort began early in CPES to develop the concept of a flexible active gate drive that would incorporate a combination of advanced features applicable to the widest possible range of MOS-gated power devices. Desired feature include active control of turn-on and turn-off transitions, level-shifting, device sensing, protection, and gate drive power supplies. New techniques were developed to independently adjust both the dv/dt and the di/dt transition rates for switching events on a pulse-by-pulse basis.

During 2002-03 a prototype motor drive IPEM was designed and fabricated that incorporated flip-chip-on-flex planar interconnect technology and a version of active gate drive control. The prototype switched 10 A from a 300 V dc bus, appropriate for a 1-3 hp motor drive.

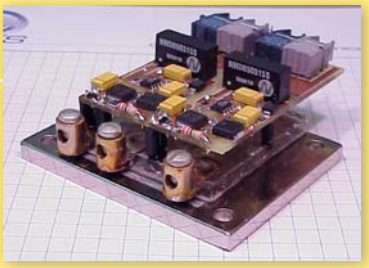
Standard cell IPEMs

After IPEMs were successfully demonstrated for both high- and low-frequency applications, CPES shifted focus to developing standard cell IPEMs, reflecting a desire to make the IPEM technology appropriate for as wide a range of applications as possible using high-volume production techniques to reduce cost. Embedded-power planar interconnect technology was adopted for subsequent generations of standard-cell-IPEMs in order to consolidate fabrication efforts and to take advantage of progress that was being made in applying this packaging technology to high-frequency IPEMs. Two generations of the embedded-power IPEMs were designed and fabricated during Years 7 to 9 and valuable improvements were made to the embedded power fabrication process during this time.

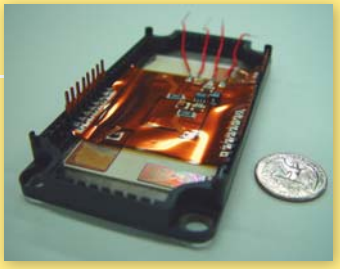
Advanced features

Several projects were conducted in parallel with the IPEM design and fabrication projects in order to develop advanced features appropriate for incorporation into IPEM designs. For example, an Augmented Phase-Leg Configuration (APLC) that is inherently immune to catastrophic shoot-through failures was invented and successfully tested. A new, charge-boosting gate drive power supply architecture was also developed that ensures the availability of gate drive power to the phase-leg upper switch under all operating conditions.

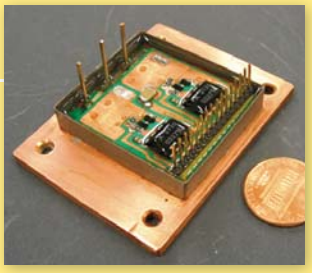
LOW FREQUENCY IPEMS: 1998 – PRESENT



High Performance Drive IPEM

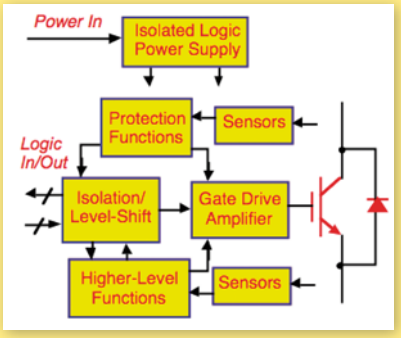


Motor Drive IPEM

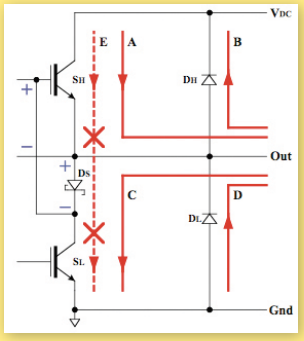


Standard Cell IPEM

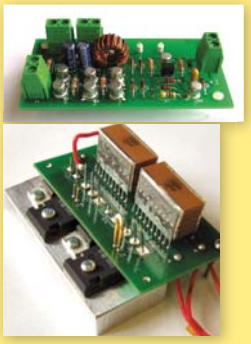
1998 YEAR 1	1999 YEAR 2	2000 YEAR 3	2001 YEAR 4	2002 YEAR 5	2003 YEAR 6	2004 YEAR 7	2005 YEAR 8	2006 YEAR 9	2007 YEAR 10	2008 YEAR 11



Universal Active Gate Drive (UAGD)



Augmented Phase-Leg Configuration



High-Temp (175°C) Phase-Leg

Significant attention was also devoted to thermal management issues. For example, early on, CPES investigated the thermal performance capabilities of heat pipes installed to remove heat from the upper surfaces of IPEMs in order to provide the advantages of double-sided cooling.

As a result, during Year 9, a high-temperature phase-leg and gate drive was developed and successfully demonstrated for operation in a 175° C environment, using silicon carbide MOSFETs and Schottky diodes for the power switches.

Continuing development

Low-frequency IPEM research conducted during the past 10 years was successful on several levels. This progress was achieved by actively encouraging the participation of CPES researchers from all of the campuses and nearly all of the research thrusts. CPES researchers plan to maintain this collaboration to continue the development and commercialization of low-frequency IPEMs. We seek to go on reducing the size and cost and to increase reliability and efficiency to meet the needs of commercial applications.

Passive IPEMs

CPES developed three standard-cell IPEMs for integration in devices: active IPEMs, passive IPEMs, and filter IPEMs. Continued development of active IPEMs is pursued in the high-frequency and low-frequency IPEMs in the preceding pages. We are also pursuing advances in passive IPEMs, which integrate the energy storage capacitors, inductors, and transformers and in filter IPEMs, which are passive devices, but used to attenuate high- and low-frequency switching noise.

Passive IPEMs influence device size

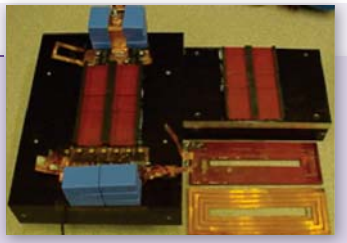
In power electronics devices, it is typically the passive components and their interconnects that determine the size and profile of a device. Continued development of this technology is therefore critical for continued miniaturization and integration.

In passive IPEMs, the passive integration is built upon multi-layer, three-dimensional structures using materials with different properties, such as high permeability, high dielectric constant, and high conductivity, in order to achieve integrated, multi-functional properties. CPES research in this area is part of our power electronics integration technology thrust and advances rely on work in high-density integration, materials, and thermal-mechanical integration.

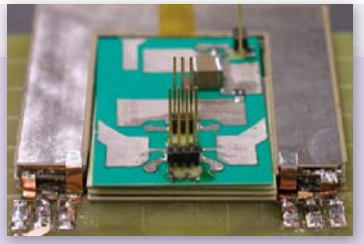
Passive IPEM advances

Functional and process integration with improved thermal management was successfully demonstrated in 2000. After the initial breakthrough, CPES quickly developed new advances in passive IPEMs, particularly exploring alternative or new materials to better integrate existing functions or to integrate new functions into passive IPEMs. Materials investigated include thin-film dielectric materials and a composite nanomaterial with ferrite and ferro-electric components.

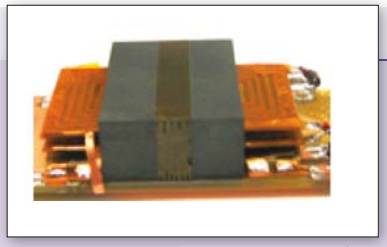
Advances in passive IPEM integration include the integration of inductors, capacitors and transformers, the development of super-passive IPEMs, thermal-passive integration, low-temperature, co-fired ceramic power inductors, and filter-integrated IPEMs.



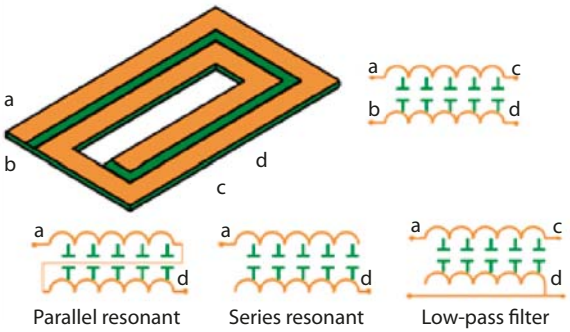
Integrated inductor, capacitor, and transformer (2000): CPES developed the construction technologies and processes for generic integration of inductors, capacitors and transformers.

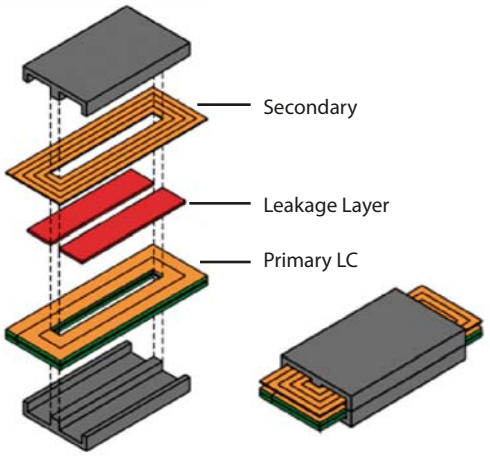


RF Filter integrated IPEMs: In 2003, CPES demonstrated an EMI filter circuit that integrates high-frequency absorbing elements as part of the construction of the converter system for a transmission-line RF filter.



Super-passives (2004): In an effort to improve the behavior of passive building blocks, an embedded layer was integrated into an EMI filter to cancel out parasitics effects, resulting in broader bandwidth.





Diagrammatic representation of technology for integration of electromagnetic power passives: LC primitive (left) and structure of a typical LLCT (right).

The structure for passive integration is built around the integrated LC-primitive, as shown in the figure above. When two primitives are located inside a magnetic core and the magnetic leakage between the two is enhanced by a magnetic leakage layer, the integrated structure exhibits the behavior of two equivalent inductors, an equivalent capacitor and transformer action called an integrated LLCT. By changing the interconnections on the same primitive, we can realize three different functions from the same physical structure. Consequently, when arranging two or more primitives in a structure as shown here, a multitude of functionalities can be obtained from the same structure merely by changing interconnections.

Ongoing challenges

Although CPES technology in passive IPEMs has broken ground on many new fronts, additional challenges arise with each new development. A major goal is to integrate active and passive IPEMs in one component, which will impose a host of new requirements upon the building blocks. For instance, the efficiency needs to be high at partial loads, or needs to be optimized for the entire system over its life. The environments will be harsher, with voltages reaching tens of kilovolts and the power reaching hundreds of kilowatts, leading to intense electromagnetic fields, temperature, and mechanical stress.

Thermal-passive integration: CPES embedded heat extractors into the magnetic materials of the passive IPEMs to improve the power density of passive modules without hurting electromagnetic performance. Our ceramic dielectric heat extractors embedded into ceramic magnetic cores doubled the loss-handling capability.

Low-temperature co-fired ceramic power inductor: A low-temperature co-fired ceramic inductor was developed for a single-phase buck converter operating at a switching frequency exceeding 1 MHz. The inductor outperformed similar commercial inductors and showed a 10x-plus power handling capability.

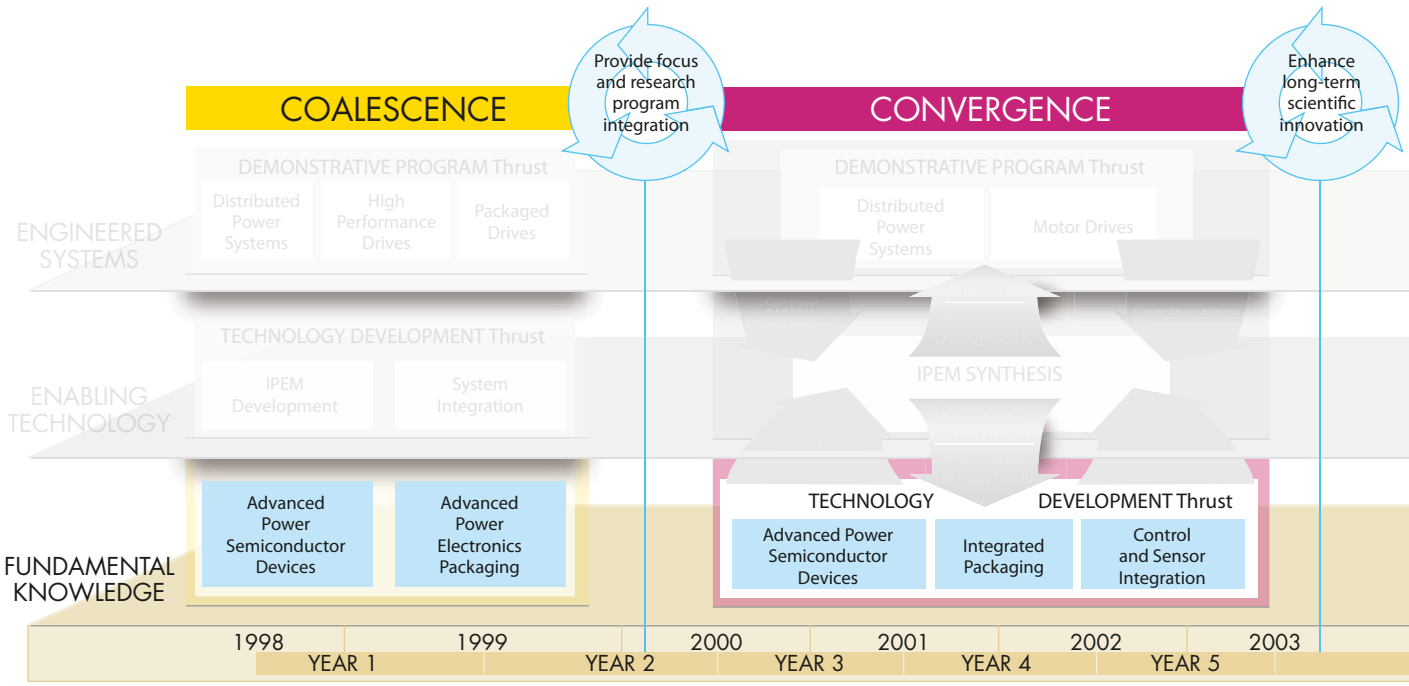
OVERVIEW
Fundamental Knowledge

Long-term, high-risk, and high-impact best describe CPES fundamental knowledge research. The development of IPEMs for power conversion and motor drives depended on significant advances in materials, integration technology, thermal-mechanical understanding, semiconductors, and controls and sensors.

Fundamental knowledge efforts were initially integrated into two general thrusts: advanced power semiconductor devices and advanced power electronics packaging. As the IPEM concept developed, the basic research in packaging shifted to integrated packaging. At the same time, advances in motor drives and power conversion created a need for specific fundamental work in control and sensor integration.

Strengthening research emphasis

After its 2003 site visit, NSF encouraged CPES to put more emphasis on long-term scientific innovation and in response. We identified five key areas: advanced power semiconductors, integratable materials, high-density integration, thermal-mechanical integration, and control and sensor integration. Those five thrusts continue today as part of our overall research strategy. Advance power semiconductors is a major component of the semiconductor power devices and ICs thrust of the post-ERC CPES. Ongoing work in control and sensor integration is being woven into the integrated motor drive systems thrust; while high density integration, integratable materials and thermal-mechanical integration are combining to form the core efforts in the integration technology thrust.



FUNDAMENTAL KNOWLEDGE THRUSTS AND GOALS

Advanced power semiconductors: The ultimate goal is balancing on-chip integration and integration at the IPEM level with optimum cost, reliability, performance, broad applicability and flexibility issues.

Control and sensor integration: The goal is to create the fundamental knowledge needed to "intelligently" integrate current and temperature sensors and active controls into power electronics with technology approaches that have the potential to significantly improve both functionality and reliability while significantly reducing costs.

High density integration: The goal is to effectively incorporate switching, energy storage and transformation, controls, conduction, and thermal management into a single system that is manufacturable, mechanically and structurally sound and can operate effectively and reliably throughout its lifetime.

Integratable materials: The goal is to develop materials technology that is fundamental to both integrating the various functions into a power electronics module and to understanding the physical mechanisms of module failure.

Thermal–mechanical integration: The goal is to develop the modeling and analysis tools to determine and overcome the thermal and mechanical barriers that might limit IPEM integration in a wide range of applications.

Many successes

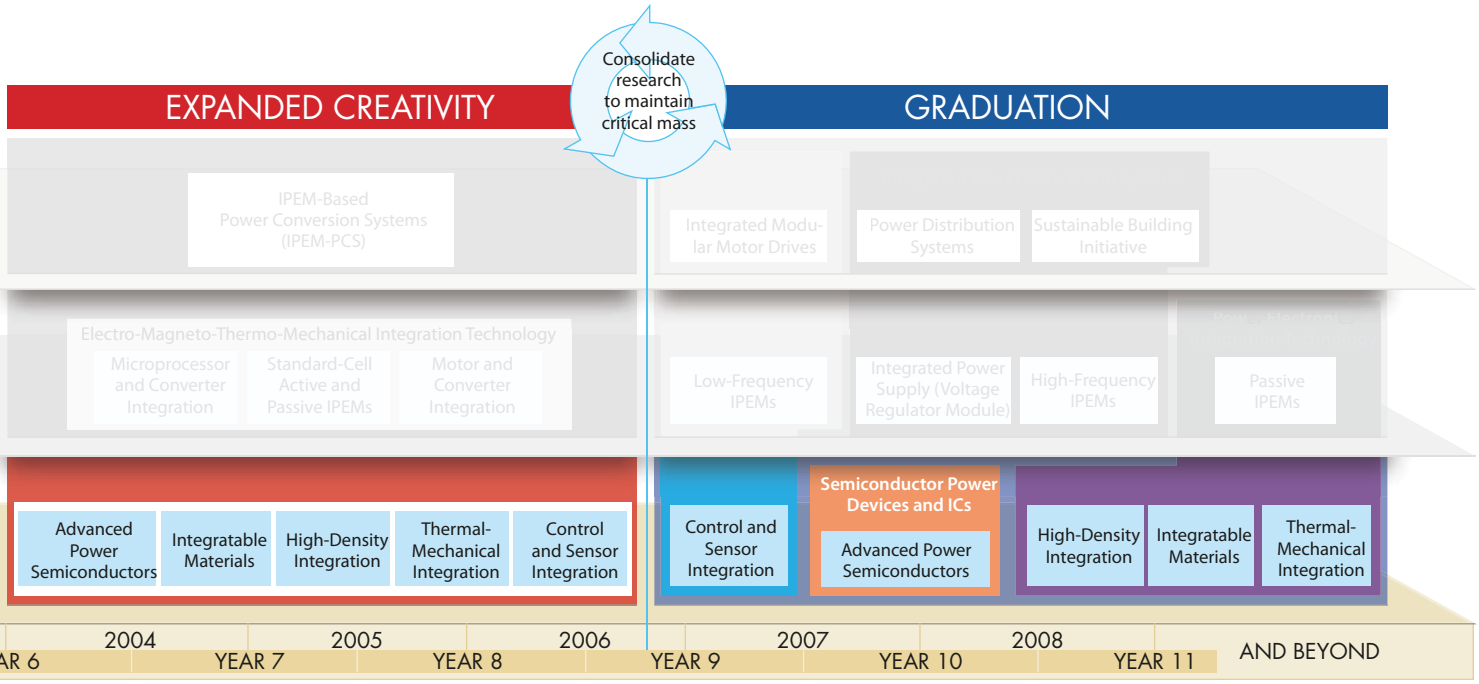
The success of the fundamental knowledge efforts is evident through the commercialization of several CPES developments, plus through the speed with which CPES was able to establish the concept and implementations of IPEM technology. Some critical advances include the nanosilver paste for attaching components, a multi-ferrous, multifunctional material,

Multi-university, multidisciplinary efforts

A key feature in the success of CPES fundamental knowledge efforts has been the interactions of researchers across universities and disciplines. The thermal-mechanical integration group, for example, pulled its team from across all five universities, tapping the special expertise of individual members.

Another example is the multidisciplinary team effort to address the needs for high-temperature packaging of wide bandgap power semiconductor devices. In this effort, the advanced power semiconductor group contributed silicon carbide device design, fabrication, and characterization; integratable materials researchers applied their nanoscale silver paste and high-density integration researchers did the package fabrication and testing.

Many such cross-functional teams were part of the CPES successes, especially after the IPEM concept developed and system-level issues arose.



High Density Integration

A power electronics system needs switching elements to regulate the flow of energy. It needs electromagnetic energy storage and transformation to allow for proper high frequency energy processing by means of switching and filtering. It needs control to execute all operations correctly, both spatially and temporally. It needs high-power, low-loss conductors, and thermal management to assure thermal stability and operation at the correct temperatures. Finally, the system needs the components, modules, and complete assembly to be mechanically and structurally sound in order to ensure appropriate operation and lifetime/reliability.

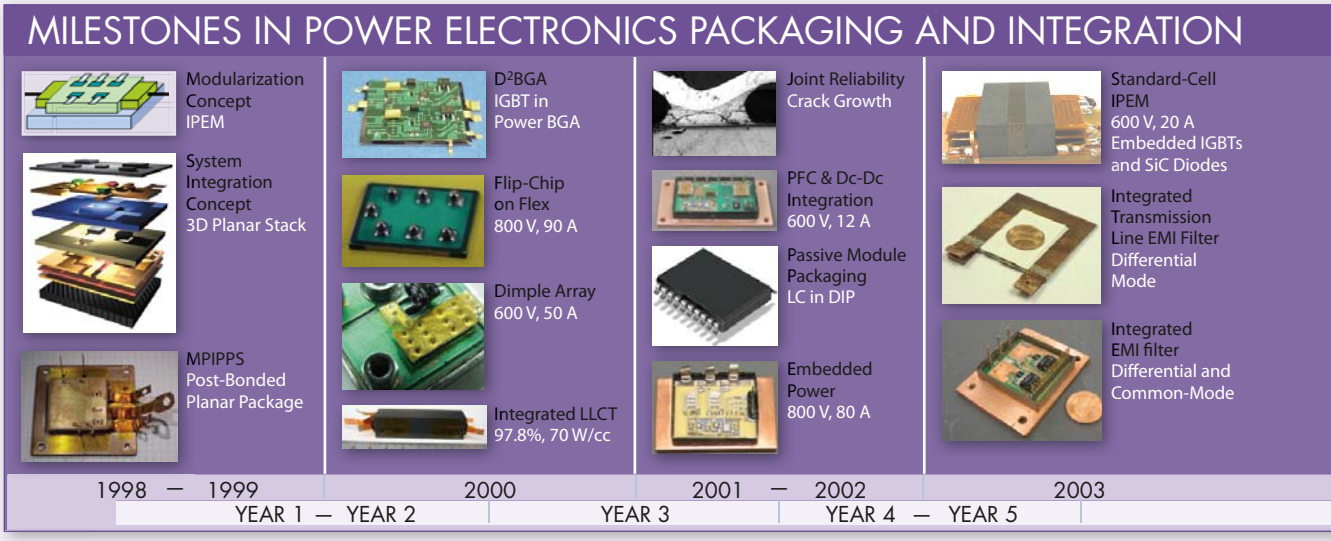
System-based hybrid integration

Considering all these requirements, it is clear while the switching function and the control function in some cases can be monolithically integratable into a semiconductor material, and in other cases might not be economically feasible. Energy storage components, on the other hand, must be integrated using different materials – especially for use at higher power levels. This leads to a system-based hybrid integration technology.

To accommodate the diversity of materials, structures, processes, functionalities, and power levels in a typical power electronics system, CPES chose the hierarchical "integrated packaging" strategy. Active, passive, and EMI filter IPEMs are essential building blocks in typical power conversion systems. Thermal management is another essential function that needs to be considered during IPEM development, especially in terms of integration opportunity.

Double-sided metalization

For integrating active modules, it would be highly desirable to have a structure with double-sided metalization. This would provide for three-dimensional integration as well as for double-sided cooling. Following the then-current wire-bond interconnect tech-



nology would not have allowed these possibilities. It was also clear that any choice of a non-wire-bond top interconnect would imply the additional process steps of making the industrially available aluminum contact pad device chips solderable by additional metal deposition. Although lead–tin solder compositions for the die attach also had industrial acceptance, it was clear that the program would have to consider lead-free interconnect material, since international pressure for lead–free electronics was mounting.

Integrating passives and filters

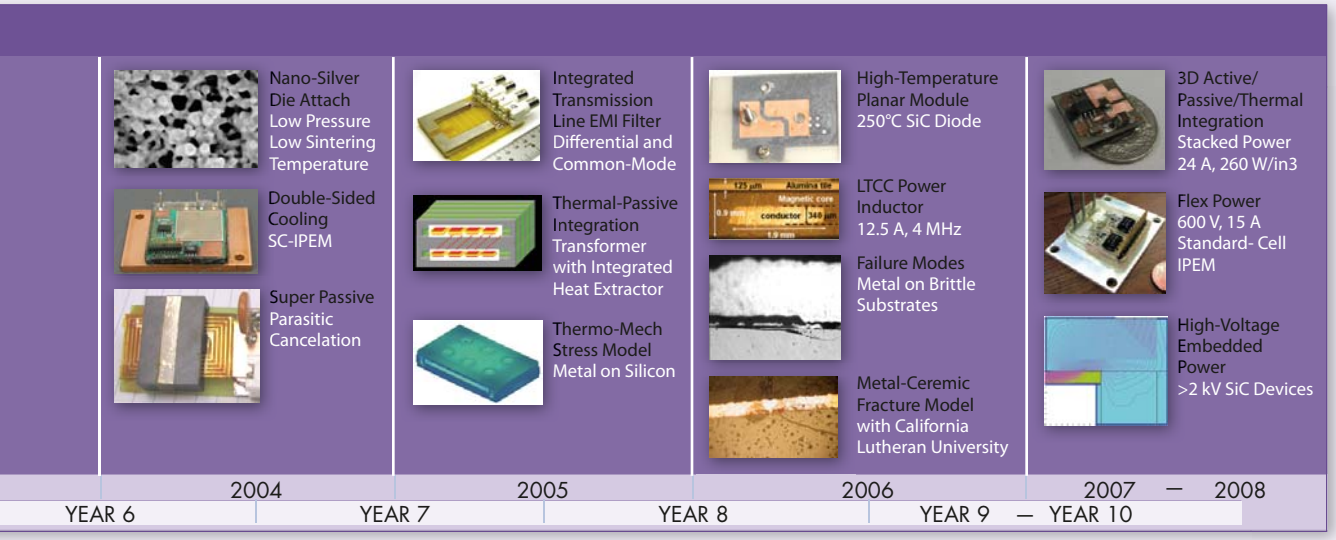
For the integration of passives and filters, the combination of ferrites and dielectric ceramics with a high dielectric constant had already been proven to be the best choice for use in frequency ranges up to 1 MHz, while for frequency ranges of 1 MHz and beyond, polymer-based dielectrics also became feasible at the kW power level. Due to the brittle nature of ceramic dielectrics, planar metalization by a deposition technology with low interface stress had to be used. Plasma metal spraying and electroplating were both developed as viable methods. While good adhesion by plasma metal spraying was readily achieved, electroplating required the deposition of thin film adhesion layers before plating, preferably by sputtering. Encapsulation of these modules could follow the practice for active integrated modules.

Optimizing volume

Having the same form factor for the active, passive and filter modules would optimize volume utilization in system packaging. Additionally, we selected planar technology for all modules for low-profile considerations and the possibilities for hybrid three-dimensional integration. Using planar conductors on ceramics, planar metal deposition of interconnects to the semiconductor die, planar magnetics, and other planar structural members in all three types of modules could lead to the same types of manufacturing processes for each type of module, which would be an important advantage for IPEM integration technology.

Improving thermal management & integration

In the interest of improved thermal management and three-dimensional integration, the technologies selected for the active power modules have rigid interconnects at both the top and the bottom of the die. A failure mode common to all the explored technologies is the cracking and voiding of the bottom die-attach solder layers due to the thermal cycling that occurred during the lifetime of the module. This work can also be extended to the failure modes in solder bodies, such as metal post interconnects and solder balls or columns, that are used in the top interconnects in place of the traditional wire bonds. In these cases, however, the stress concentrations have been shown to have a significant influence on the failure modes and lifetimes. A considerable effort also must be devoted to methods for detection of these failures by non-destructive techniques such as scanning acoustic microscopy and thermal impedance measurement.



Integratable Materials

Materials technologies are fundamental to both integrating the various functions into a power electronics module and to understanding the physical mechanisms of module failure. As such, this research thrust has played a vital role in CPES technology and development.

Materials research was initially a part of the packaging research thrust, but was strengthened in 2003 with the establishment of the integratable materials research thrust. The increased emphasis was in response to an NSF site visit encouraging CPES to emphasize the fundamental research.

Within the integratable materials thrust, CPES researchers conducted long-term, high-risk materials research in die bonding and thermal management, passive integration using multi-functional materials, electromagnetic fields sensing, and controlling physical failure mechanisms. Many of the advances from this work were inspired by developments in emerging fields, such as nanotechnology and micro-electro-mechanical systems (MEMS).

As CPES moves toward a post-graduation structure, materials research has been integrated into the power electronics integration technology thrust.

PASSIVE INTEGRATION USING MULTI-FUNCTIONAL MATERIALS

Problem: Passive components in electronic products, such as communication devices and power supplies, generally occupy a large space, resulting in bulky electronic packages. One way to reduce the overall size is to integrate or embed these components into the package substrate. This approach presents reliability challenges at the interfaces between the various types of materials stemming from mechanical, thermal, and thermo-mechanical stresses.

Solution: If a single material could have the desired ferroelectric and ferromagnetic properties, it could be used to make both capacitive and inductive components in the same space or volume. This would significantly reduce package size or weight and interconnection interfaces. Multiferroic materials in the form of ferroelectric-ferrite composites have been fabricated by mixing powders of the dielectric and magnetic constituents and then fired or sintered together to make EMI filters. However, this processing approach requires high sintering temperatures in excess of 1000°C, which challenges the use of good conductive metals, such as silver or copper in the integrated passives.

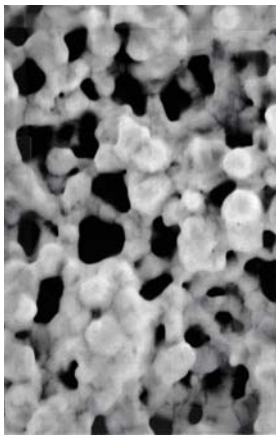
We synthesized multiferroic nanocomposites of ferromagnetic and ferroelectric materials. The sol-gel technique we used allows for uniform and intimate mixing of the individual components. Through the nanoscale route, novel structures with enhanced properties and functionalities can be realized. Nanostructures also require lower subsequent processing temperatures, thus reducing potentially adverse reactions between the components. Our multiferroic nanocomposite consists of nanosize particles of a ferrite phase coated with or embedded in a matrix of a dielectric phase. The nanocomposite can be sintered at a temperature below 1000°C.

MATERIALS FOR LARGE AREA DIE BONDING

Until recently, power semiconductor devices in single-chip packages or multi-chip power modules were fastened to substrates using either lead or lead-free solder alloys. These connections serve as electrical interconnections and heat dissipation paths. In the case of power modules, an additional large-area solder layer was often used to attach the substrate to a heavy heat-spreading plate. Solder was commonly used for chip attachment because of its low processing temperature: most solder-reflow processes can be done below 300°C. However, solders have low electrical and thermal conductivity. Also, die-attached solder layers are susceptible to fatigue failure under cyclic loading. Furthermore, because the soldering process involves the melting and solidification of solder particles in a flux mixture, voids often form due to entrapped gas evolving from the flux components and poor wetting of the surface by the solder. The growth of voids during thermal cycling is detrimental to the reliability and thermal performance of die-attached layers.

When lead was banned in electronic products, European electronic manufacturers implemented a silver sintering technology for interconnecting semiconductor chips. However the sintering technologies required a quasi-static pressure to lower the sintering temperature of thick-film silver pastes to about 250°C. The need for high pressure complicated the manufacturing process and placed critical demands on substrate flatness and chip thickness.

The CPES solution used nanoparticles of silver to lower its sintering temperature with low or no pressure. The driving force for densification of a particle compact increases with decreasing particle size, thus the densification rate – a product of thermodynamic driving force and kinetics – could still be high at low temperatures even with a low atomic diffusion rate. We formulated a uniform silver paste containing 30-nm silver particles. The paste has a uniform structure and viscosity can be adjusted for screen/stencil printing or dispensing. The sintered attachment has excellent electrical, thermal, mechanical, and thermo-mechanical properties and offers a simpler, lead-free solution for chip interconnection.



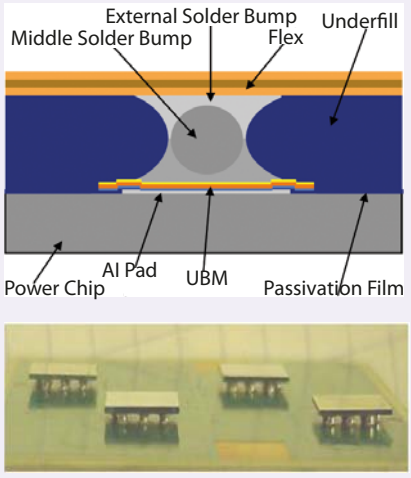
A paste made from silver nanoparticles is used to attach components resulting in much improved thermal management of integrated modules.

MATERIALS ADVANCES TO CONTROL PHYSICAL FAILURE

A key issue in the development of modules is the reliability of the interconnection scheme used and CPES has actively pursued planar interconnect technologies for packaging IPEMs. Typically, compromises are made to accommodate the electrical requirements to the detriment of mechanical integrity. In seeking to alleviate potential problems where the joints are exposed to stresses due to mismatches among the packaging materials and devices, CPES researchers developed the FlexPower concept.

With FlexPower, the top of the mounted devices (IGBTs and diodes) are interconnected by flexible metal straps. The straps can be plain copper or copper plated with silver. The joints to the devices are formed by reflowing solder to form an hourglass shape with the height controlled by a high-temperature solder ball in the middle. The increased height and hourglass shape, and the flexibility of the straps will enhance reliability.

The joints are relatively easy to fabricate as the procedure follows traditional joining processes. The technique is also conducive to automation in manufacturing. FlexPower technology also provides a route to high-temperature packaging because the devices will be attached to the substrate using nanosilver paste.



Hour-Glass Shaped Solder Joints

Thermal-Mechanical Integration

Thermal management issues are a key limiting barrier to the overall CPES goals of IPEM integration and the ability to impact a wide range of applications. These issues influence cost, reliability, and overall system performance, which necessitates the development of novel integrated cooling approaches specifically for IPEMs. The theoretical limits of these approaches must be determined, however, at a fundamental level, requiring the development of computationally efficient analysis tools.

As a result, CPES initiated the thermal-mechanical integration research in its second year to address these critical concerns. We recruited into the core team several faculty members from the mechanical engineering departments at Virginia Tech and the University of Wisconsin. Contributions were made in thermal model development and experimental verification at the IPEM and system levels, integrated design optimization, and double-sided cooling feasibility analysis.

Expanding the research group

After the second year of CPES, we expanded the team to include faculty members from North Carolina A&T and the University of Puerto Rico-Maygüez, who focused on the reduced-order model development, which was found to be a major roadblock for the advancement of integrated design methodology. In 2004, we further strengthened the team with members from Rensselaer.

The overall goal of this research thrust has been to develop integrated cooling technologies for planar structures and assess fundamental cooling limitations. Critical tasks included the development of (1) multi-level, multi-physics analysis tools and experimental techniques to determine the limitations of performance, (2) integrated thermal management technologies, (3) automated algorithms to generate reduced-order thermo-electric models, and (4) methodologies to characterize thermo-mechanical failure mechanisms.

Thermal modeling and analysis

Continuous efforts in the thermal modeling and analysis of IPEMs and IPEM-based systems have reached consistent agreement between experimental and detailed finite element results within 6 percent. To identify the fundamental limitations on the thermal management of IPEMs, we evaluated novel thermal management solutions such as double-sided cooling, thermo-electric coolers, mini- and micro-channel cooling by developing detailed thermo-electrical-mechanical finite element models, and experimental validation of the models. The feasibility of using miniature heat pipes for double-sided cooling of devices in IPEMs was established.

Fast electro-thermal lumped models

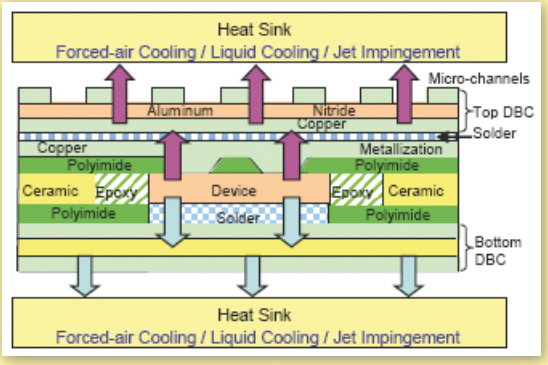
In order to facilitate the development of software integration tools for thermo-electrical parametric studies, package design optimization, and long-term reliability assessment, significant progress was made in the development of fast electro-thermal lumped models with automated parameter extraction techniques.

A novel 1-D lumped capacitance and partial element thermal modeling approach was developed and experimentally validated for several planar IPEMs. Another approach developed equivalent circuit reduced-order modeling in the form that can be automatically extracted from finite-element simulations.

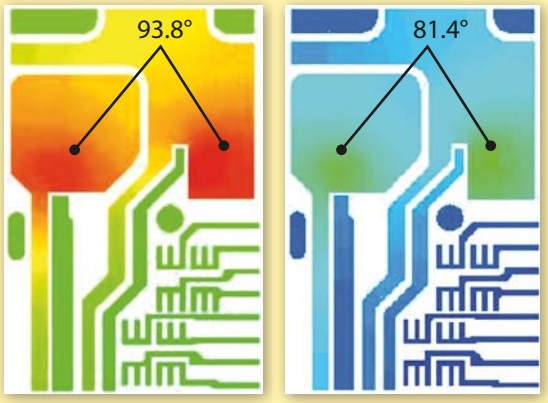
Thermal integration of IPEMs.

Later, major research focus was on integration of motor and drive electronics in a single housing, including the need to develop a modeling methodology that can be applied to the complex system associated with the thermal integration of the IPEMs with their motor poles. The modeling methodology for the design of an air-cooled system was developed and experimentally validated within the experimental and model uncertainties. More advanced thermal management systems, including forced air, liquid cooling, heat pipes, and direct liquid dielectric spray cooling were also investigated. Experimental measurements were conducted to study the cooling effectiveness of dielectric spray cooling with different nozzle configurations. The performance of mixtures of dielectric fluids in spray cooling of high heat flux surfaces was measured for the first time. Significant advantage of this technology to provide cooling was demonstrated.

CPES made major advances in double-sided cooling technology, illustrated here. One of the advances involved extracting heat by fluidic channel cooling. Using micro-channels on a silicon substrate, the CPES technology can extract heat at the astonishing flux of 200 W/cm^2.

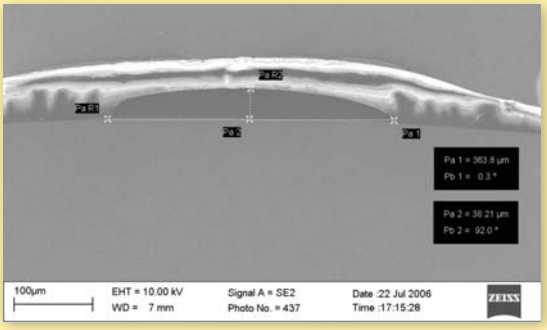


Concept of double-sided cooling for IPEM



Single sided cooling Double sided cooling

Temperature distributions on top-side metallization of standard-cell IGBT IPEM.



SEM photograph of a microchannel fabrication on Si substrate

Power Semiconductor Devices and ICs

Research in power semiconductor devices and integrated circuits (ICs) has fast-moving targets, thanks to the development speed of commercially available components. The goal is to focus on high value-added efforts relative to the marketplace, while maintaining optimum balance between short-term impact and long-term basic science and technology. The ultimate goal is balancing on-chip integration and integration at the IPEM level with optimum cost, reliability, performance, broad applicability and flexibility issues.

During the first five years, research in this area was focused on the improvement of silicon devices. Efforts included developing fast recovery diode, integrating fast recovery diode with IGBT and MOSFET, integrating pilot current sensors into IGBT, and developing lateral power ICs for low-voltage applications. During the second five years, research was more focused on wode-band gap devices using silicon carbide and gallium nitride.

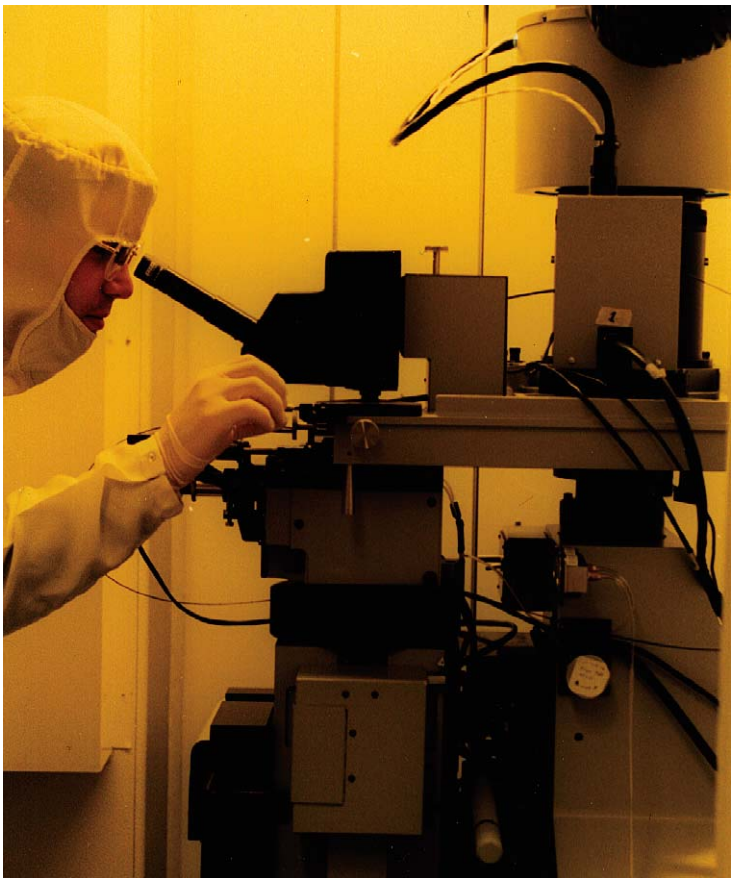
Breaking through performance limits

We are exploring and demonstrating device structures in discrete, smart discrete and integrable high-voltage power switching semiconductor devices as well as monolithic power ICs. Silicon has long been the dominant semiconductor, but some silicon power devices are approaching the theoretical performance limits imposed by material properties.

Wide bandgap semiconductors, particularly silicon carbide (SiC) and gallium nitride (GaN), have attracted much attention due to their remarkable material properties, such as wide bandgap (3.0-3.4eV), high critical electrical field (2-3MV/cm), reasonably high electron mobility (800-1000cm2/V-s) and good thermal conductivity (1.5-4.5W/cm-K), when compared to silicon. GaN has the additional advantages of heteroepitaxial growth of high-quality thin layers on large-diameter silicon substrates and device processing temperatures are compatible with those of commercial silicon foundries. These wide bandgap semiconductor devices are projected to have 100-10,000 times better performance than equivalent silicon counterparts. Besides, replacing bipolar silicon devices (such as pin rectifier and IGBT) with respective unipolar SiC or GaN devices (such as Schottky rectifier and MOSFET or HEMT) not only reduces on-state conduction power loss but also improves switching power loss. Consequently, our power device research spans silicon, SiC and GaN devices.

Technical directions

Our power device and IC research include: invention of novel device concepts and structures; design, layout and simulations to determine critical device dimensions and geometry and performance projection; development of integrated process flow, as well as key and possibly new unit process steps (such as SiC epitaxial process and GaN MOS process), for device or IC fabrication; static and dynamic electrical character-



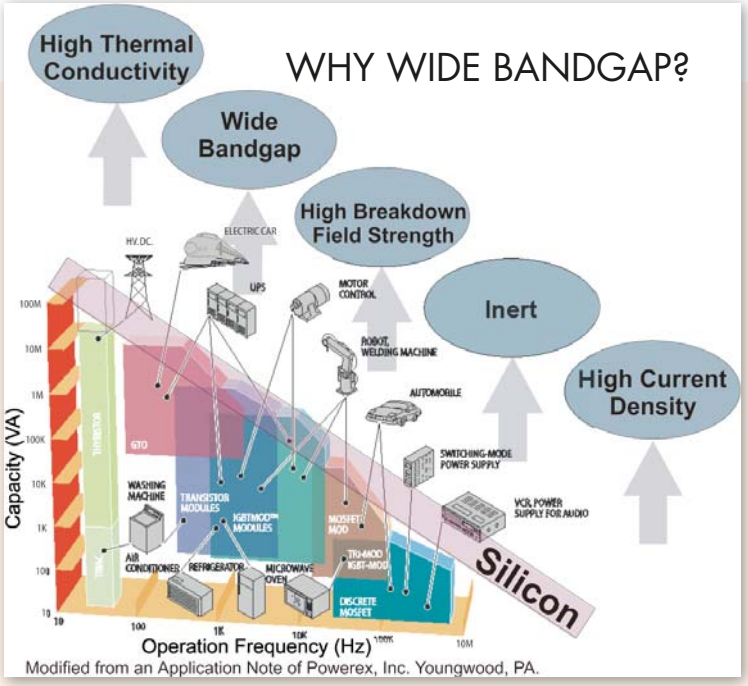
A student at Rensselaer Polytechnic Institute used a CGA stepper in his research with advanced power devices. Right: a close-up of the Karl Suss aligner in the laboratories at RPI.

ization of prototype to determine corroborations with simulation projections; and, development of SPICE-level simulation models for our novel devices as well as on packaged commercial devices to facilitate power electronic circuit simulations.

Dream device of the future

Over the last 10 years, we have demonstrated numerous silicon, SiC and GaN power devices and several Si power ICs. Also, we have transitioned several device designs and key unit processes to our industrial partners. In the future, we will continue our research into new emerging power devices and ICs, as well as into other semiconductors.

A particularly promising effort has been called the "dream device of the future." We have identified a device that can both carry and block positive and negative voltage at the same time. We are currently developing it and using a next-generation GaN device for the bidirectional current, four-quadrant switch – the first of its kind in the world.



Modified from an Application Note of Powerex, Inc. Youngwood, PA.

Some silicon power devices are approaching the theoretical performance limits imposed by material properties. Wide bandgap semiconductors, particularly SiC and GaN, offer advantages in critical electrical field, electron mobility and thermal conductivity.

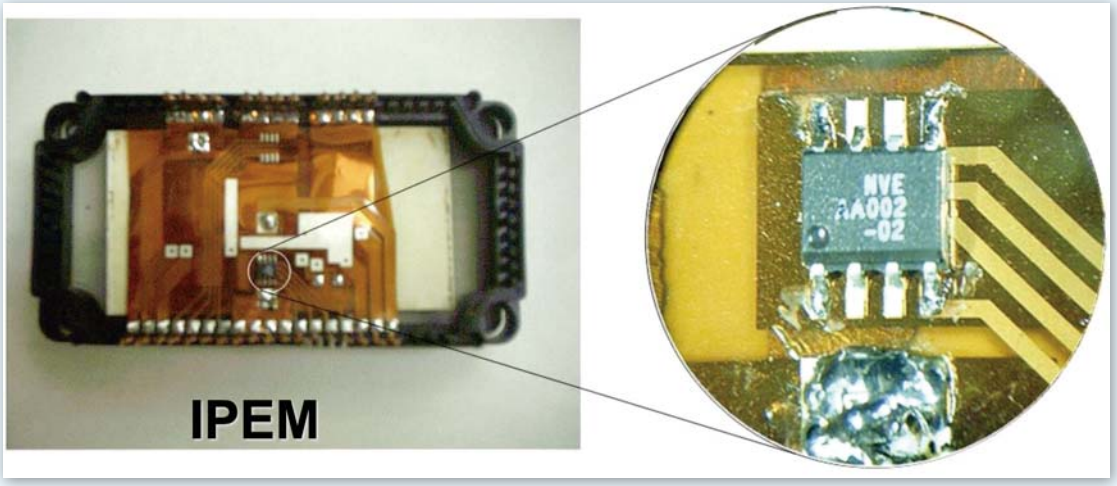
Control & Sensor Integration

The Control and Sensor Integration thrust was created as a direct result of the benchmarking study conducted in the first year and a half after the startup of CPES. The key issues identified in motor drives part of the study were that 1) reliability was dominated by thermal mechanical failures and that 2) current sensing was the most costly single component, and it also did not lend itself to high level integration in motor drives and power electronic converters.

The resulting goal of this thrust was to create the fundamental knowledge needed to "intelligently" integrate current and temperature sensors and active controls into power electronics with technology approaches that have the potential to significantly improve both functionality and reliability while significantly reducing costs. For this vision to be achieved, we indentified the critical issues: integrated current sensing internal to the IPEM structure, integrated spatial and temporal interconnect and junction temperature sensing with fast dynamics suitable for active thermal-mechanical stress control, and relative thermal control of parallel IPEMs for robust power sharing.

Consistent with our goal, there are four core subthrusts in the control and sensor integration thrust. Two subthrusts relate directly to current sensing integration fundamentals and two relate directly to active thermal-mechanical control.

- Integrated, GMR-based current, interconnect temperature, and junction temperature sensing supporting a validated thermal-mechanical observer
- Integrated pilot cell current sensing and cur-



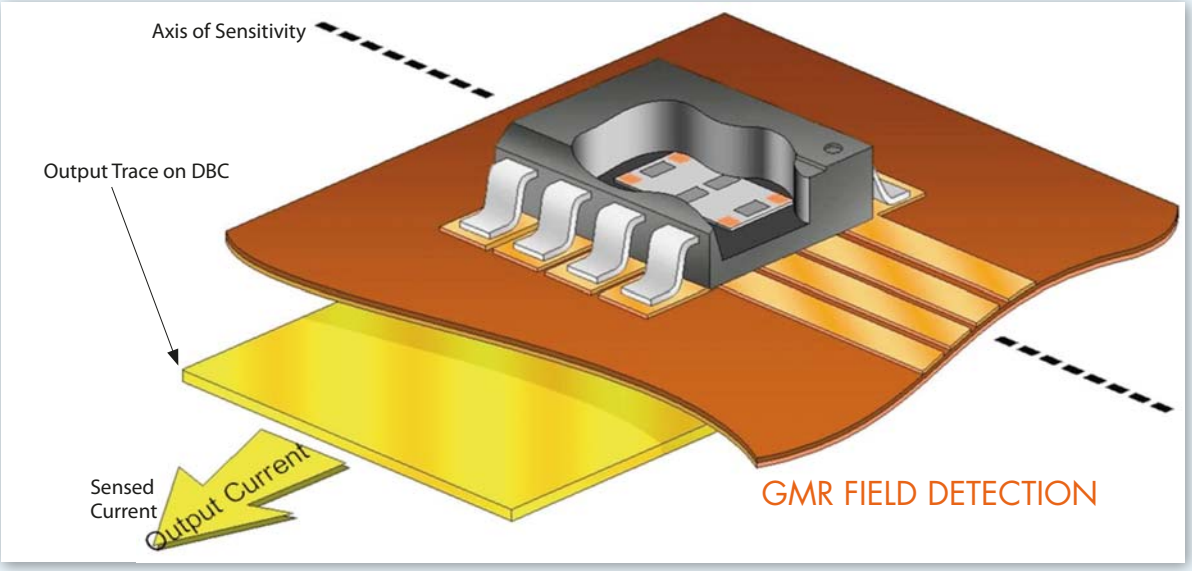
GMR FIELD DETECTION: Using the GMR field detector allows for a simplified compact integrated current sensor design.

rent reconstruction suitable for current regulated converters
- Active Tj and ΔTj controls based on validated thermal-mechanical strain to maximize reliability and device utilization
- Relative junction temperature control for thermal-based load sharing of parallel converters based on fully integrated sensing and integrated bus level signal utilization

During the 10 years of CPES, researchers in all four core subthrusts have developed the knowledge base for the technology implementation to become feasible. Even more important, the synergy between the core areas has become very evident in that the GMR point field integration technology, a multifunctional capability has been developed such that all of the key sensing needs can be addressed with these devices, thus significantly lowering cost while simultaneously improving reliability.

The control and sensor integration team is highly interdisciplinary, with strong engagement of both electrical engineers and mechanical engineers. In addition to this multi-physics team, advanced controls and estimation team members from both disciplines play a significant role in achieving robustness.

The control and sensor integration research has been integrated into the integrated motor drives systems work as we move to a post-ERC structure. This fundamental research is critical to continuing developments in motor drives and other IPEM and power electronics applications.



Education & Outreach

Power electronics is an enabling technology that can significantly improve the efficiency of electrical power use. For the discipline to achieve its potential impact, more engineers must be familiar and skilled in its technologies. In addition to developing technology and knowledge, CPES seeks to address the shortage of power electronics engineers and to improve the cultural diversity of the discipline.

Since the beginning, CPES partner universities focused on providing education and outreach programs that provide multi-disciplinary, team-driven, and systems-oriented educational opportunities to pre-college, university students, and practicing professionals. We currently oversee a power electronics curriculum at each partner campus, plus an outreach program that connects to industry, the large power electronics com-

EDUCATION & OUTREACH PROGRAM DEVELOPMENT

NSF YEAR 1: "CPES is poised to make a significant impact in power electronics education, especially on those campuses with less support and awaremess of the power electronics discipline."

NSF YEAR 3: "Educational program has accelerated and is now having significant impact across all the CPES institutions, impressive movement of students across the campuses."

1998	1999	2000	2001	2002
YEAR 1	YEAR 2	YEAR 3	YEAR 4	
	Established pre-college summer camps at VT, RPI and NC A&T Industry short courses and workshops at VT and UWM Student-led annual conference established	Cooperative agreements for distance learning and exchange New courses at VT, RPI, UPRM and NC A&T	New courses at RPI and NC A&T PER initiatives (pre-college outreach) funded	REUs established at VT and UPRM URP program at RPI SURE program at UWM Power electronics options at VT, RPI New courses at VT, RPI, UPRM and NC A&T

munity, and to pre-college students, with particular attention to women and underrepresented minorities.

Education committee

To achieve these goals, CPES established an Education Committee consisting of a director and one faculty representative from each partner campus, as well as research thrust leaders from integrated power conversion systems and integrated motor drive systems. The committee reviews programs, develops strategies for the implementation, and evaluates progress.

Cross-listed curriculum

CPES has developed 14 new courses among the partner institutions, bringing the total power electronics-related offerings to 86; almost a third – 27 – are in distance format and available to students in partner institutions and as well as some practicing engineers. A number of these new courses are a direct reflection of the Center's research results, particularly in the area of power electronics packaging, which is vital to our IPEM vision. As electronic systems grow more compact and complex, the interconnection of the components gets more difficult, requiring expertise across many disciplines. When CPES was formed in 1998, packaging was neither a mainstream research topic for power electronics nor a component of the curriculum.

Degree and certificate programs

Undergraduate options or certificate programs in power electronics are available at Virginia Tech, the University of Wisconsin, the University of Puerto Rico-Mayagüez and Rensselaer. A new M.S. program has been started at North Carolina A&T and a new Ph.D.

NSF YEAR 7: "Strong leadership and commitment to educational programs, cross-campus students visits, pre-college activities, and life long learning."

2003	2004	2005	2006	2007	2008
YEAR 5	YEAR 6	YEAR 7	YEAR 8	YEAR 9	YEAR 10
VT course module: Controls Power electronics option at UPRM Short-term exchange program New short course at VT	Power electronics concentration at UWM New Course: ECE 379 at UWM VT junior-level course modules: ballast/PFC Established diversity strategic plan Fellowship program: domestic Ph.D. students Pre-college programs at UWM and UPRM M.S. PELs program at NC A&T	New course at UPRM Second three-year REU program established at VT and UPRM LSAMP REU program at VT	More than 100 students have participated in short-term exchange to date. More than 700 students have participated in pre-college programs to date.	Revised VRM Short Course Disseminated/ published results at three conferences: ASEE - Hawaii ICEE - Portugal ICEER - Australia	Ph.D. program under development at UPRM

"The education program offered through CPES is truly exceptional and can be a model for other centers"

—2004 NSF Site Visit Report

program is in place at the University of Puerto Rico. Also, at UPR, participation in CPES has enabled the Power Engineering Group to drive a major undergraduate curricular revision, moving power electronics to a formal track; more than 150 students now take the introductory power electronics course each year. Since becoming a CPES partner, the power engineering program at UPR has become one of the largest undergraduate programs in power engineering in the U.S.

Student exchanges

CPES also has a strong commitment to furthering student education through partner exchanges and has sponsored travel scholarships for travel to partner institutions to perform collaborative research and participate in educational programs. More than 100 short-term student exchanges have occurred to date, with the participants primarily from North Carolina A&T and the University of Puerto Rico–Mayagüez.

Research experience for undergraduates

Focus in undergraduate programs has sought to raise the visibility of power electronics among students who are in the process of selecting a major field of study and to increase the numbers of domestic, female and underrepresented minority students entering the field. This was not a major emphasis before CPES. Now, the NSF has cited CPES as the model for all Engineering Research Centers for educational outreach.

Since 2002, the Center's Research Experiences for Undergraduates (REU) program has funded research experiences for students in several partner institutions. In 2005, students from outside the CPES partnership were included, with support from the Louis Stokes Alliance for Minority Participation; more than 80 percent of these students have been underrepresented minorities.

Student leadership council

The CPES Student Leadership Council plays a critical role in planning and executing the Center's education and outreach efforts. CPES students also participate in national SLC and CPES conferences.

Annual CPES Conference

The student council also organizes the CPES Annual Conference, which is designed to provide a forum for the Center to share its research progress with industry members and the larger power electronics community. CPES students are responsible for the technical program, poster session, general logistics and the development of the conference brochure, proceedings, and proceedings CD.

Pre-college outreach

Generating interest in engineering among young students is critical to growing the field. CPES has power electronics programs for pre-college students at all partner campuses, serving more than 700 high school, middle school, and elementary school students to date. These include summer camps for children of both genders, as well as sessions planned especially for girls. They also include one-day events, such as the Lego League in Southwest Virginia and Duke Power Day in North Carolina. Some events also target public school teachers.

Professional outreach

The most effective form of knowledge/technology transfer to industry is the employment of CPES

Left: E-Wheels at UWM was exposes freshmen and sophomore university students to power electronics.

Below, from left: First Lego League participants interacted with CPES students.

RPI Power Electronics Day Camp includes fundamentals of power electronics and hands-on demonstrations.

UWM's Careers Camp is held to stimulate interest in engineering and the sciences .

students. CPES has produced 382 graduates who are trained with a systems vision and are accustomed to working in a multidisciplinary team environment. To date, 216 are working in industry and contributing well, according to a CPES survey of CPES alumni and their managers.

Short courses/tutorials

In a ongoing effort to provide continuing education opportunities to professional engineers in industry, CPES has offered 10 short courses multiple times over the decade. In addition, CPES, has offered tutorials on major issues the day before the annual conferences. Research thrust leaders play a prominent role in this outreach, such as in 2006, when T.M. Jahns described the future of power electronics and electric machines in a series of invited lectures to engineering groups throughout Australia.

Professional conferences

CPES researchers actively promote the field throgh organizing research conferences and workshops. Recent examples include establishing the first international symposium on Power Electronics Technology for Distributed Generation Systems and organizing the International Power Electronics and Motion Control Conference and the Future of Electronic Power Processing and Conversion Workshop.

Industrial Collaboration

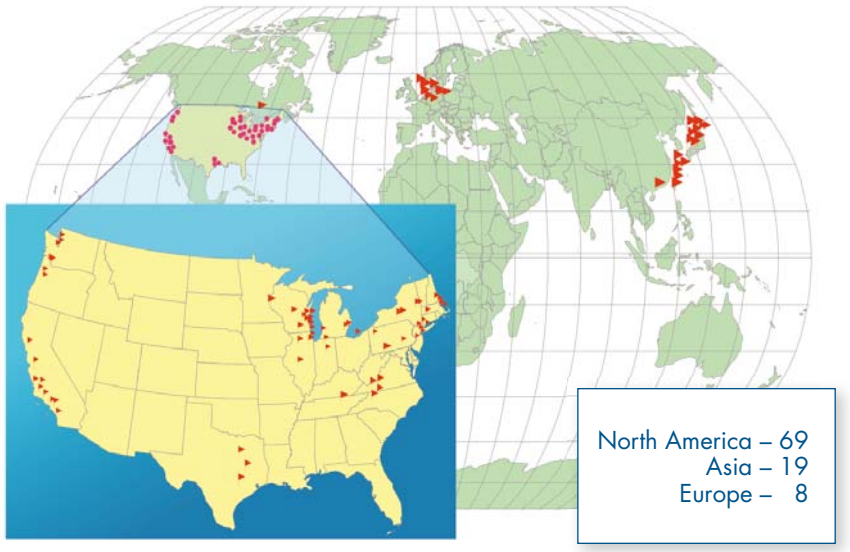
CPES is guided by a mission to improve industrial competitiveness of power electronics via an integrated system approach. With its industrial collaboration program, CPES is noted for timely knowledge dissemination and technology transfer, and a broad participation from industry members.

The industry partner program keeps the Center on track with relevant research and technologies viable for commercialization. CPES industrial collaboration and technology transfer efforts were cited by NSF as a model for all Engineering Research Centers. The CPES program includes the following components: industry membership, research collaboration, technology transfer, connectivity partnership, and graduates in the field.

Industrial membership

Before CPES, there were two pre-existing industrial consortia – VPEC at Virginia Tech and WEMPEC at the University of Wisconsin-Madison, each with about 50 industry members. These members were folded into the CPES industrial consortium. The backbone of CPES' connection to industry, the industrial consortium offers a four-tiered membership structure, with top-tier (Principal Plus) members paying $50,000 for the greatest opportunities to influence the Center's program and review CPES intellectual properties for possible product development. Principal Members also enjoy opportunities to guide CPES programs and evaluate intellectual properties, while Associate Members have less influence but access to the Center's research results, researchers, facilities, and education opportunities. The Affiliate Member category was designed to

CPES INDUSTRY MEMBERS WORLDWIDE



accommodate software and equipment donors as well as small start-ups.

The membership in CPES partnership program has remained robust despite global economic changes, mergers, and acquisitions.

Consortium support

CPES has received strong industrial consortium support through the years, from $400,000 in 1998 to more than $1.6 million in 2008. CPES faculty members have increased recruiting efforts recently to bring additional top-tier Principal Plus members on board. This increase clearly demonstrates that more companies are realizing the higher returns from their investment as they expand collaborative activities with CPES.

Industrial advisory board

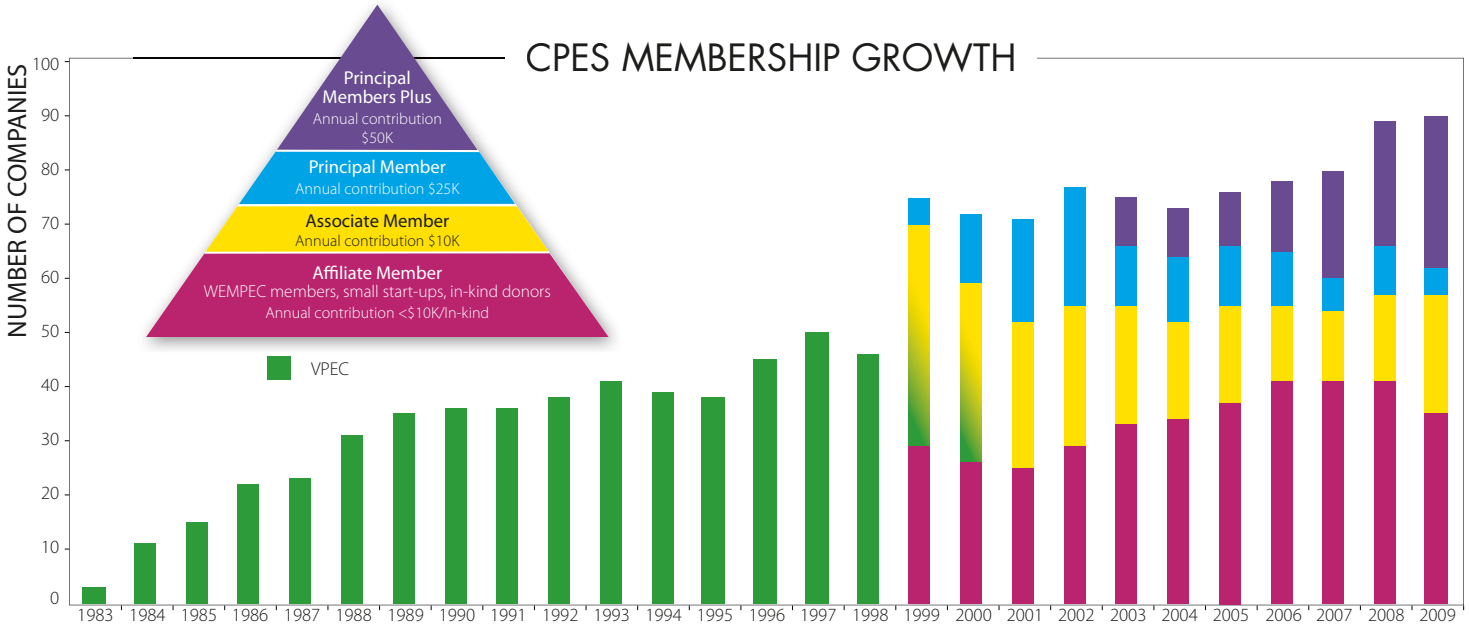
The CPES Industrial Advisory Board, which usually includes the top two tiers of the industrial consortia, grew more proactive after 1998, implementing a series of weekly and monthly board teleconferences and quarterly full-membership telecoms to filter issues and keep members engaged in CPES. As the Center grew and more issues arose, the board formed eight working groups between 1999 and 2001 on policies, research benchmarking, industry-student communications, manufacturability, SWOT analysis, research champion mentoring, reliability, and research review.

Power management mini-consortium

Power management mini-consortium research in voltage regulator modules was initiated in 1997 with the interest of a cluster of industry sponsors. After the formation of CPES, the group continued to work synergistically to develop pre-competitive technologies, pool resources, and share research results in consortium format. In 2002, the mini-consortium was folded into the CPES industrial consortium.

The multiphase voltage regulator module proposed by CPES in 1997 has been adopted as the standard industry solution to power every Intel microprocessor. The work has resulted in creating a billion-dollar market, the fastest growing sector of power electronics.

In 2006, CPES expanded the power management research scope beyond solutions for microprocessors and other point-of-load applications for mobile and wireless equipment, such as PDA, GPS, and cell phones. The power management scope encompasses the study of power architecture for laptob, desktop, server, and networking products, distributed modular power supply systems, topologies, analog/digital control, advanced packaging and system integration



CPES INDUSTRY MEMERS

PRINCIPAL PLUS MEMBER

ABB, Inc. – Corporate Research
AcBel Polytech, Inc.
ALSTOM Transport
Analog Devices
Crane Aerospace. Inc./ELDEC Corporation
Delta Electronics
Emerson Network Power
FSP Group, Inc.
GE Global Research
Hipro Electronics Co., Ltd.
International Rectifier
Intersil Corporation
Linear Technology
Lite-On Technology Corporation
MKS Instruments
Monolithic Power Systems
Murata Power Solutions
National Semiconductor Corporation
NXP Semiconductors
Primarion
Renesas Technology Corporation
Richtek Technology Corporation
Rolls-Royce
Siemens Corporate Research
Texas Instruments
The Boeing Company
TriQuint Semiconductor, Inc.
VPT Energy Systems

PRINCIPAL MEMBER

Eaton Corporation, Innovation Center
Groupe SAFRAN
Maxim Integrated Products
Rockwell Automation - Allen-Bradley
SEW-Eurodrive GmbH & Co. KG
BAE Systems Controls
Crown International

ASSOCIATE MEMBER

Dynapower Corporation
Hitachi Computer Peripherals Co., Ltd.
Huawei Technologies Co., Ltd.
Intel Corporation
Johnson Controls
L-3 Communications, Power Paragon
Microsoft Corporation
NetPower Technologies, Inc.
Nippon Chemi-Con Corporation
Northrop Grumman Corporation
OSRAM SYLVANIA, Inc.
Schneider Toshiba Inverter Europe
Semikron International GmbH
Shindengen Electric Mfg. Co., Ltd.
TDK-Lambda Corporation
Textron, Inc.
Toyota Motor Corporation
Trumpf Photonics, Inc.
Universal Lighting Technologies, Inc.
Vacon, Inc.

AFFILIATE MEMBER

American Super Conductor*
Ansoft Corporation
AO Smith Corporation*
Astronics Corporation*
Baldor/ Dodge/Reliance – Rockwell Automation*
Caterpillar, Inc.*
Continental Automotive Systems*
Curtis Instruments*
Danfoss Drives*
DRS Power and Control Technologies, Inc.*
Emerson Motor Company*
Fuji Electric Advanced Tech. Co Ltd.*
General Dynamics Land Systems*
GM Advanced Technology Center*
Hitachi, Ltd. *
Honeywell International Corporation*
JRI Solutions*
Kohler Company*
LEM USA*
Magnetek, Inc.*
Miller Electric Company*
Milwaukee Electric Tool Company*
Mori Seiki Company, Ltd. *
MPC Products Corporation*
National Instruments
Oak Ridge National Laboratory*
Oshkosh Truck Corporation*
Pacific Scientific EKD*
Phoenix International *
Plexim GmbH
Regal Beloit*
Rockwell Automation – Kinetix*
S&C Electric Company*
Schneider Electric – Square D*
Simplis Technologies
Synopsys, Inc.
TECO Westinghouse*
Trane Company *
VPT, Inc.
Whirlpool Corporation*
Yaskawa Electric America, Inc.*

*WEMPEC members

techniques. Since 2006, PMC membership has grown significantly, with 20 companies participating.

Intellectual property protection

Intellectual Property Protection Fund was implemented in 2002. Members teleconference quarterly to discuss invention disclosures with CPES inventors, and jointly decide which to protect with patenting costs covered by the fund. Members have a royalty-free, non-exclusive license to use the technology.

Industrial board workshops

As graduation from ERC status neared, the CPES Industrial Advisory Board organized strategy workshops, the Chief Technology Officer Summit in 2006 and "From Success to Significance" in 2005. International Rectifier contributed $100,000 and support for long-term technology roadmap development. With silicon carbide power devices on the brink of large-scale commercialization with a high potential to make a significant impact on future power electronics systems, CPES-RPI organized the first SiC Symposium in 2003, followed by the second one in 2005, bringing together industry experts, suppliers and users to facilitate the rapid development of SiC power devices.

Industry sponsored research

In addition to NSF core research, CPES researchers conduct a substantial number of research projects funded by industry fellowships and industry and government funded contracts that fit with the Center's strategic plan.

For the past 10 years, CPES has received $62 million overall in sponsored research funding. Since

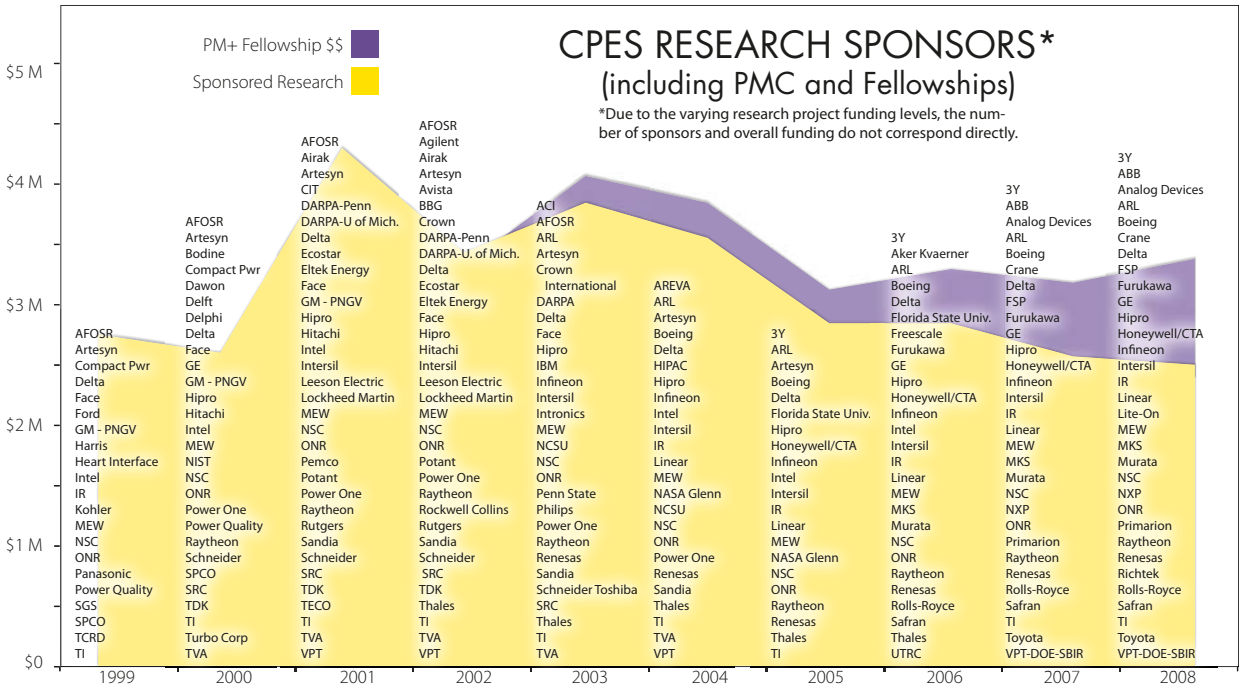
> "The Industrial Collaboration Program of CPES can be held up as a model for other Engineering Research Centers."
>
> —*2001 NSF Site Visit Report*

implementation of Principal Plus CPES partner membership in 2002, additional research funding through industrial fellowships and the power management mini-consortium has exceeded $3.4 million. Overall, CPES research collaboration with industry and government has been consistently strong, averaging $6-$7 million per year. Also, 28 CPES members sponsor graduate fellowships/scholarships.

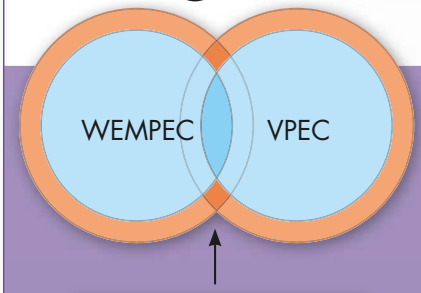
The nature of the sponsored research projects often involves collaboration among multiple campuses, such as the work on silicon carbide power devices sponsored by the Army Collaborative Technology Alliance, and electronic building block (PEBB) program sponsored by the Office of Naval Research. Overall, research efforts reflect the Center's expertise in the areas of power supplies for pulse power applications, advanced power systems for aircraft and naval ships, power system controllers for utility power, motor drives, and SiC device development and applications.

Academic collaborations

CPES has also strengthened its technical alliance with researchers outside CPES, offering an active faculty outreach program and incorporating the expertise of three research faculty members from other universities in the areas of integrating microprocessors with its power management solution and module reliability and failure analysis. Though the years, CPES has collaborated with many other power electronics faculty and students at 49 institutions globally via technical exchange visits, research projects, joint workshops, and joint publications.



CPES Industry Membership Program: Major Events



CPES MEMBERS

Two pre-existing industrial consortia at VT & UWM evolved into CPES

CPES IAB LEADERSHIP


K. Phillips


J. Steel


P. Thollot

IPPF FOR EASY IP ACCESS

VRM MINI-CONSORTIUM FOLDED INTO PRINCIPAL MEMBER PLUS

- Delta
- Hipro
- Hitachi
- IBM
- Intel
- Intersil
- National Semiconductor
- Power-One
- ST Microelectronics
- Texas Instruments
- TDK

IAB policies and procedures working group


R. Cuzner

Benchmarking working group


K. Phillips

SWOT analysis working group


P. Thollot

Reliability working group: M. Shaw

Champions working group: D. Adams

First Reliability Workshop
October 1999

CPES ANNUAL CONFERENCE

NSF SITE VISIT

INDUSTRY-STUDENT FORUM


IAB inaugural meeting: September 1998

Communications working group


J. Steel

Research review working group


G. Bruning


Second Reliability Workshop
March 2002

1998	1999	2000	2001	2002
YEAR 1	YEAR 2	YEAR 3	YEAR 4	

CPES short course offerings

IR supports CPES technology roadmap development initiative

Outreach Workshop
October 2006

NEW IAB LEADERSHIP

T. Burns

R. Zhang

PMC (FORMERLY VRM) TODAY

- AcBel Polytech, Inc.
- Analog Devices
- Crane Aerospace & Electronics
- Delta Electronics
- Emerson Network Power
- FSP Group, Inc.
- Hipro Electronics Co., Ltd.
- Infineon Technologies
- International Rectifier
- Intersil Corporation
- Linear Technology
- Lite-On Technology Corp.
- Monolithic Power Systems
- Murata Power Solutions
- National Semiconductor Corp.
- NXP Semiconductors
- Primarion
- Renesas Technology Corp.
- Richtek Technology Corp.
- Texas Instruments

Manufacturability and produceability working group

A. Kamp

IAB workshop: From Success to Significance
April 2005

CPES SiC Symposium
May 2003, June 2005

CTO Summit
April 2006

2003	2004	2005	2006	2007	2008
YEAR 5	YEAR 6	YEAR 7	YEAR 8	YEAR 9	YEAR 10

Infrastructure

CPES – a five-university ERC – is organized to effectively use assets and resources from diverse sources, including NSF, university cost sharing, industry consortium contributions, and research sponsors. The Center is structured to maximize communication and technology integration. Virginia Tech, the lead university, is responsible for the overall management and financial administration of the Center.

Fiscal resources are dispersed to partner institutions based on annual analysis the strategic plan, performance of the institution, and its expertise capabilities, expectations, and infrastructure support needs. NSF has provided more than $30 million over the past 10 years while an additional $62 million was received in sponsored research funds. Through the years, CPES has received strong industrial consortium support, from $400,000 in 1998 to more than $1.6 million in 2008. Center faculty have devoted much effort to establishing a basis of funding opportunities after the conclusion of NSF ERC award funding.

Leadership and management

CPES is administered as a sub-organization in the College of Engineering at the lead university, Virginia Tech. CPES director Fred Lee reports to the dean, and together they identify initiatives to enhance the position and contributions of the Center within the university, industry, and world. They receive counsel from the CPES Governing Board and the CPES Stakeholders Council. The Governing Board is composed of the engineering deans of all five partner universities, three representatives from the Industry Advisory Board, three representatives from the Scientific Advisory Board, the president of the Student Leadership Council, and the Center director.

Diversity

The CPES Strategic Plans for Diversity were initially developed with the input of the Governing Board, the Executive Committee, and Education Committee during the summer and fall of 2003. The Education Committee still plays an active role in updating and implementing both diversity programs by assisting in identifying pools of candidates for positions, strategies of recruitment, creating new programs targeted for participation by underrepresented groups, developing retention strategies, establishing benchmarks for progress within the Center and within CPES partner campuses, and monitoring the progress of each campus in achieving diversity goals. Campus directors and administrators are involved in these efforts when appropriate.

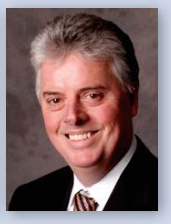
Two strategic diversity plans were developed: a plan for diversity of faculty and graduate students within the Center, and a plan for diversity in undergraduate and pre-college recruitment and program participation within the CPES Education Program. Both plans are implemented, revised, and examined as a single initiative within the Center's Governing Board, Stakeholders Committee, Leadership Team, Executive Committee, and Education Committee.

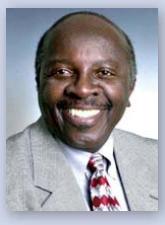
LEADERSHIP & MANAGEMENT

CPES Governing Board: Dean's Council


R. Benson, VT

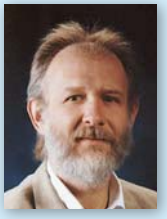

P. Peercy, UWM


A. Cramb, RPI


J. Monroe, NC A&T


R. Vasquez, UPRM

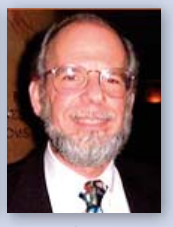

Center Director
F.C. Lee, VT


Center Co-Director
D. Boroyevich, VT

CPES Scientific Advisory Board


D. Blackburn, ret. NIST


R. Cavin, SRC


J. Kassakian, MIT

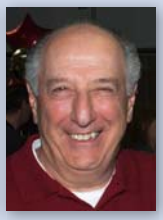

R. Steigerwald, ret. GE


A. Tucker, ret. ONR


J. Uceda, UPM, Spain

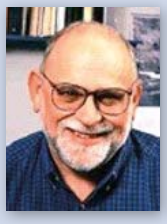
Industry Advisory Board


Chair
J. Steel


Co-Chair
K. Phillips


Secretary
P. Thollot

Campus Directors

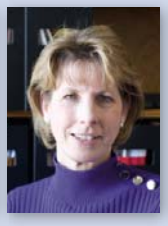

T. Lipo, UWM


T.P. Chow, RPI


M. Velez, UPRM


A. Homaifar, NC A&T


Director, Admin & Education/ Outreach
E. Tranter, VT


Financial Director
L. Long, VT


Industry Liaison
T. Shaw, VT


Student Leadership Council
C. Baisden, VT


Technical Director
F. Wang, VT

Facilities

Virginia Tech

The CPES power electronics laboratory at Virginia Tech, including offices, encompasses more than 19,000 square feet. With the aid of a $1-million DURIP grant, it has upgraded its high power electrical research capability for medium-voltage, megawatts power capability and has become one of the few universities with testing capability up to 1MVA, 4kV ac, and 15V dc.

In addition to the electrical research lab, the power electronics research space at Virginia Tech includes an integrated packaging lab and a 200-system computer lab, as well as a research library and large conference room with voice and video conferencing capabilities.

CPES is modifying four laboratory rooms at Virginia Tech as a "living lab" to incorporate emerging home/small office renewable energy technologies and power management systems. The conference room, library, kitchen, and laundry room will have a DC bus distribution system with automated source and load management powered by solar and wind energy interconnected with plug-in hybrid vehicles, battery subsystems, and the electrical grid.

The integrated packaging laboratory started with the equipment for such processes as thin film metal deposition, laser machining, etc., and now provides the latest in state-of-the art manufacturing in a unique, 4000-sq.-ft. facility. New additions include automated fluid dispensing for controlled adhesive and encapsulant application, and precision die and component bonding. The lab has been renovated to create 1,600-sq.-ft. of class 10,000 clean-room space.

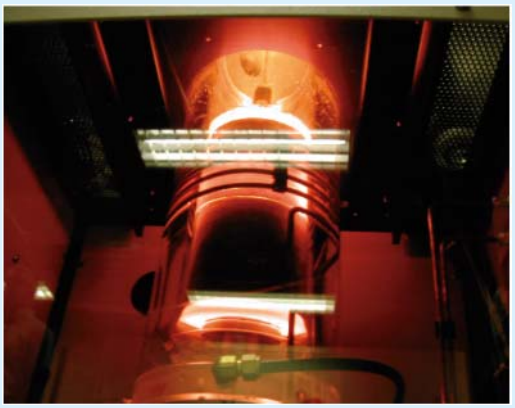
Integrated Packaging Lab at Virginia Tech

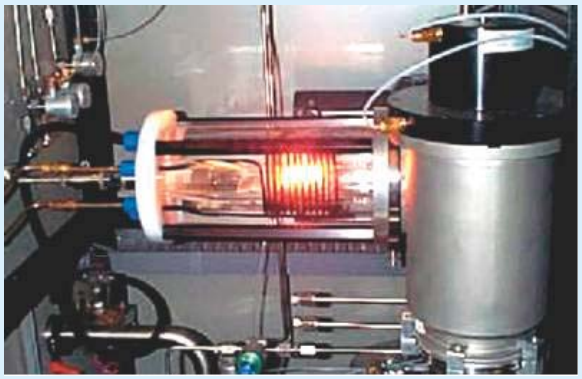
Rensselaer Polytechnic Institute

Rensselaer Polytechnic Institute – Rensselaer has well equipped facilities for materials characterization, processing, and device fabrication research. Key central facilities include a class 100 microelectronics clean room and an electron microprobe x-ray analysis. Key facilities in the CPES lab include a low-pressure cold-wall reactor dedicated to grow p-type and n-type SiC films and a vertical hotwall SiC reactor for thick, low-doped epitaxial films. RPI has all the design and simulation tools needed for device modeling and mask layout.

NSF-CPES support has provided for significant improvements to the main undergraduate education and research lab at RPI, the central lab for Electric Power Engineering. Equipment funding was especially crucial to complete the upgrade of lab equipment such as oscilloscopes, signal generators, and simulation software.

CPES also provided seed funding that led to the capture of a major grant from New York State grant to develop a renewable energy and distributed generation test-bed. The objective of this two-year, $1.25 million project is to develop a testbed for future electric grids relying heavily on renewable energies such as fuel cells, solar, etc. and distributed generation. Development began in 2007 and is expected to be complete in 2009.





University of Wisconsin-Madison

The power electronics laboratory is equipped for up to 60 graduate students to work on machines, motor drives, power electronics circuits, and machine and power electronics packaging research. A large range of test and measurement instrumentation for power electronics and machines research is also available, including an Envirotronics environmental chamber allowing testing from -73 to 177 degrees C.

CPES funding was combined with cost-shared capital equipment expenditures here to build three dynamometer test stands, critical to ongoing research to develop high-performance ac machines. Speed drives for dynamometer induction machines were donated by Rockwell Automation and Danfoss.

Facilities

University of Puerto Rico-Mayagüez

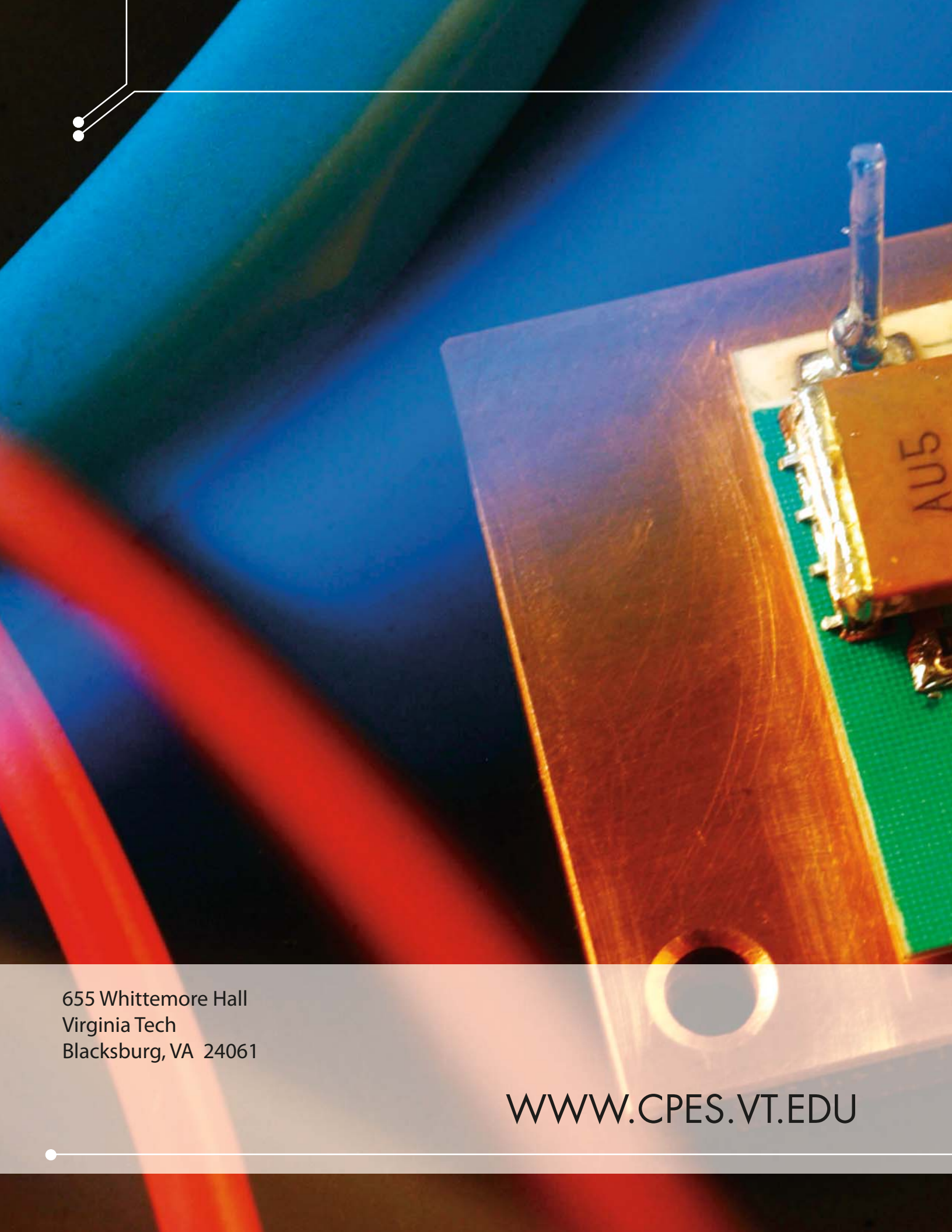
University of Puerto Rico-Mayagüez – At UPRM, the faculty has leveraged CPES resources with grants to improve laboratory infrastructure for research and education. Funds have upgraded computing resources and purchased a network analyzer, electronic loads and electronic instrumentation to support power electronic research activities.

UPRM facilities for CPES research include the power electronics laboratory, the electric energy processing systems laboratory, the integrated circuit design lab, and the rapid systems prototyping laboratory. In the last decade, over $1.3 million from federal and industrial funds have been invested to improve the infrastructure of CPES research facilities here. It is the leading Caribbean facility in electric energy research and in the education of researchers and professions in the energy field. The laboratory was established under an NSF grant (PECASE Award), and, as part of CPES, was expanded by the Major Research Instrumentation Award by NSF in 2002. This funding expanded existing facilities and built three testbeds: power electronics and drives, power quality, and transient studies. Recently power levels at the laboratory were increased to 37.5 kW. The shared state-of-the-art facilities made available through CPES partnering have been instrumental in ensuring success of proposals for associated funds, including Career Awards, equipment grants, and other large research initiatives.

North Carolina A&T State University

North Carolina A&T State University – NCA&T's power electronics laboratory, located in the Autonomous Control and Information Technology Engineering Center, is almost 3,200 sq. ft. The self-sufficient NASA-ACITE laboratory incorporates its own domain and Internet servers as well as a video conferencing room for collaboration with other universities. The center also houses a state-of-the-art, cross platform computing environment. Besides developing this lab, NCA&T has begun steps to equip a teaching lab for power electronics.

CPES continues to have a vital impact on the educational infrastructure by enhancing the curriculum at the undergraduate and graduate levels and affecting the shape of research through inter-university collaborations. NCA&T also added a power electronics professor in fall 2007.



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Virginia Tech
Blacksburg, VA 24061

WWW.CPES.VT.EDU