# Advanced Semiconductor Device and Topology for High Power Current Source Converter

Zhenxue Xu

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Alex Q. Huang, Chairman
Dushan Boroyevich
Jason Lai
Yilu Liu
Guo Quan Lu

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# ADVANCED SEMICONDUCTOR DEVICE AND TOPOLOGY FOR HIGH POWER CURRENT SOURCE CONVERTER

By

Zhenxue Xu

Alex Q. Huang, Chairman

Electrical Engineering

(ABSTRACT)

This dissertation presents the analysis and development of an innovative semiconductor device and topology for the high power current source converter (CSC).

The CSC is very attractive in high power applications due to its lower output dv/dt, easy regeneration capability and implicit short-circuit protection. Traditionally, either a symmetrical gate turn-off (GTO) thyritor or an asymmetrical GTO in series with a diode is used as the power switch in the CSC. Since the GTO has a lower switching speed and requires a complicated gate driver, the symmetrical GTO based CSC usually has low dynamic response speed and low efficiency. To achieve high power rating, fast dynamic response speed and low harmonics, an advanced semiconductor device and topology are needed for the CSC.

Based on symmetrical GTO and power MOSFET technologies, a symmetrical emitter turn-off (ETO) thyristor is developed that shows superior switching performance, high power rating and reverse voltage blocking capability. The on-state characteristics, forced turn-on characteristics, forced turn-off characteristics and the load-commutated characteristics are studied. Test results show that although the load-commutation loss is high, the developed symmetrical ETO is suitable for use in high power CSC due to its low conduction loss, fast switching speed and reverse voltage blocking capability.

The snubberless turn-on capability is preferred for a semiconductor device in a power conversion system, and can be achieved for devices with forward biased safe operation area (FBSOA). The FBSOA of the ETO is investigated and experimentally demonstrated. The ETO device has excellent FBSOA due to the negative feedback provided by the emitter switch. However, the FBSOA for a large area ETO is poor. A new ETO concept is therefore proposed for future development in order to demonstrate the FBSOA over a large area device.

To improve the turn-on performance of the large area ETO, a novel concept, named the transistor-mode turn-on, is proposed and studied. During the transistor-mode turn-on process, the ETO behaves like a transistor instead of a thyristor. Without a snubber, the transistor-mode turn-on for the ETO is hard to achieve. Through the selection of a proper gate drive and di/dt snubber, the transistor-mode turn-on can be implemented, and the turn-on performance for the ETO can be dramatically improved.

To increase the power rating of the CSC without degrading the utilization of power semiconductor devices, a novel multilevel CSC, named the parallel-cell multilevel CSC, is proposed. Based on a six-switch CSC cell, the parallel-cell multilevel CSC has the advantages of high power rating, low harmonics, fast dynamic response and modularity. Therefore, it is very suitable for high power applications. The power stage design, modeling, control and switching modulation scheme for a parallel-cell multilevel CSC based static var compensator (STATCOM) are analyzed and verified through simulation.

To my wife, Lina; my son, Brian Zhongqi; my daughter, Liwen;

my parents,

Yongcheng Xu and

Xiuzhi Wang;

and

my mother-in-law,

Fengqin Chen

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# Chapter 1. Introduction

## 1.1. Background and Literature Review

A power semiconductor switch (power semiconductor device) is a component that is controlled to either conduct a current when it is commanded ON or block a voltage when it is commanded OFF. This change of conductivity is made possible in a semiconductor by specially arranged device structures that control the carrier transportation. The time that it takes to change the conductivity is also reduced to the microsecond level as compared to the millisecond level of a mechanical switch. By employing this kind of switch, a properly designed electrical system can control the flow of electric energy, shaping the electricity into desired forms [A1].

If a power semiconductor device can block forward voltage as well as the reverse voltage during the OFF state, it is defined as a symmetrical device. On the other hand, a power semiconductor device that can only block the forward voltage during the OFF state is defined as an asymmetrical device. Most of the semiconductor devices can only conduct forward current during the ON state [A1-A2]. Therefore, the symmetrical device has three operation states: forward conduction mode, forward blocking mode and reverse blocking mode, as shown in Fig. 1.1(a). For an asymmetrical device, only two operation modes exist: forward conduction mode and forward blocking mode, as shown in Fig. 1.1(b).

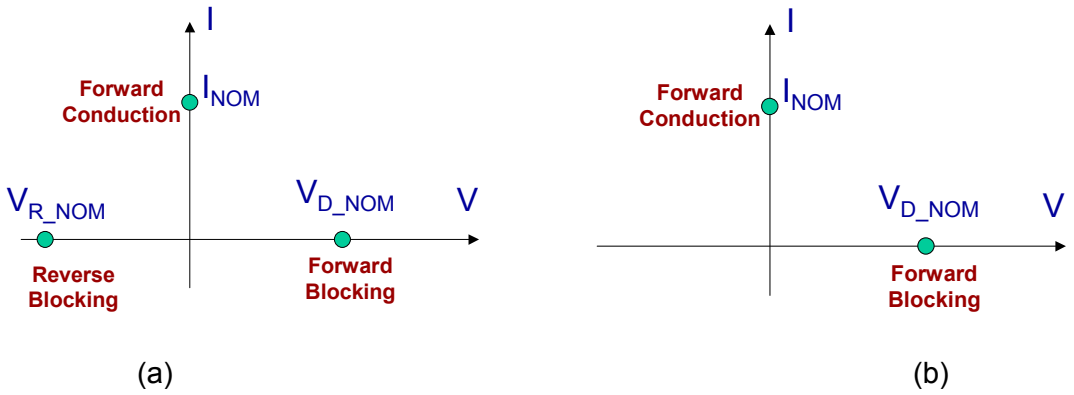



Fig. 1.1. Device operation states for (a) symmetrical device and (b) asymmetrical device.

A typical turn-on operation of a power semiconductor switch changes its operation state from its forward or reverse blocking mode to its forward conduction mode. Changing a device's operation state from forward blocking mode to forward conduction mode is defined as a forced turn-on, while changing a device's operation state from reverse blocking mode to forward conduction mode is defined as a load-commutated turn-on. The turn-on trajectory is determined by circuits rather than by the device itself. During the forced turn-on transition, the switch may simultaneously undego both high voltage and high current, as represented by curve (a) in Fig. 1.2(a), where the device's voltage stays constant while its current increases until it hits the device's nominal current level. This kind of turn-on, also called a snubberless turn-on, happens in most power converters. So the device stress is high in this case. The current overshoot occurs due to the reverse-recovery of an associated diode (or a switch). With a snubber circuit, the voltage-current trajectory can be shaped as curve (b) shown in Fig. 1.2(a), where the device voltage collapses before the current increases to the normal value, resulting in dramatically reduced device stress [A1]. During the load-commutated turn-on transition,

the device begins to conduct current only after the device voltage becomes positive, as shown in Fig. 1.2(b). Therefore, the device stress is usually low in this case.

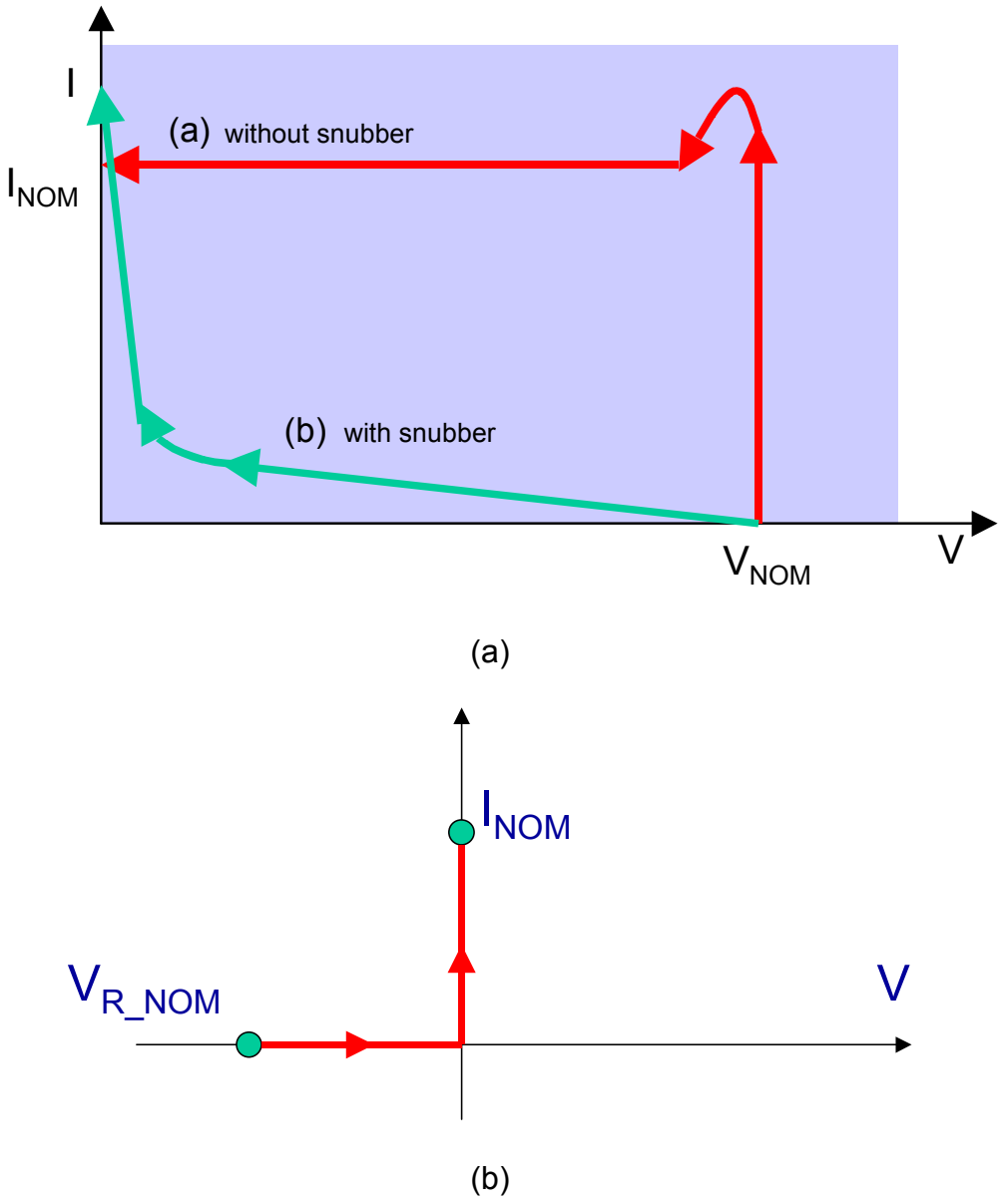



Fig. 1.2. I-V trajectories of a device for (a) forced turn-on with or without a snubber circuit and (b) load-commutated turn-on.

The forward biased safe operation area (FBSOA) defines a maximum forward voltage-current region in which the device can be commanded to operate with simultaneous high voltage and current, as shown by the shaded area in Fig. 1.3. The device current can be controlled through its gate (or base), and the length of the operation is only restricted by its thermal limitation [A4]. Devices with FBSOA normally have an active region in which the device current is determined by the control signal level, as shown in Fig. 1.3.

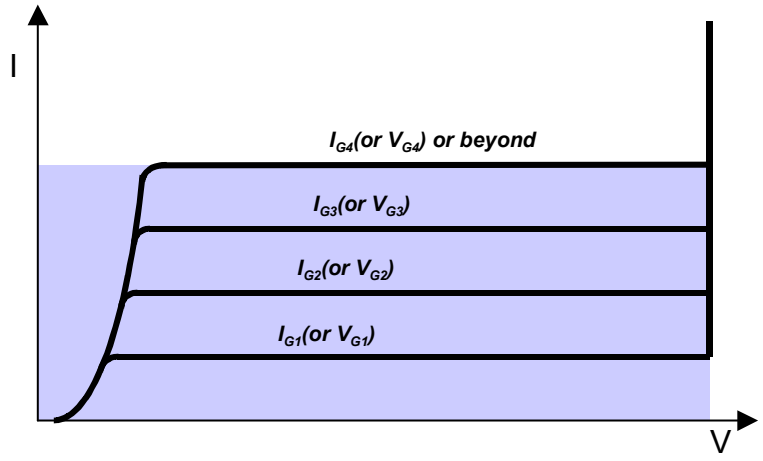



Fig. 1.3. Forward I-V characteristics of a device and its FBSOA (shaded area) definition.

A device with FBSOA (such as a MOSFET) normally has the self-current-limiting capability, the ability for a switch to limit its maximum current regardless of the voltage applied, and its typical I-V curve is shown as curve (a) in Fig. 1.4. In contrast, a device without FBSOA (such as a GTO) cannot self-limit its current, and its typical I-V curve is shown as curve (b) in Fig. 1.4. For a device with good FBSOA, hence the self-current limiting capability, the turn-on di/dt can be controlled through the gate, and most importantly no current crowding occurs during the turn-on transient. Therefore, snubberless turn-on can be applied to these devices. On the other hand, for a device without FBSOA, the turn-on di/dt is uncontrollable, and current crowding may happen in

a localized area. This is particularly true for large area devices; therefore, a snubberless turn-on is not possible in these devices, and an external snubber circuit needs to be used to avoid current-crowding problems [A1]. The snubber circuit will increase a system's component count, size and cost. Therefore, a device with good FBSOA is preferred in a power conversion system.

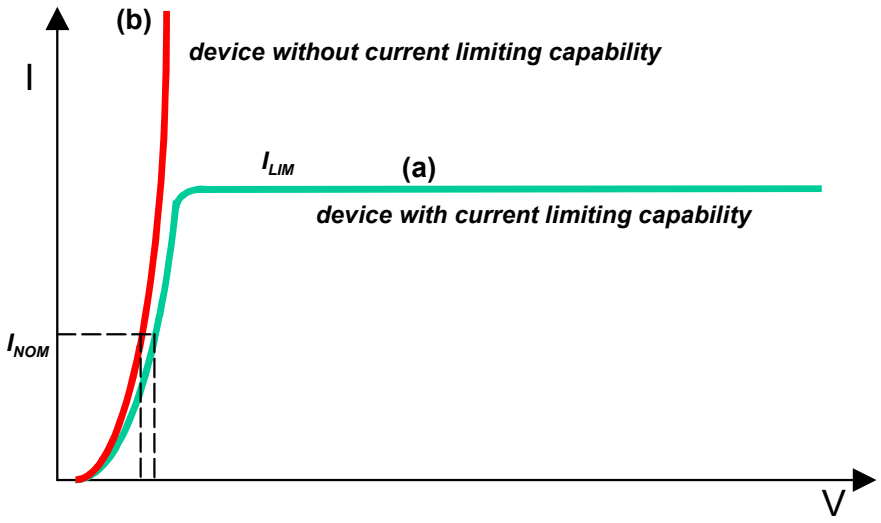
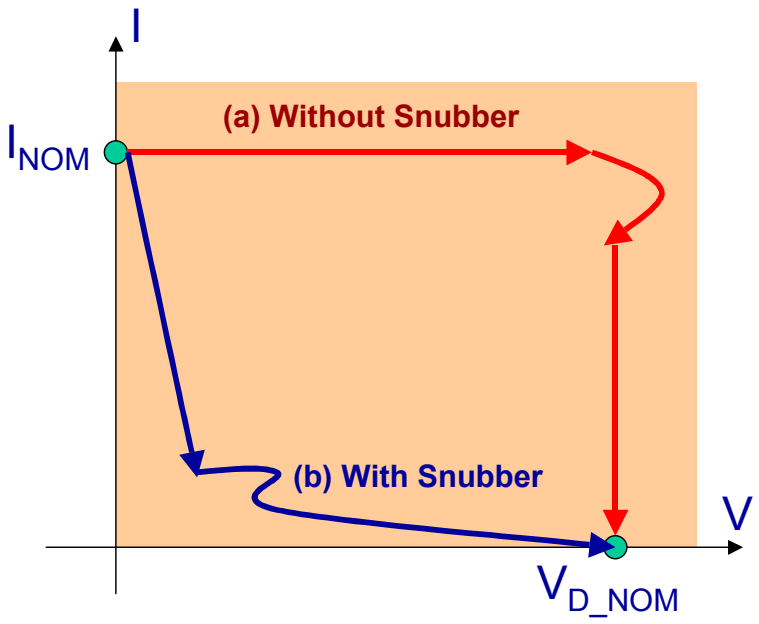



Fig. 1.4. Forward I-V characteristics of two type of devices with / without self-current limiting capability.

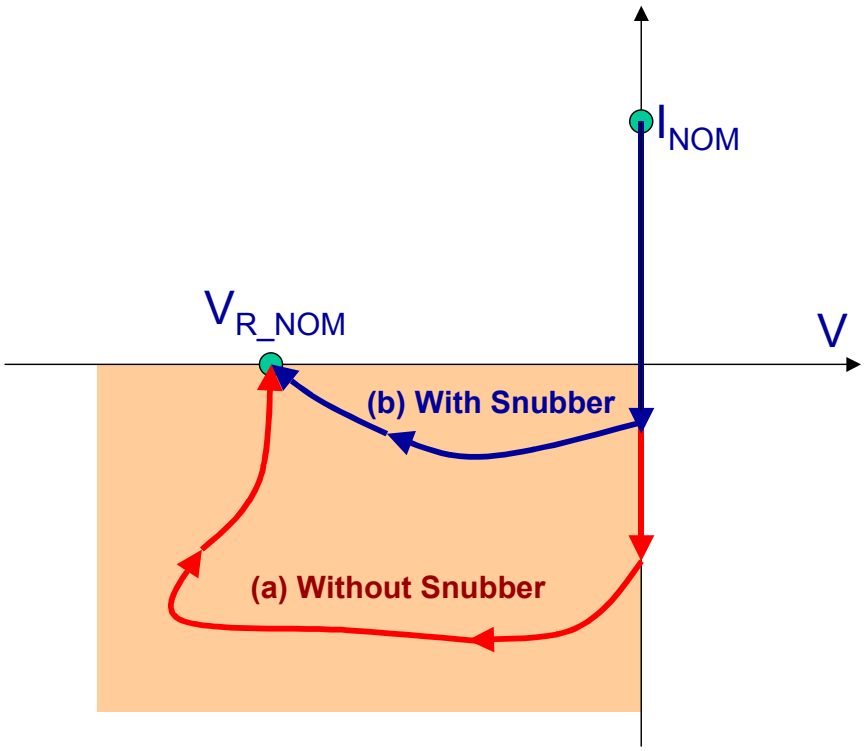
A typical turn-off operation of a power semiconductor switch changes its operation state from forward conduction mode to forward or reverse blocking mode. Changing a device's operation state from forward conduction mode to forward blocking mode is defined as a forced turn-off, while changing a device's operation state from forward conduction mode to reverse blocking mode is defined as a load-commutated turn-off. During the forced turn-off transition, the switch may simultaneously undergo both high voltage and high current, as represented by curve (a) in Fig. 1.5(a), where the device's current stays constant while its voltage increases. Once the device voltage reaches its

nominal value, the device current begins to decrease. So the device stress is high in this case. The voltage overshoot occurs due to the di/dt applied to the stray inductance in the current-commutation loop. With a snubber circuit, the voltage-current trajectory can be shaped as shown by curve (b) in Fig. 1.5(a), where the device current decreases before the device voltage increases to the normal value, resulting in dramatically reduced device stress.

During the load-commutated turn-off transition, the device current begins to decrease first while the voltage does not change much until the device current becomes negative. When the negative device current increases, the negative device voltage also increases. The negative device current begins to decrease once it reaches its peak value, resulting in a negative over-voltage as well as high stress on the device, as shown by curve (a) in Fig. 1.5(b). Similarly, with a snubber circuit, the voltage-current trajectory can be shaped as shown by curve (b) in Fig. 1.5(b) with much lower device stress.




(a)




(b)

Fig. 1.5. I-V trajectories of a device for (a) forced turn-off with or without snubber circuit and (b) load-commutated turn-off with or without snubber.

The reverse biased safe operation area (RBSOA) is defined as the maximum voltage and current boundary within which the device can turn off without destructive failure [C8]. Obviously, a device's RBSOA should be larger than all its possible turn-off I-V trajectories. A device without sufficiently large RBSOA needs an external circuit (snubber) to reduce the size of its turn-off I-V trajectory in order to ensure safe turn-off operation.

The switching operation conducted without the help of a snubber is called snubberless switching, while the process utilizing a snubber is called snubbered switching. Since a

snubber increases the system's component count, hence its size and cost, the snubberless switching capability for a device is preferred.

There are two basic topologies for DC/AC energy transfer: the voltage source converter (VSC) and the current source converter (CSC). In a VSC, the dc voltage always has one polarity, and the power reversal takes place through reversing the direction of the dc current. In contrast, the direct current of a CSC always has one polarity, while the power reversal happens when the dc voltage polarity is reversed. Since the DC voltage does not reverse in a VSC, an asymmetrical device can be used. On the other hand, the device in a CSC will undergo reverse voltage, so a symmetrical device is needed to block the forward voltage as well as the reverse voltage [A3].

### 1.1.1. Power Semiconductor Devices

Invented in the 1950s, silicon controlled rectifier (SCR) was the first power semiconductor switch to be put into use [A2]. The SCR is a latch-up device with only two stable states: ON and OFF. It does not have FBSOA. The SCR has a good trade-off between its forward voltage drop and blocking voltage due to the strong conductivity modulation provided by the injections of both electrons and holes. With a simple structure, the size of a single SCR can be easily increased to a six-inch diameter in order to increase the current rating of the device. Based on a six-inch silicon wafer, 8.0-kA/10.0-kV SCRs are commercially available. The SCR can also block reverse voltage due to its symmetrical structure. However, SCRs cannot be turned off through their gate controls, and instead must use a load-commutated turn-off, such as that shown in Fig. 1.5(b).

Since the SCR cannot be turned off through the gate, the gate turn-off (GTO) thyristor [B12] with forced turn-off controllability was subsequently developed. The basic structure of a GTO is similar to that of an SCR, except that many gate fingers are placed around the cathode of the GTO. Because of the gate control, the latch-up mechanism can be broken during the turn-off transition, resulting in full gate-control capability. For a fully controllable device, the GTO has the highest power rating and the best trade-off between the blocking voltage and the conduction loss. However, GTOs' dynamic performance is poor. Since the GTO lacks FBSOA and has poor RBSOA, a dv/dt snubber is required during turn-off, and a di/dt snubber is required during turn-on. As a current-driven device, it also requires a complicated gate driver, resulting in high gate-driver loss. GTOs can be made to be either symmetrical or asymmetrical.

The bipolar junction transistor (BJT) [C9] is the earliest controllable device, and served as the workhorse device for power-conversion applications up until two decades ago. With fairly good FBSOA and RBSOA, its dynamic performance and switching speed are better than thaose of the GTO. However, the trade-off between its blocking voltage and its forward voltage drop is poor, and so no power BJT with a good forward voltage drop is designed beyond 1.5 kV. The control circuit is usually complicated and lossy since the BJT is a current-driven device. The RBSOA and FBSOA are also significantly limited by the second breakdown of a power BJT [C3]. BJTs are asymmetrical devices.

The power MOSFET [C5] is a voltage-controlled device with excellent dynamic performance due to its majority-carrier current-conduction mechanism. Except that its power rating is limited by the resistive conduction loss, the power MOSFET has become a nearly perfect power switch for applications below 600 V due to its fast switching speed, voltage control and excellent FBSOA and RBSOA. Snubberless turn-on and turn-off can be achieved in MOSFETs. The MOSFET is also an asymmetrical device.

Based on the idea of a MOS-controlled BJT, the insulated gate bipolar transistor (IGBT) [C10] was developed. The IGBT fundamentally changes the BJT's current control into voltage control while maintaining the BJT's advantages. IGBTs have excellent RBSOA and FBSOA. In addition, the use of a wide-base PNP transistor in the IGBT structure results in a much better conductivity modulation effect than is achieved with a conventional BJT; thus, the voltage rating of the IGBT can be pushed toward that of the GTO. To date, IGBTs have become the best device for applications in the range of 600 V to 3000 V. Most commercial IGBTs are asymmetrical device although theoretically a symmetrical device can also be developed.

For high power applications, traditionally, a high power SCR is used as the symmetrical power semiconductor device for a CSC [3]. Since the SCR does not have the forced turn-off capability, the operation of the thyristor in a CSC is totally load-commutated at the line frequency. Due to its low switching frequency, its dynamic response speed is low and a large filter is needed to attenuate the harmonics.

The symmetrical GTO with capabilities of both forced turn-off and reverse voltage blocking, was then introduced to the market [B1, B2, B6]. Using a symmetrical GTO device, the Sinusoidal Pulse Width Modulation (SPWM) scheme [A6] can be used to modulate device switching. Compared to the SCR, the switching frequency for a symmetrical GTO is higher. Therefore, the dynamic response speed and output current harmonics are greatly improved for a symmetrical GTO based CSC.

However, the GTO has several disadvantages [B7-B9]. During the turn-off transient, the P-N-P-N four-layer structure causes inhomogeneous transient current distribution that results in a small RBSOA. A dv/dt snubber is needed to ensure that the GTO operates within the RBSOA during the turn-off process. During the turn-on transient, the P-N-P-N four-layer structure latches quickly and causes a current-crowding problem. Therefore, a turn-on di/dt limiting snubber is demanded. Furthermore, since the GTO is a current-controlled device, its gate driver is bulky and dissipates hundreds of watts in a typical application. The large parasitic inductance in GTO gate drivers usually result in a very long storage time and a turn-off gain of between three and five. The operation frequency of the GTO is therefore limited to less than 500 Hz.

The dominant position of GTOs in megawatt applications is being challenged by high power IGBTs that offer higher speed, a larger SOA and easier controls [C2, C6, C7, C9]. However, the conduction loss of the high power IGBTs is still much higher than that of the GTO. The IGBT's high conduction loss results in lower system efficiency.

Furthermore, since no symmetrical IGBTs are commercially available now, the IGBT based CSC is not feasible. This situation will continue into the near future.

On the other hand, a lot of efforts have recently gone into improving the switching performance of the GTO-oriented devices. One type of GTO-based semiconductor device with a wider RBSOA is the Integrated Gate Commutated Thyristor (IGCT) [D1, D4, D8]. With dramatically improved turn-off performance, the IGCT will help to maintain the domination of GTO technology in high power areas. Symmetrical GCTs have also been introduced to the market for industrial drive applications [D1, D8]. In an IGCT based CSC, the dv/dt snubber is dramtically reduced due to the improved turn-off performance of the IGCT [D8]. However, the IGCT does not have an FBSOA, so a di/dt snubber is still needed. The fairly high gate drive power is one of the limitations for high-frequency switching. Besides, the cost of the symmetrical IGCT is high due to its specially designed device structure.

The Emitter Turn-off (ETO) Thyristor [K1-K4] is another type of GTO based superior high power semiconductor device. Based on the mature technology of the GTO and power MOSFET, the ETO provides a low-cost and advantageous solution to megawatt applications. Theoretical analysis and experimental results suggest that the ETO has the combined advantages of both the GTO and the IGBT: GTOs' high voltage and current ratings and low forward voltage drop; IGBTs' voltage control, high switching speed, and wide RBSOA. High power asymmetrical ETOs with current ratings of 1 kA to 4 kA, and voltage ratings of 1 kV to 6 kV have already been demonstrated [K1-K8].

In this dissertation, a novel semiconductor device, the symmetrical ETO with good RBSOA and FBSOA, is developed and characterized, and its application in the high-power CSC is investigated.

### 1.1.2. Current Source Converter

With the advance of power semiconductor devices, more and more power electronics systems are used in high power utility and industry applications. The VSC is the most popular topology due to its simple structure, high efficiency, fast dynamic response speed and easy control [A3]. However, VSC has several disadvantages such as high dv/dt in the output voltage, no current-limiting capability in shoot-through failure, and a single direction of power flow without an easy regeneration function.

The dual circuit of the VSC is the CSC. The DC-link for a CSC is a current source, as opposed to the voltage source used in the VSC. The CSC provides the advantages of low dv/dt in the output voltage due to the output filter capacitor. The fault current during shoot-through failure is limited by the DC-link inductor, and so the over-current protection is easier for the CSC. The polarity of voltage across the DC-link inductor can be easily changed by a phase-controlled front-end rectifier, implementing the regeneration capability with less effort. Especially for high power applications, these advantages overcome the disadvantages of higher conduction loss and more complicated control and the CSC topology becomes a competitive candidate [A3, A6, E3, I5].

For high power applications, such as flexible AC transmission systems (FACTS) devices and energy storage systems, power converters with high voltage, high current, low harmonics and fast dynamic response speed are required [A3, J6]. With traditional three-level CSC topology, power semiconductor devices in series or parallel connection are needed to achieve high voltage rating. Complicated balancing circuits are required for the proper operation of the series or parallel devices. Device derating is usually needed. The switching frequency for high power semiconductor devices is usually low, since it is limited by the switching loss in high power applications. Therefore, the harmonics in the output voltage and current are high and the dynamic response is slow. To limit the harmonics within a standard, an external filter is usually needed, and this addition will further reduce the dynamic response speed. Therefore, paralleling converters instead of devices is preferred for high power applications [G1-G5]. To further increase the power rating and to reduce harmonics, multilevel converters based on PWM converter cells are developed. The multilevel converter is a trend for high power applications [H1, H3, H7].

For multilevel CSC topology, there are two kinds of topologies. In one, the multiple CSC [I1, I5], several CSCs are in parallel connection and thus share the same DC-link current through current-sharing inductors and proper control, as shown in Fig. 1.6. The capacity of the multiple CSC can be increased, and the harmonics contained in the output voltage and current waveforms can be reduced through phase-shift PWM control among parallel CSCs. However, to ensure DC current sharing and to prevent the circulating current among the parallel CSCs, additional current-sharing components and complicated control must be applied [G5-G7].

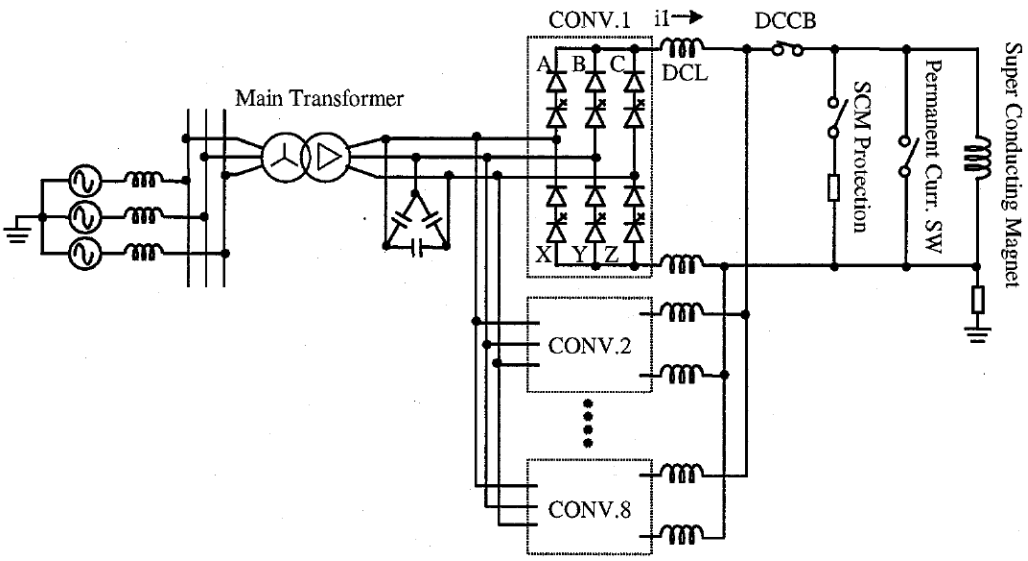
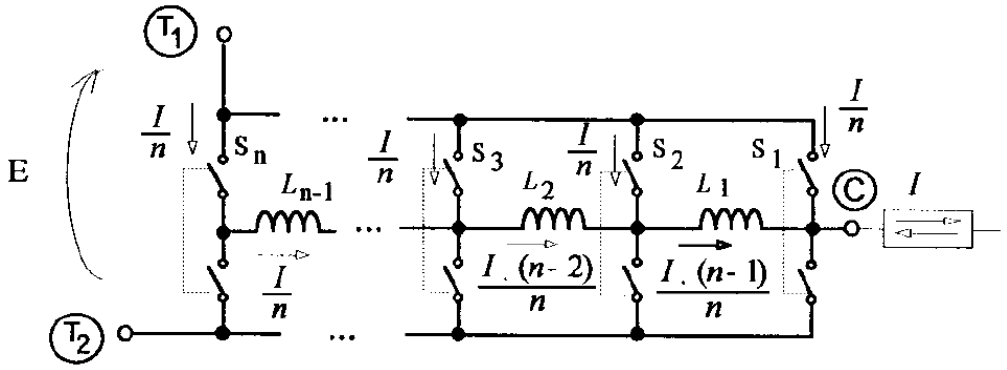
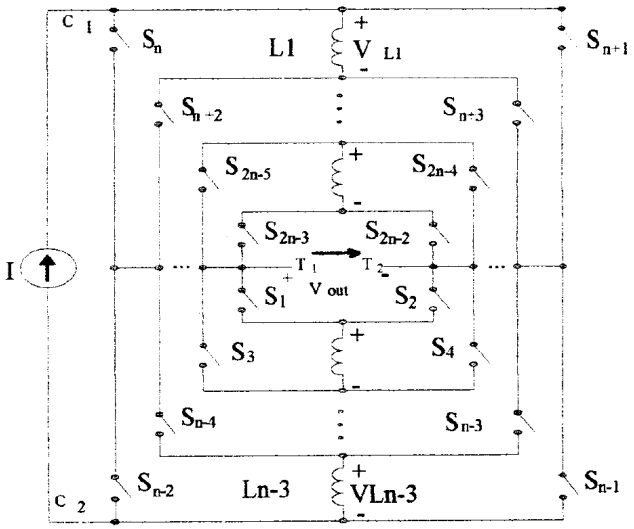



Fig. 1.6. Topology for a multiple CSC based energy storage system [I1].

Another method for achieving the low switching frequency and low harmonic distortion for high-power applications is to apply a generalized current multilevel cell (see Fig. 1.7) to form multilevel CSCs [I2-I4]. Many smaller current-sharing inductors are employed to ensure current sharing among the different branches. The multilevel output current is achieved through proper control of the active switches. In this version of multilevel CSC, the current sharing between active switches relies on their on-state voltages, and thus complicated control is also needed. In this topology, the modular design is also not used due to its complicated structure and control.




(a)




(b)

Fig. 1.7. Structure of a generalized current multilevel cell [I2] and (b) the generic multilevel current cell based multilevel CSC [I3].

To solve the problems of the existing multilevel CSCs, a novel multilevel CSC topology, named the parallel-cell multilevel CSC, is proposed and investigated in this dissertation.

## 1.2. Dissertation Outline and Major Results

This dissertation presents the analysis and development of an advanced semiconductor device and topology for high CSCs.

### 1.2.1. An Advanced Symmetrical Semiconductor Device-The Symmetrical ETO

In this dissertation, the symmetrical ETO is developed and characterized for the first time. The on-state characteristics, forced turn-on characteristics, forced turn-off characteristics as well as the load-commutated turn-off characteristics for the symmetrical ETO are characterized. Test results show that although the load-commutated loss is high, the symmetrical ETO is still suitable for use in the high power CSC due to its low conduction loss, fast switching speed, large RBSOA and reverse blocking capability.

### 1.2.2. Investigation of Snubberless Turn-on for Emitter Turn-Off Thyristor

The FBSOA allows snubberless turn-on, and is therefore preferred for a semiconductor device. The FBSOA of the ETO is studied and experimentally demonstrated. The FBSOA of a large area ETO is also investigated. It is found that The FBSOA is not realizable in the current generation of large area ETOs. A new ETO concept is then proposed for future development. Another new method for achieving a snubberless turn-on, named the transistor mode turn-on, is proposed and studied. Finally, with proper gate drive and di/dt snubber, the improved turn-on performance of the ETO is analyzed and experimentally demonstrated.

### 1.2.3. Power Stage Design of the ETO Based CSC

The power stage design for the ETO based CSC is investigated. The switching performance of the symmetrical ETO in a CSC is analyzed, and the snubber circuit design is studied. To improve the load-commutated turn-off performance of a symmetrical ETO, a novel gate-control scheme with a gate delay time for the on-coming device is proposed and evaluated. Test results show that the delay time has a limited effect on the reverse-recovery performance of the off-going device.

### 1.2.4. A Novel Multilevel CSC—the Parallel-Cell Multilevel CSC

A CSC with high power rating, low harmonics and a modular design is preferred for modern high power applications, such as FACTS devices and energy storage systems. To achieve these merits, a novel multilevel CSC, named the parallel-cell multilevel CSC, is proposed. The operation principle, modeling, control and switching modulation schemes for the parallel-cell multilevel CSC are analyzed and verified through simulation. Based on the six-switch CSC cell, the parallel-cell multilevel CSC has the advantages of high power rating, low harmonics, fast dynamic response and modular design. Therefore, it is very suitable for high power applications.

### 1.2.5. Comparison of the Multilevel CSC and the VSC in STATCOM Applications

In Static Var Compensation (STATCOM) applications, the performance of the parallel-cell multilevel CSC is compared with the stat-of-the-art multilevel VSC topology-the cascaded multilevel VSC. Compared with the cascaded multilevel VSC based STATCOM, the parallel-cell multilevel CSC based STATCOM has lower harmonics, an easier start-up process, lower power rating and comparable dynamic response speed using the same power semiconductor devices.

# Chapter 2. An Advanced Symmetrical Semiconductor Device—The Symmetrical ETO

An advanced symmetrical device, the symmetrical ETO, is proposed and developed. The operation principle is analyzed. The on-state characteristics, forced turn-on characteristics, forced turn-off characteristics as well as the load-commutated turn-off characteristics for the symmetrical ETO are characterized.

## 2.1. Operation Principle of the Symmetrical ETO

According to GTO theory [D2], the hard-driven technique can substantially improve the RBSOA and speed of the GTO. Under the hard-driven turn-off condition, the entire cathode current is quickly commutated to its gate before the anode voltage starts to rise. In this way, the thyristor latch-up is interrupted, and the whole turn-off process is like that of an open-base PNP transistor. This process is also called unity-gain turn-off. During this transition, the device I-V curve changes from curve (a) to curve (b), as shown in Fig. 2.1, resulting in a dynamic current limiting capability for the GTO cell, and hence a uniform current distribution and wide RBSOA.

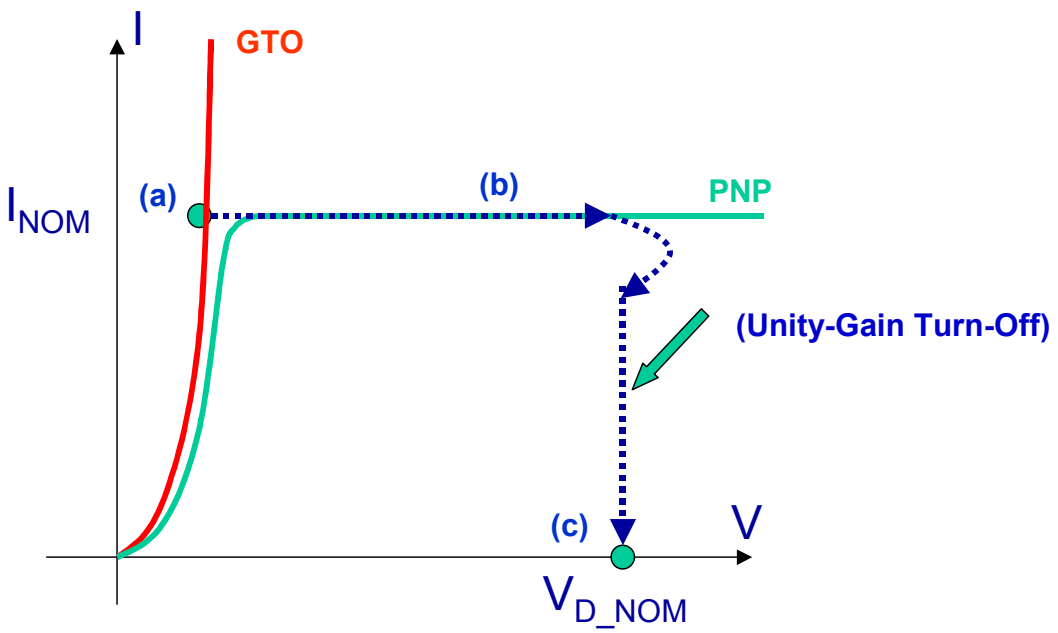
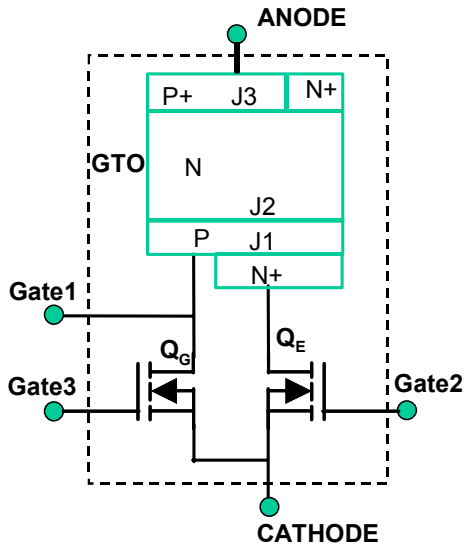
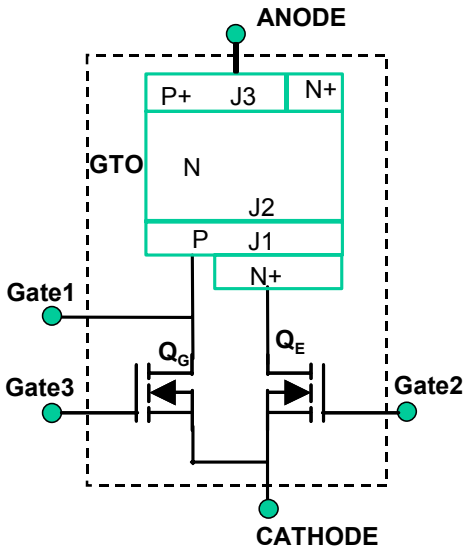



Fig. 2.1. Forward I-V characteristics of the ETO during a forced turn-off transition.

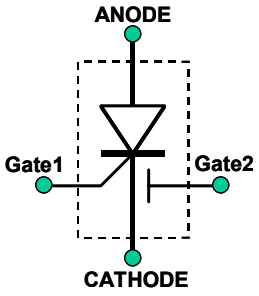
The ETO is an MOS-GTO hybrid device that makes the GTO operate under the hard-driven condition [K1-K4]. High power asymmetrical ETOs with current ratings of 1-kA to 4-kA, and voltage ratings of 1-kV to 6-kV have already been demonstrated [K1-K8]. The equivalent circuit of the asymmetrical ETO is shown in Fig. 2.2 (a). An asymmetrical ETO is realized by using an asymmetrical GTO in series with an emitter switch $Q_E$ and by connecting gate switch $Q_G$ to the GTO's gate. During the forced turn-off transient, $Q_E$ is turned off and $Q_G$ is turned on. The GTO's cathode current is totally bypassed via switch $Q_G$ before the anode voltage begins to rise. In this way, the thyristor latch-up is broken, and the ETO is turned off under a unity turn-off gain condition, resulting in snubberless turn-off capability. It should be stressed that the turn-off is a voltage-controlled process. So the gate driver of the ETO is very compact and dissipates much less power. During the turn-on transient, $Q_E$ is turned on and $Q_G$ is turned off. Thanks to the tightly integrated gate driver, a high current pulse plus a DC current are injected into the GTO gate to reduce the turn-on delay time and improve the turn-on di/dt rating.



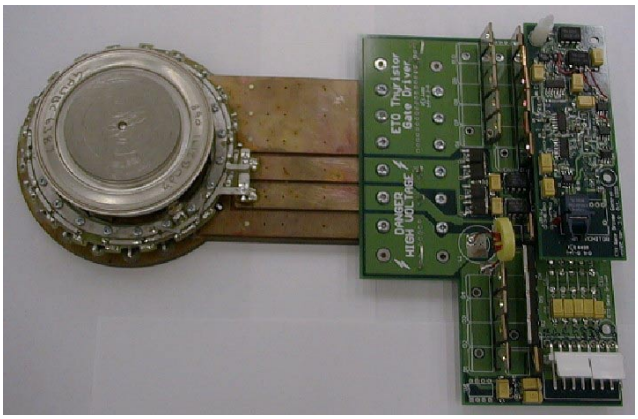

(a)




(b)




(C)

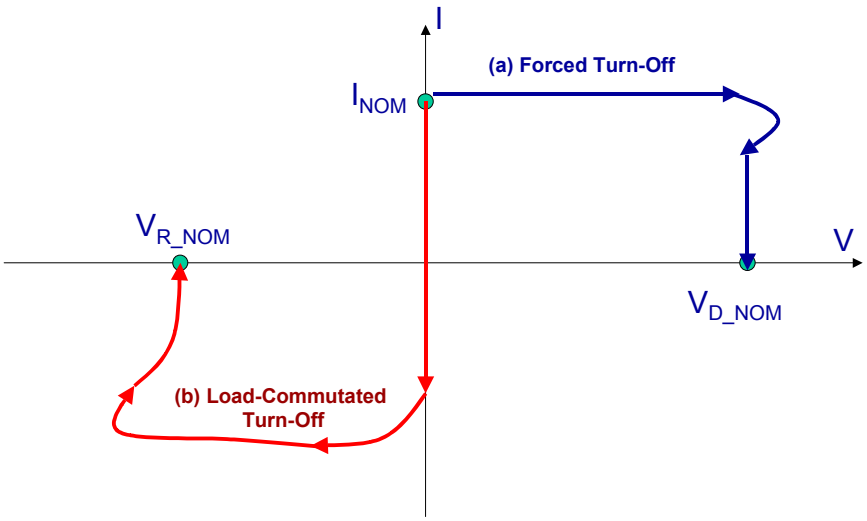


(d)

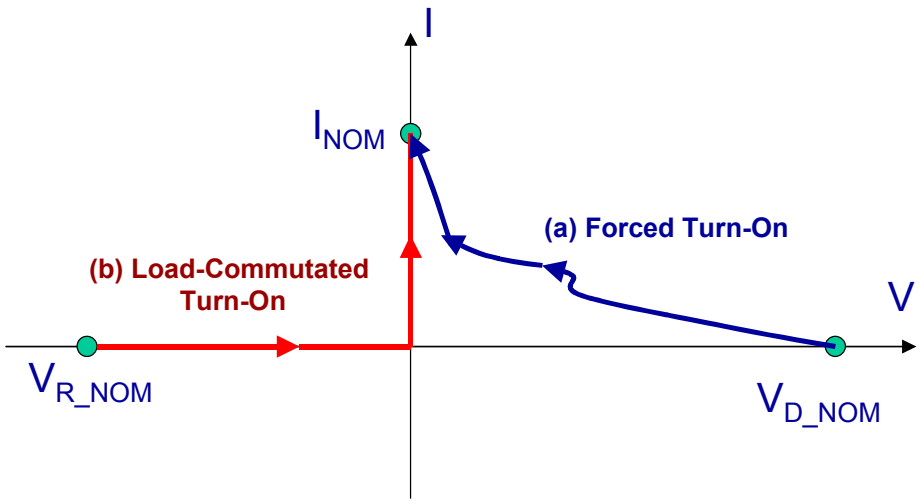
Fig. 2.2. (a) Asymmetrical ETO equivalent circuit, (b) symmetrical ETO equivalent circuit, (c) circuit symbol and (d) a picture of 1-kA/4.5-kV symmetrical ETO with its gate driver.

With superior forced turn-off capability as well as improved turn-on performance, the asymmetrical ETO is a good candidate for use in a VSC where the device always has a positive voltage stress. However, the asymmetrical ETO usually has a low reverse voltage blocking rating (about 20 V) that is dictated by the breakdown voltage of junction $J_1$ (see Fig. 2.2 (a)), since junction $J_3$ (see Fig. 2.2 (a)) cannot block reverse voltage with anode-shorting structure in the asymmetrical ETO. Therefore, the asymmetrical ETO cannot be used in a circuit that requires reverse voltage-blocking capability, such as a CSC.

By replacing the asymmetrical GTO in an asymmetrical ETO with a symmetrical GTO, the proposed symmetrical ETO can be formed as shown in Fig. 2.2(b). Compared to the asymmetrical ETO, the anode side of the symmetrical ETO has no N+ region, which would short junction $J_3$, so it can block reverse voltage. Keeping both the superior forced turn-off performance and the improved turn-on performance, the symmetrical ETO is suitable to use in a CSC due to its reverse voltage-blocking capability. The symmetrical ETO is a two-quadrant device, and its operation trajectories are shown in Fig. 2.3.



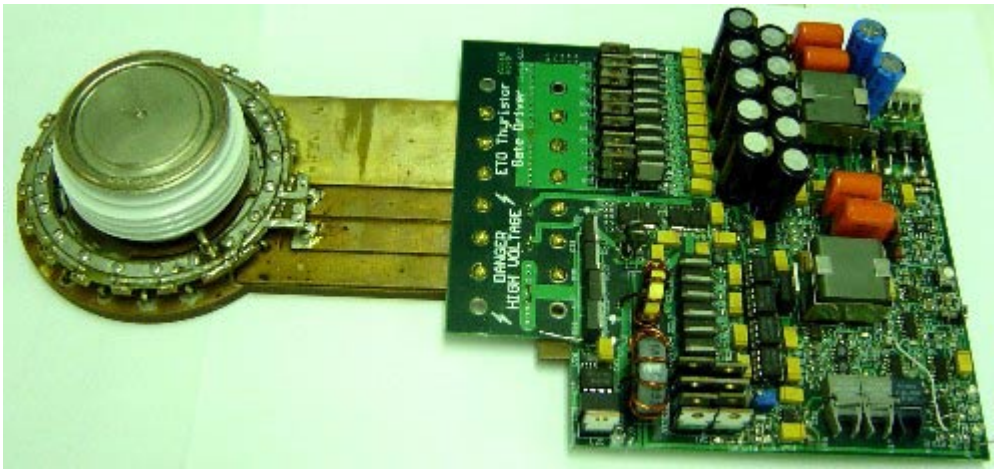

(a)




(b)

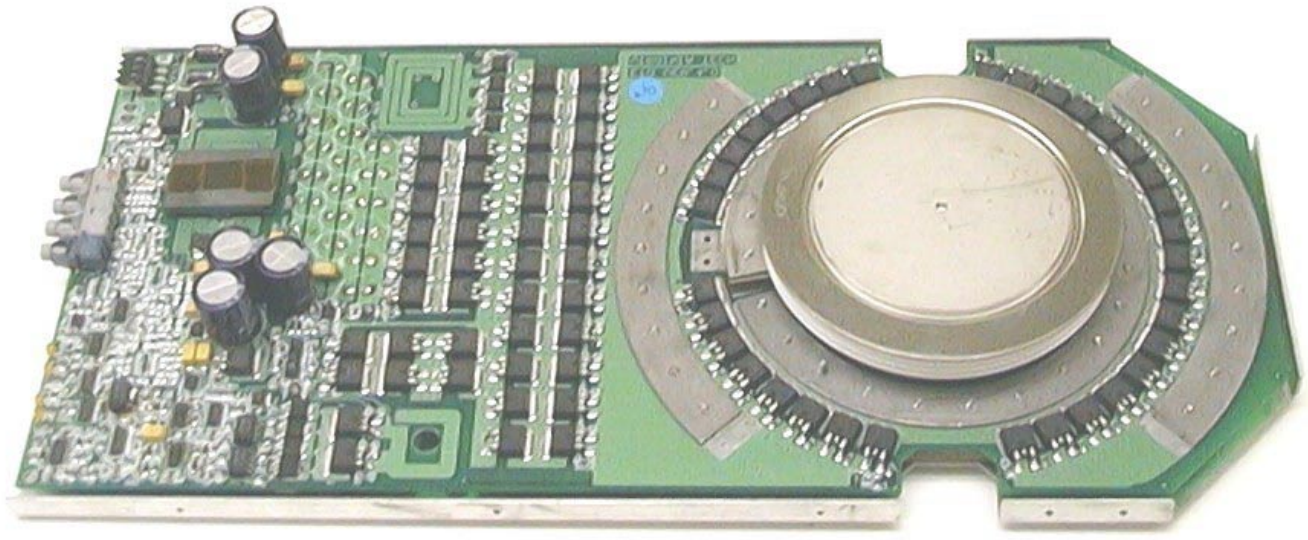
Fig. 2.3. I-V trajectories of the symmetrical ETO during (a) turn-off transition and (b) turn-on transition.

The ETO is a hybrid device created by integrating commercial GTOs and power MOSFETs. It is very convenient to use appropriate commercially available symmetrical GTOs to form desired symmetrical ETOs. Based on the 800-A/6.5-kV symmetrical GTO from Dynex, an 800-A/6.5-kV ETO0865 (see Fig. 2.4(a)) is developed. Similarly, based on the 1.0-kA/4.0-kV symmetrical GTO from Westcode Inc., a 1.0-kA/4.0-kV symmetrical ETO (the ETO1040W, see Fig. 2.2(d)) is developed. The symmetrical ETO can also be formed by using a commercial power diode in series with an asymmetrical ETO. Fig. 2.4(c) shows the picture of a 4-kA/4.5-kV asymmetrical ETO (the ETO4045TA) developed at Virginia Tech's CPES [K9]. For comparison purposes, the 800-A/6.5-kV symmetrical gate-commutated thyristor (SGCT GCU08AA130, see Fig. 2.4(b)) from Mitsubishi Inc. has also been characterized.




(a)

(b)



(c)

Fig. 2.4. Pictures of (a) an 800-A/6.5-kV symmetrical ETO, (b) an 800-A/6.5-kV symmetrical GCT and (c) a 4-kA/4.5-kV asymmetrical ETO (ETO4045TA) [K9].

## 2.2. Experimental Setup and Results

Experimental results are obtained on the 53-mm 1-kA/4.0-kV symmetrical ETO (the ETO1040W). Results are then compared with an asymmetrical ETO with the same rating. A 53-mm fast-recovery diode (SM60CXC574) is also tested for its reverse-recovery characteristics in order to establish a benchmark result for the symmetrical ETO. Finally, the 800-A/6.5-kV symmetrical GCT from Mitsubishi is characterized and evaluated.

### 2.2.1. On-state Characteristics

The on-state voltage drop of each ETO was measured by turning on the device to discharge a charged capacitor. The ETO current will first increase to a high current value and will then decrease to zero while the capacitor is discharged. The I-V curve of the device can then be obtained by monitoring the

current and voltage drop of the ETO during this discharging process. The discharging time constant in the test circuit is about 80 μs. Test results for the symmetrical ETO, asymmetrical ETO and the diode are shown in Fig. 2.5. The on-state voltage drop of ETO device is comprised of two parts: the on-state voltage of the GTO and the on-state voltage of switch $Q_E$. By paralleling more power MOSFETs for emitter switch $Q_E$, the on-state voltage drop of $Q_E$ is usually more than four times smaller than that of the GTO. So the voltage drop on the GTO is dominant in the on-state voltage drop of the ETO device. In other words, the on-state voltage drop of ETO device is mainly dictated by the GTO device part. Compared with the 1-kA/4.5-kV asymmetrical GTO with anode-shorting structure, the 1-kA/4.0-kV symmetrical GTO has a lower on-state voltage drop due to its better conductivity modulation, especially in the lower current range. This will result in the relatively lower on-state voltage drop for the symmetrical ETO. The higher the blocking voltage, the higher the on-state voltage drop of the GTO device due to the wider n-base required to block higher voltage. Compared with the 800-A/6.5-kV symmetrical ETO, the 800-A/6.5-kV SGCT has lower conduction loss due to its specially designed device structure and life time control [D8].

For asymmetrical GTOs, some advanced device processing techniques will provide a better trade-off between conduction losses and switching losses of the power semiconductor devices; one such technique uses a transparent anode. Unfortunately, these techniques will make power semiconductor devices lose their reverse blocking capability, and hence they cannot be directly used in symmetrical devices.

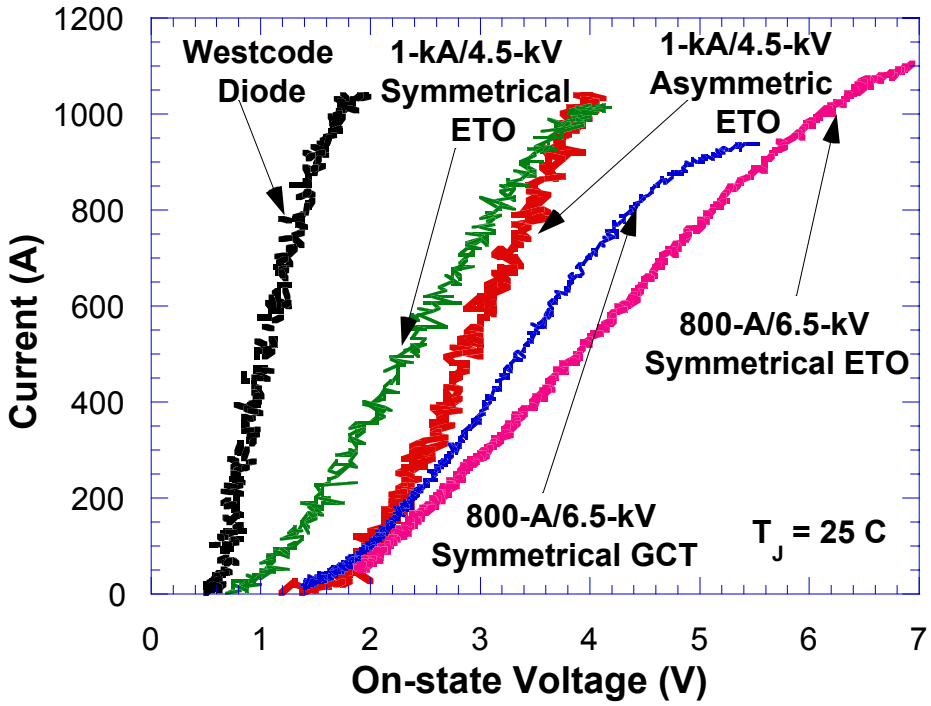



Fig. 2.5. Comparison of on-state voltage drop.

### 2.2.2. Forced Turn-off Characteristics

In a CSC, the symmetrical ETO can be used as an active switch to perform the forced turn-off and normal forced turn-on operation. Since the symmetrical ETO has high dv/dt capability due to its unity-gain turn-off, the turn-off tests are performed without a dv/dt snubber (i.e., this is a snubberless turn-off). The forced turn-off loss of the symmetrical ETO increases when the anode current or anode voltage ($V_{bus}$) increases, as shown in Fig. 2.6. The forced turn-off loss of the asymmetrical ETO is lower than that of the symmetrical ETO due to its anode-shorting structure that results in a smaller current tail. The turn-off time ($t_{off}$) of the symmetrical ETO is almost constant (2.2 μs) when the anode current or anode voltage increases, where $t_{off}$ is defined as the time between the start of the turn-off signal and the beginning of the current tail (see Fig. 2.7). Furthermore, the storage time, $t_s$, is only about 0.9 μs, and does not change

when the voltage and current vary ($t_s$ is defined as the time between the start of turn-off signal and the increase in anode voltage, as described in Fig. 2.7). The small and un-varying storage time make the ETO suitable for the series or parallel connection that is usually required by high power systems. A typical snubberless forced turn-off waveform of the symmetrical ETO is displayed in Fig. 2.7. Compared to a 1-kA/4.0-kV symmetrical ETO, the 800-A/6.5-kV symmetrical GCT has higher snubberless forced turn-off loss due to its special device structure, which is optimized for forced turn-off performance and reverse-recovery performance as well as higher voltage rating.

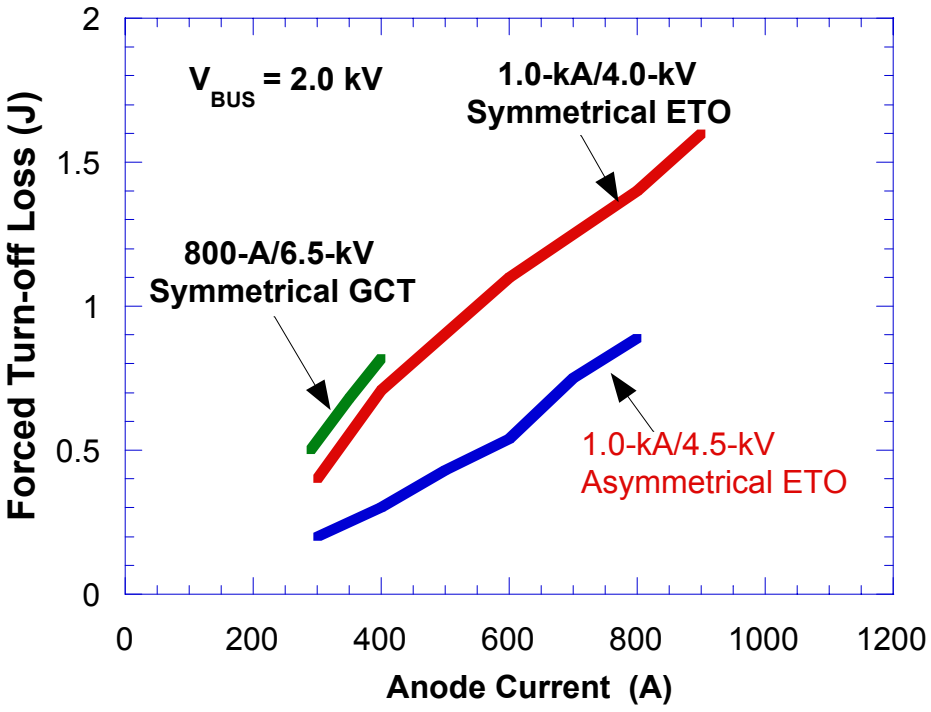



Fig. 2.6. Comparison of snubberless forced turn-off loss.

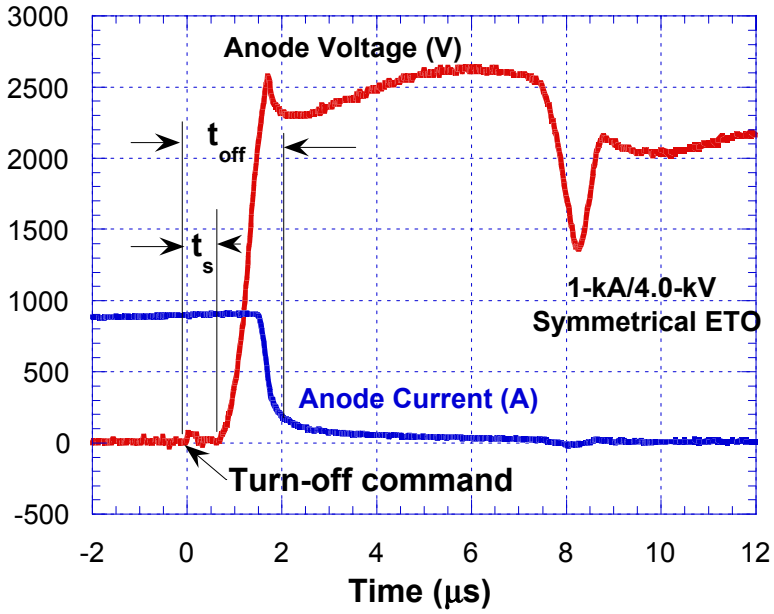



Fig. 2.7. Snubberless forced turn-off waveforms for symmetrical ETO1040W.

### 2.2.3. Forced Turn-On Characteristics

The forced turn-on process of the symmetrical ETO is similar to that of a classical GTO, and is affected by the regenerative action of the two transistors embedded in the four P-N-P-N layers. The slew rate of the gate current, the $di_G/dt$ of the ETO device, can be much higher than that of a GTO because the ETO gate driver is placed much more closely to the gate than it is in the GTO case [see Fig. 2.2(d)]. So the critical rate of the rise of the anode current for the ETO device can be dramatically improved; this will be further analyzed in Chapter 3. However, in order to limit the reverse-recovery stress of the load-commutated ETO in a CSC, a di/dt snubber is usually needed. So in our test, a turn-on di/dt snubber is used to limit the di/dt to about 80 A/μs. The measured turn-on loss increases with the anode current, as shown in Fig. 2.8. The forced turn-on loss is small as compared to the snubberless forced turn-off loss, because the di/dt snubber minimizes the overlapping of voltage and current. The turn-on delay time $t_{gd}$ is

about 0.3 μs and remains almost constant at different current levels. The $t_{gd}$ is defined as the time between the start of the turn-on signal and the decrease in anode voltage, as described in Fig. 2.9. (A typical turn-on waveform is also shown in Fig. 2.9.)

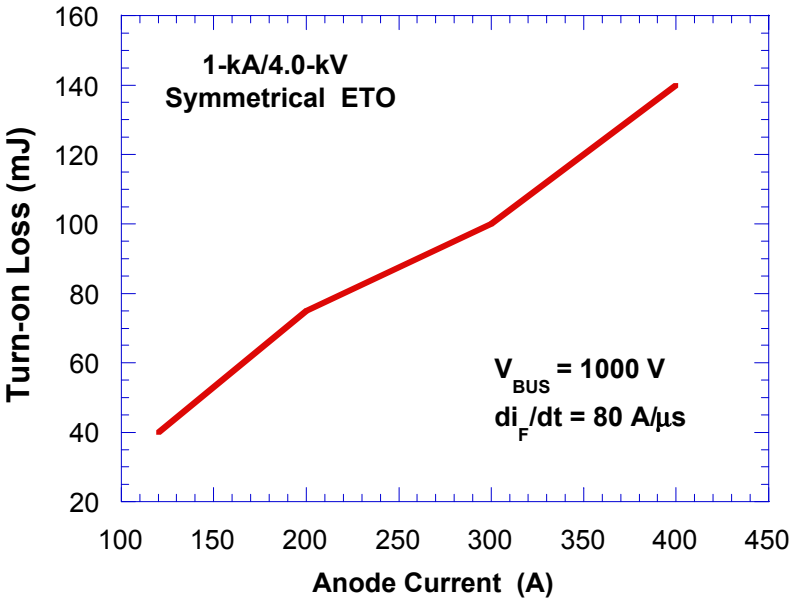



Fig. 2.8. Turn-on losses with di/dt snubber.

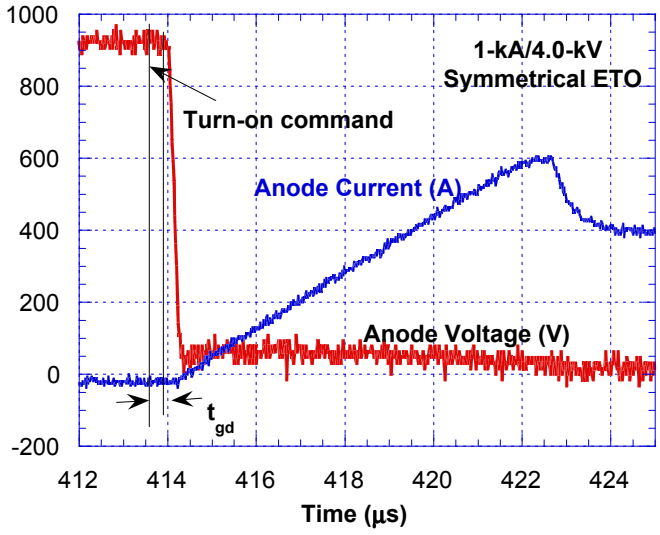



Fig. 2.9. Forced turn-on waveforms for the symmetrical ETO.

### 2.2.4. Load-Commutated Turn-Off Characteristics

The symmetrical ETO has the reverse blocking capability, and can therefore be used in circuits that require the reverse voltage to be blocked. The load-commutated turn-off (reverse-recovery) can be realized in the circuit when the voltage across the ETO changes polarity. This situation is typically encountered in a CSC. The turn-off process in this case is similar to a diode's reverse-recovery. The symmetrical ETO can be tested in this case by using it as a freewheeling diode. To properly control the main switch and freewheeling symmetrical ETO, there are several possible gating schemes that will be discussed in Chapter 4. During the device test presented in this chapter, the turn-on signal is constantly applied to the gate of the symmetrical ETO. First, a positive anode-cathode voltage is applied, and the load current will go through the tested ETO. Then, the anode-cathode voltage changes to negative, and the symmetrical ETO is turned off. The test results are shown in Fig. 2.10-Fig. 2.11, where $I_{rr}$, $E_{rec}$, $t_{rr}$ and $Q_{rr}$ are reverse-recovery current, reverse-recovery loss, reverse-recovery time and storage charge, respectively. The reverse-recovery current and storage charge of the 1-kA/4.0-kV symmetrical ETO are larger than those of a standard diode, because the ETO is optimized for forced commutation instead of load commutation. Also, unlike a standard diode, during the reverse-recovery process, the ETO behaves like an open-base PNP transistor and there are additional holes injected into the n-drift region from the p-base region on the cathode side, as shown in Fig. 2.12. In this case, the reverse-recovery loss is higher than the forced turn-off loss because although the two processes are very similar, the charge stored in the ETO is more favorable to a forced turn-off than a load-commutated turn-off, due to the device structure and doping concentration. This can be observed by comparing the dv/dt rate (2.5 kV/μs) in Fig. 2.5 with the dv/dt rate (1.0 kV/μs) in Fig. 2.13.

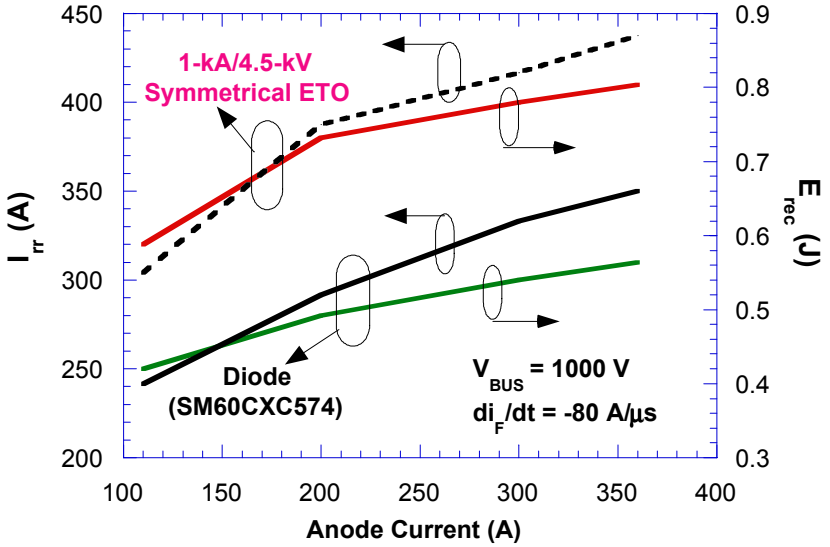



Fig. 2.10. Reverse-recovery currents and reverse-recovery losses.

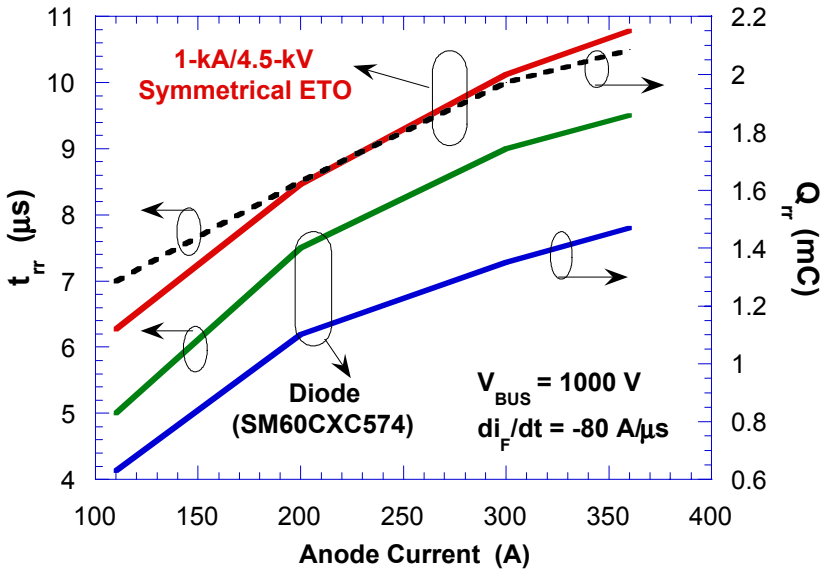



Fig. 2.11. Storage charge and reverse-recovery time.

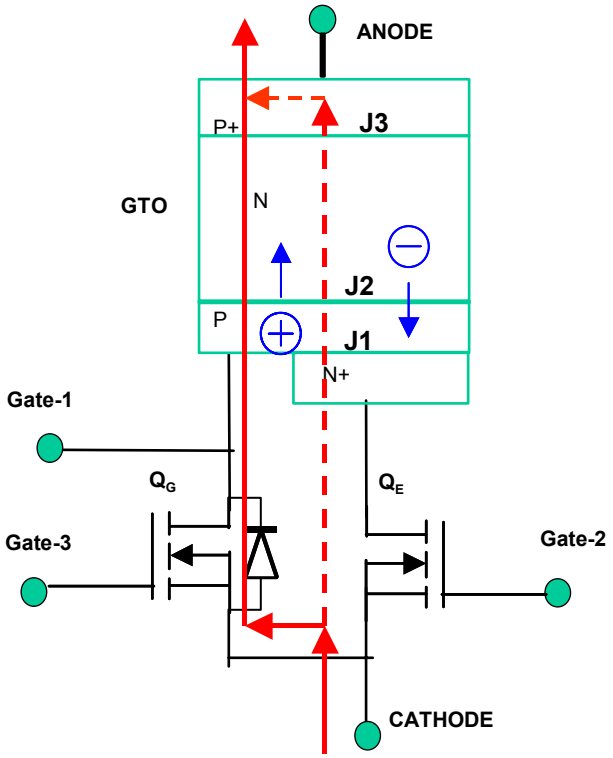



Fig. 2.12. Reverse-recovery process of symmetrical ETO.

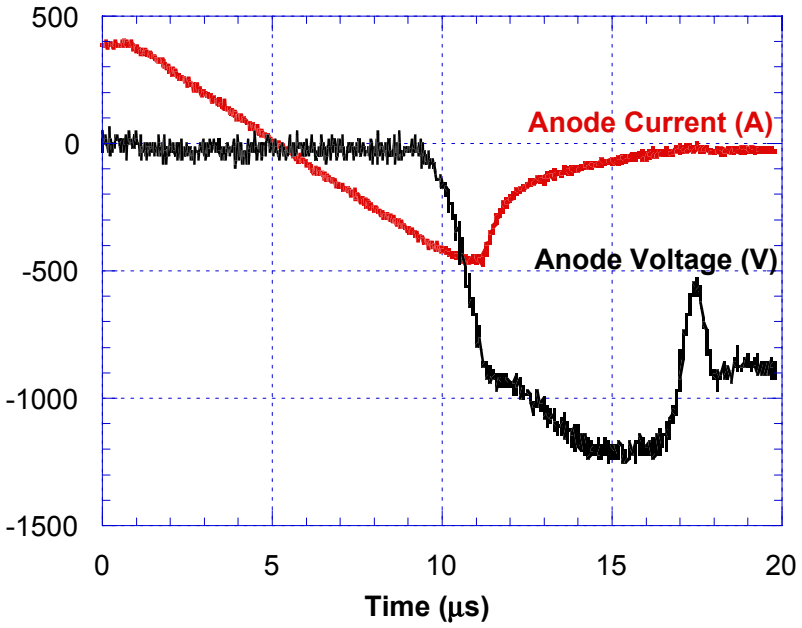



Fig. 2.13. Load-commutated turn-off (reverse-recovery) waveforms.

During the forced turn-off process, the gate driver will cut off the current path to cathode by reverse biasing junction $J_1$ (see Fig. 2.12). This will speed up the recovery of junction $J_2$ and dramatically improve the forced turn-off capability of the symmetrical ETO. However, during reverse-recovery, the gate driver only provides the path for reverse-recovery current, which is the body diode of the gate switch, as shown in Fig. 2.12. The storage charge in the N-base region close to junction $J_3$ (see Fig. 2.12) will be extracted, and junction $J_3$ will block the reverse voltage once the reverse-recovery process ends. Therefore, the gate-drive circuit has little effect on the reverse-recovery of junction $J_3$, and the reverse-recovery performance of the symmetrical ETO device is mainly dictated by the symmetrical GTO. To improve the reverse-recovery performance of the symmetrical ETO, GTO device optimization is needed. Fig. 2.14 shows a comparison of the reverse-recovery loss among the symmetrical ETO, the fast-recovery diode and the symmetrical GCT. Due to the optimization of device structure for reverse-recovery performance, the symmetrical GCT has the lowest reverse-recovery loss, but at the expense of higher conduction loss and higher forced turn-off loss, as shown in the previous section.

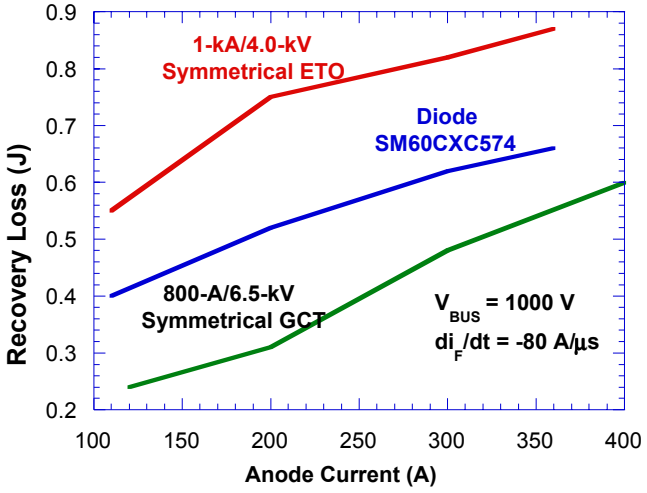



Fig. 2.14. Reverse-recovery loss comparison.

### 2.2.5. Load-Commutated Turn-On Characteristics

The load-commutated turn-on operation changes a device's operation state from reverse blocking mode to its forward conduction mode, and the I-V trajectory for this transition is shown as curve (b) in Fig. 2.3(b). With the negative anode-to-cathode voltage, the symmetrical ETO device conducts no current even when it is commanded ON. Once the device voltage becomes positive, the device current begins to increase as shown in Fig. 2.15. Since the device does not simultaneously undergo high voltage and current, the device stress as well as the switching loss is low and can therefore be neglected.

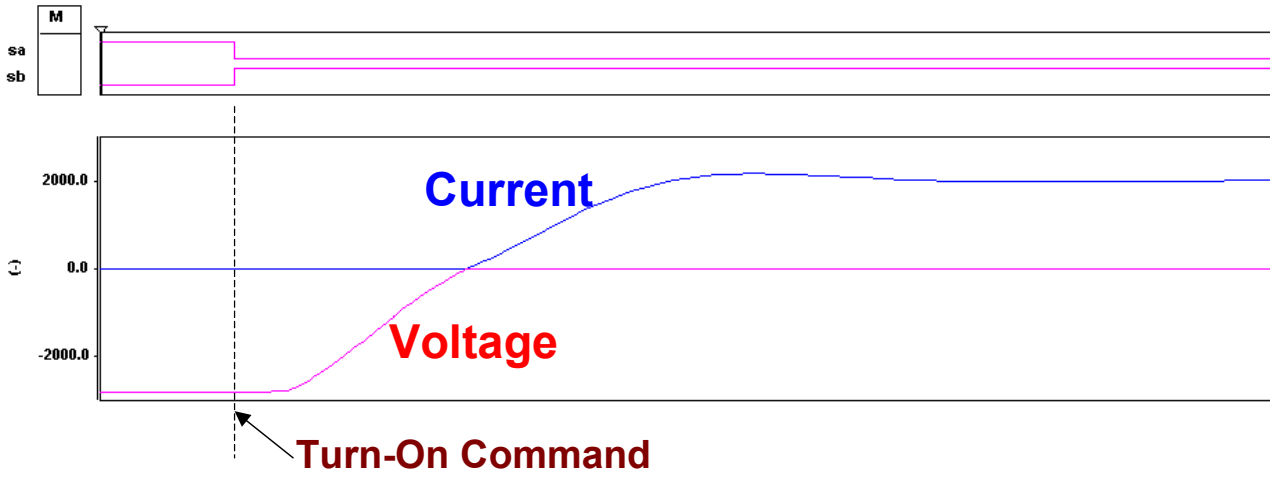



Fig. 2.15. Load-commutated turn-on waveforms for the symmetrical ETO.

## 2.3. Loss Comparison in the CSC

Due to the improved switching performance, high power rating and the reverse voltage-blocking capability, the symmetrical ETO is very suitable for use in a high-frequency CSC. Fig. 2.16 shows the simplified power circuit of the CSC using symmetrical ETOs. Compared to the asymmetrical ETO based CSC shown in Fig. 2.17, the symmetrical ETO CSC uses fewer semiconductor devices. The conduction loss and cost of the CSC are therefore reduced.

The converter loss is compared between the CSC composed of 1-kA/4.0-kV symmetrical ETOs and the CSC using asymmetrical ETOs in series with diodes. The CSC conditions are as follows: DC-link current $I_{dc}$ = 500 A; the maximum line-to-line output voltage is 2 kV; di/dt = 100 A/μs; modulation index M = 0.8; the load power factor is 0.8; the control strategy is space-vector PWM control. The loss comparison results are shown in Fig. 2.18, where $E_{on}$, $E_{off}$, $E_{rec}$ and $E_{cond}$ are the turn-on loss, forced turn-off loss, load-commutated turn-off loss and conduction loss, respectively. The asymmetrical ETO based CSC has lower switching loss due to its lower forced turn-off loss and reverse-recovery loss. However, the symmetrical ETO based CSC has much lower conduction loss, which results in a 5.7% decrease of the total loss.

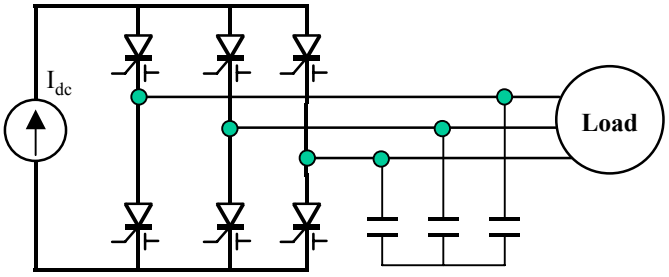



Fig. 2.16. The simplified power circuit of the symmetrical ETO based CSC.

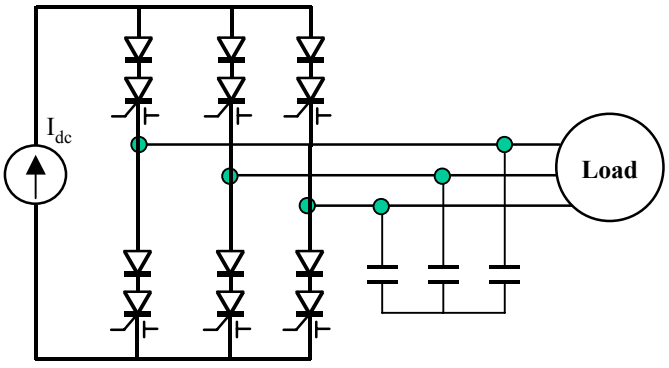



Fig. 2.17. The simplified power circuit of the asymmetrical ETO based CSC.

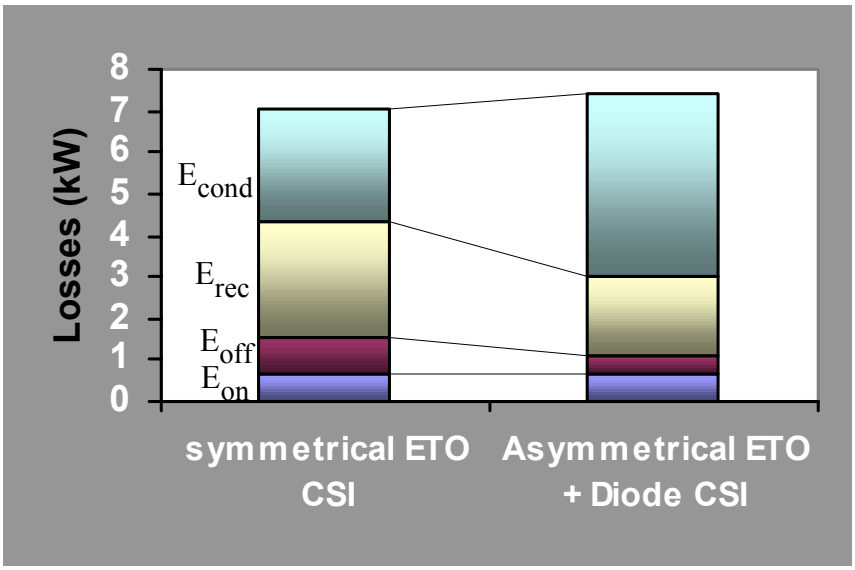



Fig. 2.18. Loss comparison between the symmetrical ETO based CSC and the asymmetrical ETO based CSC.

## 2.4. Conclusion

This dissertation offers the first-ever development and characterization of the symmetrical ETO. The on-state characteristics, forced turn-on characteristics, forced turn-off characteristics as well as the load-commutated turn-off characteristics are characterized. The results show that the symmetrical ETO has a low on-state voltage drop, which is mainly dictated by the employed symmetrical GTO device. The symmetrical ETO can also achieve snubberless forced turn-off due to the unity-gain turn-off. The forced turn-on capability is improved due to its tightly integrated gate driver. However, the reverse-recovery performance of the symmetrical ETO is also mainly dictated by the symmetrical GTO part and needs to be improved. Although the load-commuted turn-off loss is higher than that of a commercial diode, the symmetrical ETO is still suitable for use in high-power circuits that need reverse voltage-blocking capability, due to its lower conduction loss, fewer system parts, and the simplicity of its circuit without a dv/dt snubber.

# Chapter 3. Investigation of Snubberless Turn-On for the Emitter Turn-Off Thyristor

## 3.1. Introduction

A device with FBSOA (such as a MOSFET) normally has the self-current-limiting capability, i.e., the ability for a switch to limit its maximum current regardless of the voltage applied. In contrast, a device without FBSOA (such as a GTO) cannot self-limit its current. For a device with good FBSOA, hence the self-current limiting capability, the turn-on di/dt can be controlled through the gate, and most importantly no current crowding occurs during the turn-on transient. On the other hand, for a device without FBSOA, the turn-on di/dt is uncontrollable, and current crowding may happen in a localized area. An external snubber circuit can be used to avoid current crowding problems [A1]. The snubber circuit will increase a system's component count, size and cost. Therefore, a device with good FBSOA is preferred in a power-conversion system.

The ETO is a hybrid device based on the integration of a GTO and power MOSFETs. The FBSOA and high voltage-current-saturation capability of the ETO have been predicted [K1-K4] but have never been experimentally demonstrated. In this chapter, the FBSOA of the ETO is explored and experimentally demonstrated. The FBSOA of a large area ETO is also investigated. It is found that the FBSOA is not realizable in large area ETOs. A new ETO concept is then proposed for future development. Another new method for achieving snubberless turn-on is proposed and studied. Finally, using a proper gate drive and di/dt snubber, the improved turn-on performance of the ETO is analyzed and experimentally

characterized. To achieve uniform current distribution during the turn-on transient, the required gate current amplitude and rise rate are characterized for different ETO prototypes.

### 3.2. The FBSOA of the ETO

As introduced in Chapter 2, an ETO is formed by using a GTO in series with an emitter switch $Q_E$, as shown in Fig. 3.1. During the turn-on transient, $Q_E$ is turned on and $Q_G$ is turned off. A high-current pulse is injected into the GTO gate to reduce the turn-on delay time and improve the critical rate of the rise of anode current $di_A/dt$. The built-in PNP and NPN transistors inside the GTO latch up quickly, and the anode voltage of the ETO collapses to a low voltage. So the turn-on process of the ETO is just like that of a GTO.

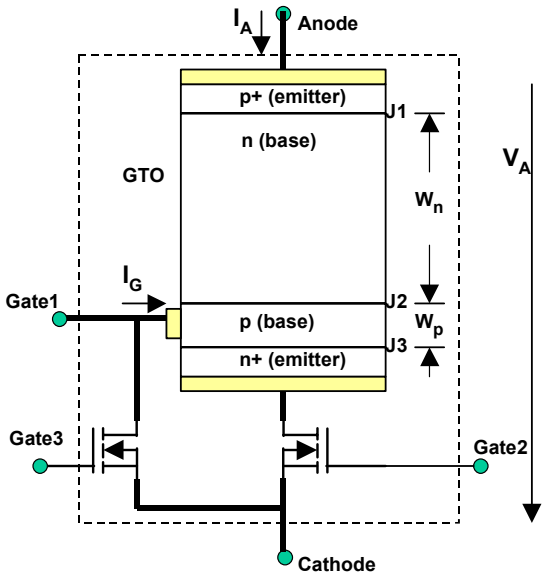



Fig. 3.1. Schematic structure of the ETO.

However, when the ETO's gate switch $Q_G$ is replaced by a self-driven MOSFET (behaving like a zener diode), as shown in Fig. 3.2, the ETO will have forward current-saturation capability [K4-K6]. In normal conduction mode, the voltage drop on the emitter switch $Q_E$ is less than ($V_{th}$-$V_{J1}$), where $V_{J1}$ is the on-

state voltage of the GTO emitter junction (see Fig. 3.2), and $V_{th}$ is the threshold voltage of $Q_G$. So $Q_G$ is off while $Q_E$ is on. Therefore, the forward-conduction behavior of the ETO is almost the same as that of the GTO. When the anode current increases, the voltage drop across $Q_E$ increases, and the voltage on $Q_G$ will also increase. When the voltage drop on $Q_G$ is larger than ($V_{th}$-$V_{J1}$), $Q_G$ conducts, and a portion of the anode current is then bypassed through the gate path. Since the current flowing out of the GTO gate is the p-base hole current that tries to turn off the ETO, both the current-conduction capability of the ETO and the voltage drop across $Q_E$ will decrease. This negative feedback process continues until the ETO reaches a balanced operation point at which the anode current no longer increases with an increase of the ETO voltage. Under the balanced operation condition, the GTO's main blocking junction $J_2$ (see Fig. 3.2) is reverse-biased, and the NPN and PNP transistor inside the GTO both operate in the active region instead of in the saturation region. The high voltage and current saturation (and hence the FBSOA) can therefore be achieved in the ETO. Under the high voltage-current-saturation state, ETO current flows into switch $Q_E$ and $Q_G$. The saturation current level of the ETO can be controlled by controlling the conduction capability of $Q_E$. This can be easily achieved if the gate voltage is controlled when $Q_E$ is a MOSFET.

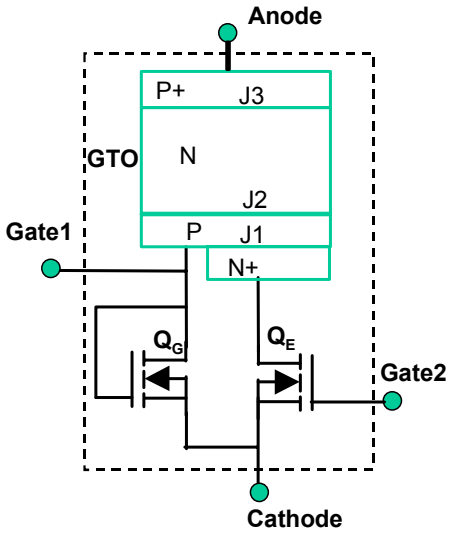



Fig. 3.2. Equivalent circuit of the ETO with self-driven gate switch $Q_g$.

### 3.2.1. Demonstration of the FBSOA of the ETO

To better understand the FBSOA of the ETO, the current-saturation capability of a 4.5-kV/1-cm$^2$ ETO was analyzed with the help of two-dimensional finite element simulations [A8]. $Q_E$ and $Q_G$ are modeled as 1-cm$^2$ low-voltage MOSFETs. The simulation results are shown in Fig. 3.3. Initially, the anode current $I_{DUT}$ increases linearly with the anode voltage $V_{DUT}$, until it reaches the saturation anode current under the given gate voltage $V_{G\text{-}DUT}$. Then any further increase of the anode current will cause part of the anode current to be bypassed through the gate path, and the GTO will operate in the active region, with main junction $J_2$ reverse-biased. Under this condition, the anode current increases slowly with the anode voltage due to the increase of the PNP transistor current gain. When the anode voltage is close to the breakdown voltage of main junction $J_2$, the anode current starts to increase significantly again and reaches the boundary of the FBSOA. The ETO saturation current density at 5-V gate voltage is about 55 A/cm$^2$, as shown in Fig. 3.3.

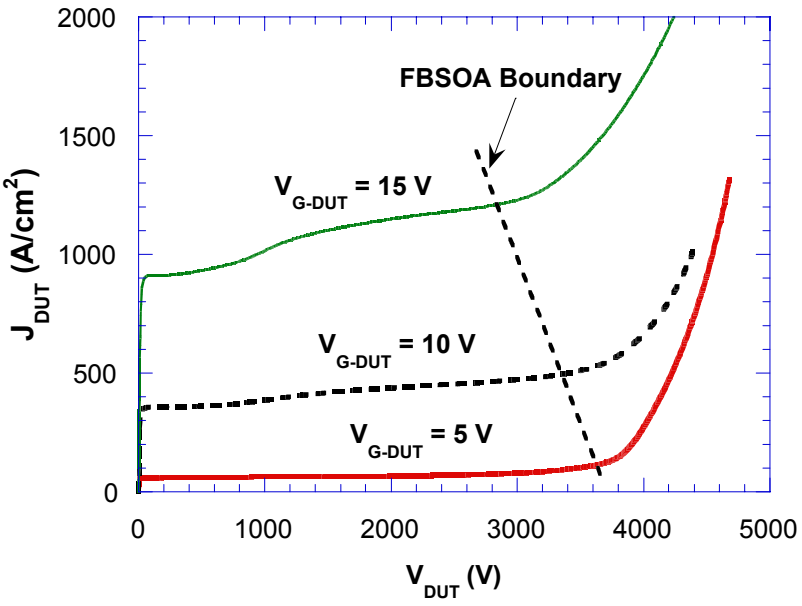
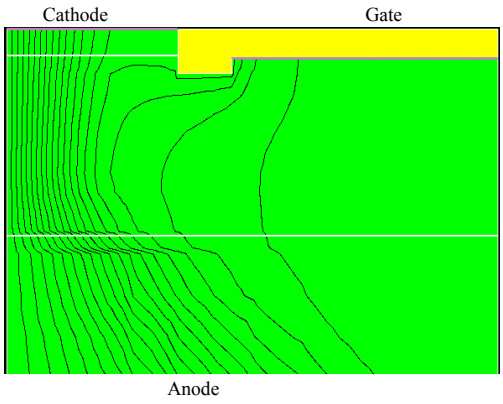
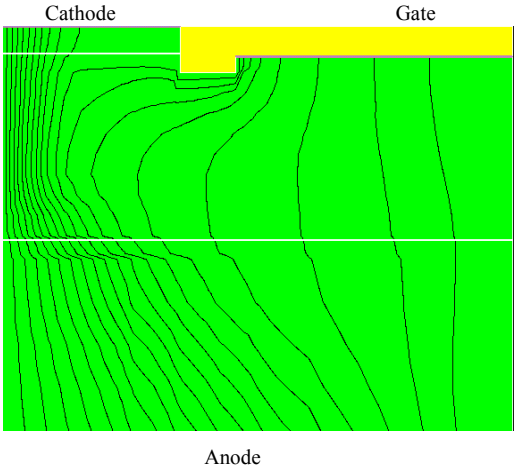



Fig. 3.3. Simulated FBSOA curve of the ETO.

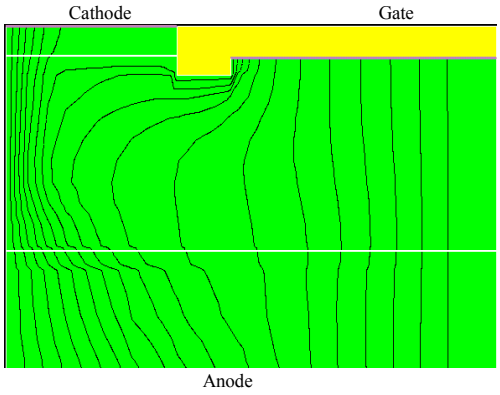
The current flow lines of the ETO under high voltage and current saturation conditions with 5-V gate voltage are shown in Fig. 3.4. The anode voltages of Fig. 3.4(a), (b) and (c) are 2.0 kV, 4.0 kV and 4.5 kV, respectively. It is apparent that the ratio of gate current to the anode current will increase with the anode voltage to keep the GTO working under high voltage and current saturation conditions. Fig. 3.4(d) shows the potential contours inside the GTO when the anode voltage is 2.0 kV with 5-V gate voltage. Clearly, main junction $J_2$ is reverse-biased and withstands most of the anode voltage.



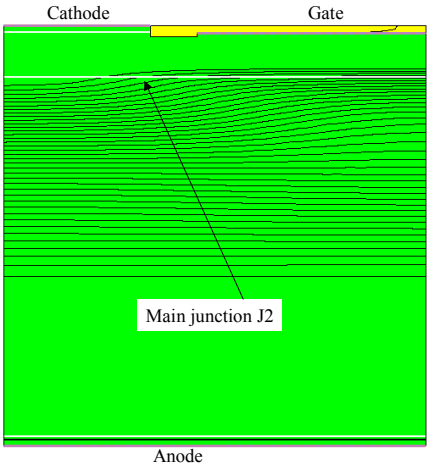

(a) ($V_{G\_DUT}$ = 5 V, $V_{DUT}$ = 2000 V)




(b) ($V_{G\_DUT}$ = 5 V, $V_{DUT}$ = 4000 V)




(c) ($V_{G\_DUT}$ = 5 V, $V_{DUT}$ = 4500 V)




(d) ($V_{G\_DUT}$ = 5 V, $V_{DUT}$ = 2000 V)

Fig. 3.4. Current flow-lines inside the GTO under high voltage and current saturation conditions ($V_{G\text{-}DUT}$ = 5 V): (a) $V_{DUT}$ = 2.0 kV, (b) $V_{DUT}$ = 4.0 kV, (C) $V_{DUT}$ = 4.5 kV, and (d) potential contours inside the GTO ($V_{DUT}$ = 2 kV, $V_{G\text{-}DUT}$ = 5 V).

In order to demonstrate the FBSOA of the ETO, an ETO is developed using a low-rating GTO BTW58-1300R (25 A, 1300 V) and the MOSFET IRF540 (28 A, 100 V) as both the emitter switch and the gate switch. In the normal conduction mode, current is injected into the GTO gate to ensure its complete

conduction through a voltage source in series with a resistor. Fig. 3.5 shows the developed ETO equivalent circuit model.

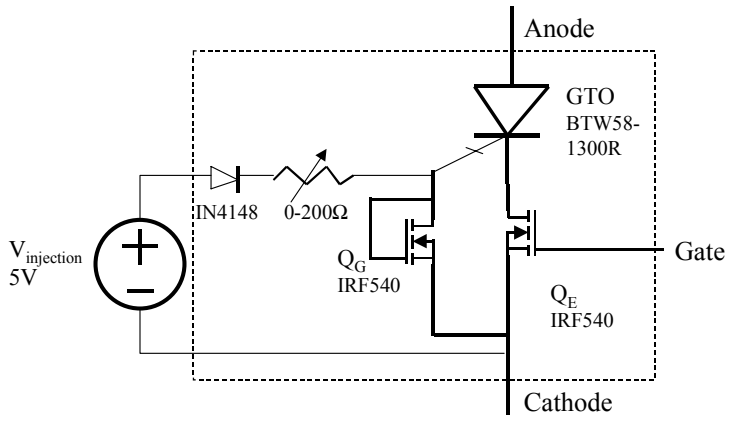
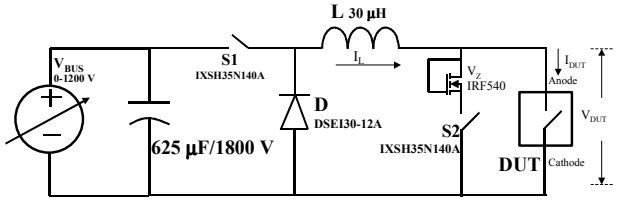


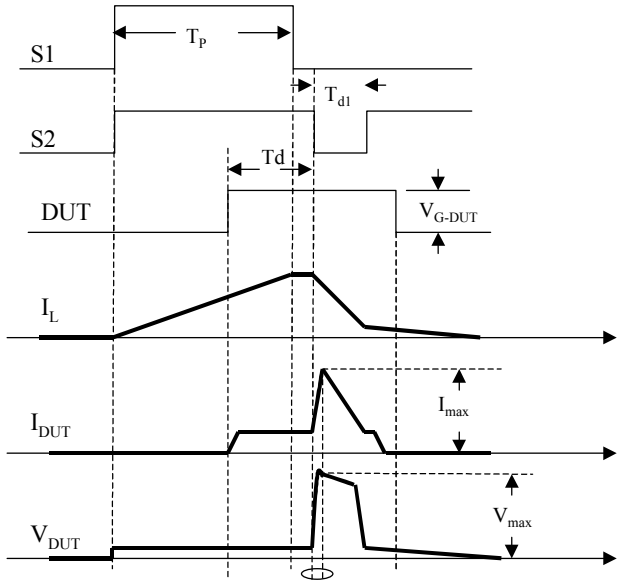

Fig. 3.5. Equivalent circuit of the developed small ETO.

The test circuit and control signal for the FBSOA test are shown in Fig. 3.6(a) and (b). When the test begins, the auxiliary switches $S_1$ and $S_2$ are turned on, and the current is built up in the inductor L. When the inductor current $I_L$ reaches the required value, $S_1$ is turned off. The device under test (DUT) is turned on with a gate bias voltage, $V_{G\text{-}DUT}$, for a period of $T_d$ (5 μs) before $S_2$ is turned off in order to ensure that the DUT is fully on. So the inductor current freewheels through diode D, switch $S_2$, and the DUT after $S_1$ is turned off (see Fig. 3.6). Then, $S_2$ is turned off and the total inductor current is forced to go through the DUT. If the inductor current is larger than the saturation current of the DUT at a given gate voltage $V_{G\text{-}DUT}$, the voltage across the DUT will increase to its forward-biased breakdown voltage. Thus, the FBSOA curve for the DUT at a gate voltage $V_{G\text{-}DUT}$ can be obtained by combining the DUT current waveform, $I_{DUT}$, and the DUT voltage waveform, $V_{DUT}$. The whole FBSOA curve for the DUT can thus be obtained by varying $V_{G\text{-}DUT}$ and inductor current $I_L$. After a delay time $T_{d1}$ (3 μs), switch $S_2$ is turned on again to

protect the DUT from failure. So the test is nondestructive, and the following test results are all obtained from the same DUT.




(a)



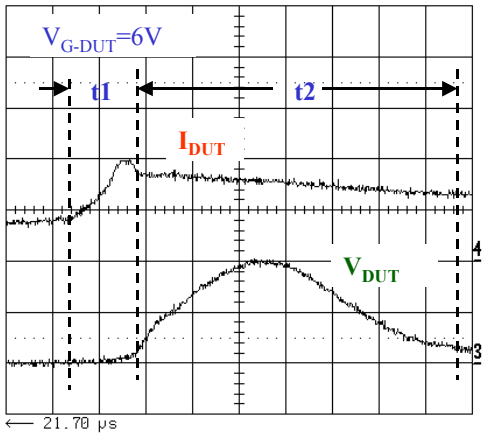

(b)

Fig. 3.6. (a) FBSOA test circuit, and (b) control signal for the FBSOA test.

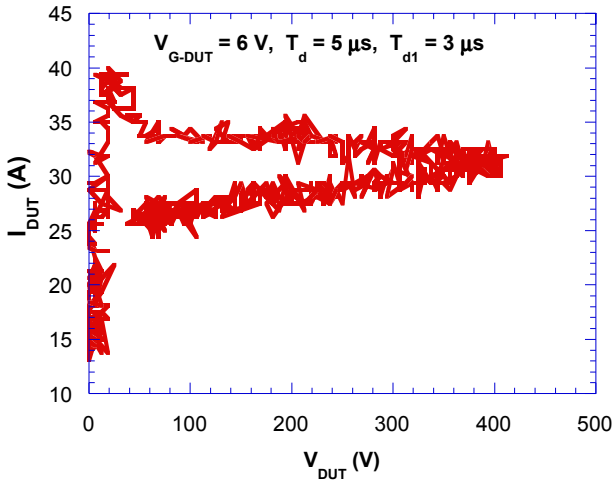
Fig. 3.7 displays the test waveforms for the ETO shown in Fig. 3.5 with 6-V gate voltage. During time interval $t_1$ (see Fig. 3.7(a)), the anode current of the ETO increases quickly due to the fast turn-off of switch $S_2$. The ETO current rises quickly to 40 A, and the anode voltage remains low. During time interval $t_2$, the ETO enters the high voltage and current saturation region, so the anode voltage increases

quickly while the anode current decreases due to the dissipation of the inductor energy. At a particular point, the rise of the ETO voltage also stops and the anode voltage starts to decrease with the slowly decreasing anode current. The locus of the voltage and current during $t_2$ is considered as a dynamic FBSOA curve, as plotted in Fig. 3.7(b). The second portion of the locus, however, is used to represent the steady-state FBSOA of the ETO, as shown in Fig. 3.7(c).

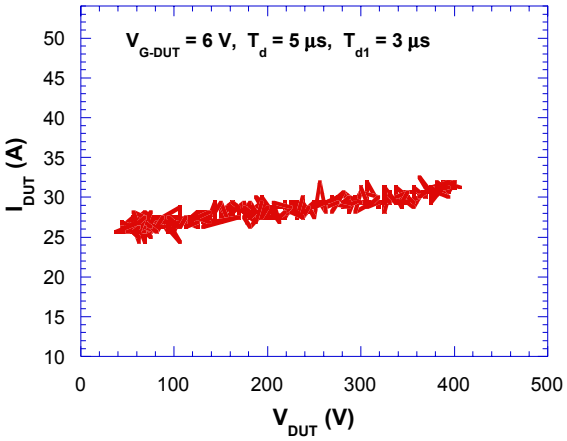
The FBSOA curves experimentally obtained for the ETO are shown in Fig. 3.8, where different saturation current levels clearly correspond to different gate voltages. The higher the gate voltage, the higher the saturation current. In normal applications, the turn-on di/dt of the ETO can therefore be controlled by limiting the rate of voltage increase in the $Q_E$ gate by using a large gate resistance.




(a)




(b)




(C)

Fig. 3.7. (a) Test waveforms for $I_{DUT}$ and $V_{DUT}$ (current: 20 A/div, voltage: 200 V/div, time: 0.2 µs/div); (b) dynamic I-V curve; and (c) FBSOA curve for the small ETO.

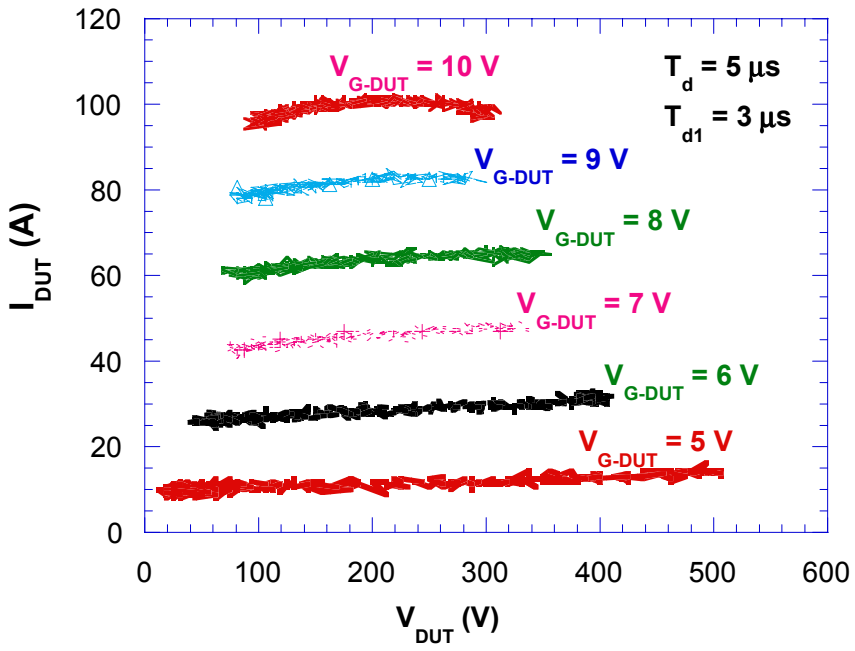



Fig. 3.8. Tested FBSOA curve of the small ETO.

The existence of the FBSOA in the ETO device is very important from the application standpoint. First, the lossy passive di/dt snubber can be minimized or eliminated in high power systems, since the turn-on di/dt can be controlled through the gate driver of $Q_E$. Second, the over-current or short-circuit protection may become easier due to the self-current-limiting capability. These capabilities allow the ETO to compete directly with the IGBT.

### 3.2.2. Analysis of the FBSOA for Large-Area ETOs

It is worthwhile to point out that the previous test results are obtained based on a small ETO device (GTO die << 1 $cm^2$). It is clearly shoen in Fig. 3.8 that the current distribution in this ETO is uniform, and that current saturation is achieved over the whole 1-$cm^2$ chip area. Simulation results are also obtained under the assumption that all the cells in the GTO are uniform and that no current-sharing problem exists.

For a large-area ETO, these assumptions are not necessarily true. The current distribution may vary widely among different cells in large area ETO devices. So the current crowding or filamentation phenomenon is more likely to occur, resulting in an increase of the current density of a few cells. Whether or not a large area ETO can have an FBSOA depends on two factors: whether the level of non-uniformity, and hence the current filamentation, occurs under turn-on or forward-biased conditions; and whether the negative feedback mechanism available at each cell level is able to self-limit the cell current to allow eventual uniform current saturation, and hence sharing.

In a large area ETO (see Fig. 3.9), emitter switch $Q_E$ is a centralized component in series with a large area GTO that consists of many cells. The filamented cell may have a current density that is too high, and thus exceeding its own FBSOA. Device failure would occur in this case if an attempt was made to turn on the device slowly or to conduct the test shown in Fig. 3.6. A large area ETO model that may clarify the FBSOA issue is shown in Fig. 3.9. A large area ETO can be modeled as two groups of GTO cells in parallel. The small GTO cells have higher saturation current levels. Once the large uniform cells enter their FBSOA, the small cells take over the total current, potentially forcing the small cells to exceed the FBSOA boundary.

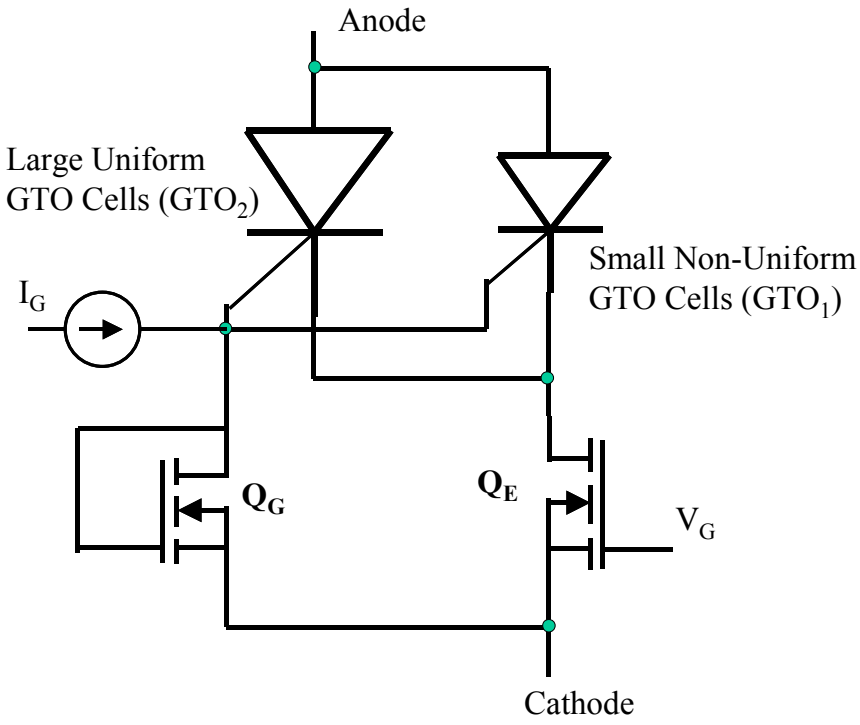
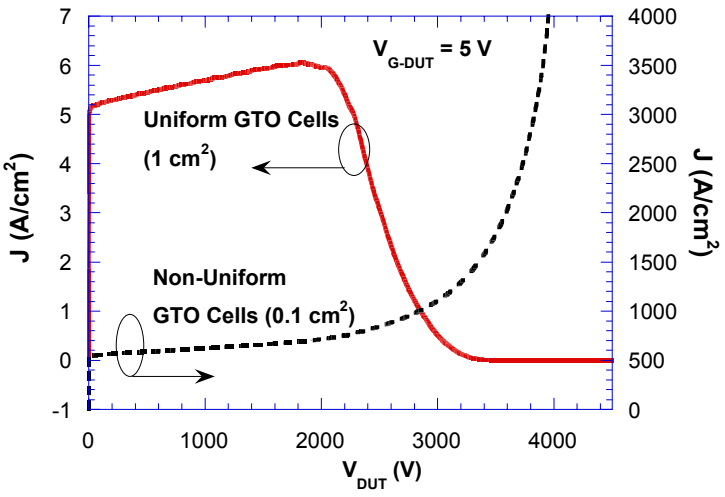



Fig. 3.9. Equivalent circuit of a large area ETO with centralized $Q_E$ and $Q_G$.

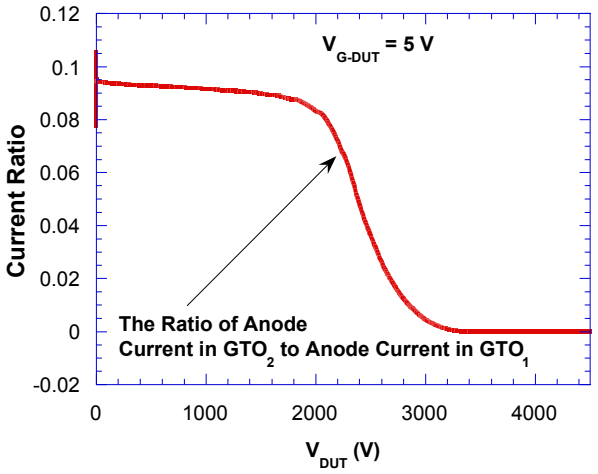
To verify this analysis, numerical simulations are performed for a large area ETO. It is assumed that the non-uniformity of the large area ETO comes from the variation in high-level carrier life time among different cells in the GTO. In the simulation, 0.1-cm$^2$ small non-uniform GTO cells (labeled $GTO_1$) with an average high-level life time of 33 μs are assumed to exist in the 1-cm$^2$, large, uniform GTO cells (labeled $GTO_2$) that have an average high-level life time of 30 μs. Other simulation conditions are the same as those described in section 3.2.1. Under 5-V gate voltage, the simulated ETO has a saturation current of 55 A, which is the same as that obtained in the previous simulation. If the simulated ETO device has uniform current distribution, the saturation current density should be 55 A/cm$^2$, and the FBSOA curve should be the same as that in Fig. 3.3. However, Fig. 3.10 shows the completely different voltage and current saturation curve of the non-uniform ETO under 5-V gate voltage. In the latched conduction state, $GTO_1$ has higher current density (due to its better current conduction capability) than

does $GTO_2$. Once they are forced to operate under the high voltage saturation condition, the negative feedback effect of $GTO_2$ is much larger than that of $GTO_1$, since they share the same $Q_E$ and $Q_G$. The unbalanced feedback effect makes the current distribution between $GTO_1$ and $GTO_2$ even worse. After both GTOs operate in the high voltage saturation region, $GTO_1$ conducts 90% of the total current, while $GTO_2$ conducts only 10% of the total current. So the saturation current density of $GTO_1$ is about 550 $A/cm^2$, which is 100 times larger than that of $GTO_2$, as shown in Fig. 3.10(a).

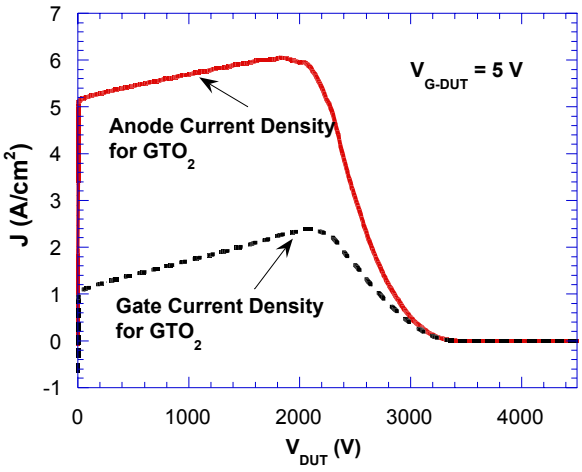
The ratio of the current in $GTO_2$ to the current in $GTO_1$ keeps decreasing due to the unbalanced negative feedback, as shown in Fig. 3.10(b). At some point, $GTO_2$ is gradually turned off due to the stronger negative feedback, as shown in Fig. 3.10(c). At last, all the current is carried by $GTO_1$, and so the current density in $GTO_1$ is extremely high (above 2000 $A/cm^2$) when the anode voltage is close to the breakdown voltage of main junction $J_2$.




(a)




(b)




(c)

Fig. 3.10. Simulated high voltage and current saturation curve of a large area ETO with centralized $Q_E$ and $Q_G$: (a) anode current in $GTO_1$ and $GTO_2$, (b) the ratio of anode current in $GTO_2$ to anode current in $GTO_1$, and (c) anode current and gate current in $GTO_2$.

Fig. 3.11 shows a proposed possible failure trajectory of a large area ETO under the FBSOA test shown in Fig. 3.6. The trajectory of large, uniform GTO cells ($GTO_2$) is from point 1 to point 2, then to point 3,

and then to point 4. The trajectory of small, non-uniform GTO cells ($GTO_1$) is from point 1 to point $2^{\#}$, then to point $3^{\#}$, and then to point $4^{\#}$. Eventually, the device fails due to the fact that the current density of the small, non-uniform GTO cells at operation point $4^{\#}$ is high enough to cause thermal runaway in the local region. Assuming that the saturation current density is $J_0$ if the ETO is uniform, the ratio of the large uniform cells' area to the small non-uniform cells' area is N, then the saturation current density of the small non-uniform cells, $J_1$, can be roughly calculated as follows:

$$J_1 = N \times J_0 . \quad (3\text{-}1)$$

Since N is much larger than 1 in a large area ETO, $J_1$ is usually large enough to cause device failure under high voltage saturation conditions, even though $J_0$ is within the FBSOA boundary.

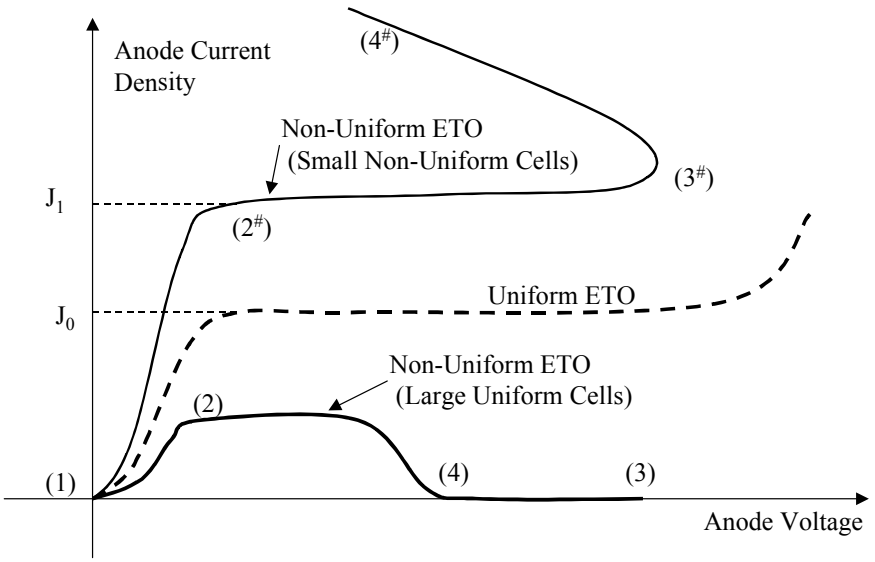



Fig. 3.11. Possible failure trajectory of a large-area ETO under the FBSOA test shown in Fig. 3.6.

From the previous simulation and analysis, it is easy to deduce that the unbalanced negative feedback effect provided by the centralized $Q_E$ may enhance the non-uniform distribution, thus possibly resulting in current filamentation in a large area ETO. So a large area ETO's FBSOA has not yet been demonstrated.

In order to achieve better FBSOA in large area ETOs, $Q_E$ should be designed to be a distributed component. In this way, each cell current is limited by the negative feedback provided by its own $Q_E$, and so can avoid current filamentation, thus maintaining uniform current distribution even under high voltage and current saturation conditions.

To verify this analysis, numerical simulations are also performed for a large area ETO device with distributed emitter switch $Q_E$ and gate switch $Q_G$. Fig. 3.12 shows the equivalent circuit for this ETO, which has the same GTO parameters as those shown in Fig. 3.9 except that this ETO has a separate emitter switch and gate switch.

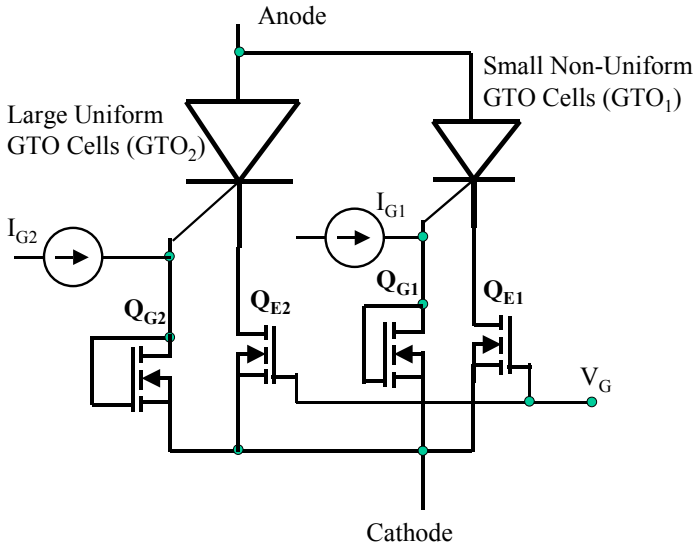
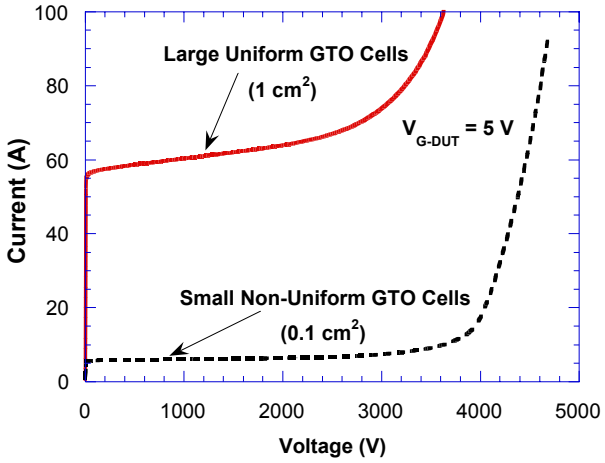


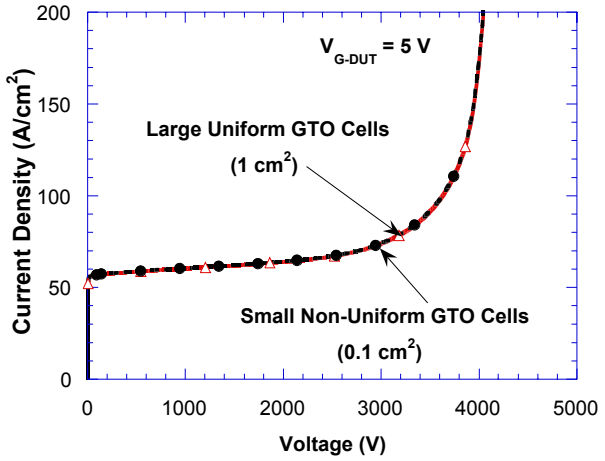

Fig. 3.12. Equivalent circuit of a large area ETO with distributed $Q_E$ and $Q_G$.

Under the same simulation conditions as those described in section 3.2.1, the high current and voltage saturation curve with 5-V gate voltage is displayed in Fig. 3.13. It is apparent that the small, non-uniform GTO cells and large, uniform GTO cells have uniform current distribution even under high voltage and

current saturation conditions, and that their saturation current densities are all about 55 A/cm$^2$, as was the case for the small-area ETO. So the proposed ETO structure is an effective way to achieve better FBSOA for large area ETOs. Future development of the ETOs, using the structure shown in Fig. 3.12, is currently underway.




(a)




(b)

Fig. 3.13. Simulated high voltage and current saturation curve of a large area ETO with distributed $Q_E$ and $Q_G$: (a) saturation current and (b) saturation current density.

### 3.3. Snubberless Turn-On Process Analysis of the ETO

From the previous analysis, we know that with a self-driven MOSFET as the gate switch, the ETO has a good FBSOA, and hence achieves the snubberless turn-on capability. However, for a large-area ETO such as that shown in Fig. 3.9, the FBSOA is poor due to the non-uniform current distribution caused by the unbalanced negative feedback provided by the centralized gate switch.

For a thyristor-based device, the critical rate of the rise of anode current ($di_A/dt$) can be improved by injecting a gate current pulse with high amplitude and high slew rate ($di_G/dt$) [B4, D2]. Due to the tightly integrated gate drive circuit, a gate current pulse with high amplitude can be injected into the GTO's gate with a much higher slew rate. Using the improved gate-drive circuit instead of the self-driven MOSFET as the gate switch, does the ETO have the snubberless turn-on capability?

To answer this question, the turn-on process of the GTO device is first introduced. Due to the large gate loop inductance (above 100 nH) of the GTO gate driver, a gate current pulse with limited amplitude as well as limited slew rate can be injected into the GTO's gate. Referring to the GTO's schematic structure shown in Fig. 3.1, by applying a pulse current to the gate, the p-base and n+-emitter junction $J_3$ is forward-biased; excess electrons are then injected from the n+-emitter layer to the p-base layer; these electrons then diffuse towards the base-collector junction $J_2$. At the same time, extra holes are provided by the gate current $I_G$ in order to maintain space charge neutrality. Therefore, the conductivity of the p-base is heavily modulated. The diffusing electrons that do not recombine in the p-base will reach the edge of the $J_2$ space-charge region after the delay time $t_p$ (also called the p-base transient time), which is given by Equation (3-2):

$$t_p = W_{p(undep.)}^{\ 2} / 2D_n, \qquad (3\text{-}2)$$

where $W_{p(undep.)}$ is the width of the un-depleted p-base, and $D_n$ is the electron diffusion coefficient.

Having reached the $J_2$ space-charge region, the electrons are quickly swept through by the built-in electric field. When approaching junction $J_1$, these electrons will serve as excess majority carriers and will lower the potential of the n-base layer. So the forward bias across junction $J_1$ is increased, and holes are injected from the p+-emitter into the n-base layer. Some injected holes are recombined in the n-base, while others will diffuse through the un-depleted n-base towards junction $J_2$. These holes will reach the edge of the $J_2$ space-charge layer after a transient time interval $t_n$ (also called the n-base transient time), which is given by Equation (3-3):

$$t_n = W_{n(undep.)}^{\ 2} / 2D_p, \qquad (3\text{-}3)$$

where $W_{n(undep.)}$ is the width of the un-depleted n-base, and $D_p$ is the hole diffusion coefficient. The holes are then instantaneously swept across junction $J_2$ and into the p-base region. These injected holes serve as excess majority carriers and will cause the increased injection of electrons from the n+-emitter into the p-base. As a result, positive feedback is formed.

The delay time $t_{gd}$ is defined as the transient time between the moment at which the gate current increases to 10% of the final value and the time when the anode voltage decreases to 90% of the initial value, as indicated in Fig. 3.14. It is the time from the application of the gate current to the moment at which the $J_2$ space-charge region is discharged. In the case of the GTO, the rate at which the gate current is applied is generally low, and the delay time $t_{gd}$ is generally longer than the transient time for the carriers diffusing through the base region, as described in Equation (3-4).

$$t_{gd} \geq t_n + t_p = W_{p(undep.)}^{\ 2} / 2D_n + W_{n(undep.)}^{\ 2} / 2D_p \qquad (3\text{-}4)$$

After the positive feedback forms, the $J_2$ space charge region is quickly flooded with excess carriers. The positive space charge region in the n-base is discharged by the electrons injected from the n+-emitter over junction $J_3$, and the negative space charge region in the p-base is discharged by the holes injected from the p+-emitter over $J_1$. So the thickness of the $J_2$ space charge region is reduced, resulting in both the fall of the anode voltage and the increase of the anode current. The voltage fall time $t_f$ is defined as the time it takes for the anode voltage to be reduced from 90% to 10% of its initial value, as indicated in Fig. 3.14.

With the formation of positive feedback, after the anode current exceeds the latching current, the gate has little control over the turn-on process. The rise of the anode current is dictated by the physical process of the device as well as the constraints of the external circuit. Since the slowly applied gate current initially only turns on a small area of the GTO, the turn-on process begins with a small cathode area that is close to the gate contact and that spreads to adjacent regions. The typical spreading speed is about 5000 cm/s [A2]. To avoid a localized overheating effect and to prevent turn-on failure in the device, an external inductor is usually used in the external circuit to limit the anode current rise rate to a level below the critical $di_A/dt$. The critical $di_A/dt$ for the commercial GTO devices is usually below 1000 A/μs. To ensure that the entire junction area is uniformly turned on before turn-off switching, a minimum turn-on time (usually about 100 μs) is required for traditional GTO devices. The typical turn-on waveforms for GTO devices are shown in Fig. 3.14. Another way of describing the non-uniform turn-on is that the turn-on process relies heavily on the self-regenerative process of the thyristor latch-up. Carriers needed for conductivity modulation are provided from the anode and cathode sides, not from the gate-drive circuit (or they are only partially provided from the gate-drive circuit).

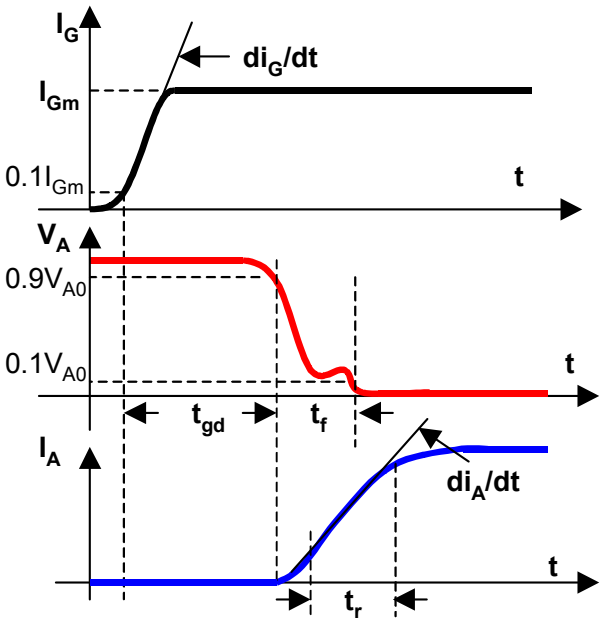



Fig. 3.14. The GTO's turn-on process.

To analyze the snubberless turn-on performance of the ETO device, the two-dimensional device simulation tool Medici is used to simulate its snubberless turn-on process. The GTO device cell structure studied is shown in Fig. 3.15. The p-base and n-base doping are $1\times10^{17}$ $cm^{-3}$ and $2\times10^{13}cm^{-3}$, respectively. The device area is 15 $cm^2$ and the simulated on-state I-V curve for the 1-kA/4.5-kV GTO is shown in Fig. 3.16. The anode current increases exponentially with anode voltage, and the gate current has little control over anode current due to the thyristor latch-up during on-state.

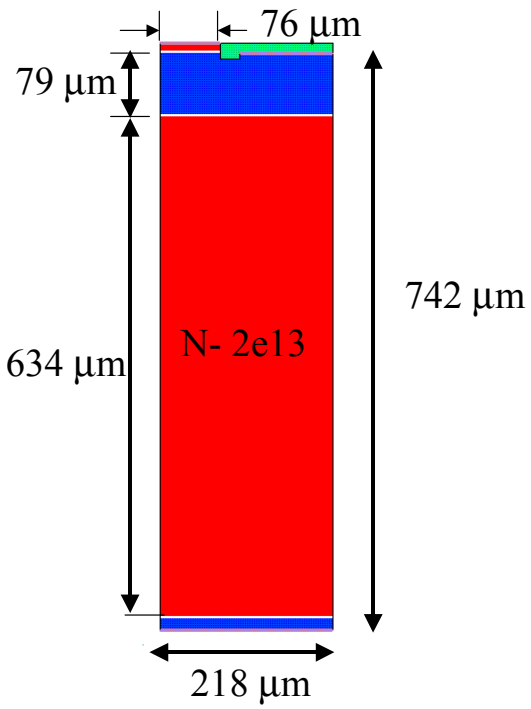



Fig. 3.15. GTO device structure.

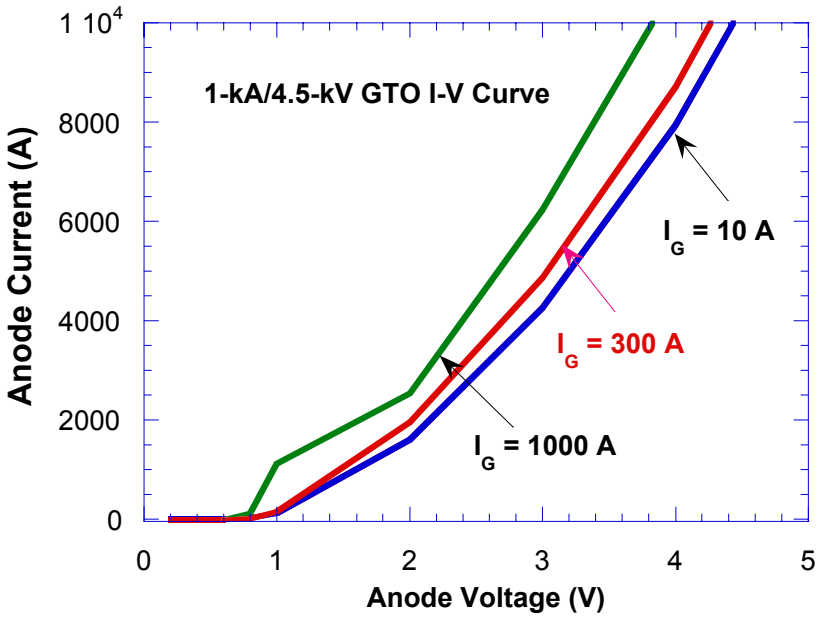



Fig. 3.16. Simulated I-V curve for 1-kA/4.5-kV GTO.

Using the simulation circuit shown in Fig. 3.17, Fig. 3.18 portraits the snubberless turn-on waveforms for the GTO device, with a gate current amplitude of 600 A and a gate current slew rate of 4 kA/μs. From these waveforms, it is clear that after a delay of about 77 ns, the anode current begins to rise slowly. After about 170 ns, the anode current rising rate increases dramatically, indicating the latch-up of the thyristor. Then, the anode current exponentially increases to the steady-state current level and the anode voltage begins to decrease until it reaches the level of the on-state voltage.

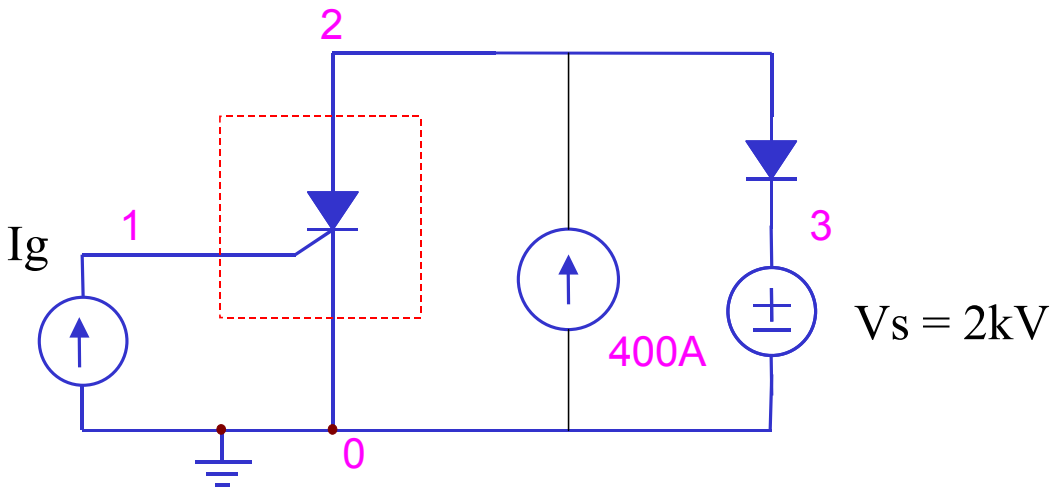



Fig. 3.17. Simulation circuit for snubberless turn-on of the ETO device.

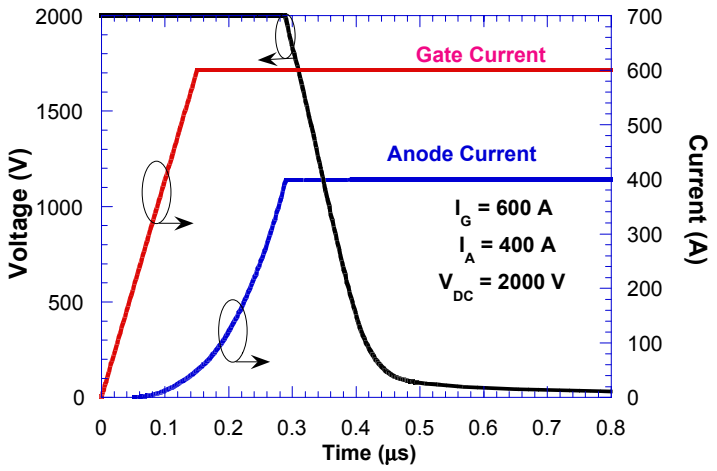



Fig. 3.18. Simulated snubberless turn-on waveforms for the ETO device.

The proceeding simulation is conducted based on the assumption of uniform current distributions among all GTO cells. For large-area devices in high-power applications, there will be some gate current delay among different cells. After latch-up, if the device current is less than the steady-state level and continues to increase, the early-triggered GTO cells will carry more current than the later-triggered GTO cells since the conductivity of the latched GTO cells is much larger than that of the un-latched ETO cells. A small device with a 0.15-$cm^2$ device area in parallel with the larger device can be used to study the delayed effect. The smaller device is triggered 50 ns earlier than the big device. With the same simulation circuit and gate-drive conditions, the small device will have a peak current density of 140 $A/cm^2$, which is more than five times higher than the average current density (26.7 $A/cm^2$), as shown in Fig. 3.19. With longer gate delay and larger device area ratio between the later-triggered device and the early-triggered device, the early-triggered device will experience a much higher current density. Under this condition, thermal runaway will probably occur due to the simultaneously high voltage and high current stress on a small area of the device, and will result in device failure.

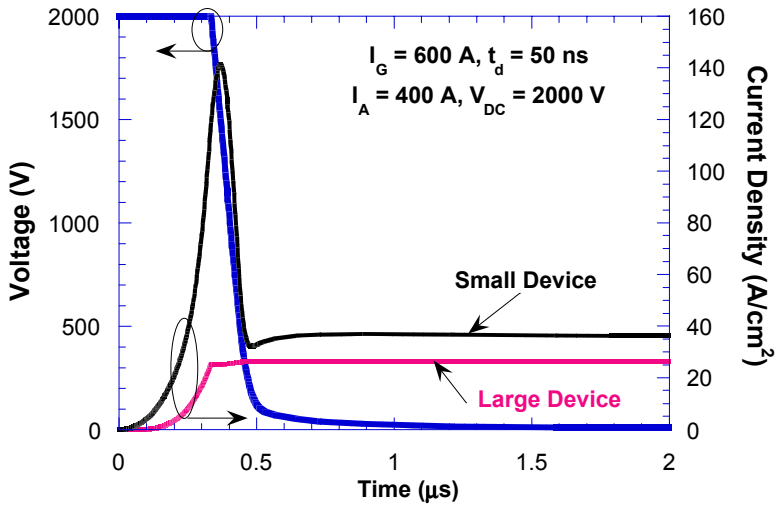



Fig. 3.19. Simulated snubberless turn-on waveforms of two ETOs in parallel.

From the analysis in Section 3.2, the current crowding problem can only be avoided if the GTO cell itself has the current-limiting capability, or an FBSOA. Thyristor operation means that the GTO does not have an FBSOA. However, we know that the NPN and PNP each have an FBSOA. During the turn-on transient, before latch-up, the built-in PNP and NPN transistor of the GTO cell operate temporarily in the active region. Once the gate current pulse is injected, the NPN transistor part of the GTO cell is turned on first. If the NPN transistor performance is dominant during the whole turn-on process (named the transistor-mode turn-on), the snubberless turn-on for the GTO, hence the ETO device, is possible. In other words, using the improved gate drive, if the voltage-current trajectory follows the dashed-line curve in Fig. 3.20, the snubbeless turn-on for the ETO device can be implemented.

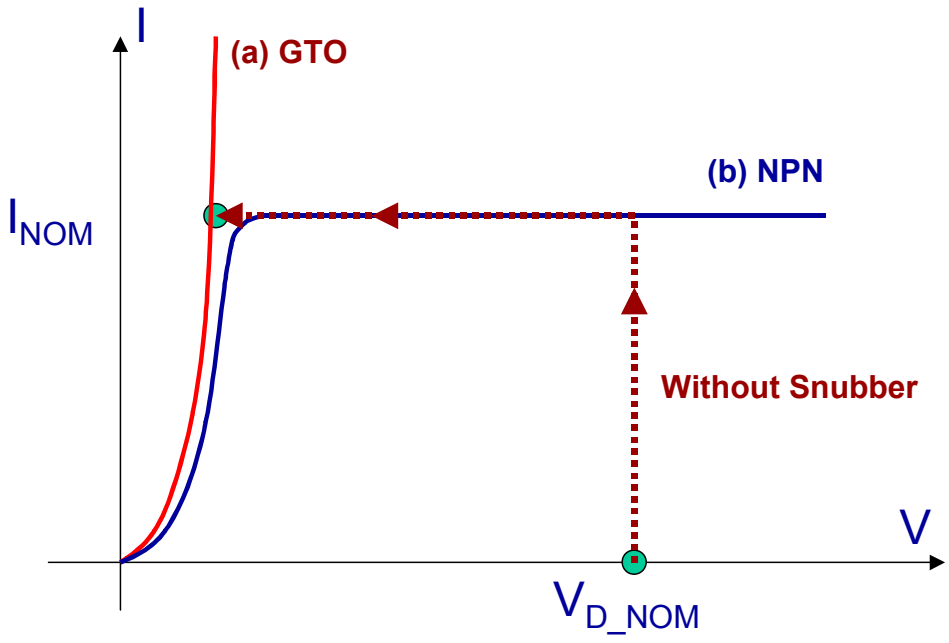



Fig. 3.20. Expected I-V trajectory for symmetrical ETO with improved gate drive during forced turn-on transition.

To further analyze the snubberless turn-on process, a 4.5-kV NPN transistor is simulated to clarify its snubberless turn-on. Compared with the ETO device structure in Fig. 3.15, the NPN device structure is almost the same except that the P+ anode layer of ETO device is replaced with an N+ collector layer, as shown in Fig. 3.21. The NPN device area is 15 $cm^2$, and its simulated on-state I-V curve is shown in Fig. 3.22(a). The collector current will saturate at a level dictated by the NPN common emitter current gain and gate-drive current. Therefore, the collector current for each NPN cell can be controlled by its gate current. The common emitter current gain decreases with the base drive current, as shown in Fig. 3.22(b).

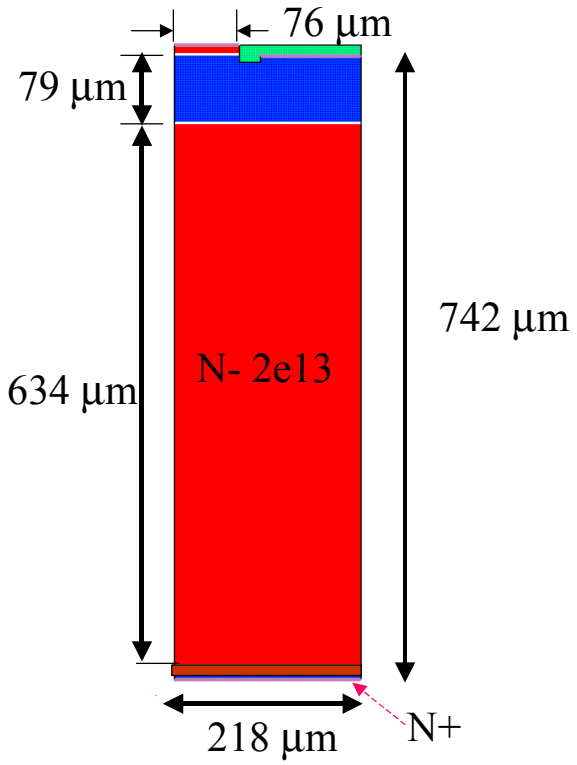
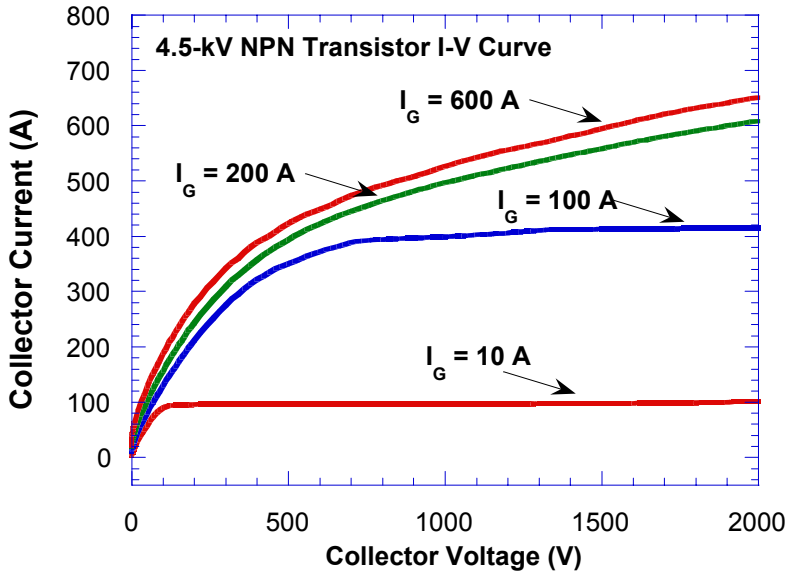
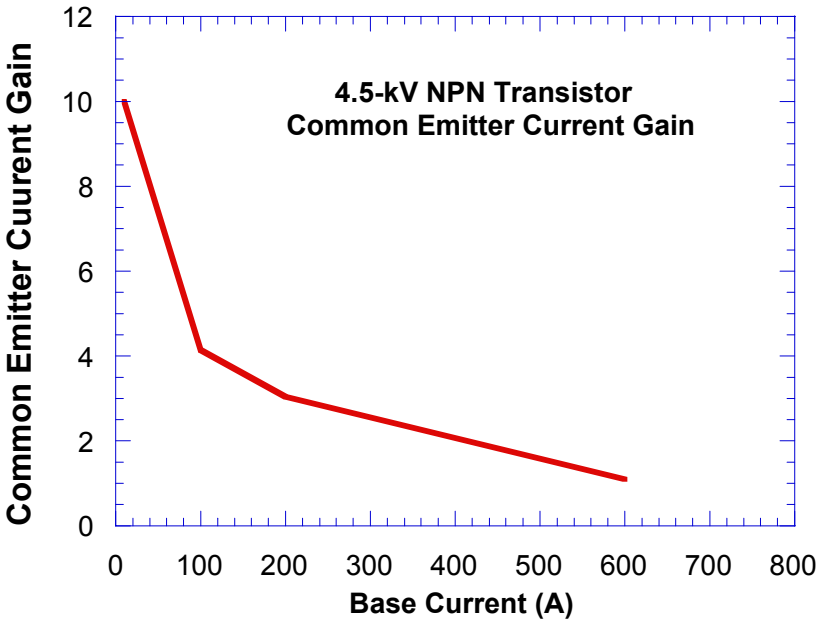



Fig. 3.21. Device structure of the NPN transistor.




(a)




(b)

Fig. 3.22. (a) Simulated on-state I-V curve and (b) common emitter current gain of the NPN transistor.

With the same simulation conditions, the snubberless turn-on process of the NPN device is simulated and compared with that of ETO device, as shown in Fig. 3.23. From the waveforms in Fig. 3.23, after a delay of about 78 ns, the device currents of the NPN and ETO begin to increase at the same rate (about 1.1 kA/μs), implying that the ETO device is operating in the NPN mode. After a delay of about 170 ns, the anode current of the ETO device increases at a higher rate, while the NPN device current rising rate remains almost the same, indicating the latch-up of ETO device. Then, the anode current of the ETO device exponentially rises to the steady-state level, while the NPN transistor maintains its same rate of increase. In the whole snubberless turn-on process, the anode current rising rate of the ETO device can only be controlled by the gate current before latch-up, while the collector current slew rate of the NPN transistor can be totally controlled by the gate current.

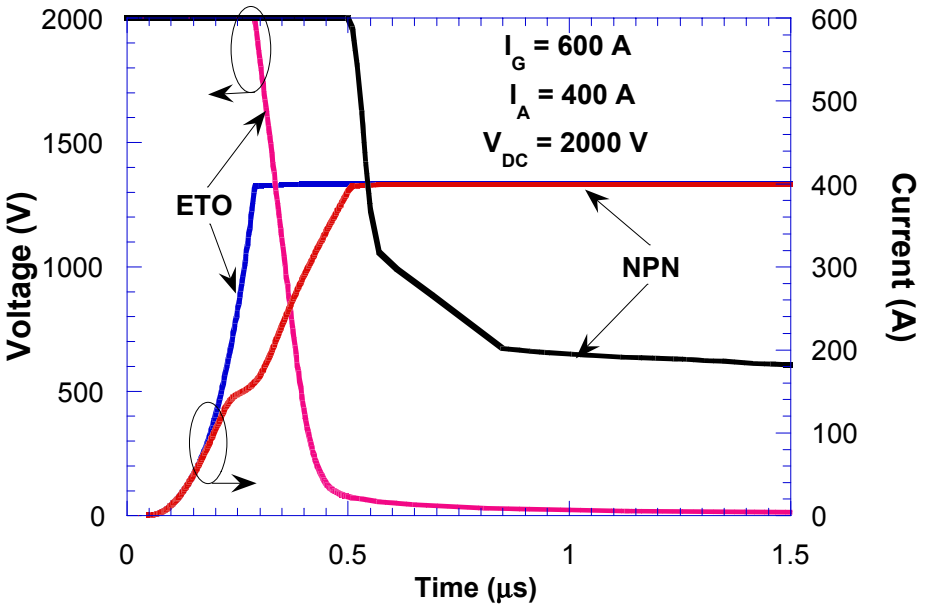



Fig. 3.23. Comparison of snubberless turn-on process between NPN and ETO devices.

With two NPN devices in parallel, the snubberless turn-on process is also simulated to investigate the current filament issue. Once the current density of the early-triggered small NPN device reaches its saturation level (about 33 A/cm$^2$), the current density of the small NPN device increases very slowly and stays almost constant, as shown in Fig. 3.24. So the maximum current density for each NPN cell is controlled by its gate current, which leads to a fairly uniform distribution. Therefore, the current-saturation capability of the NPN device will prevent current crowding during the turn-on transient, thus resulting in the snubberless turn-on capability of the NPN transistor.

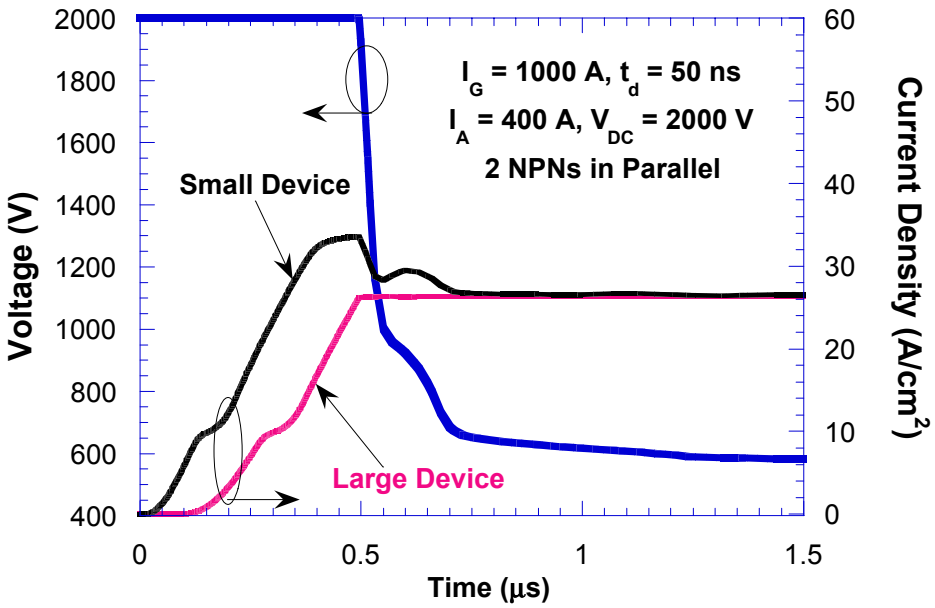



Fig. 3.24. Simulated snubberless turn-on waveforms of two NPNs in parallel.

To achieve transistor mode turn-on for the ETO device, two conditions must be met:

1) The current rising time must be less than the n-base transient time $t_n$ (also defined as the latch-up time); and

2) The saturation current for the built-in NPN transistor in the ETO device must be higher than the steady-state current level.

Condition (1) means that the device current rises to the steady-state level before the thyristor latches up. Condition (2) means that the ETO device current can reach the steady-state value without the thyristor latching up. Once these two conditions are met, the ETO device can be snubberlessly turned on without the thyristor latching up, as in the NPN transistor case.

However, for the high-voltage high-current device in high-power applications, these two conditions are hard to meet.

First, the n-base transient time will reduce dramatically at higher anode current densities since the ohmic field will speed up the transfer of holes through the n-base region. This means that the thyristor latches up sooner than predicted by Equation (3-2), which considers only the diffusion of holes through the n-base region. The simulated n-base transient time (thyistor latch up time) is shown in Fig. 3.25. The higher the gate current, the lower the n-base transient time, until it reaches a saturation value of about 170 ns when the gate current is higher than 300 A.

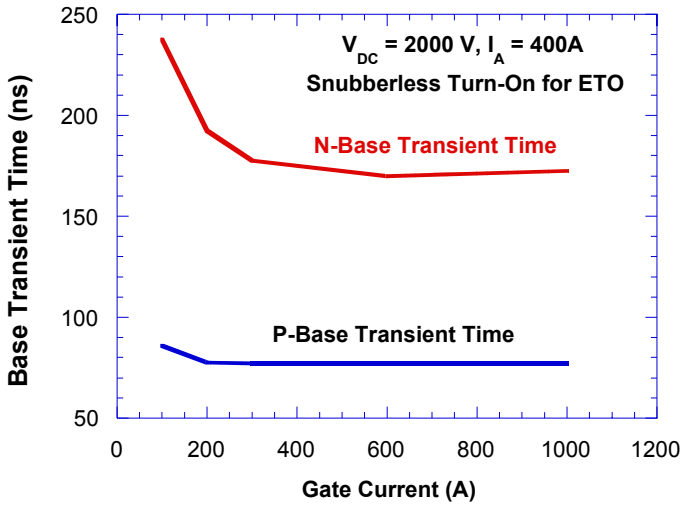



Fig. 3.25. Simulated base transient times for the ETO device in Fig. 3.15.

Second, the current rising rate of the NPN is dictated by the device structure and gate drive current. For the NPN device shown in Fig. 3.21, the current rising rate during the snubberless turn on transient is shown in Fig. 3.26. The higher the gate current, the higher the current rising rate, until it reaches a saturation current rising rate of about 1.1 kA/μs when the gate current is larger than 400 A. If the steady state current level is higher than 200 A, it is very difficult for NPN device shown in Fig. 3.21 to reach the steady state current level during the n-base transient time. So the condition (1) is hard to meet for most high power applications, in which the steady-state current is usually higher than 200 A.

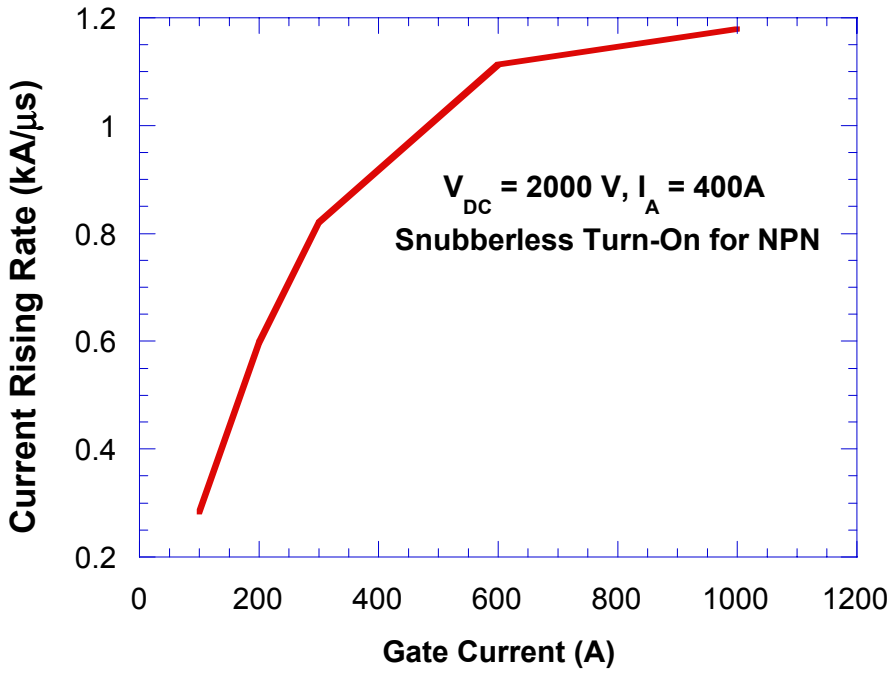



Fig. 3.26. Simulated device current rising rate for the NPN device in Fig. 3.21.

Furthermore, for the high-voltage ETO device, a wide p-base is usually needed for high voltage-blocking capability, so the common emitter current gain of the built-in NPN transistor in the ETO device is usually low. At higher current densities, the current gain will also decrease due to the Ritter effect as well as Kirk effect [A2], as shown in Fig. 3.22(b). So condition (2) is also hard to meet.

In conclusion, it is not easy for the ETO device to be snubberlessly turned on without latch-up. So current crowding is more likely to happen since the current generation of a large-area ETO device does not have current-saturation capability once latch-up. In the case of a snubberless turn on, the anode voltage cannot decrease until the total anode current reaches the steady-state value. Therefore, the instantaneous power loss for the early-triggered cells is probably high enough to cause thermal runaway, resulting in device failure.

To prevent current filamentation during the turn-on transient of today's ETO device, two methods should be adopted simultaneously: the turn-on di/dt snubber should be used; and the gate drive current amplitude and gate current rising rate should be increased. With the two methods mentioned above, the voltage-current trajectory of the ETO can be shaped as the dashed-line curve in Fig. 3.27. In this case, most voltage and current stress happens in transistor mode, resulting in more uniform current distribution even at high device current rising rate during the turn-on transient.

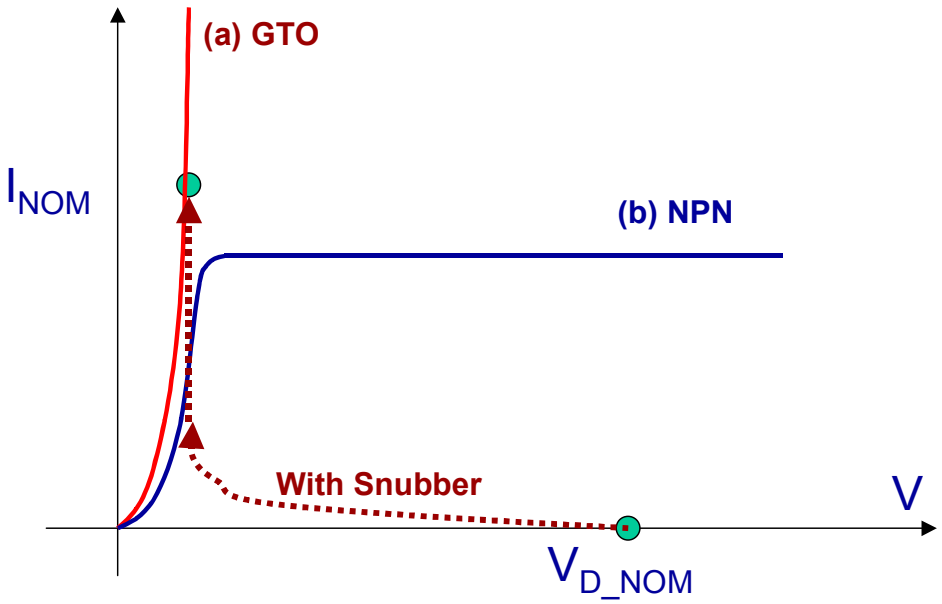



Fig. 3.27. Expected I-V trajectory for the ETO during transistor-mode turn-on with a snubber.

With the di/dt snubber, the total device current rising rate is externally limited. Furthermore, the device voltage can decrease before the device current reaches the steady-state value. The reduced anode voltage will alleviate the current crowding problem. So the instantaneous power loss for the early-triggered cells is reduced.

Using a higher gate drive current with higher slew rate will reduce the latch-up time differences between ETO cells. Since the ETO device current will increase exponentially after latch up, the difference in latch-up time is the key parameter that causes current crowding. Therefore, the reduced latch-up time differences will result in a more uniform current distribution. Besides, the higher gate current will make the device voltage decrease faster. Under this case, the instantaneous power loss for the early-triggered ETO cells during the turn-on transient is lower and easier to maintain within a safe range, even with a higher anode current rising rate.

After latch-up, the plasma spreading speed within ETO cell will increase with the emitter current density [B3]. The higher the gate current, the higher the emitter current density, and so the higher the lateral plasma spreading speed. Therefore, with higher gate current, the critical anode current rising rate is increased, and the required di/dt snubber can be reduced.

## 3.4. The Improved Turn-on Performance of the ETO

The previous analysis revealed that the current generation of large-area ETOs does not have snubberless turn-on capability. However, with a proper di/dt snubber and integrated gate driver, the turn-on performance for the ETO device can be dramatically improved, as compared with that of a traditional GTO. In this section, the improved turn-on performance for the ETO device will be analyzed and experimentally demonstrated.

### 3.4.1. ETO's Turn-On Process with More Uniform Current Distribution

Referring to the ETO's schematic structure shown in Fig. 3.1, thanks to the ETO's low-inductance (about 10 nH) gate loop, a gate current with larger amplitude and rise rate can be more easily applied during turn-on. Through applying a gate-current pulse with higher amplitude, the excess carriers can be accumulated quickly in the p-base and n-base regions during p-base delay time $t_p$. The excess electrons injected from the n+-emitter will diffuse towards junction $J_2$, and will discharge the positive space charge region in the n-base once they have passed through $J_2$. At the same time, holes provided by the gate current will discharge the negative space charge region in the p-base. Before the holes injected from the anode p+-emitter can diffuse through the un-depleted n-base and reach the negative space charge region in the p-base, the $J_2$ space charge region has already been discharged. In other words, the built-in NPN transistor is turned on uniformly within the initial phase, then operates in the active region, quickly

moving across its active region towards the quasi-saturation region before the thyristor latch-up action begins, at which point the anode current increases significantly. Another way to look at this is that the NPN transistor is turned on quickly into the saturation region before the PNP transistor starts to turn on. In this type of turn-on, the charges required to maintain the NPN transistor within the saturation region are provided by the gate drive unit. Little charges are injected from the anode side. In this case, the turn-on delay time $t_{gd}$ is larger than $t_p$ and is less than $t_p+t_n$.

To achieve this type of turn-on, during the delay time $t_d$, the gate current should deliver enough charge to discharge the $J_2$ space-charge region. So the gate current required to uniformly turn on the ETO is given by Equation (3-5).

$$I_G t_{gd} > Q_{GT} \qquad (3\text{-}5)$$

where $Q_{GT}$ is the charge needed to turn on the GTO device and discharge the space charge region. Therefore, Equation (3-6) should be satisfied.

$$Q_{GT} \geq A \cdot W \cdot n^* \cdot q / \gamma_n \qquad (3\text{-}6)$$

where $\gamma_n$ is the $J_3$ emitter injection efficiency, A is the device area, W is the total n-base and p-base width, and n* is a modulated carrier plasma level when the thyristor latch-up begins, which is much higher than the n-base background doping $N_D$. So Equation (3-7) should be satisfied.

$$I_G > A \cdot W \cdot n^* \cdot q / \gamma_n / t_{gd} . \qquad (3\text{-}7)$$

It can be seen from Equation (3-7) that a larger ETO device requires a higher gate current in order to achieve uniform turn-on. The gate current rise rate ($dI_G/dt$) should satisfy the Equation (3-8).

$$\frac{dI_G}{dt} >> \frac{I_G}{t_{gd}} \qquad (3\text{-}8)$$

During the voltage fall phase, the anode voltage collapses quickly, while the anode current stays at a low level, as shown in Fig. 3.28. The anode voltage continues to drop until it reaches a saturation voltage level in spite of the increase in anode current. The turn-on loss is therefore reduced, since there is not much overlap between the anode voltage and current. Under this condition, the GTO is uniformly turned on without current-crowding problems. Therefore, the critical anode current rise rate can be increased. The minimum on-time can also be reduced, since the turn-on process of the GTO in this case is more similar to that of a transistor than it is to a thyristor. Under this condition, the ETO's turn-on performance is greatly improved.

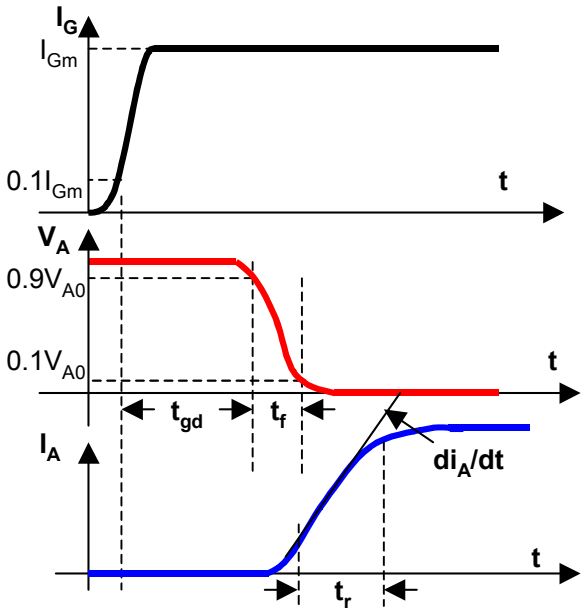


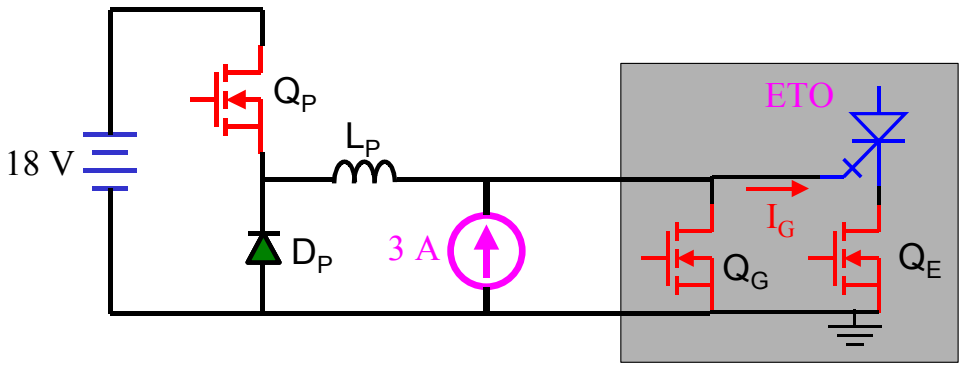

Fig. 3.28. The ETO's uniform turn-on process.

It should be mentioned that at a higher anode current rise rate (which is limited by the external di/dt inductor), an anode voltage bump may occur, indicating either that there is still an unmodulated n-base region, or that the n* level provided by the gate current is still too low. To eliminate this bump, a gate current with an even higher amplitude is required to increase n* in Equation (3-7). In other words, one

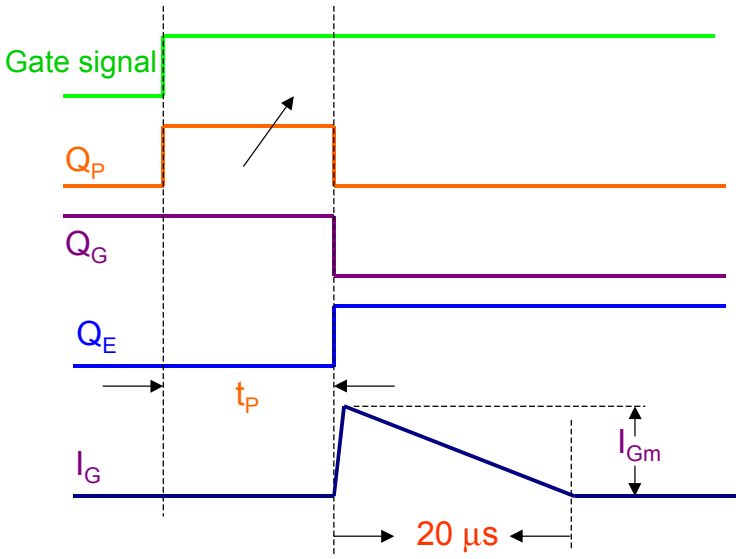
indication of uniform turn-on (this is of course a relative term depending on what $di_A/dt$ is applied) is that the voltage fall phase has no bump during the high current rise phase.

### 3.4.2. The ETO Gate Drive Circuit

The ETO's gate drive circuit and control signals are shown in Fig. 3.29. Following the turn-on command, switch $Q_P$ is turned on and the 18-V voltage source begins to charge inductor $L_p$ through $Q_p$, $L_p$ and $Q_G$. After a charging time $t_P$, $Q_P$ is turned off and the current in $L_p$ freewheels through $Q_G$ and $D_P$. Then, $Q_G$ is turned off and $Q_E$ is turned on. The current in $Q_G$ will be transferred instantaneously to the GTO's gate, since inductor $L_p$ serves as a current source at this moment. The current decrease rate in $Q_G$, which is also the gate current rise rate, is dictated only by the breakdown voltage of $Q_G$ (about 55 V) and the gate loop inductance (about 10 nH). Thus, the gate current rise rate can be as high as 4 kA/μs, which is high enough to uniformly turn on the ETO. Once the current in $L_p$ is totally commutated to GTO's gate, it will freewheel through emitter switch $Q_E$ and diode $D_p$ and will then slowly drop down to zero, as shown in Fig. 3.29(b). By varying charging time $t_P$, gate current pulses with different amplitudes can be obtained and the ETO's corresponding turn-on performance can be characterized.




(a)




(b)

Fig. 3.29. (a) The ETO's gate-drive circuit and (b) control signals.

### 3.4.3. Experimental and Simulation Results

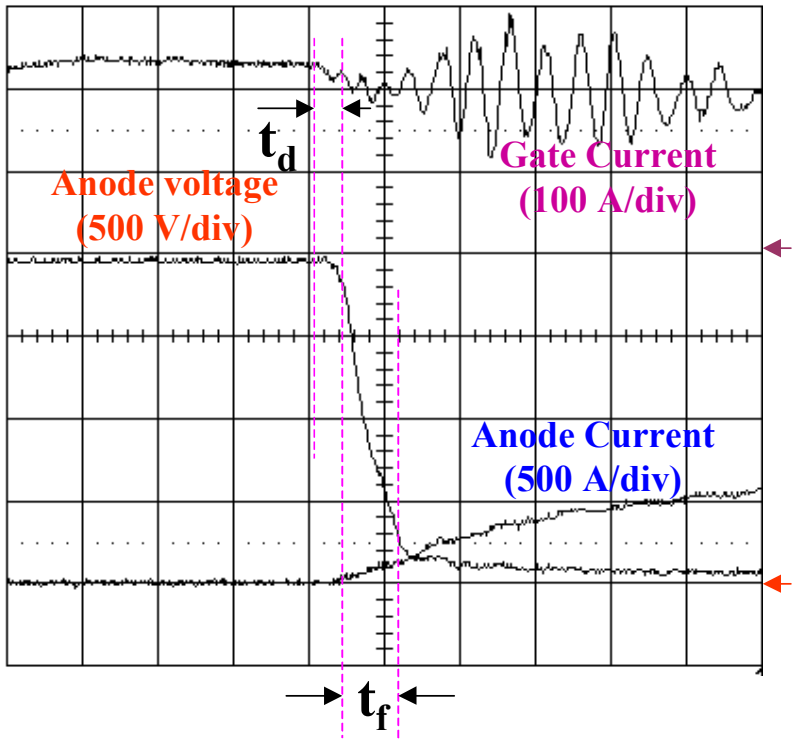
By varying the amplitude of the gate current, the ETO's turn-on performances at different current levels are tested.

Fig. 3.30(a) shows the turn-on waveforms of the 1-kA/4.5-kV ETO1045SW under a gate-current pulse with 200-A amplitude and anode current rise rate of 500 A/µs. Once the gate-current pulse is applied to the GTO's gate, the anode voltage begins to drop within 100 ns. Such a short $t_{gd}$ is another indication of a good turn-on. Then, the anode voltage quickly collapses from 2 kV down to 200 V within 100 ns, in spite of the increase in anode current. Since the anode current is still low at this point, the built-in NPN transistor is turned on into the quasi-saturation region before the thyristor latches up. In this case, the ETO behaves like a transistor instead of a thyristor. So the ETO is turned on with uniform current distribution. The turn-on loss is reduced, and the critical $di_A/dt$ of the anode current can be increased.

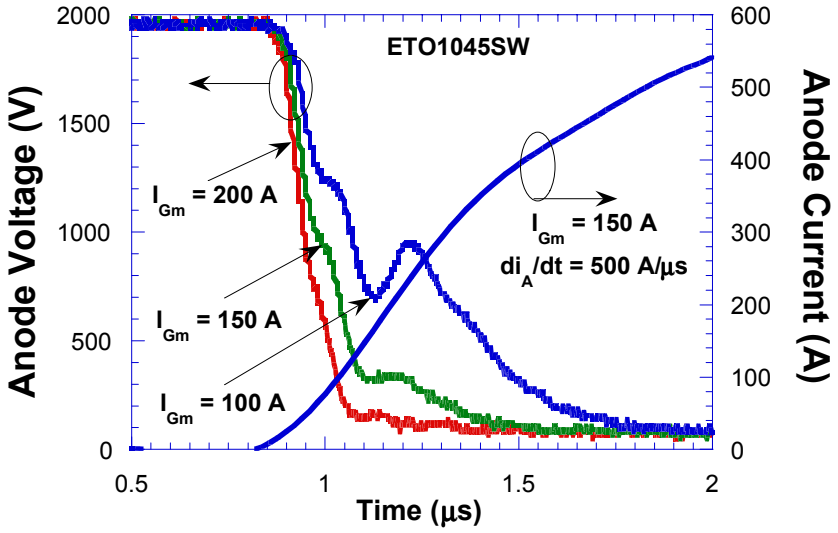
When the gate-current amplitude is reduced to 150 A, the anode voltage collapses quickly at the beginning, but a small shoulder occurs around 350 V, as shown in Fig. 3.30(b). In this case, the reduced gate current and the corresponding injected electrons from the n+-emitter cannot completely discharge the $J_2$ space-charge region before the PNP starts to inject and before the thyristor latches up. A small space charge region is maintained until it is discharged by the increased anode current. As a result, the thyristor latch-up action does not occur simultaneously in all cells. In a manner similar to that of the traditional GTO, the ETO is non-uniformly turned on, and the turn-on loss is increased.

If the gate current amplitude is further reduced to 100 A, the anode voltage has an even higher voltage bump that exists for a longer time, as shown in Fig. 3.30(b). Therefore, to achieve the uniform turn-on of the 1-kA/4.5-kV ETO1045SW (under the 500-A/μs anode current rise rate condition), a gate-current pulse with 200-A amplitude is required.

Calculation using Equation (3-7) for the ETO1045SW will result in a gate current of about 202 A using $n^*=10^{14}$ $cm^{-3}$, $t_d = 0.1\mu s$, $\gamma_n = 0.6$, $A = 15.9$ $cm^2$, and $W = 500$ μm.




(a)




(b)

Fig. 3.30. (a) Turn-on waveforms ($I_{Gm}$ =200 A, Time: 200 ns/div) and (b) turn-on waveforms comparison for the 1-kA/4.5-kV ETO1045SW ($di_A/dt$ = 500 A/µs).

To better understand the uniform turn-on mechanism of the ETO, the turn-on process of a 1-kA/4.5-kV ETO was analyzed with the help of mixed-mode two-dimensional simulations [A7]. With the same gate-drive circuit and turn-on test setup as those used in the experiments, the resulting simulated turn-on waveforms are displayed in Fig. 3.31. Similar to the experimental results, when the gate-current amplitude is 300 A and the anode-current rise rate is 500 A/μs, the ETO's voltage collapses quickly from 2 kV to about 200 V within 200 ns and continues to decrease to the saturation voltage level, as shown in Fig. 3.31. In this case, the ETO is uniformly turned on without current-crowding problems. When the gate current amplitude is reduced to 150 A, the anode voltage drops quickly at the beginning, and a small voltage bump occurs around 1200 V due to the increased anode current. In this case, the ETO is non-uniformly turned on. The voltage decrease time is longer and the anode current increase rate is limited to avoid current filamentation failure.

To achieve more insight into the uniform turn-on process, the carrier distributions at the center of the GTO cell during the turn-on transient (under 300-A gate current amplitude condition) are displayed in Fig. 3.32, with the cathode located at 0.00 μm. As shown in Fig. 3.32(a), the electrons flood the space charge region within 100 ns. However, the holes are delayed by about 200 ns from filling the space charge region, as shown in Fig. 3.32(b). Thus, with the high gate current amplitude (above 200 A) and huge gate current rise rate (about 4 kA/μs), the thyristor latch-up action is delayed about 200 ns, and the transistor-like uniform turn-on of the ETO is achieved.

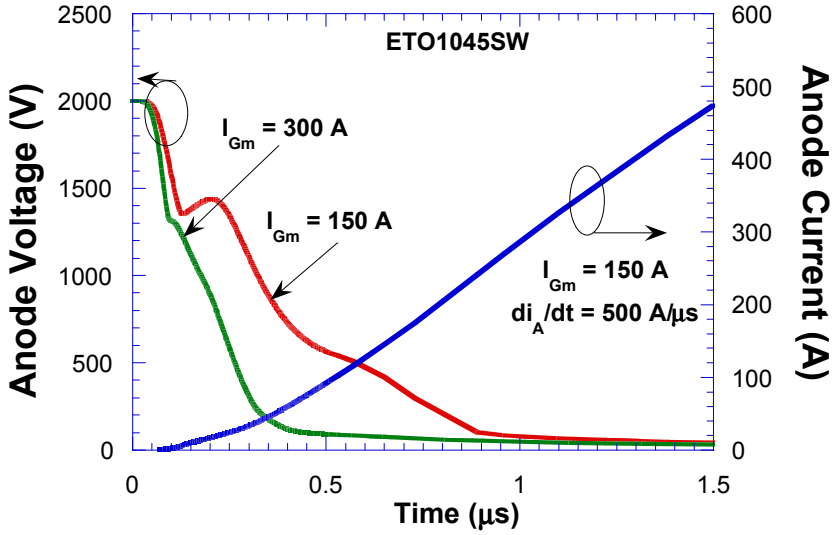
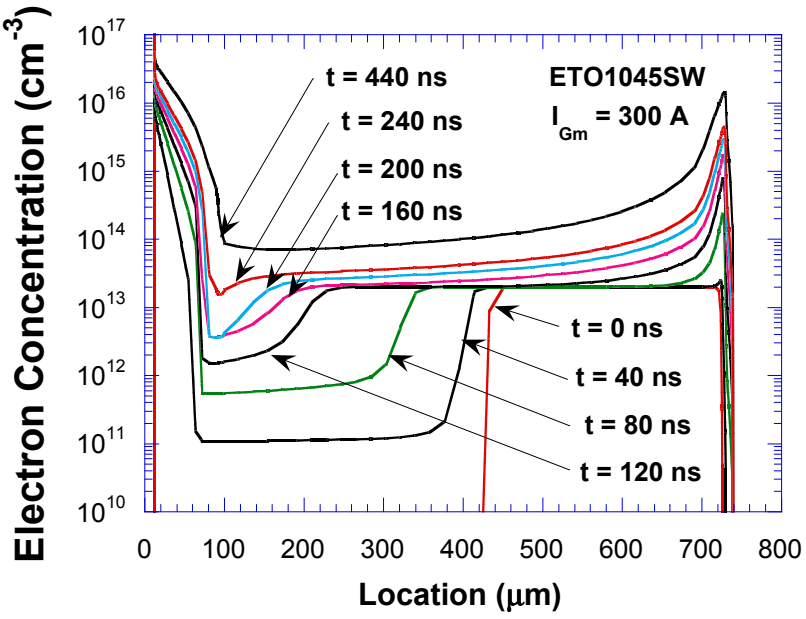
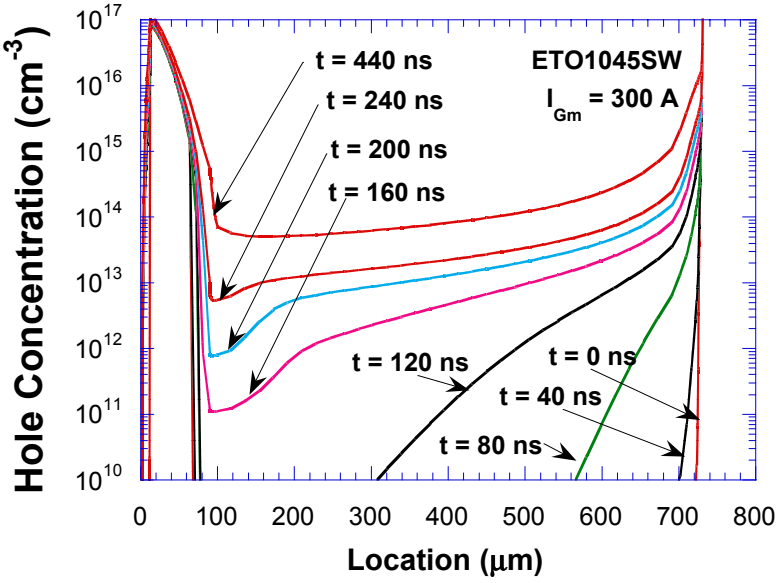



Fig. 3.31. Simulated turn-on waveforms of the 1-kA/4.5-kV ETO1045SW.



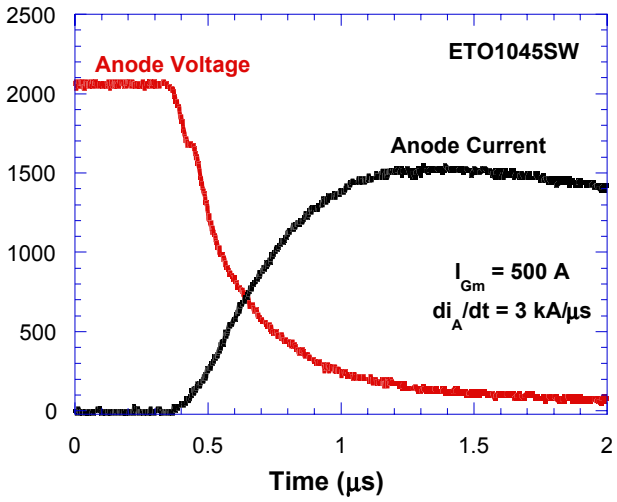

(a)



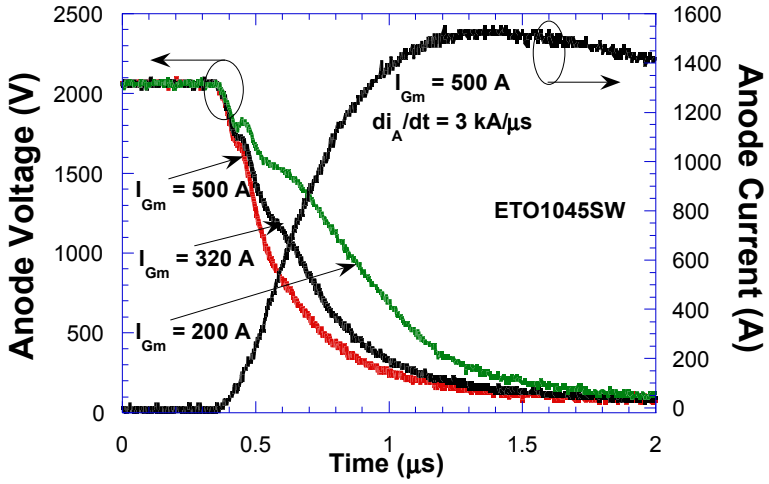

(b)

Fig. 3.32. The center of the cell of the 1-kA/4.5-kV ETO1045SW during the uniform turn-on transient ($di_A/dt$ = 500 A/μs): (a) electron concentration and (b) hole concentration.

As mentioned before, with a higher anode current rise rate, a gate current with higher amplitude is needed in order to compensate for the fast climbing speed of the anode voltage. When the anode current rise rate is 3 kA/μs, a gate current with 500-A amplitude is needed to uniformly turn on the 1-kA/4.5-kV ETO1045SW, as shown in Fig. 3.33. The minimum on-time is reduced to less than 20 μs, as shown in Fig. 3.34.




(a)




(b)

Fig. 3.33. The 1-kA/4.5-kV ETO1045SW ($di_A/dt$ = 3000 A/µs): (a) turn-on waveforms ($I_{Gm}$ =500 A) and (b) turn-on waveforms comparison.

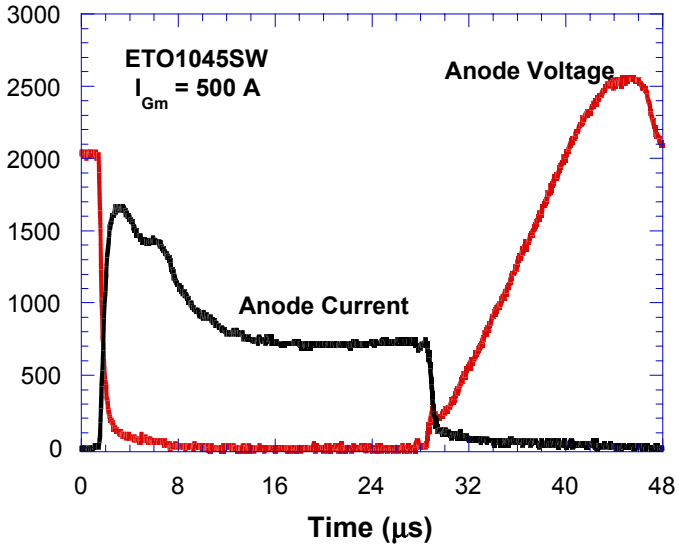
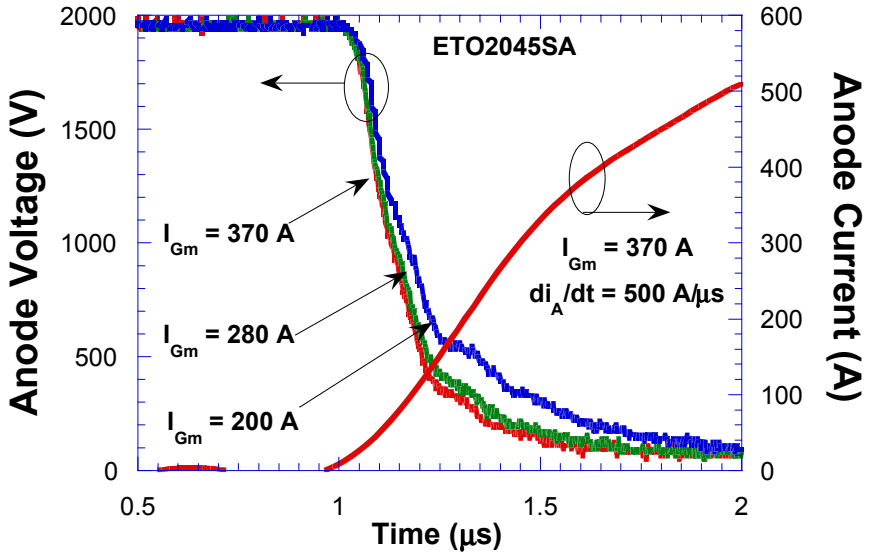
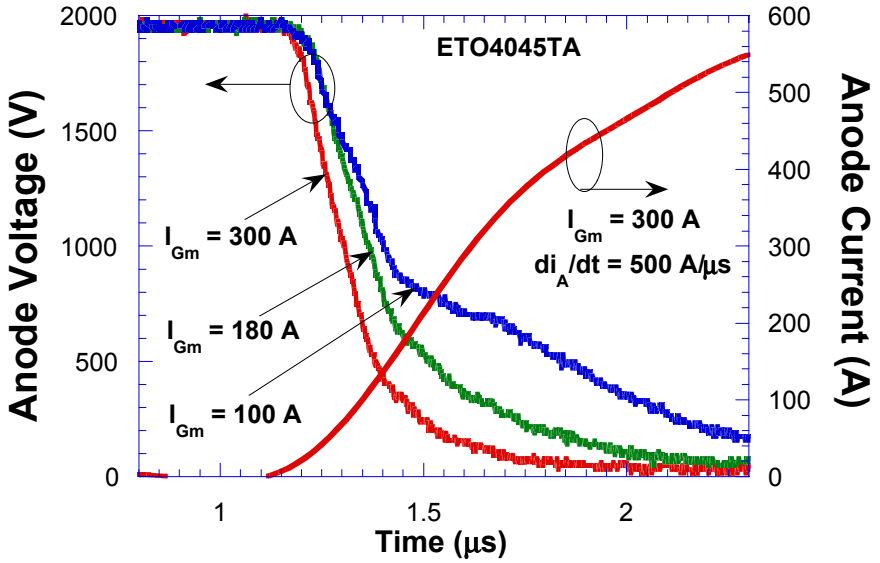



Fig. 3.34. Turn-on and turn-off waveforms ($I_{Gm}$ =500 A) of the ETO1045SW ($di_A/dt$ = 3000 A/µs).

According to Equation (3-7), for a larger-area device, a gate current with higher amplitude is required to achieve uniform turn-on. Fig. 3.35 displays the turn-on waveforms for the 2-kA/4.5-kV ETO2045SA and the 4-kA/4.5-kV ETO4045TA. To achieve uniform turn-on (under the 500-A/µs anode current rise rate condition), gate-current pulses with amplitude of 280-A and 300-A are required.




(a)




(b)

Fig. 3.35. Turn-on waveforms comparison for (a) the 2-kA/4.5-kV ETO2045SA and (b) the 4-kA/4.5-kV ETO4045TA.

## 3.5. Conclusion

The snubberless turn-on capability is preferred for a semiconductor device in a power-conversion system. Thyristor turn-on under the snubberless condition has never before been achieved due to the current filamentation problem that occurs during the turn-on of a large area thyristor device. This chapter analyzes and demonstrates the ETO's FBSOA, which dictates that the snubberless turn-on capability exists in the ETO. Using a self-driven MOSFET as the gate switch, the ETO has excellent current-saturation capability (and hence FBSOA) due to the negative feedback provided by emitter switch $Q_E$. For a large-area ETO, however, the unbalanced negative feedback will intensify the current's non-uniform distribution, thus resulting in current filamentation under high voltage and current saturation conditions. So large-area ETOs are expected to have poor FBSOA. Therefore, the newer generation of ETO is needed to achieve better FBSOA in a large-area device.

Another possible way to turn on the ETO without a snubber is proposed in this chapter. This approach is based on the fact that current crowding problem can be avoided if the device cell has the dynamic current-limiting capability, which can be implemented by driving the GTO cell into the transistor mode through the use of a higher gate-current pulse with higher slew rate. For the ETO device, to achieve transistor-mode snubberless turn-on, two conditions must be meet: the built-in NPN part must provide enough load current under a given gate-drive condition; and the current rising time for the built-in NPN part must be less than thyristor latch-up delay time. The two conditions are hard to meet due to the following: the lower NPN current gain due to due to the wide p-base; and the fact that collector-current rising time is longer than the thyristor latch-up time due to the lower collector-current rising rate, even under very high gate-current conditions. So the current generation of ETO cannot achieve snubberless turn-on capability.

Short of a snubberless turn-on, the ETO's turn-on can be improved using two methods: using a turn-on di/dt snubber; and using a high gate current with high slew rate. With a proper di/dt snubber and integrated gate driver, transistor-mode turn-on can be achieved, and the ETO can be turned on without the current-crowding problem. Correspondingly, the critical anode-current rise rate is improved, and the minimum turn-on time is reduced. These advantages, together with the snubberless turn-off capability and voltage control, make the ETO a very promising device for high-power, high-frequency power electronics systems.

# Chapter 4. Power Stage Design of ETO Based CSC

The power stage design for ETO based CSC is explored. Based on the analysis of the commutation process, the switching performance of the symmetrical ETO in a CSC is analyzed, and the snubber circuit design is presented. To improve the load-commutated turn-off performance of the symmetrical ETO, a novel gate-control scheme with a gate delay time for the on-coming device is proposed and evaluated.

## 4.1. Introduction

In CSCs, the power semiconductor device will block both positive and negative voltages. A typical forced turn-on operation of a switch in a CSC is associated with the load-commutated turn-off process of another switch [B1]. During this commutation, the di/dt is shared by both the on-coming and off-going devices. The off-going device may not withstand high di/dt. For example, a diode may have a turn-off problem, and high turn-off di/dt may over-stress it. If the on-coming device has FBSOA, and hence di/dt controllability, the dI/dt can be limited by the on-coming device through gate control. On the other hand, if the on-coming device does not have FBSOA, a di/dt snubber is needed to prevent the off-going device from undergoing reverse-recovery failure.

The analysis in Chapter 3 reveals that current ETOs have high di/dt capability during turn-on and wide RBSOA during forced turn-off. The future-generation symmetrical ETO with advanced structure will also have excellent FBSOA. So, in a CSC with a future-generation symmetrical ETO, the di/dt snubber can be eliminated, thus achieving complete snubberless commutations. The reverse-recovery performance (load-commutation) can be controlled by the on-coming device. However, the current-

generation ETO does not have FBSOA. Therefore, a di/dt snubber is still needed for a CSC with the current-generation symmetrical ETO.

## 4.2. Commutation Process Analysis and Snubber Design

### 4.2.1. Commutation Process in ETO Based CSC

The typical topology for the ETO based CSC is shown in Fig. 4.1, where $S_1$-$S_6$ are the main switching devices and $C_f$ is the output filter capacitor. As discussed in Chapter 3, the current generation of ETO does not have FBSOA, and hence di/dt snubbers are still needed. Since the symmetrical ETO device has snubberless turn-off capability, the RC dv/dt is not needed. However, it is necessary to absorb the energy stored in the di/dt snubber (inductor) during turn-off and turn-on operations. Therefore, a relatively optimized snubber circuit for the ETO based CSC also uses a small RC snubber across the switch. The RC snubber limits the voltage spike and reduces the switching loss. It also reduces the stress for the device when it undergoes load commutation. The whole snubber circuit for the ETO used in Fig 4.1 is shown in Fig. 4.2, where $L_s$ is the di/dt snubber inductor used to limit the current slew rate; $C_s$ is the dv/dt snubber capacitor used to limit the voltage spike; $R_s$ is the snubber resistor used to limit the capacitor charging and discharging current; and $L_{cl}$ is the voltage clamp loop parasitic inductance, which is dictated by the mechanical structure and can be easily measured [B1].

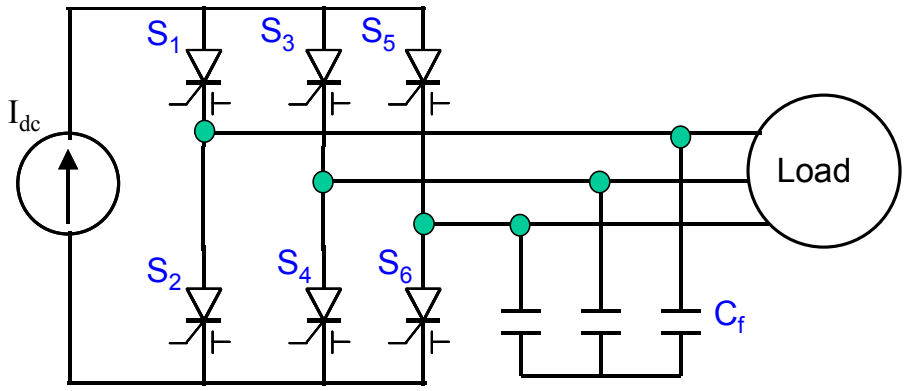



Fig. 4.1. Circuit for the symmetrical ETO based CSC.

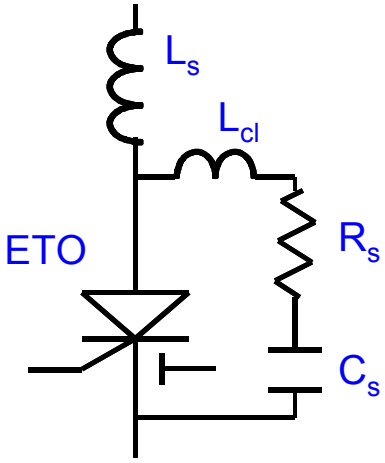



Fig. 4.2. Snubber circuit for the symmetrical ETO used in a CSC.

With the snubber circuit for each ETO device, the topology of CSC shown in Fig. 4.3 can be used to derive the equivalent circuit during commutation process. During normal operation, there are six conduction pairs that operate in sequence to deliver current to the load: $S_1$, $S_2$; $S_2$, $S_3$, $S_3$, $S_4$; $S_4$, $S_5$; $S_5$, $S_6$; $S_6$, $S_1$. The transition from one conduction pair to its subsequent conduction pair requires one device to be commutated off and one device to be turned on. From any conduction pair to its next

conduction pair, the equivalent circuit for the commutation process is identical except for the initial voltage of output filter capacitor ($C_f$). To derive the equivalent commutation circuit, $S_1$ and $S_2$ are chosen as the initial conduction pair with constant current $I_{dc}$ being commutated from $S_1$ to $S_3$. The output filter capacitors can be modeled as constant voltage sources since the voltage across the filter capacitor changes only slightly during the commutation process. Thus, the equivalent commutation circuit can be obtained as shown in Fig. 4.4, where $L_{s1}$, $L_{s2}$ and $L_{s3}$ are di/dt snubber inductors; $C_{s1}$, $C_{s2}$ and $C_{s3}$ are dV/dt snubber capacitors; $R_{s1}$, $R_{s2}$ and $R_{s3}$ are snubber resistors; $L_{cl1}$ and $L_{cl3}$ are voltage clamp loop stray inductances; and $V_{ac}$ and $V_{bc}$ are the initial voltages of the output filter capacitors.

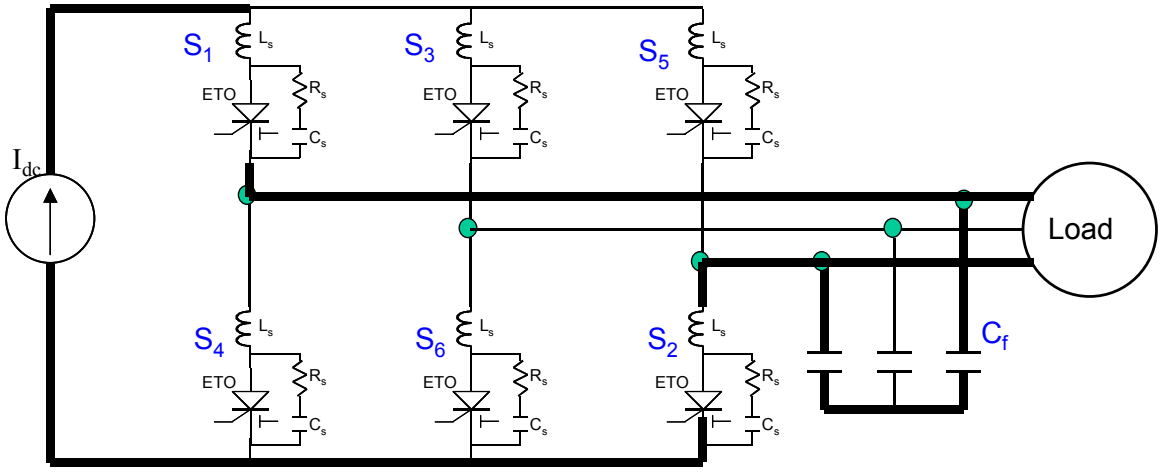



Fig. 4.3. Topology for the ETO based CSC with a snubber circuit.

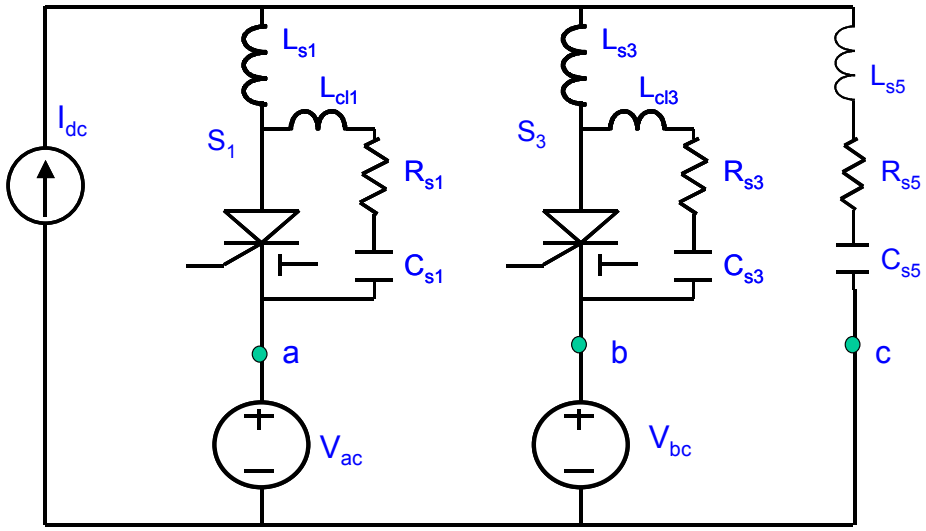



Fig. 4.4. Equivalent circuit for the commutation process in a CSC.

Before the commutation process, $S_1$ is on and $S_3$ is off. So the current conduction path is shown as the thick line in Fig. 3.3. Traditionally, for control simplicity, the firing scheme simultaneously gates on-coming device $S_3$ and off-going device $S_1$, as shown in Fig. 4.5 [B2].

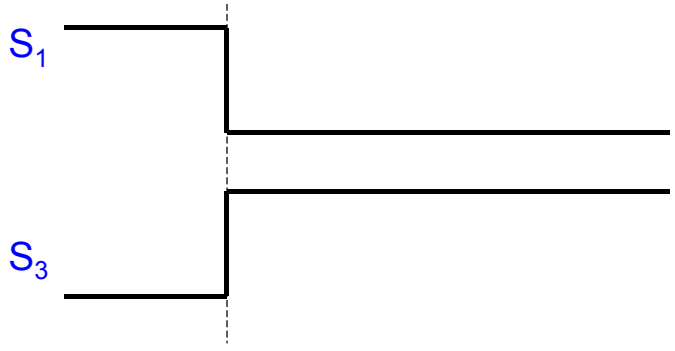



Fig. 4.5. Traditional gating scheme for the ETO based CSC.

By simultaneously applying the turn-off signal to $S_1$ and turn-on signal to $S_3$, the commutation process is initiated. Depending on the initial filter capacitor voltage $V_{ab}$, the current transfer speed and power semiconductor device parameters, there are three commutation modes for the off-going switch $S_1$, listed as follows.

(1) Forced Commutation

$$V_{ab} < 0, \qquad (4\text{-}1)$$

where, $V_{ab}$ is the initial voltage of output filter capacitor across phase a and phase b.

Condition (4-1) means that the snubber capacitor $C_{s3}$ of device $S_3$ is charged to a negative voltage before commutation. When the commutation process begins with $S_3$ being gated on, no current will flow through $S_3$ due to its negative device voltage and unidirectional current capability. At the same time, after storage time $t_s$, the current of the gated-off device $S_1$ will decay at a rate dictated by the device physics. The decayed current in $S_1$ first transfers to its snubber circuit, $R_{s1}$ and $C_{s1}$, resulting in an increase in the device voltage. The increased device voltage across $S_1$ will force the current to be transferred to the snubber circuits in phases b and c, causing an increase in the device voltage across $S_3$ in phase b. Once the voltage across $S_3$ become positive, the current in phase b will flow through $S_3$ instead of through its snubber circuit. This process continues until all the current in $S_1$ (DC-link current $I_{dc}$) is transferred to $S_3$ and the snubber circuits in three phases are charged to the new steady state value. The typical commutation waveforms of the off-going device $S_1$ are shown in Fig. 4.6.

If the di/dt snubber inductor $L_s$ is small, the DC-link current can be uniformly shared by three RC snubbers of three phases at the end of the forced commutation process. Under this condition, for the off-going device $S_1$, the peak device voltage can be approximated as follows:

$$V_s = V_{ab} + \frac{I_{dc}}{3} \cdot \sqrt{\frac{L_s}{C_s}} \quad , \quad (4\text{-}2)$$

where $V_{ab}$ is the initial voltage of the output filter capacitor across phases a and b, $I_{dc}$ is the DC-link current, $L_s$ is the snubber inductor, and $C_s$ is the snubber capacitor.

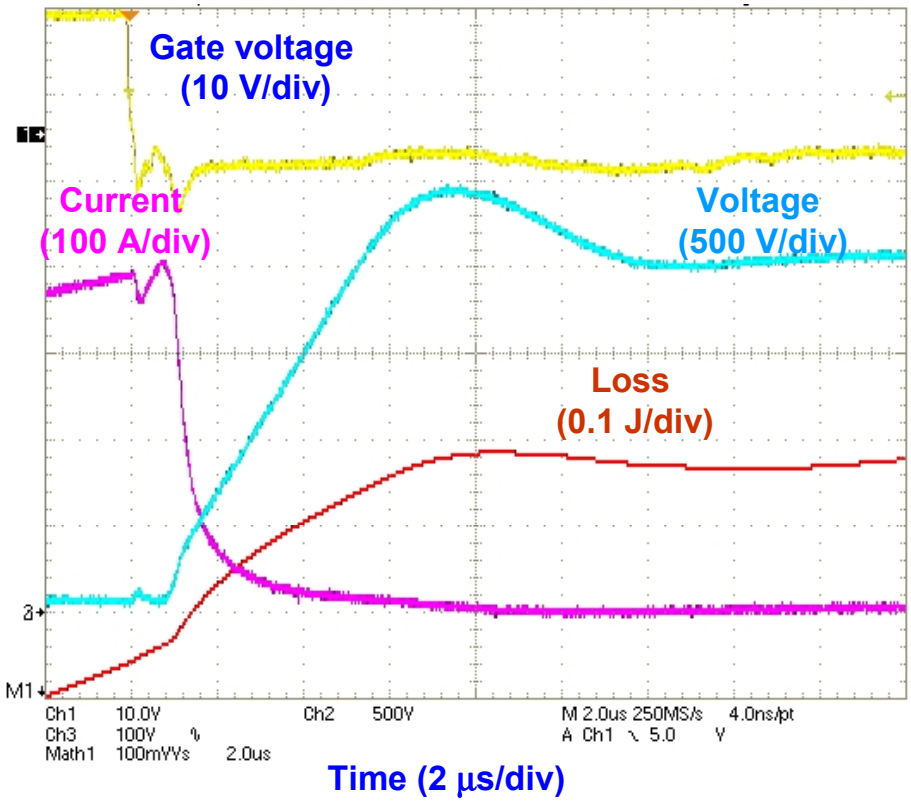



Fig. 4.6. Forced-commutation waveforms for ETO0865D.

(2) Load commutation

$$V_{ab} > 0 \qquad (4\text{-}2.a)$$

$$t_{gt} + \frac{I_{dc}}{\frac{V_{ab}}{2L_s}} < t_s \qquad (4\text{-}2.b)$$

where $V_{ab}$ is the same as that defined in Equation (4-1); $t_{gt}$ is on-coming device turn-on time, which is an interval from the time at which the turn-on gate signal is applied to the time at which the device voltage falls to 5% of its initial value; $t_s$ is the storage time of the off-going device, which is an interval from the time at which the turn-off gate signal is applied to the time at which the device current begins to decrease; $I_{dc}$ is DC-link current; $V_{ab}$ is initial voltage of the output filter capacitor and $L_s$ is the di/dt snubber inductance.

In this case, the on-coming device $S_3$ is fully on before the current of off-going device $S_1$ begins to decrease.

For the off-going device $S_1$, the turn-off process is purely load-dependent. During the turn-off transient, little or no current is transferred to the snubber circuit, so the device voltage will not increase in a positive direction. The whole turn-off process is similar to the reverse-recovery of a diode. In this case, the off-going device will experience severe stress, especially when the output filter capacitor voltage is high. A di/dt snubber is usually needed to limit the rate of fall of the anode current below a critical value, which is dictated by the off-going symmetrical ETO device. The dv/dt snubber will limit the reverse voltage spike to make sure the device operates within the RBSOA, which is defined as the maximum voltage and current boundary within which the device can turn off safely. Furthermore, the reverse voltage slew rate is also constrained by the dv/dt snubber, resulting in lower levels of reverse-recovery current and reverse-recovery loss.

For the on-coming device $S_3$, after the turn-on delay time $t_d$, the device voltage will collapse at a rate dictated by the device structure, gate drive condition and external circuit. At the same time, the

snubber capacitor $C_{s3}$ will discharge through $L_{cl3}$, $R_{s3}$ and $S_3$. The DC-link current will be transferred from $S_1$ to $S_3$ at a rate limited by $L_1$ and $L_3$. The snubber capacitor $C_{s5}$ will also discharge through $L_3$, $L_5$, $R_{s5}$ and $S_3$. Therefore, the on-coming device $S_3$ experiences a large turn-on current with high slew rate. The di/dt snubber inductor and snubber resistor should be carefully designed to limit the rate of rise of the anode current for symmetrical ETO device below a critical value, thus preventing device from turn-on failure.

In conclusion, during the load commutation, the off-going device will have severe turn-off stress, hile the on-coming device will have high turn-on stress. The typical load commutation waveforms are shown in Fig. 4.7.

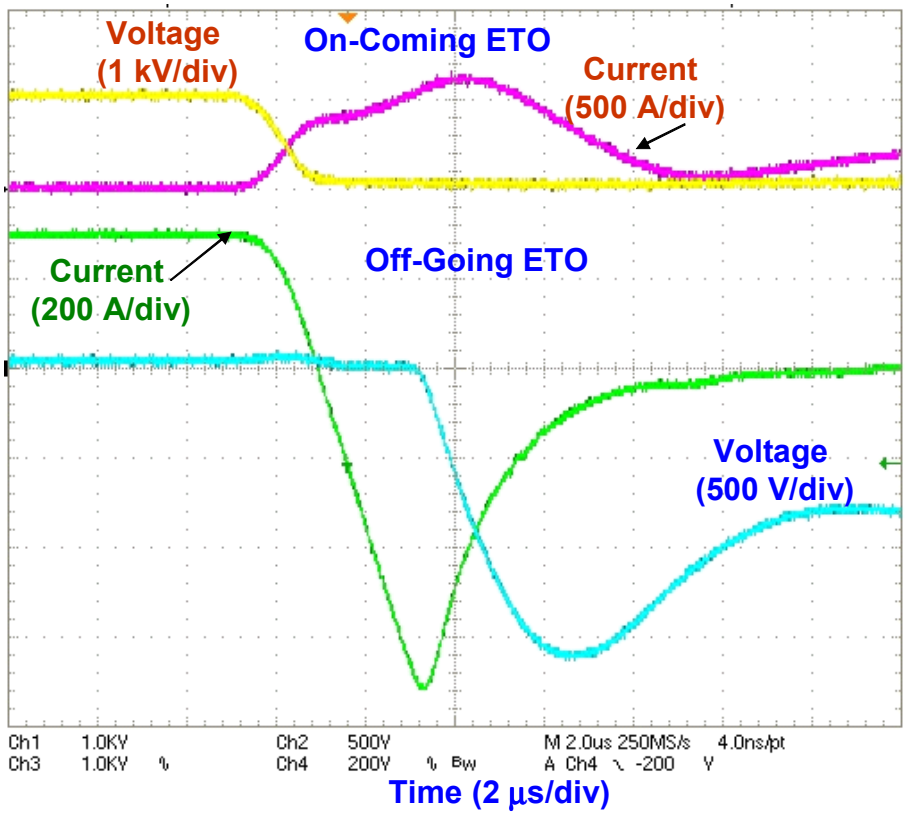



Fig. 4.7. Tested load-commutation waveforms for the ETO0865D.

For the symmetrical ETO, conditions (4-2.a) and (4-2.b) are hard to meet due to the following reasons.

First, the storage time ($t_s$) of the off-going device is small due to the unity-gain turn-off process. For an ETO device, the storage time is higher at low current levels. When the current is beyond 500 A, the storage time is saturated at about 0.9 μs [K8].

Second, for the symmetrical ETO device, the turn-on delay time is about 0.5 μs, and the voltage fall time is about 1.5 μs. The current transfer rate from the off-going device $S_1$ to the on-coming device $S_3$ is limited by the maximum device reverse-recovery current slew rate, which is usually low (below 500 A/μs). So it is usually difficult to transfer the entire DC-link current from the off-going device to the on-coming device within the storage time.

For higher levels of DC-link current, the storage time is shorter and the current transfer time is longer, so the device current will not be totally commutated to the on-coming device when the storage time ends. Then, the remaining device current will fall at a rate dictated by the device physics. The commutation process in this case contains both of forced and load-commutation processes.

(3) Combination of Forced and Load commutations

$$V_{ab} > 0 \text{ , and} \qquad \text{(4-3.a)}$$

$$t_{gt} + \frac{I_{dc}}{\frac{V_{ab}}{2 L_s}} > t_s \text{ ,} \qquad \text{(4-3.b)}$$

where $V_{ab}$, $t_{gt}$, $I_{dc}$, $L_s$ and $t_s$ are the same as those defined in Equations (4-2.a) and (4-2.b).

In this case, the storage time ends before the entire off-going device current has been transferred to the on-coming device. After delay time $t_s$, the off-going device current decays at a rate dictated by the device physics. Part of the device current is transferred to the snubber circuit, resulting in a positive device voltage. During this period, the turn-off process of the off-going device is similar to that in the forced-commutation case. When the on-coming device is fully on, the snubber capacitor $C_{s1}$ of the off-going device will be discharged through $L_1$, $L_3$ and $S_3$ until $S_1$ blocks the reverse voltage ($-V_{ab}$). During this period, the turn-off process of the off-going device is similar to that in the load-commutation case. However, since both the device current and storage charge in the off-going device are fairly low when the reverse voltage is applied, the reverse-recovery stress of the off-going device is much lower, resulting in a higher reverse current di/dt capability. So the off-going device will experience both the forced commutation and the load commutation during the turn-off process.

When condition (4-3.a) is satisfied, once the on-coming device $S_3$ is gated on, after a turn-on delay time, the voltage of the on-coming device will collapse within the turn-on time $t_{gt}$. At the same time, the snubber capacitor $C_{s3}$ will discharge through $L_{cl3}$, $R_{s3}$ and $S_3$; Snubber capacitor $C_{s1}$ will discharge through $L_1$, $R_{s1}$, $L_3$ and $S_3$; Snubber $C_{s5}$ will also discharge through $R_{s5}$, $L_5$, $L_3$ and $S_3$. This process continues until all DC-link current is transferred from $S_1$ to $S_3$ and all snubber voltages reach new steady state values. The coming on device will experience higher turn-on current with high slew rate due to the discharging of the snubber capacitors from other phase legs. The typical switching waveforms for this combined commutation are shown in Fig. 4.8.

The previous analysis show that the off-going device will have the highest turn-off stress during the load commutation. For the on-coming device, the highest turn-on stress happens during the combination of forced commutation and load commutation.

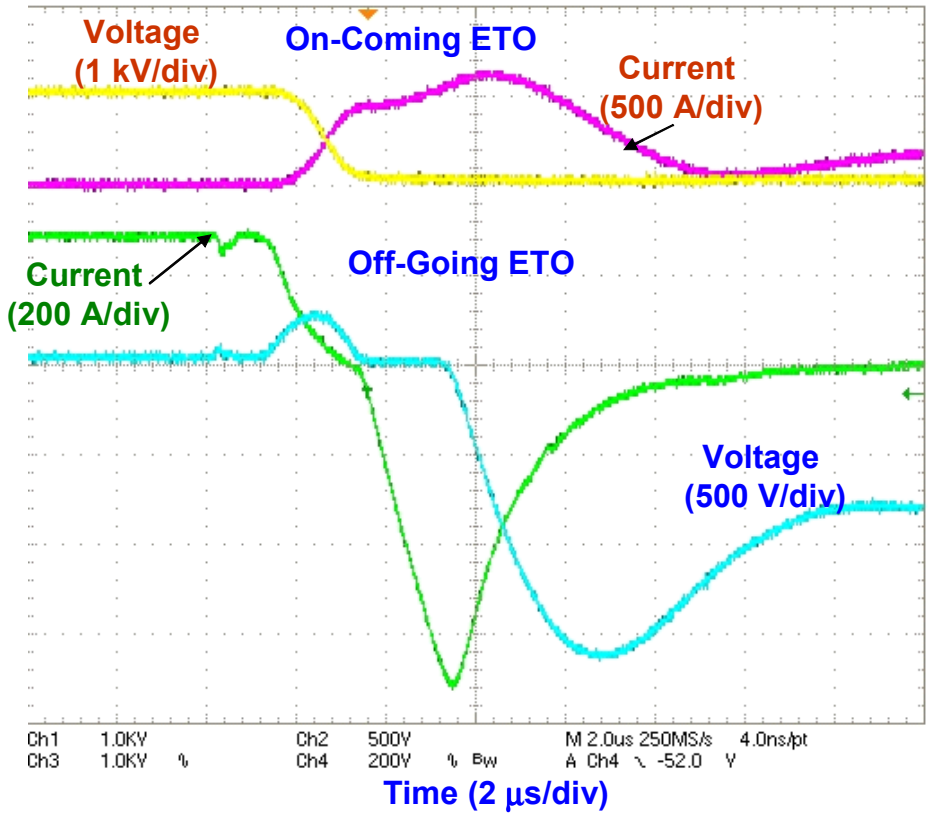



Fig. 4.8. Test waveforms for combination of the forced and load commutations based on the ETO0865D.

### 4.2.2. Snubber Circuit

The snubber circuit for the ETO device in the CSC is shown in Fig. 4.2. There are three basic snubber components: snubber capacitor $C_s$, snubber resistor $R_s$ and snubber inductor $L_s$. The snubber capacitor will limit the dv/dt as well as the voltage overshoot during the forced turn-off and reverse-recovery. $R_s$ will limit the charging as well as discharging currents for snubber capacitors, and it also provides proper damping in the snubber circuit. $L_s$ will limit both the turn-on di/dt for the on-coming device and the reverse current di/dt for the off-going device.

The following criteria for snubber circuit design must be met:

- The maximum device forward voltage should be below the device forward-blocking voltage
- The maximum device reverse voltage should be lower than the device reverse-blocking voltage
- The RC time constant must be small enough to allow the charging and discharging of snubber capacitors, with short pulse widths during normal PWM operation mode
- Proper damping in the snubber circuit must be provided
- The peak charging and discharging currents should be limited to a safe value
- The snubber resistor must have proper levels of loss
- The maximum turn-on di/dt must be lower than the critical di/dt of the on-coming device
- The maximum reverse di/dt must be lower than the critical reverse di/dt of the off-going device

During the forced turn-off process, the off-going device will simultaneously experience high-voltage and high-current stresses, depending on the snubber design. With some couplings among snubber circuits in three phases, the peak voltage for the off-going device can be approximated using Equation (4-4).

$$V_{s\_\max} = V_D + \frac{I_{dc}}{3} \cdot \sqrt{\frac{L_s}{C_s}} \qquad (4\text{-}4)$$

where $V_{S\text{-}max}$ is the maximum device voltage, $V_D$ is maximum output filter capacitor voltage between two commutation phases, $I_{dc}$ is the DC-link current, $L_s$ is snubber inductance, and $C_s$ is the snubber capacitance.

During the load-commutation process, the off-going device will support reverse voltage with the corresponding reverse-recovery current. To limit the maximum reverse-recovery current, snubber

inductor $L_s$ is used to constrain the maximum rate of fall of the anode current and the snubber inductor $L_s$ can be calculated through Equation (4-5).

$$L_s = \frac{V_D}{2 \cdot \frac{di_R}{dt}} \qquad (4\text{-}5)$$

where $V_D$ is maximum output filter voltage between two commutation phases, $di_R/dt$ is the critical rate of fall of the anode current for the symmetrical ETO device, and $L_s$ is snubber inductance for each device.

The peak reverse voltage across the off-going device should also be limited to a safe value that is below the reverse blocking voltage of the symmetrical ETO device. With the RC snubber as shown in Fig. 4.2, the peak reverse voltage can be approximated using Equations (4-6) to (4-10).

$$V_{R\_\max} = V_D(1 + e^{-\delta \cdot \frac{2\beta}{\omega}}) \qquad (4\text{-}6)$$

$$\beta = tg^{-1}\frac{\omega}{\delta} \qquad (4\text{-}7)$$

$$\omega = \sqrt{\frac{1}{L_s C_s} - (\frac{R_s}{2L_s})^2} \qquad (4\text{-}8)$$

$$\omega_0 = \frac{1}{\sqrt{L_s C_s}} \qquad (4\text{-}9)$$

$$\delta = \frac{R_s}{2L_s} \qquad (4\text{-}10)$$

where $V_{R\text{-}max}$ is the maximum device reverse voltage, $V_D$ is maximum output filter capacitor voltage between two commutation phases, $R_s$ is the snubber resistance, $L_s$ is snubber inductance and $C_s$ is the snubber capacitance.

During the load-commutation process, the on-coming device will experience a high turn-on current with high slew rate due to the discharges of the local RC snubber and the remote RC snubbers from other two phases. For local snubber capacitor $C_s$, the snubber resistor $R_s$ will limit the discharge current amplitude, and the clamp loop parasitic inductance $L_{cl}$ will limit the discharging current slew rate. For discharging the local RC snubber, the peak discharging current $I_{on\_max}$ can be approximated using Equation (4-11). To totally discharge the local snubber capacitor, the minimum on-time $t_{on(min)}$ can be estimated using Equation (4-12).

$$I_{on\_\max} = \frac{V_D}{R_s} \qquad (4\text{-}11)$$

$$t_{on\_\min} = 3R_s \cdot C_s \qquad (4\text{-}12)$$

For the 6.5-kV/800-A symmetrical ETO device ETO0865D characterized in chapter 2 with improved turn-on performance, the absolute maximum ratings are as follows:

- Critical rate of rise of on-state current $di_T/dt$ = 2 kA/μs
- Critical rate of fall of anode current $di_R/dt$ = 200 A/μs
- Repetitive peak off-state voltage $V_{DRM}$ = 6500 V
- Repetitive peak reverse voltage $V_{RRM}$ = 6500
- Repetitive peak controllable on-state current $I_T$ = 1500 A

To apply this 6.5-kV/800-A symmetrical ETO in a CSC, the recommended operation conditions are:

- Maximum filter capacitor voltage $V_D$ = 3000 V
- DC-link current $I_{dc}$ = 400 A

- Critical rate of the fall of anode current $di_R/dt = 200$ A/μs
- Maximum device voltage during forced turn-off $V_{DM} = 4500$ V
- Maximum device voltage during reverse-recovery $V_{RM} = 4500$ V

According to Equations (4-4) to (4-12), the designed snubber parameters are as follows:

- $L_s = 7.5$ μH
- $C_s = 0.5$ μF
- $R_s = 2$ Ω

With the designed snubber circuit, the forced turn-off and load commutated turn-off waveforms for the 800-A 6.5-kV symmetrical ETO (ETO0865D) are shown in Fig. 4.6 and Fig. 4.9, respectively. The forced turn-off switching is very fast due to the unity-gain turn-off, resulting in much lower turn-off switching loss than that achieved in the load-commutation case, as shown in Fig. 4.10. In the CSC, the off-going ETO device will experience both the forced- and load-commutation processes. The relatively poor reverse-recovery performance of the symmetrical ETO contributes most of the switching loss and limits the device switching frequency; this results in lower system efficiency and slow dynamic response. The poor reverse-recovery performance also requires a larger di/dt snubber inductor, which will cause more snubber loss and voltage overshoot during the switching transient. To fully utilize the improved forced turn-off and active turn-on performances of the symmetrical ETO device, the reverse-recovery performance of the symmetrical ETO must be improved.

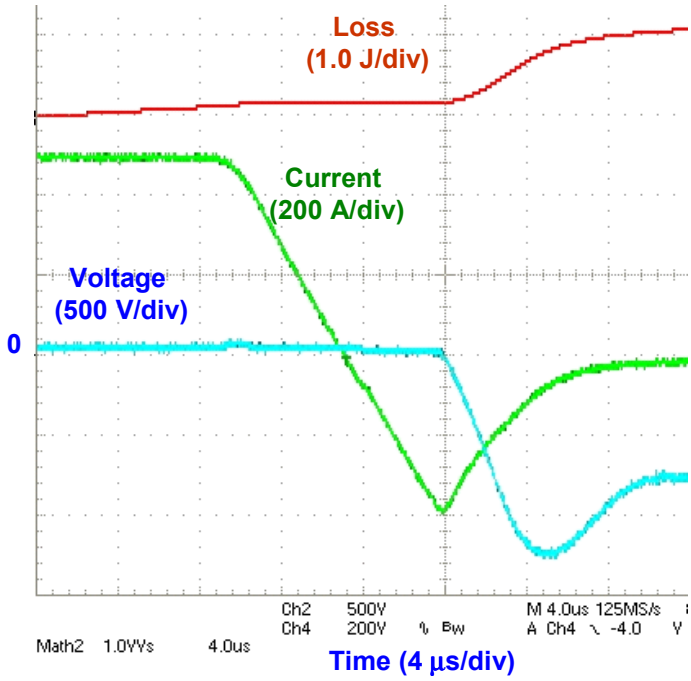



Fig. 4.9. Tested load-commutation waveforms for the ETO0865D with RC snubber.

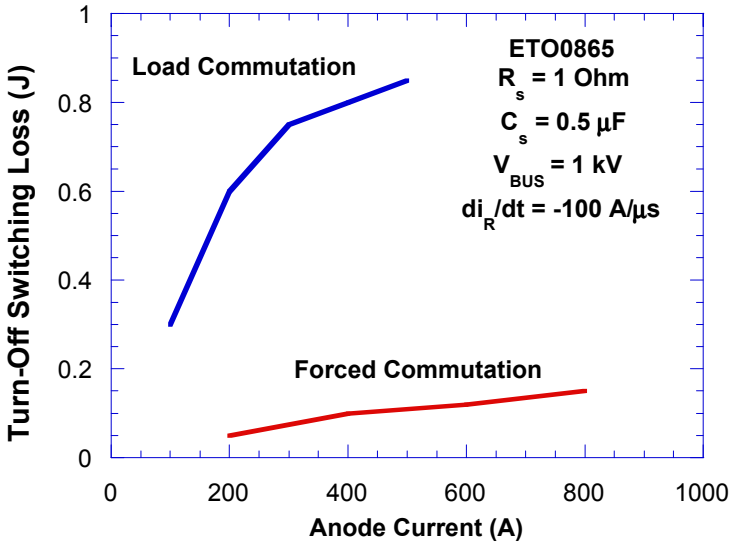



Fig. 4.10. Turn-off switching loss comparison for ETO0865D.

### 4.2.3. Switching Performance for Symmetrical ETO Using Proposed Gating Scheme

Due to the compact gate driver, the symmetrical ETO has very fast forced turn-off speed and superior active turn-on capability. Potentially, these merits make the symmetrical ETO a very good candidate for applications in CSCs. However, the relatively poor reverse-recovery performance will prevent the symmetrical ETO from fully utilizing its advantages in a CSC. To maintain the symmetrical ETO within its safe operation area during reverse-recovery, a larger di/dt snubber has to be used, resulting in a high voltage spike during the forced turn-off and higher levels of snubber loss. The switching frequency is mainly limited by the reverse-recovery loss for the symmetrical ETO, since its forced turn-off loss is only about 20% of its reverse-recovery loss, as shown in Fig. 4.10. In conclusion, the reverse-recovery performance of the symmetrical ETO has become the bottleneck for high speed switching and thus needs to be improved.

To improve the reverse-recovery performance of the symmetrical ETO, two methods can be used. First, the symmetrical GTO part of the symmetrical ETO is optimized for both forced turn-off and reverse-recovery performance, as in the symmetrical GCT case. Second, a soft-switching technique is used to reduce the forward conduction current to zero before applying the reverse voltage, resulting the less storage charge and hence improved reverse-recovery performance. This section mainly focuses on the second method.

In a CSC, due to the di/dt snubber inductance and parasitic stray inductance, the RC snubber is needed for symmetrical ETO to limit the voltage spike during turn-off transient. For the off-going device $S_1$, the forward conduction current can be reduced by first triggering off the device and shifting the device current to its RC snubber. When most or all of the anode current in the off-going device $S_1$

is transferred to its RC snubber, the on-coming device $S_3$ is gated on and the off-going device $S_1$ begins the reverse-recovery process with little or no forward current. The gating scheme in this case is shown in Fig. 4.11, where $t_d$ is the delay time needed to trigger the on-coming device.

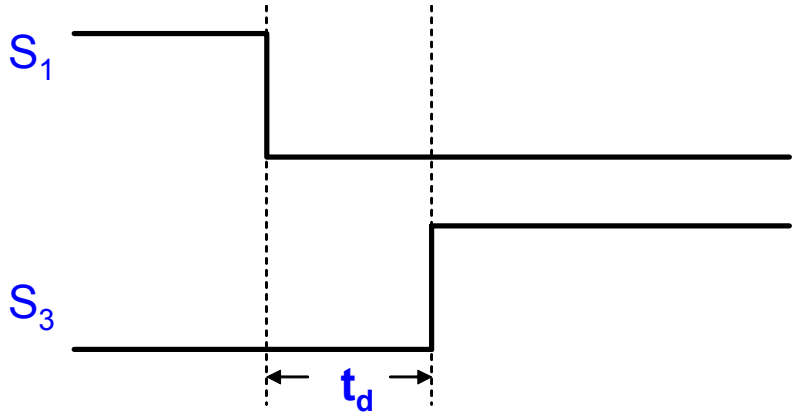



Fig. 4.11. Proposed gating scheme.

Using the proposed gating scheme, after the turn-off storage time, the anode current of the off-going device $S_1$ will decrease. Since the current in the snubber inductor cannot be changed instantaneously, the decreased anode current in $S_1$ will be transferred to its RC snubber circuit, resulting in an increase in the device forward voltage, as shown in Fig. 4.12. The anode voltage of the off-going device keeps increasing until the on-coming device is gated on after a delay time $t_d$. Once the on-coming device is gated on, the current in the RC snubber of $S_1$ will be transferred to the on-coming device, resulting in a decrease in the anode voltage of $S_1$. When the anode voltage of off-going device reduces to zero, the off-going device begins its reverse-recovery process. The reverse-recovery current slew rate as well as peak reverse-recovery current are limited by the di/dt snubber. The reverse dv/dt is constrained by the RC snubber, causing less reverse-recovery loss.

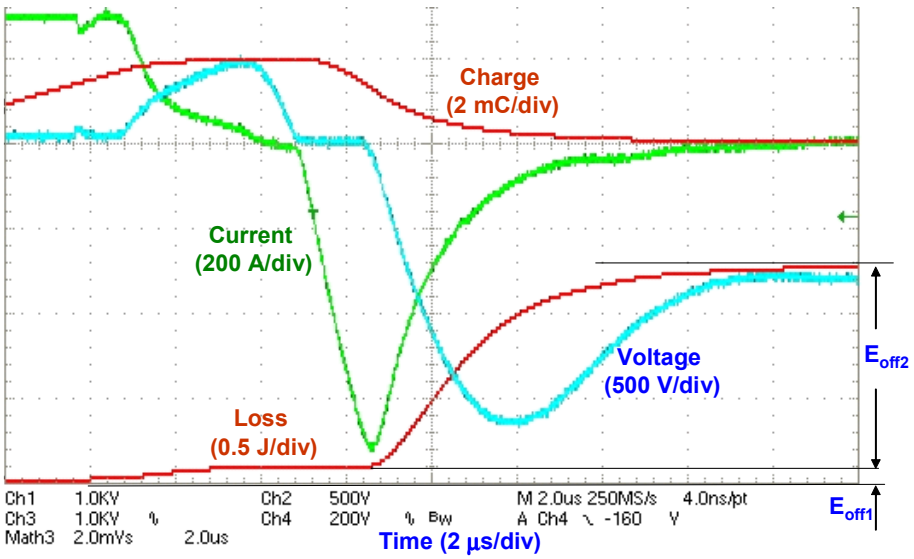



Fig. 4.12. Reverse-recovery waveforms for the ETO0865 ($t_d$ = 3 µs).

To compare the effect of the delay time $t_d$ on the reverse-recovery performance, a similar test is conducted without any delay on triggering the on-coming device, and these reverse-recovery waveforms are shown in Fig. 4.13. Although the peak reverse-recovery current remains the same (about 720 A) in the two cases, the storage charge is about 20% less in the case with the 3-µs delay, as shown in Fig. 4.14. During this kind of reverse-recovery process, with the increase of delay time $t_d$, the forced turn-off loss ($E_{off1}$) will increase and the load-commutated turn-off loss ($E_{off2}$) will decrease, resulting in almost constant total turn-off loss $E_{off}$, as shown in Fig. 4.15.

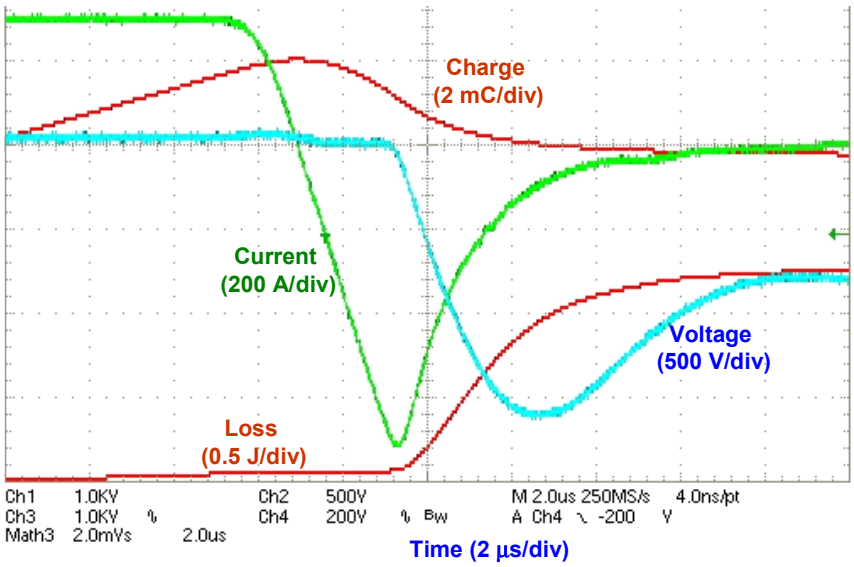



Fig. 4.13. Reverse-recovery waveforms for the ETO0865 ($t_d$ = 0 µs).

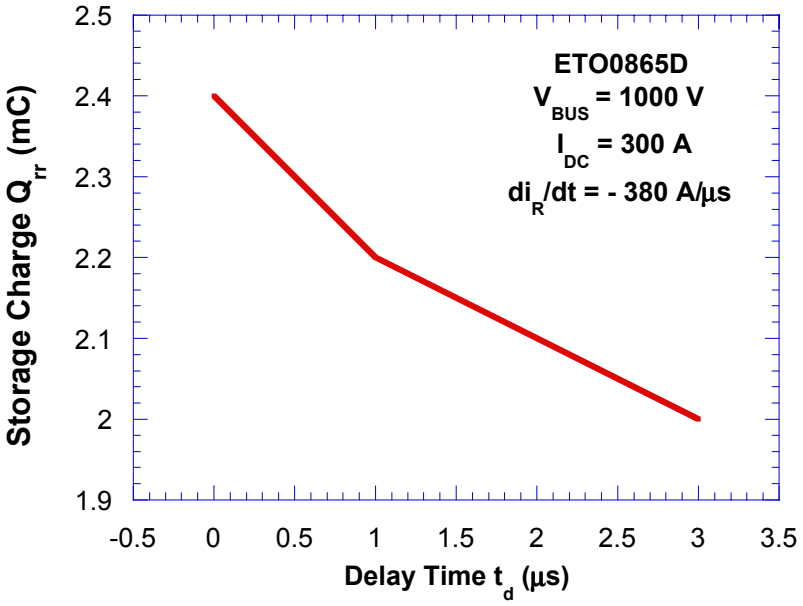



Fig. 4.14. Storage charge for the ETO0865 during reverse-recovery.

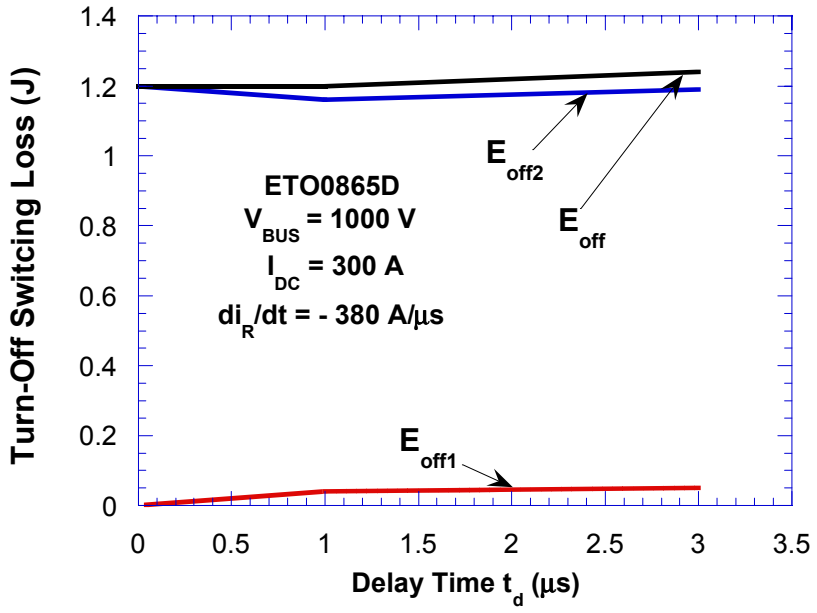



Fig. 4.15. Turn-off loss for the ETO0865 during reverse-recovery.

Since the forced turn-off process only recovers the forward-blocking junction $J_2$ of the off-going device, a further increase of delay time $t_d$ has little effect on the reverse-recovery performance, which is mainly dictated by the characteristics of the reverse blocking junction $J_3$, as shown in Fig. 2.12 in Chapter 2. Also the longer delay time will cause more voltage overshoot on the RC snubber circuit, resulting in more voltage stress and snubber loss. So the $t_d$ should be chosen in the range of device forced turn-off time.

## 4.3. Power Stage Design for ETO Based CSC

Due to the snubberless turn-off capability, low conduction loss, and the reverse voltage blocking capability, the symmetrical ETO device is suitable for use in a CSC. Shorting the reverse voltage blocking

capability, the asymmetrical ETO can also be used in a CSC when it is in series with a diode. Under normal operation conditions, the power semiconductor devices must operate within their safe operation areas to prevent device failure due to electrical stress. At the same time, the junction temperature of the power semiconductor devices should be kept with a safe region in order to meet the thermal and reliability requirement. The purpose of power stage design is to fully utilize the power semiconductor devices in order to achieve the maximum output power with required power quality.

To show the power stage design guidelines, the 4-kA/4.5-kV asymmetrical ETO (ETO4045TA) in series with a 1.9-kA/4.5-kV fast recovery diode (5SDF13H4501) is used as the symmetrical switches in the ETO based CSC, as shown in Fig. 4.16. According to the device parameters, the recommended operation conditions from the standpoint of electrical limitation are:

- Maximum filter capacitor voltage $V_D$ = 2800 V
- DC-link current $I_{dc}$ = 2000 A
- Critical rate of fall of anode current $di_R/dt$ = 400 A/μs
- Maximum device voltage during forced turn-off $V_{DM}$ = 4000 V
- Maximum device voltage during reverse-recovery $V_{RM}$ = 4000 V

Referring to the design guidelines for the snubber circuit described in the previous section, the designed snubber parameters are as follows: $L_s$ = 3.5 μH; $C_s$ = 1.0 μF; $R_s$ = 1.5 Ω.

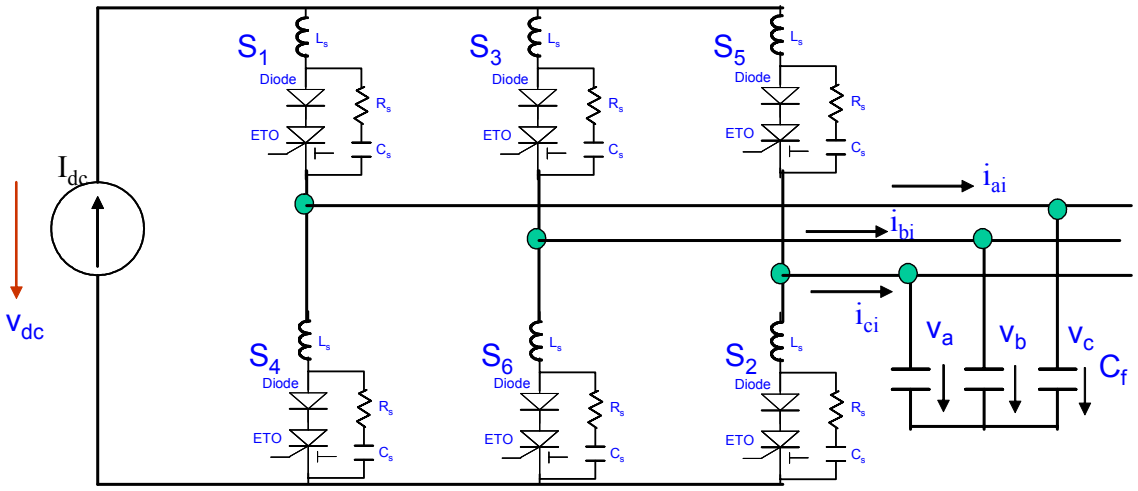



Fig. 4.16. ETO based CSC with snubber circuit.

The tested on-state voltages of the 4-kA/4.5-kV ETO at different temperatures are shown in Fig. 4.17. Correspondingly, the relationship between on-state voltage $V_F$ and on-state current $I_A$ at junction temperature of $T_j$ can be linearly approximated using Equation (4-13).

$$V_F(I_A, T_j) = (0.921 - 2.42 \cdot 10^{-3} T_j) + (6.96 \cdot 10^{-4} + 1.38 \cdot 10^{-6} T_j) \cdot I_A \quad (4\text{-}13)$$

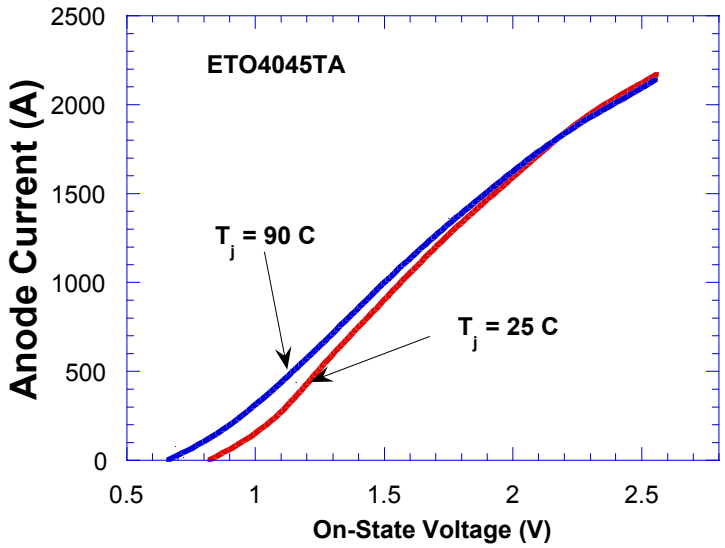



Fig. 4.17. Tested on-state voltage of 4-kA/4.5-kV ETO (ETO4045TA).

In a CSC, the DC current-source will flow through two ETOs at any time. So the average conduction loss $P_{loss\_on}$ for each ETO with current $I_{dc}$ at junction temperature $T_j$ can be calculated using Equation (4-14).

$$P_{loss\_on}(I_{dc}, T_j) = \frac{2I_{dc} \cdot V_F(I_{dc}, T_j)}{6} \quad (4\text{-}14)$$

where, $V_F$ is the on-state voltage and can be calculated using Equation (4-13).

Using the snubber circuit shown in Fig. 4.16, the tested forced turn-off losses for the ETO device at different temperatures are shown in Fig. 4.18. Based on the test results, to turn off a device current of $I_A$ under a bus voltage of $V_{DC}$ at the junction temperature of $T_j$, the turn-off loss $E_{off}$ can be linearly approximated using Equation (4-15).

$$E_{off}(I_A, V_{dc}, T_j) = (0.00305 I_A - 0.3) \cdot (0.33 + 0.333 \cdot 10^{-3} V_{dc}) \cdot \left[1 + 0.313 \cdot 10^{-2} \cdot (T_j - 25)\right] \quad (4\text{-}15)$$

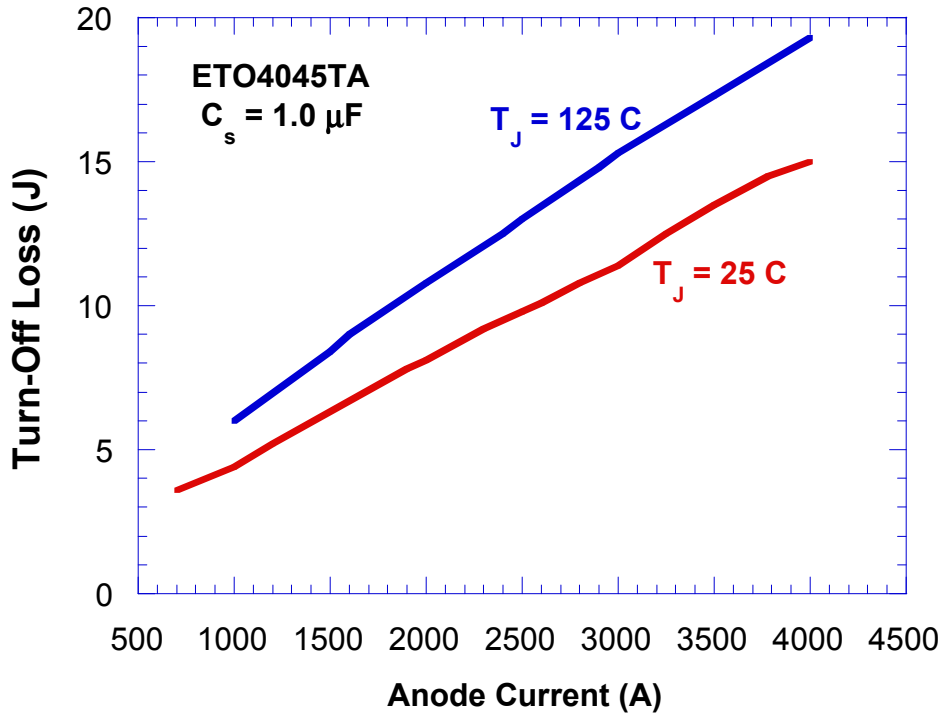



Fig. 4.18. Tested turn-off switching loss of the 4-kA/4.5-kV ETO (ETO4045TA).

In the CSC as shown in Fig. 4.16, each asymmetrical ETO device will switch during half of the fundamental cycle with positive voltage stress. The other half of the fundamental cycle with negative voltage stress will be applied to the series diode. Therefore, to turn off a device current of $I_{dc}$ at junction temperature $T_j$, the average switching loss $E_{off\_avg}$ for the asymmetrical ETO can be calculated using Equation (4-16).

$$E_{off\_avg}(I_{dc}, V_m, T_j) = \frac{1}{2\pi} \cdot \int_0^{\pi} E_{off}(I_{dc}, V_{ab}(V_m, \alpha), T_j) d\alpha \quad (4\text{-}16)$$

where, $V_m$ is the peak output line voltage and $V_{ab}$ is the sinusoidal output line voltage as shown in Equation (4-17).

$$V_{ab}(V_m, \alpha) = V_m \cdot \sin(\alpha) \quad (4\text{-}17)$$

Due to the improved turn-on performance and the use of the di/dt snubber, the turn-on loss for the ETO device is much smaller than its turn-off loss, and can be neglected in the loss analysis. Therefore, for a given switching frequency $f_{sw}$, the switching loss can be approximated using the turn-off loss, as shown in Equation (4-18), and the total device loss $P_{loss\_total}$ is described in Equation (4-19).

$$P_{off}(I_{dc}, V_m, T_j, f_{sw}) = f_{sw} \cdot E_{off\_avg}(I_{dc}, V_m, T_j) \quad (4\text{-}18)$$

$$P_{loss\_total}(I_{dc}, V_m, T_j, f_{sw}) = P_{loss\_on}(I_{dc}, T_j) + f_{sw} \cdot E_{off\_avg}(I_{dc}, V_m, T_j) \quad (4\text{-}19)$$

When the ETO device is double side cooled with a water flow rate of about 1 GPM, the thermal resistance from the heat sink to the water is about 7 K/kW and the thermal resistance from the junction to the water, $R_{thjw}$, is about 23.5 K/kW, as shown in Fig. 4.19.

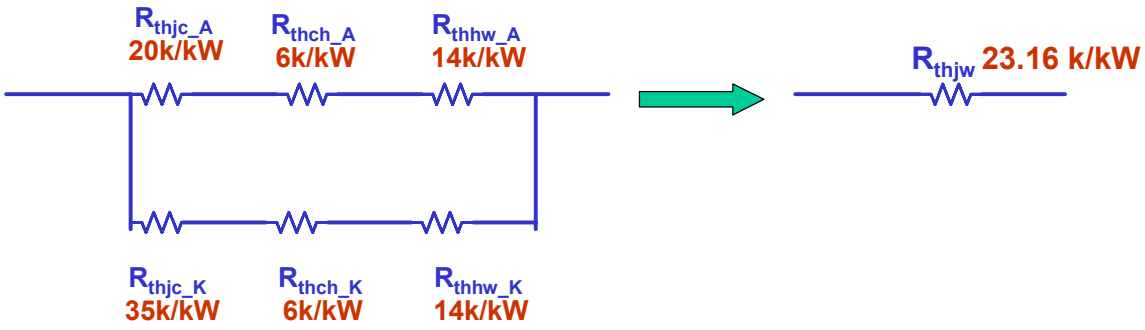



Fig. 4.19. Thermal model for the 4-kA/4.5-kV ETO (ETO4045TA).

When the junction temperature of the ETO device is $T_j$ and water temperature is $T_w$, the total power loss in the ETO ($P_{loss\_total}$) can be calculated using Equation (4-20). Based on Equations (4-19) to (4-20), the switching frequency for a given operation condition can be calculated as shown in Equation (4-21).

$$P_{loss\_total}(T_j, T_w) = \frac{T_j - T_w}{R_{thjw}} \quad (4\text{-}20)$$

$$f_{sw}(I_{dc}, T_j, T_w, V_m) = \frac{\frac{T_j - T_w}{R_{thjw}} - P_{loss\_on}(I_{dc}, T_j)}{E_{off\_avg}(V_m, I_{dc}, T_j)} \quad (4\text{-}21)$$

Since the total power loss is fixed for a given junction temperature $T_j$ and cooling water temperature $T_w$, the higher the DC-link current $I_{dc}$, the higher the conduction loss and the lower the switching loss and switching frequency, as shown in Fig. 4.20. In other words, from the standpoint of thermal limitation, for a given water temperature $T_w$ and switching frequency $f_{sw}$, the DC-link current $I_{dc}$ should be properly designed to maintain the junction temperature $T_j$ within a safe region.

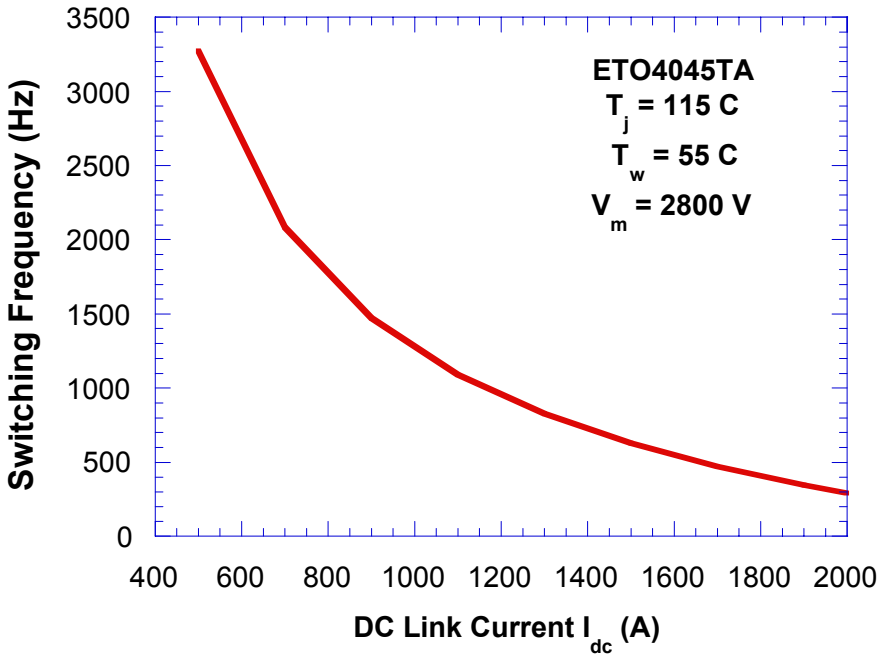



Fig. 4.20. Relationship between DC-link current and switching frequency for the 4-kA/4.5-kV ETO (ETO4045TA).

Based on the snubber circuit designed in the beginning of this section, the peak device voltage $V_{Dm}$ during the forced turn-off transient can be approximated using Equation (4-22), where $V_m$ is the peak output line voltage.

$$V_{Dm}(V_m, I_{dc}) = V_m + \frac{I_{dc}}{3} \cdot \sqrt{\frac{L_s}{C_s}} \qquad (4\text{-}22)$$

To safely turn off the device current of $I_{dc}$, the ETO device should have a maximum repetitive turn-off current $I_{tq}$ that is higher than $I_{dc}$. Usually, $I_{gt} = 2I_{dc}$ is chosen as the design criterion. To prevent device avalanche breakdown, the peak device voltage $V_{Dm}$ should always be kept below the device blocking voltage. Combining the electrical and thermal limitations mentioned above, the operation point for the ETO based CSC could be designed according to the design curve shown in Fig. 4.21. For given

conditions $T_j$ = 115 °C, $T_w$ = 55 °C, $V_m$ = 2800 V, and $f_{sw}$ = 1080 Hz, the DC-link current $I_{dc}$ of 1100 A can be chosen to meet both the thermal and electrical requirement. The DC-link-current rating is mainly thermally limited due to the higher conduction loss in the CSC case.

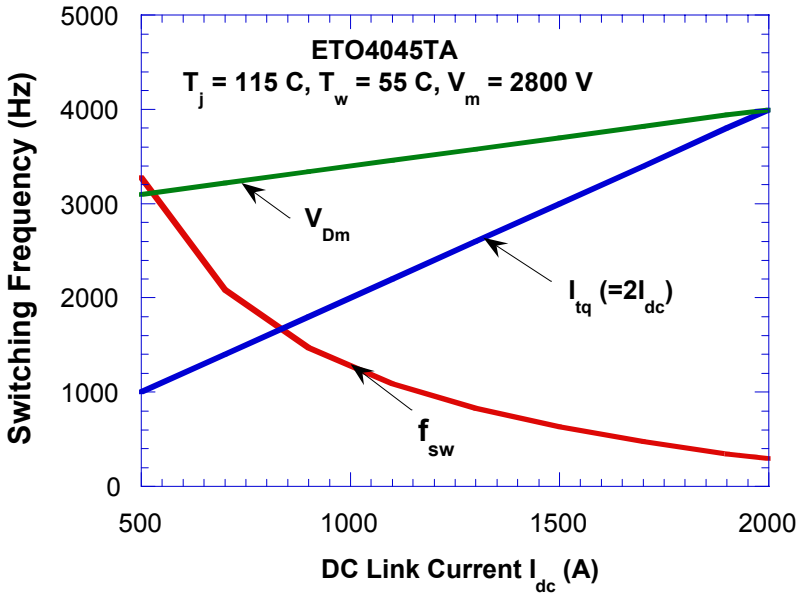



Fig. 4.21. Operation point design curve for the ETO4045TA based CSC.

The output power rating for a CSC depends on the DC-link current ($I_{dc}$) as well as the output line-to-line peak voltage ($V_m$), which is limited by the DC-link voltage rating of the device. The maximum rating ($S_m$) can then be calculated using Equation (4-23). For the previously designed ETO4045TA-based CSC with DC-link current of 1100 A and a maximum AC line-to-line voltage of 2800 V, the maximum achievable power rating is about 2.7 MVA.

$$S_m(V_m, I_{dc}) = \frac{\sqrt{3}}{2} \cdot V_m \cdot I_{dc} \qquad (4\text{-}23)$$

For a CSC based on the 800-A/6.5-kV symmetrical ETO (ETO0865), the design curve can be obtained following the same procedure, as shown in Fig. 4.22. For given conditions of $T_j$ = 115 °C, $T_w$

= 55 °C, $V_m$ = 3600 V and $f_{sw}$ = 1080 Hz, the DC-link current $I_{dc}$ of 217 A can be chosen to meet both the thermal and electrical requirement. Correspondingly, the maximum achievable power rating is about 677 kVA. The power rating for the symmetrical ETO based CSC is mainly thermally limited due to the higher load commutation loss. For CSCs based on other symmetrical ETOs, the power stage design can be performed following similar procedures.

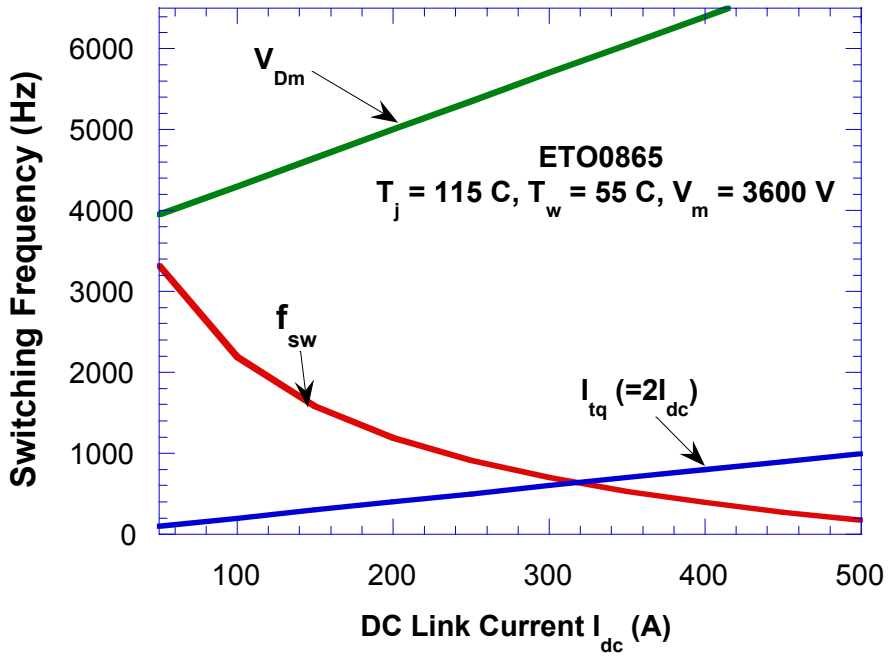



Fig. 4.22. Operation point design curve for the ETO085 based CSC.

Using the traditional CSC topology, to achieve a high power rating, devices must be in parallel or series. With devices in series or in parallel, a complicated balancing circuit and device degrading are needed, resulting in high system cost. Although the power rating can be increased through device-level series or parallel connections, neither the dynamic response nor the harmonics can be improved since the system switching frequency remains the same due to the thermal limitation.

## 4.4. Conclusion

This chapter uses the analysis of the commutation process to analyze the switching performance of symmetrical ETO in a CSC and to investigate the snubber circuit design. Depending on the voltage of the output filter capacitor, the off-going symmetrical ETO device will undergo forced turn-off, load commutated turn-off or a combination of both switching processes. The compact integrated gate driver allows for the snubberless forced turn-off capability and superior forced turn-on capability, both of which make symmetrical ETO a good choice for applications in a CSC. However, the load commutated turn-off capability of the symmetrical ETO is relatively poor, since the reverse-recovery performance of the reverse blocking junction is mainly dictated by the symmetrical GTO part instead of by the gate-drive circuit.

To improve the load-commutated turn-off performance of a symmetrical ETO, a novel gate-control schemes using a gate delay time for the on-coming device is proposed and evaluated. Test results show that the delay time has a limited effect on the reverse-recovery performance of the off-going device. To further improve the reverse-recovery performance, symmetrical GTO device optimization or other soft-switching techniques are needed.

The power stage design for the ETO-based CSC is studied. Using the asymmetrical ETO (ETO4045TA) in series with a diode as the main switch in the multilevel CSC, the operation condition is designed to maximize the output power rating while meeting the electrical and thermal requirements. Given a junction temperature of 115 °C and water temperature of 55 °C, the 4-kA/4.5-kV ETO (ETO4045TA) can operate at 1080 Hz with 1100-A DC-link current and 2.7 MVA maximum output power rating. For a given switching frequency, the DC-link current and the maximum output power rating

are mainly thermally limited due to high conduction loss in a CSC. To achieve high power rating, a device with high voltage rating is preferred.

The power rating can be increased using devices in series or in parallel. However, neither the system dynamic response speed nor the harmonics can be improved in this way. To improve these aspects, a multilevel CSC is needed, as presented in the next chapter.

# Chapter 5. A Novel Multilevel CSC—The Parallel-Cell Multilevel CSC

For high-power applications, such as FACTS devices and energy storage systems, power electronics systems with high voltage, high current, low harmonics and fast dynamic response speed are required. To achieve high voltage and current ratings, The traditional three-level CSC topology employs power semiconductor devices in series and parallel connection. Complicated balancing circuits are required for the proper operation of the series or parallel devices. Device rating degradation is usually also needed. The switching frequency for high power semiconductor devices is usually low, since it is limited by the switching loss in high power applications. Therefore, the harmonics in the output voltage and current are high, and the dynamic response is slow. To limit the harmonics within a standard, an external filter is usually needed that will further reduce the dynamic response speed. Therefore, paralleling converters instead of devices is preferred for high power applications. To further increase the power rating and reduce the harmonics, multilevel converters based on PWM converter cells are developed. The multilevel converter is a trend for high power applications [A3,A6, H7].

For multilevel CSC topology, two kinds of topologies have been developed. One of the multilevel CSCs, called the multiple CSC, has been was proposed [I1]. In the multiple CSC, several CSCs are in a parallel connection to share the same DC-link current through the current-sharing inductors and proper control. The capacity of the multiple CSC can be increased, and the harmonics contained in the output voltage and current waveforms can be reduced through phase-shift PWM control among parallel CSCs. However, to ensure the DC current sharing and to prevent the circulating current among the parallel CSCs, additional current sharing-components and complicated control must be applied .

Another method for achieving the low switching frequency and low harmonic distortion for high-power applications is to apply a generalized current-multilevel cell to CSCs to form multilevel CSCs [I2-I5]. Fewer current sharing inductors are employed as compared with the previous method. In the current multilevel cell based multilevel CSC, the current sharing between active switches relies on their on-state voltages and thus complicated control is also needed. In this topology, the modular design is also not used due to its complicated structure and control.

To solve the problems of the existing multilevel CSCs, a novel multilevel CSC topology, named the parallel-cell multilevel CSC, is proposed and explored in this dissertation. The operation principle, power stage design, modeling, control and switching modulation scheme are analyzed.

## 5.1. Operation Principle of the Parallel-Cell Multilevel CSC

### 5.1.1. Topology

The proposed parallel-cell multilevel CSC is formed by several six-switch CSC cells in parallel connection. Every six-switch CSC cell has a separate DC current source, and the ac terminals for all six-switch CSC cells are connected in parallel, as shown in Fig. 5.1. Each six-switch CSC cell has six switches, $S_{ap}$, $S_{an}$, $S_{bp}$, $S_{bn}$, $S_{cp}$ and $S_{cn}$, one DC current source, $I_{dc}$, and three filter capacitors, $C_a$, $C_b$ and $C_c$, for filtering and commutation. The phase current of the new multilevel CSC is the sum of the outputs of all six-switch CSC cells in parallel, as shown in Fig. 5.2 for a nine-level CSC case. Therefore, a parallel-cell multilevel CSC with n six-switch CSC cells can produce a 2n+1 level of output phase current, since each six-switch CSC cell can generate three-phase, three-level output currents, $+I_{dc}$, 0 and $-I_{dc}$. In this chapter, the n-level CSC is defined as the multilevel CSC with an n-level of phase current.

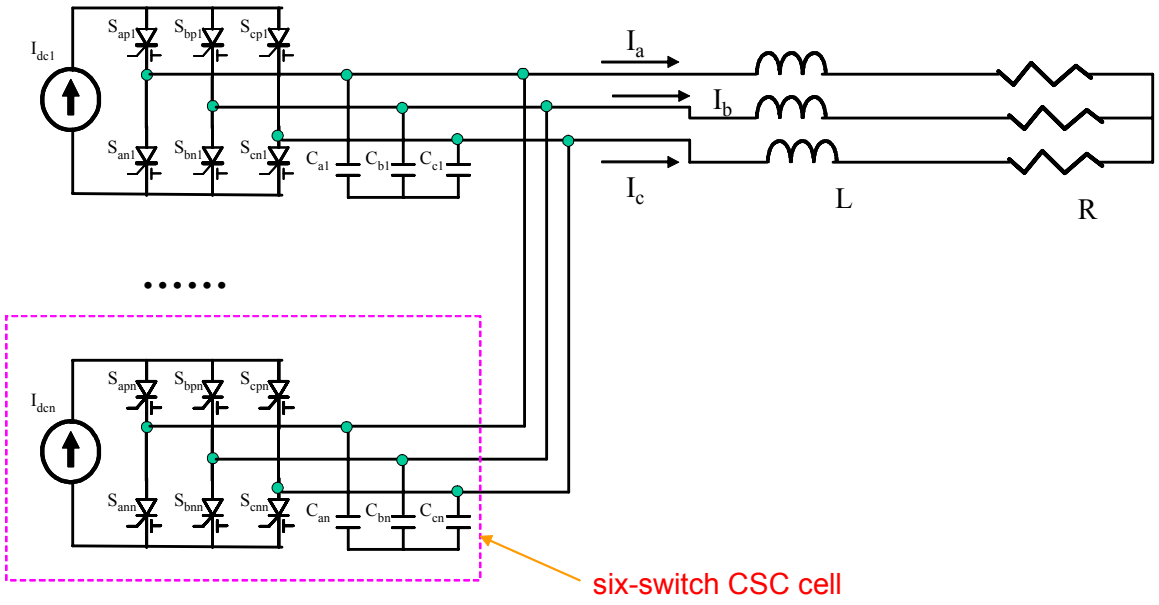



Fig. 5.1. Schematic of the parallel-cell multilevel CSC.

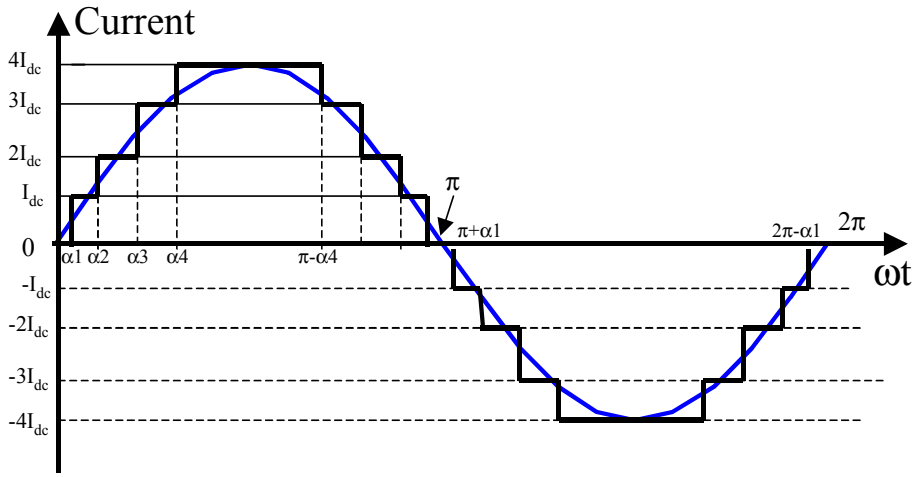



Fig. 5.2. Output phase current waveforms of the parallel-cell nine-level CSC.

### 5.1.2. Power Semiconductor Devices

Since the basic structure for the parallel-cell multilevel CSC is six-switch CSC cell, symmetrical power semiconductor devices are needed to block both the reverse voltage and the forward voltage. Traditionally, only the symmetrical GTO has been available for the high power CSC [B1, B6]. Recently, two types of high-power fast-switching symmetrical power semiconductor devices have also been available and they are symmetrical ETO and symmetrical IGCT. Symmetrical ETOs with blocking voltage up to 6.5 kV and maximum controllable turn-off current up to 1000 A have been developed at the Center for Power Electronics Systems (CPES) at Virginia Tech [K5]. Symmetrical IGCTs with the blocking voltage up to 6.5 kV and maximum controllable current up to 1500 A are commercially available [D1, D8]. Using these advanced symmetrical power semiconductor devices with superior levels of switching performance, the switching frequency for the multilevel CSC can be improved, resulting in a system with fast dynamic response and lower harmonics.

### 5.1.3. Advantages and Limitations

From the topology diagram shown Fig. 5.1, it is clear that the basic cell is the six-switch CSC cell. Based on the basic cell, the system structure for the new multilevel CSC is simplified, and modularized circuit layout and packaging can be implemented. The higher current capacity for the new multilevel CSC can be easily achieved by using more six-switch CSC cells in parallel. Since the device current is only dictated by the DC current source for each six-switch CSC cell, no current balancing components are needed, in contrast to the traditional parallel device case. Therefore, to achieve the same levels of output current, a minimum number of components and separate DC current sources are required for the new multilevel CSC, which is different from the case for other multilevel CSCs. Due to the line-frequency voltage-ripple cancellation, only the current ripple in switching frequency will show up in the DC-link

current. So the DC-link current control is simplified, and the DC-link inductor can be greatly reduced without sacrificing the current harmonics. The switching frequency can be as low as at the line frequency, since a multilevel step current is employed to approximate the required sinusoidal current. Thus, the switching loss can be very low, and high-power symmetrical semiconductor devices with low conduction loss can be used.

The parallel-cell multilevel CSC is suitable for high-current, high-power applications, such as high-power induction motor drives, high-current amplifiers and FACTS devices, due to its high current capability, low output dv/dt and low harmonics. The required separate DC current source for each CSC cell can be an inductor or a voltage source in series with an inductor. The structure of the separate DC current sources is especially well suited to applications containing renewable energy sources, such as batteries, fuel cells, photovoltaics, biomasses and so on.

## 5.2. Modeling the Parallel-Cell Multilevel CSC

### 5.2.1. Average Model at Steady Coordinates

Due to the switching function of the active device, the system shown in Fig. 5.1 is a discontinuous, time-varying nonlinear system. To properly analyze and control the proposed multilevel CSC, a continuous time-invariant model is needed. Since all the six-switch CSC cells in Fig. 5.1 are identical, it is convenient to analyze only one cell and then apply the results to other cells.

Fig. 5.3 shows the typical six-switch CSC cell structure of cell i, where number i is from 1 to n, and n is the total cell number. Since the current source cannot be open-circuit, Equations (5-1)-(5-2) must be met during normal operation:

$$S_{api} + S_{bpi} + S_{cpi} = 1 \quad (5\text{-}1)$$

$$S_{ani} + S_{bni} + S_{cni} = 1 \quad (5\text{-}2)$$

where, $S_{api} = 1$ if switch $S_{api}$ is on, and $S_{api} = 0$ if switch $S_{api}$ is off. Other switches are defined in the same way.

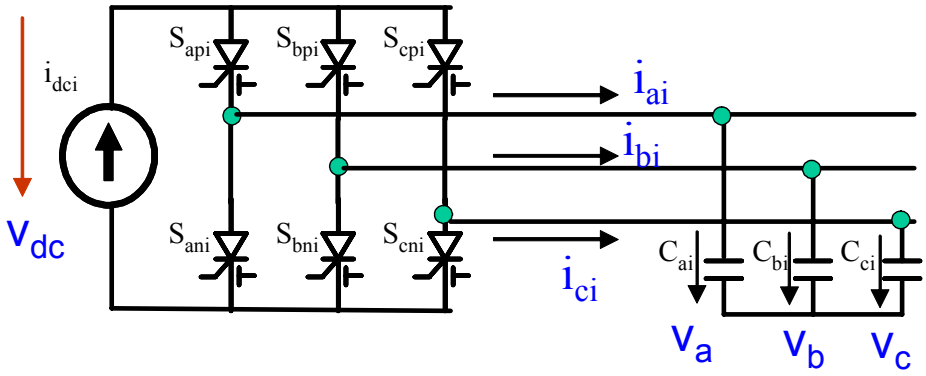



Fig. 5.3. Typical six-switch CSC cell structure of cell i.

During the normal switching operation, the relationship between the switching states and output currents as well as the voltage across DC current source are as following Equations (5-3) to (5-6).

$$i_{ai} = S_{ai} \cdot i_{dci} \quad (5\text{-}3)$$

$$i_{bi} = S_{bi} \cdot i_{dci} \quad (5\text{-}4)$$

$$i_{ci} = S_{ci} \cdot i_{dci} \quad (5\text{-}5)$$

$$v_{dci} = S_{ai} \cdot v_a + S_{bi} \cdot v_b + S_{ci} \cdot v_c \quad (5\text{-}6)$$

where, $i_{dci}$ is the DC-link current for CSC cell i; $i_{ai}$, $i_{bi}$ and $i_{ci}$ are the output phase currents for phase a, b and c in CSC cell i; $v_a$, $v_b$ and $v_c$ are the out phase voltages for phase a, b and c; $S_{ai}$, $S_{bi}$ and $S_{ci}$ are the switching functions for phase a, b and c in cell i, which are defined in Equations (5-7) to (5-9).

$$S_{ai} = S_{api} - S_{ani} \quad (5\text{-}7)$$

$$S_{bi} = S_{bpi} - S_{bni} \quad (5\text{-}8)$$

$$S_{ci} = S_{cpi} - S_{cni} \quad (5\text{-}9)$$

In a PWM converter, the average operator can be applied to Equations (5-3) to (5-6) to obtain the average parameters during one switching period T, as shown in Equations (5-10) to (5-13).

$$\frac{1}{T}\int_{t-T}^{T} i_{ai}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{ai}(\tau)\cdot i_{dci}(\tau)d\tau \quad (5\text{-}10)$$

$$\frac{1}{T}\int_{t-T}^{T} i_{bi}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{bi}(\tau)\cdot i_{dc}i(\tau)d\tau \quad (5\text{-}11)$$

$$\frac{1}{T}\int_{t-T}^{T} i_{ci}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{ci}(\tau)\cdot i_{dc}i(\tau)d\tau \quad (5\text{-}12)$$

$$\frac{1}{T}\int_{t-T}^{T} v_{dci}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{ai}(\tau)\cdot v_a(\tau)d\tau + \frac{1}{T}\int_{t-T}^{t} S_{bi}(\tau)\cdot v_b(\tau)d\tau + \frac{1}{T}\int_{t-T}^{t} S_{ci}(\tau)\cdot v_c(\tau)d\tau \quad (5\text{-}13)$$

Assuming the DC-link current and output voltages can be considered to be constant current and voltage sources with little ripple during one switching cycle T, the average output phase currents $I_{ai}$, $I_{bi}$ and $I_{ci}$ for phase a, b and c as well as the average voltage across DC-link current source $V_{dc}$ can be approximated by Equations (5-14) to (5-17).

$$I_{ai} = \frac{1}{T}\int_{t-T}^{T} i_{ai}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{ai}(\tau)\cdot i_{dci}(\tau)d\tau \approx \frac{1}{T}\int_{t-T}^{t} S_{ai}(\tau)d\tau \cdot \frac{1}{T}\int_{t-T}^{t} i_{dci}(\tau)d\tau = d_{ai}\cdot I_{dci} \quad (5\text{-}14)$$

$$I_{bi} = \frac{1}{T}\int_{t-T}^{T} i_{bi}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{bi}(\tau)\cdot i_{dci}(\tau)d\tau \approx \frac{1}{T}\int_{t-T}^{t} S_{bi}(\tau)d\tau \cdot \frac{1}{T}\int_{t-T}^{t} i_{dci}(\tau)d\tau = d_{bi}\cdot I_{dci} \quad (5\text{-}15)$$

$$I_{ci} = \frac{1}{T}\int_{t-T}^{T} i_{ci}(\tau)d\tau = \frac{1}{T}\int_{t-T}^{t} S_{ci}(\tau)\cdot i_{dci}(\tau)d\tau \approx \frac{1}{T}\int_{t-T}^{t} S_{ci}(\tau)d\tau \cdot \frac{1}{T}\int_{t-T}^{t} i_{dci}(\tau)d\tau = d_{ci}\cdot I_{dci} \quad (5\text{-}16)$$

$$V_{dci} = \frac{1}{T}\int_{t-T}^{T} V_{dc}(\tau)d\tau \approx d_{ai}\cdot V_a + d_{bi}\cdot V_b + d_{ci}\cdot V_c \quad (5\text{-}17)$$

where, $d_{ai}$, $d_{bi}$ and $d_{ci}$ are duty cycles for phases a, b and c in CSC cell i; $V_a$, $V_b$ and $V_c$ are the average phase voltages during a switching period T; and $I_{dci}$ is the average DC-link current during switching period T.

According to Equations (5-14) to (5-17), the average model for CSC cell i can be derived, as shown in Fig. 5.4.

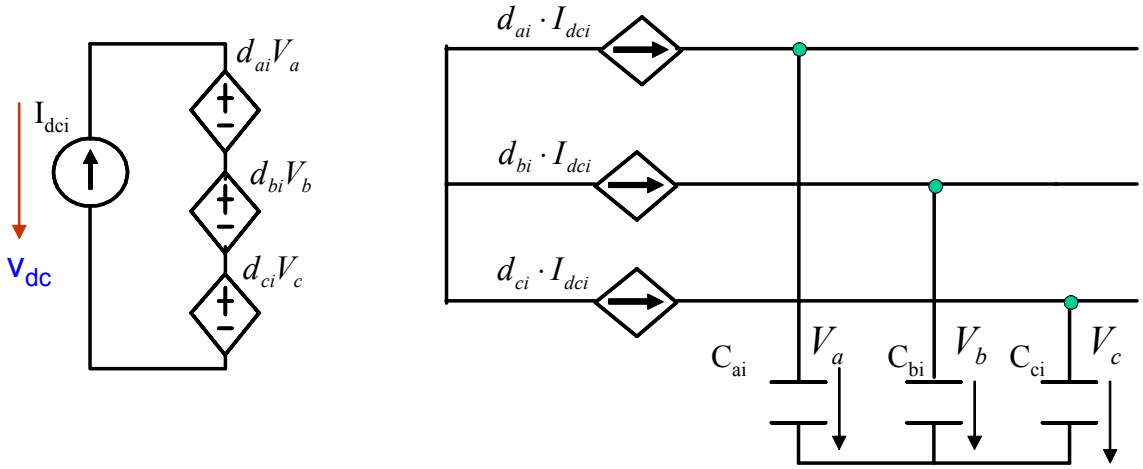



Fig. 5.4. Average model for six-switch CSC cell i.

Similarly, the average model for the parallel-cell multilevel CSC with n CSC cells, as shown in Fig. 5.1, can be obtained as in the Fig. 5.5, where $C_a$, $C_b$ and $C_c$ are the total filter capacitance defined in Equations (5-18) to (5-21).

$$C_a = C_{a1} + C_{a2} + \ldots + C_{an} \quad (5\text{-}18)$$

$$C_b = C_{b1} + C_{b2} + \ldots + C_{bn} \quad (5\text{-}19)$$

$$C_c = C_{c1} + C_{c2} + \ldots + C_{cn} \quad (5\text{-}20)$$

$$C_a = C_b = C_c = C \quad (5\text{-}21)$$

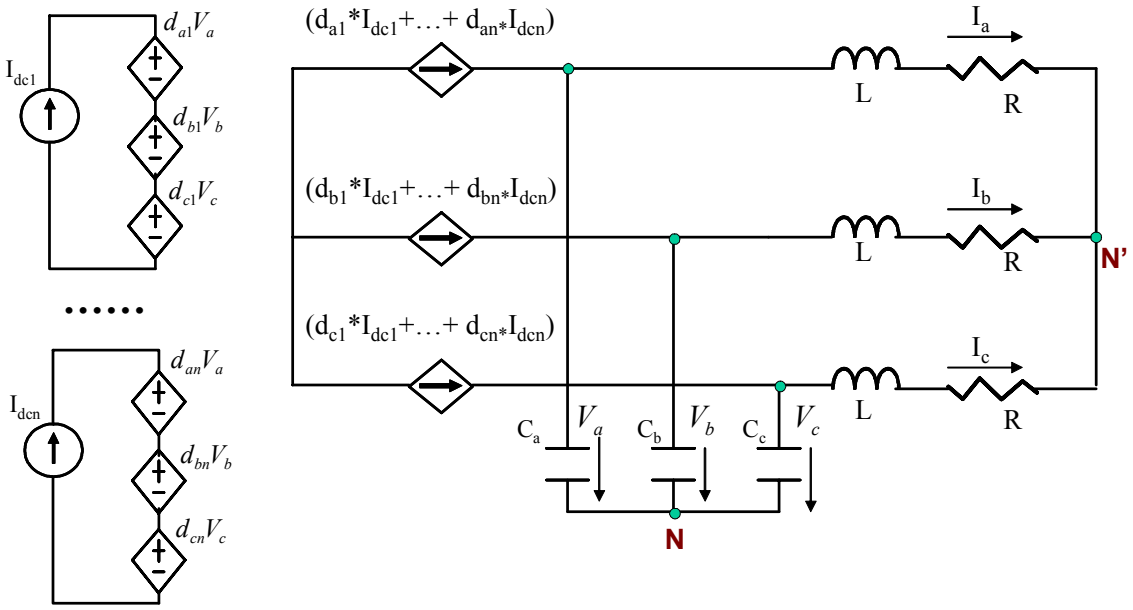



Fig. 5.5. Average model for the multilevel CSC with n six-switch CSC cells.

Assuming that an identical DC current source is used for each CSC cell and the gate signal for each cell is rotated, the average model for the multilevel CSC shown in Fig. 5.5 can be expressed as displayed in Fig. 5.6 and can be further simplified as shown in Fig. 5.7, which is similar to the average model of the traditional CSC. The average duty cycles $d_a$, $d_b$ and $d_c$ as well as average DC-link current $I_{dc}$ are defined by Equations (5-22) to (5-25).

$$d_a = d_{a1} + d_{a2} + \ldots + d_{an} \quad (5\text{-}22)$$

$$d_b = d_{b1} + d_{b2} + \ldots + d_{bn} \quad (5\text{-}23)$$

$$d_c = d_{c1} + d_{c2} + \ldots + d_{cn} \quad (5\text{-}24)$$

$$I_{dc} = (I_{dc1} + I_{dc2} + \ldots + I_{dcn})/n \quad (5\text{-}25)$$

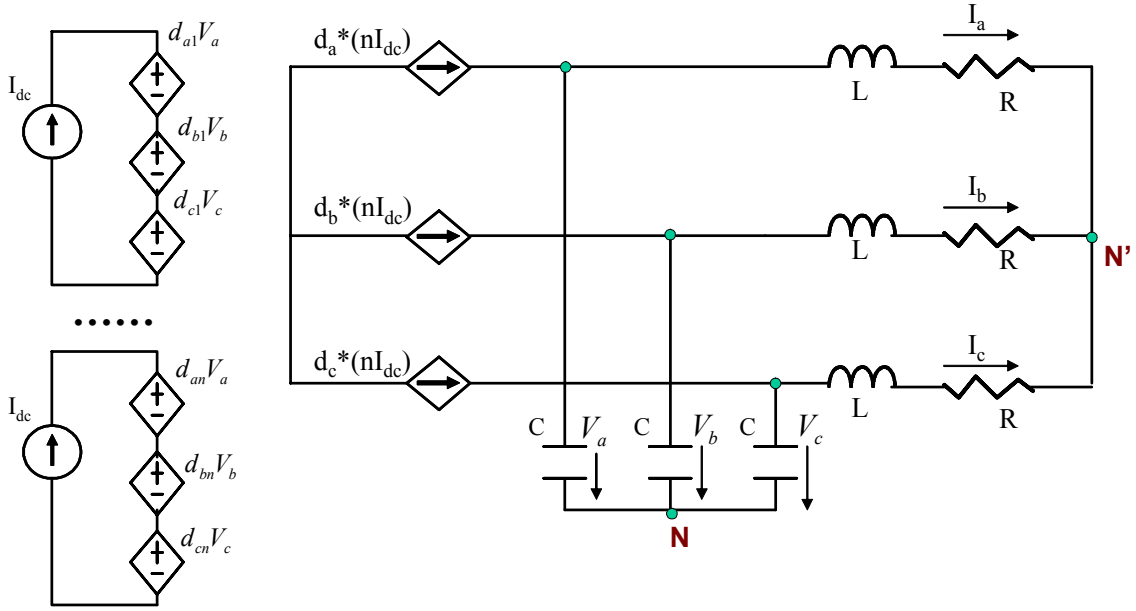



Fig. 5.6. Average model for the multilevel CSC with gate-signal rotating control.

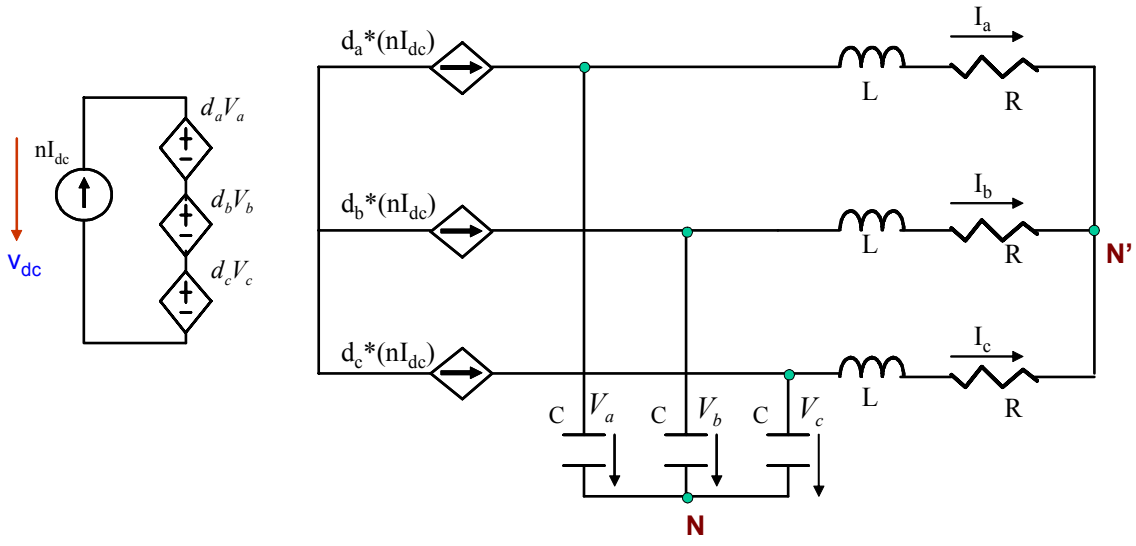



Fig. 5.7. Simplified average model for the multilevel CSC with gate-signal rotating control.

The system shown in Fig. 5.7 is a continuous time-varying system in steady coordinates, and can be described using state Equations (5-26) to (5-28).

$$V_{dc} = (d_a \quad d_b \quad d_c) \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (5\text{-}26)$$

$$\begin{pmatrix} d_a \\ d_b \\ d_c \end{pmatrix} \cdot (nI_{dc}) = C \frac{d}{dt} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} + \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} \quad (5\text{-}27)$$

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = L \frac{d}{dt} \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} + R \cdot \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} + V_{N'N} \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix} \quad (5\text{-}28)$$

where $V_{N'N}$ is the voltage difference between filter capacitor neutral point N and load neutral point N' (see Fig. 5.7).

### 5.2.2. Average Model at Rotating Coordinates

With a sinusoidal duty cycle, the multilevel CSC will have sinusoidal output current and voltage in the steady state. Since the three-phase sinusoidal variables in abc coordinates will become dc values in proper dq rotating coordinates, the dq circuit model and corresponding DC operation point can be obtained by applying the following transformation matrix (called Park's transformation matrix), as shown in Equation (5-29):

$$T_{dqo(\omega)/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (5\text{-}29)$$

where, $\omega = 2\pi \cdot f$ and f is the line frequency.

For the Park's transformation matrix shown in Equation (5-29), the following Equations are satisfied:

$$T_{dqo(\omega)/abc} \cdot \frac{d}{dt}\left(T^{-1}{}_{dqo(\omega)/abc}\right) = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \text{ and } \quad T^{T}{}_{dqo(\omega)/abc} = T^{-1}{}_{dqo(\omega)/abc}.$$

According to the definition of the voltage and current in dq coordinates shown in Equations (5-30) and (5-31) and state Equations in abc coordinates expressed in Equations (5-26) to (5-28), the state Equations in dg coordinates can be described using Equations (5-32) to (5-34).

$$\begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} = T_{dq(\omega)/abc} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (5\text{-}30)$$

$$\begin{pmatrix} I_d \\ I_q \\ I_o \end{pmatrix} = T_{dq(\omega)/abc} \cdot \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} \quad (5\text{-}31)$$

$$V_{dc} = \begin{pmatrix} d_d & d_q & d_o \end{pmatrix} \cdot \begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} \quad (5\text{-}32)$$

$$\begin{pmatrix} d_d \\ d_q \\ d_o \end{pmatrix} \cdot \left(nI_{dc}\right) = C\frac{d}{dt}\begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} + C\begin{pmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} + \begin{pmatrix} I_d \\ I_q \\ I_o \end{pmatrix} \quad (5\text{-}33)$$

$$\begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} = L\frac{d}{dt}\begin{pmatrix} I_d \\ I_q \\ I_o \end{pmatrix} + L\begin{pmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} I_d \\ I_q \\ I_o \end{pmatrix} + R \cdot \begin{pmatrix} I_d \\ I_q \\ I_o \end{pmatrix} + V_{N'N}\begin{pmatrix} 0 \\ 0 \\ \sqrt{3} \end{pmatrix} \quad (5\text{-}34)$$

According to state Equations (5-32)-(5-34) in dq coordinates (rotating at an angular speed of ω), the equivalent circuit can be obtained as shown in Fig. 5.8.

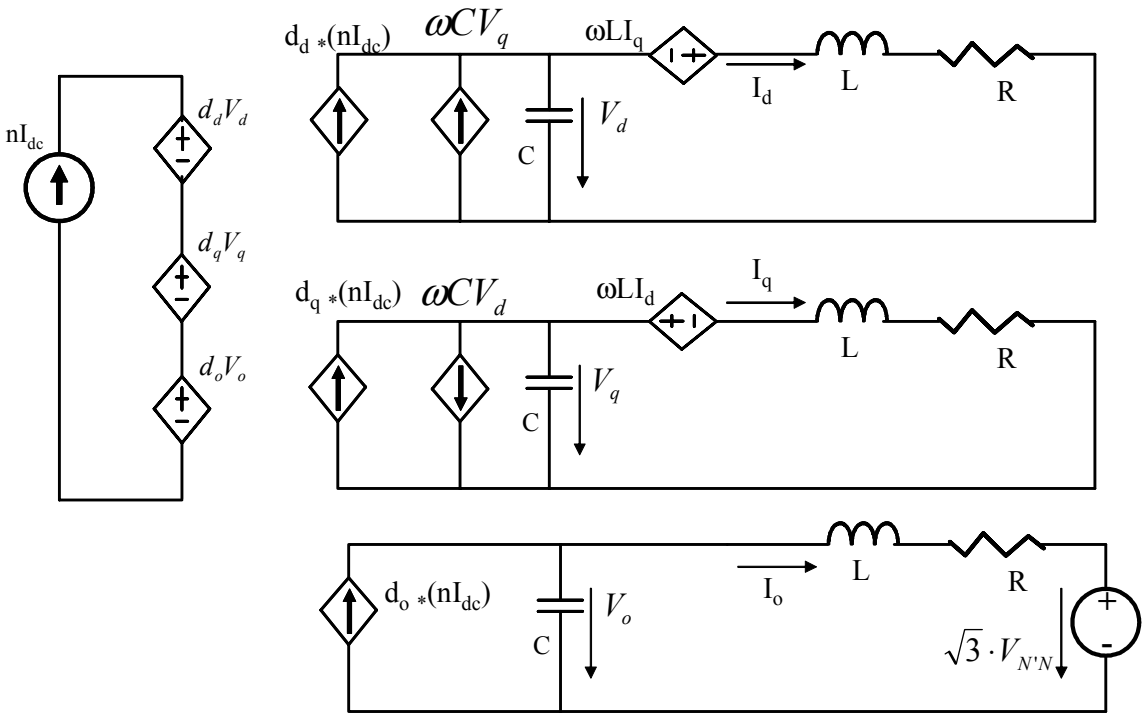



Fig. 5.8. Average model for the multilevel CSC in dqo coordinates (ω = 2πf).

In a three-wire, three-phase system, the sum of three phase currents is always equal to zero. So the o-channel current and duty cycle are always zero. Although the voltage difference between load neutral point N' and filter capacitor neutral point ($V_{N'N}$) may be a non-zero value, it only contributes to the o-channel voltage and has no effect on the d-channel circuit, q-channel circuit or voltage across DC-link current source. Therefore, the o-channel circuit in the dqo coordinates can be omitted for the three-wire three-phase multilevel CSC, and the equivalent circuit for the average model in dg coordinates can be simplified as shown in Fig. 5.9.

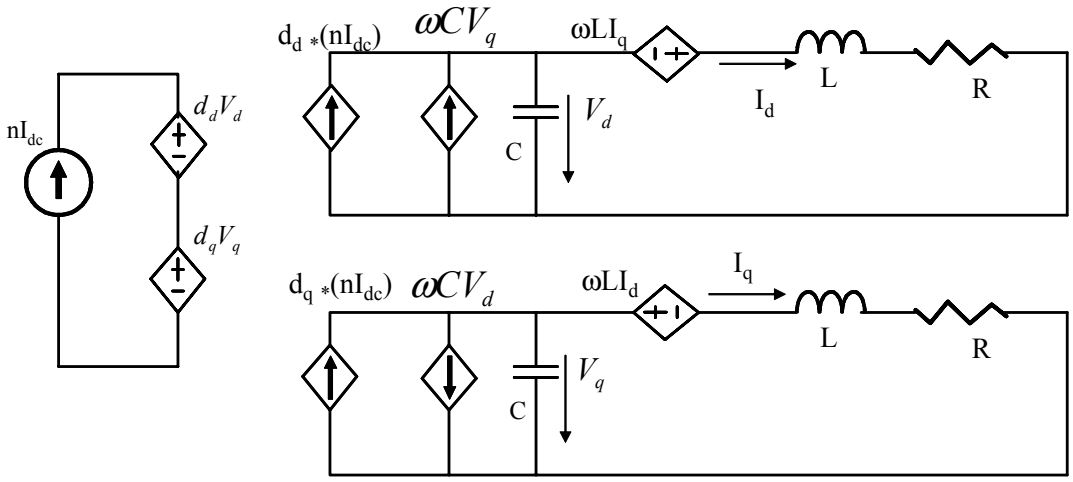



Fig. 5.9. Average model for the multilevel CSC in dq coordinates (ω = 2πf).

Similarly, using the park's transformation matrix for the mω frame as described in Equation (5-35), the average model for the multilevel CSC in dq coordinates rotating at a angular speed of mω (ω = 2πf, m is an integer) can be derived, as shown in Fig. 5.10.

$$T_{dq(m\omega)/abc} = \sqrt{\frac{2}{3}}\begin{pmatrix} \cos(m\omega t) & \cos(m\omega t - \frac{2\pi}{3}) & \cos(m\omega t + \frac{2\pi}{3}) \\ -\sin(m\omega t) & -\sin(m\omega t - \frac{2\pi}{3}) & -\sin(m\omega t + \frac{2\pi}{3}) \end{pmatrix} \quad (5\text{-}35)$$

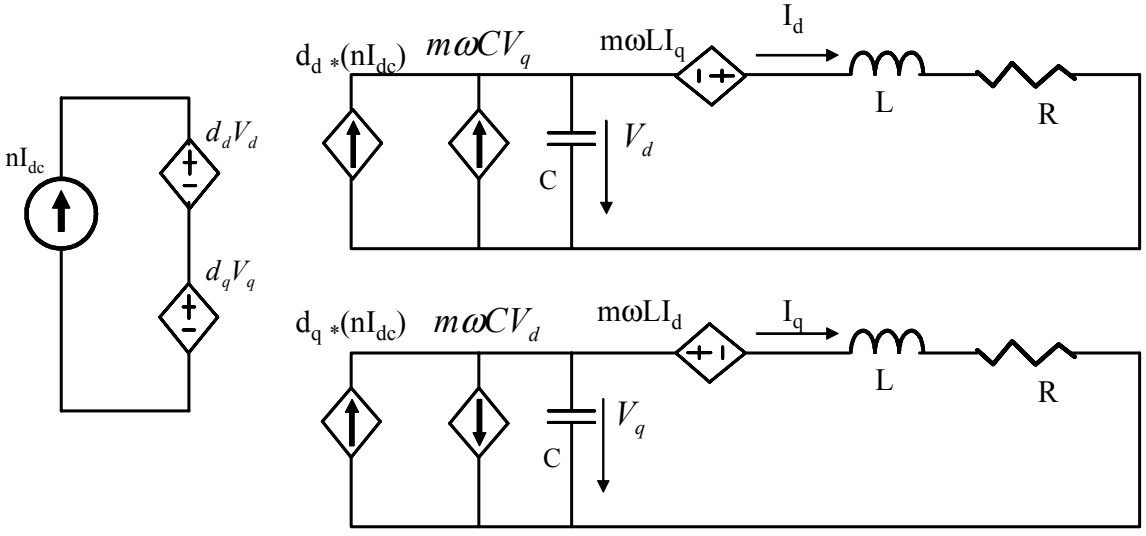



Fig. 5.10. Average model for the multilevel CSC in dq coordinates (mω = 2πmf).

During normal operation, if a sinusoidal duty cycle signal with frequency f is applied to each phase, the multilevel CSC will have sinusoidal output current and voltage waveforms with the same frequency of f in steady state. In dq coordinates rotating at an angular speed of ω (ω = 2πf), the output current and voltage will become constant values, just like in the DC-DC converter case. For example, a three-phase balanced sinusoidal voltage with an amplitude of $V_m$ and an angular speed of ω in abc coordinates will become constant current value in rotating dg coordinates as displayed in Equation (5-36), where the d-coordinate is aligned with phase **a** voltage.

$$\begin{pmatrix} V_d \\ V_q \\ V_o \end{pmatrix} = T_{dq(\omega)/abc} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = T_{dq(\omega)/abc} \cdot V_m \begin{pmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{pmatrix} = \begin{pmatrix} \sqrt{\frac{3}{2}} \cdot V_m \\ 0 \\ 0 \end{pmatrix} \quad (5\text{-}36)$$

To obtain the DC operation point, the simplified equivalent circuit (Fig. 5.11) without filter inductor L and filter capacitor C can be used, since the inductor is short-circuit and the capacitor behaves like an open circuit under DC operation conditions. For a multilevel CSC with given load current $I_d$, $I_q$ and DC-link current $I_{dc}$, the duty cycles ($D_d$, $D_q$), output voltages ($V_d$, $V_q$) and voltage across the DC-link current source ($V_{dc}$) can be calculated using Equations (5-37) to (5-38).

$$\begin{pmatrix} V_d \\ V_q \\ D_d \\ D_q \end{pmatrix} = \begin{pmatrix} R & -\omega L \\ \omega L & R \\ \frac{1-\omega^2 LC}{nI_{dc}} & -\frac{\omega RC}{nI_{dc}} \\ \frac{\omega RC}{nI_{dc}} & \frac{1-\omega^2 LC}{nI_{dc}} \end{pmatrix} \cdot \begin{pmatrix} I_d \\ I_q \end{pmatrix} \quad (5\text{-}37)$$

$$V_{dc} = \begin{pmatrix} D_d & D_q \end{pmatrix} \cdot \begin{pmatrix} V_d \\ V_q \end{pmatrix} \quad (5\text{-}38)$$

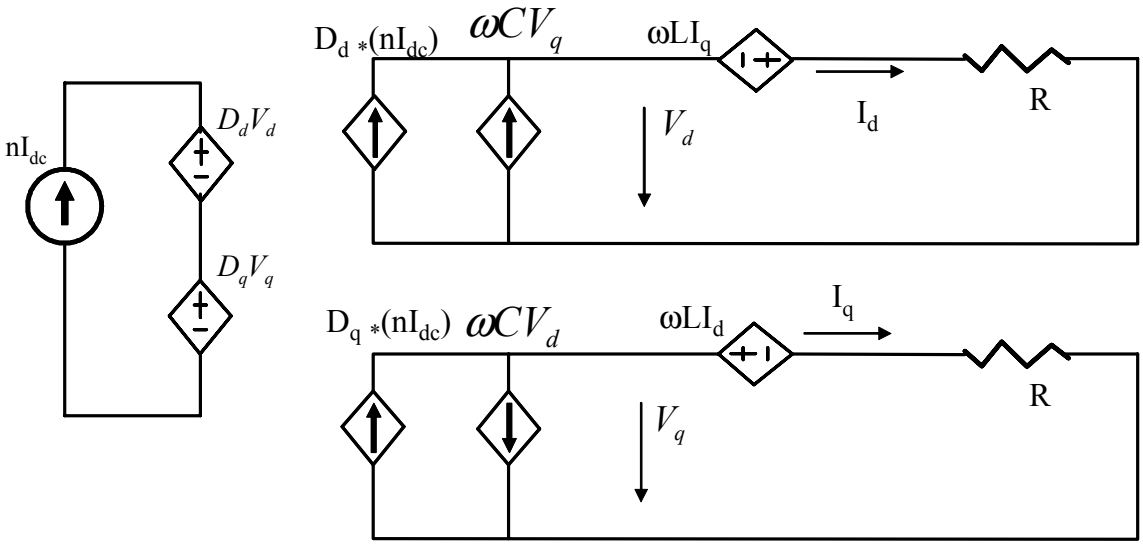



Fig. 5.11. Average model for the multilevel CSC in dq coordinates ($\omega = 2\pi f$) under DC operation conditions.

### 5.2.3. Small Signal Model at Rotating Coordinates

In dq rotating coordinates, the multilevel CSC with sinusoidal duty cycle will have a steady-state DC operation point. For the average model of the multilevel CSC in dq coordinates shown in Fig. 5.9, the state-space Equations can be rewritten as Equations (5-39) to (5-40). Based on the DC operation point obtained using Equations (5-37) to (5-38), the small-signal model (Fig. 5.12) can be derived by applying a small perturbation and linearization of the state Equations around the equilibrium point, as displayed in Equations (5-41) to (5-42).

$$V_{dc} = (d_d \quad d_q) \cdot \begin{pmatrix} V_d \\ V_q \end{pmatrix} \quad (5\text{-}39)$$

$$\frac{d}{dt}\begin{pmatrix} V_d \\ V_q \\ I_d \\ I_q \end{pmatrix} = \begin{pmatrix} 0 & \omega & -\frac{1}{C} & 0 \\ -\omega & 0 & 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 & -\frac{R}{L} & \omega \\ 0 & \frac{1}{L} & -\omega & -\frac{R}{L} \end{pmatrix} \cdot \begin{pmatrix} V_d \\ V_q \\ I_d \\ I_q \end{pmatrix} + \begin{pmatrix} \frac{nI_{dc}}{C} & 0 \\ 0 & \frac{nI_{dc}}{C} \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} d_d \\ d_q \end{pmatrix} \quad (5\text{-}40)$$

$$\tilde{V}_{dc} = (D_d \quad D_q) \cdot \begin{pmatrix} \tilde{V}_d \\ \tilde{V}_q \end{pmatrix} + (\tilde{d}_d \quad \tilde{d}_q) \cdot \begin{pmatrix} V_d \\ V_q \end{pmatrix} \quad (5\text{-}41)$$

$$\frac{d}{dt}\begin{pmatrix} \tilde{V}_d \\ \tilde{V}_q \\ \tilde{I}_d \\ \tilde{I}_q \end{pmatrix} = \begin{pmatrix} 0 & \omega & -\frac{1}{C} & 0 \\ -\omega & 0 & 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 & -\frac{R}{L} & \omega \\ 0 & \frac{1}{L} & -\omega & -\frac{R}{L} \end{pmatrix} \cdot \begin{pmatrix} \tilde{V}_d \\ \tilde{V}_q \\ \tilde{I}_d \\ \tilde{I}_q \end{pmatrix} + \begin{pmatrix} \frac{nI_{dc}}{C} & 0 \\ 0 & \frac{nI_{dc}}{C} \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} \tilde{d}_d \\ \tilde{d}_q \end{pmatrix} + \begin{pmatrix} \frac{n\tilde{I}_{dc}}{C} & 0 \\ 0 & \frac{n\tilde{I}_{dc}}{C} \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} D_d \\ D_q \end{pmatrix} \quad (5\text{-}42)$$

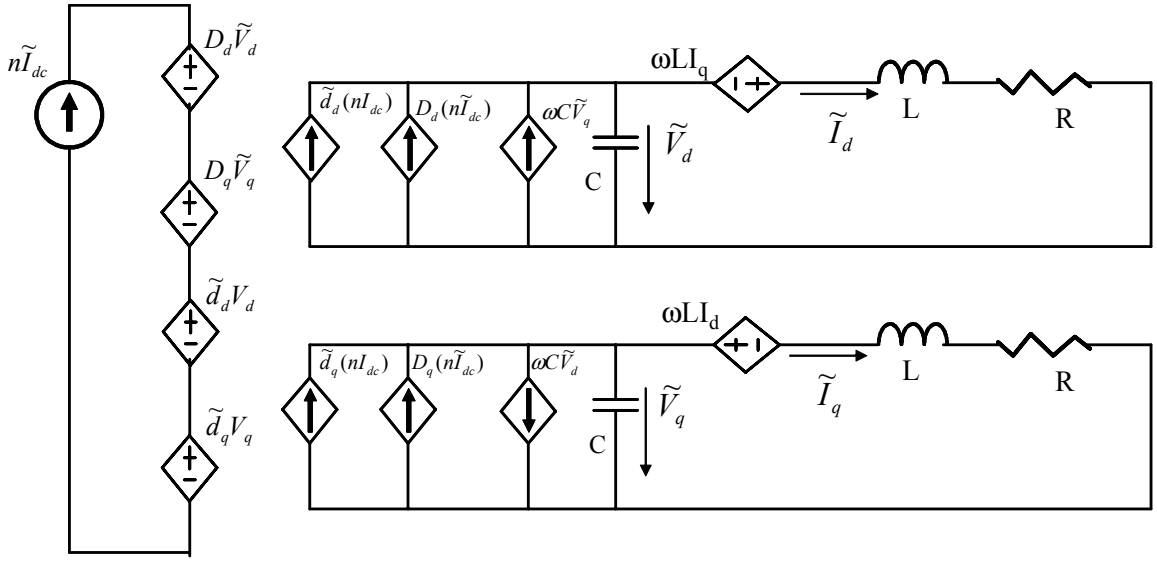



Fig. 5.12. Small-signal model for the multilevel CSC in dq coordinates (ω = 2πf).

## 5.3. Filter Design of the Parallel-Cell Multilevel CSC

One typical application of the parallel-cell multilevel CSC is in the STATCOM [A3], as shown in Fig. 5.13, where a five-level CSC based STATCOM using two six-switch CSC cells in parallel. The DC-link inductor $L_{dc}$ is employed as the DC current source in this case. After being filtered by filter capacitor $C_f$, the compensation current is injected from the multilevel CSC into the power system through coupling inductor L.

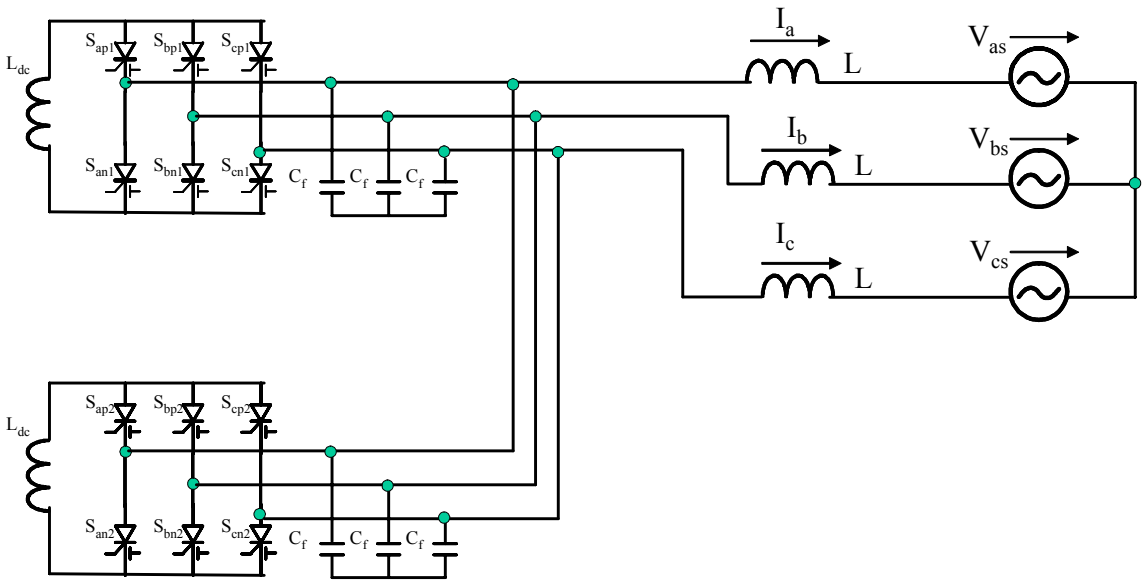



Fig. 5.13. Five-level CSC based STATCOM.

The filter capacitor $C_f$ (as shown in Fig. 5.13) provides a path to bypass the current harmonics. For fundamental frequency f, the capacitor $C_f$ should behave like an open-circuit to pass the required compensation current. So Equation (5-43) should be satisfied. On the other hand, for the first dominant harmonics ($f_1$) of output current from CSC cell, the filter capacitor $C_f$ should behave like a short-circuit in order to prevent the current harmonics from injecting into the load. Therefore, Equation (5-44) should be satisfied. At the same time, the resonant frequency between filter capacitor $C_f$ and load inductance $L_s$ should be placed in a safe region where no residual harmonics exist.

$$X_C = \frac{1}{2\pi \cdot f \cdot C_f} >> 1 \quad (5\text{-}43)$$

$$X_{C1} = \frac{1}{2\pi \cdot f_1 \cdot C_f} << 1 \quad (5\text{-}44)$$

Coupling inductor L and filter capacitor $C_f$ forms a second–order filter, which will pass current at the fundamental frequency and will bypass the harmonic current. The resonant frequency $f_R$ between L and $C_f$

should be put between the fundamental frequency and switching frequency $f_s$. Furthermore, the resonant frequency $f_R$ should not be an integer times of fundamental frequency to avoid resonance between L and $C_f$. According to the single phase equivalent circuit of the CSC based STATCOM shown in Fig. 5.14, the transfer function between the injected current I(s) and output current $I_i(s)$ from the CSC based STATCOM can be derived as shown in Equation (5-45). To effectively pass the fundamental component and filter out the harmonic current, Equations (5-46) and (5-47) should be satisfied. After all, the filter capacitor $C_f$ and filter inductor L can be designed according to Equations (5-43) to (5-47).

$$G(s) = \frac{I(s)}{I_i(s)} = \frac{1}{1+RC_f s+LC_f s^2} \quad , (5\text{-}45)$$

where, R is the total resistance of filter inductor and power line.

$$\left|G(j\omega)\right| = \left|G(j2\pi f)\right| \approx 1 \quad (5\text{-}46)$$

$$\left|G(j\omega_1)\right| = \left|G(j2\pi f_1)\right| << 1 \quad (5\text{-}47)$$

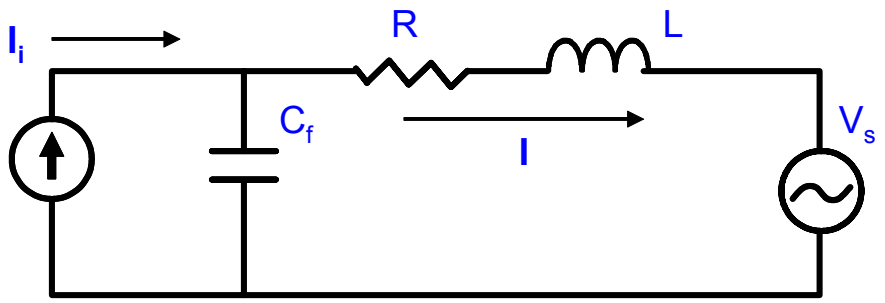



Fig. 5.14. Single-phase equivalent circuit for the multilevel CSC based STATCOM.

DC-link inductor $L_{dc}$ will smooth the DC-link current $I_{dc}$ and ensure the normal operation of the multilevel CSC. For a given DC-link current ripple $\Delta I_{dc}$, the required DC-link inductance can be approximated as follows:

$$L_{dc} = \frac{V_m}{2\Delta I_{dc} f_s}, \quad (5\text{-}48)$$

where $V_m$ is the peak line-to-line output voltage of the multilevel CSC, which is mainly dictated by the DC-link voltage rating of ETO device, and $f_s$ is the switching frequency.

Based on the previous analysis, using an asymmetrical ETO in series with a diode as the main switch, the power stage parameters for a five-level CSC based STATCOM (see Fig. 5.15) are as follows:

$V_m$ = 2800 V; $I_{dc}$ = 1100 A; $C_f$ = 100 μF; L = 0.4 mH; $L_{dc}$ = 12 mH (10% DC-link current ripple); $f_s$ = 1080 Hz; $T_j$ = 115 °C; $T_w$ = 55 °C.

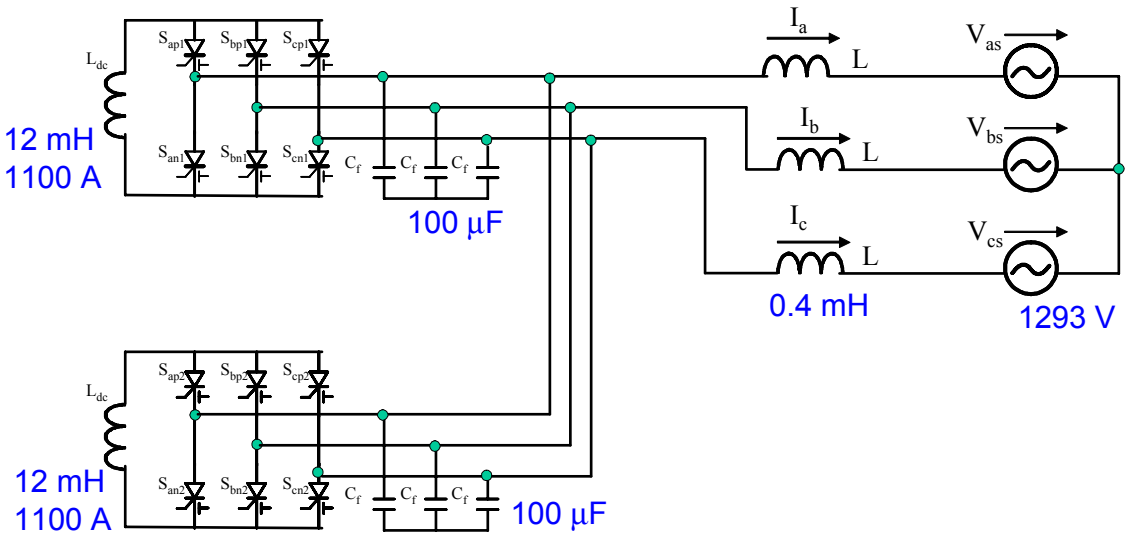



Fig. 5.15. Five-level CSC based STATCOM with designed parameters.

Correspondingly, the dq model for the five-level CSC based STATCOM at rotating frame (ω = 2πf, f = 60 Hz) is shown in Fig. 5.16. Assuming that the d-axis is aligned with phase **a** source voltage, the voltage sources in dq rotating frame are as follows: $V_{ds}$ = 1585 V; $V_{qs}$ = 0 V.

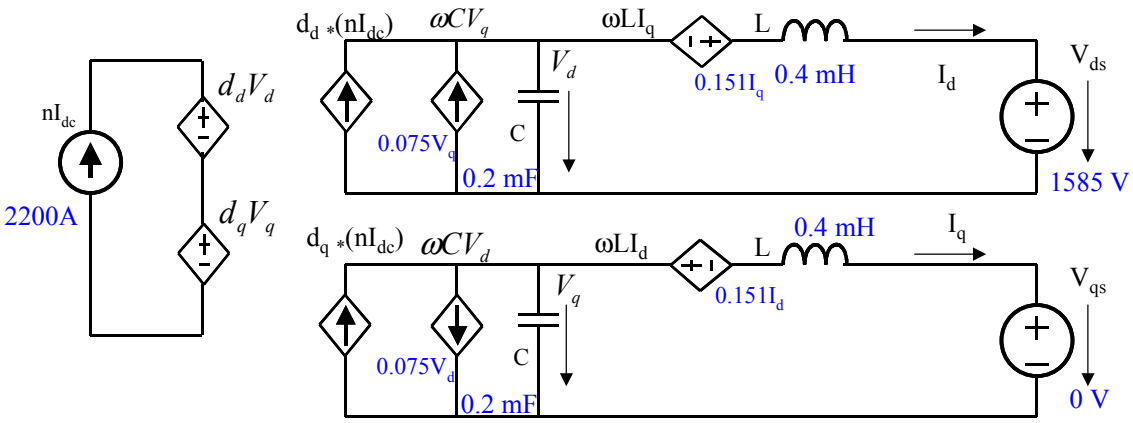



Fig. 5.16. The dq model of a five-level CSC based STATCOM.

For lagging var compensation, the reactive power rating is limited by the modulation index $D_q$, since the maximum $D_q$ is about 1.225 when a space vector modulation (SVM) scheme is used. Therefore, the DC operation point for the maximum lagging var compensation can be calculated by Equations (5-49) to (5-53).

$$I_q = \frac{D_q \cdot I_{dc} - V_{ds} \cdot \omega C_f}{1+\omega^2 L C_f} \quad (5\text{-}49)$$

$$I_d = \frac{D_d \cdot I_{dc} + V_{qs} \cdot \omega C_f}{1-\omega^2 L C_f} \quad (5\text{-}50)$$

$$V_d = V_{ds} - I_q \cdot X_L \quad (5\text{-}51)$$

$$V_q = V_{qs} + I_d \cdot X_L \quad (5\text{-}52)$$

$$S_{lag} = V_{ds} \cdot I_q + V_{qs} \cdot I_d \quad (5\text{-}53)$$

For given conditions $D_d = 0$, $D_q = 1.225$, and $I_{dc} = 2200$ A, the operation parameters at the maximum lagging reactive power are calculated as: $I_q = 2547$ A; $I_d = 0$ A; $V_d = 1200$ V; $V_q = 0$ V; and maximum lagging var $S_{lag} = 4.03$ MVA.

However, for leading var compensation, the reactive power rating is mainly constrained by the maximum output voltage $V_d$ since the maximum $V_d$, is about 2000 V due to the limited DC-link voltage for the ETO device. So the DC operation point for the maximum leading var compensation can be calculated using Equations (5-54) to (5-58).

$$I_q = \frac{V_{ds} - V_d}{X_L} \quad (5\text{-}54)$$

$$I_d = \frac{V_q - V_{qs}}{X_L} \quad (5\text{-}55)$$

$$D_q = \frac{I_q + \omega C_f \cdot V_d}{I_{dc}} \quad (5\text{-}56)$$

$$D_d = \frac{I_d - \omega C_f \cdot V_q}{I_{dc}} \quad (5\text{-}57)$$

$$S_{lead} = V_{ds} \cdot I_q + V_{qs} \cdot I_d \quad (5\text{-}58)$$

For given conditions $V_d$ = 2000 V, $V_q$ = 0 V, and $I_{dc}$ = 2200 A, the operation parameters at the maximum leading reactive power are calculated as: $I_q$ = -2759 A; $I_d$ = 0 A; $D_d$ = 0; $D_q$ = -1.1865; and maximum leading var $S_{lead}$ = -4.37 MVA.

To maximize the output power rating, the filter inductor L should be carefully designed. A smaller filter inductor will allow higher output current without causing over-voltage on the power semiconductor devices. Meanwhile, a smaller filter inductor also means less attenuation for the injected harmonic current. Therefore, filter inductor L should be designed to be as small as possible while still meeting the harmonics requirement.

## 5.4. System Control of the Parallel-Cell Multilevel CSC

In steady coordinates, the multilevel CSC is a discontinuous, time-varying system. By applying average operator and coordinates transformations, the equivalent circuit (dq model) for the multilevel CSC can become a continuous and time-invariant nonlinear system in the rotating frame. Under steady state, there is a DC operation point, as shown in the previous section. Around a DC operation point, through perturbation and linearization, the small signal model for multilevel CSC can be derived in order to analyze the system dynamic response and to design the control system. Since the small signal model is related to the DC operation point, the designed control system should meet system requirement through the entire operation range.

For the five-level CSC based STATCOM shown in Fig. 5.13, the small signal model can be obtained based on the dq model shown in Fig. 5.16, assuming that the two separate DC current sources are identical. Considering the trade-off between the current harmonics and dynamic response, modulation index M is chosen as 0.9, where modulation index M is defined as the ratio between the peak phase current $I_m$ and the DC-link current $I_{dc}$. For normal lagging var compensation, the operation parameters at the DC operation point are as follows:

$D_d = 0$; $D_q = 1.102$; $I_{dc} = 2200$ A; $I_q = 2352$ A; $I_d = 0$ A; $V_d = 1230$ V; $V_q = 0$ V; and the normal lagging var $S_{lag\_n} = 3.73$ MVA.

To achieve a fast dynamic response, low levels of power loss and a sufficient stability margin, the d-channel current controller $H_{id}$, the q-channel current controller $H_{iq}$, the DC-link current controller $H_{idc}$ and modulation index controller $H_m$ are required, as shown in Fig. 5.17. Based on the dq model, the small-

signal model can be obtained at the DC operation point. All controllers are then designed according to the dynamic response as well as the stability requirements.

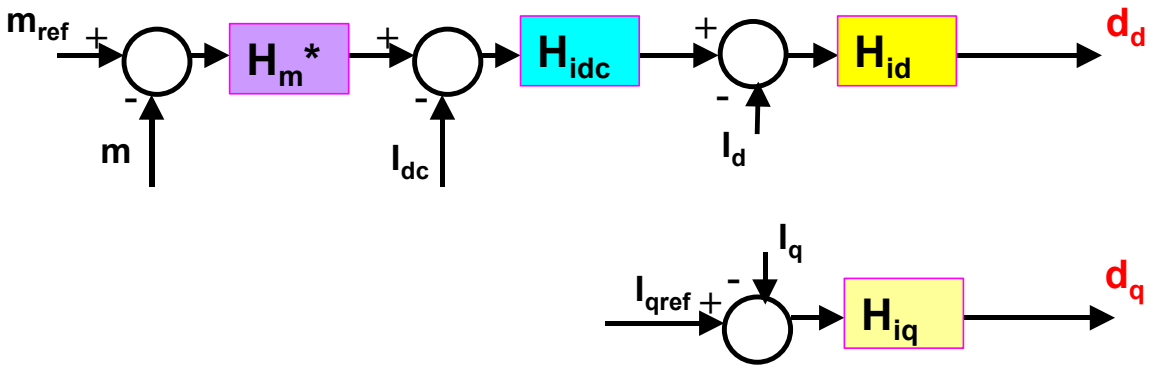



Fig. 5.17. Controller diagram of the parallel-cell multilevel CSC based STATCOM.

According to the system command, the reactive current controller will regulate the amplitude and phase of the injected current at steady state. During the transient, the dynamic response speed of the reactive current (hence the reactive var) is also dictated by the reactive current controller. So the reactive current control loop should be designed according to the system dynamic response speed requirement for the CSC based STATCOM. Assuming that the system can be approximated by the second-order un-damping system, which is roughly true for the CSC based STATCOM, for a given rising time $t_r$ that corresponds to a step command, the required control bandwidth $f_{bw}$ can be estimated using Equation (5-60):

$$f_{bw} \approx \frac{1}{4t_r}, \quad (5\text{-}60)$$

where $t_r$ is defined as the time interval during which the controlled parameter rises from the initial value to its final value. For example, if the rising time for a step response is 2.5 ms, the required control bandwidth should be above 100 Hz.

To design the reactive current control loop under the normal lagging var operation conditions as described in the beginning of this section, the transfer function of $i_q/d_q$ can be obtained using Saber simulation tool, as shown in Fig. 5.18.

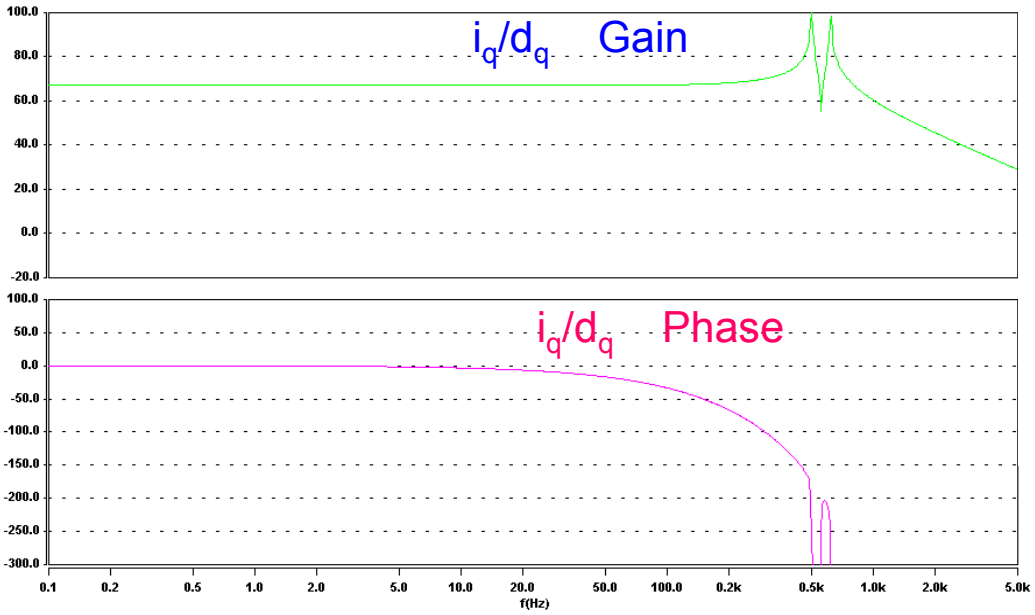



Fig. 5.18. Simulated transfer function of $i_q/d_q$ for five-level CSC based STATCOM.

Since the CSC-based STATCOM is a low-loss system, the resonant peak is huge as shown in Fig. 5.18. Without damping, the control bandwidth is limited to a value much lower than the resonant frequency and it is hard to meet the system dynamic response requirements. To prevent the resonance between the filter capacitor $C_f$ and coupling inductor L, the active damping control scheme [E2] can be used. Based on this control method, a damping resistor $R_{damp}$ is applied to the system through the control loop, as shown in Fig. 5.19. Since the damping resistor $R_{damp}$ is for harmonics only and has little effect on

the fundamental component, it will not cause any power loss as in the traditional physical damping resistor case. The damping currents for the d-channel and the q-channel can be calculated using Equations (5-60) to (5-61). The sampling frequency for damping current should be much higher than the power stage switching frequency in order to reduce the phase delay and improve the phase margin for the control system.

$$I_{d\_damp} = \frac{V_{d(harmonics)}}{R_{damp}} = \frac{V_d - V_{d(fundamental)}}{R_{damp}} \approx \frac{V_d - V_{ds}}{R_{damp}} = \frac{V_{dL}}{R_{damp}} \quad (5\text{-}60)$$

$$I_{q\_damp} = \frac{V_{q(harmonics)}}{R_{damp}} = \frac{V_q - V_{q(fundamental)}}{R_{damp}} \approx \frac{V_q - V_{qs}}{R_{damp}} = \frac{V_{qL}}{R_{damp}} \quad (5\text{-}61)$$

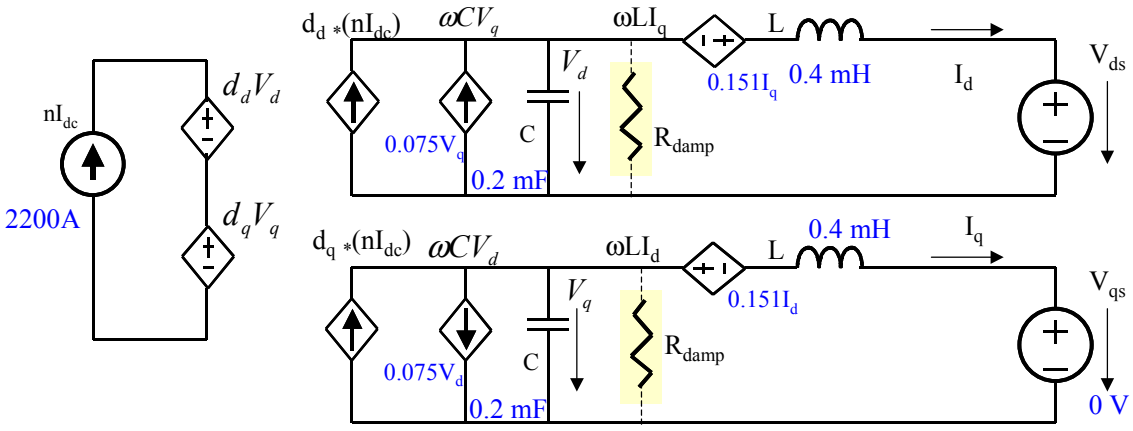



Fig. 5.19. Dq model of five-level CSC based STATCOM with active damping control.

Considering the trade-off between the control bandwidth and the stability margin, the d-channel current controller $H_{id}$ and the q-channel current controller $H_{iq}$ are designed as shown in Equations (5-62) and (5-63). Using a damping resistor of 2.5 Ω, the q-channel current loop gain $T_q$ is shown in Fig. 5.20,

with a crossover frequency of 101 Hz, phase margin of 48 ° and a gain margin of 7.4 dB. Without active damping, the q-channel loop gain $T_q$ will bump up above zero around the resonant frequency (see Fig. 5.21) and the system could become unstable during the transient.

$$H_{id}(s) = 0.3 \cdot \frac{1}{s} \cdot \frac{1}{1+\frac{s}{1800}} \quad (5\text{-}62)$$

$$H_{iq}(s) = 0.3 \cdot \frac{1}{s} \cdot \frac{1}{1+\frac{s}{1800}} \quad (5\text{-}63)$$

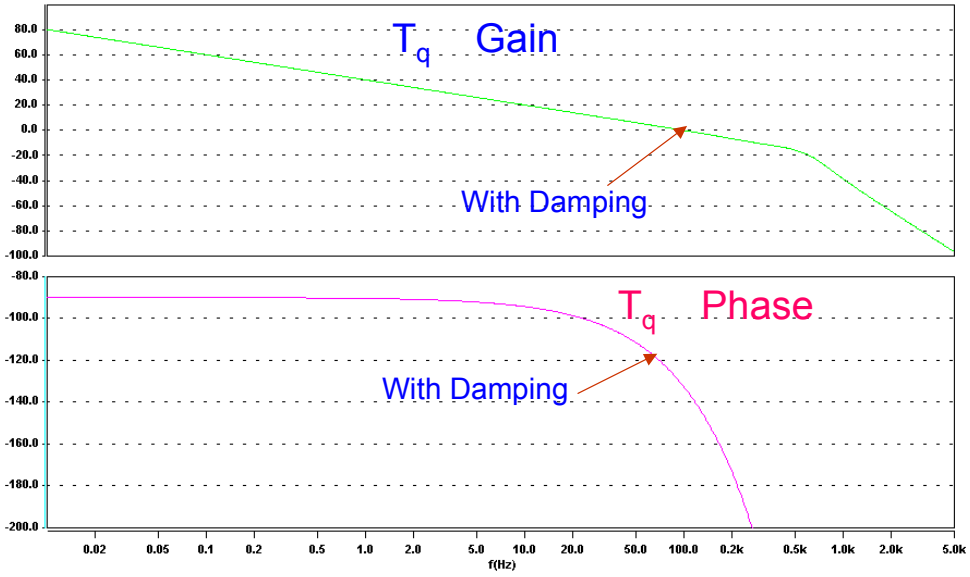



Fig. 5.20. The q-channel current control loop gain $T_q$ with active damping control.

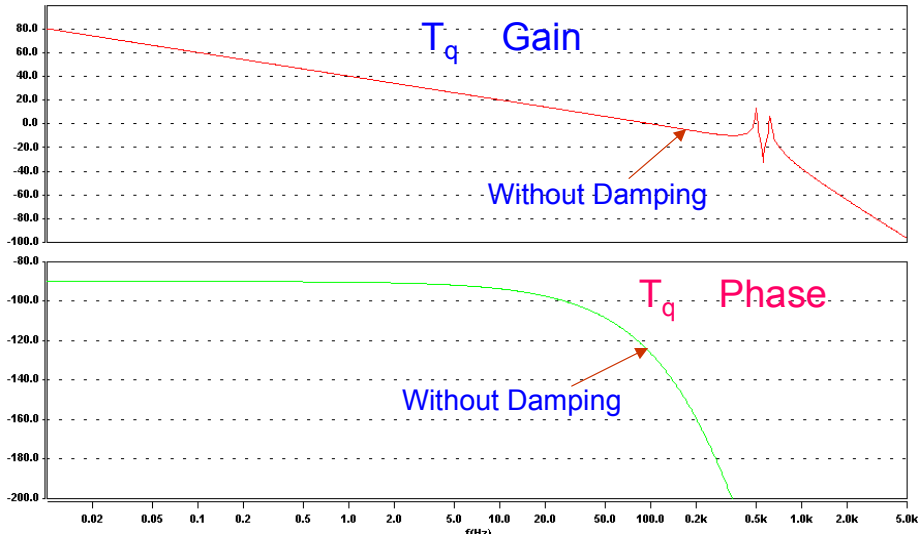



Fig. 5.21. The q-channel current control loop gain $T_q$ without active damping control.

With the designed current controllers, the response of q-channel current $I_q$ to a step command is shown in Fig. 5.22with a delay time of 0.7 ms (switching delay) and rising time of 2.2 ms which is mainly dictated by the current loop control bandwidth.

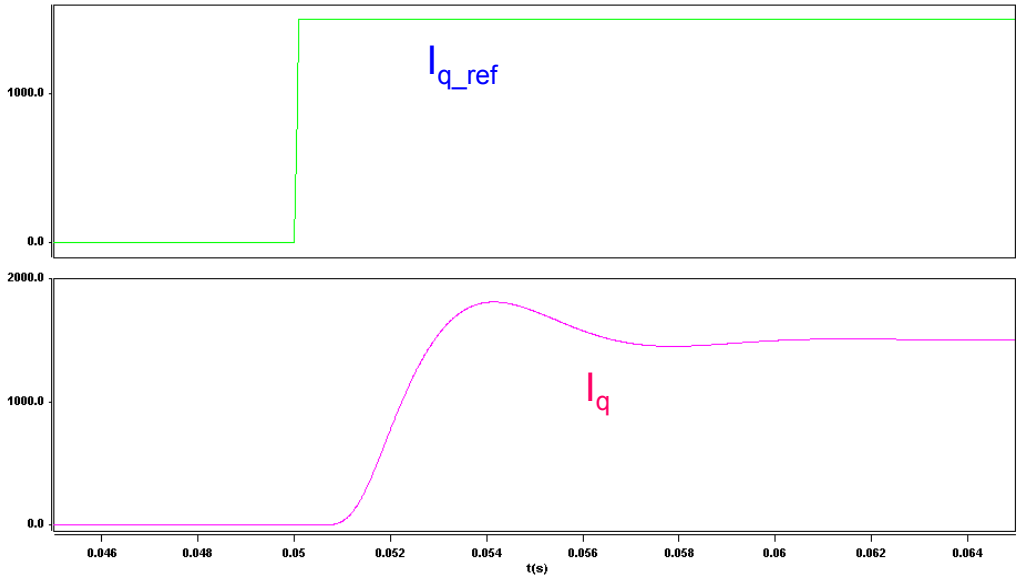



Fig. 5.22. Response of q-channel current $I_q$ to a step command.

The DC-link current controller $H_{idc}$ will control the DC-link inductor charging process and maintain a constant DC source current during the normal operation. Considering the trade-off between the DC-link inductor charging speed and DC current spike during transient, the DC-link current controller is designed as described in Equation (5-64). With the designed controller $H_{idc}$, the DC-link current loop gain $T_{idc}$ has a crossover frequency of 19 Hz, a phase margin of 80° and a gain margin of 14 dB, as shown in Fig. 5.23.

$$H_{idc}(s) = -1 \quad \text{(5-64)}$$

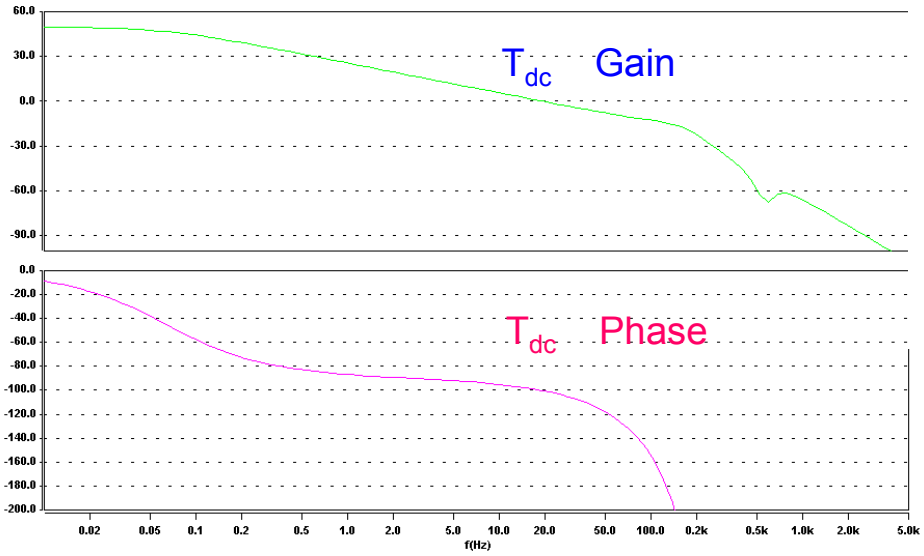



Fig. 5.23. DC-link current control loop gain $T_{idc}$ with active damping control.

Using the designed DC-link controller, the DC-link inductor can be charged from zero to a rated current level (2200 A) within 9 ms with a current overshoot of less than 469 A (23% of the rated current), as shown in Fig. 5.24. The simulated time for the DC-link current to rise from to the final value is pretty close to the time estimated using Equation (5-59) (9 ms and 10 ms, respectively).

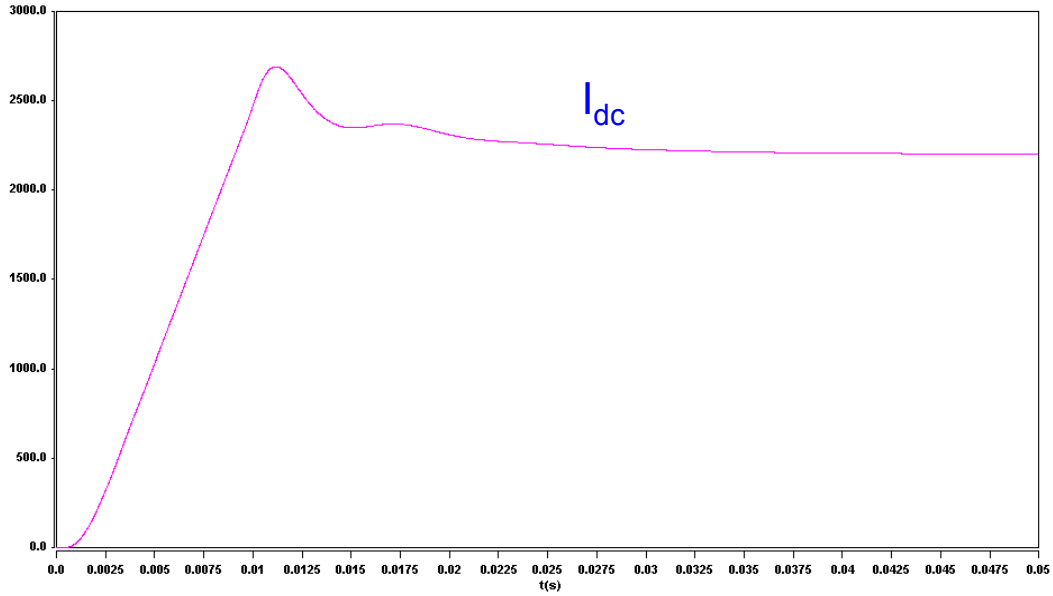



Fig. 5.24. DC-link current charging process.

In the CSC based STATCOM, the modulation index m is defined using Equation (5-65), where $I_{dc}$ is the DC-link current and $I_m$ is the amplitude of the output phase current. With sinusoidal waveforms, the maximum amplitude of the output phase current is $I_{dc}$. So the normal operation range of modulation index m is from –1.225 to 1.225.

$$m = \sqrt{\frac{3}{2}} \cdot \frac{I_m}{I_{dc}} \quad (5\text{-}65)$$

For a given load current, the higher the modulation index, the lower the levels of current harmonics and DC-link current [E4]. The lower DC-link current will cause lower conduction and switching losses for power semiconductor devices in the CSC, resulting in higher system efficiency and easier thermal design. The modulation index controller $H_m$ will regulate the modulation index to a given value. To avoid system oscillation, the modulation index control loop should have a much lower control bandwidth as compared to that of the DC-link current control loop. Based on the operation point of normal lagging var

compensation, the modulation index controller can be designed as shown in Equation (5-69). Using the designed modulation index controller, the modulation control loop has a crossover frequency of 2.3 Hz, a phase margin of 83° and a gain margin of 30dB, as shown in Fig. 5.25.

$$H_m(s) = -\frac{80000}{s} \quad (5\text{-}69)$$

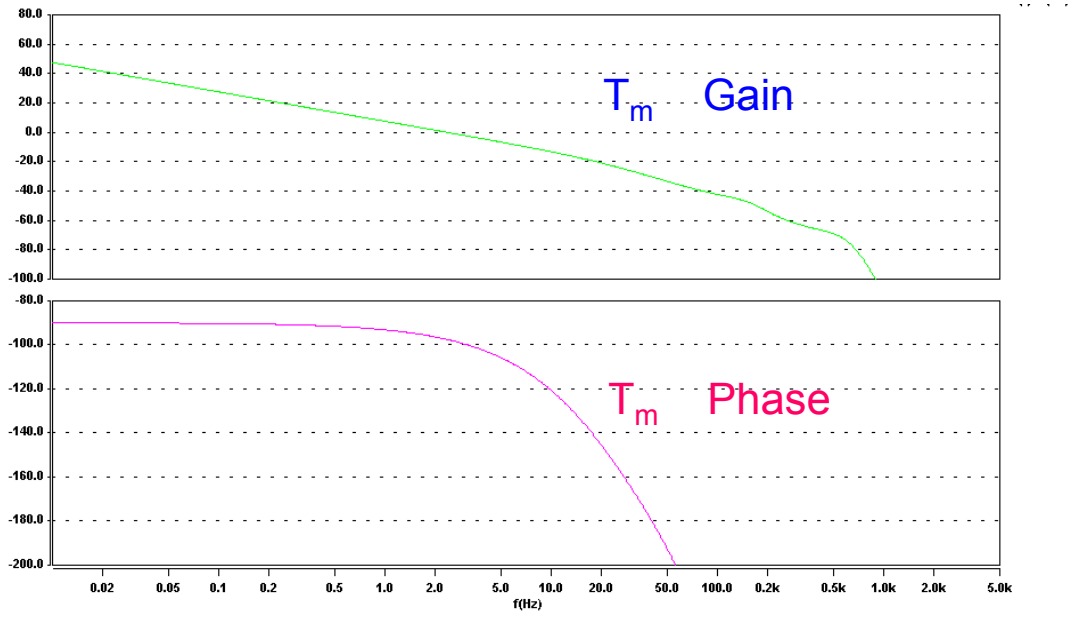



Fig. 5.25. Modulation index control loop gain $T_m$.

With the modulation index controller, the DC-link current will vary according to the load. To track the effect of a step-down command on the reactive current $I_q$, the modulation index m is first quickly deceased to a low value. Then the modulation index loop pulls the modulation index back to the setting value and the DC-link current is slowly discharged to a low level as shown in Fig. 5.26. The response speed of the reactive current $I_q$ for the step-down load is the same as that without modulation index control. However, for a step-up command for the reactive current $I_q$, the corresponding response speed will be much lower since the DC-link current needs to be charged to a higher level before providing the

required reactive current. Therefore, for the system with tight dynamic response speed requirements, the modulation index controller needs to be improved.

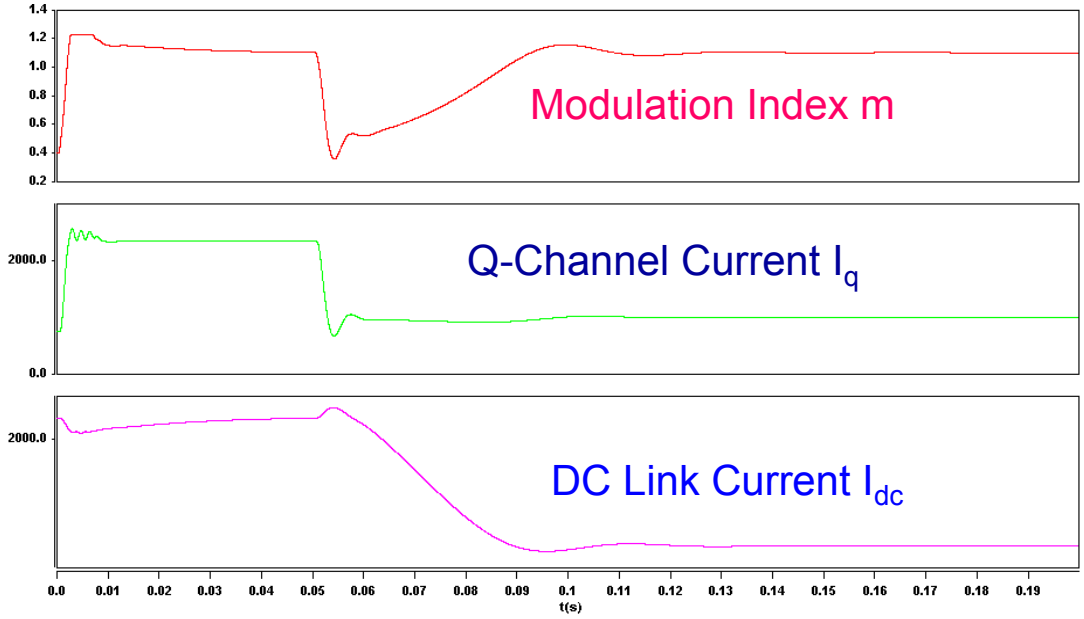



Fig. 5.26. Response of modulation index m to a step-down load change.

## 5.5. Switching Modulation Scheme of the Parallel-Cell Multilevel CSC

SVM is one of the best modulation methods for use in multilevel converters. A novel SVM algorithm for multilevel three-phase converters, proposed in [H8], can be used here to achieve low harmonics in the output currents, minimized switching loss, easy digital implementation, balanced load voltage and current levels, stabilized DC-link current and better DC-link utilization. The steps for the novel SVM are as follows:

1. Select the phase current vector ($I_a$,$I_b$,$I_c$) as the new coordinates; the corresponding output current space vector diagram is thus obtained, as shown in Fig. 5.27.
2. Transfer the reference current space vector from dq coordinates to abc coordinates through the transformation matrix shown in Equation (5-67):

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} d_d \\ d_q \end{bmatrix}, \quad (5\text{-}67)$$

where, $\theta = \omega t$, $\omega$ is the rotating speed of the dq coordinates. Usually, $\omega$ is chosen as $2\pi f$, and f is the fundamental frequency of the power system.

3. Calculate the ceilings ($C_a$, $C_b$ and $C_c$) and floors ($f_a$, $f_b$ and $f_c$) for $d_a$, $d_b$, and $d_c$.

Ceiling $C_a$ is defined as the first integer that is larger than $d_a$ and floor $f_a$ is defined as the first integer that is smaller than $f_a$. $C_b$ and $C_c$ have similar definitions.

4. Select the three nearest vectors and calculate the corresponding duty cycles.

If the sum of floors ($f_a+f_b+f_c$) is equal to –1, the reference vector belongs to the triangle shown in Fig. 5.28 (a). The nearest three vectors are $C_af_bf_c$, $f_aC_bf_c$ and $f_af_bC_c$ and the corresponding duty cycles are $d_a$-$f_a$, $d_b$-$f_b$, and $d_c$-$f_c$.

If the sum of floors ($f_a+f_b+f_c$) is equal to –2, the reference vector belongs to the triangle shown in Fig. 5.28 (b). The nearest three vectors are $f_aC_bC_c$, $C_af_bC_c$ and $C_aC_bf_c$ and the corresponding duty cycles are $C_a$-$d_a$, $C_b$-$d_b$, and $C_c$-$d_c$.

5. Select the switching sequence:

The switching sequence will affect both the output current harmonics and the average switching loss of the power semiconductor device. To achieve the lowest harmonics at the output current, the sequence for three current vectors should be selected according to the space vector's amplitude. The larger the amplitude, the earlier the space vector, as shown in Equation (5-68):

$$\left|V_1\right| \geq \left|V_2\right| \geq \left|V_3\right|, \quad (5\text{-}68)$$

where, $V_1$ is the first space vector and $V_3$ is the last space vector in one switching cycle.

6. Select the switching signals for each CSC cell.

Once the three current space vectors and corresponding duty cycles are obtained, the switching signals for each CSC cell should be selected considering the DC-link currents balancing among all cells, the load balancing for each cell, and lowest total switching loss. To better balance the load and DC-link source current for each cell, the gate signal for each cell should be rotated among the different cells.

Finally, the SVM control block using the above modulation scheme is created in Saber using mast language for the system simulation based on the switching model.

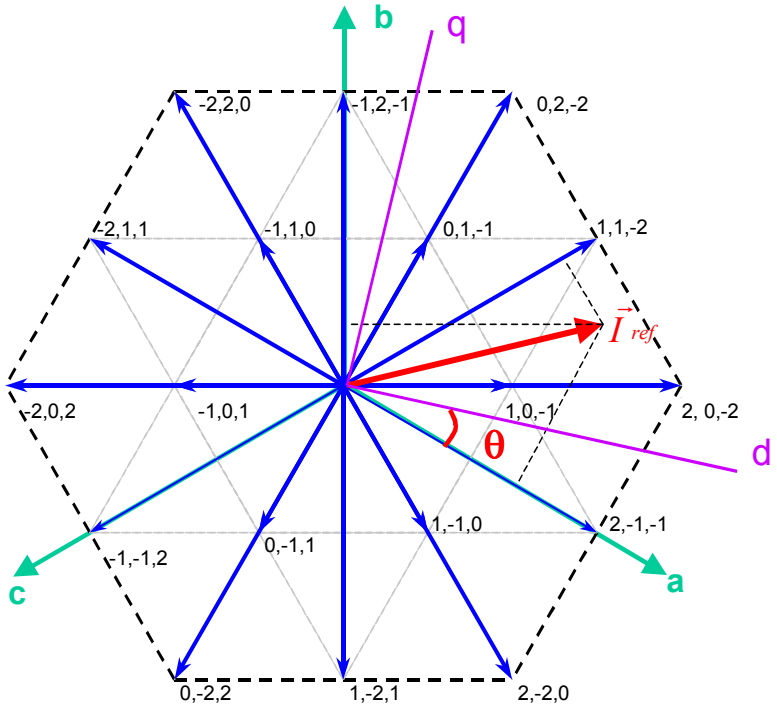
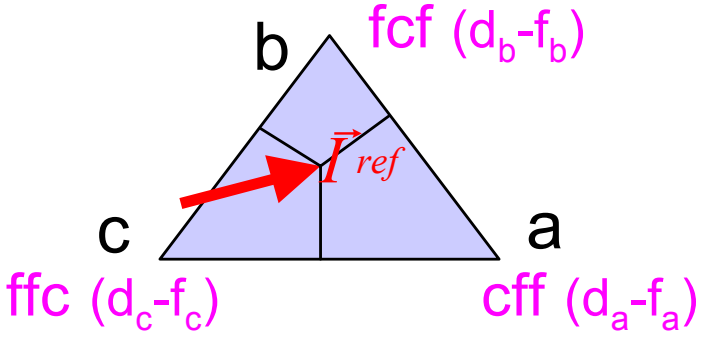
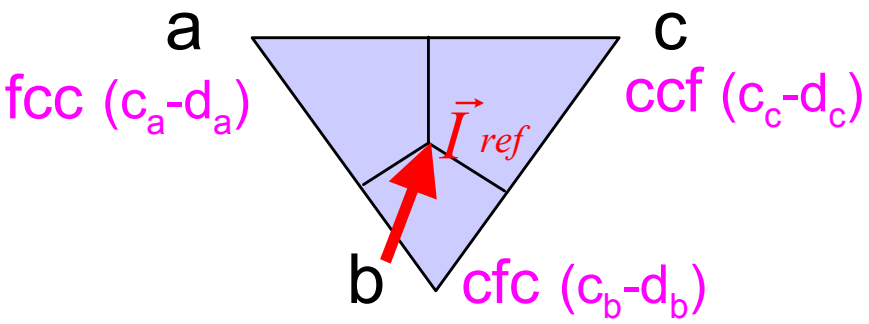



Fig. 5.27. Current space vector diagram of the novel five-level CSC.




(a)




(b)

Fig. 5.28. Current space vector diagram of the novel five-level CSC.

With the increase of the six-switch CSC cells in parallel, the number of current space vectors for the parallel-cell multilevel CSC will exponentially increase and the previously discussed multilevel SVM scheme may be too complicated to use in real applications. For this case, the interleaved multilevel SVM scheme can be used.

### 5.6. Application Example and Simulation Results

Using an asymmetrical ETO in series with a diode as the main switch, the power stage design, modeling, control and switching modulation scheme of the five-level CSC based STATCOM are

analyzed in the previous sections. Based on the previously described design guidelines, the five-level CSC based STATCOM is redesigned and analyzed in this section using the switching model.

Due to the thermal limitation, the ETO device can operate at 1100-A DC-link current with a switching frequency of 1080 Hz. To damp the switching frequency noise, the resonant frequency of the output LC snubber should be much lower than the switching frequency. Due to the power stage delay dictated by the limited switching frequency, it is difficult to push the control bandwidth of the current loop above the resonant frequency of the output LC filter. Considering all these factors, the five-level CSC based STATCOM is redesigned with the following parameters (also see Fig. 5.29):

$L_{dc}$ = 50 mH; L = 1 mH; $C_f$ = 500 μF; $I_{dc}$ = 1100 A; $V_{as}$ = 1021 V; $I_d$ = 1950 A; S = ±2.4 MVA.

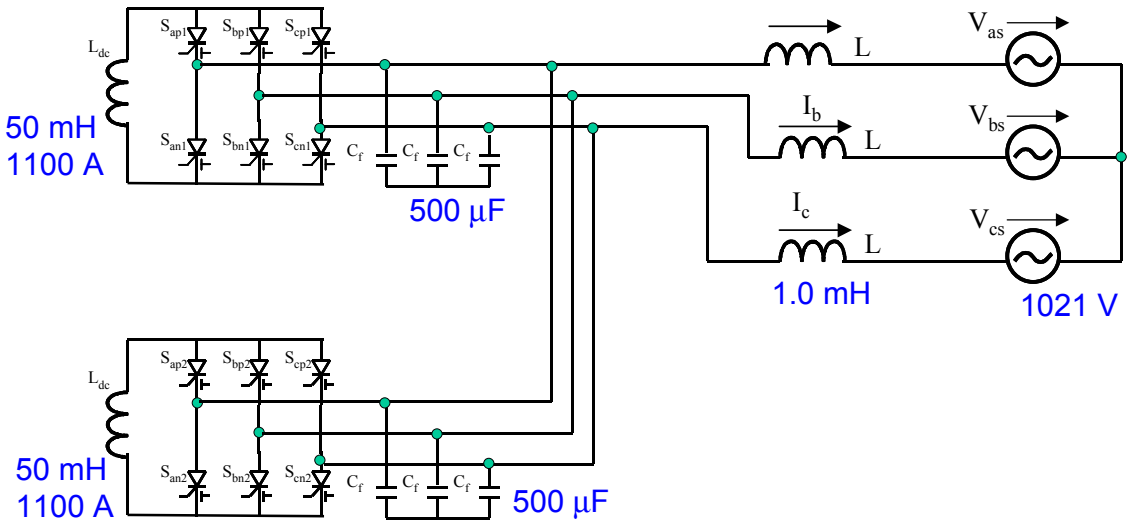



Fig. 5.29. Five-level CSC based STATCOM with redesigned parameters.

Correspondingly, the q-channel reactive current controller $H_{iq}$, d-channel current controller $H_{id}$ and DC-link current controller $H_{idc}$ are redesigned as follows:

$$H_{id}(s) = 0.07 \cdot \frac{1}{s} \cdot \frac{1}{1+\frac{s}{1800}} \quad , (5\text{-}69)$$

$$H_{iq}(s) = 0.07 \cdot \frac{1}{s} \cdot \frac{1}{1+\frac{s}{1800}}, \text{ and (5-70)}$$

$$H_{idc}(s) = -3 . \text{ (5-71)}$$

The control bandwidth for the q-channel current $I_q$ is about 27 Hz with a phase margin of 75° and a gain margin of 8.7 dB. For DC-link current control loop, the control bandwidth is 10.5 Hz with a phase margin of 62° and a gain margin of 13.4 dB.

The five-level CSC based STATCOM shown in Fig. 5.29 is implemented in Saber. Under the lagging var compensation condition (q-channel current $I_q$ = 1500 A), the simulated output currents are shown in Fig. 5.30. It is obvious that the output currents of cells 1 and 2 are similar, and there is a five-level total output current, which results in lower current harmonics. Only switching-frequency ripples are present in the DC-links with balanced fundamental reactive power compensation and the ripple current for the DC-links is less then 1.2%, as displayed in Fig. 5.31.

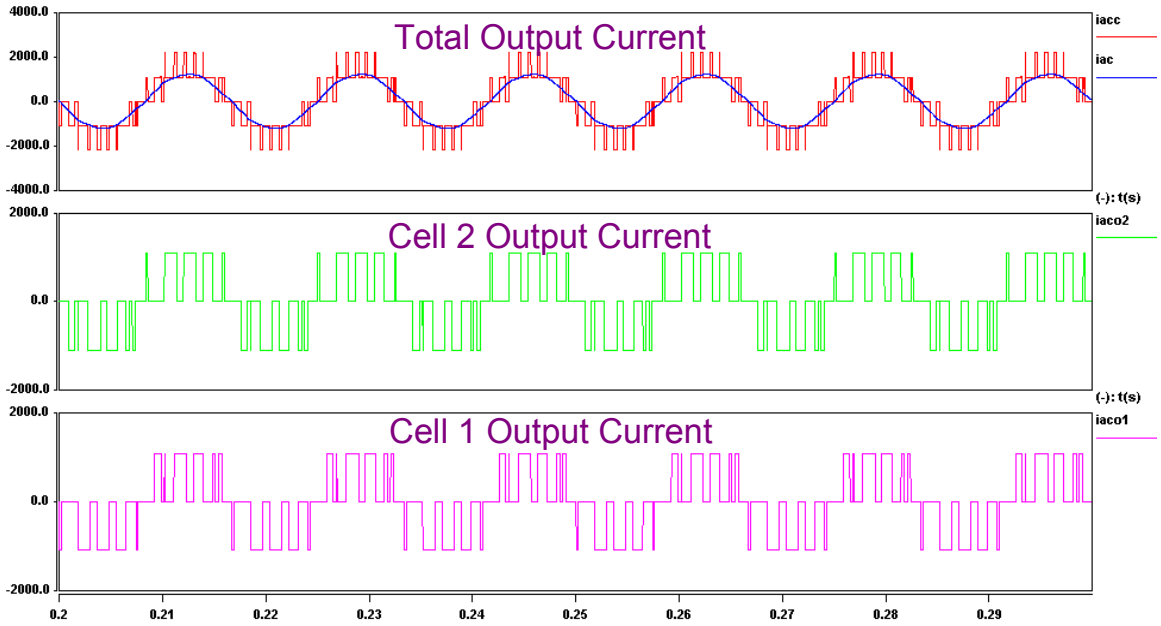



Fig. 5.30. Simulated output current waveforms.

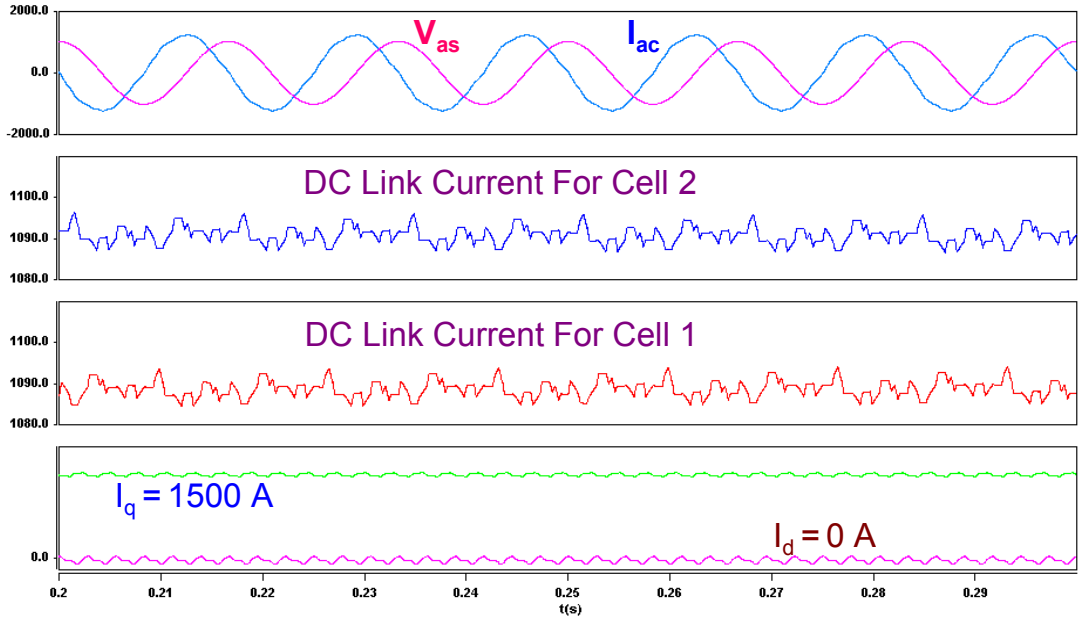



Fig. 5.31. Simulated duty cycles and DC-link current waveforms.

During start up, the DC-links are uniformly charged to the setting value within 33 ms, as shown in Fig. 5.32. No external staring components are needed for the start-up charging process since the CSC based converter operates like a Buck rectifier in this case. Under the standby mode that does not require fundamental current, the CSC based STATOM injects only small levels of harmonic current into the system due to the multilevel output current and second-order filter formed by filter capacitor $C_f$ and coupling inductor L.

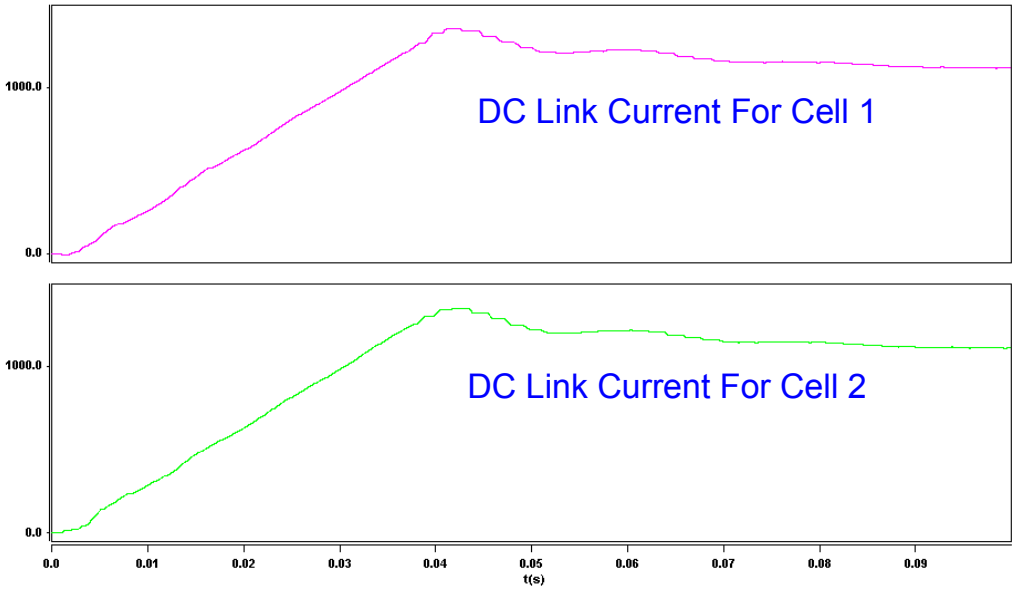



Fig. 5.32. Charging process of the DC-link Inductors.

For the step-up and step-down command, the q-channel reactive current can track the reference within 10 ms, as mainly dictated by the current control loop, and as shown in Fig. 5.33. Cells 1 and 2 have similar output currents even during the transient, as shown in Fig. 5.34.

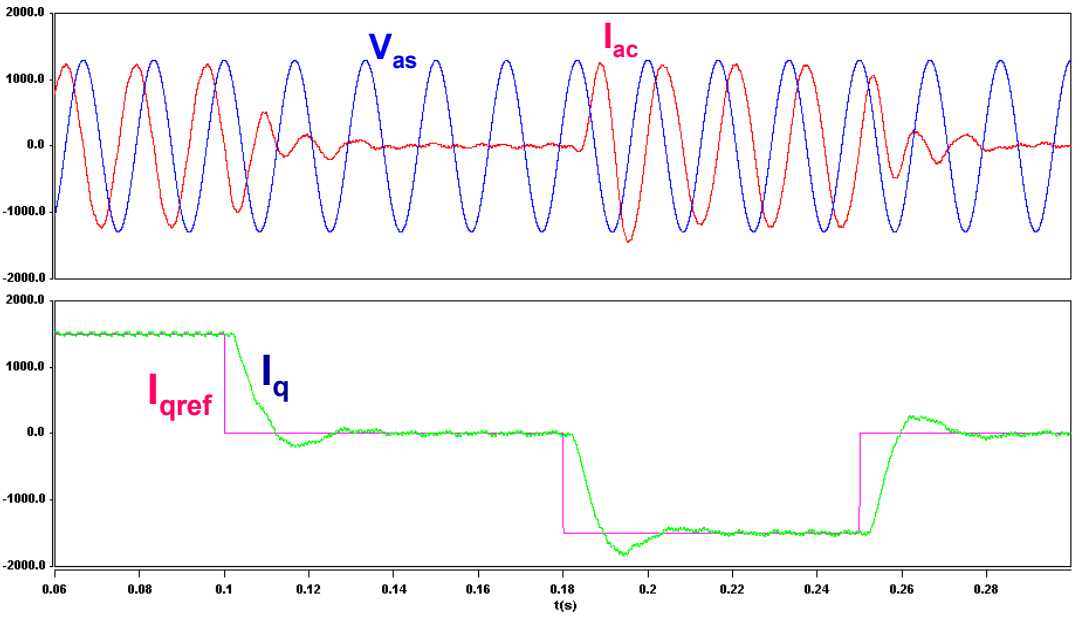



Fig. 5.33. Simulated step response.

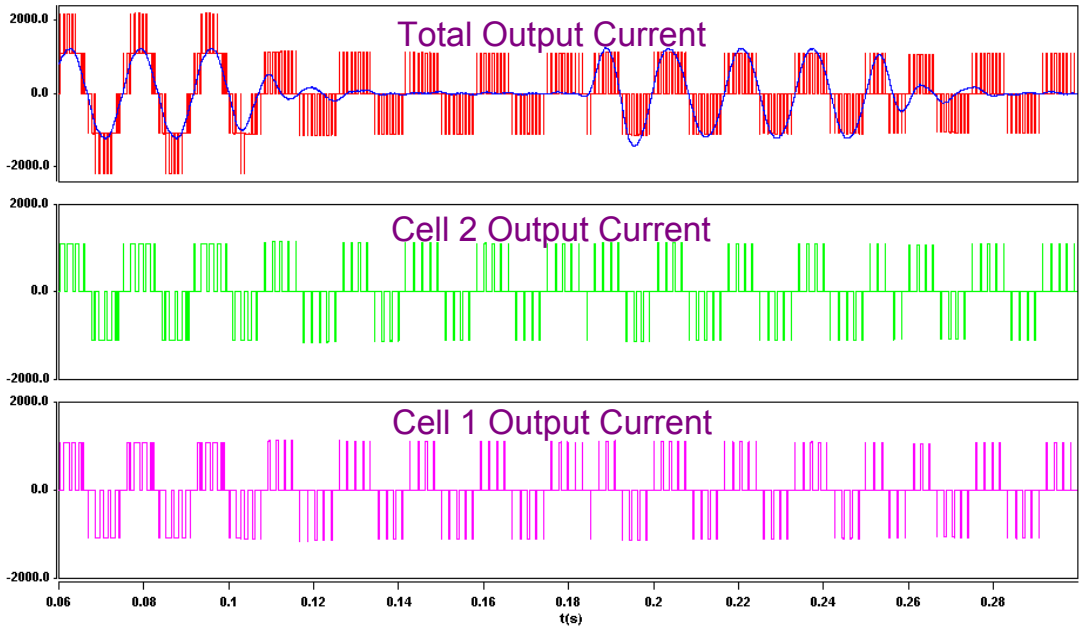



Fig. 5.34. Simulated output current waveforms during step response.

## 5.7. Conclusion

Based on the six-switch CSC cell, this chapter proposes a novel multilevel CSC-- the parallel-cell multilevel CSC. The power stage design, modeling, control and modulation scheme for the parallel-cell multilevel CSC are studied.

Based on the average model of the novel multilevel CSC at dq rotating coordinates, the small-signal model can be derived around the steady-state operation point. Then, the controllers for reactive current, DC-link current and modulation index can be designed. To prevent oscillation between the output filter capacitor and the coupling inductor, an active damping control is employed. For different load currents, the modulation index controller will maintain a constant modulation index by varying the DC-link current level, the result of which is low harmonics in the output current and lower system loss. However, for modulation index control, the step-up dynamic response will suffer due to the slow charging process.

Therefore, for systems with tight requirements for dynamic response, the modulation index control must be improved.

A novel SVM scheme for the parallel-cell multilevel CSC is proposed in this chapter. Based on the selected coordinates of three phase currents ($I_a$, $I_b$, $I_c$), for a given reference current vector, the nearest three current vectors and corresponding duty cycles can be easily derived. Then, the switching signal for each cell can be created considering DC-link current balancing, load balancing, lower switching loss and lower harmonics.

Due to the improved turn-on performance, forced turn-off and load-commutated turn-off capabilities, either the symmetrical ETO or the asymmetrical ETO in series with a diode is suitable for CSCs that require devices with reverse voltage-blocking capability. Using the asymmetrical ETO (ETO4045TA) in series with a diode as the main switch, the operation condition of the multilevel CSC is designed to maximize the output power rating while meeting the electrical and thermal requirements. Given the junction temperature of 115 °C and water temperature of 55 °C, the 4-kA/4.5-kV ETO (ETO4045TA) can operate at 1080 Hz with 1100-A DC-link current. For other devices, a similar analysis can be performed and corresponding operation conditions can be obtained.

The filter capacitor bypasses the output current harmonics while passing the fundamental output current. So the filter capacitor should be designed to behave as a short circuit for switching-frequency noise and as an open circuit for fundamental-frequency current. Together with the filter capacitor, the coupling inductor will form a second-order filter to attenuate the current harmonics. The resonant frequency of the output filter should be much lower than the switching frequency, and should be located

at a point that is not an integer times the level of the fundamental frequency. Active-damping control should be used to prevent oscillation between the load and output filter. The coupling inductor should be designed to be as low as possible in order to reduce the voltage stress on the switches. The DC-link inductor will smooth the DC-link current and maintain the normal operation of the multilevel CSC. For a given current ripple, the DC-link inductor should be designed to be as low as possible to reduce its conduction loss and cost.

Due to the phase delay caused by both the limited power stage switching frequency and the output filter of the five-level CSC based STATCOM, it is difficult to push the control bandwidth of the reactive current control loop above the resonant frequency of the output filter. The higher the switching frequency, the smaller the output filer and the lower the phase delay, which results in a higher control bandwidth. On the other hand, the higher the switching frequency, the higher the switching loss and the lower the output power rating. So there is a trade-off between the output power and dynamic response.

Using the above design guidelines, the switching model for a five-level CSC based STATCOM is built and simulated in Saber. These simulation results show that the proposed multilevel CSC has the advantages of high power capacity, low harmonics in the output current, fast dynamic response, minimum components and modular design. Therefore it is very suitable for high-power applications that require high current, low harmonics and fast dynamic response, such as induction motor drives, high-current amplifiers and FACTS devices.

# Chapter 6. Comparison of Multilevel CSC and VSC in STATCOM Applications

## 6.1. Introduction

In electrical power systems, the Static Var Compensator (SVC) is important for maximizing power transmission capability and minimizing power transmission losses. Traditionally, either thyristor-switched capacitors (TSCs) or thyristors-controlled reactors (TCRs) are used to provide leading or lagging reactive power to the power system due to their low maintenance and low cost [A7, J2]. However, their dynamic performance is slow and needs to be improved. Recently, because of their excellent dynamic performance, as required in power systems, power electronic switching converters have been applied in var compensation. Such 'advanced SVCs' are called STATCOMs [J3-J5]. The STATCOM behaves like a controllable voltage or current source. In contrast to a TSC or a TCR that produces the reactive power by capacitor or inductor banks, the STATCOM provides the reactive power using circulating energy between the phases of the AC system. One of the preferable circuit topologies for the STATCOM is the multilevel VSC. By applying the multilevel VSC with a proper control scheme, an alternating voltage source in phase with the transmission line voltage is produced. Each phase of this alternating voltage source is fed to each AC line through a small coupling inductance to form a shunt-connected STATCOM, as shown in Fig. 6.1. The corresponding single-phase equivalent circuit is shown in Fig. 6.2.

Since the output voltage ($V_C$) of the STATCOM is in phase with the system voltage ($V_S$), the current drawn by the STATCOM ($I_C$) can be determined using Equation (6-1).

$$I_C = \frac{V_S - V_C}{j(X_S + X_C)}\ , \quad (6\text{-}1)$$

where the $X_S$ and $X_C$ are the impedances of Ls and $L_C$ at line frequency as shown in Fig. 6.1.

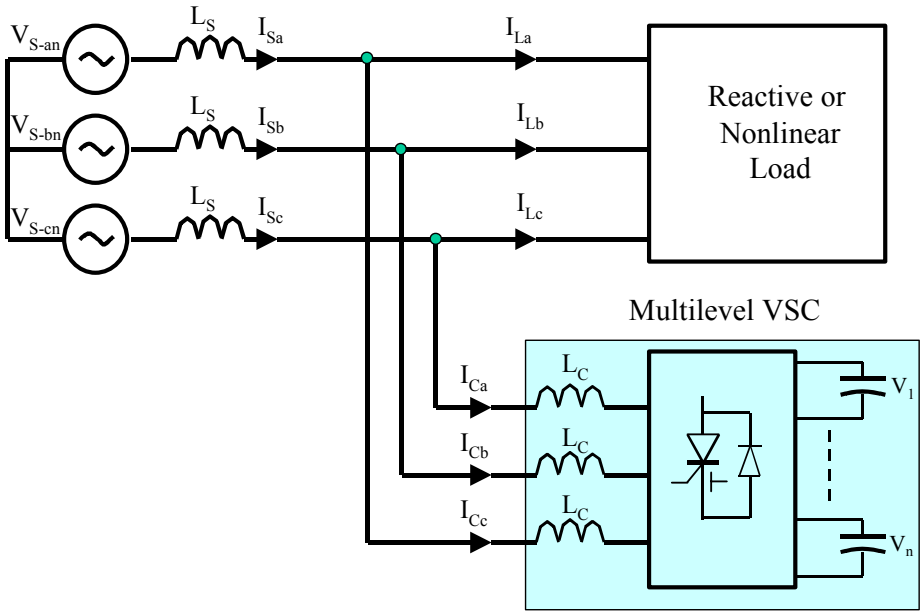



Fig. 6.1. Connecting a multilevel voltage source converter to a power system for STATCOM applications.

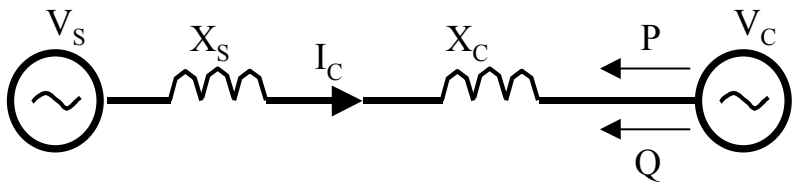



Fig. 6.2. Single-phase equivalent circuit of a STATCOM connected to an AC system.

Whenever the amplitude of $V_C$ is larger than that of $V_S$, leading current is drawn from the system and the converter behaves like a capacitor. On the other hand, when the amplitude of $V_C$ is smaller than that of

$V_S$, lagging current is drawn from the system and the converter behaves like an inductor. The corresponding phasor diagrams are shown in Fig. 6.3.

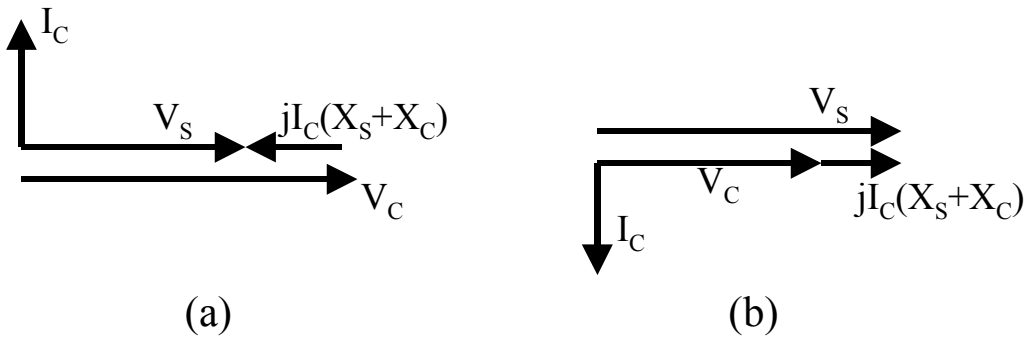



Fig. 6.3. Phasor diagrams for single-phase equivalent circuit shown in Fig. 6.2: (a) capacitive current and (b) inductive current ($V_S$ in phase with $V_C$).

In the real application, of course, a small amount of active power is also drawn from the AC system to compensate the losses of the STATCOM. Under this condition, $V_S$ is no longer in phase with $V_C$, and there is a phase angle $\delta$ (positive when $V_C$ is leading $V_S$) between them as shown in Fig. 6.4.

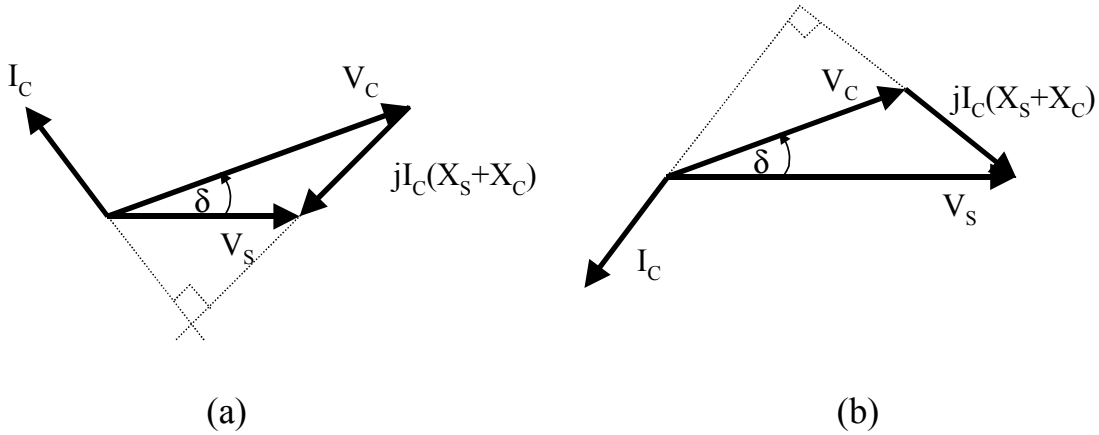



Fig. 6.4. Phasor diagrams for the single-phase equivalent shown in Fig. 1.2: (a) capacitive current and (b) inductive current ($V_S$ is not in phase with $V_C$).

From Fig. 6.2 and Fig. 6.4, the real power (P) provided by the STATCOM can be determined as follows:

$$P = 3\frac{V_S V_C}{(X_S + X_C)}\sin(\delta), \qquad (6\text{-}2)$$

where δ is the phase angle between $V_C$ and Vs.

Similarly, the reactive power delivered by the STATCOM is given by the following:

$$Q = 3\frac{V_C[V_C - V_S\cos(\delta)]}{(X_S + X_C)}. \qquad (6\text{-}3)$$

According to Equation (6-2), the real power can be controlled by varying the phase angle δ to charge or discharge the storage capacitors in the STATCOM. Equation (6-3) shows that the reactive power is controlled by changing the amplitude of the STATCOM output voltage so that the required leading or lagging reactive power can be delivered to the system.

Due to the operation principle, the STATCOM can provide the rated capacitive or inductive current even when the system voltage is low. This is a big advantage over conventional TSCs or TCRs whose currents decrease linearly with the system voltage since both the TSC and the TCR are basically fixed impedance systems. A comparison of the theoretical steady state V-I characteristics among a TSC, a TCR and a STATCOM is shown in Fig. 6.5. Notice that, in both the inductive and capacitive regions, the STATCOM also has transient overload capability of 20% for a short period (usually several line cycles).

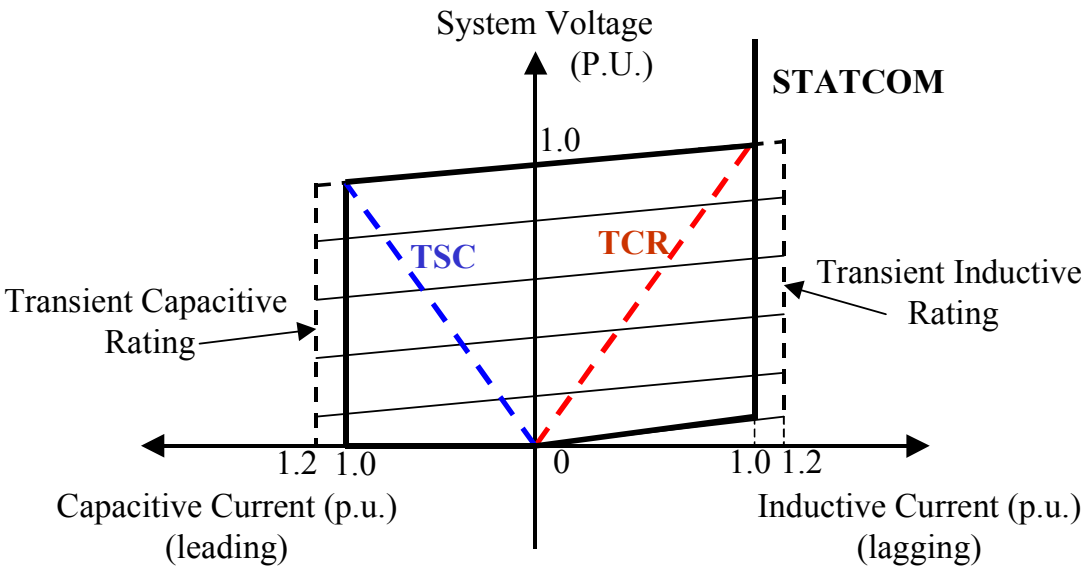



Fig. 6.5. Comparison of the steady state I-V characteristics.

Traditionally, the two-level VSC is mainly used as the converter topology in STATCOM applications [A7, J2]. With the requirements of high power rating and low harmonics, many two-level VSCs must be connected together through the coupling transformer [J3-J5], which is lossy, heavy and expensive. The dynamic response is relatively slow for the interleaved converter based STATCOM due to the lower switching frequency. To achieve fast dynamic response speed, the multilevel VSC with higher equivalent switching frequency is needed. The cascaded multilevel VSC is one of the best topologies for modern STATCOM applications due to its modular structure and control [H1-H5]. The cascaded converter has a flexible circuit layout and thus does not require either clamping diodes or voltage balancing capacitors. This topology is also the easiest to expand to high power levels. There is a degree of freedom to increase or decrease the power rating of the converter system by using an identical layout and packaging. Moreover, it can operate at a lower switching frequency in order to satisfy the given total harmonics distortion (THD) requirement. The switching loss can then be improved. At the same line-to-line voltage,

compared with the two-level VSC, a slightly higher DC capacitance is required, but lower-voltage-rating capacitors can be employed [H10-H11].

The parallel-cell multilevel CSC is another suitable candidate for STATCOM application due to its modular design, low harmonics, high current, high power, easy start-up process and fast dynamic response speed. In this chapter, the two topologies will be compared in terms of their power semiconductor devices, system losses, dynamic responses, controls and harmonics.

## 6.2. STATCOM Design Based on Cascaded Three-Level VSC

The structure of the cascaded multilevel VSC-based STATCOM is shown in Fig. 6.6. For the cascaded multilevel VSC, the basic cell is an H-bridge Building Block (HBBB), which is a single-phase VSC with a separate DC-link voltage source [H6]. Through proper control of the power semiconductor devices, the HBBB can have three output voltage levels, $+V_{dc}$, 0 and $-V_{dc}$, where $V_{dc}$ is the DC-link voltage for each HBBB. With n HBBBs in series for each phase, the cascaded multilevel VSC can have 2n+1 levels in phase voltage and 4n+1 levels in line-to-line output voltage, since the total output voltage is the sum of the output voltage for each cell. The multilevel output voltage is applied to the power line through coupling inductor L, which behaves like a first-order filter for current harmonics.

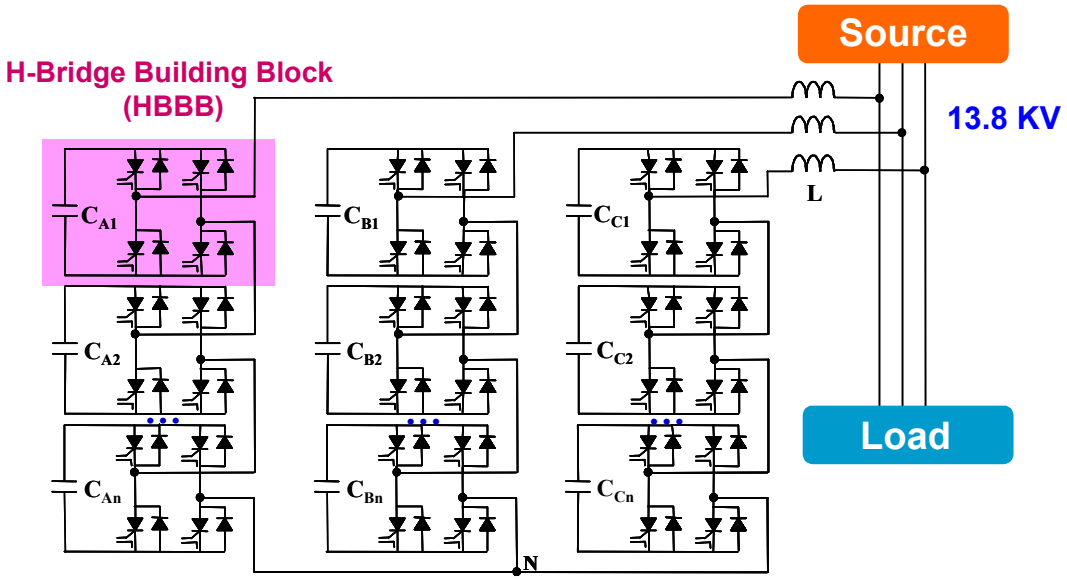



Fig. 6.6. Structure of the cascaded multilevel VSC based STATCOM.

In this chapter, the n-level cascaded VSC is defined as the cascaded multilevel VSC with n-level phase voltage. With one HBBB in each phase, the cascaded multilevel VSC is defined as the three-level cascaded VSC since it has a three-level output phase voltage. To show the design guidelines for the cascaded multilevel VSC based STATCOM, the three-level VSC with one HBBB in each phase is chosen as the main topology, as shown in Fig. 6.7.

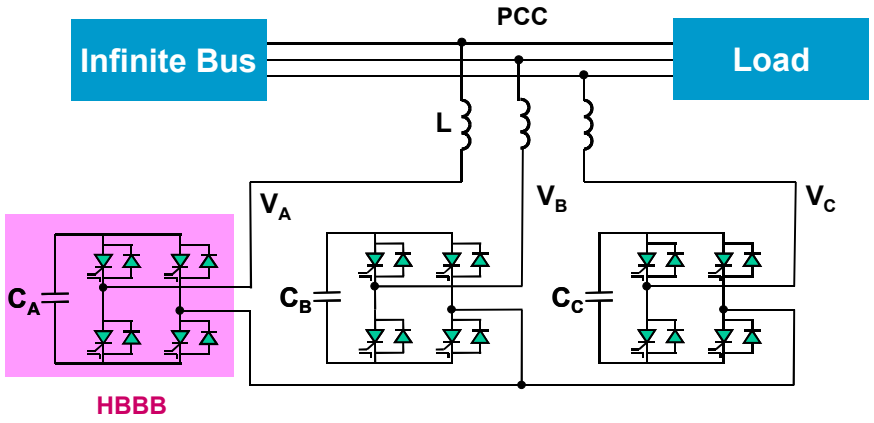



Fig. 6.7. Structure of the three-level VSC based STATCOM.

To fully utilize the capability of the ETO device, the McMurry snubber circuit [H9] can be used to limit the turn-on di/dt, turn-off dv/dt and switching loss, as shown in Fig. 6.8.

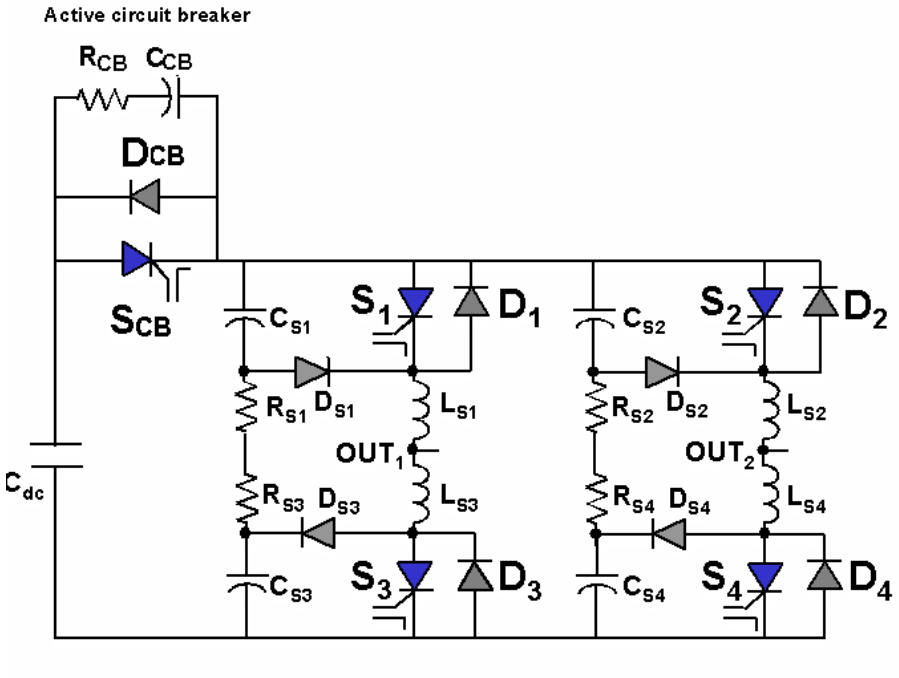



Fig. 6.8. Structure of HBBB with McMurry snubber circuit [12].

Based on the McMurry snubber circuit, during the turn-off transient, the maximum device voltage $V_{s\text{-}max}$ and the maximum device current $I_{s\_max}$ can be estimated using Equations (6-4) and (6-5), where $V_{dc\_max}$ is the maximum DC-link voltage that is dictated by the device DC-link voltage rating, $I_{rms}$ is the load RMS current, and $R_s$ is the total snubber resistance for each branch in the HBBB ($R_s = R_{s1} + R_{s2}$).

$$V_{s\_\max}(I_{rms}) = V_{dc\_\max} + \sqrt{2} \cdot I_{rms} \cdot R_s \qquad (6\text{-}4)$$

$$I_{s\_\max}(I_{rms}) = \sqrt{2} \cdot I_{rms} \qquad (6\text{-}5)$$

During the turn-on transient, the maximum diode reverse voltage $V_{d\text{-}max}$ and peak device current $I_{s\text{-}peak}$ can be approximated using Equations (6-6) and (6-7), respectively. The device current rising rate $di_A/dt$ is limited by the di/dt snubber inductor $L_s$, as shown in Equation (6-8), where $V_{dc\_max}$ is the maximum DC-

link voltage applied to the device, $L_s$ is the total snubber inductance for each branch in the HBBB ($L_s = L_{s1}+L_{s2}$), and $C_s$ is the snubber capacitance for each device ($C_{s1} = C_{s2} = C_s$).

$$V_{d\_\max} = V_{dc\_\max} \cdot (1 + \frac{R_s}{\sqrt{\frac{L_s}{2C_s}}}) \quad (6\text{-}6)$$

$$I_{s\_peak}(I_{rms}) = \sqrt{2} \cdot I_{rms} + \frac{V_{dc\_\max}}{\sqrt{\frac{L_s}{2C_s}}} \quad (6\text{-}7)$$

$$di_A / dt = \frac{V_{dc\_\max}}{L_s} \quad (6\text{-}8)$$

The snubber capacitor $C_s$ will limit the turn-off dv/dt and reduce the turn-off switching loss for the ETO device. The larger snubber capacitance will result in lower turn-off switching loss in the ETO device and will cause more snubber loss. Similarly, the large snubber inductance will reduce both the turn-on loss of ETO device and the reverse-recovery loss of the freewheeling diode, and will also induce more snubber loss. There is a trade-off in the design of these snubber components.

To fully recover the di/dt snubber before the next switching action, the time constant τ, defined in Equation (6-9), should be designed according to the minimum pulse width and dead-time between the two turn-on commands for the two switches in each branch.

$$\tau = \frac{L_s}{R_s} \quad (6\text{-}9)$$

If a 4-kA/4.5-kV ETO (ETO4045TA) and a 2-kA/4.5-kV fast diode (from ABB) are used as the main switch and freewheeling diode for three-level VSC based STATCOM, the maximum electrical operation parameters are as follows:

$V_{dc}$ = 2800 V, $I_{s\_max}$ = 2000 A, $di_A/dt$ = 400 A/μs, $V_{dm}$ = 4000 V,

where $V_{dc}$ is the DC bus voltage for each HBBB, $I_{s\_max}$ is the maximum amplitude of the load current, $di_A/dt$ is the rising rate of anode current for the ETO device which is mainly limited by the reverse-recovery performance of the freewheeling diode, and $V_{dm}$ is the peak device voltage during turn-off.

Based on the electrical operation parameters and design guidelines shown in Equations (6-4) to (6-9), the snubber parameters are designed as follows:

$C_s$ = 0.5 μF, $L_s$ = 7 μF, $R_s$ = 0.5 ohm.

With the designed snubber parameters, the switching loss for the ETO device can be characterized as shown in Fig. 4.18 in Chapter 4 and the turn-off switching loss can be approximated using Equation (4-15) in chapter 4. Since the ETO device only performs the switching function during half of the line cycle and with a positive load current, the average switching loss for ETO the device can be approximated using Equation (6-10), assuming the DC-link voltage $V_{dc}$ and junction temperature $T_j$ for the ETO device have only a slight ripple during one line cycle.

$$E_{off\_avg}(I_{rms},V_{dc},T_j)=(0.00305\cdot\tfrac{\sqrt{2}}{\pi}I_{rms}-0.15)\cdot(0.33+0.333\cdot10^{-3}V_{dc})\cdot\left[1+0.313\cdot10^{-2}\cdot(T_j-25)\right] \quad (6\text{-}10)$$

The on-state voltage drop model for the 4-kA/4.5-kV ETO (4045TA) is the same as that shown in Equation (4-13) from Chapter 4. Using a sinusoidal pulse width modulation (SPWM) scheme [13], the duty cycle for the ETO device, $D_{ETO}$, can be derived as shown in Equation (6-11), where M is the modulation index defined as the ratio between the amplitude of the output phase voltage and the DC-link voltage $V_{dc}$ when the load RMS current is zero (M= 0-1), α is the phase angle for the load current and ϕ is the power factor angle.

$$D_{ETO}(M,\phi,\alpha)=\tfrac{1}{2}\cdot[1+M\cdot\sin(\alpha+\phi)] \quad (6\text{-}11)$$

Since the ETO device only conducts current during half of the line cycle, its average conduction loss can be derived using Equation (6-12), where $I_{rms}$ is the RMS load current, $V_F$ is the on-state voltage drop

and $D_{ETO}$ is the duty cycle for the ETO device. The conduction loss is highly dependent on the power factor angle $\phi$. When the power factor equals to 1 ($\phi = 0°$), the conduction loss is the highest. On the other hand, the conduction loss is lowest with power factor of 0 ($\phi = 90°$), as shown in Fig. 6.9. Therefore, comparing with the kW rating ($\phi = 0°$), the kVA rating ($\phi = 90°$) for the multilevel VSC based STATCOM will be higher due to the lower conduction loss in this case. In this chapter, the STATCOM design is mainly based on the kVA rating with reactive power compensation. For the real power compensation, the KW rating of the STATCOM can be designed using a similar method.

$$P_{Loss\_on\_ETO}(I_{rms}, M, \phi, T_j) = \frac{1}{2\pi}\int_0^{\pi} \sqrt{2} I_{rms} \sin(\alpha) \cdot V_F(\sqrt{2} I_{rms} \sin(\alpha), T_j) \cdot D_{ETO}(M, \phi, \alpha) d\alpha \quad (6\text{-}12)$$

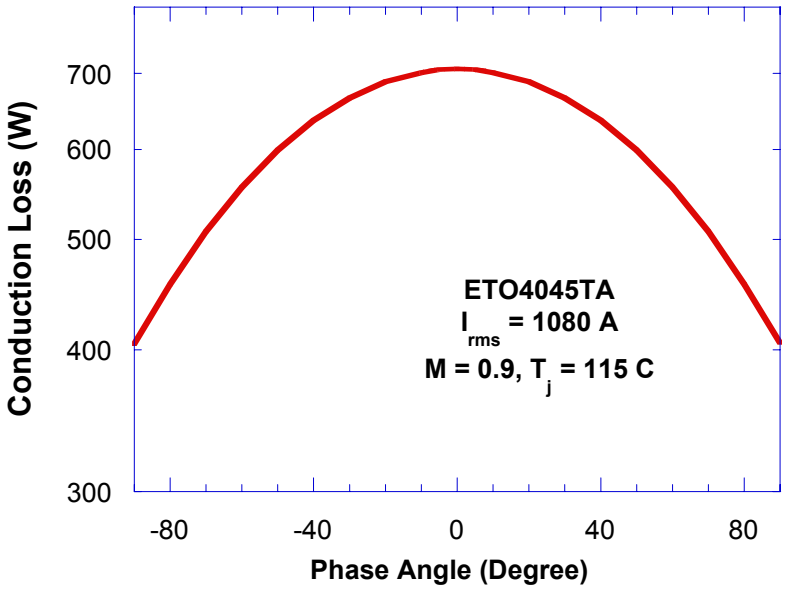



Fig. 6.9. Average conduction loss for ETO4045TA.

Using a cooling system similar to that shown in Section 3 of Chapter 4, given the device junction temperature $T_j$ and water temperature $T_w$, the switching frequency $f_{sw}$ can be calculated using Equation (6-13).

$$f_{sw}(I_{rms},T_j,T_w,M,V_{dc},\phi)=\frac{\frac{T_j-T_w}{R_{thjw}}-P_{loss\_on\_ETO}(I_{rms},M,\phi,T_j)}{E_{off\_avg}(I_{rms},V_{dc},T_j)} \quad (6\text{-}13)$$

Since the total power loss is fixed for a given junction temperature $T_j$ and cooling water temperature $T_w$, the higher the load RMS current $I_{rms}$, the higher the conduction loss, the lower the switching loss and switching frequency, as shown in Fig. 6.10. In other word, from the standpoint of thermal limitation, for a given water temperature $T_w$ and switching frequency $f_{sw}$, the DC-link voltage $V_{dc}$ and load RMS current $I_{rms}$ should be properly designed to maintain the junction temperature $T_j$ within a safe region.

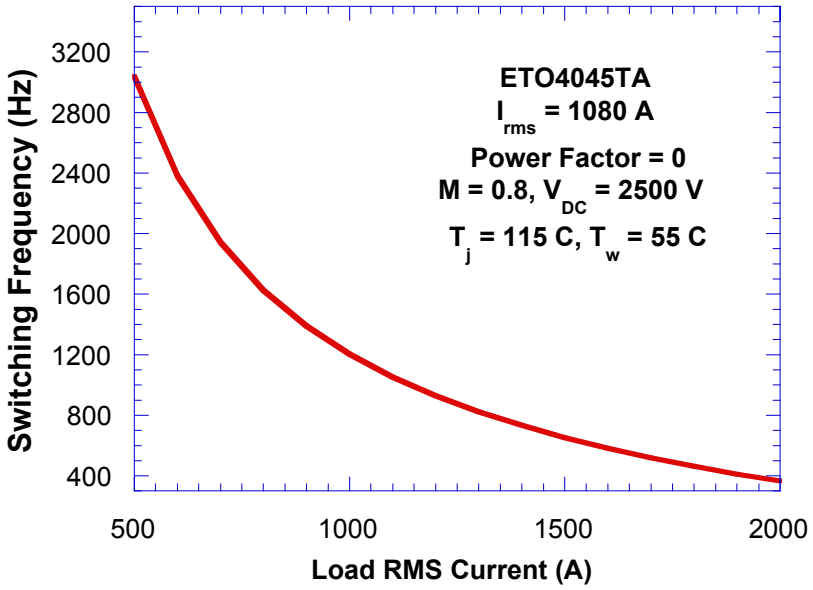



Fig. 6.10. Relationship between load current and switching frequency for the ETO4045TA in a three-level VSC based STATCOM.

Similar to the design guideline for the six-switch CSC cell described in section 4.3 of Chapter 4, to safely turn-off the peak device current of $I_m$, the ETO device should have a maximum repetitive turn-off current $I_{tq}$ that is higher than $I_m$. Usually, $I_{gt} = 2I_m$ is chosen as the design criterion. To prevent device

avalanche breakdown, the peak device voltage $V_{Dm}$ should always be kept below the device blocking voltage. Combining these electrical and thermal limitations, the operation point for the three-level VSC based STATCOM could be designed according to the design curve shown in Fig. 6.11. For a given conditions of $T_j$ = 115 °C, $T_w$ = 55 °C, $V_{dc}$ = 2500 V, M = 0.8, $\phi$ = 90° and $f_{sw}$ = 1080 Hz, the load RMS current $I_{rms}$ of 1080 A can be chosen to meet both the thermal and electrical requirement. The load RMS current rating is mainly thermally limited due to the higher switching loss.

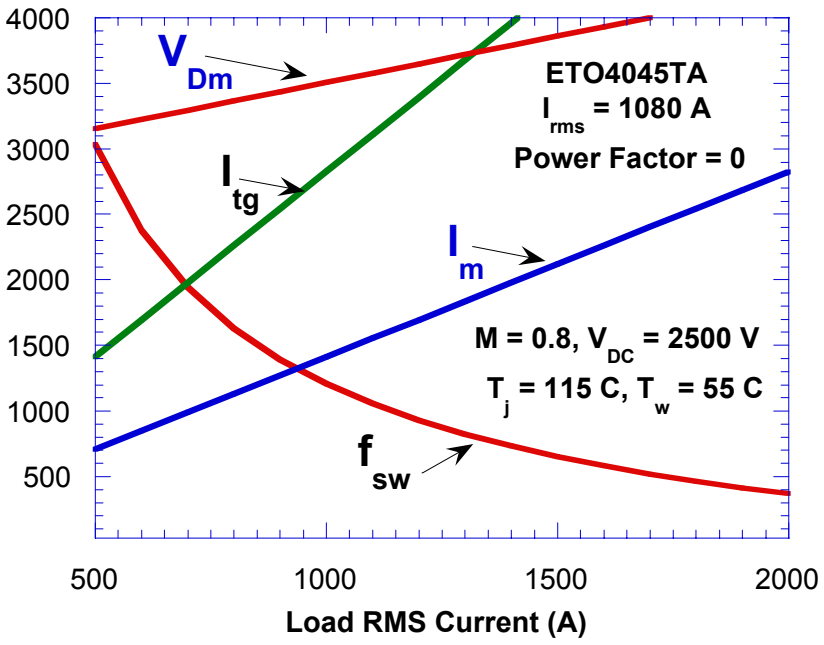



Fig. 6.11. Operation point design curve for the ETO4045TA in a three-level VSC based STATCOM.

For the three-level VSC based STATCOM, the output power rating is proportional to the modulation index M, DC-link voltage $V_{dc}$ and load RMS current $I_{rms}$, as displayed in Equation (6-14). For the given output power rating with fixed switching frequency and modulation index, the higher the DC-link voltage, the lower the output current and conduction loss, and thus the lower the total loss. In other words, if the total power loss for the ETO device is fixed, the higher the DC-link voltage, the higher the output power

rating as shown in Fig. 6.12. Therefore, from the standpoint of output power rating, the higher the DC-link voltage the better.

$$S = \frac{3}{\sqrt{2}} \cdot M \cdot V_{dc} \cdot I_{rms} \quad (6\text{-}14)$$

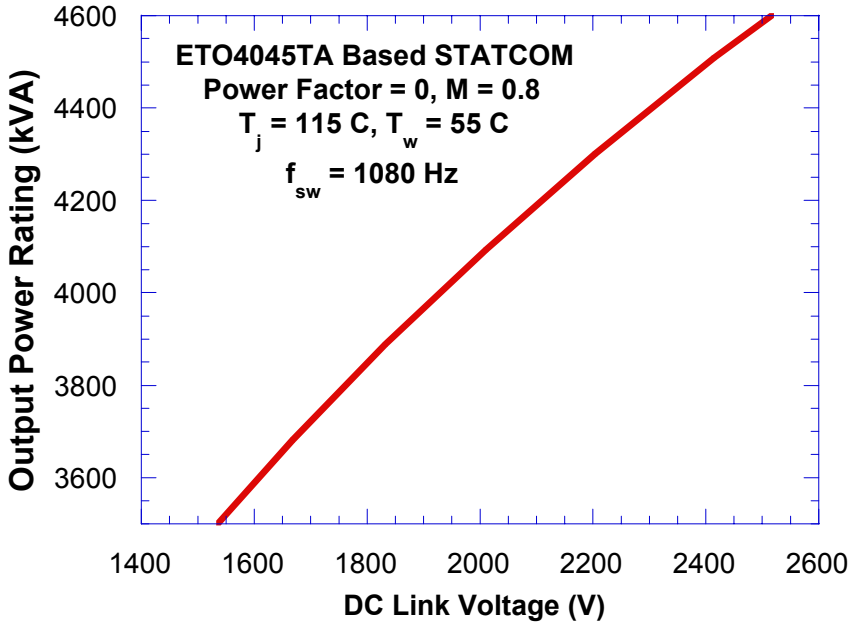



Fig. 6.12. Relationship between DC-link voltage $V_{dc}$ and output power rating.

In the cascaded multilevel VSC, the load current will flow through the DC-link capacitors in each HBBB as in the case of the single phase VSC. So the DC-link capacitors for each HBBB will have a voltage ripple with a frequency that is double the line frequency f, as shown in Fig. 6.13, where $I_a$ is phase a load current and $V_{dca}$ is phase a DC-link voltage. For the average DC-link voltage of $V_{dc}$, to limit the maximum capacitor voltage below the maximum DC-link voltage $V_{DC\_max}$, the required minimum DC-link capacitance $C_{dc\_min}$ can be calculated using Equation (6-15) [H6], where f is the line frequency, $f_s$ is the switching frequency, and $I_{rms}$ is the RMS load current.

$$C_{dc\_\min}(I_{rms}, V_{dc}, f_s) = \frac{I_{rms}}{\sqrt{2}\cdot\pi\cdot f\,(V_{dc\_\max} - V_{dc})} \cdot \frac{1}{2 - \frac{f}{f_s}} \quad \text{(6-15) [H6]}$$

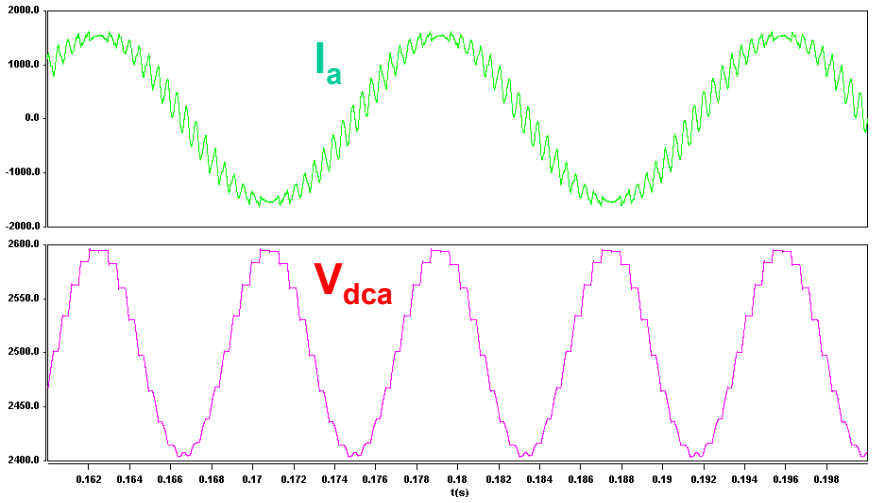



Fig. 6.13. Relationship between DC-link voltage ripple and output current.

Since the maximum DC-link voltage is dictated by the DC-link voltage rating of ETO device (2800 V for ETO4045TA), the higher the average DC-link voltage $V_{dc}$, the lower the DC-link voltage ripple and the higher the required DC-link capacitance, as shown in Fig. 6.14, where the load RMS current is 1000 A. When the average DC-link voltage is higher than 2500 V, the required minimum DC-link capacitance dramatically increases. A higher capacitance means higher cost. So from the standpoint of DC-link capacitance, a lower the DC-link voltage is better. Therefore, the DC-link voltage design is a trade-off between the output power rating and DC-link capacitance. When $I_{rms}$ = 1080 A, $V_{dc}$ = 2500 V, $V_{dc\text{-}max}$ = 2800 V, and $f_s$ = 1080 Hz, the required minimum DC-link capacitance is about 6.95 mF.

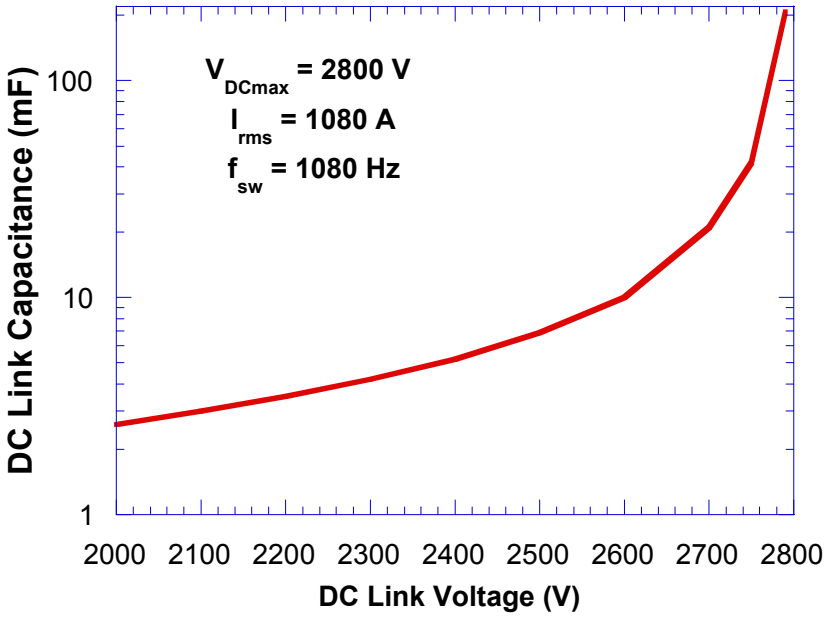



Fig. 6.14. Relationship between DC-link capacitance and average DC-link voltage.

For the given average DC-link voltage $V_{dc}$, the higher the modulation index M, the higher the output power rating, as indicated in Equation (6-14). The THD of the output voltage also decreases with the increase of the modulation index M. So higher M is preferred from the standpoint of harmonics and output power rating. On the other hand, the higher modulation index M will leave a smaller modulation index margin for the dynamic response. Furthermore, the selection range of coupling inductor L is also limited by modulation index M. So the design of modulation index M should consider the trade-off between the output power rating and dynamic response. In the three-level VSC based STATCOM, a modulation index M of 0.8 is a good choice.

Coupling inductor L serves as the first-order filter for injected current from the STATCOM. The higher the coupling inductor L, the lower the total harmonics for the injected current. On the other hand, a

higher coupling inductor L will cause higher loss and cost. Furthermore, the selection range of modulation index M is also limited by coupling inductor L. Considering the double overload capability of the STATCOM, when modulation index M is chosen to be 0.8, an impedance of 0.10 pu can be selected for coupling inductor $X_L$.

Based on the previous analysis, using the 4-kA/4.5-kV asymmetrical ETO as the main switch, the power stage parameters for the five-level VSC based STATCOM are as follows:

$V_{dc}$ = 2500 V; $I_{rms}$ = 1080 A; $C_{dc}$ = 7.65 mF (22% peak-to-peak DC-link voltage ripple); L = 0.43 mH; $T_j$ = 115 °C; $T_w$ = 55 °C; S = ±4.58 MVA.

Assuming that the system is balanced and has only a small ripple under normal operation conditions, the average model for the three-level VSC based STATCOM in rotating dq coordinates is shown in Fig. 6.15. For normal lagging var compensation, the operation conditions based on the dq model are as follows:

$V_{dc}$ = 2500 V; $I_d$ = 0; $I_q$ = 1871 A; $V_d$ = 2143 V; $V_q$ = 30.6 V; $D_d$ = 0.857; $D_q$ = 0.012.

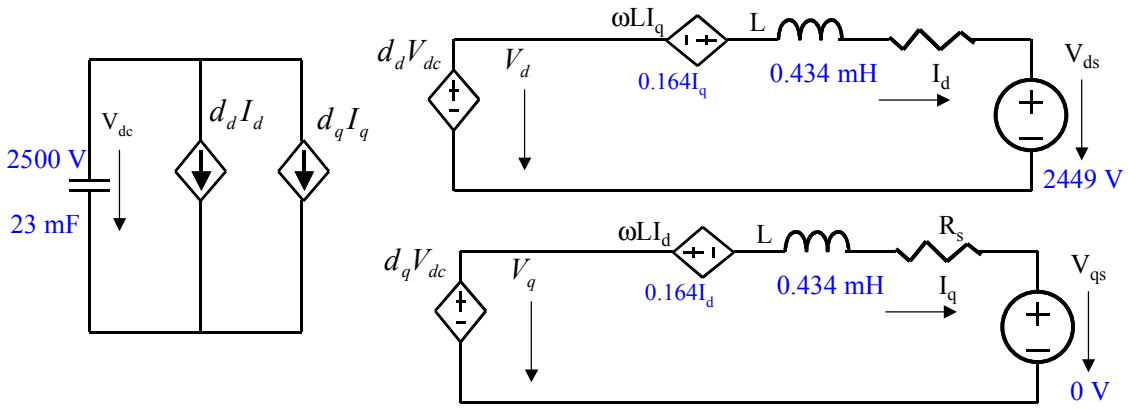



Fig. 6.15. Average dq model for the three-level VSC based STATCOM.

To achieve fast dynamic response in the current control loop and to maintain stable DC-link voltages, the d-channel current controller $H_{id}$, q-channel current controller $H_{iq}$ and DC-link voltage controller $H_{vdc}$ are required as shown in Fig. 6.16. Based on the dq model, the small-signal model can be obtained at the DC operation point. All controllers are then designed according to the requirement of dynamic response as well as the stability margin.

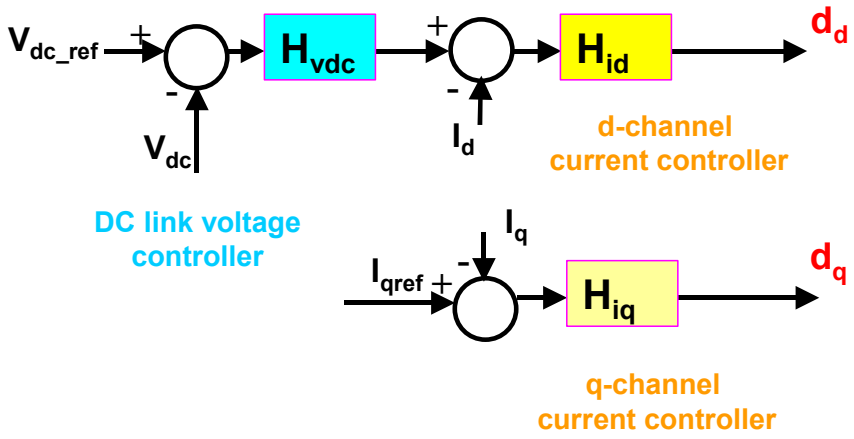



Fig. 6.16. Controller diagram of the three-level VSC based STATCOM.

For the dq model shown in Fig. 6.15, the VSC based STATCOM can be approximated as a second-order system with two passive components, since the DC-link capacitor is fairly large and can be considered as a voltage source for the inner current loop controller design. At the normal lagging var operation point, the simulated transfer function between q-channel current $I_q$ and q-channel duty cycle $d_q$ is shown in Fig. 6.17. It is obvious that the transfer function $I_q/d_q$ is a second-order system. After the resonant frequency (around 60 Hz), the system behaves like a first-order system, but with a much faster dropping phase due to the power stage switching delay.

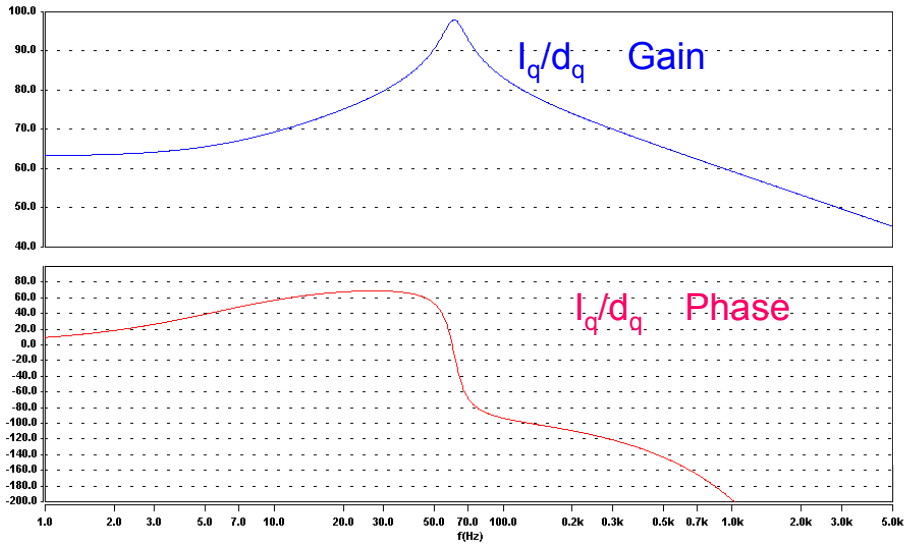



Fig. 6.17. Simulated transfer function of $I_q/d_q$ at the normal lagging var compensation condition for the three-level VSC based STATCOM.

Considering the trade-off between the control bandwidth and stability margin, the d-channel current controller $H_{id}$ and q-channel current controller $H_{iq}$ are designed as shown in Equations (6-16) and (6-17). With the designed controller, the q-channel current loop gain Tq is shown in Fig. 6.18, with a crossover frequency of 208 Hz, a phase margin of 57 ° and a gain margin of 12.6 dB.

$$H_{id}(s) = 0.06 \cdot \frac{1}{s} \cdot (1 + \frac{s}{295}) \quad (6\text{-}16)$$

$$H_{iq}(s) = 0.06 \cdot \frac{1}{s} \cdot (1 + \frac{s}{295}) \quad (6\text{-}17)$$

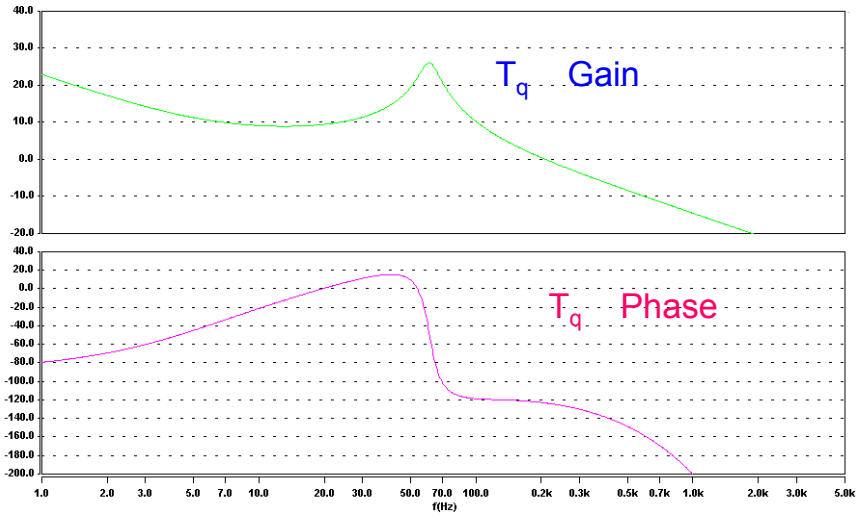



Fig. 6.18. Q-channel current control loop gain Tq for three-level VSC based STATCOM.

The DC-link voltage controller $H_{vdc}$ will control the DC-link capacitor charging process and will maintain a constant DC source voltage during the normal operation. Considering the trade-off between the DC-link capacitor charging speed and the DC voltage spike during the transient, the DC-link voltage controller is designed as described in Equation (6-18). With the designed controller $H_{vdc}$, the DC-link voltage loop gain $T_{vdc}$ has a crossover frequency of 30 Hz, a phase margin of 75° and a gain margin of 15 dB.

$$H_{vdc}(s) = 500 \cdot \frac{1}{s} \cdot (1 + \frac{s}{50}) \quad \text{(6-18)}$$

To reduce the harmonics and output dv/dt, the three-level SPWM scheme [A6] is used to switch each HBBB in the three-level VSC based STATCOM as shown in Fig. 6.19. With more HBBBs cascaded in each phase, the interleaved multilevel SPWM scheme can be used to dramatically reduce the harmonics.

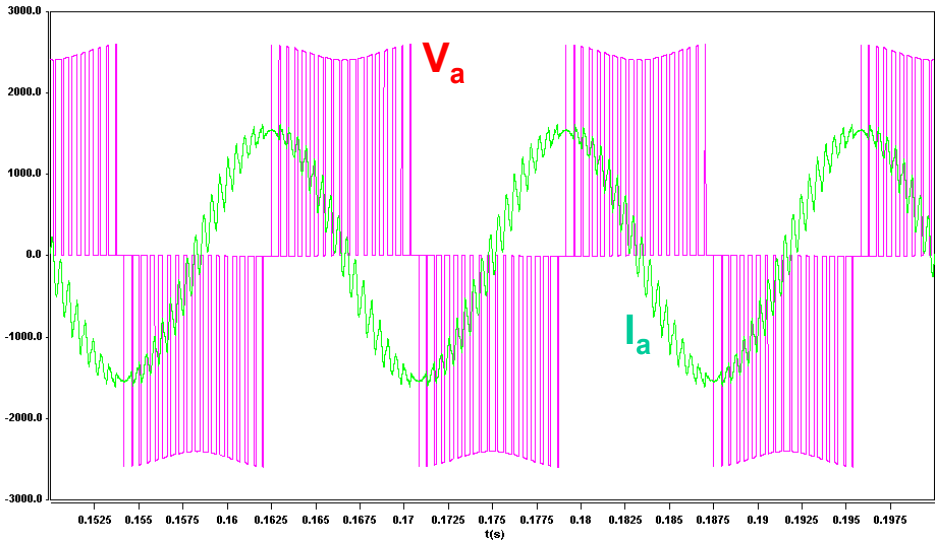



Fig. 6.19. Phase **a** output voltage and current for the three-level VSC based STATCOM.

## 6.3. STATCOM Design Based on Parallel-Cell Five-Level CSC

For comparison purposes, the same devices used in three-level VSC based STATCOM (12 ETOs and diodes) are used in the five-level CSC based STATCOM. Due to the reverse-blocking capability requirement in the CSC, the asymmetrical ETO in series with a diode is used as the main switch, as shown in Fig. 4.16 from Chapter 4. Based on the design guidelines described in Section 4.3 of chapter 4, the power stage parameters for five-level CSC based STATCOM (see Fig. Fig. 6.20) are as following:

$V_m$ = 2800 V; $I_{dc}$ = 1100 A; $C_f$ = 500 μF; L = 0.5 mH; $L_{dc}$ = 30 mH (4% DC-link current ripple); $f_s$ = 1080 Hz; $T_j$ = 115 °C; $T_w$ = 55 °C, and S = -4.12--+3.39 MVA.

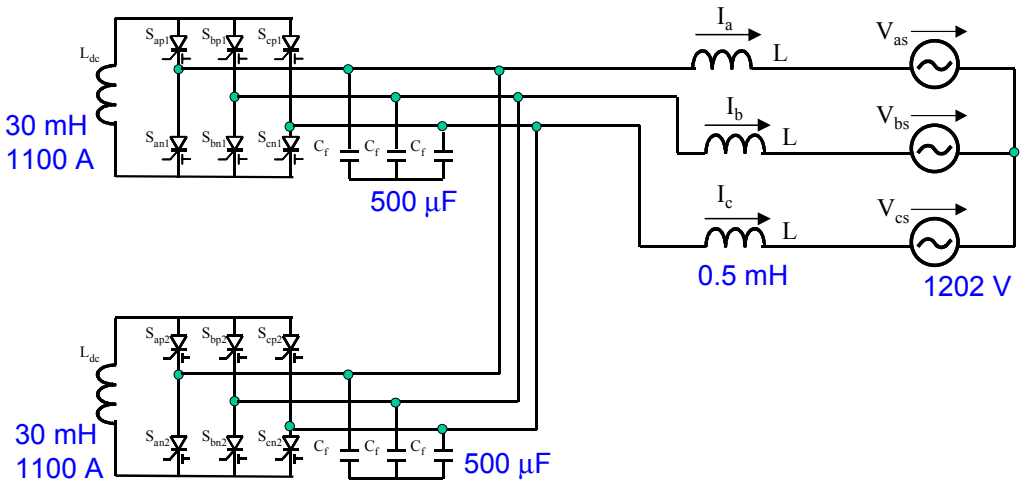



Fig. 6.20. Five-level CSC based STATCOM with designed parameters.

Fig. 6.21 shows the dq model for the five-level CSC based STATCOM with designed parameters. Under normal leading var compensation, the operation parameters are as follows:

$I_{dc}$ = 2200 A; $I_d$ = 0; $I_q$ = 2000 A; $V_d$ = 1093 V; $V_q$ = 0 V; $D_d$ = 0; $D_q$ = 1.102.

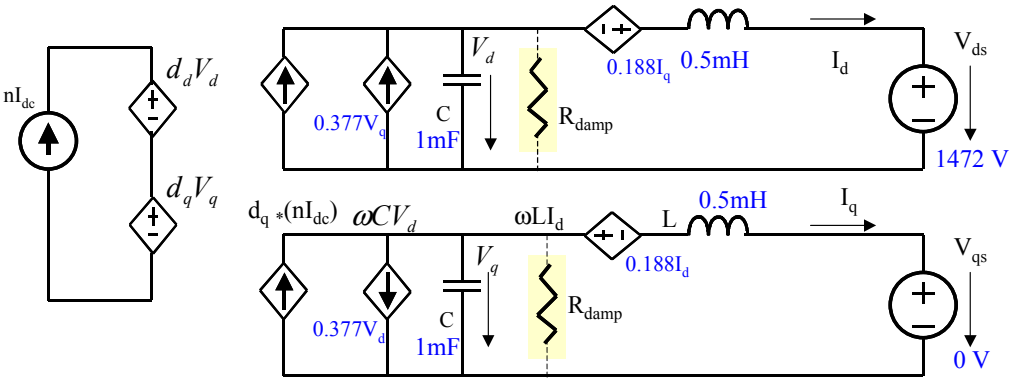



Fig. 6.21. The dq model for five-level CSC based STATCOM with designed parameters.

Based on the dq model in Fig. 6.21, following the design guidelines described in Section 5.4 of Chapter 5, the d-channel current controller $H_{id}$, q-channel current controller $H_{iq}$, and DC-link current controller $H_{idc}$ are designed as shown in Equations (6-19) to (6-21). With the designed controller, the

crossover frequency for q-channel current loop gain $T_q$ is about 58.5 Hz with a phase margin of 58 ° and a gain margin of 6.3 dB. For DC-link current loop gain, the crossover frequency is about 14 Hz with a phase margin of 77 ° and a gain margin of 13.6 dB.

$$H_{id}(s) = 0.32 \cdot \frac{1}{s} \cdot (1 + \frac{s}{1800}) \quad (6\text{-}19)$$

$$H_{iq}(s) = 0.32 \cdot \frac{1}{s} \cdot (1 + \frac{s}{1800}) \quad (6\text{-}20)$$

$$H_{idc}(s) = -2 \quad (6\text{-}21)$$

To reduce the harmonics and better utilize the DC-link current, the symmetrical SVM scheme is used for the switching modulation control of each six-switch CSC cell. The interleaved symmetrical SVM scheme is used for the five-level CSC based STATCOM, with a time delay of half of the switching cycle in the clock signal between the two six-switch CSC cells. The switching ripples of two CSC cells are interleaved and the level of harmonics is reduced, as shown in Fig. 6.22, where $I_{ao1}$ is the phase a output current of CSC cell 1 before filtering; $I_{ao2}$ is the phase a output current of CSC cell 2 before filtering; $I_{ao}$ is the total phase a output current before filtering and $I_a$ is the total phase a output current after filtering.

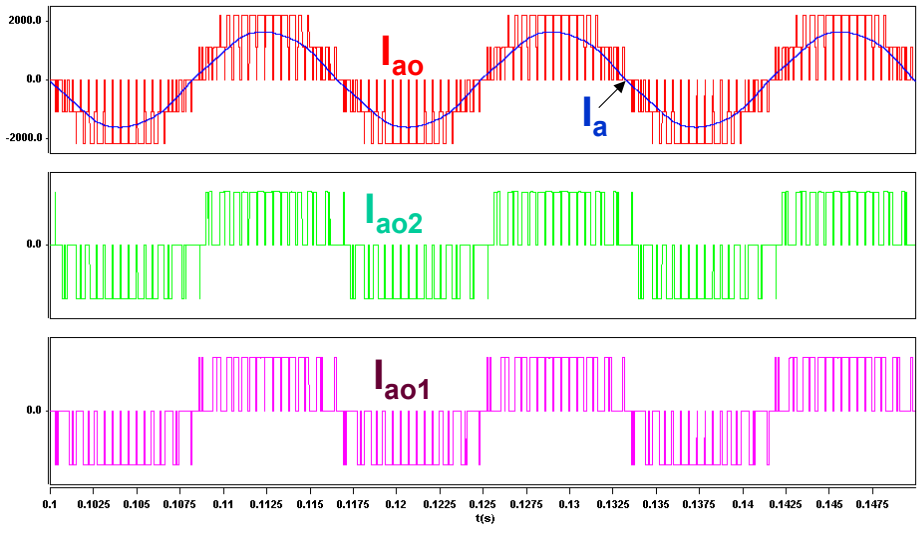



Fig. 6.22. Simulated output current of the five-level CSC based STATCOM.

## 6.4. Performance Comparison

### 6.4.1. Power Rating

Using the same power semiconductor devices, the three-level VSC based STATCOM has a power rating of 4.58 MVA that is mainly thermally limited. For lagging var compensation, the five-level CSC based STATCOM has a power rating of +3.39 MVA, which is limited by the modulation index and DC-link current. For leading var compensation, the five-level CSC based STATCOM has a power rating of –4.12 MVA, which is limited by the DC-link voltage rating for the ETO device as well as the DC-link current level. Since the asymmetrical 4-kA/4.5-kV ETO4045TA is optimized for VSC applications with high current rating and voltage ratings, the output lagging var rating of the five-level VSC based STATCOM is 20% higher than that of the five-level CSC based STATCOM. For the CSC topology, the power semiconductor device with high voltage rating and relatively lower current rating is preferred.

### 6.4.2. Device Losses

For the VSC, the conduction loss of the ETO device is mainly dictated by the load current, as described in Equation (6-12). For the CSC, the conduction loss is mainly determined by the DC-link current instead of by the load current. Compared with the conduction loss of about 0.4 kW for one ETO device in the three-level VSC based STATCOM under normal operation mode, the ETO device in the five-level CSC based SATATCOM always has a conduction loss of about 0.6 kW in spite of load conditions.

For the VSC, the power semiconductor device has the constant voltage stress of $V_{dc}$ (about 2500 V) and the average turn-off switching loss for one ETO device under normal operation mode ($I_{rms}$ = 1080 A, $V_{dc}$ = 2500 V, and $f_s$ = 1080 Hz) is about 2.15 kW. For the CSC, the power semiconductor device has a

constant current stress of $I_{dc}$ (about 1100A) and the average forced turn-off switching loss for one ETO device is about 1.95 kW under the maximum leading var operation condition ($V_m$ = 2800 V, $I_{dc}$ = 1100 A, and $f_s$ = 1080 Hz).

For the same total loss, the CSC based STATCOM has a lower lagging var rating due to its higher circulating energy, which is caused by the LC filter and higher conduction loss.

### 6.4.3. Start-Up Process

During start-up, the three-level VSC based STATCOM behaves like a boost rectifier. The minimum DC output voltage applied to the DC-link capacitor in each phase can be calculated using Equation (6-22), where $V_m$ is the peak value of the line-to-line voltage at the point of common coupling to the power system. Since the minimum output voltage for boost rectifier is higher than zero, the DC-link capacitor should be pre-charged to a proper voltage level in order to avoid a huge inrush current when connecting to the AC power system. The separate charger or pre-charge circuit with pre-charge switching in series with the current limiting resistor can be used to charge the DC-link capacitors.

$$V_{dc\_\min} = \frac{V_m}{2} \quad (6\text{-}22)$$

On the other hand, the five-level CSC based STATCOM behaves like a Buck rectifier during the start-up process. The controllable output voltage for a buck converter is from zero to $V_{dc\text{-}max}$, as described in Equation (6-23). So, through proper control, the DC-link inductor can be easily charged to the setting current level at the required slew rate, as shown in Fig. 6.23 for the five-level CSC based STATCOM. No external pre-charging circuit is needed. Similarly, DC-link inductors in the multilevel CSC based STATCOM can be totally discharged when proper controls are used during the shut-down process, but the DC-link capacitors in the cascaded multilevel CSC can only be totally discharged when an external discharging circuit is used.

$$V_{dc\_\max} = \frac{\sqrt{3}}{2} \cdot V_m \quad (6\text{-}23)$$

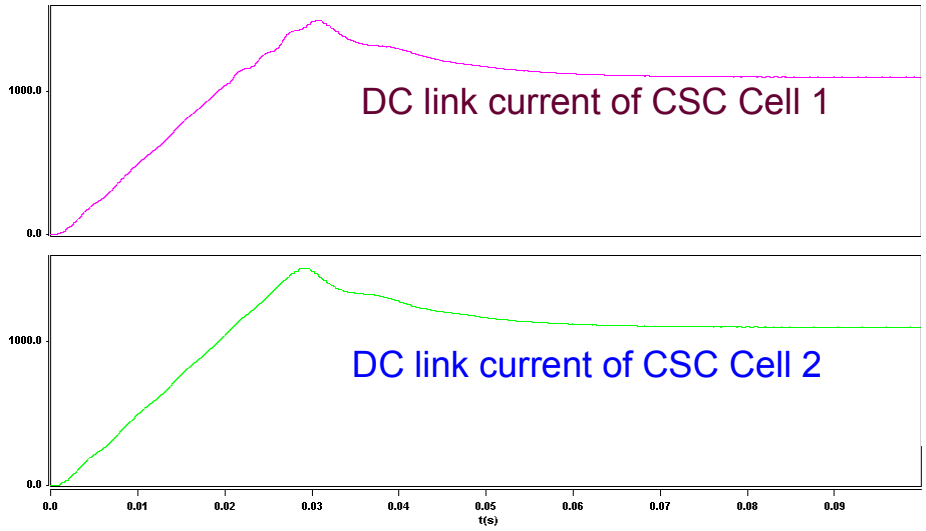



Fig. 6.23. Simulated charging process of the DC-link inductors in the five-level CSC based STATCOM.

### 6.4.4. Harmonics

During normal operation, the five-level CSC based STATCOM injects less harmonics (about 2.5% current THD at normal lagging var compensation) due to the secnd-order filter formed by filter capacitor $C_f$ and coupling inductor L (see Fig. 6.20). During standby mode and without any reactive var compensation, the CSC based STATCOM also injects very low levels of harmonic currents into the power system, as shown in Fig. 6.24, where $I_a$ is the injected phase a current and $V_{as}$ is the phase a voltage at the point of common coupling to power systems.

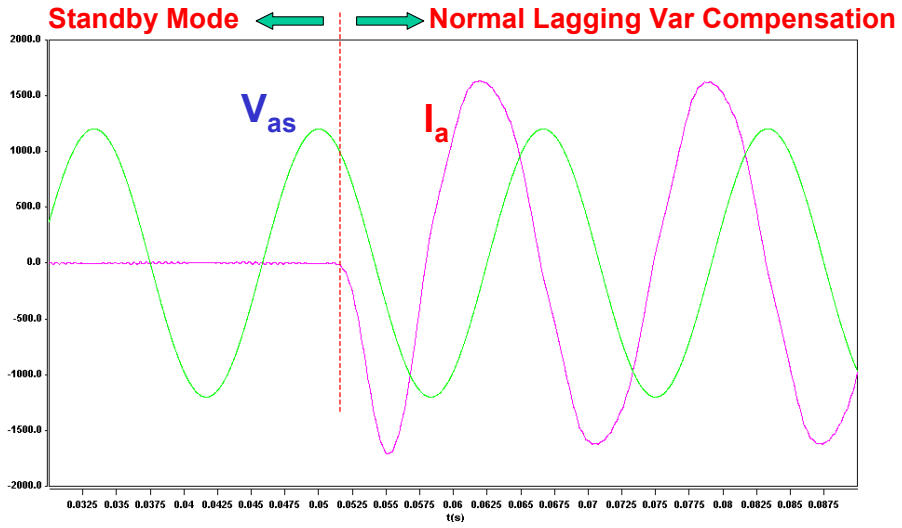



Fig. 6.24. Simulated compensation current of the five-level CSC based STATCOM.

In contrast, during normal operation, the three-level VSC based STATCOM injects more harmonics (about 13.8% current THD at normal lagging var compensation) due to the limited attenuation capability of the first-order filter formed by coupling inductor L. During standby mode and without the fundamental reactive current for compensation, the VSC based STATCOM still injects relatively higher levels of harmonic current into the power system, as shown in Fig. 6.25.

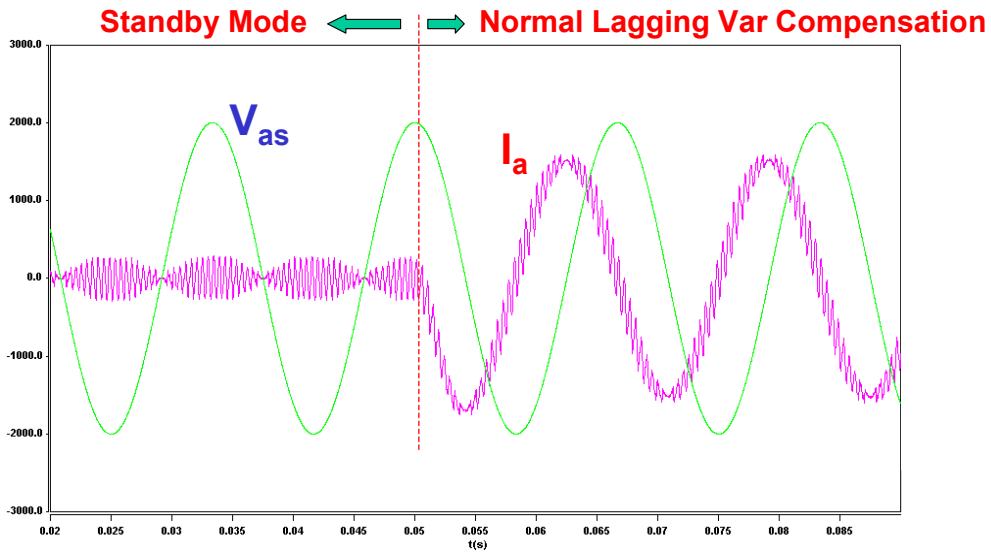



Fig. 6.25. Simulated compensation current of the five-level VSC based STATCOM.

In general, the VSC based STATCOM will inject more harmonic current into the power system. To reduce the current harmonics, either higher output voltage levels with more HBBBs in each phase or additional output filters are needed for the VSC based STATCOM.

### 6.4.5. Dynamic Response

The VSC based STATCOM has a simple power stage with two passive components in the dq model, as shown in Fig. 6.17. The control bandwidth for the inner current loop is mainly limited by the phase delay caused by the limited power stage switching frequency. Usually, for each HBBB, and using a three-level SPWM scheme for switching modulation, the equivalent switching frequency in the output voltage is about double the switching frequency of an individual power semiconductor device. The control bandwidth for the current loop can be pushed to about 10% of the equivalent switching frequency. For the previously designed three-level VSC with a switching frequency of about 1080 Hz, the control bandwidth for the inner current loop can be pushed to about 200 Hz and the rising time for its step response is about 1.9 ms, as shown in Fig. 6.26.

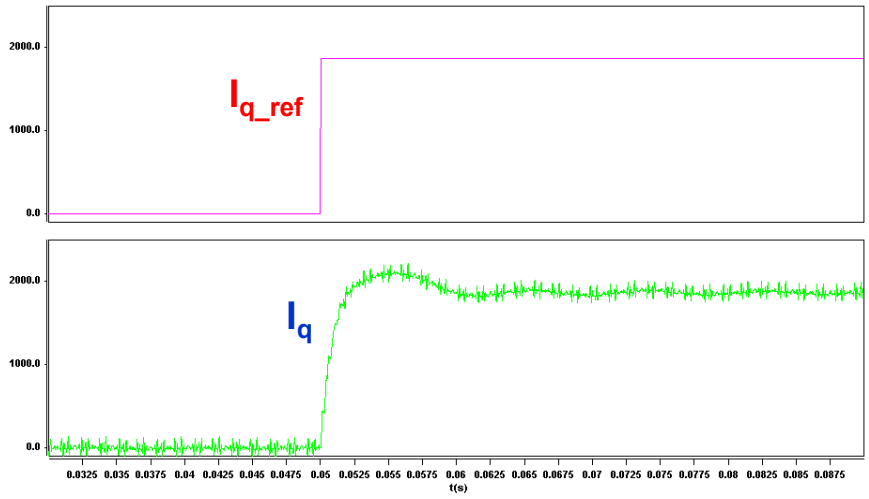



Fig. 6.26. Simulated step response for the three-level VSC based STATCOM.

Compared to the VSC based STATCOM, the one based on CSC has a complex power stage with four passive components, as shown in Section 5.4 of Chapter 5. The control bandwidth for the inner current loop is limited by the phase delay that is caused by the limited power stage switching frequency as well as the right half-plan zero. The control bandwidth is usually below the resonant frequency of the output filter and is lower than that of the VSC based STATCOM. Therefore, compared to the VSC based STATCOM, the CSC version usually has a slower dynamic response and requires more complicated control. Using proper switching modulation scheme for the six-switch CSC cell, the output current harmonics as well as the output filter can be reduced. The reduced output filter inductor will improve the power rating as well as the control bandwidth for the inner current loop, resulting in a fast dynamic response speed that is comparable to the VSC based STATCOM.

For the previously designed five-level CSC based STATCOM, the control bandwidth for the inner current loop is about 58 Hz and the rising time for its step response is about 3.9 ms, as shown in Fig. 6.27.

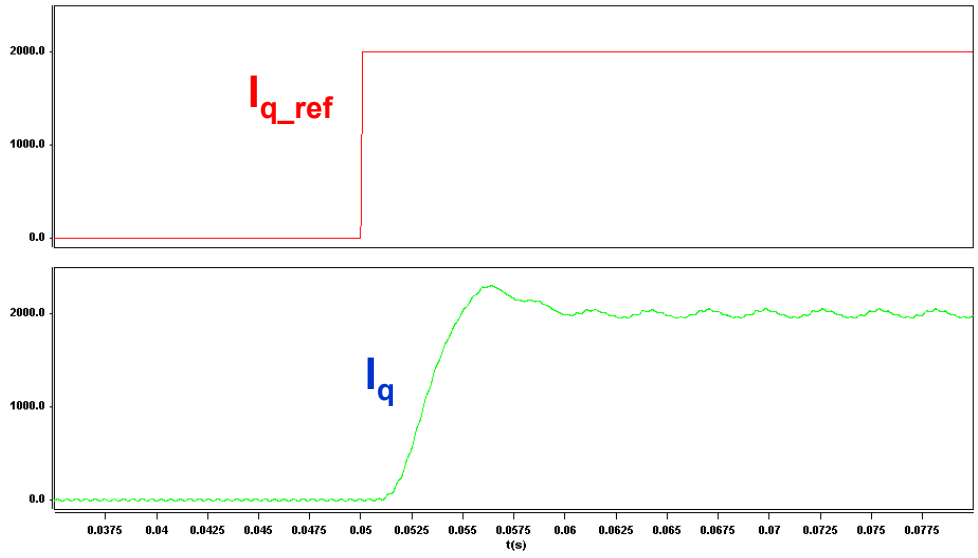



Fig. 6.27. Simulated step response for the five-level CSC based STATCOM.

### 6.4.6. Power Rating Expansion

For the cascaded multilevel VSC based STATCOM, with more HBBBs cascaded in each phase, the output power rating, output voltage level as well as equivalent switching frequency will linearly increases while the output current rating remains the same. With more HBBBs in each phase, the output voltage for the cascaded multilevel VSC based STATCOM may increase to a level close to the distribution voltage level of the power system (about 13.8 kV). Therefore, the transformerless design for the cascade multilevel VSC based STATCOM is also possible. This is highly preferable for STATCOM application in which high power ratings, fast dynamic responses and low current harmonics are needed.

With more HBBBs in each phase for the cascaded multilevel VSC based STATCOM, the DC-link voltage balance among all the HBBBs becomes a most challenging problem. System protection and reliability are also significant concerns and more research is needed in these areas.

For the parallel-cell multilevel CSC based STATCOM, with more six-switch CSC cells in parallel, the output current and power rating will linearly increases while the output voltage rating remains the same. Although the level of injected current harmonics can be very low, the coupling transformer that is needed to boost the output voltage cannot be eliminated. With higher current rating, the conduction loss increases. Therefore, the parallel-cell multilevel CSC topology is more suitable to the applications that require high current, low voltage and low harmonics, such as the static synchronous series compensator (SSSC) [14-15].

Using more six-switch CSC cells in parallel for the parallel-cell multilevel CSC based STATCOM, the DC-link current balance among all the CSC cells is not a great concern since each CSC cell has its own

DC-link current control loop. Since each CSC cell can work separately, the system protection and control for the parallel-cell multilevel CSC with more cells is similar to those of a single CSC cell. This is a huge benefit of the parallel-cell multilevel CSC since the modular structure for both the power stage and control can be implemented with less effort. It is also possible to achieve active filtering by operating one CSC cell at a lower power rating and high switching frequency, while other CSC cells operate at low switching frequencies and high power ratings for reactive power compensation.

## 6.5. Conclusion

This chapter first explains the operation principle of the STATCOM. Then the guidelines for the power stage design of the cascaded multilevel VSC based STATCOM and parallel-cell multilevel CSC based STATCOM are investigated. Finally the performances of the two versions are evaluated and compared.

The STATCOM is a key FACTS device that can quickly provide reactive power by circulating energy among the phases of the AC system. Two power circuit topologies can be used in a STATCOM: cascaded the multilevel VSC and the parallel-cell multilevel CSC. Both topologies can produce high reactive power with fast dynamic speed and low harmonics.

For the cascaded multilevel VSC based STATCOM, the 4-kA/4.5-kV asymmetrical ETO device (ETO4045TA) is used as the main switch due to its high power rating, fast switching speed, easy control and low conduction loss.

For each HBBB, the DC-link voltage design is a trade-off between DC-link capacitance and output power rating. The selection of modulation index is a trade-off between the output power rating and the dynamic response. Similarly, the coupling inductor design is a trade-off between current harmonics and output power rating. Finally, the switching frequency is a trade-off between dynamic response and output power rating.

Based on these design guidelines, for the three-level VSC based STATCOM with one HBBB in each phase, using 12 4-kA/4.5-kV ETO devices (ETO4045TA), an output power rating of ±4.58 MVA can be achieved with $V_{dc}$ = 2500 V, $f_s$ = 1080 Hz, M = 0.9, $T_j$ = 115 °C, and $T_w$ = 55 °C.

For comparison purposes, the asymmetrical ETO device (ETO 4045TA) in series with a fast recovery diode is used as the main switch in the multilevel CSC based STATCOM. With the same number of power semiconductor devices, the five-level CSC based STATCOM can achieve a leading var rating of -4.15 MVA and a lagging var rating of +3.39 MVA with $I_{dc}$ = 1100 A, $f_s$ = 1080 Hz, $T_j$ = 115 °C, $T_w$ = 55 °C, $C_f$ = 500 μF; and L = 0.5 mH.

Compared with the five-level VSC based STATCOM, the five-level CSC based STATCOM has a similar leading var rating and a lagging var rating that is about 20% lower due to the high conduction loss and greater amount of circulating energy in the CSC topology.

During start-up and shutdown, the DC-link inductors in the multilevel CSC based STATCOM can be easily charged or discharged to a designed level through proper control. In contrast, the DC-link capacitors in the multilevel VSC based STATCOM must be pre-charged to avoid huge inrush current during start-up. An external discharging circuit is also needed for the VSC based STATCOM to totally discharge its DC-link capacitors during shutdown.

With the second-order filter formed by filter capacitor $C_f$ and coupling inductor L, the multilevel CSC based STATCOM injects less harmonic current during both the normal operation mode and the standby

mode. On the other hand, the multilevel VSC based STATCOM injects higher harmonic current during both modes due to its first-order filter formed by coupling inductor L. An additional filter is needed to attenuate the current harmonics.

With a relatively simple power stage, for the inner current control loop, the VSC based STATCOM has a higher control bandwidth limited only by the phase delay that is caused by its limited switching frequency. However, the CSC based STATCOM has a relatively lower control bandwidth limited by the phase delay that exists due to both the limitation of both the switching frequency and the output filter. Therefore, as compared with the CSC based STATCOM, the VSC based STATCOM has a faster dynamic response speed.

With more HBBBs cascaded in each phase, the output voltage and power rating for the cascaded multilevel VSC based STATCOM will linearly increase. Similarly, with more six-switch CSC cells in parallel, the output current and power rating for the parallel-cell multilevel CSC based STATCOM will also linearly increase. Both topologies are good candidates for high-power, reactive power compensation devices.

The cascaded multilevel VSC is preferred in applications that require high voltage, high power, low harmonics and fast dynamic response speed, such as STATCOMs. The parallel-cell multilevel CSC is more suited to applications that require high current, high power, low harmonics and fast dynamic response speed, such as SSSCs [J1, J6].

# Chapter 7. Conclusions and Future Work

## 7.1. Conclusions

This dissertation investigates the following topics related to the advanced power semiconductor device and topology for the high-power CSC:

- An Advanced Symmetrical Semiconductor Device-The Symmetrical ETO

An advanced symmetrical device, the symmetrical ETO, is proposed and its operation principle is analyzed. Its on-state characteristics, forced turn-on characteristics, forced turn-off characteristics as well as the load-commutated turn-off characteristics for symmetrical ETO are evaluated. The results show that the symmetrical ETO has a low on-state voltage drop that is mainly dictated by its symmetrical GTO device. The symmetrical ETO has the ability to achieve snubberless forced turn-off due to its unity-gain turn-off. The forced turn-on performance is improved by its tightly-integrated gate driver. However, the reverse-recovery performance of the symmetrical ETO is mainly dictated by the symmetrical GTO part and needs to be improved. Although the load-commuted turn-off loss is higher than that of a commercial diode, the symmetrical ETO is still suitable for use in high-power circuits that require reverse voltage-blocking capability, due to its lower conduction loss, fewer components and the simplicity of its circuit without a dv/dt snubber.

- Investigation of Snubberless Turn-On of the Emitter Turn-Off Thyristor

This work analyzes and demonstrates the ETO's FBSOA, which mandates that the snubberless turn-on capability exist in the ETO. Using self-driven MOSFETs as the gate switch, the ETO has excellent

current saturation capability (and hence FBSOA) due to the negative feedback provided by emitter switch $Q_E$.

For a large-area ETO, however, the unbalanced negative feedback will intensify the current's non-uniform distribution, thus resulting in current filamentation under high voltage and current saturation conditions. So large-area ETOs are expected to have poor FBSOA. Therefore, the newer generation of ETO is needed to achieve better FBSOA in a large-area device.

Another possible way to turn on the ETO without a snubber is proposed in this dissertation. This approach is based on the fact that current crowding problem can be avoided if the device cell has the dynamic current-limiting capability, which can be implemented by driving the GTO cell into the transistor mode through the use of a higher gate-current pulse with higher slew rate. For the ETO device, to achieve transistor-mode snubberless turn-on, two conditions must be meet: the built-in NPN part must provide enough load current under a given gate-drive condition; and the current rising time for the built-in NPN part must be less than thyristor latch-up delay time. The two conditions are hard to meet due to the following: the lower NPN current gain due to due to the wide p-base; and the fact that collector-current rising time is longer than the thyristor latch-up time due to the lower collector-current rising rate, even under very high gate-current conditions. So the current generation of ETO cannot achieve snubberless turn-on capability.

Short of a snubberless turn-on, the ETO's turn-on can be improved using two methods: using a turn-on di/dt snubber; and using a high gate current with high slew rate. With a proper di/dt snubber and integrated gate driver, transistor-mode turn-on can be achieved, and the ETO can be turned on without the current-crowding problem. Correspondingly, the critical anode-current rise rate is improved, and the minimum turn-on time is reduced. These advantages, together with the snubberless turn-off capability and

voltage control, make the ETO a very promising device for high-power, high-frequency power electronics systems.

- Power Stage Design of ETO Based CSC

Based on the analysis of the commutation process, the switching performance of the symmetrical ETO in a CSC is analyzed, and the snubber circuit design is explored in this work. To improve the load-commutated turn-off performance of a symmetrical ETO, a novel gate-control scheme involving a gate delay time for the on-coming device is proposed and evaluated. Test results show that the delay time has a limited effect on the reverse-recovery performance of the off-going device. To further improve the reverse-recovery performance, symmetrical GTO device optimization or other soft-switching techniques are needed.

The power stage design for the ETO based CSC is studied. For a given switching frequency, the DC-link current and the maximum output power rating are mainly thermally limited due to the high conduction loss in a CSC. To achieve a high power rating, a device with a high voltage rating is preferred.

- A Novel Multilevel CSC—The Parallel-Cell Multilevel CSC

A novel multilevel CSC, named the parallel-cell multilevel CSC, is proposed. The operation principle, modeling, control and switching modulation scheme for this CSC are analyzed and verified through simulation. Based on the six-switch CSC cell, the parallel-cell multilevel CSC has the advantages of high power rating, low harmonics, fast dynamic response and modular design. Therefore, it is very suitable for high power applications.

A novel SVM scheme for the parallel-cell multilevel CSC is proposed in this work. Based on the selected coordinates of three phase currents (Ia, Ib and Ic), for a given reference current vector, the nearest

three current vectors and corresponding duty cycles can be easily derived. Then, the switching signal for each cell can be created taking into consideration of the DC-link current balancing, load balancing, lower switching loss and lower harmonics.

- Comparison of Multilevel CSC and VSC in STATCOM Applications

The design guidelines for the cascaded multilevel VSC-based STATCOM and parallel-cell multilevel CSC-based STATCOM are explored.

In STATCOM applications, the performance of the parallel-cell multilevel CSC is compared with the stat-of-the-art multilevel VSC topology-the cascaded multilevel VSC. Compared with the cascaded multilevel VSC-based STATCOM, and using the same power semiconductor devices, the parallel-cell multilevel CSC-based STATCOM has lower harmonics, an easier start-up process, a lower power rating and a comparable dynamic response speed.

### 7.2. Future Work

(1) To achieve snubberless turn-on over large areas, new generations of ETOs, formed by paralleling many smaller ETOs with separate gate switches and emitter switches, should be developed.

(2) To improve the load-commutated turn-off performance, the symmetrical GTO, optimized for performance in terms of both forced turn-off and load-commutated turn-off, should be used to develop a better symmetrical ETO.

(3) Based on the new ETO with improved reverse-recovery performance, the parallel-cell multilevel CSC prototype can be developed for utility and large drive applications.

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# Vita

The author, Zhenxue Xu, was born in Nei Mongol province, P. R. China in 1968. He received his B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1991 and 1996, respectively.

From 1991 to 1993, he was an electrical engineer with Power Company, Port of Qinghuangdao, Hebei Province. In 1998, he joined the Virginia Power Electronics Center (VPEC)- now the Center for Power Electronics Systems (CPES)- as a research assistant. He has been involved in several projects funded by TVA (Tennessee Valley Authority), Sandia National Laboratories and the Department of Energy (DOE). His research interests include high-power semiconductor devices, high-power conversion, modeling and control of power converters for utility applications.

He was the co-chair of the 2002 CPES Annual Seminar and National Science Foundation (NSF) site visit. He also served as the president of the IEEE Power Electronics Society Student Branch at Virginia Tech, and as a Student Council member of CPES.