Chapter 4. UMD with SRM-Based VSD System

4.1 Introduction

Increasing the use of VSDs in industries and homes has brought to the forefront the important issue of reliability. Reliability is a function of the drive topology, motor, converter components, control strategy and the availability of input power. The reliability of the VSD system is augmented by choosing optimal subsystems that would preclude higher reliability if the input power is not available. An Uninterruptible Power Supply (UPS) is not guaranteed by the utility, because it has become customary in some applications to resort to UPS systems in tandem with the utility power supply. The UPS connects the VSD system to alternate sources of energy such as batteries, fuel cells, internal combustion engine (ICE) generator systems, solar arrays and/or a combination of them, when the utility power becomes unavailable. UPSs [65] are expensive and complex designed to substitute the utility power source at a constant frequency. Constant frequency is ideal for constant speed drives, but not necessarily the optimal choice for VSD applications. VSD systems inherently require variable voltage/current and variable frequency in the case of induction and synchronous motor drives. In the case of chopper controlled DCM and SRM drives, the requirement is only a dc source, as opposed to an ac source. It becomes apparent that the inverter stage in the UPS is not required for VSD applications. This fact is of enormous consequence as it becomes obvious that for uninterruptible motor drives (UMDs) [64], it is not necessary to connect the UPS to the input power source, but integrate it into the drive system.

To maintain uninterrupted operation of a VSD during utility power failure, it is customary to install a UPS. This may be operated on- or off-line to provide a continuous power supply. This chapter considers topologies which incorporate the UPS feature into the VSD system itself, eliminating the need for a separate UPS. This results in enormous savings in cost during the process. This topic is yet to be explored, and it offers a scope for innovation in power topology of the VSD system while offering a reliable VSD system. This results in cost savings to process industries in terms of saved process output, short downtime, reduced labor costs. In the case of commercial applications, such as freezer and refrigerator drives, it results in efficiency enhancement, energy savings, and no food wastage resulting from long power outages.

Uninterrupted operation of VSDs is of interest in many applications such as textiles, paper, critical applications in semiconductor, medical applications, freezer/refrigerator drives, essential defense applications, garage doors, and sump pump motor drives. In home applications, VSDs are likely to enter the market due to high efficiency and energy-saving aspects.

The concept of an UMD without a stand-alone UPS and key topologies for the implementation of a UMD are explored in this study. The concept of UMD is illustrated with a SRM-based VSD system intended for appliance use. The experimental efficiency studies, along with the VA ratings of the UMD compared to conventional VSD systems are derived to allow comparison of the cost involved in the UMD implementation.

This chapter is organized as follows. Section 4.2 contains the topologies for the UMD. A case study of an UMD with a SRM drive is introduced in Section 4.3. The analysis of the proposed UMD system and derivation of loss model are explained in this section. Experimental set-up for the study of key variables is given in Section 4.4. Experimental results and discussions are introduced in Section 4.4. Conclusions are summarized in Section 4.5.

4.2 UMD Topologies

4.2.1 UMD for Dc Link-Based VSD System

UMDs are derived based on the type of motor drive. Consider the classification based on the number of input phases of the utility supply, i.e., single- and three-phase supplies. In the single-phase fixed-speed drive case, the uninterruptibility is provided by a stand-alone UPS only. This includes VSD systems with a SCR/TRIAC based single-phase IM. All other cases use a dc link to provide variable voltage/current and/or variable frequency. Note that drives utilizing a dc link encompass a large number of drive systems including IM, synchronous with permanent magnets or wound rotors, SRM and chopper-fed DCM drive systems.

The conventional UPS connected motor drive is shown in Figure 4.1. It contains two sets of static bypass switches to bring in either the utility power supply or the UPS system supply to the drive system. This is an off-line UPS-based system, and there will be a transfer time involved in switching between the utility power supply and the UPS system. The on-line system is in

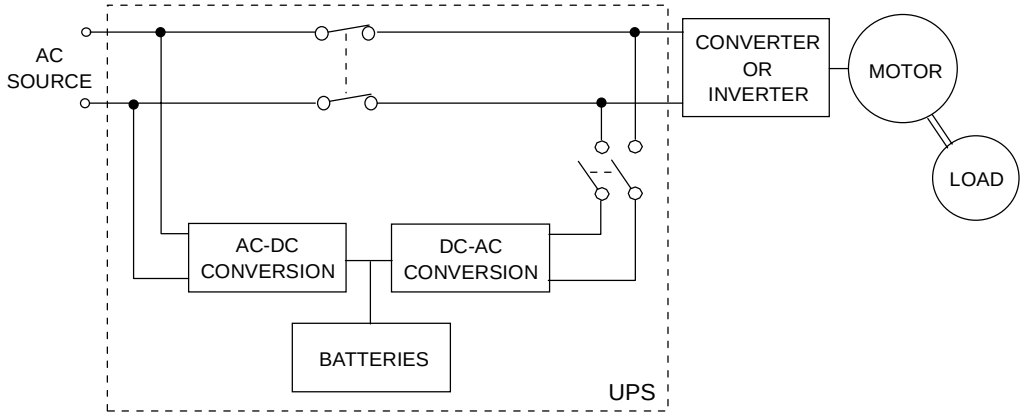


Figure 4.1 The conventional UPS with VSD.

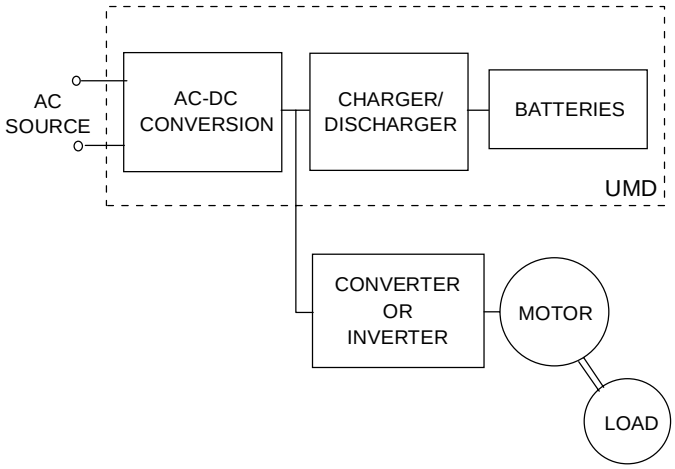


Figure 4.2 The proposed UMD system for VSD.

cascade with the utility all the time and the output of the UPS system supplies the drive system. The efficiency of such a system is less than that of the off-line based system, but it has the distinct advantage of zero transfer time when the utility power supply fails. Consider the VSD system with only a dc link. In this case, the VSD operation is obtained with a separate power electronic converter/inverter set. Therefore, it is necessary to supply the dc link rather than supplying the ac input to the drive system. This reduces the complexity of the UPS. In this case, the uninterruptible part of the power supply has the configuration shown in Figure 4.2. The proposed UMD system for VSD consists of a charger for the batteries and a discharger with a step-up of voltage to the dc link of the drive system. The subsystems may be different depending upon the requirement of the utility, such as unity power factor, source of alternate energy, the difference between the voltage levels of the alternate energy source and the dc link of the drive system, isolation requirements at the discharger end and charger front end, and the control strategies for the coordination of various subsystems. All these design parameters have a profound influence on the VA rating of the converter subsystems such as the charger and discharger, etc. The UMD consists of the subsystems shown in Figure 4.2, along with the drive module and motor. The uninterruptible power system may have different topologies for the subsystems. Some of these are briefly stated in the following section.

4.2.2 Topologies for the Charger Subsystem

The charger unit could have any one of the following type of converter subsystems [64].

Diode Bridge Rectifier with a Buck Converter

This is the simplest configuration as shown in Figure 4.3. The buck converter provides the voltage compatibility between the rectified dc link voltage and the battery voltage. Isolation between the ac source and battery may be required in some applications.

Diode Bridge Rectifier with a Power Factor Regulator and a Down Stream Buck Converter

The power factor regulator provides unity power factor and allows sinusoidal currents to be drawn from the ac source, as shown in Figure 4.4. This requirement is likely to be made universal in the course of time due to advantages to the utilities in the form of energy savings and

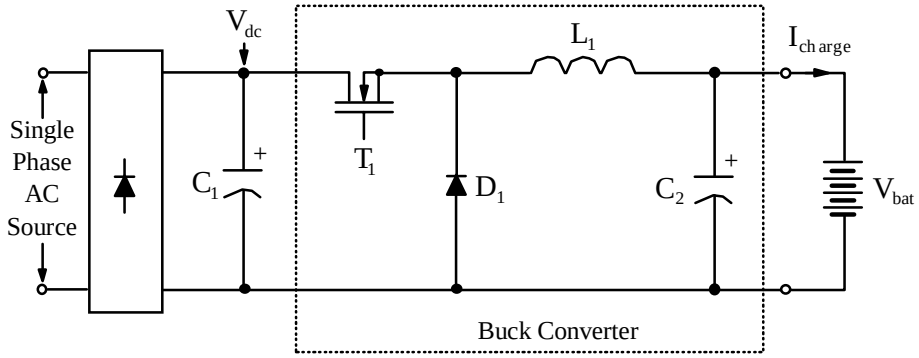


Figure 4.3 Diode bridge rectifier with a buck converter.

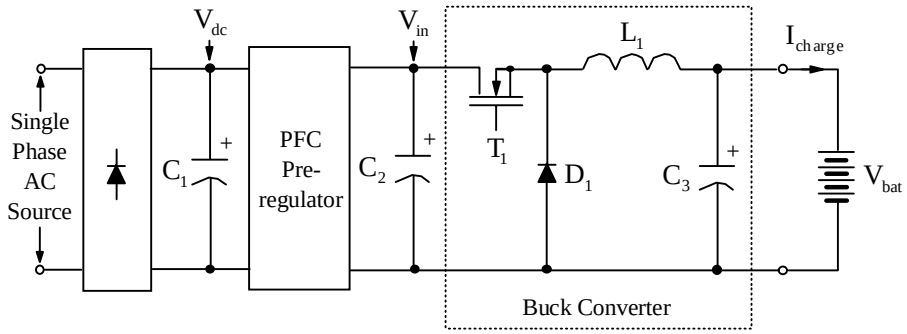


Figure 4.4 Diode bridge rectifier with a PFC preregulator and a buck converter.

reduced harmonics. For the consumer, it provides compactness of the converter subsystem, protection from interference with communication and other sensitive equipment.

Charger With High Frequency Transformer Isolation

If isolation is a system requirement, then a high frequency transformer is introduced as shown in Figure 4.5. The high frequency operation allows size reduction of the transformer and output filter. This configuration is suitable for charging batteries intended for low power applications such as appliances. Note that introduction of an anti-parallel diode across T_1 and a switching device across D_1 gives bi-directional power flow capability, making it a charger/discharger subsystem.

4.2.3 Topologies for the Discharger Subsystem

Two distinct types of discharger topologies facilitate simpler implementation of the UMD. They are described below.

Boost Converter

A simple boost converter shown in Figure 4.6 facilitates the discharging of the battery to the dc link of the drive system during utility power failure. It is a single switch configuration and

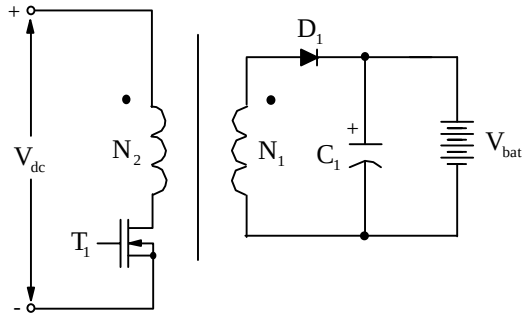


Figure 4.5 Charger with high frequency transformer isolation.

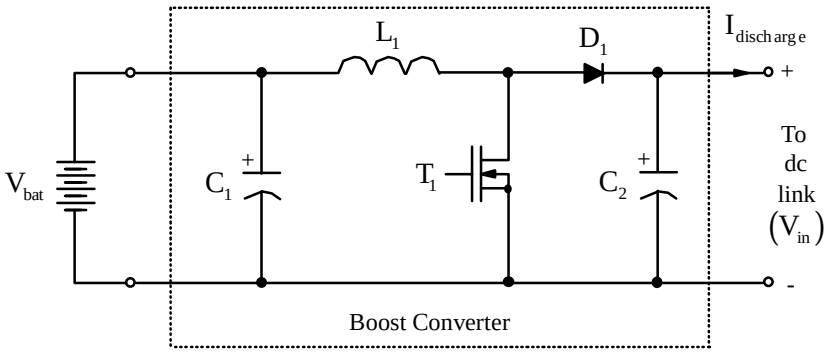


Figure 4.6 Boost converter as a discharger.

easiest to implement compared with any other method. The disadvantage is the boost converter would require nearly 5 to 10 times the rating of the motor drive system. This is unacceptable in many high power drive systems, but may be acceptable in appliance drives.

Forward Converter Topology

The forward converter topology shown in Figure 4.7 enables discharging at a lower VA rating, but involves a transformer to match the battery voltage to the dc link voltage. This is an additional requirement but it provides high efficiency in a compact subsystem due to the low power losses in the converter and transformer while compared to the boost converter scheme.

4.2.4 Comparison of Switch VA Ratings of Charger and Discharger Topologies

The dc link voltage and rated dc link current are considered base values for voltage and current, respectively, for making a comparison of the charger and discharger topologies.

Charger

Considering only the VA rating of power device, a comparison of charger topologies is given in Table 4.1. The transformer turns ratio, n, is equal to N_1/N_2. The voltage ratio between the dc

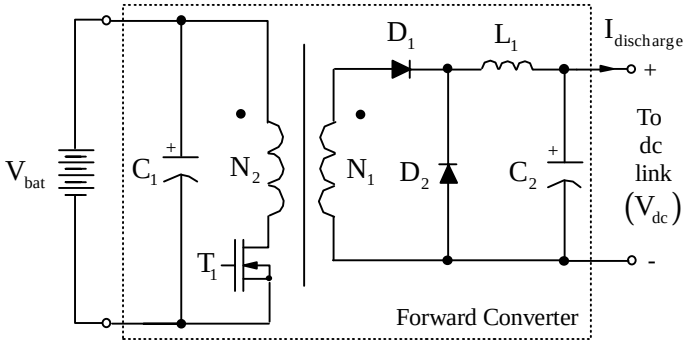


Figure 4.7 Forward converter as a discharger.

link and battery is a factor of n. It is assumed the battery charging switch rating current is 10% of its rated value. d denotes the duty cycle of the switch. A PFC with a buck configuration has a larger switch VA rating requirement, and thus may not be worth consideration for cost sensitive applications.

Table 4.1
Charger switch VA rating comparison.

Topology	V_{T1} , pu	I_{T1} , pu	P_{sw} , pu	Total P_{sw} , pu
Figure 4.3	1.0	$0.1n\sqrt{d}$	$0.10n\sqrt{d}$	$0.10n\sqrt{d}$
Figure 4.4 Buck	1.1	$0.1n\sqrt{d}$	$0.22n\sqrt{d}$	$0.22n\sqrt{d}$
PFC	1.1	$0.1n\sqrt{d}$	$0.11n\sqrt{d}$	
Figure 4.5	1.0	$0.1n\sqrt{d}$	$0.10n\sqrt{d}$	$0.10n\sqrt{d}$

Discharger

A brief comparison of switch VA ratings of discharger topologies is given in Table 4.2. Based on the comparison, the forward converter topology given in Figure 4.7 is preferable even though it requires a high frequency transformer. Further study is required to investigate various other topologies for discharger applications, particularly for high power motor drives.

Table 4.2
Discharger switch VA rating comparison.

Topology	V_{T1} , pu	I_{T1} , pu	P_{sw} , pu
Figure 4.6	1.1	$n\sqrt{d}$	$1.1n\sqrt{d}$
Figure 4.7	$2/n$	$n/\sqrt{d^3}$	$2/\sqrt{d^3}$

4.3 SRM-Based VSD as an UMD System

4.3.1 Configuration of the Proposed UMD System

Based on the developed UMD concept, a case study of UMD with the SRM drive system is performed in this section. The basic SRM-based VSD system as an UMD is illustrated in Figure 4.8. The proposed UMD system consists of four different functional modules: an input module which includes diode bridge rectifier and PFC preregulator, a charger and discharger module implemented by a conventional buck/boost scheme, a battery module and a C-dump converter based SRM drive module. Note that the charger unit which is implemented with the buck topology comes in both the versions with and without the PFC preregulator. The buck and boost converter is chosen based on the utility power readiness. A smooth transition is made possible due to the energy stored in the dc link capacitor as it would be able to supply the drive system

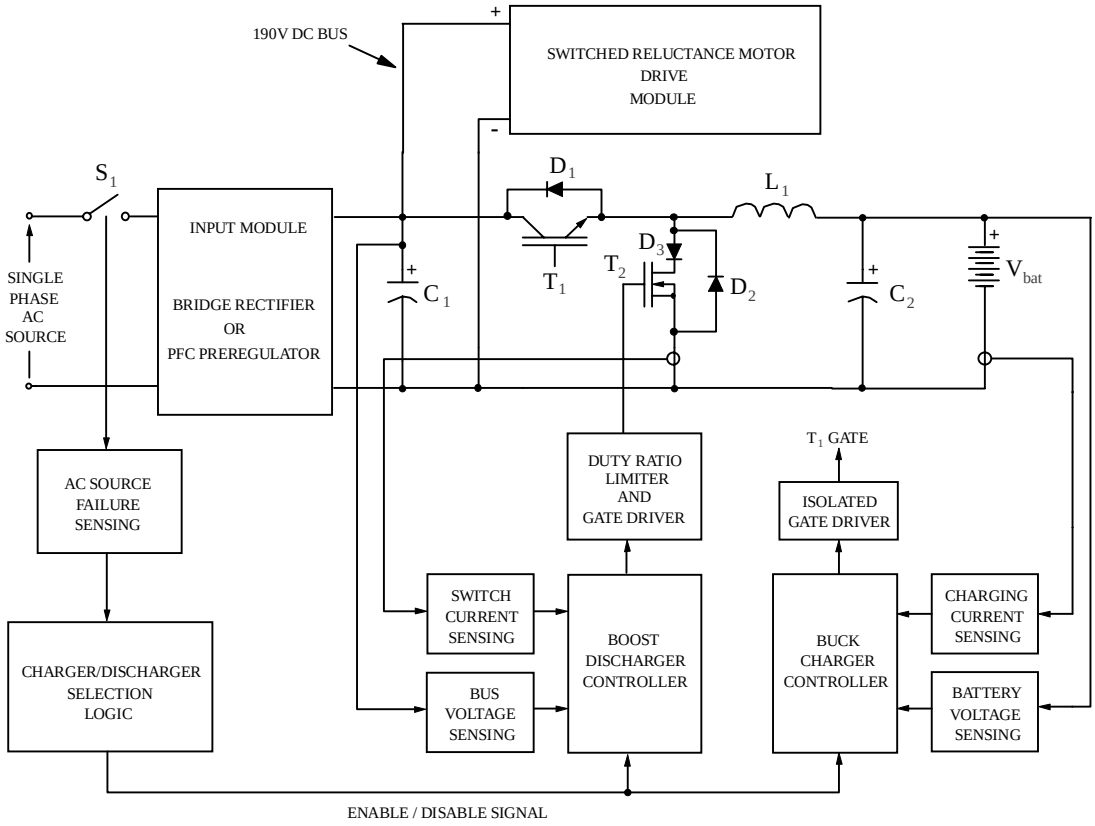


Figure 4.8 The simplified block diagram of the proposed UMD system.

until the boost comes on fully to meet the load requirement. Charging of the battery is controlled by the current limiting loop so it does not exceed the upper preset level. The voltage loop is to regulate the voltage at the preset level. The charger unit is approximately 10% of the battery VA capability due to the low current charging preferred for longer battery life.

The discharger unit has a boost power converter with an inner current limit circuit to protect the power switching device. It also contains a voltage loop to maintain the dc link voltage of the SRM drive system at the desired level. The duty ratio limit circuit is employed to set the maximum boost gain to five when there is a 20% drop in battery voltage.

The C-dump converter shown in Figure 3.6 is used in this study. The C-dump converter gives the most flexible control of the motor with the least number of switching devices [2, 13, 27]. The drive control strategies are illustrated in section 3.4.

4.3.2 Analysis of Charger/Discharger Circuit

A bi-directional charger/discharger circuit is implemented with a combination of buck and boost converters for charger and discharger, respectively. The basic circuit is illustrated in Figure 4.9. Note that the power inductor L_1 is shared between both converters, thus saving space. The motor drive is represented as the equivalent resistive load, R_{LOAD}, which is a function of the motor speed. T_1 is the buck switch implemented with an IGBT switching device, and D_2 is the

freewheeling diode for the buck charger. The MOSFET boost switch, T_2, is operating with the boost diode D_1. The battery module is modeled as a resistor in series with a voltage source. There are two distinct operational states in both charging and discharging modes. The relationship between these states is defined in Figure 4.10. The charger/discharger scheme implemented in this study operates in the discontinuous conduction mode because its average inductor current, I_{chg} in charging mode or I_{dcg} in discharging mode, is less than half of the inductor ripple current, Δi_L. This relationship is shown in Figure 4.11. Three duty cycles in discontinuous conduction mode are defined in the figure. T_s is the switching period in charging or discharging mode. The relationship between three duty cycles is presented as

$$d_1 + d_2 + d_3 = 1 . \tag{4.1}$$

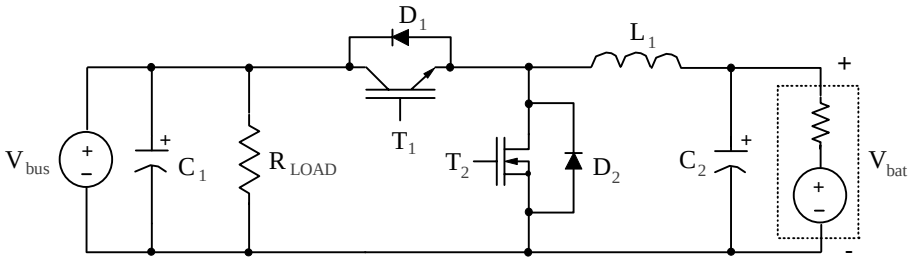


Figure 4.9 Simplified circuit diagram of the proposed charger/discharger.

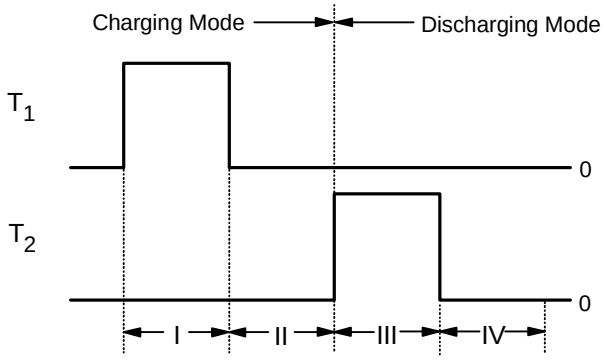


Figure 4.10 Four operational modes of the proposed charger/discharger.

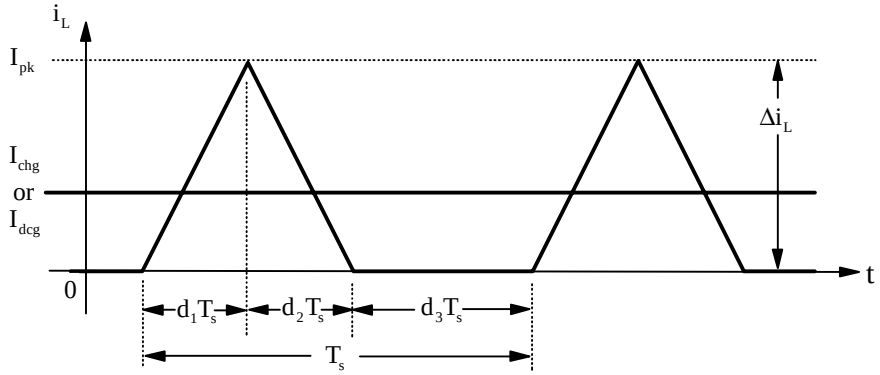


Figure 4.11 Illustration of duty cycles in the proposed charger/discharger.

where d_1 corresponds to switch on time and d_2 relates to the freewheeling time of a diode in both charger and discharger circuits.

The equivalent circuit diagrams for the four operational modes in Figure 4.10 are shown in Figure 4.12. The operational modes of the charger/discharger circuit are explained and expressions of duty cycles and peak current are derived as follows:

Mode I : T_1 on and T_2 off

This mode occurs in the battery charging mode. Both the motor drive power and the battery charging power are supplied by the bus voltage, V_{bus} which is considered an input source. There are two current paths in this mode, as illustrated in Figure 4.12. The expressions for the battery charging current, $i_{ch}(on)$, and the bus current, i_{bus}, in this operational mode are as follows:

$$i_{ch}(on) = \frac{(V_{bus} - V_{bat})}{L_1} \cdot d_1(buck) \cdot T_s(buck) \text{ , A.} \tag{4.2}$$

$$i_{bus} = i_L + i_{ch}(on) \text{ , A.} \tag{4.3}$$

where, $d_1(buck)$ is the duty ratio of the buck charger, $T_s(buck)$ is the switching period of the buck charger and i_L is the load current supplied to the SRM drive.

If we assume input and output voltages are constant, the duty ratio of the buck switch is [5]:

$$d_1(buck) = \frac{V_{bat}}{V_{bus}} \sqrt{\frac{2I_o \cdot L_1 \cdot f_c(buck)}{V_{bat}} \left(\frac{V_{bus}}{V_{bus} - V_{bat}} \right)}. \tag{4.4}$$

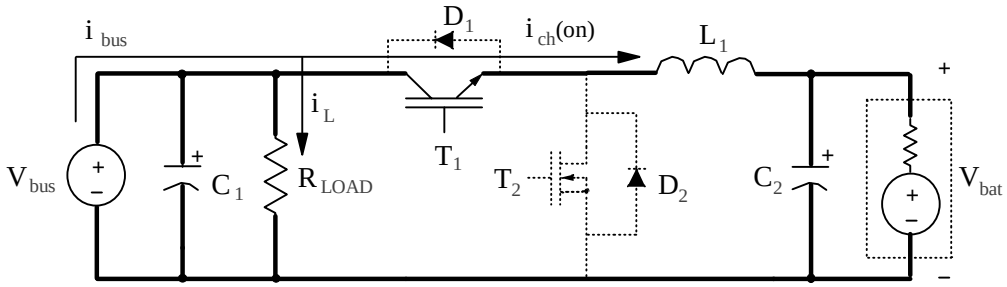
where

V_{bat}	=	buck charger output voltage, V
V_{bus}	=	buck charger input voltage, V
$I_o(buck)$	=	buck charger output current, A
L_1	=	inductance of buck inductor, H
$f_c(buck)$	=	switching frequency of buck charger, Hz

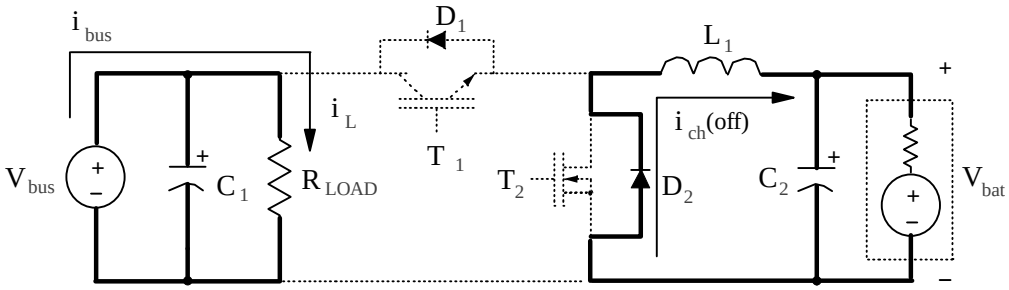
Mode II : Both T_1 and T_2 off

When the buck switch T_1 is turned off, then the charging power is supplied by the energy stored in L_1. The power for the motor drive load is supplied by the bus voltage. The buck mode charging operation continues until the source power is interrupted. There are two current paths: one is the battery charging current, which is freewheeling through diode D_2 and inductor L_1, and the other one is the bus current supplying the SRM drive. The bus current is equal to the load current in this mode.

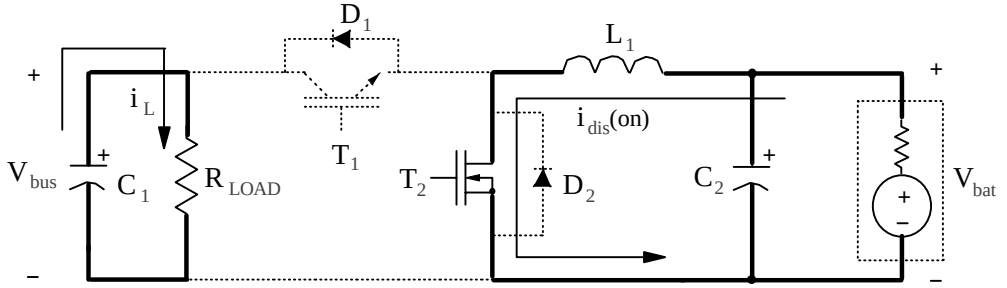
$$i_{ch}(off) = \frac{V_{bat}}{L_1} \cdot d_2(buck) \cdot T_s(buck) \text{ , A.} \tag{4.5}$$



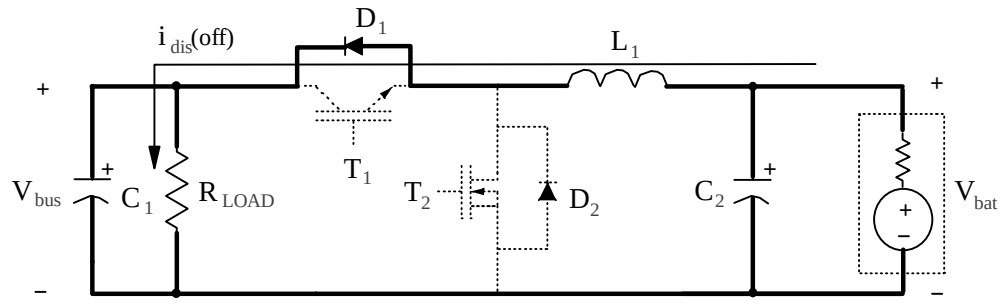
Mode I: T_1 on and T_2 off (charging mode)



Mode II: T_1 and T_2 off (charging mode)



Mode III: T_2 on and T_1 off (discharging mode)



Mode IV: T_2 and T_1 off (discharging mode)

Figure 4.12 Equivalent circuits of four operational modes in charger/discharger.

$$i_{bus} = i_L \text{ , A.} \tag{4.6}$$

The duty ratio of the diode, $d_2(buck)$, is calculated in terms of $d_1(buck)$ as

$$d_2(buck) = \frac{I_o(buck) \cdot L_1 \cdot f_c(buck)}{2V_{bat} \cdot d_1(buck)} . \tag{4.7}$$

The peak inductor current in charging mode is evaluated as,

$$I_{pk}(buck) = \frac{d_2(buck) \cdot V_{bat}}{f_c(buck) \cdot L_1} \text{ , A.} \tag{4.8}$$

The ratings and losses for key power components in the buck charger are summarized in Table 4.3 and 4.4, respectively. An IGBT device is used for a buck switch. The loss model for the buck charger circuit is derived based on loss equations (Table 4.4) and the bridge rectifier conduction losses (Table 2.2) as follows:

$$P_{UMD}(buck) = (4.45)\left[d_1(buck) + d_2(buck)\right]d_2^2(buck) + \left[9.79 + (69.60)\sqrt{d_1(buck)} + (31.64)\sqrt{d_2(buck)}\right]d_2(buck) + 3.60 \text{ , W.} \tag{4.9}$$

It should be mentioned that the constant term is the switching loss of a freewheeling diode. It is obtained with the diode switching loss equation in Table 3.2. The derived equation is used to evaluate the losses in the charger circuit. The predicted efficiency of the buck charger is explained in section 2.4.2.

Table 4.3
Ratings for key power components in buck charger.

Device	**Duty cycle**	**Ratings**		
		Voltage	**Current**	
			Peak	**RMS**
Buck switch	$d_1(buck)$	V_{bus}	$I_{pk}(buck)$	$I_{pk}(buck)\sqrt{\frac{d_1}{3}}$
Freewheeling diode	$d_2(buck)$	V_{bus}	$I_{pk}(buck)$	$I_{pk}(buck)\sqrt{\frac{d_2}{3}}$
Inductor	1	V_{bus}	$I_{pk}(buck)$	$I_{pk}(buck)\sqrt{\frac{d_1 + d_2}{3}}$

Table 4.4
Losses for key power components in buck charger.

Device	Duty cycle	Losses	
		Conduction	Switching
Buck switch	$d_1(buck)$	$I_{sw}(rms)\cdot V_{CE}(sat)$	$\frac{1}{2}V_{in}\cdot I_{pk}(buck)\times f_c(buck)\cdot(t_r+t_f)$
Freewheeling diode	$d_2(buck)$	$I_d(rms)\cdot V_f$	$E_{rr}\cdot f_c(buck)$
Inductor	1	$I_L^2(rms)\cdot R_{dc}$	-

where,

$V_{CE}(sat)$ = collector-to-emitter saturation voltage of an IGBT switch , V
t_r = rise time of an IGBT switch, s
t_f = fall time of an IGBT switch, s
V_f = forward voltage drop of freewheeling diode, V
E_{rr} = reverse recovery energy of freewheeling diode, J
R_{dc} = dc resistance of inductor, Ω

Mode III : T_2 on and T_1 off

When the source power is turned off, the converter immediately enters the discharging mode. The first mode in the discharging operation is Mode III. The power for the motor drive is supplied by the energy stored in the bus capacitor only. The battery voltage is shorted through the boost inductor by the boost switch, T_2, to store the energy into the boost inductor. Two distinct currents in this mode are,

$$i_{dis}(on)=\frac{V_{bat}}{L_1}\cdot d_1(boost)\cdot T_s(boost)\ \text{, A.} \tag{4.10}$$

$$i_L=C_1\cdot\frac{V_{bus}}{d_1(boost)\cdot T_s(boost)}\ \text{, A.} \tag{4.11}$$

An IGBT switching device is used for the boost switch. The duty ratio of the boost switch is calculated as [5],

$$d_1(boost)=\sqrt{\frac{I_o(boost)\cdot L_1\cdot f_c(boost)}{V_{bat}}\left(\frac{V_{bus}}{V_{bat}}-1\right)}. \tag{4.12}$$

where,

$I_o(boost)$ = boost discharger output current , A
$f_c(boost)$ = switching frequency of boost discharger , Hz

Mode IV : Both T_2 and T_1 off

The power for the motor drive is supplied by the battery only. The low battery voltage is boosted up to the original bus voltage level. The boost switch, T_2, and diode, D_1, provide the boost action along with the inductor, L_1. Note that the direction of the current is reversed.

$$i_{dis}(off) = \frac{(V_{bat} - V_{bus})}{L_1} \cdot d_2(boost) \cdot T_s(boost) \text{ , A.} \tag{4.13}$$

The duty cycle of the boost diode is obtained as follows:

$$d_2(boost) = \sqrt{\frac{I_o(boost) \cdot L_1 \cdot f_c(boost)}{V_{bus} - V_{bat}}} . \tag{4.14}$$

The peak current of the boost inductor is expressed as,

$$I_{pk}(boost) = \frac{d_1(boost) \cdot V_{bat}}{f_c(boost) \cdot L_1} \text{ , A.} \tag{4.15}$$

With the above equations, the ratings and losses of major power components in the boost discharger are tabulated in Tables 4.5 and 4.6. Two paralleled MOSFET switching devices are used for a buck switch.

Table 4.5
Ratings for key power components in boost discharger.

Device	**Duty cycle**	**Ratings**		
		Voltage	**Current**	
			Peak	**RMS**
Boost switch	$d_1(boost)$	V_{bus}	$I_{pk}(boost)$	$I_{pk}(boost)\sqrt{\frac{d_1(boost)}{3}}$
Freewheeling diode	$d_2(boost)$	V_{bus}	$I_{pk}(boost)$	$I_{pk}(boost)\sqrt{\frac{d_2(boost)}{3}}$
Inductor	1	V_{bus}	$I_{pk}(boost)$	$I_{pk}(boost)\sqrt{\frac{d_1(boost)+d_2(boost)}{3}}$

Table 4.6
Losses for key power components in boost discharger.

Device	Duty cycle	Losses	
		Conduction	Switching
Boost switch	$d_1(boost)$	$\frac{1}{2} I_{sw}^2(rms) \cdot R_{ds}(on) + I_{sw}(rms) \cdot V_f$	$\frac{1}{2} V_{bus} \cdot I_{pk}(boost) \times f_c(boost) \cdot (t_r + t_f)$
Freewheeling diode	$d_2(boost)$	$I_d(rms) \cdot V_f$	$E_{rr} \cdot f_c$
Inductor	1	$I_L^2(rms) \cdot R_{dc}$	-

where,

$R_{ds}(on)$ = static drain-to-source on-resistance of a MOSFET switch, Ω
t_r = rise time of a MOSFET switch, s
t_f = fall time of a MOSFET switch, s

The total loss model of the boost discharger is obtained in terms of $d_1(boost)$ and $d_2(boost)$ and based on the equation in Table 4.6:

$$P_{UMD}(boost) = (3.82) d_1^3(boost) + (2.30) d_1^2(boost) \cdot d_2(boost) + \left[3.04 + (10.63)\left(\sqrt{d_1(boost)} + \sqrt{d_2(boost)}\right)\right] d_1(boost) + 0.62 \text{ , W.} \quad (4.16)$$

The constant term in the loss model is the boost diode switching loss obtained with the diode switching loss equation in Table 3.2. The efficiency calculation of the boost discharger is similar to the buck charger case.

4.4 Experimental Verification

4.4.1 Experimental Setup and Method

The simplified block diagram of the experimental setup to verify the concept of SRM-based UMD is shown in Figure 4.13. It consists of four functional modules as explained in section 4.3. A 250W 8/6 SRM has been designed and built for the experimental system. The C-Dump converter for the SRM drive is MOSFET-based. The charger is built using an IGBT switch and tested with and without a PFC preregulator. The battery module consists of four series-connected, sealed, lead-acid rechargeable batteries; each having a 12V and 7Ah rating. A permanent-magnet brush dc generator with a resistive bank serves as the load to the SRM drive system. The supply is 120V, 60Hz ac single-phase. The losses of the dc generator, as a function of speed and current, have been experimentally pre-determined. Therefore the input to the dc generator is equal to the output of the SRM-based VSD, which consists of the power dissipated in the resistive bank and losses in the dc generator. All the ac and dc power is averaged and

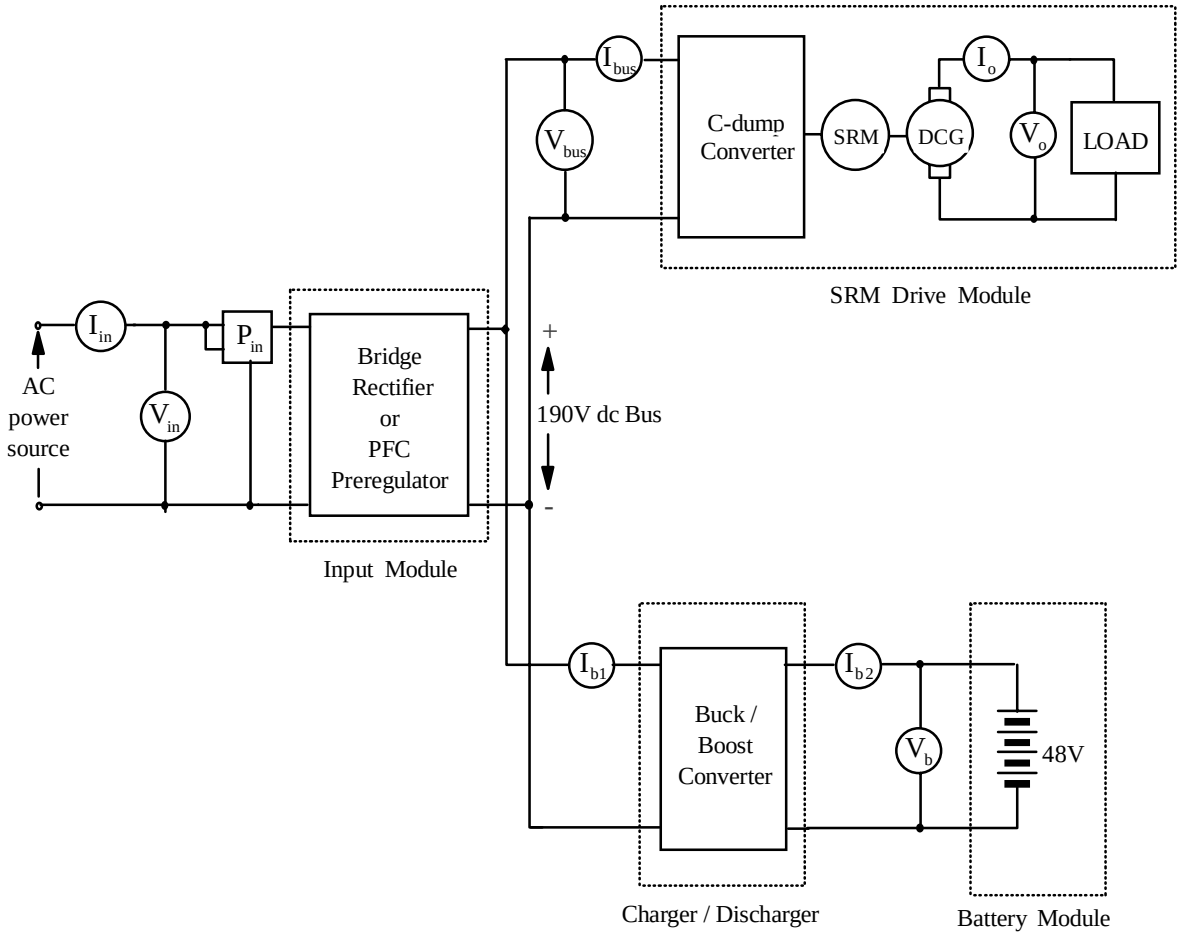


Figure 4.13 Experimental test setup for UMD system with SRM-based VSD.

measured using voltmeters, ammeters and precision wattmeters. It is estimated the error in the readings is on the order of 1 to 2%. A transient waveform verifying the UMD system at certain speed is obtained after sufficient charging of the battery module. If the charging current settles down to 2A peak, the battery is considered fully charged. By interrupting the input ac power, the transient inductor current waveform is captured. At the same time, the SRM phase current waveform is also taken to investigate the effectiveness of the UMD system. The various measurements for obtaining efficiencies in charging and discharging modes are taken from 100r/min to 2,000r/min with 100r/min speed increments. Identical experiments are repeated for the system with and without the PFC preregulator.

4.4.2 Experimental Results and Discussion

Experimental Results

The experimental results are focused on the functioning of the UMD system, proper operation of the charger and discharger modules, evaluation of the total system efficiency in the charging and discharging modes and the efficiency of the discharger module. The later aspect has the most

deleterious effect on the system efficiency. The predicted efficiency obtained in the succeeding section is compared with the measured one to validate the analysis.

Charger/Discharger Waveforms

Figure 4.14 shows the gate drive signals of the buck/boost switches before and after power failure with no power to the UMD. V_{g1} is the gate signal, isolated by the pulse transformer, for the charger switch, T_1 [4], and V_{g2} is directly connected to the gate of the boost switch T_2. The transition time of gate drive signals is within 80μs when the power failure occurs.

The current in one phase of the machine is shown in Figure 4.15. Charging/discharging currents as seen through the inductor in the buck/boost charger/discharger converter modules in the charging mode and the discharging mode are also shown. Since the discharging current is positive, the charging current appears negative in the oscillogram. Note that the charging and discharging actions are taken for two different instances. The charging current has a peak of 2A and a duty cycle of approximately 3%. This is because the dc link voltage is near 190V, whereas the battery module is at 48V nominal. The discharging current reaches a peak of 7A, but due to the short duration of discharging, the peak is nearly 3.5 times the current required for the drive system. The boost converter is optimally designed with an inductor which minimizes the peak current, but gives a higher duty cycle. From a practical point of view, it is desirable to have a continuous current in the inductor, even though the discharging current is discontinuous.

The transient response of the charger/discharger module during a utility power failure mode is shown in Figure 4.16. The phase current of the SRM has a small increase, whereas the inductor current goes as high as 10A during the first cycle of the transient. Note it settles down to the steady state value of 7A within 7 phase cycles of the SRM drive. This transient can be eliminated by soft transitioning from the charging and discharging mode, and by using a sizable dc link capacitor to supply stored energy during this transition.

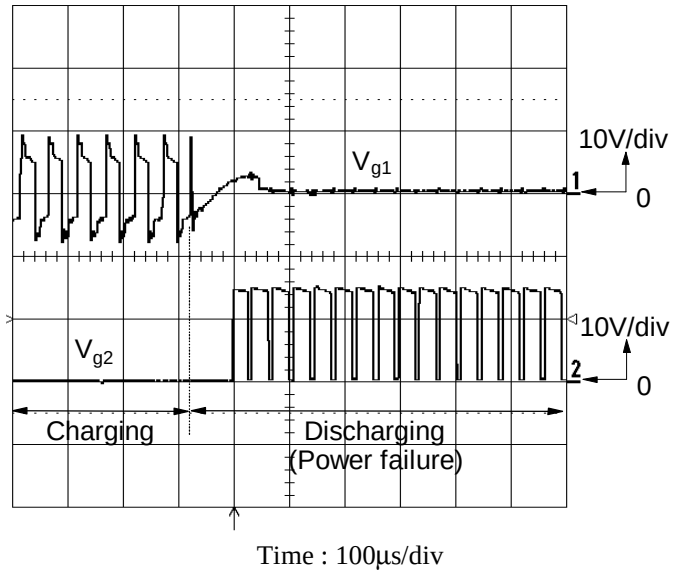


Figure 4.14 Transient gate drive signals for charger/discharger.

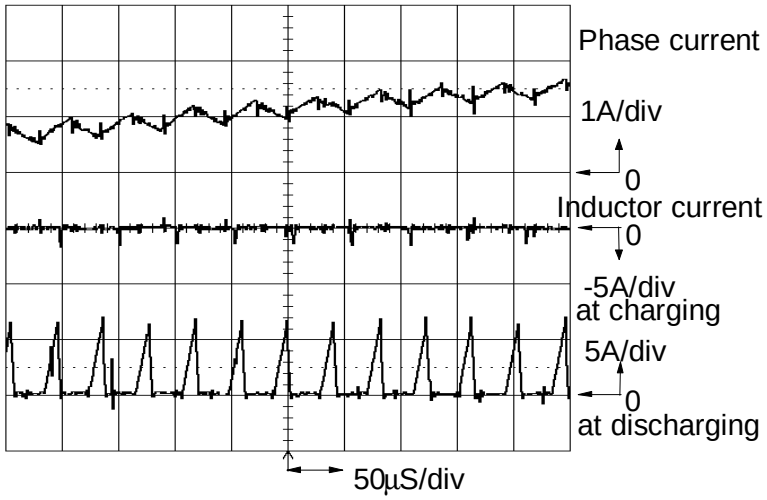


Figure 4.15 Current waveforms of SRM phase and inductor in charger/discharger at 1,000r/min.

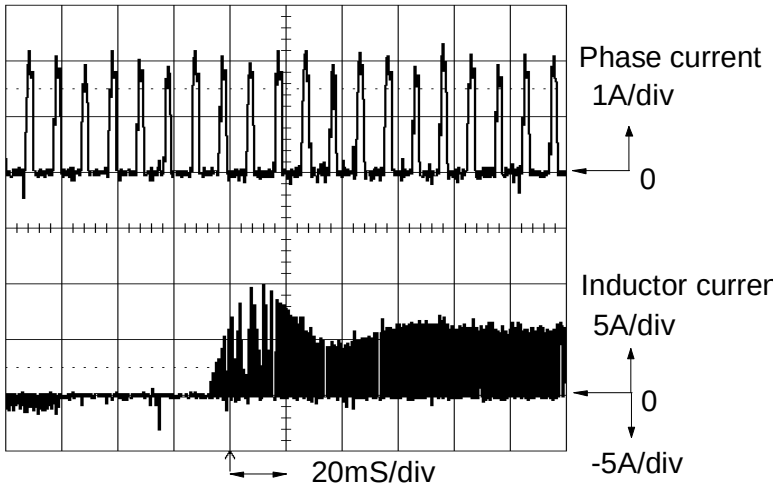


Figure 4.16 Transient current waveforms of SRM phase and inductor in charger/discharger at 1,000r/min.

4.4.3 System Performance

Charging Mode

During the charging mode, the utility input power supplies the power for SRM drive and charging power for the battery module as shown in Figure 4.17(i). The overall efficiency is the ratio between the sum of the charging power and the SRM's output to input power.

The system efficiency evaluated for the UMD with and without the power factor preregulator is shown in Figures 4.17(ii) and (iii) as a function of motor speed. Both efficiencies closely match over the entire power output range. The efficiency of the system without the power factor correction circuit has been consistently high, by a margin of 5%, throughout the entire speed range when compared to the case with the power factor preregulator. This is because the PFC preregulator contains losses in its control circuit, active and passive devices over and above that of the diode bridge rectifier. Hence its losses are higher than the simple diode bridge rectifier circuit, contributing to the poorer overall system efficiency throughout the speed region. Note the rated power of the appliance SRM drive is only 75W and a few watts of additional losses result in a significant drop in efficiency.

The predicted error of the overall UMD system efficiency in the charging mode is illustrated for cases with and without a PFC in Figure 4.18. Its statistical analysis results are shown in Table 4.7. The large prediction error (>20%) occurs in the speed range below 500r/min, in both cases with and without the PFC preregulator. This is shown in Figure 4.18. This indicates the derived loss model is useful to predict the high speed range only.

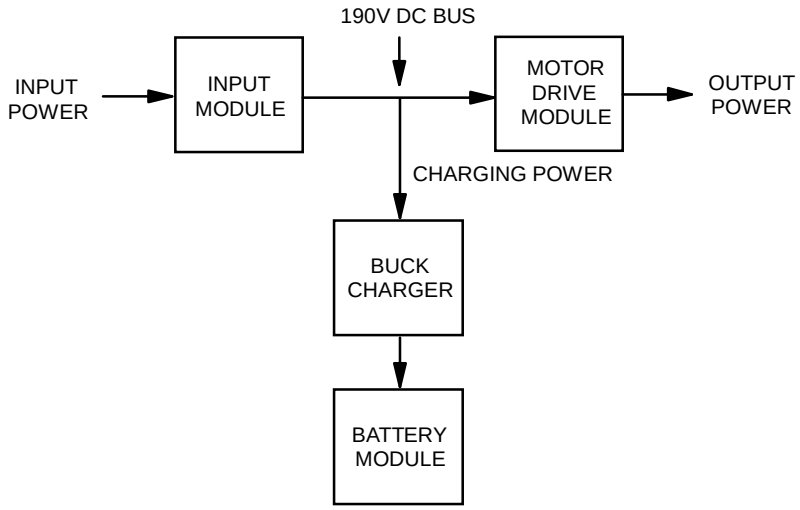


Figure 4.17(i) Power flow in charging mode.

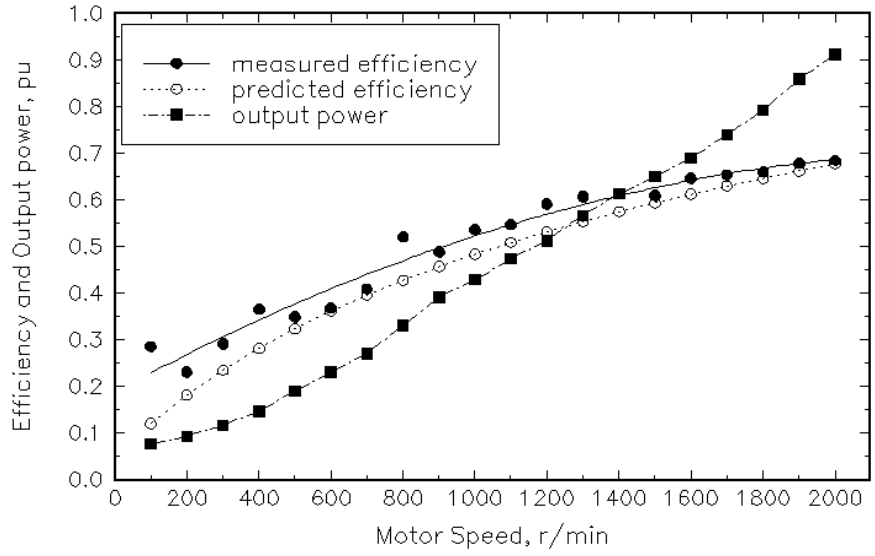


Figure 4.17(ii) Overall system efficiency and normalized output power in charging mode without PFC preregulator.

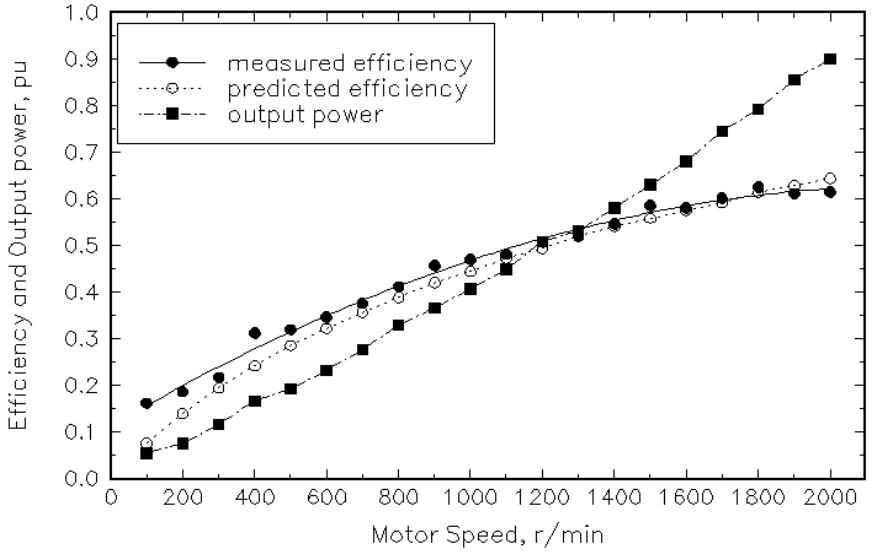


Figure 4.17(iii) Overall system efficiency and normalized output power in charging mode with PFC preregulator.

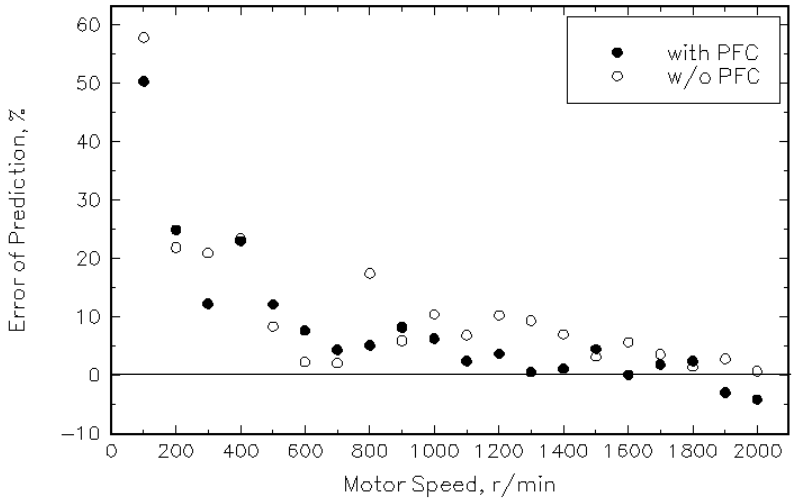


Figure 4.18 Error of prediction of the SRM-based UMD system efficiency with and without the PFC at charging mode.

Table 4.7
Statistical analysis of efficiency prediction errors for UMD drive system with and without the PFC preregulator.

	Fig. 4.17(i) without PFC	Fig. 4.17(ii) with PFC
Total Observation	20	20
Minimum Error	0.63	-4.20
Maximum Error	57.82	50.37
Mean	11.05	8.16
Median	6.89	4.39
Variance	170.67	154.37
Standard Deviation	13.06	12.42
Standard Error	2.92	2.78

Discharging Mode

During a utility power failure, the battery energy is transferred to the dc link through the boost discharger to meet the load of the SRM drive system, as shown in Figure 4.19(i). To increase the efficiency of the overall system during this time, it is important to have the discharger module operating at a high efficiency.

Measured and predicted efficiencies of the boost discharger in the discharging mode are shown in Figure 4.19(ii) without a PFC preregulator. The predicted efficiency is obtained based on the derived loss model found in equation (4.17). Both measured and predicted efficiencies closely match over the entire speed range. The efficiency prediction error of the boost discharger is

shown in Figure 4.19(iii) and Table 4.8. The derived loss model provides fairly accurate efficiency prediction for the boost discharger. But the prediction errors for speeds less than 500r/min are larger when compared to the higher speed ranges.

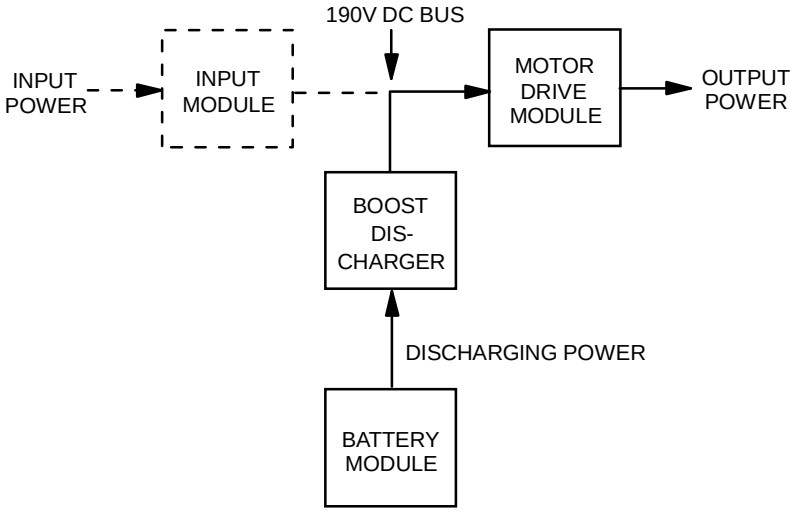


Figure 4.19(i) Power flow in discharging mode.

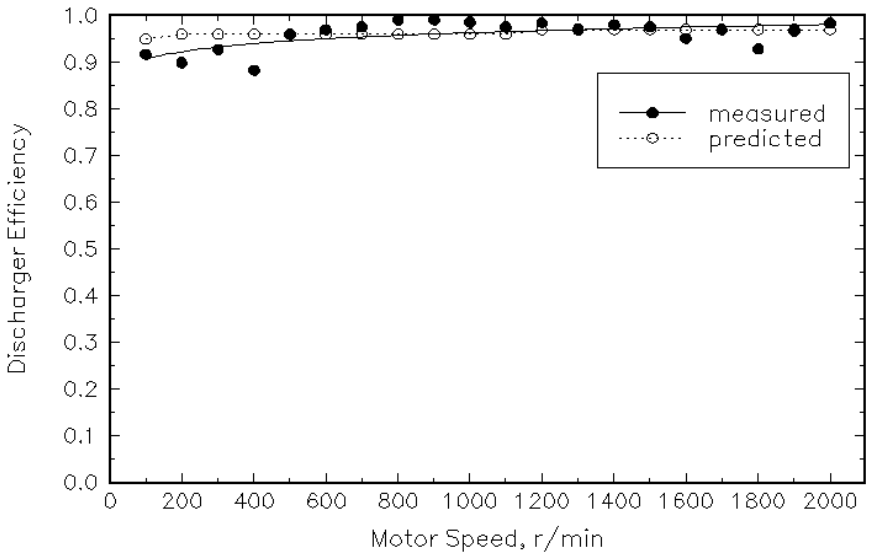


Figure 4.19(ii) Boost discharger efficiency in discharging mode.

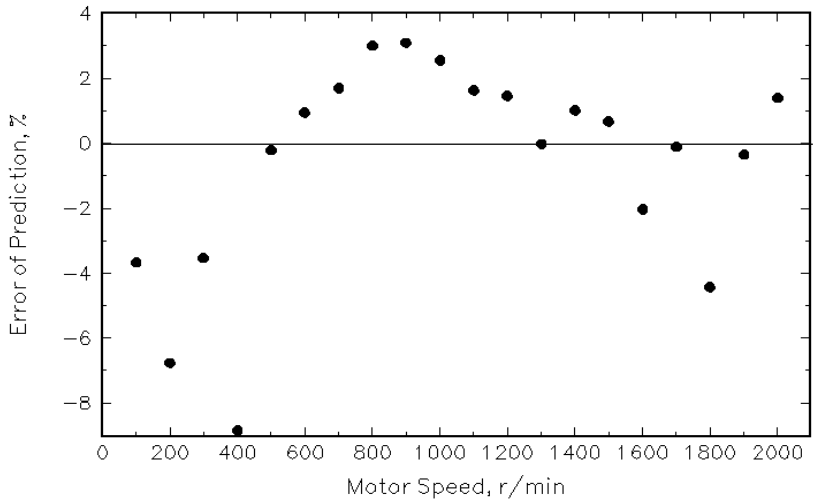


Figure 4.19(iii) Efficiency prediction error versus SRM speed for boost discharger in UMD system.

Table 4.8
Statistical analysis of efficiency prediction errors for boost discharger.

	Fig. 4.19(ii)
Total Observation	20
Minimum Error	-8.84
Maximum Error	3.09
Mean	-0.63
Median	0.32
Variance	10.69
Standard Deviation	3.27
Standard Error	0.73

The overall system efficiency during the discharging mode is defined as the ratio between the SRM's output and the battery module's output. As shown in Figure 4.19(iv), the efficiency is lower than the charging mode by nearly 7%. This is caused by factors such as higher losses in the boost converter due to the higher pulse currents involved during this mode. The power supply for the PFC preregulator is always connected to the bus, lowering the overall system efficiency slightly. Efficiency with the PFC preregulator is lower than that of the simple diode bridge case because the control logic keeps drawing the power from the dc link even during its off mode.

The predicted efficiency error in the discharging mode is shown in Figure 4.19(v) and Table 4.9. The predicted efficiency error of the UMD system in the discharging mode shows larger values below the 300r/min speed range when compared to the higher speed ranges. The derived loss model for the UMD system is valid for efficiency prediction over that speed range.

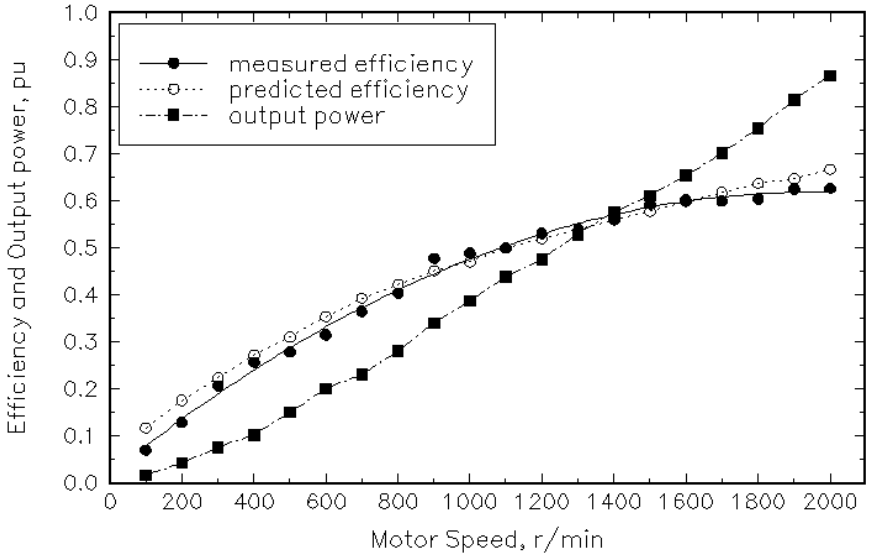


Figure 4.19(iv) Overall system efficiency and normalized output power in discharging mode without PFC preregulator.

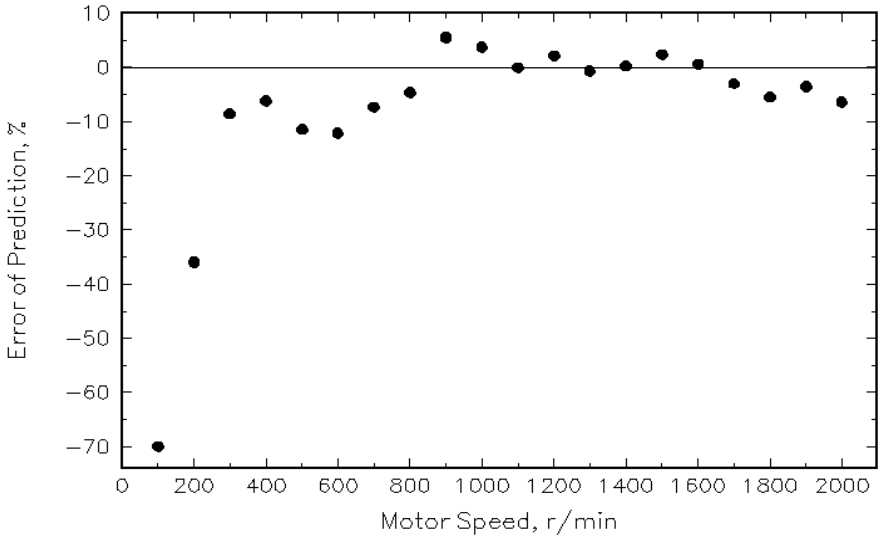


Figure 4.19(v) Prediction error versus SRM speed for UMD overall system efficiency in discharging mode.

Table 4.9
Statistical analysis of efficiency prediction errors for SRM-based UMD system in discharging mode without PFC preregulator.

	Fig. 4.19(iv) without PFC
Total Observation	20
Minimum Error	-69.96
Maximum Error	5.48
Mean	-8.04
Median	-4.09
Variance	289.93
Standard Deviation	17.03
Standard Error	3.81

4.5 Conclusions

The concept of a UMD for various uninterrupted VSD applications is proposed. The viability of the UMD concept has been illustrated with a 250W, 8/6 SRM-based VSD system. Various topologies for the UMD have been considered and a comparison between various UMD topologies is performed based on the VA ratings. One such topology, consisting of a buck/boost charger/discharger, has been experimentally evaluated.

The UMD system performance during both steady-state and transient periods have been investigated and the overall efficiency of the UMD system during the charging and discharging modes have been experimentally measured. The transient response of the UMD system during the utility power failure is experimentally tested. The motor phase current settles down within seven phase cycles of the SRM drive system with a small increase in its magnitude.

The power ratings and loss models for the buck charger and boost discharger topologies are developed to investigate steady-state system performance when considering the overall UMD system efficiency.

The system has been evaluated with and without the PFC preregulator, as the PFC will become mandated in the future. The predicted efficiencies of the UMD system with and without a PFC preregulator are obtained with the developed loss models and compared with the measured values. The developed loss model for the UMD system does not provide an accurate efficiency prediction in the low speed region because the overall system efficiency prediction in both charging and discharging modes shows relatively large errors. On the other hand, the loss model efficiency predictions for the boost discharger match the measured efficiency over the entire speed range. Significant efficiency loss occurs in the charging mode due to the inclusion of the PFC preregulator in the drive system. This is an important factor to be considered in applications.