Electrical, Magnetic, Thermal Modeling and Analysis of a 5000A Solid-State Switch Module and Its Application as a DC Circuit Breaker

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By
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ABSTRACT

This dissertation presents a systematic design and demonstration of a novel solid-state DC circuit breaker.

The mechanical circuit breaker is widely used in power systems to protect industrial equipment during fault or abnormal conditions. Compared with the slow and high-maintenance mechanical circuit breaker, the solid-state circuit breaker is capable of high-speed interruption of high currents without generating an arc, hence it is maintenance-free. Both the switch and the tripping unit are solid-state, which meet the requirements of precise protection and high reliability. The major challenge in developing and adopting a solid-state circuit breaker has been the lack of power semiconductor switches that have adequate current-carrying capability and interruption capability.

The high-speed, high-current solid-state DC circuit breaker proposed and demonstrated here uses a newly-emerging power semiconductor switch, the emitter turn-off (ETO) thyristor as the main interruption switch. In order to meet the requirement of being a high-current circuit breaker, ETO parallel operation is needed. Therefore the major effort of this dissertation is dedicated to the development of a high-current (5000A) DC switch module that utilizes multiple ETOs in parallel. This work can also be used to develop an AC switch module by changing the asymmetrical ETOs used to symmetrical ETOs.

An accurate device model of the ETO is needed for the development of the high-current DC switch module. In this dissertation a novel physics-base lumped charge model is developed for the ETO thyristor for the first time. This model is verified experimentally and used for the research and development of the emitter turn-off (ETO) thyristor as well as the DC switch module discussed in this dissertation.

With the aid of the developed device model, the device current sharing between paralleled multiple ETO thyristors is investigated. Current sharing is difficult to achieve for a thyristor-type device due to the large device parameter variations and strong positive feedback mechanism in a latched thyristor. The author proposes the "DirectETO" concept that directly benefits from the high-speed capability of the ETO and strong thermal couplings among ETOs. A high-current DC switch module based on the DirectETO can be realized by directly connecting ETOs in parallel without the bulky current sharing inductors used in other current-sharing solutions.

In order to achieve voltage stress suppression under high current conditions, the parasitic parameters, especially parasitic inductance in a high-current ETO switch module are studied. The Partial Element Equivalent Circuit (PEEC) method is used to extract the parasitics. Combined with the developed device model, the electrical interactions among multiple ETOs are investigated which results in structural modification for the solid-state DC switch module.

The electro-thermal model of the DC switch module and the heatsink subsystem is used to identify the "thermal runaway" phenomenon in the module that is caused by the negative temperature coefficient of the ETO's conduction drop. The comparative study of the electro-thermal coupling identifies a strongly-coupled thermal network that increases the stability of the

thermal subsystem. The electro-thermal model is also used to calculate the DC and transient thermal limit of the DC switch module.

The high-current (5000A) DC switch module coupled with a solid state tripping unit is successfully applied as a high-speed, high-current solid-state DC circuit breaker. The experimental demonstration of a 5000A current interruption shows an interruption time of about 5 microseconds. This high-speed, high-current DC switch module can therefore be used in DC circuit breaker applications as well as other types of application, such as AC circuit breakers, transfer switches and fault current limiters.

Since the novel solid-state DC circuit breaker is able to extinguish the fault current even before it reaches an uncontrollable level, this feature provides a fast-acting, current-limiting protection scheme for power systems that is not possible with traditional circuit breakers. The potential impact on the power system is also discussed in this dissertation.

To My parents

and

My wife Min

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1.1.1 Mechanical Circuit Breaker

A circuit breaker is defined as a mechanical switching device, capable of making, carrying, and breaking currents under normal circuit conditions and also making and carrying currents for a specified time and breaking currents under specified abnormal circuit conditions such as in the case of a short circuit [A1].

A circuit breaker [A2] is a piece of equipment which is designed to protect an electrical apparatus from damage caused by overload or short circuit. Unlike a fuse, which operates once and then has to be replaced, a circuit breaker can be reset (either manually or automatically) to resume normal operation.

Circuit breakers are often implemented with a solenoid (electromagnet) whose strength increases as the current increases and eventually trips the circuit breaker or a bimetallic strip which heats and bends with increased current or combination of a solenoid and a bimetallic strip. The electromagnet generally instantaneously responds to short, large surges in current (short circuit) and the bimetallic strip responds to I^2t overcurrent conditions. Circuit breakers for larger currents are usually arranged with external sensors to sense a fault current and to operate the trip opening mechanism.

Under short-circuit conditions, the fault current is usually many times greater than the normal current flow. When a circuit breaker tries to interrupt this current, an arc may generate. In air-insulated and miniature breakers an arc chute structure consisting of metal plates or ceramic ridges cools the arc, and blowout coils deflect the arc into the arc chute. Larger circuit breakers such as those used in electrical power distribution may use a vacuum, an inert gas such as sulfur hexafluoride or have contacts immersed in oil to suppress the arc.

Circuit breakers can be classified according to their voltage levels.

Low-Voltage Circuit Breaker

A low voltage circuit breaker is often rated 1000V AC or below, or 300V DC and below. They can be further divided into the following subcategories.

- MCB (Miniature Circuit Breaker)— rated current not more than 100A. Trip characteristics are normally not adjustable. Thermal or thermal-magnetic operation.

- MCCB (Moulded Case Circuit Breaker)—rated current up to 1000A. Thermal or thermal-magnetic operation. Trip current may be adjustable.

- Air Circuit Breaker—Rated current up to 10,000A. Trip characteristics often fully adjustable including configurable trip thresholds and delays. Usually electronically controlled—some models are microprocessor controlled. Often used for main power distribution in large industrial plant, where the breakers are arranged in draw-out enclosures for ease of maintenance.

- Vacuum Circuit Breaker—With rated current up to 3000A, these breakers interrupt the arc in a vacuum bottle. These can also be applied at up to 35,000V. Vacuum breakers tend to have longer life expectancies between overhauls than do air circuit breakers.

High-Voltage Circuit Breakers

Figure 1-1 High-voltage circuit breaker at a power substation in TVA site

Electrical power transmission networks are protected and controlled by high-voltage breakers. The definition of "high voltage" varies but in power transmission work is usually thought to be 35,000V or higher. High-voltage breakers are nearly always solenoid operated,

with current-sensing protective relays operated through current transformers. In substations the protection relay scheme can be complex, protecting equipment and busses from various types of overload or ground/earth fault.

High-voltage breakers are broadly classified by the medium used to extinguish the arc.

- Oil-filled (dead tank and live tank)
- Oil-filled, minimum oil volume
- Air blast
- Sulfur hexafluoride (SF6)

High-voltage breakers are routinely available up to 765kV AC.

A mechanical circuit breaker can be found in the catalogs of different vendors, such as ABB, Siemens, GE, Westinghouse, Square D, Cutler-Hammer and so on.

In summary, the mechanical circuit breaker is dominant in power systems to protect the industrial equipment in fault / abnormal conditions. They have a full range of voltage ratings, from residential level to transmission level, current rating from a few amperes to thousands of amperes. They are bulky and heavy. Since they utilize a mechanical actuator (typically spring or hydraulic), their response time is in the range of tens of milliseconds.

1.1.2 Solid-State Circuit Breaker

Utility engineers faced with the challenges of integrating new generations into existing power systems, clearing faults more quickly, or finding an alternative to SF6 breakers will soon have a new product to meet all of their needs: a solid-state current-limiting circuit breaker. Electric utilities have long wished for a practical, reasonably-priced, solid-state circuit breaker which could provide very reliable service with little maintenance [A3].

A solid-state circuit breaker can offer the following advantages:

- High-speed interruption
- Limited fault current
- Limited inrush current
- No arc generated
- High reliability and maintenance-free
- Low line disturbance
- Possible to include precise / intelligent fault control

The solid-state circuit breaker is widely used in the low-voltage DC power system. One example of the application is the “solid state power controller” in aircraft power distribution. Solid-state power controllers offer status outputs and permit external input logic control so that

they may be remotely located near to the load. The up-to-date products are available in 28V/80A[A4] and 15A/270V[A5] only.

The limited voltage / current ratings hinder the popularity of the solid-state circuit breaker in being deployed in the power transmission network. The higher power loss associated with the solid-state power device is another drawback.

However, there are some critical applications requiring high-speed current interruption capability, such as a solid-state rectifier in traction power systems.

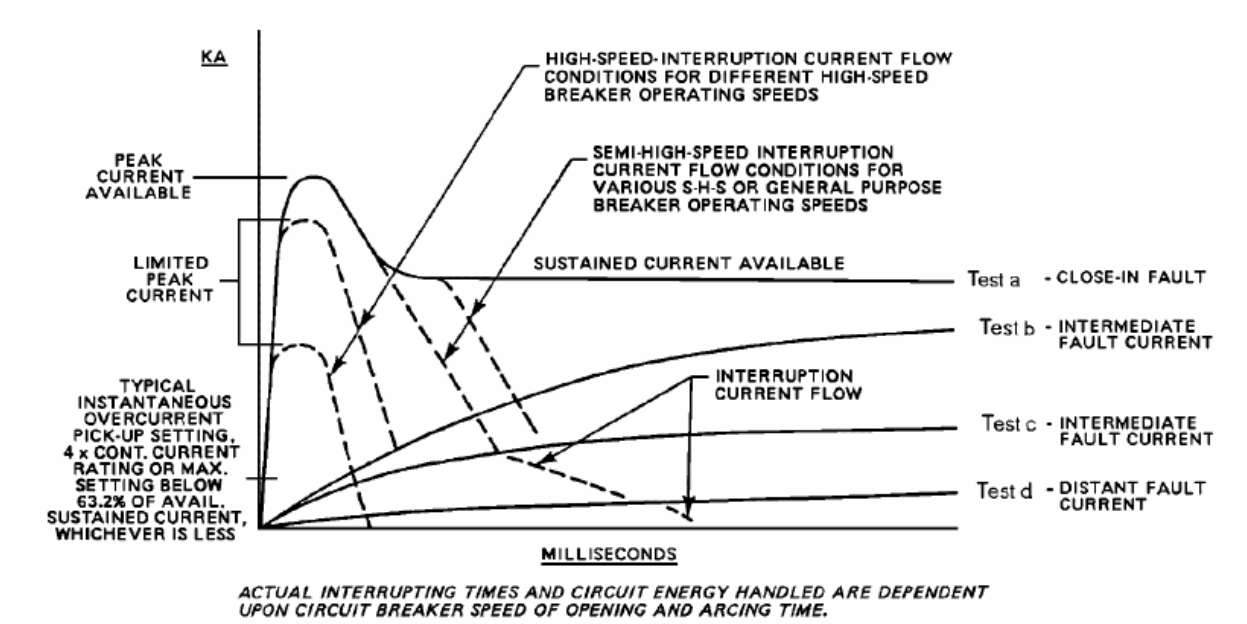


Figure 1-2 Representative circuit breaker characteristics for traction power systems [A6]

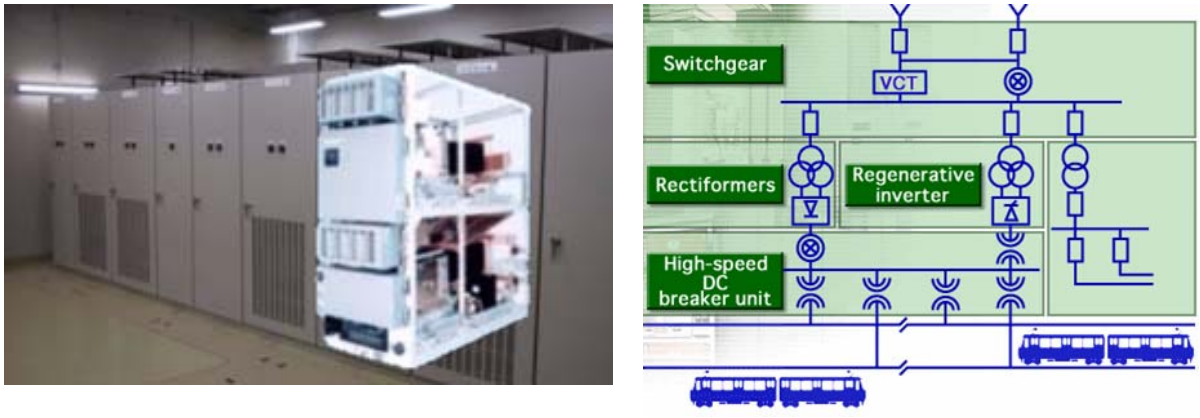
Figure 1-2 reflects the testing required for low-voltage DC solid-state circuit breaker [A7]. Test “a” is the close-in fault simulation with no intentional inductance or resistance added to the test circuit. The current rises to a maximum peak value in approximately one-half cycle of the

AC frequency and then decays to a sustained value of short-circuit current at the DC circuit breaker terminals. This sustained current is generally no more than 12 times the full-load current of the rectifier, with the peak current being no more than 1.65 times this value, occurring within 8 ms on a 60Hz AC source. The rate-of-rise of such a close-in fault is in excess of approximately $15\,A/\mu s$, with attenuation or elimination of the peak offset possible due to substation layout design or by the use of contributing rectifier inductance with or without DC reactors.

Tests "b," "c," and "d" are representative of the classic rate-of-rise curves normally associated with batteries, rotating equipment, and solid-state rectifiers. The rates of rise for these test circuits are low due to the increasing inductance in the circuit such as when representing the intermediate and distant fault conditions.

A high-speed circuit breaker that can respond quickly enough after the overcurrent trip device setting level is reached can part its contacts and build arc voltage in a sufficiently short amount of time so that the peak offset, test "a" in Figure 1-2, can be limited to a peak current appreciably less than the available (prospective) peak current.

Several solid-state circuit breakers are built to meet the high-speed, high-power requirement. A Gate Turn-Off (GTO) Thyristor-based 4160V, 2000A three-phase AC solid-state circuit breaker [A8] was built in 1993 for the US Army Pulse Power Center, which achieved 800μs opening time. A GTO DC circuit breaker (Figure 1-3) rated at 1500V-7500A is reported to have been used in Electric Traction PE system by Toshiba in 1999 with 1ms opening time.



(a)Toshiba GTO-CB (7500A,1500V, 1ms) (b)Traction Applications

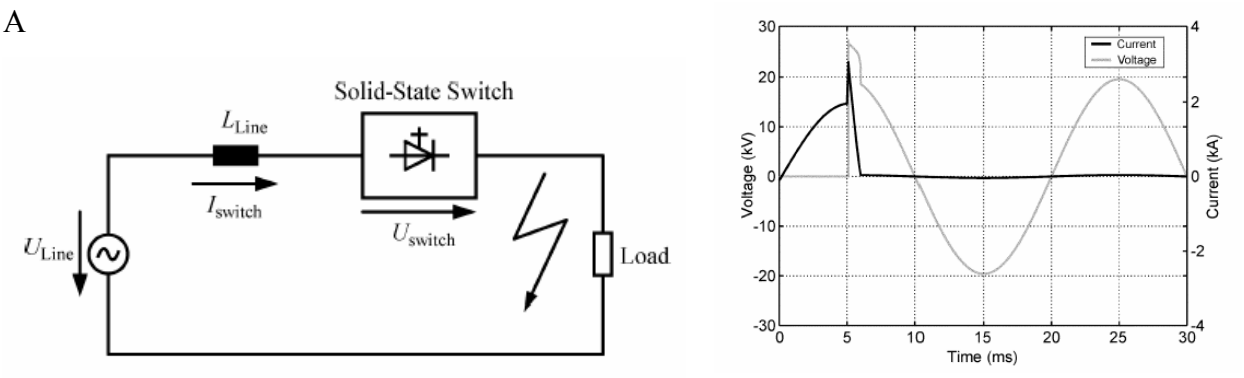
Figure 1-3 GTO DC circuit breaker for traction applications[A9]

With the aid of high-power GTO devices, a high-speed solid-state circuit breaker can achieve an opening time of several hundreds of microsecond, which is about two orders faster than a mechanical circuit breaker. With the new emerging power semiconductor switches such as the Integrated Gate Commutated Thyristor (IGCT) and Emitter Turn-Off (ETO) Thyristor, the solid-state circuit breaker speed can be further improved.

An IGCT-Based solid-state circuit breaker [A11] was studied for medium-voltage systems. The study indicated the solid-state circuit breaker can successfully interrupt the current within 100μs.

As shown in Figure 1-4 (a), a resistive load ground fault is simulated, the simulation results Figure 1-4 (b) indicate a fast current interruption.

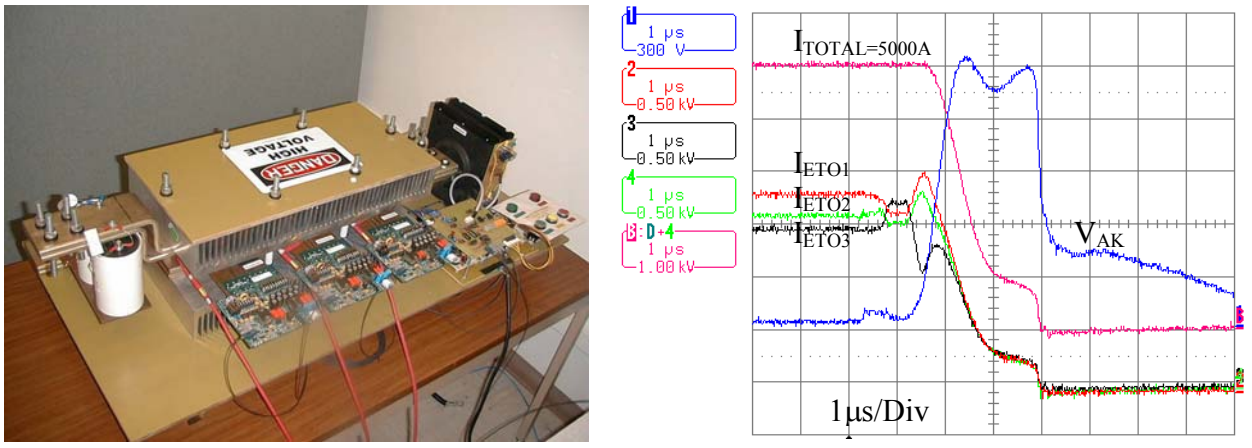
A



(a) GCT-CB(1800A, 9000V,<100us)　　(b) Simulation waveform

Figure 1-4 Solid-state circuit breaker for medium voltage systems [A11]

An ETO-based solid-state DC circuit breaker was developed at Center for Power Electronics Systems (CPES), Virginia Tech as part of this dissertation work. The solid-state circuit breaker uses three 4000A, 4500V ETO devices to achieve high-current interruption capability, which is shown in Figure 1-5 (a). The experimental results, as illustrated in Figure 1-5 (b), show that an ultra-high-speed of 5μs is achieved for a 5000A current interruption.



(a) ETO-CB(5000A, 2500V,5μs)　　(b) experimental waveform

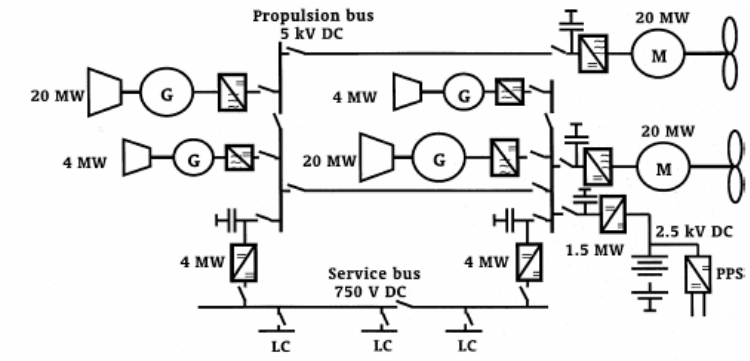
Figure 1-5 ETO-base 5000A solid-state circuit breaker

1.1.3 Hybrid Circuit Breaker

The mechanical circuit breaker generates an arc during current interruption which causes serious damage and erosion to the contacts. This leads to a shorter life time and the need for more maintenance. Developments in solid-state circuit breakers have led to switches with high-voltage breaking capabilities. Interruption is arcless and very fast. However a significant voltage drop in the on-state leads to high on-state losses. A mechanical switch shows a much lower on-state voltage, but interruption is difficult and lasts longer. A hybrid switch combines the advantages of the mechanical switch and the solid-state switch. The current is interrupted with a semiconductor. The mechanical switch is retained for low conduction losses. The combination shows a low on-state voltage and fast breaking, either arcless or with reduced arcing. Although the current interruption time is significantly reduced by eliminating or shortening the arc extinguishing phase, the hybrid circuit breaker interruption speed is fundamentally limited by the mechanical separation of the contacts.

A 600V / 6000A hybrid DC switch [A10] was developed for shipboard power systems by Ferreira in 2001. Six Eupec 1200A, 1600V IGBTs in parallel composes the solid-state switch. As shown in Figure 1-6 (a), the hybrid circuit breaker consists of the solid-state switch and the mechanical circuit breaker. The hybrid circuit breaker demonstrated current interruption time of 1.2ms.

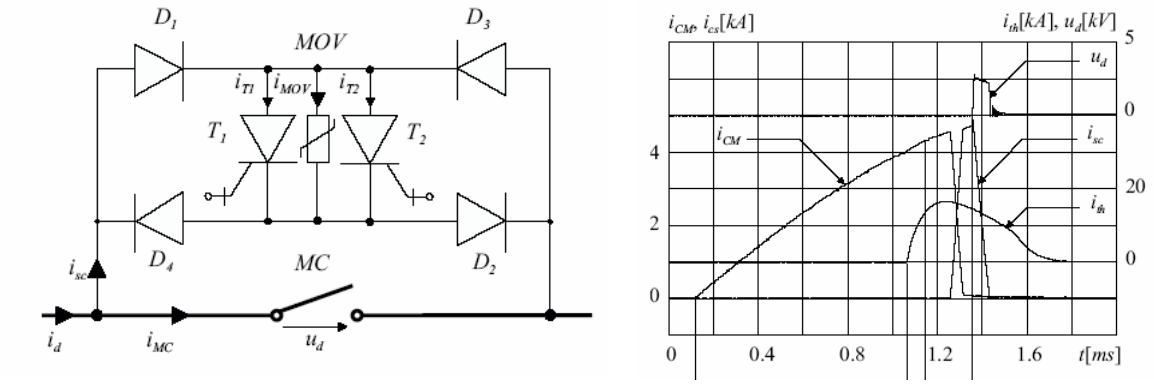
(a)Hybrid-CB (6000A,600V,1.2ms)



(b) Shipboard Power Systems

Figure 1-6 Hybrid DC switch for shipboard power systems [A10]

A 4000A, 1500V hybrid DC switch was demonstrated by Jean-Marc Meyer in 2000. Two 4.5kV IGCTs were used in the hybrid DC switch. Combined with the fast contact opening mechanical circuit breaker, a 0.75ms current interruption time was experimentally demonstrated as illustrated in Figure 1-7 (b).

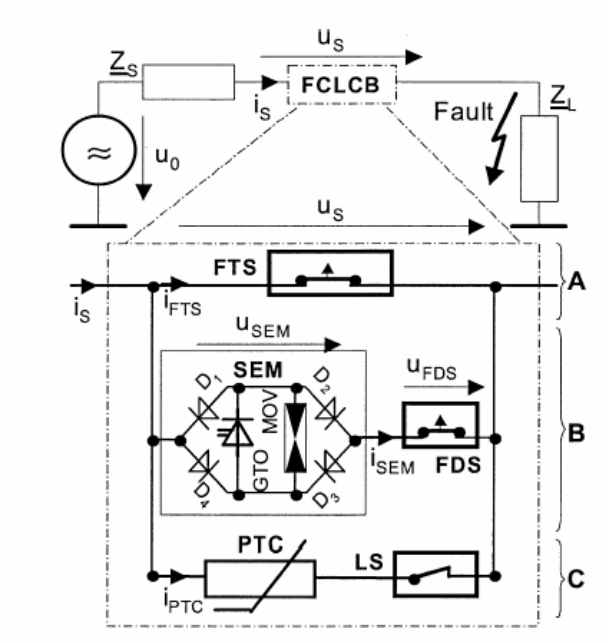


(a)Hybrid-CB (4000A,1500V,0.75ms)

(b) experimental results

Figure 1-7 Hybrid DC switch with ultra fast contact opening and IGCT[A12]

As discussed above, a mechanical circuit breaker is essential for the effective performance of the hybrid system. Its speed of operation determines how quickly after fault inception the current will be commutated to the solid-state circuit breaker. In [A13], Steurer integrated a fast-opening mechanical switch (100μs contacts separation) into the hybrid circuit breaker. It is concluded that the proposed method as shown in Figure 1-8 provides the basis for further development of a commercial hybrid current-limiting circuit breaker for medium-voltage systems.



Hybrid-CB(1000A,11000V)

Figure 1-8 Hybrid current-limiting circuit breaker for medium-voltage systems[A13]

In summary, a circuit breaker is widely used in power systems to protect the industrial equipment during fault / abnormal conditions.

Mechanical circuit breakers are dominantly used due to their full range of voltage / current ratings and low power loss. However, the current interruption time, which is about 20ms~60ms, is long. It generates severe arc during current interruption which causes serious damage to the contacts, thus demanding regular maintenance. All these disadvantages limit the use of a mechanical circuit in some critical applications, such as solid-state rectifiers, mining applications and so on. This is particularly true in DC systems where current normally can rise much faster than an AC system.

Solid-state circuit breakers offer fast response using modern power semiconductor devices. Their current interruption time varies from 5μs to 1000μs based on the different power semiconductor devices used. It generates no arc during current interruption and is hence maintenance-free. However, it has higher on-state conduction loss than a mechanical circuit breaker. The limited voltage / current ratings and high cost also hinder the popularity of the solid-state circuit breaker.

Hybrid circuit breakers combine the low on-state voltage drop of a mechanical circuit breaker and the arcless current interruption of a solid-state circuit breaker. However, the current interruption response time (about 1ms~10ms) is poorer than the solid-state circuit breaker.

Table 1-1 compares the different features of the aforementioned circuit breakers.

Table 1-1 Comparison of different circuit breaker features

	Mechanical Circuit Breaker	Solid-State Circuit Breaker	Hybrid Circuit Breaker
Response time	20~60ms	5μs~1000μs	1ms~10ms

Voltage/current rating	Full	Limited	Limited
Power loss	Low	High	Low
Arc	Yes	No	No
Maintenance required	Yes	No	No

The state-of-the-art circuit breakers are classified based on the power rating and response time which is shown in Figure 1-9. The mechanical circuit breaker is commercially available from various vendors like ABB, Siemens, GE, Westinghouse and so on. Solid-state circuit breaker and hybrid circuit breaker are under intensive investigation. The solid-state circuit breaker extends the response time to a sub-cycle range which is conventionally not protected by mechanical circuit breakers.

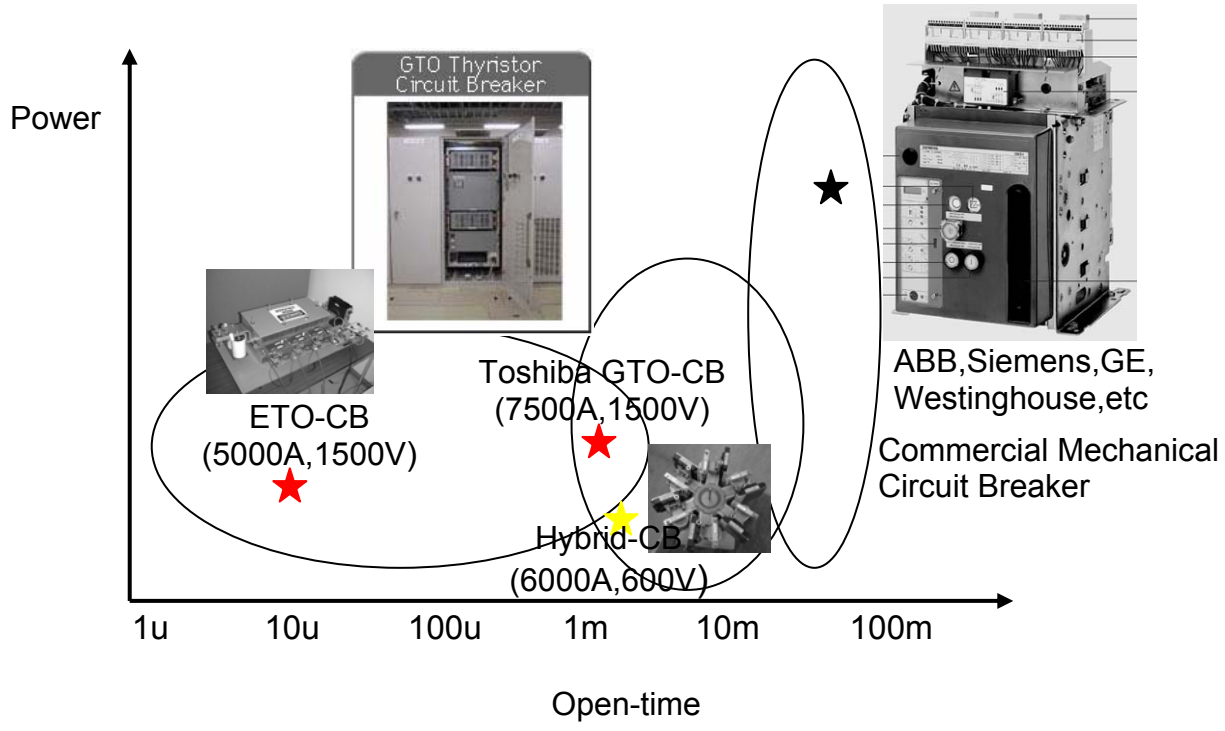


Figure 1-9 State-of-the-art circuit breaker

1.2 Research Significances

It is the objective of this study to develop a novel, high-speed, high-current solid-state circuit breaker in a mining trolley system.

The design specifications for the solid-state circuit breaker application are shown in the Time-Current-Characteristics (TCC) curve in Figure 1-10. The black curve and the blue curve represent the TCC of the example transformer and rectifier, which is protected by the solid-state circuit breaker in this graph.

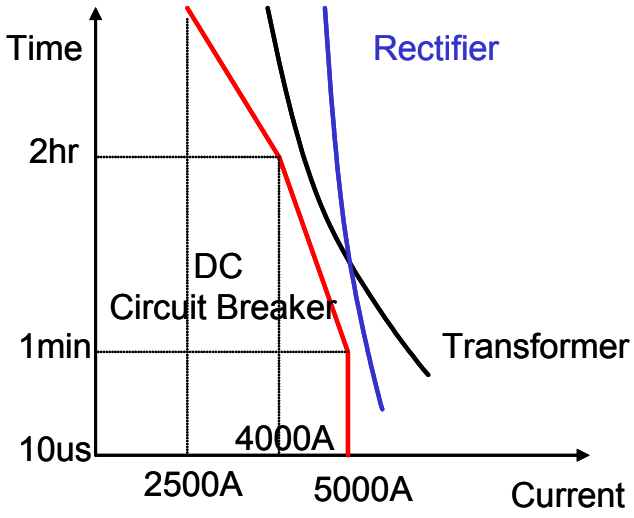


Figure 1-10 Design specifications

The rated DC voltage of the solid-state circuit breaker is 2500V, and the rated current is 2500A, with 150% overload operation for 2 hours or 200% overcurrent operation for 1 minute.

The key component in the solid-state circuit breaker is the high-current DC switch module that can also be classified as a high-power Integrated Power Electronics Module (IPEM) [A17]. Hence the research further extends our knowledge base on IPEM to much higher power levels.

Applying the high-power IPEM as a solid-state circuit breaker is also very significant because the high-speed provides fast-acting protection for industrial equipment, hence having significant impact on the power systems.

1.2.1 Development of High-Power Integrated Power Electronics Module (IPEM)

The integrated power electronics module (IPEM) is envisioned to be the driver for the next-generation power electronics industry. The envisioned integrated power electronics solution is based on advanced packaging of new generation of devices and innovative circuits and functions in the form of building blocks with integrated functionality, standardized interfaces, suitability for automated manufacturing and mass production, and application versatility, namely IPEMs, and the integration of these building blocks into application-specific systems solutions[A17].

The design specifications require a high-power IPEM with the following ratings:

DC voltage	2500V
Blocking voltage	4500V
DC current	2500A
Overload current for 2 hours	4000A
Overload current for 1 minute	5000A
Maximum turn-off current	12000A
Cooling	25^{o}C air-cooling

A switch-diode pair with an auxiliary spike suppression circuit is defined as the high-power IPEM in a typical DC system, which is shown in Figure 1-11.

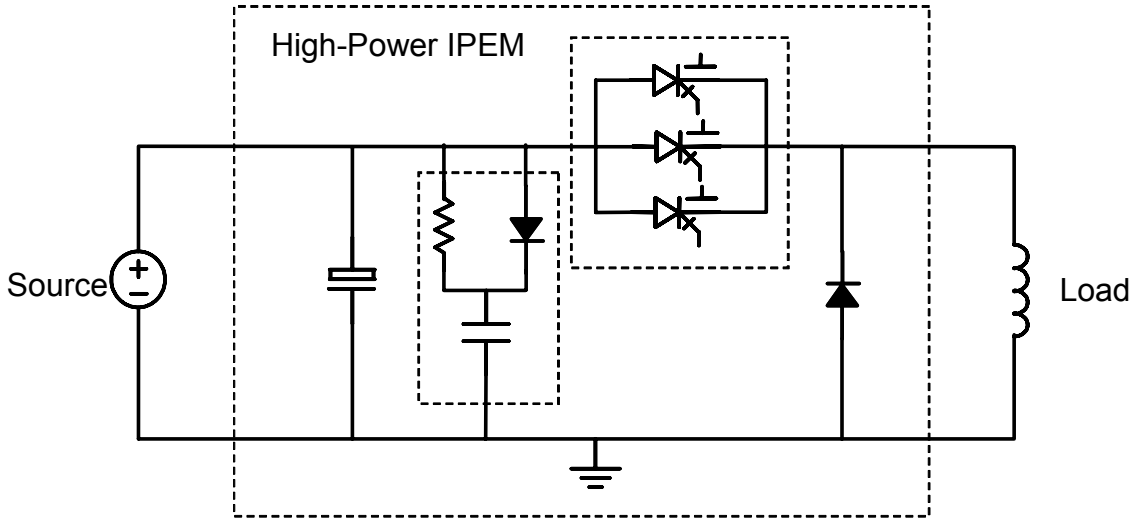


Figure 1-11 Identified high-power IPEM in a typical DC system

There is no single state-of-the-art power semiconductor device that meets the stringent current requirements. Hence, multiple devices in parallel are required. The current sharing issue in parallel devices is studied in the high-power IPEM. A physics-based device model is developed and used throughout this study. During the high-speed, high-current interruption, the high di/dt generates a high voltage spike, and parasitic modeling plays an important role in the module design. The electro-thermal model of the DC switch module and the heatsink subsystem is used to identify the "thermal runaway" phenomenon in the module that is caused by the negative temperature coefficient of selected power device. These issues and their solutions form the main focus of this study as shown in Figure 1-12.

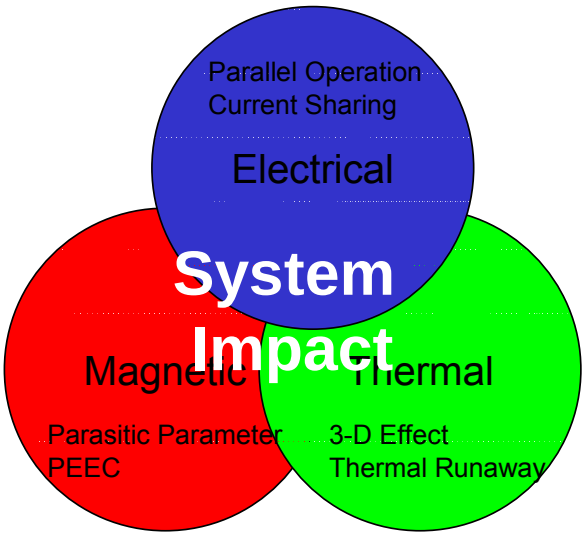


Figure 1-12 Research issues

1.2.1.1 ELECTRICAL ANALYSIS OF HIGH-POWER IPEM

1.2.1.1.1 STATE-OF-THE-ART HIGH POWER SEMICONDUCTOR DEVICE

According to the design requirements, the selected semiconductor devices should have the following features: high turn-off capability with or without snubbers, fast switching speed and low conduction loss, wide Safe Operation Area (SOA) and easy control. Based on the detailed device survey, three types of high-power hard-switching devices are available and have the potential to be used in the 4.5kV/5kA high-power IPEM. They are the Insulated Gate-Commutated Thyristor (IGCT) [A19] [A20], high-voltage Isolated Gate Bipolar Transistor (IGBT) [A21][A22] and the Emitter Turn-Off (ETO) thyristor [B1]. The state-of-the-art power semiconductor devices are shown in Figure 1-13. The characteristics of these devices are reviewed briefly in the following sections.

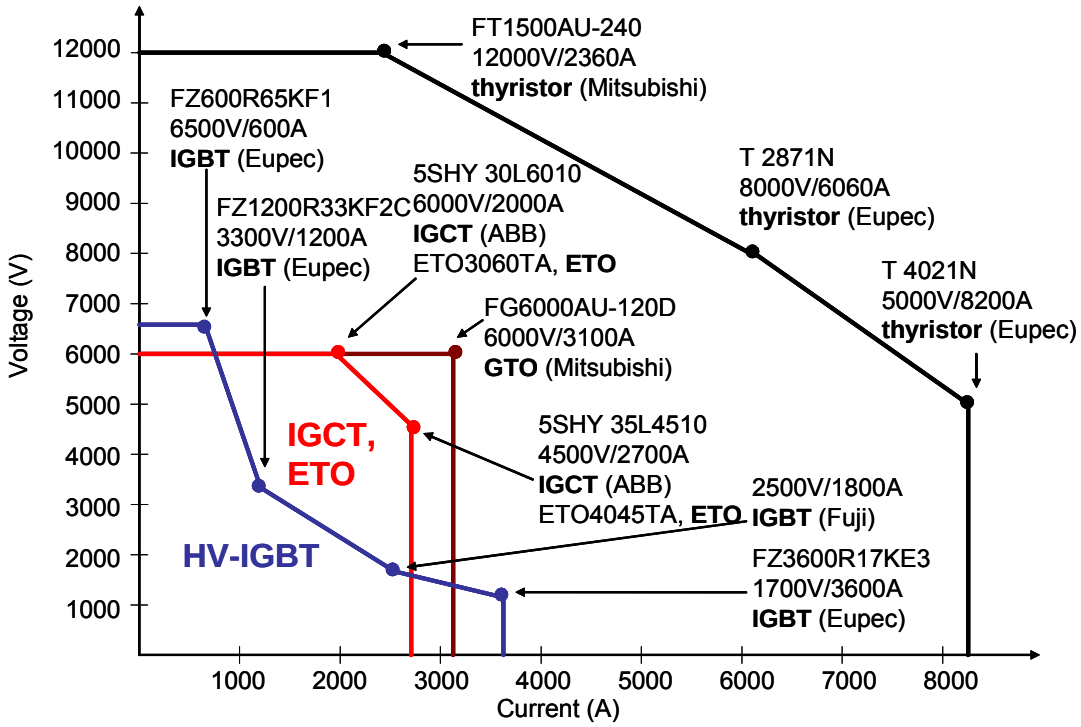


Figure 1-13 State-of-the-art high power semiconductor devices

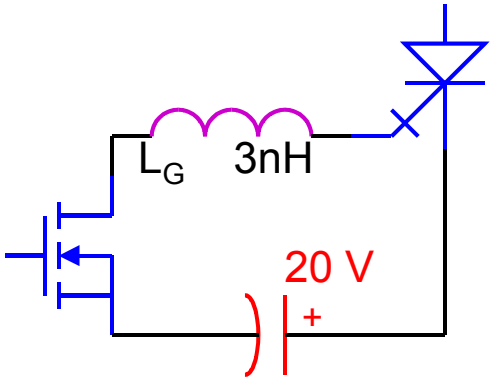
Integrated Gate Commutated Thyristor (IGCT)

IGCT is a Gate Turn-Off (GTO) thyristor based high-power device developed by ABB and Mitsubishi [A19] [A20]. Compared with a GTO, the IGCT has a faster switching speed and snubberless turn-off capability. For IGCTs, which are widely used in voltage source converters, typical device ratings are 4.5~5.5kV blocking voltage with 280~4000A turn-off capability. IGCTs with higher ratings [A20] and a higher speed will be developed in the near future.

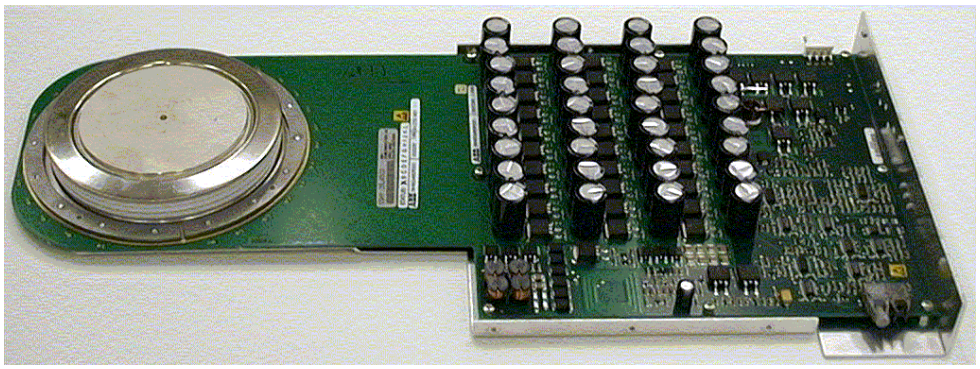
Due to their fast switching speed and the ability to be used in parallel and series, IGCTs have great advantages compared with the GTO. In the IGCT, press-pack packaging is used. Due to

better tolerance for thermal cycling and being explosion-free under fault conditions, the press-pack device has higher reliability. Furthermore, the press-pack makes double-side cooling possible, which increases the IGCT's thermal handling capability. On the other hand, the press-pack device requires the external mechanical clamp for mounting and relay on the coolant to insulate among the press-pack heatsinks.

For comparison purpose, the 4kA, 4.5kV IGCT from ABB (5SHY 35L4503) has been characterized and compared with other devices since it offers a better trade-off between conduction loss and switching loss. Limited by the switching loss and gate driver loss, the switching frequency of the IGCT is usually below 1kHz. The equivalent circuit and a picture of the chosen IGCT is shown in Figure 1-14. The tested forward I-V curve and the snubberless turn-off waveforms and losses of the 4kA, 4.5kV IGCT under 2kV DC bus voltage are shown in Figure 1-15 and Figure 1-16.



(a) Equivalent circuit



(b) Picture of the ABB 4kA, 4.5kV IGCT

Figure 1-14 ABB IGCT equivalent circuit and picture

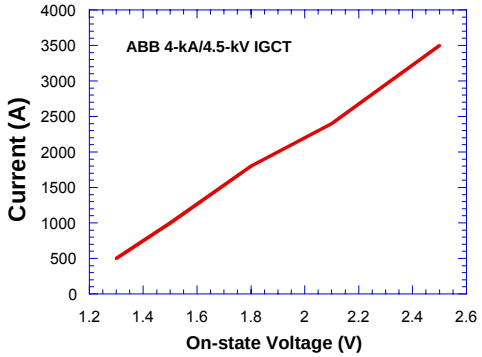
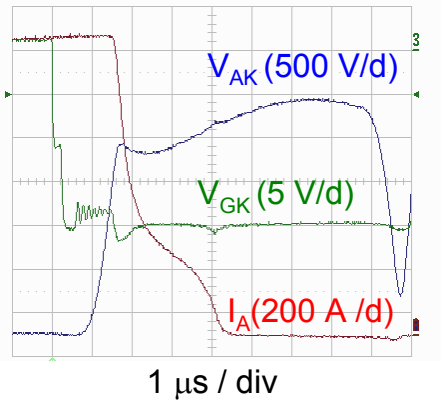
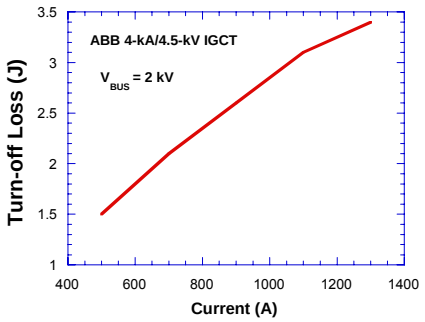


Figure 1-15 IGCT (5SHY35L4503) I-V characteristics



(a) Snubberless turn-off waveforms



(b) Turn-off losses of the 4kA, 4.5kV IGCT

Figure 1-16 IGCT (5SHY35L4503) snubberless turn-off waveform and turn-off losses

High-voltage IGBT

The IGBT is a monolithic MOS-gated power device that controls the bipolar current conduction with an insulated MOS gate as shown in Figure 1-17. The conductivity modulation results in higher forward conduction current capability than a power MOSFET. Because of the MOS gate control, the gate drive power is very low since only a voltage signal is needed to charge and discharge the IGBT's input capacitance. After turn-off, the IGBT behaves like a rugged open-base PNP transistor with uniform current and thermal distribution and so the IGBT has an excellent turn-off SOA. Due to the physics of combined MOS/bipolar current conduction, the IGBT also has a transistor-like, voltage-controlled output characteristic (hence the FBSOA) that can be used to limit the turn-on di/dt as well as the maximum current under short circuit condition. All these features have contributed to the IGBT gaining wide application in power electronics systems since its commercial introduction in 1988.

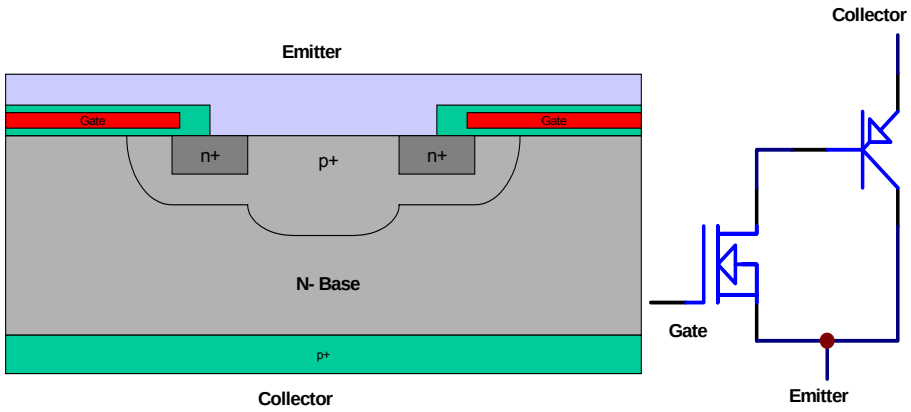


Figure 1-17 IGBT structure and equivalent circuit.

Based on Very Large Scale Integration (VLSI) technology, the cell size as well as the die of the IGBT is much smaller than the IGCT. Due to the yield limitation of the MOS gate technology, the IGBT's maximum chip size is limited to 2.6 cm^2 and so the single die IGBT's current handling capability is limited to 100A. IGBTs with higher current ratings are formed by paralleling many small IGBTs in a single housing (plastic box). Each IGBT chip is covered by a very thin aluminum metallization to which the aluminum wires can be bonded to make connections. The housing of the IGBT module is usually filled with silicon gel to protect the wire bond soldering. To provide the internal insulation between IGBT chips and the copper base plate, the IGBT chips are soldered on a Direct Bonded Copper (DBC) substrate that consists of a ceramic layer and two copper layers. To ensure uniform current sharing among the paralleled IGBTs, the chips with narrow parameters' distribution and positive temperature coefficient of the on-state voltage are preferred.

Today, 600V, 1200V, 1700V, 2500V and 3300V IGBTs with current ratings up to 2400A are commercially available. A 6500V IGBT with currents up to 600A is also being introduced by EUPEC, as shown in Figure 1-18 (a) [A21]. To improve the long-term reliability, ABB and Mitsubishi are also developing press pack IGBTs without wire bonds, as shown in Figure 1-18 (b) [A23]. The press-pack IGBTs are expected to be on the market soon.

(a) 600A/6.5kV IGBT module

(b) 700A/2.5kV press pack IGBT

Figure 1-18 Pictures of EUPEC IGBT module and ABB press-pack IGBT.

The 600A, 6.5kV IGBT has been characterized and compared with other devices. There are 24 IGBT chips, 12 fast diode chips and 24 gate resistance chips inside the IGBT module. The 600A, 6.5kV IGBT is optimized for operation at switching frequencies from 500 to 1000Hz that are typical for high-voltage traction applications. The on-state voltage of the 600A, 6500V IGBT is shown in Figure 1-19.

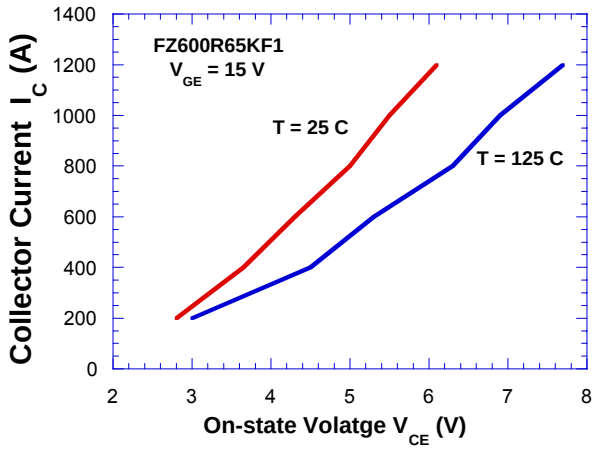


Figure 1-19 IGBT (FZ600R65KF1) I-V characteristics

Since the IGBT acts as a voltage-controlled current source during the turn-on transient, the turn-on di/dt can be controlled by the gate drive instead of the passive di/dt snubber as in the case of IGCT or ETO. By adjusting the gate resistance, the switching time, current rise rate di_C/dt and voltage deceasing rate dv_C/dt can be controlled according to safe operation requirements of the turn-off diode.

Since the IGBT behaves like an open-base PNP transistor after the turn-off of the internal MOSFET, the IGBT has a very good RBSOA and snubberless turn-off capability. There is a small current tail after the main current fall, which is a typical characteristic of the IGBT. The snubberless turn-off losses of the 600A, 6.5kV IGBT are shown in Figure 1-20.

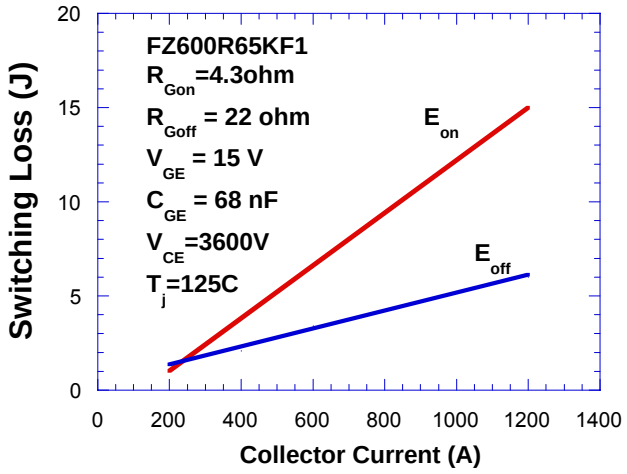


Figure 1-20 IGBT (FZ600R65KF1) snubberless turn-off losses

Since the IGBT has only one MOS gate to control, the gate drive power is very low and even a small commercial DC/DC modules can be directly used to provide the required gate drive power. Therefore, the IGBT gate driver is very compact and can be easily mounted on the package housing. Due to the excellent RBSOA and FBSOA, the di_C/dt and dv_C/dt can be controlled through the gate drive during switching transients. In the case of an internal or external short circuit, the IGBT can limit the maximum collector current to about 3 times the rated current and operate in the active region instead of the saturation region for a short period (about 10 μs). Once over-current is detected through monitoring the collector voltage during the on-state, the IGBT can be turned off safely due to its fast switching speed.

For the IGBT module, the paralleled IGBT chips are housed in a plastic box with collector and emitter terminals conveniently located for a laminated bus-bar connection. Since the

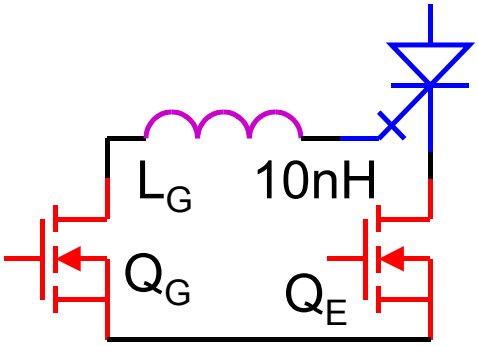
terminals are isolated from the baseplate, the IGBT module is very easy to use and can be directly mounted on the heatsink without external mechanical clamp as with the IGCT. Even though only single-side cooling is possible, low thermal impedance is still achieved due to the large IGBT chip area as well as large baseplate. However, there are some reliability concerns about the wirebonds-based IGBT module. First, the reliability of the aluminum wire as well as the wire-bond solder point is a major concern due to the thermal mismatch. Second, the increase of the thermal resistance is another reliability concern because of the degradation of the internal thermal contact and the relocation of the thermal contact grease. Furthermore, the durability of the internal insulator between the IGBT chips and baseplate is an important factor of the reliability since the baseplate of the IGBT module is isolated. In the high-voltage applications with series-connected IGBTs, the isolation become a big issue since the isolation voltage cannot be easily increased without a major cost increase. Last, once the IGBT fails due to the overcurrent, all the available energy will be dumped to the failure device and probably cause explosion. The IGBT can be open-circuit after failure and this is a very dangerous situation, especially in the applications with series-connected devices or multilevel converters. The press pack IGBTs under development may overcome these disadvantages in the near future.

Emitter Turn-Off thyristor (ETO)

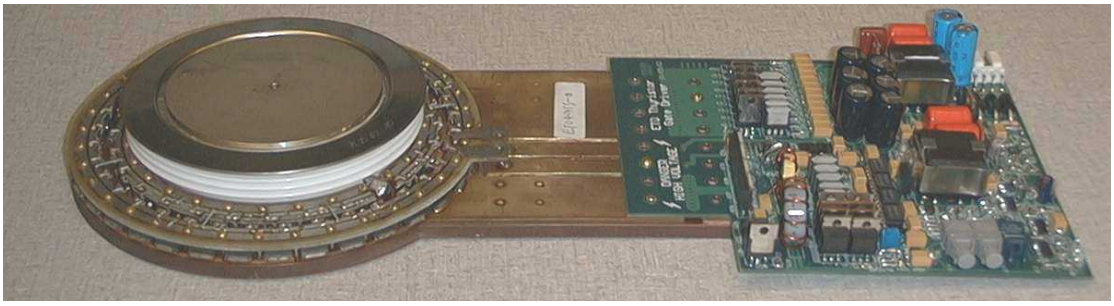
The ETO is a new type of the GTO-based high-power hard-switching device developed at CPES, Virginia Tech [B1]-[B9]. An ETO is realized using a conventional GTO in series with an emitter switch Q_E (paralleled low-voltage high-current MOSFETs). The gate switch Q_G is also

connected to the GTO's gate, as shown in Figure 1-21. The ETO in many ways is similar to the IGCT; it also uses the press-pack technology. It has a similar switching speed to an IGCT as well as snubberless turn-off capability. The major advantage of the ETO over IGCT is its lower cost and lower control power.

For the purpose of comparison, a 4kA, 4.5kV ETO 4045TA has been characterized. A low-conduction-loss 4kA, 4.5kV GTO from ABB (5SGT 40L4502) is used to construct the ETO4045TA. Figure 1-22 and Figure 1-23 show typical performance of the ETO4045TA.



(a) Equivalent circuit of ETO



(b) Picture of 4kA, 4.5kV ETO

Figure 1-21 ETO equivalent circuit and picture

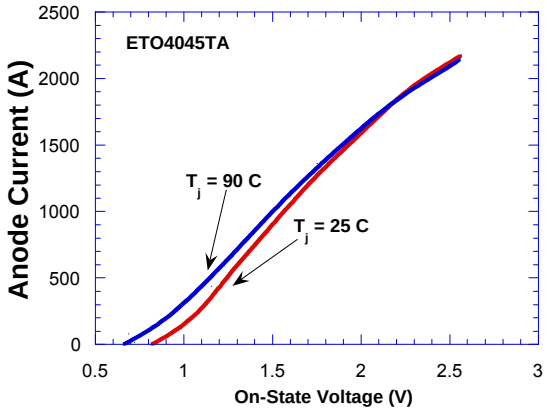


Figure 1-22 ETO (ETO4045TA) I-V characteristics

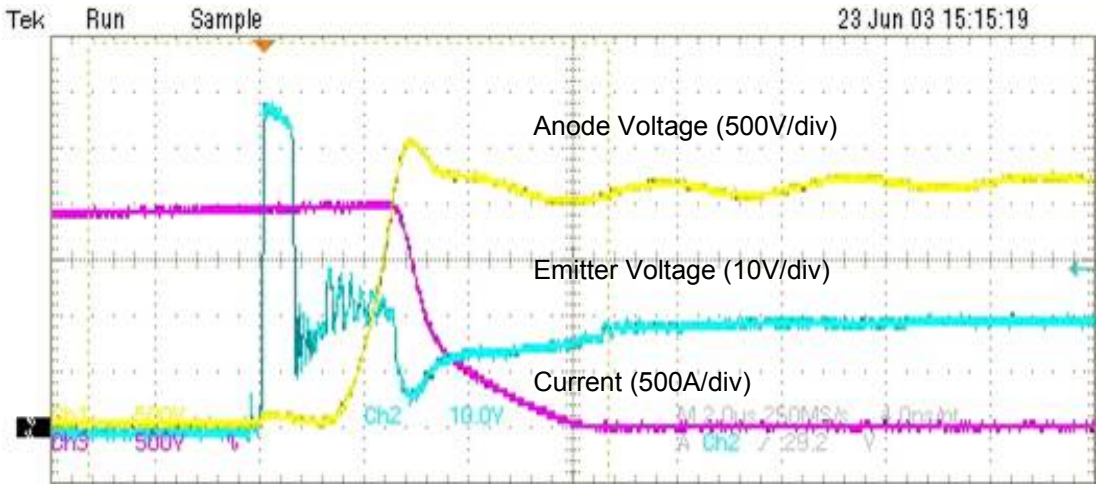


Figure 1-23 ETO (ETO4045TA) snubberless turn-off waveforms

1.2.1.1.2 DEVICE COMPARISON AND SELECTION

The characteristics of the three high-power devices have been characterized and shown previously in terms of conduction voltage drop and turn-off loss. According to the test results,

the IGBT has the lowest turn-off switching loss but the highest conduction loss. Compared with the IGCT, the ETO has the roughly same conduction loss and switching loss. The important characteristics of these devices are tabulated in Table 1-2.

Compared with the IGCT and the ETO, the IGBT offers the lowest turn-off loss and gate drive power. The limitation is its high conduction loss and long-term reliability related to the wire-bonds-based packaging. The IGCT has low conduction loss. Its drawback is the high gate drive power, especially in the higher switching frequency case. The ETO offers similar conduction loss with minimum driving power. The ETO is selected for its low conduction loss and easy scalability which will be discussed in the following chapters.

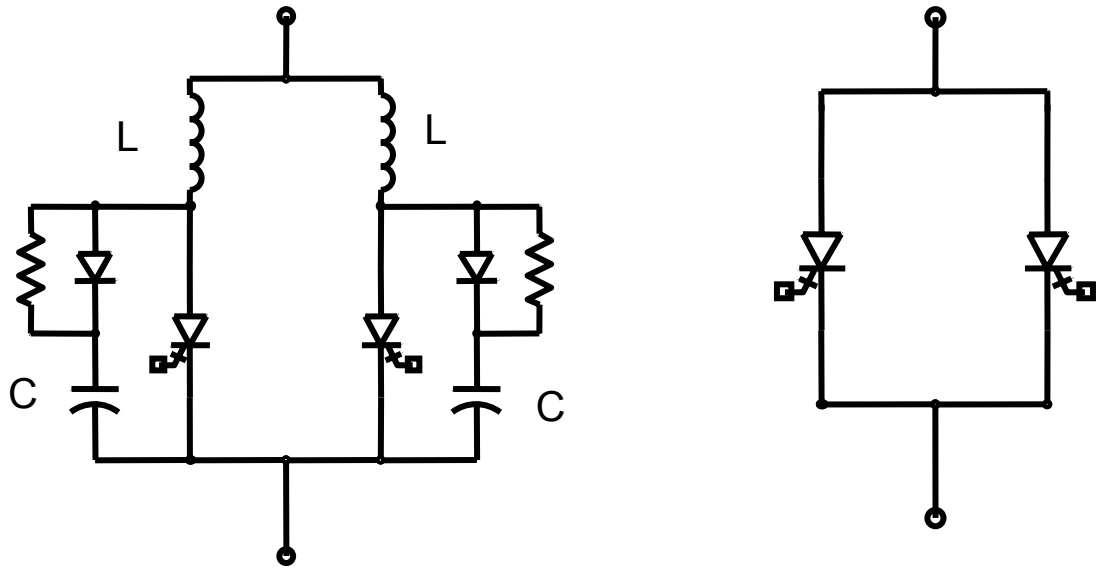
Table 1-2 Characteristics comparison among IGCT, ETO and IGBT

Metrics	**ETO3060TA**	**ETO4045TA**	**IGCT 5SHY35L 4503**	**IGCT 5SHX19L6004**	**IGBT FZ600R65KF1**	**IGBT FZ1200R33KF2**	**IGBT FZ2400R 17KF6B2**
$V_{blocking}$ (V)	6000	4500	4500	5500	6500	3300	1700
V_{DClink} (V)	3800	2800	2800	3300	#3600	#1800	#900
$I_{max}@V_{dclink}$ (A)	3000	4000	4000	1800	1200	2400	4800
On-State Voltage (V)	2.8 (125ºC, 1500A)	1.921 (125ºC, 1500A)	1.788 (125ºC, 1500A)	2.7 (125ºC, 1500A)	5.84 (125ºC, 750A)	4.78 (125ºC, 1500A)	2.43 (125ºC, 1500A)
Turn-On Loss * (J)	–	–	–	–	9.0 (125ºC, 3.6kV, 800A)	2.0 (125ºC, 1.8kV, 800A)	0.19 (125ºC, 0.9kV, 800A)
Turn-Off Loss (J)	4.8 (125ºC, 3.3kV, 800A)	4.8 (125ºC, 2kV, 800A)	4.2 (125ºC, 2.2kV, 800A)	4.5 (115ºC, 3.3kV, 800A)	4.0 (125ºC, 3.6kV, 800A)	1.2 (125ºC, 1.8kV, 800A)	0.35 (125ºC, 0.9kV, 800A)
Thermal Resistance R_{thjc} (K/W)	0.013	0.012	0.012	0.021	0.011	0.0085	0.007

1.2.1.1.3 IMPROVED ETO THYRISTOR FOR HIGH-POWER IPEM

As mentioned above, the Emitter Turn-Off (ETO) thyristor is selected for its low conduction loss and easy scalability (easy parallel and series performance). The ETO device properties are fully characterized in this study. Firstly, a physics-based device model is developed using lumped-charge method. This model uses the basic doping profile and semiconductor geometry parameters only; it calculates the internal minority carrier charge concentration and exhibits as an external voltage and current signals. The model is very convenient for the analysis of the device dynamics. It also reveals the intrinsic physics of operation during steady state and transient. The model is then verified by experimental results. It is further used to study the high-power IPEM in which multiple ETOs are in parallel. Device parallel operation is a major issue in the development of the high-power IPEM, particularly when very high current is needed. Since each ETO device has a DC current rating around 1750A, a 5000A class DC switch will require three ETOs in parallel operation. The thyristor-type of devices, such as the GTO exhibits a latch-up mechanism during conduction, meaning that the device current can rise very quickly when device voltage increases or there is an increase of temperature. The impact for parallel operation is that one device can easily see a much higher dynamic current than the others causing device failure due to the exceeding of the maximum turnoff capability of the individual device. These current-crowding phenomena limit the devices parallel operation. For slower power semiconductor devices such as the GTO, this is particularly a problem and it often requires a current-sharing inductor between paralleled devices, as shown in Figure 1-24 (a). The ETO improves the switching delay time by a factor of ten compared with the GTO, hence the current crowding issue is significantly improved. A novel series of ETO devices, so-called DirectETOs,

are further developed under this study which further improve the parallel operation performance of the conventional ETO devices. It enables the simplified connection of the devices to extend the current capacity, as shown in Figure 1-24 (b). With the aid of the developed device model, device parallel operation is intensively investigated. The improved DirectETO facilitates the parallel operation of multiple devices, and hence a 5000A high-power IPEM is developed.



(a) Conventional devices in parallel operation (b) DirectETO devices in parallel operation

Figure 1-24 DirectETO facilitates the use of devices in parallel operation

1.2.1.2 MAGNETIC ANALYSIS OF HIGH-POWER IPEM

The high-power IPEM is usually bulky. It often requires safety clearance and imposes mechanical constraints on the design. Meanwhile, the high-power IPEM has high voltage and

high current ratings. It exerts high stress on the device during the fast switching transient. For the proposed high-power IPEM, the concern is the high parasitic inductance and its impact to the device stress. Hence accurate parasitic modeling is another important issue in the design of the high-power IPEM. Using the Partial Element Equivalent Circuit (PEEC) method, the parasitic parameter can be easily extracted. This method is widely used to analyze the IC interconnections in the Very Large Scale Integrated (VLSI) circuits. This method is applied in the high-power IPEM design. It is also verified by Finite Element Analysis (FEA) simulation. The parasitics are extracted and used to evaluate the different IPEM structural designs. Combined with the developed device modeling, the device circuit interaction is conducted in a circuit simulator. The low device stress reflects the improved structural design.

1.2.1.3 THERMAL ANALYSIS OF HIGH-POWER IPEM

The high-power IPEM generates large power losses, and therefore thermal management is critical for the successful design of the high-power IPEM. The sparse distributed thermal source requires 3D effects taken into consideration. Considering the forced convection, Computational Fluid Dynamics (CFD) method is used in the thermal modeling and simulation. Thermal coupling and thermal de-coupling effects are compared in the design. Combined with the developed device model, electro-thermal simulation is conducted to investigate the "thermal runaway" phenomenon in the high-power IPEM. The thermal electrical model is also used to calculate the DC and transient thermal limit of the high-power IPEM.

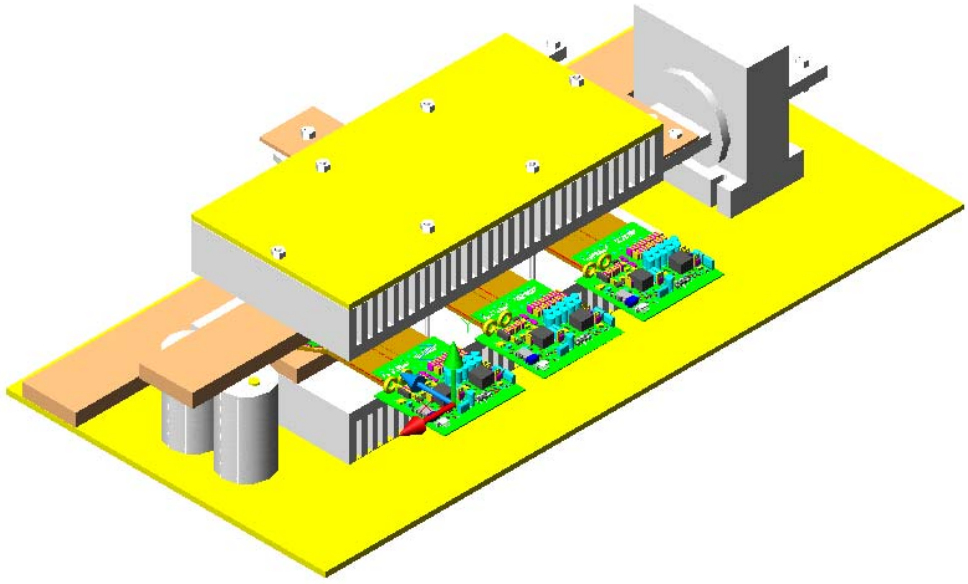


Figure 1-25 Conceptual drawing of the high-power IPEM

A 5000A high-power IPEM is designed using three of the improved "DirectETO" devices in parallel. The improved structural design reduces the parasitic inductance, which limits the device stress to a safe value at rated 2500V DC voltage. The improved thermal design increases the system thermal stability and enables the DC 2500A current with transient 5000A one-minute overload capability.

The conceptual drawing of the designed high-power IPEM is shown in Figure 1-25. Three DirectETOs are clamped by two back-to-back heatsinks. Two copper bars are used as the electrical conductors as well as heat spreaders. A voltage clamping circuit as well as an external sensor is integrated in the high-power IPEM.

1.2.2 Novel Solid-State DC Circuit Breaker Utilizing High-Power IPEM

Using the developed high-power IPEM, a novel solid-state DC circuit breaker has been demonstrated. A 5000A current interruption was experimentally demonstrated within 5 microseconds in the lab. It is the first of its kind to be demonstrated; a high-speed, high-current solid-state DC circuit breaker. After the delivery of the solid-state circuit breaker to the sponsor, it was installed in the field for testing purpose. It is commissioned for 12 months continuously as of July 2005 and has successfully tripped during several fault conditions.

The high-power IPEM can be also be used in other types of power electronics apparatus, such as solid-state AC circuit breakers, fault current limiters, transfer switches, converter applications.

1.2.3 High-Speed Solid-State DC Circuit Breaker Enables Power Systems Protection Paradigm Shift

The system impacts of the high-speed solid-state DC circuit breaker were studied, and using EMTDC software, the power systems response was simulated. The high-speed circuit breaker mitigates voltage sag during fault conditions without affecting the power system stability. The other advantages of the high-speed solid-state circuit breaker include: limiting fault current to maximum tripping level; enabling the interconnection of the distributed generation (DG); increasing the availability by seamless transfer switch and so on.

Traditionally, a mechanical circuit breaker is deployed to protect the industrial equipment in power systems, as shown in Figure 1-26. As power electronics apparatuses are increasingly

accepted in power systems, they demand fast-acting protection devices, which are shown in Figure 1-27. The emergence of a high-speed solid-state circuit breaker enables such a paradigm shift in the power system protection scheme.

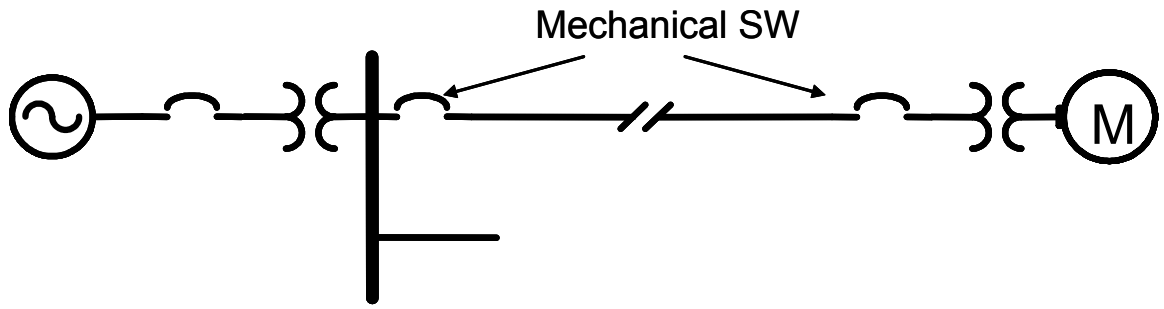


Figure 1-26 Mechanical circuit breaker in traditional power systems

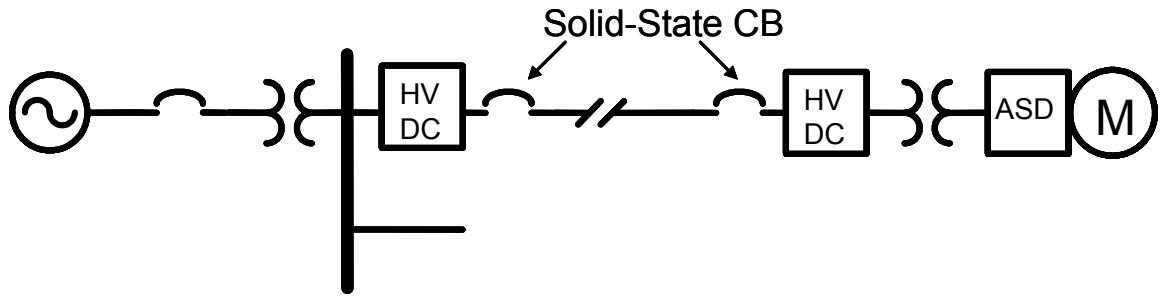


Figure 1-27 Solid-state circuit breaker in modern power systems

1.3 Dissertation Outlines

The dissertation is organized as follows, with the introduction, which explains the objectives of the dissertation by detailed survey and identified research issues. A high-power IPEM is analyzed from electrical, magnetic and thermal aspects. The high-power IPEM is then

demonstrated in a solid-state DC circuit breaker. Finally, the high-speed solid-state circuit breaker impact on the power system is discussed.

Chapter 2 describes a firstly developed physics-based model for the emitter turn-off (ETO) devices.

The parallel operation of emitter turn-off (ETO) thyristors is analyzed in Chapter 3, followed by detailed modeling and simulation, improved performance is achieved in Chapter 4.

Chapter 5 looks into the electro-magnetic modeling of the high-power integrated power electronics module.

The electro-thermal aspect of the high-power integrated power electronics module is given in Chapter 6.

Chapter 7 describes the utilization of the high-power integrated power electronics module in a novel solid-state DC circuit breaker.

Finally, conclusions are drawn in Chapter 8.

Moreover, the potential system impact of the high-speed solid-state circuit breaker is discussed in the Appendix.

Chapter 2.
Physics-based Model for Emitter Turn-Off Thyristor (ETO)

2.1 Introduction

The Emitter Turn-Off (ETO) [B1][B7] thyristor shown in Figure 2-1 is a hybrid MOS-gated thyristor, which has the high power capability of the Gate Turn-Off (GTO) thyristor and the voltage-controlled gate connections of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It improves on the switching dynamics of GTO devices and has been successfully demonstrated in several high-frequency, high-power applications, such as static compensators (STATCOM) [B10] and motor drives.

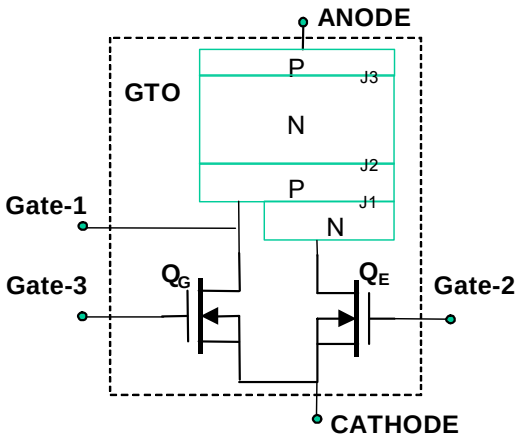


Figure 2-1 ETO equivalent circuit diagram

There is a strong need of a compact ETO circuit model for application engineers, which is capable of representing the physics mechanism of the novel power semiconductor devices and would facilitate the application design process.

Device modeling techniques generally involve analysis of the Ambipolar Diffusion Equation (ADE) which governs the carrier transportation for the bipolar power semiconductor devices. Eq. 2-1 is the typical description of the well-known ADE, where the D is the carrier diffusivity, and τ is the carrier lifetime. The carrier concentration p(x, t) is a function of the location and time.

$$\frac{\partial p}{\partial t} = D \cdot \frac{\partial p}{\partial x^2} + \frac{p}{\tau} \qquad \text{Eq. 2-1}$$

A typical software package, such as Medici [A26], solves Poisson's equation and both the electron and hole current continuity equations to analyze devices such as diodes and bipolar transistors using FEA. It generates thousands of nodes insider the device layer, and it takes hours to find the solution for all the nodes, even when using a high-end workstation. This method gives an insight into the device physics; it is widely used by device engineers for novel device development and device optimization. But the limited mixed-mode simulation (in other words the device circuit interface) and time-consuming process hinders its acceptance by the circuit engineers.

A lumped-charge modeling technique [C1][C6] was proposed by C.L, Ma and P. Lauritzen in 1990s. It collapses the excessive internal nodes in one distinctive physical layer into one charge storage node and up to two connection nodes. The charge storage node is responsible for the charge carrier storage and recombination; while connection nodes are located at junction depletion edges to connect junction voltage to charge variables. In this way, it significantly reduces the calculation while maintains the modest accuracy. It is therefore widely accepted, and lots of device models are developed using this method. A diode model [C12] [C9] [C11] [C12]

[C16] [C18] [C19] was first developed in 1991; SCR [C4] in 1993; GTO [C13] in 1995; BJT [C20] in 1996; MOSFET[C3] [C17] [C14] in 1992; MCT [C7] [C2] in 1996; IGBT [C8] [C5] and MTO [C21] in 2000. The latest improvement on the lumped-charge method includes using a 2D multicell structure [C22] [C10] [C15] to model the 2D effect and large area multicell interconnection inside the thyristors.

Other methods, such as the Fourier transformation and Laplace transformation, were also used to solve the ADE. They have been successfully applied for IGBT modeling [C24][C25].

This study is the first to implement a physics-based model for the Emitter Turn-Off (ETO) thyristor using lumped charge modeling techniques. Section 2 explains the derivation of the model in details. The ETO operation mechanism is shown in Section 3. Followed by the experimental results, the developed model is validated in Section 4. Finally, a brief conclusion is drawn in Section 5.

2.2 ETO Lumped Charge Model Derivation

The basic idea of the lumped-charge modeling technique is to discretize the device physical layer into several distinct nodes. Traditionally, the PNPN thyristor is represented by an 8-node model, as shown in Figure 2-2. To keep the hybrid nature of the ETO device, a simplified behavioral MOSFET model is used.

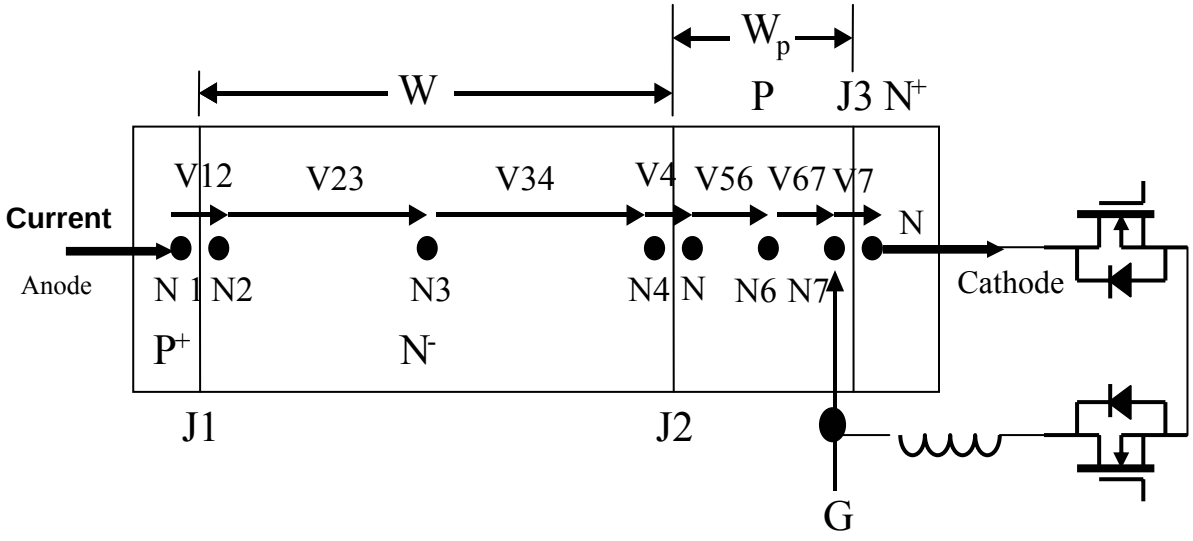


Figure 2-2 ETO lumped charge model

Current Transport Equations

The excess carrier in the lightly doped layer is governed by the current transport equations, which can be modeled as a current source between two adjacent nodes. Eq. 2-2 is the general form of the current transport equations. The current consists of two parts: drift current and diffusion current. The first term in the right side of Eq. 2-2 is the drift current density, which is proportional to the electric field. The second term is the diffusion current density, which is linearly related to the gradient of the carrier concentration. D_p and u_p are the hole diffusivity and hole mobility, q is the unit electron charge, and p is minority (hole) concentration.

$$j_p = qpu_pE - qD_p\frac{dp}{dx} \qquad \text{Eq. 2-2}$$

Taking hole current from n2 to n3 as an example,

$$i_{p23} = Aqp_3u_p\frac{V_{23}}{d_{23}} - AqD_p\frac{p_2 - p_3}{d_{23}} \qquad \text{Eq. 2-3}$$

$$i_{p23} = Aq_{p_3}u_p\frac{V_{23}}{d_{23}} - AD_p\frac{q_{p_2} - q_{p_3}}{d_{23}} \qquad \text{Eq. 2-4}$$

Using the charge storage node n3 as the origin of the drift current source, p3 is used in Eq. 2-3. q_{p3} is the product of q and p3, which is defined as charge concentration. Substituting the Einstein relation $\frac{D_p}{u_p} = \frac{kT}{q} = \Phi_T$ into Eq. 2-4, we can derive Eq. 2-5.

$$i_{p23} = sp_{23}\left[q_{p_3}V_{23} - \Phi_T\left(q_{p_2} - q_{p_3}\right)\right] \qquad \text{Eq. 2-5}$$

Where the coefficient $sp_{23} = {2Au_p}/{W}$, and Φ_T is the thermal voltage.

Similar equations can be derived for ip34

$$i_{p34} = sp_{34}\left[q_{p_3}V_{34} - \Phi_T\left(q_{p_3} - q_{p_4}\right)\right] \qquad \text{Eq. 2-6}$$

Boltzmann Relation

The Boltzmann relation is used to calculate the carrier concentration adjacent to the PN junction, which is dependent on the junction voltage.

$$\frac{n_y}{n_x} = \frac{p_x}{p_y} = e^{\frac{q}{kT}\left(V_{xy} - \Phi_{xy}\right)} \qquad \text{Eq. 2-7}$$

Eq. 2-7 is the general equation of the Boltzmann relation in a P_xN_y junction. $\Phi_{xy} = -\Phi_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$ is the built-in junction voltage, where the N_A is the doping concentration of the P region and N_D is the doping concentration of the N region.

For example, the carrier concentration at the P+N- junction is related to the junction voltage V_{12} by Eq. 2-8, where the q_{p20} is the thermal equilibrium state charge concentration.

$$q_{p_2} = q_{p_{20}} e^{\frac{q}{kT}V_{12}} \qquad \text{Eq. 2-8}$$

Similarly, the carrier concentration at the gate to cathode junction J3 is related to junction voltage V78 by Eq. 2-9.

$$q_{n_7} = q_{n_{70}} e^{\frac{q}{kT}V_{78}} \qquad \text{Eq. 2-9}$$

A charge-controlled voltage source can be used to represent the PN junction in the model.

Charge Neutrality Equations

The electron, hole, donor and acceptor are linked by the charge neutrality equation, as shown in Eq. 2-10. Considering each layer outside the space depletion region as electrostatically neutral, the space charge in each layer is balanced. The positive charges including the hole and the ionized donor atom are equal to the negative charges which are the electron and the ionized acceptor atom.

$$p - n + N_D^+ - N_A^- = 0 \qquad \text{Eq. 2-10}$$

For instance, in the base layer N-, the doping concentration is N_D.

$$q_{n2} = q_{p2} + q_{N_D} \qquad \text{Eq. 2-11}$$

$$q_{n3} = q_{p3} + q_{N_D} \qquad \text{Eq. 2-12}$$

$$q_{n4} = q_{p4} + q_{N_D} \qquad \text{Eq. 2-13}$$

For node n2, n3 and n4, the electrons are related to the holes by Eq. 2-11, Eq. 2-12 and Eq. 2-13 respectively, where $q_{N_{DB}} = qN_D$ is the doping charge density.

Continuity Equations

Similar to Kirchoff's current law in the circuit, the current continuity equation governs the time function of the holes and the electrons at each node. The left side of Eq. 2-14 can be viewed as the displacement current, which represents the node charge built-up current. Offset by the carrier generation rate G_p and combination rate U_p, the net holes flowing in the node is derived.

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\nabla J_p \qquad \text{Eq. 2-14}$$

Similarly, the electron continuity equation is

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\nabla J_n \qquad \text{Eq. 2-15}$$

The continuity equation only applies on the charge storage nodes, which are n3 and n6 in Figure 2-2. Taking n3 as example, assuming there is no generation in the N- base region, and recombination rate as $\frac{q_{p3} - q_{p30}}{\tau_B}$, where τ_B is the hole lifetime in the base region. Later, the generation and recombination rate can be characterized by the Shockley–Read–Hall (SRH) model.

$$\frac{\partial q_{p3}}{\partial t} = \frac{q_{p3} - q_{p30}}{\tau_B} - \left(ip_{23} - ip_{34}\right) \qquad \text{Eq. 2-16}$$

Poisson's Equation

In the space depletion region, the divergence of the electric displacement field is the free electric charge density, as shown in Eq. 2-17, where ε_s is the silicon dielectric constant.

$$\nabla^2\psi = \frac{-q\left(p - n + N_D^+ - N_A^-\right)}{\varepsilon_s} \qquad \text{Eq. 2-17}$$

Assuming the carrier concentration in the depletion region is negligible compared to the doping density, Eq. 2-17 can be simplified into

$$\frac{d^2v}{dx^2} = \frac{-q\left(N_D^+ - N_A^-\right)}{\varepsilon_s} \qquad \text{Eq. 2-18}$$

Integrating Eq. 2-18 over distance x, the depletion voltage is quadratic function of the depletion width X_B.

$$v = -\frac{qN_D}{2\varepsilon_s}x_B^2 \qquad \text{Eq. 2-19}$$

or,

$$x_B = \sqrt{\frac{2\varepsilon_s N_A}{qN_D\left(N_A + N_D\right)}\left(V_{45} + \Phi_{45}\right)} \qquad \text{Eq. 2-20}$$

Kirchoff's Current Law and Kirchoff's Voltage Law

Using the equations mentioned above, a lumped-charge model can be derived, which is represented in Figure 2-3. KCL and KVL are used to link the charge variables to the external voltage signals. Solving the circuit network for the branch current and nodes voltage, then reflecting the current and voltage signals to the internal charge variables using the aforementioned equations, the physic-based ETO model is obtained.

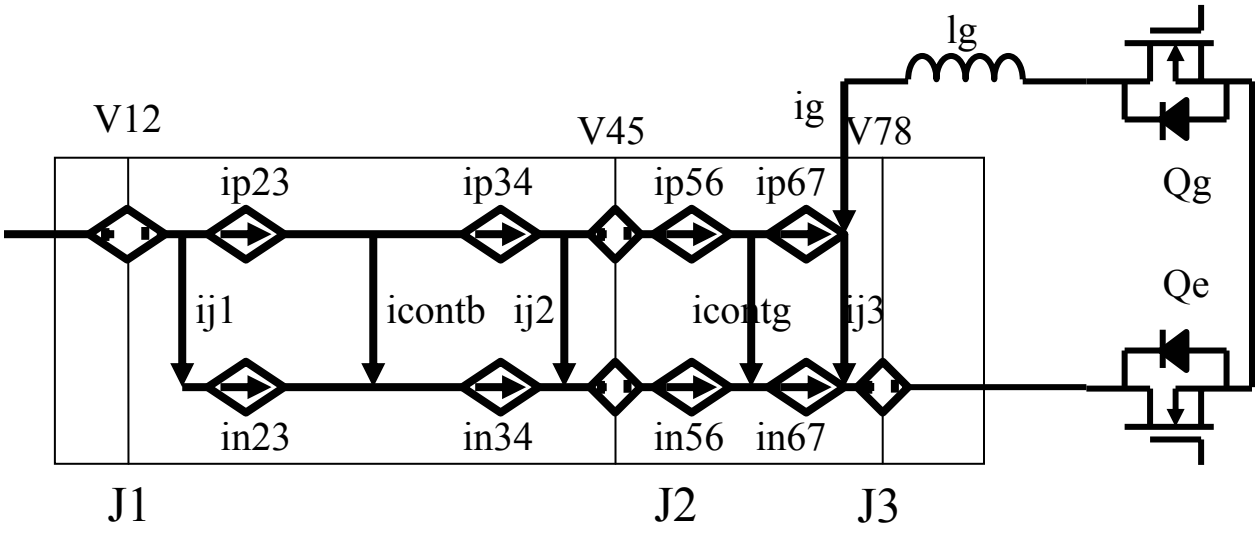


Figure 2-3 ETO lumped charge model equivalent circuit

Some other features of the model are further refined to include: the anode short effect in Eq. 2-21, the depletion carrier generation in Eq. 2-22, the avalanche breakdown of gate-to-cathode PN junction in Eq. 2-23, and the gate resistance in Eq. 2-24.

$$i_{j1} = \frac{v_{12}}{R_{short}}$$ Eq. 2-21

$$I_{j2} = A \cdot q \cdot x_d \cdot G_0$$ Eq. 2-22

$$I_{j3} = -A \cdot J_{3break} \cdot \exp\left(-v_{78} - V_{3break} \Big/ \Phi_T \right)$$ Eq. 2-23

$$I_{pG7} = \frac{V_{G7}}{R_{gate}}$$ Eq. 2-24

.

2.3 ETO Operation Mechanism

As shown in Figure 2-1, the ETO has three gate terminals. Gate 1 is the current injection terminal, gate 2 controls the emitter switch Q_E, and gate 3 controls the gate switch Q_G. The turn-on and turn-off process of the ETO involves the coordinate of the gate terminals.

During turn-on, the emitter switch Q_E is on and the gate switch Q_G is off, at the same time, a large current is injected in through the gate 1 terminal to effectively turn-on the internal GTO thyristor. With the aid of the developed model, the turn-on process of the ETO [B6] can be easily studied. The model simulated turn-on process is shown in Figure 2-4. With an increased gate current, the turn-on time of the ETO is significantly reduced. However, the increased gate current demands more power from the driver circuit. In other words, an insufficient gate current

requires long turn-on time which deteriorates the ETO switching dynamics performance. Hence, an optimum gate current can be achieved.

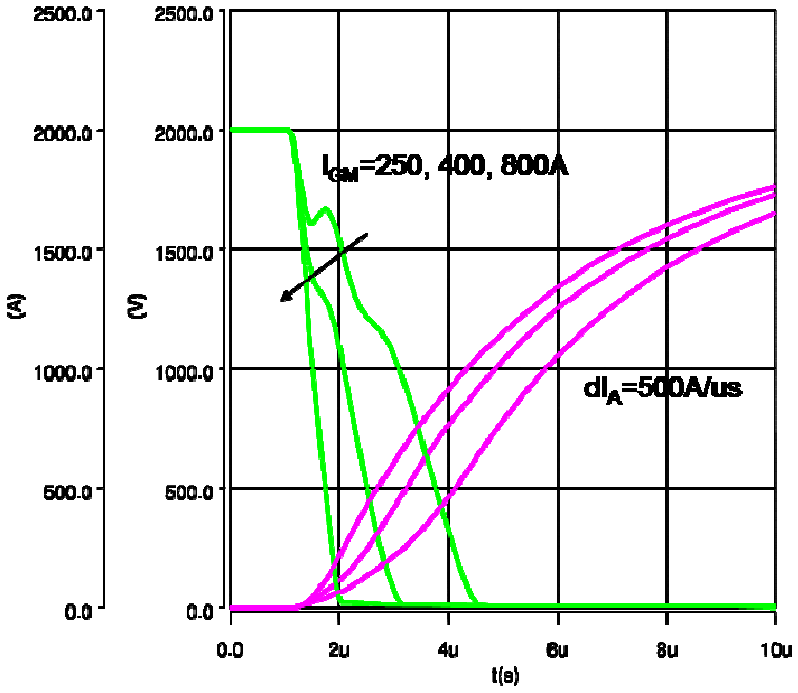
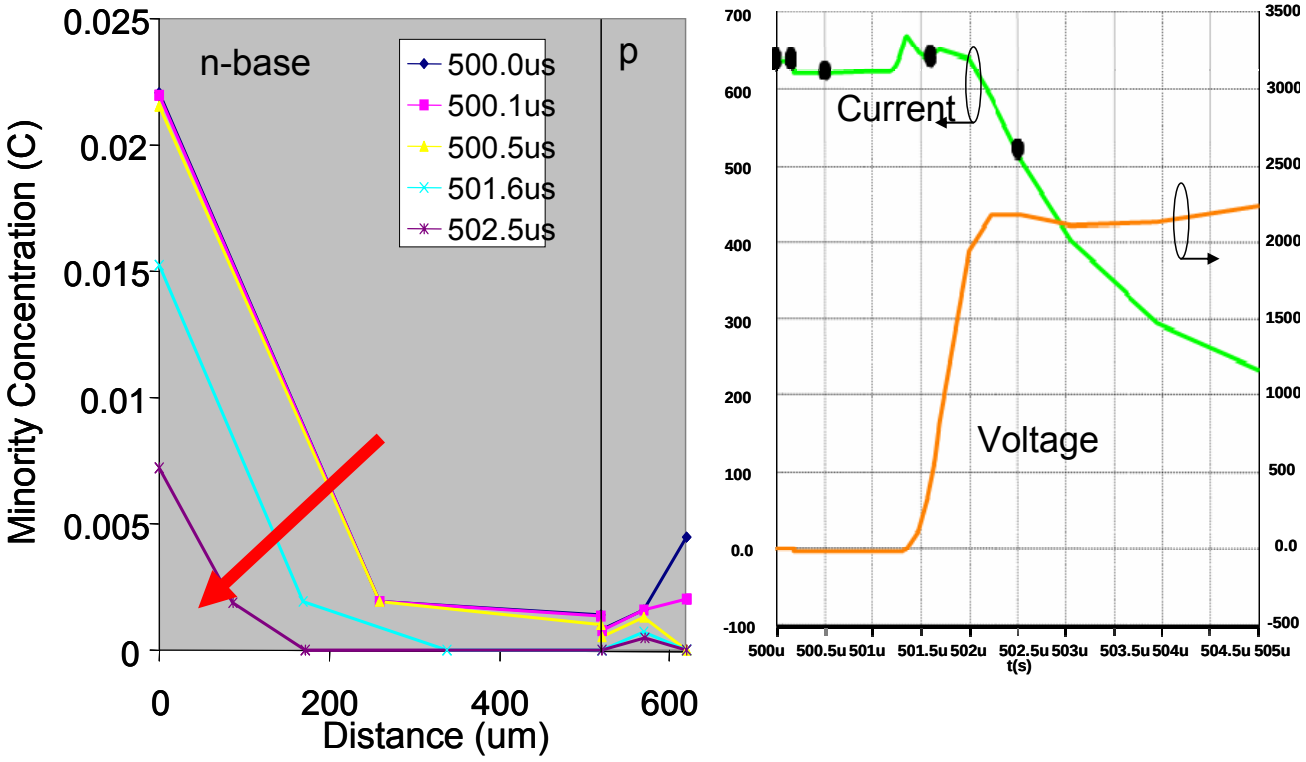


Figure 2-4 Simulation of ETO turn-on using lumped charge model

During the turn-off process, the gate switch Q_G is on, the emitter switch Q_E is off. Thus a dynamic voltage pulse is generated which diverts the GTO cathode current to the gate. After the current commutation finishes, the GTO enters into a PNP transistor mode, and eventually turns off. The turn-off process is very complicated, while the model reveals the dynamic process inside the device. Figure 2-5 shows the carrier concentration during the dynamic turn-off process. At the beginning of 500μs, a turn-off signal initiates the ETO process; the minority concentration is represented by the blue line. First, the gate-to-cathode junction is reverse-biased, which causes the junction breakdown; the electrons are extracted from the gate-connected P-base region, which is shown in Figure 2-5 (a), the pink line shows the electron concentration is greatly

reduced in the P-base region. After the cathode current commutates to the gate, the thyristor behaves as a PNP transistor, and the voltage build-up as the space depletion region expends in the N base region, which is shown in the cyan line. Finally, the space depletion region stops at the purple line when the device voltage reaches the DC-link voltage. The current and voltage waveform are shown in Figure 2-5 (b).



(a) Charge distribution (b) Turn-off waveform

Figure 2-5 Simulation of ETO turn-off using lumped charge model

2.4 ETO Model Validation

The ETO model is verified in a testbed. The test schematic is shown in Figure 2-6. Shown in Figure 2-7 is the simulated turn-off at 2000V, 2000A conditions. The pink curve is the anode current, the yellow curve is the device voltage, and the blue curve is the emitter voltage, which clearly show several distinct periods happening in the turn-off process. The dynamic voltage pulse corresponds to the current commutation period, the first voltage dip is caused by the depletion of the P-base region, and the second voltage dip is caused by the anode current falling di/dt effect. Figure 2-8 shows the experimental results. The same features are represented in details. Considering the parasitic capacitance in the GTO gate junction and the MOSFET parasitic capacitance, some oscillation occurs. The experimental results are consistent with the simulation results which verify the model in the turn-off process. Further refinement of the model needs to include the parasitic parameters to represent the device in great details.

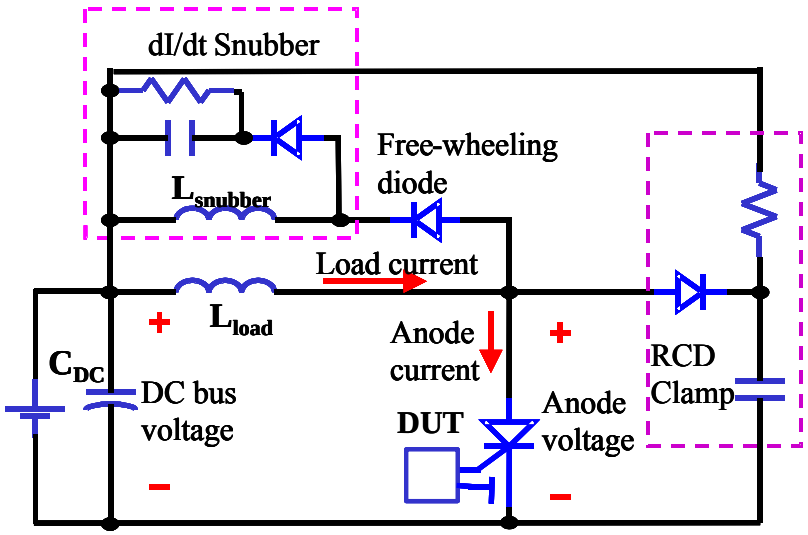


Figure 2-6 Model validation test schematic

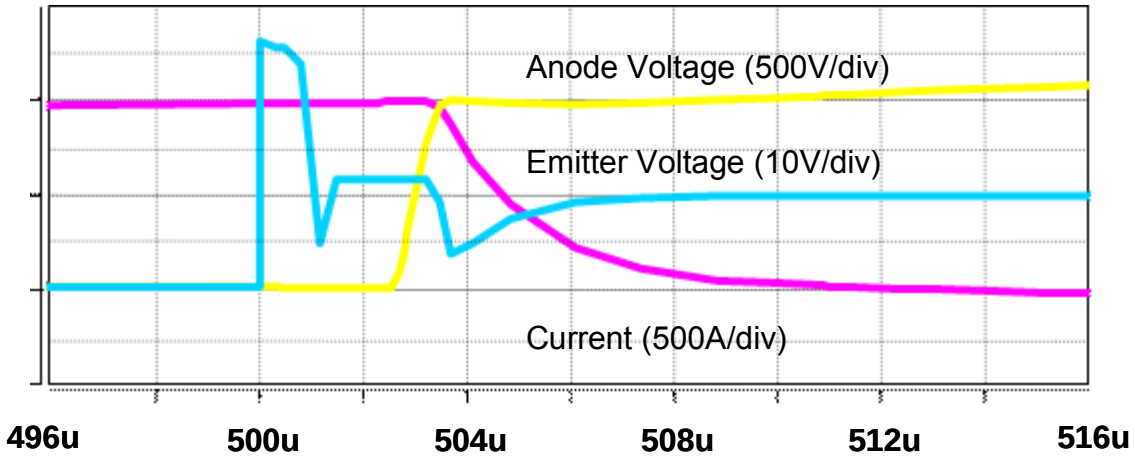


Figure 2-7 Simulated ETO turn-off waveform

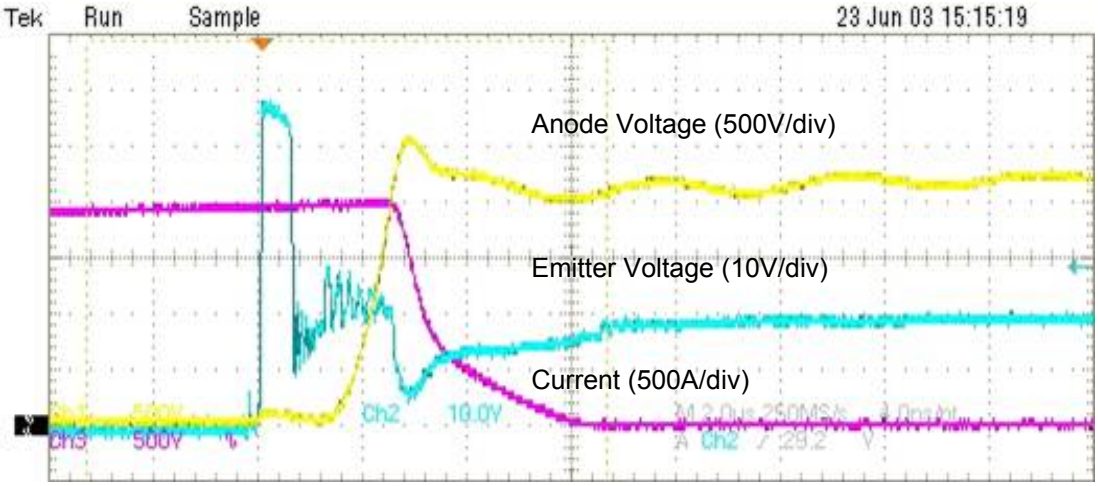


Figure 2-8 Tested ETO turn-off waveform

2.5 Conclusion

A physics-based lumped charge model is developed for the novel Emitter Turn-Off (ETO) thyristor. The model facilitates the development of this advanced power semiconductor device. With the aid of the model, the ETO operation mechanism is better understood. Experimental

results confirm the validation of the model, and the model is further used in the study of device series operation and parallel operation.

Chapter 3.
Parallel Operation of Emitter Turn-Off Thyristor

3.1 Introduction

Parallel operation of power devices is likely to be used in order to achieve higher current handling capability due to the lack of a single device with large enough current handling capability for some applications, such as a circuit breaker.

Maintaining current sharing is a critical issue in using devices in parallel. Current sharing issues include static and dynamic current sharing. The Power MOSFET has a positive temperature coefficient on-state resistance that is important for achieving static current sharing, whereas the IGBT has a negative temperature coefficient at low current ranges due to the bipolar diffusion current mechanism, and positive temperature coefficient at high current ranges due to the MOSFET current conduction mechanism. It is therefore important to design an IGBT with a low crossover point in its temperature-dependent I-V characteristic. On the other hand, both the MOSFET and the IGBT have gate-controlled transfer characteristics, which are often used as the current-balancing principle for achieving good dynamic current sharing [D1]. The statistics method [D2], spreadsheet or simulation tools [D3], and current sharing inductance [D4] are also used to maintain good dynamic current sharing in IGBT. However, these methods are hard to use for GTO devices. First of all, the GTO conducts current through a latched thyristor mechanism, thus the device current is uncontrollable during the on-state. The GTO device's forward drop usually has a negative temperature coefficient, which makes static current sharing difficult. Secondly, the GTO is a current-controlled device, which requires about 1/3 to 1/5 of the device

current to turn off the device. The turn-off delay time (storage time) is in the range of ten to twenty microseconds and is very sensitive to the gate drive circuit. Therefore there is large storage time dispersion among GTO devices, which makes the dynamic current sharing very difficult in GTO devices. Consequently, no paralleled GTO devices are in practical use.

The ETO thyristor is a novel high-power switch based on the hybrid MOSFET and GTO integration. The characteristics that make the ETO attractive have been discussed extensively elsewhere [B1]-[B5]. This chapter discusses the features that make the ETO suitable for parallel operation and investigates experimentally the parallel operation of high-power ETOs. The structure and features of the ETO are briefly described in Section 3.1.1. Experimental results of high power ETOs in parallel are shown in Section 3.2, and theoretical analysis of parallel operation is provided in Section 3.3. Finally, a conclusion is made in Section 3.4.

3.1.1 ETO Characteristics Important for Parallel Operation

The operation mechanism of the ETO can be interpreted from the turn-on process and the turn-off process. The equivalent circuit is shown in Figure 3-1. During the ETO's turn-on, the emitter switch Q_E is turned on and the gate switch Q_G is turned off, and at the same time a high-current pulse is injected in the GTO's gate. During the ETO's turn-off, the emitter switch Q_E is turned off and the gate switch Q_G is turned on, hence the GTO cathode current will be diverted to its gate almost instantly, realizing so-called "unity gain" turn-off, which means the GTO gate current equals the anode current before the end of the storage phase. The benefit of the unity gain turn-off is enormous. First, the storage time, which is the time needed for the gate-current to

remove all minority charges (electrons) in the p-base region, is now significantly decreased to about 1μs. Consequently, the latch-up state of the traditional GTO is broken, and the turn-off of an ETO is changed to an open-base PNP process that further ensures the current's uniform distribution among GTO cells over the turn-off transient. The significantly reduced storage time is critical in applying the ETO in parallel operation. Figure 3-2 shows a typical turn-off waveform of the ETO, indicating a storage time of 1.2μs at 2000A.

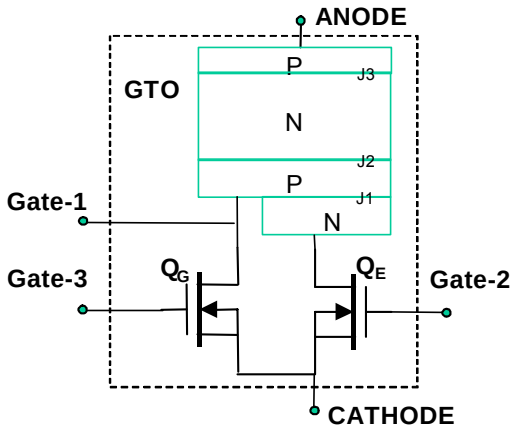


Figure 3-1 ETO equivalent circuit diagram

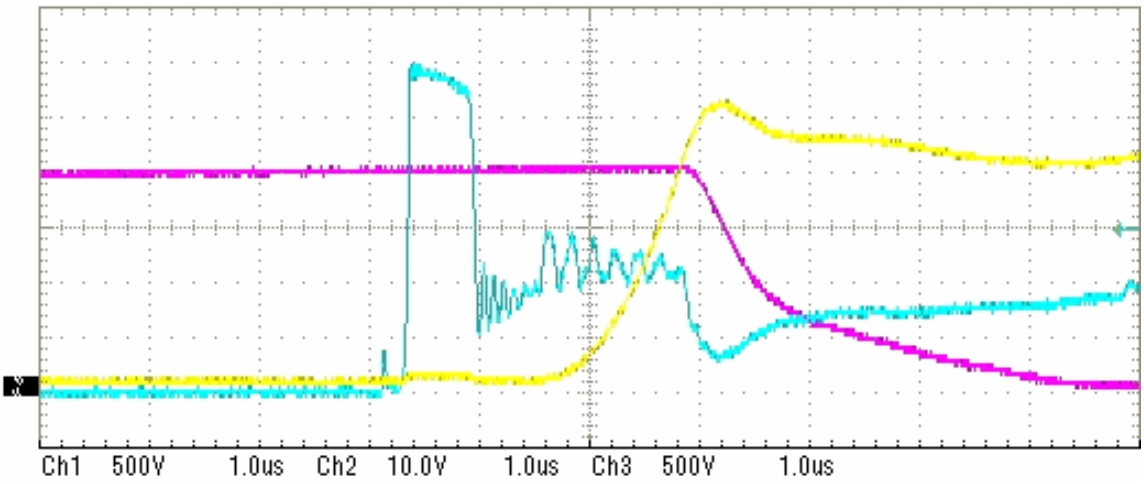


Figure 3-2 ETO4045TA turn-off waveform

3.1.2 Static Current Sharing of the ETO

Generally speaking, uniform I-V characteristics among paralleled devices (Figure 3-3) will benefit parallel operation, and the positive temperature coefficient on-state resistance will alleviate the current unbalancing due to the self-heating effect.

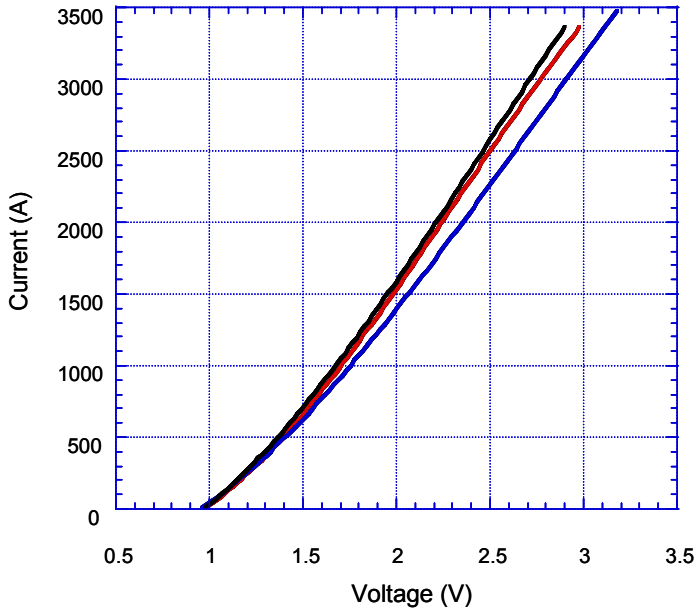


Figure 3-3 Three ETO4045TAs I-V characteristics

High-voltage GTOs are more likely to have a resistive I-V characteristic than are low-voltage GTOs and are therefore desirable for static current sharing. For the ETO, the series-connected MOSFET, which behaves like an emitter ballast resistor, makes the ETO's I-V characteristic even more resistive and therefore favorable in terms of static current sharing. Figure 3-3 shows the I-V characteristics of three ETO4045TAs, showing similar if not identical current conduction characteristics.

To avoid positive feedback of current crowding, a positive temperature coefficient I-V is very important. Typical high-voltage GTOs have a positive temperature coefficient above a critical current value. For the ETO, this critical current value moves to lower currents because of the strong positive temperature coefficient of the series-connected MOSFETs. Figure 3-4 shows measured ETO4045TA forward drops at different temperatures as well as the contribution of the MOSFET Q_E. For the measured ETO, positive temperature coefficient is obtained at above 500A while this point for the GTO is about 1000A. Static current sharing of parallel ETOs above 500A is therefore guaranteed for this type of ETO device.

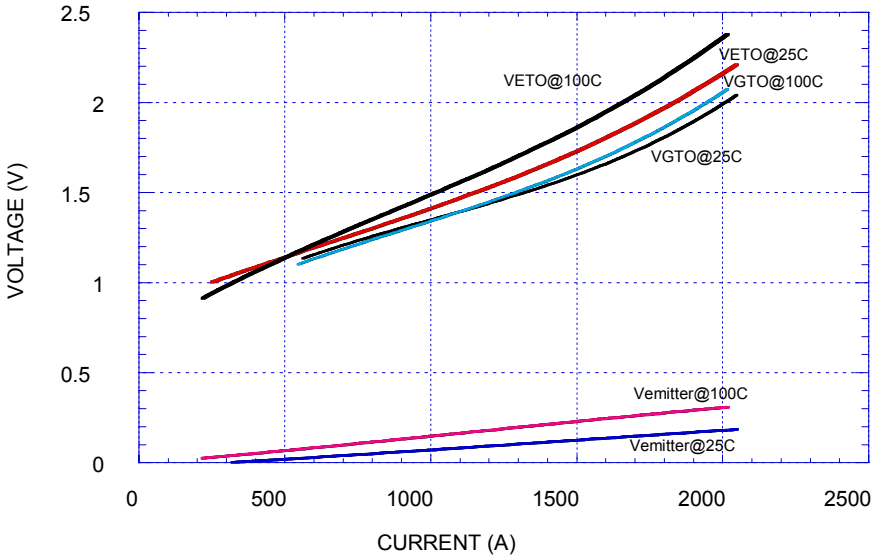


Figure 3-4 ETO4045TA I-V characteristics temperature coefficient

3.1.3 Dynamic Current Sharing of the ETO during Turn-off Transient

Dynamic current sharing is a showstopper for traditional GTOs operating in parallel connection because of their PNPN latch-up mechanism. GTOs are normally turned off with a

turn-off gain higher than unity, hence at the end of the storage phase, GTOs remain in latch state. If GTOs are in parallel, current crowding into the device with longer storage time will result in overcurrent in that GTO hence the violation of that GTO's turn-off capability. However, this mechanism is broken in the ETO turn-off operation. As soon as Q_E is turned off, a high dynamic voltage is applied to the gate loop inductance which forces the ETO device become an open-base PNP transistor before the end of the storage phase, and the cathode current completely commutates to the gate and recovers the emitter junction. This type of turn-off condition is referred as unity-gain turn-off [B2]

Under unity-gain turn-off, the storage time, which is the time needed to remove all the minority carriers in the p-base layer, is significantly reduced. As shown in Figure 3-2, the storage time of an ETO4045TA is about 1.2 μs, which is significantly less than the 20 μs storage time if the device is turned off in the GTO mode. During the storage phase, the cathode injection is cut off and the minority carriers in the p-base will simply decrease from their initial value. The current that removes the p-base minority carriers is the device's gate current, which now equals its anode current under the unity turn-off gain condition. Since the minority carrier quantity in the p-base is proportional to the anode current before the turn-off process and under unity gain turn-off, the minority carrier depletion speed is proportional to the anode current. The ETO's storage time is therefore almost a constant value over a wide current range.

Identical storage time ensures dynamic current sharing. Ten samples of ETO devices were tested under the same conditions, which is 2kV DC bus voltage and 2kA current. The storage time is defined as the time delay between the receiving of the turn-off command and the

beginning of the device voltage rising. The storage time consists of two distinct time periods: gate current commutation and carrier recombination time. Figure 3-5 shows the tested storage time for the ten samples of ETO devices, where the storage time is made up of the gate current commutation time, which is shown in the cyan portion, and the carrier recombination time which is shown in the purple portion.

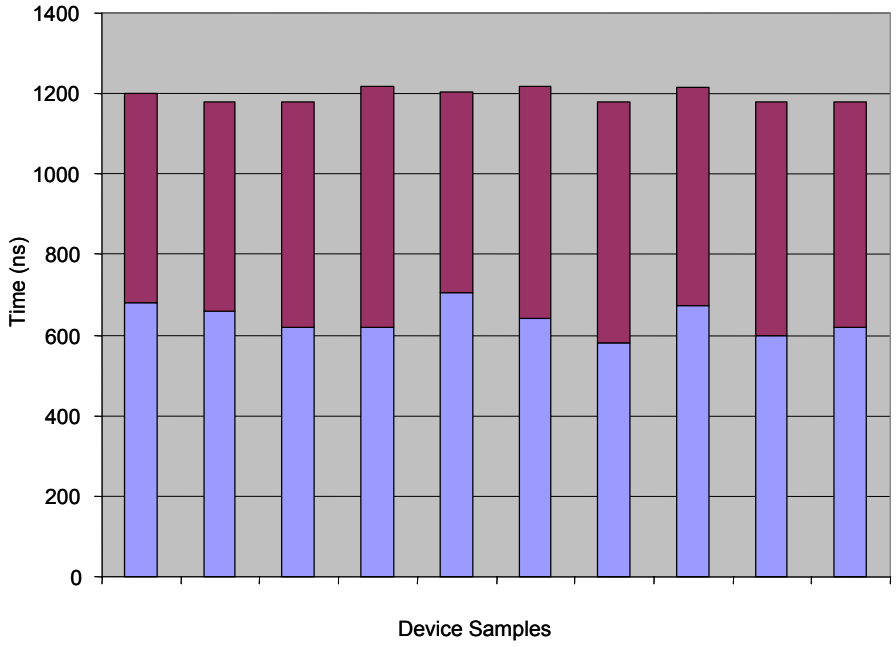


Figure 3-5 Ten ETOs storage time

The test results show extraordinary similarity between the performances of the ten devices. The mean storage time is 1196ns with a standard error deviation of 18ns.

The above analysis indicates that the ETO device is far superior to the GTO in dynamic current sharing because of its significantly reduced storage time and its insensitivity to currents. For the paralleled ETOs, dynamic current unbalance can still occur due to the dispersions or variations of the storage time between parallel devices.

Unlike the GTO, however, since the absolute value of the storage time is significantly reduced, the dispersion in storage time is also reduced. In other words, for the ETO, both ts and Δts are reduced. Because of this, the amount of current unbalance is small. Furthermore, a negative feedback mechanism exists between the current unbalancing and storage time. This can be understood by considering the case of two ETOs in parallel. The current will crowd to the slower device that has a longer storage time right after the faster ETO finishes its storage phase. However, more anode current means faster minority carrier removing speed, which makes the slower ETO's storage time shorter. This is a negative feedback process that alleviates dynamic current crowding.

3.2 Experimental Results

Three ETO4045TA devices were assembled in parallel under two back-to-back heatsinks, which are shown in Figure 3-6. The heatsinks also provide a mechanic clamp to the devices. No current sharing inductance is used for this parallel operation.

Figure 3-6 Three ETOs parallel operation test bench

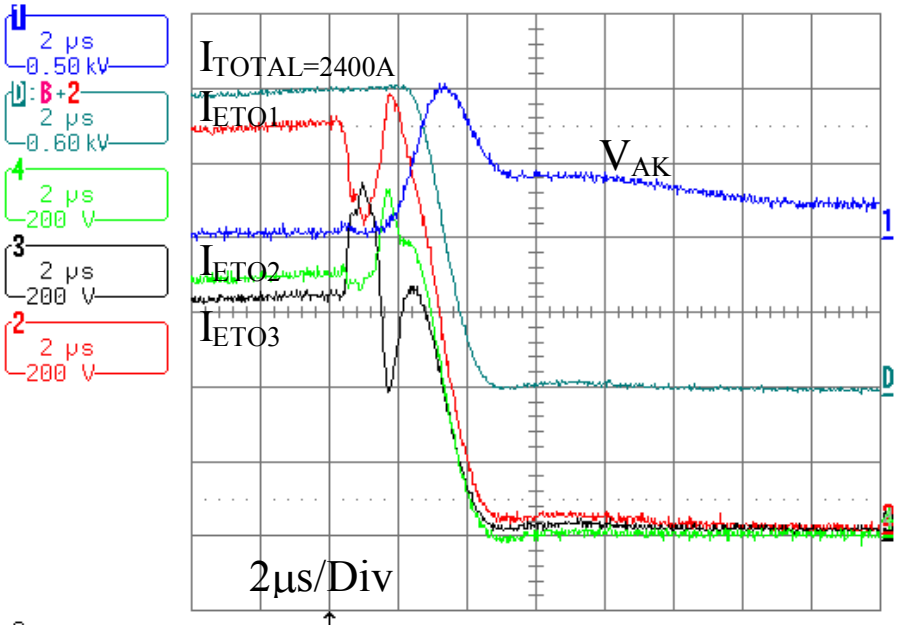


Figure 3-7 Three ETOs turn off with unbalanced initial currents.

Figure 3-7 shows three ETOs' static and dynamic current sharing characteristics under snubberless turn-off conditions. The current difference before turn-off is due to their I-V characteristic differences. Because ETO1 has a lower on-state voltage drop than the other two

ETOs, larger current differences exist among the three devices. At the turn-off point, ETO1 conducts 1100A, ETO2 conducts 700A, and ETO3 conducts 650A. As can be seen from Figure 3-9, ETO1 turns off first due to its larger initial current, and forces current to crowd into ETO3. ETO3, after receiving this additional amount of current, reduces its storage time and turns off second, forcing current back to ETO1 and ETO2. Eventually all three devices turn off with about the same current as the initial current for ETO1 and ETO3. These three devices are safely turned off even under an extremely unbalancing situation because these currents are still lower than the turn-off capability of the individual devices.

The dynamic current sharing test with a higher current was also performed for devices with slightly better static current sharing behaviours (Figure 3-8). The current sharing among three devices is good even at 5000A. The initial value of the device current is from 1500A to 1700A. A maximum current unbalance of about 200A is seen in ETO1 at the moment of final turn-off.

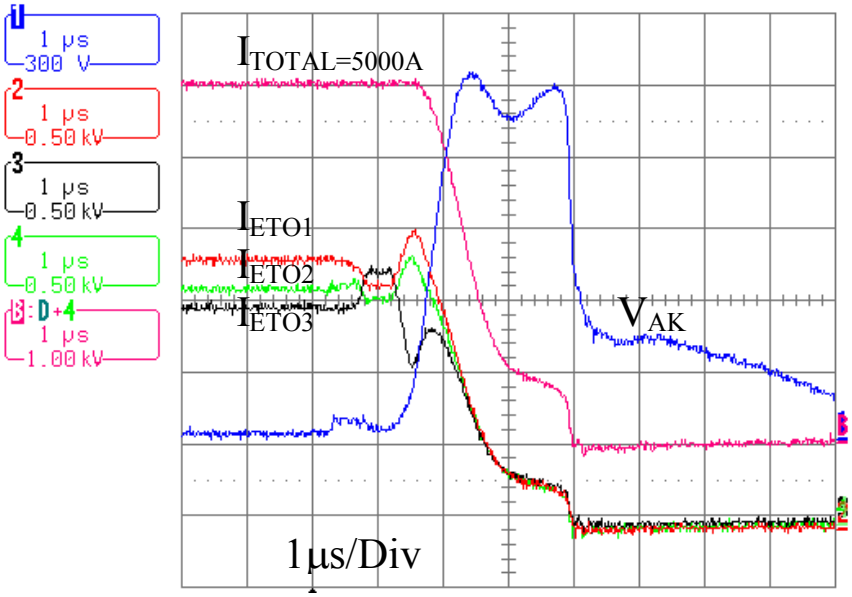


Figure 3-8 Dynamic current sharing among three ETOs

3.3 Qualitative Analysis of ETOs in Parallel

The waveform shown in Figure 3-8 suggests that current unbalancing will happen in the ETO turn-off. However, the unbalance is small and is counterbalanced during the storage phase instead of continuously increasing. The unbalance eventually disappears at the end of the storage phase and during the current fall stage. In order to understand the internal process associated with this phenomenon, the following analysis is provided with the help of the current and voltage waveforms in Figure 3-9. Initially a small difference in the P-base minority carrier distributions is assumed and ETO1 carries higher initial current than ETO3.

The turn-off process starts from ***t0.*** When the turn-off starts, MOSFET Q_E is turned off and MOSFET Q_G is turned on. A dynamic voltage V_{QE} will be applied to Q_E and divert the cathode current to the gate. Since the loop inductance between the gate and cathode can be considered constant for three ETO devices, the ETO1 that conducts larger current will need more time to completely divert the cathode current to the gate. Since the unity-gain condition is reached first in ETO3, its dynamic voltage V_{QE3} will decrease [B3]. But due to the parallel operation requirement, this cannot happen; instead its current will increase. Current transfer during this time is most likely from the device which carriers larger initial current (ETO1). As can be seen in Figure 3-9, current transfer in this phase therefore favors dynamic current sharing.

By ***t1***, all three ETOs reach unity turn-off gain. As shown in Figure 3-9, ETO3 now has higher anode current than the other two ETOs. Therefore ETO3 will finish the storage phase first

because it has a high carrier removal rate and the P-base carrier inside ETO3 has not increased. By ***t2***, ETO3 finishes its storage phase and all charges stored in the P-base are removed. It then enters the PNP mode of turn-off process while ETO1 and ETO2 are still in their storage phases. At this time ETO3 can no longer support the current, the voltage of ETO3 will have to increase or the current will have to go somewhere. Since no voltage can be increased, the current from ETO3 will flow to the slower (longer ts) device ETO1. In reality a small voltage increase normally accompanies this process and a small electrical field in the depletion layer of ETO3 is established. Once ETO1 receives more current, its carrier removal speed is enhanced which then shortens its storage phase. This negative feedback mechanism ends at ***t3*** when all three ETOs end the storage stage.

By ***t3***, ETO1 finishes its storage phase with a higher current value. From now until ***t4***, the voltage across all three devices will increase at a rate determined by all three of the devices minority carrier distributions left in the N-base region [B5]. Since the voltage increase rate of the three devices is the same, the rate of expansion of the depletion is also the same for the three ETOs. Once the voltage reaches the clamped voltage, the current of all three ETOs falls quickly. The falling rate is the fastest for ETO1 and can be explained as follows: the current decreasing rate is proportional to the carriers left in the undepleted N base and the initial current value [B5]. Since most of the carrier changes from ***t0*** to ***t3*** are at the cathode side, the carriers at the anode side and the undepeleted N-base region are similar for all three ETOs. Therefore the dominating factor for the falling di/dt is the initial current. Since ETO1 has a higher current, it will have higher di/dt. This higher di/dt helps the ETO3 to re-establish current balance with the other two ETOs during the current falling stage, as shown in Figure 3-8 and Figure 3-9.

By ***t4***, all three ETOs equally share the current again, and decrease to zero at the same rate until ***t5***.

In conclusion, our analysis clearly shows that there are three distinct processes in the dynamic current redistributions in the turn-off of paralleled ETOs. All three processes have a favorable tendency for current sharing instead of current runaway.

Similar analysis can be applied to N ETOs in parallel. It should be pointed out that this analysis also applies to other hard-driven GTO devices.

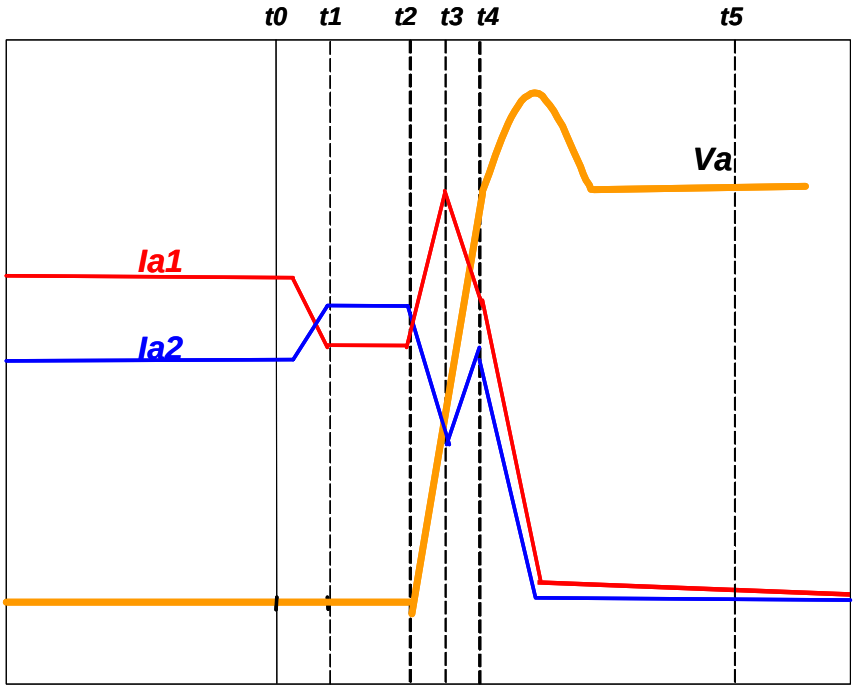


Figure 3-9 Turn-off processes for three ETOs parallel operation.

3.4 Conclusions

In this chapter, parallel operation of ETOs is analyzed and experimentally investigated. The structure and features of the ETO that makes it suitable for parallel operation are discussed, and analysis indicates that there is an intrinsic mechanism in the ETO that enables the ETO's current sharing during dynamic switching. A 5000A turn-off test verifies good current sharing between three ETOs.

Chapter 4.
Improving the Emitter Turn-Off Thyristor for Parallel Operation

4.1 Introduction

Parallel operation of power devices is used to extend the current handling capability of a single device for applications such as circuit breakers. The Emitter Turn-Off (ETO) thyristor performs well in parallel operation due to its uniform I-V characteristics and reduced storage time. Good current sharing of three ETOs in a 5000A high-power IPEM was demonstrated and an intrinsic mechanism in the ETO that enables ETO's current sharing during dynamic switching was obeserved and qualitatively analyzed in the previous chapter.

With the aid of the developed physics-based ETO model, the parallel operation of the ETOs is quantitively analyzed. Two critical factors affecting the dynamic current sharing are identified to be driver delay and storage time delay; the time-delay-caused current unbalancing is studied in a high-power IPEM. Detailed analysis of the storage time reveals the correlation between static current sharing and dynamic current sharing for the first time. The load current dependency of the storage time deteriorates the dynamic current sharing. The relationship between static current sharing and dynamic current sharing is studied and experimentally verified.

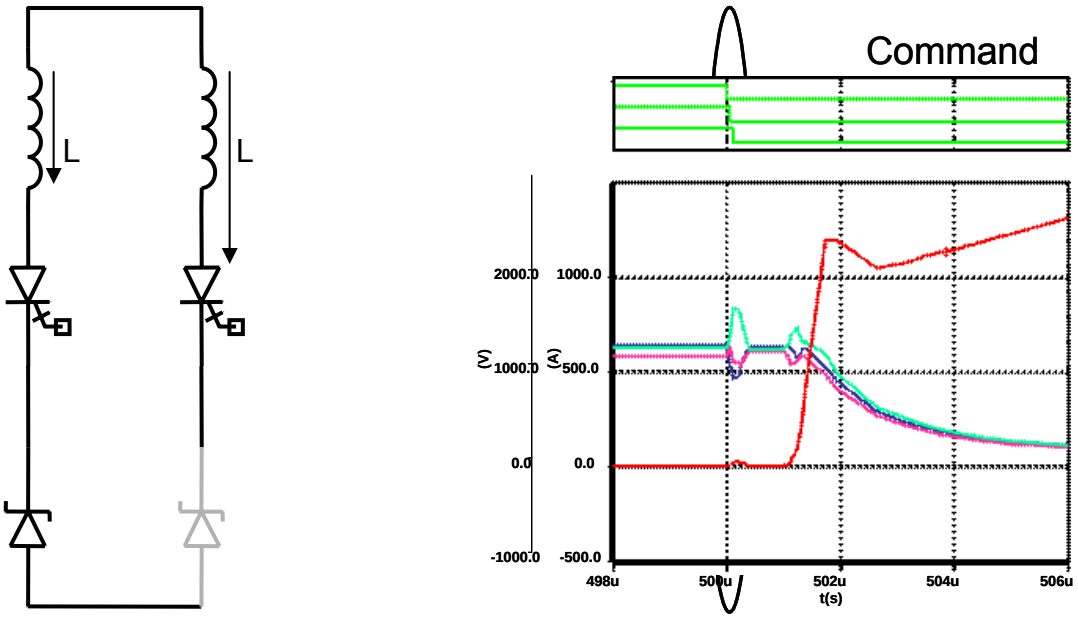
A new series of ETOs with improved performance for parallel operation is proposed. By increasing the dynamic voltage pulse during the gate current commutation phase, the gate commutation time is significant reduced, thus reducing the dependency on the load current, and

improving the device's parallel operation performance. Hence, better dynamic current sharing can be obtained regardless of the static current sharing.

4.2 Dynamic Current Sharing Factors

There are many factors affecting dynamic current sharing, the circuit related gate driver delay and the device-parameters-related storage time delay. The impact of these factors is studied with the aid of a physics-based ETO device model.

4.2.1 Gate Driver Delay



(a) equivalent circuit for dynamic current sharing (b) driver time delay impact on current sharing

Figure 4-1 Simulated driver time delay impact on dynamic current sharing

$$V_{zd} = 2 \cdot L_s \cdot \frac{di}{dt} \qquad \text{Eq. 4-1}$$

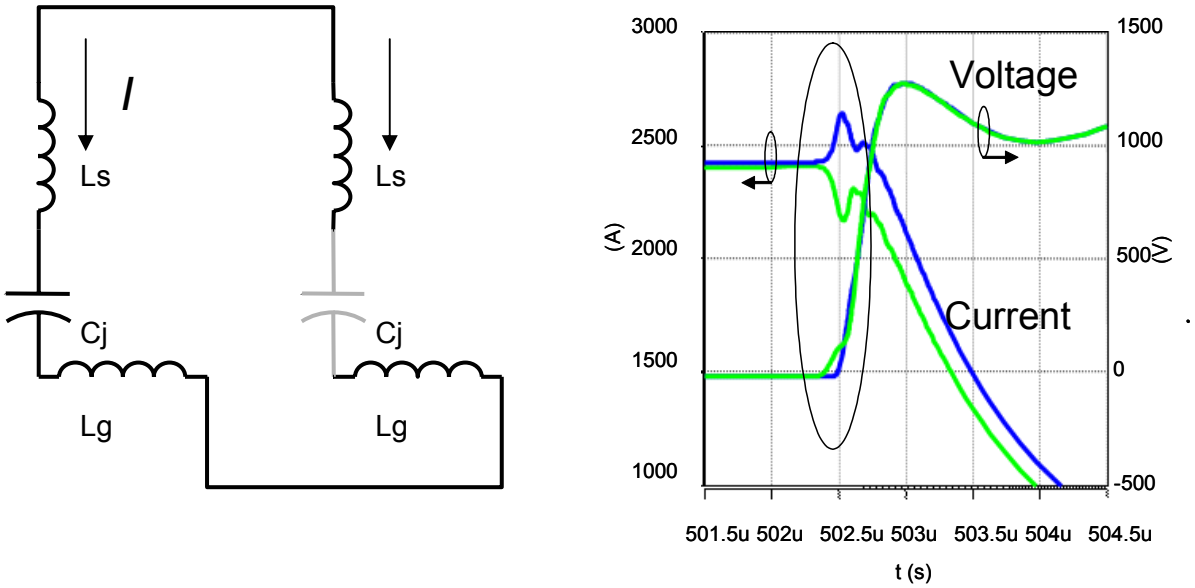
$$\Delta I = 2 \cdot \int_0^{\Delta t_d} \frac{V_{zd}}{(L_s + L_s)} \cdot dt = \frac{V_{zd}}{L_s} \cdot t_d \qquad \text{Eq. 4-2}$$

The gate driver delay includes the driver propagation delay, which is about 660ns for a typical ETO switch. After the initialization of the turn-off command, the emitter switch of the ETO device turns off first, and then behaves as a Zener diode afterward. The GTO thyristor stays in the on-state until the end of the storage time. The equivalent circuit of two ETO devices is shown in Figure 4-1 (a). The different driver delay will cause a dynamic voltage unbalance between the two ETO devices. For example, the fast turn-off switch will cause current crowding in the slow turn-off switch. The current crowding slope is determined by the dynamic voltage pulse V_{zd} and the loop inductance which is 2 times of stray inductance L_s. The relationship is shown in Eq. 4-1. Integrating Eq. 4-1 on the driver delay period, the current difference is derived in Eq. 4-2. Assuming the stray inductance between the devices is 3.8nH and the voltage pulse is 50V, a 50ns driver delay difference results in a 600A current crowding difference, as shown in Figure 4-1 (b). However, the driver delay can be adjusted by the MOSFET gate resistors. This feature can be used to match the driver delay of different ETO devices.

4.2.2 Storage Time Delay

Another current crowding phenomenon happens at the end of the storage phase. After the cathode current completely commutates to the gate terminal, the GTO device enters a PNP

transistor mode. Until the recombination of the minority carrier, the PNP transistor begins to support the voltage which indicates the end of the storage phase. At that time, the space depletion region expends to support the voltage, which forms an equivalent junction capacitor. The voltage built-up at the junction will again force a current redistribution. An equivalent circuit is shown in Figure 4-2 (a), where a junction capacitor represents the GTO device, L_s is the stray inductance between devices, and L_g is the additional gate loop inductance. Assuming the junction capacitance stays constant since the junction voltage varies in a small range, the junction voltage is governed by the relationship Eq. 4-3.



(a) equivalent circuit for dynamic current sharing (b) storage time delay impact on current sharing

Figure 4-2 Simulated storage time delay impact on dynamic current sharing

$$V_c = \frac{I}{C_j} \cdot t \qquad \text{Eq. 4-3}$$

$$\begin{aligned} \Delta I &= \int_0^{\Delta t_s} \frac{V_c}{(L_s + L_g)} \cdot dt \\ &= \int_0^{\Delta t_s} \frac{I}{(L_s + L_g) \cdot C_j} \cdot t \cdot dt \\ &= \frac{I}{2 \cdot (L_s + L_g) \cdot C_j} \Delta t_s^{\,2} \end{aligned} \qquad \text{Eq. 4-4}$$

Integrating Eq. 4-4 for the duration of the storage phase, we can derive the current ripple ΔI, which is a quadratic function of the storage time Δt_s.

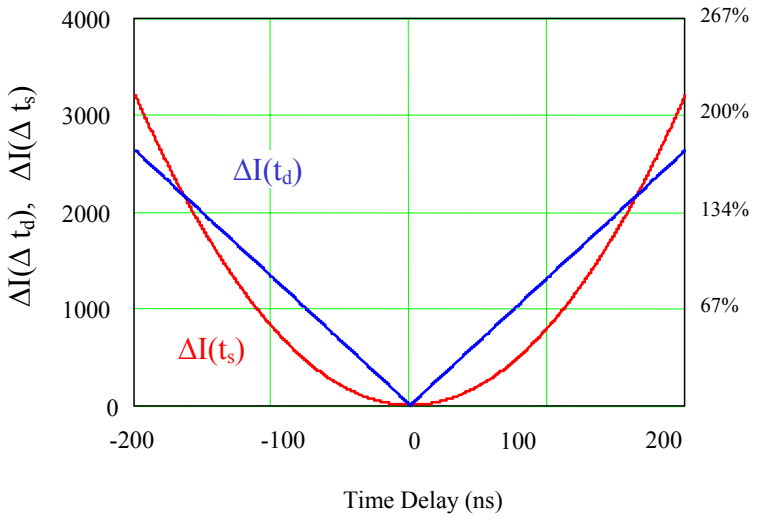


Figure 4-3 Current sharing and time delay relationship

The current ripple ΔI is a function of the driver time delay and storage time delay respectively. Figure 4-3 shows the current difference function of the time delay.

To ensure good dynamic current sharing, the driver delay difference should be less than 80ns. The storage time difference should be less than 100ns.

4.3 DirectETO—an Improved ETO Device for Parallel Operation

The time delay in the ETO device affects the current sharing performance between parallel devices. The driver delay can be adjusted by gate resistance. However, the storage time delay is related to the device's physical parameters and it is hard to match the storage time delay between different devices.

Figure 4-4 shows the time periods in a typical ETO turn-off waveform. The storage time consists of the gate current commutation time t_1 and carrier recombination time t_2.

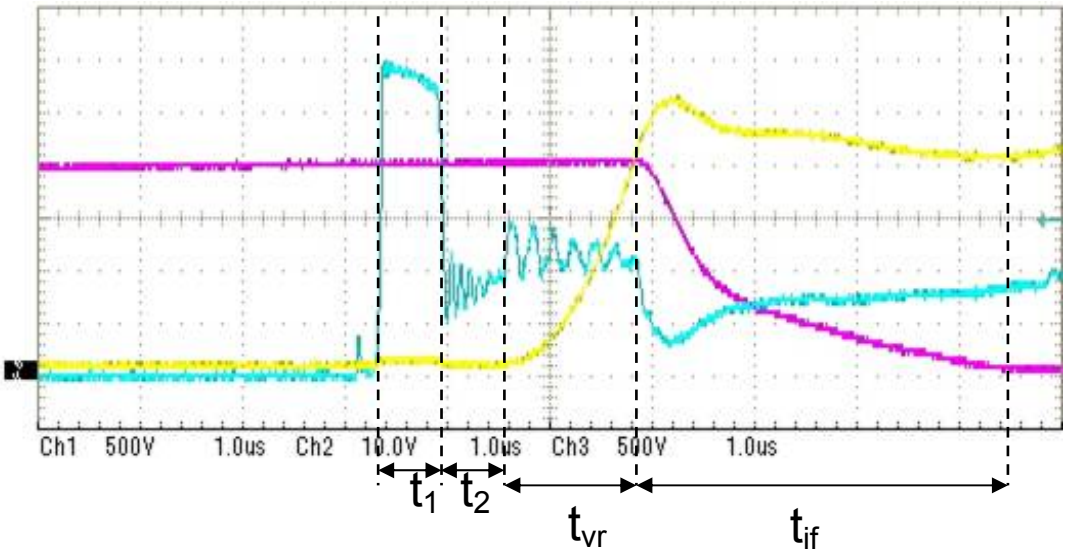


Figure 4-4 Time periods in a typical ETO turn-off waveform

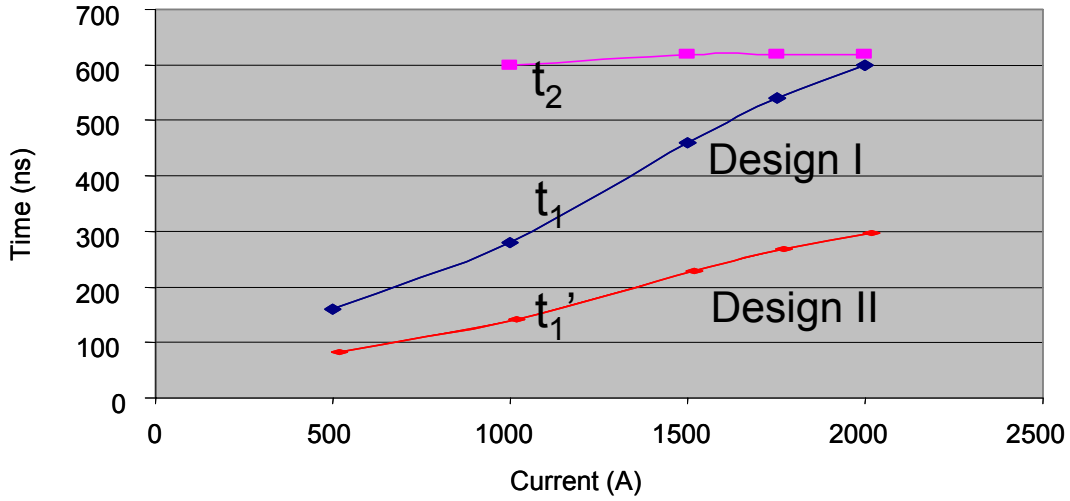


Figure 4-5 Storage time at different turn-off current

Figure 4-5 shows the relationship between the storage time and the turn-off current. The carrier recombination time t_2 is independent to the turn-off current, while the gate current commutation time t_1 is proportional to the turn-off current. The storage time is shown as a linear function of the turn-off current in Eq. 4-5. The deviation of storage time is shown in Eq. 4-6.

$$t_s = 610ns + 0.3025 \cdot I \qquad \text{Eq. 4-5}$$

$$\Delta t_s = 0.3025 \cdot \Delta I \qquad \text{Eq. 4-6}$$

A new series of ETO device is proposed to improve the device parallel operation performance. By increasing the dynamic voltage pulse during the gate current commutation phase, the gate commutation time is significant reduced. As shown in Figure 4-5, blue curve t_1 in the original design (Design I) is reduced to the red curve t_1' in the improved design (Design II).

Combining of Eq. 4-4 and Eq. 4-6, the dynamic current sharing is related to the static current sharing. Figure 4-6 shows the relationship of dynamic current sharing and static current sharing. With reduced gate commutation time t_1, the dynamic current sharing is less dependent on the static current sharing.

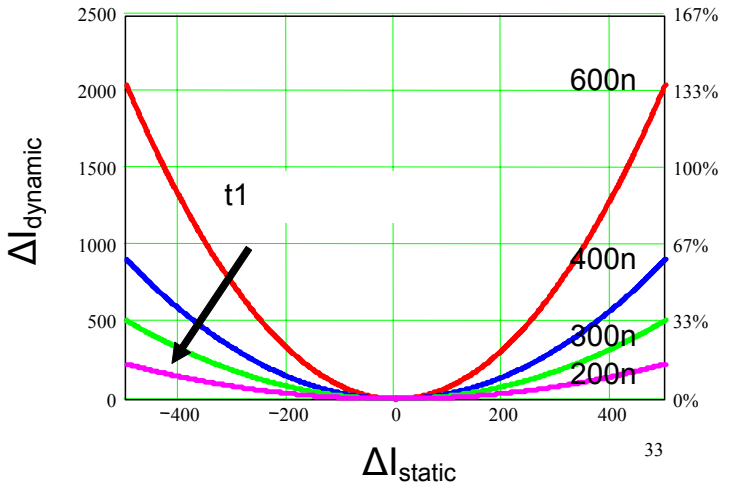
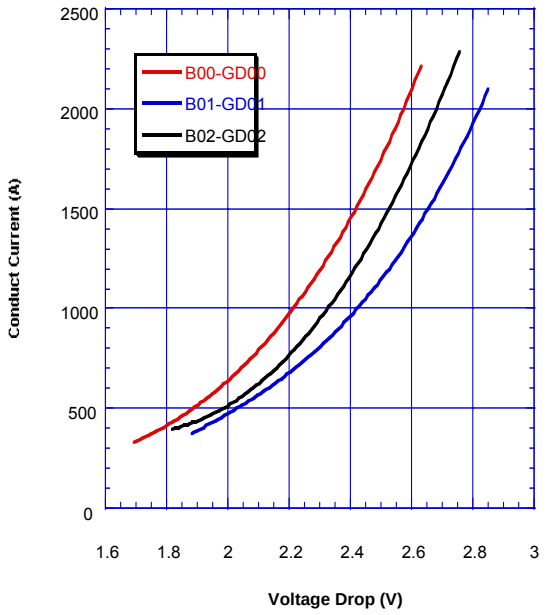
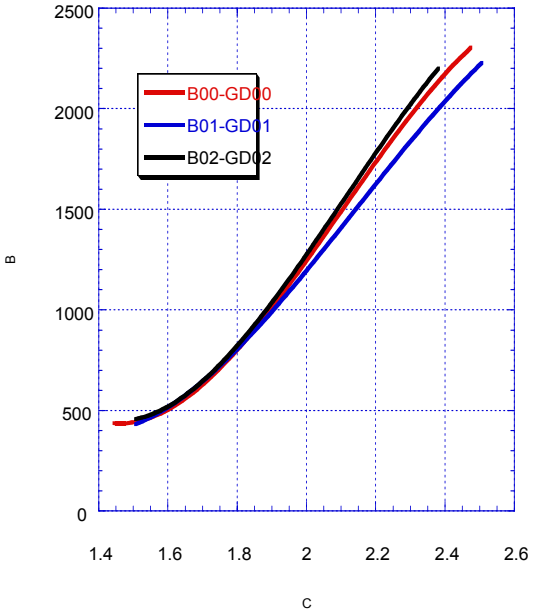


Figure 4-6 Dynamic current sharing vs static current sharing

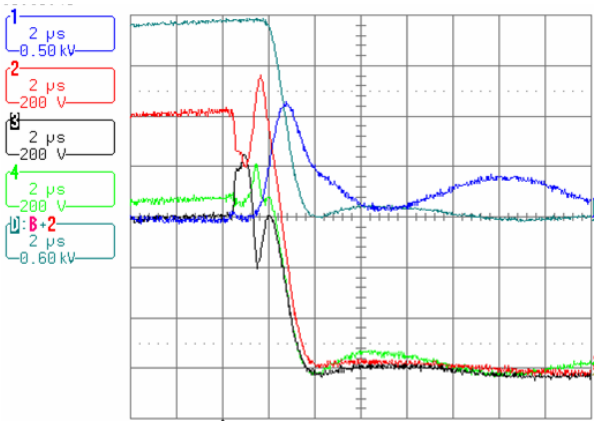
The relationship between the dynamic current sharing and the static current sharing is experimentally verified. As shown in Figure 4-7, the static current sharing represented by the static I-V curves is improved from (a) to (b), the corresponding dynamic current sharing is shown in (c) and (d).



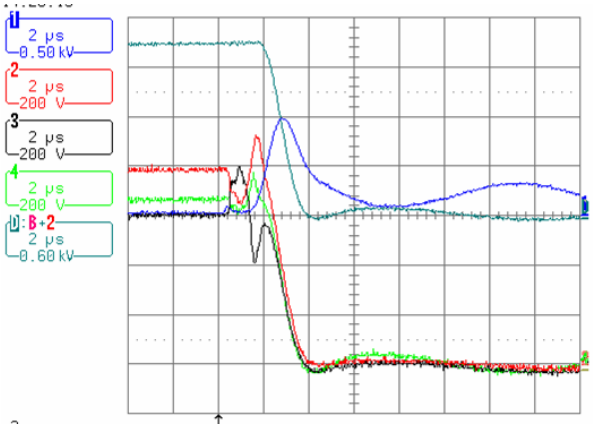
(a) original static current sharing



(b)improved static current sharing



(c)original dynamic current sharing



(d)improved dynamic current sharing

Figure 4-7 Dynamic current sharing improvement

4.4 Conclusion

The ETO device has good parallel operation performance because of the matched I-V characteristics and almost identical storage time. Two critical factors affecting dynamic current sharing are identified to be driver delay and storage time delay. In this chapter, the time-delay-caused current unbalancing is studied in a high-power IPEM. Detailed analysis of the storage time reveals the correlation between static current sharing and dynamic current sharing for the first time. The load current dependency of the storage time deteriorates the dynamic current sharing. The relationship between static current sharing and dynamic current sharing has been studied and experimentally verified.

A new series of ETO device is proposed to improve the device parallel operation performance. The main concept of this device is to decouple the storage time dependency from the load current. By increasing the dynamic voltage pulse during the gate current commutation phase, the gate commutation time is significant reduced, thus reducing the dependency on the load current, and improving the device parallel operation performance. Hence, a better dynamic current sharing can be obtained regardless of the static current sharing.

Chapter 5.
Electro-Magnetic Modeling of High-Power Integrated Power Electronics Module (IPEM)

5.1 Introduction

Integrated power electronics modules (IPEMs) [A17] are envisioned to be the primary drive for the next generation of power electronics. Significant research has been done in the CPES and elsewhere [A27] with the mission to develop advanced electronic power conversion technologies for efficient future electric energy utilization through multidisciplinary engineering research and education in the field of power electronics. An integrated system approach via IPEMs is envisioned to enable dramatic improvements in the performance, reliability, and cost-effectiveness of electric energy processing systems. The envisioned integrated power electronics solution is based on advanced packaging of new generation of devices and innovative circuits and functions in the form of building blocks with integrated functionality, standardized interfaces, suitability for automated manufacturing and mass production, and application versatility--namely IPEMs, and the integration of these building blocks into application-specific systems solutions.

The electro-magnetic modeling of the IPEMs is an important topic of the IPEMs. The fundamental function of the IPEMs is the energy transfer and conversion of the electro-magnetic field. Several important issues are also related to the electro-magnetic aspect of IPEMs, such as parasitics, electro-magnetic interface and so on.

Parasitics exist in the IPEMs at all power levels. In high-power IPEMs, the parasitics are exaggerated due to the high di/dt and dv/dt level. Even a small stray inductance can generate a high voltage spike, and hence cannot be ignored. The parasitic inductance is systematically analyzed for the 5000A high-power IPEM. With the extracted parasitic inductance, the device circuit interaction is evaluated, which results in an improved structure for the high-power IPEM.

5.2 Partial Element Equivalent Circuit (PEEC) Method

Inductance calculation is an important issue in power electronics engineering. An inductor is a circuit symbolization of the fundamental electro-magnetic field theory. Previously, because of the lack of numerical computation devices, the calculation of the electro-magnetic field was a headache for the field engineers. Grover did intensive work [A14] on this subject by providing the empirical formulas and tables to link the field theory to the practical electronic circuit geometries. The method is widely used to extract the inductance of regular-shaped inductors such as the solenoidal and toroidal inductors.

With the advance of Computer Aided Design (CAD) technology, the numerical method based on Maxwell's equations is used for field computation, which is able to provide an accurate solution for the complex 3D geometries of the interconnections, but is too slow for iterative physical design and verification.

In 1972, Ruehli proposed a partial inductance concept [A16] which is able to extract the inductance of complex 3D interconnections without complicated field computation. Thus it is widely accepted as an efficient way for inductance calculation.

To better understand the partial inductance concept, let's start with the well-known Webber's caveat: *It is important to observe that inductance of a piece of wire not forming a closed loop has no meaning* [A15]. By the nature of magnetism, the magnetic field is caused by the current loops.

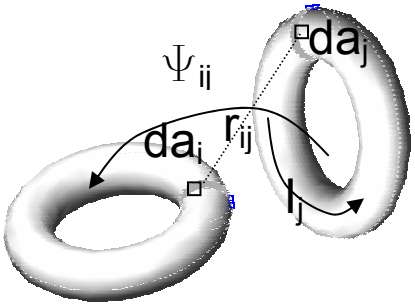


Figure 5-1 Mutual inductance of N current loops

As shown in Figure 5-1, the mutual inductance of N sets of current loop is defined as Eq. 5-1, where Ψ_{ij} represents the magnetic flux in loop I due to the current Ij in loop j.

$$L_{ij} \equiv \frac{\Psi_{ij}}{I_j} \qquad for \quad I_k = 0 \quad if \quad k \neq j \qquad \text{Eq. 5-1}$$

To calculate Ψ_{ij}, a magnetic potential vector A is defined by $B = \nabla \times A$, where $r_{ij}=|r_i-r_j|$, and dl_j is an element of loop j with the direction along the axis of the conductor.

$$A_{ij} = \frac{\mu}{4\pi} \frac{I_j}{a_j} \oint_j \int_{a_j} \frac{dl_j da_j}{r_{ij}} \qquad \text{Eq. 5-2}$$

$$\Psi_{ij} = \frac{1}{a_j} \oint_i \int_{a_j} A_{ij} \cdot dl_i da_i \qquad \text{Eq. 5-3}$$

Substituting Eq. 5-2 and Eq. 5-3 into Eq. 5-1, the Eq. 5-1 can be rewritten as Eq. 5-4.

$$L_{ij} = \frac{\mu}{4\pi} \frac{1}{a_i a_j} \oint_i \int_{a_i} \oint_j \int_{a_j} \frac{dl_i \cdot dl_j}{r_{ij}} da_i da_j \qquad \text{Eq. 5-4}$$

The discrete form of Eq. 5-4 can be rewritten as Eq. 5-5, where the Eq. 5-6 is the defined partial inductance. Partial inductance is the portion of loop inductance for a segment when its current returns in respect to infinity. This method of defining partial inductance is called Partial Element Equivalent Circuit (PEEC).

$$L_{ij} = \sum_{k=1}^{K} \sum_{m=1}^{M} L_{P_{km}} \qquad \text{Eq. 5-5}$$

$$L_{P_{km}} = \frac{\mu}{4\pi} \frac{1}{a_k a_m} \int_{a_k} \int_{a_m} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{dl_k \cdot dl_m}{r_{km}} da_k da_m \qquad \text{Eq. 5-6}$$

5.3 Parasitic Model of High-Power IPEM

Parasitic parameters are very important in a high-power IPEM. They cause high electrical stress during the switching transient, which is a potential "killer" unless properly attended to.

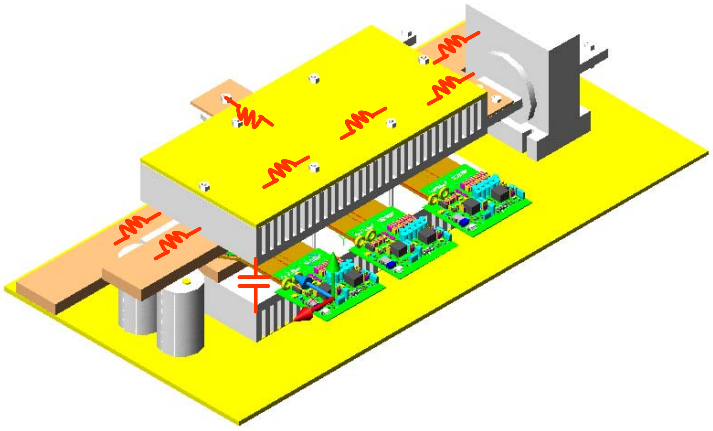


Figure 5-2 Parasitic inductance inside a high-power IPEM.

Three critical loop inductances are identified for the ETO-based high-power IPEM shown in Figure 5-2 and Figure 5-3. The red loop energy can be absorbed by the voltage clamp; the blue loop inductance affects the device current sharing; while the cyan loop inductance is harmful to the system and should be minimized.

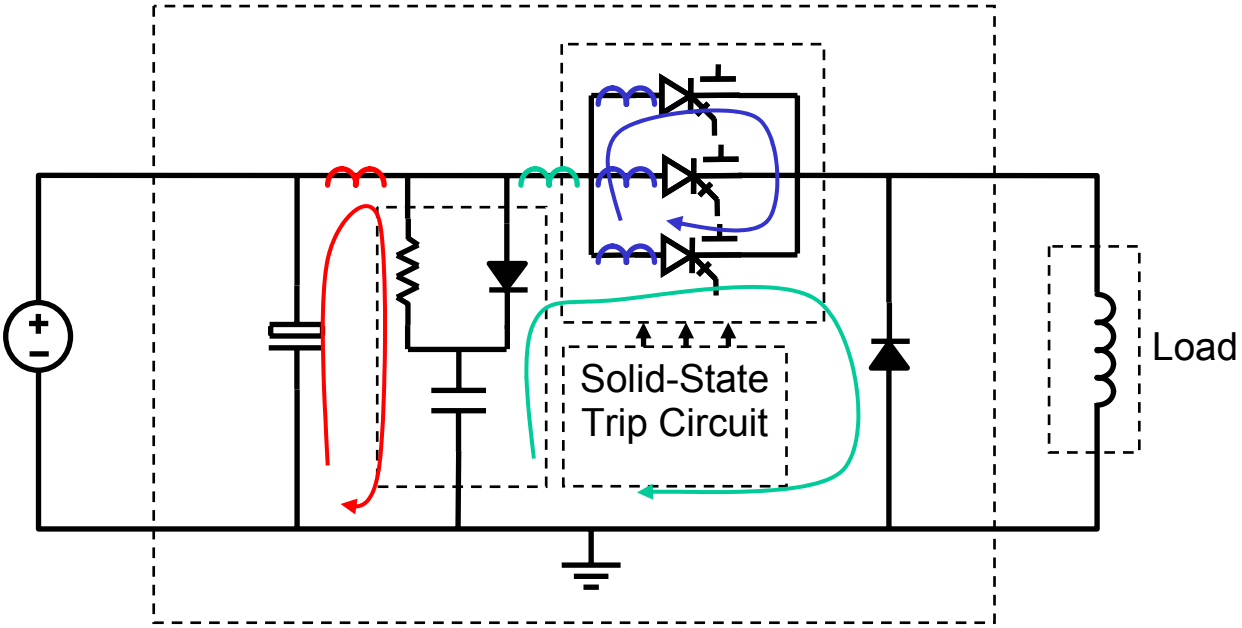


Figure 5-3 Critical parasitic loop inductance in a circuit breaker schematic

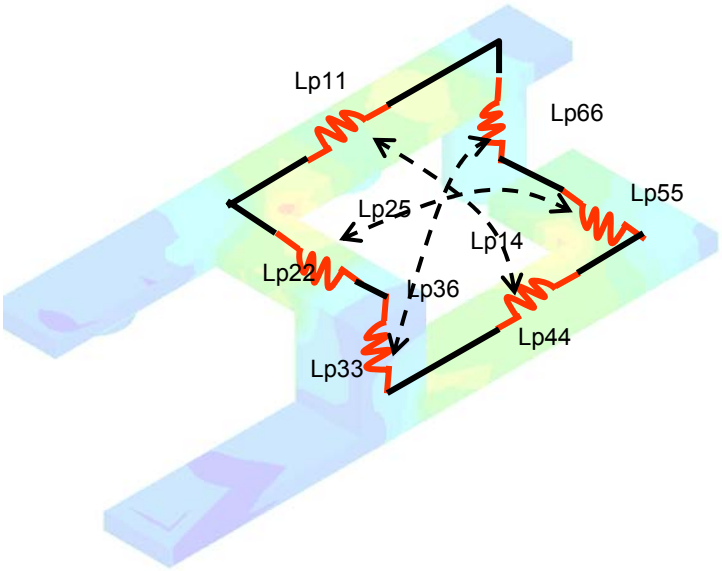


Figure 5-4 Clamped parasitic inductance PEEC model

For example, the loop inductance between the clamping capacitor and the voltage clamp, which is shown in the red loop in the schematic Figure 5-3, can be mapped back to the physical geometry, and then a PEEC model can be obtained as shown in Figure 5-4. The PEEC model consists of six partial inductances, L_{11}, L_{22}, L_{33}, L_{44}, L_{55} and L_{66}. Mutual inductance between L_{11} and L_{44} is defined as L_{14}, which is equal to L_{41}. L_{36} and L_{25} are defined accordingly. The inductance matrix can be derived as,

$$L = \begin{bmatrix} 195.3 & & & -53.0 & & \\ & 86.8 & & & -11.7 & \\ & & 34.5 & & & -4.5 \\ -53.0 & & & 195.3 & & \\ & -11.7 & & & 86.8 & \\ & & -4.5 & & & 34.5 \end{bmatrix} \quad \text{Eq. 5-7}$$

So the loop inductance is the summation of the partial inductances,

$$L_{loop} = \sum_i L_{ii} + \sum_{i \neq j} L_{ij} = 494.2nH \quad \text{Eq. 5-8}$$

This PEEC model is verified by field analysis of a 3D model in MAXWELL 3D© software. The field analysis offers more accurate results which take into consideration the skin effect and proximity effect. The PEEC model results error is within 10%.

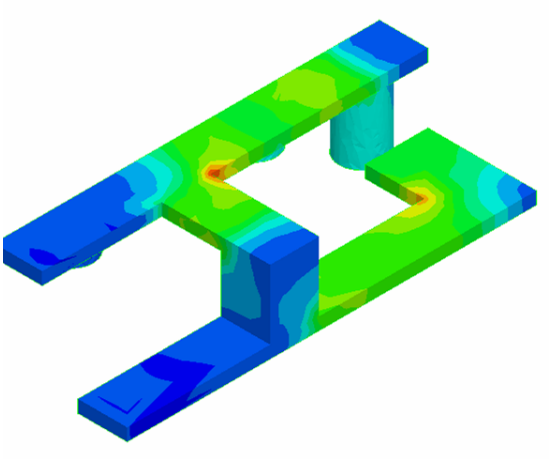


Figure 5-5 Clamped parasitic inductance Maxwell 3D model

Figure 5-5 is the DC current density distribution of the simulated static magnetic field analysis, which clearly shows the skin effect and proximity effect. The simulated loop inductance is 464nH.

$$L_s = 464nH \qquad \text{Eq. 5-9}$$

The loop inductance is further verified by experiments.

As shown in Eq. 5-10, the inductance Ls determines the magnitude of the electromagnetic force (emf) induced as a result of a given rate of change of the current. The voltage overshoot test is designed to calculate the loop inductance. From Figure 5-6, we can extract the loop inductance of 456nH.

$$\Delta V_{\max} = L_s \cdot \frac{di}{dt} \qquad \text{Eq. 5-10}$$

$$L_s = 456nH \qquad \text{Eq. 5-11}$$

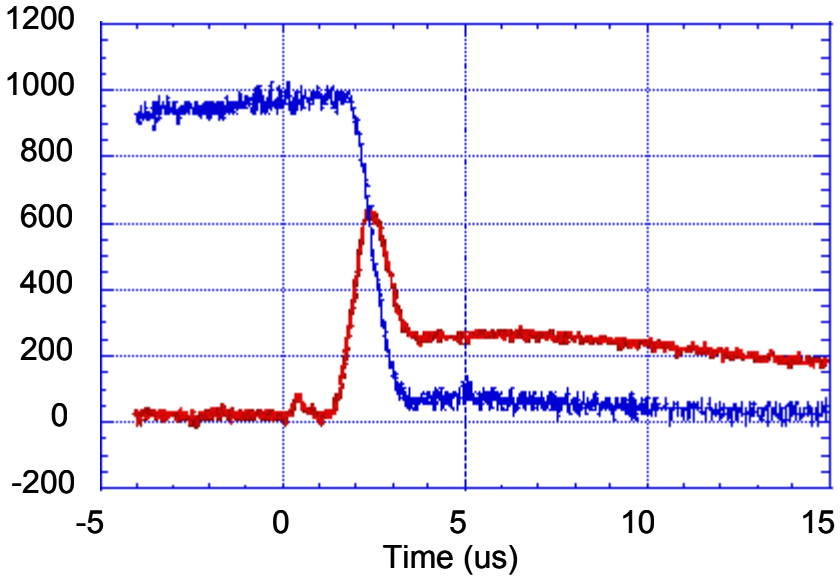


Figure 5-6 Measured voltage overshoot caused by clamped parasitic inductance

The other loops can be calculated accordingly. Figure 5-7 is the simulated DC current density distribution of the unclamped loop by the static magnetic field analysis. The extracted loop inductance is 344nH as shown in Eq. 5-12.

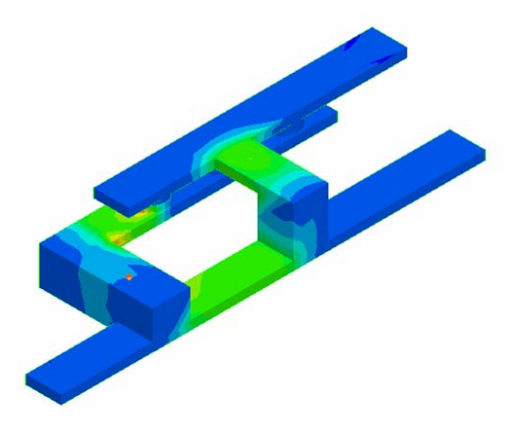


Figure 5-7 Unclamped parasitic inductance Maxwell 3D model

$$L_s = 344nH \qquad \text{Eq. 5-12}$$

Figure 5-8 shows the inter-device loop inductance simulation. The extracted loop inductance matrix is shown in Eq. 5-13.

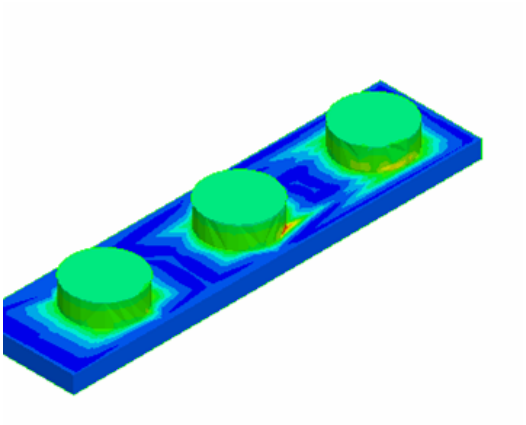


Figure 5-8 Inter-device parasitic inductance Maxwell 3D model

$$L = \begin{bmatrix} 3.8 & 0.58 & 0.03 \\ 0.58 & 3.8 & 0.57 \\ 0.03 & 0.57 & 3.8 \end{bmatrix} nH \qquad \text{Eq. 5-13}$$

5.4 Parasitic Circuit Interaction

The electro-magnetic simulation is conducted to study the high-power IPEM voltage stress. Figure 5-9 shows the simulated IPEM voltage stress in the high-power IPEM and the tested waveform. The voltage spike on the IPEM is governed by Eq. 5-14.

$$\frac{1}{2}LI^2 = \frac{1}{2}CV_2^{\,2} - \frac{1}{2}CV_1^{\,2} \qquad \text{Eq. 5-14}$$

Assuming the circuit breaker is operated at the maximum DC voltage of 2500V, the voltage spike on the IPEM is about 3200V.

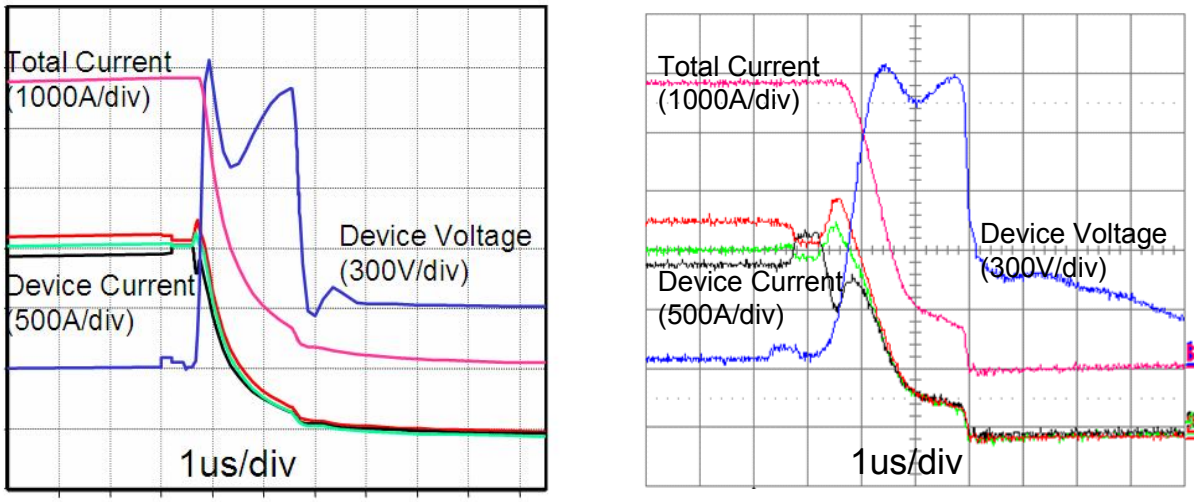


Figure 5-9 Electro-magnetic simulation vs experiment results

As the parasitic inductances are clearly identified, the side effect of the parasitics can be mitigated by reducing the unclamped loop inductance. To reduce the unclamped loop inductance, which is shown in Figure 5-10, the voltage clamping capacitor and the free-wheeling diode should be placed close to each other.

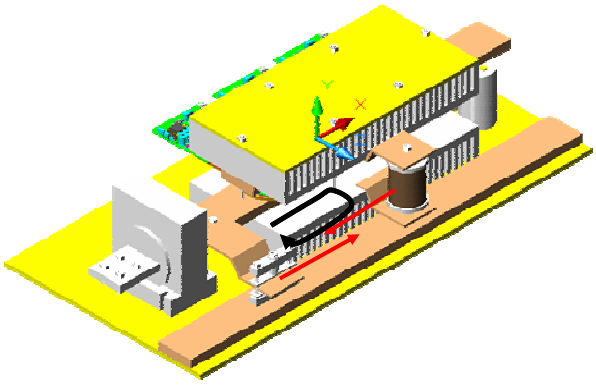


Figure 5-10 High-power IPEM structure modification to reduce the unclamped loop inductance

The circuit simulation clearly shows the effectiveness of the structure modification. The green curve is the voltage on the device before the modification; the black curve is the voltage after the modification. With reduced unclamped loop inductance, the voltage overshoot imposed on the devices is significantly reduced. The first voltage spike is caused by the unclamped loop inductance, while the second voltage spike is caused by the clamped loop inductance. The second voltage spike can be suppressed by reducing the clamped loop inductance or increasing the clamping capacitance.

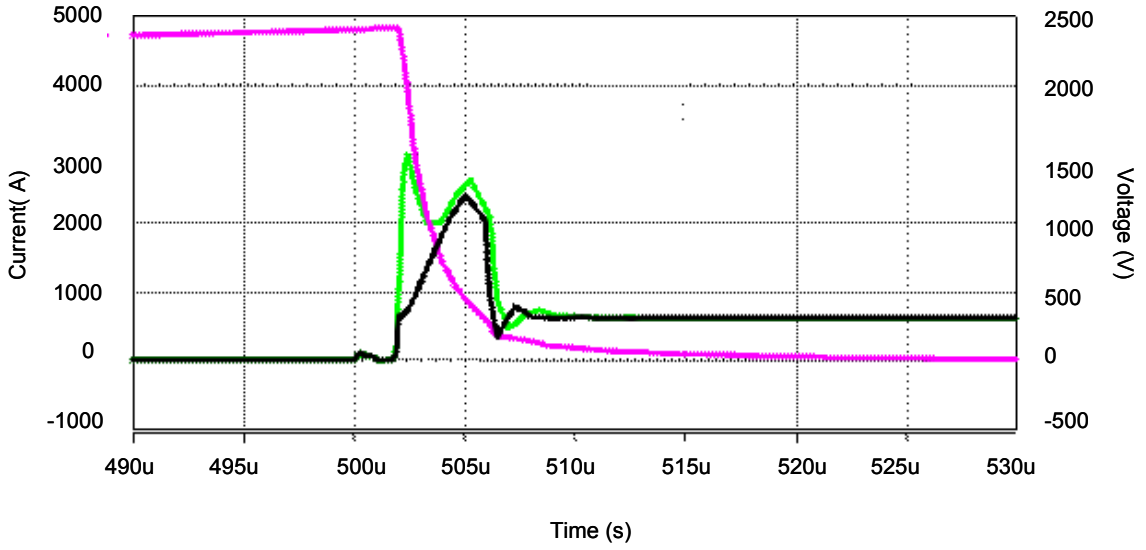


Figure 5-11 Reduced voltage spike due to structure modification

5.5 Conclusion

Parasitic inductance poses an important issue for the high-power IPEM. The Partial Element Equivalent Circuit (PEEC) is used to extract the parasitic inductance of the proposed high-power IPEM, and both field simulation and experimental results verify the effectiveness of this method.

The extracted inductance is used in the circuit simulation, which is able to evaluate the parasitic circuit interaction. Finally a modified structure is proposed which reduces the unclamped loop inductance and hence improves the circuit performance.

Chapter 6.
Electro-Thermal Modeling of High-Power Integrated Power Electronics Module (IPEM)

6.1 Introduction

The thermal properties of the IPEM are another topic in design of the power electronics module. This study systematically applies thermal modeling techniques to the 5000A high-power IPEM. With the developed thermal model, an electro-thermal simulation was conducted for the high-power IPEM. The thermal runaway phenomenon is identified in the ETO thyristor negative temperature coefficient region. Comparative study leads to the proposal of a strongly-coupled thermal network to increase the thermal stability of the high-power IPEM. The electro-thermal model is also used to calculate the DC and transient thermal limit of the high-power IPEM.

6.2 Thermal Model of High-Power IPEM

6.2.1 Heatsink Thermal Model

As the power of the IPEM increases, the power loss increases proportionally. Thus a high demand for better thermal management is imposed. In the area of high-power applications, the devices are usually cooled by liquid; however, the liquid cooling system has leakage problem and needs maintenance. As a result there are an increasing number of applications that require the use of forced convection air-cooled heatsink to control module temperature. An example of a widely-used heatsink is the parallel plate configuration shown in Figure 6-1.

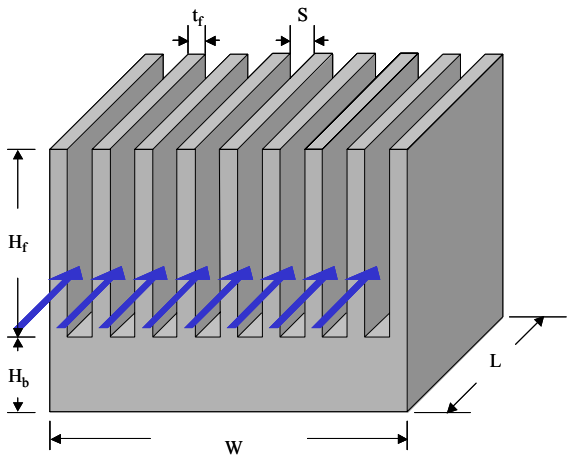


Figure 6-1 Parallel plate fin heatsink configuration

From the heatsink geometry parameters in terms of width, W, height, H, length in the flow direction, L, and fin thickness, t_{fin}, the gap, S, between the fins may be determined from

$$S = \frac{W - N_{fin} t_{fin}}{N_{fin} - 1} \qquad \text{Eq. 6-1}$$

The exposed base surface area may then be determined from

$$A_{base} = (N_{fin} - 1) SL \qquad \text{Eq. 6-2}$$

and the heat transfer area per fin from

$$A_{fin} = 2 H_f L \qquad \text{Eq. 6-3}$$

The air flow rate can be described either in terms of the average velocity, V, between the fins, or a volumetric flow rate, G. If a volumetric flow rate is used, the corresponding air velocity between the fins is

$$V = \frac{G}{N_{fin} b H_f} \qquad \text{Eq. 6-4}$$

To calculate the heat transfer coefficient acting upon the fins, several thermal dynamics equations need to be deployed.

The Prandtl number is

$$P_r = \frac{\mu \cdot c_p}{k} \qquad \text{Eq. 6-5}$$

where μ is the dynamic viscosity of air, c_p is the specific heat of air at constant pressure, and k is the thermal conductivity of air. The Reynolds number used in Eq. 6-6 is a modified-channel Reynolds number defined as

$$R_e = \frac{\rho \cdot V \cdot b}{\mu} \cdot \frac{b}{L} \qquad \text{Eq. 6-6}$$

where ρ is the density of air, μ is the thermal conductivity of the air.

$$Nu_b = \left[\frac{1}{\left(\frac{R_e P_r}{2}\right)^3} + \frac{1}{\left(0.664\sqrt{R_e} P_r^{0.33} \sqrt{1+\frac{3.65}{R_e}}\right)^3} \right]^{-0.33} \qquad \text{Eq. 6-7}$$

Eq. 6-7 is based upon a composite approximate model spanning from developing to fully-developed laminar flow regimes and was validated by Teertstra et al [A18] by comparing the model with numerical simulations over a broad range of the modified-channel Reynolds number ($0.26 < Reb < 175$) and with some experimental data as well.

The heat transfer coefficient is given by

$$h = Nu_b \cdot \frac{k}{b} \qquad \text{Eq. 6-8}$$

where k is the thermal conductivity of the heatsink material.

Assuming the heat flow in the same cross-section of the heatsink is uniform, a one-dimensional transient thermal model of the air-forced-convection heatsink can be obtained. As shown in Figure 6-2, ΔH_b is the thickness of the base chip of the heatsink; ΔH_f is the thickness of the fins chip of the heatsink. R_{bi} is conduction thermal resistance of the base chip, C_{bi} is thermal capacitance of the base chip, R_{fi} is conduction thermal resistance of the fins chip, R_{oi} is convection thermal resistance of the fins chip, C_{fi} is thermal capacitance of the fins chip, and R_o is convection thermal resistance of the open space of the heat-sink base. Connecting all the chips of the air-forced-convection heatsink, the transient model of the forced-convection air-cooled heatsink is derived, as shown in Figure 6-3.

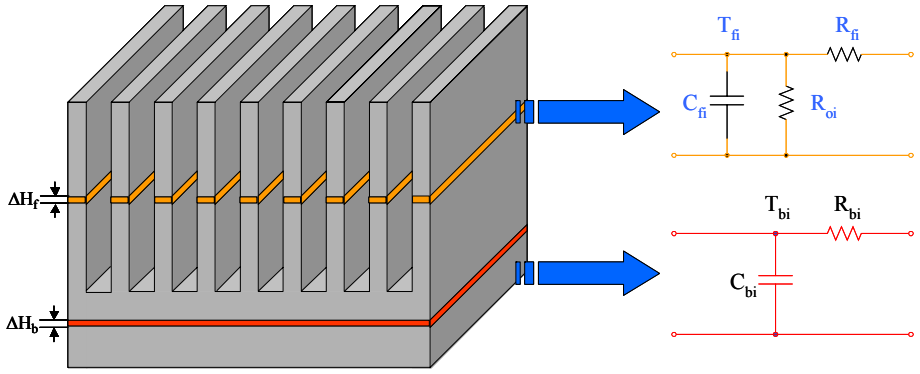


Figure 6-2. Modeling chips in forced-convection air-cooled heatsink.

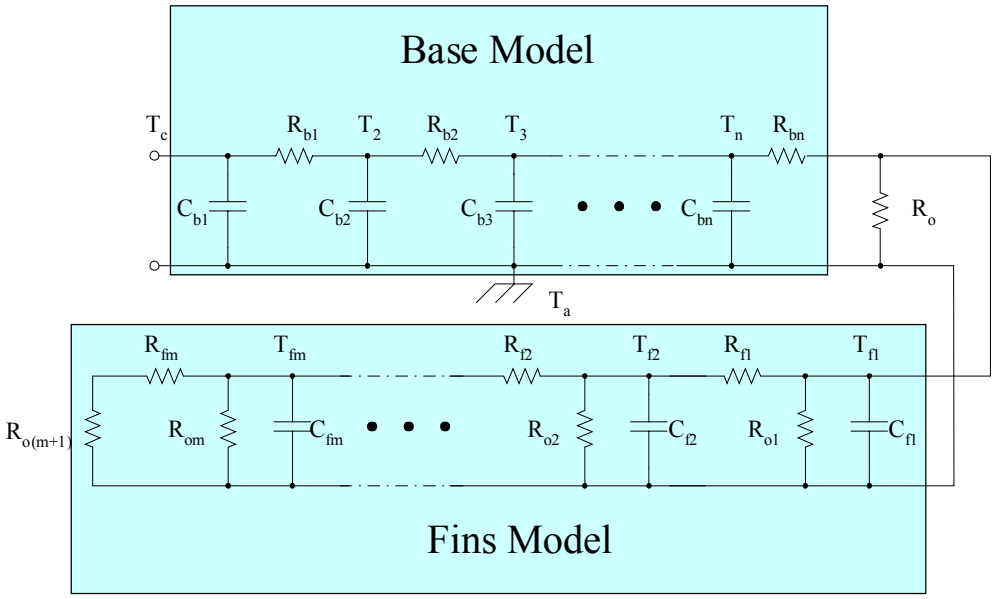


Figure 6-3. Transient thermal model of forced-convection air-cooled heatsink

The parameters in the transient thermal model of the forced-convection air-cooled heatsink can be obtained using the following equations:

$$R_{bi} = \frac{\Delta H_b}{kWL} \quad \text{Eq. 6-9}$$

$$C_{bi} = \rho c WL \Delta H_b \quad \text{Eq. 6-10}$$

$$R_{fi} = \frac{\Delta H_f}{kNt_f L} \quad \text{Eq. 6-11}$$

$$C_{fi} = \rho c Nt_f L \Delta H_f \quad \text{Eq. 6-12}$$

$$R_{oi} = \frac{1}{2hNL\Delta H_f} \quad \text{Eq. 6-13}$$

$$R_o = \frac{1}{h(W - Nt_f)L} \quad \text{Eq. 6-14}$$

where W is the width of heatsink, L is the length of the heatsink, t_f is the thickness of the fins, N is the total number of the fins, V is the air-flow velocity, k is the thermal conductivity of the material of the heatsink, ρ is the material density of the heatsink, c is the material specific heat of the heatsink, and h is the air-forced-convection heat transfer coefficient.

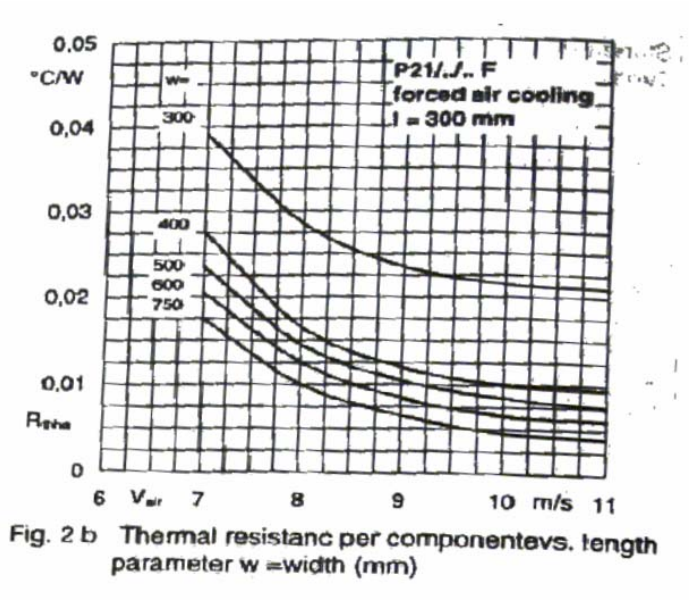


Fig. 2 b Thermal resistanc per componentevs. length parameter w =width (mm)

Figure 6-4. Heatsink thermal resistance

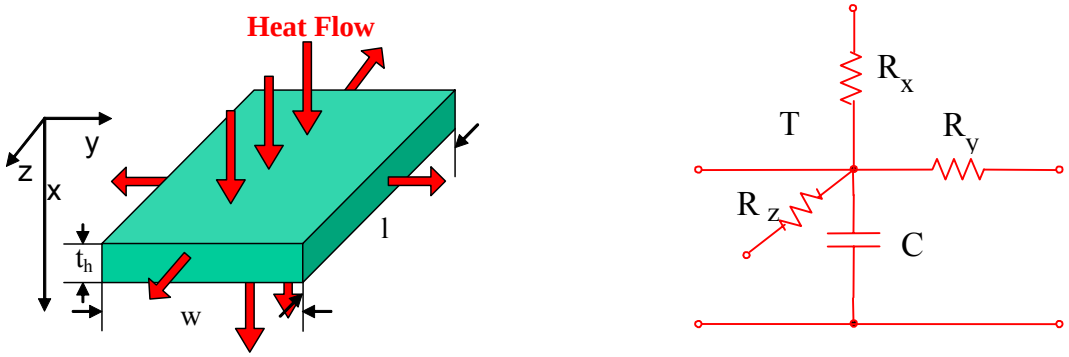
6.2.2 Heat Spreader Thermal Model

Traditionally, the 1-D thermal model assumes that the heat transfer is uniform. However, the thermal simulation shows a very strong 3-D effect in the heat spreader layer. To take the 3-D effect in consideration, the general heat equation (Eq. 6-15) is solved in 3-dimensional space, which is shown in Eq. 6-16.

$$\rho \cdot C_p \cdot \frac{\partial T}{\partial t} = \nabla \cdot \left(k \cdot \nabla T\right) + P \qquad \text{Eq. 6-15}$$

$$k \cdot \nabla^2 T = k \cdot \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) = \rho \cdot C_p \cdot \frac{\partial T}{\partial t} - P \qquad \text{Eq. 6-16}$$

Figure 6-5 shows the 3-D heat flow and equivalent thermal model, where Rx, Ry, Rz and C are represented by Eq. 6-17, Eq. 6-18, Eq. 6-19 and Eq. 6-20 respectively.



(a) 3D thermal flow chart (b) 3D thermal model

Figure 6-5 3D thermal model

$$R_x = \frac{t_h}{k \cdot w \cdot l} \qquad \text{Eq. 6-17}$$

$$R_y = \frac{w}{k \cdot t_h \cdot l} \qquad \text{Eq. 6-18}$$

$$R_z = \frac{l}{k \cdot t_h \cdot w} \qquad \text{Eq. 6-19}$$

$$C = c \cdot \rho \cdot t_h \cdot w \cdot l \qquad \text{Eq. 6-20}$$

Figure 6-6 shows the simulated heat flow in the heat spreader layer.

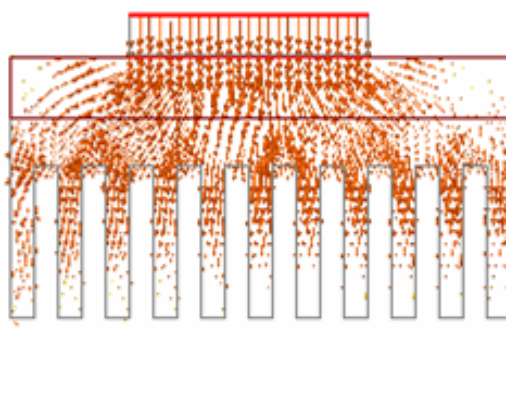


Figure 6-6 Simulated heat flow in the heat spreader layer (XY section view)

6.2.3 Device Thermal Model

The device thermal model can be extracted from the geometry of the device. Figure 6-7 shows the internal structure of a GTO device. It consists of five layers of disks. The anode is a copper disk, which is on top of a molybdenum disk. The engraved channel is for gate ring connections. The molybdenum layer has similar Coefficient of Temperature Expansion (CTE) as the silicon layer. Another molybdenum layer and copper layer are on the cathode side of the silicon GTO.

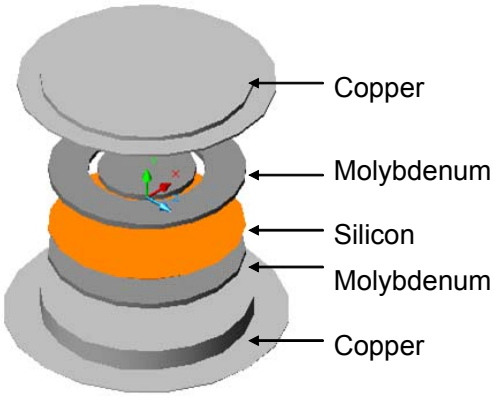


Figure 6-7 Exposed view of the GTO internal structure

The equivalent thermal model is extracted and shown in Figure 6-8.

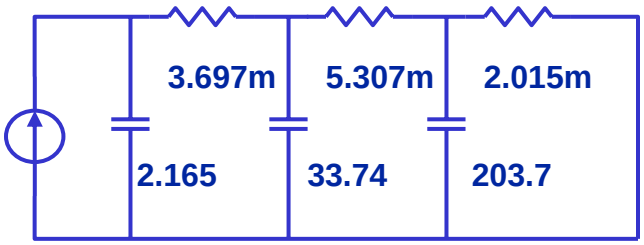


Figure 6-8 Device thermal impedance network

The ETO device has a unique device structure, which is shown in Figure 6-9. Two copper disks are used on the GTO cathode side for both electrical conduction and thermal conduction. A thin layer of insulator is inserted between the two copper disks. This feature increases the thermal impedance on the cathode side and inherently diverts the thermal flow to the anode side.

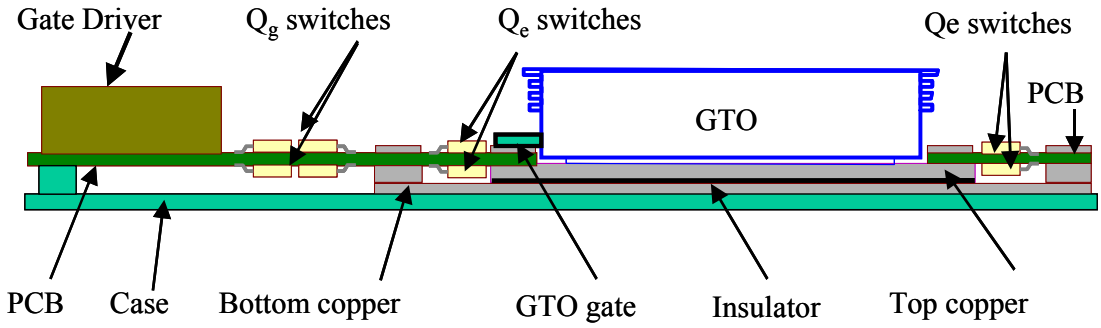


Figure 6-9 Cross-section view of the ETO internal structure

Figure 6-10 shows the static thermal impedance model of the ETO device, where the thermal resistance of copper disks and thermal resistance of insulator layer are included. A thermal contact resistance is also included in this model.

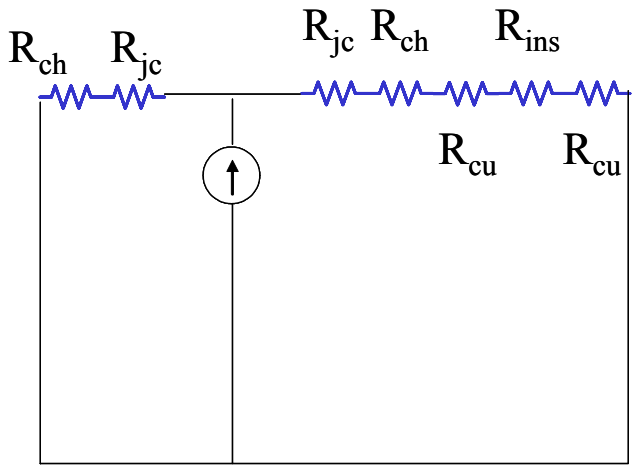


Figure 6-10 Static thermal impedance of the ETO

6.2.4 High-Power IPEM Thermal Model

With the developed heatsink thermal model, heat spreader thermal model and device thermal model, the high-power IPEM thermal model is shown in Figure 6-11.

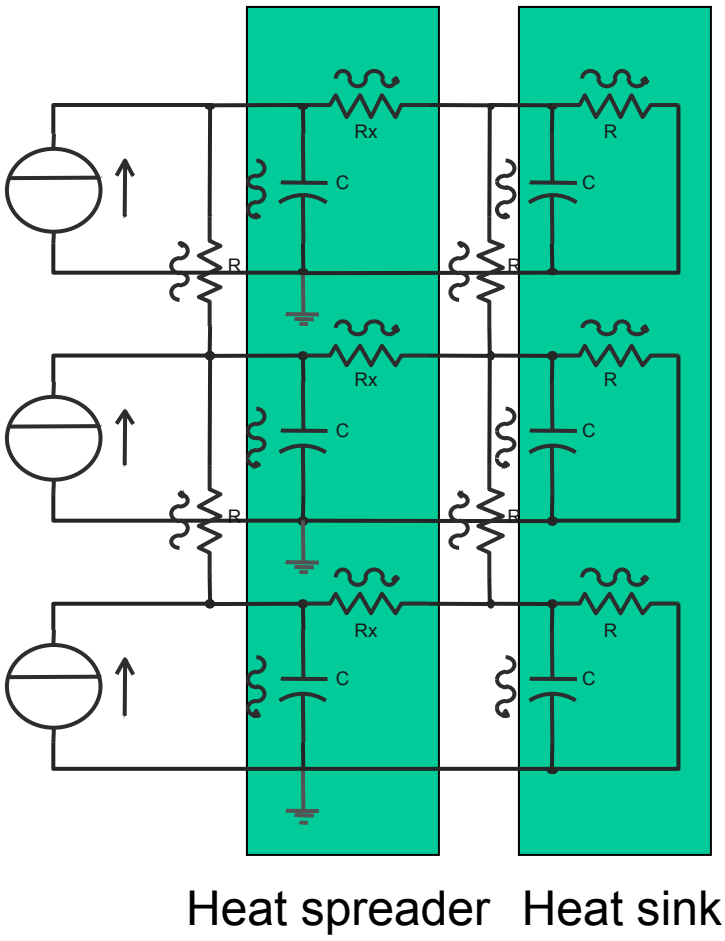
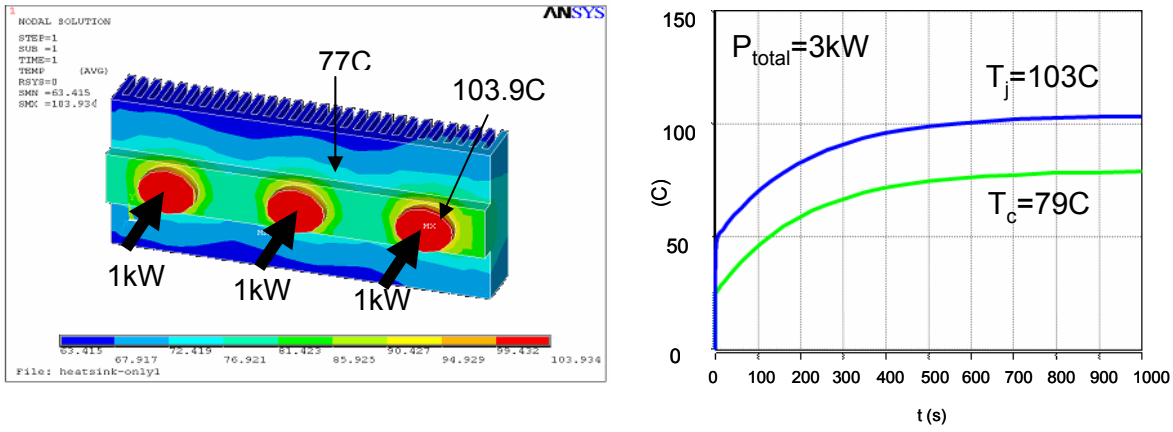


Figure 6-11 High-power IPEM thermal impedance network

This high-power IPEM thermal model is simulated under a specific load condition, which is 1kW power loss per ETO device. The model gives a dynamic temperature profile of the thermal network. The steady state of the ETO junction temperature is 103^{o}C, and the heatsink case temperature is 79^{o}C. The circuit simulation of the thermal network is shown in Figure 6-12 (b). The finite element analysis of the thermal network gives a 3D temperature distribution of the high-power IPEM, which is shown in Figure 6-12 (a). The device junction temperature is

103.9°C and the heatsink case temperature is 77°C. These two simulation results match each other.



(a)Finite element analysis of the thermal network (b)Circuit simulation of the thermal network

Figure 6-12 High-power IPEM thermal model simulation

6.3 Electro-Thermal Coupling

The electro-thermal interaction is another important issue in the high-power IPEM. The thyristor is known to have "current crowding" related thermal instability. The phenomenon is studied for the ETO device. In order to study the current crowding, first the electrical properties of the ETO device are characterized. Figure 6-13 shows the tested I-V curves. High-voltage GTOs are more likely to have a more resistive I-V characteristic than low-voltage GTOs and are therefore desirable for static current sharing. For the ETO, the series-connected MOSFET, which behaves like an emitter ballast resistor, makes the ETO's I-V characteristic even more resistive and therefore favorable in terms of static current sharing.

To avoid positive feedback of current crowding, a positive temperature coefficient I-V is very important. Typical high-voltage GTOs have this feature above a critical current value. For the ETO, this critical current value moves to lower currents because of the strong positive temperature coefficient of the series-connected MOSFETs. Figure 6-13 shows measured ETO4045TA forward drops at different temperatures as well as the contribution of the MOSFET Q_E. For the measured ETO, positive temperature coefficient is obtained at above 500A, while this point for the GTO is about 1000A. Static current sharing of parallel ETOs above 500A is therefore guaranteed for this type of ETO devices.

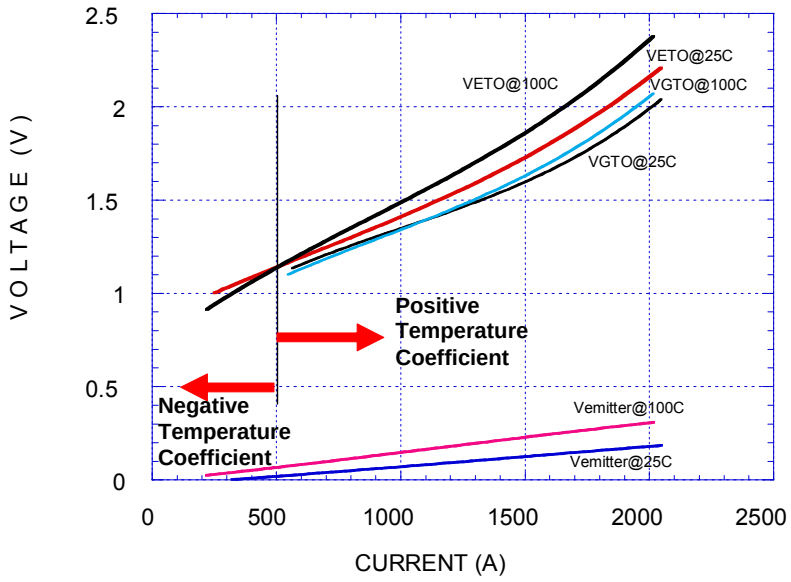


Figure 6-13 Device I-V curve temperature coefficient

An electro-thermal model is built to take in consideration of the temperature-dependant coefficient. Together with the high-power IPEM thermal model, the electro-thermal simulation is conducted to investigate the electrical and thermal interaction.

This method is used to evaluate two designs of the high-power IPEM. Design I utilized a separate heatsink approach for the module as shown in Figure 6-14, while Design II utilizes a shared heatsink, which is shown in Figure 6-15.

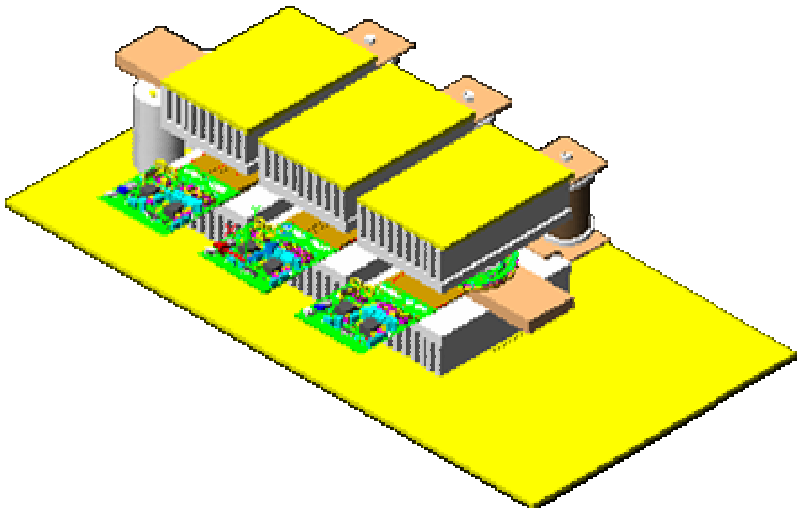


Figure 6-14 Design I: separate Heatsink

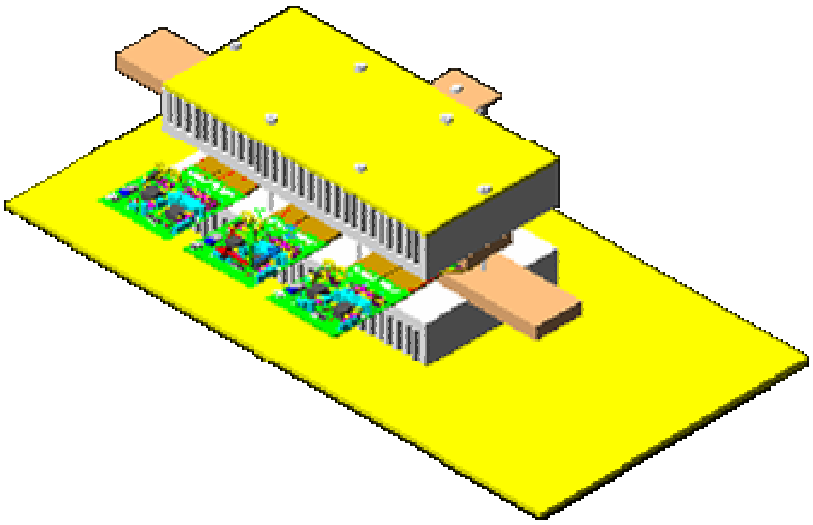


Figure 6-15 Design II: shared Heatsink

The simulation results indicate the thermal instability in Design I commonly known as "thermal runaway" phenomenon. In the device's negative temperature region, the large current device generates more power loss, and hence has higher junction temperature, which results in a low voltage drop on the device, which in turn draws more current into the device. The intrinsic positive feedback mechanism is clearly shown in Figure 6-16. The junction temperature rise is higher for the large current device. The current distribution in three devices is unbalanced; the large current device takes about 2/3 of the total current, while 1/3 of the total current is shared by the other two devices. Figure 6-17 is the simulation results for the shared heatsink, which has strong thermal coupling among the devices. The coupling thermal resistance balances the device junction temperature. The device current difference is dedicated by the device static I-V characteristics, which are all within a 10% range.

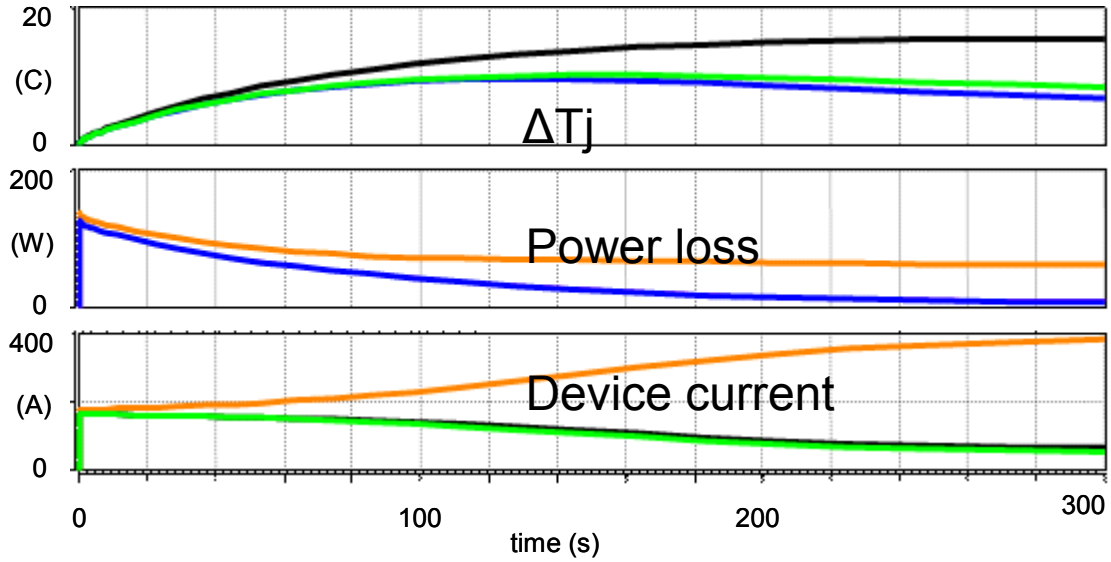


Figure 6-16 Simulation of Design I: separate heatsink

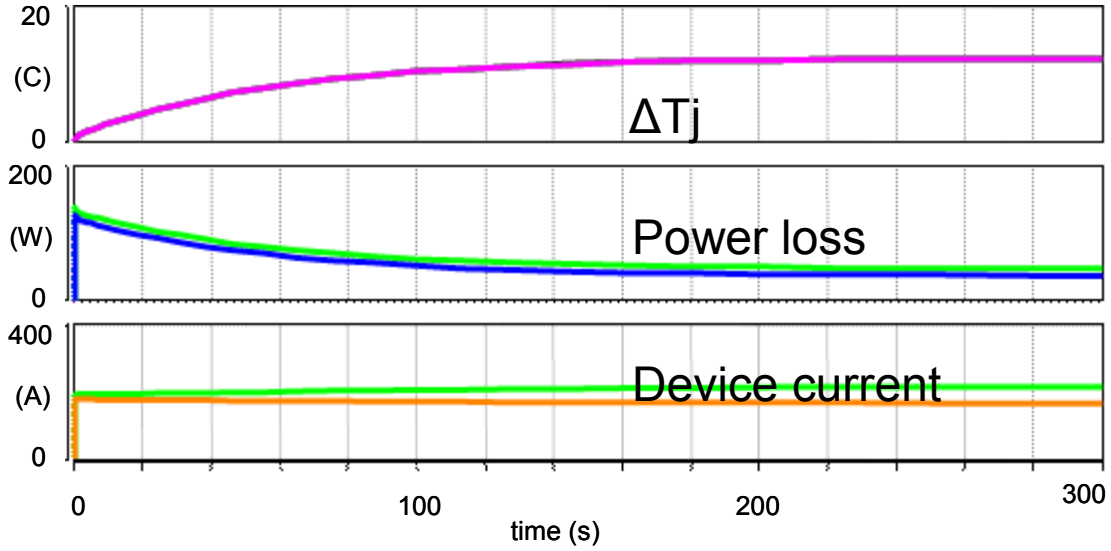


Figure 6-17 Simulation of Design II: shared heatsink

6.4 Thermal Limit of High-Power IPEM

Electro-thermal simulation is also used to verify the high-power IPEM thermal design. One of the thermal requirements is 5000A overload operation for 1 minute. This scenario is simulated using the developed device model combined with the thermal model of the high-power IPEM. Figure 6-18 shows the simulated device loss and junction temperature under 5000A overload operation. The high-power IPEM is initially operated at rated current 2500A for 30 minutes until it reaches a thermal steady state, and then is followed by a 200% overload operation, which is 5000A for 1 minute; finally the high-power IPEM is reduced to normal condition. The pink curve shows the power loss profile during the operation. The blue curve shows the transient device junction temperature, which reaches 125°C at the end of the overload operation. The green curve, case temperature, shows a modest temperature rise. This simulation verifies that the designed high-power IPEM meets the thermal requirements.

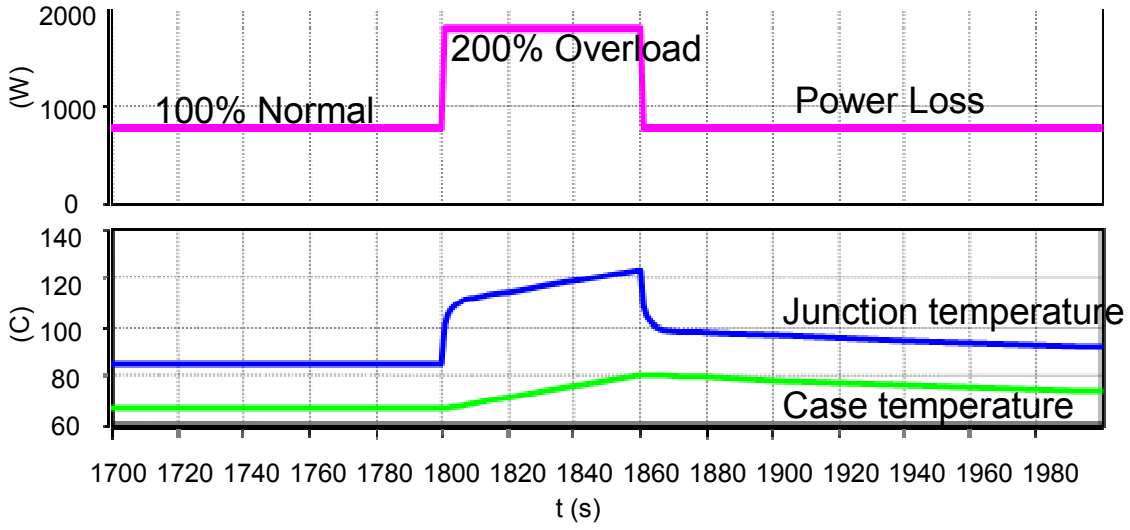


Figure 6-18 Electro-thermal simulation of 5000A one-minute overload operation

The electro-thermal simulation can further extract the Time-Current-Characteristics (TCC) of the high-power IPEM. Figure 6-20 shows the extracted TCC curve of the IPEM. This is obtained by using a maximum junction temperature of 125^{o}C as the criteria and the maximum operation time allowed is extracted from Figure 6-19. The maximum operation time allowed is the time current characteristics of the designed high-power IPEM which is shown in Figure 6-20.

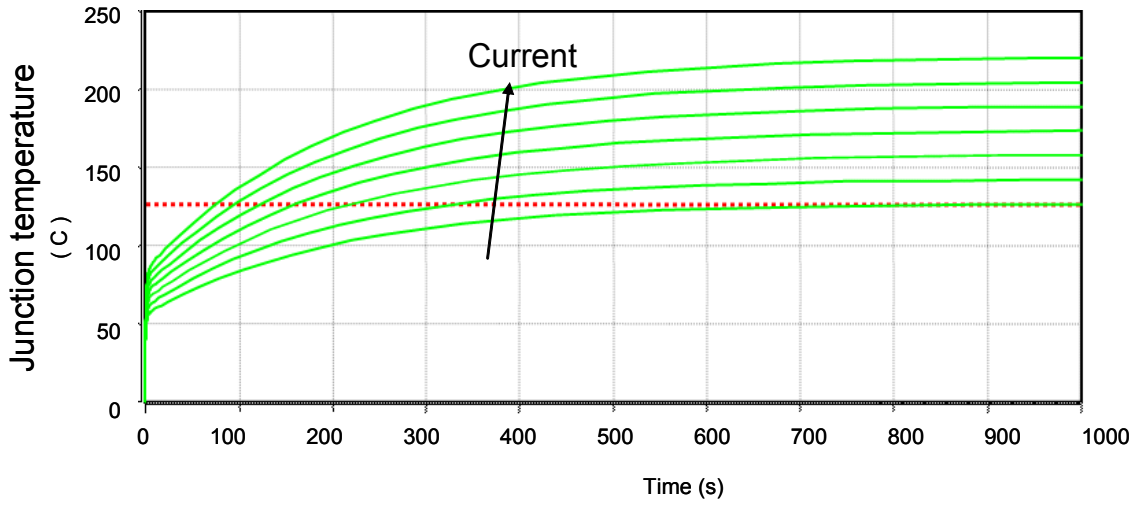


Figure 6-19 ETO device junction temperature under different load conditions

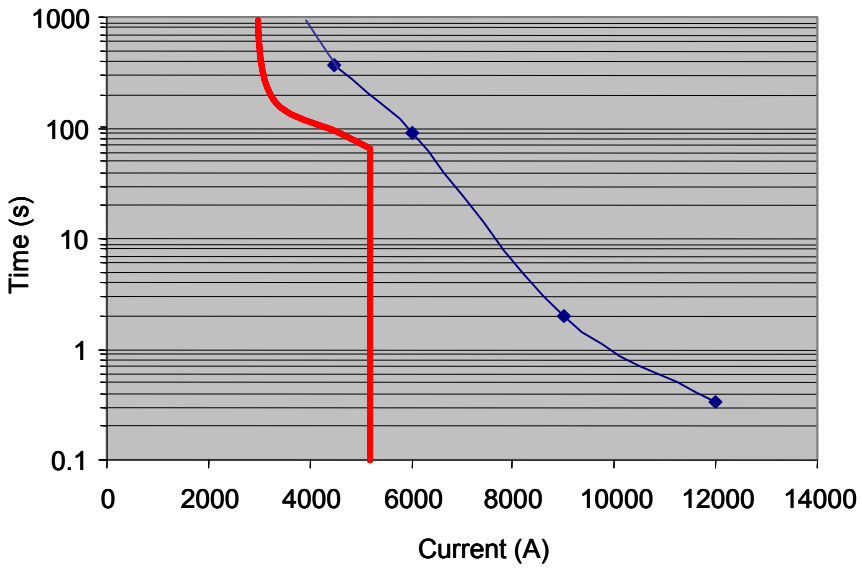


Figure 6-20 High-power IPEM TCC curve

The blue curve in Figure 6-20 shows the extracted high-power IPEM TCC curve. The red curve represents the required trip settings. Figure 6-20 shows the thermal limit of the developed high-power IPEM exceeds the designed trip limit hence the device can be classified as a 5000A high-power IPEM.

6.5 Conclusion

The thermal network of the 5000A high-power IPEM has been systematically modeled. The Computational Fluid Dynamic (CFD) included discrete model is developed for the force-convection heatsink. A heat spreader layer is used to improve the thermal performance of the high-power IPEM. The 3-D thermal model is developed for the heat spreader. The ETO device thermal model is also developed for the first time.

Electro-thermal modeling of the high-power IPEM indicates the "thermal runaway" problem in the IPEM. The tested device I-V characteristics reveal a negative temperature range for the ETO device. The electro-thermal simulation allows an evaluation of two different design approaches and it was found that a shared heatsink design provides strong electro-thermal coupling, and has better thermal stability than a separate heatsink design in the high-power IPEM. The electro-thermal model is also used to calculate the DC and transient thermal limit of the high-power IPEM. The extracted TCC curve is used to define the tripping characteristic of the high-power IPEM based circuit breaker.

Chapter 7.
High-Speed Solid-State DC Circuit Breaker Based on Developed High-Power IPEM

7.1 Introduction

Utility engineers faced with the challenges of integrating new power generations into existing power systems, clearing faults more quickly or finding an alternative to SF6 breakers will soon have a new product to meet all of their needs: a solid-state current-limiting circuit breaker. Electric utilities have long wished for a practical, reasonably-priced, solid-state circuit breaker which could provide very reliable service with little maintenance [A3].

Solid-state circuit breakers offer a fast response using modern power semiconductor devices. Their current interruption time varies from 5μs to 1000μs based on the different power semiconductor devices used. The solid-state circuit breaker generates no arc during current interruption, and is hence maintenance-free. However, it has higher on-state conduction loss than a mechanical circuit breaker. The limited voltage and current ratings also hinder the popularity of the solid-state circuit breaker.

The developed high-power IPEM uses multiple devices in parallel to extend the current rating, and uses multiple devices in series to extend the voltage rating. The compact design offers reduced parasitics, and the integrated heatsink provides effective thermal management. The electrical, magnetic and thermal modeling and analysis of the high-power IPEM are discussed in the previous chapters.

This chapter focuses on the utilization of the developed high-power IPEM in a solid-state circuit breaker. Section 7.2 proposes several novel topologies for a DC circuit breaker. Section 7.3 discusses the design considerations, such as spike suppression, current sensing and tripping circuit. The physical implementation of the solid-state circuit breaker and other variations are described in Section 7.4. A brief conclusion is drawn in section 7.5.

7.2 Novel Topologies

Traditionally, the DC circuit breaker is treated as a one-port network. It behaves as a Single Pole Single Throw (SPST) DC switch. When the DC circuit breaker opens, it cuts off the current path, thus initializing an arc between the contacts of the circuit breaker until the energy stored in the stray inductance is completely released through the arcing. The circuit is completely interrupted. An arc chute, vacuum or other insulating media such as SF6 or mineral oil could be used to suppress the arc. The arc often causes severe burn on the contacts which consequently need routine maintenance.

The above approach does not work in the case of a solid state circuit breaker due to the limited voltage capability of power switches. Over-voltage must not be allowed. The energy stored in the parasitic inductance must be absorbed by additional parts. This proposed solid-state circuit breaker uses a two-port network approach. Figure 7-1 shows one possible configuration of the solid-state DC circuit breaker. The DC voltage source is connected to a load through the solid-state circuit breaker. The solid-state circuit breaker consists of an input clamping capacitor connected across the DC voltage source, which absorbs the up-stream inductor energy during current interruption; an RCD clamp connected across the DC voltage source, which limits the

voltage spike on the IPEM; and a free-wheeling diode connected across the load, which is used to provide an alternative path for the load current. Hence functionally a single switch function will have to be performed by a high-power IPEM defined in the dash line. Because the IPEM withstands a high voltage stress during current interruption, it requires a large clamping capacitor particularly at high current ratings. This configuration is suitable for high-current DC circuit breaker applications. The clamp can be replaced by another voltage-limiting device, such as a Metal Oxide Varistor (MOV). The IPEM connects the positive terminal of the DC voltage source to the positive terminal of the load. The load is represented as an inductor because most of the industrial load is inductive.

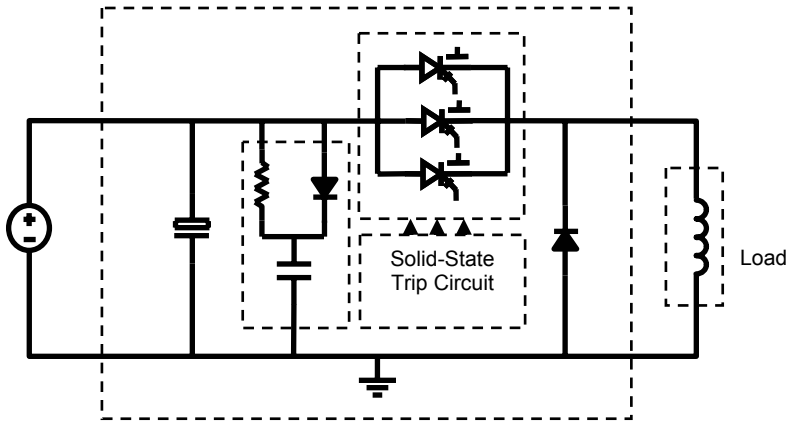


Figure 7-1 Novel solid-state DC circuit breaker with voltage clamp

Figure 7-2 shows another possible configuration of the solid-state DC circuit breaker. The DC voltage source is connected to a load through the solid-state circuit breaker. The solid-state circuit breaker in this configuration consists of an input clamping capacitor connected across the DC voltage source, which absorbs the up-stream inductor energy during current interruption; an RCD snubber connected across the IPEM, which is used to limit the voltage spike on the IPEM;

and a free-wheeling diode, which provides an alternative path for the load current. This configuration adopts the RCD snubber to limit the voltage spike by providing a commutation path for the interrupted current. The dv/dt slope can be adjusted by the proper choice of the snubber capacitor. The RCD snubber can be replaced by another voltage-limiting device, such as a MOV. The IPEM withstands low voltage stress during current interruption. This configuration is suitable for high-voltage, high-current DC circuit breaker applications.

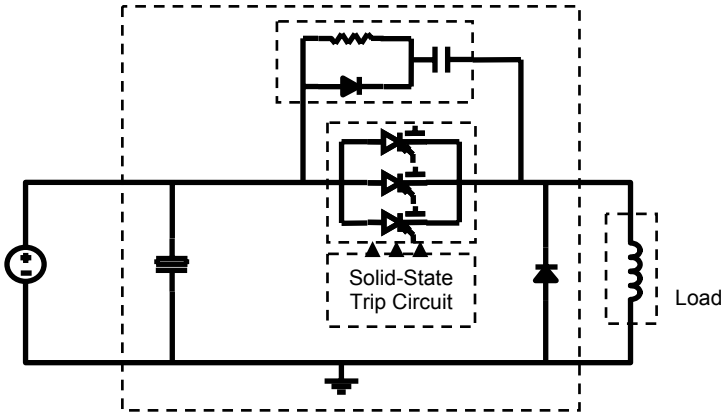


Figure 7-2 Novel solid-state DC circuit breaker with RCD snubber

Figure 7-3 shows a third possible configuration of the solid-state circuit breaker. In this configuration, the solid-state circuit breaker consists of an RC snubber connected in parallel with the IPEM, which is used to limit the voltage spike on the IPEM; and an anti-parallel diode, which is used to provide a reverse current path for the load during regeneration. The anti-parallel diode replaces the free-wheeling diode in the first two configurations. The dv/dt slope can be adjusted by proper choice of the snubber capacitor. The IPEM withstands low voltage stress during current interruption. This configuration is suitable for high-voltage DC circuit breaker applications.

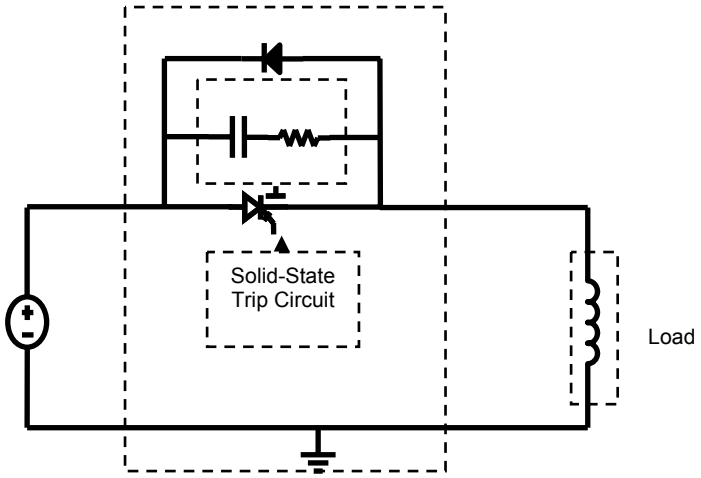
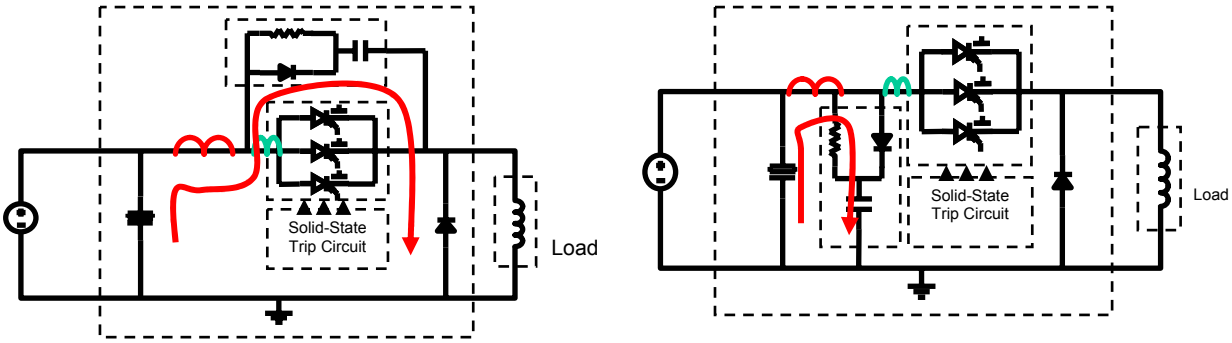


Figure 7-3 Novel solid-state DC circuit breaker with RC snubber

7.3 Design Considerations

7.3.1 Voltage Stress Suppression

These different configurations are evaluated experimentally. Figure 7-4 shows the first two configurations of the proposed solid-state DC circuit breaker. Figure 7-4 (a) shows the solid-state DC circuit breaker with a RCD snubber, while Figure 7-4 (b) shows the solid-state DC circuit breaker with a voltage clamp. Two parasitic loop inductances are included in the schematic. The red curve shows the current flow caused by the main parasitic inductance during the current interruption.



(a)Solid-state DC circuit breaker with RCD snubber (a)Solid-state DC circuit breaker with voltage clamp

Figure 7-4 Snubbering vs clamping effect schematic

Figure 7-5 shows the test results of the two configurations. The test conditions are the same for both configurations; the bus voltage is 250V; the current interruption setting is 1000A.

The blue curve is the voltage signal on the IPEM and the green curve is the current signal flowing through the IPEM. As shown in Figure 7-5, there is an oscillation when a RCD snubber is used. This phenomenon is especially severe when the circuit breaker is used in a high-current, low-voltage condition. As indicated in Figure 7-4 (a), the oscillation path is shown as the red curve, which is between the loop parasitic inductance and the snubber capacitor. The snubber also limits the dv/dt slope of the IPEM. The slowly-charged voltage on the IPEM results in a long current tail. However, the voltage spike on the IPEM exhibits approximately the same amplitude in these two cases, which means the voltage clamp can be effectively used in the high-current, low-voltage circuit breaker applications. When the solid-state circuit breaker is used in a high-voltage, low-current applications, the snubber is more effective in suppressing the voltage spike.

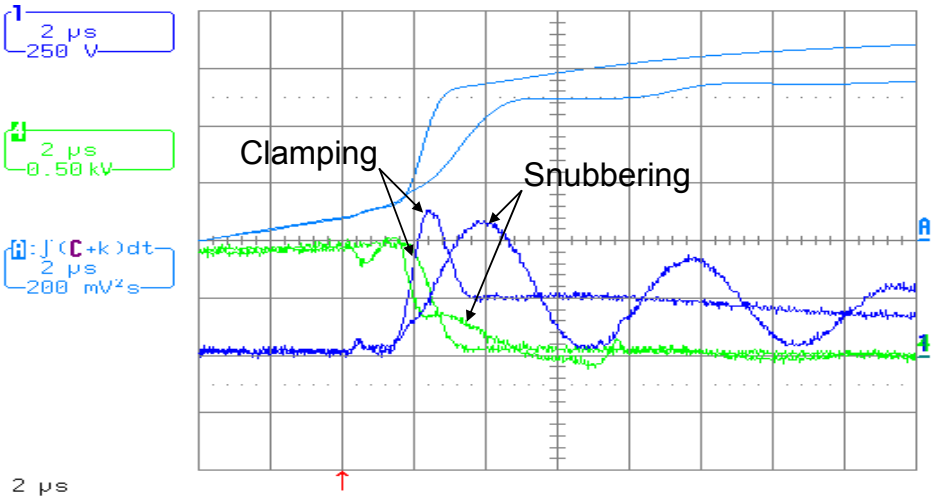


Figure 7-5 Snubbering vs clamping test results

7.3.2 Current Sensing

One feature of the high-power IPEM is the built-in current sensor. The ETO built-in current sensor [B11] can be used for overcurrent protection. However, the MOSFET resistance exhibits high temperature-dependence. As shown in Figure 7-6, the sensed MOSFET voltage signal varies with the temperature under the same current. Eq. 7-1 is the measured MOSFET temperature coefficient.

$$R = R_0 + \alpha T = 68.25\mu\Omega + 0.5\mu\Omega \cdot T \qquad \text{Eq. 7-1}$$

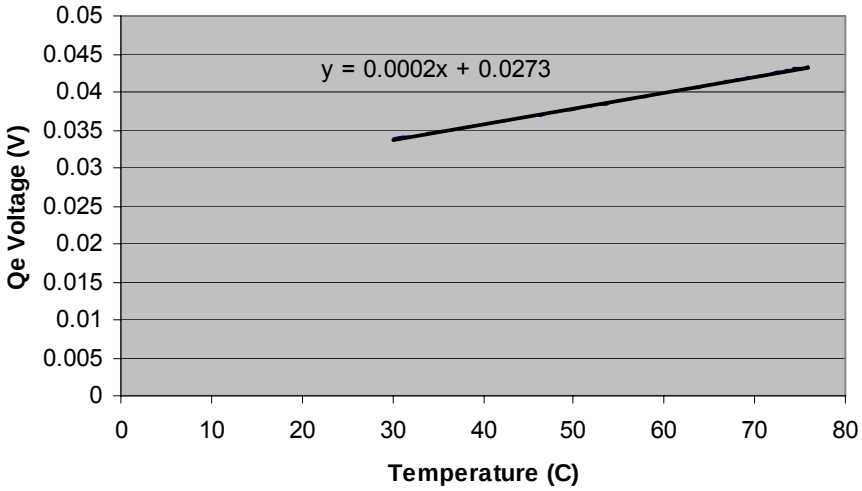


Figure 7-6 Temperature coefficient of the sensor Q_E MOSFET

Different compensation strategies have been evaluated and compared. Two signals were sampled; one is the emitter MOSFET Q_E drain-to-source voltage, the other is the emitter MOSFET Q_E temperature. Eq. 7-2 shows the first compensation method, which uses a divider to compensate the MOSFET resistance temperature coefficient. Eq. 7-3 shows the second compensation method which is the approximation of the first method, using a multiplier for compensation, a and b are the linear approximation of the MOSFET conductance. Eq. 7-4 decouples the Eq. 7-3 at the nominal operation point, where a,b is the coefficient of the Taylor series expansion. The first two methods require a microprocessor to calculate the current information, while the third method can be easily implemented by an analog circuit for protection purposes. These different compensation methods are compared in Figure 7-7. A 400A pulse is used in the test; the first method reconstructs the current signal precisely. The second

compensation gives a rough current signal within a 10% error range; the third compensation can only be used for protection purposes. The uncompensated current gives a large error.

$$I = \frac{V_{QE}}{R_0 + \alpha T} \qquad \text{Eq. 7-2}$$

$$I = V_{QE}\left(a + bT\right) \qquad \text{Eq. 7-3}$$

$$I = a\left(V_{QE} - bT\right) \qquad \text{Eq. 7-4}$$

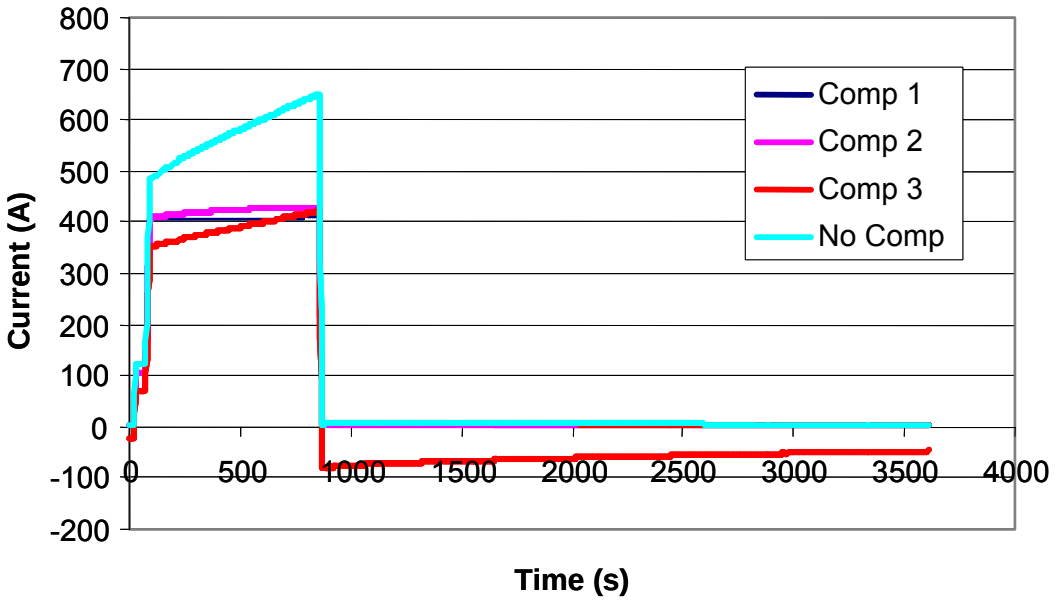


Figure 7-7 Temperature compensation comparison

7.3.3 Trip Unit

The trip unit considered here is an integral part of the circuit breaker. It may be electromechanical (thermal-magnetic) or solid-state electronic. By continually monitoring the current flowing through the circuit breaker, it will sense abnormal current conditions. Depending on the magnitude of the current, the trip unit will initiate an inverse-time response (I^2t tripping) or an instantaneous response. This action will cause a direct acting operating mechanism to open the circuit breaker contacts and interrupt current flow.

The basic function of the trip unit is to provide the long-time current-time delay (I^2t function) and instantaneous current response characteristics necessary for proper circuit protection. The combination of these characteristics provides time delay to override transient overloads; delayed tripping for sustained overloads, low-level short circuits, or ground faults of sufficient magnitude to cause overcurrent response; and instantaneous tripping for higher level short circuits or ground faults.

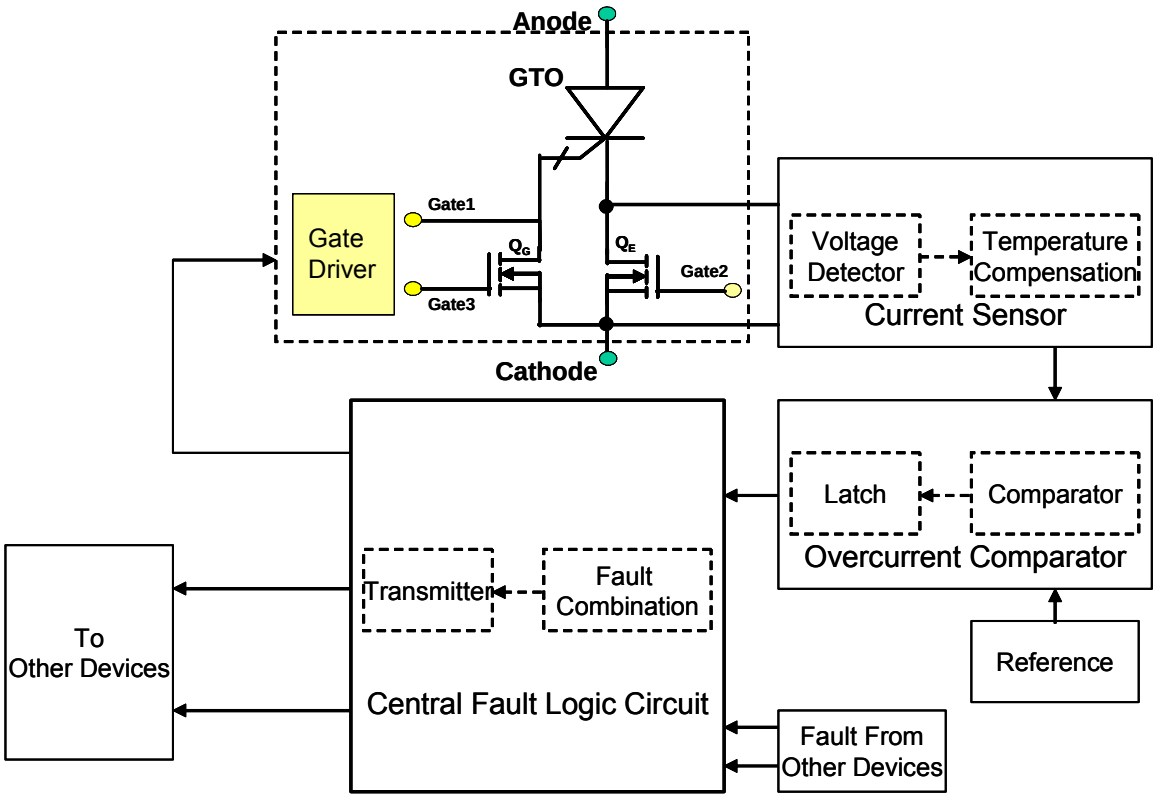


Figure 7-8 Solid-state trip circuit

Figure 7-8 shows the solid-state trip circuit used in final solid-state circuit breaker. A current sensor circuit detects the emitter switch voltage of the ETO thyristor. The current sensor includes a voltage sensor and a temperature compensation circuit. The current sensor circuit, after temperature compensation, calculates the conduction current. The overcurrent comparator compares the device current from the current sensor with a precise voltage reference. the overcurrent comparator includes a comparator and a latch. If the device current exceeds the predetermined reference, the overcurrent comparator will generate a fault signal and latch it. A central fault logic circuit receives the fault signal from the overcurrent comparator and fault signals from other devices. The central fault logic circuit includes a fault combination circuit and

a transmitter. After the fault combination, the central fault logic circuit transmits the fault signal to all the ETO devices, shutting down the ETO devices and interrupting the fault current. While the solid-state trip circuit utilizes the device's built-in current sensor, it does not exclude the use of the external current sensor, for instance, Hall-effect current sensor located in the load side to replace the current sensor.

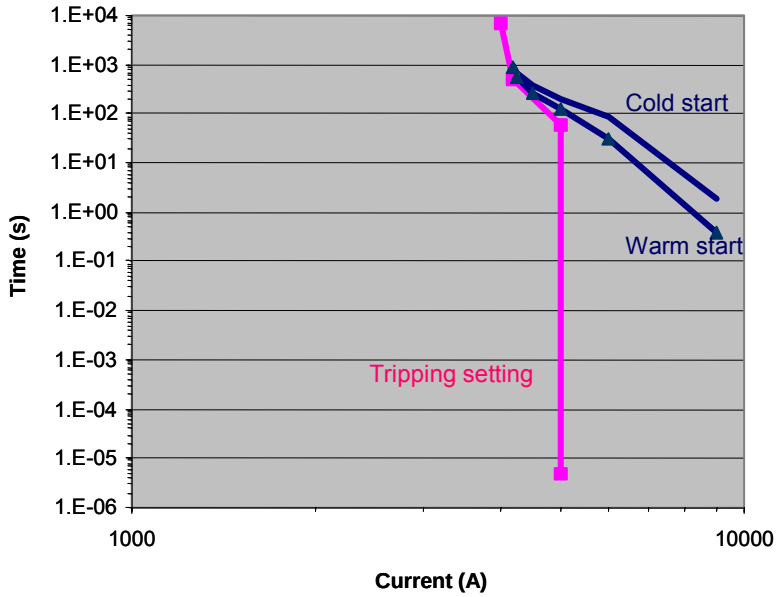


Figure 7-9 Tripping setting curve

The tripping setting is shown in the pink curve in Figure 7-9. The solid-state DC circuit breaker time-current-characteristics (TCC) are shown in the blue curve. The triangle marked blue curve represents the warm start of the circuit breaker, and the other blue curve represents the cold start of the circuit breaker.

7.3.3.1 INSTANTANEOUS TRIPPING

Ground faults, for minimum damage, must be cleared as quickly as possible regardless of their magnitude. The setting point of instantaneous tripping is determined by the load

characteristics and limited by the maximum controllable interruption current of the circuit breaker. The target application of the solid-state DC circuit breaker is a solid-state rectifier for a 2500A mining trolley system. To protect the solid-state rectifier, a maximum 5000A trip setting is chosen. The instantaneous tripping is two times of the rectifier rated current. Taking the current unbalancing into consideration, the maximum controllable current for the solid-state DC circuit breaker is 9000A, which is well above the setting point.

7.3.3.2 I^2T TRIPPING

The concept of I^2t has been introduced for protections because it represents the actual thermal stresses imposed on equipment carrying short-circuit current in the first few cycles. The quantity I^2t represents $\int i^2 dt$, the time integral of the current squared for the time under consideration.

The use of I^2t tripping is two-fold. The first aspect is to increase the system operation capability until the apparatus is thermal limited. The second aspect is to improve the power system availability for providing coordination with downstream or upstream circuit breakers.

The I^2t tripping setting is again determined by the load characteristics. The load is specified as 150% overload for 2 hours and 200% for 1 minute. A setting point of 4000A with 2 hours delay and 5000A with 1 minute delay is shown in Figure 7-9 pink curve. The I^2t tripping curve is within the thermal limitation of the solid-state DC circuit breaker TCC.

The I^2t function can be implemented by an analog circuit or a digital signal processor.

7.3.3.3 AUTO RECLOSING

Auto reclosing is required for the circuit breaker in order to further increase the power system availability by reclosing the circuit breaker after fault tripping. This function is useful when the fault is cleared before the reclosing. However, if the fault is permanent, the reclosing is destructive and causes greater disturbance to the power system. The designed solid-state circuit breaker implements the auto reclosing function, while mitigating the negative effect because the high-speed interruption of the fault current can successfully limit the initiated fault current to below a controllable level, hence causing virtually no disturbance to the power system.

7.4 Implementation

The protection of a 2500A solid-state rectifier in a mining trolley system requires a 5000A instantaneous tripping capability and specified overload capability as shown in Figure 7-9 pink curve. Therefore it demands a protection device with higher current rating and higher overload capability. Figure 7-9 blue curves show that the TCC of the developed high-power IPEM meets the requirements. A 5000A solid-state circuit breaker was implemented using the developed high-power IPEM as shown in Figure 7-10. The solid-state circuit breaker utilizes the first configuration as shown in Figure 7-1. An external current sensor is used for precise protection. The inclusion of the high-power IPEM significantly simplifies the design and construction effort, which results in a compact solid-state DC circuit breaker.

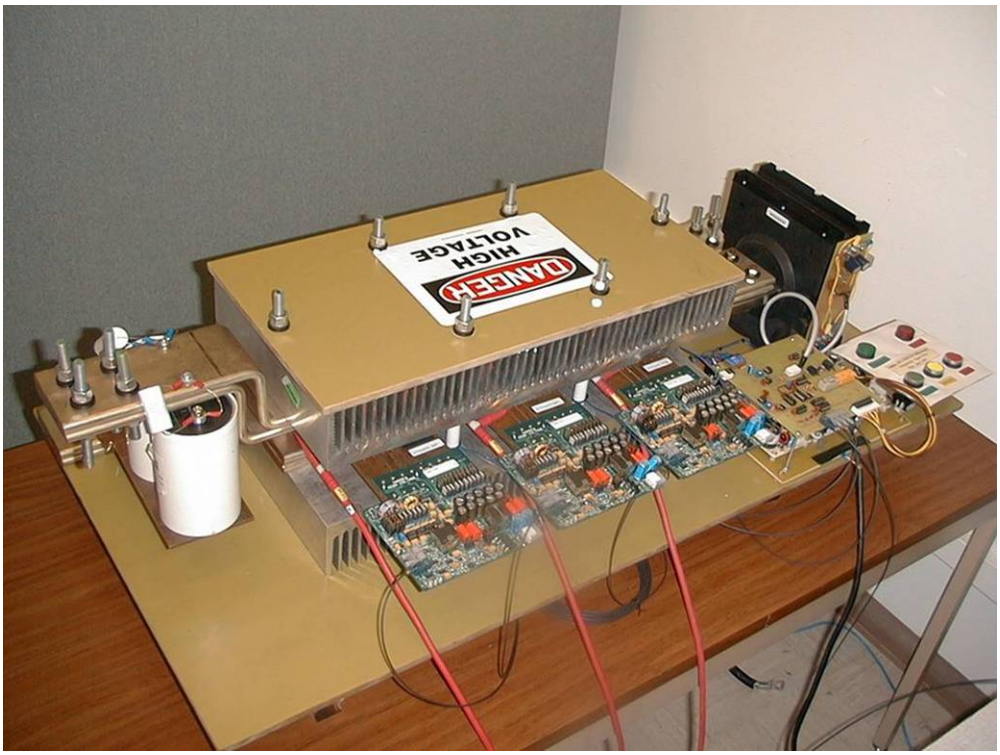


Figure 7-10 Physical implementation of a 5000A solid-state DC circuit breaker

The 5000A solid-state circuit breaker shows a full rating current interruption within 5μs (Figure 7-11). The current unbalancing issue is solved internally. The experimental results show a promising and unprecedented high-current, high-speed circuit breaker for critical industrial applications.

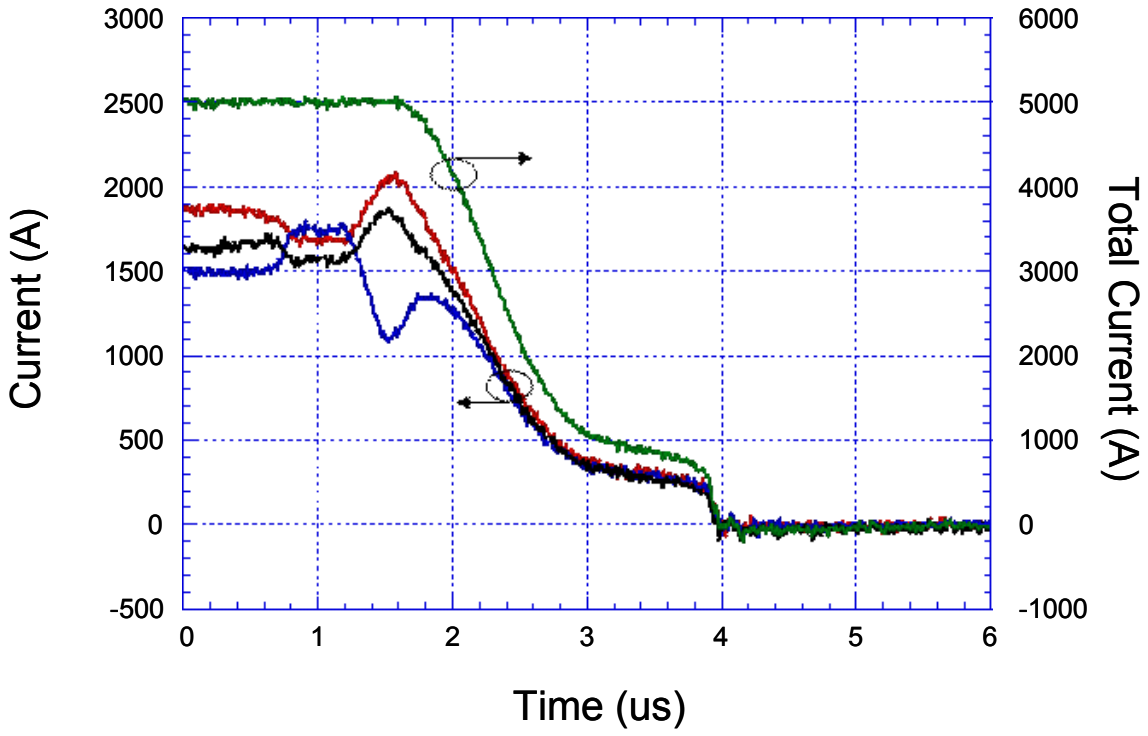


Figure 7-11 Experimental demonstration of a 5000A solid-state DC circuit breaker

Figure 7-12 shows the third configuration of high-voltage solid-state circuit breaker [B9]. The built-in current sensor is enabled. The 3000V, 1700A solid-state DC circuit breaker uses a minimum number of parts, and offers a low-cost and compact design. This circuit breaker has been used in industrial converter protection.

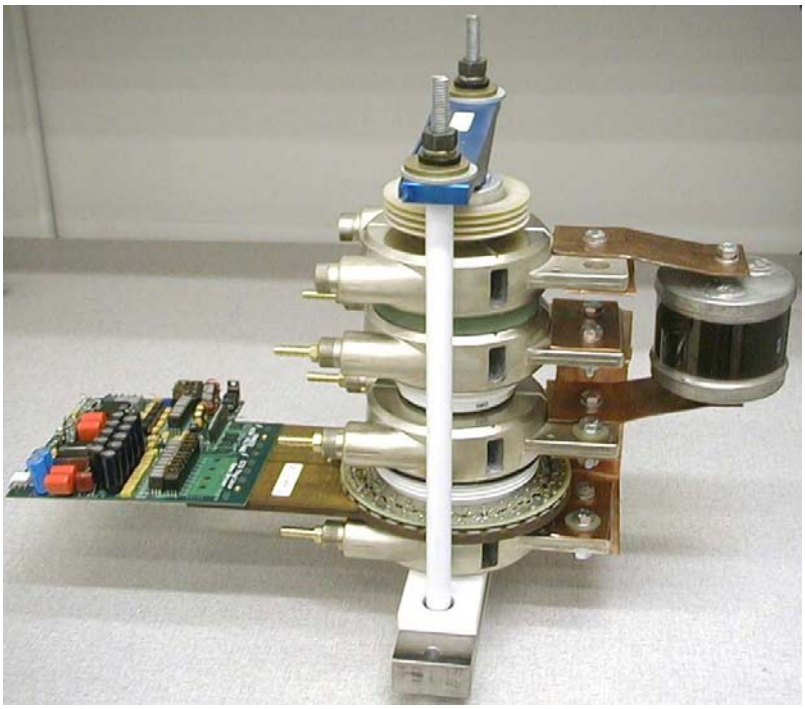


Figure 7-12 Physical implementation of a 3000V, 1700A solid-state DC circuit breaker

Figure 7-13 shows the experimental results of the 3000V, 1700A solid-state DC circuit breaker. The solid-state DC circuit breaker is tested at 2000V, 900A only. The test conditions emulate a shoot-through scenario – a terminal short. The high di/dt slope builds up 800A with in 8 microseconds. The measured response delay is less than 2 microseconds, which results in a 100A overshoot beyond the tripping current. The results again demonstrate unmatched performance of the high-speed solid-state DC circuit breaker.

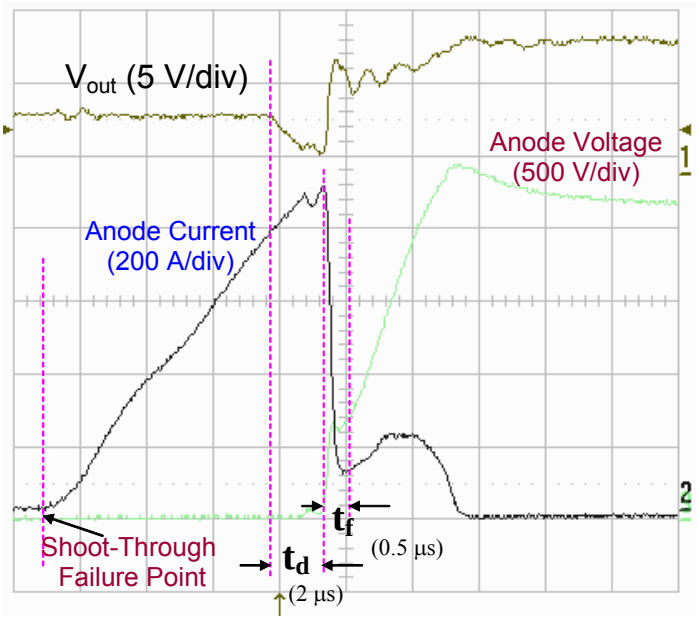


Figure 7-13 Experimental demonstration of a 3000V, 1700A solid-state DC circuit breaker

A fault current limiter (FCL) is proposed to use the high-power IPEM as illustrated in Figure 7-14. During normal operation, the IPEM shorts the high-impedance inductor, and exhibits low impedance. During a fault condition, the IPEM is open and the fault current flow through the high-impedance inductor, thus limiting the fault current to a tolerant level.

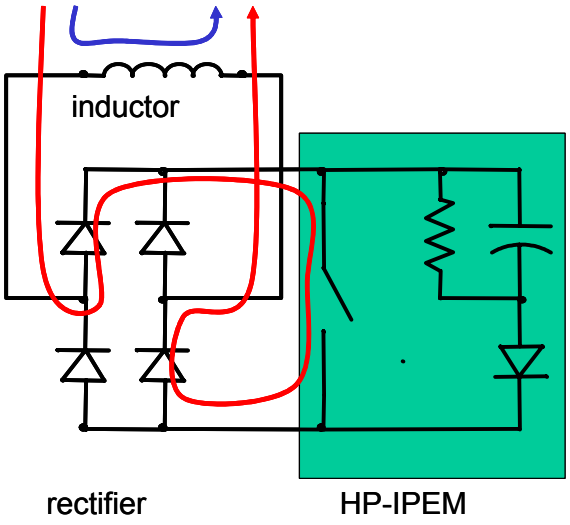


Figure 7-14 Proposed fault current limiter using the developed high-power IPEM

Figure 7-15 shows the performance of the proposed fault current limiter. Without FCL, the prospective fault current could reach 10x rated current (red dashed line). A traditional FCL acts at current zero-crossing point and can't suppress the first peak (blue dotted line). The proposed fast-acting FCL limits the fault current in the whole range (pink solid line).

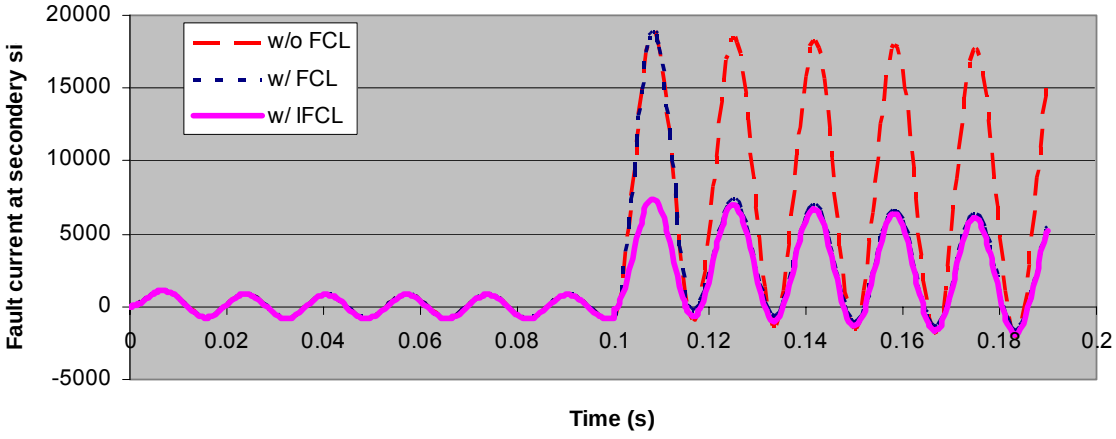


Figure 7-15 Simulated fault current limiter performance

7.5 Conclusion

The high-power IPEM coupled with a solid-state tripping unit is successfully applied as a high-speed, high-current solid-state DC circuit breaker. The experimental demonstration of a 5000A current interruption shows an interruption time of about 5 microseconds. This ultra-high-speed, high-current DC switch can therefore be used in DC circuit breaker applications as well as other types of applications including AC circuit breakers, transfer switches and fault current limiters.

Chapter 8.
Conclusion

The mechanical circuit breaker is widely used in power systems to protect industrial equipments during fault or abnormal conditions. In contrast to the slow and high-maintenance mechanical circuit breaker, the solid-state circuit breaker is capable of high-speed interruption of high currents without generating an arc; hence it is maintenance-free. Both the switch and the tripping unit are solid-state, which meet precise protection requirements and high reliability requirements.

This dissertation proposes a high-speed, high-current solid-state DC circuit breaker that uses a newly-emerging power semiconductor switch, the emitter turn-off (ETO) thyristor, as the main interruption switch.

During the research done for this dissertation, a novel physics-based lumped-charge model was developed for the ETO thyristor for the first time. This model reveals the internal physics mechanism with simple circuit interface. It is implemented in a popular circuit simulator—Saber. This model is verified experimentally and used for the research and development of the emitter turn-off (ETO) thyristor as well as the 5000A DC switch module.

With the aid of the developed device model, device current sharing between paralleled multiple ETO thyristors was investigated. The structure and features of the ETO that makes it suitable for parallel operation are discussed. The model simulation reveals several current redistribution stages during the ETO turn-off phase. And analysis indicates that there is an

intrinsic mechanism in the ETO that enables the ETO's current sharing during dynamic switching. A 5000A turn-off test verifies good current sharing between three ETOs.

Two critical factors affecting dynamic current sharing are identified to be driver delay and storage time delay. Detailed analysis of the storage time reveals the correlation between static current sharing and dynamic current sharing for the first time. The load current dependency of the storage time deteriorates the dynamic current sharing. The relationship between static current sharing and dynamic current sharing has been studied and experimentally verified.

The "DirectETO" concept is proposed to improve the device parallel operation performance. The main concept of this device is to decouple the storage time dependency from the load current. By increasing the dynamic voltage pulse during the gate current commutation phase, the gate commutation time is significant reduced, thus reducing the dependency on the load current, and improving the device parallel operation performance. Hence, a better dynamic current sharing can be obtained regardless of the static current sharing. A high-current DC switch module based on the DirectETO was realized by directly connecting ETOs in parallel without the bulky current-sharing inductors used in other current-sharing solutions.

In order to achieve voltage stress suppression under high-current conditions, the parasitic parameters, especially parasitic inductance in a high-current ETO switch module, have been studied. The Partial Element Equivalent Circuit (PEEC) model was used to extract the parasitics. And both field simulation and experimental results verify the effectiveness of this method. Combined with the developed device model, the electrical interactions among multiple ETOs were investigated which results in structural modification for the solid-state DC switch module.

The thermal network of the DC switch module has been systematically modeled. The Computational Fluid Dynamic (CFD) included discrete model is developed for the force-convection heatsink. A heat spreader layer is used to improve the thermal performance of the DC switch module. The 3-D thermal model is developed for the heat spreader. The ETO device thermal model is also developed for the first time. The electro-thermal model of the DC switch module and the heatsink subsystem was used to identify the "thermal runaway" phenomenon in the module that is caused by the negative temperature coefficient of the ETO's conduction drop. A comparative study of the electro-thermal coupling results in the identification of a strongly-coupled thermal network that increases the stability of the thermal subsystem. The electro-thermal model was also used to calculate the DC and transient thermal limit of the DC switch module which is classified as a 5000A DC switch module. The extracted Time-Current-Characteristic (TCC) curve is also used to define the tripping characteristic of the high-power IPEM-based circuit breaker

The high-current (5000A) DC switch module combined with a solid-state tripping unit was successfully applied as a high-speed, high-current solid-state DC circuit breaker. The experimental demonstration of a 5000A current interruption shows an interruption time of about 5 microseconds. Other variations of configuration are also explored and demonstrated using the same design methodology. A fault current limiter is proposed to utilize the high-speed instantaneous tripping capability of the developed high-power IPEM without sacrificing the system availability.

Since the novel solid-state DC circuit breaker is able to extinguish the fault current even before it reaches an uncontrollable level, this feature provides a fast-acting, current-limiting protection scheme for power systems that is not possible with traditional circuit breakers. Using EMTDC software, the power systems response was simulated under different fault clearing speeds. The high-speed solid-state circuit breaker mitigates voltage sag during fault conditions without affecting the system stability. The high-speed solid-state circuit breaker also provides fault current limiting features; hence it facilitates interconnection of the distributed generations (DG). The development of the high-speed, solid-state DC circuit breaker provides a viable solution for the protection of DC distribution systems. Combined with an intelligent protection and reconfiguration scheme, the high-speed solid-state DC circuit breaker is ready to be deployed in DC distribution applications, such as in shipboard power systems.

Appendix A.
Model Parameters of ETO Model

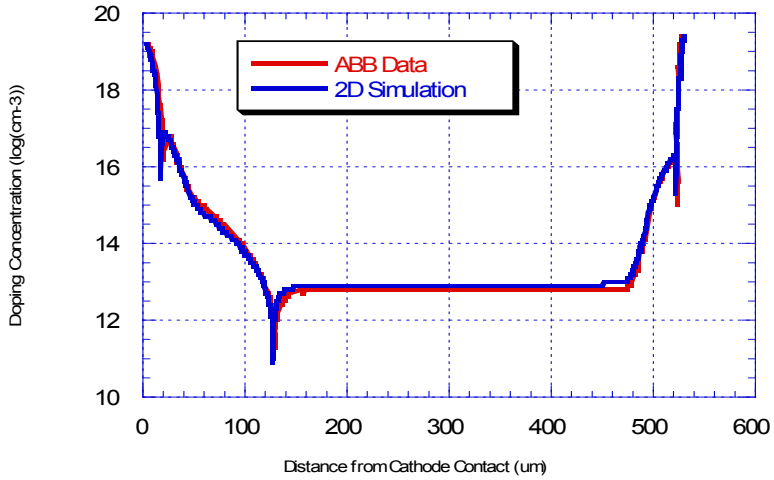


Figure A-1 Doping concentration of a 4.5kV GTO device

Medici Simulation Description File:

```
TITLE   4.5_kV  GTO

MESH     RECTANGU OUT.FILE=4.5kV_GTO.mesh
X.MESH    location=0         node=1
X.MESH    location=76        node=15  ratio=0.9
X.MESH    location=100       node=26
X.MESH    location=218       node=42  ratio=1.1

Y.MESH    LOCATION=0          NODE=1
Y.MESH    LOCATION=10         NODE=7   ratio=0.9
Y.MESH    LOCATION=12         NODE=11  ratio=0.8
Y.MESH    LOCATION=13         NODE=13  ratio=1.2
Y.MESH    LOCATION=20         NODE=18  ratio=1.2
Y.MESH    LOCATION=90         NODE=26  ratio=1
Y.MESH    LOCATION=92         NODE=29  ratio=0.8
Y.MESH    LOCATION=100        NODE=33  ratio=1.2
Y.MESH    LOCATION=692        NODE=65
Y.MESH    LOCATION=722        NODE=69  ratio=0.8
Y.MESH    LOCATION=726        NODE=73  ratio=0.8
Y.MESH    LOCATION=729        NODE=76  ratio=1.25
```

```
Y.MESH    LOCATION=742        NODE=83  ratio=1.25

eliminate  columns  x.min=60 x.max=130  y.min=110
eliminate  columns  x.min=80 x.max=110  y.min=110

COMMENT   Specify oxide and silicon regions
REGION    SILICON  polygon
    +  x.poly=(0,76,76,100,100,218,218, 0)
    +  y.poly=(0, 0,20, 20, 13,13 ,742,742)

REGION    OXIDE    polygon
    +  x.poly=(  76, 100, 100, 218, 218,  76)
    +  y.poly=(  20,  20,  13,  13,   0,   0)

COMMENT   Electrodes

ELECTRODE NAME=Gate    X.MIN=100 X.MAX=218  Y.MIN=13  Y.MAX=13
ELECTRODE NAME=Anode   X.MIN=0   X.MAX=218  Y.MIN=742 Y.MAX=742
ELECTRODE NAME=Cathode X.MIN=0   X.MAX=76   Y.MIN=0   Y.MAX=0


COMMENT   Specify impurity profiles
PROFILE   N-TYPE REGION=1 UNIFORM N.PEAK=2E13
PROFILE   P-TYPE N.PEAK=1E17 Y.JUNCTI=92
     +  X.MIN=0   X.MAX=218 Y.MIN=0  Y.MAX=0
PROFILE   N-TYPE N.PEAK=1E20 Y.JUNCTI=12
     +  X.MIN=0   X.MAX=76  Y.MIN=0  Y.MAX=0
PROFILE   P-TYPE N.PEAK=1E19 Y.JUNCTI=20
     +  X.MIN=100 X.MAX=218 Y.MIN=13 Y.MAX=13
PROFILE   P-TYPE N.PEAK=4E19   Y.JUNCTI=726
     +  X.MIN=0 X.MAX=218 Y.MIN=742  Y.MAX=742

COMMENT   Modify default carrier lifetimes
MATERIAL  SILICON TAUN0=47.95e-6 TAUP0=6.85E-6 EXN.TAU=2.2
     +  EXP.TAU=2.1 NSRHN=4.3e17 NSRHP=4.3e17 PRINT

COMMENT   Specify physical models to use
MOBILITY  SILICON PRINT B.CCS=1.0e13 A.CCS=8e20 EX.LIC=0.28
MODELS    PRINT TEMPERAT=298 FERMI CCSMOB PRPMOB FLDMOB CONSRH AUGER
     +  BGN IMPACT.I
$CONTACT   NAME=Gate RESISTAN=4e6 CAPACITA=0.0 INDUCTAN=0.0

SYMBOLIC  NEWTON CARRIERS=2
SOLVE     initial
$SOLVE     PROJECT ELECTROD=gate  VSTEP=0.2 NSTEPS=4
$SOLVE     PROJECT ELECTROD=gate  VSTEP=1 NSTEPS=2
$SOLVE     PROJECT ELECTROD=Anode VSTEP=0.2 NSTEPS=5
$CONTACT   NAME=ANODE  CURRENT
$SOLVE     PROJECT ELECTROD=Anode ISTEP=2E-5 NSTEPS=9
$SOLVE     PROJECT I(ANODE)=2.18e-4
save       out.file=gto_ini.sol SOLUTION
$save  out.file=view.tif tif all
```

Appendix B.
Model Description of ETO Model

```
# Last update: Wednesday, October 13, 2004

element template  MyETO11 a g  k =model
electrical a, g, k

struc {
number p_plus=1e19,   # Doping concentration in the P+ region
      p=1e16,        # Doping concentration in the p region
      n_plus=1e19,   # Doping concentration in the N+ region
      n_minus=2.384e13,  #Doping concentration in the N- region
      w=520e-4,        # Width of the N- region
      wp=100e-4,     # Width of the P region
      area=80,       # Active area region of the PiN diode
      Kaug=2e-31,    # The Auger coefficient
      is78=1e-8,     # leakage current at J3
      ct=2,     # thermal capacitance of device
      rt=0.0005,     # thermal resistance of device
    taug=6.43u,
    taub=22.67u
     } model= ()

{
number q=1.602e-19,   # Elementary charge
      k0=1.381e-23,  # Boltzmann constant
      ni=1.5e10,     # Intrinsic concentration of carrier
      t=298,         # Operation temperature
      e0=8.854e-14,  # Permittivity in vacuum
      esi=11.9,      # Dielectric constant of silicon
      vsat=1e7,      # Satruration velocity of carrier in silicon
      un=400,        # Mobility of electron in silicon
      up=200,        # Mobility of hole in silicon
    Rash=0.5,
    j3break=10,
    v3break=20

#constants declaration
number p_plus,p,n_plus, n_minus,w, wp, area, aug,is78,ct,rt
number bv,vt,es,v120,v450,v780,qni,qn10,qn30,qp30,
qp60,qn60,qp80,bv78,Kc,Kv,G0,Rgate,Gdisp,Kaug
number r3,r6,g3,g6
number taug, taub

#variables declaration
val v vak,vgk,vag
val i ij1,ip23,in23,ip34,in34,ip56,in56,ip67,in67,
ij3,ipg7,ij2gen
```

```
val q qn1,qp1,qp2,qn2,qn3,qn4,qp5,qp6,qn7,qp7,qp8,qn8
val q qp4,qn5
val nu exp_45 #define k=exp(-v45/vt)
var i icontb,ij2,icontg
var v v12,v45,v78
var q qp3,qn6
val q qp3_,qn6_
var v v23,v34,v56,v67
var i ia,ig,ik
val nu xb,xg,xd
var v vg7
val i iSRH3,iSRH6,iAUG3,iAUG6
val nu sp23,sn23,sn56,sp56

struc {number point, inc;}\
   nsv12[*]=[(-v120,1e-8),(-v120/1.1,1e-4),(0,0.1),(2,0)],
   nsv45[*]=[(-v450,1e-8),(-v450/1.1,1e-4),(0,0.1),(2,0)],
   nsv78[*]=[(-v780,1e-8),(-v780/1.1,1e-4),(0,0.1),(2,0)]


parameters {
     p_plus=model->p_plus
   p=model->p
   n_plus=model->n_plus
   n_minus=model->n_minus
   w=model->w
   wp=model->wp
   area=model->area
   Kaug=model->Kaug
   is78=model->is78
   ct=model->ct
   rt=model->rt
   taug=model->taug
   taub=model->taub

   bv=60*(10e16/n_minus)**(3/4)/1.1  # =4950
   bv=q*n_minus*w*w/(2*e0*esi)
   vt=k0*t/q
   es=e0*esi   # =1.0536e-12
   v120=vt*ln(p_plus*n_minus/(ni*ni))
   v450=vt*ln(p*n_minus/(ni*ni))     # =0.532
   v780=vt*ln(n_plus*p/(ni*ni))
   qni=q*ni
   qn10=q*ni*ni/p_plus
   qn30=q*n_minus
   qp30=q*ni*ni/n_minus # =1.51e-12
   qp60=q*p        # =1.602e-3
   qn60=q*ni*ni/p
   qp80=q*ni*ni/n_plus
   bv78=5.34e13*(p**(-0.75))
   Kc=0
   Kv=0
   G0=1
```

```
   r3=0
   r6=0
   g3=0
   g6=0
   Rgate=1u
   Gdisp=1
}
values {

   vak=v(a)-v(k)
   vgk=v(g)-v(k)
   vag=v(a)-v(g)

   qp1=q*p_plus
            #boundary condition
   if (v12<1.2) then
   qp2=q*ni*ni/n_minus*limexp(v12/vt)
   else
   qp2=q*ni*ni/n_minus*limexp(1.2/vt)*((v12-1.2)/vt+1)
   qn2=qp2+q*n_minus

   #qp3 is a state varible
   if (qp3>0) then
   qp3_=qp3
   else
   qp3_=0
   qn3=qp3_+q*n_minus

   if (v45>1e-3-v450) then
   exp_45=limexp(-(v45+v450)/vt)
   else
   exp_45=limexp(1e-6/vt)

   qp4=exp_45*(exp_45*q*n_minus+q*p)/(1-exp_45*exp_45)
   qn4=qp4+n_minus*q
   qn5=exp_45*(qp4+q*n_minus)
   qp5=qn5+p*q

   #qn6 is a state varible
   if (qn6>0) then
   qn6_=qn6
   else
   qn6_=0
   qp6=qn6_+q*p

   if (v78<1.2) then
   qn7=q*ni*ni/p*limexp(v78/vt)
   else
   qn7=q*ni*ni/p*limexp(1.2/vt)*((v78-1.2)/vt+1)

   qp7=qn7+q*p
   qn8=q*n_plus            #boundary condition
```

```
   if (v45>=bv) then
   xb=sqrt(2*es*p/(q*n_minus*(p+n_minus))*abs(bv+v450))
   else if (v45>-v450) then
   xb=sqrt(2*es*p/(q*n_minus*(p+n_minus))*abs(v45+v450))
   else
   xb=0
   xg=n_minus/p*xb
   xd=xb+xg

   ij2gen=area*q*xd*G0

   sn23=2*area*un/(w-xb)
   sp23=2*area*up/(w-xb)
   sn56=2*area*un/(wp-xg)
   sp56=2*area*up/(wp-xg)

   ip23=sp23*(qp3_*v23-vt*(qp3_-qp2))
   in23=sn23*(qn3*v23+vt*(qn3-qn2))
   ip34=sp23*(qp3_*v34-vt*(qp4-qp3_))
   in34=sn23*(qn3*v34+vt*(qn4-qn3))
   ip56=sp56*(qp6*v56-vt*(qp6-qp5))
   in56=sn56*(qn6_*v56+vt*(qn6_-qn5))
   ip67=sp56*(qp6*v67-vt*(qp7-qp6))  #different from Eq4.37
   in67=sn56*(qn6_*v67+vt*(qn7-qn6_))

   iSRH3=area*w*(qp3-qp30)/taub#(qp3*qn3-q*q*ni*ni)/(1*(1e-5*(qn3+Kc)+1e-5*(qp3+Kv)))#
   iSRH6=area*wp*(qn6-qn60)/taug#(qp6*qn6-q*q*ni*ni)/(1*(1e-5*(qn6+Kc)+1e-5*(qp6+Kv)))#
   iAUG3=Kaug*qp3*qp3*qp3
   iAUG6=Kaug*qn6*qn6*qn6

   ij1=v12/rash

   if (-v78>v3break) then
   ij3=-area*j3break*(-(v78+v3break)/vt+1)
   else
   ij3=-area*j3break*limexp(-(v78+v3break)/vt)

   ipg7=vg7/Rgate


}
control_section {
    newton_step(v45,nsv45)
    newton_step(v12,nsv12)
#    newton_step(v23,nsv45)
    newton_step(v78,nsv78)
    }


equations {

   ij2:ij2=-d_by_dt(area*q*n_minus*xb)-ij2gen
```

```
    ia:ia=ip23+ij1
    v12:ij1=in23
    v23:ip23=ip34+icontb
    icontb:icontb=in34-in23
    v34:ip34=ij2+ip56
    v56:in56=ij2+in34
    icontg:icontg=(ip56-ip67)
    v67:in67=icontg+in56
    v78:ij3=ip67+ipg7
    ik:ik=ij3+in67
    ig:ig=ipg7

    v45:vak=v12+v23+v34+v45+v56+v67+v78
    vg7:vgk=vg7+v78

    qp3:icontb=(iSRH3+iAUG3)+d_by_dt(w*area*qp3) #check for the sign of the differential item
    qn6:icontg=(iSRH6+iAUG6)+d_by_dt(wp*area*qn6) #check for the sign of the differential item
    i(a)+=ia
    i(g)+=ig
    i(k)-=ik

}

}
```

Appendix C.
Behavioral Loss Model for Emitter Turn-Off Thyristor

The motivation for developing a behavioral loss model is to conduct a fast circuit level simulation of semiconductor devices and predict their maximum junction temperatures (Tjmax). For this reason, it is not necessary to obtain an accurate device waveform, but an accurate instantaneous power loss prediction is required. An accurate thermal impedance model is also needed. In addition, the calculated junction temperature will update the power loss instantaneously based on the temperature dependence of the power loss, which further contributes to making this behavioral model very useful in topology optimization and device evaluation.

In this study a device behavioral loss model is developed, which takes the self-heating effect into consideration. The device parameters are temperature-dependant. It precisely calculates the losses without need for lengthy voltage and current waveform. It is implemented in a popular simulator for fast circuit simulation. Figure C-1 shows the modeling basics. The cyan dashed line is the current waveform, and the green dotted line is the voltage waveform. The power curve is derived by multiplying the voltage with the current, which is the red dotted curve. The model approximates the power loss curve by averaging the loss in three distinct periods: the turn-on period, the conduction period, and the turn-off period. The leakage loss in the blocking period is ignored.

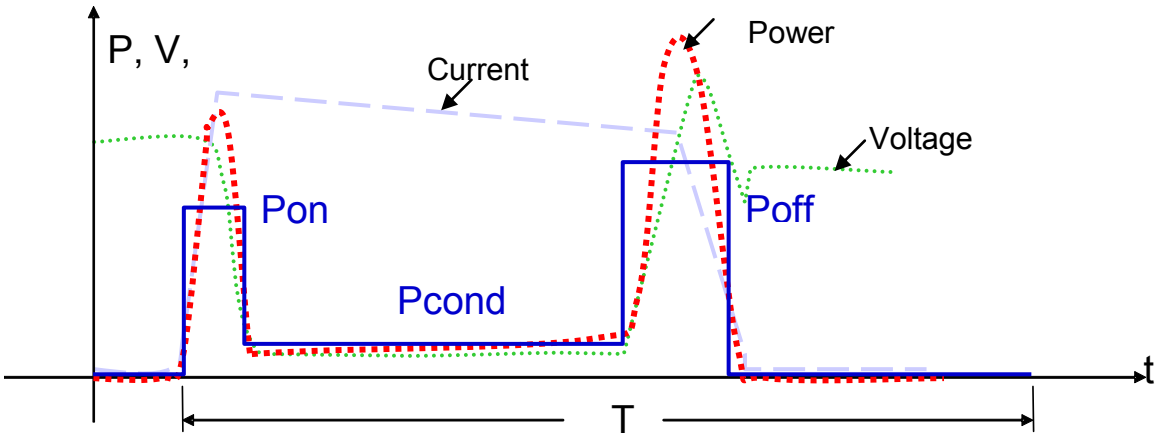


Figure C-1 Device behavioral loss curve

The following equations are used to calculate the device power losses.

$$P_{cond}(T) = V_{ds}(T) \cdot i_d = \left[V_{ds0} + k_{v1} \cdot T + \left(R_{ds0} + k_{r1} \cdot T\right) \cdot i_d\right] \cdot i_d \qquad \text{Eq. C-1}$$

$$P_{on}(T) = \frac{E_{on}(T)}{t_{on}} = \left(E_{on0} + k_{eon1} \cdot I\right) \cdot \left(1 + k_{eonT} \cdot \left(T - T_0\right)\right) \Big/ t_{on} \qquad \text{Eq. C-2}$$

$$P_{off}(T) = \frac{E_{off}(T)}{t_{off}} = \left(E_{off\,0} + k_{eoff\,1} \cdot I\right) \cdot \left(1 + k_{eoffT} \cdot \left(T - T_0\right)\right) \Big/ t_{off} \qquad \text{Eq. C-3}$$

Equivalent on-state voltage drop:

$$V_{th} = V_{th0} + k_{v1} \cdot T$$

Equivalent on-state resistance:

$$r_T = r_{t0} + k_{rt1} \cdot T$$

Turn-on loss:

$$E_{on} = E_{on0} + k_{eon1} \cdot I$$

Turn-off loss:

$$E_{off} = E_{off\,0} + k_{eoff\,1} \cdot I$$

Diodes reverse recovery loss (IGBT):

$$E_{rr} = E_{rr0} + k_{err1} \cdot I$$

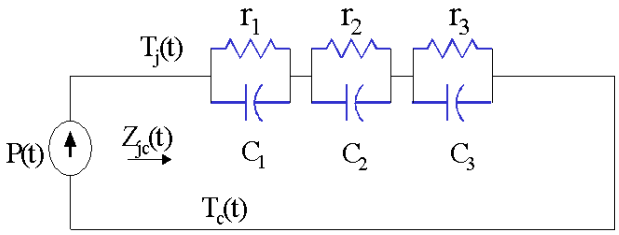


Figure C-2 Device thermal impedance model

The junction-to-case thermal impedance is modeled as a third-order thermal network (Figure C-2).

$$Z_{thjc}(t) = r_1 \cdot \left(1 - e^{-\frac{t}{r_1 \cdot C_1}}\right) + r_2 \cdot \left(1 - e^{-\frac{t}{r_2 \cdot C_2}}\right) + r_3 \cdot \left(1 - e^{-\frac{t}{r_3 \cdot C_3}}\right)$$

The model parameters listed in the above equations are extracted from experiments or manufacturer's datasheets. The model is implemented in SABER for fast circuit simulation. An

ideal switch is used to generate the voltage and current waveform, and then the behavioral loss model is invoked to calculate instantaneous power loss and instantaneous junction temperature.

The simulated device junction temperature can be used to evaluate the overload capability of the circuit breaker under different load current conditions.

Using maximum junction temperature of 125°C as a criterion, the maximum operation time allowed can be extracted from Figure C-3. The maximum operation time allowed is the time current characteristic of the designed circuit breaker, which is shown in Figure C-4.

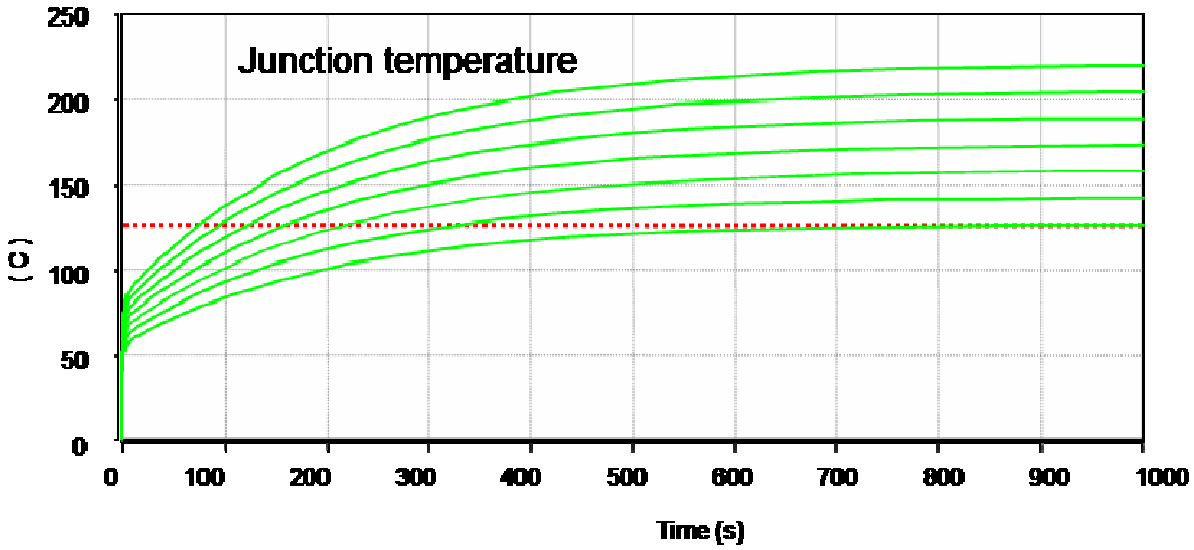


Figure C-3 ETO device junction temperature under different load conditions

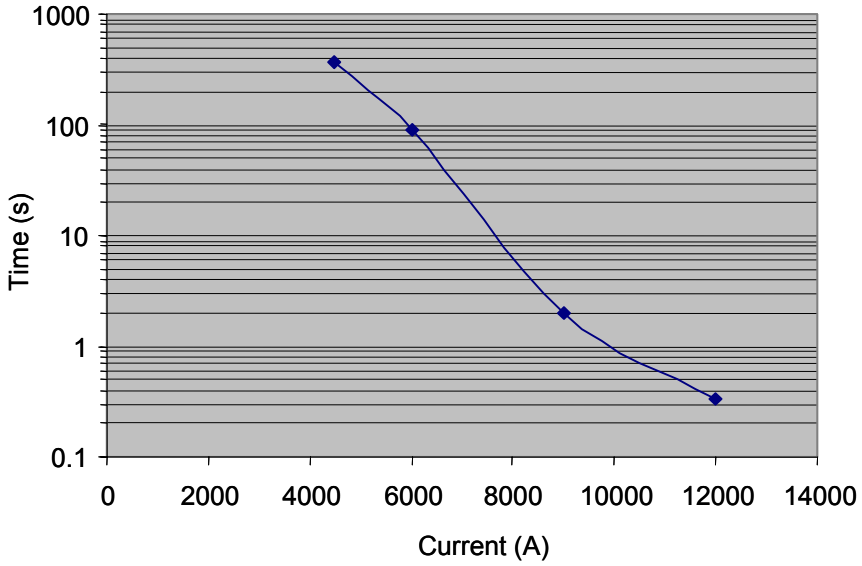


Figure C-4 Circuit breaker TCC curve

Appendix D.
Potential System Impact of High-Speed Solid-State DC Circuit Breaker

1. Introduction

Power electronics are increasingly penetrating traditional power systems. The Flexible AC Transmission System (FACTS), which is a power-electronic-based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability, are now widely accepted by utility engineers. The solid-state circuit breaker [A11][B9], which can interrupt the fault current within a few microseconds and hence limit the fault current to a much lower value, provides a new opportunity to the utility grid. However, the impact of this capability is not well understood.

The system impacts of the high-speed solid-state circuit breaker are studied in this chapter. First, the high-speed solid-state circuit breaker's impact on converter protection is discussed in Section 2. Using EMTDC software, the power systems response is simulated. The high-speed circuit breaker mitigates voltage sag during fault conditions without affecting the system stability. The high-speed solid-state circuit breaker also provides fault current limiting features; hence facilitates interconnection of the distributed generations (DG). All of the system impacts are covered in Section 3. Finally, a brief conclusion is drawn in Section 4

2. Converter Protection

Traditionally, fuses, crowbars or mechanical circuit breakers are used for converter protection. Fuses are protective devices that act as conductors in electrical circuits. When an overload or short-circuit current exceeds a fuse's continuous-current rating, the fuse will stop the flow of the current to protect equipment and personnel. There are two types of fuse: Time-Delay Fuses and Fast-Acting Fuses. However, the fuse is a one-time-use protection device; it requires replacement after each fault, which increases the operation cost.

A crowbar is an electrical circuit usually used to prevent overvoltage from a power supply unit from damaging some downstream circuit. An electrical crowbar operates by throwing a short circuit across the voltage source. Crowbar circuits are frequently implemented using a Silicon Controlled Rectifier (SCR) as the shorting device. Once triggered, the crowbar depends on the correct functioning of the power supply's current-limiting circuitry or, if that fails, the blowing of the line fuses or circuit breaker.

For a traditional power converter, which is shown in Figure D-1, if a short-circuit fault initiates at the motor terminal, the converter first fires through all the inverter devices, then fires through all the rectifier devices, then waits for the line-side AC circuit breaker to trigger at zero-crossing after about 50ms.

The disadvantage of this traditional protection scheme is that the converter/rectifier needs over-design to comply with the prospective fault current which could be 10 times the rated

current. This protection scheme also causes voltage sag to upstream users due to the delay in eliminating the fault.

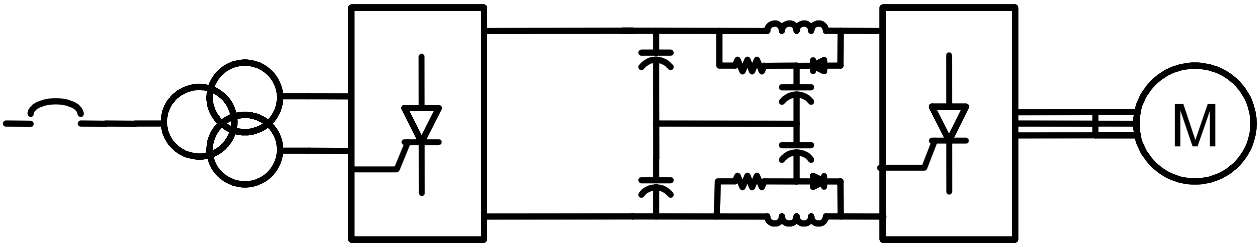


Figure D-1 Traditional power converter protection

With the emergence of the high-speed solid-state circuit breaker, different approaches for converter protection are now being adopted. Figure D-2 shows a state-of-the-art power converter with a solid-state circuit breaker. When a short-circuit fault is initiated at the motor terminal, the converter first fires on all the inverter power devices, and then turns off solid-state DC circuit breaker.

This protection scheme has significant advantages, including protection of the solid-state power converter especially the rectifier bridge and causing no disturbance to upstream users.

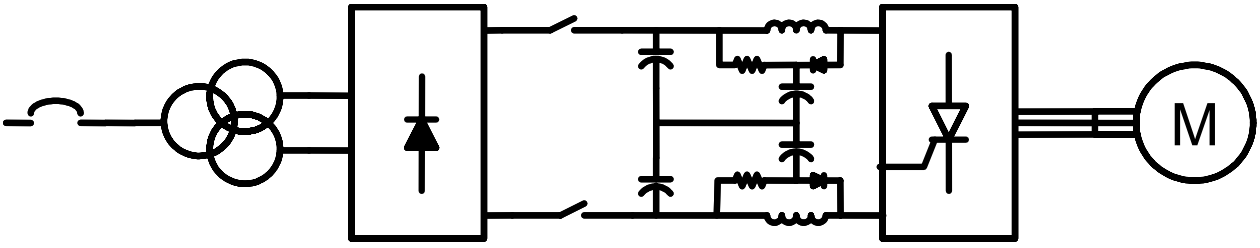


Figure D-2 State-of-the-art power converter protection

Another advantage of the solid-state DC circuit breaker is full utilization of the converter capability.

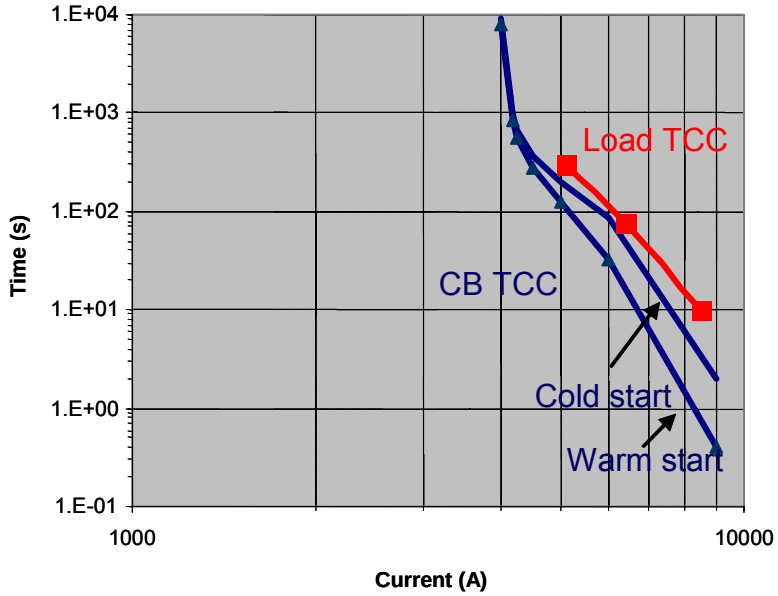


Figure D-3 Power converter protection in a 15MVA STATCOM

For instance, power converter capability of a 15MVA static compensator (STATCOM) [B12] is shown in the red curve in Figure D-3. The solid-state DC circuit breaker capability is shown in the blue curve. The blue triangle-marked curve represents the warm start of the circuit breaker, and the blue solid curve represents the cold start of the circuit breaker. It is clearly shown that the load time-current-characteristics (TCC) match the circuit breaker TCC, which mean a better utilization of both the load converter and the solid-state DC circuit breaker.

3. Power System Protection

Traditionally, a mechanical circuit breaker is deployed to protect industrial equipments in power systems, as shown in Figure D-4. As power electronics apparatuses are increasingly

accepted in the power systems, protecting these equipments demand fast-acting protection devices, an example of which is shown in Figure D-5. The emergence of a high-speed solid-state circuit breaker enables a paradigm shift in the power system protection scheme.

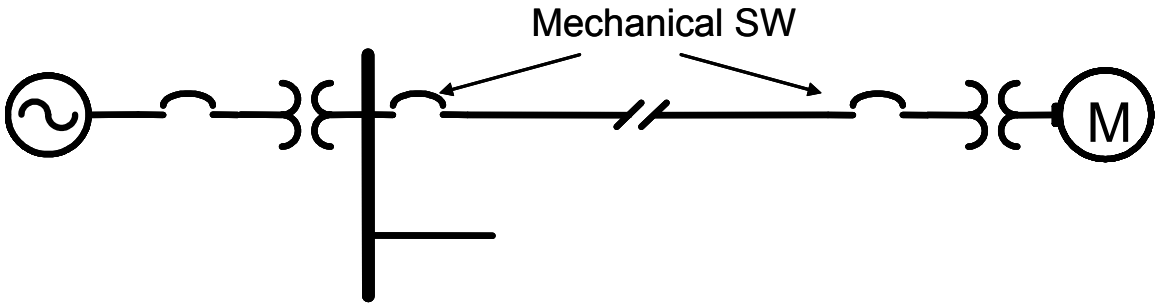


Figure D-4 Mechanical circuit breaker in traditional power systems

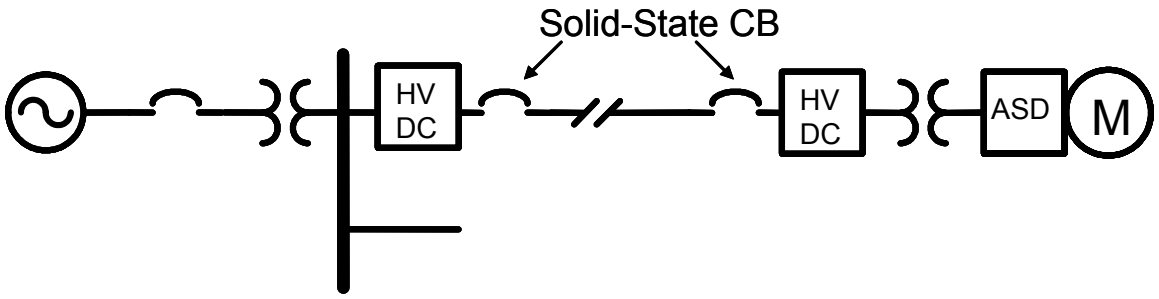


Figure D-5 Solid-state circuit breaker in modern power systems

Voltage Sag Mitigation

To demonstrate the system impact of the high-speed solid-state circuit breaker, a one-bus power system is studied, as shown in Figure D-6. The power system studied consists of a 2MW generator, a source step-up transformer, a 2MW motor as the load, and a load step-down

transformer. The load is connected to the Point of Common Coupling bus Vpcc through a circuit breaker after the rectifier. The leakage inductance of the transformer is 5% per unit with the short-circuit ratio X/R of 10.

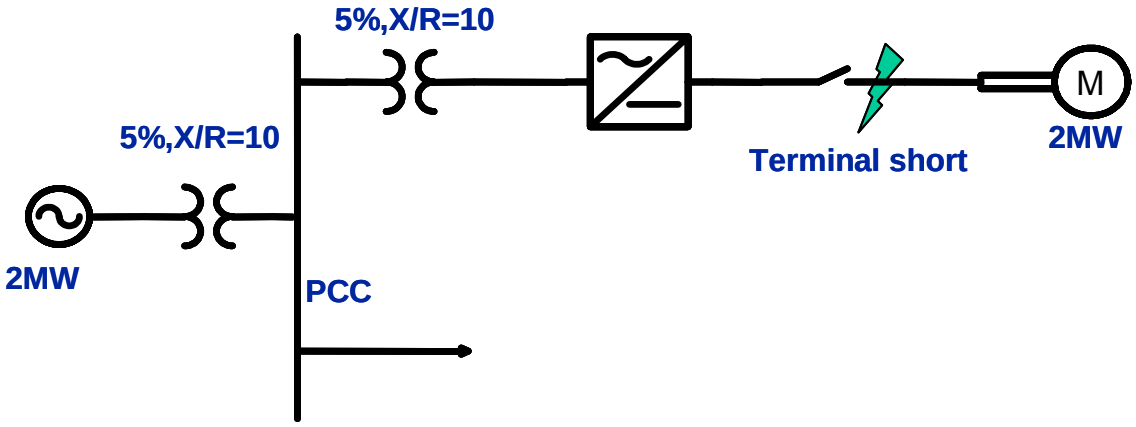


Figure D-6 Simulation schematic for system terminal short fault

A motor terminal-short fault is simulated at different circuit breaker response times. The response time varies from 5 microseconds to 100 microseconds. Figure D-7 shows the simulated voltage sag and fault current at different circuit breaker response times. The pink curve shows the voltage sag on the PCC bus seen by other users connecting to the PCC bus. The green curve shows the built-up fault current.

When the circuit breaker response time is 5 microseconds, which is the achieved current interruption time of the developed solid-state circuit breaker, the voltage sag depth, which is defined as the RMS voltage drop on the PCC bus, is almost negligible. The built-up fault current only reaches 5000A, the instantaneous trip level.

When the circuit breaker response time is 50 microseconds, the voltage sag depth is about 70% of the rated PCC voltage. The fault current exceeds 100,000A caused by the high di/dt discharging rate of the rectifier capacitor bank.

When the circuit breaker response time is 100 microseconds, the voltage sag depth is about 20% of the rated PCC voltage. The fault current reaches the maximum level allowed in the circuit.

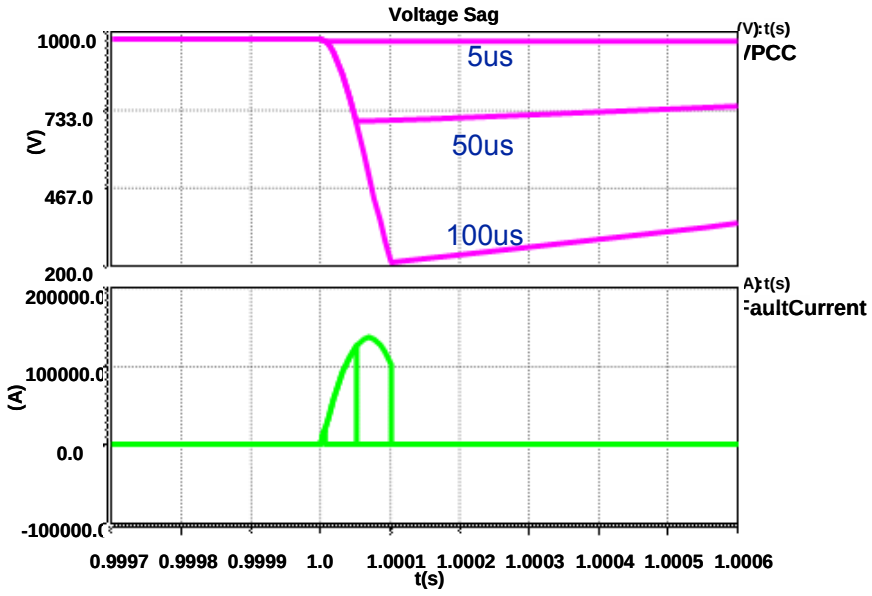


Figure D-7 Simulated voltage sag and fault current at different circuit breaker response time

The other types of circuit breakers are also simulated in the example power system. The voltage sag depth and duration for these are plotted in Figure D-8.

The industry imposes strict requirements on voltage sag. The Information Technology Industry Council (ITIC, formerly known as the Computer & Business Equipment Manufacturers

Association) describes an AC input voltage envelope which typically can be tolerated (with no interruption in function) by most Information Technology Equipment (ITE) [A24]. The curve is applicable to 120V nominal voltages obtained from 120V, 208Y/120V, and 120/240V 60Hz systems. It is shown as the red curve in Figure D-8. The revision CBEMA curve [A24] in 2000 has a more stringent requirement on the voltage sag. The Semiconductor Equipment and Materials International group (SEMI) has a similar requirement [A25] on the voltage sag as shown by the cyan curve. Figure D-8 specifies the allowed voltage sag depth and duration for industry facilities. The upper left side of the curve is the allowed zone without function interruption. The lower right side of the curve is the prohibited zone. The chart clearly shows that the high-speed circuit breaker mitigates voltage sag, thus fully meets the specified industrial standards.

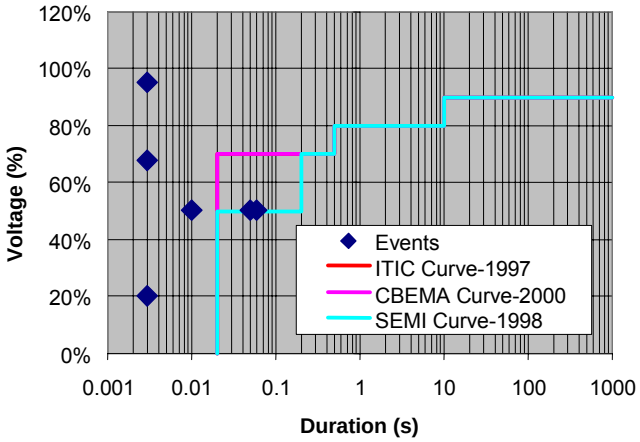


Figure D-8 Industrial standards regarding the voltage sag

System Stability Effect

Use EMTDC software, system stability can be studied. Figure D-9 shows the simulation schematic of a solid-state DC circuit breaker in a one-generator power system. The source is a synchronous generator with exciter and governor. The nominal voltage of the source is 13.8kV. A 5MVA step-down transformer connects the rectifier load to the source synchronous generator. A three-phase diode-bridge rectifier converts the AC voltage to DC voltage. The nominal DC voltage is set at 1kV, and the nominal DC current is 2.5kA. A DC circuit breaker is included in the system for protection purposes. The nominal current of the DC circuit breaker is 2.5kA. The circuit breaker is set to trigger at 5kA instantaneously. The opening time of the circuit breaker can be adjustable, which emulates the fault clearing time of different kinds of circuit breaker. The developed high-speed, solid-state DC circuit breaker is capable to interrupt the fault current within 5 microseconds. The high-speed mechanical DC circuit breaker's fault clearing time is about 5 milliseconds, while the conventional DC circuit breaker requires 50 milliseconds. A short-circuit fault is emulated with a duration of 0.5 second. The transformer voltage on the secondary side is observed for the voltage disturbance. The generator angle, generator field voltage and generator torque are studied for the system stability.

The simulation system parameters are tabulated in Table D-1.

Table D-1 Circuit breaker fault clearing speed system impact simulation parameters

Source	Syn Generator with exciter and Governor, Vnom=13.8kV
Transformer	5MVA, 13.8kV/0.7405kV
Rectifier Load	1kV, 2.5kA
Fault	Set at 3s @ Duration 0.5s
DC Circuit Breaker	Nom: 2.5kA @ Trigger:5kA

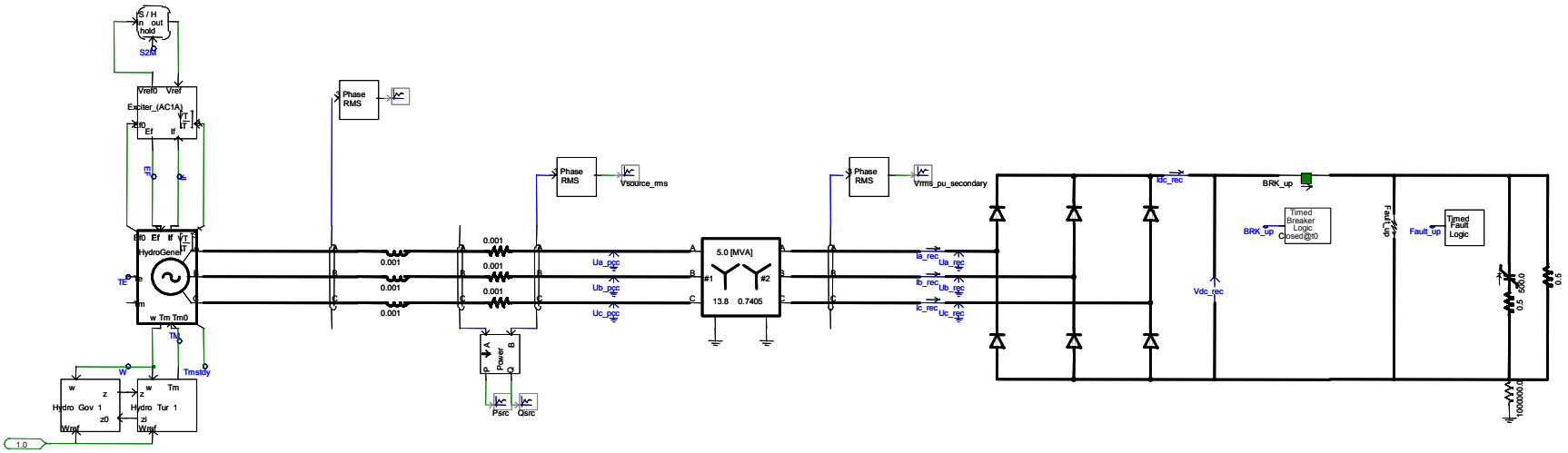


Figure D-9 Simulation of solid-state circuit breaker fault clearing speed system impact

Figure D-10 shows simulated voltage disturbance and fault current in the power system. The red curve represents the high-speed solid-state circuit breaker with a current interruption of 5 microseconds. The green curve represents the high-speed mechanical circuit breaker with a current interruption time of 5 milliseconds. And the blue curve represents the conventional mechanical circuit breaker with a current interruption time of 50 milliseconds. The voltage sag on the transformer secondary side is observed. The duration of the voltage sag is equal to the fault clearing time of the circuit breaker, and the depth of the voltage sag is determined by the location of the fault as long as the fault current is well-developed. However, the high-speed current interruption provides an opportunity to mitigate the voltage sag in the fault-current developing stage. As shown in Figure D-10, the voltage sag depth reaches 40% with current interruption time of 50 milliseconds, while the voltage sag depth is 60% for that of 5 milliseconds. This simulation further shows that the high-speed solid-state DC circuit breaker generates negligible disturbance.

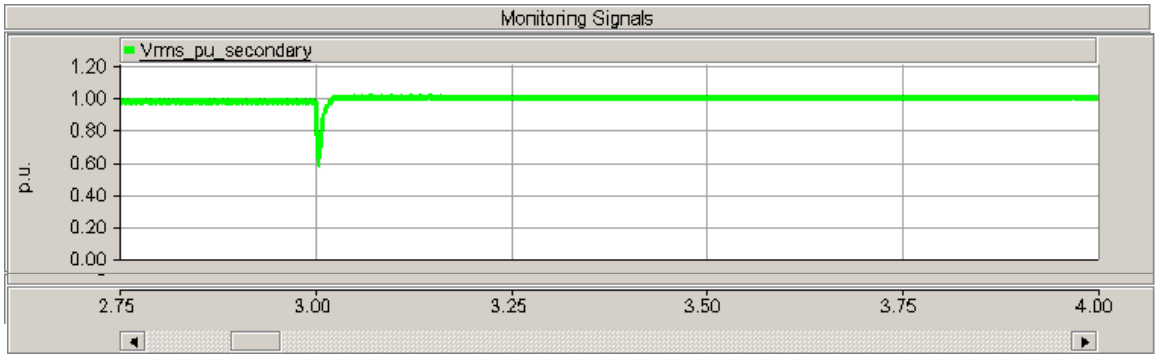


Figure D-10 Comparison of circuit breakers voltage sag mitigation performance

Figure D-11 shows simulated generator angle, field voltage and generator torque on the generator in the studied power system respectively. The red curve represents the high-speed solid-state circuit breaker with a current interruption of 5 microseconds. The green curve represents the high-speed mechanical circuit breaker with a current interruption time of 5 milliseconds. The blue curve represents the conventional mechanical circuit breaker with a current interruption time of 50 milliseconds.

The generator angle results show that the high-speed solid-state circuit breaker has almost the same impact on system stability as the conventional mechanical circuit breaker. However, the sudden lost of load causes the power system great disturbance, which is shown as the increase of the generator angle and reduction of the generator torque.

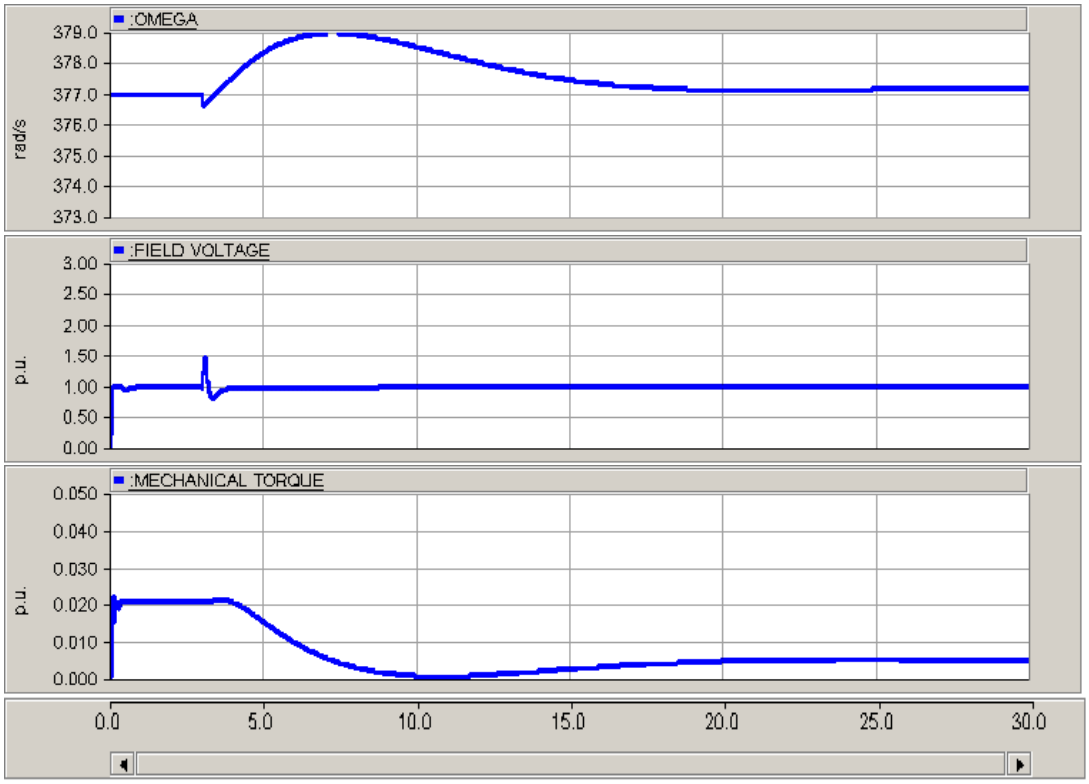


Figure D-11 Comparison of circuit breakers system stability performance

The high-speed solid-state circuit breaker can limit fault current to the maximum tripping level. This current-limiting feature will not increase the system short-circuit-ratio during the power system expansion, which facilities the interconnection of the distributed generation (DG). Its high-speed nature can be used for a "seamless" transfer switch, which increases the system availability. These and other features of the high-speed solid-state circuit breaker require further study.

The coordination of high-speed solid-state circuit breakers was proposed to use an agent based protection and reconfiguration scheme [A28] by N. Mahajan and M. Baran. The scheme was studied in a new zonal DC distribution on naval ships. With the developed high-speed, solid-state DC circuit breaker, the scheme can be practical deployed in the shipboard DC distribution.

4. Conclusion

The system impacts of the high-speed solid-state DC circuit breaker have been studied. Using EMTDC software, the power systems response is simulated under different fault clearing speeds. The high-speed circuit breaker mitigates voltage sag during fault conditions without affecting the system stability. The high-speed solid-state circuit breaker also provides fault current limiting features; hence facilitates interconnection of the distributed generations (DG). The development of the high-speed, solid-state DC circuit breaker provides a viable solution for the protection of DC distribution systems. Combined with intelligent protection and reconfiguration scheme, the high-speed solid-state DC circuit breaker is ready to be deployed in a DC distribution such as shipboard power systems.

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