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A RELIABILITY COMPARISON OF RECESSED-GATE AND SELF-ALIGNED
GATE SMALL SIGNAL GaAs MESFETS UTILIZING AN ACCELERATED LIFE
TEST SET DESIGNED FOR LARGE SCALE AUTOMATED TESTING

by

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ABSTRACT

A large scale automated test set was designed and built to address the varied accelerated life test requirements of the GaAs industry. GaAs low-noise/small-signal MESFETs with 1 x 300 micron gate peripheries and 3 different gate structures were subjected to a 1000 hour high temperature storage test:

- 1) to compare the reliability performance and manufacturability of
 - a) recessed-gate MESFETs with TiPdAu gates
 - b) realigned self-aligned gate (RSAG) MESFETs with TiWN_x Schottky and TiPdAu overlay
 - c) planarized self-aligned gate (PSAG) MESFETs with TiWN_x Schottky and TiPdAu overlay.
- 2) to study the changes in I_{dss} , R_g , R_o , g_m , and V_p over time and their effects upon MAG (Maximum Available Gain).
- 3) to study failure criteria and their applicability toward accurate life predictions.

The recessed-gate devices suffered from Au/GaAs channel interdiffusion resulting in substantial dc parameter degradation above 225°C with an activation energy of 1.7 eV. Although the most widely used device structure in the GaAs industry, its process is not conducive to parameter uniformity.

The realigned self-aligned gate (RSAG) devices are an initial attempt at the fabrication of a self-aligned gate analog MESFET. They were found to exhibit excellent electrical characteristics, but their reliability performance was unpredictable due to the critical nature of the .5 micron TiPdAu gate overlay realignment to a 1 micron TiWN_x Schottky.

Planarized self-aligned gate (PSAG) devices were found to be readily manufacturable and to exhibit excellent reliability.

The use of a decrease in MAG was found to be a more meaningful failure criterion than a 20% change in I_{dss} , which is employed extensively in the literature.

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LIST OF SYMBOLS

I	Current
V	Voltage
T	Temperature ($^{\circ}$ Kelvin)
t	Time
q	Charge on an electron
E_A	Activation Energy
L	Gate Length
W	Gate Width
V_b	Barrier voltage
k	Boltzmann's constant
A^{**}	Richardson's constant
I_{dss}	Saturated drain-source current
V_p	Pinch-off voltage
R_g	Gate resistance
R_s	Source resistance
R_o	Output resistance
g_m	Transconductance
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
MAG	Maximum Available Gain
MESFET	MEtal Semiconductor Field Effect Transistor
SAG	Self-Aligned Gate
RSAG	Realigned Self-Aligned Gate
PSAG	Planarized Self-Aligned Gate

CHAPTER I

INTRODUCTION

In the past 10 years tremendous progress has been demonstrated in the fabrication of GaAs devices and ICs for high frequency microwave and high speed digital applications. The interest in this technology in the military arena is high primarily because of the following properties inherent in the GaAs Field Effect Transistor (FET):

- 1) tolerance of high temperature
- 2) tolerance of high radiation environments
- 3) high electron mobility for high frequency operation at microwave and millimeter wave frequencies.

Mobility at 300 K ($\text{cm}^2/\text{V-sec}$)

	Electrons	Holes
Si	1500	450
GaAs	8500	400

Ion implanted material has been shown to produce excellent results and has supplanted epitaxially-grown active layers as the norm due to its adaptability to a production environment and its versatility. This versatility is derived from the fact that low noise/small-signal devices and power devices may be fabricated on the same circuit through selective implantation at different doses and energies.

Although the progress in the GaAs industry has not met the market predictions and manufacturability forecasts of 5 years ago, at least a dozen companies have established respectable pilot lines, and discrete FETs both low noise and power are readily available commercially. In the last 2 years SSI and MSI digital circuits and MMICs (Monolithic Microwave Integrated Circuits) have become commercially available and are finding their way into specialized test equipment and high speed defense hardware. Recognizing the importance of achieving manufacturability in GaAs ICs for future defense systems, the Defense Department has released the MIMIC (Microwave/Millimeter wave Monolithic Integrated Circuit) Contract to study and resolve the problem. This commitment was based upon preliminary reliability studies which verified the exceptional reliability performance of GaAs active devices in the high temperature and radiation environments common to most military hardware. The high temperature performance of GaAs MESFET (Metal Semiconductor Field Effect Transistor) devices of various fabrication processes and the subsequent problems associated with large scale accelerated life testing of these devices is the focus of this research paper.

Although GaAs devices have been in use in hybrid microwave amplifiers for quite some time, reliability studies have been limited to relatively small sample sizes or large experiments composed of a summation of smaller experiments. This

is due to characteristics of the GaAs industry, and to the problems encountered in life testing devices which are very tolerant of high temperatures. First consider the GaAs industry:

- 1) Many GaAs companies are in the transition phase between a research and development lab and pilot production facility
 - a) Process development is ongoing; reliability test results tend to lag behind.
 - b) Many facilities are "company captive" and produce small quantities of devices for "in-house" requirements.
- 2) Substantial investments in capital equipment and facilities (Class 10 cleanrooms and floating slab/anti-vibration construction) are required to successfully process devices with sub-micron geometries. The emphasis is clearly on processing.
- 3) "Production" quantities of devices from GaAs pilot lines are small compared with the silicon industry. The staffing and equipment is limited and tends to be process or process research intensive. Commercially available accelerated life test equipment developed for the silicon industry is generally programmed to test a particular product. All devices are biased identically, removed from the

environmental chamber periodically, and tested. The cost of the test equipment is small when compared with the size of the operational support producing the device and the income derived from that product. In the GaAs industry the number of circuit types and test requirements (bias and test interval) vary over quite a spectrum, but the product volumes do not warrant the purchase of separate, dedicated test equipment.

- 4) There is some disagreement among GaAs researchers concerning reliability test philosophy due to the lack of an extensive accelerated life test data base. Although it is desirable to do accelerated life testing on microwave devices under RF drive conditions, it is at least an order of magnitude more expensive than DC characterization. Accurate prediction of microwave performance from DC device parameters is well documented in the literature,⁽⁷⁾ therefore, DC characterization is very appealing from a cost standpoint. Unfortunately, RF driven life predictions, although correlating in most instances with DC life test results have on some occasions raised additional questions. Different failure mechanisms have been noted for RF driven and DC accelerated life tests performed on power devices.

The present consensus within the industry as interpreted by the author is as follows:

- a) DC characterization of small-signal low-power devices is sufficient to produce accurate life predictions.
- b) Power devices require RF drive if they will be subjected to high pulse power, however, DC characterization is useful and may be acceptable in some cases. This issue will be resolved as more data becomes available.

It is also notable that very little accelerated life test results have been published on GaAs digital circuits. DC characterizations of digital circuits are of limited value, and dynamic testing is simply not possible due to test equipment limitations (complex GaAs circuits are needed to test simple GaAs circuits!). Radiation hardness testing, however, has focused on digital circuits because some circuits (counters or memories for example) are readily tested dynamically. Analog circuit performance degradation is application specific, and therefore, difficult to relate to a consistent failure criterion for comparison purposes.

Secondly, consider the tolerance of GaAs devices to high temperatures. Temperatures in the 200-350°C range are

required to adequately accelerate active component degradation to allow life predictions and reliability evaluations to be completed in a time frame supportive of process development. As a result of this requirement numerous problems arise which are not a factor in the silicon industry where accelerated life testing can readily be performed at temperatures below 200°C.

- 1) Environmental chambers in commercially available test equipment are limited to 200°C operation.
- 2) Ovens will typically reach 325°C, however, they have no cooling capacity. Testing large numbers of power circuits can result in "thermal runaway" of the oven.
- 3) Until recently, suitable test sockets for operation above 250°C have been unavailable.
- 4) Teflon insulation, used extensively for circuit board material, oven-feedthrough wiring insulation, and key fixturing components, cannot be utilized. Welded nickel wiring and ceramic fixturing, often utilized in high temperature testing, are very expensive, difficult to replace, and not conducive to proper conductor lead dress (a typical oven might require a feedthrough with hundreds of conductors).
- 5) Stabilizing components such as ferrite beads and bypass capacitors are unavailable for use at these temperatures with any guarantees from the manufacturer. Typical curie temperatures for ferrites fall

into the 150-250°C range with operation above this limit resulting in paramagnetism. Because of the frequency of operation of typical GaAs devices, bypass capacitors must be located very close to the device under test and must therefore be physically small, have a low ESR, and minimal lead inductance. Microwave capacitors of parallel plate construction (gold-over-nickel barrier with ceramic dielectric) satisfy these requirements and should be capable of extended operation at temperatures up to 350°C, however, the manufacturer will guarantee operation only to 125°C.

- 6) Dynamic testing of circuits and circuit elements at GHz frequencies through an oven wall is even more difficult than DC characterization. To circumvent this problem, RF driven accelerated life testing has been successfully performed by heating only the part by:
 - a) Passing current through heater resistors mounted on the device package and sensing its temperature with a thermocouple or thermistor element.
 - b) Mounting the packaged devices on a hotplate or under a hot airstream heater.

RF driven accelerated life testing has generally been limited to power devices where it is believed to be necessary for producing the failure modes seen during normal operational conditions. The technique of heating the device and fixture only is of limited practicality because of the obvious problems which would be encountered in controlling the room's ambient temperature due to the heat generated by a large scale test. Typical fixturing costs for RF driven accelerated life testing is \$4000 per device due to the high cost of high frequency connectors.

CHAPTER II

LITERATURE REVIEW

Although the high frequency performance of GaAs devices was primarily responsible for the initial interest in GaAs as a semiconductor material, its reliability as a result of its high temperature and radiation tolerance is just as important to its future application in high speed electronics systems. Because there is no "field-failure" history on these devices, researchers have been forced to rely on life predictions based upon accelerated life testing. These tests have revealed failure mechanisms attributable to the degradation of the GaAs material itself and device degradation due to metallization failure. Material degradation includes trap and defect formation, and net donor density changes. Metallization failure includes electromigration, corrosion, and interdiffusion. Tremendous strides have been made in the area of GaAs material in the past 5 years. It is the author's experience that with proper QC procedures, excellent GaAs material can be purchased for pilot line production of devices operating to 25 GHz. In the digital arena, where threshold voltage uniformity is a function of material defects, MSI level circuits can be fabricated with similar material for 2-3 GHz operation. Metallization failure is therefore the dominant failure mechanism in today's GaAs MESFET devices. Unfortunately, metallization schemes and processes vary widely from manufacturer to manufacturer as do

the metals utilized. These factors have significant implications on device reliability. Properly designed and fabricated GaAs FETs have very low failure rates, and show great promise for future system applications.

2.1 Metallizations

Ideally metallizations used in MESFET fabrication should have the following properties:

- 1) high electrical conductivity.
- 2) low tendency toward electromigration.
- 3) inertness to GaAs, ambient conditions, and passivation.
- 4) good GaAs surface adhesion.
- 5) controllable GaAs penetration if desired OR no penetration at all.
- 6) good bondability.
- 7) processibility and adaptability to photolithographic techniques.
- 8) low contact resistance for ohmics, reasonably high barrier height for gates.

No single metal or metal combination provides all of the above. Usually, a compromise which optimizes most of the above is selected.

2.1.1 Ohmic Contacts

Early low resistance ohmic contacts were formed by alloying AuGe into a highly implanted N⁺ layer under the

source and drain. A layer of Au was then plated on top of the AuGe layer to form the bonding pads. This type of structure degraded with time and temperature. The Au with oxygen diffused into the GaAs and the gallium diffused through the AuGe into the Au layer causing an increase in contact resistance. Ag, Cr, Pt, Ta, Ti, and predominantly Ni were placed between the Au and AuGe as a diffusion barrier. Activation energies of .8-1.8 eV have been noted for ohmic contact degradation.^(2,3,4,18) If operating temperatures are limited to 100°C or less, deterioration is negligible, however, above this temperature, rapid degradation occurs. State-of-the-art contacts employ an additional diffusion barrier such as TiWN_x to prolong lifetimes of ohmic contacts.^(12,15,16)

2.1.2 Gate Metal

GaAs devices employ micron and sub-micron gate structures. Because of the small dimension of this key structure and the criticality of its proper fabrication to device performance, most of the metallization failure mechanisms in today's MESFETs relate to the gate metal chosen and its fabrication and passivation techniques. Aluminum was the early choice because of its ease of fabrication and because it does not react readily with GaAs at temperatures below 400°C. It does have some major drawbacks, however. It is prone to electromigration, electrolytic corrosion, Au-Al and Pt-Al phase formation, and pulse burnout. The failure mechanisms attributable to Al gate metallization are well

understood, and there are known solutions to many, if not all, of these problems.^(2,3,4,17,19,20,21,23,24,25,26,27,28) Refractory gate metallizations such as Ti/Pd/Au, TiPtAu, Ni, Mo/Au, Ti/W/Au, are widely used as alternatives to aluminum for improved reliability. Au based metallization schemes have different problems which are not as well understood, and the expected gains in reliability from switching to Au based refractory metal gates have not been totally realized.^(2,3,4,8,9,14,18,20,22,25)

2.2 Failure Mechanisms

2.2.1 Reliability of Low-Noise GaAs FETs

Early reliability studies indicated that GaAs MESFETs, like MOSFETs in silicon, are susceptible to burnout failure caused by electrostatic discharge (ESD).^(2,3,4,18,19) Reverse bias pulses were found to be more damaging than forward biased pulses. Aluminum gates were found to be more susceptible to this failure than refractory gates. ESD failure can be eliminated by proper handling techniques.

Phase formation and electromigration are not significant problems in Au based refractory gate devices, but great care must be taken in the fabrication and design of aluminum gate devices. Even if a diffusion barrier exists between the Al and Au, phase formation can occur if anything disturbs that layer. A pinhole, void, scratch, or damage due to wirebonding can cause such a disturbance. The failure resembles that of electromigration and in many cases is accompanied by

electromigration. Voiding of the metallization occurs and open gate lines resulting in a reduction or total loss of gate control indicate device failure.(2,3,4,19,21)

Electrolytic corrosion of aluminum can cause significant reliability problems. Proper passivation and hermetic package sealing is of the utmost importance. Au based refractory metal systems are less susceptible to failure due to corrosion.

Devices fabricated with Au based refractory metal gates suffer from Au/GaAs channel interdiffusion problems at elevated temperatures. This occurs because the diffusion barriers on these devices formed by Ti/Pd, Ti/Pt, Ti/W, etc are not adequate. Activation energies from .8-1.8 eV have been reported for this phenomenon.(6,8,9,14) The interdiffusion of the gate metal and the GaAs channel can be caused by either of 2 mechanisms. The first involves the movement of the effective Schottky barrier into the channel, thereby decreasing the available channel thickness. This is indicated by a reduction in I_{DSS} and pinchoff voltage V_p . The second involves the dopant action of the diffused metal atoms with a resultant change in the net donor density in the channel with similar electrical parameter shifts. The first theory is predominant in the literature, but because the channel thickness is typically .1-.4 microns thick, it is difficult to determine the exact mechanism of the failure. Aluminum gate devices do not suffer from this problem.

Because Al was the dominant gate metal in the early developmental stages of GaAs MESFETs, it is likely that some of the early reliability studies performed upon Au based gate devices erroneously concluded the ohmic contact failure mechanism (.8-1.8 eV activation energy) as the dominant failure mode (as was the case for Al gate devices). I_{dss} was the only parameter measured and with similar activation energies it was difficult to separate the two failure modes without studying many parameters. The latest studies indicate that the Au/GaAs channel interdiffusion phenomena is the dominant failure mode as ohmic contacts have improved steadily in the past 5 years. State-of-the-art devices employ additional diffusion barriers under the gate stripe and in the drain/source ohmics to increase device lifetimes.

2.3 Life Test Philosophies

2.3.1 Unbiased vs Biased RF Drive

Because of the wide variation in metal systems and processing, there are many conflicting opinions concerning failure modes and mechanisms. In addition, the MESFET structures, critical dimensions and spacings, designs, and materials vary widely between manufacturers. Depending upon the particular failure and how it relates to all of these parameters, a biased or unbiased life test may or may not produce similar results. In general, metal diffusion induced failures are not bias dependent, but failures sensitive to

electric field or current such as electromigration are. The dominant failure mode determines where bias is required to predict device lifetimes. For this reason low-noise/small-signal devices are tested in biased and unbiased modes, but seldom with RF drive. Power devices, on the other hand, are dominated by catastrophic burnout caused by high current densities and high electric fields in the presence of high channel temperatures. Biased accelerated life testing preferably with RF drive is subsequently required for life prediction of these devices. Although some life tests have produced identical degradation rates for biased and RF driven devices, the failure modes have been different in some cases. The general consensus within the industry is that RF drive is a requirement. Limited RF driven testing has been done because of high equipment and fixturing costs.

CHAPTER III

RESEARCH OBJECTIVE

Accelerated life testing of GaAs devices is difficult when compared to silicon devices due to their tolerance of high temperature. The apparent cost of testing a significant number of these devices and the present state of the GaAs industry has limited the reliability studies to date to small sample sizes with a limited number of measured parameters. Failure criteria based upon changes in one or more of these parameters have been applied, activation energies calculated, and life predictions formulated.

The basic active element used in digital and analog GaAs integrated circuits is the MESFET or Metal Semiconductor Field Effect Transistor which utilizes a Schottky gate to control drain current and produce voltage and current gain. This device has been the focus of the majority of the reliability studies to date. Gradual degradation mechanisms which dominate this device are as follows:

- 1) Gate metal interdiffusion with GaAs resulting in an effective reduction in channel thickness due to a less than optimal Au diffusion barrier. This is the most common failure mode of low noise/small signal devices.
- 2) Ohmic contact degradation due to realloying. Alloy optimization experiments yield a bathtub shaped

curve of resistance vs alloy temperature. High temperature operation increases the alloying time, and therefore, can result in an overalloyed contact with less than optimal resistance.

- 3) Electromigration failure of gate, drain, or source metalization in power devices.

The objectives of this research effort were as follows:

- 1) To design an accelerated life test facility capable of performing large scale reliability testing of GaAs discrete devices and ICs. The types of devices under test within the system must be allowed to vary, therefore, device level bias control and test intervals are a requirement. The devices under evaluation must automatically undergo an extensive DC characterization every test interval with the parameters stored on disk for later analysis. The system must be modular and versatile in design for future expansion, and cost effective.
- 2) To design low cost high temperature fixturing capable of withstanding 300°C for extended period of time.
- 3) To perform a small-scale accelerated life test on a widely used low-noise/small-signal GaAs MESFET structure (TiPdAu recessed gate) and compare its high temperature performance to two alternative

small-signal self-aligned gate MESFET structures fabricated with improved Au diffusion barriers.

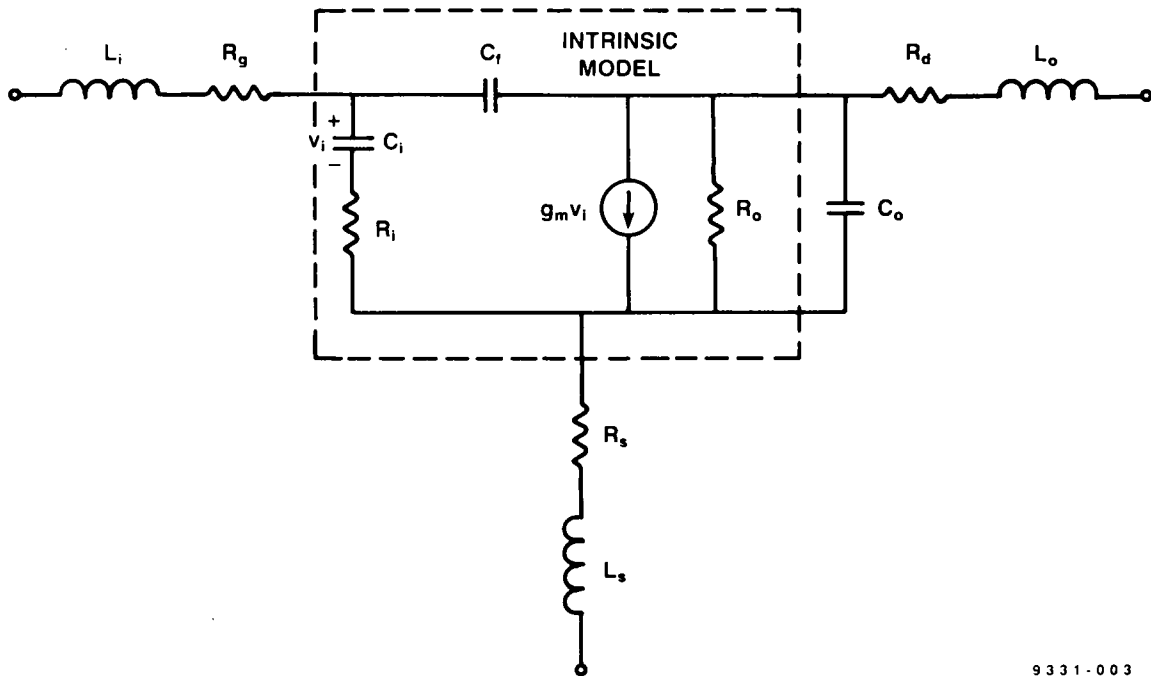
- 4) To study the changes in I_{dss} , R_g , R_s , R_o , g_m , and V_p for these three types of devices at elevated temperatures over time, their effect on MAG (Maximum Available Gain), and the subsequent implications for choosing a meaningful failure criterion for accelerated life tests.

CHAPTER IV

THEORETICAL BACKGROUND

This chapter contains a discussion of the theoretical background needed to understand the measurements made in the DC characterization of the GaAs MESFETs, and the reliability calculations used to derive activation energies and life predictions based upon Arrhenius type time-temperature dependency.

Figure 4.1 shows a lumped element model of a GaAs MESFET. For the DC characterizations in this paper, the inductances L_i , L_o , and L_s which depend upon the wire bonding/packaging of the MESFET, are set to zero. R_d , which is typically much smaller than R_o , does not play a significant role in the calculation of MAG (Maximum Available Gain). C_{gs} and C_{gd} are typically less than .5 pf for 1 x 300 micron gate low-noise/small-signal MESFETs, and could not be measured with reasonable accuracy in a large test system. They were calculated based upon typical values.



9331-003

Figure 4.1 GaAs MESFET lumped element model.

4.1 Key DC Parameters

The following DC parameters were measured or calculated at each test interval during accelerated life testing:

I_{dss} = saturated source-drain current ($V_g = 0.0$ volts at a specified $V_{ds} = 3.0$ volts)

V_p = gate-source voltage required to reduce the source-drain current to 2% of I_{dss} .

R_g = gate resistance due to the metallic resistance of the gate stripe which is generally between .4 and 1.0 microns in "length" (Note: gate length as defined in the literature is the small dimension of the gate Schottky which lies parallel to the channel). Gate width is the long dimension of the gate perpendicular to the channel. The gate Schottky dimensions of the MESFETs under study in this research paper are nominally 1 x 300 microns (L x W). The R_g value derived in the DC characterizations include R_i , the intrinsic channel resistance which is generally 2 ohms or less.

R_s = source resistance between the source metal and the gate including the ohmic contact resistance of the source.

R_o = drain-source channel resistance = $d V_{ds}/d I_d$.

g_m = transconductance = $d I_d/d V_{gs}$. Key parameter for transistor gain.

g_m is typically measured at three drain current levels

1) Full I_{dss}

2) $.5 I_{dss}$ = Typical bias for maximum gain

3) $.2 I_{dss}$ = Typical bias for minimum noise figure

C_{gs} = gate-source capacitance. Key parameter which along with g_m determines $f_t = g_m/2 \pi C_{gs}$.

Because of the magnitude of this parameter (.2 - .4 pf) and the length of cabling involved in the DC characterization, no attempts were made to perform this measurement. The parameter was given a typical value and assumed to remain constant over time for any and all calculations of MAG (Maximum Available Gain). The variation of C_{gs} with time at elevated temperature is the focus of another experiment outside the scope of this paper.

C_{gd} = gate-drain capacitance

Typically an order of magnitude smaller than C_{gs} , this parameter was also given a typical value and assumed to remain constant for all calculations of MAG (Maximum Available Gain).

MAG = Maximum Available Gain

$$\text{MAG} = 10 \text{ LOG } \frac{g_m^2}{C_{gs}\omega} \cdot \frac{1}{(R_s + R_g) \left[\frac{4}{R_o} + \frac{2 g_m C_{gd}}{C_{gs}} \right]}$$

$$\omega = 2 \pi f$$

$$f = 1 \text{ GHz/gatelength}$$

4.2 Arrhenius Calculation

The Arrhenius equation relates reaction rate to temperature.

$$R = R_o e^{-E_A/kT}$$

where R_o = a constant

E_A = activation energy in electron-volts (eV)

k = Boltzman's constant 8.6×10^{-5} eV/°K

T = absolute temperature in °K (°C + 273)

Assuming accelerated life testing is done at two temperatures, T_1 and T_2 , let R_1 and R_2 be the reaction rates at T_1 and T_2 respectively, causing failures to occur at t_1 and t_2 . The times to failure t_1 and t_2 are the median lives (the numbers least affected by sampling variation). Then

$$R_1 \times t_1 = R_2 \times t_2$$

and

$$\ln t_1 = C + \frac{E_A}{kT_1} \qquad \ln t_2 = C + \frac{E_A}{kT_2}$$

Therefore,

$$\ln \frac{t_2}{t_1} = \frac{E_A}{k} \frac{1}{T_2} - \frac{1}{T_1}$$

and

$$E_A = \frac{T_1 \times T_2 \times k \times \ln \frac{t_2}{t_1}}{T_1 - T_2}$$

Once the activation energy is known, the constant R_0 can be determined and a reaction rate and median life calculated for any temperature.

4.3 Schottky Diode Equation

The thermionic emission model states that the current I through a Schottky diode is:

$$I = \text{Area} \times A^{**} \times T^2 \exp \frac{-qV_b}{kT} \exp \frac{qV}{nkT}$$

for $V \gg kT$, where

A^{**} = effective Richardson constant = $8.4 \text{ A cm}^2\text{-K}^2$

V_b = barrier voltage

V = applied voltage

k = Boltzmann's constant

T = absolute temperature

Schottky current is therefore a linear function of diode cross-sectional area and an exponential function of barrier voltage.

CHAPTER V

EXPERIMENTAL METHODS AND MATERIALS

5.1 Accelerated Life Test Facility

An automated accelerated life test facility was designed which meets the varied test requirements of the GaAs industry. These requirements may be summarized as follows:

- 1) Operation to 300°C
- 2) Statistically valid sample size at a minimum of 3 temperatures for accurate determination of activation energies (6 temperatures are available).
- 3) Versatility to test various device types (low-noise/ small-signal and power MESFETs, diodes, resistors, capacitors (leakage current), and ICs, randomly scattered within test ovens. This requires device level bias control and test intervals.
- 4) Automated testing and data storage
- 5) Data analysis capability - trend plotting and history report printout of all measured parameters.
- 6) Device protection in the event of line power failure.
- 7) Modularity of design for extensive modification and expansion at minimal cost.
- 8) Versatile I/O capability to meet future requirements.
- 9) A convenient, removable, high-capacity storage media for creation of a data library.

- 10) Data link to a mainframe computer for accessibility to high computational power for manipulation and analysis of large data bases.

5.1.1 System Overview

The devices are life-tested in 6 computer-programmable inert atmosphere (Nitrogen) ovens capable of 300°C operation. Each oven contains fixturing for 64 test positions for a total capacity of 384. A four stage amplifier occupies four positions, and a resistor, capacitor, or MESFET one position. The devices to be tested are mounted in a test vehicle package capable of holding 8 devices. For biased accelerated life testing, bias is derived from programmable bias regulators located in cabinetry on the back of the ovens. During automated testing, bias is provided by precision power supplies located in an equipment desk with the computer/controller and measurement system. The switching between the bias and test power supplies is accomplished by a mercury wetted relay matrix also located in the cabinetry on the back of the ovens.

The automated test system requires no operator interaction once the devices are initialized for test. All commands are menu or function-key driven from a color graphics terminal which forms the operator console. A test system operator may choose from an array of status reports which indicate with color graphics the ovens which are on-line,

their associated temperature, the number and type of devices which are on test within each oven, and the status of those devices (OK, Failed, or Empty position). To initialize testing, the operator places a test vehicle package containing up to eight devices into the desired position within an oven and enters the required device identification information, test interval (1,2,3,4,6,8,12, or 24 hours), and desired life test biasing. Once all devices within the oven have been initialized, the operator sets the oven temperature from the keyboard, and testing begins automatically. The tester performs an extensive dc characterization of each device at the end of its own operator-selected test interval and stores the data on hard disk. MESFET parasitic resistances and transconductance are inserted into the Maximum Available Gain equation and MAG is stored as an indication of expected microwave performance. At any time a test system operator may select from an extensive list of analysis options in order to study any device under test including:

- 1) Plot a diode-like I-V characteristic (current vs voltage).
- 2) Plot a MESFET transistor characteristic curve.
- 3) Plot a trend characteristic of any measured parameter.
- 4) Print out a history report containing all of the data recorded since the test initialization for both a single device or an entire oven.

The plots are displayed in color on the graphics terminal where they can be screen-dumped to either paper or transparency on a high-speed color copier with the push of a button. Trend plots include a plot of both the raw data and a smoothed version obtained by plotting a running average of nine points.

The computer/controller with its storage media, measurement system, and all matrix switching logic is backed up by an uninterruptable power system (UPS) which produces its own 110 volt ac output from a bank of four 72 volt batteries. Because the line voltage is used only to charge the batteries, line disturbances and outages are unseen by the protected equipment. The system uses an on-board CMOS clock with battery back-up to maintain the accuracy of the time to failure. In the event of a power failure, an interrupt is generated that initiates a shutdown of all unnecessary system hardware. The system completes the measurements in progress and stores the data on disk. A hardware fail-safe circuit instantaneously shuts down the device-level bias regulators in the proper sequence to protect the devices under test. This fail-safe circuit can restore the voltage outputs of the bias regulators only upon receiving a command from the computer/controller. This will occur only after the ac line power to the test system has returned and stabilized.

The test system can be subdivided into three functional sub-systems which will be discussed in detail below:

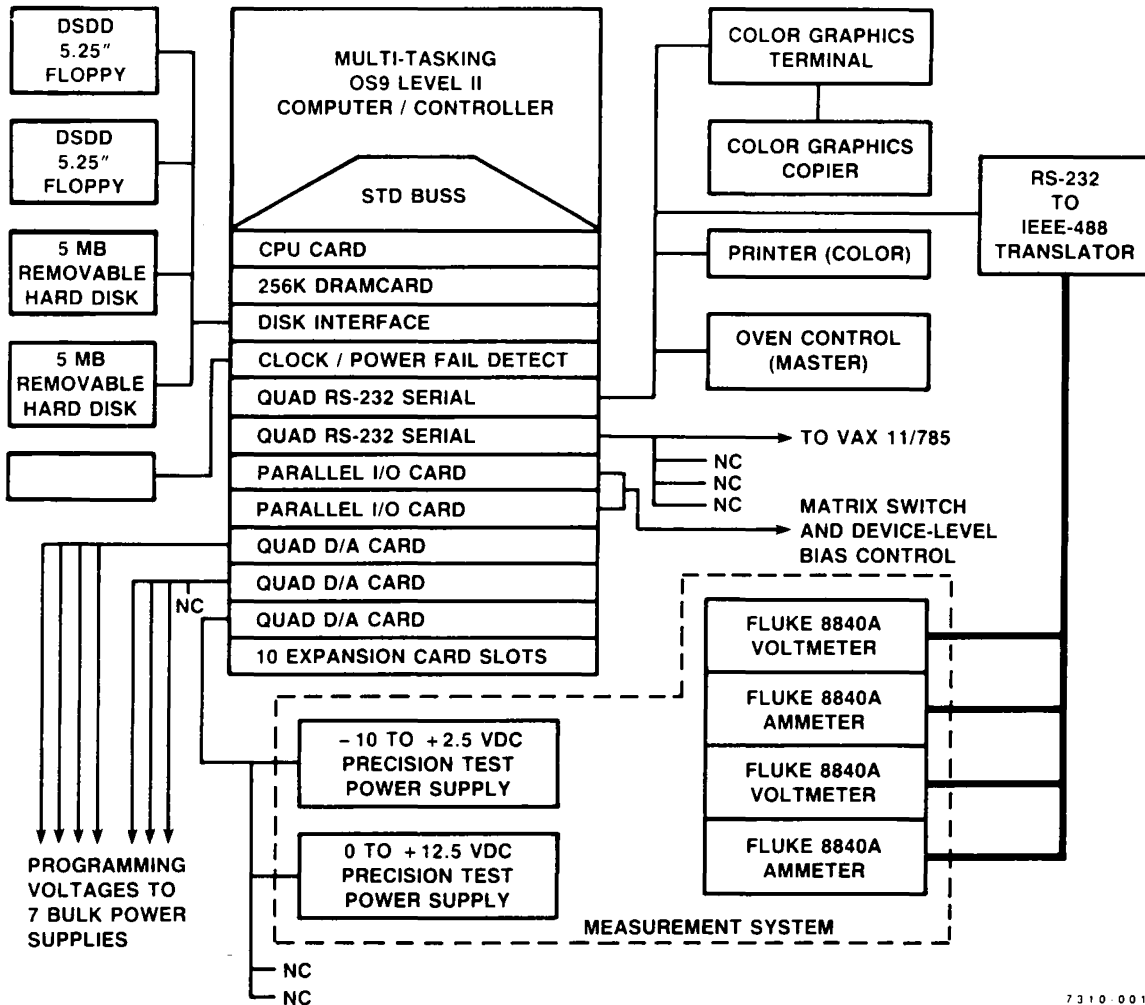
- 1) Computer/controller and measurement system (Fig 5.1)
- 2) Bias power/matrix switching and oven control system (Fig 5.2)
- 3) High temperature fixturing (Figure 5.3)

5.1.1.1 Computer/Controller and Measurement System

The computer/controller and measurement system hardware is mounted in an equipment desk used as the system operator station. The color graphics terminal and the color graphics copier used for operator input and I-V characteristic and trend plotting is located on top of this desk.

A semi-custom computer system using standard STD Bus cards was chosen as the computer/controller (Figure 5.1). A custom CPU board running the Motorola 6809 processor was developed to implement the OS-9* Level II operating system on the STD Bus. OS-9 provides a multi-user, multi-tasking, Unix-like programming environment and Basic09* is readily usable for instrument control. Many of the test modules were written in machine language for fast execution. All of the software is custom, and therefore, readily accessible for future modification. The STD Bus provides low cost interfaces for all conceivable control and data-acquisition functions. The computer uses two, 5.25-inch, DSDD floppy

* OS-9 and Basic 09 are trademarks of Microware and Motorola.



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Figure 5.1 Computer/controller and measurement system.

disk drives for program storage and booting the system. Two removable-media 5-megabyte hard disk drives are utilized for program and data storage. The 5-megabyte removable medium is an excellent choice as its small cartridge size (4.41 inches by 4.33 inches by .43 inches) is physically convenient for an archive library and its capacity is respectable. Each of the two hard disks will hold about 1 week's data for a fully loaded system operating on 2-hour test intervals.

The measurement system is composed of four precision multi-meters interfaced to the computer/controller via an IEEE-488 Bus and two precision bias power supplies with 50-mV resolution driven by STD Bus digital/analog (D/A) converter cards. One supply is capable of bipolar operation from -10 Vdc to +2.5 Vdc and the other has a single ended output of 0 to +12.5 Vdc. For MESFET testing the former supply is utilized for gate bias and the latter for drain bias referenced to grounded sources. It is notable that the measurement system also contains relays which allow the meters to measure voltages on outputs of devices on test as would be required to look at logic level outputs on digital devices.

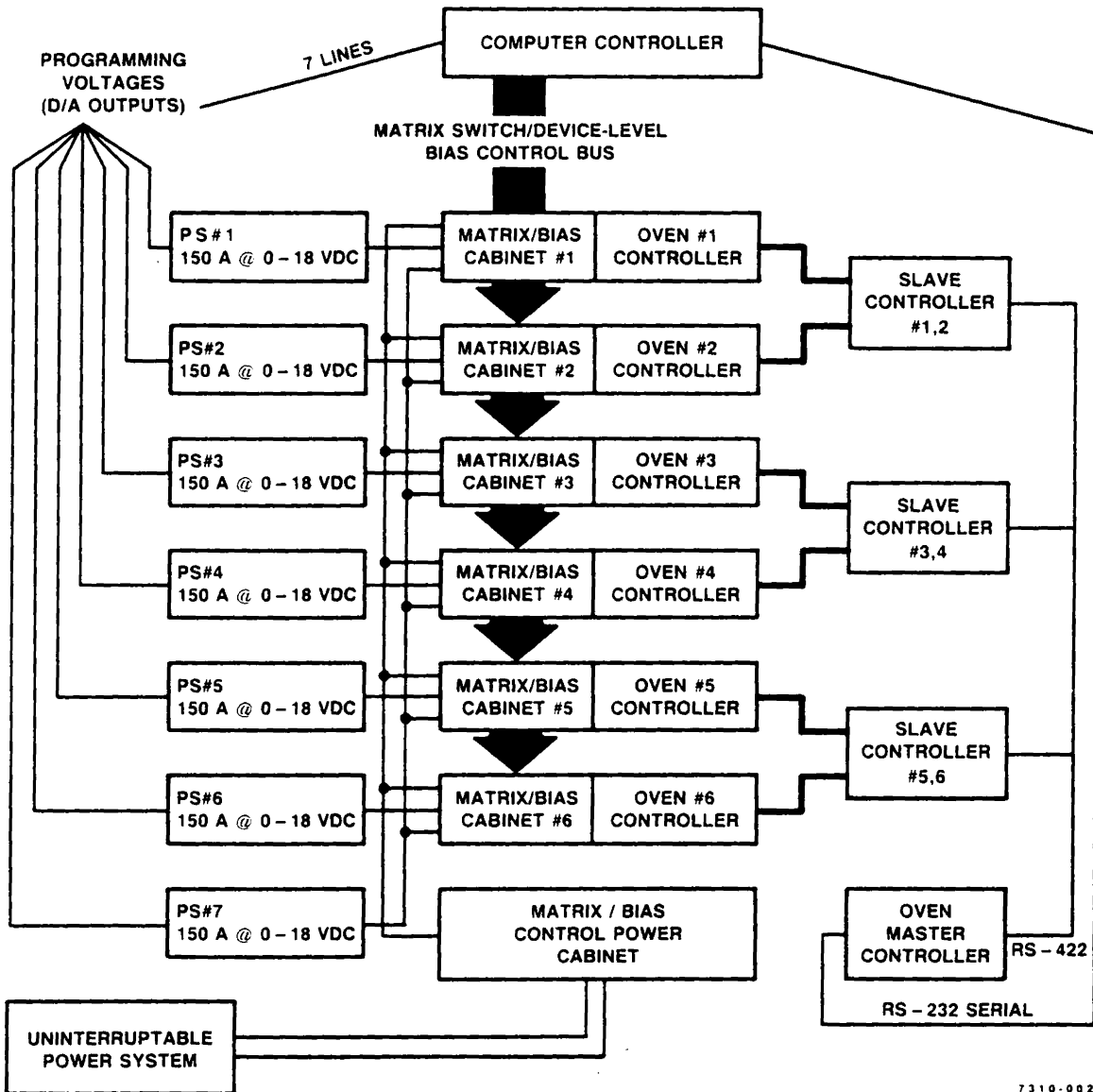
5.1.1.2 Bias Power/Matrix Switching and Oven Control

Figure 5.2 is a block diagram showing the key elements of the bias power and matrix switching section of the accelerated life test system. Also indicated in the block

diagram is the oven control hardware and computer interface.

Device-level bias control, which allows the simultaneous life testing of many different device types within the same oven, is the key to the test system's versatility. Each test position has two programmable linear regulators for life test biasing: one low current (250 mA) -12.5 to 0.0 Vdc, and one high current (3 A) 0.0 to +12.5 Vdc with on-board D/A converters and latches. A custom cabinet behind each oven contains the 128 regulators and mercury-wetted switching matrix relays required to bias and switch 64 devices. The mercury-wetted relays are utilized for high reliability, long life, and low contact resistance. The relays are capable of switching 3.0 amperes and carrying 5.0 amperes, and therefore, are suitable for power devices designed for approximately 10 watts RF power output assuming 33% power added efficiency and 30 watts (3 amperes at 10 volts) dc power dissipation.

Bulk dc power for all devices originates in seven voltage-programmable, 0.0 to 18.0 Vdc, 150 ampere power supplies. These bulk power supplies function as "smart preregulators" for the device-level life-test regulators and are located in an equipment desk adjacent to the computer/controller and measurement system. The computer/controller sets the bulk bias supplies automatically to minimize the power dissipation in the linear regulators by monitoring the voltage requirements within each oven. A positive bulk



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Figure 5.2 Bias power/matrix switching and oven control system.

supply is required for each of the six ovens. A seventh 150 ampere bulk supply provides the negative voltage power for the entire test sample. Although 384 good MESFET devices will draw very little current and require only a small negative supply, interchangeability of power supplies was a reliability requirement for the system; hence the 150 ampere negative power supply. The bulk supplies are programmed through amplifiers driven by STD Bus D/A converter cards with an optical isolator circuit required for the single supply with a negative output, where a floating programming voltage is needed. The device-level regulators and matrix switching are programmed via a parallel control bus.

The oven control hardware and interface is also shown in Figure 5.2. The ovens are equipped with microprocessor controlled temperature controllers capable of transmitting both temperature and status information back to the computer/controller. The computer/controller communicates with a master oven controller via a serial RS-232C interface. The master oven communicates with three slave oven controllers via a serial RS-422 interface for reliable long distance communication. Each of the three slave oven controllers communicates with two ovens via parallel interfaces.

5.1.2 Fixturing

A formidable task in the tester development was the design of the high temperature fixturing (Figure 5.3).

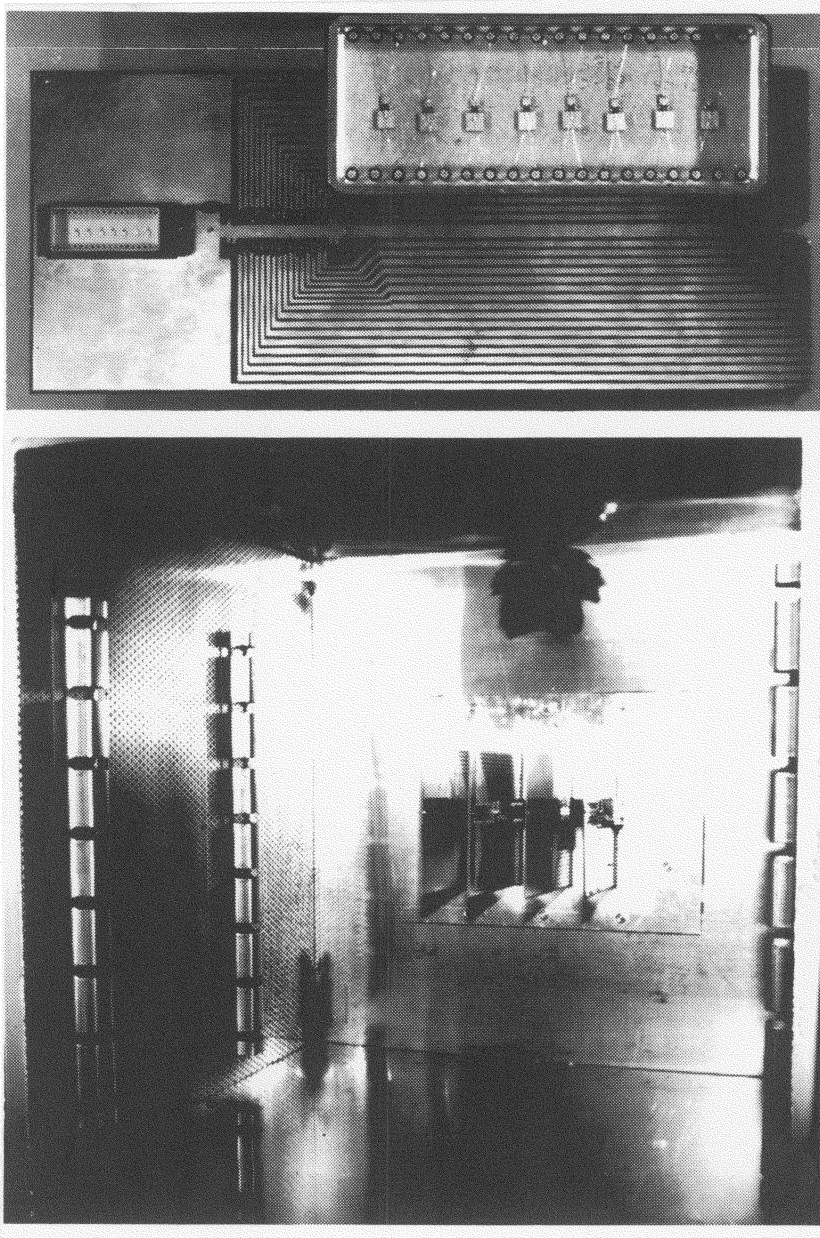


Figure 5.3 Circuit board test vehicle package with 8 devices (inset), and installed high temperature fixturing.

Biasing and test power for 64 test positions requires over 250 conductors to traverse the oven walls, thereby experiencing both high oven temperatures and temperature differentials. Although the ovens used in the test system feature a nitrogen atmosphere to minimize test fixture oxidation, it was expected that periodic replacement of the fixturing components would be required to insure reliable measurement performance. Traditional methods of utilizing nickel wire with welded connections and ceramic fixturing materials were not feasible for this application for numerous reasons. They are high in cost, difficult to use, and tedious to replace. It was decided that a circuit board-like oven feedthrough scheme would provide the best solution to the problem in terms of accessibility, reliability, and repairability. A card cage with edge connectors was mounted outside the oven walls allowing the connectors to operate at or near room temperature. The board material would have to survive 280°C temperature differentials and withstand some flexing during installation. Ceramic is very tolerant of high temperatures but is susceptible to failure in applications with either large temperature differentials or flexing. Ceramic-on-steel circuit boards used by the telephone industry were considered, however, in addition to their high cost, the lead time for their fabrication was unacceptable. Because this was the first attempt at fixturing for 300°C, it was important that the boards be fabricated quickly and evaluated for necessary

changes. A thorough investigation of available feedthrough circuit board materials was undertaken and a suitable low cost (relative to ceramic) material was found. PTFE/glass microwave laminates offer many advantages over alumina substrates for micro-stripline applications. These materials come in a variety of thicknesses and dielectric constants and are rated for microwave applications up to approximately 275°C depending upon the manufacturer and specific composition. The material is suitable for dc operation to much higher temperatures with a gradual decrease in strength with increasing temperature. Two different board constructions are available for microwave laminates. The first and earliest type developed features a woven construction. The second type, which is favored for improved microwave performance because it has a more uniform dielectric features a "particle-board"-like construction. The woven construction was selected because it is lower in cost and stronger; a definite advantage at higher temperatures. There are a few guidelines which must be followed if reliable operation is to be achieved at high temperatures for extended periods of time.

- 1) The conducting runs must be heavily plated with nickel.
- 2) The conductor widths must be maximized to insure good adhesion to the board material.
- 3) Plated through holes should be avoided to minimize cost.

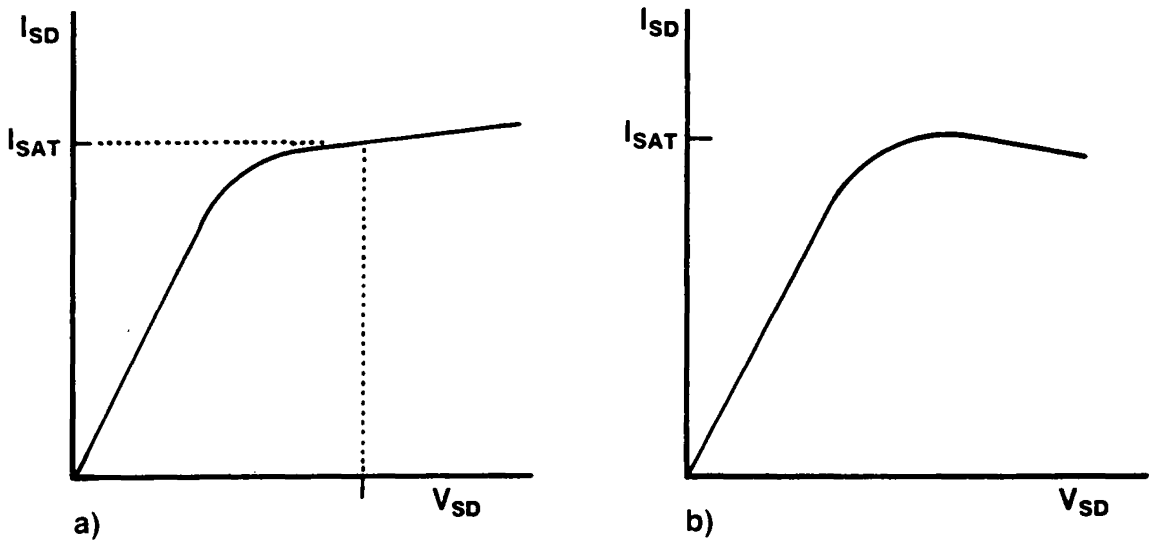
Two test-vehicle sockets were mounted on each oven-feedthrough card, one on each side of the board, to eliminate the need for plated through holes. The conductor fingers were gold plated to mate with high reliability gold-plated over beryllium-nickel card edge connectors mounted in an aluminum card cage bolted to the rear of the ovens. The four cards (16 test positions per card) required per oven were inserted through a four-layer gasket seal composed of a layer of microwave laminate and a layer of silicone rubber located on both sides of the rear wall of the test chamber. This design provided excellent heat transfer isolation and allowed the card edge connectors to operate only slightly above room temperature with the oven at 300°C. No appreciable degradation in the appearance or electrical characteristics of the boards has been noted after over 2000 hours at 280°C. The total cost for the 24 circuit boards required to fixture the entire 6 oven system was \$2500. This is exceptional performance at low cost.

In order to accommodate on-board bypass capacitors and ICs of moderate size, a 40-pin solid-sidewall dual-in-line package (DIP) was chosen as the test vehicle for eight test positions. These packages were placed into zero-insertion-force sockets (ZIF) rated to 300°C. High reliability ZIF sockets with a 300°C rating do not yet exist for flatpacks. This would have been the preferred package in the event dynamic testing was desired in the future. The test sockets were

then soldered to the oven-feedthrough cards with 305°C eutectic solder. Microwave ceramic bypass capacitors of parallel plate construction (gold coating over nickel barrier plates) were eutectically die attached (Au Sn preforms) to the hybrid package in close proximity to the MESFETs to minimize oscillations. Ferrite beads are of no use at these temperatures because they become paramagnetic. Although these capacitors are not rated to 300°C by the manufacturer, there is no reason, to the author's knowledge, why their construction would be problematic at that temperature. The manufacturer simply states that he has no way of testing them at these temperatures. Thousands of biased hours at temperature have produced no bypass capacitor failures in the reliability test system.

5.1.3 DC Measurements

Microwave devices are susceptible to unwanted oscillations during automated dc characterization. These oscillations are particularly problematic on devices with high transconductance (g_m), unless proper bypassing and/or termination techniques are applied. Generally speaking, these oscillations appear on MESFET transistor I-V characteristics just past the knee voltage where all or some of the drain current vs drain voltage curves at different gate biases bend downward as shown in Figure 5.4. Microwave ceramic chip capacitors in the 100 to 680 pf range mounted as close to the device-under-test as possible eliminated 99% of



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Figure 5.4 IV characteristics for stable and unstable bias conditions.

the oscillation problems in the test system, however, minor peaking would occasionally appear in some I-V characteristics. Test software modifications were implemented to provide accurate dc characterizations under these conditions. Because of the ability of the test system to test both low noise/small signal and power MESFETs, a variety of current levels are necessary to provide accurate dc characterizations for different device peripheries. In cases like these, current sources are more useful than voltage sources, however, they can readily destroy devices under test in the event of a momentary open circuit caused by a bouncing relay or other timing problem. In order to keep the measurement system simple, the cost low, and the devices safe from accidental destruction, it was decided that voltage, not current sources would be used as test bias supplies. This limitation increases test times because the voltage sources must be incremented to find desired current levels with the smallest increment being the voltage source's resolution (50 mV). Current levels for forced gate current are derived from desired current densities and gate Schottky dimensions.

5.1.3.1 Determination of I_{dss}

I_{dss} is derived by setting the gate voltage (V_{gs}) = 0.0 and measuring the drain current I_d at $V_{ds} = 3.0 V_{dc}$ and at $V_{ds} = 1.5 V_{dc}$ (this is approximately the bias where peaking

occurs in the event of minor oscillations). I_{DSS} is assumed to be equal to the larger (more stable) of the two current levels. The drain voltage corresponding to the more stable drain current is stored and used as the drain bias in the determination of transconductance (g_m).

5.1.3.2 Determination of R_S , R_G

R_S and R_G are derived by forcing a positive current into the gate of the MESFET with the source grounded and the drain open. If this current is of sufficient magnitude to turn the Schottky diode "on", the diode I-V characteristic becomes approximately linear. A current density of approximately 10^4 amperes per square centimeter is sufficiently high to reach this region of operation. This corresponds to 30 mA for a MESFET with gate dimensions of 1 x 300 microns. A simple formula is used to determine the magnitude of the required gate current expressed in milliamperes:

$$I_g = L \times W \times .1$$

where

L = gate length in microns

W = gate width in microns

The slope of the characteristic is equal to the inversion of the sum of R_G and R_S . With the drain open circuited ($I_D = 0.0$ and $I_S = I_g$) and a known gate current (I_g), R_S is

obtained by measuring the open circuited drain voltage (V_{ds}) and dividing by the gate (source) current (I_g). R_g is then determined by subtracting R_s from the inversion of the diode characteristic slope. Mathematically,

$$R_g + R_s = 1/\text{SLOPE} \quad \text{diode "on" resistance}$$

$$R_s = V_d/I_g$$

$$R_g = (1/\text{SLOPE}) - R_s$$

5.1.3.3 Determination of Transconductance: g_m at full, .5, and .2 I_{dss}

MESFET transconductance is a measure of the variation in drain current as a function of a variation in gate-source voltage (V_{gs}). It is therefore, determined by measuring the gate-source voltages, which produce drain current levels of I_{dss} , $.5 I_{dss}$, and $.2 I_{dss}$ at a stable drain bias, varying the gate potential by a small amount ($0.1 V_{dc}$) around these values, and measuring the subsequent drain currents. By dividing the change in drain currents by the variations in gate voltage required to produce those changes, the transconductances are determined. The change in drain current at half I_{dss} resulting from a $0.1 V_{dc}$ change in V_{gs} is stored to aid in the expeditious determination of V_p .

5.1.3.4 Determination of R_o

The output resistance R_o is determined by taking the inverse of the saturation-region slope of the MESFET I-V characteristic corresponding to a single gate voltage

potential. The two drain voltages utilized to determine the run of the slope were:

$V_{ds1} = .75 \times \text{the accelerated life test drain voltage}$

$V_{ds2} = .75 \times \text{the accelerated life test drain voltage} - 0.75 V_{dc}$

The wide voltage spacing between these points was a requirement because the slope of the I-V characteristic in the saturated region is very small (typically .001-.002), and therefore, small variations in the measurements will produce large fluctuations in the calculated value of R_0 when inverted.

5.1.3.5 Determination of Pinch-off Voltage V_p

The pinch-off voltage is the gate-source voltage required to reduce the drain current to a certain percentage of I_{dss} (usually 2%). One must be careful in applying this definition in the establishment of proper test procedures at high temperatures. At room temperature, the drain-to-gate leakage currents (typically 1 microampere or less) of low-noise/ small-signal GaAs MESFETs with 300 micron gate widths are insignificant compared to the drain-source currents (typically 30-60 milliamperes). Pinch-off is readily determined by monitoring drain current in the drain lead. At high temperature these leakage currents become significant because of the exponential temperature dependence of the leakage current of the reverse biased Schottky. The current measured in the drain lead will never fall to 2% of I_{dss} if the leakage

component alone exceeds that value. Therefore, the gate current (which is negative) must be measured and added to the current measured in the drain lead to determine the actual current flowing from the drain to source. When the calculated drain-source current reaches 2% of I_{DSS} , pinch-off is established.

In order to minimize the number of increments of V_{GS} required to determine V_p , a starting point is selected based upon measurements taken during the determination of g_m . In general, g_m decreases only slightly between I_{DSS} and half I_{DSS} , and then falls more rapidly as V_{GS} approaches pinch-off. By dividing I_{DSS} by the change in drain current due to a $0.1 V_{DC}$ change in V_{GS} (noted in the determination of g_m at half I_{DSS}), and subtracting $0.1 V_{DC}$ from that value to account for the drop in g_m with decreasing drain current, an initial value is established for the determination of V_p . This algorithm will typically result in an initial bias voltage for V_{GS} which produces a drain current in the 10-20% of I_{DSS} range. By subtracting $.5 V_{DC}$ from V_{GS} until I_D is less than 2% of I_{DSS} , adding $.2 V_{DC}$ until I_D is greater than 2% of I_{DSS} , and interpolating between the last two measurements, V_p is typically determined within $0.1 V_{DC}$ in two or three measurements.

5.1.3.6 Determination of C_{GS} , C_{GD}

The values of C_{GS} and C_{GD} are inserted into the MAG (Maximum Available Gain) equation to provide an estimation of

expected MESFET microwave performance as a function of all parasitic resistances and transconductance. Measurement of these parameters is not practical with the cable lengths required of a test facility of this physical size. The capacitance values are calculated based upon gate dimensions of the MESFETs under test and theoretical relationships based upon expected implant schedules for different device types.

Low-noise/small-signal MESFETs are typically less than 600 microns in gate width. They are implanted at high doses and low energies to increase gain and reduce noise figure. V_p values are typically -1.0 to -3.0 V_{dc} due to the thin channel layer resulting from the low implantation energy. Capacitance is proportional to gate periphery ($L \times W$) and to doping level which effects the dielectric constant of the GaAs channel. Drain-to-source spacing is 4 microns, and therefore, a 1 micron gate, centered between the drain and source will produce 1.5 micron gate-to-source and gate-to-drain spacings. Typical values for these devices with 1 x 300 micron gate structures are:

$$C_{gs} = .4 \text{ pf} \quad \text{and} \quad C_{gd} = 0.26 \text{ pf}$$

Therefore, the algorithms used to calculate C_{gs} and C_{gd} are:

$$C_{gs} = .4 \times \text{gatelength} \times \text{gatewidth}/300$$

$$C_{gd} = .026 \times (\text{gatewidth}/300) \times (3/(4-\text{gatelength}))$$

Power MESFETs are typically greater than or equal to 600 microns in gate width. They are implanted with lower doses and higher energies to provide deep channels for high current levels, high breakdown voltages for high power output, and high pinch-off voltages to allow large voltage swings without gain suppression. Because of the relationship between doping and pinch-off voltage, V_p values are typically 4-8 V_{dc} . The capacitances are reduced as a result of the lower doping levels but this tends to be offset by the use of thinner substrate material for reduced thermal impedance. Because of the combined effects of high implant energy, increased channel depth, and reduced implant dose and substrate thickness, the calculation of C_{gs} is not a straightforward adaption of the low noise/small signal C_{gs} algorithm. For comparison purposes, a typical power MESFET with a 2.5 mm gate periphery has a C_{gs} value of half I_{dss} of 2.5 pf. C_{gs} is roughly proportional to the square root of the doping level which tracks closely with V_p . The following algorithms were used to estimate the values of C_{gs} and C_{gd} in power MESFETs:

$$C_{gs} = .52 \times \text{gatelength} \times (\text{gatewidth}/300) \times \text{SQRT}(\text{ABS}(-2.0/V_p))$$

$$C_{gd} = .026 \times (\text{gatewidth}/300) \times (3/(4-\text{gatelength}))$$

5.2 Accelerated Life Testing

GaAs devices and ICs will most likely form the basic active building blocks from which a major portion of military,

supercomputer, and high speed communication equipments will be built in the 1990's. Much of this equipment will be required to operate in avionics, space, and other applications where hostile environments will require GaAs performance. Exceptional reliability is a requirement because of the critical nature of these equipments and because the accessibility for maintainability for these components will be limited. Because of the present state of process development of most GaAs pilot line facilities, accelerated life testing is required to provide process feedback on reliability of devices fabricated with experimental processing techniques and materials. This must be accomplished in a reasonable time frame.

Many failure mechanisms involve the diffusion of atoms and possess an Arrhenius type time-temperature dependence; i.e., a reaction rate which is exponentially dependent on the inverse temperature and characterized by an activation energy. The most common failure mechanism for low-noise/small-signal MESFETs with CrAu, TiPtAu, and TiPdAu gate metallization is gate metal (Au) interdiffusion with GaAs resulting in an effective reduction in channel thickness due to a less than optimal diffusion barrier. This failure mechanism has been shown to be activated by temperature, not bias voltage. Therefore, an accelerated high temperature-storage life test of traditional recessed gate TiPdAu MESFETs was initiated in the life test facility. Temperatures in the 243-280°C range

were used to accelerate degradation. A 6 hour test interval was selected with automated dc measurement of the critical parameters as described in the previous section. A 20% change in I_{DSS} , commonly used in the literature as a failure criterion, was evaluated.

5.3. Reliability Comparison of Recessed Gate MESFETs, Realigned Self-Aligned Gate (RSAG) MESFETs, and Planarized Self-Aligned Gate (PSAG) MESFETs

A comparison was made between Recessed-Gate analog MESFETs (widely used analog process), and two analog derivatives of a Self-Aligned Gate MESFET (widely used digital process). All gate fabrication processes are based upon Au gate metallization with different diffusion barriers. The performance of their diffusion barriers and susceptibility to extrinsic failure due to processing variation were studied. Changes in the critical device parameters I_{DSS} , R_g , R_s , R_o , g_m , and V_p over time at elevated temperatures were compared. The effects of these changes on MAG (Maximum Available Gain) and the application of this information toward the selection of a meaningful failure criterion for accelerated life studies was discussed. In order to understand the basic differences between these devices and how they relate to microwave and reliability performance, a review of their fabrication is in order, Figure 5.5 shows the basic device structure for the recessed-gate, realigned self-aligned gate, and planarized self-aligned gate devices.

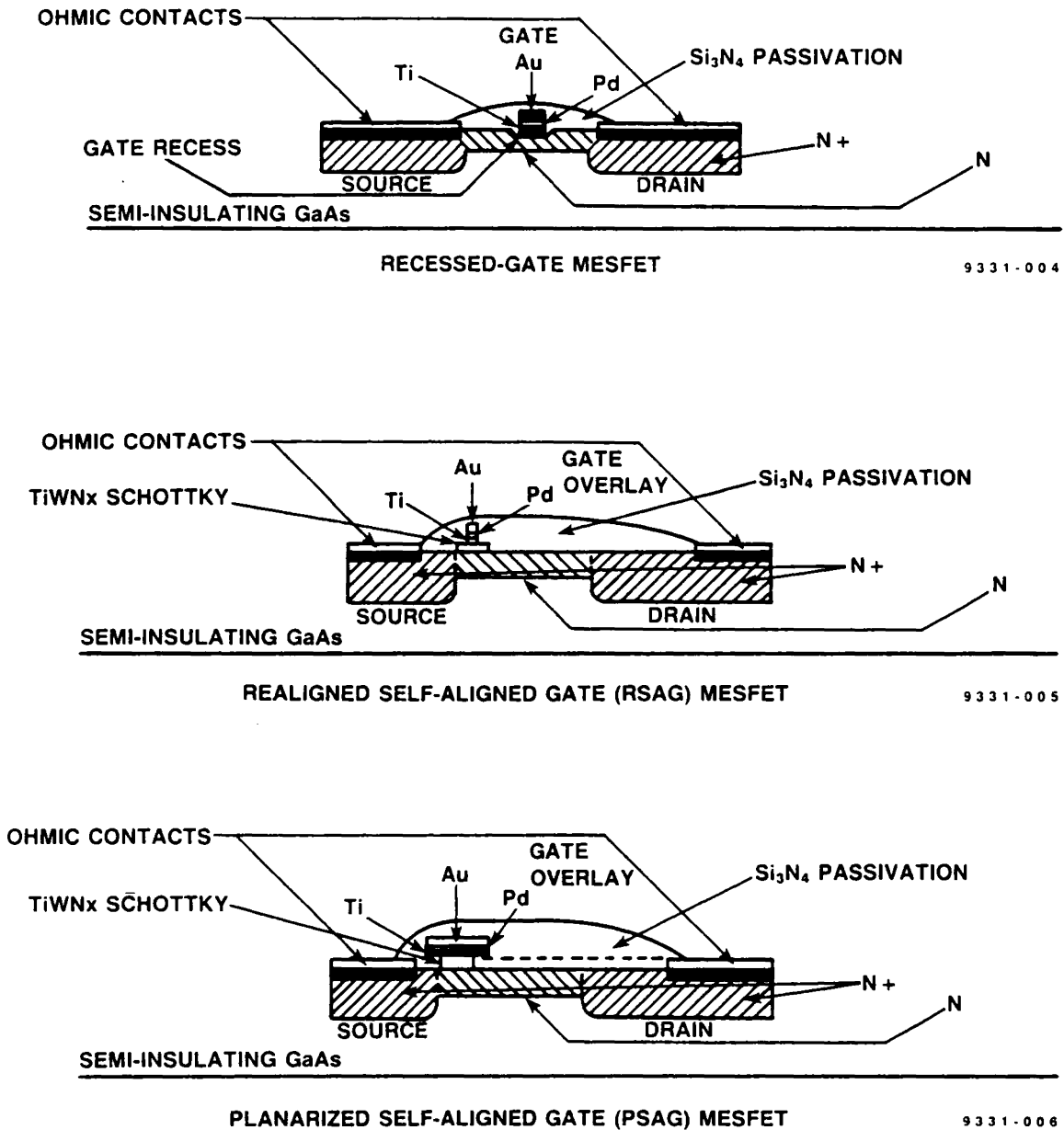


Figure 5.5 Device structures: recessed-gate, realigned self-aligned gate (RSAG), and planarized self-aligned gate (PSAG) MESFETs.

5.3.1 Recessed-Gate TiPdAu MESFETs

Recessed-gate MESFET technology dominates the GaAs industry in the analog/microwave segment. The channel and N⁺ doping are accomplished through selective ion implantation. The channel implant dose is selected to provide maximum microwave performance in the frequency band of interest. The ohmic contacts are formed and alloyed, and a channel recess is etched using a wet etching technique between the source and drain until a desired drain-source current is reached. The gate is then formed in the recess between the source and drain. In order to minimize the source resistance R_S and maximize the drain resistance R_D and breakdown voltage, the gate must be positioned as close to the source as possible within the limitations of the photolithography. There are two drawbacks to the fabrication process which reduce uniformity and manufacturability:

- 1) The wet recess etch is hard to control, and it is difficult to keep the gate Schottky area clean. The wafers must be rinsed after the wet etch before they can be loaded into an evaporator for deposition of the gate metallization.
- 2) The channel region conductivity is much lower than the N⁺ regions under the ohmic contacts. Therefore, the placement of the gate in the channel greatly affects the source resistance, extrinsic g_m , and gate-source capacitance C_{gs} .

Common gate metallization schemes include TiPtAu, TiPdAu, and TiAlTi, where Ti is the adhesion layer and Schottky contact, Pt or Pd act as a Au diffusion barrier, and Au or Al act as the conducting metal. (The Ti over the Al is required as a corrosion barrier to prevent Al_2O_3 formation.) Recessed gate MESFETs fabricated with TiPdAu gates were used in this study.

5.3.2 Self-Aligned Gate (SAG) MESFETs

Self-aligned gate MESFETs have been used extensively during recent years in the fabrication of GaAs digital ICs. They differ greatly from recessed gate devices in the following ways:

- 1) Doping of the active channel with selective ion implantation alone determines the I_{DSS} of the finished device. No recess etch is employed to thin the channel to the desired thickness. By carefully controlling the selective implant schedule, both enhancement and depletion mode devices can be fabricated on the same circuit. This is the principal in GaAs E/D logic.
- 2) The gate forms the N^+ implant mask for the ohmic contacts. The N^+ region, therefore, self-aligns to the edge of the gate lowering the source and drain resistances R_{S} and R_{D} , and increasing g_{m} for improved performance. In addition, the technique is

inherently tolerant of variations in lithography, and therefore, more manufacturable.

- 3) Because the gate structure forms the N+ implant mask, it must survive the 850°C implant anneal process. A Schottky capable of surviving this process step without interdiffusion should be very reliable.

Typical Schottky compositions are TiW and TiWN_x.

There are, however, three basic drawbacks to the self-aligned gate MESFET as processed for digital circuits which make it unsuitable for microwave applications:

- 1) The TiW and TiWN_x Schottky gate resistance is an order of magnitude higher than TiPdAu and would result in a significant gain reduction if utilized without modification. Thus an Au overlay metal is required because high R_g reduces MAG.
- 2) The reduction in R_d and consequential increase in output conductance is undesirable from a microwave gain standpoint.
- 3) The self-aligning, highly doped N+ implant region results in a significant reduction in breakdown voltage.

It is important to note at this time that if a high-performance analog MESFET could be processed using self-aligned gate technology, digital and analog circuit elements could readily be combined on the same IC and fabricated with one process. This would represent a very significant breakthrough. This was accomplished.

5.3.2.1 Realigned Self-Aligned Gate (RSAG) MESFET

This device represents an initial attempt to fabricate a self-aligned gate microwave (analog) device. In order to lower the output conductance and increase the breakdown voltage to acceptable levels, a mask level was added to produce a stripe of photoresist a few microns wide extending from the nominal center of the gate toward the drain to form part of the N⁺ implant mask. This moved the highly-doped N⁺ region away from the gate edge. In order to reduce the high gate resistance of the 1 x 300 micron TiWN_x Schottky, a .5 micron TiPdAu 50 nm/50 nm/500 nm overlay metal was carefully centered on the TiWN_x by photolithography. It was decided that, although the success of this technique hinged upon a very critical alignment, it could be attempted with the purchase of only one additional mask level for the photoresist stripe (the .5 micron gate mask was already in hand). By simply determining the proper implant schedule and making one very critical alignment, the Realigned Self-Aligned Gate device was successfully fabricated. The expected improvements in gain and uniformity of the self-aligned gate process were realized.

Although the RSAG MESFETs exhibited excellent results, there were two major concerns which led to a further development of the process. First, the alignment of the .5 micron TiPdAu overlay metal to the center of the TiWN_x Schottky was critical to the reliability of the device and difficult to

achieve in a production mode of operation. The benefits gained in manufacturability of a self-aligned gate process could easily be nullified by the difficulty and criticality of the TiPdAu alignment. From a reliability standpoint, any misalignment of the TiPdAu which resulted in its missing the TiWN_x (an excellent diffusion barrier), and contacting the GaAs channel, would result in Au interdiffusion with GaAs at elevated temperature. Electrically, misalignment would appear as a slight increase in gate-source capacitance and reduction in g_m because the actual Schottky gate length would be increased, however, at high temperature the degradation rate would be much higher than one would expect for devices with proper alignment. Secondly, although the RSAG devices exhibited excellent performance for MESFETs with a 1 micron gate length, going to shorter gate lengths (.5 micron) for higher frequency operation would certainly pose a difficult problem. Aligning a .5 micron TiPdAu overlay metal to a 1.0 micron TiWN_x Schottky requires an alignment tolerance of .5 micron. Aligning a .25 micron TiPdAu gate to a .5 micron TiWN_x Schottky reduces the tolerance to .25 micron. Although direct-write electron beam lithography has been used to fabricate .25 micron gates in GaAs MESFETs, it is far from a production-worthy technique.

5.3.2.2 Planarized, Self-Aligned Gate (PSAG) MESFET

The Planarized, Self-Aligned Gate (PSAG) MESFET was developed to address the manufacturability and high frequency performance concerns of the RSAG MESFET stemming from the critical nature and difficulty of the realignment process. The fabrication process for PSAG devices is identical to the RSAG process up through the TiWN_x Schottky formation. The TiWN_x layer is typically 200 nm thick and rises accordingly above the GaAs surface. On PSAG devices the cross-section is then planarized by coating the devices with a passivating dielectric. By reactive-ion etching the dielectric and utilizing end point detection, the TiWN_x Schottky is again exposed. Careful control of the etch chemistry is required to match the dielectric and TiWN_x etch rates to avoid removing either the entire Schottky or the entire passivation layer once the end point is reached. With the 1 micron TiWN_x Schottky exposed and the entire MESFET channel covered by passivation, a large (1.5 micron) TiPdAu gate stripe can readily be deposited forming a T-gate structure requiring an alignment accuracy of only 2.5 microns (1.5 + 1.0). The passivation under the T eliminates the potential reliability problem encountered in misaligned RSAG MESFETs.

CHAPTER VI

EXPERIMENTAL RESULTS

6.1 Accelerated Life Test Facility

The life test facility performed well during the experiment and excellent data was obtained. Although the test sample was small, the equipment would have readily performed the test on a large sample had the parts been available. Although the topic of this paper was an unbiased storage test, the equipment was used to test another sample of recessed gate devices at bias and performed well. Figures 6.1, 6.2, and 6.3 show typical diode characteristics, transistor I-V curves, and trend plots respectively generated by the test facility as a result of operator keyboard commands. The low cost fixturing performance was exceptional, with no feedthrough or bypass capacitor failures, and few oscillation problems after thousands of hours of use at temperatures up to and including 300°C.

6.2 TiPdAu Recessed Gate MESFET 1000 Hour Life Test

Recessed-gate MESFETs with TiPdAu gate metallization were subjected to a 1000 hour storage test at 261.5°C and 280°C, and characterized on 6 hour intervals. The data obtained from the dc characterizations at 261.6°C is summarized in Table 6.1. Table 6.2 lists the average percentage changes in these same parameters after 1000 hours. All of the devices at both temperatures failed according to

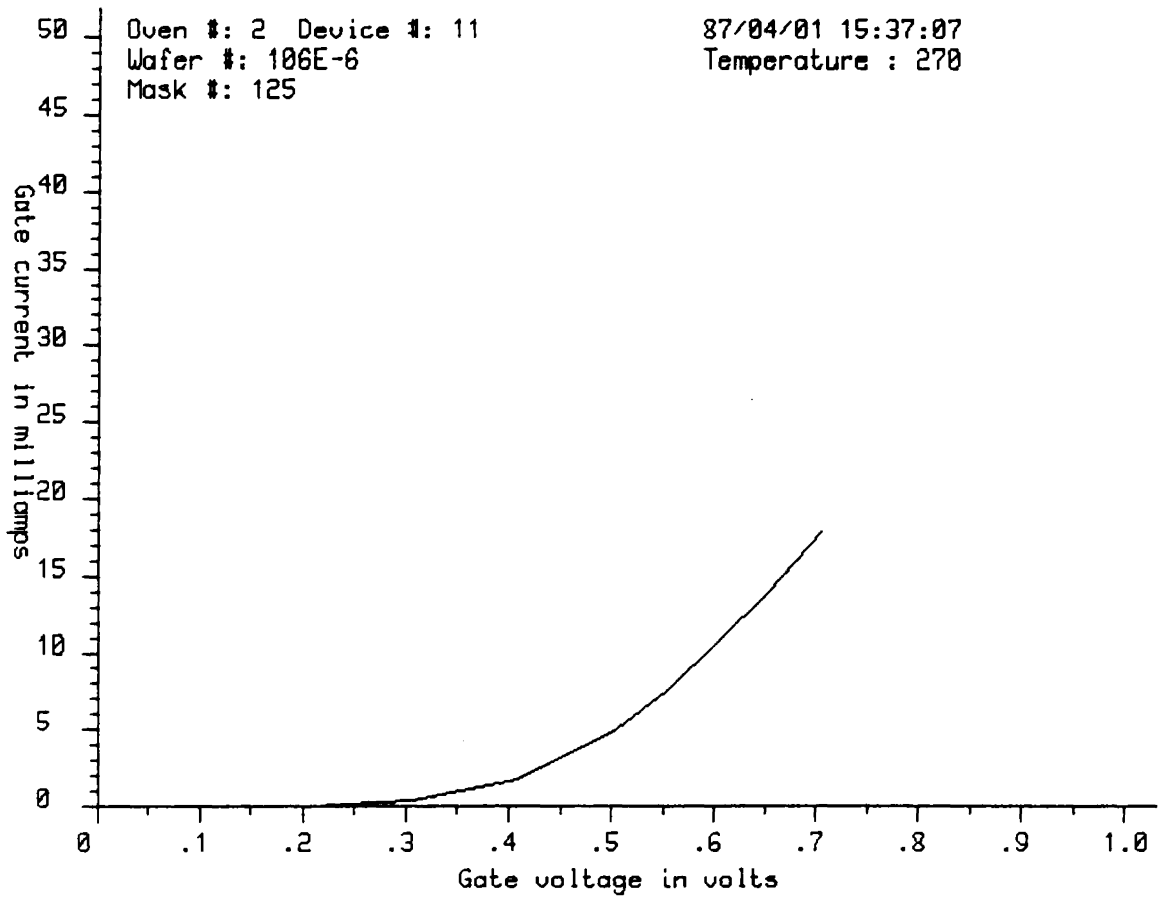


Figure 6.1 Tester generated diode characteristic plot.

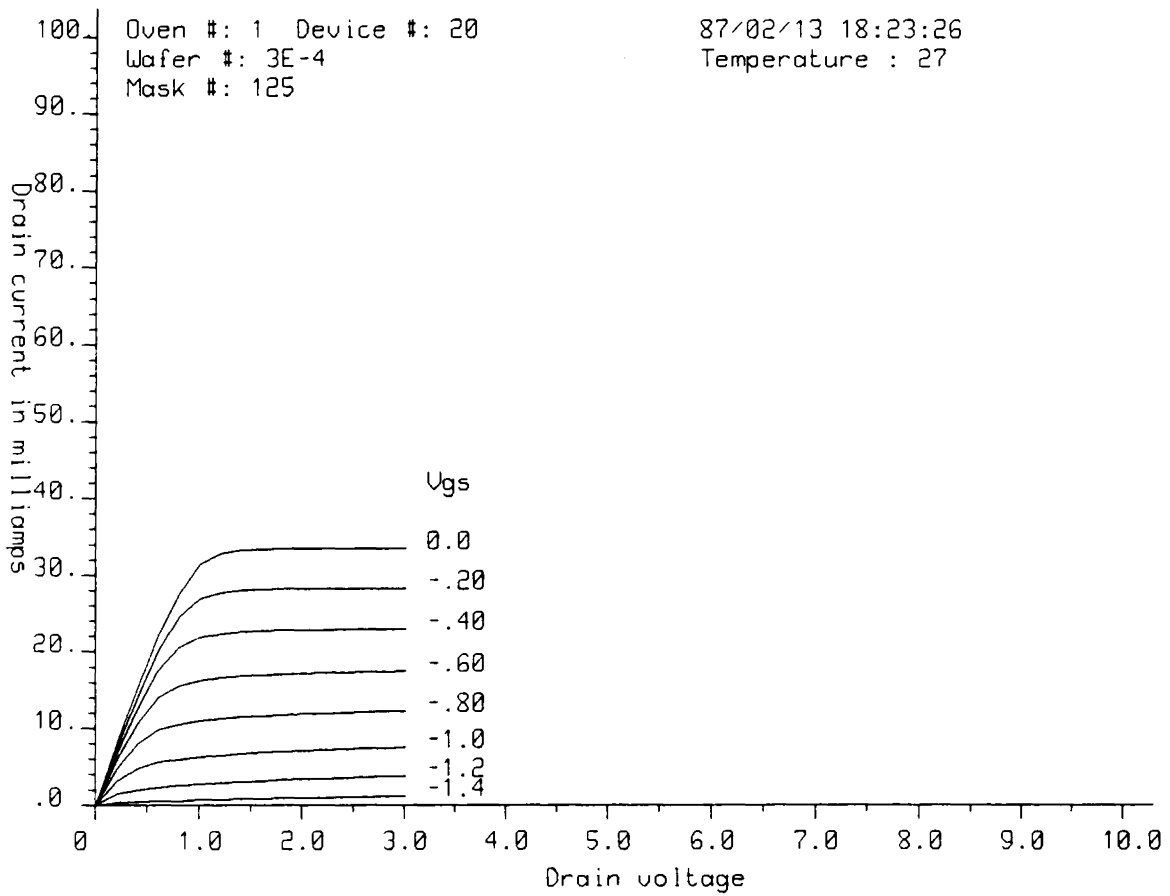


Figure 6.2 Tester generated MESFET I-V characteristic plot.

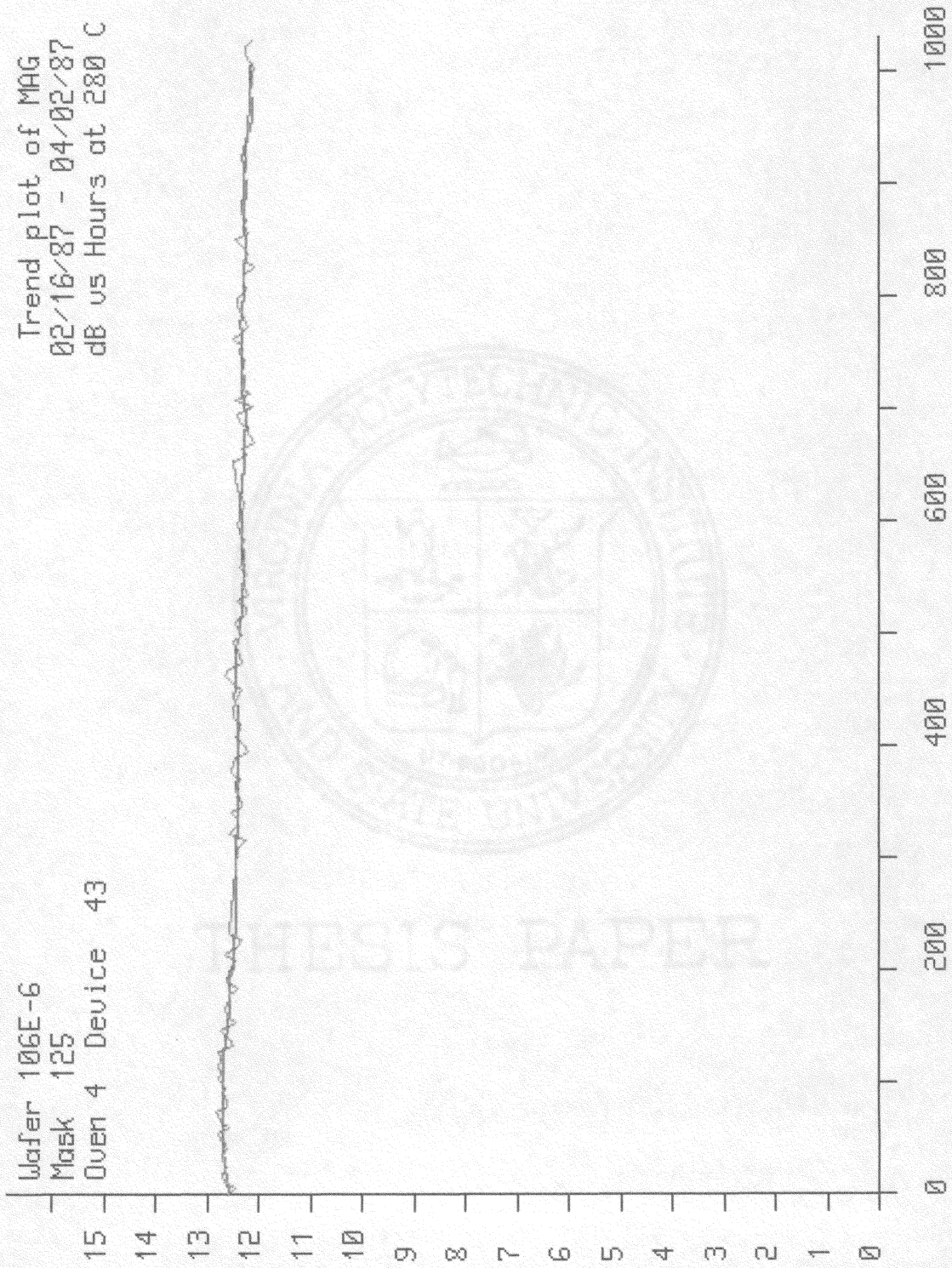


Figure 6.3 Tester generated trend plot of MAG vs. time at 280°C.

the 20% change in I_{dss} failure criterion. All channel related parameters degraded substantially; I_{dss} 28.2%, V_p 24.2%, R_o 30%, R_s 8.4%, and g_m at half I_{dss} 14%. The gate resistance R_g was quite stable, however, changing only 2%.

TABLE 6.1 Average dc parameter data for 5 recessed-gate MESFETs stored at 261.5°C for 1000 hours.

HRS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	$(.5 I_{dss})$ g_m (mS)	MAG (dB)
0	46.0	-1.78	7.2	5.48	646	39.7	33.2	10.6
1000	433.0	-1.35	7.4	5.94	452	38.3	28.7	8.8

TABLE 6.2 Average percentage change in dc parameter data for 5 recessed-gate MESFETs stored at 261.5°C for 1000 hours.

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{g_m}$	$(.5 I_{dss})_{g_m}$
-28.2	-24.2	+2.0	+8.4	-30.0	-7.0	-14.0

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -1.8 dB

At 280°C the parameters are likewise degraded. Tables 6.3 and 6.4 list the dc characterization data and average percentage changes respectively. At 280°C, I_{DSS} decreased 37.6%, V_p increased (became less negative) 36%, R_s increased 15.4%, R_o decreased 21.4%, g_m at half I_{DSS} decreased 25.6%, and R_g remained essentially unchanged (-.3%). The changes tabulated in the tables corresponding to recessed-gate devices are conservative at best. The exponential degradation rate in the measured device parameters is very high above 280°C. Eutectic die attach of the devices with AuSn preforms was done at approximately 340°C. Retrospective hot chuck measurements confirmed that unless all devices undergo this high temperature procedure in unison, erroneous life predictions are inevitable. Devices which receive additional heating will degrade slower than expected for that temperature. This was the case for the 280°C devices. A median life of 430 hours was determined for the recessed-gate devices at 261.5°C. Although not formally presented in this study, 2 devices were tested at 243°C. Neither device had failed after 1000 hours of storage. Extrapolation of the I_{DSS} degradation in these devices yields a median life of approximately 2100 hours. Solving graphically for the activation energy yields a value of approximately 1.7 eV (Figure 6.4) which is consistent with values reported in the literature.

It is notable that many GaAs companies selling their devices commercially in chip form continue to utilize Al gate metallization in spite of the electromigration, corrosion, and AuAl intermetallic problems associated with using the metallization for power devices and in conjunction with gold-based processes. Because Al does not react with GaAs up to approximately 400°C, it is very tolerant of die attach temperatures.

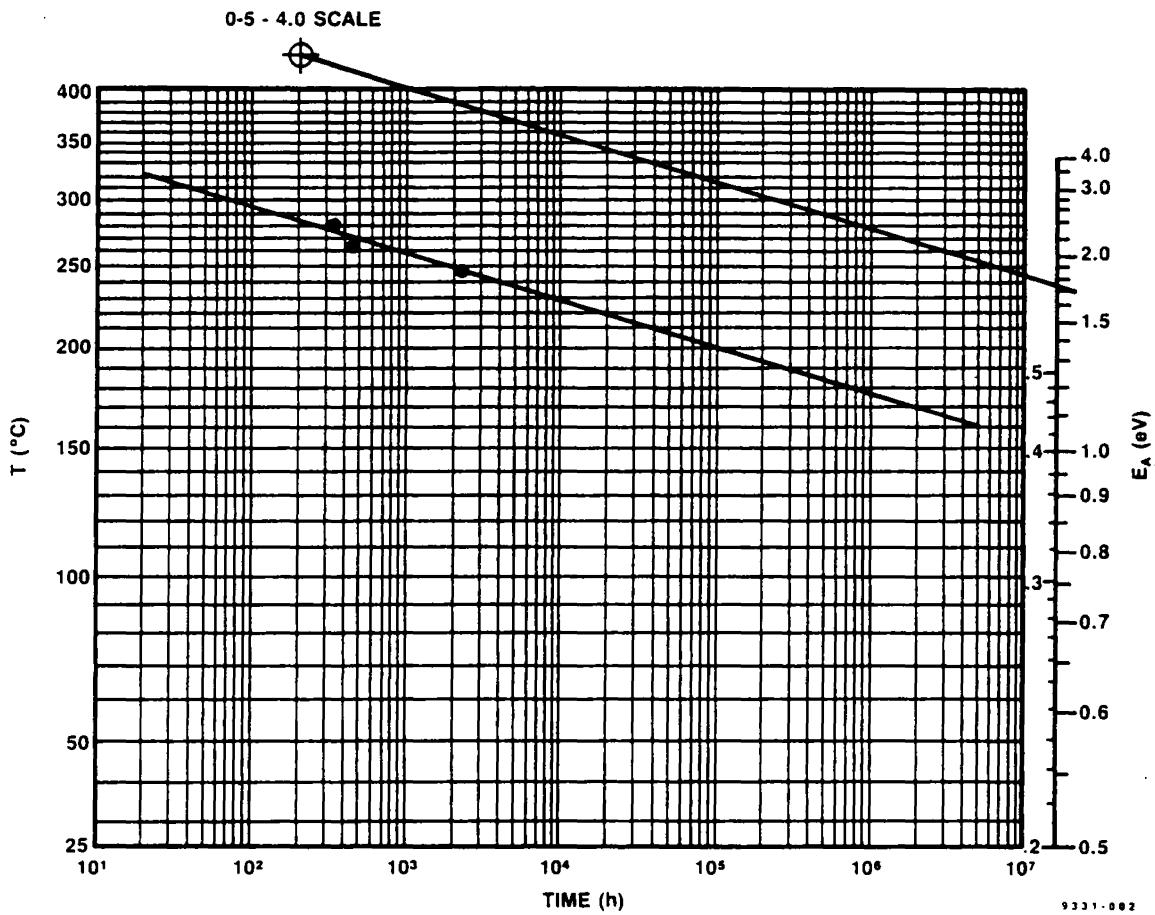


Figure 6.4 Median life and graphically derived activation energy plot for TiPdAu recessed-gate devices.

TABLE 6.3 Average dc parameter data for 7 recessed-gate MESFETs stored at 280°C for 1000 hours.

HRS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss})	(.5 I_{dss})	MAG (dB)
						g_m (mS)	g_m (mS)	
0	46.9	-1.73	7.48	5.72	495	42.0	36.3	10.2
1000	433.0	-1.35	7.46	6.60	389	36.1	24.9	7.8

TABLE 6.4 Average percentage change in dc parameter data for 7 recessed-gate MESFETs stored at 280°C for 1000 hours.

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{g_m}$	$(.5 I_{dss})_{g_m}$
-37.6	-36.0	-.3	+15.4	-21.4	-14.0	-25.6

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -3.2 dB

6.3 Realigned Self-Aligned Gate (RSAG) MESFET 1000 Hour Life Test

Realigned self-aligned gate MESFETs were subjected to a 1000 hour storage test at 243, 261.5, and 280°C and characterized on 6 hour intervals. The data obtained from the dc characterizations at 243°C is summarized in Table 6.5. Table 6.6 lists the average percentage changes in these same parameters after 1000 hours. No failures occurred at this temperature according to the 20% change in I_{dss} failure criterion. The average I_{dss} decreased 1.7%, R_0 decreased 1.7%, and R_s increased 4.0%, V_p increased (became less negative) 1.2%. The cumulative effects of the changes in the dc parameters on MAG is - .4 dB, a considerable improvement over recessed gate performance.

TABLE 6.5 Average dc parameter data for 8 RSAG MESFETs
stored at 243°C for 1000 hours.

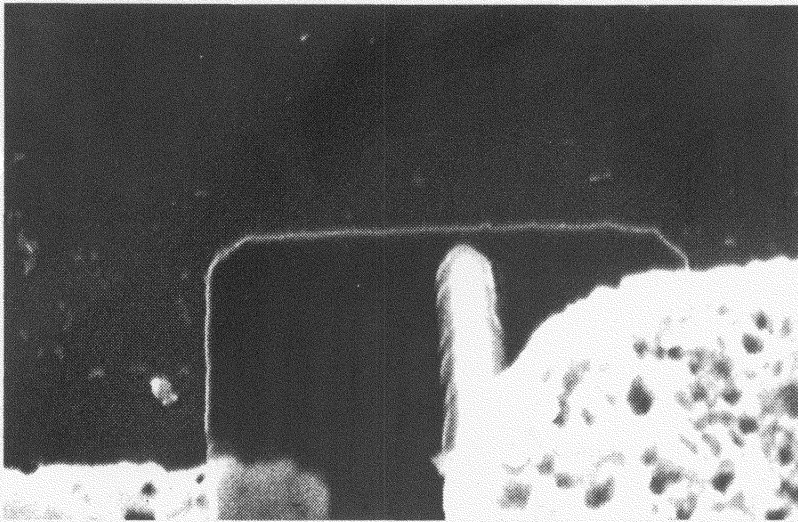
HRS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	$(.5 I_{dss})$ g_m (mS)	MAG (dB)
0	43.4	-1.75	5.48	2.60	772	36.8	33.1	13.5
1000	42.7	-1.73	5.96	2.63	759	35.6	32.4	13.1

TABLE 6.6 Average percentage change in dc parameter data for
8 RSAG MESFETs stored at 243°C for 1000 hours.

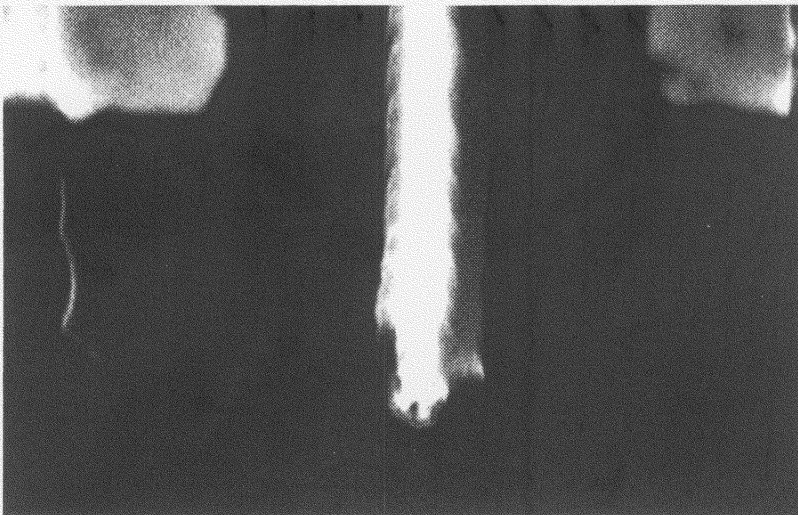
I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{g_m}$	$(.5 I_{dss})_{g_m}$
-1.7	+1.2	+5.8	+4.0	-1.7	-3.3	-2.1

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -.4 dB

The data obtained from the dc characterizations at 261.5°C is summarized in Table 6.7. Table 6.8 lists the average percentage changes in these same parameters after 1000 hours. No failures occurred at this temperature according to the 20% change in I_{DSS} failure criterion, however, an interesting phenomena was observed with this sample. Of the 8 devices in the sample, two distinct groups of 4 devices were noted. The first group exhibited an average decrease in I_{DSS} of approximately 5.3%, a small reduction in R_0 of 2.8%, and a small increase in R_S of 3.5%. R_g increased 5% and g_m at half I_{DSS} decreased in I_{DSS} , a 29% decrease in R_0 , and an 11.8% increase in R_S . V_p increased (became less negative) 5%, R_g increased 3.3% and g_m at half I_{DSS} decreased 6.1%. Figure 6.5 contains SEM photographs of the gate regions of typical devices from these two groups. The TiPdAu realignment was done successfully on the devices in the first group as shown in the top photograph. The second group of devices, however, were misaligned as shown in the bottom photograph. The cumulative effects of the dc parameters on MAG of -.06 dB for the properly processed devices is significantly better than recessed gate performance. The misaligned devices with MAG reductions averaging 1.9 dB perform no better than the recessed gate devices. It is suspected that the misaligned devices were selected from the outer edges of the wafer and the misalignment was due to runout.

ALIGNED

9331-007

MISALIGNED

9331-008

Figure 6.5 SEM photographs of aligned and misaligned RSAG device gate regions.

TABLE 6.7 Average dc parameter data for 8 RSAG MESFETs
stored at 261.°C for 1000 hours.

TOTAL (QUANTITY 8)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	44.3	-1.85	5.54	2.82	670	33.9	30.3	12.4

ALIGNED (QUANTITY 4)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	44.57	-1.98	5.57	2.76	619	32.7	28.8	11.9
1000	42.17	-1.98	5.85	2.85	602	31.9	27.6	11.3

MISALIGNED (QUANTITY 4)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	43.85	-1.78	5.51	2.88	721	35.1	31.6	12.9
1000	36.92	-1.69	5.69	3.22	512	32.1	29.7	11.0

TABLE 6.8 Average percentage change in dc parameter data
for 8 RSAG MESFETs stored at 261.5°C for 1000
hours.

ALIGNED (QUANTITY 4)

I_{dss}	V_p	R_g	R_s	R_o	$\left(\frac{I_{dss}}{g_m}\right)$	$\left(\frac{.5 I_{dss}}{g_m}\right)$
-5.3	0.0	+5.0	+3.2	-2.8	-4.2	-3.9

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -.6 dB

MISALIGNED (QUANTITY 4)

I_{dss}	V_p	R_g	R_s	R_o	$\left(\frac{I_{dss}}{g_m}\right)$	$\left(\frac{.5 I_{dss}}{g_m}\right)$
-15.8	+5.0	+3.3	+11.8	-29.0	-8.4	-6.1

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -1.9 dB

The data obtained from the dc characterization at 280°C is summarized in Table 6.9. Table 6.10 lists the average percentage changes in these same parameters after 1000 hours. No failures occurred at this temperature according to the 20% change in I_{DSS} failure criterion. Once again, the RSAG devices were readily separated into 2 distinct groups based upon alignment accuracy. The properly aligned parts exhibited 5.3% average reductions in I_{DSS} , 6.1% reductions in R_0 , and 7.3% average increases in R_S . R_G increased 8.4% and g_m at half I_{DSS} decreased 5%. The misaligned devices were substantially degraded with I_{DSS} decreasing an average of 19%, R_0 decreasing 37%, and R_S increasing 13.6%. V_p increased (became less negative) 5.8%, R_G increased 7.5%, and g_m at half I_{DSS} decreased 6.8%. The properly aligned devices' variations in dc parameters resulted in a change in MAG of -88 dB; excellent when compared with -3.2 dB recessed gate performance. The misaligned parts degraded 2.25 dB which, although better than recessed gate performance, were significantly less reliable than the properly aligned devices.

TABLE 6.9 Average dc parameter data for 5 RSAG MESFETs
stored at 280°C for 1000 hours.

TOTAL (QUANTITY 5)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	43.0	-1.82	5.0	2.56	664	33.82	29.98	12.7

ALIGNED (QUANTITY 2)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	44.2	-1.98	5.09	2.33	588	32.0	27.9	12.0
1000	41.9	-1.98	5.52	2.50	552	30.4	26.5	11.1

MISALIGNED (QUANTITY 3)

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	(.5 I_{dss}) g_m (mS)	MAG (dB)
0	42.23	-1.73	4.94	2.71	715	35.0	31.3	13.2
1000	34.2	-1.63	5.31	3.08	447	31.9	29.2	11.0

TABLE 6.10 Average percentage change in dc parameter data
for 5 RSAG MESFETs stored at 280°C for 1000
hours.

ALIGNED (QUANTITY 2)

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{9m}$	$(.5 I_{dss})_{9m}$
-5.3	0.0	+8.4	+7.3	-6.1	-5.0	-5.0

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -.88 dB

MISALIGNED (QUANTITY 3)

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{9m}$	$(.5 I_{dss})_{9m}$
-19.0	+5.8	+7.5	+13.6	-37.0	-8.8	-6.8

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -2.25 dB

6.4 Planarized Self-Aligned Gate (PSAG) MESFET 1000 Hour Life Test

Planarized self-aligned gate MESFETs were subjected to a 1000 hour storage test at 261.5 and 280°C and characterized on 6 hour intervals. The data obtained from the dc characterizations at 261.5°C is summarized in Table 6.11. Table 6.12 lists the average percentage changes in these same parameters after 1000 hours. No failures occurred at this temperature according to the 20% change in I_{DSS} failure criterion. The PSAG MESFETs are significantly better than both the recessed gate and the realigned self-aligned gate (RSAG) devices. Average I_{DSS} decreased 4%, R_0 increased 8.6%, and R_S increased 6.7%. V_p increased (became less negative) 2%, R_g increased 5.9%, and g_m at half I_{DSS} decreased 2.8%. It is notable that unlike the RSAG devices, R_0 increased with time, which tends to boost gain and improve performance. The effective reduction in MAG of .3 dB is excellent performance.

TABLE 6.11 Average dc parameter data for 7 PSAG MESFET
stored at 261.5°C for 1000 hours.

HRS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	g_m (mS)	(I_{dss}) g_m (mS)	$(.5 I_{dss})$ MAG (dB)
0	37.5	-1.57	5.07	2.22	896	38.4	32.1	14.7
1000	36.0	-1.54	5.37	2.37	973	37.2	31.2	14.4

TABLE 6.12 Average percentage change in dc parameter data
for 7 PSAG MESFETs stored at 261.5°C for 1000
hours.

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{g_m}$	$(.5 I_{dss})_{g_m}$
-4.0	+2.0	+5.9	+6.7	+8.6	-3.1	-2.8

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -.3 dB

The data obtained from the dc characterizations at 280°C is summarized in Table 6.13. Table 6.14 lists the average percentage changes in these same parameters after 1000 hours. No failures occurred at this temperature according to the 20% change in I_{DSS} failure criterion. The average I_{DSS} decreased 5.5%, the R_0 increased 9.4%, and R_S increased 7.2%. V_p increased (became less negative) 3.2%, R_g increased 6.4%, and g_m at half I_{DSS} decreased 3.1%. The PSAG devices exhibit excellent reliability performance with only a .7 dB degradation in MAG after 1000 hours of 280°C storage. This represents a .18 and 2.5 dB improvement over RSAG and recessed-gate devices.

TABLE 6.13 Average dc parameter data for 19 PSAG MESFETs
stored at 280°C for 1000 hours.

HOURS	I_{dss} (mA)	V_p (V)	R_g (Ω)	R_s (Ω)	R_o (Ω)	(I_{dss}) g_m (mS)	$(.5 I_{dss})$ g_m (mS)	MAG (dB)
0	36.0	-1.60	5.35	2.35	724	36.2	29.4	13.1
1000	34.0	-1.55	5.69	2.52	792	34.9	28.5	12.4

TABLE 6.14 Average percentage change in dc parameter data for 18 PSAG MESFETs stored at 280°C for 1000 hours.

I_{dss}	V_p	R_g	R_s	R_o	$(I_{dss})_{g_m}$	$(.5 I_{dss})_{g_m}$
-5.5	+3.2	+6.4	+7.2	+9.4	-3.6	-3.1

CUMULATIVE MAXIMUM AVAILABLE GAIN EFFECT -.7 dB

CHAPTER VII

DISCUSSION

Table 7.1 presents a comparison of the changes in dc parameters of recessed-gate and self-aligned gate MESFETs after high temperature storage for 1000 hours. The RSAG (A) column represents the properly processed RSAG devices, and the RSAG (M) column presents the data for misaligned RSAG devices. At this time it is important to note that SEM examination of the misaligned RSAG devices indicate the .5 micron TiPdAu realigned gate favors the drain side. This is a key point in understanding the high temperature performance of these devices. The discussion section of this paper will focus on the differences in reliability performance of the recessed-gate and self-aligned gate devices and how they relate to the variations in device structure.

TABLE 7.1 DC parameter stability for recessed-gate and self-aligned gate devices after high temperature storage for 1000 hours.

		PERCENTAGE CHANGES			
Temperature		Recessed Gate	RSAG (A)	RSAG (M)	PSAG
I_{dss}	261.5	-28.2	-5.3	-15.8	-4.0
	280.0	-37.6	-5.3	-19.0	-5.5
V_p	261.5	-24.2	0.0	+5.0	+2.0
	280.0	-36.0	0.0	+5.8	+3.2
R_g	261.5	+2.0	+5.0	+3.3	+5.9
	280.0	-0.3	+8.4	+7.5	+6.4
R_s	261.5	+8.4	+3.2	+11.8	+6.7
	280.0	+15.4	+7.3	+13.6	+7.2
R_o	261.5	-30.0	-2.8	-29.0	+8.6
	280.0	-21.4	-6.1	-37.0	+9.4
$g_m @ I_{dss}$	261.5	-7.0	-4.2	-8.4	-3.1
	280.0	-13.4	-5.0	-8.8	-3.6
$g_m @ .5 \times I_{dss}$	261.5	-14.0	-3.9	-6.1	-2.8
	280.0	-25.6	-5.0	-6.8	-3.1

TABLE 7.2 Cumulative effects of changes in dc parameters on MAG (Maximum Available Gain) for recessed-gate and self-aligned gate devices after 1000 hours of high temperature storage.

Temperature	Recessed Gate	RSAG (A)	RSAG (M)	PSAG
261.5	-1.8 dB	-0.6 dB	-1.9 dB	-0.3 dB
280.0	-3.2 dB	-.88 dB	-2.25 dB	-0.7 dB

7.1 Reliability Comparison Based Upon DC Parameter Change

7.1.1 Changes in I_{dss}

The degradation in I_{dss} seen in the recessed-gate devices is mainly attributed to gate metal interdiffusion with GaAs resulting in a movement of the gate Schottky into the channel which reduces the effective channel thickness. Channel resistance increases and I_{dss} degrades accordingly. The recessed-gate I_{dss} degradation of 28.2 and 37.6% at 261.5°C respectively is conservative for the following reason: eutectic die attach requires exposure to temperatures in excess of 325°C for a few minutes. The exponential decay of I_{dss} at those temperatures is substantial. Therefore, the initial I_{dss} measured in the life test is already substantially degraded from the unpackaged device I_{dss} and degradation will proceed at a reduced rate. The properly processed RSAG and PSAG devices exhibit only a slight degradation in I_{dss} in the vicinity of 5.3%. The improved diffusion barrier provided by the $TiWN_x$ Schottky is responsible for the reliability improvement. The misaligned RSAG devices exhibit I_{dss} degradations of 15.8 and 19.0% at 261.5 and 280°C respectively. If 5.3% (seen in properly aligned RSAG devices) is attributable to the $TiWN_x$ diffusion barrier performance, 10.5 and 13.7% relate to the misaligned $TiPdAu$. These values are approximately one third of the recessed-gate values.

7.1.2 Changes in V_p

The degradation in pinch-off voltage of 24.2 and 36% at 261.5 and 280°C respectively for recessed-gate devices is also attributable to gate metal diffusion. The change scales directly with the change in I_{dss} . The properly aligned RSAG and PSAG devices show only minimal degradation. Although the RSAG devices show a slight improvement over the PSAG devices, the difference is less than 50 mV which is the resolution of the test power supply. The misaligned RSAG devices with 5.0 and 5.8% changes in V_p at 261.5 and 280°C respectively show less degradation than the recessed-gate devices. The change does not scale directly with the change in I_{dss} because the misaligned TiPdAu forms only a small part of the total gate length. An examination of the average pinch-off voltages of the RSAG devices reveals consistently lower (in absolute value) pinch-off voltages in the misaligned devices. They have a $TiWN_x$ and TiPdAu Schottky side by side, but the properly aligned devices have only a $TiWN_x$ Schottky. Typical barrier voltages for these Schottky metallizations are .66 volts (TiPdAu) and .74 volts ($TiWN_x$). Because the Schottky characteristic is a linear function of area and an exponential function of barrier voltage, the TiPdAu will tend to dominate in the misaligned devices. The measured V_p is actually the sum of the intrinsic pinch-off voltage and the Schottky barrier voltage. The lower barrier voltage of the misaligned RSAG devices is at least partially responsible for the lower measured V_p . It is likely that the remaining difference is

due to some Au diffusion occurring during eutectic die attach at 340°C which is indicated by a slightly lower average I_{dss} .

7.1.3 Changes in R_g

The recessed gate MESFETs showed little or no degradation in R_g after 1000 hours. The properly aligned RSAG devices exhibit 5.0 and 8.4% increases in R_g at 261.5 and 280°C after 1000 hours. Because of the way in which the R_g measurement is made (forcing current into the Schottky until the linear resistance region is established, measuring the "on" resistance, and subtracting R_s), the 200 nanometers thick $TiWN_x$ Schottky layer (high resistance) dominates for properly aligned gates. Here in forward conduction the $TiPdAu$ (low resistance layer) and the $TiWN_x$ (high resistance Schottky layer) are in series. In actual operation, the Schottky is reverse biased and the resistances of the $TiPdAu$ and $TiWN_x$ are in parallel and the $TiPdAu$ dominates. It is suspected, although not fully understood, that the increases noted in R_g for the RSAG and PSAG devices is due to some intermetallic formation or oxidation at the $TiPdAu/TiWN_x$ interface because this change was not noted in recessed-gate devices with $TiPdAu$ Schottky gates. In the forward conduction mode, any misalignment in the RSAG devices places a thin $TiPdAu$ layer in parallel with the series combination of $TiWN_x$ and $TiPdAu$ resulting in a slight (3%) reduction in the average value of R_g . Because of the dependance of a Schottky characteristic upon area in linear fashion and upon barrier voltage in an

exponential fashion, the TiPdAu Schottky will tend to dominate in the forward conduction. The tendency for conduction in the TiPdAu slightly reduces the effects of the diffusion at the TiPdAu/TiWN_x interface, suspected of causing the increases in R_g . This is reflected in the 3.3% vs 7.5% changes in R_g for 261.5 and 280°C respectively. The PSAG devices are essentially identical to the good RSAG devices with 5.9 and 6.4% changes in R_g after 1000 hours at 261.5 and 280°C respectively.

7.1.4 Changes in R_s

The recessed-gate MESFETs exhibited 8.4 and 15.4% increases in R_s at 261.5 and 280°C respectively after 1000 hours. Because R_s is derived by injecting current into the gate of the MESFET and measuring the resulting drain voltage with the drain open circuited, it is composed of the source contact resistance, the resistance of the N⁺ region under the ohmic contacts, and a small portion of the N region of the channel under the gate. The thinning of the channel caused by the effective movement of the Schottky interface downward results in an increase in the N channel region's contribution to R_s . The properly aligned RSAG devices exhibited 3.2% and 7.3% increases in R_s after 1000 hours of high temperature storage at 261.5 and 280°C respectively. The PSAG devices degraded 6.7 and 7.2% at these temperatures. Although the RSAG devices appears to be more stable than the PSAG devices at 261.5°C, it is notable that the average R_s values are 2.76 vs 2.22 respectively. Most of the percentage difference lies in

the difference in the base values from which the percentage changes are calculated. The actual changes differ by only .06 ohms, and the two device types are essentially equivalent. The misaligned RSAG devices show considerably more degradation in R_S (11.8 and 13.6% at 261.5 and 280°C respectively) than the good RSAG devices. With the high conduction TiPdAu misaligned to the drain side of the $TiWN_x$ Schottky, the effective Schottky position shifts accordingly causing an increase in the average R_S . Gate metal diffusion from the TiPdAu overlay at high temperature causes a significant increase in the N channel region resistance which contributes to the measured R_S .

7.1.5 Changes in R_0

Large decreases in R_0 (30 and 21.4% at 261.5 and 280°C respectively) were noted for recessed-gate devices in this study. Similarly, the misaligned RSAG devices showed extensive degradation (29 and 37% at 261.5 and 280°C respectively). The RSAG devices with proper gate overlay alignment showed only slight decreases in R_0 (2.8 and 6.1% at 261.5 and 280°C respectively). A review of the literature reveals that care must be taken when the R_0 parameter is the topic of discussion. There are a minimum of 2 different meanings for the term R_0 including output resistance as measured in this study, and open channel resistance as discussed in many papers focused upon power devices. The term open channel resistance refers to the minimum channel resistance possible

for the FET equal to the minimum "on resistance" from drain to source with R_S and R_D subtracted out. This condition is achieved by placing a positive voltage on the gate with the source grounded. At high drain current levels this becomes an important parameter. With the obvious increase in the channel resistance seen throughout this study as indicated by the decrease in I_{DSS} , one would have expected the measured output resistance, R_O , value to increase as is seen in the PSAG devices (8.6 and 9.4% at the two temperatures). R_O is essentially the change in drain current divided into the associated change in drain voltage with a fixed gate bias. A decrease in R_O in the presence of an increase in channel resistance can most readily be explained by a leakage path from source to drain. Although gate to drain and gate to source leakage data was not presented in this paper, it was extracted by the test system. An order of magnitude difference exists between the leakage noted in the self-aligned and recessed-gate devices (the self-aligned gate devices showed much lower leakages). The magnitudes of these leakages was not sufficient to cause concern for the R_O measurement. In power devices where input signal amplitude is large, the MESFET will operate in or near the linear part of the I_D vs V_D characteristic as the output swings on the ac load line. In this mode of operation R_O (open channel resistance) may be on the order of less than 10 ohms. Because the devices under test are low-noise/small signal MESFETs, R_O (output resistance) was derived in the saturated drain region where it is large.

It is quite possible that if it had been measured at a different operating point, the expected trend would have been noted. The leakage current in the recessed-gate devices did not increase monotonically with time. The trend followed was an increase in leakage current for approximately 500 hours, followed by a decline. R_0 , whose calculated value is influenced by a leakage current of sufficient magnitude, followed a trend which was the inversion of that noted above. This accounts for the lower apparent degradation in R_0 at 280°C, because the R_0 value reached its minimum value sooner at the higher temperature and therefore recovered more.

7.1.6 Changes in g_m

Depletion mode MESFETs generally show slight reductions in g_m as the operating point moves from I_{DSS} toward $.5 \times I_{DSS}$. From $.5 \times I_{DSS}$ toward pinch-off, the g_m reduction is more dramatic. Any reduction in I_{DSS} will result in a corresponding drop in g_m at all bias levels. This is precisely what occurred in all of the devices in the experiment. The more dramatic the I_{DSS} degradation, the more dramatic the changes in g_m . The recessed-gate, misaligned RSAG, aligned RSAG, and PSAG devices degraded accordingly.

7.2 Failure Criteria

Utilizing a 20% change in I_{DSS} or any percentage change in any measured parameter as a failure criterion is a valid and useful practice when a particular parameter's variation, degradation, or failure mechanism is the topic of study. An

excellent example of this would be a study of the diffusion barrier performance of different gate metallization schemes and structures. The use of a percentage change in a parameter as a failure criterion to predict the median life or mean time to failure of a component has questionable value in most instances, especially in semiconductors. This became obvious in many ways during this study.

The overall performance of a microwave amplifier or any electronic component and its ability to perform a given function within a system is the result of a complex interaction of many parameters. Determination of a device failure based upon changes in one parameter ignores the possibilities that:

- 1) another parameter change might offset its effects.
- 2) another parameter change might cause the device performance to drop below the acceptable limit long before the parameter under scrutiny changes and triggers an apparent failure. Although degradation in a second parameter often is accompanied by a change in the parameter under scrutiny, this is not always the case.
- 3) a combination of small parameter changes in a number of parameters can readily cause a device malfunction.

Excellent examples of all three of these instances occurred during this study.

Offsetting parameter changes occurred in the case of the planarized self-aligned gate devices. The effects of

increasing R_g and R_s were somewhat nullified by the increase in R_0 in the calculation of MAG (Maximum Available Gain).

Changes in overall device performance which would cause a failure in a system application, but would have gone unnoticed in a study focussed on a single parameter occurred in the RSAG device sample. In the derivation of R_g and R_s a particular minimum current density was sought so that the proper current could be forced into the gate of the MESFET to place it in a certain region of operation. The current required to produce that current density was derived in the measurement subroutine from the device's gate periphery ($L \times W$). The nominal Schottky dimensions for all of the devices in this study were 1×300 microns. The realigned gate devices, however, have a $.5 \times 300$ micron TiPdAu layer (low resistance) "centered" on a 1×300 micron $TiWN_x$ (high resistance) Schottky. These devices received twice the current density of the rest of the sample during the R_g and R_s measurements. This resulted in electromigration failure of the TiPdAu stripe in numerous devices. Because these failures were "tester induced", they were removed from the test sample. The point of interest is that although the TiPdAu was open, I_{dss} and V_p were unchanged because of the presence of the $TiWN_x$ Schottky which maintained excellent gate control. The gate resistance R_g doubled and the MAG dropped by approximately 1 dB at the time of failure.

An excellent example of a number of small changes adding up to a device failure was found in the study of the PSAG

devices. These devices exhibited a .7 dB drop in gain after storage for 1000 hours at 280°C. This drop is not attributable to any single parameter change, but to a slight degradation in all of the measured parameters. This part would fail in a system requiring a gain flatness of .5 dB.

In summary, all of the pertinent lumped-element parameters must be monitored and their overall effects on system performance parameters calculated if proper life predictions are to be made based upon accelerated life data. If all of the lumped-element parameters cannot be monitored individually, then all of the performance parameters required by the system application must be measured to determine device failure. Once the life prediction is complete, experiments must be devised to determine the lumped element interactions and contributions to device failure. In accordance with this philosophy, the author must recognize the need for the determination of the variation in C_{gs} and C_{gd} under high temperature storage conditions identical to the ones imposed upon the devices in this test. Only then can the performance comparison be complete.

CHAPTER VIII

SUMMARY AND CONCLUSIONS

The main objectives of this research were: to design an accelerated life test facility capable of performing large scale reliability testing of GaAs devices at temperatures as high as 300°C; to design inexpensive and easily renewable fixturing to withstand these temperatures for extended periods of time; to perform a small scale life test comparison of recessed-gate MESFETs and two analog derivatives of a self-aligned gate digital MESFET; to study the changes in their dc parameters and their effects on MAG after a 1000 hour storage test, and the the subsequent implications for selecting failure criteria for accelerated life testing of GaAs MESFETs. The important observations of this study were:

- 1) The life test facility and low cost fixturing were designed and built. With the exception of a few anomalies which one would expect to find on a test set of this magnitude in its first design iteration, they performed well. Improvements already underway include the improvement of the test power supplies' resolution to 1 mV and the implementation of current source capability.
- 2) The planarized MESFETs studied in this research exhibit excellent reliability approaching state-of-the-art performance. Because it shares its processing technique with digital devices, it opens up the

possibility of integrating digital and analog functions on the same chip. This has not been done by any company to the author's knowledge. The increased performance, improved uniformity, and inherent manufacturability of these devices will strongly influence the future of GaAs.

The realigned self-aligned gate (RSAG) devices exhibit performance essentially equivalent to the PSAG devices if the critical realignment process is carried out to perfection. This research revealed that the process is by no means manufacturable as a high percentage of the devices tested from the same wafer showed misalignment. The misalignment is essentially undetectable electrically, and therefore their reliability can only be assured by life testing before shipment.

The recessed-gate devices which presently dominate the industry have numerous problems which make them difficult to manufacture. Most of the device parameters are determined by the gate recess etch which is difficult to control. The result is poor uniformity and mediocre performance. If an Au based metallization is utilized, diffusion will most likely occur at high temperature and reliability will suffer accordingly. Typical activation energies for this failure mechanism fall in the

0.8 to 1.8 eV range. Eutectic die attach temperatures often cause significant device degradation which can result in erroneous life predictions and poor electrical performance.

- 3) The use of percentage changes in a device parameter as a failure criterion is apt to cause numerous problems in predicting median lives for semiconductor devices. The use of a parameter such as MAG which takes into account all of the parameter interactions is a more useful and accurate technique. A single parameter change is useful for the study of a particular failure mechanism for the determination of an activation energy.

CHAPTER IX

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