A Novel Auxiliary Resonant Snubber Inverter Using Wide Bandgap Devices

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Abstract

In the application of power inverters, power density has become a key design specification where it has stringent requirements on system size and weight. Achieving high power density need to combine lasted wide bandgap (WBG) device technology and high switching frequency to reduce passive filter size thus further shrink overall space. While still maintaining decent power conversion efficiency and low electromagnetic interference (EMI) with higher switching frequency, soft-switching needs to be implemented.

A novel auxiliary resonant snubber is introduced. The design and operation are carried out, in which this snubber circuitry enables main Gallium Nitride (GaN) switches operating under zero voltage switching (ZVS) condition, and auxiliary Silicon Carbide (SiC) diodes switching under zero current switching (ZCS) condition. Besides, the auxiliary snubber circuitry gating algorithm is also optimized which allows reduction of the switching and conduction loss in auxiliary GaN switches to obtain higher system efficiency and better thermal performance. Here, this novel auxiliary resonant snubber circuitry is applied to a traditional full bridge inverter with flexible modulation suitability. This proposed inverter can be applied to a wide range of potential applications, such as string solar inverter, renewable energy combined distributed generation, dc-ac part of bi-directional electrical vehicle (EV) on-board charger, and uninterruptible power supply (UPS), etc.

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General Audience Abstract

This thesis combined an innovated resonant snubber circuit to resonate with traditional robust inverter topology with latest semiconductor devices implemented to achieve a high efficiency, high performance, low profile inverter system.

During the design procedure, control algorithm had been optimized, novel semiconductor devices were utilized, and comprehensive operation analyses were delivered. Finally an efficient and robust system was constructed and achieved the design goals.

With the reduction of non-renewable energy consumptions, the research work of this thesis carried out a novel inverter topology which can become a prominent candidate for tremendous applications such as solar panel, electrical vehicle charging, and other renewable energy sources.

Acknowledgements

Firstly, I would like to express my deepest appreciation to my advisor, Dr. Jih-Sheng Lai. Dr. Lai has been instrumental mentoring me since I joined the Future Energy Electronics Center (FEEC) and offering me tremendous opportunities to develop myself as an electrical engineer in Power Electronics. With his guidance, I learned the experience and knowledge which can't be found in any class. Also, I would like to thank my committee members, Dr. De La Ree and Dr. Li for being two of the best professors I have ever met in Virginia Tech and providing me precious support and suggestions.

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Finally, I would like to thank my parents for their unconditional encouragement and support throughout my whole life and I can never express my love and appreciation enough to them.

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1 Introduction

In this section, the outline of several considerations in selecting the novel auxiliary resonant snubber circuit is presented; next, inverter topology to verify the superiority of auxiliary resonant snubber is selected; then, the detailed working and control of one solution is introduced: a full-bridge inverter operating in bipolar modulation to combine with proposed auxiliary resonant snubber for soft-switching.

1.1 Novel Auxiliary Resonant Snubber for Soft-Switching

For reducing filter size to obtain higher power density and better dynamic performance, one promising option is to increase the switching frequency, meanwhile, minimizing switching loss to maintain decent power conversion efficiency and low harmonic, soft-switching is the way to go, which includes zero voltage switching (ZVS) and zero current switching (ZCS)[1].

There are generally two main categories to achieve soft-switching, one is passive soft-switching method, the other is active soft-switching method. Although passive soft-switching methods do not require an extra switch or any additional control circuitry, such as Figure 1.1 which is proposed in [2], it claims to be lossless however the passive method could only reduce di/dt and dv/dt but not achieve true ZVS turn-off due to non-effective dv/dt reduction. Other passive soft-switching methods are also proposed in [2]-[5].

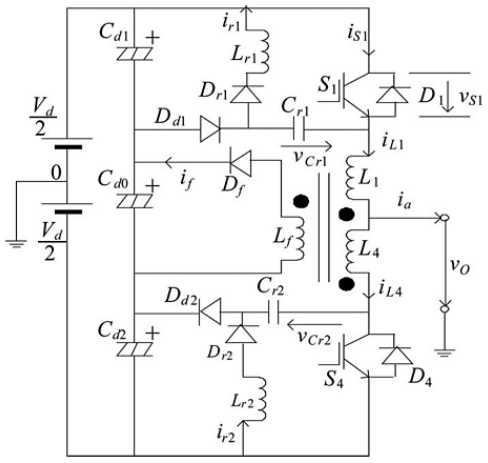


Figure 1.1. Snubber Circuitry Using Only Passive Components.

Compared to passive soft-switching method, the active soft-switching method can achieve true ZCS and ZVS through full-load condition thus it is more promising and applicable. The comparison of passive and active soft-switching method is summarized in Table 1.1.

Table 1.1. Comparison between Passive and Active Soft-switching Method.

	Passive Soft-Switching Method	Active Soft-Switching Method
Pro	1. Better price/performance ratio. 2. No active switch and control circuitry are required.	1. Good for full load range with high switching frequency. 2. Achieve true ZCS and ZVS rather than reduce di/dt and dv/dt. 3. Easier to implement.
Con	1. Lossy by dissipating the recovered switching energy. 2. Less performance in light load condition. 3. Hard to reduce both di/dt and dv/dt effectively. 4. Large components number increase the implementation complexity.	1. Most require for auxiliary switches. 2. Additional control circuitry required.

In this thesis, from the comparison and discussion above, active soft-switching method is preferred in this prototype.

Under active soft-switching category, during past several decades, a variety of active soft-switching methods has been brought out [1]. They can be divided into different categories as shown in Figure 1.2.

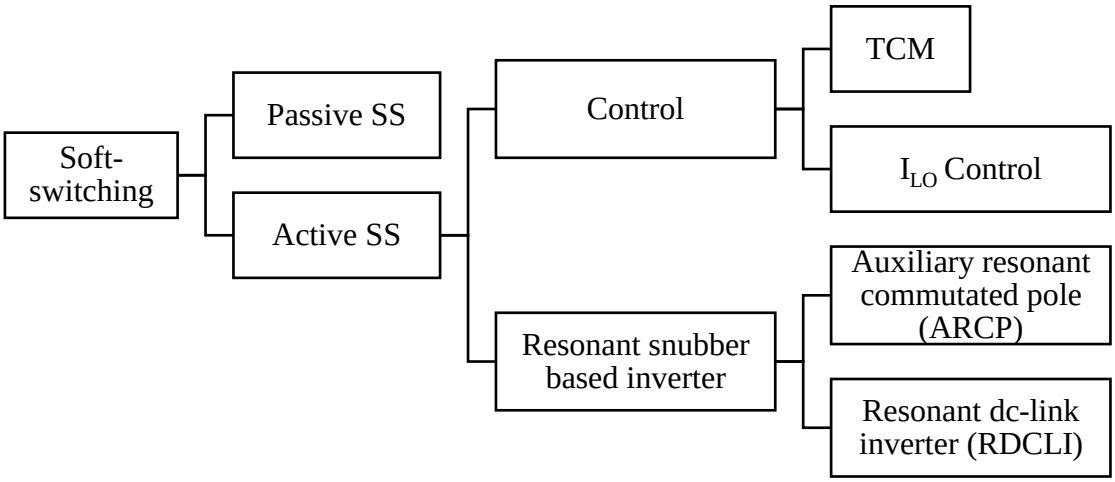


Figure 1.2. Different Methods under Active Soft-switching Category.

Under active soft-switching method, there are two main categories as well, which are control method and resonant snubber based inverter. For control method, such as triangular current mode (TCM) or output inductor current control (I_{LO} control), as proposed in [1] and [3]. These methods all require exactly precise control algorithm to achieve ZVS through controlling inductor current conducting bi-directionally in every switching cycle. This bi-directional output inductor current increases the rms current value thus leads to a larger conduction loss. The comparison of these two categories mentioned above in shown in Table 1.2.

Table 1.2. Comparison between Control and Resonant Snubber Method.

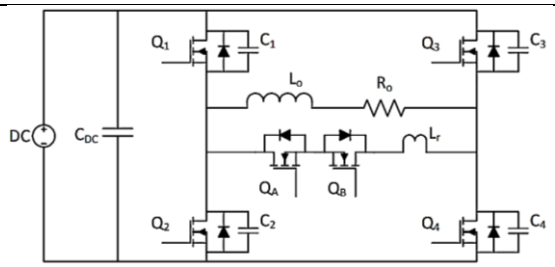
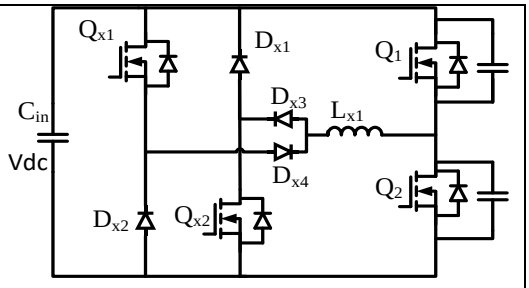
	Control	Resonant Snubber Based Inverter

Pro	1. Less auxiliary components 2. Smaller output inductor 3. Better for low power applications	1. Broadly used in single and three phase VSI 2. Simple aux switch control 3. High reliability
Con	1. Complex to implement 2. Stringent requirements for controller at high frequencies 3. Increase output current ripple 4. Require bigger harmonic filters	1. Extra components 2. Additional loss and space

From the comparison above, resonant snubber based inverter is preferred in this thesis.

Finally, under the category of resonant snubber, another comparison between different topologies is made in [4]-[10], which is shown in Table 1.3.

Table 1.3. Comparison between Different Auxiliary Resonant Snubber.

	 Figure 1.3. Normal Resonant Snubber Based Inverter.	 Figure 1.4. Novel Resonant Snubber Circuitry.
Pro	1. Less auxiliary component counts(two for full-bridge) 2. Simple auxiliary control	1. Smaller auxiliary passive components 2. Both unipolar and bipolar modulation can be implemented
Con	1. Only bipolar modulation 2. High voltage SiC Schottky diode needed	1. More aux switches(four for half-bridge)

For the sake of more comparison of soft-switching performance under different modulation to have better understanding of the topology, the novel resonant snubber [11] is selected in this thesis to achieve soft-switching, which is shown in Figure 1.4.

1.2 **Inverter Topology Selection**

This section will give an overview of the existing dc-ac pulse-width-modulation (PWM) inverters that are compatible to verify the novel soft-switching topology mentioned in section 1.1. Meanwhile the whole inverter system is design to focus on high power density, high efficiency, and easier EMI filter design.

The most commonly used single-phase voltage source inverter (VSI) is H-bridge inverters with a lot variations [12]. The basic VSI with minimum number of active switch is full-bridge inverter as shown in Figure 1.5.

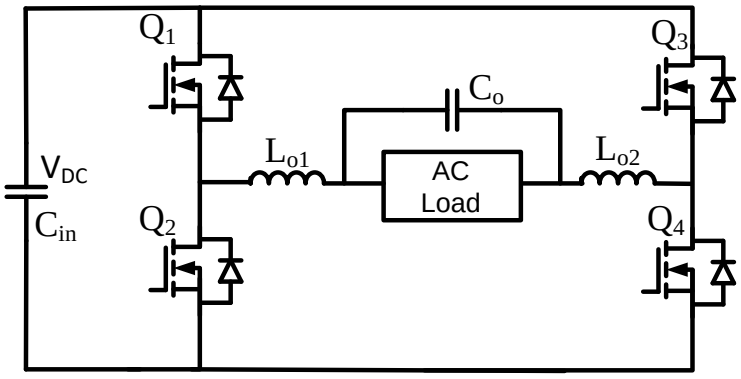


Figure 1.5. Full-Bridge VSI.

The physical configuration of full-bridge VSI is two switches per leg with total count of four semiconductor devices (Q_1-Q_4) which can conduct current in reverse direction. The low-pass LC filter at output consists of inductors (L_{o1} and L_{o2}) and capacitor (C_o) is used to reduce the high frequency harmonics generated by semiconductor devices.

Some advantages of full-bridge VSI including: a) structure simplicity, b) Flexible modulation implementation. For different modulation suitability, bipolar modulation switching operation and gating configuration are shown below in Figure 1.6, Figure 1.7. Unipolar operation and gating configuration are shown in Figure 1.8, Figure 1.9.

In this thesis, traditional full-bridge topology is selected for proposed inverter system.

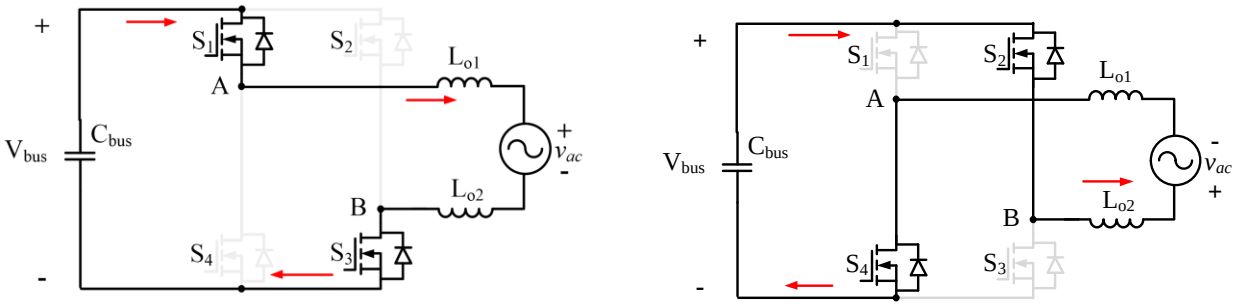


Figure 1.6. Traditional Full-bridge Inverter Bipolar Modulation.

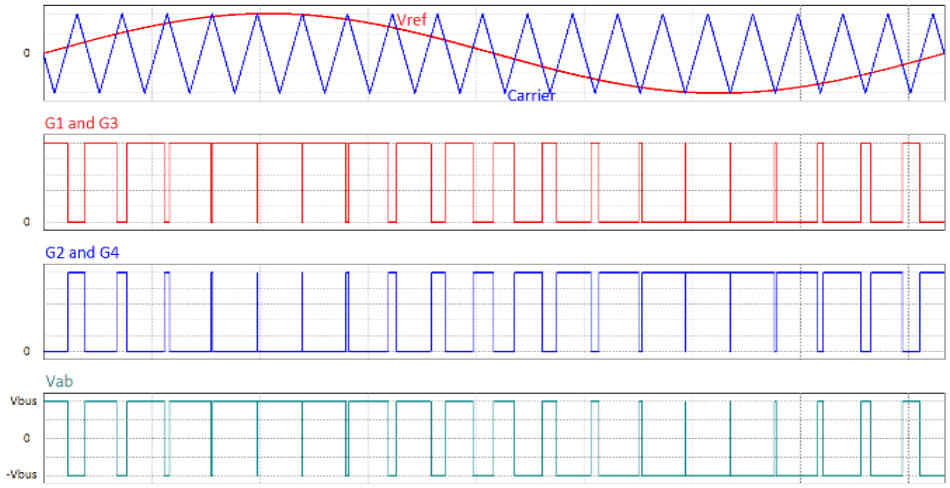


Figure 1.7. Bipolar Gating Configuration.

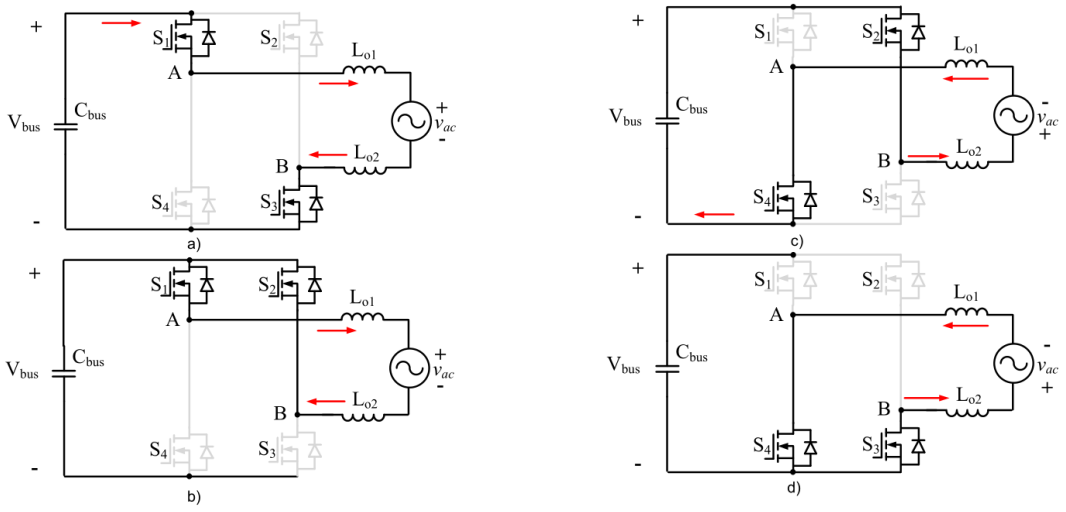


Figure 1.8. Traditional Full-bridge Inverter Unipolar Modulation.

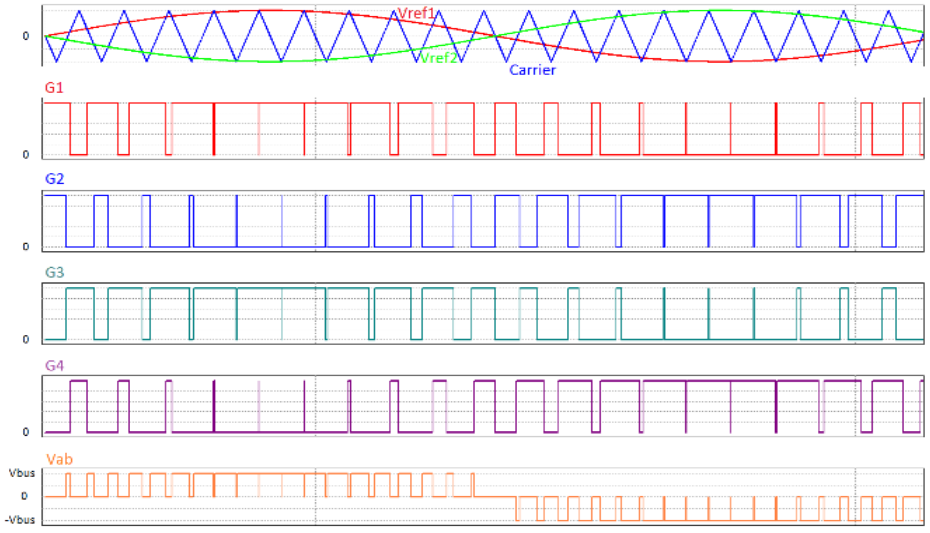


Figure 1.9. Unipolar Gating Configuration.

1.2.1 Achieving High Power Density

Idea for achieving high power density is employed from previous Future Energy Electronics Center (FEEC) projects, which is Google Little Box Challenge (LBC). Google's Little Box Challenge [13] launched in July 2014, brought power density into the global spotlight by rewarding the team who could create the smallest 2kW solar inverter with one million dollar. In

March 2016, Virginia Tech's Future Energy Electronics Center (FEEC) received 3rd place with total a power density of 69W/in^3, 38% more-dense than the competition's goals. In addition to high power density, FEEC team also managed to achieve high system efficiency, good thermal management, and EMI mitigation, these methods could also be introduced to the prototype in this thesis [14].

High power density is achieved by implementing WBG devices such as GaN and SiC, which have smaller profile and superior operating characteristics. Mechanically, a more compact printed circuit board (PCB) layout could also efficiently push the power density.

1.2.2 Achieving Low EMI Performance and easier EMI filter design

In order to achieve easier EMI filter design, according to FCC 15B in Table 1.4 [15], the harmonic frequency measurement starts from 150 kHz. Here keeping proposed inverter switching frequency below 75 kHz to avoid its multiples overlapping with 150 kHz for an easier EMI filter design.

Table 1.4. Harmonic Mearurement Freuquency According to FCC 15B.

Frequency(MHz)	Quasi-peak (dB uV)	Average (dB uV)
0.15-0.5	66-56	56-46
0.5-5	56	46
5-30	60	50

1.3 **Goal and Scope of Thesis**

The goal of this thesis is design a soft-switching inverter system to achieve high efficiency, high power density, and good harmonic performance.

The scope of this thesis will cover the operational analysis of proposed inverter, components selection, design tradeoffs, and performance assessment of proposed inverter.

The next section will cover the soft-switching operation analysis of proposed inverter along with the circuit structure, voltage divider phenomenon, and auxiliary gating optimization algorithm.

Section 错误!未找到引用源。 will cover the consideration of components selection including semiconductor devices and output filter design.

Section 错误!未找到引用源。 will discuss the experimental validation of the performance of proposed inverter, focusing on soft-switching operation, system overall efficiency, and auxiliary gating optimization.

2 Inverter Operation

2.1 Inverter Topology

The proposed novel auxiliary resonant snubber inverter is to achieve high power density and low EMI performance by switching for main devices under zero-voltage condition, and turning-off auxiliary diodes under zero-current conditions to fulfill high system overall efficiency. Besides, this soft-switching method can be applied to both bipolar and unipolar modulation for EMI performance consideration. Last but not the least, the switching frequency was selected at 60 kHz to avoid its multiples overlapping with 150 kHz, which is the starting frequency that needs to be complied for most EMI standards.

The proposed inverter topology is shown in Figure 2.1.

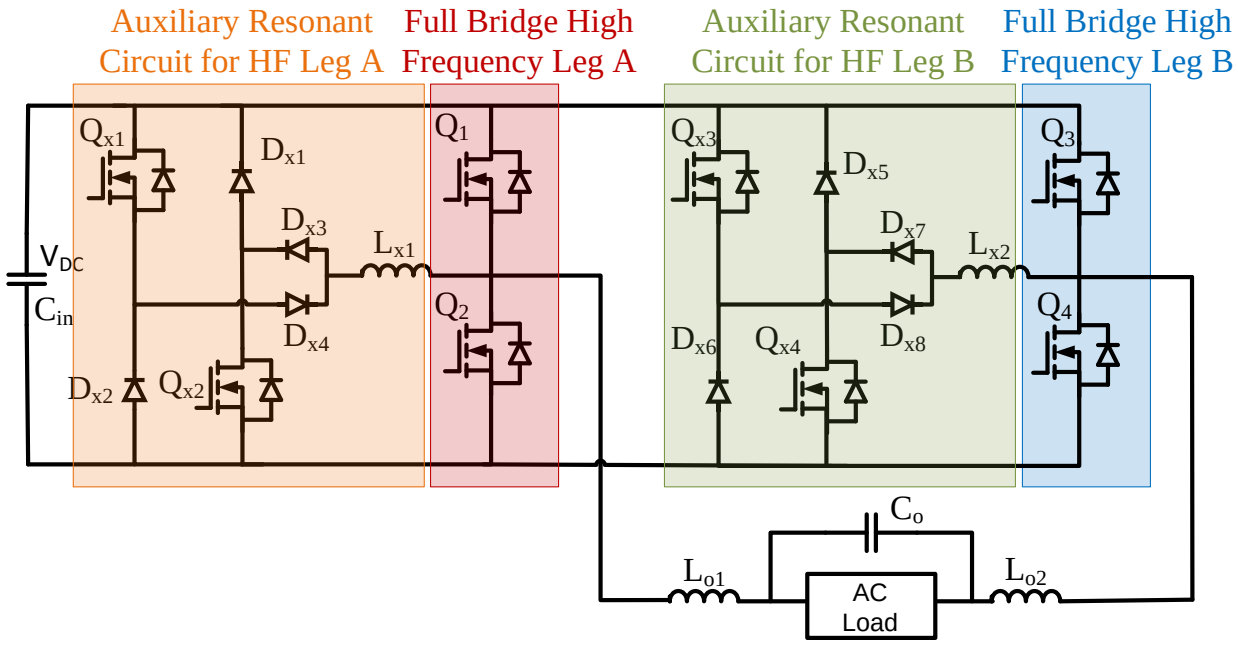


Figure 2.1. Proposed Inverter Topology.

L_{x1} and L_{x2} are auxiliary inductors that resonate with the drain-source capacitance of the main switches. The main MOSFET switches are Q_1 and Q_2 for leg A and Q_3 and Q_4 for leg B. Q_{x1},

Q_{x2}, Q_{x3}, and Q_{x4} are auxiliary MOSFETs and D_{x1}-D_{x8} are auxiliary diodes that assist the main switches in achieving zero-voltage switching (ZVS). These auxiliary switches and diodes also operate at zero-current switching (ZCS) turn-on.

2.2 **Soft-switching Operation**

As discussed in previous sections, in order to implement bipolar modulation as shown in 1.2, for the positive half line cycle, the diagonal switches Q_1 and Q_4 are turned on at the same time to allow the current to flow to the output. When Q_1 and Q_4 are turned off, the complementary diagonal switches Q_2 and Q_3 are turned on for the negative half line cycle to generate sine waveform.

Here, the operation for leg A top switch Q1 turning on under ZVS condition is illustrated in Figure 2.3-Figure 2.7. The procedure is divided into 5 stages which showing when leg 1 bottom switch Q2 is turned-off, then the auxiliary resonant snubber circuit for Q1 ZVS turn-on is enabled, and how Q1 achieves ZVS turning-on. The operation for bottom main switch Q2 turn on under ZVS is exactly the same as the top switch, so only one complementary switch soft-switching procedure is shown. Q1 naturally has ZVS by freewheeling during negative fundamental half cycle, the operation described below is during positive fundamental half cycle, when the ZVS needs to be achieved by auxiliary resonant snubber.

For clarity, the gate signal, current, and voltage across each device are kept same color with the diagram shown in Figure 2.2, e.g. all waveforms related to Qx1 are red.

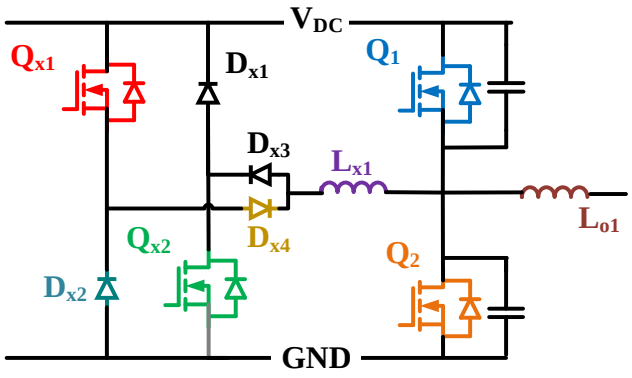


Figure 2.2. Proposed Topology Diagram for Leg A.

At t_0, bottom main switch Q_2 turns off at peak current, current continue go through Q2 anti-parallel diode, then contributes to output current, leaving the full DC bus voltage to Q_1. The auxiliary resonant snubber circuit for top main switch Q_1 is not enabled yet.

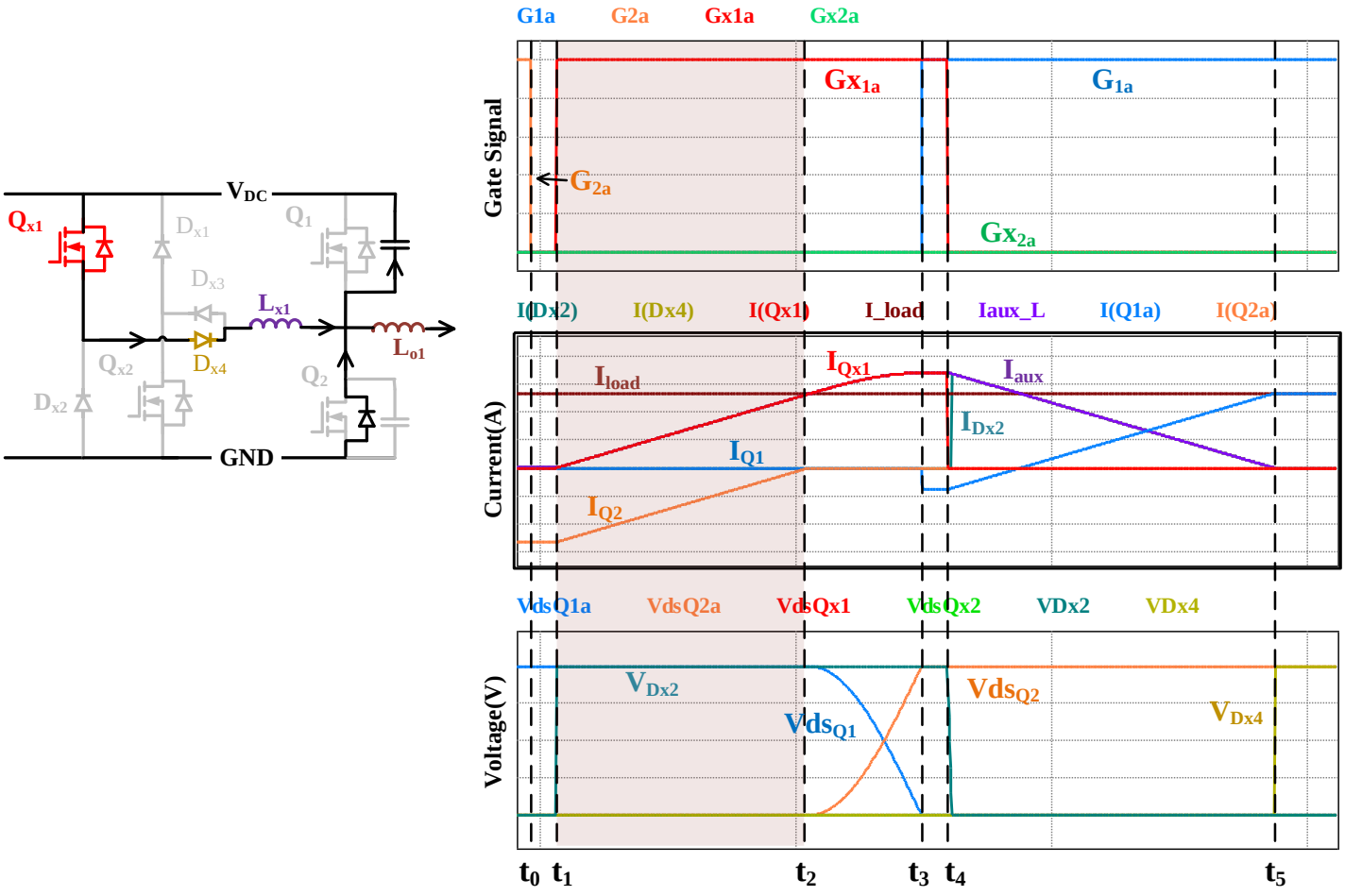


Figure 2.3. Operation for t_1-t_2 as Q_{x1} Turns on.

During t_1-t_2, as shown in Figure 2.3, auxiliary resonant switch Q_{x1} turns on and begins to conducting current through D_{x4}. The current of resonant inductor L_{x1} begins to increase linearly, and contributes to the output current, which leads the current goes through the anti-parallel diode of Q_2 decreases linearly.

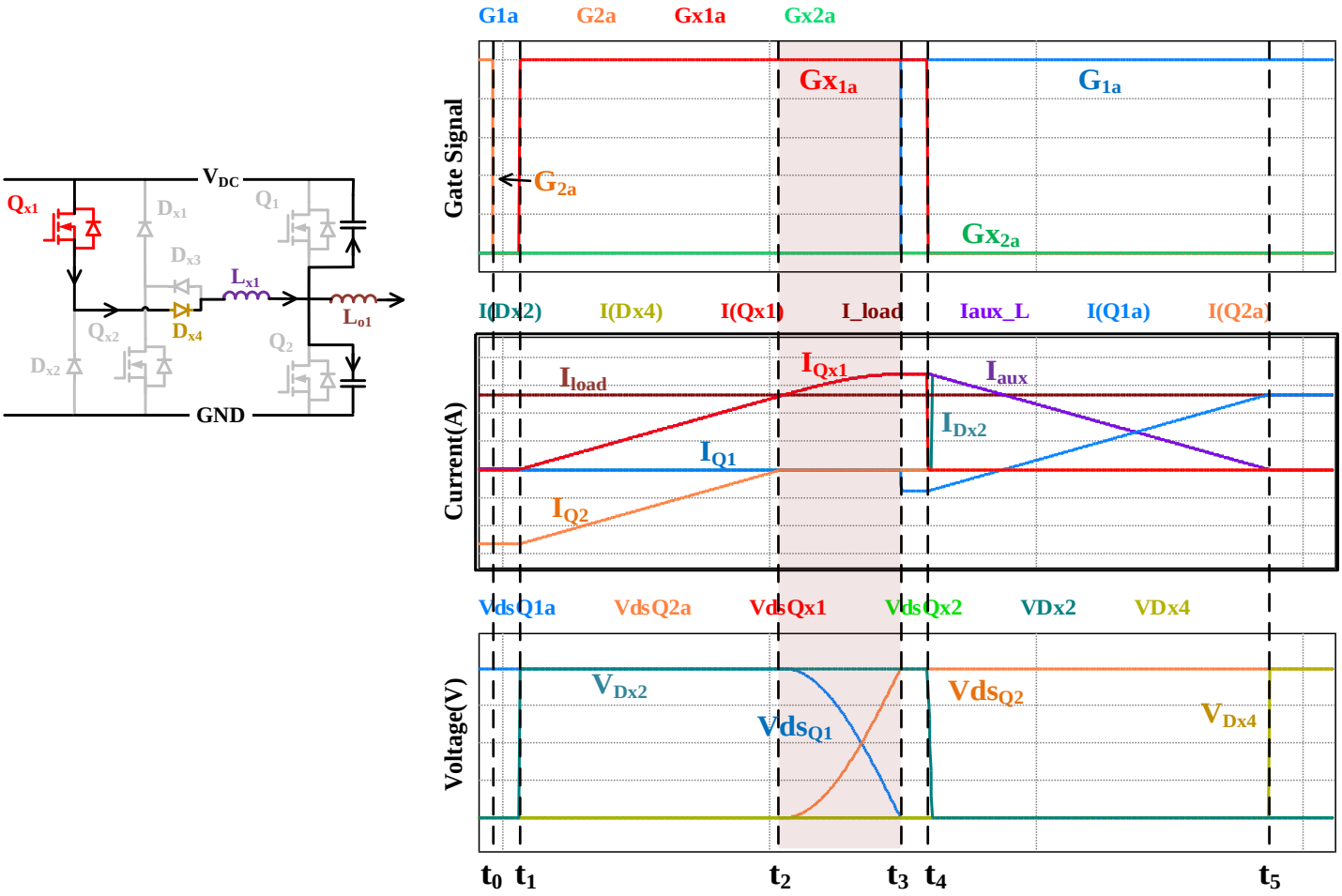


Figure 2.4. Operation of t2-t3 as Auxiliary Current Begins to Resonate.

During t_2-t_3, as shown in Figure 2.4. The current through L_{x1} is larger than output current, this current can be divided into two parts, and the matching part continues to contribute to output to maintain the current amplitude, so the anti-parallel diode of Q_2 no longer conducts current. Another one, which is the excessive current, resonates with the drain-source capacitance C_{oss} to discharge Q_1 to achieve ZVS turn-on and charge Q_2 to DC bus voltage.

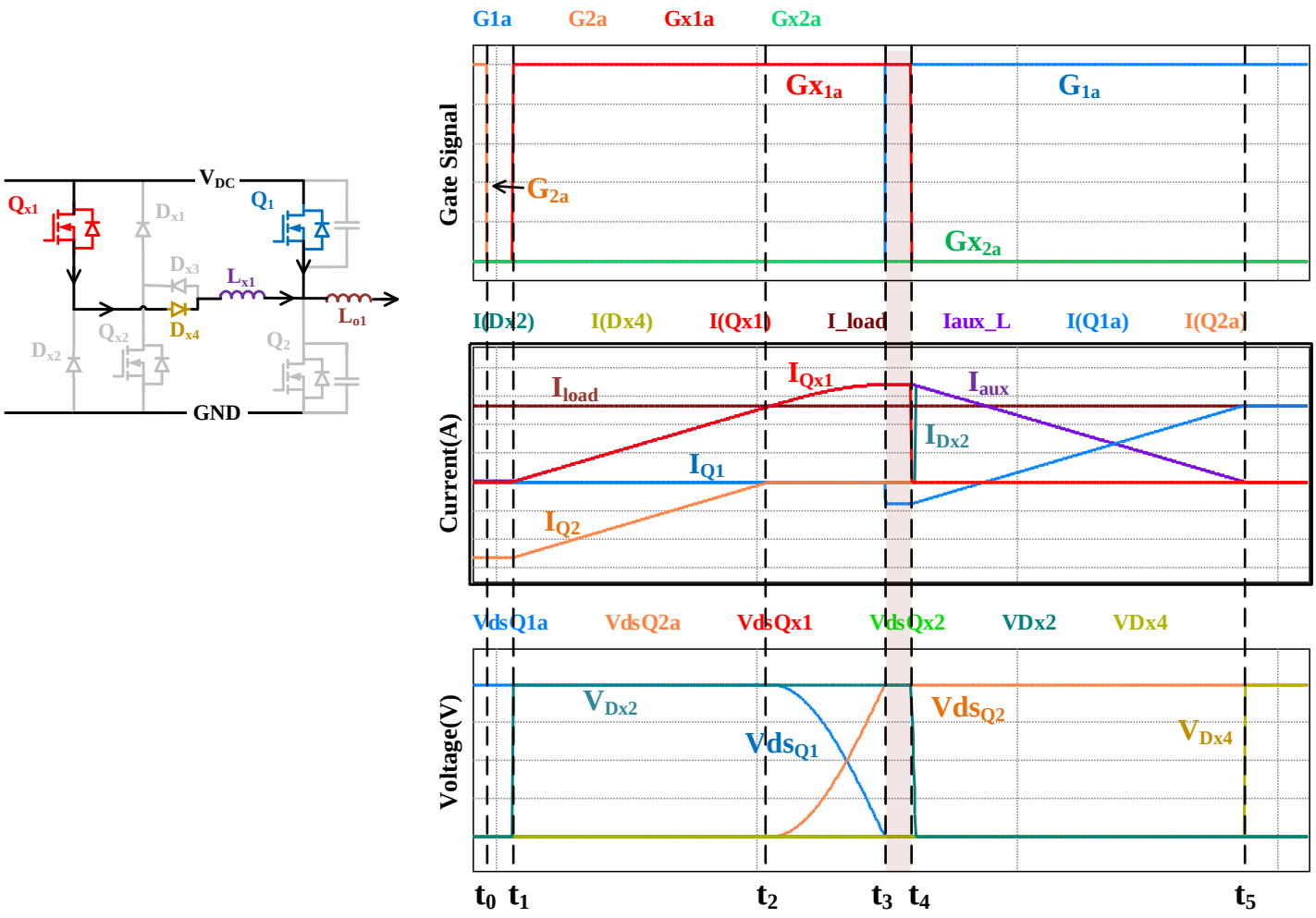


Figure 2.5. Operation of t_3-t_4 as Q1 Turns on under ZVS.

During t_3-t_4, as shown in Figure 2.5, the voltage across Q_1 is completely discharged to zero, so the top main switch can turn on under ZVS condition. The instant current through Q_1 cannot flip the polarity so it continue conducting though Q_1 anti-parallel diode. Meanwhile, C_{oss} of Q_2 is fully charged, all the DC bus voltage is across the bottom main switch Q_2.

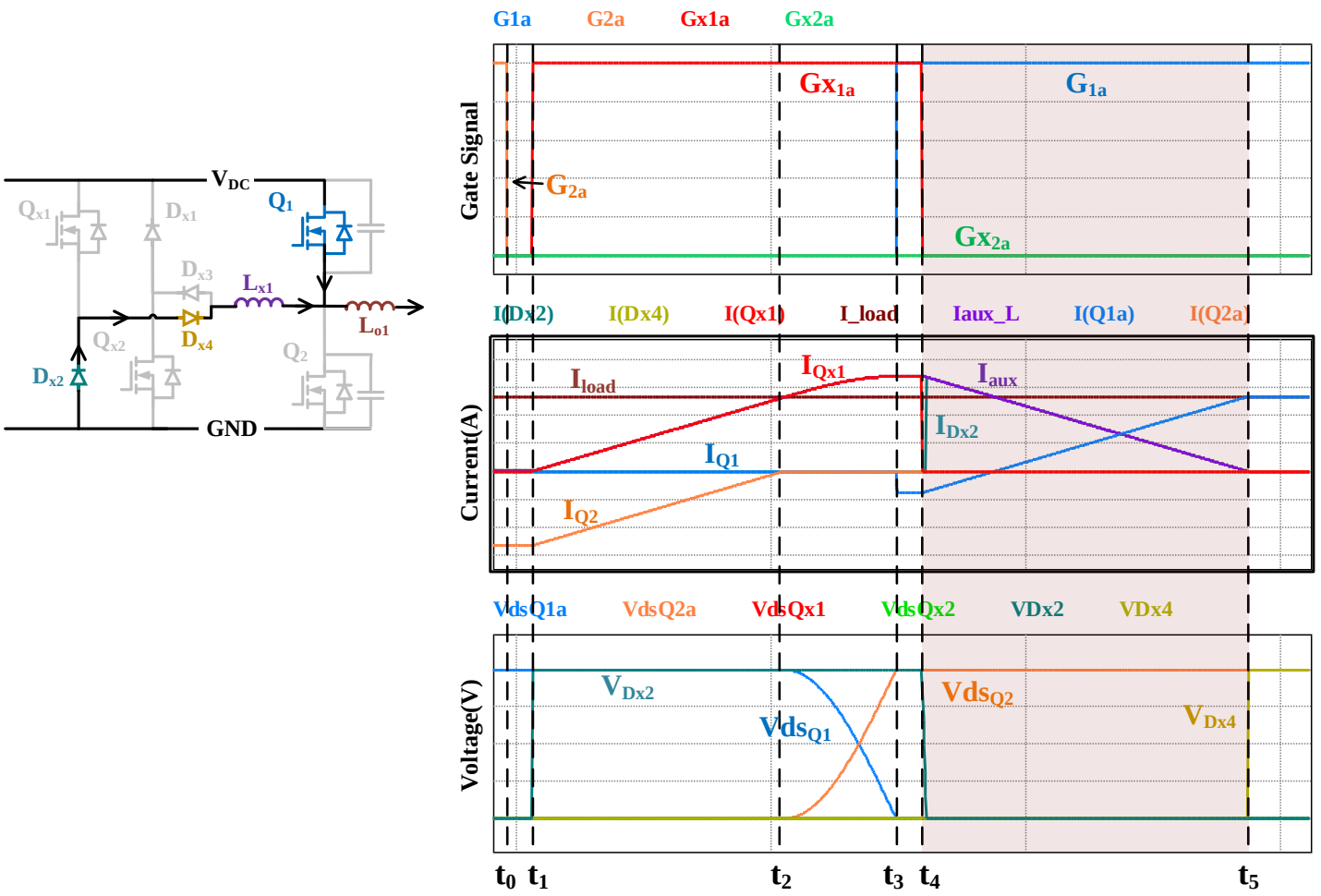


Figure 2.6. Operation of t_4-t_5 as Auxiliary Current Decreasing.

During t_4-t_5, as shown in Figure 2.6, the auxiliary resonant switch Q_{x1} turns off, auxiliary diode D_{x2} begins to conduct and the auxiliary current through D_{x4} and L_{x1} decreases linearly. When the auxiliary resonant current matches the output current, Q_1 anti-parallel diode no longer need to carry the excessive current and Q_1 begins to conduct.

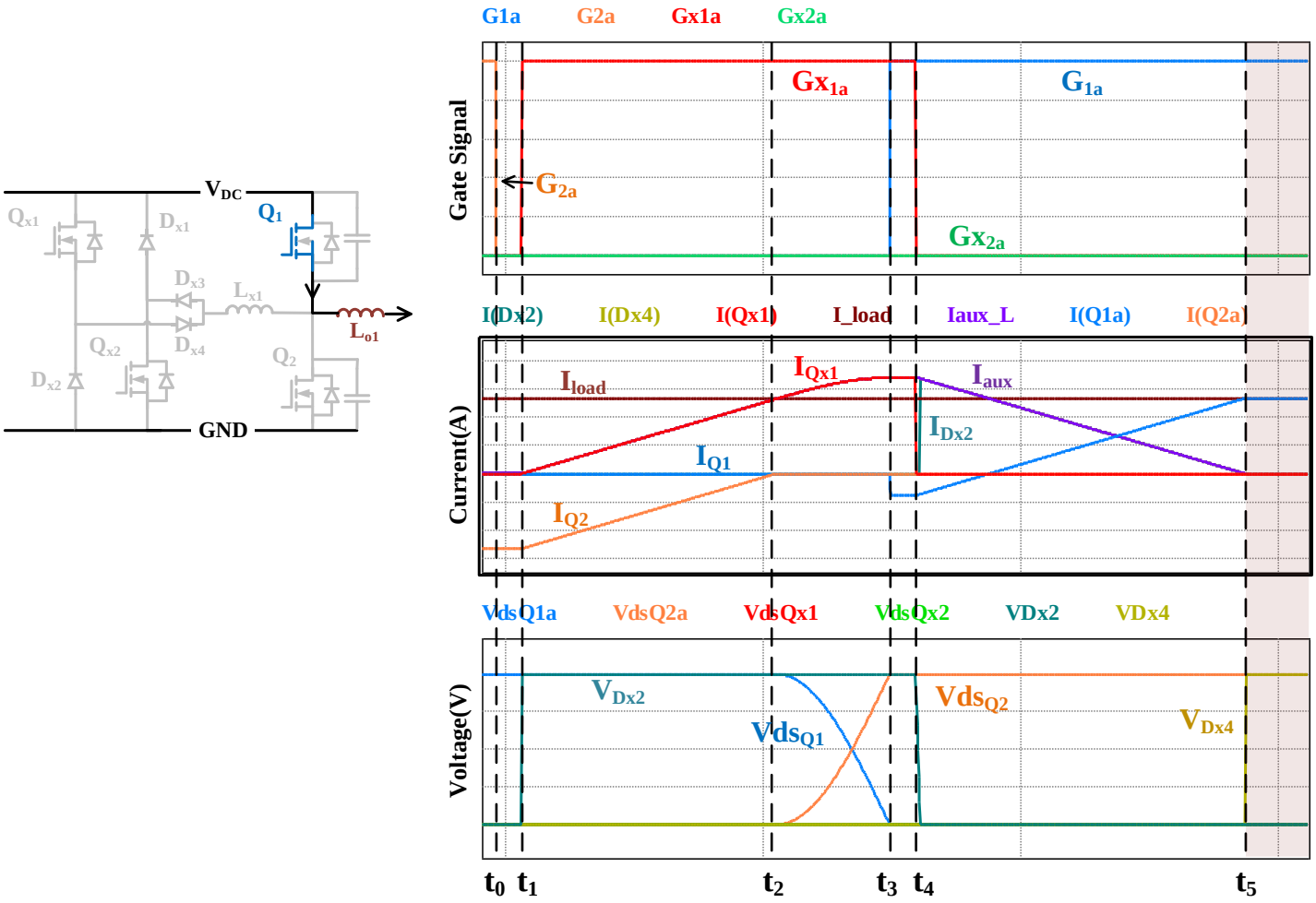


Figure 2.7. Operation after t_5 as the Auxiliary Resonant Procedure Completes.

After t_5, as shown in Figure 2.7, the auxiliary current decreases linearly to zero and the auxiliary diodes D_{x2} and D_{x4} are turned-off under ZCS condition. At this moment, the ZVS procedure for Q_1 is complete and all the output current is going through Q_1 for the remaining switching period.

2.3 Voltage Divider Phenomenon in Auxiliary Circuitry

After main switch ZVS turn-on is achieved as illustrated in section 2.2, auxiliary switches will be turned-off after 10ns in gating algorithm.

Under ideal scenario, after auxiliary switch Qx1 turning-off, the corresponding main switch Q1 is on already, another main switch Q2 is off thus leaving full dc bus voltage on the auxiliary switch.

However, under real, non-ideal circumstances, with parasitic capacitors added to auxiliary snubber circuitry in PSIM simulation, as topology for leg A which is shown in Figure 2.8. Voltage and current waveforms indicate that drain-source voltage of auxiliary switch Qx1 (Vds_Qx1) first rise to bus voltage, then Vds_Qx1 drops by 60V and after a series complex energy transfer inside the auxiliary circuitry, this part of voltage ends up to the parasitic capacitor of auxiliary diode Dx2 in the same leg. This phenomenon is carefully studied in this section since the energy transfer between active components and passive components parasitic components, it will affect the switching loss analysis for auxiliary switches and conduction loss analysis for auxiliary diodes. Furthermore, if there is current conducting during or after the voltages transfer procedure, the loss may cause severe problem such as device damage and inverter failure, which means this auxiliary snubber circuitry is not practical to implement.

Here, the energy transfer operation for leg A top auxiliary switch Qx1 is illustrated in Figure 2.9-Figure 2.12. The procedure is divided into 4 stages which showing after leg A top main switch Q1 is turned-on, then the auxiliary resonant snubber circuit for Q1 ZVS turn-on is disabled, and how Qx1 Vds drops and where this part of voltage ends up. The phenomenon for bottom auxiliary switch Qx2 is identical as the top auxiliary switch, so only study on Qx1 is described in this section.

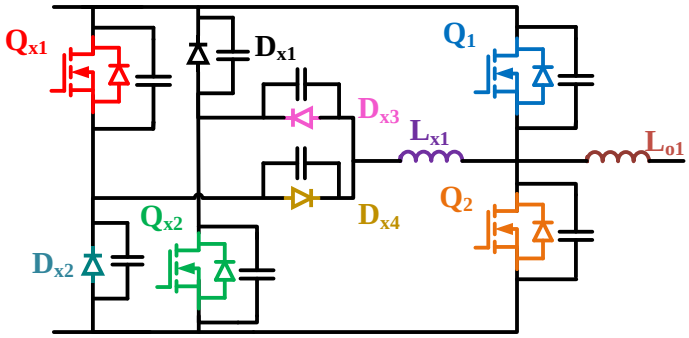


Figure 2.8 Leg A Topology with Parasitic Capacitors Added.

At t0, Qx1 turns off at peak current 10 ns after Q1 is ZVS turn-on. Current through Qx1 reduce to zero immediately.

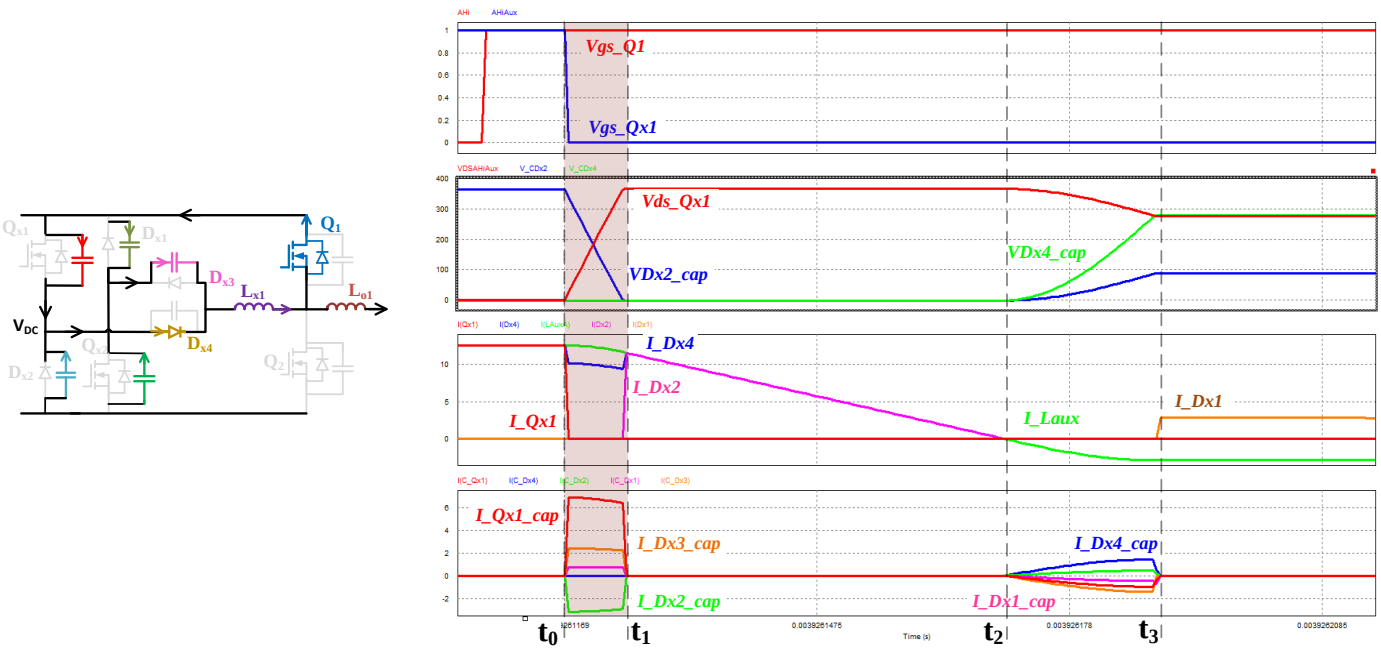


Figure 2.9. Operation During t0-t1 as Auxiliary Current Charging C_Qx1.

During t0-t1, as shown in Figure 2.9, remaining auxiliary current through auxiliary inductor (Lx1) begin decrease as Qx1 turned off, while I_Lx1 cannot change polarity immediately, the auxiliary current flow through Q1 anti-parallel diode, charging the parasitic capacitors of Qx1

and Dx3, meanwhile discharging the parasitic capacitors of Qx2 and Dx2, then the current conducting though Dx4 and charging Dx3 junction capacitor, to close the current loop.

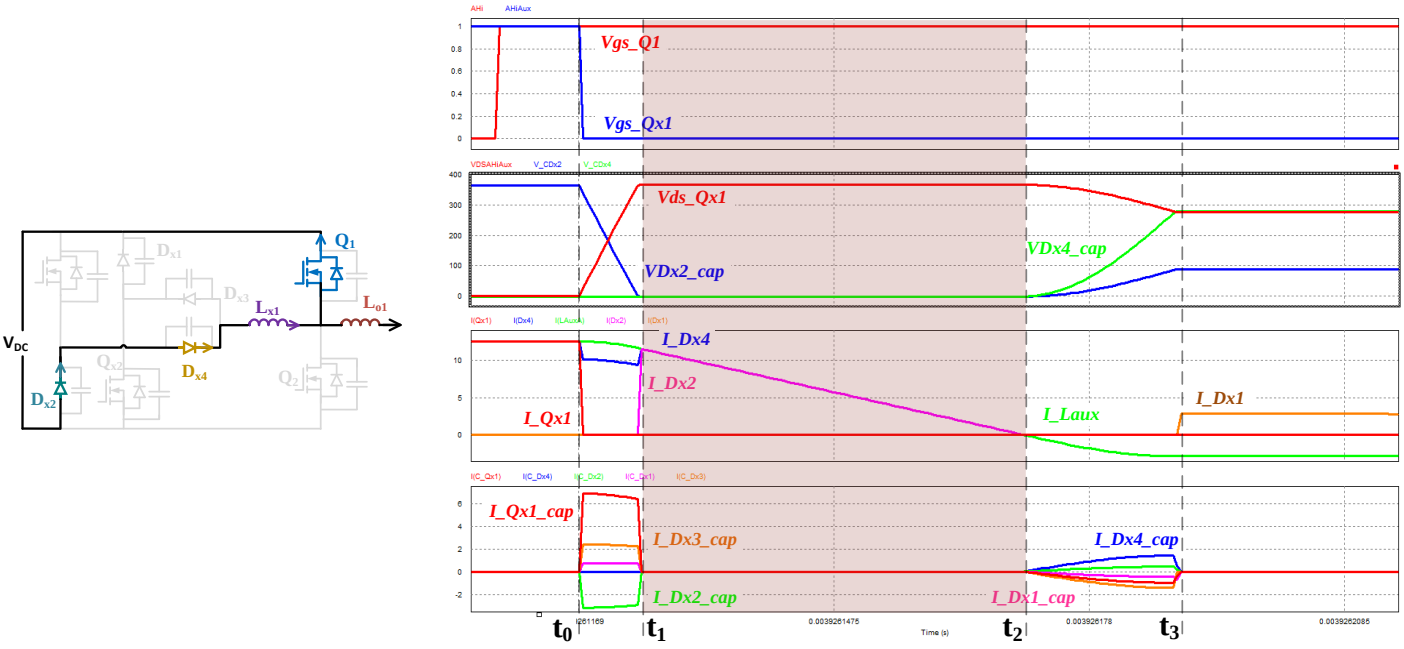


Figure 2.10. Operation During t1-t2 as Auxiliary Current Decreasing.

During t1-t2, C_Qx1 is fully charged to bus voltage. Due to much slower turn-off speed of SiC Schottky diode than GaN switch, Dx4 is not turned-off yet and auxiliary begin conducting though Dx2, dc bus and finally decrease to zero.

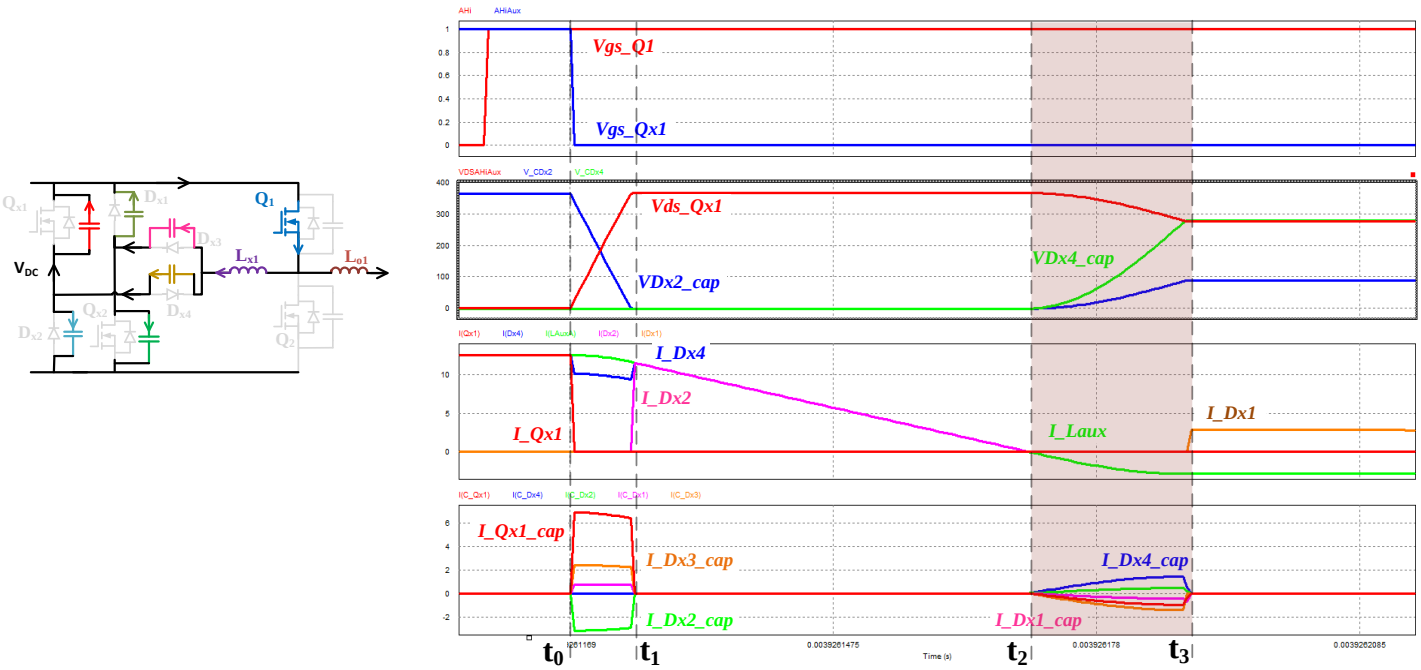


Figure 2.11. Operation During t2-t3 as Energy Transferring Between Parasitic Capacitors.

During t2-t3, voltage at middle point of leg A is bus voltage and is higher than the middle point of Qx1 and Dx2, force Dx4 turn off completely. I_Lx1 flow to reverse direction after it decreased to zero, discharging C_Qx1, C_Dx3 and C_Dx1, then through Q1 and charging C_Dx4, C_Dx2.

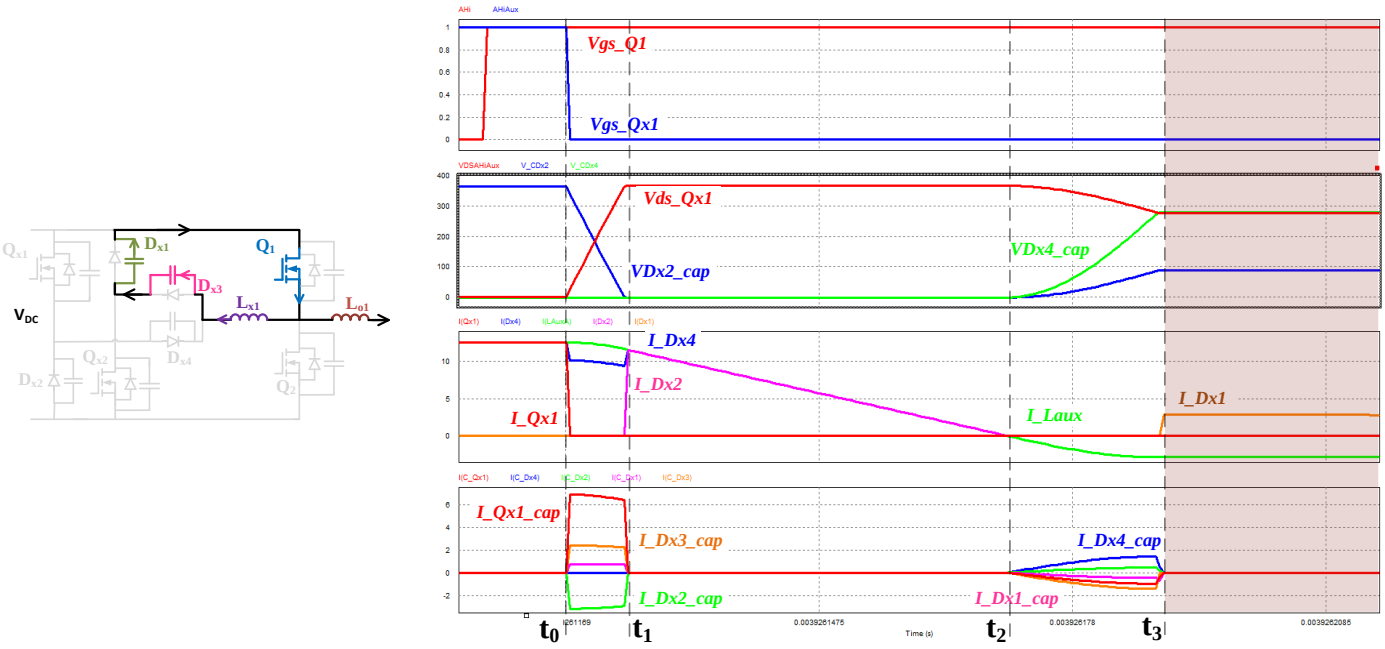


Figure 2.12. Operation after t3 as Auxiliary Current Decrease to Zero and Freewheeling.

After t3, the voltage go steady, the whole bus voltage across C_{Qx1} is transferred partially to C_{Dx2}. The unbalance of voltage division and parasitic capacitor impedance will be explained next.

In simulation, after adding parasitic capacitors paralleled to ideal auxiliary switches and diodes, device voltage is divided, which verified that this phenomenon is caused by device parasitic capacitors. From simulation, C_{Qx1} and C_{Dx2} are set to 130pF and 60 pF thus the ratio is 2.2:1. However, the voltage ratio between C_{Qx1} (V_C_{Qx1}) and CDx2 (V_C_{Dx2}) is around 3.2:1.

The capacitance are obtained from datasheet, and in simulation the parasitic capacitor nonlinearity is ignored. Due to GaN device fast turn-off capability, the di/dt of auxiliary switch (Q_{x1}) is much larger than auxiliary diode (D_{x2}), even though it is SiC Schottky diode, the auxiliary diodes still need more time than auxiliary switch to fully turned-off.

The total charge of parasitic capacitor can be calculated from equation 2.1.

$$Q = \int di / dt \qquad 2.1$$

Then the voltage across the capacitor can be obtained from equation 2.2.

$$V = \frac{Q}{C} \qquad 2.2$$

Since the total charge for auxiliary switch (Q_{SW}) is much larger than it of auxiliary diode (Q_D), although C_{Qx1} is also larger than C_{Dx2}, the voltage distribution of this leg is determined by total charge rather than capacitor impedance. As a result, in simulation, the voltage division ratio is larger than parasitic capacitance ratio.

From the analysis above, the switching loss of auxiliary switch is larger than theoretical value since the energy is transferred from C_{Qx1} to C_{Dx2}. Energy transfer also indicates the heat is transferred as well, so the thermal performance and cooling method for auxiliary switch should be paid to additional attention.

2.4 **Auxiliary Switch Gating Optimization**

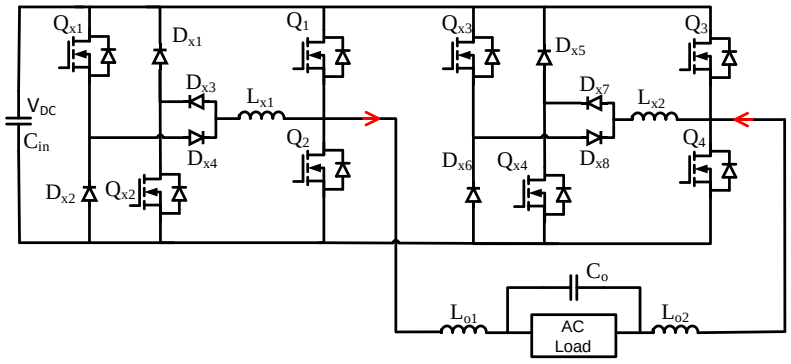


Figure 2.13. Proposed Inverter Topology with Output Current Direction During Positive Fundamental Cycle.

From the analysis in section2.2, in every fundamental cycle, one pair of main switches in diagonal will have inherent ZVS achieved by freewheeling. Take leg A (Q1 and Q2) as example, as shown in Figure 2.13, when during positive half fundamental cycle, output current going

outwards direction, thus Q2 inherently has ZVS achieved during freewheeling stage. And Q1 will have natural ZVS during negative half fundamental cycle, vice versa. Which is summarized in Table 2.1.

Table 2.1. Freewheeling Stage for Full-bridge Inverter Switches.

	Leg A		Leg B	
	Q1(HS)	Q2(LS)	Q3(HS)	Q4(LS)
Positive cycle	Qx1	freewheeling	freewheeling	Qx4
Negative cycle	freewheeling	Qx2	Qx3	freewheeling

Hence, during positive half fundamental cycle, for Q2, the corresponding auxiliary switch Qx2 can be turned-off to reduce both switching loss and conduction loss, which can further release the thermal stress on auxiliary switches and have better system overall efficiency.

In control algorithm, the auxiliary switches gating optimization is generated by sensing output inductor current (I_L). When sensed I_L average value is larger than 1A, the auxiliary switches are forced to turn-off during freewheeling half fundamental cycle.

The comparison in simulation is shown in Figure 2.14. After the auxiliary gating is optimized, Qx2 doesn't need to turn-on during Q2 freewheeling. ZVS is obtained in both figures but the optimized circuitry doesn't have unnecessary negative auxiliary resonant current.

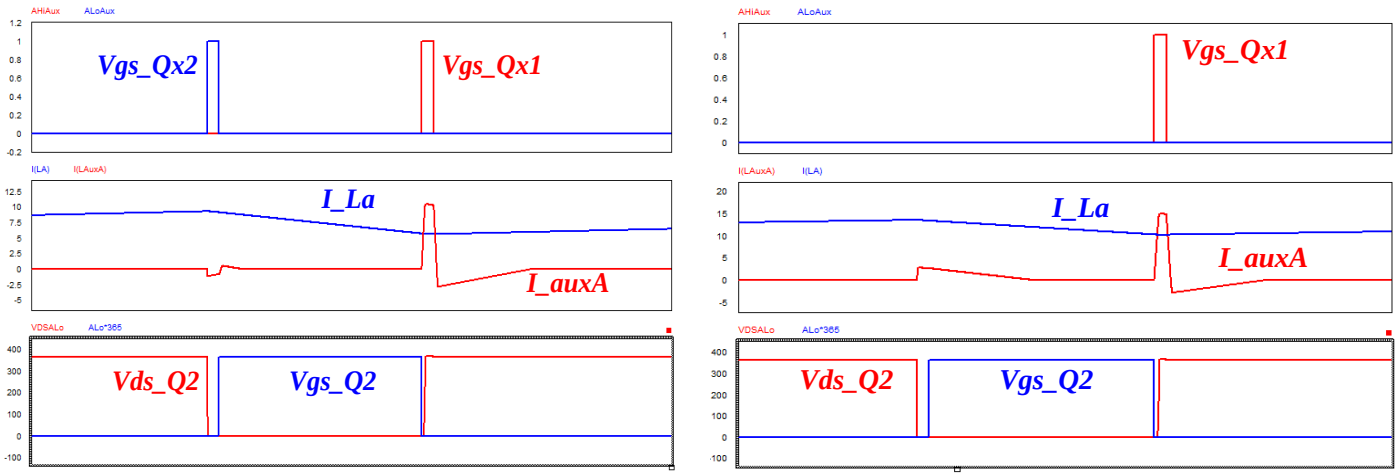


Figure 2.14. Waveform Showing After Optimization Unnecessary Auxiliary Current Reduced.

3 Inverter Power Stage Design Tradeoffs

This chapter will illustrate the design procedure of proposed inverter power stage in detail. The design and components selection are targeting at high efficiency, high power density, and low EMI performance.

The proposed inverter can connect to photovoltaic (PV) panels and stationary distribution. So the prototype specifications e.g. input DC bus voltage and output AC voltage are chosen as summarized in Table 3.1.

Table 3.1 Prototype Design Specification.

Parameter	**Value**
Input DC Voltage	365 $V_{nominal}$
Output AC Voltage	240 V_{rms}
Output Frequency	60 Hz
System Power Level	2 kW

Besides, loss breakdown analysis for major active and passive components are delivered. After the active components are selected and passive components values are determined, the voltage and current stress for each device are carried out by PSIM level 2 simulation for a better accuracy.

3.1 **Switching Frequency**

Switching frequency is one of the key design specifications. There is a tradeoff between switching loss and passive component sizes when pushing the switching frequency to high range. Since one of the design targets is low EMI performance, easier EMI filter design is also preferred. From

Table 1.4 错误!未找到引用源。, which is the FCC part B standard that specifies the frequency bands in which those emissions must be controlled in certain ranges.

The measured frequency range starts from 150 kHz and typically the most severe harmonic will be at double switching frequency. So the switching frequency is set at 60 kHz, which doubles at 120 kHz and not included in the specified measuring range, thus easier for EMI filter design to pass the requirement.

Besides, since bipolar modulation is implemented here, the common mode noise is inherent negligible, which is another advantage in EMI filter design.

3.2 **Main Switch Selection**

Main switch must have the capability to handle the voltage and current stress while minimize the loss dissipation to have better thermal and efficiency performance. From the design specification in Table 3.1 Prototype Design Specification.Table 3.1, nominal output current rms value would be 8.34A. Because the input DC bus voltage is 365V, the main device must have voltage rating of at least 600V to obtain some safety margin. Besides, a low device on-resistance is preferred to have lower conduction loss.

With the pursuit of high switching frequency to reduce passive components size and improve system overall efficiency, GaN System GS66516T 650V, 60A, 25mΩ E-mode transistor is implemented in this prototype. Compared to traditional Si device, GaN device has the advantages of lower on-resistance, higher switching speed to reduce loss and achieve higher efficiency while having a smaller package to reduce system weight and volume to obtain higher power density. Besides, GaN E-HEMT has much lower gate charge (Q_g) compared to traditional Si MOSFETs, so the gate drive loss will be less.

GaN System GS66516T is a very thin top-cooled chip, which means it can be placed on the back of the PCB board and attach directly to the heatsink while the gate driver and other gate operating components mounted on the top. This can help the device heat spread and increase the system stability.

3.2.1 Main Switch Loss Analysis

After the main switch device is selected, imported device parameters into PSIM level 2 model to calculate the switching and conduction loss of the main switches.

The main switches have ZVS turn-on and hard turn-off, so when calculating the switching loss, only turn-off loss need to be estimated. From the datasheet, the turn-off switching energy E_{off} is 14.7uJ under 20A testing condition [16]. And the average turn-off current is 3.75A, so the switching loss of the total 4 GaN MOSFETs is calculated from Equation

$$P_{sw\_off} = 14.7uJ \times (\frac{3.75A}{20A}) \times 60kHz \times 4 = 0.66W \qquad 3.1.$$

$$P_{sw\_off} = 14.7uJ \times (\frac{3.75A}{20A}) \times 60kHz \times 4 = 0.66W \qquad 3.1$$

The conduction loss expressed in $P_{cond} = 2 \times I_{Q,rms}^2 \times (R_{dson} \times 2) = 2 \times 8.33^2 \times (26 \times 4) = 7.22W$

3.2, which the $I_{Q,rms}$ is the rms current through the GaN MOSFETs and R_{dson} is the drain-source resistance of the MOSFETs.

$$P_{cond} = 2 \times I_{Q,rms}^2 \times (R_{dson} \times 2) = 2 \times 8.33^2 \times (26 \times 4) = 7.22W \qquad 3.2$$

From the analysis above, the total loss of the 4 main switches is 7.88W.

3.2.2 Gate Driver Design

Due to the high switching speed and high dv/dt, attention should be carefully paid when designing the gate driver of GaN MOSFETs. However, the proposed topology has soft-switching so the dv/dt is lower, the design criteria might be relaxed. Besides, the full-bridge topology using top-cool device package will have 4 switches placed at the bottom of the PCB board, as mentioned at beginning of section 3.2, the main switch gate driver circuit will be mounted at the top, so there is a challenge in design and arranging the main switch gate drivers.

For high side gate driver, there are two main categories, one is fully isolated gate driver, which has better accuracy and EMI performance. And another one is bootstrap gate driver, which is widely used in high-side gate driver circuit with simplicity and lower cost. The summarized comparison chart is shown in Table 3.2. From the pursuit of high power density, the device counts need to be minimized, so boot-strap gate driver is selected.

Table 3.2. High-side Gate Driver Structure Comparison.

	Full isolated	Bootstrap

Pro	1. Better performance 2. Better noise (EMI) performance	1. Lower cost(cut voltage regulator device counts to half) 2. Simpler circuit
Con	1. Higher cost 2. More device counts	1. Post-regulation or voltage clamping required 2. Fast reverse recovery bootstrap diode

There are two kinds of gate driver within bootstrap circuit category, they are unipolar and bipolar gate drivers. Unipolar gate driver means MOSFETs will turn on at positive voltage, usually 5-7V, and turn off at zero voltage. Bipolar gate driver indicates the MOSFETs will turn on at similar positive voltage as unipolar, but turn off at negative voltage. The comparison of these two gate drivers are summarized in Table 3.3.

Table 3.3. Gate Driver Voltage Comparison.

	Unipolar gate driver	Bipolar gate driver
On/off voltage	+7/0V	+6/-3V
Pros	1. Simple implementation 2. Lower deadtime reverse conduction loss	1. Lower gate oscillation risk 2. Lower switching loss
Cons	1. More sensitive to layout parasitics	1. Higher deadtime reverse conduction loss

Compared to bipolar gate driver, unipolar is more sensitive to noise, but after the soft-switching method implemented to main GaN MOSFETs, this is no longer a drawback for unipolar gate driver. Also, considering the large amount of main GaN MOSFETs and the goal of high power

density, gate driver counts need to be minimized to consume less space and benefit power density. Here in this prototype, unipolar gate driver based on Silicon Lab half-bridge gate driver Si8273 is used, combined with customized 7V isolated power supply MIC5225. The prototype gate driver schematic for one half-bridge leg is shown in Figure 3.1.

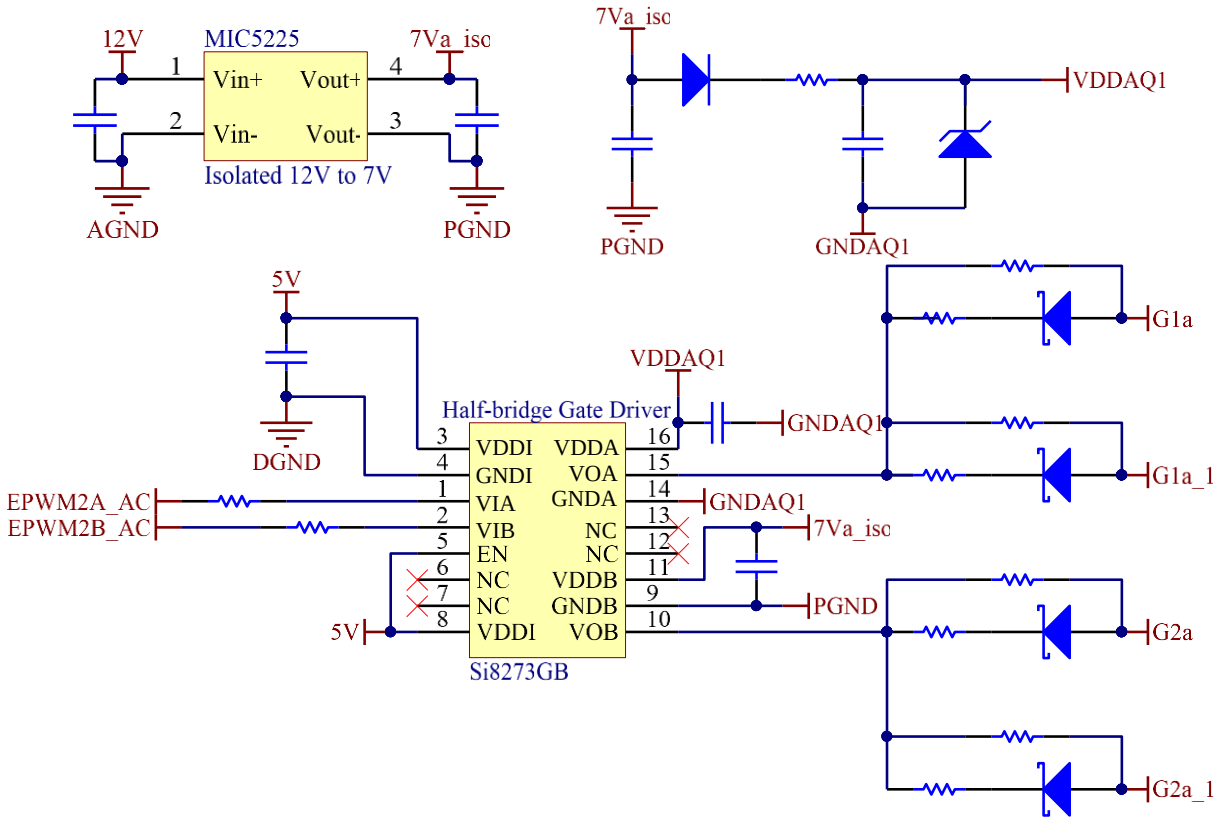


Figure 3.1. Main Switch Gate Driver Design Schematic.

3.3 **Resonant Circuit and Deadtime Relationship**

The design for auxiliary resonant circuitry contains three steps. First, the relationship between deadtime and resonance, which will be explained in this section. Next, from the equation derived in last step, fix the inductance and capacitance for resonance. Last but not least, complete the

design by selecting active component in auxiliary resonant circuitry such as auxiliary switch and diode.

The auxiliary resonant circuitry for one half-bridge leg and its equivalent topology are shown in Figure 2.2 and Figure 3.2.

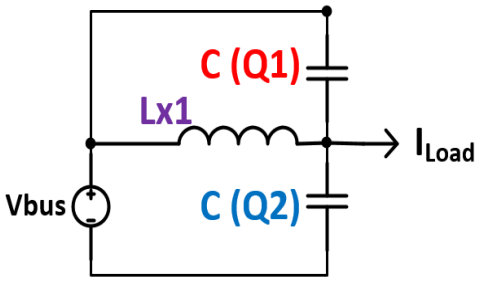


Figure 3.2. Equivalent Auxiliary Resonant Circuitry.

The relationship between deadtime and resonance is shown in equation 3.3.

$$t_d \geq t_{linear} + t_{res} = \frac{L_{x1} I_{load}}{V_{bus}} + \pi \sqrt{L_{x1}(C_{Q1} + C_{Q2})} \qquad 3.3$$

Where t_{linear} is the amount of time that auxiliary inductor (L_{x1}) current charges from zero to output current. t_{res} is the amount of time that L_{x1} begins to resonant with main switch drain-source capacitor (C_{Q1}) to drain the switch voltage to zero in order to achieve ZVS.

After setting the deadtime limitation, L_{x1} and C_Q can be calculated.

3.4 **Resonant Components Design Tradeoffs**

The relationship between deadtime and resonant inductor and capacitor equation is derived in section 3.3. In this section, how the resonant capacitance is selected, and the auxiliary resonant inductance derivation will be described in detail.

3.4.1 Auxiliary Resonant Capacitance Design

The resonant soft-switching method in this prototype is using the main switch natural drain-source capacitance (C_{DS}) as the auxiliary resonant capacitor (C_{res}). The lateral structure for E-mode GaN device has the advantage of a smaller C_{DS} compared to other Si based MOSFETs. For the main GaN MOSFET selected in section 3.2, C_{DS} is 130pF. The design consideration in this section is whether to add additional parallel capacitor to the main switch. The advantage of adding additional capacitor is that it will decrease the non-linear instability of inherent C_{DS} and also reduce the turn-off loss of the main switch. The reason is that larger C_{DS} will slow down the main switch slew rate (dv/dt), so when switch turns off, the across voltage (V_{DS}) will rise slower while the current through device (I_{DS}) still decreases at the same rate, the overlap of V_{DS} and I_{DS} is smaller so the turn-off loss is less compared to no additional capacitor added.

However, the tradeoff is increasing the deadtime and resonant current peak value. After adding additional parallel capacitor, the total charge of capacitor is increased, which leads to longer charging and discharging time hence longer deadtime is required. Also, the resonant peak current ($I_{Lx1,2\_peak}$) can be estimated from equation $I_{Lx1,2\_peak} = \frac{C_{DS} V_{BUS}}{L_{x1,2}}$ 3.4, with larger C_{DS}, the peak value will increase and cause higher current stress on the auxiliary resonant circuit devices.

$$I_{Lx1,2\_peak} = \frac{C_{DS} V_{BUS}}{L_{x1,2}} \qquad 3.4$$

The comparison is summarized in Table 3.4.

Table 3.4. Tradeoff of Adding Parallel Capacitor.

	Yes	No
Capacitance	C_{DS} + additional cap	C_{DS}

C_{DS} non-linearity	Lower	Higher
Main switch turn-off loss	Lower	Higher
Deadtime	Longer	Shorter
Device number	More	Less
Resonant peak current	Higher	Lower
Aux device stress	Higher	Lower

Considering the auxiliary device selection and the pursuit of higher system efficiency, no additional parallel capacitor is added to main switch in this prototype.

3.4.2 Auxiliary Resonant Inductor Design

Auxiliary resonant inductors (L_{x1} and L_{x2}) are the key components for proposed topology soft-switching operation. Attention need to be paid carefully to the design tradeoffs such as $I_{Lx1,2\_peak}$ and resonant time/deadtime balance. With fixed C_{res}, larger $L_{x1,2}$ will increase the resonant time and cause longer dead time, which will lead to more conduction loss in the resonant circuit.

However, if L_{res} is too small, as shown in equation $I_{Lx1,2\_peak} = \frac{C_{DS}V_{BUS}}{L_{x1,2}}$ 3.4, the resonant peak current will be too high and cause devices failure in auxiliary resonant circuit. Thus, the design principle for $L_{x1,2}$ is the largest inductance within the limited dead time.

The design procedure for $L_{x1,2}$ is shown in following steps.

First, fix the key auxiliary resonant circuit parameters, summarized in Table 3.5.

Table 3.5. System Target Specifications.

Switching Frequency(f_{sw})	60 kHz
Resonant Capacitance(C_{res_Q})	130 pF

Dead Time(t_d)	150 ns
Bus voltage(V_{bus})	365 Vdc
Output Peak Current(I_{load})	11.78 A

Second, the sum of $L_{x1,2}$ increasing linearly time (t_{linear}) and resonant time (t_{res}) should be within t_d.

From the equation 3.3, a resonant inductance of 1.46uH is chosen.

Finally, select the appropriate core shape and material for $L_{x1,2}$. The switching frequency is 60 kHz and the resonant frequency is 5.8 MHz, which is calculated from equation 3.5.

$$f_{res} = \frac{1}{2\pi\sqrt{L_{1,2} \times 2C_{res}}} = 5.8 \times 10^6 \qquad 3.5$$

From the auxiliary resonant inductor current FFT analysis in simulation, the frequency content at resonant frequency is negligible, so L_{res} core material only need to optimize at switching frequency.

Here in this prototype, 3C94 RM6 core is selected, AWG16 litz wire is used.

3.4.3 Auxiliary Resonant Inductor loss analysis

The auxiliary inductor has 6 turns for each one. The total core loss (P_{Fe}) for two $L_{x1,2}$ is calculated from equation 3.6. P_{CV} is the core power loss of material 3C94 at estimated flux density, l_e and A_e are the effective length and area of the RM6 core. The winding loss is calculated from equation 3.7 and 3.8, where litz wire DCR is calculated from the resistance/length of AWG16, which is 13.17mΩ/m, average length per turn of RM6 core, which is 31mm, and the turns ratio of $L_{x1,2}$. And P_{Cu} is the winding loss of $L_{x1,2}$, I_{rms} is the rms current through $L_{x1,2}$.

$$P_{Fe} = 2 \times P_{CV} \times l_e \times A_e$$
$$= 2 \times 60k \times 10^{-9} \times 29.2mm \times 37mm^2 = 0.13W \quad 3.6$$

DCR = Resistance per length × Average length per turn × number of turns

$$= 13.7 \times 6 \times 31 \times 10^{-3} = 2.45m\Omega \quad 3.7$$

$$P_{Cu} = 2 \times I_{rms}^2 \times DCR = 2 \times 1.83^2 \times 2.45 \times 10^{-3} = 16.4mW \quad 3.8$$

3.5 **Auxiliary Active Components Selection**

This section contains the active components of the auxiliary resonant circuit, which are the auxiliary switch and diode. The device selection consideration, switch gate driver design and loss breakdown are covered in detail.

3.5.1 Auxiliary Switch Selection

Auxiliary switch must has the capability to handle the voltage and current stress while minimize the loss dissipation to have better thermal and efficiency performance. From the soft switching operation described in section 2.2, the auxiliary switch also operates at the same frequency as the main switch to ensure main switch ZVS turn-on, thus the auxiliary switch also need to have fast-switching capability. Besides, since the soft-switching is realized in such a short period of time, the auxiliary switch should have ultra-fast turn-on and turn-off speed to manage soft-switching at every switching cycle.

The voltage stress across auxiliary switch is the 365V DC bus voltage, so the voltage rating for auxiliary switch should be at least 600V to have some safety margin. Also the auxiliary resonant inductor has peak current of 30A and it is in series with the auxiliary switch, thus the auxiliary switch should have current rating more than 30A. Considering the auxiliary switch is hard-

switching, and the overall rms current through it is very small, so compared to conduction loss, switching loss is more significant, thus switch with smaller E_{on} and E_{off} is preferred. Here in this prototype, GaN System GS66516B 650V, 60A, 25mΩ E-mode transistor is selected to meet all the design requirements discussed above. This GaN MOSFET is the same as the main switch except the package. GS66516B is bottom-cool so it will be mounted on the top of the PCB board for easier gate driver design and components placement.

3.5.1.1 Gate Driver Design

The gate driver design for auxiliary GaN MOSFETs is similar as the main switch, high side bootstrap circuit with Silicon Lab gate driver SI8271 combined with same customized 7V isolated power supply MIC5225. The auxiliary gate driver schematic for one half-bridge leg is shown in Figure 3.3.

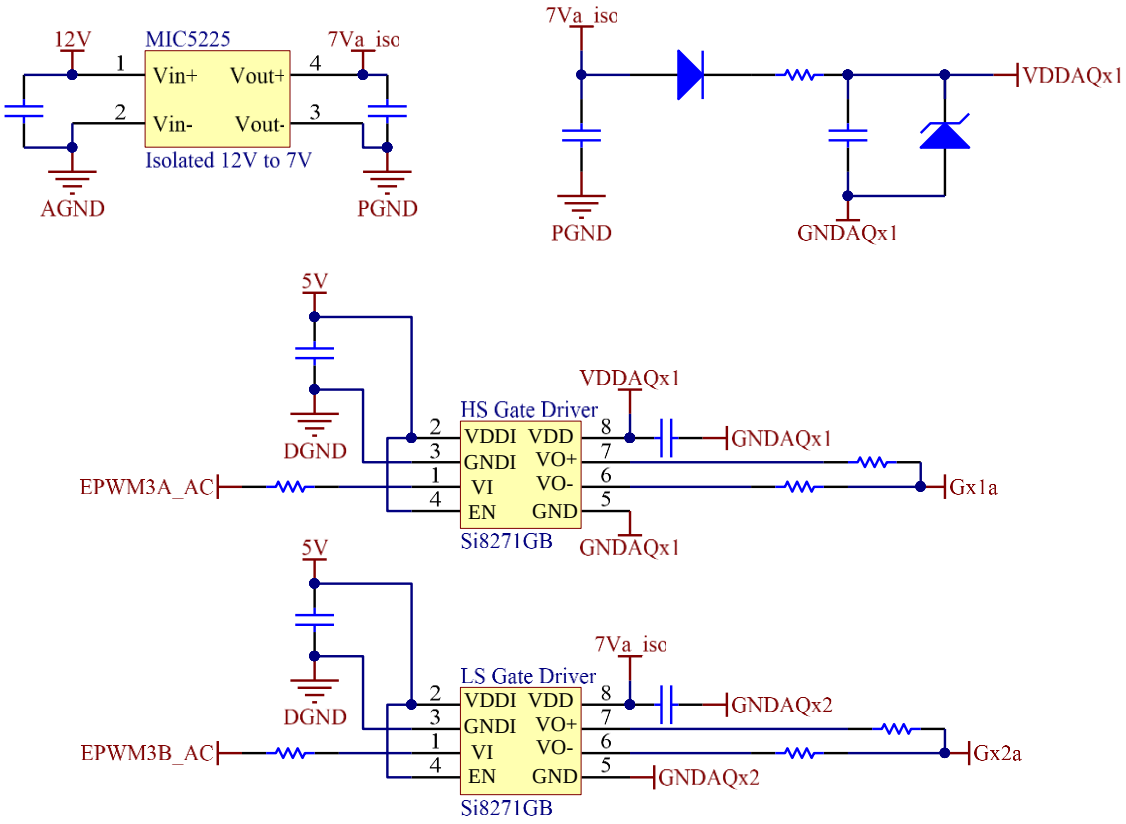


Figure 3.3. Gate Driver Design for Auxiliary Switch.

3.5.1.2 Auxiliary Switch Loss Analysis

Because the auxiliary switch is hard-switching, and with auxiliary switch gating optimization, each auxiliary switch is functioning half of the fundamental sine cycle.

However, due to the voltage divider phenomenon discussed in section 2.3, auxiliary switch will have additional loss from the complex energy transfer. Thus in this section, the switching loss is calculated from simulation under non-ideal scenario.

First, the current through auxiliary switch are still similar to sine waveform, and for a pure sine wave, as shown in Figure 3.4 [https://www.electronics-tutorials.ws/accircuits/average-voltage.html], the average value is $Vpk \times 2/\pi$, where Vpk is the peak value of the sinewave.

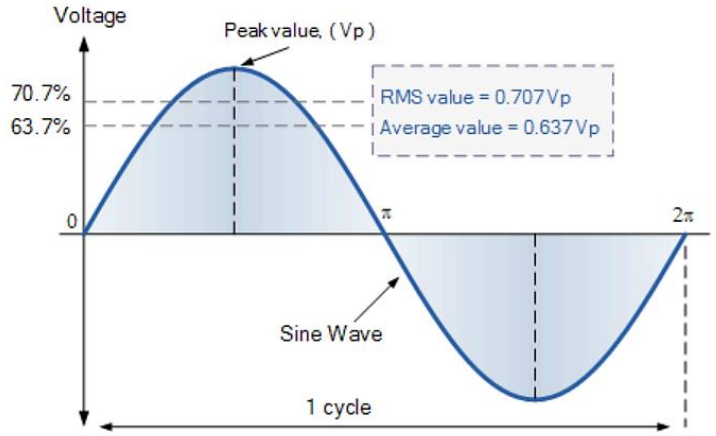


Figure 3.4. RMS and Average Value for Sine Wave.

So for the switching loss, calculate the switching energy at average point to have a more accurate estimation.

Next, calculate the overlapping area of auxiliary switch Vds and current to obtain turn-on and turn-off loss, as shown in Figure 3.5 and Figure 3.6.

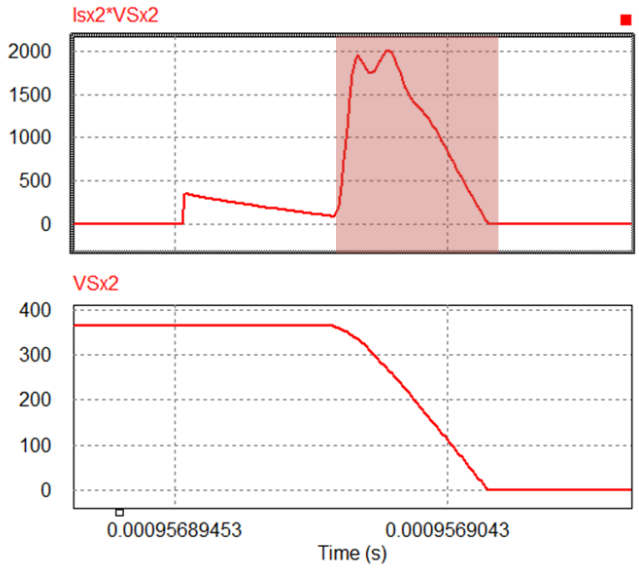


Figure 3.5. Turn-on Switching Loss Estimation.

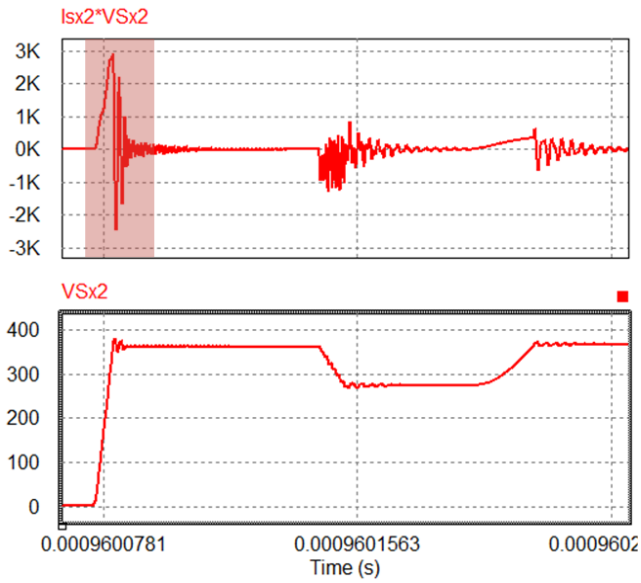


Figure 3.6. Turn-off Switching Loss Estimation.

From the power loss area in red window, turn-on loss for each auxiliary switch is 0.54W, and the turn-off loss for each auxiliary switch is 1.127W. The voltage division introduced more turn-off switching loss to the auxiliary switches.

The conduction loss for all 4 auxiliary switches is calculated from rms current which is 2.74A and the estimated R_{dson} (32.5mΩ) at operating temperature (50℃), also the auxiliary gating optimization decreases the conduction loss, as shown in equation 3.9.

$$P_{cond} = 2 \times I_{rms}^2 \times R_{dson} = 2 \times 2.74^2 \times 37.5m \times \frac{16.67 - 7.5}{16.67} = 0.134W \qquad 3.9$$

3.5.2 Auxiliary Diode Selection and Loss Analysis

The auxiliary diodes also need to handle large current spike since they are in series with L_{res}, so the SiC Schottky diode STPSC08H065 is selected for this prototype which can tolerant 33A of repetitive peak forward current.

From section 2.2, taking leg A for example, auxiliary diodes $D_{x1}$and D_{x2} are conducting during the corresponding auxiliary switch (Q_{x2}/Q_{x1}) turn-off, and D_{x3}/D_{x4} are conducting during the whole resonant period in negative/positive half cycle. The rms current of different diode sets are summarized in Table 3.6.

Table 3.6. Auxiliary Diode rms Current.

Auxiliary Diode	Dx1, Dx2	Dx3, Dx4
rms current (A)	0.4	1.44

Forward voltage drop can be obtained from datasheet. The total conduction loss for 8 auxiliary diode is calculated in 3.10.

$$P_{cond} = V_F \times I_F = 0.55V \times 0.4A \times 4 + 0.8V \times 1.44A \times 4 = 5.48W \qquad 3.10$$

Due to the existence of junction capacitor in real device, total reverse recovery loss for auxiliary diode is calculated in 3.11. Auxiliary gating optimization is also reflected in the equation.

$$P_{rr} = 4 \times \frac{16.67 - 7.5}{16.67} \times \frac{1}{2} \times C_{oss} \times V_{ds}^2 \times f_{sw} = 0.33W \qquad 3.11$$

3.6 **Output Filter Design Tradeoff**

LC low pass filter is used to regulate the output voltage to a sine waveform and filter out the switching frequency and higher order harmonics.

In the pursuit of higher power density, inductor size and loss are major concern. A larger capacitor and smaller inductor is always desirable, but it will increase the current ripple and resulting discontinuity under light load conditions and higher conduction loss for the

semiconductor devices, higher core loss for inductors as well. Vice versa, a larger inductor will increase the size and cost of the inverter thus power density is sacrificed.

The importance of lower current ripple comes to the first, so the desired inductance is determined by inductor current ripple limited within 20% of load current. The calculation is shown in equation 3.12.

$$L = \frac{V_o \times (V_{in} - V_o)}{V_{in} \times 20\% \times I_{load} \times f_{sw}} = \frac{240 \times 125}{365 \times 0.2 \times 12 \times 60k} = 570uH \qquad 3.12$$

In this prototype, 240uH output inductance for each half-bridge leg is determined. Under this condition, there is a tradeoff between inductor core loss (P_{Fe}) and winding loss (P_{Cu}). Smaller core will have less P_{Fe}, but in order to obtain enough inductance, inductor turns ratio would be larger, thus increases inductor DCR, which will lead to larger P_{Cu}.

After balancing P_{Fe} and P_{Cu} while still maintaining decent output current ripple filtering effect, the output inductor used in this prototype under bipolar modulation is shown in Figure 3.7.

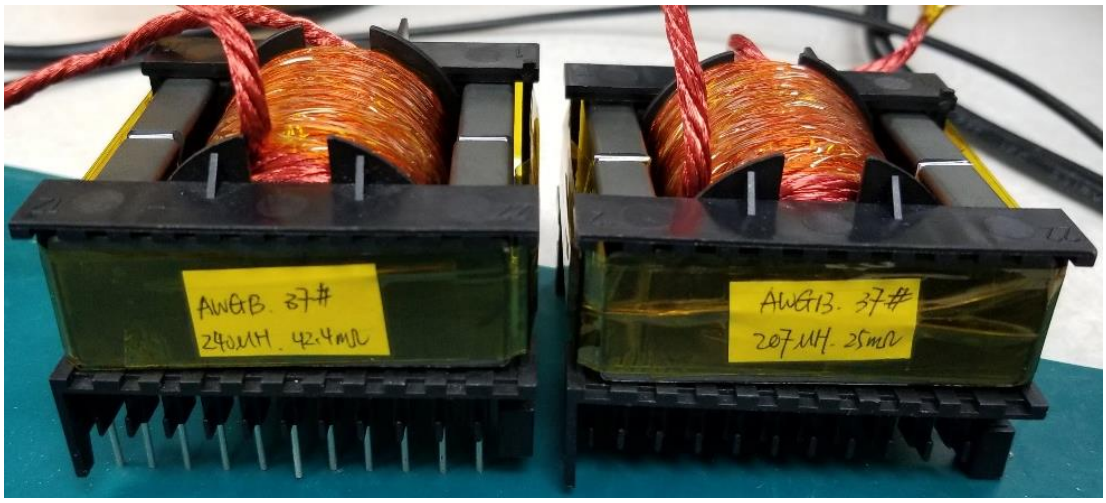


Figure 3.7. Prototype Output Inductor.

Inductor core selection and the parameters of LC filter are summarized in Table 3.7 below.

Table 3.7. Output Filter Specifications.

Parameter	Value
Capacitance	4.7uF
Inductance	240uH in 3C94 ETD54 core
Litz wire	AWG13
Turns ratio	37
DCR	23.34mΩ

3.6.1 Output Inductor Loss Analysis

The total inductance split into two inductors (L_{o1} and L_{o2}) connected to the middle point of each half bridge leg. The total core loss (P_{Fe}) for two $L_{o1,2}$ is calculated from equation 3.13. P_{CV} is the core power loss of material 3C94 at estimated flux density, which is obtained in Figure 3.8, l_e and A_e are the effective length and area of the ETD54 core. The winding loss is calculated from equation 3.14 and 3.15, where litz wire DCR is calculated from the resistance/length of AWG13, which is 6.571mΩ/m, average length per turn of ETD54 core, which is 96mm, and the turns number of $L_{o1,2}$. P_{Cu} is the winding loss of $L_{o1,2}$, I_{rms} is the rms current through $L_{o1,2}$.

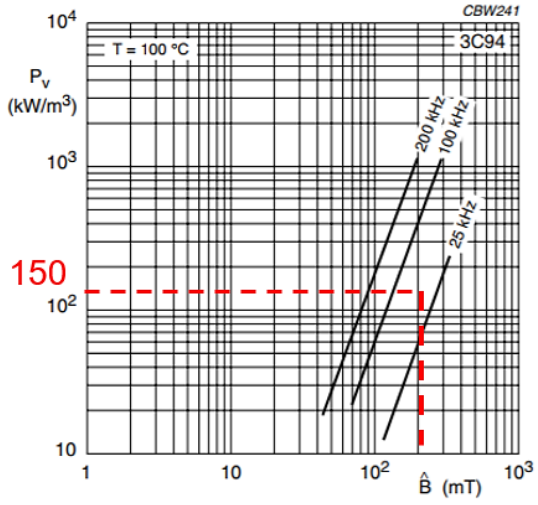


Figure 3.8. Inductor Core Power Loss.

$$P_{Fe} = 2 \times P_{CV} \times l_e \times A_e = 2 \times 150k \times 10^{-9} \times 127mm \times 280mm^2 = 10.67W \qquad 3.13$$

DCR = Resistance per length × Average length per turn × number of turns

$$= 6.571m \times 37 \times 96 \times 10^{-3} = 23.34m\Omega \qquad 3.14$$

$$P_{Cu} = 2 \times I_{rms}^2 \times DCR = 2 \times 9.1^2 \times 23.34 \times 10^{-3} = 3.87W \qquad 3.15$$

4 Experimental Results and Summary

4.1 Prototype Design Summary

A 2kW prototype with 365V nominal DC voltage and 240V ac output was constructed to verify the inverter operation. Switching frequency is 60 kHz. The detailed prototype specifications and power stage parameters are shown in Table 4.1 and Table 4.2 respectively.

With the components shown in Table 4.1, a PCB board is designed and built to test and verify the inverter. The PCB board is manufactured in four layers with 3 ounce of copper for better current and power handling capability. Traces that have large current going though such as DC bus and ground are given larger trace area to handle high power. Texas Instrument's TMS320F28069 Digital Signal Processor (DSP) is used for gate controlling implementation and sensor processing. Designed PCB layout is shown in Figure 4.1.

Table 4.1. Hardware Prototype Specification

Parameter	**Value**
Input DC Voltage	365 $V_{nominal}$
Output AC Voltage	240 V_{rms}
Output Frequency	60 Hz
System Power Level	2 kW

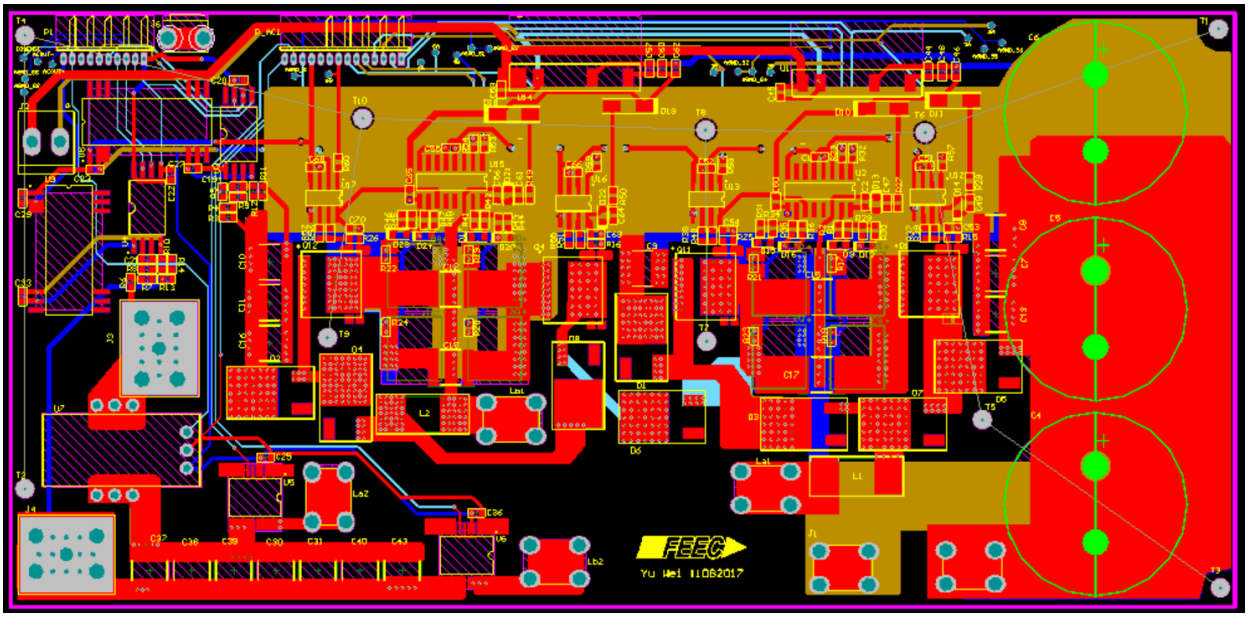


Figure 4.1. Proposed Inverter PCB Layout.

Table 4.2. Power Stage Parameter.

Switching Frequency	60 kHz
Main Switch	GaN System GS66516T
Auxiliary Switch	GaN System GS66516B
Auxiliary Diode	ST STPSC8H065
Auxiliary Inductor	1.46uH 3C94 RM6 Core
Output Inductor	240uH 3C94 ETD54 Core

4.1.1 Power Density

Although auxiliary circuitry introduces additional switches, diodes and auxiliary inductors, the profile of auxiliary active components are well selected, and the size of auxiliary inductors are optimized as well. DSP PCB board, current sensor are all 1” in height. Auxiliary inductors are small enough to directly mount on top of the PCB board. The assembled testing prototype is shown in Figure 4.2. With a very compact layout to further push to high power density, after

laying down the input electrolytic capacitors, the dimensions of proposed inverter prototype are 3.3” in width, 6.77” in length, and 1.18” in height. Now this prototype can reach to 2.14kW, which leads to a power density of 81.87 W/inch^3.

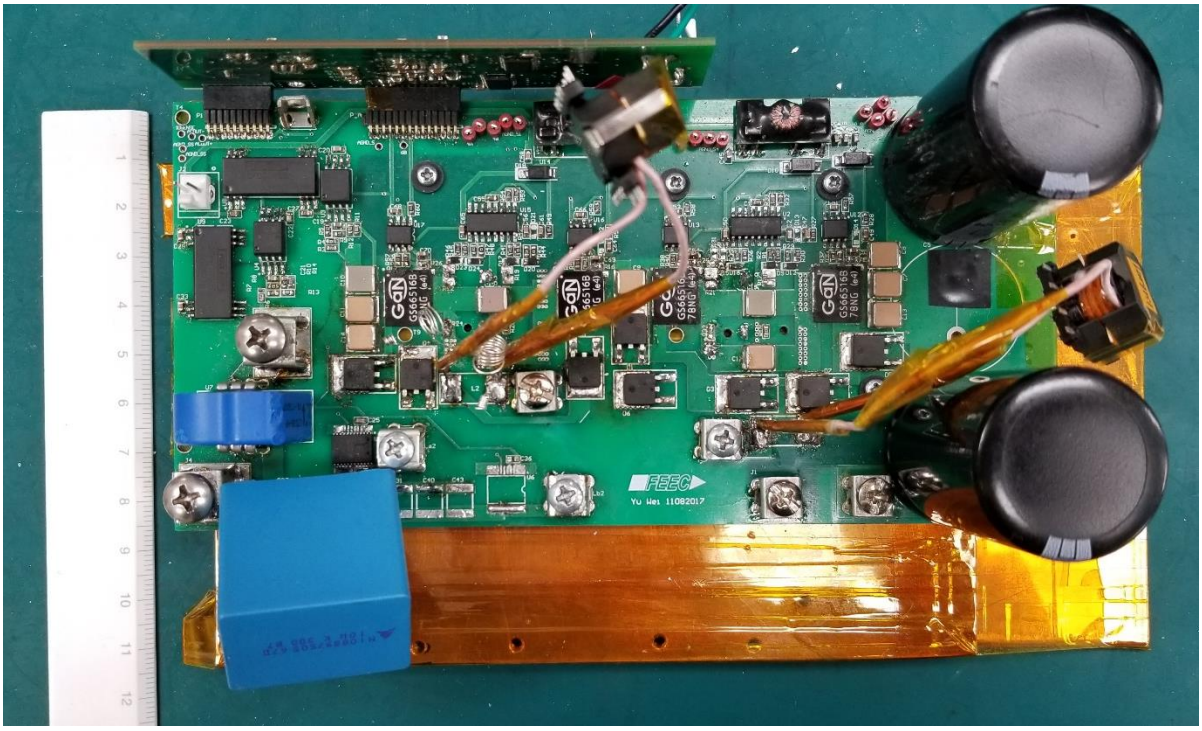


Figure 4.2. Proposed Inverter assembled PCB for Testing.

4.1.2 Main Switch Soft-Switching Achieved

The steady state waveforms of proposed inverter operating at 240V with 2kW are shown in Figure 4.3 to Figure 4.6. Soft-switching (ZVS turn-on) for full-bridge main switches are verified under full power condition. In the figures, yellow is the drain-source voltage (V_{ds}) of full-bridge low-side main switch, red is inverter output voltage (Vo), green is the auxiliary inductor current (I_{aux}), and blue is the output inductor current (I_L).

Figure 4.3 indicates that ZVS turn-on for main switches is achieved through whole fundamental cycle. Figure 4.4, Figure 4.5 and Figure 4.6 show that ZVS turn-on for main switches are fulfilled at zero-crossing, positive and negative peak I_L respectively. Since I_{aux} is larger than I_L

and the excessive current discharged main switches parasitic capacitor to let main switch body diodes conducted before the switches turning-on, as shown in V_{ds} waveform.

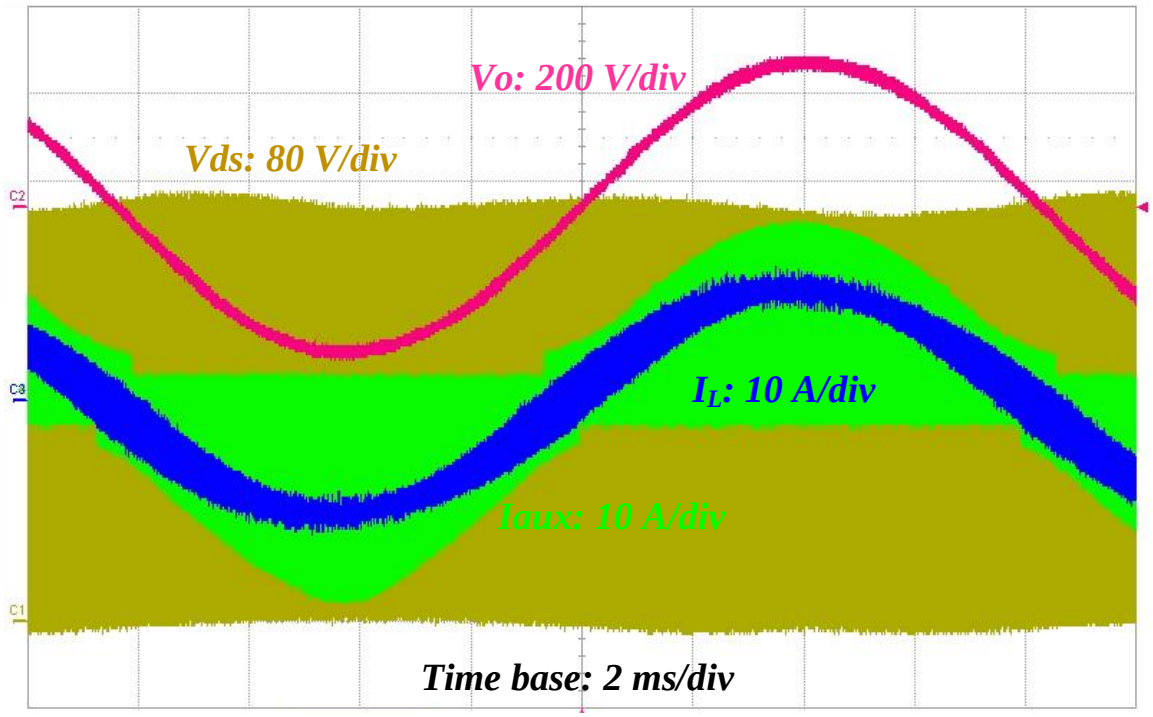


Figure 4.3. Main Switch ZVS Turn-on Achieved Through Whole 60Hz Sine Cycle.

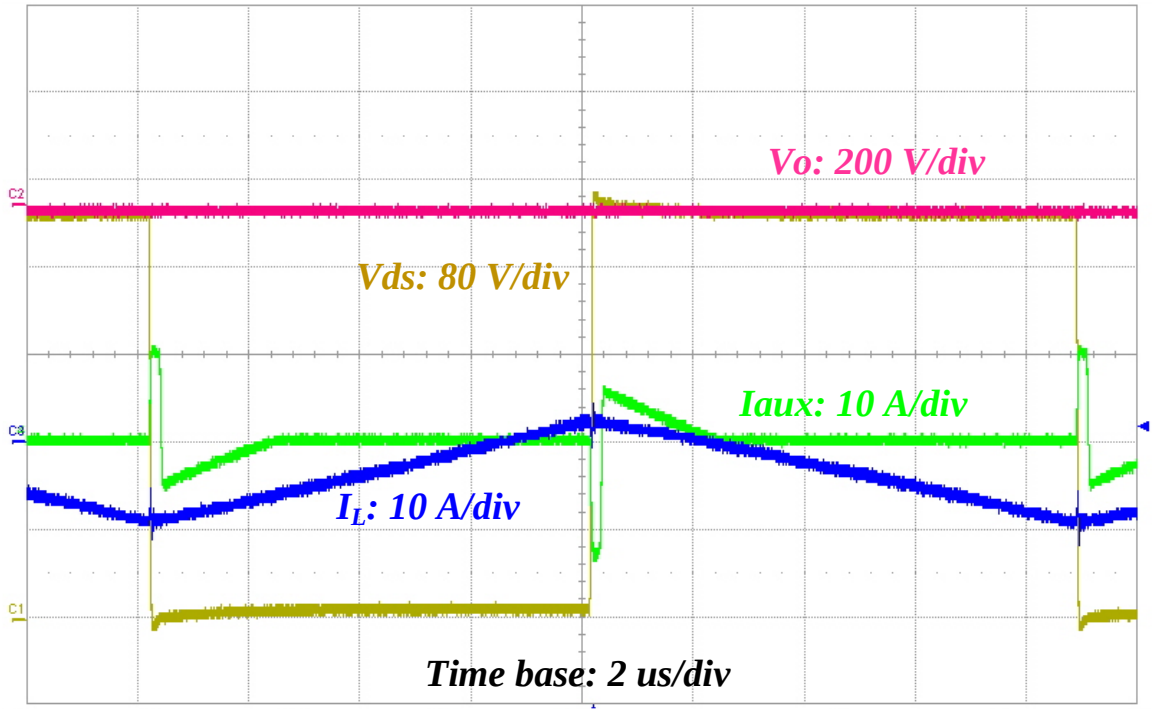


Figure 4.4. Main Switch ZVS Turn-on Achieved at Zero-crossing.

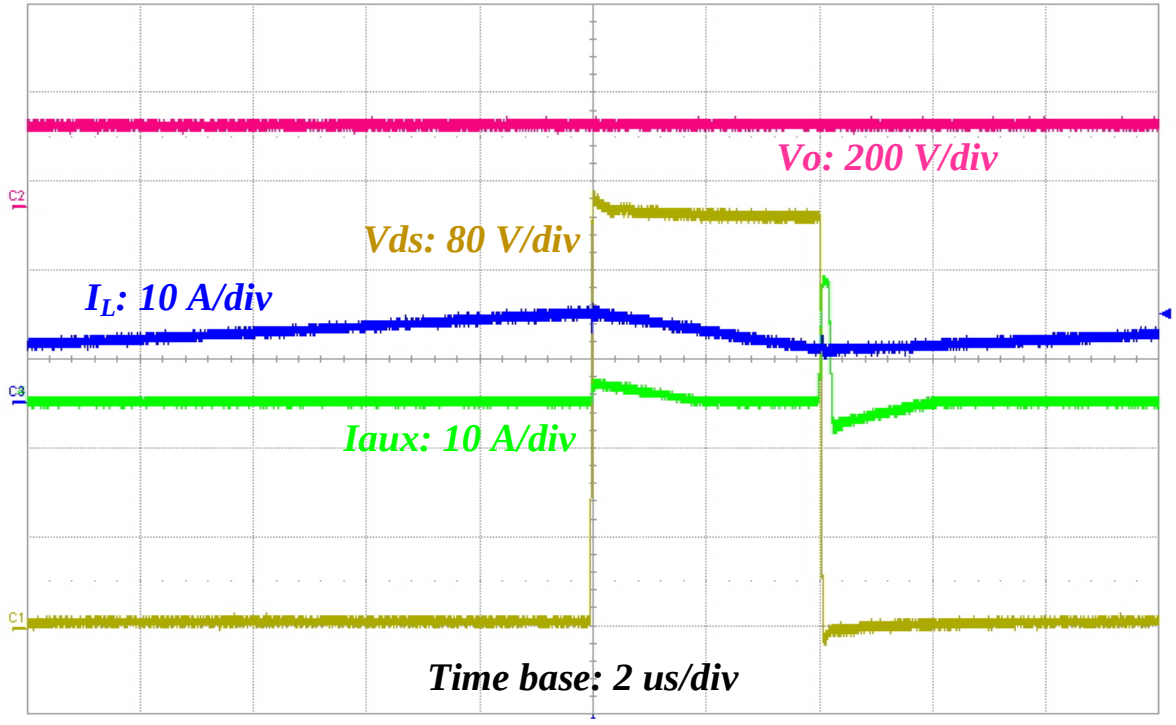


Figure 4.5. Main Switch ZVS Turn-on Achieved at Positive Peak Output Current.

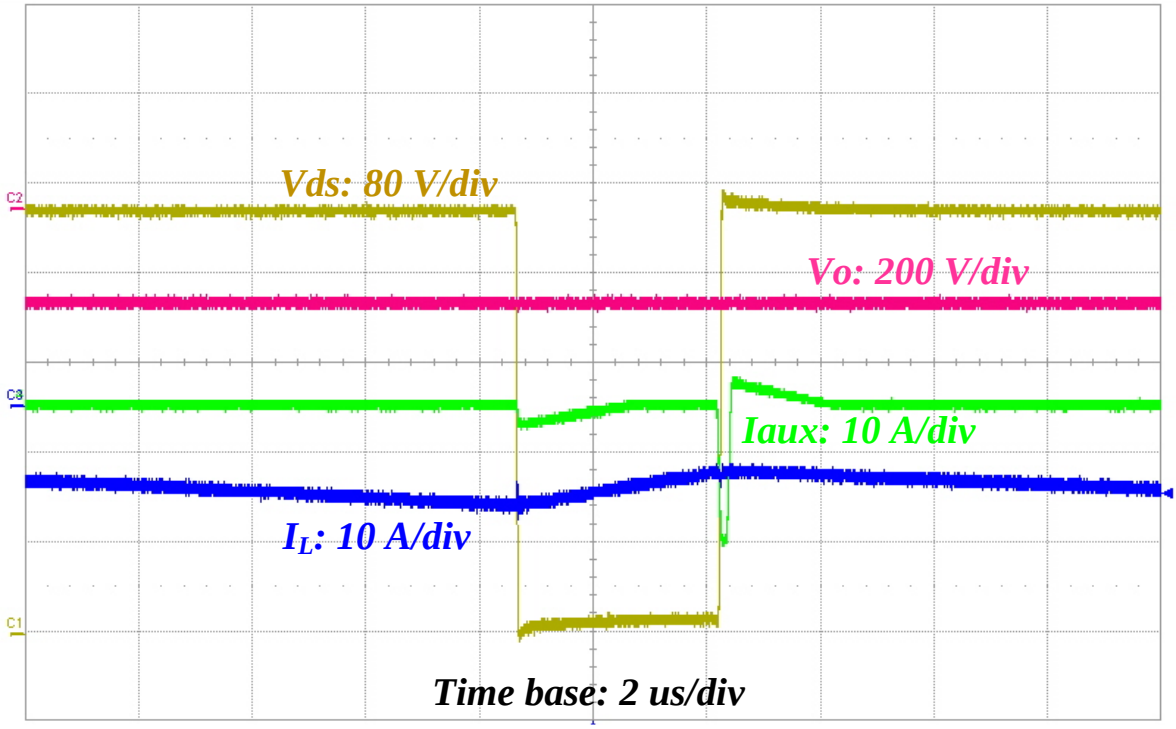


Figure 4.6. Main Switch ZVS Turn-on Achieved at Negative Peak Output Current.

4.1.3 Voltage Divider Phenomenon Verified

Voltage Divider Phenomenon discussed in section 2.3 is also verified. The steady state waveforms of proposed inverter operating at 240V with 2kW are shown in Figure 4.7Figure 4.3 and Figure 4.8. In the figures, yellow is the drain-source voltage (V_{ds_aux}) of proposed inverter low-side auxiliary switch, red is the drain-source voltage (V_{ds_main}) of proposed inverter low-side main switch, green is the auxiliary inductor current (I_{aux}), and blue is the output inductor current (I_L).

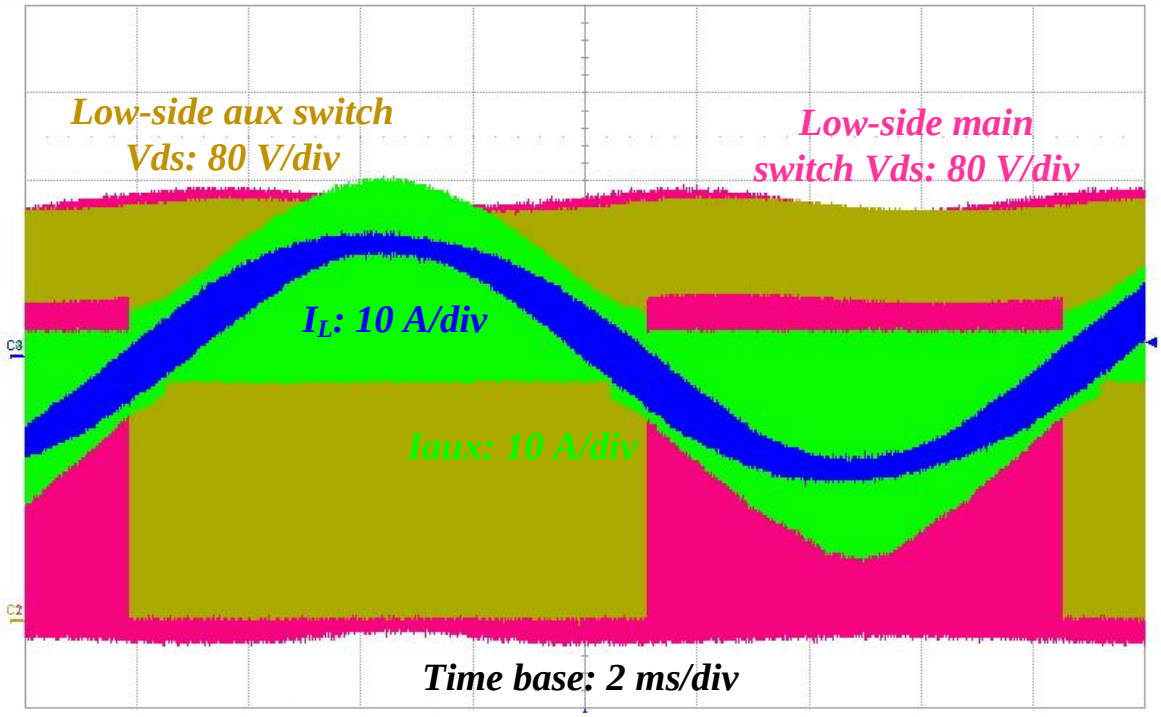


Figure 4.7. Voltage Divider Phenomenon in Whole Fundamental Cycle.

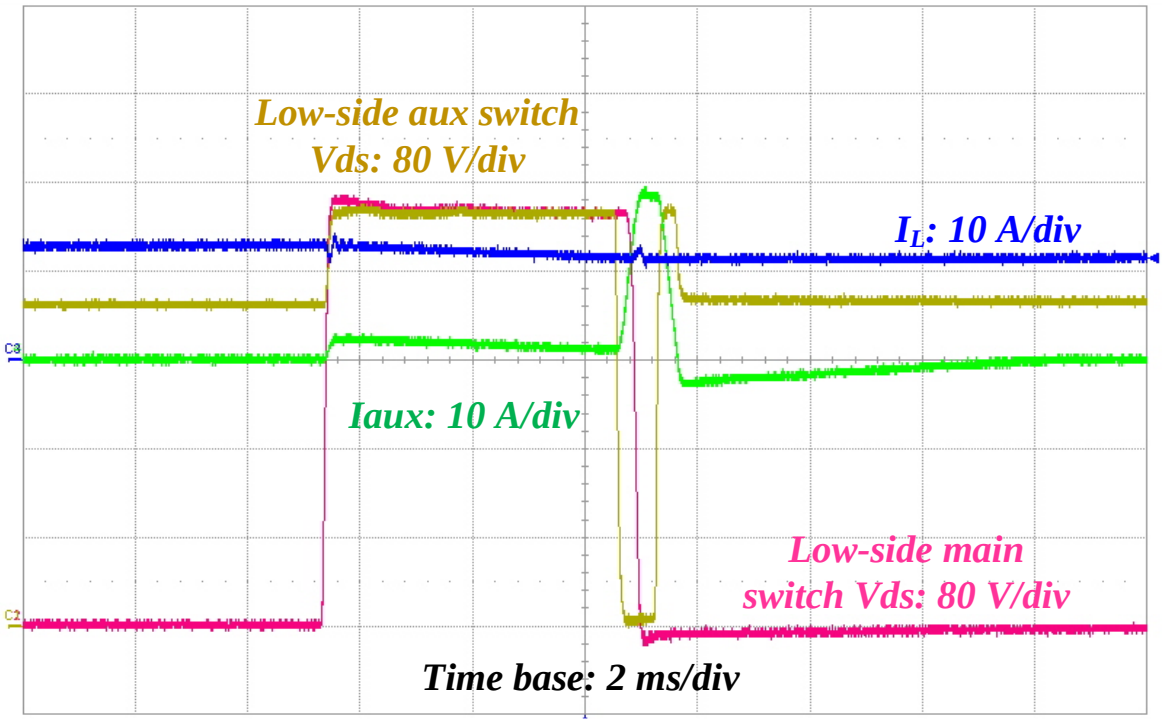


Figure 4.8. Voltage Divider Phenomenon in Each Fundamental Cycle.

4.1.4 Auxiliary Switch Gating Optimization

Auxiliary gating optimization analyzed and simulated in section 2.4 is achieved. The optimization is approved to reduce stress on auxiliary switches to obtain better thermal performance and enable the inverter system to a higher overall efficiency.

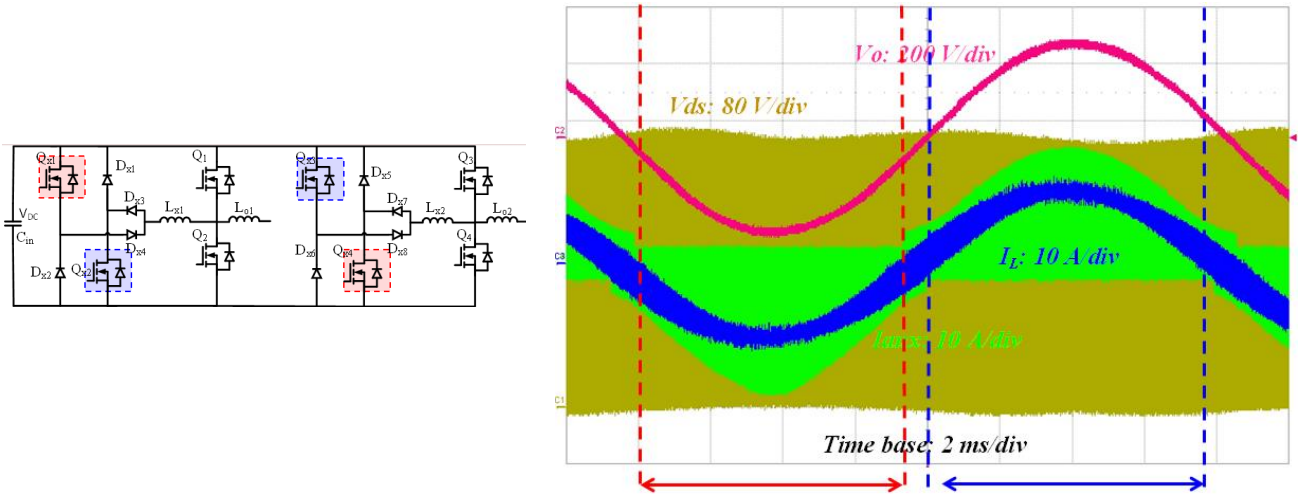


Figure 4.9. Auxiliary Gating Optimization in Whole Fundamental Cycle.

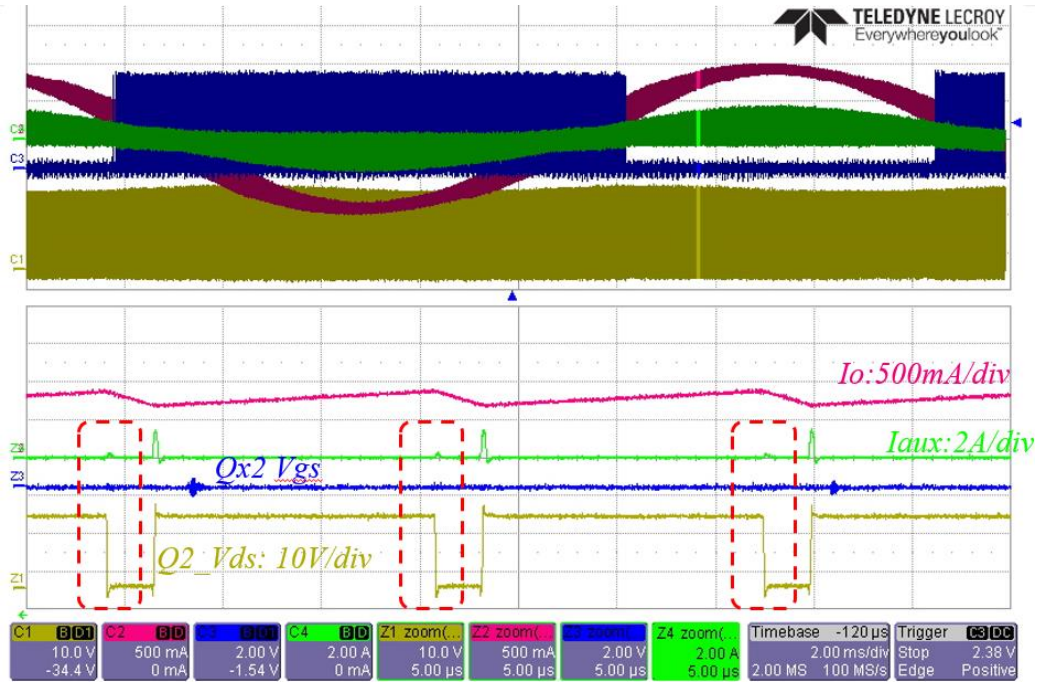
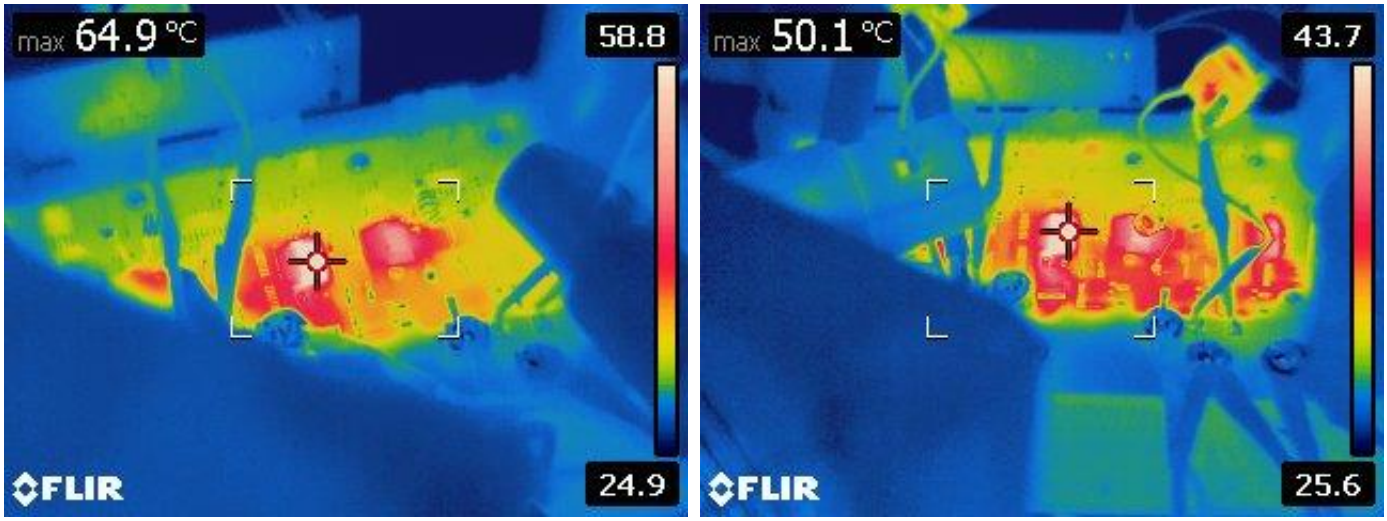


Figure 4.10. Q_2 ZVS Achieved without Auxiliary Switch Q_{x2}.

As shown in Figure 4.9, in red window, Qx1, Qx4 turn off during negative half fundamental cycle. In blue window, Qx2, Qx3 turn off during positive half fundamental cycle. And all main switches still maintain ZVS turn-on.

Zoom in waveform shown in Figure 4.10. Blue waveform is auxiliary switch Qx2 gate signal, green is auxiliary inductor current, and yellow waveform is main switch Q2 drain-source voltage. From gate signal that Qx2 is constantly off, no auxiliary current exists, and Q2 still has ZVS turn-on showing in yellow waveform.



a. Auxiliary Switch Temperature Before Optimization

b. Auxiliary Switch Temperature After Optimization

Figure 4.11. Thermal Performance Improved by Optimization.

In Figure 4.11, temperature rise on auxiliary switch is reduced by 15℃ after the gating optimization, which helps reduce loss on the switch and push to a higher system efficiency as well as higher system power rating.

The temperature of main switches and auxiliary diodes are too cool to be captured, which means the thermal performance of proposed inverter system is well organized and optimized.

4.2 **Inverter Bipolar Modulation FFT analysis**

The EMI performance of proposed inverter is carried out by measuring and differencing the middle point voltages of each full-bridge leg, which are Va and Vb respectively in Figure 4.12. Since inverter EMI performance is not fully determined by input dc voltage and load current, the following results are carried out under 250Vdc input condition to have a better view in oscilloscope screen to illustrate.

Common mode (CM) noise can be evaluated from the sum of Va and Vb as shown in Figure 4.13. Differential mode (DM) noise can be evaluated from the subtraction of Va and Vb as shown in Figure 4.14.

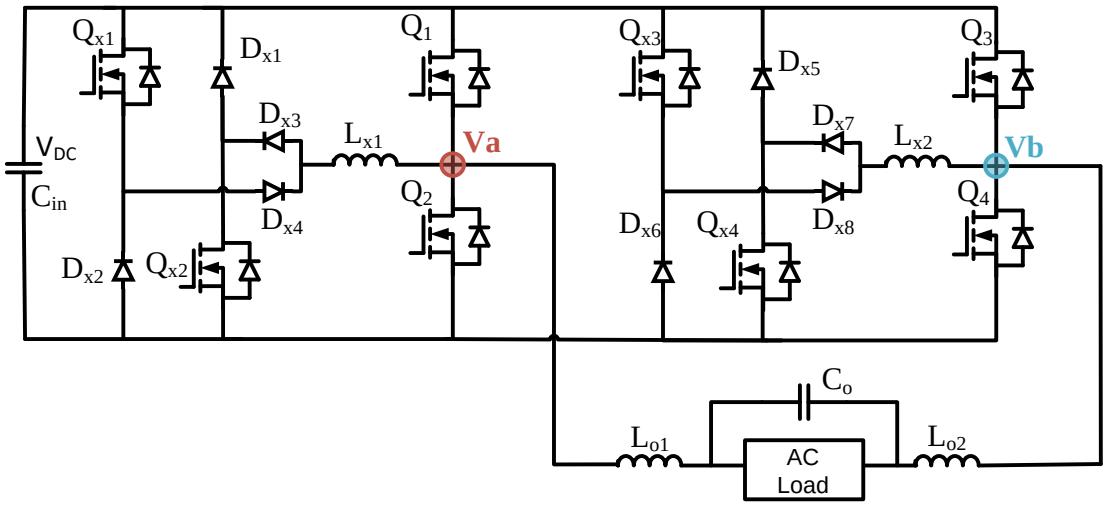


Figure 4.12. Voltage Measurement Point for Harmonic Analysis.

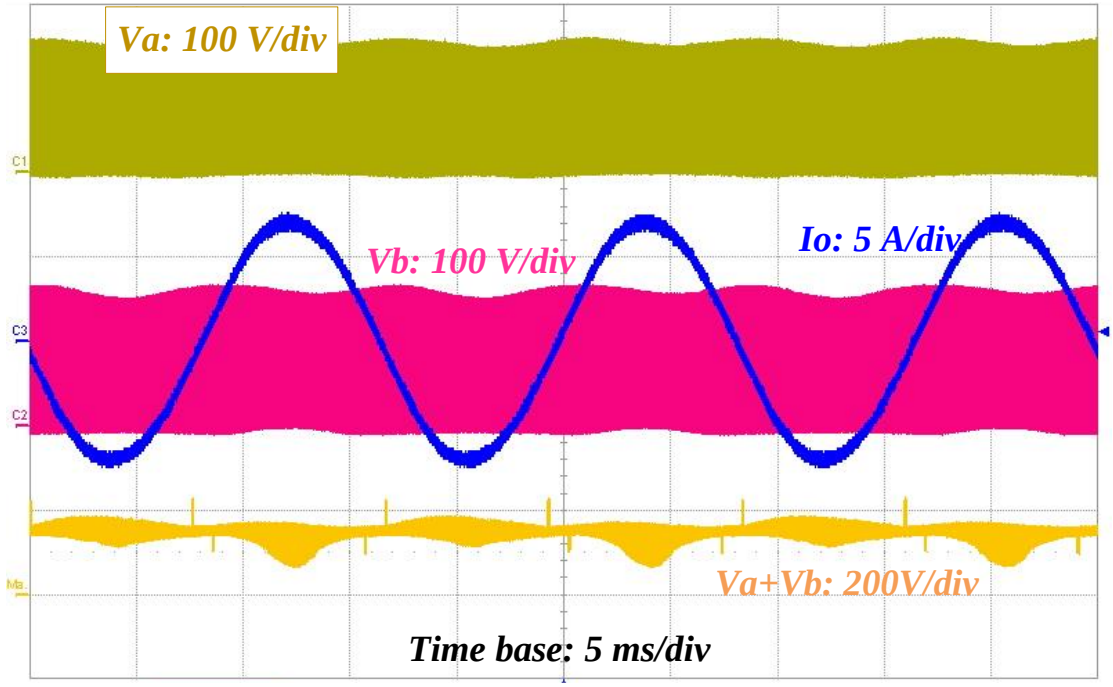


Figure 4.13. Inverter Common Mode Waveform.

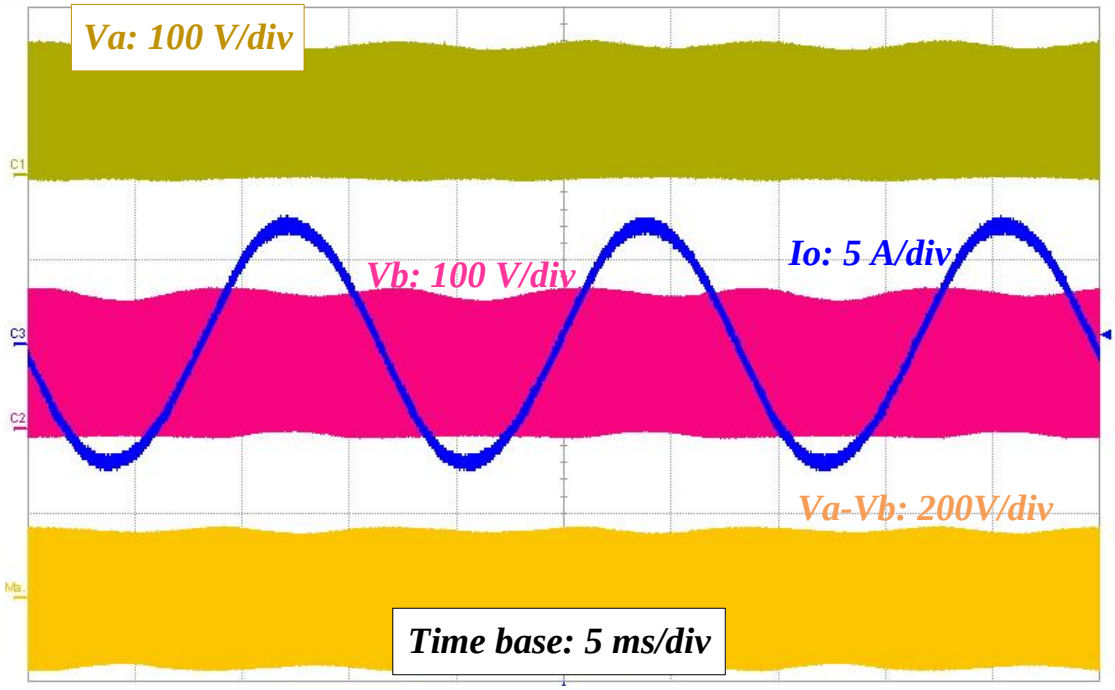


Figure 4.14. Inverter Differential Mode Waveform.

4.3 System Level Efficiency and Loss Breakdown

The efficiency of proposed inverter is carried out at nominal input dc and output ac voltage, with different output power levels, which is shown in Figure 4.15. These loss measurements consist of all system loss including control, sensing, and other auxiliary loss. The inverter's peak efficiency is 98.76 % and the CEC efficiency at the nominal 365 Vdc input is 98.36 %.

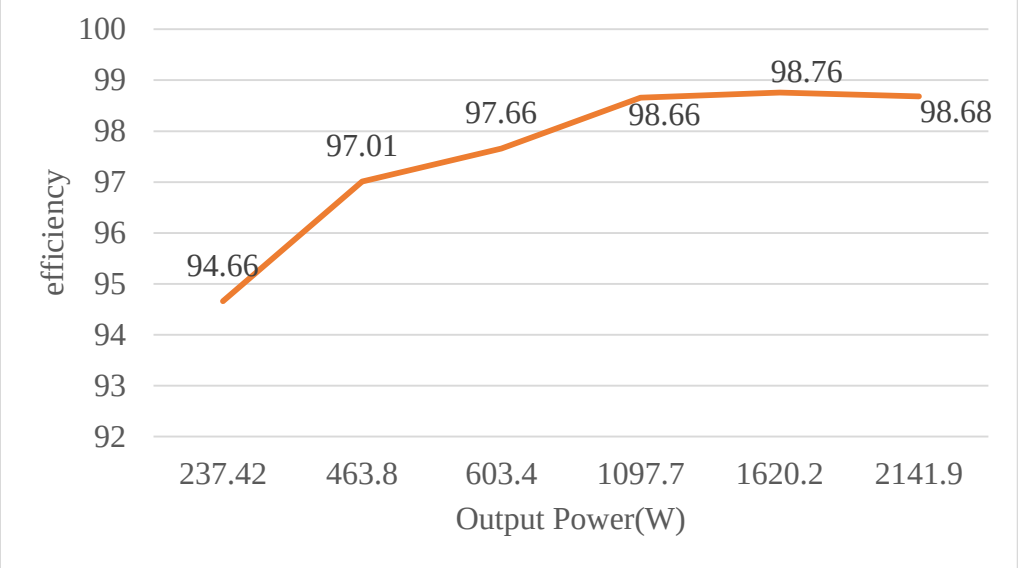


Figure 4.15. Measured Inverter Efficiency.

4.3.1 Loss Breakdown Analysis

Loss breakdown for major devices and components are carried out separately in section 3. Here presents the summary in Table 4.3 and analysis in Figure 4.16 for proposed inverter operating at full power (2.14kW) with system overall efficiency at 98.68%. Output inductor core loss and main switch conduction loss are the dominating factors.

Table 4.3. Inverter Loss Breakdown Analysis.

Main Switch Switching Loss (P_{Q,sw_off})	$P_{Q,sw\_off} = E_{off} \times \frac{I_{off\_avg}}{20} \times f_{sw}$

Main Switch Conduction Loss ($P_{Q,cond}$)	$P_{Q,cond} = I_{Q,rms}^2 \times R_{ds(on)}$
Auxiliary Switch Switching Loss ($P_{Qx,sw}$)	$P_{Qx,sw\_on} = \frac{1}{2} \times C_{oss} \times V_{ds}^2 \times f_{sw}$
	$P_{Qx,sw\_off} = E_{off,new} \times \frac{I_{off\_avg}}{20} \times f_{sw}$
Auxiliary Switch Conduction Loss ($P_{Qx,cond}$)	$P_{Qx,cond} = I_{Qx,rms}^2 \times R_{ds(on)}$
Auxiliary Diode Reverse Recovery Loss ($P_{D,rr}$)	$P_{D,rr} = \frac{1}{2} \times C_{oss} \times V_{ds}^2 \times f_{sw}$
Auxiliary Diode Conduction Loss ($P_{D,cond}$)	$P_{D,cond} = V_F \times I_F$
Output Inductor Copper Loss (P_{Cu})	$P_{Cu} = I_L^2 \times DCR$
Output Inductor Core Loss (P_{Fe})	$P_{CV} = k_{CV} f^{k_f} (\frac{\Delta B_{p-p}}{2})^{k_b}$ $P_{Fe} = P_{CV} \times l_e \times A_e$

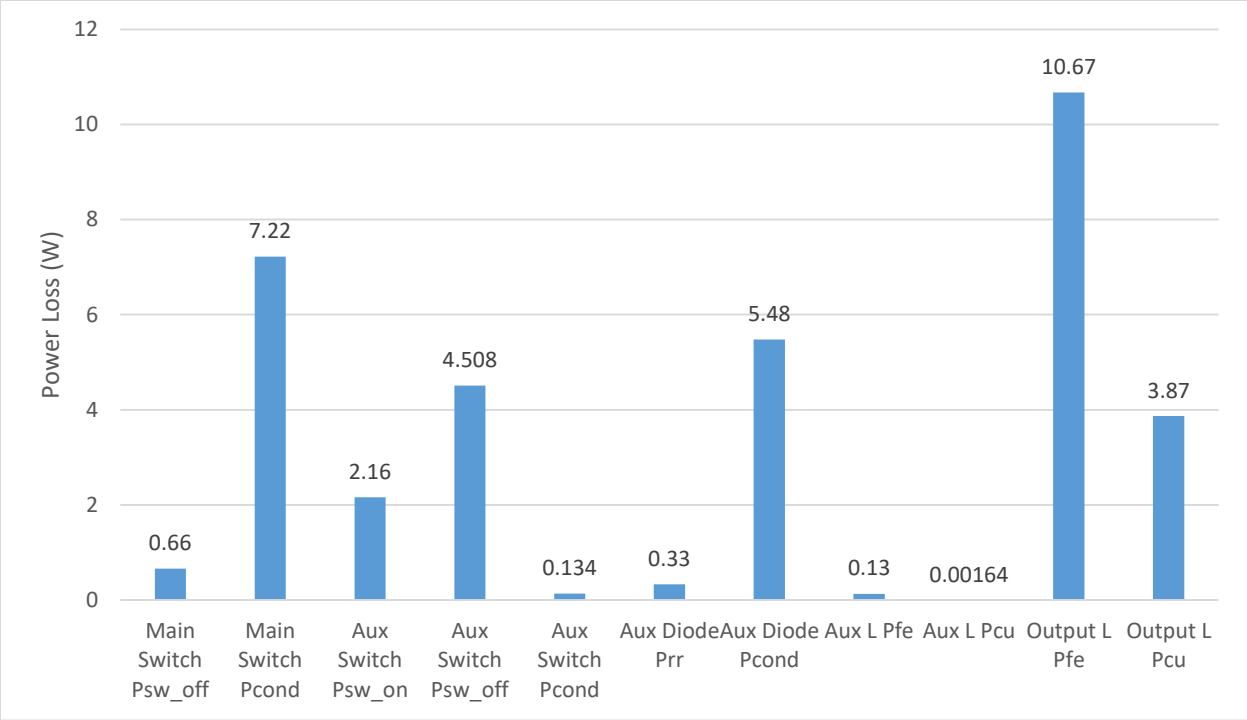


Figure 4.16. Proposed Inverter Loss Breakdown.

5 Conclusions and Future Work

5.1 Conclusions

This thesis studied a novel resonant snubber based dc-ac inverter using wide bandgap devices which can be served as EV on-board charger, solar string inverter, stationary distribution, UPS, etc. The main contents are listed as following.

A traditional full-bridge inverter combined with a novel auxiliary resonant snubber to achieve high efficiency, high power density, and easier EMI filter design was proposed. Decision making procedure for selecting soft-switching architecture was illustrated. Resonant snubber circuitry operations were analyzed. Gating optimization for auxiliary circuitry enabled inverter system to reach high efficiency and power density. The proposed topology with modulation can achieve ZVS turn-on for full-bridge main switches and ZCS turn-off for auxiliary diodes in resonant snubber circuitry. The hardware prototype demonstrated 98.76% peak efficiency and 98.36% weighted CEC efficiency including all auxiliary and control power under 365Vdc input condition. The power density of 75.87W/inch^3 is achieved at 2kW output power condition.

5.2 Future Work

Additional work could be performed on main switch gating optimization and PCB layout to further improve inverter prototype overall efficiency as well as noise immunity.

1. Deadtime can be adjustable by sensing input dc voltage rather than a fix value.
2. Thermal performance can be optimized by changing auxiliary switch to top-cooled package.

3. Independent gate driver power supply for each main switch for steady gate voltage supplement.
4. Parasitic inductance can be reduced during layout procedure, to enable hard-switching and unipolar modulation capability, since one of the full-bridge leg is more sensitive to switching noise. The gating noise that trigger main switch almost false turn-off is illustrated below.

   In Figure 5.1, after switching to unipolar modulation, under 1.6kW, 365Vdc input condition, ripple current appeared in auxiliary and output inductor.

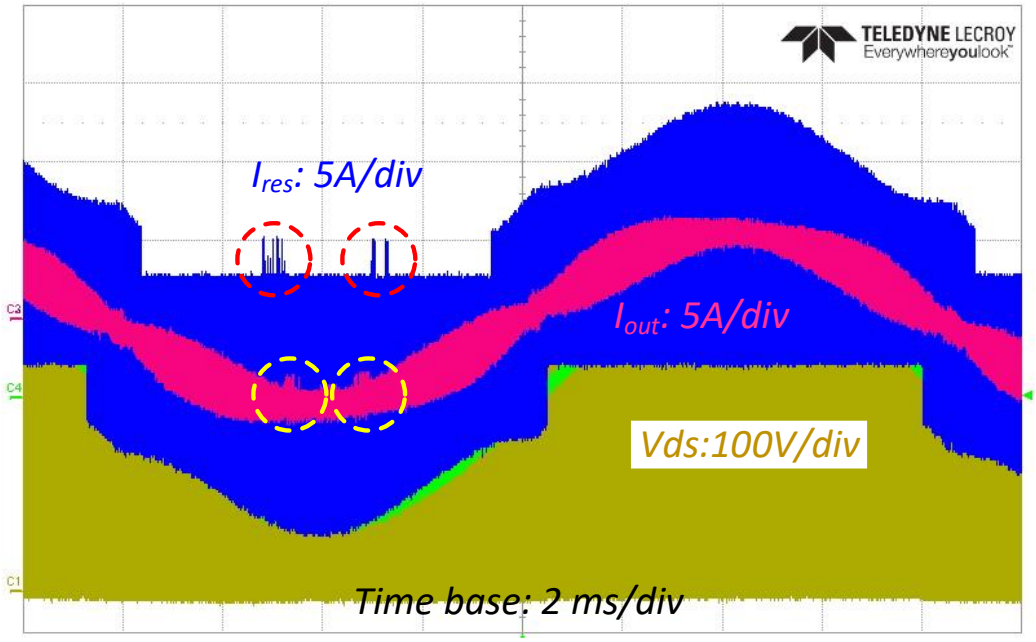


Figure 5.1. Current ripple in auxiliary and output inductor.

After zooming in the area with noisy spikes, as indicated in the red windows in Figure 5.2, it can be seen that the low side main switch of one leg is partially turned-off, which infers that the upper device is turned on, thus introducing a partially shoot-through current and glitches in inductors. This partially shoot-through current leads to more conduction loss as well as more switching loss, which causes the system overall efficiency worsened as compared to the bipolar modulation method. It also prevented the

circuit to operate at higher power levels due to higher shoot-through level and potential device failure.

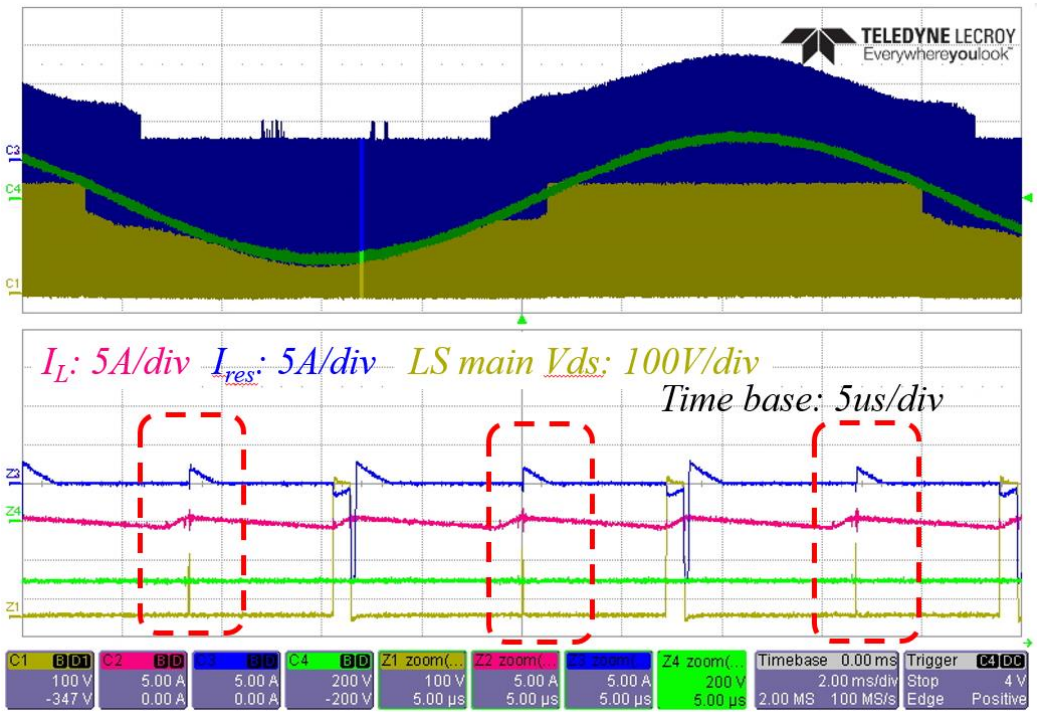


Figure 5.2. Main switch false turn-off introducing ripple current.

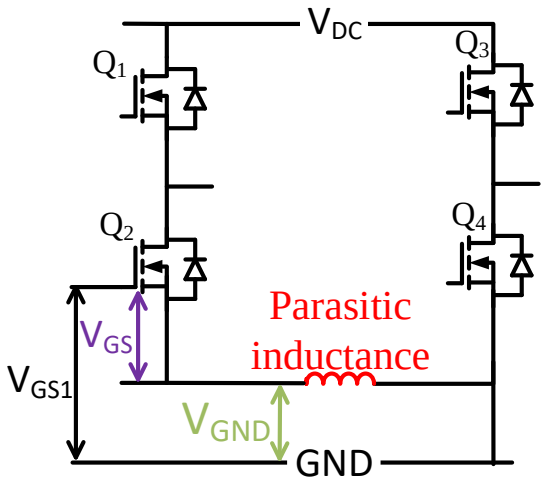


Figure 5.3. Parasitic inductance in PCB layout.

The cause for this problem is shown in Figure 5.3. V_{GS1} is the gate voltage from gate driver power supple, V_{GND} is the voltage drop on parasitic inductance, and V_{GS} is the actual gate voltage that controls the switch. There is parasitic inductance between the low

side main switches (Q_2 and Q_4). Although the inductance is small, due to GaN switch high di/dt, the voltage drop (V_{GND}) on parasitic inductance is not negligible. Thus, V_{GS} is too small to support Q_2 function normally, which causes Q_2 almost false turn-off during operating.

This problem can only be solved by redesigning the gate driver power supply structure by adding individual gate driver power supply IC to each main switch gate driver to have independent power supply ability. Besides, the board can be re-layout to reduce the parasitic inductance as well as the noise immunity of the inverter system.

6 Reference

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