5. CONTROL OF ZERO-SEQUENCE CURRENT IN PARALLEL THREE-PHASE CURRENT-UNIDIRECTIONAL CONVERTERS

5.1 A NOVEL ZERO-SEQUENCE CURRENT CONTROL

5.1.1 Zero-Sequence Dynamics

The parallel buck rectifier model in Figure 3.15 and the parallel current source inverter model Figures 3.19 show that the zero-sequence dynamics are governed by their z channels. It is interesting to note that both systems have the same z-channel equivalent circuit except for the current direction. Since

$$\Delta v_z = (v_{p1} + v_{n1}) - (v_{p2} + v_{n2}), \tag{5.1}$$

the zero-sequence current is determined by the difference in their common-mode voltages. For a single converter, the common-mode voltage does not cause any zero-sequence current because physically there is no such current path. The z channel is actually an open circuit. Besides, the common-mode voltage does not affect the converter control objectives, such as voltage regulation and current control. Therefore, the z channel is normally not considered in the control design for a single converter.

When the two converters are in parallel, the zero-sequence current path is formed. A small difference between the two common-mode voltages may cause a large zero-sequence circulating current, because the z channel is an undamped circuit with only the inductors, and their ESRs in practical cases. Figure 5.1 shows the z-channel model of the parallel buck rectifier system. The current direction is counter-clockwise for the parallel current source inverter system.

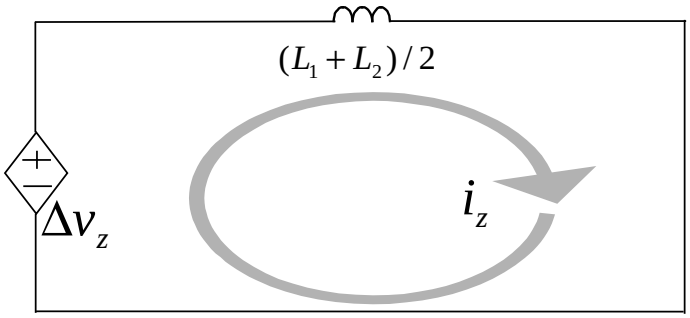
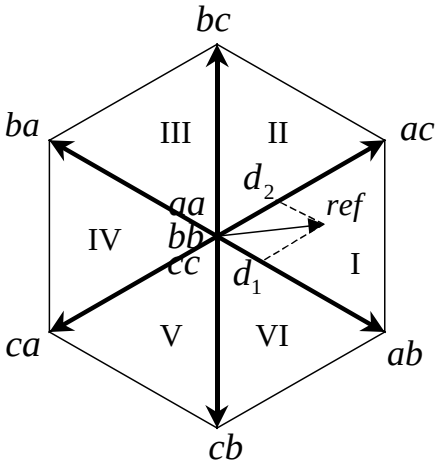


Figure 5.1 Zero-sequence dynamics model of parallel buck rectifiers.

5.1.2 A New Control Variable

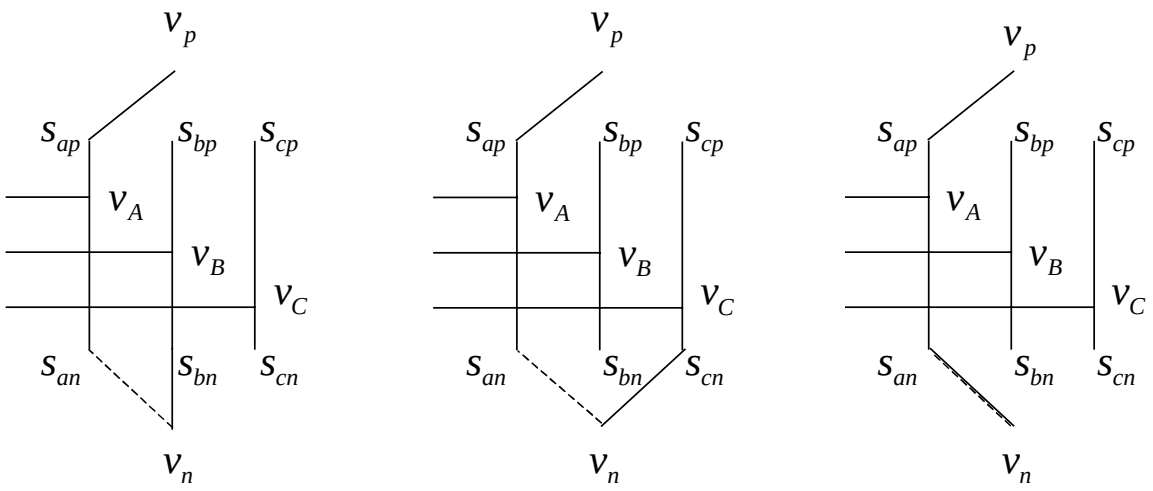
An SVM technique is commonly used in the modulation of the switching network for three-phase current-unidirectional converters. Figure 5.2 shows all the switching vectors [53].



$$d_0 = 1 - d_1 - d_2$$

Figure 5.2 Space-vector modulation in three-phase current-unidirectional converters.

In total, there are six active vectors and three zero vectors at the center point. Assuming the reference vector is in sector I, the switching vectors ab, ac, and one of the zero vectors are used to synthesize the reference vector. Normally, to reduce switching actions, phase A is always connected to both the positive and the negative DC rails. The sequencing of the switching actions is described in Fig. 5.3.



Vector 1(d_1) Vector 2(d_2) Vector 0(d_0)

Figure 5.3 Typical sequence of switching actions in the SVM of buck rectifier.

In sector I, v_A is higher than v_B and v_C. Therefore, even if s_{an} is closed, it is not conducting current until both s_{bn} and s_{cn} are open. In Figure 5.3, d_1 and d_2 are the duty cycles of vector 1 and 2, respectively, and d_0=1-d_1-d_2. The solid line represents an actual connection as well as conduction, while the dashed line means a connection only (no current conduction). s_{ap} and s_{an} are always closed in sector I and IV. s_{bp} and s_{bn} are always closed in sector III and VI. S_{cp} and s_{cn} are always closed in sector II and V.

Figure 5.4 shows a typical PWM pattern based on the sequence in Figure 5.3.

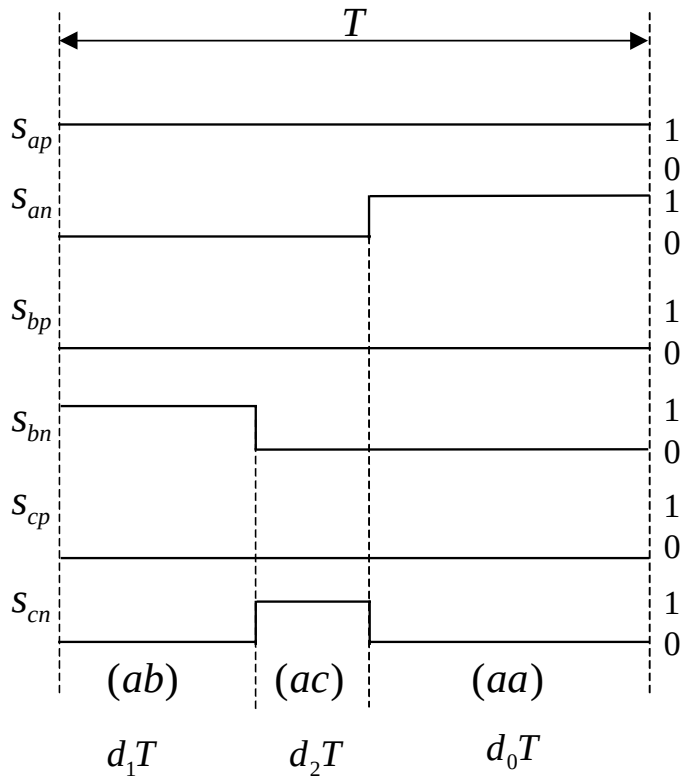


Figure 5.4 Typical SVM in sector I.

With this PWM,

$$v_z = v_p + v_n = (1 + d_0) \cdot v_A + d_1 \cdot v_B + d_2 \cdot v_C . \tag{5.2}$$

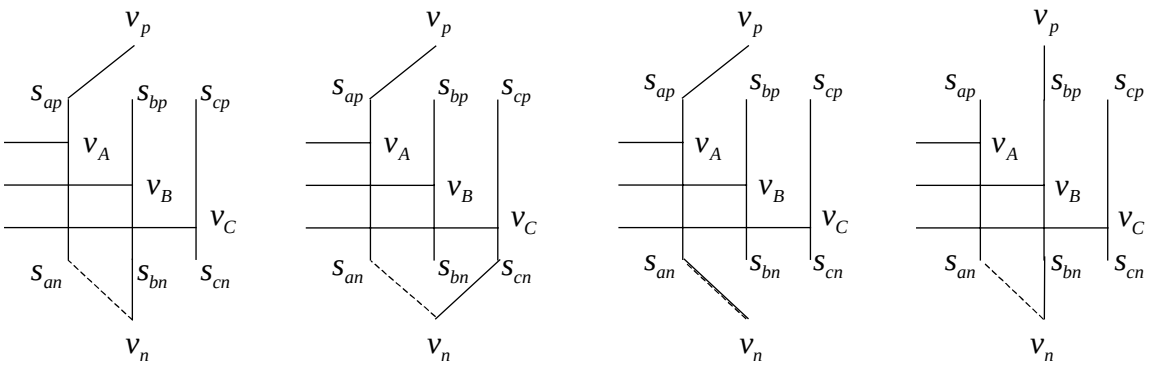
In order to control v_z, the zero vectors should not be fixed. A new control variable can be defined, assuming the reference vector is in sector I:

$$k = d_{aa} . \tag{5.3}$$

The rest of the zero-vector duty cycle will be applied to the zero-vector bb if $v_B > v_C$, or to the zero-vector cc if $v_C > v_B$. Assuming $v_B > v_C$, then

$$d_{bb} = d_0 - k . \tag{5.4}$$

Figure 5.5 shows the sequencing of the switching actions. Figure 5.6 shows the PWM pattern.



Vector 1(d_1) Vector 2(d_2) Vector 0A(k) Vector 0B(d_0-k)

Figure 5.5 Sequence of switching actions with variable zero vectors.

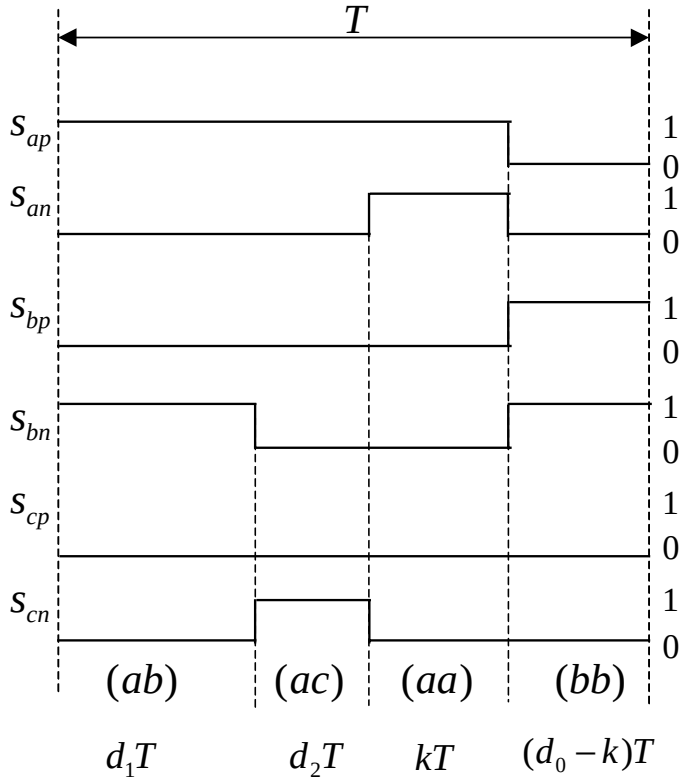


Figure 5.6 SVM in sector I with control variable k.

In this case,

$$v_z = v_p + v_n = (d_1 + d_2 + 2k)\cdot v_A + (d_1 + 2(d_0 - k))\cdot v_B + d_2 \cdot v_C . \qquad (5.5)$$

Therefore, there is

$$\Delta v_z = 2(k_1 - k_2)\cdot (v_A - v_B), \qquad (5.6)$$

assuming the two converters have the same reference vector, thus the same d_1 and d_2.

Equation (5.6) only shows the case that the reference vector is in sector I , and $v_B > v_C$. In total, there are 12 expressions for Δv_z when the reference vector is in different locations.

Figures 5.7 and 5.8 show the duty cycles of the top and bottom rails. Figure 5.9 shows the difference of the duty cycles in one phase leg. Figure 5.10 shows the common-mode voltage v_z in one converter. It can be seen that although the top and bottom rails' duty cycles are discontinuous, the common-mode voltage v_z is continuous. Therefore, it does not introduce the interaction caused by discontinuity of PWM as described in [24].

The proposed modulation in Figure 5.6 has more switching losses compared to the modulation in Figure 5.4 due to more switching actions in one cycle. A quantity analysis of the trade-off was not covered in this work.

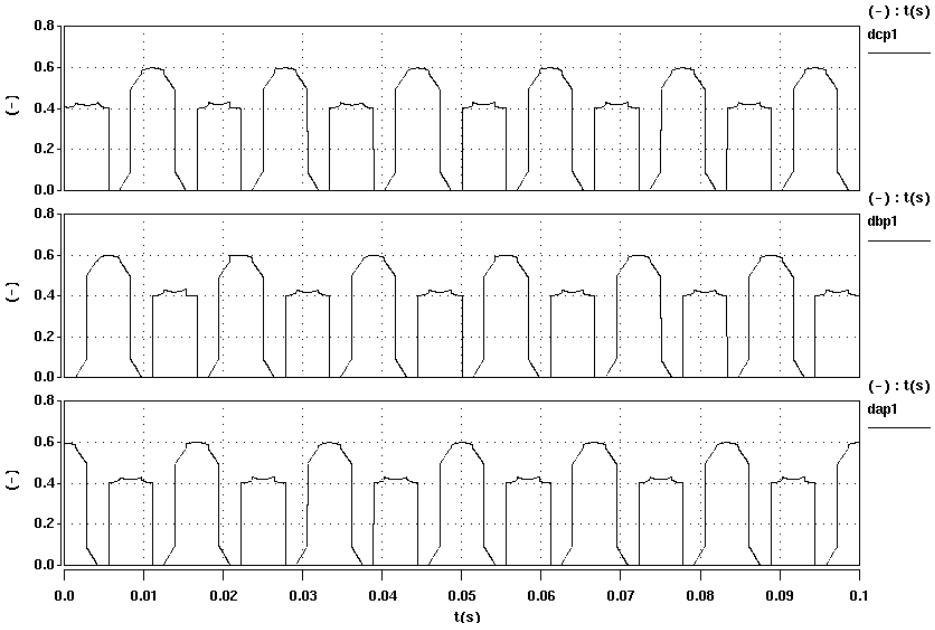


Figure 5.7 Top rail arm duty cycles d_{ap}, d_{bp} and d_{cp}.

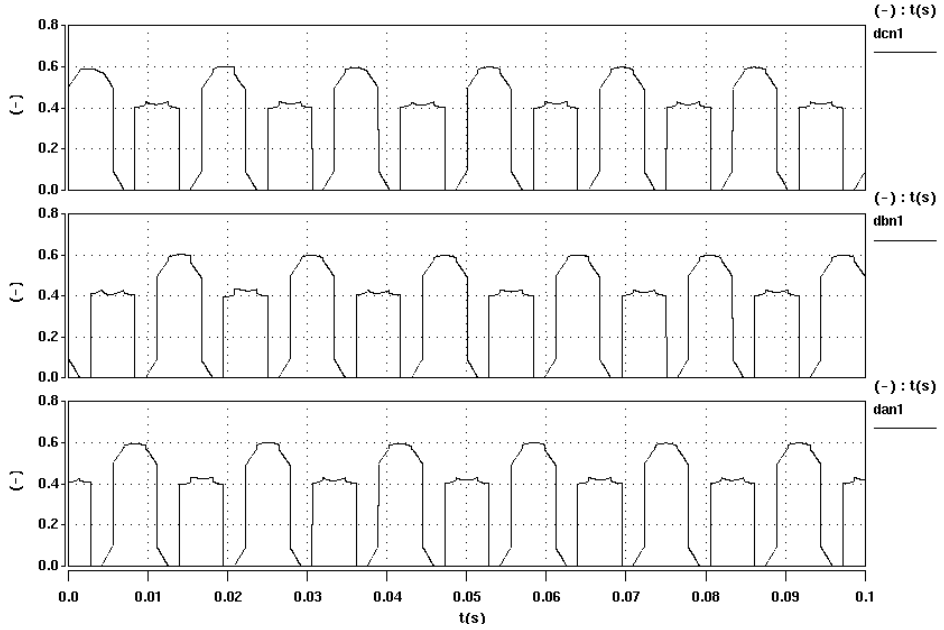


Figure 5.8 Bottom rail arm duty cycles d_{an}, d_{bn} and d_{cn}.

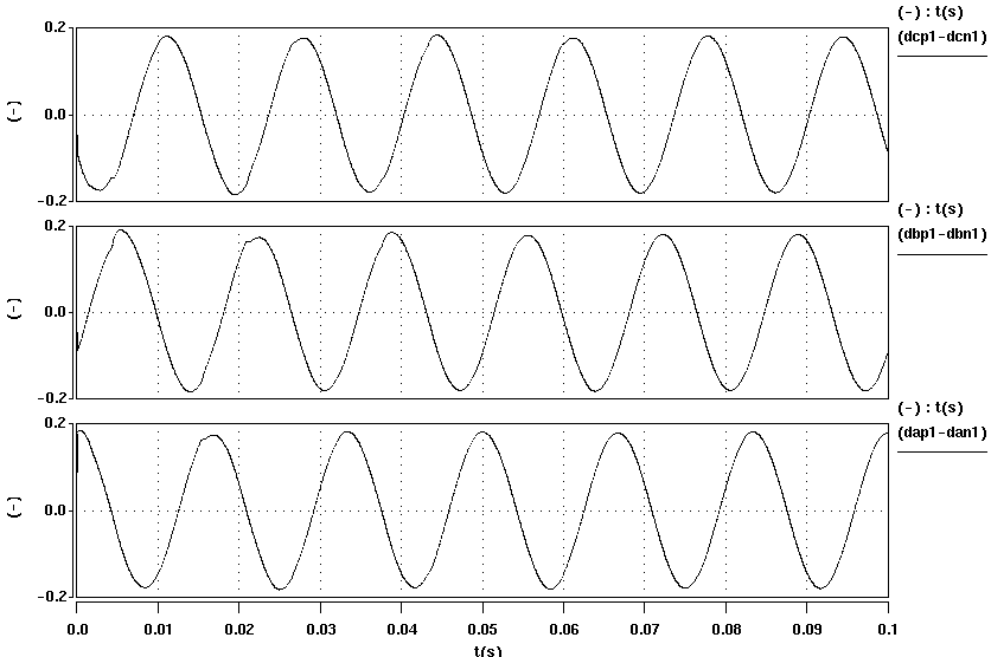


Figure 5.9 Duty cycles d_{ap}-d_{an}, d_{bp}-d_{bn} and d_{cp}-d_{cn}.

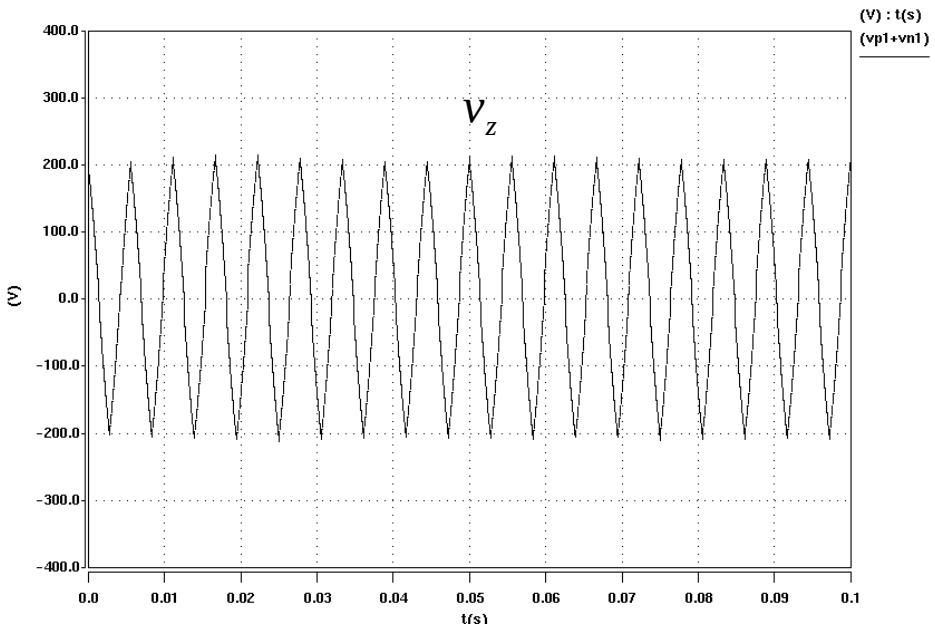


Figure 5.10 Zero-sequence voltage v_z.

5.1.3 Implementation

Since it is practically a first-order system, the control bandwidth of the zero-sequence current loop can be designed to be very high, and a strong current loop that suppresses the zero-sequence current can be achieved.

Two current sensors are placed at both positive and negative DC rails. Figure 5.11 shows the implementation of the zero-sequence current control. In a two-parallel converter system, it is sufficient to control one of the two converters because of only one zero-sequence current. The shaded block is the zero-sequence current controller added onto the rectifier's other control parts, which are not shown in Figure 5.11.

This control scheme can be designed within an individual converter and does not need any additional interconnected circuitry. Therefore, it allows modular design.

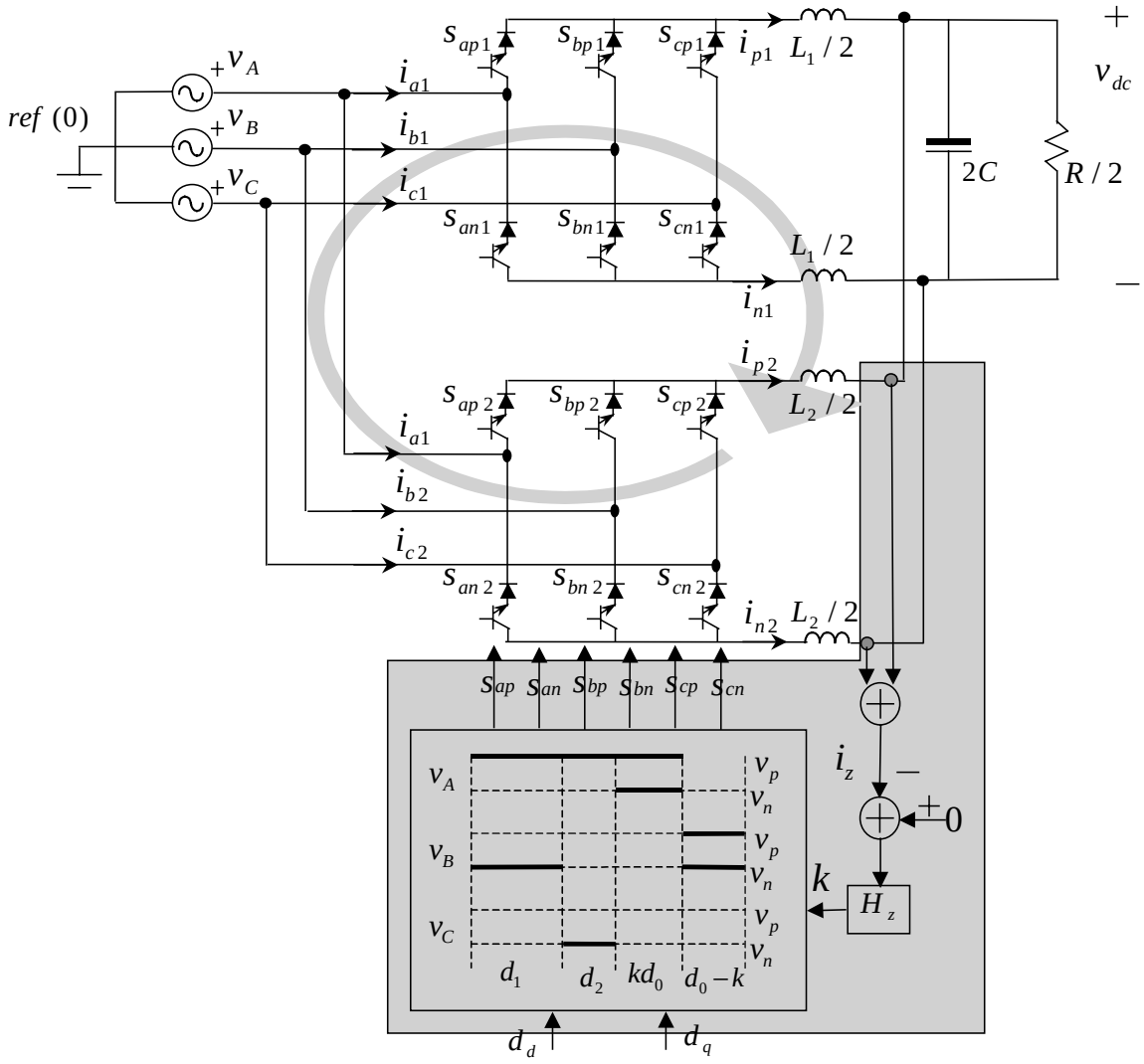


Figure 5.11 Zero-sequence current control implementation for parallel buck rectifiers.

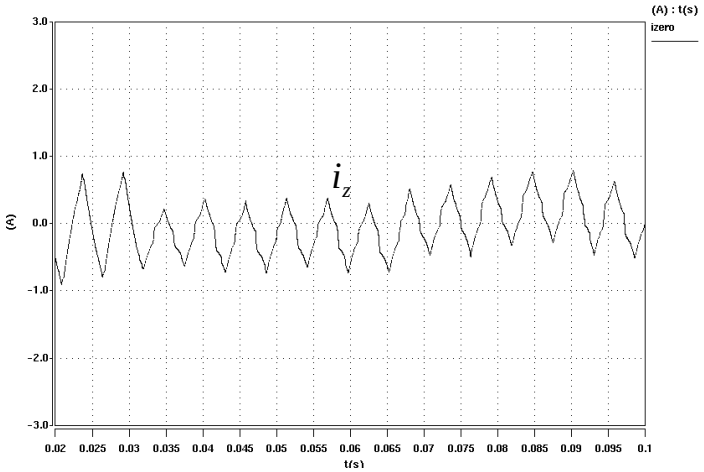
5.2 SIMULATION RESULTS

The simulation model was developed using SABER. The parameters are described below:

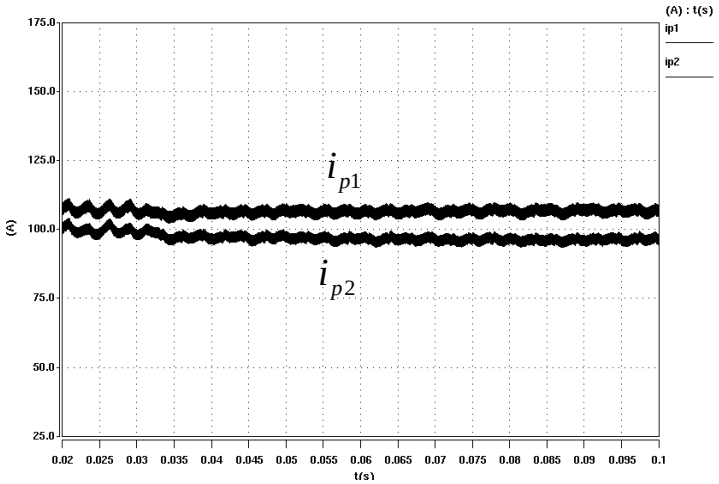
$V_{rms(a,b,c)} = 120\,\text{V}$; $\omega = 2\pi \cdot 60\,\text{rad/s}$; $V_{dc} = 100\,\text{V}$; $P_o = 0 \sim 15\text{kW}$; $L_{1,2} = 500\mu\text{H}$;

$ESR_{L_{1,2}} = 25m\Omega$, $C_{1,2} = 500\mu\text{F}$, $ESR_{C_{1,2}} = 5m\Omega$, $f_{sw} = 10\,\text{kHz}$, $H_z = \frac{0.2}{2\pi \cdot 60} + \frac{0.2}{s}$.

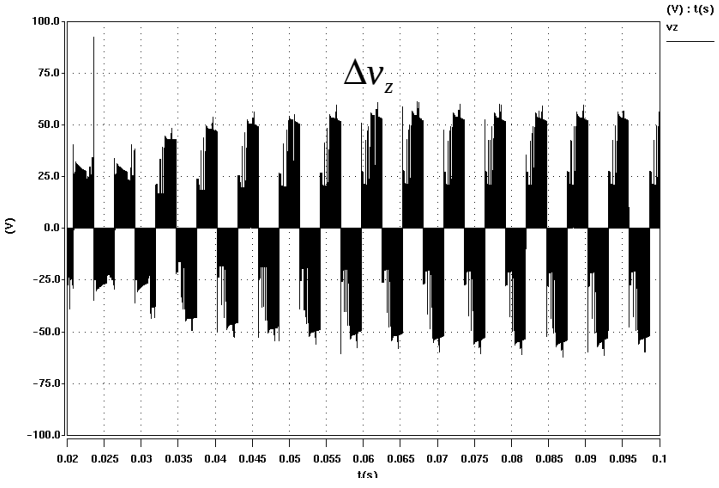
First of all, the developed average model was validated by the switch model. Figure 5.12 shows the simulation results with the switch model. Figure 5.13 shows the average model simulation results, which are practically the same as the switch model results. Figure 5.14 shows the results without zero-sequence control. By applying the zero-sequence control, the zero-sequence current is practically eliminated, as shown in Figure 5.15.



(a) Zero-sequence current.

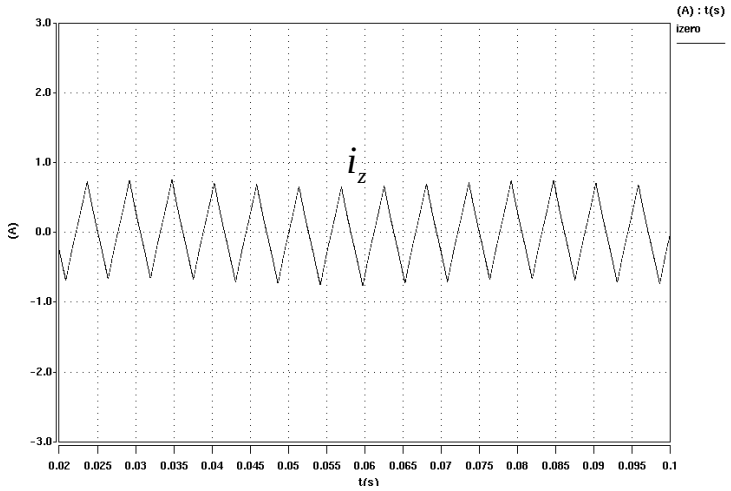


(b) DC rail currents.

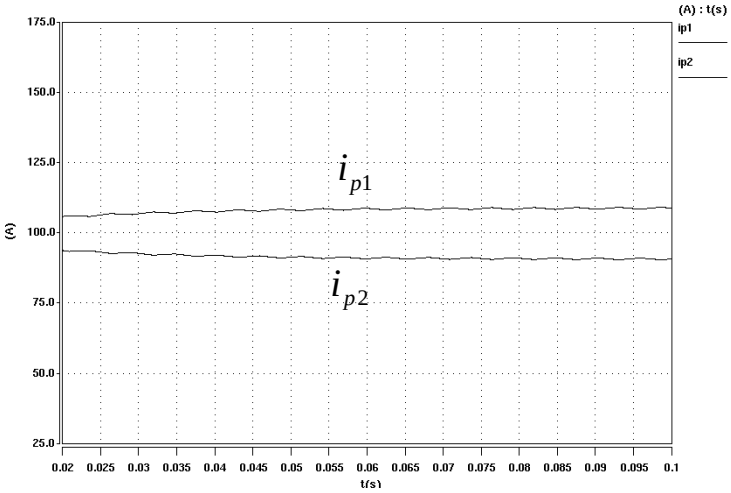


(c) The difference in the common-mode voltages.

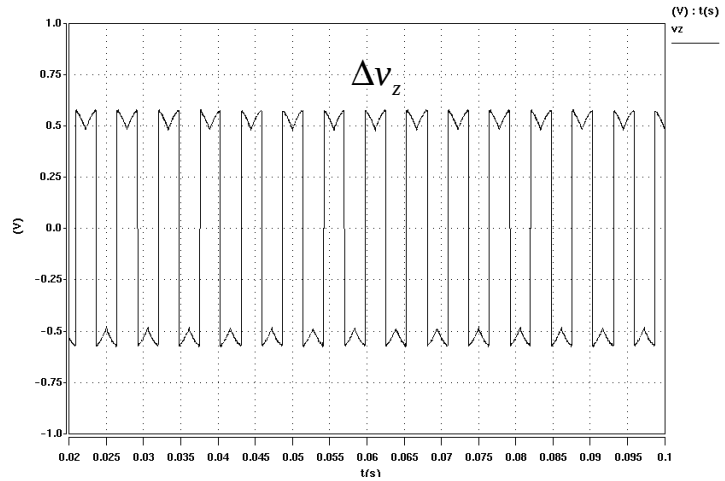
Figure 5.12 Simulated waveforms with switching model.



(a) Zero-sequence current.

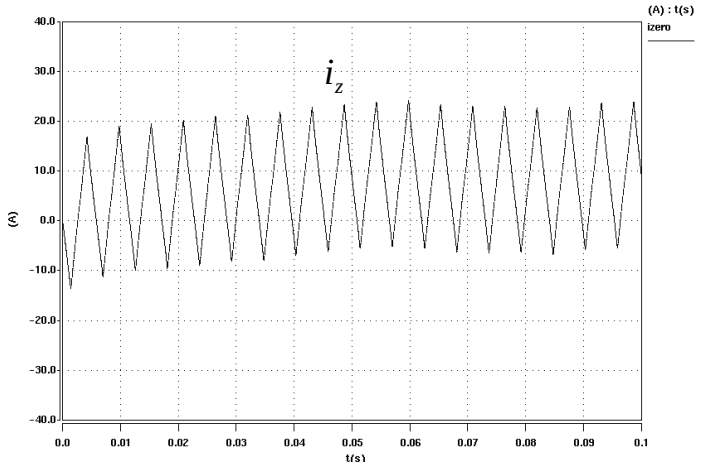


(b) DC rail currents.

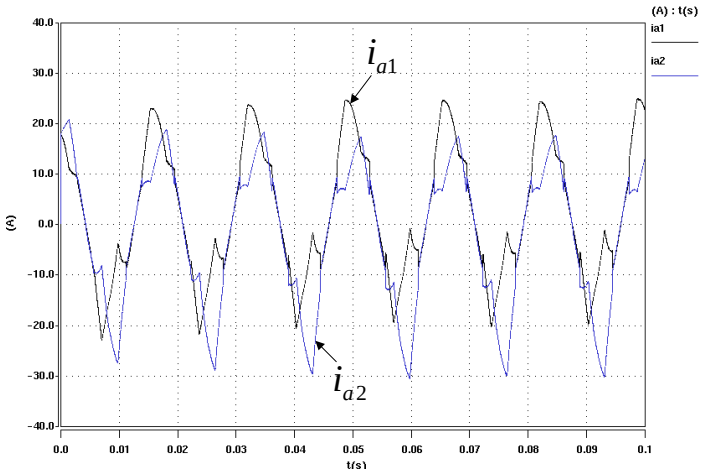


(c) The difference in common-mode voltages.

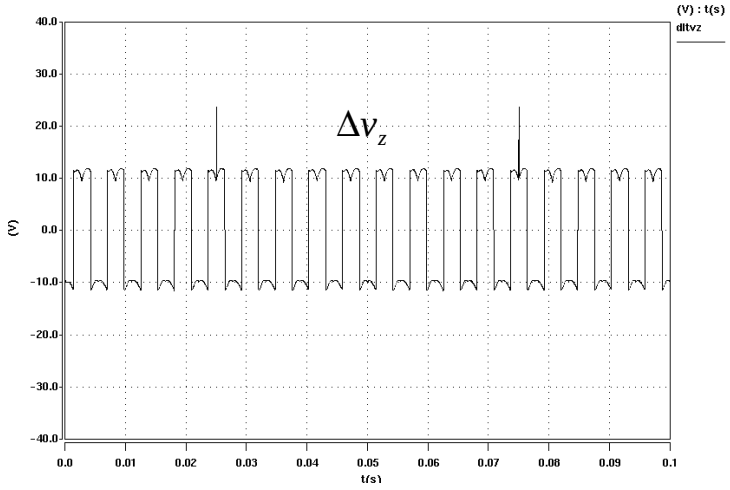
Figure 5.13 Simulated waveforms with average model.



(a) Zero-sequence current.

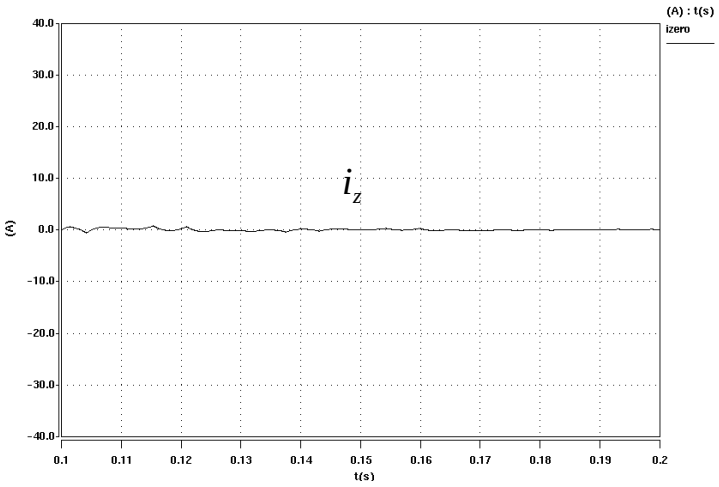


(b) Phase currents.

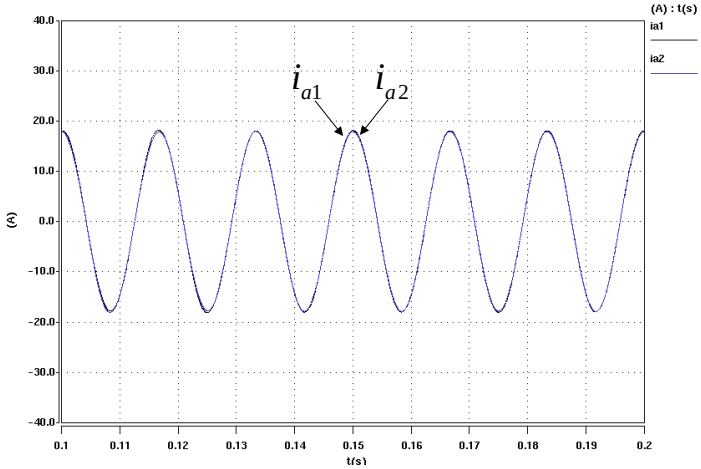


(c) The difference in common-mode voltages.

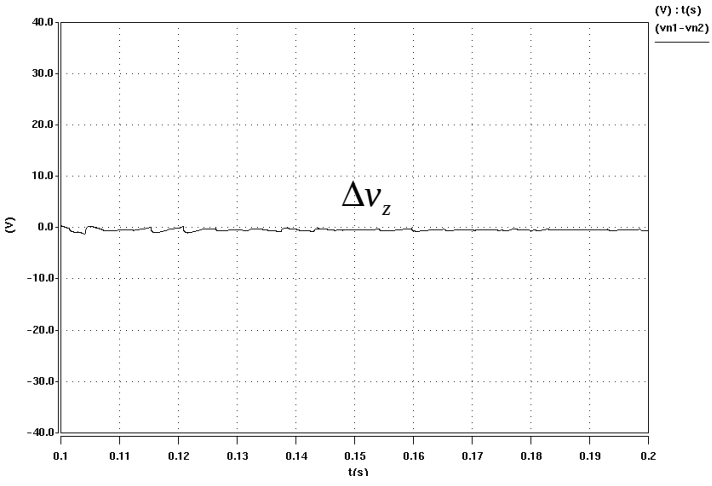
Figure 5.14 Simulated waveforms without zero-sequence control.



(a) Zero-sequence current.



(b) Phase currents.



(c) The difference in common-mode voltages.

Figure 5.15 Simulated waveforms with zero-sequence control.