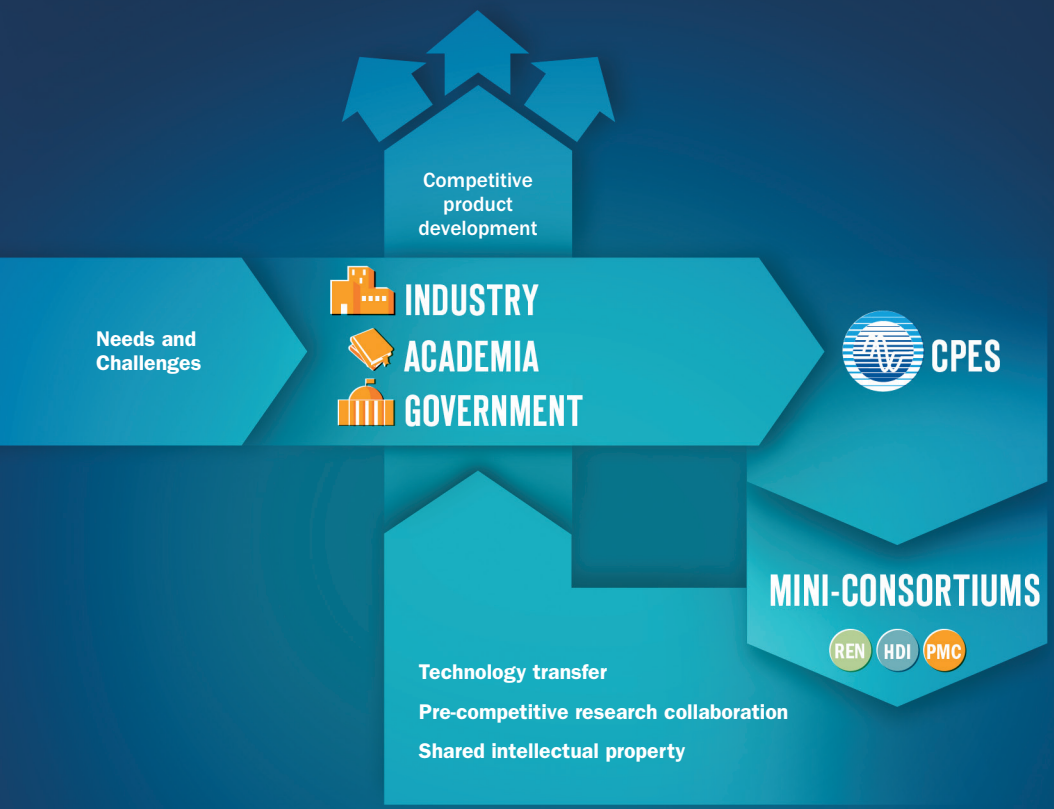
CPES

Center for Power Electronics Systems



A NEW MODEL to drive tomorrow's advances in power electronics

The knowledge and skills for the next leap in electrical efficiency are already at hand. The insights and capabilities however, are not contained in any single academic, industrial, or government laboratory. Only by tapping power electronics expertise from many groups will we solve these tough problems.

VirginiaTech

Invent the Future

Towards Collaboration

The Center for Power Electronics Systems (CPES) at Virginia Tech has created a new model for research that generates the collaboration needed to advance power electronics technology. Businesses, universities, and government agencies work together at a pre-competitive level to move the entire field forward. Individual companies then commercialize and adapt the solutions into commercial products that are more efficient, faster, and use less resources.

Join us in changing the way electricity is used.

HOW IT WORKS

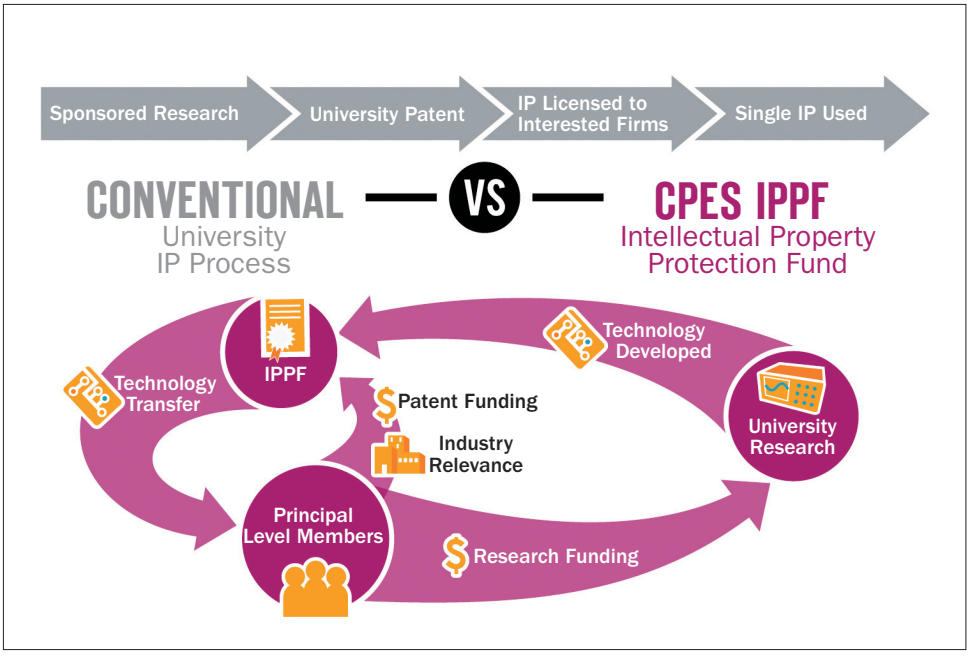
The CPES mini-consortium model provides a unique mechanism for all participants in power electronics – including industry competitors – to pool efforts to address their common challenges and develop pre-competitive advances.

Companies and organizations join CPES as a Principal Plus Member and choose the mini-consortium option. Annual membership fees are $50,000. Research results generated within a mini-consortium are shared among its members, and intellectual properties developed under the CPES industry consortium are shared among all Principal-level members as described on the next page.

The research and IP benefits are only part of what makes the mini-consortium effective. The distinctive feature of the model is discussion among all participants, which then shapes and guides research toward overcoming the major barriers in the field. Competitive plans and technologies are protected, yet participants can discuss their mutual technical problems. Mini-consortium interactions take place in the quarterly review meetings.

Additional Benefits:

- Access to CPES state-of-the-art facilities, faculty, student researchers, and research results
- Automatic IPPF (Intellectual Property Protection Fund) membership to gain easy and early access to technologies developed within the CPES industry consortium
- Representation on the CPES Industry Advisory Board (IAB) to guide and help shape CPES research direction
- Invitation to the monthly industry webinar series
- Privileged online access to CPES publications and technical presentations via member password
- Complimentary registration for CPES Annual Conference
- Significant discount for CPES short courses
- Option to participate in the Industry Residence Program and send company engineers to work on campus with CPES researchers



Novel IP process benefits all

The CPES intellectual property (IP) process offers unprecedented IP access to all Principal-level members at no extra cost. The CPES IPPF (IP Protection Fund) leverages funding from industry partners to expedite university technology into commercialization.

Principal-level members are invited to join quarterly IPPF telecon discussions with CPES inventors to decide jointly which technologies to protect, with patenting costs covered by IPPF. Once a technology is protected, all Principal-level members are granted a royalty-free, non-exclusive, non-transferable license to use technologies disclosed during their membership years. Engineers can use the technology without involving corporate lawyers and without having to develop their own proprietary technology.

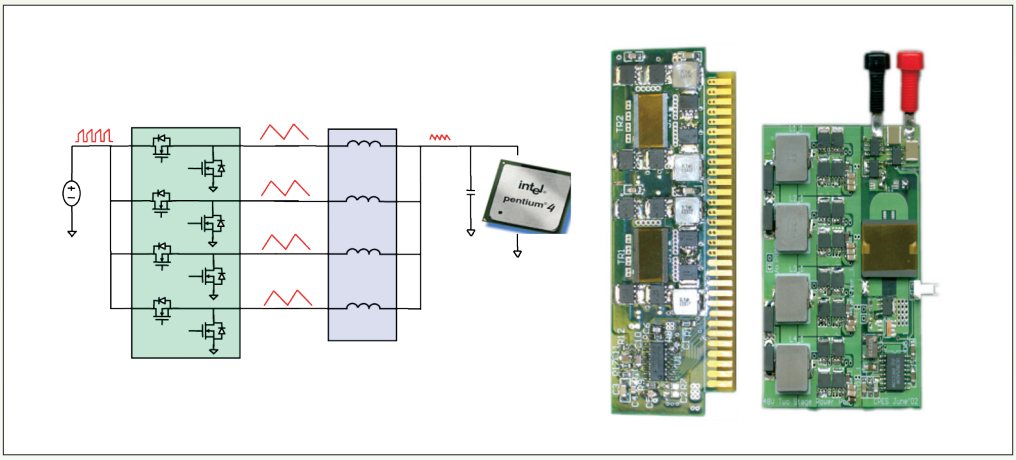
This IP model has been very successful and was instrumental in the success that triggered the U.S. National Science Foundation (NSF) to cite CPES as a model Engineering Research Center for technology transfer and industry outreach.

Pre-competitive technology

Pre-competitive collaboration is encouraged as a successful model in fast-moving fields, such as biotechnology and medicine, where advances in fundamental knowledge are tapped by different firms who then develop their own competing pharmaceuticals or technology. Society can also benefit from pre-competitive collaboration in power electronics, as the technology can move forward much quicker, generating energy efficiency in almost every industry.

"The CPES PMC program provides a very unique platform: while participants focus on the new technologies related to their own business strategy, they get a chance to see something out there that could possibly be the future."

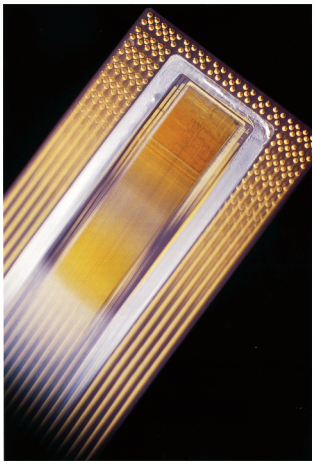
– Jinghai Zhou, Senior Manager, Technical Marketing & Applications, Monolithic Power Systems



The First CPES Mini-Consortium

CPES formed its first mini-consortium in 1997 at the request of Intel. Founding members of the CPES Voltage Regulator Module (VRM) mini-consortium included Delta, Intel, International Rectifier, National Semiconductor, STMicroelectronics (formerly SGS Thomson), and Texas Instruments.

The objective of the consortium was to help industry apply important new technologies in power delivery architecture, to meet increasing demands for the successive generations of microprocessor development in the future.



Multi-phase VRM

Within six months of beginning research, CPES developed a multi-phase VRM module. Breaking away from that era's method of paralleling power semiconductor devices to meet the increasing current demand and efficiency requirements, CPES proposed a system that paralleled a number of mini-converters. By also phase-shifting the clock signal, CPES was able to cancel more output current ripple and increase the ripple frequency, reducing the need for a large number of capacitors. Industry adopted the multi-phase VRM approach almost immediately.

Sponsored by Intel and more than 20 IC companies, CPES researchers developed more than 25 U.S. patented technologies to enable further advancements of the multi-phase VR. The technologies included power delivery architecture, modularity and scalability, control and sensor technologies, integrated magnetics, advanced packaging, and system integration.

Today, every microprocessor is powered with this multi-phase VR. With significant infrastructure established, the multi-phase VR has been further extended beyond the computer-related products to Internet infrastructure, telecommunications, and all forms of mobile electronics equipment.

Expanding into the PMC

CPES researchers continue to investigate power management issues and the mini-consortium was renamed the Power Management Consortium (PMC). Its expanded scope is to continue pursuing power efficiency in microprocessor-based computer and telecommunication applications through novel developments in power electronics topologies and system architecture.

PMC

Power Management Consortium

As processor-based systems become more complex, more power is consumed by both active and standby systems. At the same time, more systems are going portable and the emphasis on extending battery life adds more challenges to power management.

Historically, the goals of efficiency, thermal management, voltage regulation, reliability, power density, and cost drove power electronics design. These factors remain critical, particularly in the face of falling supply voltages and rising current demands. Yet, as multiple voltages proliferate across the PC board, the challenge becomes distributing and managing power across the board.

The Power Management Consortium (PMC) is an outgrowth of the VRM mini-consortium initiated in 1997. The consortium aims to develop pre-competitive technologies in power management at the board level. PMC is developing technology for distributed power system architectures, power management, EMI/EMC, power quality, ac-dc converters, dc-dc converters, and POL converters.

Advances at this level can help all participants in the industry, enabling companies to develop more efficient, more reliable systems that can successfully compete with each other in the marketplace. CPES expects PMC advances to lead to improved microprocessors, netbook, notebook, tablet, desktop, server and networking products, telecom equipment, solid state lighting, and more.

Power management challenges

- Light load efficiency of ac-dc converters and 80 PLUS
- Distributed power architecture for data centers, telecom base stations, servers, and netbook/notebook computers
- Voltage regulators for future microprocessors
- Digital control
- High-frequency modeling & control
- High-density power supply packaging and integration
- Front-end ac-dc converters
- EMI/EMC and power quality

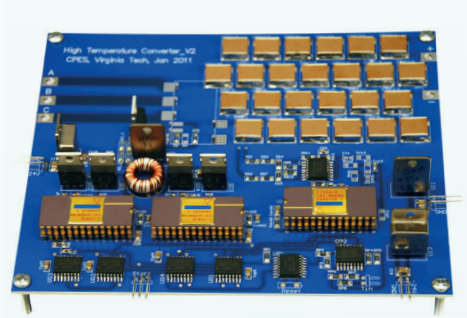
HDI

High-Density Integration

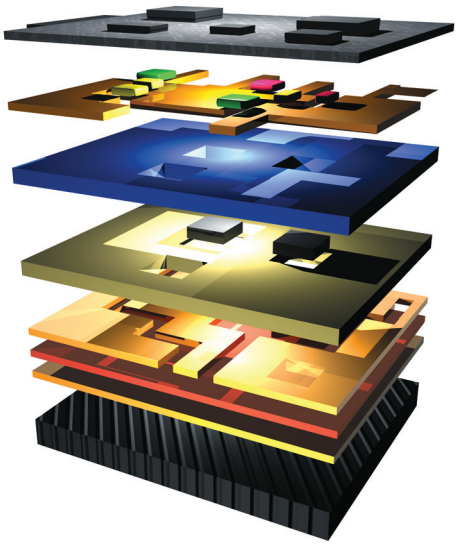
The emergence of wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) makes it possible to operate power converters at frequencies beyond 5 MHz and temperatures above 200° C. As the switching frequency increases, switching noise shifts to higher frequencies and can be filtered with small passive components — leading to improved power density. Higher operating temperatures enable not just increased power density, but also the ability for power electronics-based systems to operate in harsh environments, such as military, transportation, and outdoor industrial and utility systems.

Effective power conversion at megahertz switching frequencies and higher power levels (100 W – 100 kW) is severely constrained by impedances of the interconnecting, isolating, supporting, and cooling structures. This may be overcome by incorporating the structural impedances into the circuit operation and minimizing them through high-density integrated power electronics modules.

High-temperature, high-frequency power electronics systems, however, require more than just better semiconductor devices. Designers must also consider materials, gate drives, controller, passive components, packaging, and cooling.

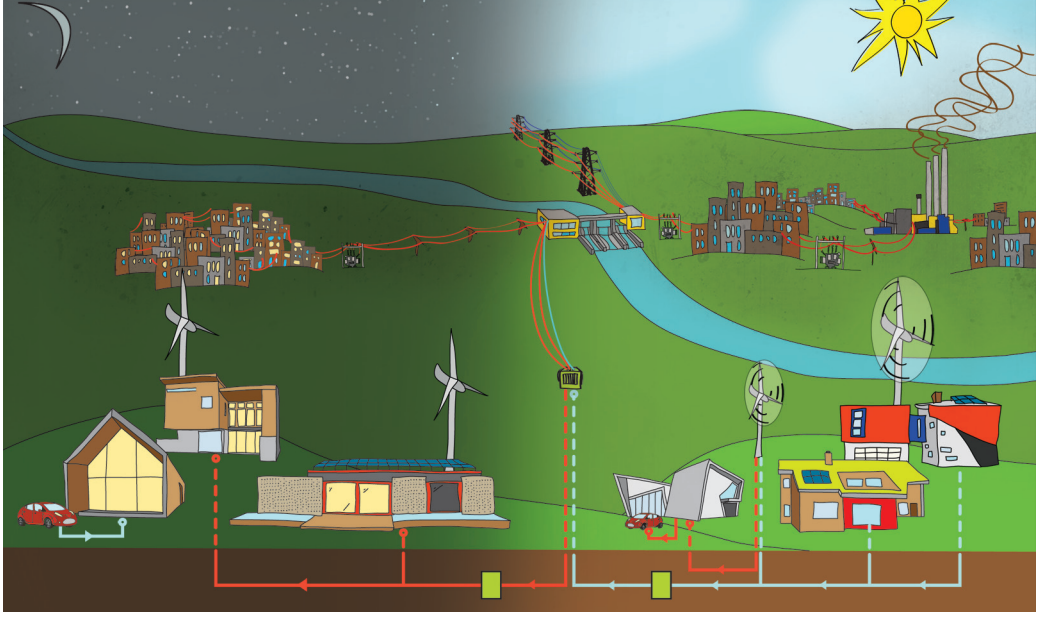


High-temperature 3-phase rectifier using SiC and Si-on-insulator components



The scope of work includes:

- **High-temperature integration**
  Reliable direct-bond-metal substrate; different die-attach technologies for thermo-mechanical reliability; high-temperature encapsulants for power electronics modules
- **Components**
  Characterization and modeling of wide-bandgap semiconductor devices; high-frequency magnetics and capacitors
- **Module-level integration**
  High-temperature packaging of power modules, including gate drives, sensors, and protection
- **System-level integration**
  High-density power supplies on a chip; high-temperature control components and system integration; integrated packaging of LEDs and drivers



REN

Renewable Energy and Nanogrids

The Renewable Energy and Nanogrids (REN) mini-consortium is developing electronic energy processing technologies for sustainable living environments that satisfy energy, functional, comfort, and zero-CO_2 emission goals.

CPES is building a living lab testbed based on ac and dc electric power systems using photovoltaic solar cells, wind generators, micro-turbines, fuel cells, and lithium-ion storage. The testbed will help address many of the nanogrid issues, such as dc bus architecture, energy/power management, and various forms of utility interface converters and inverters.

Power electronics already plays a major role in renewable-energy-based homes. Most electrical household functions depend on compact, reliable, low-cost power electronics. The sustainable-energy home, however, is expected to act as an energy producer delivering power to the grid when more energy is produced than consumed and then act as an electricity consumer from the grid the rest of the day.

Scope of work

- PV system
- Plug-in hybrid/ electric vehicles/ battery storage
- Wind power
- Energy management for the nanogrid
- Ac & dc nanogrid
- Solid state lighting
- Battery management systems

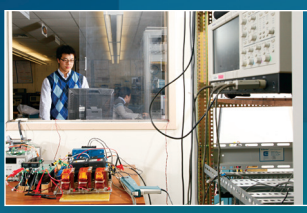
Homes that rely on renewable energy may also function as nanogrids. The interconnection between the home and the electric grid can be designed so that the home can operate both as a connection on the grid and as an island – an independent electrical system, managing internal sources and loads. In the independent case, energy storage becomes a critical component. Nanogrids can be further extended from single house systems to multiple homes, buildings, data centers, and neighborhoods.

Alternative energy systems will add complexity to the electrical power system with the coupled dynamics between thousands of distributed actively-controlled generation, storage, and consumption units.

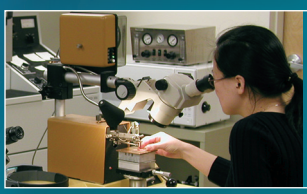
This "complexity curse" could be managed by using a single power-electronics-based load/source interface for each nanogrid. Each nanogrid could then be dynamically independent of the grid, but dispatchable by the utility operator.

CPES FACILITIES

CPES office and lab facilities encompass more than 19,000 sq.ft. of space in one building. Research space includes an Electrical Research Lab, an Integrated Packaging Lab, and a Computer Lab. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.



The electrical research laboratory is equipped with state-of-the-art power testing and measuring equipment, dynamometers, an EMI chamber, a clean room, and a mechanical shop.



The Integrated Packaging Lab is the first major university facility in the nation devoted to power electronics packaging research.

The Computer Lab supports all major software used in power electronics analysis and design.

CPES FACULTY

FACULTY

- Fred C. Lee, Center Director
- Dushan Boroyevich, Center Co-Director
- Paolo Mattavelli
- Khai Ngo
- Guo-Quan Lu (Affiliate member)

RESEARCH FACULTY & STAFF

- Igor Cvetkovic, Research Engineer
- David Gilham, Research Associate
- Alex Ji, Research Associate

SUPPORT STAFF

- Linda Gallagher, Administrative Assistant to Fred C. Lee, Center Director
- Marianne Hawthorne, Administrative Assistant to Dushan Boroyevich, Co-Director
- Linda Long, Finance Director
- Trish Rose, Procurement Officer
- Teresa Shaw, Industry Liaison
- Doug Sterk, Lab Manager

655 Whittemore Hall (0179)
Virginia Tech
Blacksburg, VA 24061
USA

WWW.CPES.VT.EDU