CHAPTER 6
ADVANCED SINGLE-STAGE PFC TECHNIQUES WITH VOLTAGE-DOUBLER RECTIFIER FRONT END FOR UNIVERSAL-LINE APPLICATIONS

6.1 INTRODUCTION

In Chapter 1-5, the state-of-art S^2PFC techniques have been studied and evaluated. It is shown that although the S^2PFC power supplies can achieve the desired performance in a variety of applications, they have significant difficulties meeting performance expectations in universal-line (90-265 V_{ac}) applications with a hold-up time requirement. As shown in Chapter 5, the difficulty of these S^2PFC circuits to deal with a wide line range and long hold-up time requirement stems from the fact that the voltage of the energy-storage capacitor, V_B, varies with the line voltage and load current. In most applications, with a proper design, $V_{B(max)}$ can be kept in the 400-420 V_{dc} range, which warrants a use of a 450-V electrolytic capacitor. Since the value of C_B is determined from the hold-up time requirement at the minimum line (worst case), the S^2PFC approach requires a relatively bulky and expensive energy-storage capacitor with V_B in 120-140 V_{dc} range at $90V_{ac}$ input and full load condition. Moreover, due to a wide-range variation of V_B that is the input to the dc/dc stage, the conversion efficiency of the dc/dc stage is reduced. In contrast, the two-stage approach, in which V_B is independently regulated at approximately 380 Vdc, requires a much smaller and, therefore, cheaper electrolytic capacitor rated at 450 V, or even 400 V. In addition, due to a regulated V_B, the efficiency of the dc/dc output stage in the two-stage approach can be made higher compared to that in the single-stage

approach. In summary, the wide capacitor voltage V_B range makes the existing S^2PFC techniques less attractive for universal-line power supplies, especially with higher output power rating.

Generally, the performance of conventional, universal-line-range power supplies without PFC can be improved by employing a voltage-doubler rectifier (VDR) [F6], as shown in Fig. 6.1. In the VDR diagram, the switch SW is a range-select switch, which is always closed in the 90-135 V_{ac} input range and opened in the 180-265 V_{ac} input range. In practice, SW can be implemented with mechanical, electrical or low-speed semiconductor switch. As shown in Fig. 6.2, the output voltage V_B of a VDR is approximately the same for both the low-line range (100/120-Vac power line) and the high-line range (220/240-Vac power line). Specifically, for the universal-line range, the VDR output voltage V_B varies from approximately 220 V_{dc} to 360 V_{dc}. Since this voltage range is much narrower than the corresponding voltage range of the conventional wide-range full-bridge rectifier (FBR), the efficiency of the dc/dc output stage can be improved. In addition, because the minimum voltage of a VDR is twice as high as that of the wide-range FBR, the total capacitance required for a given hold-up-time specification is approximately one-half of that required in the FBR. Finally, energy-storage capacitors in a VDR need to be rated at only 250 Vdc, or even 200 Vdc. Usually, electrolytic capacitors with a lower voltage rating are significantly cheaper than their counterparts with a higher voltage rating.

To reduce the S^2PFC bulk-capacitor voltage V_B range, it is nature to think about combining the VDR with S^2PFC techniques. However, there is difficulty to integrate VDR with the PWM S^2PFC topologies. Figure 6.3(a) shows one example, which simply combines the DCM S^2PFC structure with the VDR. Unfortunately, as shown in Fig. 6.3(b), the input current has high distortion in the negative half-line-cycle, at low input line range while the range-switch SW is closed. This problem is caused by the un-symmetric structure of the circuit in Fig. 6.3(a).

When the input voltage v_{in} is in the positive half-line-cycle ($v_{in}>0$), L_B is charged by $v_{in}+V_{C2}$ during switch S turn-on interval and discharged by $V_{C1}-v_{in}$ during switch S turn-off interval. However, when the input voltage v_{in} is in the negative half-line-cycle, the front-end is operated just as a diode-capacitor rectifier without any PFC. In conclusion, the voltage-doubler structure requires a horizontally symmetric circuit topologies to achieve identical charging/discharging waveform of the boost inductor L_B. Therefore, the existing S^2PFC topologies cannot be simply integrated with VDR.

In this Chapter, a new single-stage PFC technique that integrates the voltage-doubler-rectifier front end with a dc/dc output stage is introduced. Based on this concept, two families of voltage-doubler single-stage PFC (VD S^2PFC) converters are developed: a VD S^2PFC family with 2-terminal PFC cells and a VD S^2ICS family with 3-terminal PFC cells. Generalized circuit diagrams and principles of operation for both VD S^2ICS families are provided. The simulation and calculation results show both the reduction of the hold-up capacitance and improvement on the performances. Experimental results obtained on the 100W (5V/20A), 200W (5V/40A) and 450W (5V/90A) prototype circuits are given to verify the performance improvements. A comprehensive comparison among the CCM two-stage PFC converter, the CCM S^2PFC converter and the proposed CCM VD S^2PFC converter has been done to evaluated the proposed technique.

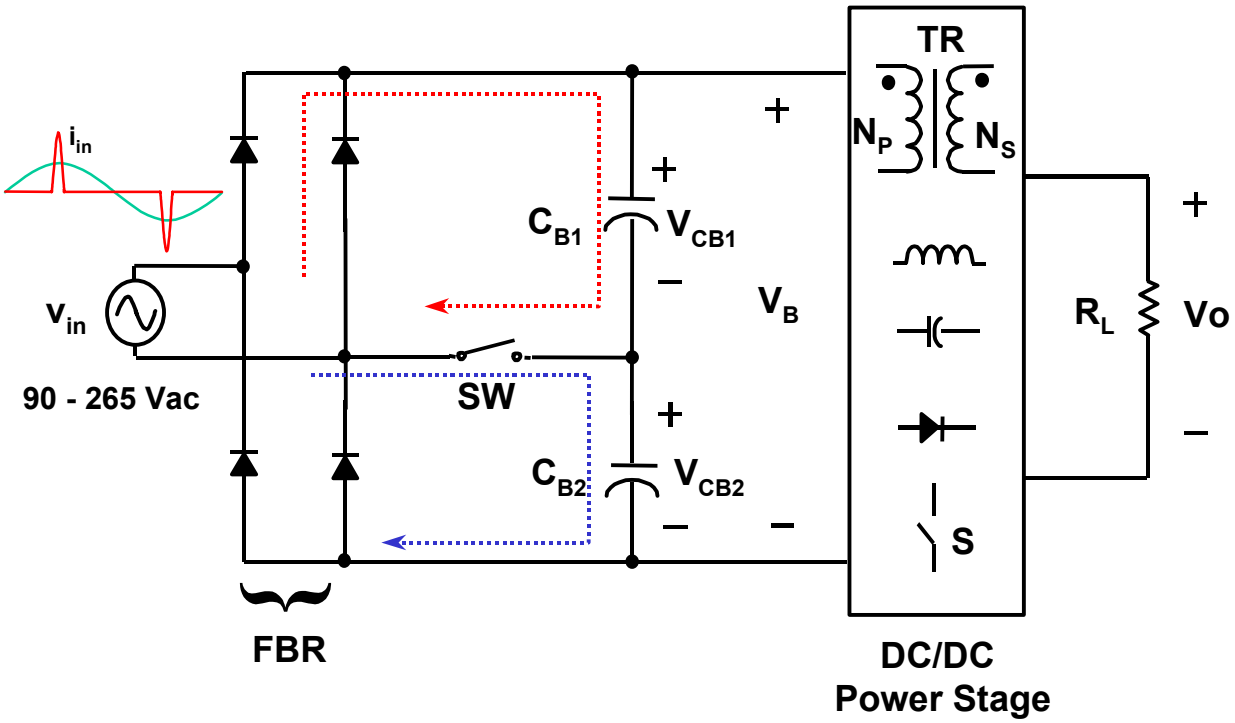


Figure 6.1 Circuit diagram of the conventional voltage-doubler rectifier (VDR) without PFC

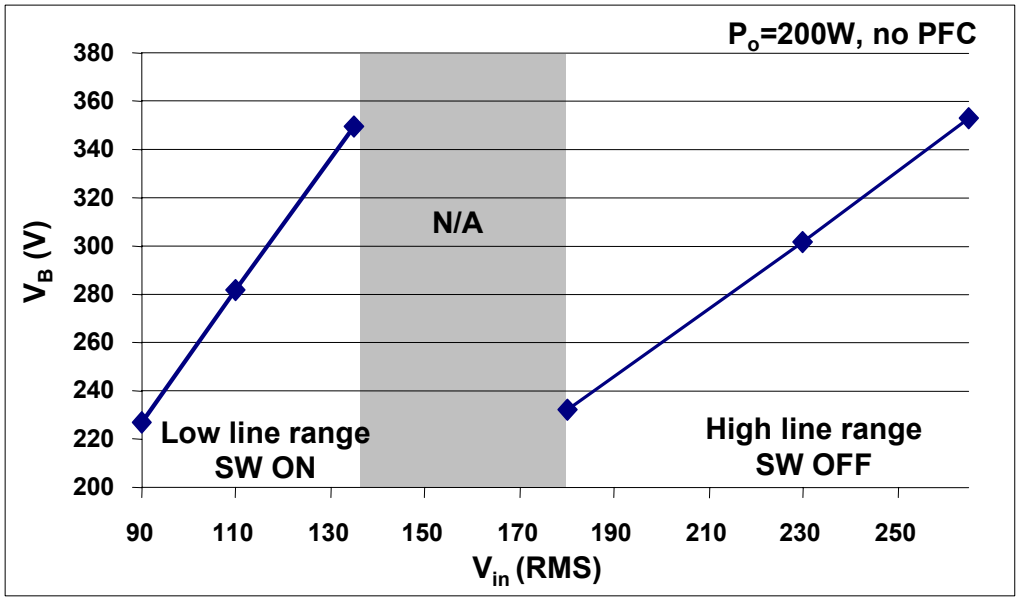
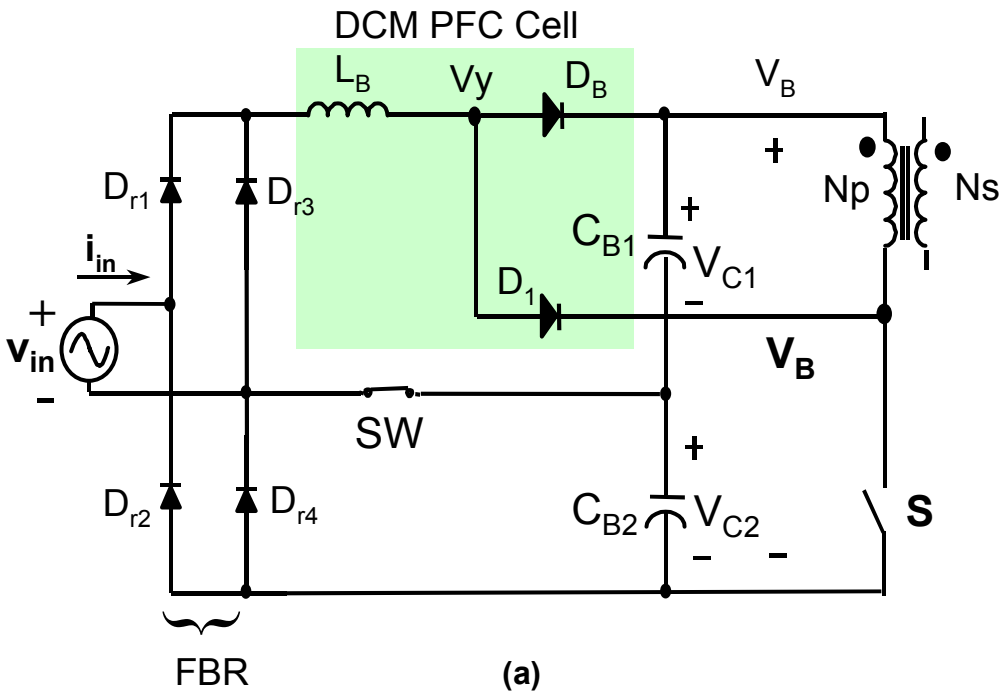


Figure 6.2 Bulk-capacitor voltage V_B vs. input voltage (VDR without PFC)



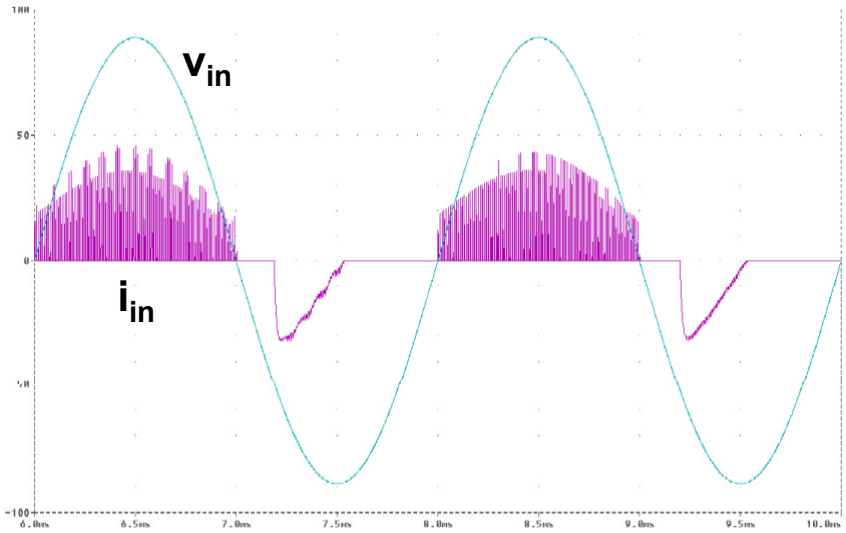


Figure 6.3 Simple integration of DCM S²PFC and voltage-doulber rectifier does not work (a) Circuit diagram, (b) input voltage and current waveforms

6.2 TOPOLOGIES AND OPERATION PRINCIPLES OF THE VOLTAGE-DOUBLER SINGLE-STAGE PFC (VD S^2PFC) CONVERTERS

6.2.1 Two-terminal voltage doubler S^2PFC converters and their principle of operation

6.2.1.1 Symmetric VD S^2PFC structure with PFC cells

Theoretically, the VDR requires a horizontally symmetric topology to provide alternative charging current to either the top capacitor C_{B1} or bottom capacitor C_{B2} in each half-line-cycle. Since the concept of the S^2PFC cells has been developed in Chapter 3, this concept can be used to develop the general VD S^2PFC structures. As shown in Fig. 6.4, to achieve symmetric topology required by VDR, two identical PFC (or ICS) cells are inserted between full-bridge rectifier FBR and energy-storage capacitors C_{B1} and C_{B2}, in both the positive and the negative rails. Each PFC cell consists of a boost inductor L_B and a 2-terminal high-frequency cell connected in series. The boost inductor L_B can be operated in either DCM or CCM mode, depending on the implementation of the high-frequency cells. All the two-terminal cells in Section 3.3.3 can be added into the general 2-terminal VD S^2PFC structure in Fig. 6.4. And the DC/DC stage can be implemented with any PWM DC/DC converters with isolated transformer TR, such as forward, flyback, half-bridge, and full-bridge topology, or any soft-switching topology.

For example, Fig. 6.5(a) shows one implementation of the DCM S^2PFC converters with two-terminal PFC cell. To minimize the number of magnetic cores, inductors L_{B1} in the top and L_{B2} in the bottom path can be wound on the same core, as shown in Fig. 6.5(a). Or, L_{B1} and L_{B2} can be combined into one winding, while L_B is put on the AC side of the diode-rectifier bridge. In the DCM VD S^2PFC circuit shown in Fig. 6.5(a), the boost charging and discharging paths are combined into one path through N_1. The top and bottom path windings N_1 are coupled with the

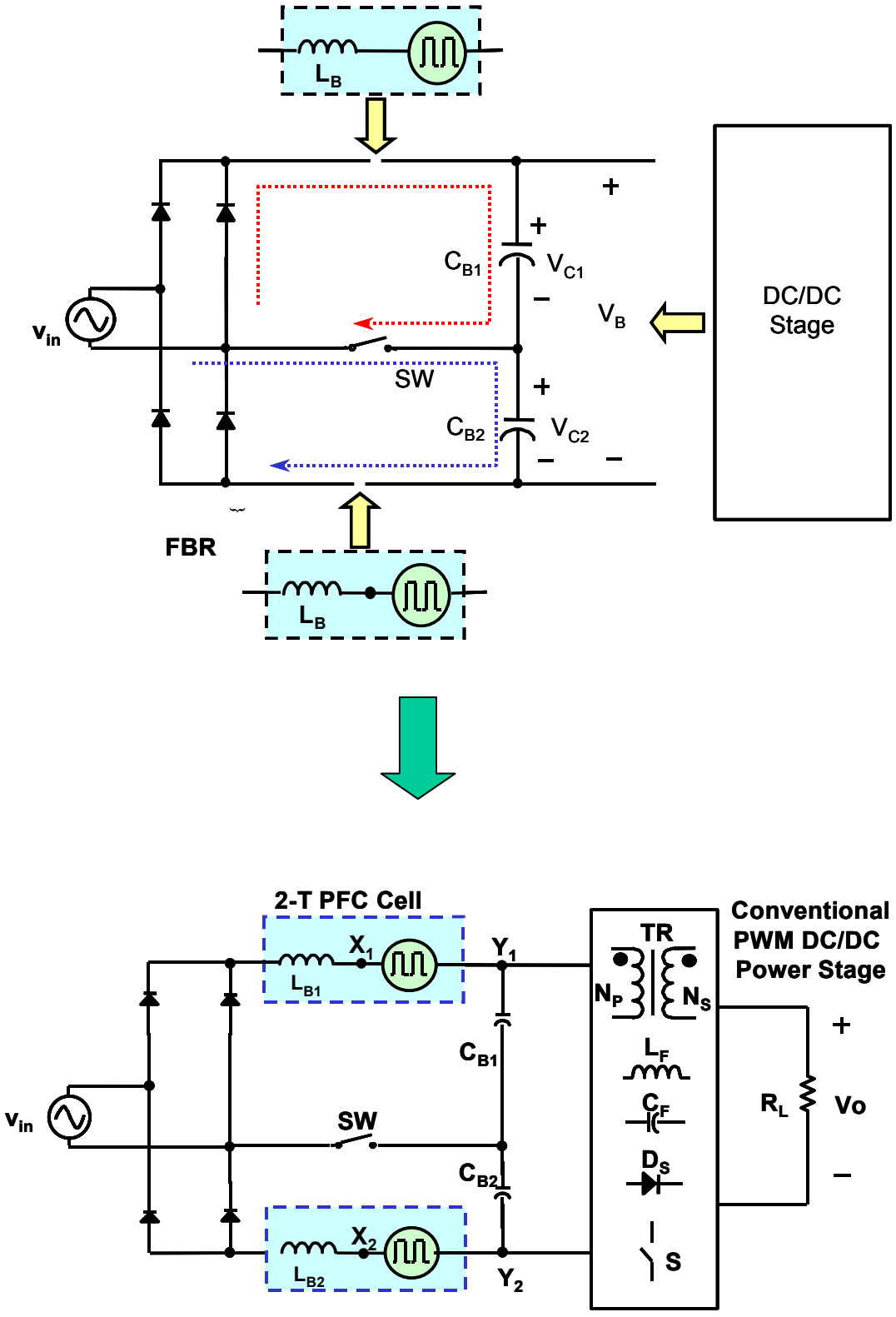
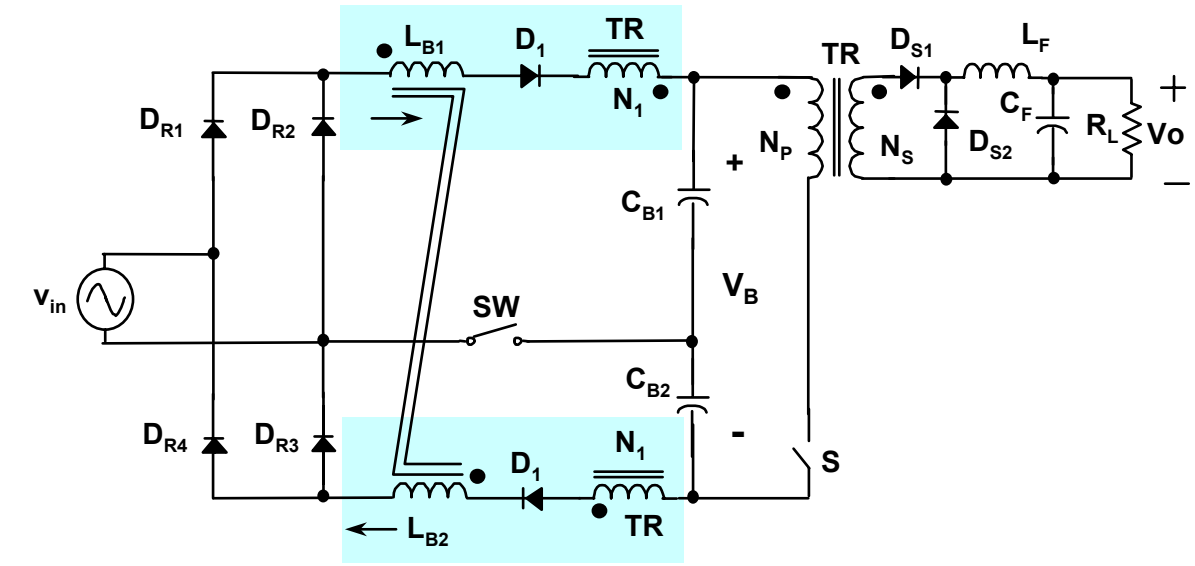
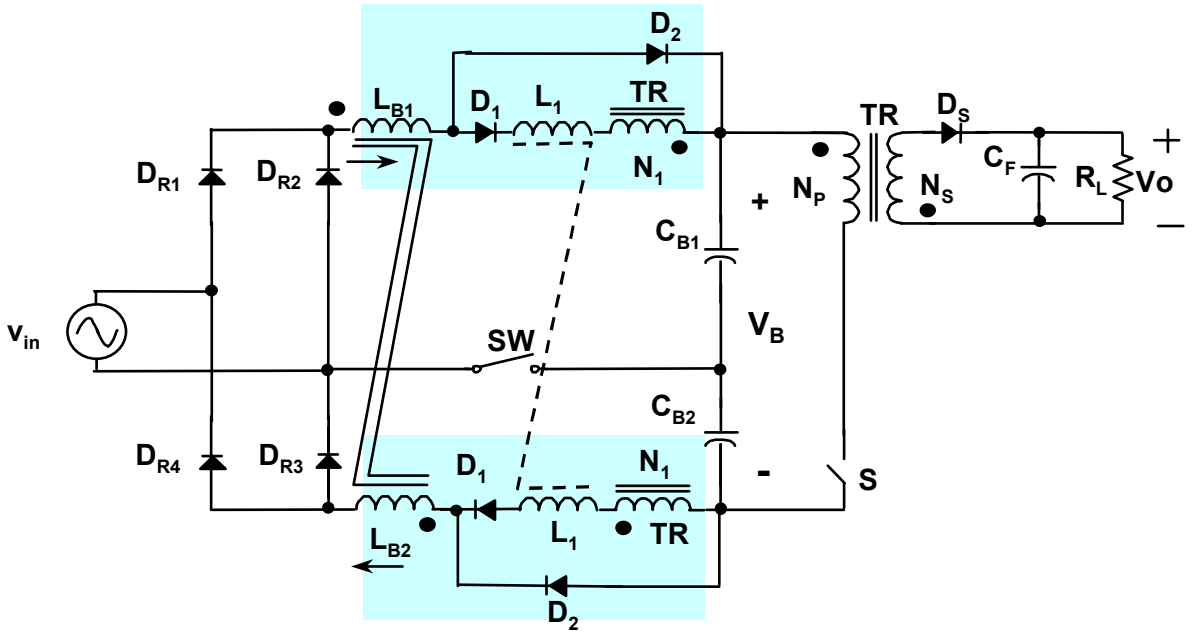


Figure 6.4 Develop the general structure of 2-terminal VD S^2PFC converters with S^2PFC cell



(a)



(b)

Figure 6.5 Implementations of the VD S^{2}PFC converters with 2-terminal PFC cells

(a) DCM VD S^{2}PFC converter, (b) CCM CS VD S^{2}PFC converter

DC/DC stage transformer TR. N_1 is also referred as the "magnetic switch" in [B12]. However, in the VD S^2PFC circuit, the turns-number of N_1 should be equal or less than $N_P/2$. In addition, the bulk-capacitor voltage "feedback winding" can be achieved by choosing $N_1<N_P/2$. The feedback ratio of the 2-terminal VD S^2PFC converters is defined as:

$$k = \frac{N_P - 2 \cdot N_1}{N_P} \qquad 6.1$$

Figure 6.5(b) provides an example of the CCM VD S^2PFC converters. The CS feed-forward cell is used in this converter with the CS inductor L_1. Similar to L_B, the top and bottom CS inductors can be winded on the same magnetic core to minimize the number of magnetic components. Again, the windings N_1 are coupled with N_P, while the turns-number of N_1 should be equal or less than $N_P/2$.

6.2.1.2 Principle of operation

The operating principle of the 2-Terminal VD S^2PFC converter can be explained by Fig. 6.6 and 6.7, in the low-line or high-line range, respectively. In the low-line range, range-select switch SW is closed and the front end operates in the voltage-doubler mode. As shown in Fig. 6.6(a), during a positive half cycle of the line voltage, with switch S in the dc/dc power stage closed, voltage v_{D1} across high-frequency source 1 is at its maximum [$v_{D1} = V_{D1max} > 0$, where $V_{D1max} < (V_{C1}+V_{C2})/2 \approx V_{C1}$] and in opposition to voltage V_{C1}. If the instantaneous line voltage is larger than $V_{C1} - V_{D1max}$, then voltage v_{L1} across L_{B1} ($v_{L1} = v_{in} + V_{D1max} - V_{C1}$) is positive and line current i_{in} increases, thereby storing energy in the boost inductor. At the same time, input current i_{DC} of the dc/dc power stage is supplied from energy-storage capacitors C_{B1} and C_{B2}. When switch S in dc/dc power stage opens, Fig. 6.6(b), current i_{DC} falls to zero, and voltage v_{D1} across dither source 1 changes sign ($v_{D1} = V_{D1min} < 0$), thus increasing the total voltage opposing

the line voltage. Consequently, voltage v_{L1} across L_{B1} ($v_{L1} = v_{in} - |V_{D1min}| - V_{C1}$) becomes negative, current i_{in} decreases, and the boost inductor discharges so that the energy stored in L_{B1} is transferred to C_{B1}. It should be noticed that since line current i_{in} cannot flow when v_{in} is smaller than $V_{C1} - V_{D1max}$, the line current is distorted around zero crossings. During a negative half cycle of the line voltage, the circuit in Fig. 6.5 operates in a similar manner as during a positive half cycle, except that diode D_{R4}, boost inductor L_{B2}, dither source 2, and bulk capacitor C_{B2} are active, as shown in Figs. 6.6(c) and (d).

When the circuit in Fig. 6.5 operates in the high-line range, range-select switch SW is open and the front end operates as a conventional full-bridge rectifier. As shown in Fig. 6.7, when operating as a conventional rectifier, boost inductors L_{B1} and L_{B2}, high-frequency sources 1 and 2, and energy-storage capacitors C_{B1} and C_{B2} are connected in series. During a positive half cycle of the line voltage, when switch S in the dc/dc power stage is closed, Fig. 6.7(a), voltages v_{D1} and v_{D2} across sources 1 and 2 are each at their maximum [$v_{D1} = V_{D1max} > 0$ and $v_{D2} = V_{D2max} > 0$, where $V_{D1max} \approx V_{D2max} < (V_{C1}+V_{C2}) / 2$], opposing voltages V_{C1} and V_{C2} across energy-storage capacitors C_{B1} and C_{B2}, respectively. If the instantaneous line voltage is larger than $(V_{C1}+V_{C2}) - (V_{D1max}+V_{D2max})$, then the sum of voltages v_{L1} and v_{L2} across L_{B1} and L_{B2}, i.e., $v_{L1}+v_{L2} = v_{in} + (V_{D1max}+V_{D2max}) - (V_{C1}+V_{C2})$, is positive and line current i_{in} increases, thereby storing energy in the boost inductors. At the same time, dc/dc power stage draws current i_{DC} from the serially connected energy-storage capacitors C_{B1} and C_{B2}. When switch S in dc/dc power stage opens, Fig. 6.7(b), current i_{DC} falls to zero. Simultaneously, voltages v_{D1} and v_{D2} across the dither sources change signs, i.e., $v_{D1} = V_{D1min} < 0$ and $v_{D2} = V_{D2min} < 0$, thus increasing the total voltage opposing the line voltage. Consequently, the sum of the voltages across boost inductors L_{B1} and L_{B2}, $v_{L1} + v_{L2} = v_{in} - |V_{D1min} + V_{D2min}| - (V_{C1} + V_{C2})$, becomes negative, thus

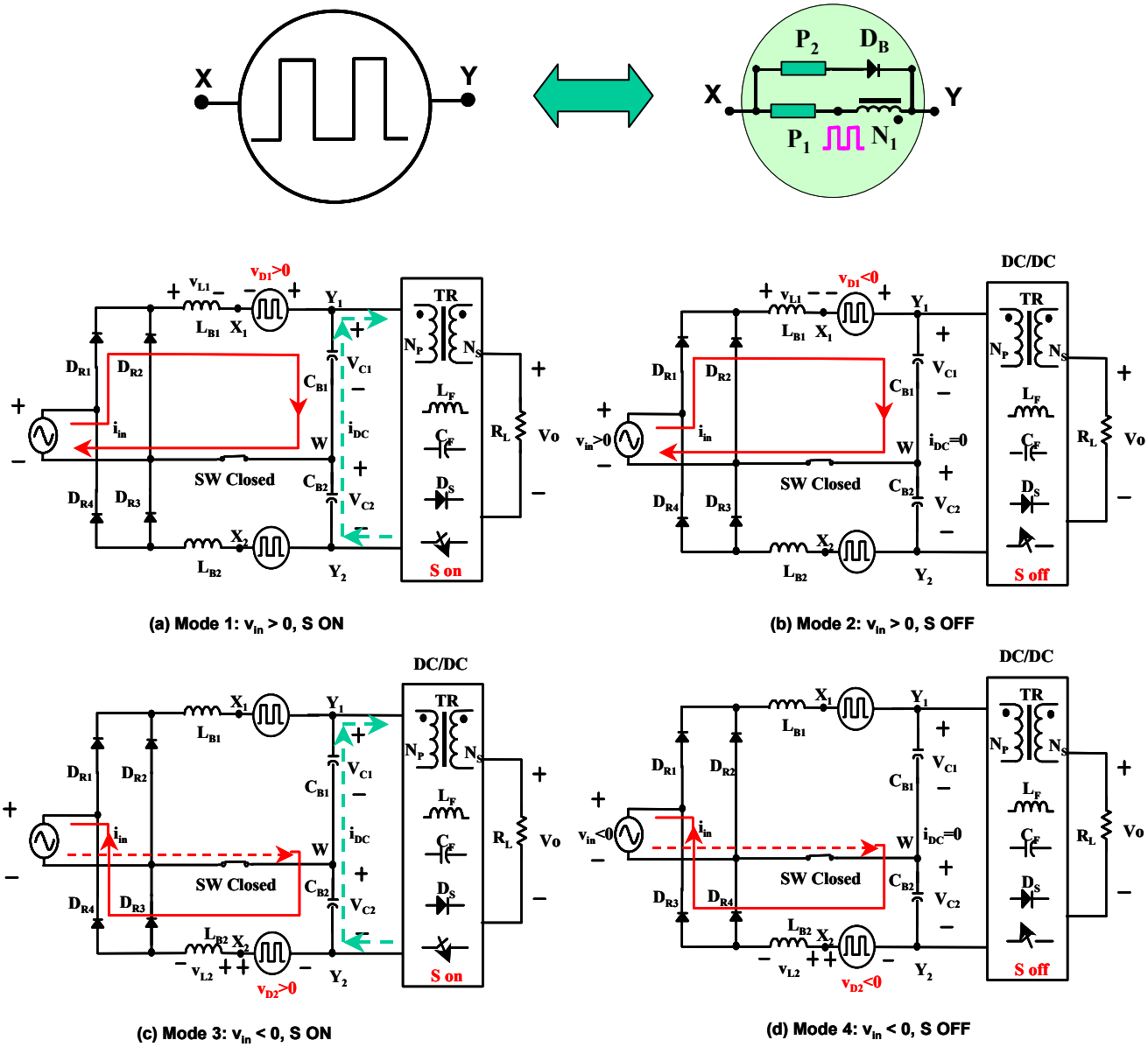


Figure 6.6 Low line operation modes of the VD S^{2}PFC circuit with 2-terminal PFC cells range: (a) v_{in}>0, S on; (b) v_{in}>0, S off; (a) v_{in}<0, S on; (a) v_{in}<0, S off

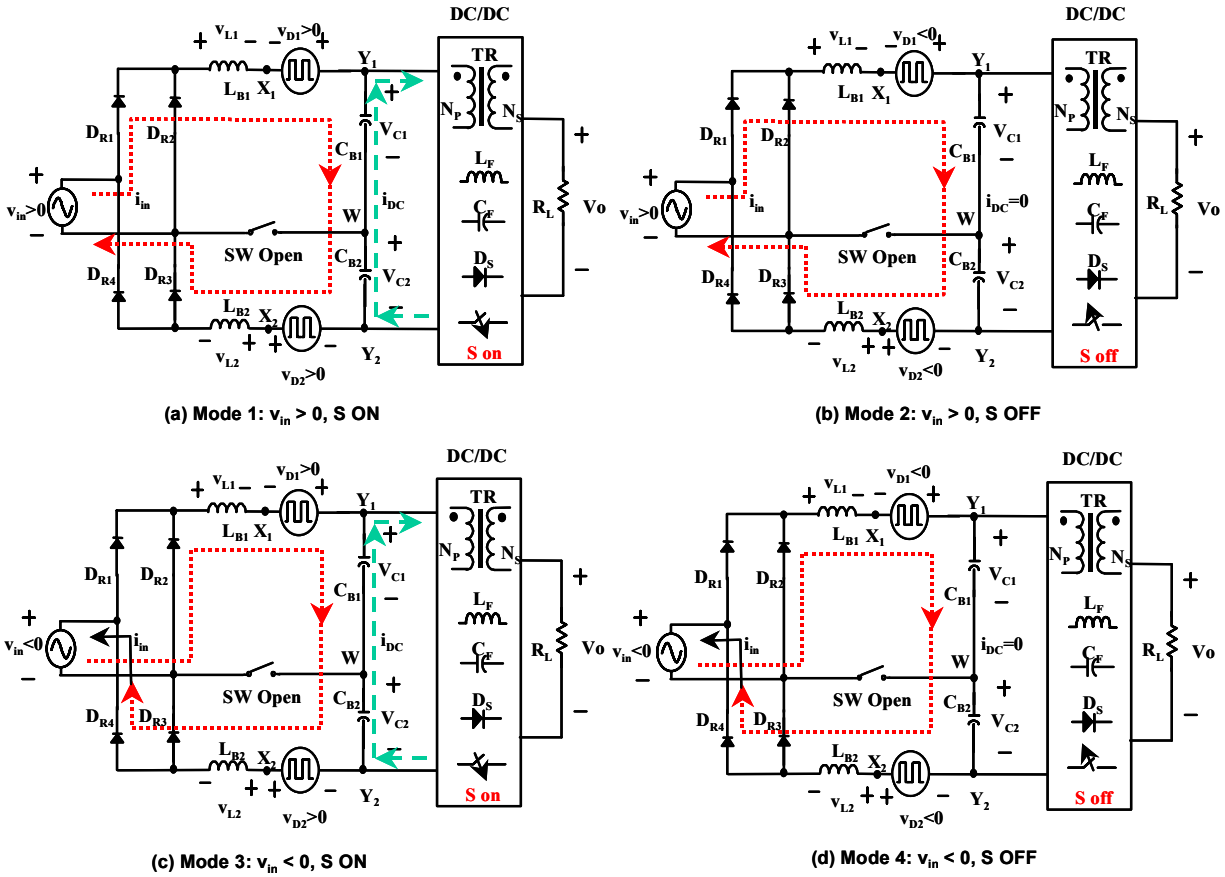


Figure 6.7 High line operation modes of the VD S^{2}PFC circuit with 2-terminal PFC cells range: (a) v_{in}>0, S on; (b) v_{in}>0, S off; (a) v_{in}<0, S on; (a) v_{in}<0, S off

decreasing line current i_{in} and transferring the energy stored in the boost inductors to the energy-storage capacitors. It should be noticed that since line current i_{in} cannot flow when $v_{in} < (V_{C1}+V_{C2}) - (V_{D1max}+V_{D2max})$, the line current is distorted around zero crossings. During a negative half cycle of the line voltage, the operation of the circuit is similar to the operation during a positive half cycle, except that rectifiers D_{R2} and D_{R4} are conducting line current i_{in}, as shown in Figs. 6.7(c) and (d).

6.2.2 Three-terminal voltage doubler S^{2}PFC converters

The equivalent relationship between the 2-terminal and 3-terminal S^{2}PFC cells and the corresponding converters have been discovered in Section 3.4. Conceptually, the general structure of the 3-terminal S^{2}PFC converter can be developed. As shown in Fig. 6.8(b), to achieve symmetric topology required by VDR, two identical 3-terminal PFC (or ICS) cells are inserted between full-bridge rectifier FBR and energy-storage capacitors C_{B1} and C_{B2}, in both the positive and the negative rails. Each PFC cell consists of a boost inductor L_B and a 3-terminal high-frequency cell connected in series. All the cells introduced in Section 3.2 can be used to achieve either DCM or CCM S^{2}PFC. In the PFC cell, the charging path terminal Z_1 and Z_2 should be connected to the switching signal in the PWM DC/DC converter.

However, different from the 2-terminal case, the 3-terminal VD S^{2}PFC also requires the PWM DC/DC stage to have horizontally symmetric structure. Figure 6.9 further shows how to split the DC/DC transformer primary winding N_P to combine two 3-terminal S^{2}PFC converters into one VD S^{2}PFC converter. Since the DC/DC stage has to be re-constructed with equally-split primary winding N_P, only single-ended DC/DC converters, such as forward or flyback converter, can be used in the 3-terminal VD S^{2}PFC converters.

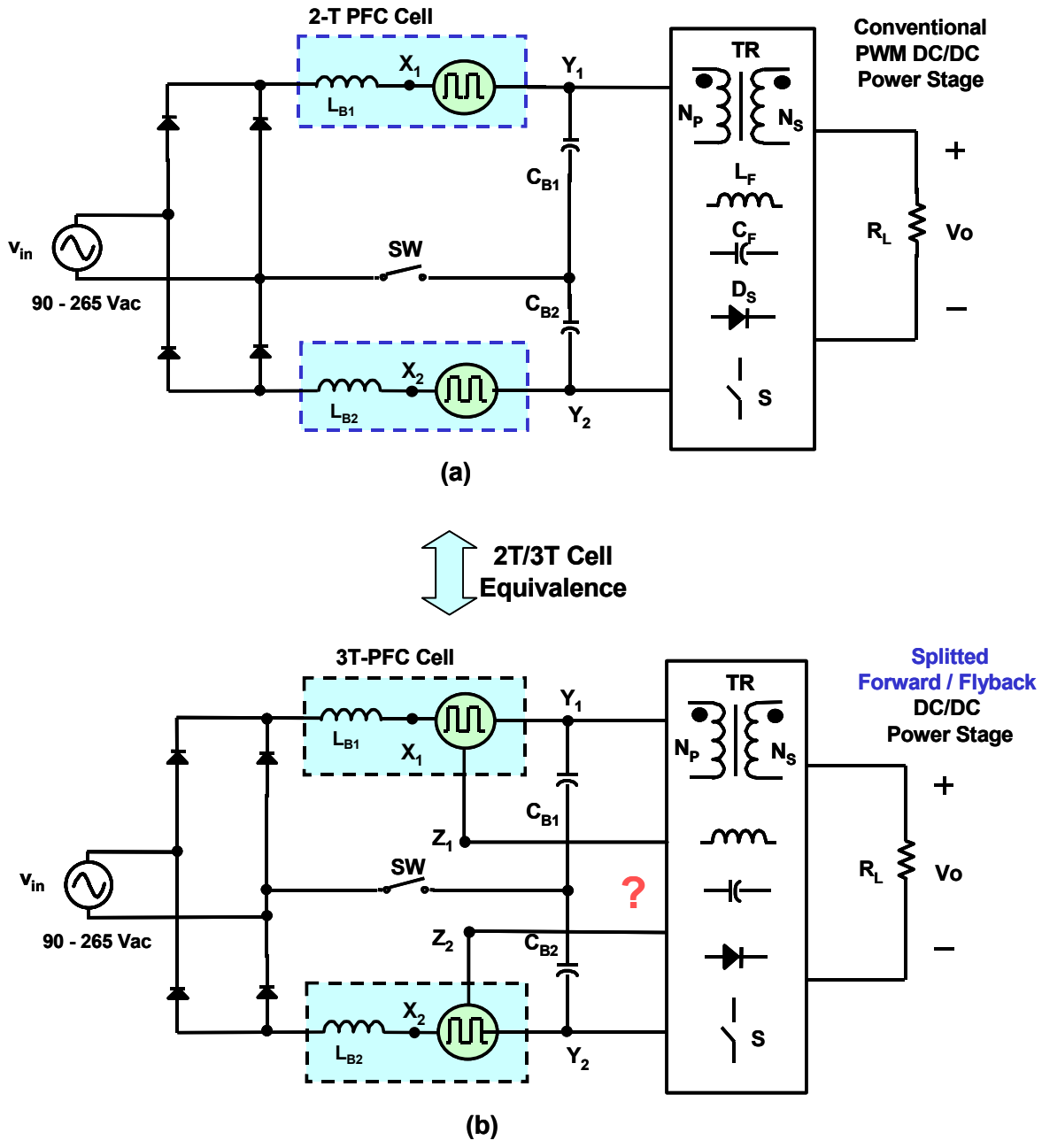


Figure 6.8 Derive the 3-terminal VD S2PFC general structure from the equivalent relationship between the 2-T and 3-T cells

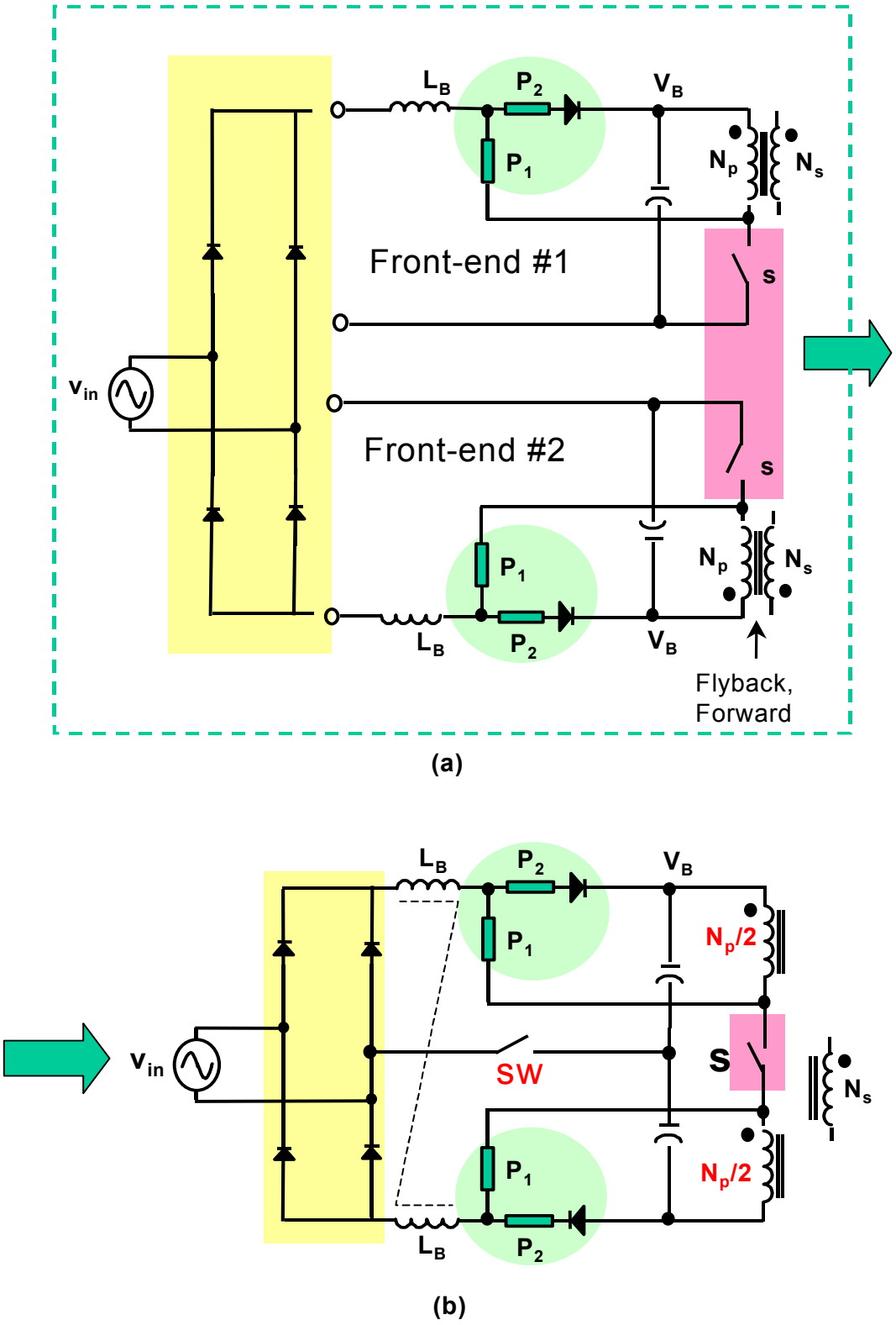


Figure 6.9 Split the DC/DC transformer primary winding N_P to implement the 3-terminal S^2PFC converter (with forward or flyback DC/DC stage only)

For example, Fig. 6.10(a) shows an implementation of the DCM 3-terminal VD S^2PFC converter with flyback DC/DC stage. As shown in Fig. 6.10(a), the bulk-capacitor voltage feedback winding N_1 can still be implemented and the feedback ratio k is defined as:

$$k = \frac{2 \cdot N_1}{N_P} \tag{6.2}$$

Figure 6.10(b) shows a CCM 3-terminal VD CS-S^2PFC converter with forward DC/DC stage. Again, to minimize the magnetic component count, the top and bottom CS inductors L_1 can be winded on that same magnetic core. It is necessary to point out that the 3-terminal VD S^2PFC front-end in Fig. 6.10(b) is equivalent to the 2-terminal front-end in Fig. 6.5(b), if $N_1=N_P/2$ in Fig. 6.5(b).

Due to the equivalent relationship between the 2-terminal and 3-terminal S^2PFC, the principle of operation of the 3-terminal VD S^2PFC converter is similar to that of the 2-terminal VD S^2PFC converter. In the high line range, the range-switch SW is opened, so the VD S^2PFC converter is operated as a conventional S^2PFC converter. In the low line range, the range-switch SW is always closed so that the bulk-capacitor C_{B1} and C_{B2} are charged in each alternative half line cycle. The total boost output voltage V_B is doubled with the integrated VDR structure and the V_B range is reduced with universal line input.

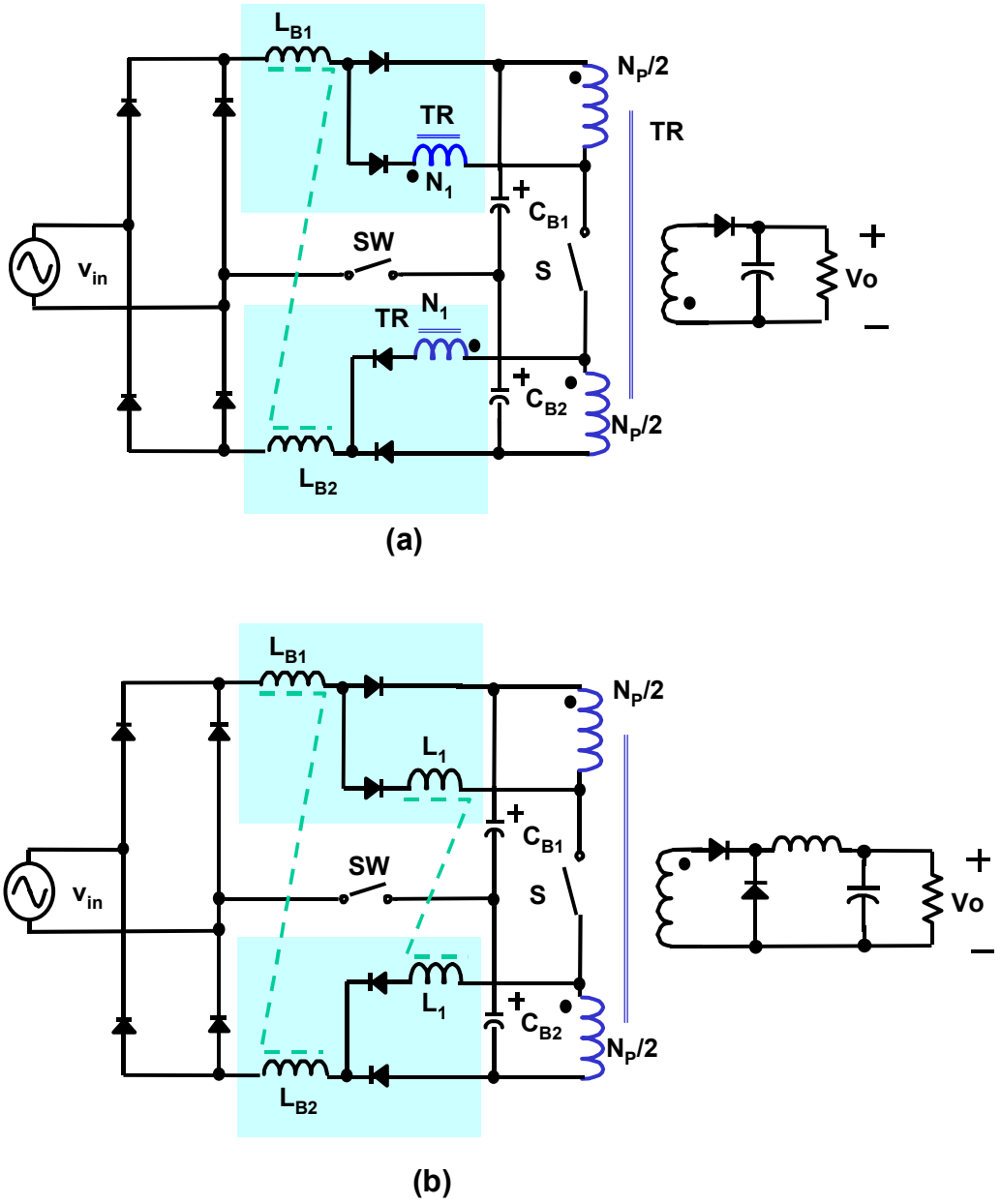


Figure 6.10 Implementations of the VD S^{2}PFC converters with 3-terminal PFC cells

(a) DCM VD S^{2}PFC converter, (b) CCM CS VD S^{2}PFC converter

6.3 SIMULATION VERIFICATIONS

6.3.1 DCM S^2PFC converter with VDR

The DCM VD S^2PFC circuit in Fig. 6.5(a) has been simulated with following specifications and key parameters: input voltage V_{in} = 90 – 135 V_{RMS} and 180 – 265 V_{RMS}; output 5V/20A; boost inductor L_B = 5 μH (each winding); transformer winding $N_P/N_1/N_S$=17/3/1; switching frequency f_s=100 kHz.

Figure 6.11 shows the simulated circuit waveforms at 90 V_{RMS} input, full load, while the range-switch SW is closed and the circuit is working in the voltage-doubler mode. As shown in Fig. 6.11, the top and bottom boost inductors L_{B1} and L_{B2} conducts current in each alternative half-line-cycle. Therefore, the boost capacitor C_{B1} and C_{B2} are charged alternatively. The total output voltage $V_B=V_{CB1}+V_{CB2}$. When the bulk-capacitor feedback winding ratio k=0.65, without VDR, the DCM S^2PFC has a boost bus voltage in the 130-150 V_{DC} range at 90V_{RMS} input. As shown in Fig. 6.11, because of the VDR structure, the boost bus voltage of the VD S^2PFC is about 290 V_{DC}, which is as twice as the voltage $V_{B(min)}$ in the conventional S^2PFC converter. Therefore, with proper design, V_B of the VD S^2PFC converter is in the range of 260 – 420 V_{DC}, while V_B in the conventional S^2PFC without VDR is in the 130 – 420 V_{DC} range with universal line input. As a result, the VD S^2PFC converter needs smaller hold-up capacitance and has better performance. The detail calculation and experimental results will be given in later sections.

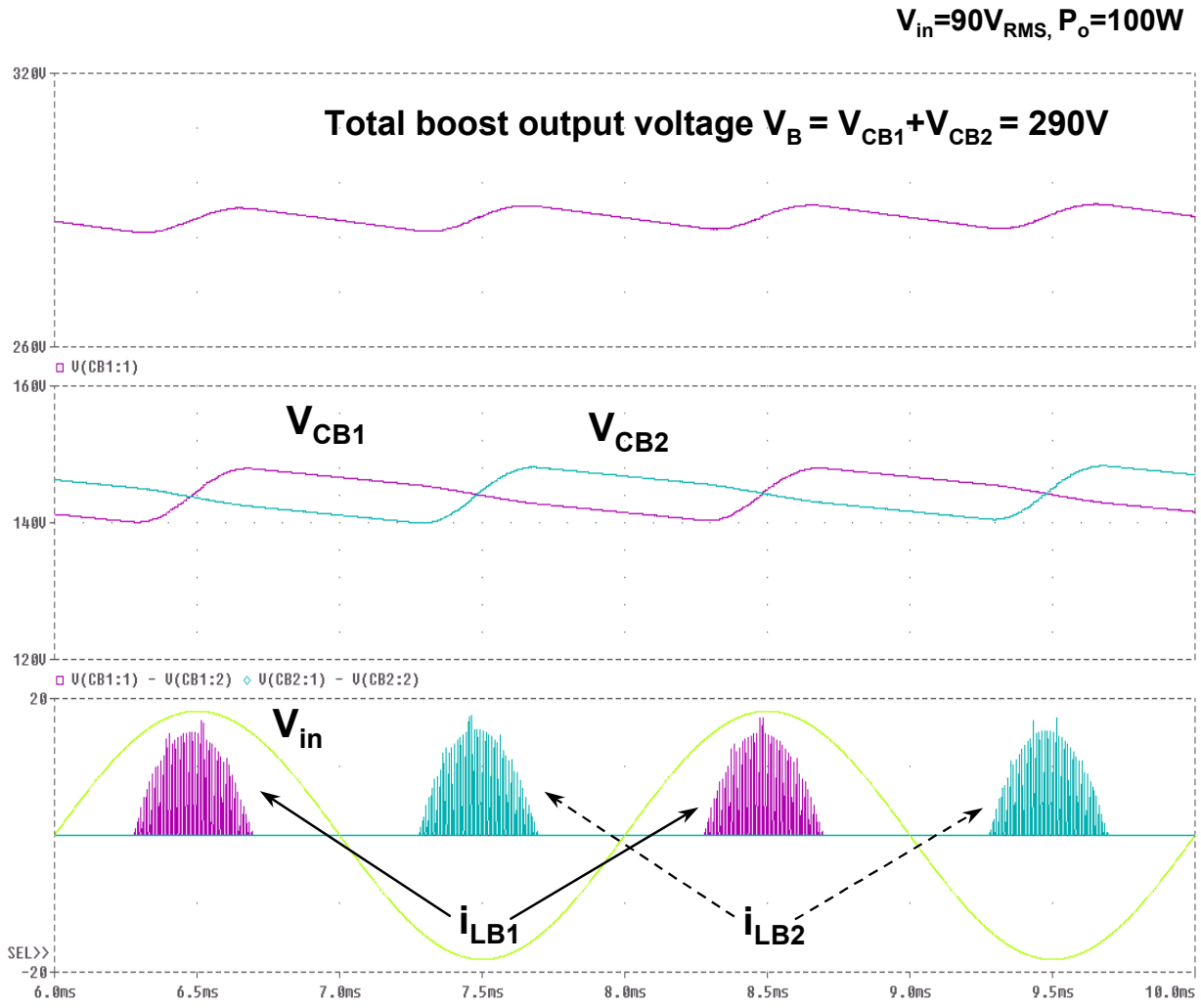


Figure 6.11 Simulated circuit waveforms of the DCM VD S^2PFC converter

(at V_{in}=90V_{RMS}, Output 5V/20A, f_s=100 kHz)

6.3.2 CCM CS-S^{2}PFC converter with VDR

The CCM VD CS-S^{2}PFC converter in Fig. 6.5(b) has been simulated with following specifications and key parameters: input voltage V_{in} = 90 – 135 V_{RMS} and 180 – 265 V_{RMS}; output 5V/20A; boost inductor L_B = 150 μH (each winding); CS inductor L_1=120 μH (each winding of the two windings coupled on the same core); transformer winding $N_P/N_1/N_S$=17/7/1; switching frequency f_s=100 kHz.

Figure 6.12 shows the simulated circuit waveforms at 90 V_{RMS} input, full load, while the range-switch SW is closed and the circuit is working in the voltage-doubler mode. Again, the top and bottom boost inductors L_{B1} and L_{B2} conduct current in each alternative half-line-cycle. Therefore, the boost capacitor C_{B1} and C_{B2} are charged alternatively. With 90 V_{RMS} input, the total output voltage $V_{B(min)}$=V_{CB1}+V_{CB2}=260 V_{DC}, which doubles the $V_{B(min)}$ in the CS-S^{2}PFC without VDR. In addition, the VD S^{2}PFC not only reduces the V_B range, but also improves the converter performance. The detailed comparison between the CS-S^{2}PFC and VD CS-S^{2}PFC will be given in Section 6.5.

6.3.3 CCM VS-S^{2}PFC with VDR

Figure 6.13(a) shows the CCM VD VS-S^{2}PFC converter with the VS capacitor C_{r1} and C_{r2} in the top and bottom PFC cells. This converter is simulated with following specifications and key parameters: V_{in} = 90 – 135 V_{RMS} and 180 – 265 V_{RMS}; output 5V/20A; boost inductor L_B = 150 μH (each winding); VS capacitor $C_{r1,2}$= 8.1 nH; transformer winding $N_P/N_1/N_S$=17/8/1; switching frequency f_s=100 kHz. Figure 6.13(b) shows the simulated circuit waveforms at 100$V_{RMS,}$ full load. The total output voltage V_B= V_{CB1}+V_{CB2}=280 V_{DC}, which also double the capacitor voltage V_B at low line range in the VS S^{2}PFC converter without VDR.

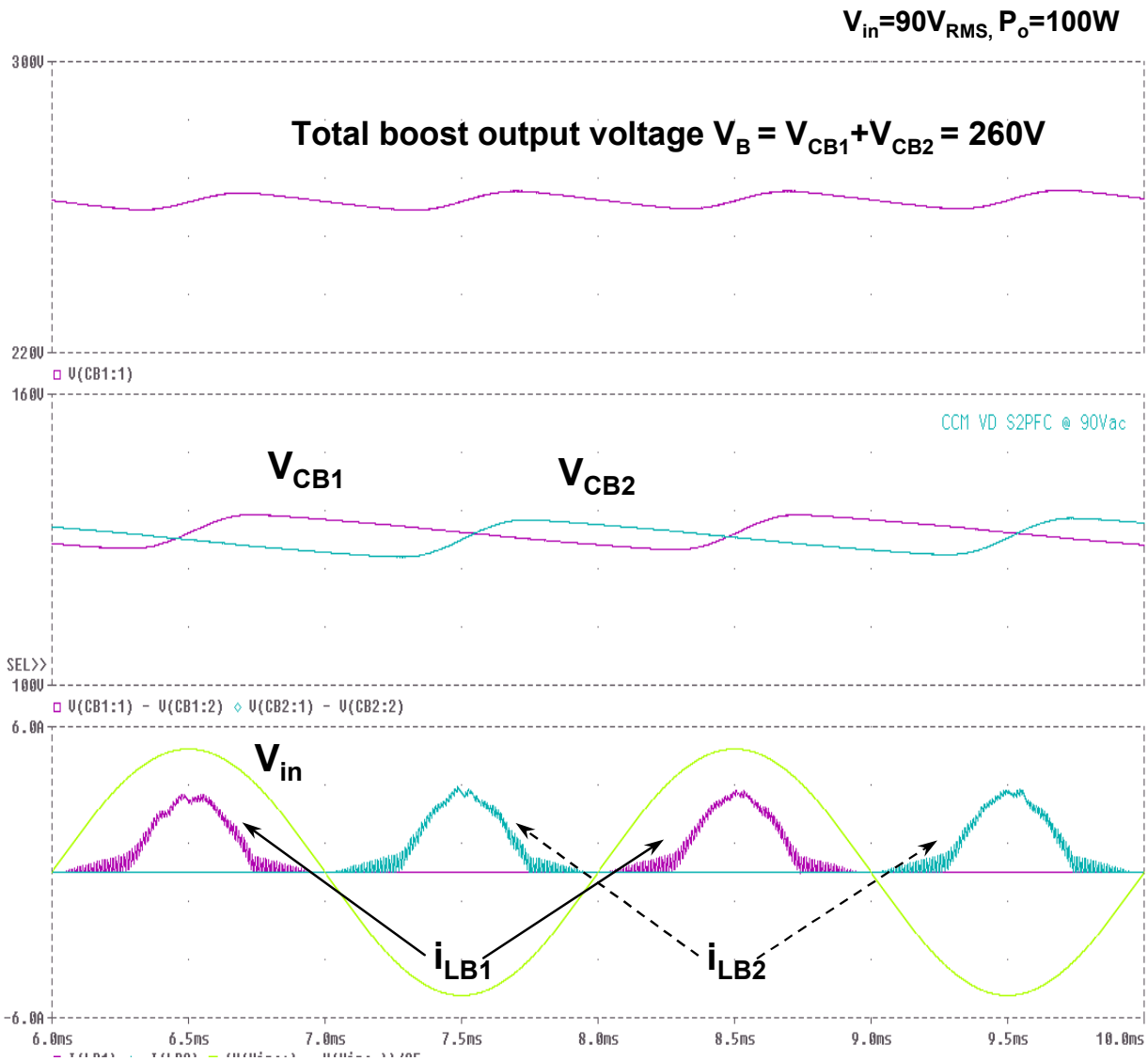


Figure 6.12 Simulated circuit waveforms of the CCM VD CS-S^{2}PFC converter

(at V_{in}=90V_{RMS}, Output 5V/20A, f_s=100 kHz)

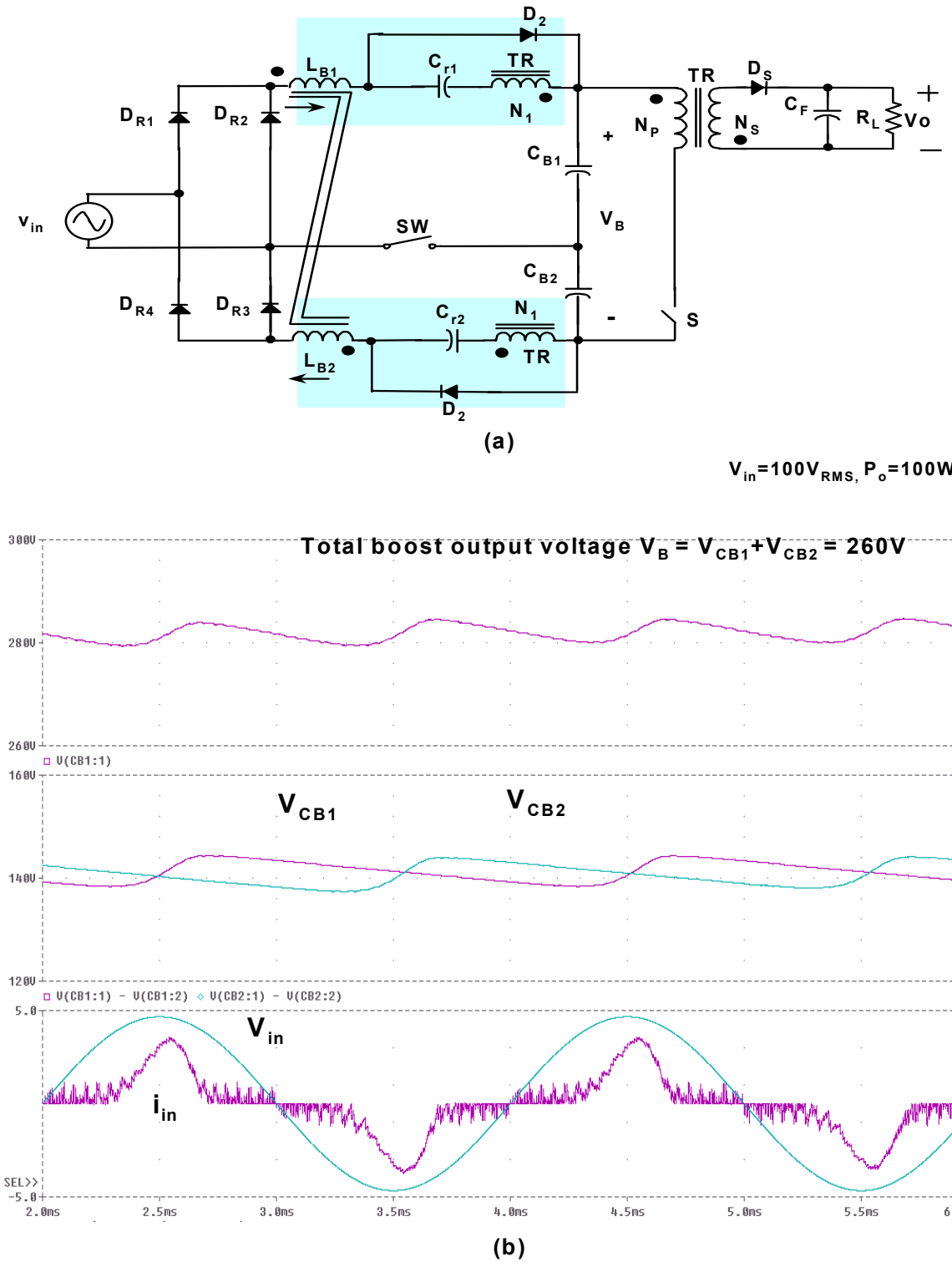


Figure 6.13 CCM VD VS-S^{2}PFC converter and its simulated circuit waveforms (at V_{in}=100V_{RMS}, Output 5V/20A, f_s=100 kHz)

(a) Circuit diagram, and (b) Simulated circuit waveforms

6.4 EXPERIMENTAL VERIFICATIONS

6.4.1 Single-switch DCM VD S^2PFC prototype with 5V/20A (100W) output [E1]

The performance of the proposed VD S^2PFC technique was first verified experimentally on a 100-W (5V/ 20A) prototype circuit designed for the universal-line range (90-264 V_{RMS}). The boost inductor in this circuit is operated in the DCM mode. The circuit diagram of the power stage of the experimental circuit along with the values of the components is shown in Fig. 6.14. The control circuit was implemented using the low-cost integrated controller UC3842. The switching frequency was 100 kHz. Measured line-voltage and line-current waveforms at nominal low line (V_{in} = 100 V_{rms}) and nominal high line (V_{in} = 230 V_{rms}), at full load (I_o = 20 A) are shown in Fig. 6.15. The measured individual line-current harmonics are well below the IEC1000-3-2 Class-D limits, i.e., they have more than 30% margin for both the nominal low line and high line. Table 6.1 summarizes the full-load power-factor (PF), total-harmonic-distortion (THD), bulk-capacitor-voltage ($V_B = V_{CB1} + V_{CB2}$), and efficiency measurements that include electromagnetic interference (EMI) filter and in-rush current limiter losses.

TABLE 6.1
MEASURED PF, THD, V_C, AND EFFICIENCY AT FULL LOAD

V_{in} [V_{rms}]	PF	THD [%]	$V_{C1}+V_{C2}$ [V]	η [%]
90	0.900	46.4	244	77.3
100	0.899	47.2	273	77.4
115	0.896	48.3	316	77.3
132	0.893	49.3	364	76.9
180	0.897	48.0	250	79.2
230	0.891	48.9	320	78.4
264	0.885	49.6	368	77.8

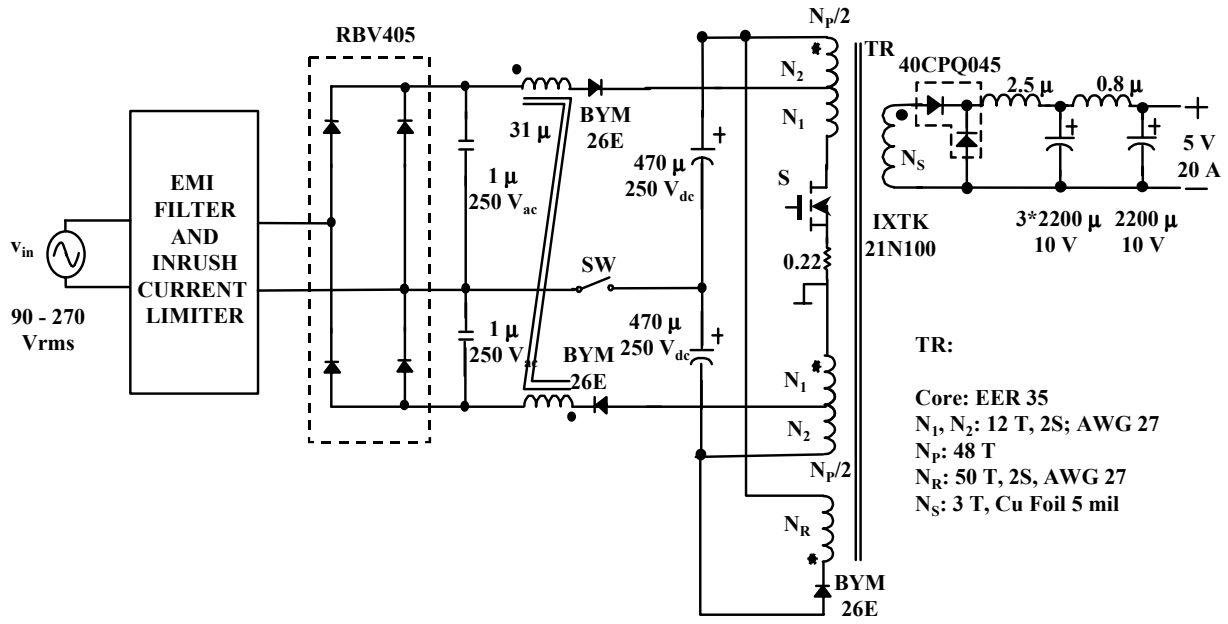


Figure 6.14 Experimental DCM VD S^{2}PFC circuit diagram [E1]

(V_{in}=90-135 / 180-265V_{RMS}, output 5V / 20A, switching-frequency f_S=100 kHz)

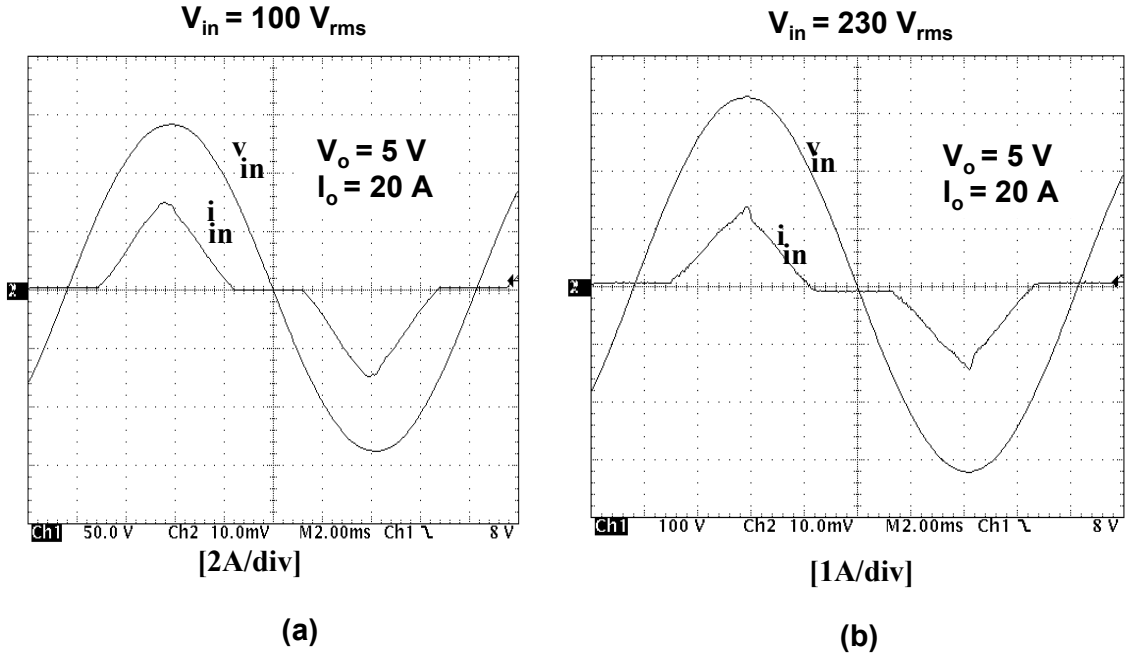


Figure 6.15 Measured input voltage and current waveforms of the DCM S^{2}PFC converter:

(a) at low line V_{in}=100 V_{RMS}, and (b) at high line V_{in}=230 V_{RMS}

To illustrate the improved performance of the proposed VD S^2PFC technique, the experimental results in Table 6.1 were compared with the measurements obtained on the corresponding 100-W (5V/20A) S^2PFC circuit with the conventional wide-range full-bridge rectifier implemented with a DCM boost inductor, reported in [B9]. It should be noted that the major components of the two S^2PFC circuits are identical. The maximum bulk voltage of the VD S^2PFC circuit in Fig. 6.14 at full load (I_o = 20 A) is about 40 V smaller than the maximum V_B of the corresponding S^2PFC circuit in [B9]. Also, the full-load efficiency of the VD S^2PFC circuit in Fig. 6.14 is around 4% higher than the efficiency of the corresponding S^2PFC circuit in [B9]. These improvements are the consequence of the significantly narrower bulk-capacitor voltage range of the VD S^2PFC circuit in Fig. 6.14 compared to the S^4ICS circuit with the conventional wide-range full-bridge rectifier in [B9].

6.4.2 Single-switch CCM VD CS-S^2PFC prototypes with 5V/40A (200W) output

For applications with high output power level, such as desktop computer power supply (i.e. silver box, P_o=150-200 W), it is necessary to use the CCM VD S^2PFC circuits. To experimentally verify the performance of the CCM VD S^2PFC converters, a universal-line-input, 5V/40A-output 2-terminal VD CS-S^2PFC prototype was built and tested. The circuit diagram of the power stage of the experimental circuit is shown in Fig. 6.16. The key experimental circuit components have been chosen as follows: L_B: 100 μH (each winding), L_1: 45 μH (each winding), N_1 = 14 T, N_p = 52 T, N_r = 52 T and N_s = 3 T, $C_{B1,2}$: 470 uF/250V, switch S: IXYS 12N100 and Schottky diode $D_{S1\text{-}2}$: IR81CND45, switching frequency fs=70kHz.

Measured line-voltage and line-current waveforms at nominal low line (V_{in} = 100 V_{rms}) and nominal high line (V_{in} = 230 V_{rms}), at full load (I_o = 40 A) are shown in Fig. 6.17.

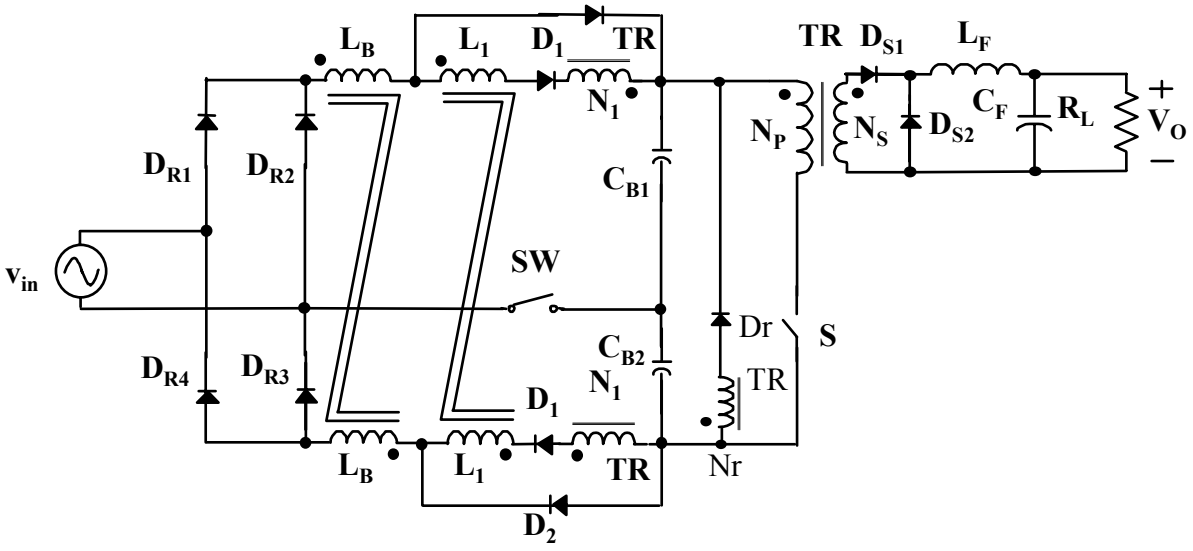


Figure 6.16 Experimental circuit diagram of the 200W CCM VD CS-S^{2}PFC converter

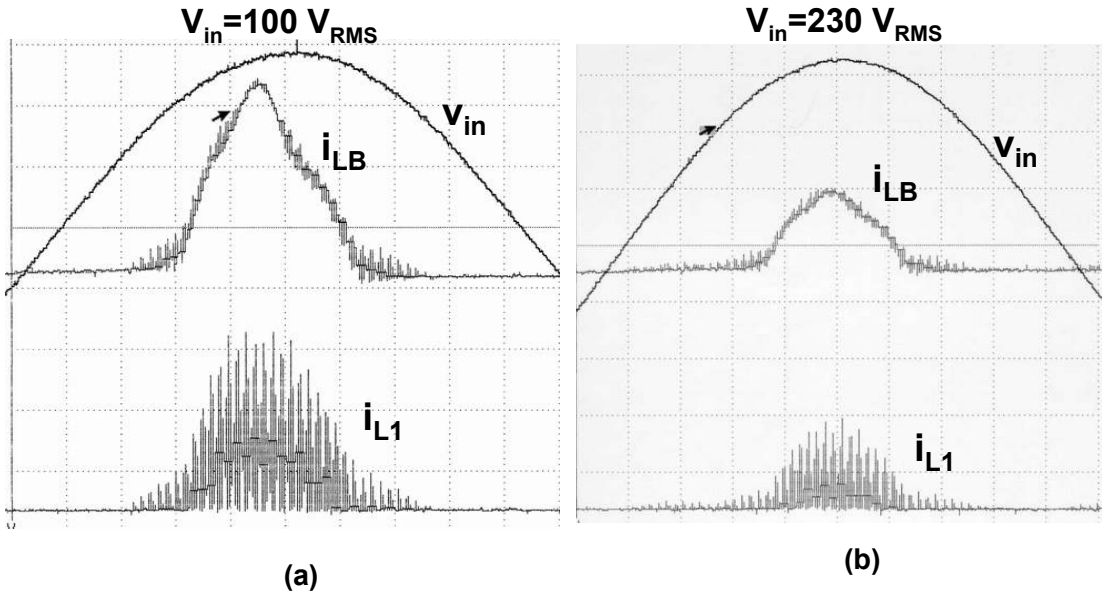


Figure 6.17 Measured input voltage v_{in}, boost inductor current i_{LB} and CS inductor current i_{L1} waveforms (at nominal line, output 5V/40A)

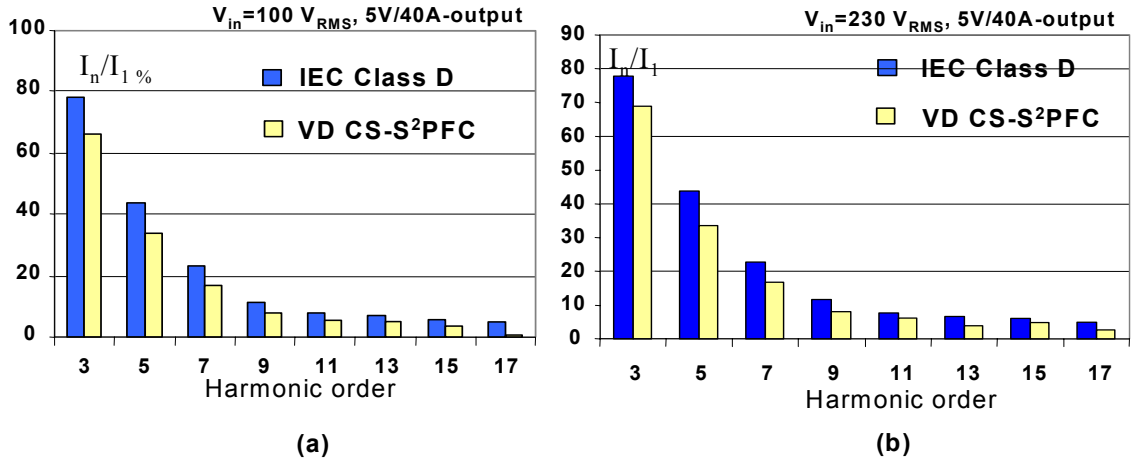


Figure 6.18 Measured input current harmonics of the VD CS-S^{2}PFC at nominal line

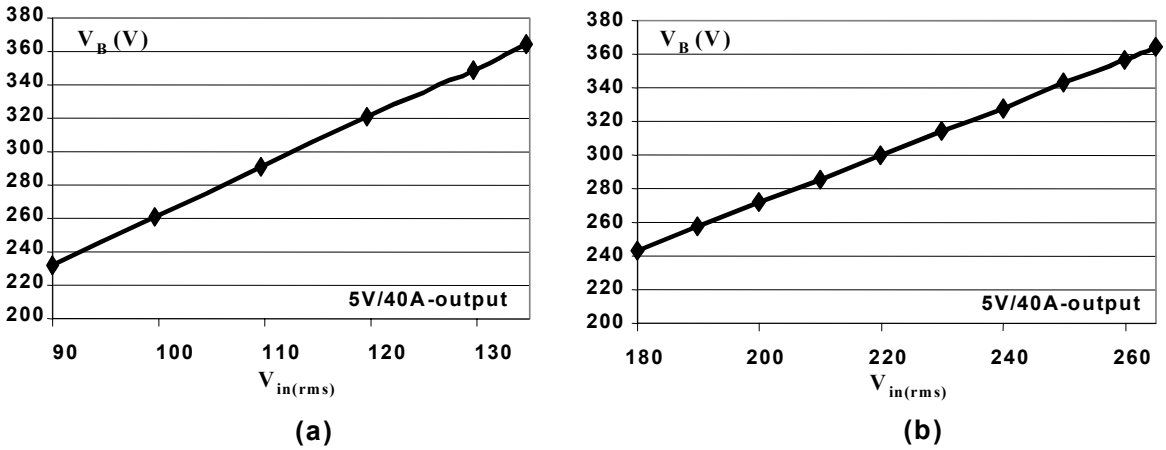


Figure 6.19 Measured bulk-capacitor voltage V_B at full load (I_o=40A)

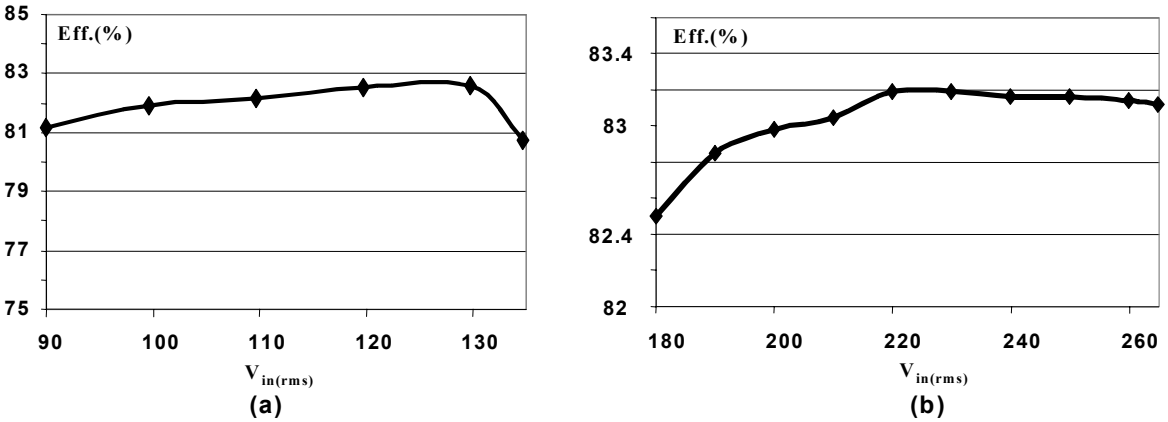


Figure 6.20 Measured full load efficiency of the VD CS-S^{2}PFC converter (Output-5V/40A)

Figure 6.18 shows that the input current of the CCM VD S^2PFC converter can meet IEC Class D and its corresponding Japanese harmonics standards with sufficient margins. As shown in Fig. 6.19, the bulk-capacitor voltage V_B is in the 230 – 370 V_{DC} range at full load (I_o=40A) and with universal-line input. The maximum V_B at 265 V_{RMS} input and light load is less than 430 $V_{DC,}$ which leaves enough voltage margins for two 250 V-rated electrolytic capacitors C_{B1} and C_{B2}. Figure 6.20 show the full-load converter efficiency in both the 90-135 V_{RMS} and 180-265 V_{RMS} line voltage range. As shown in Fig. 6.20(a), with 5 V output, the lowest efficiency is above 81% at 90 V_{RMS} input. Its efficiency is about 8-9 % higher than the CS S^2PFC converter without VDR, as reported in Section 4.4.2.5.

Another 3-terminal VD CS-S^2PFC converter prototype was also built and tested. The test results show the similar performance as the 2-terminal circuit shown in Fig. 6.16.

6.4.3 Two-switch CCM VD CS-S^2PFC prototypes with 5V/90A (450W) output

Without VDR, the existing S^2PFC converters require large hold-up capacitance and have low efficiency with universal line input. As reported in [B1]-[B19], the maximum power level of these converters is limited to be around 100-200 W range. Even though, the proposed CCM VD S^2PFC converter in Section 4.4.2 shows superior performance with single-switch and up to 200W (5V/40A)-output power. To verify the VD S^2PFC concept for applications which requires higher output power, such as low-end server power supplies, a 5V/90A-output CCM VD S^2PFC prototype has been built and tested. Figure 6.21 shows the circuit diagram of the S^2PFC converter with the voltage-doubler rectifier front-end and the CCM S^2PFC converter implemented with the two-switch forward converter dc/dc output power stage.

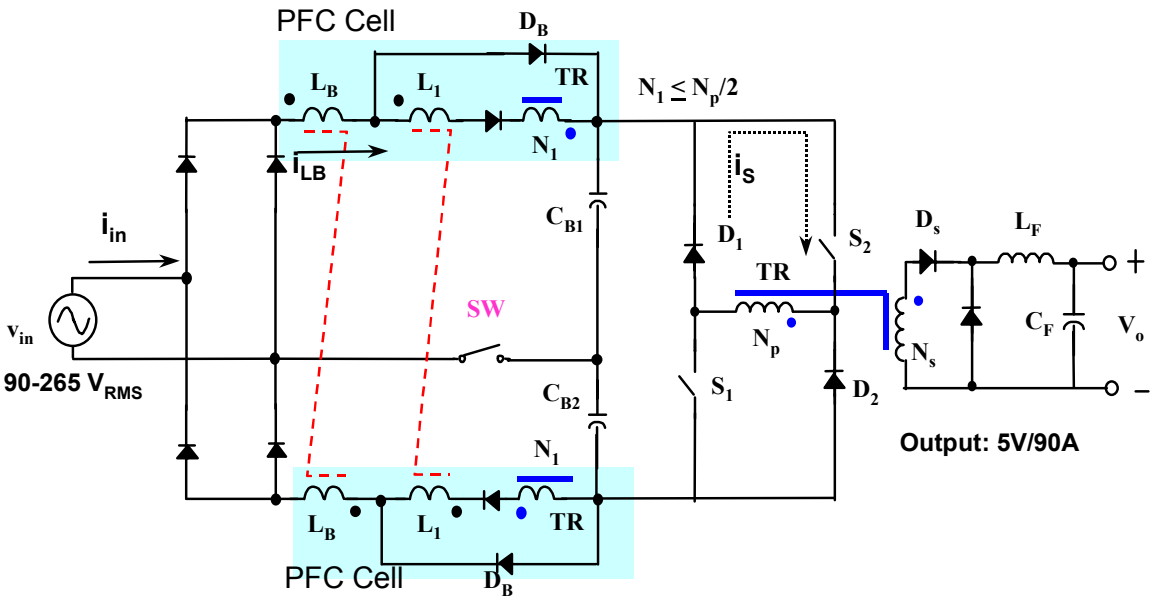
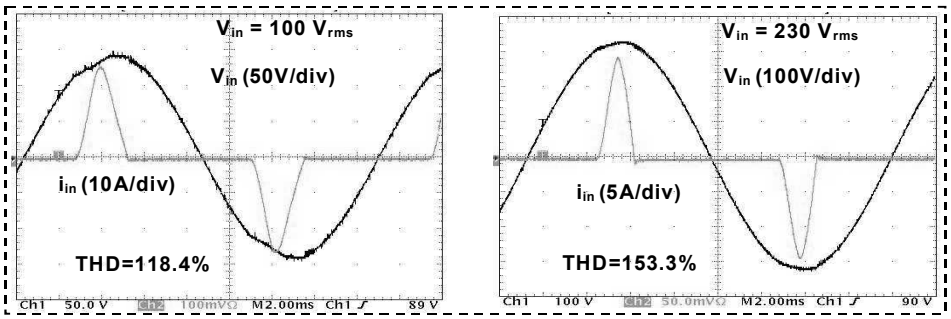
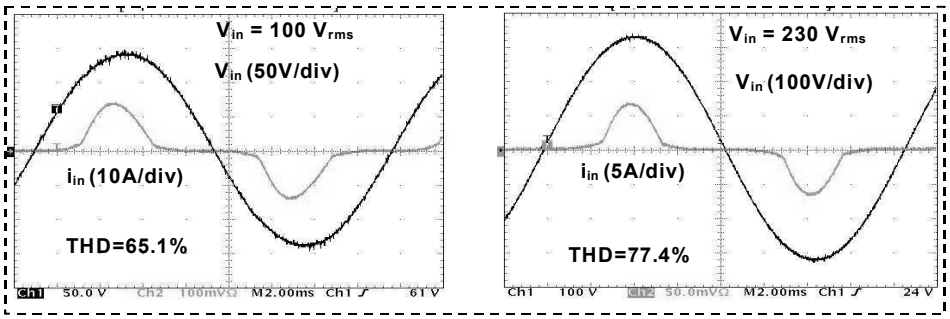


Figure 6.21 Circuit diagram of the universal-line input, 5V/90A-output CCM VD S²PFC prototype converter



(a)



(b)

Figure 6.22 Measured full load input current and voltage waveforms of:

Diode-rectifier W/O PFC; (b) VD-S²PFC converter

To verify the operation and performance of the proposed CCM VD-S^2PFC circuit shown in Fig. 6.21, the following key components were used in the implementation of the experimental circuit: $C_{B1,2}$ – 1000 μF/250 V; L_B – 40 μH(each winding)/Philips 3F3 E41/17/12 core; L_1 – 34 μH(each winding)/Philips 3F3 E41/17/12 core; Transformer TR – Philips 3F3 E42/21/15 core, N_p=34 T, N_s=2 T, N_1=9 T, which provides a feedback winding ratio k=0.47; switches $S_{1,2}$ – IRPF460 MOSFET; diode $D_{1,2}$–DSEP8-06 A; low voltage rectifier-diodes $D_{S1,2}$–2*81CNQ45; L_F –3 μH/120 $A_{(pk)}$; C_F – 4*2200 μF/16 V. The switching frequency was 70 kHz.

To determine how the introduction of PFC impacts the performance of the conventional diode-capacitor rectifier converter, the experimental circuit was first tested with L_1 opened and L_B shorted, i.e., without PFC function. Then the circuit was tested again with inductors L_B and L_1 connected. Figures 6.22(a) and (b) show the tested input current and voltage waveforms of the diode-capacitor rectifier circuit (no PFC) and the VD-S^2PFC circuit, respectively. As shown in Fig. 6.22(a), the input current in the diode-capacitor rectifier has high distortions because of its high peak and narrow conduction angle. Figure 6.22(b) verifies that the VD-S^2PFC converter reduces the input current peak and increases the input current conduction angle. As the result, the input current of the VD-S^2PFC converter has much lower THD than that in the diode-capacitor rectifier front end without PFC.

Figure 6.23 shows the comparison of the harmonic-current limits spelled out in the IEC1000-3-2 / Class D (and corresponding Japanese) document and the measured current harmonics of the diode-rectifier circuit and the VD-S^2PFC converter. As can be seen from Fig. 6.23, the diode-rectifier cannot meet the harmonic limits, while the VD-S^2PFC converter can meet the standards with sufficient margins.

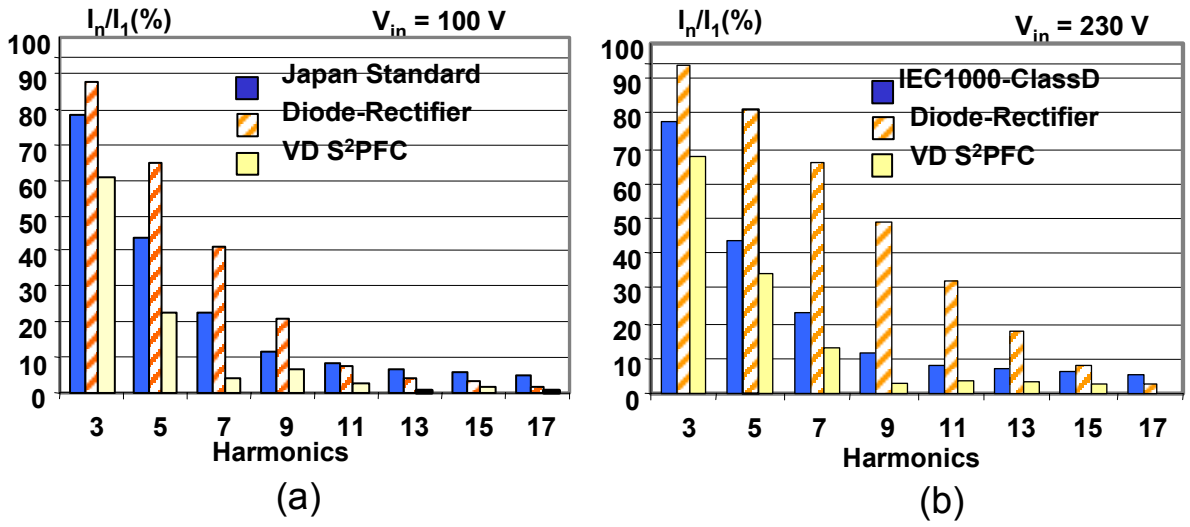


Figure 6.23 Input current harmonics comparison @ full load V_{in}=100V_{ac}; (b) V_{in}=230V_{ac}

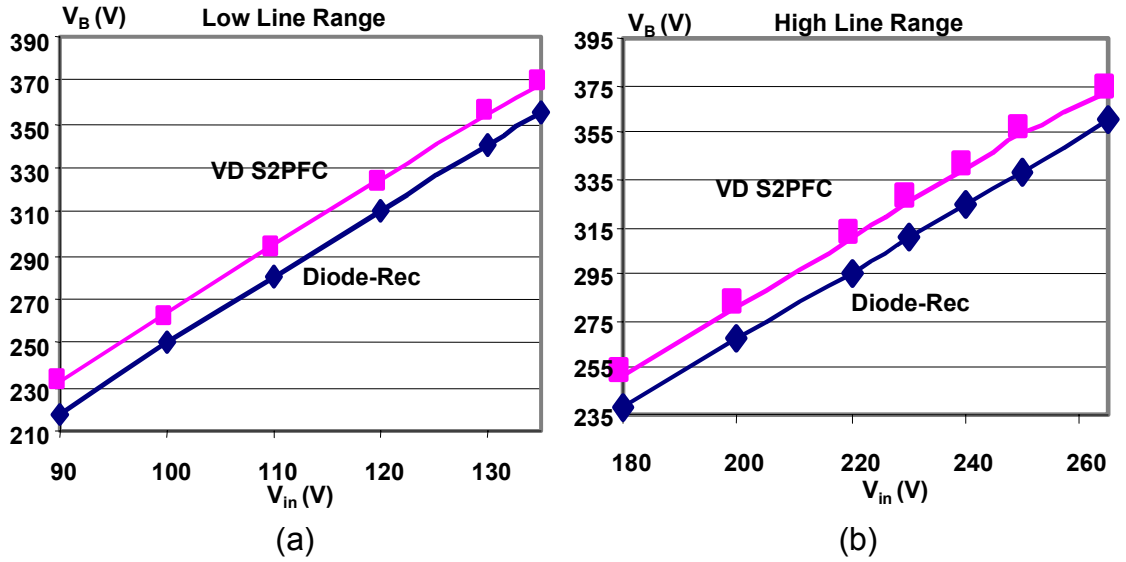


Figure 6.24 Total boost capacitor voltage comparison @ full load: (a)V_{in}=90-135 V_{ac}; (b) V_{in}=180-265 V_{ac}

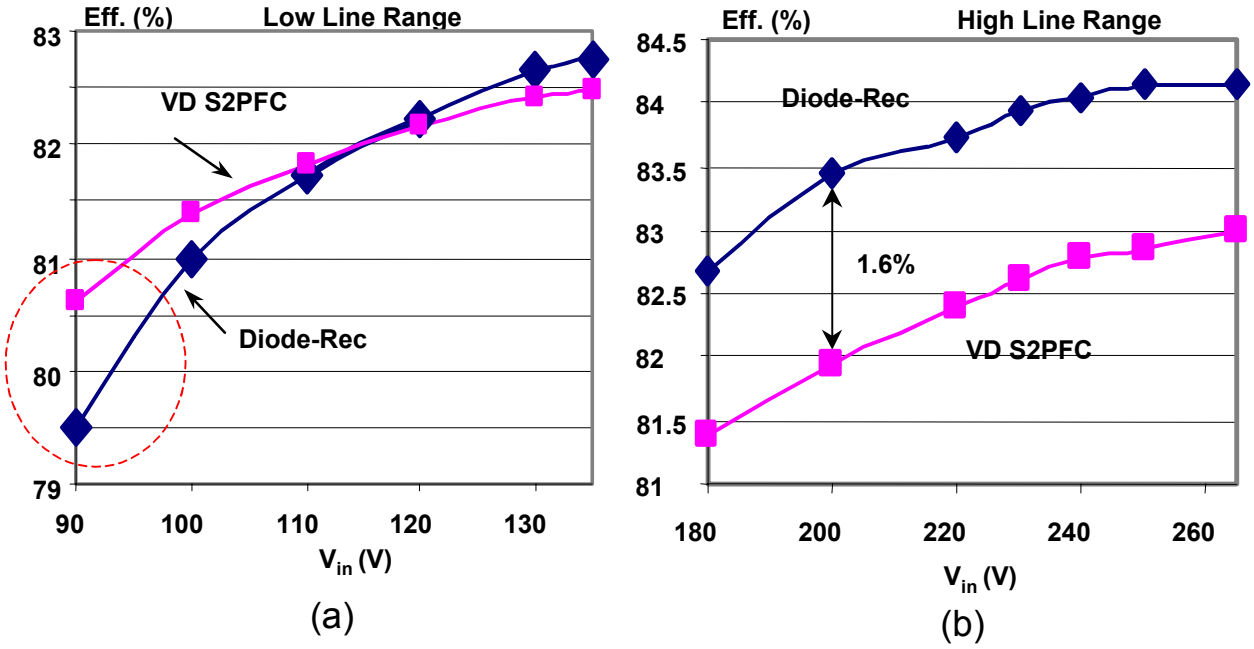


Figure 6.25 Converter efficiency (EMI filter included) comparison @ 5V/90A output: (a)V_{in}=90-135V_{ac}; (b) V_{in}=180-265V_{ac}

Figure 6.24 shows the comparison of total bulk-capacitor voltage V_B at the full-load for both the low and high input line ranges. As can been seen, by introducing S^2PFC into the conventional diode-capacitor rectifier, the full load bulk-capacitor voltage increases for about 20 V with the boost action in S^2PFC. The measured maximum total bulk-capacitor voltage, which occurs at the light load, is less than 420 V with 265 V_{ac} input. This provides a sufficient voltage margin for two 250-V rated capacitors C_{B1} and C_{B2} in series connection.

Figure 6.25 shows the efficiency comparisons in the low-line and high-line range. As can be seen, at full power (5V/90A) both converters exhibit efficiencies of around 80%. Theoretically, adding a PFC stage into the diode-capacitor rectifier converter should reduce the overall efficiency because power will be processed through an additional stage. This is also true for the S^2PFC converters. As can been seen from Fig. 6.25(b), in the high-line range, the VD S^2PFC reduces the efficiency for about 1.6%. However, this does not represent a drawback of VD S^2PFC converter since at the minimum line voltage, which due to the lowest efficiency determines the thermal design, the VD S^2PFC converter exhibits 1% higher. There are two reasons that the VD S^2PFC has better efficiency than diode rectifier at low line. First, as can been seen from Fig. 6.22, the VD-S^2PFC converter significantly reduces the peak of the input current, which reduces the loss on the rectifier-diode-bridge and EMI filter. Second, as explained previous chapters, the windings N_1 in the VD S^2PFC converter introduces a "direct-energy-transfer" path that further reduces the switch current stress.

In conclusion, the VD S^2PFC technique provides a simple approach to modify the conventional power supply with VDR to meet the IEC class D harmonic limits. The modified converter can improve the input current while still maintain the similar capacitor voltage range and conversion efficiency, with minimum number of added component count.

6.5 COMPARISON AND EVALUATION OF THE VD S^{2}PFC TECHNIQUE

To evaluate the VD S^{2}PFC techniques, the comparison among the CCM two-stage boost PFC, the S^{2}PFC (without VDR), and the VD S^{2}PFC techniques have been done. The circuits for comparison are shown in Fig. 6.26. Namely, Fig. 6.26(a) is the two-stage PFC with CCM boost rectifier, Fig. 6.26(b) is the CCM CS-S^{2}PFC converter and Fig. 6.26(c) is the proposed CCM VD CS-S^{2}PFC converter. The comparison was performed under following conditions:

- Input voltage is universal-line voltage from 90 – 265 V_{RMS}.
- Output voltage is 5 V, and output power is in the range from 100 W to 450W.
- 10 ms hold-up time is required.
- In the VD S^{2}PFC, feedback-winding ratio $k = (N_P - 2N_1)/N_P = 0.45$ is used. Due to the difficulty to meet IEC limits, no feedback-winding is used in the S^{2}PFC converter.

6.5.1 Comparison of bulk-capacitor voltage and hold-up capacitance

Figure 6.27 shows the comparison of the bulk-capacitor voltage V_B vs. the input voltage v_{in}, at the full-load output. As shown, V_B in the two-stage PFC is regulated at 400 V_{DC} in the whole line range, while V_B in the S^{2}PFC converter is in the 130-370 V_{DC} range and V_B in the VD S^{2}PFC converter is in the 260 – 400 V_{DC} range. Based on V_B at 90 V_{RMS} input voltage, the hold-up capacitance can be calculated with Eq. (5.1). Figure 6.28 shows one comparison of the hold-up capacitance for P_o=100 W. The S^{2}PFC converter needs seven times larger capacitance than needed by the conventional two-stage PFC converter. By integrating the VDR with the S^{2}PFC converter, the hold-up capacitance is significantly reduced, i.e., it is only about twice of that for the two-stage PFC converter. As a result, with VDR, the application of S^{2}PFC techniques becomes feasible even at higher power levels.

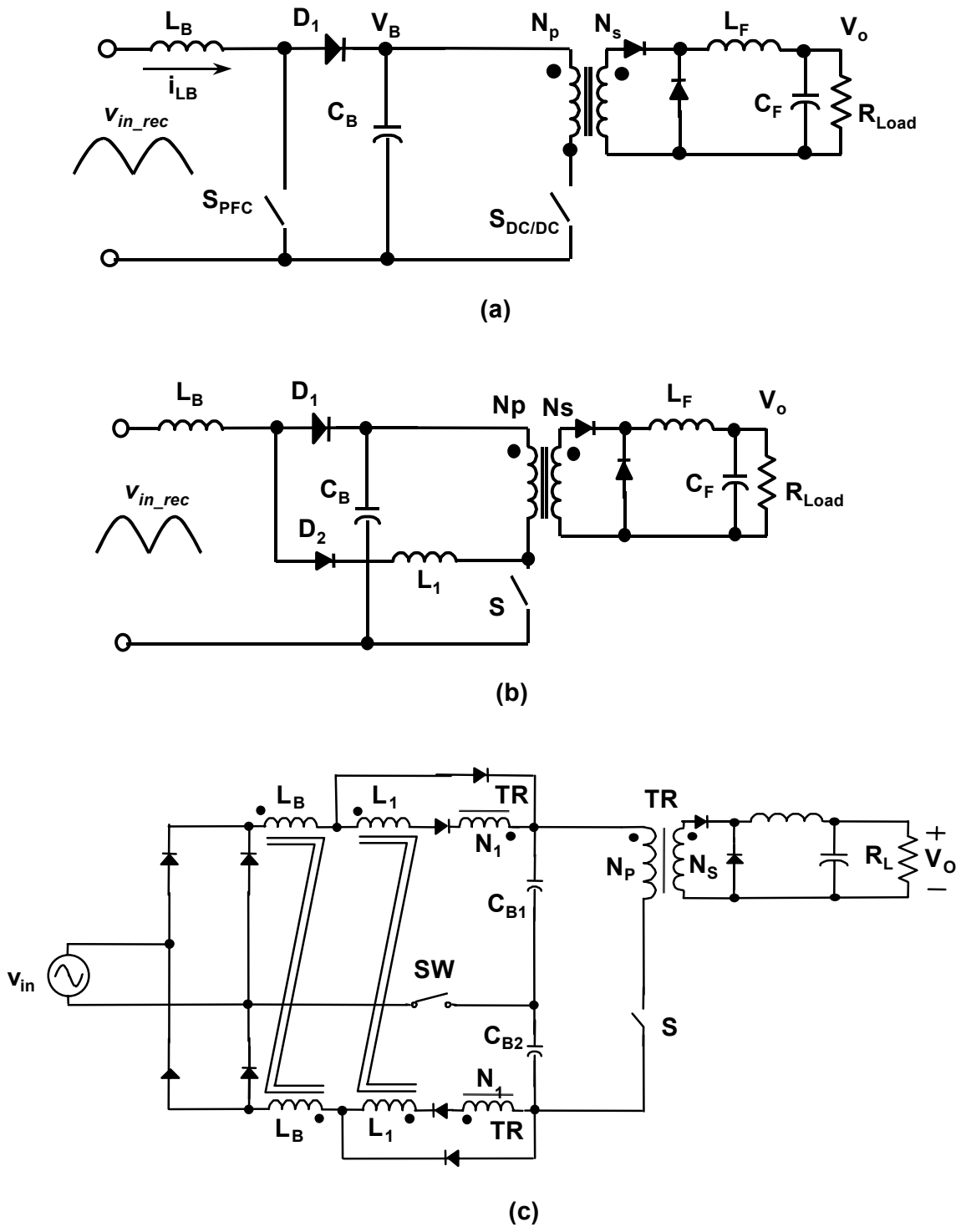


Figure 6.26 Typical example circuits for comparison:

(a) two-stage CCM boost PFC converter, (b) CCM CS S^2PFC converter, (c) CCM VD CS-S^2PFC converter

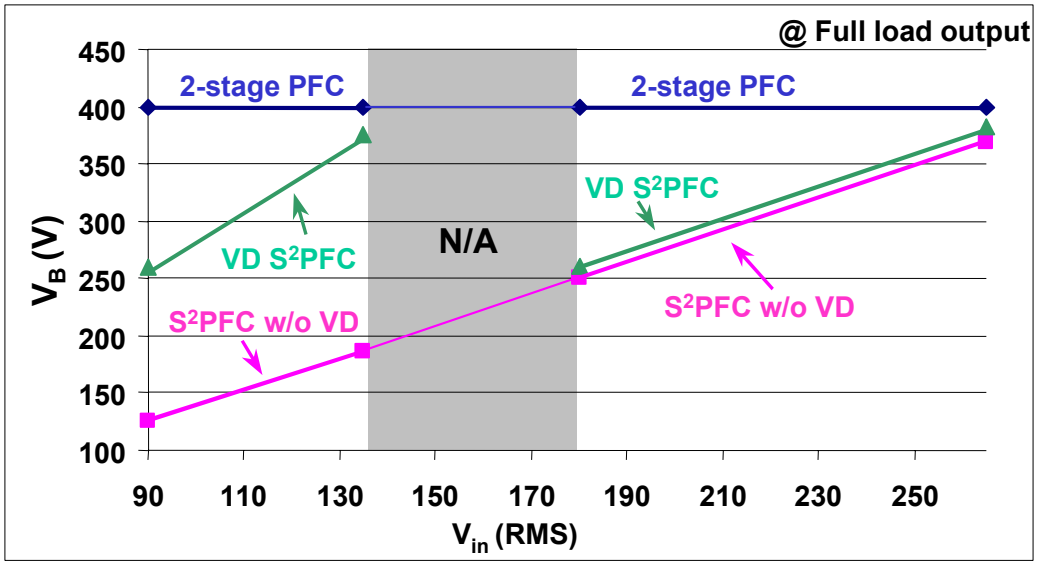


Figure 6.27 Bulk-capacitor voltage range comparison (at full load output)

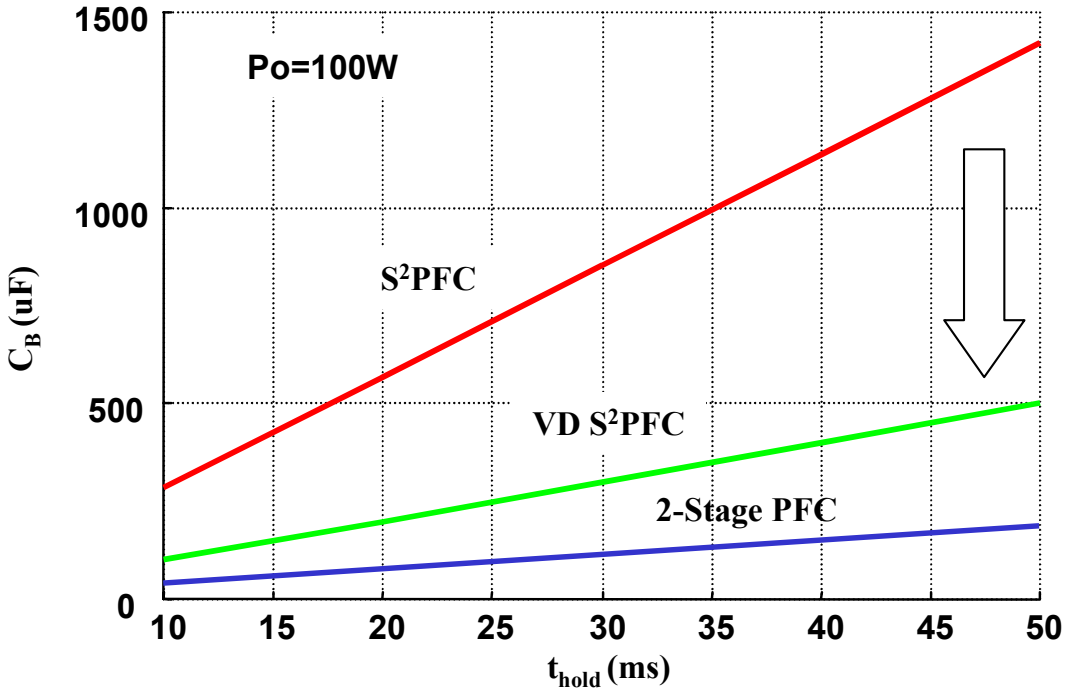


Figure 6.28 Hold-up capacitance comparison (P_o=100W)

6.5.2 Comparison of the inductors

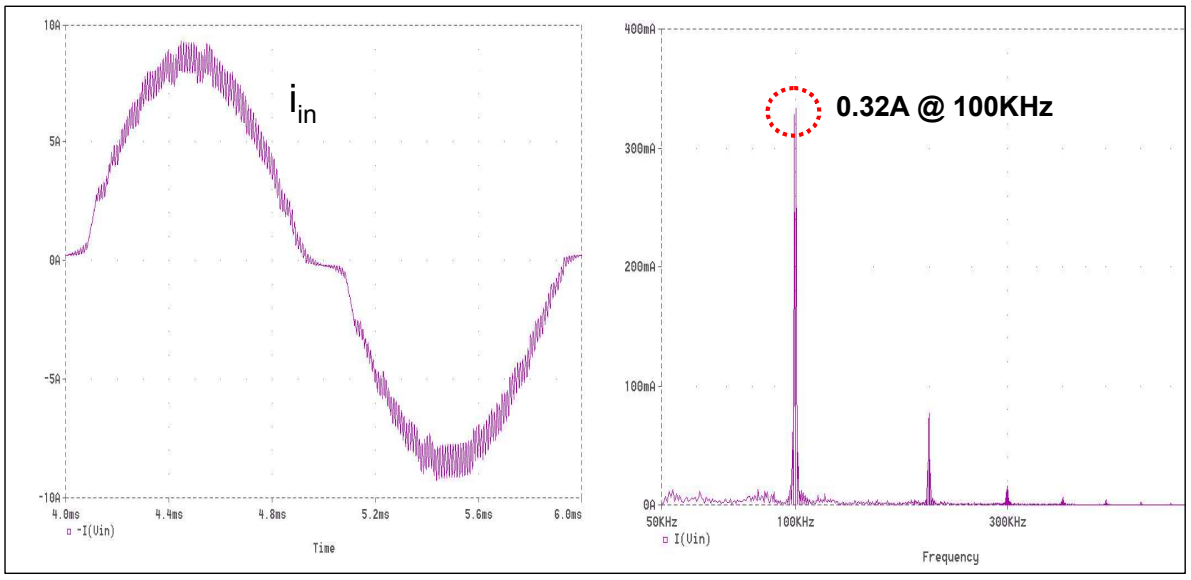
6.5.2.1 PFC inductor size comparison between the two-stage PFC and VD S^2PFC converters

The comparison of the PFC inductors is performed at 450 W. Since the VD S^2PFC has two PFC inductors and the CCM boost PFC rectifier only has one PFC inductor, the total magnetic core sizes are calculated for comparison. To fairly compare the PFC inductors in two converters, the two converters are designed to have the same ripple current and the same switching frequency, i.e., the same differential mode (DM) EMI filters.

Figure 6.29 shows the simulated input current waveform and its spectrum for the CCM boost rectifier in the two-stage PFC converter, whereas Fig.6.30 shows the simulated input current waveform and its spectrum for the VD S^2PFC converter. The design parameters of two inductors are listed in Table 6.2. The core is chosen according not only to the inductance, but also to the peak and RMS inductor current. Table 6.2 shows that the two-stage PFC and VD-S^2PFC converter requires a similar total core size, although the VD S^2PFC converter must have two inductors.

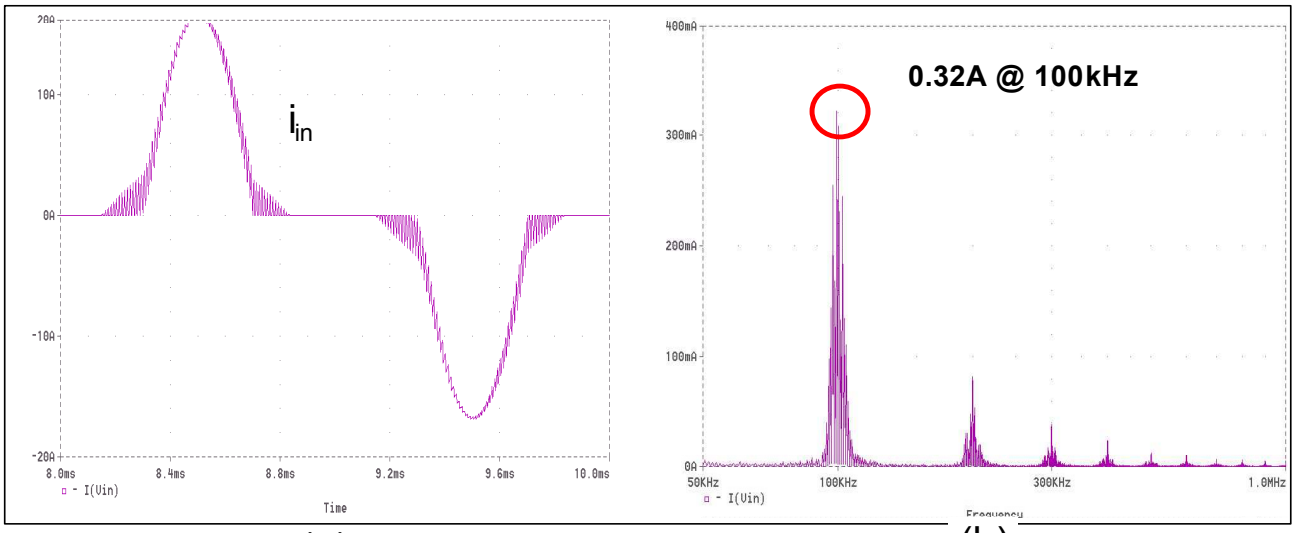
Table 6.2 Total PFC inductor(s) comparison @ Po=450W

	CCM boost inductor in two-stage PFC	PFC inductors in VD S^2PFC
Inductance (each winding)	L_B=430μH	L_B=40μH, L_1=21μH
Core selection	Philips 3F3 E42/21/15	L_B: Philips 3F3, E41/17/12 L_1: Philips 3F3, E30/15/7
Total core size	17.3 cm^3	15.5 cm^3



(a) (b)

Figure 6.29 Simulated CCM two-stage-PFC input current waveforms and its spectrum (Vin=90Vac, Po=450W, L_B=430µH, $i_{LB(pk)}$=9A)



(a) (b)

Figure 6.30 Simulated VD S^2PFC input current waveforms and its spectrum (Vin=90Vac, Po=450W, L_B=40µH each winding, $i_{LB(pk)}$=16A; L_1=21µH each winding, $i_{L1(pk)}$=16A)

6.5.2.2 Output filter inductance comparison

Since the output filter inductor L_F handle the similar DC current and peak current, the inductance comparison is enough to indicate the relative magnetic sizes. Figure 6.31 shows the output filter inductance comparison among the three PFC converters in Fig. 6.26. As can be seen, compared to the S^2PFC converter, the VD S^2PFC has reduced output filter inductance. Furthermore, the inductance difference between the two-stage PFC and VD S^2PFC is small.

6.5.3 Comparison of the semiconductors

6.5.3.1 Switch current stress comparison

When MOSFET switches are used, their RMS current determines the conduction loss. Figure 6.32(a) compares the RMS switch current of the three different circuits, at the low line and the output power is from 50 to 400W. Since the PFC switch has been eliminated in the S^2PFC and the VD-S^2PFC circuit, only the currents of the dc/dc converter switches are calculated. As can been seen, the current stress in the VD S^2PFC switch is just above one-third of that in the S^2PFC converter without the voltage-doubler rectifier. Moreover, the RMS switch current in the VD S^2PFC converter is also lower than the RMS PFC current i_{PFC} in the two-stage PFC converter. As to the power loss, Figure 6.32(b) compares the switch conduction losses in three different circuits. As shown in Fig. 6.32(b), the switch conduction loss of the VD S^2PFC converter is even much lower than the total switch conduction loss in the two-stage PFC converter.

There are two reasons why the VD-S^2PFC has a low current stress on the switch. First, compared to the S^2PFC converter without the voltage-doubler rectifier, the VD-S^2PFC converter doubles the boost capacitor voltage. As a result, the dc/dc transformer turn-ratio N_p/N_s in the VD S^2PFC is much higher than that in the S^2PFC converter without the voltage-doubler rectifier.

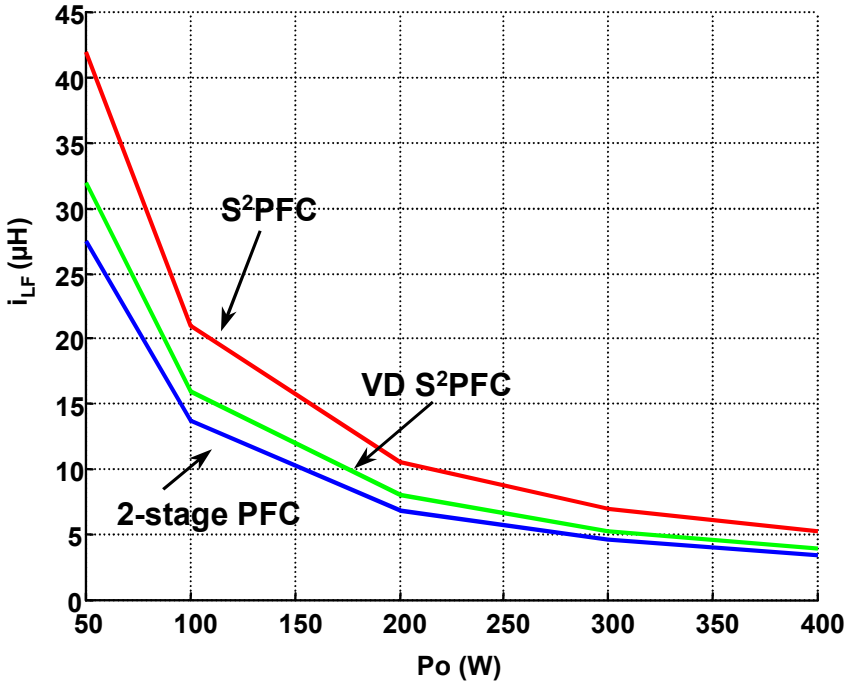


Figure 6.31 Output filter inductance comparison vs. the output power

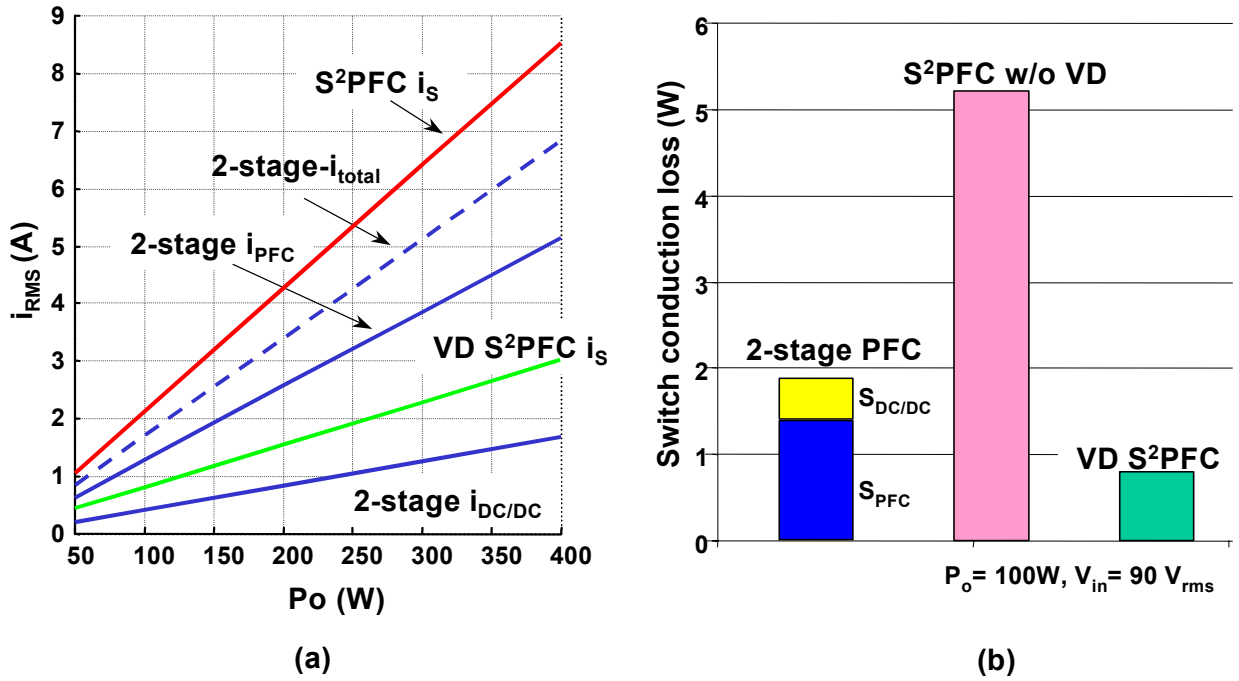


Figure 6.32 Switch RMS current comparison (V_{in}=90V_{ac}, full load 50-400W)

A higher N_p/N_s turn-ratio results in a lower value of the reflected output current to the primary side, which reduces current stress on the primary-side switches. Second, in both the S^2PFC and VD-S^2PFC converters, the low-line switch current is determined by Eq. (6.3):

$$i_S = i_{dc/dc} + i_{PFC} \cdot \frac{N_1}{N_p} \tag{6.3}$$

Since in a well-designed CCM VD CS-S^2PFC converter, N_1 is about 0.25-0.3 N_p, which is only half of N_1 in the CCM S^2PFC converter (without VD), the switch current stress are further reduced.

Furthermore, the switching losses related to the reverse recovery of the boost rectifier are reduced in the CCM S^2PFC converter because the ICS inductor L_1 reduces the di/dt of the boost diode. Therefore, the CCM S^2PFC converter has less boost diode reverse-recovery loss compared to that in the CCM two-stage PFC converter.

6.5.3.2 Diode current stress comparison

a) Boost diode

The voltage stresses on the PFC boost diodes are different in three different converters. For the two-stage PFC and S^2PFC converters, 600 V-rated fast-recovery diodes are used, while 300 V-rated diode is used in the VD-S^2PFC converter. Regardless, Fig. 6.33 shows the diode current stress comparison among three circuits at the worst case, i.e., 90 V_{RMS} input voltage and full load output. As can be seen, the VD S^2PFC has the lowest current stress on the boost diode. It is because that each diode only conducts current in half-line-cycle at low line, when the VDR range switch SW is closed. Furthermore, as discussed in previous section, the diode reverse-recovery loss is alleviated by the CS inductor L_1.

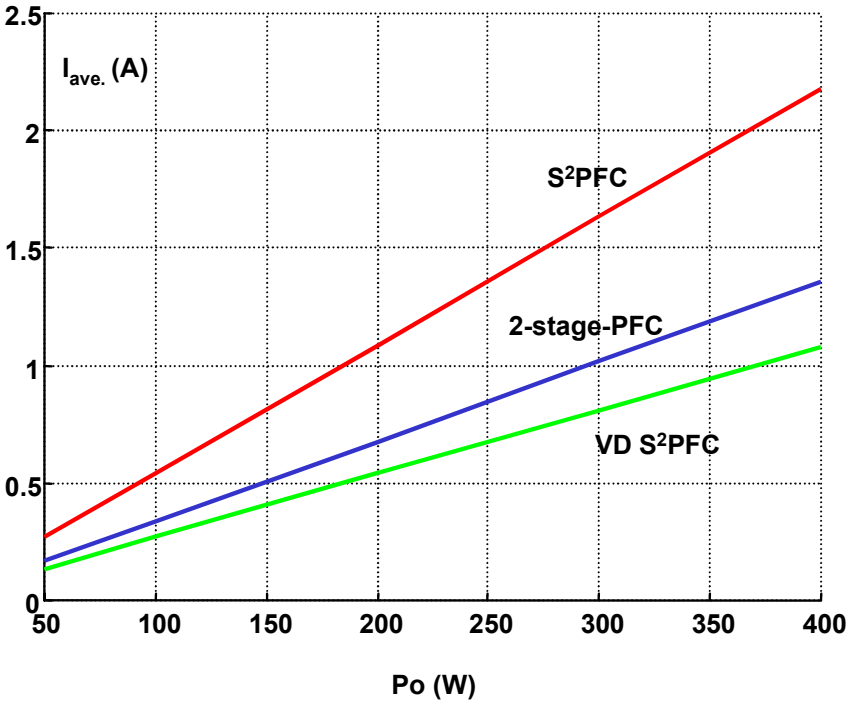


Figure 6.33 PFC boost diode average current comparison (at 90 V_{RMS} input)

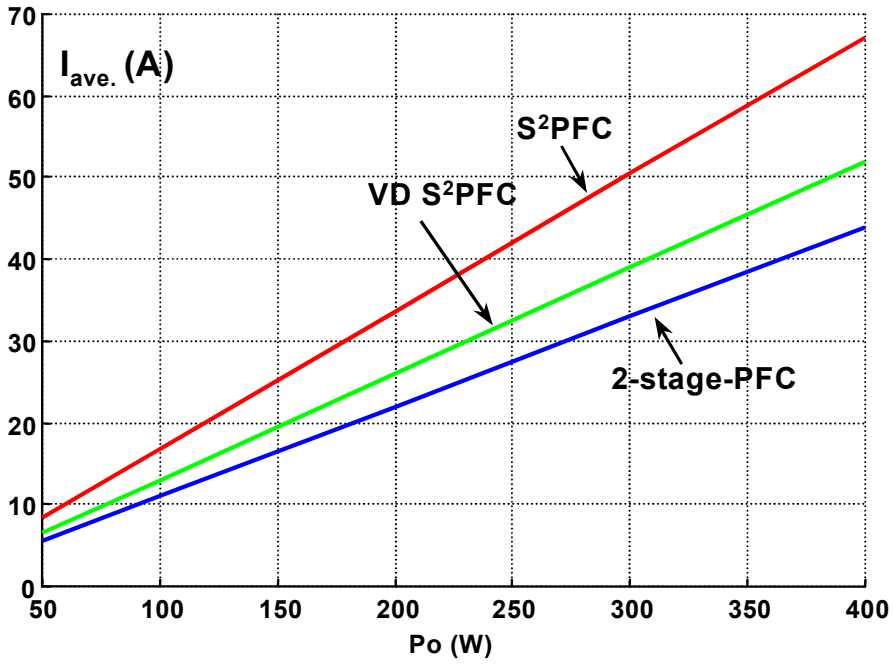


Figure 6.34 Output rectifier diode average current comparison

b) Output rectifier diode

Figure 6.34 shows the current stress comparison on the output rectifier diode. The averaged diode current was used. As can be seen, the VD S^2PFC converter reduces the output diode current stress on the S^2PFC converter by reducing the duty-cycle range. Even though, the VD S^2PFC still has slightly higher output diode current than the two-stage PFC.

6.5.4 Efficiency comparison

The conversion efficiency of three different converters has been measured experimentally from their prototype. For the CS-S^2PFC converter, due to its relatively low efficiency, the maximum output was designed as 5V/20A, while the 2-stage PFC and VD CS-S^2PFC are rated with 5V/40A output. Figure 6.35 shows the efficiency comparison in the full line range, in which the low line efficiency at 90 V_{RMS} input is the critical worst case for each converter. As can be seen, with the help of VDR, the VD S^2PFC converter increase the low-line efficiency up to 8-9% from the previous CS S^2PFC converter without VDR. Even more, with 90 V_{RMS} input voltage, the VD S^2PFC converter even has 2-3 % higher efficiency than the 2-stage PFC converter does.

There are several reasons that the VD S^2PFC has better efficiency. First, as shown in Fig. 6.32, the current stress on the VD S^2PFC is low. The reason has been explained in Section 6.5.3.1. Second, with VDR, a high bulk-capacitor voltage feedback winding ratio is used in the VD S^2PFC converter. A direct-energy-transfer path is provided by the feedback winding N_1. Third, the CS inductor L_1 alleviates the boost diode reverse-recovery loss, which also significantly improves the low-line efficiency of the CS VD S^2PFC converter.

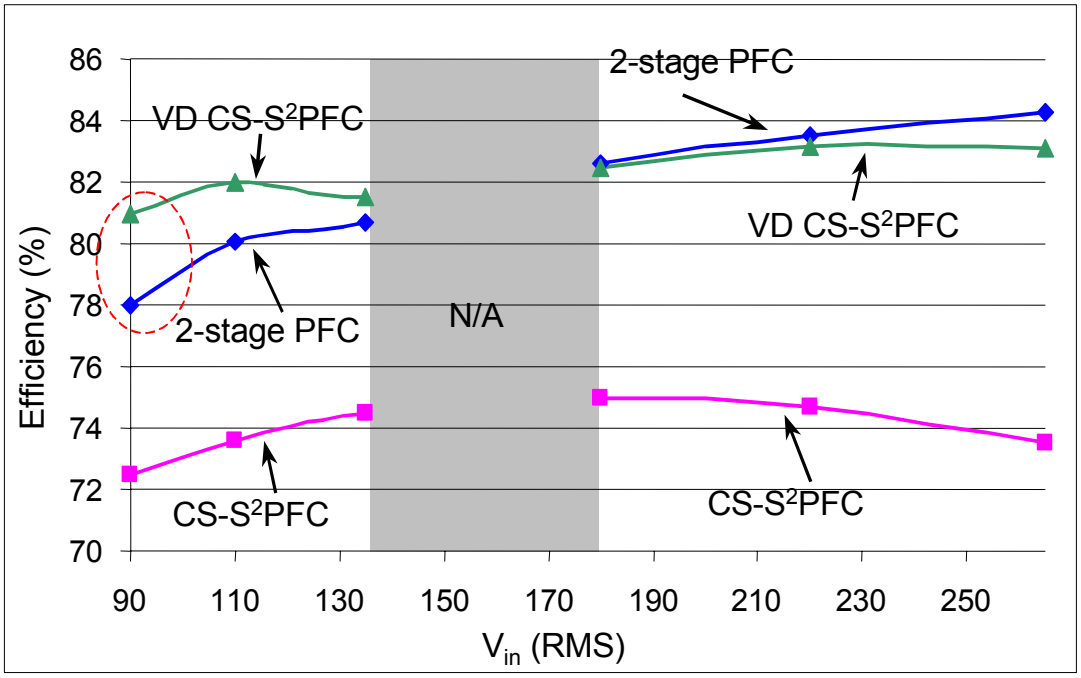


Figure 6.35 Measured efficiency comparison (Full load, 5V-output)

(CS-S^{2}PFC $P_{o(max)}$=100W, 2-stage and VD S^{2}PFC $P_{o(max)}$=200W)

6.6 SUMMARY

To solve the wide bulk-capacitor voltage range problem in the S^2PFC converters, this Chapter proposed a novel single-stage PFC technique which integrates the voltage-doubler-rectifier front end with the S^2PFC converters. Based on the feed-forward PFC cell concept, two families of voltage-doubler single-stage PFC (VD S^2PFC) converters have been developed: a VD S^2PFC family with 2-terminal PFC cells and a VD S^2ICS family with 3-terminal PFC cells. Generalized circuit diagrams and principles of operation of the VD S^2ICS converters are provided. Simulation results verified both the DCM and CCM VD S^2PFC techniques. Experimental results obtained on the 100W (5V/20A), 200W (5V/40A) and 450W (5V/90A) prototype circuits are given to verify the performance improvements.

After that, in order to evaluate the proposed VD S^2PFC technique, a comprehensive comparison among the CCM two-stage PFC converter, the CCM S^2PFC converter and the proposed CCM VD S^2PFC converter has been done with universal-line input. The results show that, with voltage-doubler rectifier front-end, the VD S^2PFC converter significantly reduce the S^2PFC converter hold-up capacitance. Compared to two-stage PFC converter, the S^2PFC converter needs 7 times larger capacitance, while the VD S^2PFC converter reduces it to twice larger capacitance. Besides, the VD S^2PFC converter has even lower switch conduction loss than that of the two-stage PFC converter. The experimental data show that the VD S^2PFC converter has 8-9% higher efficiency than that of the S^2PFC converter. Furthermore, the low line efficiency of VD S^2PFC is even 2-3% higher than that of the conventional two-stage PFC converter. In conclusion, it was found that the CCM VD-S^2PFC may be a cost-effective solution for universal-line power supplies with an input power up to 600 W, which is the maximum power required by IEC1000-3-2 Class D standards.