Anisotropic Etching for Silicon Micromachining

by

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Thesis submitted to the faculty of the

Virginia Polytechnic Institute and State University

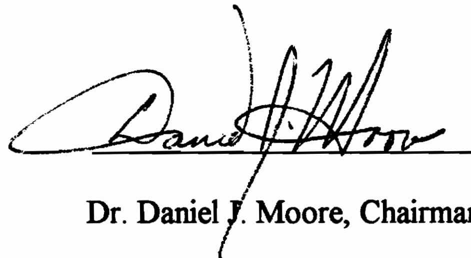
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

APPROVED:



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Abstract

Silicon micromachining is the collective name for several processes by which three-dimensional structures may be constructed from or on silicon wafers. One of these processes is anisotropic etching, which utilizes etchants such as KOH and ethylene diamine pyrocatechol (EDP) to fabricate structures from the wafer bulk. This project is a study of the use of KOH to anisotropically etch (100)-oriented silicon wafers. The thesis provides a thorough review of the theory and principles of anisotropic etching as applied to (100) wafers, followed by a few examples which serve to illustrate the theory. Next, the thesis describes the development and experimental verification of a standardized procedure by which anisotropic etching may be reliably performed in a typical research laboratory environment. After the development of this procedure, several more etching experiments were performed to compare the effects of various modifications of the etching process. Multi-step etching processes were demonstrated, as well as simultaneous double-sided etching using two different masks. The advantages and limitations of both methods are addressed in this thesis. A comparison of experiments performed at different etchant temperatures indicates that high temperatures (80° C) produces reasonably good results at a very high etch rate, while lower temperatures (50° C) are more suited to high-precision structures since they produce smoother, higher-quality surfaces.

Acknowledgments

This thesis project would not have been possible without the help of a number of people to whom I am greatly indebted. First and foremost, I would like to thank my parents, Mr. and Mrs. Kermit Hobbs, for their encouragement and support throughout my academic career. I could never have made it this far without them.

I am extremely grateful to my committee chairman, Dr. Dan Moore, for his guidance and advice in all aspects of this project. Not only has he helped me with technical matters, he has also helped me keep a positive outlook even when I ran into problems. It has been a great pleasure to work with Dr. Moore this year.

I would like to express my appreciation for the time and effort put forth by the other members of my committee, Dr. Aicha Riad and Dr. Seshu Desu. I would also like to thank Dr. Riad for her interest and concern while I was a student in her classes.

Special thanks go to three other people who made graduate study a bit easier for me: to Fred Barlow, for patiently answering question after question in the lab; to Ms. Loretta Estes, for her friendly help in dealing with assorted paperwork and other problems; and to my fiancee, Heather Carter, for her patience, understanding, and encouragement during the course of this work.

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Chapter 1
Introduction

Silicon micromachining is the collective name for several processes by which three-dimensional structures may be constructed from or on silicon wafers. Micromachining techniques can be divided into two main categories: bulk and surface micromachining. Bulk micromachining utilizes special etchants to form structures from the silicon wafer itself, while surface micromachining builds structures on top of the wafer by adding and removing layers of material. This project is concerned primarily with bulk micromachining, also known as anisotropic etching.

1.1 Background

Anisotropic etching is the selective removal of silicon using chemicals which attack the wafer at different rates in different crystallographic directions. For example, KOH will etch (100) and (110) planes at relatively high rates, while the (111) planes are nearly untouched. Actual etch rates vary depending on etching conditions, but are often on the order of nearly 1 μm/min in the fastest-etching direction; rates as high as 1.4 μm/min have been reported [1-3]. Under certain conditions, the ratio of fastest to slowest etch rates may be as high as 400:1 [3, 4].

Anisotropic etching has proved useful in many ways. The difference in etch rates allows the creation of a number of basic structural elements which may be combined to form various micromachined devices. These elements include pits, nozzles, beams, and diaphragms, along with several others. The minimum size of these elements is limited only by the resolution of the photolithographic process used to pattern the wafer. Even though the etchants' dependence on crystallography limits the types of structures that may be

created, a significant number of applications already take advantage of anisotropic etching. Common examples include nozzle arrays for inkjet printers, pressure sensors which utilize micromachined diaphragms, and cantilevered-beam accelerometers for automobile air bag deployment systems [1, 5-9].

In fabricating these devices, anisotropic etching has several advantages over traditional precision machining techniques. Its primary advantage is that it is a parallel process, allowing large quantities of identical devices to be produced at once, thereby reducing production costs. The fabrication method guarantees that device characteristics can be reproduced within very tight tolerances. In addition, etching produces much smoother surfaces than those created by precision milling operations, which usually have to be polished in a separate operation. Traditional machining leaves parts under mechanical stress and introduces dislocations in the wafer, but etching does not induce stress or lattice damage. Lastly, since anisotropic etching is merely an extension of normal IC fabrication technology, it is hoped that control circuitry will soon be directly fabricated along with the microstructures. Because of these advantages, the popularity of anisotropic etching for silicon micromachining is growing steadily [8].

1.2 Overview of the Project

The purpose of this thesis project can be divided into three main objectives. The first objective is to study the principles and theory of anisotropic etching. Second, those principles are used to develop a process by which anisotropic etching may be reliably performed in our facilities here at Virginia Tech. Finally, this process is applied to an experiment to demonstrate the feasibility of producing more complex structures using multiple etchings.

The first objective was accomplished by reviewing current literature on the subject. Various articles were collected, and their results were compiled to produce both a set of

guidelines for the etching process and a set of theoretical expectations for different etching geometries. During this research, the differences in the etching geometries of (100)- and (110)-oriented wafers were considered. While both orientations have their own applications and advantages, (100)-oriented wafers were chosen for this project because of their lower cost and more common use in the IC industry.

The second objective, to develop a reliable etching process in our own lab, was accomplished by etching wafers with a test pattern which was designed as part of the project. Process parameters were changed until the results were both satisfactory and reproducible. P-type (100) wafers were used, with KOH as the anisotropic etchant.

Once the process had been established, another etching experiment was performed which utilized two separate etching steps. In this case, the wafers were patterned and etched, then re-oxidized and etched a second time with a different mask, which had to be aligned relative to the first pattern. An alternative method was also tested in which the wafers were etched from both sides at the same time. These processes allowed the creation of more complex structures with the potential for a greater number of applications. The experiment also included a comparison of wafers etched at different temperatures.

1.3 Overview of the Thesis

This thesis paper is divided into five chapters. Chapter One provides some basic background information on the thesis project. Chapter Two will discuss, in some detail, the principles and theory of anisotropic etching as determined from the literature review. This chapter will also include descriptions of a few applications to illustrate the use of these principles for device design and fabrication. Chapter Three will describe the experiments performed to develop and verify a reliable etching process, and it will close with a summary of that process. Chapter Four will cover the double-etching experiment,

with emphasis on the additional advantages and limitations of multi-step etching. Chapter Five will conclude the thesis paper with a summary of the project and some suggestions for further study and experimentation.

Chapter 2
Theory & Principles of Anisotropic Etching

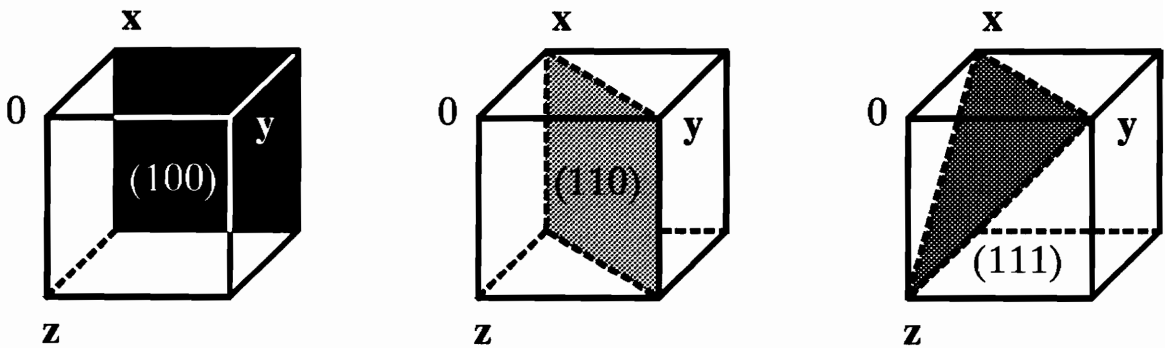
The first step in this project was to examine the principles of anisotropic etching so that they might be used to develop the etching experiments. The basic theory of anisotropic etching is compiled and explained in this chapter, followed by a survey of the many different implementations of anisotropic etching used by other researchers. The chapter will conclude with three simple examples which illustrate how these principles and techniques can be used to build practical devices.

2.1 Basic Theory of Anisotropic Etching

The theory behind anisotropic etching techniques is best explained by breaking it into three parts: an examination of the orientation-dependent nature of anisotropic etching, a discussion of the basic structural elements which may be formed using anisotropic etching, and a look at erosion effects which must also be considered for practical etching.

2.1.1 Orientation-Dependent Etching

Anisotropic etching takes advantage of the fact that certain etchants attack Si at different rates in different crystallographic directions. These same etchants etch SiO_2 or Si_3N_4 extremely slowly, so oxide or nitride layers may be deposited and patterned to selectively protect portions of the wafer surface. The most important crystallographic planes for etching purposes are the (100), (110), and (111) planes. The relationship of these planes is best illustrated by the following diagrams:



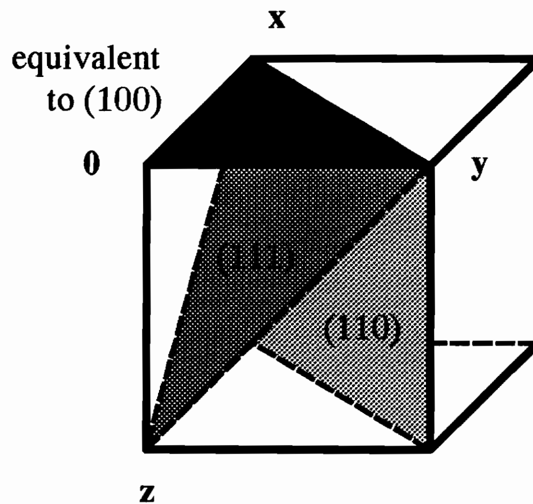


Figure 2-1. Orientation of crystallographic planes.
(a) Individual planes; (b) Combined view with equivalent (100) plane.

Figure 2-1(a) shows each of the low-index planes individually. Due to the rotational symmetry of the cubic crystal structure, an equivalent (100) plane exists as shown in the combined view of Figure 2-1(b). This equivalent diagram is more convenient when discussing the etching of (100)-oriented wafers. As shown in the figure, the (110) planes are perpendicular to the (100) planes, while the (111) planes are offset from the (100) planes by 54.74° [2].

Anisotropic etching is most often performed on (100)-oriented Si wafers [i.e., the flat surface of the wafer is a (100) plane] using potassium hydroxide (KOH) or ethylene diamine pyrocatechol (EDP) as the anisotropic etching agent. Etch rates are slowest in the (111) direction, while the (100) planes usually etch the fastest. [In some cases, however, the (110) planes etch slightly faster than the (100)'s; this depends primarily on the concentration and temperature of the etchants.] The ratio of (100) to (111) etch rates varies from as low as 35:1 for some EDP mixtures [4] up to about 400:1 for some KOH solutions [3].

The mechanism by which these etchants preferentially attack the (100) and (110) planes is not fully understood, but at least three factors are involved. The first and simplest factor is the atomic density in each of the atomic planes. When viewed in the (111) direction, the Si atoms are much more tightly packed than in the other directions, as illustrated in Figure 2-2.

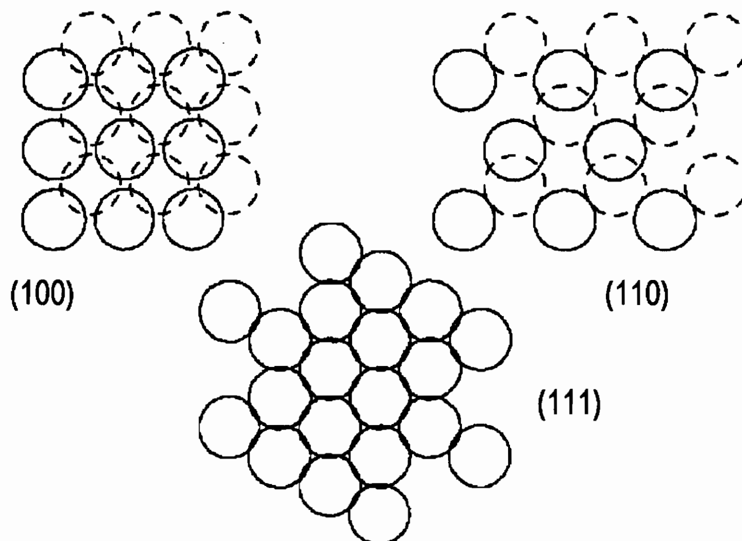


Figure 2-2. Atomic density in each of the major crystal planes. Dashed lines indicate atoms in the second planar layer.

The etching of a (111) plane will require the removal of a larger number of atoms than would the etching of the (100) or (110) planes. Another important factor is the number of dangling bonds, and, therefore, the number of remaining bonds which must be broken to remove an atom from the Si surface. Atoms on the (100) surface have only two remaining bonds, while those on the (111) surface have three. Thus, etching (111) planes requires more energy per atom than etching (100) planes. These differences in atomic density and bonding cannot entirely account for the difference in etch rates; some other factor must also be involved. It is believed that this third factor is the formation of a layer of hydrated oxide on the (111) surfaces which severely retards etching [9, 10].

2.1.2 Simple Structures

Orientation-dependent etch rates permit the creation of various structures. To better understand this process, let us consider a typical (100) wafer, Figure 2-3. First, this wafer must be coated with SiO_2 or Si_3N_4 to form a protective layer, or mask, on both sides. Now assume that we open a square hole, aligned with the (110) direction, in the protective layer on one side of the wafer. This can be done using standard photolithographic techniques; alignment of the pattern with the (110) direction is relatively easy because the wafer flat is ground parallel to them. If the masked Si surface is now exposed to an anisotropic etchant, the etchant will attack the (100) surface immediately. As the etching proceeds into the wafer, (111) planes will be exposed. These planes resist etching, so they will tend to confine the etching to the area between the exposed (111) planes. As the hole gets deeper, these (111) planes grow closer together until they eventually reach a point, forming a square pyramidal hole with 54.7°-inclined sides. It can be shown using simple geometry that the depth of this hole is 0.707 times the length of one side of the square opening [2]. If this depth is greater than the thickness of the wafer, a square, funnel-like nozzle will be formed through the wafer.

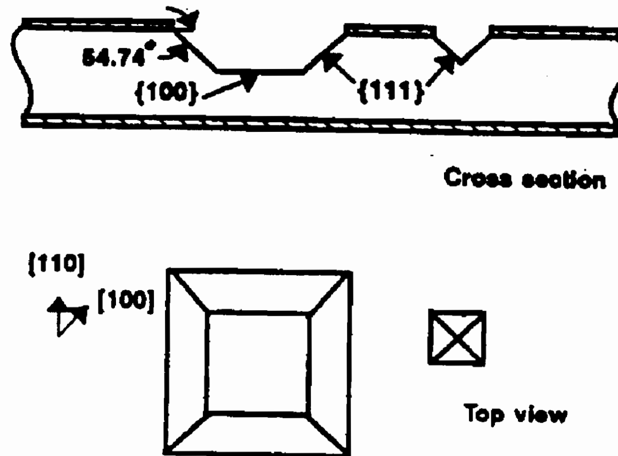


Figure 2-3. Anisotropic etching of a (100)-oriented wafer. Etch pits are defined by the slow-etching (111) planes; etching stops when these planes converge at the bottom of the pit [8].

The process described above can be extended to openings of any shape. If, for instance, we have a rectangular opening aligned with the (110) direction, it will etch a trough in the wafer with a depth of 0.707 times the smaller dimension of the opening. Openings which are not aligned either parallel or perpendicular to the (110) direction present a special problem: the etching process will not immediately expose a single (111) plane, so any pattern edges which do not lie along the (110) equivalent planes are inherently unstable. In this case, the etching will undercut the edge of the masking layer until a complete (111) face is reached. Figure 2-4 shows three examples of this phenomenon:

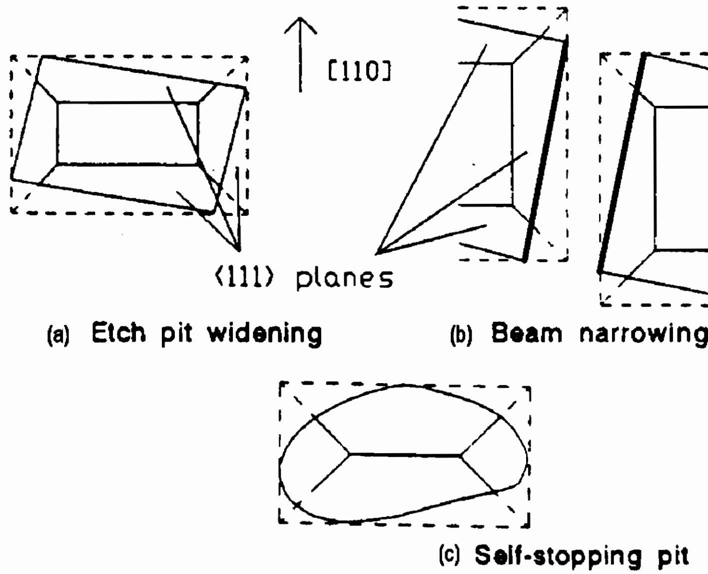


Figure 2-4. Effects of misalignment (Top View).
Solid lines indicate openings in mask; dashed
lines show extent of actual etching [8].

In the figure above, part (a) shows the result of a rectangular opening which is misaligned with respect to the (110) direction; the etching undercuts the mask until complete (111) planes are exposed. Part (b) shows how this effect can lead to the unintentional narrowing of a beam formed between two etch pits if the pattern is similarly misaligned. The bold lines represent the original beam pattern, while the vertical dashed lines show the actual beam width after etching. In (c), we see that, given sufficient time, any arbitrary opening in the protective layer will cause the formation of a rectangular pit with (111) sides which completely enclose the original opening [8]. In the case of a circular opening, etching will first produce an octagonal pit which will soon become a square [1]. This instability of non-aligned edges is one of the primary limitations in the use of anisotropic etching to build micromachined devices.

An important tool in the design and fabrication of anisotropically etched devices is boron doping. The etching action of KOH and EDP can be stopped by including a layer

of Si which has been heavily doped with boron. This B doping can be achieved in the normal manner, through diffusion or implantation, but the concentration must be greater than about 5 x $10^{19}/cm^3$, which makes the material nearly degenerate. This type of etch-stop permits the fabrication of a larger variety of structures; for example, we might pattern cantilever beams and dope them with B so that, upon etching through the wafer, only the beams remain across the opening. Another example might be the use of B to create a diaphragm by stopping the etch just short of a complete etch-through [1, 11].

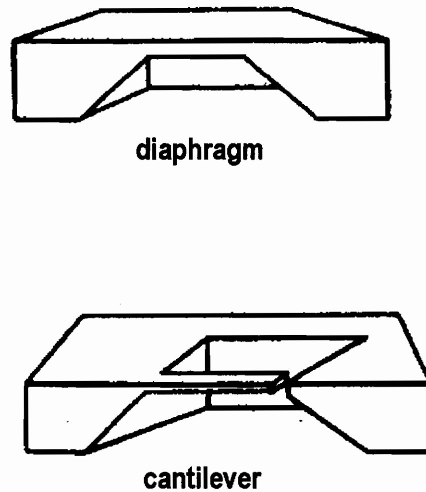


Figure 2-5. Diaphragm and cantilever structures fabricated using boron doping [8].

One limitation in the use of B to pattern structures is that the doping processes will leave a B concentration gradient in the material around the edges of the doped area; the gradient will then cause a gradual change in etch rates rather than a sharp cutoff. With EDP, this will result in rounded corners rather than sharp edges. KOH does not have this problem because it is less sensitive to variations in the B concentration. However, the trade-off with KOH is that even the highest concentrations of B cannot provide a hard etch-stop. The B etch-stop is adequate for timed applications, though, since KOH etches p^+ silicon at less than 5% of the rate at which it etches undoped silicon [11].

The boron etch-stop can be combined with the previously discussed misalignment effects to create bridges over etch-pits, even when they do not go all the way through the wafer. The first step in this technique is to lay out a pit and bridge pattern which is intentionally misaligned by about 5°-10° with respect to the (110) direction. The bridge area is doped with B to protect it from etching, and then the wafer is exposed to the etchant. The misalignment insures that the bridge edges will be undercut, creating a situation similar to that of Figure 2-4b, above. If the bridge is narrow enough and misaligned enough, the undercutting will completely free the bridge structure by etching out all of the material beneath it. Only the B-doped portion of the material will remain, leaving a thin bridge of Si across the pit [11].

2.1.3 Erosion Effects Caused by (111) Etching

At this point we should consider the effects of the small but non-zero etch rate in the (111) direction. Even when a straight-sided pattern, such as a square, is perfectly aligned with the (110) equivalent planes, some undercutting of the pattern edges will occur as the (111) planes are slowly etched back [8]. In the case of rectangular etch pits, this has the effect of widening the opening while keeping the original shape. Quantitative estimates of this widening are best made by experiment, since the actual etch rates will vary with the conditions of the etching. A unique application of this undercutting effect has been described by some researchers, who utilized undercutting to create pits of varying depths at the same time even when some of the pits had the same length and width. Their technique is best described using Figure 2-6.

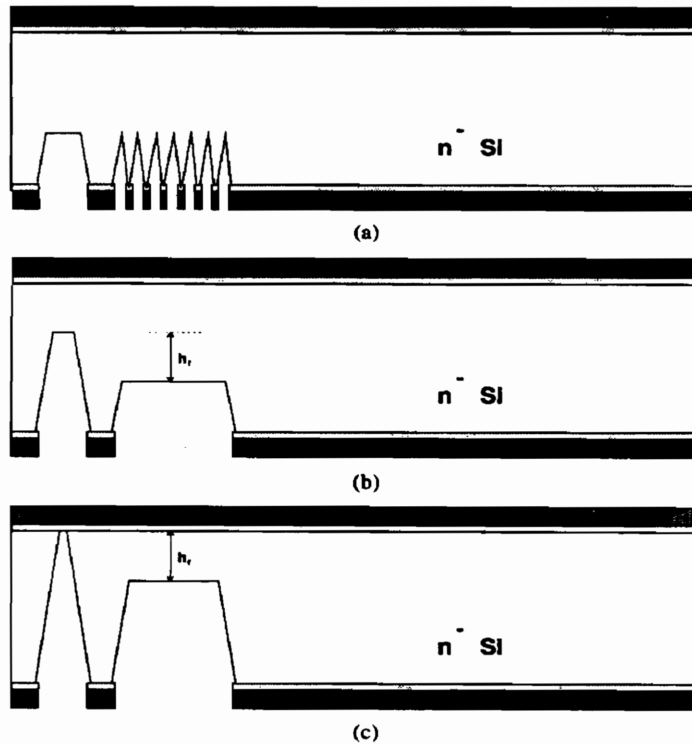


Figure 2-6. Etch-delaying technique using mesh undercutting [4].

In order to slow the etching of one pit relative to another, a delay must be built into the etching process. This is accomplished by changing the form of the mask pattern. Rather than a single opening, an array of smaller openings covers the area to be etched. These openings can be visualized as the original opening covered by a narrow mesh. When the wafer is first exposed to the etchant, a number of small pits begin to form. These small pits will quickly etch to completion, and then the (111) sides etch back very slowly (Figure 2-6a). Once the (111) sides undercut the mesh enough, the small pits merge (Figure 2-6b) and the more rapid (100) etching resumes, creating a single large pit which is shallower than those created without a mesh pattern (Figure 2-6c). The delay caused by the need to etch the (111) sides is completely predictable and can be used to form pits of varying depths at the same time. Of course, the etching must be timed carefully because if the wafer is left in the etchant indefinitely, the delayed pit will catch up to the others once they

all reach completion. Also, it should be noted that the use of this technique demands etching conditions that result in a relatively low etch rate ratio (e.g., $R_{(100)}:R_{(111)}$ on the order of 35:1, which can be achieved using certain EDP solutions) [4].

While the erosion effects discussed above can be put to good use in some applications and at least minimized in others, there are other erosion effects which are more difficult to handle. The most significant of these is the erosion of convex corners. Any mesa-type structures will suffer erosion at their corners because of the crystallography of the material. Only smooth (111) faces will prevent rapid etching; the convex edges where they meet expose fast-etching (331) planes which are attacked by the etchant. To compensate for this erosion, overhanging tabs can be added to any convex corners in the mask pattern. The tabs do not prevent erosion, but attempt to make allowances for it. Since it is hard to predict exactly how much erosion will occur, the optimum dimensions of these overhanging tabs are best found by experimentation. The problem of convex corner erosion is even more troublesome in the case of circular rather than rectangular mesa structures. While a rectangular structure has stable sides but erodes at the corners, a circular mesa is, in effect, one continuous convex corner which is subject to erosion from all angles. The erosion of a circular mesa will expose eight (331) planes near the surface of the wafer, giving the top of the mesa an octagonal shape [2].

Another type of erosion occurs when a wafer is etched through from both sides at once. This type of erosion is best described using a cross-sectional diagram, Figure 2-7.

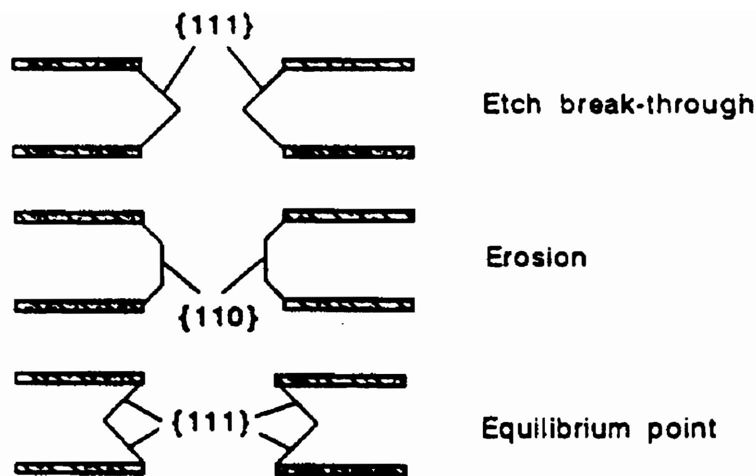


Figure 2-7. Erosion of unstable edges formed during double-sided etching [8].

As the figure above shows, the edge formed by the converging (111) planes is unstable. As the edge erodes, fast-etching (110) planes cause the sides of the hole to become concave rather than convex. This effect may not always be significant to the designer, but it must be taken into consideration in certain applications [8].

2.2 Anisotropic Etching Techniques & Practical Considerations

Up to this point we have only considered the theory of anisotropic etching without regard to the actual etching conditions or techniques. In practice, the success of bulk micromachining is limited by several factors. First, the method requires that the Si lattice structure be as nearly perfect as possible. Any dislocations or disruptions in the lattice will affect the smoothness and resolution of the etching process. Second, the wafer must be thoroughly cleaned before etching. EDP in particular is so selective that any residues or contaminants on the wafer surface will interfere with the etching process [1]. Lastly, the SiO_2, Si_3N_4, and B-doped etch-stops will also be gradually etched away, so the thickness of these layers must be sufficient to last throughout the entire process. KOH attacks these

layers more rapidly than EDP, but allowances must be made for either etchant [11]. A choice must also be made between SiO_2 and Si_3N_4 for use as the masking layer. Si_3N_4 is much more resistant to attack by the etchants, but it requires a CVD process to deposit and a plasma etch to create a mask. SiO_2 can be thermally grown in a steam ambient and is easily patterned using a buffered HF solution. Therefore, a trade-off exists between the ease of using SiO_2 and the better protection of a thinner layer of Si_3N_4 [2].

The techniques used to carry out the etching process vary greatly from one application to the next. Not only must one weigh the merits of EDP versus KOH, but the etchant concentration and temperature also must be chosen to optimize the etching speed and quality. Most researchers using KOH solutions have reported concentrations of about 35% by weight; reports of EDP concentrations vary widely. Typical etching temperatures are up to 85° C for KOH or in the range of 100°-118° C for EDP solutions. In addition, some researchers have added isopropyl alcohol to their KOH solutions, reporting that it increases the (100) etch rate relative to the (110) rate. Overall, etching in the (100) direction proceeds at a rate on the order of 1 μm/min under most etching conditions [1-4, 9-12]. In practice, it may be best to simply choose a set of etching conditions and determine the relevant etch rates (including the etch rate of the masking material) by experiment. These rates can then be used as design parameters for specific applications [1].

One last condition which should also be mentioned is agitation of the etching solution. As shown in Figure 2-8, etching carried out without agitation produces etch pits with smooth, flat bottoms, while agitating the solution creates pits with a more rounded contour. Agitating the solution will speed the etching process, but unless one is planning to etch through the entire wafer, the flat-bottomed pits are probably preferable [8].

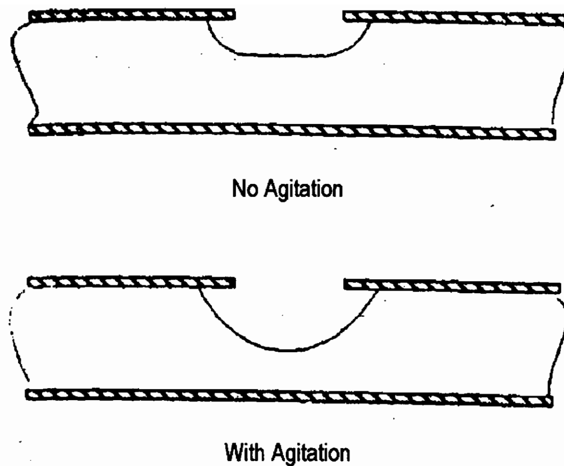


Figure 2-8. Effects of agitation during etching [8].

Finally, it should be noted that although (100) wafers are more commonly used for micromachining, (110) wafers may be used to fabricate different types of structures. The etching techniques are very similar, but the different crystallographic orientation produces etch pits with vertical (100) sides rather than sloping (111) planes. This allows the construction of, for example, channels with vertical walls. One potential application of this construct might be an array of channels which could be bonded to another wafer and used as a heat exchanger to cool a high-power IC device [1].

2.3 Example Applications

In order to illustrate the utility of anisotropic etching in the fabrication of practical devices, we will now consider three of the most common current applications of etching technology: inkjet printer nozzles, micromachined accelerometers, and miniature pressure sensors. Each of these devices is constructed using one of the basic structural elements discussed above: the nozzle, the cantilevered beam, and the diaphragm, respectively.

Perhaps the simplest current application of anisotropic etching is the fabrication of nozzle arrays for inkjet printers. These nozzles can be made simply by etching square pits through a Si wafer, creating a square opening which can have dimensions even smaller than the minimum resolution of the photolithography process [8]. To create a circular nozzle opening, a more complex version can be made using a B-doped etch-stop to create a diaphragm with a small circular opening in it. (The entire diaphragm is B-doped except for the circle to be etched.) Of course, the minimum diameter of the opening is determined by the resolution limits of the B-doping and its associated photolithographic process [1].

Another celebrated application of anisotropic etching is the micromachined accelerometer, most commonly used for crash detection in automobile air bag deployment systems. In this case anisotropic etching is used to fabricate a proof mass suspended from cantilever beams; the movement of this mass can be detected by capacitive sensing or by depositing piezoresistive or piezoelectric material on the surface of the cantilevers. Often, some type of wafer bonding is used for mounting or enclosing the structure. Wafer bonding is important in micromachining because it allows wafers to be etched separately and then combined to form more complex structures than would otherwise be possible [5, 7, 8].

Much of the current research into micromachining techniques, including anisotropic etching, is devoted to the production of a variety of miniature sensors. Perhaps the most common sensing structure fabricated with anisotropic etching is the simple diaphragm, which may be created using either a timed etch or a B-doped etch-stop. A good example of such a structure is a pressure sensor device created by bonding a flat wafer over the cavity behind a micromachined diaphragm. The flat wafer may have a small hole etched through it to enable connection to some reference pressure, or the cavity may be sealed entirely. In any case, the sensor is calibrated by measuring the deflection of

the diaphragm using capacitive or piezoresistive methods. As with the accelerometer, the primary advantages of producing these devices with anisotropic etching are low unit cost and high reproducibility. In addition, the small size of etched devices allows them to be used in a number of entirely new applications [6, 8].

2.4 Summary

The techniques of anisotropic etching are based on the preferential etching nature of solutions such as KOH and EDP, which attack the (100) and (110) planes of a silicon wafer many times faster than its (111) planes. This difference in etch rates permits the creation of a number of structural elements with semi-permanent (111) sides [relative to the (100) and (110) planes]. The use of highly doped ($\geq 5 \times 10^{19}/cm^3$) boron etch-stops permits an even greater variety of structures. In designing micromachined structures to be built by anisotropic etching, however, one must take into account the effects of erosion on convex corners and round edges. In some cases, even the small but nonzero etch rate of the (111) planes must be considered.

Currently, there is no standard procedure for anisotropic etching. Researchers use different concentrations of both KOH and EDP, and the etching is carried out at widely varying temperatures. Typically, etching temperatures are up to 85° C for KOH or in the range of 100°-118° C for EDP solutions. Other variations in techniques include the addition of isopropyl alcohol to some KOH solutions, and the agitation of the etch bath in some cases. Overall, etching in the (100) direction usually proceeds at a rate on the order of 1 μm/min under most etching conditions.

Three examples of current applications of anisotropic etching are high-precision nozzles for inkjet printers, micromachined accelerometers, and miniature pressure sensors. These devices are made up of simple structural elements which can be fabricated by applying the principles described in this chapter.

Chapter 3
Development of a Reliable Etching Procedure

The second major task in this thesis project was to develop a reliable procedure by which anisotropic etching can be performed in a typical research laboratory environment. To accomplish this goal, a suitable experiment had to be devised which would produce known results in order to verify the etching procedure. Next, several test wafers were prepared and patterned using standard techniques, and then the etchant and conditions were chosen based on the literature review. Finally, the wafers were etched and the process parameters were varied until the results were both suitable and consistent. This chapter concludes with photographs of the etching results and a summary of the final procedure.

3.1 Test Pattern Design

The first step in developing a standard etching procedure was to devise an experiment which could be used to verify the success of the procedure by producing known results. This verification was most readily accomplished using one single-sided etch step with an appropriate test pattern. More complex multi-step or double-sided etchings were reserved for later experiments.

The most important part of designing the initial experiment was the choice of a test pattern. I wanted to incorporate as many different features as possible in the pattern in order to demonstrate the theory discussed in Chapter 2. In this way, the test pattern could be used not only to verify the etching process, but also to study some basic etching

principles. The final pattern is shown in Figure 3-1, where letters have been added to aid in discussion of the various features:

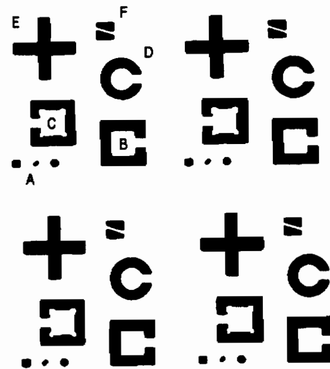


Figure 3-1. Pattern for etching experiment (Actual size).
Black areas indicate openings in oxide mask.

The straight edges in the pattern were aligned with the (110) direction, as described below (§3.2). The test pattern consists of four identical groups of features, labeled "A" through "F" in the figure above. Each of these features is described in the paragraphs which follow:

Part "A" is a group of five small openings: a square, a rectangle which is intentionally misaligned with respect to the (110) direction, a circle, and two much smaller squares (which do not even show up in this figure). This part of the experiment was meant to show that any opening, given enough time, will etch out a square or rectangular pit in the wafer. The results of the three larger openings were intended to be squares of equal size. For the circle, this equality was achieved by making its diameter equal to the length of one side of the square pattern, while the size of the rectangle was set by inscribing it inside a similar square. The two smallest openings were small enough to prevent a complete etch-through, so they were expected to form pyramidal etch pits.

Parts "B" and "C" are both suspended masses such as might be found in an accelerometer application. The objective in this case was to observe the effects of convex corner erosion on a square mesa structure and to determine the effectiveness of overhanging tabs in preventing this type of erosion. Part "B" had simple square corners, while part "C" had small tabs on two corners (the bottom ones in Figure 3-1) and larger tabs on the other two corners.

Part "D" is very similar to "B" and "C", but in this case the mesa is circular. In Chapter 2 it was suggested that this type of structure would erode very rapidly, creating an octagonal shape formed by the (331) planes around the top of the mesa.

Part "E" is a plus-shaped pattern intended to show the erosion of the convex corners created when two troughs intersect at right angles.

The objective of part "F" was to demonstrate the undercutting of the misaligned oxide "bridge" across the otherwise square mask opening. In this case the two sides were expected to etch down and rapidly merge beneath the oxide, leaving only a single square pit with 54.7° sloping sides.

Once the test pattern had been designed by hand, it was drawn on Rubylith and then photo-reduced. The resulting negative then served as the mask used in the photolithographic patterning of the test wafers.

3.2 Wafer Preparation and Photolithography

Before the wafers could be patterned, the wafer surfaces had to be oxidized to create a protective layer which would resist the etchant. While a nitride layer could have been used instead, an oxide layer was chosen because SiO_2 is easier to deposit and pattern than Si_3N_4. A 1.5 μm layer of SiO_2 was thermally grown on the wafers using a furnace at N. C. State University. In future experiments, the oxide growth may be performed here at Virginia Tech when the diffusion furnace is fully operational.

Once the wafers had been oxidized, the next step was to clean them before applying photoresist. Cleaning was accomplished by rinsing the wafers with the following series of solvents: acetone; methanol; 1,1,1,-trichloroethane; methanol; and DI water. After the final rinse with DI water, the wafers were dried in a convection heating oven for 20 minutes at 95°-100° C.

Next, the cleaned and dried wafers were coated on both sides with Shipley 1350-J photoresist. In order to accomplish this, the photoresist was spun onto the back (unpolished) side of the wafer first, at a speed of 3000 rpm for 30 seconds. The back side coating was soft-baked in the oven at 95°-100° C for 30 minutes before spinning a coat on the front of the wafer. The back side was coated first so that the photoresist on the patterned (front) side of the wafer would not be damaged by friction between the wafer and the spinner chuck. Once the front coating was soft-baked for 30 minutes (again at 95°-100° C), the wafer was ready to be exposed and developed.

Before exposing the wafer, the test pattern mask was carefully aligned along the primary wafer flat. This alignment was very important, for it ensured that the pattern edges lay parallel to the (110) equivalent planes. Misalignment would result in undercutting of the pattern edges, as described in Chapter 2, and in more complex experiments it would make opposite-side mask alignment virtually impossible. Once the mask was in place, the wafer was exposed to UV light for 9.0 seconds before developing the photoresist using Shipley 353 developer. Once the photoresist had been patterned, it was hard-baked for 30 minutes at 105°-110° C.

The next step was to remove the oxide from areas that had been exposed by the removal of photoresist. This was accomplished by immersing the patterned wafer in 10:1 Buffered Oxide Etch (BOE) for 25-30 minutes at room temperature. (BOE is a solution of HF and NH_4F.) Complete removal of the oxide was confirmed by lightly rinsing the wafer with DI water to check for hydrophobicity of the exposed silicon. Once all the

oxide was removed, the photoresist was dissolved with acetone and the wafer was ready for etching.

3.3 Choice of Etching Conditions

Given the wide range of etching conditions cited in Chapter 2, it was no small task to decide what conditions might give the best results. The first and easiest choice was the choice of etchant: KOH or EDP. KOH was selected because it was readily available and relatively easy to handle.

The etchant concentration and temperature were more difficult choices. Researchers have reported that different conditions result not only in different etch rates, but more importantly in different ratios between the etch rates in different crystallographic directions. Thus, the choice of etching conditions affects not only the speed of the etch, but also determines the geometry and quality of the resulting structures.

The initial choices for concentration and temperature were 100 g KOH per 1000 mL DI water at 35° C. It was assumed that these conditions would give a slow but smooth etch with high resolution and near-perfect features. Instead, the etching proved to be much too slow, and the ratio of (100):(111) etch rates was also very low, leading to excessive erosion of structure edges. The decision was made to raise both the concentration and temperature, using instead 400 g KOH per 1000 mL DI water at a temperature of 50° C.

3.4 Experimental Etching and Observations

A number of etching experiments had to be performed before satisfactory results were obtained. The first problem that was encountered was a complete absence of etching due to the incomplete removal of the oxide layer. Even after as much as an hour in 49%

HF, there was a substantial (perhaps 0.5 μm) layer of oxide remaining. This was a thick enough oxide to completely prevent any measurable etching. This problem was solved by using a buffered HF solution (BOE) rather than the HF alone.

Once the oxide problem was solved, a wafer was etched by immersing it horizontally (patterned side up) in a 100 g:1 L KOH:DI water solution at a temperature of 35° C. The results of this etching were unsatisfactory: after 57.5 hours in the etchant, the wafer still had not etched completely through. There were some holes through the wafer, but other areas still had as much as 35 μm of Si remaining. Also, the wafer was removed from the KOH solution three times during the course of the experiment to measure the etching progress. Examination of the wafer at these times showed extremely rough bottom surfaces in all of the etch pits, and profiles of the surfaces indicated very uneven etching. However, the test pattern did provide the expected results in terms of feature shapes, erosion, and undercutting.

In an attempt to correct some of the problems of the first etching, the second wafer was etched at 50° C in a 400 g:1 L KOH:DI water solution, with the wafer again lying horizontally in the beaker. Etching proceeded normally for 16 hours, with only 2 interruptions for measurements. The bottom surfaces of the etch pits were extremely smooth, and the etching appeared to be quite successful. However, it soon became apparent that the etch rate had fallen to nearly zero with perhaps 100 μm of Si remaining to be etched. At first it was thought that the KOH solution had been depleted, but testing with a small sample of bare Si showed that the solution was still good. At this point the effects of diffusion within the solution were also considered. It seems plausible that once the etch pits reached a certain depth, the etchant became depleted in a localized area within the etch pits, and the etch rate was then determined by the rate of diffusion of new etchant ions into this boundary layer. In order to test this hypothesis, the wafer was repositioned and etching was continued. First the wafer was etched horizontally,

patterned side down, for 5 hours with no measurable effect. Then the wafer was propped up on its edge in the etchant, and after about 4 hours, the etching was very nearly complete. Apparently the near-vertical position of this wafer allowed sufficient agitation of the solution (The etching produces hydrogen bubbles at the Si surface.) to prevent the formation of a depleted boundary layer. At this point it appeared that only the back oxide coating remained over the etch pits, so etching was suspended and the oxide was removed with BOE. A small amount of Si did remain in some of the etched patterns; these were removed by simply thinning the entire wafer in the KOH solution for a short time.

The third wafer was positioned on its edge throughout the entire etching process in order to determine if the hypothesized boundary layer had been the only problem. The etchant concentration and temperature remained the same. This time the etch resulted in very smooth pit bottoms, and also apparently sharper pattern definition (i.e., less erosion of pattern edges). It is believed that this was due to a slight increase in the (100):(111) etch rate ratio which occurs when a wafer is etched on its edge rather than horizontally. Despite this minor achievement, the overall etch time was still disappointing. After 24 hours of etching, with 5 interruptions for measurements, the wafer was still about 100 μm short of a complete etch-through. There was still a significant problem with the process.

This problem was solved by realizing that each time a wafer is removed from the etchant, such as for profilometer measurements, a native oxide forms on all the bare Si surfaces, which are highly reactive after having been etched. When the wafer is returned to the etch bath, this oxide retards all etching until it breaks up after perhaps an hour or more. In the case of my third wafer, described above, the problem was solved by dipping the wafer in 10:1 BOE for 30 seconds before returning it to the etch bath for the last time. After another 9.5 hours, the wafer etched to completion with good results. It was decided that in all future etching experiments, the wafer would be transferred as quickly as possible from the BOE used for patterning to the KOH etchant solution, allowing only a short

delay for the removal of photoresist. This transfer takes less than 45 seconds; in case of any delays, the wafer should be dipped in BOE for another 30 seconds before being rinsed with DI water and immersed in the KOH solution.

Another interesting observation was made at this point concerning the use of the profilometer. The profilometer operates by lightly scanning a finely-pointed pin across the wafer and measuring the vertical movements of the pin. This pin first contacts a sample by dropping a very short distance onto it. Although the force involved is very small, it is concentrated on a very small area due to the size of the pin. In the case of my wafer, this force introduced some type of defect in the wafer surface, although the effect was only noticeable if the initial contact point was on the bottom surface of an etch pit. Immediately after profilometer measurements were made, there was no visible damage when the wafer was viewed under an optical microscope. However, after etching the wafer for a short period of time (an hour or so), small (0.5 mm or less) square pits begin to form wherever the profilometer pin had landed. These pits did not act like normal etch pits; instead, they gradually became larger and more rounded until the etching had gone completely through the wafer. The development and behavior of these pits can probably be explained by the effects of native oxide formation when the wafer was removed from the etchant. Apparently the profilometer tip punctured or otherwise damaged the native oxide coat enough to cause certain points on the bottom of the etch pits to resume etching sooner than the others. This effect was only noticeable on the etch pit bottoms because the remainder of the wafer surface was covered by much thicker (1.5 μm) thermally grown oxide, making any damage there insignificant.

A fourth wafer was etched in an attempt to ameliorate some of the problems of the previous three experiments. Once again, a concentration of 400 g:1 L KOH:DI water at a temperature of 50° C was used. This time the wafer was transferred immediately from the BOE to the KOH bath, with only a short delay to remove the photoresist. The wafer was

etched on its edge with no interruptions in order to minimize the effects of both boundary layer problems and native oxides. Complete etch-through took 29 hours and resulted in smooth pattern edges with erosion effects exactly as expected. The average etch rate for this experiment was 13.14 μm/h, or 0.22 μm/min. This rate is in close agreement with etch rate data provided by Kendall and de Guel [13]. While the rate is a bit slower than the rates reported by researchers who used higher temperatures [2, 3], it produces high-quality results. Note also that the actual Si etch time may have been an hour or two shorter, since the back oxide coating was allowed to break up in the KOH rather than being removed with BOE. This was done to avoid stripping the oxide prematurely, as had been done with the second wafer.

3.5 Results

The etching results described above are summarized in Table 3-1:

Table 3-1. Summary of single-step etching results.

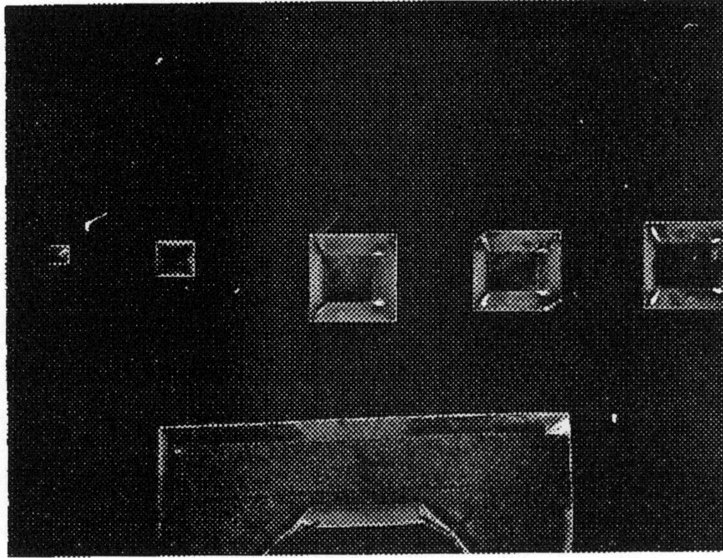
Wafer:	KOH Conc. [g/L]:	Temperature:	Total Etch Time (hours):	Total # of interruptions:	Wafer Position:	Results:
1	100	35° C	57.5	3	Flat	Rough bottoms Incomplete etching
2	400	50° C	25*	4	Flat (21 hr), Edge (4 hr)	Smooth bottoms Completed etching
3	400	50° C	33.5	5	Edge	Smooth bottoms Excellent definition Completed only after BOE dip
4	400	50° C	29	0	Edge	Smooth bottoms Excellent definition Completed Etching

*Should actually be longer for a complete KOH etch; oxide was removed prematurely and wafer was thinned slightly to finish. See §3.4.

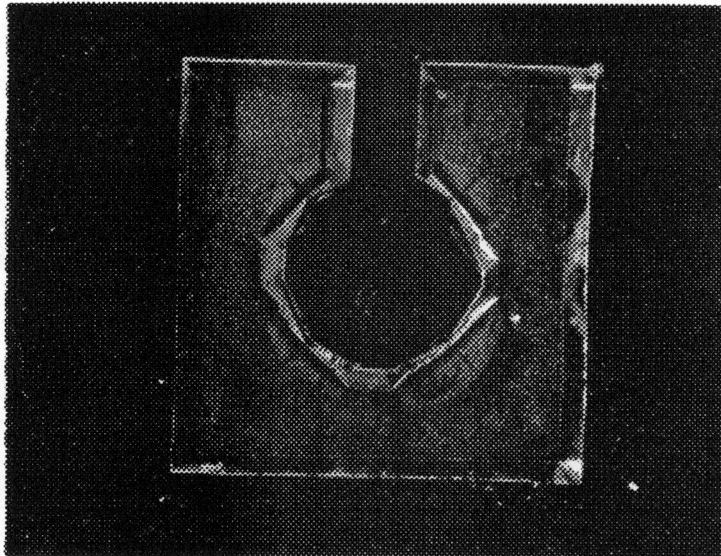
As the table shows, optimum results were obtained with the wafer etched on edge in a 400 g/L KOH solution at 50° C with no interruptions for measurements. The steps used to produce these results will be summarized at the end of this chapter.

While the etching experiments had varying degrees of success, all four experiments did accomplish one of my objectives: to demonstrate the etching principles described in Chapter 2. Each of the features included in the test pattern etched as they were intended, illustrating the expected effects of undercutting and erosion. The photographs which follow were taken to document the results. Except where noted, all are pictures of the second wafer after 16 hours etching time, about 100 μm short of a complete etch-through. Photograph 3-1 shows the five small pits labeled "A" in the test pattern of Figure 3-1. As expected, the squares and circle etched to form square pits with clearly visible sloping sides. At this point in the etch process (16 hours out of 25 total), the misaligned rectangle is the only feature which has not yet reached completion; it will form a square as soon as the two remaining corners etch out.

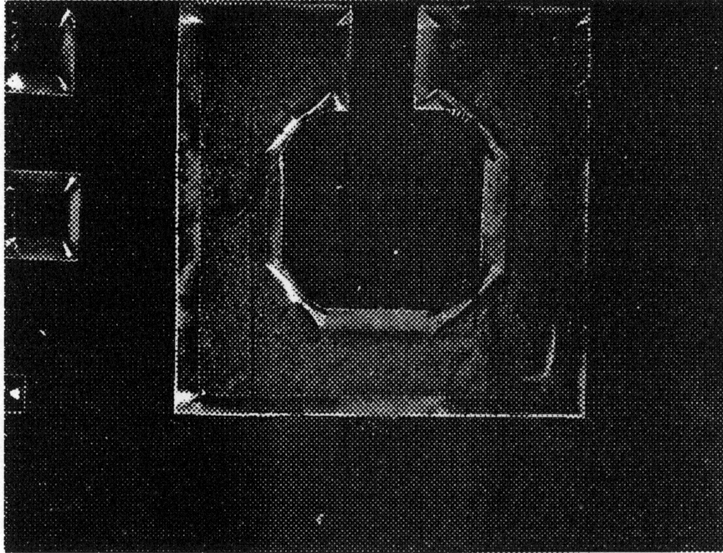
Parts "B" and "C" were both suspended masses such as might be found in an accelerometer application. The objective was to observe the effects of convex corner erosion on square mesa structures and to determine the effectiveness of overhanging tabs in preventing or compensating for this type of erosion. Part "B" had simple square corners; the result is shown in Photograph 3-2. The photograph clearly shows the effects of erosion on unprotected corners. The square mesa has already eroded significantly and become nearly round, and the etching is still a few hours from completion. In an effort to counteract this erosion, the structure labeled "C" had small tabs on two corners and larger tabs on the other two corners. Photograph 3-3 shows the etching results: the overhanging tabs did a reasonable job of maintaining a square-shaped mesa. The two larger tabs, on the right-hand side of the picture, were especially effective. To make sharper corners might require still larger tabs, though.



Photograph 3-1. Part "A": Series of etch pits (10x magnification).



Photograph 3-2. Part "B": Square mesa structure after etching (10x magnification).



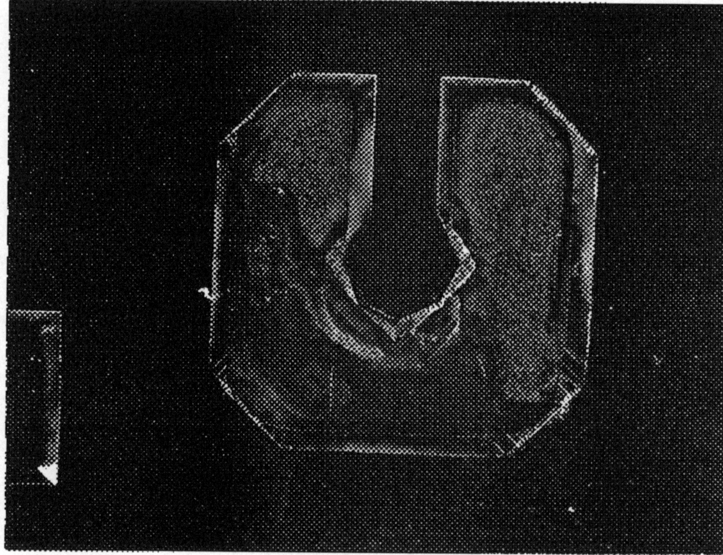
Photograph 3-3. Part "C": Square mesa with overhanging tabs (10x magnification).

Part "D" was very similar to "B" and "C", but the mesa was circular rather than square. In Chapter 2 it was suggested that this type of structure would erode very rapidly, and this was indeed the case. Photograph 3-4 clearly shows that the top of the mesa has taken on the characteristic octagonal shape formed by the (331) planes. The pattern for the circular mesa originally had a diameter equal to the width of the squares in "B" and "C." Note the drastic reduction in mesa size as compared with the square mesas in Photographs 3-2 and 3-3. Also, it is interesting to note the shape of the (originally circular) pit around the circular mesa: it is now octagonal and is rapidly becoming a square as the etchant undercuts the oxide mask.

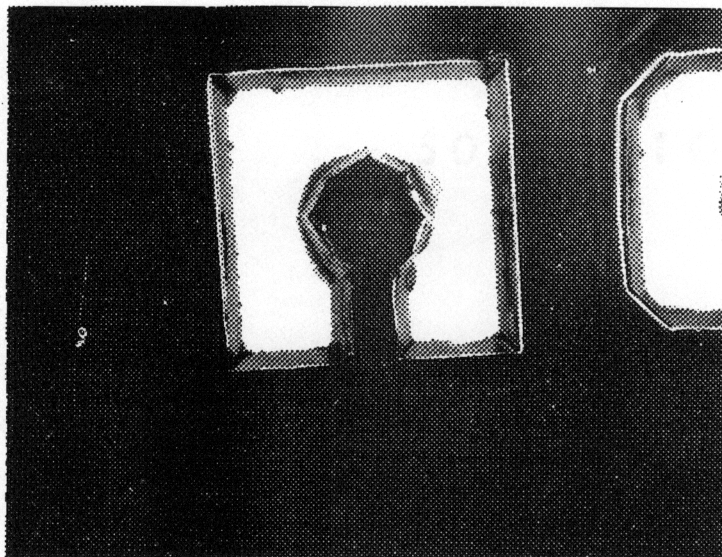
For comparison with Photographs 3-2 and 3-4, I have included photographs of the same features on the fourth wafer at the completion of the etching process. These photographs, 3-5 and 3-6, show the extent of the erosion of these features after a complete etch-through. The mesa with no corner tabs is no longer recognizable as having been a square, while the circular mesa is no longer a mesa at all; only the cantilever remains.

Part "E" was a plus-shaped pattern intended to show the erosion of the convex corners formed by two intersecting troughs. The effect was similar to that of part "B," as can be seen in Photograph 3-7. The corners have been rounded off and etched back drastically, just as expected. Overhanging tabs could have been used to compensate for much of this erosion.

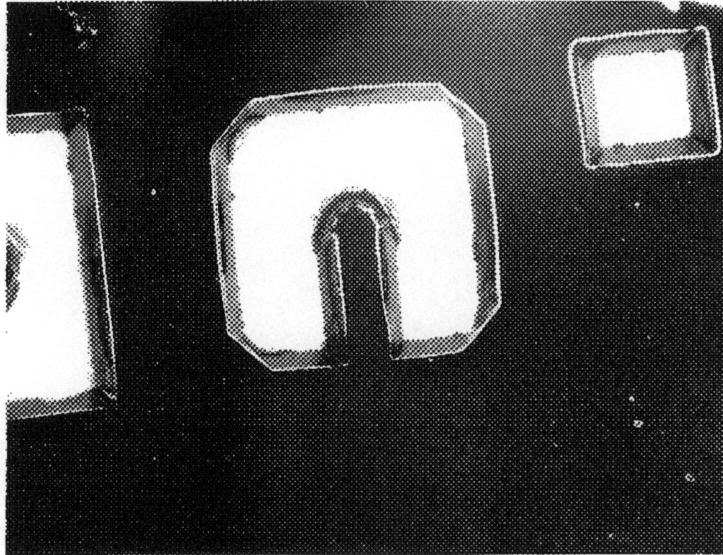
For comparison, a photograph of a similar feature on the first wafer is also included. The photograph shows the extremely rough bottom surface which resulted from an inadequate KOH concentration and a lower etchant temperature. The magnification is different due to equipment availability problems.



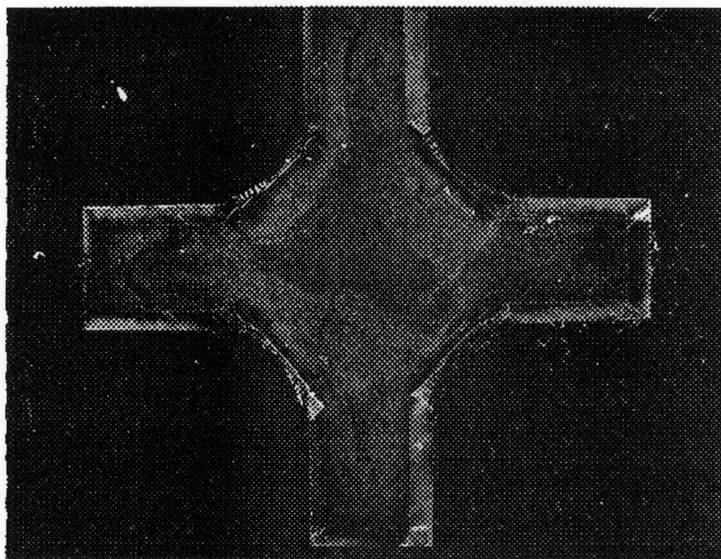
Photograph 3-4. Part "D": Circular mesa structure after etching (10x magnification).



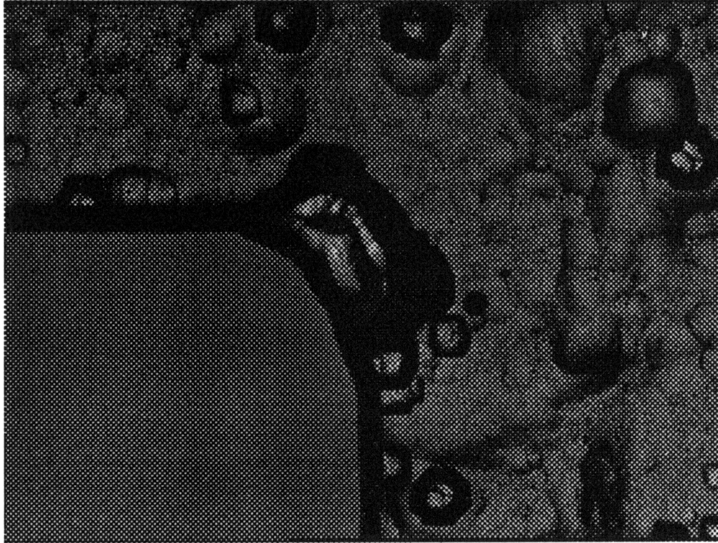
Photograph 3-5. Part "B": Total corner erosion (8x magnification).



Photograph 3-6. Part "D": Total circular mesa erosion upon completion of etching (8x magnification).



Photograph 3-7. Part "E": Convex corner erosion (10x magnification).



Photograph 3-8. Part "E," first wafer: Rough bottom due to poor etching conditions (44x magnification).

The last feature of the test pattern, labeled "F," demonstrated the undercutting of a misaligned oxide "bridge" across an otherwise square mask opening. In this case the two sides etched down and rapidly merged beneath the oxide. No photograph of this feature is included, since the result was simply a featureless square pit.

Overall, the results of my etching experiments agreed well with the results predicted by the theory discussed in Chapter 2. This agreement served to verify the success of my final etching procedure, which is summarized in the following section.

3.6 Summary of Etching Procedure

The objective of this set of experiments was to develop a reliable etching procedure which may be used to carry out anisotropic etching experiments in our labs here at Virginia Tech. The procedure which was developed is summarized below:

1. Lay out desired mask pattern on Rubylith; red areas should correspond to openings in the oxide mask. Include some type of parallel line or edge which can be aligned with the primary wafer flat.

2. Photo-reduce the Rubylith pattern to produce a negative which will be used as the photolithographic mask.

3. Obtain and oxidize 15-mil (100) wafers; 1.5 μm oxide thickness should be sufficient for any type of etching experiment.

4. Clean the wafers by rinsing with the following series of solvents for about 15 seconds each: acetone; methanol; 1,1,1,-trichloroethane; methanol; DI water. After rinsing, dry the wafers in the oven for 20 minutes at 95°-100° C.

5. Apply Shipley 1350-J photoresist to the back side of the wafers by spinning at 3000 rpm for 30 sec. Soft-bake in oven for 30 minutes at 95°-100° C.

6. Similarly apply photoresist to the front side of the wafers. Soft-bake as before.

7. Carefully align the mask with the primary wafer flat. Expose to UV light for 9.0 sec.

8. Develop using Shipley 353 developer. Hard-bake in oven for 30 minutes at 105°-110° C.

9. Pattern oxide layer by immersing wafer in 10:1 BOE for 25-30 minutes at room temperature.

10. Prepare an etchant solution of 400 g KOH per 1 L DI water. Heat to 50° C. Use a thermometer to verify the temperature of the solution before and during the etching process.

11. As quickly as possible, remove the wafer from the BOE, strip the photoresist with acetone, rinse the wafer with DI water, and place the wafer on its edge in the KOH solution. This process should take less than 45 seconds.

12. Do not disturb the wafer during the etching process. If etching must be interrupted, a 30-second dip in BOE is suggested immediately before returning the wafer to the KOH solution. A complete etch-through can be expected to take 27-29 hours.

This procedure should provide consistent, high-quality results. In the next chapter the same process will be applied to a more complicated experiment to demonstrate the fabrication of more complex structures using multiple etching steps.

Chapter 4
Multi-step Etching Experiments

The use of multiple etch steps permits the creation of more complex structures than are possible with single etchings. In fact, most of the practical devices currently being built require two or more etch steps for fabrication. This advantage is offset to some degree by complications in the patterning process. This chapter describes my own multi-step etching experiments and how those complications were overcome.

4.1 Mask Design and Preparation

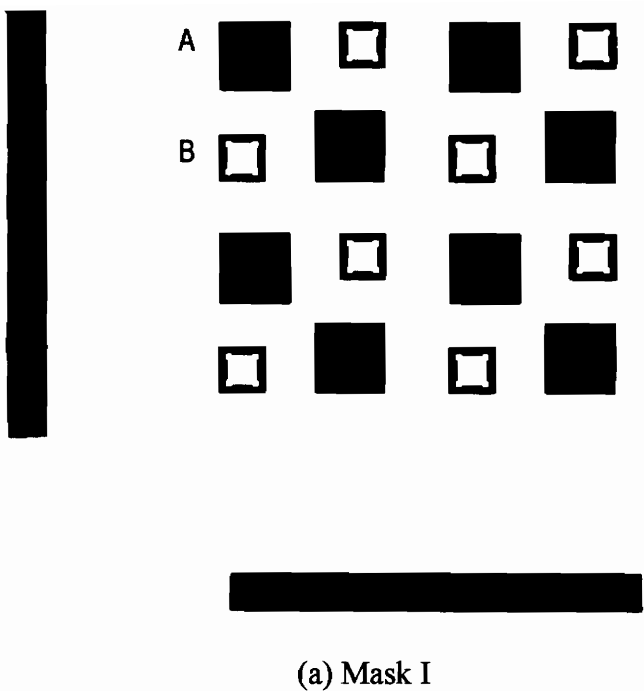
The purpose of this experiment was to demonstrate the feasibility of producing complex structures using a multi-step variation of the etching procedure described in Chapter 3. To this end, two different masks were designed for use in a two-step etching process. The plan was to etch a wafer with one mask, then re-oxidize the wafer, pattern it, and etch it using the second mask. Originally it was assumed that the polished side of the wafer would be used for both patterning steps. However, application of photoresist would be more difficult for the second step due to the depth of the initial etch pits; the photoresist would be much thicker in some areas than in others, leading to exposure problems during patterning. In order to circumvent this problem, it was decided that the second mask would be applied to the opposite side of the wafer, so variations in photoresist thickness on the etched side would be insignificant. Using opposite sides of the wafer did increase the difficulty of aligning the two masks properly, but this complication was slight compared to the issue of photoresist thickness.

It should be noted at this point that certain applications might require that the second mask be used on the same side of the wafer. For example, if some openings were

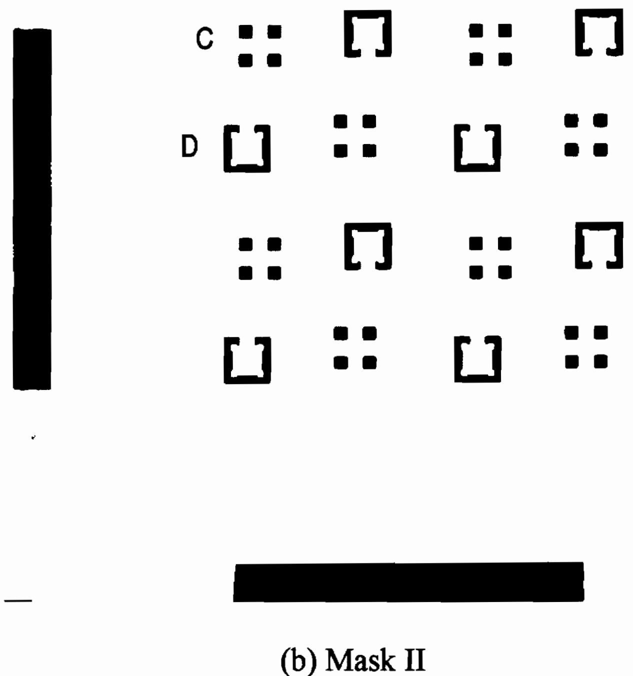
intended to be used as nozzles, the intended direction of fluid flow would determine the necessary etch direction. For my particular structures, discussed below, the direction of the etching is not critical. The Conclusions section of this chapter (§4.5) will discuss how this same-side patterning might be handled.

The mask patterns were drawn on Rubylith using AutoCad® before being photo-reduced. These patterns are shown in Figure 4-1. (Note that the color is inverted from the negatives used to expose the photoresist.) Because the masks were designed to be used on opposite sides of the wafer, Mask II was actually flipped over before it was applied to the back side of the wafer. The two wide black stripes on each mask actually represent clear areas in the negatives used to pattern the photoresist. These stripes were not intended to be etching patterns, but instead were used to align the masks by placing the inside edge of each stripe along one of the wafer flats. For my experiment, the horizontal stripe in each pattern above corresponds to the primary wafer flat.

Feature "A" on Mask I is a wide square pit intended to create a thin diaphragm on the wafer. Part "C" on Mask II should subsequently create four holes through the diaphragm. The final structure should resemble a perforated diaphragm such as might be used in certain sensors or on an integrated microphone. Feature "B" on Mask I should create a square mesa structure. Overhanging tabs have been provided to protect the mesa's corners; the dimensions of these tabs were based on the experiments described in Chapter 3. Once the mesa has been etched, part "D" of Mask II can be used to finish etching around the square, leaving it supported by a thin cantilever beam. The final structure should be similar to the cantilevered masses created in the earlier experiments, but the thinned beam will make this structure much more practical for use as an accelerometer. The thickness of both the diaphragm and the cantilever beam will be determined by the length of time the wafer is etched with each of the masks.



(a) Mask I



(b) Mask II

Figure 4-1. Masks for two-step etching experiment (Actual size). Black areas indicate openings in oxide layer. Letters have been added to identify features.

4.2 Two-Step Etching Experiments

4.2.1 First Etching Step

The first etching step was accomplished using the procedure outlined in the previous chapter. The first wafer was patterned on the polished side with Mask I. The wafer was then etched for about 13 hours, after which the depth of the etched pattern was measured to be 165 μm.

Since the masks were applied to opposite sides of the wafer, it was expected that it would make no difference which pattern was etched first. (If both masks had been applied to the same side, Mask I would have to be used first.) To confirm this expectation, a second wafer was patterned on the unpolished side first using Mask II. It was then etched for 16 hours to a depth of 190 μm. The results of this etching also indicated that the unpolished side of the wafer can be etched in exactly the same manner as the polished side. The etched surfaces, including the bottom surfaces of the etch pits, are just as smooth as those etched from the polished side. Only the surface of the bulk wafer is different.

After the first side of each wafer had been etched, the oxide coatings on both wafers were removed by immersing each wafer in BOE for 30 minutes. Once the oxide was removed, the wafers were shipped to N. C. State University for re-oxidation. A 1.0 μm layer of SiO_2 was thermally grown on each of the wafers for use in the second etching step.

4.2.2 Second Etching Step

Serious problems were encountered when patterning the wafers in preparation for the second etching step. The wafers were cleaned as before and photoresist was applied to both sides. The smooth, unetched side of each wafer was easily coated, but the nonplanar nature of the previously etched sides made it impossible to apply a consistent

layer of photoresist. Thick deposits of photoresist did not adhere well to the surface, while thin spots did not provide adequate protection of the underlying oxide layer. A number of attempts were made using different techniques to try to improve the quality of the photoresist coat. Ultimately, one of the wafers was coated by brushing and one by spinning. Each of the methods is described in more detail in the paragraphs which follow.

A number of brushing experiments were carried out in order to determine the optimum application procedure for the first wafer. Most of these experiments failed when the photoresist was brought into contact with water or the developer; the thick photoresist did not adhere to the wafer, and it simply flaked off when it became wet. A telephone call to Shipley, the photoresist manufacturer, revealed that for thick coats, a hot plate should be used for baking the photoresist instead of an oven. The Shipley engineer stated that in a convection heating oven, a thick photoresist layer might not dry properly because the solvents would be driven out of the surface of the photoresist first, possibly forming a hard "skin" on top of the layer. Thus, the remaining solvents would be trapped within the photoresist, leading to poor adhesion. He suggested that the use of a hot plate, rather than an oven, might aid in driving out the solvents from deep within the photoresist. Further experimentation seemed to confirm these recommendations.

The first wafer was patterned by spinning photoresist onto the unetched side and processing it as usual. After the pattern was developed and the photoresist had been hard-baked, the previously-etched side was coated with a thicker layer of photoresist which was applied with a brush. This layer was baked on a hot plate at 110° C for a full hour, resulting in a smooth, hard protective coat. This photoresist coat was not exposed to a developer solution, but it did not crack or flake off in DI water. At this point the wafer was etched in 10:1 BOE for about 20 minutes to pattern the oxide layer. (It did not take 25-30 minutes, as listed in §3.6, because this oxide layer was not as thick as the original oxide layer.) Etching proceeded normally at a temperature of 50° C. It soon became

apparent, however, that the brushed-on photoresist had not protected the oxide on the previously-etched side of the wafer. Most of that side, except for some areas in the etched patterns themselves, was vigorously attacked by the KOH. Complete etch-through of the patterns took 24 hours, which was much longer than expected. Apparently this was due to the much larger surface area which was actively etching. The results were poor, since much of the wafer had etched to approximately half its original thickness. Most of the patterns themselves came out well, but there was not enough of the bulk wafer left supporting the structures to allow them to be used as practical devices. Based on the appearance of the wafer immediately after the BOE etching, it is believed that tiny channels must have formed under the photoresist layer, probably as a result of the brushing. These channels allowed the BOE to reach the underlying oxide, which was not intended to be removed.

The second wafer was patterned and protected by spinning a coat of photoresist onto both sides of the wafer. The unetched side was coated in the usual manner, but coating the previously etched side was more difficult due to the nonplanar nature of the surface. Several attempts were required to find the combination of rotational speed and spin time which produced the best results. Speeds from 100 rpm to over 3000 rpm were tried, and the spinning time was varied from as little as 15 seconds at high speeds to as much as 2 minutes at low speeds. In some cases, the wafer surface was not entirely covered, while in others, the photoresist was so thick in some places that it failed to adhere to the wafer. The best coverage was obtained by spinning the wafer at 1000 rpm for 30 seconds.

Once a reasonable spinning procedure had been determined, the wafer was processed in the usual manner, using the oven to bake the photoresist on both sides of the wafer. The only deviation from the standard procedure given in Chapter 3 was the spin speed and time for the etched side. The photoresist thickness was inconsistent due to the

etch pits, but the entire wafer did appear to be covered. After the photoresist was hard-baked, the wafer was etched in 10:1 BOE for 20 minutes to pattern the oxide. Then the wafer was etched in a standard KOH solution at 50° C. Complete etch-through of the patterns required 28 hours, a great deal longer than was expected. This time, the bulk of the wafer was well-protected from the etchant. The front-to-backside alignment of the two masks also turned out to be very good, but the etched structures themselves turned out to be very rough. While the cantilevered masses turned out reasonably well, the square holes in the perforated diaphragms etched out into larger, rough-sided openings. In many cases, these openings were roughly trapezoidal. Given the orientation of the trapezoids on the wafer, I believe that they were formed due to poor photoresist coverage in the innermost corners of the previously-etched pits. It appears that, at least in the case of the perforated diaphragms, it would be better to use Mask I first, because the larger openings would be more forgiving when using spun-on photoresist.

4.2.3 Results of Two-Step Etching Experiments

The etching results described above are summarized in the following table:

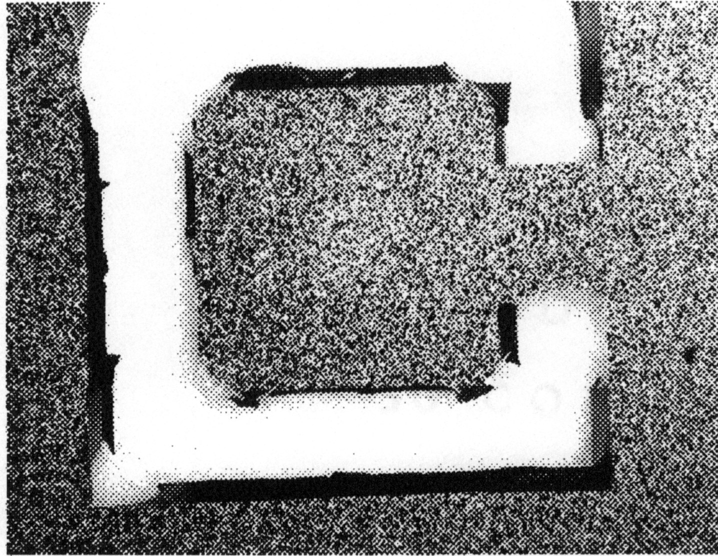
Table 4-1. Two-step etching results.

	1st Etch:			Etched-Side	2nd Etch:	
Wafer:	Initial Mask:	Time:	Depth:	Photoresist:	Time:	Results:
1	I	13 hr	165 μm	Brushed	24 hr	Patterns okay; Much of bulk wafer etched away on brushed side
2	II	16 hr	190 μm	Spun	28 hr	Poor pattern definition; Diaphragm openings eroded; Bulk of wafer well protected

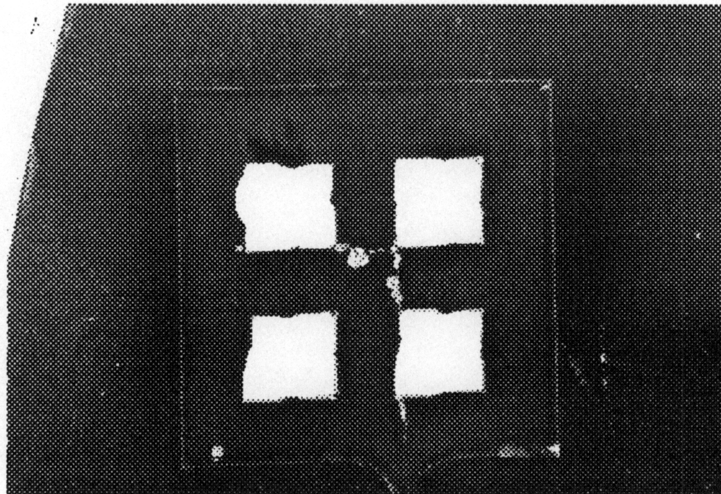
Note: All etching was done using 400 g:1 L KOH:DI water at a temperature of 50° C.

The results listed above are illustrated in a pair of photographs which follow. The first, Photograph 4-1, shows the "top" (beam) side of one of the cantilevered masses on the first wafer. This side was the second side to be etched, so the wafer surface shows no damage. However, the (111) edges of the structure are broken and uneven in many places due to etching of the bulk wafer on the other side. The photograph does show a couple of good results as well: the corner tabs did a good job of maintaining the mass's square shape, and the alignment of Masks I and II was excellent.

Photograph 4-2 shows the concave side of one of the perforated diaphragms on the second wafer. This was also the second side to be etched. In this photograph, it is easy to see how the edges of the small square pits eroded due to poor photoresist coverage, while the square sides of the newly-etched large pit (which forms the diaphragm) are straight and smooth.



Photograph 4-1. Cantilevered mass, first wafer (13x magnification).



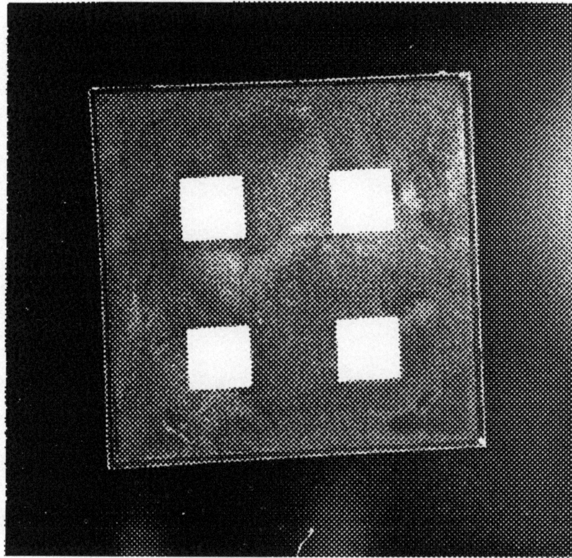
Photograph 4-2. Erosion of diaphragm openings, second wafer (6.5x magnification).

4.3 Simultaneous Double-Sided Etching

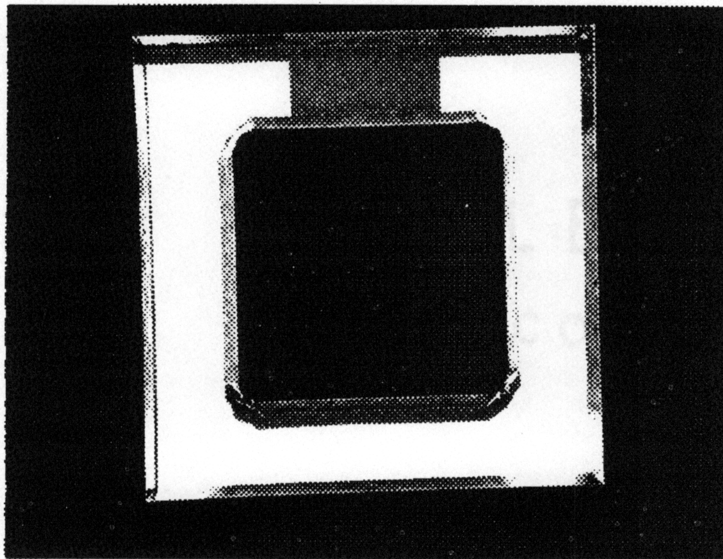
An additional approach was devised which could be used to fabricate the same structures with much better results. This time, both sides of the wafer were processed at once, and the two patterns etched until they met in the center of the wafer. The wafer was cleaned as before, and photoresist was applied using the procedure given in Chapter 3. This time, however, both sides were masked and exposed, using the masks shown above. The wafer was held vertically during the developing process so that both sides could be viewed. Then the wafer was hard-baked and prepared for etching using the procedure developed in Chapter 3. Etching took 22.75 hours and the results were excellent. The features were sharply defined and the surfaces were very smooth. Photographs of the results are included on the following pages.

Photograph 4-3 shows the concave side of one of the perforated diaphragms. Note the dramatic improvement over the results shown in Photograph 4-2. The simultaneous etching has created a structure with sharply defined square holes and very smooth surfaces.

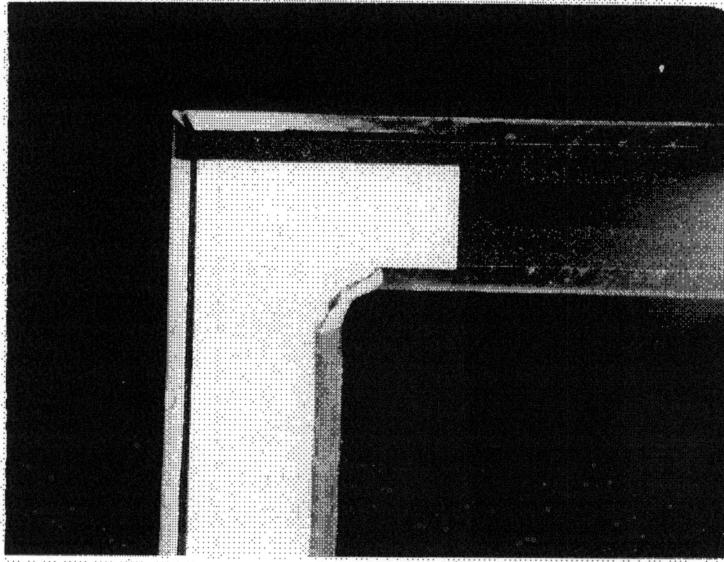
The dramatic improvements over the earlier experiments are seen even more clearly in Photographs 4-4 and 4-5, which show one of the cantilevered masses created by simultaneous etching. Note the clarity and definition of the pattern shown in Photograph 4-4. The masses created on this wafer maintained their square corners better than any others in my experiments. The only flaw in this particular wafer was a very slight misalignment of the two masks relative to one another. Photograph 4-5 shows a close-up of the slight "shelf" created when the two openings met.



Photograph 4-3. Perforated diaphragm resulting from simultaneous etching (6.5x magnification).



Photograph 4-4. Cantilevered mass created using simultaneous etching (11.5x magnification).



Photograph 4-5. Close-up showing slight degree of misalignment (23x magnification).

This simultaneous etching method has several major advantages over the two-step process described earlier. First, a number of lengthy process steps are eliminated altogether, since there is no need to re-oxidize the wafer or pattern it a second time. This has the added benefit of circumventing all the problems associated with applying photoresist to the previously-etched wafer surface. Second, the total KOH etching time is approximately halved, since both etchings are performed at once. This is not only important from the point of view of time savings, but also reduces the effects of imperfections in the oxide layer, since defects have less time to form unintended etch pits. Altogether, the use of double-sided etching greatly simplifies the etching process, resulting in both better and faster results.

It might be noted that the double-sided technique has one limitation that the two-step process does not: a loss of control over the etch depth of one pattern relative to the other. In the two-step case, we were able to determine the thickness of the cantilever support beam and the perforated diaphragm by varying the duration of each etch step. In this case, however, we are limited to letting the patterns meet in the center of the wafer, so the thickness of those elements is simply half the wafer thickness. If necessary, this limitation could be overcome without too much additional work. The etch-delaying technique described in §2.1.3 could be implemented by altering the mask patterns slightly, adding oxide meshes where needed to delay etching in certain areas.

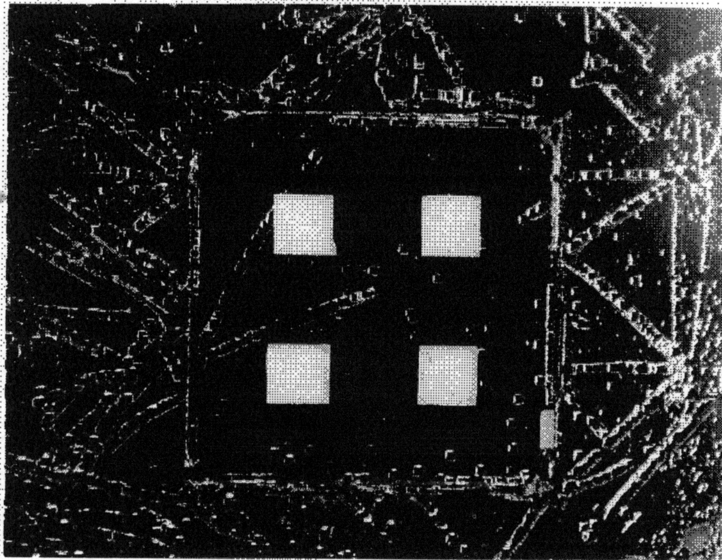
4.4 High-Temperature Etching

In an effort to further refine the etching process, another pair of etching experiments was conducted at a higher etchant temperature. Noting that other researchers commonly use etchant temperatures of about 80° C in order to speed the etching process, I decided to repeat the two-step and simultaneous etching processes with the KOH solution at that temperature.

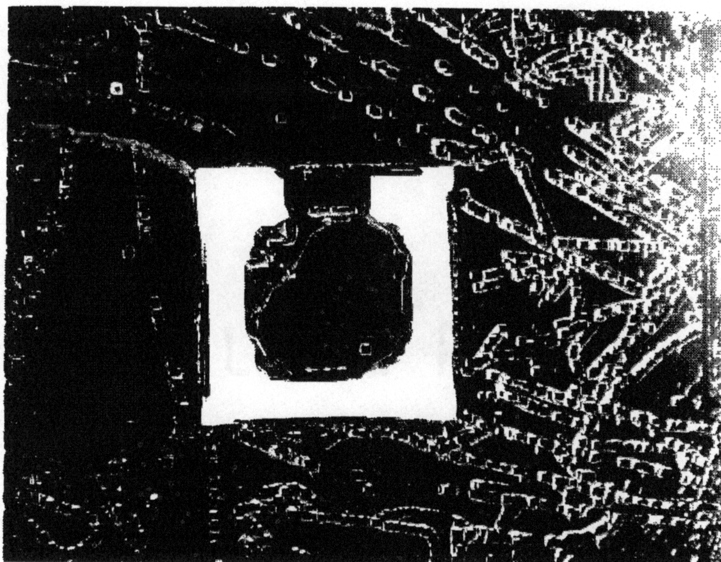
The first step was to prepare a third wafer for the two-step experiment. This wafer was prepared in much the same manner as the previous two-step wafers. The initial etch utilized Mask I on the polished side in a standard KOH solution at 50° C. After 15 hours, the etch depth was measured to be 180 μm. The wafer was then re-oxidized and prepared for the second etch step.

Patterning for the second etch step was accomplished by spinning the photoresist onto both sides of the wafer, using the standard procedure for the unetched side and 60 seconds at 1000 rpm for the previously etched side (i.e., exactly the same procedure as Wafer 2 in §4.2.2). After patterning the oxide layer with 10:1 BOE, though, the wafer was etched in a 400 g:1 L KOH:DI water solution heated to 80° C. This time the total etch-through time was only 5.5 hours, about four times as fast as the 50° C etches. However, the higher temperature had an even greater effect on the oxide etch rate. The oxide layer protecting the wafer surface began to break up after only 4.5 hours, allowing the etchant to attack large areas of the wafer surface. As a result, the structures which were created were nearly as rough as those on Wafer 2 (see above). The loss of the oxide caused widespread pitting and surface damage on both sides of the wafer. In addition, each of the cantilevered masses suffered erosion of the corner nearest the wafer's edge, a sure sign of inadequate photoresist coverage.

Photographs of the etching results have been included for comparison with the 50° C results. Photograph 4-6 shows a perforated diaphragm from this wafer. Note that while the pattern definition is somewhat better than before (cf. Photograph 4-2), the wafer is covered with tiny etch pits formed as the oxide broke up. Photograph 4-7 shows one of the cantilevered masses; in addition to similar surface damage, note the corner which has eroded. This erosion occurred on the previously etched side of the wafer, and only to the corners nearest the wafer edge, so the erosion was most likely caused by poor photoresist coverage during the spinning process.



Photograph 4-6. Perforated diaphragm with surface damage due to oxide loss (6.5x magnification).



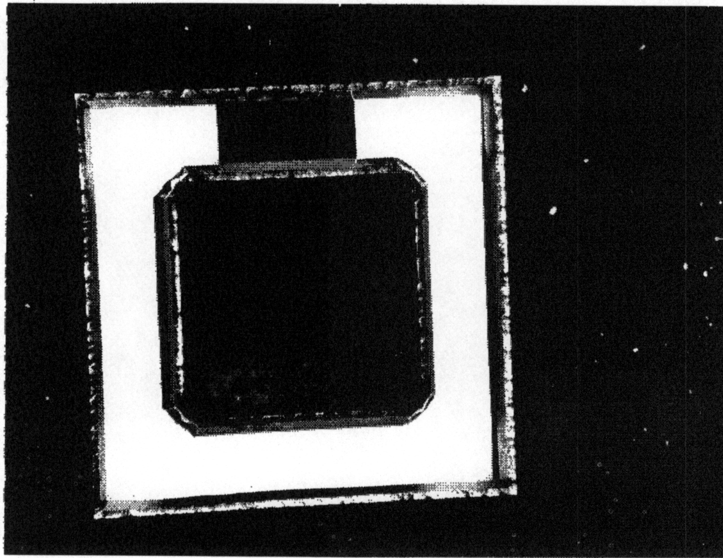
Photograph 4-7. Cantilevered mass formed by high-temperature two-step process (6.5x magnification).

The second high-temperature etching experiment was a repeat of the double-sided, simultaneous etching process described in §4.3. The wafer was prepared and patterned in exactly the same manner. Then it was etched in a standard KOH solution at 80° C. This time the etching process took only four hours to reach completion, a significant time savings over the 22.75 hours required at 50° C. However, the oxide layer (1.5 μm thick) did begin to break up about 20 minutes or so before the etching was completed. The surface damage was not very significant, though, and the results were quite good. Also, the alignment of the two masks was virtually perfect, resulting in nearly ideal structures. The calculated etch rate for this experiment was 0.8 μm/min, which is in complete agreement with the rates reported by Kendall [13] and other researchers (see §2.2).

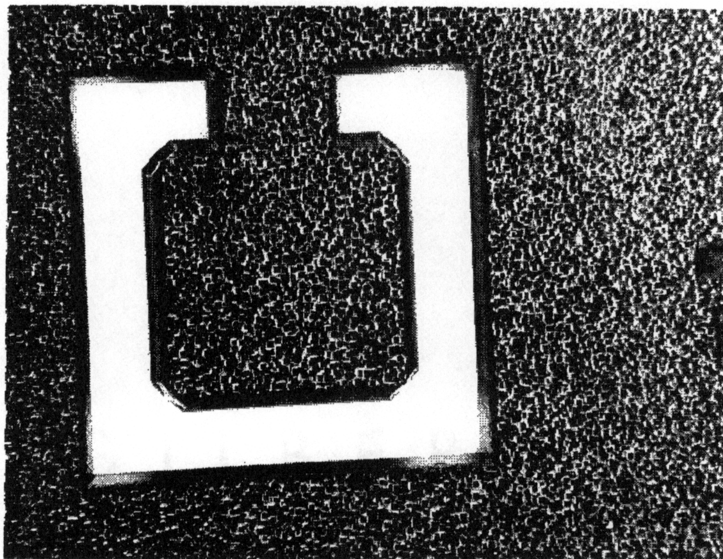
Photographs of the results are included for comparison with the results from other methods detailed in this chapter. The excellent pattern definition which can be achieved with simultaneous etching is clearly displayed in Photograph 4-8, which shows one of the cantilevered masses created in this experiment. Photograph 4-9 shows the other side of the same structure, again demonstrating nearly ideal pattern definition. Microscopic etch pits on the unpolished surface of the wafer show up as a pattern of tiny squares in this picture. These formed upon loss of the oxide layer during etching, but they did not have time to etch deeply, and the wafer appears smooth to the naked eye.

The perforated diaphragms fabricated in this experiment were virtually identical to the one shown in Photograph 4-3.

Overall, this method was highly successful. In order to make better use of it in future experiments, one should increase the thickness of the oxide layer to insure that it does not break down during the etching process.



Photograph 4-8. Cantilevered mass created by simultaneous etching at 80° C (10x magnification).



Photograph 4-9. Cantilevered mass, beam side (10x magnification).

4.5 Summary and Conclusions

This chapter has discussed my efforts to demonstrate the feasibility of producing anisotropically etched structures using multiple etching steps with different masks. In addition, an alternative method of fabricating two-mask structures using simultaneous double-sided etching was explored. Finally, both methods were repeated at a higher etchant temperature in order to compare the results and possibly refine the etching procedure. The most important details of all these experiments are summarized below:

Table 4-2. Summary of multi-mask etching experiments.

(a) Two-step etching processes:

Wafer:	Initial Mask:	Etched-Side Photoresist:	Temperature of 2nd Etch:	Total Etch Time:	Results:
1	I	Brushed	50° C	37 hr	Patterns okay; Bulk wafer loss due to inadequate protection of brushed side
2	II	Spun	50° C	44 hr	Poor diaphragm openings due to unprotected corners; Cantilevered masses okay
3	I	Spun	80° C	20.5 hr	Diaphragms okay; Mesa corners eroded due to photoresist inconsistencies; Oxide broke up too early

(b) Simultaneous double-sided etching experiments:

Wafer:	Etchant Temperature:	Total Etch Time:	Results:
1	50° C	22.75 hr	Nearly perfect; Only problem was alignment of masks
2	80° C	4 hr	Excellent results; Oxide broke up slightly early (~20 minutes)

Notes: All etching was performed using a solution of 400 g:1 L KOH:DI water.
First etch for all two-step processes used an etchant temperature of 50° C.

A number of conclusions can be drawn from these experiments. The two-step processes, in which the wafers were patterned, etched, re-oxidized, and then patterned and etched again, met with limited success. Nevertheless, these results could be improved by making some slight changes; then the process could be extended to experiments with more than two etching steps. One of the most important, and also most easily implemented, improvements would be to choose the mask order based on the specific structure one intends to fabricate. Spinning on the photoresist was much more effective than brushing, and the results of wafers 2 and 3, above, clearly indicate that the initial mask selection determines which structures will be adequately covered. In future experiments, the use of a lower-viscosity photoresist might also allow better, more consistent coverage.

Alternatives to the use of photoresist and wet patterning techniques do exist, but are not currently available in our laboratories. For example, when dealing with highly nonplanar surfaces, some researchers have used plasma etching, or ion milling, to pattern the oxide (or nitride) masking layer. Others have used scanned laser or electron beams to pattern wafers for multiple etching steps [14]. Here at Virginia Tech, however, spinning on the photoresist appears to be the best available method to achieve reasonable protection of the oxide layer.

The simultaneous etching of both sides of the wafer was by far the most successful of my experiments. This method is primarily applicable to two-mask experiments, but might also be used in multi-mask (say, three or four masks) experiments, where double-mask etch steps would reduce overall etching and re-oxidation time, as well as decrease the size and number of surface defects.

The use of higher etchant temperatures has both advantages and disadvantages. For applications where shorter etch times are more important, such as in the mass-production of a commercial device, high temperatures could be very useful. However, one must provide a much thicker oxide layer to protect the wafer, and the quality of the

structures suffers slightly when the wafers are etched at higher temperatures. Thus, for low-quantity applications such as research, or when fabricating extremely small, high-precision devices, the slower but smoother low-temperature etch might be preferable.

Chapter 5
Conclusion

Anisotropic etching for the bulk micromachining of silicon wafers has already proven its worth in a number of practical applications. These applications include devices such as miniature accelerometers, inkjet printer nozzles, and a wide variety of miniature sensors. Concepts and ideas also exist for a great many new applications of anisotropic etching, but most are dependent on advances in current technology. Ultimately, researchers would like to achieve the complete integration of anisotropic etching, silicon fusion bonding methods, and normal IC device fabrication processes. To make this integration possible, however, will require a great deal of further research in both the industrial and academic environments. The purpose of this thesis project is to pave the way for Virginia Tech to join in this research effort.

This thesis includes a step-by-step procedure for carrying out anisotropic etching in our lab. Experiments showed that this procedure, summarized in §3.6, produces results which are both reliable and reproducible. The experimental results agreed well with theoretical predictions; etch pits formed and surfaces eroded in accordance with the expected crystallographic dependencies. Further experiments examined the advantages and disadvantages of several modifications to the etching procedure. Double-sided etching was shown to produce good results, with no significant mask alignment problems. Multi-step etching was found to be feasible but more difficult

due to the need to apply photoresist to nonplanar surfaces. To produce an adequate coating, it was found that spinning on the photoresist was much more effective than brushing. One last set of experiments was performed to determine the effects of the

etchant temperature on the etch rate and the quality of the resulting structures. It was found that while 80° C etching produced reasonably good results in a short amount of time, 50° C etching produced higher quality results and was better suited to etching very small, high-resolution structures.

Suggestions for Further Research

A number of suggestions can be made for the continuation of this research. Short-term goals might include a few experiments to determine the effects of adding isopropyl alcohol to the etchant solution, as has been done by some researchers. Comparisons of experiments with and without isopropyl would help to further optimize the etching process. More complex experiments which could be undertaken at the present time would involve the combination of silicon fusion bonding techniques with anisotropic etching to create unique microstructures. Some commercial products already utilize bonding with an intermediary oxide layer, but the direct (non-insulating) bonding methods which have been demonstrated in our lab have a greater potential for future applications.

Long-term goals for continued research in this field include the use of boron-doped etch-stops and the fabrication of smaller structures at a much higher resolution. The use of boron doping will permit a wider variety of basic structural elements, since the etch-stops are not restricted by the geometry of crystallographic planes. Higher resolution and feature sizes 10-100 times smaller than those presented seem feasible in our lab, especially if the wafer cleaning processes can be optimized. Mask alignment will also become much more critical, perhaps requiring specialized fixtures or the use of a stepper.

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Vita

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Neil Townsend Hobbs

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