

**ANALYTICAL MODELING AND SIMULATION OF BICMOS
FOR VLSI CIRCUITS**

by

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(ABSTRACT)

Interest in BiCMOS technology has been generated recently due to the potential advantages this technology offers over conventional CMOS which enjoys widespread use in today's semiconductor industry. However, before BiCMOS can be readily adopted by the VLSI community, an understanding of the design issues and tradeoffs involved when utilizing it, must be achieved. The principal focus of this research is to move towards such an understanding through the means of analytical modeling and circuit simulation using PSPICE [1].

The device chosen for the modeling approach is the basic BiCMOS Inverting Buffer Driver. The model yields equations that characterize output rise and fall transients and quantify the delays incurred therein. At the end of the analysis, we have a composite set of delay equations that are a measure of the total gate delay and reflect the importance of individual device and circuit parameters in determining this delay. Further investigations conducted to determine the influence of device, circuit and process parameters on BiCMOS, indicate that this technology is far more resilient to variations in such parameters than CMOS. At the end of this research, we are able to make a definitive judgement about BiCMOS performance and its superiority over CMOS in the switching speed domain.

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Chapter 1

Introduction

BiCMOS is the newest technology to emerge on the VLSI horizon and promises to deliver better performance than CMOS, which currently dominates the VLSI market. Although the idea of integrating MOS and bipolar devices on a common wafer was proposed two decades back, it is only recently that commercial offerings utilizing BiCMOS have become available. However, before BiCMOS can become a major player in the VLSI market, a thorough understanding must be achieved regarding the design and processing tradeoffs involved when MOS and bipolar technologies are integrated. The principal aim of this research is to understand and evaluate BiCMOS technology through the methods of analytical modeling and circuit simulation.

Chapter 2 of this thesis provides a broad overview of BiCMOS and the potential benefits of utilizing it. The issues entailed by a shift to this technology and the historic precedent of the move to CMOS from NMOS are mentioned. The importance of processing technology in making BiCMOS a viable proposition is discussed and a brief description of fabrication techniques is provided. A review of the evolution of this

technology and recent developments in its implementation are also a subject of discussion.

Chapters 3 and 4 document the research that has been performed to model and simulate BiCMOS in order to determine the process, device and circuit parameters that influence its performance. In Chapter 3, the basic BiCMOS inverting buffer driver circuit is modeled analytically [7]. Both rising and falling output waveforms are considered. The step-by-step derivation explains the different regions of operation of the MOS and bipolar devices forming this circuit. The analysis itself is divided into different regions in time and models for each of these regions are described. The final products of the modeling process are sets of equations representing the change in the output voltage and the propagation delay through the gate, both in terms of circuit and device parameters. PSPICE simulations are then used to validate these theoretical results. Deviations, if any, are accounted for and justified. The modeling process provides us with insights about operation of the inverting buffer at the transistor level. It also helps us obtain a set of delay equations that allow a first approximation of gate delay to be made. Information regarding important parameters that affect this delay is also available.

The principal aim of Chapter 4 is to evaluate BiCMOS technology in relation to CMOS which is currently the most popular VLSI technology. The PSPICE circuit simulator is used as a tool for this evaluation [1]. Circuit simulators enable us to make accurate predictions about circuit performance without having to actually fabricate and test them - an expensive process given the type of technology we are dealing with. Derivatives of the SPICE circuit simulator are used almost universally for this purpose. PSPICE is one such popular version. The effects of variation in circuit, device and process parameters on BiCMOS performance are sought to be determined. Both MOS and BJT parameters are considered and results are viewed in the light of established analytical equations. Design issues, and tradeoffs necessitated by these results are also

discussed. Further studies are conducted regarding the switching characteristics of multi input BiCMOS gates and practical VLSI implementations of this technology. A definitive judgement about BiCMOS performance and its superiority over CMOS is then made.

Chapter 5 documents the conclusions that can be drawn from the analytical modeling and performance evaluation processes. A summary of the research performed and inferences drawn regarding BiCMOS is presented.

Chapter 2

An Overview of BiCMOS Technology

2.1 Introduction to BiCMOS

VLSI technology is constantly pushing towards new frontiers and the two main performance measures that characterize this advance are switching speed and power dissipation of devices. Traditionally, bipolar technology has demonstrated superior speed while MOS devices have always dissipated less power. These two technologies have evolved independently and carved specific applications for themselves. Bipolar chips have dominated markets such as fast memories, video signal processing and sensing while MOS chips are popular for slower but denser memories, gate arrays and microprocessors among others.

More specifically bipolar devices have an advantage in switching speed, analog capability and I/O (input-output) speed. MOS technology, now dominated by CMOS, scores in areas such as low power dissipation, noise margins and packaging density.

Additionally, the ability to integrate large, complex functions with high yields has resulted in CMOS far exceeding bipolar products with regard to volume of chips in today's market. CMOS technology has consistently been improved and scaled down in dimensions to yield high performance VLSI. Now, there is a feeling that CMOS fabrication technology may be pushing the limits of the laws of device physics and that new strategies must be devised. This forms the basis for a move towards BiCMOS.

The success of BiCMOS hinges on the ability to combine bipolar and CMOS technologies on the same wafer and obtain superior performance that would otherwise require super high density and expensive CMOS techniques. Bipolar processing techniques have always been more complex than CMOS processing methods. The principal tradeoff in BiCMOS is between additional process complexity and enhanced performance. In many ways, the argument to move towards BiCMOS is very similar to that which prompted the shift towards CMOS from NMOS in the early eighties. NMOS was the original VLSI MOS technology and remained dominant until density and power restraints suggested a move to CMOS with its ratioless logic style and near zero static power dissipation. NMOS proponents argued that process complexity and associated costs ruled out any serious challenges from CMOS. But, with advances in processing methods, CMOS soon caught up and then surpassed NMOS to become the dominant VLSI technology. BiCMOS poses the same kind of challenge to CMOS. Once again, as CMOS requires increased process complexity to deliver improved performance, its principal cost edge over BiCMOS will erode. In fact, the superior performance of BiCMOS can delay the move towards smaller dimensions and thereby extend the life of existing fabrication lines. There are also other advantages such as use of the bipolar epitaxial layer to suppress latchup which has been the single biggest negative factor for CMOS.

2.2 *BiCMOS processing technology*

Processing methods are the key to the success of BiCMOS since they will determine the viability of combining the two technologies on the same wafer. Therefore, it would be instructive to take a look at some of the strategies that may be employed for the purpose. In general, the approach while designing with BiCMOS would be to use bipolar devices in areas where speed is critical and MOS devices elsewhere. Hence, BiCMOS processes would utilize a base CMOS process with additional steps to realize bipolar devices.

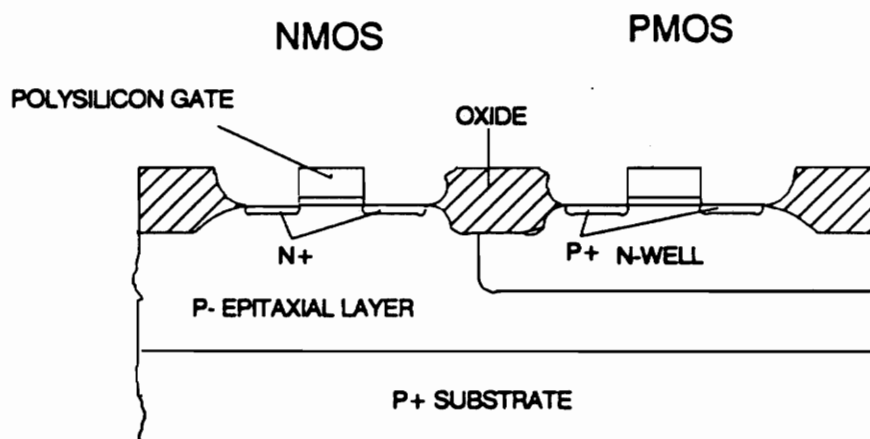
A typical N-well CMOS process that may be modified for BiCMOS is shown in Figure 2.1a [28]. The n channel device is built on a P- epitaxial layer which lies on a P+ substrate. The p channel device is built in an implanted N-well. The P+ substrate helps reduce latchup by providing a low impedance path through the vertical parasitic PNP transistor that causes it. The bipolar device may be added to this structure by using the PMOS N-well as the collector of the bipolar device and introducing an additional mask level for the P- base region. However, the N-well collector in this case would be lightly doped leading to high collector resistance which is undesirable. This may be overcome by introducing a buried N+ layer under the N-well. This layer also helps control latchup which means that the P- epitaxial layer on the heavily doped P+ substrate can be replaced by a P- substrate. A drawback of this approach is that P- substrate doping levels limit packing density. Increase in these levels leads to higher collector-to-substrate capacitance. Also, the N type epitaxial layer has to be counterdoped to isolate the N-well regions (P-wells for NMOS devices).

A solution to the above problems would be to self-align buried P layers to buried N+ regions. Bipolar packing density is improved by this step. However, collector to

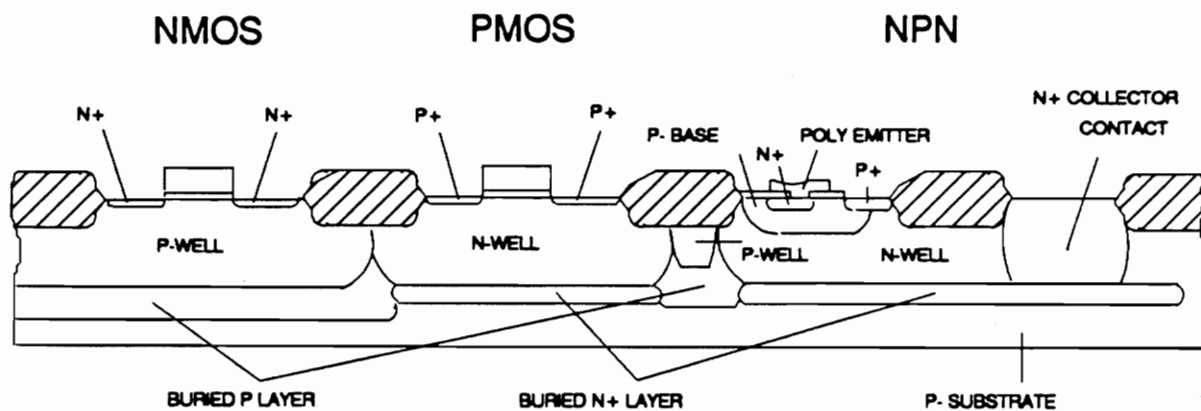
substrate capacitance is increased. The improved structure is shown in Figure 2.1b [28]. In general, use of a polysilicon emitter yields higher bipolar performance, since shallow emitters and narrow base widths are possible. Four additional mask levels (buried N⁺, deep N⁺ contact, P- base and emitter) are required to merge a BiCMOS process with CMOS process flow. The total mask count increases from ten to fourteen.

BiCMOS device isolation is a key factor in determining overall circuit performance and density. The tradeoffs between optimum speed, packing density and process complexity must be closely studied. High performance NPN devices require a heavily doped buried N⁺ layer to lower collector resistance under the epitaxial collector region. Hence, well formation in BiCMOS would be different from CMOS. In twin well CMOS, the N and P well doping profiles are optimized by separate diffusions - the background doping of the epitaxial layer is kept low to avoid the need for counterdoping during well formation.

The latchup phenomenon has been referred to in previous paragraphs. It occurs in CMOS devices due to the formation of a PNPN thyristor structure by the parasitic bipolar transistors resulting from the N and P well structure. The collector of one transistor feeds the base of the other and vice-versa. This can lead to high currents and ultimately, the destruction of the device. In essence, since BiCMOS process must be CMOS based, the N-well region which forms the NPN and PMOS transistors must be optimized. In areas where NMOS transistors are important, P-well optimization is important, with regard to isolation and mobility degradation. On the bipolar side, the N-well profile is a compromise between a thinner, heavier collector which leads to higher unity gain cutoff frequency and good current capability, and a lightly doped collector which allows larger breakdown voltages. From a CMOS viewpoint, well profiles must be optimized with respect to threshold voltages, parasitic capacitances and body effect.



CMOS Device Structure



BiCMOS Device Structure

Figure 2.1. CMOS and BiCMOS Device Structures

2.3 *BiCMOS Evolution and Advances*

The potential advantages of combining bipolar and MOS devices on the same chip were realized in 1969 [10]. The aim was to utilize the desirable features of both technologies. Common collector NPN devices were fabricated using a diffused N+ source-drain region as emitter, a diffused P- isolation region as base and a N- substrate as collector. Fabrication of a lateral NPN transistor is also described. The first industrial BiCMOS offerings were operational amplifiers in the mid-1970s, by RCA [28]. Stanford University and Texas Instruments developed the BIFET technology that was used in analog and power applications such as display drivers and voltage regulators. The thrust towards digital BiCMOS began only in the mid-80s with Hitachi, Toshiba and Motorola being the major players. For the remaining part of this section, we shall review developments in BiCMOS with specific references to processing techniques, memory design and other VLSI applications.

The static RAM area has probably felt the impact of BiCMOS more than any other category of VLSI chips. The most common approach to date has been to use BiCMOS in the critical delay paths and I/O while designing the memory cell in pure CMOS. A number of innovative designs with excellent performance have been reported. The discussion in [5] indicates that MOS technology provides the most straightforward and highest density memory array for static RAM (SRAM) design. The high performance area is dominated by emitter coupled logic (ECL). An advanced $1\mu\text{m}$ BiCMOS technology for a 256K SRAM is described. The process is an optimized 16 mask, double poly Si, double metal sequence. Effective channel length is $0.6\mu\text{m}$ for NMOS and $0.7\mu\text{m}$ for PMOS devices. The effect of both phosphorus and arsenic dopants to form polysilicon emitters, is described.

Another 256K SRAM with $1\mu\text{m}$ technology is discussed in [6]. The use of a poly emitter helps achieve a cutoff frequency of 9GHz. Effective channel lengths are $0.9\mu\text{m}$ for NMOS and $1.1\mu\text{m}$ for PMOS. A detailed schematic of the memory cell and I/O buffering is provided. Active power levels of 400mW and standby power of 150mW are reported. More 256K SRAM developments using BiCMOS technology, resulting in a die size of 213 mils X 356 mils have taken place [8]. The basic memory cell size is $6.7\mu\text{m}$ X $14.4\mu\text{m}$. A different approach has led to the development of a 512K RAM with both BiCMOS and ECL logic used [33]. A 5ns address time and 2ns write time have been achieved. The logic gate has a 150ps propagation delay and 4mW power dissipation. A combined memory-logic array configuration is adopted to reduce interconnection delays. $0.8\mu\text{m}$ BiCMOS with triple level polysilicon and aluminum is used. Bipolar base resistance and parasitic capacitances are reduced by an emitter-base self aligned structure and scaled down design rules. A 300 ohm base resistance and 11GHz cutoff frequency are achieved. Gate thickness for MOS devices is 20 nm.

Use of ECL need not be restricted to the peripheral circuits [34]. This design of a 3.5ns, 500mW 16K RAM uses wired OR logic and cascode differential amplifiers to achieve high speed. $0.5\mu\text{m}$ BiCMOS technology is used with a self aligned structure between the emitter and base electrode. A 8ns 1 megabit ECL BiCMOS RAM has also been developed [36]. The process is $0.8\mu\text{m}$ BiCMOS. This memory utilizes a $76\mu\text{m}^2$ full CMOS six transistor memory cell, a dual MOS current source BiCMOS sensing scheme, a BiCMOS current voltage reference network and a low capacitance decoding scheme to achieve a 8ns delay. The configurable memory architecture allows expandability up to 1Mb in units of 64Kb.

It has been mentioned that the ultimate factor deciding the success of BiCMOS would be processing technology. It is no surprise therefore that a number of innovative techniques have emerged here. A process utilizing high performance NPN devices has

been described [2]. Effective channel lengths for MOS devices are $0.5\mu\text{m}$. The structure enables high integration and low power to be achieved making it an ideal candidate for high speed logic circuits. It features single level polysilicon with double metal and vertical NPN transistors with walled, self aligned poly emitters. Optimal buried contacts are used between the polysilicon and all junctions on the silicon substrate. An early BiCMOS offering involved a $2\mu\text{m}$ process with 2 mask steps added to a two layer metal N well silicide CMOS process in order to fabricate poly emitter transistors [3]. Latchup is minimized by adding a $1\mu\text{m}$ epitaxial layer and adopting a retrograde P-well. The overall process flow attempts to achieve MOS and bipolar device compatibility. The performance of MOS devices at subthreshold voltages has been detailed.

A $0.8\mu\text{m}$ process used to fabricate a $117\mu\text{m}^2$ memory cell has been described in [14]. The cell employs a TiN interconnect to achieve a $5.6\mu\text{m} \times 20.9\mu\text{m}$ size. Bipolar devices are used mainly in the decoder and buffer circuits. A buried N+ layer and twin well structure is formed by implantation into a thin, intrinsically doped epitaxial layer. The process is single metal and double poly. A new non-overlapping super self-aligned structure (NOVA) has been proposed in [15]. The PMOS and NPN devices are built in the N-well with a buried layer. The low resistance N-wells suppress latchup and reduce collector resistance. An arsenic doped polysilicon gate is used. Effective channel lengths of $0.85\mu\text{m}$ are achieved for the MOS devices. Bipolar current gain of 100 and gate delay of 122ps are reported. A $0.8\mu\text{m}$ BiCMOS process with high unity gain cutoff frequency f_T has been developed [13]. An ion implanted emitter helps reduce costs. Arsenic is directly implanted to the substrate while an aluminum electrode is directly contacted to the emitter N+. Twin well CMOS with channel lengths of $0.8\mu\text{m}$ and $1\mu\text{m}$ and threshold voltages of +0.8V and -0.8V are achieved for NMOS and PMOS devices respectively. f_T of 7.5 GHz is reported. The paper suggests that in general, for a high speed sub micron BiCMOS gate, an ion implanted emitter with a buried N+ layer and

deep N⁺ collector is suitable. An interesting evaluation of phosphorus and arsenic doped emitters for a 1 μ m BiCMOS process appears in [17]. The process utilizes 16 mask levels, double level polysilicon and 2 levels of metallization. A 1.5 μ m epitaxial layer is combined with a N⁺ buried layer to provide an effective low resistance collector. The base implant is decided by the type of poly emitter. The phosphorus doped emitter can result in high emitter sheet resistance but lowers base resistance and is easier to manufacture. Use of phosphorus also allows better forward current gain and base transit time performance. Arsenic on the other hand, enables a f_T of 11.2GHz to be obtained, whereas this figure for phosphorus is only 3.2GHz.

In addition to memory design and processing publications related to BiCMOS applications in other fields are also available. A general procedure for worst case BiCMOS design is suggested in [18]. The methodology takes into account physical correlation between NPN and CMOS model parameters and results in a self consistent set of parameters for circuit simulations. Tradeoffs between FET and BJT design are discussed. The 'corners' approach which entails perturbation of a minimum number of parameters in a device model to simulate worst case conditions, is adopted. A general discussion on requirements for semi-custom BiCMOS is presented in [20]. It is proposed that three basic BiCMOS technologies will evolve - high performance, low cost and analog compatible. A suggestion that a 20-25% increase in die cost will result which can be justified only by performance improvements of 50% or more, is made. Judicious use of the technology should be able to achieve this. The main requirements for semi-custom IC's that are detailed include 1) rapid design and fabrication cycles 2) CAD tool compatibility 3) overall process flexibility. The main drawbacks of BiCMOS in this regard are fabrication costs and time, and the lack of CAD tools that can effectively handle integrated bipolar and MOS design.

Applications of BiCMOS in signal processing have emerged [21]. Design of a 10 bit video track-and-hold circuit has been described. This system provides competition to the hybrid technologies that have traditionally been used for such applications. A $1.1\mu\text{m}$ BiCMOS technology utilizing 5V supply voltages, capable of driving a 50 ohm load with 1 volt swing in either direction, is used. A f_T of 7GHz is achieved. The use of bipolar cascode devices in the transconductance amplifier minimizes phase margin degradation. PMOS input transistors provide high input impedance. Maximum power dissipation for this circuit is 1.2 watts. A 200 MHz 16 bit BiCMOS signal processor has been described in [31]. $0.8\mu\text{m}$ technology with triple layer aluminum interconnects is used. Speed improvements over a current $1.3\mu\text{m}$ process of 1.7 are reported. The BiCMOS circuits are concentrated in the driver stages and the I/O interface circuits.

Circuit level optimization using BiCMOS has been investigated in a number of publications. A merged CMOS/bipolar switch logic is introduced into the design of a BiCMOS ripple adder [22]. Bipolar levels of performance are attained without additional level conversion circuits. Speed enhancements by a factor of 5 over pure CMOS are attained. The basic gate is a merged CMOS/bipolar switch which enables CMOS/ECL level conversion and reduces propagation delay, area and power dissipation, without the need for an ECL differential pair. The technology scale is $1.5\mu\text{m}$. A single ended BiCMOS sense circuit which is noise insensitive enough to be used in a CMOS environment has been developed [23]. An analog current mirror is suggested to prevent the common emitter BJT from saturating. The process is $1\mu\text{m}/13\text{GHz}$ BiCMOS. A 32 bit adder with a delay of 12.8ns and power dissipation of 54.5 mW has been described. Improvements in the basic BiCMOS logic gate is the subject of discussion in [24]. The fact that lower supply voltages would lead to reduced MOS device currents that may not be sufficient to switch the bipolar devices, has been put forward. In addition, lowering of threshold voltages may require full logic swings in BiCMOS gates to avoid the flow

of DC currents in the following gate. In the proposed feedback schemes resistors and diodes are used to achieve a rail to rail logic swing. The diode version dissipates less power. 3 input NAND gate delays of 290 ps for a load of 0.6pF are reported.

More circuit level enhancements involve the design of a BiCMOS current source network which eliminates the impact of a drop in DC supply voltage, on ECL circuitry [26]. Using this network, reference voltages are generated locally so that ECL voltage levels are correctly referenced to local power supply potentials. The main feature of the network is a BiCMOS band gap reference circuit. A self feedback technique using a PMOS current mirror results in stable output voltage levels. BiCMOS opamps are used as analog current drivers. A suggestion that operating voltage may be lowered using an on chip conversion system is made in [32]. This can help avoid reliability problems due to lack of voltage tolerances in sub micron devices. A $0.8\mu\text{m}$ BiCMOS process based on an N-well structure, is used with added P base diffusion. Design of circuit components such as I/O buffers and voltage converters is discussed.

Use of BiCMOS for design of a programmable logic device (PLD) is suggested in [25]. This logic sequencer structure has functional density and flexibility like CMOS and bipolar like speed. The AND and OR arrays are designed for user programmability. An operating frequency of 76MHz with a 6ns clock to output delay is achieved. Input setup time is 7ns and power dissipation 370 mW. A $1.9\mu\text{m}$ technology with three layer metal and single layer poly is used. The critical path responsible for overall system delay has been described. Bipolar sense circuits are used due to their greater insensitivity to process variations. NPN beta of 100 and f_T of 13 GHz is also achieved. Use of cell based design methodology to develop a 500,000 transistor custom BiCMOS chip is described in [29]. $0.8\mu\text{m}$ BiCMOS is utilized. Automated adaptive macrocell and short-time custom VLSI methods are used to make the logical and physical design more flexible. The adaptive macrocell generate procedure consists of a logical description and a physical description

with general information. A circuit subsection consists of a Manchester static ALU with carry lookahead circuitry having an area advantage of upto 60% compared to standard techniques. Delay for 4 bits is 6ns at 3V. Another macrocell approach has been used to design a high performance 32 bit, 70MHz microprocessor, from a $1\mu m$ BiCMOS library [30]. The chip contains about 529,000 MOS devices and 8,000 NPNs. The overall strategy is to use CMOS based macrocells to increase packing density and bipolar cells in sense and drive circuits to enhance performance. A phase locked loop circuit is used to synchronize the on chip clock to an external clock. This is important because there is a danger of clock skews due to the high operating speeds. Pipelining and other advanced architectural concepts are also employed.

Chapter 3

Modeling the BiCMOS Inverting Buffer Driver

3.1 Introduction

BiCMOS is a combination of bipolar and CMOS technologies on the same wafer. Any modeling approach to BiCMOS devices can conveniently utilize readily available models of bipolar and CMOS devices. These models have been improved and refined ever since they were first proposed and are regarded as being fairly accurate. By modeling the BiCMOS inverting buffer driver analytically, we seek to gain an understanding about the various regions of operation of the constituent transistors. This enables us to develop techniques that would lead to optimized device performance in circuit applications. Further, the delay equations that are derived provide a first approximation of the principal device and circuit parameters that influence switching speeds. One can therefore make an estimation of the probable delays in circuits containing these devices.

The following sections of this chapter present an analytical modeling approach to the basic BiCMOS inverting buffer [7], [28]. The analysis consists of two main portions, one dealing with the output rise transient and the other with the output fall transient. Simple and closed form delay equations are also derived. These results are then compared with those obtained from SPICE simulations.

3.2 The BiCMOS Inverting Buffer Driver

The basic BiCMOS inverting buffer driver configuration is shown in Figure 3.1. It consists of four transistors - a PMOS, an NMOS and two bipolar NPN devices. These are marked in the figure. The operation of this inverter can be explained in the following manner. A high to low pulse at the input will cause the PMOS device (M1) to turn on and drive the base of the NPN transistor Q1 which is initially off. This base drive will eventually switch Q1 on and the load capacitance C_L will be charged to a voltage $V_{cc} - V_{BE(on)}$. The output is constrained from reaching V_{cc} by the base-emitter drop of Q1. This represents the output rise characteristic. When there is a low to high pulse at the input, M1 and consequently Q1 are turned off. NMOS transistor M2 is turned on and supplies base drive to Q2. Once Q2 is turned on, the load capacitance is quickly discharged to a voltage which is one diode drop above ground. This completes the output fall transient.

It is clear from the above description that this BiCMOS inverter does not possess rail to rail logic swing, i.e., it does not swing from ground to V_{cc} and vice versa. Both ends of the swing are constrained by one diode drop, typically 0.7 volts. Therefore threshold

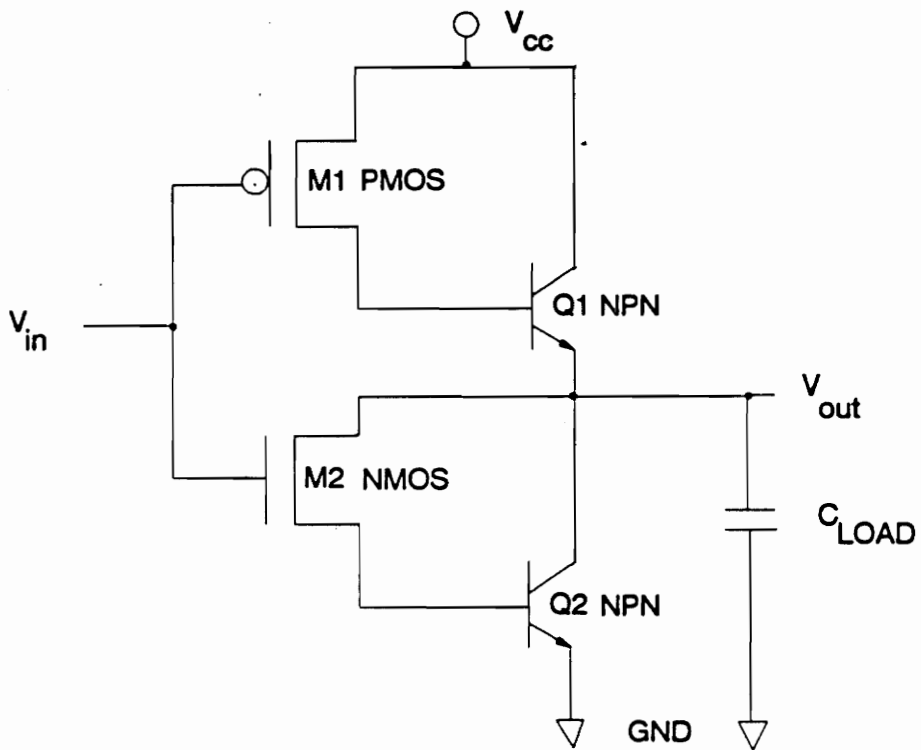


Figure 3.1. The BiCMOS Inverting Buffer Driver

voltages of the MOS devices must be closely monitored so that unwanted switching does not occur. An obvious advantage of this type of inverter is the high input impedance provided by the MOS devices and the low output impedance due to the BJTs. This results in good input-output isolation and drive capability. Hence the name "BiCMOS Inverting Buffer Driver". We are now in a position to analyze the rise and fall transients independently.

3.3 *Output Rise Characteristic Analysis*

We have already seen in the preceding section that the two devices responsible for the output rise characteristic are M1 and Q1. This subsection of the inverter is shown in Fig. 3.2 along with the external load capacitance coupled in parallel with the collector to substrate capacitance of Q2. For this analysis, we assume that both devices are off initially and V_{out} is zero. Now, a sharp high to low pulse is applied at V_{in} . M1 is turned on and enters the saturation region. A constant drain current feeds the base of Q1, which remains off until the base emitter voltage $V_{BE(on)}$ is reached at the base node. We denote the time at which this occurs as t_1 . Once Q1 is "on", it begins to supply current to the load capacitance C_L . The charging of $C_L + C_{CS}$ results in a rise in the output voltage V_{out} . When V_{out} reaches a certain voltage, M1 moves into the linear region. We denote the time of this occurrence as t_2 . Since switching delay is of primary importance in this analysis, a third region whose upper limit is set by the time it takes for V_{out} to reach $(V_{cc} - V_{BE(on)})/2$, taken as the approximate switching point, is considered. This time is

denoted as t_3 . These regions of operation are shown in Figure 3.3. We now consider each of these regions individually.

3.3.1 Region 1

This region is characterized by M1 operating in saturation and Q1 in the cutoff region. The current supplied by M1 is modeled by a single current source denoted by I_{dsat} . Q1 is modeled by a base resistance R_B , collector resistance R_C , collector capacitance C_C and an emitter capacitance C_E in series with the net output capacitance $C_L + C_{CS}$. The composite circuit model is shown in Figure 3.4a. Normally, $C_L + C_{CS}$ is much greater than C_E . Therefore the voltage at node B' is effectively the drop across C_E . In order to derive an expression for $V_{B'}$, we need to convert the circuit elements into frequency domain impedances and then use inverse Laplace transforms to arrive at relationships in the time domain. The circuit as configured in the s-domain is shown in Figure 3.4b. The steps leading to the derivation of an expression for $V_{B'}$ are worked in Appendix A.

The expression for $V_{B'}$ as derived in Appendix A is of the form,

$$V_{B'}(t) = \frac{I_{dsat}t}{C_E + C_C} + I_{dsat}R_C \left(\frac{C_C}{C_E + C_C} \right)^2 [1 - \exp(-\frac{t}{\tau})] \quad (3.1)$$

where

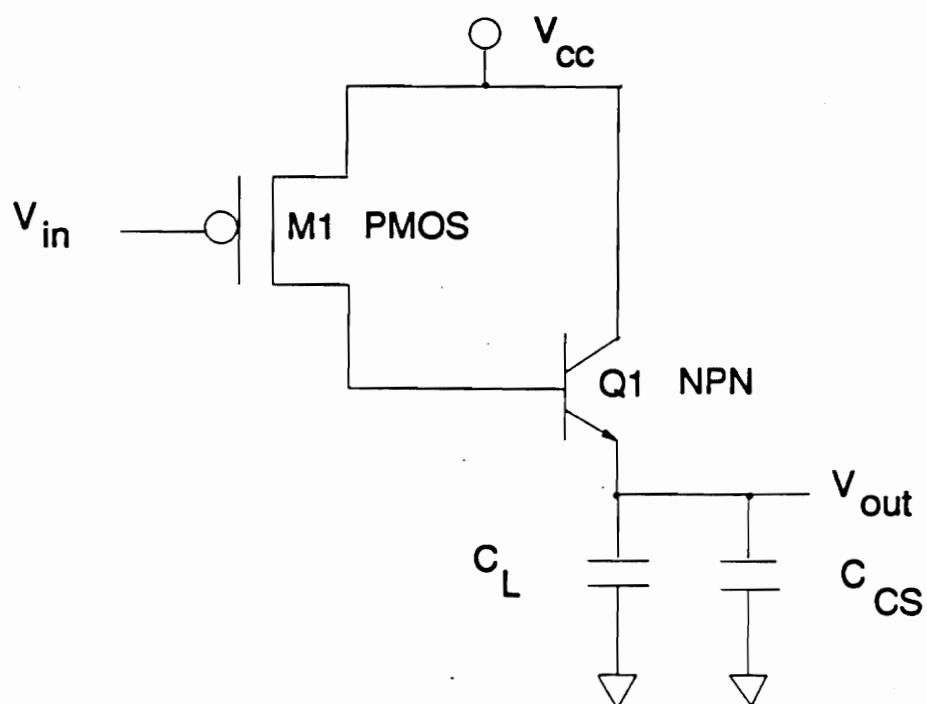


Figure 3.2. Output Charging Circuit

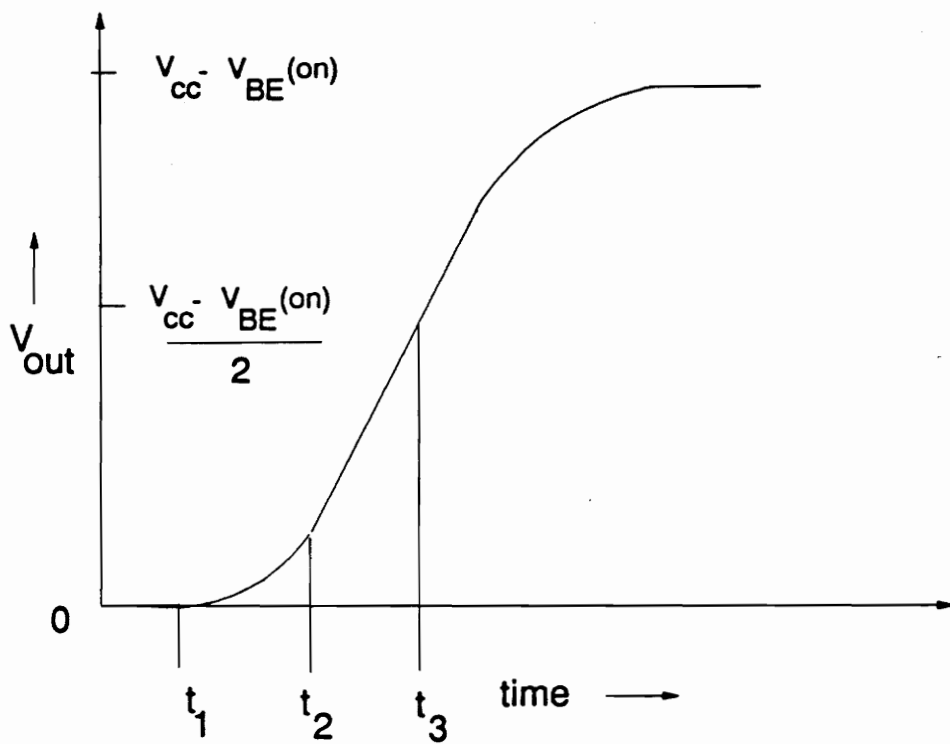
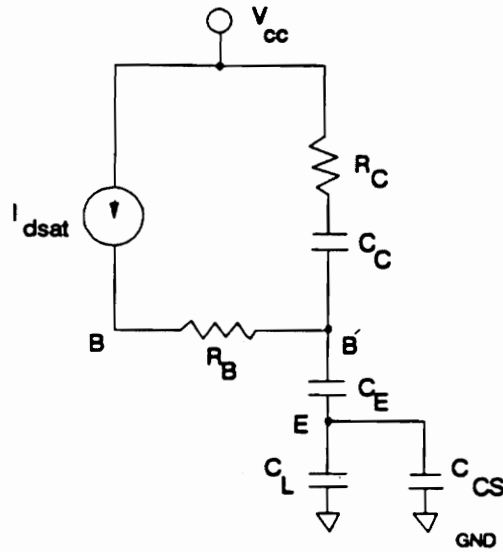
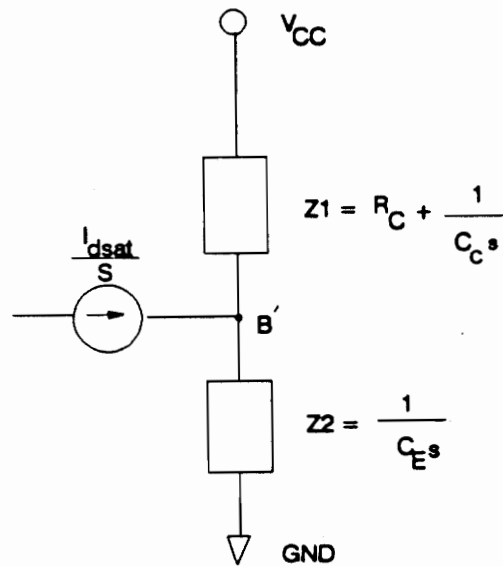


Figure 3.3. Inverter Regions of Operation for Rising Output



Circuit model for Region 1



Simplified model in s-domain

Figure 3.4. Region 1 circuit model and s-domain representation

$$I_{dsat} = \frac{W\mu\epsilon}{2t_{ox}L} (V_{cc} - |V_T|)^2 \quad (3.2)$$

μ is the mobility, ϵ is the permittivity, t_{ox} is the oxide thickness, W is the gate width, L is the gate length, V_{cc} is the supply voltage and V_T is the MOS threshold voltage. And, the term τ is of the form,

$$\tau = \frac{R_C C_E C_C}{C_E + C_C} \quad (3.3)$$

Typically, t_1 is much greater than τ so the exponential term in (3.1) can be neglected. Time delay t_1 is calculated by setting $V_B(t) = V_{BE(on)}$. The resulting expression for t_1 is

$$t_1 = (C_E + C_C) \frac{V_{BE(on)}}{I_{dsat}} - \frac{R_C C_C^2}{C_E + C_C} \quad (3.4)$$

The effective output voltage in region 1 is zero since, as mentioned earlier, $C_L + C_{cs} \gg C_E$. The total delay in this region, which is also the time it takes for Q1 to turn on, is given by (3.4).

3.3.2 Region 2

This region is characterized by M1 remaining in the saturation region and Q1 in the "on" state. The complete circuit model is shown in Figure 3.5. C_D is the base emitter diffusion capacitance. Since V_{BE} can be approximated by $V_{BE(on)}$ which is assumed to be constant, C_E can be neglected since

$$C_E \frac{dV_{BE}}{dt} = 0$$

Summing currents around the loop, we can write the following expression for the current flowing into the base of Q1 :

$$I_{dsat} = \frac{I_F}{\beta_F} + C_D \frac{dV_{B'E}}{dt'} + C_C \frac{d}{dt'} (V_{B'E} + I_C R_C + V_{out} - V_{CC}) \quad (3.5)$$

where

$$t' = t - t_1$$

and

$$I_F = I_s \exp\left(\frac{qV_{B'E}}{kT}\right) \quad (3.6)$$

which is the standard diode current relation. I_s is the saturation current, q is the electronic charge, k is the Boltzmann constant and T is the absolute temperature.

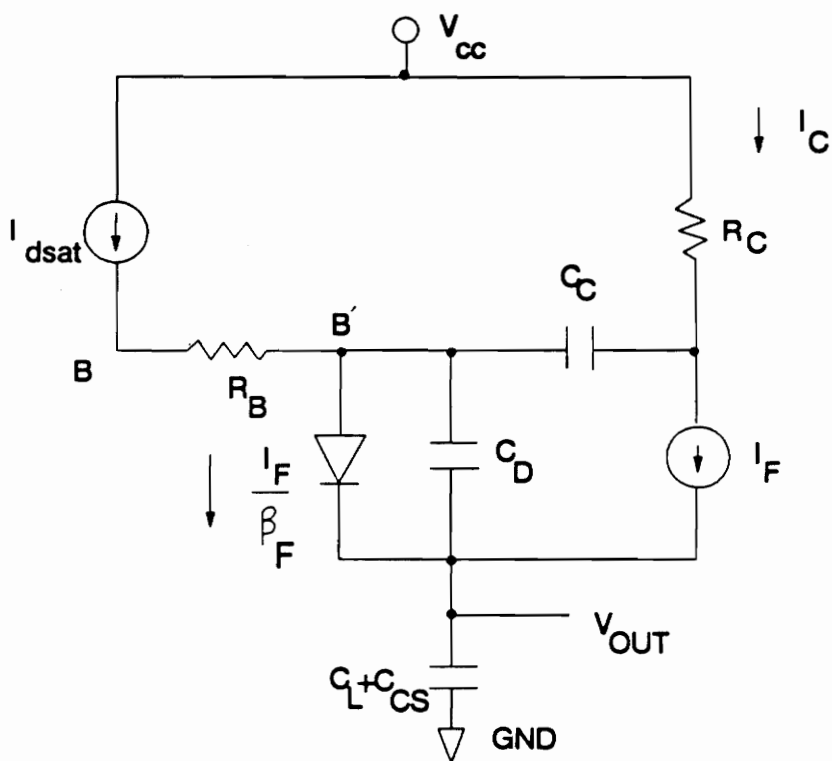


Figure 3.5. Region 2 circuit model

The base-emitter diffusion capacitance is given by [27] :

$$C_D = \frac{dQ_{DE}}{dV_{B'E}} = \frac{d(\tau_F I_{CC})}{dV_{B'E}} \quad (3.7)$$

Now I_{CC} is approximately equal to I_F so after differentiating according to (3.7) and simplifying we have

$$C_D = \frac{q}{kT} \tau_F I_F \quad (3.8)$$

where τ_F is the forward base transit time.

We know that when compared to V_{out} , V_{BE} is constant. Therefore the differential term involving $V_{B'E}$ in (3.5) can be set to zero.

Also, since $C_L + C_{CS} \gg C_C$, we can consider I_C as being equal to I_F and for standard values of β , $I_E \simeq I_C$. Hence,

$$I_F = I_S \left(\frac{qV_{B'E}}{kT} \right) \simeq (C_{CS} + C_L) \frac{dV_{out}}{dt'} \quad (3.9)$$

(3.5) can be written as

$$I_{dsat} = \left(\frac{1}{\beta_F} + \frac{C_C}{C_{CS} + C_L} + \frac{q\tau_F}{kT} \left(1 + \frac{R_C C_C}{\tau_F} \frac{dV_{B'E}}{dt'} \right) \right) I_F \quad (3.10)$$

Differentiating the expression for I_F in (3.9) we get

$$\frac{dI_F}{dt'} = I_F \frac{q}{KT} \frac{dV_{B'E}}{dt'}$$

The expression for I_{dsat} can then be rewritten as

$$I_{dsat} = \frac{1}{\beta^*} I_F + \tau^* \frac{dI_F}{dt'} \quad (3.11)$$

where

$$\frac{1}{\beta^*} = \frac{1}{\beta_F} + \frac{C_C}{C_{CS} + C_L}$$

and

$$\tau^* = \tau_F + R_C C_C$$

Solving differential equation (3.11) we get

$$I_F(t') = \beta^* I_{dsat} \left[1 - \exp\left(\frac{-t'}{\beta^* \tau^*} \right) \right]$$

Using this expression in (3.6) we get

$$\frac{dV_{out}}{dt'} = \frac{\beta' I_{dsat}}{C_{CS} + C_L} [1 - \exp(\frac{-t'}{\beta^* \tau^*})] \quad (3.12)$$

Integrating (3.12) with respect to t' and noting V_{out} is zero when $t' = 0$, we have

$$V_{out}(t') = \frac{\beta^* I_{dsat}}{C_{CS} + C_L} \{t' - \beta^* \tau^* (1 - \exp(\frac{-t'}{\beta^* \tau^*}))\} \quad (3.13)$$

Since M1 is still in saturation, the expression for I_{dsat} is the same as in (3.2). The end of region 2 which is marked by t_2 , is the time at which M1 comes out of saturation. This occurs when the gate to drain voltage of M1 is greater than the threshold i.e. when

$$V_{out} = |V_T| - V_{BE(on)}$$

since the input voltage is zero.

We have to plug this value into (3.12) and solve for t' . To do this we have to simplify (3.12) by expanding the exponential term in a Taylor's series. This is possible since t' is normally $\ll \beta^* \tau^*$. We retain terms up to the second degree, simplify and obtain a quadratic equation with the solution,

$$t' = \sqrt{(C_L + C_{CS}) (|V_T| - V_{BE(on)}) \frac{\tau^*}{I_{dsat}}} \quad (3.14)$$

The Taylor's series simplification is explained in Appendix A. Since $t' = t_2 - t_1$, we have an expression for the delay between the time Q1 turns on and M1 enters the linear region. The total delay at the end of Region 2 is the sum of delays indicated by equations (3.4) and (3.14).

3.3.3 Region 3

In this region M1 has just moved out of saturation into the linear mode while Q1 remains "on". So, the only difference from the model in Region 2 is that M1 is represented by a channel resistance instead of a current source. The complete model is shown in Figure 3.6. We can write the following expression for the current flowing into the base of Q1 :

$$I_B = \frac{V_{CC} - V_{B'E} - V_{out}}{R_{CH} + R_B} \quad (3.15)$$

$$= \frac{I_F}{\beta_F} + C_D \frac{dV_{B'E}}{dt'} + C_C \frac{d}{dt'} (V_{B'E} + I_C R_C + V_{out} - V_{CC})$$

Here, $t'' = t - t_2$.

Using the same assumptions as in the Region 2 analysis, we can write for (3.15) :

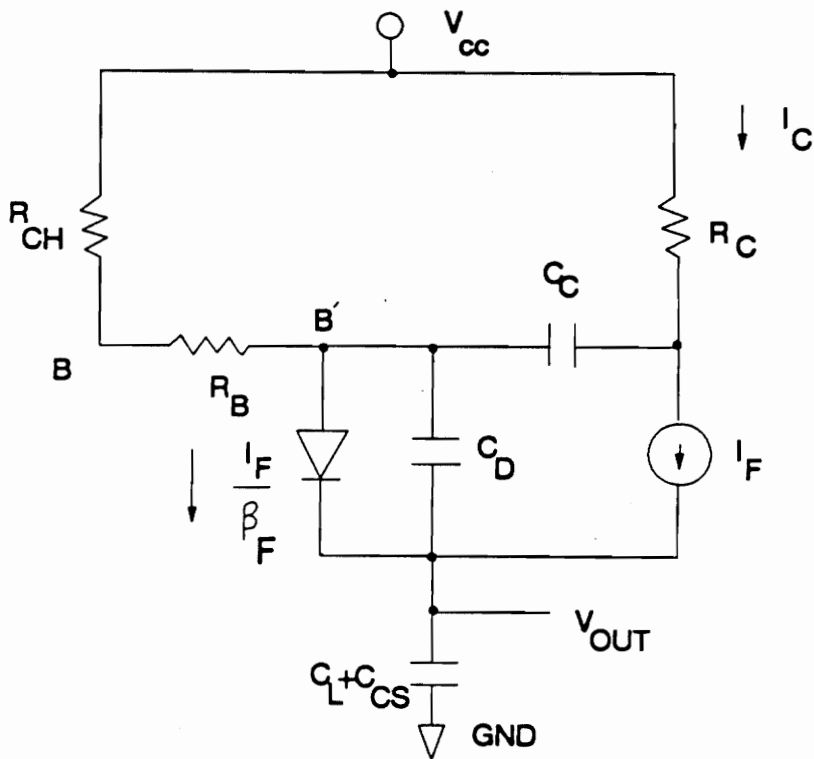


Figure 3.6. Region 3 circuit model

$$\frac{I_F}{\beta_F} + \frac{qI_F}{kT} (\tau_F + R_C C_C \frac{dV_{B'E}}{dt'} + \frac{V_{out}}{R_{CH} + R_B} + C_C \frac{dV_{out}}{dt'}) = \frac{V_{CC} - V_{B'E}}{R_{CH} + R_B} \quad (3.16)$$

We assume that $V_{BE} = V_{BE(on)}$. Further, we differentiate (3.9) to obtain

$$\frac{qI_F}{kT} \frac{dV_{B'E}}{dt'} \simeq (C_{CS} + C_L) \frac{d^2 V_{out}}{(dt')^2} \quad (3.17)$$

We can now rewrite (3.16) as

$$\tau_F^* \frac{d^2 V_{out}}{(dt')^2} + \frac{1}{\beta_F^*} \frac{dV_{out}}{dt'} + \frac{V_{out}}{(R_{CH} + R_B)C_{CS} + C_L} = \frac{V_{CC} - V_{BE(on)}}{(R_{CH} + R_B)C_{CS} + C_L} \quad (3.18)$$

which is a second order differential equation in V_{out} . A solution to (3.18) is given by

$$V_{out}(t'') = C_1 \exp(m_1 t'') + C_2 \exp(m_2 t'') + V_{CC} - V_{BE(on)} \quad (3.19)$$

where C_1 and C_2 are constants and

$$m_1, m_2 = -\frac{1}{2\beta_F^* \tau_F^*} \pm \frac{1}{T_o} \sqrt{\left(\frac{T_o}{2\beta_F^* \tau_F^*}\right)^2 - 1} \quad (3.20)$$

T_o is of the form,

$$T_o = \sqrt{(R_{CH} + R_B)(C_{CS} + C_L)\tau^*}$$

T_o is generally much smaller than $2\beta^* \tau^*$ for commonly used device parameters. Therefore, roots m_1 and m_2 will be negative. Note that we have dropped the F subscript for the β and τ terms, since we know that the bipolar device is operating in the forward mode. Since the roots are negative, (3.19) will be of the form,

$$V_{out}(t'') = [C \sin(\frac{t''}{T}) + D \cos(\frac{t''}{T})] \exp(\frac{-t''}{2\beta^* \tau^*}) + V_{CC} - V_{BE(on)} \quad (3.21)$$

where C and D are constants and

$$T = \frac{T_o}{\sqrt{1 - (\frac{T_o}{2\beta^* \tau^*})^2}}$$

We now have to determine the constants C and D in (3.21). In the preceding analysis, we have seen that at $t = t_2$, the output voltage is given by

$$V_{out} = |V_T| - V_{BE(on)} \quad (3.22)$$

At $t = t_2$, $t'' = 0$. Plugging this into (3.21) we get

$$V_{out} = D + V_{CC} - V_{BE(on)} \quad (3.23)$$

Equating (3.22) and (3.23) we have for D :

$$D = -(V_{CC} - |V_T|)$$

Differentiating (3.21) we get

$$\frac{dV_{out}(t_2)}{dt''} = \frac{C}{T} - \frac{D}{2\beta^* \tau^*} \quad (3.24)$$

To get another expression involving C, we differentiate (3.13) with respect to t' and simplify to obtain :

$$\frac{dV_{out}(t_2)}{dt''} \simeq \frac{I_{dsat}(t_2 - t_1)}{C_{CS} + C_L \tau^*} \quad (3.25)$$

We now equate (3.24) and (3.25) and solve for C, after plugging in the expression for T. The final equation for C is

$$C = \frac{D}{\sqrt{1 - (T_o/2\beta^* \tau^*)^2}} \left[\frac{T_o}{2\beta^* \tau^*} - \sqrt{2 \left(\frac{R_{CH} + R_B}{R_{CH}} \right) \frac{|V_T| - V_{BE(on)}}{V_{CC} - |V_T|}} \right] \quad (3.26)$$

Terms inside the square brackets of (3.26) are typically $\ll 1$. So, the magnitude of C will be much smaller than that of D. Hence, we can neglect C in the expression for V_{out} which is now simplified to

$$V_{out}(t'') = (V_{CC} - |V_T|)[1 - \cos(\frac{-t''}{T}) \exp(-t''/2\beta^* \tau^*)] + |V_T| - V_{BE(on)} \quad (3.27)$$

Equation (3.27) represents the final V_{out} expression for Region 3. The time delay can be obtained by approximating the exponential term in (3.27) by unity and setting $V_{out} = (V_{CC} - V_{BE(on)})/2$ which is the 50% rise mark. The time delay can now be written as

$$t'' = t_3 - t_2 \simeq T \cos\left\{\frac{V_{CC} - V_{BE(on)}}{2(V_{CC} - |V_T|)}\right\} \simeq T \cos^{-1}(0.5) \simeq T \quad (3.28)$$

The total 50 % delay is obtained by summing up delays for each of the three regions. Hence,

$$t_{50} = t_1 + t' + t'' \quad (3.29)$$

This completes the Region 3 analysis. Expressions for the output voltage and total delay up to the 50% rise mark have been derived. In the next section the effect of bipolar device saturation on the delay will be discussed.

3.3.4 Collector Saturation

The previous discussions assumed that Q1 remains in the linear region throughout Region 3 operation. However, for moderate values of load capacitance and collector resistance, Q1 can operate in the collector saturation region. Under such conditions, the following equation may be written for the drop across the collector resistance :

$$I_C(t_{sat})R_C = V_{CC} - V_{CE(sat)} - V_{out}(t_{sat}) \quad (3.30)$$

where t_{sat} is the time in Region 3 when collector saturation occurs. Since $I_C \simeq I_E$ we can write

$$I_C \simeq (C_{CS} + C_C) \frac{dV_{out}}{dt} \quad (3.31)$$

Differentiating (3.27) and using the result in (3.31) we get

$$I_C(t'') = \frac{(C_{CS} + C_L)(V_{CC} - |V_T|)}{T} \sin\left(\frac{t''}{T}\right) \exp\left(-\frac{t''}{2\beta^* \tau^*}\right) \quad (3.32)$$

Substituting (3.32) and (3.27) into (3.30) gives

$$\frac{R_C(C_{CS} + C_L)}{T} \sin\left(\frac{t_{sat}}{T}\right) = \cos\left(\frac{t_{sat}}{T}\right) + \frac{V_{BE(on)} - V_{CE(sat)}}{V_{CC} - |V_T|} \exp\left(\frac{t_{sat}}{2\beta^* \tau^*}\right) \quad (3.33)$$

For typical device parameters, the exponential term on the right hand side of (3.33) is approximately 1 and its multiplier is $\ll 1$. Hence, we can neglect this term and arrive at the following expression for t_{sat} :

$$t_{sat} = T \tan^{-1} \left(\frac{T}{R_C(C_{CS} + C_L)} \right) \quad (3.34)$$

The expression for output voltage after saturation has occurred, can be obtained by replacing the denominator of the exponential term argument in (3.27) by $R_C(C_L + C_{CS})$ to indicate the dominance of the load capacitance and collector resistance in the response. t_{ps} represents the "post saturation" delay.

$$V_{out}(t_{ps}) = (V_{CC} - |V_T|) \left[1 - \cos \left(\frac{t_{sat}}{T} \right) \exp \left(\frac{-t_{ps}}{R_C(C_{CS} + C_L)} \right) \right] + |V_T| - V_{BE(on)} \quad (3.35)$$

The value of the output voltage at saturation is obtained by setting $t_{ps} = 0$ in (3.35)

$$V_{out}(t_{sat}) \simeq V_{CC} - V_{BE(on)} - \{V_{CC} - |V_T|\} \left[1 - \cos \left(\frac{t_{sat}}{T} \right) \right] \quad (3.36)$$

The effect of saturation on the gate delay can be accounted for by including t_{sat} in the delay calculations. Total delay at saturation is calculated by adding t_1 , t' and t_{sat} .

3.4 Results and Comparison with SPICE Simulations

The equations derived in the previous sections have been programmed and a composite curve for the output response has been plotted in Figure 3.12. This is to be compared with results obtained from SPICE simulations. PSPICE 3.04 running on a 80386 based IBM-PC has been determined to be quick and accurate enough for this study [1].

The MOS device dimensions used for this study are the same for N and P devices - a width of $30\mu m$ and length $2\mu m$. Unit sized bipolar transistors are used and the load capacitance value is 5pF. In the PSPICE simulations, the Shichman-Hodges model is used for the MOS devices while a simplified Gummel-Poon model is used for the NPN transistors [27]. A list of principal MOS and NPN device parameters used, is provided on the following pages. We are assuming that high level injection effects do not occur in the bipolar transistors since only moderate collector resistance values are assumed. For the PSPICE deck we set the knee current to its default value of infinity to ensure this.

Table 3.1. PMOS Device Parameters

Symbol	PSPICE keyword	Name	Value
V_T	VTO	Zero bias Threshold Voltage	-1V
ϕ_s	PHI	Surface Inversion Potential	0.659V
t_{ox}	TOX	Gate Oxide Thickness	0.04 μm
N_b	NSUB	Substrate Doping	2.45E15cm ⁻³
x_j	XJ	Metallurgical Junction Depth	0.5 μm
μ_o	UO	Surface Mobility	200cm ² /V.sec
R_D	RD	Drain Ohmic Resistance	300 ohms
R_S	RD	Source Ohmic Resistance	300 ohms
ϕ_j	PB	Bulk Junction Potential	0.89V
C_{BGO}	CGBO	Gate-bulk Overlap Capacitance/meter	9.9E-09F
C_{DGO}	CDBO	Gate-drain Overlap Capacitance/meter	4.93E-10F
C_{SGO}	CDBO	Gate-source Overlap Capacitance/meter	4.93E-10F
v_{max}	VMAX	Max. Drift Velocity of Carriers	10000m/sec

Table 3.2. NPN Device Parameters

Symbol	PSPICE keyword	Name	Value
I_s	IS	Saturation Current	3E-16A
β_F	BF	Ideal Max. Forward Current Gain	120
r_b	RB	Base Resistance	100 ohms
r_c	RC	Collector Resistance	50 ohms
r_e	RE	Emitter Resistance	10 ohms
C_c	CJC	Collector Junction Capacitance	1E-13F
C_e	CJE	Emitter Junction Capacitance	1E-13F
C_{cs}	CJC	Collector to Substrate Capacitance	2-13F
τ_F	TF	Ideal Forward Transit Time	20ps
ϕ_E	VJE	Base Emitter Built in Potential	0.7V
ϕ_C	VJC	Base Collector Built in Potential	0.75V

We are now in a position to analyze the curves in Figure 3.7. It is clear that both the analytical results and SPICE results show good agreement up to a mark near the 3.5V level. Since our primary objective in this analysis is to obtain an expression for the delay between the 50 percent rise marks, we conclude that the analytical approach provides a fairly accurate indication of the delay. Beyond the 3.5V mark the analytical

curve approaches the 4.3V mark asymptotically while the SPICE curve continues on before doing the same, close to the 4.85V mark. The reason for this difference can be explained as follows :

Throughout the analytical modeling process, we have assumed that the base-emitter drop of the bipolar transistor remains constant i.e. at $V_{BE(on)}$ taken as 0.7V. In actual practice, this drop is not constant and is related to the collector current by the following expression :

$$I_C = I_s \left(\exp\left(\frac{qV_{BE}}{kT}\right) \right)$$

Therefore, as the collector current becomes smaller, the base-emitter drop is also reduced. At the end of the collector saturation region the collector current is very small and hence, V_{BE} is also greatly reduced from 0.7V. The expression that SPICE uses to relate I_C to V_{BE} is very complex and has to be computed iteratively. Our objective with the analytical approach is to arrive at the simplest possible closed form expression which can provide a reasonable first approximation for the delay. As mentioned before, the equations derived are able to do this. In addition, it must be noted that the times at which both curves approach their final values are similar, so the overall rise times for both will be quite close to one another in value. We conclude therefore, that the equations for delay calculations can definitely be used for first approximations, while keeping in mind the actual voltage levels achieved.

Theoretically, one way to improve the predicted voltage levels by taking into account the V_{BE} variation would be to factor results of experimental or simulated data into the analytical equations. Appendix A details how this would constrain the simplicity and closed form nature of these equations.

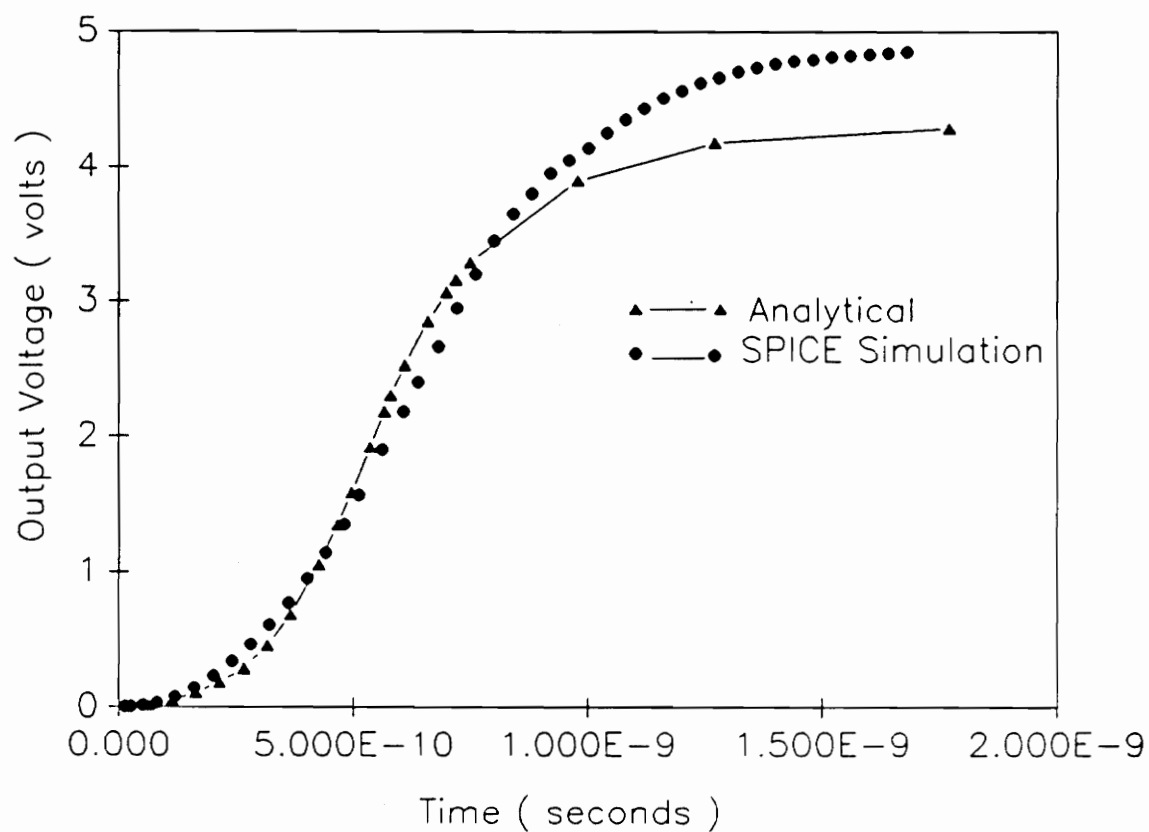


Figure 3.7. Comparison of Analytical and SPICE results for Rise Analysis

Having completed the inverter output rise analysis, we now undertake a similar approach towards the output fall analysis. It must be noted that the fall analysis is equally important, because it allows us to gauge the total delay through the gate.

3.5 Output Fall Characteristic Analysis

In this section the high to low output transient will be analyzed. We assume that the output is already at logic '1' and a sharp positive transition occurs at the input. The devices that are responsible for this operation are shown in Figure 3.8. When V_{in} goes high, NMOS device M1 is turned on and it begins to source current to the Q2 base. Q2 turns on after the base-emitter threshold voltage is reached and speeds up discharge of the load capacitance. The final output voltage is one diode drop above ground. Just as in the rise analysis, we can divide this operation into three regions in time. Initially, M1 is in saturation and Q1 is off. At time t_1 , Q1 turns on. M1 remains in saturation until time t_2 after which it moves into the linear region while Q1 remains on. We consider a third region bounded by the time at which the downward output transition crosses the $V_{high}/2$ mark, considered to be the approximate switching point. The three regions characterizing this transient are shown in Figure 3.9. We shall now undertake a detailed analysis of these regions of operation.

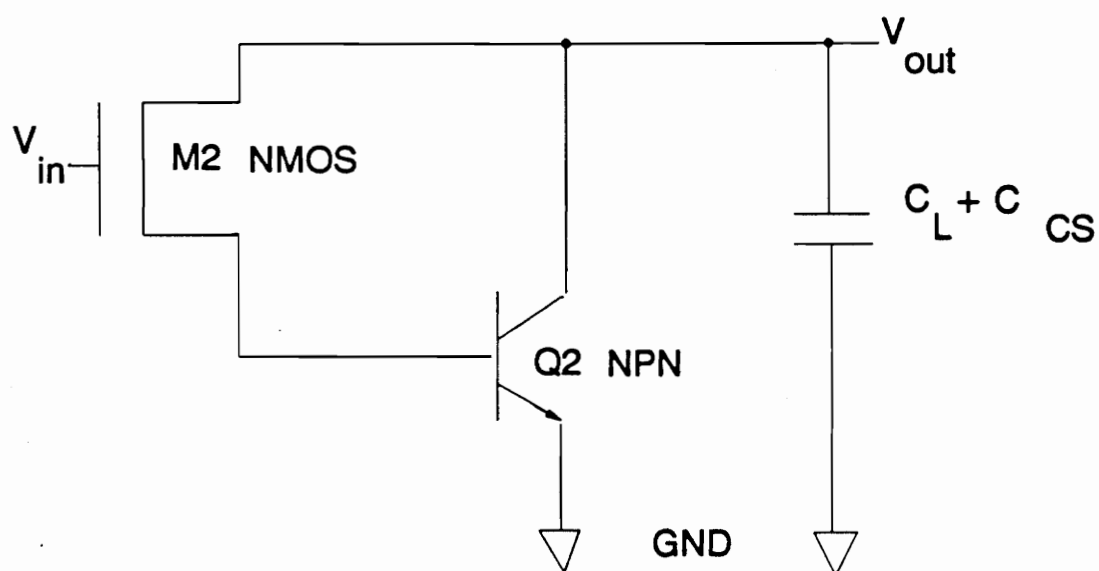


Figure 3.8. Output Discharge Circuit

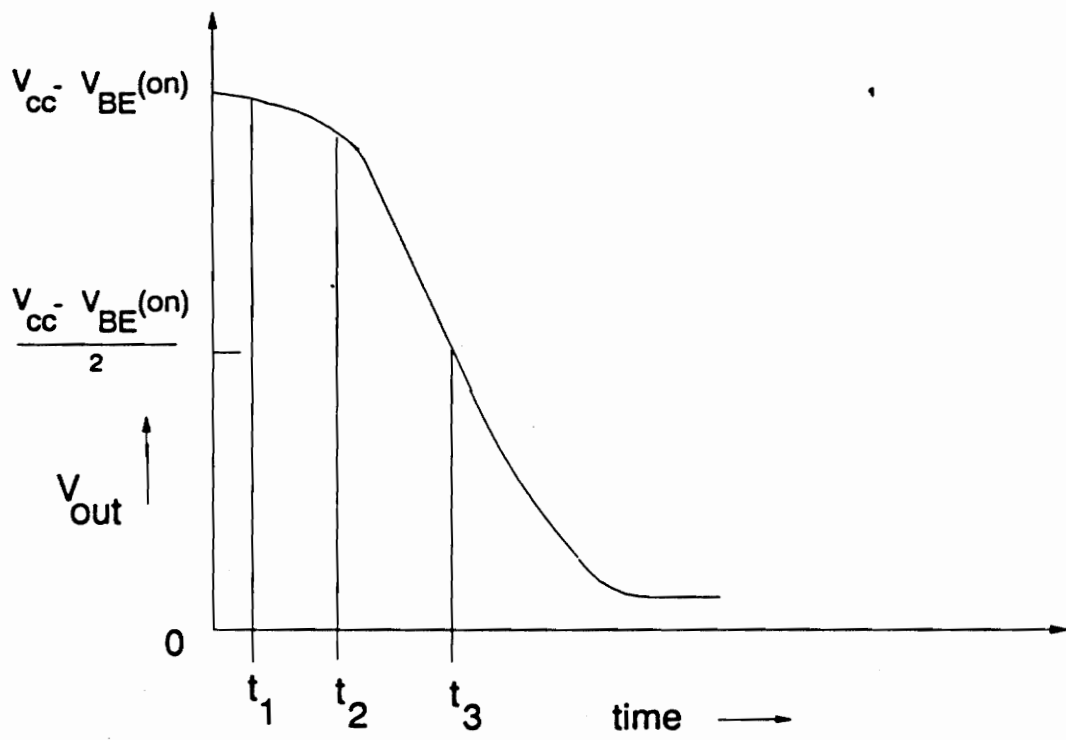


Figure 3.9. Inverter Regions of Operation for Falling Output

3.5.1 Region 1

In this region M1 is in saturation and Q1 is off. The circuit model is shown in Figure 3.10a. Since the load is being discharged only by the MOS device, we can write :

$$C_{out} \frac{dV_{out}}{dt} \simeq -I_{dsat} \quad (3.37)$$

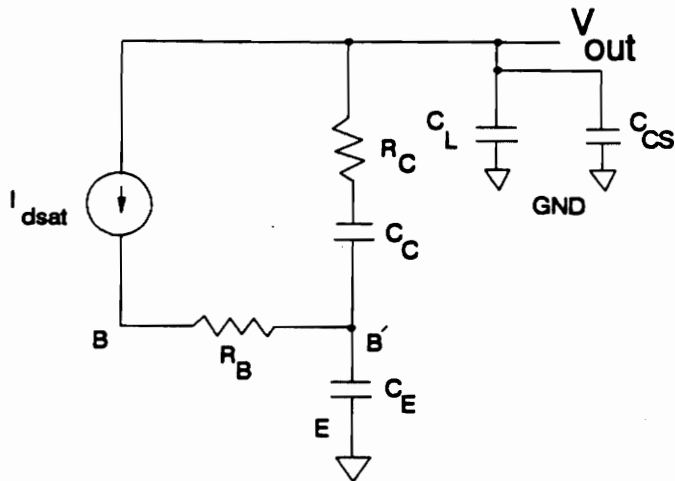
where C_{out} is the composite load capacitance comprising of the external load plus the collector to substrate capacitance. Integrating (3.36) we get

$$V_{out} \simeq -\frac{I_{dsat}}{C_{out}} t + K \quad (3.38)$$

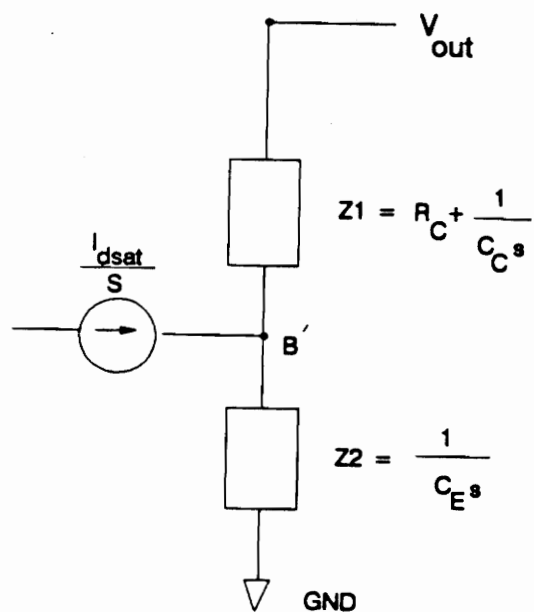
where K is a constant which may be determined by noting that at $t=0$ the output voltage is $V_{CC} - V_{BE(on)}$. The final expression for V_{out} is

$$V_{out} \simeq -\frac{I_{dsat}}{C_{out}} t + V_{CC} - V_{BE(on)} \quad (3.39)$$

To calculate the delay we have to derive an expression for the voltage at B' since we know that the boundary of Region 1 is determined by the time at which the voltage at B' is $V_{BE(on)}$. Essentially, the expression is derived in Appendix A. The simplified circuit in terms of s-domain impedances used for this analysis appears in Figure 3.10b. The expression for $V_{B'}$ is



Circuit model for Region 1



Simplified model in s-domain

Figure 3.10. Region 1 circuit model and s-domain representation

$$V_{B'}(t) = \frac{I_{dsat}t}{C_E + C_C} + I_{dsat}R_C \left(\frac{C_C}{C_E + C_C} \right)^2 [1 - \exp(-\frac{t}{\tau})] \quad (3.40)$$

In 3.40, the drain current is given by

$$I_{dsat} = \frac{W\mu\epsilon}{2t_{ox}L} (V_{cc} - |V_T|)^2 \quad (3.41)$$

τ has already been defined in (3.3). The time t_1 at which Q2 turns on is obtained by solving (3.40) for t , with $V_{B'}(t) = V_{BE(on)}$:

$$t_1 = (C_E + C_C) \frac{V_{BE(on)}}{I_{dsat}} - \frac{R_C C_C^2}{C_E + C_C} \quad (3.42)$$

This completes the Region 1 analysis. The total delay up to this point is t_1 . We now perform the analysis for Region 2.

3.5.2 Region 2

M2 operates in saturation while Q2 is "on" in this region. The complete circuit model is shown in Figure 3.11. We are assuming a constant base-emitter voltage so we neglect the emitter capacitance. From Figure 3.10 we can write the following current equation :

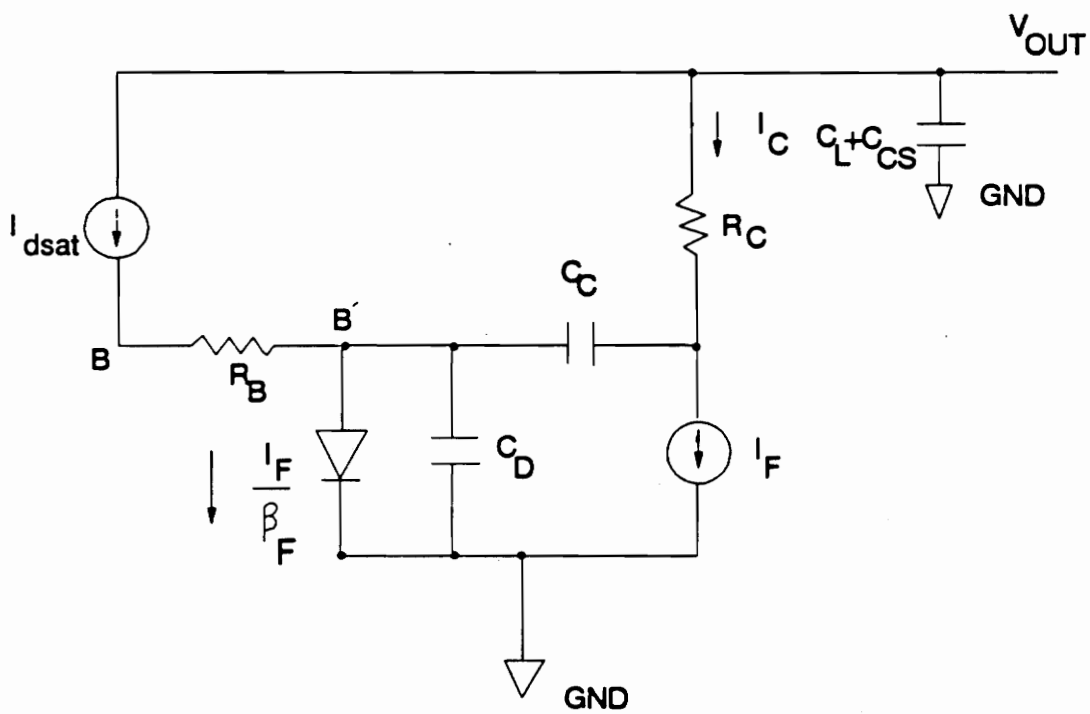


Figure 3.11. Region 2 circuit model

$$C_{out} \frac{dV_{out}}{dt'} \simeq -(I_{dsat} + I_C) \quad (3.43)$$

where t' is the time elapsed since the end of Region 1. The following relation for the drain current can be written :

$$I_{dsat} = \frac{I_F}{\beta_F} + C_D \frac{dV_{B'E}}{dt'} + C_C \frac{d}{dt'} (V_{B'E} + I_C R_C - V_{out}) \quad (3.44)$$

The $V_{B'E}$ term in the expression within parentheses can be neglected since we are assuming a constant base-emitter drop. Also we may safely assume that $I_C \simeq I_F$ following the path of near zero impedance.

The following relations for terms in the above equation are reproduced for the sake of continuity :

$$I_F = I_s \exp\left(\frac{qV_{B'E}}{kT}\right) \quad (3.6)$$

$$\frac{dI_F}{dt'} = I_F \frac{q}{kT} \frac{dV_{B'E}}{dt'}$$

$$C_D = \frac{q}{kT} \tau_F I_F \quad (3.8)$$

Using these equations, the expression in (3.44) can be simplified in the following manner,

$$I_{dsat} = \frac{I_F}{\beta_F} + (\tau + R_C C_C) \frac{q}{kT} \frac{dV_{B'E}}{dt'} I_F - C_C \frac{dV_{out}}{dt'} \quad (3.45)$$

$$= \frac{I_F}{\beta_F} + (\tau + R_C C_C) \frac{dI_F}{dt'} - C_C \frac{dV_{out}}{dt'}$$

$$= \frac{I_F}{\beta_F} + \tau^* \frac{dI_F}{dt'} - C_C \frac{dV_{out}}{dt'} \quad (3.46)$$

Using (3.43) we can rewrite (3.46) as

$$I_{dsat} = \frac{I_F}{\beta_F} + \tau^* \frac{dI_F}{dt'} + \frac{C_C}{C_{out}} (I_{dsat} + I_C) \quad (3.47)$$

Since $I_C \simeq I_F$, we can write :

$$\left(\frac{C_{out} - C_C}{C_{out}} \right) I_{dsat} = \frac{I_F}{\beta^*} + \tau^* \frac{dI_F}{dt'} \quad (3.48)$$

where

$$\frac{1}{\beta^*} = \frac{1}{\beta_F} + \frac{C_C}{C_{out}}$$

and

$$\tau^* = \tau + R_C C_C$$

(3.48) is a differential equation with the following solution :

$$I_F(t') = \beta^* \left(\frac{C_{out} - C_C}{C_{out}} \right) I_{dsat} \left[1 - \exp\left(\frac{-t'}{\beta^* \tau^*} \right) \right] \quad (3.49)$$

From (3.43) and since $I_C \simeq I_F$, (3.49) can be written as

$$\frac{dV_{out}}{dt'} = -\frac{I_{dsat}}{C_{out}} \left[1 + \beta^* \frac{(C_{out} - C_C)}{C_{out}} \left(1 - \exp\left(\frac{-t'}{\beta^* \tau^*} \right) \right) \right] \quad (3.50)$$

An expression for V_{out} can be derived by integrating (3.50) with respect to time. For $t' = 0$, $t = t_1$, which can be calculated from (3.42), and then (3.39) can be used to calculate V_{out} at this point in time.

On integrating (3.50) we get

$$V_{out}(t') = -\frac{I_{dsat}}{C_{out}} \left[t' + \beta^* \frac{(C_{out} - C_C)}{C_{out}} (t' + \beta^* \tau^* \exp(\frac{-t'}{\beta^* \tau^*})) \right] + K \quad (3.51)$$

K is a constant which can be calculated by plugging the value of V_{out} calculated from (3.39) into (3.51), keeping t' zero. We assume for the sake of brevity that K is equal to fV_{CC} , where f is a number between 0 and 1. The final expression for V_{out} in Region 2 is

$$V_{out}(t') = -\frac{I_{dsat}}{C_{out}} \left[t' + \beta^* \frac{(C_{out} - C_C)}{C_{out}} (t' + \beta^* \tau^* \exp(\frac{-t'}{\beta^* \tau^*})) \right] + fV_{CC} \quad (3.52)$$

The drain current is given by

$$I_{dsat} = \frac{W\mu_E}{2t_{ox}L} (V_{cc} - |V_T| - V_{BE(on)})^2$$

This region is bounded by the time at which M1 comes out of saturation, i.e. when

$$V_{out} = fV_{CC} - V_T + V_{BE(on)} \quad (3.53)$$

We substitute the above value of V_{out} in (3.52) and expand the exponential term in (3.52) in a Taylor's series. After retaining terms up to the second degree and simplifying, we get a quadratic equation in t' . This may be solved to yield the following expression :

$$t' = t_2 - t_1 = \frac{-1 + \sqrt{1 - \frac{4 C_{out}}{I_{dsat}\tau} (V_{BE(on)} - |V_T|)}}{2/\tau} \quad (3.54)$$

This is an expression for the delay in Region 2. The total delay at the end of this region is obtained by summing the delays predicted by (3.42) and (3.54). Next, the analysis for Region 3 is performed.

3.5.3 Region 3

M2 moves into the linear mode while Q2 stays "on" in this region. The complete circuit model is shown in Figure 3.12. We can write the following expression for the current flowing into the base of Q2 :

$$I_B = \frac{V_{out} - V_{B'E}}{R_{CH} + R_B} \quad (3.55)$$

$$= \frac{I_F}{\beta_F} + C_D \frac{dV_{B'E}}{dt'} + C_C \frac{d}{dt'} (V_{B'E} + I_C R_C - V_{out})$$

where $t' = t - t_2$ and other terms are as per earlier definitions. Once again, since we are assuming a constant base-emitter drop, the differential of the $V_{B'E}$ term in parentheses is negligible relative to that of V_{out} . Also, we substitute for C_D from (3.8) to get

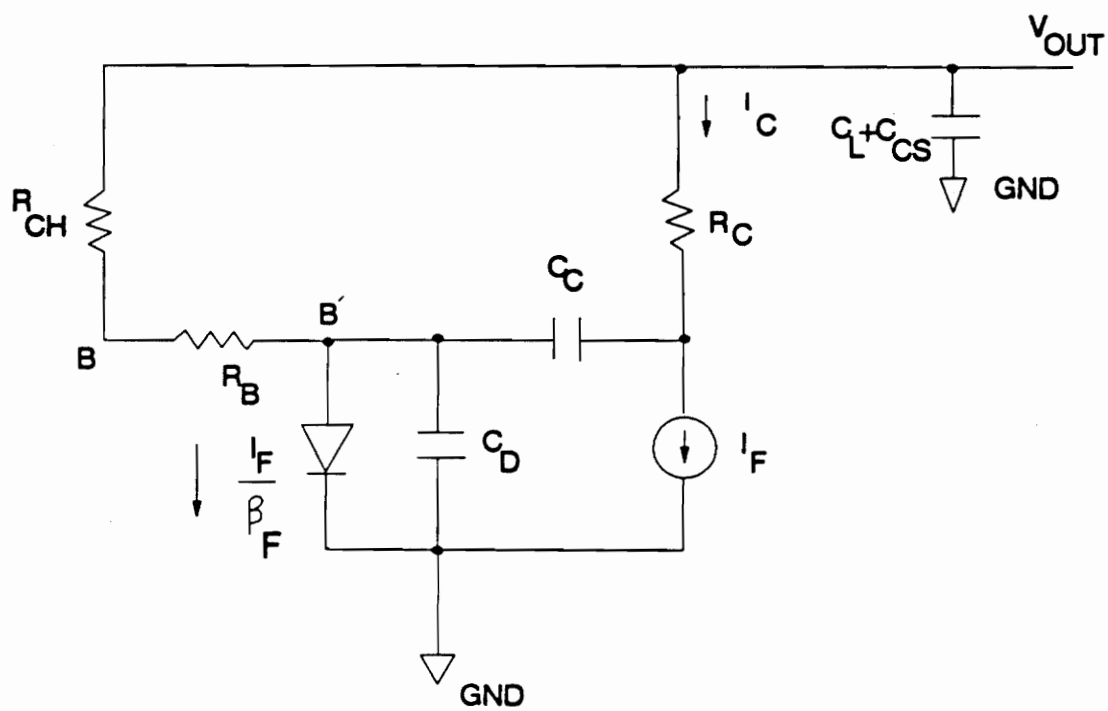


Figure 3.12. Region 3 circuit model

$$I_B = \frac{I_F}{\beta_F} + (\tau + R_C C_C) \frac{q}{kT} \frac{dV_{B'E}}{dt''} I_F - C_C \frac{dV_{out}}{dt''} \quad (3.56)$$

Now,

$$I_B + I_C \approx C_{out} \frac{dV_{out}}{dt''}$$

i.e.

$$\frac{V_{out} - V_{B'}}{R_{CH} + R_B} + I_F \approx -C_{out} \frac{dV_{out}}{dt''} \quad (3.57)$$

since $I_F \approx I_C$. Differentiating (3.57) with respect to t'' we have

$$\frac{q}{kT} I_F \frac{dV_{B'E}}{dt''} \approx -\left(C_{out} \frac{d^2 V_{out}}{dt''^2}\right) - \frac{1}{(R_{CH} + R_B)} \frac{dV_{out}}{dt''} \quad (3.58)$$

Substituting for the expression on the left hand side of (3.58) in (3.56) and simplifying we get

$$\tau^* \frac{d^2 V_{out}}{dt''^2} + \frac{1}{\beta^*} \frac{dV_{out}}{dt''} + \frac{V_{out}}{(R_{CH} + R_B)C_{out}} = \frac{V_{BE(on)}}{(R_{CH} + R_B)C_{out}} \quad (3.59)$$

where

$$\tau^* = \tau_F + R_C C_C$$

$$\frac{1}{\beta^*} = \left[\frac{C_C}{C_{out}} + \frac{1}{\beta_F} + \frac{\tau^*}{C_{out}(R_{CH} + R_B)} \right]$$

(3.59) is a second order differential equation in V_{out} . Its solution is of the form,

$$V_{out}(t'') = C_1 \exp(m_1 t'') + C_2 \exp(m_2 t'') + V_{BE(on)} \quad (3.60)$$

where C_1 and C_2 are constants and

$$m_1, m_2 = -\frac{1}{2\beta^* \tau^*} \pm \frac{1}{T_o} \sqrt{\left(\frac{T_o}{2\beta^* \tau^*}\right)^2 - 1} \quad (3.61)$$

where

$$T_o = \sqrt{(R_{CH} + R_B)(C_{CS} + C_L)\tau^*}$$

For standard device parameters, m_1 and m_2 will be negative so the expression for V_{out} will be of the form,

$$V_{out}(t'') = [C \sin(\frac{t''}{T}) + D \cos(\frac{t''}{T})] \exp(\frac{-t''}{2\beta^* \tau^*}) + V_{BE(on)} \quad (3.62)$$

where C and D are constants and

$$T = \frac{T_o}{\sqrt{1 - (\frac{T_o}{2\beta^* \tau^*})^2}}$$

To determine values of C and D we perform the following steps. From (3.62) we know that at $t'' = 0$,

$$V_{out} = D + V_{BE(on)} \quad (3.63)$$

From the Region 2 analysis we know that at $t = t_2$,

$$V_{out} = fV_{CC} - |V_T| + V_{BE(on)} \quad (3.64)$$

Equating (3.63) and (3.64) we have

$$D = fV_{CC} - |V_T|$$

Now, by differentiating (3.62) and setting $t'' = 0$ we get

$$\frac{dV_{out}}{dt''}(t''=0) = \frac{C}{T} - \frac{D}{2\beta^* \tau^*} \quad (3.65)$$

Further, we also differentiate (3.52) with respect to t' and simplify to obtain

$$\frac{dV_{out}}{dt'}(t') = -\frac{I_{dsat}}{C_{out}} \left[1 + \frac{t'}{\tau^*} \right]$$

Now, at $t = t_2$, t' is given by (3.54) so we can write

$$\frac{dV_{out}}{dt'}(t') = -\frac{I_{dsat}}{C_{out}} \left[1 + \frac{-1 + \sqrt{1 - \frac{4 C_{out}}{I_{dsat} \tau^*} (V_{BE(on)} - |V_T|)}}{2} \right] \quad (3.66)$$

Equating (3.65) and (3.66) we get

$$C = T \left\{ \frac{D}{2\beta^* \tau^*} - \frac{I_{dsat}}{C_{out}} \left[1 + \frac{-1 + \sqrt{1 - \frac{4 C_{out}}{I_{dsat} \tau^*} (V_{BE(on)} - |V_T|)}}{2} \right] \right\} \quad (3.67)$$

For typical device parameters we find from (3.67) that $C \ll D$. Hence, (3.62) can be simplified to

$$V_{out}(t'') = D \cos\left(\frac{t''}{T}\right) \exp\left(\frac{-t''}{2\beta^* \tau^*}\right) + V_{BE(on)} \quad (3.68)$$

Region 3 is bounded by the time at which the output voltage crosses the $\frac{V_{CC} - V_{BE(on)}}{2}$ mark. t'' may be estimated by setting V_{out} to this value in (3.68) and approximating the exponential term by unity :

$$t'' = t_3 - t_2 \simeq T \cos^{-1} \left(\frac{\frac{V_{CC} - V_{BE(on)}}{2} - V_{BE(on)}}{fV_{CC} - |V_T|} \right) \simeq T \quad (3.69)$$

This completes the Region 3 analysis. The total delay until the 50 percent rise point is given by

$$t_{50} = t_1 + t' + t''$$

3.5.4 Collector Saturation

The effects of the load capacitance and collector resistance are manifested in the onset of collector saturation in the device. The following relation may be written for the voltage drop across the collector resistance :

$$I_C(t_{sat})R_C = V_{out} - V_{CE(sat)} \quad (3.70)$$

From Figure 3.11 I_C can be shown to be

$$I_C = -(C_{out} \frac{dV_{out}}{dt} + I_B) \quad (3.71)$$

Differentiating (3.68) and neglecting the smaller terms we have

$$\frac{dV_{out}}{dt} = \frac{D}{T} \sin(\frac{t''}{T}) \exp(\frac{-t''}{2\beta^* \tau^*}) \quad (3.72)$$

Again, from the circuit model, the base current can be written as

$$I_B = \frac{V_{out} - V_{BE(on)}}{R_{CH} + R_B} \quad (3.73)$$

From (3.70) through (3.73) we are able to write the following :

$$\begin{aligned} I_C &= C_{out} \frac{D}{T} \sin(\frac{t''}{T}) \exp(\frac{-t''}{2\beta^* \tau^*}) - \frac{D}{R_{CH} + R_B} \cos(\frac{t''}{T}) \exp(\frac{-t''}{2\beta^* \tau^*}) \\ &= \frac{1}{R_C} [D \cos(\frac{t''}{T}) \exp(\frac{-t''}{2\beta^* \tau^*}) + \frac{V_{BE(on)}}{R_{CH} + R_B} - V_{CE(sat)}] \end{aligned} \quad (3.74)$$

We simplify (3.74) by neglecting the second terms of each of its constituent expressions as being small relative to the first terms. After further simplification we have the following expression for the time at which saturation occurs :

$$t_{sat} \simeq T \tan^{-1} \left(\frac{T}{C_{out} R_C} \right) \quad (3.75)$$

The expression for the output voltage is derived by using (3.68) as the basis and making appropriate changes to the arguments of the exponential and cosine term arguments to reflect the onset of saturation and the dominance of R_C and C_{out} in the post saturation response.

$$V_{out}(t_{ps}) = (V_{CC} - |V_T|) \left[1 - \cos \left(\frac{t_{sat}}{T} \right) \exp \left(-\frac{t_{ps}}{R_C C_{out}} \right) \right] + V_{BE(on)} \quad (3.76)$$

where t_{ps} denotes the delay after saturation is reached.

The output voltage at saturation can be calculated from (3.76) by setting $t_{ps} = 0$:

$$V_{out}(t_{sat}) = D \cos \left(\frac{t_{sat}}{T} \right) + V_{BE(on)} \quad (3.77)$$

The total delay until the onset of saturation can be calculated by adding t_1 , t' and t_{sat} .

3.6 Results and Comparison with SPICE Simulations

The equations derived for the output fall response have been programmed and a comparison with the SPICE response can be made from the curves in Figure 3.13. We continue with the same MOS device dimensions i.e. $30\mu m$ for the width and $2\mu m$ for the length. Before we analyze the results in Figure 3.13, a list of MOS and BJT parameters used in the simulations is provided on the following pages. Once again, we are assuming the Shichman-Hodges model for the MOSFETs and a simplified Gummel-Poon Model for the BJTs. High level effects for the bipolar transistors are not considered since moderate collector resistance values are assumed.

Table 3.3. NMOS Device Parameters

Symbol	PSPICE keyword	Name	Value
V_T	VTO	Zero bias Threshold Voltage	1V
ϕ_s	PHI	Surface Inversion Potential	0.659V
t_{ox}	TOX	Gate Oxide Thickness	0.04 μ m
N_b	NSUB	Substrate Doping	2.74259 cm^{-3}
x_j	XJ	Metallurgical Junction Depth	0.5 μ m
μ_o	UO	Surface Mobility	400 $cm^2/V.sec$
R_D	RD	Drain Ohmic Resistance	300 ohms
R_S	RD	Source Ohmic Resistance	300 ohms
ϕ_j	PB	Bulk Junction Potential	0.89V
C_{BGO}	CGBO	Gate-bulk Overlap Capacitance/meter	9.9E-09F
C_{DGO}	CDBO	Gate-drain Overlap Capacitance/meter	4.93E-10F
C_{SGO}	CDBO	Gate-source Overlap Capacitance/meter	4.93E-10F
v_{max}	VMAX	Max. Drift Velocity of Carriers	80500m/sec

Table 3.4. NPN Device Parameters

Symbol	PSPICE keyword	Name	Value
I_s	IS	Saturation Current	3E-16A
β_F	BF	Ideal Max. Forward Current Gain	120
r_b	RB	Base Resistance	100 ohms
r_c	RC	Collector Resistance	50 ohms
r_e	RE	Emitter Resistance	10 ohms
C_c	CJC	Collector Junction Capacitance	1E-13F
C_e	CJE	Emitter Junction Capacitance	1E-13F
C_{cs}	CJC	Collector to Substrate Capacitance	2-13F
τ_F	TF	Ideal Forward Transit Time	20ps
ϕ_E	VJE	Base Emitter Built in Potential	0.7V
ϕ_C	VJC	Base Collector Built in Potential	0.75V

An analysis of the curves in Figure 3.13 can now be made. We have assumed that for both approaches, the initial voltage is $V_{CC} - V_{BE}$ (on), taken as 4.3V. Figure 3.13 indicates that the agreement between the analytical and SPICE curves is fairly good up to a mark close to the 1V level. Beyond this, there is a gap between the two for the same reasons as in the rise analysis i.e. the effect of a non constant base-emitter drop. Clearly, the analytical equations provide an accurate indication for the gate delay. We can

therefore use them in conjunction with the rise delay equations to predict the total gate delay.

3.7 *Summary*

In this chapter, the basic BiCMOS inverting buffer driver has been modeled analytically. The principal aim has been to arrive at a set of equations that provide an accurate measure of the delays in this circuit. Both rise and fall output transients have been analyzed in detail and operation of the devices is explained at length. In both the analyses the MOS devices have been shown to be operating in the saturation and linear regions while the bipolar devices operate in cut off and active regions. The possibility that the bipolar devices will enter the region of collector saturation for moderately high values of collector resistance and capacitance as well as the load capacitance, has been discussed and elaborated upon. Under such conditions, the output response becomes heavily dependent on the collector resistance and load capacitance values. The actual effect of collector saturation on the output waveform has been shown - the waveform approaches its final value asymptotically for both the rise and fall transients.

The expressions for the output voltage and time delays in each of the regions are fairly simple and closed form in nature. Comparisons with results of PSPICE simulations have indicated good agreement for a major part of the waveform. Reasons for deviations at the end points of the voltage swings have been accounted for and justified in the light of preserving the simplicity and closed form nature of the analytical approach. The most useful end product of the analysis is the set of delay equations which allow us to make

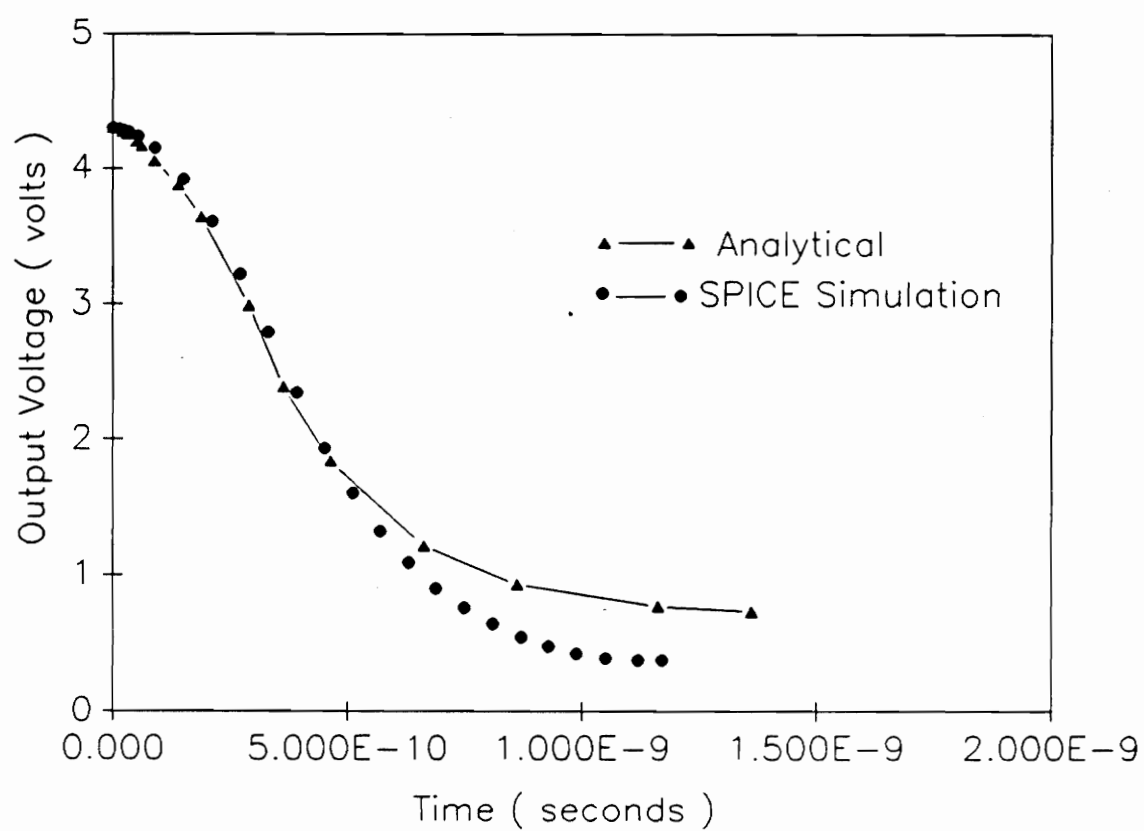


Figure 3.13. Comparison of Analytical and SPICE results for Fall Analysis

a first approximation of the total gate delay through the inverting buffer. These are measured at 50 percent of the total voltage swing and are in good agreement with the delays predicted by SPICE. The delay equations also provide information on which circuit, MOS and bipolar parameters need to be optimized to minimize the gate delay. With this knowledge, detailed simulations can be used to further fine tune the optimization process. To sum up, the analytical approach affords us valuable insights into the working of the BiCMOS inverting buffer - these could be a useful tool towards achieving better circuit and device performance.

Chapter 4

BiCMOS Performance Evaluation

4.1 *Introduction*

In the previous chapter the basic BiCMOS inverting buffer has been analyzed in detail and theoretical equations allowing time delay estimates in circuits using these devices, have been derived. Thus, an evaluation of more complex inverter configurations is possible. There are two schemes that afford improved performance in comparison to the basic buffer. These configurations are illustrated in Figures 4.1 and 4.2 [28].

The Z-type BiCMOS inverter shown in Figure 4.1 gets its name from the two resistors which are present in addition to the four active devices in the simple inverting buffer. This circuit functions in the following manner. When the load capacitance is being charged, we have seen that the output is constrained from reaching V_{CC} by the drop across the base-emitter junction of Q1. In the Z-type inverter, Z1 continues to supply current to the load after the active devices have been turned off, until the output

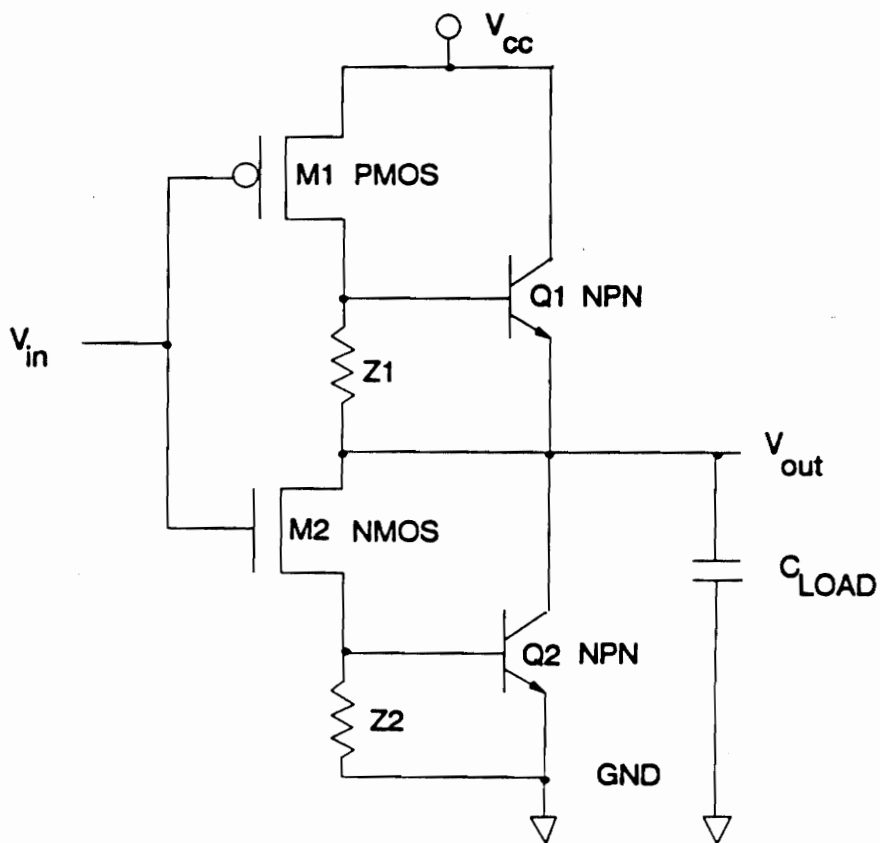


Figure 4.1. Z-type BiCMOS Inverter

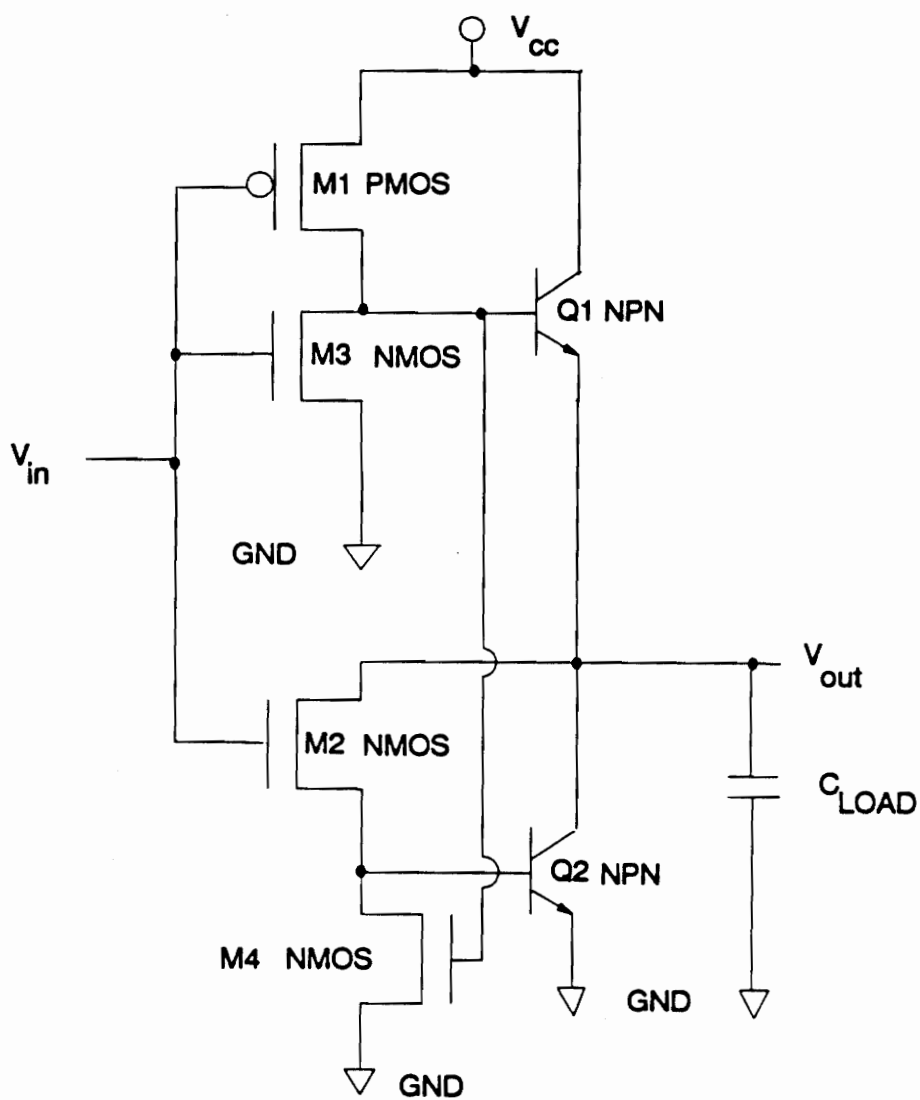


Figure 4.2. BiCMOS Inverter with Active Devices

voltage reaches V_{cc} . When the output voltage makes a downward transition, both Z1 and Z2 continue to discharge the Q1 base and the load capacitance after Q2 is turned off. Hence, this configuration provides a complete rail to rail logic swing between ground and V_{cc} . An alternative to the Z-type inverter is shown in Figure 4.2. This scheme utilizes only active devices. NMOSFETs M3 and M4 provide a discharge path to turn off the bipolar devices. This inverting buffer does not possess a zero to V_{cc} voltage swing. Further comments on the merits of the two schemes will be made later.

For the Z-type inverter, the values of Z1 and Z2 depend on circuit and device parameters. Optimal Z values have to be determined through a process of simulations. In this study, a Z value of 5 K Ω has been found to be suitable. In actual implementations, the resistors may be implemented with active devices. In the following sections, we discuss the results of simulations performed to determine the effects of circuit, device and process parameter variations, on the performance of CMOS and BiCMOS inverters. These results give us a good idea about the advantages offered by BiCMOS and the design tradeoffs involved while choosing between the two technologies. Before we proceed to the actual discussion it would be instructive to pause and define some of the performance measures that are to be used.

4.2 *Some Definitions*

The principal performance measure that we shall use in the following discussions is the ability of a gate to drive loads quickly. This capability is reflected in the peak output current achievable and the resultant gate delay. The current characteristic is a good

indicator of drive capability while the gate delay is, of course, one of the main design specifications in any VLSI circuit.

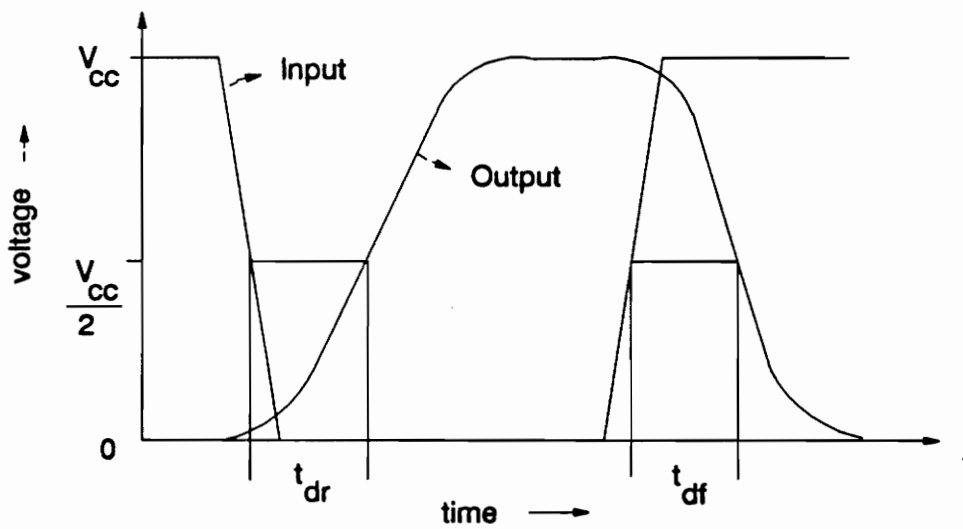
The term "gate delay" must take into account delays occurring during both rise and fall transients. Figure 4.3a represents a typical situation. In the figure, t_{dr} is the rise time delay and t_{df} represents the fall time delay. Measurements are made at the midpoint of the voltage swing, which is assumed to be the switching point. Since NMOS devices are faster than their PMOS counterparts, these delays in CMOS and BiCMOS inverter circuits will be unequal. Hence, we take the average of the two delays to balance out the differences.

$$\text{Gate Delay} = \frac{t_{dr} + t_{df}}{2}$$

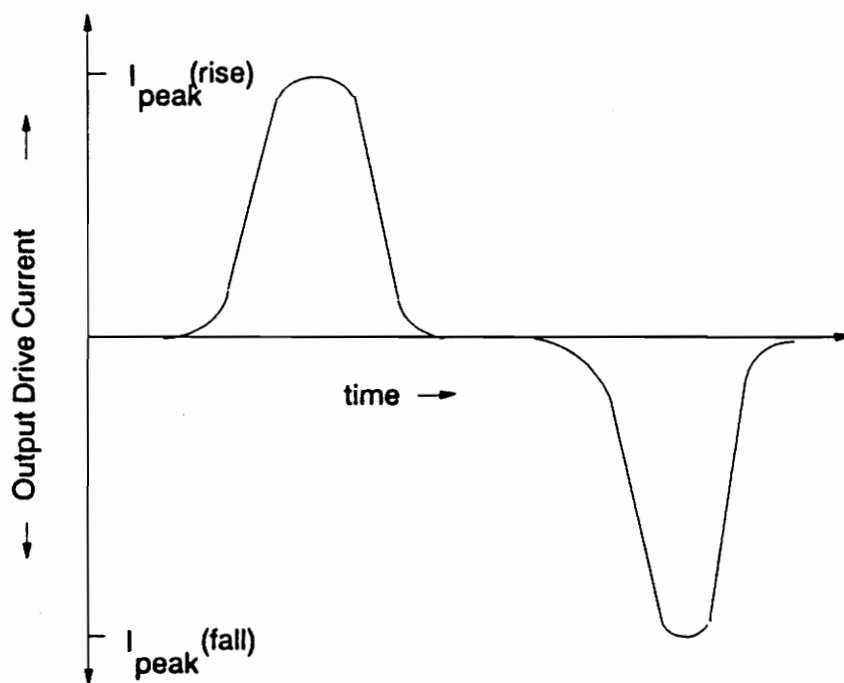
The peak output current also occurs at the switching point, as Figure 4.3b shows, in the positive direction for the output rise transient and in the negative direction or the fall transient. Again, the two values may be unequal so we take the average.

$$\text{Peak Output Drive Current} = \frac{I_{peak(rise)} + I_{peak(fall)}}{2}$$

Having defined the two terms, we can now proceed to the analysis of the simulation results. The device parameters used in these simulations are essentially the same as those listed in Chapter 3. Device dimensions and load capacitance values have been mentioned in several graph legends. Where not listed, C_L of 1pF may be assumed while MOS device



4.3a Gate Delay



4.3b Peak Output Current

Figure 4.3. Definition of Gate Delay and Peak Output Drive Current

sizes are $60\mu\text{m} \times 2\mu\text{m}$ for CMOS and $30\mu\text{m} \times 2\mu\text{m}$ for BiCMOS. For additional active devices, minimum sized transistors are used.

4.3 Effect of External Circuit Parameters and Operating Conditions

4.3.1 Fanout

A very important performance measure in integrated circuits is the number of gates a single gate can drive without a significant loss in speed of operation. This is referred to as "fanout". In this study, fairly small load gates with gate capacitances of 25 femtofarads are assumed. Figure 4.4 indicates how gate delay varies with fanout for CMOS and BiCMOS. CMOS is competitive for a fanout of 2 or less. Beyond this, its performance falls off progressively despite larger MOS device sizes compared to BiCMOS. On the other hand, the BiCMOS gate maintains a fairly steady gate delay across a wide fanout range, clearly demonstrating its superior drive capability. Therefore, an obvious design rule in this case would be to use CMOS for low fanout loads. At higher loads, BiCMOS becomes an attractive choice.

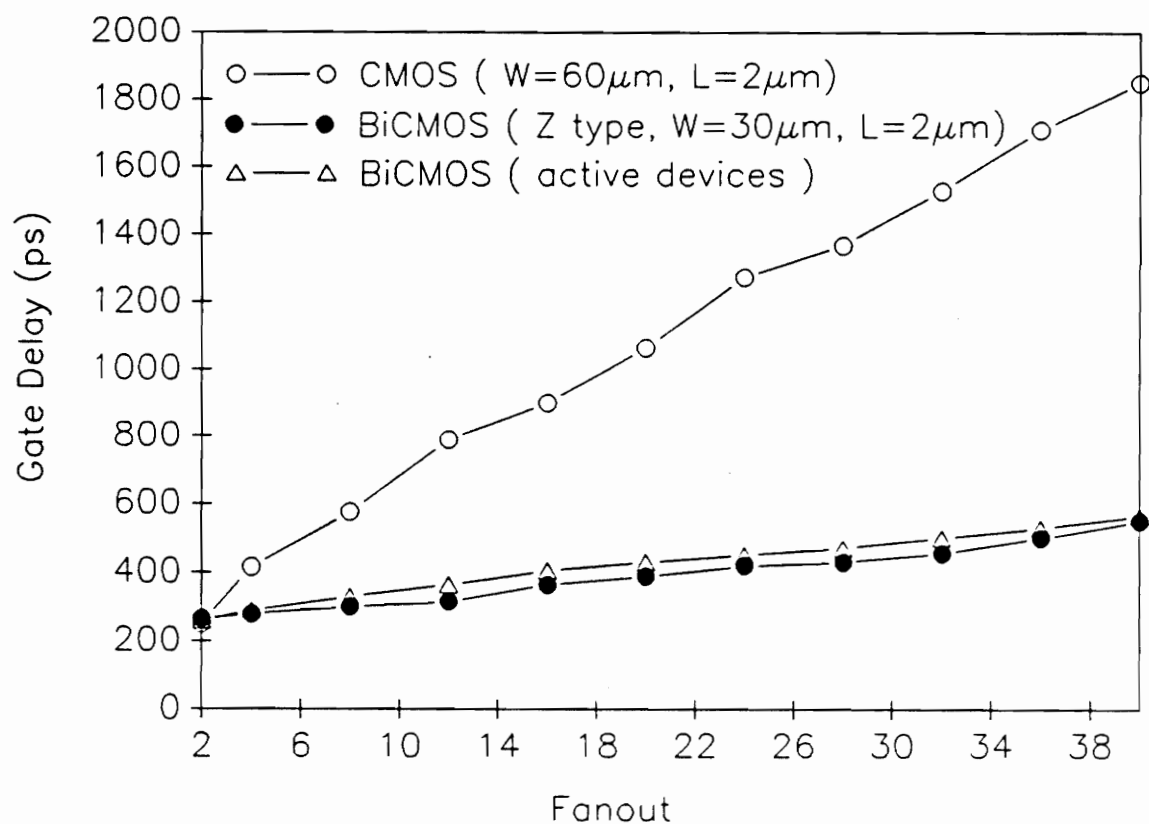


Figure 4.4. Gate Delay v/s Fanout Characteristic

4.3.2 Temperature

Temperature dependence of the gate delay is examined in Figure 4.5. There is an increase in gate delay at higher temperatures. CMOS is more prone to such variations than BiCMOS, although the difference is not great. Higher temperatures are encountered in military applications for instance, and it is desirable that device performance remains steady. Since gate delay is dependent on drive current, a simple explanation for the behavior indicated by Figure 4.5 can be offered :

In the CMOS inverter, the output driver is a MOS device whose drain current in saturation is given by

$$I_{dsat} = \frac{\mu \epsilon W}{2t_{ox}L} (V_{GS} - V_T)^2$$

where the mobility μ varies with temperature according to the relation [27],

$$\mu = \mu(300^\circ K) \left(\frac{300}{T} \right)^{1.5}$$

Hence, as temperature increases, MOS carrier mobility decreases, thereby lowering drain current and increasing gate delay.

For the BiCMOS inverter, the bipolar NPN transistor dominates the output response. For bipolar devices, the collector current is represented by the equation,

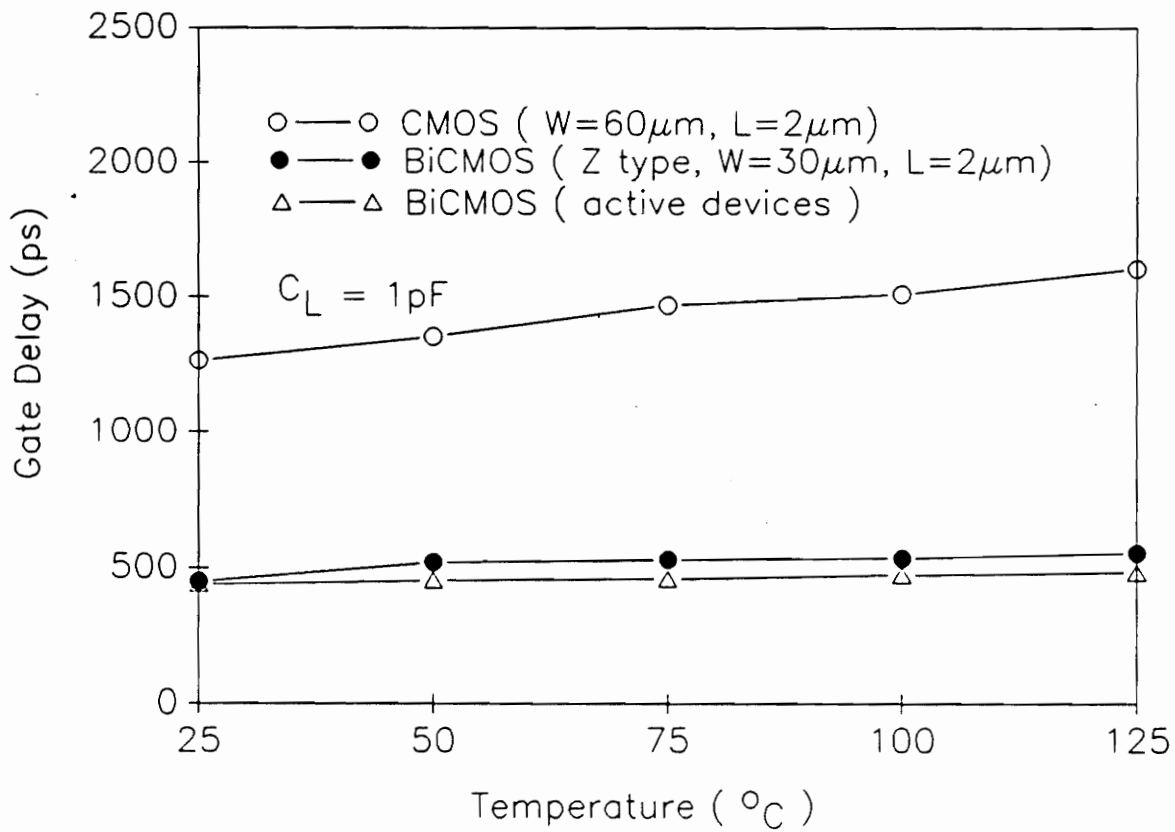


Figure 4.5. Effect of Temperature on Gate Delay

$$I_C = I_s \exp\left(\frac{qV_{BE}}{kT}\right)$$

Clearly, temperature variation has less of an effect on BiCMOS current capability than for CMOS. This results in a more stable current drive across a wide temperature range.

The one area where CMOS theoretically scores over BiCMOS is power dissipation. MOS devices have always been less power hungry than their bipolar counterparts. Consequently, most high density VLSI chips today utilize predominantly MOS technology. CMOS in particular, is a favorite with VLSI designers due to its near zero static power dissipation. However, dynamic power dissipation which occurs mainly during the switching transients, may not be significantly higher for BiCMOS. This is because BiCMOS devices, with their smaller voltage swing, spend less time switching. Figure 4.6 shows how power dissipation in the two varies as a function of ambient temperature. The superior static power characteristics of CMOS are clearly reflected in the overall measurements. The BiCMOS inverter with active devices dissipates maximum power due to the extra MOS transistors it incorporates. This effect is accentuated at higher temperatures and can be explained as follows :

For a MOS device, surface potential ϕ_s , is given by [27],

$$\phi_s = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

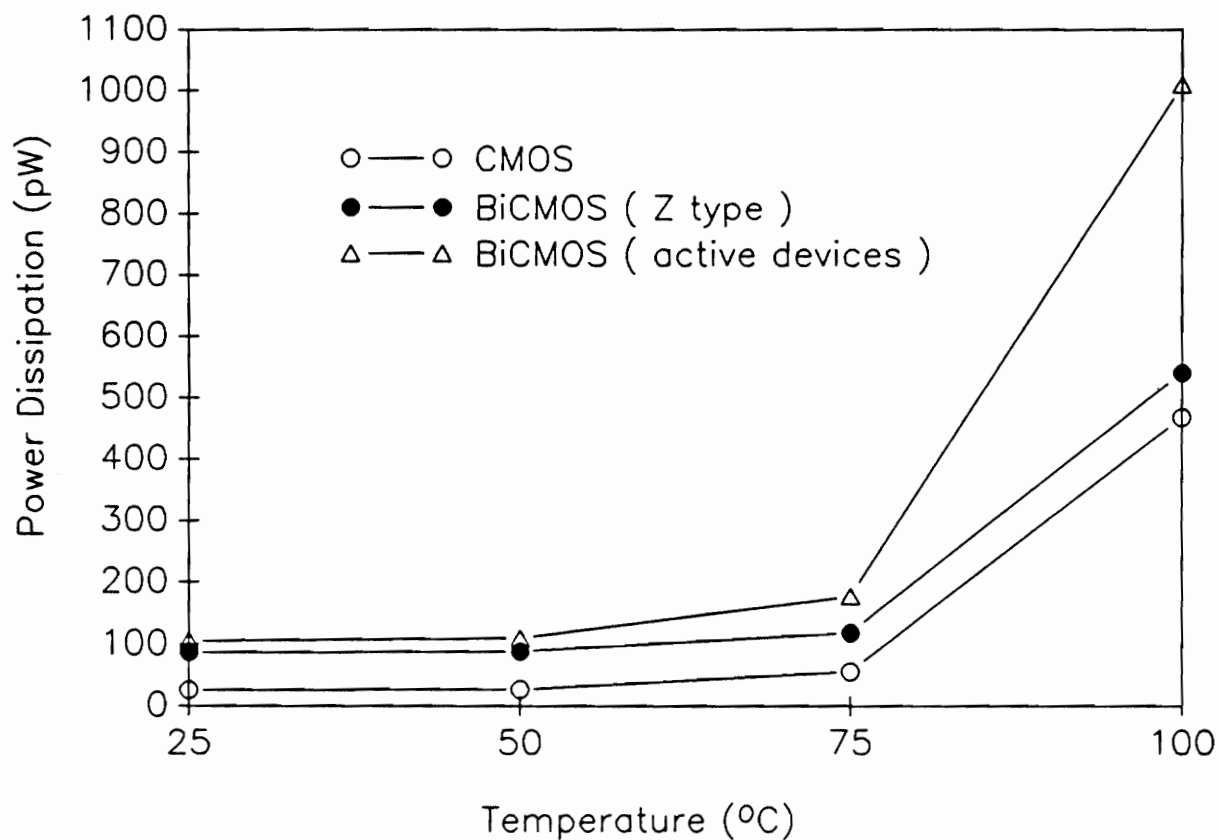


Figure 4.6. Power Dissipation v/s Ambient Temperature Characteristic

where N_A is the acceptor dopant concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, q is the electronic charge and T is the absolute temperature. The charge Q_G which determines the gate capacitance has the following relation [27] :

$$Q_G \propto \sqrt{2\epsilon_s q \phi_s}$$

Now, since

$$Q_G = C_G V_G$$

We know that an increase in temperature leads to a rise in surface potential and consequently C_G . Now,

$$\text{Dynamic Power} \simeq f C V^2$$

Increased capacitance results in more dissipation. This explains the role of temperature rise in increased MOS dynamic power dissipation.

4.3.3 Supply Voltage Scaling

As VLSI chips become more and more densely packed, there is definitely a case to be made for a downward scaling from today's supply voltage standard of 5 volts. Such a move would reduce on chip currents and power dissipation, making greater integration possible within limits imposed by acceptable dissipation levels. It is interesting to note

how such a move would affect device speed. In an inverting buffer circuit, the supply voltage is critical in speed calculations since it is the primary source of current while charging the output. Figure 4.7 indicates that the CMOS inverter is affected more by supply voltage scaling. To reduce these effects, device parameters have to be optimized further, placing greater strain on processing. BiCMOS is also affected but to a lesser extent. This may be accounted for by the fact that bipolar devices are inherently faster than MOSFETs, even at reduced supply voltages.

4.4 Influence of MOS Device Parameters

Having investigated the effect of changes in circuit and operating, parameters we now study the results of variation in MOS device parameters on CMOS and BiCMOS performance. This is particularly significant because most BiCMOS processes are necessarily CMOS based for reasons of economy and ease of integration.

4.4.1 Oxide Thickness

One such MOS process parameter is the gate oxide thickness t_{ox} , which affects the gate oxide capacitance directly :

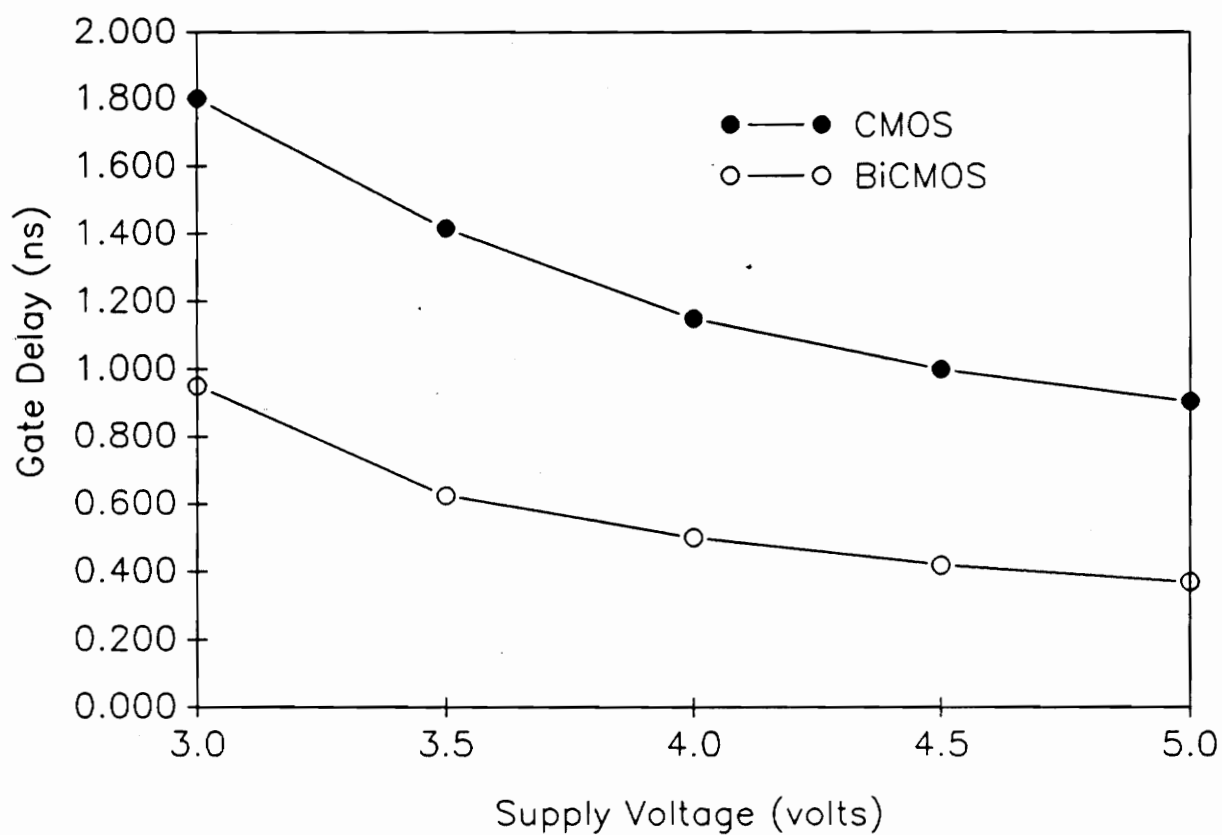


Figure 4.7. Effect of Variation in Supply Voltage

$$C_{ox} = \frac{\epsilon}{t_{ox}}$$

Now since,

$$I_{dsat} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2$$

From the above expressions, it is clear that increased oxide thickness will decrease the drain current. Figure 4.8 demonstrates how such a variation affects both technologies. CMOS gate delay is adversely affected by large oxide thicknesses. The BiCMOS gate on the other hand exhibits great tolerance to such changes mainly because the dominance of the bipolar devices compensates for any potential performance degradation. Figure 4.8 also indicates that to obtain enhanced CMOS performance, t_{ox} dimensions must be scaled downwards aggressively. This involves increased process complexity and costs. Use of BiCMOS can avoid the need for such downscaling and associated costs.

4.4.2 Mobility

Another important MOS device parameter is the mobility of n and p carriers, which is a function of the surface roughness and presence of oxide traps which can trap and retard these carriers. One empirical relationship that has been suggested for surface mobility μ [27], is

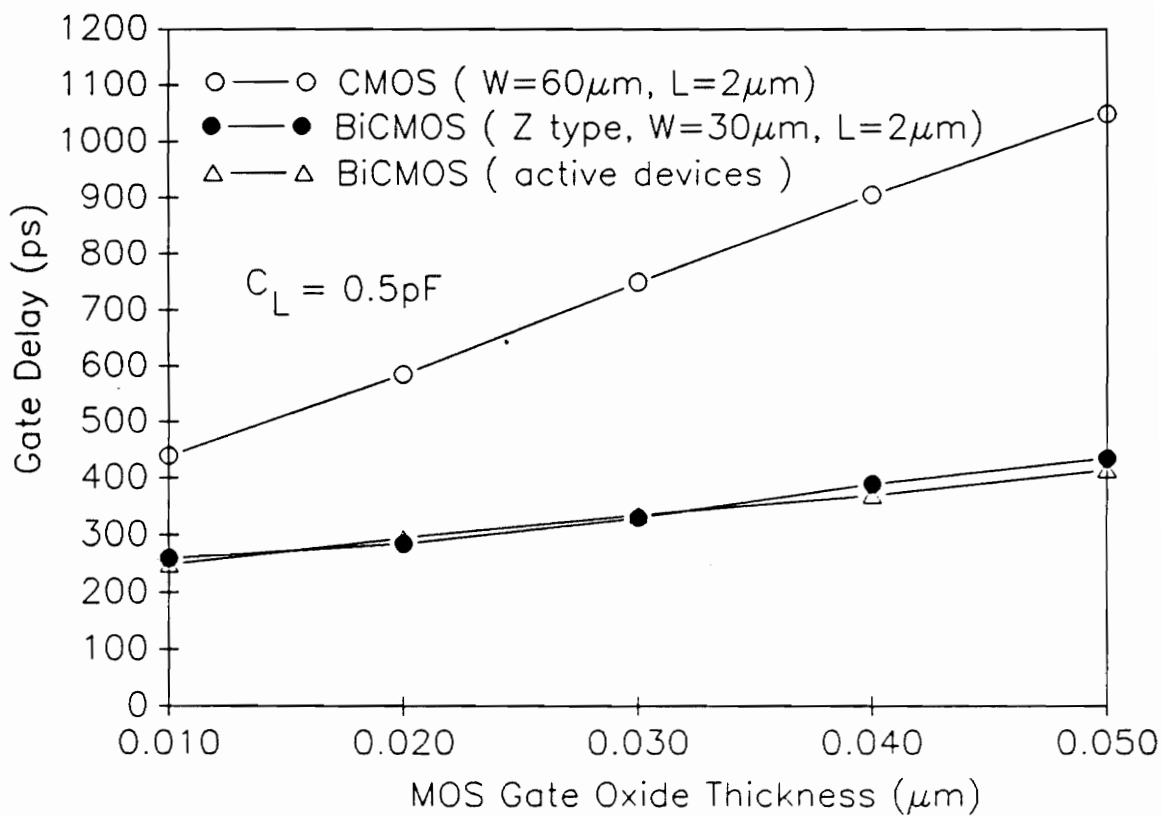


Figure 4.8. Gate Delay v/s Gate Oxide Thickness Characteristic

$$\frac{1}{\mu} = \frac{1}{\mu_o} + FRC \frac{V_G - V_T}{t_{ox}}$$

where

μ_o – low field mobility

FRC – field reduction coefficient in sec/cm

$\frac{V_G - V_T}{t_{ox}}$ – vertical field across oxide

Mobility is constant at low gate fields and starts decreasing as gate field strength increases. The above expression also indicates that mobility is dependent on oxide thickness. The electron to hole mobility ratio usually ranges from 2 to 4. Hence, in CMOS design, the width of the PMOS device is increased to compensate for this difference in mobilities. In this study, the effect of a composite increase in both NMOS and PMOS mobilities has been obtained by assuming that μ for both carriers changes uniformly and in step. The average MOS Surface Mobility shown in Figure 4.9 is the average of the n and p carrier mobilities. From the figure, it is clear that gate delay decreases with increased mobility. The effect is more pronounced for CMOS emphasizing again, how important MOS process improvements are for this technology. Such variation has less of an effect on BiCMOS, verifying its robustness.

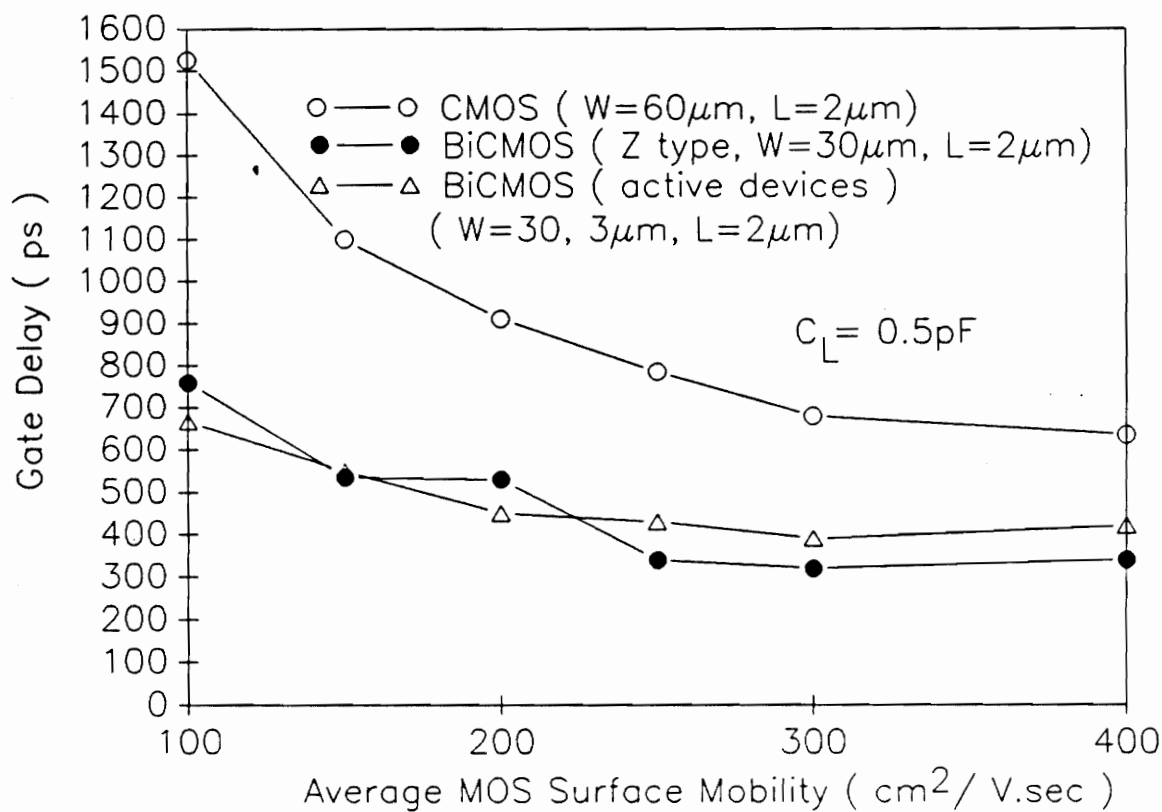


Figure 4.9. Gate Delay v/s Surface Mobility Characteristic

4.4.3 MOS Device Scaling

CMOS process technology has reached a high level of complexity. The 1 micron barrier has been surmounted and sub micron processing is very common today. However, this progression towards smaller dimensions has placed a very heavy burden on equipment and fabrication costs. There is always a search for ways and means to prolong the life of existing fabrication lines. Figure 4.10 shows the effect of MOS device dimension scaling on performance. The smallest possible dimension in a MOS technology is usually reflected by the gate length which is kept as short as possible for obvious reasons. Shorter gate lengths mean lower transit times for channel carriers and faster gate operation. However, there is a limit on minimum channel lengths due to short channel effects where the gate loses control over carrier flow. The graph in Figure 4.10 is more illustrative if the x-axis is viewed from right to left. Downward MOS technology dimension scaling significantly enhances CMOS performance while BiCMOS continues to enjoy relative immunity to such variation. More evidence that CMOS technologies of the future are going to be expensive and that BiCMOS could provide a means to avoid such costs.

4.4.4 Threshold Voltage

The MOS threshold voltage is a device parameter of primary importance in integrated circuit design. It has a direct impact on the speed and noise margin of the device. The speed aspect is clear from the following relation for the drain current for an NMOSFET in saturation :

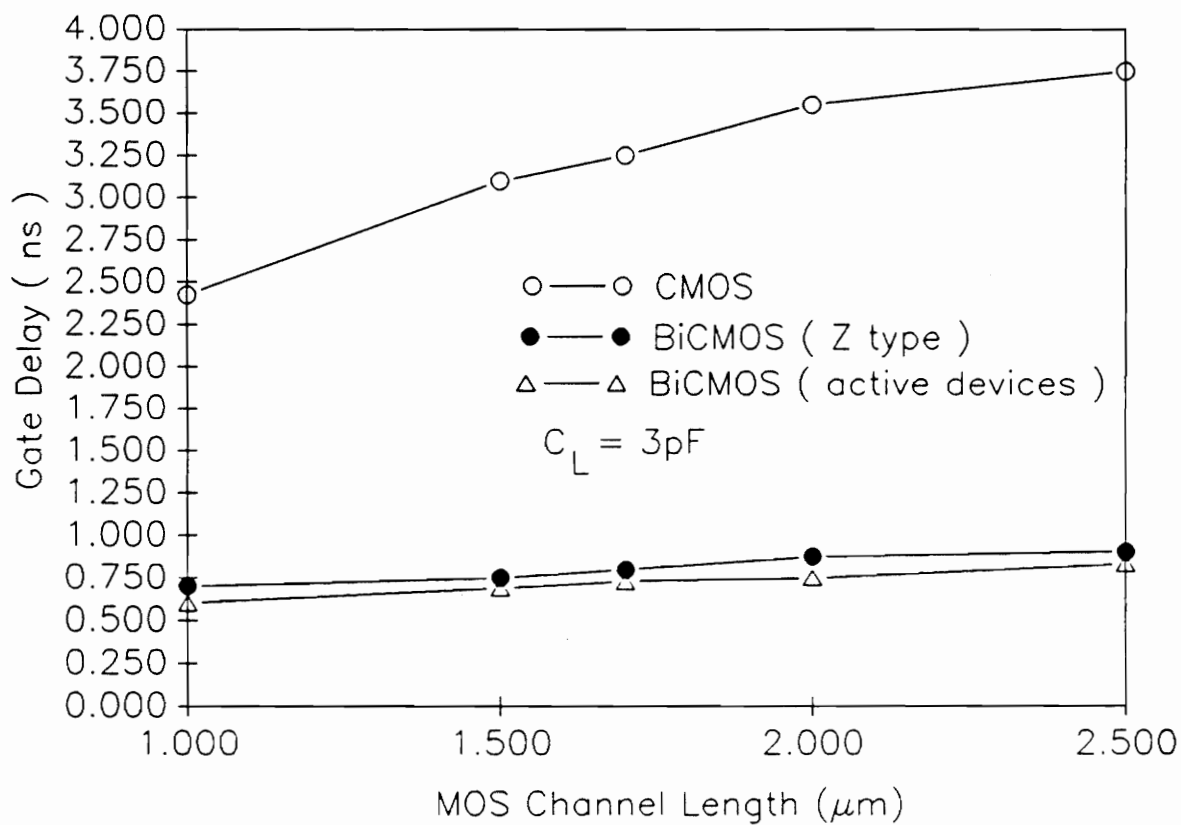


Figure 4.10. Effect of MOS Channel Length Scaling

$$I_{dsat} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2$$

An increase in V_T decreases the drain current and as a result the speed of the device. Also, it is clear that high threshold voltages will decrease the noise margin by increasing the voltage at which the device turns on. Both these effects are undesirable. V_T is of the form [27],

$$V_T = \phi_{MS} - \frac{qN_{SS}}{C_{ox}} + 2\phi_p + \gamma\sqrt{2\phi_p}$$

where γ is the body effect parameter, ϕ_p is the surface potential, N_{SS} is the background doping concentration, q is the electronic charge and C_{ox} is the gate oxide capacitance. ϕ_{MS} [27] is given by :

$$\phi_{MS} \simeq -\frac{E_G}{2} - \frac{kT}{q} \ln \frac{N_A}{n_i}$$

E_g being the energy bandgap for the material. The threshold voltage is determined mainly by the channel design and doping. Figure 4.11 indicates that variation in V_T has a greater impact on CMOS gate delay than on BiCMOS. This is a direct result of reduced drain current with increased V_T . However, it must be noted that MOS threshold voltages must be kept under close control in BiCMOS devices that do not possess rail to rail swing. High threshold voltages can cause false switching.

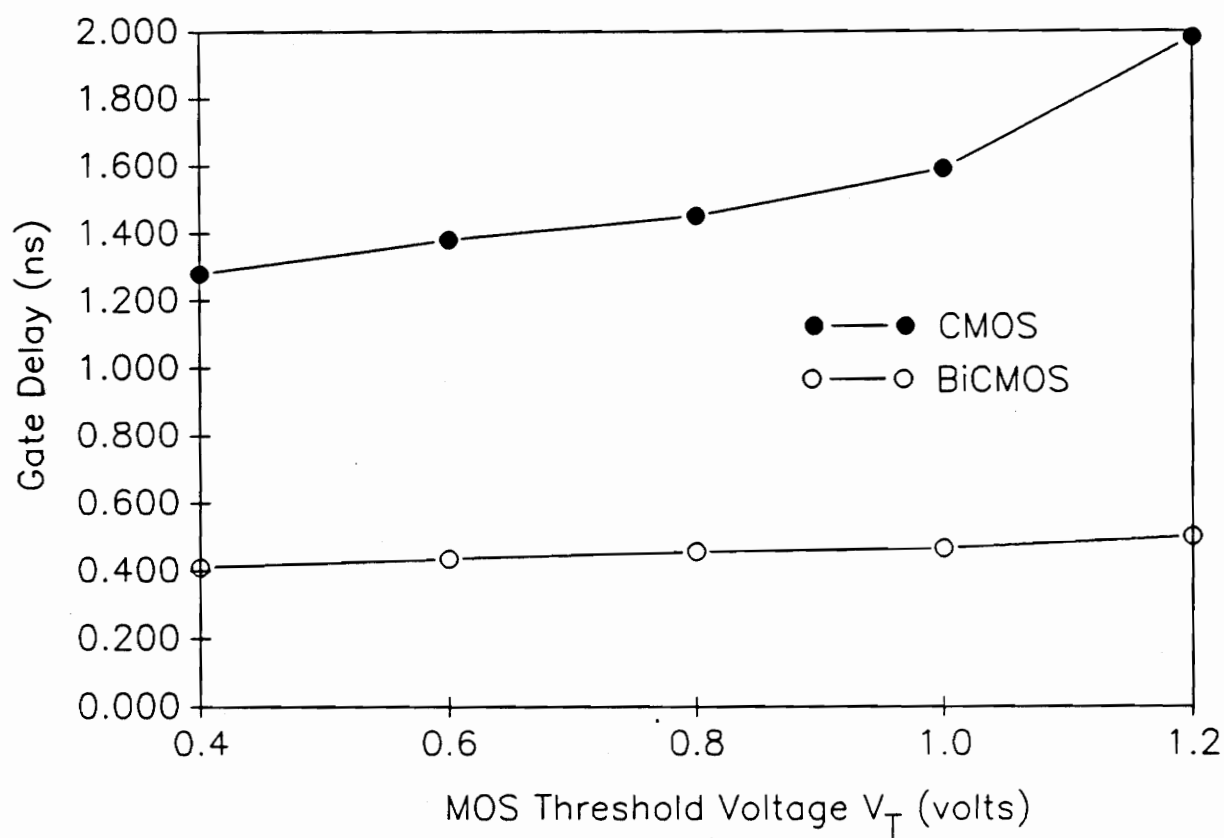


Figure 4.11. Effect of MOS Threshold Voltage variation

From these studies of the effect of MOS device parameter variations on the two technologies, we are able to conclude that BiCMOS shows far greater robustness towards such variations. This is an extremely desirable characteristic and is strong evidence that BiCMOS is very much the technology to turn to as greater demands are placed on performance of VLSI chips. We now move to study the effects of variation in bipolar device parameters on BiCMOS response.

4.5 Influence of NPN Device Parameters

The remarkable immunity of BiCMOS to MOS parameter variations is principally because bipolar devices play a dominant role in determining the delay and current drive characteristics of BiCMOS gates. It is logical therefore, to examine how bipolar parameter variations affect these characteristics. We shall study the emitter, collector and base regions along with the factors influencing their design, separately.

4.5.1 Emitter Design

The emitter capacitance is more of a parasitic effect than a device parameter. The effect of variation in C_E on the BiCMOS inverting buffer current drive capability, is not very significant. This is shown by Figure 4.12. The peak current levels are fairly steady throughout the range of C_E variation. However, it is always desirable to keep parasitics

at a minimum. Emitter design should always try to minimize capacitance and resistance. Normally, in bipolar design emitter doping is around $1E20\text{ cm}^{-3}$ to improve emitter efficiency and keep emitter resistance low. As the base width is decreased to improve performance, the emitter junction depth must be decreased to ensure good performance and manufacturability. Use of conventional metal contacts can lead to reduction in current gain β . Polysilicon contact emitters can be used to alleviate this problem. Use of polysilicon leads to an increase in emitter resistance. Hence, there is a tradeoff involved here. Arsenic or phosphorus can be used to dope the poly emitter. Use of phosphorus facilitates lower contact resistance. However, shallow emitters and narrow bases that are required for high performance NPNs can be difficult to achieve with phosphorus. Here, arsenic has an advantage. Usually, phosphorus is used for low frequency transistors while As is used where cut off frequencies greater than 10GHz are required [28].

4.5.2 Collector Design

The analytical model for the BiCMOS inverting buffer demonstrated that when the bipolar transistors enter the collector saturation region, the collector resistance and capacitance begin to dominate the output response. Figure 4.13 indicates that increased collector capacitance clearly inhibits the ability of the gate to drive loads quickly. The effect of variation in collector resistance, on gate delay is not quite as obvious. In Figure 4.14, two types of delay are plotted along the vertical axis. Gate delay, as defined earlier, is measured between the 50 percent voltage levels. The Rise/Fall delay on the other hand, is the average of the rise and fall times, measured between the 10 percent and 90

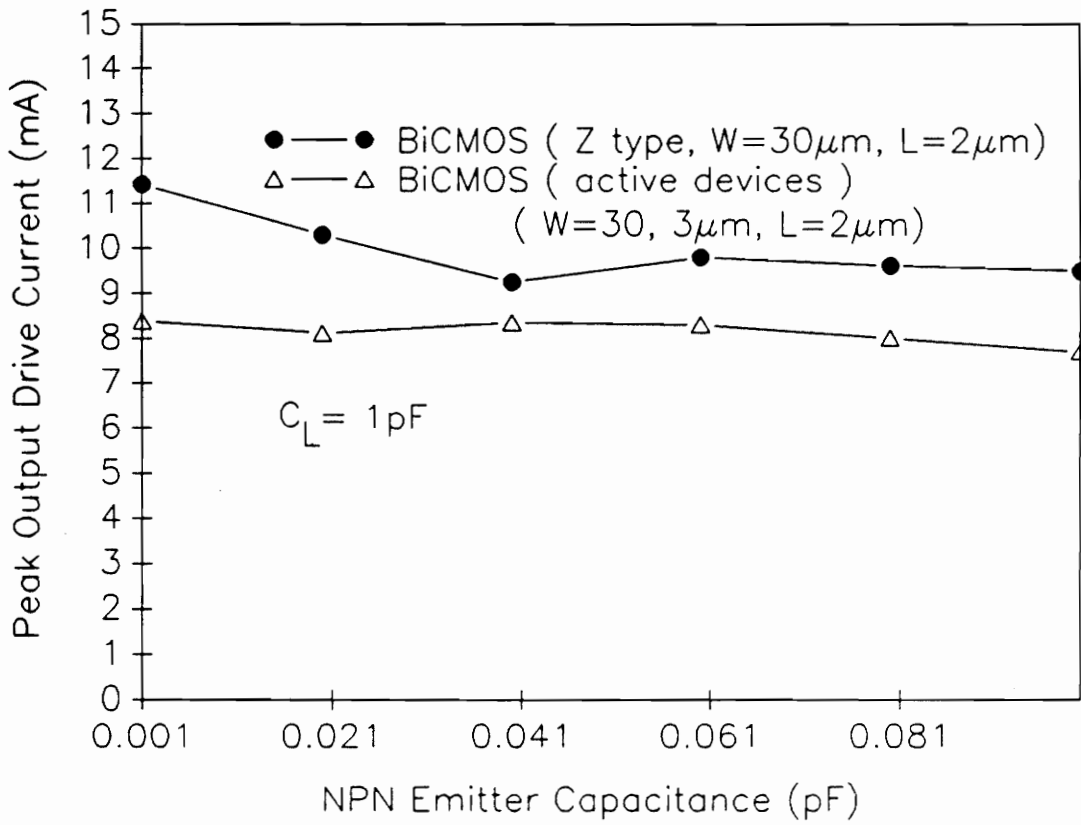


Figure 4.12. Peak Output Drive Current v/s Emitter Capacitance

percent levels. Collector resistance does not seem to affect gate delay very much, but it definitely impacts the rise and fall delays. This can be explained by the fact that collector saturation effects are felt mainly at the end points of the rise and fall responses. The midpoint of the switching curve at which gate delay is measured is not degraded. However, degradation at the edges can affect gate delay if the input pulse is not broad enough so as to allow the output to settle before switching again. Therefore, it is always desirable to keep R_C as low as possible.

The collector doping is made high to delay the onset of high level injection effects which may reduce the current gain. But, such doping may be limited by the collector-base and collector-emitter breakdown voltage considerations [28]. The N-well region which forms the collector must also be optimized with respect to MOS parameters such as threshold voltage, source drain capacitance and body effect.

4.5.3 Base Design

The base region parameters that were shown to affect the delay in the analytical model include the base resistance R_B , the forward base transit time τ_F , and the forward current gain factor β_F . If we denote the charge responsible for the base region current as Q_B it is known that Q_B is equal to the integral of the base dopant between the two space charge regions. Now, the base current is given by $I_B \simeq \frac{I_C}{\beta}$ where I_C is the collector current and β is the current gain. I_B is therefore inversely proportional to β which means that $Q_B \propto 1/\beta$. Hence, the base doping sets a limit for the collector current and the current gain. But, such doping helps reduce the base resistance. Figure 4.15 shows that increased base resistance shows a tangible but not dramatic effect on the gate delay.

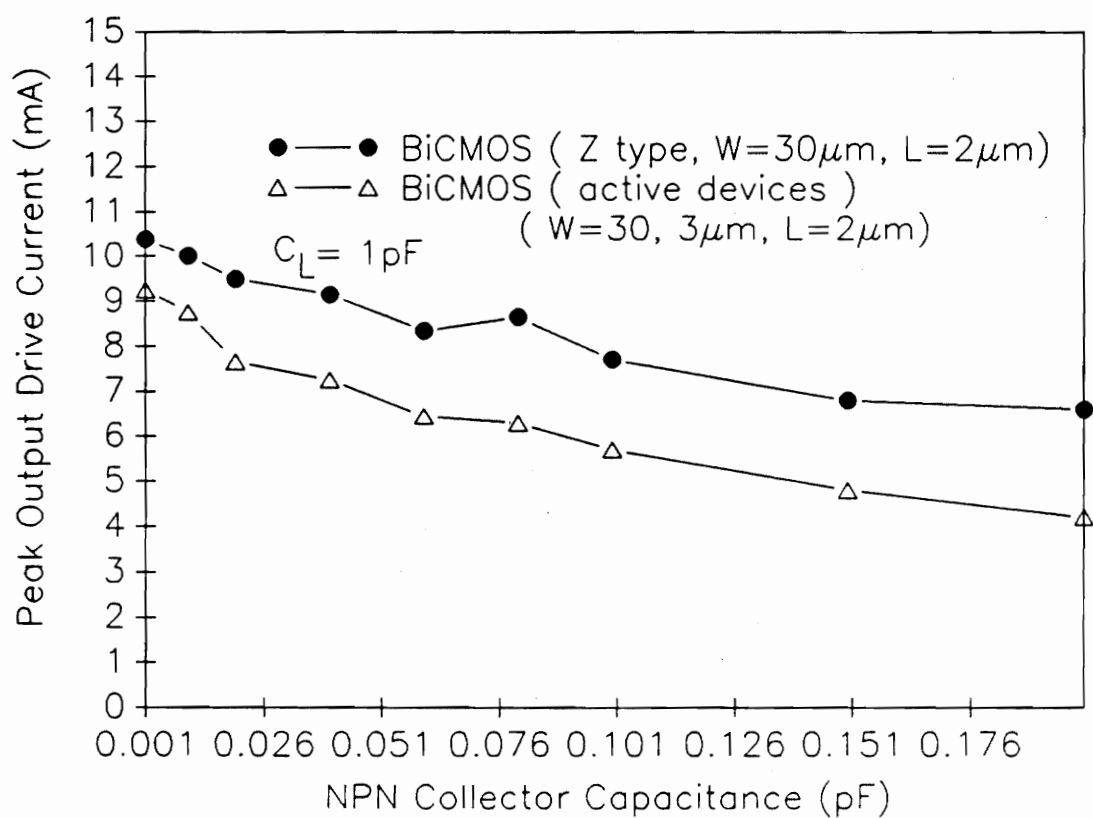


Figure 4.13. Inverter Peak Output Drive Current v/s Collector Capacitance

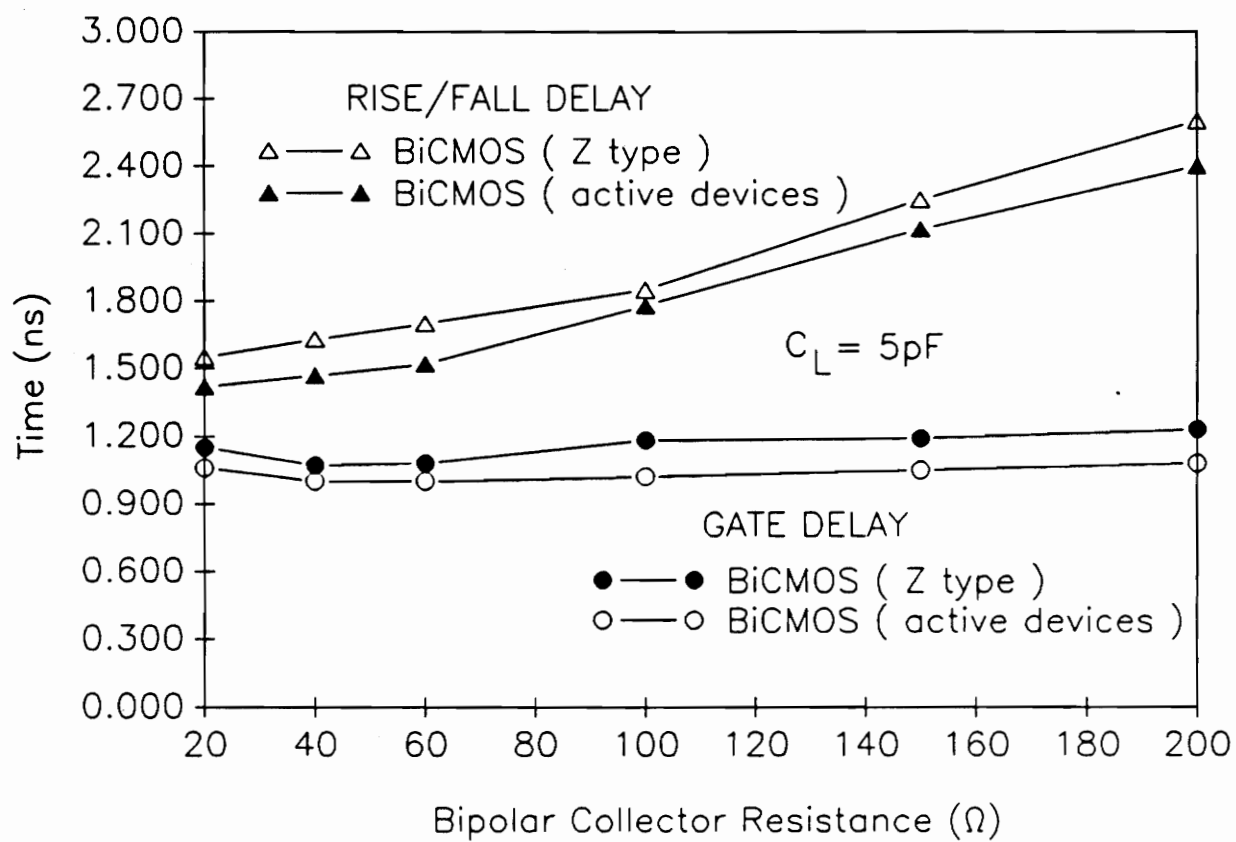


Figure 4.14. Effect of Collector Resistance variation on Gate Delay and Rise/Fall Delay

Figure 4.16 details the impact of variation in β on output drive current capability. It would seem that an optimal β value would be in the 100-120 range. Beyond this there seems to be levelling off and even a drop in current capability. The indication is that high beta NPNs or "superbeta" transistors as they are sometimes called, will not impact BiCMOS performance. The aim should therefore be to achieve a β of 100-120 while minimizing R_B . There is a tradeoff involved here since increased base doping decreases R_B which is desirable and reduces β which may not be an advantage.

Another important performance parameter is the forward base transit time τ_F . Figure 4.17 clearly shows that increased τ_F leads to larger gate delays. This increase is fairly uniform across the entire range of values, so there is a definite incentive to keep τ_F as low as possible. This may be done by minimizing the base width. However, base width is limited by a phenomenon called punchthrough wherein the base loses control over flow of carriers [28]. Punchthrough is controlled by high base doping. Such doping can also help control high level injection effects that reduce the forward current gain. However, as mentioned before, high base doping levels may adversely affect the β factor itself. This is yet another design tradeoff that must be lived with. It may be noted here that reduced base width also leads to an increase in the unity gain cutoff frequency, which is a primary AC performance measure for bipolar transistors, especially in analog applications.

4.5.4 Bipolar Device Scaling

Time and again in these discussions, the dominance of the bipolar transistors in BiCMOS response has been stated. The obvious question is how the scaling of these

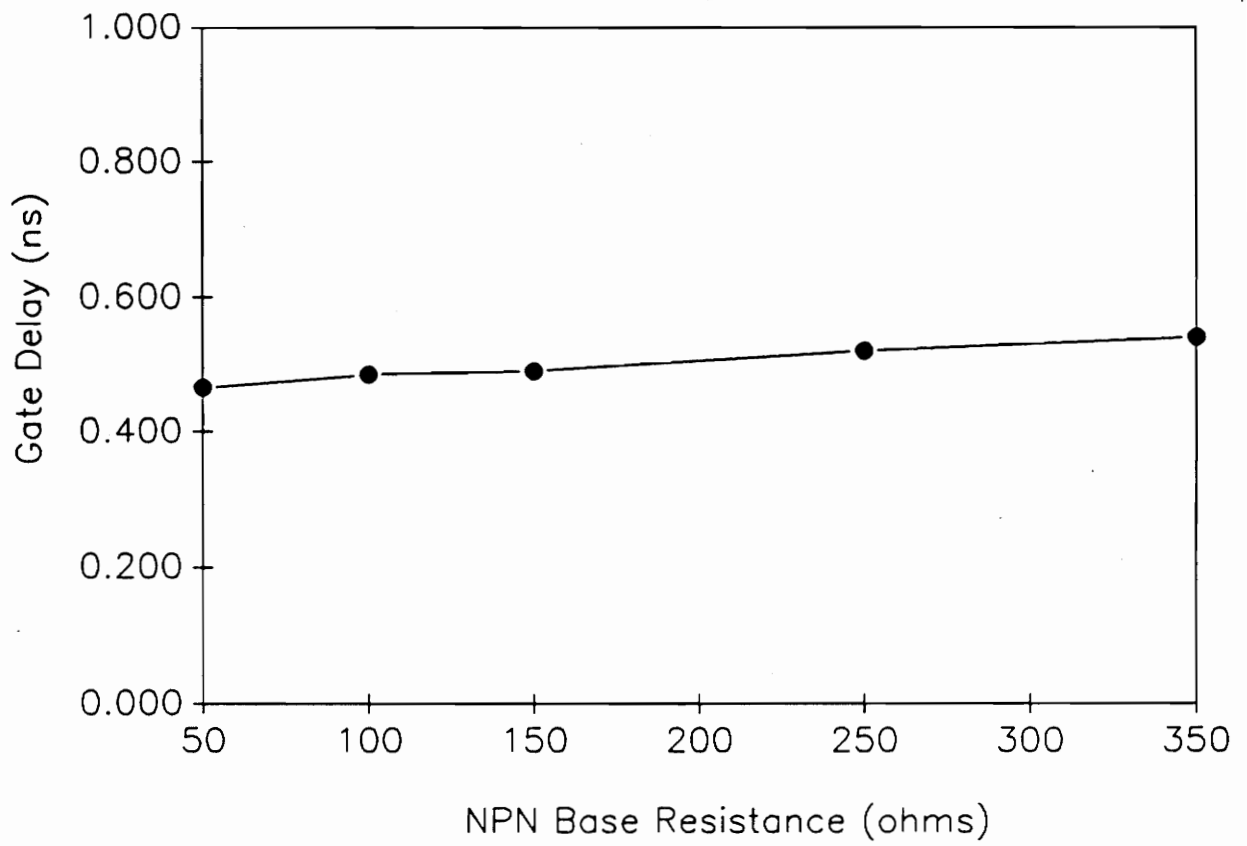


Figure 4.15. Gate Delay v/s Base Resistance Characteristic

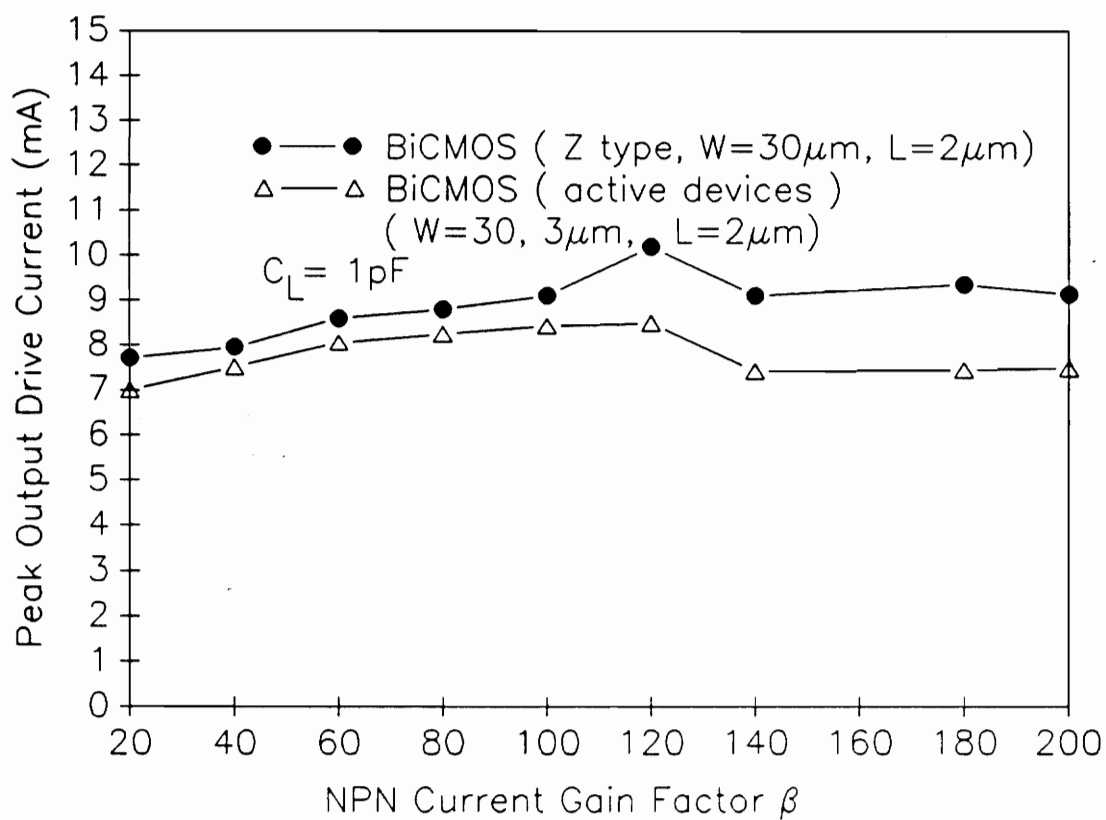


Figure 4.16. Gate Delay v/s Forward Current Gain Factor Characteristic

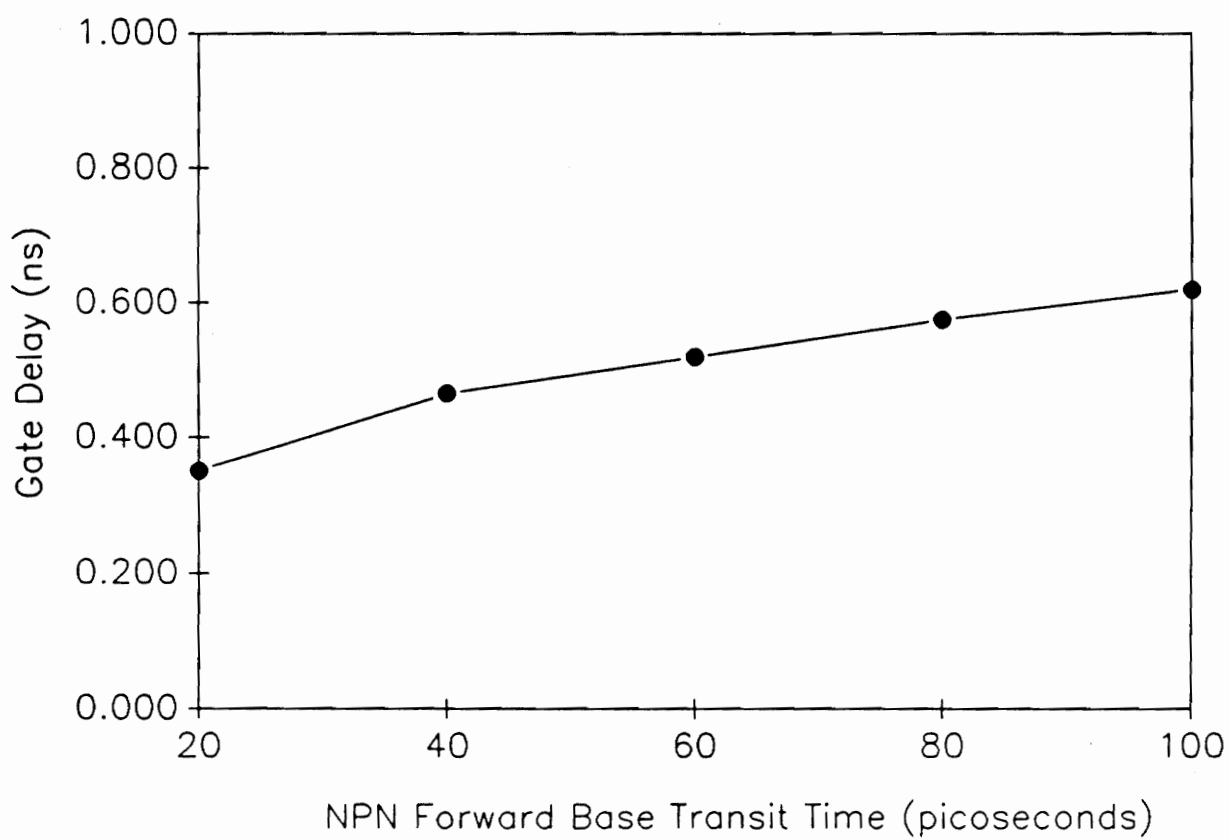


Figure 4.17. Gate Delay v/s Forward Base Transit Time Characteristic

bipolar devices affects the performance of BiCMOS gates. In PSPICE, there is a scale factor that can be used to increase bipolar device size. Throughout the study so far, unit sized bipolar devices have been assumed. There is no specific model entry in PSPICE that allows us to control the size of the NPN device. The AREA parameter determines the number of equivalent parallel devices connected in parallel. The default value is one. The principal BJT parameters affected by scaling of this factor and the nature of this effect are listed below [27] :

$$I_s = I_s \times AREA$$

$$I_F = I_F \times AREA$$

$$C_{JC}(0) = C_{JC}(0) \times AREA$$

$$C_{JE}(0) = C_{JE}(0) \times AREA$$

$$C_{JS}(0) = C_{JS}(0) \times AREA$$

$$r_B = r_B / AREA$$

$$r_E = r_E / AREA$$

$$r_C = r_C / AREA$$

Figure 4.18 shows that upward scaling of the AREA factor and hence of the bipolar devices has only a marginal impact on gate delay. This could be attributed to the fact that parasitic capacitances increase and play a major part in nullifying the expected gains due to device size. These results seem to indicate that minimum sized bipolar devices

display acceptable drive characteristics and there is no need for larger devices. This is an asset when the real estate constraints on modern day VLSI chips are considered.

4.6 Inverter Types and Multi Input Gates

In this study of the effects of device parameters on gate switching, we have at times, examined both types of BiCMOS inverters - the Z-type and one with only active devices. Essentially, both inverters display good performance. The advantage of the Z-type is the full 0 to 5V logic swing it offers. The drawback is the use of passive resistors which may be difficult to fabricate. One way around this is to use active devices suitably configured as resistors. Here, there may be some problems with controlling the resistance values. The BiCMOS inverter with active devices does not offer a full voltage swing but this may not be important as long as MOS threshold voltages are monitored. The all-active device configuration is definitely easier to fabricate. Hence, in terms of overall performance, the ultimate choice between the two is not all that important. Both offer considerably enhanced switching characteristics over the CMOS inverter.

The inverting buffer gate has been used throughout this study in order to evaluate BiCMOS technology and compare it to CMOS. We would expect the superiority of BiCMOS to extend into the realm of multi input logic gates. Along with the inverter, the NAND and NOR gates make up the three principal types used in digital VLSI design. It is useful to check how BiCMOS performance compares with CMOS for these gates. Figure 4.19 shows a 2 input BiCMOS NAND gate [28]. The basic structure is the same as CMOS with 2 NMOSFETs in series and two PMOSFETs in parallel. In addition,

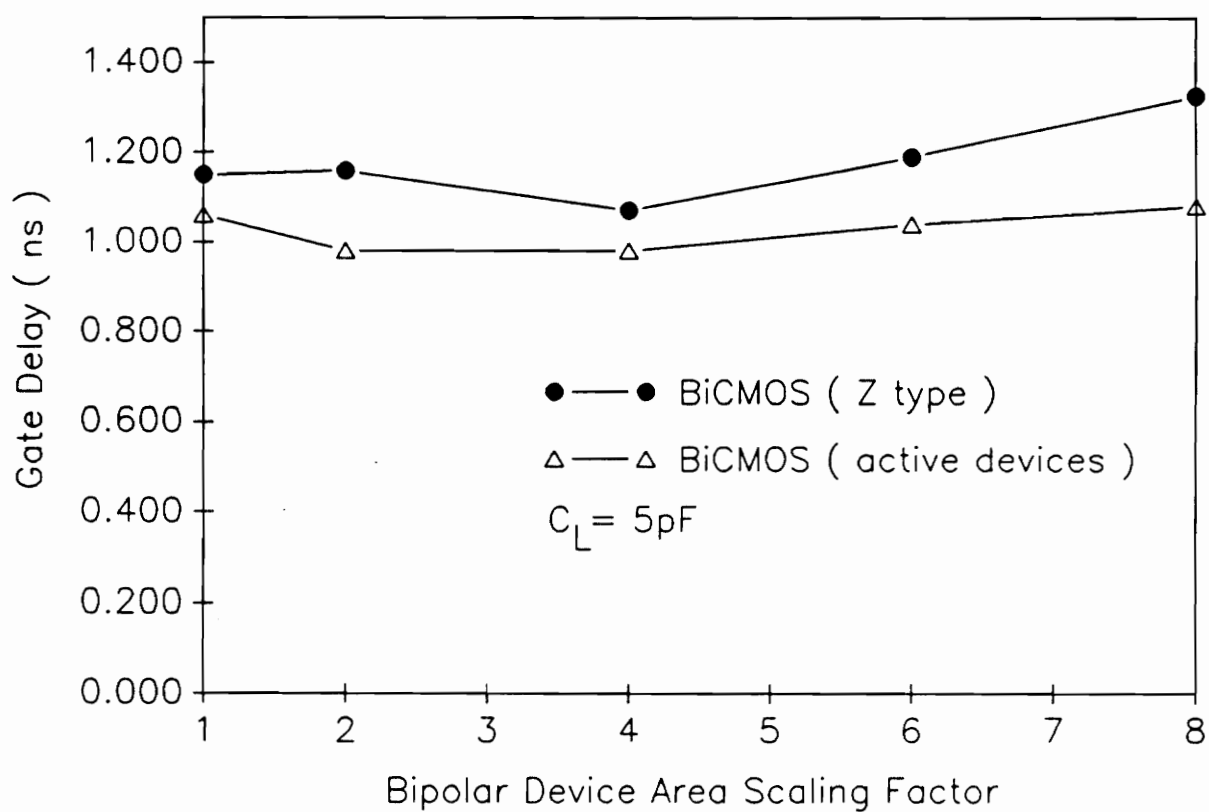


Figure 4.18. Effect of Bipolar Device Scaling on BiCMOS Gate Delay

there are two NPN devices for enhanced current drive. NPN transistor Q1 can turn on only when M1 or M2 or both are on and supply the base drive. Once Q1 is turned on, the load capacitance is charged and the output goes to logic '1'. For the discharge, both M3 and M4 have to be on to provide a current path from the output to the Q2 base. After Q2 has been turned on, the load is quickly discharged and the output goes to logic '0'. This represents the NAND function i.e. the output is low only when both inputs are high. Resistors Z1 and Z2, as in the case of the inverter, help provide a complete logic swing after the active devices have been turned off.

The BiCMOS NOR gate shown in Figure 4.20 has its PMOS devices in series and NMOS devices in parallel. Here, both P devices must be on (inputs low) for the output to be charged high. Again, Q1 is responsible for the output drive. A high on any one of the inputs or both will turn on the NMOS devices that feed the base of Q2, which discharges the load. Z1 and Z2 provide rail to rail logic swing. Figure 4.21 shows the worst case gate delays for CMOS and BiCMOS. For the NAND gate the worst case delay occurs when only one P device is available to charge the load. For the discharge, there is no choice since both NMOS devices have to be on. For the NOR gate, worst case discharge is when only one NMOS device is on. Figure 4.21 shows that BiCMOS has a clear advantage over CMOS. The worst case delays for NOR CMOS gates are seen to be higher than CMOS NAND delays. For equal device sizes, a CMOS NOR gate is inherently slower than its NAND counterpart because the slower P devices are in series. P devices are 2 to 4 times slower than N devices. Of course, transistor size ratioing may be employed to circumvent this at the cost of increased area. Interestingly, the BiCMOS equivalents show negligible difference in performance. Yet again, bipolar device dominance compensates for the effects of degraded MOS characteristics.

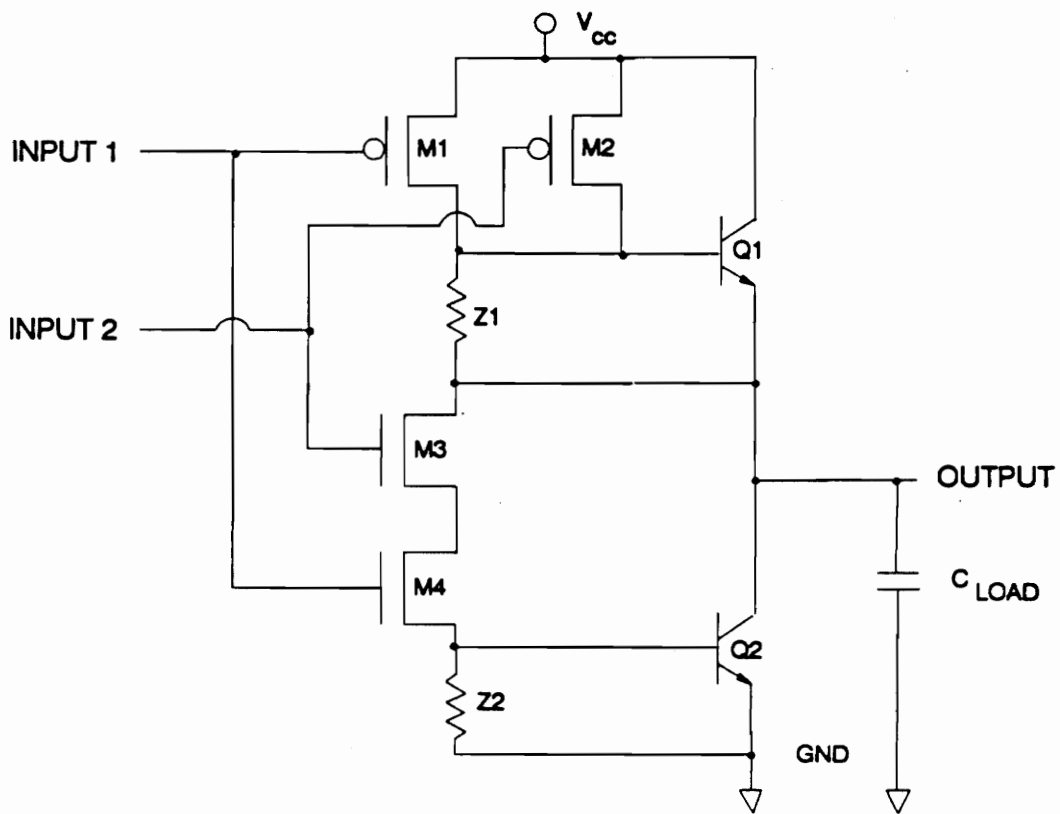


Figure 4.19. 2 input BiCMOS NAND gate

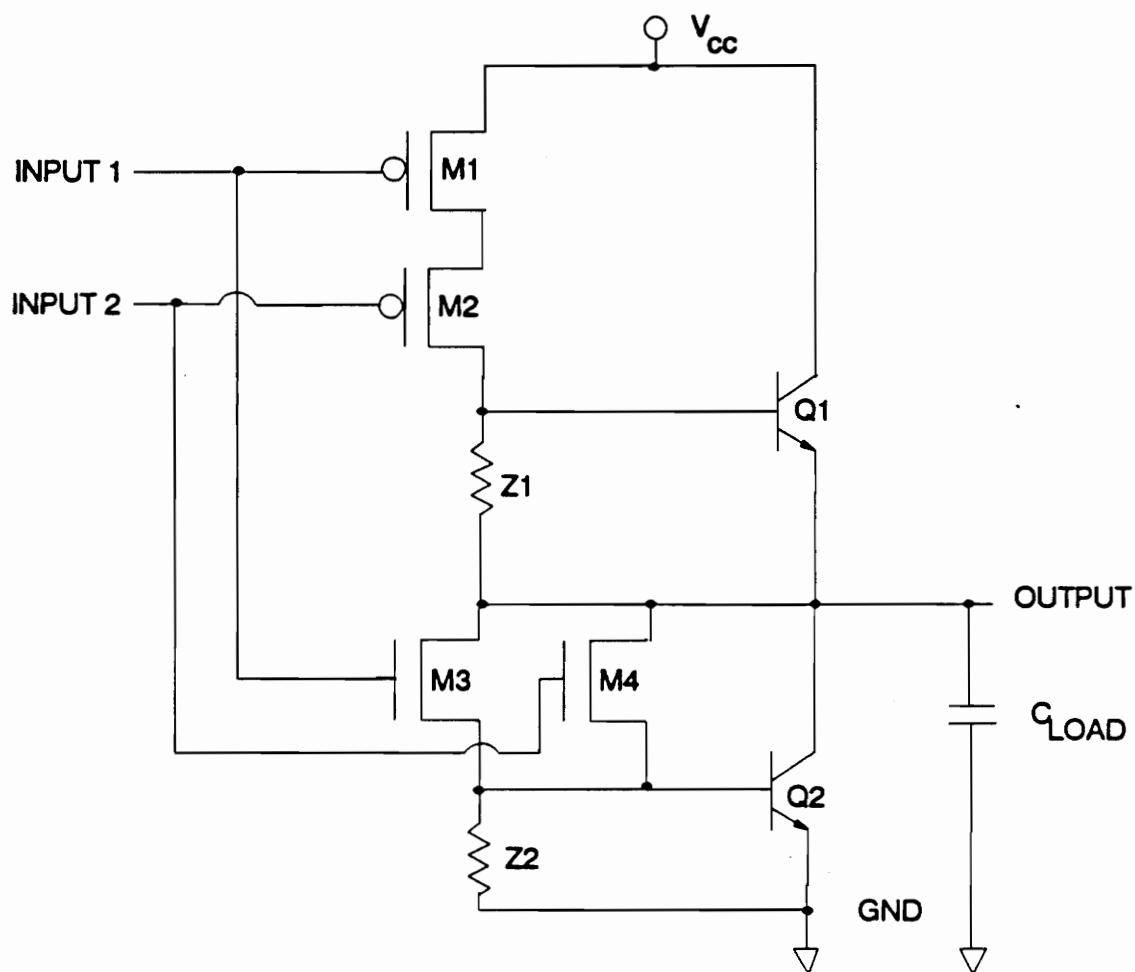


Figure 4.20. 2 input BiCMOS NOR gate

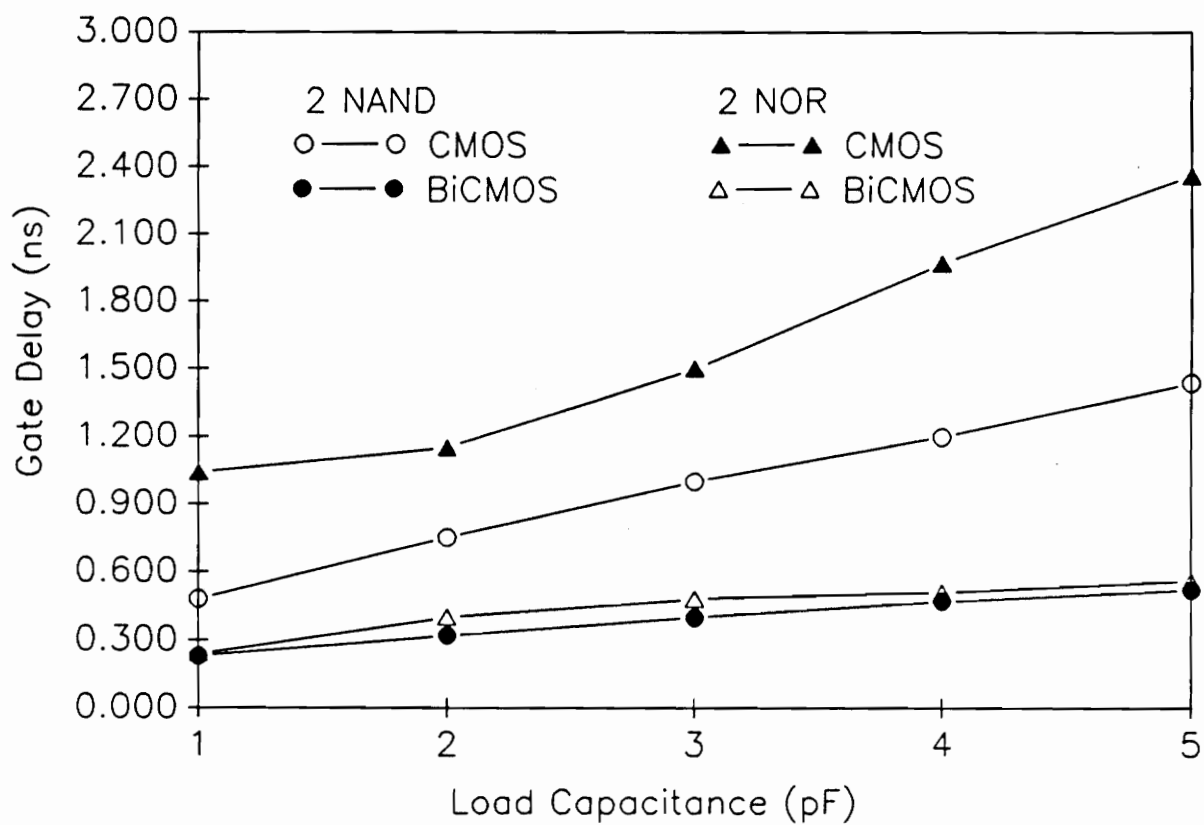


Figure 4.21. Comparison of CMOS and BiCMOS 2 input gates

4.7 *BiCMOS Applications*

In this chapter we have tried to gain an understanding of the device and circuit parameters that affect BiCMOS and have seen that it offers many advantages over conventional CMOS technology. In Chapter 2, many emerging applications of BiCMOS have been referred to. Our main focus has been on optimization of parameters for digital applications since VLSI has been most prevalent in the digital circuits area. However, analog VLSI has gained ground rapidly and BiCMOS has something to offer here. In the following sections some typical applications of BiCMOS in both areas will be described.

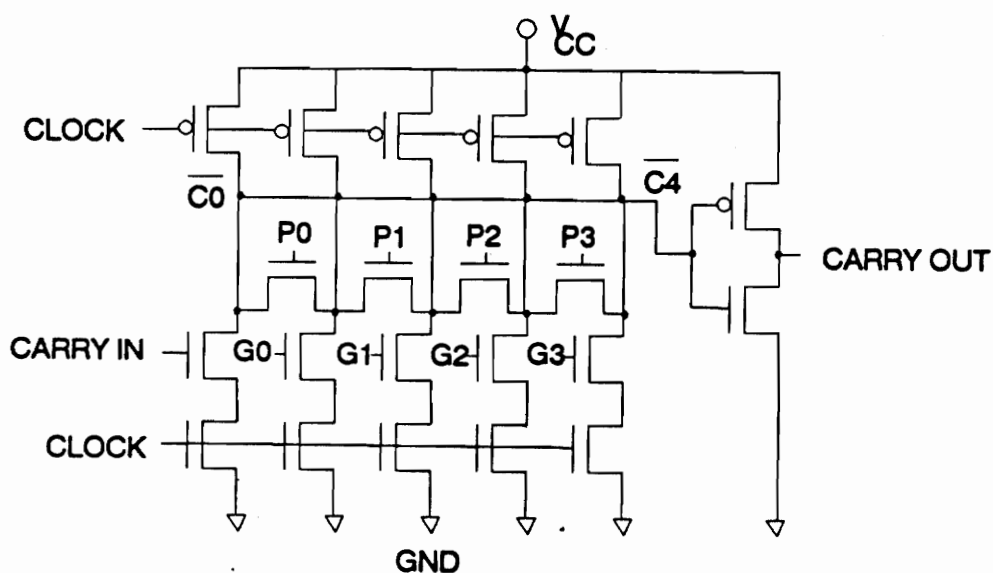
4.7.1 Digital BiCMOS

So far, BiCMOS has made an impact mainly in the digital VLSI area. The potential advantages of enhanced speed due to integrated bipolar devices are very attractive. In Chapter 2 we have seen that high performance processor chips utilizing this technology are emerging and fully commercial implementations are not very far off. The arithmetic and logic unit (ALU), is the core of any processor design and adder circuits are an integral part of these units. In a typical full adder circuit there is always a carry chain circuit which propagates the carry signal. Very often the worst case adder delay is determined by the delay through the carry chain. To minimize this delay, local carry signals are generated separately rather than doing this for each bit of the adder and feeding it to the next stage.

The CMOS version for a 4 bit carry chain is shown in Figure 4.22a. A single phase clock is used to select the mode of the circuit which is dynamic in nature. When the clock signal is low, the PMOS devices in the top row are on and precharge the nodes denoted by C0-C4. The worst case delay through this chain occurs when all the propagate signals (P0-P3) are high and all generate signals (G0-G3) are low. When the CARRY IN signal goes high and the clock is also high, the node denoted by the complement of C4 has to discharge through six NMOS devices. After added delay through the inverter, the CARRY OUT signal becomes available.

In the BiCMOS version, all but one of the PMOS precharge devices are eliminated. An NPN transistor in common emitter mode with a collector load, replaces the CMOS inverter. The lack of precharge PMOS devices is more than compensated by the bipolar device's superior drive capability. Once again the worst case delay will occur through the six NMOS devices. The SPICE plots in Figures 4.23a and 4.23b demonstrate how much faster the BiCMOS chain is. The propagation delay through the chain, measured by the time lag between the moment CARRY IN goes high and the instant at which CARRY OUT changes, is 2.3 ns for BiCMOS and 6.4ns for CMOS - a performance edge of a factor of nearly 3. This indicates that BiCMOS can play a very important role in speeding up combinational logic circuits. A SPICE listing for this simulation is available in Appendix B. The voltages shown in Figures 4.23a and 4.23b are as per this listing. V(4) is the CARRY IN signal and V(18) is the CARRY OUT voltage.

Many of the publications mentioned in Chapter 2 have referred to BiCMOS applications in design of memories. In fact, the static memory area has felt the maximum influence of BiCMOS to date. Superior I/O capability and sensing which are so important in memory design, account for this. Figure 4.24 shows a simplified memory access schematic. A BiCMOS NAND decoder with a 2 bit input is implemented with active devices. The output of this decoder is fed through an inverter which may be



4.22a 4 bit CMOS Carry Chain

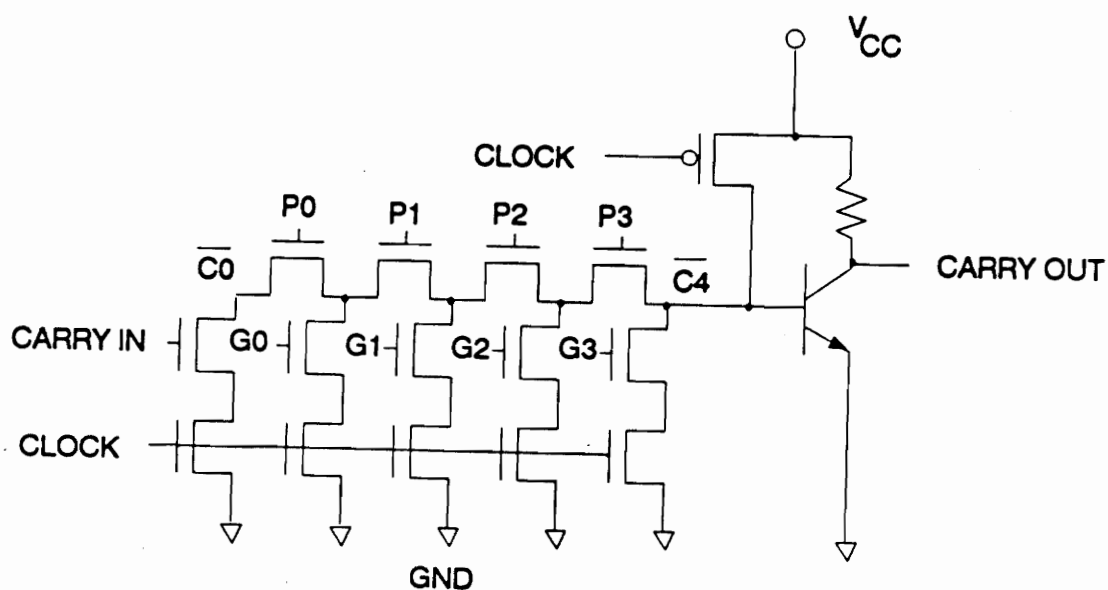


Figure 4.22b 4 bit BiCMOS Carry Chain

Figure 4.22. CMOS and BiCMOS 4-bit Carry Chain Circuits

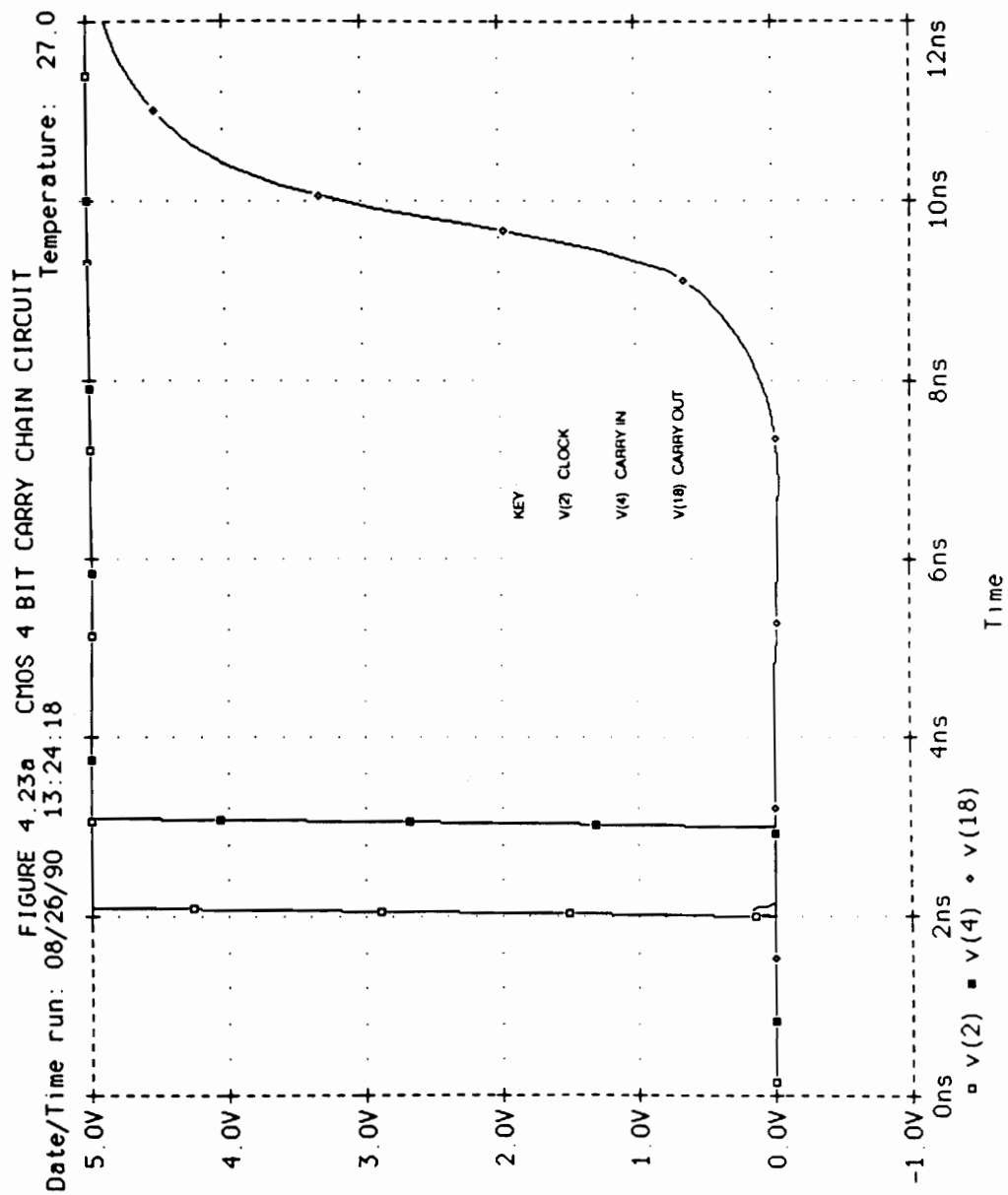


Figure 4.23a. SPICE plot for CMOS Carry Chain

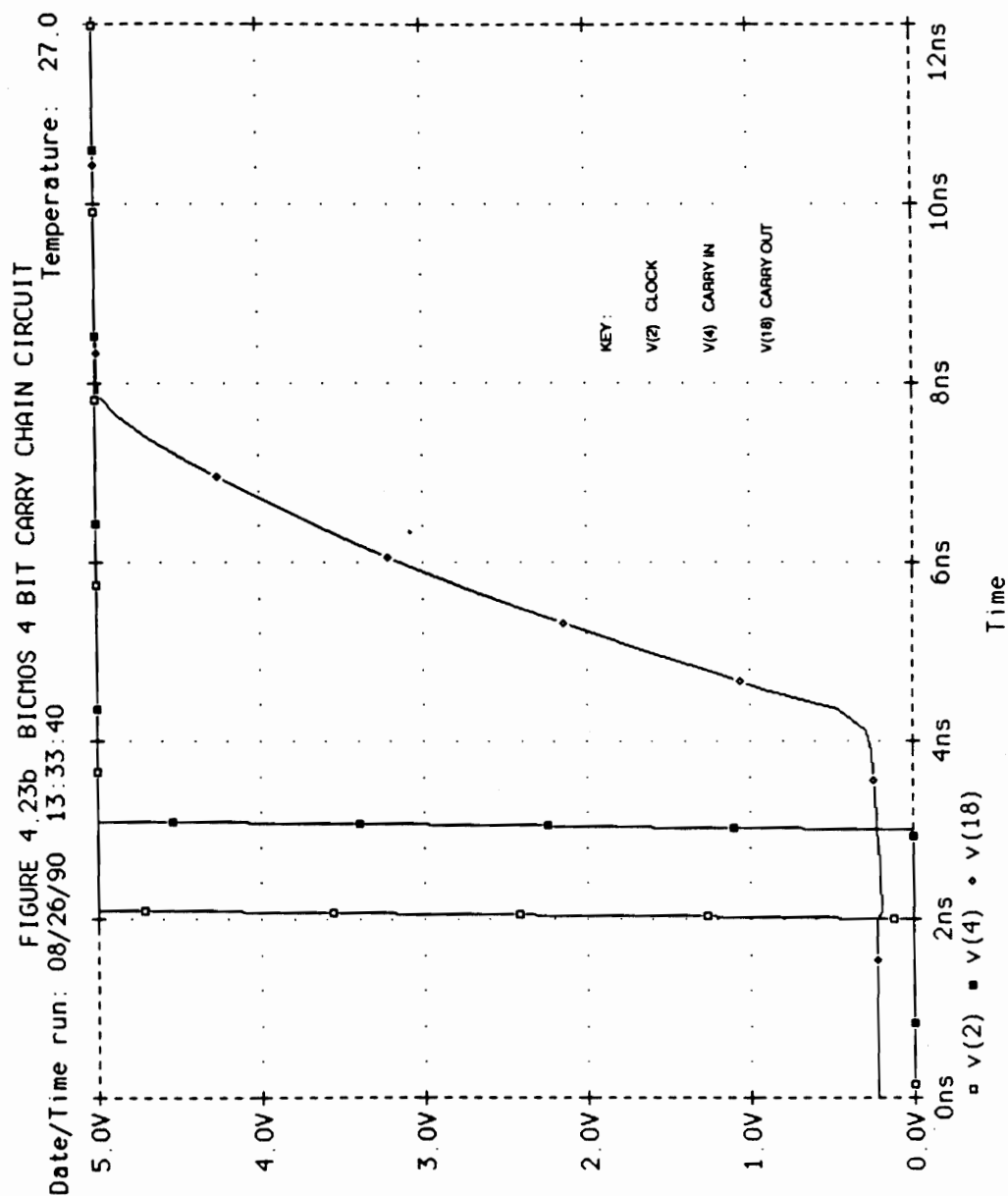


Figure 4.23b. SPICE plot for BiCMOS Carry Chain

CMOS or BiCMOS depending upon area, speed and power requirements, to the word line of the memory cell. The cell itself is the CMOS variety, which is quite typical given the levels of integration required in memories. Vertical BIT lines are also shown. We describe the operation of this when a '1' is to be written at the location represented by node 11 and a zero at node 12. Initially we assume that node 11 is at logic '0' and node 12 at logic '1'. The BIT line is precharged to '1' while BITBAR is obviously zero. After the decoder inputs change, the decoder output is available so as to assert the word line. NMOS devices M10 and M13 are turned on. The '1' on the BIT line propagates through M10 to charge node 11 while node 12 discharges through M13. This completes the write operation. Results of SPICE simulations for this operation appear in Figure 4.25. The total memory access time is 1.9ns which is fairly impressive considering given that we are using conservative 2μ dimensions. The complete SPICE deck for this simulation appears in Appendix B. Device names and node numbers are as shown in Figure 4.24 so it is instructive to consider the results in conjunction with the SPICE listing. It is important to note that device sizes have to be varied in order to achieve acceptable voltage levels.

4.7.2 Analog BiCMOS

When integrated circuits first became viable, bipolar technology dominated the analog area. With the emergence of NMOS technology, attempts were made to utilize it for analog applications, despite drawbacks such as low gain and large offset voltages. Essentially, the main difference between the two technologies is that bipolar transistors often carry signals in the form of currents while MOS devices do so in the form of

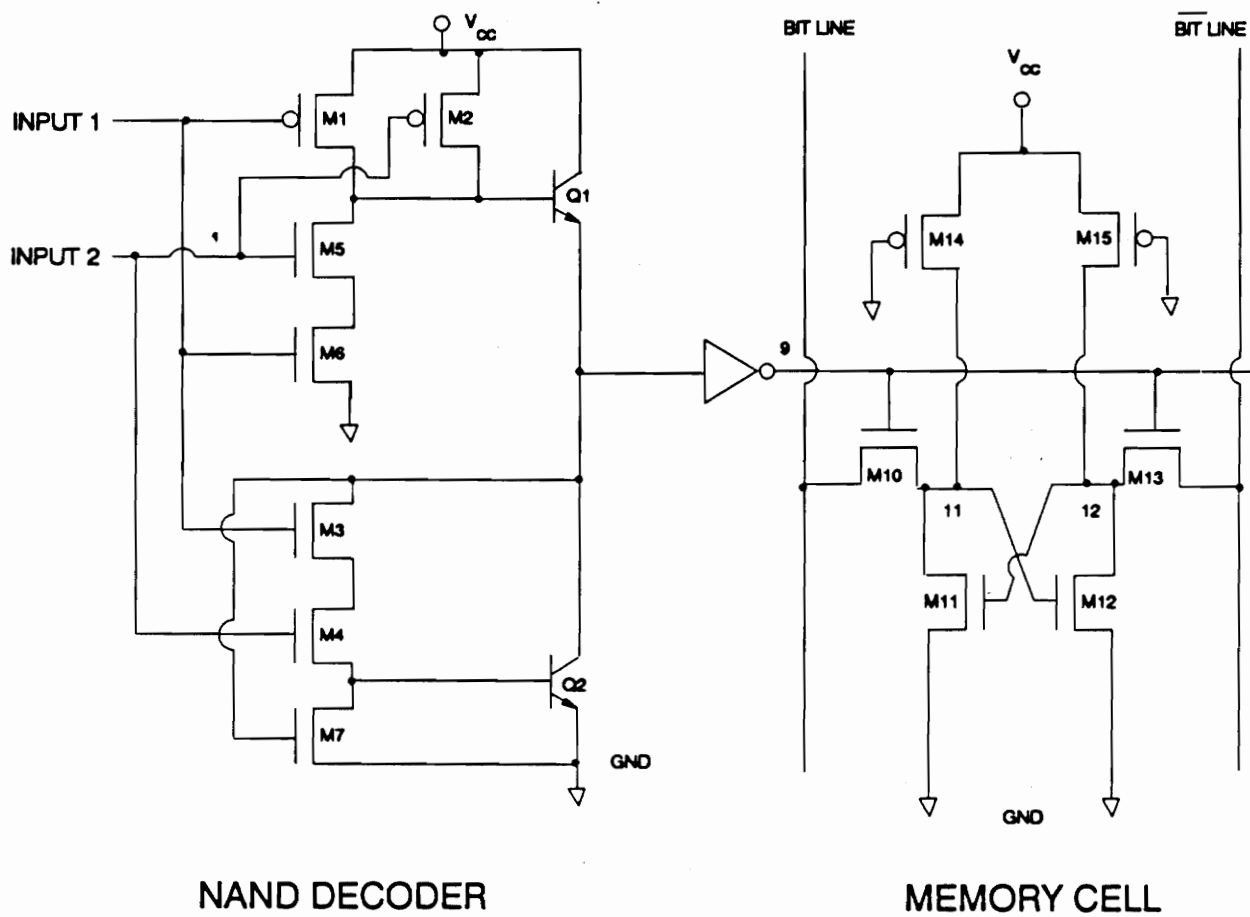


Figure 4.24. BiCMOS NAND Decoder / Memory Access Scheme

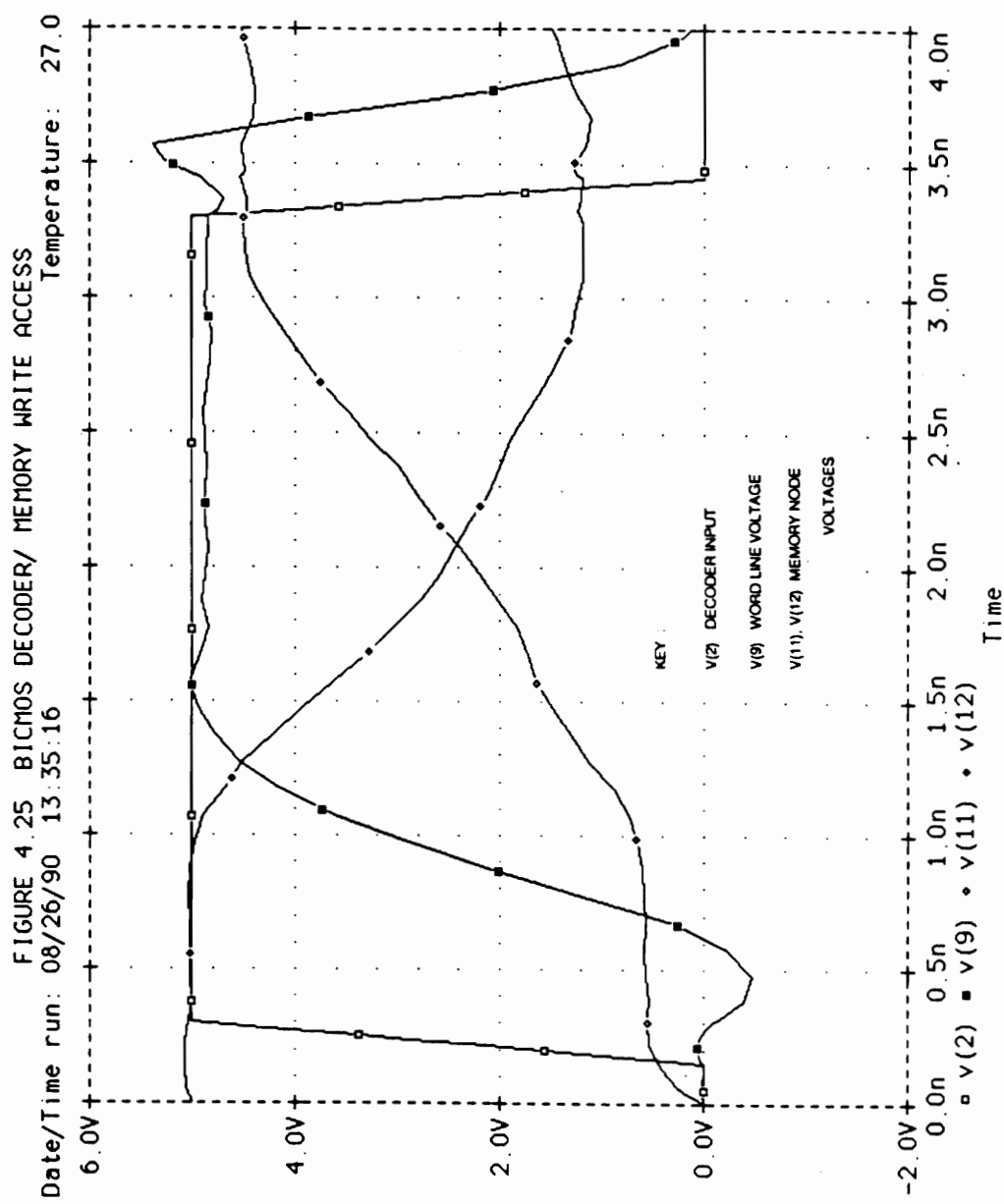


Figure 4.25. SPICE plot for BiCMOS Decoder/Memory Access Circuit

charges. Recent advances in CMOS have made high performance analog MOS circuits possible, but bipolar devices still hold the edge, given their larger transconductance. However, incompatibility with charge circuit techniques such as switched capacitor filters limits their applications. BiCMOS has the potential to bridge this gap.

One of the main difference between digital and analog VLSI circuits is the nature of the supply voltages. For digital logic, dense packaging and limits on acceptable power dissipation require low supply voltages, typically 5 volts. Analog circuits require higher voltages of 10 volts or so, for enhanced performance and dynamic range. Other requirements for analog VLSI include high breakdown voltage ratings for devices, due to higher supply voltages. One of the main performance measures in analog bipolar devices is the unity gain cutoff frequency. To make this as high as possible, a thin base and low parasitic resistances and capacitance are desirable. For the MOS devices, gate oxide thickness must be increased in order to withstand higher voltages. This indicates a tradeoff between reduced speed and extended dynamic range. Threshold voltages are important in high accuracy circuits.

The operational amplifier is one of the most common and versatile devices used in analog design. A BiCMOS opamp is shown in Figure 4.26. PMOS devices M1 and M2 constitute the differential pair at the input. They provide high input impedance and noise immunity. The principal function is of course to amplify the difference in the input voltages. Q1 and Q2 provide a current mirror load to facilitate a large voltage gain. Q3 is an emitter follower stage to avoid loading the first stage while Q4 is the final driver transistor at the output. Bipolar devices Q5-Q8 provide additional current mirror loads to maintain a steady current supply from V_{CC} .

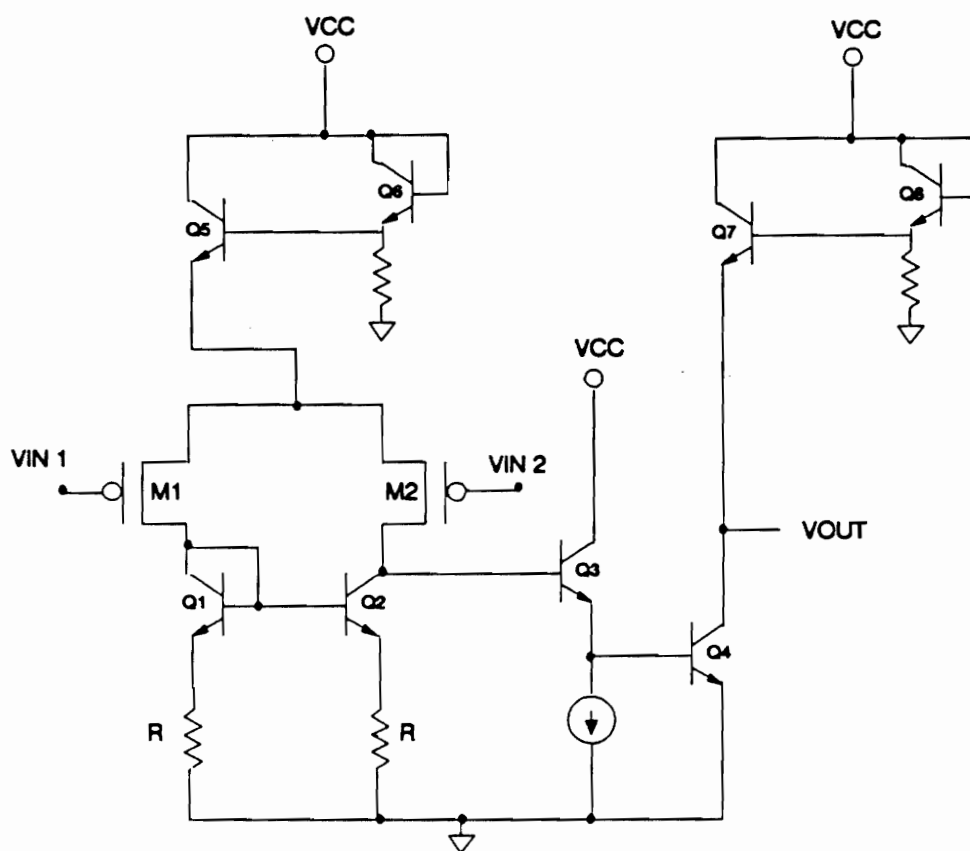


Figure 4.26. BiCMOS Operational Amplifier

4.8 *Summary*

In this chapter, a detailed study has been made regarding the influence of circuit and device parameters on BiCMOS and CMOS technologies. This has enabled us to evaluate BiCMOS in relation to CMOS, which is the dominant VLSI technology today. The study has been divided into three broad parts. The first deals with the effect of extrinsic parameters and operating conditions. Here, the impact of variables such as fanout load, temperature and supply voltage scaling has been discussed. The results clearly indicate that BiCMOS enjoys a considerable edge in terms of relative immunity to variation in such parameters. The second part of the study involves the determination of the effects of variation in MOS parameter variations. Results of mobility, threshold voltage, oxide thickness and channel length variation point towards a single conclusion - BiCMOS displays great robustness towards MOS device parameter variations.

Having clearly established an edge over CMOS in this respect, the next logical step was to test the effect of deviations in bipolar device parameters, since on more than one occasion it was demonstrated that the superior drive characteristics of the NPN device compensated for the effects of MOS parameter variations. This task has been approached in terms of the design of the emitter, collector and base regions. Device parameters and parasitics having the maximum impact on design of these regions have been detailed. The overall need for minimization of parasitics has been emphasized. However, some parasitics such as the collector capacitance and resistance have a greater impact on switching characteristics than others. Base region parameters such as transit time and forward current gain are important. Effects of bipolar device scaling have also been investigated.

Since BiCMOS process methodology utilizes proven CMOS processes as the basis, it must be remembered that the effect of bipolar and MOS device parameters must ultimately be integrated into a common design methodology. Having convincingly demonstrated the potential advantages of BiCMOS using the inverting buffer, the next part of the study goes on to show that this superiority extends into the area of multi input gates also. Practical applications of BiCMOS are demonstrated with an emphasis on the digital area. Combinational and memory logic circuit simulations have yielded impressive results. These are documented in the form of SPICE listings and plots. A brief reference has also been made to the application of BiCMOS in analog circuits.

The results contained in this chapter indicate that from a circuit and device design standpoint, the shift to BiCMOS from CMOS is a logical step in search of improved performance in VLSI circuits. However, processing complexity and associated costs are the bottlenecks that hinder such a move. The fact that BiCMOS is relatively immune to scaling considerations is evidence that BiCMOS can actually reduce costs by extending the life of present day equipment and fabrication lines. This factor may ultimately prompt a push towards this technology.

Chapter 5

Conclusions

This thesis has involved an investigation of some facets of BiCMOS technology. The principal performance measure under consideration has been device switching speed, reflected in the gate delay and output drive current levels. Two methods have been used to facilitate this study - the analytical modeling approach and the use of circuit simulation software.

The analytical approach required that a specific BiCMOS circuit be modeled. The basic BiCMOS inverting buffer was chosen because of the simplicity of its structure and the fact that it is fully representative of the technology. The analysis consisted of two main parts, one dealing with the output rise transient and the other with the fall transient [7], [28]. This allowed the development of a comprehensive set of equations for the total gate delay. Each transient was evaluated in terms of three different time regions based on the modes of operation of the individual MOS and bipolar transistors. Circuit models for all the regions have been documented and explained. Assumptions and approximations made while arriving at the final results are also clearly stated and

justified. Simple, closed form equations describing the change in output voltage and the delays for each region of operation are the final products of this analysis. These equations provide us with information about the relative importance of individual circuit and device parameters, in determining the switching response of the gate. Furthermore, the delay equations provide us with a convenient means of making first approximations of the delays involved. This helps speed up the overall circuit optimization process, by allowing the designer to make preliminary decisions regarding which parameters are most important. Comparisons with PSPICE simulations have indicated that these models are fairly accurate for the above mentioned purposes.

Evaluation of BiCMOS technology using the PSPICE circuit simulator was the other main task undertaken during this research [1]. This evaluation proceeded with CMOS technology as a performance benchmark of sorts, since BiCMOS will have to surpass CMOS to become the dominant VLSI technology. As mentioned earlier, gate delay and peak output current levels were the performance measures used for this research. The effects of variations in extrinsic, MOS and NPN device parameters were tested. BiCMOS was determined to be more resilient to changes in circuit parameters such as fanout load and temperature. Both technologies show a similar percentage wise degradation in performance due to downward supply voltage scaling, which is being put forward as a possible solution to power dissipation constraint problems. But, in absolute terms, BiCMOS continues to produce fairly high current levels compared to CMOS. As is to be expected, BiCMOS dissipates more power than CMOS due to the presence of bipolar devices. BiCMOS has demonstrated an impressive level of immunity towards variations in MOS parameters such as surface mobility, oxide thickness, threshold voltages and device scaling. The last named feature is important since it allows high BiCMOS performance at existing technology dimensions. CMOS would require an expensive shift to smaller dimensions to obtain such performance. In the context of the

relative immunity of BiCMOS to MOS process variation, it is important to note that MOS and bipolar device design cannot be viewed in isolation. Device characteristics are going to be interdependent since they are fabricated on the same wafer. Hence, an overall design methodology that takes into account both technologies will have to be adopted so that there is minimal need for compromised performance.

Since these studies clearly demonstrated that the bipolar devices have a dominant influence over BiCMOS switching response, an investigation of the effects of variation in NPN parameters was called for. It was determined that the principal bipolar parameters affecting BiCMOS inverting buffer performance are the collector resistance and parasitic capacitance, the forward base transit time and the forward current gain factor. Ways of achieving optimal values of these and other parameters have been discussed. Performance evaluation of multi input BiCMOS gates and practical VLSI applications have confirmed its superiority over CMOS in the domain of high speed circuits.

To sum up this research, it can be stated that a good understanding has been achieved regarding the issues involved in designing with BiCMOS. From a circuit and device design viewpoint, there is great incentive to adopt this technology for VLSI applications. Processing time and costs are the bottlenecks that need to be surmounted. There is plenty of scope for further research in this area, improving upon circuit and process design techniques that will facilitate integrated bipolar and MOS design with minimum performance compromises.

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Appendix A

Modeling Analysis Clarifications

A.1 s-domain derivation

From figure 3.4b, we can write for the voltage at node B':

$$V_{B'} = \frac{I_{dsat}}{s} \frac{\left(\frac{1}{C_E s}\right)^2}{\frac{1}{C_E s} + \frac{1}{C_C s} + R_C}$$

We separate the $\frac{I_{dsat}}{C_E}$ term from the right hand side and factor the remaining terms as follows :

$$\frac{1}{s^2(sR_C + [\frac{C_E + C_C}{C_E C_C}])} = \frac{K1}{s} + \frac{K2}{s^2} + \frac{K3}{sR_C + [\frac{C_E + C_C}{C_E C_C}]} \quad (A1)$$

Multiplying both sides of (A1) by the K3 term denominator and setting $s = -\frac{(C_E + C_C)}{R_C C_C C_E}$ we can solve for K3 to obtain

$$K3 = \frac{R_C^2}{[\frac{C_E + C_C}{C_C C_E}]^2}$$

Multiplying both sides of (A1) by s^2 and setting $s=0$ we have

$$K2 = \frac{1}{[\frac{C_E + C_C}{C_C C_E}]}$$

Multiplying (A1) by s^2 and differentiating both sides with respect to s , we simplify for K1 :

$$K1 = -\frac{R_C}{[\frac{C_E + C_C}{C_C C_E}]^2}$$

Substituting expressions for K1, K2 and K3 into (A1), multiplying by $\frac{I_{dset}}{C_E^2}$ and taking the inverse Laplace transform, we have for the voltage across B' :

$$V_{B'} = \frac{I_{dsat}t}{C_E + C_C} + I_{dsat}R_C \left(\frac{C_C}{C_E + C_C} \right)^2 [1 - \exp(\frac{-t}{\tau})]$$

where

$$\tau = \frac{R_C C_E C_C}{C_C + C_E}$$

Hence, we have have derived a final expression for the drop across $V_{B'}$.

A.2 Taylor's series simplification

From Chapter 3, we have for equation (3.13) :

$$V_{out}(t') = \frac{\beta^* I_{dsat}}{C_{CS} + C_L} \{t' - \beta^* \tau^* (1 - \exp(\frac{-t'}{\beta^* \tau^*}))\} \quad (A2)$$

Since $t' \ll \beta^* \tau^*$ we expand the exponential term in a Taylor's series and retain only terms up to the second power of t' to obtain at $t' = t_2 - t_1$:

$$|V_T| - V_{BE(on)} = \frac{\beta^* I_{dsat}}{C_{CS} + C_L} \{t' - \beta^* \tau^* (1 - (1 - \frac{t'}{\beta^* \tau^*}) + (\frac{t'}{\beta^* \tau^*})^2)\}$$

On simplification of the above expression we are left we are left with an equation with r'^2 . Taking the positive square root we have

$$r' = \sqrt{(C_L + C_{CS})(|V_T| - V_{BE(on)}) \frac{\tau^*}{I_{dsat}}}$$

which is the same as equation (3.14) in Chapter 3.

A.3 Effect of incorporating simulation results into analytical equations

From Chapter 3 we note that in the collector saturation region, the output voltage is of the form,

$$V_{out} = [\text{constants and time dependent variables}] + K(V_{BE(on)})$$

where K is a constant. Using simulation or experimental results, we could try and fit an exponential curve to the V_{out} v/s I_C curve, where I_C is the collector current, to get

$$I_C = K1 \exp(K2 V_{out})$$

where K1 and K2 are constants. Since

$$I_C = I_s \exp\left(\frac{qV_{BE}}{kT}\right)$$

We take the natural log on both sides of the above equation and substitute the resulting expression for V_{BE} into A3 to obtain

$$V_{out} = \frac{1}{(1 - K2)} [\text{constants and time dependent variables}] + K\left(\frac{kT}{q}\right) [\ln(K1) - \ln(I_s)]$$

Hence, we have a closed form expression for V_{out} which takes into account, the variation in V_{BE} . Unfortunately, it has been observed from simulation data that the exponential fit to the I_C v/s V_{out} curve is not accurate. The simplest accurate fit is a second degree polynomial. Then, if I_C is of the form,

$$I_C = C_1 + C_2 V_{out} + C_3 V_{out}^2$$

where all the C's are constants, then the equation for V_{BE} would look like

$$V_{BE} = \frac{kT}{q} [\ln(C_1 + C_2 V_{out} + C_3 V_{out}^2) - \ln(I_s)]$$

Using this equation in A3 would make it impossible for a closed form solution for V_{out} to be obtained.

Appendix B

PSPICE listings

NOTE : IN THE FOLLOWING LISTINGS THE '*' SYMBOL PRECEDING THE LINES BEGINNING WITH A '.' SHOULD BE DISREGARDED. THESE HAVE BEEN INSERTED TO ALLOW CORRECT PRINTING OF THE LISTING. IF INCLUDED, THE SPICE SIMULATOR WILL TREAT THESE STATEMENTS AS COMMENTS AND NOT EVALUATE THEM. EXPLANATORY COMMENTS ARE APPENDED AFTER RELEVANT STATEMENTS.

CMOS 4 BIT CARRY CHAIN CIRCUIT	- CIRCUIT NAME
VDD 1 0 DC 5	- SUPPLY VOLTAGE
VCLK 2 0 PULSE(0 5 2NS 0.1NS 0.1NS 10NS 20NS)	- CLOCK INPUT
VCIN 4 0 PULSE(0 5 3NS 0.1NS 0.1NS 12NS 20NS)	- CARRY IN
VG0 7 0 DC 0	- GENERATE SIGNALS
VG1 10 0 DC 0	

VG2 13 0 DC 0

VG3 16 0 DC 0

VP0 19 0 DC 5

- PROPAGATE SIGNALS

VP1 20 0 DC 5

VP2 21 0 DC 5

VP3 22 0 DC 5

M1 3 2 1 1 PMOD

- PMOS DEVICES

M2 6 2 1 1 PMOD

M3 9 2 1 1 PMOD

M4 12 2 1 1 PMOD

M5 15 2 1 1 PMOD

M6 3 19 6 0 NMOD

- NMOS DEVICES

M7 6 20 9 0 NMOD

M8 9 21 12 0 NMOD

M9 12 22 15 0 NMOD

M10 3 4 5 0 NMOD

M11 6 7 8 0 NMOD

M12 9 10 11 0 NMOD

M13 12 13 14 0 NMOD

M14 15 16 17 0 NMOD

M15 5 2 0 0 NMOD

M16 8 2 0 0 NMOD

M17 11 2 0 0 NMOD

M18 14 2 0 0 NMOD

M19 17 2 0 0 NMOD

M20 18 15 1 1 PMOD W=30U L=2U

M21 18 15 0 0 NMOD W=30U L=2U

*.TRAN 0.1NS 12NS

*.PROBE

*.MODEL NMOD NMOS LEVEL=1 W=10U L=2U TOX=0.04U GAMMA=0.8965
UO=350 - MODEL SPECIFICATIONS

+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ RSH=80.020 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

*.MODEL PMOD PMOS LEVEL=1 W=15U L=2U TOX=0.04U GAMMA=0.5343
UO=180

+ NSUB=2.45E+16 VTO=-1 DELTA=0.85411 VMAX=100000 PHI=0.659
+ XJ=0.50000U NFS=7.116689E+11 NEFF=1.001 NSS=1.000000E+12 TPG=1.000000
+ RSH=240.040 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=0.99E-09
+ CJ=1.511000E-04 MJ=0.503200 CJSW=8.000E-10 MJSW=0.3300 PB=0.89

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UO=350

+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
RD=300 RS=300

+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

*.MODEL MODN NPN BF=90 RB=50 + RE=10 RC=20 CJE=40E-15 CJC=33E-15
+ IS=1E-16A NF=1 NE=1.5 BR=1 NR=1 NC=2 VJE=0.75V MJE=0.33 VJC=0.75V
MJC=0.33

+ IKF=7E-03A VAF=10V TF=40PS TR=800PS

*.END

BICMOS 4 BIT CARRY CHAIN CIRCUIT

```

VDD 1 0 DC 5
VCLK 2 0 PULSE(0 5 2NS 0.1NS 0.1NS 10NS 20NS)
VCIN 4 0 PULSE(0 5 3NS 0.1NS 0.1NS 12NS 20NS)
VG1 7 0 DC 0
VG2 10 0 DC 0
VG3 13 0 DC 0
VG4 16 0 DC 0
VP1 19 0 DC 5
VP2 20 0 DC 5
VP3 21 0 DC 5
VP4 22 0 DC 5
M5 15 2 1 1 PMOD W=30U L=2U
M6 3 19 6 0 NMOD
M7 6 20 9 0 NMOD
M8 9 21 12 0 NMOD
M9 12 22 15 0 NMOD
M10 3 4 5 0 NMOD
M11 6 7 8 0 NMOD
M12 9 10 11 0 NMOD
M13 12 13 14 0 NMOD
M14 15 16 17 0 NMOD
M15 5 2 0 0 NMOD
M16 8 2 0 0 NMOD
M17 11 2 0 0 NMOD
M18 14 2 0 0 NMOD
M19 17 2 0 0 NMOD
Q1 18 15 0 MODN - BIPOLAR TRANSISTOR
R1 1 18 1K - RESISTOR

```

```

*.TRAN 0.1NS 12NS

*.PROBE

*.MODEL NMOD NMOS LEVEL=1 W=10U L=2U TOX=0.04U GAMMA=0.8965
UO=350
+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ RSH=80.020 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

*.MODEL PMOD PMOS LEVEL=1 W=15U L=2U TOX=0.04U GAMMA=0.5343
UO=180
+ NSUB=2.45E+16 VTO=-1 DELTA=0.85411 VMAX=100000 PHI=0.659
+ XJ=0.50000U NFS=7.116689E+11 NEFF=1.001 NSS=1.000000E+12 TPG=1.000000
+ RSH=240.040 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=0.99E-09
+ CJ=1.511000E-04 MJ=0.503200 CJSW=8.000E-10 MJSW=0.3300 PB=0.89

*.MODEL NMOD1 NMOS LEVEL=1 W=10U L=2U TOX=0.04U GAMMA=0.8965
UO=350
+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
RD=300 RS=300
+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

*.MODEL MODN NPN BF=90 RB=50 + RE=10 RC=20 CJE=40E-15 CJC=33E-15
+ IS=1E-16A NF=1 NE=1.5 BR=1 NR=1 NC=2 VJE=0.75V MJE=0.33 VJC=0.75V
MJC=0.33
+ IKF=7E-03A VAF=10V TF=40PS TR=800PS

*.END

```

BICMOS DECODER/ MEMORY WRITE ACCESS

VDD 1 0 DC 5

V1 2 0 PULSE(0 5 150PS 150PS 150PS 3NS 6NS)

V2 3 0 PULSE(0 5 150PS 150PS 150PS 3NS 6NS)

VBIT 10 0 DC 5

VBITBAR 13 0 DC 0

M1 4 2 1 1 PMOD W=30U L=2U

M2 4 3 1 1 PMOD W=30U L=2U

M5 4 2 5 0 NMOD W=6U L=2U

M6 5 3 0 0 NMOD W=6U L=2U

M3 6 2 7 0 NMOD W=30U L=2U

M4 7 3 8 0 NMOD W=30U L=2U

M7 8 6 0 0 NMOD W=6U L=2U

Q1 1 4 6 MODN

Q2 6 8 0 MODN

M8 9 6 1 1 PMOD W=15U L=2U

M9 9 6 0 0 NMOD W=15U L=2U

M10 10 9 11 0 NMOD W=10.5U L=2U

M11 11 12 0 0 NMOD W=9U L=2U

M12 12 11 0 0 NMOD W=3U L=2U

M13 13 9 12 0 NMOD W=3U L=2U

M14 11 0 1 1 PMOD W=4.5U L=2U

M15 12 0 1 1 PMOD W=4.5U L=2U

C11 11 0 30FF

C12 12 0 30FF

*.IC V(11)=0 V(12)=5

*.TRAN 60PS 5NS

```

*.OPTIONS  ITL1=1000  ITL2=1000  TRTOL=2000  ITL4=1000  RELTOL=0.1
ABSTOL=1mA + VNTOL=10mV ITL5=10000

*.PROBE

*.MODEL NMOD NMOS LEVEL=1 W=10U L=2U TOX=0.04U GAMMA=0.8965
UO=350
+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ RSH=80.020 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

*.MODEL PMOD PMOS LEVEL=1 W=15U L=2U TOX=0.04U GAMMA=0.5343
UO=180
+ NSUB=2.45E+16 VTO=-1 DELTA=0.85411 VMAX=100000 PHI=0.659
+ XJ=0.50000U NFS=7.116689E+11 NEFF=1.001 NSS=1.000000E+12 TPG=1.000000
+ RSH=240.040 CGDO=4.93E-10 CGSO=4.93E-10 CGBO=0.99E-09
+ CJ=1.511000E-04 MJ=0.503200 CJSW=8.000E-10 MJSW=0.3300 PB=0.89

*.MODEL NMOD1 NMOS LEVEL=1 W=10U L=2U TOX=0.04U GAMMA=0.8965
UO=350
+ NSUB=2.74E+16 VTO=1 DELTA=0.848 VMAX=80500.6 + PHI=0.659 XJ=0.50000U
RD=300 RS=300
+ NFS=2.372753E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ CGDO=4.93E-10 CGSO=4.93E-10 CGBO=9.9E-10
+ CJ=2.300E-04 MJ=0.544600 CJSW=9.0000E-10 MJSW=0.33900 PB=0.89

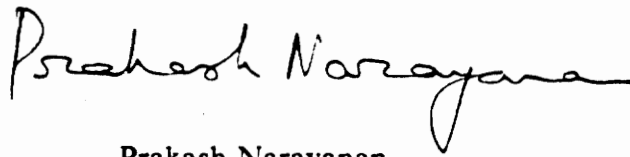
*.MODEL MODN NPN BF=90 RB=50 + RE=10 RC=20 CJE=40E-15 CJC=33E-15
+ IS=1E-16A NF=1 NE=1.5 BR=1 NR=1 NC=2 VJE=0.75V MJE=0.33 VJC=0.75V
MJC=0.33
+ IKF=7E-03A VAF=10V TF=40PS TR=800PS

*.END

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Vita

Prakash Narayanan was born on 23 October, 1965 in Chittur, India. He received his Bachelor of Engineering (Honors) degree in Electrical and Electronics Engineering from Birla Institute of Technology and Science, Pilani, India in July 1988. He enrolled at Virginia Polytechnic Institute and State University in August 1988 and completed the Master of Science program in Electrical Engineering, in September 1990. Prakash will be pursuing his professional interests at Intel Corporation, Santa Clara, California.

A handwritten signature in black ink, reading "Prakash Narayanan". The signature is fluid and cursive, with the first name "Prakash" and last name "Narayanan" clearly distinguishable.

Prakash Narayanan

9 September 1990.