# A Manufacturing Process for Single Micron Resolution Optical Gratings used in X-ray Computed Tomography

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# Abstract

X-ray Computed Tomography (CT) is a process that produces three-dimensional x-ray images, allowing for better diagnosis and analysis of complex internal medical conditions. New advances in the optical techniques used in this process promise to produce better results while reducing patient risk. One of these developments calls for precise optical gratings that can be expensive and difficult to manufacture. This paper presents a simple process developed specifically for the production of these gratings using cost effective techniques. The process uses well understood semiconductor fabrication steps including oxidation, deep reactive ion etching and electroplating. While not entirely successful, the process presented within provides a proof of concept for development of the gratings and discusses improvements that could be made to allow for success.

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# I. Introduction

X-ray Computed Tomography (CT) is a technique that allows for three-dimensional analysis of x-ray images. The method involves collecting a series of two-dimensional x-ray images taken around a single axis of rotation. These images are then combined, using software, to build a visual model of the area under observation. X-ray CT has distinct advantages over traditional two-dimensional x-ray techniques and may be used in a variety of scientific fields. As a radiological procedure, CT is non-invasive and has a number of applications including finding tumors and blood clots, assessing bone damage, and detecting inflammation and abnormalities. There were approximately 62 million x-ray CT scans performed in the United States in 2007 [1]. However, current x-ray CT practices produce a heavy dose of radiation and do not offer enough image contrast for applications in which soft tissue is being examined [1-3]. In a typical CT system, higher image resolution or contrast can be obtained by collecting more low-noise images over a longer period of time, which leads to increased radiation exposure [1]. While these negative side effects may be neglected for serious situations, such as scans that are performed to collect data for preventative health maintenance, they are undesirable for routine scans. These issues, exacerbated when scanning soft tissue, make research on improvements to x-ray CT very important to the field of radiology.

Drawbacks of CT may be partially attributed to the contrast generation method of attenuation currently used by x-ray CT devices. Attenuation is not a strong form of contrast generation when scanning poorly absorbing soft tissue [2]. In order to obtain sufficient results using attenuation on such tissue, the radiation dosage must be quite

large. X-ray CT equipment exploiting attenuation do allow for acceptable image resolution as low as 10 microns, but these machines still require a large dosage of radiation in order to produce acceptable contrast [3]. Thus, current research in the field of x-ray CT has sought to replace the attenuation technique.

A promising x-ray imaging method known as x-ray phase-contrast imaging combats the issues introduced by using attenuation. Grating-based phase-contrast x-ray interferometry is a diffraction based technique that exploits x-ray refraction rather than absorption. There are two distinct advantages to using a diffraction based technique. First, soft tissue causes much greater refraction than absorption of x-rays, making refraction more detectable. X-ray absorption caused by an element is roughly proportional to the fourth power of the element's atomic number Z [2, 3]. Therefore, materials composed of low-Z elements are weak absorbers of x-rays. Soft tissues and other organic materials consist of these low-Z elements. This property means it is difficult to resolve small differences in composition of soft tissue using attenuation techniques [2]. Conversely, x-ray phase shift is shown in [2] to have an interactive cross-section three orders of magnitude greater than that of absorption for soft tissue analyzed between 17keV and 60keV [2]. Equations (1) and (2) define optical density (D) and phase shift (Φ) of x-rays traveling along the z-axis of a medium [2].

$$(1) \qquad D(x,y) = \int \sum_k N_k(x,y,z)\mu_k^a dz$$

$$(2) \qquad \phi(x,y) = \int \sum_k N_k(x,y,z)p_k dz$$

$N_k(x,y,z)$ is the atomic density of the medium while $\mu_k{}^a$ is the absorption cross section and $p_k$ is the phase shift cross section. Both equations define a direct

proportionality between interactive cross section and their respective optical effects. Therefore, because the phase shift cross section is 1000 times greater than the absorption cross section, x-rays are 1000 times more sensitive to refraction than absorption. This increased sensitivity means diffraction based contrast generation can produce contrast at 1000 times that of absorption based contrast generation [2, 3]. In addition, it has been shown that, at higher x-ray energies, soft tissue will absorb x-rays less than at lower energies [2]. Conversely, an increase in x-ray energy has very little impact on x-ray phase-shift when passing through any medium [2]. Because x-ray absorption is directly related to patient radiation dose, higher energy x-rays may be used to reduce patient radiation exposure while maintaining high image contrast when utilizing x-ray phase shift. Unfortunately, diffraction based techniques require longer exposure times which lead to greater patient radiation exposure, a problem still being analyzed in current research [4, 5]. If this issue is solved, grating-based phase-contrast x-ray interferometry will increases image contrast while potentially reducing radiation exposure.

Grating-based phase-contrast x-ray interferometry uses three optical gratings placed at specific points in the x-ray CT device. The gratings act as an x-ray Talbot interferometer. The structure uses a source grating (G0), a phase grating (G1) and an analyzer grating (G2). In the interferometer, x-rays first pass through G0, which transforms the source x-rays into individually coherent line sources. These x-rays then travel through the material being analyzed and undergo refraction based on the phase shift in the medium. This phase shift may then be analyzed using phase-modulation techniques that transform the phase shift into an intensity pattern by using G1 and G2 to exploit the Talbot effect [5, 6]. For this study, the design specification for the gratings are

such that each have a metallic structure with a thickness of 100 microns, but vary in periodicity. The depth (d) of the grating, the 100 microns, was selected based upon the penetration depth of x-rays in lead (Pb) [7]. Equation (3) defines the intensity of an x-ray beam (I) passing through a material based on initial intensity ($I_o$), mass attenuation coefficient ($\mu/\rho$), and the depth of the material through which the beam travels (l).

$$I = I_0 e^{-(\mu/\rho)\rho l} \tag{3}$$

Using the attenuation coefficient of 30.32cm$^2$/g provided by [7], and a lead density of 11.35g/cm$^3$, equation (3) shows that 100μm of Pb will sufficiently reduce the x-ray intensity to approximately three percent of its initial value. The slits for the grating with the shortest period, G2, are on the order of 1 micron. This extremely high aspect ratio of the depth to width, 100:1, has had a drastic effect on process development.

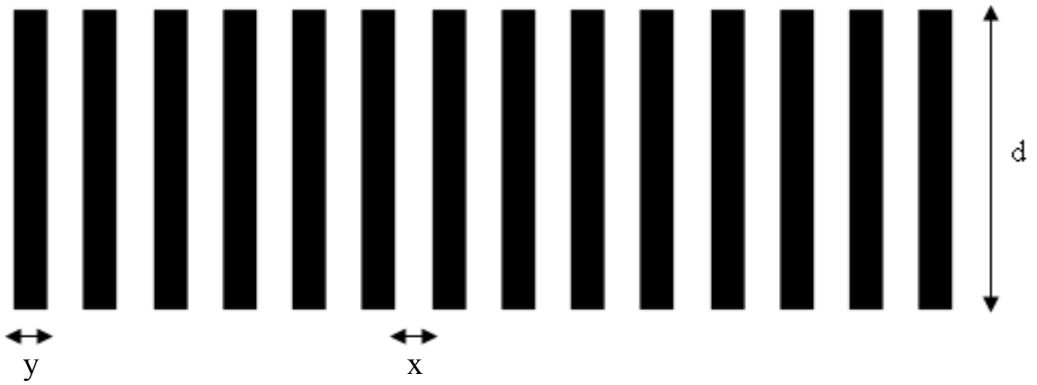


**Figure 1: Basic cross-section of grating structure illustrating depth (d) and periodicity with slits of width (x) separated by distance (y)**

The unique dimensions of these gratings make them difficult to manufacture. It has been shown that similar grating structures can be produced using a combination of photolithography and electroplating techniques [8]. The procedure involves the formation of a grating mold using photoresist on the surface of a silicon wafer.

Electroplating is then used to fill the mold, forming the metallic grating structure. However, this processing procedure is used to fabricate gratings with depth of only 30μm, which will only reduce the x-ray intensity to 36% of its initial value, according to (3). Photoresist available in the Virginia Tech Micron Technology Semiconductor Processing Laboratory (SPL), such as AZ9260, can be spun to a thickness of 30μm using layering techniques. However, this value is significantly less than the 100μm required by this study; a depth to which photoresist in the SPL cannot be properly spun, exposed and developed. Successful development of a different process used to produce the deep gratings needed in this study will lead to advances in phase-contrast x-ray interferometry research.

My research has focused on the development of an efficient and cost effective method of manufacturing thick gratings for use in x-ray CT employing phase contrast imaging. Development of the optical gratings for this project is performed using numerous semiconductor processing techniques. These methods include oxidation, photolithography, (deep) reactive ion etching, and electroplating. The gratings are made by constructing a mold using a silicon wafer covered in a layer of silicon dioxide. The mold is a series of deep trenches that form the periodic grating structure. Creating the mold involves a number of sensitive process steps that include proximity photolithography using a thick layer of high contrast photoresist, opening of the etch mask, and deep reactive ion etching of the trenches. Etching into the wafer rather than creating the mold on the surface of the wafer using photoresist allows for much deeper trenches to be formed. This increase in depth translates to an increase in grating thickness. The wafer mold is filled by an electroplating process that can be done using

one of several metals. The choice of the metal used in the electroplating process is dictated by the metal's attenuation and absorption of x-rays. Table 1 shows the x-ray mass attenuation coefficients at 30keV x-ray energy for metals that could be used to form the grating. The value for Si is also included because the mold is formed in a silicon substrate. All values were obtained from [9].

| Material | X-ray attenuation coef. at 30keV ($cm^2/g$) |
|---|---|
| Pb | 30.32 |
| Au | 27.25 |
| In | 39.49 |
| Si | 1.436 |

**Table 1: X-ray mass attenuation coefficients of various materials used in final study**

During the electroplating process, the oxide layer prevents the surface from plating, which keeps the grating structure intact. The filled mold may be used immediately because Si is effectively transparent in the x-ray spectrum [8, 9]. The process I have developed also has potential uses in other applications, specifically the cooling of certain power electronics devices.

The development of a reliable process used to produce these optical gratings was difficult due to their unique dimensions. The small feature size relative to trench depth requires high resolution lithography with photoresist that can withstand the mechanical and chemical attack during the deep reactive ion etching process. Small feature size often translates to the use of a thin photoresist layer. However, many of the available thin resists will be eroded during the deep reactive ion etching, a process that must be used to obtain the vertical sidewalls with limited lateral etching that are required for the grating structures. The relationship between feature size and depth also leads to issues in the

electroplating process including the inability to uniformly plate each trench using a stagnant plating solution. Thus, the highly anisotropic dimensions make the development of an acceptably uniform grating very difficult. Much of my research focused on finding solutions to these specific problems. The development of my final process and the characterized results are presented in the following sections.

# II. Experimental Procedure

Materials

An n-type silicon wafer with resistivity less than 0.03ohm-cm and diameter equal to 4 inches is used throughout the process. The wafer's low resistivity allows for successful electroplating, which depends on conduction through the wafer. Low resistivity also promotes uniform current flow across the wafer instead of centering at the point of the current feed. These desirable properties of n-type low resistivity wafers are shown in [10]. The wafer is approximately 500μm thick. According to equation (3) and the mass attenuation coefficient in Table 1, this thickness will have a negligible impact on x-ray intensity.

AZ9260 photoresist is used for all lithography and masking steps in the process. The AZ9200 series provides high resolution photoresists that have proven successful in deep reactive ion etching in testing in the Virginia Tech clean room [11]. Reasons for using this photoresist are covered during discussion of process development.

A 100% lead electroplating solution manufactured by Transene Company, Inc. is used to form the metallic grating structure. The solution contains fluoboric acid and metal fluoborate and requires 6V plating voltage at room temperature.

Equipment

All equipment that is used in this process is available at the Virginia Tech Micron Technology Semiconductor Processing Laboratory (SPL), which is a class 1000 clean room. Basic equipment in the SPL includes an oxidation furnace, hot plates, a

photoresist spinner and a DC power supply. Advanced equipment is also used for more complex steps of the process.

A Karl Suss MA-6 is used for photoresist exposure. The machine offers two-channel exposure with intensity of approximately 10mW/cm$^2$ for channel 2, which is used in this process. The exposure wavelength is 365nm (i-line). This value will have an impact on the minimum grating feature size that can be fabricated in the SPL. Fresnel diffraction theory can be used to approximate the minimum resolvable feature size given certain exposure conditions. Fresnel diffraction theory defines the relationship between exposure source wavelength (λ), mask to wafer alignment gap (g), and mask feature size (W) in equations (4) and (5) [12].

$$\lambda < g < \frac{W^2}{\lambda} \tag{4}$$

$$W_{\min} \approx \sqrt{\lambda g} \tag{5}$$

The minimum feature size used in this study is 1μm. This value, according to (5), will require an alignment gap of no more than approximately 2.7μm for proper resolution. This distance can be achieved using the MA-6. Smaller feature size can be obtained using soft or hard contact exposure.

An Alcatel AMS 100 deep reactive ion etcher is used for trench etching. The equipment offers Si and $SiO_2$ etching capability. The silicon etch is performed at 1800W and $4.5*10^{-2}$mbar using $SF_6$ at 300sccm. The $SF_6$ flow alternates with $C_4F_8$ passivation at 150sccm to protect the sidewalls and promote anisotropic etching. This recipe produces a Silicon etch rate of approximately 4μm/min.

A Samco RIE-1C reactive ion etching system and a Trion loadlocked RIE were used during experimentation and development of process steps. The Samco etches $SiO_2$ using $CF_4$ at flow rate of 10sccm. The etch chamber is held at 20°C and approximately 100mT. The RF power may be varied and was experimentally tested between 25W and 100W. The Samco may also be used to remove photoresist by replacing $CF_4$ with $O_2$ and using the same flow rate, temperature, pressure, and RF power settings as the $SiO_2$ etch.. The Trion RIE etches Si using $SF_6$ with flow rate of 30sccm. The etch chamber is held at 20°C and 150mT and the etch is performed using 200W RF power. Neither machine is used in the final process.

Overview of Final Process Flow

The final process flow is as follows, with each portion discussed in greater detail below, including purpose, sub steps and development:

1) Perform wafer cleaning and native oxide removal

2) Grow 500 nm $SiO_2$ layer using a sequence of dry, wet, and dry oxidation

3) Spin 10 μm of AZ9260 photoresist, expose and develop with grating pattern

4) Etch exposed $SiO_2$ down to Si surface using either a buffered oxide etch (BOE), reactive ion etching (RIE), or deep reactive ion etching (DRIE)

5) Etch exposed Si to a depth of 100μm using DRIE

6) Strip photoresist in acetone bath

7) Fill trenches with Pb using an electroplating process at 800mA at a deposition rate of 1μm/min

Step-by-Step Processing Procedure

Figure 2 presents a simplified illustration of the final process steps. (a) is a representation of the cross-section of the wafer prior to exposure at Step 3 of the process; the silicon wafer is shown in gray, coated with the 500nm thick-$SiO_2$ layer in green (not to scale) and the 10μm thick layer of AZ9260 photoresist (pink). In (b), the photoresist has been exposed and developed and the $SiO_2$ has been etched to expose the wafer surface (completion of Step 4). In (c), the silicon wafer has undergone deep reactive ion etching and the final grating mold has been formed (Step 5). In (d), the photoresist has been stripped and the trenches have been filled with Pb (blue) using electroplating, which completes the process (Step 7).

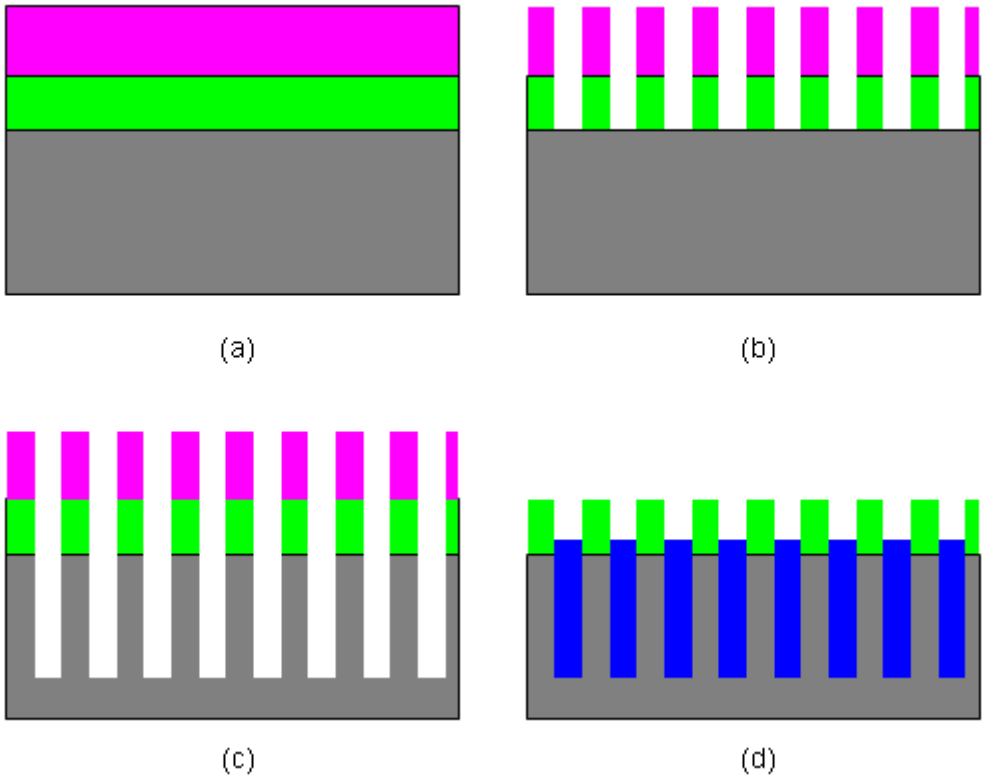


**Figure 2: A simplified illustration of the final process steps**

The wafer is first prepared using a basic acetone/isopropanol alcohol/water clean followed by a native oxide etch in a solution of 10:1 BOE for 30 seconds. Immediately following these steps, a layer of $SiO_2$ is grown using thermal oxidation. This oxide is, ideally, 500nm thick. To obtain this thickness, a wet oxidation time of 56 minutes at 1050°C with 5 minutes of dry oxidation at the beginning and end of the process is performed. Oxide thickness can be measured in the SPL using a Filmetrics F20 film thickness measurement system. The presented process consistently produced oxide thicknesses less than, but within 10% of, 500nm. The oxide has been included into the process flow to solve a problem introduced by using electroplating to form the metal grating. The trenches that will be etched into the surface of the wafer form a mold of the metal grating and the separation between trenches will become the open apertures of the grating. However, there will be bare silicon at the surface between the trenches if an oxide layer is not present. The Si surface will conduct during electroplating and metal will grow between the trenches, destroying the periodic structure of the grating. The oxide is included to act as an insulator during the electroplating process so that plating stops at the top silicon surface and the slits remain intact.

An initial process design sought to use the layer of photoresist used in the Si etch step as the insulator during electroplating. However a $C_4F_8$ polymer passivation layer is deposited on the sidewalls of the wafer during the DRIE etch step. This polymer prevents the deposition of Pb on to the etched Si sidewalls during electroplating and, therefore, must be removed. Typically acetone is used to remove this layer, but the acetone will also strip the photoresist from the wafer. Therefore, without a more

selective polymer removal method, the photoresist layer cannot be used as both a mask in the DRIE process and as an insulator during the electroplating process.

Following successful oxidation, the wafer must be prepared for etching of the $SiO_2$ and the Si. The grating dimensions lead to numerous complications during development of this step. The $SiO_2$ cannot undergo standard wet etching due to the isotropic nature of this etch type. With a depth of 500nm and feature size of 1μm, the grating structure would not be maintained due to over etching and lateral undercut. RIE is less isotropic and was extensively tested. However, RIE lead to the destruction of all tested photoresists and left the wafers unusable. The results of the variety of RIE tests performed are covered in the discussion of photoresist later in this section. Because both RIE and wet etching have proven unsuccessful, DRIE must be used for the $SiO_2$ etch. The extreme depth to which the SI must be etched leads to the same conclusion regarding the etching process to be used. Therefore, the lithography step must lead to a high resolution layer of photoresist capable of withstanding DRIE. Many variations on three main solutions that involved one of two types of photoresist or a metal mask were explored in the development of this step.

Initial process design incorporated the S1813 photoresist from Shipley's Microposit S1800 series. This photoresist is readily available, well understood, and provides excellent resolution of less than one micron [13]. This photoresist was initially tested using RIE for the $SiO_2$ etch. RIE of $SiO_2$ is done using a $CH_4$ plasma in a Samco model RIE-1C reactive ion etcher. The equipment offers variable gas flow and RF power. A large portion of time during my research project was spent attempting to incorporate RIE into the final process flow because it is simple, cost effective and

provides an acceptably anisotropic etch of thin layers of $SiO_2$. The earliest tested process employed a 1200nm thick layer of S1813 photoresist and did not use Hexamethyldisilazane (HMDS) or a hardbake. These choices were made to promote the exposure of a pattern with high resolution and narrow linewidth, which can be more readily obtained when HMDS is not used. Additionally, resist removal is easier when the resist has not undergone a hardbake. The first reactive ion etch was performed at 50W RF power with $CF_4$ flow rate of 10mL/min at 20°C and 100mT chamber temperature and pressure. The RIE process left the photoresist burned onto the wafer and completely destroyed the mask pattern. The hardened photoresist could not be removed with standard acetone rinses or a more extreme Piranha bath consisting of a three-to-one mixture of sulfuric acid to hydrogen peroxide maintained at a temperature of 110°C. To combat these issues, the S1813 was spun to a thickness of 1500nm and a one minute hardbake was included to help the photoresist withstand RIE. These parameters lead to similar results. A number of parameter combinations were tried including increased photoresist thickness, variable hardbake time, and variable RF power. No combination of factors allowed the S1813 to withstand the 12 to 15 minute etching time required for 500 nm of oxide. These results lead to the replacement of $SiO_2$ etch using the RIE with DRIE. Unfortunately, S1813 photoresist typically spins to a thickness of 1200nm to 1500nm [13]. This thickness would not be sufficient for two DRIE steps, so another solution is needed.

The possibility of using a metal mask was explored. The authors in [14] show excellent results from using aluminum as an etch mask in DRIE. However, there were several reasons why the use of a metal mask was not desirable in the process flow that I

developed. First, the grating masks were not designed to account for an intermediate metal mask that would result in narrowing of the pattern linewidths. This issue can be corrected by adjusting the spacing of the photomask pattern to insure that the grating mold obtained after DRIE is within the initial grating specifications. However, the purchase of new photomasks was not within the budget of my project. Secondly, the inclusion of a metal mask calls for an undesirable metal etch and physical vapor deposition (PVD) to be introduced into the process flow, increasing the expense and complexity of the grating fabrication process. Furthermore, the Virginia Tech Alcatel DRIE does not typically support etching using metal masks, which is the principal factor that prevented any attempt to test an actual metal mask when patterning the gratings during this project. Ultimately, this solution introduced many unneeded steps and special configurations that did not fit the efficient process model being sought.

The final solution uses the AZ9260 photoresist. As part of the AZ9200 series, this resist is capable of 1μm resolution at film thicknesses of 10μm [11]. AZ9260 has proven successful in the DRIE steps called for in the final process. The AZ9200 series also includes the AZ9245 photoresist that has a similar chemistry but allows for higher resolution, which could prove useful for the gratings with smaller feature size. The full lithography process is as follows:

1) Dehydration bake: 110°C for 5 minutes

2) Spin HMDS: 1500rpm for 20 seconds

3) Dispense AZ9260: 300rpm for 10 seconds

4) Spin: 2400rpm for 60 seconds

5) Softbake: 110°C for 30 seconds

6) Expose: 1500mJ/cm$^2$ (Approximately 150 seconds on channel 2 using the VT MA-6)

7) Develop: Approximately 4 minutes in AZ400:water 1:3 bath

The process follows the general guide provided by AZ [11] with some small changes. HMDS was added to the process to prevent photoresist liftoff of the thin lines of the mask during development. The time associated with the softbake was also made shorter to account for the HMDS. With HMDS and the recommended 2 minute softbake, the mask would not develop correctly, if at all. Shortening the softbake to 30 seconds solved this problem.

The required exposure for 10 μm of AZ9260 is 1500mJ/cm$^2$. This exposure takes 150 seconds at 10mW/cm$^2$ when using the MA-6 available in the Micron clean room. Proximity exposure is used because hard contact exposure could damage the photo resist and threaten the yield at future steps of the process. After experimentation using the G0 mask, it was found that an alignment gap of 50μm correctly exposed the mask pattern. This distance is within the parameters defined by equation (4). After development, no noticeable changes in the pattened linewidths were observed. However, inspection and measurement of the resist lines was limited by the resolution of the SPL optical microscopes used at 1000 times magnification. Measurements of the photoresist lines in a scanning electron microscope was not performed as the purpose of this project was to determine a set of processing procedures to fabricate the grating structure and did not include the optimization of the grating photomask and resulting grating dimensions.

Development time is also a sensitive parameter. Overdevelopment causes the pattern of lines to lift off the surface of the Si wafer, destroying the mask. Four minutes will typically lead to a successful development. The mask's pattern and color, in contrast to the oxide color, allows for immediate visual feedback that can help identify when the development is completed during this process. If development is closely monitored, one can see the oxide slowly exposed and remove the wafer once the full square pattern transferred from the photomask is showing. The lines should be checked using a microscope to ensure full development.

Following mask development, the $SiO_2$ must be etched to expose the Si surface. Again, the possibility of using RIE was explored using the AZ9260 photoresist. Through a series of tests similar to those performed using S1813, it was found that the AZ9260 will not properly withstand the Samco RIE process. The AZ9260 does not harden on the wafer surface and can be removed using an acetone clean and an $O_2$ plasma etch. However, the mask pattern is completely destroyed, leaving non-uniform lines that will not lead to correct development of the mold structure in subsequent process steps. Two solutions to this problem were explored; using the remaining oxide as a mask during DRIE or replacing the RIE process.

The first solution to the above problem involved using the existing oxide layer as the mask during the DRIE process. DRIE of Si uses $SF_6$ plasma which typically has a selectivity of approximately 200:1 for $SiO_2$ layers. However, there are some issues with this solution. First, because the wafer must be etched to a depth of 100 microns, 500nm of oxide will also be etched at a selectivity of 200:1. Therefore, to ensure that enough oxide remains to act as an insulator during electroplating, at least one micron should be

grown in the initial process step. This increase in thickness will lead to a longer RIE process, which implies more resist degradation and less accurate etching of the grating pattern. Additionally, DRIE will cause degradation of the oxide layer, which could cause problems during electroplating. Ultimately, this solution has too much of a negative impact on the oxide layer to be useful.

Instead of combating the problems introduced by RIE, it is more reasonable to remove the process entirely. The $SiO_2$ etch can be performed using deep reactive ion etching instead of standard RIE. The Alcatel offers DRIE of $SiO_2$ using a $CH_4$ plasma. The AZ9260 photoresist has successfully withstood this process in the SPL. This solution allows for the single photoresist layer to serve as the mask during etching of both the $SiO_2$ and Si layers. Unfortunately, during the development of the full process, the Alcatel DRIE at the SPL could not etch $SiO_2$ due to an unknown maintenance issue. To continue process development, it was decided that a liquid etch would be used on the G0 grating. The large feature size of this grating lessens the effects of the isotropic liquid etch. Wet etching was done using a solution of 6:1 BOE. For 500nm, this etch typically takes approximately 10 to 12 minutes, but the wafer should be examined using a microscope to ensure that the underlying Si is fully exposed. It was discovered that the BOE did not etch each trench equally. Sections of adjacent trenches would etch at similar rates, but this rate was not constant across the wafer. Visual inspection showed that the slower etching sections had formed air bubbles at the ends of the trenches. This was a sign that the BOE was not filling the trenches properly. This problem is fixed by dipping the wafer in water immediately prior to submersion in BOE in order to improve the wetting of the BOE within the trenches.

Once the Si surface is exposed by the $SiO_2$ etch, the Si must be etched to a depth of 100μm to form the mold. This etch is done using deep reactive ion etching employing an $SF_6$ etch at 1800W alternating with $C_4F_8$ passivation. The AZ9260 photoresist can continue to serve as a mask during this process. The Si etch rate of the Alcatel DRIE is 4 μm/minute, which provides an etch time of 25 minutes. Following this etch, the photoresist and the polymer layer are removed. Removal is done in an ultrasonic acetone bath for 30 minutes. An $O_2$ ashing process could also be used to ensure total solvent removal. After removal of these layers, the wafer is rinsed with deionized (DI) water and dried. The extreme trench depth makes drying difficult and extra care should be taken to ensure that the full surface is dry.

The wafer is now ready for electroplating. Seedless electroplating has proven successful on a bare silicon surface [15, 16]. The process was chosen because it is simple, inexpensive, and requires very little equipment. Additionally, the electroplating process will produce fewer voids than physical vapor deposition (PVD), which could also be used to fill the trenches. PVD relies on metal vapor condensing on the surface of the wafer. Because the trenches are very deep and the vapor reaches the top of the trenches first, condensation of the metal is biased towards the top of the trenches rather than deep within them. As the vapor condenses, the metal grows inward from the trench sidewalls at a greater rate towards to top of each trench as compared to the bottom. Eventually the metal at the top of a trench will seal off the rest of the trench before it is fully plated, leading to large voids in each trench. Electroplating eliminates this issue because the trenches are completely filled with the electroplating solution before plating begins.

Therefore, as long as the ions in the solution are able to flow into the trenches, we ensure that the trench is plated evenly without bias towards the upper portions.

A lead electroplating solution containing fluoboric acid and metal fluoborate is used in the electroplating process. The wafer is submerged in the plating solution opposite a platinized Ti grid, which serves as the plating anode. The wafer must be the cathode to complete the circuit. Ideally, the grid should be at least two times greater in area than the wafer to produce a uniform electric field [17]. The product datasheet obtained from the lead solution manufacturer, Transene, calls for 6V plating voltage. Through experimentation, it was found that approximately 800mA at 6V produced uniform smooth plating. Any value well above 800mA caused immediate over-plating in which the lead would build-up at the edges of each trench and destroy the grating structure. The plating bath is also stirred at 200rpm to promote ion distribution in the solution. Experiments performed in this study have shown that the mixture plates at about 1 to 1.2 microns per minute. This does not translate to a 100 minute plating step for the gratings since the lead will plate from the trench sidewalls as well as the bottom of the trench. However, it has not been determined what the plating time for each grating should be since this step has not proven entirely successful, as discussed in the following section.

# III. Results

There are two main sets of results that have been obtained from fully developed processes. Each process uses the G0 grating and was analyzed with the focused ion beam and scanning electron microscope (FIB/SEM) at the Virginia Tech Institute for Critical Technology and Applied Science (ICTAS) laboratory. The first set of results was obtained from a process that was developed during the down-time of the DRIE machine. DRIE is a key component in the development of these gratings. During the down-time, it was decided that RIE could be used to show proof-of-concept. The Si would be etched to a depth of 5-10 microns using RIE. Additionally, the $SiO_2$ deposition and patterning steps were removed since a polymer would no longer be introduced by DRIE and the photoresist could act as the insulating layer between trenches. This process flow is similar to that discussed in [8]. This experiment proved unsuccessful for two reasons, but it does provide useful results that can be applied to the full process or used to develop a new solution to the problem.

Figure 3 shows that the process is successful in creating the periodic grating structure. The darker lines are the AZ9260 photoresist and the lighter lines are the lead plating.

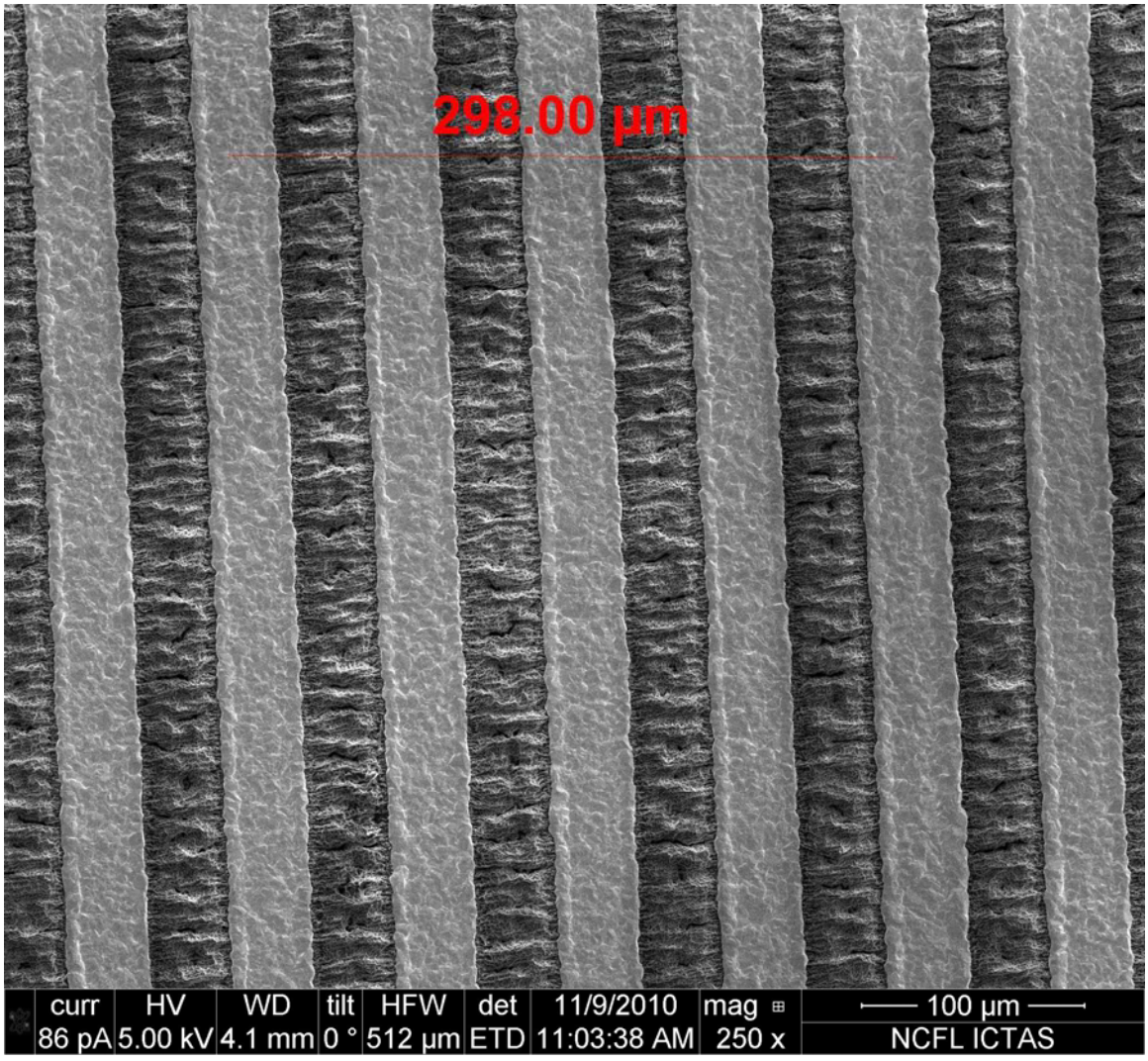


**Figure 3: Top-down view of G0 developed using RIE**

These materials do not transition abruptly as is desired. Instead, the photoresist lines are rough and the lead has filled the voids, which affects the uniformity of the grating structure along the length of the slit as well as from slit to slit. The roughening of the resist is due to the photoresist damage introduced by the RIE process, as discussed in the previous section. The Si RIE is done at 200W forward power using $SF_6$ at a flow rate of 30sccm. The chamber is kept at 150mT pressure and 20°C. These parameters will etch

Si at approximately 4μm /min, but severely damages the photoresist and destroys the integrity of the established mask structure.

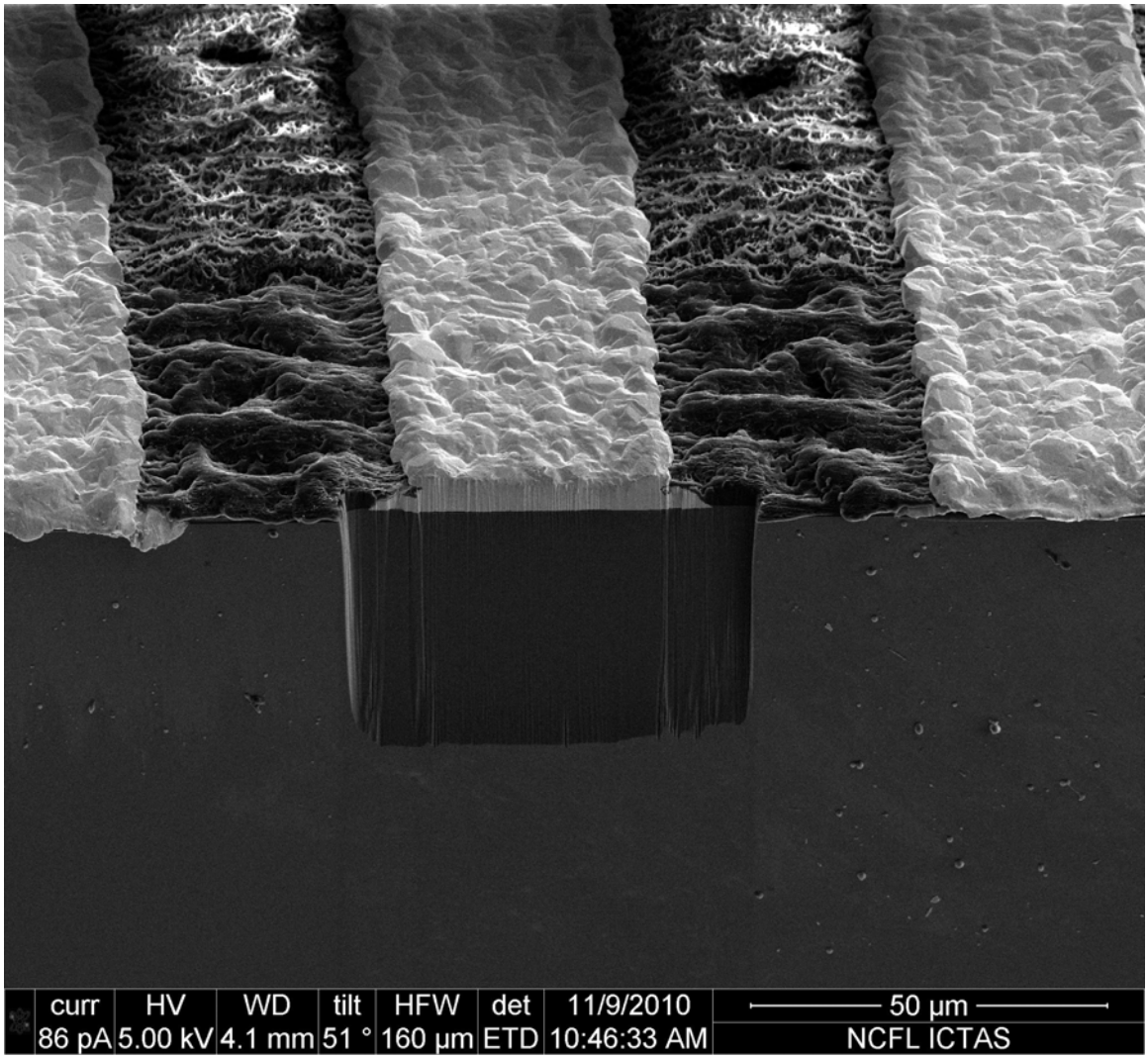


**Figure 4: Side view of G0 developed using RIE**

Figure 4 shows a side view of the wafer. The side view provides a variety of insights. The most apparent issue is the lack of any trench having been etched. While likely a technical problem with the RIE machine at the time, the result allows for an interesting analysis. Because there is no Si trench and the photoresist is non-conductive, the lead will only plate from the surface of the Si instead of working in from the

sidewalls. We can see in the figure that this method is effective and does not produce voids or air pockets. There is, however, some evidence that the adhesion of the resist to the wafer was being compromised during the electroplating step as the image shows that Pb was plating between the wafer and the photoresist along the edge of the patterned stripe. The reason for the laterial plating is likely a combination of the loss of adhesion between the damaged resist and the wafer along the resist edges as well as a water-promoted loss of adhesion of the undamaged resist during the somewhat lengthy plating process. Figure 5 shows an enhanced view of this result. This enhanced view also further illustrates the issue with using standard RIE since it is clear that the photoresist has been damaged. SEM measurements place the plating depth at approximately 6 microns which is consistent with the 5 minute plating time that was used.

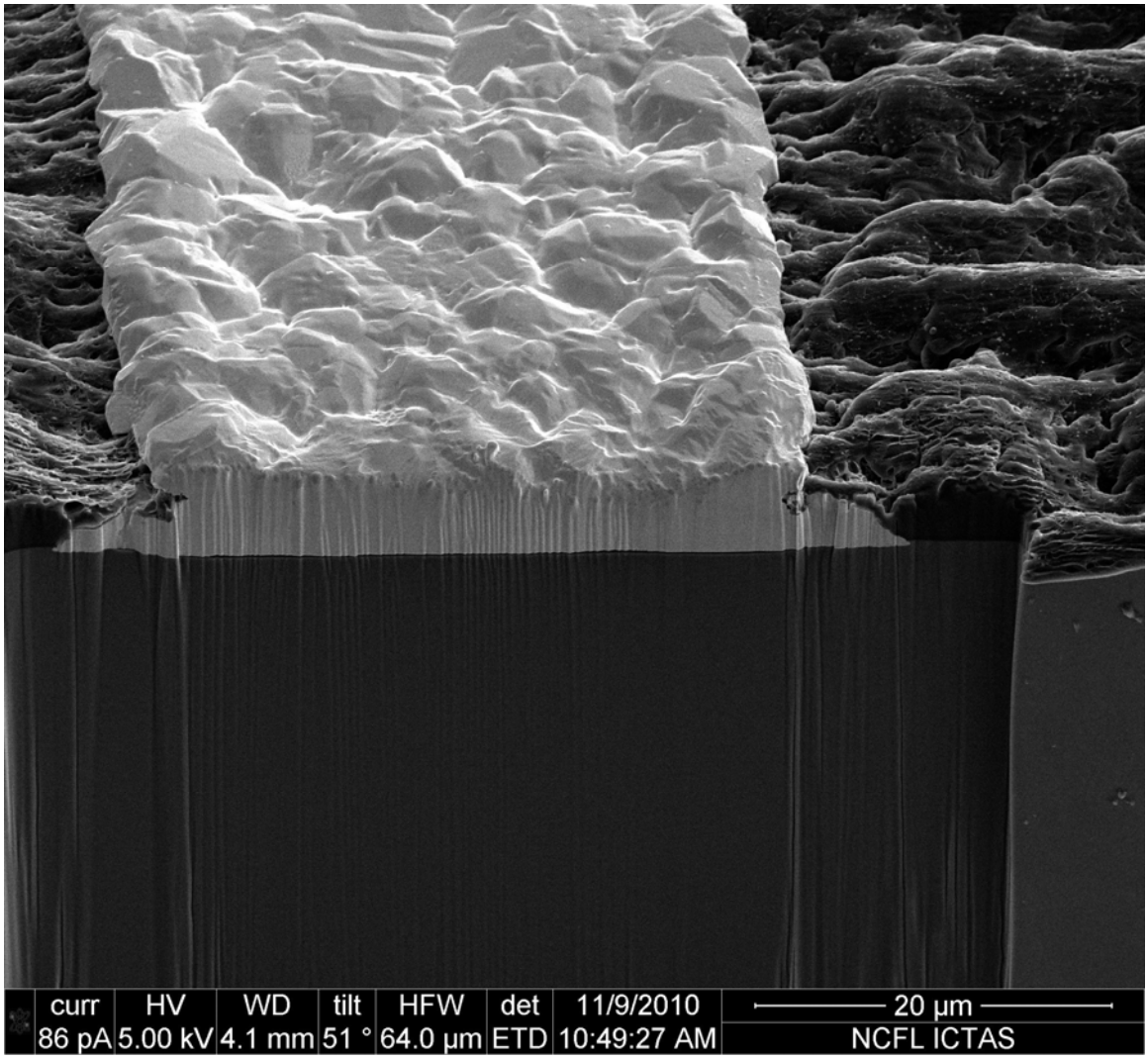


**Figure 5: Enhanced side view of G0 developed using RIE**

From this analysis, we can determine that a process that plates on the Si surface between photoresist outlining the trenches would be highly effective once the adhesion issues were resolved. The photoresist would not be damaged by a DRIE etch so the lines would be more exact. However, this technique is impractical for trench depths of 100 microns since that dimension would be nearly impossible to spin, expose, and develop correctly. Additionally it is highly unlikely that undamaged photoresist would adhere to

the Si wafer in a water-based plating bath for the 85-100 minutes that would be required to plate a 100μm thick layer of Pb.

This experiment allowed for characterization of the plating process by providing a plating rate and showing that plating is successful in producing an acceptably uniform layer free of voids. Results also hint at the possible etch-free solution that would be useful for gratings of lesser depth. However, machine issues kept this experiment from providing a suitable proof of concept for the final process.

Once the Si etch portion of the Alcatel DRIE at the clean room was operational, the full process was performed. A wet etch of the $SiO_2$ layer was used because of the still malfunctioning $SiO_2$ DRIE etch process. The following results show the result of the full process applied to the G0 grating as seen in the images collected from ICTAS FIB/SEM. Figure 6 shows top-down view of the plated trenches.

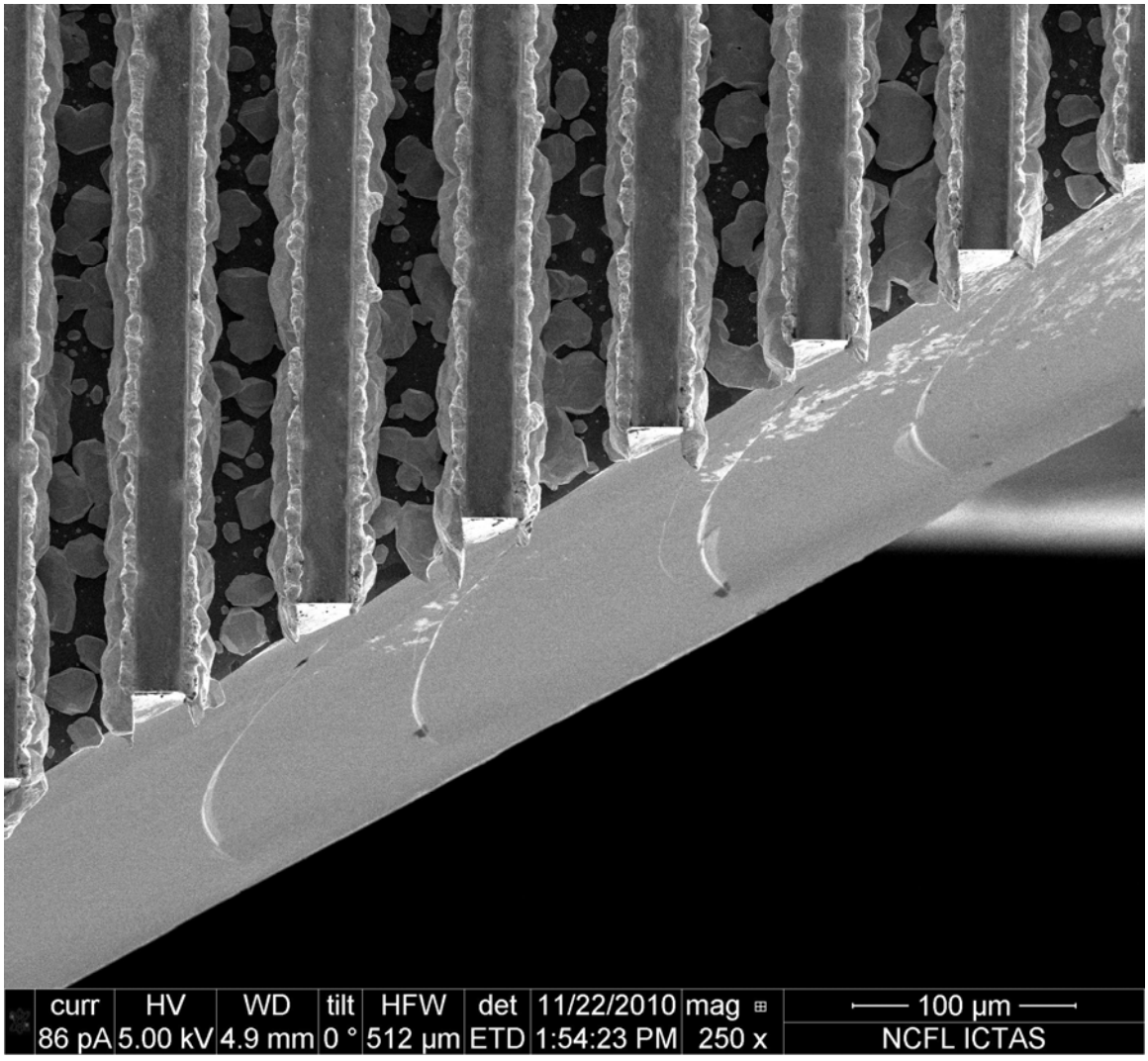


**Figure 6: Top-down view of G0 developed using DRIE**

It can be seen that the trenches have not completely filled with lead. Plating has occurred on both the sidewalls and bottom of the trenches, but there are voids throughout the grating. At first, it would seem that more plating time is needed; however, this is not the case. Multiple wafers underwent this final process with slight variations to plating time and current in each case. However, each wafer exhibited highly non-uniform plating. Not shown in Figure 6 are the areas of the wafer that overflowed with lead, destroying the periodic structure. It was found that the plating process produced

unpredictable results. There are two likely explanations. The first is a non-uniform electric field produced by the process. However, this is not likely since the areas of lead distribution would fit some pattern produced by a symmetric field, which is not the case. The more likely reason is that there is poor, non-uniform flow of fresh solution in the trenches. As was seen with the non-uniform BOE etch, it can be difficult for liquid to fill and refresh the trenches because of their narrow opening. Thus, as the metal plates inside the trenches, the lead ions are depleted from the electroplating bath solution within the trenches. The mixture in a single trench will eventually be fully depleted and plating will stop in that trench. It is therefore necessary to refill each trench with new portions of the solution. However, this experiment was performed in a mixture that was only stirred using a magnetic stirrer at the bottom of the electroplating bath, which is not likely to force the refilling of every trench with fresh solution. A possible solution to this issue is discussed in the future works section of this paper.

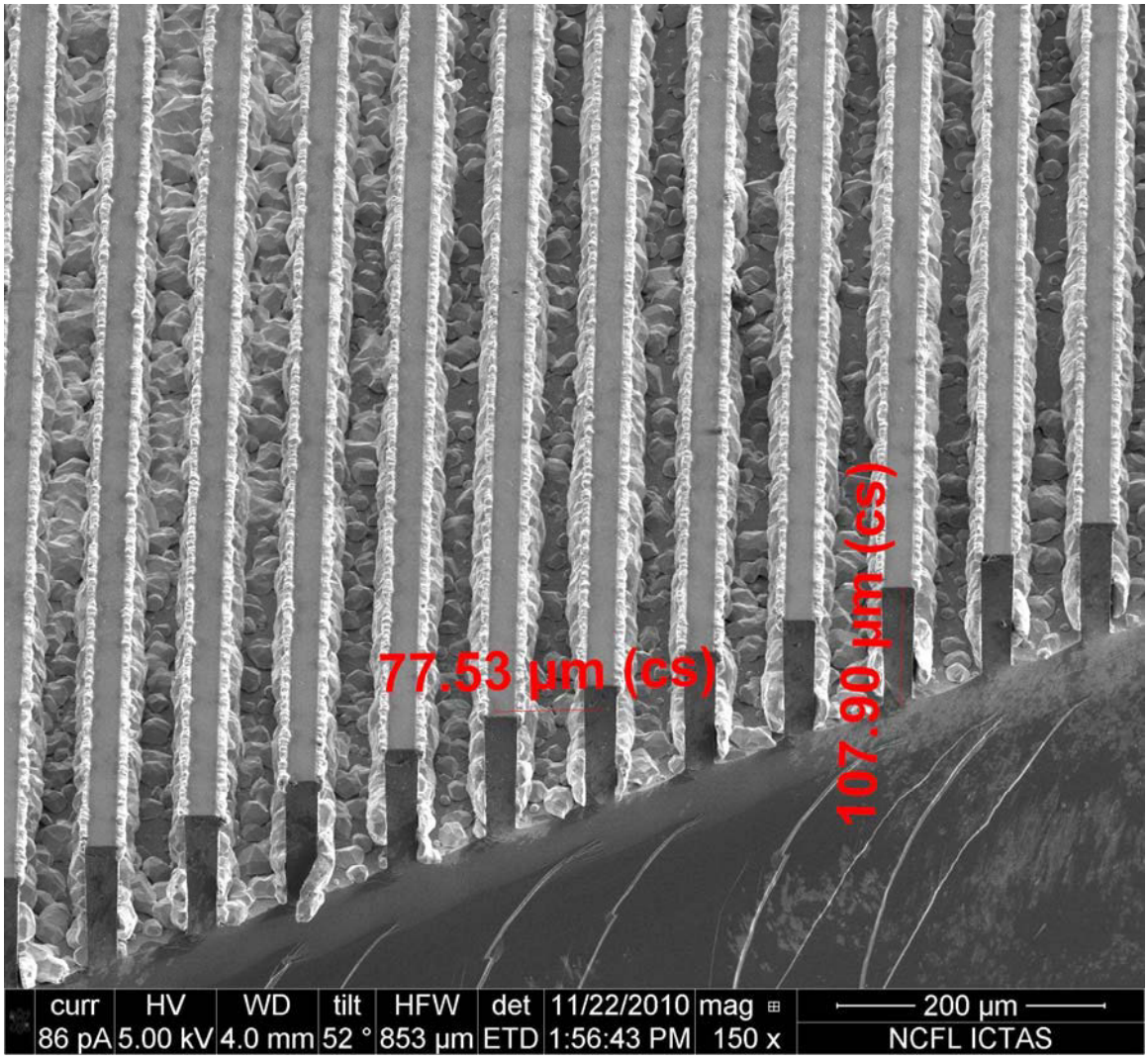


**Figure 7: Side view, with measurements, of G0 developed using DRIE**

Figure 7 shows a side angle view of the plated trenches and includes depth and period measurements obtained using the FIB/SEM. The above results are consistent in this micrograph and are amplified by noting the distribution of the lead. The sidewalls appear to have better lead coverage than the bottom of the trench. This outcome matches the fact that the plating solution is less likely to refresh lower portions of the trench. Figure 7 shows two promising results. First, we see that the trenches have etched very nicely. The sidewalls are vertical and straight, which is a requirement of the grating

structure. The etch depth is approximately 108 microns. This depth is nearly consistent with an etch rate of 4μ/minute. Overetching is not a problem since more lead will still serve to completely absorb the incoming x-rays, only an under etch presents a problem as long as the gratings are aligned perpendicular to the propagation direction of the x-ray beam. The period is also consistent with the dimensions of the G0 grating. Secondly, plating has not occurred between the trenches. The result shows that the insulating layer of oxide functions correctly. However, it may also be an indication that the entire polymer layer that was introduced in the DRIE process may not have been removed. Figure 8 shows an amplified cross-sectional view of this result.

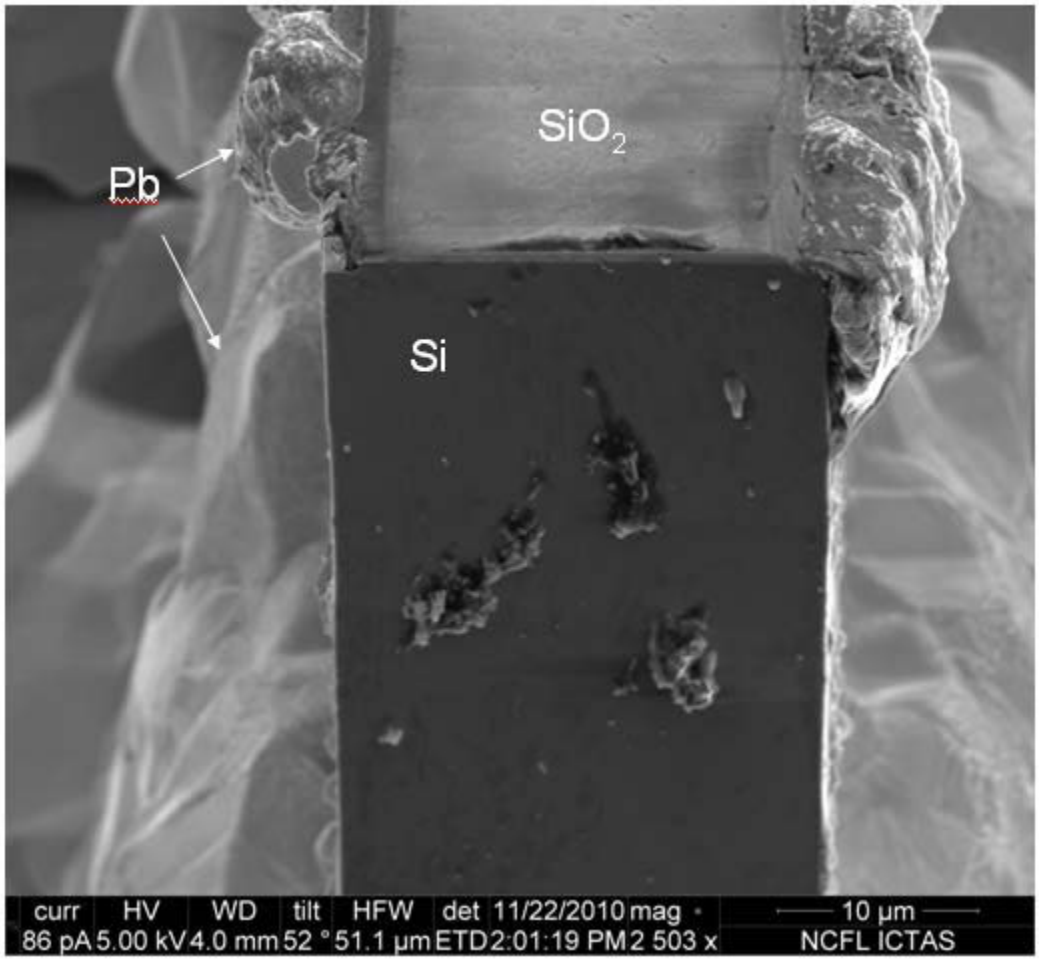


**Figure 8: Enhanced cross-sectional view of trench separation in G0 developed using DRIE**

The lead has begun to plate the top corner edges of each trench. However, this is an expected result since an isotropic wet etch was used to define the pattern in the oxide layer, leading to some removal of the oxide from the top of the grating structure. . Minimal lateral etching will occur when a DRIE process is used to open windows in the oxide layer because of the highly directional nature of DRIE. Thus, the top edges of the Si wafer will not be exposed and we will no longer see the edge plating issue shown in Figure 8. Additionally, DRIE will allow for an even thicker layer of oxide to be used to ensure electrical isolation, which will increase the yield of the grating fabrication process.

The above experiments have provided for proof of concept of the general process. Acceptable trenches may be etched to a depth of 100μm and kept electrically isolated by relatively thin layers of oxide. The trenches can be filled using the electroplating process. However, a basic plating procedure will not be successful in this case because of the extreme depth of the trenches and the difficulty in keeping the solution fresh in each trench. Solutions to this problem and other changes and improvements are discussed in the following section.

# IV. Future Work

This thesis has provided a proof of concept for production of the x-ray CT gratings. Some work must still be done to fully fabricate these components. The most apparent issue presented is the unsuccessful filling of every trench in the wafer. The non-uniform plating of the wafer is not acceptable. There are a few steps that may be taken to combat this issue. First, a larger plating grid should be used to ensure a uniform field distribution across the wafer. At the time of this experiment, no such material was available. Second, new plating solution must be constantly moved into each trench so that they may continue to plate uniformly. This can be accomplished using a system in which the solution is pumped toward the wafer. This added flow should force new solution into each trench. If this change does not lead to a successful process, plating could be performed in short increments; removing, rapidly heating, and then cleaning the wafer between each increment so that the lead deposited reflows to fill the bottom of the trench before the next short plating period.

Once the trenches have been filled, it is possible that voids may develop at the lower center section of each trench. This situation can occur if the plating sidewalls meet each other and seal the trench before all portions of the trench are fully filled. This problem would have to be observed by cross-sectioning the wafer and then collecting images using SEM. If such a problem did occur, there is a possible solution as permitted by the Pb-Si phase diagram [18]. The wafer could be heated to the melting point of lead after plating. This would effectively reflow the solution and fill the trenches in a uniform manner. This technique could be used to combat voids introduced for any other reason as

well. With a melting point of 327°C, lead should melt before adverse effects are seen at other points on the wafer. However, this solution could cause some damage to the wafer and heating the sample may cause layers of oxide to form on non-plated portions of the trenches. These small oxide layers could cause problems during electroplating, which means that a more complicated setup would be needed to melt the Pb correctly. These additional arrangements include reflowing the Pb in an oven under vacuum or one into which forming gas is being introduced, which raises some safety issues. Therefore, this solution should be attempted only if the other options presented do not work.

The above process must also be performed using the more detailed gratings with feature size on the order of 1μm. These devices may call for a higher resolution photoresist. The AZ9200 line of resists includes AZ9245, which uses the AZ9260 chemistry but will produce greater resolution masks [11]. This may be needed for the G2 and G1 gratings.

Another final process solution lies in a combination of the two experiments shown in the previous section. The first experiment proved that a photoresist layer may be used as insulation between trenches. However, introduction of a polymer in the DRIE step means the photoresist will be removed (along with the polymer) before plating. This removal makes inclusion and etching of a $SiO_2$ layer necessary. The etching of this layer proved to be a key difficulty throughout process development. Elimination of this step would decrease complexity and increase yield. This elimination can be accomplished by removing the polymer without removal of the photoresist. The polymer created and deposited on the Si surface during the Alcatel DRIE process is $C_4F_8$. This layer can be removed after the Si etch using Ar ion bombardment. This step would leave the

photoresist intact and the surface clean of any $C_4F_8$, allowing the resist to act as the insulator between trenches. A short directional bombardment could also be used to remove only the $C_4F_8$ along the bottom of each trench, leaving the sidewalls coated with the polymer. This solution leaves the bottom of each trench as the only conductive surface during electroplating. Therefore, plating occurs from the bottom of each trench upwards, instead of in from the sidewalls. This mechanism is similar to that seen in the RIE experiment in which the lead plates on the exposed wafer surface in between non-conductive photoresist sidewalls. The RIE experiment shows that this plating method produces excellent trench fill. However, because $C_4F_8$ is extremely hydrophobic, this solution may exacerbate the issue regarding flowing solution into each trench. Additionally, this plating method would lead to plating times of approximately 85 to100 minutes. Extended time in the plating bath can cause resist degradation and threaten the electrical isolation of each trench. These two issues could prevent this method from resulting in a viable solution.

A noteworthy side effect of the final developed process is its potential use in power electronics. If the oxide layer is not used, the trenches can be etched into the back of a bare silicon wafer. These trenches can act as a heat sink since they greatly increase the surface area of the wafer. Because heat transfer is directly proportional to the exposed cross-sectional area of the wafer, the wafer will dissipate more heat produced by planar devices constructed on the front of the wafer.

# V. Conclusions and Summary

The above work provides proof of concept for a process designed to create gratings used in x-ray computed tomography. It has been shown that the unique dimensions of these gratings increases process complexity and introduces many subtle issues. The thickness of the gratings establishes a strenuous depth requirement. This condition can be satisfied using deep reactive ion etching, as shown in this experiment. Furthermore, the electroplating results show that the process can be successful. A thin oxide barrier is sufficient for isolating individual trenches during electroplating. The only problem remaining is that the trenches do not plate completely. However, since all portions of the trenches do at least begin to plate, and some trenches show complete plating, the modifications will only need to increase uniformity.

The final process is simple and requires only a few machines and four to five man-hours (including waiting on etch steps). While the fabrication of the gratings as designed was unsuccessful, the few needed changes to the presented process should allow for full development of the gratings and would not require expensive equipment. The outstanding portion of the process is only a method for producing constant flow of the plating solution into the etch trenches during the Pb electroplating step. Additional improvements have been presented to simplify the solution and combat some possible future issues. The solution can also be applied to other areas of interest in the semiconductor industry.

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