D-Mode GaN HEMT with Direct Drive

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***Abstract*—A direct-driven gate driver circuit has been developed for the depletion-mode gallium nitride (d-mode GaN) high electron mobility transistor (HEMT), which is a "normally on" device and is typically connected in series with a low-voltage power MOSFET to prevent shoot-through faults. The switching of such a "cascode" device is substantially delayed due to a large MOSFET input capacitance. This paper introduces a charge-pump based direct-driven approach to provide a negative voltage in the gate drive loop so that the device becomes "normally off." The switching characteristics of the direct-driven HEMT is analyzed through computer simulation and hardware testing. Results indicate that the switching delays due to MOSFET gating is eliminated, and the voltage slew rate can be directly controlled by the gate resistance.**

***Keywords*—Direct drive GaN, Gate driving, HEMT**

I. Introduction

The depletion-mode (d-mode) gallium nitride (GaN) high electron mobility transistor (HEMT) can be combined with a low-voltage silicon (Si) MOSFET in a series connection to create a cascode device, transforming it from a normally-on to a normally-off device. Currently, there are two types of cascode-structured commercial products available. The first type utilizes the conventional cascode approach, where the gate pin of the HEMT is tied to the source pin of the MOSFET [1-3]. When the dc-bus voltage is applied, the initially conducting HEMT is blocked by the MOSFET's drain-source voltage, which provides a negative gate-source voltage for the HEMT. However, this approach introduces MOSFET junction capacitances and parasitic components during switching, resulting in higher losses and increased noise. In addition, the input capacitance of MOSFET tends to create a gating delay that will impact the duty cycle under high-frequency switching condition.

The second type of cascode design involves driving the HEMT gate with a negative voltage. There are two methods of implementation found in this regard. One method adds an internal buck-boost converter [4-5], while the other method uses a charge-pump capacitor to produce a negative voltage [6-7]. In the charge-pump approach, a diode is added from the gate pin of the HEMT to the source pin of the MOSFET, serving as a blocking element. This is similar to the conventional cascode approach. The diode, along with the charge pump capacitor, provides a positive voltage during turn-on and a negative voltage during turn-off. The MOSFET remains on after the initial charge, so pulse-width modulation (PWM) only applies to the HEMT. The switching waveform can be much cleaner due to fewer parasitic component loops.

The distinct advantage of both direct drive designs is that the switching speed or delay is not affected by the bottom MOSFET. However, the start-up control to prevent initial shoot-through has never been addressed. During normal PWM operation, the HEMT can be turned off by an external negative voltage or a charge-pump capacitor and turned on by zero volt across gate-to-source.

However, existing commercial cascode devices lack flexibility as they integrate both devices or even the gate drive circuitry inside the package, preventing users from selecting appropriate components for different switching conditions, such as hard- or soft-switching. To further study the switching characteristics under different gating approaches or applications, discrete GaN HEMT products are necessary. Nonetheless, even with the availability of the HEMT chip, the package or layout needs to be highly integrated to minimize parasitic inductances at the circuit level, which can cause ringing with the junction capacitances.

In this paper, we use an in-house developed high-voltage GaN metal-insulator-semiconductor (MIS) HEMT device for direct drive design and switching characteristic study [8]. To mitigate parasitic effects, the HEMT device is not housed in a conventional plastic package and can be connected to the MOSFET with minimal loop inductances. In order to allow the HEMT pins to be soldered onto the circuit board, we apply micro solder bumps on to each pin. For the direct drive gating operation, we begin with a topological study and then follow by SPICE circuit simulations to explain the switching behavior. A hardware double-pulse test (DPT) circuit has been developed and fabricated to test the switching transient and verify the analytical results.

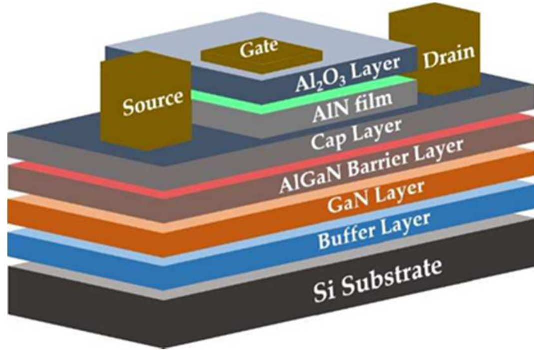
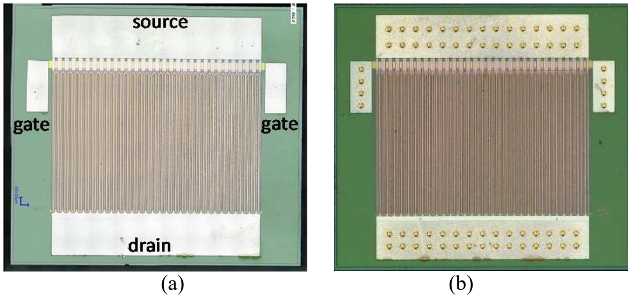


Fig. 1 Cross-sectional view of a GaN MIS HEMT.



(a) (b)

Fig. 2 (a) photograph of the HEMT bare die, and (b) GaN HEMT with added solder bumps.

II. Structure of GaN HEMT and Solder Bumps for Flip Chip Layout

Fig. 1 illustrates the stacked cross-sectional view of a high-voltage GaN metal-insulator-semiconductor (MIS) HEMT device that is used in this analysis. The device adopts low-cost silicon substrate and places a GaN/AlGaN buffer layer on its top. A GaN layer is deposited on top of the buffer layer, followed by a thick AlGaN barrier layer and a GaN capping layer, and finally an AlN space layer. The source and drain ohmic contact is created by evaporating the Ti/Al/Ni/Au multi-layer metal-stack, and the metal gate electrode is insulated by an Al_2O_3 layer [1].

Fig. 2(a) shows the bare-die photograph of a high-voltage GaN MIS HEMT device that is used in the hardware implementation and testing. The device adopts a low-cost silicon substrate and places a GaN/AlGaN buffer layer over it. First, a GaN layer is deposited on top of the buffer layer, followed by a thick AlGaN barrier layer and a GaN capping layer, and finally an AlN space layer. The source and drain ohmic contact is created by evaporating the Ti/Al/Ni/Au multi-layer metal-stack, and the metal gate electrode is insulated by an Al_2O_3 layer [5]. All the drain, source and gate pads are aluminum. The dimension of the bare die is 3850×4010 µm.

In order to solder the HEMT chip on the printed circuit board (PCB), we added micro solder bumps (or solder balls) for each pad, as shown in Fig. 2(b). The ball diameter is 93 µm, and the height is 65 µm. The added solder balls grant the flip-chip layout a substantial reduction of parasitic inductances

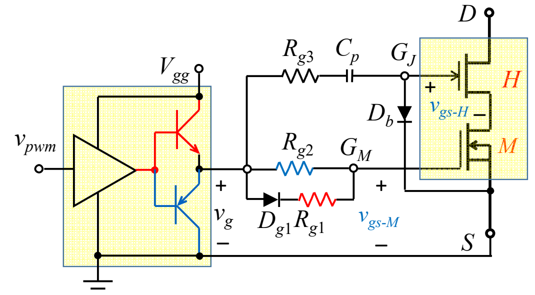


Fig. 2. Direct drive using charge pump for a cascode device.

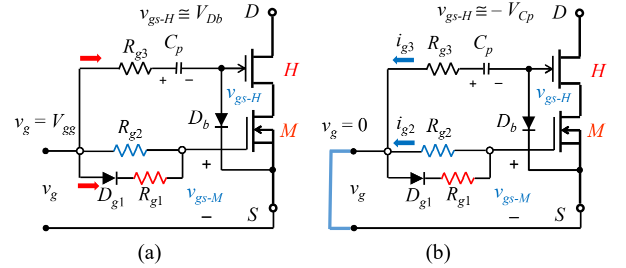


Fig. 3. (a) Turn-on transient waveforms, (b) turn-off transient waveforms.

III. Direct Drive Gating Circuit and Basic Operation

For a buck or flyback converter, the cascode type blocking is unnecessary as there is no shoot-through path to worry about. In such cases, the HEMT can be directly driven with a negative voltage using a conventional gate driver. For most other converters, however, the cascode structure is essential to prevent the shoot-through fault during the initial startup. As the use of an external negative-voltage gate driving approach is quite straightforward, this paper only describes the charge-pump approach in detail.

Fig. 2 illustrates the driver circuit, comprising a conventional non-isolated gate driver with a totem-pole output. The HEMT and MOSFET gate pins are driven independently. Diode D_b supplies a negative voltage for v_{gs-H} when the MOSFET conducts. The charge-pump capacitor C_p maintains a constant voltage with the magnitude about the same as the gate driver voltage V_{gg}. Resistor R_{g3} controls the gating speed of the HEMT. Resistor R_{g1} provides an initial delay to prevent MOSFET from conducting at the startup. Resistor R_{g2} prevents the MOSFET gate voltage from discharging too quickly when v_g is zero.

Fig. 3(a) and (b) depict the gating current paths during turn-on and -off conditions. The time constant $R_{g1}C_{iss-M}$ needs to be large enough to prevent the initial shoot through but small enough to allow v_{gs-M} getting charged when v_g is high. On the other hand, the time constant $R_{g2}C_{iss-M}$ needs to be large enough to prevent v_{gs-M} from discharging too quickly when v_g is zero. The charge pump capacitor C_p gets charged when v_g is high and discharged when v_g is zero. Typically, C_p needs to be two orders of magnitude higher than C_{iss-H}.

The gating path clearly shows that the gate drive resistors are directly connected to the GaN HEMT, which sets the direct drive apart as the primary distinction from the conventional cascode approach. Unlike the conventional cascode case, which lacks control over the turn-off voltage slew rate, the direct drive allows for regulating both the turn-off delay and the voltage slew rate through gate drive resistance selections.

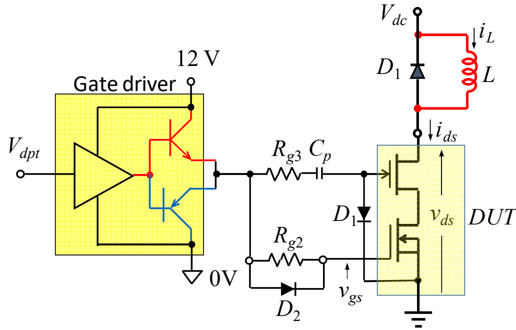


Fig. 4. Power circuit for the double-pulse test.

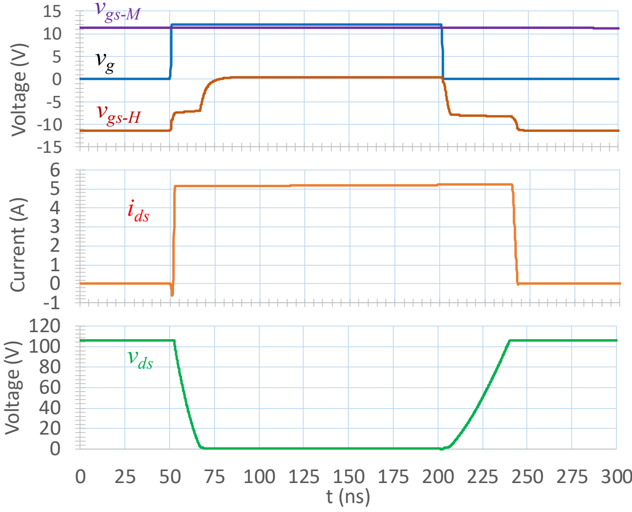


Fig. 5. Simulated key voltages and current waveforms for the direct drive gating circuit.

IV. Simulation Study

a. Switching Operation Verification

To better understand the switching delay and transient operation, the device is analyzed and simulated without parasitic inductances. Fig. 4 shows the complete switching test circuit without inclusion of parasitic inductances. A diode D_1 and an inductor L are connected between a dc bus voltage and the drain of the cascade device. The inductor serves as a current source, and the diode serves for freewheeling when the device is turned off. Key component parameters used in the simulation study are: V_{gg} = 12 V, R_{g1} = 470 Ω, R_{g2} = 10 kΩ, R_{g3} = 10 Ω, C_p = 220 nF. The device threshold voltage is $V_{th\text{-}H}$ = –10 V, and the MOSFET on-drop resistance is $R_{ds\text{-}M}$ = 3 mΩ, which results in 2% voltage drop can be omitted in the overall voltage drop plot.

Fig. 5(a) and 5(b) depict the simulation results under turn-on and -off switching transients. The MOSFET gate-source voltage $v_{gs\text{-}M}$ maintains at a constant after initial startup. During turn-on, $v_{gs\text{-}H}$ rises from –12 V. At –7 V, the HEMT current starts rising and reaches the full load current in less than 1 ns. The drain-source voltage v_{ds} falls to zero during a plateau region.

During turn-off, the HEMT voltage v_{ds} is charged when $v_{gs\text{-}H}$ falls below $V_{th\text{-}H}$ (–10 V). After v_{ds} reaches the dc bus voltage, current i_{ds} falls to zero in a few nanoseconds. above $V_{th\text{-}H}$. Again, a plateau clearly presents due to a large gate drive resistance.

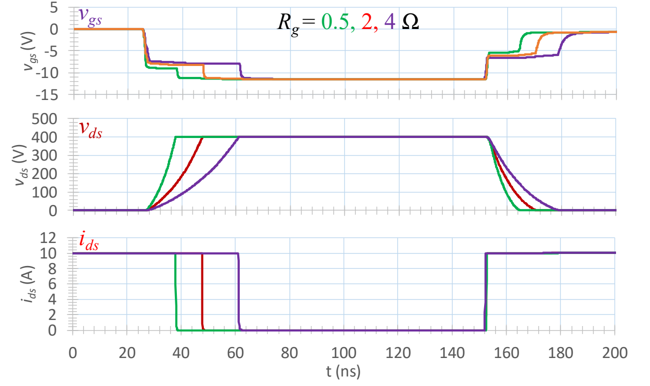


Fig. 6. Simulation results comparison showing gate drive resistance effects on switching.

b. Comparison with Different Gate Drive Resistances

As the gating control directly applies to the d-mode GaN HEMT, the gating delay caused by the Si MOSFET in a conventional cascode device no longer exists. In this case, the voltage rise and fall rates during turn-off and -on transitions are influenced by the gate drives resistances. Consequently, the miller plateau, absent in cascode gating becomes evident. The simulation results in Fig. 6 demonstrate the impact of the gate drive resistance (R_g) effects on switching delay and voltage slew rates during these transition. An ideal diode is employed in the simulation setup to avoid complications arising from reverse recovery and junction capacitance induced current spikes. The simulation also assumes the same R_g for both turn-on and -off gate charge loops.

During turn off, the gate-source voltage v_{gs} reduces from 0 to –12 V. Once it reaches the threshold voltage V_{th}, the drain source voltage starts rising with a slew rate determined by the product of gate drive resistance and miller capacitance ($R_g{\cdot}C_{gd}$). The current begins to decrease after v_{ds} rises to the dc bus voltage.

During turn on, voltage v_{gs} increases from –12 V to 0. As it surpasses V_{th}, the drain current i_{ds} starts to rise, and the inductor current i_L transfers to the device in less than one nanosecond. Once i_{ds} reaches i_L, the gate-drain capacitance or miller capacitance C_{gd} gets charged, resulting in appearance of the miller plateau. Voltage v_{ds} falls to zero after miller charging completes. It is important to note that the length of the plateau region is directly proportional to R_g during both turn-on an turn-off transitions.

c. Comparison with Conventional Cascode Approach

From the above simulation results, it is clear that the HEMT turn-on and turn-off transition processes are very similar to a conventional JFET with which the gate drive resistance and junction capacitances dominate the switching delay and voltage slew rates. It would be interesting to see how the switching transition behaves with a side-by-side comparison between direct drive and the conventional cascode approaches.

Simulation results comparing switching transients between cascode and direct drive approaches are illustrated in Fig. 7. In this simulation, all gate drives resistances are the same at 0.5 Ω, and the freewheeling diode is assumed ideal.

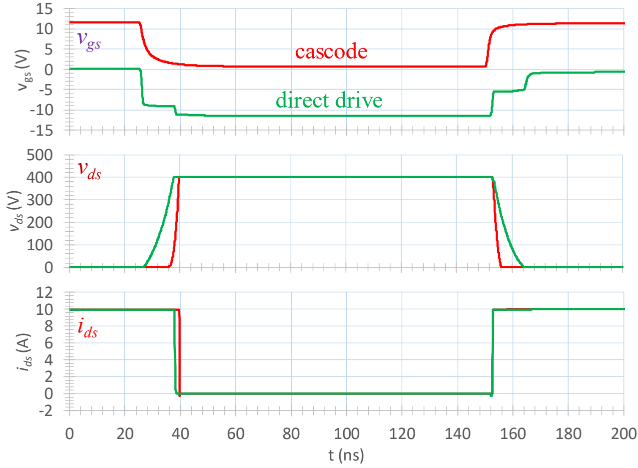


Fig. 7. Simulation results comparing switching transients between cascode and direct drive approaches.

During turn-off, the direct drive approach eliminates the delay observed in the cascode approach. However, a distinct plateau region is clearly present in the direct drive due to miller charging, which is absent in the cascode case. Furthermore, the voltage rise rate differs significantly between the two approaches. In the cascode case, the voltage slew rate depends solely on the load current, while in the direct drive, it is directly controlled by the gate resistance.

During turn-on, the current rise rate is nearly identical in both cases. Once again, with miller charging, the direct drive approach exhibits a voltage decrease with a slope proportional to the length of the plateau region.

V. Experiment Verification

a. Experimental Setup and Low Power Test

Fig. 8 shows the photograph of the test setup. The double pulse is generated with an in-house developed DPT controller which employs TI DSP 320F28079D. The pulse widths are programmable and controlled through analog inputs and fed into DSP through ADC ports. The power circuit consists of local bulk and film capacitors for testing voltage up to 450 V and an inductor rated 470 μH, 20 A. The freewheeling diode is a SiC Schottky diode (IDL04G65C5XUMA2), rated 650 V, 4 A.

Key parameters of the HEMT device are listed in Table 1. These parameters were also used in the previous simulations. The gate drive resistances are set at $R_{g\text{-}on}$ = 4.7 Ω and $R_{g\text{-}off}$ = 10 Ω.

Table 1: Key parameters of the HEMT device used in this study

Parameter	Value
Breakdown voltage V_{BV}	650 V
On-drop resistance $R_{ds\text{-}on}$	150 mΩ
Nominal $V_{th\text{-}H}$	–10 V
C_{iss} at v_{gs} = –15 V, v_{ds} = 200 V	165 pF
C_{oss} at v_{gs} = –15 V, v_{ds} = 200 V	60 pF
C_{oss} at v_{gs} = –15 V, v_{ds} = 200 V	28 pF
Nominal MOSFET V_{th}	2.5 V

Fig. 9 shows experimental results of the direct-driven gating circuit under a low-voltage low-current condition. With a bench power supply as the source, the dc bus voltage is limited to 34 V, and the current is limited to 3 A.

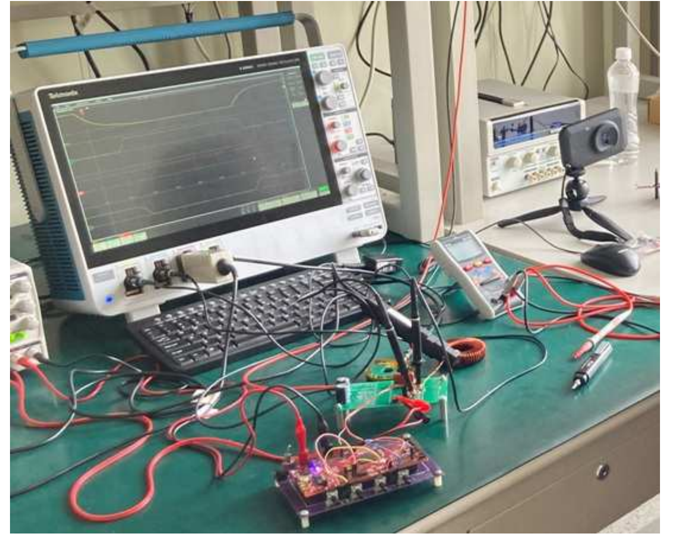


Fig. 8. Photograph of the double pulse testing controller and power circuits

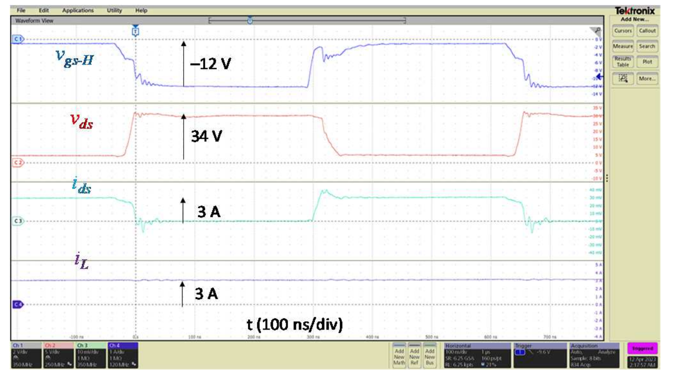


Fig. 9. Experimental results showing key voltage and current waveforms of direct driven GaN HEMT.

The device current is monitored with a home-made current transformer (CT) with 10:1 current transfer ratio, and the output of the small CT goes into a wide bandwidth CT with 1 V/0.1 V ratio. The measured i_{ds} indicates a noticeable overshoot during turn-on due to the freewheeling diode junction capacitance charging. The gating signal is also corrupted due to the current shunt, which is 3-mm high and injects a total of 4-nH loop inductance into the source pin. This inductance has been regarded as a common source inductance because it has both gate and drain currents flowing through it.

b. Experimental Results at High Voltages

From simulation results shown in Figs. 6 and 7, we can observe that the current rise and fall times are all in sub-nanosecond range. Even with a scope bandwidth of 1 GHz, the bandwidth of a current probe or sensor would not be able to appropriately measure the current under transition conditions. Therefore, not only the current sensing can induce noises, but also its measurement may not be accurate enough to verify the performance observed in simulations.

For high-voltage tests, to avoid the common source parasitic inductances induced noises, a PCB is designed to eliminate the device current measurement. As the current waveform can be observed with simulation, the test without current viewing allows a better observation of the gating delays and voltage slew rates.

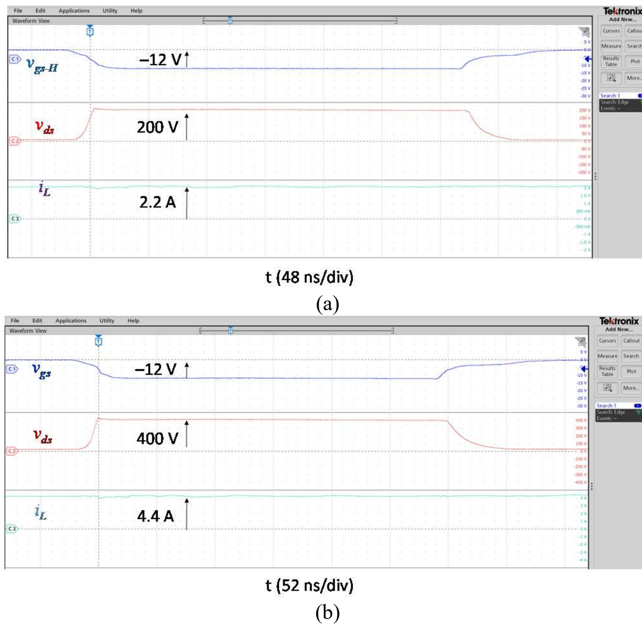


Fig. 10. Experimental HEMT voltage and current waveforms with the direct drive gating control: (a) at 200 V, 2.2 A and (b) 400 V, 4.4 A.

In Fig. 10, experimental HEMT voltage and current waveforms are presented for two different conditions: (a) 200 V, 2.2 A and (b) 400 V, 4.4 A. As compared to the test results shown in Fig. 9, the waveforms are much cleaner because of the absence of current sensing loop induced noises. Notice that with the same R_g, both test conditions exhibit the same voltage slew rates under both turn-on and turn-off conditions. Their lengths of the plateau region are also identical. These experimental waveforms provide strong evidence that R_g is the dominant factor influencing voltage slew rates.

The inductor current is monitored with a 100-MHz current probe that comes with a 350-MHz oscilloscope. Because the inductor current remains nearly constant, the current probe's bandwidth is sufficient. However, for voltage measurements, the bandwidth appears to be insufficient in capturing the transient precisely. Nevertheless, given the limited voltage slew rates in the test, such a bandwidth is sufficient for observing performance.

Figs. 11 and 12 compare the simulation and experimental results under the same test conditions. During turn off, the gate-source voltage follows the gating command at 50 ns without any delay. However, the experimental waveform presents a slope that falls to the threshold voltage without displaying a clear plateau.

As the SPICE model adopts the conventional first-order equation to calculate the capacitance, their magnitudes are sigificantly lower than the actual value. This discrepancy suggests that the device input capacitance C_{iss} and the miller capacitance C_{rss} are much smaller than their actual counterparts. The CV curves in Fig. 13 clearly indicate such an underestimation within the SPICE model.

Similar underestimated output capacitance C_{oss} is also observed. With the model adopting a linear CV relationship, the voltage rise and fall characteristics also exhibit similar linearity. Although the mismatched device capacitances result in different gate charging curves, the switching delays and voltage slew rates agree reasonably well between simulation and experimental results.

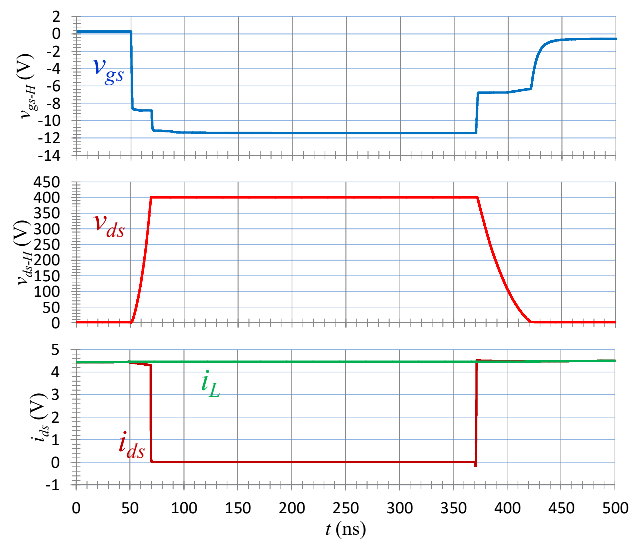


Fig. 11. Simulated key voltages and current waveforms for the direct drive gating circuit.

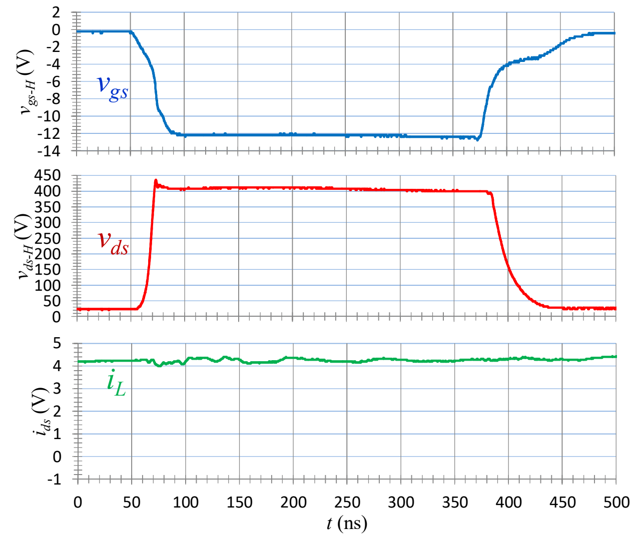


Fig. 12. Experimental results showing key voltage and current waveforms of direct driven GaN HEMT.

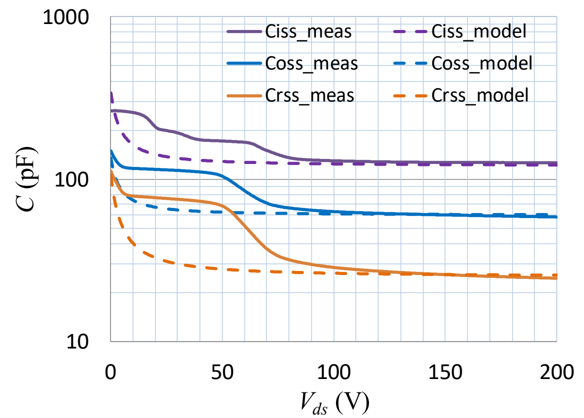


Fig. 13. CV curves comparison between first-order SPICE model and actual measurement.

Since the gating waveforms are relatively cleaner as compared to most report waveforms reported with cascode approaches, it is possible to further reduce the gate drive resistance, to reduce the plateau region and the associated voltage fall and rise times during both turn-on and –off periods, respectively.

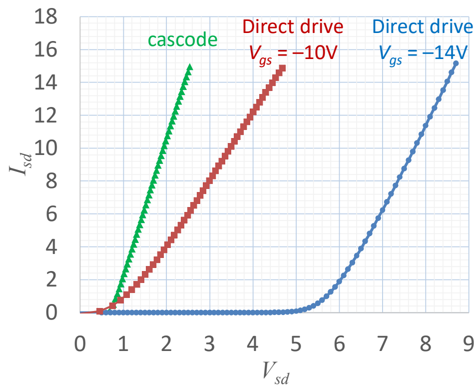


Fig. 14. Reverse conduction voltage drops with cascode and direct drive approaches.

VI. Conduction Voltage Drop Test with Direct Drive

Despite the direct-drive approach has demonstrated superior switching performance showcasing free from switching delay and gating noises, it does raised concerns regarding the reverse conduction voltage drop during freewheeling stage. Fig. 14 illustrates a comparison of the reverse conduction voltage drop V_{sd} as a function of the reverse conducting current I_{sd} under three conditions: (a) traditional cascode, (b) direct drive with $V_{gs} = -10$ V, and (c) direct drive with $V_{gs} = -14$ V. At 10-A load current, the voltage drops are 2 V, 3.5 V, and 7.8 V, respectively.

A higher gating voltage magnitude is generally desirable to enhance reverse voltage blocking, but it comes at the cost of a substantial increase in reverse voltage drop when the gating voltage magnitude is proportionally increased. If the synchronous rectification (SR) control signal is delayed, a high reverse conducting voltage can result in a significant reverse conduction loss. Such a loss is proportionally increased as a function of switching frequency, and thus the loss can be considered a part of switching related losses even though it is calculated as a conduction loss.

This reverse VI characteristic is a major concern when the synchronous rectification signal delay does not promptly adapt to reverse conductions. Consequently, the efficiency suffers considerably in high-frequency power conversions. Therefore, a design tradeoff is essential between selection of gating voltage magnitudes and the gating delay of the SR control signals, and even the choice between the conventional cascode and direct drive approaches for overall efficiency considerations.

VII. Conclusion

Through extensive computer simulations and hardware experiments, we have come to realize that the direct drive approach for GaN HEMT is not as straightforward as it initially anticipated. The in-house developed HEMT devices along with the flip chip package with solder balls have been instrumental in achieving low parasitic inductance layout and obtaining clean waveform measurements. However, the main challenge in experimental verification is to measure the device current. Two primary obstacles contribute to this difficulty: the added loop inductance, and the limited bandwidth of the current sensing traducer.

Despite the difficulty of measuring device current, the voltage measurements allow us to observe and validate some crucial aspects of HEMT device gating and switching. Key findings of the study can be summarized as follows.

- Compared to the conventional cascode approach, the direct drive eliminates MOSFET input capacitance induced delays, avoiding duty cycle changes.
- Under direct drive conditions, the gate-drive resistance plays a critical role not only in switching delays, but also in voltage slew rates. This controllable voltage slew rate clearly distinguish a key feature of from direct drive method from the conventional cascode approach.
- Simulation results indicate that the current rise and fall times are all in the sub-nanosecond range. As a result, measuring device current is not only limited by the additional parasitic inductance in the loop but also constrained by the sensor bandwidth.
- Highly nonlinear device capacitances cause smoothing effects on gate-source voltages during both turn-on and turn-off transitions, making the traditional plateau region not clearly evident in experimental waveforms, despite its existence.
- Gating voltage selection is crucial in managing the reverse conducting voltage drop. A voltage higher than V_{th} is necessary to ensure voltage blocking, but it will result in a much higher voltage drop that requires a swift synchronous rectification control to minimize the voltage drop related switching losses.

Overall, the study presented in this paper suggests that direct drive approach requires comprehensive design optimization involving gate drive resistance selection for switching delay and voltage slew rate control, careful circuit layout for parasitic component reduction, and precise timing control of synchronous rectification during freewheeling stage for efficiency considerations.

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