Fully Soft-Switching Modulation Methods for SRC-Unfolding Inverter

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ABSTRACT

Isolated inverters feature the freedom in voltage step-up/down, electrical safety, and modularity. Among them, pseudo-dc-link inverters have the advantage of high efficiency due to their single-stage structure. Traditionally, pseudo-dc-link inverters are based on pulse-width-modulated converters, which suffer from hard switching, the need for auxiliary components, and/or high current stresses. Meanwhile, the series resonant converter has been prevalent in past decades due to its simplicity and high efficiency. Therefore, it is intriguing to design a single-stage inverter based on a series resonant converter.

However, there are limited papers regarding such an inverter topology. To figure out the reason, basic modulation methods proposed or implied in the literature are summarized and evaluated through circuit simulation software. It turns out each basic modulation method has at least one critical drawback in modulation range, hard switching, and/or high current stresses.

Given the deficiencies in the basic modulation methods, a hybrid modulation method is proposed here. The proposed method combines variable-frequency modulation in the high-output region and short pulse-density modulation in the low-output region. In this way, all the aforementioned critical drawbacks can be greatly alleviated. The hybrid modulation method is compared to the basic modulation methods based on three design metrics: the rms value of the resonant current, the magnetic flux of the transformer, and the turn-off current. By these design metrics that directly related to power losses, the benefit of the proposed method in terms of efficiency can be explained. Moreover, a power loss model is also established to provide more

insights into the inverter's efficiency performance. It helps demonstrate how the selection of resonant tank and other factors affects the power loss distribution. Also, an inverter design procedure is introduced and a prototype is built to verify the proposed modulation method. The results show that the switching losses, especially the turn-on loss, can be well suppressed, and the losses in other passive components are well restrained. This implies the proposed method is suitable for high-frequency applications.

Other than efficiency, output waveform quality is also important for an inverter. However, the changing plant model makes the controller design difficult. Therefore, a third-order model established by other researchers has been adopted to identify the pole locations. In addition, a gain-varying method is proposed for the compensator to reduce the gain variance caused by different operating conditions. The experimental results show that without the gain-varying method, the inverter may have issues in slow tracking and/or instability.

Finally, in some scenarios, the inverter based on a series resonant converter can be regarded as a module. A multi-modular inverter can be formed by connecting the modules in an input-parallel-output-series configuration. In this case, a technique termed sequential waveform synthesis can be applied. The proposed technique can extend the region of variable-frequency modulation and shorten the region of short pulse-density modulation. This is beneficial to efficiency based on an analysis. With more than a certain amount of modules connected, the short pulse-density modulation can even be waived, which means the multi-modular inverter can be free from turn-on loss.

In summary, this dissertation focuses on developing modulation methods for inverters based on the series resonant converter. Soft-switching feature and high efficiency are the two top priorities. The analytic and experimental results are provided based on standalone applications.

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GENERAL AUDIENCE ABSTRACT

Inverters are an important part of a modern electric power system, as they convert dc electric power into ac electric power. In some applications, inverters with electrical insulation (isolated inverters) are preferred due to the need for engineering freedom, safety, and other reasons. However, each conventional isolated inverter has some of the following drawbacks: hard-switching in semiconductor devices, high circulating current, poor transformer utilization, and high complexity. These drawbacks limit the efficiency and compactness of an inverter system, making the system less attractive to practical applications.

An inverter based on a series resonant converter seems to be a solution because the series resonant converter is known for being simple and highly-efficient. However, there has yet to be a proper modulation method for it. Therefore, the main contribution of this dissertation is to propose a hybrid modulation method. With the proposed method, the inverter can operate with high efficiency. Furthermore, the hard-switching can be well suppressed, which means a high-frequency, compact design is possible.

Besides the theory of the proposed method, this dissertation also includes a power loss model, a hardware design procedure, and analytic comparisons with other methods. In addition, a digital approach to control the inverter is proposed. Without it, the output voltage waveform may be highly distorted.

Finally, another sequential control strategy is proposed in this dissertation for an integrated system. The integrated system is composed of multiple inverters based on a series resonant

converter. With the sequential control strategy, the overall output waveform quality of the integrated system can be improved.

To my parents,
Kang-Hsiung Yeh
Hui-Yin Chen

Acknowledgments

Back in winter 2014 when I first met Dr. Jih-Sheng Lai, I was a novice in power electronics. Nevertheless, he generously offered me the opportunity to enter the Ph.D. program and study under him. It always amazes me how broad his knowledge is, and how he never stops learning new technologies. I heartily appreciate the spirit of learning he taught me, and his support throughout these years.

Studying at Virginia Tech is a precious experience because the faculty put a lot of effort into guiding their students. I would like to thank my Ph.D. committee members: Dr. Khai Ngo, Dr. Mona Ghassemi, Dr. William Baumann, and Dr. Douglas Nelson. Their valuable comments from different perspectives encourage me to think deeper about the essence of my dissertation.

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The night before the final oral defense, my roommates Po-Jen Shih and Fu-An Lu fixed me a plate of chips and fried dough twist. This is one of the thousand moments my friends in Blacksburg warm my heart. I am thankful for all the colorful memories they brought me. Also, I

would like to dedicate my gratitude to my family: Mr. Kang-Hsiung Yeh, Mrs. Hui-Yin Chen, and Miss Chin-Yi Yeh. Their unconditional love is always my strongest support. Without them, this journey and accomplishment would be meaningless.

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Chih-Shen Yeh

12/4/2020 in Blacksburg

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Chapter 1

Introduction

1.1 Background

The future electrical grid is predicted to be integrated with various energy sources, including solar photovoltaics (PV), wind turbines, and other renewable energy sources [1]. This reduces our reliance on fossil fuel and other unsustainable energy sources, along with their negative impacts on the environment [2]. In the transformation of the electric power system, the development of inverter technologies plays an important role. For instance, the market of central PV inverters is projected to grow with a compound annual growth rate of 4% to 2026 [3]. The residential PV inverters are also promising, given the electricity generated by end-use solar PV (e.g., rooftop PV systems) is projected to reach 3.5% of the generation by 2050 in the United States, as shown in Figure 1.1 [4].

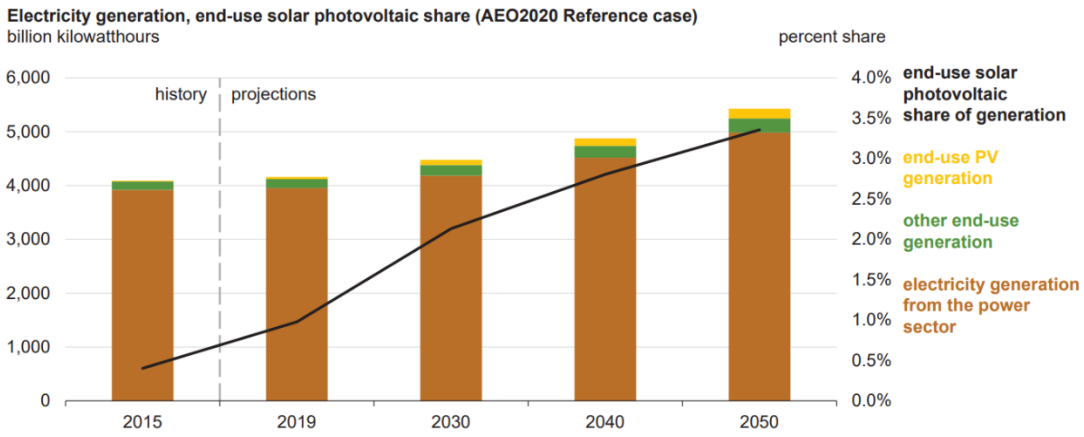
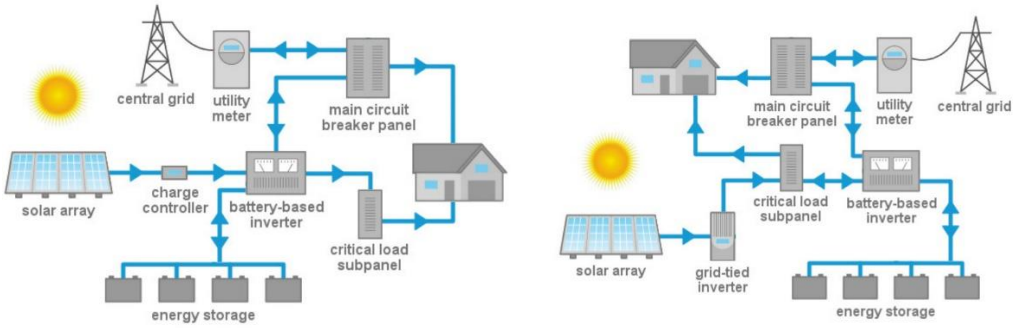


Figure 1.1. Electricity generation and end-use solar PV share [4].

Since the power generated from renewable energy sources may be inconsistent and not in accord with the demand, the significance of energy storage systems also rises [1]. There are multiple ways to integrate energy storage systems into the electrical grid. For instance, in residential applications, battery storage systems can be connected to a local dc or ac bus (e.g, Figure 1.2), and either option eventually requires an inverter to interface between the battery and the grid [5]-[6]. In utility-scale battery storage systems, an inverter is also needed to send out the power [7]. This exemplifies the diverse applications of inverters in emerging renewable energy technologies. Therefore, it is worthwhile to investigate the structure, topology, and control of inverters, for the sake of energy saving, cost reduction, and miniaturization.



(a) DC-coupled system. (b) AC-coupled system.

Figure 1.2. Conceptual diagrams of a residential PV system with an energy storage system installed [5].

1.2 Isolated Inverters

Line-frequency inverters condition a dc source into a 50-Hz or 60-Hz ac output. The common uses of them include utility interfacing and motor driving. In the applications of utility interfacing, an inverter ought to deliver energy to a utility grid or a local ac system, and thus the inverter can be further referred to as a grid-tied inverter or a standalone inverter [8]. In many cases out of these applications, having a transformer in an inverter system can be beneficial for three main reasons:

(i) Although galvanic isolation is not mandatory for all safety standards, it contributes to additional safety margins against electric shock and other hazards [9]. A common example is PV inverters, which may have the issue of ground leakage current if the inverters are not isolated [10]. As depicted in Figure 1.3, the return path of leakage current through panel capacitance (C_{pv}) could be interrupted if a transformer existed. In addition, a transformer can also block dc current injection to the grid [11], preventing nearby distribution transformers and grounding cables from overheating, corrosion, and other problems that affect system lifetime [12]-[13].

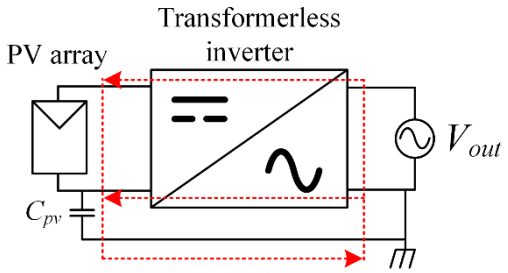


Figure 1.3. The leakage current path in a transformerless PV inverter.

(ii) In the design stage, the voltage conversion ratio can easily be adjusted with the transformer turns ratio. This is particularly helpful to high step-up applications like PV micro-inverters [14], medium-voltage grid-tied inverters [15]. On the other hand, some impedance source inverters (e.g., current source inverter, Z-source inverter) [16]-[17] and boost-type inverters [18]-[19] are also capable of voltage step-up, but their boost ratios are limited. Adding additional components is also essential for these transformerless step-up inverters.

(iii) By connecting transformer terminals in series/parallel, inverters can be tied together to share voltage/current stresses. Therefore, using transformers allows a large inverter system to be realized by multiple lower-scaled inverters. Such modularity equals the scalability of a system's voltage and power levels. Besides, it can often lead to a better output waveform and less switching losses [20].

Following the concept of isolated dc/dc converters, inverters with a transformer separating primary and secondary sides can be termed as isolated inverters. Traditionally, the isolation is achieved by adding a line-transformer to the back-end of an inverter system (cf., Figure 1.4). It is a simple solution, but the massive size and weight of line-transformers are apparent disadvantages [15]. Therefore, different approaches have been taken to replace the line transformers with high-frequency transformers.

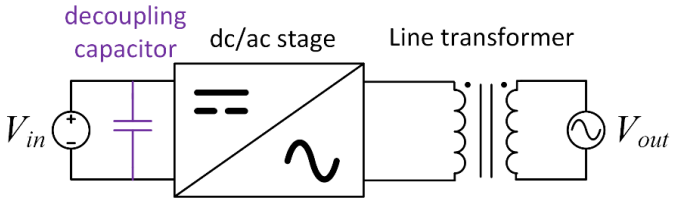


Figure 1.4. The system structure of line-transformer-tied inverters.

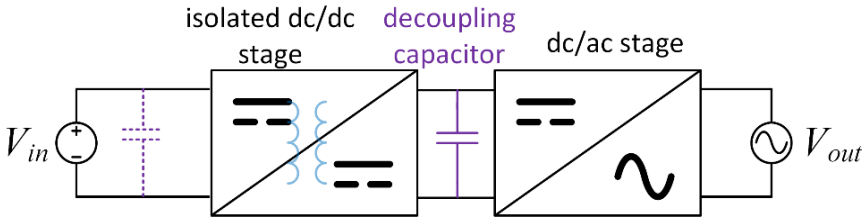


Figure 1.5. The system structure of high-frequency dc-link inverters.

The first approach is high-frequency dc-link inverters and the system structure is illustrated in Figure 1.5. The isolation of this type of inverters is provided by an isolated dc/dc stage, which can be an isolated dc/dc converters (e.g., flyback converters [21], LLC resonant converters [22], and dual active bridge converters [23]). One of the applications for this approach is inverters with input ripple requirements since it is possible to divert the ripple to the dc-link. The diversion not only changes the position of decoupling capacitors but also reduces the volume of capacitors needed for energy buffering [24]. Despite the potential for decoupling capacitor reduction, high-frequency dc-link inverters are not a perfect solution, since the system is composed of two stages.

The additional stage introduces more components, causing a more complex and less efficient circuit [25].

The second approach is high-frequency pseudo-dc-link inverters (PDIs) and the system structure is illustrated in Figure 1.6. Instead of maintaining a constant dc voltage, the isolated dc/dc stage generates an m-shaped rectified sinusoidal output waveform. This implies that the decoupling capacitors have to be placed at the source side, and the capacitors at a pseudo-dc-link ought to be limited. PDIs are favorable for high-efficiency design because they are typically referred to as single-stage inverters [25]. Such merit is attributed to the unfolder stage, where switches operate at the line frequency only to turn a rectified sinusoidal wave into a sinusoidal wave. The unfolder creates nearly zero switching losses. Therefore, the structure of the PDIs is attractive and adopted in this dissertation. The past research related to PDIs will be discussed in the next section.

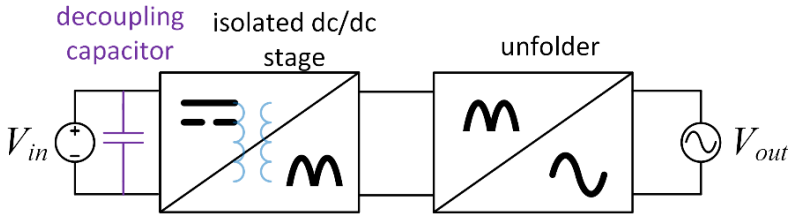


Figure 1.6. System structure of high-frequency pseudo-dc-link inverters.

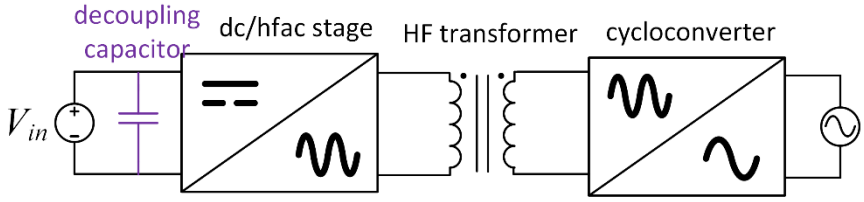


Figure 1.7. System structure of high-frequency ac-link inverters.

The third approach is high-frequency ac-link inverters. Their system structure is illustrated in Figure 1.7. Their ac/ac cycloconverter stage works similar to the rectifier (in the isolated dc/dc stage) plus the unfolder of PDIs. Yet, it is composed of bidirectional switches [26]-[27]. Therefore,

the inverters using this approach own similar characteristics with PDIs and are considered as a variation of PDIs.

1.3 State-of-the-Art Pseudo DC-Link Inverters

The performance of PDIs is dominated by its isolated dc/dc stage, and out of many options, flyback converters are the most popular due to simplicity [28]. The circuit topology of a basic flyback-converter-based PDI (FC-PDI) is plotted in Figure 1.8 with gate signals shown in Figure 1.9. S_1 to S_4 form the unfolder and each diagonal pair of switches work simultaneously to manage the direction of output current. The duty cycle of S_a determines the voltage gain of the flyback converter, and therefore it varies with the phase of the output voltage.

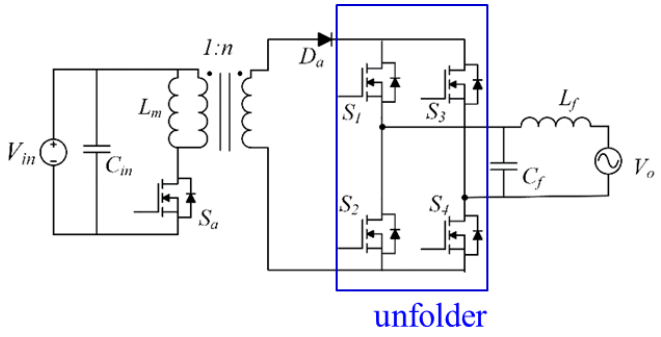


Figure 1.8. The topology of a basic flyback-converter-based PDI.

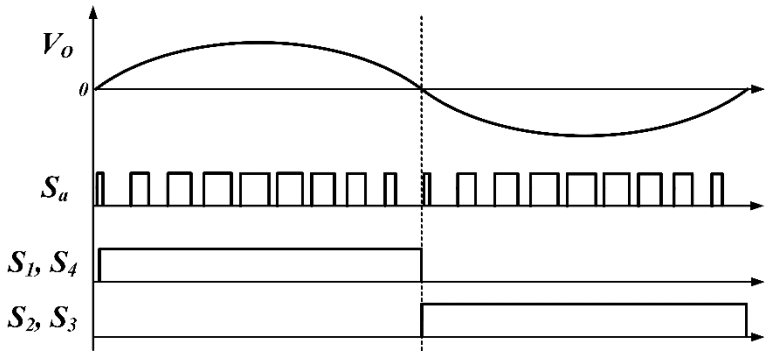
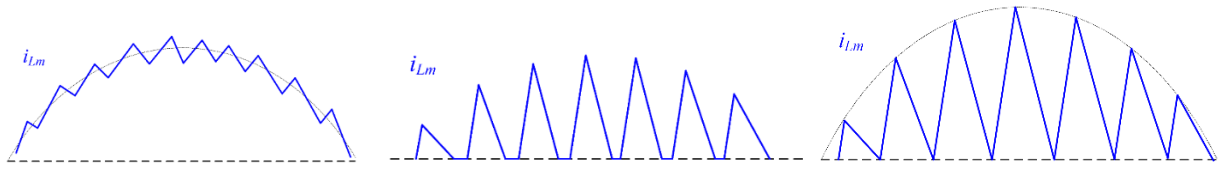


Figure 1.9. Gate signals of a basic FC-PDI.

The operation of an FC-PDI can be categorized into continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM). The mode of

operation is determined by the magnetizing current (cf., Figure 1.10), just like a regular flyback converter. In a CCM FC-PDI, a continuous magnetizing current has lower ripples, but S_a suffers from switching losses. Additionally, a right-half-plane (RHP) zero exists in the circuit, causing difficulty in controlling output waveforms [29]. In a DCM FC-PDI, S_a can turn on with zero-current-switching (ZCS), but the current ripples are higher. BCM can alleviate the current ripples in DCM, but variable-frequency control may be required [30]. In general, BCM and DCM are preferred due to the absence of the RHP zero and the chance to reduce device output capacitance (C_{oss}) loss by a quasi-resonant operation [31]-[32]. Once the magnetizing current becomes depleted, the C_{oss} of S_a resonates with the primary-side inductance, being discharged before S_a turns on. When S_a turns on, the remaining voltage of the C_{oss} is even lower with BCM, as voltage valley detection can be implemented [33]. However, the effect of the quasi-resonant operation is subject to the phase of the output voltage, and therefore only a part of the C_{oss} loss can be removed. Some methods have been proposed to enhance the performance of basic FC-PDIs. In [31], a BCM-DCM dual-mode strategy is developed to lessen current ripples while restraining the switching frequency range. In [32], bidirectional switches are utilized to replace the diode rectifier, allowing a reverse current flow that assists in soft-switching. However, the issue of the C_{oss} loss remains and affects inverter efficiency, even with the advanced methods.



(a) CCM. (b) DCM. (c) BCM.

Figure 1.10. The magnetizing current of a basic FC-PDI under different operation modes.

Besides the difficulty in choosing a proper operation mode, another issue basic FC-PDIs are faced with appears every time S_a turns off. When S_a turns off and cuts off the current path, the

transformer leakage inductance leads to a voltage spike across the drain-source of S_a. The consequent problems of overvoltage, noises, and power losses can be solved by using an active clamp (cf., Figure 1.11), but at the expense of one additional switch [34]. Furthermore, flyback converters always have the issue of poor transformer utilization, which makes losses hard to be suppressed [35]. The same drawback is inherited by FC-PDIs and therefore they are deemed to lack power capability. To process a higher power, FC-PDIs are often paralleled to share current stresses through interleaving techniques [36]-[37].

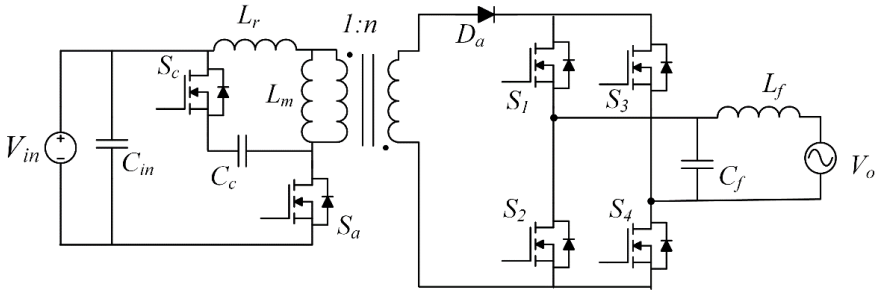


Figure 1.11. The topology of an active clamp FC-PDI.

Aside from FC-PDIs, there are many other pulse-width-modulated (PWM) converters being used in a PDI structure. Cuk converter has been selected in [38] due to a higher power capability and low input and output current ripples. However, the PDI based on a Cuk converter (cf., Figure 1.12) requires two more inductors than that of FC-PDIs, which causes additional power losses. In [39], a forward converter is selected (cf., Figure 1.13) considering its output inductor that can work as a current source. Although the discontinuity of the output current is eliminated, a third winding is essential for balancing the transformer. In [40], a PDI based on an isolated dual-active-bridge converter is proposed, as shown in Figure 1.14. It allows bidirectional power flow and features a wide soft-switching range. However, the wide range is achieved by extra commutation inductances (i.e., L_{c1} and L_{c2} in Figure 1.14), which result in an extra component count and high current stresses. Moreover, there is still a “dead-zone” where the turn-on loss

cannot be wiped out. Besides these converters, push-pull converters [41], full-bridge converters [42], isolated dual-boost converters [43], and zeta converters [44] have also been chosen as a base for PDIs.

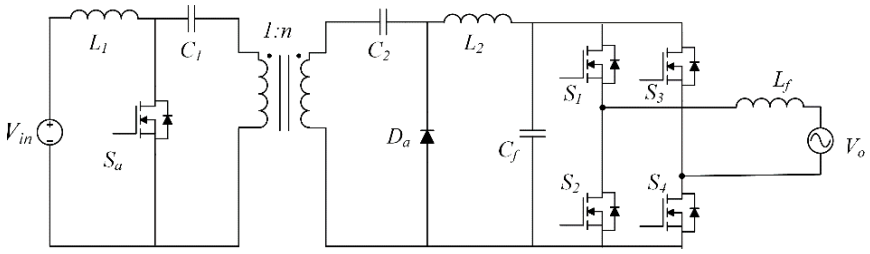


Figure 1.12. The topology of a PDI based on a Cuk converter.

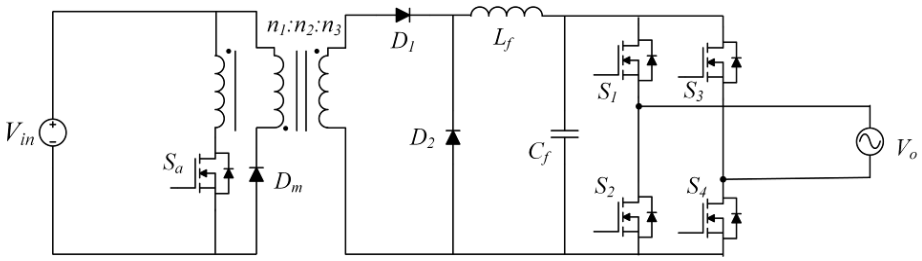


Figure 1.13. The topology of a PDI based on a forward converter.

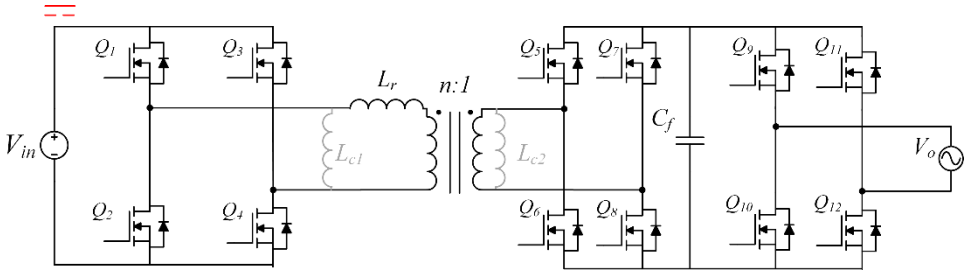


Figure 1.14. The topology of a PDI based on a dual-active-bridge converter.

A different choice of the base converter leads to a PDI with different characteristics. Nevertheless, the aforementioned PDIs based on PWM converters have some common drawbacks that are also seen in FC-PDIs:

(i) To avoid switching losses, most of the PWM converters have to operate in DCM/BCM, which yields high current stresses.

(ii) Even in DCM/BCM, the effect of soft-switching is subject to the phase of the output and/or the load condition. In other words, the PDIs still run with hard-switching in an interval every line-frequency cycle. This eventually stops the PDIs from efficiently operating at a high switching frequency.

(iii) Auxiliary circuits may be needed. More specifically, many PWM converters are vulnerable to transformer leakage inductance and require a snubber or an active clamp like the one used in Figure 1.11.

(iv) The transformer of the PDIs may be poorly utilized or require an additional circuit for flux balancing. This is especially of great concern for the most popular FC-PDIs.

Given the limitations of PWM converters, it is intriguing to investigate the PDIs based on resonant converters. Out of various kinds of resonant converters, a series resonant converter (SRC) seems like a proper candidate due to its simplicity and proven high efficiency in dc/dc applications [45]. It has one of the simplest resonant tank structures. Also, it performs the desired soft-switching without the need for an auxiliary circuit, being able to utilize transformer leakage inductance, and owns a rotationally symmetric hysteresis loop in the transformer [46]. As a result, it does not have the drawbacks (iii) and (iv) in the PWM PDIs. However, as the author kept digging into the literature, it appeared that there were only a few relevant papers and most of them provided limited analysis and experimental results.

1.4 Research Objectives and Dissertation Outline

Given the potential of SRC in PDI applications, it is worth further research despite limited past works. The research begins with revisiting the basic modulation methods directly or indirectly been used by others. Additional analysis and simulation works are performed to reveal the details and insights of these basic methods. However, it turns out that each basic method has at least a

crucial drawback, which is why using SRC has yet to be a prevalent option in PDIs. The works regarding the basic modulation methods will be covered in Chapter 2.

In order to restrain both conduction and switching losses, a hybrid modulation method is proposed in this dissertation. With the proposed method, the switching loss of the SRC in PDIs can be reduced substantially in full range, which facilitates high-frequency operation and size shrinking. The principle of the hybrid modulation method will be explained in Chapter 3. Next, a 400 V to 230 V_{ac}, 2 kW prototype is built and tested to verify the idea. The hardware design based on a power loss model will be discussed in Chapter 4.

Besides soft-switching and efficiency, output waveform quality is another key factor determining an inverter's performance. Due to the non-linearity of SRC, there is no simple equation to output a sinusoidal wave and therefore a feedback loop is essential for tracking a sinusoidal reference. In addition, a gain-varying method is applied to compensate for the non-linearity. The relevant modeling and control will be discussed in Chapter 5.

It has been previously mentioned that isolated inverters are capable of modularity. In Chapter 6, a control strategy will be introduced specifically for input-parallel-output-series multi-modular inverters composed of SRC-based PDIs. It extends the upper region of the hybrid modulation method, where the turn-on loss is eliminated.

In summary, the main research objective of this dissertation is to develop proper modulation methods for SRC-based PDIs and achieve the following characteristics:

- The switching loss has to be curtailed in full range.
- The current stress has to be maintained in a reasonable range.
- The losses in passive components should also be well restrained.
- The output waveforms should have low distortion.

Chapter 2

Basic Modulation Methods for SRC-Unfolding Inverters

2.1 SRC-Unfolding Inverters

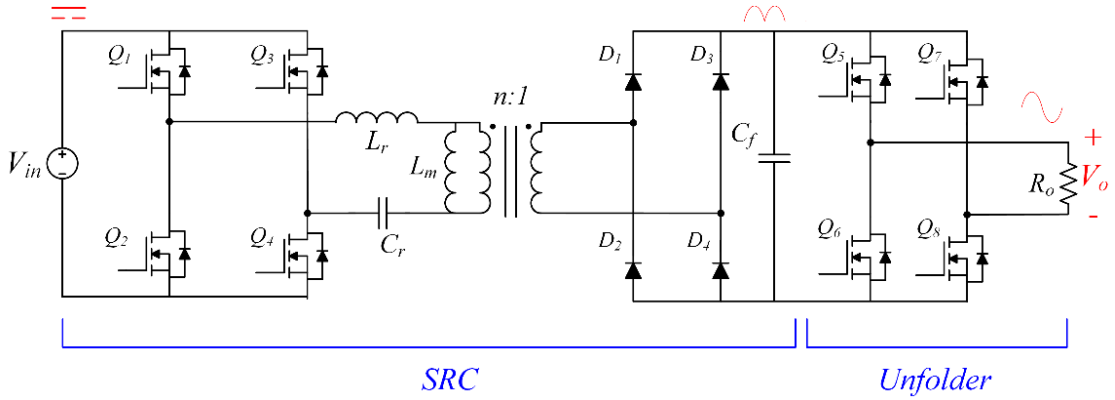


Figure 2.1. The topology of SRC-unfolding inverter.

The topology of a PDI based on an SRC is shown in Figure 2.1 and it is also coined as an SRC-unfolding inverter (SRCUI). $Q_1 – Q_4$ are primary-side high-frequency switches. $D_1 – D_4$ are secondary-side rectifiers. $Q_5 – Q_8$ are the line-frequency unfolder. C_f is an output filtering capacitor which has a rectified sinusoidal voltage across. A resonant inductor (L_r), a resonant capacitor (C_r), and the magnetizing inductance (L_m) of an *n:1* transformer form the resonant tank of the SRC. Traditionally, the circuit with such a resonant tank is regarded as an LLC resonant converter, but it is treated as an SRC in this dissertation for two main reasons. (i) Later with the proposed modulation method, the switching frequency (f_s) of the converter is higher than the series resonant frequency (f_r) defined in (2.1). Therefore, the converter operates in the above region ($f_s > f_r$), where LLC resonant converters and SRCs have similar characteristics [46]. (ii) Assuming the converter

to be an SRC can substantially simplify many mathematical expressions, leaving more concise and meaningful equations.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

2.2 Variable-Frequency Modulation

To generate a rectified sinusoidal voltage across C_f, the voltage gain of the SRC has to vary over time. The most typical way to vary the voltage gain is by changing f_s. Under the fundamental harmonic approximation [35], the equivalent circuit model of the SRC can be illustrated as Figure 2.2, where R_e is the equivalent load resistance defined in (2.2). The normalized voltage gain (M) can then be derived in (2.3), with the effective quality factor (Q_e) defined in (2.4). The gain curves are plotted in Figure 2.3(a) using the horizontal axis of the normalized switching frequency (f_s/f_r). By comparing to the gain curves of an LLC converter plotted in Figure 2.3(b), the similarity in the above region can be observed.

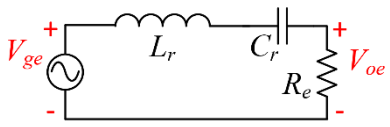
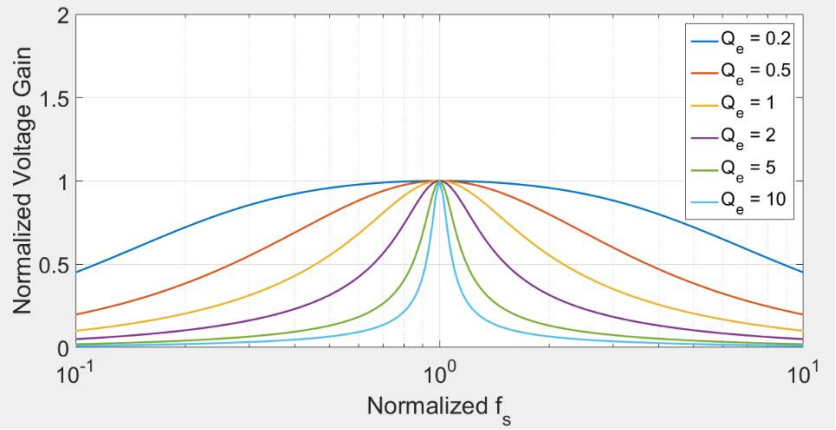


Figure 2.2. The equivalent circuit model of an SRC under the fundamental harmonic approximation.

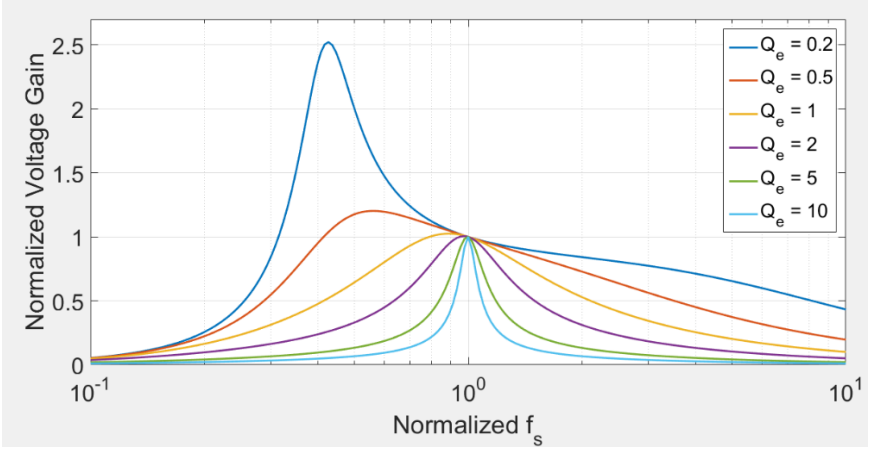
$$R_e = \frac{8}{\pi^2} n^2 R_o \tag{2.2}$$

$$M(f_s) = \frac{V_{oe}}{V_{ge}} = \left| \frac{R_e}{R_e + \frac{1}{j2\pi f_s C_r} + j2\pi f_s L_r} \right| = \frac{1}{\sqrt{1 + Q_e^2 \left(\frac{f_s}{f_r} - \frac{f_r}{f_s}\right)^2}} \tag{2.3}$$

$$Q_e = \frac{Z_r}{R_e} = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_e} \tag{2.4}$$



(a) SRC.



(b) LLC resonant converter with $L_m = 5L_r$.

Figure 2.3. Voltage gain curves of resonant converters.

In [47], the f_s of an SRCUI varies in the below region ($f_s < f_r$) to obtain ZCS for IGBT, but the test was only performed with the full load and the half load. The main reason is the load-dependency of SRCs. When the load decreases, Q_e also decreases and the gain curve becomes flatter (cf., Figure 2.3(a)). As a result, it is difficult to achieve low output voltage in a light load, even with the wide f_s range (20 kHz to 100 kHz) in [47]. In modern MOSFETs, zero-voltage-switching (ZVS) is preferred over ZCS [48], because the turn-on loss of one MOSFET is commonly a few times higher than the turn-off loss. Therefore, the variable-frequency modulation (VFM) in [49] is operated within the above region. However, it requires an unrealistic infinite f_s

to obtain a zero voltage gain, so a duty cycle control is used for the region with low absolute output voltage (i.e., low-output region). The mechanism of the duty cycle control in [49] is not explained at all, but a reasonable guess of it is a synonym for the phase-shift control introduced in the next section, according to another paper with the phrase "duty cycle control" [50]. In conclusion, an SRCUI using VFM has trouble modulating in a low-output region, whether it operates in the above region or the below region.

Table 2.1. Circuit parameters for simulation and analysis of modulation methods.

Parameters	Value	Parameters	Value
V_{in}	400 V	L_r	120 μH
V_{out}	230 V_{rms}	C_r	33.3 nF
P_{out}	0 – 2 kW	L_m	517 μH
n	1.2	f_r	79.6 kHz
C_f	10 μF for PDM, 1 μF for the others	f_s	80 – 250 kHz for VFM, 80 kHz for the others

The operation of VFM is simulated with PSIM software, using the parameters summarized in Table 2.1. The SRC in the inverter operates in the above region and has high-frequency waveforms shown in Figure 2.4, where T_s indicates the switching period and corresponds to the explicit definition of f_s in (2.5). The gate signal of Q_1 is always synchronous with Q_4 and complementary to Q_2 and Q_3. As a result, the SRC consistently delivers power to the unfolder. In addition, the resonant current pointed by the blue arrow flows through the C_{oss} of Q_1 – Q_4 and assists in the ZVS turn-on of Q_2 and Q_3. However, such a turn-off current is subject to two factors, the load current and f_s. In addition to a light-load condition, the turn-off current can also be

insufficient in a low-output region, since a high f_s results in an early turn-off timing. The quantitative analysis of the turn-off current will be provided in the next chapter.

$$f_s = \frac{1}{T_s} \tag{2.5}$$

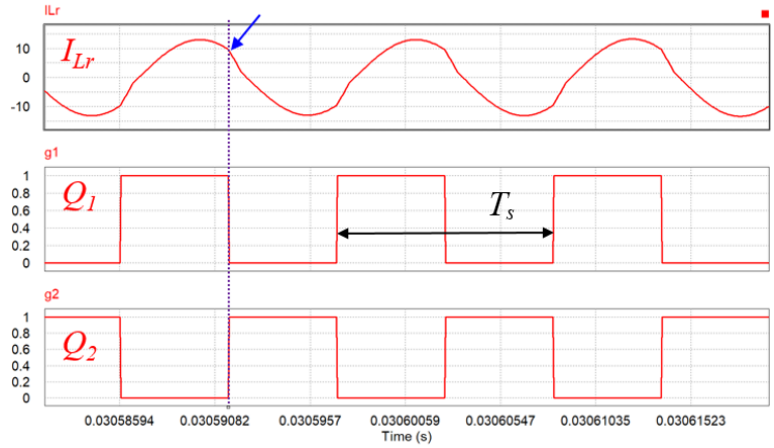


Figure 2.4. High-frequency waveforms of VFM in the above region.

The line-frequency waveforms of VFM are shown in Figure 2.5. Since the SRCUI loses both modulability and the ZVS in the low-output region, $Q_1 - Q_4$ are all turned off around the zero-crossing points (ZCP). Consequently, the SRC is turned off and a distortion appears in the output voltage waveform. The distortion can be alleviated by widening the range of f_s, but the upper limit of f_s cannot violate practical concerns like magnetic permeability, controller speed, device switching speed, gate driver capability, etc. Besides, the effect of raising the f_s range on reducing distortion gradually diminishes because the slope of the SRC's gain curves gradually flattens as well. Furthermore, the distortion is only worse in a light-load condition due to the previously mentioned load-dependency of SRCs. The degree of distortion can be evaluated by the total harmonic distortion (THD). With the full load in Figure 2.5, the output voltage has a THD of 4.2%, but with the half-load in Figure 2.6, the output voltage has a much higher THD of 10.4%. In summary, VFM can eliminate the turn-on loss without creating a circulating current, but it has

critical drawbacks in the low-output region. Therefore, it is very difficult for an SRCUI to meet the needs of practical applications by using only VFM.

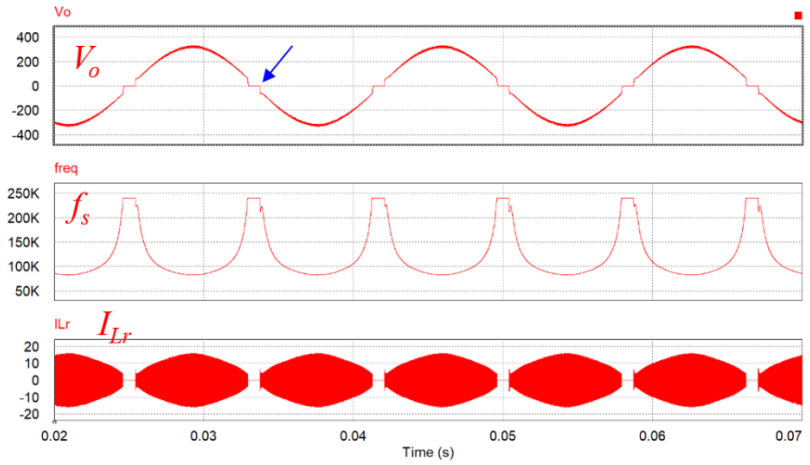


Figure 2.5. Full-load line-frequency waveforms of VFM in the above region.

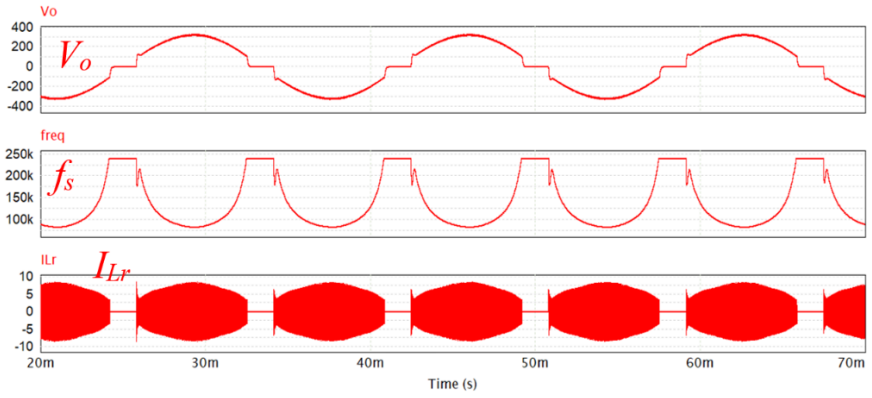


Figure 2.6. Half-load line-frequency waveforms of VFM in the above region.

2.3 Phase-Shift Modulation

The voltage gain of an SRC can also be decreased by making the operation of two primary-side half-bridges asynchronous. Creating a sinusoidal output accordingly is termed the phase-shift modulation (PSM). The gate signals of Q_1 and Q_2 are still complementary, and so do Q_3 and Q_4. However, both top switches turn on together for a duration of T_{ps} every cycle, and so do both bottom switches, as shown in Figure 2.7. When both top/bottom switches are on, the SRC cannot

import any power from the source, and thus a current circulates within the resonant tank and the switches. Therefore, PSM has higher current stresses than VFM and tends to be less efficient.

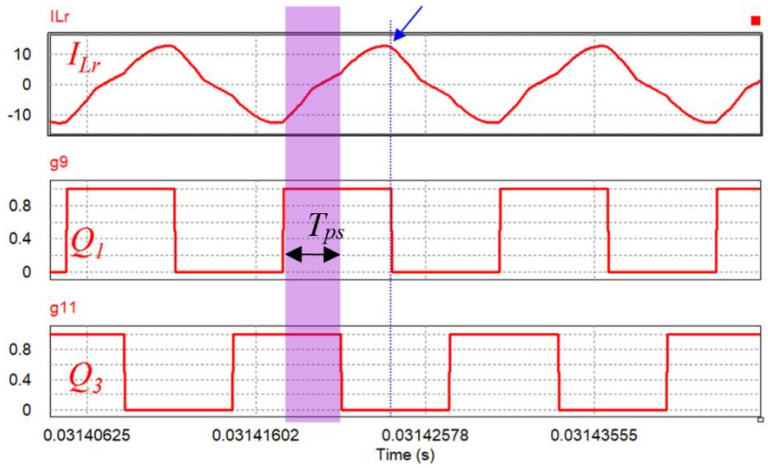


Figure 2.7. High-frequency waveforms of PSM.

When the phase shift duty (D_{ps}) defined in (2.6) is 0.5, Q_1 and Q_4 are totally out of phase and the SRC delivers zero power. Therefore, an SRCUI can easily reach the low-output region with PSM and does not have the problem of modulabilty like in VFM. The equation of D_{ps} has been derived in another paper regarding a phase-shifting dc-dc SRC [51]. After a few modifications, the equation of D_{ps} for the topology here is given in (2.7). In addition, the line-frequency waveforms of PSM are shown in Figure 2.8. The f_s is fixed to the f_r to obtain the maximum output voltage range. The waveform of the output voltage does not have the distortion near ZCP, and the SRC never totally shuts down. Due to the modulability in low-output regions, PSM has been used to support VFM in previously introduced [49]. Furthermore, PSM has been directly applied to an SRCUI [52] and its cycloconverter variant [53].

$$D_{ps} = \frac{T_{ps}}{T_s} \tag{2.6}$$

$$D_{ps} = 0.5 - \frac{\pi - \cos^{-1}\left(\frac{P_o T_s (2M-1) - 4V_{in}^2 C_r (1-M)}{P_o T_s + 4V_{in}^2 C_r (1-M)}\right)}{\omega_r T_s} \tag{2.7}$$

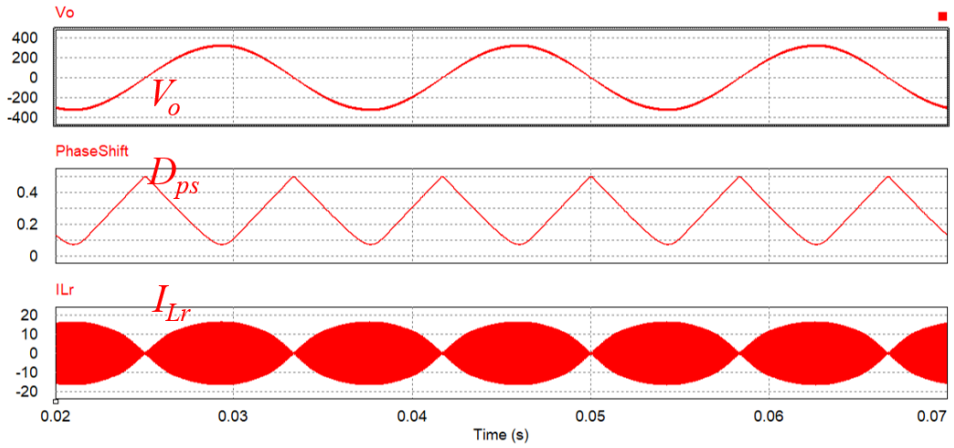


Figure 2.8. Line-frequency waveforms of PSM.

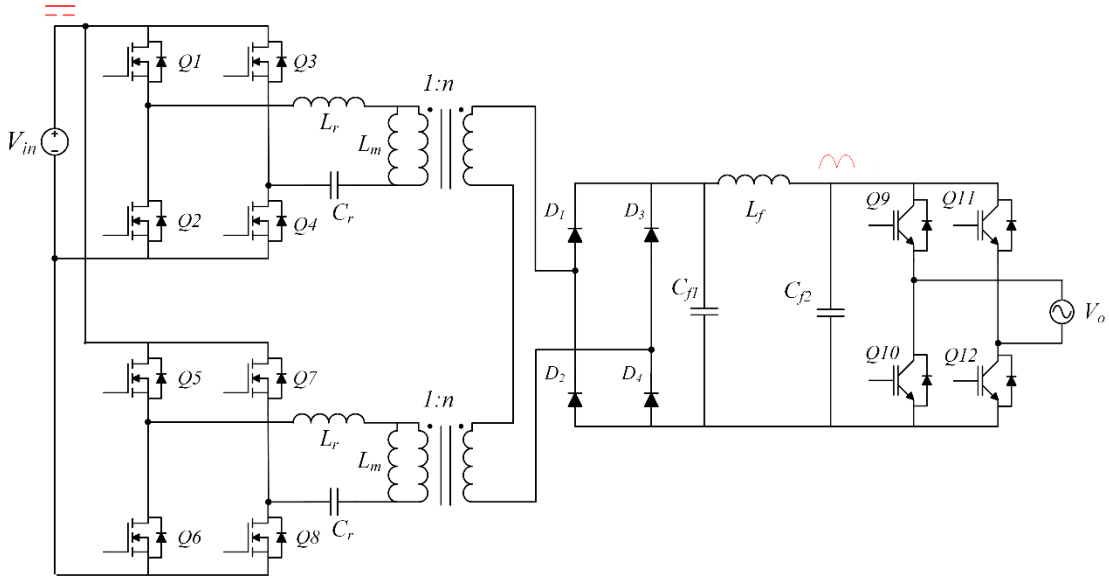


Figure 2.9. The topology of a series dual SRCUI.

Although PSM fixed the waveform quality issue in the low-output region, the issue of losing the ZVS remains [54]. The ZVS mechanism under PSM is the same as VFM. It also relies on a turn-off current (cf., the blue arrow in Figure 2.7) to discharge C_{oss} before devices turn on. When D_{ps} is higher, the turn-off timing is earlier and the turn-off current can be insufficient. Therefore, an SRCUI with PSM also fails to maintain the ZVS in a light-load condition or the low-output region. In order to ensure a full-range ZVS, a series-dual SRCUI is proposed [55], as shown in Figure 2.9. Instead of the phase-shifting between two half bridges, the series dual SRCUI utilizes

a phase-shifting between two SRCs to modulate the output. A full-range ZVS can be achieved by the turn-off current generated by L_m. However, at the moment of zero output, two secondary-side windings have voltages at opposite polarities and both SRCs still function. This reflects the fact that the phase-shifting between two SRCs induces a high circulating current. As a result, the peak efficiency of the prototype in [55] is only 91.1%. Aside from the high circulating current, the almost-doubled component count is another reason making the series dual SRCUI unattractive.

2.4 Asymmetrical Phase-Shift Modulation

Besides frequency-varying and phase-shifting, other advanced methods have been developed for dc-dc applications. These methods are generally a combination and/or a variant of frequency-varying and phase-shifting. An example can be found in [56] with the high-frequency waveforms shown in Figure 2.10. Similar to PSM, both top/bottom switches may jointly turn on to restrain the output power. However, the gate signals within a half-bridge are no longer equal since the top switches are on for a shorter duration. Therefore, modulating an SRCUI with such a control scheme is termed the asymmetrical phase-shift modulation (APSM). Under APSM, T_{on} is the variable used to modulate the output. Q_2 and Q_4 turn off when resonant current (I_{Lr}) almost reaches zero. Consequently, Q_2 and Q_4 can turn off with ZCS but a current sensor is needed.

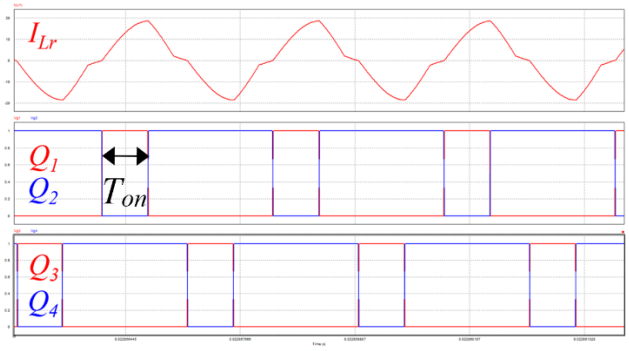


Figure 2.10. High-frequency waveforms of APSM.

The line-frequency waveforms of APSM are shown in Figure 2.11. As the SRCUI moves toward the low-output region, T_{on} gradually decreases and thus switching frequency increases. Therefore, APSM also has difficulty in modulating in the low-output region. Furthermore, the turn-off current for the ZVS again can be insufficient when T_{on} is too short. In summary, the operation principle and characteristics of APSM are a mixture of PSM and VFM. This includes the common drawback of the two previous methods: losing the ZVS in the low-line region or a light-load condition. The case of APSM exemplifies that other advanced control schemes may create some different advantages and features. But in general, it is hard to completely mitigate the turn-on loss from an SRCUI, as long as Q_1 – Q_4 keep switching.

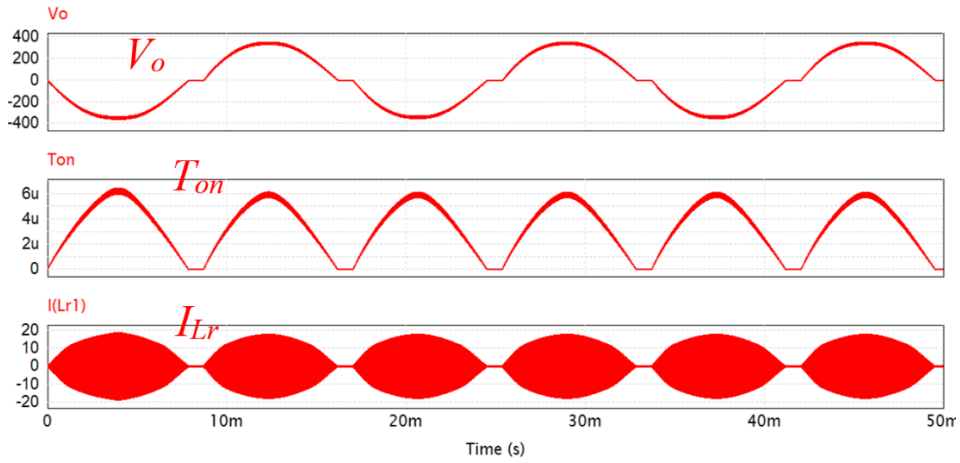


Figure 2.11. Line-frequency waveforms of APSM.

2.5 Pulse-Density Modulation

Given the limited soft-switching function in VFM, PSM, and APSM, an alternative approach — the pulse density modulation (PDM) — draws the attention. In PDM, the blank time (T_{blank}) is added between two batches of consecutive high-frequency gate signals, as shown in Figure 2.12. During the blank time, Q_1 – Q_4 are all turned off to prevent power delivery, so a longer T_{blank} leads to a lower output voltage. The f_s of PDM is also same as the f_r, but the switching losses

can be reduced since no switching event occurs during the blank time. In principle, the mechanism of switching-loss reduction in PDM does not rely on the turn-off current, so efficiency does not suffer from a light-load condition or the low-output region. Switching losses are almost gone near ZCP since the pulse density (ρ_p defined in (2.8)) is almost zero.

$$\rho_p = \frac{T_{pulse} - T_{blank}}{T_{pulse}} \tag{2.8}$$

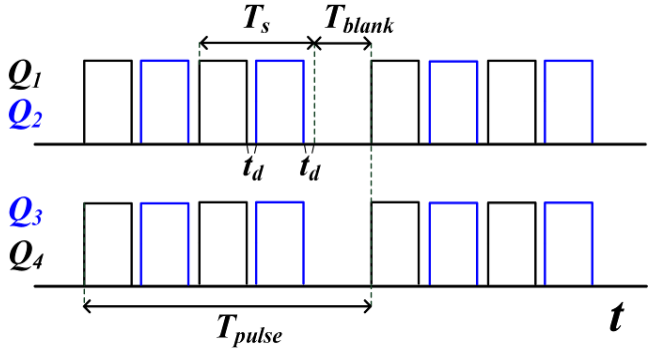


Figure 2.12. High-frequency gate signals of PDM.

Traditionally, the idea of the blank time is used in the burst mode control for improving dc-dc SRC's light-load efficiency [57]-[58]. It is uncommon to find the idea being used to modulate an inverter output, especially for SRCUIs. The closest studies found in the literature utilize PDM for cycloconverters based on an SRC [59]-[60], but they provide limited circuit waveforms or analysis of power loss. Therefore, an SRCUI using the parameters in Table 2.1 is simulated with PDM and the results are shown in Figure 2.13. Ideally, PDM has no trouble in terms of modulability, but the output voltage waveform shows tremendous ripples, even with the output filtering capacitor (C_f) being added to ten times. The reason behind the ripples can be traced back to the I_{Lr}, which has a wave envelope trending against the output voltage. Besides, the peak I_{Lr} is much higher than in other modulation methods. The consequent high conduction loss can harm efficiency drastically. Since L_r and C_r are connected in series, the peak resonant voltage (V_{Cr})

is also tremendous and even exceeds five times the input voltage. This implies high-tolerance components are required to handle such high energy in the resonant tank.

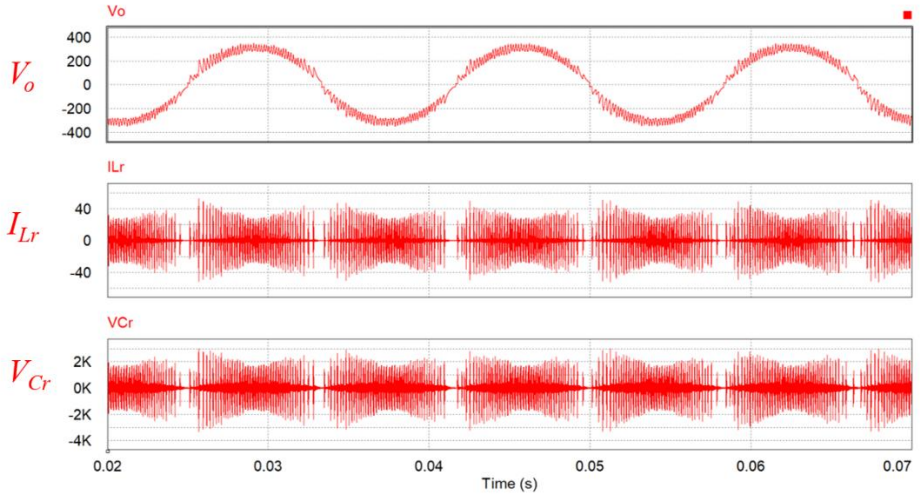


Figure 2.13. Line-frequency waveforms of PDM.

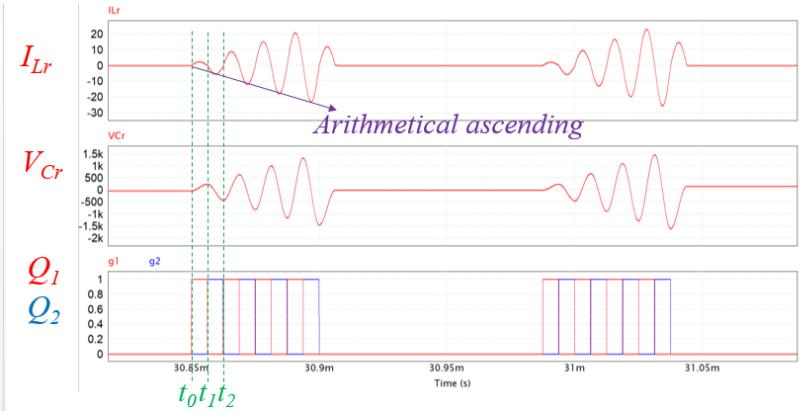


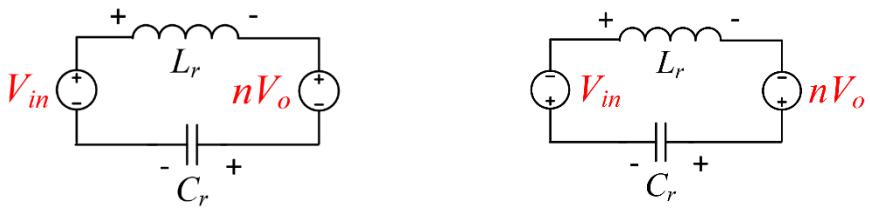
Figure 2.14. High-frequency resonant tank waveforms of PDM.

The high I_{Lr} and V_{Cr} make PDM unattractive to practical applications, so it is important to get to the bottom of the phenomenon. The waveforms of the resonant tank are zoomed in and shown in Figure 2.14. Before t_0, the SRC is shut down so I_{Lr} and V_{Cr} can be assumed zero. From t_0 to t_1, Q_1 and Q_4 are on and the equivalent circuit model of the SRC is plotted in Figure 2.15(a). The state equations are listed in (2.9) and show that the peak V_{Cr} reaches $2\cdot(V_{in}\text{-}nV_o)$. Next, from t_1 to t_2, Q_2 and Q_3 are on and the equivalent circuit model of the SRC becomes Figure 2.15(b).

Since I_{Lr} and V_{Cr} are zero and $2\cdot(V_{in}\text{-}nV_o)$ respectively at t_1, the state equations can be derived in (2.10). In this interval, the peak V_{Cr} is increased to $4\cdot(V_{in}\text{-}nV_o)$. The remaining resonant tank energy at the end of an interval results in a higher peak V_{Cr} and I_{Lr} in the next interval. Therefore, if the gate signals keep firing, the peak V_{Cr} will be $6\cdot(V_{in}\text{-}nV_o)$, $8\cdot(V_{in}\text{-}nV_o)$ and then keep ascending. At a certain point, the huge I_{Lr} will impact the output voltage and nullify (2.9) and (2.10). But even with a few repetitions, the resulting high V_{Cr}, I_{Lr}, and output voltage ripples are already unbearable. In addition, it is clear from (2.9) and (2.10) that the resonant amplitude is larger when the output voltage is lower. This explains why the highest I_{Lr} and V_{Cr} appear near the ZCP. In summary, despite an independent switching-loss reduction mechanism, PDM is not favorable to practical applications. It inherently generates high I_{Lr} and V_{Cr}, stressing the resonant tank components and the semiconductor devices.

$$\begin{cases} i_{Lr}(t) = \dfrac{V_{in} - nV_o}{Z_r}\sin(\omega_r(t-t_0)) \\ v_{Cr}(t) = (V_{in} - nV_o) + (V_{in} - nV_o)\cos(\pi - \omega_r(t-t_0)) \end{cases} \tag{2.9}$$

$$\begin{cases} i_{Lr}(t) = \dfrac{3(nV_o - V_{in})}{Z_r}\sin(\omega_r(t-t_1)) \\ v_{Cr}(t) = (nV_o - V_{in}) + 3(V_{in} - nV_o)\cos(\omega_r(t-t_1)) \end{cases} \tag{2.10}$$



(a) From t_0 to t_1. (b) From t_1 to t_2.

Figure 2.15. Equivalent circuit models of the SRC in PDM.

2.6 Summary

Table 2.2. Comparison of basic modulation methods for SRCUIs.

	VFM	PSM	APSM	PDM
Variable	T_s	T_{ps}	T_{on} (and T_s)	T_{blank}
Modulation range	Invalid in the low-output region	Full	Invalid in deep low-output region	Full
Switching loss reduction	ZVS except for the low-output or light-load region	ZVS except for the low-output or light-load region	ZVS except for low-output or light-load region, extra ZCS	Equivalently low switching frequency
Resonant current	Medium	High	Between PSM and VFM	Very high
Comment	Varying frequency is a traditional way to control an SRC	The only practical basic method	A mixture of PSM and VFM	Pulse-density control is traditionally used for improving light-load dc-dc efficiency

The characteristics of different basic modulation methods are summarized in Table 2.2. The table indicates that each basic method has at least one critical drawback written in red. The problems in VFM, APSM, and PDM are especially serious, since their output waveforms may have the ZCP distortion or the tremendous ripples. Failing to generate a proper sinusoidal output means an inverter fails its basic function, and from this perspective, PSM is the only practical basic method. However, the development of PSM in high-frequency power electronics is limited by its deficiency in the ZVS range.

Given the drawbacks of the basic methods, an alternative modulation method is needed to fulfill the potential of SRCUIs. This new method has to maintain a decent output waveform quality, restrain the resonant current, and curtail the switching loss across an entire operating range. In the next chapter, such a new method will be introduced and then compared to the basic methods. Therefore, more quantitative comparisons regarding the basic modulation methods can be found in the next chapter.

Chapter 3

Proposed Hybrid Modulation Method

3.1 General Description

In view of the critical drawbacks in Table 2.2, a hybrid modulation method (HMM) is proposed here to combine the merits of different basic methods. VFM is chosen as the base of HMM because it creates the least resonant current. To overcome the hard-switching in the low-output or light-load region, a short pulse-density modulation (SPDM) is proposed and applied. The gate signals of the proposed VFM-SPDM hybrid modulation method are plotted in Figure 3.1 over one line-frequency cycle. By the nature of symmetry, the operation between t_m and t_z is enough to represent the entire cycle. The output phase angle (θ_l) is defined as 0˚ at t_m and 90˚ at t_z. The controller switches between VFM and SPDM at the moment t_b, which corresponds to the θ_l of θ_b. Therefore, the boundary angle (θ_b) should be between 0˚ and 90˚. The operation of VFM and SPDM will be introduced in the following sections in detail.

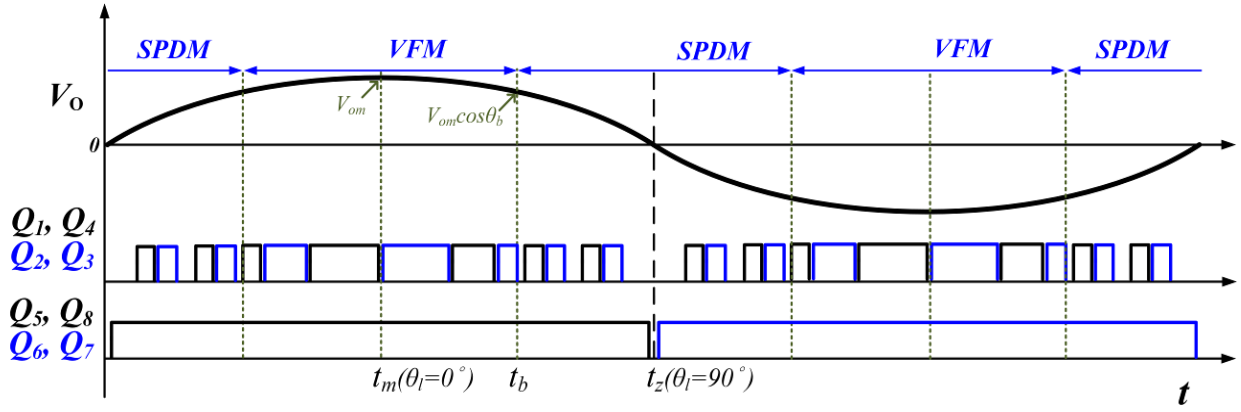


Figure 3.1. Gate signals of the proposed HMM.

To provide a general view of the operation of HMM, the steady-state waveforms of SRCUI over 3 line-frequency cycles are also demonstrated in Figure 3.2. Figure 3.2 is generated in a PSIM simulation using the circuit parameters in Table 2.1.

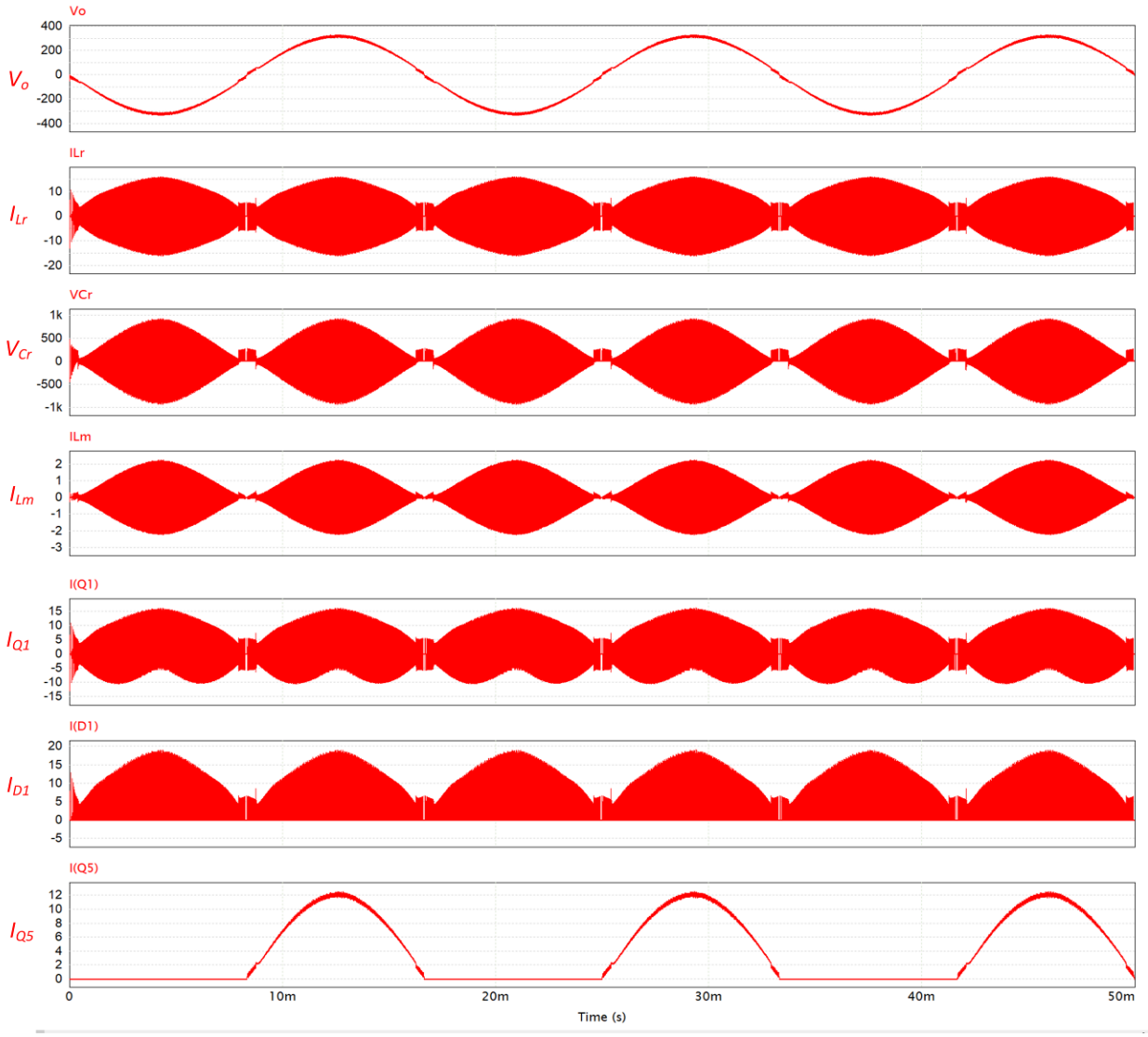


Figure 3.2. Simulated steady-state waveforms of an SRCUI under HMM.

3.2 Operation in Variable-Frequency Modulation Region

The operation of VFM is the same as Section 2.2, but more analytical details are provided here. Figure 3.3 is the high-frequency waveforms of the SRC. In such a short duration, the voltage across the output filtering capacitor (v_{Cf}) is assumed to be constant. The operation can be divided

into several intervals and the circuit status of each interval is shown in Figure 3.4. Due to symmetry, only the positive half of a high-frequency cycle is discussed. In addition, the inverter operates in the positive line cycle (Q_5, Q_8 are on), but Figure 3.3 is also valid for the negative line cycle.

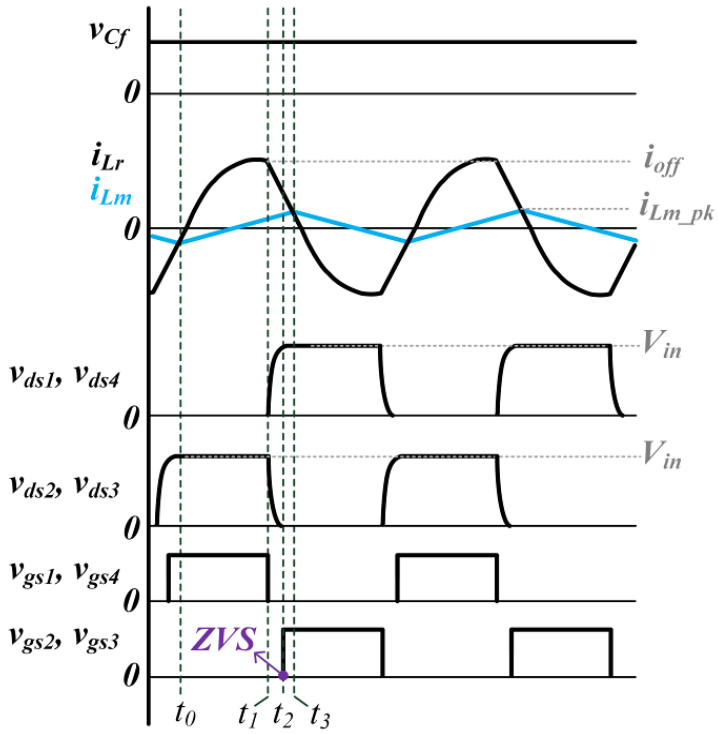
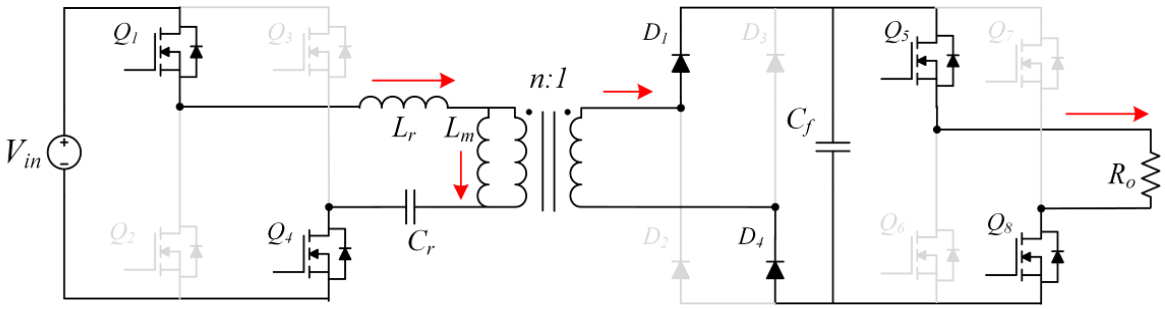
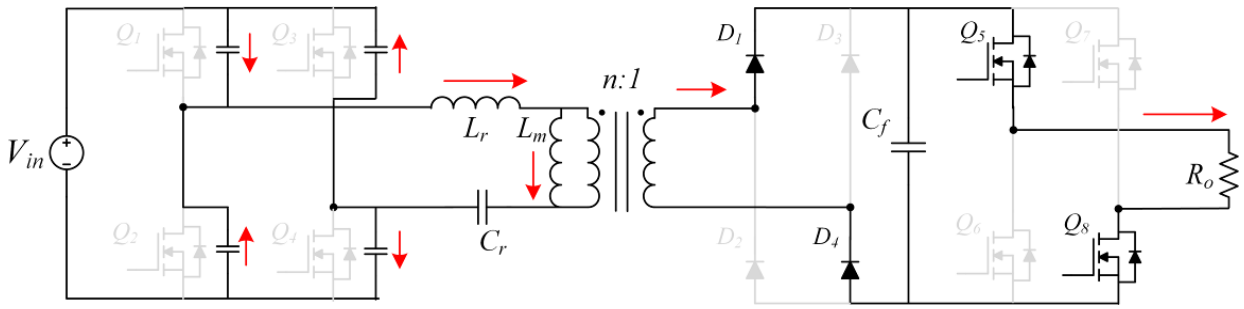


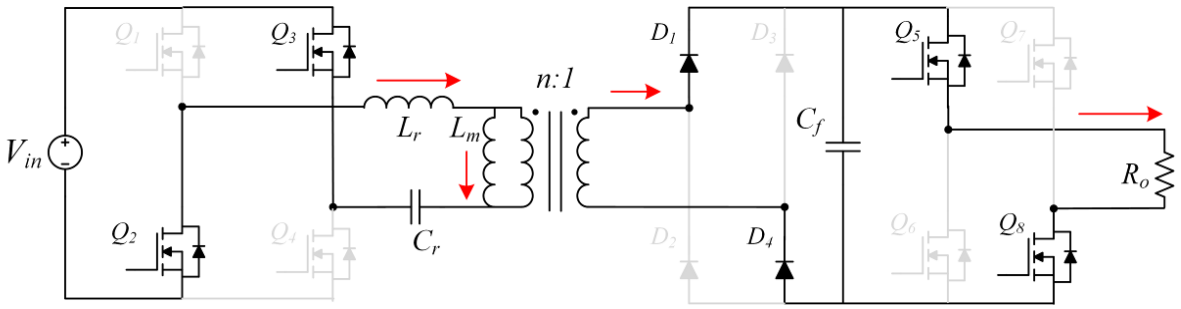
Figure 3.3. High-frequency waveforms in the VFM region.



(a) *Interval* [t_0, t_1].



(b) *Interval* [*t1*, t_2].



(c) *Interval* [t_2, t_3].

Figure 3.4. Circuit status of each interval in the VFM region.

Interval [t_0, t_1]: The resonant tank is charged in this interval, and power is delivered to the load. The equivalent circuit of SRC is the same as Figure 2.15(a), but the initial conditions are different. At t_0, I_{Lr} equals the peak of the magnetizing current, so the initial condition can be written in (3.1). Next, the zero-crossing-point of I_{Lr} is close to t_0, so it is fair to assume V_{Cr} at t_0 equals the peak of the resonant capacitor voltage, which can be estimated by (3.2). (3.2) is derived by assuming average I_{Lr} in the positive half cycle equals the average input current, which can be estimated by the output voltage (V_o), the input voltage (V_{in}), and the load resistance (R_o) [51].

$$i_{Lr}(t_0) = -i_{Lm\_pk} = \frac{-nV_o}{4 f_s L_m} \tag{3.1}$$

$$v_{Cr}(t_0) = -\Delta v_{Cr} = \frac{-V_o^{\,2}}{4V_{in} C_r R_o f_s} \tag{3.2}$$

The state equations of Figure 2.15(a) are written in (3.3). The solutions using (3.1) and (3.2) can be found in (3.4), with the angular resonant frequency (ω_r) and characteristic impedance (Z_r) defined in (3.5) and (3.6).

$$\begin{cases} V_{in} = nV_o + v_{Cr}(t) + L_r \dfrac{di_{Lr}(t)}{dt} \\ i_{Lr}(t) = C_r \dfrac{dv_{Cr}(t)}{dt} \end{cases} \tag{3.3}$$

$$\begin{cases} i_{Lr}(t) = \sqrt{\left(\dfrac{V_{in} - nV_o + \Delta V_{Cr}}{Z_r}\right)^2 + {i_{Lm\_pk}}^2} \bullet \sin\left(\omega_r(t - t_0) - \tan^{-1}\left(\dfrac{Z_r i_{Lm\_pk}}{V_{in} - nV_o + \Delta V_{Cr}}\right)\right) \\ v_{Cr}(t) = -\sqrt{(V_{in} - nV_o + \Delta V_{Cr})^2 + {i_{Lm\_pk}}^2 {Z_r}^2} \bullet \cos\left(\omega_r(t - t_0) - \tan^{-1}\left(\dfrac{Z_r i_{Lm\_pk}}{V_{in} - nV_o + \Delta V_{Cr}}\right)\right) + V_{in} - nV_o \end{cases} \tag{3.4}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{3.5}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{3.6}$$

Interval [t_1, t_2]: At t_1, Q_1 and Q_4 turn off so a current flows through the C_{oss} of the primary-side switches. The C_{oss} of Q_2 and Q_3 ought to be fully discharged before t_2 for the sake of ZVS turn-on. Conventionally, such a ZVS condition is expressed as (3.7) [61], where the dead time (t_d) and the turn-off current (i_{off}) are the two major factors. The latter one is especially crucial since it changes over the circuit's working conditions. After the C_{oss} of Q_2 and Q_3 are depleted, the current flows through the body diode of Q_2 and Q_3 instead and therefore their drain-source voltage can be regarded as zero.

$$i_{off}(t_2 - t_1) = i_{off} t_d \geq 2C_{oss} V_{in} \tag{3.7}$$

Interval [t_2, t_3]: Since the drain-source voltage of Q_2 and Q_3 is zero, they turn on with ZVS at t_2. In this interval, the input voltage source is reversely connected to the SRC, as shown in Figure 3.5. As a result, I_{Lr} decreases rapidly until it meets the magnetizing current. This process can also

be modeled by state equations (3.8) and the solutions (3.9). Note that the initial conditions applied are $i_{Lr}(t_1)$ and $v_{Cr}(t_1)$ because the device voltage commutation in the previous interval generally takes a very short time.

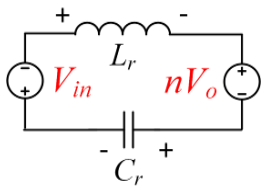


Figure 3.5. Equivalent circuit model of the SRC in interval [t_2, t_3] of VFM region.

$$\begin{cases} 0 = V_{in} + nV_o + v_{Cr}(t) + L_r \dfrac{di_{Lr}(t)}{dt} \\ i_{Lr}(t) = C_r \dfrac{dv_{Cr}(t)}{dt} \end{cases} \tag{3.8}$$

$$\begin{cases} i_{Lr}(t) = -\sqrt{\left(\dfrac{V_{in} + nV_o + v_{Cr}(t_1)}{Z_r}\right)^2 + i_{Lr}{}^2(t_1)} \bullet \sin\left(\omega_r(t-t_1) - \tan^{-1}\left(\dfrac{i_{Lr}(t_1)Z_r}{V_{in} + nV_o + v_{Cr}(t_1)}\right)\right) \\ v_{Cr}(t) = \sqrt{(V_{in} + nV_o + v_{Cr}(t_1))^2 + i_{Lr}{}^2(t_1)Z_r{}^2} \bullet \cos\left(\omega_r(t-t_1) - \tan^{-1}\left(\dfrac{i_{Lr}(t_1)Z_r}{V_{in} + nV_o + v_{Cr}(t_1)}\right)\right) - V_{in} - nV_o \end{cases} \tag{3.9}$$

Since *Interval* [t_0, t_1] occupies most of the period, the power transfer under VFM is efficient. Furthermore, the equation of i_{off} can be simplified to (3.10) if we assume *Interval* [t_1, t_2] and *Interval* [t_2, t_3] are negligible. In (3.10), ΔV_{Cr} and i_{Lm_pk} change over V_o, and V_o changes over f_s. Therefore, (3.10) can be plotted as a function of f_s, as demonstrated in Figure 3.6. The following parameters are used for generating Figure 3.6: V_{in} = 400 V, n = 1.2, L_r = 120 μH, C_r = 33.3 nF, L_m = 400 μH and R_o = 26.5 Ω for the 100% load condition. All the curves meet at f_r, where i_{off} solely relies on the load-independent magnetizing current. As f_s goes up, most of the curves first rise due to an earlier turn-off, until they reach the peak. But after that, i_{off} gradually decreases due to the shrinking amplitude in (3.10). Besides, an earlier turn-off is no longer helpful after f_s goes beyond roughly $2f_r$. i_{off} is also subject to the load condition since R_o affects V_o and ΔV_{Cr}. Such an effect of

loads is exemplified in Figure 3.6 and it is quite intuitive. The lighter the load is, the lesser the turn-off current is.

$$i_{off} = \sqrt{\left(\frac{V_{in} - nV_o + \Delta V_{Cr}}{Z_r}\right)^2 + {i_{Lm\_pk}}^2} \bullet \sin\left(\frac{\omega_r}{2f_s} - \tan^{-1}\left(\frac{Z_r i_{Lm\_pk}}{V_{in} - nV_o + \Delta V_{Cr}}\right)\right) \tag{3.10}$$

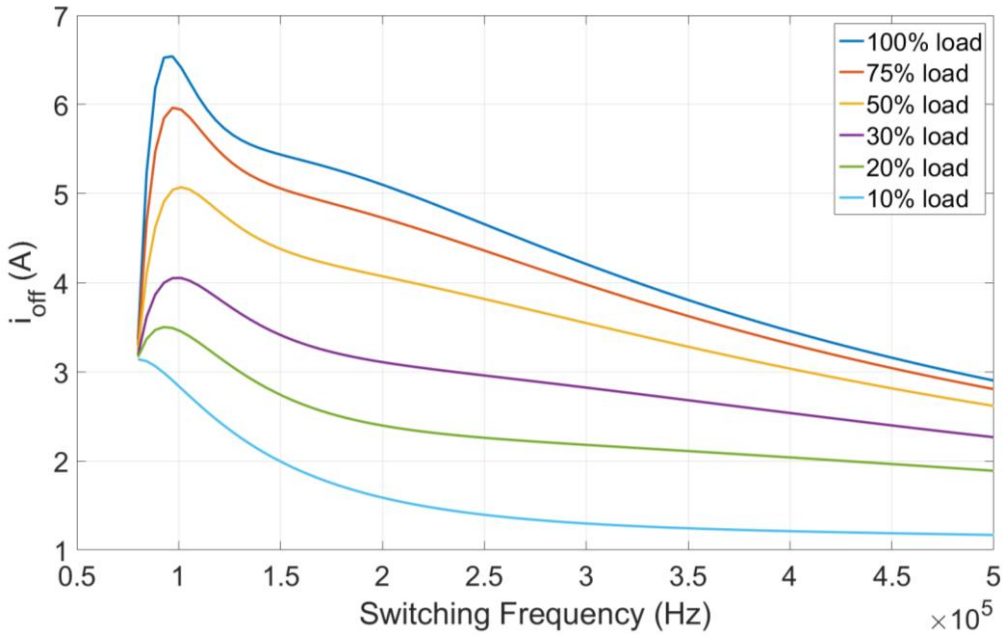


Figure 3.6. The turn-off current (i_{off}) under different loads and switching frequencies.

The voltage gain curves under VFM have already been plotted in Section 2.2. Nevertheless, calculating f_s at a given V_o or θ_l is also significant for the modeling purpose. To do so, an explicit expression can be derived from (2.3) and listed in (3.11). If a more accurate estimation is needed, L_m should be taken into account. But in that case, finding numerical solutions is the better approach as the explicit solution becomes overly tedious.

$$f_s = f_r \sqrt{1 + \frac{1 - M^2}{2M^2 Q_e^2} + \frac{1}{2}\sqrt{\frac{4(1 - M^2)}{M^2 {Q_e}^2} + \frac{(1 - M^2)^2}{M^4 {Q_e}^4}}} \tag{3.11}$$

Based on (3.11), the curves of f_s over θ_l are plotted in Figure 3.7. At a fixed f_s, θ_l is higher with a larger Q_e. For instance, θ_l is 79˚ at f_s of 250 kHz when Q_e = 2.0, but it drops to 52˚ when Q_e = 0.5. Consequently, the output voltage can reach a lower level at a heavier load. This paraphrases

the lack of modulability of VFM in light-load conditions. To sum up, VFM has critical drawbacks in light-load and low-output regions in terms of the ZVS feature and modulability.

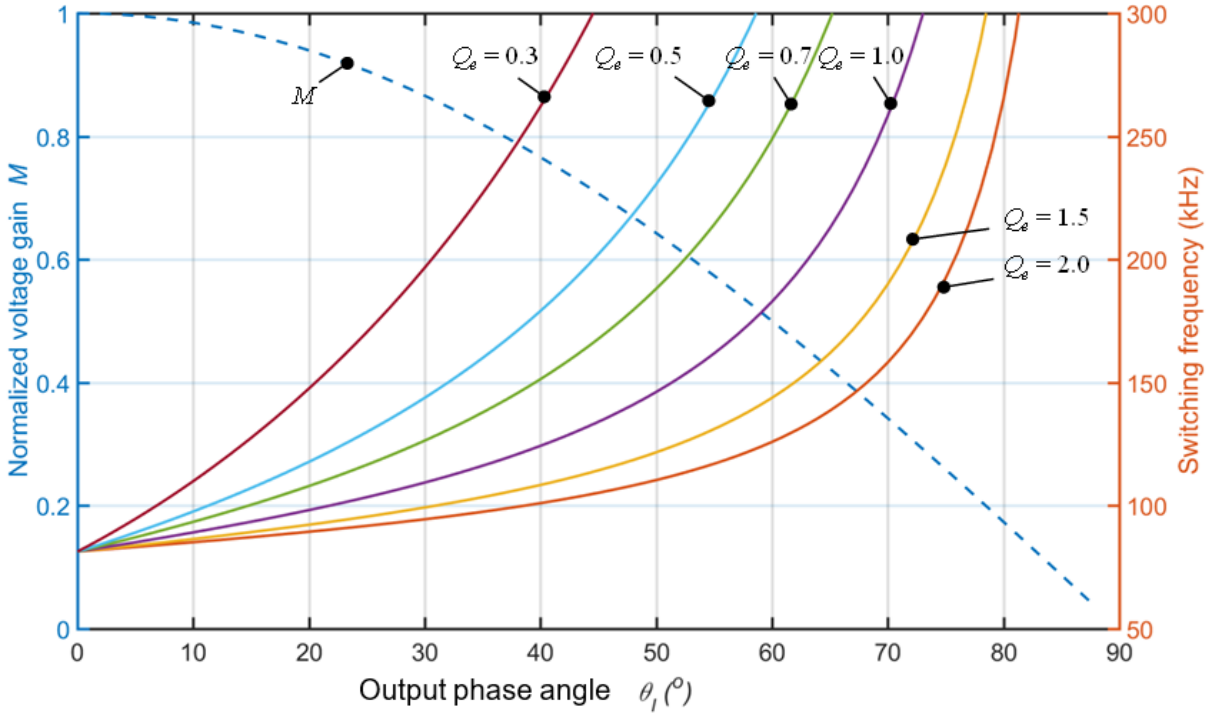


Figure 3.7. Switching frequency (f_s, solid lines) and normalized voltage gain (M, dashed line) over output phase angle (θ_l) under VFM.

3.3 Operation in Short Pulse-Density Modulation Region

To overcome the drawbacks under VFM, SPDM is applied to low-output and light-load regions. The high-frequency waveforms under SPDM are shown in Figure 3.8. Similar to PDM, SPDM also has a blank time where all switches are turned off. But unlike PDM, where the f_s is the same as or very close to f_r, SPDM has an f_s much higher than f_r. In addition, the SRC always enters a blank time after firing the exact two pulses. These create significant differences in circuit characteristics. To explain the differences, the circuit operation in each interval should be analyzed first. The circuit status of each interval is shown in Figure 3.9.

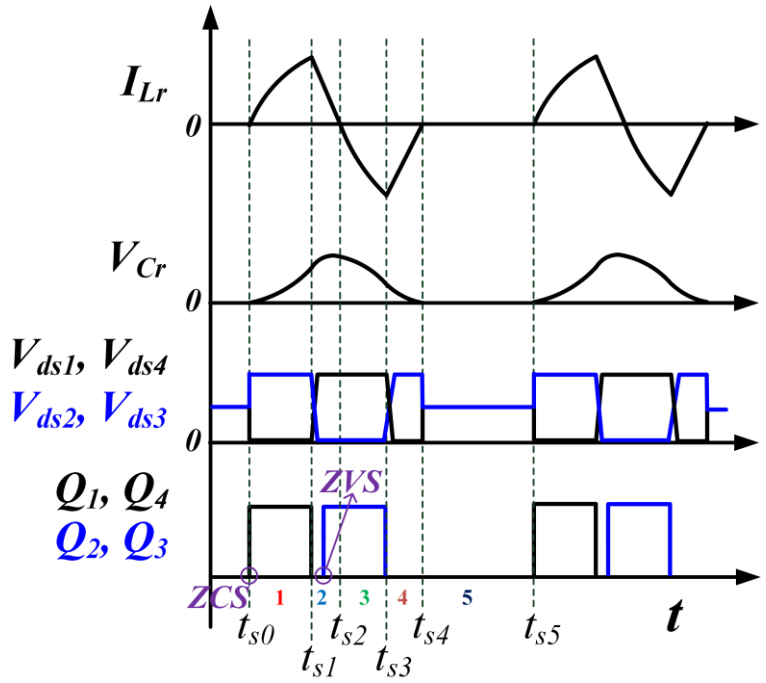
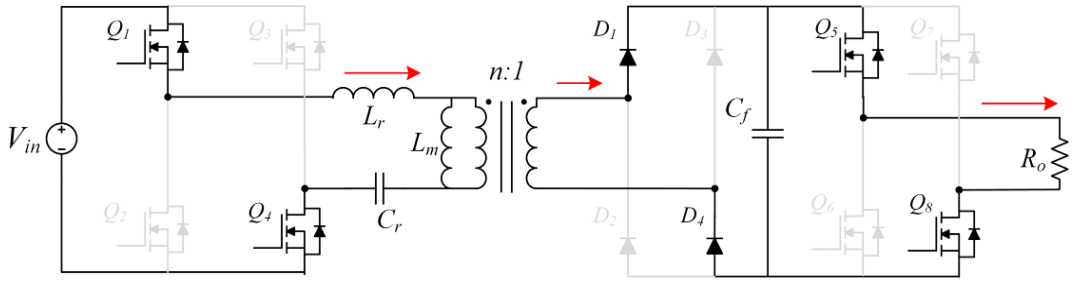
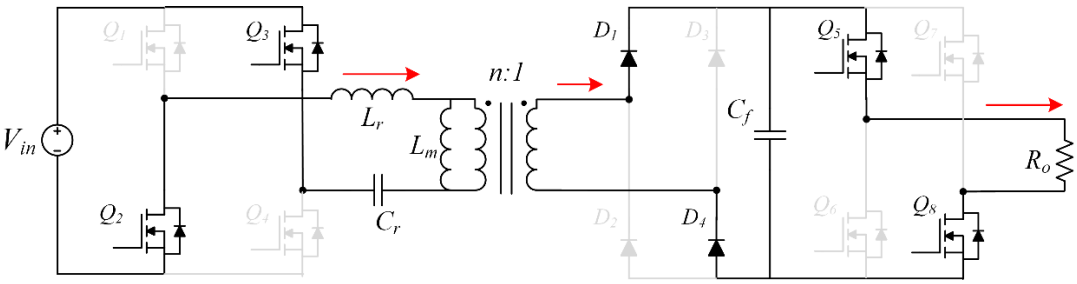


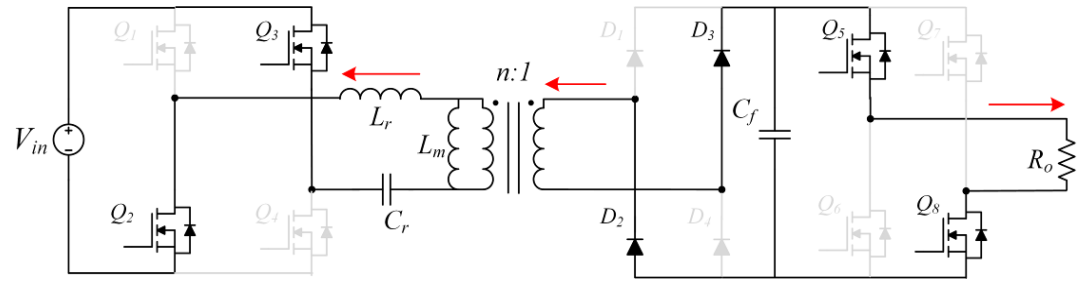
Figure 3.8. High-frequency waveforms in the SPDM region.



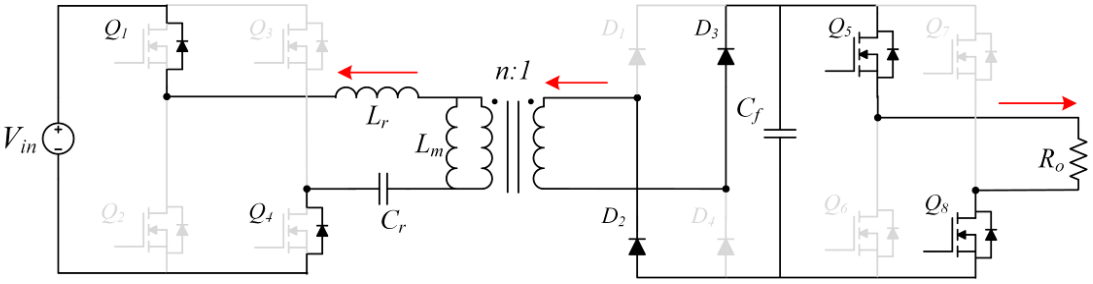
(a) *Interval* [t_{s0}, t_{s1}].



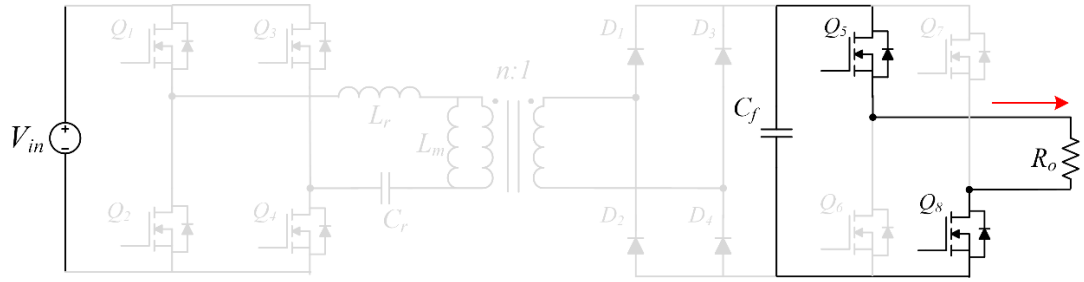
(b) *Interval* [t_{s1}, t_{s2}].



(c) *Interval* [t_{s2}, t_{s3}].



(d) *Interval* [t_{s3}, t_{s4}].



(e) *Interval* [t_{s4}, t_{s5}].

Figure 3.9. Circuit status of each interval in the SPDM region.

Interval [t_{s0}, t_{s1}]: Just before t_{s0}, the SRC is in an idle state, so both I_{Lr} and V_{Cr} are zero. Therefore, Q_1 and Q_4 turn on at t_{s0} with ZCS. Although the channel loss can be mitigated, the loss caused by the C_{oss} still exists [62]. After t_{s0}, the resonant tank is connected to the input and begins to store energy.

Interval [t_{s1}, t_{s2}]: At t_{s1}, Q_1 and Q_4 turn off and trigger a ZVS process same as *Interval* [t_1, t_2] and *Interval* [t_2, t_3] in the VFM region. This means during this interval, the C_{oss} of Q_2 and Q_3 is fully discharged and a current flows through their body diode. Since the drain-source voltage is

zero beforehand, Q_2 and Q_3 can turn on with ZVS. After the body diodes are conducted, the input source is reversely connected to the SRC. Therefore, I_{Lr} decreases rapidly and reaches zero at t_{s2}. For the analysis of SPDM, the effect of the magnetizing current is neglected, as it is negligible due to a high f_s (cf. Equation (3.1)). Also, Figure 3.9(b) only shows the diagram after Q_2 and Q_3 are on because the ZVS process is assumed to be completed within the dead time, which is much shorter than the entire high-frequency cycle.

Interval [t_{s2}, t_{s3}]: After t_{s2}, the output is reversely connected to the SRC, since I_{Lr} flows in the opposite direction. Due to the remaining V_{Cr}, the changing rate of I_{Lr} is even higher than the first interval. But note that this interval is shorter than the first interval since *Interval* [t_{s1}, t_{s2}] already occupies part of the on-time of Q_2 and Q_3.

Interval [t_{s3}, t_{s4}]: At t_{s3}, Q_2 and Q_3 turn off and both I_{Lr} and V_{Cr} start to decrease. All the switches are turned off, but the current can still freewheel through the body diode of Q_1 and Q_4. The energy in the resonant tank is fully released in this interval.

Interval [t_{s4}, t_{s5}]: All switches are turned off in this interval, so the SRC is in an idle state. The duration of this interval is the blank time (T_{blank}) in Section 2.5. Ideally, I_{Lr} and V_{Cr} are both zero in this interval, which greatly simplifies the later time-domain analysis. However, when f_s is too close to f_r, or when *Interval* [t_{s4}, t_{s5}] is too short, the ideal assumption may no longer hold.

To analyze the operation in each interval, the equivalent circuit model of the SRC is plotted in Figure 3.10, where V_{ie} and V_{oe} depend on the working interval. If the input and output voltages of the SRC are assumed to be constant over one cycle, then V_{ie} and V_{oe} can be given in Table 3.1.

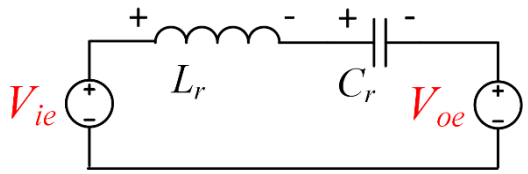


Figure 3.10. Equivalent circuit model of the SRC in the SPDM region.

Table 3.1. Parameters of the equivalent circuit model in the SPDM region.

Interval	$[t_{s0}, t_{s1}]$	$[t_{s1}, t_{s2}]$	$[t_{s2}, t_{s3}]$	$[t_{s3}, t_{s4}]$
V_{ie}	V_{in}	$-V_{in}$	$-V_{in}$	V_{in}
V_{oe}	nV_o	nV_o	$-nV_o$	$-nV_o$

With Figure 3.10, the state equations for each interval can be derived as (3.12) – (3.13). β represents the initial angle in each interval; κ_i and κ_v are the signs for individual state equations. O represents the horizontal center of the state trajectory. r represents the radius of the state trajectory, implying the energy stored in the resonant tank. The parameters of the state equations are summarized in Table 3.2. Some of the parameters require information from the previous interval, so the explicit solutions can be tedious. Alternatively, the state equations can be solved in the order of the intervals, with the aid of calculating software.

Table 3.2. Parameters of the state equations (3.12) – (3.13) in the SPDM region.

Interval	$[t_{s0}, t_{s1}]$	$[t_{s1}, t_{s2}]$	$[t_{s2}, t_{s3}]$	$[t_{s3}, t_{s4}]$
t_i	t_{s0}	t_{s1}	t_{s2}	t_{s3}
r	$V_{in} - nV_o$	$\sqrt{(V_{in} + nV_o + v_{Cr}(t_i))^2 + (i_{Lr}(t_i)Z_r)^2}$	$V_{in} - nV_o + v_{Cr}(t_i)$	$\sqrt{(V_{in} + nV_o - v_{Cr}(t_i))^2 + (i_{Lr}(t_i)Z_r)^2}$
B	0	$\tan^{-1}\left(\frac{i_{Lr}(t_i)Z_r}{V_{in} + nV_o + v_{Cr}(t_i)}\right)$	0	$\tan^{-1}\left(\frac{-i_{Lr}(t_i)Z_r}{V_{in} + nV_o - v_{Cr}(t_i)}\right)$
O	$V_{in} - nV_o$	$-V_{in} - nV_o$	$-V_{in} + nV_o$	$V_{in} + nV_o$
κ_i	1	-1	-1	1
κ_v	-1	1	1	-1

$$i_{Lr}(t) = \frac{\kappa_i r}{Z_r} \sin(\omega_r (t - t_i) - \beta) \tag{3.12}$$

$$v_{Cr}(t) = \kappa_v r \cos(\omega_r (t - t_i) - \beta) + O \tag{3.13}$$

The state equations not only describe the operation in SPDM but also provide other valuable information like the voltage gain equation. To begin with, the duration of each interval should be derived, as summarized in Table 3.3. T_{sx} and β_x represent the duration and β of *Interval* $[t_{s(x-1)}, t_{sx}]$. In every cycle, from t_{s0} to t_{s5}, the total charges (Q_{tot}) sent to the load can be calculated by integrating the equations of I_{Lr} as shown in (3.14), where r_x is the r of *Interval* $[t_{s(x-1)}, t_{sx}]$. Since the period of each cycle can be expressed as $(f_s \cdot \rho_p)^{-1}$, the pulse density can be derived by considering the average output current, as shown in (3.15).

Table 3.3. Duration of each interval in SPDM region.

Interval	$[t_{s0}, t_{s1}]$	$[t_{s1}, t_{s2}]$	$[t_{s2}, t_{s3}]$	$[t_{s3}, t_{s4}]$
T_{sx}	$\frac{1}{2f_s}$	$\frac{\beta_2}{\omega_r}$	$\frac{1}{2f_s} - \frac{\beta_2}{\omega_r}$	$\frac{\beta_4}{\omega_r}$

$$\begin{aligned} Q_{tot} &= \sum_{k=1}^{4} Q_k = n \sum_{k=1}^{4} \left(\int_{t_{s(k-1)}}^{t_{sk}} \left| i_{Lr}(t) \right| dt \right) \\ &= nC_r \left[r_1 (1 - \cos(\omega_r T_1)) + r_2 (1 - \cos(\beta_2)) + r_3 (1 - \cos(\omega_r T_3)) + r_4 (1 - \cos(\beta_4)) \right] \end{aligned} \tag{3.14}$$

$$\rho_p = \frac{V_o}{Q_{tot} f_s R_o} \tag{3.15}$$

Using (3.12) – (3.15), voltage gain curves in the SPDM region can be plotted in Figure 3.11. All the component parameters are the same as the last section and f_s = 250 kHz. When ρ_p is unity, the inverter works under VFM. At a lighter load, ρ_p drops earlier since the inverter enters SPDM earlier to cover the shortage of the modulation range with VFM.

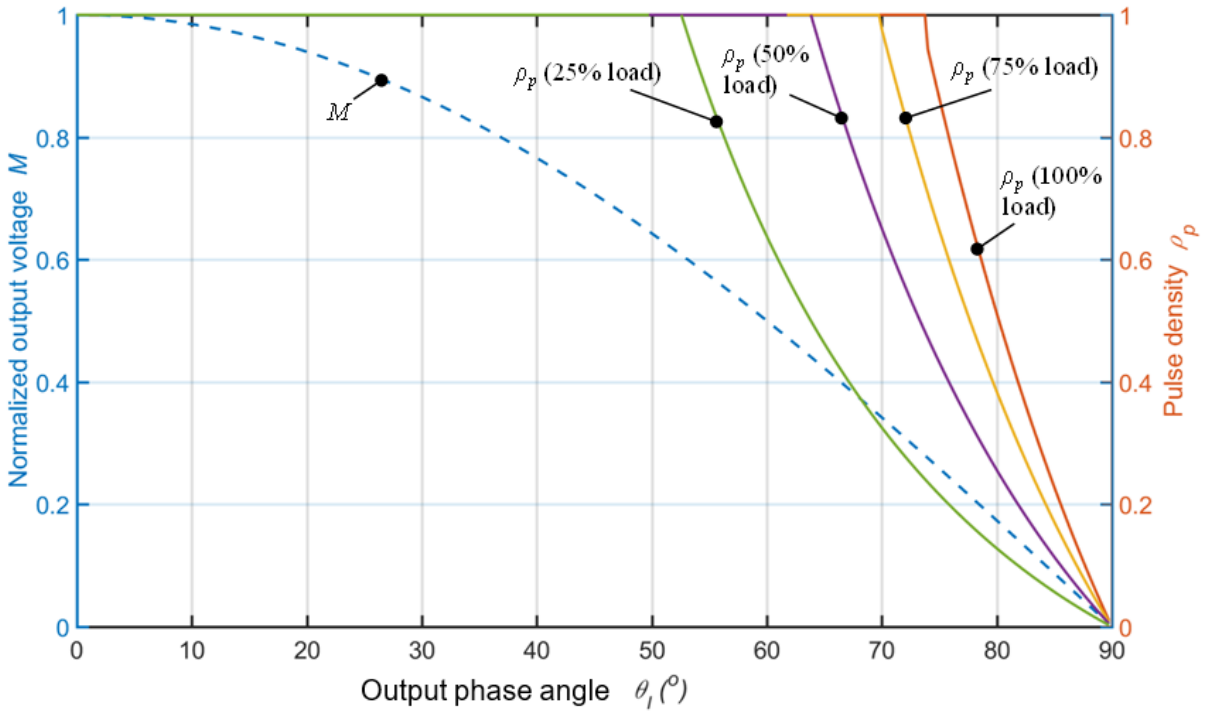


Figure 3.11. Pulse density (ρ_p, solid lines) and normalized voltage gain (M, dashed line) over output phase angle (θ_l) under SPDM.

In addition to the voltage gain curves, the state equations also provide an insight into how SPDM reduces current stresses over PDM. A simple indicator is the positive and negative peaks of I_{Lr} in a high-frequency cycle. In other words, they are the I_{Lr} at t_{s1} and t_{s3} in Figure 3.8, respectively. During *Interval* [t_{s0}, t_{s1}], r is only subject to V_{in} and V_o, so f_s only affects the trigonometric part of (3.12). If $f_s < 2f_r$, then $r_1 \cdot Z_r^{-1}$ is the positive peak value $i_{Lr}(t_{s1})$. Otherwise, the positive peak value reduces as f_s increases. In *Interval* [t_{s2}, t_{s3}], the V_{Cr} left in the previous interval contributes to r_3. Such a voltage tends to be higher at a lower f_s because I_{Lr} brings charges to C_r for a longer period. This is why the radius of the state trajectory keeps expanding in PDM, as earlier explained in Section 2.5. Additionally, the trigonometric part also lessens when f_s increases in a segment higher than $2f_r$. As a result, the negative peak value $|i_{Lr}(t_{s3})|$ reduces as f_s increases. In a nutshell, SPDM has lower current stresses than PDM because of a higher f_s. With a higher f_s, the energy accumulation in the resonant tank can be broken up earlier, which prevents high resonant

current peaks and the resulting high current stresses. For the same reason, the circuit under SPDM enters the blank time after only two pulses.

The positive and negative peaks over different f_s are plotted in Figure 3.12. Both peaks can be reduced by choosing a higher f_s, which strictly speaking, is on the premise that the f_s is higher than $2f_r$ (=160 kHz in Figure 3.12). In addition, the impact of the output voltage is also illustrated with different M. The peaks are the highest when M = 0.01 and lessen with a higher output voltage. This is also hinted by the equation of r_1 and r_3, where V_o can only decrease their magnitude. Consequently, the highest resonant current peaks in an SPDM region appear at ZCP and the positive peak at ZCP can be expressed as (3.16).

$$i_{Lr\_ZCP}(t_{s1}) = \frac{V_{in}}{Z_r}\sin\left(\frac{\omega_r}{2f_s}\right) \tag{3.16}$$

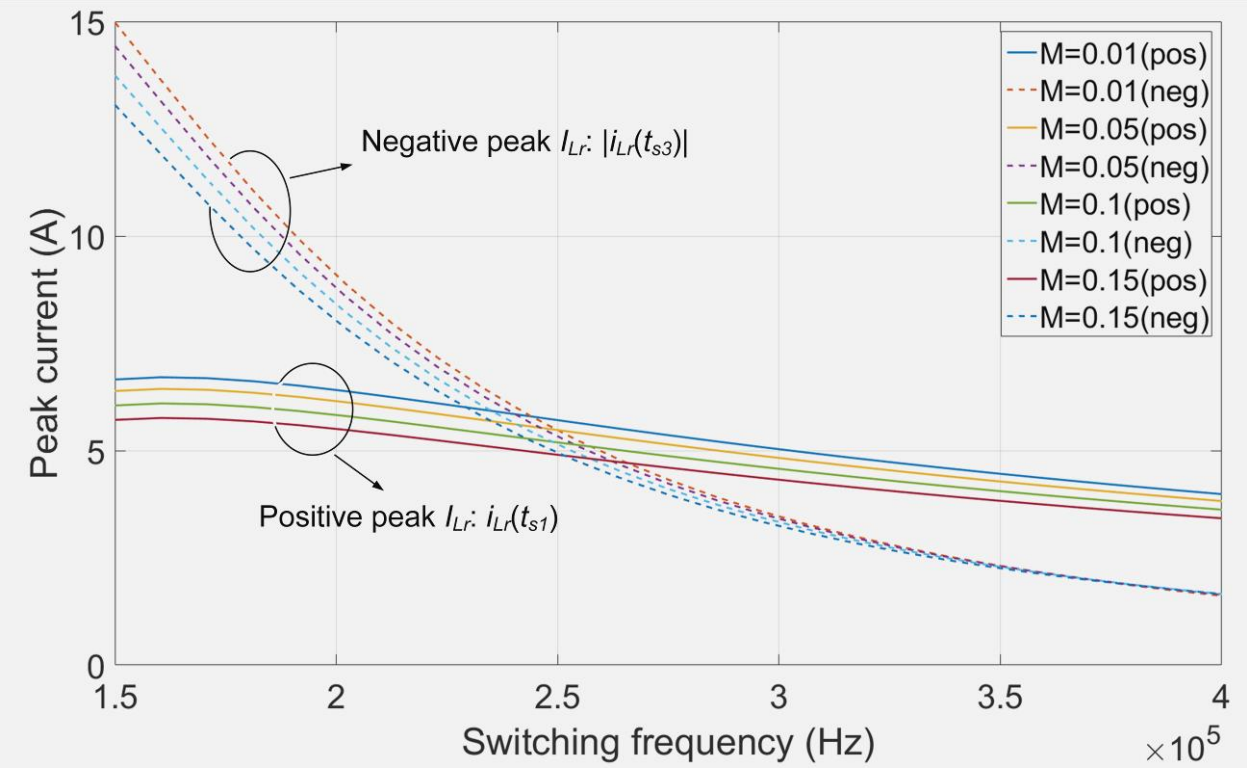


Figure 3.12. Resonant current peaks in a high-frequency SPDM cycle over switching frequency (f_s).

Unlike PWM converters, the calculation of component rms currents is complicated for resonant converters, not to mention using them in a dc/ac scenario. Therefore, by introducing the positive and negative peaks, the circuit designer can have a tool to preliminarily evaluate the performance of a design. For instance, the peaks of I_{Lr} should not exceed the current rating of the devices and the resonant inductor. Also, they are an important reference to choose the maximum f_s (i.e., the f_s in the SPDM region) for the system. More details regarding the usage of the peaks in the hardware design process will be covered in the next chapter.

3.4 Control Strategy

Through previous sections, the benefits of the proposed HMM have been explained. With that being said, the inverter system requires a control strategy to decide which modulation method should be adopted at a moment.

The flowchart of the control strategy is illustrated in Figure 3.13. It can also be interpreted as the program flowchart used by a digital controller of the inverter. First of all, HMM requires at least two pieces of information from the system regardless of its application scenario, and here, V_o and I_o are sensed. Next, the output phase angle (θ_l) and boundary angle (θ_b) should be calculated, and again, both angles are bounded between 0˚ and 90˚, as stated in Section 3.1. In a standalone application, θ_l can be provided internally, and in a grid-tied application, θ_l can be acquired by detecting V_o. Meanwhile, θ_b is subject to the load condition, R_o, which can be estimated when both V_o and I_o are known. Aside from using a lookup table, θ_b can also be estimated by (3.17), an equation derived from (2.3) with Q_e related to R_o. In Figure 3.13, the acquisition of I_o and the calculation of θ_b are marked purple, because in a standalone application, these processes are allowed to be completed at a much lower speed than acquiring $V_o[n]$.

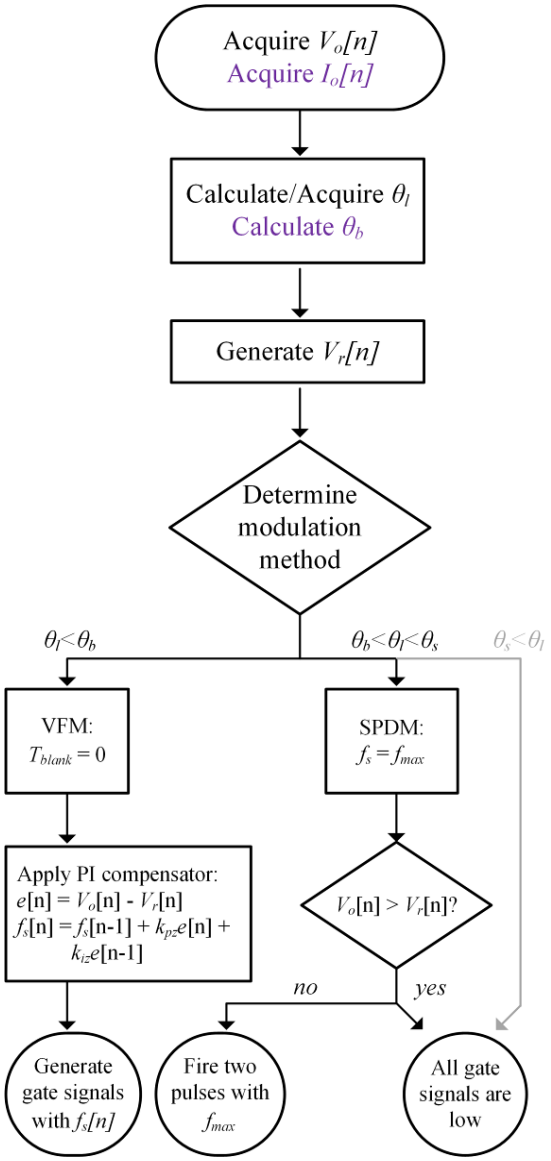


Figure 3.13. Control strategy of the proposed hybrid modulation method in a standalone application.

$$\theta_b = \cos^{-1}\left(\left(\sqrt{1+Q_e^2\left(\frac{f_{\max}}{f_r}-\frac{f_r}{f_{\max}}\right)^2}\right)^{-1}\right) \tag{3.17}$$

The modulation method can then be determined by comparing θ_b and θ_l. If $\theta_l < \theta_b$, the inverter adopts VFM and no blank time exists. Based on the error between $V_o[n]$ and the reference voltage $V_r[n]$ (which can easily be generated from θ_l), a compensator can update $f_s[n]$ to perform reference tracking. Due to the characteristics of the resonant converter, the compensator design is

not trivial and will be discussed separately in Chapter 5. On the other hand, if $\theta_l > \theta_b$, the inverter adopts SPDM and operates with the maximum switching frequency (f_{max}). To follow the sinusoidal reference, a simple on-off control can be used to control the output voltage. When $V_o[n] > V_r[n]$, all gate signals should remain low to shut down the SRC. Otherwise, two consecutive pulses should be fired to deliver power to the output.

When the inverter operates near ZCP, the theoretical pulse density may be very low. In this case, even two pulses can bring excessive power and create a spike on the output waveform. To mitigate such a spike, an optional way is to introduce the stop angle (θ_s) as illustrated in the gray path in Figure 3.13. θ_s should be an angle lower than but very close to 90˚. When θ_l goes beyond θ_s, the SRC is shut down, not firing any pulses. This mitigation method helps reduce the distortion near ZCP and improves output waveform quality.

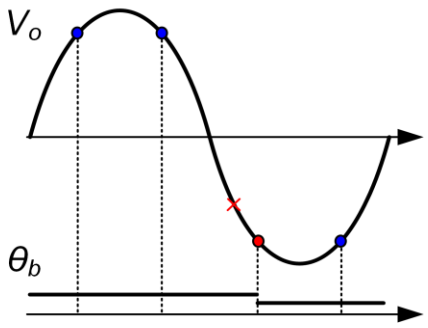


Figure 3.14. The dynamic change of θ_b.

Figure 3.14 is an illustration of how θ_b changes based on the load condition. The dots on the output voltage waveform indicate the moments when the controller acquires the load condition and then updates θ_b. Some delay is inevitable in this case. For example, if a load transition occurs at the red cross, it will not be reflected on the θ_b until the red dot. In addition, Figure 3.15 is an illustration of how an SRCUI transfers from the VFM region to the SPDM region. The transition occurs when θ_l hits θ_b. In a standalone application, θ_l is generated within the controller, so ideally no additional control is required to smoothen the transition.

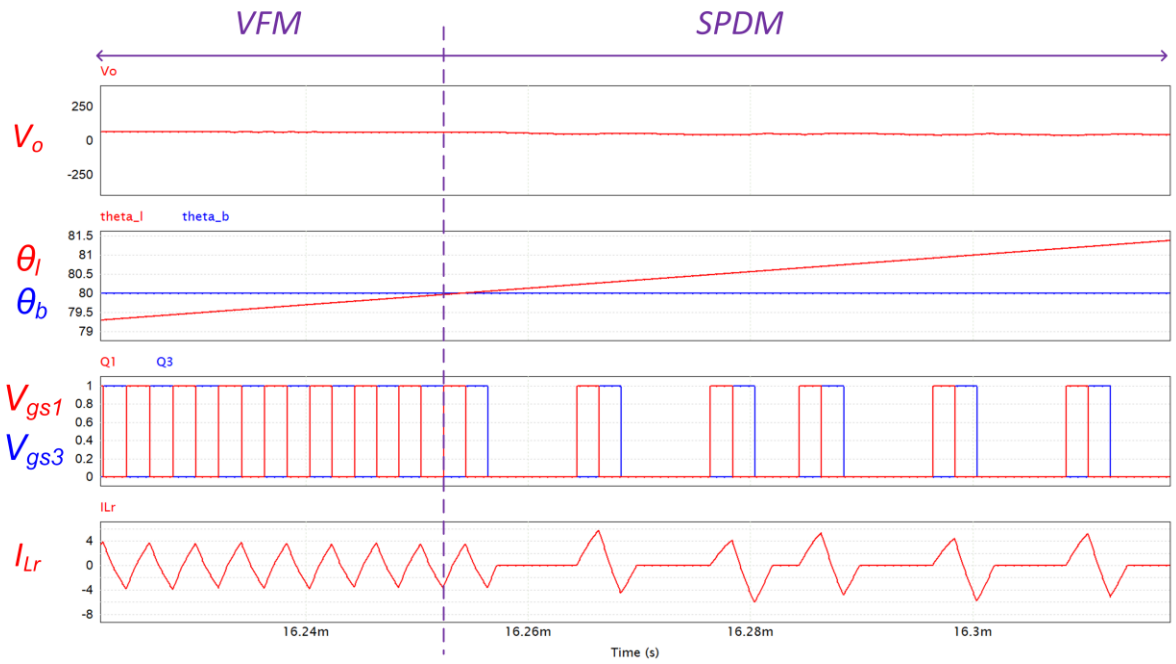


Figure 3.15. The transition from VFM to SPDM.

3.5 Comparison with Basic Modulation Methods

In this section, the performance under HMM will be compared to basic modulation methods for SRCUI. The basic methods have been introduced in Chapter 2. Since APSM is regarded as a mixture of other basic methods, only VFM, PSM, and PDM are included in the comparison. The bases of the comparison are given as follows:

- The purpose is to compare design metrics in terms of circuit characteristics irrelevant to actual implementation (e.g., device selection).
- The circuit parameters are the same (except C_f) for all modulation methods, as listed in Table 2.1. The range of f_s for HMM is the same as that of VFM.
- The data is mainly generated by simulation software PSIM and computing software MATLAB. All switches are assumed to be ideal. The equivalent series resistance (ESR) of all passive components are assumed to be zero.

3.5.1 Comparison of Resonant Current

The comparison starts with one of the most crucial factors, the resonant current (I_{Lr}). The magnitude of I_{Lr} directly impacts the conduction losses in semiconductor switches and winding losses. Figure 3.16 shows the comparison between HMM and PSM and their resonant current waveforms are overlapped in the third row. In the high-output region, the waveform envelop of HMM is lesser than that of PSM due to the advantage of using VFM. In the low-output region, PSM has a lower waveform envelop that smoothly diminishes with the output voltage, and the I_{Lr} with HMM seems higher. However, one has to keep in mind that the losses under SPDM are weighted by its pulse density. Figure 3.17 shows the comparison between HMM and PDM. With the resonant current waveform under both methods being overlapped, the drawback of PDM becomes more apparent. The current spikes of PDM exceed HMM in both high-output and low-output regions, leading to a high rms value of current.

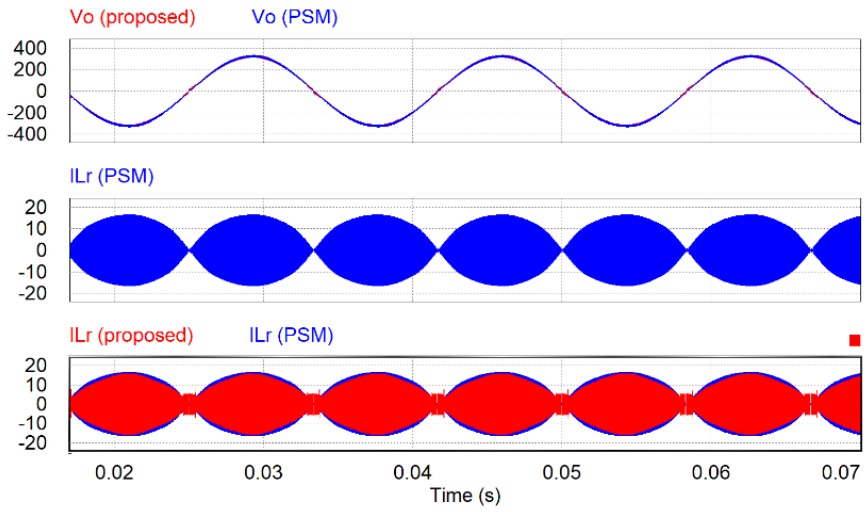


Figure 3.16. Resonant current comparison between HMM and PSM with the full load.

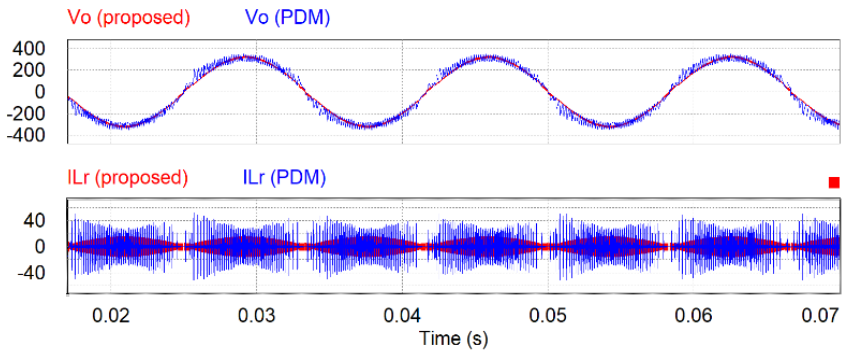


Figure 3.17. Resonant current comparison between HMM and PDM with the full load.

The I_{Lr} under different modulation methods is summarized in Figure 3.18. HMM has current stresses lower than PSM, and much lower than PDM. At the full load, the ohmic conduction losses under HMM are 7% less than PSM, and 50% less than PDM. Furthermore, the benefit in current reduction is valid across the entire load range. On the other hand, VFM has current stresses very similar to (or to be precise, slightly lower than) HMM, since with a heavy load, the VFM region in HMM dominates the operation of SRCUI. The curve of VFM only extends down to the half load, because the output waveform under VFM is highly distorted with a light load. The comparison would be unfair if one of the modulation methods did not need to process power in the low-output region.

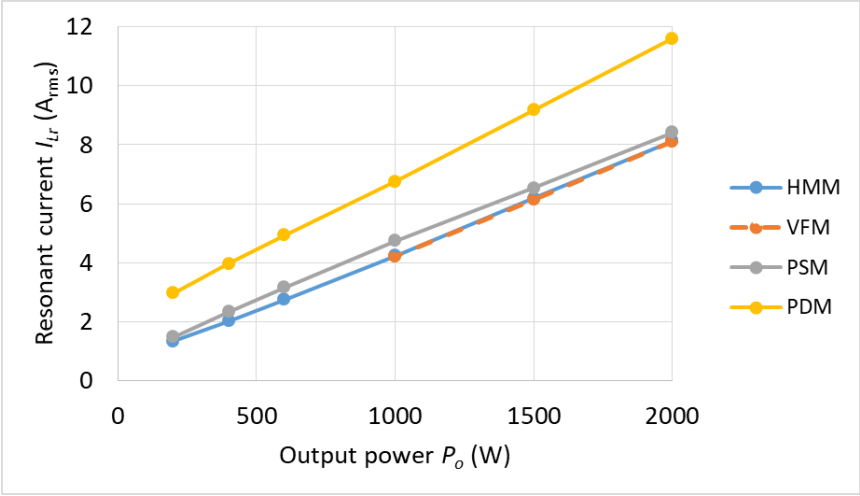
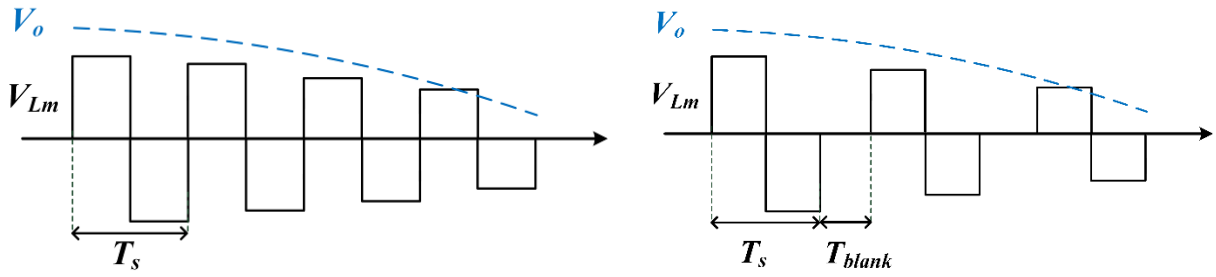


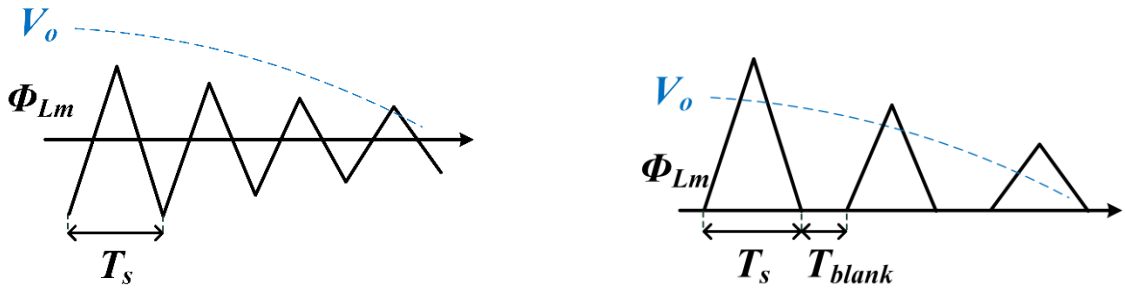
Figure 3.18. Resonant current comparison under different load conditions.

3.5.2 Comparison of Maximum Magnetic Flux



(a) For VFM and PSM (b) For PDM and SPDM

Figure 3.19. Transformer voltage waveform.



(a) For VFM and PSM (b) For PDM and SPDM

Figure 3.20. Transformer magnetic flux waveform.

Next, the magnetic flux of the transformer is also important, since it directly affects the core loss. In here, the resonant tank of SRCUI is located at the primary side, so the voltage applied to the transformer is subject to V_o. This can be explained by the waveform of the voltage across L_m (V_{Lm}), as shown in Figure 3.19. The positive and negative voltages of V_{Lm} are the same and equal to $\pm nV_o$. Therefore, the volt-second seen by L_m in a half switching cycle can be calculated by (3.18). Under VFM and PSM, the B-H curve of the transformer is symmetrical, so according to Faraday's law, the maximum magnetic flux ($\Phi_{max\text{-}a}$) can be written in (3.19), where N_p is the number of turns of the primary-side winding. Note that the $\Phi_{max\text{-}a}$ of PSM is independent of the phase shift duty (D_{ps}). On the other hand, the situation for PDM and SPDM is different and a little more complicated. Ideally, during the blank time, the resonant tank is completely depleted, and the

magnetic flux returns to zero. In this case, the B-H curve of the transformer is asymmetrical, and its maximum magnetic flux becomes (3.20). However, in the high-output region under PDM, there may be many consecutive pulses and limited T_{blank}. In that case, the maximum magnetic flux may not follow (3.20). The magnetic flux waveforms in the two different scenarios are compared in Figure 3.20.

$$VS_{p-p} = \frac{nV_o}{2f_s} \tag{3.18}$$

$$\Phi_{\max-a} = \frac{nV_o}{4f_sN_p} \tag{3.19}$$

$$\Phi_{\max-b} = \frac{nV_o}{2f_sN_p} \tag{3.20}$$

The product of $\Phi_{max\text{-}a}/\Phi_{max\text{-}b}$ and N_p under different modulation methods are compared in Figure 3.21. $\Phi_{max}\cdot N_p$ can represent the stress of magnetic flux without involving transformer design details. For PSM and PDM, the curves are load-independent. For HMM and VFM, the curves are load-dependent since f_s and θ_b change with the load. Based on Figure 3.21, PDM has the highest stress that is more than double the others, so it is vulnerable to core saturation. As to PSM and VFM, they share the same equation. But since the f_s of PSM always stays at the minimum, the stress of PSM is greater than VFM/HMM.

One should be aware that Figure 3.21 represents more about the difference in maximum magnetic flux, rather than the core loss itself. In PDM and SPDM, the core loss should be reduced since the effective switching frequency $f_{max}\cdot\rho_p$ is lower. In [63], the author suggested that the core loss involving re-magnetization processes (like in PDM/SPDM) is proportional to the effective switching frequency. On the other hand, the core loss calculation for PSM and VFM can refer to regular Steinmetz's equation. Steinmetz's equation states that the core loss density is proportional to f_s to the power of k_f and peak flux density to the power of k_B. Since $\Phi_{max\text{-}a}$ is proportional to the

reciprocal of f_s, the comparison of core loss comes down to the comparison of the Steinmetz coefficients. For the ferrite materials in a proper operating range, typically, $1 < k_f < 2.5$ and $2 < k_B < 3$. In most cases, k_B is higher than k_f [64]-[67]. Therefore, the core loss under PSM is generally higher than the VFM/HMM. In conclusion, VFM/HMM has the lowest $\Phi_{max} \cdot N_p$. This not only makes the transformer less vulnerable to saturation but also implies less core loss according to the Steinmetz coefficients of general ferrite core materials.

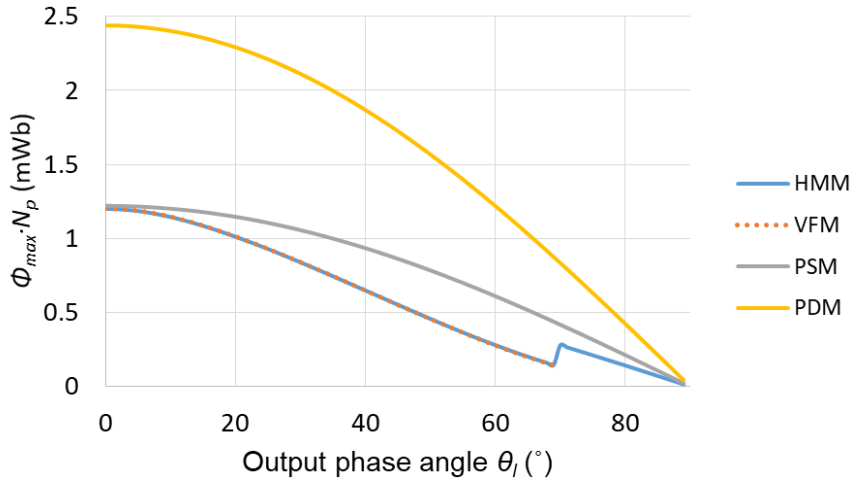
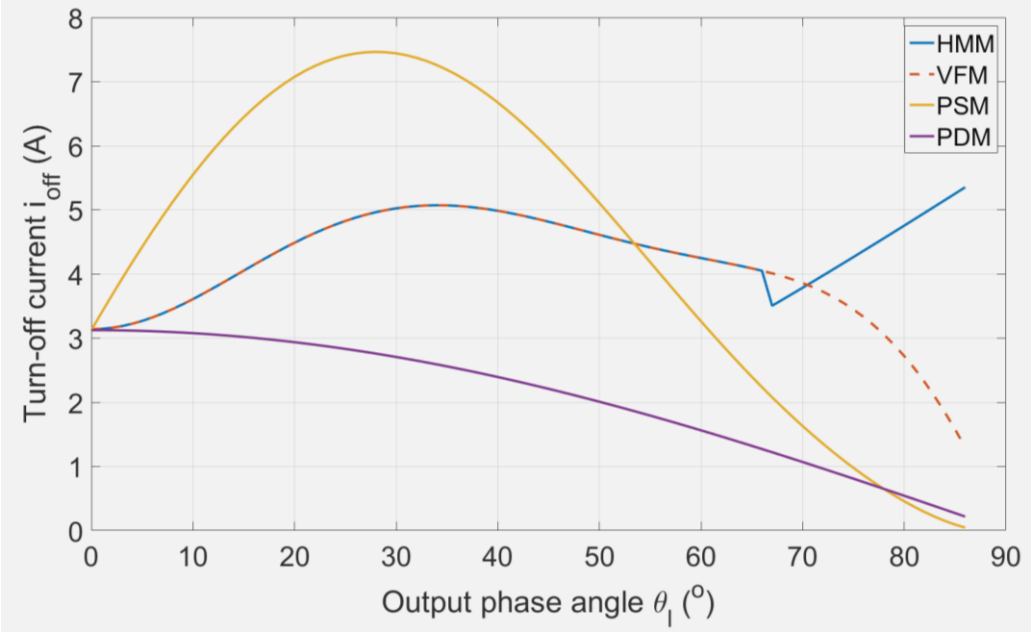


Figure 3.21. $\Phi_{max} \cdot N_p$ over output phase angle (θ_l) with the half load.

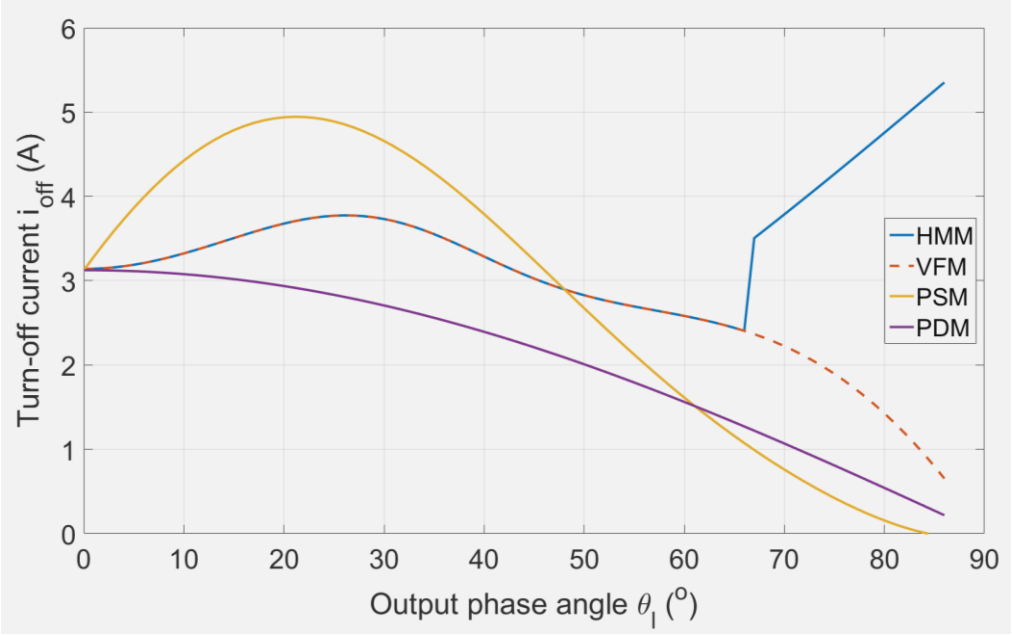
3.5.3 Comparison of the Turn-off Current for ZVS

The soft-switching function is another critical factor affecting the performance of SRCUI. As previously explained, eliminating the turn-on loss is more important than eliminating the turn-off loss. Therefore, the turn-off current (i_{off}) is selected to measure the capability of the ZVS turn-on. If i_{off} is insufficient, the device voltage commutation during the dead time cannot be completed in time to perform ZVS. The i_{off} under VFM has been explained in Section 3.2 in detail. As to PSM, its mechanism of ZVS and the calculation of i_{off} are very similar to VFM, except that the cutoff angle is altered by D_{ps} rather than f_s. Since the inverter under PDM has a fixed f_s and no early turn-off, its i_{off} simply follows the magnetizing current. Lastly, the i_{off} of SPDM can be calculated through the state equations introduced in Section 3.3. With all the calculation methods

being described, the i_{off} under different modulation methods are plotted in Figure 3.22 with the half load and the quarter load conditions.



(a) With half load.



(b) With quarter load.

Figure 3.22. Comparison of the turn-off current (i_{off}).

Higher i_{off} implies a stronger capability of ZVS. In Figure 3.22, PDM has the worst capability because its i_{off} follows the magnetizing current, which diminishes with the output voltage. The i_{off} of PSM exceeds VFM in the high-output region, which reflects the higher resonant current stress of PSM (cf., Figure 3.18). However, such a high i_{off} does not provide extra benefits, as i_{off} only needs to be "enough" for ZVS. In the low-output region, the i_{off} of PSM becomes lower and reaches zero at ZCP. This concurs with the fact that the resonant current under PSM is zero at ZCP. Although the i_{off} of VFM decreases slower than PSM in the low-output region, it may still fall short after a certain point. On the other hand, HMM adopts SPDM for the low-output region and it is able to maintain the strength of i_{off}.

Just like the case of magnetic flux comparison, the comparison of i_{off} is an indicator of ZVS capability, but it cannot be directly translated as a comparison of switching loss. The main reason comes from PDM and SPDM since the switching losses for both of them should be weighted by pulse density. In other words, PDM and SPDM utilize a different mechanism for switching loss reduction that does not show up in Figure 3.22. Under SPDM, due to its two-pulse pattern, only half of the switches experience the ZVS brought by i_{off}, and the other half always have the C_{oss} loss.

3.5.4 Summary

At the end of Chapter 2, Table 2.2 told us all basic modulation methods have their critical drawback. The analysis in this chapter should provide enough insights on how the proposed HMM overcomes all these drawbacks and meets the objectives set in Section 1.4: full-range switching loss reduction, resonant current restraint, and passive component loss restraint.

Firstly, by adopting SPDM in the low-output region, HMM has the ability to modulate output waveform in the entire operating range. Next, in the VFM region, all the primary-side

switches can obtain ZVS turn-on. In the SPDM region, although half of the switches do not have ZVS turn-on, they only generate C_{oss} loss that is further weighted by pulse density. Finally, based on Figure 3.18, HMM basically has the lowest resonant current stress. As a result, HMM is free from the critical drawbacks in Table 2.2.

In addition to the advantages of soft-switching and low resonant current over basic modulation methods, HMM also tends to have a low magnetic flux. Therefore, the losses in passive components (mainly from the transformer) can be well restrained under HMM. Despite that the hardware design of SRCUI has not been discussed, through the circuit analysis, HMM already shows great potential in reducing power losses. Therefore, HMM is an attractive approach that meets the first three objectives listed in Section 1.4.

Chapter 4

Inverter Design, Loss Analysis, and Experimental Results

4.1 Power Loss Model

In this chapter, an efficiency-oriented inverter design process will be established. To evaluate the performance of each design, a model for power losses should be established as well.

4.1.1 Losses in Primary-side Switches

The modeling work starts with the semiconductor switches. The total conduction loss of primary-side devices (P_{cond}) can be calculated in (4.1). Note that the current stress of Q_1, Q_4 are not the same as Q_2, Q_3 in the SPDM region, but the difference is minor and neglected in (4.1). Also, note that the on-resistance of Q_1 – Q_4 ($R_{ds\_on\_Pri}$) may be affected by their operating temperature and driving voltage. The critical part for (4.1) is to know the rms value of I_{Lr} (I_{Lr_rms}). An easier approach is to gather the data from circuit simulation software. Alternatively, it can be calculated through the state equations introduced in Chapter 3. The derivation and the solution may be tedious, but it helps understanding some processes and assumptions used to calculate other power losses under HMM.

$$P_{cond} = 2I_{Lr\_rms}^2 R_{ds\_on\_\mathrm{Pri}} \tag{4.1}$$

Step 1: For a general piecewise waveform, the rms value can be calculated by (4.2) [35]. D_k is the duty ratio of the k^{th} segment. u_k is the rms value of the k^{th} segment based on its own time

frame. u_k^2 is also called the contribution of the k^{th} segment. In HMM, the operation of SRCUI is divided into the VFM region and SPDM region, so I_{Lr_rms} can be written in (4.3).

$$rms = \sqrt{\sum_{k=1}^{n} D_k {u_k}^2} \tag{4.2}$$

$$I_{Lr\_rms}^2 = I_{Lr\_rms(VFM)}^2 \frac{2\theta_b}{\pi} + I_{Lr\_rms(SPDM)}^2 (1 - \frac{2\theta_b}{\pi}) \tag{4.3}$$

Step 2: The rms current of individual regions is calculated by summing up the contribution of the segments divided by different output phase angles. When the division of the angles is infinitely fine, it can be written in the form of an integration formula, as listed in (4.4) – (4.5). $i_{Lr\_rms(VFM)\_hf}$ and $i_{Lr\_rms(SPDM)\_hf}$ represent the rms current of I_{Lr} in a high-frequency cycle under VFM and SPDM respectively. They are both a function of θ_l.

$$I_{Lr\_rms(VFM)}^2 = \frac{1}{\theta_b} \int_{\theta_l=0}^{\theta_b} i_{Lr\_rms(VFM)\_hf}^2(\theta_l) d\theta_l \tag{4.4}$$

$$I_{Lr\_rms(SPDM)}^2 = \frac{2}{\pi - 2\theta_b} \int_{\theta_l=\theta_b}^{\pi/2} i_{Lr\_rms(SPDM)\_hf}^2(\theta_l) d\theta_l \tag{4.5}$$

Step 3: In order to find out the rms current value in a high-frequency cycle, another integration should be performed. The formula for the VFM region is listed in (4.6) based on the state equation in Section 3.2. Note that we assume the main *Interval* [t_0, t_1] takes up the whole period. For SPDM region, the formula is listed in (4.7), where $i_{Lrx(SPDM)}$ is the state equation (3.12) in *Interval* [$t_{s(x-1)}$, t_{sx}].

$$i_{Lr\_rms(VFM)\_hf}^2 = 2 f_s \int_{t=0}^{1/2 f_s} \left(\left(\frac{V_{in} - nV_o + \Delta V_{Cr}}{Z_r} \right)^2 + {i_{Lm\_pk}}^2 \right) \bullet \sin^2 \left(\omega_r t - \tan^{-1} \left(\frac{Z_r i_{Lm\_pk}}{V_{in} - nV_o + \Delta V_{Cr}} \right) \right) dt \tag{4.6}$$

$$i_{Lr\_rms(SPDM)\_hf}^2 = f_s \rho_p \sum_{x=1}^{4} \left(\int_{t_{s(x-1)}}^{t_{sx}} i_{Lrx(SPDM)}^2 dt \right) \tag{4.7}$$

Step 4: Finally, I_{Lr_rms} can be calculated by summarizing (4.3) – (4.7). Note that variables like V_o, f_s, ΔV_{Cr}, i_{Lm_pk}, and ρ_p require equations derived in Chapter 3 to transfer into an expression of θ_l. In that way, the integration in (4.4) and (4.5) can then be performed.

In addition to the conduction loss through the device channel, the body diode of a device also generates power loss when a current flows through. This happens when the SRC enters the dead time, so the loss from the device body diode is also termed the dead-time loss. To simplify the model, the device voltage commutation after switches turn off is assumed to finish immediately, and a constant current goes through the body diodes within the dead time. Therefore, in the VFM region, such a loss is mainly determined by the product of i_{off}, f_s, t_d, and the voltage drop of the body diode [62]. The formula of the dead-time loss in the SPDM region is similar, but i_{off} is replaced by the positive peak $i_{Lr}(t_{s1})$ and negative peak $|i_{Lr}(t_{s3})|$. The equation for the total dead-time loss (P_{dt}) can be found in (4.8). Lastly, just like regular diodes, the forward voltage drop of a body-diode (v_{sd}) is subject to its forward current. In a reasonable range, such a relationship with the forward current can be modeled by an equivalent resistance R_f [68]. Therefore, v_{sd} can be written in (4.9), where v_{f0} is the v_{sd} when the current is infinitesimal.

$$P_{dt} = \frac{2}{\pi}\left(\int_0^{\theta_b} 4 i_{off}(\theta_l) v_{sd} t_d f_s(\theta_l) d\theta_l + \int_{\theta_b}^{\frac{\pi}{2}} 2\left[i_{Lr}(t_{s1}, \theta_l) t_d + \left| i_{Lr}(t_{s3}, \theta_l) \right| T_{s4} \right] v_{sd} f_{\max} \rho_p(\theta_l) d\theta_l \right) \tag{4.8}$$

$$v_{sd} = v_{f0} + i_{sd} R_f \tag{4.9}$$

The soft-switching function of HMM focuses on eliminating the device turn-on loss since the device turn-off loss is relatively low. But in the loss breakdown, the total turn-off loss (P_{off}) is non-negligible as the inverter always operates with hard turn-off. The estimation of P_{off} requires information from device testing or datasheet. For example, the turn-off energy (E_{off}) of SCT3030AL can be found from its datasheet [69], representing the energy lost in each turn-off event. P_{off} can then be calculated by (4.10). Most of the time, the test conditions of E_{off} are different

from real working conditions. To adapt E_{off} for various switching currents, we can use the approach of curve fitting to obtain a quadratic equation (cf., Figure 4.1). As to various switching voltages, we can assume E_{off} is proportional to the switching voltage [70]. In these ways, E_{off} can be expressed as a function of the switching voltage and current. In an SRCUI, the switching voltage is always V_{in} so it is omitted from (4.10).

The equations for P_{off} and P_{dt} may seem complicated, but in fact, they simply follow some of the processes previously introduced: splitting the losses into VFM and SPDM regions, integrating the power losses with respect to θ_l.

$$P_{off} = \frac{2}{\pi}\left(\int_0^{\theta_b} 4E_{off}(i_{off}(\theta_l))\, f_s(\theta_l) d\theta_l + \int_{\theta_b}^{\frac{\pi}{2}} 2\left[E_{off}(i_{Lr}(t_{s1},\theta_l)) + E_{off}(i_{Lr}(t_{s3},\theta_l)) \right] f_{\max} \rho_p(\theta_l) d\theta_l \right) \quad (4.10)$$

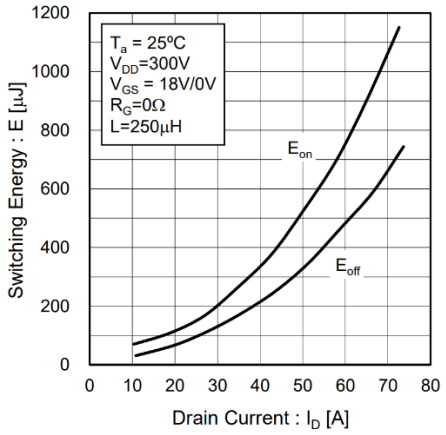


Figure 4.1. The switching energy of SCT3030AL [69].

Under HMM, the turn-on loss has been substantially curtailed. However, it is still interesting to see how much turn-on loss is left. The total turn-on loss (P_{on}) can be calculated by (4.11) and only comes from Q_1 and Q_4 in the SPDM region. In addition, the channel loss is eliminated by ZCS turn-on, so only C_{oss} loss counts. C_{oss} loss is caused by the energy wasted in charging and discharging C_{oss} every cycle, which can be estimated by the C_{oss} stored energy (E_{oss}) in a datasheet [62]. If E_{oss} is not provided in a datasheet, it can be estimated by (4.12) [71].

$$P_{on} = \frac{2}{\pi}\left(\int_{\theta_b}^{\frac{\pi}{2}} 2E_{oss}(V_{in})\, f_{\max} \rho_p(\theta_l) d\theta_l \right) \tag{4.11}$$

$$E_{oss} = \int_{v_{ds}=0}^{V_{in}} v_{ds} C_{oss}(v_{ds}) dv_{ds} \tag{4.12}$$

Finally, there is the total gate driver loss (P_{drive}) that is consumed for driving $Q_1 - Q_4$. P_{drive} is proportional to the driving voltage (V_{drive}) and the corresponding gate charge (Q_g). The gate charge can typically be found in the device datasheet. In addition, since the circuit operates with ZVS in most switching events, the gate charge related to the plateau region of V_{GS} can be subtracted from Q_g [62]. In Figure 4.2, such a plateau gate charge is approximately 43 nC (= 67 nC – 24 nC).

$$P_{drive} = \frac{8 Q_g V_{drive}}{\pi}\left(\int_0^{\theta_b} f_s(\theta_l) d\theta_l + \int_{\theta_b}^{\frac{\pi}{2}} f_{\max} \rho_p(\theta_l) d\theta_l \right) \tag{4.13}$$

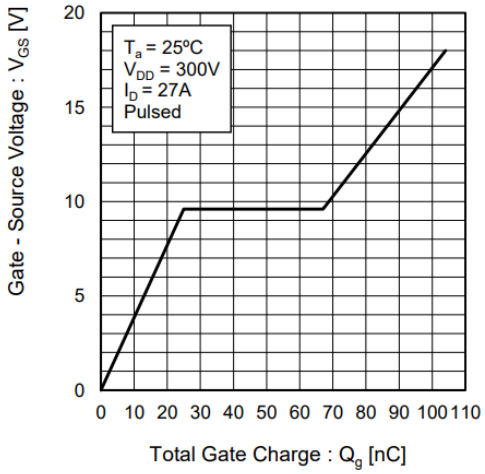


Figure 4.2. The gate charge curve of SCT3030AL [69].

4.1.2 Losses in Magnetic Components

On top of the primary-side devices, the magnetic components of SRCUI are also critical to its efficiency performance. Though it is possible to integrate the resonant inductor and the transformer to reduce volume [72], such an approach is usually available only when the ratio of L_r/L_m is low. But in HMM, L_r/L_m affects θ_b and should not be overly small. Therefore, the resonant inductor and the transformer are assumed to be separate components here.

Since I_{Lr_rms} has been obtained in the last subsection, the estimation of copper loss becomes easier, as shown in (4.14) and (4.15). R_{pri}, R_{sec}, and R_{Lr} are the primary-side, secondary-side transformer, and resonant inductor winding resistance. In the scope of this dissertation, ac winding resistance is identical to dc winding resistance. Since the prototyped SRCUI operates at no more than 300 kHz, the proximity effect and fringing effect are assumed negligible. The skin effect is also assumed negligible when proper litz wire is selected.

$$P_{Cu\_XF} = I_{Lr\_rms}^2 (R_{pri} + n^2 R_{\sec}) \tag{4.14}$$

$$P_{Cu\_Lr} = I_{Lr\_rms}^2 R_{Lr} \tag{4.15}$$

The flux density of HMM has previously been discussed in Section 3.5, and here, it should be used for modeling transformer core loss. In the VFM region, the core loss can be estimated by regular Steinmetz's equation as (4.16). V_e is the volume of the magnetic core and k_1 is another Steinmetz coefficient. B_m is the maximum magnetic flux density and A_e is the cross-sectional area of the core. In the SPDM region, the core is re-magnetized every cycle, so the core loss can be estimated by a modified Steinmetz's equation as (4.17) [63]. The total core loss of the transformer (P_{Fe_XF}) can then be calculated by integrating both Steinmetz's equations, as shown in (4.18).

$$P_{Fe\_XF(VFM)\_hf} = V_e k_1 f_s^{k_f} B_m^{k_B} = V_e k_1 f_s^{k_f} \left(\frac{nV_o}{4 f_s N_p A_e} \right)^{k_B} \tag{4.16}$$

$$P_{Fe\_XF(SPDM)\_hf} = V_e k_1 f_s^{k_f - 1} (f_{\max} \rho_p) B_m^{k_B} = V_e k_1 f_s^{k_f - 1} (f_{\max} \rho_p) \left(\frac{nV_o}{2 f_s N_p A_e} \right)^{k_B} \tag{4.17}$$

$$P_{Fe\_XF} = \frac{2}{\pi} \left(\int_0^{\theta_b} P_{Fe\_XF(\mathrm{VFM})\_\mathrm{hf}}(\theta_l) d\theta_l + \int_{\theta_b}^{\frac{\pi}{2}} P_{Fe\_XF(\mathrm{SPDM})\_\mathrm{hf}}(\theta_l) d\theta_l \right) \tag{4.18}$$

The resonant inductor also generates core loss, but its magnetic flux is not subject to the output voltage. Instead, the core loss is related to the resonant current. By the definition of an inductor, the maximum flux density should satisfy (4.19). Therefore, the core loss equation used

in the VFM and SPDM region can be written in (4.20) and (4.21) respectively. V_{e2} and A_{e2} are the volume and cross-sectional area of the core of the resonant inductor. N_{Lr} is the number of turns of the resonant inductor. The form of (4.20) and (4.21) are basically the same as (4.16) and (4.17), except the estimation of B_m, which utilizes the state equation derived in Chapter 3. Note that in (4.21), we assume the positive peak of I_{Lr} represents the current peak in a high-frequency cycle. Finally, the total core loss of the resonant inductor (P_{Fe_Lr}) can be obtained by (4.22).

$$\Phi_{\max\_Lr} = L_r I_{Lr\_\max} \tag{4.19}$$

$$P_{Fe\_Lr(VFM)\_hf} = V_{e2} k_1 f_s^{k_f} B_m^{k_B} = V_{e2} k_1 f_s^{k_f} \left(\sqrt{\left(\frac{V_{in} - nV_o + \Delta V_{Cr}}{Z_r} \right)^2 + i_{Lm\_pk}{}^2} \left(\frac{L_r}{N_{Lr} A_{e2}} \right) \right)^{k_B} \tag{4.20}$$

$$P_{Fe\_Lr(SPDM)\_hf} = V_{e2} k_1 f_s^{k_f - 1} (f_{\max} \rho_p) B_m^{k_B} = V_{e2} k_1 f_s^{k_f - 1} (f_{\max} \rho_p) \left(\left(\frac{L_r}{N_{Lr} A_{e2}} \right) \frac{V_{in} - nV_o}{Z_r} \sin\left(\frac{\omega_r}{2 f_{\max}} \right) \right)^{k_B} \tag{4.21}$$

$$P_{Fe\_Lr} = \frac{2}{\pi} \left(\int_0^{\theta_b} P_{Fe\_Lr(\text{VFM})\_\text{hf}}(\theta_l) d\theta_l + \int_{\theta_b}^{\frac{\pi}{2}} P_{Fe\_Lr(\text{SPDM})\_\text{hf}}(\theta_l) d\theta_l \right) \tag{4.22}$$

4.1.3 Other Power Losses

Other power losses are significant but relatively easy to calculate. The total rectifier diode loss (P_{diode}) coming from $D_1 - D_4$ can be roughly estimated by (4.23). (4.23) is valid because the average current flowing through a rectifier diode is half of the absolute output current. Note that P_{out} and V_{out} are the overall output power and voltage, rather than an instantaneous value. V_f is the diode forward voltage drop at the device average current. If the resistance of the diode needs to be considered, the calculation has to go through double integration just like for I_{Lr_rms}. The process will be tedious because the actual current waveform at a rectifier diode contains high-frequency components.

$$P_{diode} = 2 \langle |I_{out}| \rangle V_f = \frac{4\sqrt{2}}{\pi} \frac{P_{out}}{V_{out}} V_f \tag{4.23}$$

Since C_r is connected in series with L_r, it also has the entire I_{Lr} flowing through. Therefore, the ESR of C_r (R_{Cr}) creates a resistive resonant capacitor loss (P_{Cr}) that is calculated by (4.24).

$$P_{Cr} = I_{Lr\_rms}^2 R_{C_r} \tag{4.24}$$

The unfolder $Q_5 - Q_8$ switches at the line frequency and in theory with ZVZCS. Therefore, the relevant switching losses are negligible. Only the total conduction loss of unfolder (P_{uf}) matters and can be calculated by (4.25), where R_{uf} is the on-resistance of $Q_5 - Q_8$.

$$P_{uf} = 4\left(\frac{I_{out}}{\sqrt{2}}\right)^2 R_{uf} = 2\left(\frac{P_{out}}{V_{out}}\right)^2 R_{uf} \tag{4.25}$$

4.1.4 Summary

Table 4.1. Summary of power loss formulas

Category	Formula	Metrics
Total conduction loss of primary-side devices (P_{cond})	(4.1)	I_{Lr_rms}
Total dead-time loss (P_{dt})	(4.8) – (4.9)	i_{off}
Total turn-off loss (P_{off})	(4.10)	i_{off}
Total turn-on loss (P_{on})	(4.11)	N/A
Total gate driver loss (P_{drive})	(4.13)	N/A
Copper loss of transformer (P_{Cu_XF})	(4.14)	I_{Lr_rms}
Copper loss of resonant inductor (P_{Cu_Lr})	(4.15)	I_{Lr_rms}
Core loss of transformer (P_{Fe_XF})	(4.16) – (4.18)	Φ_{max}
Core loss of resonant inductor (P_{Fe_Lr})	(4.20) – (4.22)	N/A
Total rectifier diode loss (P_{diode})	(4.23)	N/A
Resonant capacitor loss (P_{Cr})	(4.24)	I_{Lr_rms}
Total conduction loss of unfolder (P_{uf})	(4.25)	N/A

The power losses modeled in this section are summarized in Table 4.1. Needless to say, other equations and information from datasheets are also necessary for calculating the actual power

losses in an inverter. These equations include but are not limited to: the calculation of I_{Lr_rms} (4.3) – (4.7), state equations (3.1) – (3.6), (3.12), and voltage gain equations (2.3) – (2.4), (3.11), (3.14) – (3.15).

Table 4.1 also explains the choice of design metrics compared in Section 3.5. Those design metrics were specifically selected based on the power loss model. Over half of the items are related to either the resonant current, the turn-off current, or the maximum magnetic flux. Some other items like P_{uf} and P_{diode} receive little to no effect from the choice of modulation method. This justifies that the design metrics in Section 3.5 can effectively predict the efficiency performance of SRCUI.

4.2 Inverter Design Procedure

With the power loss model established, the design of the inverter can be carried out. Figure 4.3 is an efficiency-oriented design procedure. To explain the procedure, each process has been labeled by a green note at its upper-left corner.

Process P1: The selection of switching frequency is crucial to power electronics, as it directly impacts the size of the system. In contrast to conventional converters operating with a fixed frequency, the f_s of SRCUI varies under HMM. In this case, the minimum switching frequency (f_{min}) can be used as a basis for high-level trade-off analysis, because the magnetic flux in the transformer and the resonant inductor reaches the maximum at the crest and trough of the output, where $f_s = f_{min}$. In the example of this section, we assume f_{min} is predetermined at 80 kHz according to size and other considerations.

Process P2: To initiate the design iteration, some guesses have to be made for the first attempt. The initial f_{max} can be set at $4f_{min}$ as a rule of thumb. For example, $f_{max} = 4f_{min} = 320$ kHz.

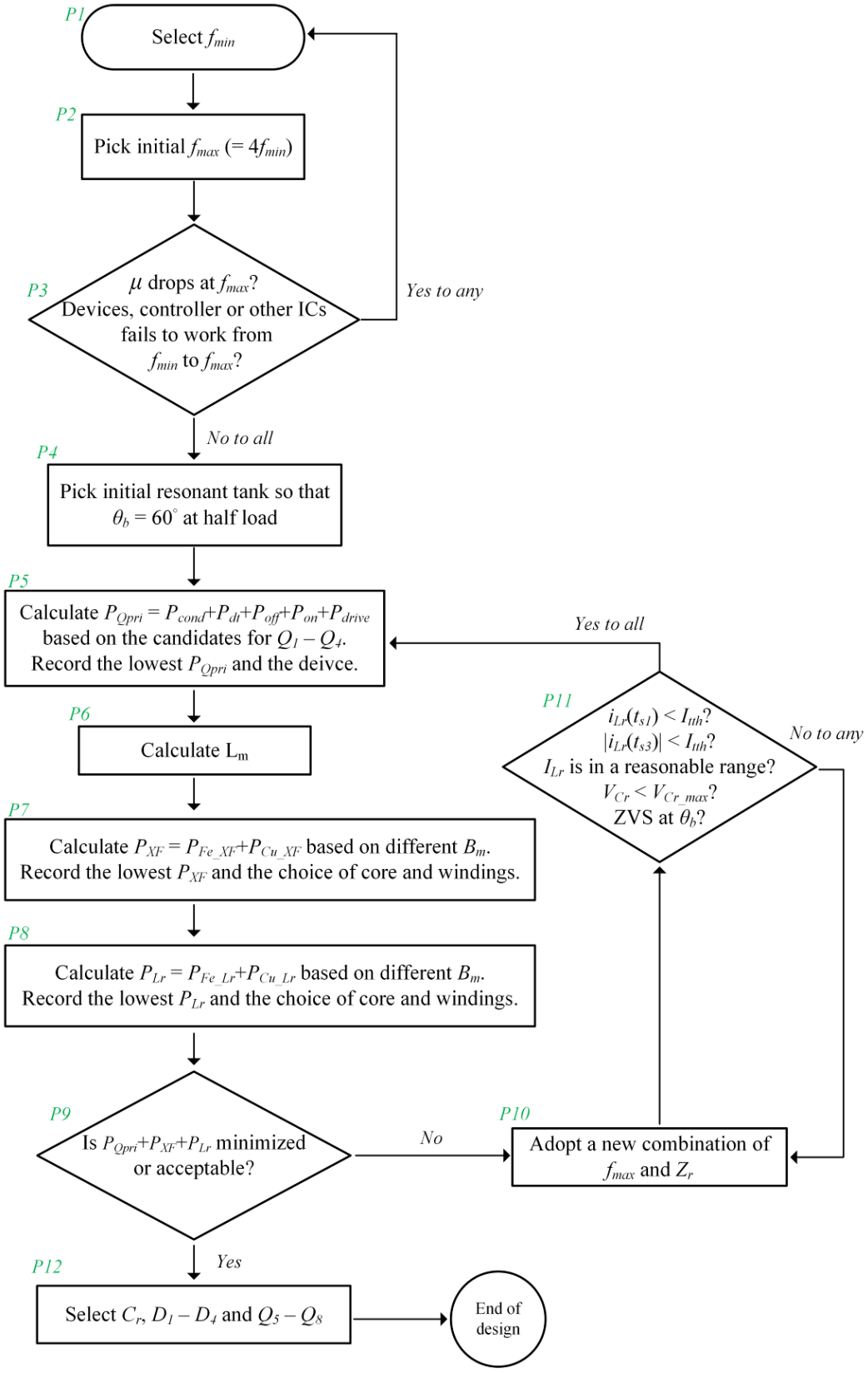


Figure 4.3. Design procedure of SRCUI under HMM.

Process P3: Once the initial f_{min} and f_{max} are decided, a quick scan can be carried out to confirm whether the frequency range is reasonable. For instance, the candidates of magnetic material should work from f_{min} to f_{max}, and avoid the roll-off in the permeability (μ). In Figure 4.4, the complex permeability of 3C95 is plotted and the roll-off does not take place before 320 kHz. Also, the loss tangent (=μ"/ μ') is still low at 320 kHz, so conventional formulas are still available [74]. In addition, if any controllers, ICs (e.g., gate drivers), or semiconductor devices is already selected, it should also satisfy the working frequency from f_{min} to f_{max}.

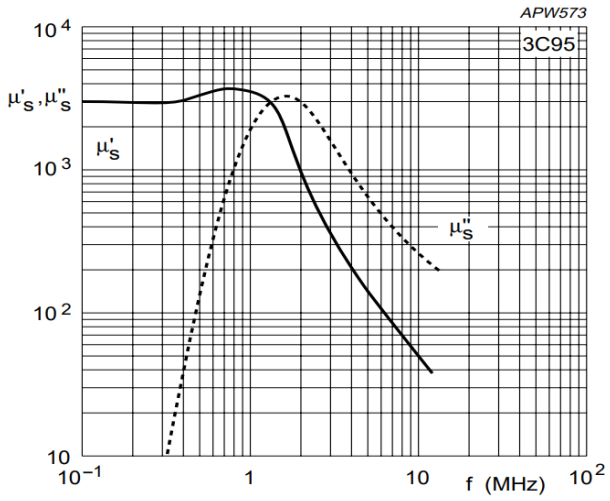


Figure 4.4. Complex permeability of 3C95 as a function of frequency [73].

Process P4: Similar to *Process P4*, an initial design of the resonant tank is needed for the design iteration. The series resonant frequency in (2.1) should be the same or slightly lower than f_{min} to process the largest instantaneous power with the optimal point of SRC [46]. Later, L_r and C_r can be found out once the characteristics impedance (Z_r) is decided. Z_r can be set to let $\theta_b = 60^\circ$ at the half load (R_{o_half}), which means it can be calculated by (4.26) based on (3.17). In this way, the inverter with R_{o_half} switches the modulation method when V_o reaches half of its peak value.

$$Z_r = \frac{8n^2 R_{o\_half}}{\pi^2} \frac{\sqrt{3}}{\frac{f_{max}}{f_r} - \frac{f_r}{f_{max}}} \tag{4.26}$$

Process P5: After the initial resonant tank and switching frequency range are known, one can assume an initial L_m that equals $4L_r$, since the impact of L_m is relatively minor. In addition, turns ratio n can be decided by (4.27). Dead-time t_d can be selected as a certain percentage of a high-frequency cycle (e.g., 1% of f_{max}^{-1}). From now on, the inverter has all the parameters it needs for simulation and modeling. Therefore, the losses in the primary-side switches (P_{Qpri}) can be calculated by adding up P_{cond}, P_{dt}, P_{off}, P_{on}, and P_{drive}. P_{Qpri} should be estimated for each candidate of the primary-side switches to identify the one with minimal loss. To be a candidate, the voltage and current rating of a device should at least satisfy (4.28) and (4.29).

$$n \le \frac{V_{in}}{V_{om}} = \frac{V_{in}}{\sqrt{2}V_{out}} \tag{4.27}$$

$$\text{voltage rating of } Q_1 - Q_4 > V_{in} \tag{4.28}$$

$$\text{average current rating of } Q_1 - Q_4 > P_{out\_max}/(2V_{in}) \tag{4.29}$$

Process P6: After $Q_1 - Q_4$ is selected, L_m should be re-selected to satisfy the ZVS condition. At the crest and trough of the output, f_s is very close to f_r and the turn-off current is basically solely contributed by the magnetizing current. Therefore, based on (3.1) and (3.7), the constraint on L_m can be written in (4.30). V_{om} is the maximum absolute output voltage. Also, note that C_{oss} is not constant in a real device. So the C_{oss} in (4.30) is a time-related $C_{oss(tr)}$ defined in (4.31).

$$L_m \le \frac{nV_{om}t_d}{8f_sC_{oss}V_{in}} \tag{4.30}$$

$$C_{oss(tr)} = \frac{1}{V_{in}}\int_0^{V_{in}} C_{oss}(v_{ds})dv_{ds} \tag{4.31}$$

Process P7: The design of the transformer starts with an estimation through the area product (A_p). Related to both power loss and size, A_p is defined as the product of the core cross-sectional area (A_e) and the window area (W_A) as (4.32). According to [75], the volume of the transformer can be seen as a function of A_p as (4.33), where K_{vol} is a constant determined by core

configuration (e.g., K_{vol} = 14.5 for pot core). Therefore, the maximum A_p can be obtained once the volume restriction and desired core configuration are known. In a power converter design, there is a trade-off between efficiency and power density [76]. Since the procedure here is supposed to be efficiency-oriented, a larger A_p is preferred in general.

$$A_p = W_A A_e \tag{4.32}$$

$$V_e = K_{vol} A_p^{0.75} \tag{4.33}$$

Up until now, the designer should already have candidates for core material and core configuration along with the limitation on A_p. So by finding the cores that have high A_p without violating the limit, a list of candidates for the core can be generated. For each candidate, a different winding design also leads to different power loss. To sweep over the possible options, one can starts with N_p (number of turns of the primary-side winding) = 1 and then gradually increase. Before launching the loss calculation process, the magnetic flux density needs to be inspected first to avoid saturation, as shown in (4.34). The saturation flux density (B_{sat}) is usually provided in the datasheet of the core material. If the core is not saturated, the core loss can then be calculated using the model in Section 4.1.

$$B_{\max} = \frac{nV_{om}}{4 f_{\min} N_p A_e} < B_{sat} \tag{4.34}$$

Next, the actual windings should be designed based on window utilization as (4.35). K_u is the window utilization factor. A_{wp} and A_{ws} are the cross-sectional area of the primary and secondary-side windings. If the current density at both sides is designed to be the same, A_{wp} and A_{ws} satisfy (4.36). To facilitate the estimation of transformer copper loss, (4.14) is further written into (4.37), providing the mean length per turn (MLT) is the same for both sides. ρ is the electrical resistivity of copper.

$$N_p A_{wp} + \frac{N_p}{n} A_{ws} \le K_u W_A \tag{4.35}$$

$$A_{ws} = nA_{wp} \tag{4.36}$$

$$P_{Cu\_XF} = I_{Lr\_rms}^2 (N_p \rho \frac{MLT}{A_{wp}} + \frac{N_p}{n} \rho \frac{MLT}{A_{ws}}) \tag{4.37}$$

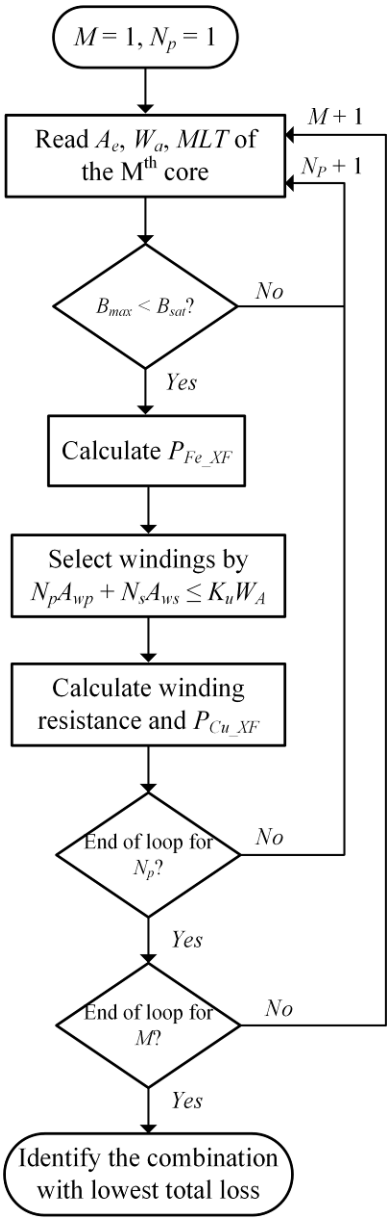


Figure 4.5. Sweeping program for transformer loss estimation.

The calculation of core loss and copper loss has to be repeated to find out the design with the least total loss. This can be achieved by a sweeping program shown in Figure 4.5. The program sweeps over two loops – one for N_p and the other for the candidates of the core. At the end of the program, the transformer design with the least power loss is accomplished. Finally, to adjust L_m to the desired value, the air gap (l_g) can be estimated by (4.38).

$$l_g \approx \frac{1}{2}\frac{\mu_o N_p^2 A_e}{L_m} \tag{4.38}$$

Process P8: In here, the resonant inductor is also realized by a high-μ core and an air gap, so the design process is very similar to *Process P7*, including the initial screening with A_p. The difference mainly lies in the calculation of core loss and copper loss, as the formulas are much different. Also, the magnetic flux density is controlled by the resonant current rather than the output voltage, so the saturation should be checked by (4.39) instead. (4.39) involves with the maximum current of L_r at the peak of the output, where ΔV_{Cr} and i_{Lm_pk} also reach their maximum. In addition, the window utilization restriction (4.35) should also be modified since only one winding presents.

$$B_{\max} = \frac{L_r}{N_{Lr} A_{e2}} \sqrt{\left(\frac{V_{in} - nV_{om} + \Delta V_{Cr\_\max}}{Z_r} \right)^2 + i_{Lm\_pk\_\max}{}^2} < B_{sat} \tag{4.39}$$

Process P9 and *Process P10*: Now the losses in Q_1 – Q_4 and magnetic components are obtained. However, these are only the losses in terms of the initial attempt. To find out the design with the least power loss, the previous *Process P5* – *P8* should be iterated. For each iteration, a new combination of f_{max} and Z_r should be used. As a matter of fact, these two parameters affect θ_b (cf., (3.17)) and many other characteristics. They are crucial and special design parameters of HMM.

Process P11: However, each iteration has to sweep through many candidates of the device and magnetic parts. To accelerate the search, some constraints can be set to rule out the unreasonable options before entering *Process P5 – P8*. Firstly, if Z_r is too large, the resulting small C_r may lead to an excessive resonant capacitor voltage. So based on (3.2), the first constraint can be written in (4.40), or (4.41) with respect to Z_r. V_{Cr_rate} is the voltage rating of C_r and R_{o_full} is the load resistance at the full load. On the other hand, the resonant current can be excessive if Z_r is too small. The peak resonant current (i_{Lr_peak}) in a line-frequency cycle is estimated by (4.42). If an upper limit is set for i_{Lr_peak}, a lower bound can be obtained for Z_r. For example, we can set the upper limit as twice of the i_{Lr_peak} derived in the initial iteration.

$$\Delta v_{Cr\_\max} = \frac{V_{om}^{\ 2}}{4V_{in}C_r R_{o\_full} f_{\min}} < V_{Cr\_rate} \tag{4.40}$$

$$Z_r < \frac{2V_{in}V_{Cr\_rate}R_{o\_full}}{\pi V_{om}^{\ 2}} \tag{4.41}$$

$$i_{Lr\_peak} = \sqrt{\left(\frac{V_{in} - nV_{om} + \Delta V_{Cr\_\max}}{Z_r}\right)^2 + i_{Lm\_pk\_\max}^{\ 2}} \tag{4.42}$$

To avoid going through *Process P3* again, f_{max} should not exceed the value chosen in *Process P2*. In addition, the turn-off current (i_{off}) may be insufficient if the f_{max} is too high. This can be prevented by checking the ZVS condition of $Q_1 – Q_4$ at the boundary (when $\theta_l = \theta_b$). To do so, one can apply (3.7) and (3.10), which have been explained in Section 3.2.

On the other hand, the lower bound of f_{max} can be set by using the resonant current peaks in the SPDM region discussed in Figure 3.12, Section 3.3. With a lower f_{max}, the current peaks tend to be higher and therefore a current threshold I_{tth} can be set. A lower bound for f_{max} is drawn when the resonant current peaks have to comply with (4.43) and (4.44). As a rule of thumb, I_{tth} should be lower than $0.5 \cdot i_{Lr\_peak}$.

$$i_{Lr}(t_{s1}) < I_{tth} \tag{4.43}$$

$$|i_{Lr}(t_{s3})| < I_{tth} \tag{4.44}$$

Process P12: When *Process P9* outputs "yes", the procedure should have gained all the circuit parameters and the design of $Q_1 - Q_4$ and magnetic components. The rest of the components are not that sensitive to circuit parameters, so they can be designed in the last process. Besides the capacitance and voltage rating, the design of C_r should also take ESR, current capability, and the ability of dv/dt into consideration. These properties may be degraded when C_r operates with a high frequency.

The rectifier $D_1 - D_4$ is also important to system efficiency. Its voltage stress is V_{om} and the average current stress is written in (4.45). Here, the effect of the junction capacitance of $D_1 - D_4$ is not included in the analysis. However, it is worth mentioning that overly large junction capacitance may hinder $Q_1 - Q_4$ from ZVS [77]-[78].

$$I_{diode\_avg} = 0.5\langle |I_{out}| \rangle = \frac{\sqrt{2}}{\pi} \frac{P_{out}}{V_{out}} \tag{4.45}$$

Finally, the power loss in the unfolder $Q_5 - Q_8$ can always be reduced if a lower on-resistance device is used. The typical trade-off between conduction loss and switching loss does not apply, since $Q_5 - Q_8$ are line-frequency switches with ZVZCS. Its voltage stress and average current stress are the same as $D_1 - D_4$. The unfolder is commonly realized with low-cost devices.

4.3 Prototype and Experimental Results

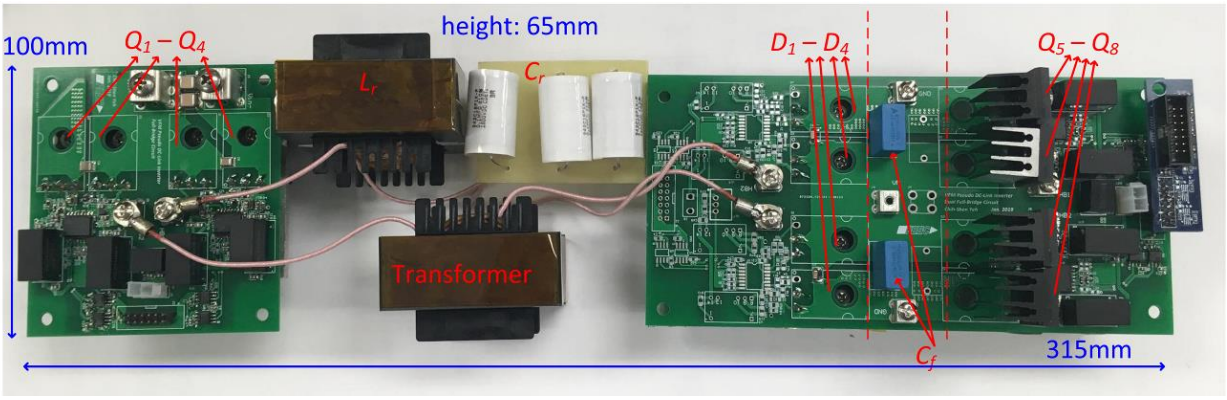


Figure 4.6. SRCUI prototype.

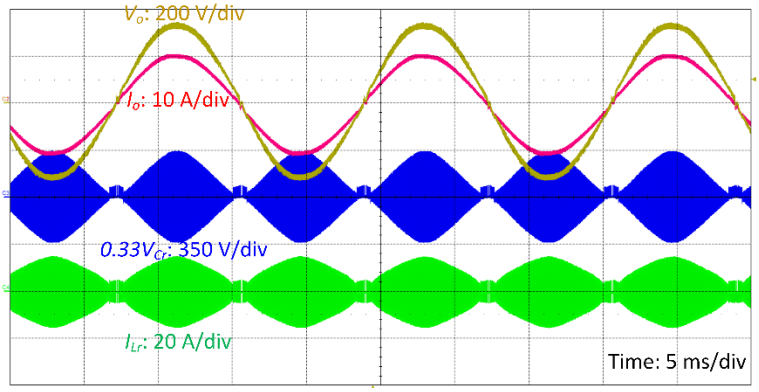
Table 4.2. Key components of the SRCUI prototype

Components	**Part numbers/ Design details**
Primary-side switches ($Q_1 - Q_4$)	SiC MOSFET SCT3030AL
Rectifier ($D_1 - D_4$)	Si diode STTH6006W
Unfolder ($Q_5 - Q_8$)	CoolMos IXKK85N60C
Transformer	Core: EE65/32/27, 3C95 Primary-side winding: 660 strand #44 AWG litz wire, 18 turns Secondary-side winding: 660 strand #44 AWG litz wire, 15 turns
Resonant inductor (L_r)	Core: EE65/32/27, 3C95 Winding: 660 strand #44 AWG litz wire, 21 turns
Resonant capacitor (C_r)	942C16P1K-F * 3 (in series)
Output filtering capacitor (C_f)	B32922C3474M000 * 2
Gate driver	UCC21521

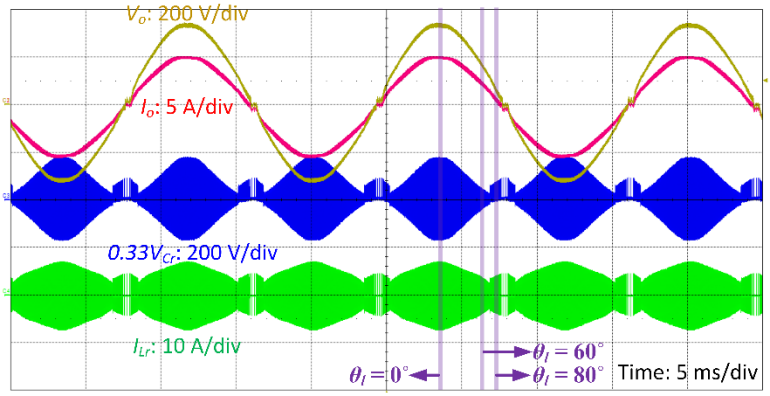
To verify the concept and analysis of HMM, a prototype is built with the circuit parameters listed in Table 2.1, and the photo is shown in Figure 4.6. The components of the prototype are

summarized in Table 4.2. The controller is implemented by a digital signal processor (DSP) F28379D.

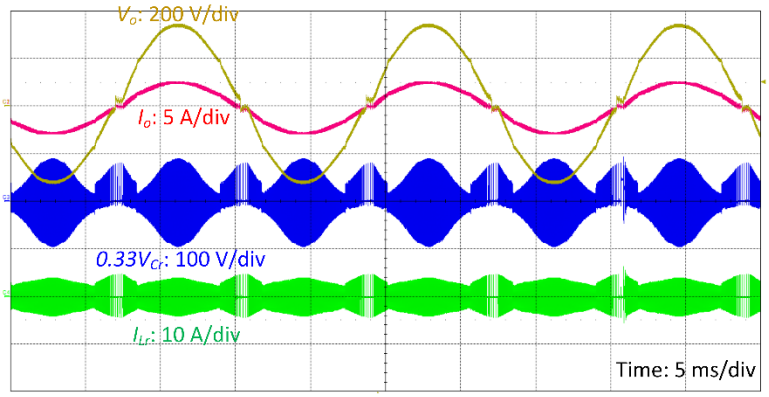
The low-frequency steady-state waveforms under HMM are shown in Figure 4.7, proving that the prototype successfully outputs a sinusoidal voltage. The discontinuity can be observed from the waveforms of I_{Lr} and V_{Cr}, marking the boundary between VFM and SPDM region. At the crest and trough of the output, the instantaneous power is the largest, so I_{Lr} and V_{Cr} are also at their peak. By comparing Figure 4.7(a) and (c), it is clear that the SPDM region is longer at a light load. In addition, the magnitude of I_{Lr} and V_{Cr} in the SPDM region is independent of the load condition, as discussed in Section 3.3. Therefore, the peak I_{Lr} and V_{Cr} in the SPDM region can even exceed the VFM region at a lighter load. The THD of V_o under 100%, 50% and 25% load are 1.79%, 2.96% and 3.91% respectively. The waveform quality is lower at a light load because of the longer SPDM region. In the SPDM region, the circuit operation is analogous to burst mode control, so even with the two-pulse pattern, the output voltage ripple still tends to be high. This causes the degradation of output waveform quality.



(a) P_o = 2 kW (100% load)



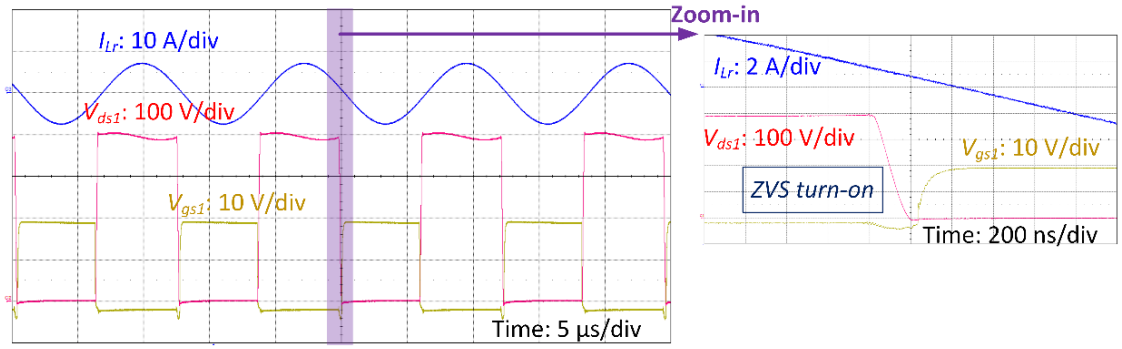
(b) P_o = 1 kW (50% load)



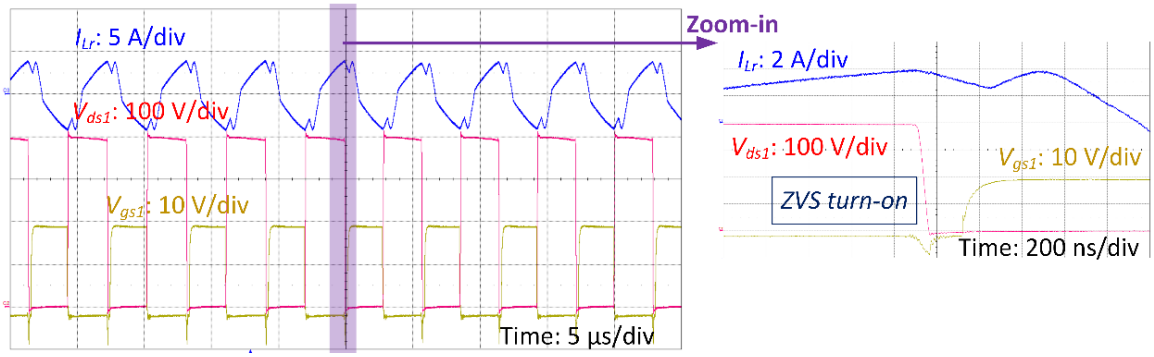
(c) P_o = 500W (25% load)

Figure 4.7. Line-frequency steady-state waveforms of SRCUI under HMM.

Figure 4.7(b) is zoomed-in at different output phase angles to demonstrate the details of HMM. The high-frequency waveforms in the VFM region are shown in Figure 4.8. Figure 4.8(a) is the waveforms at the crest and trough of the output, where $f_s = f_{min}$. As explained in the last section, f_{min} is almost the same as the series resonant frequency (f_r). Consequently, I_{Lr} looks like a sinusoidal wave without interruption. By the magnetizing current, $Q_1 – Q_4$ are able to obtain ZVS turn-on. In Figure 4.8(b), the inverter goes deep into the VFM region and f_s becomes 175 kHz. The waveform of I_{Lr} is no longer sinusoidal since it gets cut off early. The resulting turn-off current assists the ZVS of $Q_1 – Q_4$ and again removes the turn-on loss.



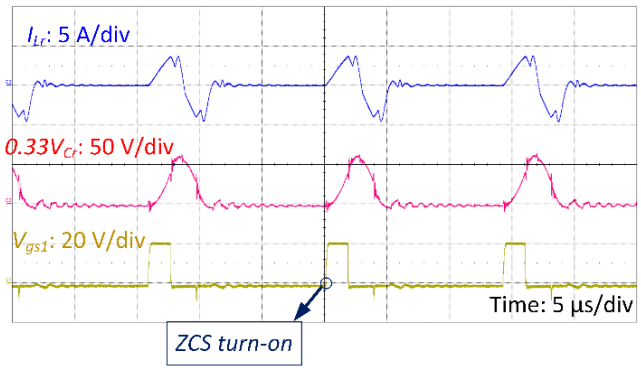
(a) $\theta_l = 0^\circ$, $\rho_p = 1$, $f_s \approx f_{min} = 80$ kHz.



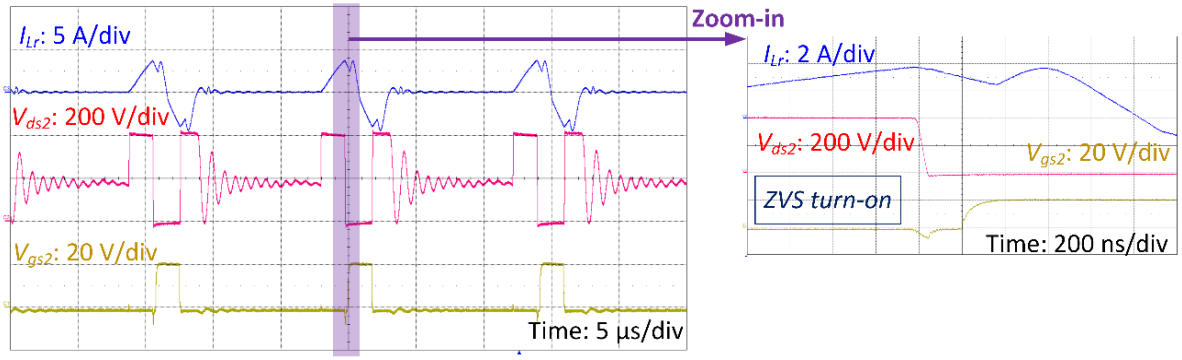
(b) $\theta_l = 60^\circ$, $\rho_p = 1$, $f_s = 175$ kHz.

Figure 4.8. High-frequency test waveforms in VFM region.

The high-frequency waveforms in the SPDM region are shown in Figure 4.9. Figure 4.9(a) is triggered by the first pulse using the gate-source voltage of Q_1. I_{Lr} is zero before the gate driving pulses and therefore Q_1 (and Q_4) turns on with ZCS. In Figure 4.9(b), the second pulse is used for triggering. By the resonant current built up within the first pulse, the drain-source voltage of Q_2 can be fully discharged, so it turns on with ZVS. Therefore, Q_2 (and Q_3) is free from the turn-on loss.

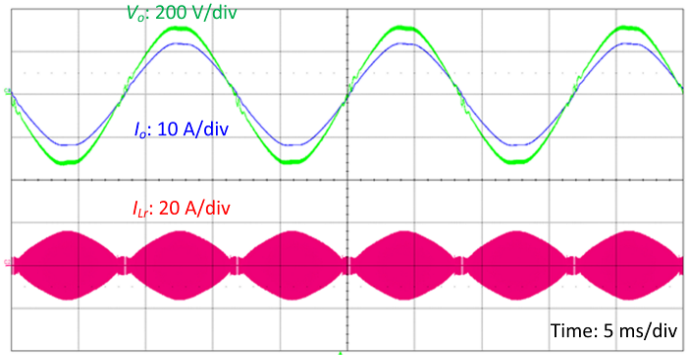


(a) High-frequency waveforms triggered with the first pulse. $\theta_l = 80^\circ$, $\rho_p = 0.32$, $f_s = f_{max} = 250$ kHz.

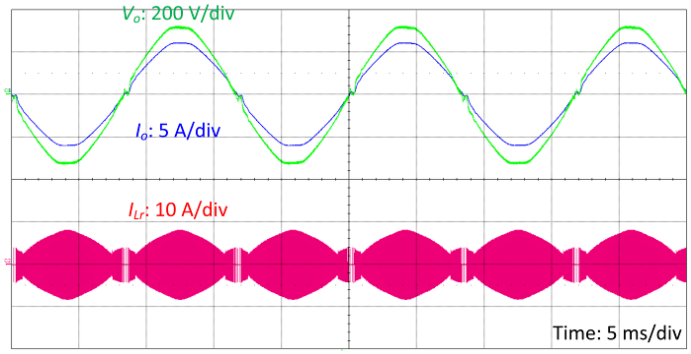


(b) High-frequency waveforms triggered with the second pulse. $\theta_l = 80^\circ$, $\rho_p = 0.32$, $f_s = f_{max} = 250$ kHz.

Figure 4.9. High-frequency test waveforms in SPDM region.



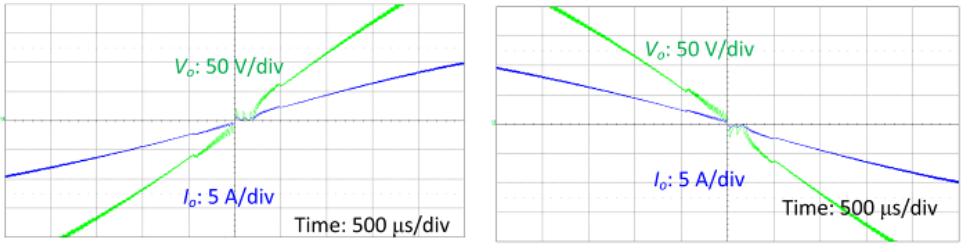
(a) 100% load.



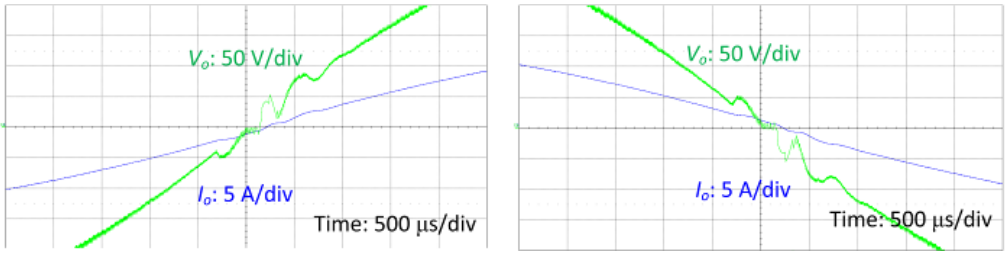
(b) 50% load.

Figure 4.10. Steady-state waveforms with R-L load.

In the scope of this dissertation, the diode rectifier of SRCUI is realized by diodes rather than active switches. Therefore, power flow is not allowed to return from the load to the source. Since only the output filtering capacitor (C_f) can take reverse current flow, the ability to handle reactive power is limited. Subsequently, the SRCUI in Figure 2.1 is not suitable for an inductive load like a motor, which may require a power factor lower than 0.9 [79]. This issue is not unique to SRCUI, but common to most PDIs [80].



(a) With pure resistive load.

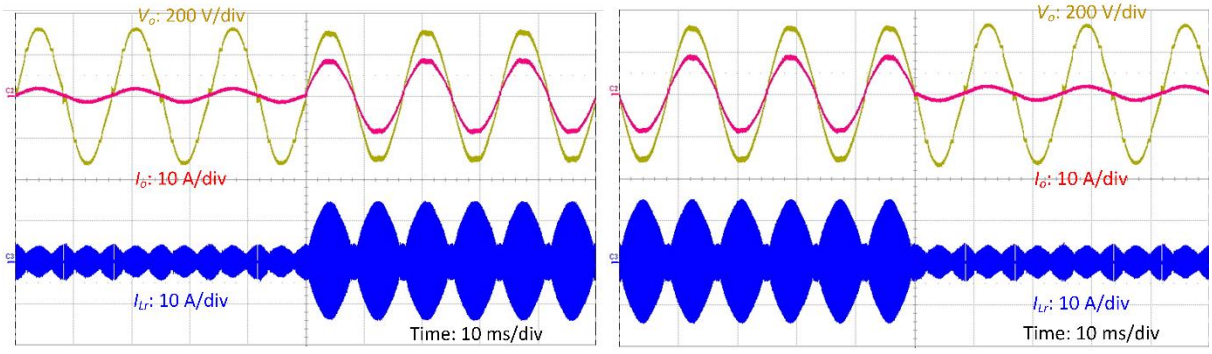


(b) With R-L load.

Figure 4.11. Zero-crossing-point waveforms with 100% load.

Even in standalone and gird-tied applications, a certain degree of reactive power capability is needed because of the grid inductance caused by a lengthy power cable, leakage inductance of a back-end line transformer, and/or other reasons. To test if the prototype has basic reactive power capability, an inductor of 4 mH is connected between the load and the inverter output. This emulates a grid inductance of 0.057 pu and a scenario between stiff grid condition and weak grid condition [81]-[82]. The test waveforms with the R-L load are shown in Figure 4.10, proving that the basic function of an inverter remains. However, minor distortion occurs in the output waveforms, so the THD of V_o drops to 2.38% and 3.13% for 100% and 50% load, respectively. The waveforms at ZCP are compared in Figure 4.11, with and without the extra inductor of 4 mH. With a purely resistive load, the output voltage and current are always in phase. However, with the extra inductor, there is a slight delay between the voltage and current waveforms, which leads to minor distortion.

Lastly, dynamic load tests are conducted between 15% and 90% load, as shown in Figure 4.12. The prototype works in a standalone application and it maintains the output voltage despite the load changes. The control of the inverter will be further discussed in the next chapter.



(a) Load step-up. (b)Load step-down.

Figure 4.12. Dynamic load test between 15% and 90% load.

4.4 Efficiency Analysis

4.4.1 Efficiency Measurement and Loss Breakdown

To evaluate the performance of the prototype with HMM, power efficiency is measured through digital power meter WT1030. The measurement includes all the power losses, except the gate driver loss and the loss from DSP and sensors. The results are plotted in Figure 4.13 along with the efficiency predicted by the power loss model in Section 4.1. The measurement and the model agree with each other at the half load, where efficiency peaks at more than 97.9%. Except for the data at the lightest load, the error of the model is less than 0.4%. This proves the validity of the developed power loss model.

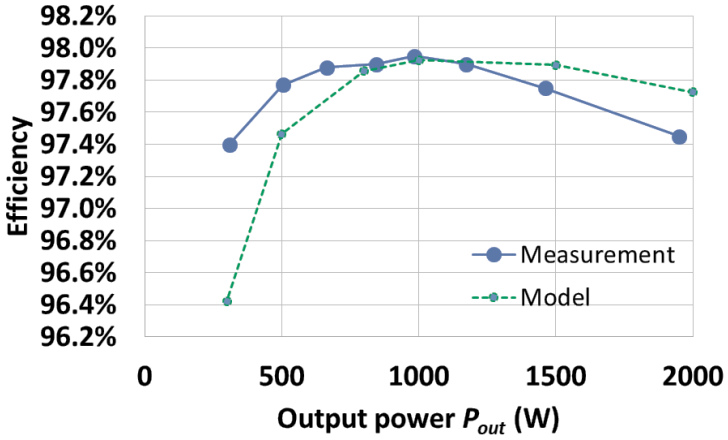


Figure 4.13. Measured power efficiency and predicted power efficiency.

The loss breakdown of the inverter is shown in Figure 4.14 and it helps identify the most significant loss components. Note that the losses in the transformer and the resonant inductor are combined in Figure 4.14. Since the inverter works in a step-down scenario, the secondary-side current is relatively large. Therefore, rectifier diode loss is the most significant under the full load. The turn-off loss is also important since it is the most significant loss under the half load and the quarter load. From the full load to the quarter load, the turn-off loss only drops by 38%. This can be attributed to the gain curve of SRC. At a fixed output phase angle, the f_s of the SRC is higher

with a lighter load. In other words, the "average f_s" over a line-cycle is higher with a lighter load, making the turn-off loss more significant over other losses. In addition, the core loss is subject to the load condition mainly because of the resonant inductor. Otherwise, the core loss of the transformer is dominated by the output voltage, with a little influence from the load through f_s. In Figure 4.14, the turn-on loss is the only one increasing with a lighter load. This is due to the expansion of the SPDM region and the fact that E_{oss} is independent of load condition. The tendency of the turn-on loss is certainly unfavorable, but it does not have a substantial impact on overall efficiency. The turn-on loss is kept below 2 W in Figure 4.14 and the credit belongs to multiple loss-reduction mechanisms: low equivalent switching frequency (= $\rho_p \cdot f_{max}$), elimination of channel loss, and the ZVS for Q_2, Q_3.

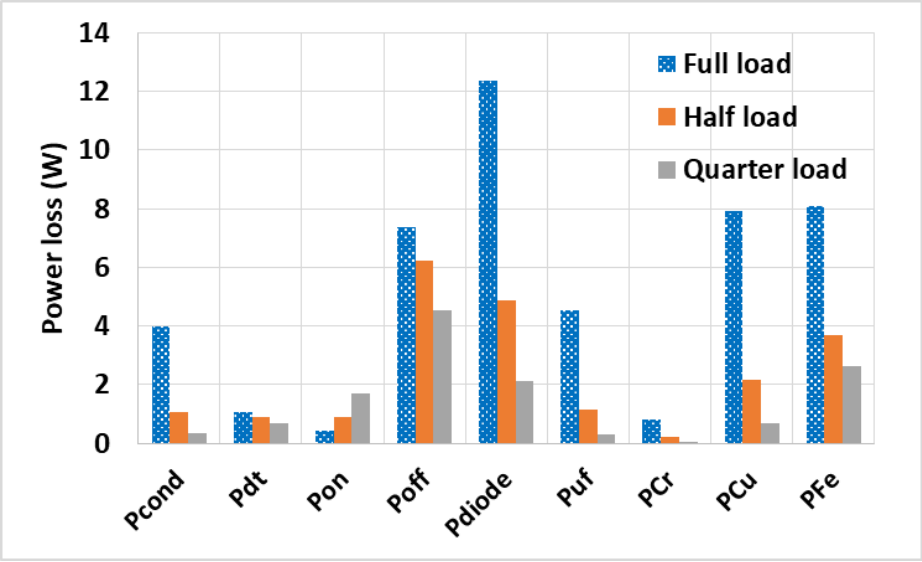


Figure 4.14. Loss breakdown of the prototype.

Figure 4.14 also implies the direction to further improve power efficiency in the future. To improve the full-load efficiency, one can replace the diode rectifier with active switches using the technique of synchronous rectification [83]. For instance, if $D_1 - D_4$ are replaced by SCT3030AL, the device of $Q_1 - Q_4$, the total diode loss at the full load can ideally be decreased by 55.3%. Consequently, the full-load efficiency will increase from 97.7% to 98.0%. In addition, the inverter

can benefit from advanced semiconductor technologies since switching losses still exist. For example, gallium nitride (GaN) devices have advantages in high-frequency, low-voltage (<1 kV) applications [84]-[85]. If GaN transistors GS66516T are applied for $Q_1 - Q_4$ instead, the turn-off loss can be reduced by 80% according to the device datasheets [86]. This can bring peak efficiency from 97.9% to 98.4%. The reduction in switching losses is even more important in an application with higher switching frequencies. Furthermore, the dead-time t_d is set as a constant in the prototype here. To reduce the dead-time loss, adaptive dead-time or ZVS detection techniques can be considered. In either way, the dead-time with a high turn-off current can be reduced to limit the current circulating through the body diodes. In a nutshell, the efficiency and switching frequencies of the SRCUI under HMM are not limited to the level presented in this dissertation. There is still room for improvement by applying advanced devices.

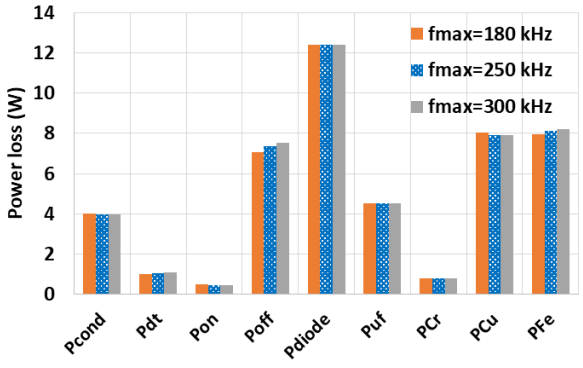
4.4.2 Selection of f_{max} and Z_r

Table 4.3. Boundary angle (θ_b) with different combinations of f_{max} and Z_r.

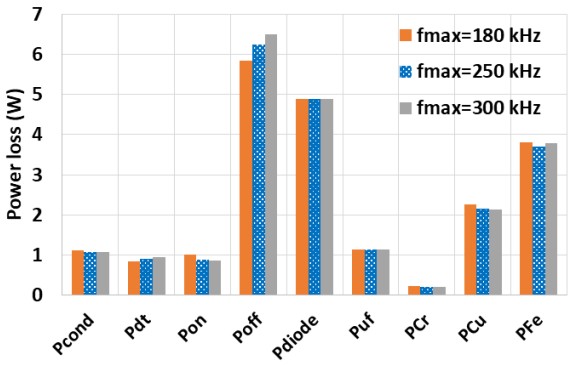
Case	f_{max}	Z_r	θ_b (P_o = 2 kW)	θ_b (P_o = 1 kW)	θ_b (P_o = 500 W)
i	250 kHz	60 Ω	79˚	69˚	55˚
ii	180 kHz	60 Ω	73˚	60˚	46˚
iii	300 kHz	60 Ω	81˚	73˚	60˚
iv	250 kHz	120 Ω	84˚	79˚	70˚
v	250 kHz	30 Ω	69˚	54˚	38˚

In previous sections, the selection of f_{max} has been discussed regarding its limitations caused by component capability, the ZVS of $Q_1 - Q_4$, and the resonant current peaks in the SPDM region. The discussion on f_{max} will be continued here, but in the aspect of power efficiency. The

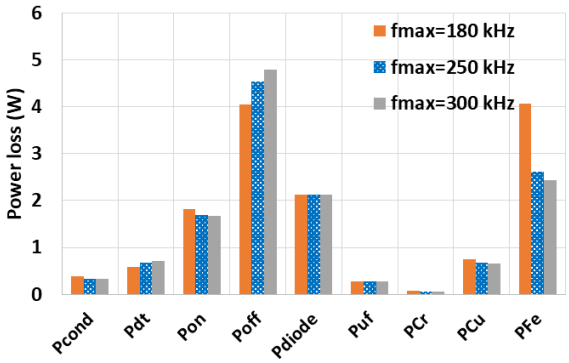
power losses are compared in Figure 4.15 with different f_{max}. All the calculations are based on the same prototype, so the θ_b can be summarized in Table 4.3.



(a) With full load.



(b) With half load.



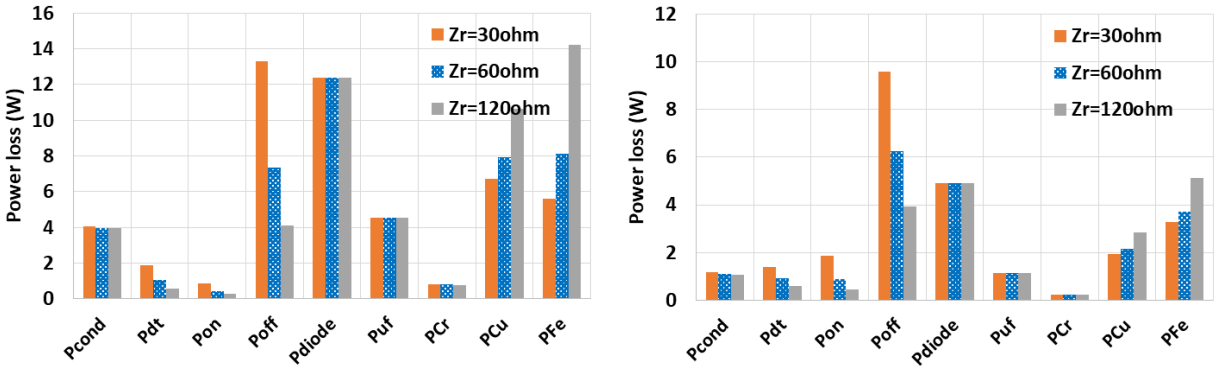
(c) With quarter load.

Figure 4.15. Power loss comparison between different f_{max}.

With a fixed Z_r of 60 Ω, *case ii* with 180-kHz f_{max} has the lowest θ_b, widest SPDM region and therefore it has the highest I_{Lr_rms} among the three. However, the increment in copper loss and conduction loss is negligible or neutralized by the reduction of the turn-off loss. Consequently, the efficiencies at the full load and the half are almost the same for *cases i*, *ii*, and *iii*. The differences are less than 0.05%. On the other hand, the quarter-load efficiency of *case ii* is about 0.2% less than the other two, and the efficiency drop mainly comes from the core loss of the transformer. The difference becomes more notable at the quarter load because the SPDM region becomes more prevailing. Given Figure 4.15 and the analysis above, a high f_{max} is preferred as long as it does not

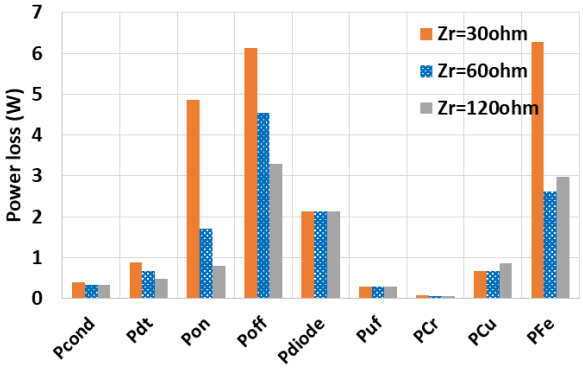
violate any restrictions. The main benefits are better light-load efficiencies and better output waveform quality.

In addition to different f_{max}, Table 4.3 also includes θ_b with different Z_r. When Z_r is increased to 120 Ω, L_r is doubled and C_r is halved. In here, we assume C_r keeps the same ESR and L_r keeps the same size and shape. Since L_r is proportional to the square of its number of turns, N_{Lr} becomes 1.414 times the original. With more number of turns, a thinner winding should be used and therefore R_{Lr} becomes 2 times the original. The new N_{Lr} and R_{Lr} for *case v* can be obtained in the same way.



(a) With full load.

(b) With half load.



(c) With quarter load.

Figure 4.16. Power loss comparison between different Z_r.

The power loss comparison between *case i*, *iv*, and *v* (different Z_r) is shown in Figure 4.16 and the efficiencies are compared in Figure 4.17. In *case v*, Z_r is only 30 Ω so its equivalent quality

factors are lower than the others. This means within a fixed interval in the VFM region, *case v* has the highest "average f_s" and subsequently the highest turn-off loss. At the quarter load, *case v* operates in the SPDM region for over half of the period, so its turn-on loss and transformer core loss become significant. As a result, the efficiency of *case v* is lower than the others in Figure 4.17. On the other hand, *case iv* has better half-load and quarter-load efficiency than *case i* due to the reduction of switching losses. However, its high core loss from the resonant inductor drops the full-load efficiency. In addition, the high L_r required in *case iv* would make the future integration of magnetic components difficult.

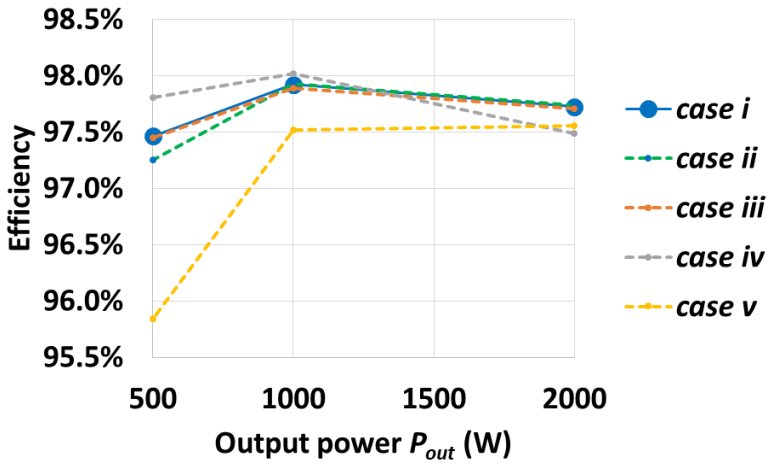
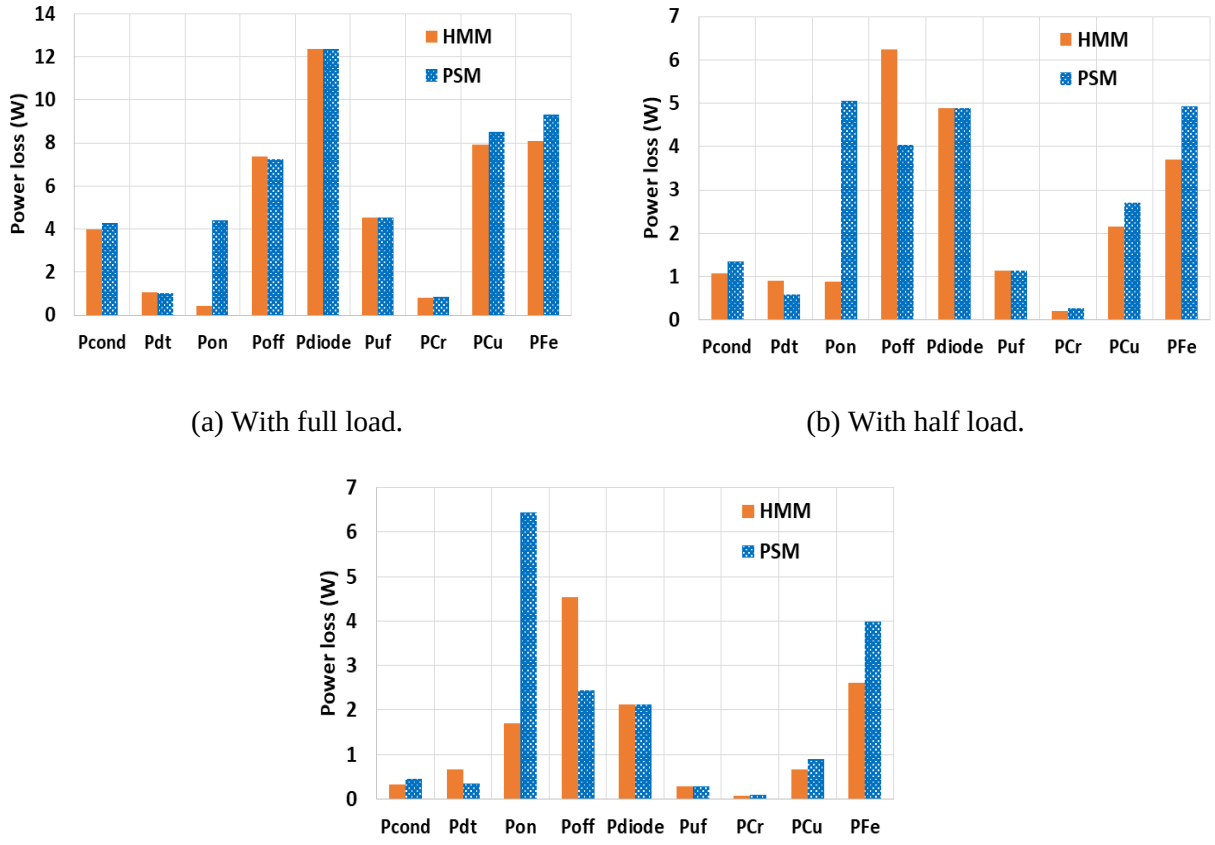


Figure 4.17. Efficiency comparison between different combinations of f_{max} and Z_r.

In reality, each new combination of f_{max} and Z_r triggers a new selection loop for components, so the optimized efficiency may differ from Figure 4.17. Nevertheless, a conclusion can be drawn for the prototype in this chapter: high θ_b is preferred, whether through high f_{max} or high Z_r. It is arguable to apply this conclusion to every SRCUI, but it can be treated as a general rule given all the design requirements (e.g., ZVS in the VFM region) are met. After all, the power delivery in the SPDM region is naturally uneven and concentrated within the time when gate signals are fired.

4.4.3 Comparison between HMM and PSM

In a practical application, VFM may not be considered because of its limited modulation range. PDM may not be considered either, because of the terrible output waveform demonstrated in Figure 3.17, and the tremendous current stress demonstrated in Figure 3.18. This leaves PSM as the only mature basic modulation method. The hard-switching of PSM is undesired, but the inverter can still operate.



(a) With full load.

(b) With half load.

(c) With quarter load.

Figure 4.18. Power loss comparison between HMM and PSM.

Therefore, it is worthwhile to compare the power loss breakdown between HMM and PSM, as shown in Figure 4.18. The HMM and PSM are applied to the same prototype. As expected, PSM has a higher turn-on loss with all the load conditions. The turn-on loss of PSM is even higher with the quarter load because the turn-off current for ZVS becomes smaller. Also, the conduction

loss of PSM is higher due to more circulating current. On the other hand, HMM has higher turn-off loss despite a lower turn-off current in the high-output region (cf., Figure 3.22). This is caused by the higher f_s of HMM. The measured power efficiencies are compared in Figure 4.19.

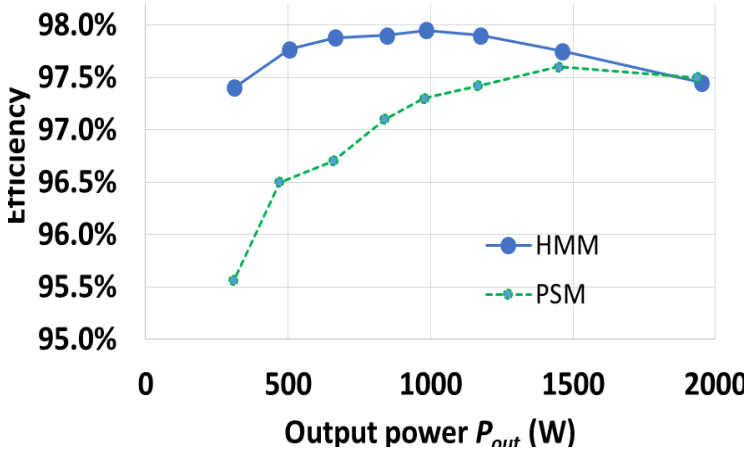


Figure 4.19. Efficiency comparison between HMM and PSM.

In terms of efficiency, PSM is only 0.23%, 0.33%, and 0.74% lower than HMM, with the full load, half load, and quarter load respectively. The efficiency difference will be further enlarged if the prototype adopts higher f_s since the total switching loss of PSM is higher. Moreover, in SiC MOSFET SCT3030AL (650 V, 30 mΩ), the turn-on energy is twice of the turn-off energy at switching voltage/current of 400V/20A. But with the same switching voltage/current, the turn-on energy of GaN HEMT GS66516T (650 V, 25 mΩ) is about 8 times of the turn-off energy [86]. This implies HMM is even more advantageous if GaN devices are used for Q_1 – Q_4.

Chapter 5

Modeling and Control

in Standalone Applications

5.1 Background

In the scope of this dissertation, SRCUI is designed and tested in standalone applications and this chapter will provide guidance for controller design. More specifically, the focus will be put on the VFM region as the control of the SPDM region has been described in Figure 3.13. Besides, the VFM region is normally the longer one in HMM. To begin with, the background information of inverter control will be briefly introduced in this section.

In a regular full-bridge inverter, the small-signal plant model has constant coefficients independent of the output phase angle [87]. Therefore, the compensator also remains constant during a steady-state operation. In standalone applications, the main duty of an inverter is to form a grid voltage. Even so, current sensing is often implemented at output filtering inductor or capacitor. The additional current information can lead to a multi-loop control scheme that features a faster dynamic response [88].

However, not every inverter has a concise plant model and FC-PDI (introduced in Chapter 1) is a good example. In [89], the control-to-primary current transfer function of a specially controlled CCM FC-PDI has a pole at 0 Hz and a moving left-half-plane (LHP) zero. The gain of the transfer function at 100 Hz varies with grid voltage, and the LHP zero varies with both grid

voltage and power level. Therefore, it is suggested to identify the corner cases and design correspondingly to avoid instability.

The plant model of an FC-PDI directly relates to its flyback converter, since the unfolder is not engaged in the high-frequency operation. Similarly, to find out the plant model of SRCUI, one should begin with the plant model of SRC/LLC resonant converter. To facilitate the experiment, the parameters of SRCUI in this chapter are changed to Table 5.1.

Table 5.1. Circuit parameters of SRCUI in Chapter 5.

Parameters	Value	Parameters	Value
V_{in}	50 V	L_r	12.7 μH
V_{out}	50 V_{rms}	C_r	200 nF
P_{out}	0 – 150 W	L_m	56 μH
n	0.667	f_r	99.8 kHz
C_f	1 μF	f_s	100 – 300 kHz

5.2 Plant Model in VFM Region

The modeling of resonant converter is not an easy task as the conventional state-space averaging method cannot preserve the details regarding the beat frequency dynamics, an interaction between the switching frequency and the natural resonant frequency [90]. Different approaches have been attempted to accurately capture the beat frequency dynamics, but most of them lack physical insights and are numerical methods. Nevertheless, a third-order equivalent circuit model of SRC was proposed in [90], and it achieved a good balance between accuracy and simplicity. Later, the result is extended to LLC resonant converter and creates equivalent circuit models for $f_s \geq f_r$ and $f_s < f_r$ respectively [91].

In previous chapters, the effect of L_m can be neglected in many circumstances, yet it has a great impact on the small-signal plant model. The voltage gain curves of SRC and LLC resonant converter have been plotted in Figure 2.3, and the slope of the curves represents dV_o/df_s, namely the dc gain of the control-to-output transfer function. In an SRC, the slope at $f_s = f_r$ is zero, but in an LLC resonant converter, it is not always zero. Therefore, without diving into small-signal models, we know the dc-dc stage here cannot be simplified as an SRC.

By applying the conclusion in [91], the small-signal equivalent circuit model can be derived in Figure 5.1. L_e and C_e dominate the double pole location of the system, while R_{ed} provides the damping effect. Their expressions can be found in (5.1) – (5.4), which include the beat frequency dynamics. Note that $\omega_s = 2\pi f_s$, $\omega_r = 2\pi f_r$ and $\omega_n = \omega_s/\omega_r$. In addition, the gain terms regarding the switching frequency are listed in (5.5) and (5.6).

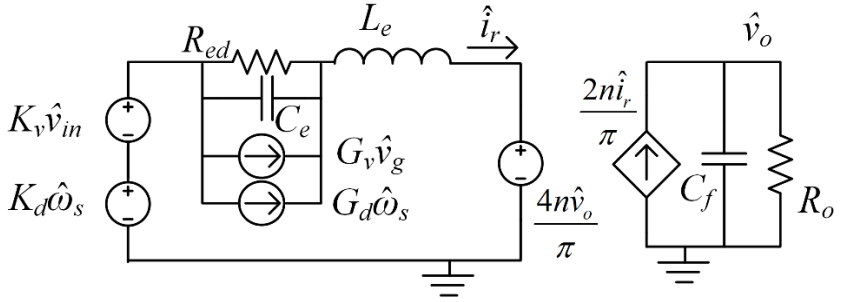


Figure 5.1. Small-signal equivalent circuit model of an LLC converter ($f_s > f_r$).

$$L_e = L_r\left(1+\frac{\omega_r^2}{\omega_s^2}\right) \tag{5.1}$$

$$C_e = \frac{1}{L_e(\omega_s-\omega_r)^2} \tag{5.2}$$

$$R_{ed} = \frac{L_e\left|X_{eq}\right|\left|\omega_s-\omega_r\right|}{R_e} \tag{5.3}$$

$$X_{eq} = \omega_s L_r - \frac{1}{\omega_s C_r} \tag{5.4}$$

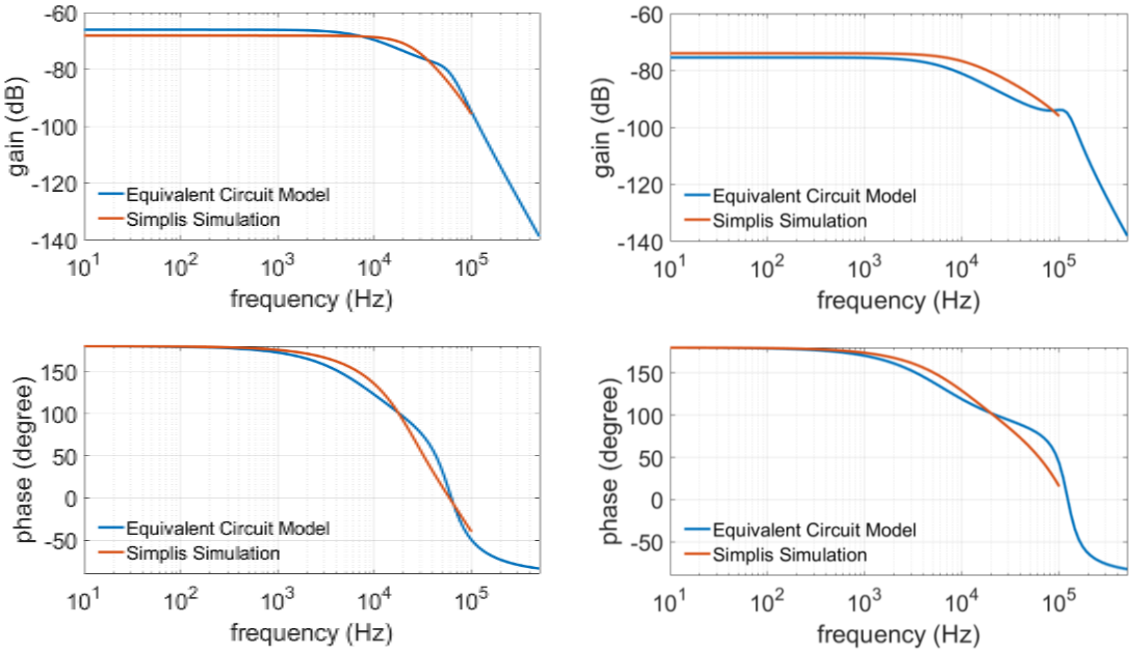
$$K_d = \frac{-8V_{in}}{\pi\omega_r L_n} \tag{5.5}$$

$$G_d = \frac{4V_{in}L_n}{\pi\omega_r R_{ed}} \tag{5.6}$$

With the small-signal equivalent circuit model, the control-to-output transfer function (G_{vf}) can be derived in (5.7) with its dc gain (K_{DC}) in (5.8). On top of the fruitful verification works in [91], the results of the model are also compared to the results of an ac analysis performed in Simplis, as shown in Figure 5.2.

$$G_{vf} = \frac{\hat{v}_o(s)}{\hat{\omega}_s(s)} = K_{DC}\frac{X_{eq}{}^2 + R_e{}^2}{(s^2 L_e{}^2 + sL_eR_e + X_{eq}{}^2)(1 + R_oC_f s) + R_e(sL_e + R_e)} \tag{5.7}$$

$$K_{DC} = \frac{V_{in}L_n}{n\omega_s}\frac{(\frac{1}{\omega_n{}^2} - \omega_n{}^2)(Q_eL_n)^2 - (L_n + 1 - \frac{1}{\omega_n^2})(\frac{2}{\omega_n^2})}{\left(\sqrt{(L_n + 1 - \frac{1}{\omega_n^2})^2 + ((\frac{1}{\omega_n} - \omega_n)Q_eL_n)^2}\right)^3} \tag{5.8}$$



(a) f_s = 150 kHz. (b) f_s = 200 kHz.

Figure 5.2. Comparison of G_{vf} between the small-signal equivalent circuit model and Simplis simulation.

(5.7) and (5.8) indicate that both K_{DC} and the pole locations are subject to f_s. Since f_s changes with θ_l (cf., Figure 3.7) in the VFM region, K_{DC} is also a function of θ_l. Figure 5.3 shows how K_{DC} varies with θ_l and the load condition. K_{DC} tends to be higher with a heavier load and drops to zero at ZCP. This again matches the trends that appear in the gain curves of Figure 2.3(b): (i) the slope is steeper with a larger Q_e, which can be caused by a heavier load. (ii) The curves are gradually flattened out as they approach infinite f_s.

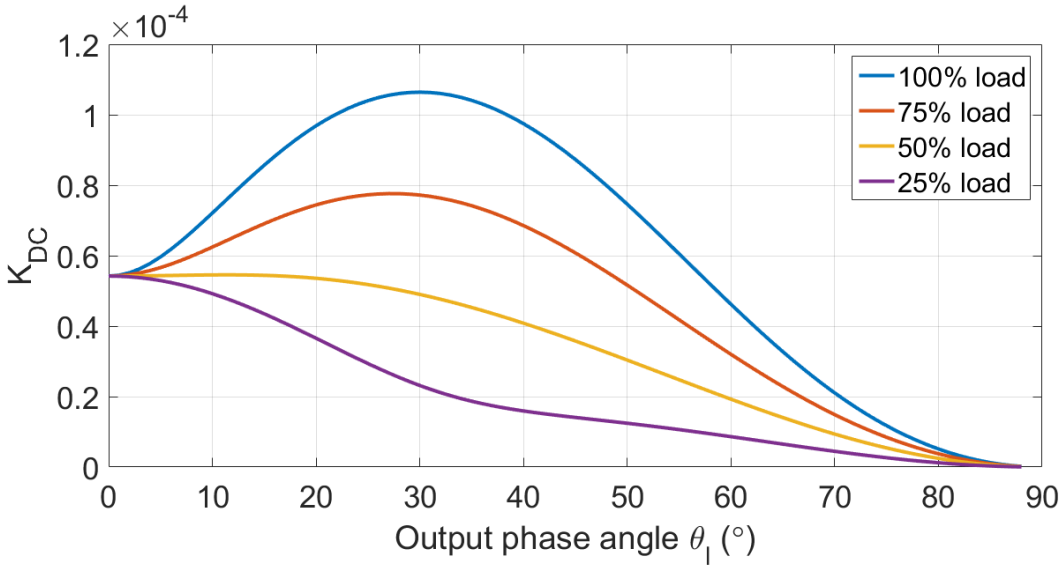


Figure 5.3. K_{DC} over output phase angle (θ_l).

There are a double pole and a single pole in the plant model, and the pole locations with different θ_l are plotted in Figure 5.4. When θ_l is low, the double pole is lower than the single pole. The order is reversed when θ_l is high, which demonstrates the moving nature of the pole locations. Using Figure 5.4, the pole locations are summarized in Table 5.2.

Table 5.2. Pole locations of G_{vf} with different θ_l (P_{out} = 150 W).

$\boldsymbol{\theta_l}$	**1°**	**16°**	**31°**	**46°**	**61°**	**76°**
Single pole location (kHz)	36.1	37.4	32.1	10.7	6.53	5.3
Double pole location (kHz)	13.4	14.2	18.4	43.9	95.2	260

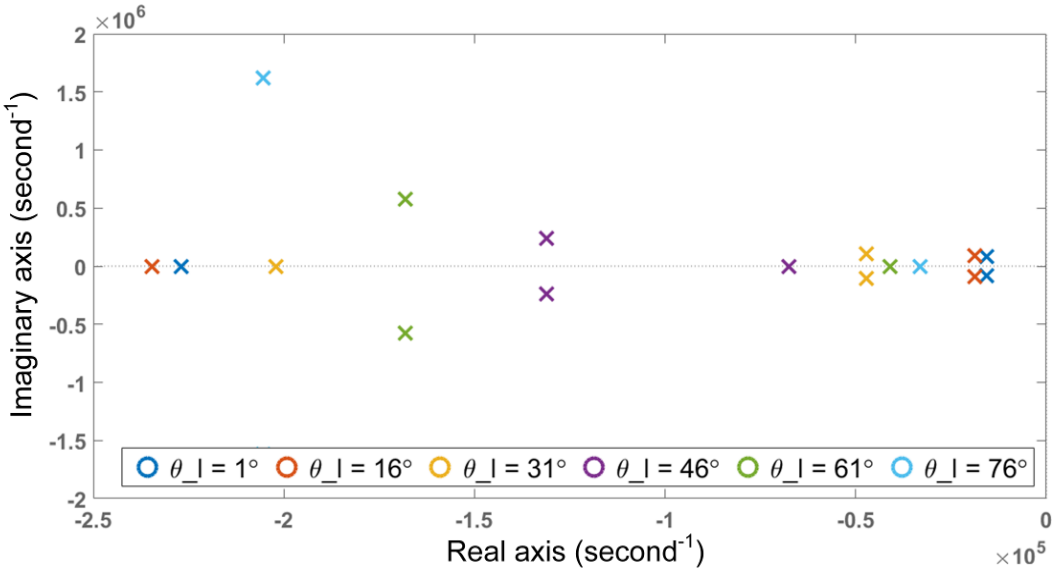


Figure 5.4. Pole-zero plot of G_{vf} with P_{out} = 150 W.

5.3 Gain-Varying Compensator Design

It would be a difficult task to compensate the poles of the plant model given their wide moving range as demonstrated in Table 5.2. Since the inverter system here does not need an ultra-fast bandwidth, the compensator design will simply avoid the poles. In addition, given the complexity of (5.8) and the limited calculation speed in a DSP, maintaining a unified loop gain is hard to be realized. Therefore, a PI compensator with a proposed simple gain-varying method will be introduced to control the output voltage in the VFM region. The control block diagram in the VFM region is plotted in Figure 5.5, where T_{fv} is the compensator. Before diving into the details about the compensator, other control blocks should be explained first.

Both V_o and I_o are sensed and the sensing signals pass through a voltage/current transducer (H_v/H_i) and a low-pass-filter (LPF_v/LPF_i). The transducers convert signals to a value within 0 V and 3.3 V for the DSP. The low-pass-filters get rid of high-frequency noises. The sensing of I_o in Figure 5.5 has low bandwidth. It is added to acquire the load condition, rather than join the cycle-by-cycle compensation like in a regular standalone full-bridge inverter. In a DSP, the sensing

signals are read by ADC that is triggered by a clock signal (e.g, ePWM module). Therefore, the sensing signals may not be read in an instant and such a delay is referred to as the zero-order-hold (*ZOH*). In the prototype, the ADC performs at a fixed sample time (T_{ADC}) so *ZOH* can be estimated by (5.9) [92]. In a standalone application, the reference voltage (V_{ref}) can be generated within the controller, and the error between V_{ref} and the sensed V_o is sent to the compensator. The compensator then outputs a new f_s, but it will not be updated until the end of an ePWM cycle (the exact update timing depends on the configuration in a DSP). Such an updating delay is typically modeled as Z^{-1} in (5.10) [92]. Finally, the DSP generates the gate signals for Q_1 – Q_4 and sends them to the power stage of an SRCUI.

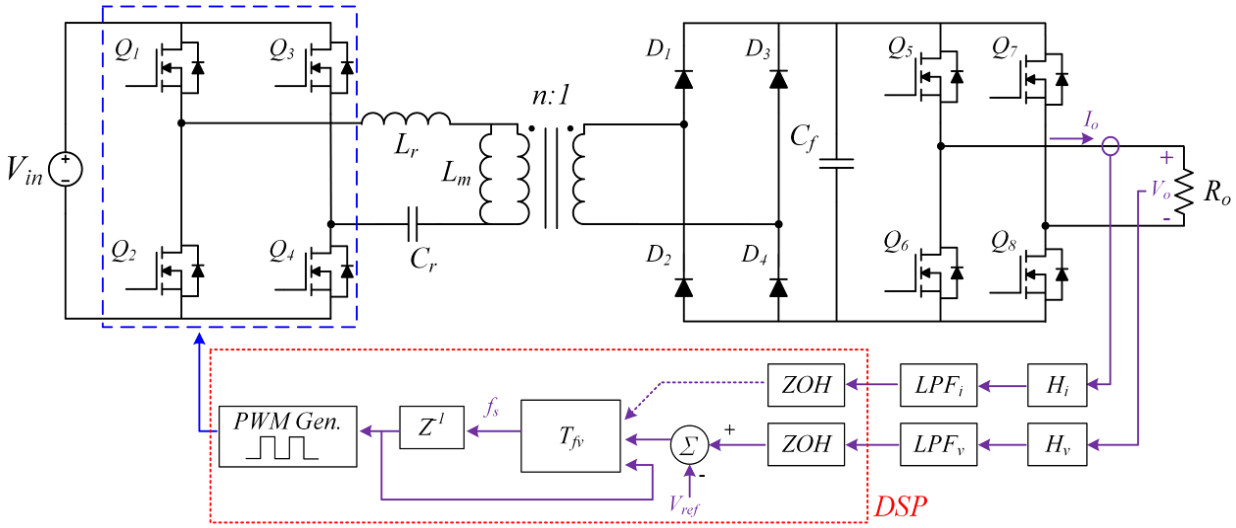


Figure 5.5. The control block diagram in the VFM region.

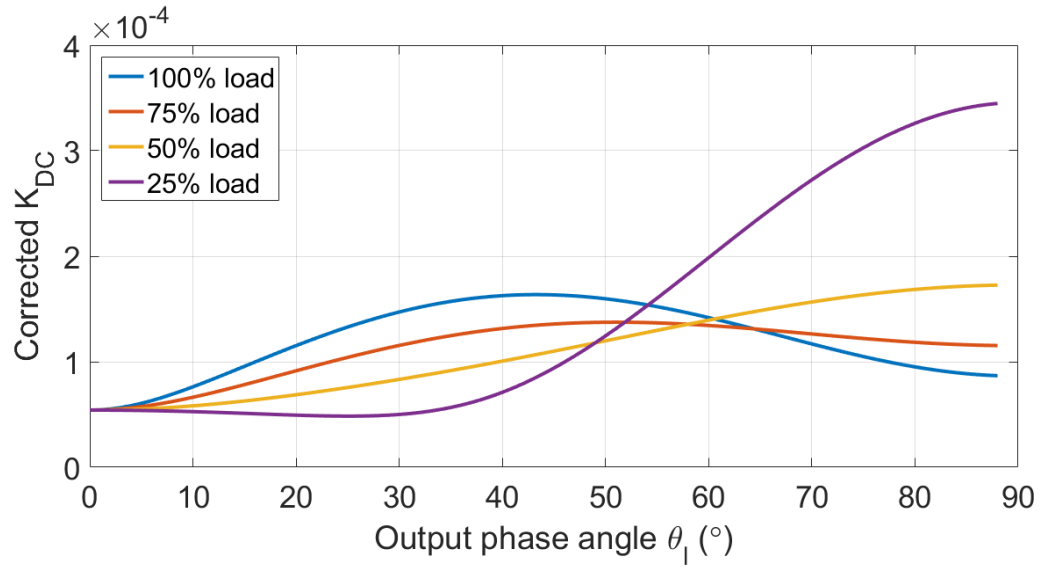
$$ZOH = \frac{1 - e^{-sT_{ADC}}}{sT_{ADC}} \tag{5.9}$$

$$Z^{-1}(s) = e^{-sT_s} \tag{5.10}$$

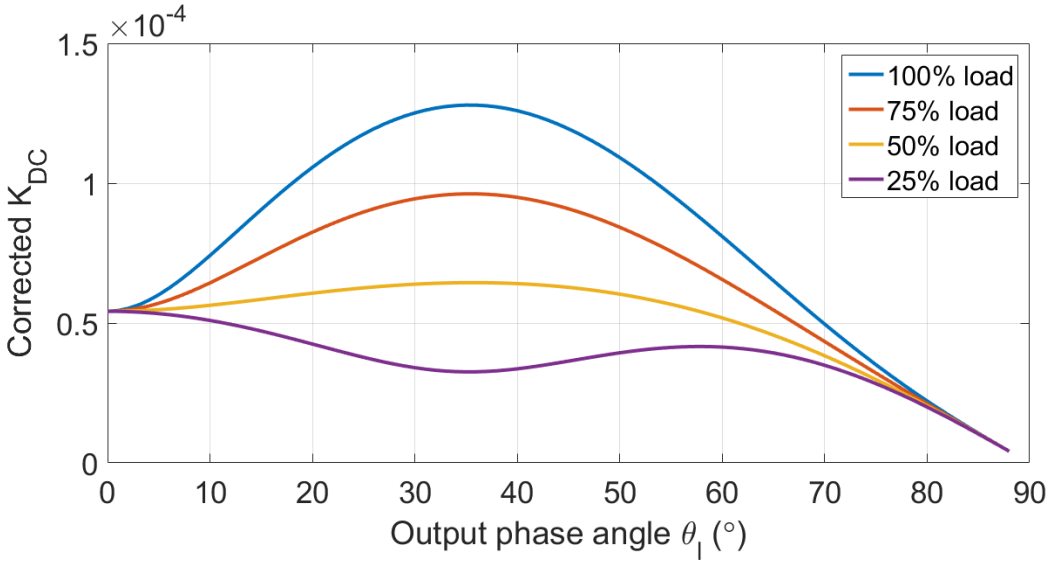
Based on Figure 5.5, the voltage loop gain (T_v) can be written in (5.11) and G_{vf}' represents the loop gain without the T_{fv}. Hence, G_{vf}' can be used as a reference for compensator design. In the prototype, the ADC sampling frequency is 200 kHz and the update on f_s is performed every

switching-frequency cycle. These are much higher than the lowest pole location in Table 5.2, so the digital delay effects do not have a critical influence on the phase margin.

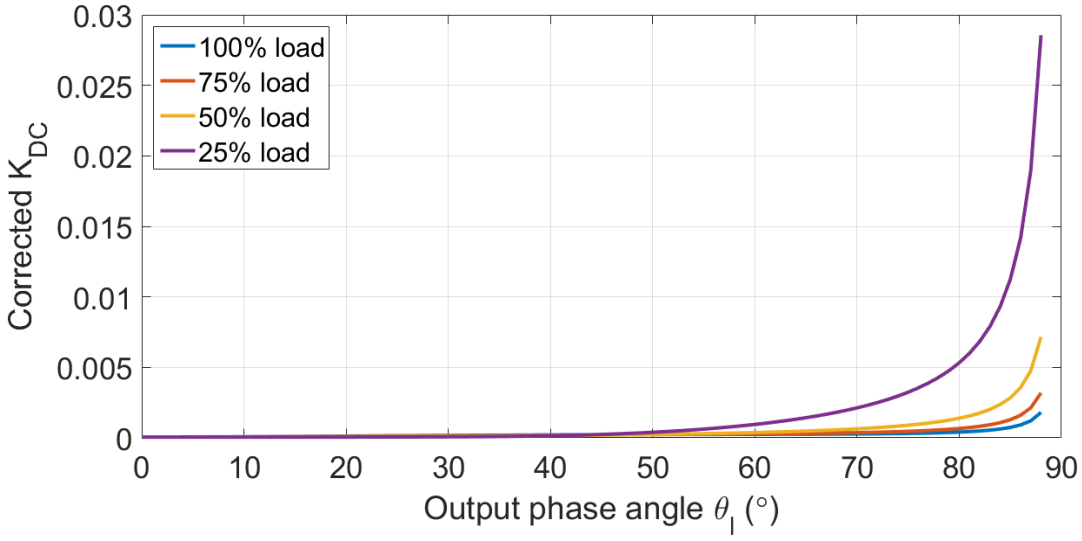
$$T_v = G_{vf} H_v (LPF_v)(ZOH) Z^{-1} T_{fv} = G_{vf}^{'} T_{fv} \tag{5.11}$$



(a) Proposed.



(b) Proportional to f_s.



(c) Proportional to f_s^3.

Figure 5.6. K_{DC} after gain-varying method over output phase angle (θ_l).

The PI compensator with a simple gain-varying method is proposed as (5.12). The corner frequency is fixed and the gain is subject to f_s. When $\theta_l = 0^\circ$ ($f_s \approx f_{min}$), the gain is basically unchanged. But in low-output regions, the gain of the compensator is boosted because of higher f_s. In addition, as mentioned in section 4.4, the average f_s is higher with a lighter load, so the gain-varying method also increases the gain with a light load. The proposed method only utilizes two steps of multiplication, so the calculation time in a digital controller is short. In (5.12), $(f_s/f_{min})^2$ can be considered as a "correction term" that corrects the variance in the dc gain of the plant model. To evaluate the effect of the gain-varying method, the "corrected K_{DC}" ($=(f_s/f_{min})^2 \cdot K_{DC}$) is plotted in Figure 5.6(a), since all the other terms in T_v are independent of θ_l and R_o at 0 Hz. Compared to Figure 5.3, the corrected K_{DC} is more concentrated and no longer drops to zero. Although K_{DC} with the 25% load seems excessive in the low-output region, the SRCUI has already switched to the SPDM region when $\theta_l = 48^\circ$. Additionally, Figure 5.6(b) and (c) show the corrected K_{DC} with the formula $(f_s/f_{min}) \cdot K_{DC}$ and $(f_s/f_{min})^3 \cdot K_{DC}$ instead. In Figure 5.6(b), the effect of correction is not

enough so the variance is still clear. In Figure 5.6(c), the gain in the low-output region becomes too much. This explains why the gain-varying method is specifically designed as (5.12).

$$T_{fv} = k_p\left(1+\frac{k_{i0}}{s}\right)=\left(k_{p0}(\frac{f_s}{f_{\min}})^2\right)\left(1+\frac{k_{i0}}{s}\right) \tag{5.12}$$

Finally, the sensed I_o is unrelated to T_{fv} here and it is used by the controller only to determine θ_l. Nevertheless, it is always an option to update T_{fv} based on I_o along with the update of θ_l. Such a low-frequency update can help improve steady-state output waveform quality.

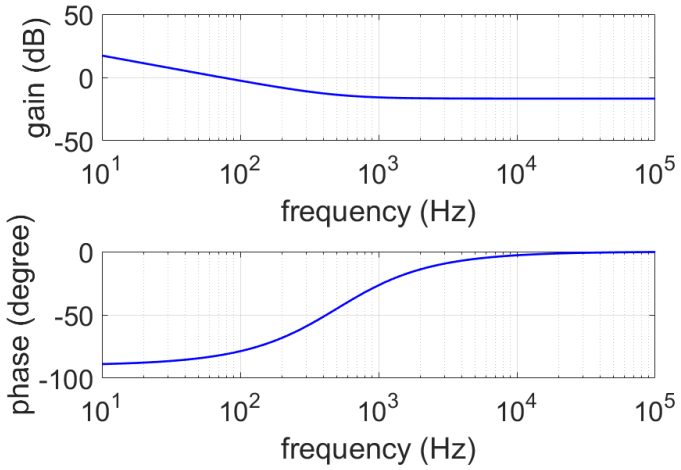
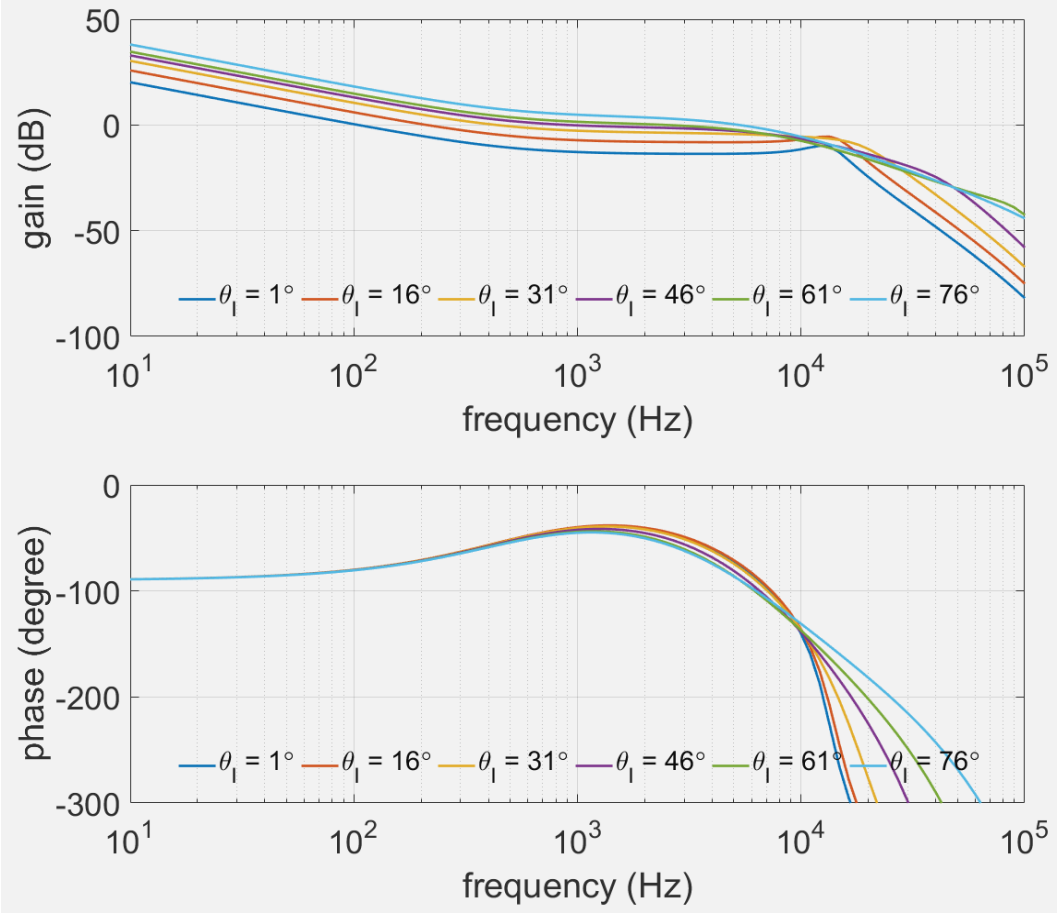


Figure 5.7. Compensator (T_{fv}) with k_{po} = 0.1, k_{io} = 2π·500 and f_s = 118 kHz.

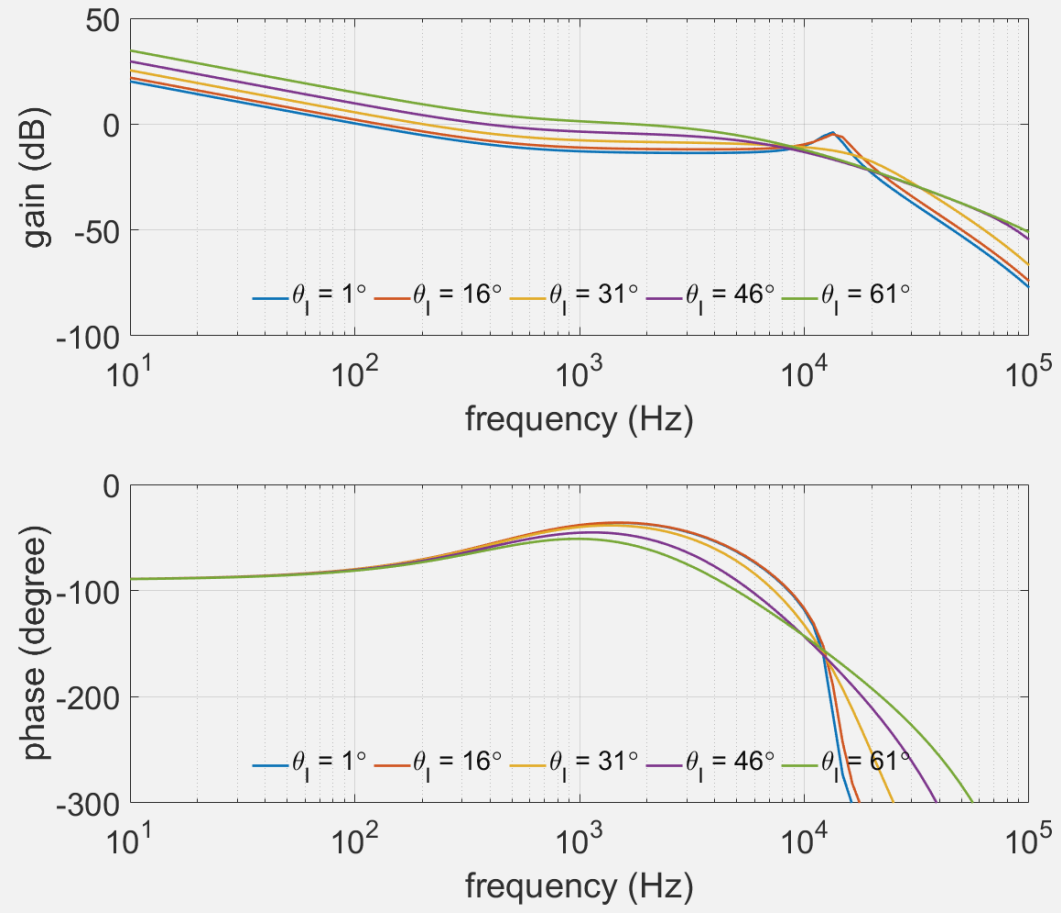
Besides the gain-varying method, the coefficients k_{po} and k_{io} in (5.12) should also be designed. In Table 5.2, the lowest pole of G_{vf} is located at 5.27 kHz, so the control loop crossover frequency is expected to lie between 60 Hz and 5 kHz. Therefore, the corner frequency (f_{corner}) is set at 500 Hz, and k_{io} is calculated by (5.13). In this way, the phase drop of T_{fv} has limited overlap with the phase drop of G_{vf} and the digital delay effects. Next, k_{po} should be tuned to make the crossover frequency at all different θ_l fall into the desired range. For the prototype in this chapter, k_{po} is selected as 0.1 and a bode plot of T_{fv} is exemplified in Figure 5.7. Finally, the loop gains at different θ_l are plotted in Figure 5.8 and the relevant information is summarized in Table 5.3. Over the entire operating range, the crossover frequencies are scattered in a wide spectrum. From the

perspective of phase margin, the system has a conservative feedback control design that meets the stability requirement of most applications [93]-[94]. In this dissertation, there are no specific application scenarios assigned to SRCUI, so there are no specific bandwidth requirements. If the bandwidth is insufficient, especially in the high-out region, one will have to consider a more aggressive approach that actively compensates for the moving poles.

$$k_{i0} = 2\pi f_{corner} \tag{5.13}$$



(a) P_o = 150 W.



(b) P_o = 75 W.

Figure 5.8. Voltage loop gain (T_v) with different θ_l.

Table 5.3. Phase margin, gain margin, and crossover frequency of the voltage control loop (T_v).

θ_l (P_o = 150 W)	**1˚**	**16˚**	**31˚**	**46˚**	**61˚**	**76˚**
Crossover frequency	126 Hz	264 Hz	497 Hz	910 Hz	2.5 kHz	5.2 kHz
Phase margin	113.6˚	122.1˚	129.6˚	136.8˚	125.5˚	90.6˚
Gain margin	10.1 dB	5.7 dB	6.4 dB	10.0 dB	13.2 dB	14.5 dB
θ_l (P_o = 75 W)	**1˚**	**16˚**	**31˚**	**46˚**	**61˚**	
Crossover frequency	126 Hz	161 Hz	274 Hz	566 Hz	1.7 kHz	
Phase margin	114.1˚	117.5˚	123.9˚	129.1˚	122.7˚	
Gain margin	5.2 dB	5.5 dB	12.7 dB	18.1 dB	19.4 dB	

To implement the designed compensator in a DSP, equations for discrete PI controller have to be adopted (cf., (5.14) – (5.15)). Therefore, the previous coefficients of PI compensator are further transferred by Tustin transform and the equations can be found in (5.16) – (5.17).

$$e[n] = V_o[n] - V_{ref}[n] \tag{5.14}$$

$$f_s[n] = f_s[n-1] + k_{pz}e[n] + k_{iz}e[n-1] \tag{5.15}$$

$$k_{pz} = \frac{k_p}{T_s} + \frac{1}{2}k_p k_{io} \tag{5.16}$$

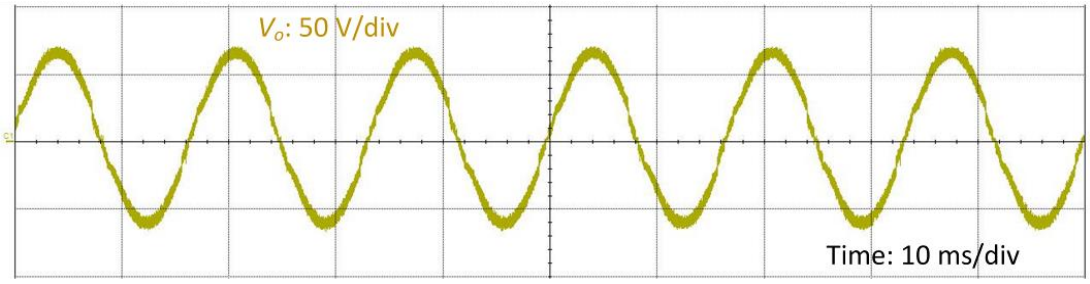
$$k_{iz} = \frac{-k_p}{T_s} + \frac{1}{2}k_p k_{io} \tag{5.17}$$

5.4 Experimental Verification

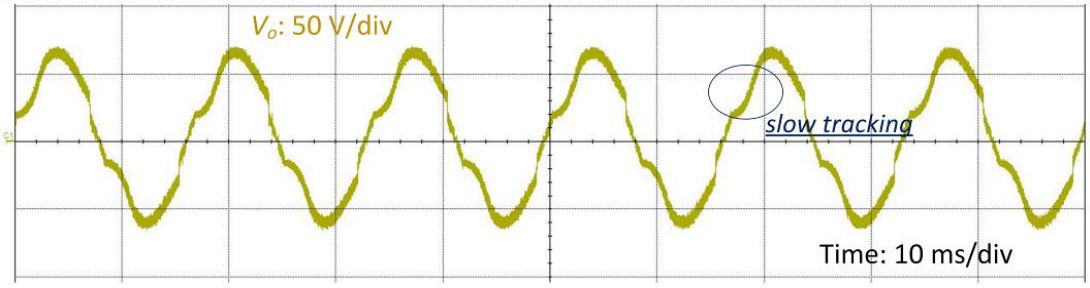
Due to the limitations of testing instruments, the loop gain cannot be directly measured, so time-domain output waveforms are used for verification instead. The experiments were performed with one of the circuit modules in Figure 6.10. The steady-state output voltage waveform based on the designed compensator is shown in Figure 5.9(a). On the other hand, Figure 5.9(b) is the waveform without the gain-varying method. At the crest and trough of the output, the compensator is the same as the original so the reference tracking is still accurate. However, the loop gain is insufficient in the low-output region, which leads to slow reference tracking and subsequent waveform distortion. As a result, the THD is 3.51% in Figure 5.9(a) but then drops to 11.99% in Figure 5.9(b).

In Figure 5.9(c), the compensator gain is doubled and still without the gain-varying method. Although the slow tracking in the low-output region is slightly alleviated, a sign of instability appears in the high-output region along with an audio noise. The reason is that the compensator gain at $\theta_l = 0^\circ$ is now doubled than in Figure 5.9(a), causing the decrement in phase margin. The THD in Figure 5.9(c) is only 8.29%. In conclusion, the necessity and effectiveness of

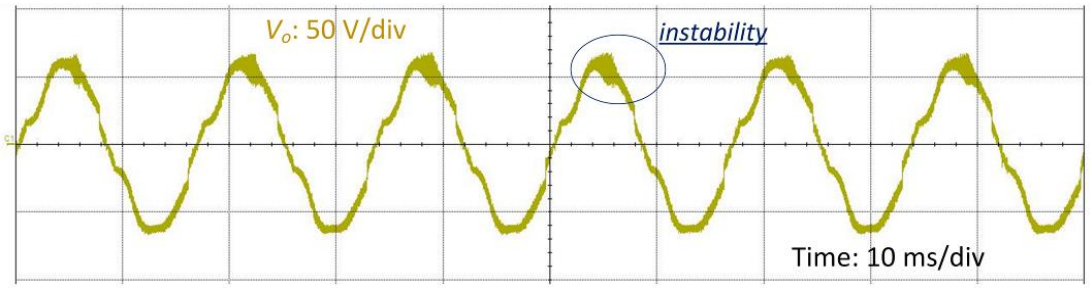
the gain-varying method are verified in Figure 5.9. The plant model of the LLC converter is doomed to vary in a cycle due to the changing nature of inverter output, and the proposed method helps reduce such a variance. Finally, a dynamic load test is conducted and proves the ability of the controller to maintain output voltage in a standalone application.



(a) With the gain-varying method.

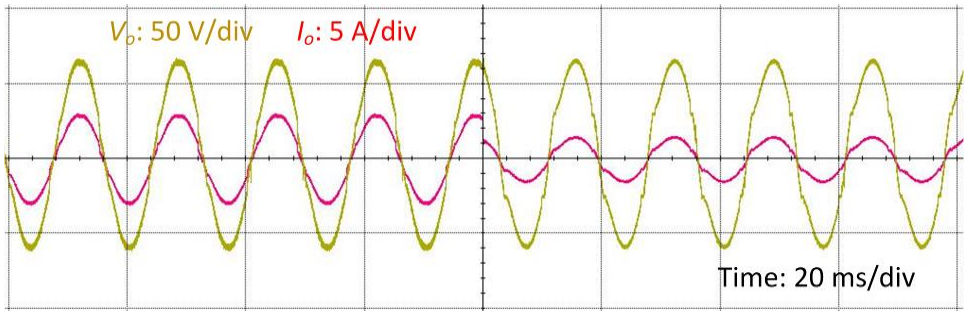


(b) Without the gain-varying method. $k_p = k_{po}$.

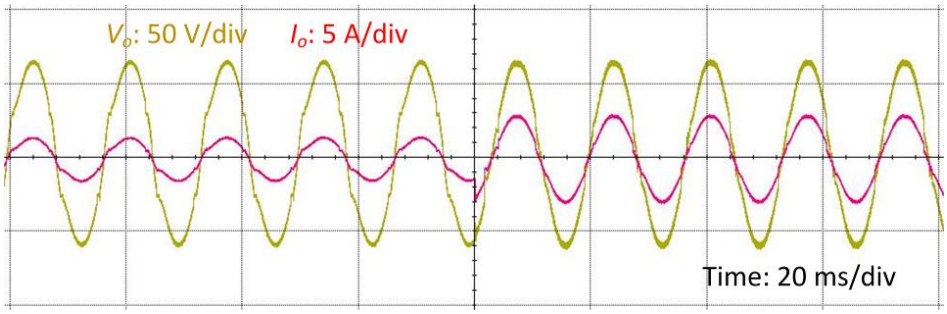


(c) Without the gain-varying method. $k_p = 2k_{po}$.

Figure 5.9. Output voltage waveforms with different compensator design (P_o = 150 W).



(a) From 150 W to 75 W.



(b) From 75 W to 150 W.

Figure 5.10. Dynamic load test.

Chapter 6

Sequential Waveform Synthesis

6.1 Background

Back in Chapter 1, it is mentioned that an isolated inverter has the advantage of modularity because its transformer allows the series/parallel connection with other modules. This can be useful for high-power, high step-up applications, like the power conversion from a solar farm to a medium-voltage grid [96]. In these applications, the dc-link inverter is commonly used as an individual module. An example is plotted in Figure 6.1, showing an input-parallel-output-series multi-modular inverter (MMI) based on dc-link inverters. The isolated dc/dc converters in Figure 6.1 have been realized with LLC resonant converter [97]-[98] and phase-shift full-bridge converter [99], which are suitable for medium to high-power applications. Before the harmonic filter, the output of the MMI has a discrete number of possible voltage levels, so the structure in Figure 6.1 can be referred to as multi-level inverters.

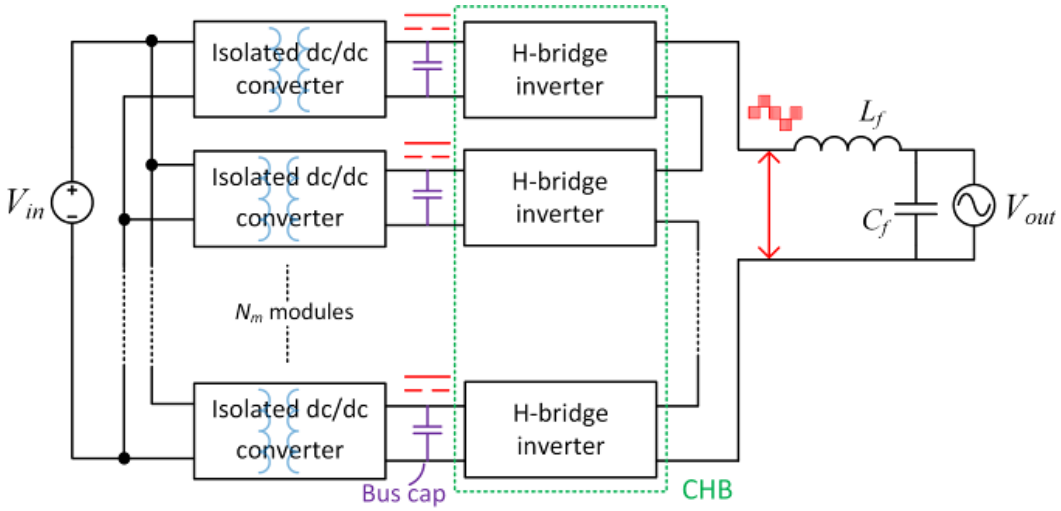


Figure 6.1. A multi-modular inverter based on dc-link inverters.

On the other hand, an MMI can also be composed of PDIs and inherit their advantages of power loss reduction (in the second stage), smaller bus capacitors, and so on. This concept has been realized with FC-PDI. Typically, the MMI based on FC-PDI has modular inputs paralleled with an interleaving technique to obtain a higher power capability [34], [36], [100]. In addition, all modules share an unfolder to reduce the total component count. Even so, the output power of the MMI is usually not greater than a few kW, since the poor transformer utilization of flyback converter still hinders. Alternatively, SRCUI can be used as a module for an MMI, and the system structure is plotted in Figure 6.2. Each module keeps its unfolder for the sake of device voltage rating and more control freedom. Since the bus voltages are no longer constant, the MMI in Figure 6.2 does not belong to multi-level inverters.

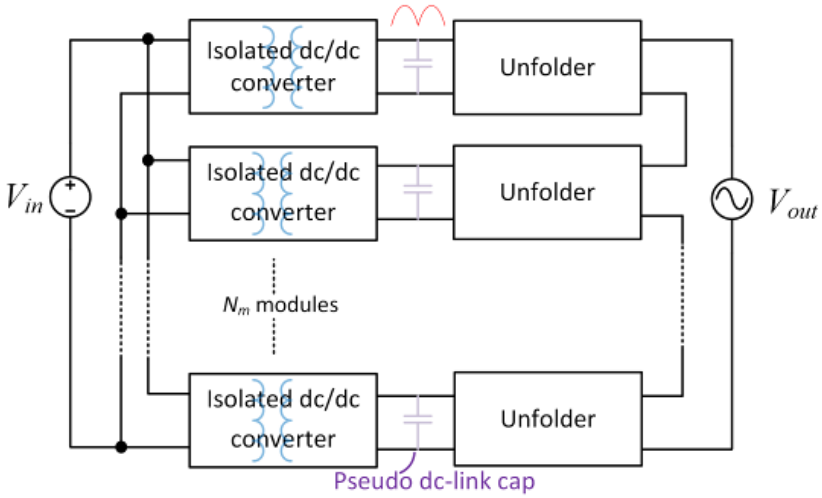


Figure 6.2. A multi-modular inverter based on PDIs.

In previous chapters, the modulation methods of SRCUI have been thoroughly studied, and the benefits of HMM have been presented. Ideally, HMM can be directly applied to the system in Figure 6.2 by duplicating the gate signals, which means the gate signals of the primary-side circuit of every module are identical and simultaneous. The gate signals of every unfolder are also synchronized. In this way, the output at each unfolder is sinusoidal and in phase with the other

unfolder outputs. Consequently, the total output is simply an individual output multiplied by the number of modules.

In Section 4.4, a general conclusion said that an extensive VFM region is preferred for the sake of efficiency improvement. Therefore, a control method termed sequential waveform synthesis (SWS) is proposed in this section. The operation of SWS requires multiple modules, so it is specifically designed for MMI. Compared to directly applying HMM, SWS can extend the VFM region and thus shorten the SPDM region. In some applications that use total demand distortion (TDD) as the standard of output waveform quality, SPDM may even be unnecessary. TDD is determined by the performance with full load [101], where SRCUI under VFM (plus SWS) has its best output waveform quality.

6.2 Principle of Operation

To focus on explaining SWS, the SRCUI in this chapter will operate with VFM only. In other words, the inverter is shut down in the low-output region. The MMI is exemplified with 3 modules so the system can be drawn as Figure 6.3. v_{CfX} and v_{uX} are the output capacitor voltage and output voltage of module X. Therefore, $v_{CfX} = |v_{uX}|$. Without SWS, the low-frequency waveforms of a module are plotted in Figure 6.4 and they are nothing more than the regular VFM waveforms. Here, we follow the custom in Chapter 3 to define θ_l. θ_l is 0˚ at the peak of the output voltage and 90˚ at the following ZCP. The cutoff angle (θ_{cut}) is where VFM stops. In fact, the theoretic THD of V_o can be calculated in a software tool if θ_{cut} is given, as shown in Figure 6.5. Not too surprisingly, lower θ_{cut} results in a higher THD. As a result, θ_{cut} can later be used to measure the effect of SWS. Without SWS, gate signals are the same for all modules, so the θ_{cut} of the MMI is the same as the θ_{cut} of an individual module.

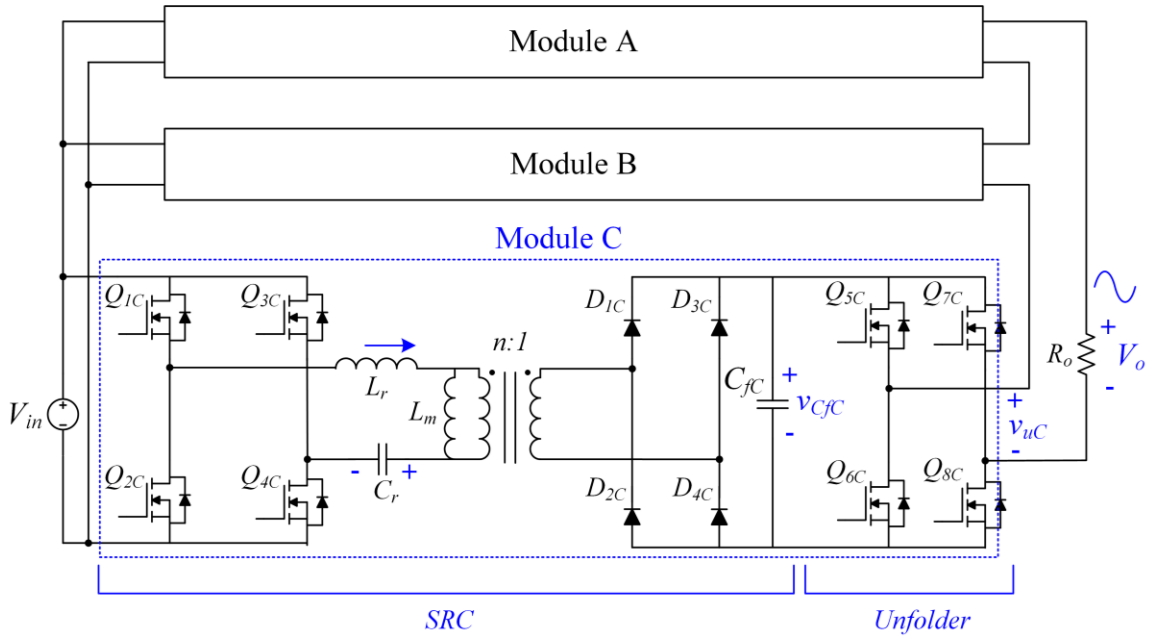


Figure 6.3. The topology of an MMI based on 3 SRCUIs.

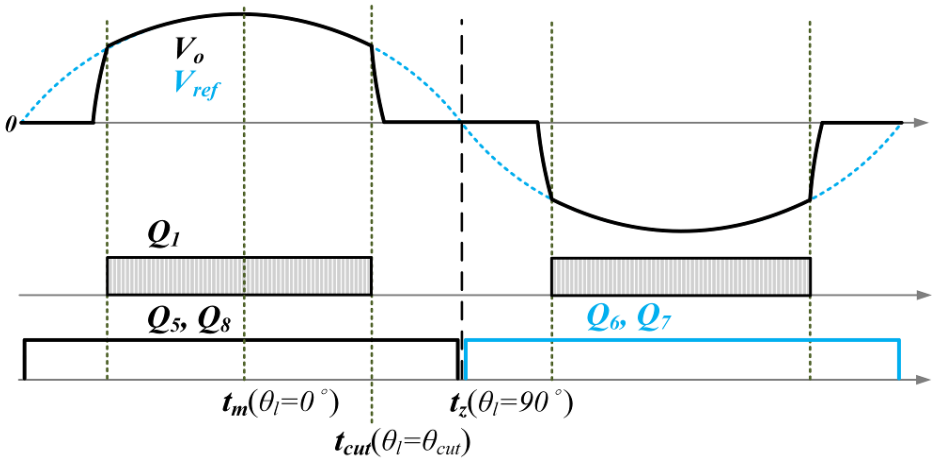


Figure 6.4. Steady-state waveforms of a VFM SRCUI module over one line-frequency cycle.

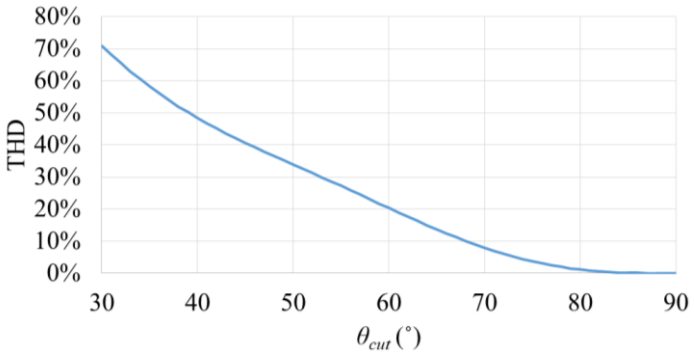


Figure 6.5. THD of V_o as a function of cutoff angle (θ_{cut}).

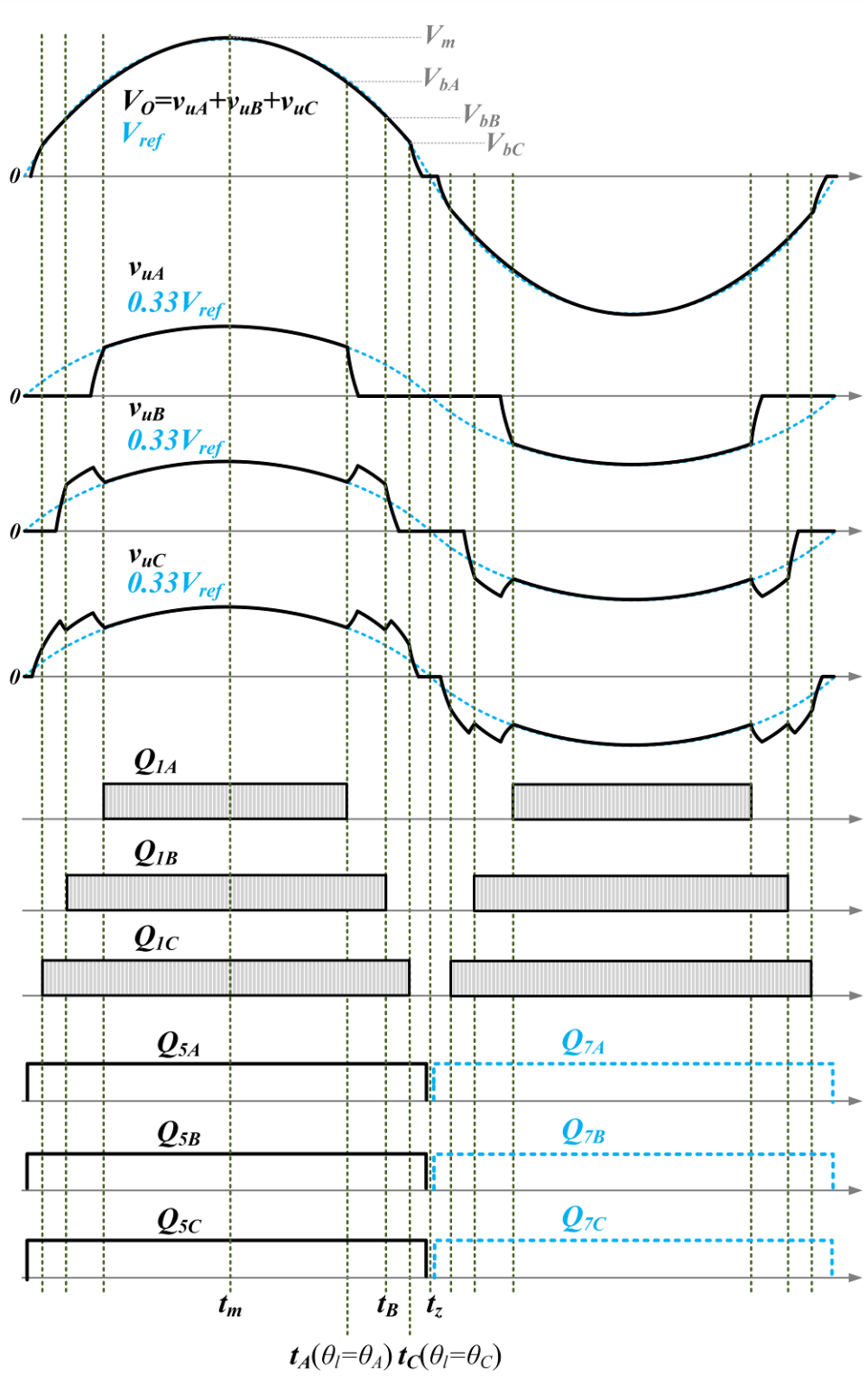


Figure 6.6. Steady-state waveforms of the MMI based on SRCUIs with SWS.

Without SWS, all modules enter/leave the VFM region at once. With SWS, each module enters/leaves the VFM region sequentially. The operational principle of SWS is illustrated in Figure 6.6. The angle θ_A is the same as θ_{cut} in Figure 6.4. But in here, only module A is turned off at θ_A so module B and module C pick up the power and output voltage left by module A. This means module B and module C individually gains more output power and output voltage, which help the ZVS of the primary-side switches. As a result, module B and module C can keep operating without violating the ZVS condition. Note that all active modules have the same f_s. In addition, all unfolders have the same gate signals and thus switch at ZCP together. Figure 6.6 also indicates that the power in modules A, B, and C is not balanced. However, the resulting thermal unbalance can always be solved by rotating the role of modules A, B, and C between different physical modules.

In Figure 6.4, V_{ref} is the reference voltage of the total output voltage. From t_m and t_A, each module follows $V_{ref}/3$. From t_A to t_B, the remaining module B and module C each follows $V_{ref}/2$. From t_B to t_C, module C alone should follow V_{ref}. Therefore, the output waveforms of each module are in-phase but different. A sinusoidal output waveform is achieved only when v_{uA}, v_{uB}, v_{uC} are synthesized together, and hence the operation is termed sequential waveform synthesis.

The number of active modules has an impact on the voltage gain curve, and it determines the effective load resistance seen by an individual module. From t_m to t_A, the effective load resistance is $R_o/3$. From t_A to t_B, the effective load resistance is $R_o/2$, and so on. Consequently, the output voltage of the MMI with N_m active modules can be estimated by (6.1), which is modified from (2.3). The definition of Q_e remains the same as (2.2) and (2.4). Furthermore, θ_A, θ_B, and θ_C, the angles where a module activates/deactivates, can be estimated by (6.2) – (6.4).

$$V_o(f_s, N_m) = \frac{N_m V_{in}}{n} \frac{1}{\sqrt{1+(N_m Q_e)^2 (\frac{f_s}{f_r} - \frac{f_r}{f_s})^2}} \tag{6.1}$$

$$\theta_A = \cos^{-1}\left(\left(\sqrt{1+(3Q_e)^2 (\frac{f_{\max}}{f_r} - \frac{f_r}{f_{\max}})^2} \right)^{-1} \right) \tag{6.2}$$

$$\theta_B = \cos^{-1}\left(\left(\frac{2}{3} \sqrt{1+(2Q_e)^2 (\frac{f_{\max}}{f_r} - \frac{f_r}{f_{\max}})^2} \right)^{-1} \right) \tag{6.3}$$

$$\theta_C = \cos^{-1}\left(\left(\frac{1}{3} \sqrt{1+Q_e^2 (\frac{f_{\max}}{f_r} - \frac{f_r}{f_{\max}})^2} \right)^{-1} \right) \tag{6.4}$$

Table 6.1. Prototype circuit parameters of the MMI based on SRCUIs.

Parameters	Value	Parameters	Value
V_{in}	80 V	L_r	12.7 μH
V_{out}	230 V_{rms}	C_r	200 nF
P_{out}	540 – 1080 W	L_m	56 μH
n	0.667	f_r	99.8 kHz
C_{fX}	1.6 μF	f_s	100 – 300 kHz

To demonstrate the operation of SWS, the circuit parameters summarized in Table 6.1 are used in this chapter. Through (6.1), the f_s of the MMI is plotted as a function of θ_l in Figure 6.7. Most of the time, f_s increases with θ_l just like under normal VFM. But once f_s hits f_{max}, one module is turned off and that moment is one of θ_A, θ_B, and θ_C. After a module is turned off, the remaining active modules decrease f_s to catch up on the reference voltage. With the 50% load, θ_A, θ_B, and θ_C are 63˚, 67˚ and 76˚ respectively. With the 100% load, θ_B and θ_C merge at 79˚ for being too close to each other, and θ_A is 75˚. This implies that SWS is more effective with a light load. Based on

Figure 6.5, the theoretic THD of V_o with the 50% load can drop from 16% to 3%, since the cutoff angle increases from 63˚ to 76˚. As to the 100% load, the theoretic THD only drops from 3.7% to 1.5%.

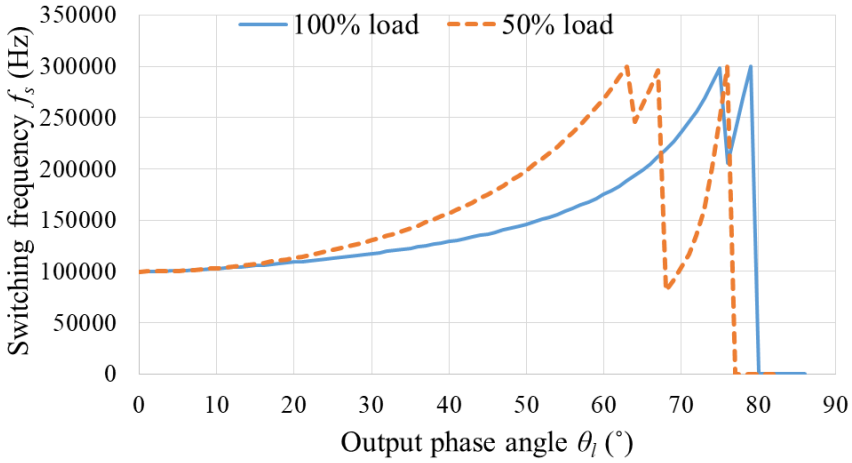


Figure 6.7. Switching frequency (f_s) as a function of output phase angle (θ_l) under SWS.

6.3 Control Strategy

The control strategy of SWS is plotted in Figure 6.8. Similar to HMM, V_o and I_o are sensed while the latter one is used to determine the load condition. The acquired load condition can be used to calculate θ_A, θ_B, and θ_C, following (6.2) – (6.4). The calculation of the angles is performed with a slow bandwidth, so it is marked in purple in Figure 6.8. The rest of the steps are in black and executed every switching-frequency cycle. Since the basis of the control is VFM, it also suffers from the changing plant model of SRC. Therefore, the gain varying method proposed in Chapter 5 is applied to correct the compensator gain over θ_l. Furthermore, the second compensator gain correction is performed after the number of active modules (N_m) are determined by θ_A, θ_B, θ_C, and θ_l. The second correction is set to compensate for the variance in dc loop gain caused by N_m. With a fixed change in f_s, the change in V_o of the MMI is N_m times of the change in a single module, because the modules are connected in series at the output. Consequently, the compensator gain has

to be higher when there are fewer active modules. With both corrections included, the formula of the compensator of SWS can be written in (6.5), where N_{tot} is the total number of modules. After the compensator is determined, f_s can be calculated, updated, and utilized to generate PWM signals.

Aside from the flow chart in Figure 6.8, the concept of SWS is also plotted in a form of a control block diagram, as shown in Figure 6.9. Note that in this chapter, standalone applications are still the targeted application, so the controller has to maintain V_o. Therefore, the design of compensator coefficients still follows the principles introduced in Chapter 5.

$$T_{fv} = k_p\left(1+\frac{k_{i0}}{s}\right)=\left(k_{p0}\left(\frac{f_s}{f_{\min}}\right)^2\frac{N_{tot}}{N_m}\right)\left(1+\frac{k_{i0}}{s}\right) \tag{6.5}$$

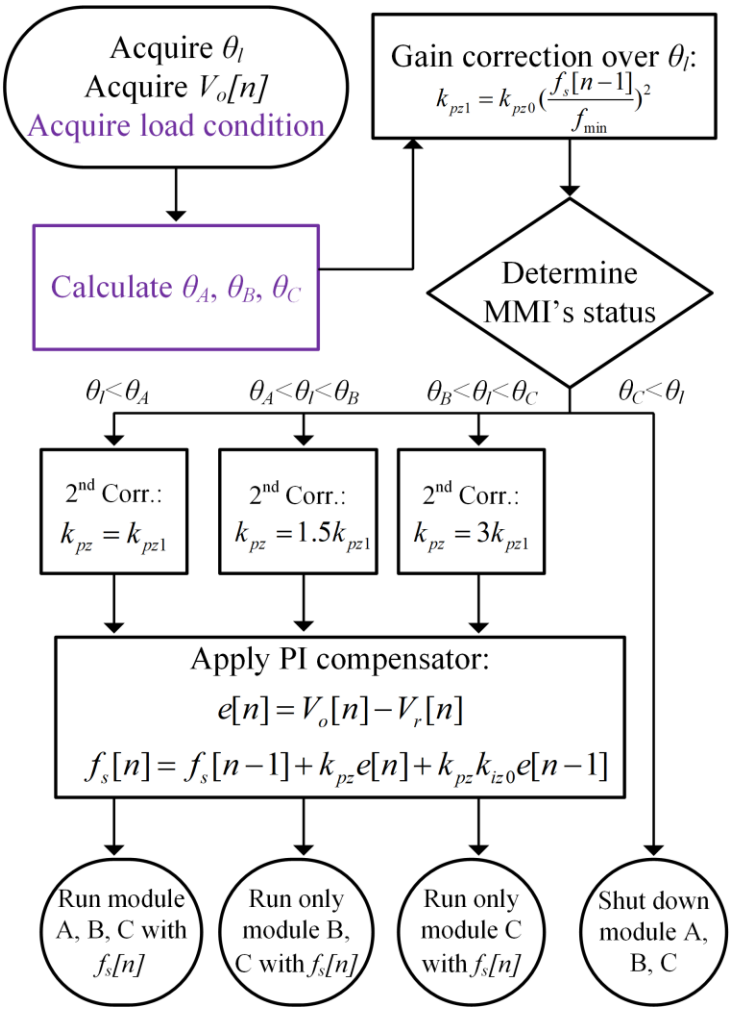


Figure 6.8. Control strategy of the MMI with SWS.

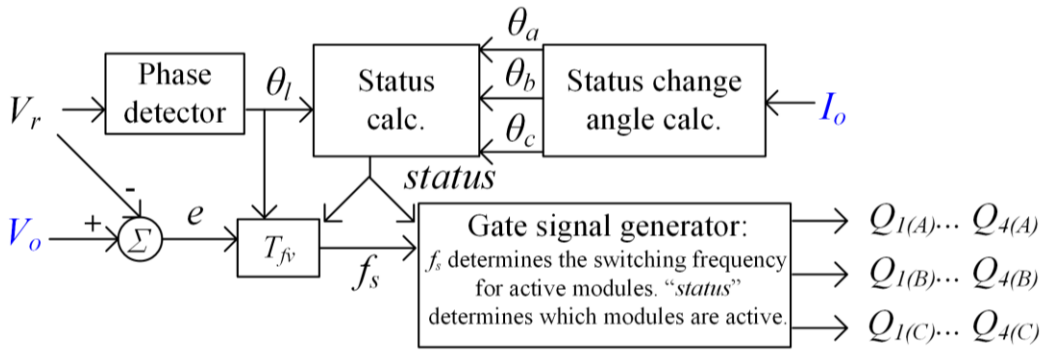


Figure 6.9. Control block diagram of SWS for standalone applications.

6.4 Experimental Results

To verify the concept of SWS, a prototype is built with the circuit parameters in Table 6.1 and the components in Table 6.2. The photo of the prototype is shown in Figure 6.10. The controller is also implemented with a DSP F28379D. The ADC sampling frequency is still 200 kHz.

With SWS, the output voltage waveforms are shown in Figure 6.11. V_o is the total output voltage that equals $v_{uA} + v_{uB} + v_{uC}$. The THD of V_o decreases with output power and is 3.6%, 4.5%, and 5.5% in Figure 6.11(a), (b), and (c). If SWS was not applied, all waveforms would have the same cutoff angle as module A. Therefore, the THD of v_{uA} can represent the THD of V_o without SWS, and it is 8.7%, 12.8%, and 20.1% in Figure 6.11(a), (b), and (c). By comparing the THD with and without SWS, it is clear that SWS is able to extend the VFM region in an MMI based on SRCUIs. Additionally, the steady-state waveforms of I_{Lr} and V_{Cr} are shown in Figure 6.12 based on module C with the 50% load. Similar to regular VFM, I_{Lr} and V_{Cr} have the highest stress at the crest and trough of the output.

Table 6.2. Key components of the MMI prototype.

Components	**Part numbers/ Design details**
Primary-side switches ($Q_{1X} - Q_{4X}$)	Si MOSFET FDP150N10A-F102
Rectifier ($D_{1X} - D_{4X}$)	Si diode BYW29-200-E3/45
Unfolder ($Q_{5X} - Q_{8X}$)	Si MOSFET IRF200P222
Transformer	Core: RM14, 3C95 Primary-side winding: 1050 strand #44 AWG litz wire, 6 turns Secondary-side winding: 660 strand #44 AWG litz wire, 9 turns
Resonant inductor (L_r)	Core: RM14, 3C95 Winding: 1050 strand #44 AWG litz wire, 8 turns
Resonant capacitor (C_r)	942C16P1K-F * 2
Output filtering capacitor (C_{fX})	B32922C3474M000 * 2 + B32922C3334M189 * 2
Gate driver	UCC21521

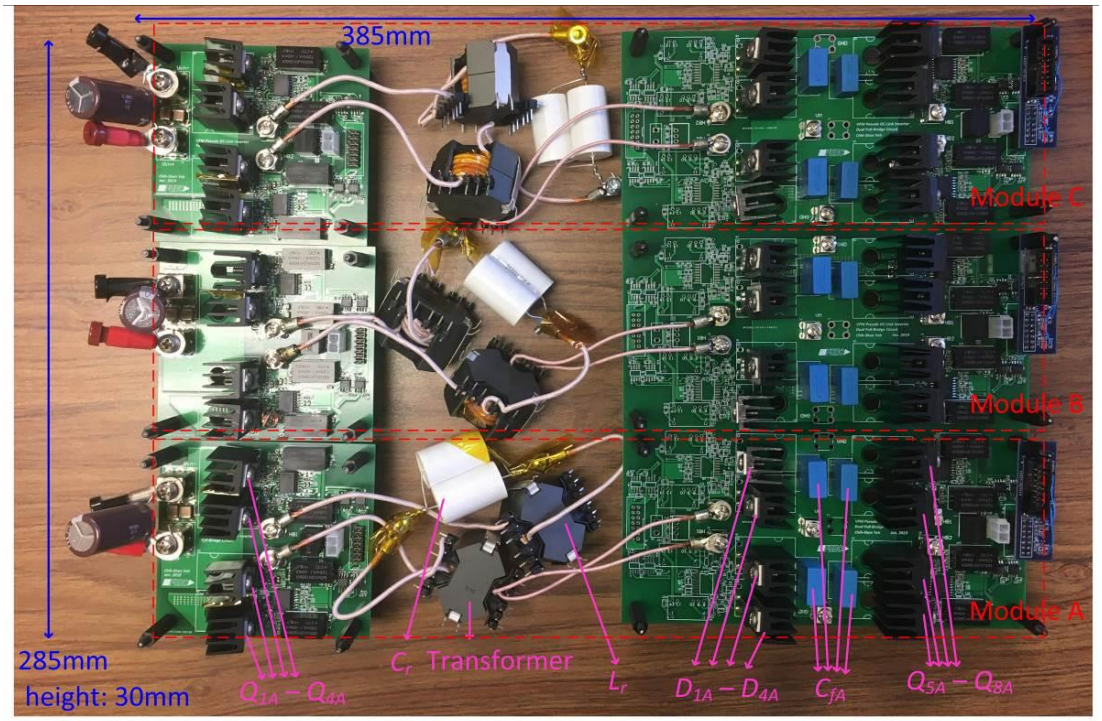
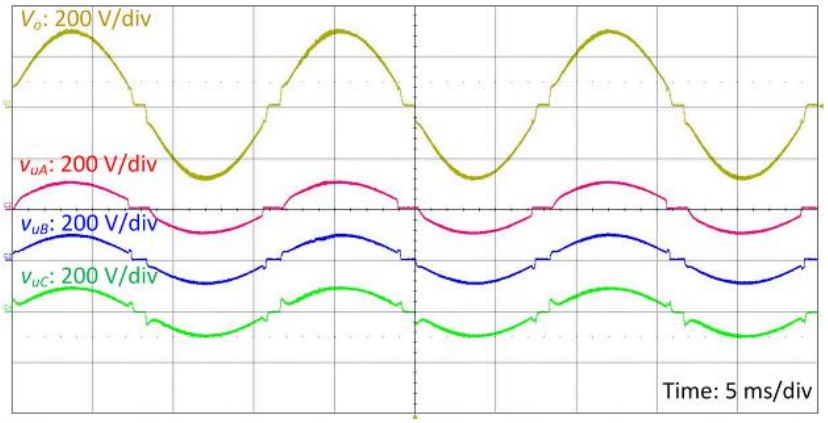
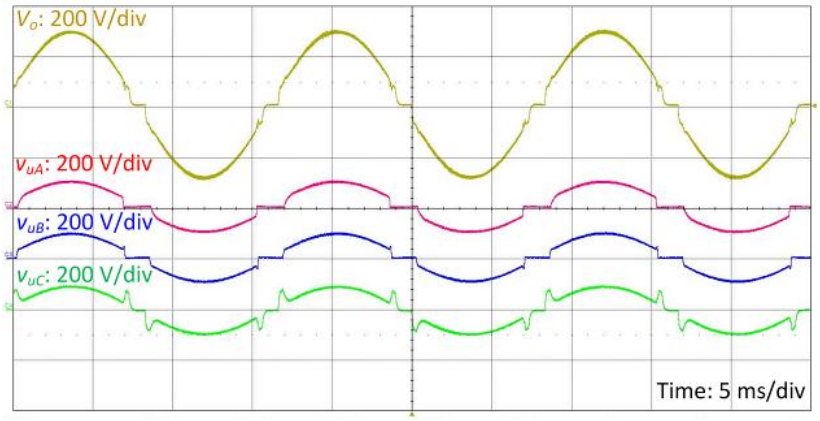


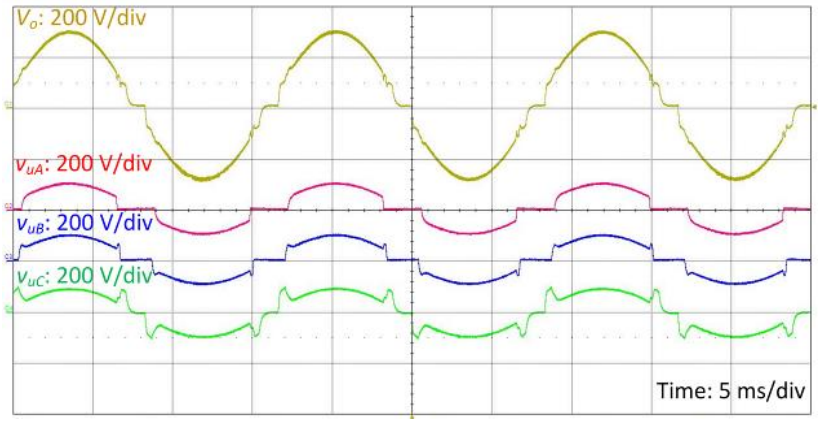
Figure 6.10. MMI prototype based on 3 SRCUIs.



(a) P_o = 1080 W (100% load).



(b) P_o = 810 W (75% load).



(c) P_o = 540 W (50% load).

Figure 6.11. Output voltage waveforms of SWS.

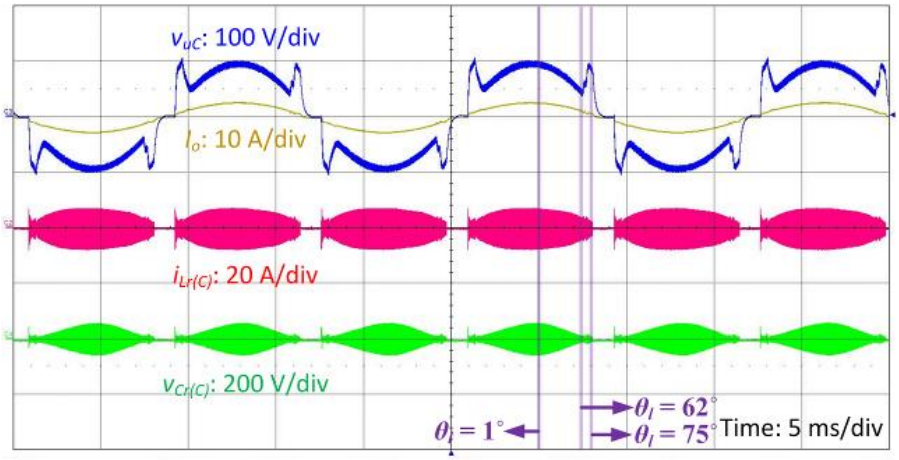
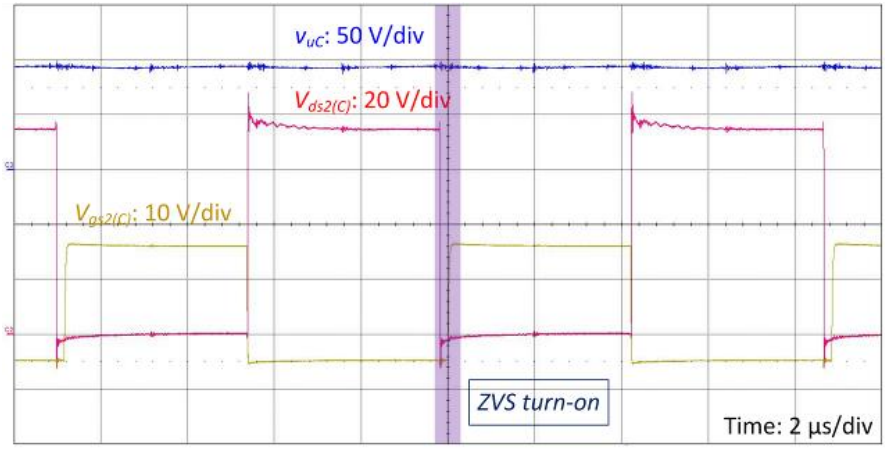
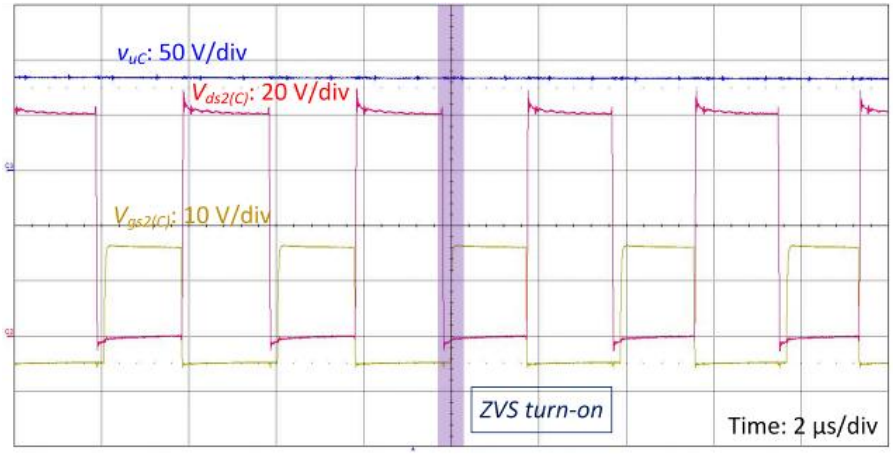


Figure 6.12. Steady-state waveforms of module C with 50% load.

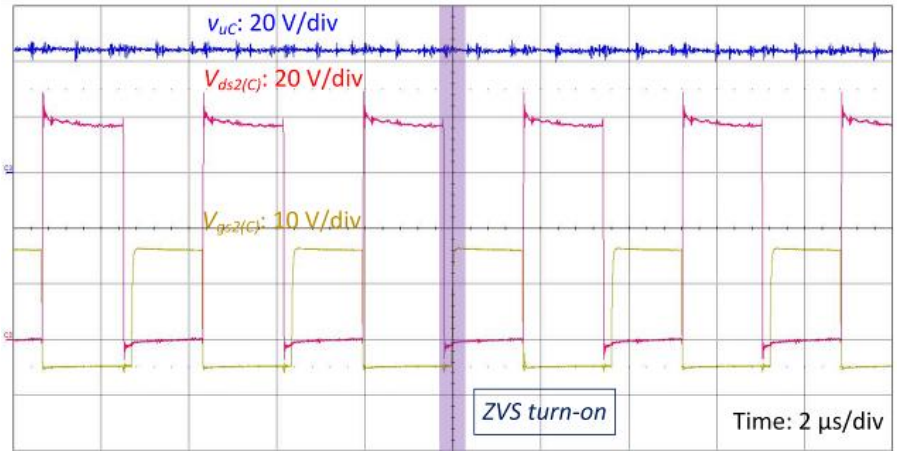
Regular VFM has trouble reaching the low-output region partly due to the limited ZVS capability. Therefore, as SWS extends the VFM region, it is also important to examine whether the primary-side switches still keep ZVS turn-on. The ZVS waveforms of module C with the 50% load are captured and shown in Figure 6.13 as an example. In Figure 6.13(a), the output voltage reaches the peak and the magnetizing current assists the ZVS of Q_{2C}. In Figure 6.13(b), $\theta_l = \theta_A = 62^\circ$ and the ZVS is achieved by the turn-off current. In Figure 6.13(c), the output voltage of the MMI is lower than that of Figure 6.13(b) since $\theta_l = \theta_C = 75^\circ$. However, v_{uC} becomes higher than in Figure 6.13(b), which ensures the ZVS of the primary-side switches.



(a) $\theta_l = 1^\circ$, $f_s = 112$ kHz.



(b) $\theta_l = 62^\circ$, $f_s = 281$ kHz.



(c) $\theta_l = 75^\circ$, $f_s = 280$ kHz.

Figure 6.13. ZVS waveforms of module C with 50% load.

In addition, the prototype is tested under other load conditions to verify the functionality of the MMI with SWS. To emulate the common grid inductance seen by inverters, an inductor of 4.7 mH (0.037 pu) is connected between the load resistor and the output of the MMI. The tested steady-state waveforms are shown in Figure 6.14 along with zoomed-in waveforms at ZCP. The THD of V_o drops from 3.6% to 4.6%, but the function of the MMI remains.

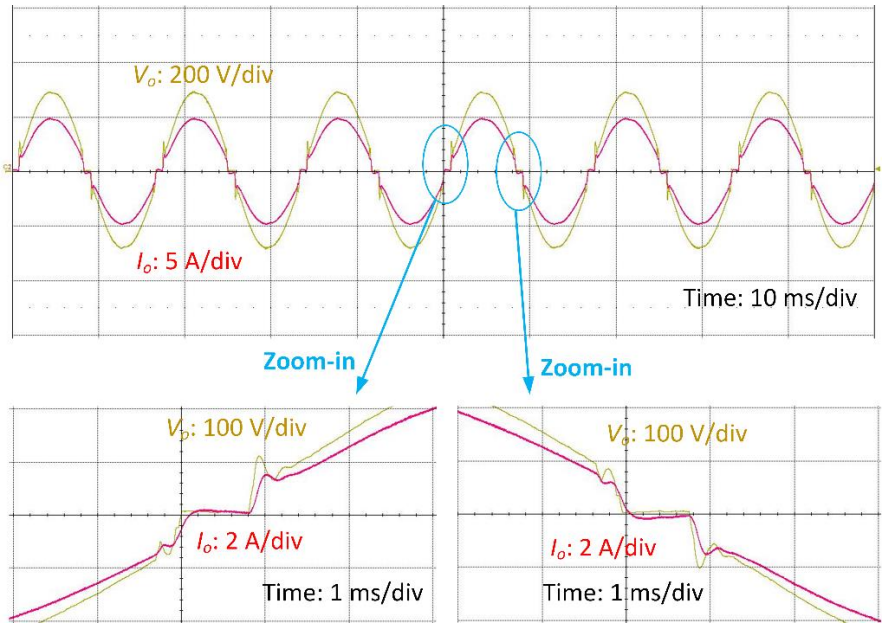
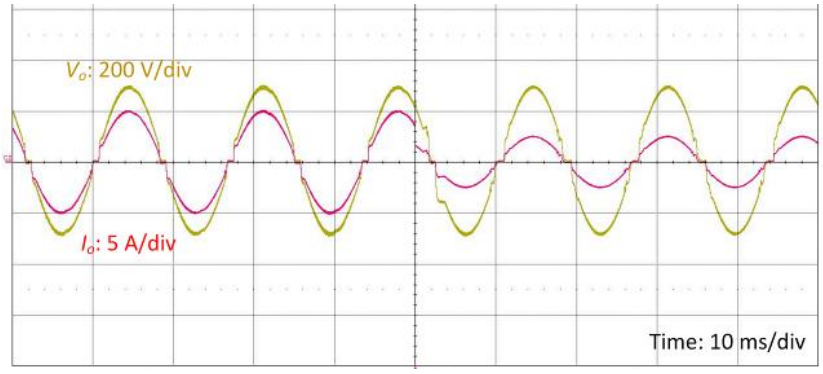
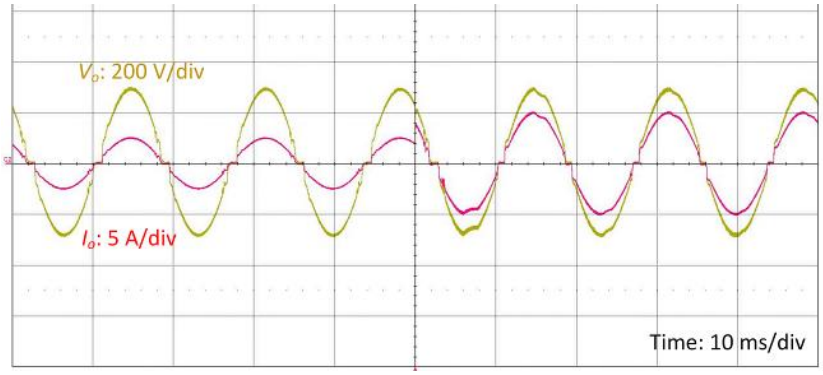


Figure 6.14. Steady-state waveforms of the MMI with R-L load (R_o = 49 Ω).



(a) From 100% to 50% load.



(b) From 50% to 100% load.

Figure 6.15. Dynamic load test of the MMI with SWS.

The load-transient test is also performed and the results are shown in Figure 6.15. The controller successfully maintains the output voltage despite the change in load condition. Similar to Chapter 5, the loop gain bandwidth is only a few hundred Hz in the high-output region. Therefore, it may take a few cycles until the output voltage is fully back to normal from a transient.

6.5 Summary

Under regular VFM, SRCUI has to turn off in the low-output region due to the limitations of the SRC's voltage gain and ZVS capability. In an output-stacked MMI based on SRCUIs, the issue can be alleviated by turning on and off modules sequentially. Once a module is turned off, the f_s of the remaining active modules decreases to follow the reference voltage. Moreover, the output power of each active module increases. With decreased f_s and increased modular power, the active modules can operate with ZVS in an extended range.

In an MMI operating with only VFM, SWS can directly improve the output waveform quality. Therefore, it is beneficial for applications that use only the full-load waveform as the output quality standard (i.e., TDD), since VFM alone may be sufficient. This means the inverter can completely get rid of turn-on loss and the relevant electromagnetic interference [102]-[103]. Moreover, the modularity of SRCUI makes it possible for high-power applications, where an MMI may be composed of more than 3 modules. In this case, SWS can be even more effective. With the same circuit parameters, the predicted THD is shown in Figure 6.16 over a different number of modules. With 6 SRCUI modules, the theoretic THD is lower than 1% even with the 10% load.

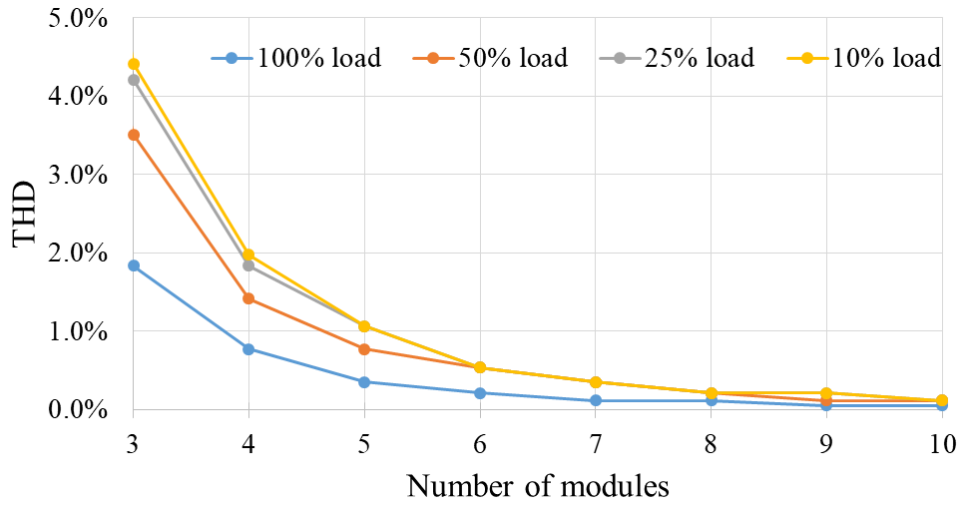


Figure 6.16. Predicted THD of V_o with a different number of modules.

In the other applications, the output waveform quality may also be important for a light load and thus the inverter operates under HMM. In this case, the effect of SWS is to extend the VFM region and shorten the SPDM region. This is preferred from the perspective of efficiency, as discussed in Section 4.4.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

In this dissertation, the basic modulation methods for SRCUI were examined and each of them showed at least a critical drawback – incomplete modulation range, limited soft-switching (especially ZVS) function, and/or excessive current stresses. Therefore, HMM was proposed in Chapter 3 and it is free from those critical drawbacks. To prove that HMM is better than the basic modulation methods in terms of power efficiency, three design metrics were introduced – the rms value of the resonant current, the maximum magnetic flux of the transformer, and the turn-off current. By these design metrics, the performance of the modulation methods can be compared without involvement in hardware design details. The comparison results showed that HMM has the best performance regarding the design metrics, which holds important implications for over half of types of power losses. In other words, HMM is more beneficial to power efficiency than the previous modulation methods.

Furthermore, an analytic power loss model was built in Chapter 4 along with an SRCUI prototype. Through the efficiency analysis, a general conclusion was established and stated that a longer VFM region is preferred over the SPDM region for the sake of efficiency and output waveform quality. The power loss model also indicates that the most concerning turn-on loss has been well eliminated or suppressed by (i) the ZVS of Q_1 – Q_4 in the VFM region, (ii) the ZVS of Q_2, Q_3 in the SPDM region, (iii) the ZCS of Q_1, Q_4 in SPDM region and (iv) the equivalently low switching frequency in SPDM region.

The control of SRCUI is not straightforward because the plant model of SRC changes dramatically. In Chapter 5, a third-order small-signal equivalent circuit model introduced in [91] was adopted to identify the change in the plant model's dc gain and polo locations. Later, a gain-varying method was proposed to compensate for the dc gain variance caused by different operating points. By using the gain-varying method, the digital PI controller is able to improve output waveform quality and maintain the output voltage in standalone applications. Finally, SWS was proposed in Chapter 6 and it works for the MMI based on SRCUIs. With VFM alone, SWS helps improve output waveform quality. With HMM, SWS helps extend the VFM region.

By the proposed modulation and control methods, SRCUI can operate with high efficiency, low switching losses, and low output waveform distortion. Therefore, the research objectives set in Chapter 1 are met.

7.2 Future Work

Nevertheless, the research on HMM and other proposed methods does not stop here. There are several directions to proceed with the development.

(i) The most important implication for full-range soft-switching is the potential for high-switching-frequency, high-power-density applications. In Chapter 4, we have suggested that SRCUI may even be more advantageous if high-frequency GaN devices are adopted. However, the high-frequency magnetic design has not been covered in this dissertation. In the field of high-frequency electromagnetics, skin effect, proximity effect, and fringing effect kick in [104], making the power loss model established here inapplicable. Therefore, the estimation of the non-ideal electromagnetic effects has to be studied with the aid of finite-element-analysis software. The wide switching-frequency spectrum of HMM has to be considered as well.

(ii) The control of the inverter has to be further improved for higher bandwidth. For instance, many studies regarding uninterrupted power supply inverter have a bandwidth of around 1 kHz [105]-[106], which is not entirely achieved in Chapter 5. To do so, the controller will have to compensate the poles of the SRC rather than simply avoid them. In addition, the controller design for grid-tied applications is also intriguing, although it requires another deep research into SRC's plant model. Since the adopted plant model is based on a resistive load.

(iii) The study of EMI filter for HMM SRCUI is also an important future work for practical applications. The EMI filter will have to handle a wide spectrum of frequencies caused by both the varying switching frequency in the VFM region and the varying equivalent switching frequency in the SPDM region.

(iv) Finally, some well-known methods may further improve the efficiency of the prototype. These methods include but are not limited to synchronous rectification and the integration of the transformer and the resonant inductor.

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