Topology Investigation and System Optimization of Resonant Converters

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Dianbo Fu

(Abstract)

Over the past several years, energy efficiency and power density have become the top concerns for power conversion. Rising energy intensity leads to a higher cost of delivering power. Meanwhile, the demand for compact power supplies grows significantly. It requires power supplies with high efficiency, low profile and high power density.

Dc-dc power conversion has been widely applied for industry, medial, military and airspace applications. Conventional PWM dc-dc converters have relatively low power transfer efficiency and low power density. In contrast, resonant dc-dc converters have numerous advantages for dc-dc power conversions. In this work, topologies and system optimization of resonant converters are investigated to meet challenges of high efficiency, high power density, low EMI, easy startup and over current protection.

LLC resonant converters can achieve zero-voltage-switching (ZVS) for primary side devices and zero-current-switching (ZCS) for the secondary side rectifiers. The switching loss is minimized. LLC is very attractive to overcome the issues of conventional circuits. However, challenges still remain.

First of all, for low-voltage high-current applications, the synchronous rectifier (SR) with lower conduction loss is a must for high efficiency. To solve the driving issues of SRs, a novel synchronous driving scheme is proposed. Experimental results demonstrate the considerable loss reduction with utilization of the proposed driving scheme.

Secondly, dc-dc converters are required to meet EMI standard. This work proposes an EMI mode. Based on the proposed model, EMI analysis and noise attenuation techniques are proposed and verified by experiments.

Thirdly, startup and over-load protection are another issues of LLC resonant converters. With proposed multi-element resonant converters, the current limit issues can be resolved. In addition, the proposed multi-element resonant converters can utilize higher-order harmonics to enhance power transfer.

Fourthly, for high-current applications, the secondary side structure becomes very critical. An improved secondary side construction is proposed to alleviate ac termination losses and SR paralleling issues. Novel winding structures are proposed to reduce the winding loss. The magnetic integration technique is proposed and analyzed, and an optimal integrated transformer design is proposed, which has low loss and compact size.

To my family:

My parents: Zhiyang Fu and Huizu Zhang

My wife: Pei Xiao

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Chapter 1

Introduction

1.1 Background and Introduction

Over the past several years energy efficiency and power density have become the top concerns for power conversions. Rising energy intensity leads to a higher cost for delivering power. Meanwhile, the demand for compact power supplies grows significantly. It requires power supplies with high efficiency, low profile and high power density.

With the development of information technology, computing system applications, such as telecom, server and computers, consumer electronics, such as flat-panel TVs and lighting systems, such as LED lamps, have become a large market for the power supply industry. Recent statistic data show that the demands for these systems are continuously increasing [A.1]. Moreover, because of the improving of integrated circuit technology, which follows Moore's Law, computing systems and consumer electronics are continually increasing their density and functionality. The increasing functionality requires more power consumption and higher density requires less size on the power supplies. Therefore, the power supplies for the computing, consumer electronics and lighting applications are required to provide more power with small size and low cost [A.1]-[A.15].

Fig. 1.1. Typical examples of front-end converters adopted by information technology applications.

Ac-dc front-end converters are needed for most off-line applications. Front-end converters are widely adopted by computing and consumer electronics applications, such as telecom, servers, desktop PCs, laptops, gaming systems, and flat panel TVs, etc. An example of a typical front-end converter is shown in Fig. 1.1.

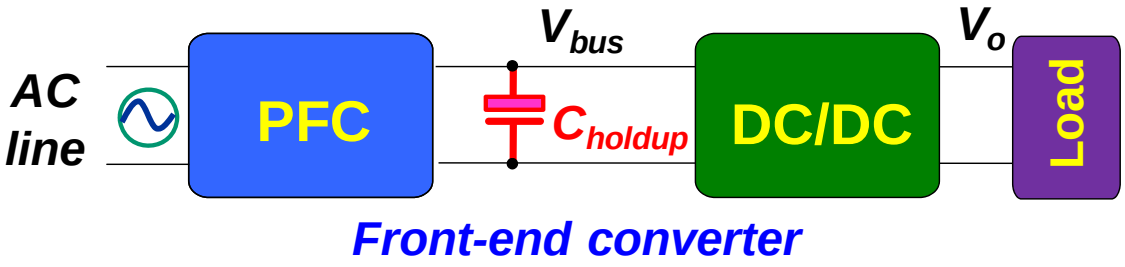


Fig. 1.2. The typical structure of front-end converters for off-line applications.

Front-end converters are normally implemented by the two-stage approach, which includes a power factor correction (PFC) stage followed by a dc-dc stage. The typical structure of front-end ac-dc converters is shown in Fig. 1.2.

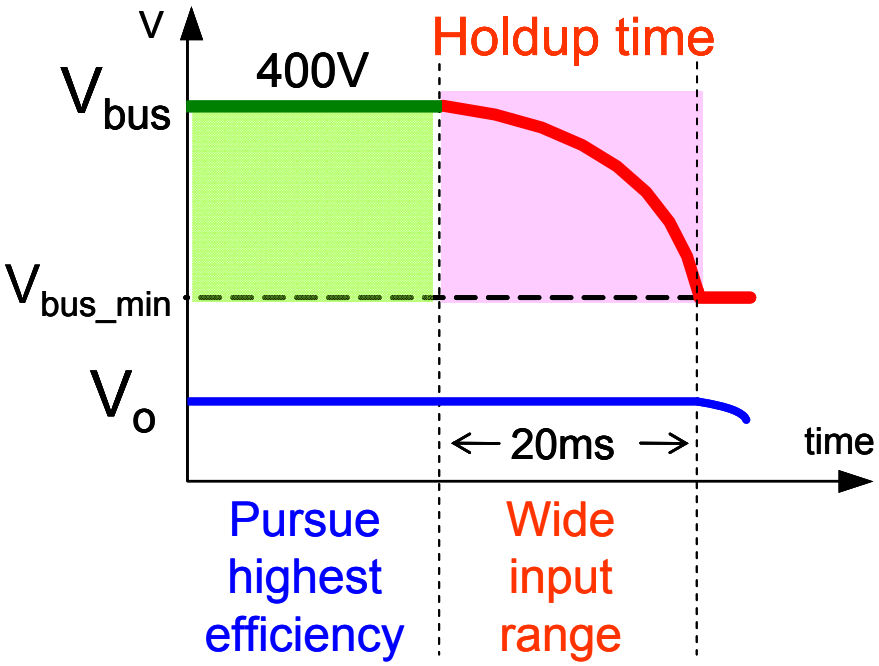


Fig. 1.3. Holdup time operation scenario for front-end converters.

According to the specifications of computing systems, such as servers [A.9], front-end ac-dc converters are required to maintain regulated output voltage for about 20ms

when the input ac line is lost. The holdup time operation requirement is illustrated in Fig. 1.3.

During holdup time, all the energy transferred to the load comes from the holdup time capacitor. Therefore, large holdup time capacitors are required to provide the energy during holdup time. The holdup time capacitor requirement is determined by the system power level and the input voltage range of dc-dc converter. Apparently, the wider dc-dc stage input voltage range, the more energy stored in the holdup time capacitor can be used during holdup time. Thus, fewer holdup time capacitors can be used.

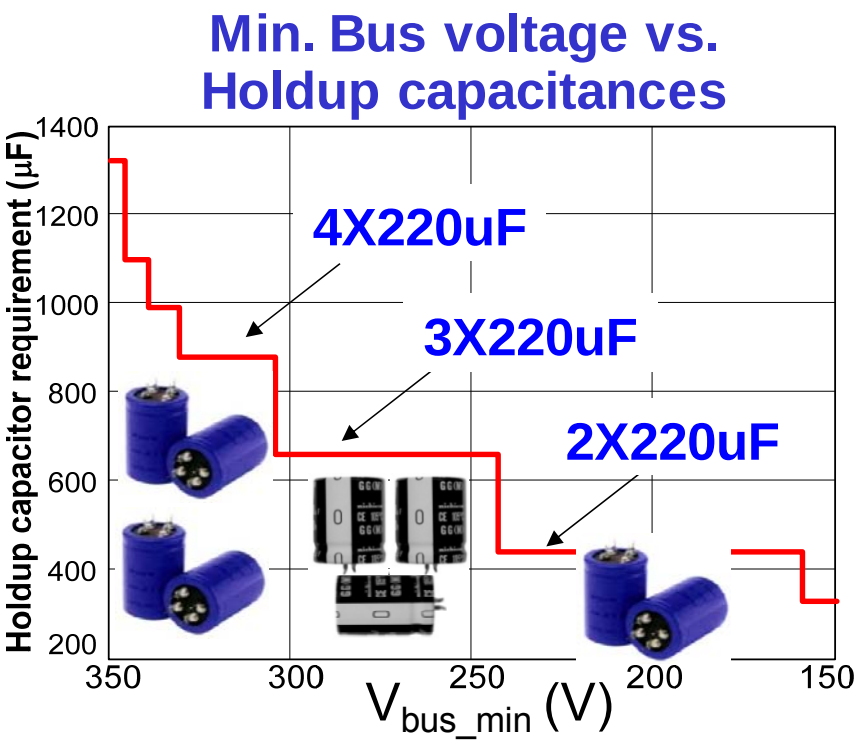


Fig. 1.4. Holdup time capacitance vs. input voltage range for dc-dc converters of the front-end converter.

The relationship between holdup time capacitor requirement and minimum dc-dc stage input voltage for 1kW front-end converter is shown in Fig. 1.5. Obviously, a wide operation range in the dc-dc stage is required to reduce the holdup time capacitance. Therefore, the size and cost of the bulky capacitors are reduced. Due to the holdup time operation requirement, the capability to operate with a wide input voltage range is required for the dc-dc stage in front-end converters.

For the dc-dc stage of front-end converters, high efficiency is desirable at the nominal input voltage. Meanwhile, wide input voltage range of the dc-dc stage is required to deal with the holdup time operation. This is the general characteristic for the dc-dc stage of front-end converters with holdup time requirements [A.14] and [A.15].

High efficiency and high power density are becoming more and more desired for ac-dc front-end converters. Driven strongly by economic and environmental concerns, a high efficiency over a wide load range is required by various organizations and programs, such as the U.S. Energy Star [A.10], 80 Plus [A.11], Climate Savers [A.12], and German Blue Angel [A.13], whose logos are shown in Fig. 1.5.

Fig. 1.5. Worldwide energy saving organizations and programs [A.10-A.13].

The 80 PLUS program provides a basic efficiency requirement for front-end converters, as shown in Fig. 1.6. It requires the efficiency to be higher than the specified value at 20%, 50%, and 100% load. Other than the 80 PLUS requirement, Climate Savers is targeting at higher efficiency. It even target to achieve 4% or 3% efficiency improvement every year until 2010. By June, 2010, participants are expected to achieve 88% efficiency at 20% and 100% load, and 92% efficiency at 50% load. The coming trend will target even higher efficiency, 92%, 94%, 92% at 20%, 50% and 100% loads, respectively, as shown in Fig. 1.6. It is going to be or is being required in very near future. Determining how to meet such a stringent requirement is very challenging for power conversion technologies.

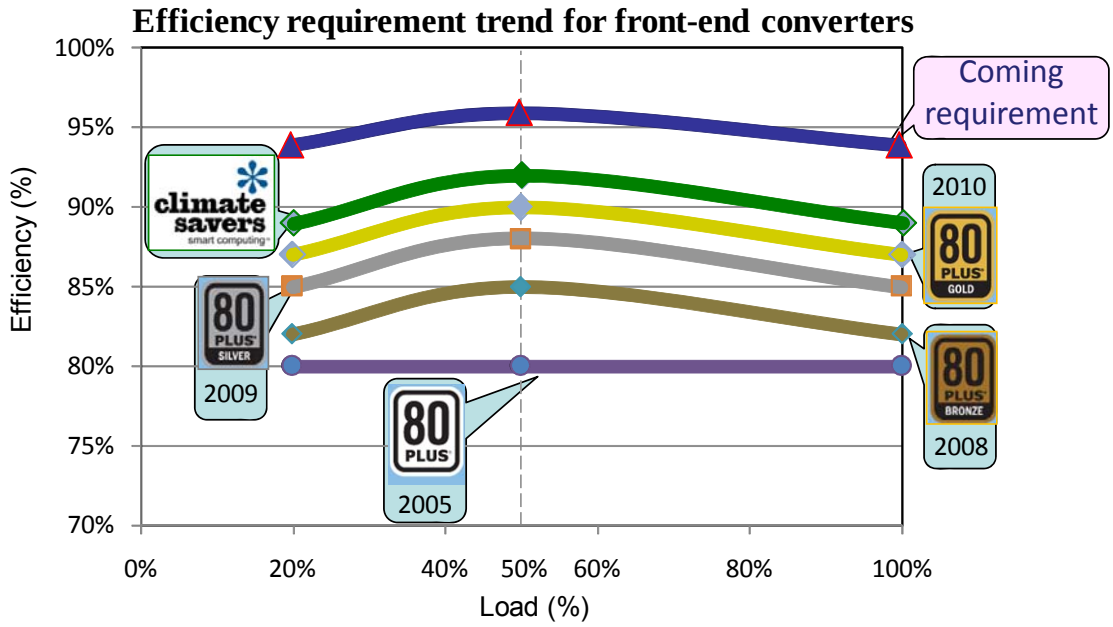


Fig. 1.6. Efficiency requirement trend for front-end converters [A.11-A.12].

Front-end ac-dc converters are under the pressure of continuous increasing power density requirements. As shown in Fig. 1.7, the power density of the front-end converter for computing systems is continuously increasing [A.1]. Higher power density can eventually reduce the converter cost and allows for accommodating more equipment in the existing infrastructures. Due to the rapidly evolving IC technologies, the ac-dc front-end converters have relatively short life spans as products in the market. The typical power density of front-end power supplies for servers was in the $5W/in^3$ range about ten years ago [A.1]. The power density of these power supplies today is in the $25W/in^3$ range. As this trend continuous, the power density is expected to be pushed up even over $30W/inch^3$ in the near future in order to meet industrial needs. This continuously increasing power density target pose challenges for today's ac-dc front-end converter technology.

To meet the increasing stringent requirement of high efficiency and high power density, improvement of dc-dc conversion technology over wide input voltage range is a must. Therefore, this dissertation mainly focuses on the investigation of novel techniques to improve the overall performance of front-end dc-dc converters with wide input voltage range operation.

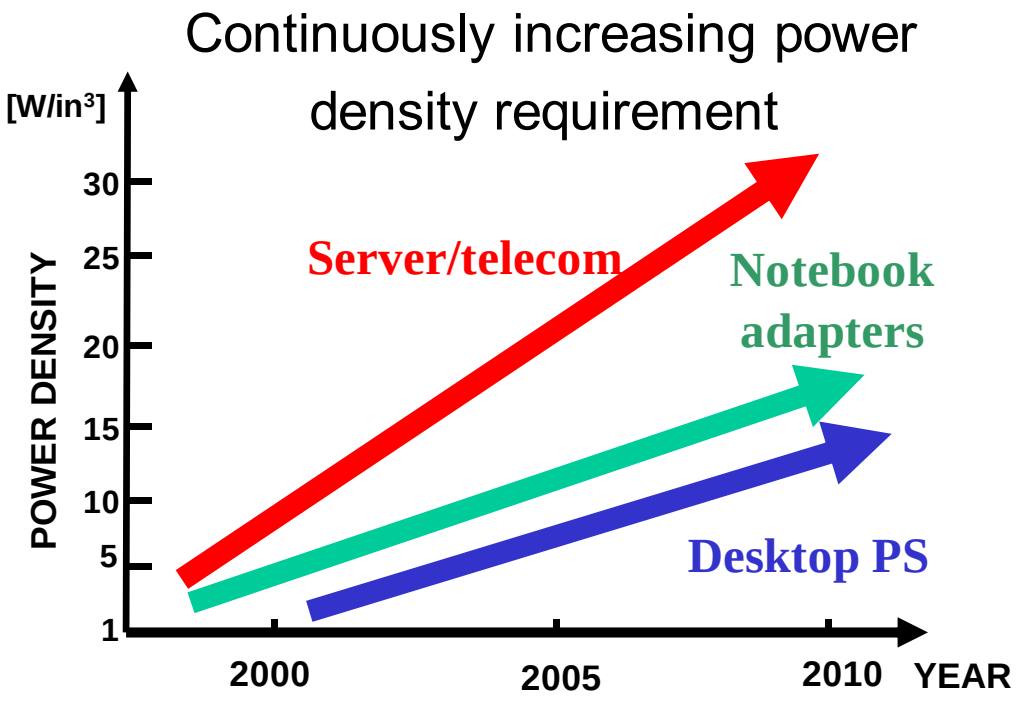


Fig. 1.7. Continuously increasing power density requirement [A.1].

1.2 Challenges of DC-DC Power Conversions with Holdup Time Requirement

1.2.1 Challenges of Conventional PWM DC-DC Converters with Holdup Time Requirement

A growing demand for saving energy and reducing the size of power systems have stimulated substantial research and development efforts towards high-efficiency and high-power-density power supplies. Stringent efficiency requirements for future servers and computing applications are shown in Fig. 1.6. On the other hand, the power density is expected to increase continuously. Figuring out how to meet these requirements is really a big challenge.

The most effective way to achieve high power density in converters is to increase the switching frequency so that the size of the passive components, such as the capacitor and inductor, as well as the size of the transformer can be reduced.

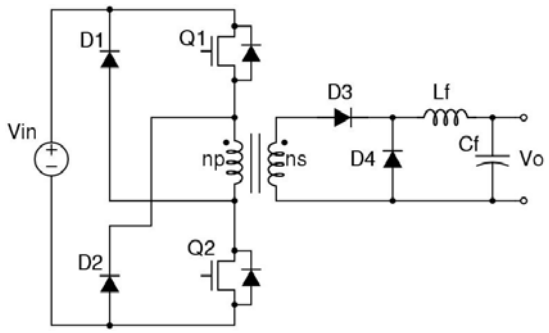


Fig. 1.8. Two-switch forward converters.

PWM converters are widely applied for dc-dc power conversions [B.1]-[B.31].

Hard-switching PWM converters, such as two-switch forward converters, are used for this application. The schematic of two-switch forward converters is shown in Fig. 1.8 [B.1]-[B.3]. Two-switch forward converters received a lot of interest and appreciations because of robustness. For half-bridge and full-bridge converters, the primary switches are connected in a totem pole structure. Whenever the two switches are turned on at the same time due to electromagnetic noise or radiation, it will be a destructive failure. For two-switch forward converters, this problem is solved, which is very critical for airspace power supplies, which are exposed to high-energy radiation. The major disadvantages of two-switch forward converters are hard switching and the large filter inductor. Hard switching leads to high switching loss for high frequency operation. In addition, the voltage-second on the output inductor is much higher in two-switch-

forward converters than in half-bridge and full-bridge converters. Because of these penalties, two-switch forward converters are not very desirable for meeting higher efficiency and high-power-density requirements in the future.

Soft-switching PWM circuits, such as the phase-shift full-bridge PWM converter and the asymmetrical half-bridge PWM converter, are widely used for front-end dc-dc conversion. These topologies are plotted in Fig. 1.9 and Fig. 1.12, respectively. Soft-switching PWM converters can achieve zero-voltage-switching (ZVS). Therefore, lower switching loss and higher frequency can be accomplished compared with hard-switching converters.

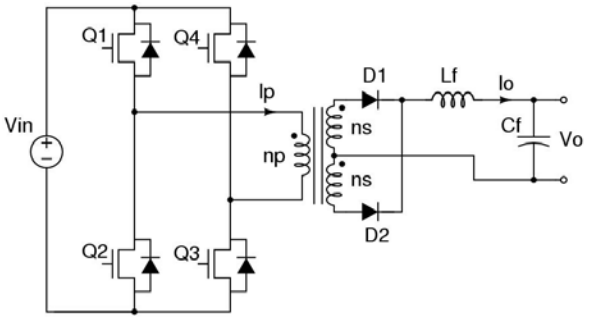


Fig. 1.9. The phase-shift full-bridge PWM converter.

However, bulky capacitors are used to provide energy during the holdup time. The bulky holdup time capacitor becomes the bottleneck to increasing power density because the size of the capacitor is determined by the energy required during the holdup time and the conducting rms current. Enlarging the operation range of the dc-dc stage could reduce the holdup time capacitors. In this way, more energy stored in the capacitor could be utilized. However, conventional PWM converters have to sacrifice

normal operation efficiency to extend their operation range. It is difficult to design a wide-operation-range PWM converter with high efficiency. Normally, the duty cycle is designed to be as high as possible to handle the holdup time operation. Thus, at normal conditions, the duty cycle is much smaller. The primary side to secondary side transformer turns ratio is small, which leads to high primary side current. Both conduction loss and switching loss increase. Consequently, efficiency suffers at normal operation conditions.

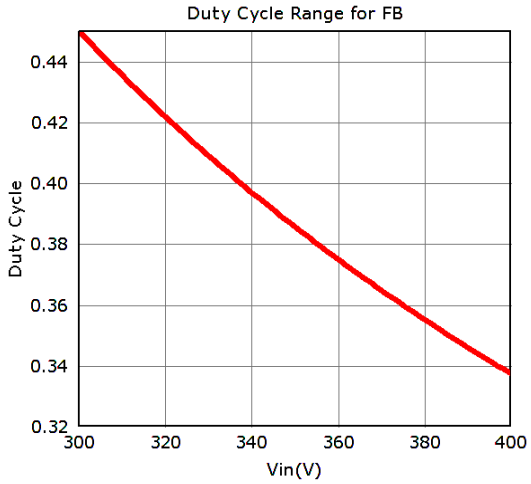


Fig. 1.10. Duty cycle range for full bridge converter with hold up requirement.

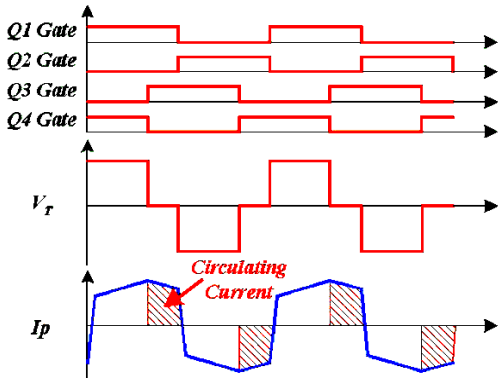


Fig. 1.11. Circulating current of full-bridge converter at normal conditions.

For phase-shift full-bridge converters (PSFB), the major problems are the high circulating current during normal operation, hard switching on the secondary side and light load efficiency. As seen in Fig. 1.11, during each switching cycle, there are freewheeling periods. High current circulates in the converter. To satisfy the holdup requirement, the duty cycle is relatively small at 400V. Thus, it leads to relatively high circulating current and a large amount of conduction loss. In addition, due to duty cycle loss problem [B.8], the effective duty cycle is even smaller. More conduction loss deteriorates the efficiency. On the other hand, although soft switching is achieved at the primary side, hard switching problems still remain for the secondary side devices. Switching loss and voltage stress of secondary side devices are severe issues. At light-load conditions, ZVS may be lost. Thus, the efficiency under light loads is another concern.

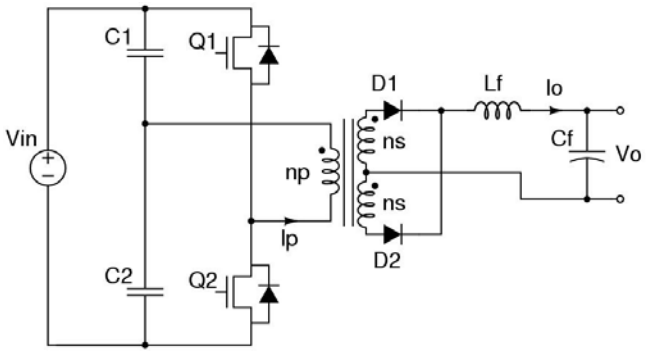


Fig. 1.12. The asymmetrical half-bridge PWM converter.

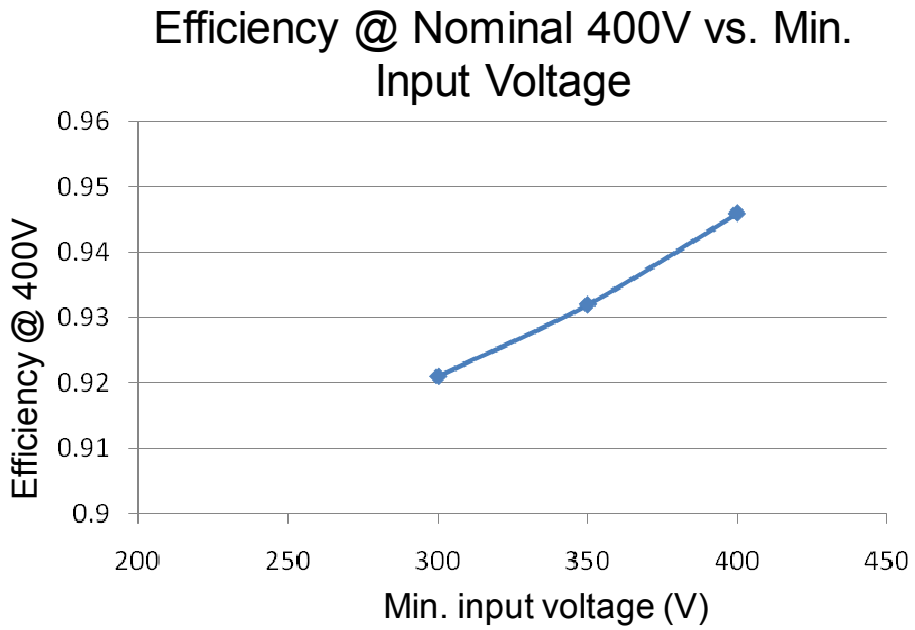


Fig. 1.13. The efficiency curves of different input voltage operation range for asymmetrical half bridge PWM converter.

The asymmetrical half-bridge converter (AHB) is desired to operate with 50% duty cycle and achieve maximum efficiency. However, to ensure a wide operation range, during normal operation the duty cycle has to be reduced to realize regulation capabilities. Thus, circuit normal operation condition has to be compromised to achieve wide operation range. As demonstrated in Fig. 1.13, a 1 kW, 48V output asymmetrical half-bridge converter is able to achieve 94.5% optimal efficiency at 200 kHz switching frequency when it is dedicatedly designed for 400V input and operates with 50% duty cycle. However, to achieve an operation range from 300V to 400V, the duty cycle at 400V input has to be reduced to 30%, which dramatically reduces the converter efficiency. As demonstrated in Fig. 1.13, the converter efficiency reduces to 92% when the wide input voltage operation range is realized. Due to the low switching frequency,

the power density of AHB is not very high. The prototype of 1kW, 400V/48V, 200kHz, asymmetrical half-bridge converter can only achieve 13W/in^3 power density [A.14] and [A.15]. In sum, neither the efficiency nor the power density can be satisfied with the conventional soft switching PWM techniques.

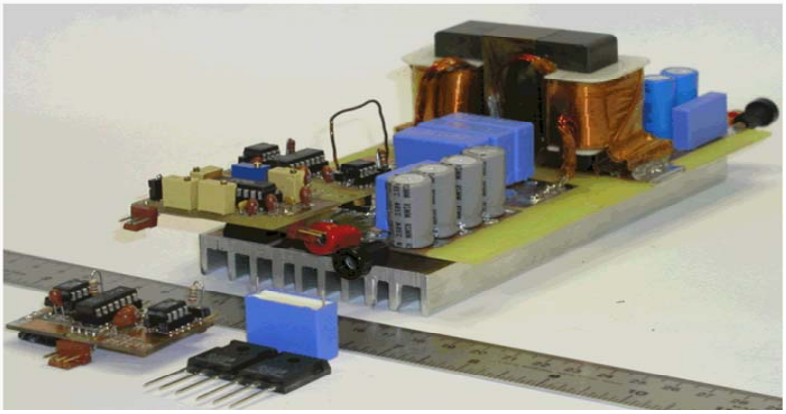


Fig. 1.14. The 1kW, 400V/48V, 200kHz, asymmetrical half-bridge PWM converter with 13W/in^3 power density.

1.2.2 Improvement and Limitations of Alternative Strategies for Conventional PWM DC-DC Converters with Holdup Time Requirement

To alleviate holdup time issues, several alternative strategies have been proposed. This section explores the most important of these strategies.

i. Range winding for wide input range

In [B.19], a range winding approach is proposed to deal with the holdup time operation problem. The concept of a range winding solution is to change the transformer turns ratio according to different input voltages, so that the transformer can be optimized for high input voltage.

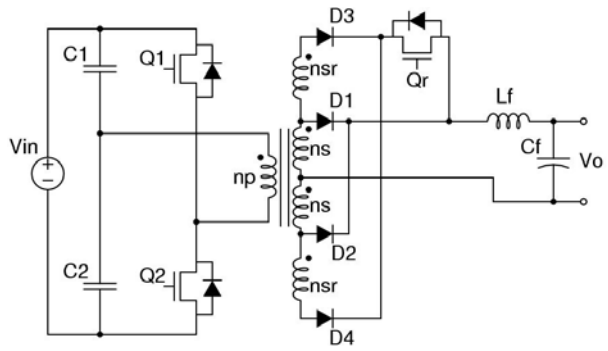


Fig. 1.15. Asymmetrical half-bridge converter with range winding for duty cycle extension [B.19].

Range-windings (nsr) and range-switches (D3, D4 and Qr) circuits are illustrated in Fig. 1.15. Conceptually, the range-winding strategy provides a variable turns ratio of the transformer. At nominal conditions, range switches and range windings are not conducting. During the holdup time operation, range switches are turned on. Range-windings deliver power to the load. Thus, the primary-side-to-secondary-side turns ratio of the transformer becomes smaller than the nominal condition. The voltage gain is boosted with the extra range windings.

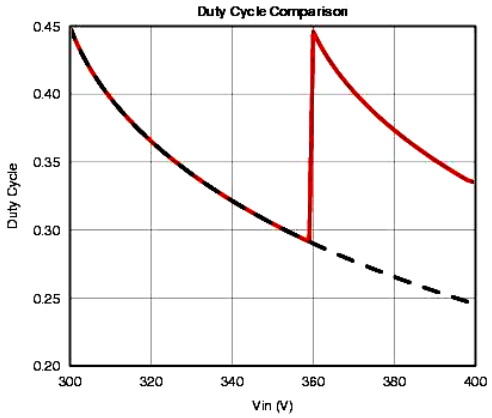


Fig. 1.16. Duty cycle range comparison of asymmetrical half-bridge converter with/without range switch.

An example is shown in Fig. 1.16 to illustrate the improvement. For the traditional AHB, the duty cycle at 400V is less than 0.25. With range windings, the duty cycle is extended to 0.34. As a result, both loss and stress are reduced quite a lot, and the performance can be improved. The efficiency results are given in Fig. 1.17. The range winding approach improves the efficiency at normal operation conditions.

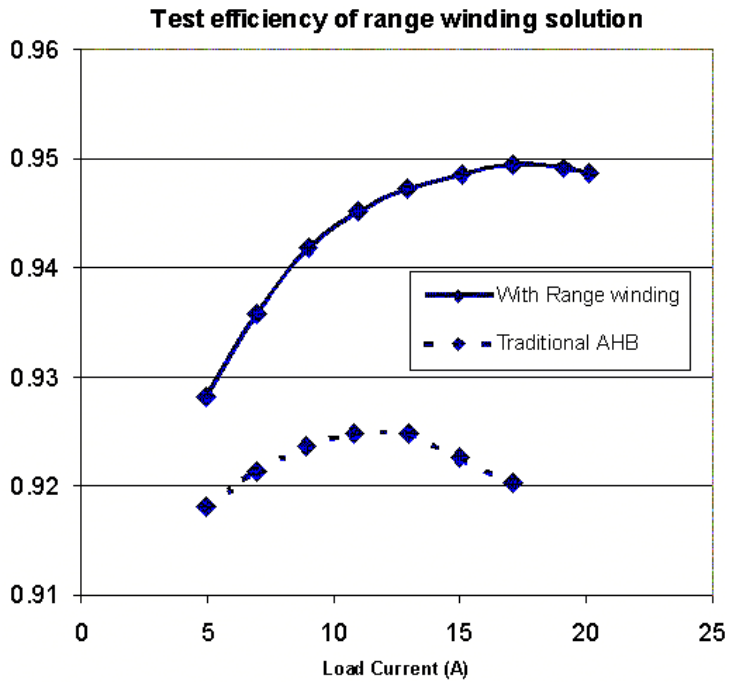


Fig. 1.17 Test efficiency at normal operation for range winding solution.

However, there are some disadvantages of the range-windings approach. First of all, although the duty cycle can be somewhat extended, the duty cycle is still small at the normal condition. Thus efficiency is still sacrificed. Secondly, many extra components are required, such as an input voltage-sensing circuit. The higher cost and complicated circuits are major concerns. Thirdly, the transformer structure becomes complicated. Due to the complicated circuit structure of the secondary side, it is very difficult to

achieve optimal design and circuit layout, especially for low-voltage, high-current applications. Fourthly, dynamic performance is another issue. During holdup time operation, the range switch is turned on. The range windings begin to transfer energy. When the range switch Qr is turned on, the volt-second of the output choke Lf changes abruptly. Normally, the bandwidth of the ac-dc front-end converter is not very high. Thus, there is an overshoot on the output voltage. This overshoot may increase the voltage stress of the output rectifiers and range switch. Furthermore, this voltage overshoot may be beyond the range of the required output voltage and it is difficult to suppress.

In sum, the range-windings strategy brings a lot of problems and might not be practical for this application.

ii. Holdup time extension circuit

In [B.20], a holdup time extension circuit is proposed to deal with the holdup time operation problem. The concept of the holdup time extension circuit is to employ an additional dc-dc boost type converter for the higher voltage gain required for holdup time.

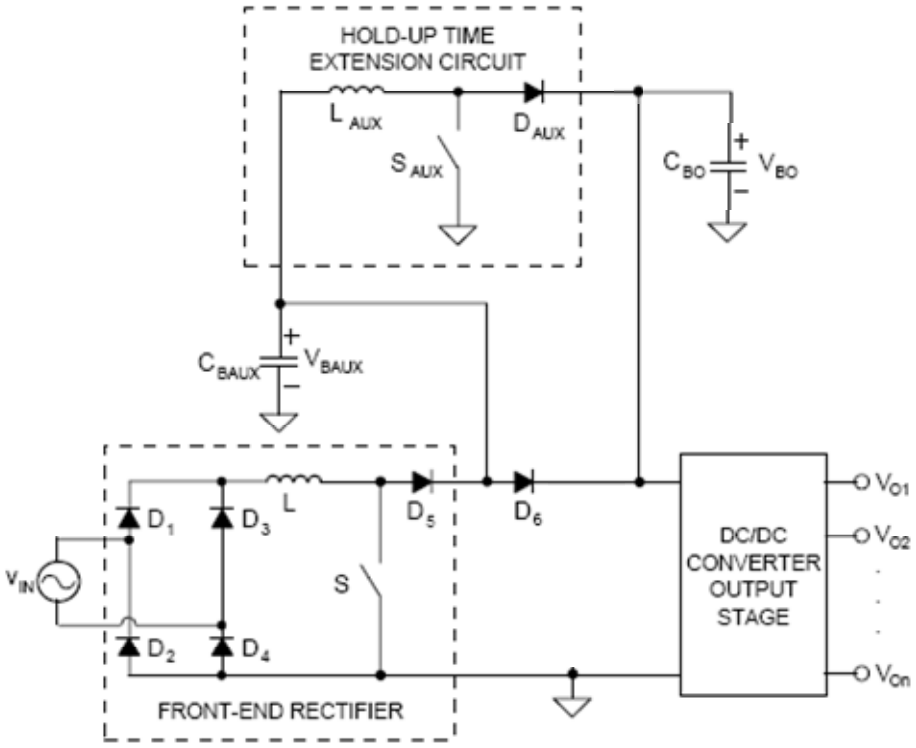


Fig. 1.18. Holdup time extension circuit to achieve narrow input voltage range of front-end dc-dc converters.

The complete circuit is depicted in Fig. 1.18. The holdup time extension circuit is connected at the input of the dc-dc converter. During normal conditions, the extension circuit remains off. When the ac line is absent and the front-end PFC circuit stops, the extension circuit is activated and helps to boost the voltage gain. To make it work, an extra diode is placed in the power delivery path. Under normal conditions, the input voltage of dc-dc converter V_{BO} almost equals the input voltage of the extension circuit V_{BAUX}. When the ac line drops, both V_{BO} and V_{BAUX} decrease. Once V_{BO} is lower than the preset threshold voltage V_{BMIN}, the extension circuit begins to work and boosts V_{BO} at V_{BMIN} during the required holdup time.

The narrow input voltage range of the main dc-dc converter is the major benefit of the holdup time extension circuit. Thus, the duty cycle of the main dc-dc stage can be relatively large, and better performance can be achieved. Meanwhile, to reduce the passive component size, the auxiliary inductor can be integrated with the main boost inductor. This simple integration approach results in a smaller size.

However, the drawbacks of this system are: (i) the extension circuit needs an extra power converter, sensing circuits and control circuits. These complicate the circuit design and increase the cost considerably. (ii) An extra diode is in series with the main power delivery. This diode induces extra loss at normal conditions.

iii. Boost-type PWM converters with holdup time extension capability

Most conventional PWM converters, such as the forward, half-bridge and full-bridge converters, are buck-type converters. When there is a requirement of holdup time operation, optimal operation cannot be achieved at nominal conditions.

To solve the holdup time issue in buck-type PWM converters, boost-type PWM converters are proposed in [B.21]. The circuit of the isolated dual active boost converter (DAB) is depicted in Fig. 1.19. The DAB can achieve ZVS and be designed optimally at nominal conditions. During holdup time, due to the boost gain function, DAB can achieve enough gain. Thus, the isolated boost converter can achieve higher efficiency than conventional buck-type PWM converters.

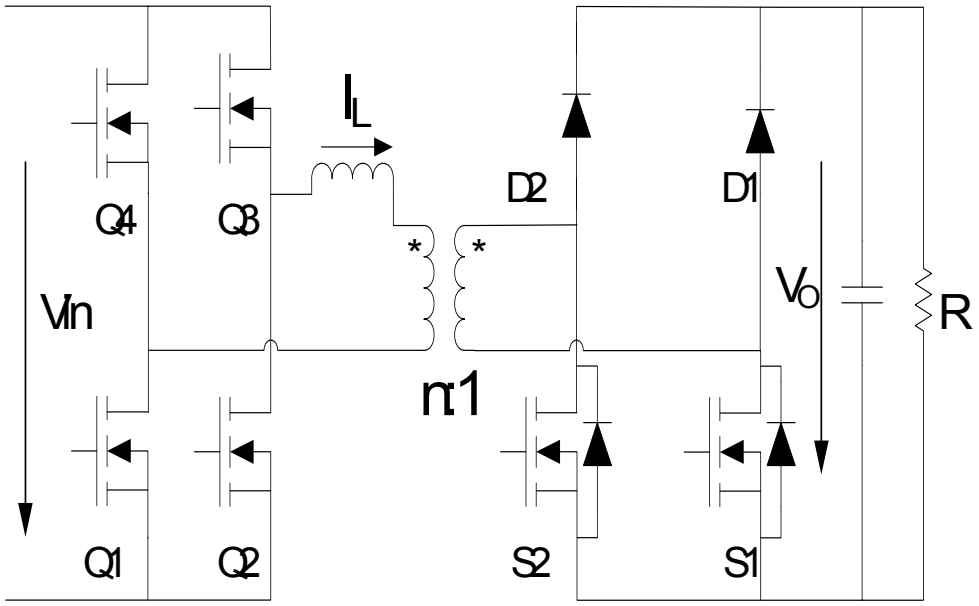


Fig. 1.19. Isolated dual-boost converter with holdup time extension capability in [B.21].

However, the drawbacks of the isolated boost converter are: (i) ZVS is lost at light load; (ii) the primary side switch turn-off current is relatively high, and hence leads to relatively high turn-off switching loss.

Thus, better approaches are still needed.

In sum, all the aforementioned solutions have limitations. New approaches should be investigated to accomplish the target of high efficiency and high power density.

1.2.3 Opportunities and Challenges of Resonant DC-DC Converters with Holdup Time Requirement

1.2.3.1 Challenges of Conventional Resonant Converters with Holdup Time Requirement

Resonant converters, which have been investigated intensively [C.1]-[C.59], can achieve very low switching loss, thus enabling resonant topologies to operate at high switching frequencies. In resonant topologies, series resonant converters (SRC), parallel resonant converters (PRC), and LCC resonant converters are the three most popular topologies.

(i) Series resonant converters

The circuit diagram of an SRC is shown in Fig. 1.20. The DC characteristic of the SRC is shown in Fig. 1.21. The operating region is on the right side of resonant frequency f_0 owing to preferred ZVS operation.

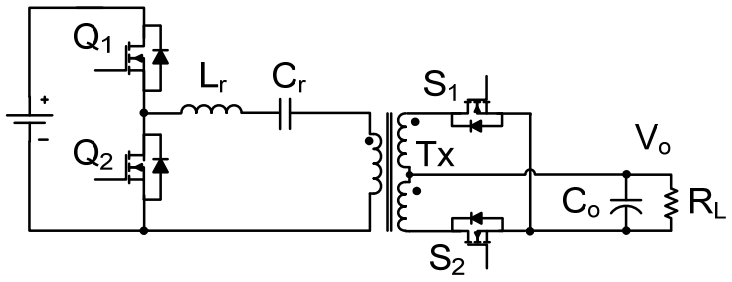


Fig. 1.20. Series resonant converters.

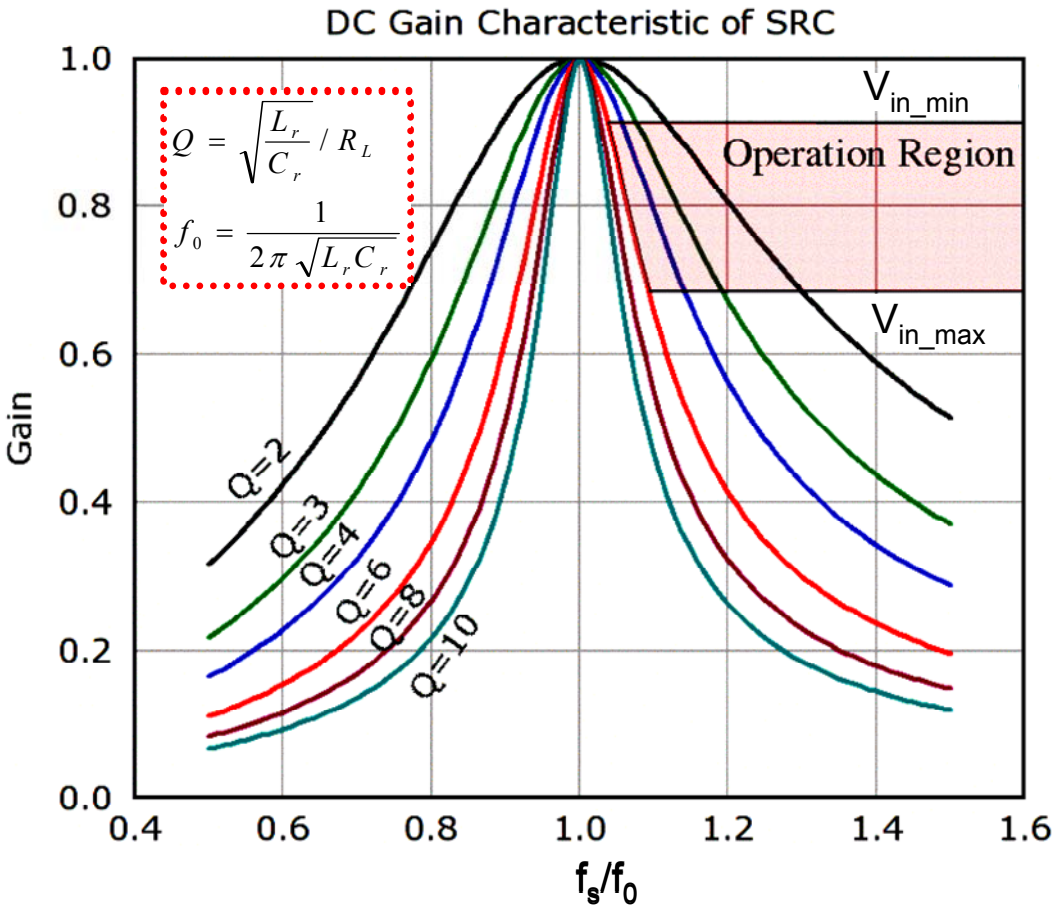


Fig. 1.21. DC characteristic and operating region of SRC.

It can be seen from the operating region that at light load, the switching frequency needs to increase to a very high value to keep the output voltage regulated. Theoretically, the SRC will lose voltage regulation capability at a no load condition. This is a problem for SRC.

At 300V input, the converter is working close to resonant frequency. As the input voltage increases, the converter is working at a higher frequency, away from the resonant frequency. This means more and more energy is circulating in the resonant tank instead of being transferred to output.

On the other hand, when converters operate far from the resonant frequency, the turn-off current increases significantly due to large phase shift between excitation voltage and current of the resonant tank. The switching loss will be high.

With the above analysis, we can see that SRC is not a good candidate for dc-dc converters with holdup time requirement. The major problems are: light-load regulation, high circulating energy and high turn-off current at nominal input voltage.

(ii) Parallel resonant converters

The schematic of a PRC is shown in Fig. 1.22. Its DC characteristic is shown in Fig. 1.23.

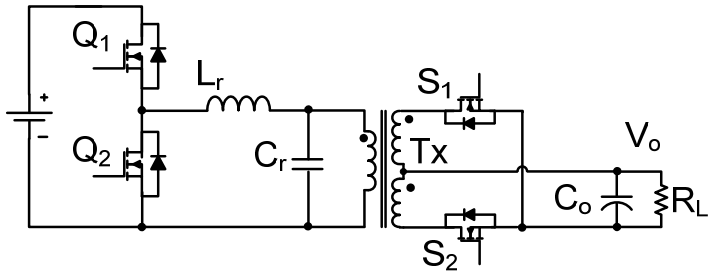


Fig. 1.22. Parallel resonant converters.

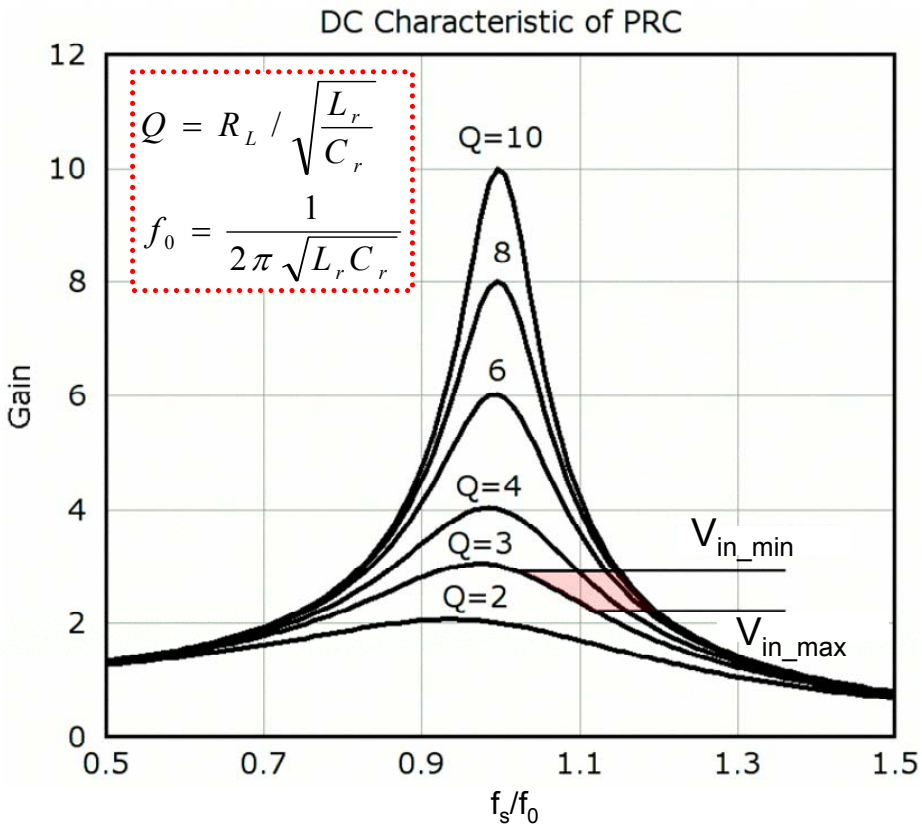


Fig. 1.23. DC characteristic and operating region of PRC.

The operating region of the PRC is shown in Fig. 1.23 as shaded area. Similar to SRC, the operating region is also designed on the right hand side of resonant frequency to achieve ZVS.

Compare with SRC, the operating region is much smaller. At light load, the frequency doesn't need to change too much to keep output voltage regulated. So light load regulation problem doesn't exist in PRC.

However, one problem for the PRC is that the circulating energy is very high, even at light load. For PRC, since the load is in parallel with the resonant capacitor, even at a

no-load condition the input still sees a pretty small impedance of the series resonant tank. This will induce pretty high circulating energy, even when the load is zero.

With the above analysis, we can see that a PRC is not a good candidate either. The major problems are: high circulating energy, high turn off current at high input voltage condition.

(iii) LCC resonant converters

The schematic of LCC resonant converters is shown in Fig. 1.24. The DC characteristic of LCC resonant converters is shown in Fig. 1.25. Its resonant tank consists of three resonant components: L_r, C_r and C_p. The LCC resonant tank can be considered as the combination of SRC and PRC. LCC resonant converters combine the merits of PRCs and SRCs. LCC resonant converter can regulate the output voltage at no-load conditions. From the graph of the operating region, it can be observed that LCC resonant converters can achieve a narrow switching frequency range with load change compared with SRC. At light-load conditions, the circulating energy is smaller than that of the PRC [C.39].

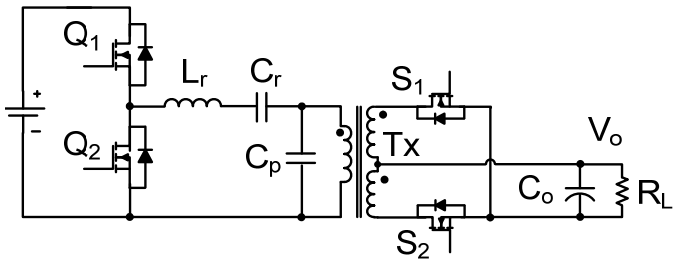


Fig. 1.24. LCC resonant converters.

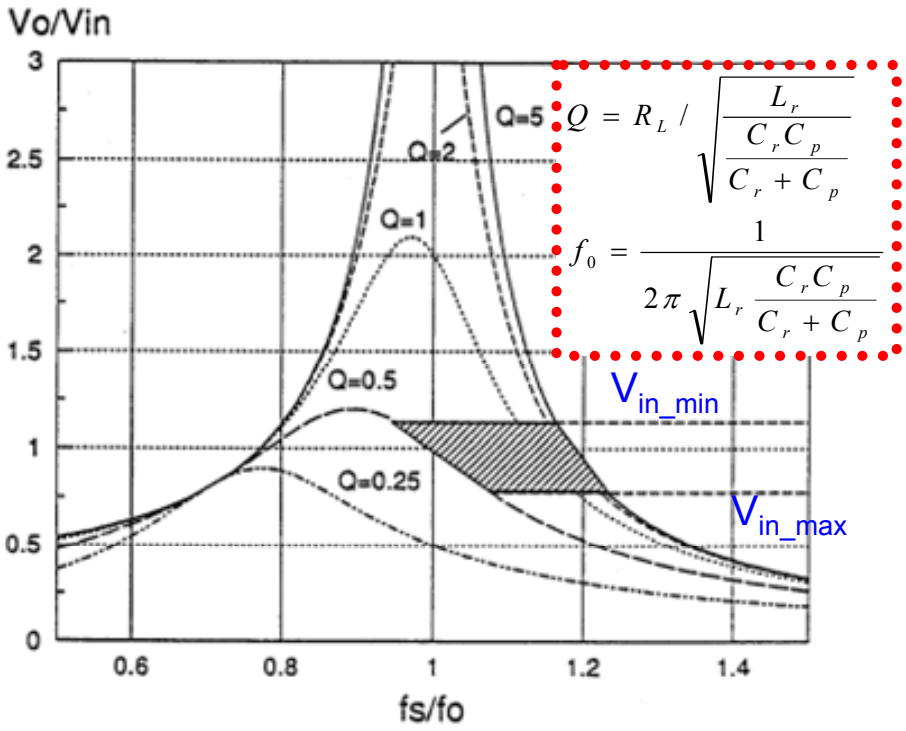


Fig. 1.25. DC characteristic and operating region of LCC.

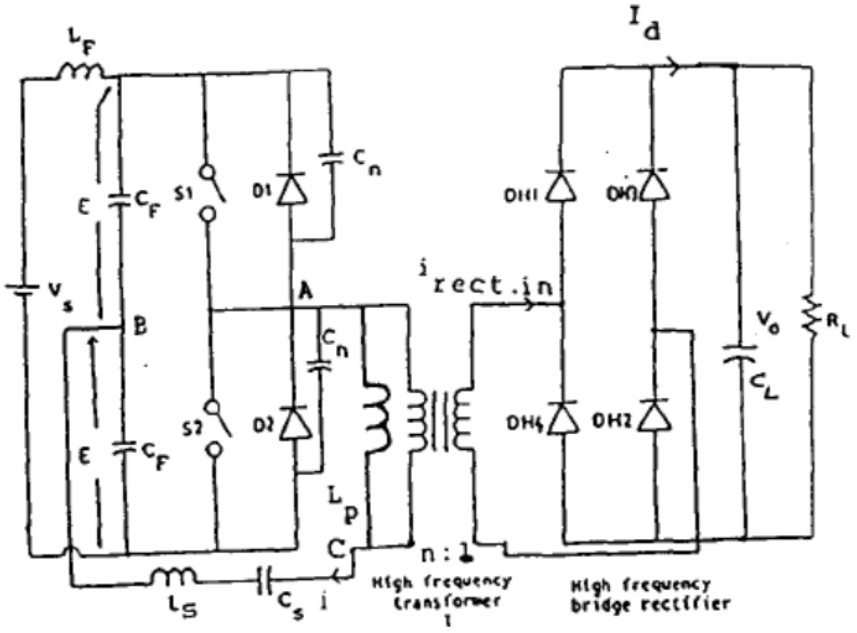
The LCC has two resonant frequencies, series resonant frequency and parallel resonant frequency. Although operating at the series resonant frequency is desirable for high efficiency, when doing so, ZVS is lost for certain load conditions. Thus, the operating region is designed to be on the right-hand side of the parallel resonant frequency to achieve ZVS at all load conditions.

Unfortunately, like the PRC and SRC, for the LCC, the circulating energy and turn-off current of the devices also increase at nominal input voltage V_{in_max}.

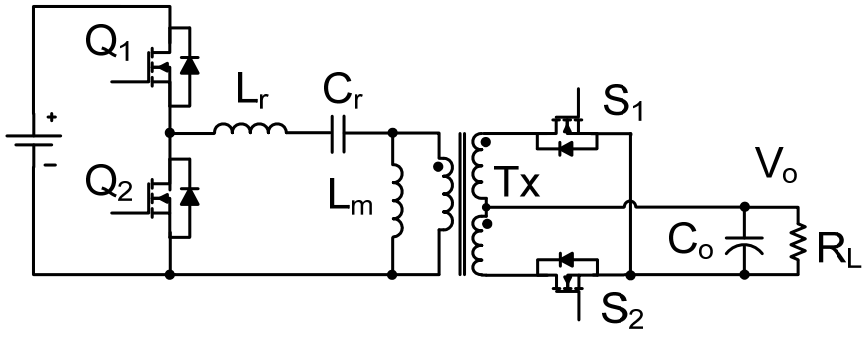
In sum, to deal with a wide input voltage range, all these traditional resonant converters encounter some problems. To achieve higher efficiency, other resonant topologies should be considered.

1.2.3.2 Opportunities and Challenges of LLC Resonant Converters with Holdup Time Requirements

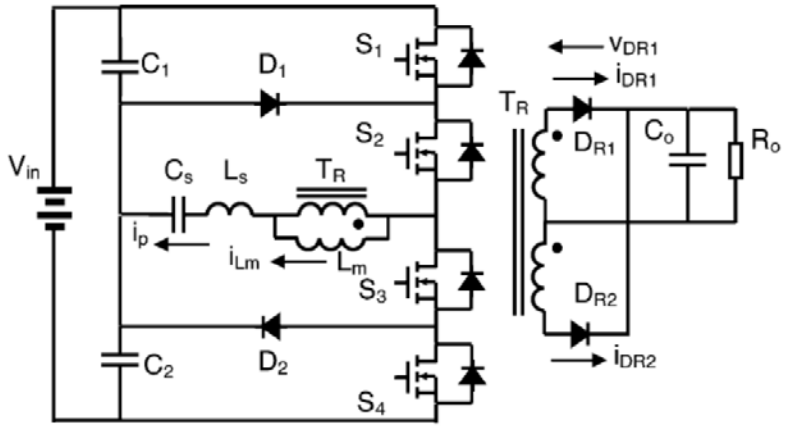
LLC resonant converters, illustrated in Fig. 1.26, have been studied for a long time. In 1990, A.K.S. Bhat proposed LLC resonant converter [C.50]. However, the LLC converter was designed similar as a series resonant converter. Thus, its superior characteristics were not fully utilized. For a while, the LLC resonant converters were almost neglected. However, in 2002, B. Yang and F.C. Lee revealed the advantages of LLC resonant converters [C.51]. Since then, LLC resonant converters have drawn a lot of attention [C.51]–[C.59].



(a)LLC resonant converter proposed in [C.50].



(b) Half-bridge LLC resonant converter with SR [C.53].



(c) Three-level LLC resonant converters [C.56].

Fig. 1.26. LLC resonant converters presented in literature.

Based on the LLC resonant tank, different topologies, such as half-bridge and three-level structures, are utilized for different applications [C.51]-[C.59]. Two-phase LLCs are proposed in [C.57]. Variable frequency control is the major control method. A digitally controlled LLC resonant converter is also reported in [C.58]. Optimal designs of LLC resonant converters are discussed in [C.52] and [C.56].

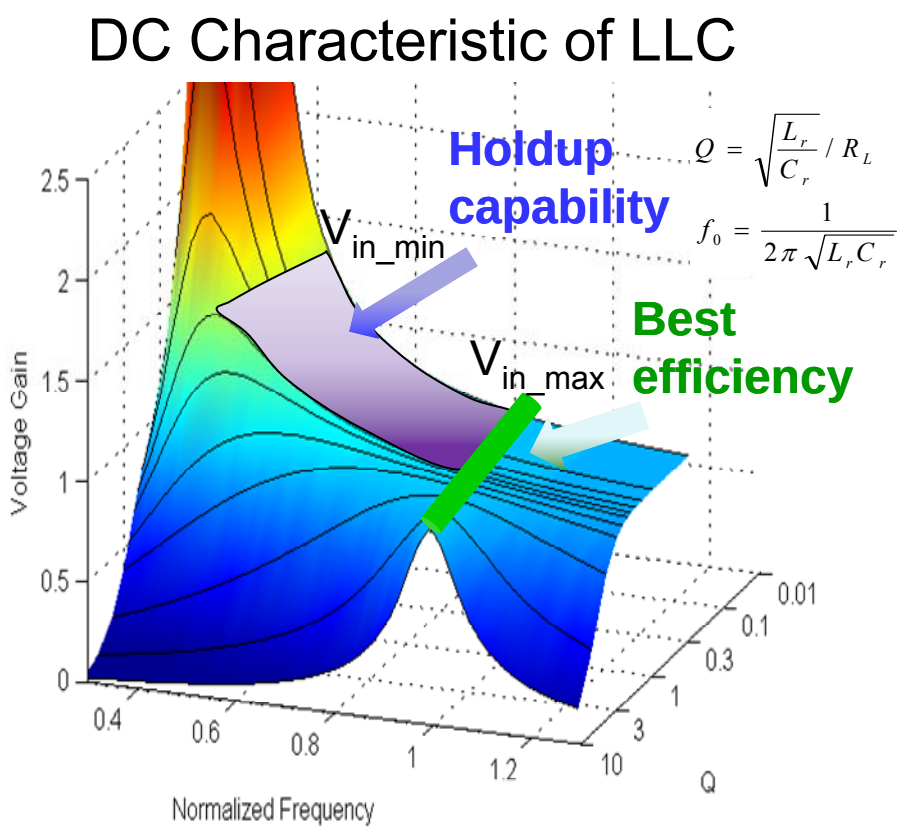


Fig. 1.27. The voltage gain of LLC resonant converters.

The voltage gain of the LLC resonant converter is drawn in Fig. 1.27. With variable frequency control, the voltage gain of LLC resonant converter can be controlled as boost mode or buck mode. During the holdup time, the LLC resonant converter can operate in boost mode. Thus, high voltage gain is achieved. Meanwhile, at the nominal condition, the LLC resonant converter operates very close to the resonant frequency, which is the best operation point to accomplish high efficiency. In addition, voltage gains of different Q converge at the series resonant point. The LLC resonant tank parameters can be optimized to achieve high efficiency for a wide load range. As a result, holdup time extension capability is accomplished without sacrificing the

efficiency at the nominal condition. The LLC resonant converter is considered as one of the most desirable topologies for wide input voltage range.

The advantages of LLC resonant converters are:

- ZVS capability from the zero load to the full load and low turn-off current for primary side switches, so switching loss is low;
- Zero-current-switching (ZCS) is achieved for secondary side rectifiers and low voltage stress;
- High voltage gain capability, which is suitable for holdup time operation, and means that bulky capacitors can be reduced considerably.

Fig. 1.28. B. Lu's 1kW, 1MHz, 400V/48V LLC resonant converter.

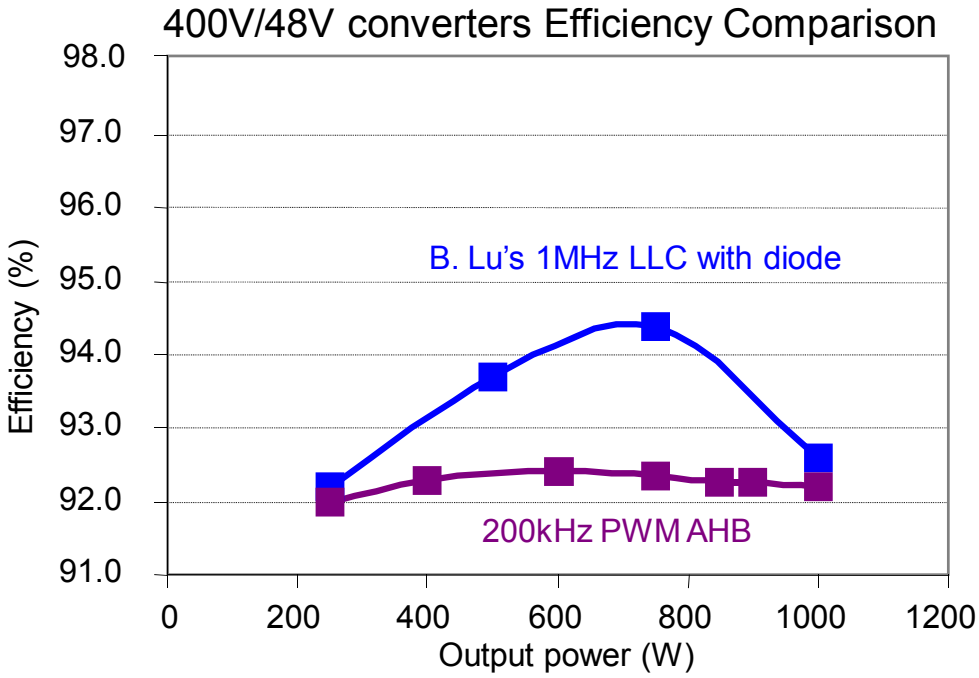


Fig. 1.29. The efficiency comparison of LLC resonant converters and asymmetrical half bridge PWM soft-switching converters.

In [A.15], a 1kW, 1MHz 400V/48V LLC resonant converter is constructed; this is shown in Fig. 1.28. A power density of 76W/in^3 is achieved, which is about 6 times higher than the conventional PWM counterpart. An efficiency comparison of LLC resonant converters and conventional soft-switching PWM converters is given in Fig. 1.29. Apparently, both efficiency and power density have been substantially improved with LLC resonant converters.

However, there are still many issues for LLC resonant converters to deal with; high efficiency, high power density and other performance requirements. The challenges are:

- How to achieve synchronous rectifiers (SR) driving scheme
- How to achieve low EMI noise

- How to achieve startup and current limit
- How to choose the optimal structure for the transformer and SR in high-current applications

Specifically, details are discussed as follows.

i. Synchronous Rectifiers (SR) Driving Scheme

For PWM converters, SR driving schemes are straightforward. For low-voltage applications, self-driven methods are widely applied for two-switch forward, RCD clamp forward, active clamp forward and half bridge circuits [D.2]-[D.12].

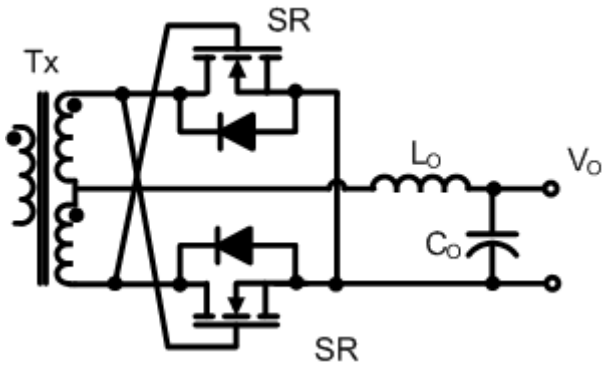
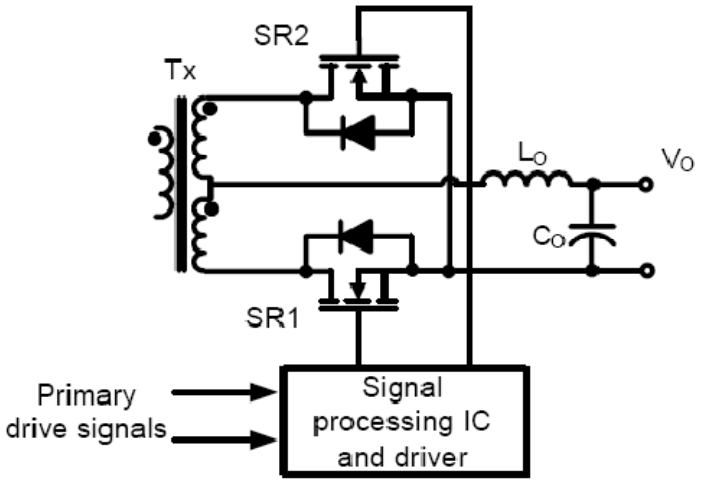


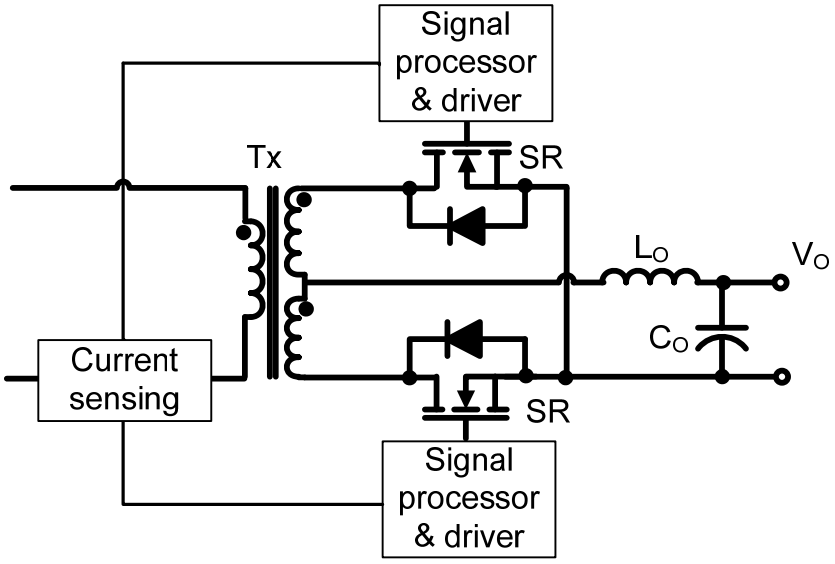
Fig. 1.30. Self-driven SR configurations for PWM converters.

Externally-driven schemes are another category of driving schemes for the SR [D.10]. First of all, for some PWM converters, such as forward converters, the primary side device-driving signals and the secondary side device-driving signals are either in phase or out of phase. As shown in Fig. 1.31 (a), SRs can be driven directly according to the control signal. Secondly, as shown in Fig. 1.31 (b), current-driven SRs are another approach. Specifically, a current transformer is used to sense the SR current. The sensed

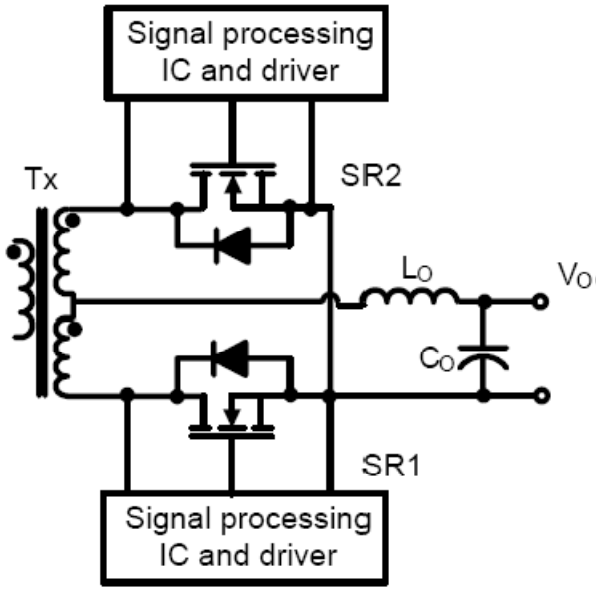
current information is processed by a commercial IC and thus controls the switching of the SR. Thirdly, shown in Fig. 1.31 (c), the voltage information from the SR can be used to drive the SR. For instance, the drain-source voltage of the SR can be sensed to determine the on and off timing of the SR.



(a) Control-driven SR



(b) Current-driven SR



(c) Voltage-driven SR

Fig. 1.31. Externally-driven SR configurations.

For resonant converters, not all the conventional SR driving schemes can be applied. Thus, thorough investigation of SR driving schemes for resonant converters is very important.

Generally speaking, power conversion topologies of resonant converters can be classified into two types, based on the circuit configuration: the voltage-fed inductor-loaded configuration and the current-fed capacitor-loaded configuration [D.37]. For a topology with a voltage-fed inductor-loaded configuration, such as parallel resonant converters and series-parallel resonant converters, voltage self-driven schemes can be applied for SR driving, as shown in Fig. 1.32 [D.37]. However, this driving method is not optimal due to the sinusoidal voltage waveform on the secondary winding of the power transformer (in PWM converters, the voltage on the secondary winding of the

power transformer is a square wave). During the initial and end conduction intervals of the SR, the driving voltage is very low. Thus, higher conduction losses are generated.

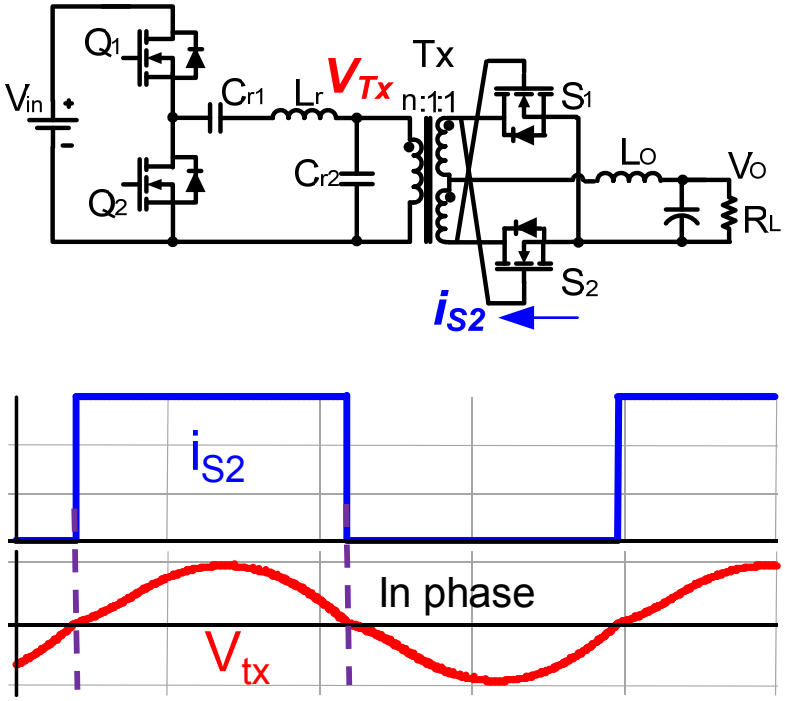
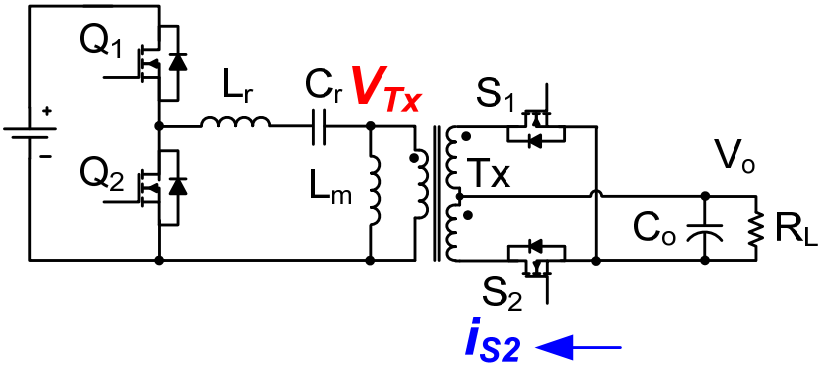


Fig. 1.32. Examples of resonant converters with self-driven SR: LCC resonant converters. Self-driven SR can be achieved with explanation of the waveforms.



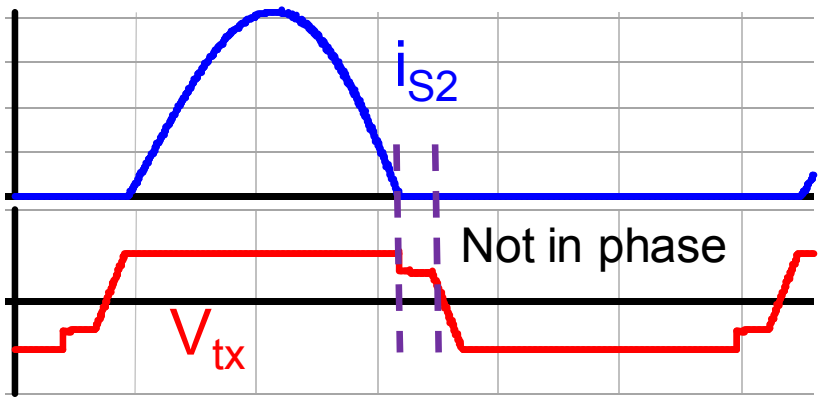


Fig. 1.33. Examples of resonant converter with current-fed capacitor-loaded structure: LLC resonant converters. Self-driven cannot be achieved for LLC resonant converters due to out of phase of voltage and current waveforms.

Fig. 1.34 illustrates an example of turn-on and turn-off timing of the primary side and the secondary side devices of LLC resonant converters. Unlike PWM switching converters, the on and off timing of the switches on the primary side of the power converter circuit and the on and off timing of the switches in the SR on the secondary side of the circuit are not exactly in phase for resonant converters, and thus they cannot use the same driving signal for control of the conduction times. Otherwise, the SR would conduct circulating energy, namely a reverse current from the load to the source; thus causing much increased RMS currents and turn-off current, and causing efficiency to deteriorate dramatically. Therefore, a different driving arrangement for the SR is required.

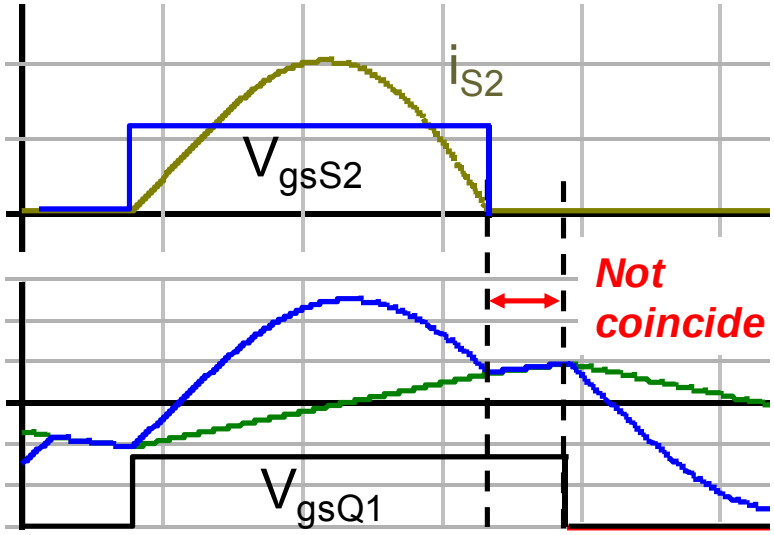


Fig. 1.34. SR drive timing waveforms of LLC resonant converters. Direct control SR drive cannot be achieved for LLC resonant converters due to out-of-phase of driving signals.

ii. EMI performance

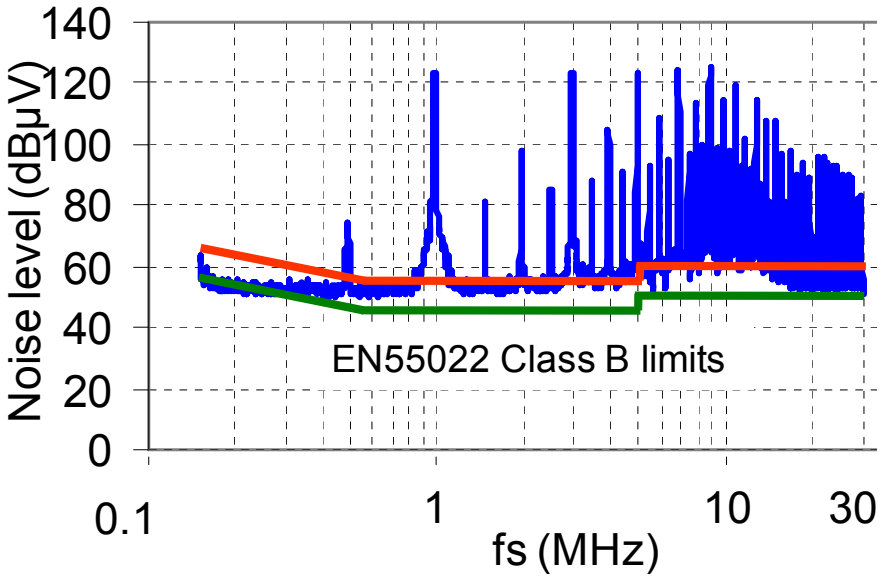


Fig. 1.35. CM noise spectrum of LLC resonant converters.

In EMC standards, such as FCC part 15 in the United States and EN55022, CISPR 22 in Europe, the conducted EMI noise emissions of devices are limited. It is required to meet the EMI standard for front-end converters.

The measured EMI noise spectrum of LLC resonant converters is shown in Fig. 1.35. It is a stringent challenge to reduce the EMI noise due to the EMI standard requirement.

The mechanism of conducted EMI emissions of LLC resonant dc-dc converters is not clear and should be studied thoroughly. The DM and CM EMI noise models for LLC resonant converters are needed, and the switching frequency's impact on the EMI emissions of LLC resonant converters should be provided.

One of the goals of this dissertation is to build EMI model for LLC resonant converters and study noise reduction techniques.

iii. Startup and current limit

Dc-dc converters are required to apply startup control schemes or circuitries to reduce the large in-rush current when they are turned on.

The current limitation capability must be provided for all the working conditions, especially for startup and overload conditions. The purpose of over-current protection is to limit the current stress in the system during over-load or short circuit conditions, and also to limit the inrush current during start up when the output voltage is zero, so that the power converter can be protected from destructive damage under those conditions. Telecom power supplies require a constant output-current characteristic.

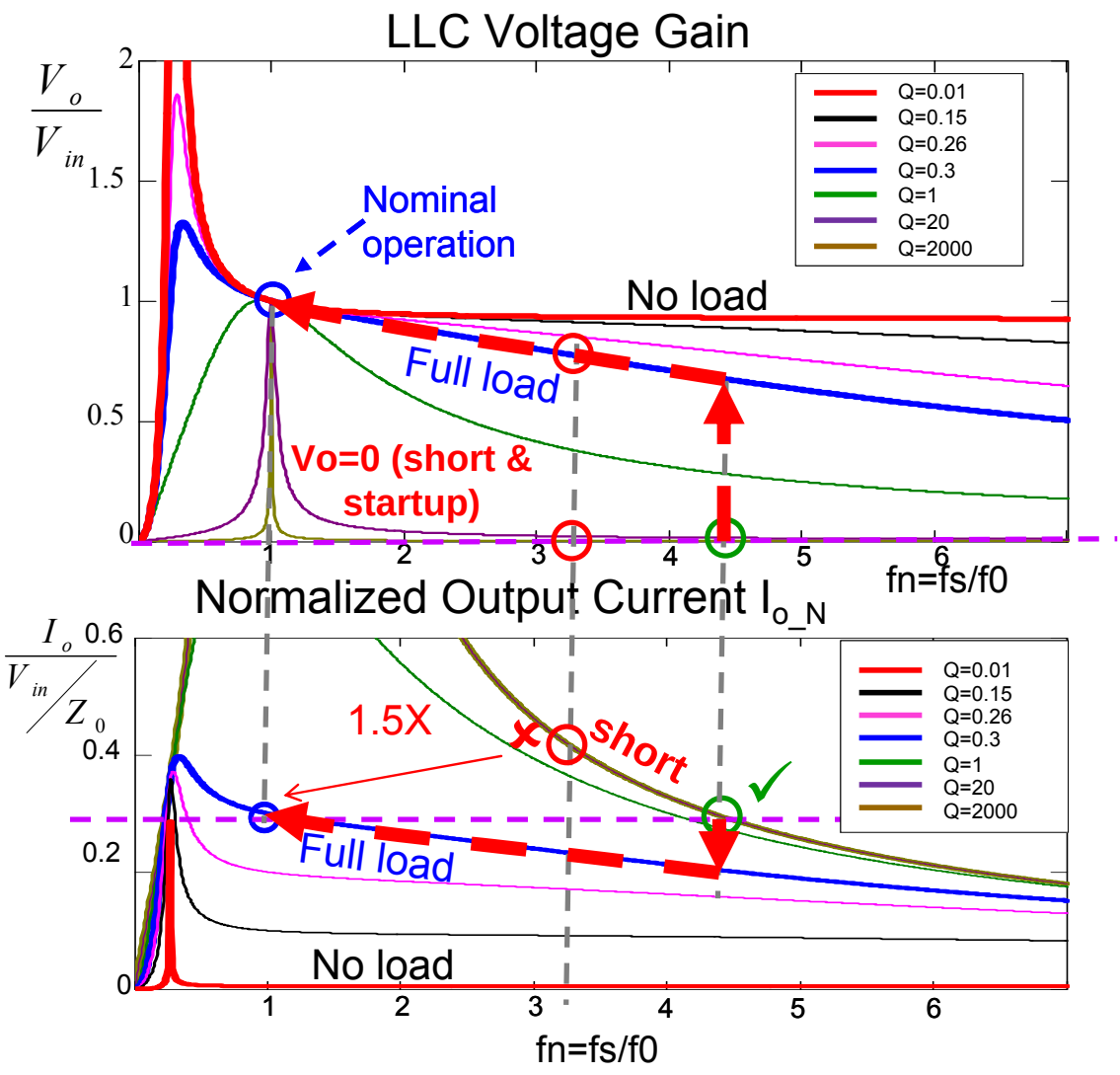


Fig. 1.36. Startup and current protection issues of LLC resonant converters. The conventional way to startup is to increase the fs very far from the nominal condition.

To limit the current, the switching frequency has to be increased considerably. At the resonant frequency, the LLC resonant tank impedance is almost zero. Therefore, high current occurs at over load conditions. With the increase of switching frequency, the resonant tank impedance is also increased. The tank current can be limited; however, on the right-hand side of the series resonant point, the voltage gain becomes very flat. The

frequency selectivity is very poor. Thus, to limit the current, the frequency has to be pushed much higher than the nominal frequency. This phenomenon is also illustrated in Fig. 1.36. For high-frequency (MHz) LLC resonant converters, doing this is not practical.

To overcome startup and current limitations, this work focuses on improving the characteristics of the LLC resonant converters with topology synthesis and shaping the voltage gain characteristics of the resonant tanks. To achieve the best efficiency, the band pass filter characteristic is still preferred and thus should be maintained. For startup and current limit capability, the voltage gain should be reshaped to increase the frequency selectivity and controllability. Thus, sharp voltage gain curves are expected. Finding a way to achieve the gain reshaping and improve the performance of the LLC resonant converters is a stringent challenge.

iv. Transformer termination loss and SR parallel issues

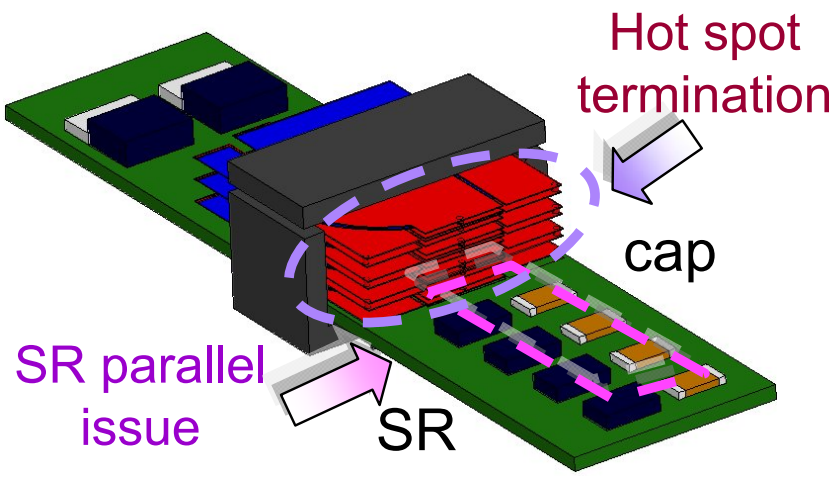


Fig. 1.37. Conventional transformer and the secondary side structure. Issues are lossy termination and SR paralleling.

The conventional planar transformer and the secondary side structure are depicted in Fig. 1.37. The circuit schematic of the transformer and SR structure is shown in Fig. 1.38. For low-voltage high-current applications, a paralleled winding structure is a common practice. However, this structure suffers high termination losses. Due to the proximity effect and skin effect, the currents in adjacent terminals with opposite directions attract each other. Thus, very high losses and hot spots are generated. This termination loss deteriorates efficiency significantly. High termination loss is a barrier to improving the system efficiency.

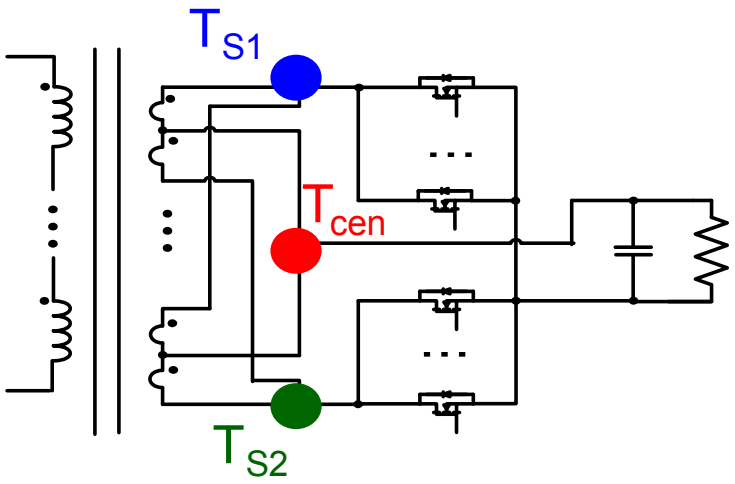


Fig. 1.38. Circuit schematic of the conventional transformer and SR structure.

On the other hand, to reduce the high current conduction loss, a large number of MOSFETs must be paralleled as a SR. For the conventional design, all SRs are placed on the motherboard. Physically speaking, a large loop of the secondary side rectifiers is inevitable. Although a multi-layer printed circuit board (PCB) with heavy coppers can reduce dc conduction loss, there is little effect in reducing the high frequency ac losses.

Consequently, a large distribution loss will be generated. In addition, for large number of SR devices, it is extremely difficult to achieve a symmetrical layout for each SR. Hence, current-sharing of the SR is a severe problem.

Thus, an improved transformer and the secondary side structure are critical to improve the system efficiency and need further investigation.

v. Transformer winding loss and magnetic integration

For conventional PWM converters, such as forward, half-bridge, and full-bridge circuits, the magnetizing inductance required is usually large. Hence, there is no gap in the transformer design. To reduce winding loss, interleaving techniques are widely applied According to interleaving winding design, the skin effect and proximity effect can be effectively reduced. Thus, lower winding loss can be achieved. On the other hand, interleaving can also reduce the leakage inductance, which causes problems for some PWM converters.

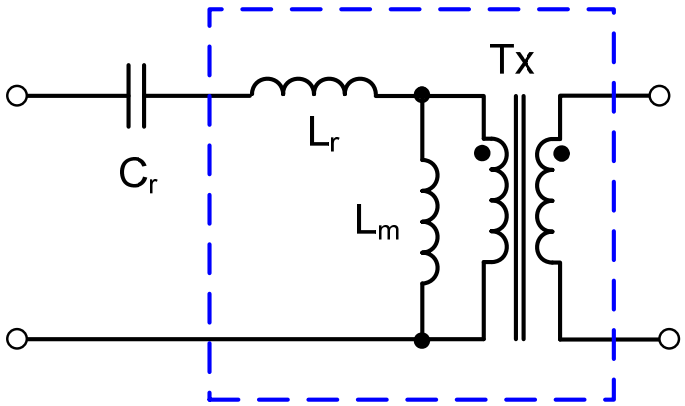


Fig. 1.39. Magnetic components integration: transformer, magnetizing inductance and leakage inductance.

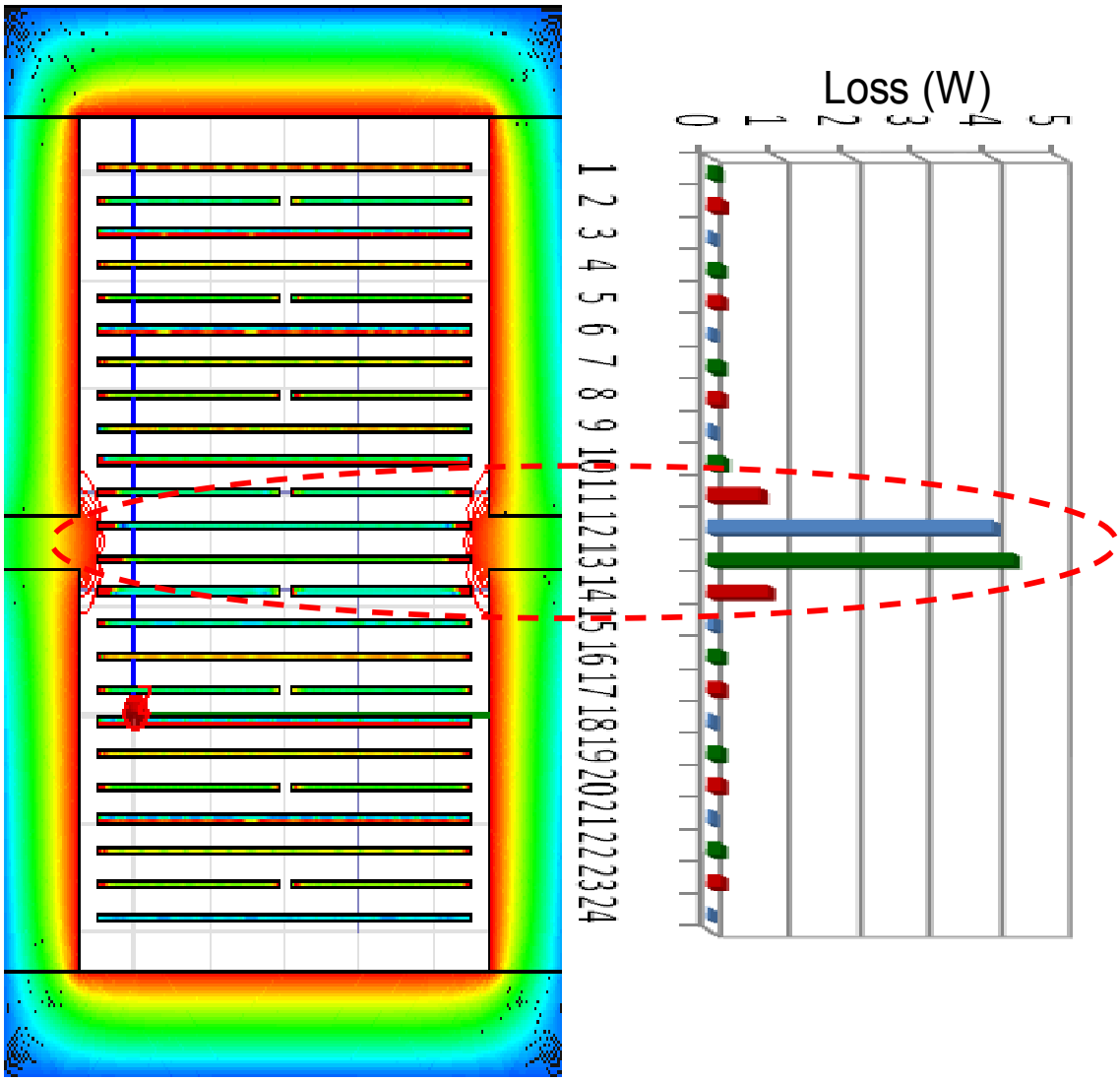


Fig. 1.40. Current, loss and flux distribution of the conventional transformer design. Very high loss close to the gap due to fringing flux.

However, for LLC resonant converters, there are three magnetic components, which are depicted in Fig. 1.39. To meet the power density requirement, it is preferable to integrate the magnetic components. It is very attractive to integrate all the magnetic components into one.

The PCB winding is adopted in the conventional planar transformer structure, which is shown in Fig. 1.40. For LLC resonant converters, normally, magnetizing inductance is used to achieve ZVS and designed as a small value. A large gap is normally required to achieve the designed magnetizing inductance. However, due to the large gap, fringing flux penetrates the PCB winding. Hence, very high eddy current is generated. The high winding loss is unavoidable due to strong fringing effect. On the other hand, as we can see from Fig. 1.40, the winding current of the PCB winding is very unevenly distributed. Therefore, excessive winding loss is generated. Based on the FEA result, there is very high winding loss. This is detrimental to meeting the high efficiency requirement.

Fig. 1.41 illustrates the conventional transformer design to achieve enough leakage inductance for series resonant inductance. A sandwich structure is applied. The secondary side windings are interleaved with the primary side windings. To achieve enough leakage inductance, the air space between the primary and secondary side windings is large. It can be observed the outer layers of the secondary side windings take a lot of current, while the inner-layer copper plates conduct very little current. Thus, high conduction losses are generated.

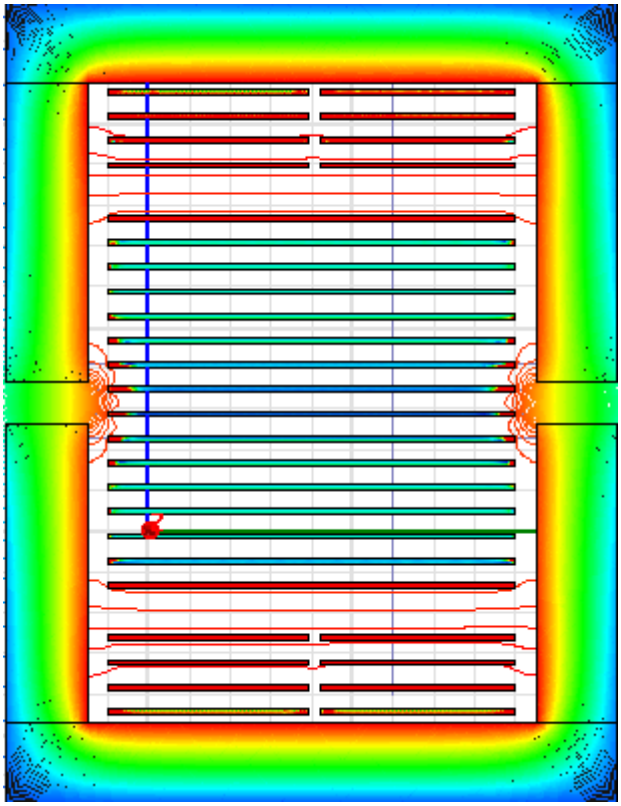


Fig. 1.41. The conventional transformer design to utilize leakage inductance as series resonant inductance.

Determining how to achieve an optimal integration solution with minimum loss is very challenging. A novel transformer winding structure is required to reduce the winding losses. An optimal design of integrated magnetic components is the key to improving the system power density and efficiency.

1.3 Dissertation Objective and Outline

This dissertation is divided into four chapters. They are organized as follows.

The first chapter is the background review of targeted dc-dc conversions with holdup time requirements. Trends for these applications are high efficiency, high-power density

and low profiles. To achieve high power density, high switching frequency is a must. This calls for advanced technology. Conventional PWM circuits can achieve good performance within a very narrow voltage operation range; however, to deal with operation with a very wide voltage range, conventional circuits generally sacrifice performance, such as efficiency. In contrast, resonant converters may introduce opportunities to overcome the drawbacks of the PWM converters. The primary target of this dissertation is to develop suitable topologies and techniques of resonant converters to achieve high-efficiency and high-power-density dc-dc conversions for wide-voltage-range operations. Front-end dc-dc conversions and capacitor charging applications are two specific examples for targeted applications.

In Chapter 2, synchronous rectifications are studied for front-end dc-dc conversions. SR driving schemes are the key to efficiency in low–voltage, high-current front-end applications. Reviews of the existing SR driving scheme for PWM and resonant converter are given, and the challenges of the SR driving scheme of LLC resonant converter is addressed. A novel SR driving scheme is proposed to solve the SR driving issues of LLC resonant converters. With the proposed SR driving method, high efficiency and low stress operation are achieved and are verified experimentally.

EMI issues for LLC resonant converters are addressed in final part of Chapter 2. To thoroughly understand the EMI issues of LLC resonant converters, an EMI model is proposed. Based on the proposed EMI model, several EMI suppression approaches are proposed. With step-by-step improvements, EMI noises are attenuated substantially

without the assistance of an EMI filter. The proposed EMI reduction techniques are discussed and compared.

Chapter 3 is dedicated to the investigation of suitable resonant topologies for easy startup, inherent current limiting and lower circulating energy. LLC resonant converters provide many advantages over PWM converters. However, startup and over current protection are issues for LLC resonant converters. LLC can be treated as a band-pass filter in terms of voltage gain. Due to the flat voltage gain characteristics, the frequency selectivity of the LLC band-pass filter is very poor. As a consequence, it is very difficult to achieve current-limiting functionality. To solve these issues, many papers propose alternative techniques, such as modulation control and clamping circuits. However, none of these can solve the problems without sacrificing the performance of LLC resonant converters. Based on the notch filter characteristics, novel multi-element resonant converters are proposed to solve the current limit issues without hurting the performance. Furthermore, a higher-order harmonics injection concept is proposed to reduce the circulating energy of the resonant converters. A family of multi-element resonant converters with double band-pass filter characteristics are proposed to achieve the utilization of the third-order harmonics.

Chapter 4 describes how to achieve high efficiency for low-output-voltage, high-output-current dc-dc converters. Great attention should be paid to alleviating the extra winding loss caused by the magnetizing current. High termination loss is another stringent challenge of transformer design. An improved transformer structure is proposed to reduce the termination loss and to simplify the transformer winding

configuration. This optimal transformer structure is proposed and verified with FEA and hardware. Low loss is achieved for transformer with the integration of an extra two resonant inductors. The proposed concepts could be extended to other resonant dc-dc converters.

Finally, conclusions and the suggestions for future work are given at the end of this dissertation.

Chapter 2

System Optimization for LLC Resonant Converters

2.1 Review of Prior Optimal Design Methodologies of LLC resonant converters

For conventional PWM converters, it is difficult to achieve both high efficiency and a wide operation range. LLC resonant converters exhibit superior performance, such as low switching loss and low voltage stress on the secondary side rectifiers, as well as higher efficiency, than PWM converters

In [A.15], B. Lu proposed an optimal design strategy of LLC resonant converters. In B. Lu's work, the LLC resonant converter design goal is to achieve minimum loss at normal operation conditions and be able to achieve the required maximum gain to ensure a wide operation range. This work reveals the relationships between the resonant inductance ratio L_n and quality factor Q with the converter performance, especially the conduction loss at normal operation conditions and the voltage operation range. These relationships can be used to develop an optimal design methodology of LLC resonant converters. B. Lu's design methodology can be explained by the flow chart shown

in Fig. 2.1. The keys of successful design rely on choosing the suitable magnetizing inductor and the resonant inductance ratio.

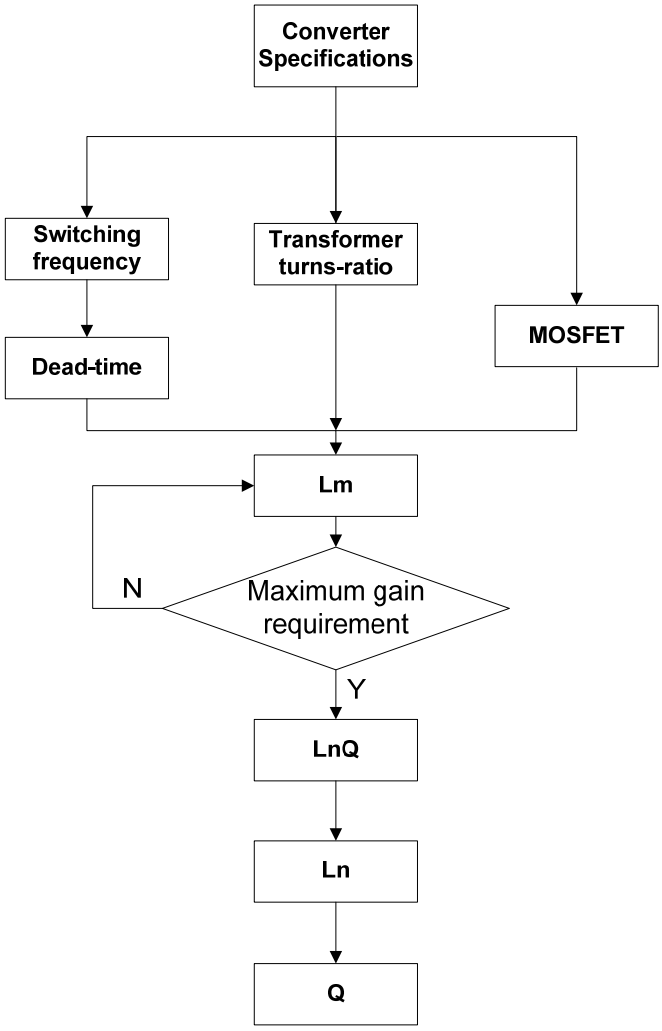


Fig. 2.1. B. Lu's optimal design procedure for LLC resonant converters.

In B. Lu's work, a 1kW, 1MHz 400V/48V LLC resonant converter with diode rectifiers was built to demonstrate the design results of the LLC. The planar transformer is applied in this prototype, and PCB windings are used. B. Lu's design shows significant improvement over conventional PWM converters, and has been discussed in

Chapter I. For high-frequency (1MHz) and high-voltage-output (48V) applications, even Schottky diodes show considerable reverse recovery current. From [A.15], the loss breakdown of B. Lu's 1kW, 1MHz 400V/48V LLC resonant converters is shown in Fig. 2.2.

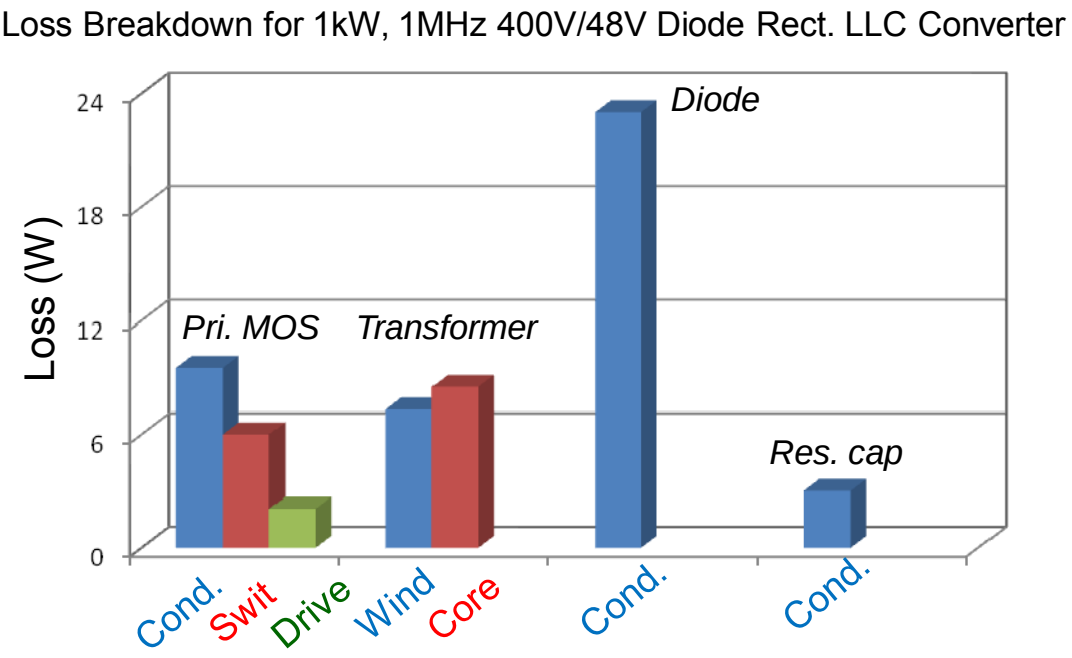


Fig. 2.2. Loss breakdown of B. Lu's LLC resonant converter.

B. Lu's methodology reveals an optimal design to achieve high efficiency with wide input voltage range for holdup time operation. Nevertheless, at high frequencies, the dead time design may affect the optimal design result.

In order to quantify the dead time effect on optimal design results, Y. Liu proposed an improved optimal design strategy in [A.16]. In B. Lu's design, the primary side and the secondary side rms currents are calculated without consideration of dead time. In Y. Liu's work, dead time is considered for conduction loss calculation and hence a more

precise result is obtained. Similarly, more precise switching loss is obtained. Further, Y. Liu's design procedure includes the efficiency analysis over a wide load range; the improved design procedure is shown in Fig. 2.3.

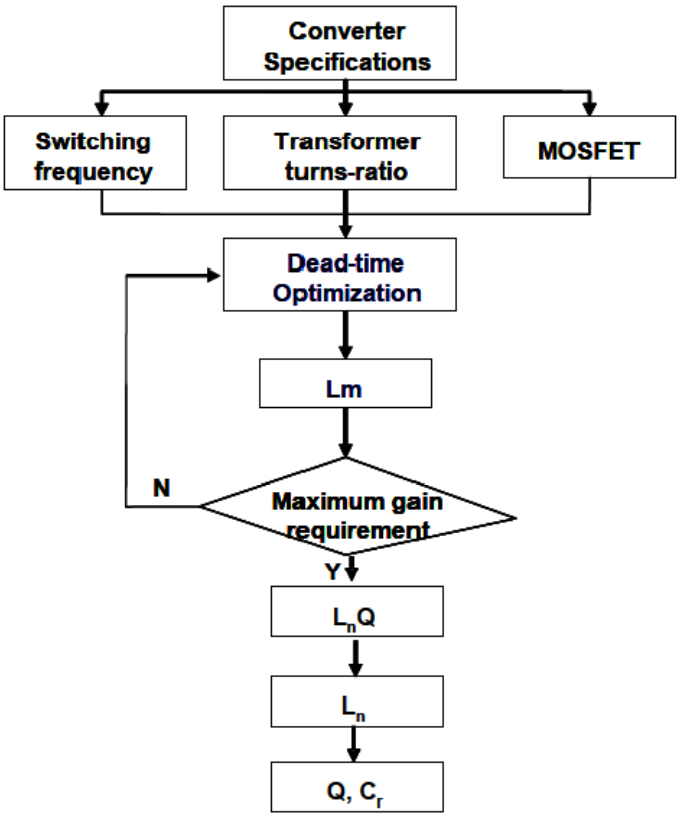


Fig. 2.3. Y. Liu's improved optimal design procedure for LLC resonant converters.

The existing design methodologies focus on optimization of resonant tank parameters and dead time to achieve high efficiency. Nevertheless, the performance of LLC resonant converters can be further improved from optimization of the devices, the synchronous rectification driving scheme, EMI noise cancelation and topology.

In this chapter, system optimization of LLC resonant converters is investigated. Optimal devices suitable for resonant soft-switching applications are studied. Novel driving schemes for synchronous rectifiers are proposed to improve the efficiency of LLC resonant converters, and novel EMI suppression techniques are proposed to improve the EMI performance.

2.2 Improved Devices Selection for LLC Resonant Converters

2.2.1 Performance Evaluation of Super-Junction MOSFETs for High Frequency Resonant Converters

Among high-voltage (>500V) MOSFETs, super-junction MOSFETs, such as Infineon's CoolMOS, offer lower R_{ds} (on) than conventional MOSFETs [D.41], and are a natural choice to improve efficiency for this application. However, there is a history of converter failure due to reverse recovery problems with the primary switch's body diode. Before deciding to use CoolMOS devices for use in a LLC resonant converter, it is necessary to investigate their performance in this application. Field failures of PWM soft-switching phase-shift full-bridge converters have been attributed to a large reverse recovery charge in the primary side MOSFET body diode [D.42], and [D.43]. Under low-load conditions the device cannot fully recover, and the large reverse recovery current can cause the device to enter secondary breakdown, leading to failure. The unique structure of super-junction MOSFETs, such as CoolMOS, avoid this failure mode by providing a different path for the reverse current [D.44]; however, the reverse recovery charge of CoolMOS devices is large and can cause a loss of efficiency.

Based on the analysis of the operating waveforms of the LLC resonant converter, it can be seen that the conditions that caused failure of the primary side devices in the phase-shift full-bridge converter are present in the LLC converter as well. The conventional MOSFET failures occur when the current through the device is small, leading to a small reverse voltage applied to the device. With a small reverse voltage, the time that the device conducts in the first quadrant is not sufficient for the body diode to fully recover. The two factors that influence the reverse recovery of the body diode have been identified as the voltage during the first quadrant conduction of the MOSFET, and the length of time the body diode is reversed biased before the device is turned off.

The failure mode in the phase-shift full-bridge was caused by the reverse recovery charge of the primary side device's intrinsic body diode. The failure was reported for conventional silicon MOSFETs. In a super-junction MOSFET, P columns are introduced into the N-epi region. The P columns act to balance out the charge in the conduction channel and allow for the device to have a higher doping concentration while still maintaining the same blocking voltage [D.41]. The higher doping concentration in the N-epi region results in a much lower on-resistance in the device. While a portion of the reverse current flows laterally through the P+ region in a conventional MOSFET, the reverse current in a super-junction MOSFET flows through the P compensation columns and cannot trigger the intrinsic bipolar device. In this way, a super-junction MOSFET cannot fall into secondary breakdown due to a large reverse current. While super-junction MOSFETs do not suffer from the failure mechanism that

has been reported in conventional devices when used in soft-switching converters, they still have large reverse recovery charge, which could cause a soft-switching converter to not behave as designed and have poor efficiency due to partial or full loss of zero voltage switching.

In the case without reverse recovery, the primary switches operate with zero voltage switching, as intended. In the second case, there is a partial loss of zero voltage switching due to the reverse recovery of the primary switches. Since the body diode is not fully recovered when the device is turned off, the switch cannot immediately begin blocking voltage, and the time from when the switch is turned off until the output capacitance is charged is increased. Since the output capacitance takes longer to charge than the designed dead time, the opposite switch in the totem pole will be turned on before the voltage across it has reached zero volts. Since zero voltage switching has been lost, the efficiency of the converter will be decreased.

It can be seen that as the frequency increases and the reverse recovery of the body diode takes more of the dead time to recover, the voltage across the opposite switch will be higher, resulting in a greater loss of efficiency. A third condition can also occur due to the reverse recovery of the body diode. In this case, the body diode does not recover at all before the end of the dead time. The opposite switch turns on with the full voltage across it and any remaining charge in swept out of the body diode. In this case there is total loss of soft switching, so the efficiency of the converter will be low. Furthermore, if a significant amount of charge is remaining in the body diode when the other switch

is turned on, a large current will flow through both devices and the increased component stress could cause the devices to fail.

For low-frequency operation, the slow body diode may have enough time to recover. Thus, there are no significant adverse effects. However, for high-frequency operation, such as 1MHz, the body diode reverse recovery might become a potential issue. Thus, it is not recommended to apply super-junction MOSFETs with slow body diodes at very high frequencies.

In this work, to avoid the body diode reverse recovery problems, MOSFETs with fast body diodes are considered as the candidates of the primary side MOSFETs.

2.2.2 Improved Primary Side Devices Selection for LLC Resonant Converters

In B. Lu's LLC resonant converter, an IXFH21N50F with a fast body diode was chosen as the primary side device. To further reduce the primary side loss and increase efficiency, it is worthwhile to investigate the device selection.

There have been several device and material figures of merit (FOMs) published. Some of these focus on evaluating the semiconductor material performance, and some of them focus more on evaluating the device's processing technology.

In 2008, Y. Ying and F. C. Lee proposed a new FOM to further improve the FOM [D.1].

Y. Ying and F. C. Lee proposed a new FOM in [D.1] with consideration of switching loss, gate driving loss and conduction loss of the MOSFETs.

$$P_{loss} = \underbrace{\frac{V_{in} I_o}{2} \frac{(Q_{gd} + Q_{gs2}) R_g}{V_{gs} - V_{plt}} f_s}_{\text{Turn on loss}} + \underbrace{\frac{V_{in} I_o}{2} \frac{(Q_{gd} + Q_{gs2}) R_g}{V_{plt}} f_s}_{\text{Turn off loss}} + \underbrace{I_o^2 R_{on} \frac{V_o}{V_{in}}}_{\text{Cond. loss}} + \underbrace{Q_g V_{gs} f_s}_{\text{Drive loss}}$$

(2.1)

$$K_{gs2}(V_{DR}) = 1 + \frac{V_{DR}}{V_{plt} - V_{th}} \frac{2V_{plt}(V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g} \tag{2.2}$$

$$FOM = (Q_{gd} + K_{gs2} \cdot Q_{gs2}) \cdot R_{dson} \tag{2.3}$$

However, these existing FOMs are derived based on the hard-switching PWM converters. Thus, they are not suitable for soft-switching resonant converters.

To choose preferable MOSFETs for soft-switching LLC resonant converters, proper device selection criteria should be identified.

Owing to ZVS operation of LLC resonant converters, the turn-on loss of MOSFETs is virtually eliminated. Thus, the turn-off loss, gate-driving loss and conduction loss should be considered to derive the proper FOM. The derivation of the FOM of MOSFETs for LLC resonant converters is described below.

The total loss of MOSFETs, which includes turn-off loss, conduction loss and gate-driving loss, can be expressed as:

$$P_{loss} = \underbrace{\frac{V_{in} I_{off}}{2} \frac{(Q_{gd} + Q_{gs2}) R_g}{V_{plt}} \cdot f_s}_{\text{Turn off loss}} + \underbrace{\frac{I_o^2}{n^2} \frac{\pi^2}{4} R_{on}}_{\text{Cond. loss}} + \underbrace{Q_g V_{gs} f_s}_{\text{Drive loss}} \quad (2.4)$$

$$P_{loss\_\min} = \sqrt{\frac{\pi^2}{2} \frac{I_o^2 I_{off}}{n^2} V_{in} R_g f_s} \sqrt{\frac{1}{V_{plt}}} \sqrt{(Q_{gd\_sp} + Q_{gs2\_sp} + \frac{2V_{plt} V_{gs}}{V_{in} I_{off} R_g} Q_{g\_sp}) R_{on\_sp}} \quad (2.5)$$

$$K_{loss} = 1 + \frac{V_{gs}}{V_{plt} - V_{th}} \frac{2V_{plt} V_{gs}}{V_{in} I_{off} R_g} \quad (2.6)$$

$$FOM = (Q_{gd} + K_{loss} \cdot Q_{gs2}) \cdot R_{on} \quad (2.7)$$

Hence, the FOM of MOSFETs with a fast body diode for LLC resonant converters can be expressed as (2.7). The derived FOM is different from the previously proposed FOMs of MOSFETs for general applications. This is one step forward in the improvement of the FOM proposed by Y. Ying and F. C. Lee. It should be noted that the output capacitances (C_{oss}) of MOSFETs affect both conduction loss and switching loss. The influence of C_{oss} is studied in resonant tank parameter optimization [A.15]. For the sake of simplicity, the effect of C_{oss} is not considered in the derived FOM.

The FOM described in (2.7) is applied to choose the suitable primary side devices for LLC resonant converters. This FOM can be extended to other circuits with the ZVS operation.

For primary side device selection, different MOSFETs selected with the improved FOM are shown in Fig. 2.4. The devices for comparison include: APT5024BFLL from

APT, STW20NM50FD from ST, IRFB16N50K from IR, FDP20N50F from Fairchild, IXFH21N50F from IXYS and SPW20N60CFD from Infineon. Because it has the lowest FOM, STW20NM50FD from ST is selected.

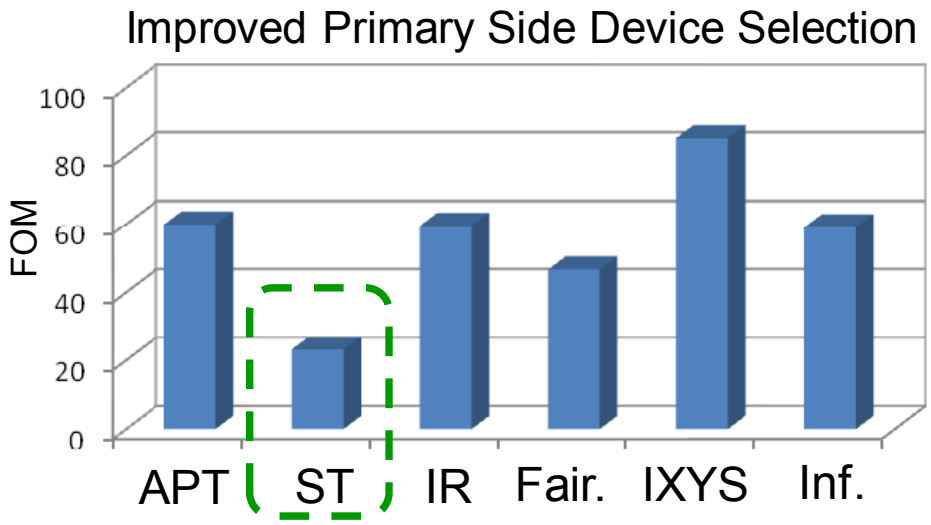


Fig. 2.4.Improved primary side device selection based on improved FOM.

2.2.3 Improved Secondary Side Devices Selection for LLC Resonant Converters

The FOMs of power devices have been discussed for the selection of the primary side devices, but it is also critical to know how to choose the correct secondary side devices.

While diodes have been used in the past in power converter designs, power MOSFETs have much lower forward voltage drop than, for example, Schottky diodes in low–voltage, high-current applications.

To choose the favorite SR devices for soft-switching LLC resonant converters, proper device selection criteria should be identified. The simulated and experimental waveforms of output rectifiers for LLC resonant converters are depicted in Fig. 2.5

and Fig. 2.6. The rectifiers can achieve ZVS turn on and ZCS turn off. Furthermore, according to the proposed novel SR driving scheme, the body diode conduction of an SR is almost zero. Thus, the output rectifiers can be considered to be virtually without reverse recovery loss. This is the basic assumption of using the SR for LLC resonant converters. This is normally true when the LLC resonant converters operate at the resonant frequency or less.

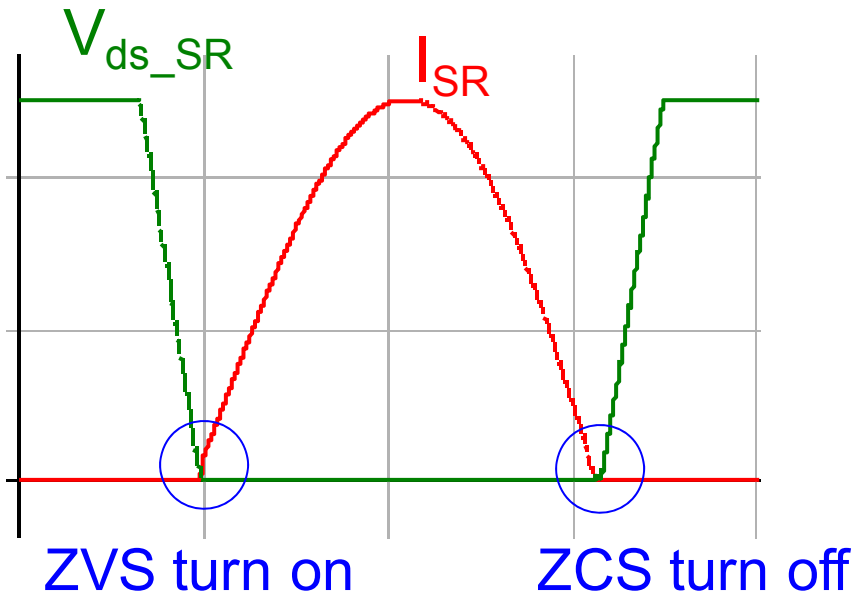


Fig. 2.5. Simulated waveforms of output rectifiers for LLC resonant converters.

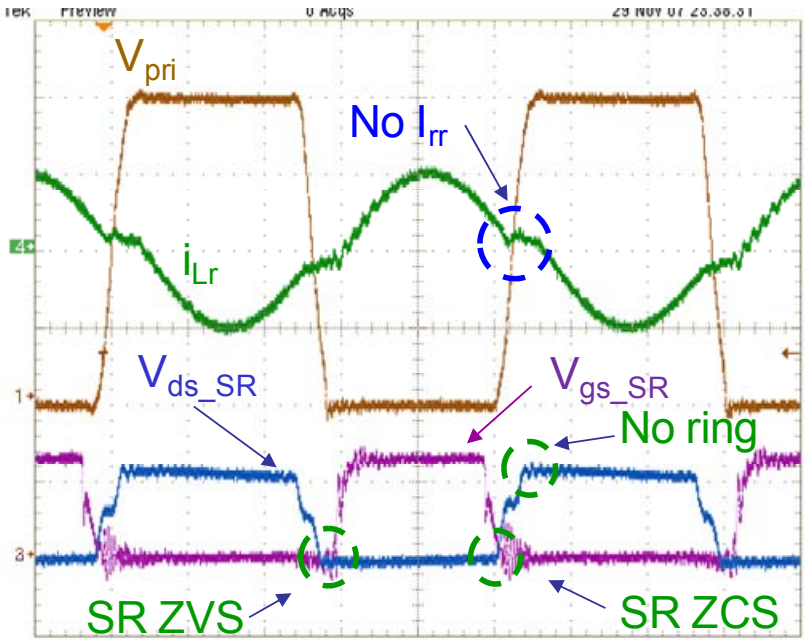


Fig. 2.6. Experimental waveforms of output rectifiers for LLC resonant converters.

Hence, the FOM of the SR for LLC resonant converters can be derived as follows. To simplify the derivation, it is assumed LLC resonant converters operate at the resonant frequency.

The total loss of the SR, which includes conduction loss and driving loss, can be expressed as:

$$P_{loss\_SR} = \underbrace{I_{rms\_SR}^2 R_{on\_SR}}_{\text{Cond. loss}} + \underbrace{Q_{g\_SR} V_{gs\_SR} f_s}_{\text{Drive loss}} \tag{2.8}$$

$$P_{loss\_SR} = 2 I_{rms\_SR} \cdot \sqrt{f_s} \cdot \sqrt{V_{gs\_SR}} \cdot \sqrt{Q_{g\_sp\_SR} \cdot R_{on\_sp\_SR}} \tag{2.9}$$

$$FOM = Q_{g\_SR} \cdot R_{on\_SR} \tag{2.10}$$

Hence, the FOM of the SR for LLC resonant converters can be expressed as (2.10).

The FOM described in (2.10) is applied to choose the suitable SR devices for LLC resonant converters. This FOM can be extended to other circuits with the ZVZCS operation.

For SR devices selection, different MOSFETs with the improved FOM are shown and compared in Fig. 2.7. The devices for comparison include: FDP2532 from Fairchild, IXFP102N15T from IXYS, SUM75N15-18P from Vishay and IRFI4321PbF from IR. Because it has the lowest FOM, FDP2532 SR devices from Fairchild are selected.

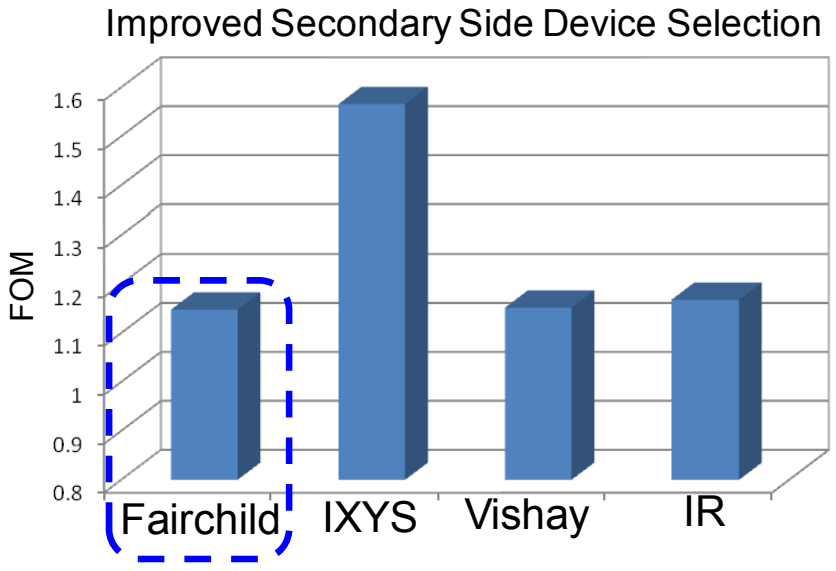


Fig. 2.7. Improved secondary side device selection based on improved FOM.

2.3 Proposed Novel Driving Schemes for Synchronous Rectifications in Resonant Converters

As discussed in Chapter 1, it is very challenging to achieve SR driving schemes for LLC resonant converters. Thus, different approaches should be investigated.

It has been suggested that SR driving signals can be generated by sensing the SR current with a current transformer. This SR driving method can also be applied to LLC resonant converters. However, there are some limitations to this driving method for high-switching-frequency and high-power-density application. Putting the inductance in series with the synchronous rectifier, which is introduced by the current-sensing transformer, would be detrimental to current commutation in the rectifier. For low-voltage, high-current applications, the extra resistance of the current transformer winding and termination becomes lossy and thus sacrifices efficiency.

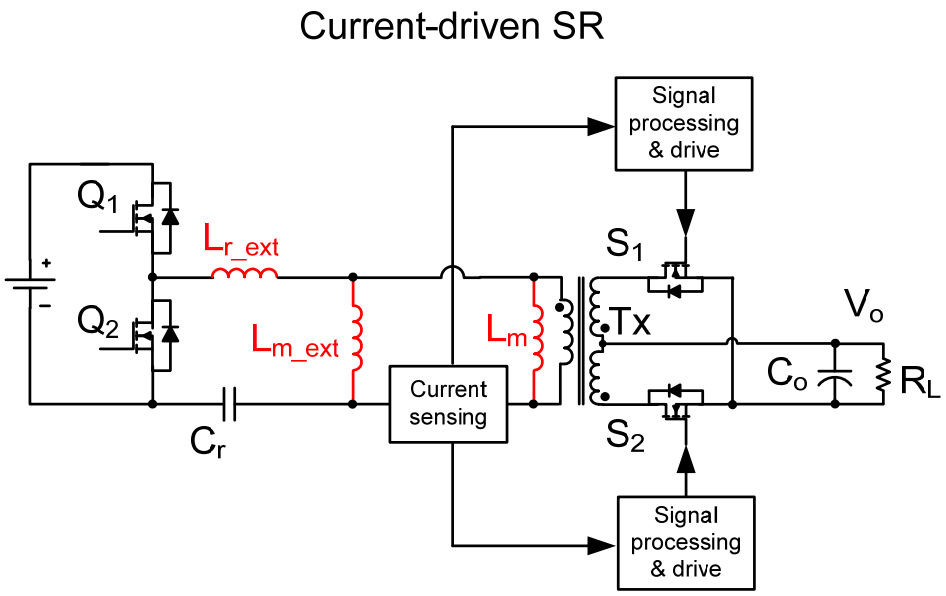


Fig. 2.8. Current-driven SR for LLC resonant converters.

To avoid issues related to the high current, the current transformer can be placed on the primary side [D.45]. However, for LLC resonant converters, the magnetizing inductance is usually utilized as resonant inductance. The magnetizing current is used to achieve ZVS and therefore is designed to have a relatively large value. As a consequence, the directly-sensed primary side current is not exactly in phase with the SR current. This method cannot provide accurate SR driving signals. To solve this problem, an external inductance can be used to replace the magnetizing inductance as the resonant component, which is plotted in Fig. 2.8. However, in this configuration, all the magnetic components have to be designed as discrete components, which defeats the benefits of the magnetic integration for LLC resonant converters. The disadvantages of higher loss, larger size and much more complicated structure make this approach unacceptable.

A promising driving method is to utilize the drain-to-source voltage of the SR, which is depicted in Fig. 2.9. The sensed V_{ds} of the SR is processed by control circuits to determine the level of the current. The SR can be switched in close proximity of the zero current transition. With advanced IC technology and the proper noise immunity layout, the voltage-sensing range reaches a precision of around millivolts without a problem.

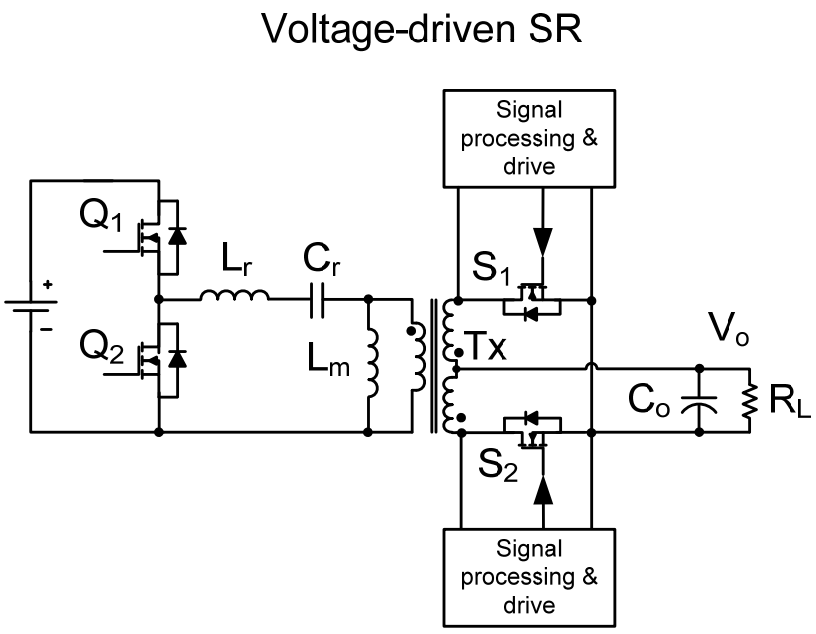


Fig. 2.9. Voltage-driven SR for LLC resonant converters.

It is easy to implement the voltage-sensing SR drive method without breaking the power delivery path of the original circuits. Thus, it is a very attractive strategy. However, the accuracy of this driving scheme is highly affected by the packaging of the SR. Due to the inevitable package inductance, the sensed terminal drain-to-source voltage of the SR is actually the sum of the MOSFET's resistive voltage drop and the package's inductive voltage drop. The sensed $V_{d's}$ of the SR terminal deviates greatly from the real V_{ds} of the MOSFET. The SR drive signal V_{gsSR} is much lower than the expected value.

The duty cycle of the SR D_{SR} can be calculated mathematically. T_{on_SR} and T_s represent the turn-on period of the SR and the switching cycle, respectively. D_{SR} is defined as the ratio of T_{on_SR} and $0.5T_s$. D_{SR} is determined by SR package inductance L_{sr},

SR on-resistance R_{ds_on}, switching frequency f_s, turn-off threshold voltage V_{th1}, and load current I_o. $V_{d's}$ is expressed in (2.11). D_{SR} is derived in (2.12), where the second item in the numerator is related to the phase loss due to L_{sr}. This part equals the phase lead of $V_{d's}$ over V_{ds}. In an ideal case, without L_{sr}, the phase difference should be zero. In (2.12), the third item in the numerator is related to the phase loss due to V_{th1}. In an ideal case, $V_{th1}=0$. In practical applications, $V_{th1}<0$. Thus, the extra phase loss should be considered.

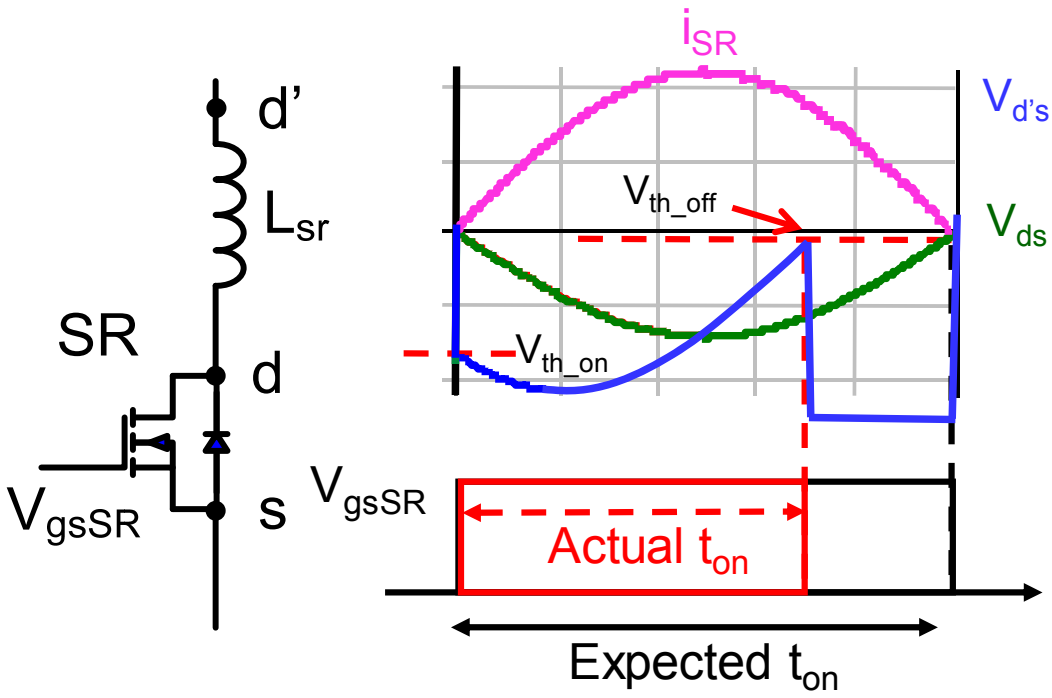


Fig. 2.10. Sensing voltage deviation due to SR package inductance.

The experimental result shown in Fig. 2.11 reveals the duty cycle loss of the SRs.

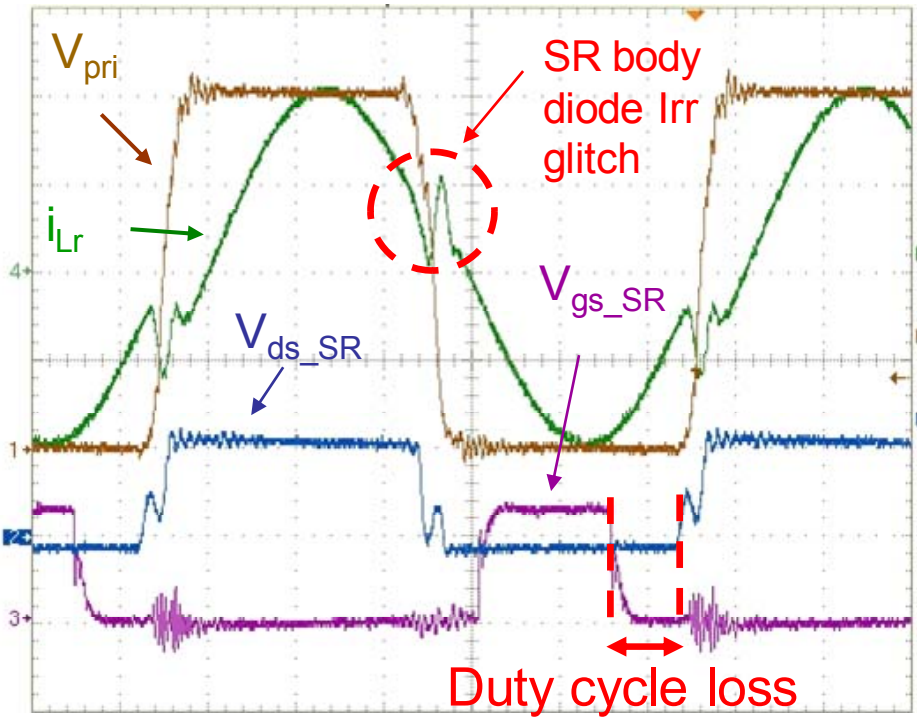


Fig. 2.11. SR driving duty cycle loss due to SR package inductance.

$$V_{d's}(t) = -\frac{\pi}{2} I_o \sin\left[2\pi f_s t + a\tan\left(\frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right)\right] \cdot \left|R_{ds\_on} + j \cdot 2\pi f_s L_{sr}\right| \quad (0 \le t \le 0.5T_s) \tag{2.11}$$

$$D_{SR} = \frac{T_{on\_SR}}{0.5T_S} = \frac{\pi - a\tan\left(\frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right) - a\sin\left(\frac{-V_{th1}}{\frac{\pi}{2} I_o \left|R_{ds\_on} + j \cdot 2\pi f_s L_{sr}\right|}\right)}{\pi} \tag{2.12}$$

The DirectFet is considered to be the device with the least package inductance, at only 0.5nH for its compact package [D.30]. For the tested 1kW 400V-12V prototype, DirectFet IRF6635 is chosen, which has a R_{ds_on} of 1.3mΩ. Fig. 2.12 plots the actual

duty cycle versus the switching frequency at full load for different package inductances. The higher the switching frequency, the worse the duty cycle loss becomes. There is much higher package inductance in packages other than DirectFet, and the operation conditions for these packages are even worse. On the other hand, normally, the duty cycle loss due to effect of V_{th1} is very small. Thus, if the effect of V_{th1} can be ignored, the SR duty cycle can be approximated as $D_{SR} = 1 - a\tan\left(\omega_s L_{sr} / R_{ds\_on}\right)/\pi$.

The approximate SR duty cycle is plotted in Fig. 2.13. It can be observed the SR duty cycle is greatly affected by the impedance ratio of the package inductor and the on-resistor.

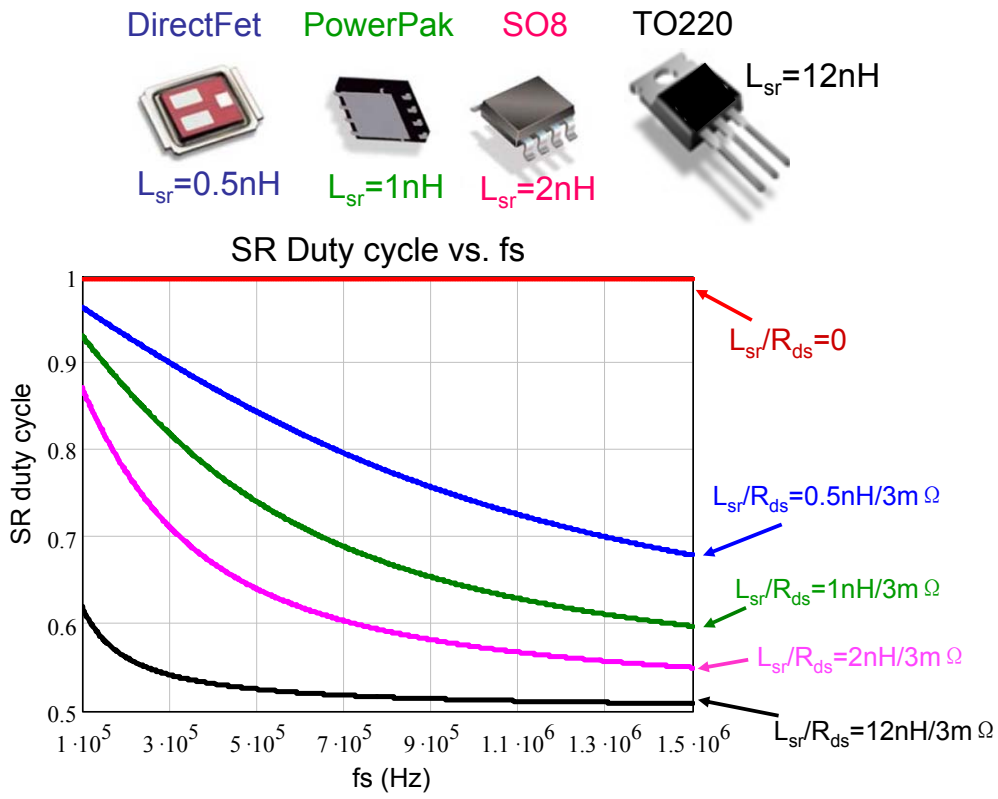


Fig. 2.12. SR duty cycle vs. f_s for different L_{sr}.

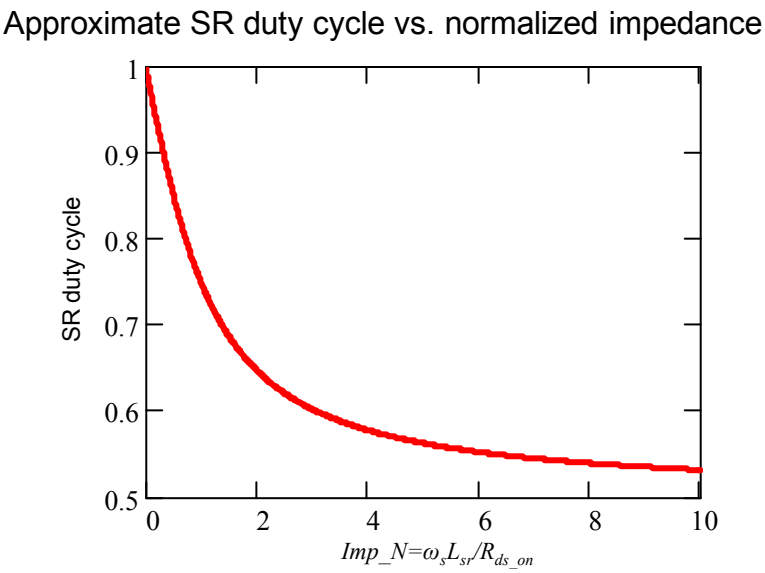


Fig. 2.13. Approximate SR duty cycle vs. normalized impedance.

2.3.1 Proposed Driving Scheme for Synchronous Rectifications in LLC Resonant Converters

It is actually simplest and most cost effective to utilize the R_{ds_on} of SRs as the shunt resistor. The conventional DCR sensing method requires a constant resistance [D.33]. Thus, the passive R and C can restore the current information. However, for SR devices, the impedance is highly non-linear. Thus, this method cannot be applied directly.

In order to overcome the issue of phase deviation due to package inductance L_{sr}, we introduce an improved novel phase compensation driving scheme. Fig. 2.14 shows a block diagram of the proposed SR driving circuit. The main sections of the proposed circuit are the V_{ds} phase compensation network and the signal-processing and gate-driver stages for the SR. The input signal for the proposed driving circuit is a voltage

waveform across the physical terminal of the power MOSFET's SR. Based on the analysis above, such a voltage waveform is actually $V_{d's}$ and cannot be directly used to drive the SR. An active phase compensation network is used to provide the true resistive voltage of V_{ds}. Thus, the generated voltage precisely reflects the conduction period of the SR. The phase-compensated V_{ds}, as the output signal of the compensation network, is then transferred to the next stage. The post-signal processing block consists of a set of window comparators that converts the input signal into control pulses. The driving circuit utilizes these control pulses to ultimately drive the SR using discrete transistors or integrated circuits, which may be specifically developed for the purpose.

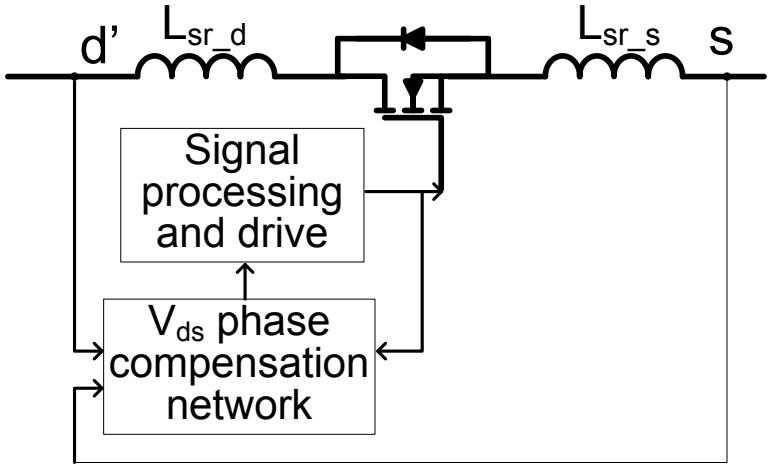


Fig. 2.14. Simplified functional diagram for the proposed SR driving scheme.

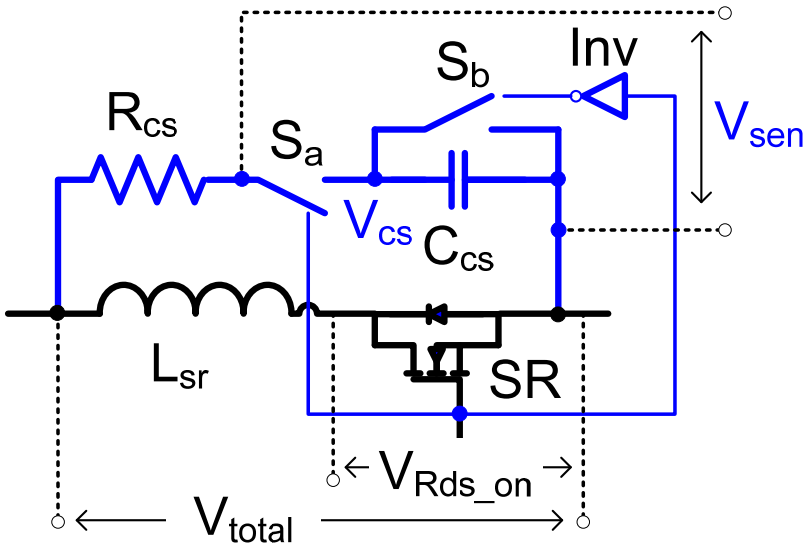
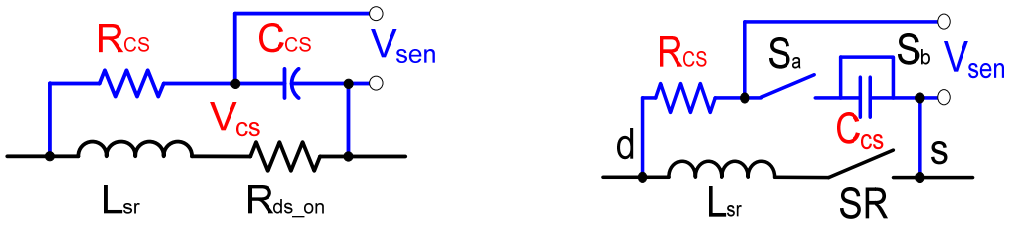


Fig. 2.15. Schematic of V_{ds} phase compensation network.

The detailed schematic of the active phase compensation network is illustrated in Fig. 2.15. R_{cs} and C_{cs} act as a passive network to generate compensated voltage. S_a and S_b are small-signal active switches used to reset the passive phase compensation network for each cycle. *Inv* represents an inverter. When the SR is turned on, the passive network operates to provide the emulated true resistive voltage of the SR. Once the current diminishes to zero, the SRs can be properly turned off. Due to the very high blocking resistance of SRs, the R_{ds_on} of SRs is modeled as piecewise linear resistance. Therefore, the active network of the proposed compensation scheme is designed to reset the passive network and to sustain the SRs' reverse voltage, which is utilized to determine the turn-on timing of the SRs. The equivalent circuits for the turn-on and turn-off periods are illustrated in Fig. 2.16. It should be noted that the package inductances of the MOSFET include drain inductance L_{sr_d} and source inductance L_{sr_s}, which are plotted in Fig. 2.14. After the SR is turned on, the passive network begins to

work. Thus, the drain inductance and source inductance can be considered as a lumped inductance without affecting operation mode analysis. After the SR is turned off, the passive network is in reset mode. S_a is off and S_b is on. C_{cs} is in shorted mode. The parasitic inductances can be ignored as well. Therefore, for the sake of simplicity, the drain inductance and source inductance are modeled as one lumped package inductance during the discussion below.



(a) Equivalent circuit when the SR is on.

(b) Equivalent circuit when the SR is off.

Fig. 2.16. Equivalent circuits for compensation network.

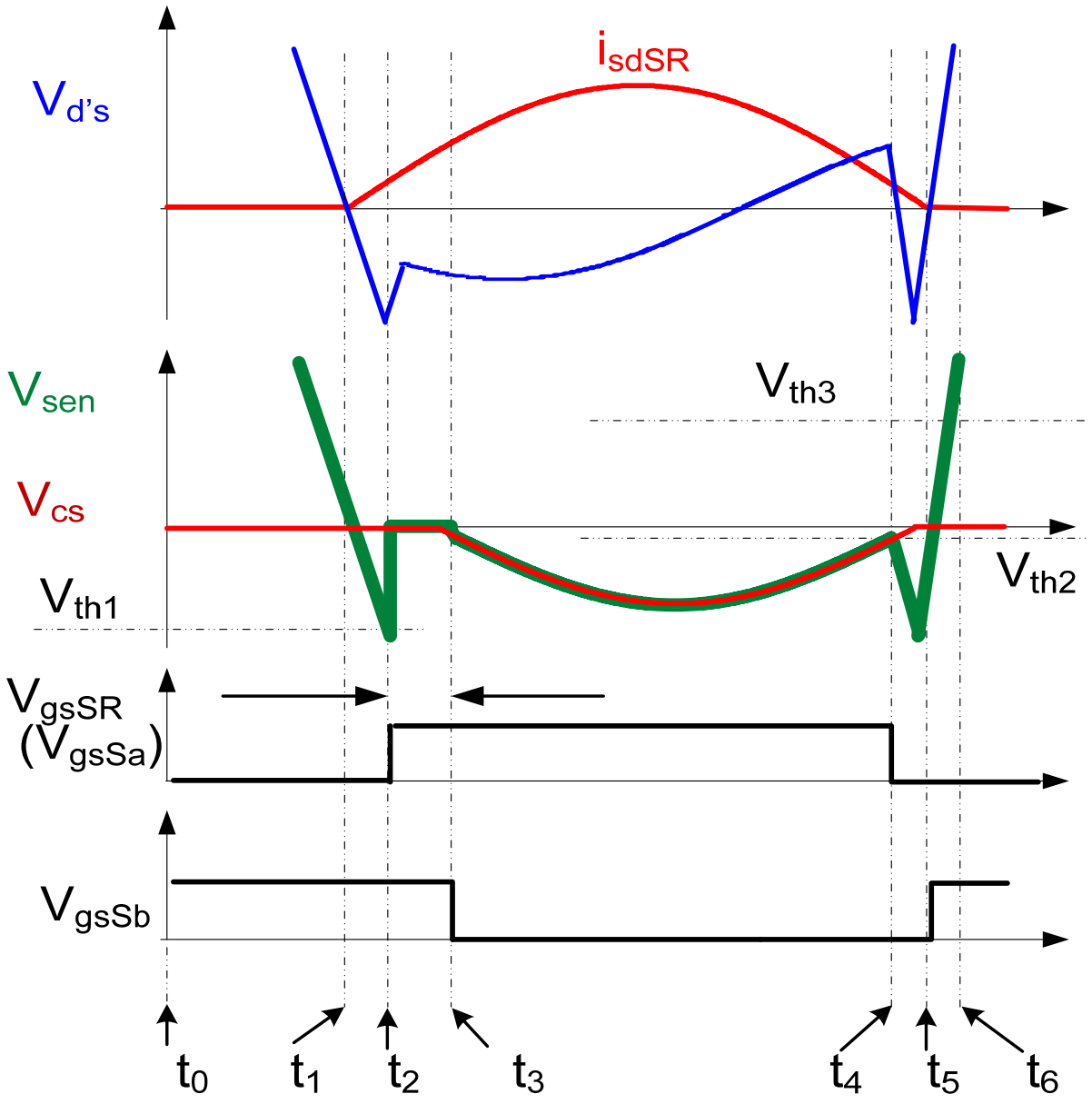


Fig. 2.17. Operation mode analysis for proposed driving scheme of SR in LLC resonant converter.

The operating process is as follows and plotted in Fig. 2.17.

[t_0-t_1]: Both the SR and S_a are off. S_b is on. Therefore, compensation capacitor C_{cs} is shorted. The voltage is zero on C_{cs}.

[t_1-t_2]: The primary side devices switch. Current begins to go through the body diode of the SR. The $V_{d's}$ of the SR becomes negative. During this period, the compensated voltage V_{cs} equals $V_{d's}$. Thus, V_{cs} also becomes negative. Once V_{cs} touches the threshold voltage V_{th2} at t_2, the SR can be turned on.

[t_2-t_3]: During this short period, S_a and S_b remain at the same status as during previous stage t_1-t_2. This guarantees the full turn-on of the SR and also eliminates the adverse effect of oscillation.

[t_3-t_4]: S_a is turned on and S_b is turned off. The passive compensation network begins to operate. The compensated V_{cs} follows the resistive voltage of the SR. V_{cs} can be applied to accurately control the SR conduction time. Meanwhile, $V_{d's}$ is out of phase of the resistive voltage of the SR due to the L_{sr}.

[t_4-t_5]: At t_4, the current of the SR drops close to zero. V_{cs} touches the threshold voltage V_{th1}. As a result, the SR can be turned off. Meanwhile, S_a is turned off and S_b is turned on. The passive compensation network is in reset mode. The active network takes the $V_{d's}$ of the SR.

[t_5-t_6]: The voltage drop on the SR changes from negative to positive potential. The driving circuit is blanked until the V_{cs} touches the V_{th3} at t_6. Similarly, this short period is meant to avoid the adverse effect of turn-off ringing.

[t_6-]: After t_6, SR remains off. The passive compensation network remains in reset mode.

To precisely capture the resistive voltage drop on the SRs during the turn-on period, the phase compensation network should be properly designed. The SR is modeled as an ideal switch in series with R_{ds_on} and L_{sr}. V_{total} is the terminal voltage of $V_{d's}$. V_{Rds_on} is the actual resistive voltage of the SR's V_{ds}. V_{cs} is the compensated voltage for the SR driving scheme. Assuming the current going through the SR is i_{sdSR}, the Laplace transformation expressions of their time domain expressions can be represented as $v_{Rds\_on}(s)$, $v_{cs}(s)$ and $i_{sdSR}(s)$, respectively. In accordance with the circuit described in Fig. 2.16, $v_{cs}(s)$ is derived in (2.13). The passive compensation network is designed to satisfy (2.14), while the active switches are set to satisfy (2.15) for the initial conditions of every cycle. Thus, (2.16) is derived. Based on the inverse Laplace transformation of (2.16), $v_{Rds\_on}(t)=v_{cs}(t)$ is obtained. As a result, the compensation network can precisely represent the voltage of the SR's on-resistance. It should be noted that (2.13), (2.15) and (2.16) are valid for every cycle in which the SRs are on.

$$v_{cs}(s) = -\frac{i_{sdSR}(s) \cdot R_{ds\_on} \cdot (1 + s \cdot L_{sr} / R_{ds\_on})}{1 + s \cdot R_{cs} \cdot C_{cs}} \tag{2.13}$$

$$R_{cs} \cdot C_{cs} = \frac{L_{sr}}{R_{ds\_on}} \tag{2.14}$$

$$v_{cs}(0^-) = v_{Rds\_on}(0^-) \tag{2.15}$$

$$v_{cs}(s) = i_{sdSR}(s) \cdot R_{ds\_on} = v_{Rds\_on}(s) \tag{2.16}$$

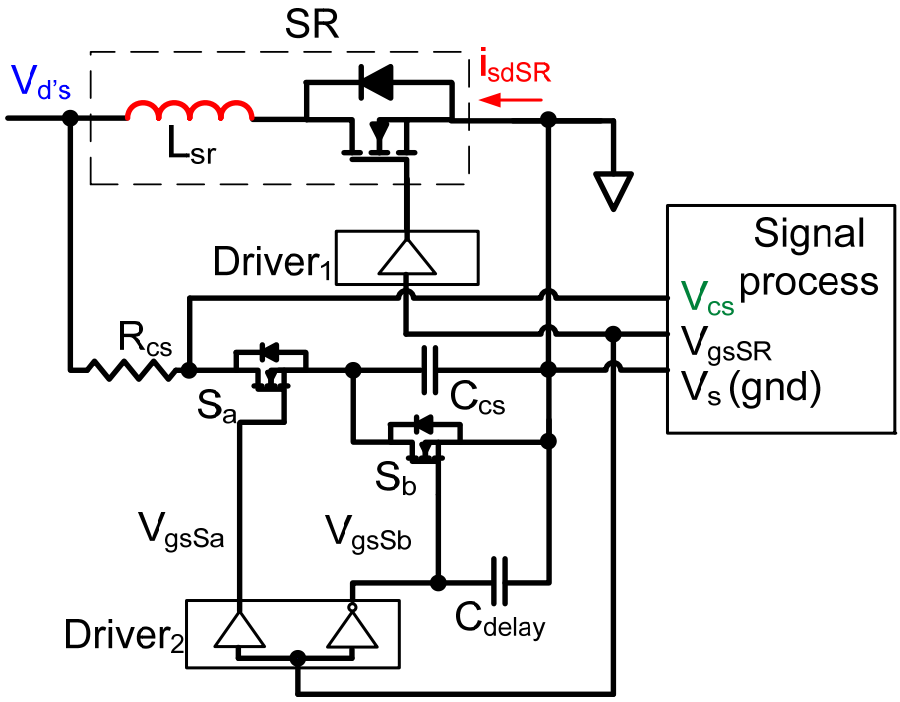


Fig. 2.18. Implementation of proposed compensation driving scheme.

Theoretically, V_{cs} closely follows V_{Rds_on}. They are identical in phase and amplitude. In practice, there are parasitic capacitances, such as the junction capacitances of the MOSFETs. When the SR is off, the drain-to-source capacitance of the SR is in parallel with the whole compensation network. During this period, only the active compensation network operates. The compensated voltage V_{cs} represents the drain-to-source voltage of the SR. Thus the junction capacitance of the SR will not affect the compensation network. When the SR is on, the SR has very low resistance, and the junction capacitances can be ignored. As a result, the effect of junction capacitances on the

compensation network can be neglected. On the other hand, S_a and S_b introduce small package inductances and on-resistances. A compensation passive network can be easily designed with a large R_{cs}. Thus, the impedance of R_{cs} is several orders of magnitude larger than the package inductance and on-resistance impedances of S_a and S_b. As a result, these parasitics can be ignored.

The implementation of the proposed novel driving scheme of the SR for LLC resonant converters is illustrated in Fig. 2.18. $Driver_1$ and $Driver_2$ are the drivers for the switches. A capacitor C_{delay} is placed in parallel with S_b to generate a short delay time. It should be noted that the signal processor includes a zero-voltage detector and logic gate circuits. The signal processor can be built with discrete components or ICs. A commercial IC, such as the IR1167, can be applied as a signal processor. $V_{d's}$ is the voltage drop on the drain-to-source of the SR, and i_{sdSR} is the SR current. V_{gsSR}, V_{gsSa} and V_{gsSa} are the gate-source voltages of the SR, S_a and S_b, respectively.

2.3.2 Experimental Results

B. Lu's 1MHz, 1kW, 400V-48V LLC converter with diode rectifiers is the benchmark used for comparison. The LLC resonant tank design parameters are: $L_r=1\mu H$, $C_r=25nF$, and $L_m=12\mu H$. Due to reverse recovery problems, the primary side resonant tank current exhibits glitches at the switch transition time. The reverse-recovery rings also generate voltage overshoots on the diode.

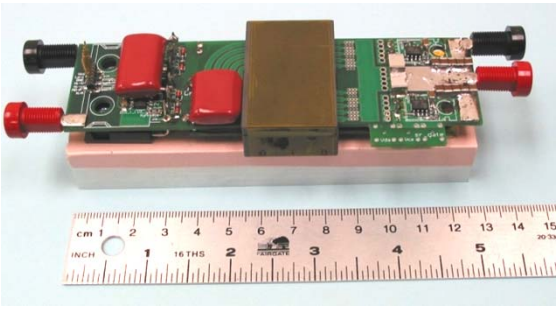


Fig. 2.19. The prototype of a 1MHz 1kW 400V-48V LLC resonant converter with SRs.

A 1MHz, 1kW, 400V-48V prototype, shown in Fig. 2.19, is built to verify the proposed improved SR driving scheme for LLC resonant converters. The L_m is chosen to be 13μH. The resonant inductor L_r is 0.9μH, and the resonant capacitor is chosen to be 21nF. The transformer turns ratio is 4.

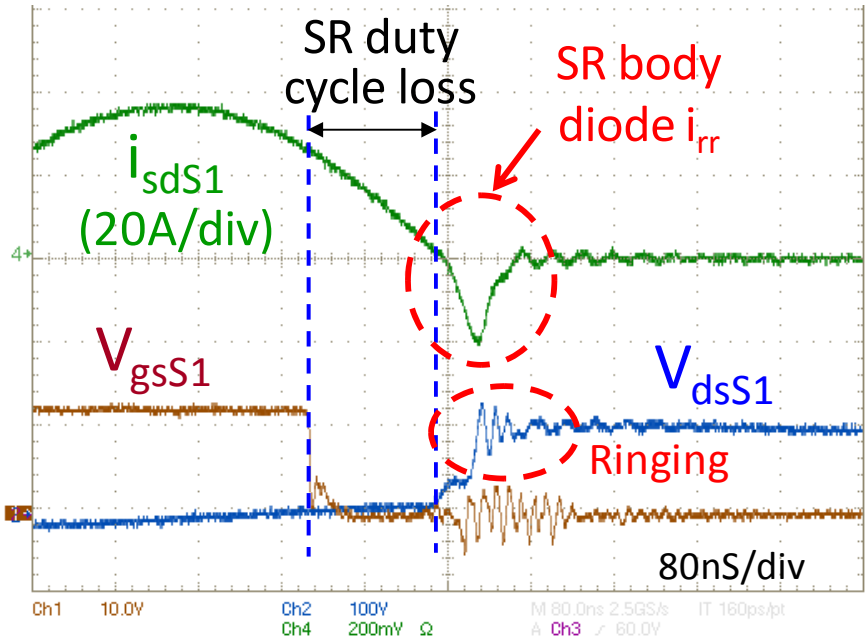


Fig. 2.20. For conventional SR driver, SR body diode reverse-recovery current due to SR duty cycle loss.

With the proposed SR driving method, turn-off duty cycle losses of the SR driving signals are compensated. The waveform is shown in Fig. 2.22. Based on the proposed driving method, i_{rr} is also measured and shown in Fig. 2.21. The reverse-recovery current is considerably reduced to almost zero. Due to the great reduction of the SR body diode conduction time, the reverse recovery problems of the SR body diode at high frequency are eliminated.

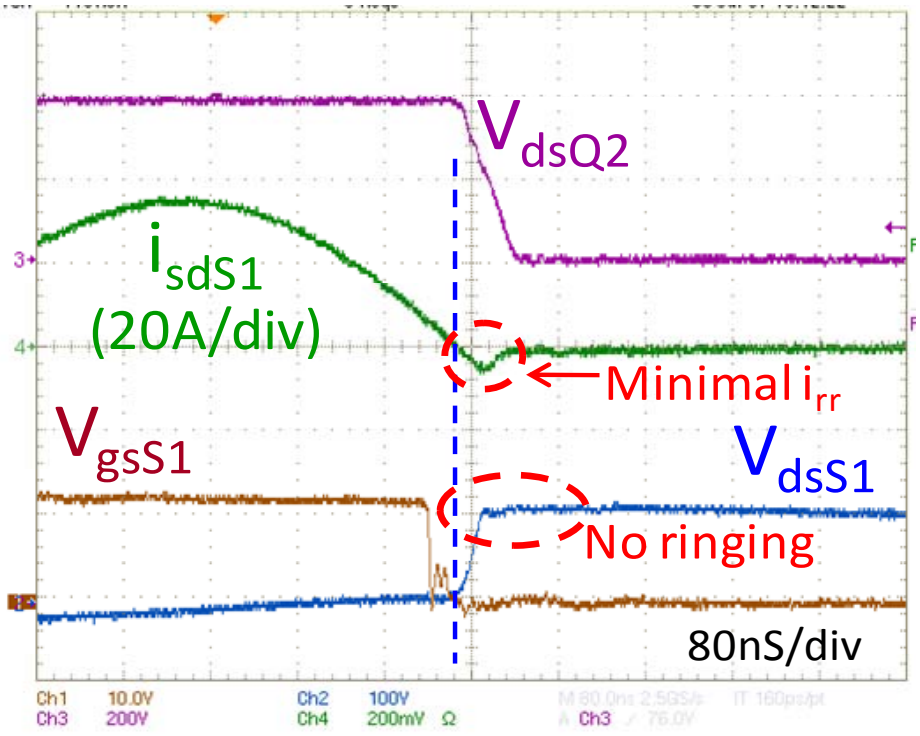


Fig. 2.21. Achieved zero reverse-recovery current & no duty cycle loss by proposed driving scheme.

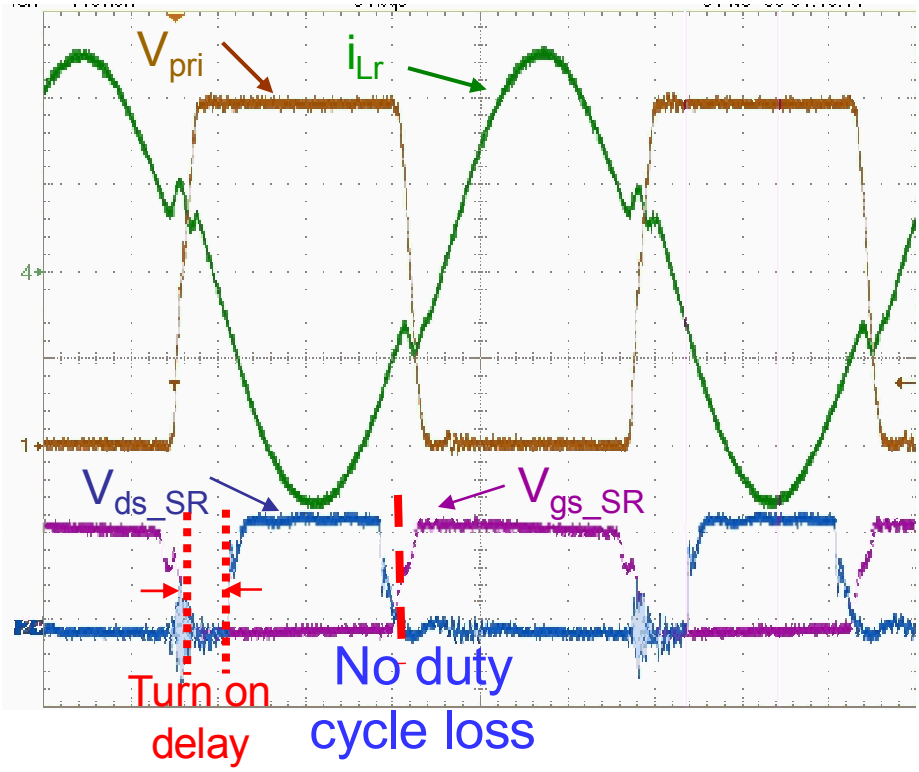


Fig. 2.22. Waveforms of SR with proposed driving scheme.

The waveforms of the SR for a LLC resonant converter without a compensation network are shown in Fig. 2.20. The SR duty cycle loss is clearly shown, and it matches the derived analytical result. Due to a long body diode conduction time, the reverse-recovery current of the SR body diode is pronounced. The reverse-recovery current i_{rr} is measured. Both the conduction loss and switching loss of the SR body diode compromise efficiency. Consequently, only one percent efficiency improvement is obtained over the Schottky diode rectifier.

2.3.3 Further Discussion and Improvement for Practical Applications

To apply the proposed SR driving scheme into practice, several practical non-idealities should be considered.

Normally, the propagation delay of driving circuits is short, and it can be ignored in some circuit designs. However, for high-frequency converters, the propagation delay may affect the circuit operation. Hence, careful study is required.

Following the compensation network design procedure, the SR driving signal is almost ideal. However, due to the unavoidable propagation delay of driving circuits, the SR will be turned off later than is ideal. Consequently, the SRs are turned off after zero current is reached. The reverse current may be generated if the propagation delay time is considerably long.

To overcome the turn-off propagation delay problem, the compensation network can be adjusted to offset the short turn-off propagation delay period, t_{offd}. Thus, the passive network of R_{cs} and C_{cs} can be adjusted to offset the turn-off propagation delay. β is defined as the adjustment factor in (2.17). Without consideration of t_{offd}, the ideal compensation period t_o is calculated in (2.18). In (2.18), the first item in the numerator is related to the compensation time or phase due to L_{sr}. The second item in the numerator is related to the compensation time or phase due to V_{th1}. When considering t_{offd}, the actual required compensation period should be less. It is adjusted by β and is derived in (2.19). Solving (2.19) leads to the solution for β, which is derived in (2.20). As a result, the turn-off delay can be accommodated. Even for MHz-range converters,

very high–speed, costly driving circuits are not necessary. This is another benefit of the proposed improved driving scheme.

$$\beta = \frac{R_{cs} \cdot C_{cs}}{L_{sr} / R_{ds\_on}} \tag{2.17}$$

$$t_\theta = \left[a\tan\left(\frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right) + a\sin\left(\frac{-V_{th1}}{\frac{\pi}{2} I_o \cdot R_{ds\_on} \cdot \left|1 + j \cdot \frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right|}\right)\right] \Big/ 2\pi f_s \tag{2.18}$$

$$t_\theta - t_{offd} = \left[a\tan\left(\beta\frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right) + a\sin\left(\frac{-V_{th1}}{\frac{\pi}{2} I_o \cdot R_{ds\_on} \cdot \left|1 + j \cdot \beta\frac{2\pi f_s L_{sr}}{R_{ds\_on}}\right|}\right)\right] \Big/ 2\pi f_s \tag{2.19}$$

$$\beta = \frac{V_{th1} - \frac{\pi}{2} I_o R_{ds\_on} \sin(2\pi f_s t_\theta - 2\pi f_s t_{offd})}{\left[1 - \sin(2\pi f_s t_\theta - 2\pi f_s t_{offd})^2\right] \cdot L_{sr} 2\pi f_s I_o \pi / 2} \cdot \cos(2\pi f_s t_\theta - 2\pi f_s t_{offd}) \tag{2.20}$$

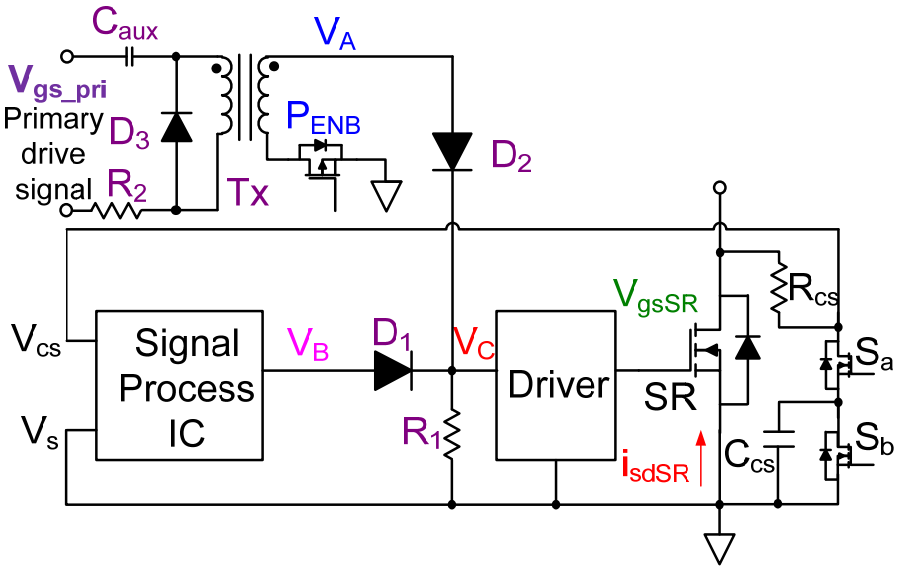


Fig. 2.23. Turn-on compensation circuit.

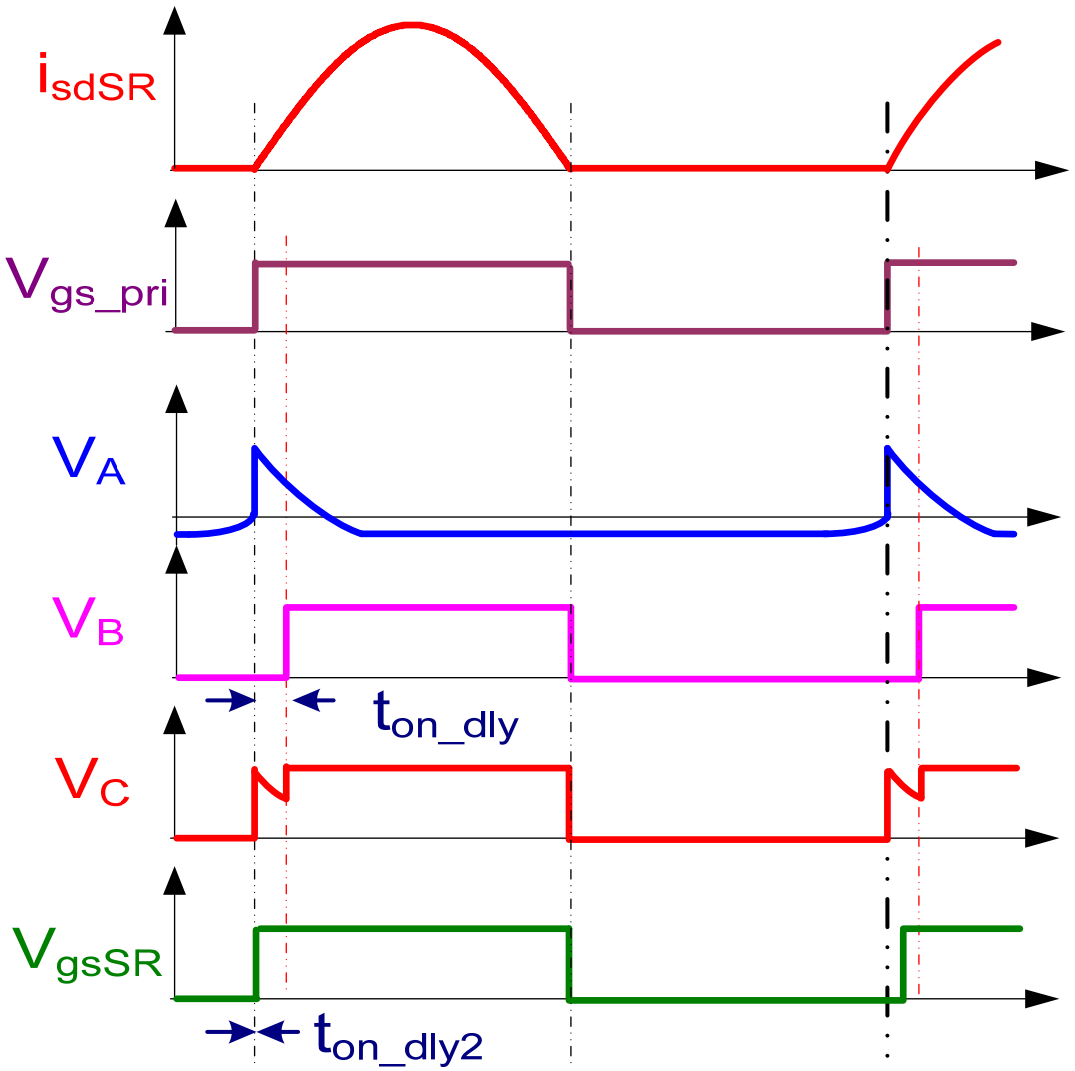


Fig. 2.24. Turn-on compensation circuit operation analysis.

For SR driving circuits, turn-on propagation delay always occurs. The same happens with the SR driving scheme discussed here. With state-of-the-art integrated circuit technology, the propagation delay of a discrete driver can be as small as 10-20ns, but the propagation delay of the sensed V_{ds} processing circuit is still in the range of tens of ns. One reason for the large propagation delay from the V_{ds} processing circuit is the

large gain needed for window comparators. Shown in Fig. 2.22, the total SR turn-on delay time at the turn-on edge on a 1kW, 1MHz, LLC prototype is 75nS due to the turn-on propagation delay t_{on_dly} in the driving circuit.

According to the above discussion, the turn-off propagation delay can be compensated. However, the turn-off compensation network discussed above barely affects the turn-on propagation delay, as shown in Fig. 2.22. As a result, the SR duty cycle loss due to the turn-on propagation delay still exists.

A turn-on propagation delay compensation circuit, shown in Fig. 2.23, is proposed to solve the problems of turn-on duty cycle loss [D.37]. Based on the characteristics of LLC resonant converters, the turn-on edge of the primary side switches, V_{gs_pri}, is in phase with the turn-on edge of the SR, V_{gsSR}. Therefore, the primary side turn-on signal is utilized to synchronize the SR turn-on timing. The detailed operation principle is illustrated in Fig. 2.24. When the primary switch turns on, a small pulse signal, V_A, can be generated and delivered to the SR driving circuits. This small pulse-driving signal compensates the turn-on delay time. Thus, the driving signal is reshaped and virtually no turn-on delay exists. V_A also represents the secondary side winding voltage of *Tx*. After the positive pulse, V_A becomes negative due to the forward voltage drop of D_3. During the rest of the switching period, which is much longer than the positive pulse, *Tx* is reset. The damping resistor R_2 may or may not be necessary.

Particularly during startup, when the operating frequency is far beyond the LLC tank resonant frequency, the primary side and SR turn-on timings are not synchronized.

When this occurs the turn-on compensation circuit will be disabled by a P-MOSFET P_{ENB}.

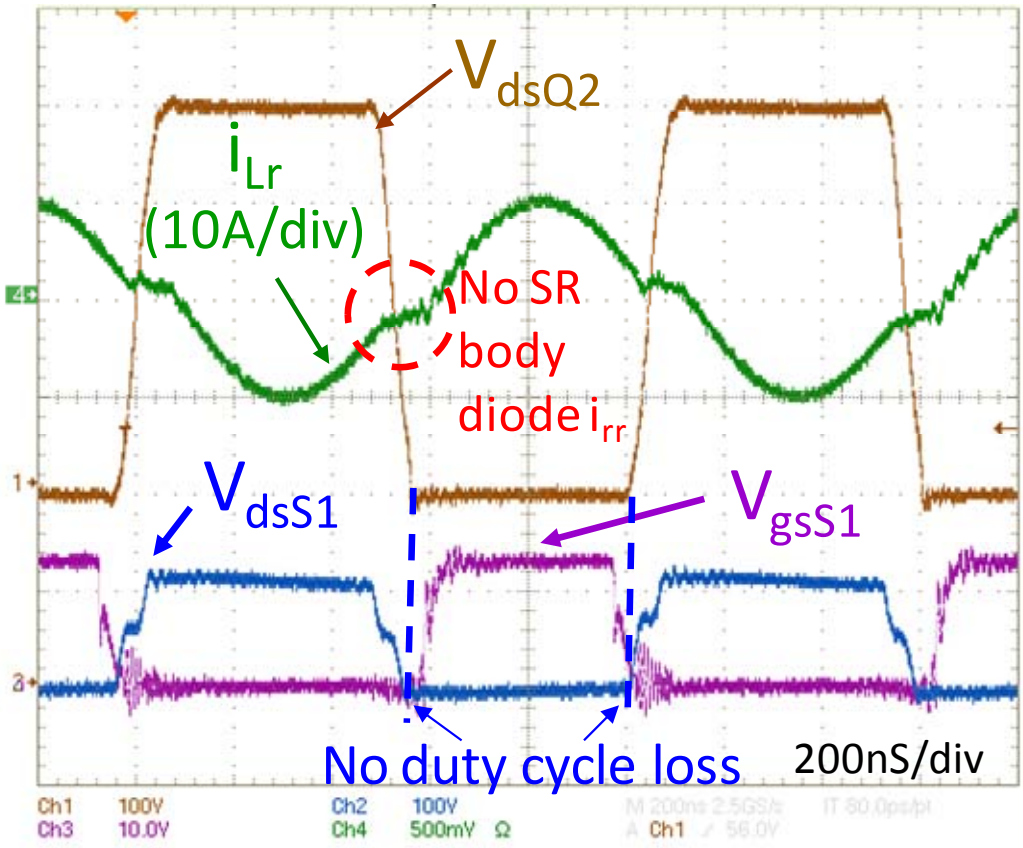


Fig. 2.25. Waveforms of SR with proposed driving scheme.

Finally, the proposed turn-on timing compensation circuit is verified experimentally. The result is shown in Fig. 2.25. 0.1% efficiency increase can be achieved.

In summary, with the proposed driving circuit, the SR can be finally driven in almost ideal mode. There is virtually no turn-on or turn-off duty cycle loss. The proposed driving scheme can be easily extended to other resonant topologies and some PWM circuits.

For 1kW, 1MHz, 400V/48V LLC converters, with a great improvement for both conduction loss and switching loss, 95.9% efficiency can be achieved at full load. The overall efficiency is above 95.3% for the 20%-100% load range. The efficiency curves for different load conditions are drawn in Fig. 2.26. The efficiency of the LLC resonant converter with MBR20200 Si Schottky diodes is also plotted in Fig. 2.26 for comparison.

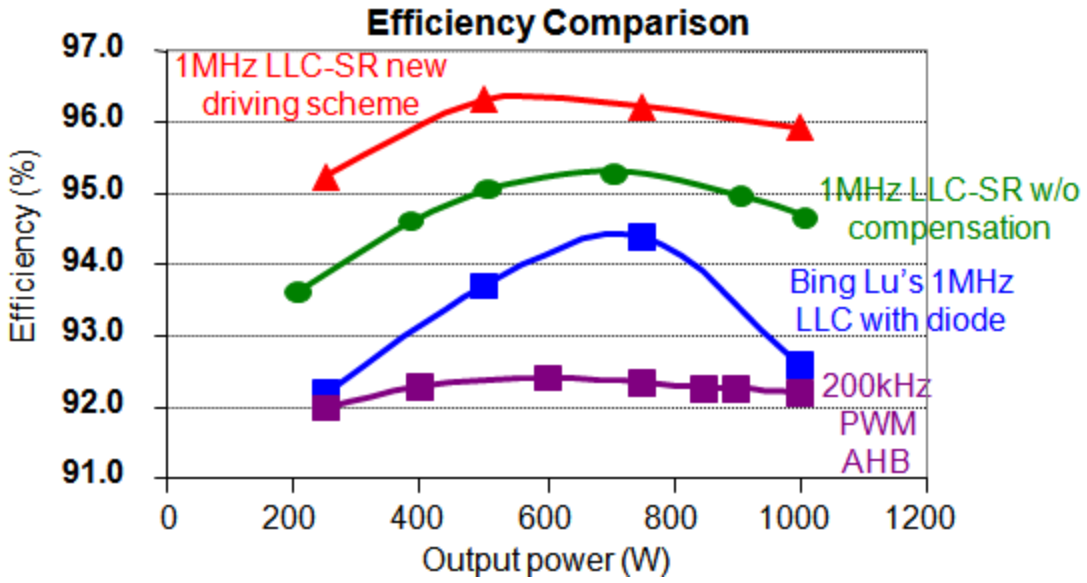
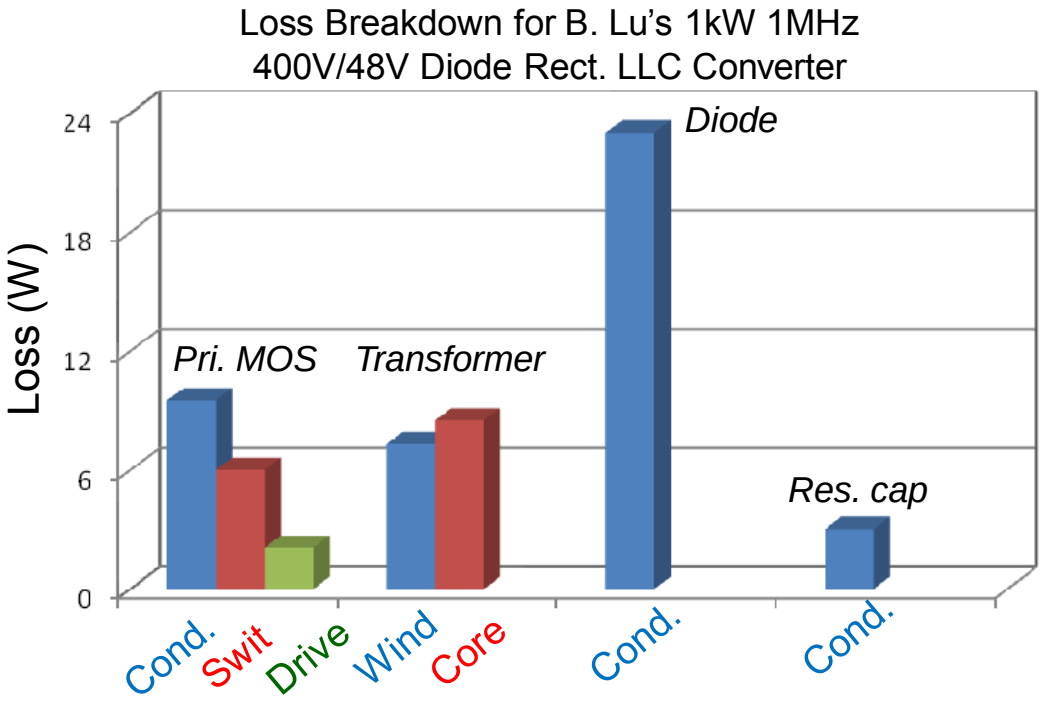


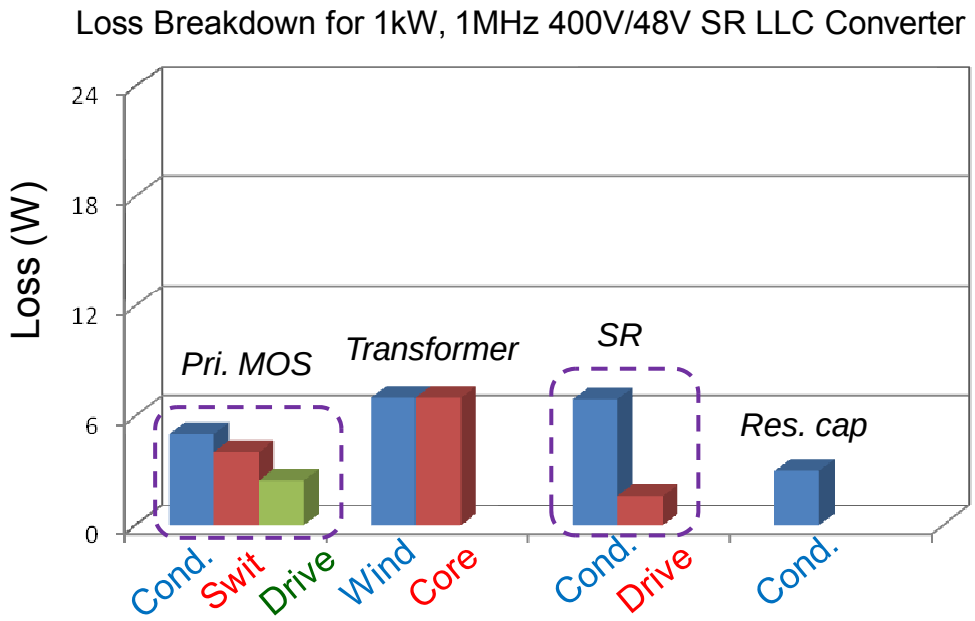
Fig. 2.26. Efficiency comparison of 1kW 1MHz 400V/48V LLC converters with diodes and with SR based on the proposed driving scheme.

For 1kW, 1MHz, 400V/48V LLC converters, the power density has been increased from 76W/in^3 to 96W/in^3 due to lower total losses.

The loss breakdown comparison of B. Lu's LLC resonant converter and the proposed optimal LLC resonant converter are illustrated in Fig. 2.27.



(a) Loss breakdown of B. Lu's 1kW 1MHz 400V/48V LLC resonant converter with diode rectifiers.



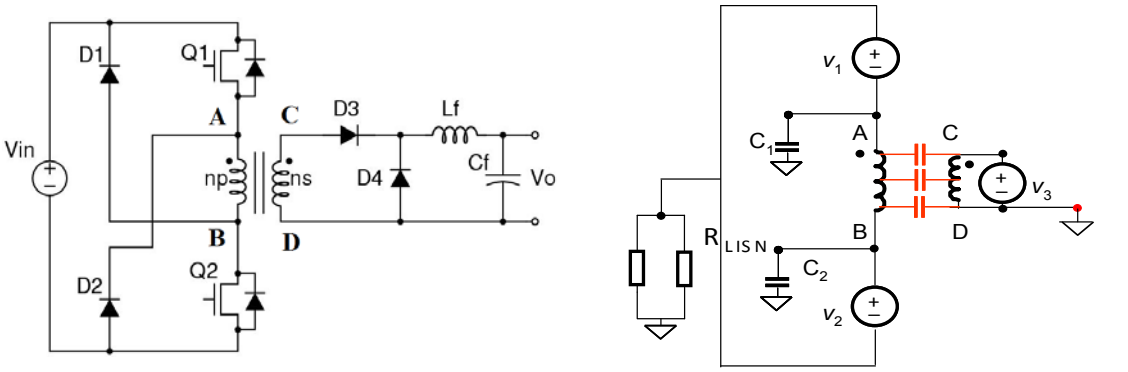
(b) Loss breakdown of improved 1kW 1MHz 400V/48V LLC resonant converter with SR.

Fig. 2.27. Loss breakdown comparison for B. Lu's LLC resonant converter and the proposed optimal LLC resonant converter.

2.4 Introduction of EMI Issues

Front-end converters are required to meet EMI standards.

In [F.1], P. Kong analyzed the CM EMI performance of two-switch forward converters. Two-switch forward converters are symmetric on the primary side. P. Kong proposed applying the symmetry concept to reduce CM noise. The concept and the noise reduction results reported by P. Kong are shown in Fig. 2.29.

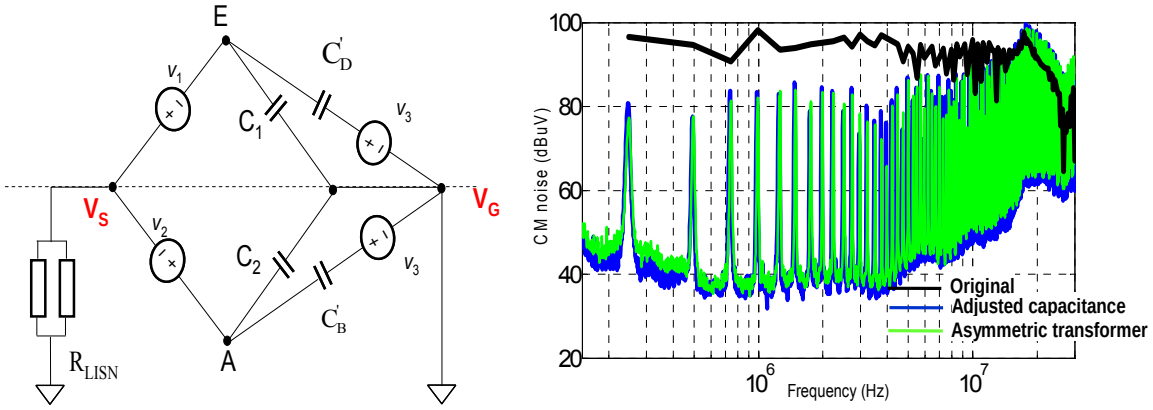


(a) Two-switch forward converter

(b) CM noise model of two-switch forward converter

Fig. 2.28. P. Kong's CM noise model of two-switch forward converter.

In [F.2], the EMI performance of phase-shift full-bridge converters was analyzed. In this paper, the CM noise model was provided, it is illustrated here in Fig. 2.30. The simulated EMI spectrum matches the measurement very well. However, this model is very complicated. The EMI spectrum can only be obtained with dedicated simulation software. The CM noise spectrum of phase-shift full-bridge converters are shown in Fig. 2.31.



(a) CM noise is canceled with symmetry concept.

(b) CM noise reduction with application of symmetry concept

Fig. 2.29. P. Kong's CM noise reduction with symmetry concept.

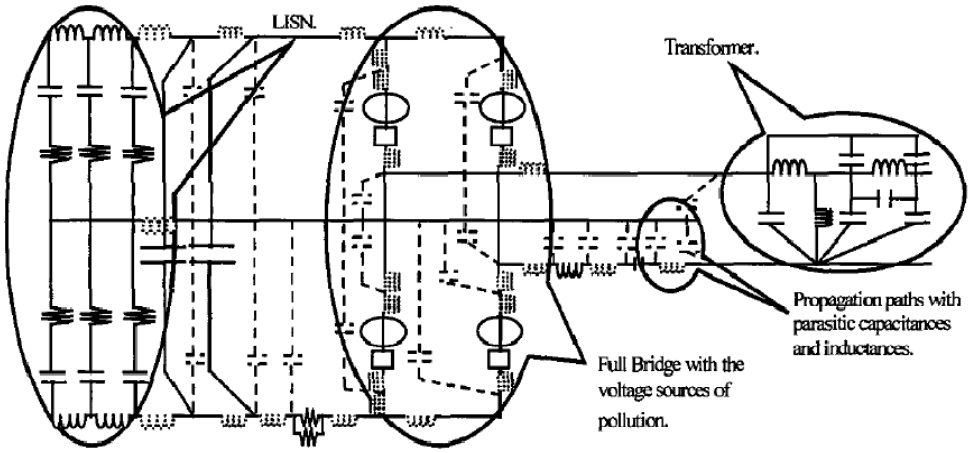


Fig. 2.30. CM noise model of phase-shift full-bridge converters.

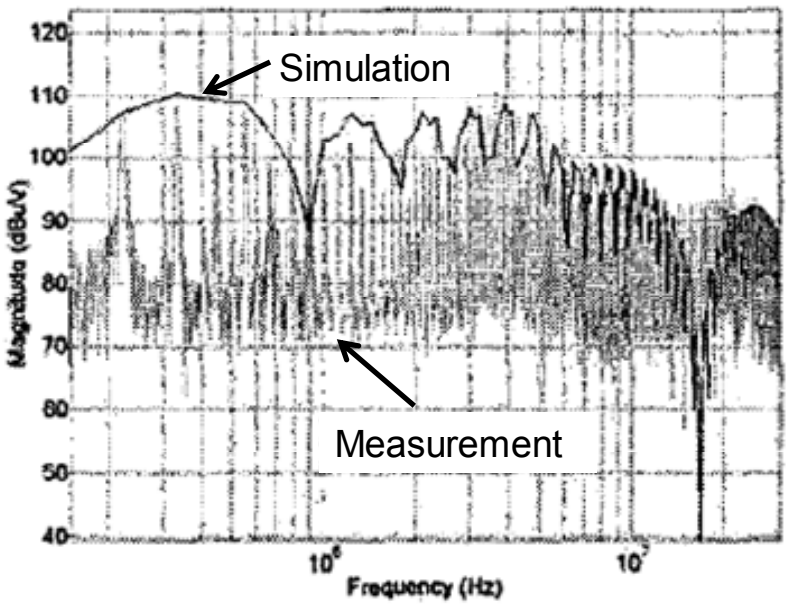


Fig. 2.31. CM noise spectrum of phase-shift full-bridge converters.

The measured EMI noise spectrum of LLC resonant converters is shown in Fig. 1.35. The EN55022 Class B EMI limits are also plotted. Apparently, the EMI noise of LLC resonant converters is far beyond the EMI standard. Thus, the EMI reduction approaches are very critical. Due to asymmetrical primary side structure, CM noise cancelation cannot be performed easily with the symmetry concept.

However, very little of the literature addresses the EMI issues of LLC resonant converters. To meet the EMI standard, it is very important to achieve low EMI noise. Hence, it is critical to identify and improve the EMI of LLC dc-dc converters.

The mechanism of conducted EMI emissions of LLC resonant dc-dc converters is not clear and should be studied thoroughly. The DM and CM EMI noise models for LLC resonant converters are needed, and the switching frequency's impact on the EMI emissions of LLC resonant converters should be identified.

2.5 EMI Model of LLC Resonant Converters

This section identifies different noise sources in LLC resonant converters and analyzes their propagation paths and effects on total DM and CM noise.

The front-end converter includes the EMI filter, diode bridge, PFC circuit and dc-dc converter. Normally, a single-switch continuous-current-mode (CCM) boost converter acts as the PFC stage for kW-range front-end converters. In this paper, the LLC resonant converter acts as the dc-dc stage. Between the PFC and the dc-dc converter, there are bulk (hold-up time) capacitors. During the hold-up time (one ac line cycle), these hold-up time capacitors should provide full energy to the dc-dc converter. At 1kW power level, the typical capacitance range is 440μF ~ 1000 μF. In this chapter, a 1kW, 1MHz, 400V/48V LLC resonant converter is analyzed. The derived result can be extended to other circuits.

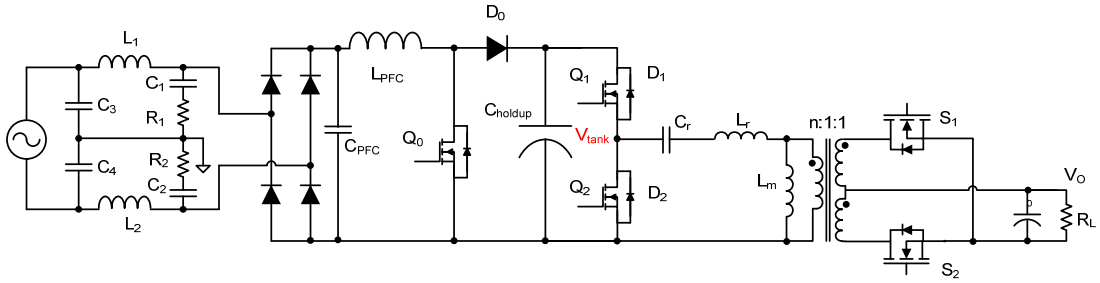


Fig. 2.32. The front-end ac-dc converter with LISN.

Line impedance stabilize networks (LISN) are the standard EMI measurement equipment, and can detect EMI noise through the LISN resistors. The structure of a front-end converter connected with an LISN is shown in Fig. 2.32. Here the EMI filter is not loaded. Because LISN inductors and capacitors act as a high-pass filter, most of

the EMI noise current goes through LISN resistors R_1 and R_2 (both are 50 Ω). Since the CCM PFC circuit is adopted, the input diode bridge can be ignored in the noise path. Here, the MOSFET branch of the PFC circuit is modeled as a voltage source, and the switching diode of the PFC circuit is modeled as a current source. The LLC resonant converter is modeled as a current source. For the LLC resonant converter, the DM current-transferring path includes the LLC switches, PFC diode, PFC inductor, LISN capacitors C_1, C_2 and LISN resistors R_1 and R_2. The equivalent circuit of the DM noise path is depicted in Fig. 2.33.

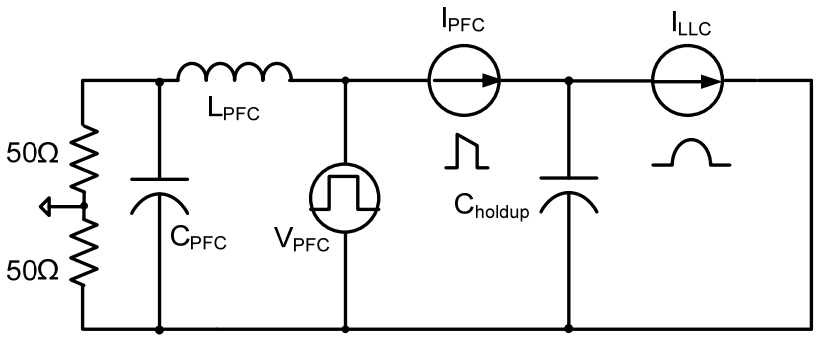


Fig. 2.33. DM equivalent circuit of LLC resonant converters.

Due to PFC input capacitor, C_{PFC}, PFC inductanor, L_{PFC} and bulk capacitor C_{holdup}, DM noise of LLC resonant converters is attenuated considerably when the signal reaches the LISN. Consequently, DM noise is not a problem for LLC resonant dc-dc converters in front-end converters. Hence, CM noise is the dominant part of the total EMI emissions, and should be studied thoroughly.

In general, at the nominal condition, it is preferred for the LLC resonant converter to operate close to the resonant frequency to achieve the highest efficiency. The

waveforms of the LLC resonant converter are plotted in Fig. 2.34. It can be observed that the voltage source V_{SR1} is in phase with V_{tank}. Voltage source V_{SR2} is out of phase with V_{SR1}.

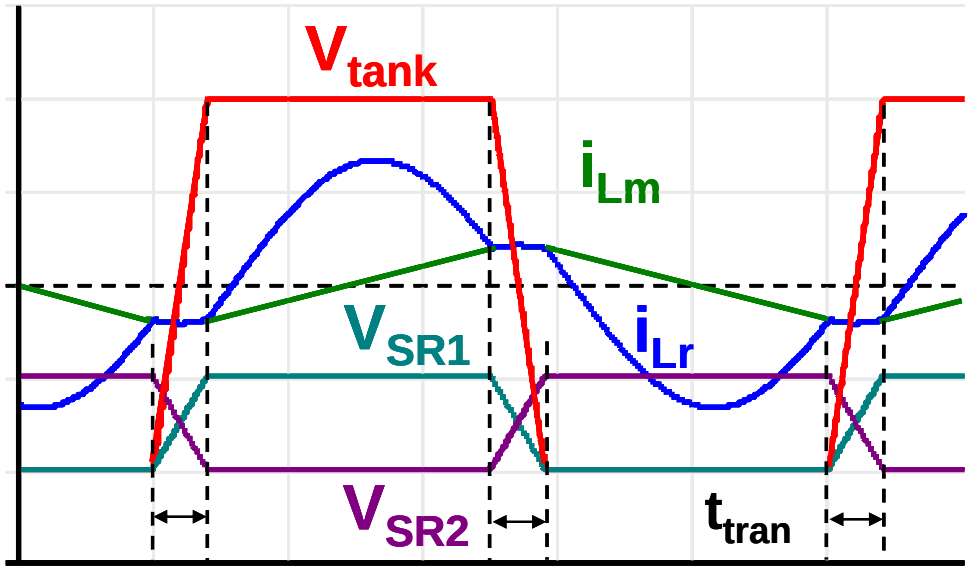


Fig. 2.34. Typical waveforms of LLC resonant covnerters.

To address the CM noise model of LLC resonant converters, the parasitics of the transformer should be studied. In this application, planar transformer is widely applied. Particularly, magnetic integration techniques are widely adopted for LLC resonant converters. Leakage inductance and magnetizing inductance can be designed and utilized as resonant inductances. In this paper, magnetic integration is applied so that all the magnetic components are integrated into one unit. There are 4 turns for the primary side winding. The center tap structure is used for the secondary side rectifiers. There is 1 turn for each secondary side winding.

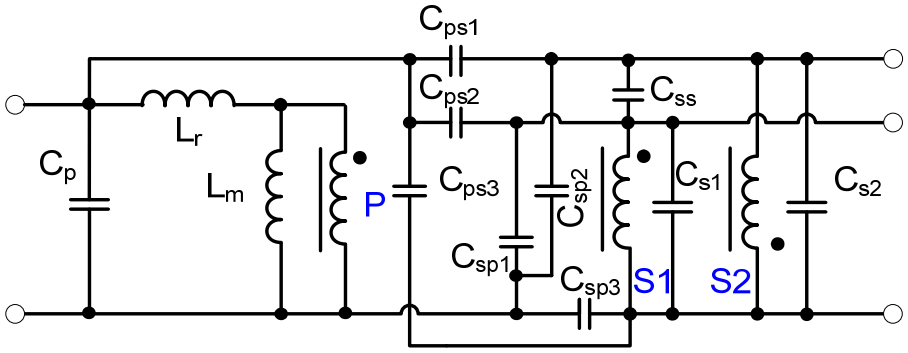


Fig. 2.35. The lumped model of the transformer for LLC resonant converters.

The lumped model of the transformer is illustrated in Fig. 2.35. *P* represents the primary side winding. S_1 and S_2 represent secondary side windings, and L_m represents the magnetizing inductance. C_p, C_{s1} and C_{s2} are modeled as the self-capacitance of the primary side winding and the secondary side windings respectively. C_{ss} represents the mutual capacitance of the secondary side windings. C_{ps1}, C_{ps2}, C_{ps3}, C_{sp1}, C_{sp2} and C_{sp3} are modeled as mutual capacitances between the primary side winding and the secondary side windings.

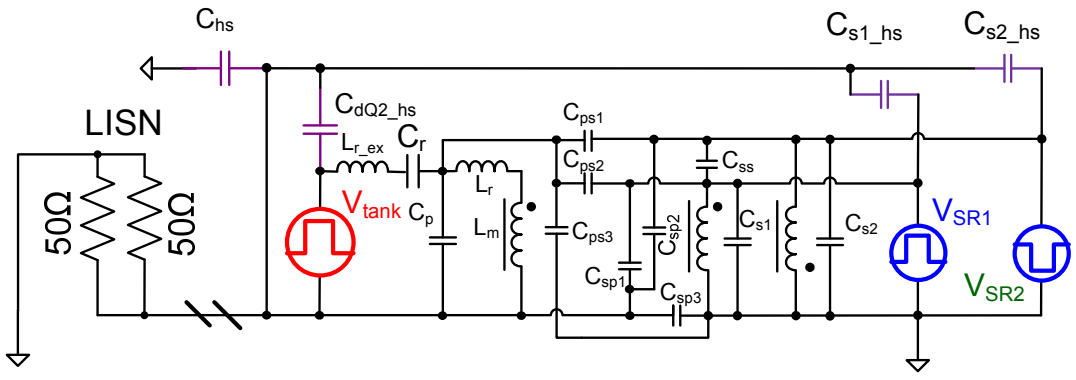


Fig. 2.36. CM noise model of LLC resonant converters.

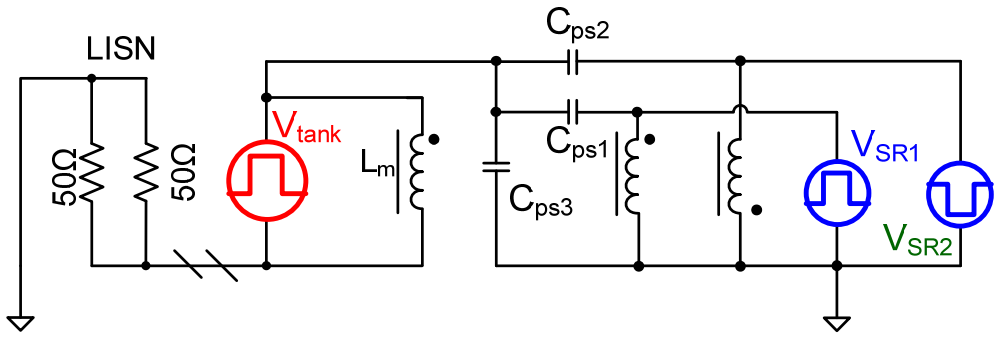
The CM noise model of LLC resonant converters is shown in Fig. 2.36. The middle point of the primary side bridge leg is modeled as the noise voltage source V_{tank}. The SR branches of the secondary side represent noise voltage sources V_{SR1} and V_{SR2}. C_{dQ2_hs}, C_{S1_hs} and C_{S2_hs} represent the capacitive coupling of primary side MOSFET Q_2, the secondary side SR_1, and SR_1 to the heat sink, respectively. C_{hs} is modeled as the stray capacitance between the heat sink and the ground. To reduce the effect of C_{dQ2_hs}, the heat sink is connected with the negative terminal of the input voltage. This method is also widely applied for dc-dc converters for commercial products.

The CM noise model, which is shown in Fig. 2.36, is highly complicated. It is very difficult to capture the dominant factor of the CM noise. As a result, the CM noise model should be simplified to provide greater physical insight into the actual CM noise coupling mechanisms.

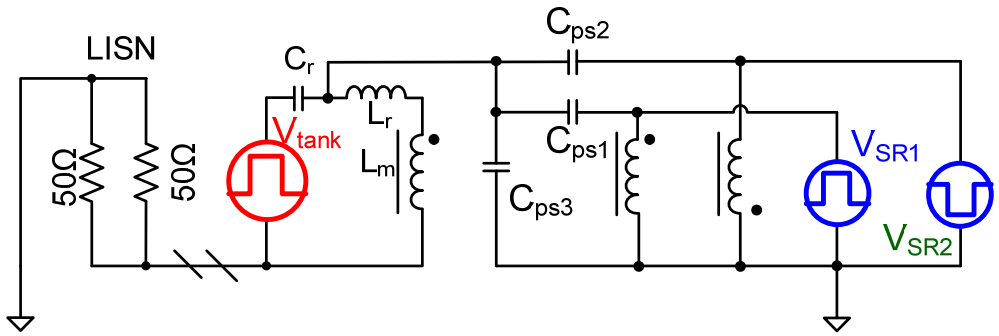
First of all, as mentioned above, the heat sink is connected with the negative terminal of the input voltage. The displacement current circulates in the noise source V_{tank}. As a result, the CM noise coupling of C_{dQ2_hs} can be ignored. For the same reason, C_p, C_{s1}, C_{s2} and C_{ss} are not included in the simplified model. In general, for front-end converters, EMI filters with CM capacitors (or Y capacitors) are adopted. Thus, the negative terminal of the input voltage is considered as a stable voltage level with low impedance to the ground in terms of EMI. Therefore, stray capacitance C_{sp3}, which is connected with two stable points, can be ignored. Secondly, CM currents coupled by C_{sp1} and C_{sp2} go through the LISN resistors. However, these currents are induced by V_{SR1} and V_{SR1}. Actually, V_{SR1} and V_{SR2} are signals with the same magnitude that are 180°

out of phase. The coupled CM currents are canceled. Therefore, in sake of simplicity, it is assumed that C_{sp1} equals C_{sp2} and can be ignored. However, it should be carefully noted that C_{sp1} and C_{sp2} may not be the same value. For instance, if the layout of the secondary side windings is unsymmetrical, the difference between C_{sp1} and C_{sp2} may be very pronounced. Thus, they may not be ignored. Thirdly, the resonant inductor can be constructed as a discrete inductor or an integrated inductor. If a discrete inductor is selected, the leakage inductance may be ignored. At the resonant frequency, the sum of the voltage drops on the resonant inductor and on the resonant capacitor is very close to zero due to series resonance. Hence, the EMI model can be simplified as Fig. 2.37(a). If an integrated inductor is adopted, it is preferable for the resonant inductance to be small, and for the resonant capacitance C_r to be much larger than the parasitic capacitance. Hence, for EMI analysis, the effect of C_r is negligible at high frequencies. For the low-frequency range, the *dv/dt* of V_{tank} is much higher than the *dv/dt* of a large resonant capacitor. Hence, assuming a large C_r is chosen, the effect of C_r is negligible for EMI analysis. The EMI model can be simplified as Fig. 2.37(c).

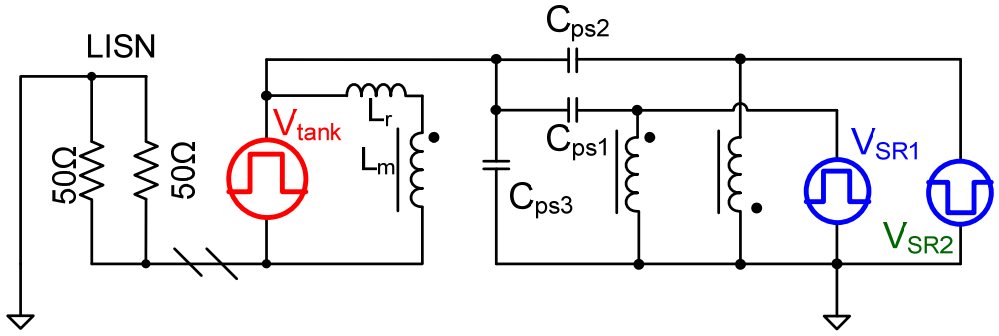
Finally, the simplified CM noise model of LLC resonant converters is derived and illustrated in Fig. 2.37. The figure clearly shows that the inter-winding capacitances C_{ps1}, C_{ps2}, and C_{ps3} are the dominating parasitic capacitances, which contribute to the CM noise.



(a) Lr constructed with discrete resonant inductor ignoring the leakage inductance.



(b) Lr constructed with integrated resonant inductor.



(c) Further simplified CM noise model for integrated resonant inductor ignoring the *dv/dt* effect of the resonant capacitor.

Fig. 2.37. Simplified CM noise model of LLC resonant converters.

According to the derived CM noise model of LLC resonant converters, EMI performance can be predicted. The CM noise currents are induced by V_{tank}, V_{SR1} and V_{SR2}. Based on the superposition theory, the CM currents induced by V_{SR1} and V_{SR2} can be canceled because C_{ps1} equals C_{ps2}. As a result, the CM current, which go through LISN resistors, is determined by *dv/dt* of V_{tank}.

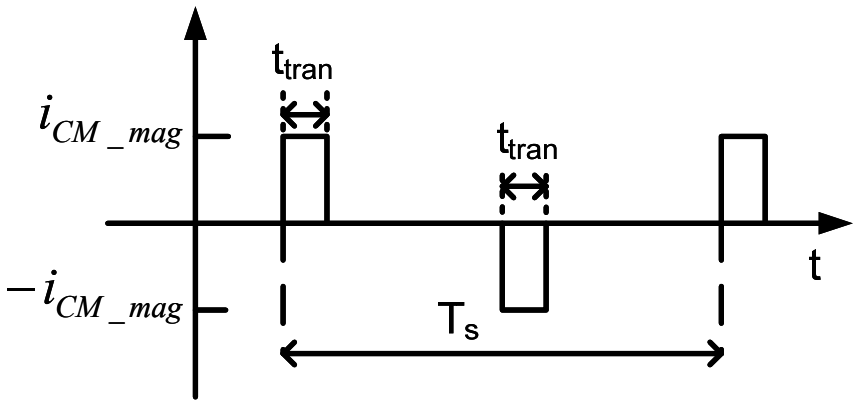


Fig. 2.38. CM noise current waveforms.

For LLC resonant converters, zero-voltage-switching (ZVS) is achieved by the magnetizing current i_{Lm}. To achieve high efficiency, normally, LLC resonant converters operate close to the resonant frequency. For the sake of simplicity, this paper assumes that the LLC resonant converter operates at the resonant frequency. During switching transition time t_{tran}, the magnetizing current charges and discharges the junction capacitances of the MOSFETs. The magnetizing current i_{Lm_tran} during t_{tran} is calculated in (2.21), where N presents the transformer turns ratio, V_o is the output voltage, L_m is the magnetizing inductance, and T_s represents the switching cycle. Because t_{tran} is usually very small and L_m is very large, the magnetizing current changes very little

during t_{tran}. Hence, i_{Lm} is almost constant and does not vary with the load. Therefore, the *dv/dt* of V_{tank} during t_{tran} can be calculated in (2.22), where C_{MOS_Jun} represents the junction capacitances of the MOSFETs. According to (2.23), the magnitude of CM noise current i_{CM_mag} during t_{tran} can be obtained. Substituting (2.21) and (2.22) into (2.23), i_{CM_mag} is rewritten in (2.24). Therefore, the CM current waveform in the time domain can be attained, and it is depicted in Fig. 2.38. Based on (2.24), Fourier series analysis is provided in (2.25). Then the EMI spectra can be calculated from the noise voltages picked up by LISN (2.26). It should be noted that C_{MOS_Jun} is modeled as equivalent linear capacitances. In a real circuit, the CM current should be slightly different due to nonlinear characteristics of C_{MOS_Jun}. Nevertheless, according to the experimental results, for low frequency range, the predicted spectra are still valid. At high frequencies, the predicted spectra deviate slightly compared with the experimental results.

$$i_{Lm\_tran} = \frac{NV_o}{L_m}\frac{T_s - 2t_{tran}}{4} \tag{2.21}$$

$$\frac{dV_{\tan k}}{dt} = i_{Lm\_tran} / C_{MOS\_Jun} \tag{2.22}$$

$$i_{CM\_mag} = (C_{ps1} + C_{ps2} + C_{ps3})\frac{dV_{\tan k}}{dt} \tag{2.23}$$

$$i_{CM\_mag} = \frac{C_{ps1} + C_{ps2} + C_{ps3}}{C_{MOS\_Jun}}\frac{NV_o}{L_m}\frac{T_s - 2t_{tran}}{4} \tag{2.24}$$

$$i_{CM}(t) = i_{CM\_mag} \frac{4t_{tran}}{T_s} \sum_{n=1,3,5...}^{\infty} \frac{\sin(n\pi \cdot t_{tran} / T_s)}{n\pi \cdot t_{tran} / T_s} \sin(\frac{2n\pi}{T_s} \cdot t) \quad (2.25)$$

$$v_{CM}(t) = i_{CM}(t) R_{LISN} \quad (2.26)$$

To verify the derived EMI noise model, a 1kW, 1MHz 400V/48V LLC resonant converter prototype is constructed and discussed in previous section. The parameters are: $t_{tran} = 70ns$, $C_{MOS\_Jun} = 600pF$, the sum of C_{ps1}, C_{ps2} and C_{ps3} is 20pF. The resonant inductor is integrated with the transformer. Based on the derived EMI noise model, the CM noise spectra is calculated in Fig. 2.39. The measured CM noise spectra of the hardware are also shown in Fig. 2.39. It can be observed that the derived model matches the experimental result at low frequencies up to 15MHz. At high frequencies, the model does not fit the experimental results very well. However, for EMI filter design, low-frequency spectra are very important, so the derived model is still beneficial. To obtain a more accurate result for a wider frequency range, more complex factors (i.e., parasitic inductances and the nonlinear characteristics of MOSFET junction capacitances) should be considered.

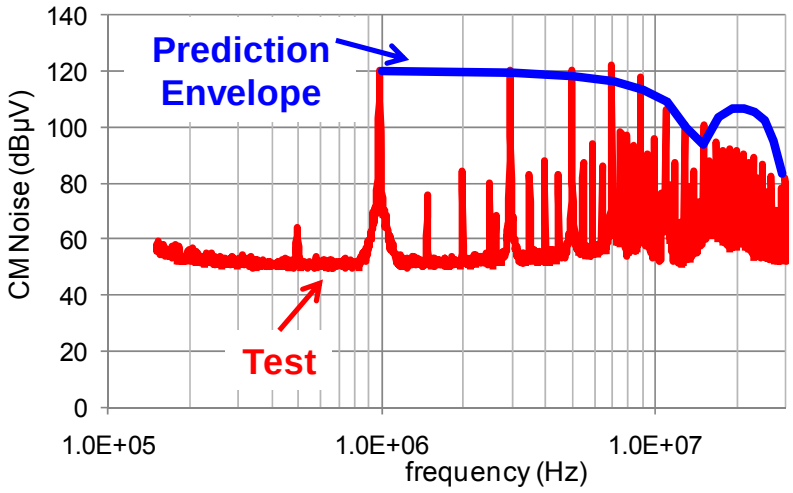


Fig. 2.39. Calculated and measured CM noise spectra comparison of the LLC resonant converter.

On the other hand, based on the derived CM noise model, the CM current is determined by the magnetizing current and thus is not affected by the load. The CM spectra at no-load condition is also measured and shown in Fig. 2.40. Compared with the full-load condition, there is very little difference. This matches the model prediction very well. The no-load switching frequency is 1MHz.

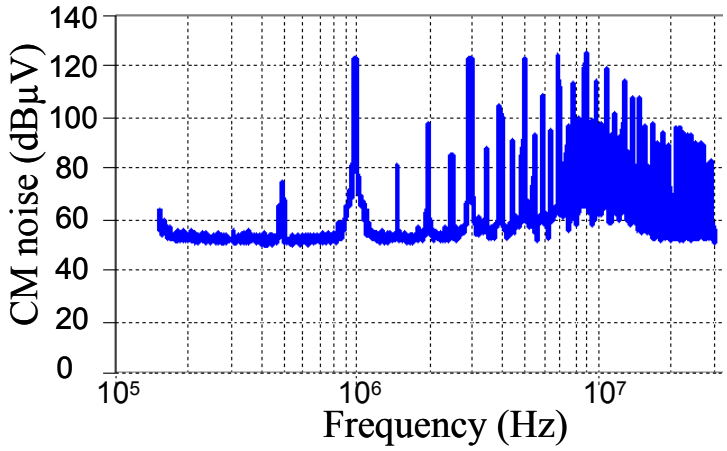


Fig. 2.40. The experimental result of CM noise for LLC resonant converter at no load condition.

2.6 Proposed Approaches to Reduce the EMI Noise of the LLC Resonant Converters

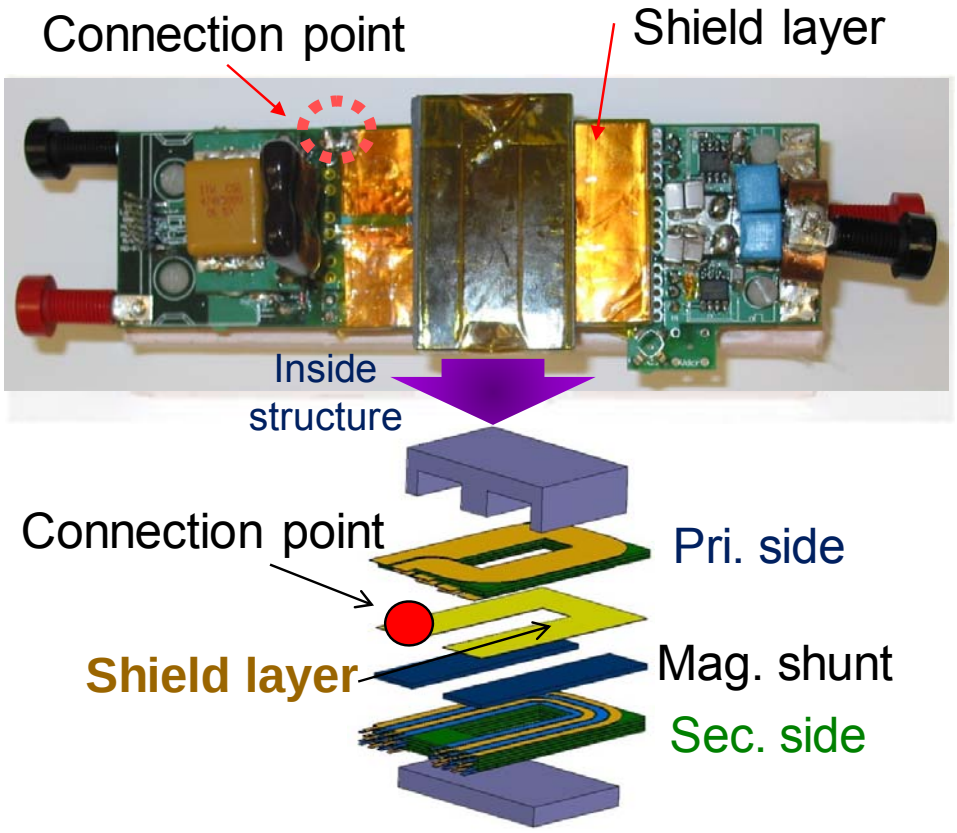
Based on the derived CM noise model of LLC resonant converters, several EMI noise reduction techniques are proposed and studied in this section.

(i) CM Noise Suppression with the Shield Layer

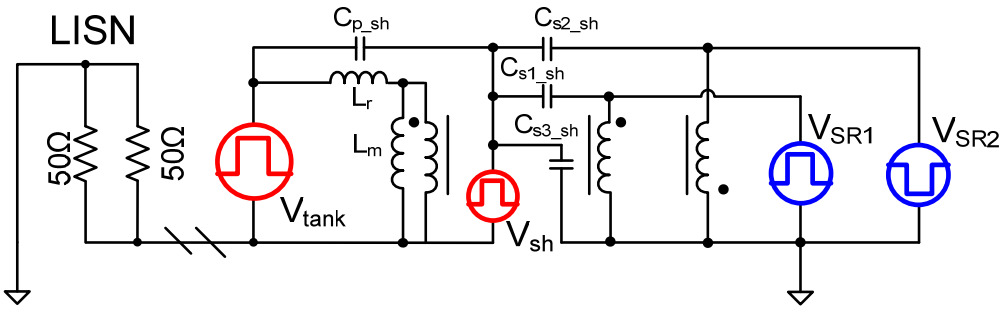
From the derived CM noise model, it is found that the CM noise coupling channel is determined by the inter-winding capacitances C_{ps1}, C_{ps2} and C_{ps3}. To reduce coupling, a shield layer can be introduced. Normally, Faraday shields can be placed between the primary and secondary windings of the transformer to reduce the noise capacitive coupling between the windings of the transformer. The shield layers can be connected with a voltage-stable point. In this paper, the shield layer is connected to the negative terminal of the input voltage. However, choosing the connection point on the shield layer itself is very important. With different connection points, the EMI suppression results are very different. With an improper connection point on the shield layer, very little EMI suppression will be attained. To address this issue, two cases are given.

In case I, the shield layer connection point is selected as the end terminal of the shield layer, which is marked in Fig. 2.41(a). For 400V/48V LLC resonant converters, the primary and secondary side are designed to have 4 transformer turns and 1 transformer turn, respectively. Due to magnetic coupling between the shielding layer and the transformer winding, an induced voltage will be generated on the shield layer. The equivalent CM noise circuit is described in Fig. 2.41(b). Because there are very few

transformer turns in this application, the shield layer acts as another winding with open load. Although the net current on the shield layer is zero, the shield layer will be coupled as inductance and *dv/dt* voltage source due to $d\Phi/dt$. The coupled inductance is calculated as 0.7μH, which can be ignored below 20MHz. As can be seen from the equivalent model, the shield layer can bypass displacement current induced by V_{tank}. However, due to the magnetic coupling, the induced *dv/dt* on the shield layer behaves as a new noise source. Since the shield layer is considered as single turn, the induced *dv/dt* is *Nth* of the V_{tank}. Theoretically, based on the derived CM noise model, the noise attenuation is 12dB. In practice, the experimental result shows only 7dB suppression. This is partially due to increased capacitances coupled by the shield layer and the secondary side winding.



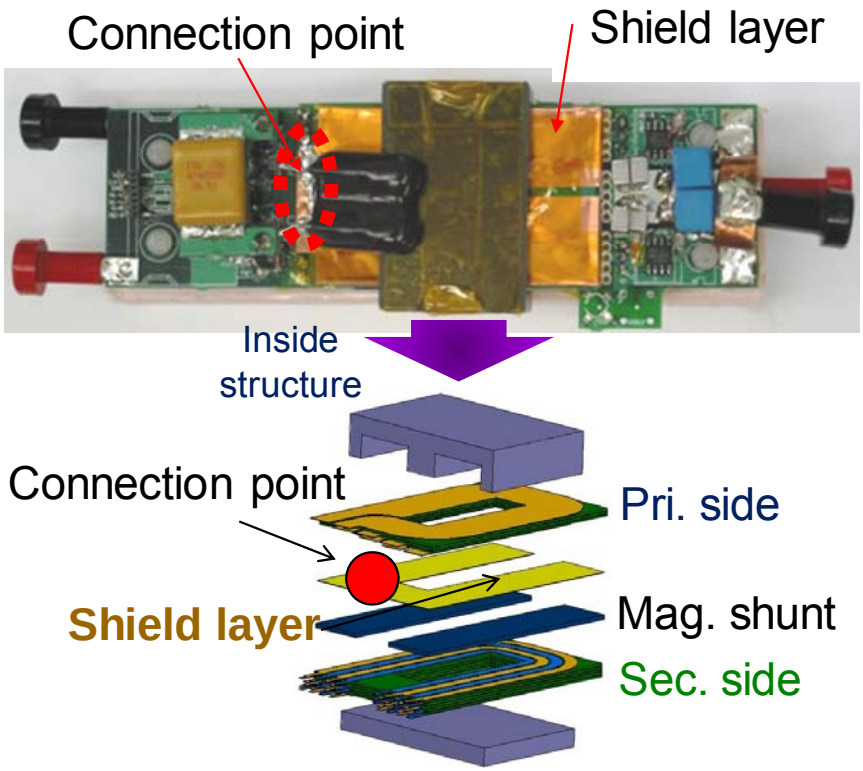
(a) The shield layer connection structure case I.



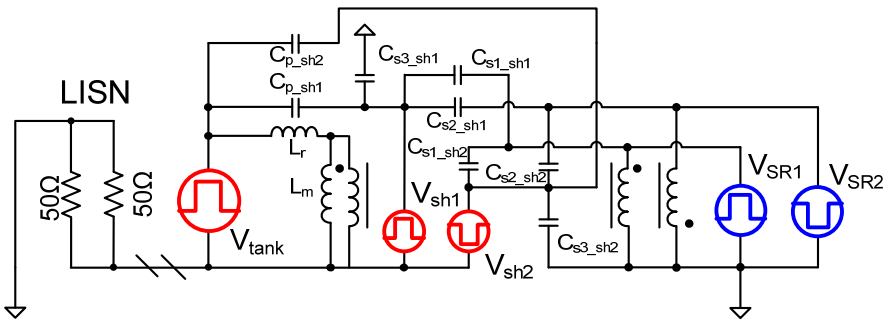
(b) Equivalent CM model of the LLC converter with the shield layer case I.

Fig. 2.41. The LLC resonant converter with the shield layer case I.

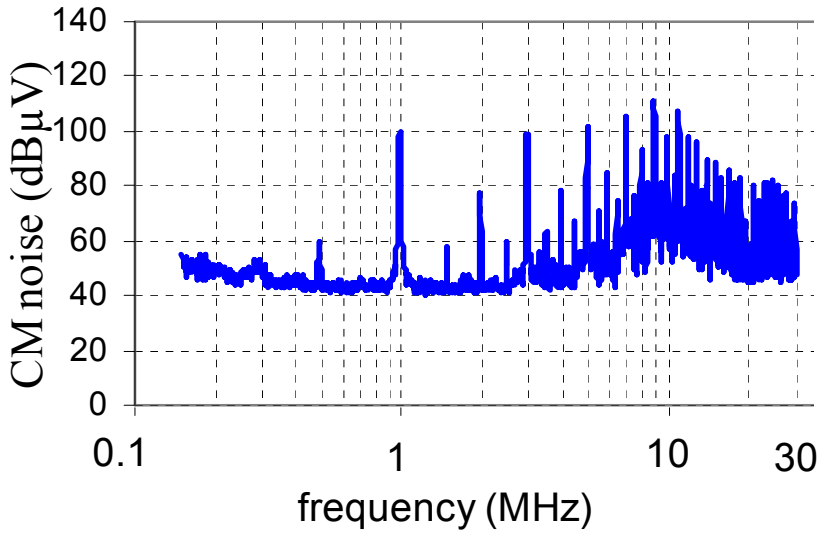
To further improve the CM noise reduction of the shield layer, it is proposed to ground the shield layer at the middle point, which is illustrated in Fig. 2.42(a). The equivalent CM model is shown in Fig. 2.42(b). In this way, the CM noise current induced by *dv/dt* on two symmetrical halves of shield layer can be canceled. Due to symmetrical layout, it can be assumed that $C_{s1\_sh1} = C_{s1\_sh2}$, $C_{s2\_sh1} = C_{s2\_sh2}$, *and* $C_{s3\_sh1} = C_{s3\_sh2}$. Thus, according to the superposition theory, the CM noise current induced by the shield layer can be canceled. Meanwhile, the CM noise current induced by the *dv/dt* of V_{SR1} and V_{SR1} can be canceled. On the other hand, the displacement current induced by V_{tank} is bypassed. With the optimal arrangement of the shield layer, the CM noise can be reduced significantly. Shown in Fig. 2.42(c), 20dB reduction can be achieved with the proposed method by the experimental result.



(a) The shield layer connection structure case II.



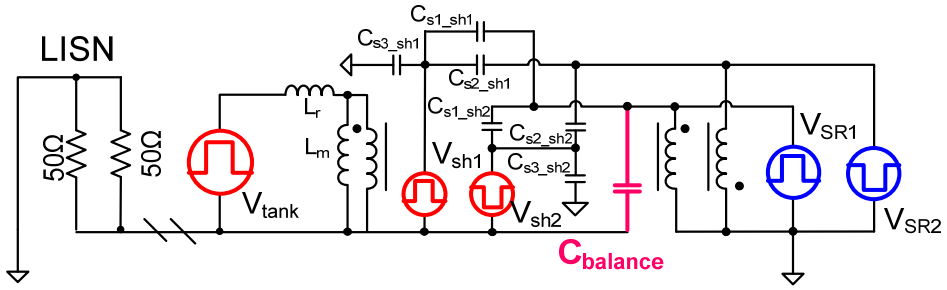
(b) Equivalent CM model of the LLC converter with the shield layer case II.



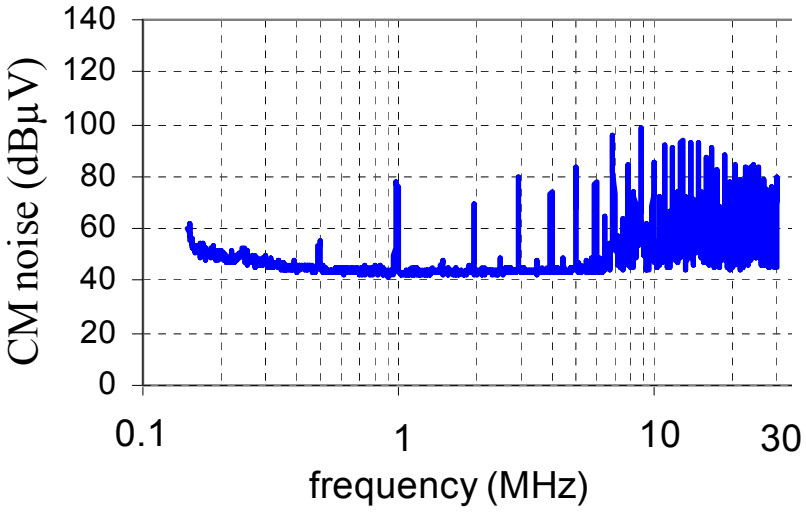
(c) Experimental results.

Fig. 2.42. The LLC resonant converter with the shield layer case II.

(ii) CM Noise Suppression with the Shield Layer and Balanced Capacitance



(a) Equivalent model with added balance capacitor.



(b) Experimental result of CM noise with added Cbalance.

Fig. 2.43. The LLC resonant converter with the shield layer case II and added balance capacitor.

With a symmetrical shield layer, the CM noise can be effectively reduced. However, the CM suppression is highly affected by the symmetry of the winding layout and shield layer layout. Even with the proposed improved shield layer proper connection, it is difficult to cancel all the related CM current. To further reduce the CM noise, an extra CM balance capacitor can be added to balance the unexpected unsymmetrical parasitic capacitance. This CM balance cap can also help to cancel the CM current introduced by other parasitics. The equivalent model is shown in Fig. 2.43(a).

The inserted CM balance cap is connected between the primary side stable point (virtual ground) and the secondary side winding terminal. Due to the *dv/dt* of the secondary side winding, the CM current goes through the balance cap. There are two

secondary side windings. Shown in Fig. 2.43(a), the *dv/dt* of V_{SR1} is in phase with the primary side winding. The balance cap should be connected with V_{SR1}. Hence, the generated CM current can be utilized to cancel the original CM current.

As a result, the CM noise can be further suppressed. As verified by the experiment result in Fig. 2.43(b), 40dB noise reduction is achieved.

(iii) Two-channel interleaving LLC resonant converters to cancel the CM noise

Although the shield layer and the CM balance capacitance can help to reduce the CM noise, there are some limitations. Eddy currents are induced on the shield layer, which cause extra losses. This leads to a 0.1% efficiency reduction for the developed prototype. To obtain the best CM noise reduction, the CM balance capacitance should be chosen very carefully. In some cases, the capacitance should be determined experimentally. Once the layout is changed, the value of the capacitance should be corrected accordingly. A change in layout may introduce design complexity. Thus, an alternative strategy can be studied to reduce the EMI without affecting the performance of the original designs.

Two-channel interleaving LLC resonant converters are proposed to cancel the CM current. The topology is shown in Fig. 2.44. With 180^o phase shift operation, ideally, the CM current should be totally canceled. Shown in Fig. 2.45 and Fig. 2.46, the CM noise currents of the two LLC channels, which go through the LISN, are 180^o phase-shifted with the same amplitude. Therefore, the total current going through the LISN resistors will be zero, which means the lowest EMI noise can be obtained. Meanwhile,

no extra components are required, and no modifications of designs are needed. Hence, it can achieve very low EMI without hurting the performance (efficiency, size, etc.).

According to the experimental results shown in Fig. 2.47, 30dB noise reduction is achieved. Compared with the shield layer with the CM balance capacitance case, the CM noise attenuation is less than the expected value. This is due to the nuances of the asymmetry of the circuits. However, the noise suppression effect is still significant

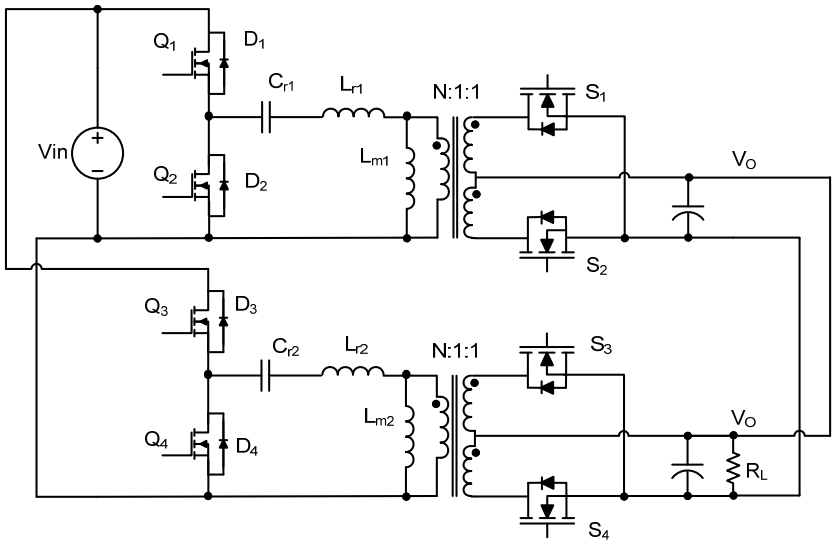


Fig. 2.44. The proposed two-channel interleaving LLC resonant converters with 180 degree phase shift.

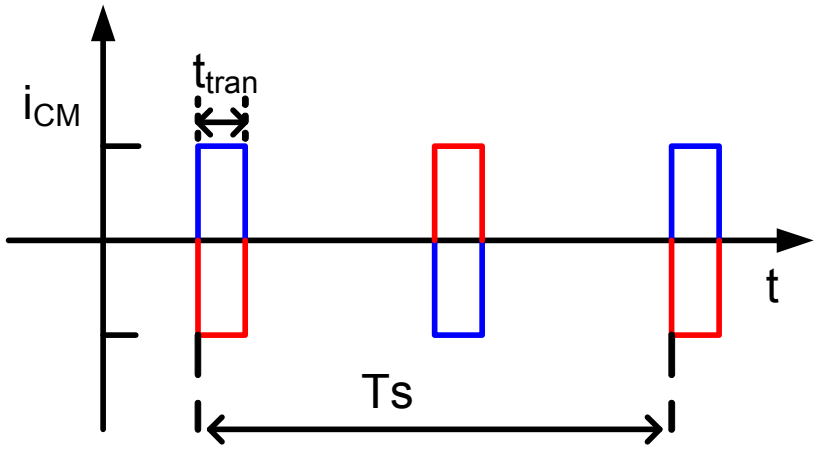


Fig. 2.45. The CM current cancelling effect of the proposed two-channel interleaving LLC resonant converters with 180° phase shift.

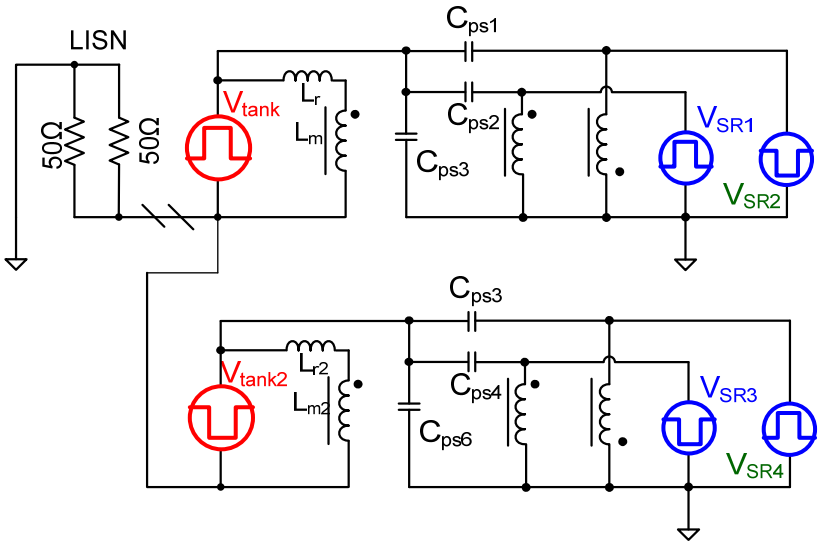


Fig. 2.46. The CM noise model of the proposed two-channel interleaving LLC resonant converters with 180° phase shift.

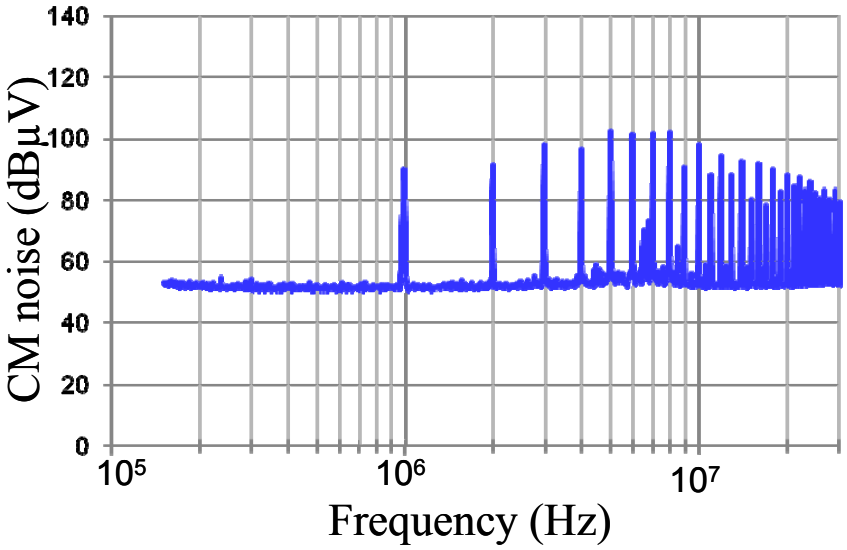


Fig. 2.47. Experimental result of the CM noise for proposed two-channel interleaving LLC resonant converters with 180° phase shift.

The CM noise reduction results are shown in Fig. 2.48. Over 40dB noise reduction is achieved with the proposed noise suppression techniques.

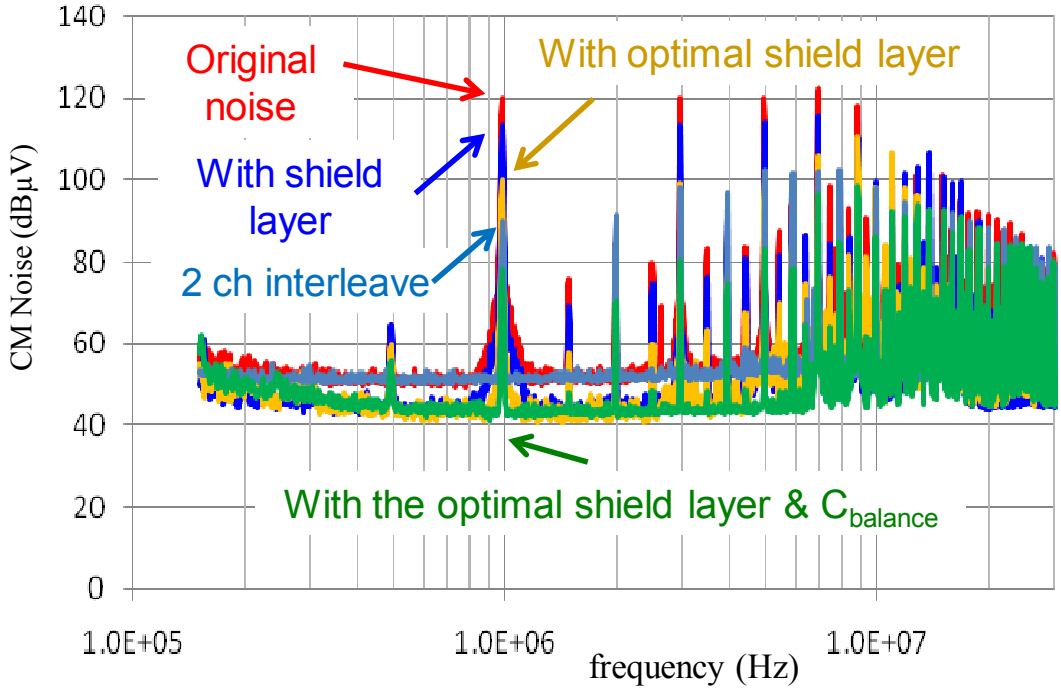


Fig. 2.48. CM noise results comparison with the proposed noise reduction techniques.

Chapter 3

Improvement of LLC Resonant Converters — Proposed Multi-Element Resonant Converters

3.1 Introduction

As discussed in Chapter 1, startup and current protection are the stringent challenges of LLC resonant converters. To limit the current, several methods have been proposed.

In [D.38] and [D.39], clamped-mode LLC converters were proposed to solve the startup and over current protection problems. The method in [D.38] was to apply diode clamping circuits, and in [D.39] it was to adopt transformer-coupled diode clamping circuits. These topologies are illustrated in Fig. 3.1.

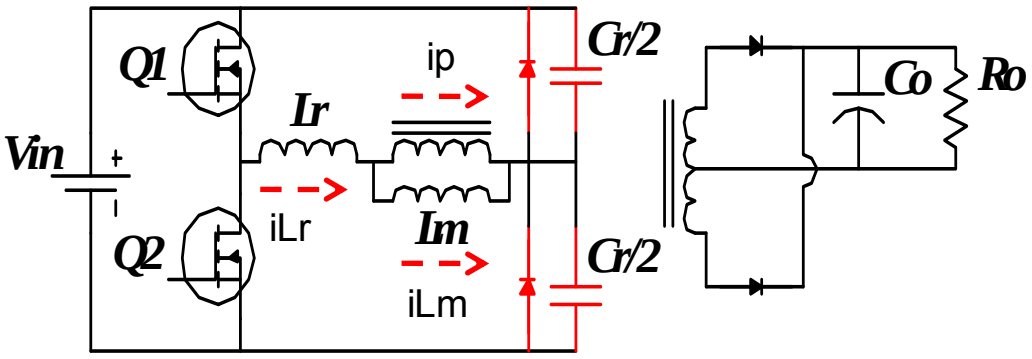


Fig. 3.1. Diode-clamped LLC resonant converters.

With the clamping circuits, the voltage of resonant capacitor is clamped. As shown in Fig. 3.2, according to state plane analysis, the resonant capacitor stores energy and resonant tank energy is clamped. As a result, the resonant tank current can be limited. The relationship of the resonant tank current and output current are expressed as follows:

$$i_{Lr} = i_p + i_{Lm} \tag{3.1}$$

$$\frac{\int_0^{\pi} i_{Lr}}{\pi} = \frac{\int_0^{\pi} i_p}{\pi} + \frac{\int_0^{\pi} i_{Lm}}{\pi} \tag{3.2}$$

$$\frac{\int_0^{\pi} i_{Lr}}{\pi} = I_o / N^2 + \frac{\int_0^{\pi} i_{Lm}}{\pi} \tag{3.3}$$

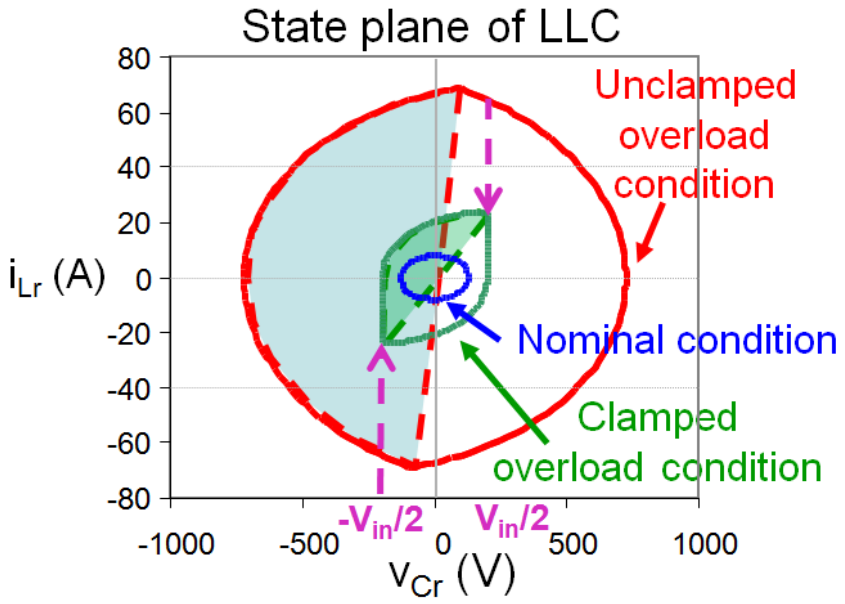


Fig. 3.2. State plane analysis of clamped and unclamped LLC resonant converters.

The initial angle 0 is defined as the phase at which negative i_{Lr} meets i_{Lm}. Angle π is defined as the phase at which positive i_{Lr} meets i_{Lm}. Under over load or short conditions, the output voltage is very low. Hence, i_{Lm} is very low. Thus, according to (3.3), the resonant tank current almost reflects the load current. As Fig. 3.2 suggests, the average value of resonant tank in one half-cycle roughly represents the load current reduced to the primary side. The shaded area reflects the resonant tank current stress and load current stress.

At startup and over-load conditions, the stored energy of the resonant tank and the resonant tank current for the clamped LLC converter are significantly lower than the unclamped counterpart. Hence, clamped LLC resonant converters can limit the resonant tank current and load current effectively. Thus clamped mode characteristics are clearly revealed.

However, with clamping circuits, the resonant tank energy needed for a wide input voltage range is also compromised. Shown in Fig. 3.3, the state plane analysis illustrates the difference of the resonant tank energy for clamped mode and unclamped mode LLC resonant converters. Apparently, due to the clamping effect, very little energy can be stored in the resonant tank. Thus, high voltage gain capability for holdup time operation of LLC resonant converters will be sacrificed.

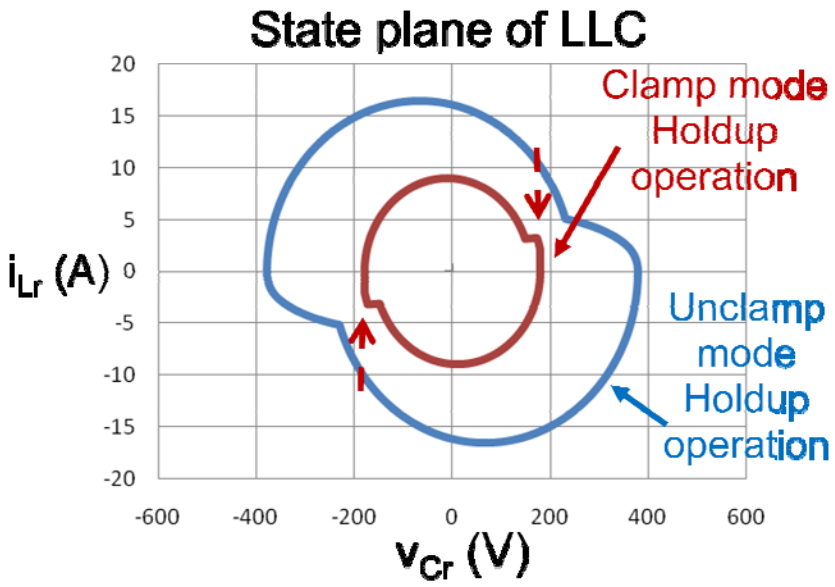


Fig. 3.3. State plane analysis of clamped and unclamped LLC resonant converters for holdup time operation.

Another method of limiting the inrush current is to use a combination of varied-frequency control and PWM control [D.40]. In this case, as shown in Fig. 3.4, a full-bridge topology is chosen. PWM control can be applied to limit the resonant tank input voltage. Therefore, the current can be lower. However, the drawback of this method is the loss of ZVS conditions during the duty cycle control. As illustrated in Fig. 3.5, ZVS is only achieved for S_2 and S_4. For S_1 and S_3, ZVS is lost, which is detrimental to the circuits. The ZVS operation region under duty cycle control is plotted in Fig. 3.6. Only a limited duty cycle can be utilized to limit the current. The duty cycle control might be combined with variable frequency control to solve the issue of ZVS loss. However, this method requires a very complicated control scheme. As a result, this strategy is not attractive.

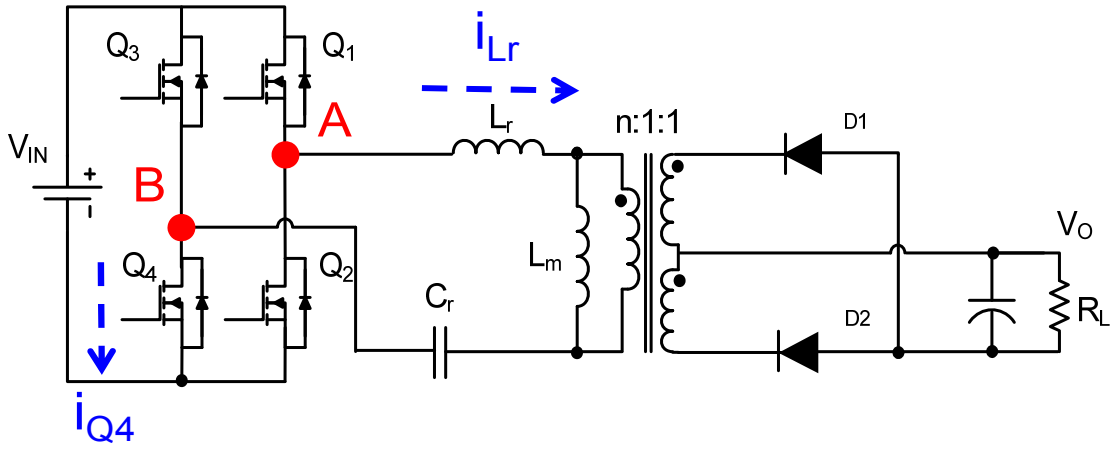


Fig. 3.4. Full-bridge LLC resonant converters.

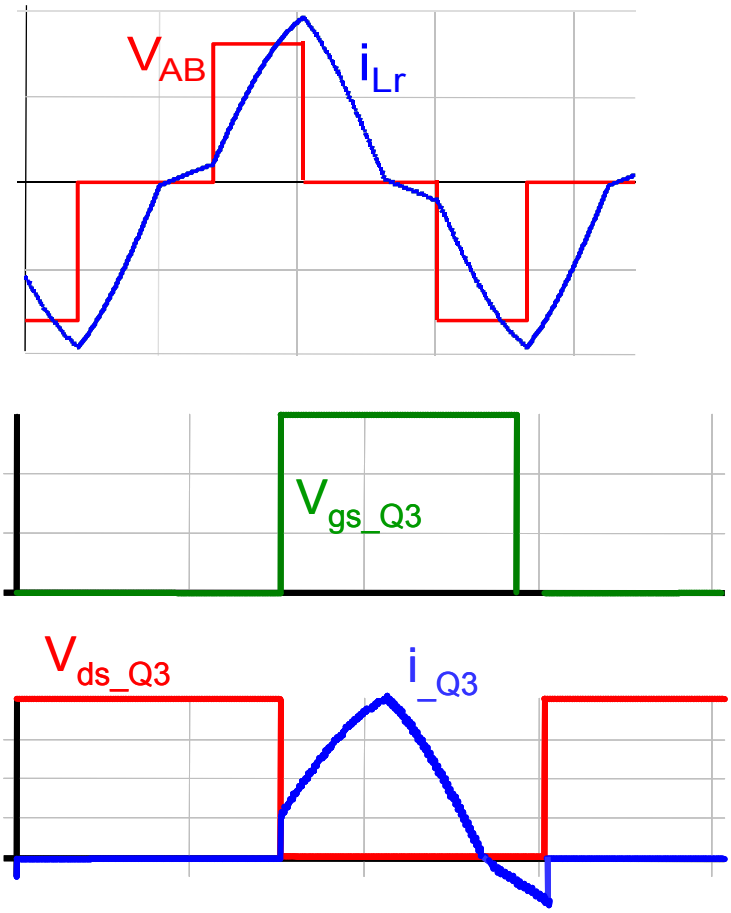


Fig. 3.5. Lost ZVS in PWM mode control of LLC resonant converters.

The LLC resonant tank can be considered as a band pass filter, but the frequency selectivity of the LLC tank is poor. Due to very wide bandwidth, the frequency has to be increased very high to achieve enough voltage gain controllability. However, this is not practical for dc-dc converters due to the limitation of driving circuits and the excessive switching & driving losses.

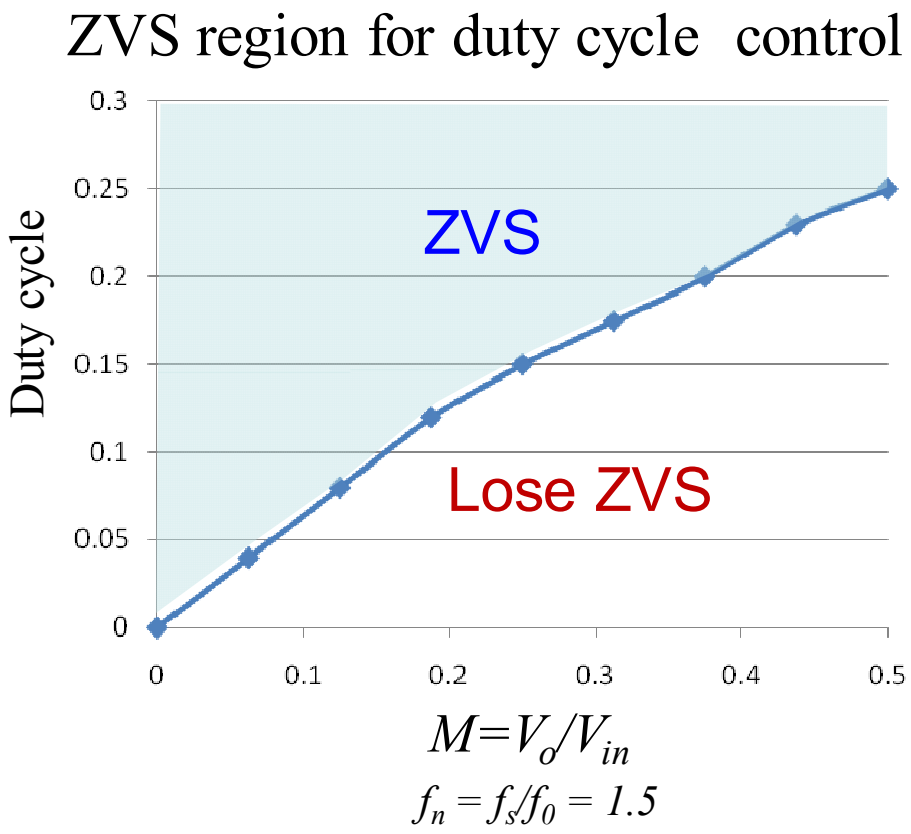


Fig. 3.6. ZVS operation region for PWM duty cycle control of LLC resonant converters.

3.2 Proposed Multi-Element Resonant Tank to Solve Startup and Current Protection Issues

To avoid adding complex auxiliary circuits, an alternative strategy is to enhance the performance by shaping the characteristics of the resonant tanks. To improve the characteristics of LLC resonant converters, an additional resonant element can be introduced.

With an additional resonant element component, a multi-element resonant tank, which combines a band pass filter and a notch filter, is proposed to solve the current protection issues. The basic resonant tank cell is depicted in Fig. 3.7. The notch filter section is created with L_r and C_p. The band pass filter section consists of L_r, C_r and C_p.

The voltage gain of this four-element resonant tank is illustrated in Fig. 3.8. The resonant frequencies f_{01} and f_{02} are defined in (3.4) and (3.5), respectively. The LCCL resonant tank with notch filter characteristics can create zero voltage gain. Theoretically, infinite impedance can be created when the frequency operates at the resonant frequency of the notch filter, f_{02}. As a result, if an overload or even a shorted output condition occurs, the current is inherently limited by the resonant tank characteristic. The notch filter center frequency f_{02} can be designed to achieve overload protection. f_{02} is designed to be close to nominal resonant frequency f_{01}. Thus, it is easy to limit the current without an excessive increase of the switching frequency.

On the other hand, the resonant tank parameters should be designed very carefully. Otherwise, the notch filter section will adversely affect the nominal operation. For

instance, if f_{01} is designed to be very close to f_{02}, the notch filter section 'traps' energy. As a consequence, energy circulates in the notch filter section. Determining how to choose the notch filter resonant frequency is very critical. In general, with variable frequency control, the resonant tank input voltage is excited as a square waveform. According to the Fourier analysis (3.6), the voltage excitation only consists of odd harmonics. Therefore, to avoid circulating energy at nominal conditions, notch filter resonant frequency f_{02} might be designed far away from the odd harmonics. In this way, the network of L_r and C_p trap the least energy of odd order harmonics. Thus, $f_{02} \approx 2 f_{01}$ is a good choice.

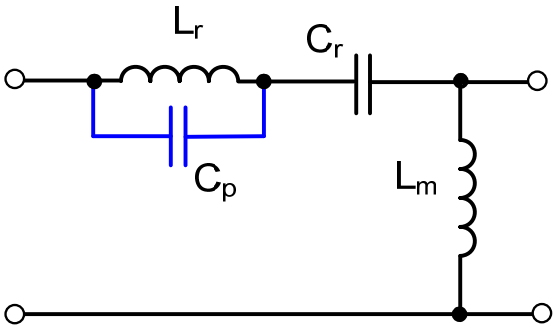


Fig. 3.7. Multi-element resonant tank with combination of band pass filter and notch filter characteristics.

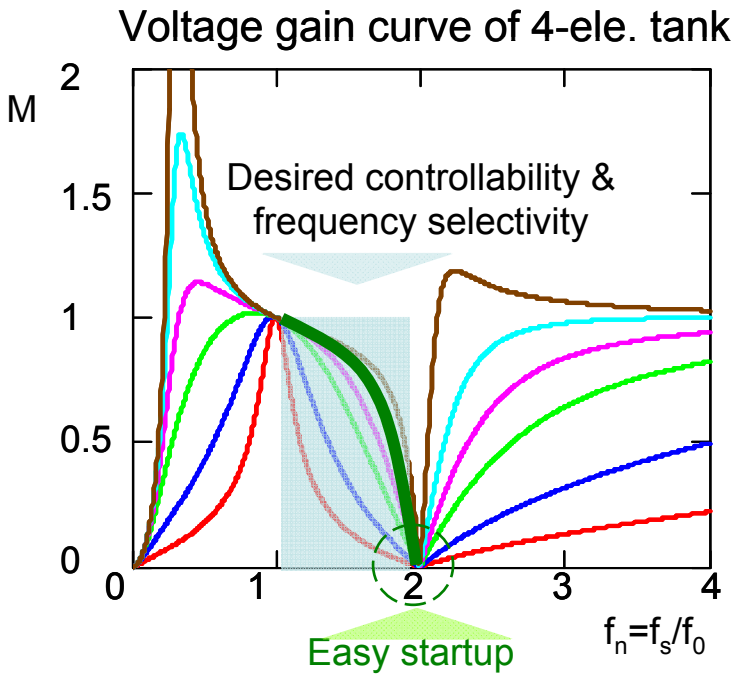


Fig. 3.8. Voltage gain of multi-element LCCL resonant tank.

$$f_{01} = \frac{1}{2\pi} \frac{1}{\sqrt{L_r (C_r + C_p)}} \tag{3.4}$$

$$f_{02} = \frac{1}{2\pi} \frac{1}{\sqrt{L_p C_p}} \tag{3.5}$$

$$v_{in}(t) = \frac{4}{\pi} \cdot V_{in} \cdot \sum_{n=1,3\cdots}^{\infty} \frac{\sin(n\omega_s t)}{n} \tag{3.6}$$

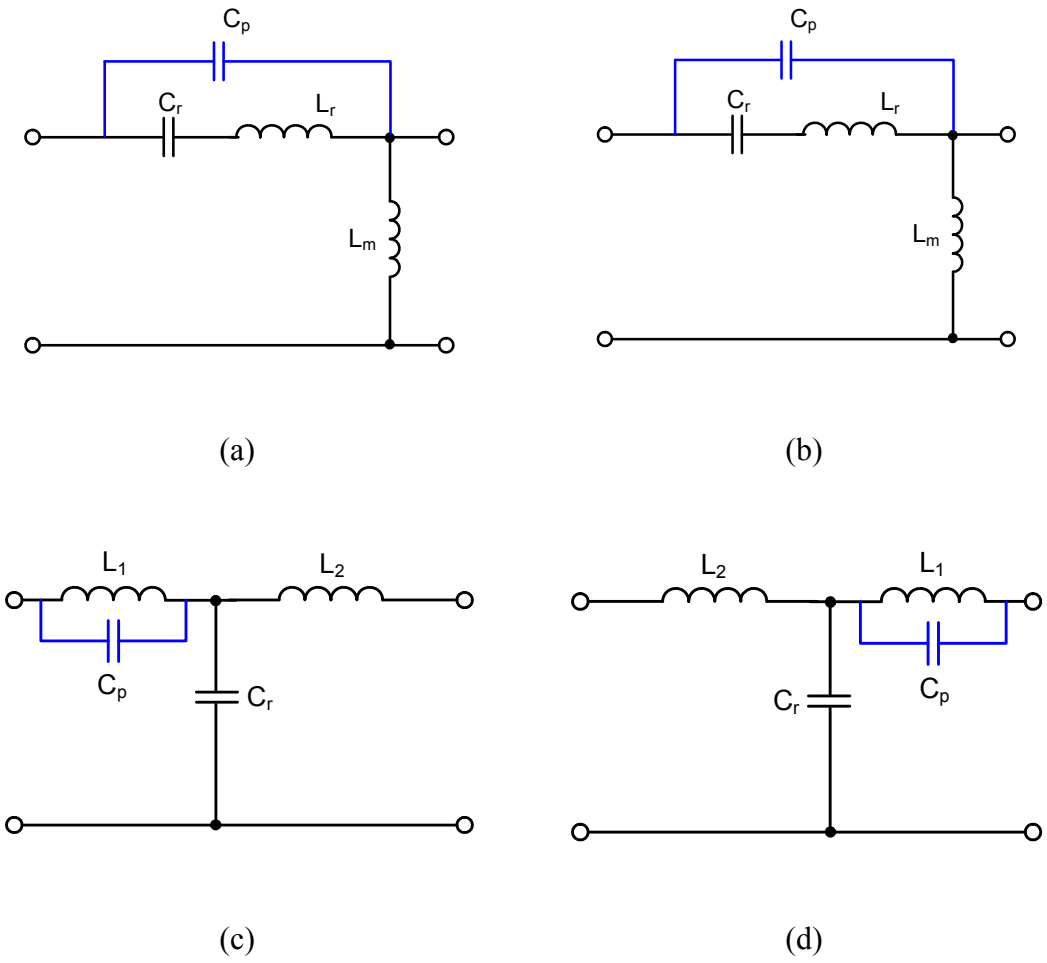


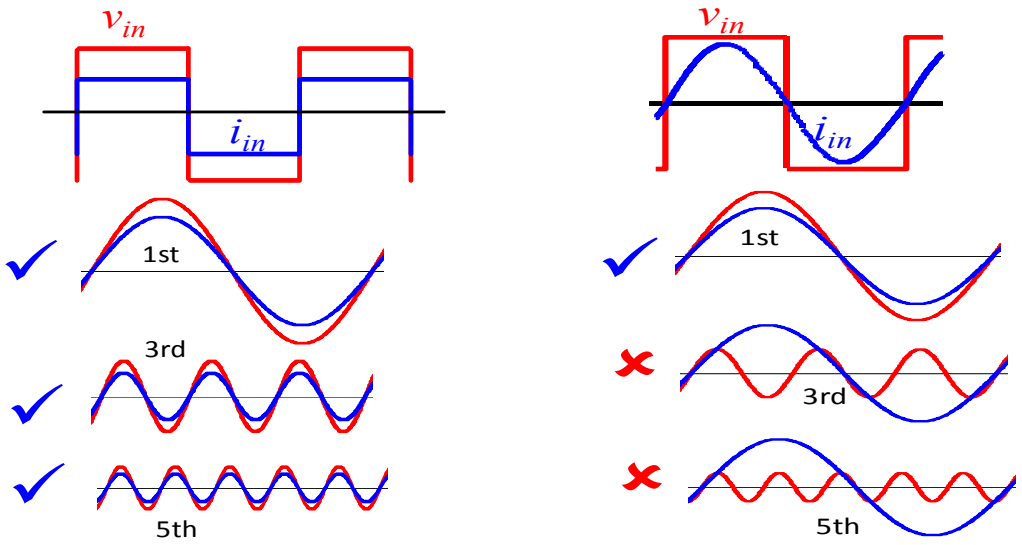
Fig. 3.9. Other possible resonant tanks combined with band pass and notch filter characteristics.

With the extension of the filter characteristics combination, other constructions of resonant tanks are drawn in Fig. 3.9. It should be noted that the real circuit performance of these proposed resonant tanks may or may not be the same as the performance of LLC resonant converters, and should be identified specifically.

The low-frequency gain characteristic of the LCCL resonant tank is very desirable. However, in the very high frequency range, the voltage gain is not preferable. The high-

frequency voltage gain is lightly damped, which means the resonant tank controllability of high-order harmonics might be compromised. Fortunately, the resonant tank can be improved further to reinforce controllability of the higher-order harmonics.

3.3 Multi-Element Resonant Tank with Utilization of Higher Order Harmonics to Enhance Power Delivery



(a) Typical waveforms and power delivery analysis for PWM converters

(b) Typical waveforms and power delivery analysis for resonant converters

Fig. 3.10. Fourier analysis of waveforms for PWM and resonant converters.

Most of the resonant converters developed so far include some inherent weaknesses, such as increased conduction losses due to circulating energy generation. In general, the current and voltage of the primary side of isolated PWM converters are square waves

without a noticeable phase shift. Therefore, virtually no circulating energy is generated during the power processing. For the resonant converter, a square-wave inverter and a resonant network transfer and control the fundamental power to the output in a piece-wise sinusoidal manner. As a result, the high-order harmonics of the input voltage and the current of the resonant tank exhibit reactive power, which never contributes to the power delivery. It is also assumed that there is no phase shift between the voltage and the current of the resonant converters. With additional phase shift, the circulating energy becomes even larger. Generally speaking, the amount of power processed by the resonant converter is usually larger than that of a PWM converter with the same output power. This has an adverse effect on the performance of resonant converters.

However, once PWM circuits process all the harmonics, the switching performance of the main devices is sacrificed. At the turn-off edge of the switch cycle, the current is high. Although achieving ZVS can eliminate turn-on switching loss, the-turn off loss is high. The conventional resonant converters control the fundamental component and limit the turn-off current. Therefore, the switching loss of resonant converters is lower than the switching loss of PWM circuits. Our question now becomes, is there a strategy to combine the benefits of PWM converters and resonant converters? Namely, how can we utilize the higher-order harmonics for power delivery without compromising the switching performance?

The answer is simple. With an additional resonant element, there are opportunities to combine all of the advantages of PWM converters and resonant converters. Novel five-element resonant converters are proposed to solve all of these problems.

With one additional resonant element, a second band pass filter is created. A novel LCLCL resonant tank is proposed as an example. The basic resonant tank cell is shown in Fig. 3.11. The structure is similar to the previously proposed four-element resonant tank, but an extra resonant inductor is inserted.

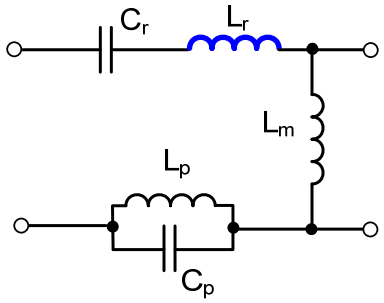


Fig. 3.11. A novel LCLCL five-element resonant tank to achieve startup and utilize high order harmonics.

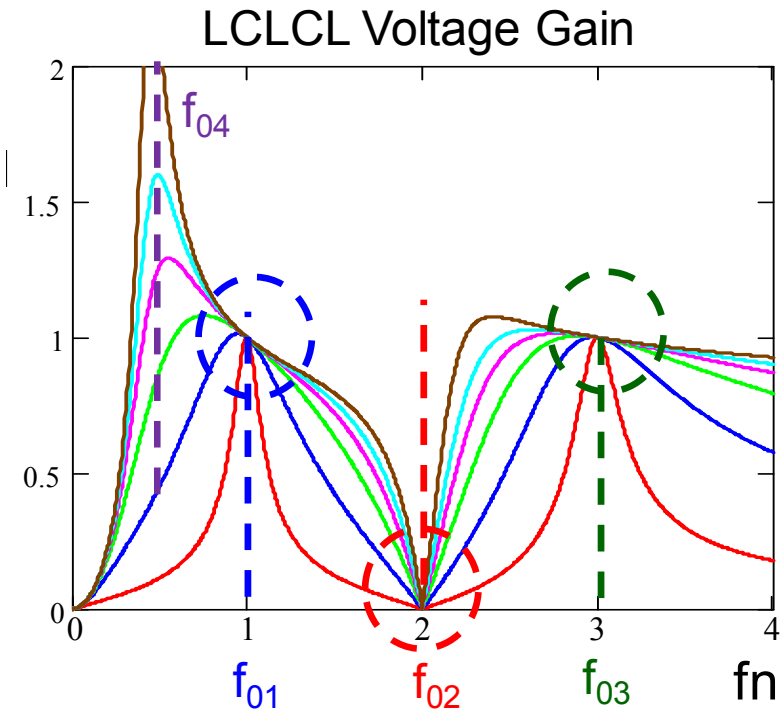


Fig. 3.12. Approximate voltage gain of the novel LCLCL five-element resonant tank.

The typical resonant parameters are defined in (3.7) – (3.14). N represents the transformer turns ratio and R_L represents the load. The approximate voltage gain of the proposed LCLCL resonant converter is illustrated in Fig. 3.12. Conceptually, L_r, C_r and L_p contribute to the first band pass filter at low frequencies. The second band pass filter consists of L_r, C_r and C_p, which dominate at high frequencies. The first band pass filter can help to deliver the fundamental component to the load. It functions as the traditional resonant converters. The second band pass filter enhances the power delivery with utilization of higher harmonics. Consequently, with the injection of higher-order harmonics, the reactive power of the resonant tank can be reduced and lower rms current and lower conduction loss can be achieved. The simulated waveforms are shown in Fig. 3.13.

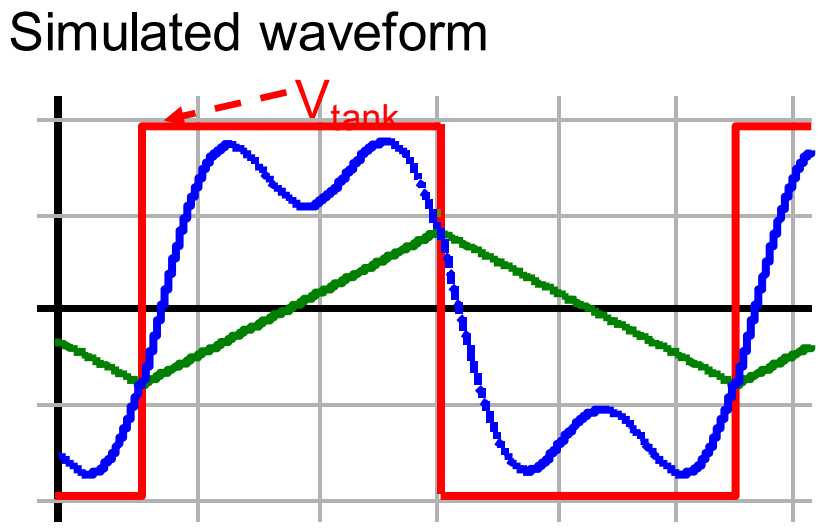


Fig. 3.13. The typical waveforms of the proposed novel LCLCL five-element resonant tank.

On the other side, to maintain the very low switch current of the main devices, highly distorted current should be avoided. Hence, excessive high-order harmonics should not

be included in the resonant tank. The second band pass filter is designed to provide enough damping to prevent this at very high frequencies. Therefore, the performance of the resonant converter is improved. In this application, the resonant frequency of the second band pass filter is designed to be three times the nominal frequency. That is, $f_{03} = 3 f_{01}$. Obviously, the third-order harmonics helps to transfer the power. According to Fourier analysis, 10% of the power can be processed by the third-order harmonic. The circulating energy is therefore reduced.

$$f_{01} = \frac{1}{2\pi}\sqrt{\frac{L_rC_r + L_pC_p + L_pC_r - \sqrt{(L_rC_r + L_pC_p + L_pC_r)^2 - 4L_rC_rL_pC_p}}{2L_rC_rL_pC_p}} \approx \frac{1}{2\pi}\sqrt{(L_r + L_p)C_r} \tag{3.7}$$

$$f_{02} = \frac{1}{2\pi}\frac{1}{\sqrt{L_pC_p}} \tag{3.8}$$

$$f_{03} = \frac{1}{2\pi}\sqrt{\frac{L_rC_r + L_pC_p + L_pC_r + \sqrt{(L_rC_r + L_pC_p + L_pC_r)^2 - 4L_rC_rL_pC_p}}{2L_rC_rL_pC_p}} \approx \frac{1}{2\pi}\sqrt{L_r\frac{C_rC_p}{C_r + C_p}} \tag{3.9}$$

$$f_{04} = \frac{1}{2\pi}\frac{1}{\sqrt{C_r(L_r + L_m + L_p)}} \tag{3.10}$$

$$Z_0 = L_r 2\pi f_{01} \tag{3.11}$$

$$Q = \frac{Z_0}{N^2 R_L} \tag{3.12}$$

$$f_n = f_s / f_{01} \tag{3.13}$$

$$L_n = L_m / L_r \tag{3.14}$$

However, one of the main purposes of the converter is to provide over current protection. Therefore, the notch filter characteristic should be retained. L_p and C_p keep the notch filter performance without adversely affecting the other two band pass filters. The discussions above reveal how to determine the frequency of the notch filter section for a four-element resonant tank. The derivation is also valid for a five-element LCLCL resonant tank.

The current of L_p can be normalized with the base value of full load current. With different selection of f_{02}, the current of L_p is different. The result is shown in Fig. 3.14. If f_{02} is chosen to be too close to f_{01} or f_{03}, due to large impedance of notch filter section, more energy is trapped. Thus, higher circulating current goes through the notch filter. The lowest current is obtained if f_{02} is designed around $2f_{01}$.

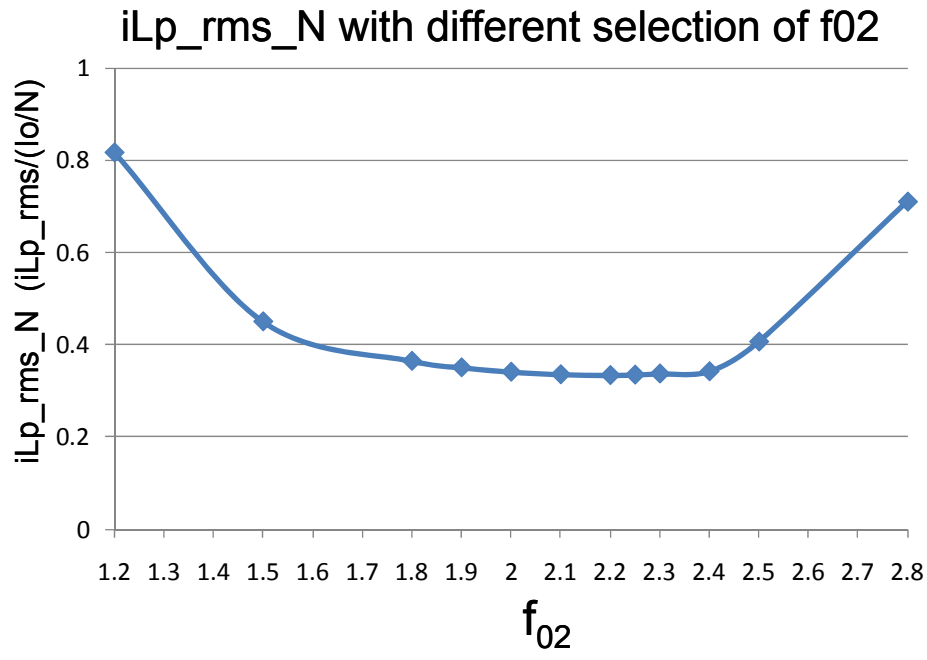


Fig. 3.14. Normalized current of L_p for different selections of f_{02}.

The LCLCL resonant tank is selected as the core of this converter. The half-bridge topology is adopted as the primary side structure. It is easy to extend to other types of input structures, including full-bridge, stacked half–bridge, and three-level structures. The center tap structure with synchronous rectifiers (SR) is chosen for use on the secondary side. Similarly, it is easy to use other types of output structures, such as full-bridge, voltage-doubler and current-doubler structures. The secondary side with the SR is better for low-voltage output applications. The secondary side devices can be replaced by diodes for high-voltage applications. Thus, complicated SR driving circuits can be avoided. For front-end converters, SR output is applied to increase the efficiency.

The LCLCL resonant converter can achieve ZVS for the primary side and ZCS for the secondary side. With proper design, the magnetizing current i_{Lm} can help to achieve ZVS for zero load to full load range. At the nominal condition, the LCLCL resonant converter operates at the resonant frequency f_{01}, where nearly ZVZCS conditions can be achieved for the primary side devices. The current of the secondary side rectifiers naturally falls to zero, and the reverse recovery issue is eliminated. Very low switching losses are accomplished due to the soft-switching operation. Furthermore, compared with traditional resonant converters, the third-order harmonic is injected and improves the power process. Hence, both the peak current and rms current of the resonant tank are reduced, and the conduction losses and current stresses of devices are alleviated.

L_m is designed to be 13μH according to ZVS conditions. $L_n=13$, based on the holdup voltage gain requirement. f_{01} is chosen to be 1MHz. Based on (3.7)–(3.14), $L_r=1\mu H$, $C_r=11.3nF$, $L_p=0.9\mu H$ and $C_p=6.8nF$ are obtained.

As shown in Fig. 3.12, in ZVS Region I, the voltage gain of the LCLCL resonant converter is lower than one and drops sharply. When the switching frequency is close to resonant frequency f_{02}, the voltage gain is almost zero. The operation waveforms are illustrated in Fig. 3.17 for the most serious case of a short in the output. The primary side current is limited and does not exceed the current rating of the power devices. At the same time, ZVS can be achieved, and thus very low voltage stress can be achieved. In overload or short conditions, the LCLCL resonant converter can operate close to f_{02}. Therefore, the output current can be still limited to a very low value. The circuit can survive without damage to the components. The switching frequency range is also satisfactorily limited. This is the superior characteristic of the proposed LCLCL resonant converter. However, for other conventional resonant converters, such as the LLC resonant converter, the operation frequency must be increased to be several times higher to achieve the same protection function. For high-frequency operation (MHz), an extremely wide switching frequency range cannot be achieved due to the limit of the gate-driving circuits and thermal design.

Hardware is designed to verify the theoretical analysis. Shown in Fig. 3.15, a 1kW, 1MHz 400V/48V prototype is built to demonstrate the advantages of the proposed multi-element resonant converters. In the real circuit, $L_m=13\mu H$, $L_r=1\mu H$, $C_r=12nF$, $L_p=1\mu H$ and $C_p=4.7nF$.

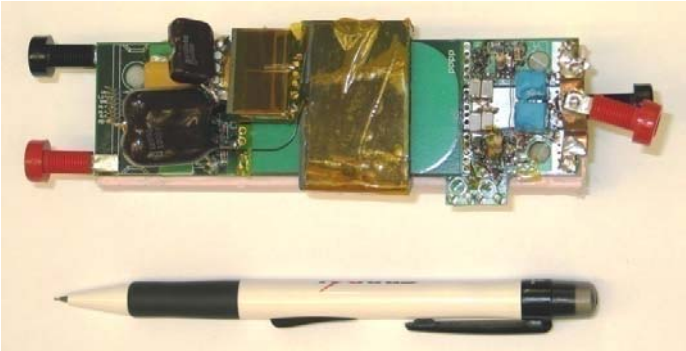


Fig. 3.15. 1kW 1MHz prototype with 86W/in^3 power density.

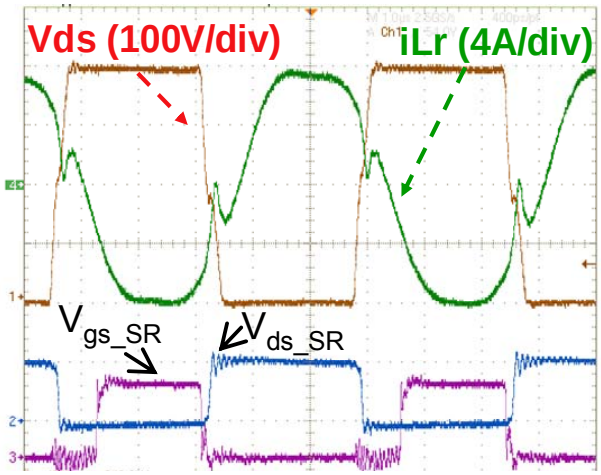


Fig. 3.16. Operation waveforms at nominal condition — 1kW, 1MHz.

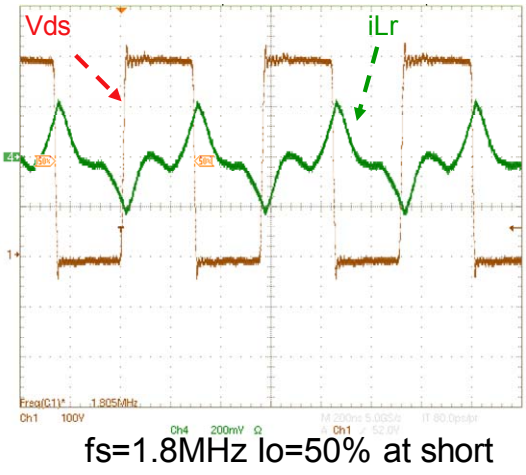


Fig. 3.17. Operation waveforms at short output condition.

With additional resonant elements, the passive component size is increased. The passive component integration technique is applied to achieve high power density. The magnetic components L_m, L_r and the transformer are successfully integrated into one component. In this prototype, L_p is the only magnetic component that is not integrated.

The power density of the prototype is 86W/in^3. The efficiency is 95.5%, which is very high for MHz-frequency operation. The waveforms for the nominal condition are shown in Fig. 3.16. This is very close to the square waveforms with low rms current. The short circuit protection of the LCLCL resonant converter is also verified by the experimental result, and is illustrated in Fig. 3.17. When the output is shorted, the LCLCL resonant converter can operate at 1.8MHz. The output current is limited without hurting the operation of the converter. The short protection has been tested with a prototype. The experimental results of multi-element resonant converter with notch filter are shown in Fig. 3.17. The current has been limited successfully at short condition.

Using a similar concept, a family of multi-element resonant converters is proposed. Some of the five-element resonant tanks are shown in Fig. 3.18. Due to space limitations, the formation of all of the five-element resonant converters cannot be exhibited completely in this work. Please refer to the details in the cited patent [E.14].

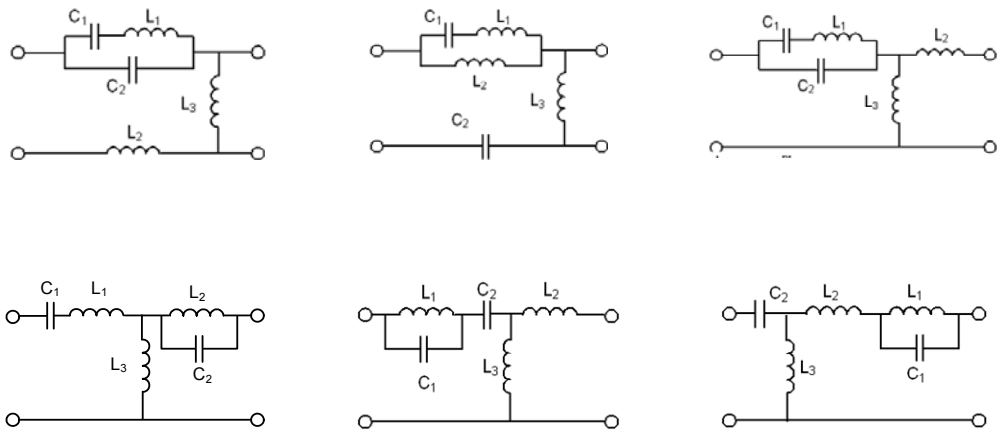


Fig. 3.18. Examples of proposed multi-element resonant converters.

Chapter 4

Investigation of Package and Optimal Design of High Current Resonant Converters

4.1 Introduction

For telecom applications, the output voltage of front-end dc-dc converters is 48V. The previous chapters focus on improvements of 48V output resonant converters. Recently, for server applications, the output voltage of front-end ac-dc converters is mainly 12V. For low-output-voltage high-output-current applications, achieving high efficiency is a stringent challenge.

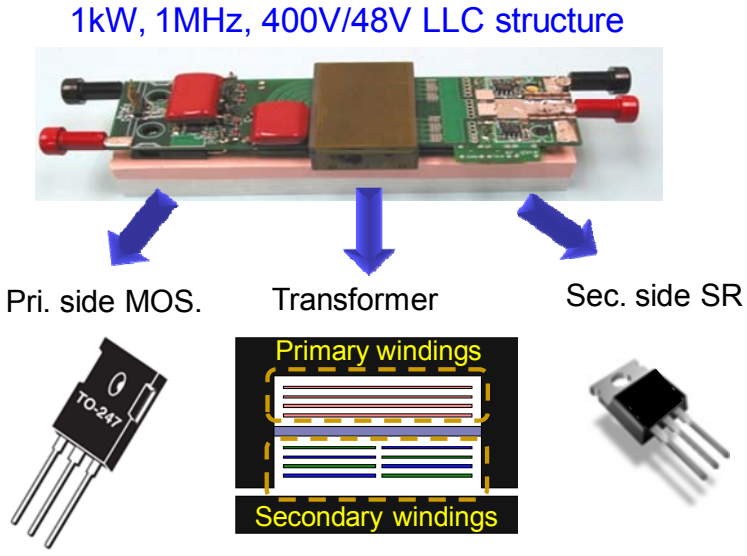


Fig. 4.1. Basic design structure of 1kW, 1MHz, 400V/48V LLC resonant converters.

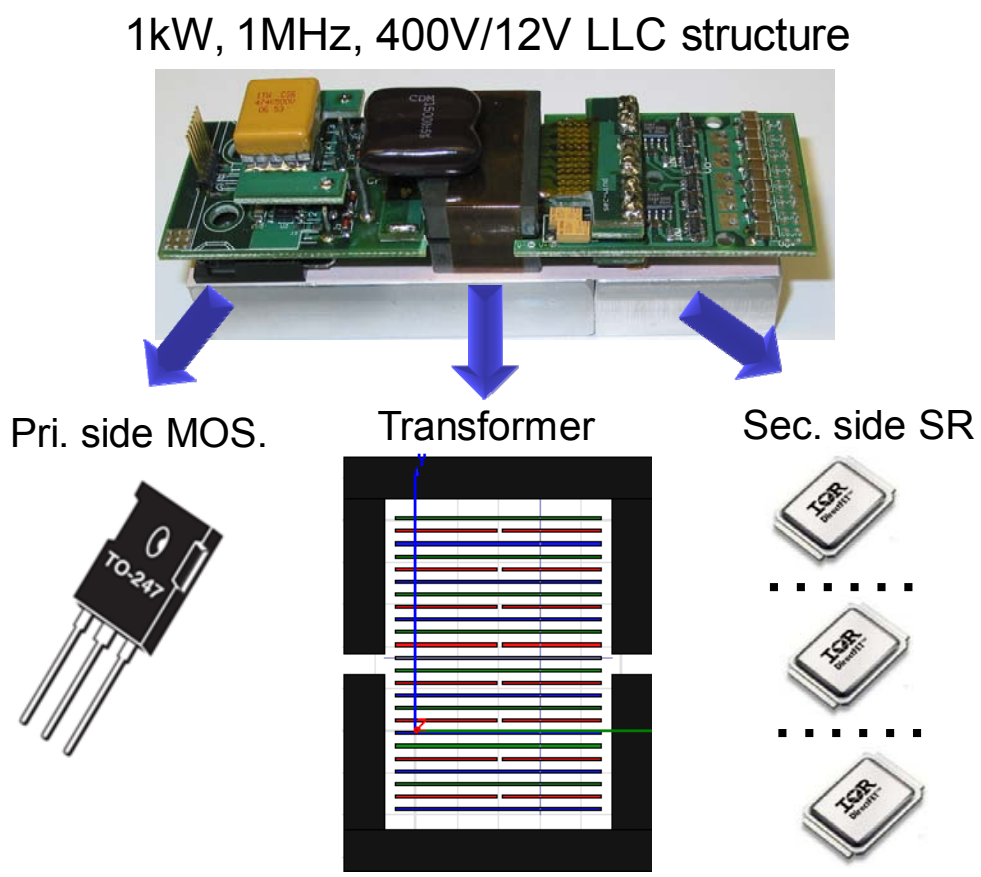


Fig. 4.2. Basic design structure of 1kW, 1MHz, 400V/12V LLC resonant converters with extension of 400V/48V version LLC resonant converters.

For 1kW 48V output LLC resonant converters, the output current is only 20.8A. Thus, one SR is enough to handle the current and there is no SR parallel issue. The current on the secondary side winding is not very high either. Transformer winding design is not a problem. The basic structure of a 1kW 1MHz 400V/48V LLC resonant converter is depicted in Fig. 4.1. However, for 1kW 12V output LLC resonant converters, the output current is substantially increased to 83A. Finding a way to achieve low conduction loss becomes very critical. With the extension of 400V/48V version LLC resonant converters, the basic design structure of 1kW, 1MHz, 400V/12V

LLC resonant converters is shown in Fig. 4.2. More SR devices and more transformer windings are required to handle the high current.

In this chapter, system optimization of LLC resonant converters for low-output-voltage high-output-current applications is investigated. Novel technologies are proposed to improve the efficiency of LLC resonant converters.

4.2 Issues and Challenges of Conventional Design

4.2.1 SR Device Selection

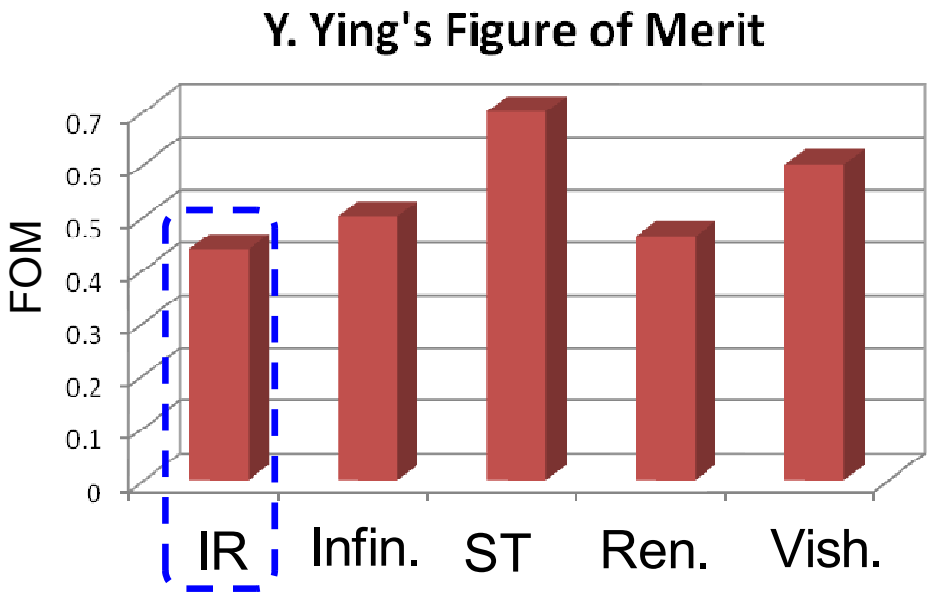


Fig. 4.3. SR selection based on Y. Ying's FOM.

According to Y. Ying's FOM shown in Fig. 4.3, SR from IR can be selected. The output voltage is 12V. Thus, the driving voltage can be directly obtained from the output voltage. The SR losses for different numbers of parallel SRs at a full-load

condition are plotted in Fig. 4.4. To obtain the lowest total loss, the optimal number of SRs in parallel is 4.

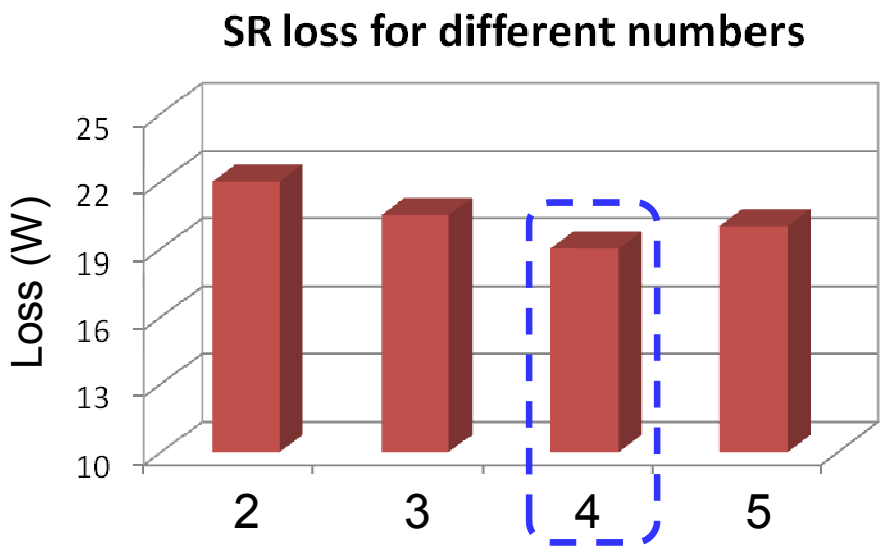


Fig. 4.4. SR loss for different numbers for V_{gs}=*12V* at full-load condition. Based on the lowest loss, 4 is chosen as the suitable number of SRs in parallel.

The conduction loss and driving loss are the major losses. It is very critical to further reduce the losses to improve the efficiency.

4.2.2 Termination Loss and SR Parallel Issues

The transformer of 12V output can be designed with PCB windings. For LLC resonant converters, as shown in Fig. 4.5, it is preferred to utilize the magnetizing inductance as one of resonant inductors. Thus, a gap is needed to generate the desirable magnetizing inductance. The planar PCB transformer winding structure is adopted and is shown in Fig. 4.7. To reduce eddy current loss, the primary side and the secondary side windings are placed with interleaving structure.

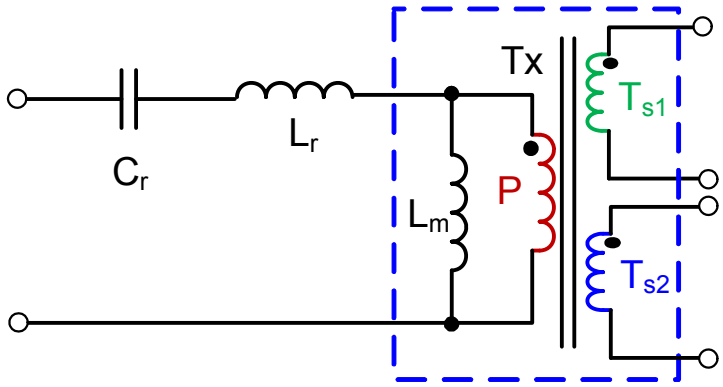


Fig. 4.5. Center-tapped transformer of LLC resonant converters with integration of magnetic inductance.

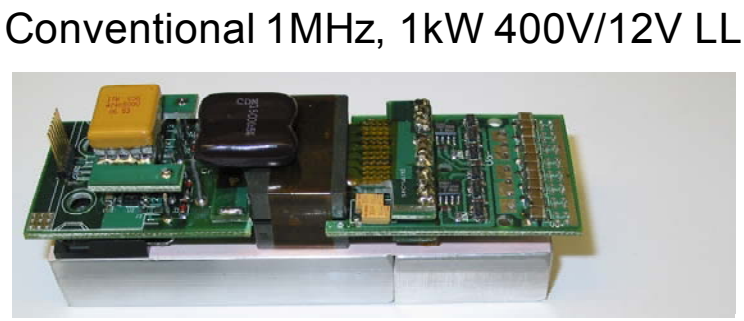


Fig. 4.6. 1kW, 1MHz, LLC resonant converters.

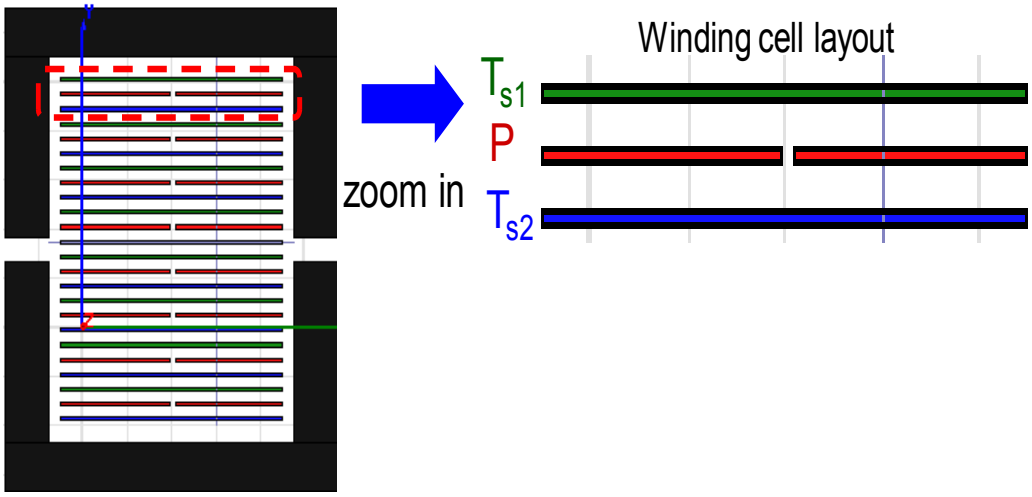


Fig. 4.7. Basic transformer structure for 12V output LLC.

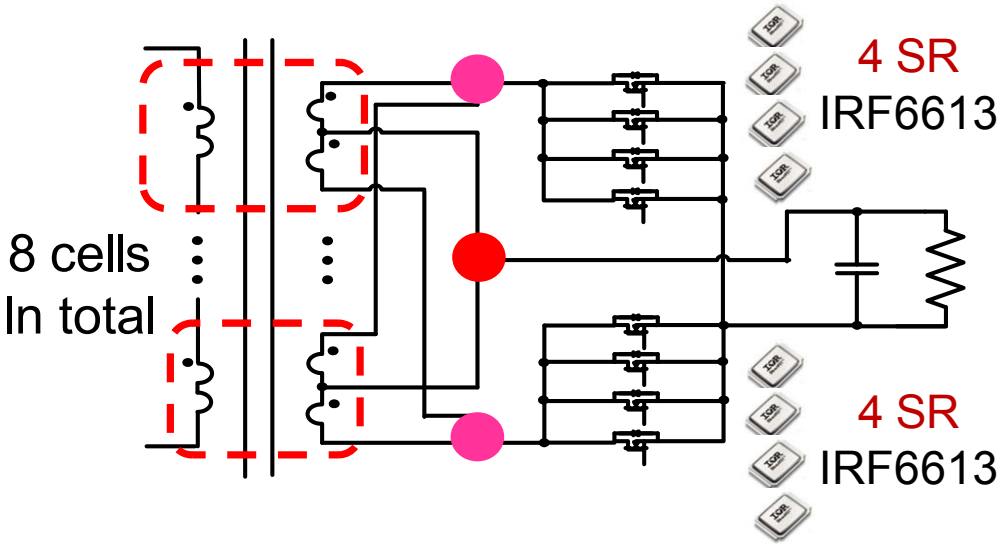


Fig. 4.8. Basic transformer and SR structure for 12V output LLC.

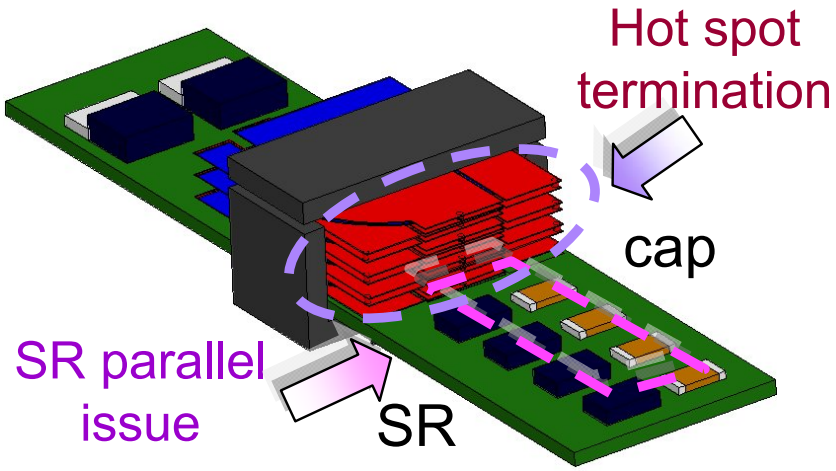


Fig. 4.9. Terminations of conventional transformer and the secondary side structures.

The conventional planar transformer and the secondary side structure are depicted in Fig. 4.9. The current distribution of the termination is shown in Fig. 4.10. Due to the proximity effect and the skin effect, the currents in adjacent terminals with opposite directions attract each other. Thus, very high losses and hot spots are generated. According to the FEA result, there is 6.5W loss at the winding terminals for 1kW,

1MHz, 400V/12V LLC resonant converters. This termination loss significantly deteriorates the efficiency. High termination loss is a barrier to improving the system efficiency.

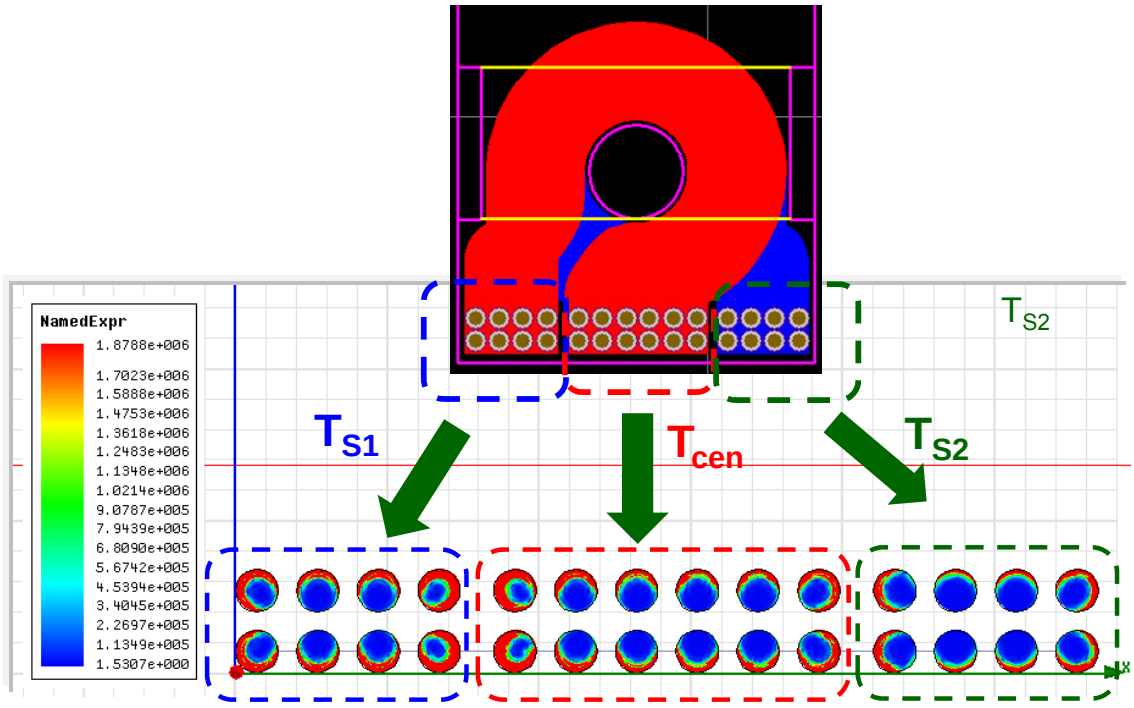


Fig. 4.10. Current distribution of termination for the conventional transformer design.

On the other hand, to reduce the high current conduction loss, a large number of SRs should be paralleled. For the conventional design, all SRs are placed on the mother board. Physically speaking, large loop of the secondary side rectifiers is inevitable. Although multi-layer printed circuit board (PCB) with heavy coppers can reduce dc conduction loss, there is little effect in reducing the high-frequency ac losses. Consequently, a large distribution loss will be generated. In addition, for a large number

of SR devices, it is extremely difficult to achieve symmetrical layout for each SR. Hence, current sharing of the SRs is a severe problem.

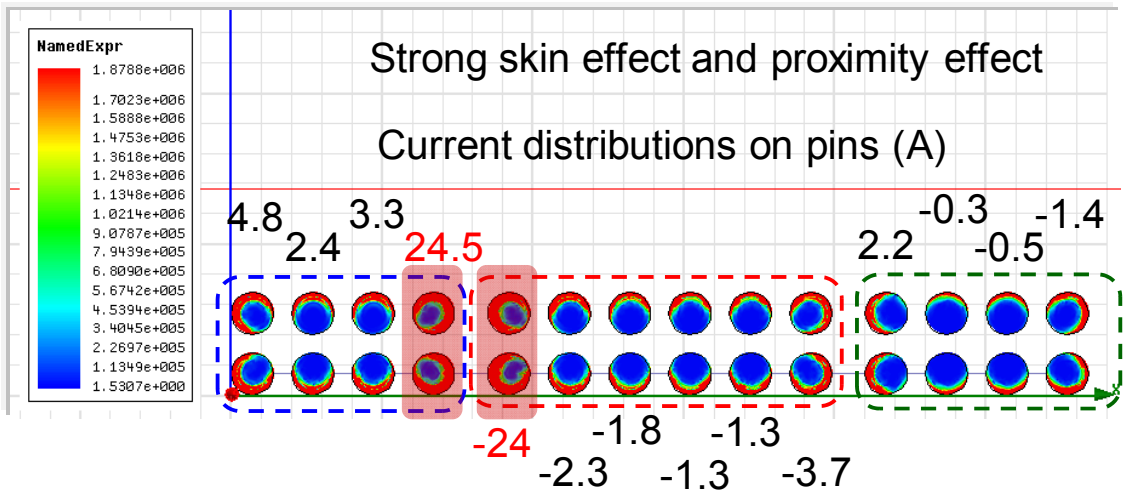


Fig. 4.11. Current distribution of termination for the conventional transformer design.

4.2.3 Winding Loss Issues for Conventional Transformer Design

An interleaving structure is applied to alleviate ac winding loss. The primary side winding has 16 turns, which are placed in 8 PCB layers. Each secondary side winding consists of 8 parallel layers. Normally, magnetizing inductance is used to achieve ZVS and designed as a small value. A large gap is normally applied to achieve the desirable magnetizing inductance. However, due to the large gap, fringing flux penetrates the PCB winding. Hence, very high eddy current is generated. The high winding loss is unavoidable due to strong fringing effect. Therefore, excessive winding loss is generated. Based on the FEA result, there is very high winding loss. This is detrimental to achieve high efficiency.

From Fig. 4.12, it can be observed that most of the winding loss comes from the PCB layers close to the gap.

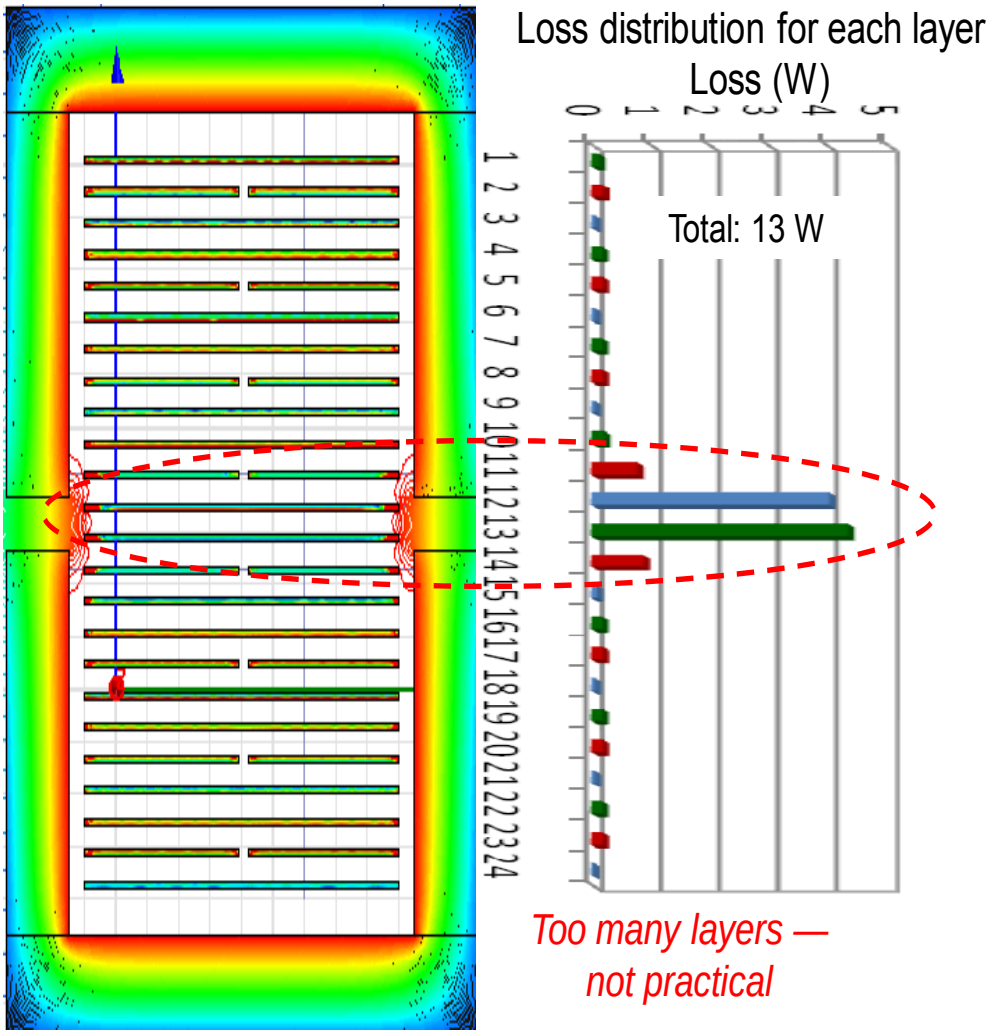


Fig. 4.12. Current, loss and flux distribution of the conventional transformer design with gap and integration of L_m.

The value of the magnetizing inductance is determined by the transformer gap design. For the target 1kW, 1MHz LLC resonant converter, the required magnetizing inductance is 16μH, and the associated gap distance is 1mm. If the gap distance is

reduced by 20%, the magnetizing inductance is increased to 18 μH. Due to the short gap distance, the fringing effect is reduced. From the detail FEA analysis, it can be observed that the fringing flux is considerably reduced. Also, a small gap leads to higher magnetizing inductance. Higher magnetizing inductance means less magnetizing current. Thus, the primary side current will be reduced also, and the induced eddy current will be less. As a result, 14% winding loss can be saved.

An increase of the gap distance leads to a higher winding loss. If the gap distance is increased by 20%, 12% more winding loss is generated.

The relationship of winding loss, gap distance and magnetizing inductance are shown in Fig. 4.13. With a larger gap and smaller magnetizing inductance, the winding losses increase rapidly.

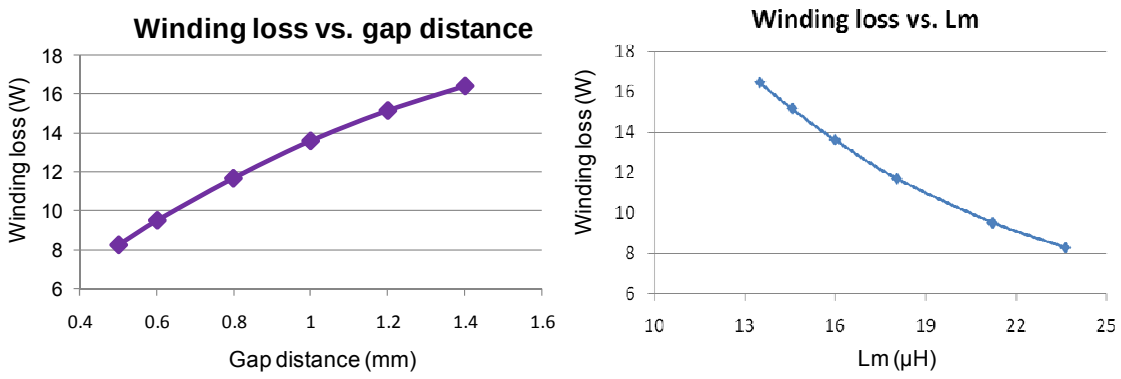


Fig. 4.13. Winding loss comparison for different gaps and L_m.

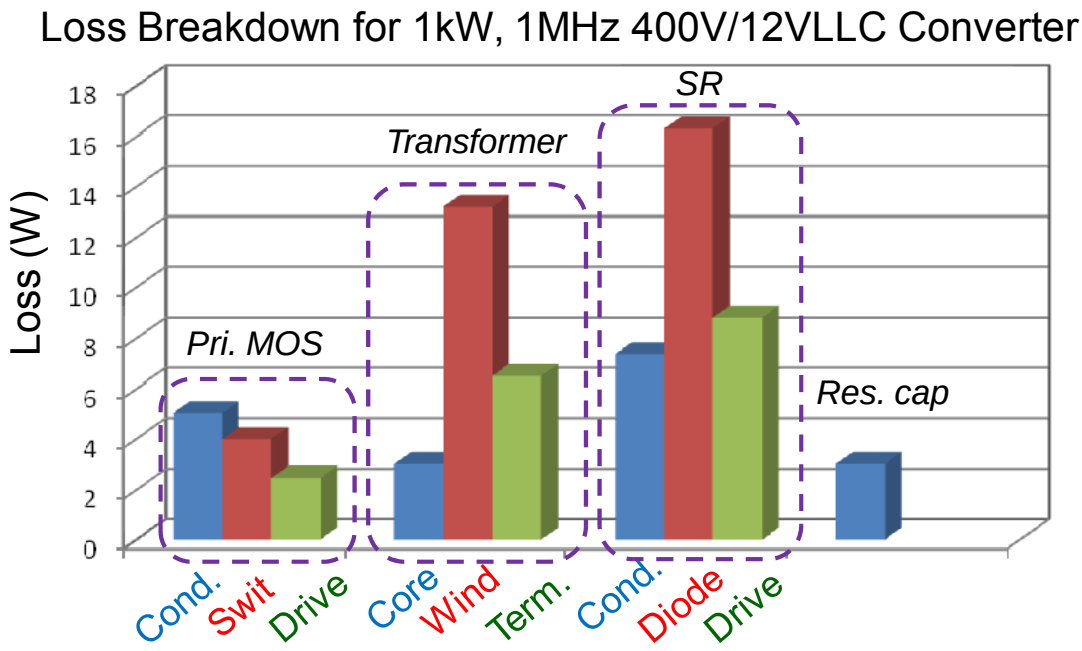


Fig. 4.14. Loss breakdown of conventional 1kW 1MHz 400V/12V LLC resonant converters.

The impacts of magnetizing inductance have been studied. To reduce the winding loss, it is preferred to achieve large magnetizing inductance with smaller gap. However, because the magnetizing inductance is normally determined by the whole system design, it is not convenient to change the magnetizing inductance in some circumstances. Other methods should be investigated for loss reduction.

The loss breakdown of conventional 1kW 1MHz 400V/12V LLC resonant converters is shown in Fig. 4.14. It can be observed that more than 79% of the losses come from the secondary side due to very high secondary side current. It should be noted that the SR is driven with a commercial voltage-sensing method. Therefore, reducing and optimizing the secondary side losses becomes extremely critical for low-voltage front-end dc-dc converters.

4.3 SR Optimization Design

4.3.1 SR Device Selection Improvement

Y. Ying's FOM is used to choose SR devices in a conventional design procedure. However, Y. Ying's FOM is derived based on hard-switching PWM converters. Thus, it is not preferable for soft switching resonant converters. The improved FOM of SR for resonant converters is proposed in Chapter 2.

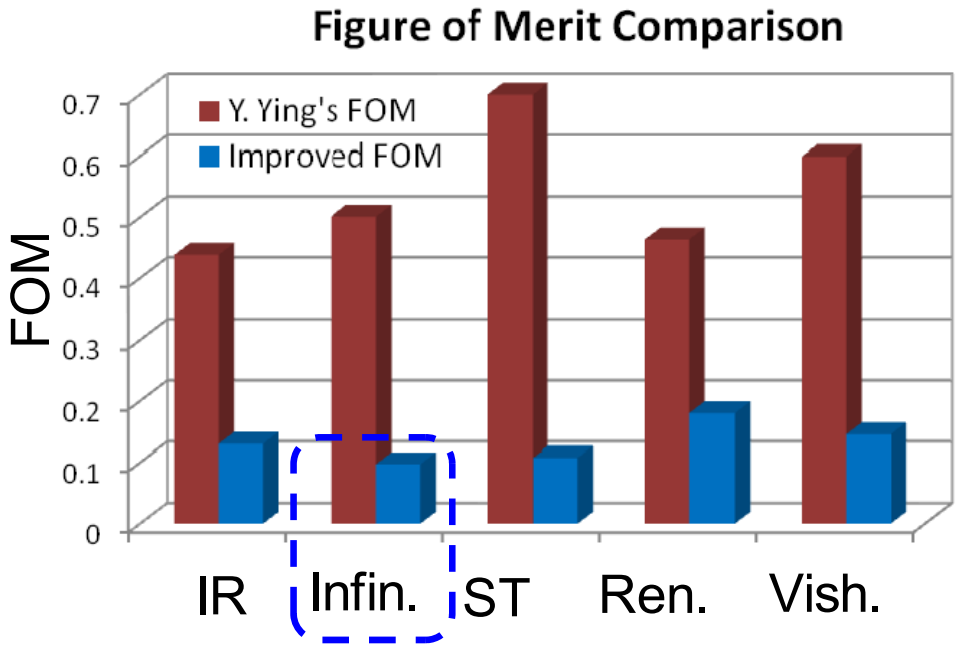


Fig. 4.15. SR device comparison based on Y. Ying's FOM and the improved FOM.

According to Y. Ying's FOM, SR devices from IR outperform SRs from other vendors. Based on the proposed improved FOM of SR for LLC resonant converters, the performance of currently available SRs from different vendors are shown in Fig. 4.15. Results of Y. Ying's FOM are also shown in Fig. 4.15. Different FOMs lead to different results. Thus, the device selection for soft-switching applications is very different from

the hard-switching applications. Because it has the lowest FOM, the IR6613 SR devices are replaced with Infineon devices.

4.3.2 SR Driving Voltage and SR Parallel Number Optimization

SR driving voltage is a critical factor that determines both conduction loss and driving loss. Thus, SR driving voltage optimization should be studied thoroughly.

It is preferred to achieve high efficiency over a wide load range, such as at 20%, 50% and 100% load conditions. The SR should be optimized accordingly.

To address the load related loss, the SR loss percentage is defined below:

$$\delta_{SR} = \frac{P_{loss\_SR}}{P_o} = \frac{I_{rms\_SR}^2 R_{on\_SR} + Q_{g\_SR} V_{gs\_SR} f_s}{P_o} \tag{4.1}$$

To achieve the highest efficiency, apparently, lowest SR loss percentage should be obtained.

The optimization target is to achieve the lowest SR loss percentage over wide load range.

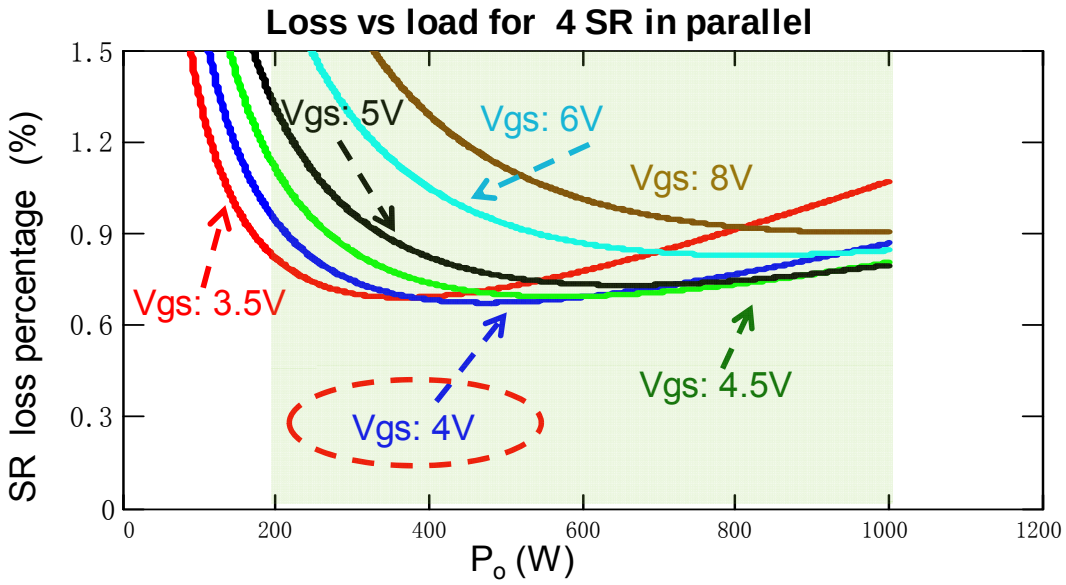


Fig. 4.16. SR loss percentage vs. power with different SR driving voltages. Vgs=4V is chosen as the optimal driving voltage to achieve highest efficiency over wide load range.

To achieve the lowest SR loss percentage, different SR driving voltages are swept and shown in Fig. 4.16. $V_{gs\_SR}=4V$ is finally chosen as the optimal driving voltage to achieve the lowest SR loss over the wide load range.

Similarly, as shown in Fig. 4.17 and Fig. 4.18, the optimal driving voltage can be obtained for different SR parallel number. *Vgs=4.5* is chosen for three SRs in parallel. *Vgs=3.7V* is chosen for five SRs in parallel.

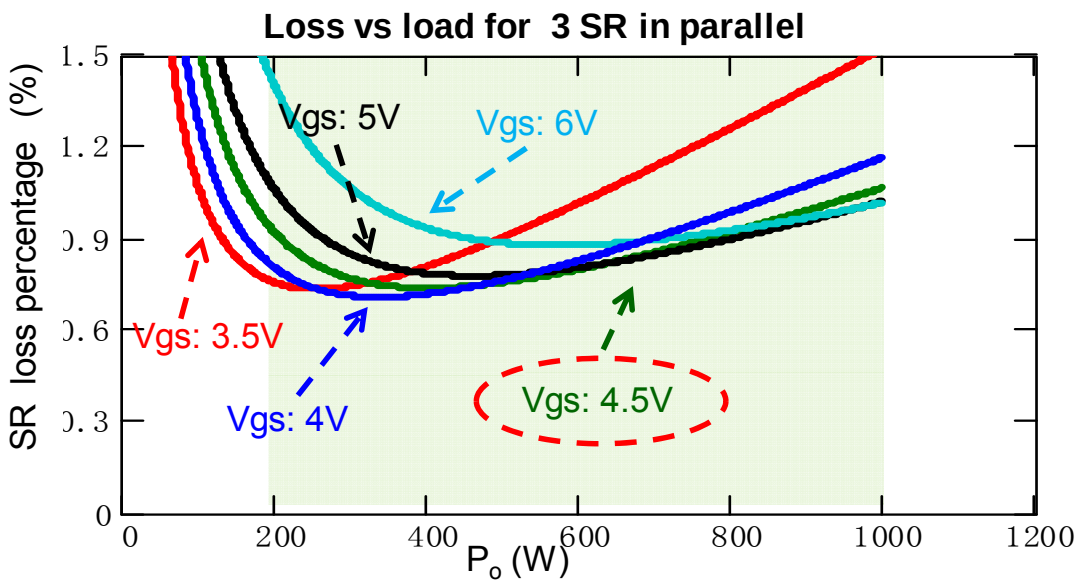


Fig. 4.17. SR loss percentage vs. power with different SR driving voltages for three SRs in parallel.

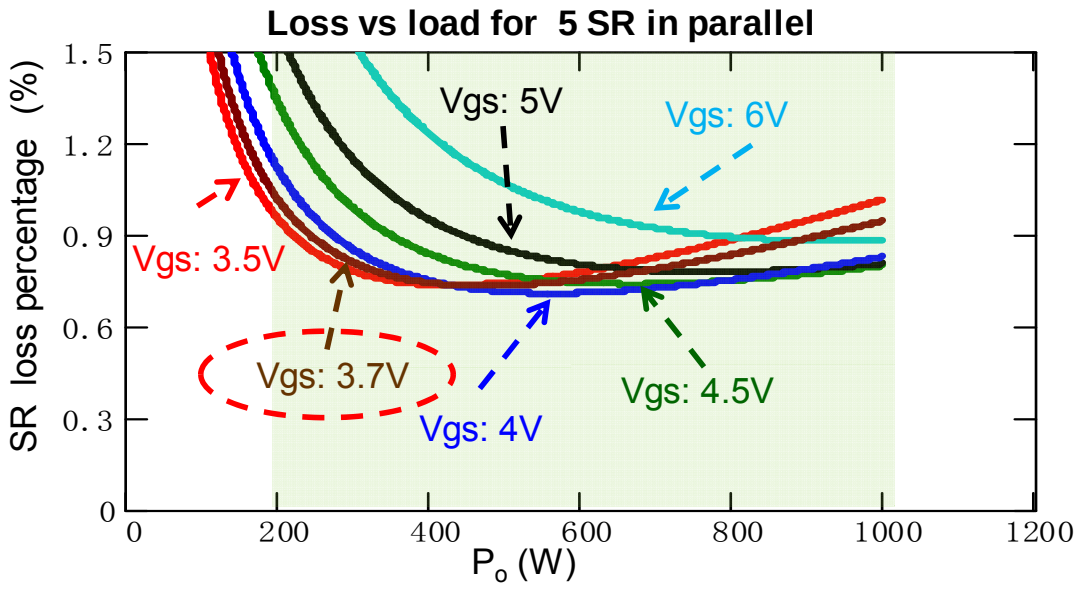


Fig. 4.18. SR loss percentage vs. power with different SR driving voltages for five SRs in parallel.

The SR loss results with different numbers of SRs are compared in Fig. 4.19. For a 1kW converter, four SRs should be used to achieve low loss over a wide load range.

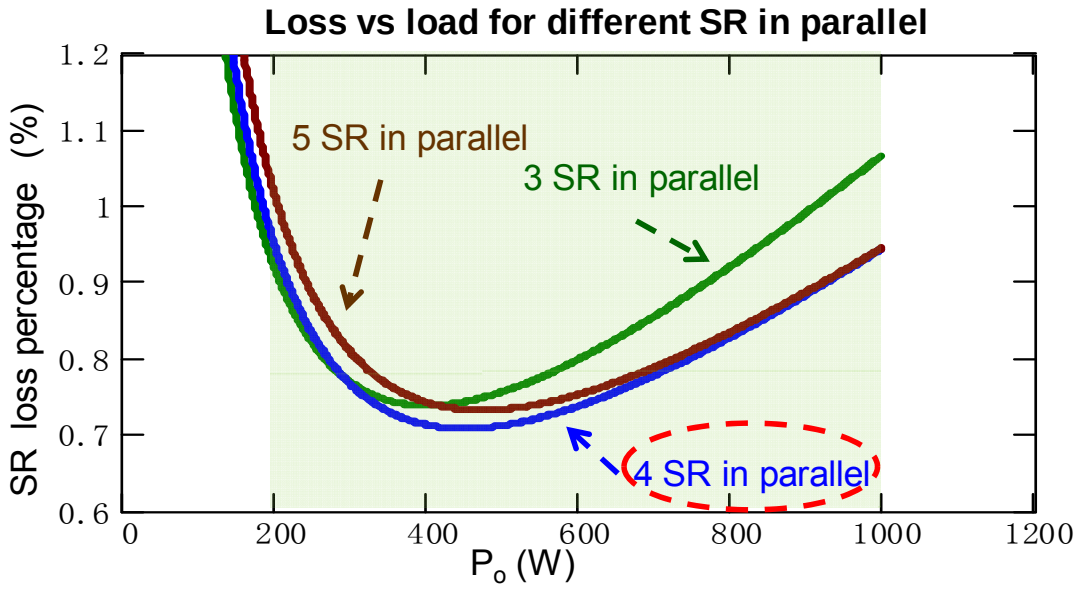


Fig. 4.19. SR loss percentage vs. power with different SR parallel number.

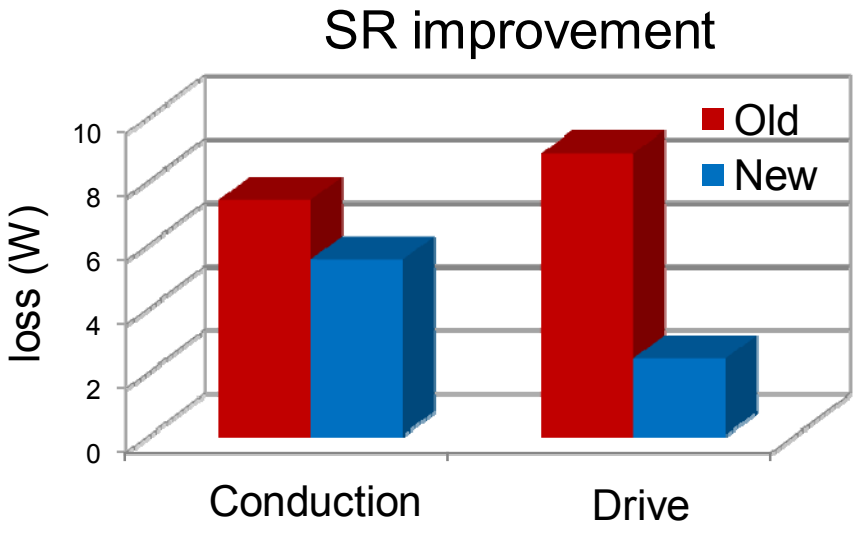


Fig. 4.20. SR optimization comparison.

Finally, SR improvements results are shown in Fig. 4.20. According to the improved FOM, the optimal SR devices are chosen. The optimization of the SR driving voltage

and SR parallel number further reduces the conduction loss and driving loss. Therefore, considerable loss reduction is accomplished.

4.4 Transformer Structure & Secondary Side Winding Structure Optimization

With a conventional termination configuration, conduction loss is very high due to a strong proximity effect. In [G.1], the interleaving termination approach was proposed to reduce the ac termination loss. With an interleaving termination scheme, the current can be distributed more evenly among the termination pins. Thus, lower conduction loss can be attained. However, the design of the interleaving termination is very complicated. Terminations should be interleaved many times to effectively reduce the proximity effect. The clearance areas between the interleaving terminals are relatively large. There is less copper close to the termination regions; hence, more conduction loss may be generated. More importantly, for a center-tapped transformer structure, three terminals are adopted. An interleaved termination design becomes quite difficult and may be impractical in some cases, especially in a planar PCB transformer design.

In [G.2], a PCB winding concept is proposed. As shown in Fig. 4.21, the secondary side winding is integrated with the device PCB board. Hence, for secondary side windings, there is no ac termination, so the termination loss can be reduced significantly.

According to the device PCB concept, the transformer structure can be redesigned and is plotted in Fig. 4.22. Thus, the high ac termination loss can be reduced. The SR parallel problems can also be alleviated.

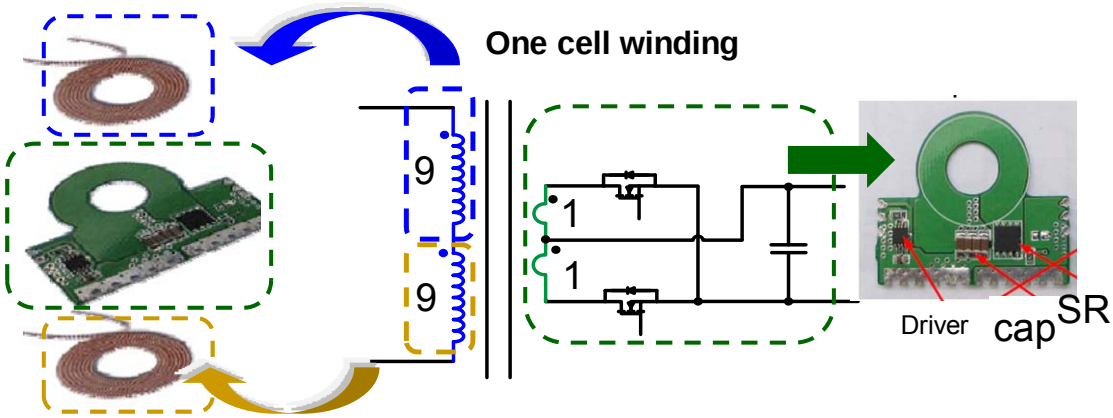


Fig. 4.21. One cell of PCB winding structures.

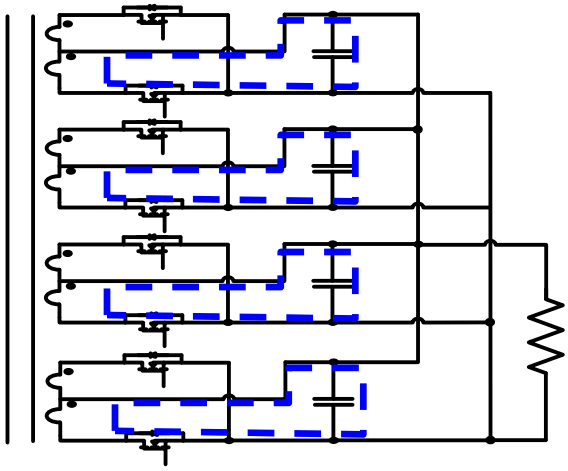


Fig. 4.22. Improved transformer structure with device PCB windings.

In [G.2], SRs with 3.5 mΩ are selected. Due to the large resistance, eight cells are required for 1200W converters. In the previous section, an improved device FOM is used to select SRs. SRs with 1.6 mΩ are selected based on the new FOM. Thus, only

four cells are needed for target 1kW converters. The whole improved secondary side structure is shown in Fig. 4.23.

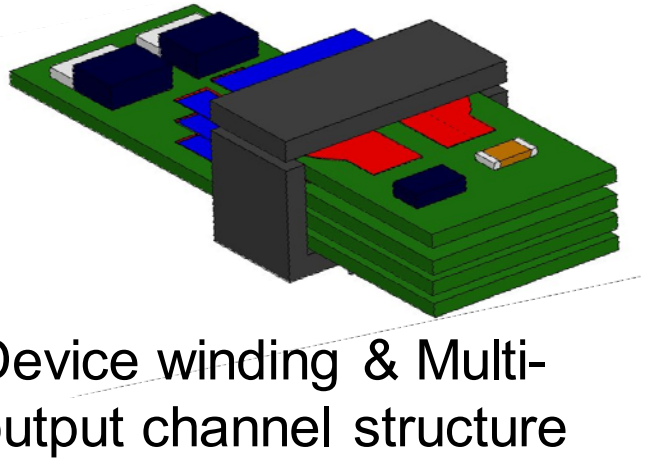


Fig. 4.23. The improved device winding & multi-output channel structure.

4.5 Transformer Winding Loss Reduction and Optimization

Litz wires are widely applied for high frequency applications. Litz wires are not sensitive to internal and external flux. Thus, the litz wire can be applied to alleviate the fringing effect losses. In [G.2], a PCB winding combined with litz wire winding is proposed; this is shown in Fig. 4.24. The primary side windings are interleaved with the secondary side windings to reduce ac winding loss. For each cell, two sets of primary side windings are used. Each set of primary side windings consists of 18 turns, which are wound in two layers. The two 18-turn primary side windings are then paralleled to complete one cell. To finish the whole transformer winding structure, 8 cells of such mini-sandwich windings are applied. As a result, a 16-layer PCB and 144turns of the primary side windings are used.

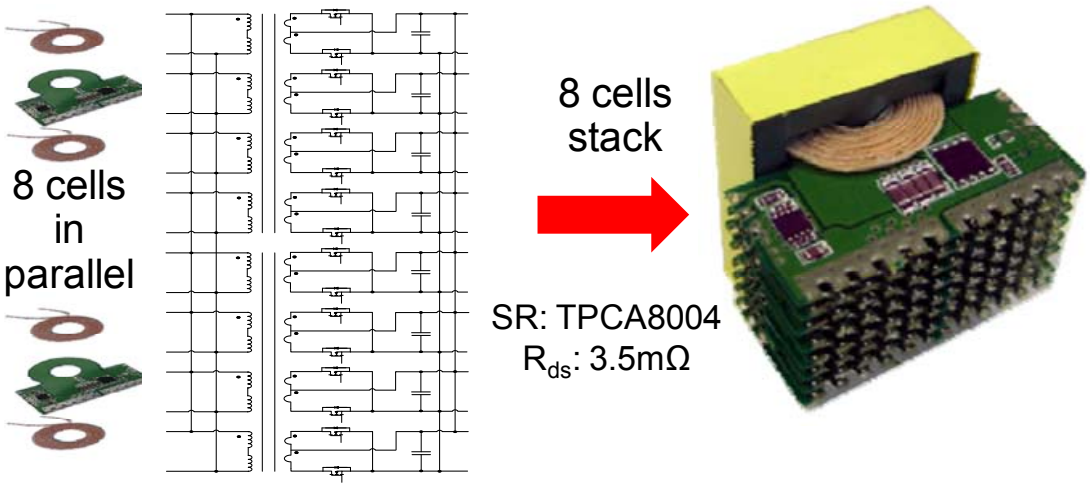


Fig. 4.24. PCB winding structures without ac winding termination.

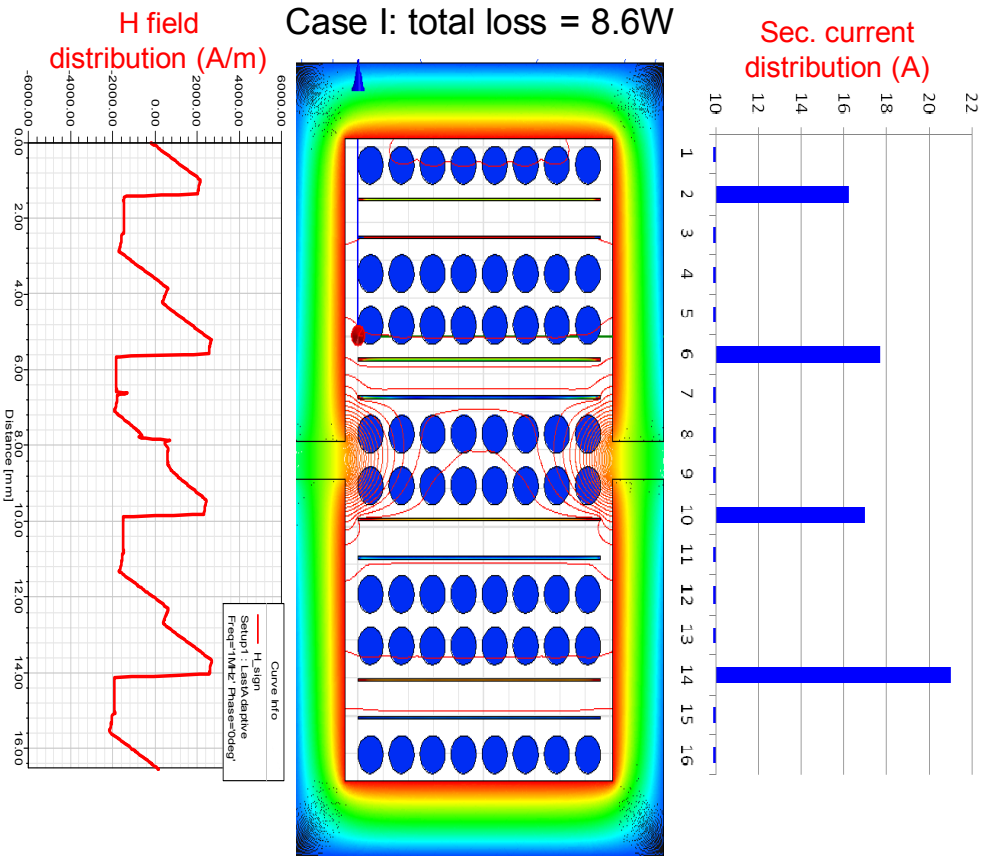


Fig. 4.25. Current and flux distribution of transformer structure case I.

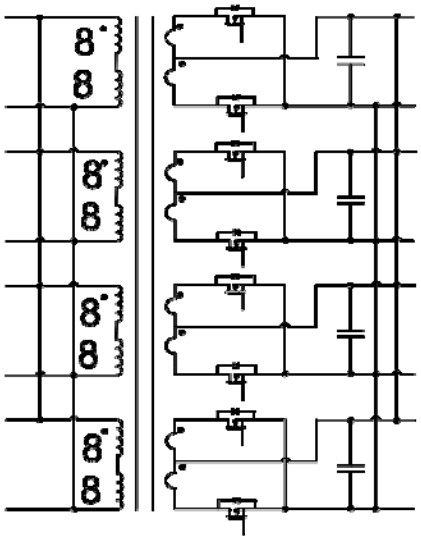


Fig. 4.26. Transformer structure without ac winding termination, case I.

In the previous section, based on the proposed improved FOM of SR, the optimal SR device has been identified. Based on the SR number and driving voltage optimization, the optimal number of SRs is 4, and the optimal driving voltage is 4V. Thus, for a 1kW converter, four sets of SR device windings are necessary.

Following the concept of transformer configuration in [G.2], the circuit schematic of the transformer winding structure is drawn in Fig. 4.26. Due to improvement of SR, the winding cells can be reduced to four sets.

Because the PCB windings are placed far from the gap, much less eddy current is induced. Thus, the winding loss is considerably reduced. The winding loss comparison for conventional design and the improved design is drawn in Fig. 4.27.

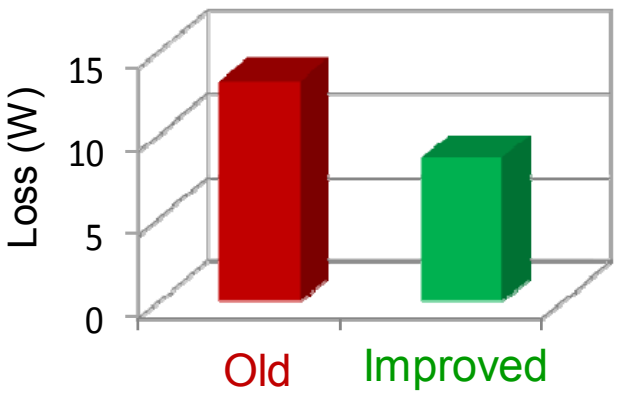


Fig. 4.27. Improvement of winding loss reduction with combined litz wire and PCB winding structure.

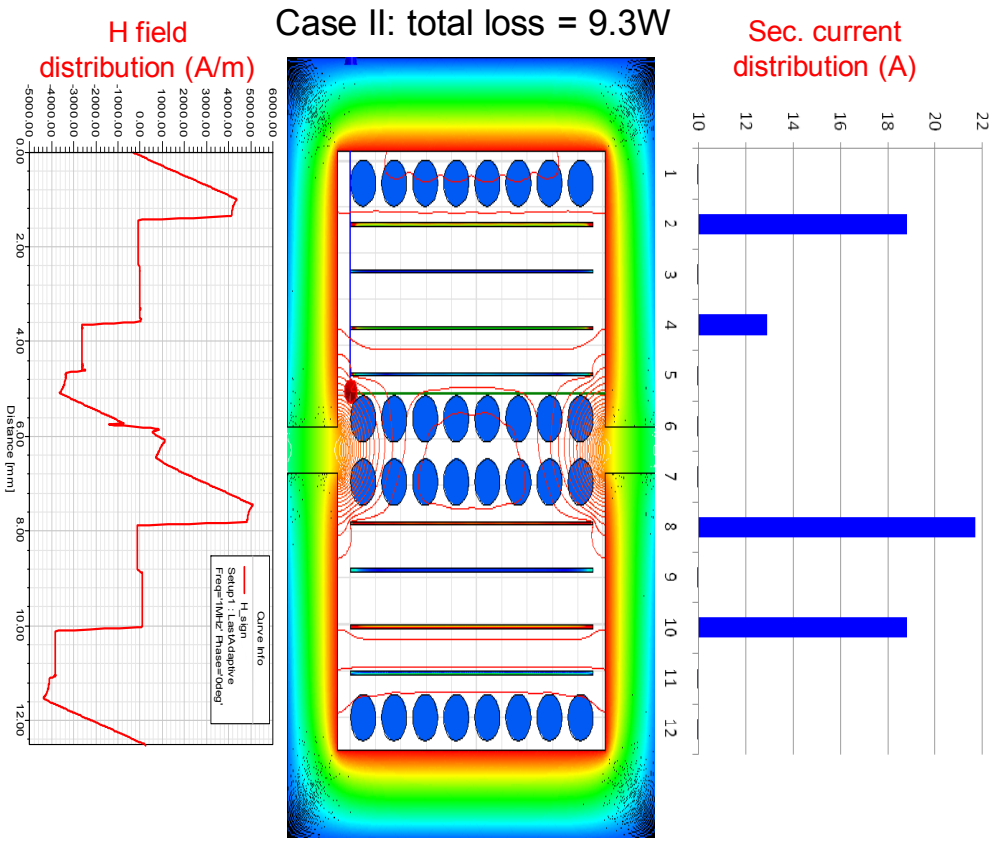


Fig. 4.28. The simplified transformer structure, case II.

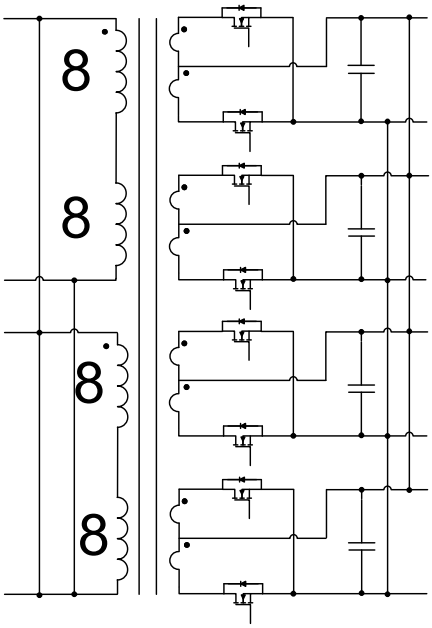


Fig. 4.29. The circuit schematic of the simplified transformer structure, case II.

However, for this structure, there are some limitations. The winding structure is highly complicated. Also, the secondary side current sharing is not good. Thus, further improvement is necessary.

Actually, the interleaving structure can be simplified to that shown in Fig. 4.28. The circuit schematic of transformer winding structure is drawn in Fig. 4.29. The transformer winding structure becomes simpler, which leads to many fewer winding connection efforts.

With less interleaving structure, magneto-motive force (MMF) is increased. The winding loss increases 0.7W. For a 1kW converter, this is acceptable. Because the winding loss related to fringing effect has been greatly reduced, the increase of winding

loss due to less interleaving and higher MMF is not very significant. It is worthwhile to adopt a simple structure with easy connections.

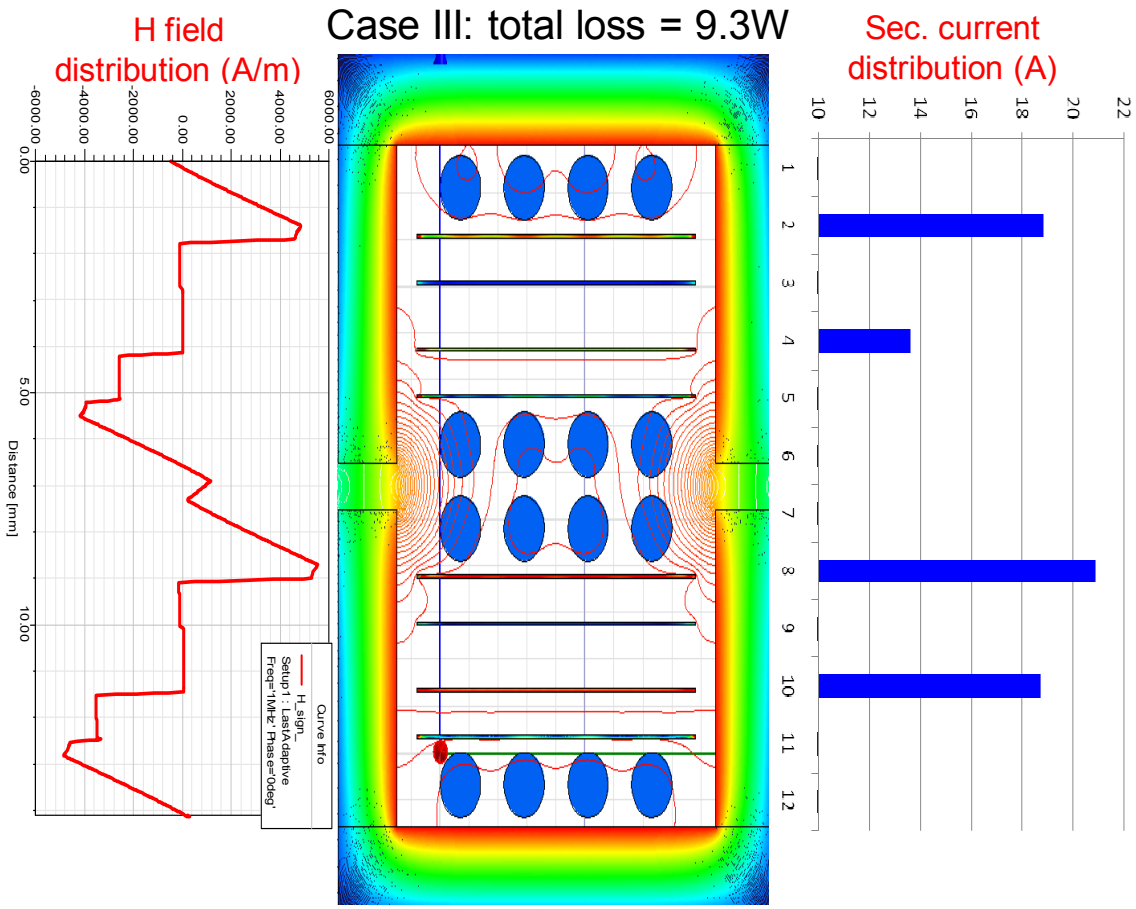


Fig. 4.30. The more simplified transformer structure, case III.

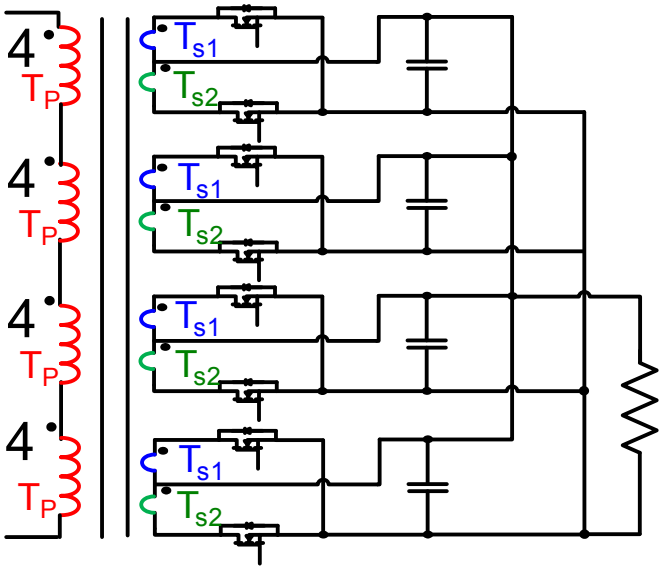


Fig. 4.31. The circuit schematic of more simplified transformer structure, case III.

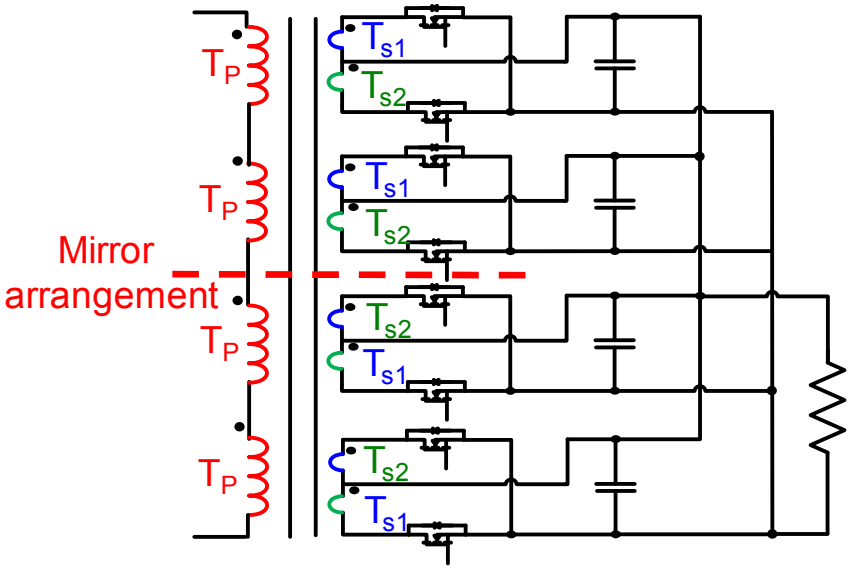


Fig. 4.32. The circuit schematic of improved simplified transformer structure, case IV.

A more simplified transformer structure is shown in Fig. 4.30. The circuit schematic of transformer winding structure is drawn in Fig. 4.31. In this case, all primary side

windings are straight forward connected in series, which is the simplest winding configuration. Comparing case II and case III, we can see that the MMF does not change much. As a result, no extra loss is generated.

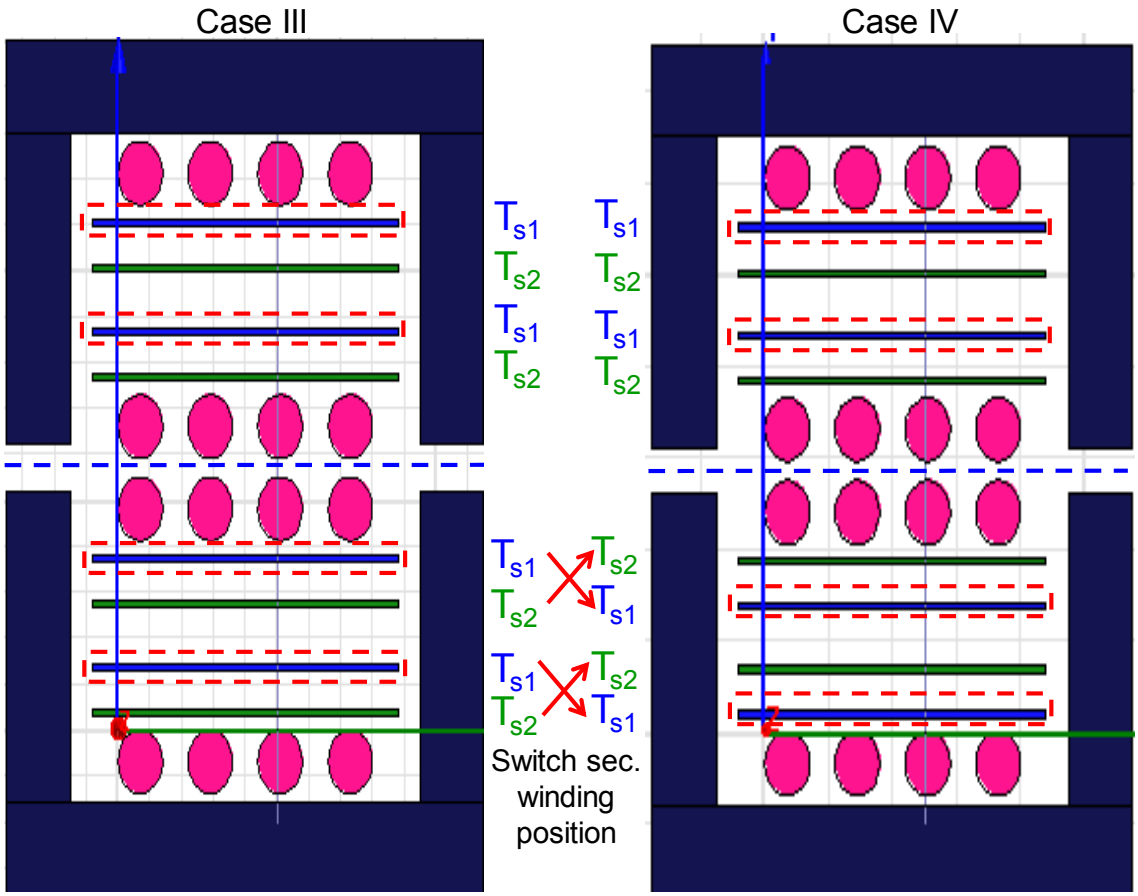


Fig. 4.33. The layout comparison of the proposed improved transformer structure, case IV.

The problem with the case III structure is the uneven current sharing among the secondary side windings. Due to unsymmetrical winding configuration, the secondary side windings carry different current. To achieve more evenly distributed current, the secondary side winding structure can be modified. As plotted in Fig. 4.32 and Fig. 4.33, respectively, the position of secondary side windings can be switched. Thus, the

transformer windings become symmetrical, and better current sharing among the secondary side windings can be achieved. The FEA result is shown in Fig. 4.34. The winding loss is reduced when compared with the case III structure.

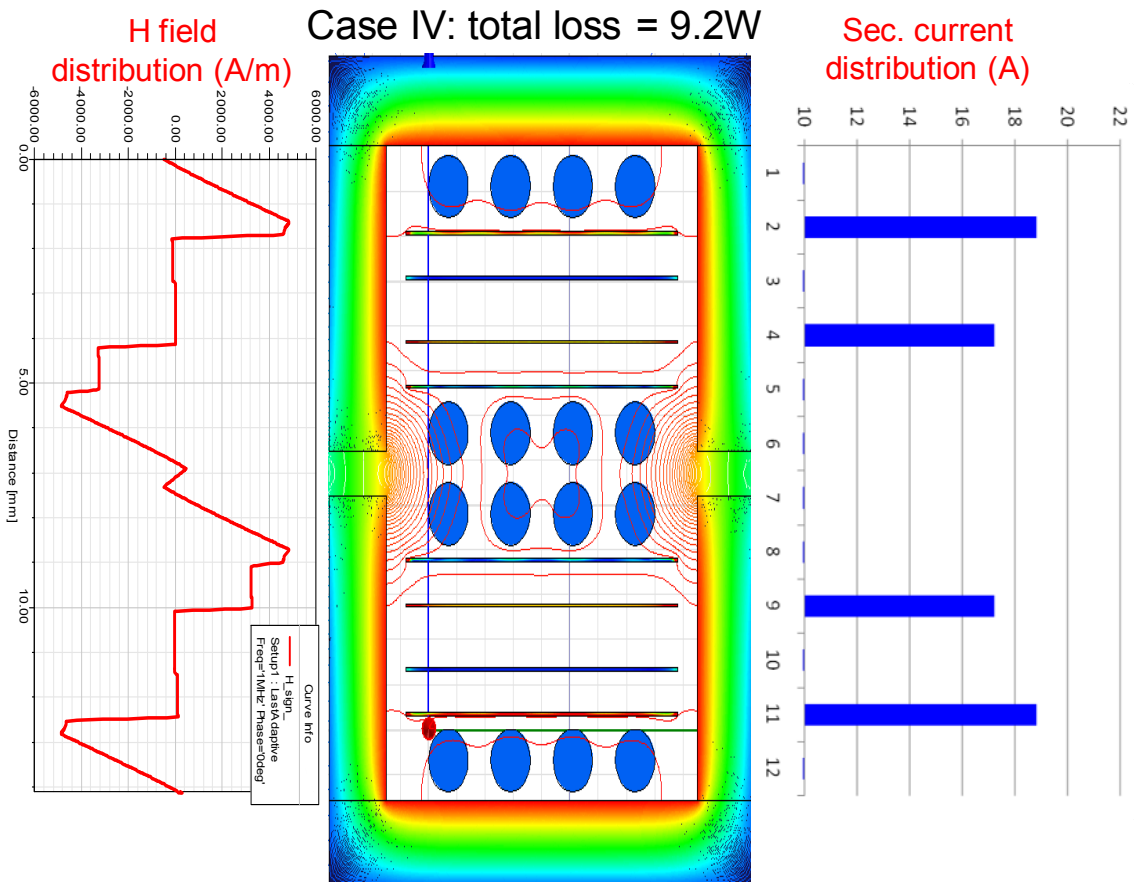


Fig. 4.34. The current distribution, flux and H field distribution of the proposed improved transformer structure case IV, which is finally chosen as the optimal structure.

Finally, the improved structure of case IV is chosen as the optimal winding structure.

The proposed improved transformer winding structure has several merits:

(1) Because the SR devices and the output capacitor filter are directly placed on each winding plate, the ac termination loss is considerably reduced.

(2) Litz wires are applied to reduce winding loss, which is induced by fringing flux. The primary side windings are placed in series and can be interleaved with the secondary side windings. Simple primary side connection is achieved.

(3) The transformer winding structure is designed symmetrically. More even current sharing is accomplished on the secondary side. This is also beneficial to current sharing among SR devices.

Reference [G.3] studies winding loss reduction for gapped inductors, and proposes to reduce winding loss by reshaping the winding structure. In [G.3], the areas close to the gaps are designated as the "keep-away" regions, and the 2D FEA tool is used to explore general rules for defining an appropriate keep-away region for a given core. This concept can be also applied to the transformer design of LLC resonant converters.

Because the most of the fringing flux has been avoided by placing the PCB winding far from the gap, it is easy to further reduce the fringing effect loss by reshaping the PCB winding. Shown in Fig. 4.35, the winding loss can be reduced by slightly cutting the copper adjacent to the gap.

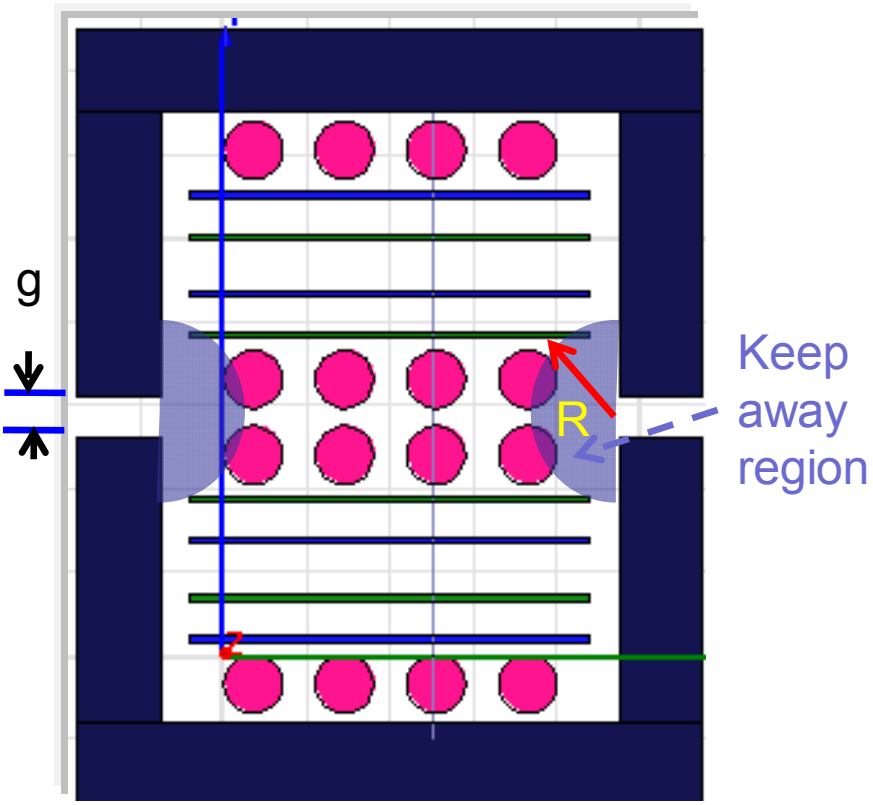


Fig. 4.35. Winding reshape concept to reduce the fringing effect losses [G.3].

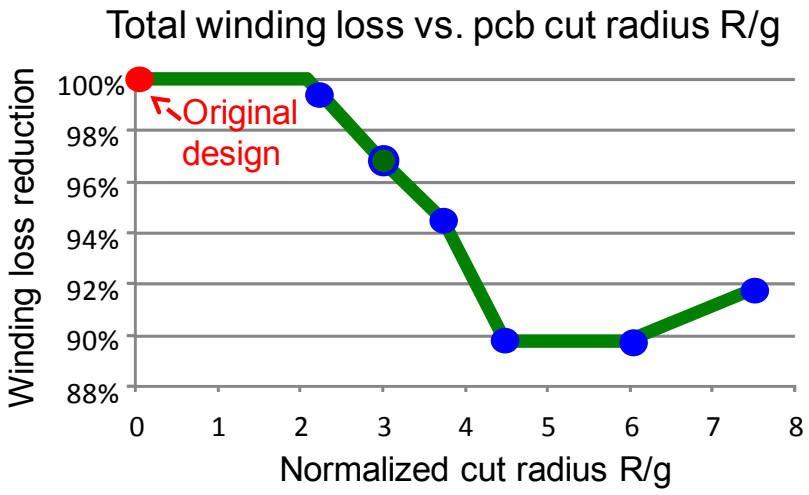


Fig. 4.36. Winding loss reduction vs. normalized reshape radius.

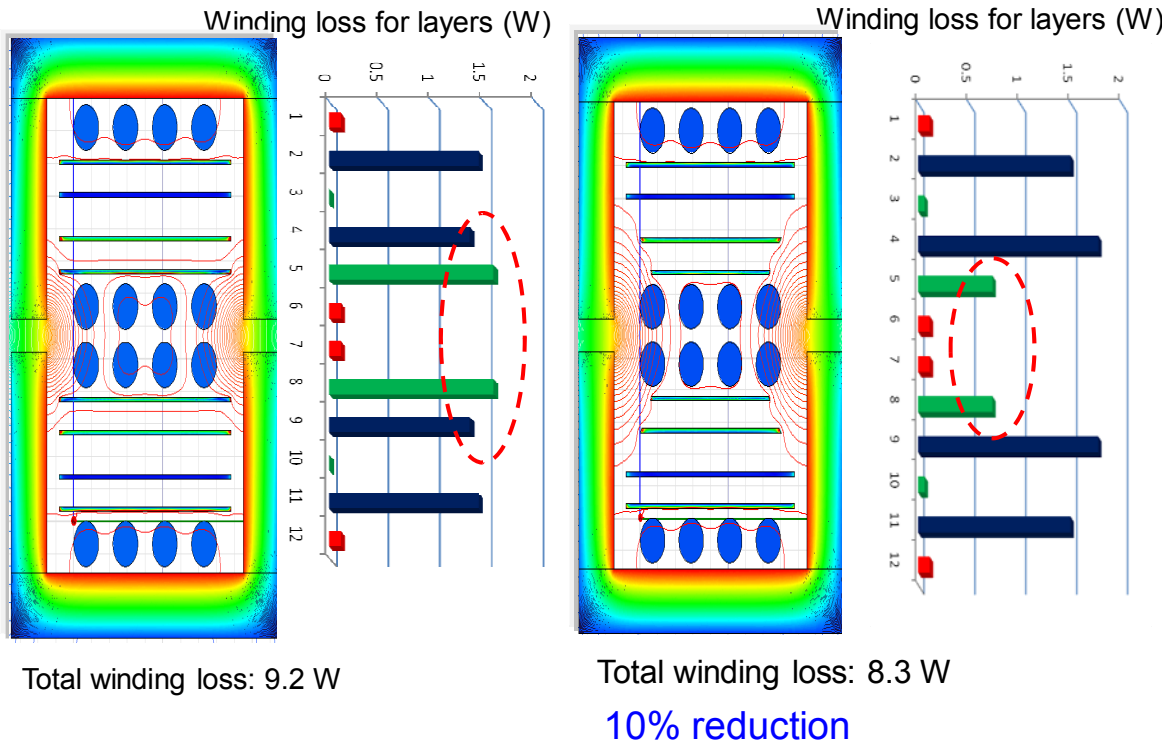


Fig. 4.37. Winding loss comparison with and without winding reshape.

The winding loss optimization result is illustrated in Fig. 4.36. With more of a cutting area of copper, the winding areas with very high current density can be avoided. Therefore, lower winding loss can be achieved. However, excessive copper leads to a higher overall winding resistance. Therefore, there is an optimal cutting area range. Within this range, the winding loss can be reduced effectively.

Fig. 4.37 illustrates the detail FEA result. Apparently, less fringing effect loss benefits the winding loss reduction, and a 10% winding loss reduction can be accomplished. It should be noted the virtual 'cutting' can be easily achieved in the initial PCB winding layout. Thus, there is no manufacturing problem.

The winding loss improvement is shown in Fig. 4.38.

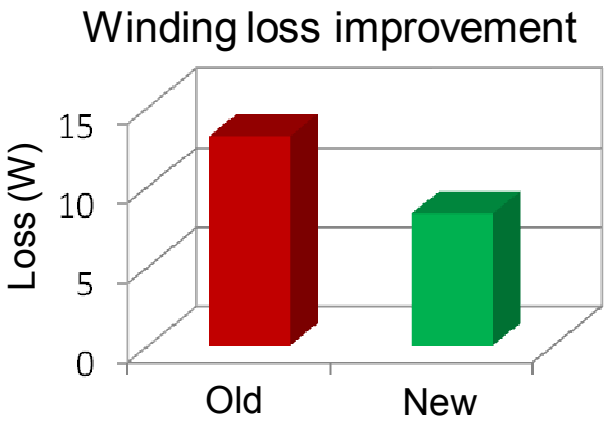


Fig. 4.38. Winding loss improvement results.

4.6 Investigation of Series Resonant Inductance Integration

For LLC resonant converters, there are three magnetic components. To meet the power density requirement, it is preferable to apply magnetic components integration. As shown in Fig. 4.39, it is very attractive to integrate all the magnetic components into one. Thus, fewer magnetic components, smaller passive components, and simple connection can be achieved.

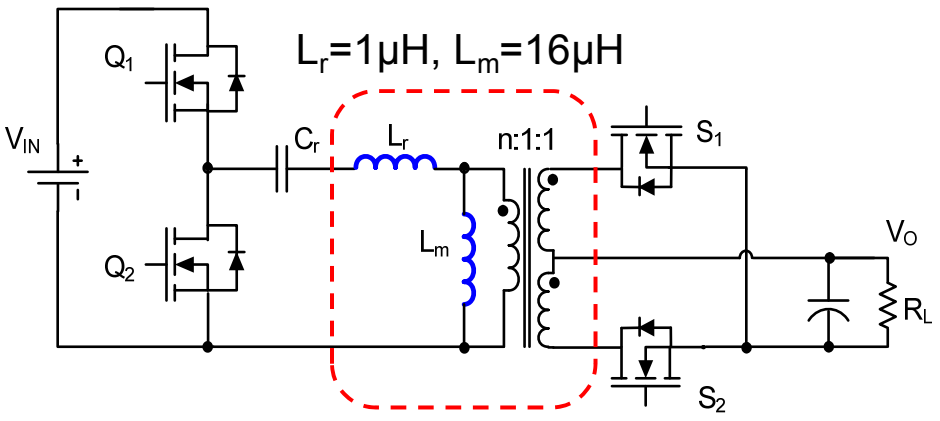


Fig. 4.39. LLC magnetic components integration with transformer, magnetizing inductance and leakage inductance.

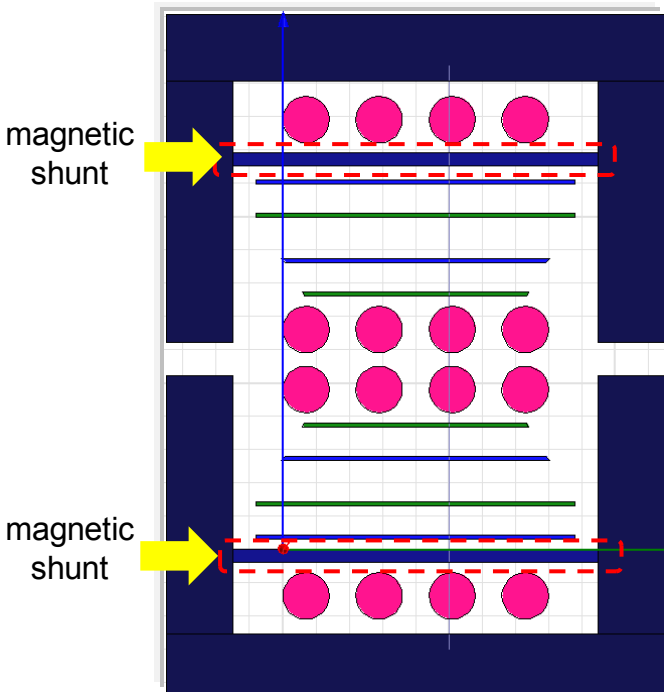


Fig. 4.40. Integration of Lr with insertion of magnetic shunt layer.

The impacts of integration of magnetizing inductance have been discussed. To reduce the winding loss, it is preferred to achieve a large magnetizing inductance with smaller gap. Winding and reshaping techniques can reduce the adverse effect of fringing flux.

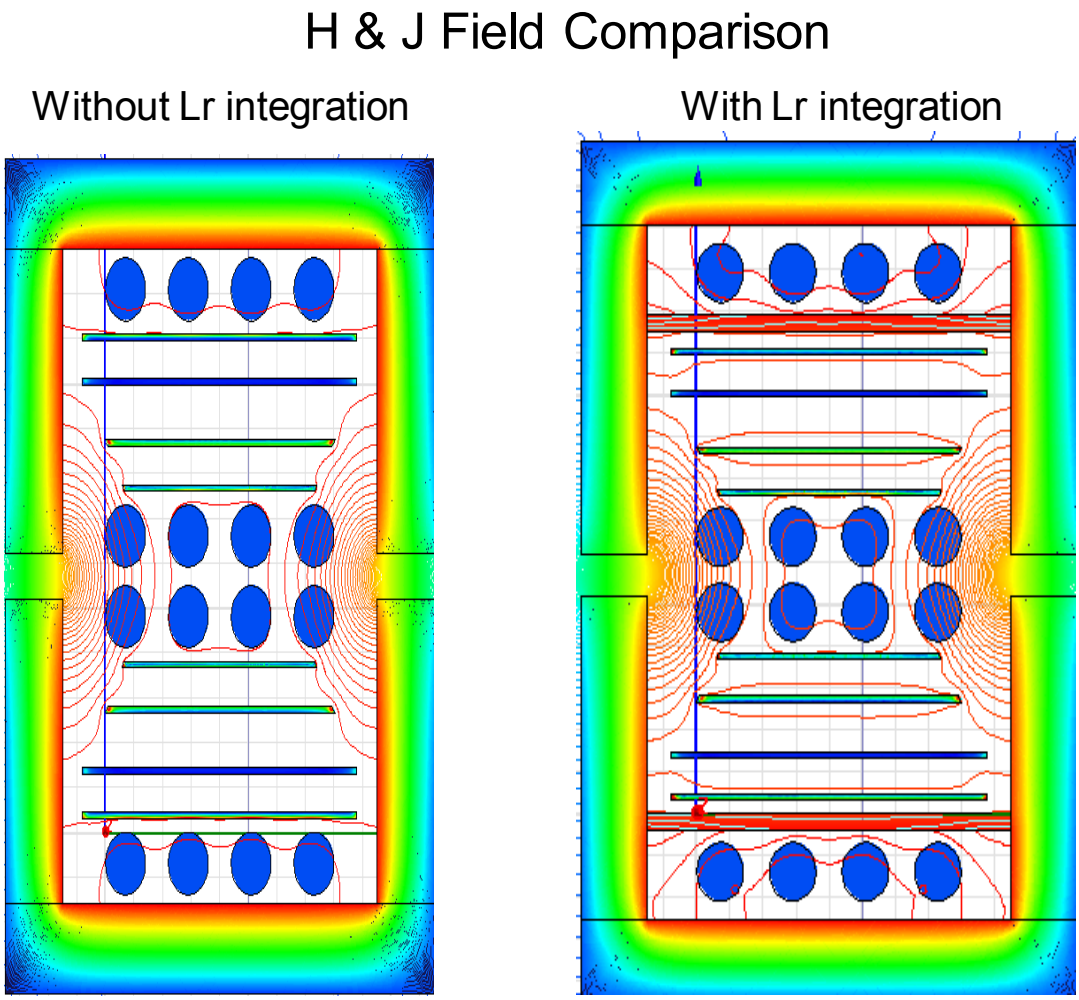


Fig. 4.41. H & J field distribution comparison for case I: transformer without Lr integration and case II: transformer with Lr integration.

It is preferable to integrate the leakage inductance as one of the resonant inductor. However, the natural leakage inductance of the transformer is not good enough for this purpose. Normally, it is not convenient to adjust the leakage inductance by increasing the space between the primary side and the secondary side windings. This leads to poor winding window utilization.

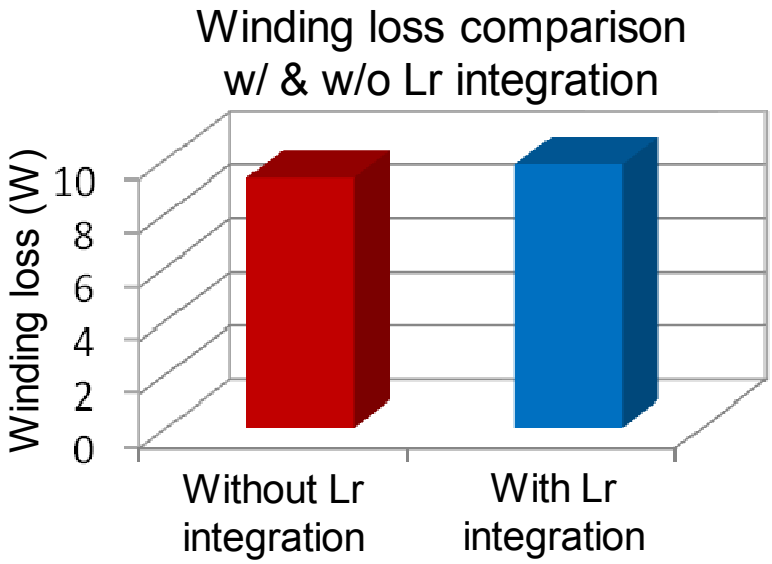


Fig. 4.42. Winding loss comparison with and without L_r integration. There is a loss increase of only 0.5W, which is acceptable for 1kW converters.

Insertion of a magnetic shunt is an effective way to create the required leakage inductance. The concept of the utilization of magnetic shunt is shown in Fig. 4.40. A magnetic material can be inserted between the primary side and the secondary side windings. Thus, the induced leakage energy can be increased if high-permeability materials are applied. The leakage inductance can be adjusted with the variation of the magnetic shunt thickness. In this application, a ferrite polymer composite (FPC) is applied. The relative permeability of FPC is 9, which is high enough to create the needed leakage inductance. Compared with the normal ferrite materials with much higher permeability (~1000), the leakage inductance created by FPC is not very sensitive to the thickness of the shunt layer. Thus, very precise leakage inductance can be obtained. For a 1kW, 1MHz, 400V/12V LLC converter design, 1μH leakage inductance is desired. According to FEA result, a 0.4mm magnetic shut is inserted.

The H & J filed distribution of different transformer structures with and without magnetic shunt layers are illustrated and compared in Fig. 4.41. The magnetizing flux lines and H fields do not change significantly. Compared with μ_r>1000 for the main ferrite core, the permeability of the magnetic shunt is so low that the magnetic shunt layer can hardly affect the main flux. Nevertheless, magnetic shunt layers do attract more flux and induce a slight fringing effect close to the edge of the shunt layers. Because a magnetic shunt is not a good magnetic conductor, the induced extra flux bends a little bit. The curved leakage flux increases the winding loss slightly. A detailed loss breakdown of each winding layer is depicted in Fig. 4.42. According to the curved leakage flux, 0.5W extra winding loss will be induced. For a 1kW converter, this is acceptable. Easy design and convenient implementation make this integration method attractive.

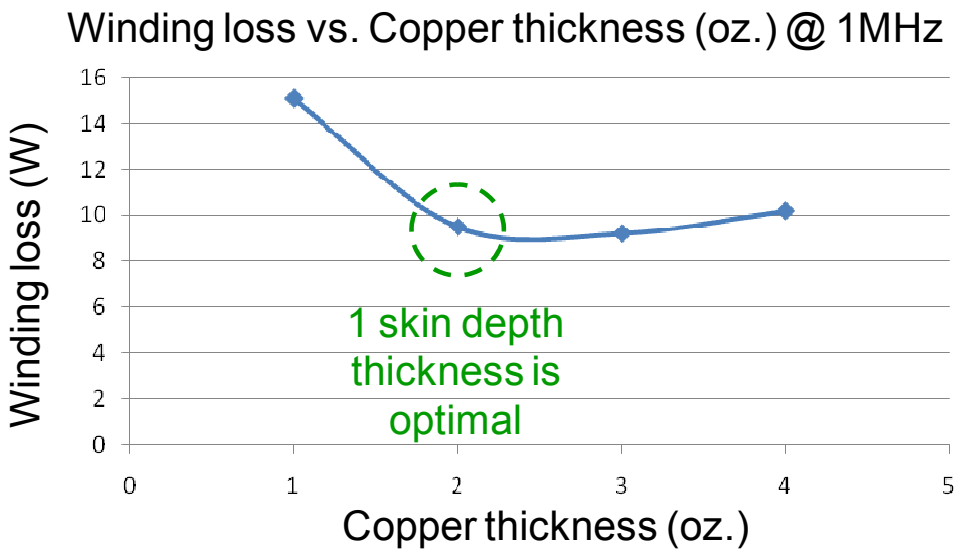


Fig. 4.43. Winding loss comparison of winding loss for different inserted magnetic shunt structures.

Another factor that affects the winding loss is the thickness of the winding copper. The winding loss is affected by the winding copper thickness at high-frequency operation. The relationship of winding loss versus copper thickness is given in Fig. 4.42. It can be observed that thicker copper does not lead to lower winding loss at high frequencies such as 1MHz. On the contrary, too thick copper increases the total winding loss. In addition, more copper thickness means higher cost. Thus, an optimal copper thickness should be chosen. In the 1MHz case, 2 oz. and 3 oz. copper achieve the lowest winding loss. With consideration of cost, 2 oz. copper is chosen for the improved design. As a result, the optimal copper thickness is chosen as 1 skin depth of the operating frequency.

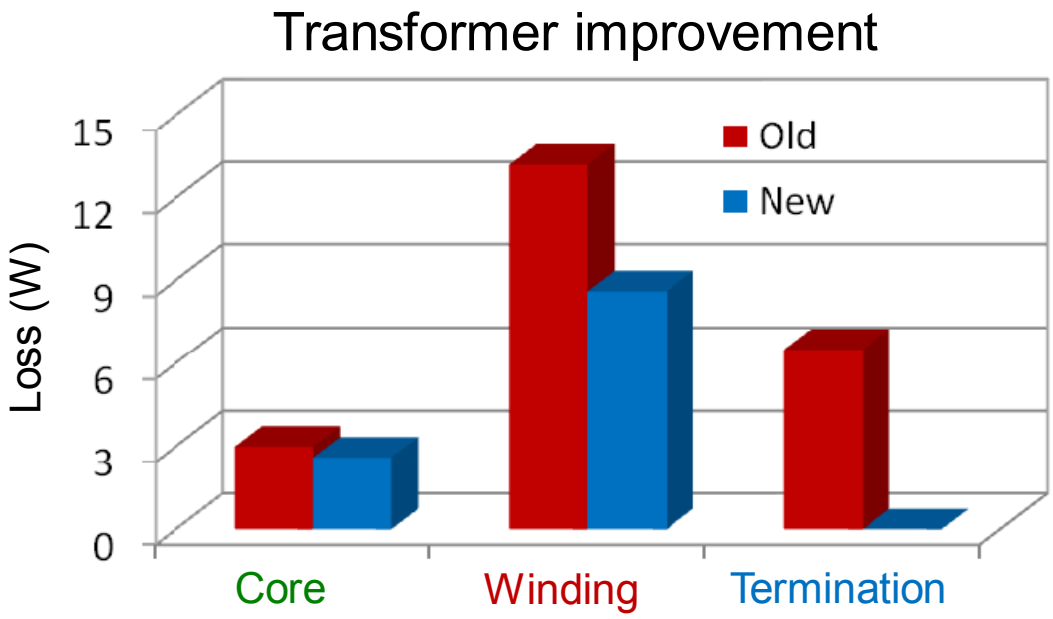


Fig. 4.44. Transformer optimization summary.

With the replacement of the ferrite core of 3F4 with the N49, the core loss will also be reduced.

Finally, the results of the optimization of the transformer design are shown in Fig. 4.44. With the proposed transformer structure, the termination loss can be reduced. With the optimal design of the transformer winding structure, the winding loss can also be significantly reduced. The impacts of the magnetic integration have been analyzed. The magnetizing inductance and the leakage inductance are integrated with the transformer without a significant increase of the winding loss. The total transformer losses have been successfully reduced.

4.7 Summary of Optimization

Utilizing the aforementioned optimization, the major losses related to SR and transformer have been considerably reduced.

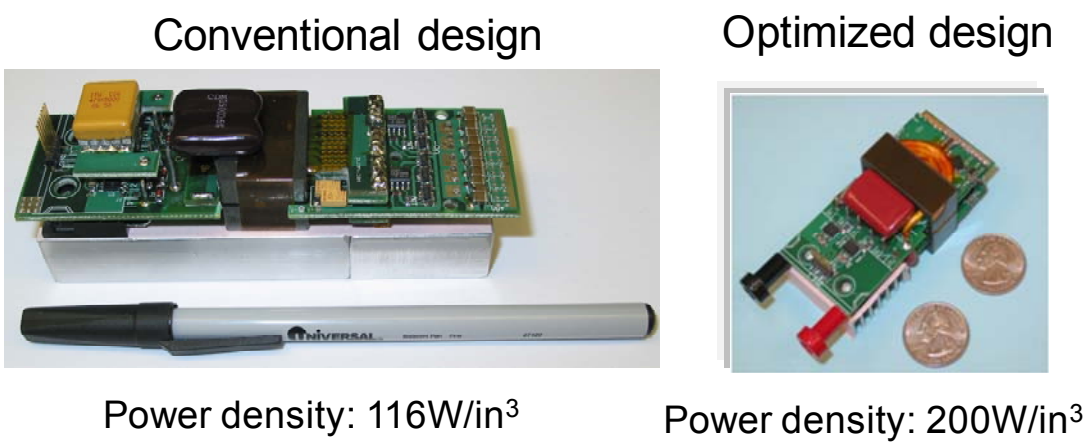


Fig. 4.45. Power density comparison for conventional and the optimal LLC resonant converters.

Fig. 4.45 shows prototypes of the 1kW, 1MHz, 400V/12V LLC resonant converters that were built to verify the theoretical analysis. The power density has been increased from 116W/in^3 to 200W/in^3.

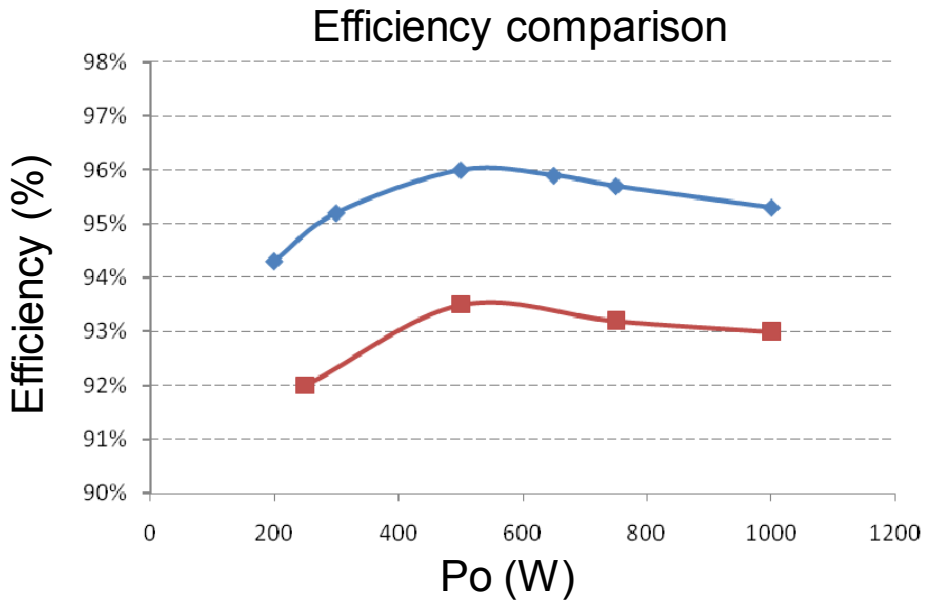


Fig. 4.46. The efficiency comparison for conventional and the optimal LLC resonant converters.

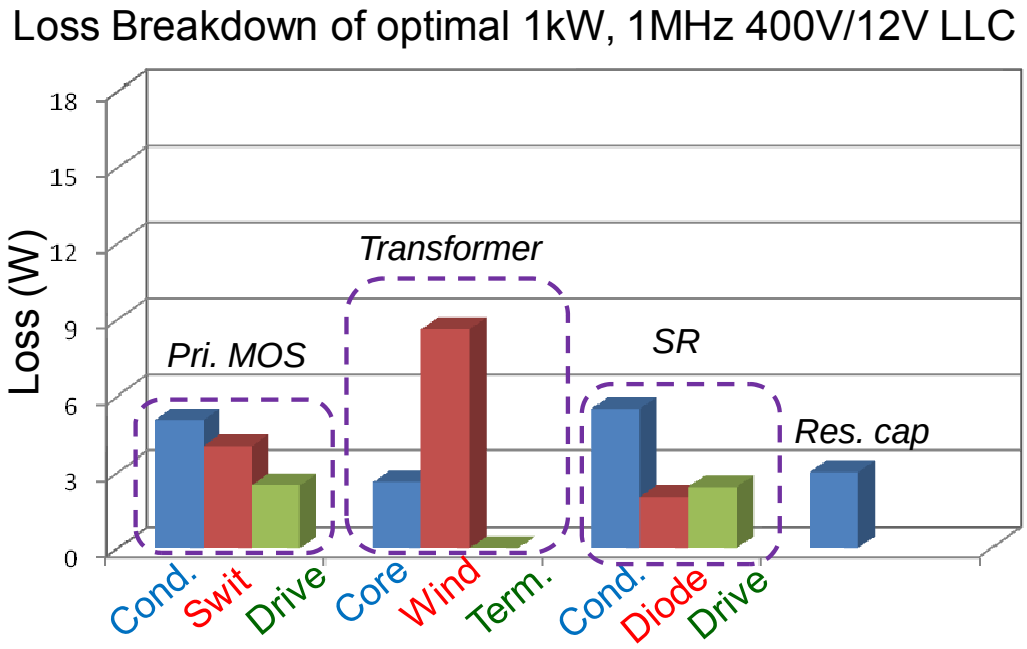


Fig. 4.47. The loss breakdown of the optimal LLC resonant converter.

The measured efficiency of the conventional and the proposed LLC resonant converters are shown and compared in Fig. 4.46. Due to overall optimization, the efficiency has been increased considerably. Very high efficiency is finally achieved.

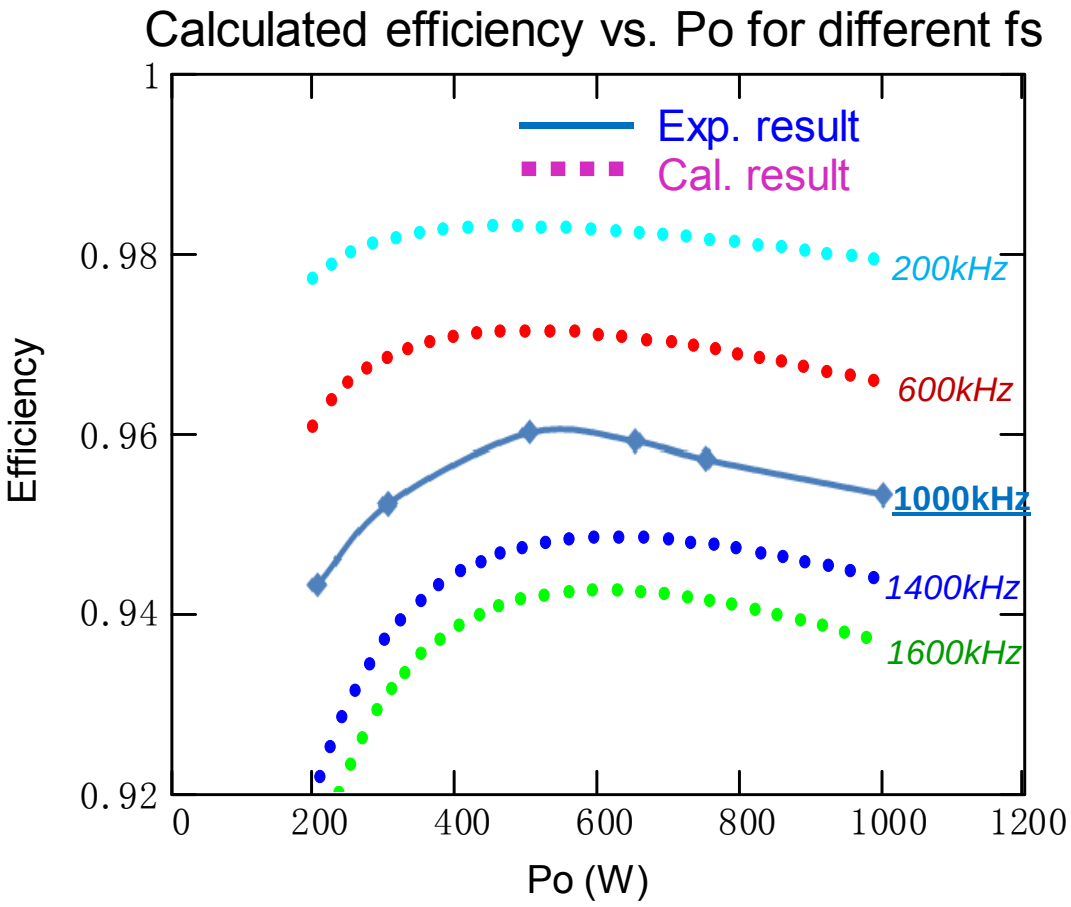


Fig. 4.48. The calculated efficiency of LLC resonant converter at different frequency.

The loss breakdown of the proposed optimal 1kW, 1MHz, 400V/12V LLC resonant converter is shown in Fig. 4.47. The theoretical calculation is in good agreement with the experimental results.

Pursuing higher efficiency is a trend for power conversion technologies. LLC resonant converters are believed to be very suitable for high-frequency operation because of the soft-switching of semiconductors. However, at high frequencies, driving loss and ac copper loss increase substantially. Thus, to achieve higher efficiency, low-frequency operation becomes attractive when efficiency is the first priority.

According the developed loss model and constructed hardware, the theoretical calculation is in good agreement with the experimental results. Based on the developed optimal design procedure and the loss model, the efficiency at different frequency is calculated and given in Fig. 4.48 and Fig. 4.49. The transformer winding losses are obtained from FEA.

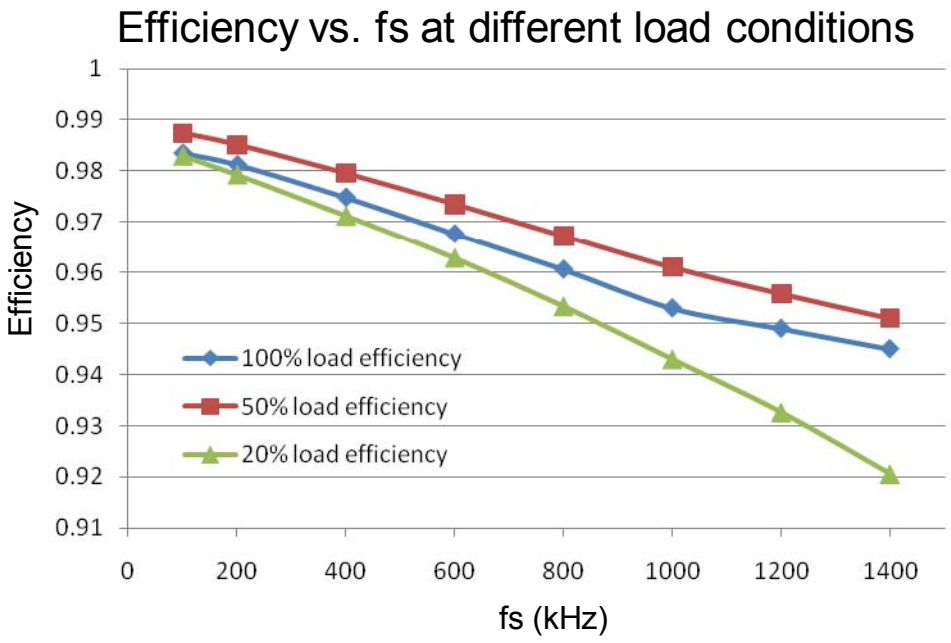


Fig. 4.49. The calculated efficiency of LLC resonant converter vs frequency at different load conditions.

Chapter 5

Conclusion

5.1 Conclusion

There is a large incentive to achieve high efficiency and high power density in power delivery systems. Resonant dc-dc converters exhibit higher efficiency and higher power density characteristics than conventional PWM circuits. Hence, resonant converters are becoming popular for dc-dc converters in commercial products. To further improve the performance and solve the existing issues of resonant converters, novel concepts and techniques are being studied and developed.

This dissertation proposes a novel SR driving scheme for resonant converters. It is very suitable for high-frequency, high-efficiency and high-power-density dc-dc resonant converters. The LLC resonant converter with the proposed SR driving method is designed and analyzed. The SR body diode conduction is reduced to almost zero. The reverse recovery problem of SRs is eliminated. Both conduction loss and reverse recovery loss of SRs are considerably reduced.

To meet the EMI standard and reduce EMI noise, an EMI model for LLC resonant converters is proposed. The DM and CM noise of LLC resonant converter are analyzed, and several EMI noise reduction approaches are proposed. Shield layers are applied to reduce CM noise; by properly choosing the ground point of shield layer, significant

noise reduction can be obtained. With an extra EMI balance capacitor, CM noise can be reduced further. Two-channel interleaving LLC resonant converters are proposed to cancel the CM current. Conceptually, when two channels operate with a 180° phase shift, CM current can be canceled. Therefore, significant EMI noise reduction can be achieved.

This work also proposes a family of novel multi-element resonant converters for front-end converters. The proposed resonant converter provides inherent current protection with superior performance and very low circulating energy. With the optimized design, the proposed resonant converters can operate with a short output circuit. Based on a third-order harmonic injection, the circulating energy of the resonant tank can be reduced to be lower than other conventional resonant converters, such as the LLC resonant converter. ZVS and ZCS can be achieved for the primary side and secondary side devices, respectively. Furthermore, high voltage gain can be designed for holdup time operation.

System optimization of LLC resonant converters has been studied to achieve high efficiency for low-output-voltage, high-output-current applications. Great attention should be paid to alleviate the extra winding loss that occurs due to magnetizing current. High termination loss is another stringent challenge of transformer design. This work proposes an improved transformer structure to reduce the termination loss and simplify the transformer winding configuration. An optimal transformer structure is proposed and verified with the FEA and hardware. Low loss is achieved for the

transformer with the integration of extra two resonant inductors. The proposed concepts might be extended to other resonant dc-dc converters.

5.2 Future Work

This work proposes an SR driving scheme for resonant converter. However, due to its relatively complex control structure, possible further improvements should be investigated. With a digital control approach, control components can be reduced and the design can be simplified further. Precise control may be easier to achieve with an advanced digital controller; hence a digital control approach should be investigated further.

The proposed multi-element resonant converters demonstrate advantages over existing LLC resonant converters. The multi-element resonant converter is designed to limit the current during startup. Due to the extremely large impedance of the section with the notch filter resonant elements, the inrush current can be limited to be small. The current outside of the notch filter resonant section is also small. However, the current may circulate inside the notch filter resonant section. Thus the notch filer resonant components should be carefully designed. Meanwhile, a family of multi-element resonant converters has been proposed. One of these has been studied in detail, and its advantages are demonstrated. It is believed there are many more candidates that are suitable for dc-dc power conversions. Therefore, more study should be continued to find better topologies. It is worthwhile to investigate how to systematically identify the desirable topology for the specific application.

On the other hand, for the proposed multi-element resonant converters, due to one extra magnetic component, the power density and efficiency may be reduced. Magnetic integration techniques should be studied further to shrink the size and reduce the loss of the magnetic components.

Further, the EMI performance of multi-element resonant converters should be evaluated. The proposed EMI suppression approaches could be applied, and they should be verified experimentally in the future.

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