Thermal and EMI Modeling and Analysis of a Boost PFC Circuit Designed Using a Genetic-based Optimization Algorithm

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Thesis submitted to the faculty of

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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July 24, 2001

Blacksburg, VA

Keywords: optimization, genetic algorithms, power factor correction (PFC), electromagnetic interference (EMI), temperature rise, per unit analysis

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(ABSTRACT)

The boost power factor correction (PFC) circuit is a common circuit in power electronics. Through years of experience, many designers have optimized the design of these circuits for particular applications. In this study, a new design procedure is presented that guarantees optimal results for any application. The algorithm used incorporates the principles of evolution in order to find the best design. This new design technique requires a rethinking of the traditional design process. Electrical models have been developed specifically for use with the optimization tool. One of the main focuses of this work is the implementation and verification of computationally efficient thermal and electro-magnetic interference (EMI) models for the boost PFC circuit. The EMI model presented can accurately predict noise levels into the 100's of kilohertz range. The thermal models presented provide very fast predictions and they have been adjusted to account for different thermal flows within the layout. This tuning procedure results in thermal predictions within 10% of actual measurement data. In order to further reduce the amount of analysis that the optimization tool must perform, some of the converter design has been performed using traditional methods. This part of the design is discussed in detail. Additionally, a per unit analysis of EMI and thermal levels is introduced. This new analysis method allows EMI and thermal levels to be compared on the same scale thus highlighting the tradeoffs between the both behaviors.

Acknowledgements

I would like to express my deepest appreciation to Dr. Dushan Boroyevich for being my advisor and serving as chairman of my master's committee. His imagination, determination, and vast knowledge of power electronics have been an invaluable resource to me as well as the rest of our research center.

I am very grateful to Dr. Dan Chen for his excellent teaching and his willingness to offer advice. I would like to thank Dr. D. K. Lindner and Dr. Zafer Gurdal for their friendship and valuable expertise in the Schneider project. Additionally, I thank Dr. Jason Lai for taking the time to be in the lab and work with students.

Michel Arpilliere and Herve Boutillier of Schneider Electric also deserve special thanks. Their patience and valuable engineering experience resulted in a very successful collaboration between CPES, Adoptech, and Schneider Electric. Also my thanks go to Scott Ragon and Grant Soremukun of Adoptech. Without their help the results of this thesis would still be academic.

Sincerest thanks go to Sergio Busquests-Monge who was my partner in the Schneider project. I could not have had a more dedicated person to work with and I hope we remain friends far beyond our stay at CPES.

I also wish to acknowledge Bob Martin, Gary Kerr, Steve Chen and Jon Grimsley who are largely responsible for making this lab work on a daily basis. I have noticed a significant improvement in the functioning of the lab since I arrived in the fall 1999 and it is no small part due to them.

I thank all my friends that have made life in the lab much easier. Over the past two years I have found friends in Jingdong Zhang, Jia Wei, Matt, Kevin, Yuxin Li, Yuhui Chen, Sriram, Wei Dong, Christophe, Dengming Peng, Ivan, Raphael, Nikola, Fransisco, Peter, Jose, Johan, Alex, Michael, Rob, Troy, Jeremy, Len, Cory, Carl, Heath, Dan H., Dan C. and Dimos to name a few. I have really appreciated all the good times we had inside and outside the lab.

Additionally, I would like to thank Dr. Roger King and Dr. T.A. Stuart for suggesting that I come to Virginia Tech to study power electronics. It was their undergraduate classes in power electronics that inspired me to study the field.

Finally I thank my parents for teaching me the value of education and encouraging me throughout my studies.

The work in this thesis was supported primarily by Schneider Electric S.A. and made use of ERC Shared Facilities supported by the National Science Foundation under Award Number EEC-9731677.

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Chapter One

1 Introduction

Good circuit design is a result of successful manipulation of various tradeoffs. For example, thermal performance affects many aspects of an electronic circuit's behavior. The transistor operating temperature influences the delay, rise and fall time, and the turn on and off energy. The temperature of a diode affects the amount of reverse recovery current and the forward voltage. Additionally, the switch rise and fall time and the reverse recovery affect the electro-magnetic interference (EMI) levels. These are just a few of the tradeoffs that must be considered during the design of an electric circuit. Considering all the possible combinations and finding the best design is a daunting task. This has motivated the development of optimization tools that can automatically design power electronic circuits.

1.1 Optimization in Power Electronics

Optimization is not new in power electronics. Beginning in the 1970's, methods for automatic circuit design started appearing [5], [6]. Since then there have been many efforts to apply optimization techniques to power electronics. These efforts have primarily been focused on solving a specific problem in an automated way. [7] proposes an automated way to design cabling in power electronics converters for the lowest possible inductance. An optimization procedure for heat sink design is described in [8]. [9] uses reduced order models to optimize the gate drive circuitry in a half-bridge circuit. In [10] an optimization procedure is used to study the tradeoffs between BJT's and MOSFET's in a Half-bridge DC to DC circuit. Some optimization studies have focused on linking several software packages together and managing them with an optimization program [8], [9], [11]. This method suffers from long simulation times and the significant challenge of forcing different software packages to communicate with each other.

Although the previous optimization procedures are able to produce good results in less time, there can still be improvements. The above-mentioned studies lack the ability to capture the discrete nature of power electronics design. If actual devices were incorporated into the design, optimization results could be physically realized immediately. Also, using discrete components enables the electrical models of the system to be much more accurate. Instead of general loss

equations for an inductor core, the actual loss equations from the manufacturer's data sheet could be used. Additionally, the optimization program could consider the actual cost of each component. Taking these considerations into account it is interesting to utilize Genetic Algorithms (GA's) to find the optimum solution. GA's have the ability to handle discrete variables. They also tend to converge to a reasonable solution much more easily than classical gradient-based optimization algorithms. There have been recent efforts to apply GA's to power electronics optimization procedures [12], [13], [14], [15], [16]. In [12] a buck regulator is designed for optimum transient performance. [14] proposes the use of GA's for induction motor parameter identification. The control parameters for a sensorless induction motor are optimized on-line using GA's in [15]. GA's are also applied to the design of an active filter in [14]. The current work has been motivated by the need to optimize overall system cost. Also, to make the optimization tool even more attractive to industry, real components are used by the GA. This is fairly easy to implement due to the discrete nature of GA's. A major drawback of GA's is the number of iterations that are required to find an optimum point. This requires computationally efficient electrical models. Traditionally, in order to compute EMI and thermal behavior of a circuit, complicated simulations were required. In this work, more computationally efficient thermal and EMI models are described and validated. The following section provides a brief explanation of genetic algorithms.

1.2 Genetic Algorithms

A genetic algorithm is a problem solving method loosely based on the concept of natural selection [4]. GA's are superior to the more traditional gradient-based techniques in that they are general enough to be applied to any optimization problem and they are not subject to being trapped in local minima. Other optimization procedures discussed in [1], [2], [3] are not as adaptable as GA's.

In GA's, an initial population is created either randomly or based upon a designer's intuition. The population then evolves toward an optimum solution that is determined by a cost (or fitness) function. The evolution process uses the ideas of heredity, selection, and mutation. Each member of the population is called a chromosome (or member). Each chromosome represents a complete solution to the problem. For example a single chromosome could contain all the parameters for the power stage of a boost converter. The parameters that make up the

chromosome are called genes. The content of each gene is called an allele. These genes could be core size, capacitance, or a particular MOSFET or IGBT. This discrete make-up of the chromosomes makes GA's especially attractive to electronic circuit design. It is well known that even devices with the same voltage and current ratings can vary significantly. Another advantage to the chromosome structure used in GA's is the ability to apply constraints to individual genes. For example if one gene in a chromosome is number of inductor turns, a maximum and minimum limit could easily be imposed on that particular gene. The GA continually mixes and matches the best chromosomes in order to attain an optimum design after many generations. The cost (or fitness) function is specific to each application. As discussed above, the fitness function could be for optimum performance, parameter identification, system cost, or some other figure of merit.

The four primary operators used by GA's are reproduction, mutation, crossover and elitism. In reproduction the GA selects individuals with a high degree of fitness to become parents of the next generation. The idea is that some children would inherit the best traits of the parents and thus attain a higher fitness level. Of course other children would inherit the worst traits of the parents, but these children are less like to survive another generation because they would have a low fitness level. It is important not completely exclude individuals with low fitness levels because they may have sequences that may be important to future generations.

Crossover is the process by which two parents are paired together to form two children. As shown in Fig. 1.1, the GA mixes sub-strings of the two parents. Some chromosomes resulting from crossover would have very useful sub-strings; however, other chromosomes would have undesirable sub-strings. Overall, the average fitness level of the next generation should improve because those individuals selected for crossover would in general have a higher fitness level.

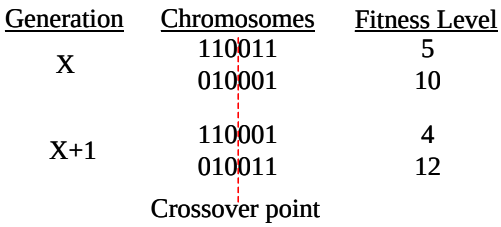


Fig. 1.1. Crossover Operation

A gene of a chromosome can be randomly altered due to the mutation operator. This altered chromosome would join the next generation with possibly a new and advantages trait. Obviously, the probability for mutation must be kept low; otherwise the GA would have difficulty converging to an optimum design.

Another useful GA tool is elitism. If this concept is used, then the chromosomes with the highest fitness level are allowed to pass into the next generation unaltered. This tool tends to keep good traits in the population. Also it ensures that really good designs (chromosomes) are not lost due to the other three operators.

Once the fitness function is defined and the GA is provided with good electrical models, the GA is able to determine the optimum design without an understanding of the system. This can only be accomplished with many iterations (many generations). Therefore the models given to the GA must be computationally efficient. Accuracy of the models is also very important. This work describes the development and validation of computationally efficient and accurate electrical models for a PFC boost circuit.

1.3 Objectives and Design Specifications

In this implementation of GA's, the objective has been to optimize a power factor correction (PFC) front-end converter for a 1 horsepower general-purpose AC drive (see Fig. 1.2). The study focuses on how to minimize the converter cost while still satisfying all requirements. The completion of this goal can be divided into four main tasks. The first task is the design of the boost PFC circuit. The second is the development of the models that the GA will use to evaluate the circuit. The third task is verification of the optimization results through hardware testing. The fourth and final task is the development of the genetic-based optimization tool. In the next

sections, the basic operating principle of the boost PFC circuit is discussed, the design specifications are given and the four main tasks are introduced.

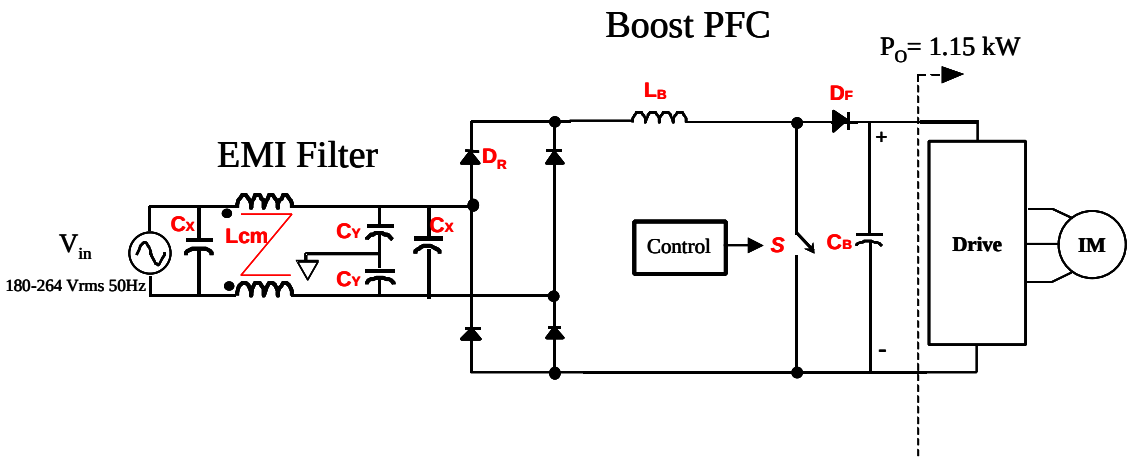


Fig. 1.2. System Schematic

1.3.1 Operating Principle of Boost PFC's

For most AC to DC conversions, the AC input is rectified and a bulk capacitor is connected directly after the rectifier bridge supplies the DC input to a switch mode power supply. The pulsing input current demanded by this topology is no longer tolerated by certain utilities. Fig. 1.3 shows input voltage, input current and capacitor voltage for a standard single-phase diode-bridge rectifier. To comply with recent standards [17], [18], active input stages have been implemented to shape the input current [19], [20], [21], [22], [23]. The boost PFC circuit in Fig. 1.3 is widely used to fulfill this requirement because it easily can be implemented to provide high power factor with good efficiency.

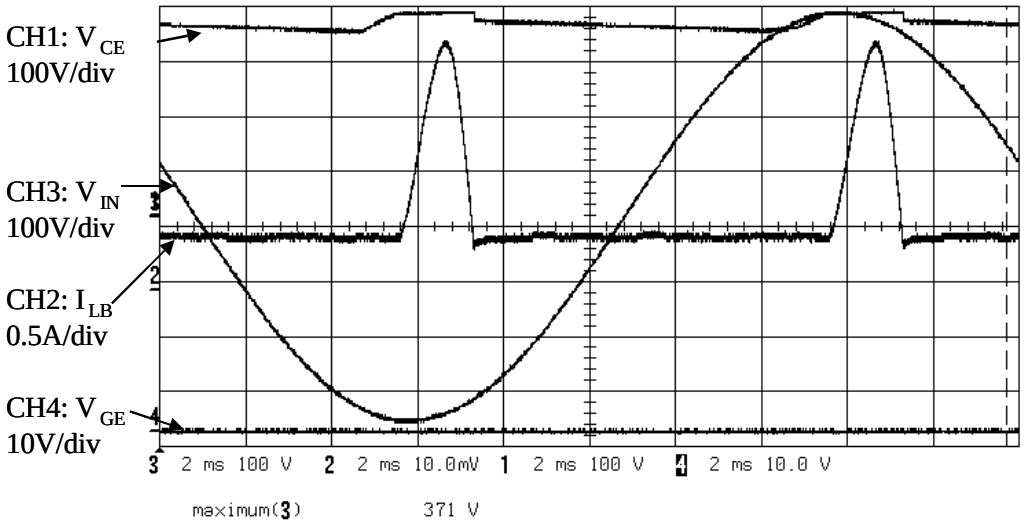


Fig. 1.3. Standard Single-phase Diode-bridge Input Waveforms without PFC

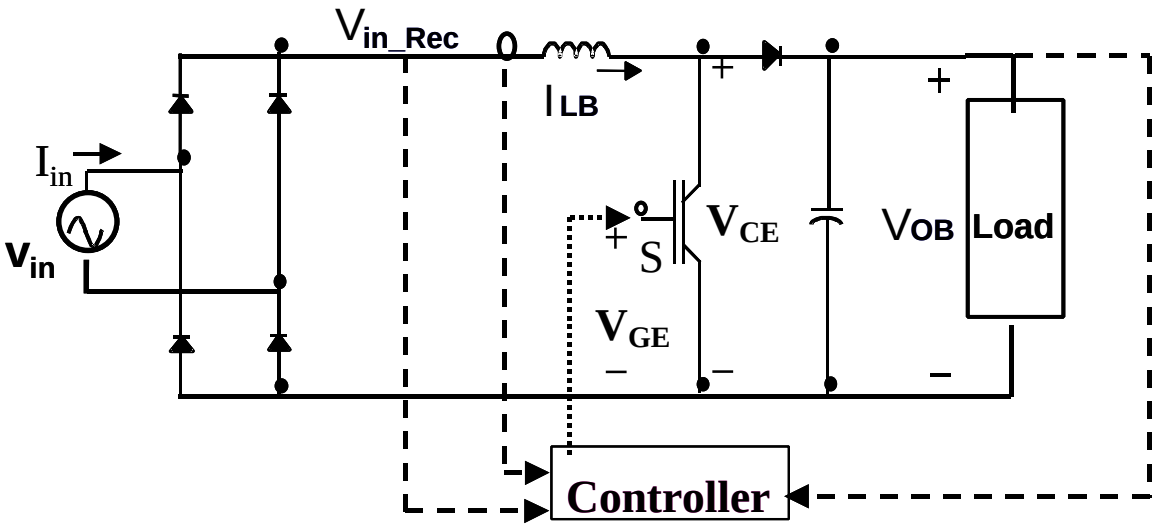


Fig. 1.4. Boost PFC Circuit and Control

The basic idea in PFC is to control the switch such that the inductor current is a sinusoidal waveform. Fig. 1.5 shows input voltage and inductor current for the boost PFC circuit. Note that the inductor current's (I_{LB} in Fig. 1.4) low frequency shape is a rectified sinusoid. This results in the input current (I_{in} in Fig. 1.4) being sinusoidal and in phase with the input voltage. For the boost topology, this is relatively easy to implement. The presence of the inductor at the input of the power stage allows for easy input current shaping. Since the rectifier bridge is always conducting, the voltage V_{in_Rec} is a rectified sinusoid; therefore, it can be used as the

inductor current reference. A slower voltage loop can then be used to regulate the voltage V_{OB}. Standard PFC control IC's can be used to realize this control scheme [24], [25], [26]. There are various control strategies and many methods of choosing the power stage components. Typical control strategies are discussed in [26], [27], [19]. Also a small-signal model for the boost PFC circuit is given in [28]. The average current mode control law is implement in this design [26], [29]. The waveforms for this control implementation are shown in Fig. 1.5 and Fig. 1.6. The current ripple, ΔI_{LB} in Fig. 1.6, is chosen so that the current stays in continuous conduction mode (CCM) through most of the line cycle.

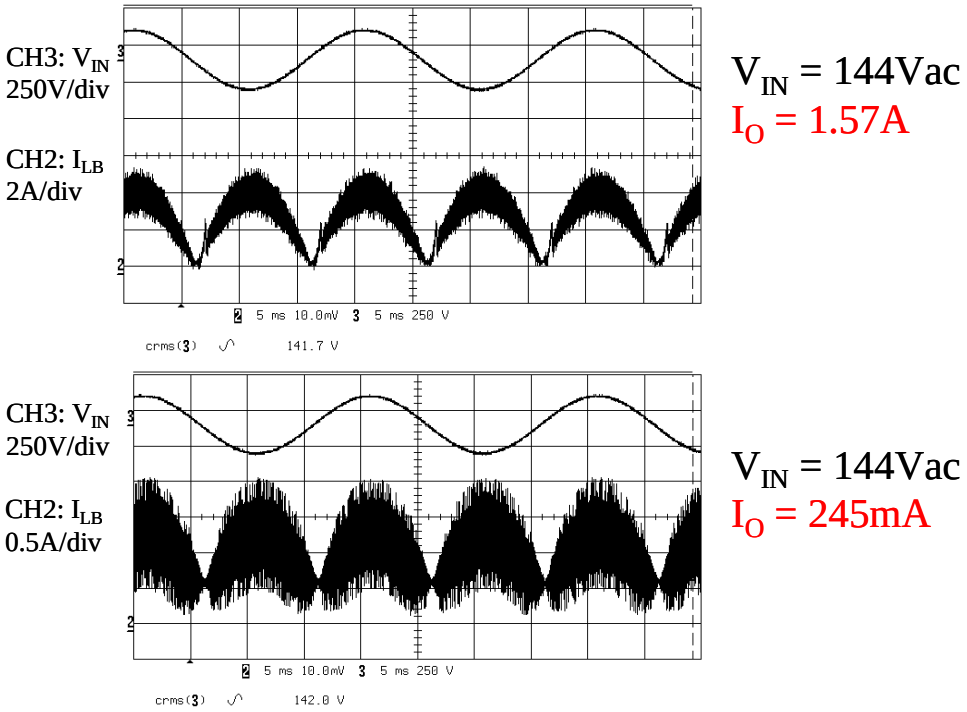


Fig. 1.5. Full and Light Load PFC Line Cycle Waveforms

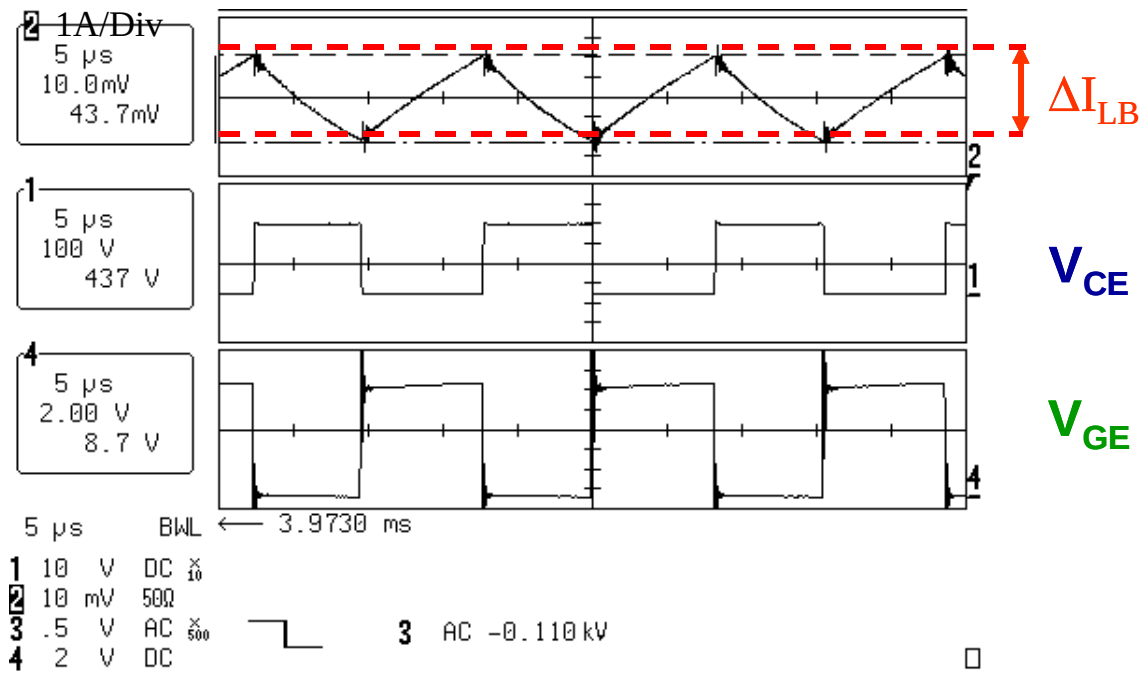


Fig. 1.6. PFC Switching Cycle Waveforms

1.3.2 Design Specifications

The goal of the optimization tool has been to produce a complete design of the boost PFC circuit introduced above. The following specifications have been considered.

Table 1.1 and Table 1.2 list conditions on the input network, boost PFC circuit, and motor drive.

Table 1.1. Input Voltage and Line Frequency Range

Magnitude	Min	Max
Input Voltage (rms)	180	264
Input Voltage (complying with IEC 61000-3-2 [17])	180	240
Line Frequency (Hz)	47.5	63

Table 1.2. External Conditions

Magnitude	Value
Output Power (W)	1150
Input Line Inductance (µH)	750
Drive internal capacitance (µF)	624 - 1060
Drive Breaking Voltage (V)	380
Drive Inrush Relay Trip Voltage (V)	200

In addition to electrical design specifications, there are certain standards that the final product must satisfy in order to be sold in the consumer market. These standards are list in Table 1.3.

Table 1.3. Standards

Type	Standards	Level
EMC		
EMC emission [18]	EN 55011 IEC 61800-3	Conducted: Class B (public sector) Radiated: Class B (public sector)
EMC immunity [17]	IEC 61800-3 IEC 6100-4-X	61000-4-2 (level 3) 61000-4-3 (level 3) 61000-4-4 (level 4) 61000-4-5 (level 3) 61000-4-6 (level 3) 61000-4-11 (level 3) 61000-4-12 (level 3)
Input Harmonic Current	IEC 61000-3-2	Class A
Environmental requirements		
Ambient air temperature		Storage: -25C to 80C Nominal operation: -10C to 50C(1) Operation with current derating: -10C to 60C

1.3.3 Boost PFC Design

Due to the large number of designs that the GA must evaluate during a single optimization run, some parts of the boost PFC design have been performed outside the optimization tool. Fig. 1.7 distinguishes the parts of the system designed by the automated optimization tool from the parts that have been manually designed. As shown in Fig. 1.7, the manual design consists of inrush circuit evaluation, selection of the output voltage and capacitance, and the controller design. In addition to these three, the layout has also been designed manually as well as verification of converter operation under non-PFC conditions and verification of converter operation using US line input voltage. Simulations and hardware testing have been used to aid in these parts of the boost PFC design. The details and results are presented in Chapter Two. The automated optimization tool has performed the rest of the boost PFC design. Details of this part of the design can be found in [13].

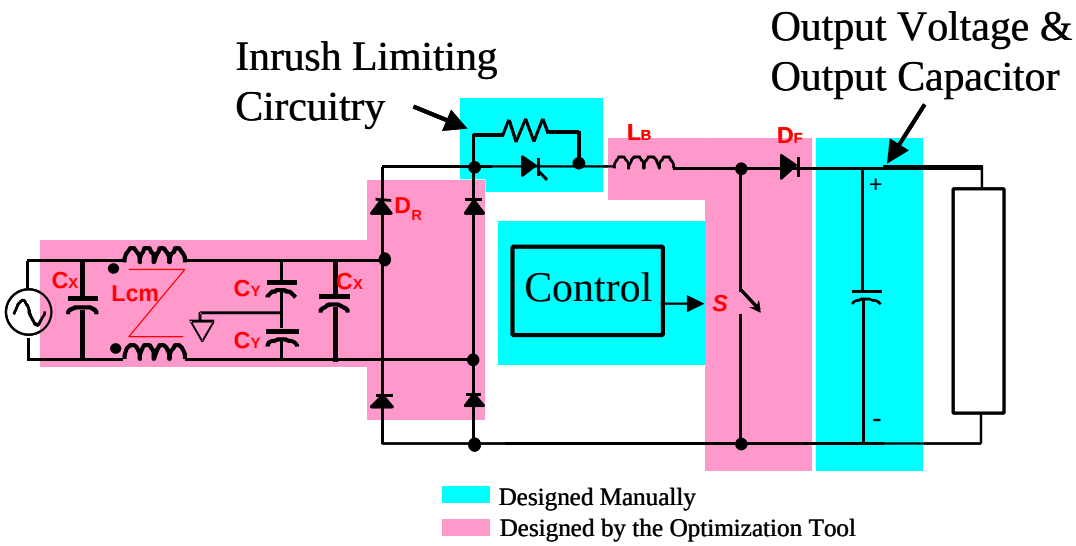


Fig. 1.7. Boost PFC Design: Manual and Automated

1.3.4 Modeling

The goal of the modeling effort is to provide simulation tools that can be used by the GA to predict the performance of the actual circuit. Switching and algebraic models are developed to predict the electrical, EMI, and thermal behavior of the circuit. Due to the fact that the GA must evaluate many designs, only algebraic steady-state models are implemented in the optimization tool. The most challenging task in the modeling process has been to develop fast and accurate EMI and thermal models. This challenge as well as the rest of the modeling effort is explained in Chapter Three.

1.3.5 Verification of the Optimization Tool

Experimental verification is very important in this case because the end result of the optimization tool should be a physically accurate design. Verification of the optimization tool can be divided into two levels. The first level is the individual verification of the models themselves. As mentioned above the thermal and EMI models are the most challenging. Their verification is discussed at the end of Chapter Three. A per unit analysis is presented in Chapter Five. Using this analysis it is possible to manually find optimum points considering thermal and EMI tradeoffs. These manually found optimums are compared to optimization results to verify that the optimization tool is selecting good designs.

1.3.6 Development of the Optimization Tool

Results of the optimization tool are discussed in Chapter Five; however details on its development can be found in [13].

1.4 Outline

The overall goal is to design a power electronics converter with minimum cost. Considering the recent success of GA-based optimization algorithms in power electronics, an optimization based upon GA's has been chosen. Although the GA has many attributes that fit well with power electronics design, the large number of analysis required is still a significant drawback. In order to reduce the amount of variables that the GA must consider, some initial optimization was performed on the boost PFC design. Chapter Two discusses design issues that are not dealt with by the GA. The models used by the GA are discussed in Chapter Three and their accuracy is also verified. Chapter Four presents experimental data and describes the hardware test set-ups. Thermal and EMI behaviors are also discussed in Chapter Four. A new per unit analysis of the EMI and thermal measurements is presented in Chapter Five as well as the results of the optimization process. The per unit analysis in Chapter Five is used to highlight thermal and EMI tradeoffs and gives additionally insight into their behaviors. Closing remarks are made in Chapter Six as well as suggestions for future applications of GA-based optimization procedures in power electronics.

Chapter Two

2 Boost PFC Design and Functionality

As Mentioned in Chapter One, the GA is currently not sophisticated enough to design every aspect of the PFC circuit. Certain issues such as the maximum voltage requirement on the motor drive and the stipulation that the circuit works at North American line are specific to this particular implementation. The follow sections address the manual aspects of the boost PFC design and also show results on the functionality of the converter.

2.1 Boost PFC Design

2.1.1 Controller Design

The basics of PFC have been discussed in Chapter One. The controller design is based upon design procedures described in [25] [26]. The details of the control design are given in Appendix One. Normally before implementing a control law in the hardware, a simulation model is used to verify the operation of the controller.

The functionality of the converter is evaluated with simulations and experiments. It is most important to verify that the circuit operates properly under normal conditions. The next concern is to explore the converter operation under abnormal conditions. Therefore the models presented in Chapter Three also include the various safety functions of the L4981A control IC [25]. With these models it is possible to evaluate that the control design behaves properly and the converter is adequately protected under abnormal conditions.

2.1.2 Boost Output Capacitor and Output Voltage Selection

According to the design specifications given in Chapter One the maximum boost PFC output voltage cannot exceed 375 V in normal operation. For this particular implementation, the drive breaking voltage is 380 V. If a voltage over 380 V is applied to the drive input, a relay shunts a resistor across the drive DC link capacitor. This feature is used by the drive to dissipate energy due to reverse power flow from the motor. Tripping this mechanism during normal operation would result in low efficiencies and improper operation of the drive. 375 V has been chosen as the maximum boost output voltage in order to maintain a 5 V margin and to avoid any tolerance

issues on the drive relay. Fortunately, there is already significant capacitance in the drive (624 – 1060 μF). Therefore the boost capacitance does not have to be exceedingly large. The waveforms for the input current and voltage and the output voltage are shown in Fig. 2.2. The functions V_{in_Rec} and I_{in_Rec} and the current and voltage on the DC side of the rectifier bridge shown in Fig. 2.1. The waveform V_{OB} is the output voltage also shown in Fig. 2.1. In this case the value of $V_{BusHigh}$ cannot exceed 375 V. The difference between $V_{BusHigh}$ and V_{BusMin} is the voltage ripple. Assuming that this ripple is small compared to V_{OB}, (2.1) can be used to find the required boost capacitance. Fig. 2.3 shows a plot of (2.1) for the following conditions.

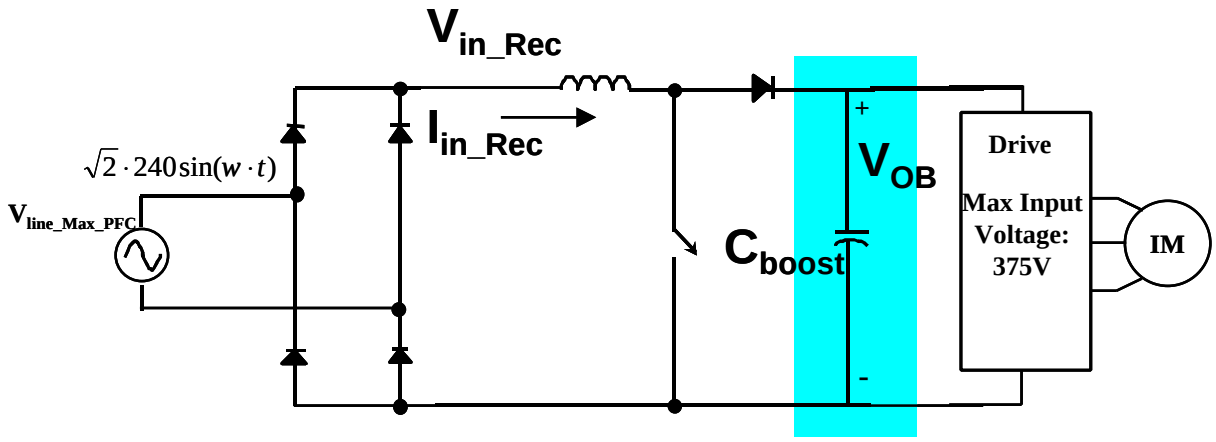


Fig. 2.1. Boost PFC Output Voltage and Capacitor Selection

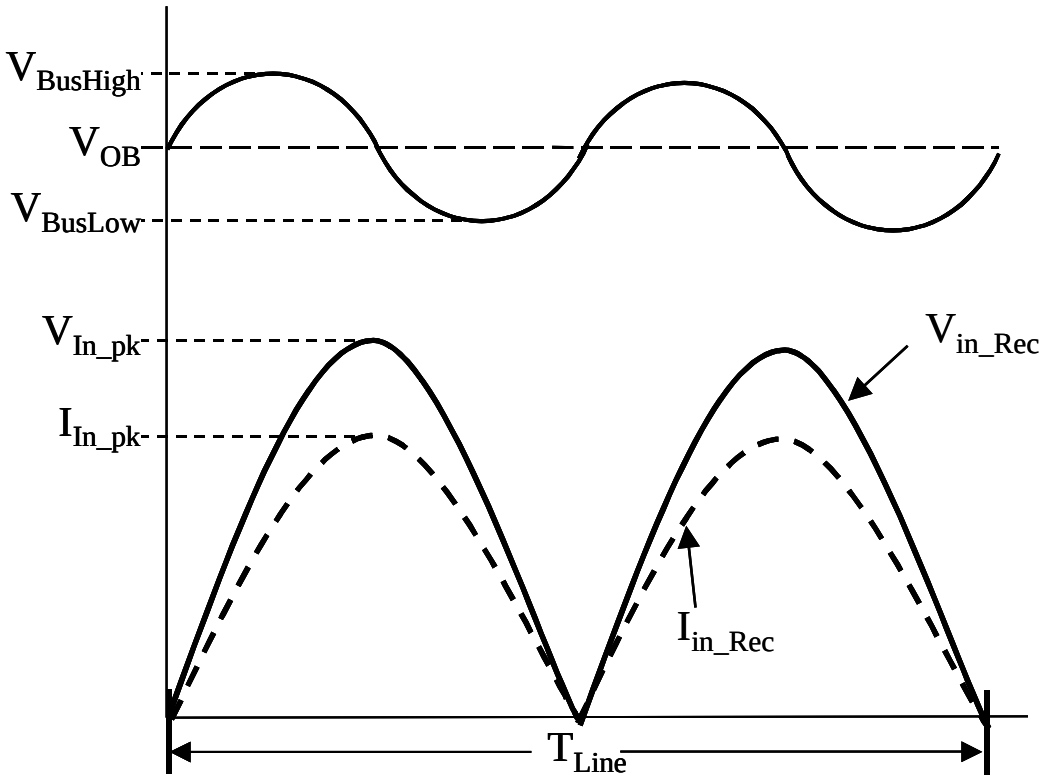


Fig. 2.2. Input Voltage and Current and Output Voltage Waveforms

$$C_{Boost} = \frac{T_{Line} \cdot (V_{In\_pk} \cdot I_{In\_pk})}{2\pi \cdot (V_{BusHigh}^2 - V_{BusMin}^2)} - C_{Drive\_Min} \tag{2.1}$$

CONDITIONS:

$V_{Min} = 180\,Vrms \quad Low\,Line\,Condition$

$V_{In\_pk} = \sqrt{2} \cdot V_{Min}$

$\eta = 0.96 \quad An\,efficiency\,is\,assumed.$

$P_{Out} = 1150\,W \;\; Output\,Power$

$$P_{In} = {P_{Out}}/{\eta} = 1198W \;\; Input\,Power$$

$$I_{In\_pk} = \sqrt{2} \cdot \frac{P_{In}}{V_{Min}}$$

$$T_{Line} = 50Hz$$

$$C_{Drive\_Min} = 624\mu F \;\; see\,Table 1.2$$

$$V_{BusHigh} = 375V$$

$$V_{BusLow}(V_{OB}) = 2 \cdot V_{OB} - V_{BusHigh}$$

Note that V_{BusLow} is expressed as a function of V_{OB}.

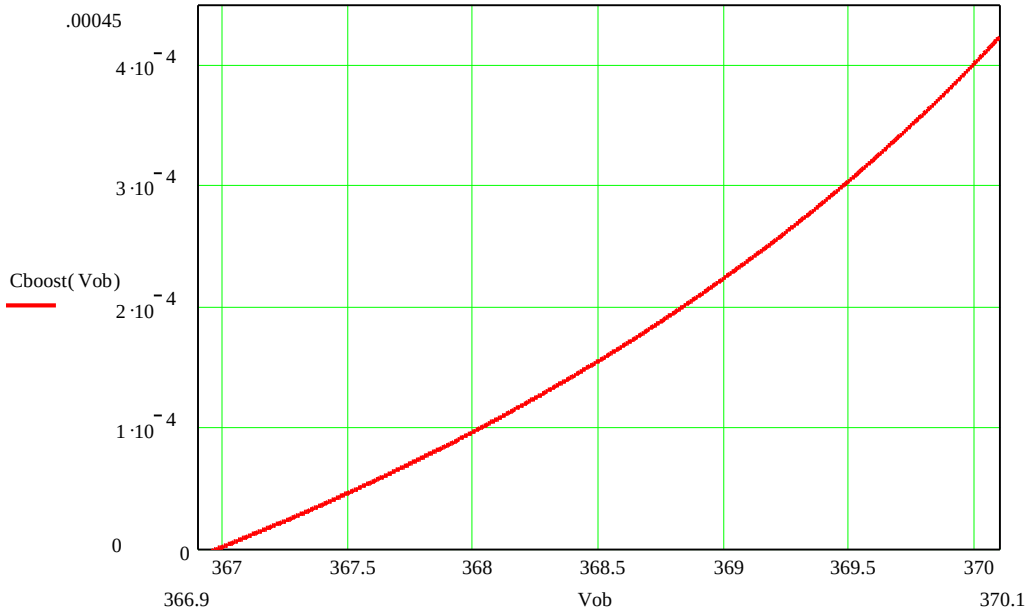


Fig. 2.3. Boost Capacitance vs. Output Voltage

From Fig. 2.3, it is obvious that if the output voltage is lowered below 367 V then a boost capacitor is no longer necessary. However in order to ensure that the converter would work in every case, the tolerances of the control IC and the output voltage divider network must be considered. According to the L4981A data sheet [25], the tolerance of the reference voltage is 2%. If the resistors in the voltage divider network have a tolerance of 0.1%, then the accuracy of the output voltage could be guaranteed within 2.2% (two resistors plus the reference voltage). If a 2.2% tolerance were used, then the average regulated output voltage must be 359 volts.

$$359 - 0.022*359 = 351$$

Where 351 V is the minimum average output voltage. This allows the converter to provide PFC up to an input voltage of 248 Vac. Note that in Table 1.1 the converter must comply with IEC 61000-3-2 for a maximum input voltage of 240 Vac. Therefore if the converter operates at a 359 V output the converter would easily satisfy IEC 61000-3-2. The maximum average boost output voltage is given by

$$359 + 0.022*359 = 367.$$

Therefore 367 V is the highest regulated output voltage. This voltage must be used to size the output capacitor such that the maximum output voltage is not exceeded. Fig. 2.4 provides an illustration. Fig. 2.3 is used to determine that the minimum boost capacitance required is 68 μF. Note that from Fig. 2.3 no capacitor is required for an output voltage of 367 V, however if a one-volt margin of error is considered the capacitance should be around 68 μF. Also to avoid any stability issues with the drive filter a capacitance should be placed in the boost PFC stage. The length of the cable from the boost PFC stage to the drive is not considered here, so adding some capacitance should stabilize the output voltage in the event that the cable is exceedingly long.

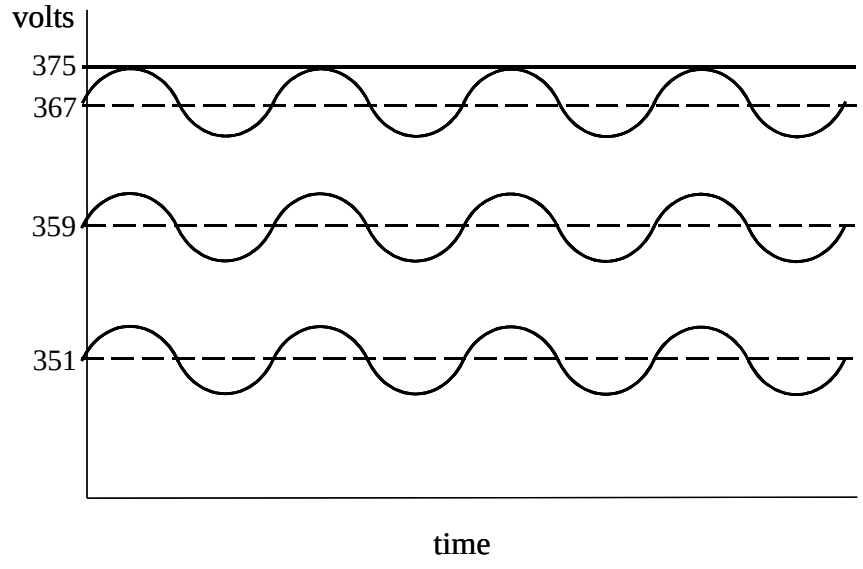


Fig. 2.4. Output Voltage Range Based Upon 2.2% Tolerance and a 68 μF Boost Cap

It is also important to use 0.1% resistors in the over-voltage protection network of the control IC (L4981A). This is obvious from Fig. 2.4. If the over-voltage trip level of 375 V varies too much, then the over-voltage protection may activate under normal circuit operation.

2.1.3 Inrush Transient

The boost converter is inherently vulnerable to inrush currents because the switch is not in series with the input current path. Also the large bulk capacitor draws a large current when the input is first connected or disconnected and then reconnected. Normally the boost inductor does not provide significant impedance to the inrush current because the current level is high enough to push the core into saturation. Fig. 2.5 shows the inrush current path through the system. Note that there is inrush-limiting circuitry already present in the drive. A pre-charge resistor of 47 Ω is used to limit the current. The aim of this study is to determine what the worst-case inrush current will be in the boost stage and whether or not to implement inrush-limiting circuitry in the boost stage.

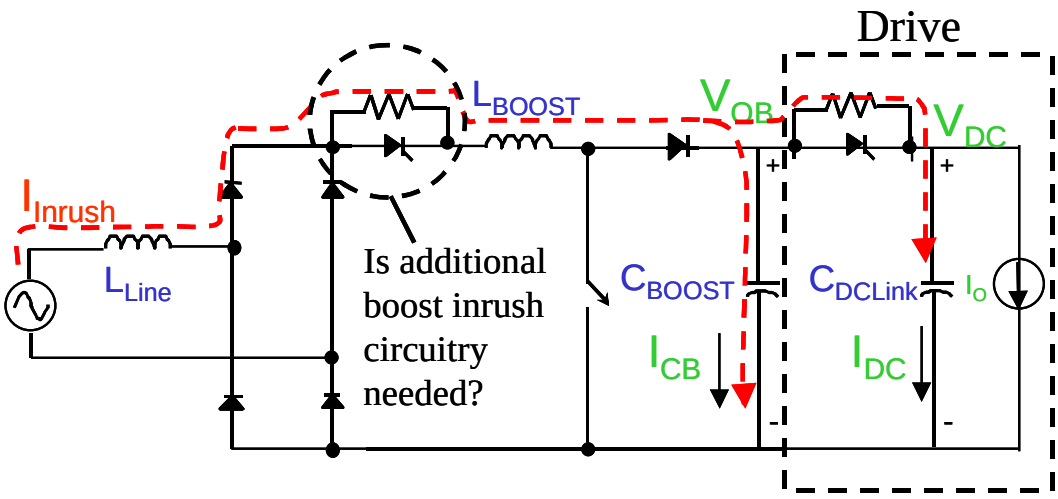


Fig. 2.5. Inrush Current Path

2.1.3.1 Inrush Simulation

Fig. 2.6 displays the SABER schematic used for calculating the inrush transient. Looking at the inrush current path shown in Fig. 2.5, it can be seen that the most important impedances affecting the inrush are the line inductance, boost inductance, boost capacitance and the drive capacitance. Therefore these parameters were varied to obtain the worst-case inrush conditions. It should be noted that the boost capacitance value was not fixed because the boost capacitor design was not completed at the time of the inrush study.

L_{LINE} = 750 µH 624 µF < C_{DCLink} < 1060 µF

10 µF < C_{BOOST} < 100 µF L_{BOOST} = 350 µH – considered to be saturated after 100 µs

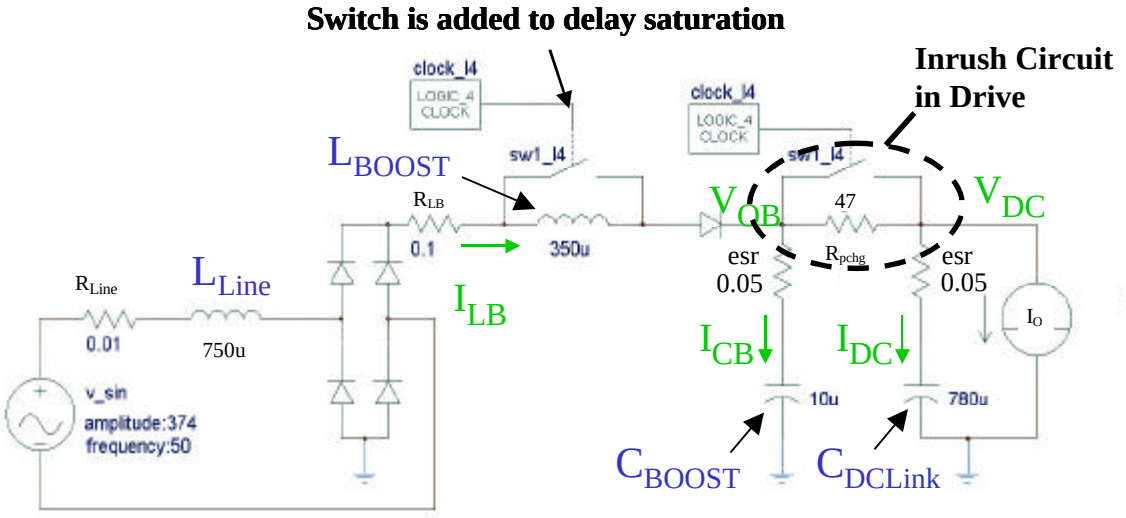


Fig. 2.6. SABER Simulation Model for Inrush Evaluation

Table 2.1. Worst-case Inrush Transient Parameters

During Start-up	During Fast Disconnect/Reconnect
R_{LB} = 0.1Ω	R_{LB} = 0.1Ω
R_{Line} = 0.01Ω	R_{Line} = 0.01Ω
R_{pchg} = 47Ω	R_{pchg} = 0Ω
L_{LINE} = 750µH	L_{LINE} = 750µH
C_{DCLink} = 1060µF	C_{DCLink} = 1060µF
C_{BOOST} = 100µF	C_{BOOST} = 100µF
L_{BOOST} = 350µH (before saturation)	L_{BOOST} = 350µH (before saturation)
I_O = 0A	I_O = 3.11A
$V_{OB(initial)}$ = 0V	$V_{OB(initial)}$ = 200V

There are two cases that result in severe inrush transients. The first case is during start-up. This occurs when the converter is first connected to the input line and all initial conditions are zero. The second case occurs when the converter is operating at full load and is disconnected from the input line and then reconnected. Table 2.1 lists the conditions for both cases.

The simulation result for the start-up transient is displayed in Fig. 2.7. After the first 100 µs of the transient a switch closes and shunts the boost inductor thus mimicking the core saturation. The boost output voltage V_{OB} over-shoots to 674 V, the boost inductor current I_{LB} reaches 130 A. Note that the boost capacitor current I_{CB} is exactly the same as the inductor current. Due to the

fact that the pre-charge resistor is still in the series path from the boost stage to the drive, the drive current I_{DC} is not significant. For the same reason the voltage overshoot of V_{DC} is not significant.

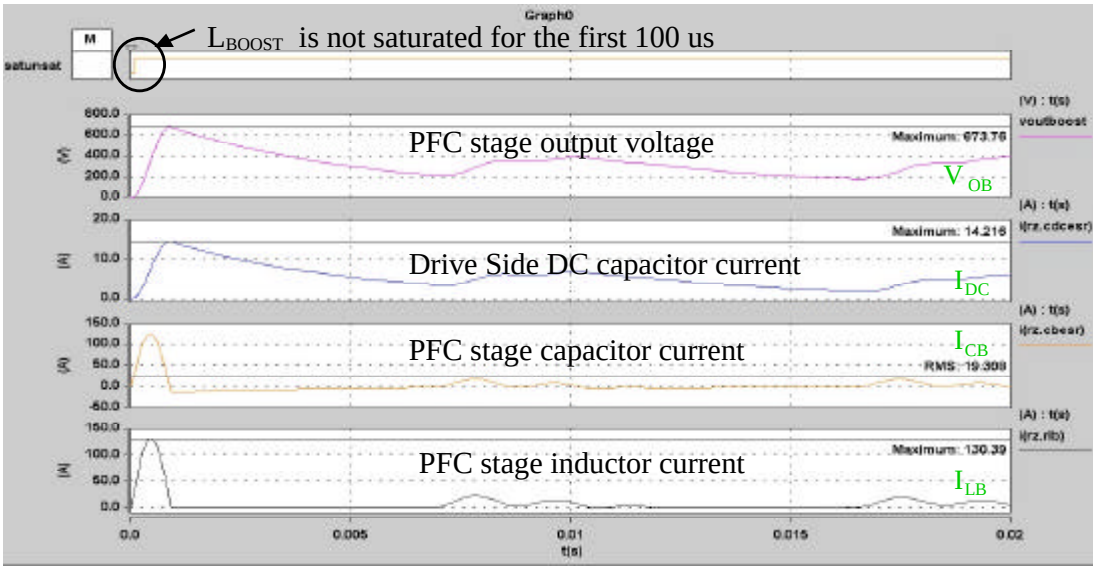


Fig. 2.7. Inrush Transient During Start-up

The results for fast disconnect/reconnect to the input line are shown in Fig. 2.8. These results are greatly influenced by the operation of the inrush circuitry in the drive. If the drive DC link, V_{DC}, is below 200 V a pre-charge resistor of 47 Ω is connected in series between the drive and the boost stage. This is the case during start-up. However during normal circuit operation when the drive DC link is above 200 V the pre-charge resistor is shunted. Thus the worst-case fast disconnect/reconnect scenario occurs when the drive is operating at full load and there is sudden disconnection. The drive DC link voltage falls exactly to 200 V and then there is a sudden reconnection. In the simulation it has been considered that the drive pre-charge resistor is still shunted when the reconnection occurs. Therefore the boost output voltage V_{OB} and the drive voltage V_{DC} are exactly the same and their initial condition is set to 200 V. The load current I_O is set to its full load value of 3.11A. A switch is used to mimic the saturation of the boost inductor after 100 μs. In Fig. 2.8 it can be seen that the boost output voltage reaches 439 V and the inductor current reaches 178 A. The results from both SABER simulations are summarized in Table 2.2 below.

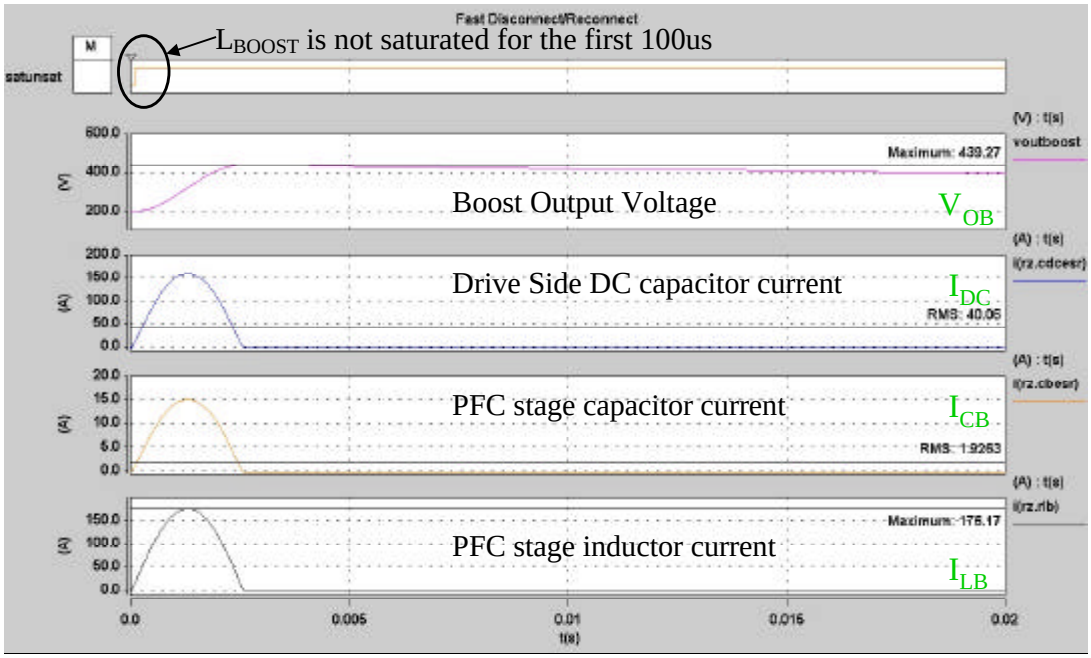


Fig. 2.8. Inrush Transient During Fast Disconnect/Reconnect

Table 2.2. Simulation Results

Start-up	Fast Disconnect/Reconnect
$V_{OB(max)}$ = 674V Δt = 5ms	$V_{OB(max)}$ = 440V
$-I_{LB(max)}$ = 131A	$I_{LB(max)}$ = 177A Δt = 2.5ms
$I_{CB(rms)}$ = 20A	$I_{CB(rms)}$ = 2A

2.1.3.2 Recommendations

When making the final recommendations for surge current and over-voltage ratings it is important to consider the length of the transient. Most data sheets give maximum nonrepetitive ratings based upon transients that last half of a 60 Hz cycle (8.3 ms). The results in Table 2.2 show that the greatest over-voltage is only applied for 5 ms and the largest current is only applied for 2.5 ms. Therefore it is more prudent to select devices with slightly lower ratings than the ones shown in Table 2.2 because they would still be robust enough to survive the inrush transients shown in Fig. 2.7 and Fig. 2.8 With these issues in mind, the recommended component ratings are listed below. These ratings are implemented as constraints in the optimization tool; therefore, the optimization tool does not choose any components that cannot satisfy these maximum ratings. A cost analysis has shown that the cost of sizing the components for the

ratings shown below is cheaper than choosing smaller components and adding inrush limiting circuitry to the boost stage. Additionaly inrush circuitry would also decrease the overall reliability of the converter.

Boost Capacitor: V_{max} = 400V I_{max} = 20Arms

Rectifier Bridge: I_{FSM} = 150A

Fast Diode: I_{FSM} = 150A

Boost Switch: V_{BR} = 600V.

2.1.4 Layout

Layout parasitics have a significant effect on the conducted EMI noise, especially those in the loops that carry high-frequency switching currents. In switch-mode power supplies, these loops usually involve semiconductor devices. For the boost circuit, the high di/dt loop is identified and shown in Fig. 2.9.

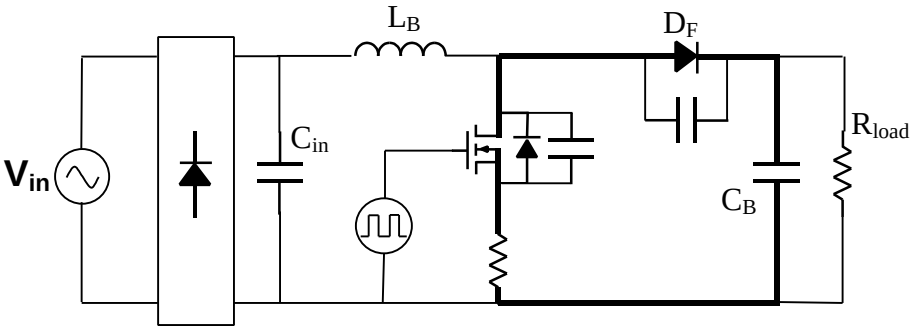


Fig. 2.9. High di/dt Path

The thick lines indicate the critical di/dt loop. To reduce the effect of the parasitic loop inductance, which may cause EMI noise due to high di/dt, this loop area needs to be as small as possible.

For a hard switching circuit, the device characteristics and gate resistance mainly determine the dv/dt slew rate. To suppress the common mode (CM) noise, which is related to C·dv/dt, the common-mode capacitance needs to be as small as possible. In the boost converter, this CM

capacitance is contributed mainly from the capacitance between the IGBT collector and the earth ground. The thick lines indicate the high dv/dt traces in Fig. 2.10. To reduce the effect of the parasitic capacitor, which may cause CM noise due to high dv/dt, the total area of these traces need to be as small as possible.

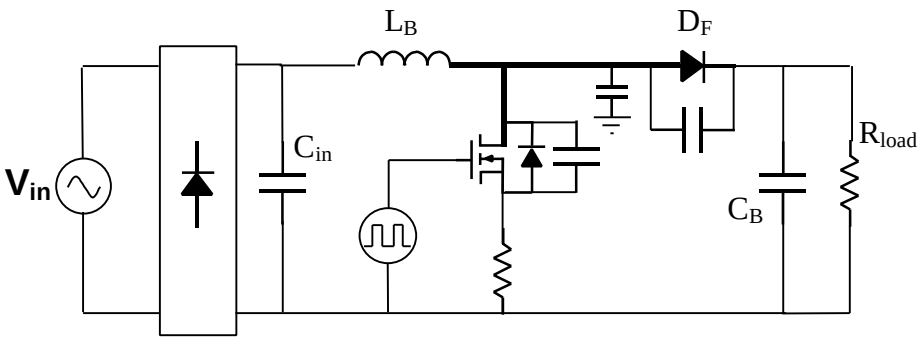


Fig. 2.10. High dv/dt Node

As stated above, the collector to ground capacitance is the main cause of CM noise. One way to reduce it is to minimize the area of the collector trace. A second way would be to consider the position and orientation of the switch heat sink. Whether the switch is isolated or not, the distance from the switch heat sink to ground should be maximized. The orientation of the switch heat sink should also be considered. The surface area of the heat sink that is directly parallel to the ground plane should be minimized. Considering the case where the switch heat sink is discrete and the circuit is packaged in a grounded metallic enclosure, Fig. 2.11 shows that the distance "D" should be maximized. Fig. 2.11 also shows that the area "A" should be minimized. Of course, the main function of the heat sink is too cool the switch. Therefore the tradeoff between the thermal efficiency of the heat sink and the magnitude of the collector to ground capacitor must be considered in the final layout. The layout design used for testing is shown in Appendix Three**.**

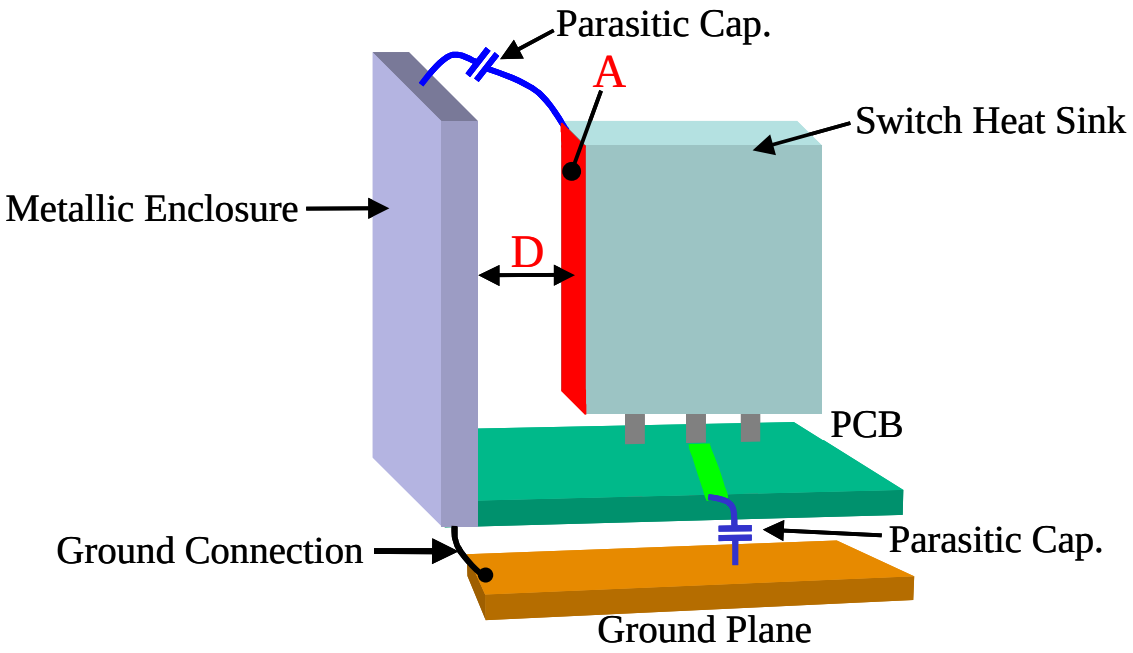


Fig. 2.11. Heat Sink Orientation

As mentioned above, reducing the high dv/dt and di/dt traces can attenuate EMI as well as floating the heat sink. However it also is desirable to have a high performance input capacitor (C_{in} in Fig. 2.10) because this can shunt differential mode noise. Overall, it is beneficial to have large spacing between the ground plane and the PCB. The measurement of parasitic elements is covered in Chapter Four.

2.2 Functionality

In order to ensure that the final product is robust, hardware tests have been performed under high line conditions and US line conditions.

2.2.1 Operation at High Line

In normal circuit operation, a boost converter always produces a higher output voltage than input. However, in retrofit applications there are usually pre-existing limits on output voltage and input line voltage. Due to these limits, the boost output voltage may be less than the input line voltage for some parts of the line cycle, see Fig. 2.12. In Section 2.1.2, it has been determined that the lowest regulated boost output voltage was 351 V. This means that the line voltage would be larger than the input voltage for $V_{Line} > 248$ Vac.

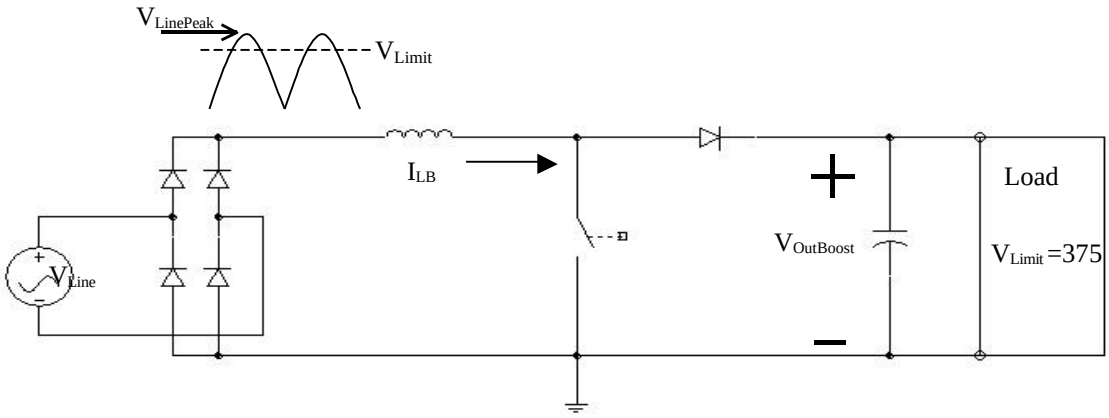


Fig. 2.12. Boost PFC Circuit

2.2.1.1 Initial Testing

From Fig. 2.13, it can be seen that the high line condition results in distortion of the inductor current, I_{LB}, and $V_{OutBoost}$ becomes unregulated varying from 340 V to 400 V. This could be very dangerous because the maximum allowable voltage on the drive capacitor is 400 V. This test is performed on a 100 kHz prototype. An input voltage feedforward loop has been added to provide power balance between input and output power.

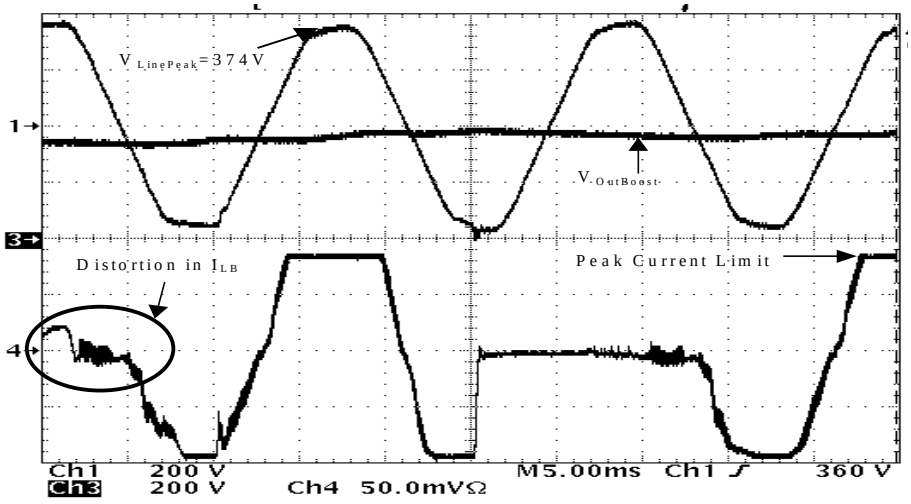


Fig. 2.13. Experimental Results From High Line Test on the SE Prototype

Test Conditions for Fig. 2.13

V_{LINE} = 264 Vac P_{OUT} = 300W V_{OB} = 370V

Another test has been performed with the SABER switching model displayed in Fig. 2.14 (the SABER models are discussed further in Chapter Three). Here the feedforward circuit is modeled as a simple gain to attain power balance. The simulation results are shown in Fig. 2.15. Note that this test does not indicate instability at high-line. It is also important to recognize that the test shown in Fig. 2.15 is at full load while the test shown in Fig. 2.13 is at light load.

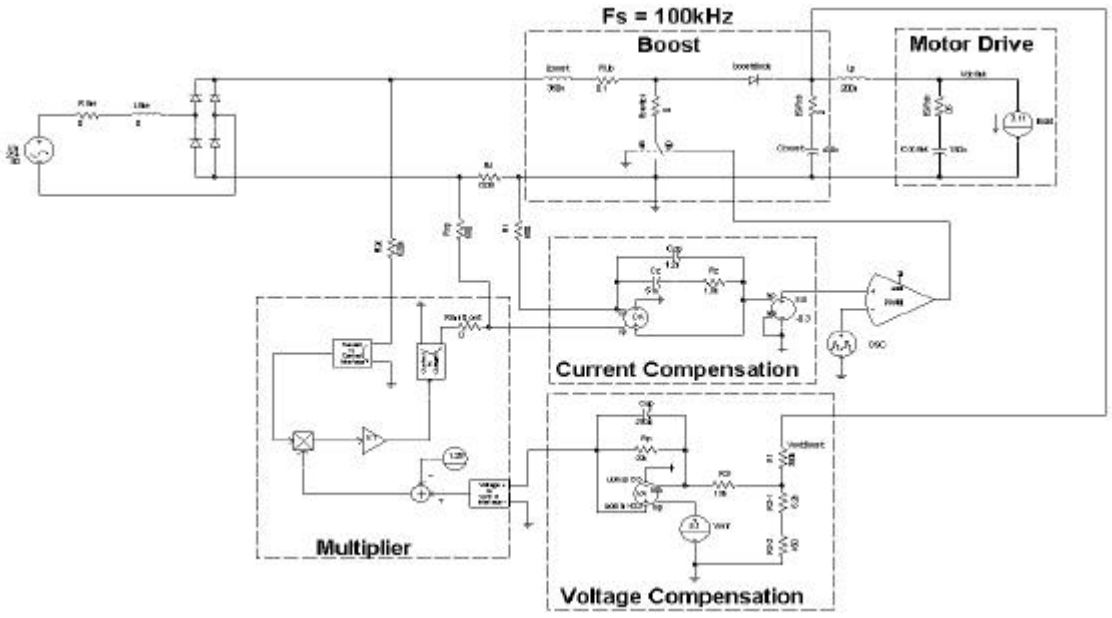


Fig. 2.14. 100 kHz SABER Switching Model

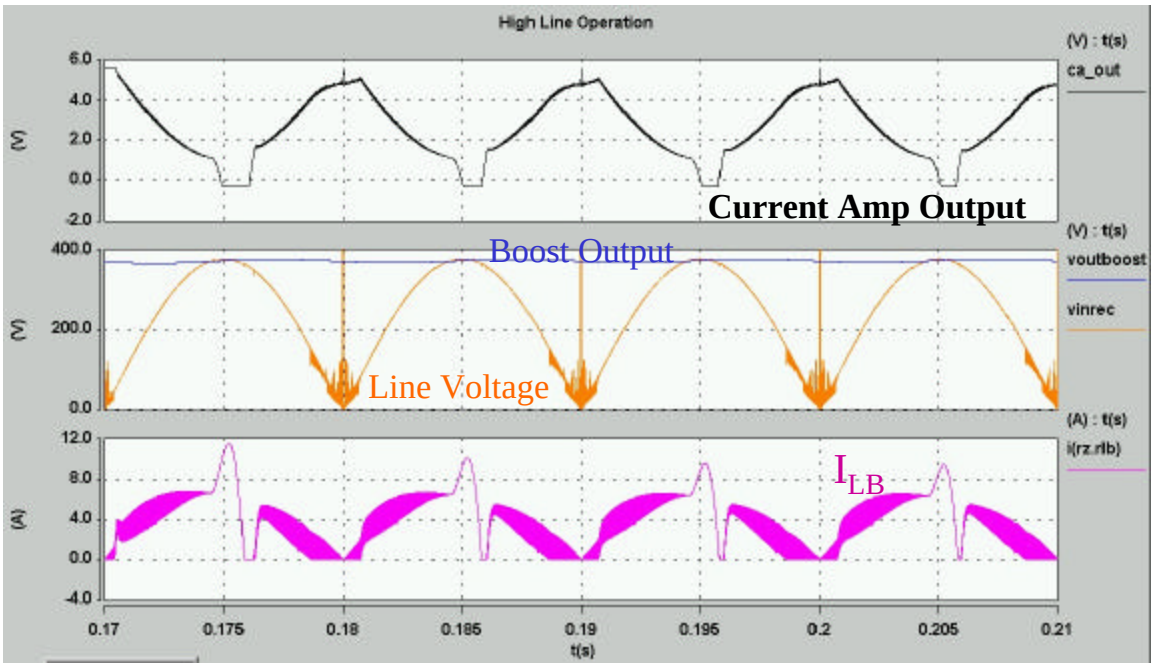


Fig. 2.15. Simulation Waveforms at High Line

Simulation Test Conditions for Fig. 2.15

V_{LINE} = 264 Vac P_{OUT} =1150W V_{OB} = 370V

2.2.1.2 Final Testing

Table 2.3 lists the components/parameters used to test the high line condition on a different prototype. This design is based upon early results from the discrete optimization.

Table 2.3. Component List

Component	Reference
Switch	Intersil: HGTP7N60A4
Anti-parallel diode	Phillips: BYM36C
Fast diode	IR: MUR1560
Bridge Rectifier	Diodes Inc: GBJ806B
Boost Inductor	Micrometals: T225-26: 98 turns of 16AWG
Common mode choke	SDI142-21
Cx(2)	2.24 µF
Cy(2)	10 nF
Boost capacitor	100 µF
Switching Frequency	35kHz

The converter is tested under high line conditions with light load and full load. Fig. 2.16 displays the results of the test at high line and light load. In the condition shown in Fig. 2.16, the converter behaves as a rectifier. No instability has been observed for this operating point. Fig. 2.17 shows the converter operating at the threshold between boost mode and rectifier mode where V_{IN} equals 261 Vac. The system is still stable. Once the input voltage is reduced the converter operates in normal boost operation.

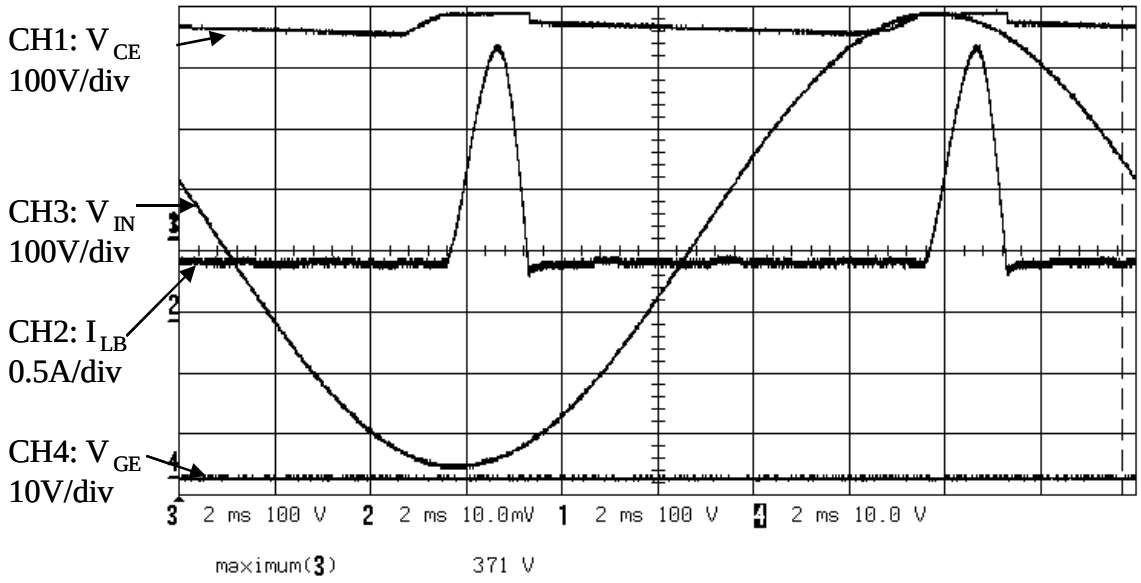


Fig. 2.16. Experimental Results with V_{IN} = 264Vac, I_O = 245mA, P_{Out} = 89W, V_{OB} = 364V

The operation at high-line is also verified at half load. Fig. 2.18 shows the converter operating at half power under high-line conditions. Note that the threshold occurs at V_{IN} equal to 251 Vac and at the highest line condition of 264 Vac the output voltage rises to 357 V. The same test has been performed under full load. Fig. 2.19 shows the results of this test. The results are very similar except that the threshold voltage is 248.9V for the full load case.

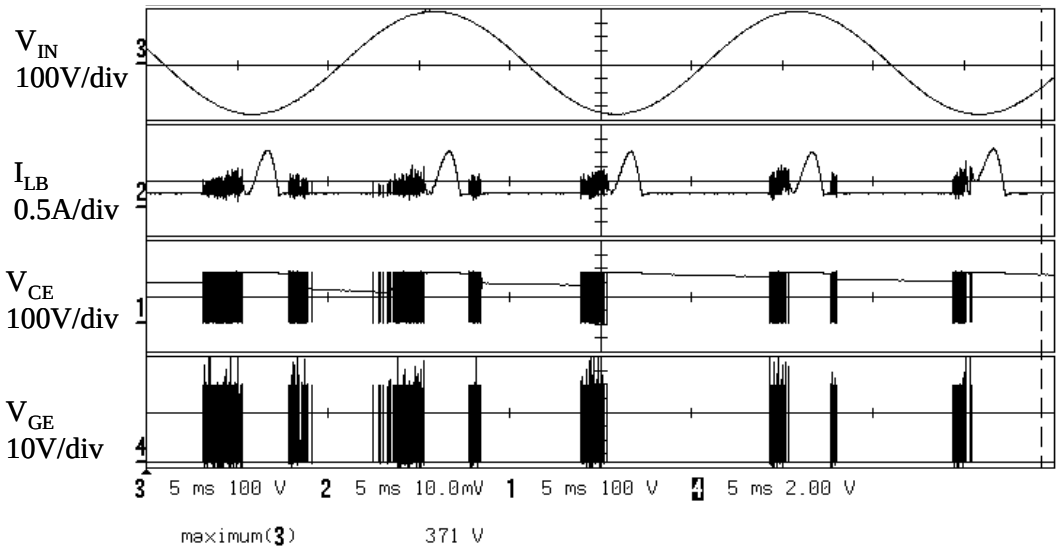
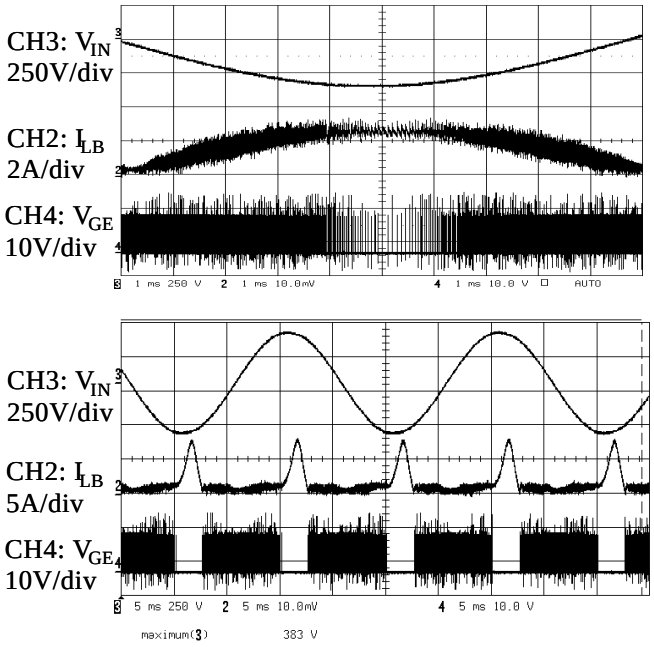


Fig. 2.17. Experimental results with V_{IN} = 261Vac, I_O = 245mA, P_{Out} = 89W, $V_{OB} \cong$ 364V



V_{IN} = 251Vac
V_{OB} = 356V

V_{IN} = 264Vac
V_{OB} = 357V

Fig. 2.18. Experimental Results for High Line Operation with I_O = 1.57 A

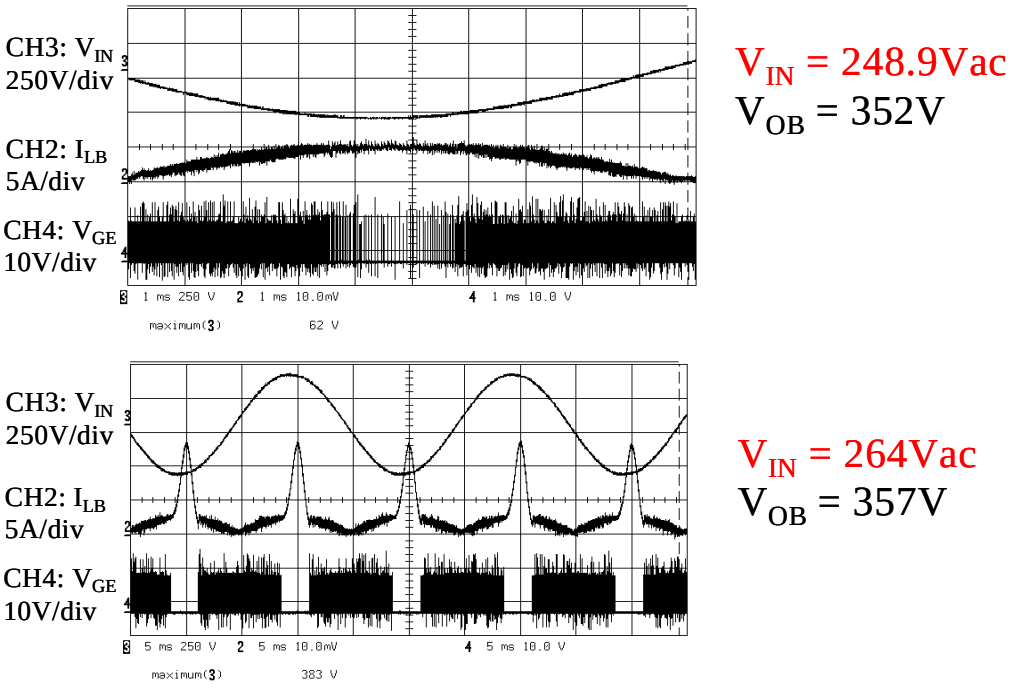


Fig. 2.19. Experimental Results for High Line Operation with I_O = 3.3 A

2.2.1.3 Conclusions

The boost PFC circuit is able to operate as a rectifier when the input voltage becomes greater than the output voltage. Thus no additional circuitry is needed to facilitate high line operation. This result makes sense because during the high line condition, the voltage loop forces the converter to stop switching. This is because the output voltage is too high and therefore the voltage loop is saturated at its most negative value. As the input voltage drops, the output voltage would drop and therefore the voltage loop reference would start to rise. This causes the voltage error signal to be pulled out of its negative saturation thus allowing the converter to act in the normal boost mode.

2.2.2 North American Line

The circuit is tested with the components listed in Table 2.3. The US line tests are done considering a 20% line variation. In other words,

$$96 > V_{IN} > 144$$

Fig. 2.20 shows measurement waveforms at light-load and full-load for a V_{IN} equal to 96 Vac. Note that for the US line application, the full-load is considered to be 1.57 A or 550 W. Fig.

2.21 shows results from the test at the US nominal line. This test is also performed at light-load and full-load. Fig. 2.22 verifies that the circuit operates at US high line.

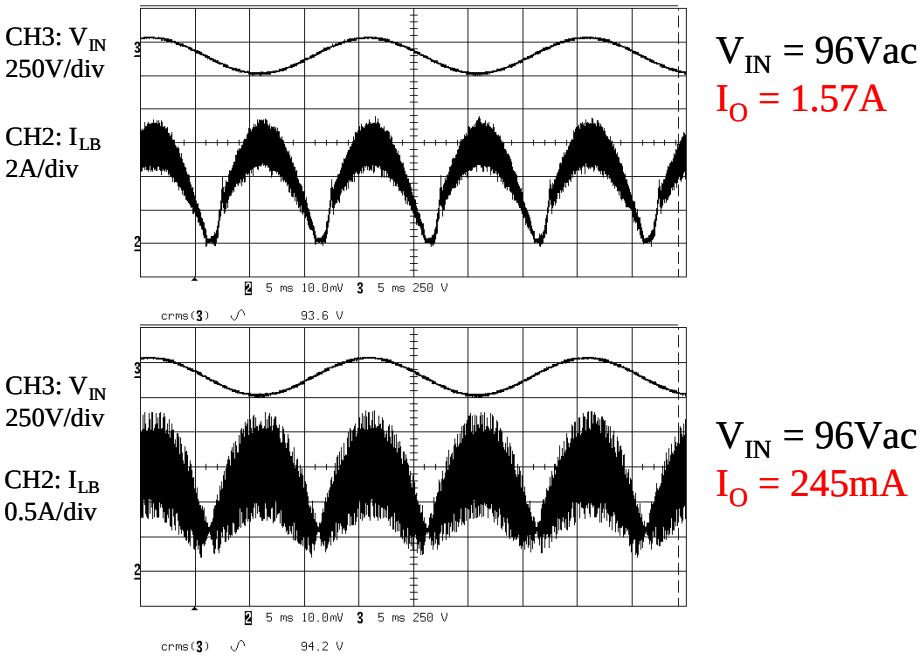


Fig. 2.20. US Low Line

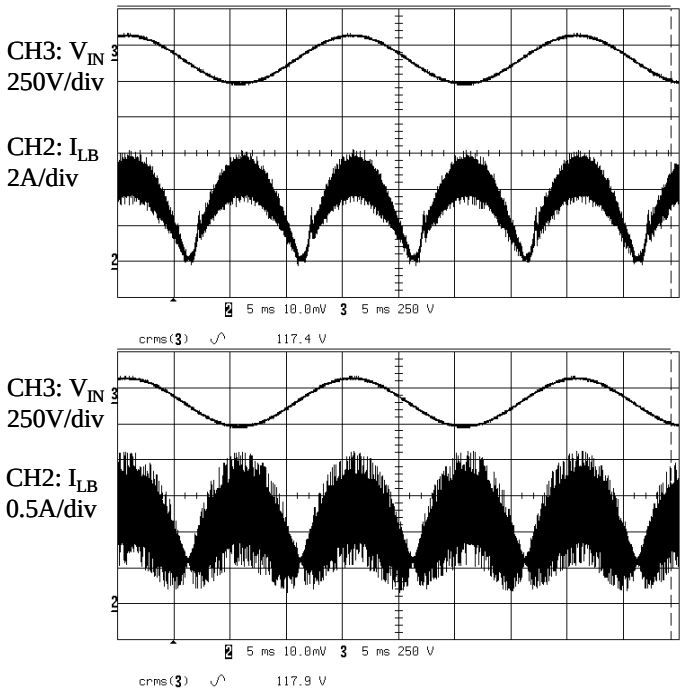


Fig. 2.21. US Nominal Line

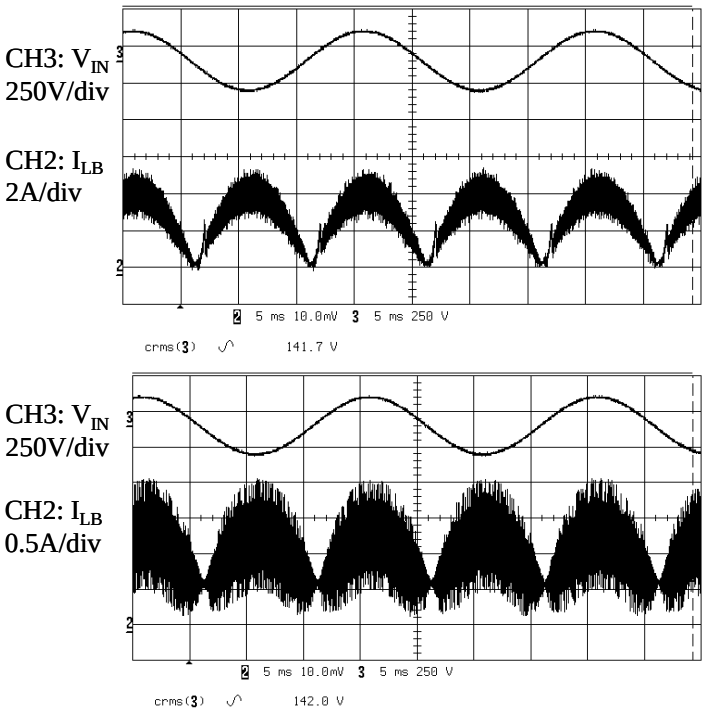


Fig. 2.22. US High Line

2.2.2.1 Conclusions

The circuit performs well throughout the US line voltage range and output power range. Therefore this circuit can provide PFC for input voltages ranging from 96 Vac to 248.9 Vac. From the results of the tests at high-line and tests at US line, it is apparent that the feedforward circuitry is not needed.

2.3 Summary

An average current mode control design has been completed to provide unity power factor. A boost capacitor and output voltage has been chosen considering the tradeoff between maintaining PFC for a wide input voltage range and the size of the boost capacitor. The worst-case inrush values have been identified and the recommended device ratings can be implemented as constraints in the GA. Layout guidelines have been developed to minimize common and differential mode EMI. It has been verified that the converter can operate under high line and US line conditions. Once good electrical models are developed, the GA can be used to design the rest of the boost PFC circuit.

Chapter Three

3 Modeling

The goal of the modeling effort is to provide simulation tools that can be used by the GA to predict the performance of the actual circuit. Models also provide a way to evaluate the performance of a certain design before implementing that design in the hardware. Because many simulations can be performed in a relatively short time, circuit modeling can be a valuable time saving tool for the circuit designer.

3.1 Electrical Models

Electrical models are used to evaluate the steady-state and transient performance of the circuit. The following SABER models are not incorporated into the GA because they require time intensive simulations. They have been used to accurately model the various functions of the control law and the safety functions on the L4981A control IC. The GA uses steady-state algebraic equations to model the electrical behavior. These equations are described in [13].

3.1.1 SABER Switching Model

The purpose of a switching simulation is to verify the transient and steady state performance of a particular converter. The SABER switching model incorporates many of the features of the L4981A controller. These features include, over-voltage and over-current protection, and under-voltage lockout. Fig. 3.1 shows the SABER switching model for a specific design. A more detailed explanation of the switch model can be found in Appendix Two. The control parameters have been selected based upon the design procedure in Appendix One. Fig. 3.2 shows results from a SABER switching model. The control design is adequate to regulate the converter under transient conditions.

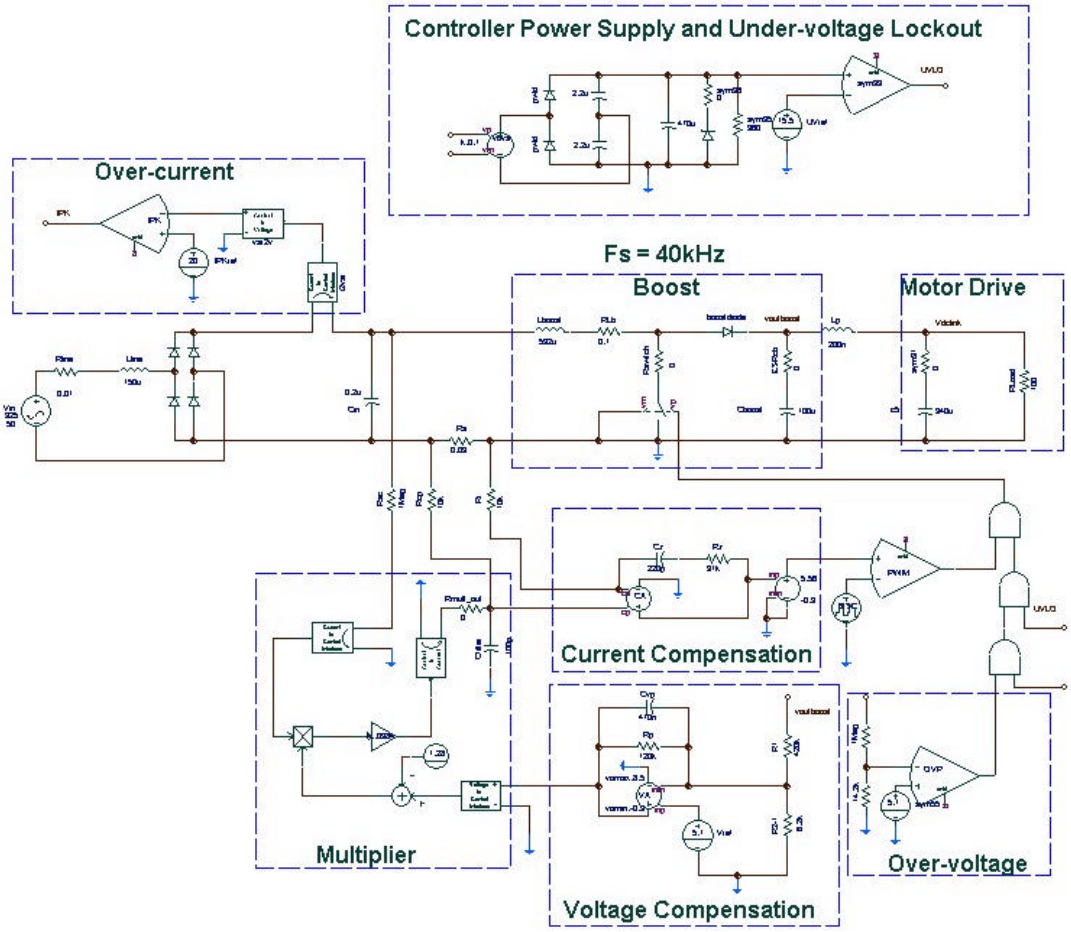


Fig. 3.1. SABER Switching Model

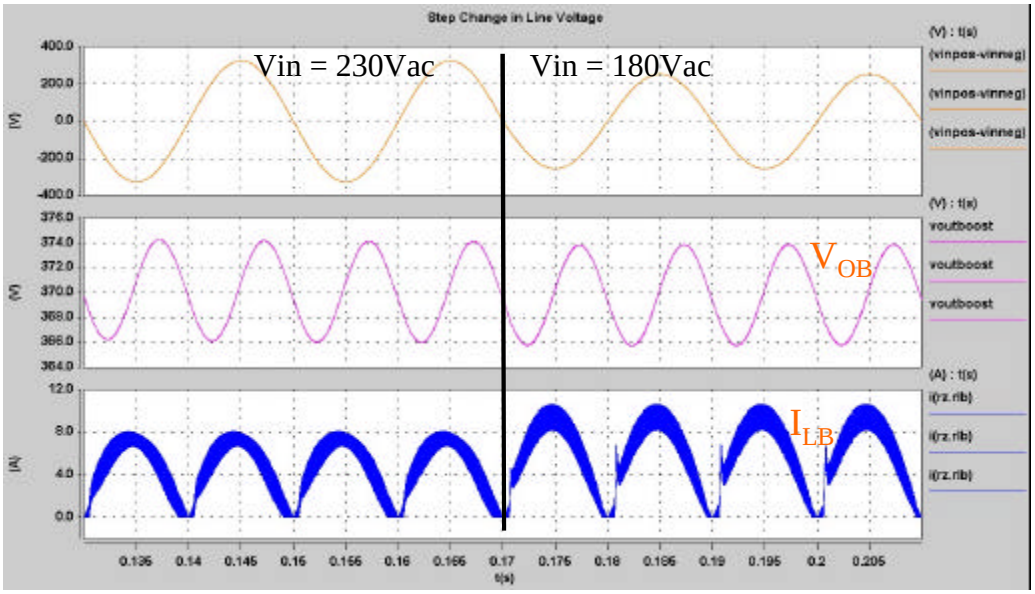


Fig. 3.2. Simulation Results for a Line Transient

3.1.2 SABER Average Model

The benefit of an average model is that the simulation time is greatly reduced. This is due to the fact that the commutation of the switch and the diode is averaged. Although the average model cannot predict exact electrical behavior, it can be used to examine the general behavior of the system. Fig. 3.3 shows the SABER schematic of the average model. Appendix Two provides more detail about the average model.

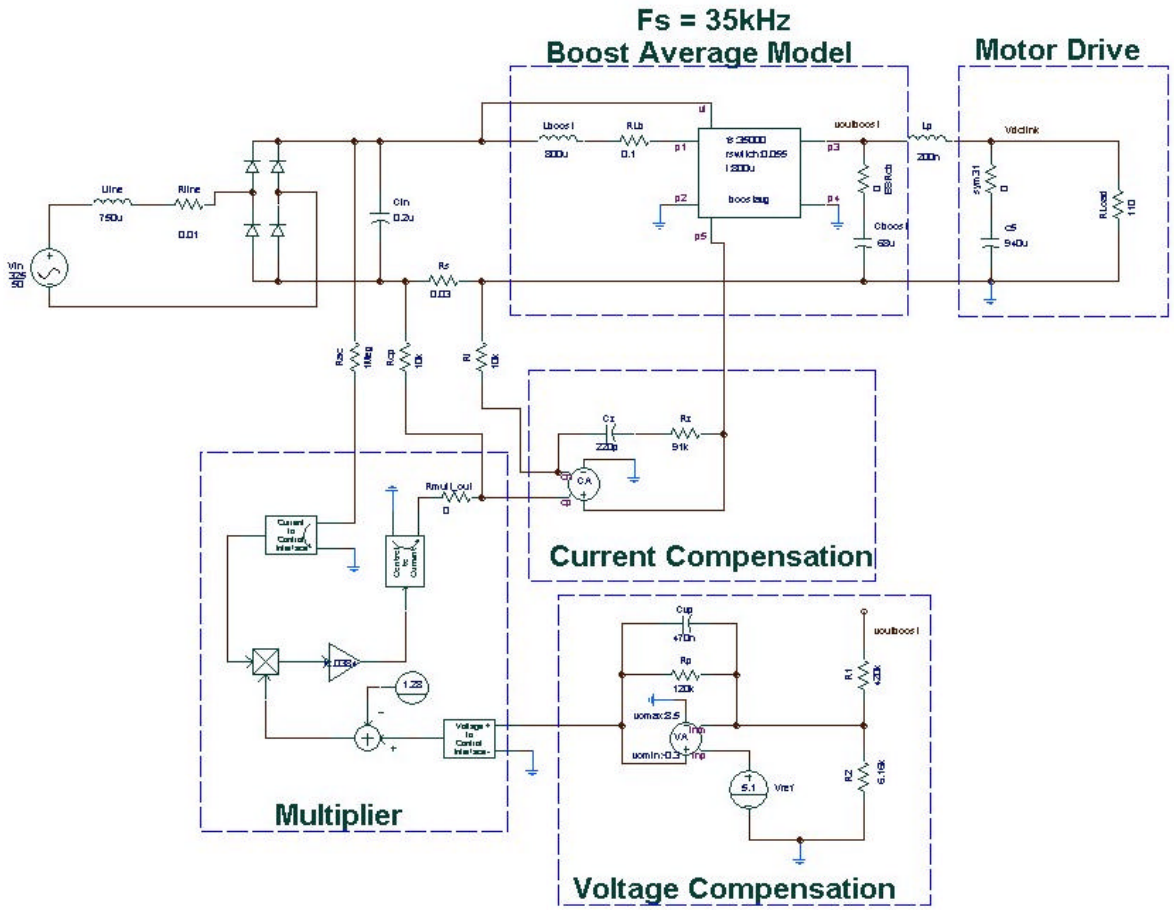


Fig. 3.3. SABER Average Model

3.2 EMI Models

For any EMI prediction, it is necessary to characterize the main parasitic elements in the circuit. Device parasitics and magnetic component parasitics contribute greatly to the EMI levels. The high frequency boost PFC circuit shown in Fig. 3.4 includes some of the most important parasitics. By studying the DM and CM paths, it is possible to identify the parasitics

that would contribute most to the EMI level. From Fig. 3.4, it is can be determined that the most important parasitic elements are the collector to ground capacitor, the resonance of the boost inductor, and the leakage of the CM choke. Therefore these parasitics are measured while the rest are estimated. The collector to ground capacitor (C_{Dg} in Fig. 3.4) provides the main coupling mechanism for CM EMI [34]. The CM current is generated by the high dv/dt applied at the collector node. The main impedance to DM current is the boost inductor. As long as the boost inductance maintains high impedance, the DM current cannot propagate back into the line. However all inductors have a parasitic inter-winding capacitance. The boost inductor can be modeled as a parallel resonant circuit. In this way, it is possible to determine at which frequency the boost inductor impedance begins to fall. At this point, the DM current would propagate much more easily back into the line. The leakage of the CM choke is a parasitic element that can be used to attenuate DM EMI. Since the leakage inductance of the choke is caused by leakage flux, this parasitic can be used over the entire frequency range. However, the leakage of the CM choke is often small therefore the boost inductor must still provide the bulk of the DM EMI attenuation.

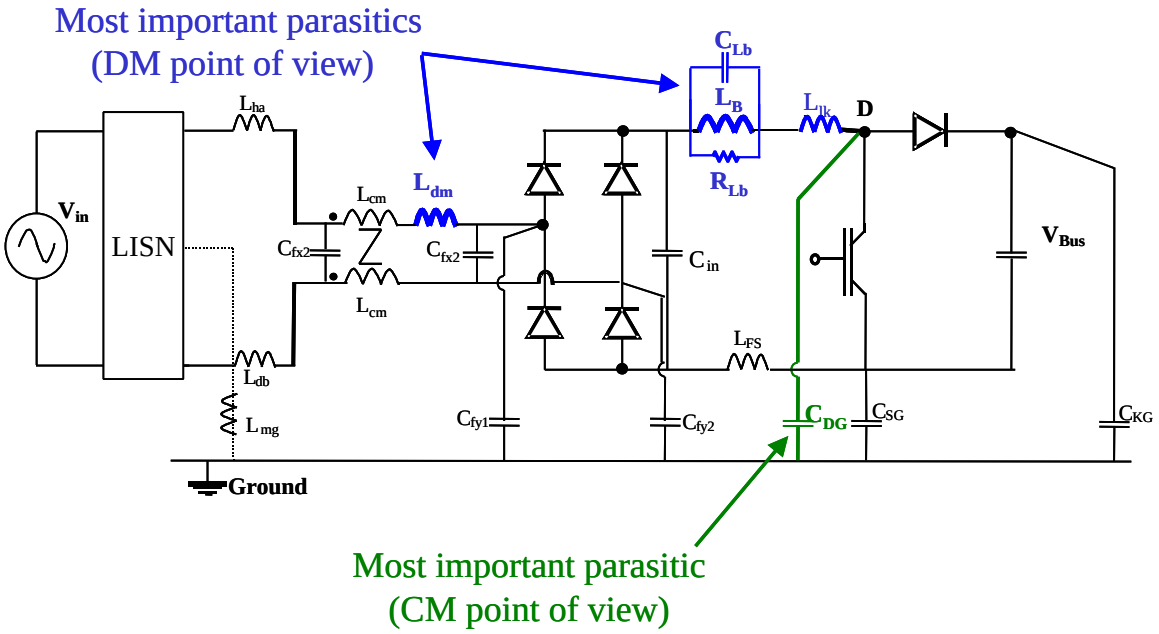


Fig. 3.4. High Frequency Model of the Boost PFC Circuit

3.2.1 Common Mode Parasitic Measurements

The collector to ground capacitance is the most difficult parasitic to measure. This capacitance is highly dependent upon layout. The capacitance is very sensitive to the distance and orientation of the collector node to the ground. There are two places where the collector is close to the ground plane. Since the heat sink is tied to the collector, the capacitance from the heat sink to the metallic case is significant and the capacitance from the collector trace to the ground plane is also significant. Fig. 3.5 displays the position of each capacitance. The capacitances are measured separately using a Hewlett Packard 4194A network analyzer. However, it is important to note that the measurement set-up itself can influence the results. The leads of the network analyzer combine to form a series RLC circuit. The impedance characteristic of such a circuit is displayed in Fig. 3.6. In this case, it is only interesting to know the capacitance value; therefore the measurement data should be taken in the lower frequency range where the characteristic is capacitive.

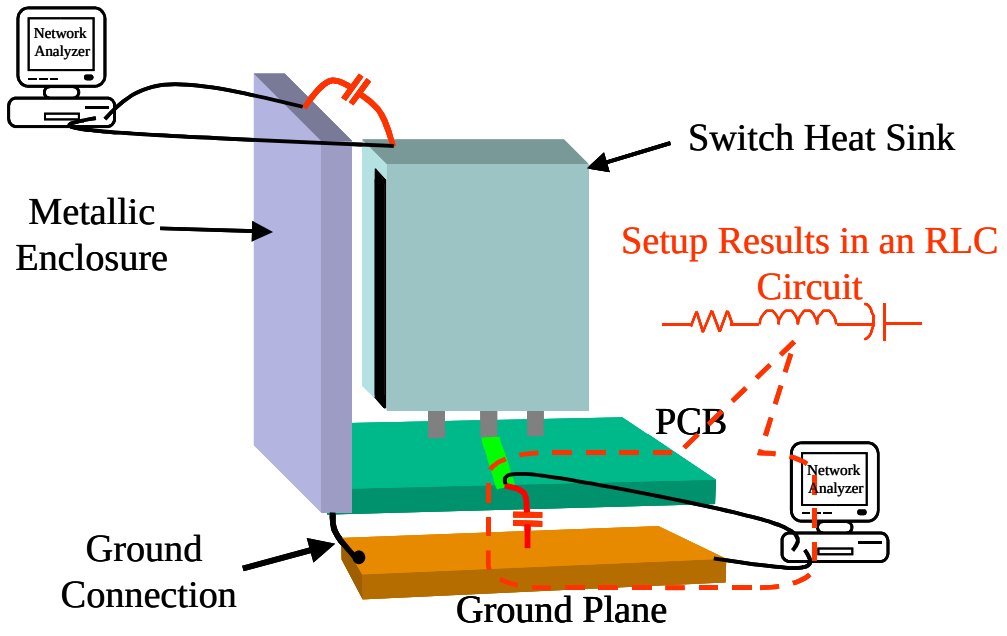


Fig. 3.5. Measuring Collector to Ground Capacitance

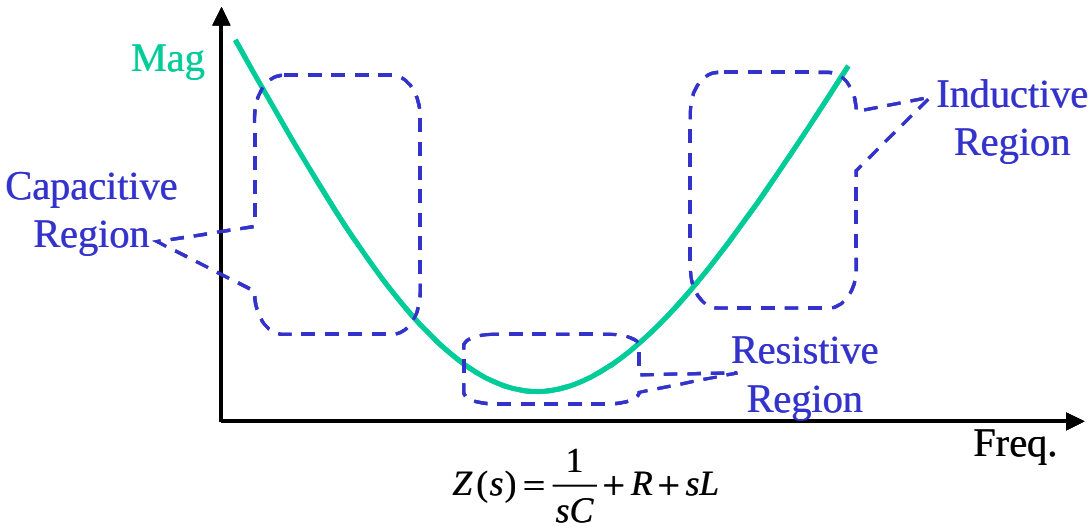


Fig. 3.6. Series RLC Circuit Frequency Response

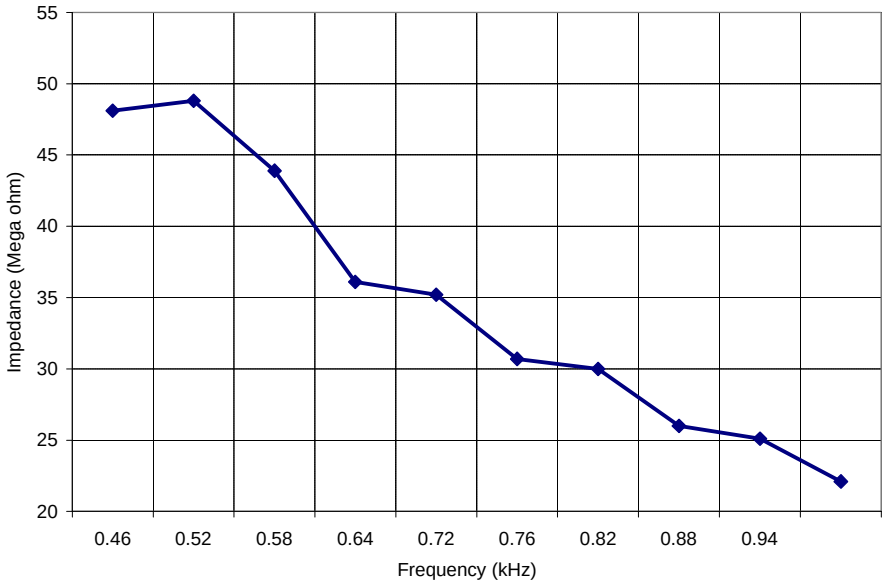


Fig. 3.7. Measurement Data for the Collector to Case Capacitance

Fig. 3.7 shows measurement data from the network analyzer. Normally, there is significant noise in the low frequency portion of the measurement. Since the data in Fig. 3.7 has been manually extracted, the low frequency noise is not included. Also the data only goes up to frequencies where the impedance is still capacitive. Therefore in this frequency range, the capacitance should be fairly constant and the resistive and inductive behavior of the measurement leads does not have a great influence. Note that this measurement procedure is

different than setting an equivalent circuit in the network analyzer and simply asking for the component values. Since the data is in the capacitive region, (3.1) can be used to compute the capacitance value. Each data point from Fig. 3.7 gives a slightly different capacitance value, however the variation is very small. After averaging the different capacitance values, the capacitance from collector to case is 6.6 pF. The capacitance from the collector trace to the ground plane has been measured exactly the same way and is 14.5 pF thus the total collector to ground capacitance is 21.1 pF. Table 3.1 summarizes these results.

$$X_C = \frac{1}{2p \cdot f \cdot C} \tag{3.1}$$

Table 3.1. Measurement Data for CM Capacitance

Component	Value
Capacitance from Heat Sink to Metallic Case	6.6 pF
Capacitance from Collector Trace to Ground	14.5 pF
C_{TOTAL}	21.5 pF

3.2.2 Differential Mode Parasitic Measurements

The network analyzer also has been used to measure the parallel RLC network in the boost inductor. This case is different than the measurement of the collector to ground capacitance because the lead inductance and resistance is very small compared to the inductor. Therefore the network analyzer is used to compute an equivalent parallel RLC circuit shown in Fig. 3.8. The results of that measurement are shown in Table 3.2. The leakage of the boost inductor is modeled using (3.2) [35]. Where $Lb_{Leakage}$ is the leakage inductance in micro Henries, *Tolerance* is a unitless dimension that accounts for manufacturing variations, n is the number of turns of wire on the core, A_C is the cross-sectional area of the core in square centimeters, and l_m is the equivalent length of the magnetic path in the core in centimeters. For the core listed in Table 3.2, these values can be easily found in the Micrometals catalogue [36].

$$Lb_{Leakage} = \left(1 - \frac{Tolerance}{100}\right) \cdot \left(292 \cdot n^{1.065} \cdot \frac{A_C}{l_m \cdot 10^8}\right) \quad (\mu H) \tag{3.2}$$

Table 3.2. Boost Inductor Measurements from the Impedance Analyzer

Boost Inductor: 184-26 Core with 123 turns of 16 AWG ***Tolerance = 50%, n = 123, A_C = 1.88 cm^2, lm =11.2 cm***	
R	25.8 kΩ
L	1830 µH
C	25.0 pF
$Lb_{Leakage}$	41 µH

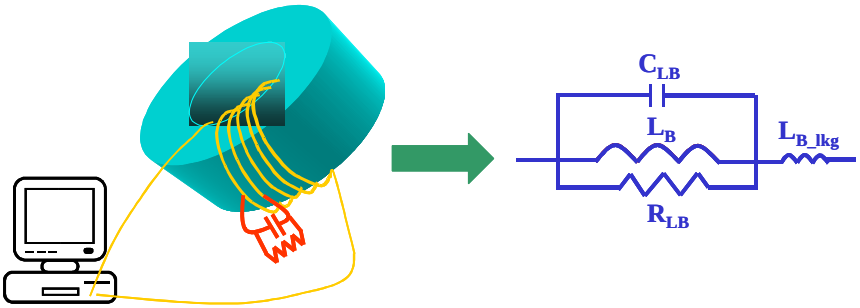


Fig. 3.8. Boost Inductor RLC Measurement

Additionally, the saturation of the boost inductor must be considered. Theoretically, the maximum current ripple occurs when the duty cycle is 0.5. Fig. 3.9 shows the current and duty cycle waveforms for the ideal boost PFC circuit. Due to the varying input current, the DC magnetizing force applied to the core varies throughout the line cycle. Thus the core is operating at different points on the hysteresis curve. For the chosen Micrometals –26 material, current peak and number of turns this results in operation along parts of the hysteresis loop where the permeability starts to decrease. This causes a significant drop in the inductance value. When the core starts to saturate, the current rises at a faster rate thus causing the ripple to be higher. In PFC circuits, the highest current value occurs at the peak of the line voltage, see Fig. 3.10. This point may or may not be where the duty cycle is 0.5. The saturation inductance of the boost inductor has been determined by measuring the inductance at the point in the line cycle where the current ripple is the greatest. Fig. 3.11 displays the method to measure the inductance. For the prototype measured below, the value of L_{SAT} is 901 µH. This value is less than half of the inductance measured at zero DC bias (see Table 3.2). Therefore, when predicting EMI levels, the saturation of the boost inductor must be taken into account.

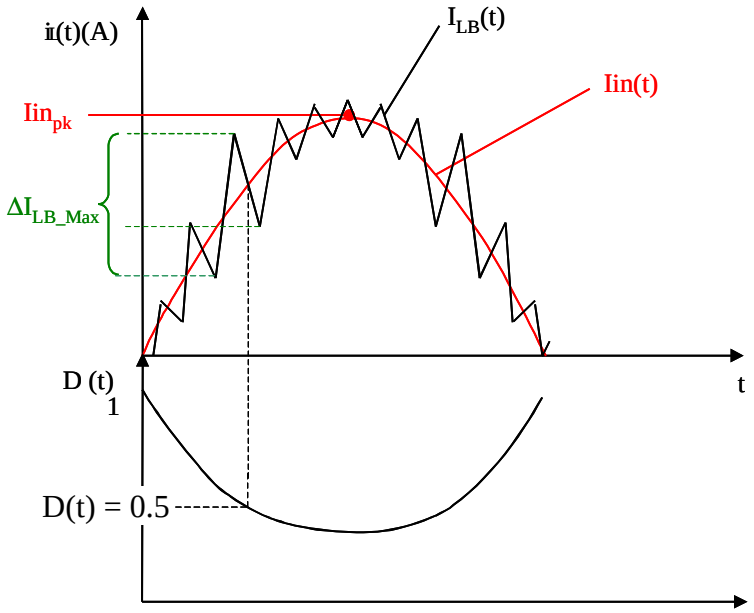


Fig. 3.9. Ideal Current Ripple

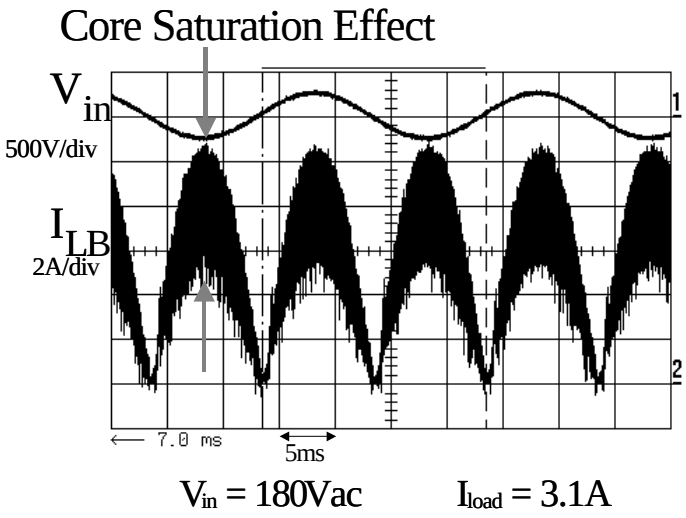


Fig. 3.10. Core Saturation in a Real Circuit

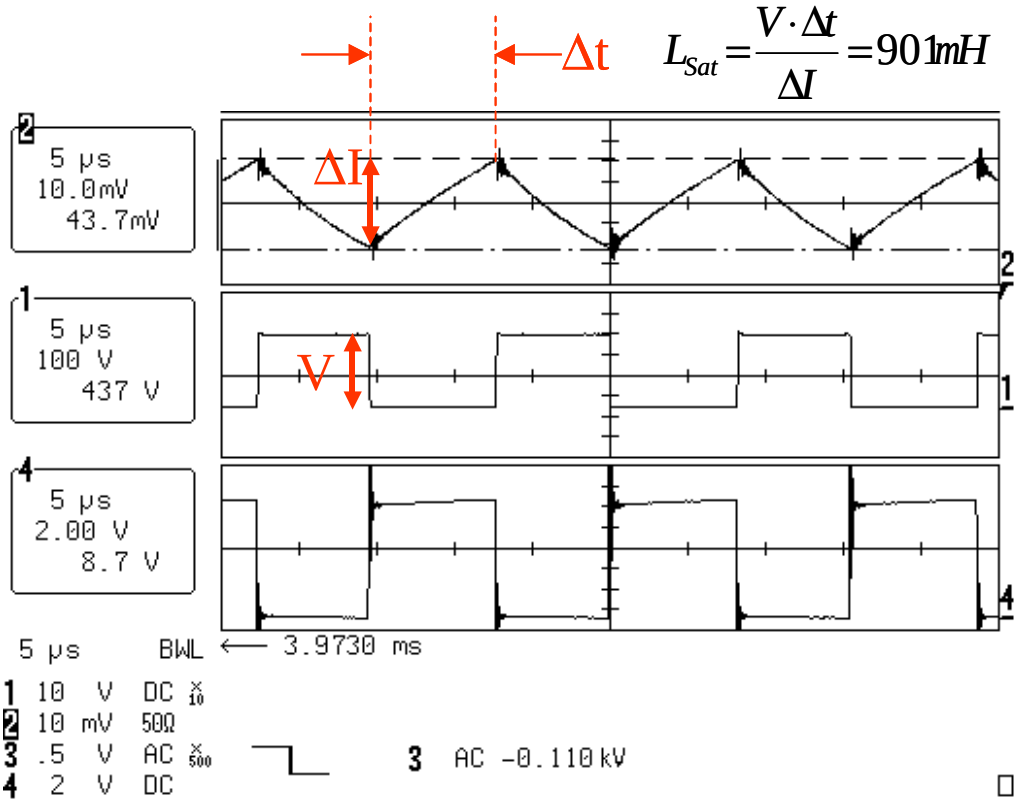


Fig. 3.11. Experimental L_{SAT} Measurement

3.2.3 Common Mode Choke Characterization

The input filter choke affects both DM and CM propagation. The network analyzer is used to determine the DM and CM inductance of the choke. Fig. 3.12 shows the test for both values. It is important to note that the configuration shown in the right half of Fig. 3.12 gives twice the differential mode inductance ($L_{leakage}$ = 2*L_{DM}). Also, the parasitic capacitance of the choke is not considered because this normally affects the very high frequency range. As mentioned before, the EMI prediction is only used for predicting lower frequencies. Table 3.3 shows the results of the tests on the CM choke. The DM inductance is very small compared to the CM inductance because the core itself is small and the windings are fairly close together. This reduces the amount of leakage inductance therefore reducing the amount of DM inductance.

Table 3.3. CM Choke Parameters

CM Choke: SDI 142-22	
L_{CM}	3.36 mH
$L_{Leakage}$	7.95 µH (0.24% of L_{CM})

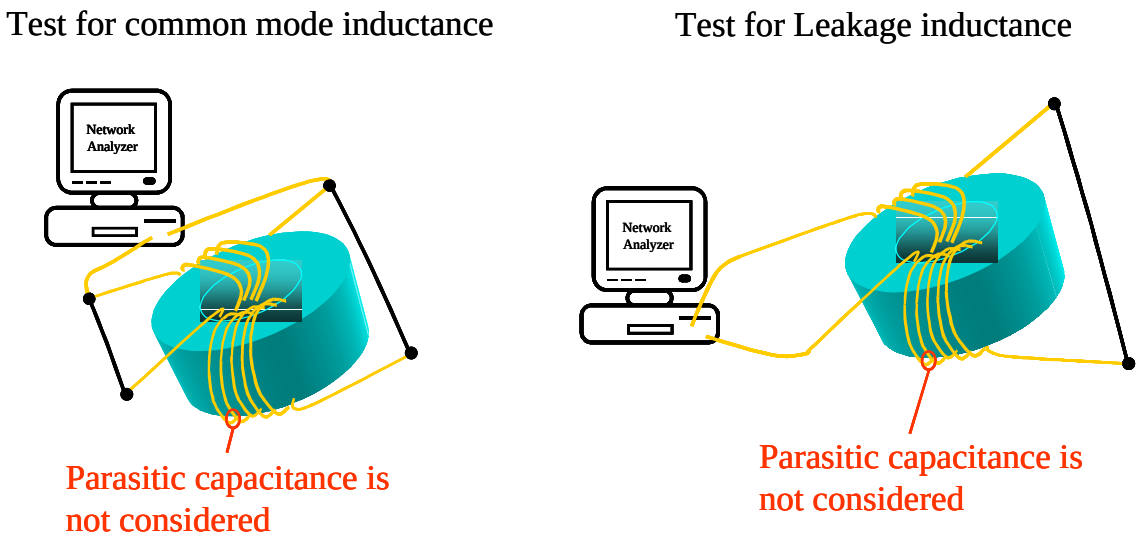


Fig. 3.12. Leakage Inductance and CM Inductance Measurements

3.2.4 SABER EMI Model

Now that the main parasitic elements have been identified it is possible to develop circuit models to predict the EMI. The SABER schematic shown in Fig. 3.13 includes the parasitics measured above plus parasitics in the CM and DM capacitors in the input filter. Note that the boost inductor and CM choke have different parasitics values than listed above. The CM choke shown in Fig. 3.13 is the SDI142-21 and the boost inductor parameters are based on the Micrometals T225-26 core with 98 turns of 16 AWG. To improve convergence issues with SABER's numerical solver, the CM ground is not the same as the SABER ground node. Using this method allows the SABER ground node to be the DC minus point on the output and a reference in the controller. The voltage loop is left open in the model for faster times to steady-state. In fact with the initial condition set to the steady-state value on the boost output capacitor, the converter starts immediately in steady-state operation. This is extremely useful because any FFT done in SABER must be done with a fixed time step in order to guarantee the proper resolution. Fig. 3.14 displays the FFT for the DM noise signal from the noise separator. Note

that an ideal switch and diode are used in this model. More information is provided about the SABER model in Appendix Two.

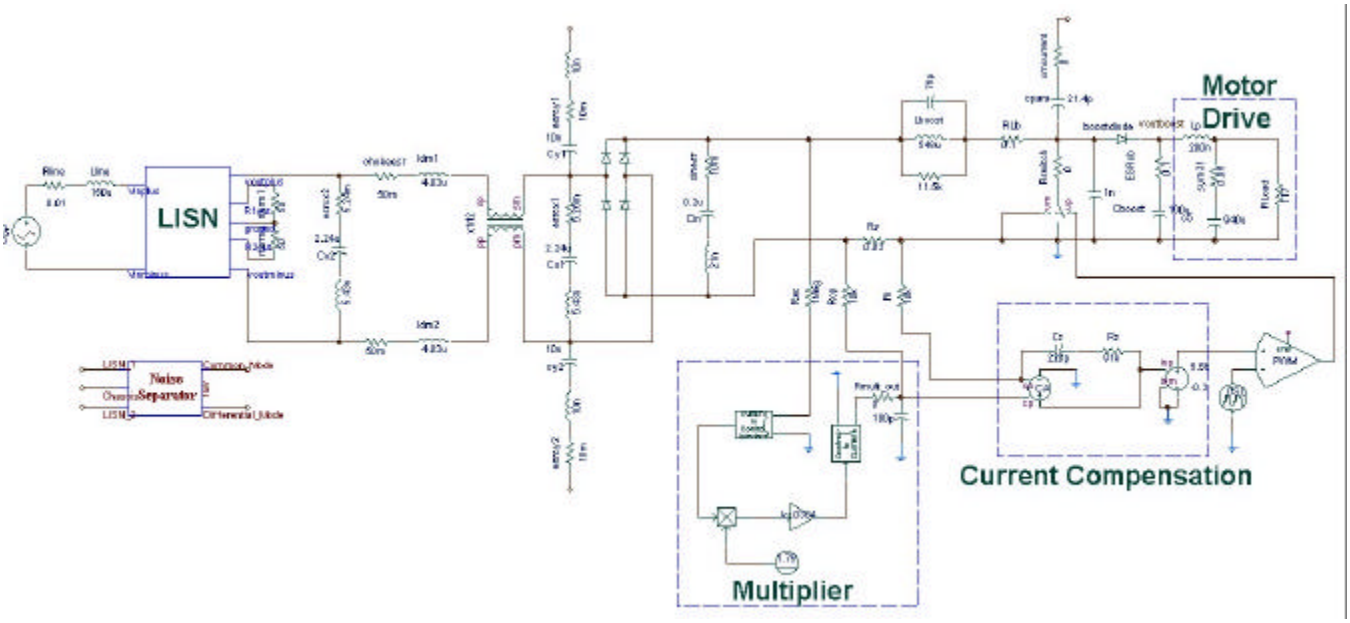


Fig. 3.13. SABER EMI Model

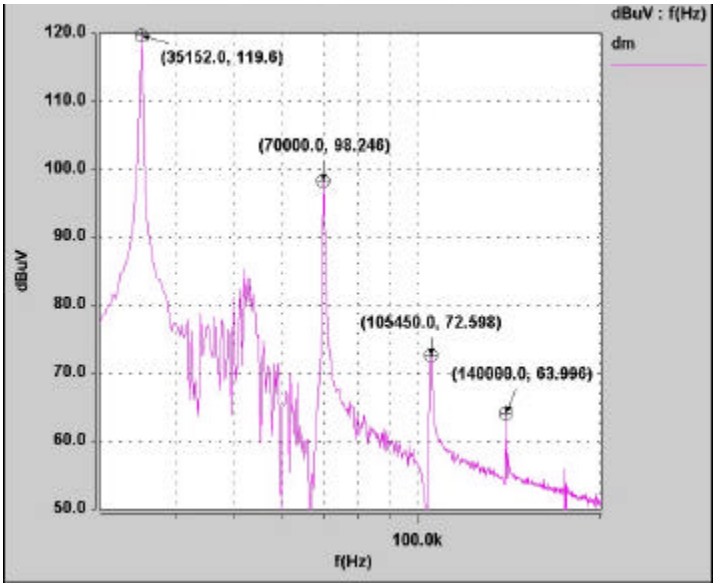


Fig. 3.14. Simulation Result for DM Noise

3.2.5 EMI Algebraic Model

The results displayed in Fig. 3.14 require around 30 minutes on a Pentium III 500 MHz processor to generate the transient data plus another 5 to 10 minutes for the FFT. Due to the

nature of genetic algorithms, hundreds of circuits must be analyzed in a single optimization run. Therefore using a SABER switching model to predict EMI would be computationally prohibitive. Fortunately, there has been recent work done to increase the speed of EMI predictions [30] [31] [32] [33]. The work done in [30] is especially interesting because it applies directly to EMI predictions for the boost PFC circuit and does not require any switching simulations.

The basic idea in [30] is to simplify the converter by replacing the switch/diode commutation cell with an equivalent voltage perturbation source. The rectifier diodes are always conducting and therefore do not contribute any switching disturbances. Therefore the only disturbance in the circuit is the drain to source voltage of the switch.

The high frequency model proposed in [30] is displayed in Fig. 3.15. Since the rectifier diodes are always conducting, simple voltage drops can replace them. The switch and diode are replaced with an equivalent voltage disturbance V_{Pert} that excites both common and differential mode noise via the corresponding propagation paths. Rise time, fall time and the diode reverse recovery current all contribute to the shape of the V_{Pert} waveform. Fig. 3.16 shows the general shape of V_{Pert}. The perturbation source can be modeled as a trapezoidal voltage source with high frequency ringing. However, further simplifications can be made.

To make the optimization runs even faster, the EMI level is only predicted up to the first harmonic limited by the specification. For the EN55011 Class B limit, the first limited harmonic is the first switching harmonic above 150 kHz. Therefore, the EMI prediction only needs to be accurate up to this frequency. Thus the additional complexity of adding ringing to V_{Pert} is not needed. The final waveform used is simply the trapezoidal waveform shown in Fig. 3.16 disregarding the high frequency ringing. Now the waveform in Fig. 3.16 can be represented by an addition of sinusoids, each at a multiple of the fundamental frequency. In the case of PFC, the waveform V_{Pert} is periodic with the line frequency (50 Hz). As a result, the switching harmonics must be exactly integer multiples of the line frequency. To predict the EMI levels at 150 kHz, network analysis can be carried out on the circuit. More detail on the application of the model in [30] to this particular application can be found in [13].

Since this topology is symmetric over a line cycle, the differential and common mode EMI levels can be easily identified since the odd harmonics correspond to differential mode noise and

the even harmonics to common mode noise. Therefore, the differential mode noise level at each switching frequency can be evaluated by calculating the square root of the quadratic sum of the odd harmonics of the line frequency around this frequency. The common mode noise level is computed in the same way but considering only the even harmonics. The square root of the quadratic sum of the differential and common mode levels is equal to the total noise

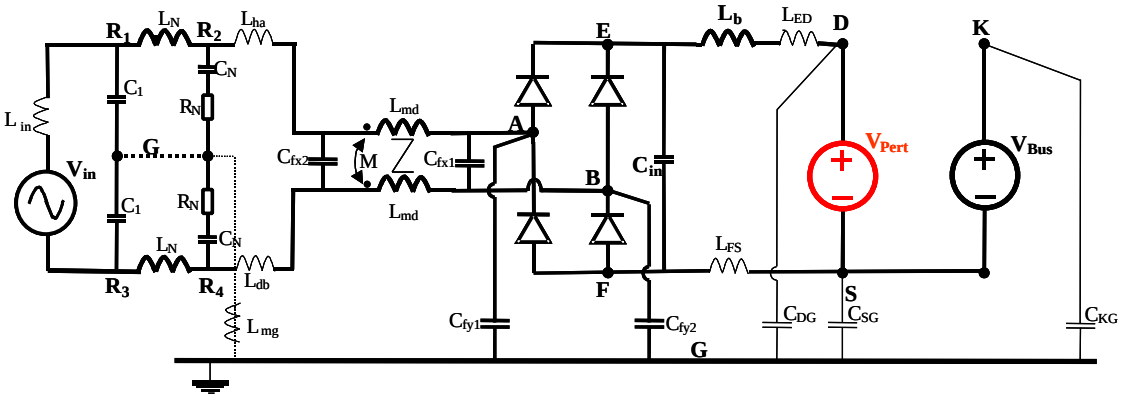


Fig. 3.15. High Frequency Boost PFC Circuit with Equivalent Voltage Perterbation

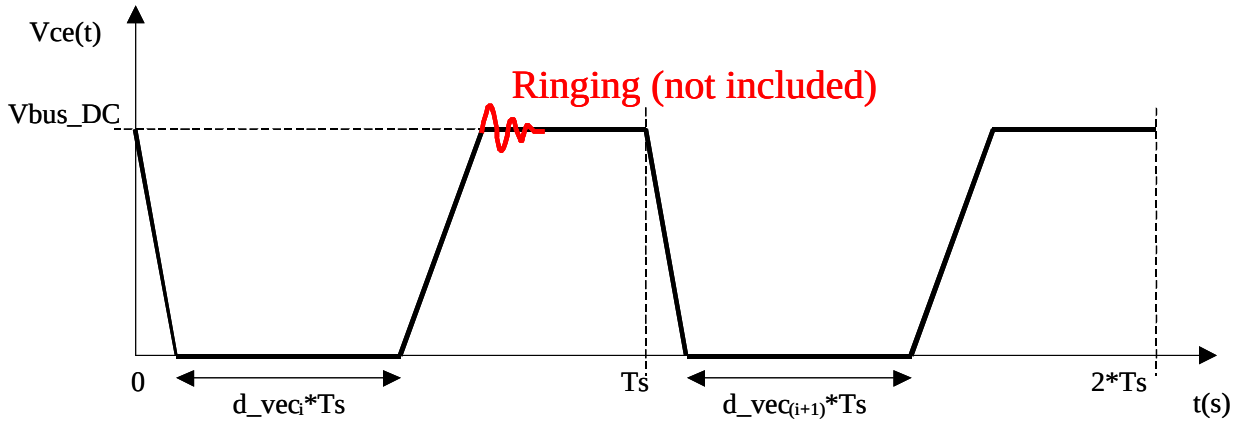


Fig. 3.16. V_{Pert} Waveform

3.3 Thermal Models

Just like EMI, many physical factors affect temperature rises in a circuit. The layout is certainly one of the most significant influences on the thermal behavior of the circuit. The presence of a cooling fan can greatly affect the temperature of semiconductor devices and magnetic components. Whether or not the circuit is in an enclosure has a large influence on the airflow through the circuit. The position of one component with respect to another is also a factor. For example, if the switch were very close to the fast diode then the radiated heat from the switch would most likely increase the temperature of the diode. For these reasons, the temperature rise calculation for devices and magnetic components is not a trivial task. Fortunately, for the boost PFC circuit there are only a few temperature rises that are interesting to compute. In this case, only the inductor, switch, fast diode, and rectifier bridge temperature rises are calculated.

All temperature models are simple steady-state algebraic equations. For the core, equations from the manufacturer's catalogue are used [36]. There have been studies that report successful modeling of the IGBT with switching simulations [37], [38], [39]. However the use of GA's requires a much less time intensive approach. Fortunately there have been experimentally verified algebraic approaches to modeling IGBT switching loss [40], [41]. The diode and rectifier bridge temperature rise equations are also algebraic. A detailed description of all temperature rise equations used in this design can be found in [13].

3.4 EMI and Thermal Model Validation

In modeling, there are always assumptions made to simplify the analysis. Also, models are only mathematical representations of physical phenomena. Therefore it is very important to verify that a model is able to predict the real circuit behavior in the range of interest. Hardware tests have been performed and the data has been used to verify the models described in this chapter. The results in this section are shown only to illustrate the accuracy or inaccuracy of the models. The hardware test set-up, measurement tools and operating conditions are described in detail in Chapter Four.

3.4.1 SABER EMI Prediction

Even without exact device models, the SABER EMI model is able to provide a reasonably accurate low frequency prediction. Fig. 3.17 and Fig. 3.18 show comparisons between the predicted DM and CM noise and the measurements. The DM prediction is within 5 dBμV of the measurement. The CM noise is fairly close except for the first harmonic at 35 kHz. The CM is slightly better in the high frequency (compare Fig. 3.19 and Fig. 3.21), however neither prediction is reliable above 500 kHz. These results show the necessity of accurate device models and that more work is needed to identify additional high frequency parasitics. As mentioned previously, the EMI simulations are very time intensive. Therefore even if the accuracy of the model were improved, it would still not be usable for the GA.

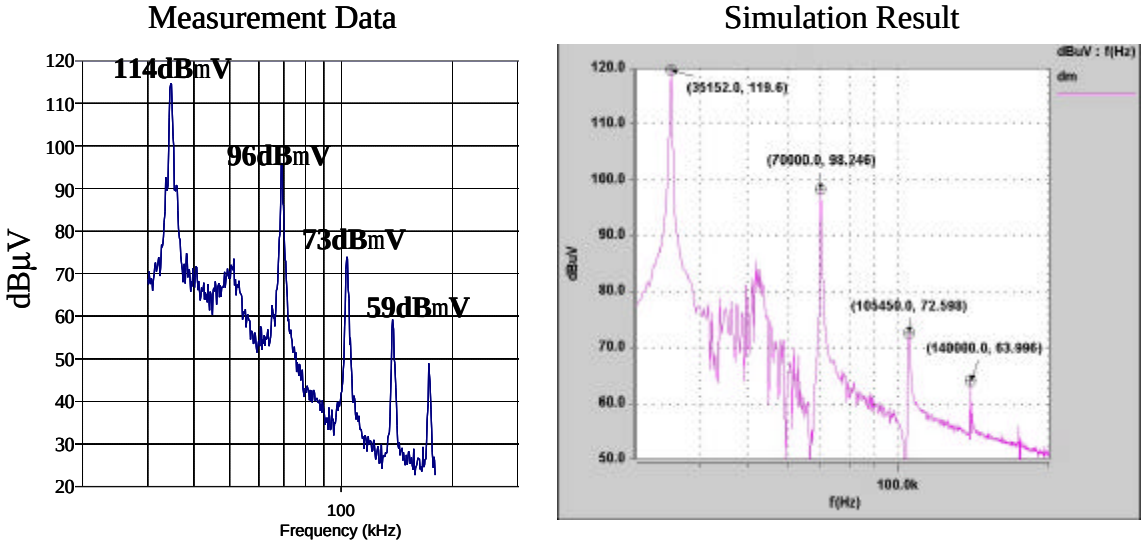


Fig. 3.17. DM Noise Measured and Predicted

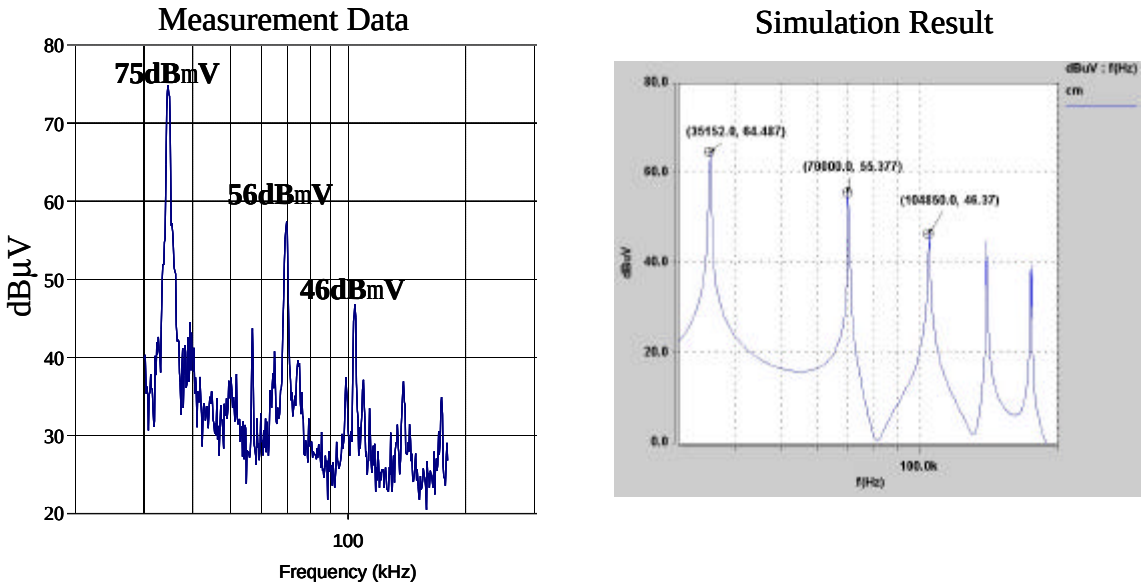


Fig. 3.18. CM Noise Measured and Predicted

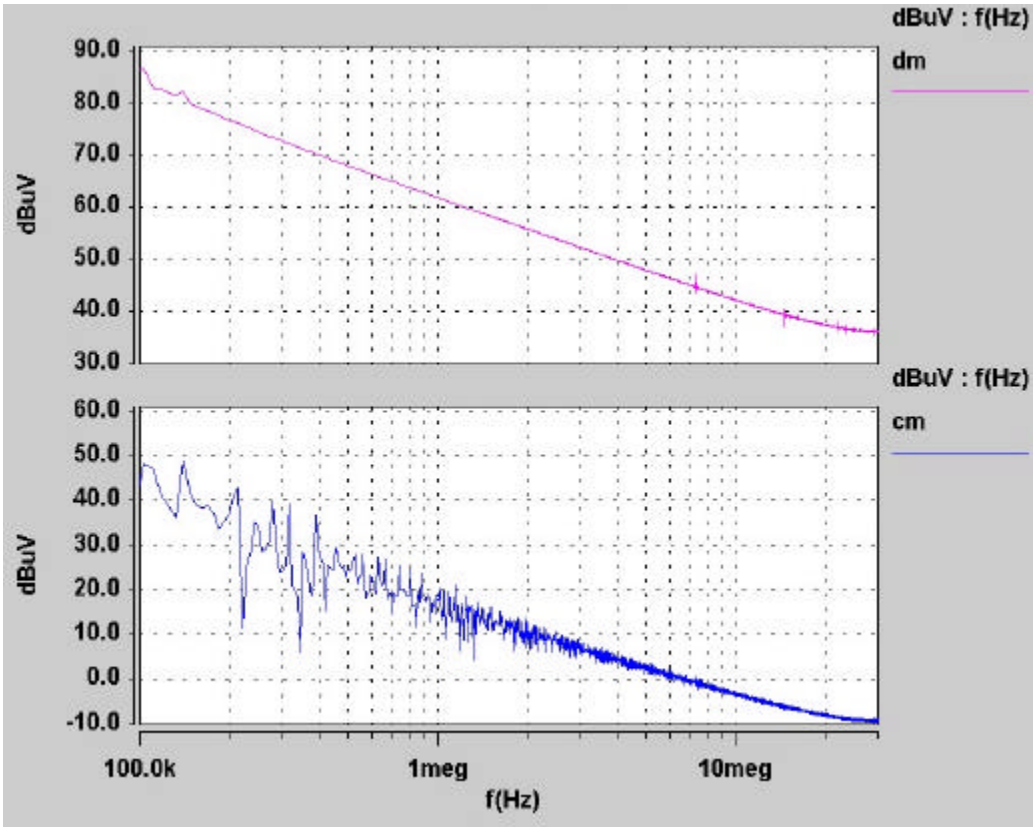


Fig. 3.19. CM and DM Noise High Frequency Predictions

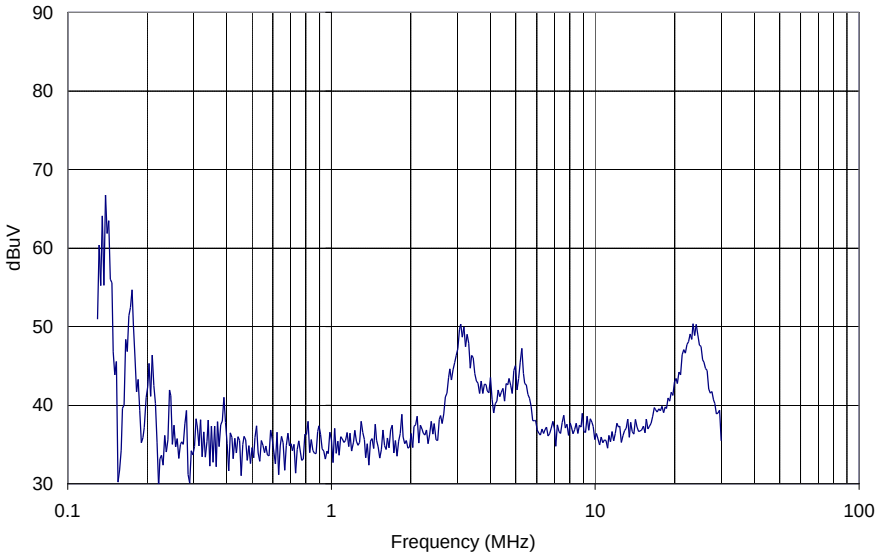


Fig. 3.20. DM Noise High Frequency Measurement

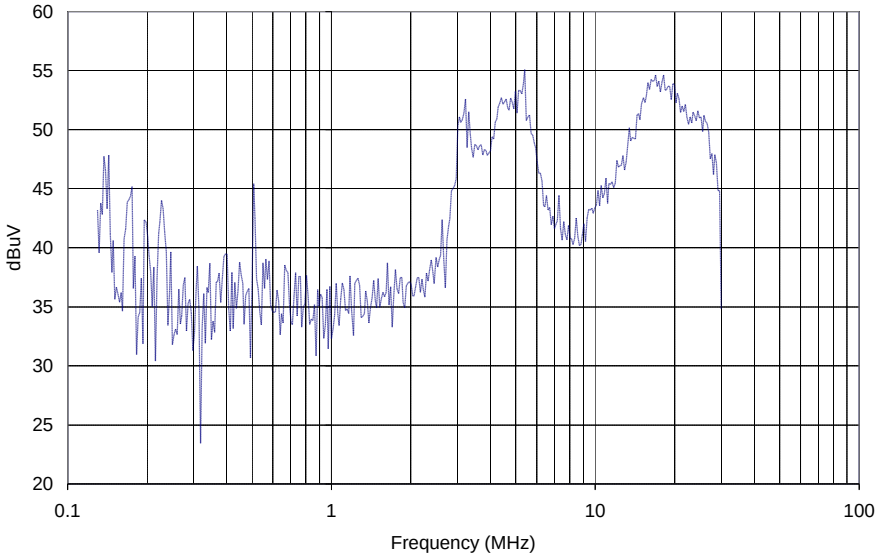


Fig. 3.21. CM Noise High Frequency Measurement

3.4.2 Algebraic EMI Prediction

DM, CM and total noise levels have been verified experimentally. Fig. 3.22, Fig. 3.23 and Fig. 3.24 show that the algebraic EMI model matches fairly well with the measurement results. The goal of the prediction tool has been to predict the level of the first harmonic to enter the EMI standard limit (the first harmonic after 150 kHz). Analyzing Fig. 3.22, Fig. 3.23 and Fig. 3.24 it can be seen that the prediction tool is able to satisfy this goal. These results line up with the SABER results. Both prediction tools are valid up to around 500 kHz and both models are based upon the same parasitics and an ideal switch and diode commutation cell.

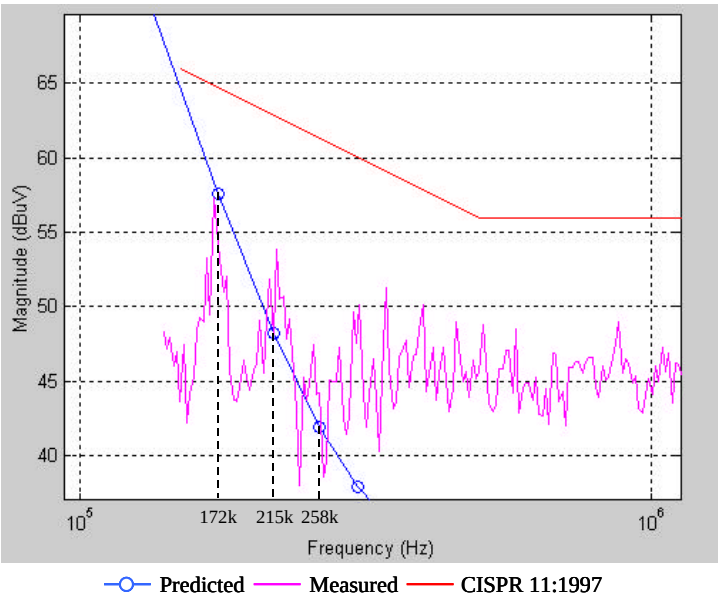


Fig. 3.22. Comparison Between Predicted and Measured Total Noise

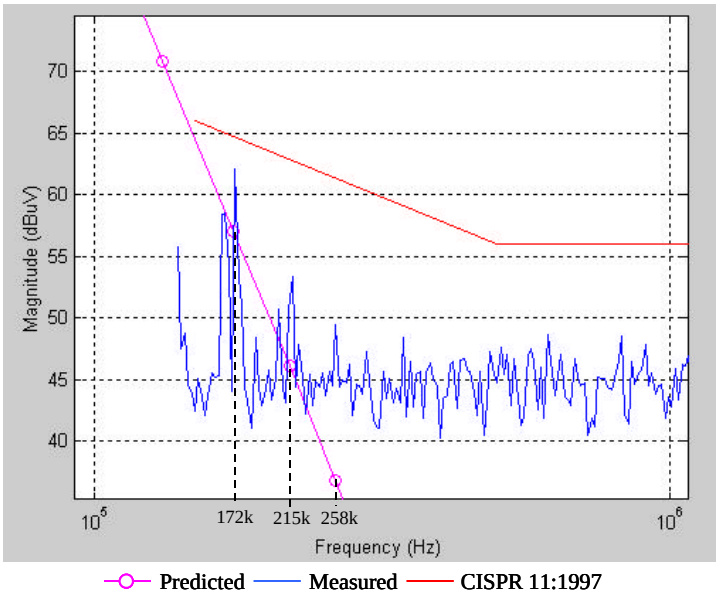


Fig. 3.23. Comparison Between Predicted and Measured DM Noise

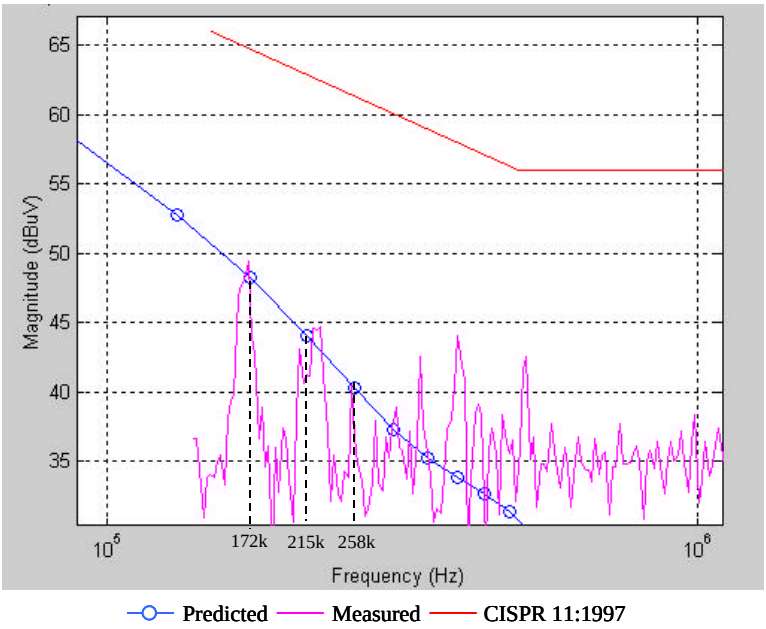


Fig. 3.24. Comparison Between Predicted and Measured CM Noise

3.4.3 Thermal Prediction

In order to account for radiated heat and forced air convection the temperature rise equations have been adjusted. For example the inductor core temperature is affected by the airflow from the fan. However it is not a straightforward relationship because the air over the inductor is actually heated by the switch and diode. Fig. 3.25 shows that the air over the inductor is not flowing in a straight path thus making an exact calculation even more complicated. A simple scaling factor is one way for the genetic algorithm to take all these effects into account. Expression (3.3) shows how the scaling factor X_{Tuning} is used to help predict the core temperature. In (3.3), T_{Core} is the core temperature, T_A is the ambient temperature, P_{Core} is the core loss in milliwatts, P_{Cu} is the copper loss in milliwatts and A_S is the core surface area in square centimeters [36]. For the semiconductor devices the thermal resistance of the heat sinks have been adjusted to match with experimental results. The conditions for the thermal tuning test are listed in Table 3.4. In Fig. 3.26, it can be seen that after the thermal scaling factors have been adjusted, the measured results fit well within the minimum and maximum predictions. Tolerances are taken into account in all temperature rise equations. The minimum and maximum temperature predictions shown in Fig. 3.26 correspond to the best case and worst-case variations due to the tolerance. The results in Fig. 3.26 only verify that the thermal prediction is accurate for one set of conditions. Additional testing has been done to verify the accuracy of the thermal predictions for many different operating conditions while keeping X_{Tuning} constant. Depending on the layouts used the value of X_{Tuning} ranged from 1.2 to 1.4.

The number of inductor turns was reduced from 98 to 75 and the same thermal measurements were made as in the tuning test. Fig. 3.27 shows that the prediction is still accurate for a reduced number of turns. The switching frequency was also varied from 35 kHz to 55 kHz. Fig. 3.28 shows that the prediction tool still was accurate. Finally, the output power was reduced from 1150 W to 740 W. Fig. 3.29 shows that the tool made good predictions in this case. Overall these results confirm that the thermal predictions have a satisfactory degree of precision.

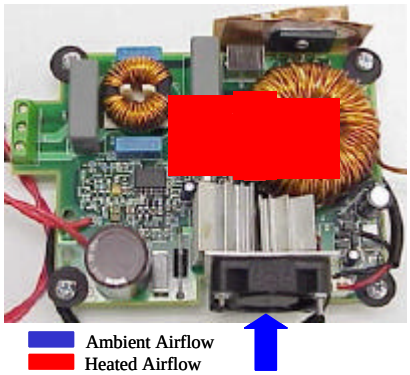


Fig. 3.25. Airflow within the Converter

$$T_{Core} = T_A + X_{Tuning} \cdot \left[\frac{P_{Core} + P_{Cu}}{A_S} \right]^{0.83} \quad (^{o}C) \tag{3.3}$$

Table 3.4. Thermal Testing Conditions for Fig. 3.26

Condition	**Value**
Ambient Temperature	23 ^{o}C
Input Voltage	180 Vac
Line Frequency	50 Hz
Output Voltage	368 V
Output Power	1154 W
Switching Frequency	35 kHz
Number of Turns	98

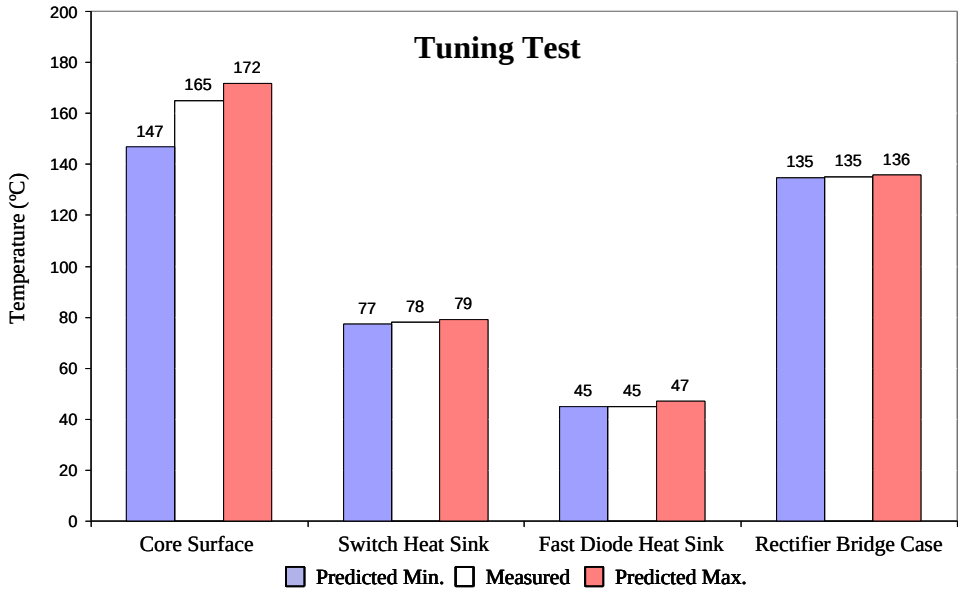


Fig. 3.26. Comparison Between Predicted and Measured Temperatures

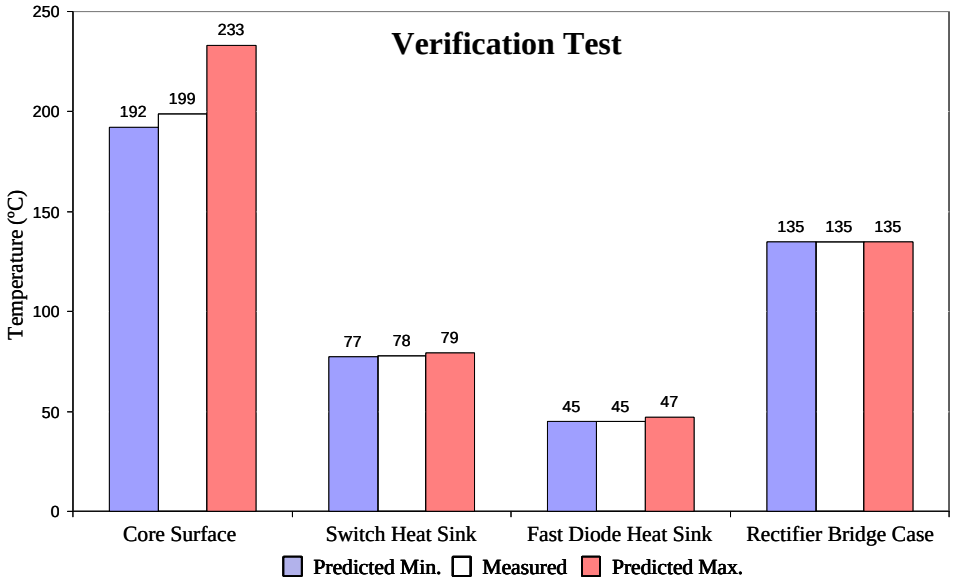


Fig. 3.27. Verification of Predictions with 75 Turns on the Boost Inductor

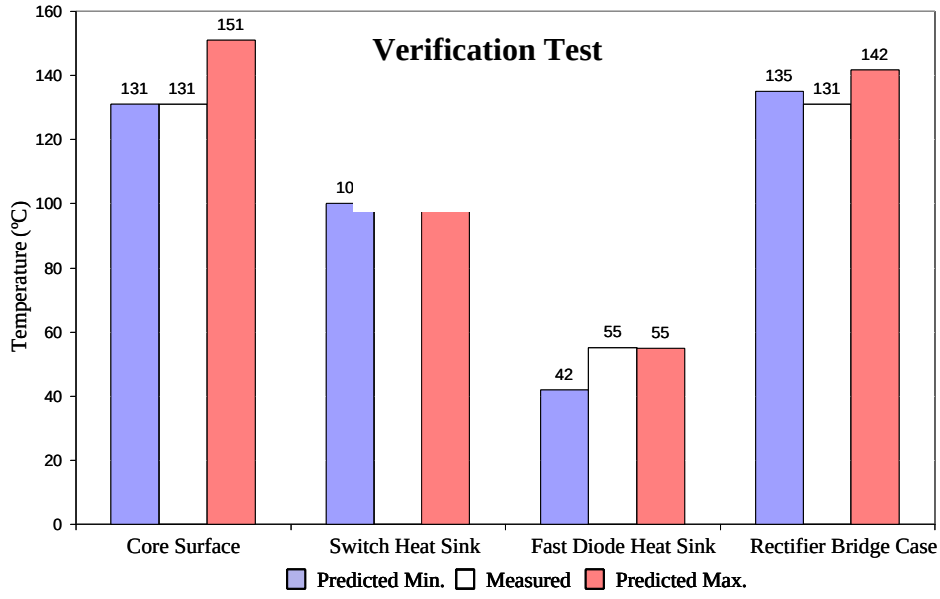


Fig. 3.28. Verification of Predictions with a Switching Frequency of 55kHz

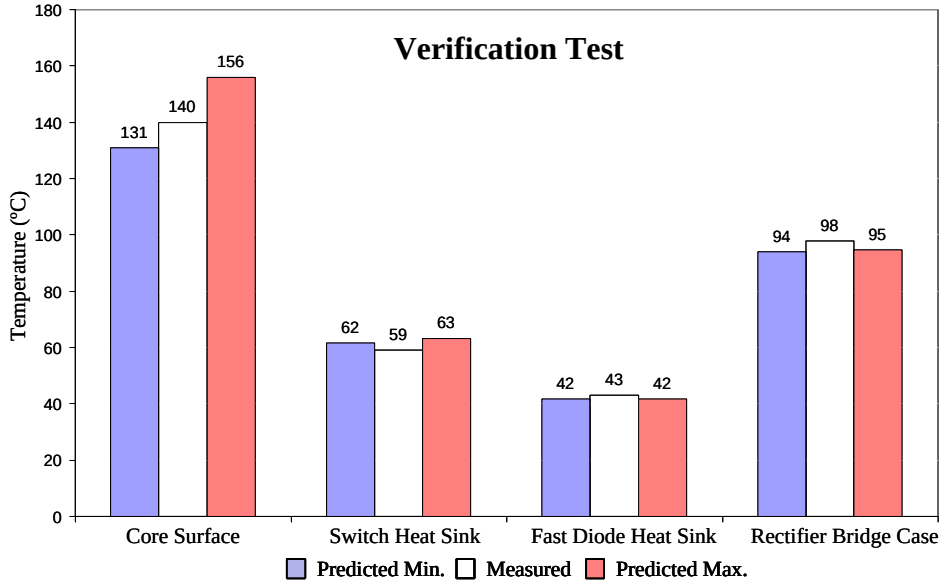


Fig. 3.29. Verification of Predictions with at 740W Output Power

3.5 Summary

Electrical models have been developed that can be used to predict steady-state and transient behaviors of the converter. These models also can evaluate any final design produced by the GA before the design is implemented in the hardware.

The important parameters of the boost PFC high frequency model in Fig. 3.4 have been identified and measured. Switching and algebraic EMI prediction tools have been developed and verified. To extend the EMI prediction tool to a higher frequency range, more parasitic values would have to be determined and the high frequency ringing induced by the switch and diode commutation should be included.

General algebraic temperature rise equations are presented in [13]. Since all these equations are algebraic, a GA can easily use them. A tuning procedure has been applied to these equations to account for higher order thermal effects. The accuracy of this approach has been experimentally verified. To extend the thermal predictions to automatically include radiated heat and the effect of a cooling fan, much more complicated models would have to be developed.

4 Thermal and EMI Testing and Analysis

4.1 Thermal Measurements

Thermal performance affects many aspects of an electronic circuit's behavior. The transistor operating temperature influences the delay, rise and fall times, and the turn on and off energy. The temperature of a diode affects the amount of reverse recovery current and the forward voltage. The switch rise and fall time and the reverse recovery also affect the EMI levels. In addition, the core temperature of inductors dictates the lifetime of the core. Because all of these effects are very important in the performance of power supplies, it is important to predict and measure them with as much accuracy as possible. Also, measurement data can highlight important tradeoffs that designers might use to optimize their circuits. The following sections describe the measurement procedures and test set-up. Some results are presented and the accuracy of the measurements is discussed.

4.1.1 Measurement Set-up

The most important measurement guideline is consistency. Using the same procedure, operating conditions and equipment throughout the testing is very important. This is especially important if the goal is to verify mathematical predictions with experimental results. Also a sound measurement procedure can be very helpful when the measuring equipment is less than state-of-the-art. After all, the goal is to measure temperature rise not an absolute value. Time is also a very important factor when measuring temperatures. Most electric circuits reach steady state in a few microseconds; however reaching thermal steady state requires significantly more patience.

K-type thermocouples are used to record temperatures. The thermocouples are placed inside the semiconductor heat sinks (see Fig. 4.1) and on the surface of the boost inductor core. Thermocouples are used to measure the most interesting parameters: the heat sinks on the semiconductors and the core surface temperature. The infer-red (IR) gun is used to measure other parts of the circuit. The IR gun is less accurate but the number of thermocouples is limited. The placement of the fan is also very important. In this case, the fan is used only to cool the switch and the fast diode. The distance and orientation of the fan to these devices can

significantly affect the temperature rise. Therefore the fan must be kept in exactly the same position for all tests. The thermocouples are imbedded in the heat sinks. Small holes have been drilled in the heat sinks and the end of the thermocouples has been placed in the holes, see Fig. 4.1. Some thermal grease is used to help the thermocouple stay in place and to facilitate the heat transfer from the heat sink to the thermocouple. Also, the windings on the boost core have been wound around the thermocouple. Fig. 4.2 shows the configuration for thermal testing. The circuit is tested at an input mains voltage of 180 Vac and a constant current load of 3.3 A The lower input voltage has been selected to obtain the worst-case thermal operating point.

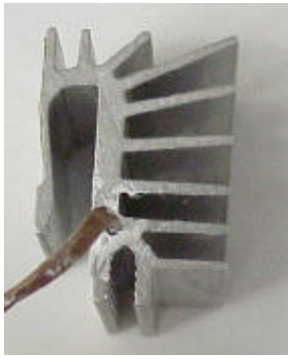


Fig. 4.1. Thermocouple and Heat Sink

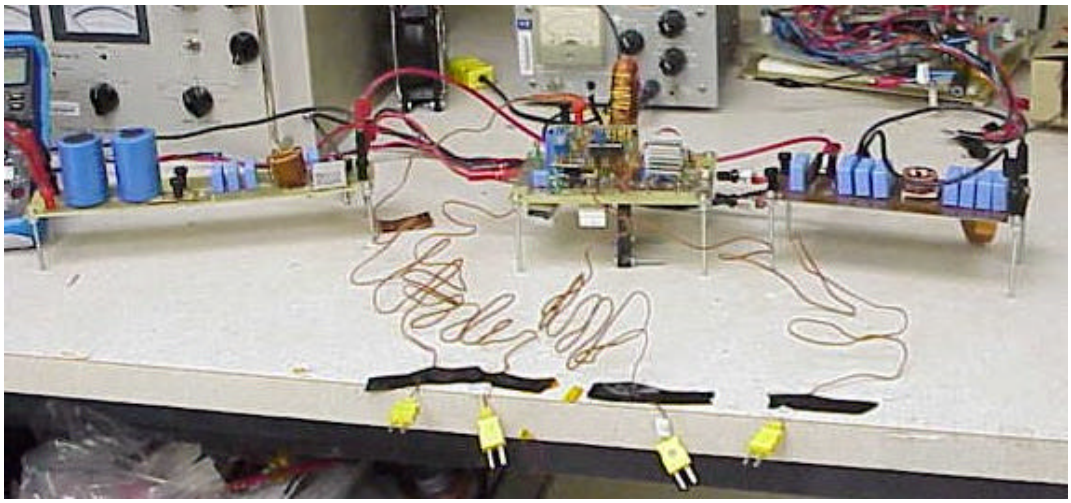


Fig. 4.2. Thermal Testing Configuration

Table 4.1 lists the components/parameters of the 35 kHz prototype. These are constant throughout the testing process unless otherwise noted.

Table 4.1. 35 kHz Prototype

Component	Reference/Value
Switch	Intersil: HGTP7N60A4
Anti-parallel diode	Phillips: BYM36C
Fast diode	Motorola: MUR1560
Bridge Rectifier	Diode Inc.: GBJ806B
Boost Inductor	Micrometals: T225-26, 98 Turns of 16 AWG L=832μH, C=76pF, R=11.5kΩ, L_{SAT}=548μH
Common mode choke	SDI142-21: Lcm=1.65 mH, Ldm=4.03 μH
Cx(2)	2.24 μF
Cy(2)	10 nF
C_{in}	0.2 μF
Boost capacitor	100 μF + 2*470 μF
Switch heat sink	Thermalloy: ML516F
Fast diode heat sink	Thermalloy: ML516F
Rectifier heat sink	Thermalloy: ML516G
Fan	Power-on: MO N5010B-8
Switching Frequency	35 kHz
Gate Resistance	20 Ω
Control Law	Average Current Mode
Control IC	SGS Thompson: L4981A

4.1.2 Methodology

Taking just one set of thermal data at one operating point only shows that the converter can work with one set of parameter values. Also, this only provides one data point for verifying the mathematical model. However, the goal here is to observe trends in the thermal behavior; therefore, several parameters are varied. Of course, most of these trends are intuitive, however by observing thermal trends of all the circuit components some important tradeoffs are brought to light. In addition, the sensitivity of the thermal behavior changes for different parameter ranges. If a parameter is varied over a wide enough range, then the thermal sensitivity can be evaluated. A full table of all thermal testing is located in Appendix Four. The following results are the more interesting ones.

4.1.2.1 Switching Frequency

Switching frequency has a large impact on the converter design and performance. Results from the GA indicated that a low switching frequency would yield the best design (35 kHz for the design in Table 4.1). However, thermal testing has been performed at many different switching frequencies. This allows the thermal behavior of the circuit to be more fully explored.

Fig. 4.3 displays thermal data for the core surface, switch and fast diode heat sinks, and the anti-parallel diode's case. The winding temperature rise is not shown because in this case it varies proportionally to the core surface temperature. Also it was observed that the core temperature is always greater than the winding temperature.

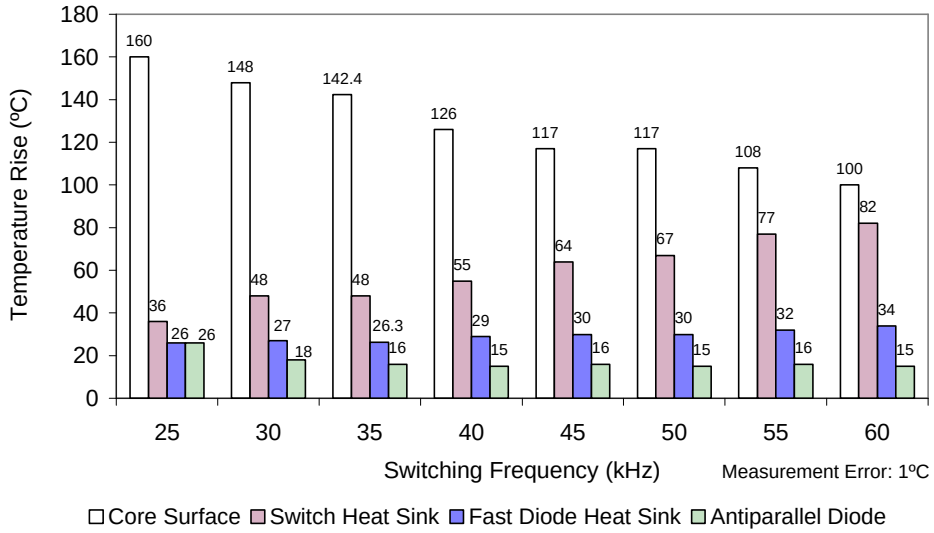


Fig. 4.3. Temperature Rise vs. Frequency

The temperature rise data in Fig. 4.3 has been measured at the following operating conditions: an input voltage of 180 Vac, a line frequency of 50 Hz, an output power of 1150 W, and an output voltage of 368 V. Any difference in ambient temperature between measurements has been taken into account. In general the ambient temperature was 23 ºC. The values/components in Table 4.1 are used except that the switching frequency is varied.

Fig. 4.3 shows that the fast diode temperature tends to rise as switching frequency increases while the anti-parallel diode temperature tends to fall. The fast diode temperature rise is due to the fact that the amount of reverse recovery losses increases as the switching speed increases. The most important tradeoff observed in Fig. 4.3 is between the core temperature and the switch temperature. The switching losses in the IGBT are a significant part of the overall losses [42]. This explains why the IGBT tends to heat up significantly as the frequency increases. The core temperature rise decreases as the switching frequency increases because both the core and copper losses decrease. The expression for core loss can also be expressed as

$$P_{Core} = K \cdot \Delta B^{\alpha} \cdot F_S^{\beta}. \qquad (W) \tag{4.1}$$

Where K is a constant that depends upon the material and volume of the core, B is flux density and F_S is switching frequency. The parameters α and β are empirical values that depend upon the core material. ΔB is inversely proportional to switching frequency. If β were less than α, then the core losses would increase as the switching frequency is decreased. In general this is the case [36].

4.1.2.2 Current Ripple

Current ripple results from the charging and discharging of the boost inductor. As discussed in Chapter Three, the core saturation effect significantly influences the current ripple. For the purpose of studying the effect of current ripple, the ripple measurement is always taken at the point where the ripple is the highest. For circuit described in Table 4.1, this point is almost always at the peak of the line voltage, see Fig. 4.4. All current ripple values are peak to peak.

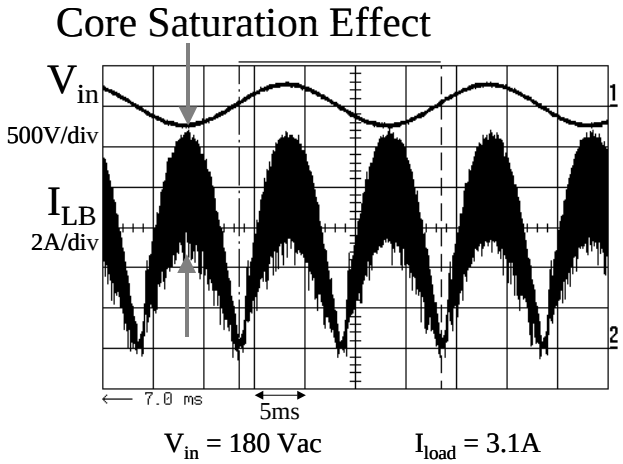


Fig. 4.4. Effect of Core Saturation

Fig. 4.5 displays thermal data for the core surface, switch, fast diode, and rectifier bridge heat sinks, and winding of the input choke. These parameters are the most sensitive to changes in the current ripple. The other temperature rises in the circuit do not vary significantly.

The temperature rise data in Fig. 4.5 have been measured at the following operating conditions: input voltage of 180 Vac, line frequency of 50 Hz, output power of 1150 W, output

voltage of 368 V. The values in Table 4.1 are used except that the number of turns on the core is varied. For the 4.7 A case, the number of turns is 90. For 5.83 A, the number of turns is 75.

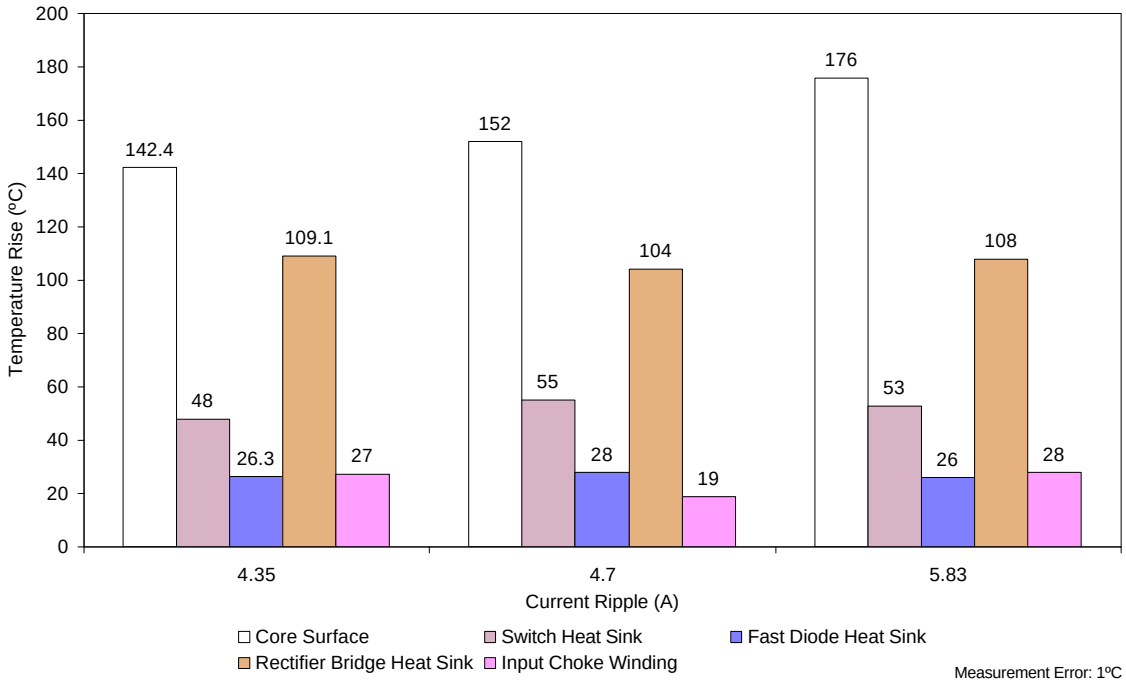


Fig. 4.5. Temperature vs. Current Ripple (varying the number of turns)

Fig. 4.5 shows that as the current ripple rises (the number of turns on the core is reduced) the temperature rise increases. This occurs because the AC flux is increasing with the reduction in the number of turns. The losses in the core can be expressed as

$$P_{Core} = Vol \cdot F_S \cdot \oint H dB \qquad (W) \tag{4.2}$$

where *Vol* is the volume of the core, F_S is switching frequency and the integral represents the area of the dynamic hysteresis loop. The expression (4.2) is a more general case of (4.1). Usually (4.1) is empirically derived for the case when the current is slowly varying thus the hysteresis loop is traversed slowly. When the inductance is lowered (i.e. the current ripple is increased), the increased current speed induces more eddy currents in the core. This produces increased losses that have the effect of broadening the hysteresis loop [43]. The expression in (4.1) does not account for this; however, (4.2) can be used for any general case. Additionally, a higher current ripple implies higher copper losses. Since the windings are in direct contact with the core surface, the copper losses also contribute to the core temperature rise.

The general relationships for core and copper losses are shown in (4.3) and (4.4). In this case, F_S is the switching frequency, ΔB is the change in flux density, and ΔI is the current ripple. From these relationships it can be seen that for a fixed F_S the core and copper losses are proportional to ΔB and ΔI respectively. Fig. 4.5 shows that varying the number of turns n increases the core temperature. However there are other core parameters that influence the losses. Expression (4.5) shows that the change in flux density is also dependent on V the voltage applied to the winding, d the duty cycle, F_S, and A_C the core cross-sectional area. If all other parameters were fixed, then an increase in A_C would decrease ΔB thus reducing the core losses. The current ripple, ΔI, given in (4.6) is equal to the magnetic path length l_m multiplied by the change in magnetic field intensity ΔH divided by the number of turns n. Since ΔI is directly proportional to l_m, increasing l_m would increase ΔI thus increasing the copper losses P_{Cu},. The losses in the core would be unaffected by a change in l_m because this does not affect F_S or ΔB. In (4.7) the relationship between flux density B and magnetic field intensity H is given where μ is permeability. From (4.5), (4.6), and (4.7) it is apparent that ΔI is very sensitive to a decrease in turns n. With fewer turns, ΔB increases thus increasing ΔH and making the numerator of (4.6) larger. At the same time, the denominator of (4.7) grows smaller because n is smaller. For the case of the toroidal core it is not possible to change l_m and A_C therefore the number of turns is the only parameter varied.

$$P_{Core} \propto F_S, \Delta B \tag{4.3}$$

$$P_{Cu} \propto \Delta I \tag{4.4}$$

$$\Delta B = \frac{V \cdot d}{F_S \cdot n \cdot A_C} \qquad \left(\frac{Wb}{m^2}\right) \tag{4.5}$$

$$\Delta I = \frac{l_m \cdot \Delta H}{n} \qquad (A) \tag{4.6}$$

$$B = \mu \cdot H \qquad \left(\frac{Wb}{m^2}\right) \tag{4.7}$$

The relationship between the switch and fast diode temperature rise and the current ripple is not as obvious. Fig. 4.6 shows that the highest switch and diode temperatures occur when the current ripple is 4.70 A. As the current ripple increases, the rms value of the current increases, causing a small increase in the conduction losses of both the IGBT and the diode. However, the

switching losses also vary. Due to the current tail of the IGBT a significant portion of the switching loss is generated during turn-off [42]. Since the current tail is proportional to the turn-off current, a high current ripple would likely produce increased switching losses. However, the reverse recovery of the diode is better at a high current ripple. A high ripple value means that less current would be flowing through the diode when the switch turns on, thus reducing the maximum reverse recovery current. Part of the reverse recovery losses occur in the diode and part of them occur in the switch. It is not easy to discern how they divide between both devices. The existence of these trade-offs makes difficult to predict the optimum value of the current ripple that minimizes the temperature rise in the switch and diode.

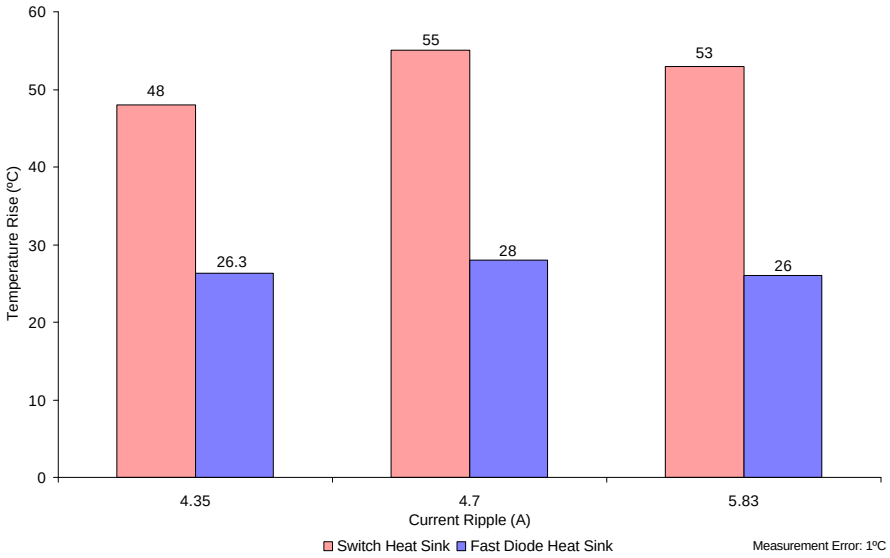


Fig. 4.6. Switch and Diode temperature rise vs. Current Ripple

4.1.2.3 Gate Resistance

Switching losses can significantly affect the temperature of the switch and diode. Therefore, it is important to select the correct gate resistance to turn an IGBT on and off. For these tests, the gate on-voltage is held constant at 14V. Fig. 4.7 shows thermal measurements for various values of R_g (gate resistance). The data seems to indicate that there is an optimum point between an R_g of 10 Ω and 33 Ω. Fig. 4.8, Fig. 4.9, Fig. 4.10 and Fig. 4.11 can be used explain the switching behavior and the loss mechanisms. The waveforms are measured using the design listed in Table 4.1.

The switching loss can be divided into two mechanisms: overlap and overshoot. For a low gate resistance, the dv/dt and di/dt of the switching voltages and currents are increased. As a result, the voltage overshoot during turn-off is increased and the reverse recovery is increased during turn-on. Also, the reverse recovery current adds to the switch current thus causing more losses in the switch. For higher gate resistances, the dv/dt and di/dt of the switching currents and voltages are reduced, but the overlap time is increased. Comparing the overlap losses in the waveforms shows that the switch overlap losses are worse than the diode's. The switch overlap occurs during high current and voltage transitions for both turn-on and turn-off. The diode overlap only occurs during high voltage and current transitions for turn-off, see Fig. 4.11. The decrease in temperature going from 10 Ω to 20 Ω occurs because at 10 Ω the overshoot and reverse recovery losses are dominant. The increase in temperature going from 20 Ω to 33 Ω is due to the fact that the overlap losses increase. From 33 Ω to 75 Ω, the switch temperature continues to rise while the diode temperature is almost constant. This occurs because the reverse recovery has been significantly reduced and the diode is no longer significantly affected by the overlap losses.

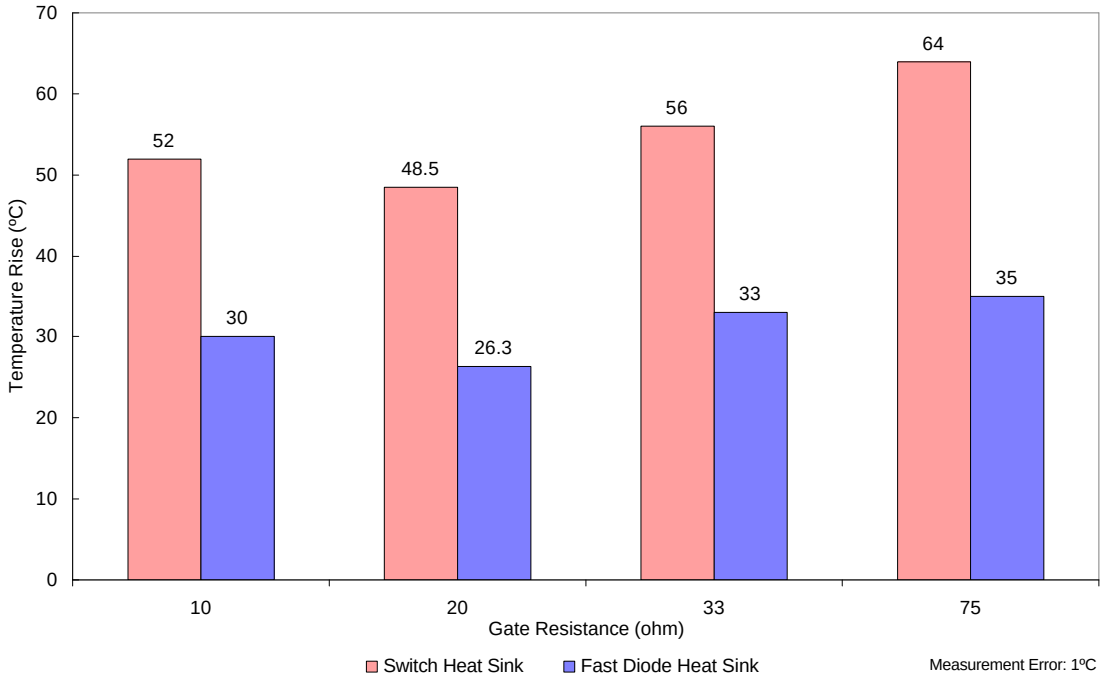


Fig. 4.7. Temperature Rise vs. Gate Resistance

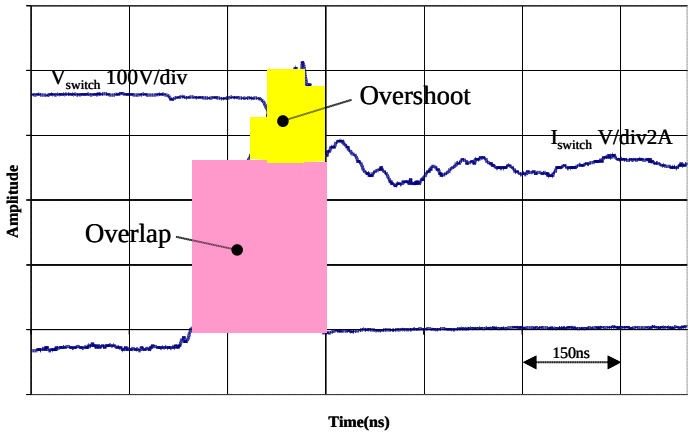


Fig. 4.8. Switch Turn-on: Switch Waveforms

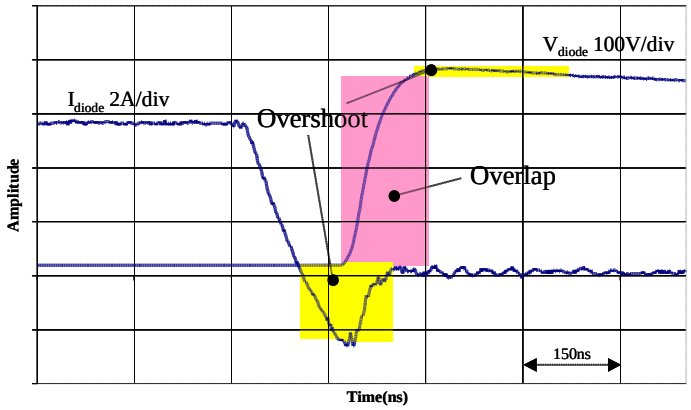


Fig. 4.9. Switch Turn-on: Diode Waveforms

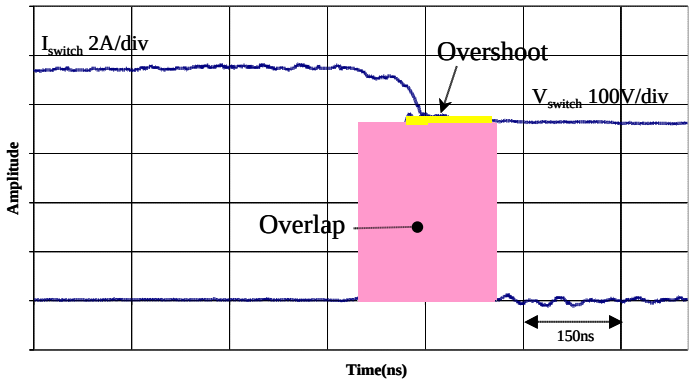


Fig. 4.10. Switch Turn-off: Switch Waveforms

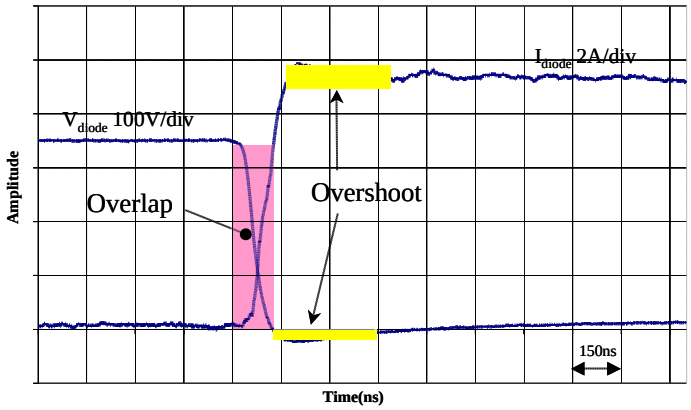


Fig. 4.11. Switch Turn-off: Diode Waveforms

4.2 EMI Measurements

By studying the trends in EMI noise levels, certain tradeoffs can be observed. These tradeoffs can aid not only in understanding the mechanism of EMI but also in the circuit design itself.

4.2.1 Measurement Set-up

Consistency is the most important factor in the EMI measurement set-up. Each time the circuit is tested the orientation of the Equipment Under Test (EUT) and the measuring devices must be the same. Careful attention must be given to the settings on the Spectrum Analyzer. These settings can greatly affect the magnitude of the measured noise. The EMI chamber is used to provide a good ground plane and attenuates any radiated noise from outside sources. Table 4.2 lists the measurement equipment used for the testing and Fig. 4.12 shows a typical test set-up. Unless otherwise noted the circuit parameters in Table 4.1 are used in the EMI measurements. The circuit is tested at an input mains voltage of 230 Vac and a constant current load of 3.3 A. The attenuation on the Spectrum Analyzer is set to 30 dB, the Resolution Bandwidth is 10 kHz, and the video bandwidth is set equal to the resolution bandwidth.

Table 4.2. EMI Measurement Equipment

Device	Manufacturer	Model
Spectrum Analyzer	Hewlett Packard	4195 A
LISN	Solar Electronics Company	8028-50-TS-24-BNC
Common Mode Rejection Network	EMC Services	CMRN-1
Differential Mode Rejection Network	EMC Services	DMRN-1
Network Analyzer	Hewlett Packard	4194 A

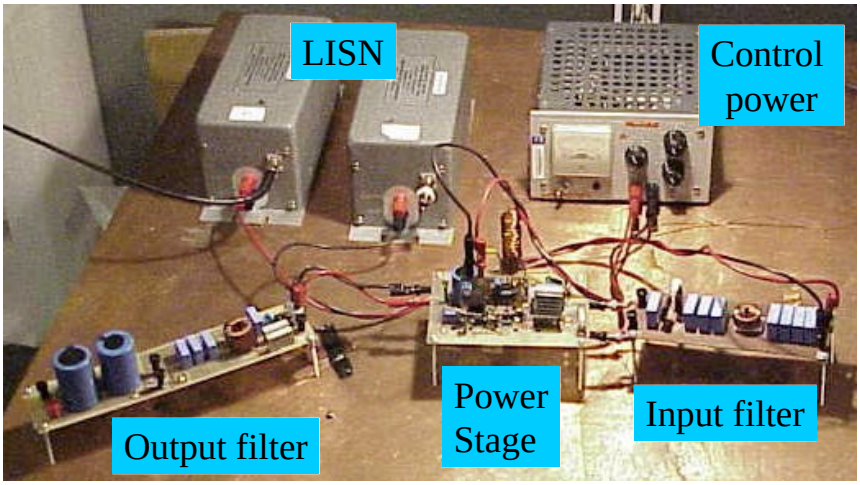


Fig. 4.12. EMI Measurement Set-up

4.2.2 Accuracy of Measurements

As mentioned above, the settings on the spectrum analyzer are very important. Ideally, use of consistent settings should yield consistent results. However, for PFC converters there is an additional complication. It is impossible to synchronize the oscillator in the spectrum analyzer with the line period. In other words, the output of the spectrum analyzer does not include the same portion of the line cycle every time. This causes the measurements to vary from one sweep to another. Fig. 4.13 and Fig. 4.14 show examples of this phenomenon. The data in Fig. 4.13 and Fig. 4.14 has been recorded under the exact same operating condition. In fact, the sweeps (manual trigger) have been taken one right after the other. For this reason, it is recommended that each measurement should include several sweeps of the frequency spectrum. The magnitudes generated by these sweeps could then be averaged to produce an “average” EMI

spectrum. This ensures that EMI predictions and analysis are not based upon extraneous noise spikes.

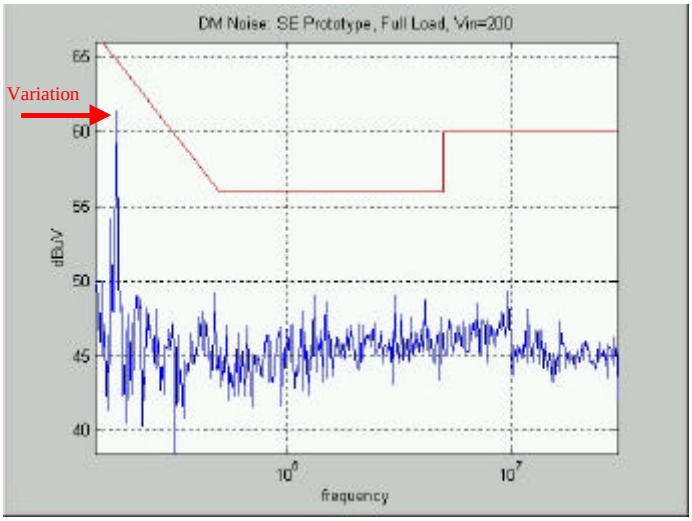


Fig. 4.13. Amplitude Variation

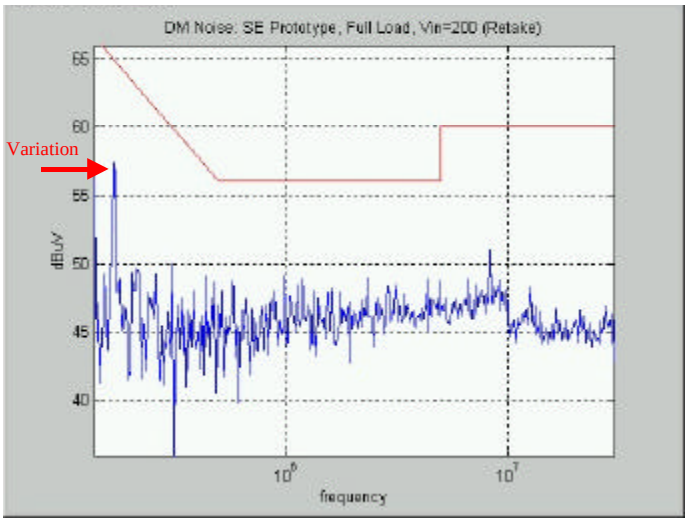


Fig. 4.14. Amplitude Variation

4.2.3 Methodology

Many factors contribute to the total noise disturbance. In the Chapter Three, important parasitic impedances are identified and measured. In this section, certain circuit parameters are varied and the impact on the noise spectrum is analyzed. This experimental approach enables certain trends in the EMI behavior of the circuit to be identified. Of course, some of these trends are intuitive, however some important tradeoffs are brought to light. In addition, due to component tolerances the parameters in the power stage vary from one converter to the next. If it is known that a certain variation is especially detrimental to the converter performance, then the component tolerance could be considered to ensure that any variation would not cause an increase in the noise level.

4.2.3.1 Gate Resistance

Section 4.1.2.3 describes how the gate resistance value affects the losses in the switch and diode. It is also very important to consider the effect of the gate resistance on the EMI levels. As mentioned before, a low gate resistance increases the dv/dt and di/dt of the switching voltages and currents. As a result, the voltage overshoot during turn off is increased and the reverse recovery current is increased during turn-on. This voltage overshoot and the reverse recovery current produce ringing in the circuit. This high frequency ringing is the primary excitation for high frequency EMI. Fig. 4.15 shows several envelopes for total EMI noise levels for varying values of R_g. Clearly there is a large reduction in the noise levels as R_g increases.

Experimental results show that almost all of the noise above 1 MHz is CM (see Fig. 4.16). The primary contribution to the high frequency CM noise is the dv/dt of the switch and the collector to ground parasitic capacitance [34]. Therefore it is logical that reducing the dv/dt could impact significantly the high frequency noise levels.

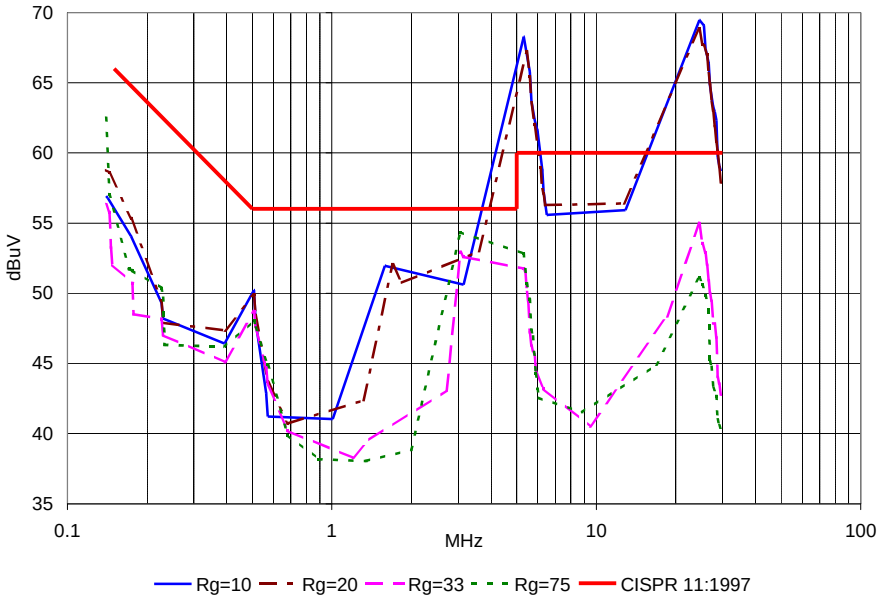


Fig. 4.15. Total Noise Envelope vs. Gate Resistance

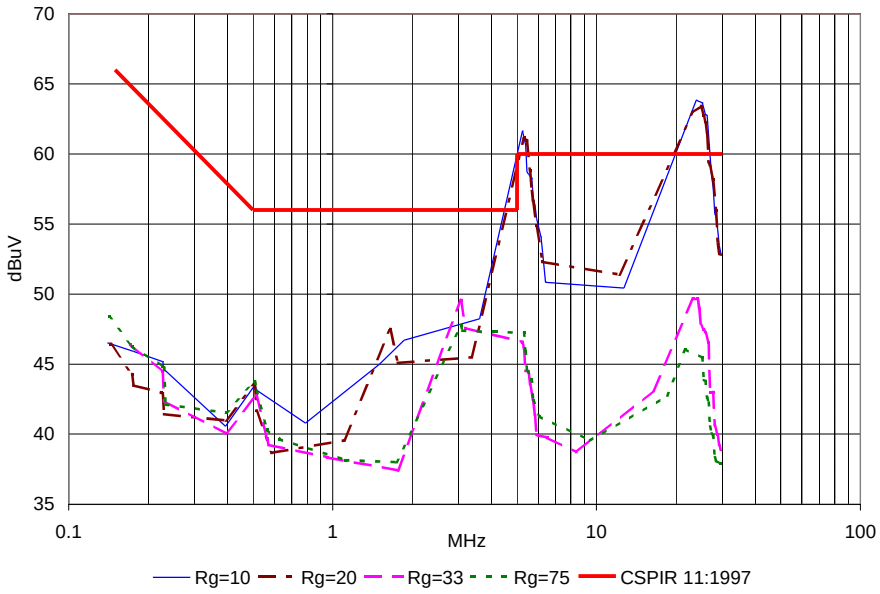


Fig. 4.16. CM Noise Envelope vs. Gate Resistance

4.2.3.2 Current Ripple

The current ripple is a direct result of the boost inductance. The smaller the boost inductance, the larger the current ripple. As discussed in Section 4.2.3, a lower boost inductance causes more EMI. However, the current ripple also affects the reverse recovery of the diode (see

Section 4.1.2.2). The ringing due to reverse recovery is a major source of high frequency EMI [44]. Therefore the tradeoff is not straightforward. Ripple values of 4.35, 4.70 and 5.83 A have been tested with the T225-26 core. The different ripple values are achieved by reducing the number of turns on the core. Note also that the ripple values are the maximum ripple over the line-cycle. Fig. 4.17 displays the total noise envelopes for varying current ripples. As discussed in Section 4.1.2.2, changing the core area, A_C, and the magnetic path length, l_m, could also vary the current ripple, however these parameters are fixed due to the use of a toroidal core.

The general pattern is that the larger current ripple produces higher EMI at low frequencies (150 kHz to 1 MHz), while the lower ripple has higher EMI for high frequencies (1 MHz to 30 MHz). This may be due to the fact that the larger ripple provides less inductance therefore the impedance is lower between the switch voltage and the LISN, thus producing a larger current through the LISN. A higher ripple is also known to reduce the reverse recovery problem of the fast diode. This could explain why the higher ripple produces less noise from 1 MHz to 30 MHz.

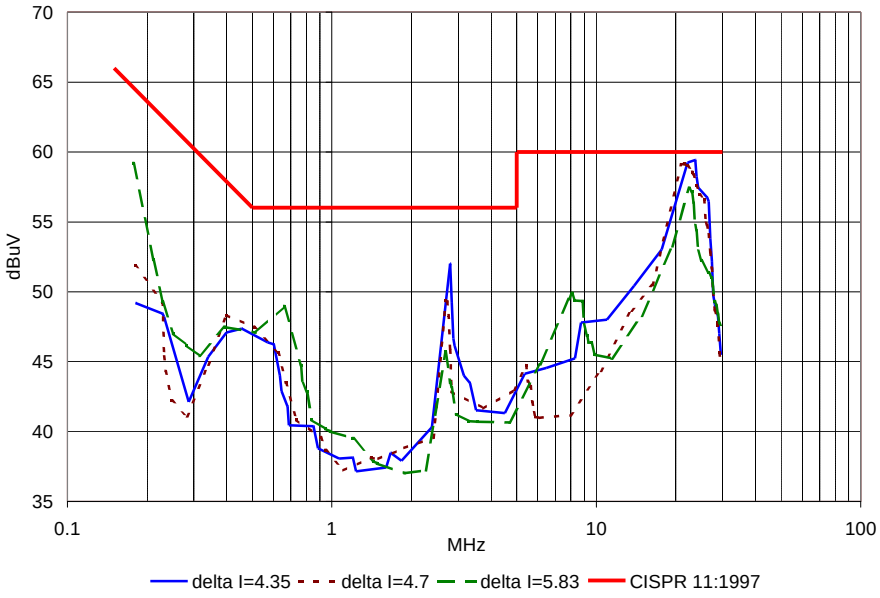


Fig. 4.17. Total Noise Envelope vs. Current Ripple

The next set of tests has been done with different current ripples using the T184-26 core. The input voltage, output power, and spectrum analyzer settings are identical to the tests with the T225-26 core. Fig. 4.18 displays the results from the tests with the T184-26 core. Here the effect of the reverse recovery ringing is even more apparent. There is a 10 dBμV difference between the EMI level at around 20 MHz. Fig. 4.19 shows the T225-26 core and the T184-26 core with approximately the same ripple. The low frequency behavior of the inductors is very similar. This makes sense because they both have similar inductances. However there is a slight difference in the high frequency behavior. In this range (5 MHz and above), the parasitics of the inductor are a dominant factor. These parasitics, such as inter-winding capacitance and inductive coupling between the inductor and other circuit traces, vary significantly for different cores. Different cores have different geometries, and the geometry has significant influence on the inter-winding capacitance and the radiated flux.

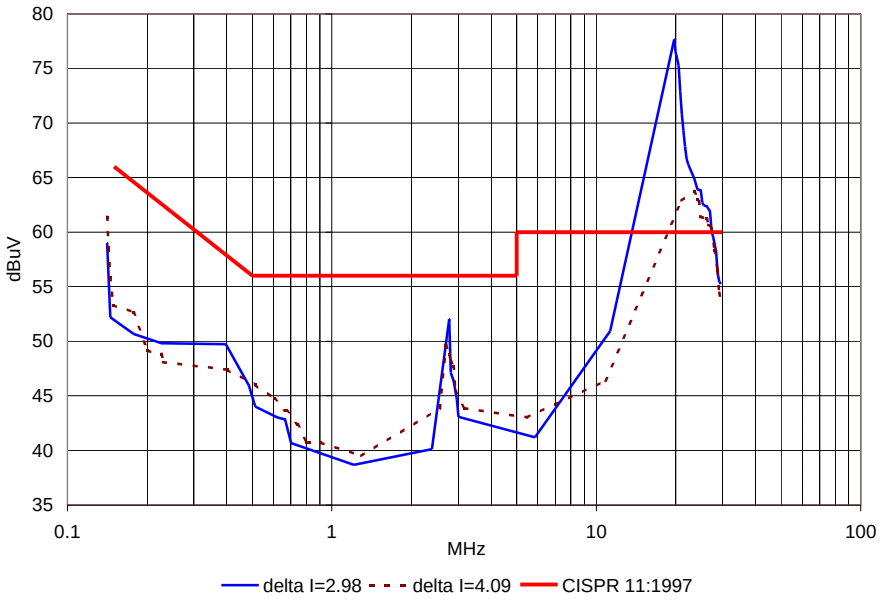


Fig. 4.18. Total Noise Envelope vs. Current Ripple

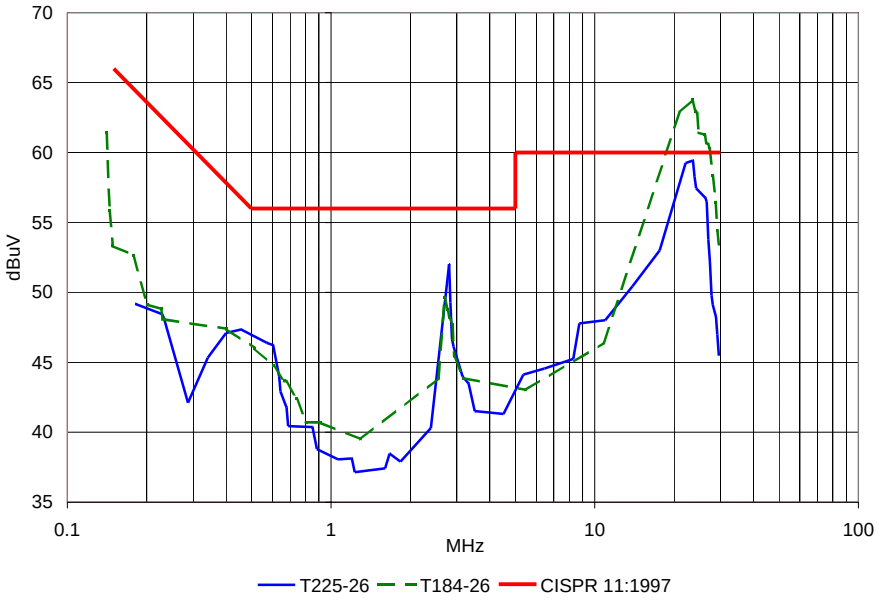


Fig. 4.19. T225-26 Core vs. T184-26 Core

To summarize, the larger inductor current ripple produces less EMI noise in the high frequency range (1 MHz to 30 MHz), but it produces more EMI noise in the low frequency range (150 kHz to 1 MHz). Also, the noise at high frequencies varies with different cores.

4.2.3.3 Switching Frequency

The switching frequency is also varied to determine the tradeoffs related to EMI. This testing is divided into two sections. The first tests are from 25 kHz to 45 kHz switching frequency using an IGBT. The second group of tests is performed from 35 kHz to 65 kHz using a MOSFET. This accomplishes two goals. The EMI spectrum can be analyzed over a wider switching frequency range that is not limited by the frequency bound on the IGBT. This method also allows the differences between a MOSFET and IGBT to be studied. All tests are performed with an input voltage of 230 Vac, a constant current load of 3.3 A, an attenuation of 30 dB on the spectrum analyzer input and a resolution bandwidth of 10 kHz. The circuit parameters are the same as those listed in Table 4.1 except that the switching frequency and switch are varied. The IGBT used is the Intersil HGTP7N60A4 while the MOSFET used is the International Rectifier IRFP22N60A. The IGBT is tested with switching frequencies between 25 and 45 kHz. The results are shown in Fig. 4.20.

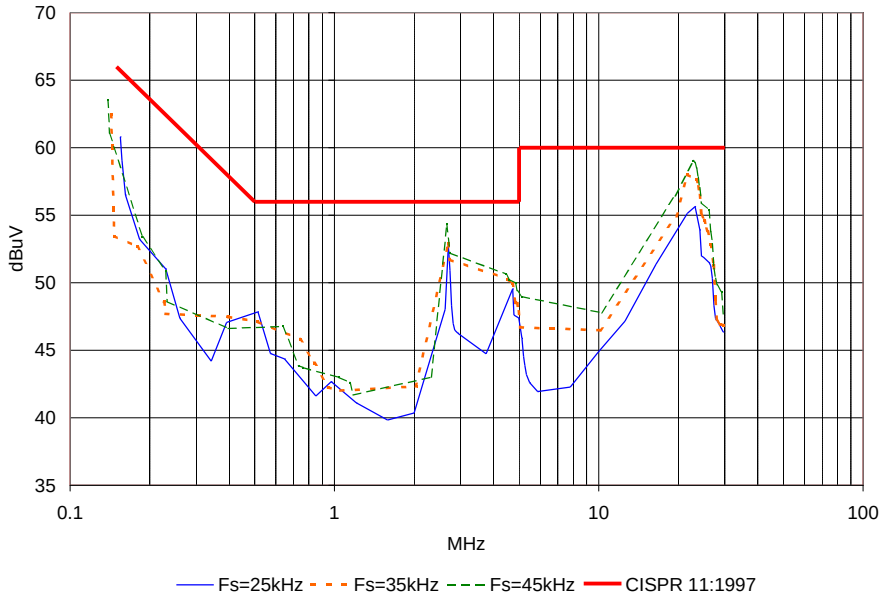


Fig. 4.20. Total Noise Envelope for an IGBT at Several Switching Frequencies

From the results in Fig. 4.20, it can be observed that the EMI noise increases as the switching frequency increases. As switching frequency is increased, more harmonics are pushed into the measurement range (0.150 – 30 MHz), thus the EMI levels increase. This is more noticeable in the high frequency range (1 MHz to 30 MHz) because after 1 MHz the filter is less effective due to the filter parasitics. It is also important to note that the EMI filter given in Table 4.1 has been designed for a switching frequency of 35 kHz. Although EMI noise increases, raising the switching frequency by 10 or 20 kHz may be an option to reduce the size of the inductor.

The switching frequency also is varied using a MOSFET for the switch. Fig. 4.21 shows the results of this testing. These data show the same behavior observed in the tests with the IGBT. The EMI noise increases as the switching frequency increases. The limit for increasing the switching frequency is about 65 kHz. However this is only for the current filter design and layout.

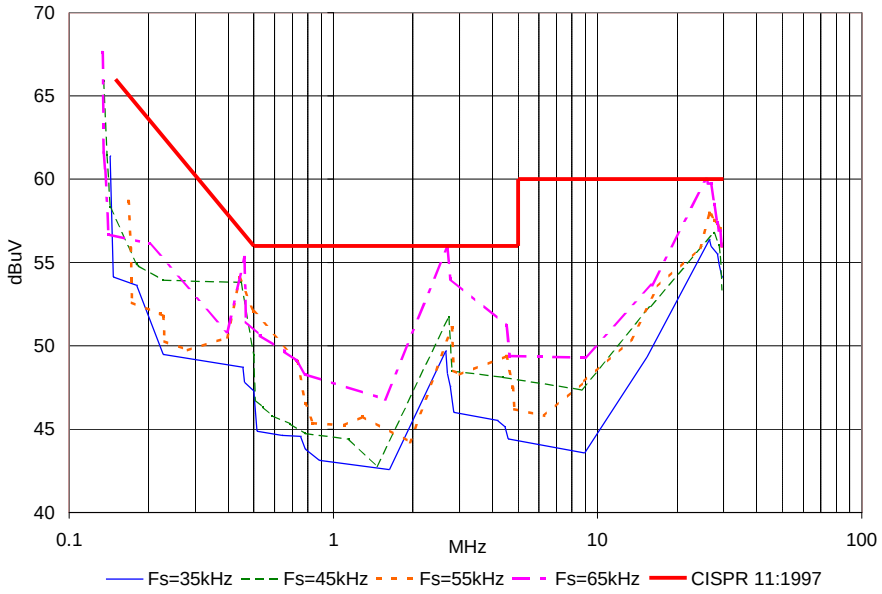


Fig. 4.21. Noise Envelopes for a MOSFET at Several Switching Frequencies

4.2.3.4 IGBT vs. MOSFET

Since the IGBT and MOSFET have different switching characteristics (delay time, rise time, etc.), it is interesting to compare the EMI generated from each switch. However, it should be noted that the same heat sink is used for both the IGBT and MOSFET. Each switch has a different thermal resistance, so if the same heat sink were used then each switch would operate at a different temperature. As stated in Section 4.1, the temperature has a direct influence on rise, fall, and delay times. Therefore, the EMI characteristic of the switch is also temperature dependent. This temperature dependence has not been studied here. However some general conclusions can be made. Fig. 4.22 and Fig. 4.23 show that the EMI noise is lower for the MOSFET in the high frequency range (1 MHz to 30 MHz), while the EMI noise is lower for the IGBT in the low frequency range (150 kHz to 1 MHz). Since the high frequency characteristic is dominated by parasitics, it could be possible that the packaging of the IGBT inherently leads to greater EMI production.

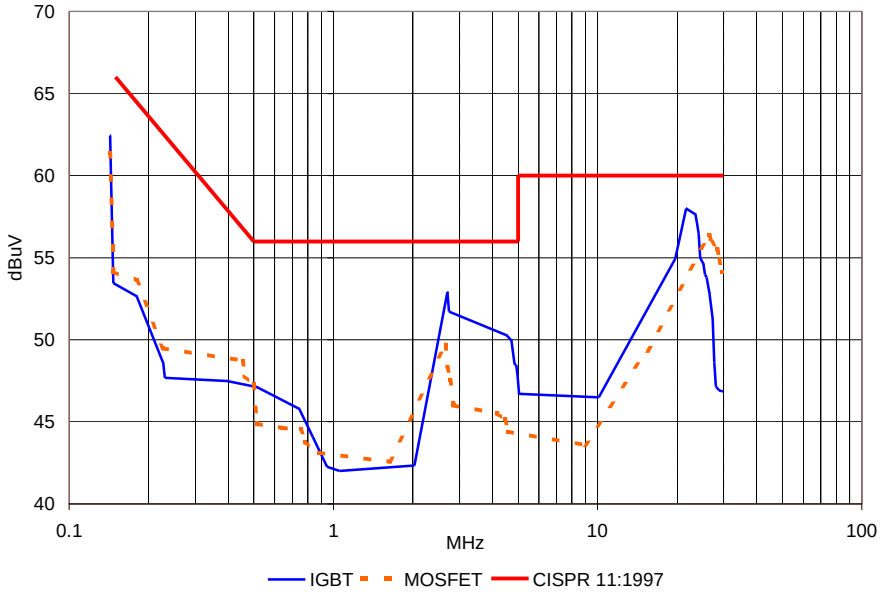


Fig. 4.22. Noise Envelopes with IGBT and MOSFET switching at 35 kHz

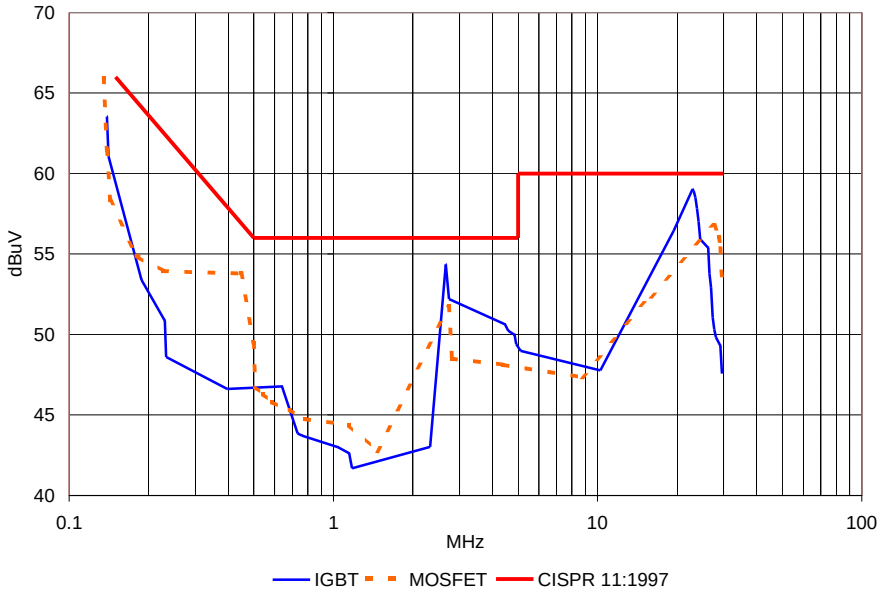


Fig. 4.23. Noise Envelopes with IGBT and MOSFET switching at 45 kHz

4.2.3.5 Input Voltage

In this application, the line voltage can vary from 180 to 264 Vac. In EN55011, it states that the test site must provide a well-regulated line voltage. However, studying the effect of the input voltage can lead to additional insight into the mechanisms of conducted EMI generation. Fig. 4.24 shows that as the line voltage decreases the noise level increases. This is especially obvious around 50 kHz. As the line voltage is lowered, the peak current must grow higher in order to maintain the same power output. Therefore the inductor saturates more thus reducing its ability to attenuate EMI.

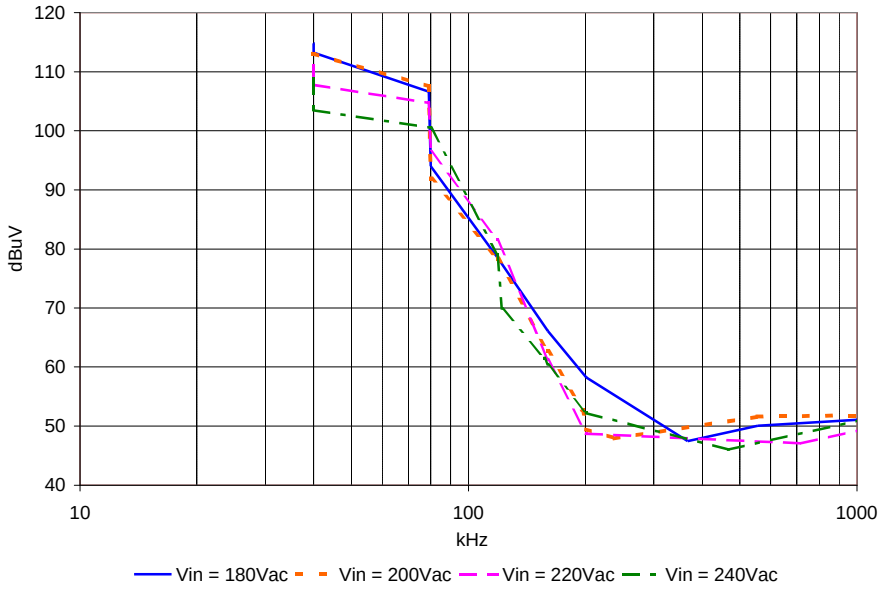


Fig. 4.24. Total Noise Envelope for Several Values of Input Voltage

4.3 Summary

Certain trends in the thermal behavior of the circuit have been observed. It is clear from Fig. 4.3 that in determining the switching frequency, there is a tradeoff between the temperature rise of the switch and core. Due to the fact that the rest of the circuit is fairly insensitive to the switching frequency (with regard to temperature rise), the switching frequency could be used to directly affect the thermal performance of the switch and core. In Fig. 4.5, it is shown that the current ripple can be used to directly affect the temperature rise of the core. However, the switch and diode are also sensitive to the current ripple. Adding even more complexity is the fact that

the switch and diode are not affected in a simple manner by a change in current ripple. The optimum value of the gate resistance in order to minimize the temperature rise in the switch and fast diode appears to be around 20 Ω however from the EMI data Section 4.2.3.1 it is apparent that the gate resistance also affects the EMI noise levels.

Accurate EMI measurements have been realized and several tests have been performed. In PFC applications, the spectrum changes from sweep to sweep so it is important to take the average of several sweeps to determine the most appropriate data set. The gate resistance can significantly affect the high frequency EMI noise level. A larger current ripple provides better performance above 1MHz. Conversely; a smaller ripple provides better performance below 1MHz. When the switching frequency is increased, the noise levels at high frequencies (above 1MHz) increase at a greater rate than noise levels at medium frequencies. The MOSFET is worse for low frequencies while the IGBT is worse for higher frequencies. A decrease in the mains voltage causes the EMI noise level to increase if the boost inductor saturates.

Many tradeoffs have been highlighted in the data presented in this chapter. As shown in Chapter Three, the EMI models are accurate up to the first limited harmonic. Therefore all tradeoffs concerning thermal performance and low frequency EMI can be considered by the GA. However, parameters influences on the high frequency cannot be considered. In Chapter Five a per unit analysis is presented that enables a designer to consider both thermal and EMI performance on the same scale. In this way it is possible to evaluate some of the tradeoffs concerning high frequency EMI and also to validate the designs produced by the GA.

Chapter Five

5 Thermal and EMI Tradeoff Analysis and Optimization Results

5.1 Tradeoff Analysis

Using optimization techniques, it is possible to deal with the tradeoffs between EMI and thermal behavior in an automated way. There are some instances where it is not efficient to implement an intensive optimization procedure. Many experienced designers already have an idea of two or three good designs that are close to a global minimum. Additionally, good models of high frequency EMI levels do not exist. Therefore to explore tradeoffs relating to high frequency EMI, an experimental approach must be taken. However quantifying the tradeoffs between thermal and EMI behavior is not a trivial task. In the following section a per unit analysis of thermal and EMI levels is proposed. The test data from Chapter Four is then analyzed on a per unit basis.

5.1.1 Figures of Merit

In order to compare thermal and EMI levels, a figure of merit (FOM) has been developed. The idea is to assign a single, normalized value to the EMI level. The object of the EMI filter is to attenuate the EMI such that the converter complies with the standard limit; therefore, any figure of merit should be related to the standard. Fig. 5.1 shows the EN 55011 standard for the Class B quasi-peak measurement. In this case, if the EMI level is higher than the standard at any one point, then the converter violates the standard. For this reason, it is more interesting for the figure of merit to consider the peak EMI level rather than an average or rms type quantity. Finally, any figure of merit should be simple to calculate and use. Taking into account all these considerations, the EMI figure of merit is noise peak closest to the standard divided by the standard at that frequency. In this way, it is possible to have a per unit (pu) number that can be compared to the temperature rises in the circuit. Additionally, the EMI standard could be divided into three regions and a figure of merit could be assigned to each region (see Fig. 5.1). Using the example depicted in Fig. 5.1, the figure of merit for region 1 would be applied to the noise peak in red because it is the closest to the standard in region 1. Its value would be

$$FOM1 = \frac{60}{66 - 19.12 \cdot \left[\frac{\log(200k)}{\log(10)} - \frac{\log(150k)}{\log(10)} \right]}$$
$$= 0.94\,pu.$$

A pu value can be assigned to temperature rise in much the same way. For semiconductor devices, a maximum allowable case temperature can be determined from the data sheet. For the inductor core, a maximum temperature rise can be assigned based upon maximum PCB temperature, wire coating temperature, core coating temperature or core lifetime. For the prototype listed in Table 5.3 (same as Table 4.1), the lifetime criterion is the limiting factor. Therefore the pu temperature rise is simply the measured temperature rise divided by the maximum allowable temperature rise. For the semiconductor devices a maximum case temperature of 125 ºC has been selected. For the inductor core a maximum temperature of 200 ºC is used.

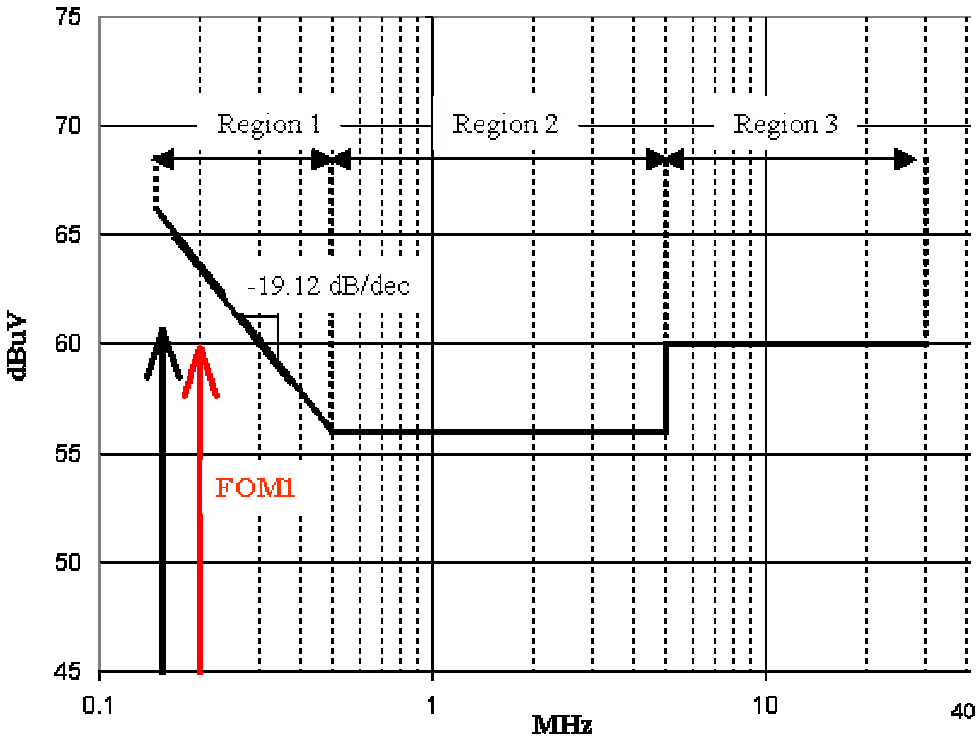


Fig. 5.1. EMI Standard and FOM Regions

5.1.2 Current Ripple

The amount of current ripple also affects the reverse recovery of the diode, the temperature of the switch and the core temperature. Therefore there are many factors to consider. The circuit parameters in Table 5.3 are used in all measurements except that the number of turns and the core type is varied. (Note that the use of the T184-26 core in the design listed in Table 5.2 is purely coincidental. The following results are all based upon the 35 kHz design.) The test set-up is the same as the one described in Chapter Four.

5.1.2.1 EMI Analysis

In Chapter Four many tests are presented showing thermal and EMI data for different current ripples and different cores. Using the figure of merits described in Section 5.1.1, this data can be further analyzed. Fig. 5.2 displays the results of the EMI per unit analysis for different current ripples on the T225-26 core. The quantity "Sum" in Fig. 5.2 is computed by adding the three EMI figures of merit and then normalizing the result (dividing by three). In Chapter Four it is stated that the larger ripple decreases the EMI in the upper frequency range. Using the per unit analysis shows that there is only a small reduction in the region 3 EMI level, FOM3, when the current ripple is increased. Comparing the 5.83 A and 4.35 A designs, there is only a 0.03 pu reduction in the FOM3 level at the higher current ripple. However there is a 0.16 pu reduction in the FOM1 level when comparing the 4.35 A and 5.83 A designs. Comparing the Sums of the EMI levels in Fig. 5.2, it is apparent that the best designs from an EMI point of view are the lower ripple values (4.35 and 4.70). The results of the testing with the T184-26 core are displayed in Fig. 5.3. The same poor performance is observed at lower current ripples; however the Sum indicates that the best design for EMI is at 4.09 A of ripple rather than 2.98 A. Overall, the best EMI designs are with the T225-26 core at 4.35 or 4.70 A of ripple.

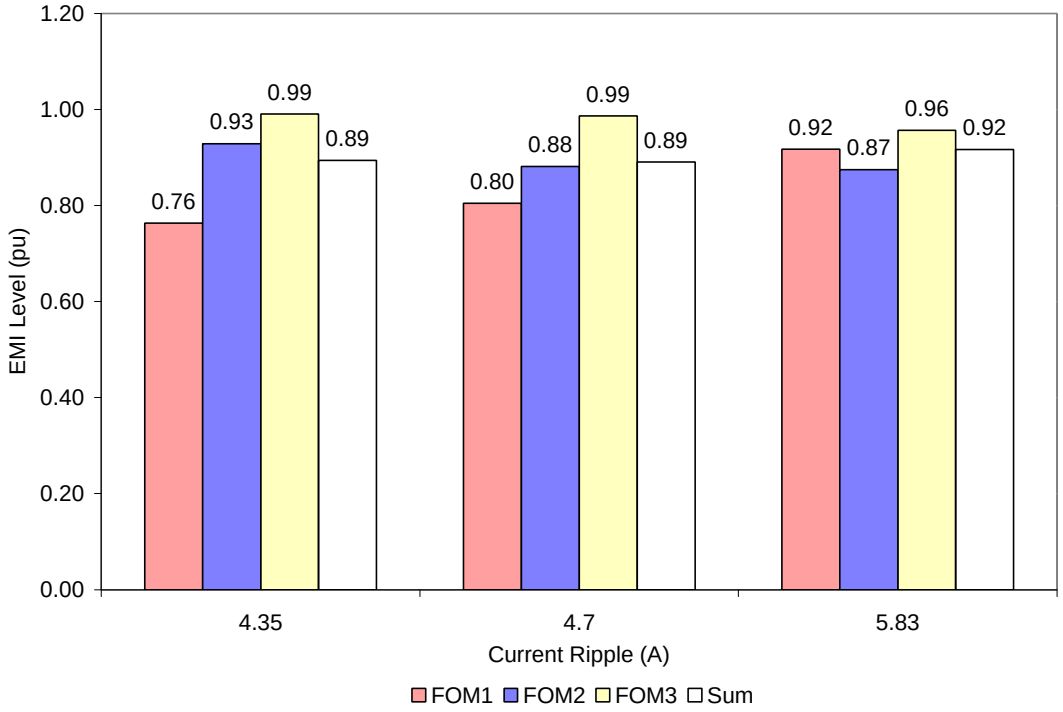


Fig. 5.2. EMI Levels vs. Current Ripple for the T225-26 Core

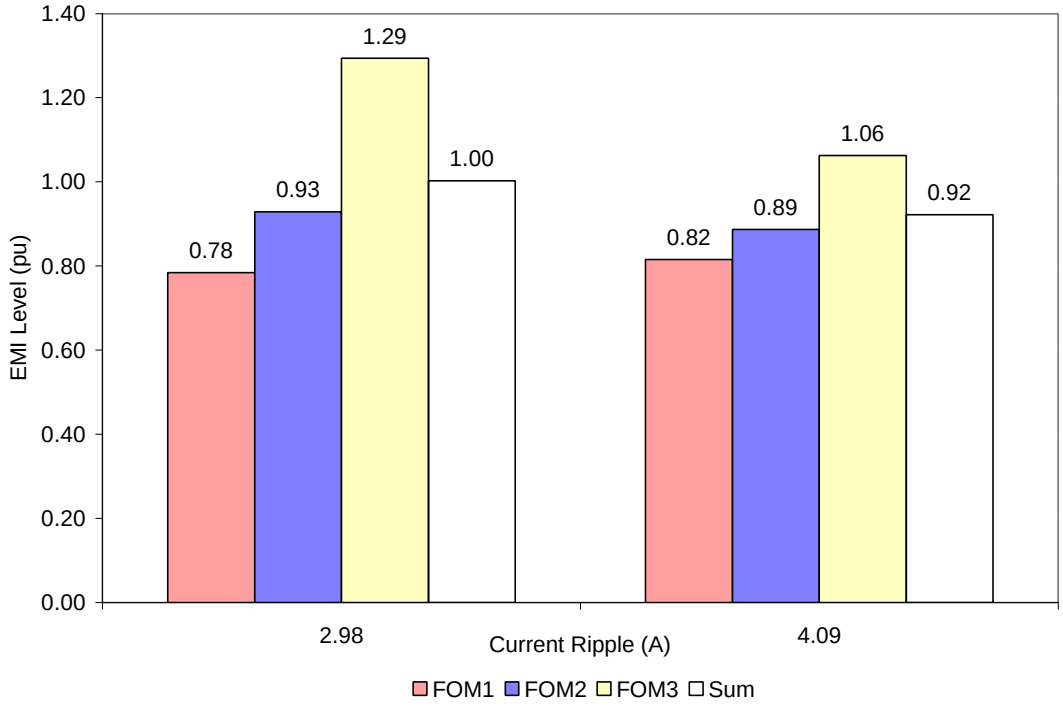


Fig. 5.3. EMI Levels vs. Current Ripple for the T184-26 Core

5.1.2.2 Thermal Analysis

The per unit analysis has been applied to the thermal data from Chapter Four in Fig. 5.4. The optimum point for the switch is with the T184-26 core at 4.09 A of current ripple. The T225-26 core is especially sensitive to current ripple. Excessive core losses cause the temperature to rise to almost 200 ºC at 5.83 A of ripple. The thermal trends for each design are reversed. The design with the T225-26 core increases with current ripple while the T184-26 design decreases with current ripple. Here it is important to consider the winding temperature. Although the thermocouple has been placed directly on the surface of the core, the inner inductor winding is still in direct contact with the couple. The design with the T184-26 core at 2.98 A current ripple requires 123 turns resulting in three winding layers. The 4.09 A design only requires 87 turns and less than two layers. The higher number of turns causes increased copper losses in the 2.98 A design and the multiple layers causes increased thermal coupling between the core and windings. Thus the windings are heating the core in the 4.09 A and 2.98 A designs. The designs with the T225-26 core have fewer thus the windings cover significantly less surface area of the core. This coupled with the lower copper losses results in the core temperature being higher than the winding temperature. Therefore the thermal behavior follows the core losses and not the copper losses. The variation in the switch and diode temperatures is a tradeoff between reverse recovery losses and turn-off losses, however the overall thermal figure of merit (Sum) follows the core temperature. This is in large part due to the dominance of the core temperature on the thermal figure of merit. The overall thermal optimum point is achieved using the T184-26 core at 4.09 A of ripple. It should be noted that all five tests were performed at a switching frequency of 35 kHz.

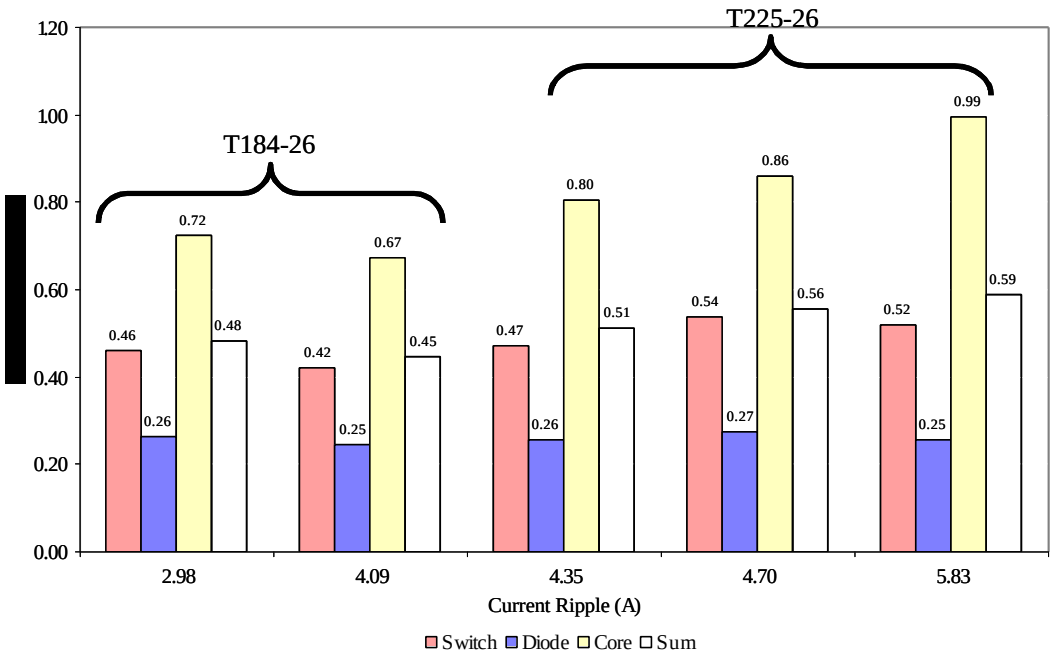


Fig. 5.4. Temperature Rise vs. Current Ripple

5.1.2.3 Thermal and EMI Tradeoffs

In Fig. 5.5, the trend in the EMI is toward a median current ripple value. If the ripple is too small, the high frequency EMI becomes excessive whereas if the ripple is too large the low frequency EMI is not attenuated enough. Looking at the normalized sum of both the EMI and thermal figures of merit, the best design is the one with the T184-26 core at 4.09 A of current ripple; however cost is not considered. The optimization results listed in Table 5.3 show that cheapest design is using the T225-26 core at 4.35 A of ripple. Although the EMI models do not include the effects of high frequency EMI, the per unit analysis has shown that in the case of the T225-26 core the low frequency effects are the most dominant.

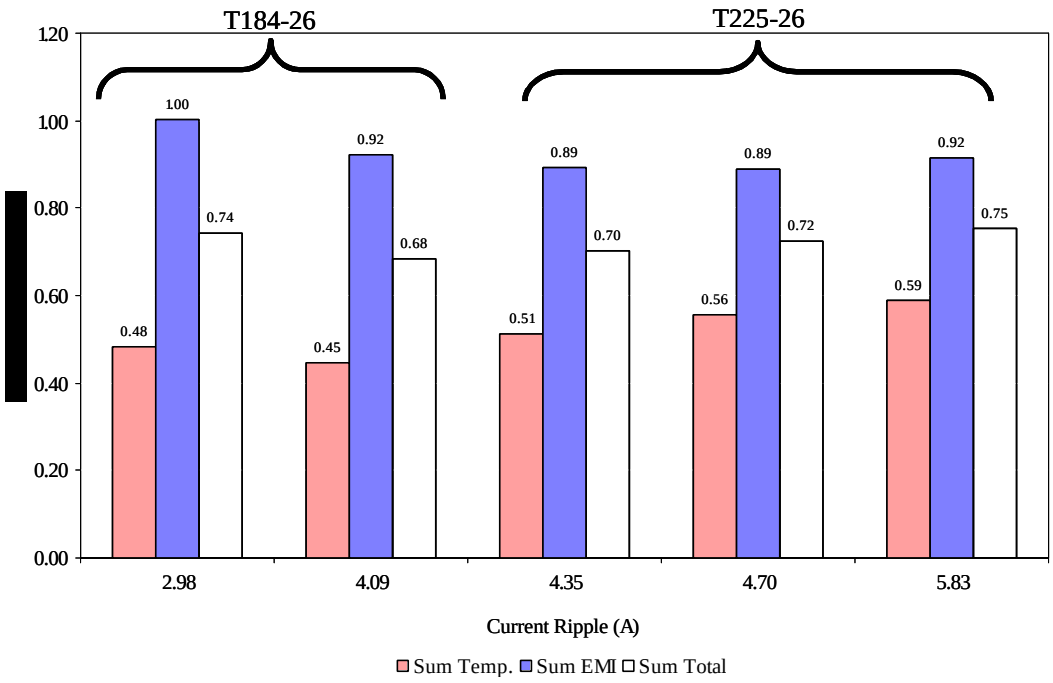


Fig. 5.5. Current Ripple Tradeoff Analysis

5.1.3 Switching Frequency

Switching frequency has a large impact on the converter design and performance. Core losses, switch losses, and the EMI levels are all directly affected by the switching frequency. The measurement set-up is the same as the one described in Chapter Four. The parameters/components in Table 5.3 are used except that the switching frequency is varied.

5.1.3.1 EMI Analysis

In Chapter Four many tests are presented showing EMI data for different current ripples and different cores. Using the figure of merits described in Section 5.1.1, this data can be further analyzed. In Chapter Four, it was observed that the MOSFET performs better than the IGBT at high frequencies while the IGBT is better at low frequencies. Comparing Fig. 5.6 and Fig. 5.7 this pattern is more obvious. The overall Sum of the EMI levels for 35 and 45 kHz shows that the MOSFET has better EMI performance. The general pattern in the IGBT data shows that as the switching frequency is increased FOM2 and FOM3 tend to increase more than FOM1. The MOSFET however has a more even distribution. The optimization tool does not consider this increase in the high frequency because the EMI model does not include the higher frequency

ranges. Since the IGBT cost was much less than the MOSFET, the GA tended to select low switching frequency designs using a IGBT, see Section 5.2. If the EMI model had considered the entire EMI spectrum, the better performance of the MOSFET may have offset its higher cost. A higher switching frequency design with a MOSFET would have lead to additional savings in the cost of the boost inductor.

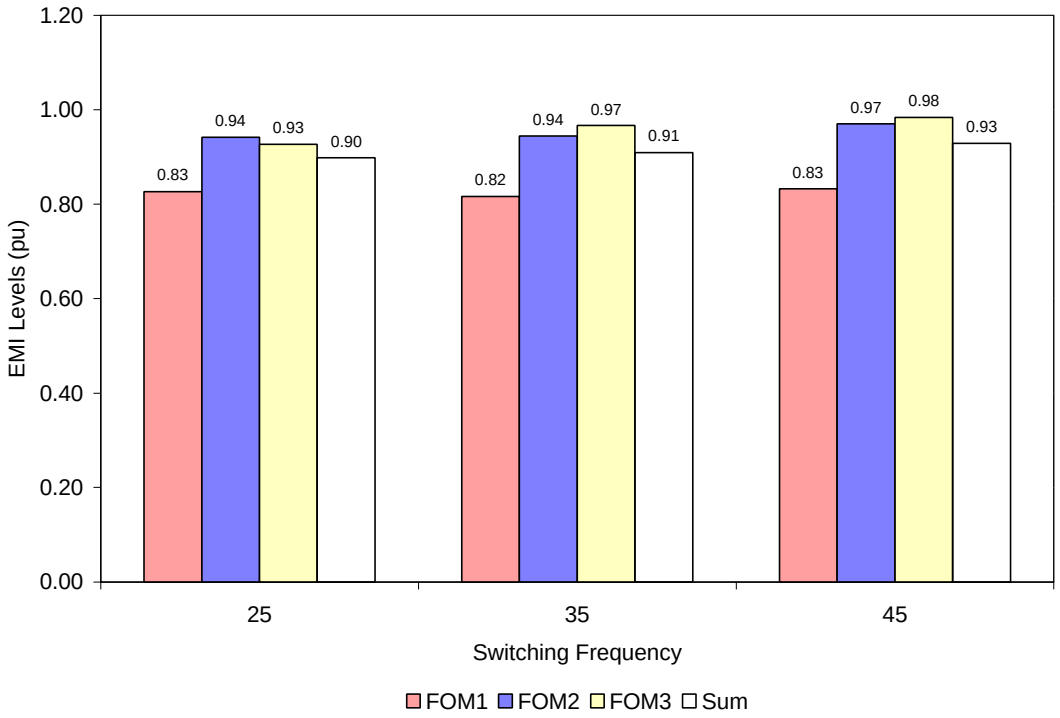


Fig. 5.6. EMI Levels vs. Switching Frequency for the IGBT

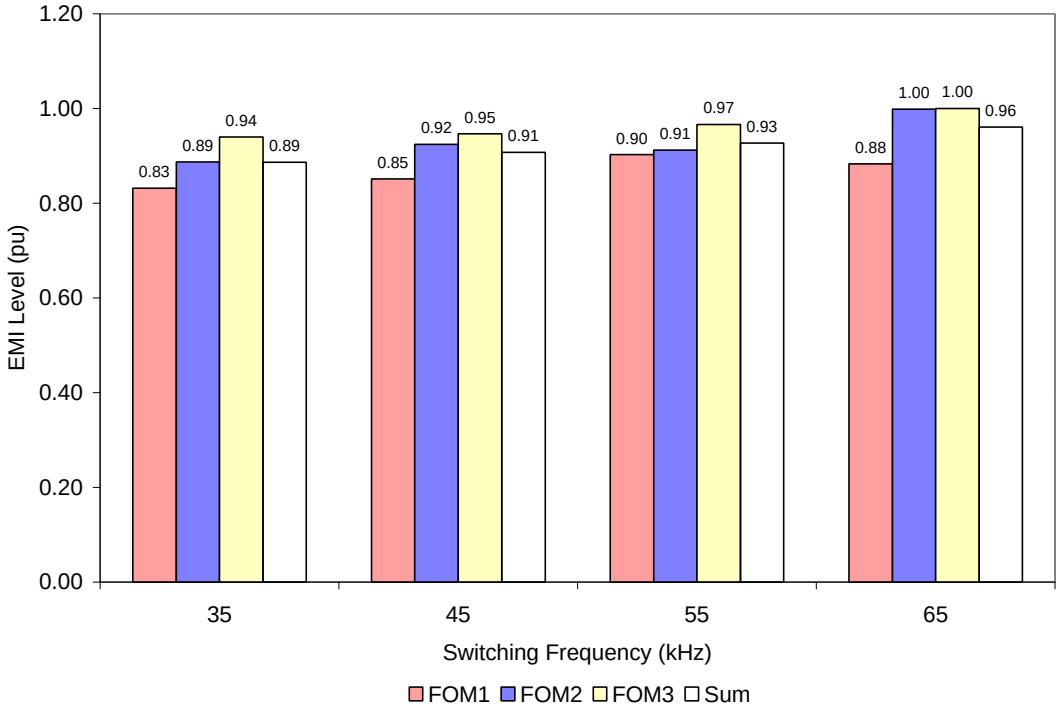


Fig. 5.7. EMI Levels vs. Switching Frequency for the MOSFET

5.1.3.2 Thermal Analysis

The EMI results alone dictate a low switching frequency when using an IGBT. When the thermal results are included, this conclusion is still correct. Fig. 5.8 shows that the best thermal design is at a switching frequency of 25 kHz. The switch temperature rise is increasing at a faster rate than the core temperature rise is decreasing. Thus the overall thermal performance of the converter is actually decreasing as the switching frequency increases.

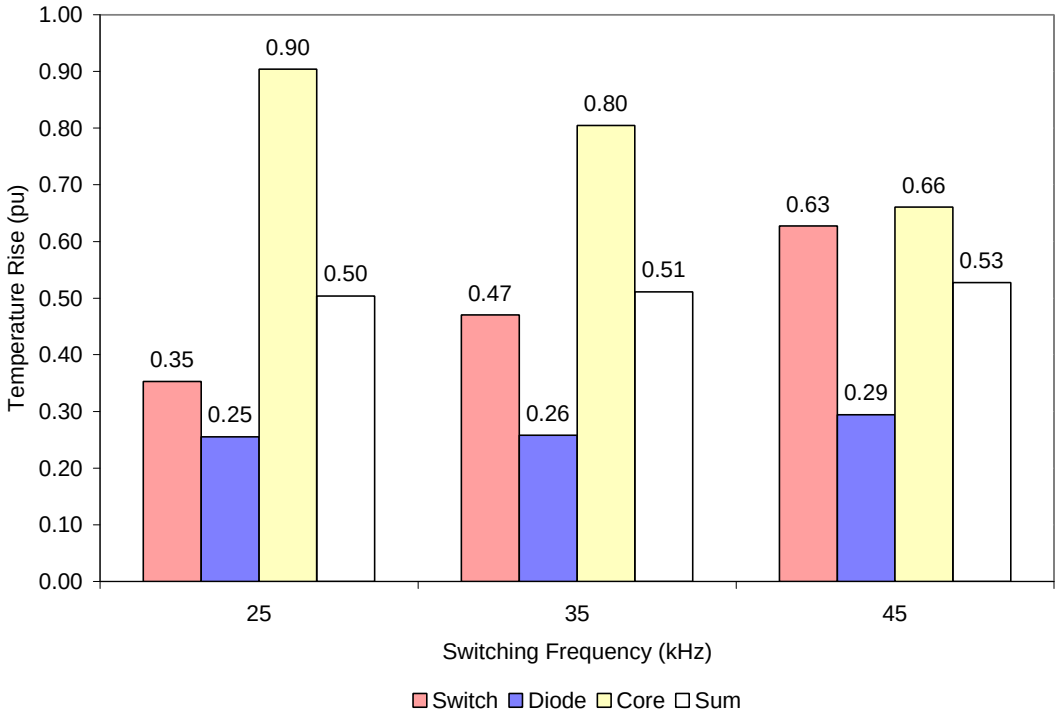


Fig. 5.8. Temp. Rise vs. Switching Frequency for the IGBT

5.1.3.3 EMI and Thermal Tradeoffs

The data in Fig. 5.9 shows that the lower switching frequency is clearly the best choice. The optimization results discussed in Section 5.2 agree with this conclusion. A design at 25 kHz places the sixth harmonic exactly at the same frequency as the start of the EN 55011 standard (150 kHz). In the final optimum design listed in Table 5.4, a slightly lower switching frequency of 24 kHz is selected. This is certainly a better design because it moves the sixth harmonic below the start of the standard.

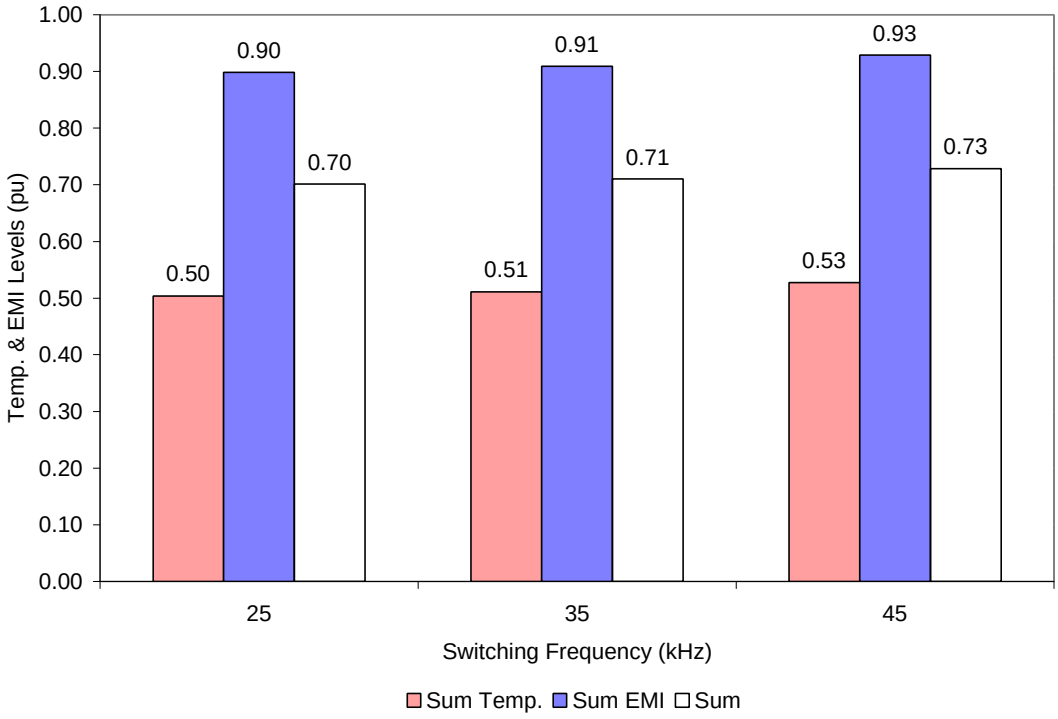


Fig. 5.9. Overall Comparison for different Switching Frequencies

5.1.4 Gate Resistance

The per unit analysis has been applied to the data in Chapter Four. The conclusion using this method confirms the conclusion in Chapter Four. The gate resistance is not considered by the optimization tool.

5.1.4.1 EMI Analysis

The results in Fig. 5.10 show that the EMI levels are relatively unaffected when the gate resistance is increased from 10 to 20 Ω. As the gate resistance is increased to 33 Ω, there is a significant change in the EMI levels. The most significant reduction is in the region 3 EMI level dropping 0.23 pu. The region 3 level also drops when the gate resistance is increased to 75 Ω ; however, the increases in the lower frequency regions cause the overall EMI performance to be the same. Obviously, the sensitivity of the EMI level changes depending on the resistance value. It should be noted that the switching speed is proportional to gate charge not gate resistance.

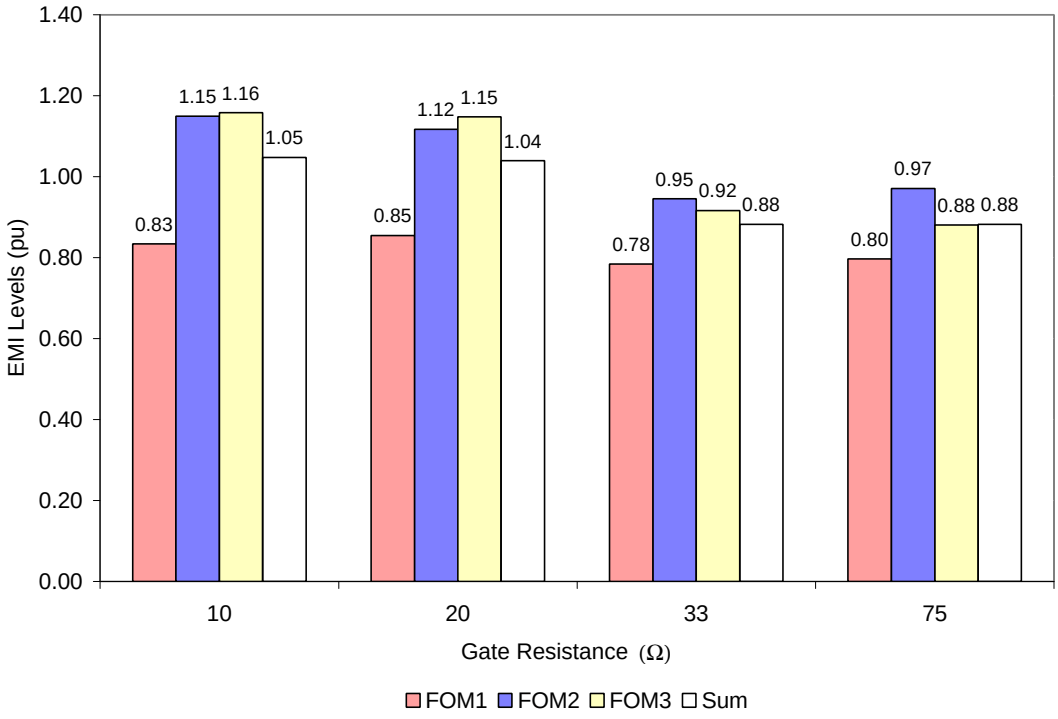


Fig. 5.10. EMI Levels vs. Gate Resistance

5.1.4.2 Thermal Analysis

As discussed in Chapter Four the thermal tradeoff with gate resistance is between over-lap and overshoot losses. In the IGBT, the switching losses are higher than the conduction losses therefore it is fairly sensitive to the gate resistance value. The inductor and diode temperature are fairly independent of the gate resistance value. Thus the overall thermal performance is dominated by the switching. Looking at the Sum and the switch case temperature in Fig. 5.11 shows that the optimum thermal design is at 20 Ω.

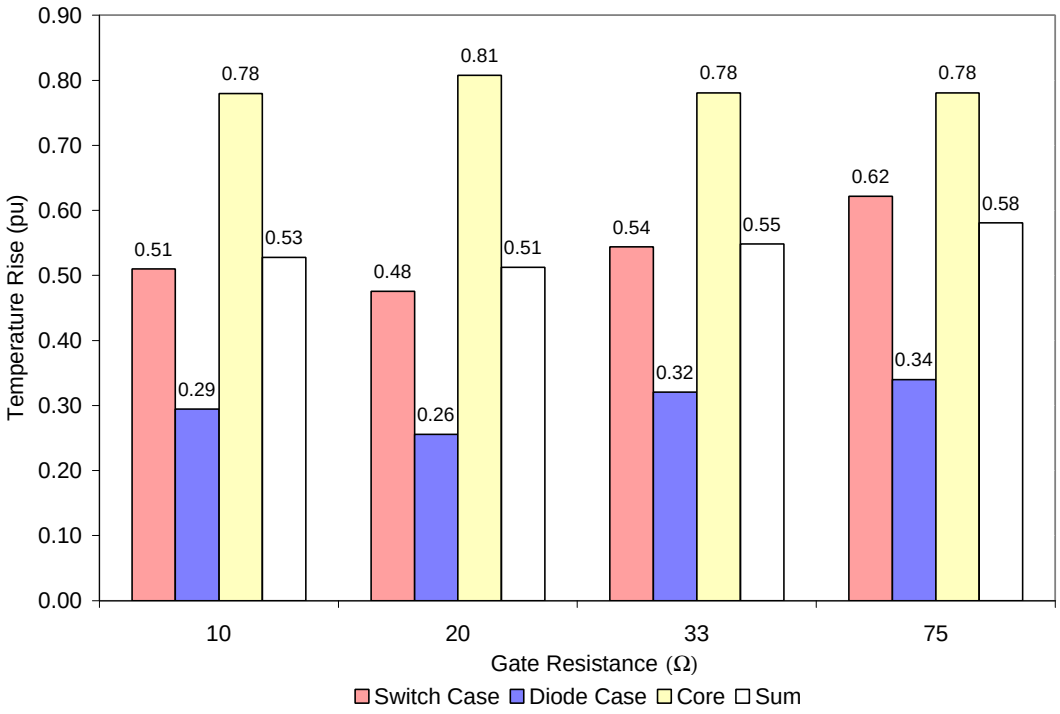


Fig. 5.11. Temperature Rise vs. Gate Resistance

5.1.4.3 EMI and Thermal Tradeoffs

In this case, the thermal optimum and the EMI optimum are clearly at different points. The penalty in the EMI level at 20 Ω is too high for that to be the best design point. The overall sum in Fig. 5.12 indicates that 33 Ω is the optimum point for thermal and EMI performance. This value is actually a very common choice for the switches used at this voltage and current level. However the above analysis does show that the gate resistance does provide another degree of freedom with which high frequency EMI can be controlled. For higher cost applications, the most effective way to control the switch slew rate and therefore the high frequency EMI would be to implement an active gate drive control [50].

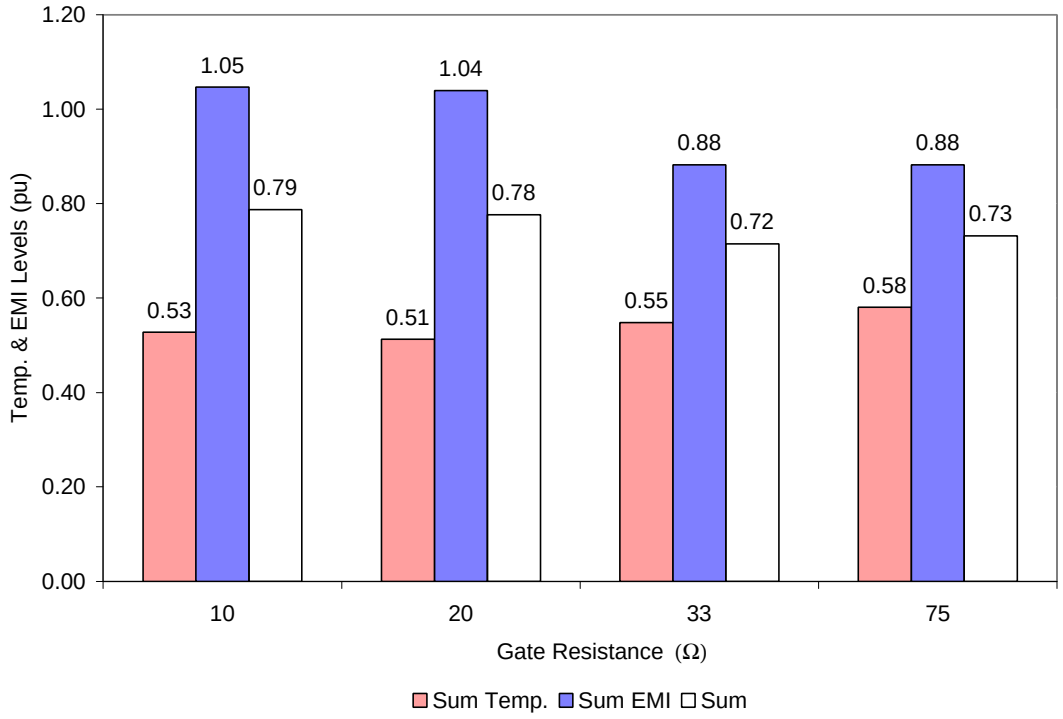
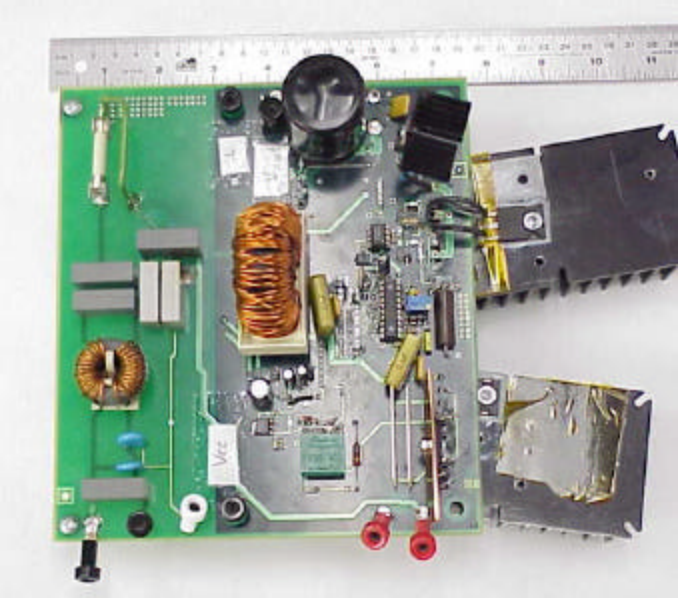


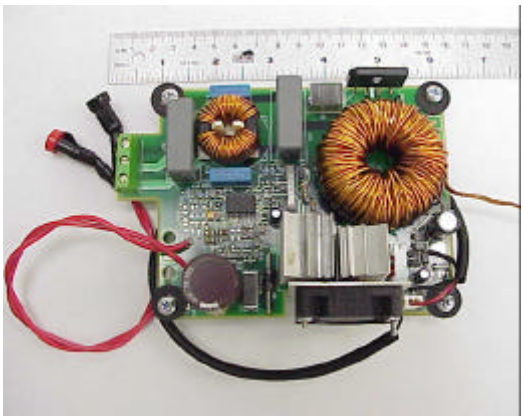
Fig. 5.12. Overall Analysis for varying Gate Resistances

5.2 Optimization Results

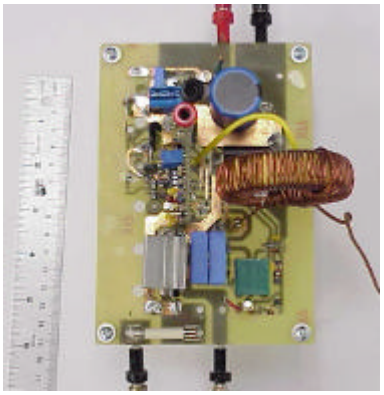
The details of the implementation of the GA are discussed in [13]. However some brief design results are shown here. The goal has been to design a minimum cost boost PFC circuit. This design processes has required much iteration between prototype development and validation of the software models. The corresponding prototypes are shown chronologically in Fig. 5.13. The prototype tested in Chapter Four is shown in Fig. 5.13(c) the components are listed in Table 5.3. As the optimization tool became more accurate the general progression was for lower switching frequency designs. As discussed in Section 5.1.1, the maximum inductor core temperature was chosen to be 200 ºC for the per unit analysis. This temperature is too high for safe operation on the PCB. However the design given in Table 5.3 yields very hot core temperatures (see Appendix Four Table A.5.1), so for the normalization factor to make sense it was set to 200 ºC. The high core temperature was a result of early thermal predictions that were inaccurate. The final design shown in Fig. 5.13(d) and listed in Table 5.4 was based upon more accurate thermal models and yielded cooler core operating temperatures.



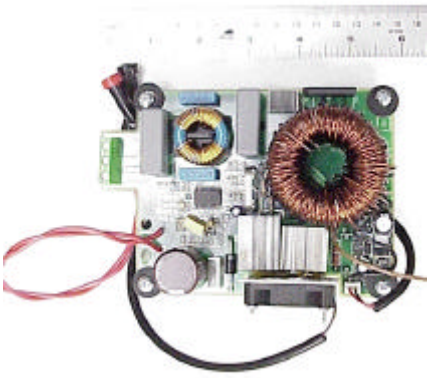
(a)



(b)



(c)



(d)

Fig. 5.13 a) 100 kHz Design, b) 45 kHz Design, c) 35 kHz Design, d) Final Design at 24 kHz

Table 5.1. Initial Prototype (shown in Fig. 5.13(a))

Component	**Reference/Value**
Switch(MOSFET)	IR: IRFP22N50A
Anti-parallel diode	NA
Fast diode	IR: HFA15TB60
Bridge Rectifier	Diode Inc.: FBI 8K 5M1
Boost Inductor	Pulse FEE: FEE 830-10-4
Common mode choke	SDI142-22: Lcm=3.3 mH, Ldm=8.4 µH
Cx(2)	1.47 µF
Cy(4)	10 nF
C_{in}	0.2 µF

Boost capacitor		390 μF + Drive capacitance
Switch heat sink		Single heat sink 1.3 ºC/W
Fast diode heat sink		Single heat sink 1.3 ºC/W
Rectifier heat sink		Copper plate
Fan		4.5” computer fan
Switching Frequency		100 kHz
Inrush Circutiry	Thyristor	Phillips: BT152-800R/B
	Pulse transformer	Timonta: IL1-11-1
Total normalized cost		100 units

Table 5.2. Second Prototype (shown in Fig. 5.13(b))

Component		**Reference/Value**
Switch(IGBTT)		Intersil: IRFP22N50A
Anti-parallel diode		Phillips: BYM36C
Fast diode		Motorola: MUR1560
Bridge Rectifier		Diode Inc.: FBI 8K 5M1
Boost Inductor		Micrometals: T184-26, 123 Turns of 16 AWG L=1.8mH, C=25pF, R=26kΩ, L_{SAT}=900μH
Common mode choke		SDI142-21: Lcm=3.3 mH, Ldm=8.4 μH
Cx(2)		1.0 μF
Cy(2)		10 nF
C_{in}		0.2 μF
Boost capacitor		68 μF + Drive capacitance
Switch heat sink		Thermalloy: ML516F
Fast diode heat sink		Thermally: ML516F
Rectifier heat sink		Thermalloy: ML516G
Fan		Sunon KDE1204PFB2-8
Switching Frequency		45 kHz
Inrush Circutiry	Thryristor	NA
	Pulse transformer	NA
Total normalized cost		55 units

Table 5.3. Third Prototype (shown in Fig. 5.13(c))

Component	**Reference/Value**
Switch	Intersil: HGTP7N60A4
Anti-parallel diode	Phillips: BYM36C
Fast diode	Motorola: MUR1560
Bridge Rectifier	Diode Inc.: GBJ806B
Boost Inductor	Micrometals: T225-26, 98 Turns of 16 AWG L=832μH, C=76pF, R=11.5kΩ, L_{SAT}=548μH
Common mode choke	SDI142-21: Lcm=1.65 mH, Ldm=4.03 μH
Cx(2)	2.24 μF
Cy(2)	10 nF
C_{in}	0.2 μF
Boost capacitor	100 μF + drive capacitance
Switch heat sink	Thermalloy: ML516F
Fast diode heat sink	Thermally: ML516F
Rectifier heat sink	Thermalloy: ML516G
Fan	Power-on: MO N5010B-8

Switching Frequency		35 kHz
Inrush Circutiry	Thryristor	NA
	Pulse transformer	NA
Total cost		50 units

Table 5.4. Final Design (shown in Fig. 5.13(d))

Component		**Reference/Value**
Switch		Intersil: HGTP7N60A4
Anti-parallel diode		Phillips: BYM36C
Fast diode		Motorola: MUR1560
Bridge Rectifier		Diode Inc.: FBI 8K 5M1
Boost Inductor		Micromet: T200-26B, 118 Turns of 16 AWG
Common mode choke		32V25 A0 00 SV2
Cx(2)		1.0 μF
Cy(2)		4.7 nF
C_{in}		0.2 μF
Boost capacitor		68 μF + drive capacitance
Switch heat sink		Thermalloy: ML516F
Fast diode heat sink		Thermally: ML516F
Rectifier heat sink		Thermalloy: ML516G
Fan		Sunon KDE1204PFB2-8
Switching Frequency		24 kHz
Inrush Circutiry	Thryristor	NA
	Pulse transformer	NA
Total normalized cost		42 units

A final estimated cost reduction of approximately 58 % has been achieved in the optimum design with respect to the initial. Around 45-50% of this reduction can be attributed to the following:

- Elimination of the inrush current circuitry by selecting bridge diodes and fast diodes with enough surge current rating to withstand the possible transients.
- Reduction of the required output boost capacitance in the optimum design by prudent selection of the boost output voltage and by utilizing the DC link capacitor in the motor drive.
- Selection of Iron Powder as the core material instead of Kool Mu, and custom design of the boost inductor instead of buying a standard one from a manufacturer.
- Selection of separated heat sinks, which decreases the common mode noise levels, and therefore allows a smaller common mode choke to be selected.

The initial design operates at a high switching frequency (100 kHz), thus requiring a more expensive heat sink and EMI filter as a result of the increased switching losses and EMI noise

level. The remaining reduction (approximately 10 %) can be attributed to the automated optimization design performed by the GA. Although 10 % may seem like a small cost reduction, it comes from the GA's ability to consider all the complicated thermal and EMI interrelationships simultaneously. Also, the GA uses actual cost information. By selecting components based on cost the GA can make some non-intuitive choices that lead to a lower cost design. For example, Fig. 5.5 shows that the best design considering thermal and EMI performance is one using the T184-26 core at 4.09 A of current ripple. However, the optimization tool selected the design using the T225-26 core at 4.35 A of current ripple. Although this design has does not perform as well electrically, the overall cost of the design is still less. (Note that this result is for an optimum design switching at 35 kHz.) The optimization tool's ability to consider many parameters simultaneously and incorporating the actual component cost is a significant improvement from the traditional design process. Normally, a designer does not have the time to consider all the available components and evaluate their individual costs. The GA, however, is ideal for that type of analysis. Thus the software tool developed (OPES) for the design optimization of the boost PFC stage and input EMI filter can be of valuable help in the design of future prototypes, providing low-cost designs in a short time for any desired specifications for which the topology considered is appropriate.

5.3 Summary

Important tradeoffs have been identified. These tradeoffs provide a better understanding of the mechanisms that affect high frequency EMI and thermal levels. EMI and thermal figure of merits have been developed so that the two behaviors can be easily compared. Using this method, it is possible to quantify changes in the EMI and thermal levels on the same scale. It is also possible to evaluate the sensitivity of the EMI and thermal behaviors over certain ranges of selected parameters. Design issues not covered by the optimization tool have been discussed and areas for improvement have been identified. The results of the tradeoff analysis show that lower switching frequency and lower current ripple are better design choices. This verifies the general behavior of the optimization program. The optimization program has also shown that it can choose optimum designs that are not obvious using traditional design approaches.

Chapter Six

6 Conclusions

6.1 Summary

Design issues such as boost capacitor and output voltage selection have been completed. The worst-case inrush values have been identified and the recommended device ratings are implemented as constraints in the GA. Layout guidelines have been developed to minimize common and differential mode noise. The converter performance under various operating conditions has been verified.

Switching and average models have been developed to verify the control design and to predict the converter performance transient conditions. The crucial parameters for the boost high frequency model have been identified and measured. Both switching and algebraic EMI models have been developed and their accuracy has been discussed. General algebraic temperature rise equations have been tuned and verified.

Important tradeoffs between EMI levels and temperature rises have been identified. An EMI and thermal figure of merit has been developed so that the two behaviors can be easily compared. The tradeoff analysis has highlighted certain strengths and weaknesses in the optimization procedure.

6.2 Future Considerations

The current reduced order thermal and electrical models require calibration for a specific topology and layout. As a result any implementation of GA's becomes problem specific and cannot be generalized for every power electronics design. The basic limitation is that the models have to be simple algebraic equations. There has been work to include more complicated thermal and EMI analysis into circuit optimization [51]. However as mentioned in Chapter One, these complicated models require a considerable amount of processor time, thus making GA's an unattractive option. To remedy the problem, a combination of optimization algorithms could be used. The GA could be used to create the initial population and find the minima of the design

space. The best designs could be chosen from each minimum region and more complicated EMI and thermal models could be applied to these designs. Another optimization algorithm could then be used to complete the optimization using more accurate models as depicted in Fig. 6.1.

There is a compromise between how accurate the electrical models need to be and how successful the GA is in finding the design space minima. If the GA can reliably find the minima with generalized reduced order models, then a different algorithm using more complex models could complete the rest of the optimization. A potential drawback of this method is that the GA must be managed in such a way to guarantee that all the minimum regions are found. This requires that the person operating the optimization tool have knowledge of the algorithms being used.

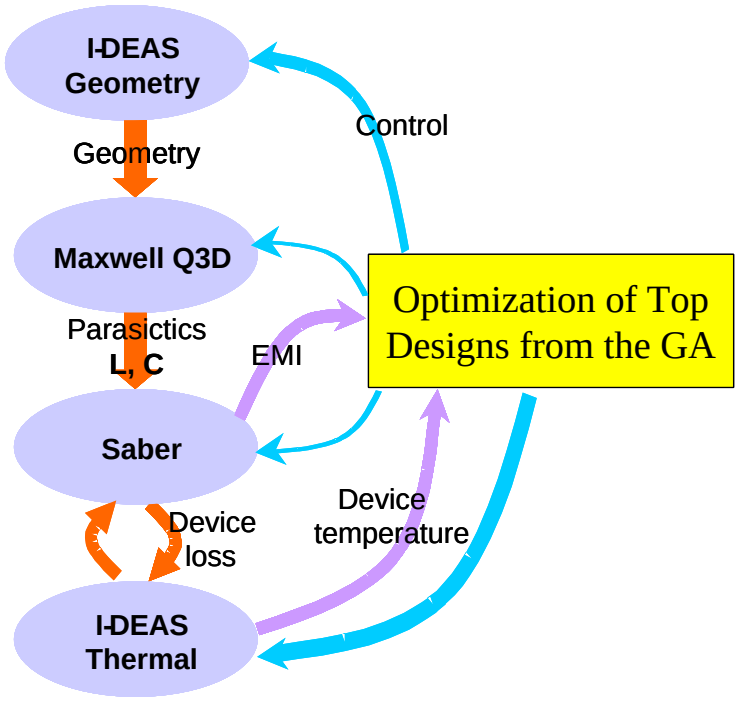


Fig. 6.1. Using an Optimization Tool to Manage Thermal and EMI Analysis

There should be more work done to provide generalized reduced order models. However the building blocks already exist. The loss equations for a MOSFET or IGBT for example do not change with layout or topology. Only the parameter values need to be adjusted. Presently temperature and loss predictions for magnetic components are not very reliable and should be improved. For EMI and thermal calculations the relationships are also complicated because they are greatly influenced by layout. Higher order EMI and thermal models for different layouts could be pre-calculated outside of the GA. This would create a database of layouts that the GA could choose from. The GA could then choose the best combination of devices and layout as shown in Fig. 6.2. This would result in a more generalized optimization procedure without compromising the speed of the algorithm.

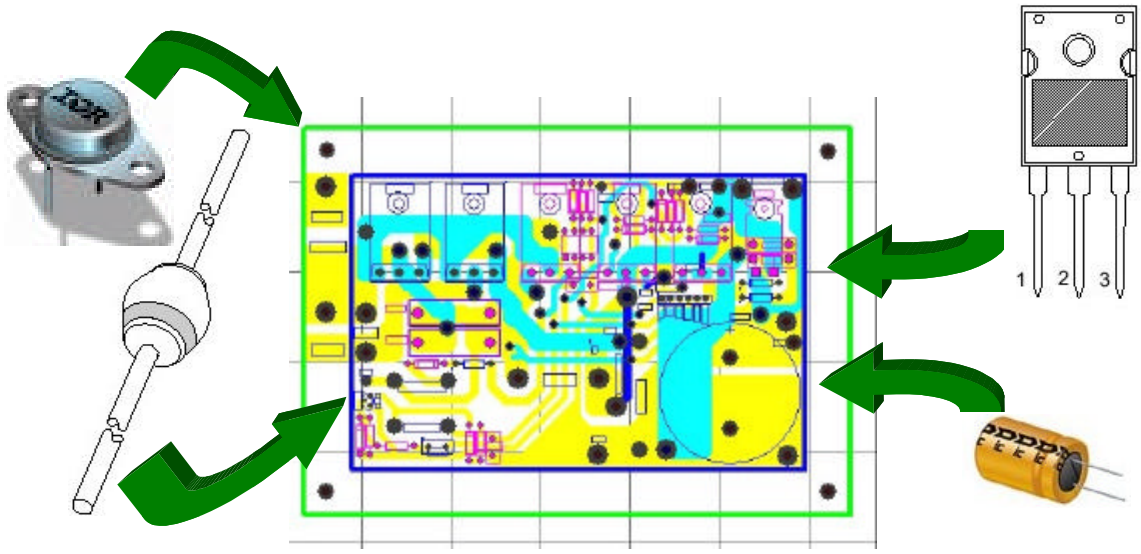


Fig. 6.2. Best Combination of Layout and Devices Selected by the GA

6.3 Conclusion

When using well-tuned models, GA-based optimizers have many advantages such as robustness, global optimums, and the ability to accurately predict circuit performance. As discussed in Chapter Five, it is important to simultaneously consider many issues to obtain the optimum power electronics design. A GA-based optimization tool is able to consider electrical, thermal, EMI, and cost issues at the same time. Thus ensuring that a global optimum point is achieved. This is a major step forward in optimization of power electronics systems. With the traditional gradient-based techniques referenced in Chapter One, it was very difficult to give a convincing argument that a global optimum had been reached. The optimization tool developed here has also gone further than previous attempts with GA's in [12] [14] [15] [16]. Here the tool produces a complete design that can be built and tested immediately after the optimization run. Also the actual cost of the system is known. Despite the current limitations, industry interest in such a powerful tool will no doubt inspire more research and continued refinement of GA-based optimization procedures.

Appendix 1

A.1 Control Design of a Boost PFC Circuit

A.1.1 Controller Design

The controller design is based upon the procedures described in [25] [26]. The following sections give a brief description of the operation of each control loop.

A.1.1.1 Current Loop

The purpose of the current loop is to force the input current to follow a sinusoidal reference. Therefore the current loop bandwidth must be high enough to easily track the current reference signal and low enough to provide adequate phase and gain margin.

A.1.1.2 Voltage Loop

The voltage loop regulates the output voltage. If the voltage loop bandwidth were very high, then the output voltage would be constant but the input current would be distorted. Therefore the voltage loop bandwidth must be less than the line frequency. A larger 2^{nd} harmonic voltage ripple is tolerated on the output thus allowing the current loop to regulate the input current more precisely.

A.1.1.3 Feedforward Network

The feedforward network is used to adjust the duty cycle to compensate for changes in the input line voltage. This is accomplished by supplying a DC signal proportional to the rms value of the line voltage. For this application, the feedforward network is not necessary.

A.1.2 Controller Design Example

The following equations and comments are used to provide an example controller design for a particular PFC boost circuit.

Control Design of PFC Converters

Design Specifications

Input AC Voltage	$Vi\_min := 180$ Vrms	$Vi\_max := 240$ Vrms
Output DC Voltage	$Vo := 354$ Vdc	
Output Power	$Po := 1150$ W	
Input Power	$Pin := \frac{Po}{0.9} \rightarrow 1277.7777777777777778$	
Switching Frequency	$fs := 40 \cdot 10^{3}$ Hz	
Line Frequency	$fl := 50$ Hz	

Given Power Stage Parameters

Capacitance of the drive	$Cdc := 920 \cdot 10^{-6}$
Boost Output Capacitance	$Cb := 68 \cdot 10^{-6}$
PFC Input Inductor	$L := 0.532 \cdot 10^{-3}$
Total Output Capacitor	$C := Cdc + Cb$
Minimum Output Capacitance	$C\_min := 680 \cdot 10^{-6} + 0.8 \cdot Cb$
Voltage Feedback Resistor	$R1 := 420 \cdot 10^{3}$
Current Sense Resistor	$Rs := 0.03$
External Ramp	$Vs := 5$

Control IC 4981 A

Magnitude and Phase Definitions

$$gain(X, s) := 20 \cdot \log(|X(s)|)$$

$$P(X, s) := \frac{180}{\pi} \cdot angle(Re(X(s)), Im(X(s)))$$

$$phase(X, s) := if(P(X, s) \geq 90, P(X, s) - 360, P(X, s))$$

$$phase1(X, s) := P(X, s) - 360$$

$$ga(X, y, s) := 20 \cdot \log(|X(y, s)|)$$

$$P(X, y, s) := \frac{180}{\pi} \cdot angle(Re(X(y, s)), Im(X(y, s)))$$

$$ph(X, y, s) := if(P(X, y, s) \geq 90, P(X, y, s) - 360, P(X, y, s))$$

$$ph1(X, y, s) := P(X, y, s) - 360$$

$$n := 0, 1 .. 600 \qquad f_n := 1 \cdot 10^{\frac{n}{100}} \qquad ff_n := 0.1 \cdot 10^{\frac{n}{100}}$$

Step 1 Multiplier Setup and the Feedforward Loop Design

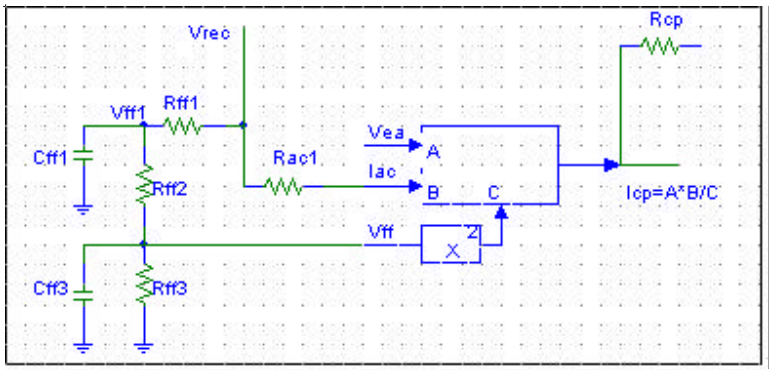


Fig 1 the Multiplier circuit in 4981

(1) Rac1 design

From the Date sheet of 4981, the port of Iac is to sense the rectified voltage and force the inductor current to follow the voltage.

$Iac\_max := 600 \cdot 10^{-6}$ A

the best working condition is $Iac := 300 \cdot 10^{-6}$ A

So

$$Rac1\_min := \frac{Vi\_max \cdot \sqrt{2}}{Iac\_max} \qquad Rac1\_min = 5.657 \cdot 10^{5}$$

SELECT $Rac1 := 10 \cdot 10^{5}$

(2) Feedforward voltage set

From the Data sheet of 4981, there is a relationship of the multipler input and output:

$$Icp = \frac{Iac \cdot (Vea - 1.28)}{Vff^2}$$

$Icp \le 2 \cdot Iac$

$1.4\ V \le Vff \le 4.5\ V$

$Vea \le 8.5\ V$

Normally set Vea=5.1V as the full-load voltage EA output, which means that we still have about 60% overload power limit.

When input voltage is the lowest, Iac is the lowest and Im will reach twice Iac, the EA output will be the maximum. So, we can get the minumun feedforward voltage requirement:

$Vea\_max := 8.5$

$Vea\_min := 0$ $\qquad Vff\_min := \sqrt{\frac{|Vea\_max - 1.28|}{2}}$ $\qquad Vff\_min = 1.9$

In this condition $\qquad Vff\_max := Vff\_min \frac{Vi\_max}{Vi\_min}$ $\qquad Vff\_max = 2.533$

Thus the design is in the range of 4981 working specifications.

(3) Feedforward loop design

(a)design resistors to get the desired feedforward DC voltage

From Fig 1, we have following relationship:

$$Vff1 = 0.9 \cdot Vi \cdot \frac{Rff2 + Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vff2 = 0.9 \cdot Vi \cdot \frac{Rff3}{Rff1 + Rff2 + Rff3} = Vff1 \cdot \frac{Rff3}{Rff2 + Rff3}$$

There are two voltage dividers. Define:

$$K1 = \frac{Vff1}{0.9 \cdot Vi} \qquad K2 = \frac{Vff}{Vff1}$$

Set K1=K2, we know:

$$Vff1 := \sqrt{\frac{0.9 \cdot Vi\_min}{Vff\_min}} \qquad Vff1 = 9.234$$

SELECT $Rff3 := 47 \cdot 10^3$

Given $Vff1 = 0.9 \cdot Vi\_min \cdot \frac{Rff2 + Rff3}{Rff1 + Rff2 + Rff3}$ $Vff\_min = Vff1 \cdot \frac{Rff3}{Rff2 + Rff3}$

$$Find(Rff1, Rff2) \rightarrow \begin{bmatrix} 3778953.2405620946409 \\ 181415.18049053693809 \end{bmatrix}$$

SELECT $Rff1 := 3.9 \cdot 10^6$ $Rff2 := 180 \cdot 10^3$

(b) design capacitors to attenuate the 2rd harmonic

Normally, the second harmonic ripple of the rectified voltage is 66.2% of the input AC line voltage, which is the input of the devider.

DESIGN the total harmonic distoration of Vff is less than 1%

So, the required attenuation is:

$$Gff := \frac{1}{66.2} \qquad Gff = 0.015$$

the filter is a second order filter. To get the widest bandwith, set the two poles at the same place and set the gain of each order filter as the same. So the cutoff frequency of each filter is:

$$fc := \sqrt{Gff} \cdot 100 \qquad fc = 12.291$$

So, we can get Cff1 and Cff3 as follows:

$$Cff1 := \frac{1}{2 \cdot \pi \cdot fc \cdot Rff2} \qquad Cff1 = 7.194 \cdot 10^{-8} \qquad Cff3 := \frac{1}{2 \cdot \pi \cdot fc \cdot Rff3} \qquad Cff3 = 2.755 \cdot 10^{-7}$$

SELECT $Cff1 := 82 \cdot 10^{-9}$ $Cff3 := 0.33 \cdot 10^{-6}$

(c) Get the transfer function and bode plot of the feedforward loop $Gff = \frac{vff}{vrec}$

From Fig 1, we konw

$$Kff := \frac{Rff3}{Rff1 + Rff2 + Rff3}$$

$$Wff := \sqrt{\frac{1}{Rff2 \cdot Cff1 \cdot Rff3 \cdot Cff3}} \qquad Fff := \frac{Wff}{2 \cdot \pi} \qquad Fff = 10.519$$

$$Qff := \frac{1}{Wff \cdot ((Rff2 + Rff3) \cdot Cff1 + Rff3 \cdot Cff3)} \qquad Qff = 0.443$$

$$Gff(s) := \frac{Kff}{1 + \frac{s}{Qff \cdot Wff} + \frac{s^2}{Wff^2}}$$

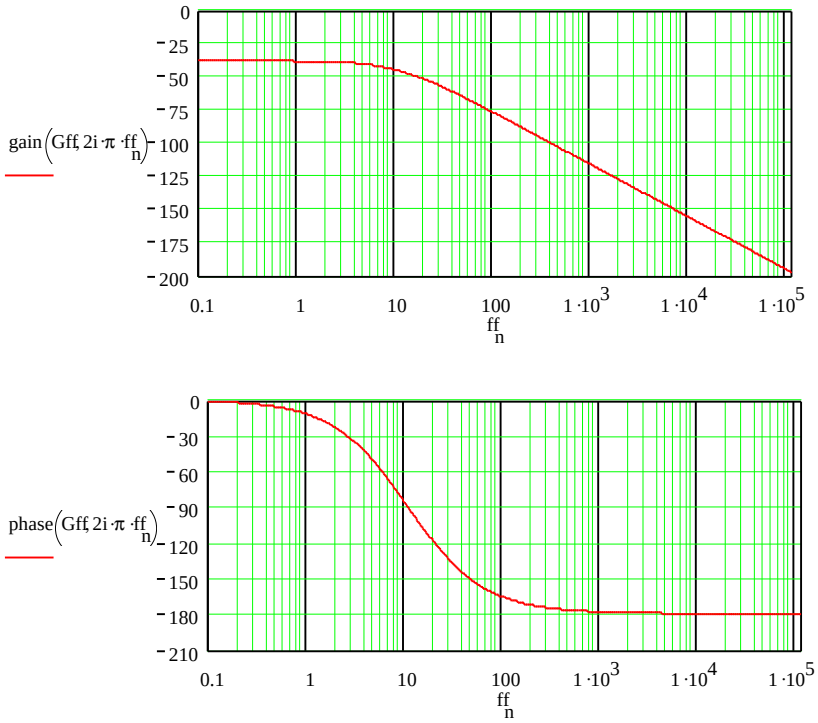


Fig 2 the Bode Plot of feedforward loop

$gain\_100 := gain(Gff, 2i \cdot \pi \cdot 100)$ $\qquad$ $gain\_0 := gain(Gff, 2i \cdot \pi \cdot 0)$ $\qquad$ $gain\_0 = -38.871$

$$Vff\_100 := 66.2 \cdot 10^{\frac{gain\_100 - gain\_0}{20}} \qquad Vff\_100 = 0.72$$

We can see, the designed filter can attenuate the 2nd ripple to 1% requirement. It satisfies the design requirement.

(4) Rcp design

Since Icp is the current reference, and the voltage across Rs is the sensed inductor current information, so it is required:

$$Rcp \cdot Icp = IL \cdot Rs$$

In the condition when Vi is lowest, and assume the PFC efficiency is 90%

$$IL := \frac{Pin}{Vi\_min}$$

$$Iac := \frac{Vi\_min \cdot \sqrt{2}}{Rac1} \qquad Icp := 2 \cdot Iac$$

$$Rcp := \frac{IL \cdot Rs}{Icp} \qquad Rcp = 418.299$$

SELECT $Rcp := 420$

Current Loop Compensator Design Procedure

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sensing resistor (Rs). The equation is:

$$Gc = \frac{vrs}{vcea} = Vo \cdot \frac{Rs}{Vs \cdot (sL)}$$

where Vo is the boost output voltage
Rs is the sensing resistance
Vs is the peak to peak voltage of the oscillator ramp
L is boost inductance

This equation is only valid for frequencies above the resonant frequency of the boost inductor and capacitor and below the switching frequency. For frequencies below the LC resonance the equation is different.

A zero at low frequency in the current amp response is used to give high gain which makes current mode control work. The gain of the current amp near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the oscillator ramp. These two signals are the inputs to the comparator in the L4981A.

The down slope of the inductor current current is maximum when the input voltage is zero. At this point (Vin=0) the inductor current is given by the ratio of the output voltage and the inductance (Vo/L). The current flows through the sensing resistor and produces a voltage with slope = VoRs/L. This slope multiplied by the gain of the current error amplifier must be equal to the slope of the oscillator ramp. If the gain is too high, then the slope of the inductor current would be greater than the ramp and the loop could go unstable. This instability would be greatest at the zero crossing of the input voltage.

The gain of the current amp near the cross-over frequency is simply :

$$Gcea = 1 + \frac{Rz}{Ri}$$ current amp gain

The current loop gain is simply Gcea*Gc

$$Gloop = \frac{Vo \cdot Rs \cdot Rz}{Vs \cdot 2 \cdot \pi \cdot f \cdot L \cdot Ri} + \frac{Vo \cdot Rs}{Vs \cdot 2 \cdot \pi \cdot f \cdot L}$$

The slope of the voltage across the sensing resistor is given by:

$$Cslope := Vo \cdot \frac{Rs}{L \cdot 10^6}$$

$Cslope = 0.02$ volts per microsecond

The slope of the oscilllator in the L4981A at 40kHz is given by

$$Oslope := Vs \cdot \frac{fs}{10^6}$$

$Oslope = 0.2$ volts per microsecond

Therefore the current amp must have a gain of: $\frac{Oslope}{Cslope} = 10.019$ at the switching frequency.

thus $Gcea := \frac{Oslope}{Cslope}$

Let $Ri := 10 \cdot 10^3$

therefore $Rz := Gcea \cdot Ri - 1$ $Rz = 1.002 \cdot 10^5$

SELECT $Rz := 0.91 \cdot 10^5$

Now the loop gain (Gloop) is set to one and thus the cross-over frequency can be found.

$$fic := \frac{Vo \cdot Rs \cdot \left(1 + \frac{Rz}{Ri}\right)}{Vs \cdot 2 \cdot \pi \cdot L}$$

$fic = 6.418 \cdot 10^3$

The placement of the zero in the current loop response must be at or below the cross-over frequency. If the zero is at fic then the phase margin would be 45 degrees. If the zero is below fic then the phase margin would be slightly more than 45 degrees. To place the zero directly at the cross-over frequency the impedance of Ccz at that frequency must be equal to Rcz. Thus the equation is:

$$Cz := \frac{1}{2 \cdot \pi \ fic \cdot Rz}$$

$Cz = 2.725 \cdot 10^{-10}$

SELECT $Cz := 220 \cdot 10^{-12}$

The selected value is clearly too low. This places the zero after the cross-over frequency thus our phase margin is less than 45 degrees. This is probably due to the fact that the value for Cz was chosen for the 100kHz prototype which had a different boost inductance.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. The best place for the pole is at half the switching frequency. In this way the pole does not affect the current loop response and it provides good attenuation at the switching frequency. However the pole should be at least one decade after the zero otherwise the phase margin would be greatly reduced.

$$fz := \frac{1}{2\cdot\pi\cdot Rz\cdot Cz}$$

$fz = 7.95\cdot 10^{3}$ frequency of the zero

$$fp = \frac{(Ccp + Cz)}{Ccp\cdot Cz\cdot Rz\cdot 2\cdot\pi}$$ frequency of the pole

sloving for Ccp

$$Ccp(fp) := \frac{Cz}{2\cdot\frac{\pi\cdot fp}{2}\cdot Rz\cdot Cz - 1}$$

$Ccp(10\cdot fz) = 5.5\cdot 10^{-11}$

$$fp := \frac{(Ccp(10\cdot fz) + Cz)}{Ccp(10\cdot fz)\cdot Cz\cdot Rz\cdot 2\cdot\pi}$$

$fp = 3.975\cdot 10^{4}$ In our case the switching frequency is too low for this technique to be effective.

SELECT $CCp := 0$

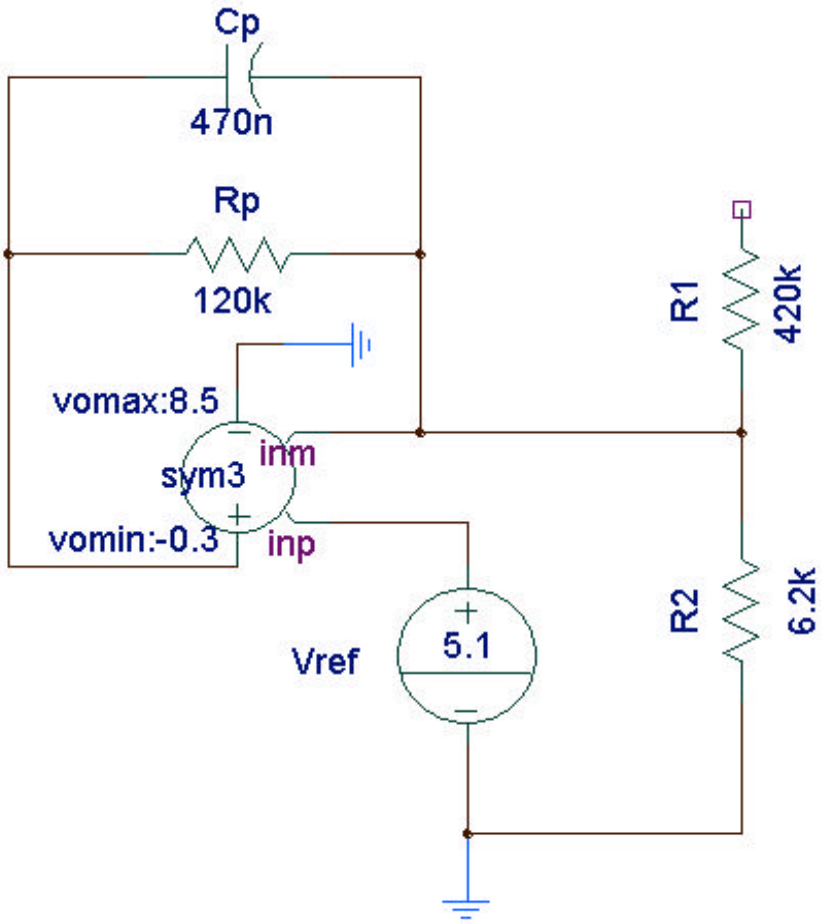


Figure 11: Voltage compensation network

Voltage Loop Compensator Design:

The voltage loop must be compensated for stability but because the bandwidth of the voltage loop is so much lower than the switching frequency the requirements for the voltage compensation are mainly driven by the need to reduce the input distortion.

A pole in the amplifier is needed to reduce the amplitude of the second harmonic and to shift the phase by 90 degrees.

The choice of R1 is somewhat vague. It is selected to be small enough so that the amplifier bias current does not affect the output but R1 must be large enough to avoid too much power dissipation. In our case:

$$R1 = 4.2 \cdot 10^5$$

Note that R2 has no effect on the small signal gain because the potential across R2 is fixed to Vref. The error amp small signal gain can be seen as the ratio between the error amp output ripple and the imposed output voltage ripple of the boost. The error amp output voltage can swing between 1.28 and 5.1V. A value less than 2.5% of the error amp swing voltage can be chosen to fix the value of Cp. So the desired gain at the output voltage ripple frequency determines the value of Cp. This will ensure proper attenuation at 100Hz (2*fl).

$$Gea(s) = \frac{1}{s \cdot R1 \cdot Cp} = \frac{vea}{vo}$$ error amp small signal gain

$\Delta Vvea := 5.1 - 1.28$ The error amp voltage swing

$ripple := 0.025 \cdot \Delta Vvea$ The amount of output ripple we will tolerate

$$Vopk := \frac{Pin}{2 \cdot fl \cdot \pi \cdot C\_min \cdot Vo}$$ the output voltage ripple

$Vopk = 15.645$ The peak to peak ripple would be twice this value.

$$Gea := \frac{ripple}{Vopk}$$ desired gain at 2*fl based on 2.5% distortion.

$$Cp := \frac{1}{2 \cdot \pi \cdot 2 \cdot fl \cdot R1 \cdot Gea}$$ Cp is selected to acheive the desired gain at 2*fl

$Cp = 6.208 \cdot 10^{-7}$

SELECT $Cp := 470 \cdot 10^{-9}$

$$Xcp(fvc) := \frac{1}{2 \cdot fvc \cdot Cp}$$ impedance of Cp

$$Xc(fvc) := \frac{1}{2 \cdot fvc \cdot C}$$ impedance of output capacitor

This is slightly smaller than the theoretical value however there is no noticable 100Hz ripple in the control signals on the prototype.

The system must be able to compensate the total external load variation through the error amp output response (ΔVvea). The power gain transfer function (Gpw) can be written as:

$$Gpw = Io \cdot \frac{Xc}{\Delta Vvea}$$ where Io is the load current and Xc is the output capacitor impedance.

The total load variation can be considered as:

$$Gpw(fvc) := \frac{(Po \cdot Xc(fvc))}{Vo \cdot \Delta Vvea}$$

The gain of the voltage loop is the product of Gpw and Gea

$$Gloop(fvc) := \frac{(Pin \cdot Xc(fvc) \cdot Xcp(fvc))}{\Delta Vvea \cdot Vo \cdot R1}$$

Note that this transfer function contains two poles at the origin 1/sC and 1/sCp. This could cause a stability problem. To avoid this a resistor (Rp) is added in parallel with Cp to move the voltage compensator pole to 1/(sCpRp).

The cross-over frequency (fvc) can be calculated by setting Gloop =1 and solving for fvc.

$$fvc := \sqrt{\frac{Po}{Vo \cdot \Delta Vvea \cdot R1 \cdot C \cdot Cp \cdot (2 \cdot \pi)^2}} \qquad fvc = 10.51 \qquad \text{cross-over frequeuncy}$$

to allow the highest DC gain while maintaining a phase margin of at least 22 degrees Rp is chosen as:

$$Rp := \frac{2.75}{2 \cdot \pi \cdot fvc \cdot Cp}$$

$$Rp = 8.861 \cdot 10^4$$

SELECT $\quad Rp := 12 \cdot 10^4$

The output voltage is set by the voltage divider circuit created by R1 and R2. Since the value of R1 is already selected R2 is chosen to give the desired output voltage.

Guess $\quad R2 := 10 \cdot 10^3$

Given $\quad \frac{R2}{R1 + R2} = \frac{5.1}{Vo} \qquad Find(R2) = 6.139 \cdot 10^3$

SELECT $\quad R2 := 5.7 \cdot 10^3$

In practice it is best to determine R2 by adjusting the value manually until the desired bus voltage is obtained. The value of R2 has no effect on the ac characteristics of the voltage compensation network. R2 is only used to set the DC bus voltage.

Discussion of the design consideration and results

(1) about the feedforward loop design

The feedforward loop design is a trade-off between quick converter responsce and low current distortation. The crossover frequency can only designed high below 120Hz so the 2nd harmonic will have little influence to the current reference and the input current distortation will be small. We select a two stage filter to increase the respense time and achieve a high attenuation of 2nd harmonic.

Fig 2 shows the designed feedforward filter has about 18Hz crossover frequency, and the attenuation of 2nd harmonic is below 1.5%. It can satisfy the requiment.

(2) about the current loop design

The design is based upon an intuitive time domain analysis given in the Unitrode application note for the UC3854 PFC controller and the ST application not for the L4981A PFC controller.

(3) about the voltage loop design

The voltage loop design procedure is based upon an intuitive time domain analysis given in the Unitrode appication note for the UC3854 PFC controller and the ST application note for the L4981A PFC controller. This analysis is mainly based on suppression of the 100Hz ripple in the boost output voltage.

In the previous file a low frequency model of the boost stage is used to perform classical voltage loop compensation. However this low frequency model is not so clear because the output voltage, input voltage and current cannot be considered constants. Therefore it is theoretically impossible to linearize the system and have an accurate power stage model. This is always a difficulty when modelling any single phase PFC circuit.

Appendix 2

A.2 SABER Models

A.2.1 Switching Model

The switching model has been implemented in SABER and incorporates many features of the actual circuit. To simulate four or five line cycles typically requires sixteen to twenty minutes on a Pentium III. The model described in the following section is based on early optimization results and has a switching frequency of 40 kHz. Fig. A.2.1 displays the SABER switching model. The model is broken into several sections, which are described in the following text.

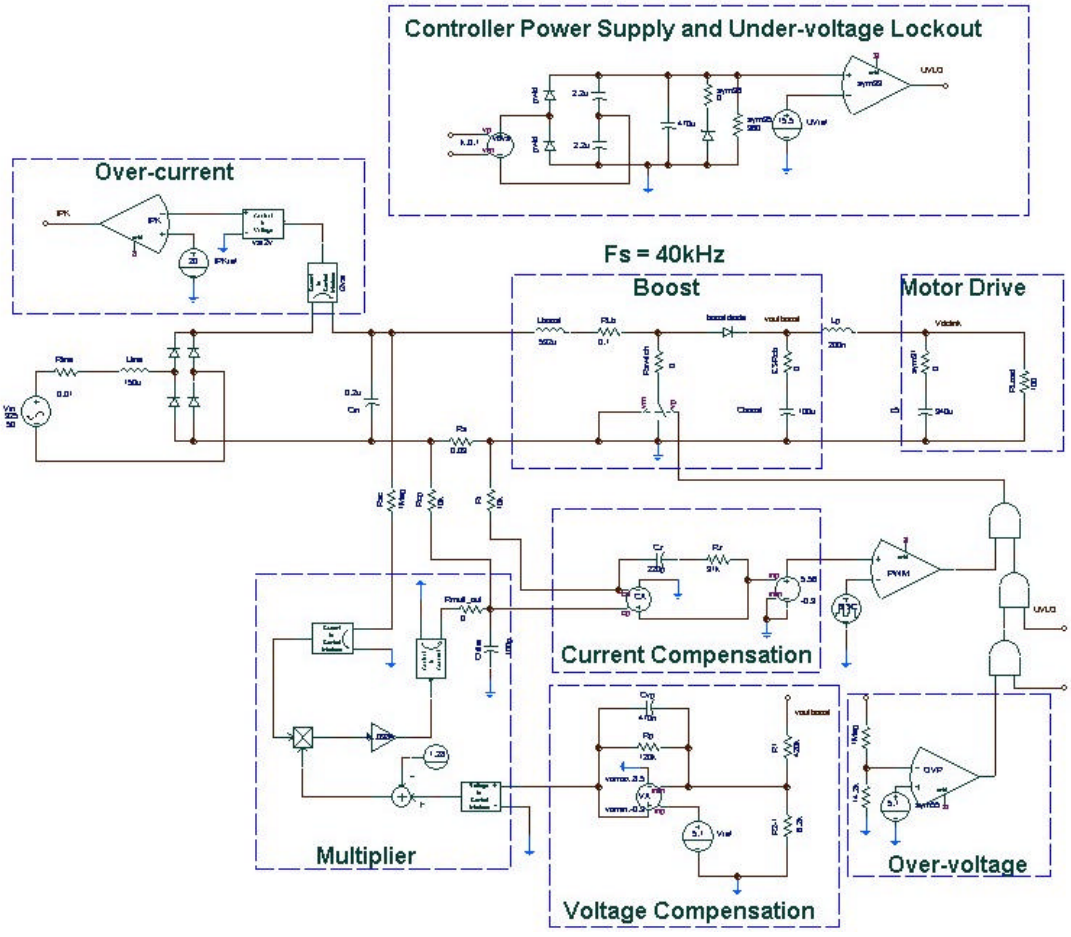


Fig. A.2.1. SABER Switching Model

A.2.1.1 Boost PFC Power Stage

The power stage is simply the classic single switch boost PFC topology. The components are listed below in Table A.2.1

Table A.2.1. Boost PFC Values

Component/Parameter	SABER Part
Rectifier diode	pwld
Input Capacitor	C – 0.2u
Boost Inductor	L – 532u
Switch	sw-vcsp
Fast diode	pwld
Output capacitor	C – 100u
Mains voltage	v_sin – 50 Hz
Mains Inductance	L – 150u
Switching Frequency	40 kHz

A.2.1.2 Motor Drive

For this application, the PFC stage is used as a front end for a motor drive. Due to the fact that this is a retrofit, the load already includes a rectifier bridge followed by a significant bulk capacitance. Therefore, it seems appropriate to model the load as a large bulk capacitance in parallel with a resistor. Also the lead inductance between the PFC stage and the motor drive is modeled. Table A.2.2 lists the motor drive model.

Table A.2.2. Motor Drive Values

Component	SABER Part
Lead inductance (parasitic)	L – 200n
Bulk Capacitor	C – 940u
Load Resistor	R – 100 to inifinity

A.2.1.3 Current Compensation

The current compensation network allows the circuit to provide unity power factor. A proportional integral compensation is implemented with an amplifier and an RC network. The trans-resistance amplifier is modeled with a current controlled voltage source of very high gain. Limits are also imposed on the output to model saturation and duty cycle limit. Table A.2.3 describes the current compensation network.

Table A.2.3. Current Compensation Values

Component	SABER Part
Sensing Resistor	Rz.rz – 0.03
R cp	rz.rcp – 10k
Ri	rz.ri – 10k
Cz	c.cz – 220p
Rz	rz.rz – 91k
Current amp output	Vca_out - -0.3 to 5.56 V

A.2.2 Voltage Compensation

Integrator compensation is implemented with an amplifier and an RC network. The amplifier is modeled with a voltage controlled voltage source of very high gain. The saturation

of the amplifier is also modeled by specifying limits on the maximum and minimum output voltage of the amplifier. Table A.2.4 lists the components used in the voltage compensator.

Table A.2.4. Voltage Compensation Values

Component	SABER Part
Voltage divider	rz.R1 – 420k
Voltage divider	rz.R2 – 6.2k
Integrator	rz.Rp – 120k
Integrator	c.Cvp – 470n
Voltage amp output	Vva_out - -0.3 to 8.5 V

A.2.2.1 Multiplier Circuit

The multiplier network is the most important part of PFC control. Without the multiplier the PFC circuit would not work. Since the final design does not implement a feedforward loop the multiplier can be modeled by a multiplication of the current and voltage reference signals multiplied by a constant gain. The values in the multiplier circuitry are chosen from the data sheet of the L4981A. Table A.2.5 lists these values.

Table A.2.5. Multiplier Values

Component	SABER Part
Voltage drop	Vva_out – 1.28 V
Current Reference Resistor	rz.Rac – 1 Meg
Gain	0.0384

A.2.2.2 Over-voltage

The over-voltage protection is designed to disable the boost switch whenever the output voltage rises above a specified value. Therefore, during an over-voltage condition, the converter shorts the input rectified voltage to the output node. This network is implemented with a

comparator, voltage reference, voltage divider, and logic gates. For the 40 kHz design, the over-voltage protection is designed to activate when the output voltage exceeds 365 V. This can easily be adjusted by changing rz.sym56. Table A.2.6 lists the values for these components.

Table A.2.6. Over-voltage Values

Component	SABER Part
Voltage divider	rz.sym58 – 1 Meg
Voltage divider	rz.sym56 – 14.2k
Voltage Reference	v_dc – 5.1
Comparator	comp_14 – delay: 1us, hysteresis: 250mV

A.2.2.3 Over-current

The over-current circuit is implemented by directly sensing the input current through a control block. The sensed current is then compared to a reference with a comparator. The over-current protection is designed to activate when the input current exceeds 20 A. This can easily be adjusted by changing the current reference. Table A.2.7 lists the values for this network.

Table A.2.7. Over-current Values

Component	SABER Part
Current Reference	v_dc - 20 A
Comparator	comp_14 – delay: 1us, hysteresis: 1A

A.2.2.4 Control Power Supply and Under-voltage Lockout

The auxiliary power supply is implemented with a voltage controller voltage source, which represents the auxiliary winding on the boost inductor. The voltage source then supplies a voltage doubler circuit that has a zener diode on the output to protect V_{CC} from voltage spikes. The under-voltage lockout is modeled with a simple comparator and a reference. The under-voltage lockout is designed to activate whenever the voltage at node Vcc falls below 15.5 volts.

This value can be adjusted by changing the value of the UVLO reference. Table A.2.8 lists the values for all components.

Table A.2.8. Control Power Supply and Under-voltage Lockout Values

Component	**SABER Part**
Voltage controlled voltage source	vcvs – gain: 0.1
Zener diode	zd – vzt: 18V
Comparator	comp_14 – delay: 1us, hysteresis: 2.25V
UVLO Reference	v_dc – 15.5

A.2.3 Average Model

The average model is implemented in SABER to provide a fast way to evaluate the average behavior of the converter under certain conditions. Fig. A.2.2 displays the average model schematic. The control loops, input mains, and load are identical to the switching model. A SABER block is used to implement the average model of the power stage. Fig. A.2.3 shows the parameters used in this SABER part (note that this is a 35 kHz design).

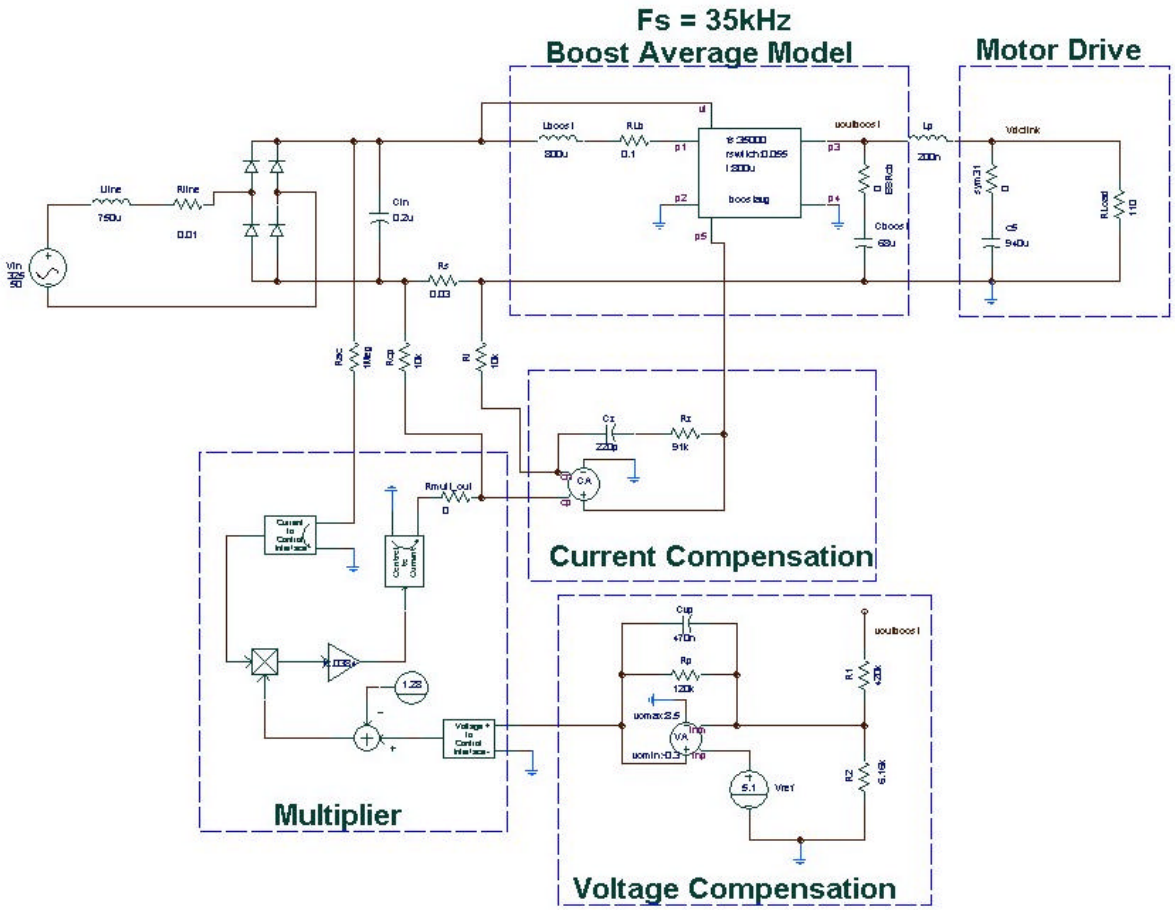


Fig. A.2.2. Average Model

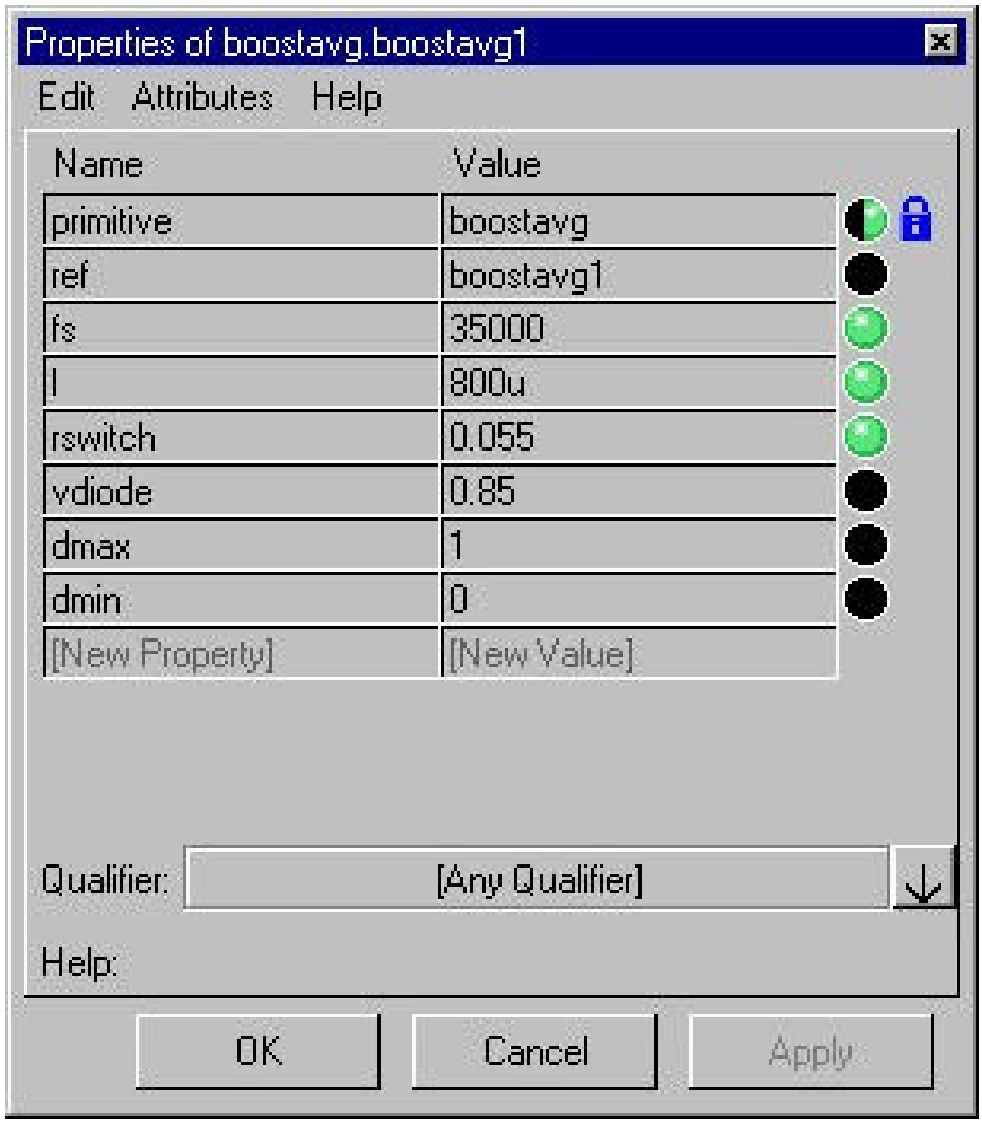


Fig. A.2.3. Parameters for the Average Model

A.2.4 EMI Model

The EMI model includes all the parasitics measured in Chapter Three. Otherwise the basic model is the same as the switching model. To make convergence more likely, the SABER ground node is used on the DC minus and for references in the control. Using the ground node for chassis ground and then floating the DC minus normally resulted in non-convergence in the transient analysis. Fig. A.2.4 shows the schematic of the circuit. It is also important to note that the voltage loop is open. The initial condition on the boost output capacitor is set to its steady-state value and the voltage reference to the multiplier corresponds with that value. This results in

the simulation starting immediately in steady-state. This is very beneficial because the FFT analysis must be done with a fixed step size to guarantee the proper resolution. It is possible to run a variable step transient analysis and then use that end point file as the initial point file for a succeeding fixed step analysis. However, normally this model does not converge unless the transient analysis is fixed step or a tightly controlled variable step.

The LISN schematic is shown in Fig. A.2.5. Note that the 50 Ω termination must be made outside the LISN. The noise separator is shown in Fig. A.2.6. It is important that the separator measurements are made with respect to the chassis ground. (In other words, the same ground as the LISN.) The input of the boost PFC stage has a large 100 Hz voltage applied to it. Since the chassis is floating, the CM coupling also causes the chassis to also float with a large 100 Hz signal. In the real hardware the DC plus and minus would float while the chassis remains true ground. In this case the 100 Hz signal must be subtracted out of the CM measurement to give accurate results.

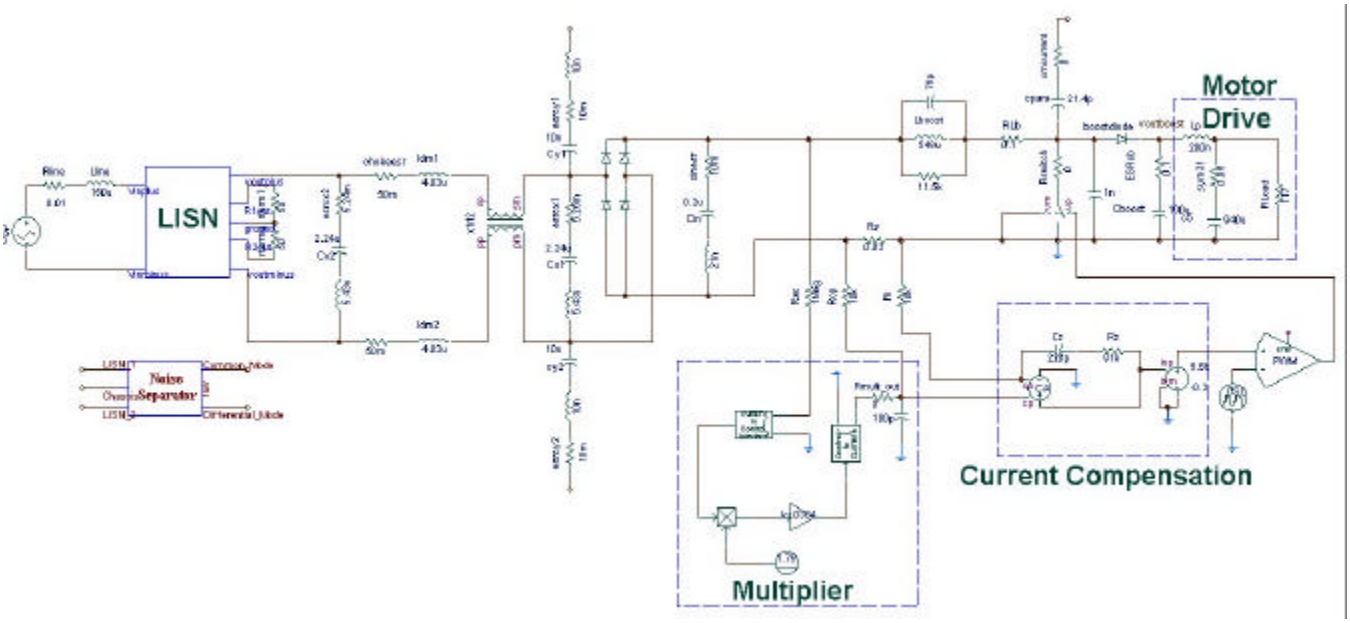


Fig. A.2.4. SABER EMI Schematic

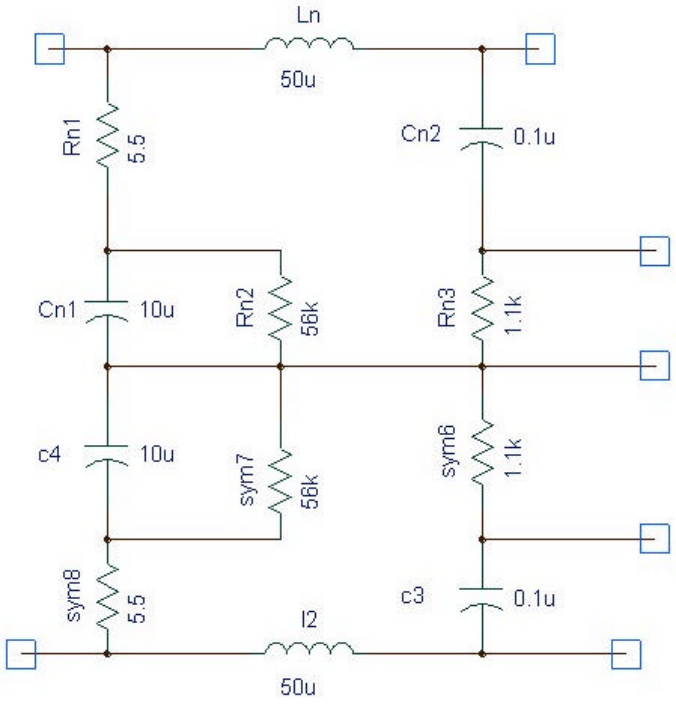


Fig. A.2.5. LISN Schematic

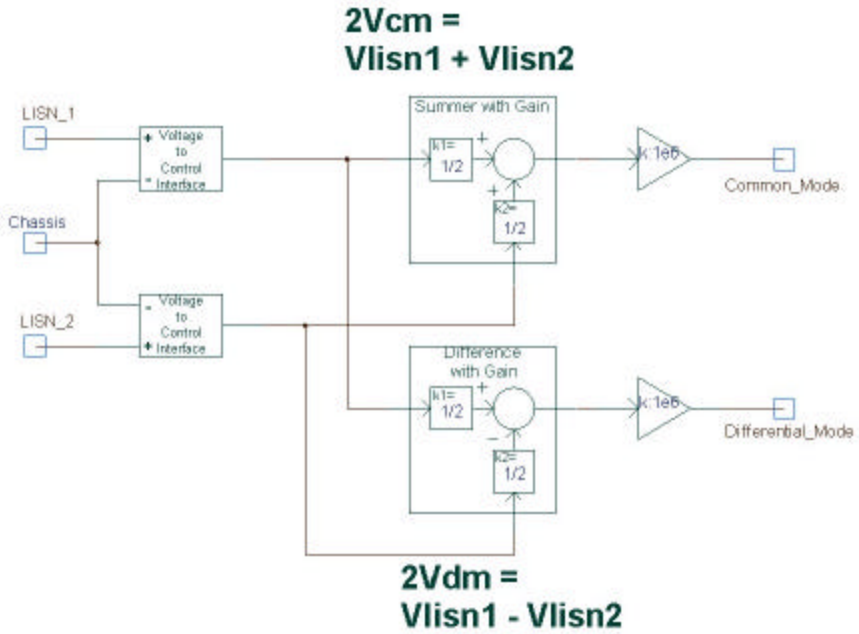


Fig. A.2.6. Noise Separator Schematic

As mentioned before, the FFT must be taken using a fixed time step in order to ensure the proper RBW. If the RBW of the simulation does not match the hardware test then none of the results can be compared. Fig. A.2.7 shows an example FFT input. The general relationships are given below and an example

$$BW = 1/T_{step}$$

Where BW is the maximum frequency of interest and T_{step} is the step size of the transient analysis

$$BW/RBW = \#FFT$$

Where RBW is the resolution bandwidth and #FFT is the number of points calculated by the FFT

$$\#Trans = \#FFT$$

where #Trans is the number of points from the transient analysis

$$T_{period} = \#Trans * T_{step}$$

Where T_{period} is the part of the transient waveform that we want to run the FFT on

EXAMPLE

Maximum frequency = 30 MHz yields: $T_{step} = 33.3$ ns

RBW = 10 kHz yields: #FFT = 3000

but SABER requires that the number of FFT points be a power of 2 therefore

$$\#FFT = 2^{12}$$

$$\#Trans = 4096$$

$$T_{period} = 136\ \mu s$$

If we want to center around 2.5ms

Time Data Start = 2.43ms

Time Data Stop = 2.57ms

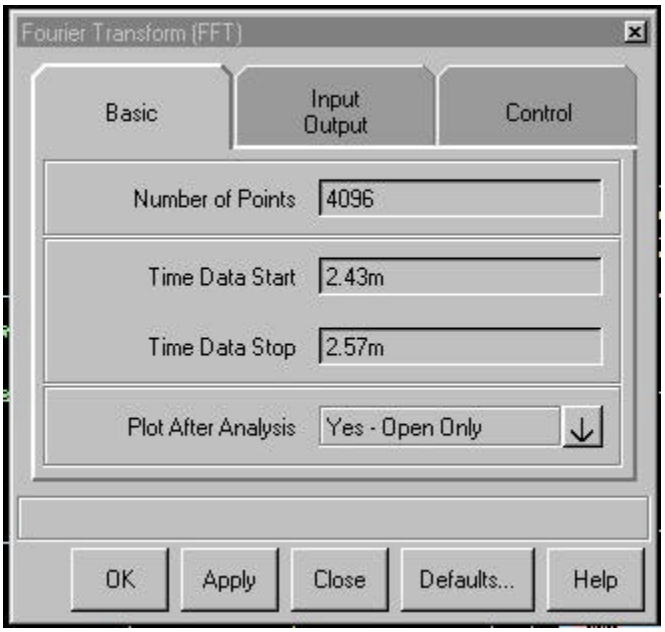


Fig. A.2.7. FFT Example

Using the above method guarantees a proper RBW in the FFT analysis. The RBW can be checked by looking at the FFT waveform. If the RBW is supposed to be 10 kHz then the FFT waveform should look flat up until 10 kHz.

Appendix 3

A.3 Layout

A.3.1 CPES Prototype

Layout has a large impact on the thermal and EMI behavior of any electronic circuit. The following pictures detail the layout for the converter tested in Chapter Four.

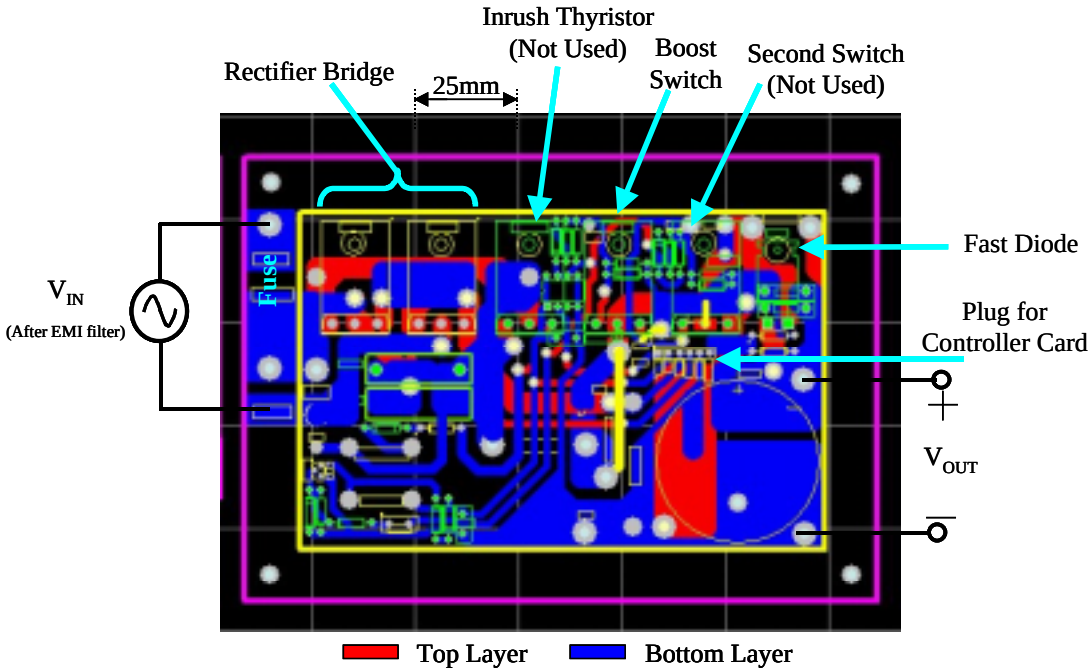


Fig. A.3.1. Boost PFC Power Stage looking from the Bottom

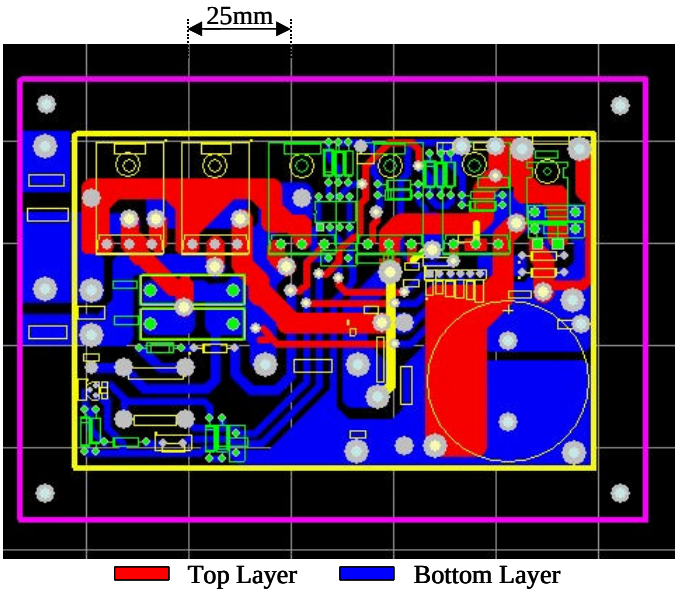


Fig. A.3.2. Boost PFC Power Stage looking from the Top

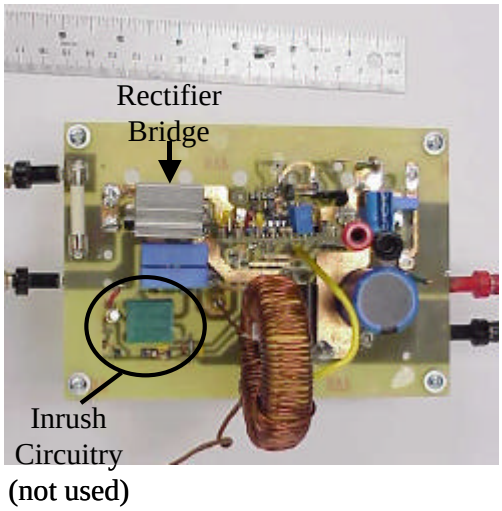


Fig. A.3.3. Boost PFC Power Stage Hardware

Note that Fig. A.3.3 shows that for the testing, the bridge rectifier is mounted on the top of the board. The original layout allowed for two TO-247 packages to be used as a bridge (see Fig. A.3.1), however results from the optimization process showed that the GBJ806B would be a better choice.

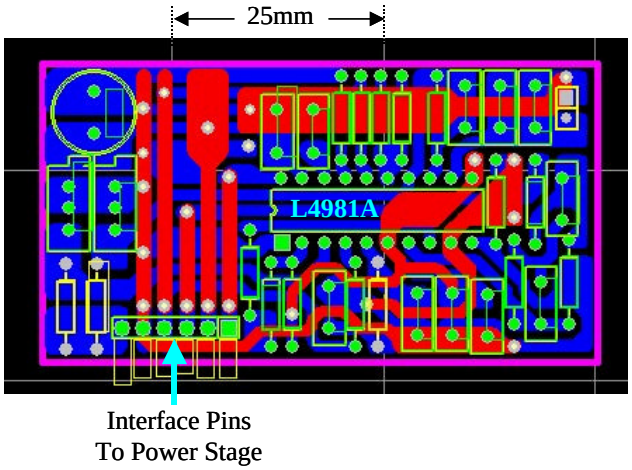


Fig. A.3.4. Control Card looking from the Top

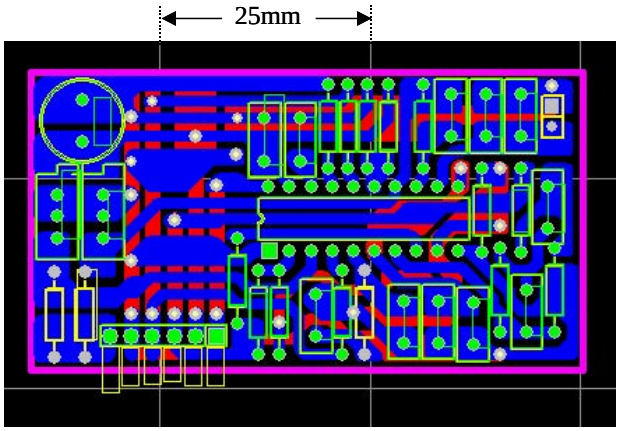


Fig. A.3.5. Control Card looking from the Bottom

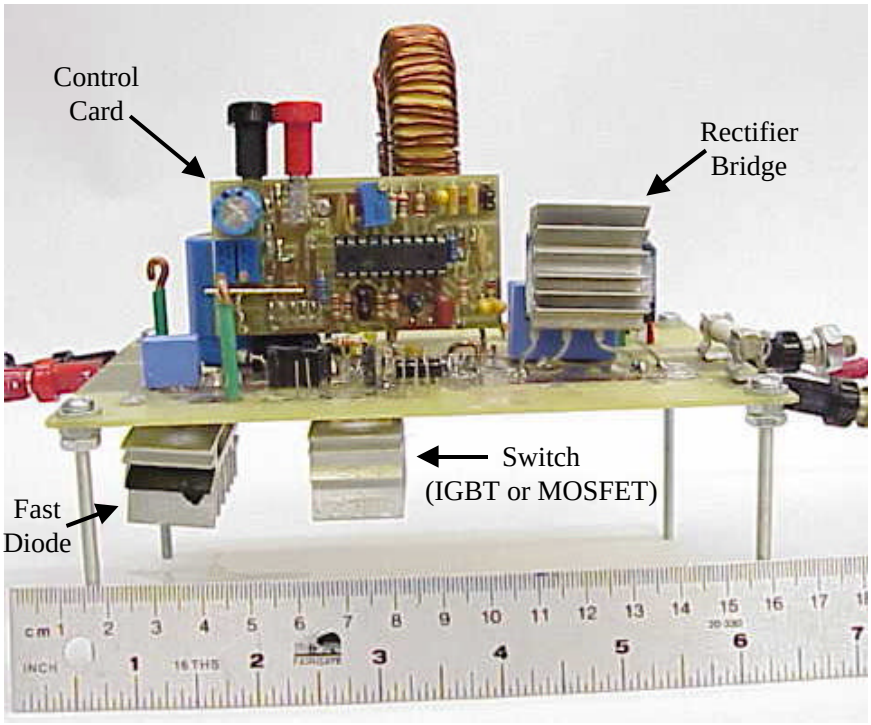


Fig. A.3.6. PFC Boost Power Stage

Fig. A.3.7. Fan Position and Airflow

Fig. A.3.7 shows that only the switch and diode are forced air-cooled. In the final prototype (not tested in Chapter Four) the layout was changed so that the inductor and rectifier bridge were also cooled by the fan. For the EMI testing the converter was placed directly on the ground plane with the four metal screws shown in Fig. A.3.6 acting as stand-offs.

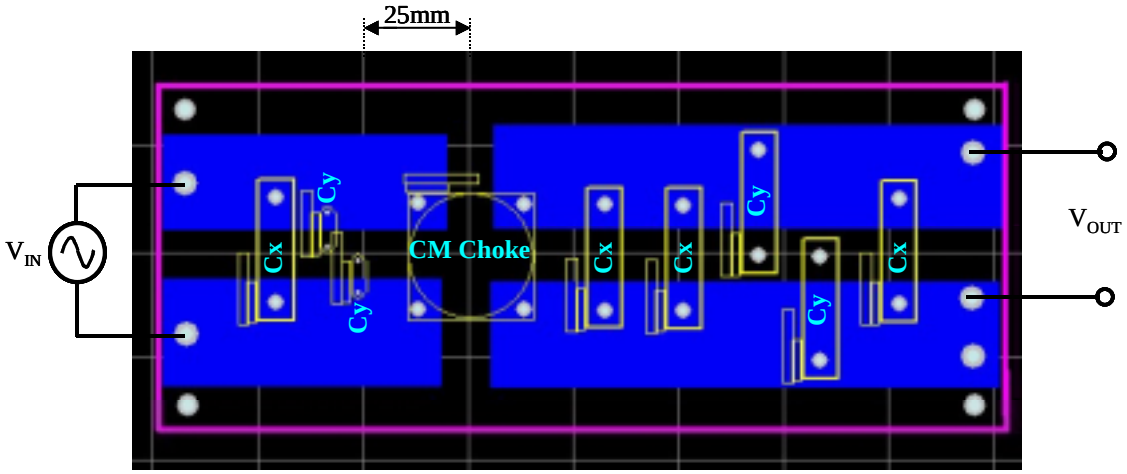


Fig. A.3.8. EMI Filter Bottom Layer

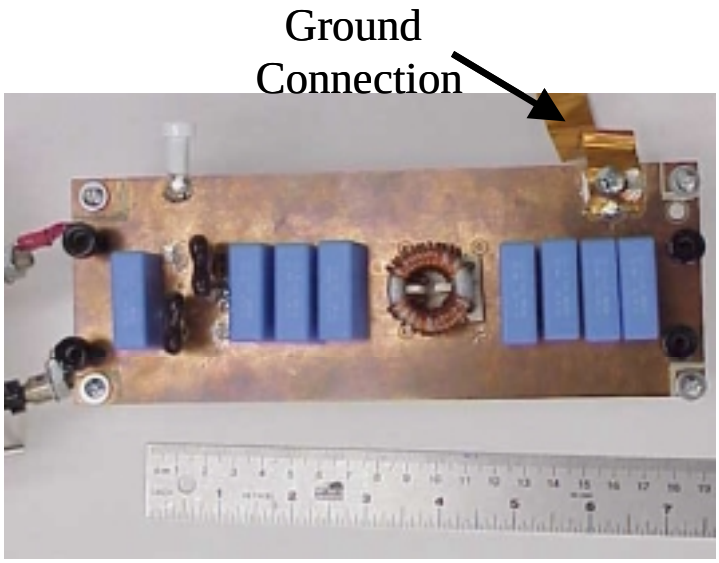


Fig. A.3.9. EMI Filter Hardware

The entire top layer of the EMI filter has been used a ground plane (see Fig. A.3.9). Ideally, the EMI filter should be symmetric so as not to induce any differential mode noise.

Appendix Four

A.4 Thermal Test Data

A.4.1 35 kHz Prototype

Table A.5.1 lists the results of the thermal testing on the converter shown in Fig. A.4.1. The components used are listed in General Hardware in the table. Any modifications to the General Hardware are listed in the right hand column marked Comments. The following is a description of each of the quantities measured in Table A.4.1. Note that this is the same design that is listed in Table 4.1 in Chapter Four and Table 5.3 in Chapter Five.

Vin: input voltage into the EMI filter (Vrms)

Ptot_Lb: power dissipation in the inductor (W)

Fline: line frequency of the input voltage (Hz)

T_coreLb: surface temperature of the core (ºC)

Po: output power of the system. (W)

Ths/case_sw: inside temperature of the switch heat sink (ºC)

Vo: output voltage of the systems (Vdc)

Ths/case_fd: inside temperature of the fast diode heat sink (ºC)

Io: output current into the load (Idc)

Ths/case_rd: inside temp. of the rectifier bridge heat sink (ºC)

Pin: **i**nput power to the system (W)

Ths/case_ad: inside temp. of the anti-parallel diode heat sink (ºC)

Iin_rms: **i**nput current to the system (Irms)

TwndngLB: surface temp. of the boost inductor winding (ºC)

Eff.: efficiency of the whole system calculated by dividing Po by Pin (%)

TwndngInChoke: surface temperature of the input EMI filter CM choke windings (ºC)

ILb_pk: **t**he peak instantaneous value of the current through the inductor during the line cycle (A)

TwndngOutChoke: surface temperature of the output EMI filter CM choke windings (in the drive) (ºC)

dILbmax: the maximum current ripple through the inductor during the line cycle (A)

Tamb: temperature of the wall next to the test set-up (ºC)

Rise Time: time required for the switch voltage to reach the bus votage at the point in the line cycle where the ripple is highest (10%-90% criteria) (ns)

delta_t: The amount of time the switch is on at the point of maximum current ripple (us)

Lb_min: the lowest inductance during the line cycle calculated by sqrt(2)*Vin*delta_t/dILbmax (μH)

Fall Time: time required for the switch voltage to reach vce_sat at the point in the line cycle where the ripple is highest (10%-90% criteria) (ns)

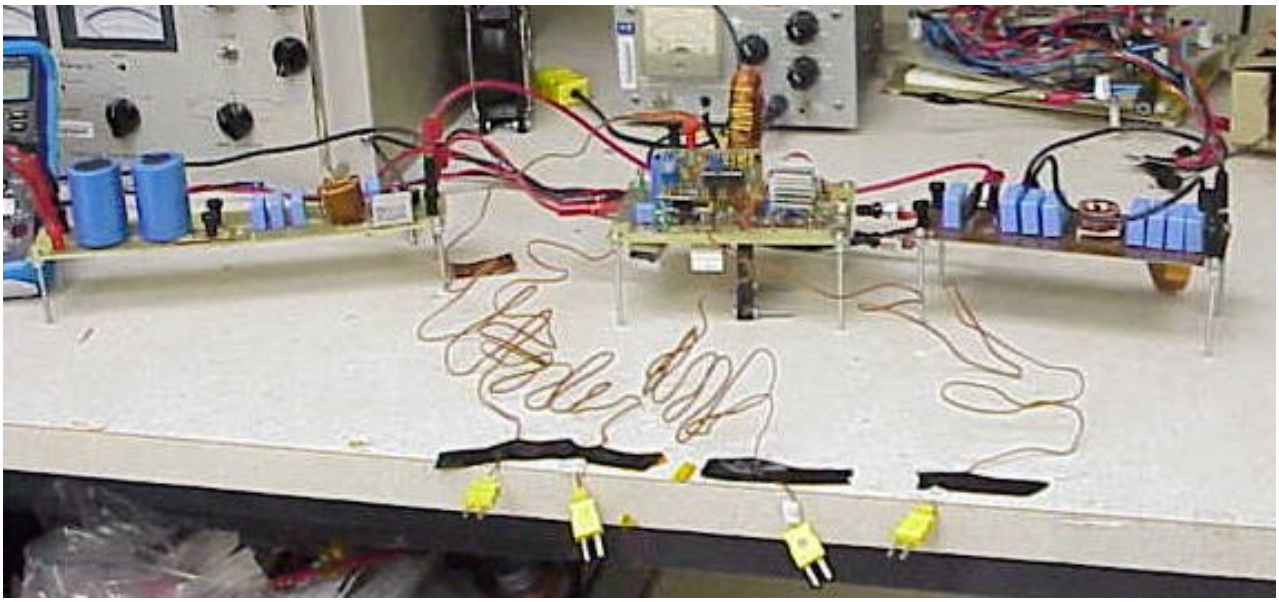


Fig. A.4.1. Thermal Testing Configuration

Table A.4.1. 35 kHz Design

CPES Prototype: Thermal Test Data

General Hardware	zwitch: IGBT #HGTP7N60A4, anti-parallel diode: BYM36C, Switch Heat Sink: 516F, Fast Diode: MUR1560, Fast Diode Heat Sink: 516F, Bridge Rectifier: GBJ806B, Bridge Rectifier Heat Sink: 516G, Core: T225-26, AWG: 16, Turns: 98, CM Choke: SDI142-21, Cx: 2.24uF @ 275V, Cy: 10nF @250V, Fs: 35kHz, Fan: MONS010B2-8, Load: Constant Current																								
Measurement Equipment		Power Analyzer								Lecroy Oscilloscope					Thermocouple					IR Gun							
Accuracy															0.1 °C					1 °C							
	Date	Vin	Fline	Pa	Va	Ia	Pin	Iin_rms	Eff.	iLb_pk	dILbmax	deltat(us)	Lb_min (uH)	Ptot_Lb	T_coreLb	Thrfcore_ru	Thrfcore_fd	Thrfcore_rd	Tcore_ad	T_undrqLb	T_undrqInChoke	T_undrqOutChoke	Tamb	Rise Time	Fall Time	Comments
Test #1-15-10	10/15/00	179.8	50	1155	369.1	3.13	1222	6.813	94.5	11.16	4.35	NA	636	NA	165.4	71	49.3	132.1	39	153	50	31	23			Using general hardware
	10/15/00	179.8	50	744	369.1	2.02	784	4.39	94.9	NA	3.2	10.2	811	NA	145.5	53	31	98	36	128	34	27	23			
	10/15/00	180	50	371	368.1	1.01	396	2.23	93.7	NA	2.14	9.58	1140	NA	124.3	40	31	64	31	109	26	24	23			
Test #2-15-10	10/15/00	180	50	1153	367	3.15	1220	6.8	94.5	12	4.7	9.65	523	NA	175	78	51	127	40	160	42	31	23			Modified Lb: T225-26 with **90** turns
	10/15/00	180	50	740	369	2	784	4.37	94.4	8.1	3.5	10.16	739	NA	153	59	40	94	35	136	32	27	23			
	10/15/00	180	50	375	370	1.02	401	2.26	93.5	4.7	2.5	10.55	1074	NA	135	49	31	62	32	119	26	24	23			
Test #3-16-10	10/16/00	180	50	1154	368.5	3.14	1234	6.87	93.5	12.76	5.83	10.17	444	28	199	76	49	131	41	186	51	31	23			Modified Lb: T225-26 with **75** turns
	10/16/00	180	50	739	368.3	2.01	788	4.41	93.8	8.6	4.24	10.43	626	22.4	178	60	39	95	36	165	36	27	23			
	10/16/00	180	50	374	369.2	1.02	407	2.29	91.9	4.92	3.3	10.61	818	19	162	50	31	63	33	151	27	24	23			
Test #4-16-10	10/16/00	180	50	1152	368.4	3.13	1216	6.78	94.7	11.6	3.28	10.25	795	20	151	70	50	132	41	135	48	31	23			Modified Lb: **T184-26** with **123** turns of **16** AWG wire.
	10/16/00	180	50	738	369.5	2	773	4.32	95.5	7.62	2.42	10.66	1121	12.8	127	52	39	95	37	112	34	27	23			
	10/16/00	180	50	367	368.6	1.01	385	2.17	95.3	4.01	1.35	10.25	1933	8.4	109	39	31	62	34	90	27	24	23			
Test #5-17-10	10/17/00	180	50	1149	367.4	3.13	1213	6.75	94.7	11.86	4.08	10.098	630	17.2	142	66	48	88*	39	150	47	31	23			Modified Lb: **T184-26** with **87** turns of **16** AWG wire.* Thrfcore_rd was measured with IR Gun
	10/17/00	180	50	739	368.9	2.01	779	4.35	94.9	7.84	2.89	10.115	891	14	128	52	38	64*	37	130	33	27	23			
	10/17/00	180	50	367	368.8	1.01	389	2.19	94.3	4.47	1.71	10.79	1606	9.8	110	38	30	46*	32	110	26	24	23			
Test #6-17-10	10/17/00	180	50	1151	368.4	3.13	1224	6.81	94.0	13.18	6.42	13.55	537	24	183	59	49	132	49	170	48	31	23			General Hardware with **Fs - 25kHz**
	10/17/00	180	50	739	369.5	2	784	4.38	94.3	8.66	4.64	13.9	763	20.4	161	47	38	96	44	148	34	27	24			
	10/17/00	180	50	368	368.4	1	394	2.22	93.4	5.01	2.94	13.88	1202	16.2	139	37	30	62	36	125	27	24	23			
Test #7-23-10	10/23/00	180	50	1152	368.5	3.13	1218	6.78	94.6	13.08	5.7	12.1	540	24.8	171	71	50	133	41	150	46	31	23			General Hardware with Fs - 30kHz
	10/23/00	180	50	742	369.3	2.01	785	4.38	94.5	8.94	4	11.95	760	19.2	151	52	39	98	36	138	33	27	23			
	10/23/00	180	50	370	369.5	1	396	2.23	93.4	4.79	2.67	11.73	1118	15.2	130	39	31	63	32	110	26	24	23			
Test #8-23-10	10/23/00	180	50	1152	368.4	3.13	1221	6.79	94.3	12	4.56	9.04	505	18	149	78	52	131	38	135	47	31	23			General Hardware with Fs-40kHz
	10/23/00	180	50	740	367.7	2.02	780	4.36	94.9	8.12	2.92	9.22	804	15.2	130	58	40	98	34	118	34	27	23			
	10/23/00	180	50	365	367.3	1	388	2.18	94.1	4.31	1.98	8.87	1140	11.6	112	42	31	62	34	100	27	24	23			
Test #9-24-10	10/24/00	180	50	1147	367	3.13	1219	6.79	94.1	11.72	3.96	7.75	498	11.2	140	87	53	131	39	120	70	32	23			General Hardware with Fs-45kHz
	10/24/00	180	50	740	368.2	2.01	782	4.37	94.6	8.16	2.67	8.25	787	9.6	121	60	41	98	34	110	46	27	23			
	10/24/00	180	50	367	367.7	1	390	2.2	94.1	4.28	1.82	8.04	1125	9.6	105	44	31	63	33	96	31	24	23			
Test #10-25-10	10/25/00	180	50	1156	367.7	3.15	1215	6.81	95.1	11.72	3.56	7.01	501	11.6	140	90	53	132	38	125	58	31	23			General Harware with Fs-50kHz
	10/25/00	180	50	736	368.4	2	777	4.34	94.7	7.88	2.46	7.29	754	10	117	63	41	97	33	100	38	27	23			
	10/25/00	180	50	371	368.9	1	393	2.2	94.4	4.26	1.69	7.22	1088	9	100	42	32	63	31	90	28	24	23			
Test #11-25-10	10/25/00	180	50	1156	368.7	3.14	1230	6.85	94.0	11.48	3.08	7.44	615	14.8	131	100	55	131	39	119	46	32	23			General Hardware with Fs-55kHz
	10/25/00	180	50	740	368.3	2.02	778	4.35	95.1	7.74	2.21	6.71	773	10.6	112	64	42	96	36	100	32	27	23			
	10/25/00	180	50	370	368	1.02	392	2.21	94.4	4.13	1.59	6.24	999	9.1	95	46	32	62	31	85	26	24	23			
Test #12-25-10	10/25/00	180	50	1152	368.5	3.13	1220	6.81	94.4	10.9	2.92	5.94	518	15.6	123	105	57	128	38	110	44	32	23			General Hardware with Fs-60kHz
	10/25/00	180	50	740	368.1	2.02	780	4.36	94.9	7.2	2.17	6	704	11.2	106	68	42	98	34	95	32	27	23			
	10/25/00	180	50	369	367.4	1.01	390	2.2	94.5	3.97	1.43	5.93	1056	9	93	48	42	62	31	83	26	24	23			
Test #13-20-12	12/20/00	180	50	1147	367	3.13	1211	6.75	94.7	12.3	4.96	9.97	512	21.6	161	75	53	132	41	130	42	33	23	45ns	70ns	General Hardware with Rg - 10 ohms
	12/20/00	180	50	739	369	2.01	781	4.36	94.6	8.3	3.6	10.17	719	11.8	143	58	42	101	39	120	32	29	23	34.5	41.5	
	12/20/00	180	50	376	369	1.02	401	2.25	93.8	4.42	2.2	9.55	1105	14.2	123	45	33	66	33	110	27	26	22	45.5	45	
Test #14-21-12	12/21/00	180	50	1152	368	3.13	1218	6.79	94.6	11.8	4.88	10.81	564	17	161	78	55	132	37	140	47	32	22	47	65	General Hardware with Rg - 33 ohms
	12/21/00	180	50	740	367	2.02	782	4.36	94.6	7.84	3.3	10.3	795	12.6	140	59	43	98	32	125	34	28	22	60	56	
	12/21/00	180	50	371	369	1.01	395	2.22	93.9	4.4	2.32	9.92	1088	11.7	123	44	33	65	32	105	27	26	22	51.5	54.5	
Test #15-21-12	12/21/00	180	50	1151	367	3.13	1221	6.8	94.3	11.9	4.92	9.99	517	15.6	161	86	57	134	39	144	46	32	22	67.5	72	General Hardware with Rg - 75 ohms
	12/21/00	180	50	738	368	2	781	4.36	94.5	7.74	3.26	9.75	761	12.8	139	59	44	100	34	128	34	29	22	61.5	67	
	12/21/00	180	50	371	368	1.01	396	2.22	93.7	4.38	2.19	9.44	1097	11.2	122	41	33	66	31	110	27	26	22	51	84.5	
Test #16-23-01	1/23/01	180	50	1147	367.6	3.13	1213	6.76	94.6	11.9	4.74	9.58	514	18	160	91	56	130	37	144	44	32	22	40.5	46.5	General Hardware with Rg - 20 ohms
	1/23/01	180	50	737	368	2	779	4.35	94.6	7.88	3.28	9.92	770	13.2	141	63	43	97	33	129	33	27	22	47	39.5	
	1/23/01	180	50	363	367.5	0.99	387	2.18	93.8	4.33	NA	NA	NA	11.4	123	43	33	64	35	112	27	26	22	NA	NA	
Test #17-24-01	1/24/01	180	50	1150	368	3.13	1217	6.78	94.5	12.1	5.06	9.36	471	21.6	166	85	59	133	39	151	49	32	22	43	42.5	Modified Lb: T225-26 with **95** turns
Test #18-14-01	1/24/01	180	50	1150	368	3.13	1220	6.8	94.3	12.4	5.7	10.39	464	28.8	179	78	56	134	38	164	47	33	23	47	41.5	Modified Lb: T225-26 with **85** turns
Test #19-24-01	1/24/01	180	50	1155	368.7	3.13	1228	6.8	94.1	12.5	5.84	10.17	443	23.2	187	78	58	137	40	165	46	33	23	39.5	38	Modified Lb: T225-26 with **80** turns

A.4.2 43 kHz Prototype

The final layout is shown in Fig. A.4.2. Thermal test results from this layout are listed in Table A.4.2. Note that this is the same design as the one listed in Table 5.2 in Chapter Five. Although that prototype is listed at 45 kHz the various control IC and component tolerances resulted in the actual switching frequency being 43 kHz.

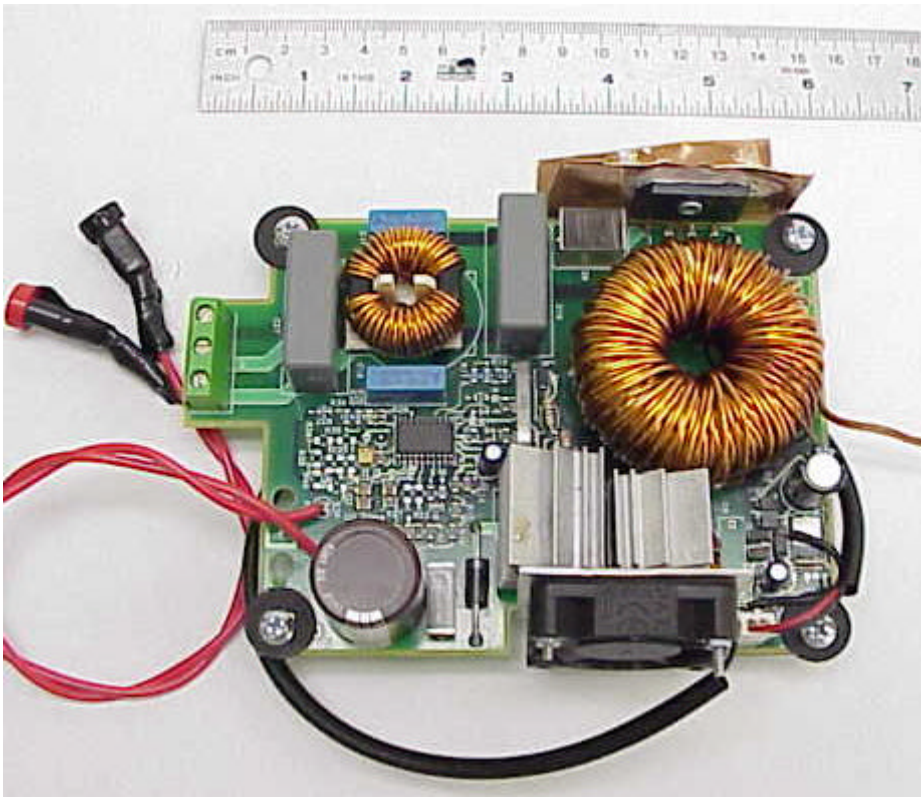


Fig. A.4.2. Final Layout

Table A.4.2. 43 kHz Design (using T184-26 core)

General Hardware	switch: IGBT $HGTP7N60A4, anti-parallel diode: BYM36C, Switch Heat Sink: 516G, Fast Diode: MUR1560, Fast Diode Heat Sink: 516F, Bridge Rectifier: FBI 8J15M1, Bridge Rectifier Heat Sink: 516G, Core: T-26, AWG: 16, Turns: 23, CM Choke: SDI1442-21, Cx: 1.0uF @ 275V, Cy: 10nF @ 250V, Fs: 43kHz, Fan: Sunon KDE1204PFB2-8 Load: Constant Current																												
Measurement Equipment					Power Analyzer							Lecroy Oscilloscope						Thermocouple					IR Gun						
Accuracy																		0.1C					1°C						
	Date	Vin	Fline	Po	Vo	Io	Pin	Iin_rms	Eff.	iLb_pk	dILbmax	delta t (us)	iLb_min (uH)	Ptot_Lb	T_coreLb	Thdcase_rw	Thdcase_fd	Thdcase_rd	Tcase_od	T_wndngLb	T_wndngInChoke	T_wndngOutChoke	Tamb	Comments						
Test #1-21-10	10/29/00	200	50	1156	355	3.26	1211	6.08	95.5	10.2*	1.89	5.78	864.38388	10	90	104	68	129	NA	NA	NA	NA	22	Converter is enclosed in a cardboard box. *The current limit was reached at full load with Vin=200.						
	10/29/00	200	50	717	357	2.01	749	3.76	95.7	6.31	1.2	5.74	1052.331	7.6	74	68	51	90	NA	NA	NA	27	23							
	10/29/00	200	50	353	353	1	375	1.9	95.6	3.25	0.66	5.31	2532.7279	5.75	60	47	38	57	NA	NA	NA	NA	23							
	10/29/00	230	50	1151	356	3.24	1193	5.22	96.5	8.88	0.95	2.73	334.72073	10.8	81	86	65	114	NA	NA	NA	31	23							
	10/29/00	230	50	171	357	2.01	744	3.25	23.0	5.45	0.83	3.03	1167.4282	7.6	65	61	48	81	NA	NA	NA	27	23							
	10/29/00	230	50	358	353	1	373	1.65	96.0	2.84	0.55	3.69	2182.2601	5.6	53	45	37	53	NA	NA	NA	24	23							

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Vita

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