IMPROVEMENTS IN INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS

by

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ABSTRACT

The integrated high-quality rectifier-regulators [1] are not practical for universal input-voltage and wide load range applications because of high bulk-capacitor voltage stress at lighter loads. This load dependent characteristic of the bulk-capacitor voltage is due to the integration of a discontinuous conduction mode boost converter and a continuous conduction mode dc-dc converter. In addition, this power factor correction technique suffers from high-voltage spike on the switch at turn-off. In this thesis, a variable frequency control, swinging choke and low loss LC snubber techniques are proposed to alleviate these problems. Finally, several experimental converters with different specifications are evaluated with respect to efficiency and ability to meet the IEC555-2 standards.

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1. INTRODUCTION

Utility / dc interfaces that draw nearly perfect sinusoidal current from the utility has been around for the past decades. The use of the low harmonic interface achieves power factor close to unity permits more power to be extracted from a wall outlet. Furthermore, government standards such as the IEC555-2 standards which will be enforced in the imminent future justifies the use of such low harmonic interface even in low power applications. However, the cost of the low harmonic interface appears to be high in part due to the high voltage and current ratings for which the converter's switches and filter elements must be rated. On the other hand, the interface itself as another converter stage adds considerable amount of cost to a power supply. This is significant especially to low power level power supplies such as those in personal computers and home electronics appliances.

One approach to deal with the voltage stress problem is to split the bulk (dc bus) capacitor to form a mid-point. Then, the switch of the boost converter will have only half of the stress of the full bus voltage, as described in [3]. But this approach has the penalty of interruption of the utility current flow when the utility voltage is lower than the mid-point voltage of the bulk capacitor. It also requires a charge removal circuit to remove the charge at the capacitor node. Another way to cut the cost and simplify the converter is to have a single-stage, single-switch converter. This can be achieved by using a boost converter which operates in discontinuous conduction mode (DCM) instead of the conventional way of employing an active controlled boost converter which operates in continuous conduction mode (CCM). The DCM boost converter is found to possess inherent power factor correction capability, as described in [2]. Therefore, there is no need to have active control over the boost converter in order to shape the input current to the desired sinusoidal waveforms as is done conventionally by using a multiplier. Hence, a dc-dc converter with isolation can be combined with this DCM boost converter. The resulting converter is an integrated high-quality rectifier-regulator which has inherent power factor correction and requires only a single switch, as described in [1].

However, the family of integrated high-quality rectifier-regulators suffers from high bulk-capacitor voltage stress at lighter loads. This represents a severe drawback in terms of

cost and size, and practically eliminates this technique from universal input voltage range and wide load range applications. In addition, this power factor correction technique suffers from high-voltage spike on the switch at turn-off. In this thesis, a novel variable-frequency control, swinging choke and LC snubber techniques are proposed to alleviate these problems.

The following chapter discusses the DCM boost converter with inherent power factor correction (PFC) based on [2]. It is then followed by a summary on the formations and operations of the integrated high-quality rectifier-regulators [1] in chapter 3. The discussion and evaluation specifically are focused on the flyback and forward versions of this type of converter. A simple algorithm accompanied by two numerical examples are suggested to illustrate the performance of this type of converters with respects to the IEC555-2 standards. The advantages and limitations of such a converter are also discussed in this chapter. The improvements are discussed in chapter 4. The variable frequency control, swinging choke and low loss LC snubber techniques are proposed to alleviate the problems of this type of converters. Design examples which employ the proposed techniques are given in chapter 5. Prototypes based on these examples are built and tested. The performance of the converters are improved by using the proposed methods. Finally, experimental results of the prototypes evaluated with respect to efficiencies and the ability to meet IEC555-2 standards are presented in chapter 6.

2. ACHIEVE POWER FACTOR CORRECTION BY EMPLOYING DCM BOOST CONVERTER.

2.1 INHERENT POWER FACTOR OF A DCM BOOST CONVERTER.

There are generally two ways to correct the power factor of a switch-mode power supply. One is to use passive element like an inductor to reduce the harmonic content of the line current and give good power factor. But the 60 Hertz line current requires a very large inductor rendering this method not practical at all with switch-mode power supplies. The other way is to use active control as mentioned in the introduction. A flyback or a boost converter can serve this purpose. However, the flyback converter usually has a higher loss and lower efficiency. The isolation it provides will not give more advantage because it only acts as an interface to shape the line current. It still needs a dc-dc converter to give a tight output voltage regulation. On the other hand, the boost converter which steps up the input voltage generally gives better efficiency. Thus, the boost converter is normally chosen to be the power factor correction interface. There are again two ways to operate the boost converter to achieve power factor correction. One is to operate it in continuous conduction mode. This requires a multiplier to sense the boost inductor current and the output voltage in order to control the shape of the line current to the desired sinusoidal form. This is more complex and cost more. Another way is to operate the boost converter in discontinuous conduction mode. In this mode, the boost inductor current will automatically follow the sinusoidal line voltage waveform without having active control over the shaping of the input line current as described in [2]. The voltage mode control loop which controls the switch on time is the only loop needed for a power factor better than 0.98.

A boost converter that operates in discontinuous conduction mode (DCM) is shown in Fig.2.1. In this circuit, the peak input voltage is V_{inpk}. Since the input voltage, $V_{in,}$ is sinusoidal, V_{in} can be expressed as a constant peak input voltage times a sine function with a certain period, as shown in equation (2.1). If the switch on time, $T_{on,}$ and the inductance L are constant over one line cycle, then the peak inductor current I_{pk} will follow the sinusoidal line voltage waveform naturally, as shown in equation (2.2). Where

T is the switching period and D is the duty ratio. The assumption is generally true, because the switching frequency is usually at least 50 K Hz and the AC line current cycle is only 100 or 120 Hz after passing through the full bridge rectifier. Thus, the modulation of the duty cycle will appear constant within one line cycle. So, D can be assumed constant. The resulting boost inductor current waveform in half a line cycle is shown in Fig. 2.2.

$$V_{in} = V_{inpk} \bullet \sin \varpi t \tag{2.1}$$

$$I_{pk} = \frac{(V_{in} \bullet T_{on})}{L} = \frac{(V_{inpk} \bullet \sin \varpi t \bullet D \bullet T)}{L} \tag{2.2}$$

2.2 HARMONICS DISTORTION DUE TO THE INDUCTOR CURRENT DISCHARGING TIME.

It should be noticed that the line current waveform of the DCM boost converter is not purely sinusoidal even though the peak inductor current follows the sinusoidal line voltage naturally, as explained in section 2.1. The input line current will contain harmonics distortions due to the inductor current discharging time of the boost converter, as described in [2]. This can be seen clearly from the averaged line current expression in equation (2.8). The averaged inductor current is obtained by averaging the boost converter inductor current during on and off time in one cycle as shown in the following equations which are derived in [2]

During the switch on time, T_{on}, the average inductor current, $I_{lon(ave)}$, is given by,

$$I_{on(ave)} = \frac{(I_{pk} \bullet T_{on})}{2T} \tag{2.3}$$

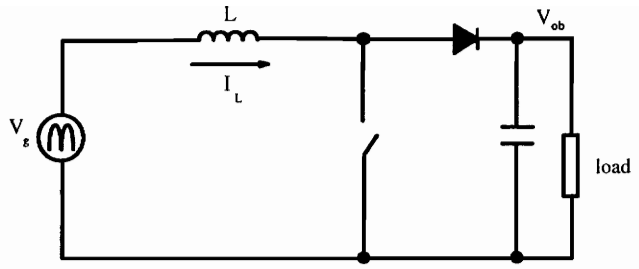

Fig.2.1 DCM boost with inherent PFC

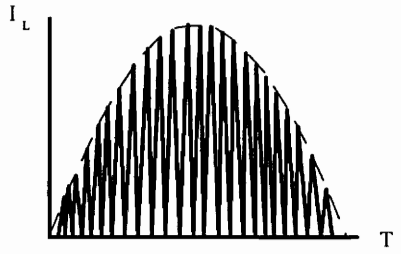

Fig.2.2 DCM boost peak inductor current follows the sinusoidal line voltage naturally.

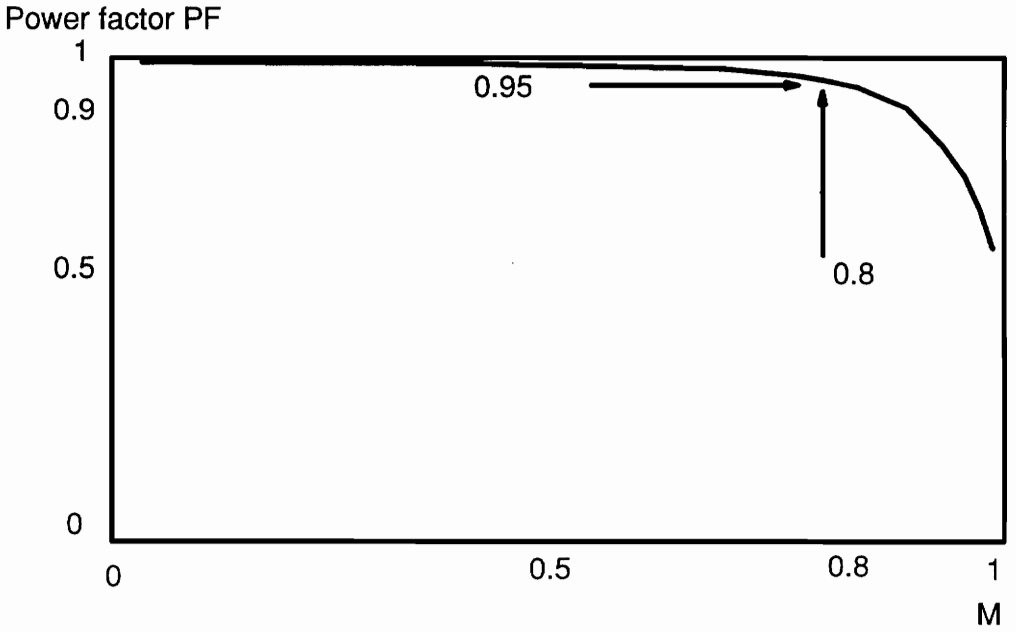

Fig. 2.3 Power factor as a function of M.

During the switch off time, T_{off}, the average inductor current $I_{loff(ave)}$ is given by,

$$I_{off(ave)} = \frac{(I_{pk} \bullet T_{off})}{2T} \tag{2.4}$$

Therefore, the averaged inductor current over one period is given by,

$$I_{in(ave)} = \frac{(I_{pk} \bullet T_{on})}{2T} + \frac{(I_{pk} \bullet T_{off})}{2T} \tag{2.5}$$

Since the peak inductor current during switch off time can be written as,

$$I_{pk} = \frac{(V_{ob} - V_{in}) \bullet T_{off}}{L} \tag{2.6}$$

Where V_{ob} is the output voltage of the boost converter stage. Therefore, T_{off} can be expressed as,

$$T_{off} = \frac{I_{pk} \bullet L}{(V_{ob} - V_{in})} \tag{2.7}$$

Substitute (2.2) and (2.7) into (2.5), the averaged input inductor current over one period can be expressed as,

$$I_{in(ave)} = \frac{V_{ob} \bullet D^2 \bullet T}{2L} \bullet \frac{\left(\frac{V_{inpk}}{V_{ob}} \bullet \sin \varpi t\right)}{\left(1 - \frac{V_{inpk}}{V_{ob}} \bullet \sin \varpi t\right)} \tag{2.8}$$

0r (2.8) becomes,

$$I_{in(ave)} = K \bullet \frac{(M \bullet \sin \varpi t)}{(1 - M \bullet \sin \varpi t)} \tag{2.9}$$

Where

$$K = \frac{V_{ob} \bullet D^2 \bullet T}{2L} \tag{2.10}$$

M is the inverse voltage gain of the boost converter and is given by,

$$M = \frac{V_{inpk}}{V_{ob}} \tag{2.11}$$

As shown in the equation (2.9), as M increases, distortions also increase. This is understandable, because the boost inductor gets closer to the continuous conduction mode boundary when M is larger. The inductor current will no longer follow the sinusoidal line voltage if it gets into continuos conduction mode. It is because the inductor current then will have a dc component which follows the load current instead.

2.3 POWER FACTOR AS A FUNCTION OF THE DCM BOOST CONVERTER INVERSE VOLTAGE GAIN M.

The power factor, PF, can be expressed as a function of the DCM boost converter inverse voltage gain M as described in [2]. Power factor is the ratio of the averaged power measured at the terminals to the product of the root means square (RMS) values of the terminal current and voltage as shown in equation (2.12). It can reflect how effectively the power is being used. So, if the boost inductor current (which is equal to the line current) is a function of M, the relationship between the power factor and M can be obtained for the DCM boost converter. The desired power factor can then be controlled by M. Whereas, M is determined by the DCM boost converter design. The relationship between the power factor and M is illustrated in the following derivations obtained from [2].

P_{in} is the average input power measured at the terminals. So, the definition of power factor, PF, is given by,

$$PF = \frac{P_{in}}{V_{rms} \bullet I_{rms}} \tag{2.12}$$

P_{in} can be expressed as,

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} V_{in} \bullet I_{in} \bullet d\varpi t \tag{2.13}$$

Substitute equations (2.2) and (2.9) into (2.13),

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} V_{inpk} \bullet \sin \varpi t \bullet K \bullet \frac{(M \bullet \sin \varpi t)}{(1 - M \bullet \sin \varpi t)} \bullet d\varpi t \tag{2.14}$$

The RMS power can be written as,

$$V_{rms} \bullet I_{rms} = \sqrt{\left(\frac{1}{\pi}\int_0^{\pi} {I_{in}}^2 \bullet d\varpi t\right)} \bullet \frac{V_{inpk}}{\sqrt{2}} \tag{2.15}$$

Substitute (2.9) into (2.15)

$$V_{rms} \bullet I_{rms} = \sqrt{\left(\frac{1}{\pi}\int_0^{\pi} \left(\frac{K \bullet M \bullet \sin \varpi\ t}{1 - M \bullet \sin \varpi\ t}\right)^2 \bullet d\varpi\ t\right)} \bullet \frac{V_{inpk}}{\sqrt{2}} \tag{2.16}$$

Let X be

$$X = \int_0^{\pi} \frac{\sin^2 \varpi t}{1 - M \bullet \sin \varpi t} \bullet d\varpi t \tag{2.17}$$

Expand (2.17) as, described in [2] and the mathematical tables in [10], X can be expressed as,

$$X = -\frac{2}{M} - \frac{\pi}{M^2} + \frac{2}{M^2\sqrt{1-M^2}} \bullet \left(\frac{\pi}{2} - tan^{-1}\left(\frac{-M}{\sqrt{1-M^2}} \right) \right) \tag{2.18}$$

Let Y be,

$$Y = \int_0^{\pi} \frac{sin^2 \varpi t}{(1 - M \bullet sin \varpi t)^2} \bullet d\varpi t \tag{2.19}$$

Expand (2.19) as described in [2] and the mathematical tables in [10], Y can be expressed as,

$$Y = \frac{2}{M \bullet (1-M^2)} + \frac{\pi}{M^2} + \frac{2 \bullet (2M^2 - 1)}{M^2 \bullet (1-M^2)^{\frac{5}{2}}} \bullet \left(\frac{\pi}{2} - tan^{-1}\left(\frac{-M}{\sqrt{1-M^2}} \right) \right) \tag{2.20}$$

Substitute (2.14) and (2.16) into (2.12), the power factor PF can be expressed as,

$$PF = \frac{\sqrt{2} \bullet X}{\sqrt{\pi \bullet Y}} \tag{2.21}$$

From the equations (2.18), (2.20) and (2.21), a curve showing the relationship between power factor, PF, and the inverse voltage gain, M, of the boost converter is plotted in Fig.2.3. It can be observed from Fig.2.3 that if M is less than 0.8, PF is better than 0.95. When M is larger than 0.9, PF decreases drastically.

2.4 SUMMARY

When the boost converter is operated in discontinuous conduction mode, the boost inductor line current will follow the sinusoidal line voltage naturally. Even though there

is some distortion in the line current due to the discharging time of the boost inductor, it is able to obtain a power factor better than 0.98.

3. THEORY OF OPERATION OF THE INTEGRATED HIGH-QUALITY RECTIFIR-REGULATORS.

3.1 THE INTEGRATION OF DCM BOOST CONVERTER AND FLYBACK CONVERTER.

As discussed in chapter two, a single-stage, single-switch converter can be obtained when a DCM boost converter is combined with a dc-dc converter. As long as the boost converter operates in DCM, the converter will have inherent power factor correction. This section gives a brief summary on the ways to develop such a single-stage, single-switch converter. The DCM boost converter alone cannot give isolation, a low output voltage, and energy storage capability. Thus, this circuit needs to have something more added to it. But this does not mean that it needs to have another stage. The followings present the way to convert a conventional two stages converter with power factor correction and isolation into a single-stage one. It needs to be recognized that the input boost converter stage must operate independently in the discontinuous conduction mode after the combination. It is needed in order to have the output voltage regulation and yet without affecting the power factor correction. Because only one switch alone is being used in this single-stage converter. This can be ensured by putting a diode right after the inductor as shown in Fig.3.1. The diodes of the full bridge can not be used because they are slow and only suitable for line frequency range. The integration steps of the DCM boost and CCM flyback converters are shown in Fig.3.1, Fig.3.2, and Fig.3.3.

Fig.3.1 shows the conventional way of putting the flyback converter behind the boost converter. The two switches shown in Fig.3.1 are reduced into one as illustrated in Fig.3.2. The switch of the boost converter is eliminated. As it is mentioned earlier that the boost inductor needs to be followed by a diode to ensure discontinuous conduction,

hence, the diode of the boost converter is preserved. Then, the connection between the boost converter diode and the bulk capacitor is broken. The loose end of the diode is attached to the switch of the dc-dc converter. The resulting circuit is a *B*oost converter *I*ntegrated with a *F*lyback *R*egulator/ *E*nergy storage *D*c-dc converter (BIFRED), as described in [1]. The BIFRED converter is shown in Fig.3.3.

There are three topological modes within one cycle of operation of the BIFRED converter. They are shown in Fig.3.4, Fig.3.5 and Fig.3.6.

In Fig.3.4, when the switch is turned on, the boost inductor is energized by the input voltage source, while the transformer is energized by the bulk capacitor. The bulk capacitor serves as the dc voltage source of the flyback converter. During this period of time, the load current is supplied by the filter capacitor as shown.

In Fig.3.5, when the switch is turned off, the boost inductor current charges the bulk capacitor. The output diode current is equal to the reflected inductor current plus the transformer's magnetizing current. This current supplies the load and charges the output capacitor as shown.

In Fig.3.6, the boost inductor current is depleted. The bulk capacitor voltage does not change any more. The output diode current becomes equal to the magnetizing current as shown.

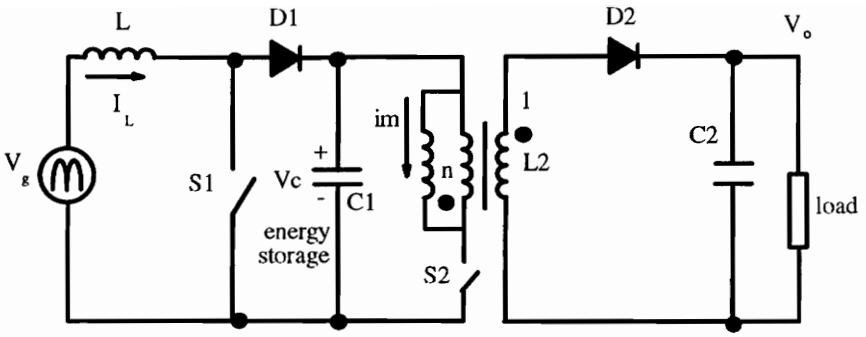

Fig.3.1 Cascaded boost and flyback converters.

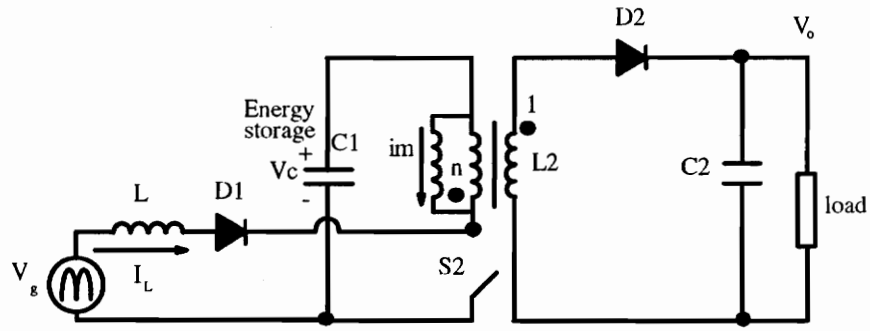

Fig.3.2 Combination of two switches into a single one.

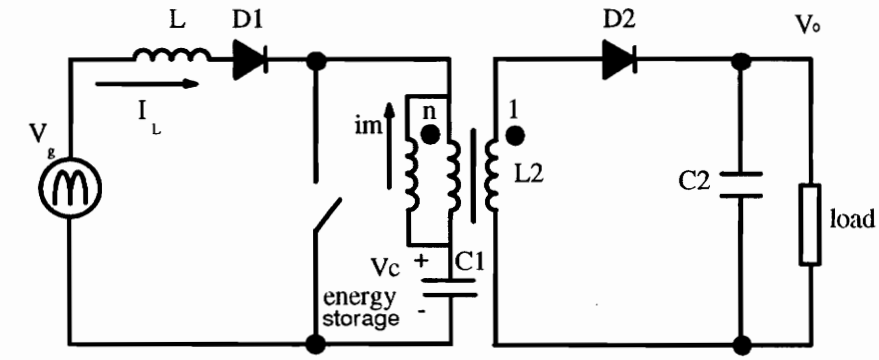

Fig.3.3 Boost integrated with a flyback regulator/ Energy storage dc-dc converter (BIFRED).

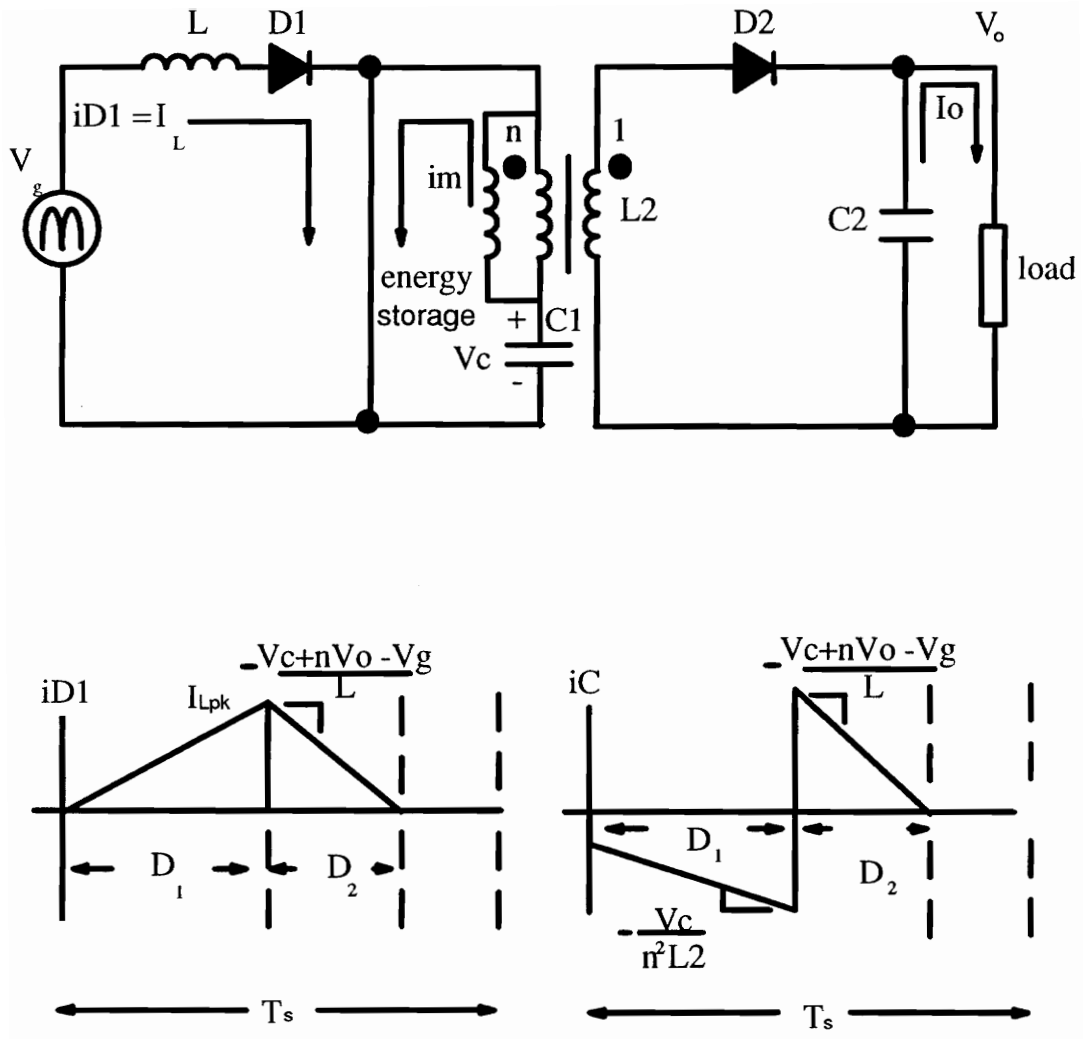

Fig.3.4 BIFRED operation and current waveforms during on time.

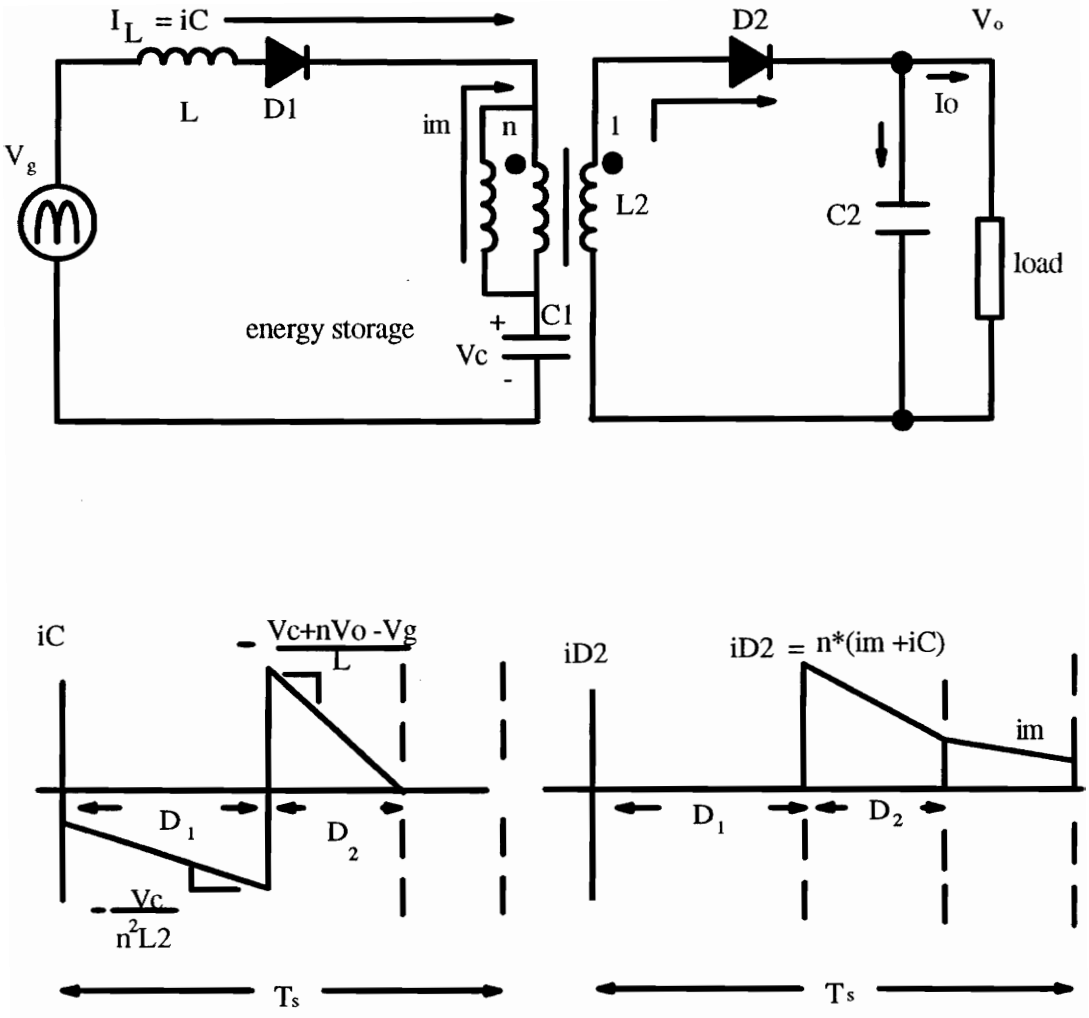

Fig.3.5 BIFRED operation and current waveforms during off time.

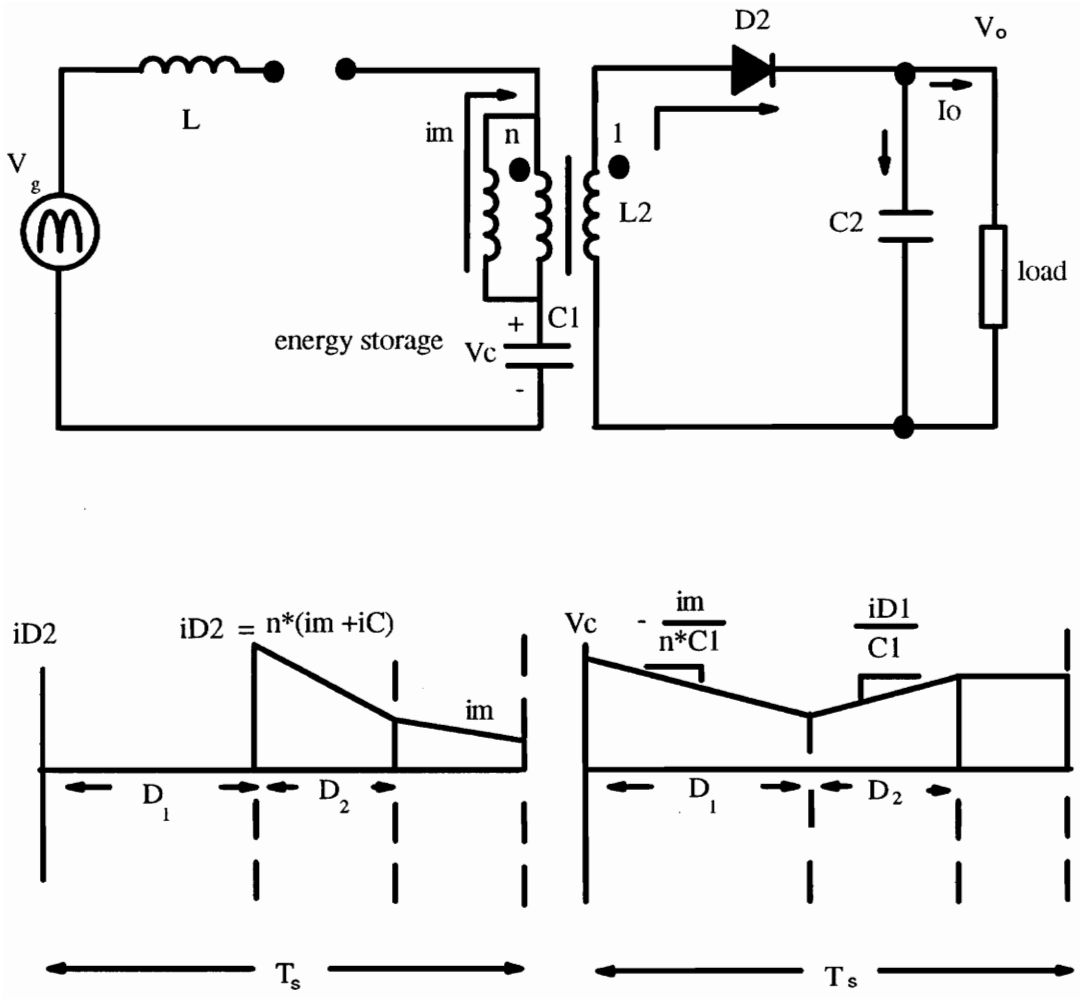

Fig.3.6 BIFRED operation and current waveforms when the boost converter is in DCM.

3.2 THE INTEGRATION OF DCM BOOST CONVERTER AND FORWARD CONVERTER.

As in the BIFRED converter case, discussed in the previous section, a single-stage, single-switch forward type converter can be obtained when a DCM boost converter is combined with a forward converter. As long as the boost converter operates in DCM, the resulting converter will have inherent power factor correction.

The integration steps of DCM boost converter and forward converter are shown in Fig. 3.7, Fig.3.8, and Fig.3.9. Fig.3.7 shows the conventional way of putting the forward converter behind the boost converter. The two switches shown in Figure3.7 are reduced into one as illustrated in Fig.3.8. The switch of the boost converter is eliminated.

As it is mentioned in the previous section that the boost inductor needs to be followed by a diode to ensure discontinuous conduction. So the diode of the boost converter is preserved. Then, the connection between the boost converter diode and the bulk capacitor is broken. The loose end of the diode is attached to the switch of the forward converter. However, the boost converter current needs to flow into the bulk capacitor through the primary winding of the transformer, so there must be a path for the reflected current to flow in the direction opposite to that when the switch is turned on. Thus, the forward diode which allows the current to flow in only one direction can no longer be used. The forward diode is replaced by a coupling capacitor which allows current to flow in both directions. The resulting circuit is a *B*oost converter *I*ntegrated with a *B*uck *R*egulator with isolation/ *E*nergy storage *D*c-dc converter (BIBRED), as described in [1]. The resulting BIBRED converter is shown in Fig.3.9.

There are three topological modes within one cycle of operation of the BIBRED converter. They are shown in Fig.3.10, Fig.3.11 and Fig.3.12.

In Fig.3.10, when the switch is turned on, the boost inductor is energized by the voltage source, while the transformer is energized by the bulk capacitor. The bulk capacitor serves as the dc voltage source for the forward converter. During this period of time, the freewheeling diode is reversed biased and the load current is supplied by the reflected

bulk-capacitor current which flows through the coupling capacitor and the output choke as shown.

In Fig.3.11, when the switch is turned off, the boost inductor current charges the bulk capacitor. The transformer core is then reset automatically by this process. The output choke current keeps on flowing through the freewheeling diode to supply the load. The reflected DCM boost inductor current also flows through the freewheeling diode to recharge the coupling capacitor as illustrated.

In Fig.3.12, when the inductor current is depleted, the bulk capacitor voltage does not change any more. The output choke current continues to freewheel as shown. It should be noticed that there can be no average voltage across the transformer or the output choke windings. So, the voltage of the coupling capacitor at the secondary side of the transformer is equal to the output voltage of the converter. Because the existence of this coupling capacitor the original forward converter is no longer be the same. The resulting voltage conversion ratio will not be the same as the forward converter. The analysis will be discussed in section 3.3.2.

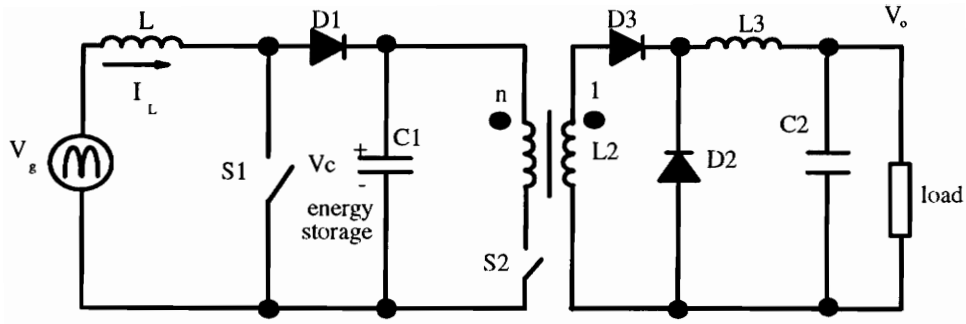

Fig.3.7 Cascaded boost and buck converters.

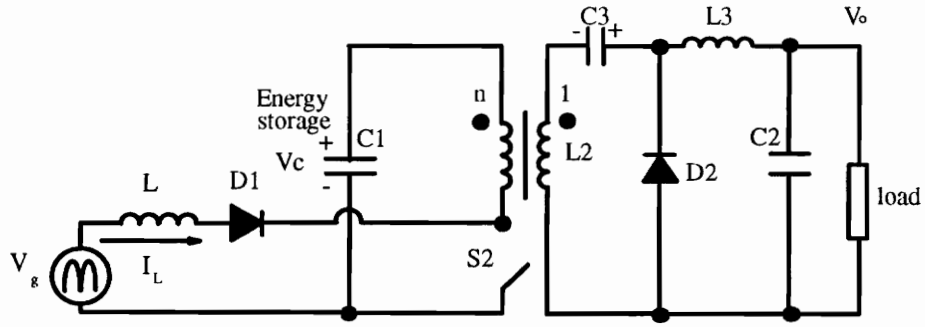

Fig.3.8 Combination of two switches into a single one.

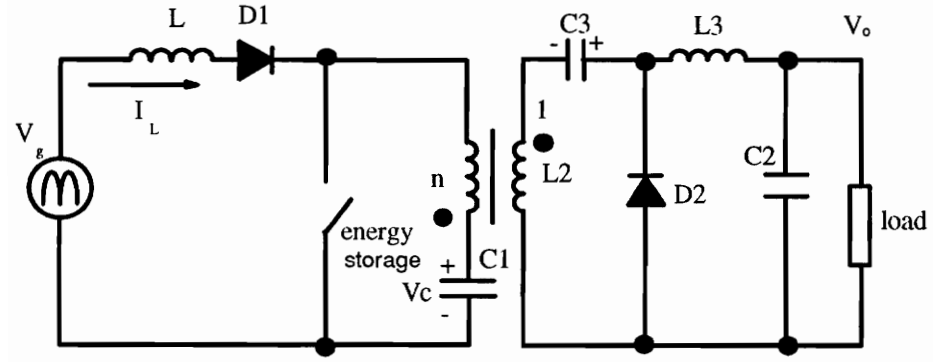

Fig.3.9 Boost integrated witha Buck regulator/energy storage dc-dc converter (BIBRED).

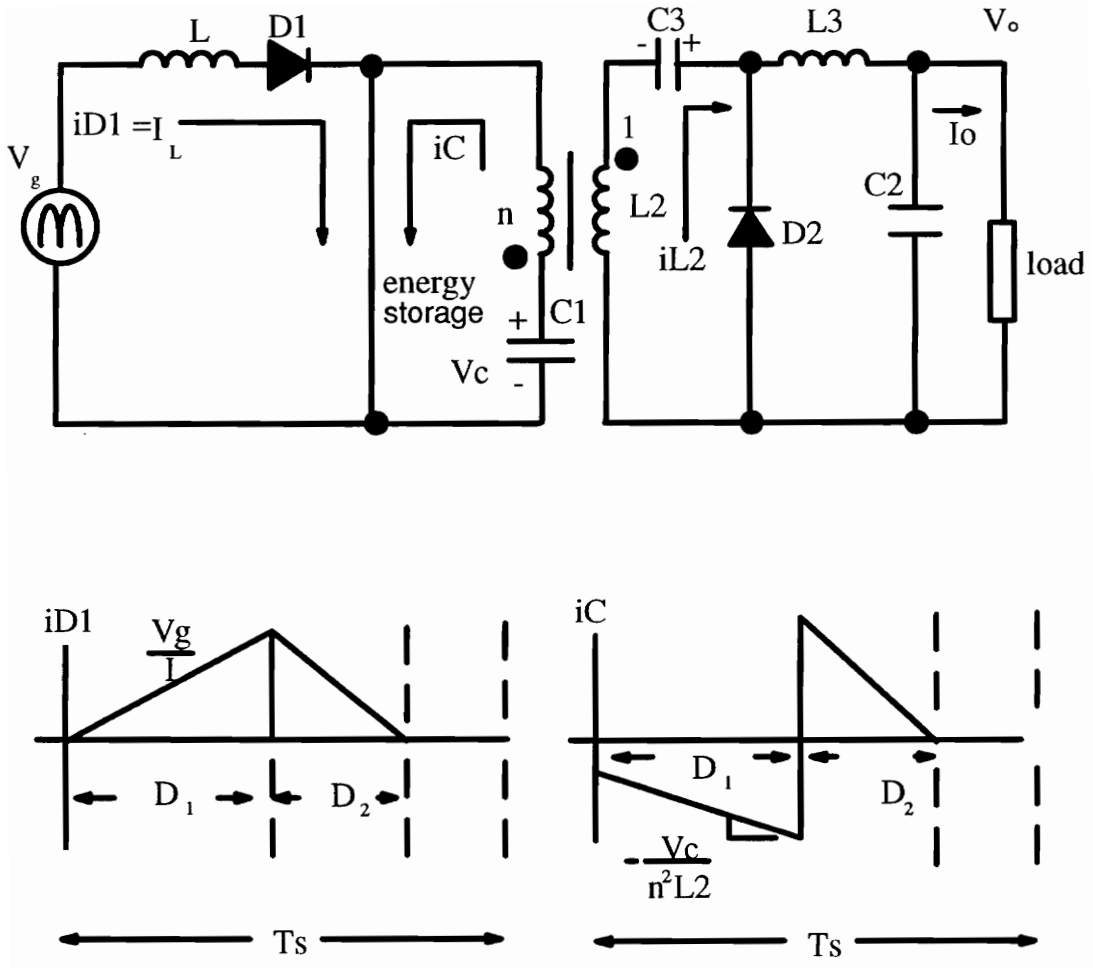

Fig.3.10 BIBRED operation and current waveforms during on time.

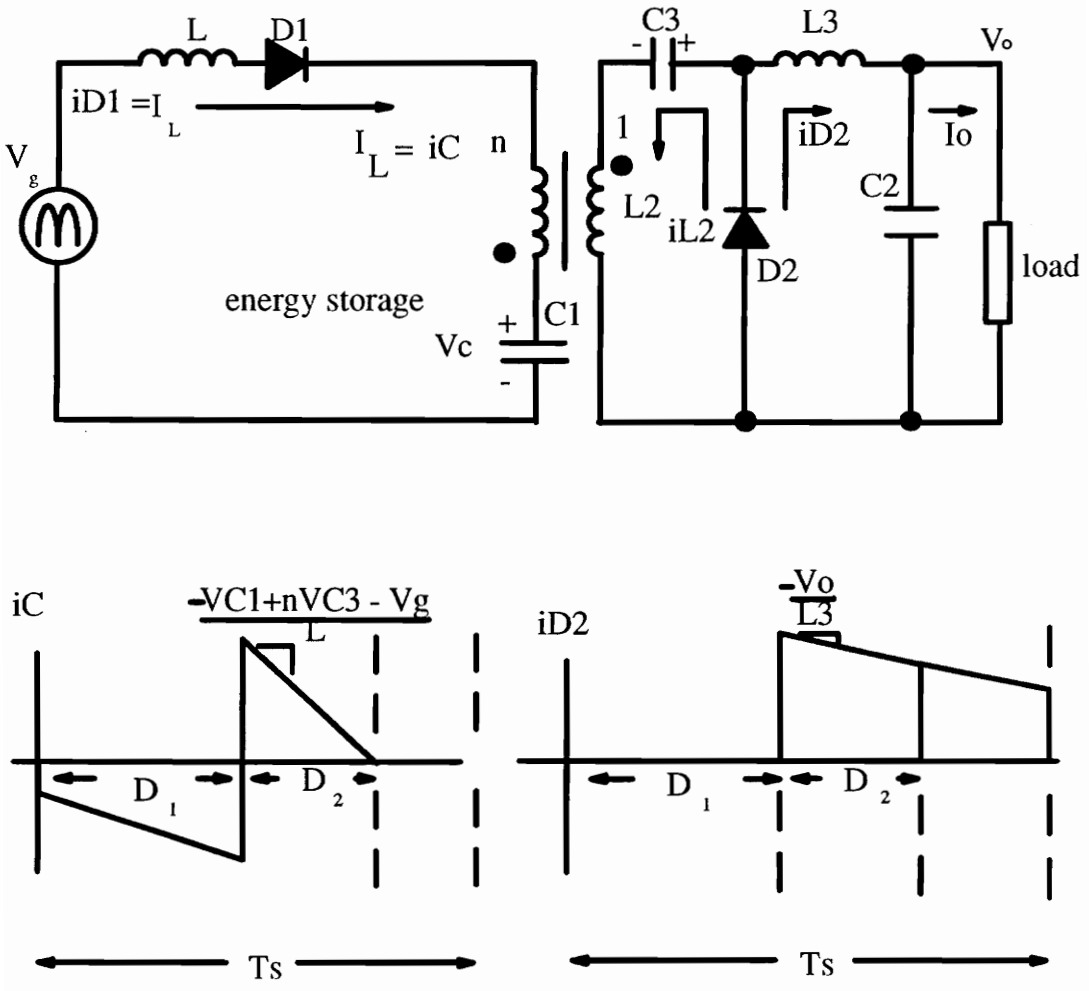

Fig.3.11 BIBRED operation and waveforms during off time.

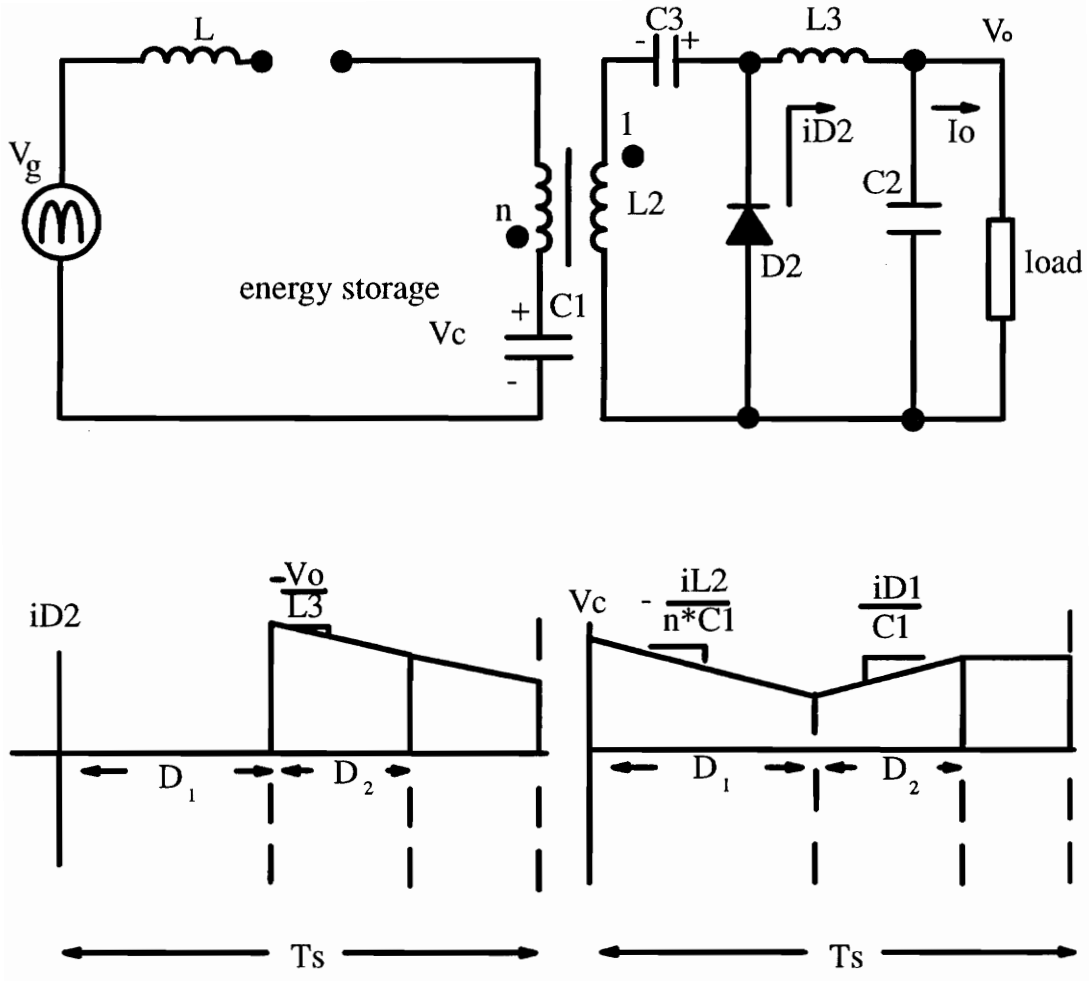

Fig.3.12 BIBRED operation and current, voltage waveforms when the boost inductor current is depleted.

3.3 DC ANALYSIS OF THE BIFRED AND BIBRED CONVERTERS

3.3.1 THE ANALYSIS OF THE BIFRED CONVERTER

The BIFRED converter is composed of the DCM boost converter and the flyback converter sharing the same switch. So, the on time duty ratio is the same in both topologies. A simple way to do the analysis is to work on individual converter and combine the steady state equations by eliminating the common terms.

The three topological modes within one cycle of operation of the DCM boost converter are shown in Fig.3.13, Fig.3.14 and Fig.3.15. Let V_g be the input voltage, V_{ob} be the output voltage of the boost converter stage, D_1 be the switch on time duty ratio, D_2 be the switch off time duty ratio before the inductor current is depleted, T be the switching period, I_{d2} be the boost inductor discharging current, L be the inductance, R_{ob} be the resistive load, and I_{ob} be the output current of the boost converter stage. Applying flux balance on the inductor in the DCM boost converter,

$$V_g \bullet D_1 \bullet T = (V_{ob} - V_g) \bullet D_2 \bullet T \tag{3.1}$$

$$\frac{V_{ob}}{V_g} = 1 + \frac{D_1}{D_2} \tag{3.2}$$

The output current is equal to the inductor discharging current. Hence,

$$I_{d2} = I_{ob} = \frac{V_{ob}}{R_{ob}} = \frac{1}{2} \bullet \frac{D_1 \bullet T \bullet V_g}{L} \bullet D_2 \tag{3.3}$$

Substitute (3.3) into (3.2) to eliminate D_2,

$$\frac{V_{ob}}{V_g} = \frac{1}{2} \bullet \left(1 + \sqrt{1 + \frac{2D_1^2 \bullet T \bullet R_{ob}}{L}} \right) \tag{3.4}$$

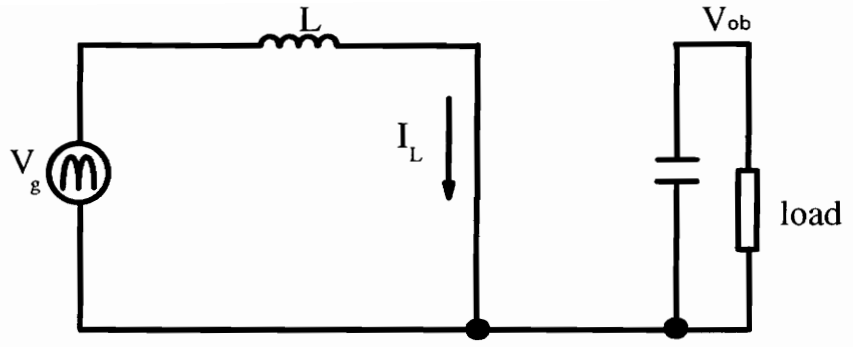

Fig.3.13 Boost converter during switch on time.

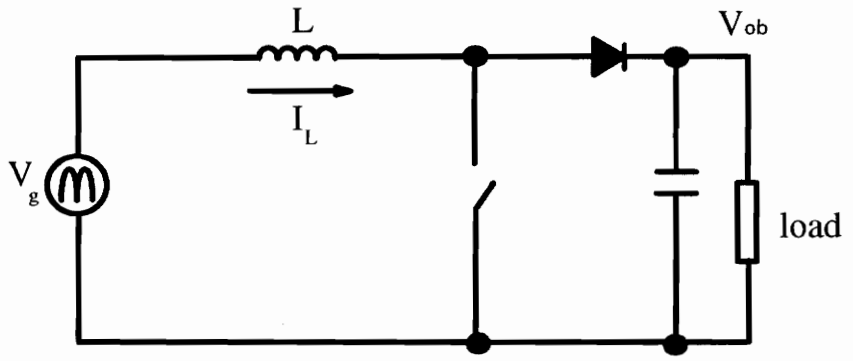

Fig.3.14 Boost converter during switch off time.

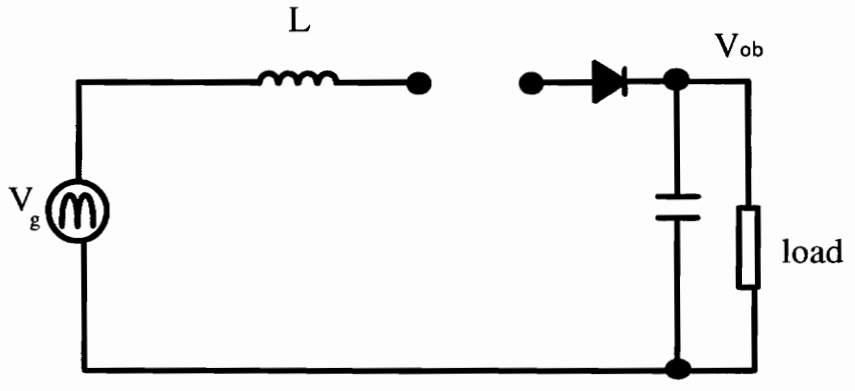

Fig.3.15 Boost converter when inductor current is depleted.

Let V_c be the bulk-capacitor voltage, n be the turns ratio of the transformer, R be the output resistive load, and V_o be the output voltage of the flyback converter. The flyback converter voltage conversion ratio is then given by,

$$V_c = n \bullet V_o \frac{(1 - D_1)}{D_1} \tag{3.5}$$

Furthermore, the output voltage of the boost converter stage is actually equal to the sum of the bulk capacitor voltage and the reflected output voltage of the flyback converter as illustrated in Fig.3.5 of section 3.1. Hence,

$$V_{ob} = n \bullet V_o + V_c \tag{3.6}$$

Combining equations (3.3), (3.4) and (3.5) and followed by some approximations and iterations, the following steady state solution of the bulk capacitor voltage of the BIFRED converter is obtained, as derived in [1]. Where the boost converter voltage gain must be between 1.4 and 3.0 to have accuracies within 10%.

$$\frac{V_c + n \bullet V_o}{V_{grms}} \approx \frac{1}{\sqrt{2}} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet n^2 \bullet T \bullet V_o}{L \bullet I_o}} \right) \tag{3.7}$$

3.3.2 THE ANALYSIS OF THE BIBRED CONVERTER

As in the BIFRED converter case, the BIBRED is composed of the DCM boost converter and a dc-dc converter with isolation. However, as discussed in section 3.2, the forward converter is changed after the integration with the DCM boost converter. Let V_{cp} be the coupling capacitor voltage. The resulting voltage conversion ratio is shown in the following derivation based on Fig.3.6 of section 3.2. Applying flux balance on the voltage across the output choke of the BIBRED converter,

$$\left(\frac{V_c}{n}+V_{cp}-V_o\right)\bullet D_1\bullet T=V_o\bullet(1-D_1)\bullet T \tag{3.8}$$

Since there can be no average voltage across both the transformer winding and the output choke winding, the coupling capacitor voltage V_{cp} is equal to the output voltage V_o. Hence equation (3.8) is reduced to,

$$V_c=n\bullet V_o\frac{(1-D_1)}{D_1} \tag{3.9}$$

The resulting voltage gain is the same as the one of a flyback converter. The same analysis procedure can be done on the BIBRED converter as described in the last section. Thus, it is concluded that the steady state solution of the bulk capacitor of the BIBRED converter is same as that of the BIFRED converter and is repeated here as shown in equation (3.10).

$$\frac{V_c+n\bullet V_o}{V_{grms}}\approx\frac{1}{\sqrt{2}}\bullet\left(1+\sqrt{1+\frac{0.852\bullet n^2\bullet T\bullet V_o}{L\bullet I_o}}\right) \tag{3.10}$$

3.4 THE PERFORMANCE OF THE INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS WITH RESPECT TO THE IEC555-2 STANDARDS.

The IEC555-2 standards have requirements on each harmonic current according to different input power. The IEC555-2 standards are outlined in Table 3.1. This set of standards imposes a tighter requirement on higher power applications. It has a looser requirement however on lower power applications. Thus, the more expensive and complex two stages converters which give very good power factor is not needed. On the contrary, the less expensive and simpler integrated high-quality rectifier-regulator is sufficient to meet the requirements in lower power applications. These will be illustrated in the examples of the following discussion.

Due to the half wave symmetry of the line current waveform, only the odd harmonics are significant. And the third harmonic current is the highest amongst all the harmonics. Furthermore, the power factor can be expressed as the product of the distortion factor K_d and the displacement factor K_θ as shown in equation (3.11). But, it is generally true that the line voltage is sinusoidal. Therefore, the displacement factor is equal to 1 and the power factor depends only on K_d. The total harmonics distortions (THD) is defined as the square root of the ratio of the summation of all harmonics currents square except the fundamental current to the square of the fundamental current I_1, as shown in equation (3.12), as derived in [8]. Hence, the power factor, PF, required to meet the IEC555-2 standards can then be determined by the PF and THD relation, as shown in equation (3.13).

$$PF = K_d \cdot K_\theta \tag{3.11}$$

Since $K_\theta = 1$, the total harmonics distortions definition, and the PF / THD relation is given by,

$$THD = \sqrt{\frac{\sum_{n \neq 1} I_n^2}{I_1^2}} \tag{3.12}$$

$$PF = K_d = \sqrt{\frac{1}{1 + (THD)^2}} \tag{3.13}$$

Example 1:

Suppose the efficiency of a 450 W, 5 V output converter is 75%. Thus, the input power P_{in} is 600 W. It is assumed that the input line voltage is a pure sinusoidal waveform. The fundamental line current is then equal to the input power divided by the line voltage. The highest line current would be at the lowest line voltage, which is 85 V_{rms}.

$$I_1 = \frac{600}{85V} = 7.05A$$

Table 3.1 IEC555-2 standards for class D equipment.

Harmonic order n	Range of input power P (W)		
	P ⩽ 75W	75W < P ⩽ 400W	400W < P ⩽ 600W
	Maximum permissible harmonic current		
Odd Harmonics	(mA)	(mA)	(A)
3	275	275 + 3.4 * (P - 75)	1.38
5	175	175 + 1.3 * (P - 75)	0.6
7	125	125 + 1.0 * (P - 75)	0.45
9	100	100 + 0.4 * (P - 75)	0.23
11 ⩽ n ⩽ 39	550/n	(550 + 3.3 * (P - 75))/n	1.62/n
Even Harmonics			
2	100	100 + 0.4 * (P - 75)	0.23
4	50	50 + 0.2 * (P - 75)	0.12

By equation (3.12), the maximum THD allowed according to IEC555-2 standards is,

$$THD = \sqrt{\frac{1.38^2 + 0.6^2 + 0.45^2 + 0.23^2 + 0.23^2 + 0.12^2}{7.05^2}} \approx 22.8\%$$

The required PF is then given by,

$$PF = \sqrt{\frac{1}{1 + (22.8\%)^2}} \approx \underline{\underline{0.975}}$$

Example 2:

Suppose the efficiency of a 100W, 5V output converter is 75%.
$P_o = 100W, \eta = 75\%$. Thus, the input power P_{in} is = 133.3W.
The highest line current would be at the lowest line voltage, which is 85 V_{rms}.

$$I_1 = \frac{133.3W}{85V} = 1.57A$$

By equation (3.12), the maximum THD allowed according to IEC555-2 standards is,

$$THD = \sqrt{\frac{0.473^2 + 0.25^2 + 0.183^2 + 0.123^2 + 0.123^2 + 0.06^2}{1.568^2}} \approx 38\%$$

The required PF is then given by,

$$PF = \sqrt{\frac{1}{1 + (38\%)^2}} \approx \underline{\underline{0.934}}$$

One can follow the examples above to design the converter which can meet IEC555-2 standards. According to the power factor and inverse voltage gain relationship shown in Fig.2.3, the required M is 0.85 for a 100 W power supply which has a efficiency of 75%. Thus, if the power factor is equal to or better than 0.934 (or M is 0.85 or better), then the converter will meet the IEC555-2 standards. However, there are some severe drawbacks in the family of integrated high-quality rectifier-regulators. The limitations of this converter are discussed in the following section.

3.5 LIMITATIONS OF THE INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS.

3.5.1. THE BULK-CAPACITOR VOLTAGE STRESS PROBLEM.

The bulk-capacitor voltage of both the BIFRED and BIBRED converters is load dependent. The capacitor voltage increases when load current decreases. This is due to the load dependent characteristic of the DCM boost converter. It can be observed from the inductor current waveform of the DCM boost converter, as shown in Fig.3.16. When the load current is lighter, both the on time and off time duty ratios of the DCM boost converter will decrease. In addition, there is a dc-dc converter, a CCM flyback converter in the case of BIFRED converter, and a forward converter in the case of a BIBRED converter, right behind the DCM boost converter. The on time duty ratio of the boost converter is the same as the dc-dc converter because the switch is the same for both converters. The BIFRED converter is used as an example for the illustration. Since the bulk capacitor acts as the supply voltage source of the flyback converter, as discussed in section 3.1, so V_c becomes the input voltage of the dc-dc converter. The flyback converter voltage conversion ratio is shown in following equation.

$$V_c = n \bullet V_o \frac{(1-D_1)}{D_1}$$

Since the output voltage, V_o, is regulated and the flyback converter is in CCM, the duty ratio decreases when the input voltage increases. Therefore, the bulk-capacitor voltage has to increase in order to have a smaller duty cycle at lighter loads. As observed from the DC voltage gain characteristic of the boost converter in Fig.3.17, when the duty cycle decreases, the boost converter in DCM could have a larger voltage gain or a smaller one depends on the operating region. If the duty cycle decreases very quickly, then the voltage gain is smaller. But if the duty cycle decreases not as much, the voltage gain will be higher. Since the output voltage of the DCM boost converter is equal to the sum of the reflected output voltage and the bulk-capacitor voltage, a higher voltage gain means a higher bulk capacitor voltage for the output voltage is regulated.

But as discussed in the previous paragraph, the bulk capacitor voltage has to increase in order to have a smaller duty cycle, so the DCM boost converter needs to operate in the upper region of the dc voltage gain curve shown in Fig.3.17. The bulk capacitor voltage stress cannot be reduced by the conventional way of reducing the duty cycle by using fast control. This load dependent characteristic of the bulk capacitor voltage can also be observed readily in the steady state equation (3.7) of the BIFRED converter.

However, this bulk capacitor voltage stress problem can be alleviated a little bit by operating the dc-dc converter in discontinuous conduction mode at very light load. As in the DCM boost converter case, the duty ratios will decrease as the load current decreases if the dc-dc converter operates in DCM. Thus, the bulk capacitor voltage does not need to increase further. But the dc-dc converter should not run in discontinuous conduction mode for the whole range of operation. This is because of the high current stress, high current ripple, and higher conduction loss due to higher root means square current in DCM. These factors are especially significant at the secondary side of the transformer when the output voltage is low and load current is high. Therefore, there is more harm than good by operating both the boost converter and the dc-dc converter with isolation in discontinuous conduction mode. Since the boost converter has to run in discontinuous conduction mode in order to have inherent power factor correction capability, the only realistic combination of this integratred high-quality rectifier-regulators is a DCM boost converter followed by a CCM dc-dc converter. A better way to reduce the bulk capacitor voltage stress problem will be discussed in the next chapter.

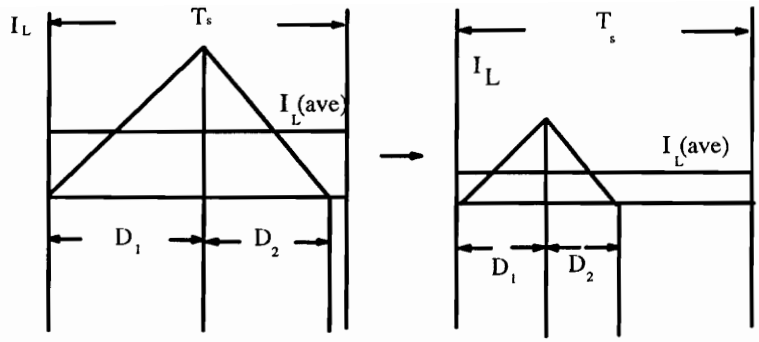

Fig.3.16 Duty ratios decrease as load current decreases.

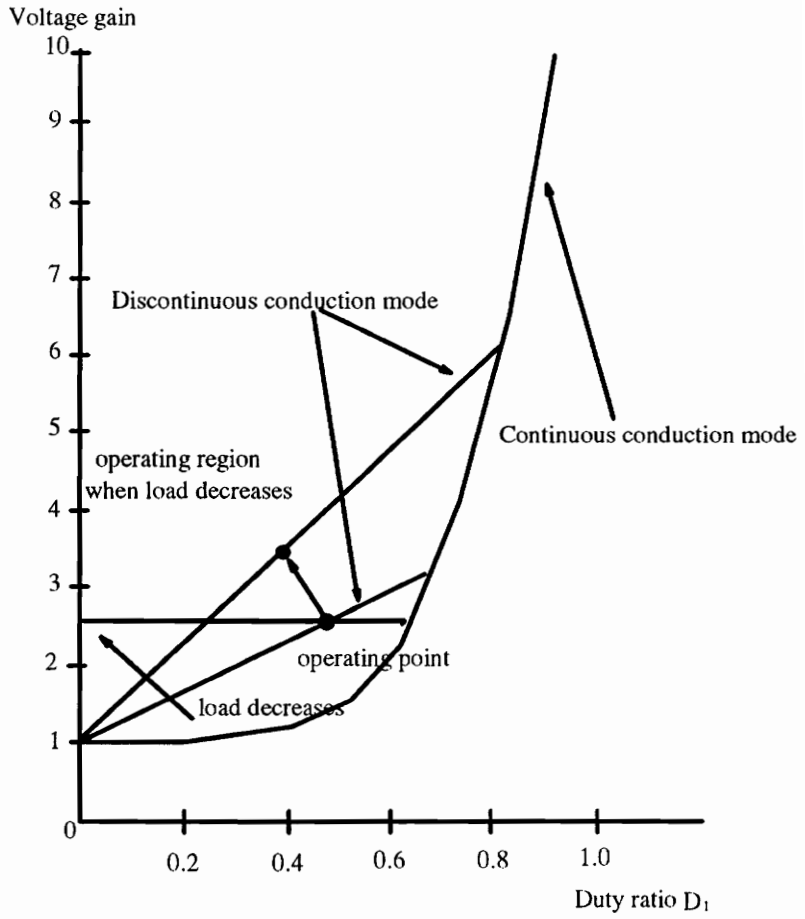

Fig.3.17 DC gain characteristic of DCM boost converter.

3.5.2 A NUMERICAL EXAMPLE TO SHOW THE BULK CAPACITOR VOLTAGE STRESS PROBLEM

The bulk-capacitor voltage stress problem at light-load is illustrated in the following numerical example. The bulk capacitor voltage stress can be calculated using the BIFRED converter steady state equation (3.7).

Specifications:

1. Input voltage : 85 to 270 Vac.
2. Output voltage : 5Vdc.
3. Load current : 1.8A to 18A.

In order to have harmonic currents which meet IEC555-2 standards, the inverse voltage gain, M should be less than or equal to 0.75 in order to have a PF equal to or better than 0.96, as discussed in chapter 2. M is chosen to be 0.7 to have some margin. This condition ensures the boost inductor operates in DCM and the resulting line harmonics currents will comply with the IEC555-2 standards. The turns ratio of the transformer is chosen to be 10. This is based on the fact that a larger turn ratio will give higher bulk capacitor voltage stress due to the reflected equivalent output voltage. But a smaller ratio will give smaller duty cycle and thus higher current stress and larger conduction loss on the switch and the output diode. It is due to the higher RMS current and longer conduction period for the output diode for a smaller duty cycle. So, a ratio of 10 is a reasonable choice. Substitute these conditions into the steady state solution of the bulk capacitor voltage equation (3.7),

$$n = 10, \quad T = 20\mu\ s, \quad V_o = 5Vdc, \quad I_o = 18A, \quad M = 0.7$$

$$\frac{1}{0.7} \approx \frac{1}{2} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet 20 \bullet 10^{-6} \bullet 5}{L \bullet 18}} \right)$$

The boost inductance L needed is $= 194\mu\ H$.

The resulting bulk capacitor voltage at different loads can then be calculated. The values obtained are plotted in Fig.3.18. The bulk-capacitor voltage at 10% load (1.8A), with input voltage at 85Vac, 135Vac, and 270Vac, are 310Vdc, 520Vdc, and 1100Vdc respectively. Therefore, the integrated high-quality rectifier-regulator has limited voltage and load range for an universal input-voltage range and wide load range design. The schemes to alleviate this bulk-capacitor voltage stress problem will be discussed in the next chapter.

3.5.3 BOOST INDUCTOR CURRENT CRASHES WITH THE TRANSFORMER LEAKAGE CURRENT WHEN THE SWITCH IS TURNED OFF.

Another disadvantage is the current crashing between the boost inductor current and the leakage inductance of the transformer when the switch is turned off. As mentioned in the previous section, the boost inductor current charges the bulk capacitor and reset the transformer when the switch is turned off. The leakage current of the transformer needs not only to stop but to reverse in the direction of the boost inductor current at the instance of turning off of the switch. This is opposite to the original direction of the current flows in the primary side of the transformer. Thus, the rate of change of the leakage inductor current is so high that it generates a large voltage spike. This voltage spike problem due to current crashing between the boost inductor current and the leakage current of the transformer is illustrated by a Pspice simulation waveforms shown in Fig.3.19.

The BIBRED converter is used in the simulation. The input voltage applied is 150 Vdc. The output voltage is 5 Vdc and the output power is 50 W. the resulting drain-to-source voltage spike is 2K Vdc. The scheme to alleviate this voltage spike problem will be discussed in the next chapter.

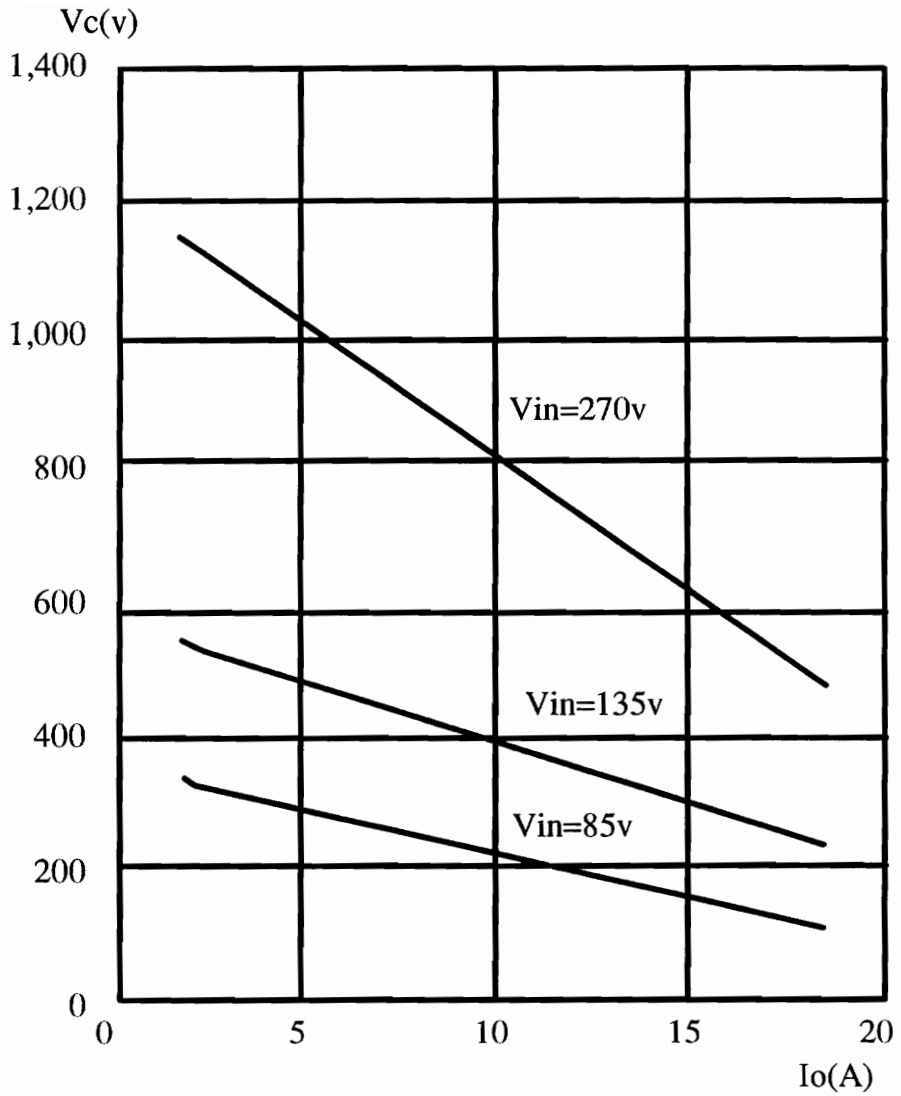

Fig.3.18 Load dependent characteristic of the bulk capacitor voltage of the BIFRED converter.

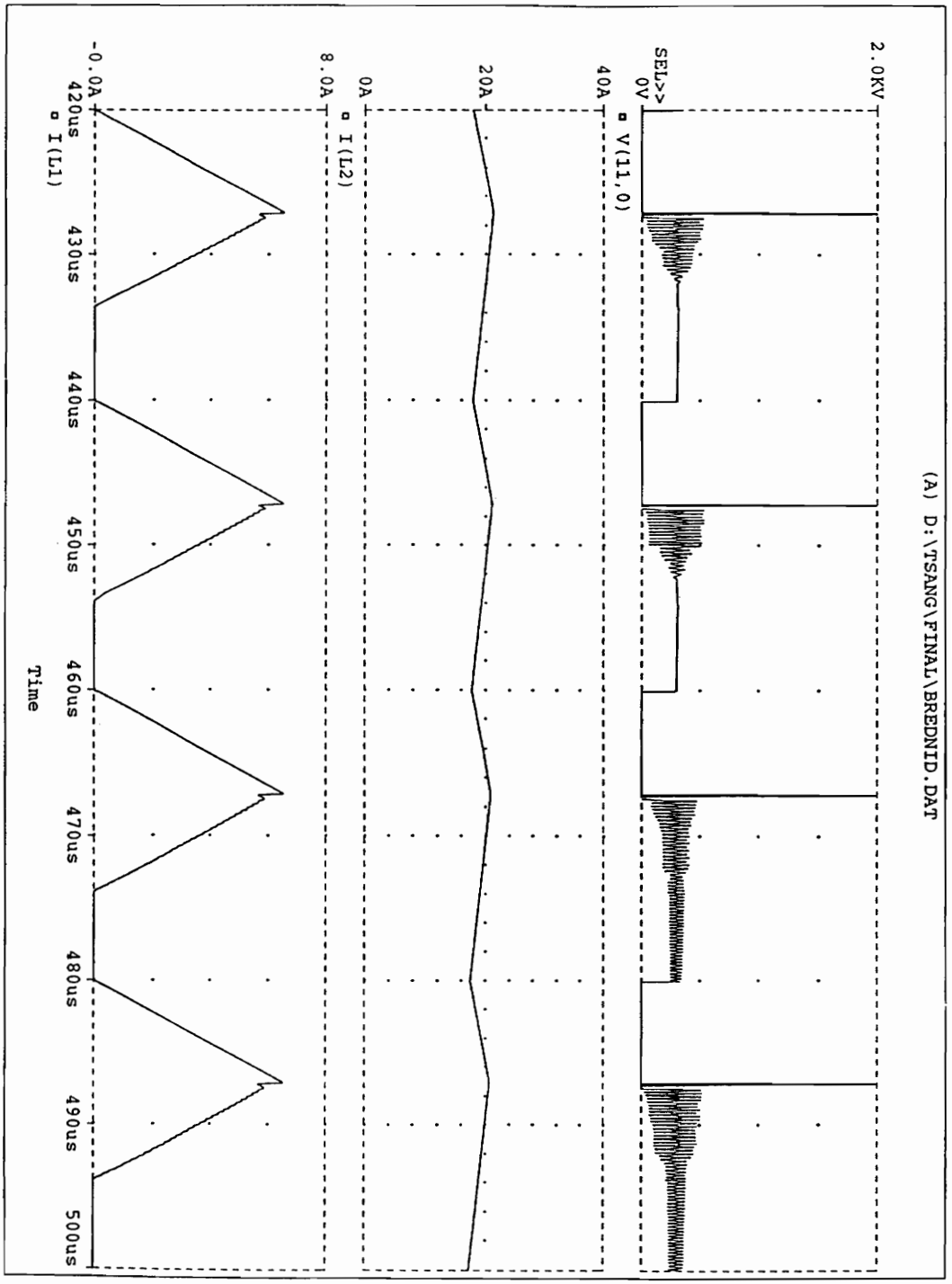

Fig.3.19 Voltage and current waveforms at switch turn-off.

3.5.4 CURRENT STRESS OF THE INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS.

Since the boost converter needs to operate in discontinuous conduction mode, the current stress is high. This results in higher conduction loss due to higher RMS current value. This drawback also affects the attaching dc-dc converter. It is because when the switch is turned off in the BIFRED converter, the discontinuous boost inductor current is reflected to the secondary side of the transformer. So, there is a large current ripple on the top of the current on the secondary side of the transformer. This again contributes to the increase of conduction loss. The same drawback exists in the BIBRED converter and the other integrated high-quality rectifier-regulators. Even though there is a output choke which reduces the current at the output terminal in the BIBRED converter, the coupling capacitor still needs to handle the large reflected ripple of the boost inductor current. Besides, the EMI filter also needs to be larger due to the discontinuous conduction boost inductor current. This drawback renders this type of integrated high-quality rectifier-regulators limited to low power applications.

3.6 SUMMARY

The procedures to obtain the BIFRED, BIBRED converters from the integration of the DCM boost converter and the flyback, forward converters are discussed. The operations of both converters are discussed by demonstrating each topological modes in one complete cycle of operation. It is then followed by the DC analysis of the converters. This is done by doing analysis separately on the DCM boost converter and the dc-dc converter with isolation. The steady state equations obtained in each converter are then combined to obtain the steady state solutions of the resulting BIFRED and BIBRED converters. The advantage of using this converter with respect to IEC555-2 standards in low power applications is discussed and illustrated by two numerical examples. Finally, the limitations of this type of single stage converter with PFC are discussed and illustrated with a numerical example and a Pspice simulation. The converter has limited input

output load ranges due to the bulk-capacitor voltage stress problem. The crashing of the boost inductor current and the current of the leakage inductance of the transformer results in high voltage spike when the switch is turned off. In addition, the discontinuous boost inductor current gives high current stress, high conduction loss due to the high RMS current, and requires a larger EMI filter. Thus, this family of integrated high-quality rectifier-regulators is limited to low power applications.

4. IMPROVEMENTS IN THE INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS.

4.1 REDUCE BULK-CAPACITOR VOLTAGE STRESS BY INCRESAING SWITCHING FREQUENCY AT LIGHTER LOADS.

According to the argument In section 3.4.1, the bulk capacitor voltage V_c increases when the on time duty ratio, D_1, decreases at lighter loads. Hence, if there are some ways to increase D_1 at lighter loads, then V_c can be reduced. In Fig. 4.1, the switch on time duration will decrease as the switching frequency increases. Thus, the energy input to the bulk capacitor through the boost inductor will also decrease. The bulk-capacitor voltage will be reduced when the switching frequency is increased for a constant load. This can be explained analytically. It should be noticed that duty ratio, D_1, (not the on time duration) does not necessarily decrease when the switching frequency increases. This is because the switching period decreases as the switching frequency goes up. The duty ratio is possible to increase even though the on time duration decreases. This can be observed in the DCM boost converter dc voltage gain characteristic plot as shown in Fig.4.2 and equation (4.1).

$$\frac{V_{ob}}{V_g} = \frac{1}{\sqrt{2}} \cdot \left(1 + \sqrt{1 + \frac{2 \cdot D_1^2 \cdot T \cdot R}{L}} \right) \tag{4.1}$$

Where V_{ob} is the output voltage of the DCM boost converter, V_g is the input voltage, L is the boost inductance, T is the switching period and R is the load resistance. Since V_g, L and R are constant, it is possible that the duty ratio, D_1, increases when T decreases or the switching frequency increases depends on the operating region. However, the CCM dc-dc converter integrated with the DCM boost converter limits the operating region, such that D_1 has to increase when the switching frequency increases at constant load. This can be oberserved readily from the BIFRED (BIBRED) steady states equations derived in [1], as shown in the followings,

$$\frac{V_o}{V_{grms}} \approx \frac{D_1}{\sqrt{2} \cdot n} \cdot \left(1 + \sqrt{1 + \frac{0.852 \cdot n^2 \cdot T \cdot V_o}{L \cdot I_o}} \right) \tag{4.2}$$

$$\frac{V_c + n \cdot V_o}{V_{grms}} \approx \frac{1}{\sqrt{2}} \cdot \left(1 + \sqrt{1 + \frac{0.852 \cdot n^2 \cdot T \cdot V_o}{L \cdot I_o}} \right) \tag{4.3}$$

From the above two equations, it can be observed D_1 will actually increase when the switching frequency increases. And the bulk capacitor V_C will decrease when the switching frequency increases with the load remains constant. Therefore, the bulk capacitor voltage stress can be reduced by increasing the switching frequency at lighter loads.

Furthermore, the switching frequency should not be increased for the whole load range. It is because the boost converter must operates in DCM in order to have inherent power factor correction capability. The boost inductor current will reach CCM faster at a higher switching frequency for the same amount of power. Thereby, it limits the amount of power the circuit can handle. Thus, the switching frequency increases at lighter loads can help reducing the bulk-capacitor voltage stress and yet without affecting the amount of power the circuit can handle.

The variable frequency control needed at lighter loads can be realized by using a voltage controlled oscillator. This is discussed in the following section. The improvements in the bulk-capacitor voltage stress is shown in Fig.4.3.

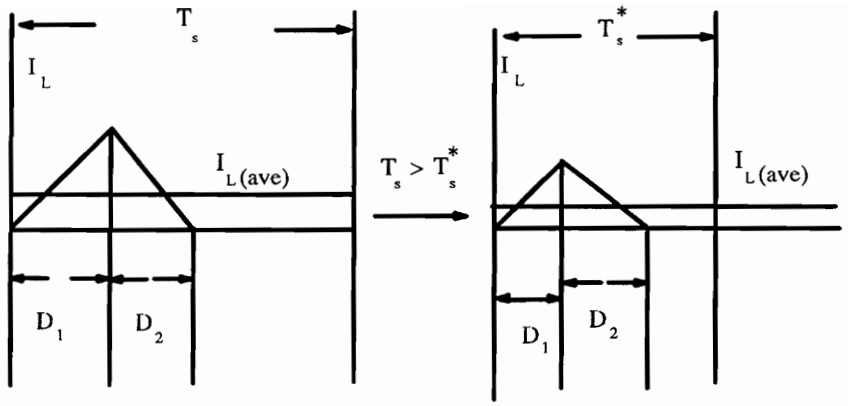

Fig.4.1 Duty ratio increase as switching frequency increases.

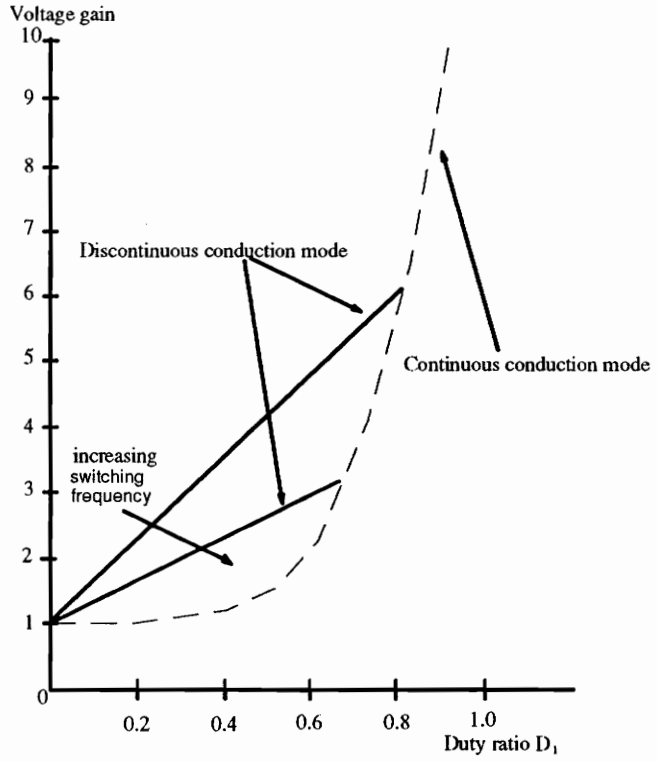

Fig.4.2 DC gain characteristic of DCM boost converter to show the effect of increasing switching frequency.

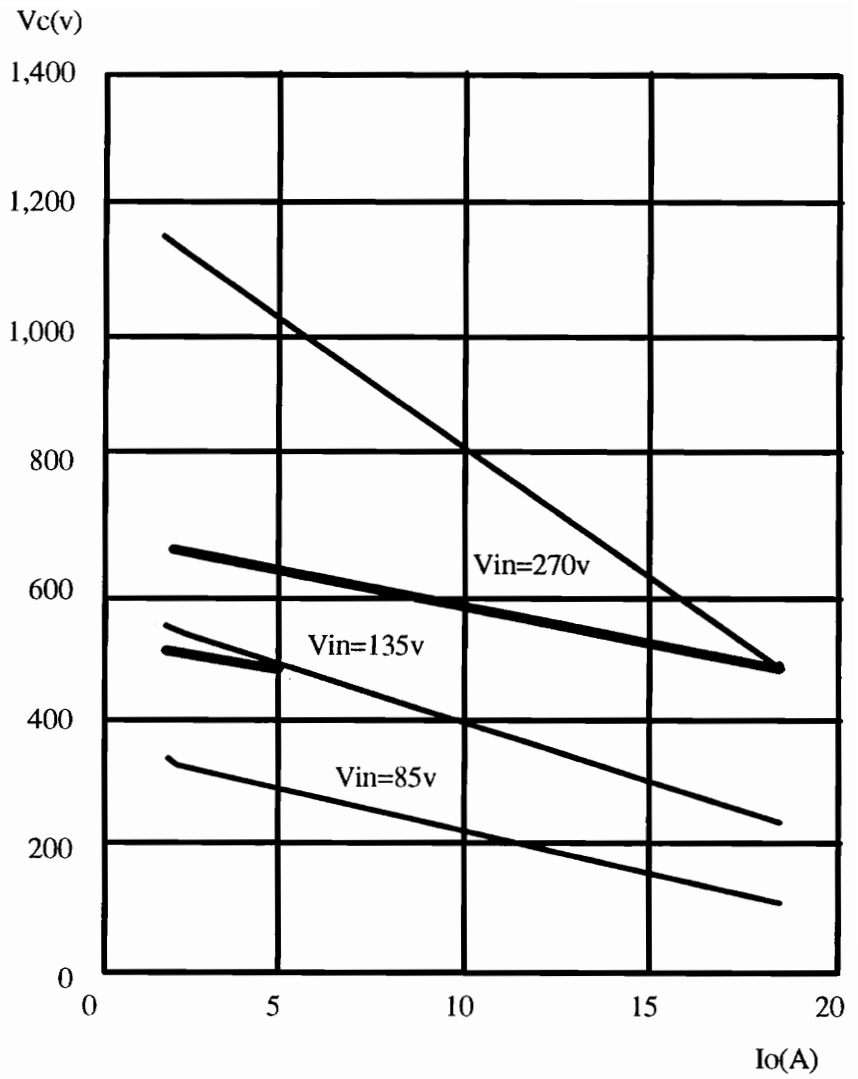

Fig.4.3 Improvements in the bulk-capacitor voltage stress by using variable frequency control.

4.2 IMPLEMENTATION OF VARIABLE FREQUENCY CONTROL.

The variable frequency control is obtained by using a voltage controlled current source (a BJT) connected in parallel to the timing resistance pin of the PWM controller chip as shown in Fig.4.4. The bulk-capacitor voltage is sensed and stepped down by using a voltage divider. The resulting voltage is compared with a reference voltage by using a difference amplifier to generate a base drive voltage to bias the BJT. (A higher gain of this control loop can be achieved by adding an integrator, one pole and one zero to the comparator circuit with the cross-over frequency behind the pole). The BJT is turned on when the bulk capacitor voltage reaches a certain level which needs to be controlled. When the bulk-capacitor voltage increases, the base drive voltage of the BJT increases. The equivalent resistance of the BJT decreases accordingly. Since the BJT is connected in parallel to the timing resistance of the PWM controller chip, the equivalent timing resistance decreases also. The switching frequency will then increase.

Furthermore, it can be designed in such a way that the bulk-capacitor voltage is not high enough to turn on the BJT at desired heavier load range. Thus, the switching frequency remains the same at heavier loads and increases only at lighter loads at which the bulk capacitor-voltage is higher. This is desirable, because higher the switching frequency, lower the power the BIFRED or BIBRED converter can handle in order to keep the boost converter operates in DCM. Therefore, the switching frequency increases at lighter loads only will not further limit the maximum power level of the converters.

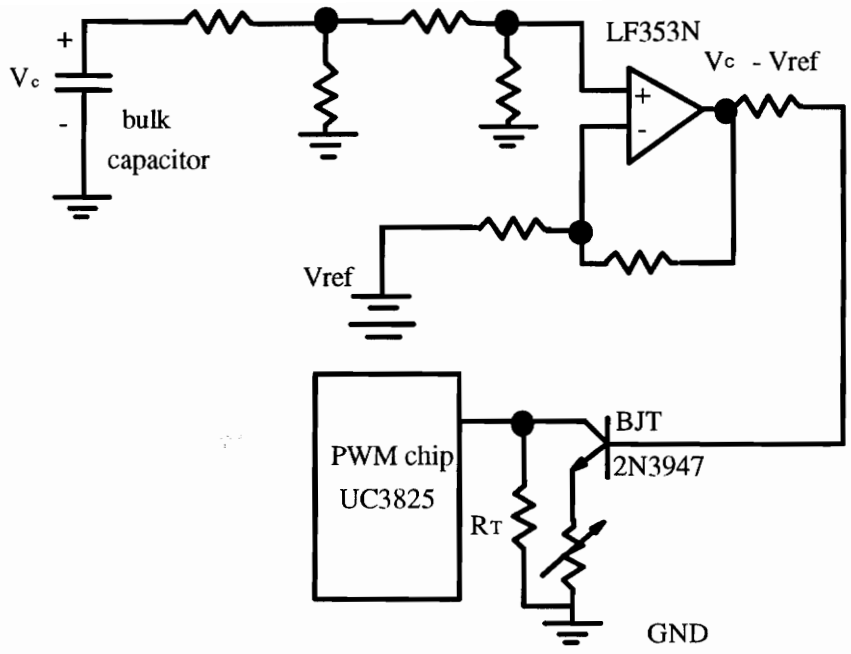

Fig.4.4 Variable frequency control circuit.

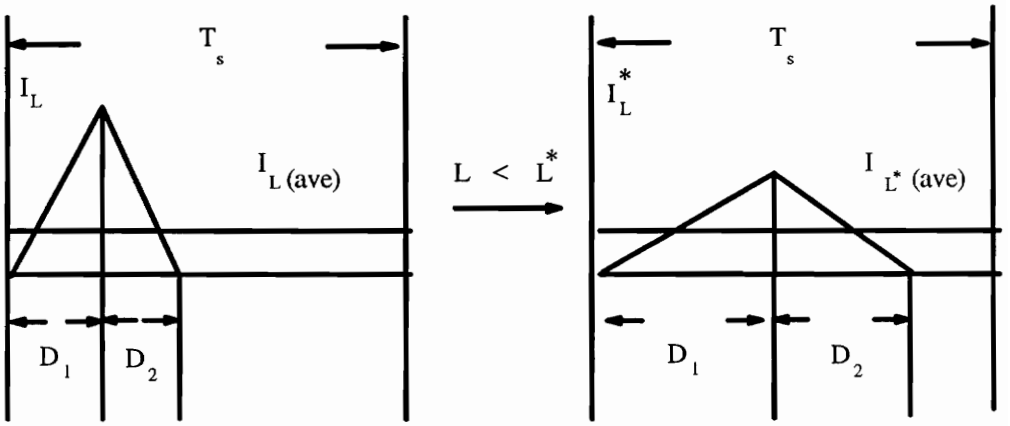

Fig.4.5 Duty ratio increases as boost inductance increases.

4.3 BULK-CAPACITOR VOLTAGE DECREASES WHEN THE BOOST CONVERTER INDUCTANCE INCREASES.

Another way to counteract the rise in bulk-capacitor voltage is to increase the inductance of the boost converter inductor at lighter loads. The on time duty cycle increases when the inductance increases. It is because the peak value of the inductor current will be smaller with higher inductance. So, for the same average input power, the boost inductor current will have a lower peak and wider base as shown in Fig.4.5. Hence, a larger on time duty ratio results. This also can be observed readily from the characteristic equation (4.4) of the boost converter inductor.

$$V_g = L\frac{I_{pk}}{D_1 \bullet T} \tag{4.4}$$

Since the input voltage V_g and the switching period T are constant, the on time duty ratio D_1 will increase when the inductance increases. Although the peak inductor current will decrease at the same time, there will be a net increase in D_1, as illustrated in the energy equation (4.5) of an inductor. Where E_L is the energy of the inductor

$$E_L = \frac{1}{2}L \bullet I^2 \tag{4.5}$$

For instance, if inductance L increases N times, the inductor current will only decrease by a factor of square root N for the same amount of energy. Hence, there will still be a net increase in the on time duty ratio as the inductance increases.

4.4 THE IMPLEMENTATION OF A VARIABLE INDUCTIVE ELEMENT.

The concept of the swinging choke as an variable inductive element is employed here. The swinging choke is designed in such a way that its inductance can swing up at lighter dc load currents. However, due to the nonlinear properties of the core materials, it is difficult to design without substantial trial and error. In order to avoid complicated issues like the finite element modeling of the inductance versus current relationship which can be another topic of its own, a simple reluctance model plus several trials and errors will be the adopted approach.

The inductance of the swinging choke varies with the bias current. This is done by exciting some part of the core at a different level than the rest of the core. One method is to use a core material such as certain ferrite core which naturally has a lower permeability at higher flux level which is close to the saturation region. But this means that the core has to be operated near saturation to have swinging in inductance. Therefore, even though this method is simple, the core loss is large. So, this method is not preferred. Another way to have a swinging choke is by cutting the core. A normal EE core is intentionally cut in the outer-leg (or the center-leg) to form a stepped gap core as shown in Fig.4.6. It is more convenient to cut the outer-leg for manufacturing purpose. But for a larger swing in inductance, the center-leg which usually has the larger cross sectional area is the one needs to be cut. Furthermore, the EE core is more convenient to do the gapping in the trials and errors process otherwise the toroidal core would be even more convenient to be used.

Suppose the EE core is cut at the center-leg as shown in Fig.4.6, the reluctance of the uncut portion of the core has smaller reluctance due to a smaller gapping. The magnetic flux will go through these smaller reluctance part of the core first. As the bias current increases, the smaller reluctance part saturates first. The magnetic flux will then spread to the stepped-gap portion of the core. The inductance then swings from a higher value to a lower value as the bias current increases. The B/H curve of the swinging choke is shown in Fig.4.7.

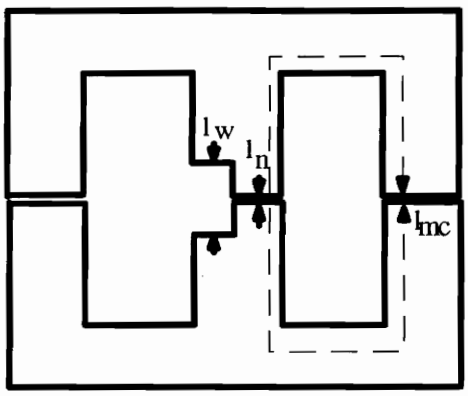

Fig.4.6 Stepped gap in the center leg of a EE core.

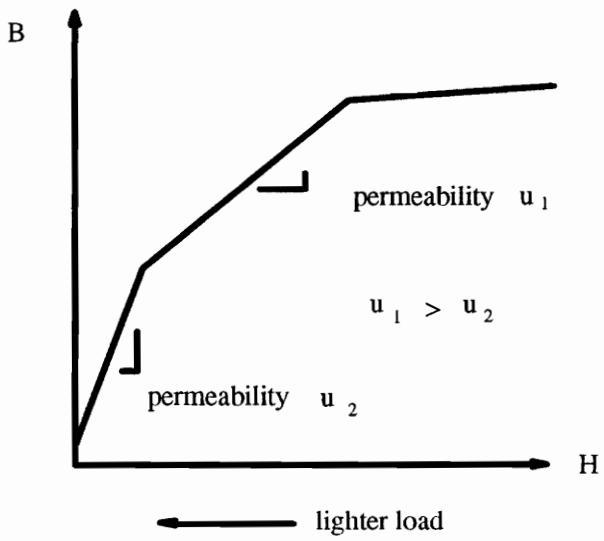

Fig.4.7 B-H curve of a swinging choke.

The required inductance swing can be designed by using the reluctance model. As an example, the magnetic circuit is based on the stepped-gap EE core structure illustrated in Fig.4.6. The step gives two air gaps. One of which is a wider gap of length l_w which covers an area of A_w. The other is a narrower gap of length l_n which covers an area of A_n. The equivalent magnetic circuit model is shown in Fig.4.8, as a series-parallel arrangement. R_{mc} consists of the main core which are the outer legs and the center one up to the air gaps. R_w and R_n consist of the wide and narrow air gap respectively. In general, the permeability of the region of the core in the immediate vicinity of the narrow gap would be less than that of the main core due to the concentration of the flux lines through the lower reluctance narrow gap. But for the sake of simplicity, it is treated as the same of the rest of the core. The reluctances are given by the following equations, as described in [7]. Where μ_g is the permeability of the air, μ_{mc} is the permeability of the core material, and A_{mc} is the area of the main core which consists of the outer legs.

$$R_{mc} = \frac{l_{mc}}{\mu_m \bullet A_{mc}} \tag{4.6}$$

$$R_w = \frac{l_w}{\mu_g \bullet A_w} \tag{4.7}$$

$$R_n = \frac{l_w - l_n}{\mu_m \bullet A_n} + \frac{l_n}{\mu_g \bullet A_n} \tag{4.8}$$

If R_P is the equivalent reluctance of the parallel branch,

$$\frac{1}{R_p} = \frac{1}{R_n} + \frac{1}{R_w} \tag{4.9}$$

Then, for a N turns winding inductor, the inductance L can be expressed in terms of the reluctance as in the following.

$$L = \frac{N^2}{R_{mc} + R_p} \tag{4.10}$$

Substitute (4.6), (4.7), and (4.8) into (4.9).

$$\frac{1}{R_p} = \frac{l_w\left((l_w - l_n)\bullet\mu_g + l_n\bullet\mu_{mc}\right)}{\mu_g\bullet\mu_{mc}\bullet A_n\bullet l_w + \mu_g\bullet A_w\left((l_w - l_n)\bullet\mu_g + l_n\bullet\mu_{mc}\right)} \tag{4.11}$$

For low applied current, μ_{mc} dominates and Rp is approximately equal to,

$$\frac{1}{R_p} \approx \frac{l_n\bullet l_w}{\mu_g\bullet\left(A_n\bullet l_w + l_n\bullet A_w\right)} \tag{4.12}$$

For structures which has a smaller wide air gap region, or $A_n\bullet l_w >> A_w\bullet l_n$, equation (4.12) further reduces to,

$$\frac{1}{R_p} \approx \frac{l_n}{\mu_g\bullet A_n} \tag{4.13}$$

This is equivalent to a structure which has just a uniform narrow gap.

As the applied current increases, the permeability of the magnetic material near the narrow gap will fall quickly due to the concentration of flux, and equation (4.11) reduces to (4.14).

$$\frac{1}{R_p} \approx \frac{l_w}{\mu_g\bullet A_w} \tag{4.14}$$

This is equivalent to a structure which has a uniform wide air gap.

Furthermore, because the boost converter must operate in discontinuous conduction mode, the inductor current needs to swing from a higher inductance value to lower inductance value even at heavy load. Therefore, the swinging choke affects the whole load range while the variable frequency control affects only lighter loads range.

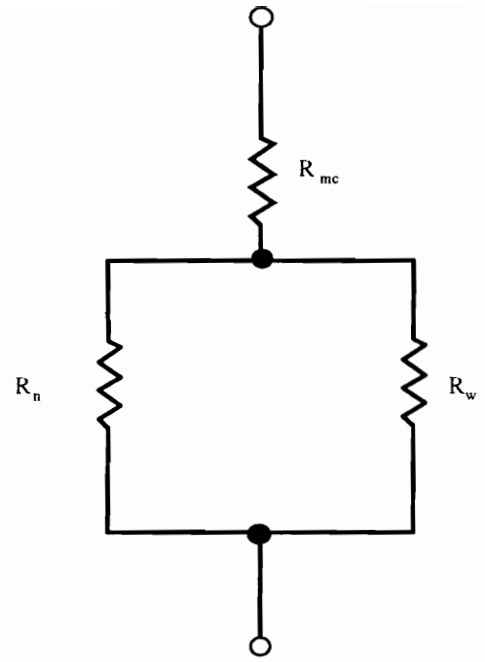

Fig.4.8 Reluctance model of the magnetic circuit in Fig.4.6.

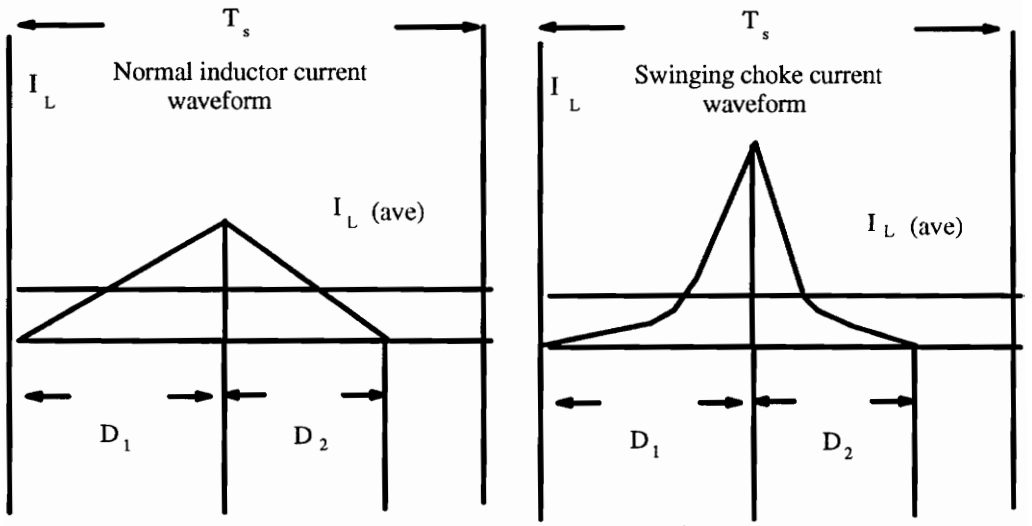

Fig.4.9 current waveforms of normal and swinging chokes.

The boost inductor current at heavy load is illustrated in Fig.4.9. In order to process the same amount of power and remain in discontinuous conduction mode, the inductor current must have a higher peak in order to process the same amount of current processed by a normal choke. The peak inductor current will be higher for a larger swing. Thus, the drawbacks in using a swinging choke are even higher current stress, higher conduction loss at full load, and larger inductor and transformer sizes. These drawbacks will be illustrated in the design example in the following chapter. The air gap widths of the swinging choke at light loads and full load can be approximated by equations (4.13) and (4.14) respectively to obtain the desired inductance swing. However, several trials and errors are needed in practice.

4.5 REDUCE THE DRAIN-TO-SOURCE VOLTAGE SPIKE BY USING A LOW LOSS LC SNUBBER.

The boost inductor current energizes the bulk capacitor when the switch is turned off. So, the transformer leakage current will be forced to reverse its direction. This creats a large voltage spike due to the high rate of change of the leakage current. This drawback applies to both the BIFRED and BIBRED converters. In order to clamp the drain-to-source voltage spike and reduce loss, a LC snubber is used to recover some energy back to the bulk capacitor, as shown in Fig.4.10.

When the switch is turned off, the leakage current charges the snubber capacitor, C_s ,through diode, D_{s1}. So, energy is returned back to the bulk capacitor, as illustrated in Fig.4.11. When the switch is turned on again, C_s and the snubber inductor, L_s, resonate through the switch and the diode, D_{s2}. The voltage of C_s is then reversed by the resonance process and is ready to receive the leakage current when the switch is turned off again, as illustrated in Fig.4.12. The voltage and current waveforms of this type of LC snubber are shown in the Pspice simulation plot of the BIBRED converter in Fig.4.13. This is the same as the first simulation in Fig.3.19 except for the LC snubber that is added.

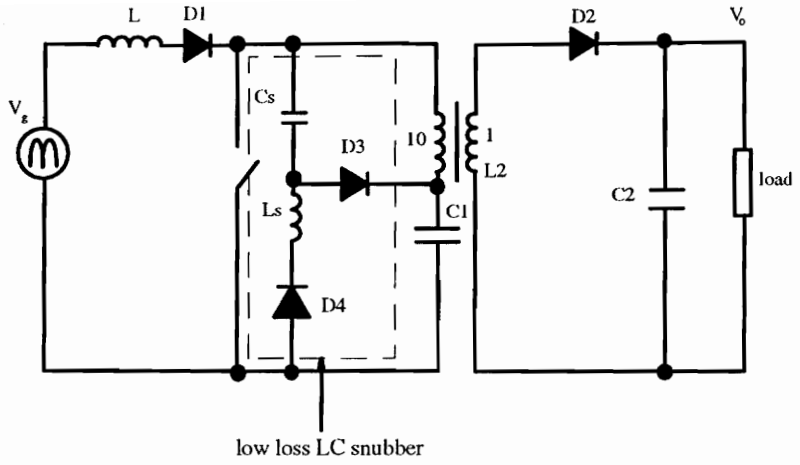

Fig.4.10 Using a LC snubber in the BIFRED converter.

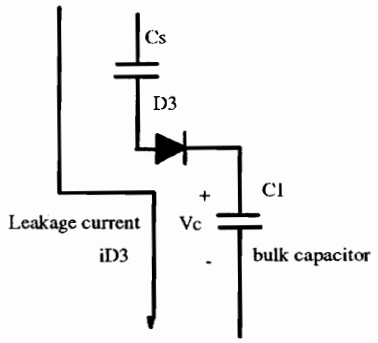

Fig.4.11 Energy returned to bulk capacitor.

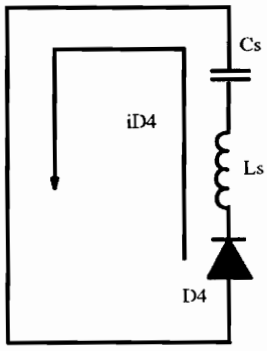

Fig.4.12 LC resonance through diode D4.

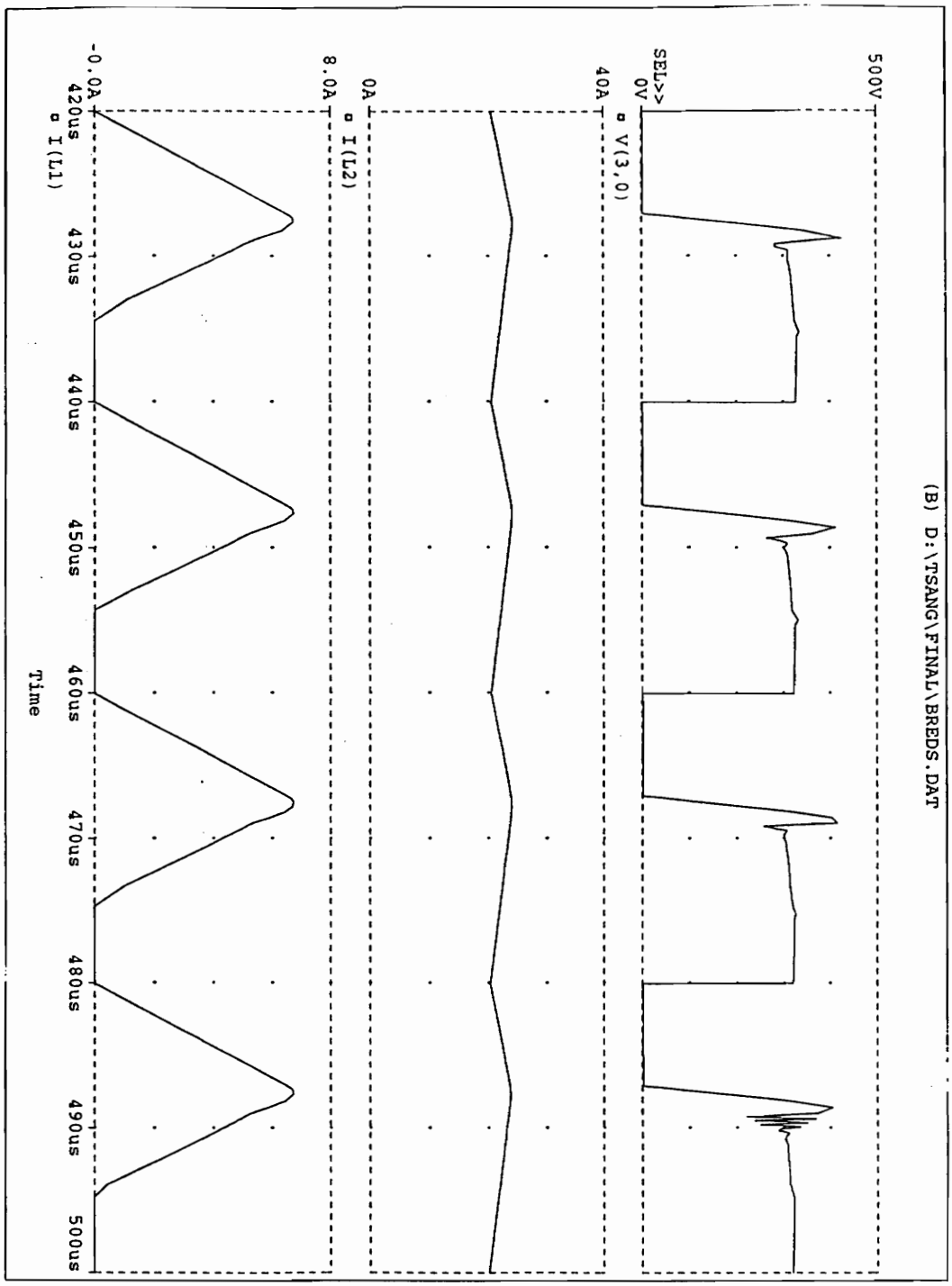

Fig.4.13 Voltage and current waveforms at switch turn-off with LC snubber.

The design equations are listed in the followings, as discussed in [8]. The maximum voltage V_{csm} of the snubber capacitor C_s is given by equation (4.15). Where n is the turns ratio of the transformer, V_o is the output voltage, L_{lk} is the leakage inductance of the transformer, and I_{pk} is the peak boost inductor current.

$$V_{csm} = n \bullet V_o + I_{pk}\sqrt{\frac{L_{lk}}{C_s}} \tag{4.15}$$

Whereas, the required snubber inductance L_s is given by,

$$L_s \geq C_s \bullet \frac{\left(n \bullet V_o + I_{pk}\sqrt{\frac{L_{lk}}{C_s}}\right)^2}{I_{LM}^{\ 2}} \tag{4.16}$$

Where L_s is the required snubber inductance. I_{LM} is the allowed peak current of the snubber inductor. It should be noticed that the capacitor must be fully discharged during switch on time and before the switch is turned off again. The timing requirement is checked by the half-cycle time of the LC resonant circuit. From [8], the time constraint T_p is given by,

$$T_p = \pi \bullet \sqrt{L_s \bullet C_s} \tag{4.17}$$

4.6 SUMMARY

Several techniques to improve the integrated high-quality rectifier-regulators are suggested and discussed in this chapter. The bulk-capacitor voltage stress can be reduced by using variable frequency control. It is found that the bulk-capacitor voltage decreases when the switching frequency increases. A voltage controlled oscillator is employed to increase the switching frequency only at lighter loads to reduce the bulk-capacitor voltage

stress. Furthermore, the bulk-capacitor voltage also decreases when the inductance of the boost inductor increases. The swinging choke is employed to obtain the inductance swing at lighter loads. However, the boost inductor current is discontinuous for the whole range of operation. The inductor current needs to have a higher peak than that in the normal choke in order to process the same amount of power. The boost inductor current peak will be higher for a larger swing of inductance. It results in even higher current stress than that in a normal DCM boost inductor. So, the swinging choke affects the whole range of operation of the converter. The swinging choke method is not as good as the variable frequency control technique. Finally, a low loss LC snubber is introduced to alleviate the drain-to-source voltage spike when the switch is turned off. The resulting voltage and current waveforms are illustrated in a PSpice simulation plot.

5. DESIGN EXAMPLES AND EXPERIMENTAL RESULTS

5.1 BIFRED CONVERTER WITH VARIABLE FREQUENCY CONTROL AND LC SNUBBER.

Specifications:

1. Input voltage : 85 to 135 Vac.
2. Output voltage : 5Vdc.
3. Load current : 1.8A to 18A.

In order to have harmonic currents which meet IEC555-2 standards, the inverse voltage gain M should be less than 0.85 at low line and full load (the line current is largest at this operating point) in order to have a PF better than 0.934 as discussed in chapter 3. M is chosen to be 0.7 to have some margin. This condition ensures the boost inductor operates in DCM and the resulting line harmonics currents will comply with the IEC555-2 standards. The turns ratio of the transformer is chosen to be 10. This is based on the fact that a larger turn ratio will give higher bulk capacitor voltage stress due to the reflected equivalent output voltage. But a smaller ratio will give smaller duty cycle and

thus higher current stress and larger conduction loss on the switch and the output diode. It is due to the higher RMS current and longer conduction period for the output diode for a smaller duty cycle. After several iterations on (3.7) and (3.5), a ratio of 10 is chosen. The switching frequency should not be too high so that the boost converter can operate in DCM and the current stress is not too high. But if the switching frequency is too low, the magnetic components will be bulky. Thus, the switching frequency is chosen to be 50KHz. Substitute these conditions into the steady state solution of the bulk capacitor voltage equation (3.7),

$$n = 10, \quad T = 20\mu\ s, \quad V_o = 5Vdc, \quad I_o = 18A, \quad M = 0.7$$

$$\frac{1}{0.7} \approx \frac{1}{2} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet 20 \bullet 10^{-6} \bullet 5}{L \bullet 18}} \right)$$

The boost inductance L needed is $= 194\mu\ H$. However, the boost inductance value in practice will be a bit lower because the converter will have losses. More input current is then needed in a real circuit for the same amount of output power. Thus, the boost inductance needs to be smaller, for example $L = 170\mu\ H$. The duty cycle can be calculated by using (3.5).

$$\frac{85}{0.7} \bullet \sqrt{2} - 5 \bullet 10 = 5 \bullet 10 \frac{(1 - D_1)}{D_1}$$

$$D_1 = 0.291$$

The peak inductor current at low line full load is calculated by equation (4.4)

$$V_g = L \frac{I_{pk}}{D_1 \bullet T}$$

$$I_{pk} \approx 3.6A$$

The second step is to find the magnetizing inductance, L_m, of the transformer. Since the flyback converter needs to operate in CCM most of the load range, L_m is obtained by the following equation determined by the DCM/CCM boundary condition. Suppose The CCM/DCM boundary is when the output current is around 2.5A. Therefore,

$$\frac{L_m}{n^2} > \frac{1}{2} \bullet (1 - D_1) \bullet T \bullet \frac{V_o}{I_o} \tag{5.1}$$

$$L_m > 1.4mH$$

L_m is chosen to be 1.5 mH. Since the duty ratio, the values of the boost inductor inductance and the magnetizing inductance of the transformer are known, the transformer and boost inductor designs are obtained readily.

The next step is to obtain the variable frequency control parameters. The difference amplifier is biased in such a way that it will give an error voltage of 0.5 Vdc to turn on the BJT when the stepped down bulk capacitor voltage is around 2.75 Vdc (refer to Fig.4.4). So, the threshold voltage is chosen to be 2.75 V. The BJT will be saturated when the base drive voltage is around 4.5 Vdc. The maximum switching frequency can be obtained by adjusting the potentiometer which biases the BJT. The maximum frequency is chosen to be 200K Hz. It is desired to start changing the switching frequency when the capacitor voltage is around 200 Vdc. The bulk capacitor voltage is then stepped down to 2.75 Vdc by a voltage divider. The highest frequency will be at high line and the output current is around 2.5 A. The maximum drain to source voltage of the MOSFET is chosen to be 350 Vdc. Since the flyback converter will enter into DCM when the output current drops below 3 A, the bulk capacitor voltage will stop increasing as the load current decreases further. The highest frequency F_s can be calculated again by using equation (3.7).

$$\frac{350}{135} \approx \frac{1}{\sqrt{2}} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet T \bullet 5}{194 \bullet 10^{-6} \bullet 2.5}} \right)$$

$$F_s \approx 140KHz$$

The drain to source voltage of the MOSFET will be around 510 Vdc without changing the frequency. There is a 160 Vdc reduced in bulk-capacitor voltage stress. A MOSFET of 500 V rating can be used instead of a 700 or 800 V rating one (power MOSFET usually come in 500 V, 800 V, 900 V cases) for a 25% safety margin.

Finally, it comes to the LC snubber design. If the maximum snubber capacitor voltage is allowed to be 130 V, so the peaking at the turn off instant is allowed to be 80V. Suppose the leakage inductance of the transformer is 7.5μ H. Thus, C_s can be obtained by (4.15).

$$130 = 50 + 3.6\sqrt{\frac{7.5\mu\ H}{C_s}}$$

$$C_S = 16nF$$

The peak current of the snubber inductor is chosen to be 5A. The snubber inductance L_s can be calculated by equation (4.16)

$$L_s \geq 16nF \bullet \frac{\left(50 + 3.6\sqrt{\frac{7.5\mu\ H}{16nF}}\right)^2}{5^2}$$

$$L_s \geq 11\mu\ H$$

Since the snubber capacitor has to be fully discharged during the on time of the switch, the time constraint T_p is checked given by equation (4.17).

$$T_p = \pi \bullet \sqrt{15\mu\ H \bullet 16nF}$$

$$T_p = 1.54\mu\ s$$

The on time is at least $5.8\mu\ s$, as obtained from above. So, the snubber capacitance and inductance parameters meet the requirement. The experimental results of this prototype are presented at the end of this chapter.

5.2 BIBRED CONVERTER WITH VARIABLE FREQUENCY CONTROL AND LC SNUBBER.

Specifications:

1. Input voltage : 85 to 270 Vac.
2. Output voltage : 5Vdc.
3. Load current : 1.8A to 18A.

The highest input current (and harmonics currents) is at low line and full load. Since the steady state solution of the BIBRED converter is the same as the BIFRED converter, the steps to obtain the value of the inductance of the boost inductor is the same. The process is therefore not repeated here. The parameters obtained from the previous example are listed as in the followings. Substitute these conditions into the steady state solution of the bulk capacitor voltage equation (3.7),

$$n = 10, \quad T = 20\mu\ s, \quad V_o = 5Vdc, \quad I_o = 18A, \quad M = 0.7$$

$$\frac{1}{0.7} \approx \frac{1}{2} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet 20 \bullet 10^{-6} \bullet 5}{L \bullet 18}} \right)$$

The boost inductance L needed is $= 194\mu\ H$.

The duty cycle can be calculated by using (3.5).

$$D_1 = 0.291$$

The peak inductor current at low line full load is calculated by equation (4.4)

$$V_g = L\frac{I_{pk}}{D_1 \bullet T}$$

$$I_{pk} \approx 3.6A$$

The next step is to obtain the variable frequency control parameters. As in the previous example, the threshold is around 2.75 V. The maximum frequency is chosen to be 200 K Hz. It is desired to start changing the switching frequency when the bulk capacitor voltage is at around 450 Vdc. The bulk capacitor voltage is then stepped down to 2.75 V by a voltage divider. The highest switching frequency will be at high line and output current at around 2.5 A. The maximum drain-to-source voltage of the MOSFET is chosen to be 680 Vdc. Since the modified forward converter will enter into DCM when the output current drops below 2.5 A, the bulk-capacitor voltage will stop increasing as the load current decreases further. The highest switching frequency F_s can be calculated again by using equation (3.7).

$$\frac{680}{270} \approx \frac{1}{\sqrt{2}} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet T \bullet 5}{194 \bullet 10^{-6} \bullet 2.5}}\right)$$

$$F_s \approx 157KHz$$

The drain-to-source voltage will be around 1020 Vdc without variable frequency control. There is a 340 V reduced in bulk-capacitor voltage stress accordingly. A MOSFET of 800 V rating can be used instead of a 1200 V rating one for a 15% safety margin.

Finally, the LC snubber design procedures is the same as in the previous example. So, it is not repeated here. The, C_s and L_s obtained are 30 nF and 20μ H respectively for a leakage inductance of 8μ H. The experimental results of this prototype are presented at the end of this chapter.

5.3 BIBRED CONVERTER WITH VARIABLE FREQUENCY CONTROL, SWINGING CHOKE, AND LC SNUBBER.

Specifications:

1. Input voltage : 85 to 135Vac.
2. Output voltage : 5Vdc.
3. Load current : 1.8A to 10A.

For a normal boost inductor the steps to obtain the value of the inductance of the boost inductor is the same as the one in the first example. The detailed discussion is therefore not repeated here. The parameters obtained from he previous example are listed as in the followings. Substitute these conditions into the steady state solution of the bulk capacitor voltage equation (3.7),

$$n = 10, \quad T = 20\mu\ s, \quad V_o = 5Vdc, \quad I_o = 10A, \quad M = 0.7$$

$$\frac{1}{0.7} \approx \frac{1}{2} \bullet \left(1 + \sqrt{1 + \frac{0.852 \bullet 10^2 \bullet 20 \bullet 10^{-6} \bullet 5}{L \bullet 10}} \right)$$

The boost inductance L needed is $= 348\mu\ H$.

The duty cycle can be calculated by using (3.5).

$$D_1 = 0.291$$

The peak inductor current at low line full load is calculated by equation (4.4)

$$V_g = L \frac{I_{pk}}{D_1 \bullet T}$$

$$I_{pk} \approx 2A$$

For the swinging choke design , it is chosen to have a 1.5 times inductance increase when the load current is below 4 A. The averaged inductor current is therefore equal to 0.4 A. The bulk capacitor voltage at this operating point is found by,

$$\frac{V_c+50}{85} \approx \frac{1}{\sqrt{2}} \bullet \left(1+\sqrt{1+\frac{0.852 \bullet 10^2 \bullet 20 \bullet 10^{-6} \bullet 5}{576 \bullet 10^{-6} \bullet 4}} \right)$$

$$V_c \approx 140V$$

$$D_1 = 0.263$$

For DCM boost inductor,

$$\frac{V_{ob}}{V_g} = 1+\frac{D_1}{D_2}$$

$$D2 = 0.45$$

The swinging choke must process the same average current as the normal boost inductor. As shown in Fig.4.5, the averaged current is contributed by the higher inductance which has a smaller slope at the sides and the lower inductance with a steeper slope in the middle. The higher inductance carries only 0.4 A as discussed in the previous calculation.. The rest of the current needs to be contributed by the lower inductance portion. The peak of the inductor current is approximated by ,

$$I_{pk} \approx \frac{0.6 \bullet 2}{(1-0.45-0.263)}$$

$$I_{pk} \approx 4.1A$$

Assume the duty ratio is the same as the one in the normal boost inductor, the required inductance is given by equation (4.4),

$$120 = L\frac{4.1}{0.291 \bullet 20\mu}$$

$$L \approx 170\mu\ H$$

Therefore, 40% of the swinging choke cross sectional area needs an air gap which gives 510μH and 60% of the cross sectional area which has a gap to produce 170μH. The effect of the swing in inductance is the same as the increase in switching frequency. Therefore, when the swinging choke and variable frequency control are both used, the switching frequency will decrease by the same factor of the increase in boost converter inductance when the load current is below 4A. For instance, the 1.5 times increase in boost inductance at light load should reduce the switching frequency from 100KHz to about 70KHz.

Finally, variable frequency control design and the LC snubber design procedures are similar to the previous examples. So, they are not repeated here. The maximum drain-to-source voltage is around 300 V. The, C_s and L_s obtained are 30nF and 20μ H respectively for a leakage inductance of 8μ H. The experimental results of this prototype are presented in the next chapter.

5.4 EXPERIMENTAL RESULTS

The specifications of the prototypes are listed in the followings.

5.4.1 BIFRED converter with variable frequency control and LC snubber.

Input voltage range: 85 to 135 Vac.
Output voltage: 5 Vdc.
Load range: 1.8 to 18 A.
Switching frequency range: 50 to 125K Hz.

Maximum drain to source voltage of the switch: 350 Vdc.

5.4.2 BIBRED converter with variable frequency control and LC snubber.

Input voltage range: 85 to 135 Vac.
Output voltage: 5 Vdc.
Load range: 1.8 to 18 A.
Switching frequency range: 50 to 125K Hz.
Maximum drain to source voltage of the switch: 350 Vdc.

5.4.3 BIBRED converter with variable frequency control and LC snubber.

Input voltage range: 85 to 270 Vac.
Output voltage: 5 Vdc.
Load range: 1.8 to 18 A.
Switching frequency range: 50 to 125K Hz.
Maximum drain to source voltage of the switch: 680 Vdc.

5.4.4 BIBRED converter with variable frequency control, LC snubber, and swinging choke.

Input voltage range: 85 to 135 Vac.
Output voltage: 5 Vdc.
Load range: 1.8 to 10 A.
Switching frequency range: 50 to 75K Hz.
Maximum drain to source voltage of the switch: 300 Vdc.

Table 5.1 BIFRED experimental data (full load = 90W)

	Vin=85vAC	Vin=110vAC	Vin=135vAC
Pin (w)	130.49	125.76	124.24
Vo (v)	4.99	4.99	4.99
Io (A)	17.936	17.926	17.926
Po (w)	89.5	89.45	89.45
Eff. n(%)	68.58	71.12	71.99
1st (A)	1.52	1.138	0.9219
3rd (%)	17.13	16.84	16.72
5th (%)	3.58	2.715	3.25
7th (%)	2.1	2.3	2.78
Fs (KHz)	50.0	50.0	50.0

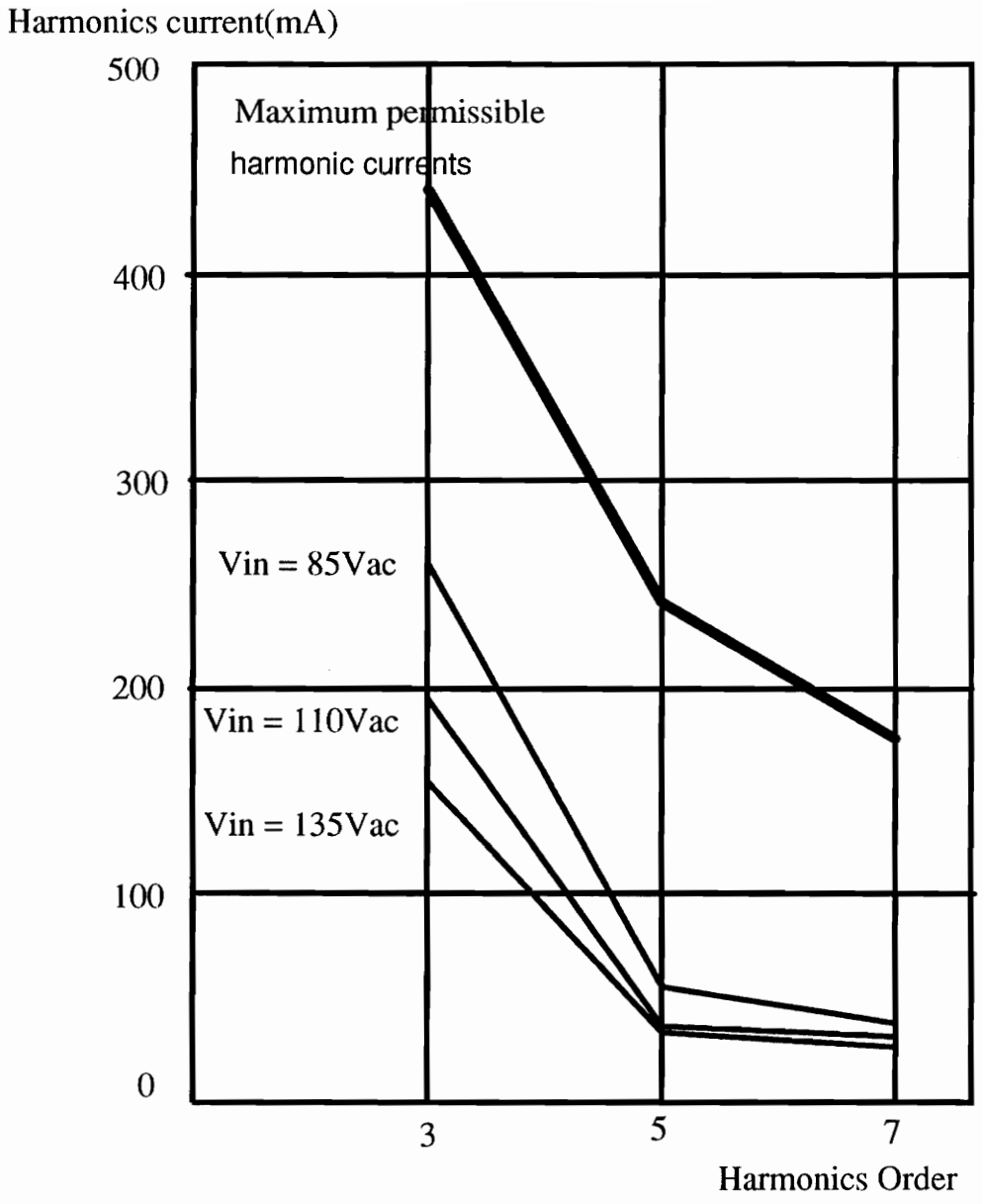

Fig.5.1 BIFRED converter harmonics currents at full load.

Table 5.2 BIFRED experimental data (10% load = 9W)

	Vin=85vAC	Vin=110vAC	Vin=135vAC
Pin (w)	19.58	25.13	30.86
Vo (v)	5.01	5.01	5.01
Io (A)	1.7958	1.7948	1.7946
Po (w)	8.997	8.99	8.99
Eff. n(%)	45.94	35.78	29.13
1st (A)	0.2318	0.2296	0.2312
3rd (%)	15.67	16.65	17.62
5th (%)	4.843	4.13	3.92
7th (%)	3.51	3.125	2.52
Fs (KHz)	62.5	71.5	91.0

Table 5.3 BIBRED experimental data (full load = 90W)

	Vin=85Vac	Vin=110Vac	Vin=135Vac
Pin(W)	126.01	122.81	122.48
V0(V)	5.0	4.99	4.99
Io(A)	18.0	17.97	17.967
Po(W)	90.0	89.67	89.66
Eff.n(%)	71.4	73.0	73.2
1st(A)	1.478	1.119	0.914
3rd(%)	18.86	20.1	20.4
5th(%)	3.02	2.65	2.78
7th(%)	2.502	2.7	2.88
PF	0.98	0.978	0.979
Fs(KHz)	50.0	50.0	50.0

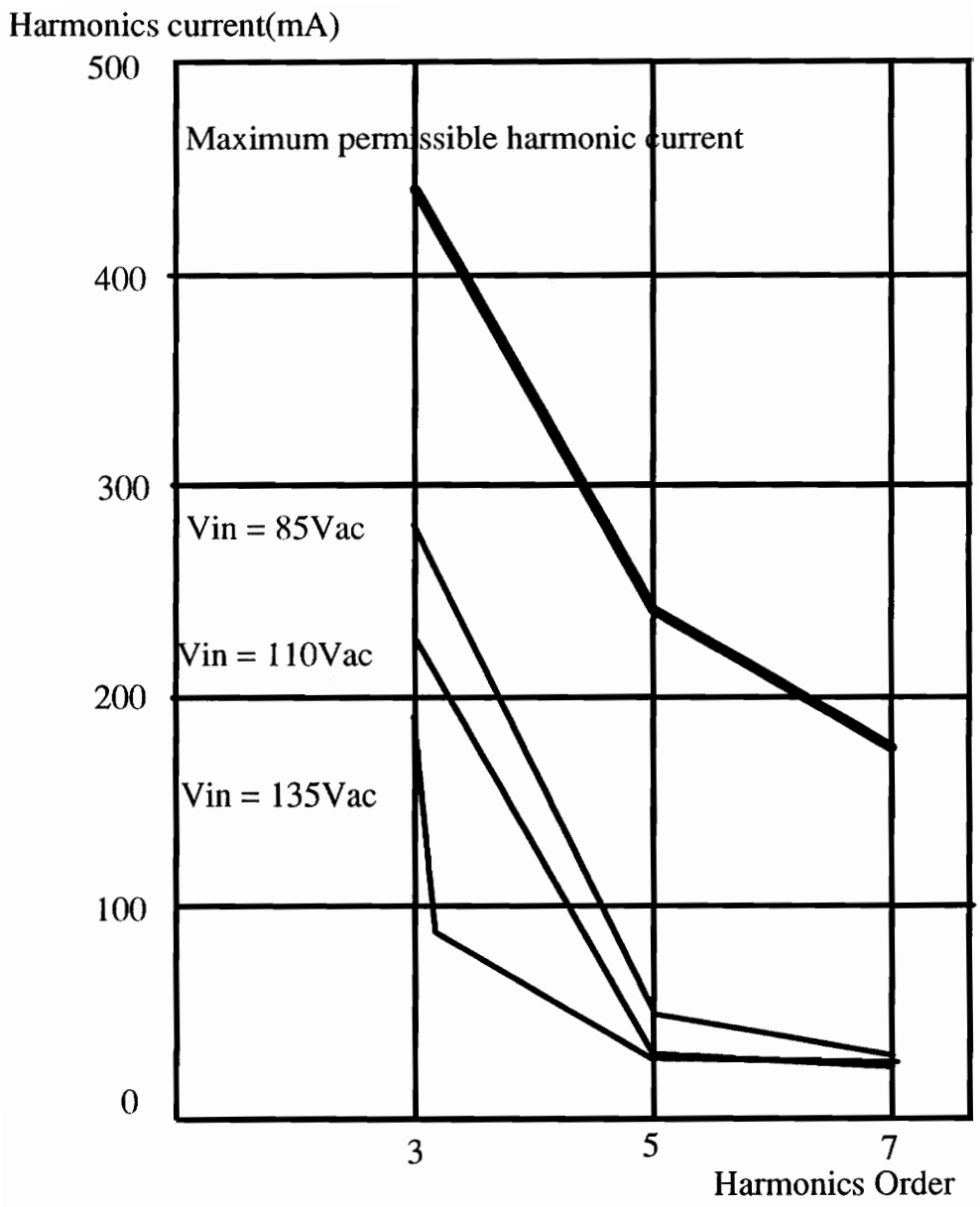

Fig.5.2 BIBRED converter harmonics currents at full load.

Table 5.4 BIBRED data at full load and with universal input.

	Vin=85Vac	Vin=170Vac	Vin=270Vac
Pin(W)	134.34	127.35	140.85
V0(V)	4.99	4.99	4.99
Io(A)	17.971	17.95	17.952
Po(W)	89.55	89.57	89.58
Eff.n(%)	66.7	70.3	63.6
1st(A)	1.579	0.7465	0.529
3rd(%)	20.4	21.46	23.17
5th(%)	4.0	2.413	3.26
7th(%)	2.48	2.363	2.043
PF	0.974	0.974	0.957
Fs(KHz)	50.0	50.0	54.0

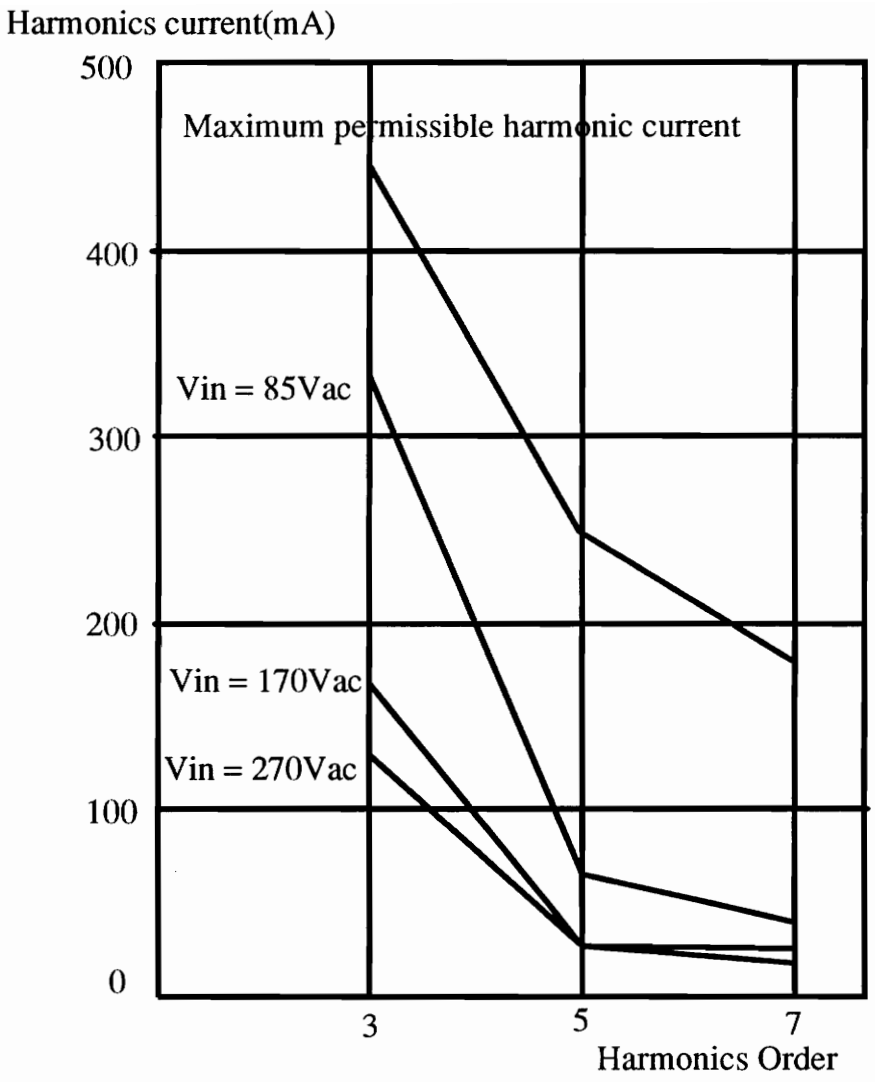

Fig.5.3 BIBRED converter harmonics currents at full load and universal input.

Table 5.5 BIBRED data with normal choke.

	Vin=85Vac	Vin=135Vac
Fs(KHz)	50.0	50.0
PF	0.973	0.948
Vds(V)	180.0	280.0
Eff.(%)	72.9	73.2
Io(A)	10.0	10.05
Vo(V)	5.01	5.01

a. BIBRED WITH NORMAL CHOKE (Po=50W)

	Vin=85Vac	Vin=135Vac
Fs(KHz)	50.0	104.0
PF	0.98	0.928
Vds(V)	240.0	320.0
Eff.(%)	63.1	45.2
Io(A)	1.816	1.814
Vo(V)	5.03	5.03

b. BIBRED WITH NORMAL CHOKE (Po=9W)

Table 5.6 BIBRED data with swinging choke.

	Vin=85Vac	Vin=135Vac
Fs(KHz)	50.0	50.0
PF	0.947	0.948
Vds(V)	180.0	280.0
Eff.(%)	71.2	72.9
Io(A)	10.0	10.05
Vo(V)	5.0	5.01

a. BIBRED WITH SWINGING CHOKE(Po=50W)

	Vin=85Vac	Vin=135Vac
Fs(KHz)	50.0	79.4
PF	0.975	0.903
Vds(V)	220.0	320.0
Eff.(%)	65.4	49.2
Io(A)	1.805	1.805
Vo(V)	5.03	5.03

b. BIBRED WITH SWINGING CHOKE (Po=9W)

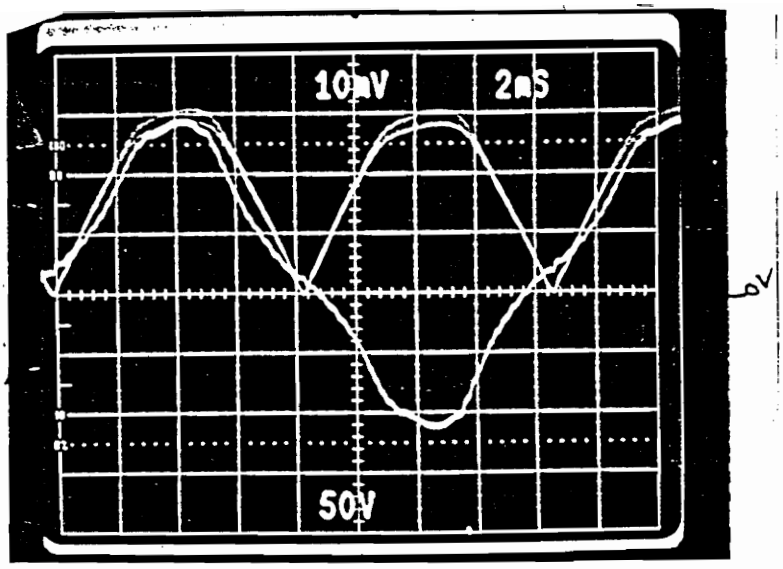

Fig. 5.4 Closed loop line current and line voltage of a BIFRED converter.

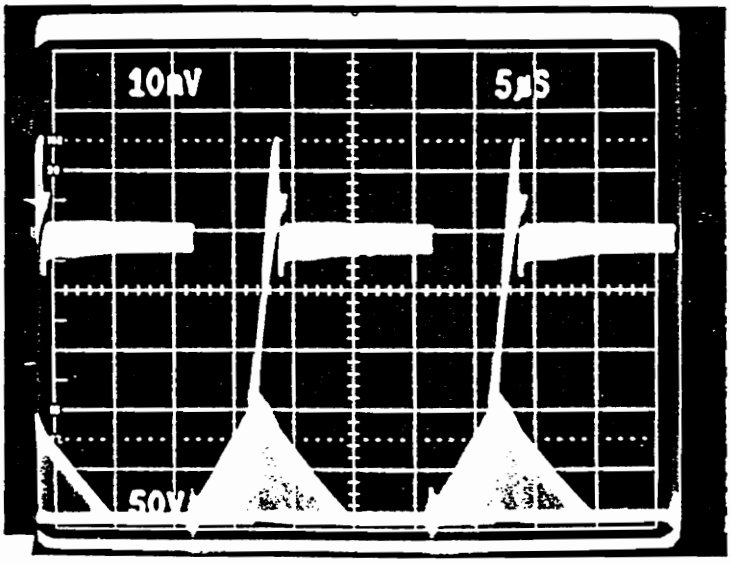

Fig. 5.5 Drain-to-source voltage and boost inductor current of a BIFRED converter.

Vin=110 Vac, output power=55 W, output voltage=5 V, switching frequency=50K Hz

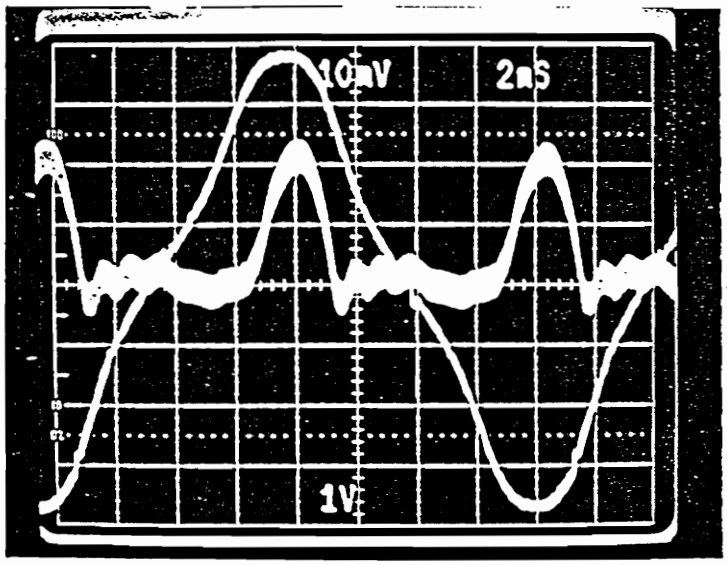

Fig. 5.6 Opened loop line current and output voltage of a BIBRED converter.

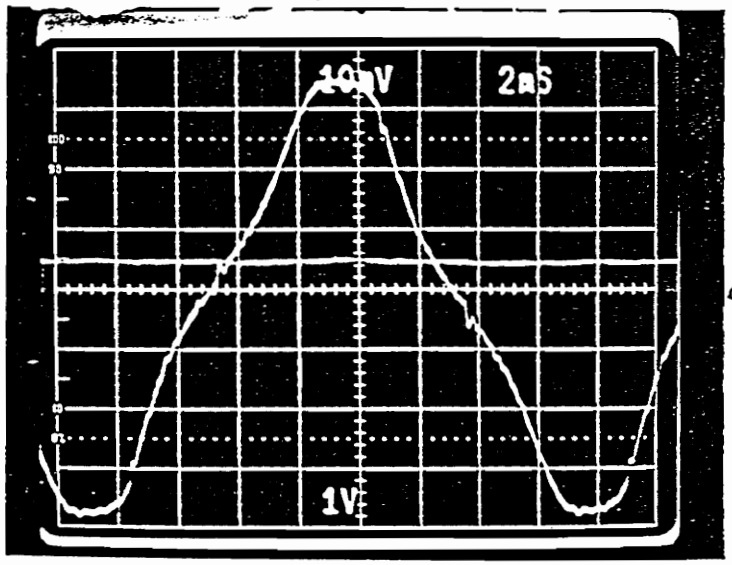

Fig. 5.7 Closed loop line current and output voltage a BIBRED converter.

Vin=110 Vac, output power=40 W, output voltage=20 V, switching frequency=50K Hz

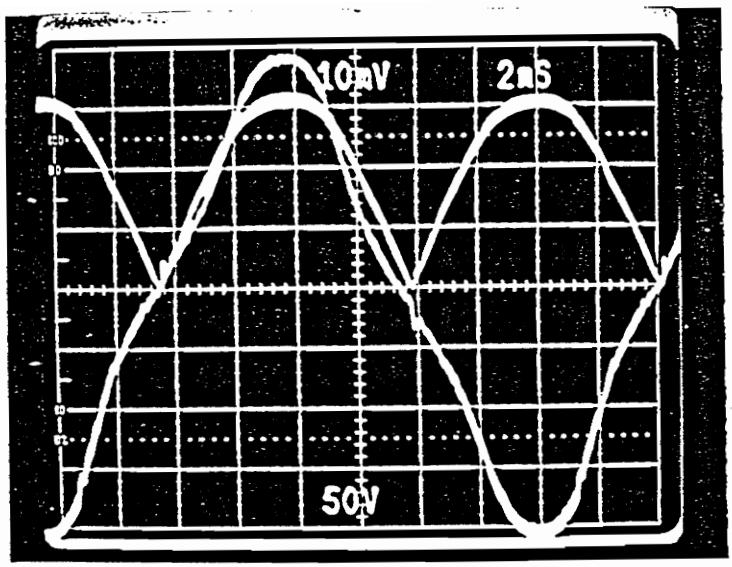

Fig. 5.8 Opened loop line current and line voltage of a BIBRED converter.

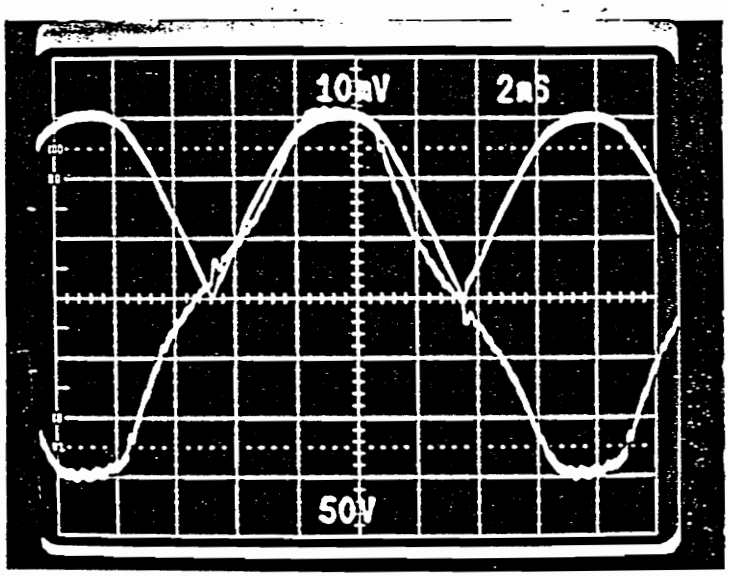

Fig. 5.9 Closed loop line current and line voltage of a BIBRED converter.

Vin=110 Vac, output power=40 W, output voltage=20 V, switching frequency=50K Hz

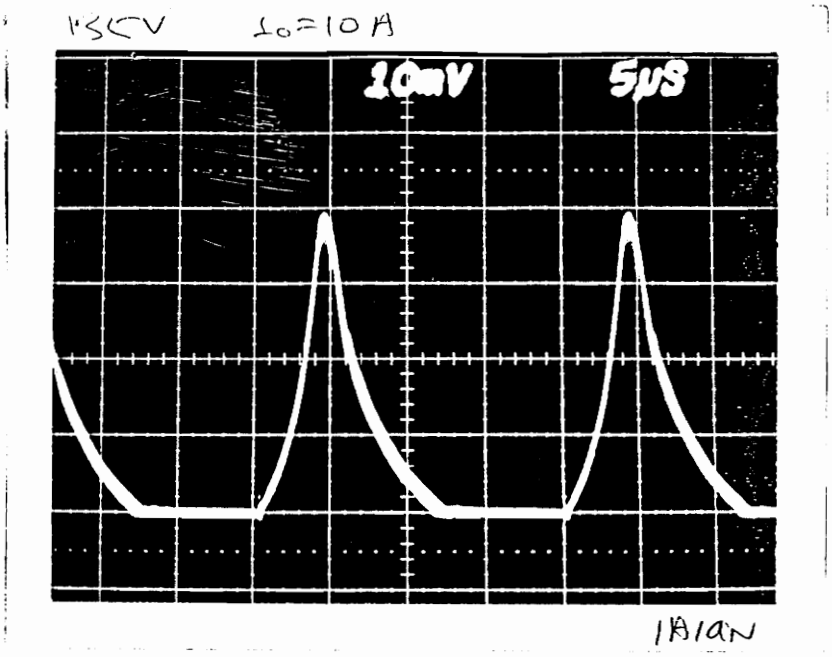

Fig. 5.10 Boost inductor current of a BIBRED converter with swinging choke.

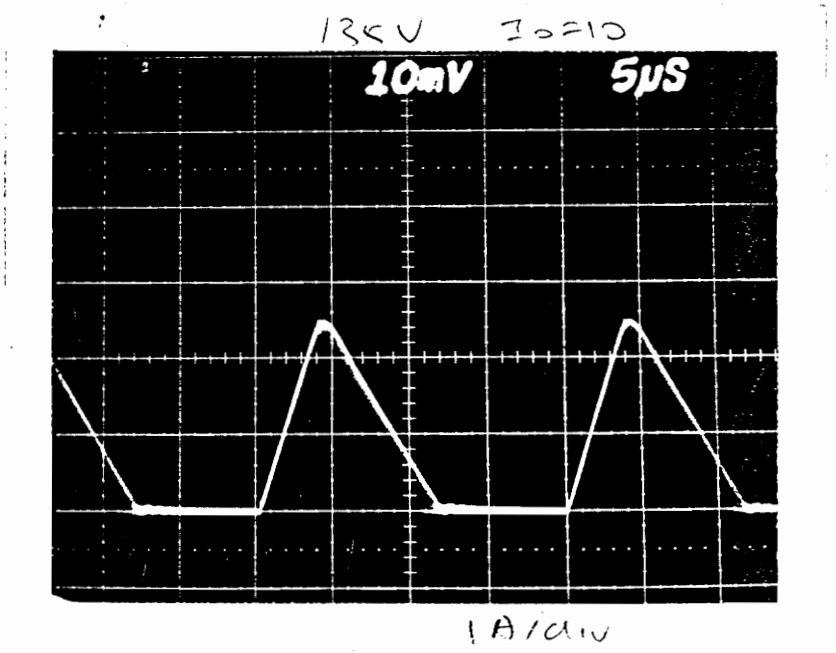

Fig. 5.11 Boost inductor current of a BIBRED converter with normal choke.

Vin=135 Vac, output power=50 W, output voltage=5 V, switching frequency=50K Hz

6. CONCLUSIONS

The bulk-capacitor voltage of the integrated high-quality rectifier-regulators is load dependent. This load dependency causes a high bulk-capacitor voltage stress at lighter loads. This represents a severe drawback in terms of cost and size. As a result, the load range and the input voltage range are limited, rendering the integrated high-quality rectifier-regulators not practical especially for applications with universal input-voltage range and wide load range. In addition, this power factor correction technique suffers from high-voltage spike on the switch at turn-off. However, the bulk-capacitor voltage stress can be reduced by increasing the switching frequency at lighter loads. The bulk-capacitor voltage stress can also be reduced by increasing the DCM boost inductance at lighter loads. In this thesis, the variable frequency control, swinging choke, and low loss LC snubber techniques are proposed to alleviate these problems. Furthermore, the performance of the integrated high-quality rectifier-regulators with respect to the IEC555-2 standards is discussed and illustrated by examples. An algorithm is outlined to help design the circuit which is able to meet the IEC555-2 standards.

Finally, four prototypes are built and tested. They are evaluated with respect to efficiency and ability to meet the IEC555-2 standards. All of the prototypes employ the variable frequency control and low loss LC snubber technique. The first two prototypes are 90W BIFRED and 90 W BIBRED converters. The input and output voltages of both converters are 85 to 135 Vac, and 5 V. The bulk-capacitor voltage stresses of both converters at high line and 10% load are reduced by 150V as opposed to the fixed-frequency counterparts. The switching frequency swings from 50K Hz to 125K Hz for both converters. The third prototype is a 90 W BIBRED converter with universal input-voltage range and 5 V output. The bulk capacitor-voltage stress at high line and 10% load is reduced by 340 V as opposed to the fixed-frequency counterpart. The switching frequency swings from 50K Hz to 125K Hz. The fourth prototype is a 50 W BIBRED converter using swinging choke. The input and output voltages are 85 to 135 Vac, and 5 V respectively. The bulk-capacitor voltage stress is reduced by 200 V as opposed to the fixed-frequency and normal choke counterpart. The switching frequency swings from 50K Hz to 75K Hz. The switching frequency is reduced by 25K Hz, but with a double input inductor current stress as opposed to the variable frequency and normal choke counterpart. All of the prototypes meet the IEC555-2 standards

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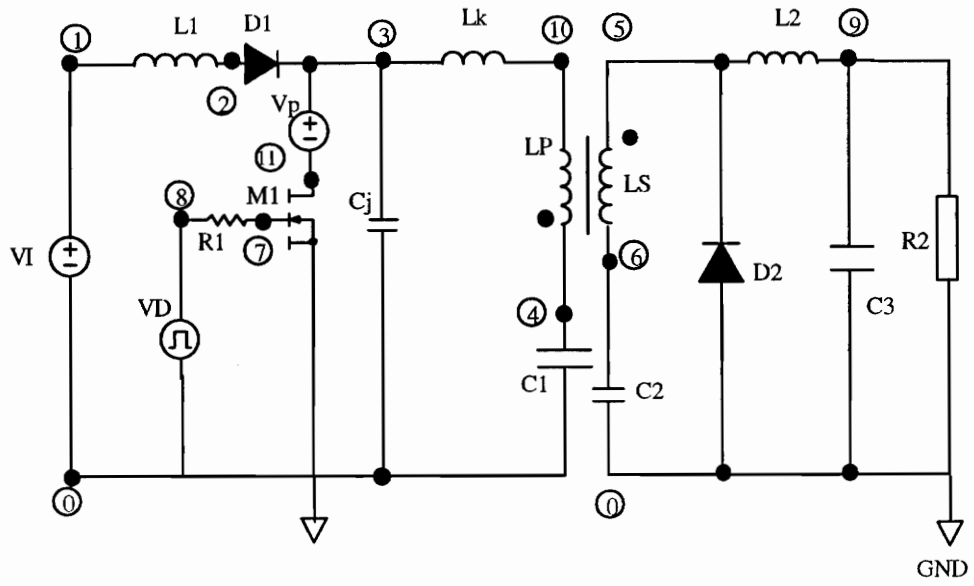
APPENDIX A. Pspice computer programs

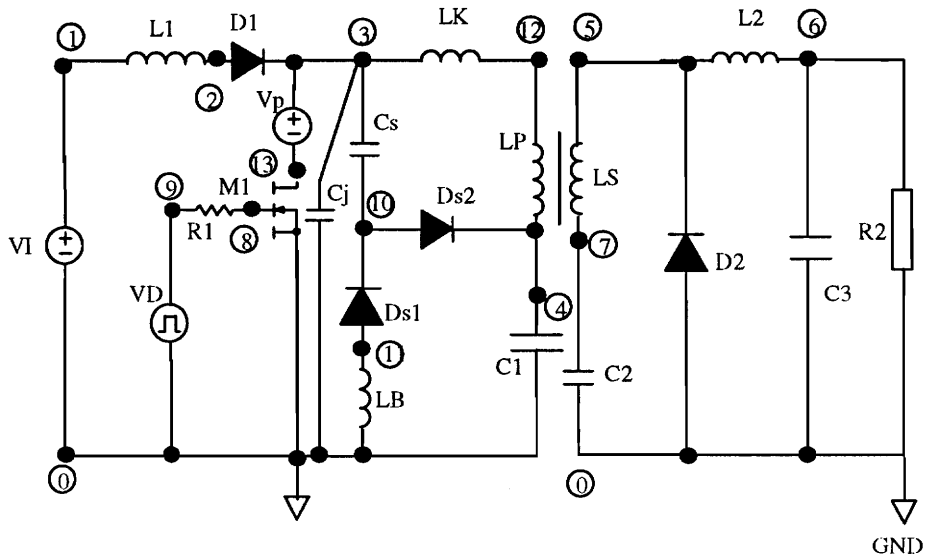
A.1 Pspice computer program on a BIBRED converter.

```
* BIBRED CONVERTER
VI 1 0 150
VD 8 0 PULSE (0 12 0 50ns 50ns 7us 20us)
R1 7 8 5
L1 1 2 160uH IC=1A
Lk 3 10 7.5uH
Cj 3 0 150pF
D1 2 3 DIODE
C1 4 0 100uF IC=200V
Vp 3 11 DC 0
M1 11 7 0 0 MOSFET
.MODEL MOSFET NMOS (VTO=4 KP=15.5 RD=0.2)
LP 4 10 1mH
LS 5 6 10uH
K LP LS 0.99999
C2 6 0 80uF
D2 0 5 DIODE
.MODEL DIODE D
L2 5 9 40uH
C3 9 0 100uF IC=5V
R2 9 0 0.5
.TRAN 1us 0.5ms 20us UIC
.PROBE
.END
```



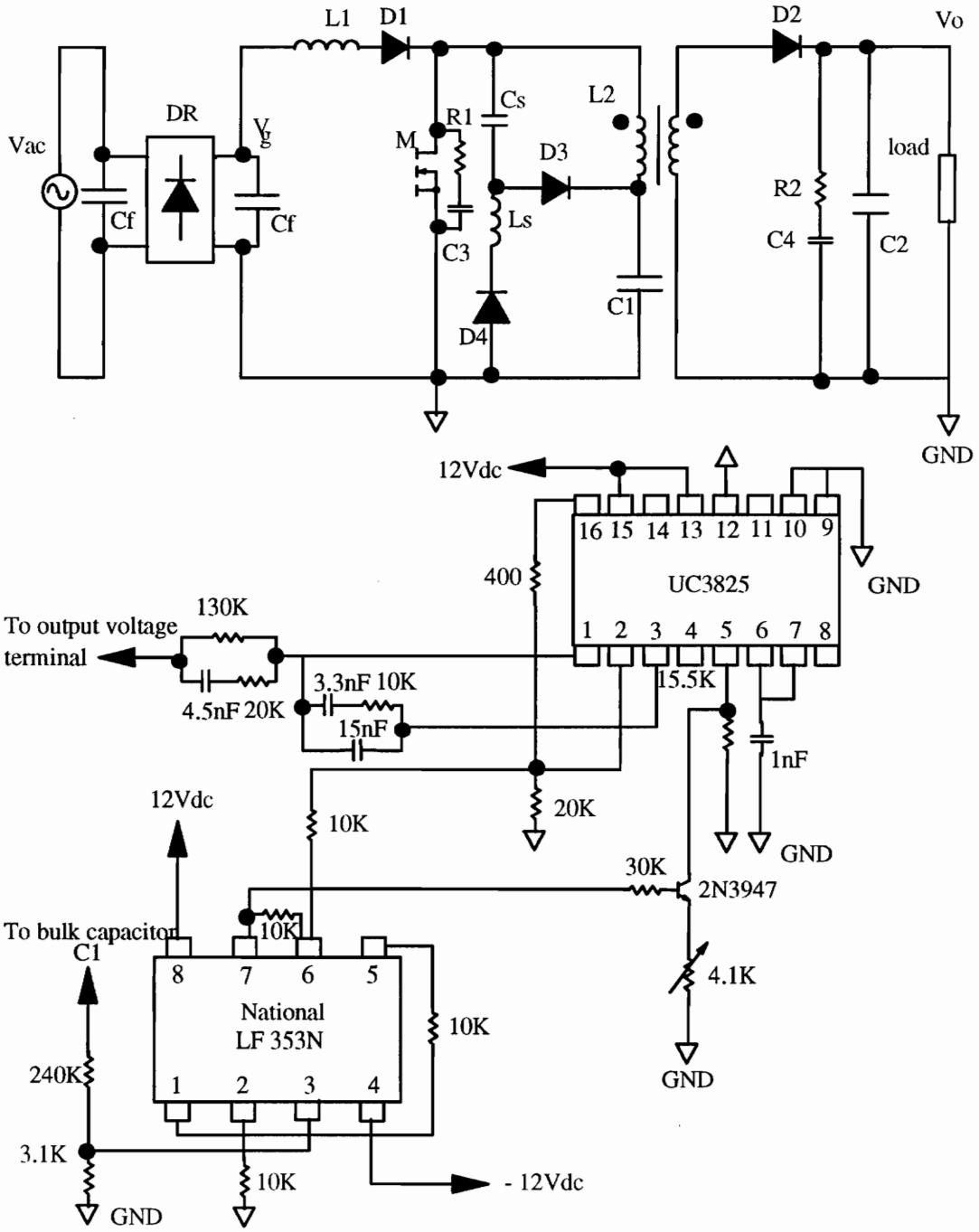
A.2 Pspice computer program on a BIBRED converter with LC snubber.

```
* BIBRED CONVERTER
VI 1 0 150
VD 9 0 PULSE (0 12 0 50ns 50ns 7us 20us)
R1 8 9 5
L1 1 2 160uH IC=1A
Lk 3 12 7.5uH
Cj 3 0 150pF
D1 2 3 DIODE
C1 4 0 100uF IC=200V
Vp 3 13 DC 0
M1 13 8 0 0 MOSFET
.MODEL MOSFET NMOS (VTO=4 KP=15.5 RD=0.2)
LP 4 12 1mH
LS 5 7 10uH
K LP LS 0.99999
C2 7 0 80uF
D2 0 5 DIODE
Cs 3 10 33nF
LB 11 0 40uH
Ds1 11 10 DIODE
Ds2 10 4 DIODE
.MODEL DIODE D
L2 5 6 40uH
C3 6 0 100uF IC=5V
R2 6 0 0.5
.TRAN 1us 0.5ms 20us UIC
.PROBE
.END
```



APPENDIX B. Circuit Schematics and Component Lists.

B.1 BIFRED converter with variable frequency control and LC snubber



Specifications:

Input voltage range: 85 to 135 Vac.

Output voltage: 5 Vdc.

Load range: 1.8 to 18 A.

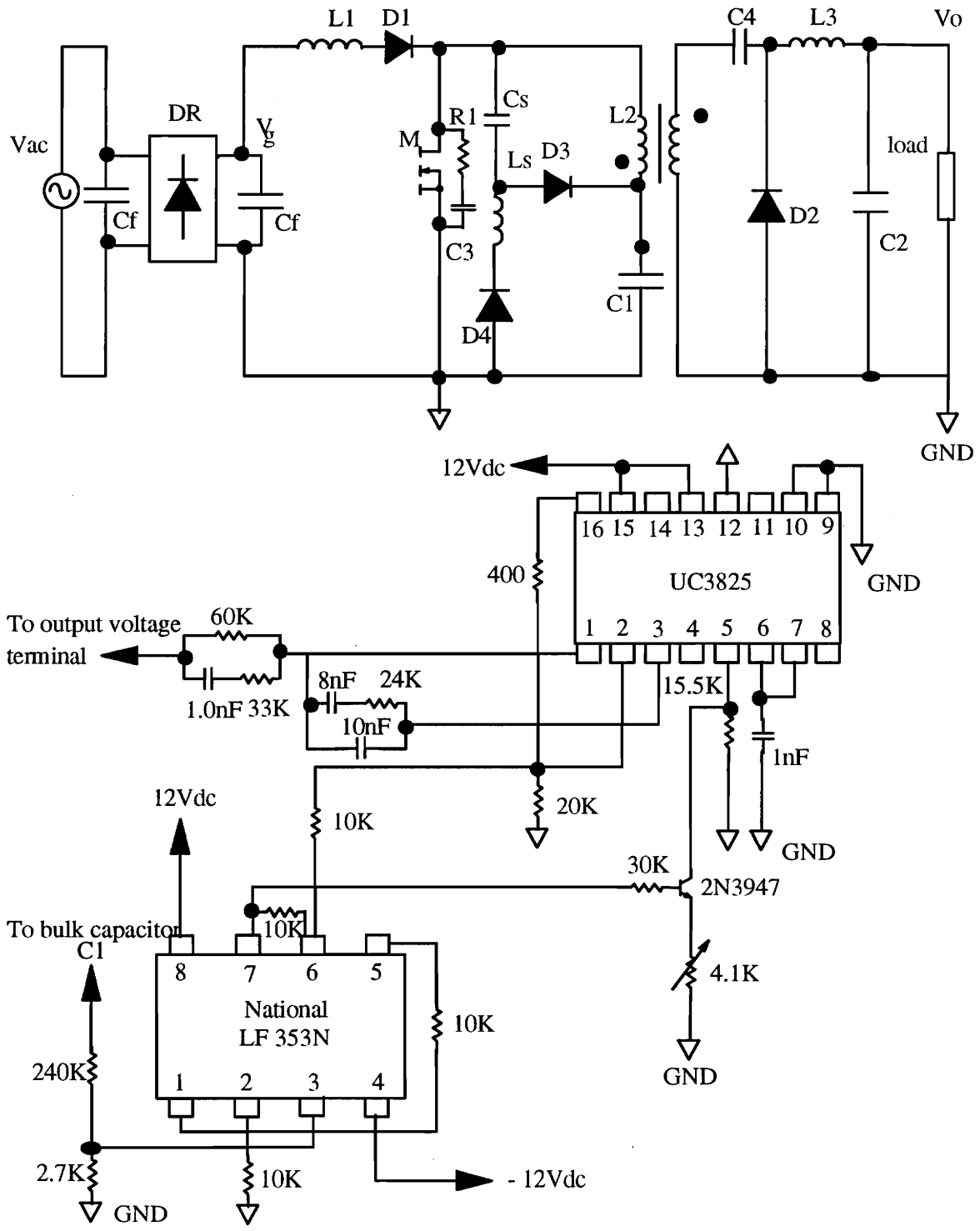
Switching frequency range: 50 to 125K Hz.

Maximum drain to source voltage of the switch: 350 Vdc.

Components:

1. M : IRFP450.
2. L1 : TDK EEC28L, #22 windings, (22 turns), inductance- 200uH.
3. L2 : TDK PC40 2205Z, primary windings- #27, (54 turns), secondary- 3 mil copper foil, 5 turns. Magnetising inductance- 1.15mH.
4. Ls : Magnetic 547L 55353-A2, 25uH.
5. D1 : PH BYT79.
6. D2 : PH BYV143.
7. D3 : PH BYM26C.
8. D4 : PH BYT79.
9. Cs : 400 V, 0.4uF.
10. Cf : 400 V, 0.47uF.
11. C1 : 450V, 330uF.
12. C2 : OSCON 16V, 100uF X2.
13. C3 : 630 V, 0.5nF.
14. C4 : 1nF.
15. R1 : 260 ohm.
16. R2 : 120ohm.
17. DR: KBU8J GI9206.
18. UC3825.
19. LF353N.

B.2 BIBRED converter with variable frequency control and LC snubber



Specifications:

Input voltage range: 85 to 135 Vac.

Output voltage: 5 Vdc.

Load range: 1.8 to 18 A.

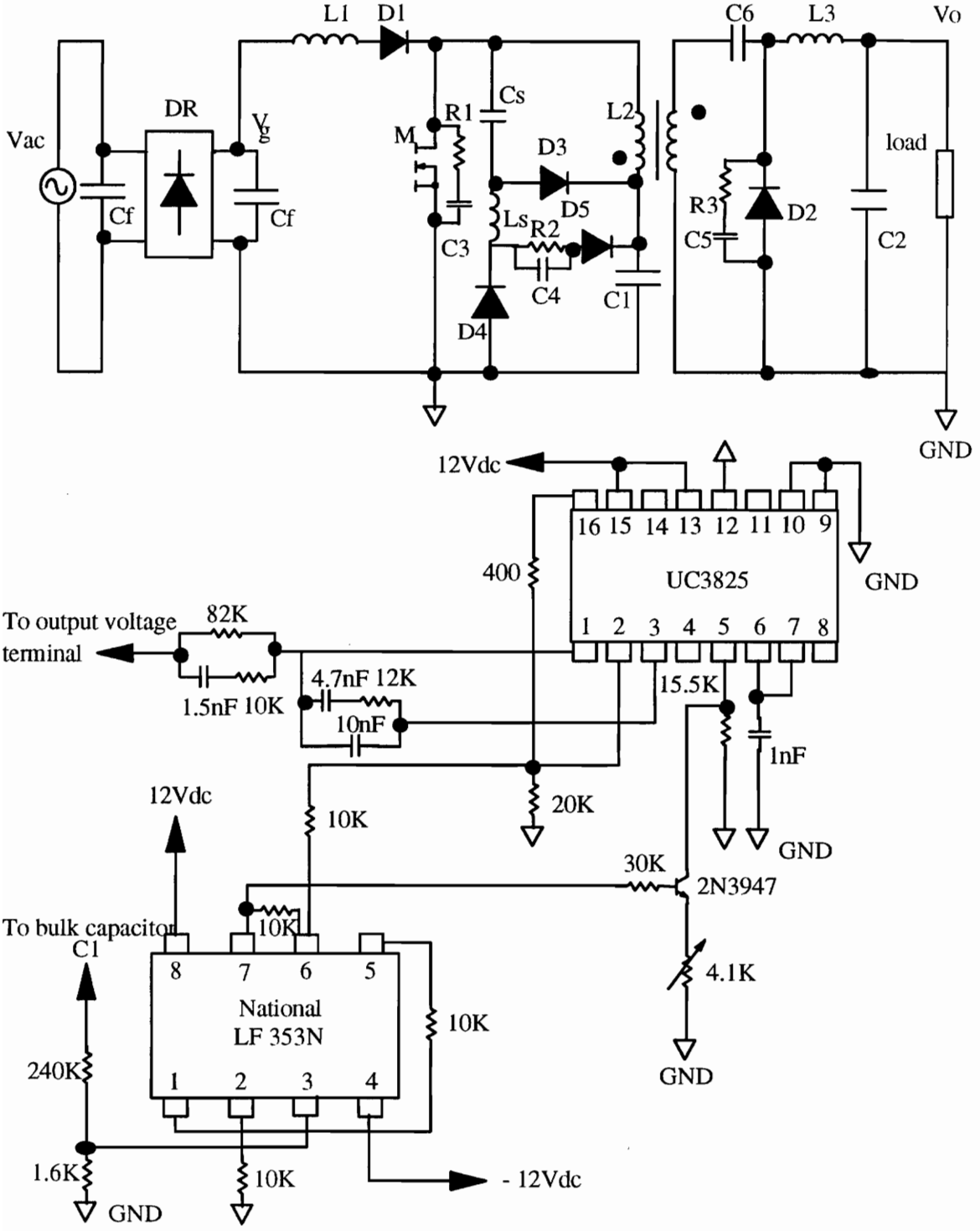
Switching frequency range: 50 to 125K Hz.

Maximum drain to source voltage of the switch: 350 Vdc.

Components:

1. M : IRFP450.
2. L1 : TDK PC40 1407Z, #22 windings, (22 turns), inductance- 190uH.
3. L2 : TDK PC40 1407Z, primary windings- #26, (50 turns), secondary- 3 mil copper foil, 5 turns. Magnetising inductance- 1.35mH.
4. L3 : Micrometals T106-26, 23uH
5. Ls : Magnetic 547L 55353-A2, 25uH.
6. D1 : PH BYT79.
7. D2 : PH BYV143.
8. D3 : PH BYM26C.
9. D4 : PH BYT79.
10. Cs : 400 V, 0.4uF.
11. Cf : 400 V, 0.47uF.
12. C1 : 450V, 330uF.
13. C2 : 50 V, 47uF X 4, electrolytic.
14. C3 : 630 V, 0.5nF.
15: C4 : OSCON 15V, 15uF X 6.
16. R1 : 160 ohm.
17. DR: KBU8J GI9206.
18. UC3825.
19. LF353N.

B.3 BIBRED converter with variable frequency control and LC snubber (universal line)



Specifications:

Input voltage range: 85 to 270 Vac.

Output voltage: 5 Vdc.

Load range: 1.8 to 18 A.

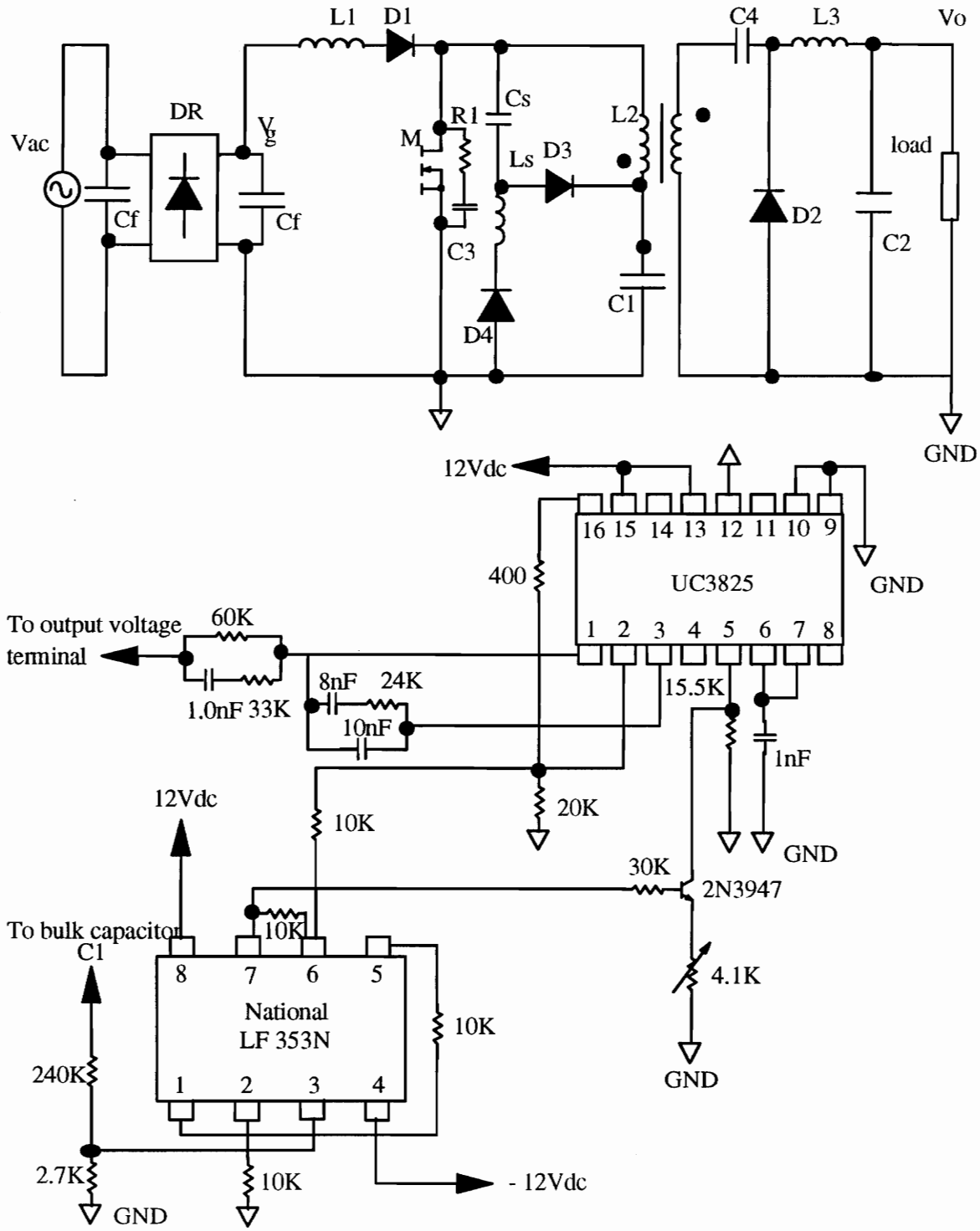
Switching frequency range: 50 to 125K Hz.

Maximum drain to source voltage of the switch: 680 Vdc.

Components:

1. M : IRFPE50.
2. L1 : TDK PC40 1407Z, #22 windings, (22 turns), inductance- 170uH.
3. L2 : TDK PC40 1407Z, primary windings- #26, (50 turns), secondary- 3 mil copper foil, 5 turns. Magnetising inductance- 1.35mH.
4. L3 : Micrometals T106-26, 23uH
5. Ls : Magnetic 547L 55353-A2, 25uH.
6. D1 : PH BYR34.
7. D2 : PH BYV42.
8. D3 : PH BYR34.
9. D4 : PH BYR34.
10. D5 : PH M26C.
11 Cs : 400 V, 0.4uF.
12. Cf : 400 V, 0.47uF.
13. C1 : 450V, 100uF X 2 in series.
14. C2 : 50 V, 47uF X 4, electrolytic.
15. C3 : 630 V, 0.5nF.
16. C4 : 0.1uF.
17. C5 : 1nF.
18: C6 : OSCON 15V, 15uF X 6.
17. R1 : 170 ohm.
19. R2 : 10K ohm.
20. R3 : 100 ohm.
21. DR: KBU8J GI9206.
22. UC3825.
23. LF353N.

B.4 BIBRED converter with variable frequency control, LC snubber and swinging choke.



Specifications:

Input voltage range: 85 to 135 Vac.

Output voltage: 5 Vdc.

Load range: 1.8 to 10 A.

Switching frequency range: 50 to 75K Hz.

Maximum drain to source voltage of the switch: 300 Vdc.

Components:

1. M : IRFP450.
2. L1 : TDK PC40 1407Z, #22 windings, (22 turns), two third of center-leg and outer legs stepped gap- 0.2cm.
3. L2 : TDK PC40 1407Z, primary windings- #26, (50 turns), secondary- 3 mil copper foil, 5 turns. Magnetising inductance- 1.35mH.
4. L3 : Micrometals T106-26, 23uH
5. Ls : Magnetic 547L 55353-A2, 25uH.
6. D1 : PH BYT79.
7. D2 : PH BYV143.
8. D3 : PH BYM26C.
9. D4 : PH BYT79.
10. Cs : 400 V, 0.4uF.
11. Cf : 400 V, 0.47uF.
12. C1 : 450V, 330uF.
13. C2 : 50 V, 47uF X 4, electrolytic.
14. C3 : 630 V, 0.5nF.
15 C4 : OSCON 15V, 15uF X 6.
16. R1 : 160 ohm.
17. DR: KBU8J GI9206.
18. UC3825.
19. LF353N.

VITA

Dan Man Cheung Tsang was born in Hong Kong on August 30, 1964. He came to study in the United States in 1984 in pursuit of the Bachelor degree of science in electrical engineering. He graduated from Oklahoma State University, Stillwater, Oklahoma with honor in December 1987. He is a member of the honor societies of Phi Kappa Phi and Tau Beta Pi since August 1986.

After graduation, he went to Taipei, Taiwan in February 1988 to attend a Christian missionary training for two years. Upon completion of the training in December 1989, he married Ms. Yeu Chuen Sarah Yang. After being an assistant evangelist for four months, he went to Hong Kong in April 1990 to set up a Christian bookstore and published christian newspaper. He decided to further his education after the book store was operating stably. He came back to United States in August 1991 to enroll in the graduate program in Virginia Tech to work towards his Masters degree of Science in Electrical Engineering. He joined the Virginia Power Electronics Center (VPEC) in January 1991 as a graduate assistant with Dr. Fred C. Lee as his principal advisor. He is under the Delta Fellowship since then. His first project was 'Improvement of standby-mode efficiency of lap-top computer dc-dc converters'. The second project is the 'Feasibility study of a single stage power factor correction converter'.

Upon graduation in August 1993, he will join a power supplies company in Gaithersburg, Maryland.

Dan Tsang