Silicon-Based PALNA Transmit/Receive Circuits for Integrated Millimeter Wave Phased Arrays

Iskren Abdomerovic

Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Sanjay Raman, Chair
Allen B. MacKenzie
Charles T. Clancy
Yang Yi
Alireza Haghighat

November 15, 2019
Arlington, Virginia

Keywords: millimeter-wave frequencies, phased arrays, transmit/receive circuits, PALNA, LNAPA, bidirectional T/R circuits, switchless T/R circuits, power amplifier, low noise amplifier, noise figure, power added efficiency, output power

Copyright 2019

Silicon-Based PALNA Transmit/Receive Circuits for Integrated Millimeter Wave Phased Arrays

Iskren Abdomerovic

ABSTRACT

Phased array element RF front ends typically use single pole double throw (SPDT) switches or circulators with high isolation to prevent leakage of transmit energy into the receiver circuits. However, as phased-array designs scale to the millimeter-wave range, with high degrees of integration, the physical size and performance degradations associated with switches and circulators can present challenges in meeting system performance and size/weight/power (SWAP) requirements. This work demonstrates a loss-aware methodology for analysis and design of *switchless* transmit/receive (T/R) circuits. The methodology provides design insights and a practical, generally applicable approach for solving the multi-variable optimization problem of switchless power amplifier/low-noise amplifier (PALNA) matching networks, which present optimal matching impedances to both the power amplifier (PA) and the low noise amplifier (LNA) while maximizing power transfer efficiency and minimizing dissipative losses in each (transmit or receive) mode of operation.

Three PALNA example designs at W-band are presented in this dissertation, each following a distinct design methodology. The first example design in 32SOI CMOS leverages PA and LNA circuits that already include 50 Ω matching networks at both input and output. The second example design in 8XP SiGe develops the PA and LNA circuits and integrates the PA output and LNA input matching networks into the PALNA matching network that connects the PA and the LNA. The third design in 32SOI CMOS leverages the loss-aware PALNA design methodology to develop a PALNA that achieves simulated maximum power added efficiency of 18 % in transmit and noise figure of 7.5 dB in receive at 94 GHz, which is beyond the published state-of-art for T/R circuits. In addition, for

comparison purposes, this dissertation also presents an efficient, switch-based T/R circuit design in 32SOI CMOS technology, which achieves a simulated maximum power added efficiency of 15 % in transmit and noise figure of 6.5 dB in receive at 94 GHz, which is also beyond the published state-of-art for T/R circuits.

Silicon-Based PALNA Transmit/Receive Circuits for Integrated Millimeter Wave Phased Arrays

Iskren Abdomerovic

GENERAL AUDIENCE ABSTRACT

In military and commercial applications, phased arrays are devices primarily used to achieve focusing and steering of transmitted or received electromagnetic energy. Phased arrays consist of many elements, each with an ability to both transmit and receive radio frequency (RF) signals. Each element incorporates a power amplifier (PA) for transmit and a low noise amplifier (LNA) for receive, which are typically connected using a single pole double throw (SPDT) switch or a circulator with high isolation to prevent leakage of transmit energy into the receiver circuits. However, as phased arrays exploit the latest technological advances in circuit integration and their frequencies of operation increase, physical size and performance degradations associated with switches and circulators can present challenges in meeting system performance and size/weight/power (SWAP) requirements. This dissertation provides a loss-aware methodology for analysis and design of switchless transmit/receive (T/R) circuits where the switches and circulators are replaced by carefully designed power amplifier/low-noise amplifier (PALNA) impedance matching networks. In the switchless T/R circuits, the design goals of maximum power efficiency and minimum noise in transmit and receive, respectively, are achieved through impedance matching that is optimal and low-loss in both modes of operation simultaneously.

Three distinct PALNA example designs at W-band are presented in this dissertation, each following a distinct design methodology. With each new design, lessons learned are leveraged and design methodologies are enhanced. The first example design leverages already available PA and LNA circuits and connects them using 50 Ω transmission lines whose lengths are designed to guarantee optimum impedance match in receive and

transmit mode of operation. The second example design develops new PA and LNA circuits and connects them using 50 Ω transmission lines whose lengths are designed to simultaneously achieve optimum impedance matching for maximum power efficiency in transmit mode of operation and lowest noise in receive mode of operation. The third design leverages a loss-aware PALNA design methodology, a multi-variable optimization procedure, to develop a PALNA that achieves simulated maximum power added efficiency of 18 % in transmit and noise figure of 7.5 dB in receive at 94 GHz, which is beyond the published state-of-art for T/R circuits. In addition, for comparison purposes with the third PALNA design, this dissertation also presents an efficient, switch-based T/R circuit design, which achieves a simulated maximum power added efficiency of 15 % in transmit and noise figure of 6.5 dB in receive at 94 GHz, which is also beyond the published state-of-art for T/R circuits.

To

My family

Acknowledgments

I would like to express my sincere appreciation and gratitude to my advisor, Dr. Sanjay Raman. Thank you very much for giving me the opportunity to earn my Ph.D. and thank you for all your help, advice, and guidance during my Ph.D. studies.

I would like to thank my advisory committee members for their help and support, and my VT colleagues Sadia (Lisa) Afroz, Christopher Maxey, Hyunchul Kim, Yahya Mortazavi, Dongseok Shin, and Shinwoong Park for their help, collaboration, and support.

I am thankful to Mr. Bruce Wallace of the Defense Advanced Research Projects Agency (DARPA) Strategic Technology Office (STO) for his sponsorship under the Multifunction RF program and Dr. Mustafa Sayginer of the University of California at San Diego for his help, collaboration, and support.

I would like to thank Booz Allen Hamilton for their tuition assistance sponsorship and particularly, I am indebted to Mr. Saverio Fazzari for his guidance, support, and help throughout my studies.

I am thankful to Dr. Alfred Hung, Mr. Edward Viveiros, and Mr. Khamsouk Kingkeo of the Army Research Laboratory (ARL) for their support with the measurement and analysis of the fabricated chips and I am thankful to Mr. Daniel Marrujo of Defense

MicroElectronics Activity (DMEA) for enabling the fabrication of the switch-based T/R circuit.

Finally, I am thankful to my family. Thank you for your constant and continuing support, inspiration, and encouragement.

Table of Contents

List of Figures

List of Tables

List of Abbreviations and Nomenclature

Symbol	Definition
ARL	Army Research Laboratory
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DARPA	Defense Advanced Research Projects Agency
DMEA	Defense MicroElectronics Activity
DoD	Department of Defense
EM	Electromagnetic
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GSG	Ground-Signal-Ground
IC	Integrated Circuit
InP	Indium Phosphide
LNA	Low Noise Amplifier
LNAPA	Low-Noise Amplifier/Power Amplifier
mm-Wave	Millimeter Wave
MFRF	Multifunction Radio Frequency
MIM	Metal-Insulator-Metal
MN	Matching Network
MOM	Metal-Oxide-Metal
NF	Noise Figure
PA	Power Amplifier
PAE	Power Added Efficiency
PALNA	Power Amplifier/Low-Noise Amplifier
P_{out}	Output Power
PNA	Performance Network Analyzer
RF	Radio Frequency

RX	Receive
SiGe	Silicon Germanium
SOA	State-of-Art
SOI	Silicon on Insulator
SPDT	Single Pole Double Throw
SWAP	Size, Weight, and Power
TL	Transmission Line
T/R	Transmit/Receive
TX	Transmit
W-band	Millimeter Wave Band Covering from 75 GHz to 110 GHz

Chapter One: **Introduction**

1.1 Motivation and State-of-the-art

Traditional phased array element RF front ends, in which a single antenna is shared between the transmit and the receive signal chains, use transmit/receive (T/R) switches or circulators to provide the required isolation (see Fig. 1.1(a) – 1.1(b)). However, with recent interest in integrated phased array circuits up to millimeter wave frequencies, it has been recognized that on-chip integrated T/R switches take up a substantial amount of overall die area [1]. Similarly, ferrite circulators are not readily integrated and, while passive on-chip circulators have been demonstrated, they have yet to be scaled up to 94 GHz with acceptable loss performance [2]. Therefore, there has been increasing interest in T/R circuit architectures that eliminate, or make innovative use of, T/R switches [3]-[15].

A circuit architecture that has received considerable attention in literature is based on the bidirectional power amplifier/low-noise amplifier (PALNA) concept (see Fig. 1.1(c)). By moving the T/R switch to the transceiver side of the amplifiers, a bidirectional PALNA reduces the impact of switch losses on the overall performance of the T/R circuit. The first known millimeter wave bidirectional PALNA amplifier was reported in [3] and [4]. The amplifier leverages an inherent symmetry of the common gate amplifier topology and the

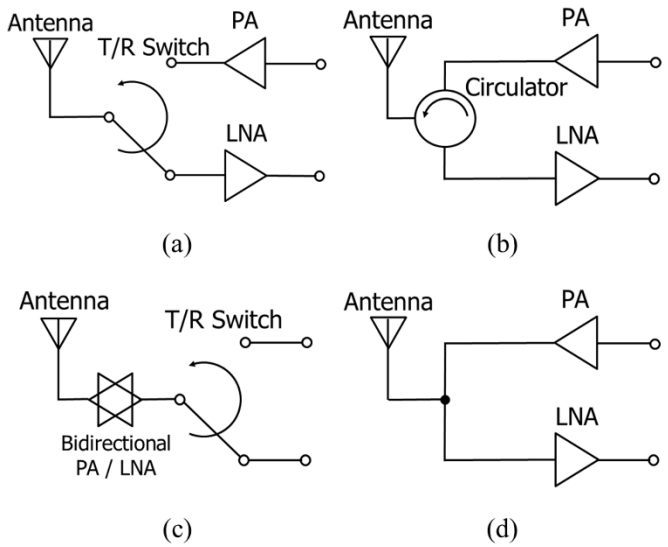


Fig. 1.1. T/R circuit architectures: (a) traditional, switch-based; (b) traditional, circulator based; (c) bidirectional PALNA; (d) switchless PALNA.

same devices are used for both the LNA and the PA function, which can be limiting since the transistor size cannot be separately optimized for each function. To allow transistor sizing flexibility, a common-source T/R circuit topology was introduced in [5] and [6], although details on the design of the matching networks that connect the LNA and the PA circuits were not presented. Circuits reported in [3]-[6] were fabricated in GaAs, and more recently an InP implementation was shown in [7]. However, recent interest in the use of silicon for millimeter wave phased array T/R circuits has resulted in silicon implementations of the bidirectional PALNA T/R circuits [8]-[13].

In [8] and [9], a two-port PALNA circuit was reported based on a time-duplexing approach where the PA and the LNA branches are each interchangeably turned on and off by bias switching. The input impedance of the “off” branch is designed to be as high as possible, to minimize the loading of the "on" branch, however detailed analysis of the PALNA matching network losses in both the transmit and the receive mode of operation was not presented. In [10], a load-pull analysis of the PA is used for a PALNA matching network design which maximizes P_{out} in transmit, however in receive, the “off” state PA branch isolation was maximized without detailed analysis of the resulting loss and its impact on the NF. In [11], a PALNA matching network design provides optimum impedance

matching for both the LNA NF and PA P_{out}, however the PALNA is based on PA and LNA that are matched to 50 Ω and the loss contribution of the 50 Ω matching networks to overall PALNA loss was not analyzed. In [12] and [13], optimum impedance matching network designs are pursued for both the LNA and the PA, however detailed analysis of matching network losses and design tradeoffs in transmit and receive was not presented.

In [14] and [15], T/R circuit architectures similar to the switchless PALNA (see Fig. 1.1(d)) are presented. In [14], the matching network that connects the PA and the LNA at the antenna is designed so that the PA branch in the "off" state looks like an open circuit and the matching network is optimized to favor the NF performance of the LNA. In [15], a transformer-based isolation network design approach is explored. However, detailed analysis of the PALNA matching network losses in transmit and receive was not presented in [14] and [15].

This dissertation primarily focuses on the switchless PALNA T/R circuit architecture shown in Fig. 1.1(d). A methodology for loss-aware PALNA matching network design is presented, which provides the optimally matched impedances to both the LNA and the PA. The "off" branch (i.e., the branch with bias turned off) is treated as an impedance matching stub for the branch that is "on" and the matching network losses are carefully managed in both modes of operation. The LNA input matching network and the PA output matching network are integrated into the PALNA and the best achievable performance is explored as compared to a switch-based T/R circuit with the 50 Ω match.

1.2 Why mm-Waves?

Due to desirable physical properties at mm-wave frequencies, there has been an increased amount of interest in applications involving mm-Waves. Table 1.1 summarizes some known current and emerging mm-Wave applications and the applicable standards. In particular, for communications applications, higher channel capacities are obtainable at mm-Wave frequencies than at lower frequencies, potentially enabling high data rate

Table 1.1.
Current and Emerging mm-Wave Applications.

IEEE Frequency Bands [GHz]	Frequency [GHz]	Applications	Applicable Standards
Ka (27-40)	28, 38	Mobile communications for 5G Cellular networks	ITU's IMT-2020
	27.5-30	SATCOM uplinks (e.g., Inmarsat Global Xpress: 27.5-30) and downlinks (e.g., Iridium: 29.1-29.3)	MIL-STD-188-164, ITU-R S.524-9, FCC 25.138, ETSI EN 303 978
	24.25-30	L-3 ProVision imaging scanners at airports	IEEE C95.1
	35	Munitions and missiles seekers and sensors	Unknown
V (40-75)	43.5-45.5	U.S. AEHF military SATCOM system uplinks*	MIL-STD-3015
	57-66	"Last inch", short range wireless communications	IEEE 802.11ad, IEEE 802.11aj, IEEE 802.15c
	71-75	"Last mile", point-to-point backhaul wireless communications	ETSI TS 102 524
W (75-110)	75-76, 81-86, 92-95	"Last mile", point-to-point backhaul wireless communications	ETSI TS 102 524
	76-77	Autonomous cruise control (ACC) "long range" automotive radar	ETSI EN 301 091 parts 1 & 2
	77-81	Short range "stop & go" automotive radar	ETSI TR 102 263
	94	Missile seekers, collision avoidance radars	Unknown
	85-110	Imaging for medicine, biology, and security	IEEE C95.1
G (110-300)	110-120	Imaging for medicine, biology, and security	IEEE C95.1
	220-240	Long range wireless communications, atmospheric research radar	None yet available
	120, 183, 325	Short range wireless communications (emerging)	None yet available

* U.S. AEHF system downlink frequencies are located at 20.2 GHz – 21.2 GHz (IEEE K band).

communications. For radar applications, the increased bandwidth at mm-wave frequencies translates into improved range resolution. For imaging applications, mm-waves can supplement visible and infrared (IR) systems by providing penetration and visibility under optically opaque conditions such as smoke, fog, clouds, dust and sandstorms. More generally, for a fixed aperture size, antenna directivity at mm-Wave frequencies is higher than at lower frequencies because the antenna is large compared to the wavelength. This higher directivity helps compensate for higher mm-wave absorption in the air and for reduced output power levels available from solid state devices. For communication systems in particular, increased directivity translates into narrower beam patterns, which potentially provides an increased level of security and allows for increased frequency reuse through spatial diversity. Further discussion of benefits of mm-waves, and in particular as may be applicable to phased arrays, is given in [16].

1.3 Phased Array Architectures

1.3.1 Functional View

Beamforming in active phased arrays has traditionally been implemented in the RF/analog domain, by carefully controlling the delay/phase of the RF signal through each antenna element using RF phase shifters. In order to minimize MMIC area needed, one phase shifter is typically used per antenna element (T/R module) in a “common leg” approach, where the phase shifter path is switched between PA input and LNA output, as needed, to support beamforming in transmit or receive mode of array operation. This RF beamforming approach has been the standard in military applications of phased arrays for decades and has more recently become a de-facto standard in emerging commercial applications as well.

Enabled by advances in integrated circuit technologies, the phased array functional architectures have been evolving toward the element-level digital phased array architecture shown in Fig. 1.2 [17]. The element-level digital phased arrays seek to achieve the ultimate in application flexibility by leveraging digitization and control of both the transmitted and received waveforms at each antenna element and using digital processing for application-specific optimization and reconfigurability [18]. However, as we can see from Fig. 1.2, their overall performance still depends on PAE and NF performance of the individual, RF front-end, T/R circuits. In fact, this is even more true for digitally beamformed arrays than for the more traditional phased array architectures because of the additional power consumption required for digitization and data processing [19]. Therefore, there is a need and a motivation for studying high performance T/R circuits.

As summarized above and shown in Fig. 1.2, T/R circuits have more traditionally consisted of three basic components: 1. PA, 2. LNA, and 3. SPDT T/R switch or a circulator. However, this dissertation will focus on a novel switchless PALNA T/R circuit architecture shown in Fig. 1.1(d).

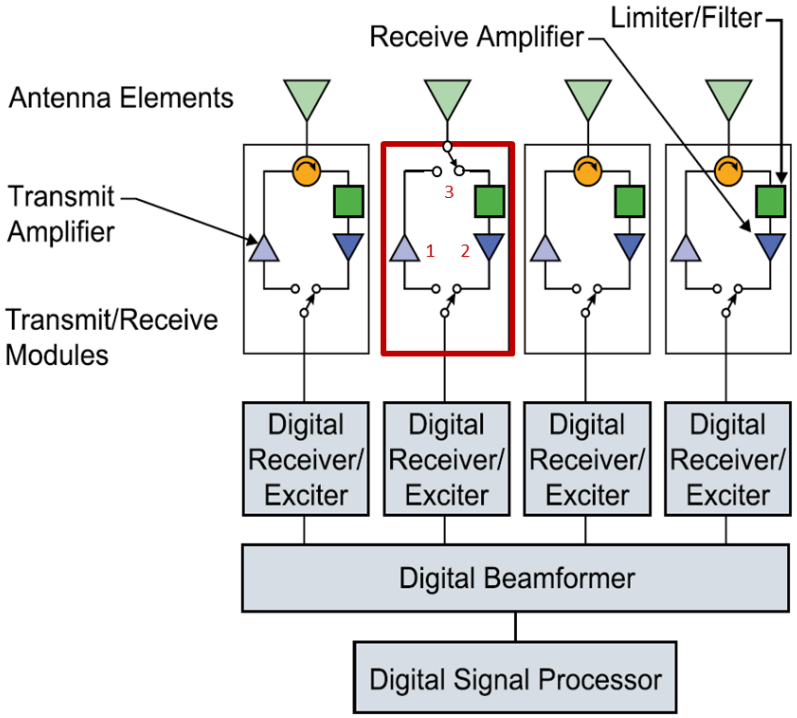


Fig. 1.2. Element-level digital phased array architecture [17].

1.3.2 Wafer Scale Arrays and Silicon Implementations

The work presented in this dissertation is motivated by the ongoing evolution of phased array technologies. The scale of integration in silicon has recently enabled highly integrated mm-wave wafer-scale phased arrays in which high directivity (i.e., array gain) is achievable using a large number of antenna elements [20]. Therefore, mm-wave wafer scale phased arrays are of interest for commercial and DoD applications.

Fig. 1.3 shows the concept of the wafer-scale phased array where the EM-coupled antenna layer is directly attached to the silicon wafer that contains the phased array electronics [20]. Fig. 1.4 shows the photograph of a recently reported 256-element SiGe phased array fabricated on a 200-mm wafer using the wafer-scale integration approach [20].

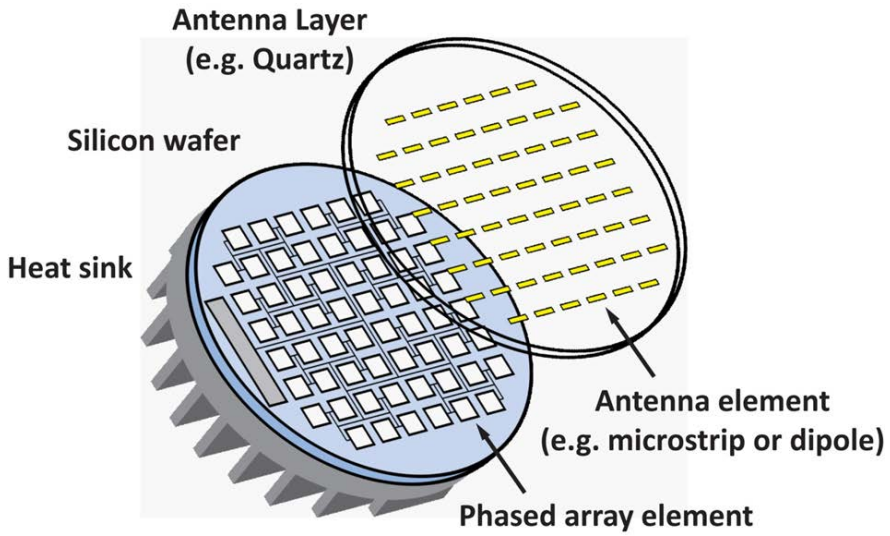
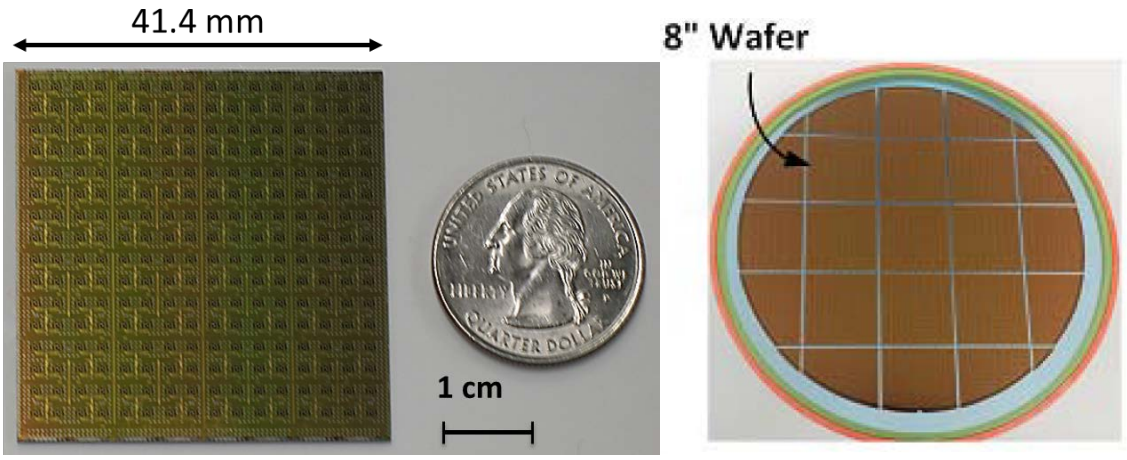


Fig. 1.3. Highly integrated wafer-scale phased array concept [20].



(a) (b)

Fig. 1.4. (a) Photograph of a 256-element SiGe phased array fabricated on a 200-mm wafer using the wafer-scale integration approach. (b) Photograph of the 200-mm (8") wafer containing multiple phased array electronics chips [20].

As discussed in [20], the wafer-scale integration approach is appealing because it eliminates 3–4 dB of transition loss between the silicon chip RF port and the antenna port at mm-wave frequencies (6–8 dB system loss for a communication or radar application). This loss is typically present in the traditional design approach where which the electronics are coupled to the antennas via conductive, transmission line based, complex distribution networks. An additional benefit of this approach is cost, because both the RF distribution

networks and the baseband-to-RF electronics can be integrated on-chip, which can be placed on a low-cost board handling only IF-frequency signals, thus eliminating exotic, costly external RF PCBs that would otherwise be required.

However, the wafer-scale approach requires large silicon chips and makes a relatively inefficient use of the overall silicon wafer area, particularly at lower frequencies where antenna element sizes are larger, which are two potential disadvantages. However, the elimination of 3-4 dB of distribution loss allows for a lower number of antenna elements (0.5-0.4x less elements) to generate the same effective isotropic radiated power (EIRP) as the traditional design, thus resulting in a smaller overall wafer-scale phased array.

Therefore, the wafer-scale approach is attractive. However, for a large number of elements, poor T/R circuit performance translates into poor system/platform performance (e.g., T/R PAE = 0.02 % - 4 %), and that is both a concern and a great opportunity for mm-Wave silicon phased array circuit designers. This dissertation will explore ways in which the phased array PAE can be increased by improving the efficiency of the PA/LNA interface.

1.4 Millimeter Wave T/R Circuit Concepts

1.4.1 T/R Circuit Performance Metrics

The work presented in this dissertation was funded under the Defense Advanced Research Project Agency (DARPA) Multifunction RF (MFRF) program. Under an MFRF seedling effort, the Virginia Tech team explored 94 GHz T/R circuits in advanced silicon technology nodes, targeting NF < 10 dB, PA P_{out} of 3-5 dBm, and PA PAE > 20 %. This performance is summarized in Table 1.2 and compared with technology state-of-the-art at the time. Therefore, work presented in this dissertation was planned and executed with the intention of meeting or exceeding those performance goals. As is usually the case in phased arrays, the element pitch of interest was $\lambda/2$, which drove the need for very compact T/R circuit design. On the other hand, since application platform prime DC power can be limited, the

Table 1.2.
Virginia Tech MFRF Metrics Summary and Comparison with Prior Art.

Metrics	State-of-the-art	Goal Performance
Frequency of Operation [GHz]	94	94
LNA Noise Figure [dB]	11	< 10
PA Output Power [dBm]	-5	3 - 5
PA PAE [%]	3	> 20

power added efficiency of the PALNA circuit in the transmit mode of operation was considered the most important performance metric. In addition to the above-mentioned metrics, PALNA power gain in the transmit mode and the PALNA small signal gain in the receive mode were considered.

1.4.2 PALNA Problem Description

Fig. 1.5 shows the schematics of the proposed PALNA circuit in the transmit and receive mode, respectively. The switchless PALNA design problem considered in this chapter involves simultaneous transmit/receive co-design of passive PA and LNA matching networks such that the 50 Ω antenna impedance becomes transformed into optimal $Z_S=Z_{opt\_LNA}$ and $Z_L=Z_{opt\_PA}$ impedances at the LNA input and PA output, respectively. It is assumed that the LNA and PA will never be on or off at the same time. Rather, in receive

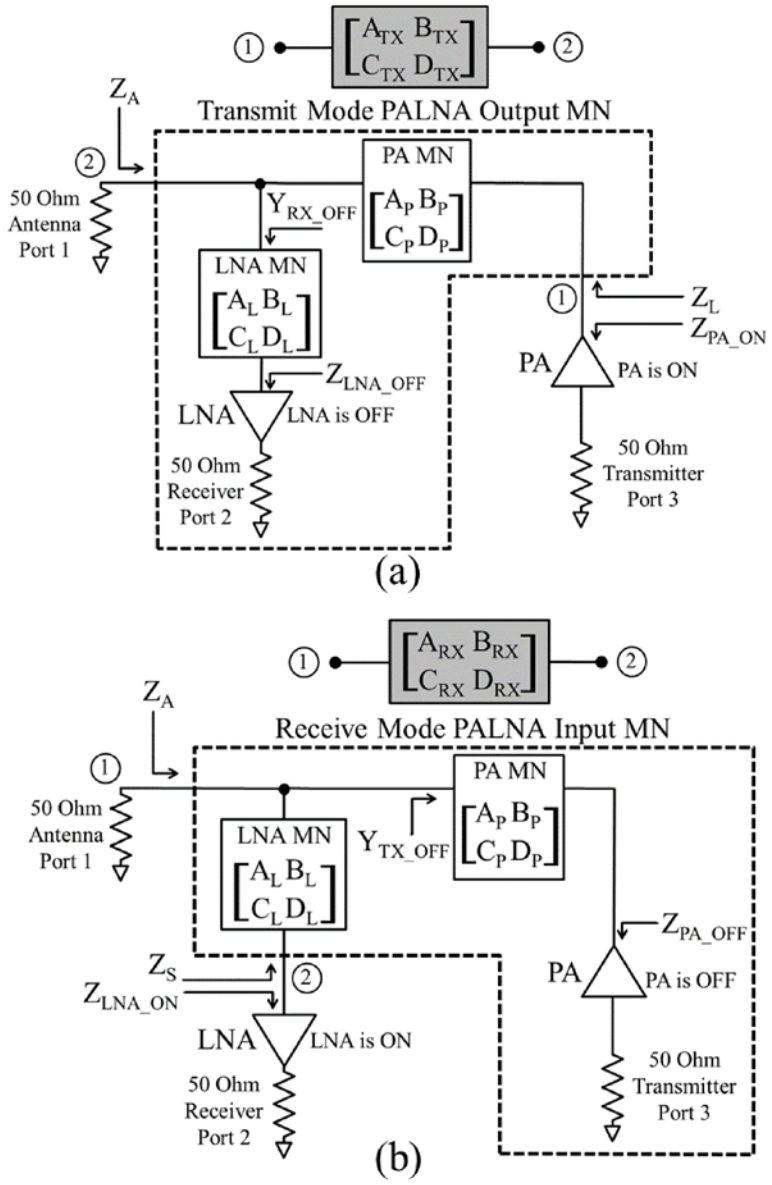


Fig. 1.5. PALNA circuit schematic: (a) the transmit mode; (b) the receive mode.

mode of operation, the LNA is on while the PA is off; and, in transmit mode of operation, the PA is on while the LNA is off. The PA and the LNA matching networks considered in this chapter include transmission lines and lumped element LC networks of various orders.

In addition to achieving the optimal impedances at the PA and the LNA, good PALNA performance requires that both the transmit and receive PALNA matching networks, as shown in Fig. 1.5, have minimal transducer loss. Any loss in the PALNA matching

networks directly translates into performance (e.g., PAE, NF, gain) degradations in transmit and receive modes, respectively. Therefore, a parallel task of the simultaneous co-design procedure is to realistically evaluate and manage the implementation losses associated with the candidate matching networks, using EM simulated components. Those networks that introduce minimal losses in both the receive and the transmit mode of operation should be selected as the final solution. In addition, other practical considerations must be taken into account, such as matching network physical size and implementation feasibility, which are discussed below.

1.5 Dissertation Objectives and Organization

The focus of this dissertation work is to explore switchless PALNA circuit architectures and design approaches to improve the PAE and NF of mm-wave phased array T/R circuits and compare to what is possible with traditional T/R circuit architectures. This is accomplished by developing and presenting a loss-aware PALNA circuit design methodology described above. By designing a switch-based T/R circuit and a switchless PALNA circuit, using the same basic PA and LNA cells, it is shown that the properly designed switchless PALNA circuit is superior in performance in comparison with a traditional switch-based T/R circuit.

This dissertation is organized into seven chapters. Chapter 2 presents a state-of-the-art 94 GHz switch-based T/R circuit design, which is used for performance comparison purposes with a final PALNA circuit. Chapter 3 presents an initial 94 GHz switchless PALNA design leveraging existing 50 Ω PA and LNA cells. The focus in chapter 3 is to optimize the PALNA matching network only to achieve optimum small-signal performance in both modes of PALNA operation. Chapter 4 presents an evolved 94 GHz switchless PALNA design with simultaneous optimum impedance matching for maximum PAE and minimum NF. The focus of chapter 4 is on exploring an iterative optimization approach, using both small-signal and large-signal Cadence simulations, to achieve optimum performance as defined by the PALNA circuit metrics above. Chapter 5 presents a final 94 GHz switchless

PALNA design with simultaneous optimum impedance matching and minimum transducer loss in both modes of operation. A loss-aware, iterative PALNA design methodology is developed in chapter 5 and the PAE and NF performance metrics are pursued directly. LNA and PA core circuit designs are presented, which are suitable for execution of the iterative PALNA design procedure. The switchless PALNA matching network design and implementation in 32-nm silicon-on-insulator CMOS (32SOI) technology is described. The iterative optimization procedure discussed integrates the LNA and the PA circuits designs mentioned above and ensures that the PALNA matching networks simultaneously provide an optimum input impedance match for the LNA and an optimum output impedance for the PA with minimal losses. Chapter 5 presents the 32SOI PALNA circuit simulation results, including discussion of the PALNA circuit losses and comparison with a switch-based T/R circuit design presented in Chapter 2. Chapter 6 considers bandwidth performance of PALNA matching networks and presents an updated loss-aware, iterative PALNA design methodology, which includes bandwidth as one of the PALNA design criteria. The updated methodology was applied to investigate the performance of six PALNA topologies and simulations are presented demonstrating a bandwidth-extended PALNA design. Chapter 7 presents the conclusions, a list of contributions that resulted from this dissertation, a description of recommendations for future research, and a list of published papers.

Chapter Two: **A 94 GHz Switch-based T/R Circuit**

2.1 Introduction

The performance of highly integrated mm-Wave multifunction phased arrays is highly dependent on power added efficiency (PAE) and noise figure (NF) performance of the constituent T/R circuits. Since complex, multi-function mm-wave phased arrays may incorporate tens of thousands of T/R circuits, power generation and thermal management on platforms of interest are significant system design issues, and the PAE becomes perhaps the most important Tx performance metric. Advanced understanding of technical issues that affect the performance of mm-Wave power amplifiers (PAs) and low noise amplifiers (LNAs) designed in deeply scaled silicon-based technologies provides an opportunity to demonstrate high-performance, integrated T/R circuits at 94 GHz [21], [22].

This chapter presents a switch-based T/R circuit design in Global Foundries 32SOI technology. Since the focus of this dissertation is on PALNA circuit design, the relevant details of the 32SOI process are discussed in sections 3.1 and 5.1 below and are not repeated here. The proposed circuit consists of three major components: the PA, the LNA,

and the single pole double throw (SPDT) T/R switch. The SPDT switch connects the antenna port to the PA output and LNA input in transmit and receive, respectively.

2.2 PA Design

The main design goal for the PA was to maximize the PAE. For maximum PAE, switched-mode PA architectures leveraging multiple stacked SOI devices have demonstrated excellent results, albeit at frequencies below W-band [21].

A Class-E-like PA circuit with two stacked devices is used in the transmit path of the proposed T/R circuit. Fig. 2.1 shows the schematic of the PA. To maximize device f_{max} and the PAE performance at 94 GHz, 24 μm nFET transistors with 1 μm fingers are used.

Cadence Spectre simulations are used to generate constant PAE load pull contours and determine the optimum PA load impedance required for maximum PAE at 94 GHz. Then, the PA output matching network is designed. The PA input matching network is also optimized until the value of the highest PAE contour is maximum. The capacitors are implemented as custom-made, metal-oxide-metal (MOM) structures in 32SOI metallization stackup. Transmission lines and the inductors are implemented as microstrips in LB metal with ground on layer E1. Transistor terminals are connected to the rest of the circuit using terminal embedding networks modeled using the Sonnet electromagnetic (EM) software as shown in Fig. 2.2.

Fig. 2.3 shows a more detailed circuit schematic of the 94 GHz Class-E-like PA design in 32SOI CMOS. It is a PA modeled after switching mode, Class-E PA, which is known to be a desirable PA topology from the PAE perspective. However due to the difficulty of obtaining an ideal square-wave drive and the limited amount of harmonic shaping of voltages and currents that is feasible at 94 GHz, this circuit is referred to as "switch-like" or "Class-E-like", rather than a "Class-E" circuit.

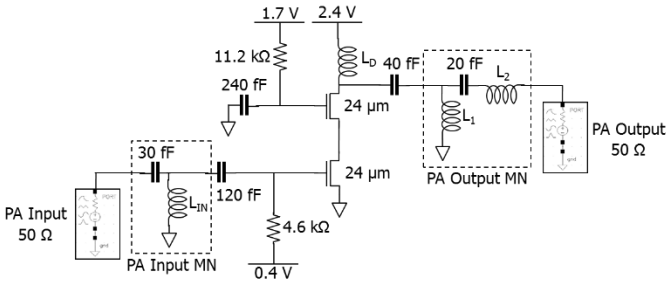


Fig. 2.1. Circuit schematic of the PA.

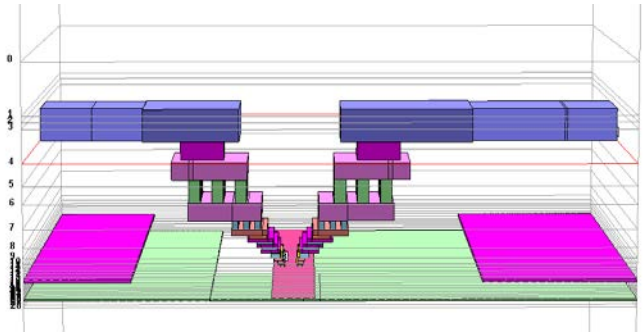


Fig. 2.2. Transistor terminal embedding network EM model constructed in Sonnet. Left stackup and right stackup model transistor drain and source connections, respectively, to the top metallization layer LB.

The main idea in this circuit is that stacking nFET transistors in series allows operation of the stack at twice the supply voltage that is suitable for the operation of a single transistor. Therefore, transistor stacking allows us to potentially overcome the breakdown voltage limitation of the 32SOI process technology for mm-Wave PAs. In terms of the maximum voltage swing at the top node of the stack, the voltage equals up to 4.8 V (2 transistors x 2.4 V, given that 2 pn junctions are present in one nFET transistor).

For maximum PAE and good P_{out} and power gain at 94 GHz, nFET transistors with 1 µm fingers and a total width of 24 µm were selected through experimental simulation. The voltage swing at the intermediate node controls the turn-on and turn-off of the top transistor. The top transistor gate is connected to ground via the large, 240 fF bypass capacitor, to prevent the gate from experiencing voltage swing, per published design methodology for a two-stack circuit [21]. The top transistor drain is loaded with an output network that is designed based on Class-E principles. The output network consists of the

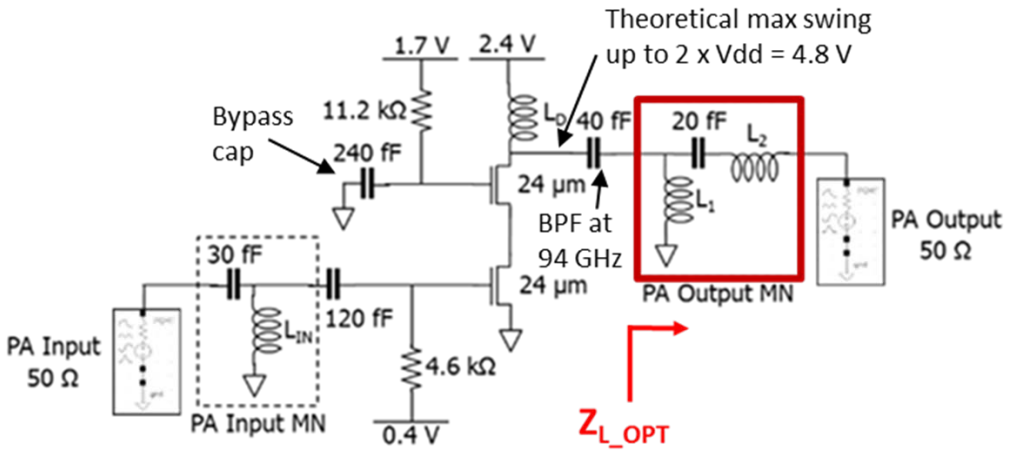


Fig. 2.3. A detailed circuit schematic of the 94 GHz Class-E-like PA design in 32SOI CMOS.

40 fF capacitor structure, which includes embedding networks at both ends. The structure performs a resonant band-pass function at 94 GHz, consequently allowing the transistor drain to sustain Class-E-like waveforms, which were verified in simulation.

As shown in Fig. 2.4, load pull contours were generated to aid in determination of the optimum PA load impedance for maximum PAE. With some subsequent experimentation, using large signal simulations in Cadence, it was determined that the optimum load impedance is 90 Ω. The PA output matching network is then designed to transform the 50 Ω impedance of the antenna into 90 Ω seen by the PA, as needed for maximum PAE of the PA.

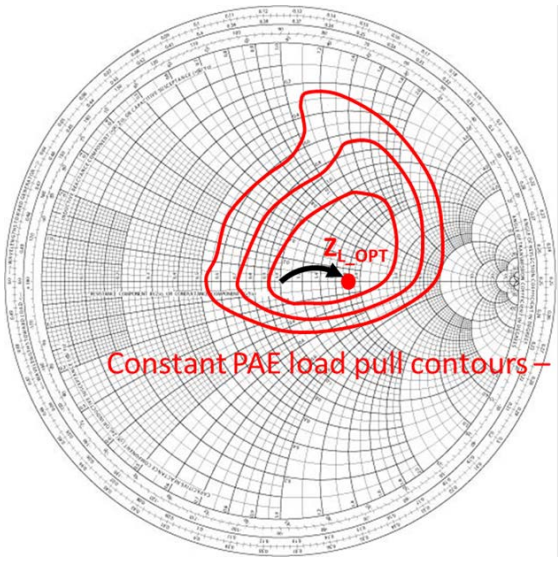


Fig. 2.4. PA load impedance matching is done using the PA load pull contours. The optimum load impedance, Z_{L_OPT} = 90 Ω, was determined through simulation experimentation.

2.3 LNA Design

For the integrated LNA design, optimum transistor size and biasing choices can enable a simultaneous noise and impedance input match [22]. In this dissertation, a single-ended, single-stage cascode circuit with current mirror biasing is used. Since transistor biasing current density required for minimum NF or maximum gain is independent of CMOS technology, an initial current density of 0.1 mA/μm was chosen for biasing of the 32SOI nFETs in the LNA circuit [22]. Then, the current density was gradually increased and the LNA NF and gain were simulated with each increase. Finally, it was determined by simulation experiments that the main LNA transistors should be biased at an optimum current density of 0.3 mA/μm for best simultaneous NF and small-signal gain performance. Fig. 2.5 shows the schematic of the LNA. For maximum LNA gain and minimum NF, with minimal output matching network complexity and thus minimal loss, transistors with 1 μm fingers and a total width of 12 μm were found, by experimental simulation, to be the most favorable. The biasing circuit uses a 1.2 μm transistor, to minimize the circuit's power overhead. The capacitors are implemented as MOM structures. The transmission lines and the inductors are implemented as LB metal microstrips with ground on layer E1. Again,

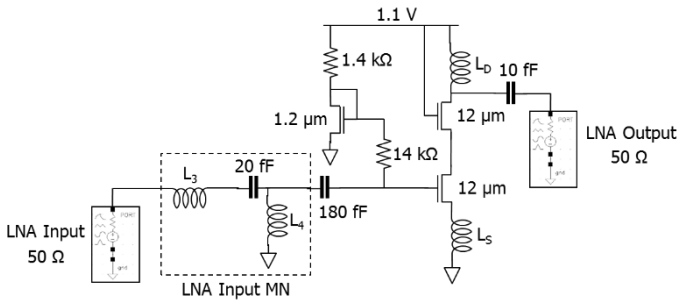


Fig. 2.5. Circuit schematic of the LNA.

transistor terminals are connected to the rest of the circuit using terminal embedding networks as shown in Fig. 2.2.

Once the optimum transistor size and bias point for simultaneous noise and impedance input match are chosen, a single optimum LNA source impedance is identified that will simultaneously guarantee a minimum LNA NF and a maximum LNA small signal gain. This is conceptually illustrated in the detailed LNA schematic shown in Fig. 2.6. A Cadence Spectre simulation is used to generate the constant NF and gain circles of the LNA circuit, as shown in Fig. 2.7. The circles help guide some further experimental simulations and allow determination of the optimum LNA source impedance, which is 150+j25 Ω. This source impedance is required for minimum NF and maximum small signal gain of the LNA at 94 GHz. It is noted that both NF goal and gain goal can be achieved simultaneously.

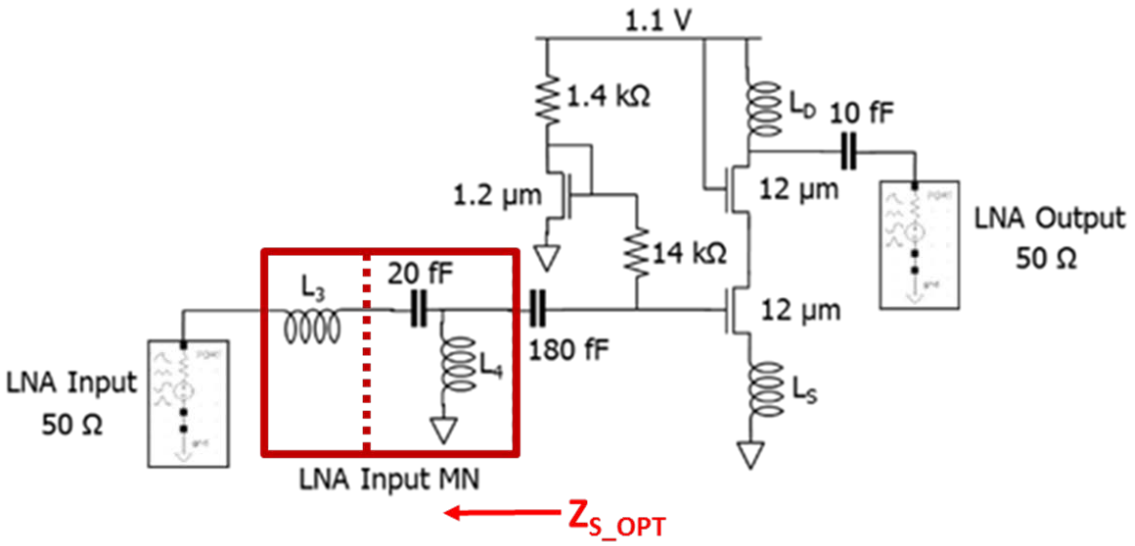


Fig. 2.6. A detailed circuit schematic of the 94 GHz cascode LNA design in 32SOI CMOS.

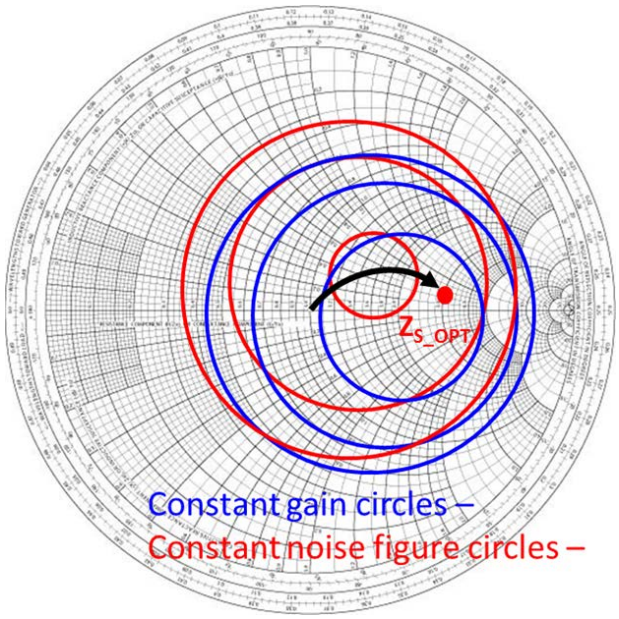


Fig. 2.7. LNA source impedance matching is done using the LNA constant gain and constant noise figure circles. The optimum source impedance, Z_{S_OPT} = 150+j25 Ω, was determined through simulation experimentation.

Then, the LNA input matching network is designed, whose purpose is to transform the 50 Ω impedance seen at the T/R switch, into the required LNA source impedance of 150+j25 Ω. With the chosen device size and bias point, a minimum LNA NF and a maximum LNA small signal gain are simultaneously achieved in the T/R circuit receive mode. At the same

time, LNA output impedance match to 50 Ω is achieved with minimal output matching network complexity (one series capacitor) and loss.

2.4 SPDT T/R Switch Design

The PA output and the LNA input are connected to the antenna port via a T/R SPDT switch, as shown in Fig. 2.8 below. The T/R switch design consists of two arms, as shown in Fig. 2.9, one for the antenna-to-LNA connection and another for antenna-to-PA connection. The arms are joined at the antenna port and each arm consists of a λ/4 transmission line with shunt nFETs at the opposite, amplifier port. A switch control signal toggles the transistors so that they are simultaneously biased "ON" in one arm and "OFF" in the other. When the transistors in one arm are biased "ON", the short circuit is transformed to an open circuit by the λ/4 transmission line, and the arm becomes isolated from the antenna port, leaving the other arm to provide a conductive path to the antenna. The λ/4 transmission lines are implemented in LB metal with ground on layer B1. The switch, previously fabricated and measured as a standalone test cell circuit, achieves < 2.2 dB of loss at 94 GHz.

2.5 Switch-based T/R Circuit Layout and Simulated Performance

The T/R circuit design presented in this dissertation includes thorough simulation of all transmission lines, lumped components, and transistor terminal embedding networks using their exact 32SOI layout geometries in the Sonnet EM simulator. All transistor models used in the simulations include post-layout extracted parasitics. The performance of the final T/R circuit was simulated using Cadence Spectre simulations. Each signal path was simulated separately and the measured loss of the T/R switch was approximated by inserting a 50 Ω, 2.2 dB, resistive attenuator into each path. Fig. 2.10 shows the simulated output power and the PAE of the T/R circuit in the transmit mode of operation.

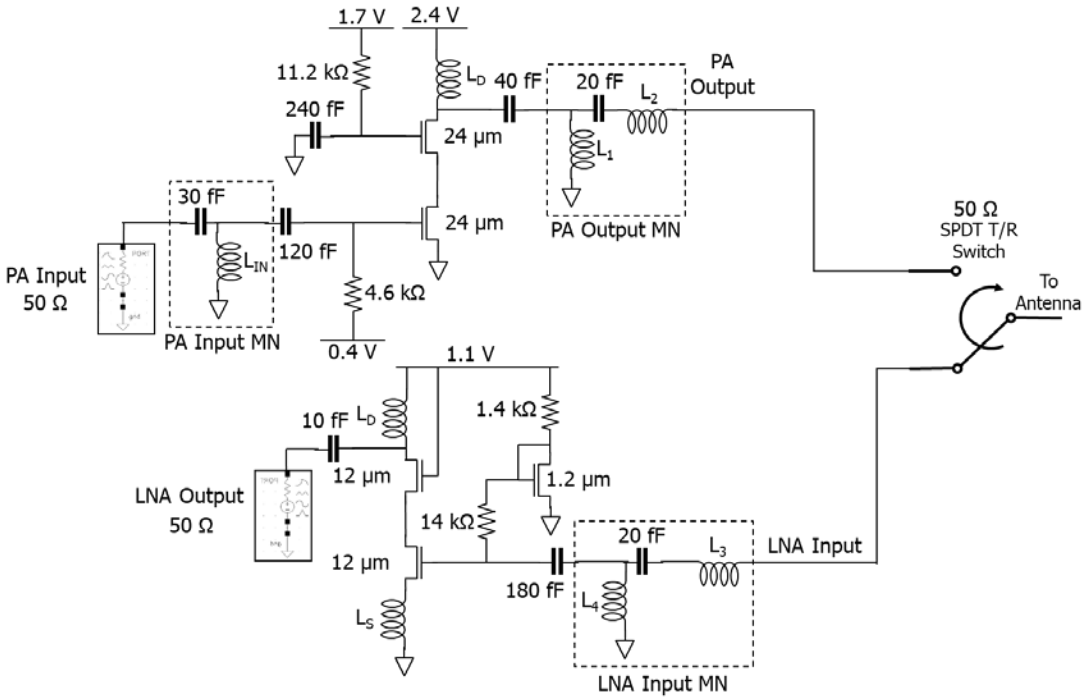


Fig. 2.8. 32SOI switch-based TR circuit schematic.

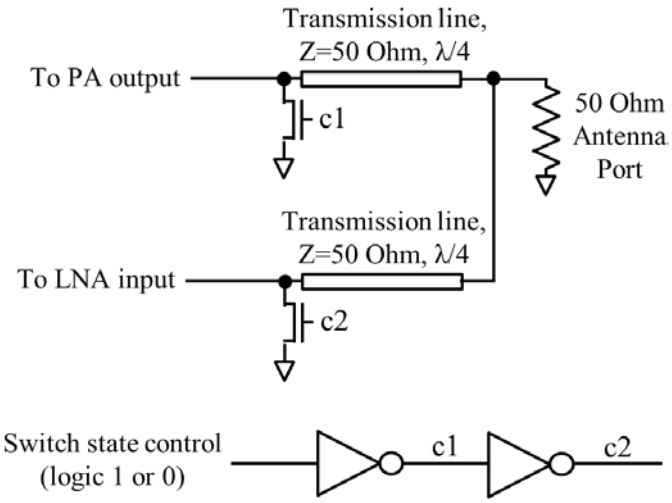


Fig. 2.9. Circuit schematic of the SPDT switch.

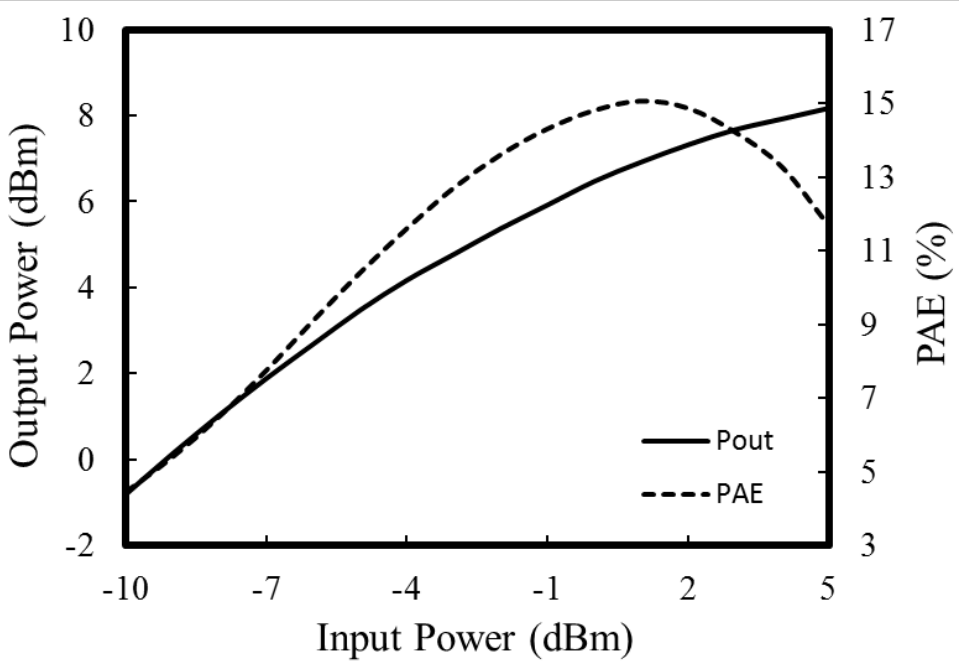


Fig. 2.10. Simulated large signal performance of the T/R circuit including switch loss in the transmit mode of operation.

The Class-E-like PA achieves a saturated output power of >8 dBm and maximum PAE of >15%, including 2.2 dB switch loss, at 94 GHz. Fig. 2.11 shows the simulated small signal s-parameters in the transmit mode of operation. Fig. 2.12 shows the simulated small signal s-parameters and NF of the T/R circuit in the receive mode of operation. Fig. 2.13 shows the layout of the T/R SPDT switch and the layout of the switch-based T/R circuit in 32SOI. Table 2.1 summarizes the simulated performance of the T/R circuit as well as comparison to other recently published works. The results presented in the published works, are all measured results. The simulated PAE of the PA only, excluding the T/R switch loss, exceeds 28 % at 94 GHz. Cascode LNA achieves NF of 6.5 dB and small signal gain of 8.8 dB, including 2.2 dB switch loss, at 94 GHz. As can be seen from Table 2.1, based on simulation, the presented circuit compares favorably to other similar circuits from literature, particularly in the PAE category. Therefore, the T/R circuit was fabricated and measured, as will be discussed in the next section.

In integrated circuit (IC) manufacturing, the interlevel dielectric (ILD) thickness variation must be carefully controlled in order for the IC to meet its performance and yield

requirements. Chemical-mechanical polishing (CMP), which is used in IC fabrication for planarizing interlayer dielectrics, is sensitive to metal layout patterns on individual metal layers [23]. Since no other technique is available for effectively controlling the dielectric thickness variation between metal layers, large open areas on metal layers are filled with a floating metal pattern during fabrication to compensate for metal pattern dependent variations in dielectric thickness. This process is known as metal-fill patterning. A more detailed description of this process is given in [23].

As discussed later in this work, the introduction of metal fill around and into transmission line structures causes loss, which results in performance degradation in RF ICs. Therefore, the issue of metal fill must be addressed. There are two possible approaches for addressing the issue:

1. By excluding metal fill during IC design using specially provided metal fill exclusion layers.

2. By designing RF circuits with the assumption that the metal fill would be added during fabrication. For example, coplanar waveguide (CPW) transmission line structure could be used to minimize the number of floating metal pieces that end up in close proximity to the center conductor. And, metal fill can be added in open areas by the designer, grounded, and designed into the overall RF IC design.

In order to maximize the circuit design performance, no fill presence was assumed in this work and metal fill exclusion layers were leveraged during layout to address the issue of metal fill. The metal fill exclusion layers can be identified in Fig. 2.13(b) as the brown rectangles placed on top of the layout-sensitive transmission line areas.

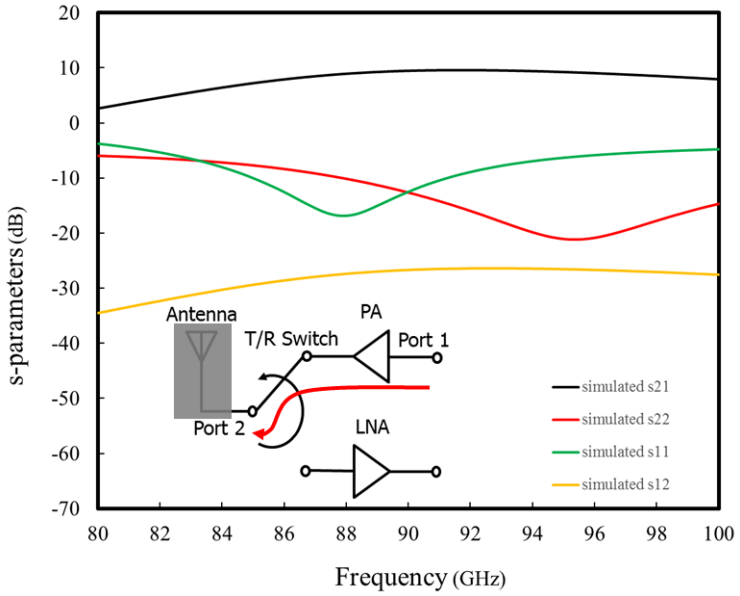
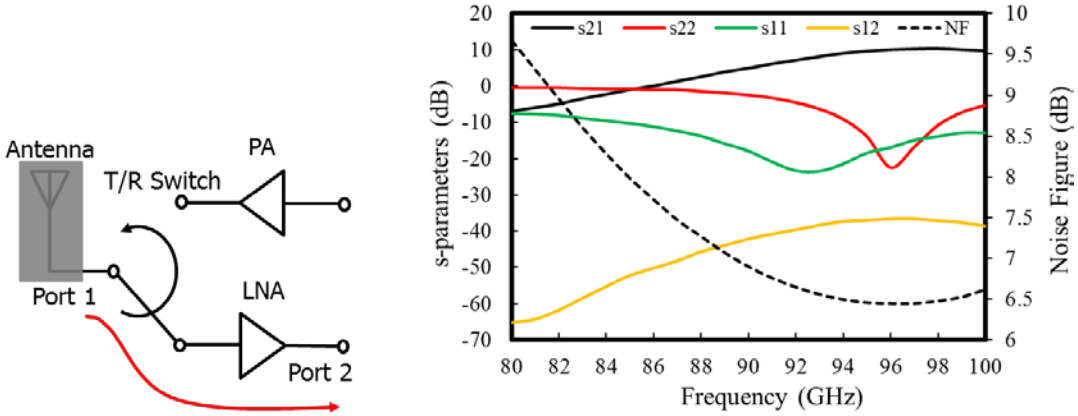
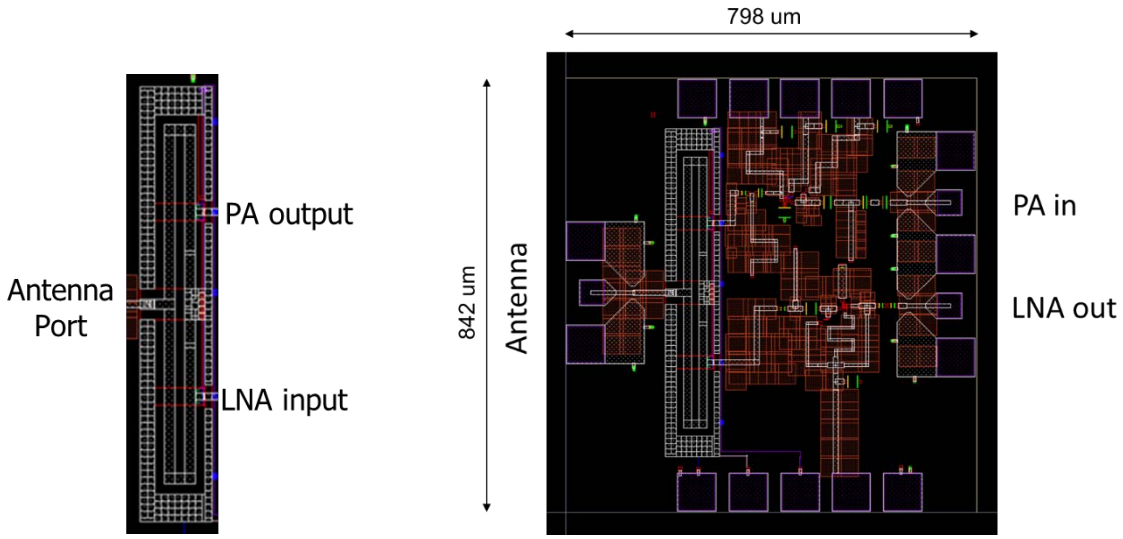


Fig. 2.11. Simulated small signal s-parameters performance of the T/R circuit including switch loss in the transmit mode of operation.



(a) (b)

Fig. 2.12. (a) High level schematic of the T/R circuit receive mode of operation. (b) Simulated small signal s-parameters performance of the T/R circuit including switch loss in the receive mode of operation.



(a) (b)

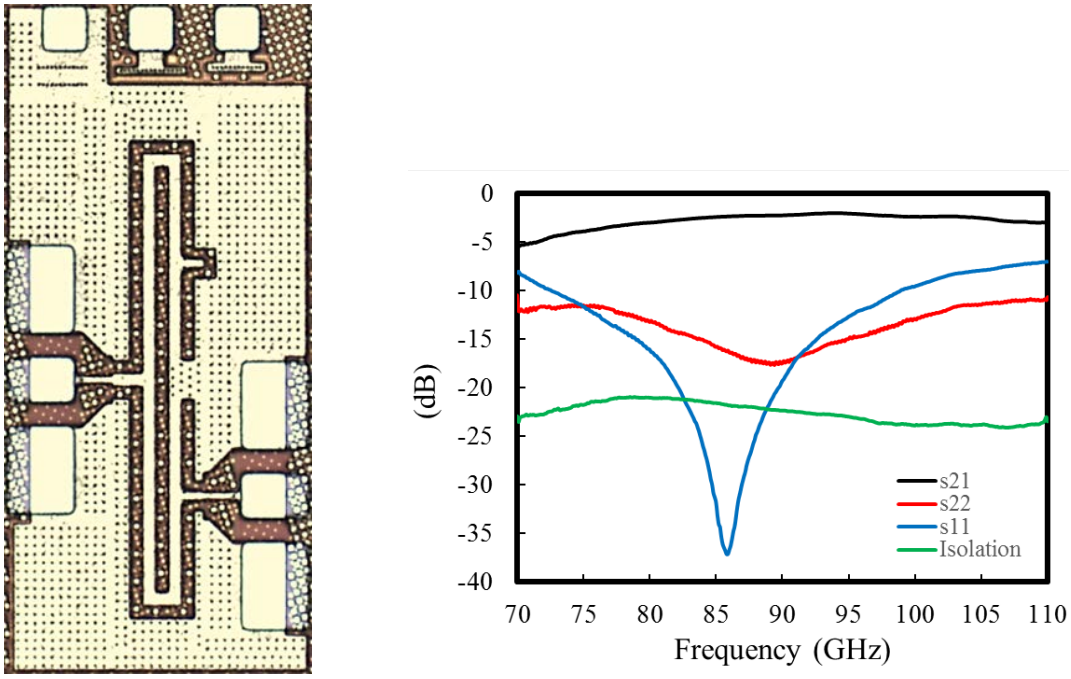
Fig. 2.13. (a) Layout of the T/R SPDT switch. (b) Layout of the switch-based T/R circuit.

Table 2.1.
T/R Circuit Simulated Performance Summary and Comparison With State-of-Art W-band Phased Array Front Ends.

Performance metric	**This work**	**[24]**	**[25]**	**[26]**	**[27]**	**[28]**	**[29]**
Technology	32 nm SOI CMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	180 nm SiGe BiCMOS	65 nm CMOS	130 nm SiGe BiCMOS
Frequency (GHz)	94	94	94	94	76	96	94
Tx Saturated output power (dBm)	> 8	7	-5	3	18	-12	6.4
Tx Maximum PAE (%)	> 15	< 2	< 0.02	1.7	4	0.02	4
Tx Maximum power gain (dB)	> 10	-	13	> 25	30	0	30
Rx Small signal gain (dB)	8.8	> 30	20	30	15	20	25-38
Rx NF (dB)	6.5	6	9	8.2	> 10	-	12.5
Phase shifters / TR switch included (yes or no)	no/yes	yes/no	yes/no	yes/yes	no/no	no/no	yes/no

2.6 Experimental Results

Fig. 2.14 shows the photograph of the T/R SPDT switch standalone test cell and the associated measurement results. The switch achieves less than 2.2 dB of insertion loss at 94 GHz and more than 20 dB of isolation from 70 GHz to 110 GHz, which is comparable to switch results presented in [25]. Integrated W-band switch architectures presented in



(a) (b)

Fig. 2.14. (a) Chip photograph of the SPDT switch circuit. (b) Measured performance of the SPDT switch. Chip photo and measured switch data were provided through the courtesy of Dr. M. Sayginer, Nokia Bell Labs.

[30] and [31] have a higher insertion loss at 94 GHz, however they also have higher isolation.

Based on excellent simulated performance of the switch-based T/R circuit presented above, the proposed T/R circuit was taped-out through TAPO and the chips were fabricated in the 32SOI technology. Fig. 2.15 shows the chip photograph of the T/R circuit. Probe station measurements of the chip were made and the small signal gain values, s_{21}, were found to be 10 dB and 9 dB smaller than the simulated values at 94 GHz in transmit and receive, respectively. Fig. 2.16 and Fig. 2.17 show the preliminary comparisons of small signal s-parameter simulated and measured results for the switch-based T/R circuit in the transmit mode and the receive mode of operation, respectively. Table 2.2 shows the summary comparison of the simulated and the measured results for the switch-based T/R circuit.

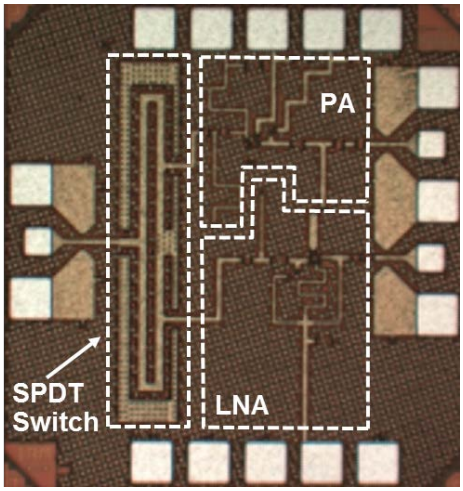


Fig. 2.15. Chip photograph of the switch-based T/R circuit.

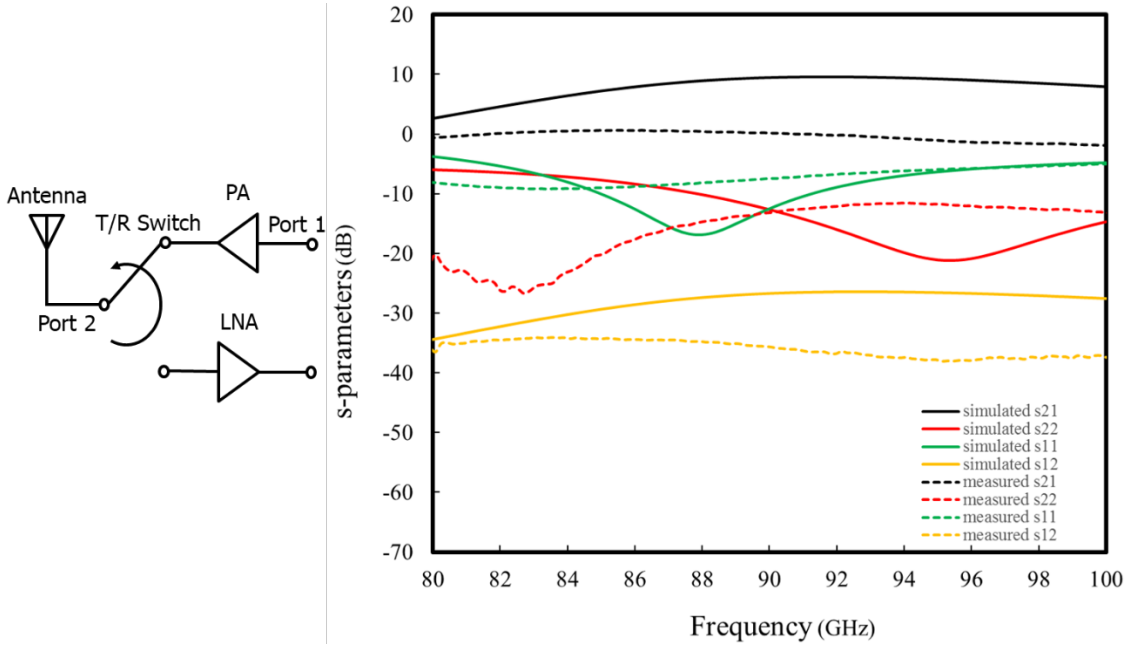


Fig. 2.16. Preliminary comparison of small signal s-parameter simulated and measured results for the switch-based T/R circuit in the transmit mode of operation.

In summary, the following degradations and discrepancies between the simulated and measured results are noted: (a) large drop in gain; (b) shift down in frequency; and (c) return loss degradation. Closer inspection of the chip revealed extensive presence of metal fill artifacts on metal layers LB, MA, and MB, which were inserted around and into the circuit transmission line structures during fabrication; this was unexpected since fill had been excluded in those locations in layout.

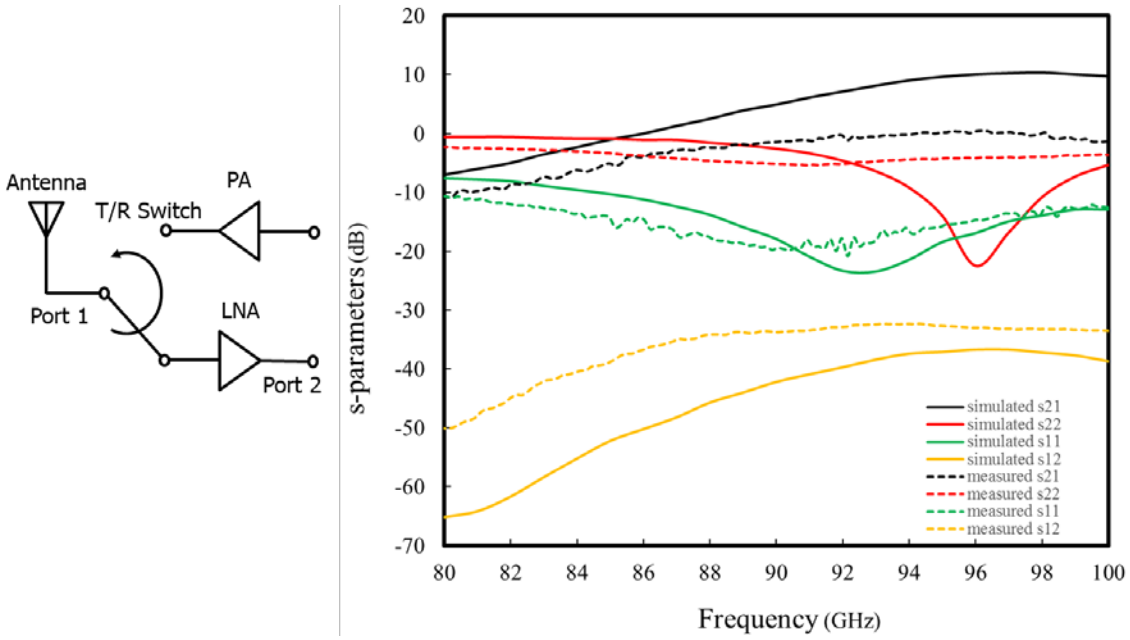


Fig. 2.17. Preliminary comparison of small signal s-parameter simulated and measured results for the switch-based T/R circuit in the receive mode of operation.

Table 2.2.
Summary Comparison of the Simulated and the Measured Results for the Switch-based T/R Circuit.

	PA+LNA+SPDT*
Design Frequency [GHz]	94
Small signal Tx Gain [dB]	9.5 (simulated at 94 GHz) 0.7 (measured at 85.5 GHz)
Tx power consumption [mW]	25.3 (11 mA at 2.3 V)
Small signal Rx Gain [dB]	9 (simulated at 94 GHz) 0.5 (measured at 96.2 GHz)
Rx power consumption [mW]	12.6 (7 mA at 1.8 V)

(*) Simulation based on a measured 2.2 dB SPDT loss (updated based on switch measurements done after the PALNA circuit design)

Subsequent EM simulations of the taped out circuit with the metal fill inserted have shown that the metal fill is the main cause of the above-mentioned degradations. The simulation effort to understand and reconcile the differences between the original simulated results and the measured results is described in detail below.

Fig. 2.18 shows four photographs of the switch-based T/R circuit. In Fig. 2.18(a), a picture

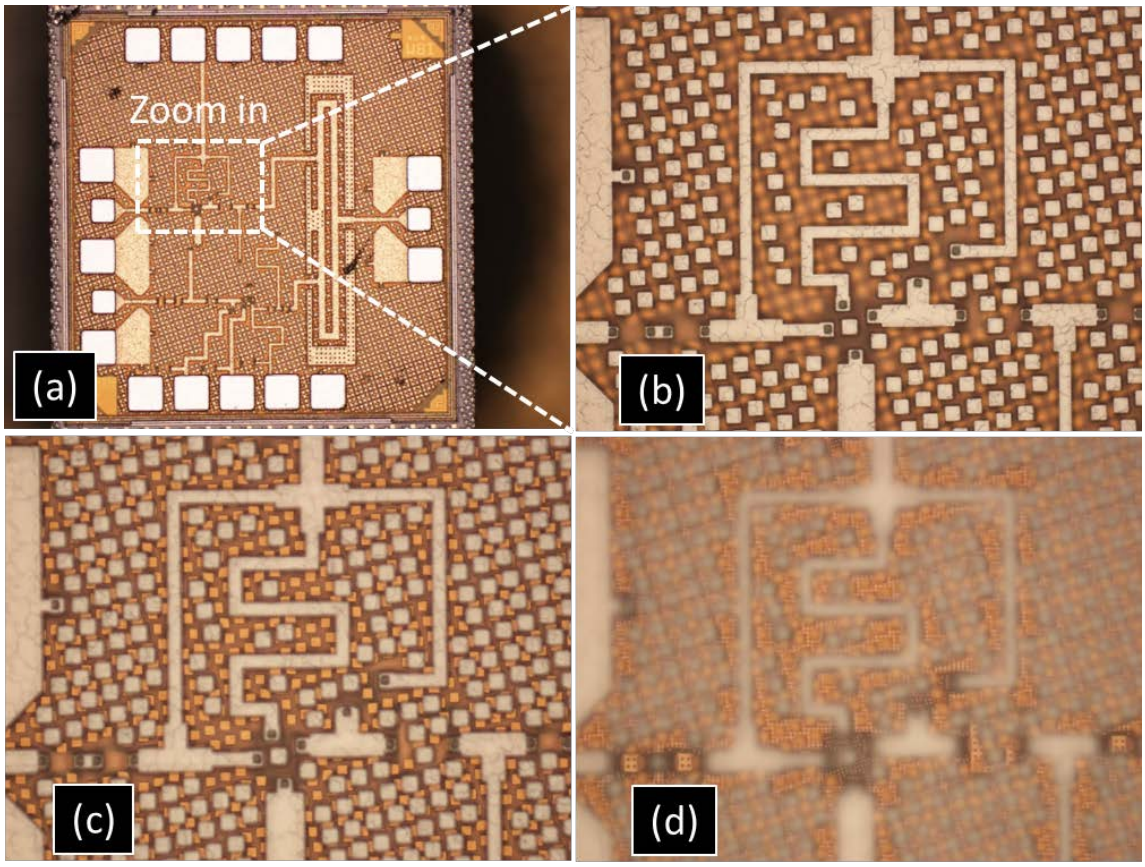


Fig. 2.18. Switch-based T/R circuit chip photographs showing metal fill inserted during the 32SOI16A tapeout. (a) A circuit area is selected for zoom-in. (b) Top metal (LB) fill squares are seen to be very close to transmission lines. (c) MA layer, MB layer, or both metal fill squares are located under the transmission lines. (d) Focus adjustment reveals layer E1 ground plane ("fine mesh"), which is below the MA and MB layer fill squares.

of the entire T\R chip is seen with an area designated by the white dashed boundary lines for camera zoom-in and further examination. In Fig. 2.18(b), the zoomed-in area of the chip is shown with the camera focused on the top metal layer where the circuit's microstrip transmission lines are located. It can be seen that there are numerous metal fill squares dispersed around the transmission lines, which is undesirable from the transmission line performance perspective. In particular, metal fill was found to make transmission lines lossy [32] - [34]. Further, as can be seen in Fig. 2.18(c), the camera focus is adjusted to look beyond the top metal layer and numerous, smaller metal fill squares of dark yellow color are seen to be located under the transmission lines. And, even further, as can be seen in Fig. 2.18(d) with further adjustment of the camera focus to look deeper into the circuit,

a fine 4-micron mesh appears, which is the intended ground plane for the circuit's transmission line structures. Therefore, it can be concluded that metal fill is present both around and directly inside the circuit's transmission line structures.

The discovery of this was very surprising since the metal fill was specifically excluded in the circuit layout, using specific metal-exclusion layers. However, given this new understanding of a potential cause for circuit performance degradation, the circuit simulation was updated, as shown in Fig. 2.19 below. In particular, per model described in [33], metal fill was added (first, second, and some third neighbors) around transmission lines, capacitors, and embedding networks. Additionally, since the GSG pads of the T/R circuit could not be calibrated out during the measurements, the GSG pads representative EM-simulated s-parameter model files were included in the circuit simulation. Finally, it was noticed by analyzing the measurement results that there was a shift downward in frequency from 94 GHz, which was not present in the simulation results. It was discovered through analysis and simulation that the T/R switch model needed updating. Since switch measurements and a refined RF model were not available at the time when the T/R circuit was being designed, the switch was modeled using a 50 Ω resistive network. While this allowed the inclusion of the switch loss, the full RF behavior of the switch was not captured. The updated T/R switch model consisted of EM-simulated λ/4 lines with slightly increased length of PA and LNA input and output matching network stubs, to reflect the measured shift downward in frequency. When the circuit model update was completed, the circuit was re-simulated in Cadence and the results are shown in Fig. 2.20 and Fig. 2.21. Fig. 2.20 and Fig. 2.21 show the comparison of the updated small signal s-parameter simulation results and the measured results in the transmit mode and the receive mode, respectively. As can be seen, the simulation results match the measured results reasonably well and it may be concluded that the addition of the metal fill, the GSG pads, and the updated RF switch model into the simulation explains the measured T/R circuit results.

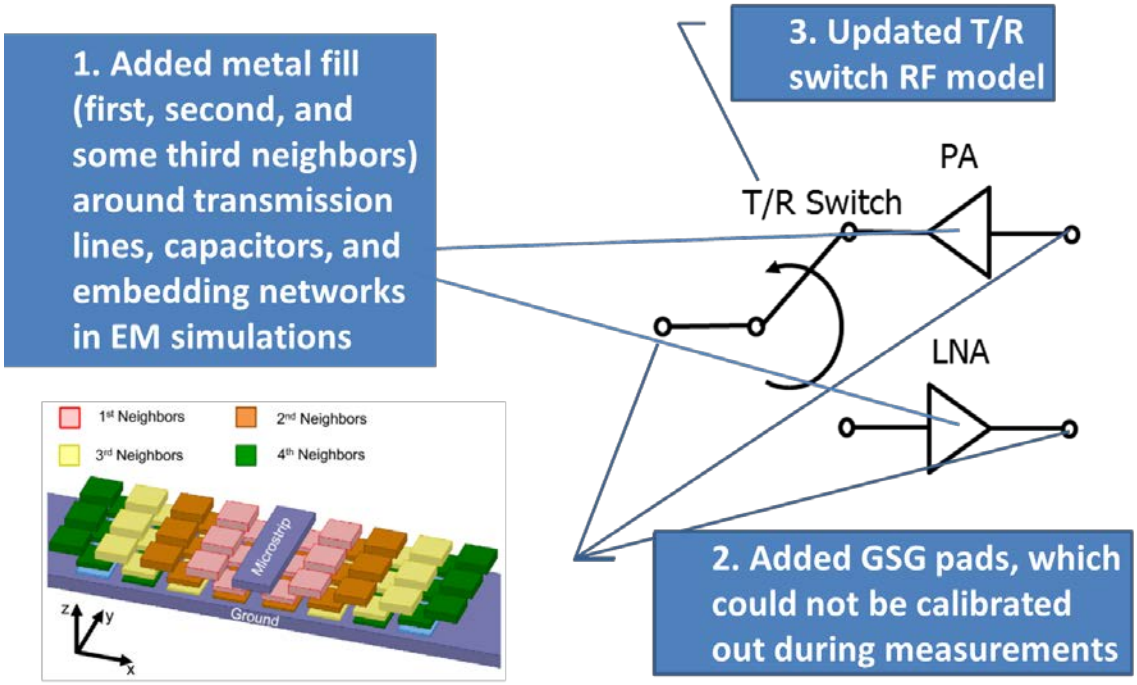


Fig. 2.19. Updated T/R circuit simulation. The metal fill graphic was taken from [33].

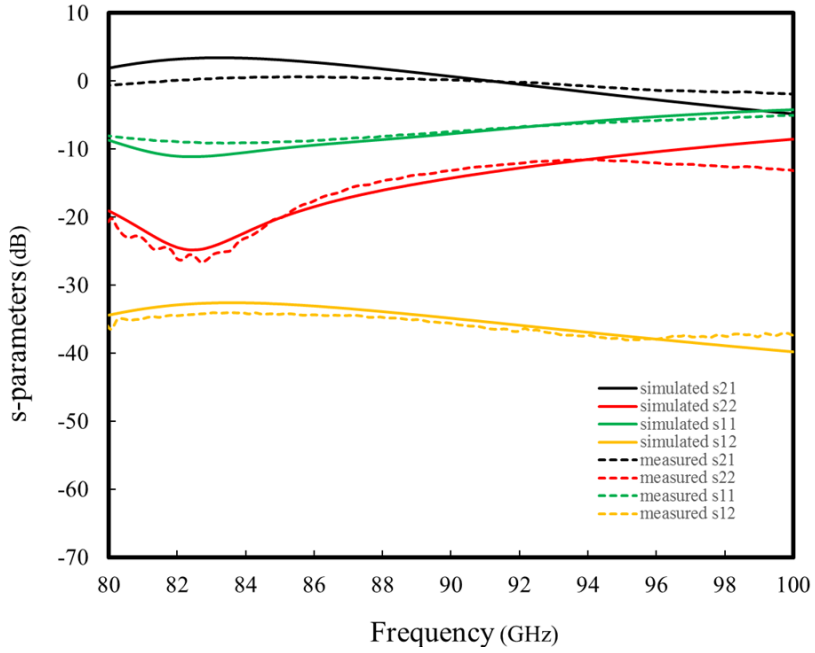


Fig. 2.20. Comparison of updated small signal s-parameter simulation results and measured results in the transmit mode of operation.

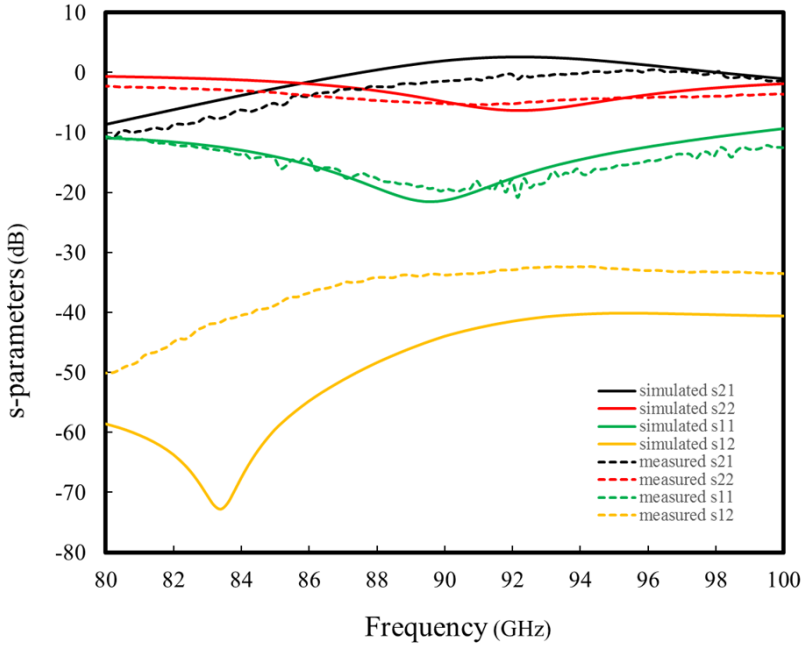


Fig. 2.21. Comparison of updated small signal s-parameter simulation results and measured results in the receive mode of operation.

2.7 Summary

An efficient, switch-based T/R circuit design in 32SOI technology is presented in this chapter and its three major component sub-circuits were discussed in detail (PA, LNA, and SPDT T/R switch). Simulated and measured performance results of the circuit were presented. The circuit achieves maximum power added efficiency of 15 % in transmit and noise figure of 6.5 dB in receive at 94 GHz in simulation. The simulation includes a thorough accounting of circuit nonidealities, except the metal fill artifacts around and in the transmission line structures, which were inserted during the circuit fabrication. The simulated performance of the circuit compares favorably to performance of other similar circuits reported in literature.

Chip fabrication metal fill issue was studied and discussed and chip measurements were reconciled with the original simulation through specific simulation updates. It may be concluded that the metal fill inserted at the foundry is by far the largest cause of small signal gain loss. The GSG pads account for ~1 dB of loss. And, the SPDT T/R switch RF model needed to be updated to account for slight frequency translation downward, which was observed in measurements but not seen in the original simulation.

Future work should focus on further improving the PAE of the PA, which is currently 28 % in simulation at 94 GHz with the T/R switch loss excluded.

Chapter Three: **A 94 GHz Switchless PALNA Leveraging Existing 50 Ω Power Amplifier and Low Noise Amplifier**

3.1 Technology Overview and Considerations

The 32SOI process used for this design is a 12-metal aluminum and copper process. In order to maximize Q of the transmission lines, the top four metal layers (LB-MB-MA-E1) are used to implement the transmission lines as microstrips with the LB layer serving as the signal layer and the E1 layer serving as the ground layer. No metal or vias are used on layers between LB and E1, and those intervening layers are filled with dielectric. Fig. 3.1 shows the structure of the transmission lines designed in 32SOI.

3.2 PALNA Approach Methodology

In this particular design, the LNA MN and the PA MN shown in Fig. 1.5 above were implemented using transmission lines and a small signal 50 Ω impedance matching approach was pursued. This means that only small signal circuit parameters were considered and that both the PA and the LNA cells include 50 Ω matching networks such that, in normal "on" operation, both cells are matched to 50 Ω at both input and output. In transmit mode (PA bias is on, LNA bias is off), the characteristics of the LNA MN and PA MN transmission lines are chosen to provide an optimum output impedance, Z_L, for the power amplifier for maximum small signal gain. Simultaneously, in receive mode (PA bias is off, LNA bias is on), the same transmission lines provide optimum source impedance, Z_S, to the LNA required for minimum noise figure and acceptable small signal gain. Fig. 3.2 illustrates a step-by-step design flow of the PALNA matching network.

Step 0: The PA and the LNA core circuits leveraged in this PALNA design were previously designed and simulated using small-signal Cadence Spectre simulations. The resulting s-parameter files, for the PA and the LNA ON-state and OFF-state, were provided for use in this PALNA design. Both circuit designs contained matching networks for 50 Ω input and output match. Therefore, this PALNA design flow begins by characterizing the PA and the LNA circuits by simulating further the provided s-parameter files to determine the ON-state, the OFF-state, and the optimal impedance for each circuit. Then, the PALNA matching network is designed by following the following three steps.

Step 1: First, The initial versions of the matching network that simultaneously achieves the optimal PA and LNA impedances are designed. For the transmit mode, the optimum PA load impedance is defined as the impedance that maximizes the power transfer out of the ON-state PA and thus maximizes the small signal gain. For the receive mode, the optimum LNA source impedance is defined as the impedance that minimizes the NF and produces good small signal gain. Fig. 3.3 and Fig. 3.4 show the PALNA transmit and receive impedance matching conditions, respectively.

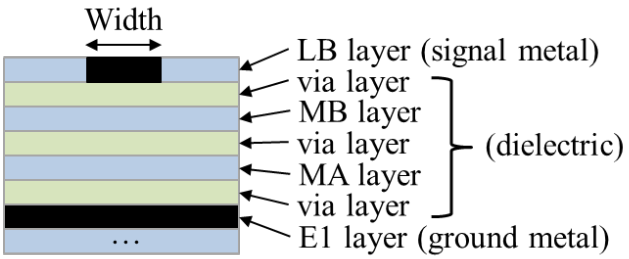


Fig. 3.1. The cross-section of the transmission lines used in this PALNA design. Microstrip substrate parameters are not provided due to proprietary restrictions.

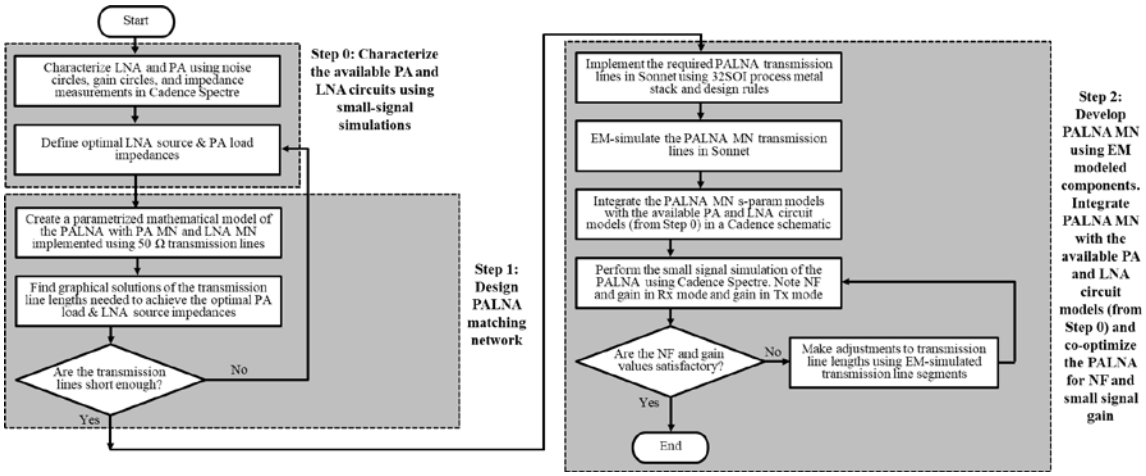


Fig. 3.2 Design approach flowchart for the 50 Ω PALNA.

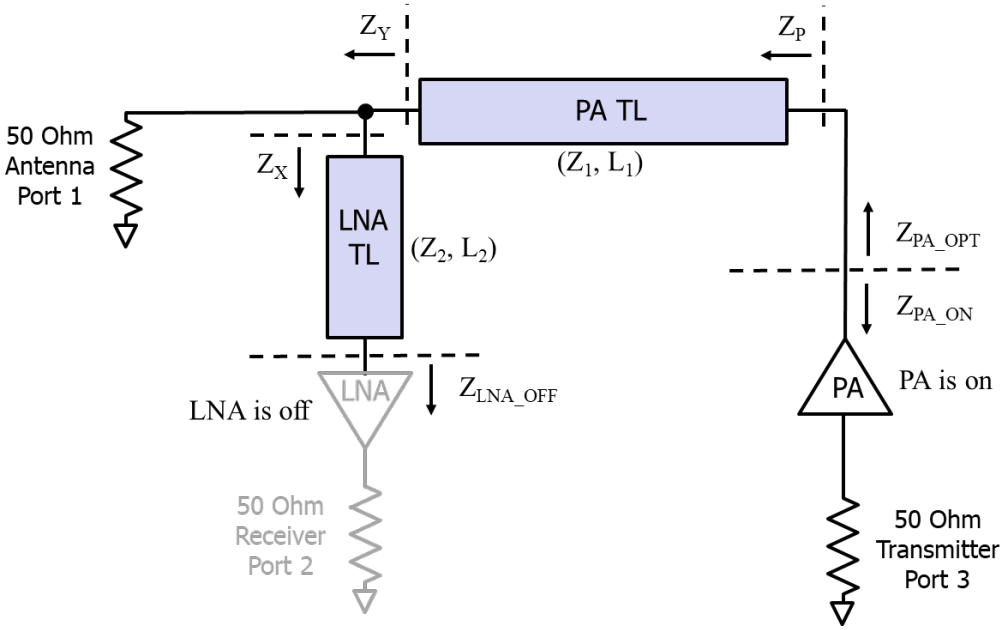


Fig. 3.3. Switchless PALNA transmit matching condition.

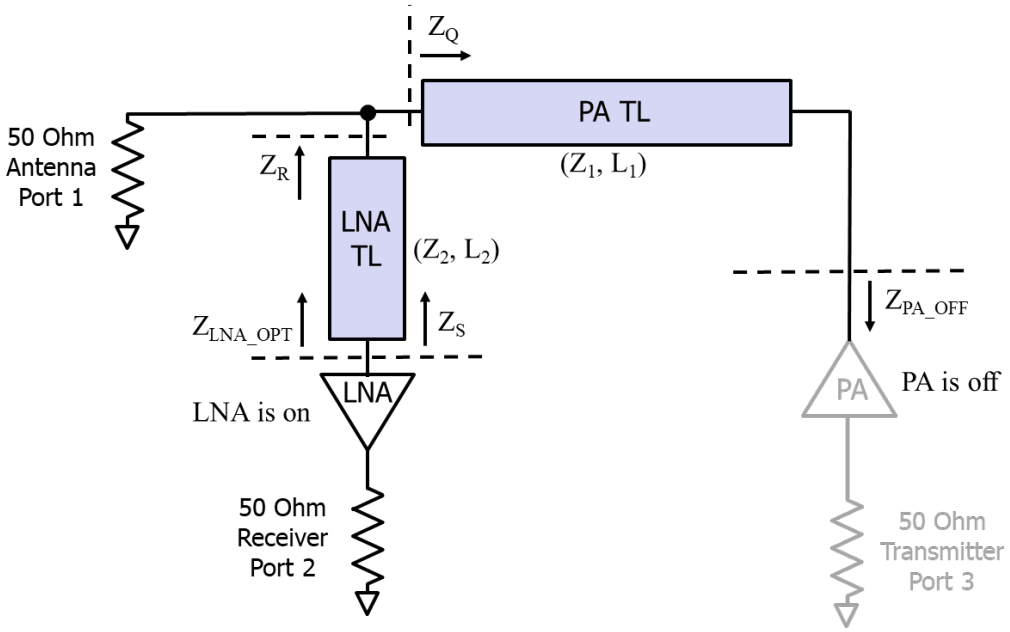


Fig. 3.4. Switchless PALNA receive matching condition.

The matching conditions can be described mathematically as follows. For transmit, the impedances Z_X, Z_Y, and Z_P are given by (3.1) - (3.3). In order to achieve the optimum PA performance, which in this design is defined as the maximum small signal gain, the output impedance Z_P seen by the on-state PA needs to equal the pre-determined optimum output impedance Z_{PA_OPT}, as shown in (3.4), which is the transmit mode impedance matching condition.

$$Z_X = \frac{Z_2 \cdot \left[Z_{LNA\_OFF} + jZ_2 \tan \beta l_2\right]}{\left[Z_2 + jZ_{LNA\_OFF} \tan \beta l_2\right]} \tag{3.1}$$

$$Z_Y = \frac{Z_X \cdot 50}{Z_X + 50} \tag{3.2}$$

$$Z_P = \frac{Z_1 \cdot [Z_Y + jZ_1 \tan \beta l_1]}{[Z_1 + jZ_Y \tan \beta l_1]} \tag{3.3}$$

$$Z_P = Z_{PA\_OPT} \tag{3.4}$$

For receive, the impedances Z_Q, Z_R, and Z_S are given by (3.5) - (3.7). In order to achieve the optimum LNA performance, which in this design is defined as the minimum NF and a good small signal gain, the input impedance Z_S seen by the on-state LNA needs to equal the pre-determined optimum input impedance Z_{LNA_OPT}, as shown in (3.8), which is the receive mode impedance matching condition.

$$Z_Q = \frac{Z_1 \cdot \left[Z_{PA\_OFF} + jZ_1 \tan \beta l_1\right]}{\left[Z_1 + jZ_{PA\_OFF} \tan \beta l_1\right]} \tag{3.5}$$

$$Z_R = \frac{Z_Q \cdot 50}{Z_Q + 50} \tag{3.6}$$

$$Z_S = \frac{Z_2 \cdot [Z_R + jZ_2 \tan \beta l_2]}{[Z_2 + jZ_R \tan \beta l_2]} \tag{3.7}$$

$$Z_S = Z_{LNA\_OPT} \tag{3.8}$$

Equations (3.4) and (3.8) express the design criteria of the PALNA circuit. In order to determine the lengths of the transmission lines needed to achieve the design criteria in both modes of operation, a computer-based graphical approach is pursued using MATLAB. In this PALNA design, $Z_1 = Z_2 = 50\ \Omega$, so (3.4) and (3.8) have two unknowns, namely l_1 and l_2. For (3.4), the design space can thus be plotted in the (l_1, l_2) plane by varying βl_2 from $-\pi/2$ to $+\pi/2$ in increments of $\pi/100$ and solving for l_1 for each value of βl_2. Similarly, for (3.8), the design space can be plotted in the same (l_1, l_2) plane by varying βl_1 from $-\pi/2$ to $+\pi/2$ in increments of $\pi/100$ and solving for l_2. A MATLAB is written to implement (3.1) – (3.8), solve for l_1 and l_2, and plot both curves in the (l_1, l_2) plane. Each curve represents a single mode of operation, transmit or receive, and the associated impedance matching condition. Each point in the (l_1, l_2) plane where the two curves intersect is a PALNA design solution, a (l_1, l_2) pair defining the transmission line lengths for which both of the impedance matching conditions are met simultaneously.

MATLAB-based graphical solution is convenient and simple to implement, and the circuit parameter design space can be fully explored. On the other hand, if the MATLAB-based approach is replaced by manual optimization in a circuit design tool (e.g. Cadence in this work), the MN design process would require extensive trial-and-error and the MN performance outcome would be uncertain.

Step 2: Then, to include the dissipative losses of the transmission lines, the PALNA MN is implemented and simulated in Cadence, using Global Foundries 32SOI EM-simulated transmission lines s-parameter models. Particular attention is paid to practical considerations such as required length of the transmission lines, and physical size of the overall matching network layout. If the matching network is deemed practical from the implementation point of view, it is integrated with the PA and LNA circuits and co-optimized manually using Cadence Spectre small signal simulations. The co-optimization procedure involves manually switching between the transmit and the receive modes of operation, simulating the performance of interest, and manually adjusting the transmission line lengths to fine-tune the performance in each mode. In particular, in the transmit mode, the performance is optimized using the small signal s-parameters. In the receive mode, the performance is optimized using the noise circles, the NF, and small signal s-parameters. The matching network parameters adjusted are transmission line lengths.

3.3 PALNA Design and Implementation

Step 0: The ON/OFF/optimal impedances for the PA and the LNA at 94 GHz are obtained by using Cadence Spectre small signal simulations. In particular, the ON and OFF impedance of each circuit is obtained as a complex Z_{11} parameter, with circuit biasing in ON and OFF state, respectively. For the PA, the optimum load impedance is the impedance that guarantees the maximum power transfer out of the ON-state PA, which is $Z_{PA\_OPT} = Z_{PA\_ON}^*$. Since Z_{PA_ON} of the PA is 25+j12 Ω, Z_{PA_OPT} = 25-j12 Ω. For the LNA, the gain and noise circles are plotted on one Smith chart and a suitable source impedance is selected for minimum NF and good small signal gain. Fig. 3.5 shows the constant NF circles and

constant gain circles of the LNA at 94 GHz. Based on the circle locations, Z_{LNA_OPT} = 40-j20 Ω, by definition. Table 3.1 summarizes the simulated impedances of the PA and LNA core circuits discussed above.

As discussed above, a three-step process is then followed to complete the PALNA circuit design.

Step 1: As described above, a parametrized model of the PALNA circuit is implemented in MATLAB and a graphical solution approach is pursued. Fig. 3.6 shows the plot of the transmit/receive condition curves for this particular PALNA design in the (l_1, l_2) plane. By inspection, we see that the curves intersect at five different points, which means that there exist five distinct solutions for the PALNA design problem at hand. Since transmission lines have losses and take up valuable die surface, the solution that requires the shortest lines is the best. As shown in Fig. 3.6, this solution occurs when $\beta l_1 = 1.049$ and $\beta l_2 = 0.1595$. Since the theoretical wavelength λ at 94 GHz is approximately 3192 μm, the corresponding physical lengths of the transmission lines can be calculated as follows:

$$l_1 = \frac{1.049}{2\pi}\lambda = \frac{1.049}{6.28} * 3192\ \mu m = 533\ \mu m \tag{3.9}$$

$$l_2 = \frac{0.1595}{2\pi}\lambda = \frac{0.1595}{6.28} * 3192\ \mu m = 81\ \mu m \tag{3.10}$$

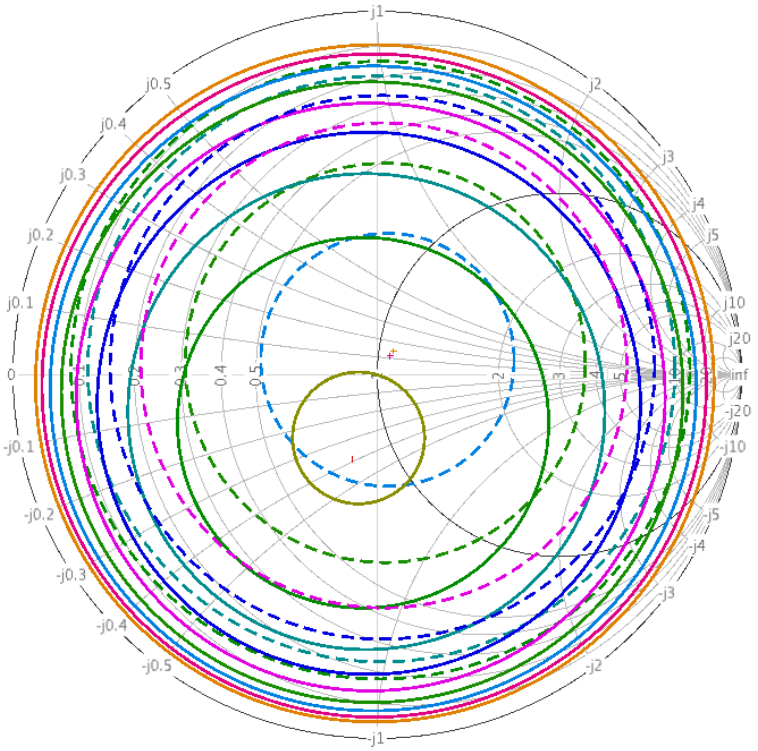


Fig. 3.5. Constant NF circles and constant gain circles define the optimum source impedance for the LNA at 94 GHz. Constant NF circles are shown using solid lines and constant gain circles are shown using dashed lines. The innermost circles represent 4 dB and 20 dB, for NF and gain. NF circles increase in 1 dB steps and gain circles decrease in 1 dB steps. The optimum source impedance is selected to be 40-j20 Ω, at the approximate location of the red mark inside the 4 dB NF circle.

Table 3.1.
Impedances Associated With the Core PA and LNA Circuits at 94 GHz.

	ON Impedance [Ω]	**OFF Impedance [Ω]**	**Optimal Impedance [Ω]**
PA Output	25+j12	15+j3	25-j12
LNA Input	54-j8	17+j47	40-j20

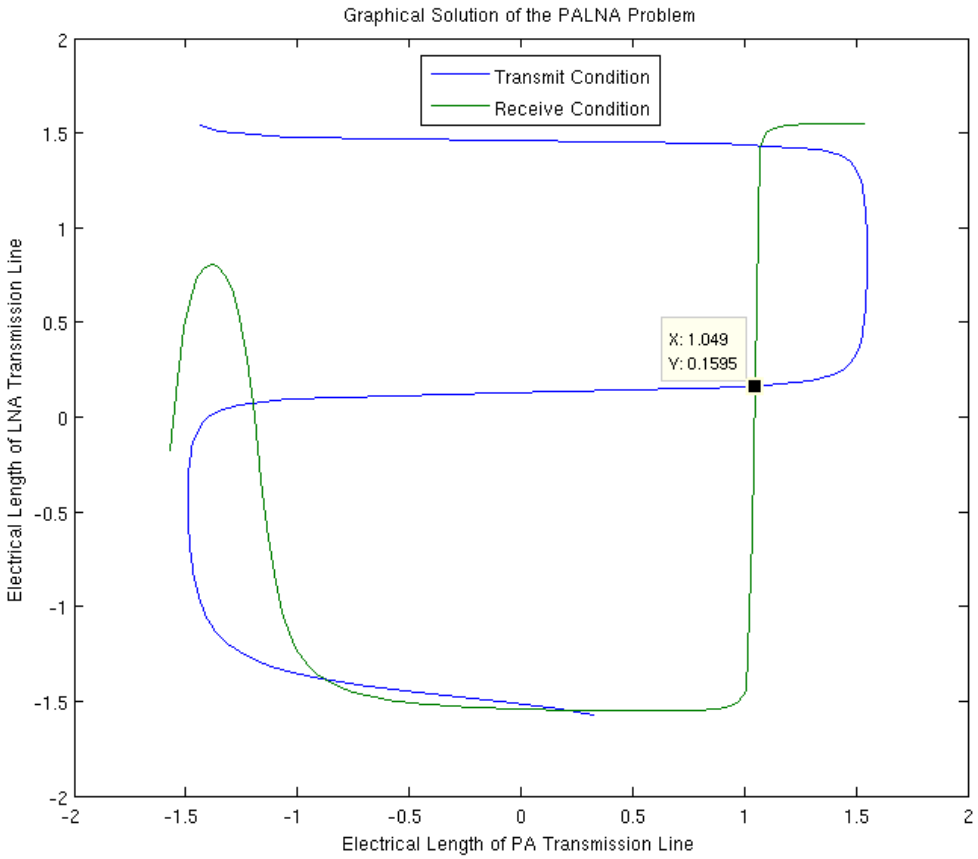
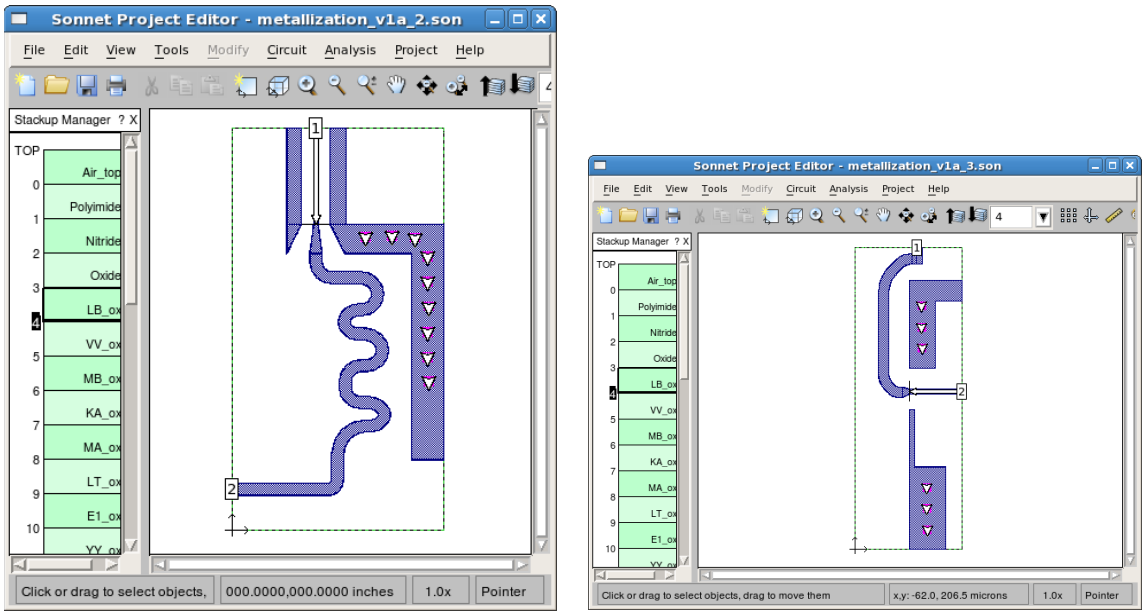


Fig. 3.6. MATLAB simulation generated transmit/receive condition curves for this PALNA design. Five PALNA solutions exist at the five points where the curves intersect. The solution that requires the shortest transmission lines is considered the best.

Step 2: After the lengths of the required transmission lines are calculated, EM models of the transmission lines are implemented using Sonnet. The exact 32SOI technology metallization stackup is used in the Sonnet models, as shown in Fig. 3.1 above, and the transmission lines are implemented as microstrips, assuming that the signal metal is on LB layer and the ground is on the E1 layer. Initially, the transmission lines are implemented using straight transmission line segments, which is helpful because the line lengths have to be adjusted through an iterative PALNA simulation process for best circuit performance. Sonnet EM simulations generate s-parameter models, which are integrated into a Cadence Spectre schematic with the available PA and LNA s-parameter circuit models. Then, the overall PALNA circuit schematic is simulated using the Spectre small signal simulation. In this design step, the Cadence simulation is manually switched between the transmit and the receive mode, and the lengths of the PALNA MN transmission lines are manually

adjusted until satisfactory performance is obtained in both modes. In transmit, the PALNA is optimized for small signal gain while maintaining stability. In receive, the PALNA is optimized for small signal gain and NF while maintaining stability. When the design procedure is completed and satisfactory performance is obtained in both modes of operation, the full transmission lines are implemented in Sonnet with their exact layout geometries and the small signal simulations are repeated with their s-parameter models until the expected PALNA performance is achieved. Fig. 3.7 shows the final Sonnet models of the PA and LNA transmission lines developed in this design, respectively. The transmission line structures are microstrips, except for the structure at the input of the PA, which is a CPW. Appropriate CPW-to-microstrip transitions were designed and included in the Sonnet simulations, as shown in Fig. 3.7.

Since it was anticipated that the calibration standards would not be available, which would allow de-embedding of the GSG probe pads during final circuit measurements, GSG pads were also EM modelled in Sonnet (using the exact 32 SOI stack-up and assuming that the signal metal is on LB layer and the ground is on the E1 layer) and their s-parameter models were included in the design schematic. Fig. 3.8 shows the final, labeled Cadence Spectre schematic of the overall PALNA circuit. Except for the three ideal 50 Ω ports, all circuit components (the PA, the LNA, the transmission lines, and the GSG pads) are represented by their s-parameters models. The final lengths of the PA and LNA MN transmission lines are 436 μm and 144 μm, respectively. The width of each 50 Ω transmission line is 10 μm. The next section includes the summary of the PALNA circuit simulation results.



(a) (b)

Fig. 3.7. Sonnet EM model of: (a) PA transmission line; (b) LNA transmission line.

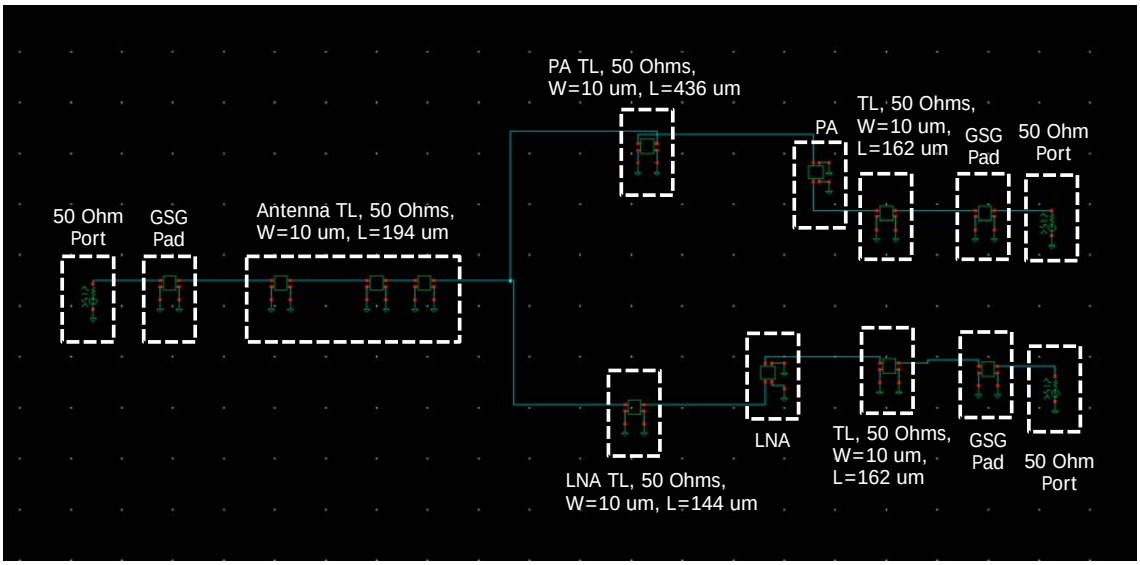


Fig. 3.8. Cadence schematic of the PALNA circuit.

3.4 Simulation Results

Fig. 3.9 – Fig. 3.11 show the final simulated small signal performance of the designed PALNA circuit in both the transmit and the receive mode of operation.

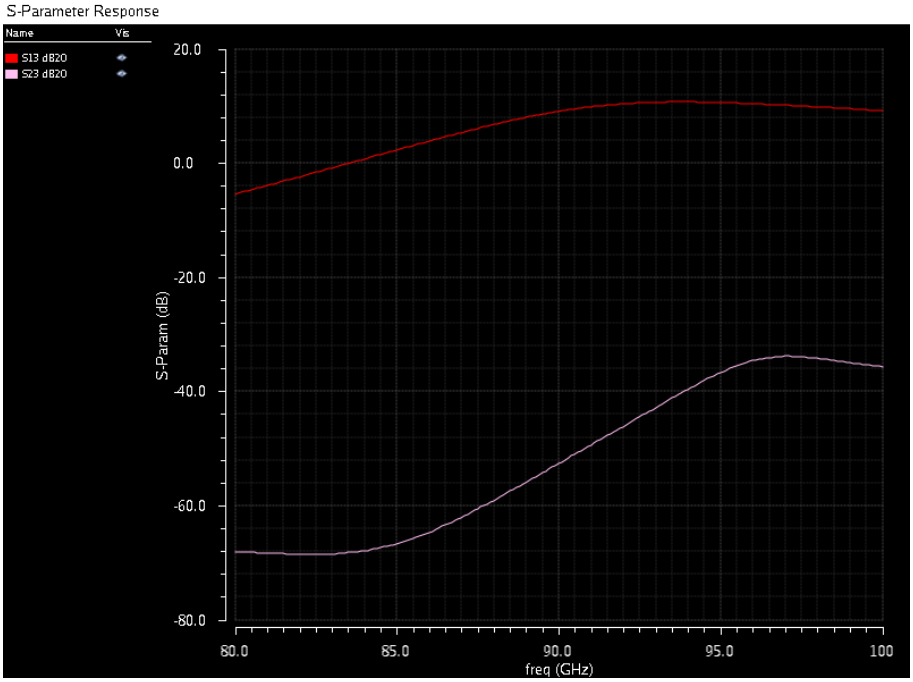


Fig. 3.9. Simulated gain of the PALNA circuit in the transmit mode (red curve), leakage into the receive port (white curve), and transmit-to-receive isolation (the difference between the two curves).

The simulations were done using Cadence Spectre. Fig. 3.9 shows the simulated small signal gain of the PALNA in the transmit mode, along with the leakage into the receiver and the implied transmit-to-receive isolation. Fig. 3.10 shows the simulated PALNA gain realized in the receive mode. Fig. 3.11 shows the simulated noise figure of the PALNA circuit in the receive mode.

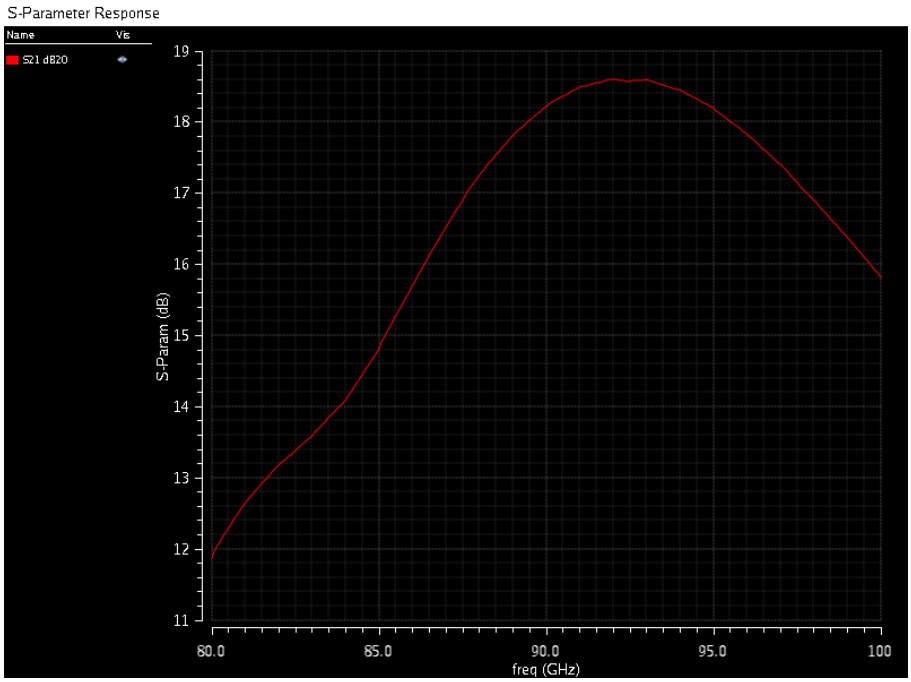


Fig. 3.10. Simulated gain of the PALNA circuit in the receive mode.

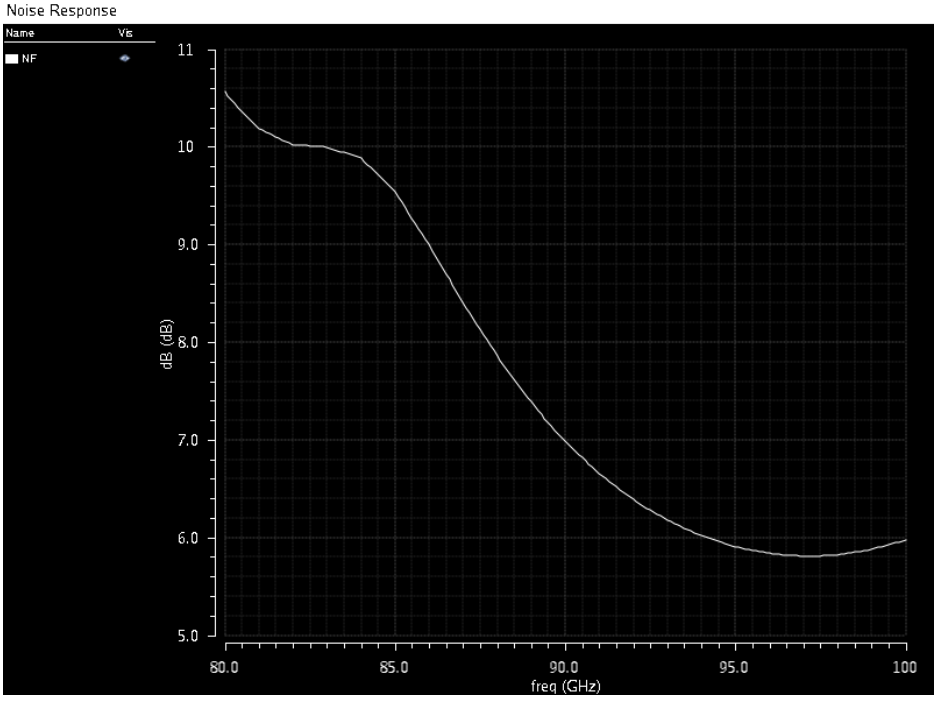


Fig. 3.11. Simulated noise figure of the PALNA circuit in the receive mode.

Table 3.2 summarizes the performance of the PALNA circuit in comparison with performances of the standalone PA and LNA circuits. In the transmit mode, the simulated

Table 3.2.
Summary of the Simulated PALNA Performance and Comparison With Standalone PA and LNA.

Metric	PA	LNA	PALNA	PALNA Mode
Tx Gain	12.5	N.A.	10.68	Transmit
Rx Gain	N.A.	20.6	18.4	Receive
Noise Figure	N.A.	4.0	6.02	Receive

transmit-to-receive isolation was approximately 50.6 dB, which exceeds the isolation that is achievable with integrated T/R switches at 94 GHz [1].

Fig. 3.12 shows a dimensioned image of PALNA chip layout. Although not shown in the image, metal fill exclusions were applied in areas where transmission lines are located.

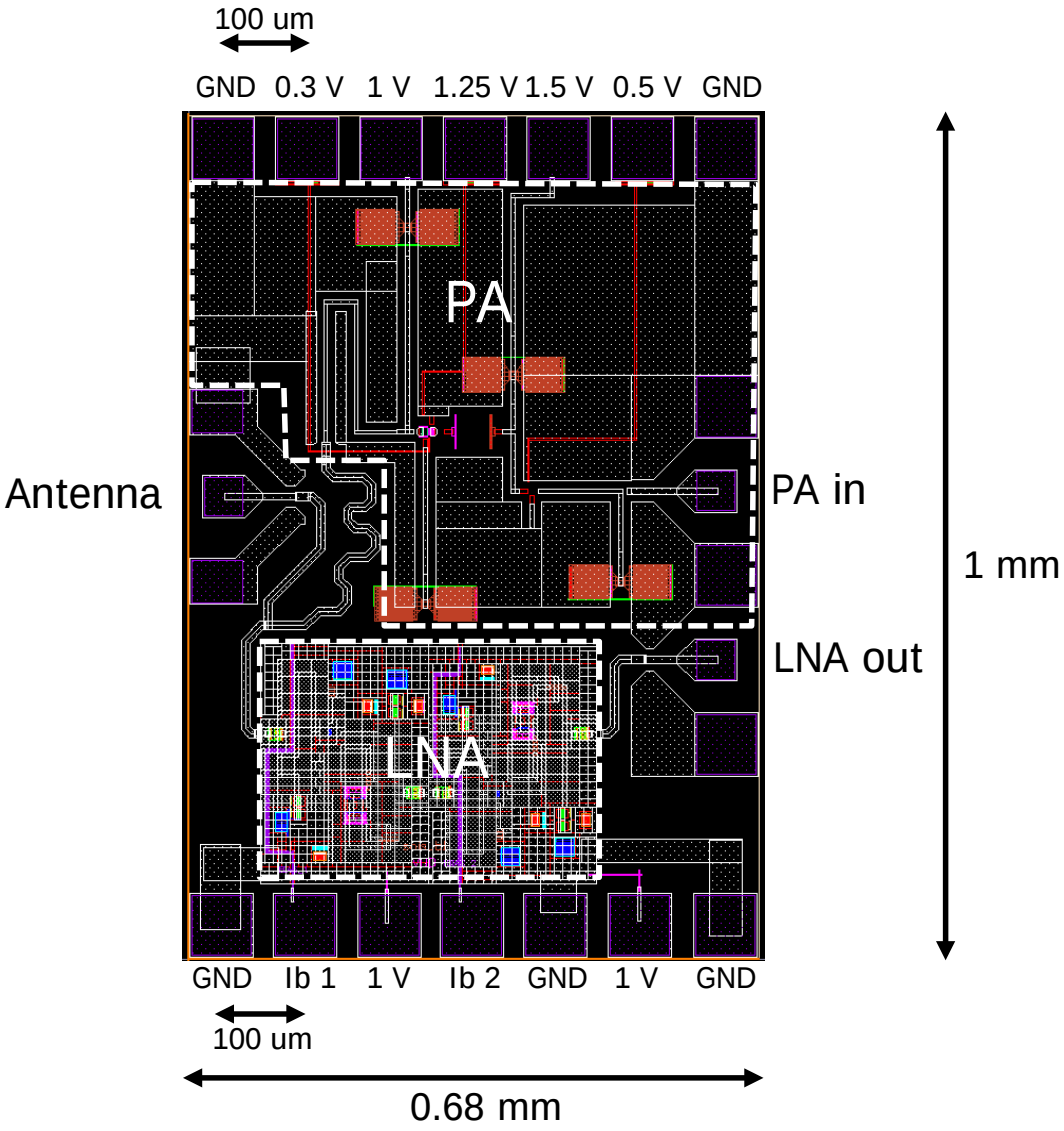


Fig. 3.12. Layout of the PALNA circuit.

3.5 Experimental Results

The designed PALNA circuit was taped-out through TAPO in February 2015 and the chips were fabricated in the 32SOI technology, as part of TAPO run 32SOI15A. Fig. 3.13 shows the chip photograph of the fabricated PALNA circuit. Probe station measurements of the PALNA chip were made at Virginia Tech in Blacksburg, VA on Oct. 14-15, 2015 and at the Army Research Laboratory in Adelphi, MD on December 1-14, 2015. Fig. 3.14 – Fig.

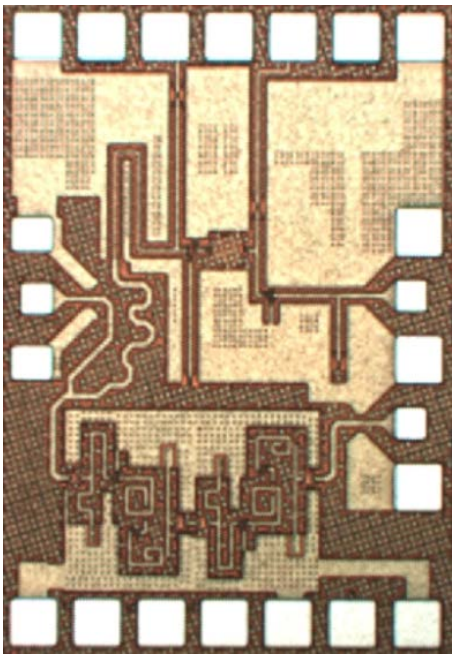


Fig. 3.13. Chip photograph of the PALNA circuit.

3.18 show the measured chip results in the receive mode of operation and Fig 3.21 – Fig. 3.24 show the measured results in the transmit mode of operation. Fig. 3.19 and Fig 3.20 show the schematics of the LNA and the PA, respectively.

Fig. 3.14 shows K-factor stability measurements of 24 data sets collected at various bias conditions of the LNA with the PA turned off. For stable operation, $K_f > 1$ is required, which, as shown in Fig. 3.14, is achieved for 7 of the 24 bias conditions. The s-parameter measurements are considered valid only if the LNA is stable. A preliminary s_{21} parameter measurement indicated that there was a center frequency downshift for the LNA, from the originally intended design frequency of 94 GHz to 87.5 GHz. Therefore, all the receive measurements are noted at 87.5 GHz, rather than at 94 GHz. Fig. 3.15 shows PALNA receive small signal s_{21} parameter measurements of the 24 data sets at various bias conditions of the LNA with the PA turned off. Fig. 3.16 – Fig. 3.18 show the PALNA receive small signal s_{11}, s_{22}, and s_{12} parameter measurements, respectively, of the 7 stable data sets at various bias conditions of the LNA with the PA turned off.

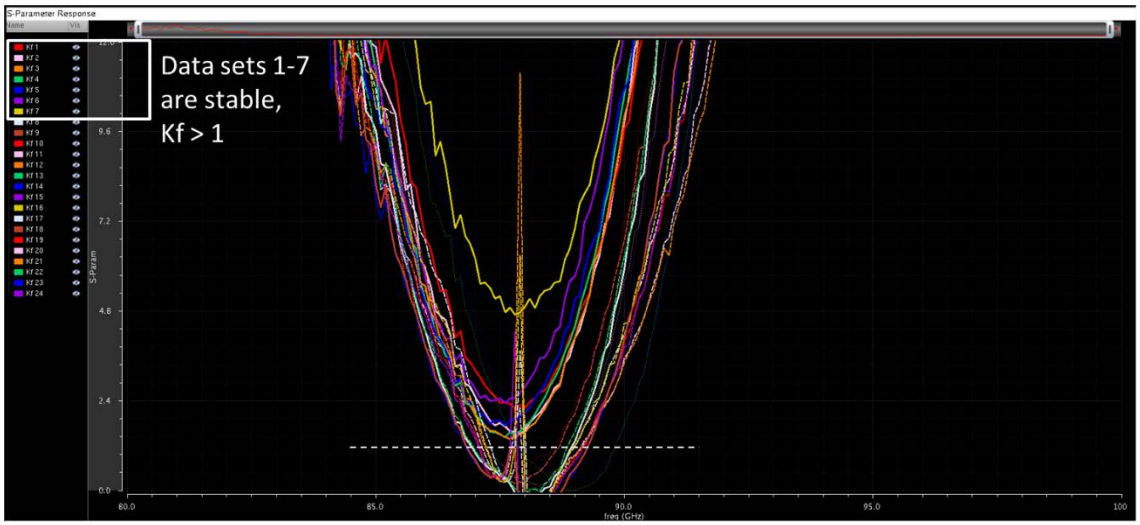


Fig. 3.14. PALNA receive small signal K-factor stability measurements of 24 data sets at various bias conditions of the LNA. The PA is turned off.

In addition to the downshift in frequency, it is noted that the measured small signal gain is more than 10 dB smaller than predicted in simulation. An independent look into a similar result for the standalone LNA found that a substantial part of this degradation can be attributed to the limitations of the available 32SOI device models (see section 7.3). In particular, single stage LNA measurement produced ~5 dB of gain, versus the ~10 dB predicted in simulation. The LNA used in this PALNA design is a two-stage LNA, and it would be expected to have ~10 dB of gain as a standalone two-stage LNA circuit, versus the simulated ~20 dB. Therefore, this unexpected shortcoming of the available LNA thus accounts for ~10 dB of the measured PALNA loss. With ~2 dB of assumed gain loss due to PALNA matching network at LNA input, 8 dB or less of small signal gain might be expected, which is consistent with what was measured. And, for some of the bias conditions, less than 8 dB of gain was measured. One contributor to the PALNA matching network loss, as will be discussed in more detail below, is the presence of metal fill that was inserted into the transmission line structures at the chip fabrication facility. The presence of metal fill was unexpected, since the fill was specifically excluded in the chip layout.

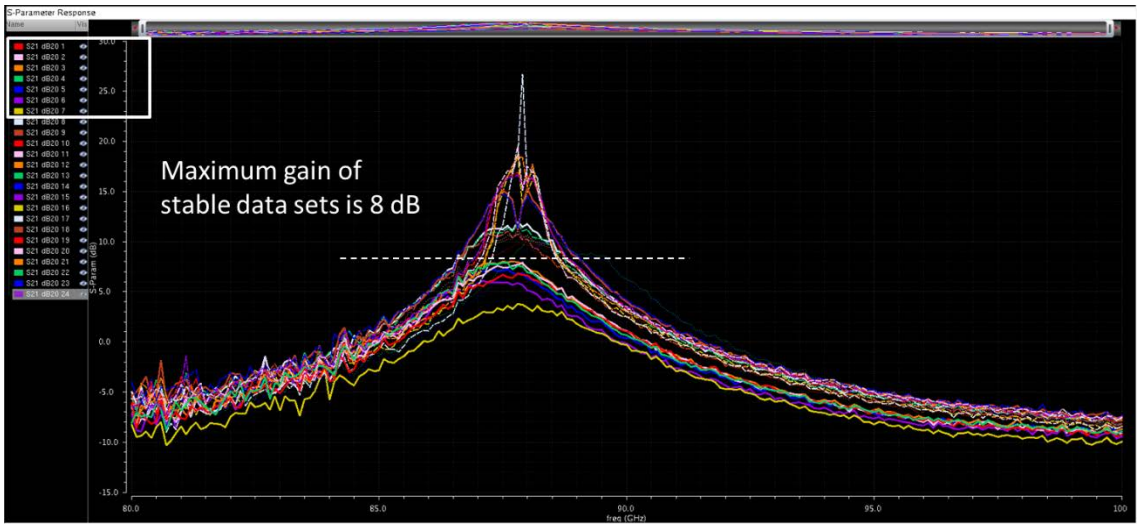


Fig. 3.15. PALNA receive small signal s_{21} measurements of 24 data sets at various bias conditions of the LNA. The PA is turned off.

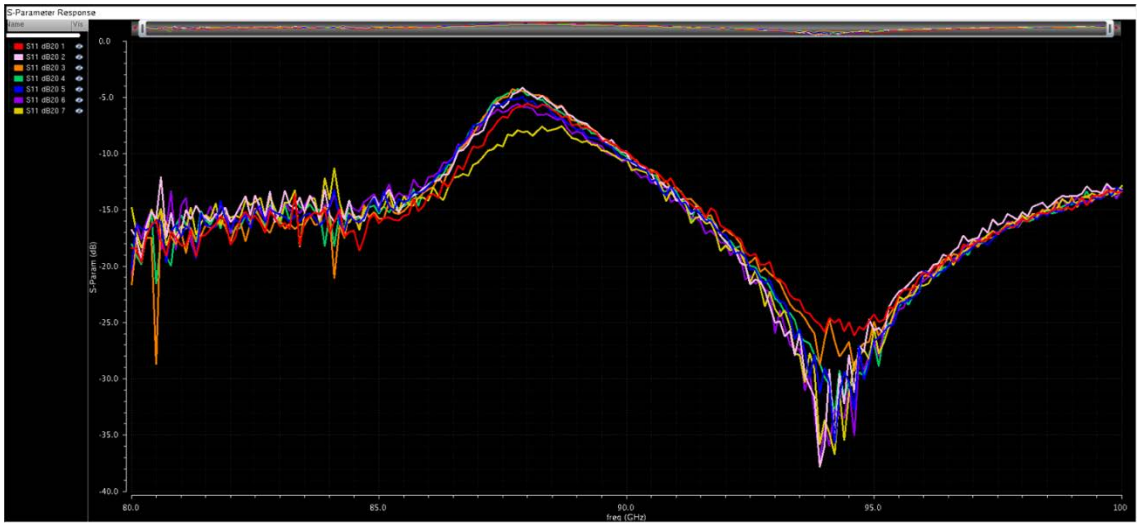


Fig. 3.16. PALNA receive small signal s_{11} measurements of the 7 stable data sets at various bias conditions of the LNA. The PA is turned off.

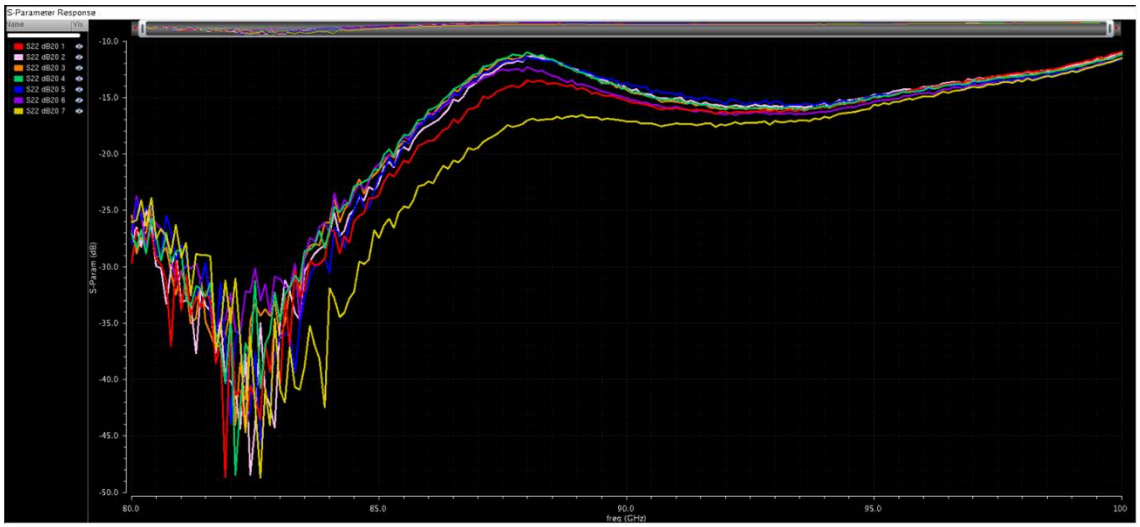


Fig. 3.17. PALNA receive small signal s_{22} measurements of the 7 stable data sets at various bias conditions of the LNA. The PA is turned off.

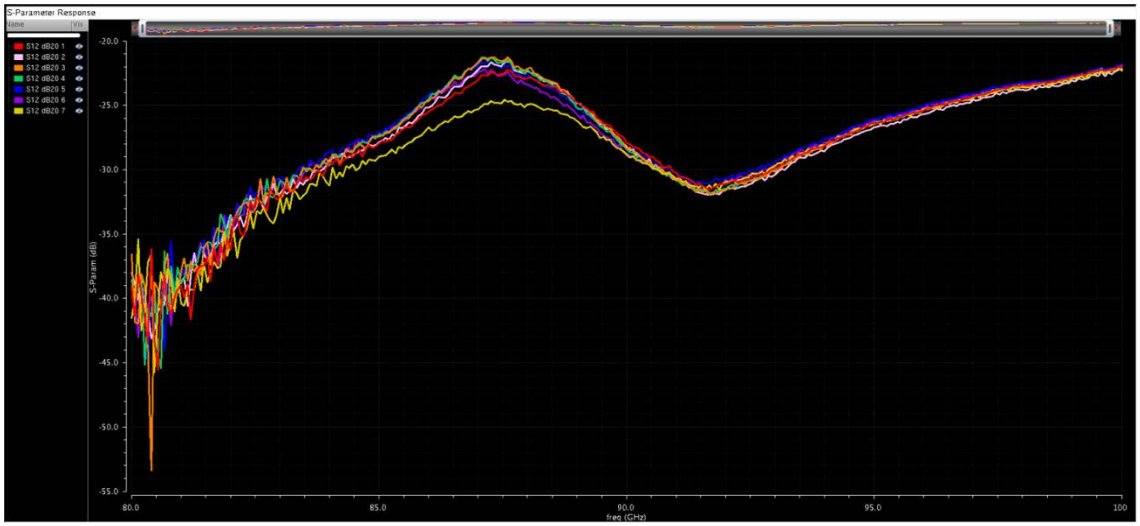


Fig. 3.18. PALNA receive small signal s_{12} measurements of the 7 stable data sets at various bias conditions of the LNA. The PA is turned off.

Table 3.3 below summarizes the bias conditions for the two-stage LNA circuit used in the PALNA, corresponding to the seven stable data sets discussed above. For reference, Fig. 3.19 shows the schematic of the LNA single stage. The PALNA presented in this chapter uses two such cascaded stages, provided as a courtesy by Dr. Mustafa Sayginer of UCSD.

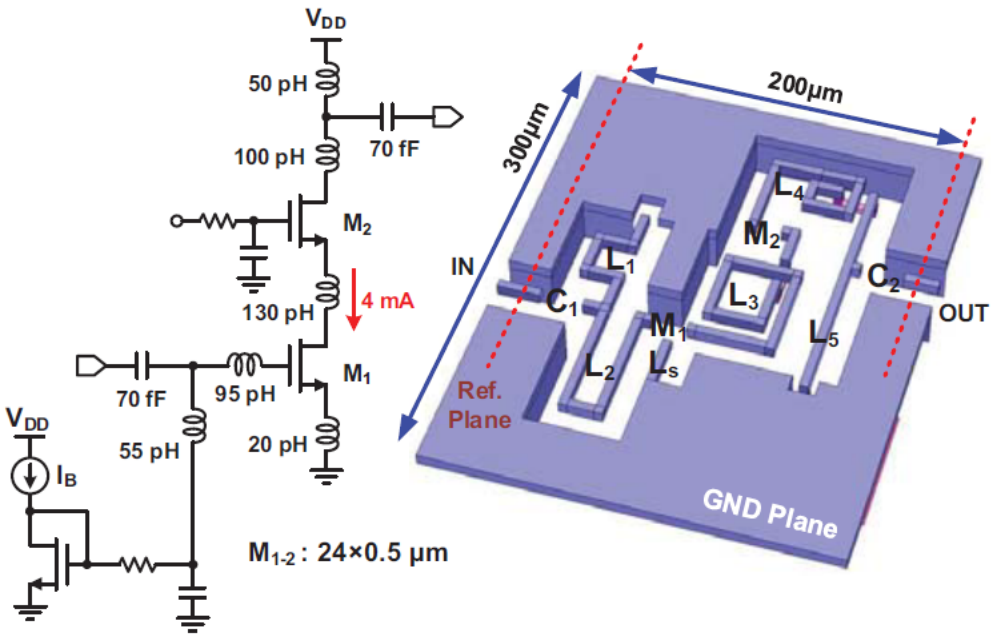


Fig. 3.19. The schematic of the cascoded LNA single stage with EM interconnect model [35]. The PALNA uses two such cascaded stages, provided as a courtesy by Dr. Mustafa Sayginer of UCSD.

Table 3.3.
Summary of the Bias Conditions for the Stable, Receive Mode, Small-signal PALNA Measurements Described Above.

Data Set #	Ib1, Ib2 Series R [Ohm]	Ib1 [V]	Ib1 [mA]	V1 [V]	V1 [mA]	Ib2 [V]	Ib2 [mA]	V2 [V]	V2 [mA]
1	150	1	2	1	9	1	10	1	1
2	150	1.1	3	1.1	11	1.1	10	1.1	1
3	150	1.2	3	1.2	13	1.2	11	1.2	2
4	150	1.3	3	1.3	15	1.3	11	1.3	1
5	150	1.4	3	1.4	17	1.4	11	1.4	2
6	150	1.5	3	1.5	19	1.5	11	1.5	2
7	150	0.9	2	0.9	8	0.9	10	0.9	<1

The PALNA noise figure was measured using 150 Ω series resistors at 1.1 V bias settings. The PALNA main LNA was biased at 1.0 V supply. The measured noise figure is 11.15 dB at 88 GHz, which is higher than the 6.02 dB predicted in simulation. Considering that the PALNA in the receive mode is a cascade of the PALNA MN and two LNA stages,

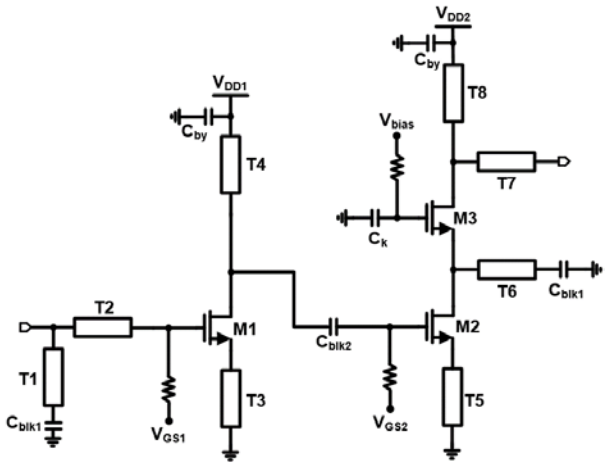


Fig. 3.20. Schematic of the PA used in the PALNA circuit. The schematic is courtesy of Mr. Hyunchul Kim of the Virginia Tech MICS laboratory.

where each LNA stage has independently measured NF of 5.53 dB and measured gain of ~5 dB, it can be calculated that the apparent loss of the PALNA MN is 4.7 dB. As will be discussed below, this is understandable and in line with expectations, given the presence of the metal fill in the fabricated chip.

For the transmit part of the PALNA circuit operation, Fig. 3.20 shows the schematic of the PA used in the PALNA circuit. There are a total of five bias voltages required to turn on the circuit. Fig. 3.20 will be referenced in the following text where necessary, to state the biasing conditions under which various measurements were made. Fig 3.21 – Fig. 3.24 show the measured PALNA results in the transmit mode of operation. The large signal performance of the PALNA is measured and included here, even though the large signal performance was not an explicit goal for this particular PALNA. Fig. 3.21 and Fig. 3.22 show the measured output power (P_{out}), power gain, and PAE of the PALNA in transmit mode of operation at 94 GHz and at the "simulation bias" and the "high gain bias", respectively. With reference to Fig. 3.20 schematic, the "simulation bias" is defined with the following settings of the PA biasing voltages: V_{GS1} = 0.3 V, V_{DD1} = 1.0 V, V_{GS2} = 0.5 V, V_{bias} = 1.25 V, V_{DD2} = 1.5 V. The "high gain bias" is defined with the following PA bias voltage settings: V_{GS1} = 0.4 V, V_{DD1} = 1.2 V, V_{GS2} = 0.6 V, V_{bias} = 1.35 V, V_{DD2} = 1.8 V. Fig. 3.23 shows the measured P_{out}, power gain, and PAE of the PALNA at 93 GHz and at high gain bias.

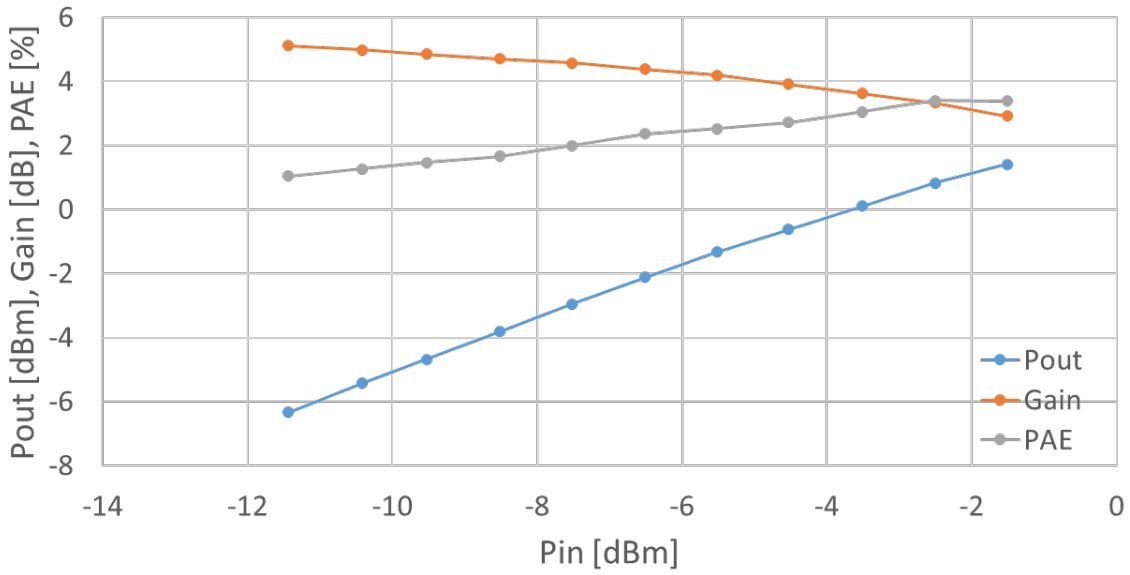


Fig. 3.21. Measured output power (P_{out}), power gain, and PAE of the PALNA in transmit mode of operation at 94 GHz. This measurement was done at “simulation bias”.

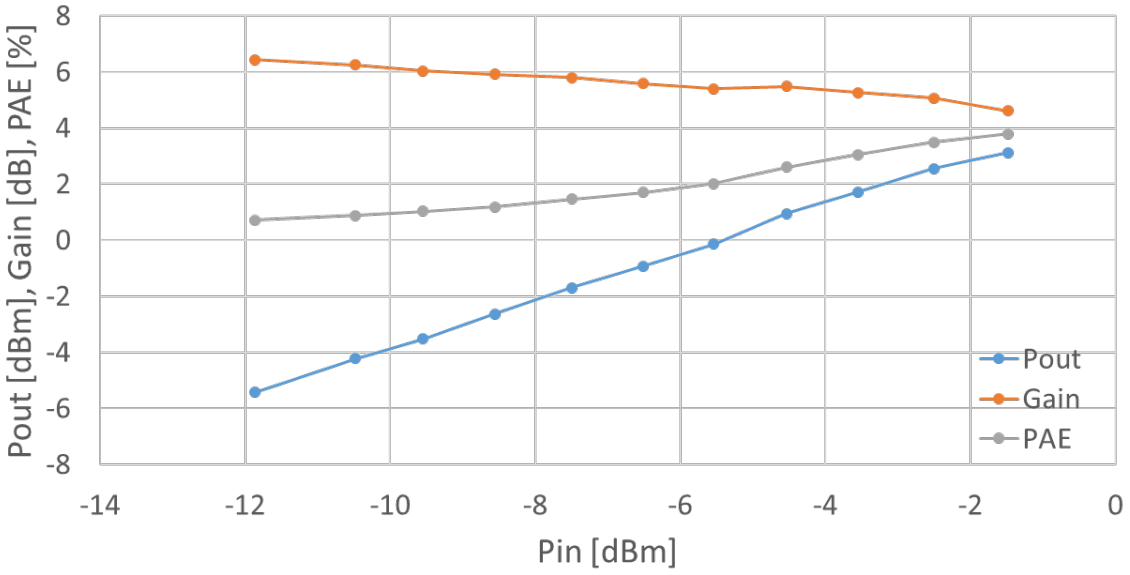


Fig. 3.22. Measured output power (P_{out}), power gain, and PAE of the PALNA in transmit mode of operation at 94 GHz. This measurement was done at “high gain bias”.

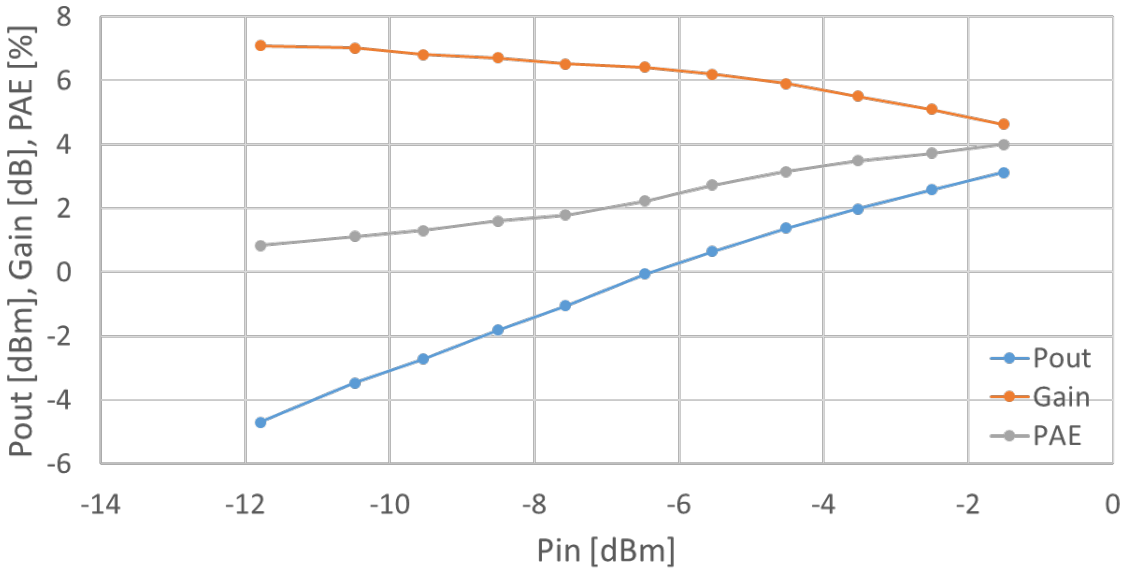
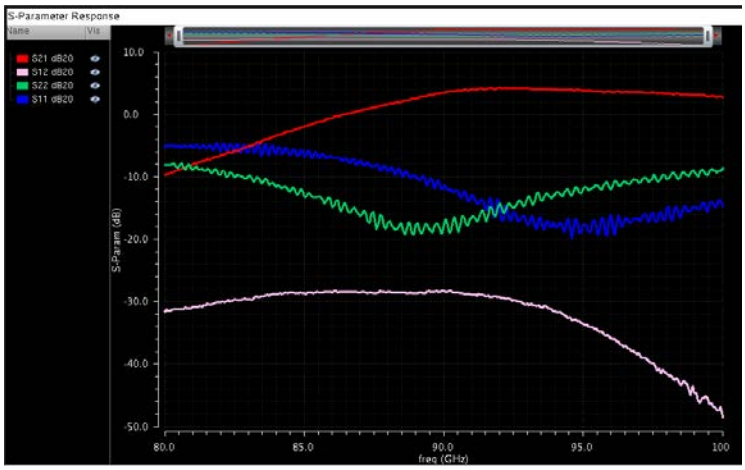


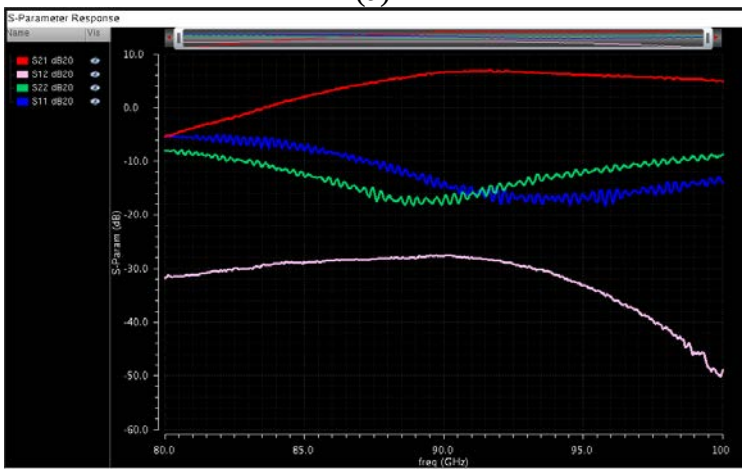
Fig. 3.23. Measured output power (P_{out}), power gain, and PAE of the PALNA in transmit mode of operation at 93 GHz. This measurement was done at “high gain bias”.

Fig. 3.24 shows the measured small signal parameters of the PALNA in the transmit mode of operation under three different PA bias conditions. The maximum gain is measured in Fig. 3.24(c), 7.5 dB at 90.5 GHz.

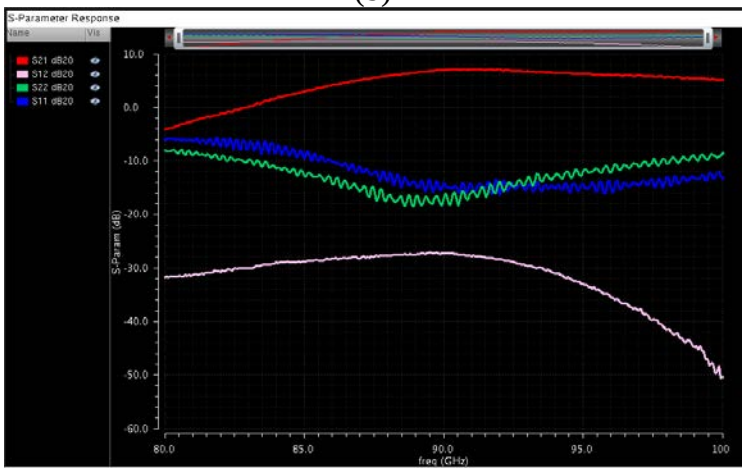
Table 3.4 below summarizes and compares the above presented simulated and measured PALNA performance results. As mentioned above, the measured performance was worse than simulated, however it is understandable and explainable.



(a)



(b)



(c)

Fig. 3.24. Measured small signal parameters of the PALNA in the transmit mode of operation under three different PA bias conditions: (a) V_{GS1} = 0.3 V, V_{DD1} = 1.0 V, V_{GS2} = 0.5 V, V_{bias} = 1.25 V, V_{DD2} = 1.5 V; (b) V_{GS1} = 0.4 V, V_{DD1} = 1.2 V, V_{GS2} = 0.6 V, V_{bias} = 1.35 V, V_{DD2} = 1.8 V; (c) V_{GS1} = 0.5 V, V_{DD1} = 1.2 V, V_{GS2} = 0.65 V, V_{bias} = 1.35 V, V_{DD2} = 1.8 V.

Table 3.4.
Summary Comparison of the Simulated (Expected) and Measured (Observed) PALNA Performance Results.

Metric	Simulated (Expected)	Measured (Observed)
Tx Frequency [GHz]	94	90.5
Small Signal Tx Gain [dB]	10.68	7.5
Rx Frequency [GHz]	94	88
Small Signal Rx Gain [dB]	18.4	8.0
Noise Figure [dB]	6.02	11.15

As mentioned above, closer inspection of the PALNA chip revealed extensive presence of metal fill artifacts on metal layers LB, MA, and MB, which were inserted around and into the circuit transmission line structures; this was unexpected since fill had been specifically excluded in those locations in the layout. Fig. 3.25 shows detailed images of the PALNA chip.

Subsequent EM simulations of the taped out PALNA circuit with the metal fill inserted have shown that the metal fill is a significant contributor to the above-mentioned performance degradations. Fig. 3.26 and Fig. 3.27 show the PALNA matching network transmit mode and receive mode transducer loss simulation results with no metal fill present and with metal fill present. It can be seen that the metal fill is responsible for a slight frequency downshift of approximately 2 GHz. Also, the metal fill increases the transducer loss of the PALNA matching network by approximately 0.5 dB and 1 dB, respectively.

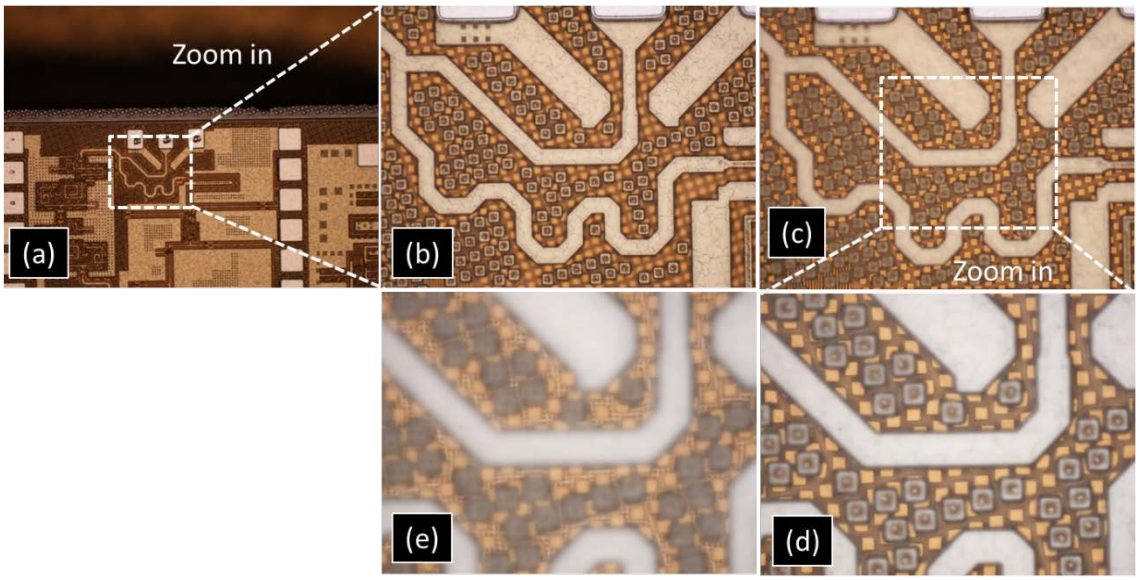


Fig. 3.25. Switchless PALNA T/R circuit chip photographs showing metal fill inserted during the 32SOI15A tapeout. (a) A circuit area is selected for zoom-in. (b) Top metal (LB) fill squares are seen to be very close to transmission lines. (c) MA layer, MB layer, or both metal fill squares are located under the transmission lines. An area is selected for further zoom-in. (d) Zoomed-in picture provides further confirmation that MA layer, MB layer, or both metal fill squares are located under the transmission lines. (e) Focus adjustment reveals layer E1 ground plane ("fine mesh"), which is below the MA and MB layer fill squares.

Given the simulation results shown in Fig. 3.26 and Fig. 3.27, the discussion of PALNA measurement results may now be completed. For the receive mode small signal gain, a minimum of ~3 dB PALNA MN loss should be expected, as seen in Fig. 3.27, and the measured gain of 8 dB or less is expected given the measured performance of the LNA used. For the receive mode noise figure, the above estimated apparent loss of the PALNA MN of 4.7 dB is ~1.7 dB larger than the minimum expected loss of ~3 dB seen in Fig. 3.27. This is already a reasonably good agreement between the measurement and simulation. And, if the metal fill is in reality responsible for a frequency downshift larger than the 2 GHz seen in simulation (6 GHz downshift is seen in measurements), the simulation result and the measured result would be in even a better agreement because the transducer loss shown with pink curve in Fig. 3.27 increases above 94 GHz (i.e., the simulated receive mode transducer loss at 94 GHz + 4 GHz is ~4.3 dB). The frequency downshifting effect of the metal fill, as applicable to spiral inductors, is discussed in [33]. For the transmit mode small signal gain, 10.68 dB – 7.5 dB = 3.18 dB is the difference between the

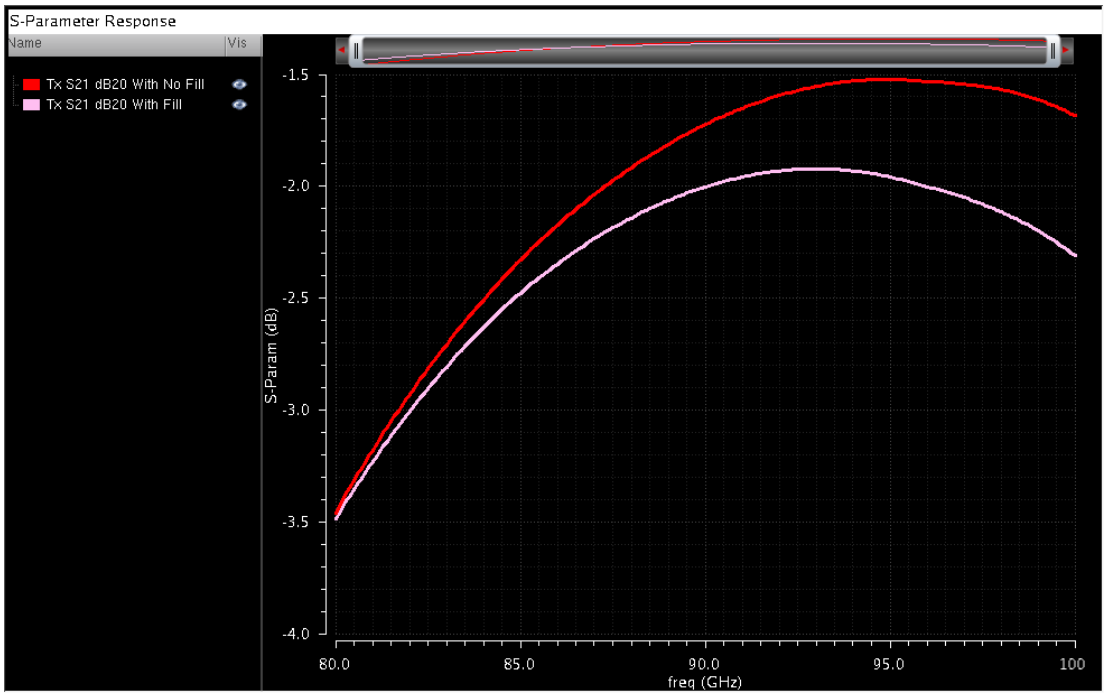


Fig. 3.26. PALNA transmit mode transducer loss simulation results with no metal fill and metal fill, respectively.

simulated and the measured values. With the additional minimum of ~0.5 dB attributable to metal fill, as can be seen in Fig. 3.26, the difference is ~2.7 dB, which represents a reasonably good agreement between the measurement and the simulation.

Additionally, the large signal performance of the PALNA was measured. The PALNA PAE reached its maximum of 4% at the PA "high gain bias" at 93 GHz, as shown in Fig. 3.23, for P_{out}=2.05 mW. The measured PAE of the PA only at this bias and frequency was 10.2% for P_{out}=4.03 mW. Using these two output powers, the PALNA MN loss in the transmit mode can be estimated at $10*\log_{10}(4.03\text{ mW} / 2.05\text{ mW}) = 2.9$ dB, which is ~ 1dB more loss than predicted in the simulation result in Fig. 3.26 with the pink curve. While this represents a reasonably good agreement between the measurement and the simulation, it is also consistent with the PALNA MN loss estimates made for the receive mode from NF measurements above, where the fill-based PALNA model also predicted a slightly smaller loss than was measured.

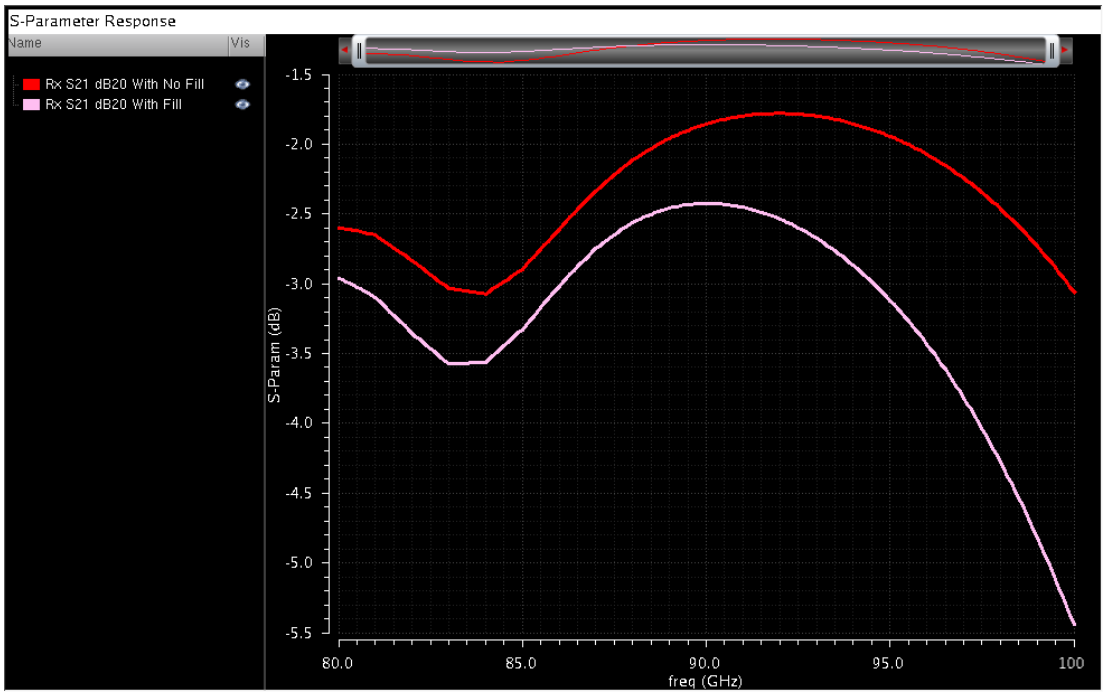


Fig. 3.27. PALNA receive mode transducer loss simulation results with no metal fill and metal fill, respectively.

3.6 Summary

This chapter presents a 94 GHz switchless PALNA design leveraging existing PA and LNA with 50 Ω matching networks. PALNA design methodology and implementation details were presented, followed by simulated and measured results. The simulated and measured results were compared in both modes of operation and the differences were discussed in detail using quantitative calculations as needed. Two main sources of the differences were identified: (a) The two-stage LNA used in the PALNA had a significantly smaller measured gain than was simulated; (b) Unexpected metal fill was inserted into PALNA transmission line structures at the fabrication facility. Given this knowledge, the PALNA measurements and simulations were reconciled through analysis and simulation. In particular, the measured receive small signal gain of 8 dB is in line with what is expected. The updated NF estimate using 3 dB of PALNA MN loss and the two-stage LNA with degraded gain is 9.45 dB, which is within 1.7 dB of the measured NF value of 11.15 dB, which represents a reasonably good agreement. The measured transmit mode small signal gain is within ~2.7

dB of the expected value, which also represents a reasonably good agreement between the measurement and the simulation. Additionally, PALNA and PA large signal measurements provided another avenue to estimate the PALNA MN loss in the transmit mode, which was found to be within ~1 dB of the simulated value.

In both modes of operation, a frequency downshift was observed, which was equal to 3.5 GHz and 6 GHz in transmit and receive mode, respectively. At least a part of this downshift can be attributed to the metal fill.

The next chapter will discuss a switchless PALNA design approach focused on matching specifically for NF and PAE, using both small signal and large signal simulations, versus just small signal simulations discussed in this chapter. In addition, the PA and LNA 50 Ω matching networks will be incorporated into the PALNA MN, for reduced loss. Finally, the PALNA design and optimization will be done manually in Cadence, by switching between transmit and receive modes, in an attempt to directly capture all the PALNA losses that affect the PALNA performance.

Chapter Four: **A 94 GHz Switchless PALNA with Simultaneous Optimum Impedance Matching for Maximum PAE and Minimum NF**

4.1 Technology Overview and Considerations

The GlobalFoundries SiGe 8XP process used in this design represents an update of a previously existing SiGe 8HP process, where a high performance 130 nm SiGe HBT demonstrating peak f_T/f_{MAX} of 250/330 GHz was added for mm-wave and high performance RF/analog applications. The 8HP process features are summarized in [36] and the 8XP process features are summarized in [37]-[39], including a list of available transistors, passive devices, and mm-wave passive devices.

The 8XP process is a 5-metal aluminum and copper process. In order to achieve good Q of the transmission lines and increase the achievable impedance values, the top three metal layers (AM-LY-MQ) are used to implement the transmission lines as microstrips with the

AM layer serving as the signal layer and the MQ layer serving as the ground layer. No metal or vias are used on layers between AM and MQ, and those intervening layers are filled with dielectric. Fig. 4.1 shows the structure of the transmission lines as used in 8XP for the purposes of this design. All inductors included in the PALNA circuit design presented in this chapter were implemented as microstrips.

The 8XP process supports the metal-insulator-metal (MIM) capacitors and this type of capacitor was used in the PALNA circuit design presented in this chapter. Fig. 4.2 shows a 3D model of a MIM capacitor built in the Sonnet EM simulation software. The QY metal layer in the 8XP process is a thin, specialized metal layer specifically used for MIM capacitor construction. In Fig. 4.2, the QY metal represents the top plate of the MIM parallel plate capacitor and the LY metal layer represents the bottom plate. Both LY and QY plates are connected to the top metal AM using vias.

PALNA circuit design presented in this chapter leverages an 8XP npn transistor with 3 μm emitter length whose layout and EM simulation terminal embedding network model are shown in Fig. 4.3.

4.2 PALNA Approach Methodology

Just like in the PALNA design presented above, in this design the LNA MN and the PA MN shown in Fig. 1.5 above were implemented using transmission lines. However, in this design, a preliminary attempt was made to integrate the output MN of the PA and the input MN of the LNA with the PA MN and the LNA MN, respectively. This was done in order to eliminate the 50 Ω MN inside of PA and LNA and improve overall PALNA performance by eliminating the loss attributable to each 50 Ω MN. Additionally, with reference to Fig. 3.3 and Fig. 3.4, Z_{PA_OPT} and Z_{LNA_OPT} impedances were explicitly defined to maximize the PALNA PAE in the transmit mode and to minimize the PALNA NF in the receive mode. This means than, in transmit mode (PA bias is on, LNA bias is off), the characteristics of the LNA MN and PA MN transmission lines are chosen to provide an optimum output

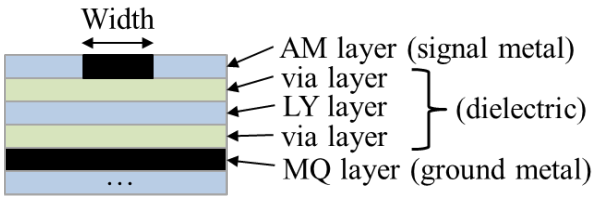


Fig. 4.1. The cross-section of the transmission lines used in this PALNA design. Microstrip substrate parameters are not provided due to proprietary restrictions.

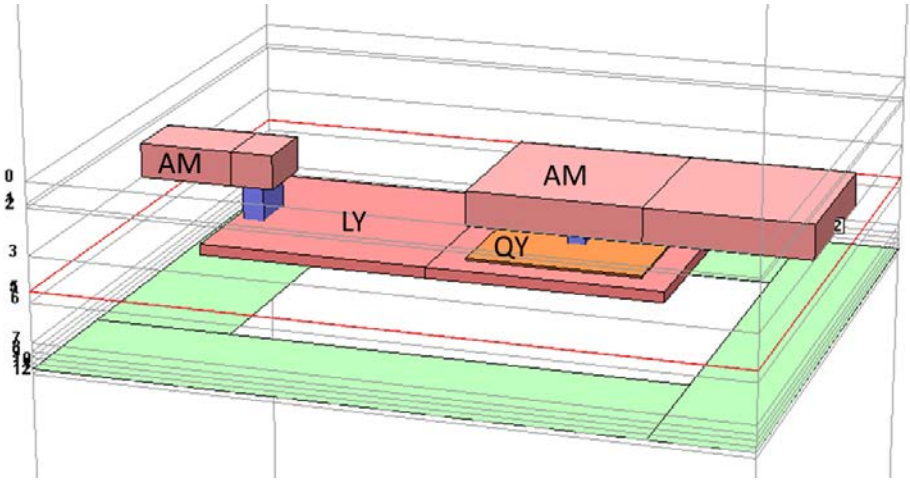
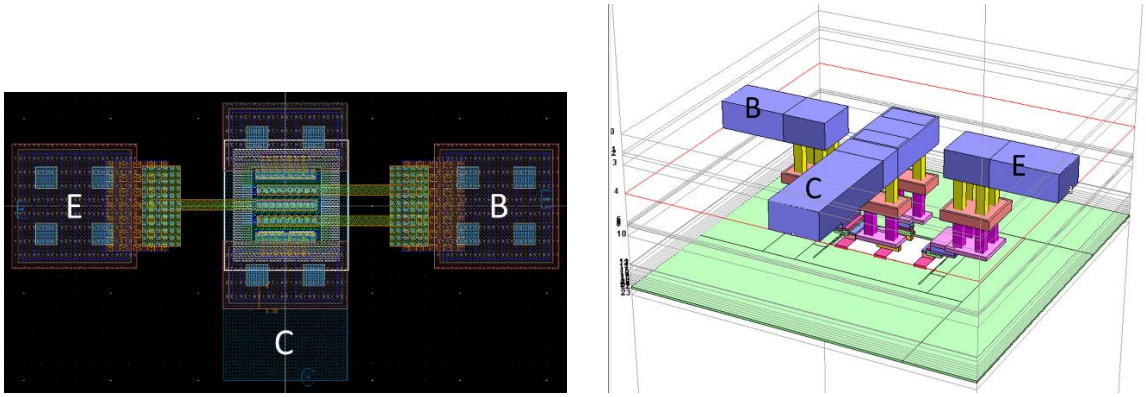


Fig. 4.2. MIM capacitor model constructed in Sonnet.



(a) (b)

Fig. 4.3. Layout of 8XP npn transistor with 3 μm emitter length (a) and an EM simulated transistor terminal embedding network model (b), which were included in the PALNA circuit simulations presented in this chapter.

impedance, Z_L, for the power amplifier to achieve the maximum PAE. Simultaneously, in receive mode (PA bias is off, LNA bias is on), the same transmission lines provide

optimum source impedance, Z_S, to the LNA required for minimum noise figure and acceptable small signal gain. For simulation purposes in Cadence, consideration of small signal circuit parameters was sufficient for the receive mode and consideration of large signal circuit behavior was, in addition, necessary in the transmit mode. Finally, it was recognized that MN TL losses were a key contributor to overall PALNA performance and an attempt was made to capture all the associated losses by doing manual circuit design and optimization directly in Cadence. Therefore, the MATLAB simulation step was not done for this design. Fig. 4.4 illustrates a step-by-step design flow of the 8XP PALNA circuit.

Whereas in the above design the PA and the LNA were leveraged from other designs, in this design they were designed from scratch, as described in the following sections. Then, with the PA output MN and LNA input MN excluded, the PA and the LNA were integrated with a preliminary PALNA matching network. At first, when the integration into the PALNA is done, the PAE and the NF performance of PALNA becomes severely degraded as compared with the performance of the standalone PA and LNA circuits. However, with adjustment of PA MN and LNA MN transmission line lengths, a satisfactory PALNA performance is obtained in both modes of PALNA circuit operation, as discussed below.

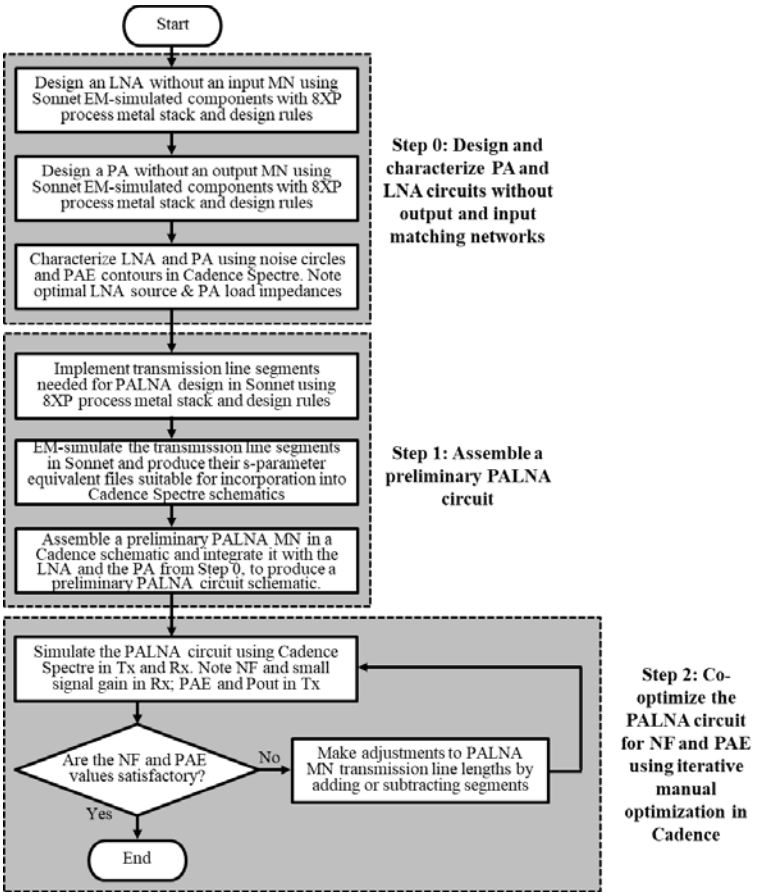


Fig. 4.4. An iterative, manual optimization design approach flowchart for design of PALNA with simultaneous optimum impedance matching for maximum PAE and minimum NF.

4.3 PA and LNA Core Designs in 8XP

4.3.1 PA Core Design

For the PA core design, an inductively-coupled common-emitter PA was used, as shown in Fig. 4.5. The PA is a class-A amplifier with quiescent voltage of approximately 2V, enabling voltage swing above and below the 2V supply voltage. The PA transistor input is impedance matched to the 50 Ω PA input port using the input matching network, which ensures maximum power transfer to the PA transistor input and a good PA gain. The 3 μm npn transistor shown in Fig. 4.3 is a baseline device, which was used on other designs, and

was leveraged in this design for convenience. The bias point was chosen through experimental simulations, for maximum PAE.

Fig. 4.6 shows the constant PAE contours of the 3 μm 8XP transistor PA at 94 GHz at the collector current DC bias of I_C = 0.3 mA. The area of the Smith chart inside of the innermost contour defines a set of optimum reflection coefficient values (i.e., load impedances) that the PA needs to see at its output in order to produce maximum PAE. When the PA is connected to a final, optimized PALNA MN, including the off-state LNA and a 50 Ω antenna, and the large signal load pull simulation is repeated at the antenna port, it is anticipated that the load pull contours will migrate such that the innermost contour will occupy the area around the center of the Smith chart, which is the location of the 50 Ω antenna impedance. Therefore, as shown in Fig. 4.6 with an arrow, this is the transmit mode impedance matching goal of the PALNA that is pursued in this chapter. And, it is desirable that the loss of the PALNA MN is minimal, such that the resulting contour values will be minimally degraded with respect to the values shown in Fig. 4.6.

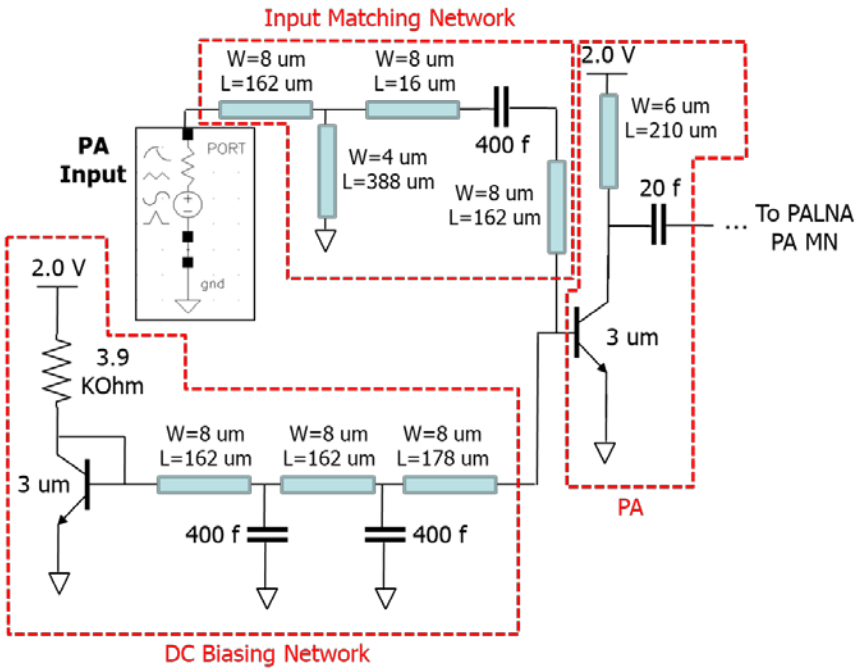


Fig. 4.5. Schematic of the 8XP inductively coupled common-emitter class-A PA circuit.

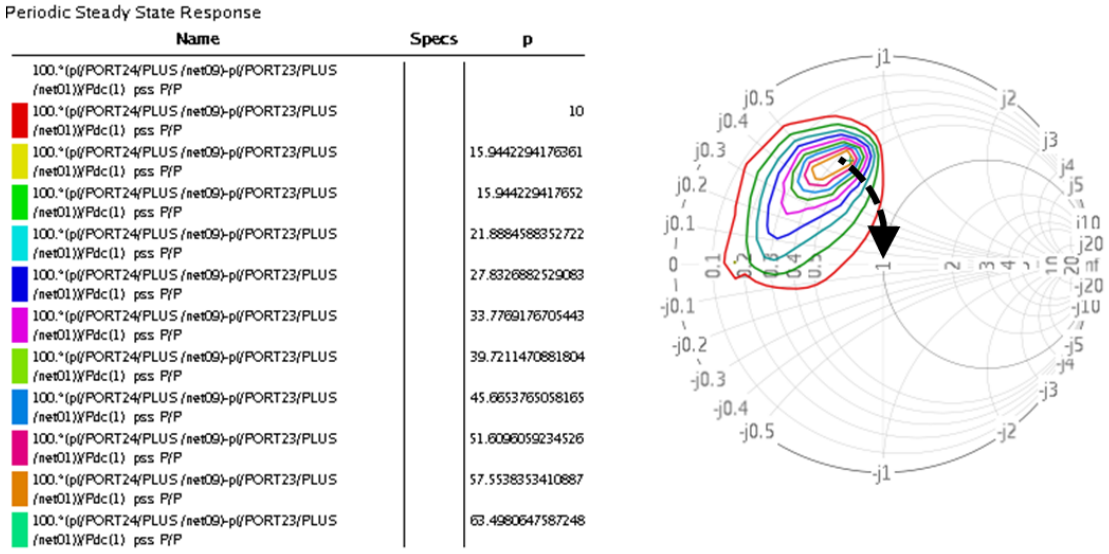


Fig. 4.6. Transmit mode PALNA design goal. Constant PAE contours define the desired reflection coefficient values for the 3 μm 8XP npn transistor PA at I_C=0.3 mA bias and at 94 GHz operating frequency. The PALNA MN design goal is for the contours generated from the PALNA antenna port to become relocated to the center of the Smith chart.

4.3.2 LNA Core Design

For the LNA core design, an inductively-degenerated cascode LNA was used, as shown in Fig. 4.7. The LNA output is well matched to the 50 Ω LNA output port, therefore no impedance matching is needed in addition to the short 50 Ω 64 μm stub connecting the LNA output and the output port. The LNA leverages the same 3 μm npn transistor shown in Fig. 4.3. The LNA bias point was chosen through experimental simulations, for minimum NF and maximum small signal gain.

Fig. 4.8 and Fig. 4.9 show the constant NF and constant gain circles of the 3 μm 8XP transistor LNA at 94 GHz and at the LNA collector DC bias current of I_C = 1.8 mA. In Fig. 4.8, the red + mark defines the reflection coefficient (i.e. the source impedance) that the LNA would like to see looking back from its input in order to achieve the minimum possible NF = 3 dB. Therefore, from the NF point of view, when the LNA is connected to a final PALNA MN, including the off-state PA and a 50 Ω antenna, and the small signal noise circle simulation is repeated at the antenna port, it is anticipated that the noise circles will migrate such that the location of the red + sign will occupy the area around the center of the Smith chart, which is the location of the 50 Ω antenna impedance. Therefore, as shown in Fig. 4.8 with an arrow, this is NF receive mode impedance matching goal of the PALNA that is pursued in this chapter. And, it is desirable that the loss of the PALNA MN is minimal, such that the resulting noise circle values will be minimally degraded with respect to the values shown in Fig. 4.8. Similarly, Fig. 4.9 shows the PALNA receive mode impedance matching goal as viewed from the perspective of the LNA gain. When the LNA is connected to a final PALNA MN, including the off-state PA and a 50 Ω antenna, and the small signal gain circle simulation is repeated at the antenna port, the goal is for the highest gain circle to be centered around the center of the Smith chart, for maximum gain, which is the location of the 50 Ω antenna impedance.

And, for the PALNA receive mode overall, the goal is for both NF and gain impedance matching goals to be satisfied simultaneously.

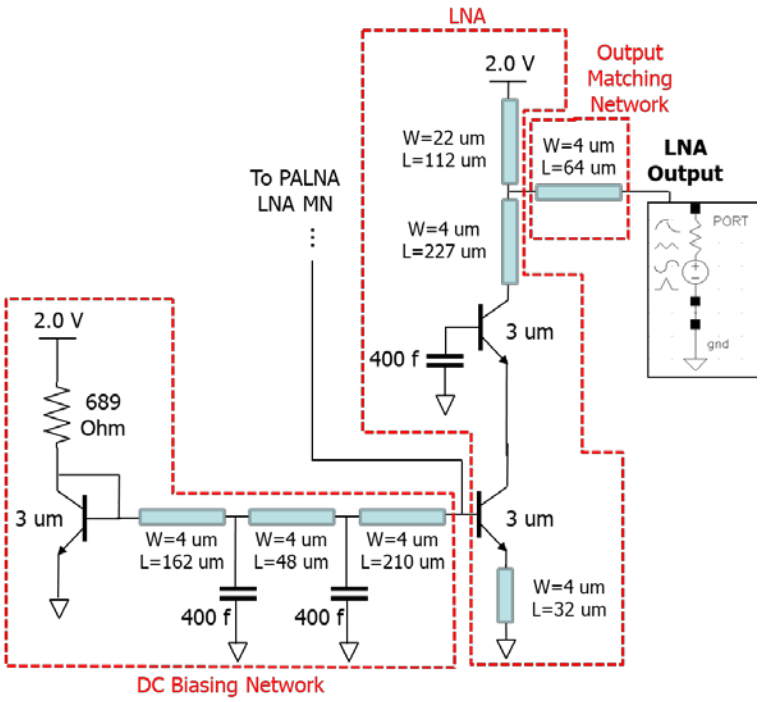


Fig. 4.7. Schematic of the 8XP LNA circuit.

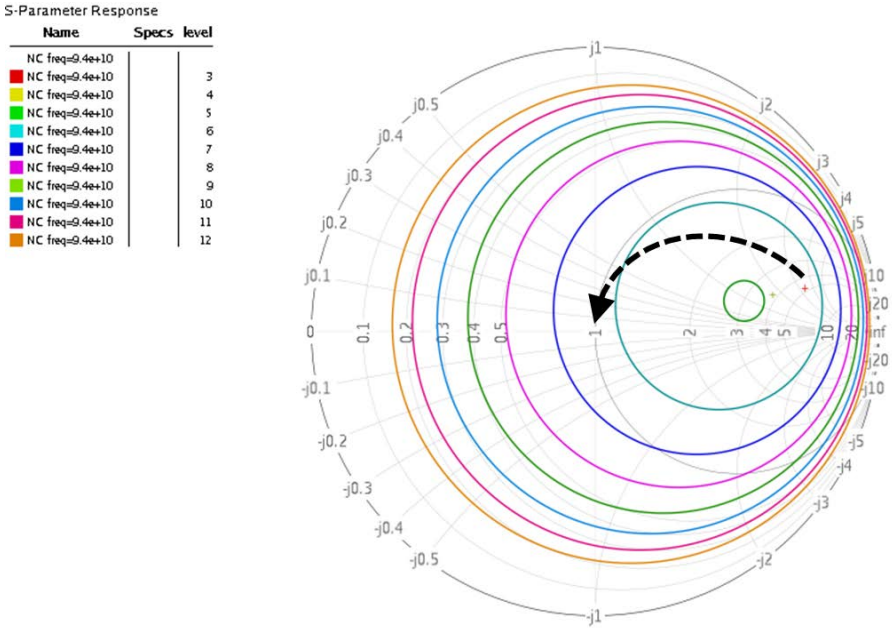


Fig. 4.8. Receive mode PALNA design goal as seen from the NF perspective. Constant noise figure circles define desired reflection coefficient values for the 3 μm 8XP npn transistor LNA at I_C =1.8 mA bias and at 94 GHz operating frequency. The PALNA MN design goal is for the noise circles generated from the PALNA antenna port to become relocated such that the location of the red + mark is at the center of the Smith chart, which is the location of the 50 Ω antenna impedance.

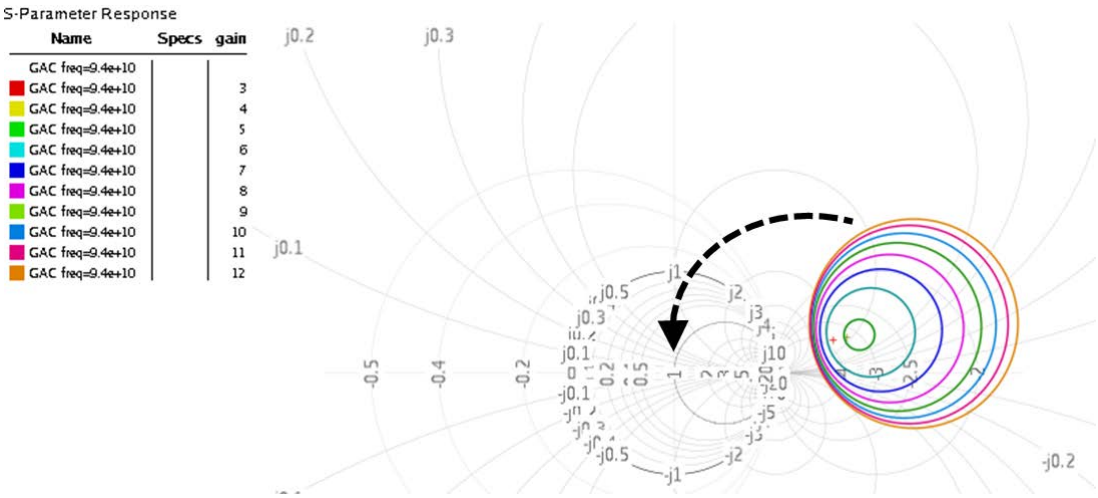


Fig. 4.9. Receive mode PALNA design goal as seen from the LNA gain perspective for the 3 μm 8XP npn transistor LNA at I_C =1.8 mA bias and at 94 GHz operating frequency. With the LNA is connected to a final PALNA MN, including the off-state PA and a 50 Ω antenna, the design goal is for the highest gain circle to be centered around the center of the Smith chart, for maximum LNA gain.

4.4 PALNA Design and Implementation in 8XP

After the core PA and LNA circuits are designed as described above, a two-step process is followed to complete the PALNA circuit design, as discussed in section 4.2 above.

First, a variety of transmission line segments are implemented in Sonnet using 8XP process metal stack and design rules. In this design, straight transmission line segments of 16 μm (short segment) and 162 μm (longer segment) were implemented and EM simulated with a variety of widths to represent the practically realizable range of impedances between 30 Ω and 94 Ω. The Sonnet EM simulations of the transmission line segments produced an s-parameter equivalent file for each segment, which is suitable for incorporation into Cadence Spectre schematic of the PALNA circuit. Then, the core PA and the LNA are connected into a preliminary PALNA circuit schematic using transmission lines of arbitrary lengths. The PAE and the NF performance of this preliminary PALNA will not be satisfactory when first simulated between the PALNA antenna port and PA input and

LNA output, in transmit and receive mode of operation, respectively. However, with adjustment of PA MN and LNA MN transmission line lengths, a satisfactory PALNA performance is eventually obtained in both modes of PALNA circuit operation.

Then, after the preliminary PALNA circuit schematic is assembled in a Cadence Spectre, the iterative, manual PALNA circuit optimization process takes place. First, biasing the PALNA circuit for the transmit mode of operation and using Spectre large signal simulation, load pull PAE contours of the PALNA circuit are generated between the PA input port and the 50 Ω antenna port. Location and the PAE levels of the contours are noted and the P_{in}-vs-P_{out} curves are generated, to verify the maximum PAE, P_{out}, and power gain. Second, biasing the PALNA circuit for the receive mode of operation and using Spectre small signal simulation, noise and gain circles of the PALNA circuit are generated between the 50 Ω antenna port and the LNA output. Location and the levels of the circles are noted and the NF and s_{21} gain curves are generated versus frequency, to verify the minimum NF and small signal gain.

If the PAE, P_{out}, power gain, NF and s_{21} gain are not satisfactory as compared to the known, published state-of-the-art values found in literature, the lengths of the PALNA MN transmission lines are adjusted by adding or subtracting transmission line segments. The above simulations are repeated and differences in performance are noted. Then, the transmission line lengths are adjusted again, in a direction needed to improve the overall PALNA performance, and the iterative process is repeated until satisfactory PALNA performance is reached simultaneously in both modes of circuit operation. Fig. 4.10 and Fig. 4.11 show the schematics of the final PALNA circuit design presented in this chapter.

In this particular design approach, the number of manual iterations between the transmit and the receive mode of operation involving transmission line length adjustments, which was needed to achieve the final PALNA design, was large. Also, the design process was very time consuming overall particularly because Cadence large signal simulation for a circuit of this complexity takes a relatively long time to complete.

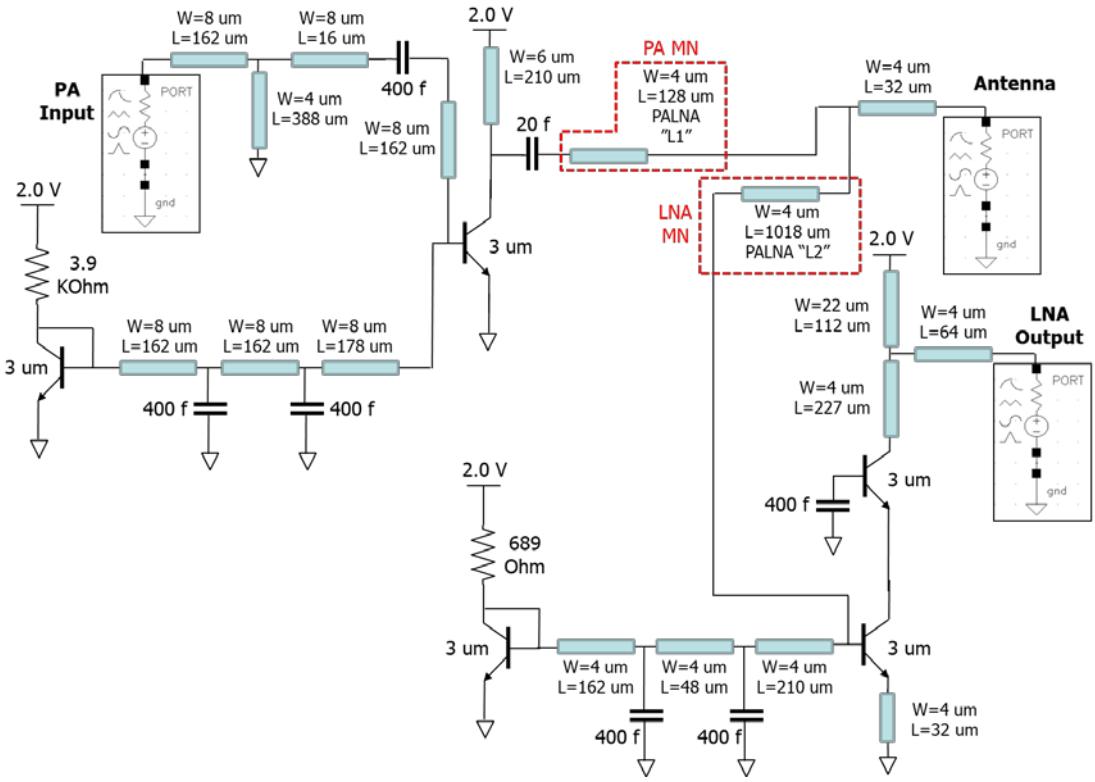


Fig. 4.10. The schematic of the final 8XP PALNA circuit design.

The widths of the transmission lines were varied too, however due to the multivariable complexity of the manual optimization approach, only the 4 μm 50 Ω transmission lines were ultimately shown feasible to arrive at the final PALNA design solution.

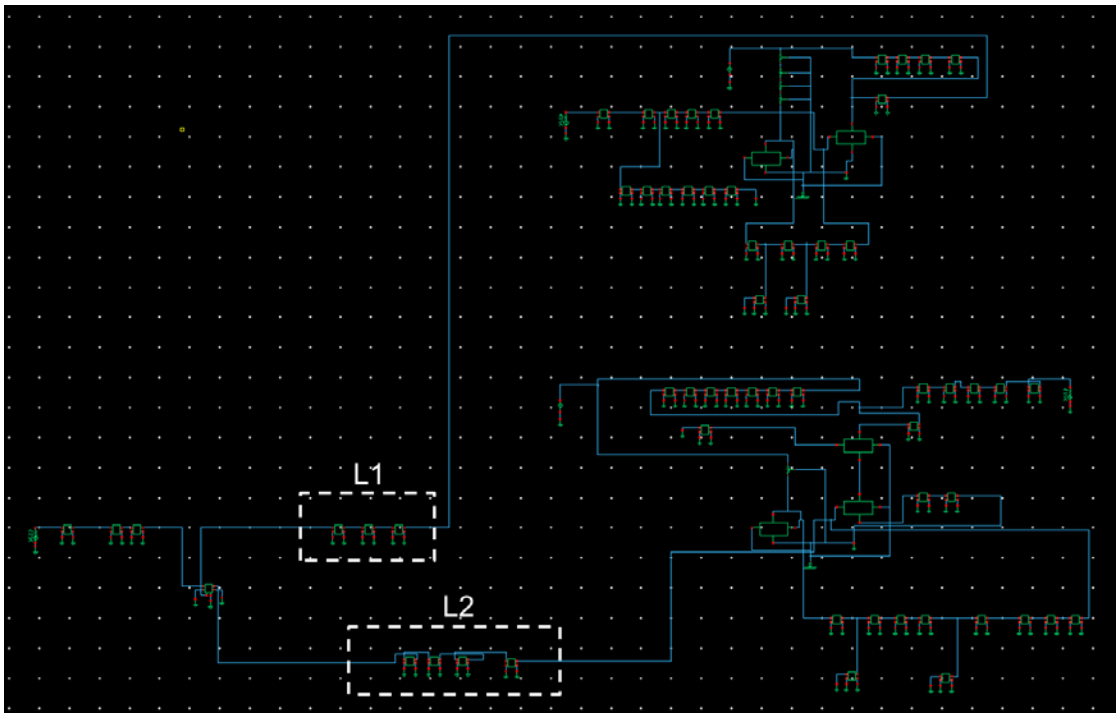


Fig. 4.11. The Cadence schematic of the final 8 XP PALNA circuit design.

4.5 Simulation Results

After the PALNA design procedure was completed, a full set of final simulations was run and the simulations results are shown in figures Fig. 4.12 – Fig. 4.18 below. Fig. 4.12 shows the simulated PALNA transmit mode performance at 94 GHz. With 8.5 % PAE achieved for this switchless PALNA, the PALNA meets the SOA performance at 94 GHz, as can be seen from Fig. 21 of [40], which shows SOA survey of PAE versus frequency for various published silicon PAs.

Fig. 4.13 – Fig. 4.15 show the simulated PALNA receive mode performance at 94 GHz. Fig. 4.13 shows the small signal s-parameters versus frequency. At 94 GHz, small signal gain s_{21} = 11.3 dB. Fig. 4.14 shows the NF performance versus frequency. At 94 GHz, NF = 9.5 dB, which is a SOA performance. Fig. 4.15 shows the stability factors, $K_f > 1$ and $B1_f > 0$, which means that the designed circuit is stable. Table 4.1 summarizes the 8XP

Table 4.1.
Summary of the 8XP PALNA Simulation Results, Including a Comparison with a Hypothetical Switch-based 8XP T/R Circuit and the PALNA Presented in Chapter Three.

Metric	8XP PALNA	8XP Switch-Based T/R Circuit (*)	32 SOI PALNA
Pout (Pin=0dBm) [dBm]	2.8	1.5	-
Power Gain [dB]	3(**)	2.2(**)	10.68
PAE [%] (at Pin=0dBm)	8.5	10.4	-
Rx Gain [dB]	11.3	13	18.4
Noise Figure [dB]	9.5	8.3	6.02

(*) A single SPDT switch at the antenna is assumed with 2.0 dB of insertion loss and 0 mW power consumption (passive switch). (**) Simulation result listed is for P_{in} <= 0dBm. (***) The bandwidth of all circuits is approximately 5% (i.e., ~5 GHz at the 94 GHz center frequency, with measurements that are reasonably constant over that bandwidth.

PALNA circuit simulation results, including a comparison with a hypothetical switch-based 8XP T/R circuit and the 32SOI PALNA circuit presented in Chapter 3.

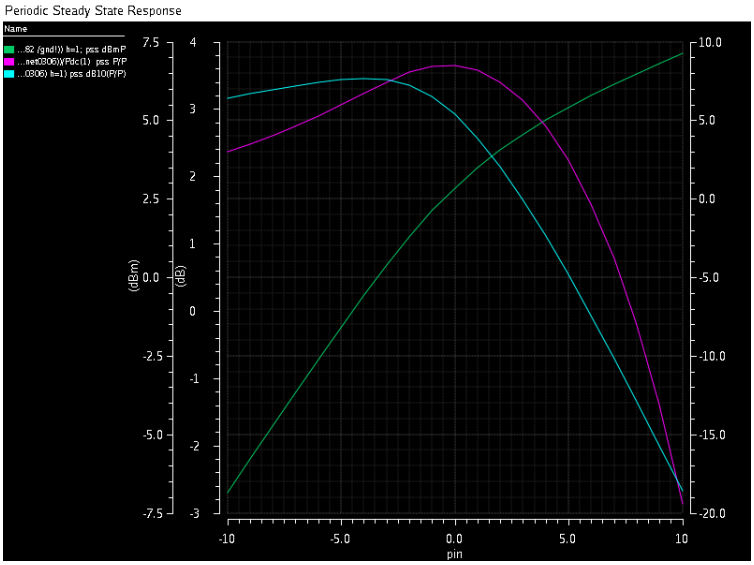


Fig. 4.12. Simulated PALNA transmit mode performance at 94 GHz showing P_{out} = 2.8 dBm at P_{in} = 0 dBm, power gain ~3 dB for P_{in} <= 0 dBm, and PAE = 8.5% at P_{in} = 0 dBm.

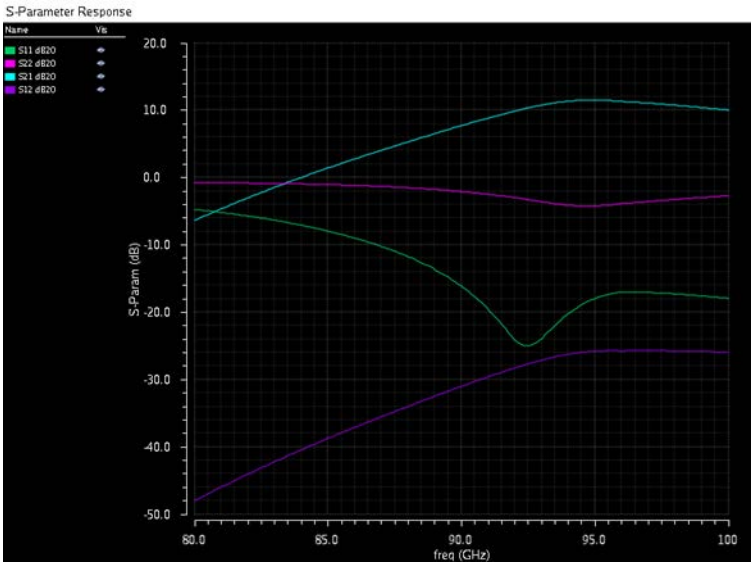


Fig. 4.13. Simulated PALNA receive mode performance showing small signal s-parameters versus frequency. At 94 GHz, small signal gain s_{21} = 11.3 dB.

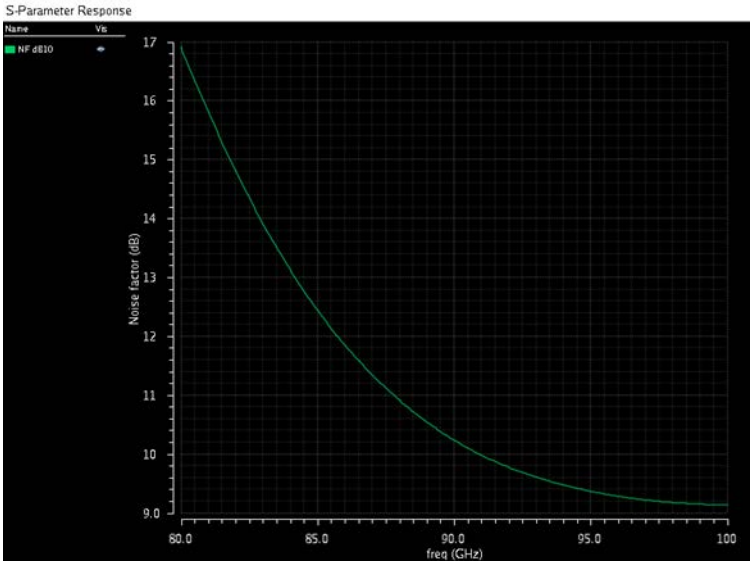


Fig. 4.14. Simulated PALNA receive mode performance showing noise figure versus frequency. At 94 GHz, NF = 9.5 dB, which is a SOA performance.

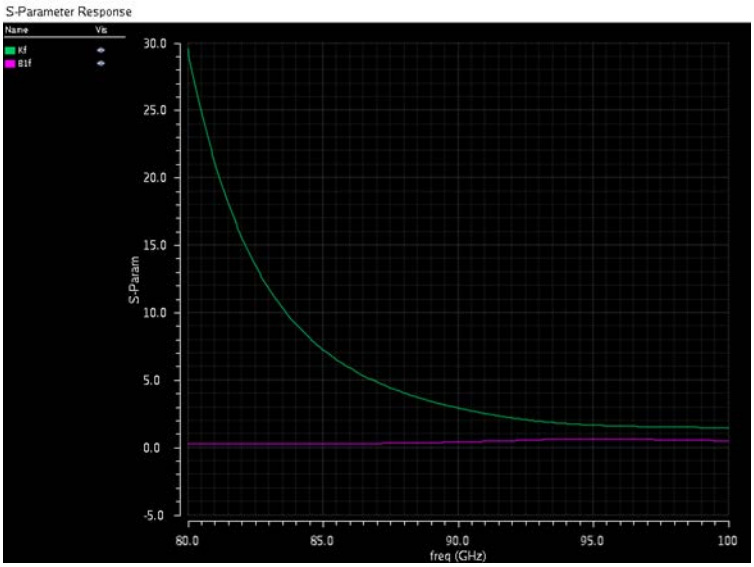


Fig. 4.15. Simulated PALNA receive mode performance showing stability factors, $K_f > 1$ and $B1_f > 0$, which means that the designed circuit is stable.

For further perspective on the 8XP PALNA simulated results Fig. 4.16 – Fig. 4.18 are included below. Fig. 4.16 shows the transmit mode load pull PAE contours of the final 8XP PALNA circuit. It can be seen that the innermost PAE contour is not centered around the center of the Smith chart as desired. This indicates that the PALNA performance in transmit, while acceptable and comparable with the SOA, is not optimal and that the

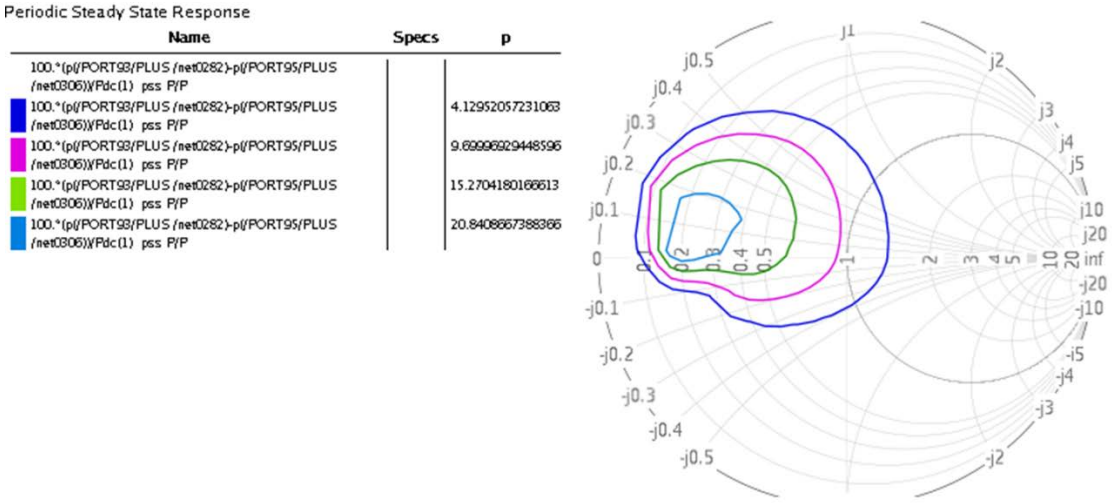


Fig. 4.16. Transmit mode load pull PAE contours of the final 8XP PALNA circuit. The innermost contour is not centered around the center of the Smith chart indicating that, while acceptable and comparable with the SOA, the PALNA impedance match for PAE is not optimal.

PALNA impedance match for PAE could be further improved. One lesson learned from this PALNA design approach and result is that a different design methodology was needed.

Fig. 4.17 shows the receive mode constant noise and gain circles of the final 8XP PALNA circuit on the Smith chart. It can be seen that the intersection region of the innermost gain and noise circles, which is the region shaded in blue color, is centered at the center of the Smith chart, indicating that the PALNA impedance match for NF and receive gain is very close to optimal. This means that both a good NF and good small signal gain are being achieved, as originally intended. Fig. 4.18 shows both the transmit mode and receive mode impedance matching results simultaneously achieved by the 8XP PALNA circuit. The blue shaded region centered at the center of the Smith chart, which contains the final matching results, represents the compromise region of interest between the PAE, NF, and small signal gain impedance matching requirements in both modes of operation. While the receive mode result is nearly optimal, it was achieved at the obvious expense of some reduced performance in the transmit mode of operation. This result clearly indicated that a better, more effective methodology for design of PALNA circuits was needed.

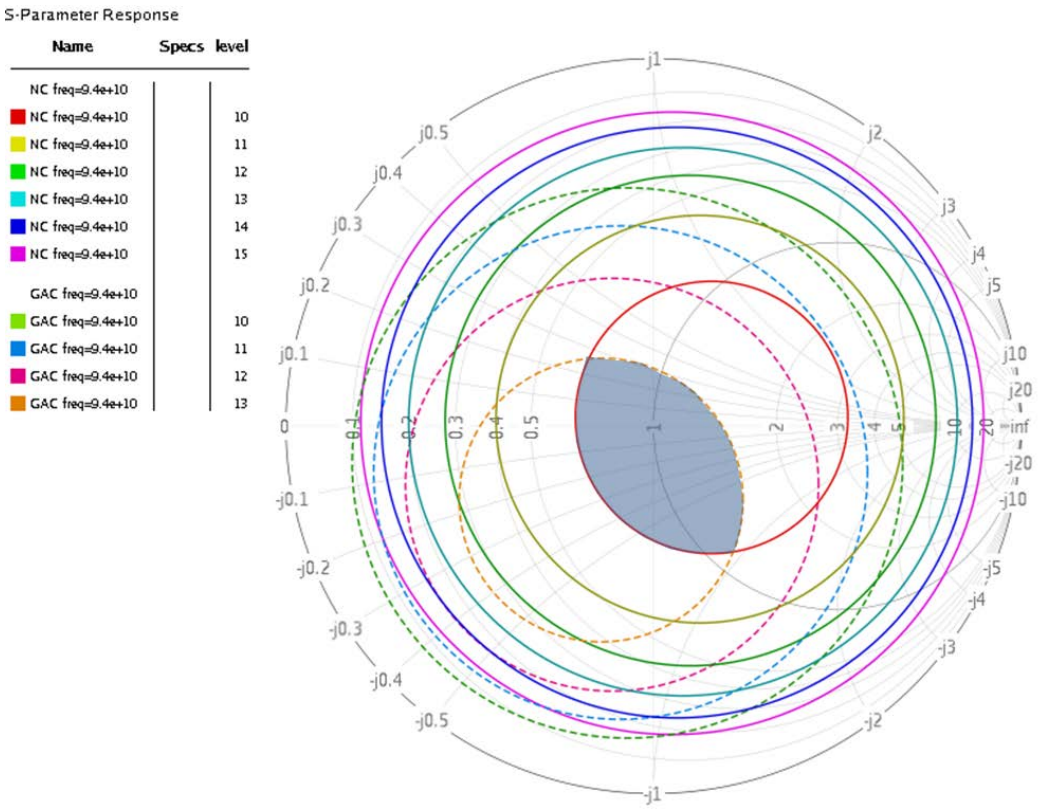


Fig. 4.17. Receive mode constant noise and gain circles of the final 8XP PALNA circuit. The intersection region of the innermost gain and noise circles (shaded region) is centered at the center of the Smith chart, indicating that the PALNA impedance match for NF and receive gain is very close to optimal.

Fig. 4.19 shows the layout of the final 8XP PALNA circuit and Fig. 4.20 shows how the layout was verified using EM simulations in Sonnet. All transmission lines included in the layout design were EM simulated using Sonnet for final design verification. Fig. 4.20 shows only a limited subset of transmission lines used in the design. The simulation results presented in this section are the results of the final, fully EM verified PALNA layout.

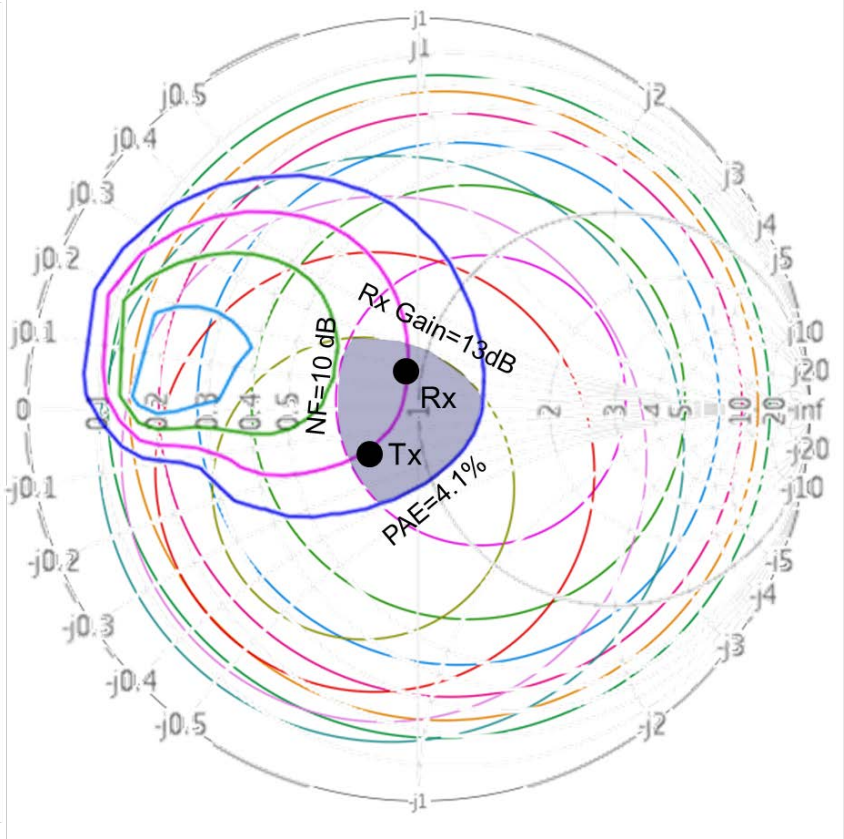


Fig. 4.18. Transmit mode and receive mode impedance matching results simultaneously achieved by the 8XP PALNA circuit. The blue shaded region centered at the center of the Smith chart, which contains the final matching results, represents the compromise region of interest between the PAE, NF, and small signal gain impedance matching requirements in both modes of operation. While the receive mode result is nearly optimal, it was achieved at the obvious expense of some reduced performance in the transmit mode of operation.

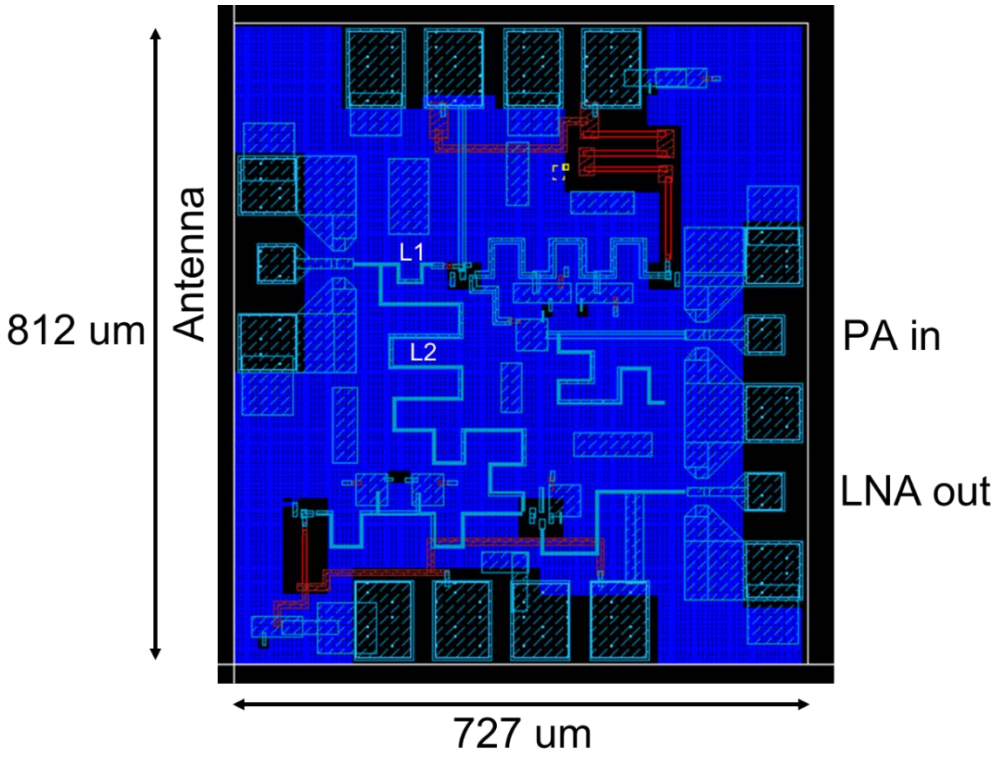


Fig. 4.19. Layout of the final 8XP PALNA circuit.

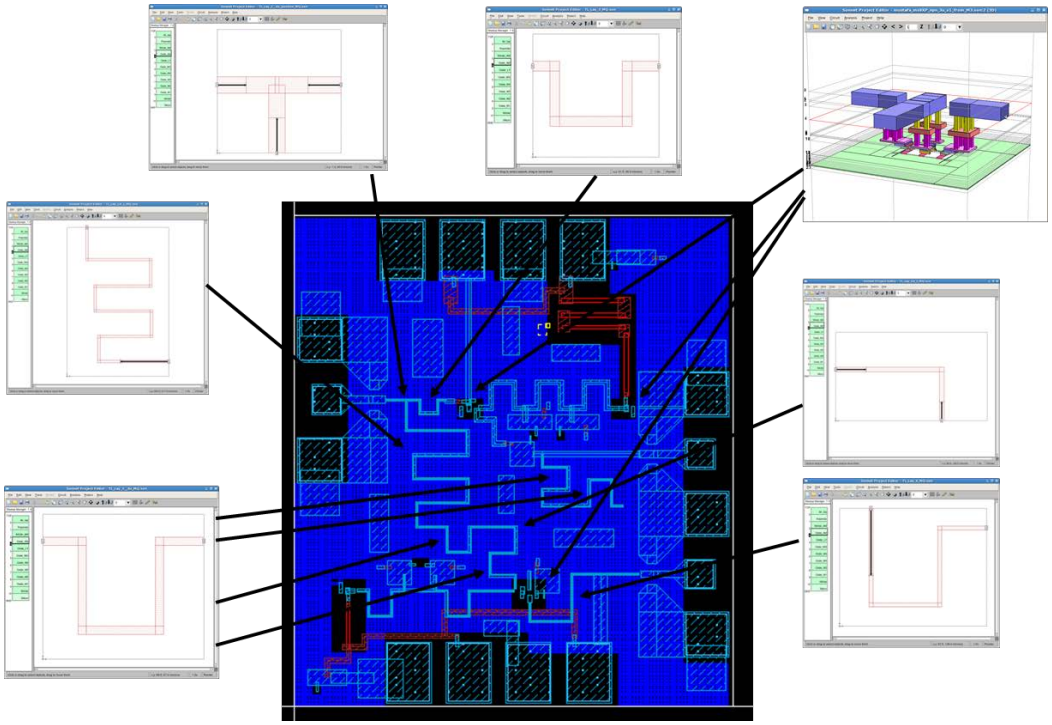


Fig. 4.20. Layout of the final 8XP PALNA circuit showing the layout EM verification using Sonnet. All transmission lines included in this design were EM simulated using Sonnet for final design verification. Only a limited set of examples shown here.

4.6 Experimental Results

Based on the simulated PALNA performance presented in the previous section, which met the published SOA performance in both the transmit and the receive mode of operation at 94 GHz, the PALNA circuit was taped out. Fig. 4.21 shows the chip photograph of the 8XP PALNA circuit.

The small signal s-parameters of the PALNA circuit were measured at ARL. In summary, the measured small signal transmit gain at 94 GHz is approaching 0 dB, which is ~ 5dB smaller than the simulated transmit gain of 4-5 dB. Since the measured small signal rain was lower than expected, the PAE measurement of the PALNA circuit was not attempted. The measured small signal gain in the receive mode of operation was found to be 5-6 dB, albeit at the slightly higher frequency of 97 GHz, which is ~ 5dB smaller than simulated value of 11.3 dB. Fig. 4.22 shows the receive mode s_{21} parameter measurements of the 8XP PALNA circuit, with the bias levels shown. The designed DC bias point of 2.0 V and 1.8 mA, was confirmed by measured DC current. The NF measurement of the chip in the receive mode was never attempted.

The fabricated chip essentially worked, albeit with a reduced performance. There are two possible reasons for this. First, the designer made an error during the final layout EM verification, where he accidentally used an incorrect transmission line segment in the schematic as part of the LNA MN transmission line "L2". This slightly shortened the line L2 with respect to its intended design value, likely resulting in the slight frequency upshift measured in the receive mode discussed above. Also, it was found in subsequent simulation that this L2 shortening has impact on receive performance but not on the transmit performance. It was also found that the issue could be fixed by using a higher LNA bias voltage. It can be noted from Fig. 4.22 that the measured gain did indeed increase as the bias voltage was increased beyond the design voltage of 2 V. On the other hand, ~ 5 dB of degradation was observed in both modes of operation, which points to the second possible reason – incorrect device models. The parasitic extraction tool could possibly not have

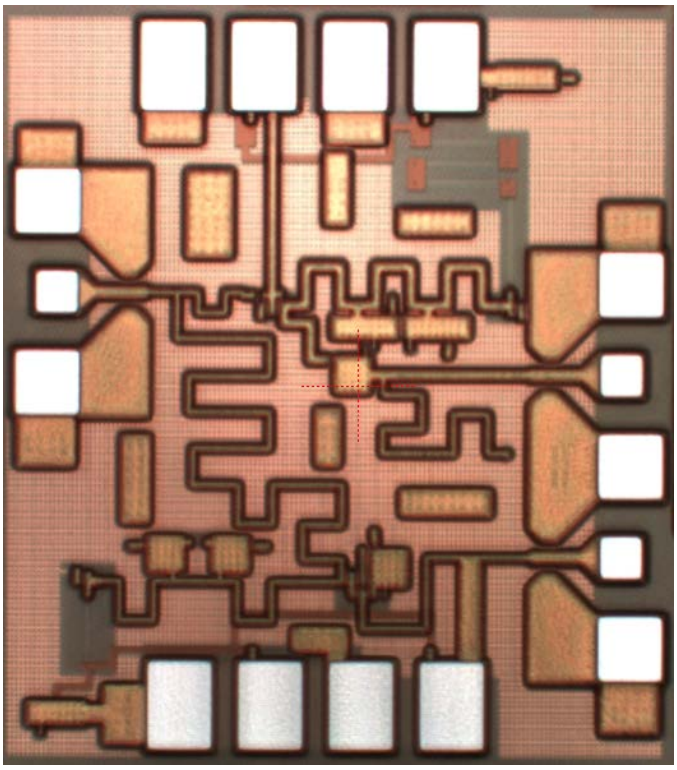


Fig. 4.21. Chip photograph of the 8XP PALNA circuit.

captured all the parasitics correctly, resulting in an impedance mismatch caused gain reduction. As in other designs presented in this dissertation, no measured transistor s-parameter data was used in this design.

Inspection of the fabricated chip using a high-resolution camera revealed that the 8XP transmission lines were fabricated as designed, with no undesirable metal fill present anywhere. Fig. 4.23 shows the fabricated chip images.

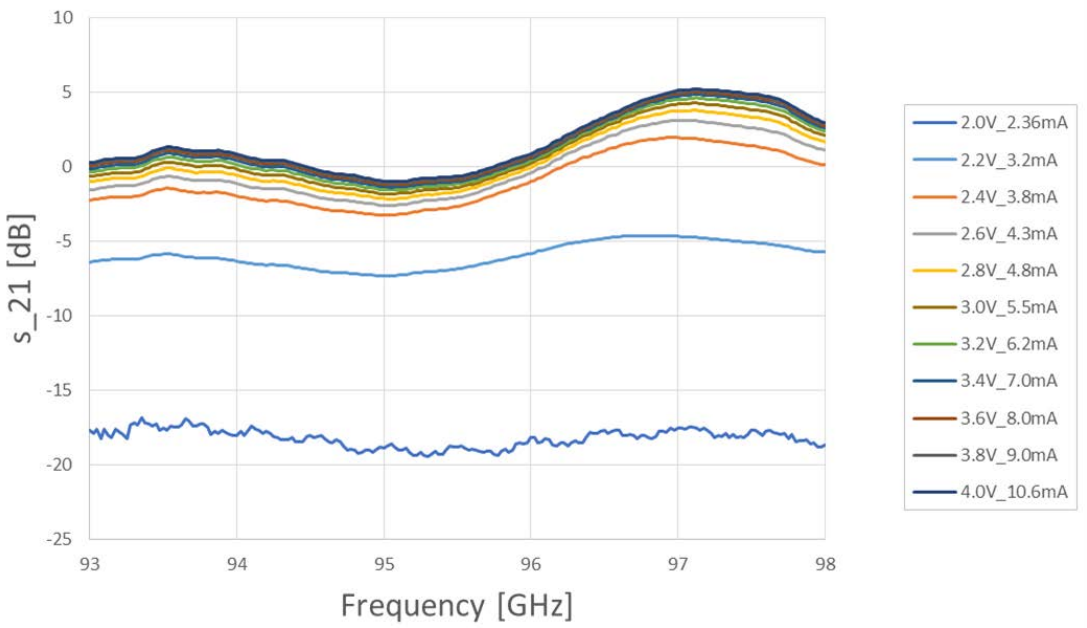


Fig. 4.22. Small signal receive mode s_{21} parameter measurements of the 8XP PALNA circuit.

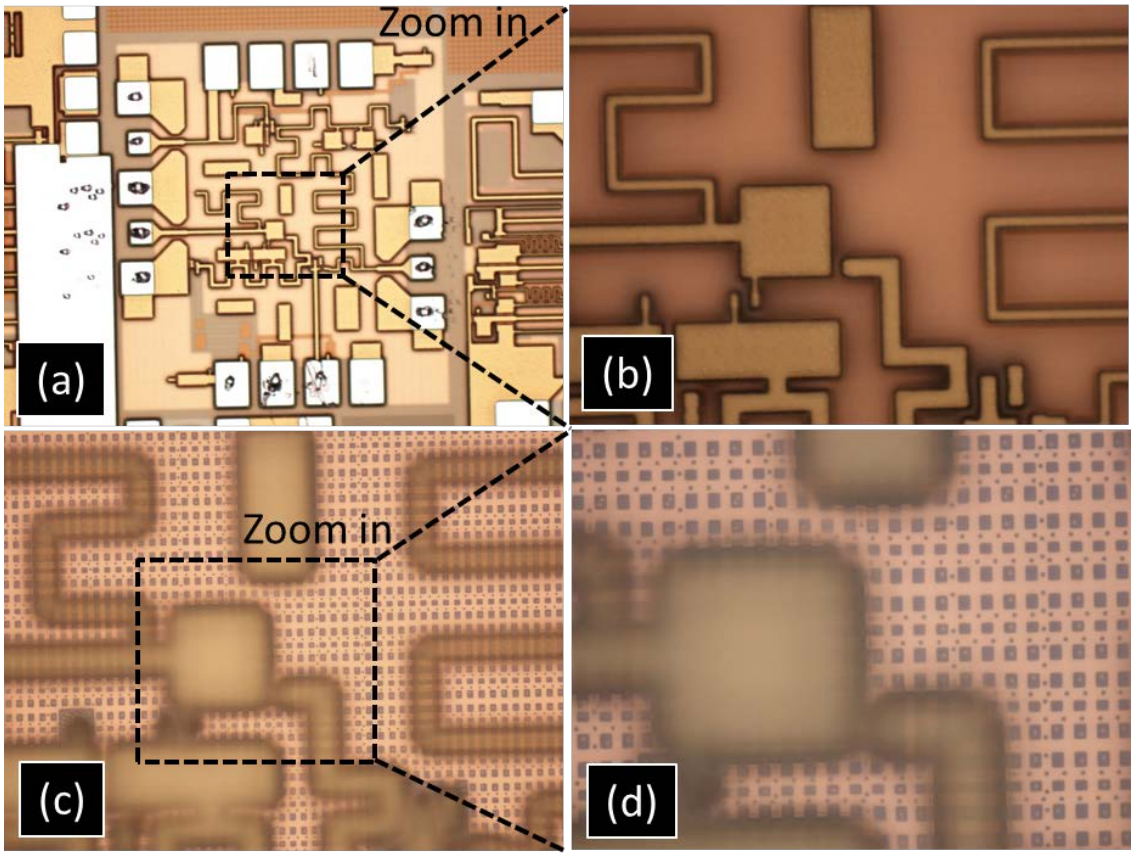


Fig. 4.23. The 8XP PALNA chip images taken using a high resolution camera. (a) A chip area is selected for zoom-in. (b) No undesirable metal fill is observed around the top metal transmission lines. (c) Focus adjustment reveals the ground plane “fine mesh” and no metal fill artifacts are observed between the top layer transmission line signal metal and the ground plane. (d) Further zoom and focusing reveals no fill presence.

4.7 Summary

This chapter presented a PALNA design in GlobalFoundries 8XP technology where the PALNA MNs were implemented using transmission lines. However in this design, unlike in the design presented in the previous chapter, the PA and the LNA were designed from scratch and the output MN of the PA and the input MN of the LNA were integrated with the PALNA MN, eliminating the 50 Ω MNs inside of PA and LNA. Further, in this design the PALNA MN impedance matching was done specifically to maximize the PALNA PAE in the transmit mode and to minimize the PALNA NF in the receive mode. Based on simulations presented, SOA performance was achieved with this PALNA in both modes

of operation. However, it was recognized that the PALNA performance was slightly tilted in the favor of the receive mode and less than fully optimal in the transmit mode of operation, motivating the need for a new PALNA design methodology that is more effective than the Cadence-based manual optimization approach followed in this design.

By being done fully in Cadence, the manual optimization approach followed in this chapter attempted to include and mitigate all the PALNA MN transmission line losses as contributors to the overall PALNA performance. However, it is noted that the length of the transmission line L2 in the LNA MN of the final PALNA design is 1018 μm, which is quite long and likely more lossy that desired. Therefore, an alternative PALNA design methodology is needed, where the best possible PALNA solution can be found, with minimal losses in the PALNA MN.

Building on the lessons learned in this design, the next chapter develops and presents a novel loss-aware PALNA design methodology. The methodology is then applied to produce a PALNA design whose performance is both optimal in transmit mode and receive mode, and superior to the published SOA of mm-wave T/R circuit design.

Chapter Five: **A 94 GHz Switchless PALNA with Simultaneous Optimum Impedance Matching and Minimum Loss**

5.1 Technology Overview and Considerations

As described in Chapter 3, the 32SOI process used for this design is a 12-metal aluminum and copper process. The top four metal layers (LB-MB-MA-E1) are again used to implement the transmission lines as microstrips with the LB layer serving as the signal layer and the E1 layer serving as the ground layer. And, again, no metal or vias are used on layers between LB and E1, and those intervening layers are filled with dielectric. However, unlike the PALNA design in Chapter 3, the PALNA designs presented in this section take into account the losses attributable to the transmission lines and these losses are a key consideration in the PALNA design and implementation methodology. Fig. 5.1 shows the attenuation constant of the transmission lines designed in 32SOI at 94 GHz as a function of characteristic impedance. The attenuation constant represents the transmission

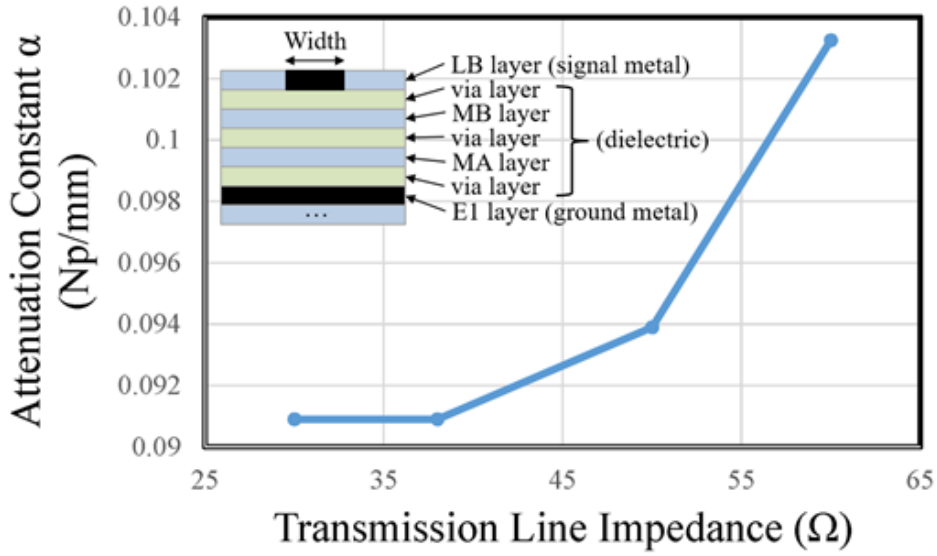


Fig. 5.1. The attenuation constant of the transmission lines (cross-section is shown) at 94 GHz as a function of transmission line impedance. Microstrip substrate parameters are not provided due to proprietary restrictions.

line dissipative loss per unit length. Additionally, the designs presented in this section leverage lumped elements capacitors and inductors, whose losses are also carefully considered in the design procedure. Fig. 5.2 shows the equivalent series resistance (ESR) of capacitors and inductors designed in 32SOI technology at 94 GHz as a function of capacitance and inductance, respectively. The ESR is used to model the dissipative loss of the lumped components. The attenuation constant values and the ESR values shown in Fig. 5.1 and Fig. 5.2 are found using Cadence simulations with s-parameter files obtained from EM simulations of transmission line segments and lumped components in Sonnet.

The Global Foundries 32SOI process features active devices (e.g., FETs, MOSVARs, Forward Bias Diode) and passive devices (e.g., MIMs, resistors, inductors, transmission lines, etc.) with nominal nFET and pFET performance of f_T = 300 GHz and f_{MAX} = 350 GHz [41]. The 32SOI nFET design and biasing considerations are discussed below, in the PA and LNA core circuit design sections. In circuit designs presented in this chapter, EM simulation software Sonnet was used, to custom build and simulate all transmission lines, transistor and capacitor embedding structures, MOM capacitors, transmission line junctions, etc.

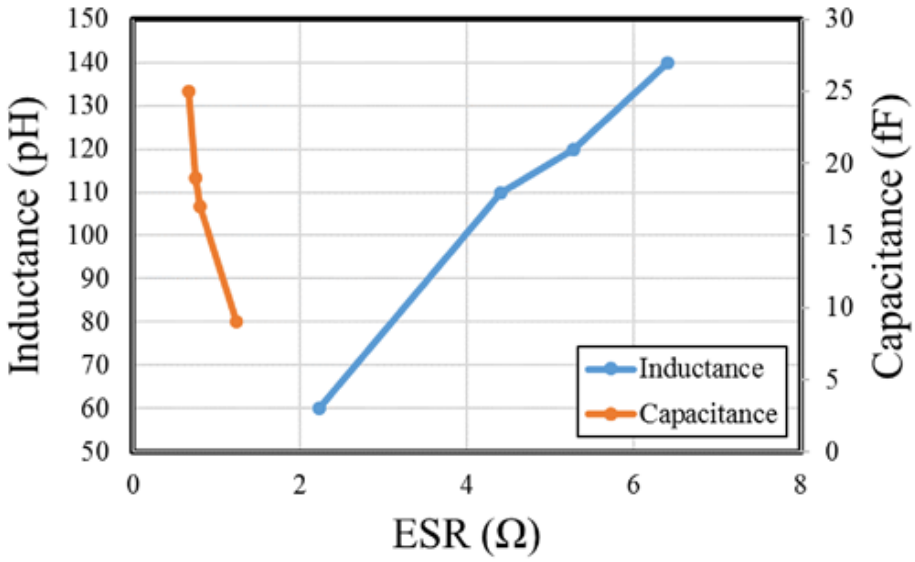


Fig. 5.2. The ESR of capacitors and inductors at 94 GHz.

5.2 PALNA Design Methodology

Practical matching networks introduce two types of losses, one due to the reflection of energy (mismatch loss), and the other due to the dissipation of energy (dissipative loss) [42]. In order to capture all the losses present in the PALNA matching network, the transducer loss of the network between the active ports of the circuit is simulated in both the transmit and the receive mode of operation. For a thorough characterization of losses due to finite conductivity and dielectric loss in the transmission lines, transistor embedding networks, and the on-chip lumped components, EM simulated s-parameter models are used for each component. Fig. 5.3 illustrates a step-by-step design flow of the PALNA matching network.

Step 0: The design flow begins by designing LNA and PA core circuits without the 50 Ω output and input matching networks. All transmission lines, lumped components, and transistor terminal embedding networks used in the core circuits are designed and modeled using their exact 32SOI layout geometries in the Sonnet electromagnetic (EM) simulator.

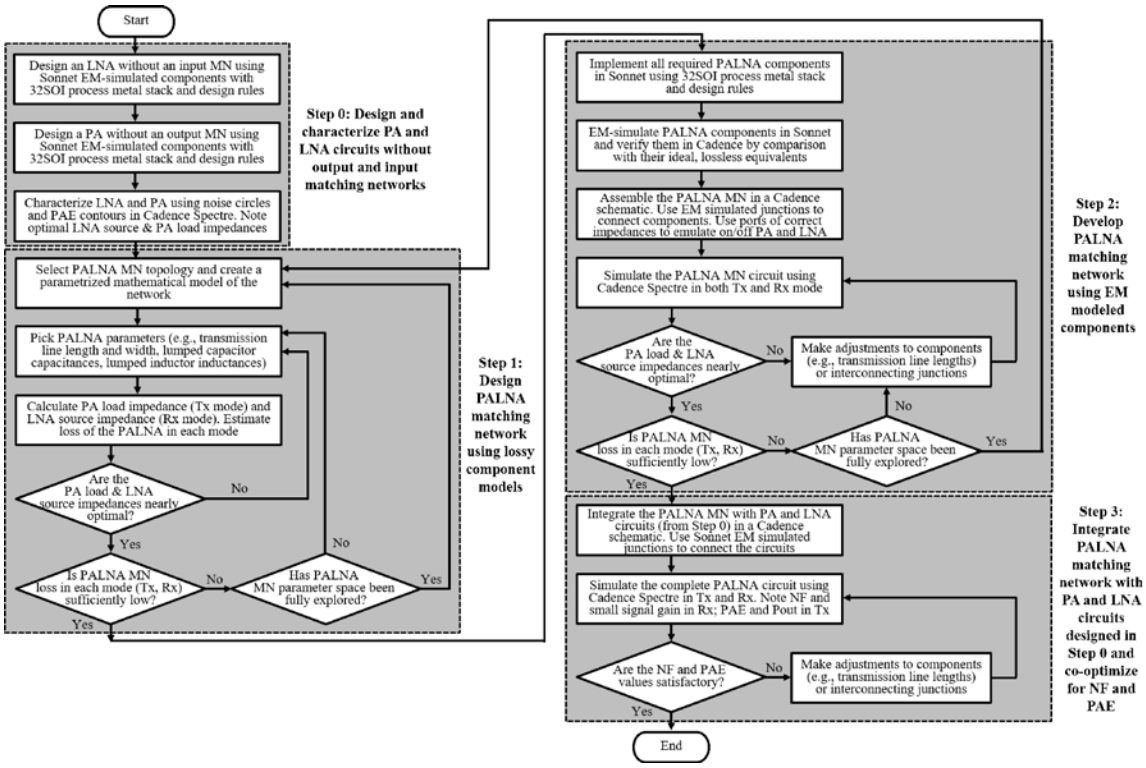


Fig. 5.3. PALNA design methodology flowchart.

All transistors in the core circuit designs include post-layout extracted parasitics. Once the core LNA and PA circuits are designed, their ON-state, OFF-state, and optimal impedances are determined experimentally, by simulation, and the PALNA matching network is designed in the following three basic, iterative steps.

Step 1: Initial versions of matching networks that simultaneously achieve the optimal PA and LNA impedances are designed. For the transmit mode, the optimum PA load impedance is defined as the impedance that maximizes the PAE and produces good P_{out} and power gain. For the receive mode, the optimum LNA source impedance is defined as the impedance that minimizes the NF and produces good small signal gain. Transducer loss is estimated in the receive and the transmit mode of operation for each network and the candidate networks with the lowest losses in both modes are selected. Transmission lines and lumped components are modeled as lossy, using the attenuation constant α and equivalent series resistance (ESR), respectively, obtained from Sonnet EM simulations.

In PALNA transmit mode shown in Fig. 1.5(a), a two port network can be defined as the cascade of the PALNA Output MN and the antenna, where the input port (i.e., port 1) is defined at the PA looking into the PALNA Output MN, and the output port (i.e., port 2) is defined at the antenna looking out. It can be shown that the [ABCD] matrix of that two-port network is:

$$\begin{bmatrix} A_{TX} & B_{TX} \\ C_{TX} & D_{TX} \end{bmatrix} = \begin{bmatrix} D_P + B_P(Y_{ANT} + Y_{RX\_OFF}) & B_P \\ C_P + A_P(Y_{ANT} + Y_{RX\_OFF}) & A_P \end{bmatrix} \tag{5.1}$$

where $Y_{ANT} = 1/(50\ \Omega)$ is the admittance of the antenna port and Y_{RX_OFF} is the admittance of the "off" LNA branch, which equals:

$$Y_{RX\_OFF} = \frac{C_L Z_{LNA\_OFF} + D_L}{A_L Z_{LNA\_OFF} + B_L} \tag{5.2}$$

In PALNA receive mode shown in Fig. 1.5(b), a two port network can be defined as the cascade of the antenna and the PALNA Input MN, where the input port (i.e., port 1) is defined at the antenna looking toward the PALNA Input MN, and the output port (i.e., port 2) is defined at the LNA looking toward the LNA. It can be shown that the [ABCD] matrix of that two-port network is:

$$\begin{bmatrix} A_{RX} & B_{RX} \\ C_{RX} & D_{RX} \end{bmatrix} = \begin{bmatrix} A_L & B_L \\ C_L + A_L(Y_{ANT} + Y_{TX\_OFF}) & D_L + B_L(Y_{ANT} + Y_{TX\_OFF}) \end{bmatrix} \tag{5.3}$$

where Y_{TX_OFF} is the admittance of the "off" PA branch, which equals:

$$Y_{TX\_OFF} = \frac{C_P Z_{PA\_OFF} + D_P}{A_P Z_{PA\_OFF} + B_P} \tag{5.4}$$

Then, using the two-port z-parameters, PALNA input impedances and their associated PALNA impedance matching criteria can be expressed as follows:

$$Z_L = Z_{11\_TX} = \frac{A_{TX}}{C_{TX}} = Z_{opt\_PA} \tag{5.5}$$

and

$$Z_S = Z_{22\_RX} = \frac{D_{RX}}{C_{RX}} = Z_{opt\_LNA} \tag{5.6}$$

In addition to impedance matching, as discussed above, PALNA must have minimal transducer loss in each mode of operation. The theoretical upper limit of a two-port network power transfer efficiency can be predicted using the concept of the kQ product [43]. Given the [ABCD] matrices in (5.1) and (5.3) and assuming $Y_{ANT} = 0$, PALNA Z parameters can readily be calculated using the two-port network conversion expressions

$$Z_{11} = \frac{A}{C}, Z_{12} = \frac{AD - BC}{C}, Z_{21} = \frac{1}{C}, Z_{22} = \frac{D}{C} \tag{5.7}$$

where AD – BC = 1 since PALNA matching networks are reciprocal. Since, in each mode of operation, the PALNA Z matrix equals

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} + j \begin{bmatrix} X_{11} & X_{12} \\ X_{21} & X_{22} \end{bmatrix} \tag{5.8}$$

and

$$kQ = \frac{|Z_{21}|}{\sqrt{|\boldsymbol{R}|}} = \frac{\sqrt{R_{21}^2 + X_{21}^2}}{\sqrt{R_{11}R_{22} - R_{12}R_{21}}} = \tan 2\theta \tag{5.9}$$

then

$$\eta_{max} = (\tan\theta)^2 \tag{5.10}$$

quantifies the PALNA's maximum available power transfer efficiency [43]. Stated in terms of power transfer loss, the minimum loss caused by the network is expected to be

$$Loss_{min} = 10\log_{10}(\eta_{max}) \tag{5.11}$$

For lower dissipative loss, PALNA circuits with maximum η_{max} are of interest, which can be achieved by optimizing the PALNA with respect to kQ in both modes of operation. For example, since η_{max} is a monotonically increasing function of kQ and a higher kQ corresponds to a higher η_{max}, a kQ of 20 would result in η_{max} > 90 % which, if achieved, would be equivalent to minimum achievable PALNA loss of 0.43 dB.

As mentioned above, in addition to the dissipative loss described by (5.11), the PALNA network in each mode of operation will sustain conjugate mismatch losses at the antenna port and at the ON amplifier port. These losses can be computed using the expression [42]

$$M = 10log_{10}\frac{|Z_G + Z_1|^2}{4R_G R_1} \tag{5.12}$$

The dissipative and mismatch losses, in each mode of operation, can conveniently be combined into a single, overall loss metric using the concept of transducer loss [44]

$$Loss_{combined} = 10log_{10}(Loss_{transducer}) = 10log_{10}\left(\frac{1}{G_{transducer}}\right) \tag{5.13}$$

where

$$G_{transducer} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} = \frac{4R_G R_L|Z_{21}|^2}{|(Z_{22}+Z_L)(Z_{in}+Z_G)|^2} \tag{5.14}$$

Equations (5.5), (5.6), and (5.13) express the design criteria of the PALNA circuit in terms of the [ABCD] variables of the PA and LNA MNs. Selection of specific MN circuit topologies (e.g., transmission line, lumped element LC circuit) defines the MN [ABCD]

values in terms of MN circuit component values (e.g., transmission line length and width, inductance, capacitance). In order to identify candidate PALNA MNs that achieve the design criteria in both modes of operation, a multi-variable design and optimization problem must be solved. In this paper, for each candidate PALNA MN and its optimization variables (i.e., circuit component values), this problem was solved using a computer-automated exhaustive search, where four objective functions (transmit impedance match, transmit loss, receive impedance match, and receive loss) defined by equations (5.5), (5.6), and (5.13) were implemented inside a MATLAB nested loop and evaluated over a range of optimization variable values until a small number of variable sets emerged that achieved the design criteria. The ranges of values over which the variables were swept represent constraints defined by component values practically obtainable in 32SOI.

MATLAB-based optimization is convenient and simple to implement, and the circuit parameter design space can be fully explored for a variety of MN topologies. On the other hand, if the MATLAB-based optimization is replaced by manual optimization in a circuit design tool (e.g. Cadence in this work), the MN design process would require extensive trial-and-error and the MN performance outcome would be uncertain.

Step 2: To further improve the dissipative losses model, candidate matching networks are implemented and simulated in Cadence, using Global Foundries 32SOI EM-simulated transmission lines and lumped components s-parameter models. Particular attention is paid to practical considerations such as required length and width of the transmission lines, and physical size of the overall matching network layout.

Step 3: The matching networks that perform well and are deemed practical from the implementation point of view are integrated with the PA and LNA circuits and co-optimized manually using Cadence Spectre small signal and load pull simulations. The co-optimization procedure involves manually switching between the transmit and the receive modes of operation, simulating the performance of interest, and manually adjusting the matching network design to fine-tune the performance in each mode. In particular, in the transmit mode, the performance is optimized using PAE load pull contours, P_{in} vs. P_{out}

curve, power gain curve, and PAE curve. In the receive mode, the performance is optimized using the noise circles, the NF, and small signal s-parameters. The matching network parameters adjusted are transmission line dimensions and sizes of capacitors.

It should be noted that formulating the PALNA design as a traditional optimization problem is not feasible (see Appendix A).

5.3 PA and LNA Core Designs in 32SOI

5.3.1 PA Core Design

Integrated PA design involves numerous approaches and techniques aimed at managing tradeoffs between P_{out}, PAE, linearity, and operational bandwidth [45]. In this PALNA design, the primary goal is to maximize the PAE. For this design, a "Class-E-like" PA circuit topology with two stacked devices is chosen [21]. Fig. 5.4 shows the schematic of the core 94 GHz PA circuit. In order to facilitate the circuit integration into a 50 Ω RF front end, it is assumed that the PA input source impedance is 50 Ω. For maximum PAE and good P_{out} and power gain at 94 GHz, nFET transistors with 1 μm fingers and a total width of 24 μm were selected through iterative simulation. Fig. 5.5 shows the result of Cadence Spectre simulation, with constant PAE load pull contours, without and with the input matching network. The contours define the needed PA output load impedance for maximum PAE at 94 GHz. The addition of the input matching network increases the value of the highest PAE contour by 6.6 %. It may be noted that the PA optimal output load impedance, Z_{opt_PA}, lies in an *allowed region* on the Smith chart [46] so, other than the series 40 fF DC blocking capacitor, no pre-matching is needed at the output of the PA. The goal of the PALNA matching network will be to transform the 50 Ω antenna impedance to an optimum load impedance at the PA, Z_{opt_PA}, and achieve the maximum PA PAE in the PALNA transmit mode.

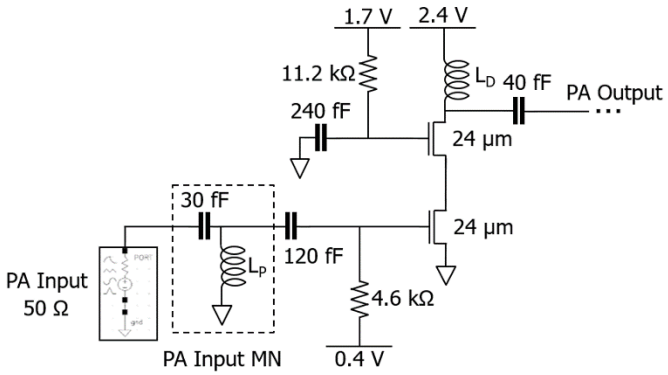


Fig. 5.4. Schematic of Class-E-like PA circuit with two stacked devices.

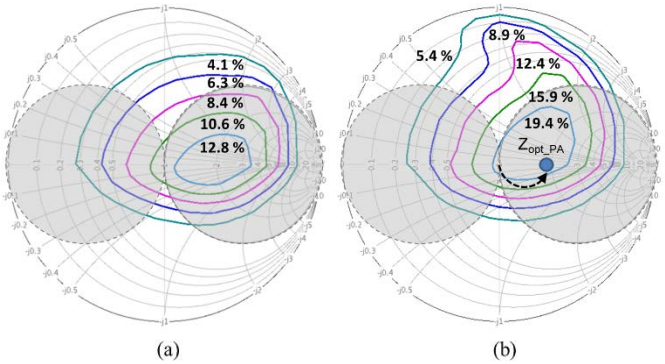


Fig. 5.5. Constant PAE load pull contours without (a) and with (b) PA input matching network. The optimum PA output load impedance needed for the maximum PAE at 94 GHz is shown in (b). The optimum load impedance is found to be 90 Ω using simulation experiments.

5.3.2 LNA Core Design

Recently, in integrated LNA design, it has been observed that an optimum transistor size choice can enable a simultaneous noise and impedance input match, greatly relieving the traditional LNA design tradeoffs [22]. In this PALNA design, the LNA design methodology outlined in [22] is followed, and the LNA circuit is optimized for best NF and small-signal gain performance.

Fig. 5.6 shows the schematic of the core 94 GHz LNA circuit. In order to facilitate the circuit integration into a 50 Ω RF front end, it is assumed that the LNA output load impedance is 50 Ω. A single-ended, single-stage cascode circuit is used with current mirror

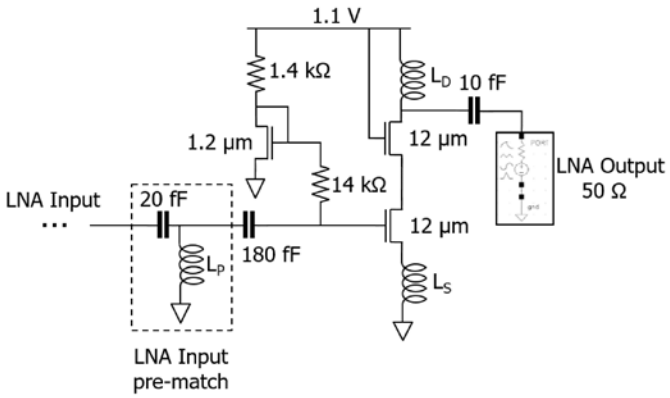
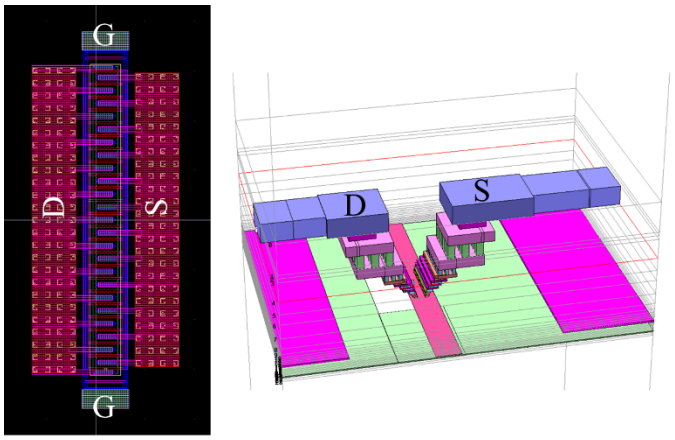


Fig. 5.6. Schematic of LNA circuit with input pre-match.

biasing. For maximum LNA gain and minimum NF, with minimum output matching required and thus minimum loss, transistors with 1 µm fingers and a total width of 12 µm were found, by iterative simulation, to be the most favorable. Fig. 5.7 shows the LNA transistor layout and a corresponding EM simulated transistor terminal embedding network model included in the LNA circuit simulations.

Since transistor biasing current *density* (I_{DS}/W) required for minimum NF or maximum gain is independent of CMOS technology [22], an initial current density of 0.1 mA/µm was chosen for biasing of the 32SOI nFETs in the LNA circuit. Then, the current density was gradually increased and the LNA NF and gain were simulated with each increase. Finally, it was determined by the simulation trials that the 32SOI nFETs in the LNA circuit should be biased at an optimum current density of 0.3 mA/µm, which is consistent with the 94 GHz numerical design example given in Table 1 of [22]. The biasing circuit was designed using a 1.2 µm transistor, in order to minimize the circuit's power overhead. The 180 fF series capacitor at the input and the 10 fF series capacitor at the output are the DC blocking capacitors. Fig. 5.8 shows the constant noise and gain circles of the LNA circuit, which were generated using a Cadence Spectre simulation.



(a) (b)

Fig. 5.7. LNA transistor layout (a) and an EM simulated transistor terminal embedding network model (b), which were included in the LNA circuit simulations.

Series transmission line sections can be used to match complex load impedances to complex source impedances, however the impedances must lie within the *allowed regions* on the Smith chart [46]. In Fig. 5.8, these allowed regions are shaded with light gray color on each Smith chart. It can be seen that source impedances Z_{opt_N} and Z_{opt_G}, which must be seen by the LNA input in order to achieve minimum LNA NF and maximum gain, lie outside the *allowed regions*. This means that, in this particular case and in general, LNA MN could not be a single transmission line section unless a "LNA Input pre-match circuit" is added to the core LNA circuit in order to move impedances Z_{opt_N} and Z_{opt_G} into the *allowed regions* [46].

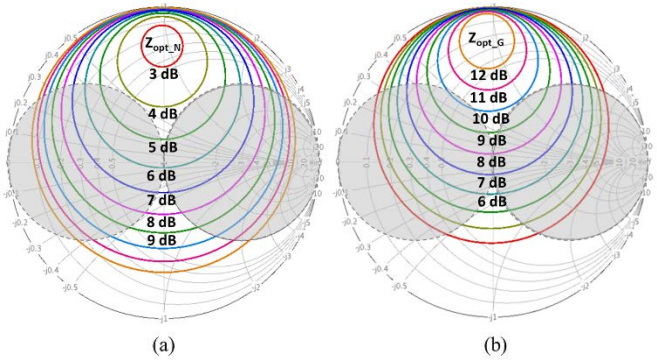


Fig. 5.8. Constant NF circles (a) and constant gain circles (b) define the optimum source impedance for the 12 μm nFET transistor at 94 GHz.

Since it is of interest to achieve the simplest possible PALNA solution, it is desirable for the PA and LNA MNs to possibly be series transmission lines. Therefore, in this case, the LNA needs to be "pre-matched", by adding the "LNA Input pre-match circuit" at LNA input, before an iterative PALNA design procedure is employed. The pre-match of the LNA is accomplished using an L-network, consisting of a series, lumped 20 fF capacitor and a shunt inductor implemented using a transmission line section. After the pre-match, as shown in Fig. 5.9, the LNA optimal source impedances move to an *allowed region* of the Smith chart, as needed. From this point on, the goal of the PALNA matching network will be to transform the 50 Ω antenna impedance to an optimum source impedance at the LNA, Z_{opt_LNA}, and simultaneously achieve a minimum LNA NF and a maximum LNA small signal gain in the PALNA receive mode. All transmission lines, lumped components, and transistor embedding networks as referenced and used in simulations described in this paper, were designed and modeled using their exact 32SOI layout geometries in the Sonnet electromagnetic (EM) simulator. All transistors include post-layout extracted parasitics.

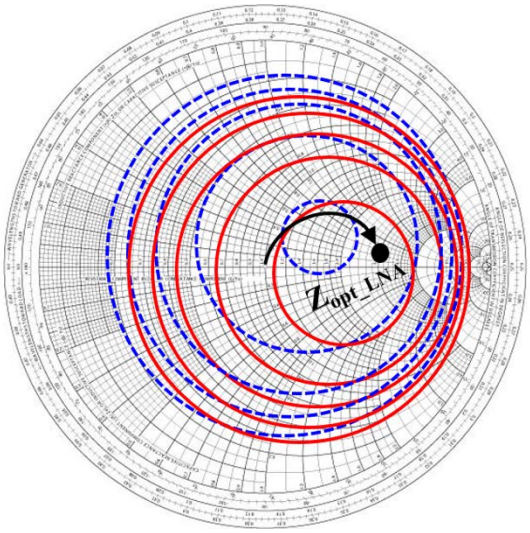


Fig. 5.9. Constant NF circles and constant gain circles define the optimum source impedance for the LNA pre-match at 94 GHz. The optimum source impedance is found to be 150+j25 Ω using simulation experiments. Constant NF circles are shown using dashed blue lines and constant gain circles are shown using solid red lines. The innermost circles represent 4 dB and 11 dB, for NF and gain. NF circles increase in 1 dB steps and gain circles decrease in 1 dB steps.

5.4 PALNA Design and Implementation in 32SOI

After the core PA and LNA circuits are designed as described in sections 5.3.1 and 5.3.2, including all components shown in Fig. 5.4 and Fig. 5.6, their ON/OFF/Optimal impedances at 94 GHz are obtained from Cadence simulations. ON and OFF impedance of each circuit is obtained as a complex Z_{11} parameter from one-port s-parameter simulation, with circuit biasing in ON and OFF state, respectively. Table 5.1 summarizes the simulated impedances of the PA and LNA core circuits discussed above.

As discussed in section 5.2 above, a three-step process is then followed to complete the PALNA circuit design.

Table 5.1.
Impedances Associated With Core Circuits From Section III at 94 GHz.

	ON Impedance	**OFF Impedance**	**Optimal Impedance**
LNA Input	117+j13	38+j38	150+j25
PA Output	289+j1	441+j177	90

Step 1

Fig. 5.10 shows a PALNA network topology with PA MN and LNA MN implemented using transmission lines. The following four tasks are completed, as an iterative design procedure using MATLAB, to determine the values of Z_1, Z_2, l_1, l_2, and thereby produce PALNA design that satisfies the design criteria.

(1) A parametric mathematical model of the network from Fig. 5.10 is created first. Since the PA MN and the LNA MN are implemented using transmission lines, each MN is represented using the following [ABCD] matrix:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TL} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \frac{1}{Z_0}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \tag{5.15}$$

where Z_0 and l are the transmission line characteristic impedance and length, and $\gamma = \alpha + j\beta$ is the complex transmission line propagation constant with the attenuation constant, α, representing the transmission line dissipative loss per unit length and the phase constant, β, representing the phase shift per unit length of the transmission line. α and β are found using Cadence simulations with s-parameter files obtained from EM simulations of transmission line segments in Sonnet.

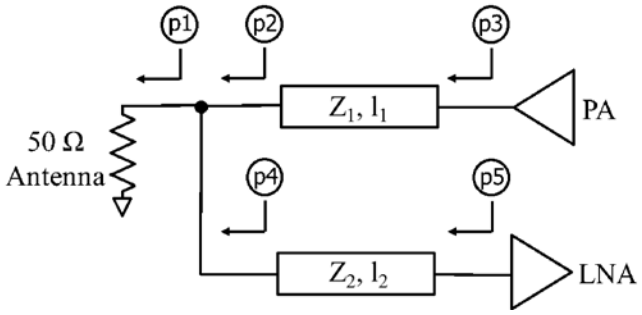


Fig. 5.10. PALNA topology with MNs implemented as transmission lines. The LNA includes the "input pre-match" network shown in Fig. 5.6. The PA includes the "PA input MN" network shown in Fig. 5.4. The PALNA MN transforms the 50 Ω impedance seen at point p1 into optimal impedances needed at points p3 and p5 in transmit and receive mode of operation, respectively.

In order to maximize Q of the transmission lines, as described above, the top four metal layers (LB-MB-MA-E1) are used to implement the transmission lines as microstrips with the LB layer serving as the signal layer and the E1 layer serving as the ground layer. Fig. 5.1 shows the attenuation constant α of the transmission lines designed in the 32SOI technology at 94 GHz as a function of characteristic impedance. Using (5.1) - (5.4) and (5.15), the parametric model of the given network topology is completed. The network parameters of interest that are unknown are Z_1, Z_2, l_1, and l_2, and their optimal values are found through an automated search and optimization procedure. The network parametric model described is coded into a MATLAB program. The program consists of a four-layer iterated loop representing parameters Z_1, Z_2, l_1, and l_2, which are swept across all of their practically realizable values. Each time the loop is executed, for a specific set of the parameter values, the quantities described in the following steps are computed inside the loop.

(2) Assuming that the circuit is in transmit and that the LNA bias is turned off (LNA off-state impedance is given), Z_L is computed at point p3 (Fig. 5.10) and compared to Z_{opt_PA} as shown in (5.5). Minimum transducer loss of the network in transmit is computed using (5.13).

(3) Assuming that the circuit is in receive and that the PA bias is turned off (PA off-state impedance is given), Z_S is computed at point p5 (Fig. 5.10) and compared to Z_{opt_LNA} as shown in (5.6). Transducer loss of the network is computed using (5.13).

(4) A minimum range of deviation from the optimal impedances, as expressed in the design criteria in (5.5) and (5.6), is user defined and, if both of the computed impedances Z_L and Z_S are within this range, the network parameters and performance metrics are stored in a data file for subsequent review. When the code execution inside the loop is completed, the network parameters are updated and tasks 2 and 3 are repeated. The loop runs until all combinations of Z_1, Z_2, l_1, and l_2 have been considered. When the loop execution stops, the candidate solutions stored in the data file are reviewed for loss performance and suitability of implementation.

For the network topology shown in Fig. 5.10, the best solution was achieved for the following combination of parameters: Z_1=38 Ω, Z_2=30 Ω, l_1=223^o, and l_2,=132^o. The minimum transducer transmit and receive losses achieved are 5.16 dB and 4.19 dB, respectively. Fig. 5.11 shows the impedance matching performance of the PALNA in both modes of operation.

It is noted that, while the network topology from Fig. 5.10 is capable of achieving good simultaneous impedance match in both modes of circuit operation, the kQ achieved with this topology is limited to 7 in both modes. To improve kQ and simultaneously meet both the impedance matching and loss design criteria, PALNA topologies with additional degrees of freedom are considered. Fig. 5.12 shows a PALNA network topology where the LNA MN is implemented using a lumped-element CLC circuit.

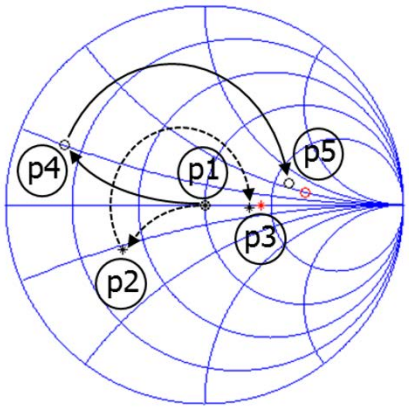


Fig. 5.11. The impedance matching performance of network topology shown in Fig. 5.10, designed using loss aware methodology in MATLAB. The dashed arrow lines and solid arrow lines represent the transmit mode and the receive mode impedance transformations, respectively. Red circle and red asterisk show the optimal, goal impedances at LNA and PA, respectively. In receive, LNA bias is turned ON and PA bias is turned OFF. In transmit, LNA bias is turned OFF and PA bias is turned ON. The design frequency is 94 GHz.

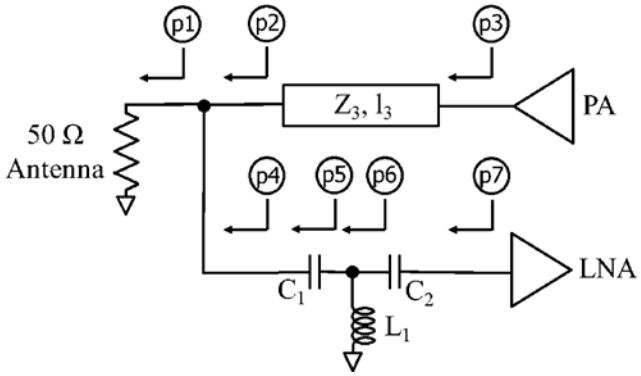


Fig. 5.12. PALNA circuit topology with LNA MN implemented using a lumped-element CLC circuit. The PALNA MN transforms the 50 Ω impedance seen at point p1 into optimal impedances needed at points p3 and p7 in transmit and receive mode of operation, respectively.

The LNA MN [ABCD] matrix can be expressed as matrix product

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{LNA\ MN\ 1} = \boldsymbol{M_1 M_2 M_3} \tag{5.16}$$

where

$$\boldsymbol{M_1} = \begin{bmatrix} 1 & \frac{1}{j\omega C_1} + R_1 \\ 0 & 1 \end{bmatrix}, \boldsymbol{M_2} = \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_1 + R_2} & 1 \end{bmatrix}, \boldsymbol{M_3} = \begin{bmatrix} 1 & \frac{1}{j\omega C_2} + R_3 \\ 0 & 1 \end{bmatrix} \quad (5.17)$$

and resistors R_1 ... R_3 represent the ESRs of the reactive elements. Resistor values R_1 ... R_3 are determined using Cadence simulation experiments on s-parameter files obtained from EM simulations of capacitors and inductors in Sonnet. Fig. 5.2 shows the ESR of the capacitors and inductors designed in the 32SOI technology at 94 GHz as a function of capacitance and inductance, respectively. For the network topology shown in Fig. 5.12, the four design tasks described above were completed and the best solution was achieved for the following combination of parameters: Z_3=54 Ω, l_3=122°, C_1=25 fF, L_1=120 pH, C_2=10 fF. The minimum transducer transmit and receive losses achieved are 3.58 dB and 3.49 dB, respectively.

Similarly, Fig. 5.13 shows a PALNA network topology where the LNA MN is implemented using a lumped-element LCLC circuit, with an additional degree of freedom. The LNA MN [ABCD] matrix can be expressed as matrix product

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{LNA\ MN2} = \boldsymbol{M_1 M_2 M_3 M_4} \quad (5.18)$$

where

$$\boldsymbol{M_1} = \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_2 + R_4} & 1 \end{bmatrix}, \boldsymbol{M_2} = \begin{bmatrix} 1 & \frac{1}{j\omega C_3} + R_5 \\ 0 & 1 \end{bmatrix},$$
$$\boldsymbol{M_3} = \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L_3 + R_6} & 1 \end{bmatrix}, \boldsymbol{M_4} = \begin{bmatrix} 1 & \frac{1}{j\omega C_4} + R_7 \\ 0 & 1 \end{bmatrix} \quad (5.19)$$

Table 5.2.
Estimated Loss Metrics of the Above Three PALNA Topologies. Transducer Loss is Calculated Using (5.13).

Loss Metric	Fig. 5.10 PALNA		Fig. 5.12 PALNA		Fig. 5.13 PALNA	
	Tx	Rx	Tx	Rx	Tx	Rx
kQ	5.38	6.87	8.2	4.5	10.93	3.22
Dissipative Loss [dB]	1.6	1.26	1.1	1.9	0.79	2.66
Mismatch Loss at Active Amplifier [dB]	1.71	0.15	1.57	0.19	1.18	0.28
Mismatch Loss at the Antenna Port [dB]	1.62	1.49	0.73	0.68	0.25	0.26
Transducer Loss [dB]	**5.16**	**4.19**	**3.58**	**3.49**	**2.73**	**3.31**

and resistors R_4 ... R_7 represent the ESR of the lumped capacitors and inductors. After the four design tasks from above were completed, the best solution was achieved for the following combination of parameters: Z_4=44 Ω, l_4=115º, L_2=60 pH, C_3=17 fF, L_3=140 pH, C_4=20 fF. The minimum transducer transmit and receive losses are 2.73 dB and 3.31 dB. Fig. 5.14 shows the impedance matching performance of the PALNA networks from Fig. 5.12 and Fig. 5.13. Table 5.2 summarizes the loss metrics estimated in MATLAB for the three shown PALNAs.

In addition to the three PALNA circuit topologies shown in Fig. 5.10, Fig. 5.12, and Fig. 5.13, other circuit topologies were investigated as potential solution candidates. In particular, topologies with various lumped element LC circuits in both the PA MN and the LNA MN were considered. Also, additional performance improvement was attempted by further increasing the order of the LC circuit in the LNA MN. However, the topologies shown in Fig. 5.10, Fig. 5.12, and Fig. 5.13 emerged as the best performers for the particular LNA and PA cores used. Table 5.3 summarizes the number of required loop executions.

MATLAB script source code for design of PALNA network shown in Fig. 5.13 is provided in Appendix B.

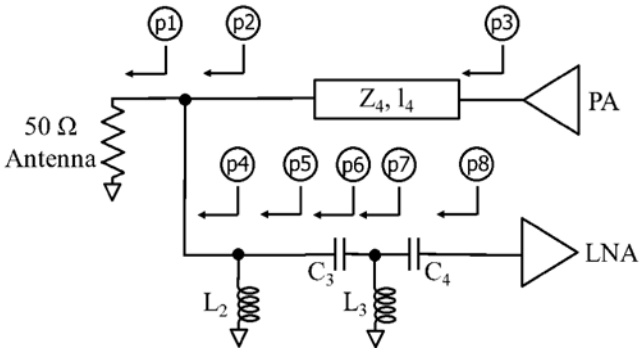
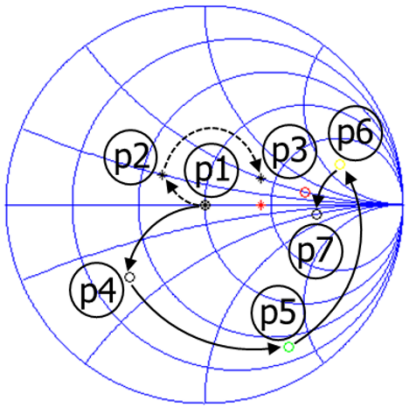
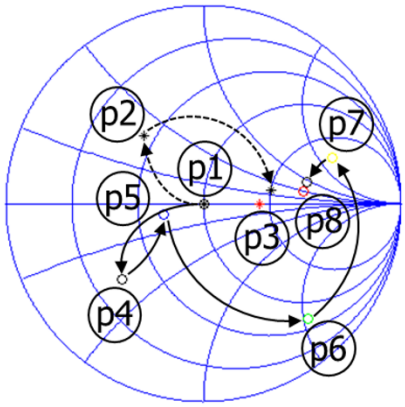


Fig. 5.13. PALNA circuit topology with LNA MN implemented using a lumped-element LCLC circuit. The PALNA MN transforms the 50 Ω impedance seen at point p1 into optimal impedances needed at points p3 and p8 in transmit and receive mode of operation, respectively.



(a)



(b)

Fig. 5.14. The impedance matching performance of network topologies shown in (a) Fig. 5.12 and (b) Fig. 5.13. The dashed arrow lines and solid arrow lines represent the transmit mode and the receive mode impedance transformations, respectively. Red circle and red asterisk show the optimal, goal impedances at LNA and PA, respectively. In receive mode, LNA bias is turned ON and PA bias is turned OFF. In transmit mode, LNA bias is turned OFF and PA bias is turned ON. The design frequency is 94 GHz.

Table 5.3.
Number of Required Optimization Nested Loop Executions in MATLAB and Search Script Total Execution Time.

	Fig. 5.10 PALNA	**Fig. 5.12 PALNA**	**Fig. 5.13 PALNA**
Number of Executions	361,890*	2,082,730*	782,994*
Search Script Total Execution Time in Seconds	87.5	398.2	154.4

Step 2

First, the EM models of all components required for the above PALNA circuits are implemented in Sonnet including the full transmission lines with their envisioned layout geometries. The exact 32SOI technology metallization stackup is used in the Sonnet models. The transmission lines and the inductors are implemented as microstrips and the capacitors are implemented as metal-oxide-metal (MOM) structures. The exact geometries of the inductors and the capacitors are optimized through simulation, by varying their geometrical features until their simulated performance most closely matches the performance of the ideal components needed. For the inductors, the microstrip width and length were varied and, for capacitors, the dimensions of the overlapping metal plates and the amount of the overlap were varied. Table 5.4 shows the dimensions of the microstrips needed to realize the circuits in Fig. 5.10, Fig. 5.12, and Fig. 5.13 in 32SOI, using the microstrip structure from Fig. 5.1. After the EM s-parameter models of the components are generated in Sonnet, they are integrated into Cadence Spectre schematics of circuits from Fig. 5.10, Fig. 5.12, and Fig. 5.13 in place of the corresponding transmission lines, capacitors, and inductors. The PA and the LNA core circuits are replaced with ports of appropriate ON/OFF complex impedance, shown in Table 5.1 above, and the schematics are simulated using Cadence Spectre small signal simulation. In accordance with the PALNA design criteria, two quantities are noted for each mode of operation in each PALNA network, namely the impedance that the network presents to the active amplifier and the transducer loss that the network introduces between the antenna and the active amplifier port.

Table 5.4.
Transmission Lines Needed to Realize Circuits From Step 1.

	Component	Width [µm]	Length [µm]
Transmission Lines	38 Ω, 223°	17	486
	30 Ω, 132°	24	306
	54 Ω, 122°	8.5	274
	44 Ω, 115°	13	258
Inductors	60 pH	5	120
	120 pH	5	210
	140 pH	5	226

Since the transducer loss readily translates to PALNA performance degradation in terms of NF and PAE and the noise circle and load pull simulations of the entire PALNA circuit in Cadence Spectre are very time consuming, this is an effective, time-efficient, and a necessary approach to designing PALNA circuits. Given that the abstracted PALNA simulations run very fast, designers can make numerous optimization runs, switching between modes of operation, making circuit adjustments, and simultaneously co-designing PALNA until the design criteria are met in both modes.

Table 5.5 summarizes the simulation results for the Cadence implementations of the three PALNA networks shown in Fig. 5.10, Fig. 5.12, and Fig. 5.13. It may be noted from the table, with reference to Fig. 5.11 and Fig. 5.14, that all three of the networks present acceptable impedance matches to the PA and the LNA. However, the network shown in Fig. 5.13 introduces the smallest amount of transducer loss in both modes of operation.

Also, by adjusting the PALNA matching networks for varying degrees of transducer transmit or receive loss, the co-design procedure makes it possible to design PALNA matching networks which trade off the transmit side performance against the receive side performance. This is potentially useful with regards to specific application designs, for example a T/R circuit where some NF performance can be sacrificed in order to improve the overall PAE performance. A traditional, 50 Ω matched, switch-based T/R circuit does not have this flexibility since the amount of loss introduced by the switch is usually approximately equal in both modes of operation.

Table 5.5.
Cadence Simulation Results for the Three PALNAs From Step 1.

Mode	PALNA Network	Goal Z_{OPT} [Ω]	Simulated Z_{OPT} [Ω]	Transducer Loss [dB]
Tx	Fig. 5.10	90	87-j2	5.3
	Fig. 5.12		66+j17	3.9
	Fig. 5.13		72+j9	3.7
Rx	Fig. 5.10	150+j25	130+j15	4.6
	Fig. 5.12		140+j52	4.3
	Fig. 5.13		125+j28	3.5

Table 5.6.
Summary of PALNA Losses at 94 GHz.

Mode of Operation	Minimum Loss in PALNA MN [dB]	Conjugate Antenna Mismatch Loss [dB]	Conjugate Amplifier Mismatch Loss [dB]	Transducer Loss [dB]
Tx	0.9	0.11	1.08	2.6
Rx	2.9	0.06	0.22	3.3

Based on the simulation performance shown in Table 5.5, the networks shown in Fig. 5.10 and Fig. 5.12 were dropped, and the network shown in Fig. 5.13 was selected for further investigation below. Also, the network from Fig. 5.10 requires transmission lines that are relatively long and wide, necessitating a physically larger final T/R circuit, which is undesirable from the implementation perspective.

Next, EM s-parameter models of component junctions are added to the selected PALNA circuit schematic and the PALNA transmission line lengths are readjusted, through an iterative procedure, to re-optimize the PALNA performance. Table 5.6 summarizes the losses associated with the final PALNA circuit, which were obtained from Cadence simulations. The simulated maximum power transfer efficiencies of the PALNA MN are 81 % and 51 % in the transmit and receive modes of operation, respectively. These efficiencies determine the minimum amount of power that is dissipated in the PALNA MN itself, independently of the impedance matching conditions at the antenna and at the PA/LNA amplifier circuits. As shown in column 1 of Table 5.6, the efficiencies translate into minimum theoretical loss of the PALNA MN of 0.9 dB and 2.9 dB in the transmit and receive modes, respectively.

In addition to the minimum loss due to the PALNA MN itself, additional losses result due to conjugate impedance mismatches at the antenna and at each of the amplifier circuits. These losses are shown in Table 5.6 and can be put into context by examining Fig. 1.5. In particular, the PALNA MN loss is the transducer loss measured between the antenna port and PA output or LNA input in transmit or receive mode, respectively. The conjugate antenna mismatch loss is measured at the antenna and is the result of impedance mismatch between Z_A and the 50 Ω antenna. The conjugate amplifier mismatch loss is measured at each ON amplifier; for the PA, the loss is the result of impedance mismatch between Z_{OUT_PA} and Z_L, and, for the LNA, the loss is the result of mismatch between Z_{IN_LNA} and Z_S. It should be noted that the losses summarized in Table 5.6 are in good agreement with the results presented in Table 5.2 above. Fig. 5.15 shows the impedance matching results of Cadence simulations of the final PALNA matching network. PAE load pull contours, which are representative of Tx mode matching goal, are overlaid on top of noise circles, which are representative of Rx mode matching goal. The red dot represents the achieved transmit mode impedance and the blue dot represents the achieved receive mode impedance. Good match is achieved in both modes. It should be noted that LNA gain circles are not shown for clarity reasons, however, maximum gain is realized with a minimal degradation in NF.

Step 3

In the final design step, the full PALNA circuit is implemented in Cadence and a complete set of simulations is performed, including small signal s-parameters, gain circles, noise circles, stability, constant-PAE load pull contours, and large signal simulations. This is the critical, final step in PALNA circuit design, which takes into account all the circuit variables and losses. The Cadence simulation is manually switched between the transmit and the receive mode, and the parameters of the PALNA circuit are manually adjusted until satisfactory performance is obtained in both modes. In transmit, the PALNA is optimized for PAE, P_{out}, and power gain. In receive, the PALNA is optimized for small signal gain and NF while maintaining stability. The optimization procedure takes into account, as additional constraints, the maximum current and voltage ratings of the LNA and the PA,

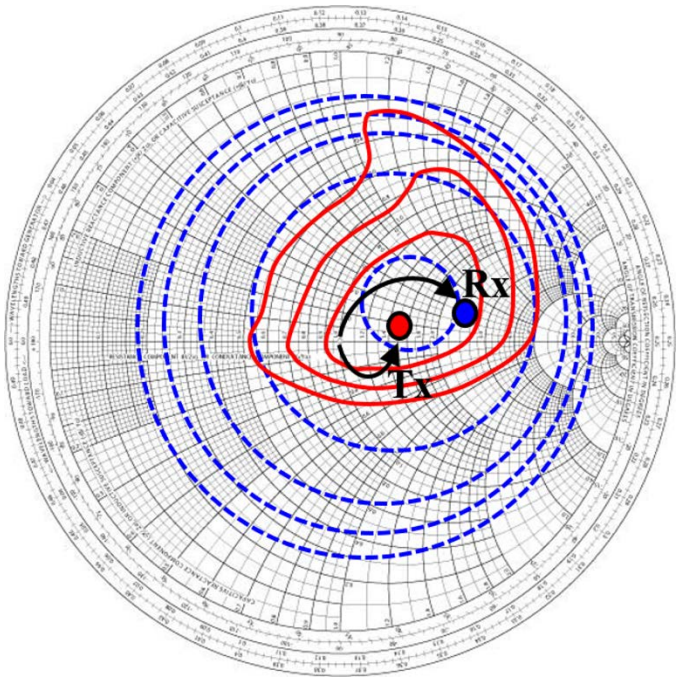


Fig. 5.15. The Cadence simulation results of PALNA circuit from Fig. 5.13. PAE load pull contours (solid red lines), which are representative of Tx mode matching goal, are overlaid on top of noise circles (dashed blue lines), which are representative of Rx mode matching goal. The red dot represents the achieved transmit mode impedance and the blue dot represents the achieved receive mode impedance. LNA gain circles are omitted for clarity reasons, although maximum LNA gain is realized with a negligible degradation in NF. LNA noise circles and the associated NF values are as shown in Fig. 5.9. PAE load pull contours, and the associated PAE values, are as shown in Fig. 5.5(b), with only the three most significant contours shown.

to ensure their robustness (e.g., peak current and voltage magnitudes are checked at the LNA input when PA is in transmit). Fig. 5.16 shows the schematic of the final 94 GHz PALNA circuit design. The number of manual design iterations needed to complete the circuit design shown was less than 10. Section 5.5 includes the summary of the PALNA circuit simulation results.

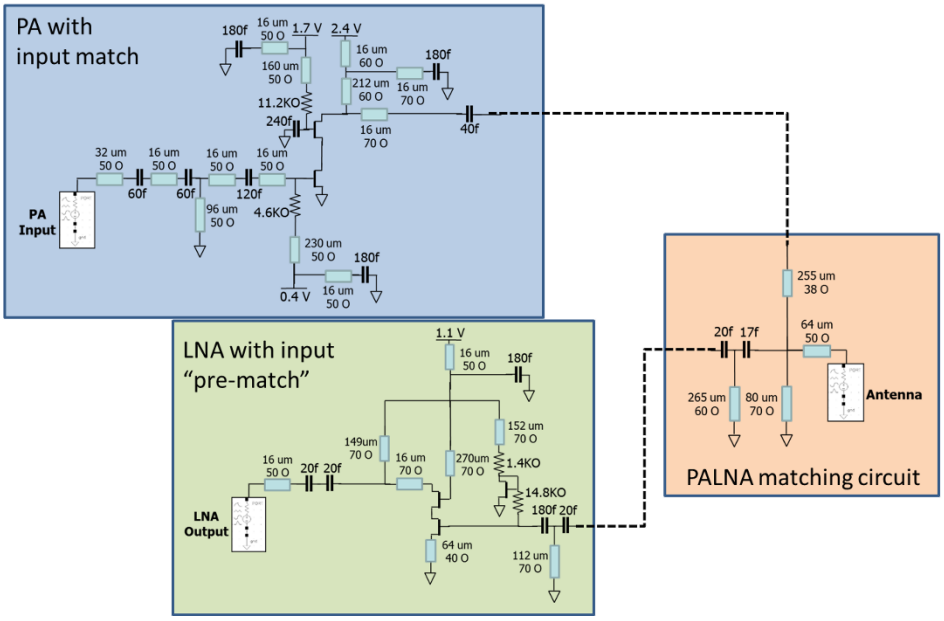


Fig. 5.16. Schematic of the final PALNA circuit design.

5.5 Simulation Results

The simulated performance of the final PALNA circuit design is shown in Figs. 5.17 – 5.21. Fig. 5.17 shows the simulated transducer loss of the PALNA matching network in the transmit and the receive modes of operation. Although a loss of 3 dB can be achieved simultaneously in both modes of operation, since a major design objective is to maximize the PAE, the transmit mode was intentionally designed to have a slightly lower loss than the receive mode. Fig. 5.18 shows the simulated PALNA small signal s-parameters and NF in the receive mode of operation. At the design frequency of 94 GHz, the s_{21} gain is 8 dB and the circuit is stable. The NF is 7.5 dB, which is in line with expectations given the minimum simulated NF of the LNA core circuit and 3.3 dB loss of the PALNA matching network. Fig. 5.19 shows the simulated PALNA large signal P_{out}, Power Gain, and PAE in the transmit mode of operation. Fig. 5.20 shows the simulated PALNA large signal performance as a function of frequency of operation. Fig. 5.21 shows the simulation of the PALNA port isolation as a function of frequency. The transmit and receive port isolations at 94 GHz are 18.7 dB and >20 dB, respectively. These isolation results are comparable with isolation performance that is achievable with integrated T/R switches at 94 GHz [1].

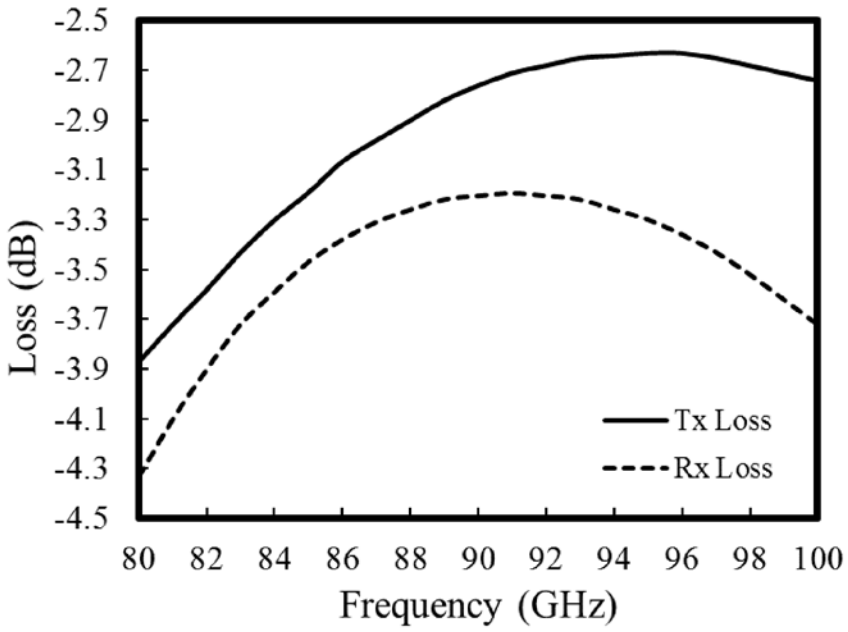


Fig. 5.17. Cadence Spectre simulation of PALNA matching network transducer losses. At the design frequency of 94 GHz, the receive mode transducer loss is 3.3 dB and the transmit mode transducer loss is 2.6 dB.

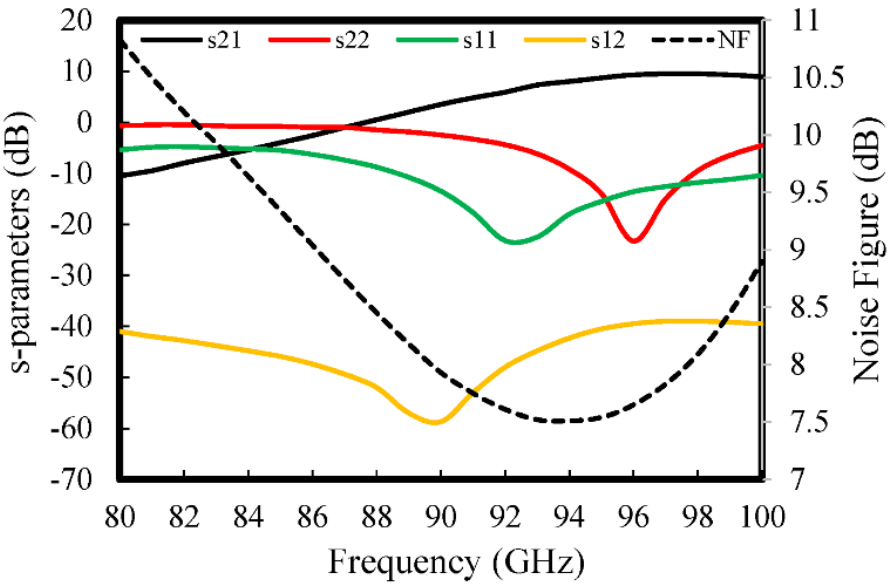


Fig. 5.18. Cadence Spectre simulation of PALNA small signal s-parameters and NF in the receive mode of operation. At 94 GHz, the s_{21} gain is 8 dB, the NF is 7.5 dB, and the circuit is stable.

Based on transient simulations, PALNA circuit can switch modes at rates up to 4 GHz, which is anticipated to be sufficient for most applications of interest.

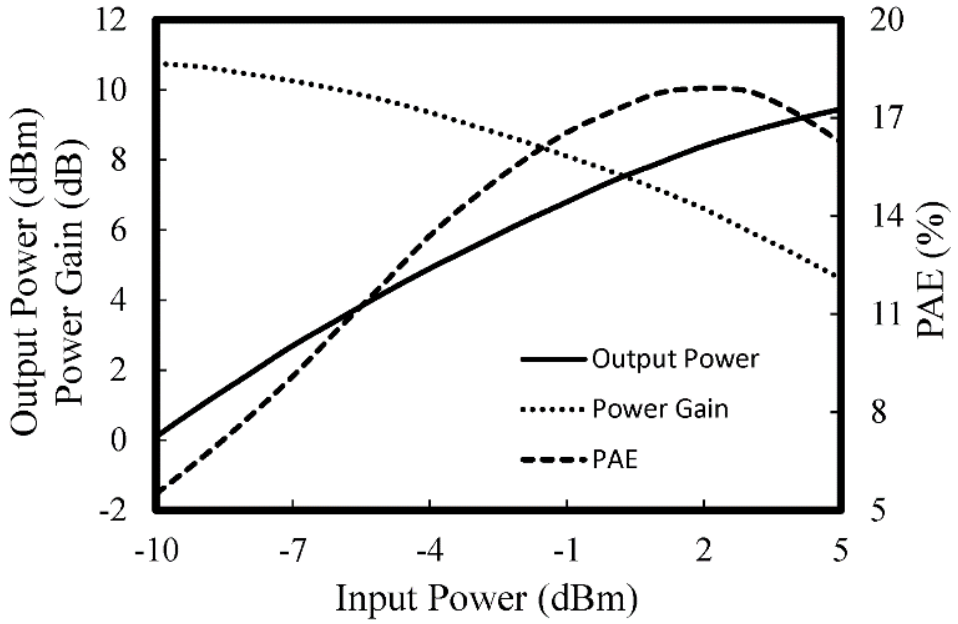


Fig. 5.19. Cadence Spectre simulation of PALNA P_{out}, Power Gain, and PAE in the transmit mode of operation at 94 GHz. P_{sat} exceeds 9 dBm and PAE reaches 18 %. Maximum Power Gain exceeds 10 dB.

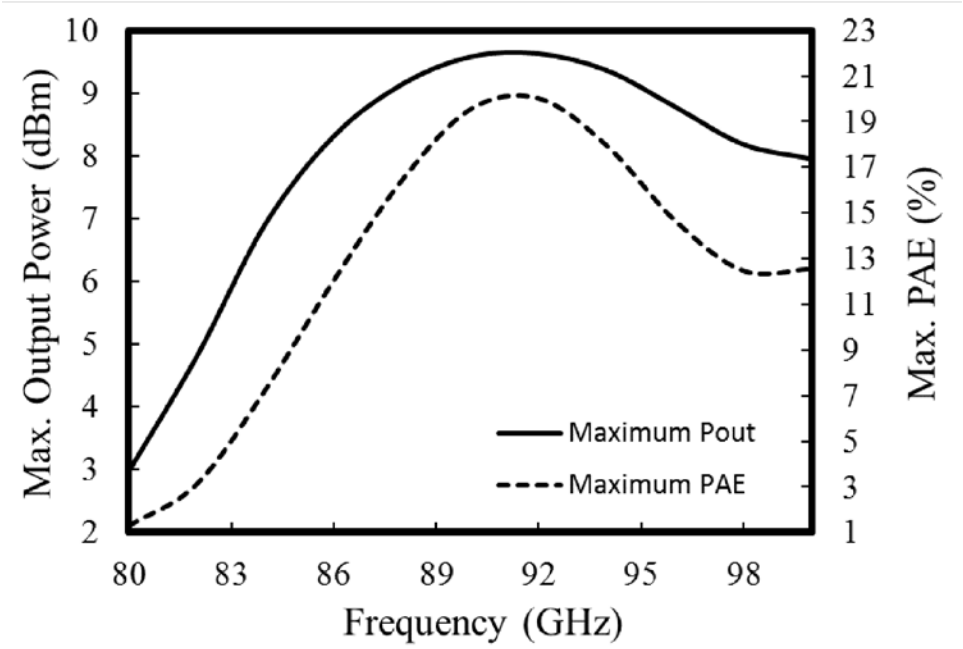


Fig. 5.20. Cadence Spectre simulation of PALNA transmit mode large signal performance as a function of frequency of operation. At its peak, around 92 GHz, Maximum PAE exceeds 20 %.

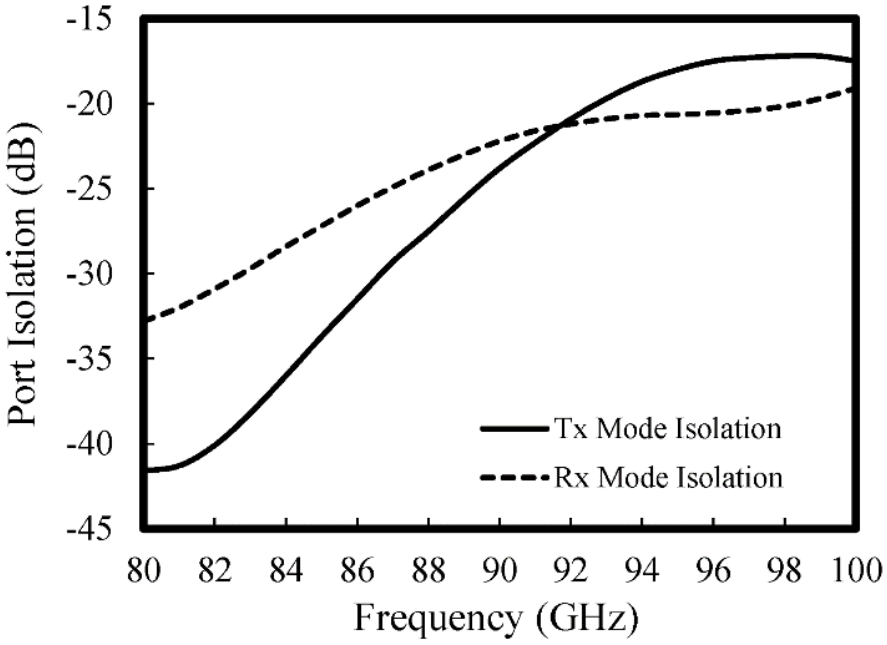


Fig. 5.21. Cadence Spectre simulations of PALNA port isolation. The transmit and receive port isolations at 94 GHz are 18.7 dB and >20 dB, respectively.

Table 5.7.
PALNA Performance Comparison.

	SoA [14]	**SoA [15]**	**Switch-based T/R, PA+LNA+SPDT* [1]**	**PALNA, this work**
Frequency [GHz]	94	79	94	94
Max Power Gain [dB]	-	-	> 10	> 10
Max PAE [%]	-	-	> 15	18
P_{sat} [dBm]	2	9.2	> 8	> 9
Receive Gain [dB]	-	-	8.8	8
NF [dB]	8.2	9	6.5	7.5

(*) Simulation is based on a measured 2.2 dB SPDT loss.

Table 5.7 shows the simulated performance comparison of the switchless PALNA circuit against two comparable state-of-art (SoA) circuits and a traditional, switch-based T/R circuit from Chapter 2 and from [1] that uses the same PA and LNA circuits as the switchless PALNA circuit. The performance of both the switch-based T/R circuit and the switchless PALNA was simulated using Cadence Spectre. The PA and the LNA in the switch-based T/R circuit have 50 Ω matching networks at the output and the input, respectively, because the switch has 50 Ω terminals.

Each signal path in the switch-based T/R circuit was simulated separately and the measured loss of the T/R switch was approximated by inserting a 50 Ω, 2.2 dB, resistive attenuator into each path [1]. The PALNA avoids the use of the 50 Ω matching networks at the antenna port and achieves performance advantage over the switch-based T/R circuit in transmit even though the PALNA loss in transmit is 2.6 dB and larger than the switch loss of 2.2 dB.

On the other hand, the switch-based T/R circuit from Chapter 2 is 40 % larger in terms of the required die layout area than the switchless PALNA circuit, which is a significant disadvantage. Fig. 5.22(a) shows the layout of the switchless PALNA circuit and Fig. 5.22(b) shows the layout of the comparable switch-based T/R circuit from Chapter 2.

PALNA bandwidth was not explicitly considered in the design methodology, but was inferred from the results in Fig. 5.18 and Fig. 5.20 and was considered sufficient for the system applications of interest. In particular, the 1 dB NF bandwidth is 12 GHz, extending from 87.5 GHz to 99.5 GHz, and the -5 % PAE bandwidth is 9 GHz, extending from 87 GHz to 96 GHz. Post-design sensitivity analysis, done by varying the length of the PA MN transmission line about its design value by +/- 20%, showed that the 1 dB NF bandwidth varies from 11 GHz to 13 GHz about the design value of 12 GHz. Based on this Rx mode performance alone, we would be driven to make the length of the PA MN transmission line as short as possible. However, by considering the Tx performance, we chose the design length of 226 μm, while sacrificing some LNA bandwidth performance. Bandwidth can also be formally included as an objective in the PALNA design methodology, at the expense of further nested iterative loops. To include bandwidth as a design goal, designers would first have to define a bandwidth metric in each mode of circuit operation. Then, with each iteration, bandwidth would have to be evaluated as one or more additional objective functions, which would influence the final PALNA solution.

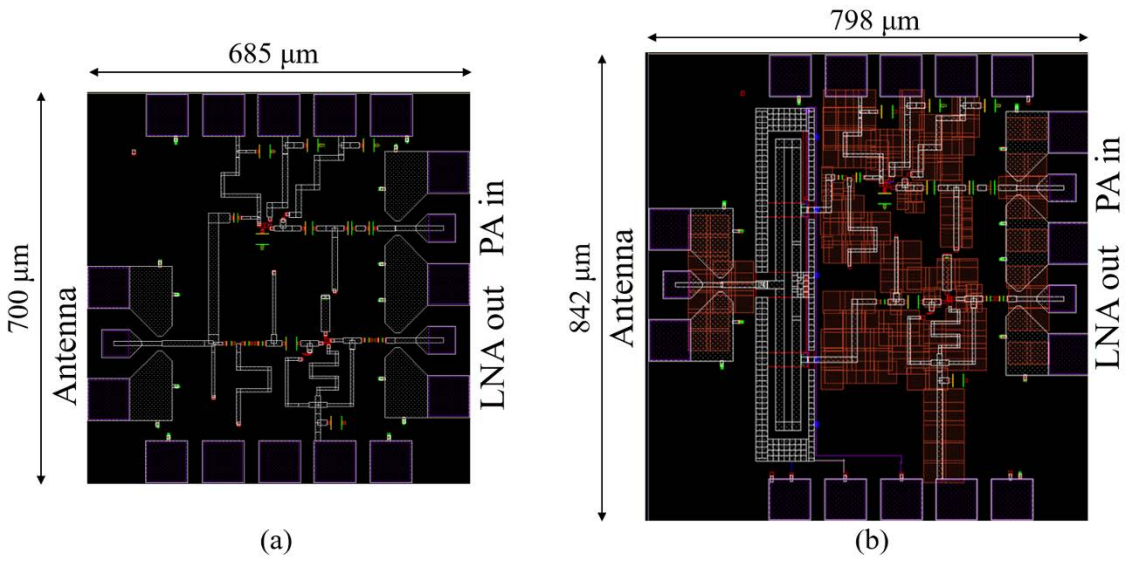


Fig. 5.22. Cadence layout photos of comparable T/R circuits: (a) switchless PALNA; (b) switch-based, traditional T/R circuit using the same PA and LNA circuits as the switchless PALNA. The layout photos are sized on the same relative scale, to illustrate the size advantage of the switchless PALNA circuit.

5.6 Experimental Results

Based on excellent simulated performance of the switchless PALNA T/R circuit presented above, the proposed PALNA T/R circuit was taped-out through TAPO and the chips were fabricated in the 32SOI technology. Fig. 5.23 shows the chip photograph of the PALNA T/R circuit. Probe station measurements of the chip were made and the small signal gain values, s_{21}, were found to be 8.5 dB and 16.9 dB smaller than the simulated values at 94 GHz in transmit and receive, respectively. Fig. 5.24 shows the photograph of the probe station and the test and measurement setup used at the ARL to make the chip measurements. The measurements were made using an Agilent Technologies performance network analyzer (PNA) with the front panel connections as shown in Fig. 5.25. Fig. 5.26 and Fig. 5.27 show the preliminary comparisons of small signal s-parameter simulated and measured results for the switchless PALNA T/R circuit in the transmit mode and the receive mode of operation, respectively. Table 5.8 shows the comparison of the simulated and the measured results for the switch-based T/R circuit, which was discussed in Chapter 2, and the switchless PALNA T/R circuit, which is discussed in this chapter.

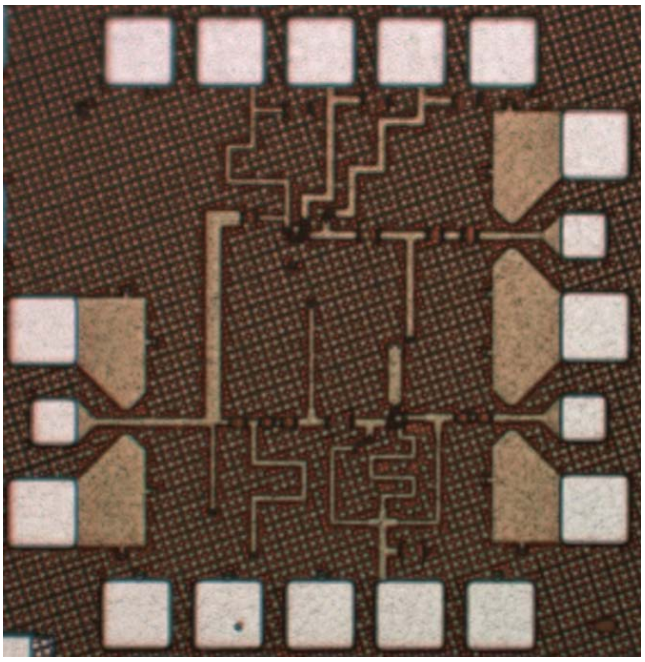


Fig. 5.23. Chip photograph of the PALNA circuit.

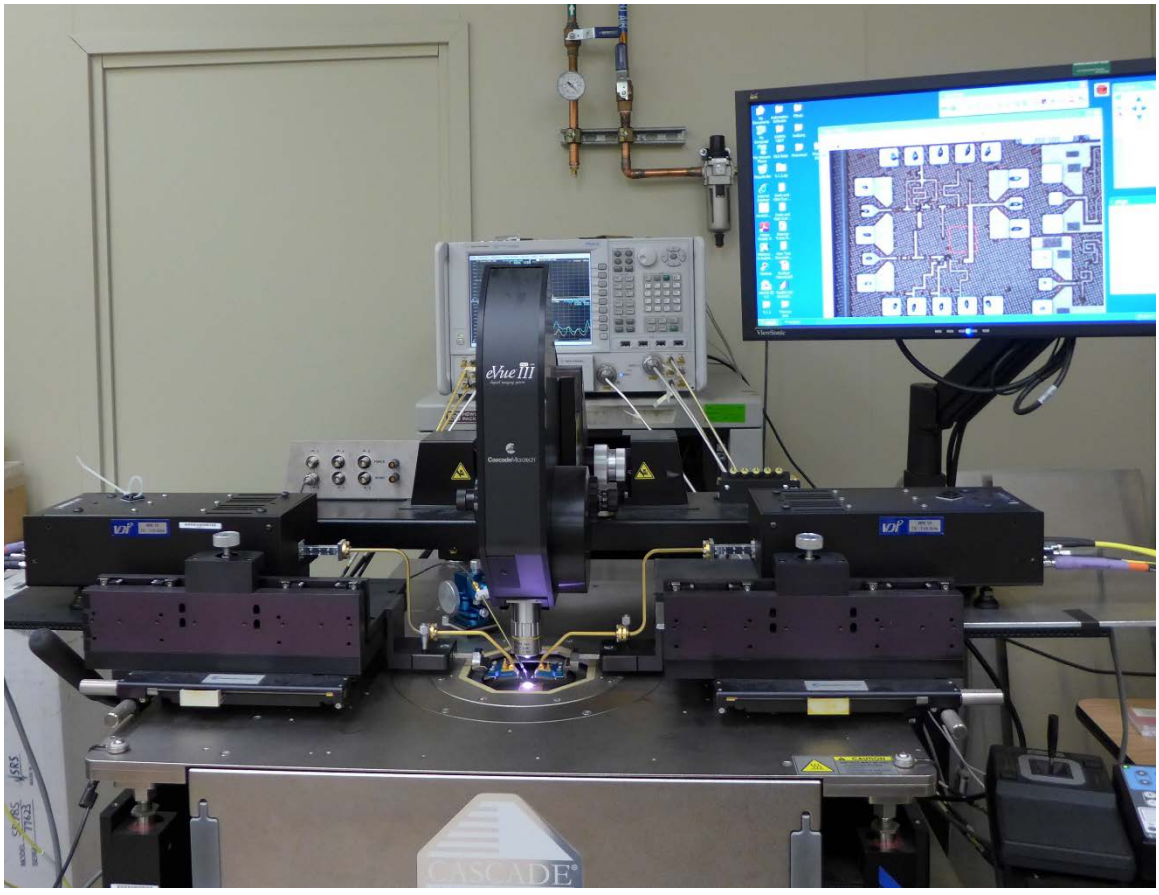


Fig. 5.24. Photograph of the ARL probe station and the test and measurement setup.

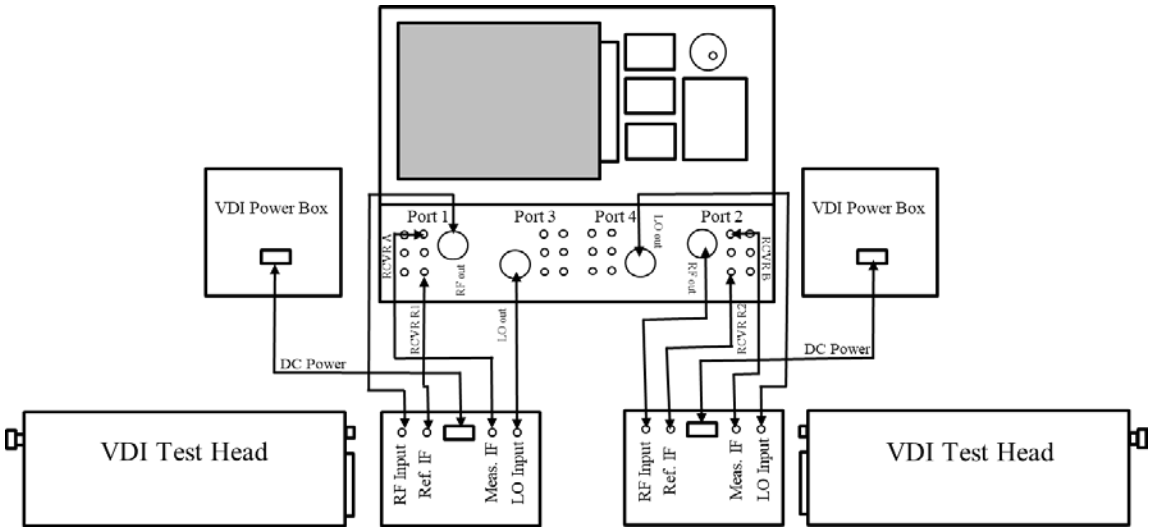


Fig. 5.25. Block diagram of the PNA front panel connections as used in the ARL test and measurement setup.

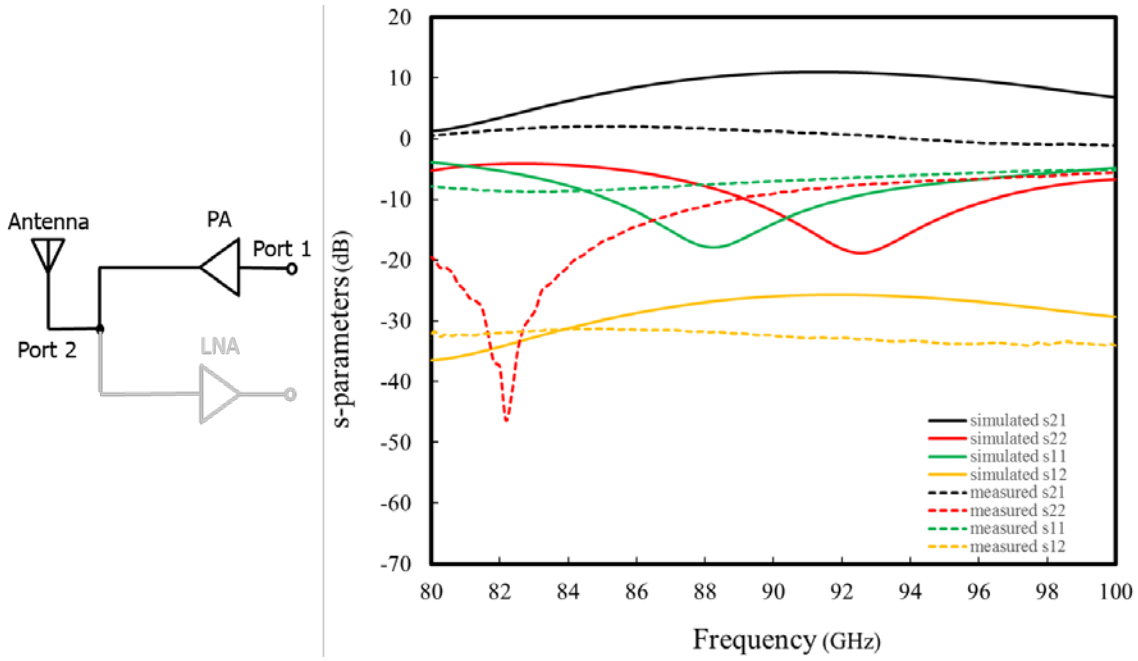


Fig. 5.26. 32SOI PALNA small signal s-parameters transmit mode preliminary results.

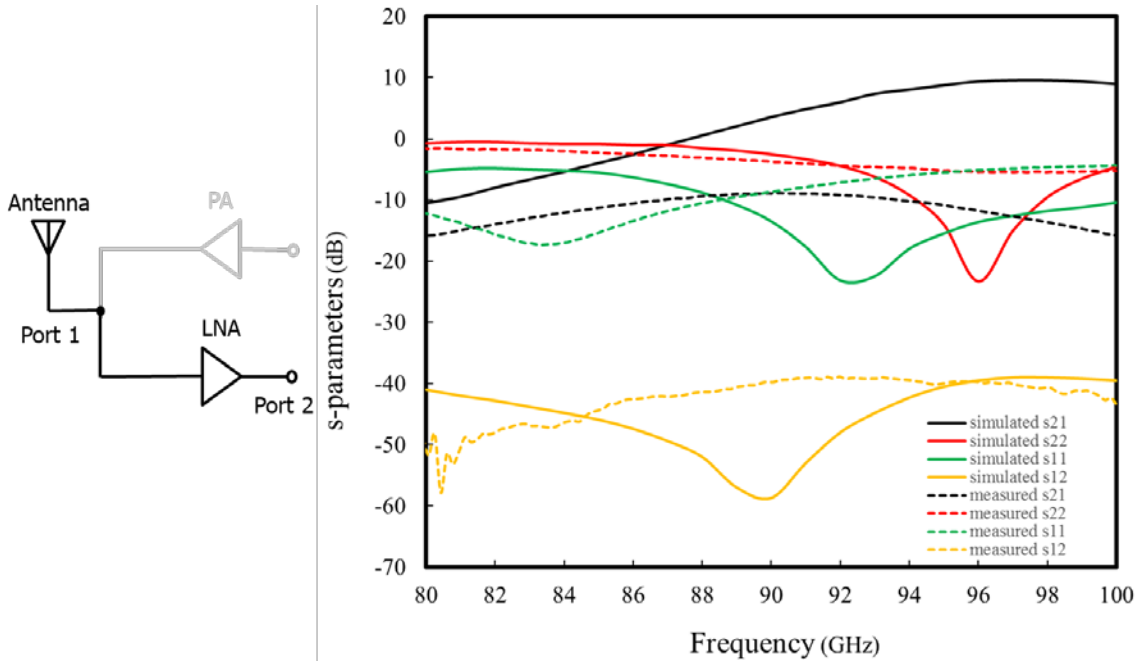


Fig. 5.27. 32SOI PALNA small signal s-parameters receive mode preliminary results.

A variety of operating bias conditions was investigated during the measurements and the best results obtained are presented above. SOLT calibration, leveraging the ARL calibration standard, was used to calibrate the ARL PNA measurement setup with reference planes up to, but not including, the chip GSG pads. Therefore, the GSG pads could not be calibrated out, which added ~1 dB of loss in each mode of operation.

In summary, the following degradations and discrepancies between the simulated and measured results are noted: (a) large drop in gain; (b) shift down in frequency. Just like in the case of the switch-based T/R circuit in Chapter 2, closer inspection of the chip revealed extensive presence of metal fill artifacts on metal layers LB, MA, and MB, which were inserted around and into the circuit transmission line structures during fabrication. Again, this was unexpected since fill had been excluded in those locations in layout. Subsequent EM simulations of the taped out circuit with the metal fill inserted have shown that the metal fill is a substantial, but not the only, cause of the above-mentioned degradations. The simulation effort to understand and reconcile the differences between the original simulated results and the measured results for the switchless PALNA circuit is described in detail below. Fig. 5.28 shows four photographs of the switch-based T/R circuit.

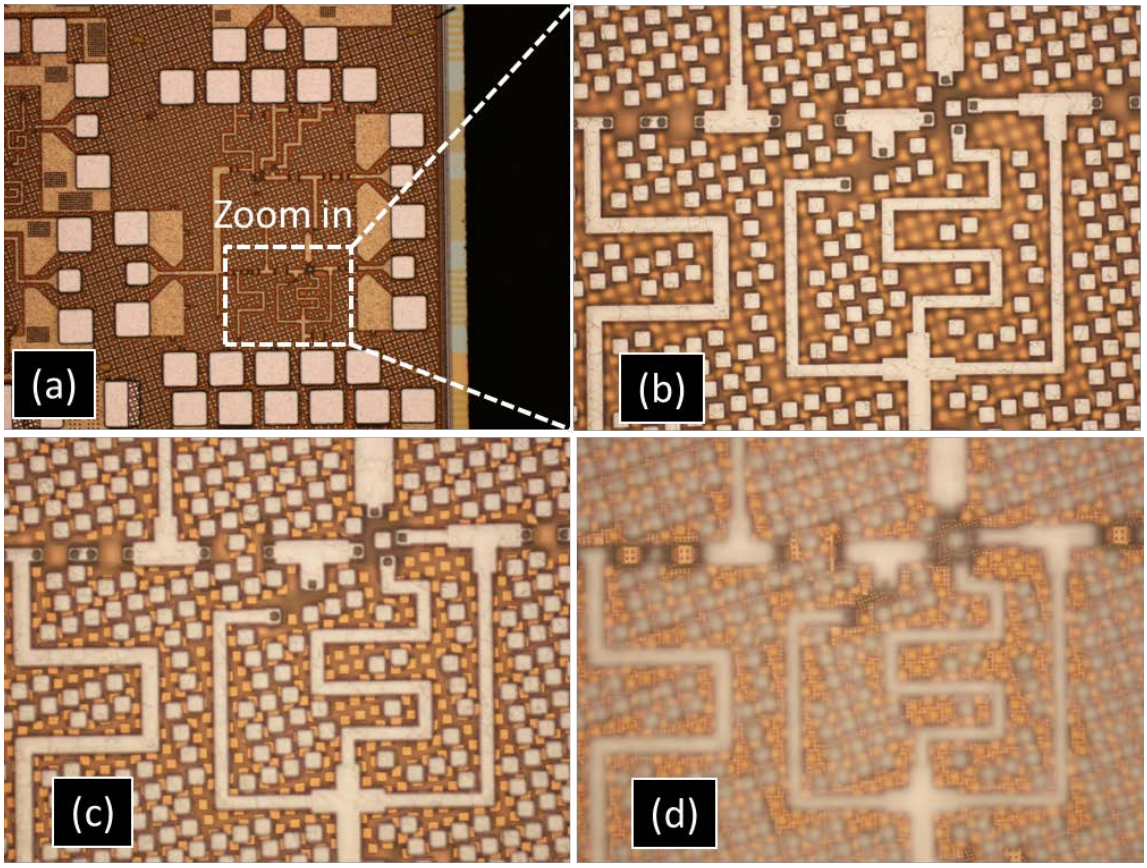


Fig. 5.28. Switchless PALNA T/R circuit chip photographs showing metal fill inserted during the 32SOI16A tapeout. (a) A circuit area is selected for zoom-in. (b) Top metal (LB) fill squares are seen to be very close to transmission lines. (c) MA layer, MB layer, or both metal fill squares are located under the transmission lines. (d) Focus adjustment reveals layer E1 ground plane ("fine mesh"), which is below the MA and MB layer fill squares.

Table 5.8.
Summary Comparison of the Simulated and the Measured Results for the Switch-based T/R Circuit from Chapter 2 and the Switchless PALNA T/R Circuit From This Chapter.

	PA+LNA+SPDT*	PALNA
Design Frequency [GHz]	94	94
Small signal Tx Gain [dB]	9.5 (simulated at 94 GHz) 0.7 (measured at 85.5 GHz)	10.5 (simulated at 94 GHz) 2 (measured at 85.5 GHz)
Tx power consumption [mW]	25.3 (11 mA at 2.3 V)	23.4 (9 mA at 2.6 V)
Small signal Rx Gain [dB]	9 (simulated at 94 GHz) 0.5 (measured at 96.2 GHz)	8 (simulated at 94 GHz) -8.9 (measured at 90.2 GHz)
Rx power consumption [mW]	12.6 (7 mA at 1.8 V)	7.5 (5 mA at 1.5 V)

(*) Simulation based on a measured 2.2 dB SPDT loss (updated based on switch measurements done after the PALNA circuit design)

In Fig. 5.28(a), a picture of the entire T\R chip is seen with an area designated by the white dashed boundary lines for camera zoom-in and further examination. In Fig. 5.28(b), the zoomed-in area of the chip is shown with the camera focused on the top metal layer where the circuit's microstrip transmission lines are located. It can be seen that there are numerous metal fill squares dispersed around the transmission lines, which is undesirable from the transmission line performance perspective since the metal fill was found to make transmission lines lossy [32] - [34]. Further, as can be seen in Fig. 5.28(c), the camera focus is adjusted to look beyond the top metal layer and numerous, smaller metal fill squares of dark yellow color are seen to be located under the transmission lines. And, even further, as can be seen in Fig. 5.28(d) with further adjustment of the camera focus to look deeper into the circuit, a fine 4-micron mesh appears, which is the intended ground plane for the circuit's transmission line structures. Therefore, it can be concluded that metal fill is present both around and directly inside the circuit's transmission line structures.

The discovery of this was very surprising since the metal fill was specifically excluded in the circuit layout, using specific metal-exclusion layers. However, given this understanding, the circuit simulation was updated, similar to what is shown in Fig. 2.19 above. In particular, per model described in [33], metal fill was added (first, second, and some third neighbors) around transmission lines, capacitors, and embedding networks. Additionally, since the GSG pads of the T/R circuit could not be calibrated out during the measurements, the GSG pads representative EM-simulated s-parameter model files were included in the circuit simulation. When the circuit model update was completed, the circuit was re-simulated in Cadence and the results are shown in Fig. 5.29 and Fig. 5.30. Fig. 5.29 and Fig. 5.30 show the comparison of the updated small signal s-parameter simulation results and the measured results in the transmit mode and the receive mode, respectively. As can be seen, the updated simulation accounted for a substantial amount of gain loss. However, the addition of metal fill and the GSG pads did not fully account for the frequency downshift and all the gain loss observed in the measurements. This appears to be consistent across all three the 32SOI designs presented in this dissertation and it is also consistent with measurements of the single-stage LNA circuit done at UCSD, which is discussed in Chapter 3. Since the simulation including the effects of the metal fill and GSG

pads was based on thorough EM-based modelling in Sonnet, which is known to be accurate in comparison to measurements, the source of these degradations is most likely attributable to the inaccurate device models used in the designs. In particular, the parasitic extraction tools used, which are known to be less accurate than the EM-based simulators, likely didn't quite capture the device parasitics accurately enough, during the process of parasitic extraction. Thus, with the devices slightly more capacitive than the tool predicted, the peak frequency would be smaller than simulated and the gain would likely be reduced because of the resulting impedance mismatch. Therefore, an important lesson learned from the tapeouts done is that RF designers must design with device models that not only contain estimated parasitics, but with device models that are validated against measured data at same bias levels. Best yet, if possible, designers should design with measured s-parameter files, measured at the correct bias levels, that are representative of all devices used in the design (see section 7.3).

Aside from the frequency downshift and loss apparent in s_{21} in both transmit and receive, s_{12} also appears to have undergone a frequency downshift of similar magnitude in both modes of operation. In receive, measured parameters s_{11} and s_{22} actually show < 4 dB difference from the simulated values across the entire frequency range, from 80 GHz to 100 GHz, which represents a good agreement between measurement and simulation. In transmit, measured parameters s_{11} and s_{22} are also reasonably close to the simulated values across most of the frequency range, except from 80 GHz to 85 GHz where measured values of s_{22} differ substantially from the simulated values.

Given the above-discussed degradations seen in measured performance of small signal s-parameters, s_{21} in particular, noise figure and large signal measurements were not attempted.

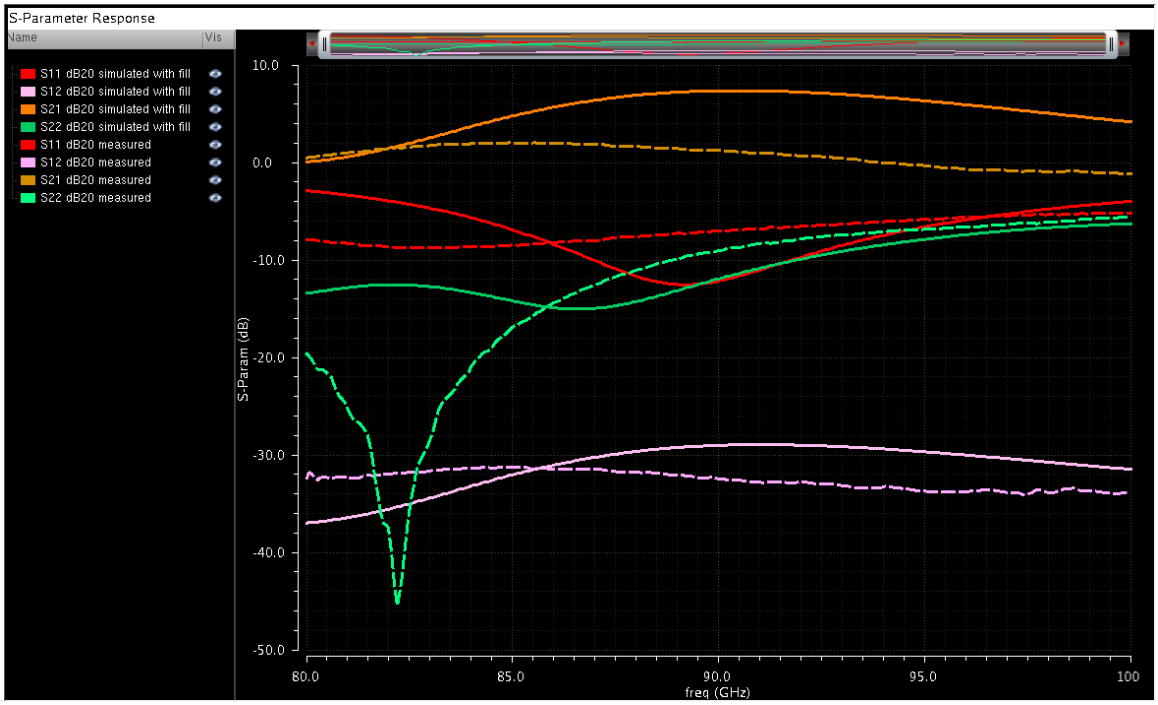


Fig. 5.29. Comparison of updated small signal s-parameter simulation results and measured results in the transmit mode of operation.

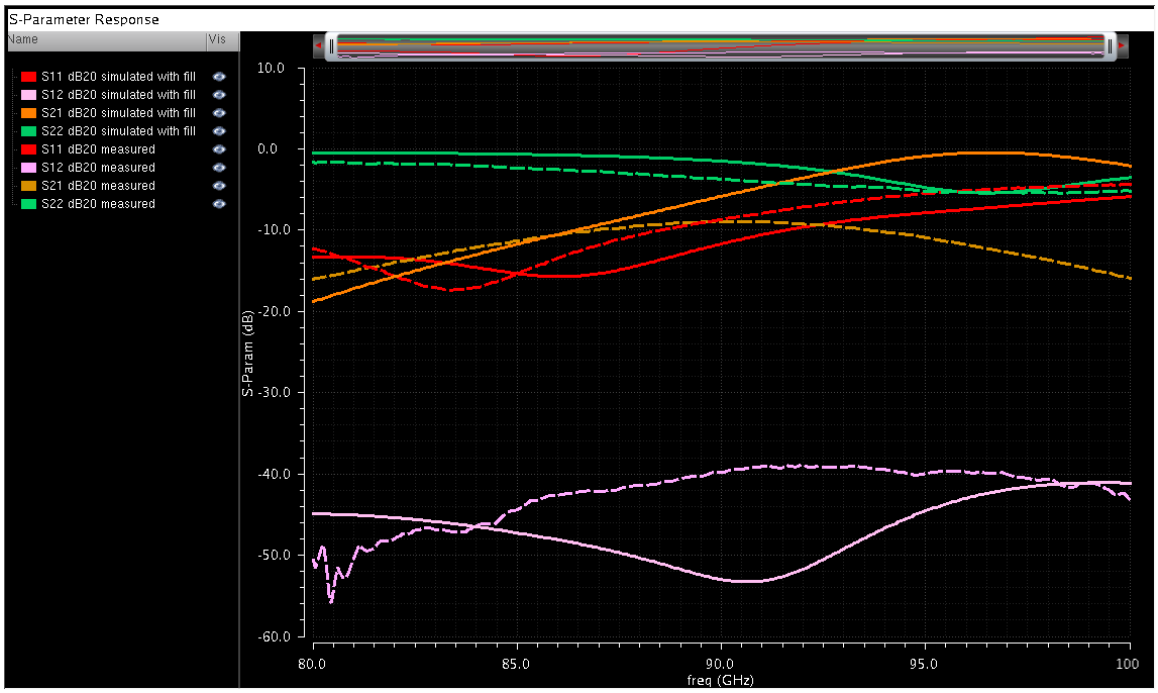


Fig. 5.30. Comparison of updated small signal s-parameter simulation results and measured results in the receive mode of operation.

5.7 Summary

This chapter provides a loss-aware methodology for analysis and design of switchless PALNA T/R integrated circuits suitable for use in emerging millimeter wave phased arrays. The methodology is a practical, iterative, generally applicable approach for solving the multi-variable optimization problem of developing a PALNA matching network, which presents optimal matching impedances to both the PA and the LNA while minimizing dissipative and mismatch losses in transmit and receive modes of operation. The methodology may be applied for PALNA designs in any integrated circuit fabrication technology and at any frequency of operation, to reduce the size of T/R circuits or improve their performance as compared to equivalent switch-based or circulator-based designs. For comparison purposes, two practical 94 GHz integrated T/R circuits were designed in 32SOI technology, a T/R circuit with a SPDT switch that is discussed in Chapter 2 and a switchless PALNA that is discussed in this chapter. The switch-based T/R circuit is ~40% physically larger than the switchless PALNA, and the PALNA demonstrates comparable or improved performance in parameters of interest such as PAE.

As discussed above in detail, the measured results of the PALNA differed substantially from the simulated values, s_{21} parameter in particular, even after the loss-inducing metal fill was added to the PALNA circuit simulation. Even though the metal fill addition accounted for a large amount of the observed loss, it did not account for all of the loss and for the notable s_{21} frequency downshift. Since the fill simulation is based on accurate EM component models, it is trusted, and the remaining s_{21} loss and frequency downshift is likely attributable to the less than accurate device models used in the simulations, which are based on less than accurate parasitic extraction process. Therefore, an important lesson learned from the tapeouts presented in this dissertation is that RF designers should design with device models that are either validated against measured data, at same bias levels, or with measured s-parameter files that are representative of the devices used in the design, at the same bias levels (see section 7.3).

Chapter Six: **PALNA Design for Improved Bandwidth Performance**

6.1 Enhanced Bandwidth PALNA Design Methodology

As was discussed in the previous chapter, PALNA matching networks (MNs) can be designed using lossy components to provide good simultaneous impedance match in both the transmit and the receive mode of operation, albeit with component loss translating into PALNA MN loss and the corresponding PAE and NF degradations. However, what is the fundamental, theoretical limitation on bandwidth performance of the PALNA matching network? What is the impact on bandwidth performance if a finite number of lossy components is used to design the PALNA and how close to the theoretical performance limits is it possible to get in practice? How can the PALNA design methodology presented in Fig. 5.3 be updated to become suitable for designing PALNAs with an optimal tradeoff between bandwidth performance and transducer loss performance?

In order to answer these questions, the following four objectives are accomplished in this

chapter:

1. PALNA bandwidth is defined
2. PALNA bandwidth theoretical performance limits are calculated and practical PALNA design goal is established
3. PALNA design approach is developed
4. PALNA design approach is implemented and simulation studies are conducted on numerous PALNA topologies to find the best answers to the above stated questions

The first three of these objectives are accomplished in this section. The fourth objective is accomplished in sections 6.2 – 6.4. Section 6.2 of this chapter summarizes the results of the nested search procedure applied to the three PALNA topologies presented in Chapter 5 plus five additional PALNA topologies that are candidates for improved reflection coefficient performance over frequency. As in Chapter 5, the nested search procedure is implemented in MATLAB and lossy component models are used. Section 6.3 summarizes the results of the iterated PALNA MN development in Cadence using EM modelled PALNA MN components. Section 6.4 summarizes the simulation results of the fully integrated example PALNA in Cadence including the PA and the LNA cells from Chapter 5. Section 6.5 provides the summary and a discussion of the results.

6.1.1 PALNA Bandwidth Definition

Since the basic function of a PALNA MN is to serve as a transmit/receive simultaneous impedance matching network, PALNA MN bandwidth can be formulated and studied in the context of the Bode-Fano criterion [44]. If the PALNA MN performance was ideal and the antenna port was disconnected, impedance Z_A looking into the PALNA MN would equal the complex conjugate of the antenna impedance in both modes of operation (see Fig. 1.5). Similarly, if the PA was disconnected in the transmit mode of operation, impedance Z_L looking into the PALNA MN would equal the PA optimal impedance Z_{PA_OPT} (see Fig. 1.5). And, if the LNA was disconnected in the receive mode of operation, impedance Z_S looking into the PALNA MN would equal the LNA optimal impedance Z_{LNA_OPT} (see Fig. 1.5). Fig. 6.1 shows the transmit mode and the receive mode

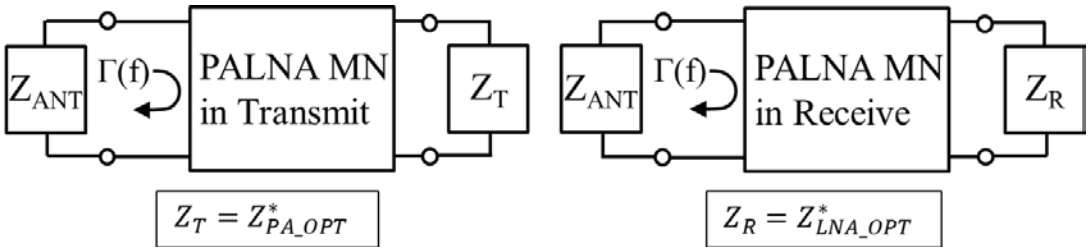


Fig. 6.1. A representation of PALNA MN functionality suitable for definition and analysis of PALNA bandwidth performance in the context of the Bode-Fano criterion. (a) PALNA representation in transmit mode of operation. (b) PALNA representation in receive mode of operation.

representations of the PALNA MN functionality with Z_{ANT} representing an arbitrary antenna impedance. Therefore, if impedances Z_T and Z_R are defined as in (6.1) and (6.2),

$$Z_T = Z^*_{PA\_OPT} \tag{6.1}$$

$$Z_R = Z^*_{LNA\_OPT} \tag{6.2}$$

the PALNA MN functionality can be viewed as a more traditional, maximum power transfer impedance matching problem, as shown in Fig. 6.1, suitable for study in the Bode-Fano context.

Using the PALNA MN functionality representation shown in Fig. 6.1, PALNA bandwidth can be defined in terms of the reflection coefficient seen at the antenna in each mode of PALNA operation. As shown in Fig. 6.2, the PALNA design goal is to achieve as small a reflection coefficient magnitude as possible $|\Gamma(f)| \leq \Gamma_{min}$ over a specified bandwidth Δf [44]. Assuming the shape of $|\Gamma(f)|$ as shown in Fig. 6.2, PALNA bandwidth can be mathematically defined as

$$\Delta f \stackrel{\text{def}}{=} \{f \in F \mid |\Gamma(f)| \leq \Gamma_{min}\} \tag{6.3}$$

where F is the set of all frequencies and $\Gamma_{min} > 0$.

It should be noted that, since the Bode-Fano impedance matching criterion is defined in

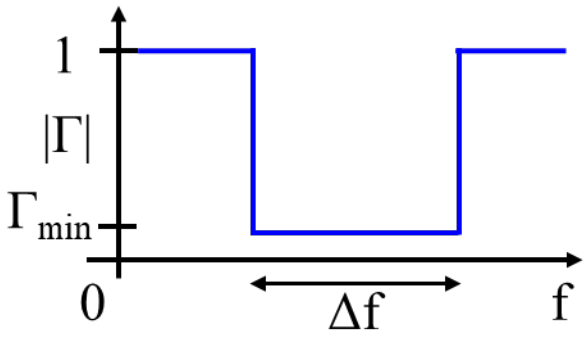


Fig. 6.2. Desired response of the reflection coefficient Γ(f) seen at the antenna of impedance Z_{ANT} in each mode of PALNA operation. The PALNA design goal is to achieve a small reflection coefficient magnitude $|\Gamma(f)| \leq \Gamma_{min}$ over a specified bandwidth Δf.

terms of the reflection coefficient Γ(f) at the antenna port, no specific antenna impedance needs to be assumed in general. However, in the following sections of this chapter where specific PALNA designs are explored, the antenna is assumed to have a 50 Ω impedance across all frequencies of interest. This assumption is made without the loss of generality and it is consistent with the antenna assumptions made in the preceding chapters of this text.

6.1.2 PALNA Theoretical Bandwidth Performance Limits and Design Goal

Given the PALNA bandwidth definition developed in the previous sub-section, the theoretical limit on bandwidth performance of the PALNA MN can be established using the Bode-Fano criterion. In particular, the best possible impedance match can be quantitatively expressed as a function of given frequency bandwidth. This is generally useful because it allows consideration of tradeoffs between the quality of impedance match and bandwidth over which the impedance match can be achieved in theory. The Bode-Fano criterion theory assumes the availability of an infinite number of lossless components (i.e., capacitors, inductors, transmission lines, etc.) with which a PALNA MN can be constructed. Therefore, the theory yields an ideal performance goal that can only be approximated with practical PALNA designs. In practice however, due to substantial losses

associated with realistic passive components at mm-Wave frequencies, only a limited number of components may be used in PALNA designs to achieve multiple performance goals. So, the PALNA MN design process entails selection of PALNA MN topology and complexity to achieve an acceptably low reflection coefficient over a specified bandwidth. In this sub-section, the theoretical limits of lossless PALNA MN bandwidth performance are considered first. Then, second, a design benchmark is introduced, which is frequently used in practice and is suitable for evaluating the performance of practical matching networks. Third, a design approach is developed that is suitable for loss-aware design of PALNAs with a specified reflection coefficient performance over a given bandwidth. Fourth, in sections 6.2 – 6.4, the design approach is leveraged to investigate feasibility of PALNA MNs that cover the entire W-band, from 75 GHz to 110 GHz. A variety of PALNA MN topologies are investigated for increasing the bandwidth, including lumped-element PALNA MNs of various complexities, the use of multisection matching transformers as PA MN, and the use of short-step-stub transformers as PA MN, while maintaining all the other desirable properties of PALNAs such as simultaneous impedance matching and minimal loss in both modes of operation. It is assumed that wideband PA and LNA cells are available and that their optimum impedance matching conditions are constant over the frequency range of interest. This is a realistic assumption consistent with standard wideband amplifier design practices and the focus of this chapter is on passive PALNA MNs only [47].

If $Z_{PA\_OPT} = 90 + j10\ \Omega$ and $Z_{LNA\_OPT} = 150 + j25\ \Omega$ as established in Chapter 5 at 94 GHz, both Z_T and Z_R defined in (6.1) and (6.2) have the general form R – jX, where the negative reactance can be realized using a capacitor since $X_C = -j(1/2\pi fC)$. Impedances Z_T and Z_R can then both be realized as a series RC circuit and, according to the Bode-Fano criterion [44]

$$\int_0^\infty \ln\frac{1}{|\Gamma(\omega)|}\,d\omega < \pi\omega_0^2 RC \tag{6.4}$$

Assuming a PALNA matching network with a reflection coefficient response as shown in

Fig. 6.2, applying (6.4) gives [44]

$$\Delta\omega \ln\frac{1}{\Gamma_{min}} < \pi\omega_0^2 RC \tag{6.5}$$

and since ω=2πf,

$$\Delta f \ln\frac{1}{\Gamma_{min}} < 2\pi^2 f_0^2 RC \tag{6.6}$$

Using Δf = 110 GHz – 75 GHz = 35 GHz and f_0 = 92.5 GHz as the bandwidth of interest and the center of the bandwidth, respectively, and applying (6.6) gives

$$\frac{1}{\Gamma_{min}} < e^{75.1} \tag{6.7}$$

for transmit mode PALNA MN and

$$\frac{1}{\Gamma_{min}} < e^{50.1} \tag{6.8}$$

for receive mode PALNA MN.

The minimum theoretically achievable reflection coefficients Γ_{min} from 75 GHz to 110 GHz calculated in (6.7) and (6.8) for both modes of operation are extremely small. These performance limits were calculated under the assumption of a PALNA MN constructed using an infinite number of lossless elements and thus represent an ideal result that may only be approximated in practice. Also, conceptually, since the resistance part of the impedance looking away from the antenna is assumed to vanish outside of the useful bandwidth of the PALNA, the performance limits calculated in (6.7) and (6.8) depend on the defined fractional bandwidth of the PALNA [48]. In particular, the exponent values shown in (6.7) and (6.8) are inversely proportional to the defined PALNA fractional

bandwidth, which equals ($\Delta f / f_0$) x 100% = (35 GHz / 92.5 GHz) x 100% = 38 % in both modes of PALNA operation. If, for example, the PALNA fractional bandwidth was defined to be the maximum 200 %, the exponent values in (6.7) and (6.8) would be 14.2 and 9.5, respectively. However, these results are important in quantifying the upper limit of performance, an ideal benchmark presented for context, comparison, and completeness purposes against practical PALNA designs. In practice, components are lossy and an infinite number of components is not available, thus another benchmark used frequently is considered, which requires that the antenna return loss is greater than 10 dB. Since [44]

$$\text{Return Loss} \stackrel{\text{def}}{=} -20 \log|\Gamma| \tag{6.9}$$

using the 10 dB goal in combination with (6.9) yields

$$|\Gamma| < 0.316 \tag{6.10}$$

As a practical performance goal, the reflection coefficient value calculated in (6.10) is significantly less stringent than the theoretical limits calculated in (6.7) and (6.8). However, the goal in (6.10) is realistic and achievable in practice whereas the goals in (6.7) and (6.8) are not.

6.1.3 Broadband PALNA Design Methodology

The starting point of an approach suitable for loss aware design of PALNAs that have a specified reflection coefficient performance over a given bandwidth is the design approach summarized in Fig. 5.3. All of the PALNA design aspects discussed in Chapter 5 and summarized in Fig. 5.3 are also applicable to the design approach considered in this sub-section. In addition here, Step 1 and Step 2 of the approach from Fig. 5.3 are updated to add design tasks that account for the PALNA reflection coefficient performance over frequency. Fig. 6.3 shows the flow chart of the updated PALNA design approach with the added design tasks highlighted in yellow. Specifically, in Step 1, the MATLAB nested search scripts were updated to calculate a bandwidth metric in each mode of operation for

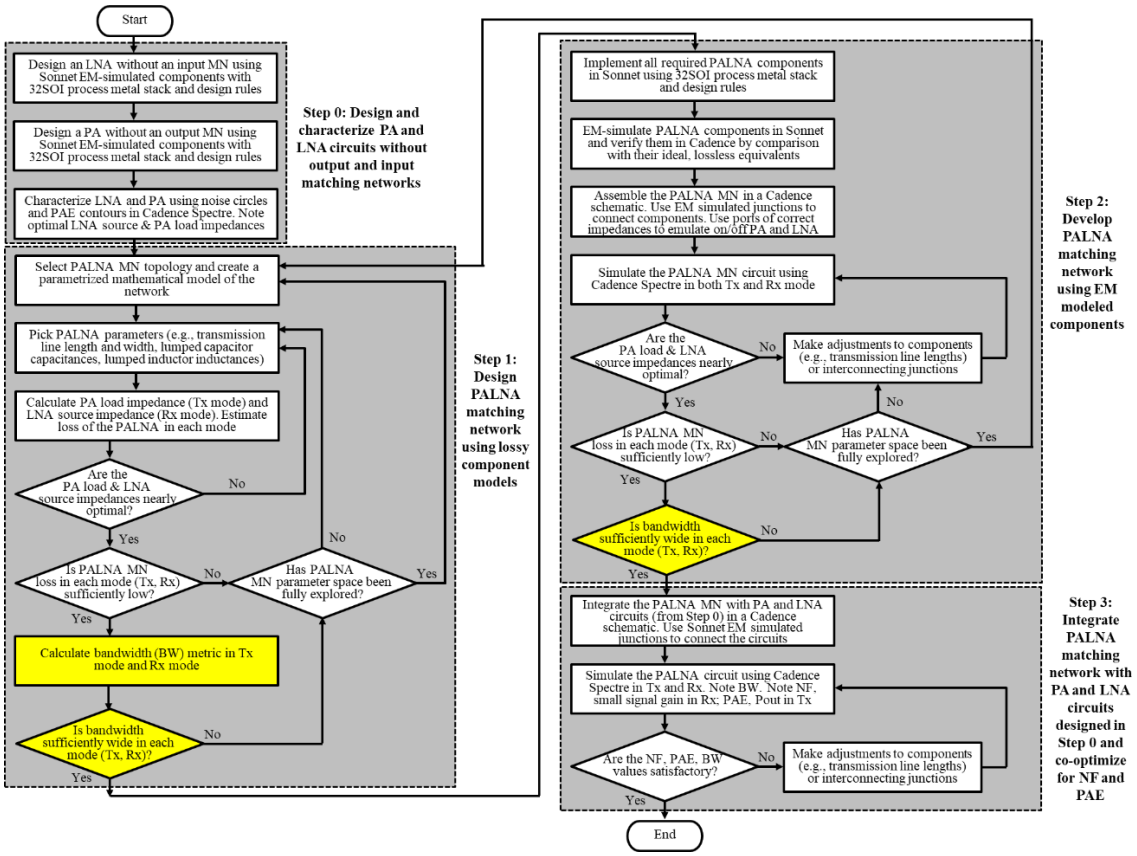


Fig. 6.3. PALNA design methodology flowchart including the additional design steps (highlighted in yellow) for improved bandwidth performance.

each candidate PALNA solution. The bandwidth metric is then considered, in addition to impedance matching and transducer loss performance, in the process of selecting the optimal PALNA solution. Similarly, in Step 2, the reflection coefficient performance over frequency is simulated in Cadence and considered in each step of the iterative PALNA design process.

6.2 PALNA MN Design in MATLAB Using Lossy Component Models (Step 1)

The goal of this section is to twofold: (1) to study the bandwidth performance of the three

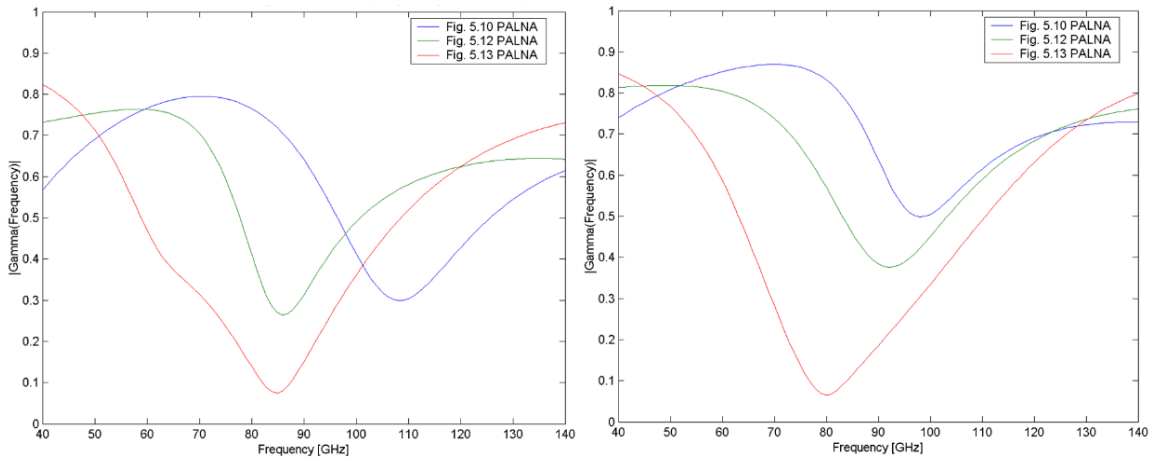
PALNA topologies presented in Chapter 5, and to explore the bandwidth performance limits of the topology which performs the best; and (2) to study the overall performance of five alternative PALNA topologies, which promise to extend the bandwidth beyond what is achievable with the PALNA topologies studied in Chapter 5.

6.2.1 Bandwidth Performance of PALNAs From Chapter 5

First, it should be noted that, for the purposes of studying the PALNA MN bandwidth performance in the context of the Bode-Fano criterion, the PALNA MN representation described above and shown in Fig. 6.1 is not constrained by the direction of signal propagation (i.e., away from the antenna and into the PALNA MN for transmit versus away from the PALNA MN and into the antenna for receive). In general, the Bode-Fano criterion is formulated in terms of the reflection coefficient magnitude at the antenna [44]. And, for a given mode of PALNA operation, the magnitude of the reflection coefficient looking into the antenna is equal to the magnitude of the reflection coefficient looking away from the antenna. Second, since a 50 Ω antenna was assumed for the PALNA designs in Chapter 5, it is also assumed here that the antenna has a 50 Ω input impedance over the frequency range of interest.

So, in order to establish an initial bandwidth performance baseline, antenna reflection coefficient magnitude versus frequency was plotted using MATLAB for the three lossy PALNAs from Chapter 5, as shown in Fig. 6.4 for both modes of circuit operation. With regard to the goals of having the antenna reflection coefficient magnitudes best approach the above calculated Bode-Fano limits or be better than 0.316 from 75 GHz to 110 GHz, the PALNA topology from Fig. 5.13 clearly shows the most promise and was chosen for further study. The other two topologies were dropped from consideration at this point.

When the Fig. 5.13 PALNA circuit had been designed in Chapter 5, its solution space in MATLAB consisted of 46 different PALNA circuits, with each circuit meeting the



(a) (b)

Fig. 6.4. Comparison of the lossy PALNAs from Chapter 5. Antenna reflection coefficient magnitude versus frequency is shown in: (a) the transmit mode; (b) the receive mode.

impedance matching goals and having low loss in both modes of operation. So, each of these 46 solutions was revisited from the perspective of bandwidth performance. Fig. 6.5 shows the antenna reflection coefficient magnitude versus frequency for all 46 available solutions of the lossless Fig. 5.13 PALNA in both modes of operation. In order to compare these solutions in terms of bandwidth, it is necessary to define a bandwidth performance metric consistent with the PALNA bandwidth design goals described above.

Since the PALNA design goal is to achieve as small a reflection coefficient $|\Gamma(f)|$ magnitude as possible over a specified bandwidth Δf, PALNA bandwidth metric was defined as the area under the reflection coefficient curve, from 75 GHz to 110 GHz, as shown with light blue color shading in Fig. 6.6. The bandwidth metric is calculated separately in both transmit and receive and the PALNA design goal is to minimize the metric in both modes of operation. Mathematically, the shaded area is represented and estimated as shown in (6.11), and the PALNA bandwidth metric is computed in MATLAB as the sum, from 75 GHz to 110 GHz, with $\Delta f = 1$ GHz increments. The bandwidth metric units are GHz. The $\Delta f = 1$ GHz increments were found, through simulation experimentation, to be both sufficiently fine for bandwidth performance comparisons and manageable from the computational efficiency point of view.

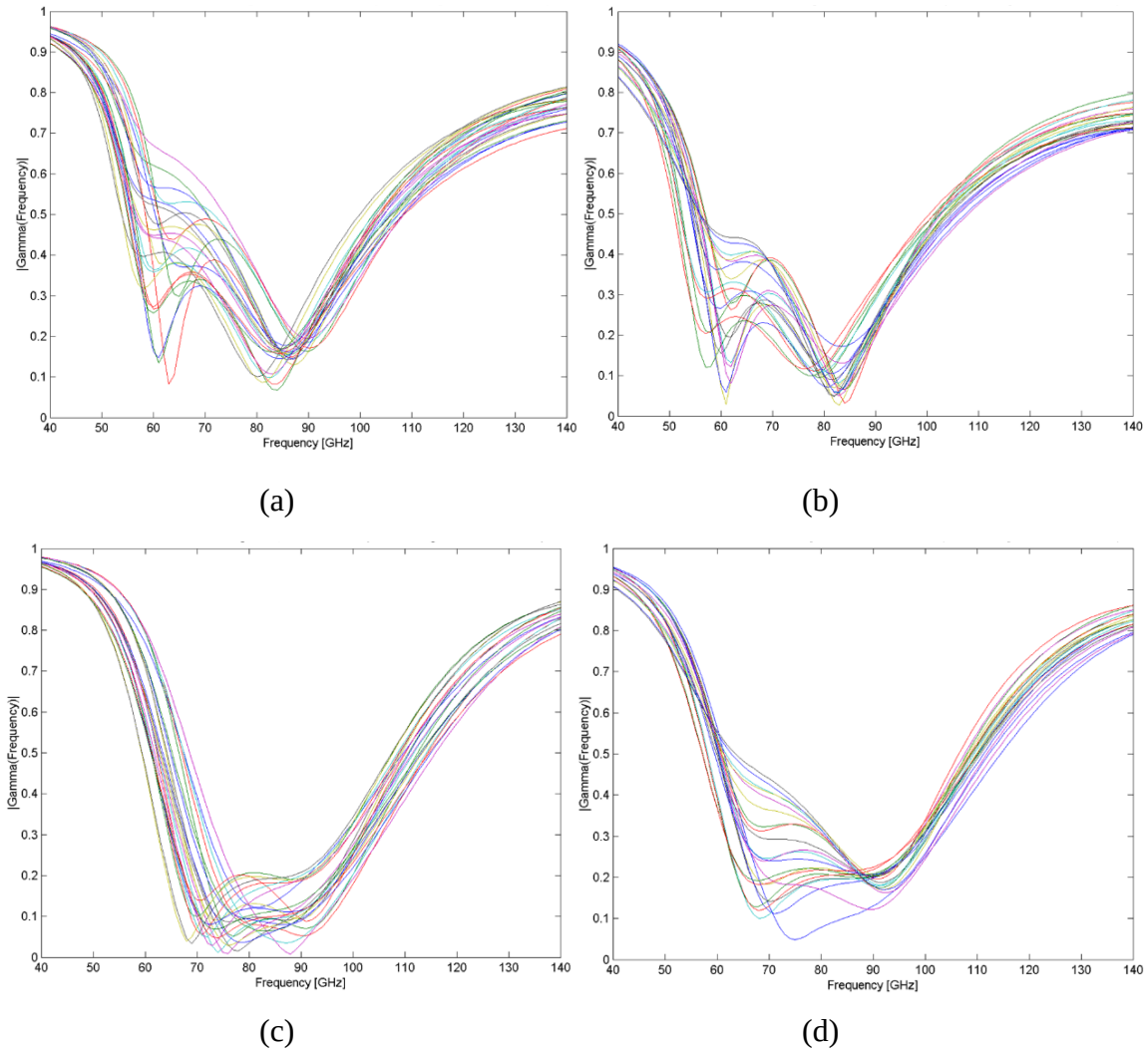


Fig. 6.5. Bandwidth performance of lossless PALNA from Fig. 5.13. Antenna reflection coefficient magnitude versus frequency is shown for: (a) solutions 1-24 in the transmit mode; (b) solutions 25-46 in the transmit mode; (c) solutions 1-24 in the receive mode; (d) solutions 25-46 in the receive mode.

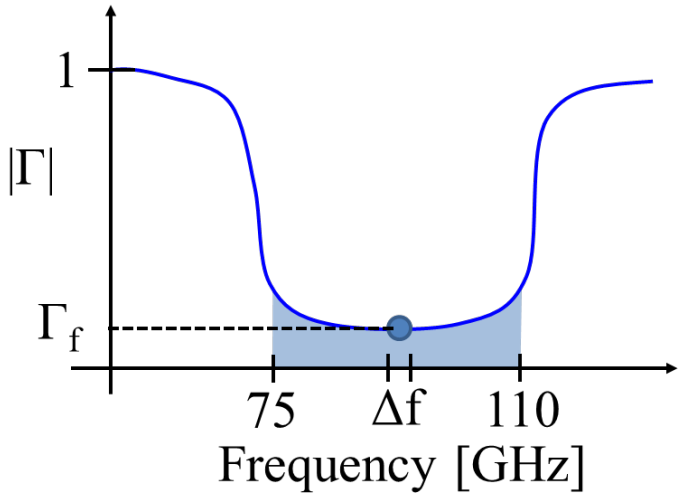
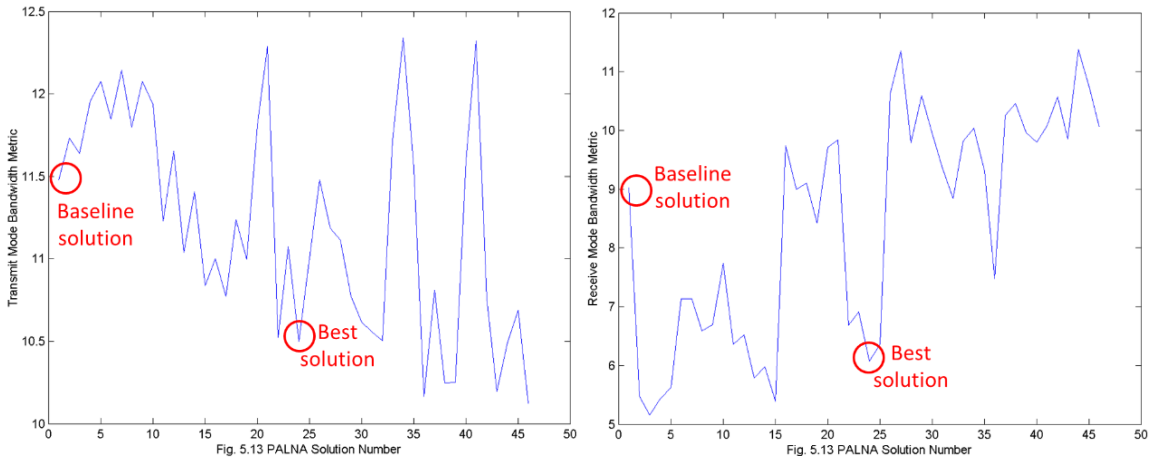


Fig. 6.6. PALNA bandwidth metric in GHz is defined as an estimate of the shaded area under the reflection coefficient curve, from 75 GHz to 110 GHz, which is calculated separately in both transmit and receive. The design goal is to minimize the metric in both modes of operation.

$$PALNA\ Bandwidth\ Metric = \int_{75}^{110} |\Gamma(f)| df \sim \sum_{75}^{110} \Gamma_f \Delta f \tag{6.11}$$

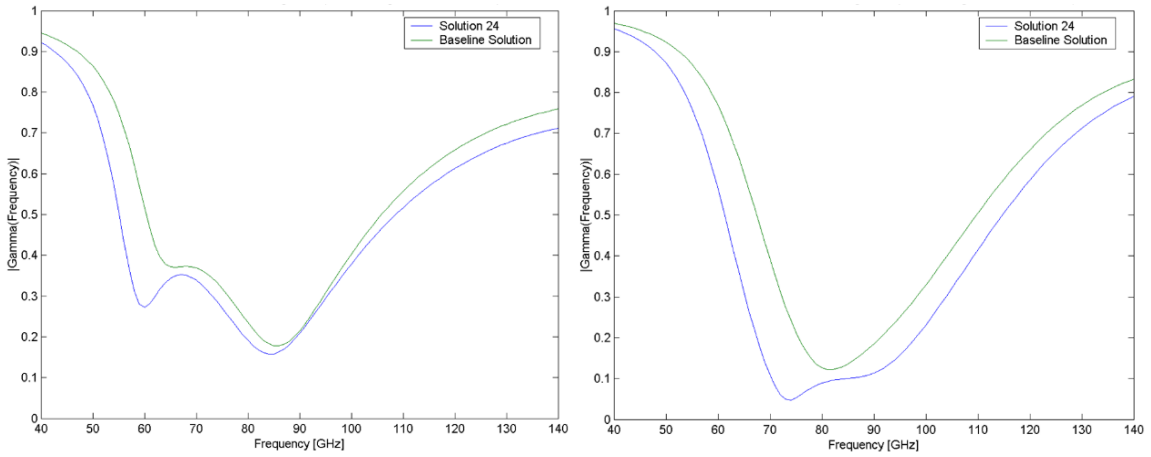
After the bandwidth performance metric was defined, the metric was computed for the 46 solutions of the Fig. 5.13 PALNA in both modes of operation. Fig. 6.7 shows the summary of the bandwidth metric computation results. Solution #1 is the baseline solution presented in Chapter 5 and the Solution #24 represents the best bandwidth performance compromise solution between the transmit mode and receive mode, of the 46 solutions available. It is noted that Solution #24 represents bandwidth performance improvement over the baseline solution in both modes of PALNA operation.

The impedance matching performance of Solution # 24 is good at 94 GHz, near the center of the band of interest, where the PA sees 98+j26 Ω in the transmit mode and the LNA sees 173-j15 Ω in the receive mode. The achieved impedance in each mode is very close to the goal, optimal impedance and certainly within the areas of interest on the Smith chart defined by the PA and LNA cells from Chapter 5. Fig. 6.8 shows the best possible bandwidth performance of the Fig. 5.13 PALNA topology (blue curve) compared to the bandwidth performance of the baseline solution (green curve) in transmit and receive.



(a) (b)

Fig. 6.7. Bandwidth metric of the 46 solutions for the Fig. 5.13 PALNA in: (a) transmit mode; (b) receive mode. Solution #1 is the baseline solution discussed in Chapter 5. Solution #24 represents a compromise between the transmit mode and receive mode performance, which is considered the best of the 46 solutions available.



(a) (b)

Fig. 6.8. Best possible bandwidth performance of Fig. 5.13 PALNA (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

Antenna reflection coefficient magnitudes of lossless circuits are shown. It is noted that Solution #24 clearly improved upon the bandwidth performance of the baseline solution; however, its performance did not achieve the reflection coefficient magnitude better than 0.316 in both modes of operation. Therefore, to further improve the bandwidth performance, alternative PALNA topologies were considered. Each of the following five

sub-sections explores a different PALNA bandwidth enhancement topology (BWET). The design rationale and approach are described for each topology and Step 1 simulation results that were generated using MATLAB are presented.

As in the previous chapters, it is noted that each topology was designed under the assumption of a wideband, 50 Ω antenna. While the impedance of real antennas generally varies as a function of frequency, the assumption of constant impedance, 50 Ω antenna was made here without the loss of generality and for the reasons of computational efficiency. If antenna impedance variation as a function of frequency were considered for a given PALNA topology, the nested search for the optimal PALNA components values would need to be repeated for each antenna impedance value, prolonging the search program execution time. Depending on the number of antenna impedance points considered, the resulting execution time could become very long. If, however, the antenna impedance variation over frequency was approximated using a small number of constant-impedance sections, the search program execution time may not be significantly prolonged, depending on the PALNA circuit complexity. On the other hand, if a PALNA solution were given, it would be straightforward and computationally inexpensive to study and evaluate in MATLAB simulations the effects of antenna impedance variation over frequency on the transmit mode and receive mode antenna reflection coefficients.

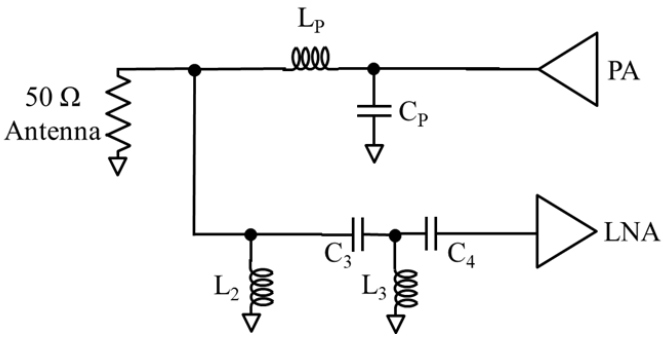
6.2.2 PALNA Bandwidth Enhancement Topology 1

Based on the results shown in Fig. 6.4, two conclusions were drawn. First, using a simple transmission line as a MN appears to be limiting from the perspective of bandwidth performance. Second, increasing the order (i.e., complexity) of a lumped-component MN appears to improve the bandwidth performance. So, with these two considerations in mind, an alternative PALNA topology was envisioned where the PA MN transmission line is replaced with a lumped-component LC network, while keeping the LNA MN topology the same as in Fig. 5.13 PALNA.

The Step 1 procedure from Fig. 6.3 flowchart was executed for a variety of PA MN LC

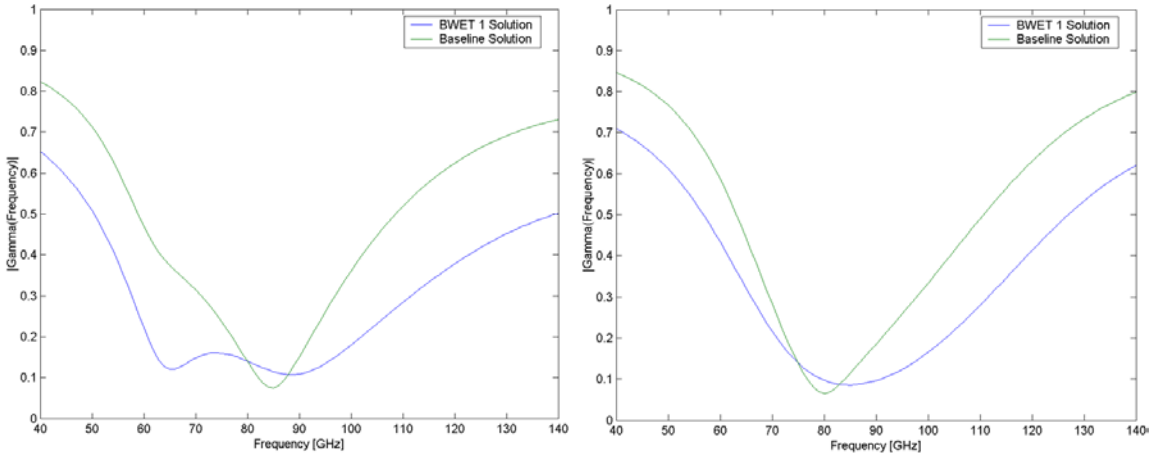
configurations. The first PA MN considered is a LCLC network with parallel Ls and series Cs. The resulting PALNA configuration produces some solutions, which means that the PALNA meets the impedance matching criteria in both transmit and receive, however the solutions are not favorable in terms of transducer loss and bandwidth metric performance. The second PA MN considered is a LCLC network with series Ls and parallel Cs and it was found that the resulting PALNA does not produce any immediate solutions. Then, a variety of the sub-topologies of the two PA MNs were considered. As a third topology, a PA MN was considered with one parallel L and one series C and it was found that the resulting PALNA does not result in any solutions. Fourth, when the order of the PA MN was increased to LCL, with parallel Ls and series C, it was found that the resulting PALNA produces some solutions however with unsatisfactory transducer loss and bandwidth metric performance. Fifth, a LCL PA MN was considered with series Ls and parallel C and it was found that the resulting PALNA configuration produces numerous solutions albeit with transducer loss and bandwidth metric performance that still seem limited. Finally, sixth, a LC PA MN was considered with series L and parallel C and it was found that the resulting PALNA configuration produces numerous solutions with good transducer loss and good bandwidth metric performance. Thus, this PALNA topology, whose schematic is shown in Fig. 6.9, is considered to be the first PALNA topology alternative, which is referred to as the PALNA bandwidth enhancement topology 1 in the remainder of this text.

After the Step 1 procedure from Fig. 6.3 flowchart was executed for bandwidth enhancement topology 1, the best solution was achieved for the values of circuit parameters shown in Fig. 6.9. Figure 6.10 shows the final bandwidth performance of the lossy PALNA bandwidth enhancement topology 1 compared to the bandwidth performance of the baseline solution (i.e., the Fig. 5.13 PALNA). The transducer transmit and received losses achieved at 94 GHz, near the center of the band of interest, are 2.33 dB and 2.87 dB, respectively. The minimum bandwidth transmit and receive metrics achieved are 5.73 GHz and 5.01 GHz.



Circuit Parameter	Value	Unit
L_P	80	pH
C_P	17	fF
L_2	120	pH
C_3	17	fF
L_3	150	pH
C_4	17	fF

Fig. 6.9. Schematic of the PALNA bandwidth enhancement topology 1 and the optimum values of circuit parameters.

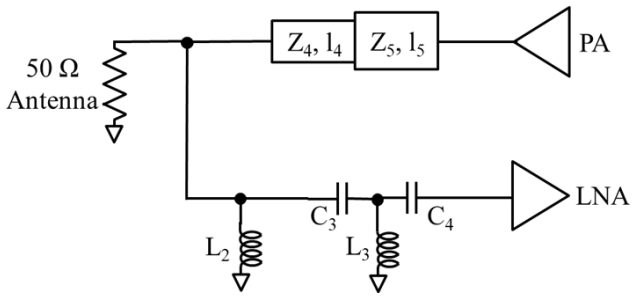


(a) (b)

Fig. 6.10. Bandwidth performance of PALNA bandwidth enhancement topology 1 (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

6.2.3 PALNA Bandwidth Enhancement Topology 2

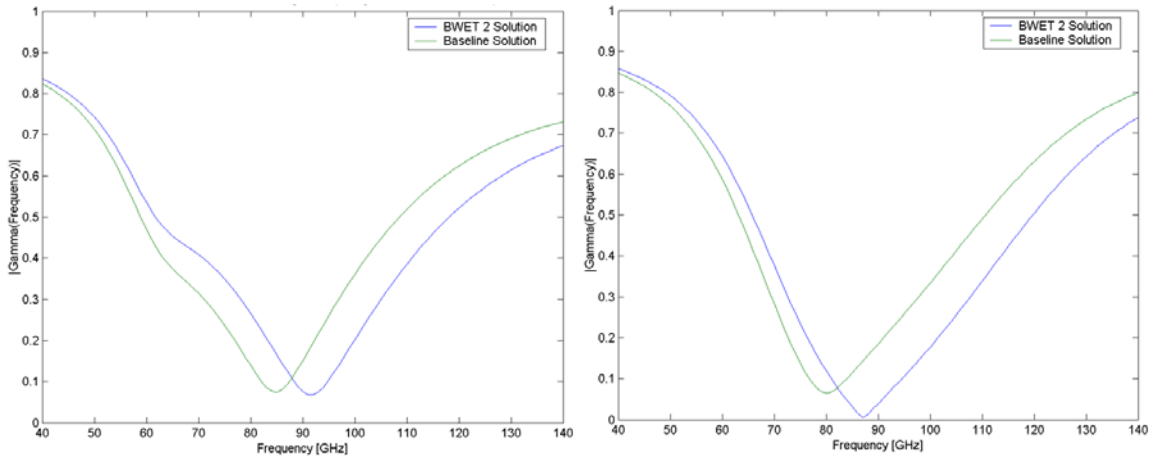
Continuing the reasoning described in the previous sub-section, the PA MN transmission line in the Fig. 5.13 PALNA was replaced with a multi-section impedance transformer. Multi-section impedance transformers offer a well-known approach for increasing the bandwidth [44]. The simplest multi-section impedance transformer consists of only two transmission line sections and thus, the PALNA topology whose schematic is shown in Fig. 6.11, was chosen as the second PALNA topology alternative. This PALNA topology is referred to as the PALNA bandwidth enhancement topology 2 in the remainder of this



Circuit Parameter	Value	Unit
Z_4	58	Ω
l_4	65	o
Z_5	30	Ω
l_5	29	o
L_2	60	pH
C_3	17	fF
L_3	140	pH
C_4	20	fF

Fig. 6.11. Schematic of the PALNA bandwidth enhancement topology 2 and the optimum values of circuit parameters.

text. In the study of PALNA bandwidth enhancement topology 2, the PA MN transmission line sections were of arbitrary lengths and their impedance was subjected to 20 Ω – 70 Ω range practically realizable in the 32SOI process [49]. The completion of the Step 1 procedure from Fig. 6.3 flowchart for the PALNA bandwidth enhancement topology 2 resulted in a large number of acceptable solutions. In general, a clear tradeoff was noticed between the transducer loss performance and the bandwidth performance for this topology. The solutions with longer transmission line segments tend to produce very good bandwidth performance results but at the cost of higher transducer loss. The solutions with shorter segments, which result in better loss performance, tend to produce acceptable bandwidth performance, which is better than the Fig. 5.13 PALNA baseline solution bandwidth performance, but is still somewhat limited. The best solution overall was achieved for the values of circuit parameters shown in Fig. 6.11. Figure 6.12 shows the bandwidth performance of the lossy PALNA bandwidth enhancement topology 2. The minimum transducer transmit and received losses achieved are 2.55 dB and 2.93 dB, respectively. The minimum bandwidth transmit and receive metrics achieved are 7.69 GHz and 5.18 GHz.

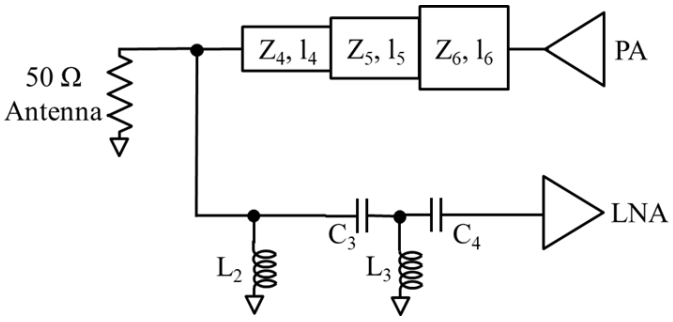


(a) (b)

Fig. 6.12. Bandwidth performance of PALNA bandwidth enhancement topology 2 (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

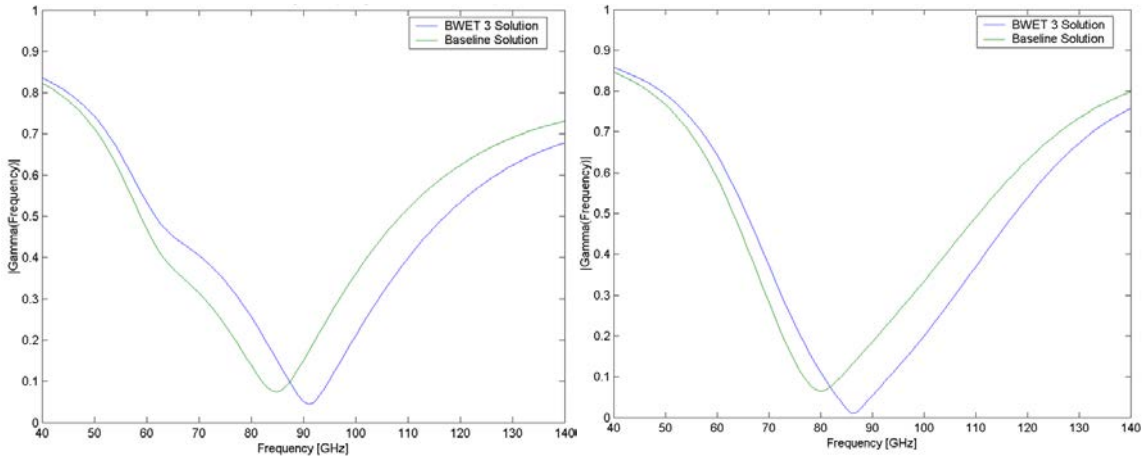
6.2.4 PALNA Bandwidth Enhancement Topology 3

The PA MN complexity was then increased by the addition of another transmission line section. Fig. 6.13 shows the schematic of an alternative PALNA topology that is referred to as the PALNA bandwidth enhancement topology 3. In bandwidth enhancement topology 3, the PA MN was implemented as a three-section transmission line transformer with sections of arbitrary length [49]. As in the previous sub-section, the impedance of the transmission line segments was limited to the 20 Ω – 70 Ω range that is practically realizable in the 32SOI process. Completion of the Step 1 procedure from Fig. 6.3 flowchart for the PALNA bandwidth enhancement topology 3 resulted in a large number of acceptable solutions, with many of the solutions outperforming the Fig. 5.13 PALNA baseline solution. The best solution was achieved for the values of circuit parameters shown in Fig. 6.13. Figure 6.14 shows the bandwidth performance of the lossy PALNA bandwidth enhancement topology 3. The minimum transducer transmit and received losses achieved are 2.42 dB and 3.07 dB, respectively. The minimum bandwidth transmit and receive metrics achieved are 7.55 GHz and 5.56 GHz.



Circuit Parameter	Value	Unit
Z_4	64	Ω
l_4	42	o
Z_5	54	Ω
l_5	20	o
Z_6	34	Ω
l_6	34	o
L_2	60	pH
C_3	17	fF
L_3	140	pH
C_4	20	fF

Fig. 6.13. Schematic of the PALNA bandwidth enhancement topology 3 and the optimum values of circuit parameters.

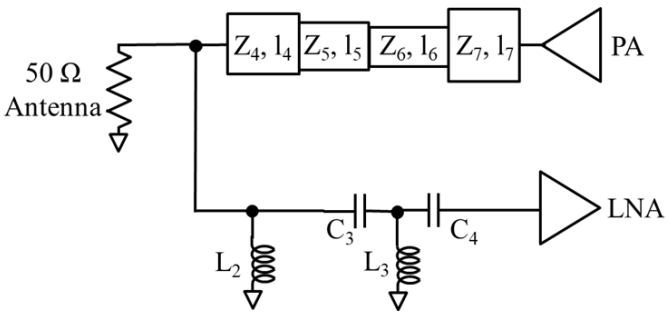


(a) (b)

Fig. 6.14. Bandwidth performance of PALNA bandwidth enhancement topology 3 (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

6.2.5 PALNA Bandwidth Enhancement Topology 4

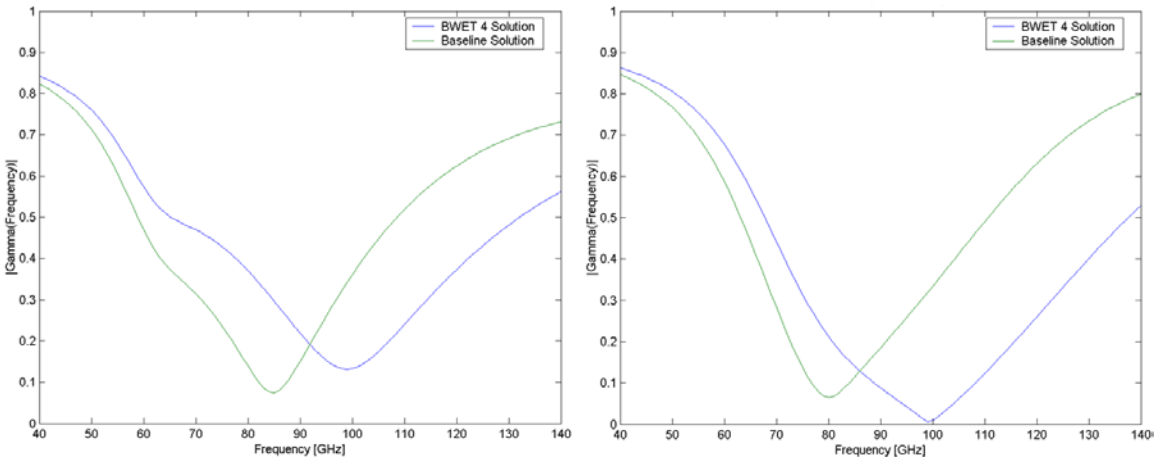
Continuing the reasoning from the previous sub-sections, the PA MN complexity was increased further. Fig. 6.15 shows the schematic of an alternative PALNA topology that is referred to as the PALNA bandwidth enhancement topology 4. In PALNA bandwidth enhancement topology 4, the PA MN was implemented as a four-section transmission line transformer with sections of arbitrary length and with impedance constrained to the practically realizable 20 Ω – 70 Ω range [49]. After the Step 1 procedure from Fig. 6.3



Circuit Parameter	Value	Unit
Z_4	42	Ω
l_4	7	o
Z_5	54	Ω
l_5	59	o
Z_6	56	Ω
l_6	12	o
Z_7	28	Ω
l_7	12	o
L_2	60	pH
C_3	17	fF
L_3	140	pH
C_4	20	fF

Fig. 6.15. Schematic of the PALNA bandwidth enhancement topology 4 and the optimum values of circuit parameters.

flowchart was completed for the PALNA bandwidth enhancement topology 4, the best solution was achieved for the values of circuit parameters shown in Fig. 6.15. Figure 6.16 shows the bandwidth performance of the lossy PALNA bandwidth enhancement topology 4. The minimum transducer transmit and receive losses achieved are 3.12 dB and 2.48 dB, respectively. The minimum bandwidth transmit and receive metrics achieved are 8.90 GHz and 4.24 GHz.

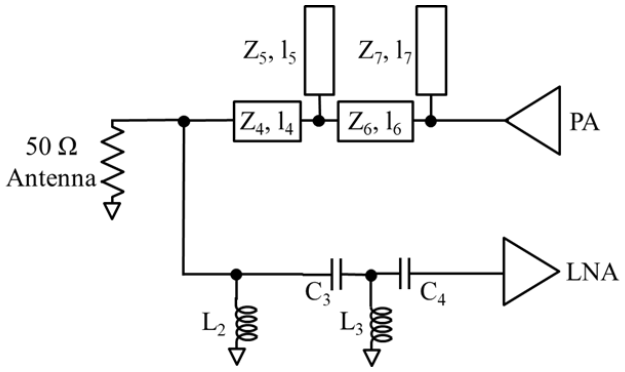


(a) (b)

Fig. 6.16. Bandwidth performance of PALNA bandwidth enhancement topology 4 (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

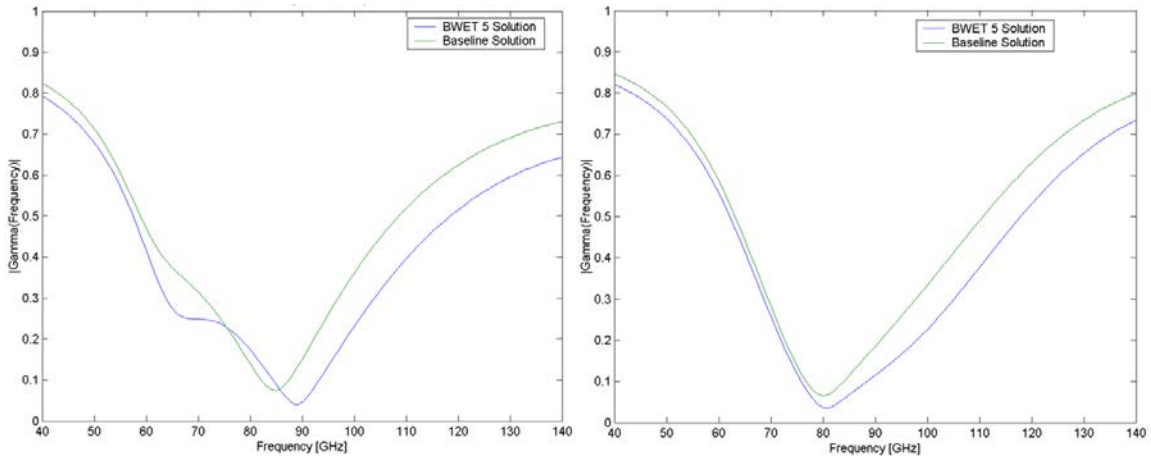
6.2.6 PALNA Bandwidth Enhancement Topology 5

In addition to replacing the PA MN transmission line with lumped component circuits and multi-section impedance transformers, as was described in the preceding four sub-sections, a broadband and low loss PALNA performance can be achieved by replacing the PA MN transmission line with a short-step-stub impedance transformer [50]. The main advantage of the short-step-stub impedance transformers is that their physical size can be relatively small (i.e., they can be implemented using relatively short transmission line segments), thus creating a possibility for an improved loss performance [50]. Therefore, an alternative PALNA topology that is shown in Fig. 6.17 was envisioned. The PALNA topology is referred to as the PALNA bandwidth enhancement topology 5 in the remainder of this text. In the PALNA bandwidth enhancement topology 5, the PA MN short-step-stub impedance transformer was implemented using transmission line sections of arbitrary length whose impedances were constrained to the practically realizable 20 Ω – 70 Ω range. After the Step 1 procedure from Fig. 6.3 flowchart was completed for bandwidth enhancement topology 5, the best solution was achieved for the values of circuit parameters shown in Fig. 6.17. Figure 6.18 shows the bandwidth performance of the lossy PALNA bandwidth enhancement topology 5. The minimum transducer transmit and received losses achieved



Circuit Parameter	Value	Unit
Z_4	60	Ω
l_4	82	o
Z_5	48	Ω
l_5	13	o
Z_6	38	Ω
l_6	9	o
Z_7	54	Ω
l_7	9	o
L_2	70	pH
C_3	17	fF
L_3	140	pH
C_4	17	fF

Fig. 6.17. Schematic of the PALNA bandwidth enhancement topology 5 and the optimum values of circuit parameters.



(a) (b)

Fig. 6.18. Bandwidth performance of PALNA bandwidth enhancement topology 5 (blue curve) is compared to the bandwidth performance of the baseline solution in: (a) transmit; (b) receive.

are 2.49 dB and 3.06 dB, respectively. The minimum bandwidth transmit and receive metrics achieved are 6.65 GHz and 5.73 GHz.

In addition to the PALNA configuration shown in Fig. 6.17, which produces a large number of acceptable solutions, five other related PALNA configurations were considered. First, the PA MN short-step-stub transformer was flipped, so that the PA output connects to the

segment of impedance Z_4 and the antenna junction connects to the stub segment of impedance Z_7. The resulting PALNA produces some solutions, albeit with unacceptable transducer loss and bandwidth performance. Second, four PALNA configurations were considered where both the PA MN and LNA MN were implemented using the short-step-stub transformers both in the "usual" configuration, such as the one shown in Fig. 6.17 PA MN, and the "flipped" configuration described above. None of these four PALNA configurations produces any appealing solutions.

6.2.7 Summary of Step 1 Simulation Results For The Five Bandwidth Enhancement Topologies

Based on the Step 1 results presented and discussed in the preceding five sub-sections, the performance of the PALNA bandwidth enhancement topology 1 approaches closest to the above-calculated Bode-Fano limits and exceeds the performance goal of $|\Gamma| < 0.316$ from 75 GHz to 110 GHz in both modes of operation with the highest amount of margin and with low loss. Table 6.1 summarizes the Step 1 performance of the five lossy PALNA bandwidth enhancement topologies considered. The impedance matching performance of all topologies is good at 94 GHz, near the center of the band of interest, as shown in Table 6.1. The impedance transformation that is achieved with each topology in each mode of operation is very close to the applicable optimal impedance and certainly within the areas of interest on the Smith chart defined by the PA and LNA cells from Chapter 5. Based on these results, the PALNA bandwidth enhancement topology 1 was selected for further implementation in Cadence using EM modeled components (Step 2, discussed in the next section) and the other four PALNA bandwidth enhancement topologies were dropped from further consideration.

The nested search programs written and executed in MATLAB for the PALNA topologies discussed above vary significantly in computational complexity and the required execution time, which depend on the number of parameters required to implement each PALNA circuit model. For example, circuit models for PALNA topologies 4 and 5 each have 12

Table 6.1.
Lossy PALNA bandwidth enhancement topologies performance summary. The transducer loss and the impedance values were noted at 94 GHz. Topology 1 achieves the best overall performance.

		Results Achieved in MATLAB Simulations				
Performance Metric	Unit	Topology 1	Topology 2	Topology 3	Topology 4	Topology 5
Transmit Transducer Loss	dB	2.33	2.55	2.42	3.12	2.49
Receive Transducer Loss	dB	2.87	2.93	3.07	2.48	3.06
Transmit Bandwidth Metric	GHz	5.73	7.69	7.55	8.90	6.65
Receive Bandwidth Metric	GHz	5.01	5.18	5.56	4.24	5.73
Impedance at PA Output	Ω	125+j33	110+j34	119+j34	85+j51	117+j33
Impedance at LNA Input	Ω	181+j8	162+j21	163+j25	172-j4	155+j20

parameters and require 12-layer nested loops, which were found through experimentation to be too computationally cumbersome to be fully executed on a standard commercial laptop computer. Therefore, for topologies where the parameter space could not be fully explored in a reasonable amount of time, various tricks were used to arrive at acceptable solutions. One of these tricks involved performance evaluation of candidate PALNA solutions using randomized settings of PALNA parameters (i.e., capacitances, inductances, transmission line lengths and impedances) over the full range of their values. To implement such randomized searches, a single loop was used in the search program and the loop was allowed to execute for a number of times that required a reasonable amount of time. During each loop execution, each PALNA parameter value was randomized within an interval of its possible values. For each PALNA topology where the randomized search was used, the program was executed several times. This approach ensured that the PALNA solution spaces were fully explored, albeit not with the fidelity of a full nested search. The search program execution time was one of the reasons why PALNAs with more parameters were not explored at this time. MATLAB scripts used for design of PALNA networks discussed in this chapter are provided in Appendix B.

6.3 PALNA MN Development in Cadence Using EM Modeled Components (Step 2)

After Step 1 from Fig. 6.3 flowchart was completed and PALNA bandwidth enhancement topology 1 was identified as the most promising topology with best overall performance, the PALNA bandwidth enhancement topology 1 was implemented in a Cadence schematic. First, EM models of all the required PALNA components (inductors and capacitors) were implemented and simulated in Sonnet using 32SOI process metal stack and design rules to produce representative s-parameter files, and they were verified in Cadence schematic by comparison with their ideal, lossless equivalents. Next, the PALNA MN schematic was assembled in Cadence, by adding the appropriate EM-simulated transmission line junctions to connect the components. Then, the PALNA was simulated in both modes of operation and all the performance parameters of interest were noted as the lengths of the transmission lines were iteratively adjusted with each simulation cycle until the simulated PALNA performance became optimal. After this process of iterative optimization was completed for PALNA bandwidth enhancement topology 1, the final PALNA schematic was obtained, which is shown in Fig. 6.19.

Fig. 6.20 shows the receive mode comparison of reflection coefficient bandwidth between the baseline PALNA topology from Chapter 5 and PALNA bandwidth enhancement topology 1. For the baseline PALNA topology, s_{11} of -10 dB or better is achieved from 77.5 GHz to 104.1 GHz, over a 26.6 GHz bandwidth. For the PALNA bandwidth enhancement topology 1, s_{11} of -10 dB or better is achieved from 75.8 GHz to 107 GHz, over a 31.2 GHz bandwidth. The PALNA bandwidth enhancement topology 1 implementation therefore represents a bandwidth performance improvement of 4.6 GHz. Also, with s_{11} = - 9.3 dB at 75 GHz and s_{11} = - 8.3 dB at 110 GHz, the PALNA bandwidth enhancement topology 1 comes very close to meeting the $s_{11} \leq$ -10 dB benchmark over the entire W-band.

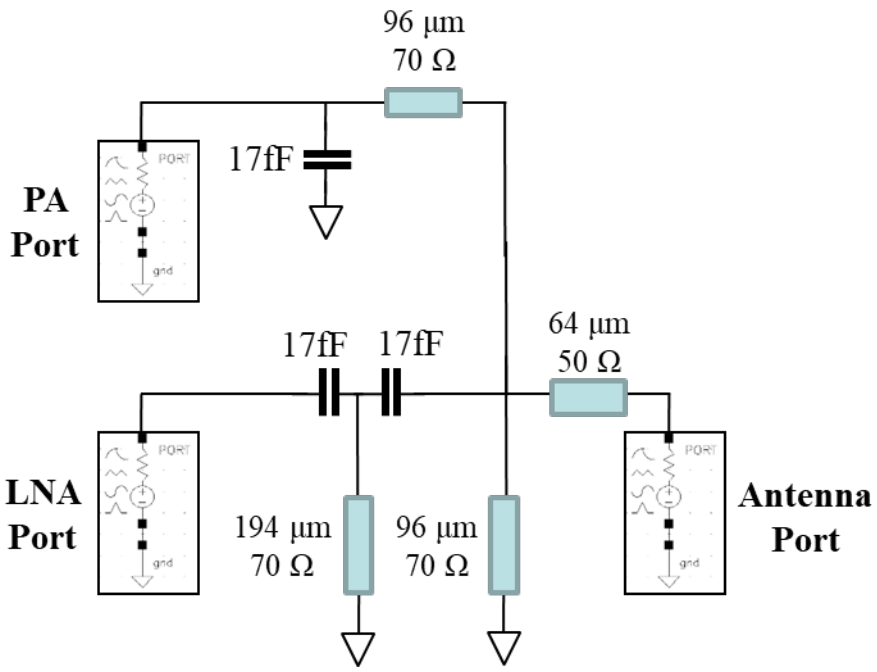


Fig. 6.19. The final PALNA bandwidth enhancement topology 1 schematic obtained through Step 2 iterative optimization. All schematic components, except for the ports, are represented by s-parameter files generated through EM model simulations in Sonnet.

Fig. 6.21 shows the transmit mode comparison of reflection coefficient bandwidth between the baseline PALNA topology from Chapter 5 and PALNA bandwidth enhancement topology 1. For the baseline topology, the s_{11} of -10 dB or better is achieved from 79.4 GHz to 99.9 GHz, over a 20.5 GHz bandwidth. For the PALNA bandwidth enhancement topology 1, the s_{11} of -10 dB or better is achieved from 71.9 GHz to 103.7 GHz, over a

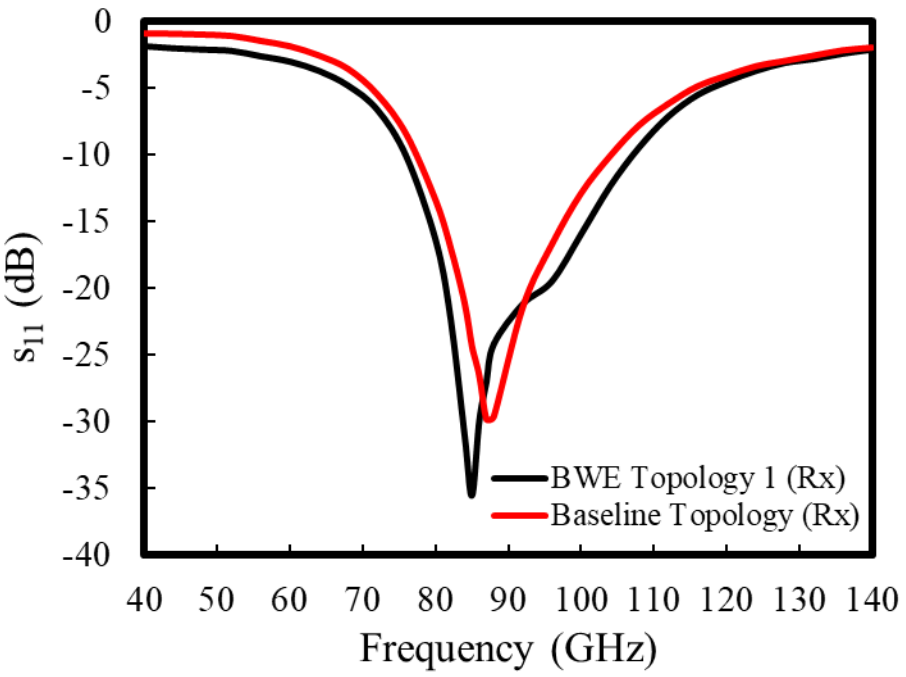


Fig. 6.20. Receive mode comparison of reflection coefficient bandwidth between the baseline PALNA topology from Chapter 5 and bandwidth enhancement topology 1.

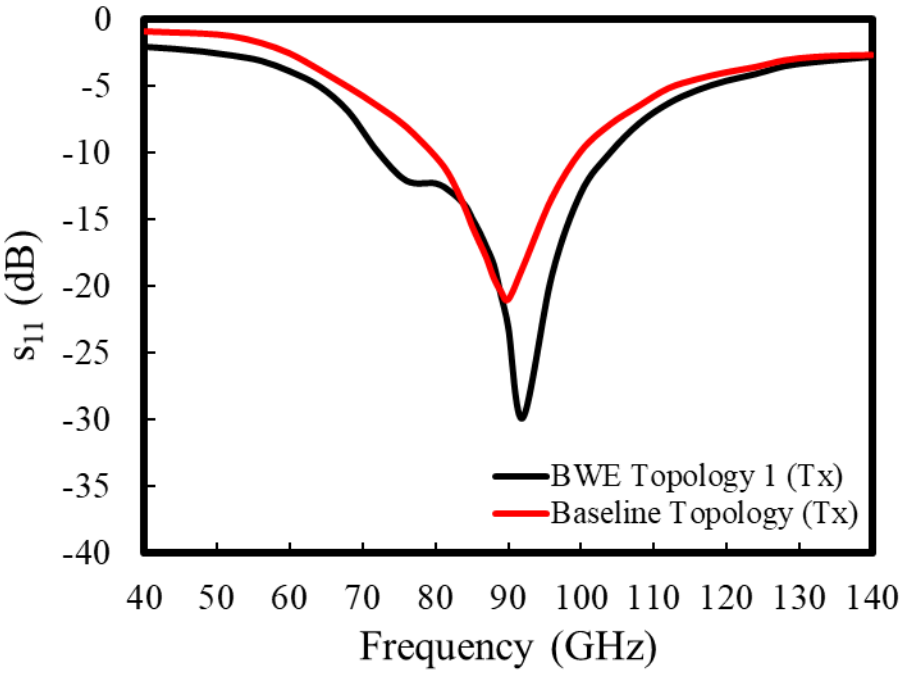


Fig. 6.21. Transmit mode comparison of reflection coefficient bandwidth between the baseline PALNA topology from Chapter 5 and bandwidth enhancement topology 1.

31.8 GHz bandwidth. The PALNA bandwidth enhancement topology 1 therefore represents a bandwidth improvement of 11.3 GHz. Also, with s_{11} = - 11.8 dB at 75 GHz and s_{11} = - 7.0 dB at 110 GHz, the PALNA bandwidth enhancement topology 1 comes very close to meeting the $s_{11} \leq$ -10 dB benchmark over the entire W-band.

It is noted that, in order to achieve the best PAE and NF performance possible, the final PALNA bandwidth enhancement topology 1 circuit was not optimized for maximum bandwidth possible but for the most favorable tradeoff between the transmit and receive transducer loss. If further improvement is needed in bandwidth performance, it can be achieved by making circuit design tradeoffs. For example, when the PALNA bandwidth enhancement topology 1 PA MN inductor transmission line was shortened from 96 μm to 80 μm, the s_{11} of -10 dB or better was achieved from 77.1 GHz to 112.2 GHz in receive (35.1 GHz bandwidth) and from 73.8 GHz to 107.5 GHz in transmit (33.7 GHz bandwidth). This modified bandwidth enhancement topology 1 will be referred to as “BWET 1 Mod”. These improved bandwidth results are clearly shown in Fig. 6.22 and Fig. 6.23. However, the shortening of the PA MN inductor transmission line also resulted in a less optimal transducer loss performance; the transmit mode transducer loss increased by 0.4 dB and the receive mode transducer loss decreased by 0.3 dB. Since the most important PALNA design metric has been PAE throughout this work, this might not be the tradeoff worth making because the additional PALNA loss in the transmit mode will translate into degraded PAE performance. Nevertheless, with bandwidth performance being a PALNA design criterion, tradeoffs like this one are available to be made at each step of the PALNA design process.

Fig. 6.24. shows the simulated transducer loss of the final, optimized PALNA bandwidth enhancement topology 1 circuit in the transmit and the receive modes of operation. At 94 GHz, the simulated transducer loss is 2.8 dB and 3.1 dB in transmit and receive, respectively.

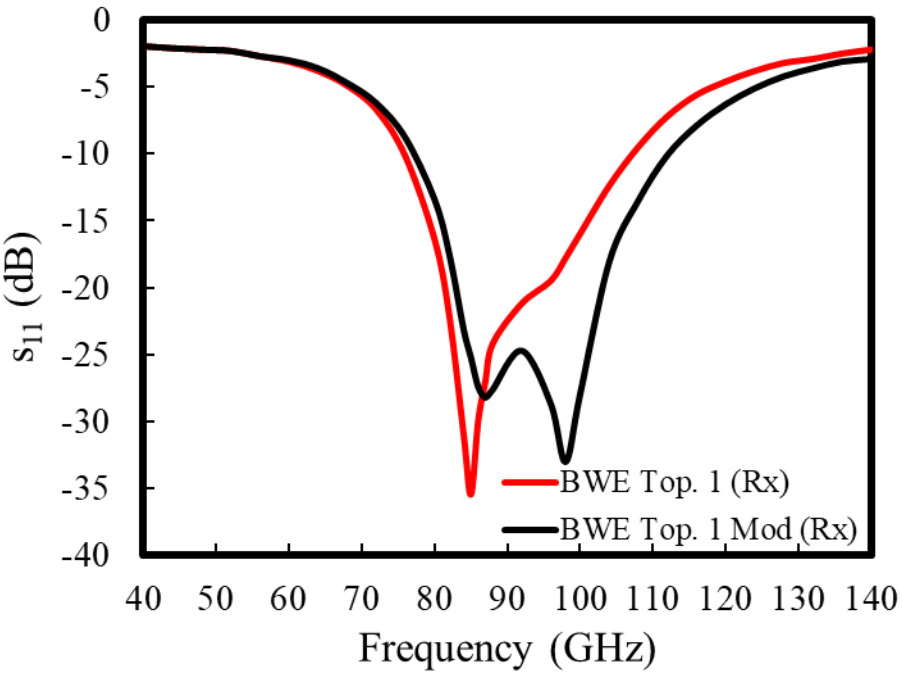


Fig. 6.22. Effect on bandwidth performance in receive mode of bandwidth enhancement topology 1 operation when the PA MN inductor transmission line is shortened from 96 μm to 80 μm.

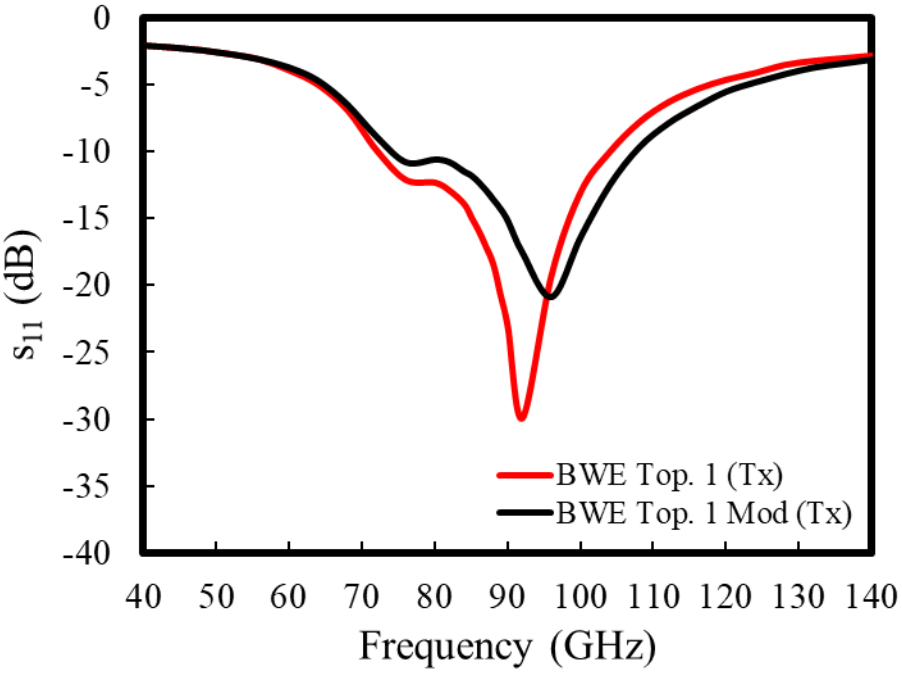


Fig. 6.23. Effect on bandwidth performance in transmit mode of bandwidth enhancement topology 1 operation when the PA MN inductor transmission line is shortened from 96 μm to 80 μm.

The impedance matching performance of the final PALNA bandwidth enhancement topology 1 circuit is good at 94 GHz, near the center of the band, and the impedances seen by the PA and the LNA are 109.5 + j22.2 Ω and 151.8 – j1 Ω, respectively. These impedances are very close to the optimal PA and LNA impedances of 90 Ω and 150 + j25 Ω and are located well within the impedance matching regions defined on the Smith chart for the PA and the LNA, which were discussed in Chapter 5 (Fig. 5.5 and Fig. 5.9).

Table 6.2 summarizes the simulation performance of the lossy BWET 1 and BWET 1 Mod PALNAs implemented in Cadence using EM simulated component models. The transducer loss and the impedance values were noted at 94 GHz. BWET 1 Mod achieves bandwidth performance gain at the expense of transducer loss performance.

To complete the PALNA bandwidth enhancement topology 1 study, the PA and the LNA ports were replaced with the original PA and LNA cells from Chapter 5. Then, the complete PALNA was resimulated in Cadence. The results of these simulations are discussed in the following section.

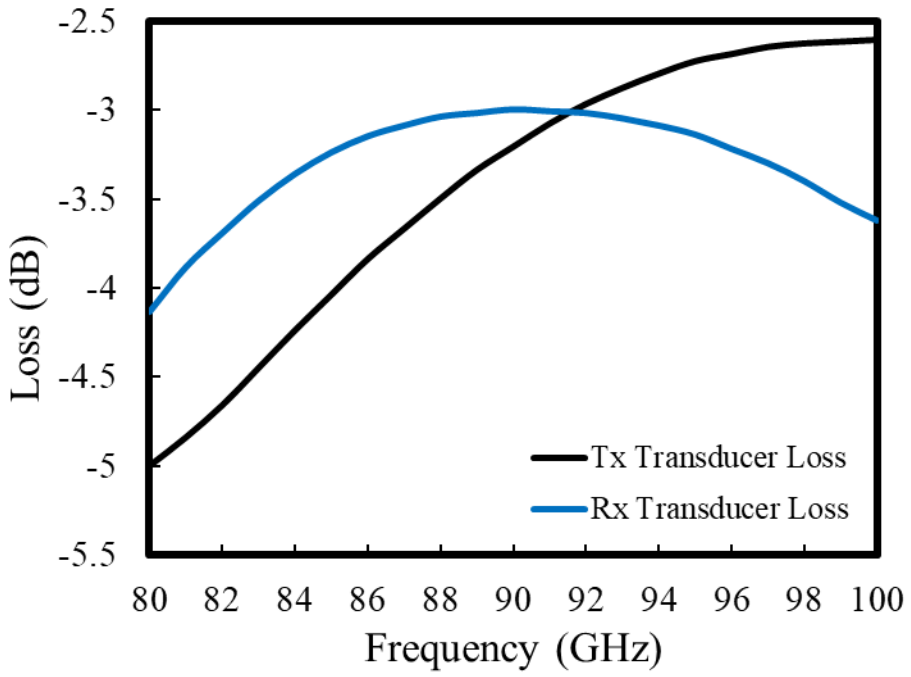


Fig. 6.24. Simulated transducer loss of the final, optimized bandwidth enhancement topology 1 PALNA circuit in the transmit and the receive modes of operation.

Table 6.2.
Performance summary of the lossy BWET 1 and BWET 1 Mod PALNAs implemented in Cadence using EM simulated component models. The transducer loss and the impedance values were noted at 94 GHz. BWET 1 Mod achieves bandwidth performance gain at the expense of transducer loss performance.

Performance Metric	Unit	BWET 1 Cadence Simulation Results	BWET 1 Mod Cadence Simulation Results
Transmit Transducer Loss	dB	2.8	3.2
Receive Transducer Loss	dB	3.1	2.8
Transmit Bandwidth (with $\|\Gamma\| < 0.316$)	GHz	31.8	33.7
Receive Bandwidth (with $\|\Gamma\| < 0.316$)	GHz	31.2	35.1
Impedance at PA Output	Ω	109.5 + j22.2	91.4 + j32
Impedance at LNA Input	Ω	151.8 – j1	153.2 – j17.4

6.4 Fully Integrated PALNA Cadence Simulation Results (Step 3)

After Step 2 from Fig. 6.3 flowchart was completed and PALNA bandwidth enhancement topology 1 MN was implemented in Cadence using EM modeled components, the PALNA MN was integrated with the PA and LNA cells that were designed in Step 0 and described in section 5.3. Then, the resulting PALNA was simulated in both modes of operation and its performance results were noted and analyzed. Fig. 6.25 – Fig. 6.31 show the PALNA simulation results. Fig. 6.25 shows the simulation results of PALNA bandwidth enhancement topology 1 small signal s-parameters and NF in the receive mode of operation. At 94 GHz, the s_{21} gain is 8 dB and the NF is 7.4 dB, which is consistent with expectations given the known PALNA bandwidth enhancement topology 1 MN transducer loss in receive mode. In comparison with Fig. 5.18, it should be noted that the bandwidth of the PALNA did not change substantially. This is also expected and is a consequence of the bandwidth limitations of the PA and LNA cells. In order to increase the bandwidth of the overall PALNA, it is necessary to start by designing PA and LNA cells that cover the bandwidth of interest. While increasing the bandwidth of the PA and the LNA cells to cover the entire W-band, from 75 GHz to 110 GHz, requires fundamentally different PA and LNA architectures and is beyond the scope of work presented here, extensive treatment of broadband amplifier design is available in literature [47], [51].

Fig. 6.26 shows the result of the Cadence Spectre simulation of the PALNA port isolation in the receive mode of operation as a function of frequency of operation. The isolation exceeds 20 dB at 94 GHz and the curve has a close resemblance to the receive mode curve of Fig. 5.21. Fig. 6.27 shows the result of the Cadence Spectre simulation of the PALNA P_{out}, Power Gain, and PAE in the transmit mode of operation at 94 GHz. P_{sat} reaches 10 dBm, maximum PAE reaches 16 %, and Maximum Power Gain reaches 10.5 dBm. The PAE performance is slightly worse than the performance shown in Fig. 5.19, which was

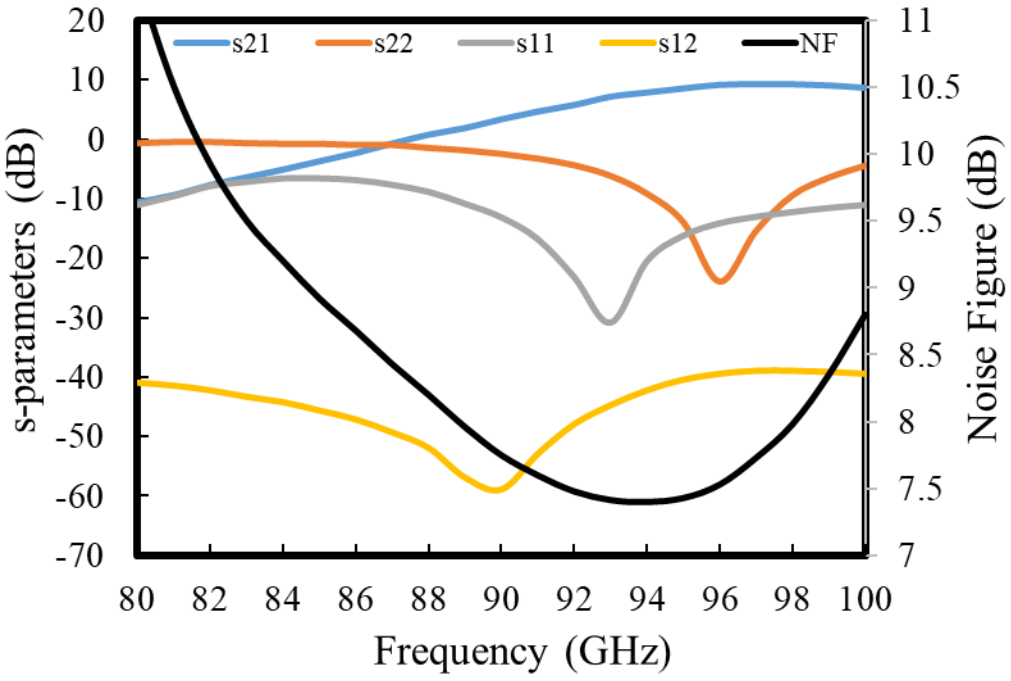


Fig. 6.25. Result of the Cadence Spectre simulation of bandwidth enhancement topology 1 PALNA small signal s-parameters and NF in the receive mode of operation. At 94 GHz, s_{21} gain is 8 dB and the NF is 7.4 dB.

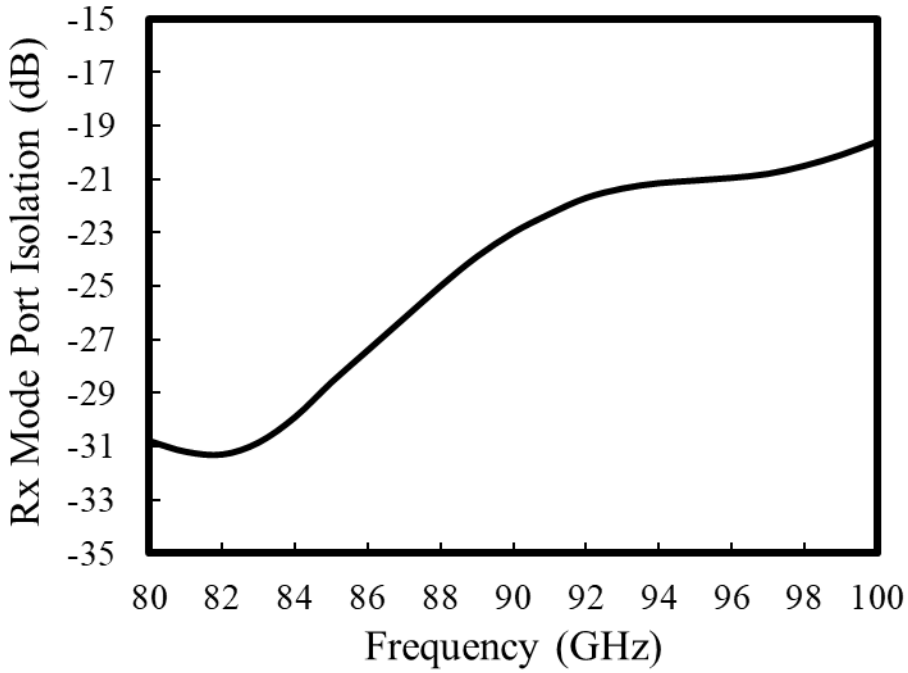


Fig. 6.26. Result of the Cadence Spectre simulation of PALNA port isolation in the receive mode of operation as a function of frequency of operation. The isolation is > 20 dB at 94 GHz.

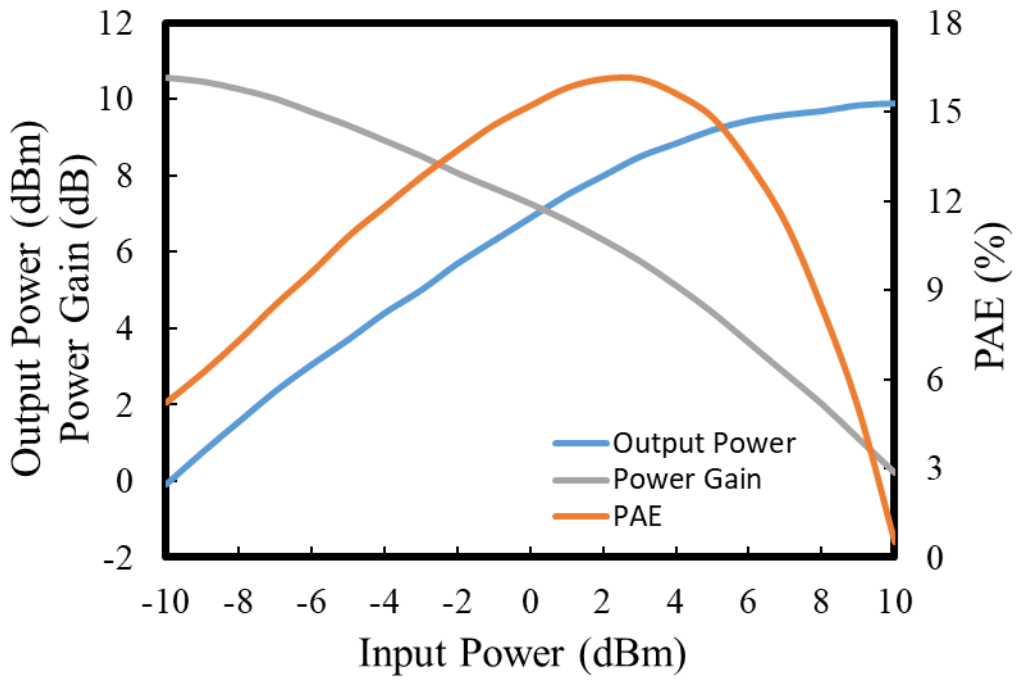


Fig. 6.27. Result of the Cadence Spectre simulation of bandwidth enhancement topology 1 PALNA P_{out}, Power Gain, and PAE in the transmit mode of operation at 94 GHz. P_{sat} reaches 10 dBm, maximum PAE reaches 16 %, and Maximum Power Gain reaches 10.5 dBm.

expected because the PALNA MN loss in the transmit mode is slightly higher for PALNA bandwidth enhancement topology 1 PALNA than it is for the baseline PALNA.

Fig. 6.28 and Fig. 6.29 show the Cadence Spectre simulations of PALNA transmit mode large signal Maximum Output Power and PAE, respectively, as a function of frequency of operation. PALNA bandwidth enhancement topology 1 and baseline PALNA performances were plotted and compared. In both figures, the performance of PALNA bandwidth enhancement topology 1 is slightly worse than the performance of the baseline PALNA, which is expected due to slightly higher PALNA MN loss of the bandwidth enhancement topology 1. Otherwise, the curves have very similar shapes and, like in the LNA case, the bandwidth performance is dominated by the bandwidth performance of the PA cell. In Fig. 6.28, the Maximum P_{out} was noted at P_{in} = 10 dBm, so the performance shown is slightly better than the performance shown in Fig. 5.20, where Max. P_{out} was noted at P_{in} = 5 dBm.

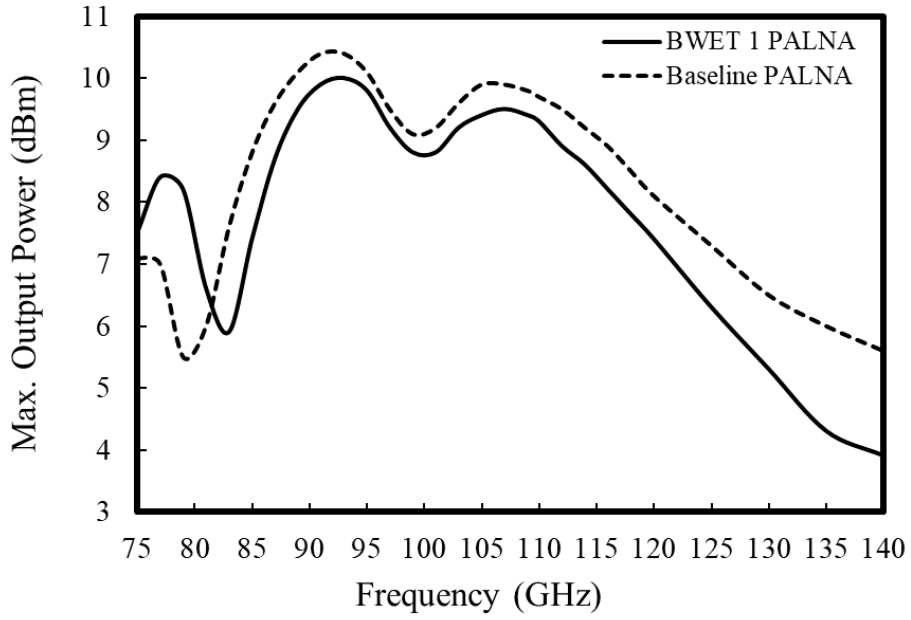


Fig. 6.28. Result of the Cadence Spectre simulation of PALNA transmit mode large signal Maximum Output Power as a function of frequency of operation. bandwidth enhancement topology 1 PALNA and Baseline PALNA are compared. Maximum P_{out} is noted at P_{in} = 10 dBm.

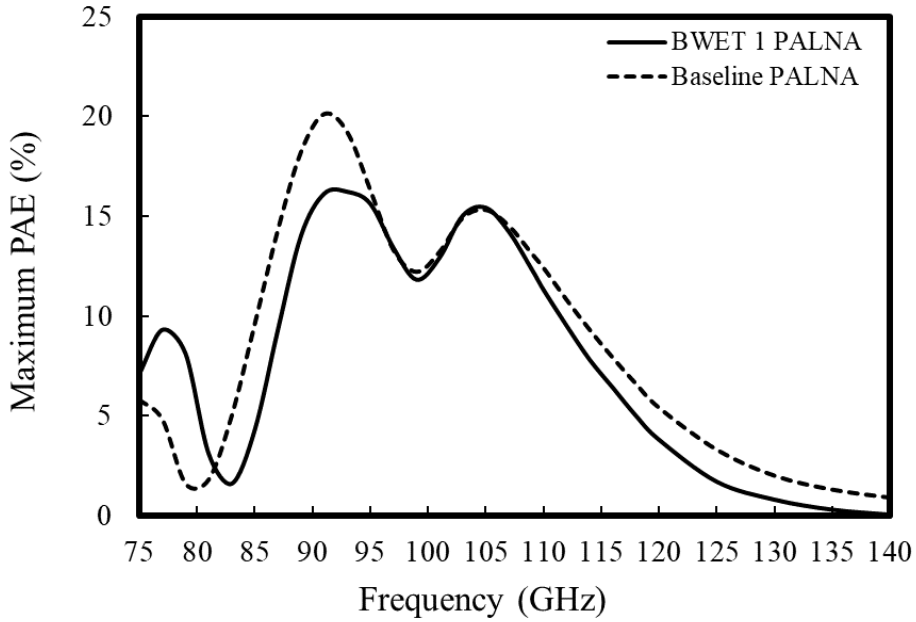


Fig. 6.29. Result of the Cadence Spectre simulation of PALNA transmit mode large signal Maximum PAE as a function of frequency of operation. bandwidth enhancement topology 1 PALNA and Baseline PALNA are compared.

Fig. 6.30 shows the result of the Cadence Spectre simulation of PALNA bandwidth enhancement topology 1 small signal s-parameters in the transmit mode of operation. It was noted that at 94 GHz, the s_{21} gain is 10.3 dB. Comparison of the results shown in Fig. 6.30 with the simulated results shown in Fig. 5.26 revealed a high degree of similarity, indicating that the PALNA bandwidth performance in the transmit mode is dominated by the bandwidth performance of the PA cell rather than the performance of the PALNA MN alone.

Fig. 6.31 shows the result of the Cadence Spectre simulation of PALNA port isolation in the transmit mode of operation as a function of frequency of operation. The isolation exceeds 17 dB at 94 GHz and the curve has close similarity to the transmit mode curve shown in Fig. 5.21.

Table 6.3 summarizes the Cadence simulation performance of the lossy PALNA bandwidth enhancement topology 1 with PA and LNA cells from Chapter 5.

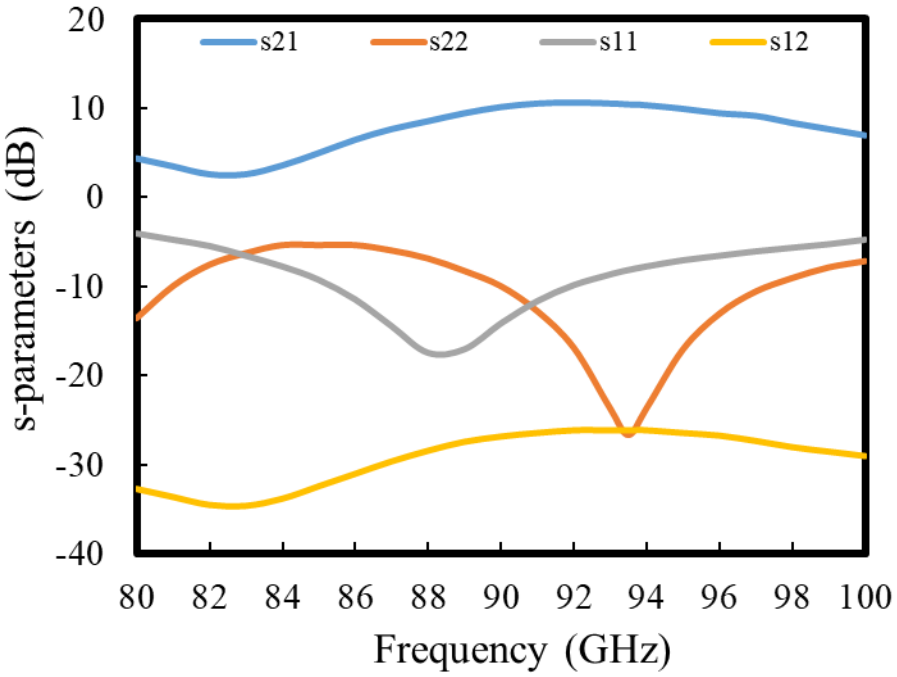


Fig. 6.30. Result of the Cadence Spectre simulation of bandwidth enhancement topology 1 PALNA small signal s-parameters in the transmit mode of operation. At 94 GHz, the s_{21} gain is 10.3 dB.

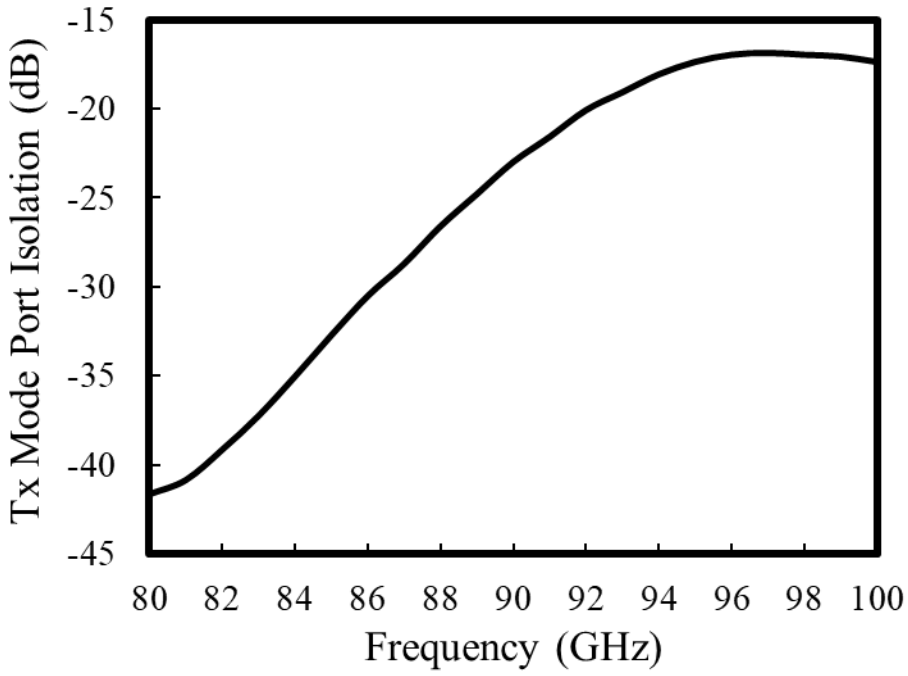


Fig. 6.31. Result of the Cadence Spectre simulation of PALNA port isolation in the transmit mode of operation as a function of frequency of operation. The isolation is > 17 dB at 94 GHz.

Table 6.3.
The performance summary of the lossy PALNA bandwidth enhancement topology 1 implemented in Cadence using EM simulated component models and PA / LNA cells from Chapter 5.

Performance Metric	Baseline Design Results	BWET 1 Results
Max Power Gain @ 94 GHz [dB]	> 10	10.5
Max PAE @ 94 GHz [%]	18	16
P_{sat} @ 94 GHz [dBm]	> 8 (*)	10 (**)
Transmit IP_{1dB} @ 94 GHz [dBm]	1.5	2.7
Receive Gain @ 94 GHz [dB]	8.8	8
NF @ 94 GHz [dB]	6.5	7.4
Transmit Port Isolation @ 94 GHz [dB]	18.7	> 17
Receive Port Isolation @ 94 GHz [dB]	> 20	> 20
Transmit Bandwidth, s_{11} < -10 dB [GHz]	7.2	7.5
Receive Bandwidth, s_{11} < -10 dB [GHz]	12.0	13.3

(*) Value noted at P_{in} = 5 dBm. (**) Value noted at P_{in} = 10 dBm.

6.5 Summary and Discussion

In this chapter, bandwidth performance of PALNA matching networks was considered. First, fundamental, theoretical Bode-Fano limits on bandwidth performance of PALNA matching networks were computed assuming the availability of an infinite number of lossless components. Second, in addition to the Bode-Fano limits, another design metric suitable for benchmarking of practical, lossy MNs was introduced in terms of return loss at the antenna and a standard value of $|\Gamma| < 0.316$ was adopted as a design goal. Third, an updated PALNA design methodology was presented, which includes bandwidth as one of the design criteria, and the methodology was leveraged to investigate the performance of six PALNA topologies consisting of a finite number of lossy components.

Based on the design methodology Step 1 results, the performance of the PALNA

bandwidth enhancement topology 1 approaches the closest to the calculated Bode-Fano limits and exceeds the goal of $|\Gamma| < 0.316$ from 75 GHz to 110 GHz in both modes of operation with the highest amount of margin and with low loss. It was noted that PALNA bandwidth enhancement topology 1 is a circuit topology consisting primarily of lumped components. PALNA bandwidth enhancement topology 2, PALNA bandwidth enhancement topology 3, and PALNA bandwidth enhancement topology 4 leverage multi-section transmission line transformers for PA MN implementations. Traditionally, multi-section transmission line transformers have been implemented using transmission line segments that are of $\lambda/4$ length, which are very long and would result in a substantial amount of loss if used in a PALNA MN. Therefore, Step 1 procedure explored using multi-section transformers consisting of transmission lines of arbitrary length, which could be shorter than $\lambda/4$ and much less lossy [49]. However, as is shown in [49], the reduced transformer length comes at a cost of high transmission line impedance ratios, for example $m = Z_2 / Z_1 = 38$ in [49]. Considering that the maximum transmission line impedance ratio that can be achieved in the 32SOI process is approximately $m = 70\ \Omega / 20\ \Omega = 3.5$, multi-section transmission line transformers that can be implemented in 32SOI understandably have limited performance, as was seen from the results presented in section 6.2.

PALNA bandwidth enhancement topology 5 leverages a short-step-stub impedance transformer for PA MN implementation, which can in theory be very compact and low-loss [50]. However, similar to [49], it is seen in [50] that a ratio of 14 is required between the highest and the lowest characteristic impedances, which is not obtainable in 32SOI. Therefore, the performance of PALNA bandwidth enhancement topology 5 that was implemented under the assumption of the 32SOI process limitations, as seen in section 6.2, is understandably limited.

PALNA bandwidth enhancement topology 1 achieved the best performance in Step 1 of the PALNA design methodology (see Table 6.1 above) and was subsequently implemented in Cadence using EM modeled components as part of Step 2 of the design methodology. After Step 2 was completed, the $|\Gamma| < 0.316$ criterion is met by the optimized PALNA bandwidth enhancement topology 1 from 75.8 GHz to 107 GHz in the receive mode and

from 71.9 GHz to 103.7 GHz in the transmit mode. With some further optimization for bandwidth performance, PALNA bandwidth enhancement topology 1 bandwidth was expanded to achieve $|\Gamma| < 0.316$ from 77.1 GHz to 112.2 GHz in the receive mode and from 73.8 GHz to 107.5 GHz in the transmit mode, while sacrificing an increase of 0.4 dB in the transmit mode transducer loss.

After Step 2 of the PALNA design procedure was completed, the PALNA MN was integrated with the PA and LNA cells and simulated for completeness. The PALNA performance results were analyzed, noting that the bandwidth limitations of the cells limit the bandwidth performance of the PALNA. In future PALNA designs, bandwidth performance of the cells will have to be taken into account if a wideband PALNA is needed.

In conclusion, PALNA bandwidth performance can be formally included as an objective in the PALNA design methodology presented in Fig. 5.3. As was described in this chapter, bandwidth metrics can be defined in each mode of circuit operation and bandwidth performance can be evaluated as an additional objective function during each iteration in the design methodology, ensuring that the final PALNA solution achieves the desired overall optimum performance.

Chapter Seven: **Conclusions and Future Work**

7.1 Summary and Contributions

In this dissertation, silicon-based T/R circuits for integrated millimeter wave phased arrays are considered, with a primary focus on switchless PALNA T/R circuit architectures. A methodology for loss-aware PALNA matching network design was proposed and implemented, which provides the optimally matched impedances to both the LNA and the PA with minimal losses. The LNA input matching network and the PA output matching network are integrated into the PALNA MN for minimum overall loss. The following contributions are made to the advancement of integrated T/R circuit design.

- A switching-mode-like PA design approach was demonstrated at 94 GHz and used to design an efficient, switch-based T/R circuit in 32SOI technology. With maximum power added efficiency of 15 % in transmit and noise figure of 6.5 dB in receive at 94 GHz in simulation, the circuit performance significantly exceeded the published state-of-the-art.

- A switchless PALNA circuit in 32SOI technology was demonstrated, by leveraging PA and LNA circuits with 50 Ω matching networks, with loss of ~ 1.5 dB in transmit and receive modes of operation. This is less than the 2.2 dB loss expected if an SPDT switch is used. Therefore, even for designs where PA and LNA with 50 Ω matching networks are used, it is still advantageous to design a switchless PALNA circuit rather than use the switch.

- A manual, Cadence-only-based switchless PALNA design methodology was initially used. While it is possible to design and optimize PALNA circuits manually in Cadence and achieve state-of-the-art performance, it is shown that manual PALNA design is a time consuming, laborious, and painful process whose outcome may not be the most optimal PALNA circuit.

- A formal, general, loss-aware PALNA design methodology was developed and demonstrated. The methodology was applied to design and demonstrate a PALNA circuit in 32SOI technology with PAE of 18% which, despite having a 2.6 dB transducer loss in the transmit mode of operation that exceeds the 2.2 dB loss of an SPDT switch, achieves better PAE performance than the equivalent switch-based T/R circuit. This is possible because PALNA eliminated the intermediary 50 Ω matching networks. Also, the PALNA is physically smaller than the equivalent switch-based T/R circuit. Therefore, it was demonstrated that the design of PALNAs is advantageous in comparison to switch-based T/R circuits, because they can achieve better performance and because they can save valuable die real estate. Additionally, it was demonstrated that PALNA bandwidth performance can be formally included as an objective in the PALNA design methodology, making it possible to design PALNAs for an optimum tradeoff between bandwidth performance and other performance criteria (e.g., transducer loss).

7.2 Automated RF Circuit/System Synthesis: The “Holy Grail” of RF Design

Over the past two decades, the field of digital circuit design has experienced dramatic gains in productivity, enabling digital circuit designer teams to fully leverage the ever-increasing numbers of on-chip transistors made available through transistor scaling [52]. A key factor in these designer productivity gains has been the progress in the area of digital logic synthesis, which has become systematic, structured, and highly automated [52]. Unlike digital logic synthesis, the synthesis of RF circuits generally still requires the use of accurate and time-consuming EM simulations for modeling of passive components and a significant amount of custom “human in the loop” work by the design expert in order to achieve an optimal balance between a multitude of conflicting performance requirements. With the trend towards growing RF design complexities and shortening times to market (e.g., SoCs for 5G wireless communications and the Internet of Things), the highly custom nature of RF circuit design has motivated the need for new RF circuit design tools and methods that would enable RF circuit designers to increase their capabilities and productivity [53]. Thus, the area of automated RF circuit synthesis, including the development of the associated tools, has been an active area of academic research [53], [54].

The envisioned goal of automated RF circuit synthesis is to automatically determine the optimum values of parameters of a large RF system (e.g., capacitances, inductances, transmission line dimensions, transistor sizes and bias points, etc.), given the RF circuit/system schematic and performance specifications, such that the circuit/system meets the specifications at an optimal cost [54]. Fig. 7.1 depicts the general flow of this optimization-based RF circuit/system synthesis. In this model, the optimization engine determines the optimum circuit/system parameter values and the evaluation engine provides performance assessment.

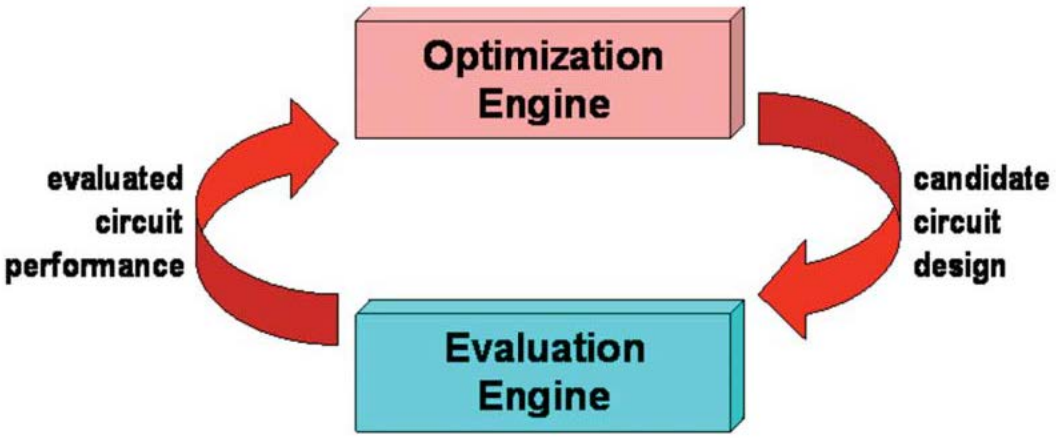


Fig. 7.1. Flow of optimization-based RF circuit/system synthesis [54].

RF circuits/systems are typically constructed using a hierarchical approach. For example, a PLL is typically assembled using four components: phase detector, loop filter, VCO, and fractional-N divider. In turn, a VCO is assembled using one or more transistors and multiple passive devices, all of which typically require EM simulation modelling. In order for the system-level performance requirements to be met (e.g., PLL phase noise), component level requirements must be met (e.g., VCO close-in phase noise), which are functions of a multitude of sub-component performance characteristics (e.g., device switching characteristics). Thus, overall, a RF circuit/system design typically incorporates a large number of variable degrees of freedom and a large number of related, continuous-valued performance requirements across the multiple levels of the system's intrinsic design hierarchy.

Due to the large number of degrees of freedom and complex dependencies, it is generally recognized that synthesizing and optimizing RF systems, as described above, is not feasible if they are considered "flat". Further, it has been recognized in the research community that the intrinsically hierarchical structure of RF systems not only requires but can also greatly benefit from hierarchical design tools, where the performance of various individual circuit/system component blocks can be abstracted, modeled, verified, and leveraged for simulation and verification of the overall system [54]. Therefore, development of hierarchical design tools has been the focus of the research community.

The effectiveness of the hierarchical design approach depends on the availability of models that are good representations of the component circuit blocks. There are four major mathematical modeling techniques (i.e., system models) that are used in RF circuit/system design [54]:

1. Linear Time Invariant (LTI)
2. Linear Time Variant (LTV)
3. Nonoscillatory Nonlinear
4. Oscillatory

An overview description of each of these techniques can be found in [54].

It should be noted that the above listed circuit modeling approaches are generally "instance oriented", which means that the circuit models that they produce are valid for fully designed/specified circuit "instances" and that the models generally must be re-generated if any of the circuit variables are changed. This is generally undesirable and inefficient in situations such as the above-described optimization-based synthesis, where it is necessary to evaluate circuit performance across many instances of circuit parameter combinations. Therefore, the component circuit block parametric modeling approaches are being investigated, which describe the performance characteristics of the component block circuits such as gain, bandwidth, output power, etc. as a function of the circuit parameters such as capacitance, inductance, transmission line impedance/length, etc.) [54]. Parametric circuit modelling is an active area of academic research and summary overview of the modelling techniques can be found in [54].

So, given the availability of the "instance oriented" and "parametric" circuit modelling approaches, the above-described hierarchical, optimization-based automatic RF circuit/system synthesis methodologies can be implemented. These methodologies heavily leverage various numerical approaches for managing the circuit/system degrees of freedom while understanding the circuit/system performance tradeoffs. A summary overview of

several popular design methodologies is provided in [54], including: constraint-driven top-down methodology, hierarchical techniques based on ad hoc equation sets, Pareto front based techniques, and multi-objective bottom-up (MOBU) methodology. More detailed reporting on optimization-based automatic RF circuit/system synthesis methodologies is provided in [55] – [74].

As was mentioned above, the synthesis of RF circuits/systems typically requires the use of accurate and time-consuming EM simulations for modeling of passive components. However, in the context of the above-described hierarchical optimization-based synthesis, direct integration of EM simulation-based passive component synthesis into the overall circuit/system synthesis approach is prohibitive given the anticipated time-consumption of individual EM simulation runs. Therefore, significant effort has been dedicated in the research community to addressing the problem of passive component synthesis [75]. As explained in [75], there exists a fundamental tradeoff between the efficiency (i.e., as measured by algorithm execution time consumption) and accuracy (i.e., as measured by algorithm solution quality) of the passive component synthesis approaches. Fig. 7.2 illustrates this fundamental tradeoff graphically, where the ideal passive component synthesis approach would reside in the upper right corner of the chart, indicating both high efficiency and high solution quality. The shown algorithms are: Equivalent Circuit Model and Global Optimization (ECGO), EM-simulation and Global Optimization (EMGO), Surrogate EM-simulation and Global Optimization (SEMGO), Surrogate Model and Local Optimization (SMLO), and Memetic Machine Learning-based Differential Evolution (MMLDE). A summary description of each of these algorithms is provided in [75]. ECGO leverages equivalent circuit models to represent behavior of passive components. EMGO leverages EM simulations. SEMGO leverages a surrogate component model based, for example, on neural networks. SMLO leverages a locally optimized surrogate model derived from coarse and fine mesh EM simulations. MMLDE leverages an EM simulation trained surrogate model for rough component performance estimation in conjunction with an online surrogate-model-based evolutionary algorithm for improvement of accuracy and integration with the overall circuit optimization function.

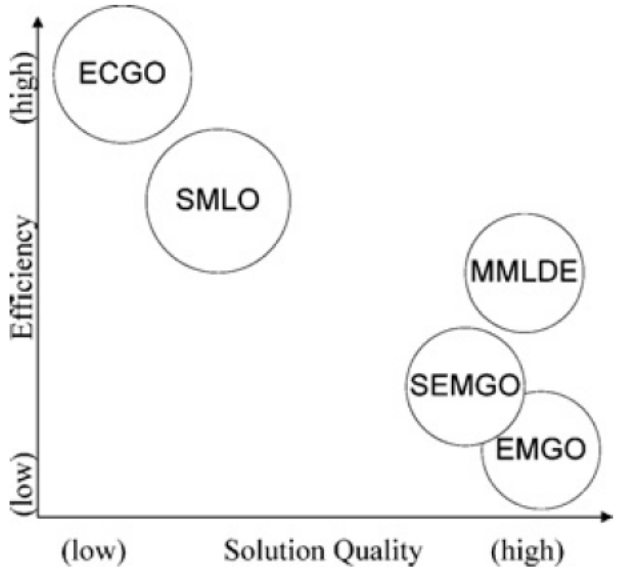


Fig. 7.2. The fundamental tradeoff between passive component synthesis approaches [75]. The shown algorithms are: Equivalent Circuit Model and Global Optimization (ECGO), EM-simulation and Global Optimization (EMGO), Surrogate EM-simulation and Global Optimization (SEMGO), Surrogate Model and Local Optimization (SMLO), and Memetic Machine Learning-based Differential Evolution (MMLDE).

Additional passive component synthesis surrogate modeling approaches reported in literature, which are based on neural networks, support vector machines, parametric models, or Kriging functions, are described in [76].

Academic research is continuing to explore approaches to overcoming the fundamental efficiency-accuracy tradeoff in the area of optimization-based automatic RF circuit/system synthesis. Particularly promising are recent approaches that synthesize good passive component surrogate models offline (i.e., prior to beginning circuit optimization) using parametric Pareto front approach [77] and integrate the RF circuits/systems in a bottom-up optimization approach across multiple hierarchical levels [78]. However, further research is needed at frequencies above ~2.5 GHz and for a broader set of example circuits.

More generally, based on research presented in open literature, the research trends of combining global optimization techniques with EM simulations to achieve accuracy, and leveraging machine learning techniques to improve efficiency are promising. And, achieving effective integration of these three techniques to realize the dream and the

promise of automated RF circuit/system synthesis is expected to remain a significant challenge and an active area of academic research for the foreseeable future.

7.3 Remarks on Device Modelling

High-speed/RF MOSFET models may be based on the assumption of quasi-static or non-quasi-static (NQS) device operation. In quasi-static device operation, the charge densities at any position in the channel are assumed to depend on the instantaneous values of the terminal voltages only [79]. When the device terminal voltages vary rapidly, however, such as in the design of millimeter wave RF circuits, the quasi-static assumption is invalid and a distributed, or NQS, device model must be used [79].

The Berkeley Short-channel IGFET Model (BSIM) group develops physics-based MOSFET SPICE models for circuit simulation and CMOS technology development [80]. BSIM group started device modelling in the 1980s and has since developed several industry standard MOSFET models that have been widely used by major semiconductor companies and design houses [81]. An overview description of the evolution of BSIM family of MOSFET models is provided in [81].

In order to be useful for the design of millimeter wave RF circuits, the well-known BSIM models have generally accounted for NQS device behavior [82], [83]. And, in order to fully define a NQS model of a MOSFET device such that the model may be used in RF circuit design, measured s-parameters data of the device itself is required [84].

Researchers are actively working to determine the frequency of operation at which NQS device behavior emerges and two criteria involving transadmittance efficiency were recently proposed [85]. According to one of those criteria, the 10^{o} phase shift of the transadmittance efficiency, NQS behavior of a 28 nm nMOS SOI transistor becomes prominent at around 40 GHz [85]. Similar research data is not available for the 32SOI process used in this work, however it is strongly suspected that at the operating frequency of 94 GHz NQS behavior of 32SOI nMOS transistors is prominent and requires careful

modeling based on measured transistor s-parameter data.

The device models used in GlobalFoundries' 32SOI plug-in developer's kit (PDK) are based on the BSIMSOI4.3.1 MOSFET models, which are built assuming quasi-static device behavior [86]. These device models may be sufficient for many circuit design applications of potential interest however, for the reasons discussed above, it is strongly suspected that these device models are not suitable for analog/RF circuit design at 94 GHz. Since the NQS model is not available in GlobalFoundries' 32SOI PDK, it is strongly recommended in future millimeter wave analog/RF circuit designs that the 32SOI devices be modelled using measured s-parameters files at desired device bias levels.

7.4 Future Work

The PALNA design methodology work presented in this dissertation, and particularly in Chapter 5 and Chapter 6, was verified through MATLAB and Cadence simulations involving a high degree of "designer-in-the-loop" participation. Improving the design methodology in a way that would minimize or eliminate the need for designer intervention would be an important step in future work. In this regard, approaches discussed in section 7.2 should be considered. A particularly important aspect is the improvement of computational efficiency, which is currently low due to the difficulty of leveraging traditional optimization methods (i.e., since computing the transducer loss objective function gradient is very difficult, as discussed in Appendix A) and the need to resort to a nested search approach that is essentially of a combinatorial optimization nature. In general, combinatorial optimization problems have been solved using neural networks (Hopfield networks and self-organizing maps) and genetic algorithms [87], [88]. So, it would be important to investigate how to represent the PALNA MN design problem in a way that is efficiently solvable by these alternative approaches.

Since linearity was less important for near-term system applications considered, linearity was not used as a PALNA optimization objective in this dissertation work. Therefore, linearity is one research avenue that should be considered in future PALNA research.

Table 5.6 provides insights into the origins of PALNA MN losses and suggests possible approaches for loss reduction in future PALNA designs. In particular, future research should focus on two approaches. First, it is noted in Table 5.6 that the PA conjugate mismatch loss is 1.08 dB, whereas LNA conjugate mismatch loss is only 0.22 dB. While the use of the gain circles to select the optimum LNA source impedance ensures that the LNA input conjugate mismatch loss is low, the optimum PA load impedance was chosen for maximum PAE only. Since, in general, optimum PA load impedances required for maximum PAE and minimum conjugate mismatch loss are different, future research should pursue two paths: (1) How to design PA cores in which the output matching requirements for maximum PAE and minimum conjugate output mismatch loss coincide; (2) How to choose an optimum PA load impedance that provides the most favorable tradeoff between PAE and loss built into the PALNA MN due to conjugate mismatch loss at PA output. Second, the presented PALNA MN optimization approaches for both modes of operation should be leveraged to explore additional PALNA topologies that maximize power transfer efficiency, thereby minimizing the amount of power dissipated in the PALNA MN itself.

Finally, future work should address the tapeout and measurement of bandwidth-extended PALNA circuits discussed in Chapter 6. The PA and LNA cells leveraged in the PALNAs should be redesigned using new transistor models based on measured s-parameters of the transistors, as discussed in section 7.3. And, the designs can be ported to other advanced non-SOI CMOS technologies, such as the 28 nm CMOS process.

7.5 List of Publications

[1] I. Abdomerovic and S. Raman, "A Millimeter Wave Loss-Aware Methodology for Switchless PALNA Integrated Circuit Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, accepted for publication in 2018.

[2] I. Abdomerovic, K. J. Koh, M. Sayginer, G. Rebeiz, and S. Raman, "An Efficient 94 GHz Switched T/R Circuit Design in 32SOI Technology," *Proceedings of the*

Government Microcircuit Applications and Critical Technology Conference (GOMAC Tech), March 2018.

[3] W. D. Palmer, I. Abdomerovic, P. M. Asbeck, T. LaRocca, and S. Raman, "Advancing Silicon mm-wave Transmitter ICs for Satellite Communications," *Proceedings of the IEEE International Microwave and RF Conference (IMaRC)*, 2014.

[4] I. Abdomerovic, W. D. Palmer, P. M. Watson, R. Worley, and S. Raman, "Leveraging Integration: Toward Efficient Linearized All-Silicon IC Transmitters," *IEEE Microwave Magazine*, vol. 15, no. 3, pp.86–96, May 2014.

Appendix A: Remarks on Optimization

Assuming that the PALNA design problem can be formulated as an optimization problem, the formulation would involve the following [88]:

1. Selection of optimization variables,
2. Definition of an objective function, and
3. Identification of constraints.

Assuming further that a particular PALNA topology is selected, the PALNA optimization variables would be the values associated with the capacitors, inductors, and the transmission lines needed to implement the PALNA circuit (i.e., capacitances, inductances, transmission line impedances, transmission line lengths). The loss factors associated with the optimization variables are not optimization variables themselves, since they are functions of the optimization variables as shown in Fig. 5.1 and Fig. 5.2. The PALNA topology may also be considered an optimization variable, however it is considered to be fixed in this discussion for simplicity and without the loss of generality.

The PALNA design has four basic objectives:

1. Achieve impedance match in the transmit mode
2. Achieve impedance match in the receive mode
3. Minimize the transducer loss in the transmit mode
4. Minimize the transducer loss in the receive mode

Additional objectives may also be stated, for example, to maximize linearity or operational bandwidth. The objective function for optimization purposes would be defined as a composite function incorporating mathematical expressions of these objectives. It should be noted that the objectives stated above may trade off against each other and therefore the PALNA design would be considered a fundamentally difficult optimization problem [88].

The PALNA optimization constraints would consist of mathematical expressions quantifying the following:

1. Range of capacitance values realizable in the given process
2. Range of inductance values realizable in the given process
3. Range of transmission line impedance values realizable in the given process
4. Capacitor loss, which is a function of capacitance
5. Inductor loss, which is a function of inductance
6. Transmission line loss, which is a function of transmission line length

Next, in order to solve the PALNA design optimization problem, the objective function must be expressed mathematically in terms of the optimization variables. For simplicity, it is assumed here that the objective function to be maximized is given by the transducer gain expression given in (5.14). Assuming transmit mode of operation,

$$Z_{in} = \frac{A_{TX}Z_L + B_{TX}}{C_{TX}Z_L + D_{TX}} \qquad (A.1)$$

where the [ABCD] matrix values are given in (5.1). Using (5.7), the expression in (5.14)

may be rewritten as

$$G_{transducer} = \frac{4R_G R_L}{|A_{TX}Z_L + B_{TX} + Z_G(C_{TX}Z_L + D_{TX})|^2} \qquad (A.2)$$

Assuming a PALNA topology shown in Fig. 5.13, substitution of [ABCD] matrix values, expressed in terms of the above-described optimization variables (Z_4, l_4, L_2, L_3, C_3, and C_4), into (A.2) can be done. Fig. A.1 shows the substitution steps needed to express the transducer gain in terms of the optimization variables.

Next, after the objective function (i.e., transducer gain) is expressed in terms of the optimization variables, solution of the PALNA design optimization problem requires computation of its gradient

$$\nabla f_{OBJ} = \begin{pmatrix} \frac{\partial f_{OBJ}}{\partial x_1} \\ \vdots \\ \frac{\partial f_{OBJ}}{\partial x_n} \end{pmatrix} \qquad (A.3)$$

and its Hessian

$$\nabla^2 f_{OBJ} = \begin{pmatrix} \frac{\partial^2 f_{OBJ}}{\partial x_1^2} & \cdots & \frac{\partial^2 f_{OBJ}}{\partial x_1 \partial x_n} \\ \vdots & \ddots & \vdots \\ \frac{\partial^2 f_{OBJ}}{\partial x_n \partial x_2} & \cdots & \frac{\partial^2 f_{OBJ}}{\partial x_n^2} \end{pmatrix} \qquad (A.4)$$

where $f_{OBJ} = G_{transducer}$ and $x_1 \ldots x_n$ represent the optimization variables. However, this is very difficult because the transducer gain is a very complex, transcendental expression and not easily differentiable. Therefore, traditional optimization methods cannot be used to solve the PALNA design problem and a combinatorial optimization approach (such as pursued in this work) must be pursued instead [88].

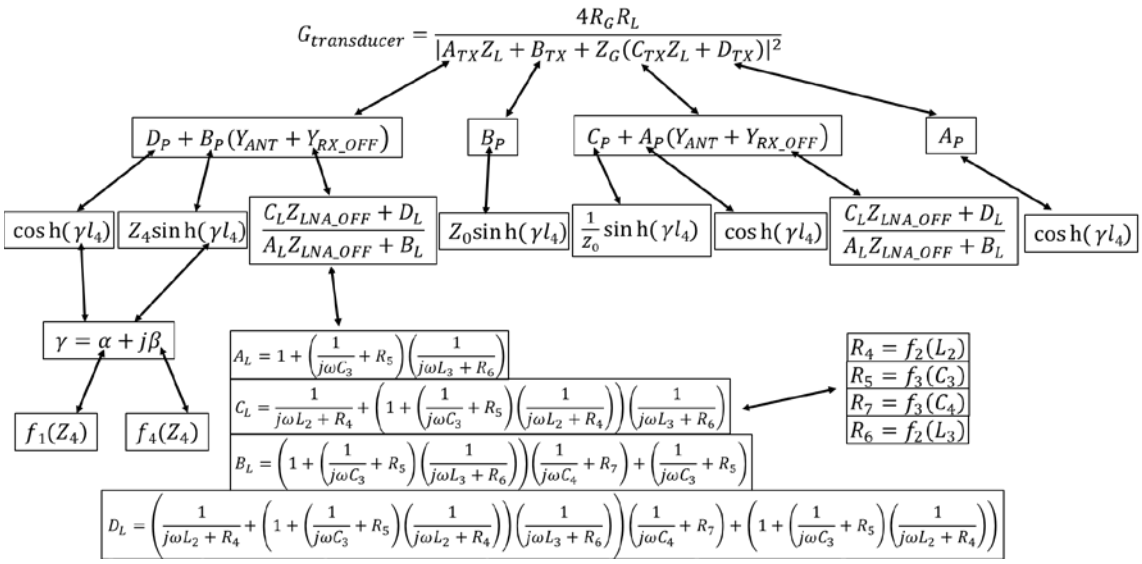


Fig. A.1. Substitution steps required to express the transducer gain in terms of the optimization variables Z_4, l_4, L_2, L_3, C_3, and C_4.

Further, due to the need for accurate EM simulation models of passive components and the need to iteratively optimize the PALNA circuits in Cadence, the PALNA design methodology can only be semi-autonomous at this time. A fully automated design of PALNA circuits is a subject to be considered in future work.

Appendix B: MATLAB Source Code

B.1 MATLAB Search Script for PALNA Topology Shown in Fig. 5.13

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 5.13
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%*************************************************************************************************

clear all;

% Receive mode impedances
Z_opt_LNA=172+j*21;               % LNA ON
%Z_opt_LNA=150+j*25;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
Z_opt_PA=105+j*14;                % PA ON
%Z_opt_PA=90;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod2_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

for Z_pa = 20:2:70    % PA MN components
   for L1 = -pi/2:pi/50:pi/2

% PA MN - transmission line
zp=Z_pa;
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
```

```
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D


for L = 50:10:100     % LNA MN components
   for C1r = 15:2:25
      for Lr = 60:10:150
         for C2r = 15:2:25

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/10000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/10000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% Calculate and plot impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-10 & real(Z_rx_l)<=real(Z_opt_LNA)+10 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-10 & imag(Z_rx_l)<=imag(Z_opt_LNA)+10 & real(Z_tx_p)>=real(Z_opt_PA)-10
& real(Z_tx_p)<=real(Z_opt_PA)+10 & imag(Z_tx_p)>=imag(Z_opt_PA)-10 & imag(Z_tx_p)<=imag(Z_opt_PA)+10
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
```

```
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl1=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp1=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl1*zp1)/(zl1+zp1);
    % Transmit mode
    zl1=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp1=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl1*zp1)/(zl1+zp1);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % 1. PALNA MN components
    fprintf(fid,'======================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L, C1r, Lr, C2r,
iteration_count);

    % 2. Mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    count=count+1;

   end

end
end
end
end
end
end

count

fclose(fid);
```

B.2 MATLAB Search Script for PALNA Topology Shown in Fig. 5.13 With Bandwidth Metric Calculations Included

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 5.13
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod3_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;


for Z_pa = 20:2:70    % PA MN components
   for L1 = -pi/2:pi/50:pi/2

% PA MN - transmission line
zp=Z_pa;
tp=L1;
if tp>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D


for L = 50:10:100     % LNA MN components
   for C1r = 15:2:25
      for Lr = 60:10:150
         for C2r = 15:2:25

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
```

```
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate and plot impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-10 & real(Z_rx_l)<=real(Z_opt_LNA)+10 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-10 & imag(Z_rx_l)<=imag(Z_opt_LNA)+10 & real(Z_tx_p)>=real(Z_opt_PA)-10
& real(Z_tx_p)<=real(Z_opt_PA)+10 & imag(Z_tx_p)>=imag(Z_opt_PA)-10 & imag(Z_tx_p)<=imag(Z_opt_PA)+10
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl1=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp1=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl1*zp1)/(zl1+zp1);
    % Transmit mode
    zl1=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp1=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl1*zp1)/(zl1+zp1);
```

```
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwith metric
    index=1;
    tp1=tp;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tp2=tp1*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gp1=ap+j*tp2;
       p1(1,1)=cosh(gp1);            % A
       p1(1,2)=zp*sinh(gp1);         % B
       p1(2,1)=(1/zp)*sinh(gp1);     % C
       p1(2,2)=cosh(gp1);            % D
       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(p1(1,1)*Z_load_PA+p1(1,2))/(p1(2,1)*Z_load_PA+p1(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(p1(1,1)*Z_out_PA+p1(1,2))/(p1(2,1)*Z_out_PA+p1(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L, C1r, Lr, C2r,
iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);

    count=count+1;

   end

end
end
end
end
end
```

```
end

count

fclose(fid);
```

B.3 MATLAB Search Script for PALNA Topology Shown in Fig. 6.9

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.9
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod5a_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;


% PA MN components
for L0 = 40:10:100
   for C1r0 = 15:2:35

% PM MN - LC
ind10=L0/1000000000000;   %pH
esr10=0.0521*L0-0.892;    % interpolated ESR value
cap10=C1r0/1000000000000000; %fF
esr20=(-0.036)*C1r0+1.566; % interpolated ESR value
ll10=[1 esr10+s*ind10;0 1];
lc10=[1 0;1/(esr20+1/(s*cap10)) 1];
p=ll10*lc10; %[ABCD]

for L = 50:10:200     % LNA MN components
   for C1r = 15:2:25
      for Lr = 100:10:160
         for C2r = 15:2:45

% LNA MN - LC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
```

```
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl1=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp1=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl1*zp1)/(zl1+zp1);
    % Transmit mode
    zl1=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp1=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl1*zp1)/(zl1+zp1);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
```

```
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwith metric
    index=1;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - LC
       ll12=[1 esr10+s1*ind10;0 1];
       lc12=[1 0;1/(esr20+1/(s1*cap10)) 1];
       p2=ll12*lc12; %[ABCD]
       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(p2(1,1)*Z_load_PA+p2(1,2))/(p2(2,1)*Z_load_PA+p2(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(p2(1,1)*Z_out_PA+p2(1,2))/(p2(2,1)*Z_out_PA+p2(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L0, C1r0, L, C1r, Lr, C2r,
iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);


    count=count+1;

   end

end
end
end
end
end
end

count

fclose(fid);
```

B.4 MATLAB Search Script for PALNA Topology Shown in Fig. 6.11

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.11
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
Z_opt_PA=105+j*14;              % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod6_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;


for Z_pa = 20:2:70    % PA MN components
   for L1 = -pi/2:pi/50:pi/2
      for Z_pa1 = 20:2:70
         for L11 = -pi/2:pi/50:pi/2

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D


zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
```

```
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

p=p*p1;   % update p ABCD matrix

for L = 50:10:100     % LNA MN components
   for C1r = 15:2:25
      for Lr = 60:10:150
         for C2r = 15:2:25

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-10 & real(Z_rx_l)<=real(Z_opt_LNA)+10 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-10 & imag(Z_rx_l)<=imag(Z_opt_LNA)+10 & real(Z_tx_p)>=real(Z_opt_PA)-10
& real(Z_tx_p)<=real(Z_opt_PA)+10 & imag(Z_tx_p)>=imag(Z_opt_PA)-10 & imag(Z_tx_p)<=imag(Z_opt_PA)+10
   % Potential solution => calculate and store quantities of interest

    % calculate losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
```

```
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/940000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/940000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D

       pp=pp*pp1;   % update pp ABCD matrix

       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
```

```
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'============================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L11, Z_pa1, L, C1r,
Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);

    count=count+1;

   end

end
end
end
end
end
end
end
end

count

fclose(fid);
```

B.5 MATLAB Search Script for PALNA Topology Shown in Fig. 6.11 With Constant LNA MN Component Values

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.11
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;              % LNA ON
Z_opt_LNA=172+j*21;              % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;               % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod6a_a.txt','w');
```

```
f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;


% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

for Z_pa = 20:2:70    % PA MN components
   for L1 = 0:pi/50:pi/2  %restricted TL lengths to positive values for shorter length and lower loss
      for Z_pa1 = 20:2:70
         for L11 = 0:pi/50:pi/2

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

p=p*p1;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
```

```
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwith metric
    index=1;
    tp0=tp;
```

```
    tp10=tp1;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/940000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/940000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D

       pp=pp*pp1;   % update pp ABCD matrix

       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L11, Z_pa1, L, C1r,
Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);

    count=count+1;

   end

end
end
end
end


count
```

```
fclose(fid);
```

B.6 MATLAB Search Script for PALNA Topology Shown in Fig. 6.11 With Constant LNA MN Component Values and Randomized TL Lengths

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.11
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%       Note 6: TL lengths are randomized for speed of execution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod6b_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;


% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]
```

```
for Z_pa = 20:2:70    % PA MN components
   for Z_pa1 = 20:2:70
L1 = (pi/2)*rand;  % restricted TL lengths to positive values only for shorter length and lower loss
L11 = (pi/2)*rand;

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

p=p*p1;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
```

```
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D

       pp=pp*pp1;   % update pp ABCD matrix

       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
```

```
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L11, Z_pa1, L, C1r,
Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);

    count=count+1;

   end

end
end



count

fclose(fid);
```

B.7 MATLAB Search Script for PALNA Topology Shown in Fig. 6.13 With Constant LNA MN Component Values and Randomized TL Lengths

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.13
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%       Note 6: TL lengths are randomized for speed of execution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;              % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod7_temp_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

for num=1:1:500 % repeat 500 times

for Z_pa = 20:2:70    % PA MN components
   for Z_pa1 = 20:2:70
      for Z_pa2 = 20:2:70

L1 = (pi/2)*rand;  % restricted TL lengths to positive values only for shorter length and lower loss
L11 = (pi/2)*rand;
```

```
L12 = (pi/2)*rand;

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

zp2=Z_pa2;  % TL segment 3
tp2=L12;
if tp2>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len2=L12*(3245/2)/6.28;
else
    phys_len2=L12*(3245/2)/6.28+3245/2;
end
if zp2<=38            % calculate TL attenuation constant, alpha
    alpha2=0.0000909;
elseif (zp2>38 & zp2<=50)
    alpha2=(0.00000025)*zp2+0.0000814;
else
    alpha2=(0.00000093)*zp2+0.0000474;
end
ap2=alpha2*phys_len2;
gp2=ap2+j*tp2;
p2(1,1)=cosh(gp2);            % A
p2(1,2)=zp2*sinh(gp2);         % B
p2(2,1)=(1/zp2)*sinh(gp2);     % C
p2(2,2)=cosh(gp2);            % D

p=p*p1*p2;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
```

```
% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    tp20=tp2;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
```

```
        pp(2,1)=(1/zp)*sinh(gpp);     % C
        pp(2,2)=cosh(gpp);            % D

        tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
        gpp1=ap1+j*tpp1;
        pp1(1,1)=cosh(gpp1);            % A
        pp1(1,2)=zp1*sinh(gpp1);         % B
        pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
        pp1(2,2)=cosh(gpp1);            % D

        tpp2=tp20*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
        gpp2=ap2+j*tpp2;
        pp2(1,1)=cosh(gpp2);            % A
        pp2(1,2)=zp2*sinh(gpp2);         % B
        pp2(2,1)=(1/zp2)*sinh(gpp2);     % C
        pp2(2,2)=cosh(gpp2);            % D

        pp=pp*pp1*pp2;   % update pp ABCD matrix

        % LNA MN - LCLC
        ll11=[1 0; 1/(esr1+s1*ind1) 1];
        lc11=[1 esr2+1/(s1*cap1);0 1];
        ll21=[1 0; 1/(esr3+s1*ind2) 1];
        lc21=[1 esr4+1/(s1*cap2);0 1];
        l1=ll11*lc11*ll21*lc21; %[ABCD]
        % Reflection coefficients at the antenna
        % Receive mode
        zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
        zjr1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Rx1=zjr1/Z0;
        Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
        mrx = abs(Gamma_Rx);
        % Transmit mode
        zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
        zjt1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Tx1=zjt1/Z0;
        Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
        mtx = abs(Gamma_Tx);
        freq(index)=ct;             %frequency in GHz
        rc_rx(index)=mrx;
        rc_tx(index)=mtx;
        index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L11,
Z_pa1, L12, Z_pa2, L, C1r, Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);


    count=count+1;

   end

end
end
end

end %num loop

count

fclose(fid);
```

B.8 MATLAB Search Script for PALNA Topology Shown in Fig. 6.13 With Constant LNA MN Component Values

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.13
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod7a_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

for Z_pa = 46:2:52    % PA MN components
   for L1 = 0.5:pi/50:1.0  %Restricted TL lengths to positive values for shorter length and lower loss
      for Z_pa1 = 22:2:38
         for L11 = 0.04:pi/50:0.3
            for Z_pa2 = 44:2:68
               for L12 = 0.0:pi/50:0.3

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
```

```
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

zp2=Z_pa2;  % TL segment 3
tp2=L12;
if tp2>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len2=L12*(3245/2)/6.28;
else
    phys_len2=L12*(3245/2)/6.28+3245/2;
end
if zp2<=38            % calculate TL attenuation constant, alpha
    alpha2=0.0000909;
elseif (zp2>38 & zp2<=50)
    alpha2=(0.00000025)*zp2+0.0000814;
else
    alpha2=(0.00000093)*zp2+0.0000474;
end
ap2=alpha2*phys_len2;
gp2=ap2+j*tp2;
p2(1,1)=cosh(gp2);            % A
p2(1,2)=zp2*sinh(gp2);         % B
p2(2,1)=(1/zp2)*sinh(gp2);     % C
p2(2,2)=cosh(gp2);            % D

p=p*p1*p2;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;
```

```
   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    tp20=tp2;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D
```

```
        tpp2=tp20*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
        gpp2=ap2+j*tpp2;
        pp2(1,1)=cosh(gpp2);            % A
        pp2(1,2)=zp2*sinh(gpp2);         % B
        pp2(2,1)=(1/zp2)*sinh(gpp2);     % C
        pp2(2,2)=cosh(gpp2);            % D

        pp=pp*pp1*pp2;   % update pp ABCD matrix

        % LNA MN - LCLC
        ll11=[1 0; 1/(esr1+s1*ind1) 1];
        lc11=[1 esr2+1/(s1*cap1);0 1];
        ll21=[1 0; 1/(esr3+s1*ind2) 1];
        lc21=[1 esr4+1/(s1*cap2);0 1];
        l1=ll11*lc11*ll21*lc21; %[ABCD]
        % Reflection coefficients at the antenna
        % Receive mode
        zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
        zjr1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Rx1=zjr1/Z0;
        Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
        mrx = abs(Gamma_Rx);
        % Transmit mode
        zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
        zjt1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Tx1=zjt1/Z0;
        Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
        mtx = abs(Gamma_Tx);
        freq(index)=ct;             %frequency in GHz
        rc_rx(index)=mrx;
        rc_tx(index)=mtx;
        index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1, Z_pa, L11,
Z_pa1, L12, Z_pa2, L, C1r, Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);


    count=count+1;

   end

end
end
end
end
end
end

count

fclose(fid);
```

B.9 MATLAB Search Script for PALNA Topology Shown in Fig. 6.15 With Constant LNA MN Component Values and Randomized TL Lengths

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.15
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%       Note 6: TL lengths are randomized for speed of execution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod8_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;


% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/10000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/10000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]


for num=1:1:1 % repeat 1 times


for Z_pa = 20:2:70    % PA MN components
   for Z_pa1 = 20:2:70
      for Z_pa2 = 20:2:70
```

```
          for Z_pa3 = 20:2:70

L1 = (pi/2)*rand;  % restricted TL lengths to positive values only for shorter length and lower loss
L11 = (pi/2)*rand;
L12 = (pi/2)*rand;
L13 = (pi/2)*rand;

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

zp2=Z_pa2;  % TL segment 3
tp2=L12;
if tp2>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len2=L12*(3245/2)/6.28;
else
    phys_len2=L12*(3245/2)/6.28+3245/2;
end
if zp2<=38            % calculate TL attenuation constant, alpha
    alpha2=0.0000909;
elseif (zp2>38 & zp2<=50)
    alpha2=(0.00000025)*zp2+0.0000814;
else
    alpha2=(0.00000093)*zp2+0.0000474;
end
ap2=alpha2*phys_len2;
gp2=ap2+j*tp2;
p2(1,1)=cosh(gp2);            % A
p2(1,2)=zp2*sinh(gp2);         % B
p2(2,1)=(1/zp2)*sinh(gp2);     % C
p2(2,2)=cosh(gp2);            % D

zp3=Z_pa3;  % TL segment 4
tp3=L13;
if tp3>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len3=L13*(3245/2)/6.28;
else
    phys_len3=L13*(3245/2)/6.28+3245/2;
end
if zp3<=38            % calculate TL attenuation constant, alpha
    alpha3=0.0000909;
elseif (zp3>38 & zp3<=50)
```

```
    alpha3=(0.00000025)*zp3+0.0000814;
else
    alpha3=(0.00000093)*zp3+0.0000474;
end
ap3=alpha3*phys_len3;
gp3=ap3+j*tp3;
p3(1,1)=cosh(gp3);            % A
p3(1,2)=zp3*sinh(gp3);         % B
p3(2,1)=(1/zp3)*sinh(gp3);     % C
p3(2,2)=cosh(gp3);            % D

p=p*p1*p2*p3;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
```

```
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    tp20=tp2;
    tp30=tp3;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D

       tpp2=tp20*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp2=ap2+j*tpp2;
       pp2(1,1)=cosh(gpp2);            % A
       pp2(1,2)=zp2*sinh(gpp2);         % B
       pp2(2,1)=(1/zp2)*sinh(gpp2);     % C
       pp2(2,2)=cosh(gpp2);            % D

       tpp3=tp30*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp3=ap3+j*tpp3;
       pp3(1,1)=cosh(gpp3);            % A
       pp3(1,2)=zp3*sinh(gpp3);         % B
       pp3(2,1)=(1/zp3)*sinh(gpp3);     % C
       pp3(2,2)=cosh(gpp3);            % D

       pp=pp*pp1*pp2*pp3;   % update pp ABCD matrix

       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
       lc11=[1 esr2+1/(s1*cap1);0 1];
       ll21=[1 0; 1/(esr3+s1*ind2) 1];
       lc21=[1 esr4+1/(s1*cap2);0 1];
       l1=ll11*lc11*ll21*lc21; %[ABCD]
       % Reflection coefficients at the antenna
       % Receive mode
       zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
       zjr1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;             %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
```

```
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1,
Z_pa, L11, Z_pa1, L12, Z_pa2, L13, Z_pa3, L, C1r, Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);

    count=count+1;

   end

end
end
end
end

end %num loop

count

fclose(fid);
```

B.10 MATLAB Search Script for PALNA Topology Shown in Fig. 6.15 With Constant LNA MN Component Values

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.15
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;               % LNA ON
Z_opt_LNA=172+j*21;               % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;                % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod8a_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;
```

```
count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;
C2r = 20;

% LNA MN - LCLC
ind1=L/1000000000000;   %pH
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/10000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/10000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

for Z_pa = 38:2:45    % PA MN components
   for L1 = 0:pi/50:0.1   %restricted TL lengths to positive values for shorter length and lower loss
      for Z_pa1 = 50:2:60
         for L11 = 0.3:pi/50:0.7
            for Z_pa2 = 50:2:60
               for L12 = 0:pi/50:0.2
                  for Z_pa3 = 24:2:34
                     for L13 = 0.1:pi/50:0.3

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=cosh(gp1);            % A
p1(1,2)=zp1*sinh(gp1);         % B
p1(2,1)=(1/zp1)*sinh(gp1);     % C
p1(2,2)=cosh(gp1);            % D

zp2=Z_pa2;  % TL segment 3
tp2=L12;
if tp2>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len2=L12*(3245/2)/6.28;
else
```

```
    phys_len2=L12*(3245/2)/6.28+3245/2;
end
if zp2<=38            % calculate TL attenuation constant, alpha
    alpha2=0.0000909;
elseif (zp2>38 & zp2<=50)
    alpha2=(0.00000025)*zp2+0.0000814;
else
    alpha2=(0.00000093)*zp2+0.0000474;
end
ap2=alpha2*phys_len2;
gp2=ap2+j*tp2;
p2(1,1)=cosh(gp2);            % A
p2(1,2)=zp2*sinh(gp2);         % B
p2(2,1)=(1/zp2)*sinh(gp2);     % C
p2(2,2)=cosh(gp2);            % D

zp3=Z_pa3;  % TL segment 4
tp3=L13;
if tp3>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len3=L13*(3245/2)/6.28;
else
    phys_len3=L13*(3245/2)/6.28+3245/2;
end
if zp3<=38            % calculate TL attenuation constant, alpha
    alpha3=0.0000909;
elseif (zp3>38 & zp3<=50)
    alpha3=(0.00000025)*zp3+0.0000814;
else
    alpha3=(0.00000093)*zp3+0.0000474;
end
ap3=alpha3*phys_len3;
gp3=ap3+j*tp3;
p3(1,1)=cosh(gp3);            % A
p3(1,2)=zp3*sinh(gp3);         % B
p3(2,1)=(1/zp3)*sinh(gp3);     % C
p3(2,2)=cosh(gp3);            % D

p=p*p1*p2*p3;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-15 & real(Z_rx_l)<=real(Z_opt_LNA)+15 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-15 & imag(Z_rx_l)<=imag(Z_opt_LNA)+15 & real(Z_tx_p)>=real(Z_opt_PA)-15
& real(Z_tx_p)<=real(Z_opt_PA)+15 & imag(Z_tx_p)>=imag(Z_opt_PA)-15 & imag(Z_tx_p)<=imag(Z_opt_PA)+15
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
```

```
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
    zm_rx(2,1)=1/C_rx;
    zm_rx(2,2)=D_rx/C_rx;
    kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
    theta_rx=atan(kQ_rx)/2;
    eta_rx=tan(theta_rx)^2;
    loss_rx=10*log10(eta_rx);    % in dB

    % Mismatch losses at the amplifiers
    MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
    MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

    % Mismatch losses at the antenna
    % Receive mode
    zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
    zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
    zjr=(zl10*zp10)/(zl10+zp10);
    % Transmit mode
    zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
    zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
    zjt=(zl10*zp10)/(zl10+zp10);
    MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
    MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

    % Calculate the transducer loss

Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
    Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
    Gt_tx=10*log10(Gt_transmit);
    Gt_rx=10*log10(Gt_receive);

    % Calculate bandwidth metric
    index=1;
    tp0=tp;
    tp10=tp1;
    tp20=tp2;
    tp30=tp3;
    for ct = 40:1:140
       f1=ct*1000000000;           % frequency in GHz
       s1=j*2*pi*f1;
       % Circuit 3. Lossy
       % PA MN - transmission line
       tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp=ap+j*tpp;
       pp(1,1)=cosh(gpp);            % A
       pp(1,2)=zp*sinh(gpp);         % B
       pp(2,1)=(1/zp)*sinh(gpp);     % C
       pp(2,2)=cosh(gpp);            % D

       tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp1=ap1+j*tpp1;
       pp1(1,1)=cosh(gpp1);            % A
       pp1(1,2)=zp1*sinh(gpp1);         % B
       pp1(2,1)=(1/zp1)*sinh(gpp1);     % C
       pp1(2,2)=cosh(gpp1);            % D

       tpp2=tp20*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp2=ap2+j*tpp2;
       pp2(1,1)=cosh(gpp2);            % A
       pp2(1,2)=zp2*sinh(gpp2);         % B
       pp2(2,1)=(1/zp2)*sinh(gpp2);     % C
       pp2(2,2)=cosh(gpp2);            % D

       tpp3=tp30*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
       gpp3=ap3+j*tpp3;
       pp3(1,1)=cosh(gpp3);            % A
       pp3(1,2)=zp3*sinh(gpp3);         % B
       pp3(2,1)=(1/zp3)*sinh(gpp3);     % C
       pp3(2,2)=cosh(gpp3);            % D

       pp=pp*pp1*pp2*pp3;   % update pp ABCD matrix

       % LNA MN - LCLC
       ll11=[1 0; 1/(esr1+s1*ind1) 1];
```

```
        lc11=[1 esr2+1/(s1*cap1);0 1];
        ll21=[1 0; 1/(esr3+s1*ind2) 1];
        lc21=[1 esr4+1/(s1*cap2);0 1];
        l1=ll11*lc11*ll21*lc21; %[ABCD]
        % Reflection coefficients at the antenna
        % Receive mode
        zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
        zjr1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Rx1=zjr1/Z0;
        Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
        mrx = abs(Gamma_Rx);
        % Transmit mode
        zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
        zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
        zjt1=(zl11*zp11)/(zl11+zp11);
        Z0=50;
        Z_Tx1=zjt1/Z0;
        Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
        mtx = abs(Gamma_Tx);
        freq(index)=ct;             %frequency in GHz
        rc_rx(index)=mrx;
        rc_tx(index)=mtx;
        index=index+1;
     end
     rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
     tx_bw_metric=sum([rc_tx(35:70)]);

     % 1. Record component characteristics
     fprintf(fid,'================================================================\n');
     fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1,
Z_pa, L11, Z_pa1, L12, Z_pa2, L13, Z_pa3, L, C1r, Lr, C2r, iteration_count);

     % 2. Record mismatch losses at the amplifiers
     fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

     % 3. Record mismatch losses at the antenna
     fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

     % 4. Record transducer loss
     fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

     % 5. Record bandwidth metric
     fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);


     count=count+1;

    end

end
end
end
end
end
end
end
end


count

fclose(fid);
```

B.11 MATLAB Search Script for PALNA Topology Shown in Fig. 6.17 With Constant LNA MN Component Values and Randomized TL Lengths

```
%*************************************************************************************************
% MATLAB search script for PALNA topology given in Fig. 6.17
%       Note 1: Calculations are based on PA MN and LNA MN ABCD matrices
%       Note 2: Component losses are accounted for, based on data from EM simulations
%       Note 3: Transducer loss is calculated and stored for each potential solution
%       Note 4: Bandwidth metric calculation is added for each solution
%       Note 5: Values of lumped components in LNA MN are kept constant for computation efficiency
%       Note 6: TL lengths are randomized for speed of execution
%*************************************************************************************************

clear all;

% Receive mode impedances
%Z_opt_LNA=150+j*25;              % LNA ON
Z_opt_LNA=172+j*21;              % LNA ON
Z_in_LNA=117+j*13;       % LNA ON
Z_load_PA=441+j*177;        % PA OFF

% Transmit mode impedances
%Z_opt_PA=90;                % PA ON
%Z_opt_PA=289;
Z_opt_PA=105+j*14;               % PA ON
Z_out_PA=289+j*1;          % PA ON
Z_load_LNA=38+j*38;     % LNA OFF

fid=fopen('results_mod9_a.txt','w');

f=94000000000;           % 94 GHz
s=j*2*pi*f;

count=1;

iteration_count=0;

L = 60;     % LNA MN components
C1r = 17;
Lr = 140;   % NO SOLUTIONS AVAILABLE
C2r = 20;

L = 70;     % LNA MN components
C1r = 17;
Lr = 140;   % SOLUTIONS AVAILABLE
C2r = 17;

L = 80;     % LNA MN components
C1r = 17;
Lr = 140;   % SOLUTIONS AVAILABLE
C2r = 17;

L = 75;     % LNA MN components
C1r = 17;
Lr = 140;   % SOLUTIONS AVAILABLE
C2r = 17;

L = 70;     % LNA MN components
C1r = 17;
Lr = 140;   % SOLUTIONS AVAILABLE
C2r = 17;


% LNA MN - LCLC
ind1=L/1000000000000;   %pH
```

```
esr1=0.0521*L-0.892;    % interpolated ESR value
cap1=C1r/1000000000000000; %fF
esr2=(-0.036)*C1r+1.566; % interpolated ESR value
ind2=Lr/1000000000000;   %pH
esr3=0.0521*Lr-0.892;    % interpolated ESR value
cap2=C2r/1000000000000000;  %fF
esr4=(-0.036)*C2r+1.566; % interpolated ESR value
ll1=[1 0; 1/(esr1+s*ind1) 1];
lc1=[1 esr2+1/(s*cap1);0 1];
ll2=[1 0; 1/(esr3+s*ind2) 1];
lc2=[1 esr4+1/(s*cap2);0 1];
l=ll1*lc1*ll2*lc2; %[ABCD]

for num=1:1:1 % repeat 1 times

for Z_pa = 20:2:70    % PA MN components
   for Z_pa1 = 20:2:70
      for Z_pa2 = 20:2:70
          for Z_pa3 = 20:2:70

L1 = (pi/2)*rand;  % restricted TL lengths to positive values only for shorter length and lower loss
L11 = (pi/2)*rand;
L12 = (pi/2)*rand;
L13 = (pi/2)*rand;

% PA MN
zp=Z_pa;  % TL segment 1
tp=L1;
if tp>=0   %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len=L1*(3245/2)/6.28;
else
    phys_len=L1*(3245/2)/6.28+3245/2;
end
if zp<=38            % calculate TL attenuation constant, alpha
    alpha=0.0000909;
elseif (zp>38 & zp<=50)
    alpha=(0.00000025)*zp+0.0000814;
else
    alpha=(0.00000093)*zp+0.0000474;
end
ap=alpha*phys_len;
gp=ap+j*tp;
p(1,1)=cosh(gp);            % A
p(1,2)=zp*sinh(gp);         % B
p(2,1)=(1/zp)*sinh(gp);     % C
p(2,2)=cosh(gp);            % D

zp1=Z_pa1;  % TL segment 2, open stub 1
tp1=L11;
if tp1>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len1=L11*(3245/2)/6.28;
else
    phys_len1=L11*(3245/2)/6.28+3245/2;
end
if zp1<=38            % calculate TL attenuation constant, alpha
    alpha1=0.0000909;
elseif (zp1>38 & zp1<=50)
    alpha1=(0.00000025)*zp1+0.0000814;
else
    alpha1=(0.00000093)*zp1+0.0000474;
end
ap1=alpha1*phys_len1;
gp1=ap1+j*tp1;
p1(1,1)=1;            % A
p1(1,2)=0;         % B
p1(2,1)=(1/zp1)*tanh(gp1);     % C
p1(2,2)=1;            % D

zp2=Z_pa2;  % TL segment 3
tp2=L12;
if tp2>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len2=L12*(3245/2)/6.28;
else
    phys_len2=L12*(3245/2)/6.28+3245/2;
end
if zp2<=38            % calculate TL attenuation constant, alpha
    alpha2=0.0000909;
elseif (zp2>38 & zp2<=50)
    alpha2=(0.00000025)*zp2+0.0000814;
else
    alpha2=(0.00000093)*zp2+0.0000474;
```

```
end
ap2=alpha2*phys_len2;
gp2=ap2+j*tp2;
p2(1,1)=cosh(gp2);            % A
p2(1,2)=zp2*sinh(gp2);         % B
p2(2,1)=(1/zp2)*sinh(gp2);     % C
p2(2,2)=cosh(gp2);            % D

zp3=Z_pa3;  % TL segment 4, open stub 2
tp3=L13;
if tp3>=0  %calculate physical length of the transmission line in micrometers. lambda=3245um @ 94 GHz.
    phys_len3=L13*(3245/2)/6.28;
else
    phys_len3=L13*(3245/2)/6.28+3245/2;
end
if zp3<=38            % calculate TL attenuation constant, alpha
    alpha3=0.0000909;
elseif (zp3>38 & zp3<=50)
    alpha3=(0.00000025)*zp3+0.0000814;
else
    alpha3=(0.00000093)*zp3+0.0000474;
end
ap3=alpha3*phys_len3;
gp3=ap3+j*tp3;
p3(1,1)=1;            % A
p3(1,2)=0;         % B
p3(2,1)=(1/zp3)*tanh(gp3);     % C
p3(2,2)=1;            % D

p=p*p1*p2*p3;   % update p ABCD matrix

Ya=1/50;
Y_tx_off=(l(2,1)*Z_load_LNA+l(2,2))/(l(1,1)*Z_load_LNA+l(1,2));
Y_rx_off=(p(2,1)*Z_load_PA+p(2,2))/(p(1,1)*Z_load_PA+p(1,2));

A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
B_tx=p(1,2);
C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
D_tx=p(1,1);

A_rx=l(1,1);
B_rx=l(1,2);
C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);

% calculate impedances
Z_PA=A_tx/C_tx; % impedance seen by the PA in Tx
Z_LNA=D_rx/C_rx; % impedance seen by the LNA in Rx

Z_tx_p=Z_PA;            % impedance seen by PA looking forward
Z_rx_l=Z_LNA;           % impedance seen by LNA looking back

iteration_count=iteration_count+1;

   if real(Z_rx_l)>=real(Z_opt_LNA)-20 & real(Z_rx_l)<=real(Z_opt_LNA)+20 &
imag(Z_rx_l)>=imag(Z_opt_LNA)-20 & imag(Z_rx_l)<=imag(Z_opt_LNA)+20 & real(Z_tx_p)>=real(Z_opt_PA)-20
& real(Z_tx_p)<=real(Z_opt_PA)+20 & imag(Z_tx_p)>=imag(Z_opt_PA)-20 & imag(Z_tx_p)<=imag(Z_opt_PA)+20
   % Potential solution => calculate and store quantities of interest

    % calculate and plot losses
    Ya=0; % remove antenna and recalc ABCD matrices
    A_tx=p(2,2)+p(1,2)*(Ya+Y_tx_off);
    B_tx=p(1,2);
    C_tx=p(2,1)+p(1,1)*(Ya+Y_tx_off);
    D_tx=p(1,1);
    A_rx=l(1,1);
    B_rx=l(1,2);
    C_rx=l(2,1)+l(1,1)*(Ya+Y_rx_off);
    D_rx=l(2,2)+l(1,2)*(Ya+Y_rx_off);
    % transmit mode
    zm_tx(1,1)=A_tx/C_tx;
    zm_tx(1,2)=(A_tx*D_tx-B_tx*C_tx)/C_tx;
    zm_tx(2,1)=1/C_tx;
    zm_tx(2,2)=D_tx/C_tx;
    kQ_tx=abs(zm_tx(2,1))/sqrt(det(real(zm_tx)));
    theta_tx=atan(kQ_tx)/2;
    eta_tx=tan(theta_tx)^2;
    loss_tx=10*log10(eta_tx);    % in dB
    % receive mode
    zm_rx(1,1)=A_rx/C_rx;
    zm_rx(1,2)=(A_rx*D_rx-B_rx*C_rx)/C_rx;
```

```
zm_rx(2,1)=1/C_rx;
zm_rx(2,2)=D_rx/C_rx;
kQ_rx=abs(zm_rx(2,1))/sqrt(det(real(zm_rx)));
theta_rx=atan(kQ_rx)/2;
eta_rx=tan(theta_rx)^2;
loss_rx=10*log10(eta_rx);    % in dB

% Mismatch losses at the amplifiers
MLra=10*log10((abs(Z_in_LNA+Z_LNA))^2/(4*real(Z_in_LNA)*real(Z_LNA)));%Receive mismatch loss in dB
MLta=10*log10((abs(Z_out_PA+Z_PA))^2/(4*real(Z_out_PA)*real(Z_PA)));%Transmit mismatch loss in dB

% Mismatch losses at the antenna
% Receive mode
zl10=(l(1,1)*Z_in_LNA+l(1,2))/(l(2,1)*Z_in_LNA+l(2,2));
zp10=(p(1,1)*Z_load_PA+p(1,2))/(p(2,1)*Z_load_PA+p(2,2));
zjr=(zl10*zp10)/(zl10+zp10);
% Transmit mode
zl10=(l(1,1)*Z_load_LNA+l(1,2))/(l(2,1)*Z_load_LNA+l(2,2));
zp10=(p(1,1)*Z_out_PA+p(1,2))/(p(2,1)*Z_out_PA+p(2,2));
zjt=(zl10*zp10)/(zl10+zp10);
MLr=10*log10((abs(50+zjr))^2/(4*50*real(zjr))); % Receive mismatch loss in dB
MLt=10*log10((abs(50+zjt))^2/(4*50*real(zjt))); % Transmit mismatch loss in dB

% Calculate the transducer loss
Gt_transmit=(4*real(Z_out_PA)*real(50)*abs(zm_tx(2,1))^2)/(abs((zm_tx(2,2)+50)*(Z_PA+Z_out_PA))^2);
Gt_receive=(4*real(50)*real(Z_in_LNA)*abs(zm_rx(2,1))^2)/(abs((zm_rx(2,2)+Z_in_LNA)*(zjr+50))^2);
Gt_tx=10*log10(Gt_transmit);
Gt_rx=10*log10(Gt_receive);

% Calculate bandwith metric
index=1;
tp0=tp;
tp10=tp1;
tp20=tp2;
tp30=tp3;
for ct = 40:1:140
   f1=ct*1000000000;           % frequency in GHz
   s1=j*2*pi*f1;
   % Circuit 3. Lossy
   % PA MN - transmission line
   tpp=tp0*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
   gpp=ap+j*tpp;
   pp(1,1)=cosh(gpp);            % A
   pp(1,2)=zp*sinh(gpp);         % B
   pp(2,1)=(1/zp)*sinh(gpp);     % C
   pp(2,2)=cosh(gpp);            % D

   tpp1=tp10*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
   gpp1=ap1+j*tpp1;
   pp1(1,1)=1;            % A
   pp1(1,2)=0;         % B
   pp1(2,1)=(1/zp1)*tanh(gpp1);     % C
   pp1(2,2)=1;            % D

   tpp2=tp20*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
   gpp2=ap2+j*tpp2;
   pp2(1,1)=cosh(gpp2);            % A
   pp2(1,2)=zp2*sinh(gpp2);         % B
   pp2(2,1)=(1/zp2)*sinh(gpp2);     % C
   pp2(2,2)=cosh(gpp2);            % D

   tpp3=tp30*(f1/94000000000);  %At 300 GHz TL would be ~3 times as long
   gpp3=ap3+j*tpp3;
   pp3(1,1)=1;            % A
   pp3(1,2)=0;         % B
   pp3(2,1)=(1/zp3)*tanh(gpp3);     % C
   pp3(2,2)=1;            % D

   pp=pp*pp1*pp2*pp3;   % update pp ABCD matrix

   % LNA MN - LCLC
   ll11=[1 0; 1/(esr1+s1*ind1) 1];
   lc11=[1 esr2+1/(s1*cap1);0 1];
   ll21=[1 0; 1/(esr3+s1*ind2) 1];
   lc21=[1 esr4+1/(s1*cap2);0 1];
   l1=ll11*lc11*ll21*lc21; %[ABCD]
   % Reflection coefficients at the antenna
   % Receive mode
   zl11=(l1(1,1)*Z_in_LNA+l1(1,2))/(l1(2,1)*Z_in_LNA+l1(2,2));
   zp11=(pp(1,1)*Z_load_PA+pp(1,2))/(pp(2,1)*Z_load_PA+pp(2,2));
   zjr1=(zl11*zp11)/(zl11+zp11);
```

```
       Z0=50;
       Z_Rx1=zjr1/Z0;
       Gamma_Rx = (Z_Rx1 - 1)/(Z_Rx1 + 1);
       mrx = abs(Gamma_Rx);
       % Transmit mode
       zl11=(l1(1,1)*Z_load_LNA+l1(1,2))/(l1(2,1)*Z_load_LNA+l1(2,2));
       zp11=(pp(1,1)*Z_out_PA+pp(1,2))/(pp(2,1)*Z_out_PA+pp(2,2));
       zjt1=(zl11*zp11)/(zl11+zp11);
       Z0=50;
       Z_Tx1=zjt1/Z0;
       Gamma_Tx = (Z_Tx1 - 1)/(Z_Tx1 + 1);
       mtx = abs(Gamma_Tx);
       freq(index)=ct;            %frequency in GHz
       rc_rx(index)=mrx;
       rc_tx(index)=mtx;
       index=index+1;
    end
    rx_bw_metric=sum([rc_rx(35:70)]);  % Add reflection coefficients from 75 GHz to 110 GHz
    tx_bw_metric=sum([rc_tx(35:70)]);

    % 1. Record component characteristics
    fprintf(fid,'=====================================================================\n');
    fprintf(fid,'%6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.4f %6.2f %6.2f %6.2f %6.2f %6.2f %d\n', L1,
Z_pa, L11, Z_pa1, L12, Z_pa2, L13, Z_pa3, L, C1r, Lr, C2r, iteration_count);

    % 2. Record mismatch losses at the amplifiers
    fprintf(fid,'%6.2f %6.2f\n', MLra, MLta);

    % 3. Record mismatch losses at the antenna
    fprintf(fid,'%6.2f %6.2f\n', MLr, MLt);

    % 4. Record transducer loss
    fprintf(fid,'%6.2f %6.2f\n', Gt_rx, Gt_tx);

    % 5. Record bandwidth metric
    fprintf(fid,'%6.2f %6.2f\n', rx_bw_metric, tx_bw_metric);


    count=count+1;

   end

end
end
end
end

end %num loop

count

fclose(fid);
```

References

[1] I. Abdomerovic, K. J. Koh, M. Sayginer, G. Rebeiz, and S. Raman, "An Efficient 94 GHz Switched T/R Circuit Design in 32SOI Technology," *Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMAC Tech)*, March 2018.

[2] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A Millimeter-Wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation," *IEEE Journal of Solid-State Circuits*, Vol. 52, No. 12, pp. 3276-3292, Dec. 2017.

[3] J. W. Archer, R.A. Batchelor, and O. Sevimli, "Millimetre-wave Bi-Directional Amplifiers," *IEEE Top. Symp. on Mill. Waves*, pp.19–22, Kanagawa, Jul. 1997.

[4] J. W. Archer, O. Sevimli, and R.A. Batchelor, "Bi-Directional Amplifiers for Half-Duplex Transceivers," *IEEE Gallium Arsenide Integrated Circuit Symposium*, pp.251–254, Monterey, California, Oct. 17-20, 1999.

[5] J. M. Yang et al, "Compact Ka-Band Bi-Directional Amplifier for Low-Cost Electronic Scanning Array Antenna," *IEEE Journal of Solid-State Circuits*, vol.39, no.10, pp.1716–1719, Oct. 2004.

[6] J. M. Yang et al, "GaAs Bi-Directional Amplifier For Low Cost Electronic Scanning Array Antenna," *IEEE Gallium Arsenide Integrated Circuit Symposium*, pp.129–130, San Diego, California, November 9-12, 2003.

[7] S. Shiba et al, "F-band Bidirectional Amplifier using 75-nm InP HEMTs," *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp.1-4, La Jolla, California, October 14-17, 2012.

[8] J. Kim, and J.F. Buckwalter, "A Fully Integrated Q-band Bidirectional Transceiver in 0.12-μm SiGe BiCMOS Technology," *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp.57–60, 2010.

[9] J. Kim, and J.F. Buckwalter, "A Switchless, Q –Band Bidirectional Transceiver in 0.12-μm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, vol.47, no.2, pp.368–380, Feb. 2012.

[10] T. Kijsanayotin, J. Li, and J.F. Buckwalter, "A 70 GHz Bidirectional Front-End for a Half-Duplex Transceiver in 90-nm SiGe BiCMOS," *Proc. IEEE Compound Semiconductor Integrated Circuit Symposium,* pp.1-4, New Orleans, Louisiana, October 11-14, 2015.

[11] P. Wu, T. Kijsanayotin, and J.F. Buckwalter, "A 71-86-GHz Switchless Asymmetric Bidirectional Transceiver in a 90-nm SiGe BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no.12, pp.4262-4273, Dec. 2016.

[12] F. Meng, C. C. Boon, S. Xu, K. Ma, and K.S. Yeo, "Millimeter-Wave IC Design Techniques for Beam-Forming Applications," *IEEE International Workshop on Electromagnetics*, pp.1-3, Nanjing, Jiangsu, China, May 16-18, 2016.

[13] F. Meng et al, "A Compact 57-67 GHz Bidirectional LNAPA in 65-nm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol.26, no.8, pp.628–630, Aug. 2016.

[14] A. Valdes-Garcia et al, "A Fully-Integrated Dual-Polarization 16-Element W-band Phased-Array Transceiver in SiGe BiCMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, pp.375–378, 2013.

[15] P. Peng, C. Kao, C. Wu, and J. Lee, "A 79-GHz Bidirectional Pulse Radar System with Injection-Regenerative Receiver in 65 nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, pp.303–306, 2014.

[16] A. Puglielli et al., "Design of Energy- and Cost-Efficient Massive MIMO Arrays," *IEEE Proceedings Special Issue on Phased Array Technologies*, vol.104, no.3, pp.586–606, Mar. 2016.

[17] Herd and Conway, “The Evolution to Modern Phased Array Architectures”, *IEEE Proceedings Special Issue on Phased Array Technologies*, vol. 104, no. 3, pp. 519-529, Mar. 2016.

[18] C. Fulton et al., “Digital Phased Arrays: Challenges and Opportunities”, *IEEE Proceedings Special Issue on Phased Array Technologies*, vol. 104, no. 3, pp. 487-503, Mar. 2016.

[19] DARPA MIDAS Broad Agency Announcement (BAA) can be downloaded at: https://www.fbo.gov/index?s=opportunity&mode=form&id=d8c414aaf7c707bc4f7ac896a7b68b29&tab=core&_cview=0

[20] S. Zihir et al., "60-GHz 64- and 256-Elements Wafer-Scale Phased-Array Transmitters Using Full-Reticle and Subreticle Stitching Techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol.64, no.12, pp.4701–4719, Dec. 2016.

[21] A. Chakrabarti and H. Krishnaswamy, "High Power High-Efficiency Class-E-Like Stacked mmWave PAs in SOI and Bulk CMOS: Theory and Implementation," *IEEE Transactions on Microwave Theory and Techniques*, vol.62, no.8, pp.1686–1704, Aug. 2014.

[22] K. Iniewski, *Wireless Technologies: Circuits, Systems, and Devices*, CRC Press, 2007, Chapter 12, pp. 329–348, “Design of Silicon Integrated Circuit W-Band Low-Noise Amplifiers.”

[23] B. E. Stine et al, “The Physical and Electrical Effects of Metal-Fill Patterning Practices for Oxide Chemical-Mechanical Polishing Process,” *IEEE Transactions on Electron Devices*, Vol. 45, No. 3, March 1998, pp 665-679.

[24] S. Shahramian, Y. Baeyens, N. Kaneda, and Y. K. Chen, "A 70–100 GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset Demonstrating 10 Gb/s Wireless Link," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp.1113–1125, May 2013.

[25] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90–100-GHz 4x4 SiGe BiCMOS Polarimetric Transmit/Receive Phased Array With Simultaneous Receive-Beams

Capabilities," *IEEE Transactions on Microwave Theory and Techniques*, vol.61, no.8, pp.3099–3114, Aug. 2013.

[26] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. K. Reynolds, and B. D. Parker, "W-Band Dual-Polarization Phased-Array Transceiver Front-End in SiGe BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol.63, no.6, pp.1989–2002, Jun. 2015.

[27] T. Fujibayashi, Y. Takeda, W. Wang, Y. S. Yeh, W. Stapelbroek, S. Takeuchi, and B. Floyd, "A 76- to 81-GHz Multi-Channel Radar Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp.2226–2241, Sep. 2017.

[28] K. Tokgoz et al, "A 56Gb/s W-Band CMOS Wireless Transceiver," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2016 IEEE International, Feb 2016, pp. 242–243.

[29] A. Townley, P. Swirhun, D. Titz, A. Bisognin, F. Gianesello, R. Pilard, C. Luxey, and A. M. Niknejad, "A 94-GHz 4TX–4RX Phased-Array FMCW Radar Transceiver With Antenna-in-Package," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp.1245–1259, May 2017.

[30] C. C. Chou, S. C. Huang, W. C. Lai, H. C. Kuo, and H. R. Chuang, “Design of W-Band High-Isolation T/R Switch,” in *Proc. European Microwave Conference*, pp. 1084-1087, Sep. 2015.

[31] W. C. Lai, C. C. Chou, S. C. Huang, T. H. Huang, and H. R. Chuang, “75–110-GHz W-band High-Linearity Traveling-Wave T/R Switch by Using Negative Gate/Body-Biasing in 90-nm CMOS,” in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 5, pp.488-490, May 2017.

[32] V. S. Shilimkar, S. G. Gaskill, and A. Weisshaar, “Experimental Characterization of Metal Fill Placement and Size Impact on Spiral Inductors,” *IEEE 18th Conference on Electrical Performance of Electronic Packaging and Systems*, pp.101-104, Oct. 19-21, 2009.

[33] S. G. Gaskill, V. S. Shilimkar, and A. Weisshaar, “High-Frequency Modeling of Metal Fill Eddy-Current Loss in Integrated Circuits,” in *Proc. European Microwave Conference*, pp. 975-978, Oct. 2013.

[34] V. S. Shilimkar, and A. Weisshaar, “Modeling of Metal-Fill Parasitic Capacitance and Application to On-Chip Slow-Wave Structures,” *IEEE Transactions on Microwave Theory and Techniques*, vol.65, no.5, pp.1456–1464, May 2017.

[35] M. Sayginer and G. M. Rebeiz, “A 94-96 GHz Phased-Array Receive Front-End with 5-bit Phase Control and 5 dB Noise Figure in 32 nm CMOS SOI,” *Proceedings of the IEEE International Microwave Symposium (IMS)*, pp.768–770, Jun. 2017.

[36] B. A. Orner, et al., “A 0.13 μm BiCMOS technology featuring a 200/280 GHz (fT/fMAX) SiGe HBT”, *Proc of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 203- 206, 28-30 Sept. 2003.

[37] GlobalFoundries brochure “SiGe 8XP & SiGe 8HP 130 nm SiGe BiCMOS Technologies”, located at https://www.globalfoundries.com/sites/default/files/product-briefs/130nm-sige-performance-brief.pdf

[38] P. Candra et al., “A 130nm SiGe BiCMOS technology for mm-Wave applications featuring HBT with fT/fMAX of 260/320 GHz”, *IEEE Radio Freq Integrated Circuits Symp (RFIC)*, pp. 381-384, 2-4 Jun 2013.

[39] V. Jain et al., “Device and circuit performance of SiGe HBTs in 130nm BiCMOS process with fT/fMAX of 250/330GHz”, *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 96-99, 2014.

[40] S. Y. Mortazavi and K. J. Koh, "Integrated Inverse Class-F Silicon Power Amplifiers for High Power Efficiency at Microwave and mm-Wave," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2420–2434, October 2016.

[41] Lee et al, “Advanced modeling and optimization of high performance 32nm HKMG SOI CMOS for RF/analog SoC applications”, *IEEE Symposium on VLSI Technology*, pp.135-136, Jun. 12-14, Honolulu, Hawaii, 2012.

[42] R. W. Beatty, “Insertion Loss Concepts”, *Proceedings of the IEEE*, vol. 52, no. 6, pp. 663-671, 1964.

[43] T. Ohira, "What in the World Is Q?," *IEEE Microwave Magazine*, vol. 17, no. 6, pp. 42-49, Jun. 2016.

[44] D. M. Pozar, *Microwave Engineering, second edition*, John Wiley & Sons Inc., 1998.

[45] I. Abdomerovic, W. D. Palmer, P. M. Watson, R. Worley, and S. Raman, "Leveraging Integration: Toward Efficient Linearized All-Silicon IC Transmitters," *IEEE Microwave Magazine*, vol. 15, no. 3, pp.86–96, May 2014.

[46] Hee-Ran Ahn, "Complex Impedance Transformers Consisting of Only Transmission-Line Sections," *IEEE Transactions on Microwave Theory and Techniques*, vol.60, no.7, pp.2073–2084, Jul. 2012.

[47] N. Kumar and A. Grebennikov, *Distributed Power Amplifiers for RF and Microwave Communications*, Artech House, 2015.

[48] H. W. Bode, *Network Analysis and Feedback Amplifier Design*, Van Nostrand, N.Y., 1945.

[49] G. Chen and M. Hamid, "Multi-Section Transmission Line Transformer of Arbitrary Length," *IEEE 1986 Symposium on Antenna Technology and Applied Electromagnetics*, 13-14 Aug. 1986, Winnipeg, Canada.

[50] P. W. Van Der Walt, "Short-Step-Stub Chebyshev Impedance Transformers," *IEEE Transactions on Microwave Theory and Techniques*, vol.34, no.8, pp.863–868, Aug. 1986.

[51] G. Nikandish, R. B. Staszewski, A. Zhu, "The (R)evolution of Distributed Amplifiers," *IEEE Microwave Magazine*, vol. 19, no. 4, pp.66–83, June 2018.

[52] L. Lavagno, G. Martin, I. L. Markov, L. K. Scheffer, *Electronic Design Automation for IC Implementation, Circuit Design, And Process Technology*, CRC Press, Taylor & Francis Group, Boca Raton, FL, USA, 2016.

[53] G.G.E. Gielen, "CAD tools for embedded analogue circuits in mixed signal integrated systems on chip", *IEE Proc.-Comput. Digit. Tech.*, Vol. 152, No. 3, May 2005, pp 317-332

[54] R. A. Rutenbar, G. G. E. Gielen, and J. Roychowdhury, "Hierarchical modeling, optimization, and synthesis for system-level analog and RF designs," *Proc. IEEE*, vol. 95, no. 3, pp. 640–669, Mar. 2007.

[55] B. Liu, G. Gielen and F.V. Fernandez, *Automated design of analog and high-frequency circuits*, Springer, 2014.

[56] G. Tulunay and S. Balkir, “A synthesis tool for CMOS RF low-noise amplifiers,” *IEEE Trans. Comp.-Aided Design Integr. Cir. Sys.*, vol. 27, no. 5, pp. 977–982, May 2008.

[57] R. Gupta, B. Ballweber and D. Allstot, “Design and optimization of CMOS RF power amplifiers,” *IEEE J. Solid-State Cir.*, vol. 36, no. 2, pp. 166-175, Feb. 2001.

[58] G. Zhang, A. Dengi, and L. R. Carley, “Automatic synthesis of a 2.1 GHz SiGe low noise amplifier,” *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, pp. 125–128, 2002.

[59] Y. Xu, K.-L. Hsiung, X. Li, L. T. Pileggi, and S. P. Boyd, “Regular analog/RF integrated circuits design using optimization with recourse including ellipsoidal uncertainty,” *IEEE Trans. Comp.-Aided Design Integr. Cir. Sys.*, vol. 28, no. 5, pp. 623–637, May 2009.

[60] C. Ranter, et al., “CYCLONE: automated design and layout of RF LC oscillators,” *IEEE Trans. Comp.-Aided Design of Integr. Cir. Sys.*, vol. 21, no. 10, pp. 1161-1170, Oct. 2002.

[61] G. Alpaydin, S. Balkir and G. Dundar, “An evolutionary approach to automatic synthesis of high-performance analog integrated circuits,” *IEEE Trans. Evol. Comp.*, vol.7, pp. 240-252, June 2003.

[62] R. Povoa, I. Bastos, N. Lourenço, N. Horta, “Automatic synthesis of RF front-end blocks using multi-objective evolutionary techniques,” *Integration, the VLSI Journal*, vol. 52, pp. 243-252, 2016.

[63] M. Chu and D. J. Allstot, "Elitist nondominated sorting genetic algorithm based RF IC optimizer," *IEEE Trans. Cir. and Sys. I*, vol. 52, pp. 535-545, 2005.

[64] F. Passos, R. Gonzalez-Echevarria, E. Roca, R. Castro-Lopez and F. V. Fernandez, “A two-step surrogate modeling strategy for single-objective and multi-objective optimization of radiofrequency circuits,” *Soft Computing*, Volume 23, Issue 13, July 2019, pp 4911–4925.

[65] R. Gonzalez-Echevarria, et al., “An automated design methodology of RF circuits by using Pareto-optimal fronts of EM-simulated inductors,” *IEEE Trans. Comp.-Aided Design of Integr. Cir. Sys.*, vol. 36, no. 1, pp. 15-26, Jan. 2017.

[66] D. Ghai, S. P. Mohanty and E. Kougianos, "Design of parasitic and process-variation aware nano-CMOS RF circuits: a VCO case study," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 9, pp. 1339-1342, Sept. 2009.

[67] S. P. Mohanty and E. Kougianos, "Incorporating manufacturing process variation awareness in fast design optimization of nanoscale CMOS VCOs," *IEEE Transactions on Semiconductor Manufacturing*, vol. 27, no. 1, pp. 22-31, Feb. 2014.

[68] G. Gielen, "Modeling and analysis techniques for system-level architectural design of telecom front-ends," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, no. 1, pp. 360-368, 2002.

[69] W. Sheng, A. Emira, and E. Sanchez-Sinencio, "CMOS RF receiver system design: A systematic approach," *IEEE Trans. Cir. and Sys. I*, vol. 53, pp. 1023-1034, May 2006.

[70] S. Rodriguez, J. Atallah, A. Rusu, L. Zheng and M. Ismail, "ARCHER: an automated RF-IC Rx front-end circuit design tool," *Analog Integrated Circuits and Signal Processing*, vol. 58, no. 3, pp. 255-270, 2009.

[71] Zhijian Pan, Chuan Qin, Zuochang Ye and Y. Wang, "Automatic design for analog/RF front-end system in 802.11ac receiver," *The 20th Asia and South Pacific Design Automation Conference*, Chiba, 2015, pp. 454-459.

[72] A. Nieuwoudt, T. Ragheb, and Y. Massoud, "Hierarchical optimization methodology for wideband low noise amplifiers," *Proc. Asia South Pacific Design Automat. Conf.*, Jan. 2007, pp. 68–73.

[73] J. Crols, S. Donnay, M. Steyaert, and G. Gielen, "A high-level design and optimization tool for analog RF receiver front-ends," *Proc. IEEE Inter. Conf. Comput. Aided Design*, Nov. 1995, pp. 550–553.

[74] P. Vancorenland, C. De Ranter, M. Steyaert, and G. Gielen, "Optimal RF design using smart evolutionary algorithms," *Proc. 37th Design Automat. Conf.*, Jun. 2000, pp. 7–10.

[75] B. Liu, Dixian Zhao, Patrick Reynaert, and G. G. E. Gielen, "Synthesis of Integrated Passive Components for High-Frequency RF ICs Based on Evolutionary Computation and Machine Learning Techniques," *IEEE Transactions on Computer-*

Aided Design of Integrated Circuits and Systems, Vol. 30, No. 10, Oct. 2011, pp 1458-1468.

[76] M. B. Yelten, T. Zhu, S. Koziel, P. D. Franzon, and M. B. Steer, "Demystifying surrogate modeling for circuits and systems," *IEEE Circuits Syst. Mag.*, vol. 12, no. 1, pp. 45–63, 1st Quart., 2012.

[77] F. Passos, E. Roca, R. Castro-Lopez, and F. V. Fernandez, "A Comparison of Automated RF Circuit Design Methodologies: Online Versus Offline Passive Component Design," *IEEE Transactions on VLSI Systems*, Vol. 26, No. 11, Nov. 2018, pp 2386-2394.

[78] F. Passos et al., "A Multilevel Bottom-up Optimization Methodology for the Automated Synthesis of RF Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, early access article, 2018.

[79] C. Galup-Montoro, *MOSFET Modelling For Circuit Analysis and Design*, World Scientific Publishing Co., 2007.

[80] http://www-device.eecs.berkeley.edu/bsim/

[81] Y. S. Chauhan et al, "BSIM Compact MOSFET Models for SPICE Simulation," MIXDES 2013, 20th International Conference on Mixed Design of Integrated Circuits and Systems, June 20-22, 2013, Gdynia, Poland, pp 23-28.

[82] BSIM4.3.0 MOSFET Model Users' Manual, University of California at Berkeley, December 2003.

[83] BSIM4v4.8.0 MOSFET Model User's Manual, University of California at Berkeley, December 2013.

[84] W. Liu and C. Hu, *BSIM4 and MOSFET Modelling For IC Simulation*, World Scientific Publishing Co., 2011.

[85] S. El Ghouli, J. Sallese, A. Juge, P. Scheer, and C. Lallement, "Transadmittance Efficiency under NQS Operation in Asymmetric Double Gate FDSOI MOSFET," *IEEE Transactions On Electron Devices*, Vol. 66, No. 1, Jan. 2019, pp 300-307.

[86] BSIMSOI4.3 MOSFET MODEL Users' Manual, BSIM GROUP, December 2009.

[87] K. Smith, M. Palaniswami, and M. Krishnamoorthy, “Neural Techniques for Combinatorial Optimization with Applications,” *IEEE Transactions on Neural Networks*, vol.9, no.6, pp.1301–1318, Nov. 1998.

[88] M. Asghar Bhatti, *Practical Optimization Methods*, Springer-Verlag, New York, 2000.