# Integrated Electrical and Thermal Modeling, Analysis and Design for IPEM

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**Integrated Electrical and Thermal Modeling, Analysis and Design for IPEM**

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(Abstract)

The goal of this dissertation is to present a systematic approach to integrating the multidisciplinary design process in power electronics through the integration of existing CAD tools, multidisciplinary modeling and system optimization. Two major benefits are expected from the utilization of the proposed integrated design methodology. Firstly, it will significantly speed up the design process and will eliminate errors resulting from repeated manual data entry and information exchange. Secondly, the integrated design optimization will result in better utilization of materials and components.

In order to understand the basic relationship between electrical and thermal phenomena, the self-heating effect of a simple copper conductor is modeled analytically. Based on these models, a guideline for copper trace design is proposed.

The next step towards developing an integrated design methodology is to create three-dimensional solid-body-based models that characterize the electrical, thermal and mechanical properties. The electrical model of an integrated power electronics module (IPEM), including parasitic parameters, is developed and experimentally verified with impedance measurements. Together with the thermal model, it lays the foundation for the integrated electrical and thermal analysis and design.

The software integration framework is presented along with the software tools chosen for this study, which include Saber for electrical circuit simulation, Maxwell Q3D Extractor for parameter extraction, and I-DEAS for geometry and thermal modeling. Each of these software tools is controlled via its own macro language files. iSIGHT is then used to interface with these tools in order to achieve software integration.

The DC-DC IPEM layout design is investigated and improved upon by using the integrated design methodology. Several examples of parametric study are presented. The first example shows the tradeoff between electrical and thermal performance for different ceramic layer thicknesses of module substrate. The next example looks at the common-mode noise problem that exists in different direct-bonded copper (DBC) layouts.

To my wife

Mingjie Zhai

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# Chapter 1. Introduction

## 1.1. Research Background

Throughout the history of power electronics, advancements in power semiconductor technology have always been the driving force for achieving higher power density, higher reliability and reduced cost in the manufacture of power electronics. For example, in the area of low-voltage power supplies, the switching speed improvement of bipolar power transistors in the mid-1960s made it possible to operate DC-DC converters in the frequency range of 10 – 20 kHz. Thus the linear regulator technology was rendered obsolete by the switching regulator which was more efficient and had higher levels of power density. The emergence of the power MOSFET in the late 1970s – with its switching frequency normally from 100 kHz to 1MHz – further reduced the size of switching-mode power supplies. Therefore, it is reasonable to believe that device technology has been, and will continue to be, the major factor impacting the overall performance improvement of power electronics systems.

However, with continuous increases in switching frequency and power density, packaging technology-related issues like parasitic parameters and thermal management have became more critical. For example, because of undesired parasitic inductance and capacitance, the switching action may need to be slowed down in order to limit the electrical stress of a device and/or to meet the electromagnetic interference (EMI) standard.

At the same time, thermal management is becoming the most critical factor for the further reduction of converter size. It is also vital for the improvement of product reliability. According to statistics from the U.S. Department of Defense, thermal over-stressing is the primary cause of failure in electronic systems, and the failure rate of equipment is directly related to the junction temperature of semiconductor devices [1-1], as shown in Figure 1.1.

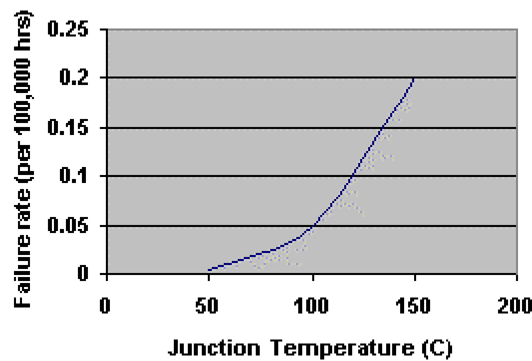



Figure 1.1. Equipment failure rate as a function of junction temperature.

The layout of a power electronics module should be designed to reduce electrical parasitics and to improve thermal management, thus improving the long-term reliability of modules under power and thermal cycling. However, there is a tradeoff between electrical and thermal performance. For example, devices should be closely spaced to achieve high power density, and in this way parasitics can be reduced to avoid high voltage stress during the turn-on and turn-off periods. However, from the thermal standpoint, the thermal interaction between different devices will cause higher junction temperatures if they are located too close to each other.

In order to quantify these effects, integrated multidisciplinary design methodology is needed. The need for integrated analysis and design tools is more pressing than it has ever been, now that further advancements are limited by the fundamental relationships between electrical, thermal, mechanical and material properties of the components and packaging of power electronic systems [1-2].

## 1.2. State-of-the-Art Integrated Design Practice

Due to the very nature of electronic power processing, the design of power electronics components, converters and systems has always involved many disciplines: from circuits and solid-state physics, to electromagnetics, systems and control, thermodynamics, structural mechanics, material science and reliability. However in the past, these designs have been done sequentially, progressing from one discipline to the other and involving many prototyping iterations [1-3]. Although some form of an integrated design approach is now used for the design of all power electronics products [1-4]-[1-6], it has achieved the highest levels of sophistication in the design of integrated circuits [1-7], [1-8].

Figure 1.2 shows the current design practice for power electronics systems; from identifying specifications, functional design, electromechanical design, and hardware prototyping to manufacture and documentation. Each box represents a particular kind of analysis, which has its input, output and main function (as shown in Figure 1.2) as three fields: IN, OUT and EXEC. The color of the box indicates how often it is included in the

overall design process. The arrows between boxes represent the data flow between different analysis processes, and the arrows are also color-coded to show whether the data can be automatically transferred.

It can be seen that multidisciplinary designs are involved in each of the above design phases. However, the degrees of involvement for various disciplines vary widely. For example, electrical circuit design is very often performed in all of the design phases, while mechanical stress and strain analysis is seldom included except for some very basic calculations.

The major limitation for multidisciplinary analysis and design is that there are very few extant automatic (or even manual) data translation links. While the present approach has worked well in the past, the design cycle will continue to lengthen when we try to include more disciplines in the design of power electronic systems as required to achieve higher power density and higher reliability.

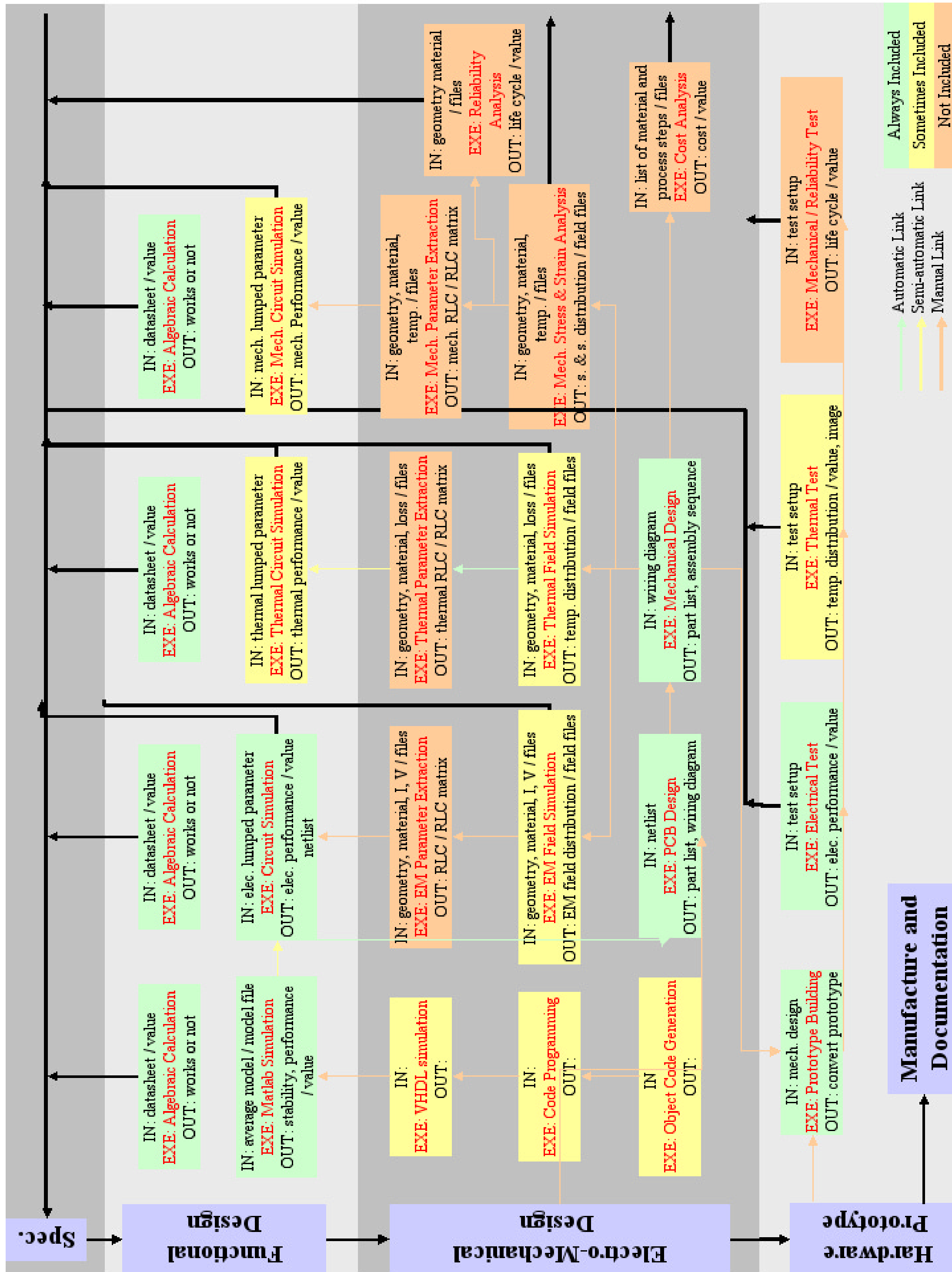



Figure 1.2. State–of-the-art design process for power electronics systems.

Although the use of computer-aided design (CAD) tools is widespread today [1-9]-[1-13], there is a lack of design-oriented tools that allow integrated analysis and optimization of device, circuit, EMI, thermal, packaging and reliability aspects of the integrated power electronics modules (IPEMs) and systems. There are numerous commercially available software packages for most of these aspects [1-14]-[1-18]. Each serves as a useful tool, but it is difficult or impossible to link them together to facilitate system-level design. As a result, today's design process in power electronics is still a long way away from the automation levels now common in many other industries. The resulting long design cycles unduly increase cost and turn-around time, and, coupled with the lack of standardization, prevent levels of optimization that are now standard in other high-tech industries.

The need for integrated analysis and design tools is even more pressing now, when further advancements are limited by the fundamental relationships between electrical, thermal, mechanical and material properties of the components and packaging [1-19][1-20]. Today's CAD tools offer huge opportunities as well as challenges for the development of the integrated design methodology [1-21]. Besides enabling complex analyses at unprecedented speeds, many tools incorporate enormous amounts of knowledge and empirically verified expertise in their respective disciplines, which is extremely difficult and rarely possible to assemble in a functional design team. On the other hand, existing software tools rarely "talk" to each other even within the same discipline, not to mention between disciplines. Therefore, software integration is essential in order to enable the development of an integrated design methodology. Integrated virtual prototyping for power electronics systems will allow industry to bring schedules, performance, tests, support,

production, life-cycle costs, reliability prediction and quality control into the earliest stages of the product creation process. For new power electronics products, this will allow a faster design-to-market period than is possible with current state-of-the-art design tools for power electronics systems that do not allow integrated system analysis.

In the last ten years, several companies have begun developing self-contained CAD software products that integrate multidisciplinary simulations within a unified design environment. Currently being developed at the University of South Carolina, the Virtual Test Bed (VTB) [1-22] is a simulation environment that is intended for virtual prototyping of modern electric power distribution systems and power electronics components. In the area of microelectronics, there is a powerful design suite, ISE TCAD [1-23], that provides an integrated multidisciplinary design environment, but it is not well-suited for the large geometries, high energy levels, and the variety of materials that appear in power electronics. Additionally, these "do-it-all" software products are inherently inadequate in some disciplines, and rely on proprietary software codes in order to facilitate the development of captive markets. There are commercial software integration tools, such as iSIGHT [1-24] and Model Center [1-25], available to facilitate the integration of CAD software. These tools automate the data flow between programs, and they control the execution of these programs. iSIGHT also provides a highly customizable and flexible multidisciplinary design optimization (MDO) language for integrating simulation tools, analysis programs and custom optimization techniques.

However, these integration tools do not define a universal data model. Instead, it is the responsibility of the system designer to customize the data access and the program control in such a way that the integration tool can navigate through the data and control the data and program flow. The Standard for the Exchange of Product Data (STEP) is an international standard (ISO 10303) for the computer-interpretable representation and exchange of product data [1-26]. The objective of STEP is to provide a neutral mechanism capable of describing product data independent from any particular system. There is an application protocol within STEP, Part AP 210, for the exchange of electrical printed circuit board (PCB) assembly design information [1-27].

The first step towards developing an integrated design methodology is to create three-dimensional solid-body-based models that characterize the electrical, thermal and mechanical properties of various constituents forming a system. The models should include active and passive devices, power interconnects and buses, sensing and control system components, PCBs, multi-layer ceramics, adhesives, metallurgical interfaces, encapsulation, thermal spreaders and heat sinks, structural components, etc.

The second step is the development of coherent and systematic multi-fidelity modeling and analysis to enable efficient and comprehensive design. This requires the development of reduced-order models for the IPEM constituents, which enable capturing of properties and behavior that is relevant for the interactions within the IPEM, and at the same time are fully consistent with the detailed three-dimensional models. The issues of model reduction and parameter extraction have recently received considerable attention in the design of

integrated circuits [1-28]-[1-32]. Similarly, the effect of layout and packaging technology used in power electronics is an important issue in the design process [1-33], [1-34], together with the loss estimation in different parts of the circuit [1-35], [1-36], and the analysis of thermal effects on the circuit [1-37]-[1-40]. Such a complexity of multidisciplinary interactions is a major reason that today's development of power electronics systems relies heavily on hardware prototyping to validate designs.

The overall concept of the proposed integrated design methodology is schematically summarized in Figure 1.3. A detailed model of each discipline lies on the outer loop of the illustration of the design process. Each discipline has a lumped parameter model in the inner loop, which is derived from a detailed model based on some approximations. All these models are incorporated into the model database, through which data exchange is possible. It may not be practical to run all detailed simulations in all disciplines. However, by using the lumped parameter model, it is quite possible to have a simulator that will take several disciplines into consideration. Based on this, design optimization can be achieved.

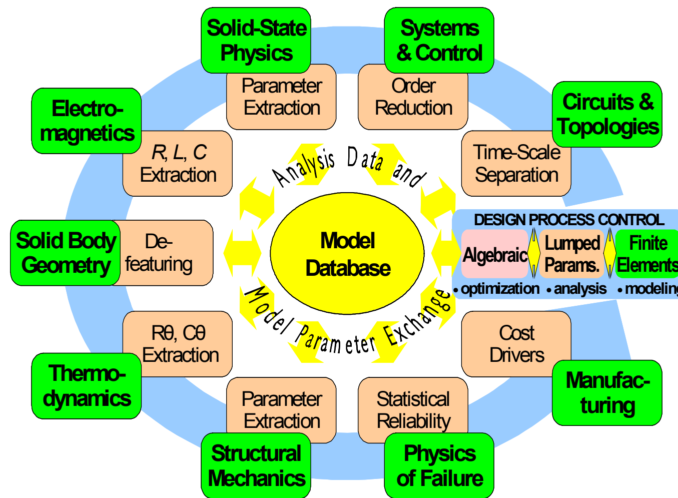
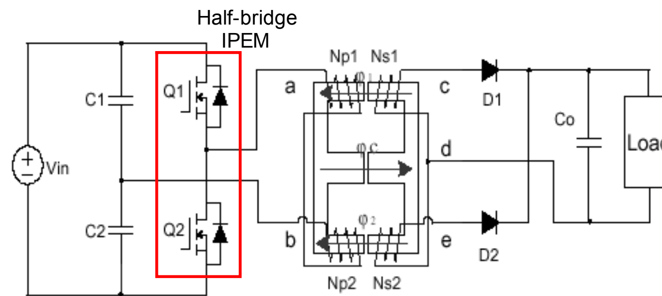


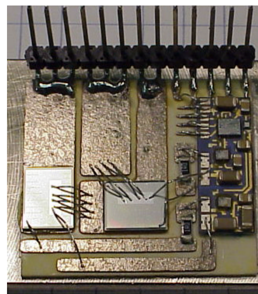

Figure 1.3. Schematic representation of the integrated design methodology.

## 1.3. IPEM Definition

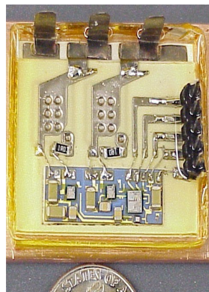
As a way of illustrating the issues and procedures described, let us consider a relatively simple example of designing a half-bridge IPEM for a DC-DC converter. The application is targeted at a 1kW power module for a computer server and for low-end telecommunications systems. The DC-DC converter has 400V DC input, provides a regulated 48V bus, and operates in zero-voltage-switching (ZVS) mode so that the MOSFET body diodes can be used instead of additional anti-parallel diodes [1-41]. It is designed using a modular approach, as shown in Figure 1.4(a).




(a)



(b)



(c)

Figure 1.4. IPEM and IPEM-based converter: (a) asymmetrical half-bridge DC-DC converter with integrated magnetics, (b) wire-bond module, and (c) "embedded power" module.

This module, consisting of two MOSFETs in bare-die form and a hybrid gate driver, can be packaged by conventional wire-bond technology, as shown in Figure 1.4(b).

Alternatively, a different packaging method, the "embedded power" technology [1-42], can be adopted. As shown in Figure 1.4(c), the two bare chips of MOSFETs are buried in a ceramic frame, and are covered by a dielectric layer with etched holes over the aluminum pads of the chips. The power devices are interconnected to other circuits by metal deposition, instead of bonded wire. The procedure for designing such a module, including layout, fabrication and systems applications, provides an excellent illustration for the proposed integrated design methodology.

The design goals for such a module would usually include low electrical stress, low conducted EMI, high thermal conductivity, high structural ruggedness, high power density, high reliability, and low cost. The design variables include component and material selection, geometrical layout, and the interconnect method. The design constraints fall into two broad groups. The first group includes the usual inequality constraints related to the converter design, such as the maximum peak and average currents and voltages, switching frequency range, ambient temperature range, etc., as well as the assortment of available components, materials and packaging technologies, together with their associated physical limitations. The second group of design constraints consists of the physical relationships that exist between the design goals, design variables, and the first group of constraints. These relationships are captured within the models that are used for the design; e.g., device models, models of the electromagnetic and thermal fields, structural stress models, etc.

For optimized designs, the models must take the multidisciplinary interactions into account. For example, the electrical characteristics of the semiconductor devices are

greatly influenced by the temperature distribution inside the module and the mutual thermal interaction between multiple heat sources (mainly the semiconductor devices). The thermal behavior mostly depends on the geometry and the material properties of the isolating, conducting and structural components within the module, which also define the structural (parasitic) impedances that determine the static and dynamic (overshoot) voltage stresses and the electromagnetic compatibility. At the same time, the choice of materials and geometrical limitations are set by the manufacturing technology as well as by the initial and life-cycle structural integrity considerations.

The tradeoff between the quality and difficulty of the design is mostly determined by the accuracy and complexity of the models describing these relationships, and by the features of the software tools used in the design, including their ability to share common data.

## 1.4. Major Contributions and Dissertation Outline

The goal of this dissertation is to present a systematic approach to integrating the multidisciplinary design process in power electronics through the integration of existing CAD tools, multidisciplinary modeling, and system optimization. Two major benefits are expected from the utilization of the proposed integrated design methodology. First, it will significantly speed up the design process and will eliminate the errors resulting from repeated manual data entry and information exchange. Second, the integrated design

optimization will result in better utilization of materials and components and will possibly allow for the discovery of new paradigms in electronic power processing.

In order to understand the basic relationship between electrical and thermal phenomena, the self-heating effect of a simple copper conductor (as found in a PCB layout) is modeled analytically in Chapter 2. Maxwell FS3D will be used within this chapter to validate both the electrical and the thermal models as it provides a direct link for the transfer of loss information from electrical finite-element modeling (FEM) analysis to thermal FEM simulation. Based on the models, guidelines for copper trace design are proposed. For example, the minimal thickness of the copper tracer can be determined by using the derived analytical equations at all frequencies.

Chapter 3 presents the electrical and thermal model of the DC-DC IPEM and power-factor-correction (PFC) IPEM. At first, the fundamentals of the partial element equivalent circuit (PEEC) are reviewed. Then, of two software tools based on the PEEC method (the Maxwell Q3D Extractor and InCa), the former was chosen for this study based on functionality and convenience for software integration; for both the DC-DC IPEM and the PFC IPEM the parasitic inductance and capacitance are calculated using this software. The simulation results are then verified by the impedance measurements. The DC-DC IPEM is compared with both a discrete module and with traditional wire-bond IPEMs in terms of parasitic parameters. Finally, the thermal model of the DC-DC IPEM, which will be used later in the integrated design, is also presented.

The concept of integrated design methodology is described in detail in Chapter 4. The software integration framework is presented, as are the software tools chosen for this study, including Saber for electrical circuit simulation, Maxwell Q3D Extractor for parameter extraction, and I-DEAS for geometry and thermal modeling. Each of these software tools is controlled via its own macro language files. iSIGHT is then used to interface with these tools in order to achieve software integration. Model reduction techniques in various areas are also reviewed in this chapter.

For the DC-DC IPEM layout design, Chapter 5 presents several examples of parametric study using the integrated design methodology. The first example shows the tradeoff between electrical and thermal performance for different thicknesses of DBC ceramics. The next example looks at the common-mode EMI problem with different DBC copper layouts. It has been found that in order to minimize the common-mode EMI noise, the copper trace area of the middle terminal O should be minimized. Conversely, the copper trace area of positive and negative buses should be maximized; this discovery leads to the investigation of adding the embedded bus capacitor inside the DC-DC IPEM.

Chapter 6 presents the final conclusion of the integrated electrical and thermal modeling, analysis and design of the IPEM. Design guidelines for the layout design of power electronics module are summarized, and suggestions for future work are given.

# Chapter 2. Electro-thermal Parametric Study of Copper Trace

In order to understand the basic relationship between electrical and thermal phenomena, this chapter will model a simple copper conductor, such as those found in PCB layout.

From an electrical point of view, the copper conductor serves as a channel to conduct current. But at the same time, the conductor itself will generate loss according to Ohm's Law. Since the loss is the major link between electrical and thermal energy, it is very important that we have an accurate model to predict the conductor loss at all frequencies. In the case of DC, the loss is easy to calculate. However, at high frequencies, an accurate AC loss model is very difficult to obtain because of the skin effect and the proximity effect. In fact, no exact, closed-form solution exists for the rectangular cross-section shape. In this study, among many approximate models developed over the years [2-1]-[2-5], a 2D model [2-3] is reviewed and compared with FEM simulation and experimental measurement before it is used to derive the basic guidelines for copper conductor design in power electronic circuits.

In terms of thermal energy, the copper trace also serves as thermal conductor because of its excellent thermal conductivity. The self-heating effect is modeled based on loss distribution. Under different thermal boundary conditions, the temperature distribution of the conductor can be obtained by solving heat-transfer equations.

On the other hand, simulation tools can always be used to evaluate both the electrical and thermal performance after the initial design is obtained by following certain design rules. Maxwell FS3D will be used in this chapter to validate both the electrical and thermal models, as it provides a direct link to transfer loss information from electrical FEM analysis to thermal FEM simulation.

Based on the models, guidelines for copper trace design are proposed. Specifically, the minimal thickness of the copper tracer can be determined by using the derived equation at all frequencies.

## 2.1. Temperature Limit

In practice, the maximum temperature a copper conductor can withstand is defined by thermal-induced stress. Considering the deposited copper layer on top of the carrier ceramic, which is a commonly-used substrate in IPEMs, the thermal stress is determined by the Coefficient of Thermal Expansion (CTE) mismatch of the copper and alumina ($Al_2O_3$). Since copper has a larger CTE, it tends to expand more than alumina, as shown in Figure 2.1.

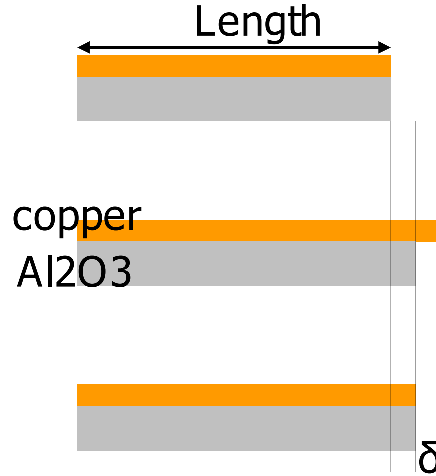



Figure 2.1. Illustration of thermal expansion.

With temperature rise of $\Delta T$, the deformation of copper layer should be:

$$\delta = (\alpha_{copper} - \alpha_{alu\min a}) \cdot \Delta T \cdot Length \tag{2.1}$$

where $\alpha_{copper} = 16.4*10^{-6}$ /K

$\alpha_{alumina} = 7.4*10^{-6}$ /K

However, the binding between the copper and the alumina layer will keep them together. Therefore, the induced stress is as following if uniform stress is assumed.

$$\sigma = E_{copper} \cdot \delta / Length = E_{copper} \cdot (\alpha_{copper} - \alpha_{alu\min a}) \cdot \Delta T \tag{2.2}$$

where Young's modulus $E_{copper}$ = 120 GPa.

Therefore, we have:

$$\sigma = 1.08\Delta T \quad \text{MPa.} \tag{2.3}$$

For the deposited copper, $\sigma$ should be less than the yield stress, which has a typical value of 300 MPa. Thus the maximum $\Delta T$ is about 300 K. However in practice, $\Delta T$ should be much less than 300 K because of reliability considerations. Therefore, in the following discussion, we will assume $\Delta T << 300$ K. And we will assume the electrical resistivity to be constant and not to change with the temperature.

## 2.2. AC Loss Modeling

A precise power loss model that is valid at all frequencies is very difficult to obtain, but is critical to the development of design rules that consider both electrical and thermal constraints.

In this section, we assume there is an infinitely long copper conductor with a rectangular cross-section shape as shown in Figure 2.2. The conductor has a width $w$ and thickness $t$, where $w >> t$. The conductor is sitting in the surrounding free space and has a conductivity of $\sigma$.

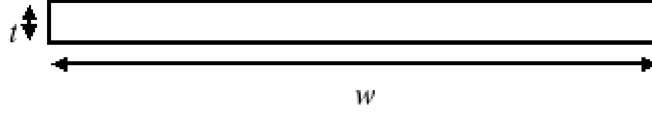



Figure 2.2. Cross-section view of copper conductor.

The current $I$ of frequency $f$ flows through the conductor. The skin depth $\delta$ at this frequency is:

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \quad (2.4)$$

When $t \geq 3\delta$, according to solution obtained by conformal mapping technique [2-6], the AC resistance is

$$R_{ac} = \frac{1}{\pi^2 \sigma \delta w'} K(\sqrt{1 - t^2 / w^2})(1 - e^{-t'/\delta}) \quad (2.5)$$

where $w' = \frac{w}{\sqrt{\pi}}$ (2.6)

$$t' = \frac{t}{\sqrt{\pi}} \quad (2.7)$$

and $K(\sqrt{1 - t^2 / w^2})$ is the complete elliptic integral of the first kind with modulus of $\sqrt{1 - t^2 / w^2}$.

The above approach is only valid at high frequencies when $t \geq 3\delta$ . For lower frequencies, a power series solution was developed by Dwight [2-1]. The AC/DC resistance ratio is:

$$\frac{R_{ac}}{R_{dc}} = 1 + k_1 p^4 + k_2 p^8 + k_3 p^{12} + \cdots \tag{2.8}$$

where $p^2 = 2\mu_0 \cdot \sigma \cdot t \cdot w \cdot f$ , and $k_1$ = 8.743 * $10^{-3}$, $k_2$ = -3.84 * $10^{-4}$, $k_3$ = 1.89 * $10^{-5}$. This solution converges only if $p$ is small. Therefore the upper frequency limit of this solution corresponds to $t \leq 0.6\delta$.

In order to cover the frequency gap ( $0.6\delta \leq t \leq 3\delta$ ), an asymptotic solution was proposed in [2-3]. The AC/DC resistance ratio is given by:

$$\frac{R_{ac}}{R_{dc}} = \left[1 + (\frac{f}{f_l})^{\alpha} + (\frac{f}{f_h})^{\beta}\right]^{1/\gamma} \tag{2.9}$$

where $\alpha = 2$ , $\gamma = 11$ , and $\beta = \gamma / 2 = 5.5$ .

The lower corner frequency $f_l$ is calculated by Dwight's solution:

$$f_l = \frac{\pi}{2\sigma \cdot \mu_0 \cdot w \cdot t} \tag{2.10}$$

And the upper corner frequency $f_h$ is obtained by:

$$f_h = \frac{\pi^2}{\sigma \cdot \mu_0 \cdot t^2} K^{-2}(\sqrt{1 - t^2 / w^2}) \tag{2.11}$$

Since for the case $w >> t$, $\sqrt{1 - t^2 / w^2} \to 1$, we have:

$$K(\sqrt{1 - t^2 / w^2}) = \ln(4w/t) \tag{2.12}$$

Therefore, the upper corner frequency can be simplified to:

$$f_h = \frac{\pi^2}{\sigma \cdot \mu_0 \cdot t^2} \cdot \frac{1}{\ln^2(4w/t)} \tag{2.13}$$

The above model was verified with both numerical simulation and experimental measurement. For a 0.25 inch wide and 1.4 mm thick copper foil with length of 1 m, Maxwell FS3D is used to calculate the AC resistance at frequencies of 1 kHz, 10 kHz, 100 kHz, 1 MHz, 10 MHz and 100 MHz. The simulation result as well as the measured AC resistance is shown in Figure 2.3. The model is accurate in the frequency range of 100 Hz to 2 MHz. After 2 MHz, the measured AC resistance rises rapidly because of self-resonance. However, the calculated value is still close to the simulation results, with less than 10% error.

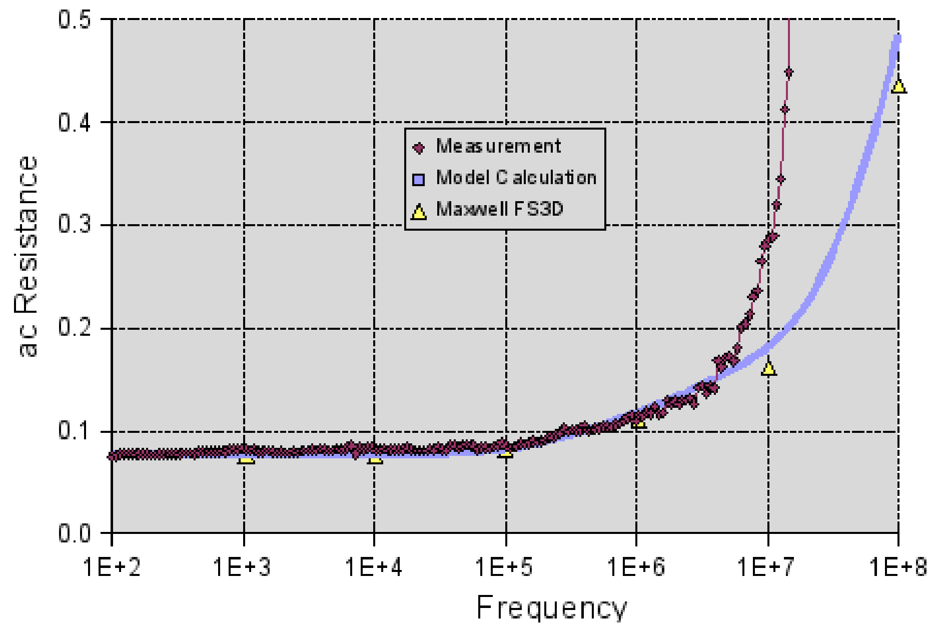



Figure 2.3. AC resistance with 0.25 inch width.

Figure 2.4 is the result for a copper foil of 0.5 inch in width, 1.4 mil in thickness and 1 m in length. Similar results were achieved.

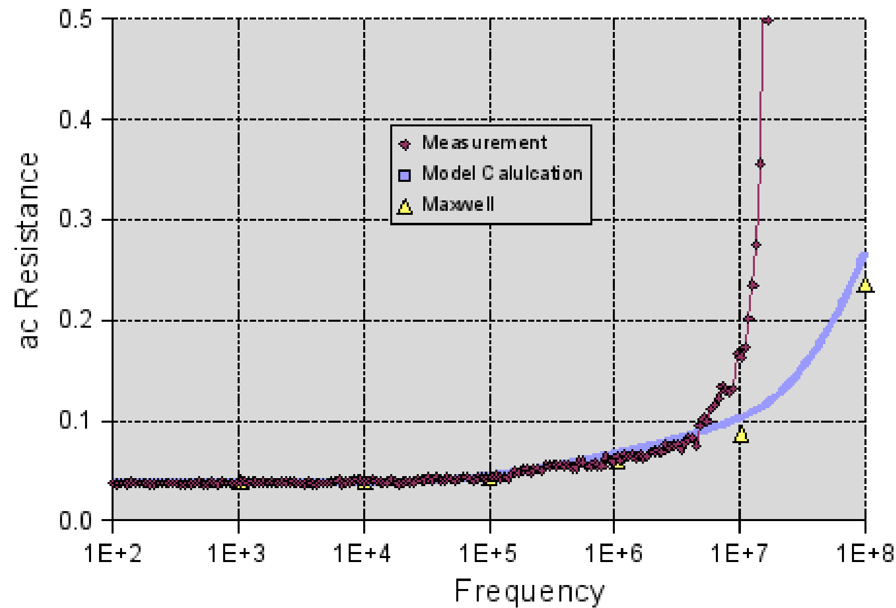



Figure 2.4. AC resistance with 0.5 inch width.

## 2.3. Thermal Modeling

In terms of thermal energy, the same copper trace also serves as thermal conductor because of its excellent thermal conductivity. With different thermal boundary conditions, the temperature distribution of the conductor can be obtained by solving heat transfer equations.

One important example is a conductor with its temperatures fixed at its two ends. Heat transfer only occurs at the cross-section of the two ends. This is a reasonable simplification for the deposited copper tracer in the IPEM. One end of the copper tracer is connected to the silicon device, which has the highest temperature within the module. The

other end of the copper tracer is soldered to the module terminals, which usually have lower temperatures. The heat transfer coefficient H between the deposited copper tracer and the carrier ceramic is very small because of the additional polyimide layer and solder mask layer which have very poor thermal conductivity. Therefore we can assume that no heat is being transferred to the ceramic layer.

There are also cases where the heat transfer at the bottom surface of a conductor cannot be neglected; for instance the copper trace on the DBC board. In this case, the heat transfer coefficient H is considerably large since all the heat must go though the copper-ceramic interface.

These two cases will be illustrated separately.

**Case 1: $H = 0$**

Let us consider the same copper conductor with the length of $l$, as shown in Figure 2.5. The temperatures at the both ends of the conductor are fixed at $T_1$ and $T_2$. First it is assumed that no other heat transfer paths exist except for the two ends of the conductor.

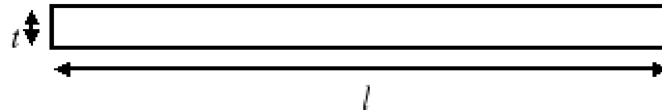



Figure 2.5. Dimension of copper trace.

With the loss $P$ calculated in the previous section, the temperature distribution of the conductor can be obtained by solving the heat transfer equations:

$$T(x) = -\frac{P \cdot R_{th}}{2l^2} x^2 - (T_1 - T_2 - \frac{P \cdot R_{th}}{2})x + T_1 \tag{2.14}$$

where $R_{th} = \frac{l}{k \cdot w \cdot t}$ is the thermal resistance, and k is the thermal conductivity.

When $P < 2(T_1 - T_2)/R_{th}$, $T_1$ is the maximum temperature. The temperature distribution is shown as Figure 2.6.

Figure 2.6. Temperature distribution when $P < 2(T_1 - T_2)/R_{th}$.

When $P > 2(T_1 - T_2)/R_{th}$, the temperature distribution is as shown in Figure 2.7. The maximum temperature will occur in the middle of conductor.

$$T_{\max} = \frac{P \cdot R_{th}}{8} + (T_1 + T_2)/2 + \frac{(T_1 - T_2)^2}{2P \cdot R_{th}} \tag{2.15}$$

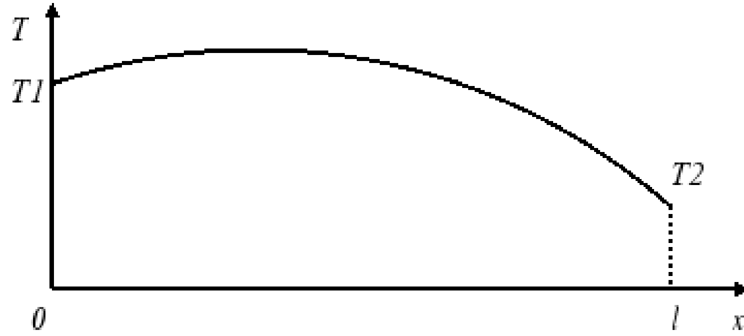



Figure 2.7. Temperature distribution when $P > 2(T_1 - T_2)/R_{th}$.

It should be noted that in this case, the heat is actually flowing out of the conductor from both ends. This may not be desirable in practice since it means that the heat is flowing from the conductor to the silicon device.

Maxwell Thermal Solver is used to verify the thermal model. Figure 2.8 shows the temperature distribution of the conductor with a 1 mm * 1 mm cross-section and 50 mm length. The power loss is 1 W in this case, and $R_{th}$ is 125 K/W. Therefore,

$$P = 1W < 2(T_1 - T_2)/R_{th} = 1.6W \tag{2.16}$$

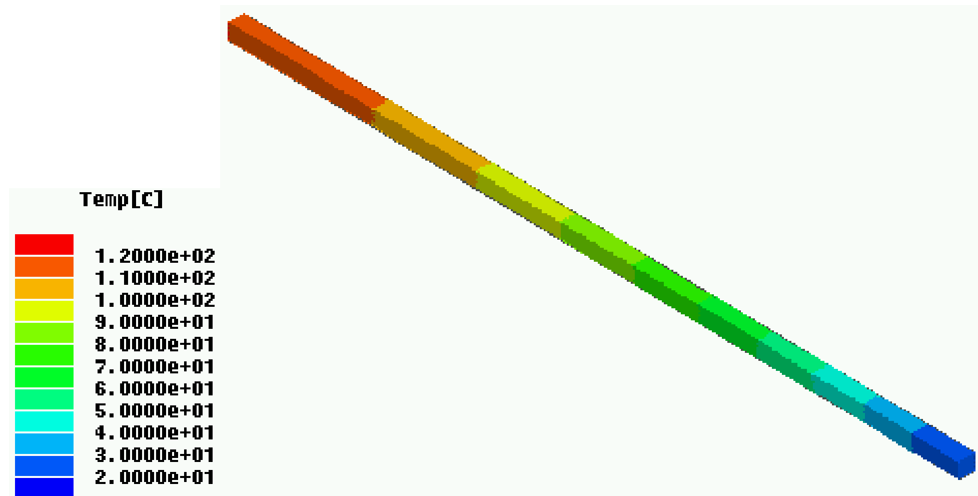



Figure 2.8. Maxwell simulation results when $P < 2(T_1 - T_2)/R_{th}$.

Figure 2.9 shows the calculated temperature using the model, which is very close to the simulation results.

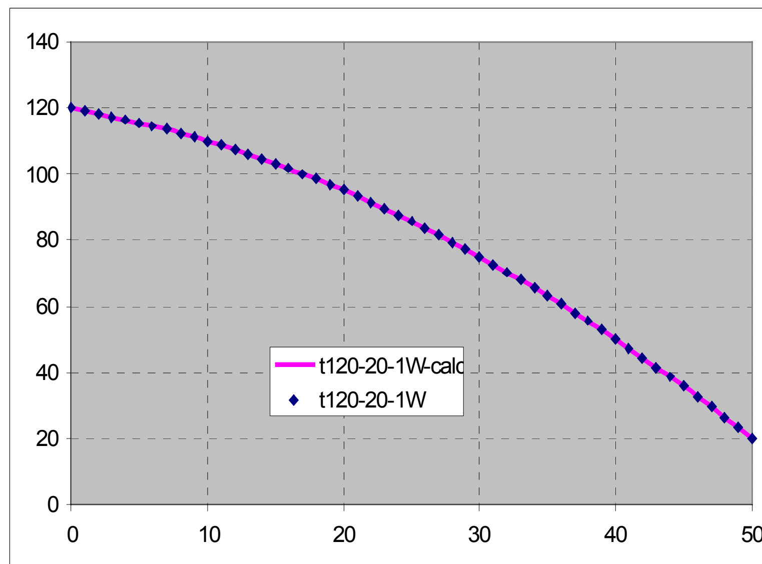



Figure 2.9. Comparison of Temperature distribution when $P < 2(T_1 - T_2)/R_{th}$.

For the same conductor, if the power loss is 18 W, then

$$P = 18W > 2(T_1 - T_2)/R_{th} = 1.6W \ . \tag{2.17}$$

Figure 2.10 shows the temperature distribution from the Maxwell Thermal simulation. The maximum temperature is 353 K, according to equation (2.15), which is same as the simulation results. Figure 2.11 shows the calculated temperature using the model, which is again very close to the simulation results.

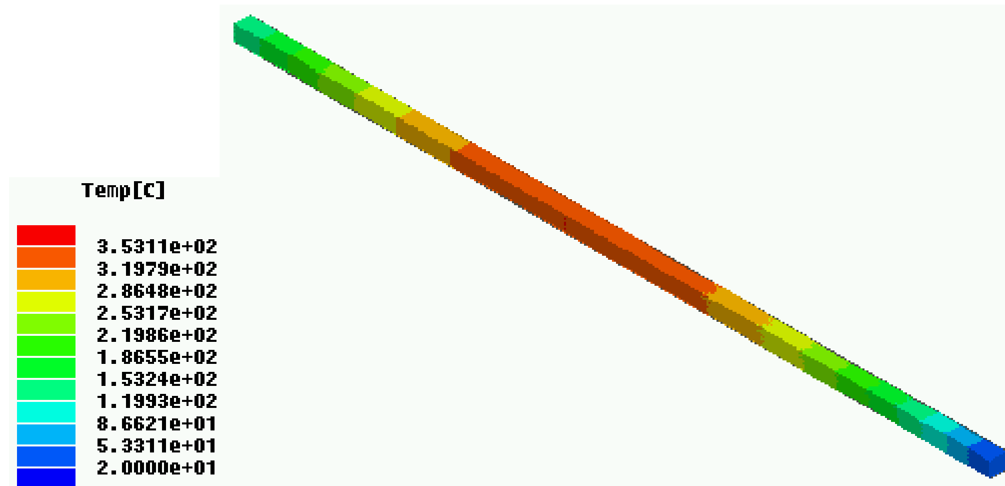



Figure 2.10. Maxwell simulation results when $P > 2(T_1 - T_2)/R_{th}$ .

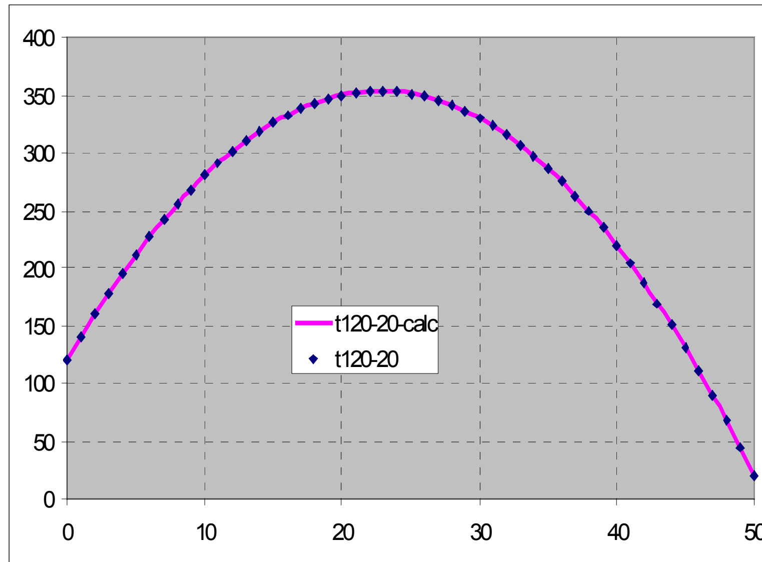



Figure 2.11. Comparison Temperature distribution when $P > 2(T_1 - T_2)/R_{th}$.

**Case 2:** $H \neq 0$

For the copper trace on the DBC board, the H value is considerably larger since all the heat must go though the copper-ceramic interface.

Similar results can be obtained by solving the heat transfer equations if the constant H boundary is assumed in the bottom surface of the conductor regarding ambient temperature $T_a$, as shown in Figure 2.12.

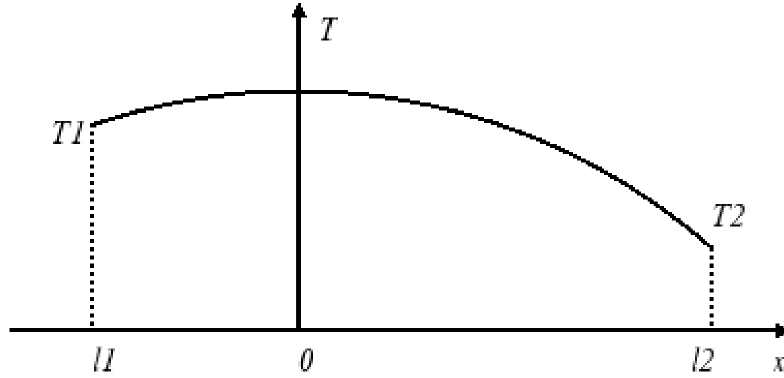



Figure 2.12. Temperature distribution when $H \neq 0$.

$$T(x) = c \cdot \cosh(\sqrt{k_2}\, x) + k_1 / k_2 \tag{2.18}$$

where

$$k_1 = \frac{P \cdot R_{th}}{l^2} + \frac{H \cdot w \cdot R_{th}}{l} T_a \tag{2.19}$$

$$k_2 = \frac{H \cdot w \cdot R_{th}}{l} \tag{2.20}$$

$$c = \frac{T_1 - k_1 / k_2}{\cosh(\sqrt{k_2}\, l_1)} \tag{2.21}$$

$$e^{\sqrt{k_2} l_1} = \sqrt{\frac{(k_1 / k_2 - T_1) e^{\sqrt{k_2} l} - (k_1 / k_2 - T_2)}{(k_1 / k_2 - T_2) - (k_1 / k_2 - T_1) e^{-\sqrt{k_2} l}}} \tag{2.22}$$

Figure 2.13 shows the temperature of the same conductor, with H = 100 W/(K*m$^2$), when loss is equal to 1 W, 2 W, 10 W and 18 W. It can be seen that the model calculated value is almost same as the Maxwell thermal simulation result.

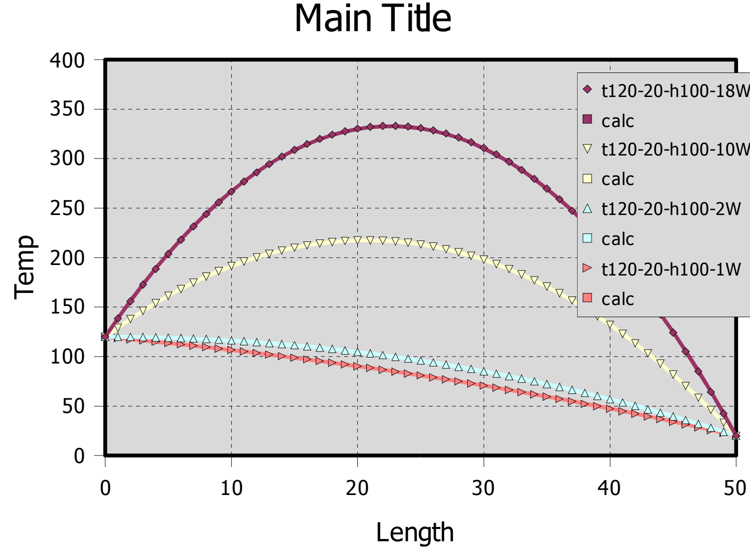



Figure 2.13. Comparison of Temperature distribution when $H \neq 0$.

The boundary condition when $T_{max}$ occur at $x = 0$ is:

$$P = H \cdot w \cdot l \frac{\cosh(\sqrt{\frac{H \cdot l^2}{k \cdot t}}) \cdot (T_1 - T_a) - (T_2 - T_a)}{\cosh(\sqrt{\frac{H \cdot l^2}{k \cdot t}}) - 1} \tag{2.23}$$

when $H \to 0$, $P \to 2(T_1 - T_2)/R_{th}$ which agrees with the $H = 0$ case.

For the conductor above, the boundary loss $P$ = 2W, and the cyan curve in Figure 2.13 is the boundary condition.

## 2.4. Design Rules

**DC case:**

In order to minimize the junction temperature of the silicon device, it is desirable that part of the heat generated by the device can dissipate through the deposited copper trace. For the H = 0 case, this means $P < 2(T_1 - T_2)/R_{th}$.

At very low frequency, $P = I^2 R_{dc}$, therefore, we can have:

$$\frac{w \cdot t}{l} > \frac{I}{\sqrt{2\sigma \cdot k(T_1 - T_2)}} \tag{2.24}$$

For example, if we want to conduct a 20 A current, with $T_1 - T_2 = 10\,\mathrm{K}$, $w$ = 10 mm and $l$ = 20 mm. In order to meet the above requirements, the thickness of the copper layer must be larger than 0.06 mm (2.3 mil or 1.7 ounce). Therefore in this case, we shall not use 1 ounce copper PCB board.

Another example would be the copper trace of the O terminal in the IPEM. Because of the huge d*v*/d*t* associated with this conductor, it is crucial that we minimize the product of width and length in order to minimize the common-mode capacitance. While we choose to have a smaller width, we also have to choose the corresponding thickness to be larger than the minimum value determined by the equation. For the above example if we choose to decrease width by half, we will have to double the minimal thickness.

**AC case:**

Similarly, for the current at frequency higher than the DC case, we have:

$$\frac{w\cdot t}{l}\cdot\frac{1}{[1+(f/f_l)^2+(f/f_h)^{5.5}]^{1/22}}>\frac{I}{\sqrt{2\sigma\cdot k(T_1-T_2)}} \tag{2.25}$$

Considering the previous example, the minimum thickness is 2.8 mil at 200 kHz, 3.5 mil at 2 MHz, and 8.6 mil at 20 MHz. Since the above equation is valid for all frequencies, we can also use it to calculate the DC case, which results in the same 2.3 mm minimal thickness.

In a practical situation, because of the ground plane and proximity effect, the AC resistance of the copper conductor can be twice as high as the AC resistance of the single isolated conductor [2-7]. Therefore, we should add some margin to the minimum thickness considered above.

for $H\neq 0$ the case, we can have:

$$w^2t\cdot\frac{\cosh(\sqrt{\frac{H\cdot l^2}{k\cdot t}})\cdot(T_1-T_a)-(T_2-T_a)}{\cosh(\sqrt{\frac{H\cdot l^2}{k\cdot t}})-1}\cdot\frac{1}{[1+(f/f_l)^2+(f/f_h)^{5.5}]^{1/22}}>\frac{I^2}{\sigma\cdot H} \tag{2.26}$$

In term of meeting the boundary requirements, this case has loose constraints compared with the $H = 0$ case, because the additional heat transfer path helps to cool down the whole

conductor. In order to simplify the calculation, we can use equation (2.25) to calculate the minimal thickness, which will guarantee to work in the case of $H \neq 0$.

However, as shown in Figure 2.14, the minimum thickness required differs quite a lot in the cases when H = 0 and H = 100. Therefore, in order to better utilize the deposited copper layer in the IPEM, it is better to solve the complicated equation shown above than to rely on the very conservative H = 0 case.

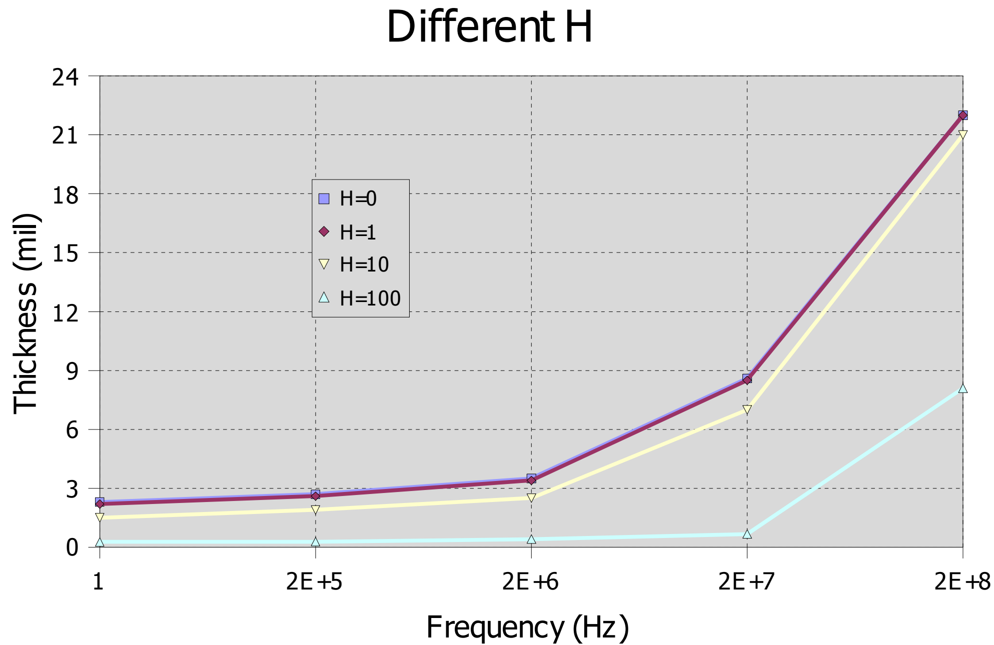



Figure 2.14. Minimum thickness for different H values.

## 2.5. Summary

Based on integrated electro-thermal study, the method to develop rules for a rule-based layout design has been demonstrated for the first time.

It has been shown that for the deposited copper trace in “embedded power” IPEM, H = 0 is a reasonable assumption, while for DBC copper traces, a large H value has to be considered.

Based on the models, guidelines for copper trace design are proposed. The minimal thickness of the copper tracer can be determined by using the derived analytical equation at all frequencies.

# Chapter 3. Electrical and Thermal Model of IPEM

This chapter presents the electrical and thermal model of the DC-DC IPEM. The development of these models is the critical portion of integrated design methodology, which will be illustrated in later chapters.

In the beginning, the fundamental principles of partial element equivalent circuit (PEEC) are reviewed. Then of two software tools based on the PEEC method, the Maxwell Q3D Extractor was chosen for this study over InCa, based on functionality and convenience for software integration. For the “embedded power” IPEM, the parasitic inductance and capacitance are calculated by using Maxwell Q3D Extractor. The modeling technique and procedure are described in detail. The simulation results are then verified by the impedance measurements. The “embedded power” IPEM is compared with discrete module and traditional wire bond IPEMs, in terms of parasitic parameters. Finally, the thermal model of IPEM, which will be used later in the integrated design, is also presented.

## 3.1. Introduction

Parasitic inductance stores energy when current flows through it. When the device needs to be turned off, the energy is released in the form of a voltage spike if no external snubber circuit exists. The spike is a function of the inductance and the di/dt rate, and the di/dt rate becomes larger at higher switching frequencies. To improve long-term reliability,

it is required that the parasitics be small enough to limit the spike. Furthermore, the common-mode capacitance needs to be reduced in order to meet the EMI standard. Therefore, it is important to use analysis tools to calculate the parasitic inductance and the capacitance of the IPEM.

Conventionally, electromagnetic field simulation is done at device or component level, using finite element analysis (FEA) by solving the Maxwell's differential field equations. When it comes to the interconnections between components, full field simulation requires extensive computation because of the complex structure, and sometimes shows poor convergence. In addition, it requires the predetermination of the current loop for calculation. This is difficult for power converters because current loops may vary in different sub-topologies, which are determined by the switching combinations of semiconductor devices. Also, very often system designers want to look at the effects of different interconnect or layout design on overall performance, such as efficiency, device switching characteristics, and EMI, which can't be obtained directly by EM field simulation.

The PEEC method [3-1] uses Maxwell's integral equations instead of differential equations and calculates inductance analytically, based on the geometry and material information only. It also breaks the loop inductance into the partial inductance associated with each trace, and relates these partial inductances with mutual inductances, so that the overall loop inductance can be easily computed for any arbitrary combination of traces. Therefore, it can easily be applied to nonlinear switching circuits.

Nowadays, the PEEC method has been widely applied to both VLSI and power semi-conduction device modeling [3-2]-[3-5]. Its success is due to the following factors: first, there are commercial software tools, for example Maxwell Q3D Extractor, available to extract the models, and it is considerably faster than electromagnetic field simulation. Therefore they are more suited in high-level system simulation, or when large number of design iterations are involved. Second, it is very convenient to combine PEEC models with other component models for a circuit simulator like SPICE. Because of this, it is very easy for a system designer to look at converter efficiency, power device utilization and EMI filter design. Last, PEEC models work well both in time and frequency domains.

In terms of an experiment-based approach, there are two methods to measure the parasitic parameter: time-domain-reflectometry (TDR) -based measurement [3-6] and impedance measurement [3-7]. While the TDR method requires complicated experimental measurements and special hardware (TDR/sampling hear) and software, impedance measurement is simple and straightforward. In our case, impedance measurement was used to verify the Maxwell Q3D simulation results.

The purpose of this chapter is to develop and verify the electrical model, including parasitic parameters for the IPEM. Then the IPEM was compared with traditional wire bond IPEMs, in terms of parasitic parameters.

## 3.2. PEEC Method Illustration

The loop inductance of the rectangular loop formed by four traces, as shown in Figure 3.1(a), is defined as:

$$L_{loop} = \frac{1}{I} \oiint_S \vec{B} \cdot d\vec{s} \tag{3.1}$$

where $I$ is the conduction current, $\vec{B}$ is the magnetic flux intensity, and $s$ is the loop area.

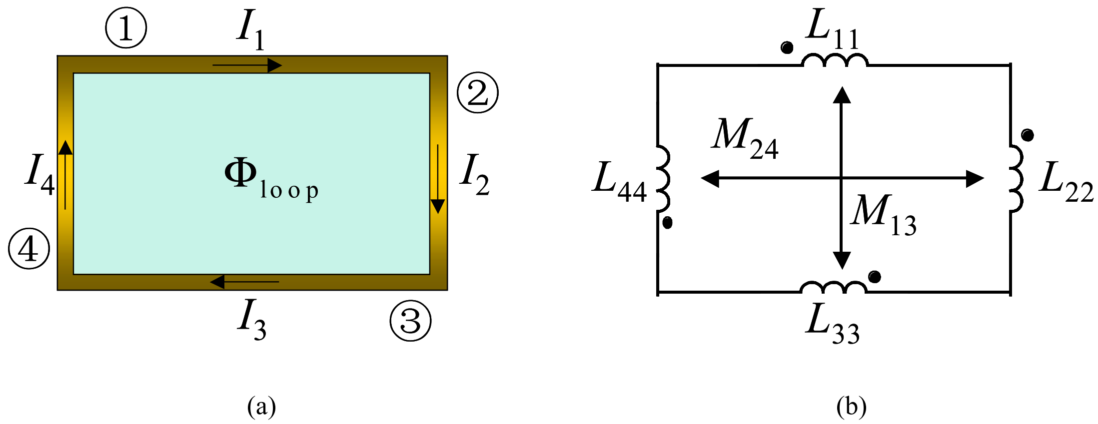



Figure 3.1. A rectangular shaped loop described with PEEC method: (a) loop layout, (b) equivalent circuit representation.

Using the Maxwell equation, $\vec{B} = \nabla \times \vec{A}$, and the Stokes' theorem $\oiint_S (\nabla \times \vec{X}) \cdot d\vec{s} = \oint_C \vec{X} \cdot d\vec{l}$, $L_{loop}$ can be rewritten as

$$L_{loop} = \oint_C \vec{A} \cdot d\vec{l} = \frac{1}{I}[\sum_{n=1}^{4} \int \vec{A} \cdot d\vec{l}\,] \tag{3.2}$$

where $\vec{A}$ is the magnetic potential, and can be decomposed into the contribution from each traces, i.e.,

$$\vec{A} = \sum_{m=1}^{4} \vec{A}_{l_m} \tag{3.3}$$

where $\vec{A}_{l_m}$ is the magnetic potential generated by the current flowing through $l_m$.

Then combining Equations (3.2) and (3.3) give

$$L_{loop} = \frac{1}{I}[\sum_{n=1}^{4}\sum_{m=1}^{4}\int_{l_n} \vec{A}_{l_m} \cdot d\vec{l}\,] \tag{3.4}$$

Let $L_n = \frac{1}{I}\int_{l_n} \vec{A}_{l_m} \cdot d\vec{l}$ and $M_{mn} = \frac{1}{I}\int_{l_n} \vec{A}_{l_m} \cdot d\vec{l}$ when $m \neq n$, Equation (3.4) becomes

$$L_{loop} = \sum_{n=1}^{4} L_n + \sum_{n=1}^{4} \sum_{m=1 m\neq n}^{4} M_{mn} \tag{3.5}$$

Therefore, the loop inductance can be expressed as the combination of the trace partial self-inductance $L_n$, and partial mutual-inductance, $M_{mn}$ ($M_{mn} = M_{nm}$). The representation of using an equivalent circuit is shown in Figure 3.1(b). It should be noted that in this rectangular loop example, only the paralleled traces have mutual inductance between them, i.e., $M_{12} = M_{23} = M_{34} = M_{41} = 0$, because perpendicular traces have null induced fields.

There are several improvements that have been proposed for the original PEEC method. [3-8] described how to compute inductance and resistance of any simple loop

located near a conductive plane. The image method was used to take the ground plane into account, when assuming infinite ground plane dimension and conductivity.

[3-9] extended the PEEC method to include retardation. Retardation is the effect of finite speed of electromagnetic signals. It was shown in this paper that the inclusion of retardation made PEEC equivalent to a full-wave solution of Maxwell's equation. Therefore, as long as enough "lumps" are used, the resulting model holds for all configurations and frequencies except extremely low ones, which made it possible for circuit models to predict EMI.

There have also been several improvements made to the efficiency of capacitance calculation [3-10]-[3-13].

## 3.3. InCa Model of PCB Layout

InCa [3-14][3-15] is a software tool developed using the PEEC concept to calculate inductance based on geometry and material information. Figure 3.2 shows the InCa model of a loop inductor.

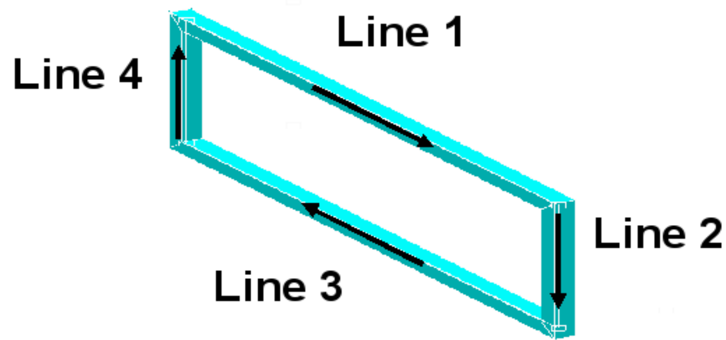



Figure 3.2. InCa Model of loop inductor

Table 3.1 shows the InCa results with comparison of the Maxwell FS3D simulation and analytical calculation. It can be seen that the difference is within 10%.

Table 3.1. Inductance Calculation Results of loop inductor.

| | Inca | | | | | Maxwell | Appr. |
|---|---|---|---|---|---|---|---|
| | Line 1 | Line 2 | Line 3 | Line 4 | Eqv. L | | |
| Line 1 | 2.35 | 0 | -0.66 | 0 | 1.69 | / | 1.72 |
| Line 2 | 0 | 0.57 | 0 | -0.03 | 0.54 | / | 0.79 |
| Line 3 | -0.66 | 0 | 2.35 | 0 | 1.69 | / | 1.72 |
| Line 4 | 0 | -0.03 | 0 | 0.57 | 0.54 | / | 0.79 |
| Total Loop | / | / | / | / | 4.46 | 4.21 | 5.02 |

For more complicated geometry, such as that shown in Figure 3.3 for a four-channel interleaved VRM or PEBB module [3-16], InCa is not very convenient in inputting the 3D structure directly, nor does it provide geometry import function using standard file formats. In addition, it is very difficult to interface with InCa in batch mode, because of its lack of macro language support. Therefore, Maxwell Q3D Extractor is chosen for further study.

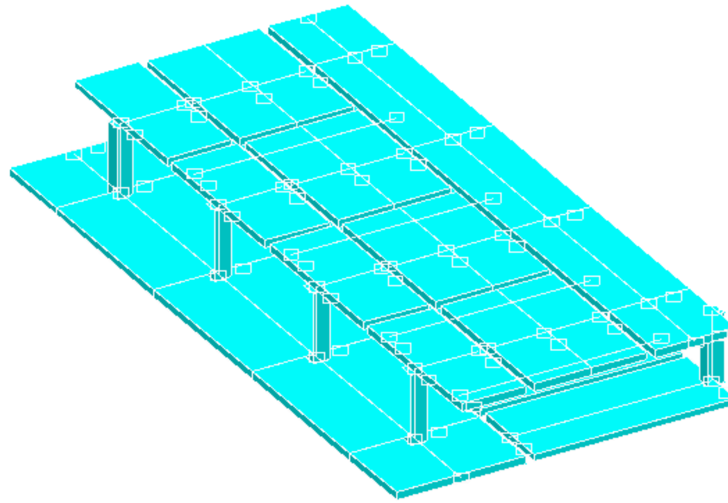


Figure 3.3. InCa Model of four channel VRM layout

### 3.4. Electrical Model of “Embedded Power” IPEM

The integrated power electronics module (IPEM), consisting of two MOSFETs in bare-die form and a hybrid gate driver, is packaged using “embedded power” technology, a hybrid MCM-based packaging technology. As shown in Figure 3.4, the two bare chips of MOSFETs are buried in a ceramic frame, and covered by a dielectric layer with etched holes over the aluminum pads of the chips. The power devices are -connected to the rest of circuits by metal deposition. This new packaging method eliminates wire bonds, which could lead to potential benefits in terms of parasitic parameters.

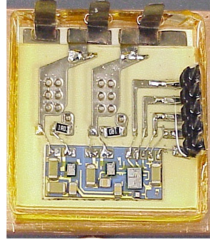


Figure 3.4. IPEM packaged using "embedded power" technology.

### 3.4.1. Model Development

Table 3.2 lists the components used in this module. Figure 3.5 shows the IPEM model in Maxwell Q3D extractor. The general steps of using Maxwell Q3D Extractor are listed as follows:

1. Solid model creation. A geometry model can be created in its 3D solid modeler or imported from another MCAD system in STEP or IGES format.
2. Material setup.
3. Conductor setup to assign a net.
4. Boundary setup. In this step, the source and sink of current are specified. Therefore, the current paths are determined.
5. Solution setup, including meshing and convergence criteria.
6. Solve.

The parasitic inductance and capacitance results from the Maxwell Q3D Extractor analysis on the IPEM are shown in Table 3.3 and Table 3.4, respectively. The diagonal elements in Table 3.3 are self-inductance. The diagonal elements in Table 3.4 are capacitance-to-ground, where the bottom copper layer of DBC was assumed to be ground. The non-diagonal elements in both tables are the mutual inductance and mutual capacitance.

Table 3.2. Components Used in the "embedded power" IPEM

| Part | Part Number/ Thickness | Description |
|---|---|---|
| MOSFET | IXFD26N50 | 500V/26A |
| Copper | 12mil | Top layer of DBC |
| $Al_2O_3$ | 25mil | Middle layer of DBC |
| Copper | 12mil | Bottom layer of DBC |
| $Al_2O_3$ | 35mil | Surrounding layer |
| Copper | 10mil | Deposited layer |

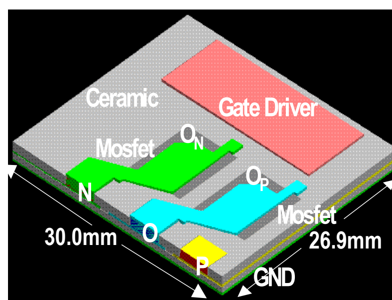



Figure 3.5. Maxwell model of the "embedded power" IPEM.

Table 3.3. Inductance Matrix (nH) of the "embedded power" IPEM.

| Terminal | P | N | $O_P$ | $O_N$ |
|---|---|---|---|---|
| P | 1.0 | 0.2 | -0.6 | -0.3 |
| N | 0.2 | 3.1 | -0.7 | -0.4 |
| $O_P$ | -0.6 | -0.7 | 3.4 | 0.4 |
| $O_N$ | -0.3 | -0.4 | 0.4 | 1.2 |

Table 3.4. Capacitance Matrix (pF) of the "embedded power" IPEM.

| Conductor | P | N | O |
|---|---|---|---|
| P | 20 | 0.3 | 7.0 |
| N | 0.3 | 5.1 | 8.6 |
| O | 7.0 | 8.6 | 20 |

The entire inductance and capacitance matrix were then imported to Saber as one component, as shown in Figure 3.6. Together with the device model, it can be simulated in Saber to get the impedance curve of the IPEM.

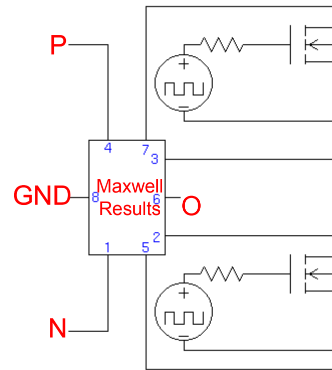



Figure 3.6. Saber model of the "embedded power" IPEM.

The device model we used in Saber is for IXFH26N50, since there is no model for IXFD26N50. While IXFH26N50 uses the TO-247 package and IXFD26N50 is in bare-die form, they use the exact same die. Furthermore, Saber simulation was conducted to make sure that the Saber model of IXFH26N50 did not include any package inductances and capacitances.

Figure 3.7 shows the Saber simulation result with the IXFH26N50 model when the MOSFET was off and DC bias voltage was 5 V. The black curve is the simulation result. The light gray curve is fitted curve with C = 1.4 nF, which overlaps with simulation curve. It clearly shows that package inductances were not included in the model. Because a typical TO-247 package will have an inductance of around 20 nH for the drain-to-source path [3-17], a resonant frequency of 30 MHz would have shown in the impedance plot if the package inductances were modeled. According to the data sheet, the $C_{oss}$ is around 1.2 nF, which is close to the simulation result.

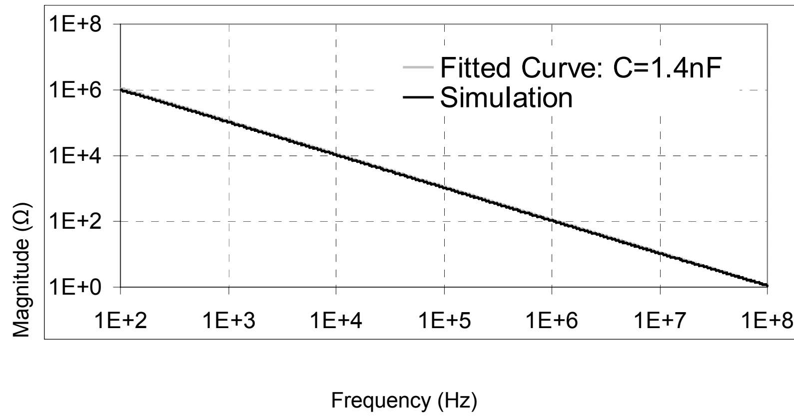



Figure 3.7. IXFH26N50 model characteristic, when switch was off, DC bias = 5 V.

Figure 3.8 shows the simulation result when the MOSFET was on. The $R_{DS(on)}$ is 0.16 Ω, which is slightly different from the data sheet value as 0.2 Ω. According to our measurement, $R_{DS(on)}$ is closer to 0.2 Ω, as will be seen in the next section.

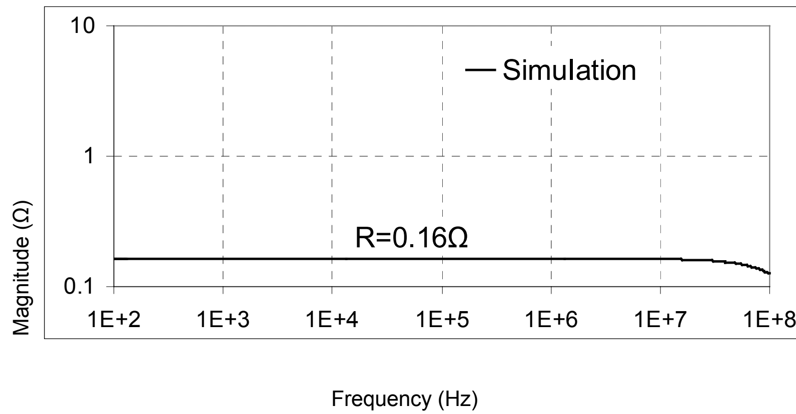



Figure 3.8. IXFH26N50 model characteristic, when switch was on, DC bias = 0 V.

### 3.4.2. Impedance Measurement

Impedance measurement was used to verify the Maxwell Q3D simulation results. The IPEM was measured using the Agilent 4294A precision impedance analyzer, which has a frequency range of 40 Hz to 110 MHz. The measurement setup is shown in Figure 3.9. The sweeping source was set with a magnitude equal to 0.1 V and frequency from 100 Hz to 100 MHz. In order to measure the parasitic inductance, the 42941A Pin Probe from the impedance analyzer was either connected to P and O, as shown in Figure 3.9, or connected to O and N. After the calibration of the impedance analyzer and probe, a set of impedance curves was obtained under various conditions, including under different DC bias voltages andthe switch turned on or off.

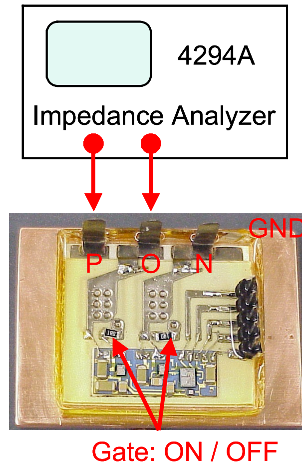



Figure 3.9. Impedance measurement setup.

Figure 3.10 is the impedance curve between terminal P and O, when the switch was turned off and the DC bias between P and O was 5 V. In this case, the switch should behave like a single capacitor ($C_{oss}$). The black curve is the measured curve. The dark gray

curve is the L-C-R fitted curve, which overlaps with the measured curve. According to the fitted curve, L is equal to 3.5 nH. Since the impedance analyzer can only measure loop inductance, this L should correspond to the P - $O_P$ loop in Table 3.3. The loop inductance from Table 3.3 is $L_{PP} + L_{O_PO_P} + L_{PO_P} + L_{O_PP} = 3.2\ \text{nH}$, which is close to the measured value. The light gray curve is from Saber simulation, while taking the entire inductance and capacitance matrix into consideration. As can seen from Figure 3.10, the simulated curve agrees with the measurement very well, for both magnitude and phase.

In this case, according to the fitted curve, C is equal to 1.0 nF, which is close to the data sheet $C_{oss}$ value of 1.2 nF. Since all the inductance and capacitance values are quite close, the resonant frequencies also match well.

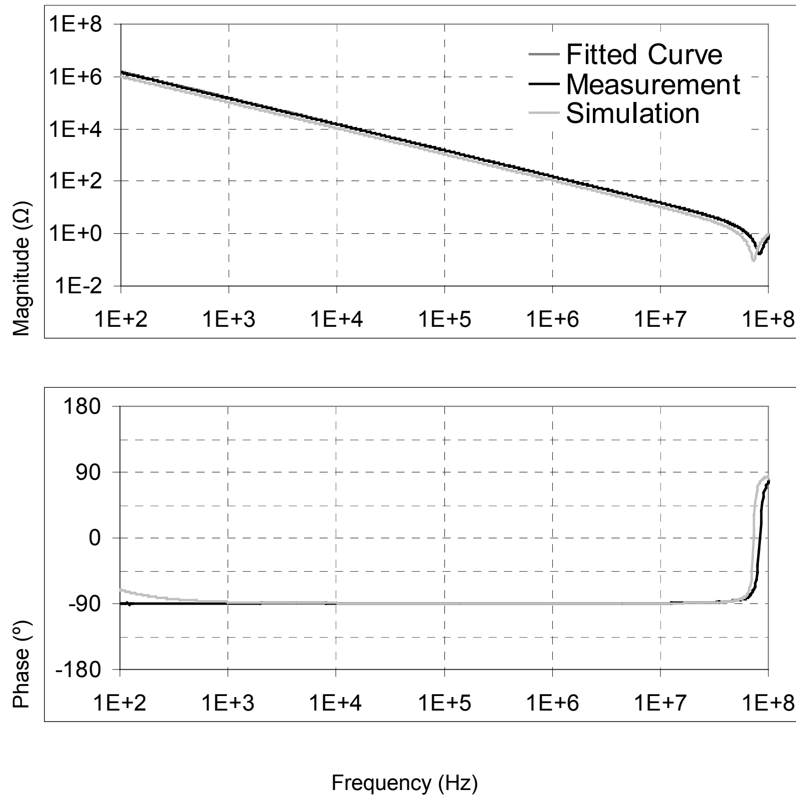



Figure 3.10. Impedance curve between P and O, when switch was off, DC bias = 5 V.

Figure 3.11 is the impedance curve measured between P and O when the switch was turned on. Since the switch was on, it behaved like a single resistor ($R_{DS(on)}$). For inductance, since we measured the same loop as in the previous case, we should expect the same inductance value. The black measured curve and the overlapped dark gray L-R fitted curve show that *L* is equal to 3.5 nH, which is again close the simulated value. The light gray curve is the Saber simulation result. The only major discrepancy between simulation and measurement is the $R_{DS(on)}$ value. The reason for this is that in measurement, $R_{DS(on)}$ is equal to 0.2 Ω, while in the device Saber model $R_{DS(on)}$ is equal to 0.16 Ω, as shown in the previous section. In this case, the fitted curve shows that C is equal to 4.7 nF, which is quite different from the previous case because of the nonlinearity of $C_{oss}$.

Measurements were also conducted between O and N. Similar results were observed.

In order to verify the capacitance matrix, the impedances between P and GND (the bottom copper layer of DBC), O and GND, O and GND were measured, as shown in Figure 3.12. Because the $C_{oss}$ of the switch is at least ten times larger than the parasitic capacitance as shown in Table 3.4, the measured curve for P and GND, N and GND, O and GND are so close that they all overlap each other. According to the C fitted curve for O and GND, the total measured C is equal to 45 pF, while the sum of the diagonal elements in Table 3.4 is 45.1 pF. The light gray curve is the Saber simulation result, which is still very close to the measurements.

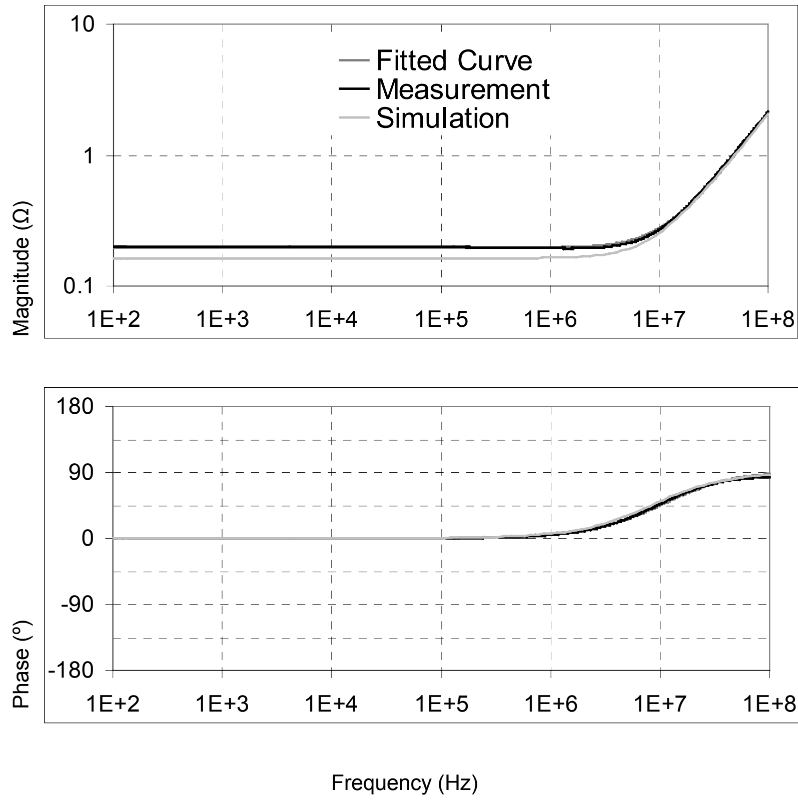



Figure 3.11. Impedance curve between P and O, when switch was on, DC bias = 0 V.

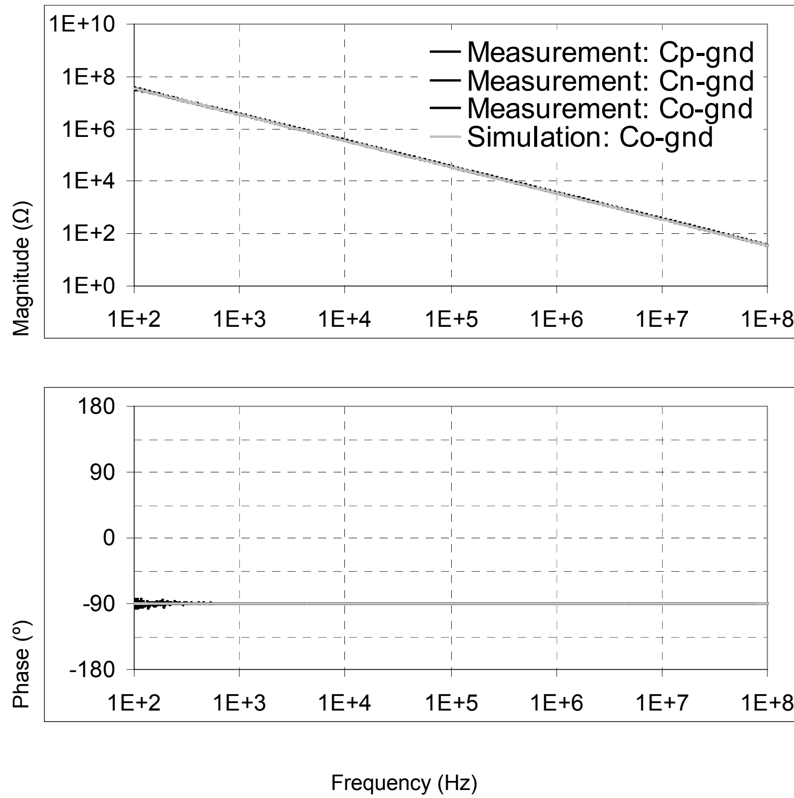



Figure 3.12. Impedance curve between P and GND, O and GND, N and GND when switch was off, DC bias = 0 V.

### 3.4.3. Conclusions

The Maxwell Q3D model was developed for "embedded power" IPEM. Impedance measurement results verified the loop inductances when the switch is both on and off. The capacitances between three terminals and ground were verified using impedance measurements as well.

## 3.5. Electrical Model of wire-bonded IPEM

A wire-bond IPEM, as shown in Figure 3.13, consists of two MOSFETs, which are soldered on one side of the Aluminum Oxide Direct Bonded Copper (DBC) board. The component list is shown in Table 3.5. The copper substrate of DBC is etched to give the desired pattern. A wire-bonding technique is used to connect the MOSFETs and the copper substrate of DBC board. Another side of the DBC board, which is also copper substrate, can be attached to the heat sink directly.

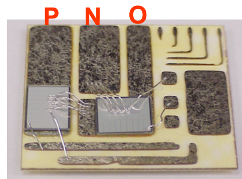



Figure 3.13. Wire-bonded IPEM.

Table 3.5. Components used in the wire-bonded IPEM.

| Part | Part Number | Description |
|---|---|---|
| MOSFET | IXFD21N50 | 500V/20A |
| Copper | 12mil (thickness) | Top layer of DBC |
| Aluminum Oxide | 25mil (thickness) | Middle layer of DBC |
| Copper | 12mil (thickness) | Bottom layer of DBC |
| Wirebond | 15mil (diameter) | 4 in parallel |

Figure 3.14 shows the Maxwell model of IPEM and Table 3.6 and Table 3.7 shows the extracted parasitic inductance and capacitance value.

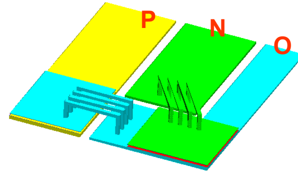



Figure 3.14. Maxwell model of the wire-bonded IPEM.

Table 3.6. Inductance Matrix (nH) of the wire-bonded IPEM.

| Terminal | P | N | $O_P$ | $O_N$ |
|---|---|---|---|---|
| P | 5.7 | 2.6 | -1.4 | -1.4 |
| N | 2.6 | 8.9 | -3.1 | -3.5 |
| $O_P$ | -1.4 | -3.1 | 11.8 | 8.1 |
| $O_N$ | -1.4 | -3.5 | 8.1 | 8.0 |

Table 3.7. Capacitance Matrix (pF) of the wire-bonded IPEM.

| Conductor | P | N | O |
|---|---|---|---|
| P | 25 | 0.1 | 33 |
| N | 0.1 | 16 | 34 |
| O | 33 | 34 | 23 |

In order to verify whether the voltage spike is within the limits of the device, the equivalent circuit of IPEM, together with the passive components, source, and load, can be

entered into Saber to perform transient simulation. Figure 3.15 shows the tester circuit in Saber. From this Saber simulation, we can also get the power losses of devices. Understanding these losses is very critical when performing the thermal analysis in the later chapters.

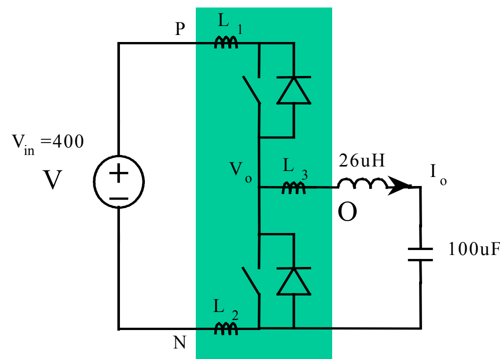



Figure 3.15. Tester circuit in Saber for the wire-bonded IPEM.

In order to verify the electrical model, simulation results are compared with the experimental results. A tester has been build to test the IPEMs. The circuit diagram is the same as Figure 3.15, which is a half-bridge structure with an inductive load. The switching frequency is 200kHz. The duty cycles of the two MOSFETs are 50%, and they conduct complementarily.

By comparing the voltage waveform, the validity of the model can be verified. According Figure 3.16 and Figure 3.17, the performance of the module in experiment agrees with the simulation results. Both the voltage overshoot and the oscillation frequency match. Therefore this model can be used for further study.

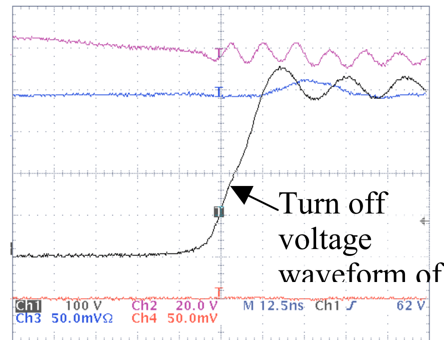



Figure 3.16. Experimental result of the wire-bonded IPEM.

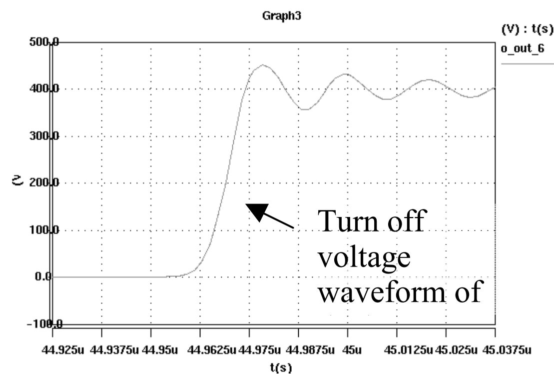



Figure 3.17. Saber simulation result of the wire-bonded IPEM

Both simulation and experimental result show that there is a voltage overshoot of about 50V during the turn-off period of the device. This is induced by the parasitic inductance of layout. In order to minimize the voltage overshoot of the device, special consideration is needed when designing the layout. The software packages we used above provide us tools to see the effect of different layouts by performing simulations instead of by building prototypes.

Impedance measurements were also conducted for this module and again agreed with simulation results[3-18].

### 3.6. Electrical Model of Discrete DC-DC Module

The parasitic inductance of the discrete DC-DC module, as shown in Figure 3.18, was also calculated using Maxwell Q3D. According to the simulation results, the PCB traces from terminal P and O to the device have about 7 nH inductance. From the data sheet we know that the TO-247 packaged device itself has about 7 nH inductance for its drain-to-source loop. An impedance measurement of the discrete DC-DC module reveals that the parasitic inductance is a total of 14 nH between terminals P and O, which is close the simulation results.

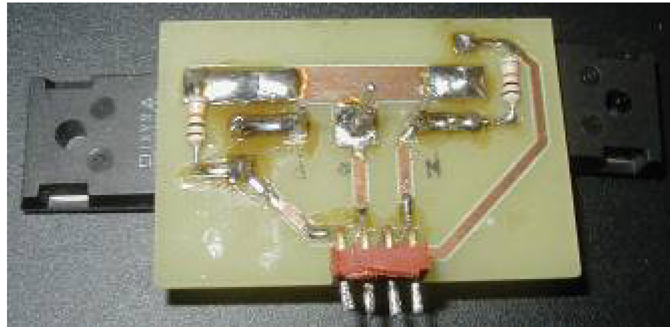


Figure 3.18. Discrete DC-DC module.

### 3.7. Electrical Model of "Embedded Power" PFC IPEM

The "Embedded Power" PFC IPEM was designed with the similar approach of a DCDC IPEM, except that CoolMOS and Sic Diode are used instead of the IXYS MOSFET. In order to handle high current, two CoolMOS and two Sic Diodes are used in

parallel form. Therefore, the physical structure is more complicated than that of DCDC IPEM.

Table 3.8 lists the components used in this module. Figure 3.19 shows the IPEM model in Maxwell Q3D extractor, where the surrounding Al2O3 layer is not solid in order to reveal the internal structure.

The parasitic inductance and capacitance results from the Maxwell Q3D Extractor analysis on the IPEM are shown in Table 3.9 and Table 3.10 respectively.

Table 3.8. Components Used in the PFC IPEM.

| Part | Part Number/ Thickness | Description |
|---|---|---|
| CoolMOS | SPW20N60C3 | 650V / 20A |
| SiC Diode | SDP06S60 | 600V / 6A |
| Copper | 10mil | Deposited layer |
| $Al_2O_3$ | 35mil | Surrounding layer |
| Copper | 12mil | Top layer of DBC |
| $Al_2O_3$ | 25mil | Middle layer of DBC |
| Copper | 12mil | Bottom layer of DBC (GND) |

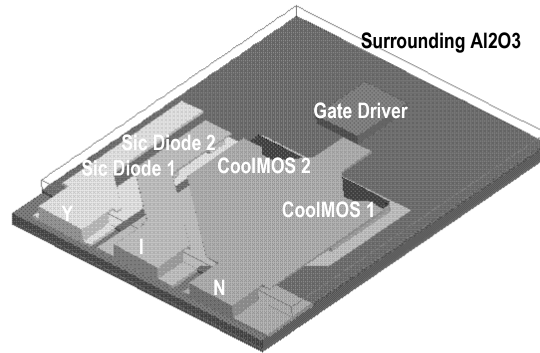



Figure 3.19. Maxwell model of the PFC IPEM.

Table 3.9. Inductance Matrix (nH) of the PFC IPEM.

| Terminal | N: CoolMOS1 | N: CoolMOS2 | I: CoolMOS1 | I: CooLMOS2 | I: Diode1 | I: Diode2 | Y: Diode1 | Y: Diode2 |
|---|---|---|---|---|---|---|---|---|
| N:CoolMOS1 | 3.9 | 3.5 | -1.8 | -1.7 | 1.0 | 1.3 | 0.7 | 1.0 |
| N:CoolMOS2 | 3.5 | 4.9 | -1.1 | -1.9 | 1.5 | 1.9 | 0.7 | 1.1 |
| I:CoolMOS1 | -1.8 | -1.1 | 3.6 | 2.8 | 1.3 | 1.7 | 1.1 | 1.6 |
| I:CooLMOS2 | -1.7 | -1.9 | 2.8 | 3.0 | 1.8 | 2.1 | 1.1 | 1.6 |
| I:Diode1 | 1.0 | 1.5 | 1.3 | 1.8 | 4.3 | 4.7 | -1.2 | -1.7 |
| I:Diode2 | 1.3 | 1.9 | 1.7 | 2.1 | 4.7 | 6.1 | -1.7 | -2.9 |
| Y:Diode1 | 0.7 | 0.7 | 1.1 | 1.1 | -1.2 | -1.7 | 3.3 | 3.9 |
| Y:Diode2 | 1.0 | 1.1 | 1.6 | 1.6 | -1.7 | -2.9 | 3.9 | 5.9 |

Table 3.10. Capacitance Matrix (pF) of the PFC IPEM.

| Conductor | N | I | Y |
|---|---|---|---|
| N | 5.9 | 28.3 | 0.01 |
| I | 28.3 | 28.9 | 4.1 |
| Y | 0.01 | 4.1 | 10.0 |

The simulation results are very similar to that of DC-DC IPEM. The only difference is that in PFC IPEM, we have two parallel current paths because two CoolMOSs and two SiC diodes are used in parallel. As illustrated in Figure 3.20, for conductor Y, we define interface Y as the current source and interfaces Y-D1 and Y-D2 as current sinks. Similarly for conductor I, we define interfaces I-D1 and I-D2 as current sources and interface I as a current sink. The resulting inductance matrix is included in Table 3.9, shown as the highlighted portion. However, whether the simulation result is still valid in this case is not clear.

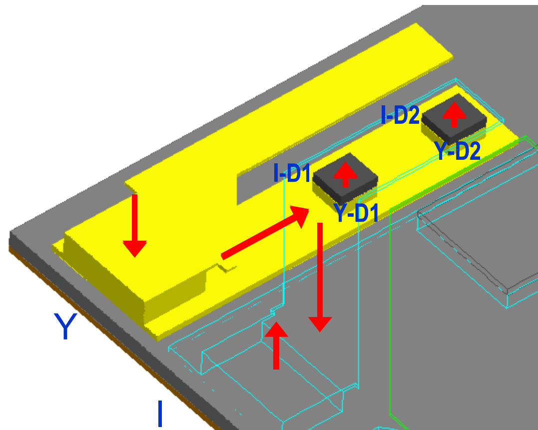



Figure 3.20. Two parallel current paths in Maxwell model of the PFC IPEM.

The same impedance measurement method is used to verify the simulation results. Since the impedance analyzer can only measure loop inductance, the loop inductance must be calculated for the parallel current paths. According to the equivalent circuit shown in Figure 3.21, the loop inductance can be expressed as:

$$L = (K_1 * K_2 - M^2) / (K_1 + K_2 - 2*M) \quad (3.6)$$

Where

$$K_1 = L_1 + L_3 + 2 * M_{13} \quad (3.7)$$

$$K_2 = L_2 + L_4 + 2 * M_{24} \quad (3.8)$$

$$M = M_{12} + M_{23} + M_{34} + M_{14} \quad (3.9)$$

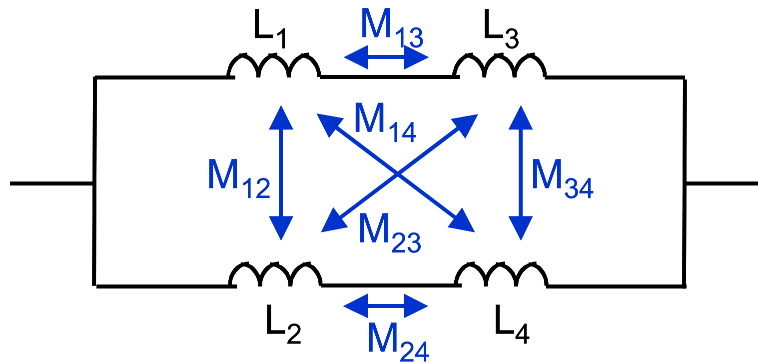



Figure 3.21. Equivalent circuit of two parallel current paths.

Figure 3.22 is the impedance curve measured between I and Y for the Sic Diode loop, when the reverse voltage is 0 V. In this case, the Sic Diode behaved like a single capacitor. The black measured curve and the overlapped dark gray L-R fitted curve show that *L* is

equal to 5.3 nH. Based on Table 3.9 and Equation (3.6), the calculation of loop inductance for the parallel I:Diode1 - Y:Diode1 and I:Diode1 - Y:Diode1 loop gave 5.2 nH, which is very close to the simulated value.

The agreement between experiment measurements and simulation results indicates that Maxwell Q3D calculation is still valid in the case of multiple current sources/sinks, which is quite common in power electronic systems.

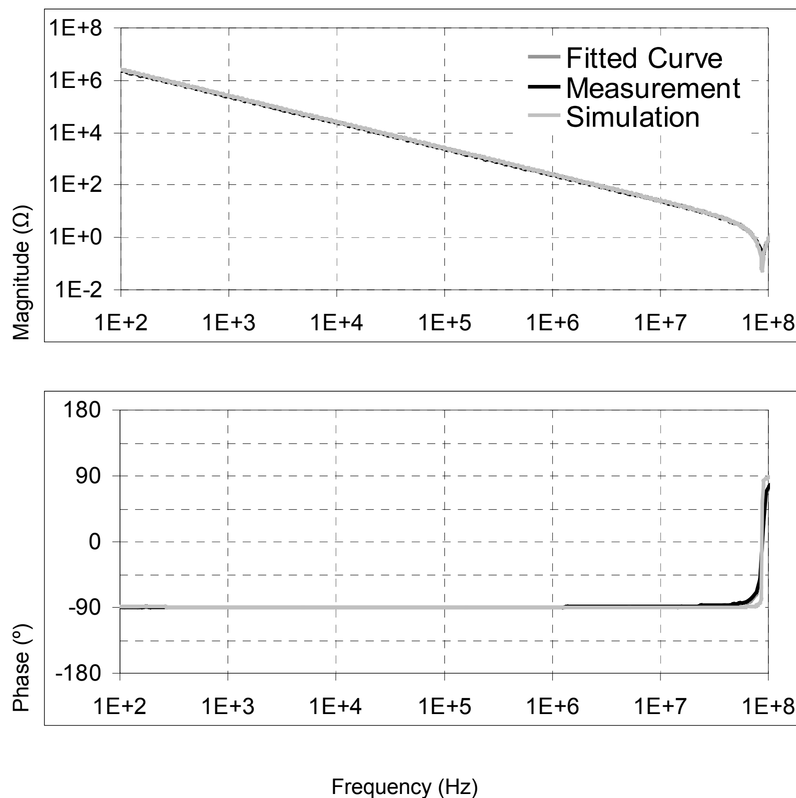


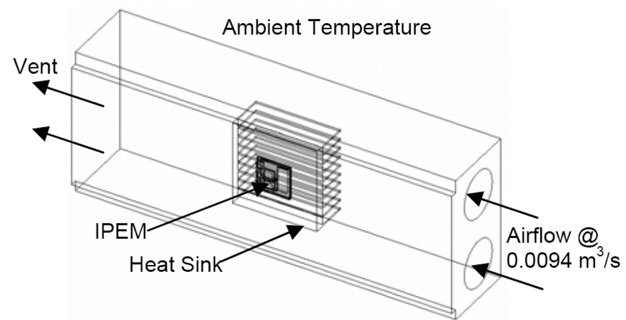

Figure 3.22. Impedance curve between I and Y, when Sic Diodes were off.

## 3.8. Thermal Model of "Embedded Power" IPEM [3-19]

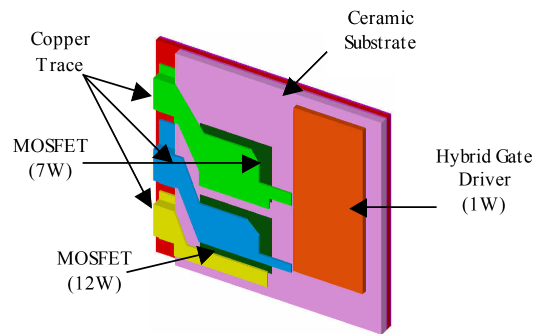
The thermal model of "Embedded Power" IPEM was developed using the commercial finite element software I-DEAS to identify hot spots as well as predict steady-state temperature distributions within the module.

The model included a full 3D IPEM with an optional heat spreader mounted on an aluminum heat sink. A flow channel was included to provide air flow over the model. An inlet fan with a constant volumetric flow rate of 0.0094 m3/s was applied at one end of the channel, while the other end of the channel was vented to an ambient temperature of 50°C, as shown in Figure 3.23(a). The area of the channel was fixed, resulting in an outlet velocity of 1.1 m/s. The top of the module was assumed to be adiabatic.

Each module had three heat sources: two MOSFETs and a gate driver. The two MOSFETs dissipated a total of 19W; 7W of which was for the innermost MOSFET and 12W for the outside MOSFET. The hybrid gate driver only dissipated 1W, as shown in Figure 3.23(b). Due to its relatively low power loss, the gate driver was modeled as a homogeneous ceramic block.




(a)

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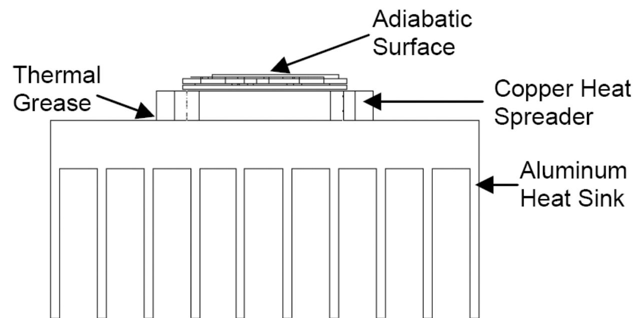



(c)

Figure 3.23. Thermal model of "embedded power" IPEM: (a) Thermal boundary conditions, (b) Details of the IPEM thermal model, (c) Positioning of module on the heat sink.

Fine grids were used for the heat dissipating surfaces. In addition, all soldered components and interfaces with thermal grease (e.g. at the interface between the heat spreader and the heat sink in Figure 3.23(c)) were represented by equivalent thermal resistance values. Within the IPEM model, it was assumed that there was a conduction path from the two heat sources to the copper trace and the surrounding ceramic substrate, from the copper trace to the second DBC ceramic layer, and from the ceramic layer to the bottom copper layer. From there, it was assumed that the major heat-flow paths involved conduction from the IPEM module to the (optional) heat spreader, conduction from the heat spreader to the heat sink, and convection from both the heat spreader and the heat sink to the ambient air. Another path of resistance was from the gate driver to the ceramic substrate, from the ceramic substrate to a layer of gel, and from the gel to the DBC layer.

## 3.9. Conclusion

For the reduced order electromagnetic modeling, software tools based on the PEEC method such as InCa and Maxwell Q3D have been evaluated. Maxwell Q3D has been used to model and optimize the layout of a power electronic module for the first time. A systematic modeling procedure using Maxwell Q3D has been developed and described in detail. The assumptions made in the Maxwell Q3D modeling have been identified and verified with experimental measurements.

According to the simulation and measurement results, the inductance values for the wire-bonded IPEMs are considerably larger than those for "embedded power" IPEMs.They are close to the TO-247 packaged devices, which have inductance values in the order of 10 nH. The reason is that both wire-bonded IPEMs and To-247 packaged devices use very thin wires for source interconnection, which result in a rather large inductance. Therefore, the "embedded power" IPEMs will have the smallest voltage stress for the semiconductor device compared to either wire-bonded IPEMs or To-247 packaged devices. For the parasitic capacitance, the values are similar for both wire-bonded IPEMs and "embedded power" IPEMs.

A similar conclusion can be reached for the "Embedded Power" PFC IPEM, which was designed by the similar approach of DC-DC IPEM. PFC IPEM has a smaller parasitic inductance than modules consisting of discrete components which have longer PCB traces. Therefore, PFC IPEM should have less voltage stress on the semiconductor device.

# Chapter 4. Integrated Design Methodology

## 4.1. Concept of Integrated Design Methodology

Due to the nature of electronic power processing, the design of power electronics components, converters and systems has always involved many disciplines: from circuits and solid-state physics to electromagnetics, systems and control, thermodynamics, structural mechanics, material science and reliability. Traditionally, these designs have been done sequentially, progressing from one discipline to another and involving many prototyping iterations. Although the use of CAD tools is widespread, these tools are largely "mono-disciplinary" and, hence, require an inordinate number of labor-intensive and time-consuming iterations. As a result, today's design process in power electronics is still much less advanced than the automation levels now common in many other industries. The resulting long design cycles unduly increase the cost and turn-around time, and, coupled with the lack of standardization, prevent levels of optimization that are now standard in most high-tech industries. The need for integrated analysis and design tools is even more pressing now, when further advancements are limited by the fundamental relationships between electrical, thermal, mechanical and material properties of the components and packaging [4-1], [4-2].

The goal of this chapter is to present an approach to integrating the multidisciplinary design process in power electronics through the integration of existing CAD tools, multidisciplinary modeling, and system optimization. Two major benefits are expected

from the utilization of the proposed integrated design methodology. First, it will significantly speed up the design process and eliminate the errors resulting from repeated manual data entry and information exchange. Second, the integrated design optimization will result in better utilization of materials and components and will possibly allow for the discovery of new methods in electronic power processing. The feasibility of the approach is illustrated by the design of an integrated power electronics module package.

The major disciplines involved in power electronics design are shown in Figure 4.1. It is practically impossible (and ultimately unnecessary) to model, analyze, and design any component or system by using fundamental physical laws of energy fields and matter continuity. Therefore, the design of any specific component, converter, or system would involve some disciplines to a great extent and would need more detailed modeling and accurate analysis, while the importance of other disciplines may be only marginal. This occurs by using different levels of abstraction, i.e., models of varying levels of fidelity, for different types of analysis that are suitable or necessary for different designs.

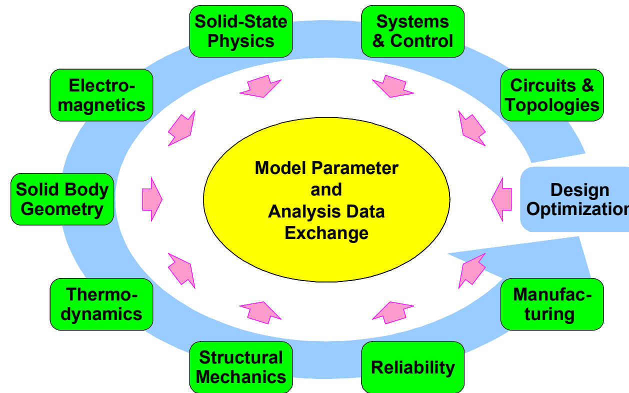



Figure 4.1. Schematic representation of multidisciplinary design process in power electronics

Traditionally, the multidisciplinary aspects in the power electronics design have involved only algebraic modeling [4-3]-[4-6]. Although this approach may be physically justified in many instances, it often leads to significant design deficiencies. For example, the satisfactory functioning of a component or a system under nominal steady-state operation is a necessary condition, but it is not sufficient for reliable functioning during the lifetime of the product in the field. The standard ways of dealing with the problem are different forms of "worst-case" analyses, and component de-rating based on empirical experience is used as "insurance" against "unpredictable" circumstances. This is defensible inasmuch as the circumstances are truly unpredictable (i.e., they result from our lack of knowledge), but if the "unpredictability" results from the known but un-modeled dynamics or multidisciplinary interaction, significantly better designs might be achieved, and would result in better performance, cost and reliability.

The systematic approach to model reduction is at the center of the integrated design methodology concept. Although the progression of the analyses to higher levels of abstraction is different for each discipline, in principle the reduction of modeling fidelity follows the distribution of the physical phenomena that need to be analyzed along the three dimensions of space, time, and function, as shown in Figure 4.2. The models and analysis methods in the space-time (horizontal) plane reflect our understanding of natural phenomena and our ability to predict it, and therefore correspond to different scientific disciplines. The vertical axis reflects our ability to manufacture objects with useful properties and combine them to perform different functions; i.e., it reflects the level of engineering complexity.

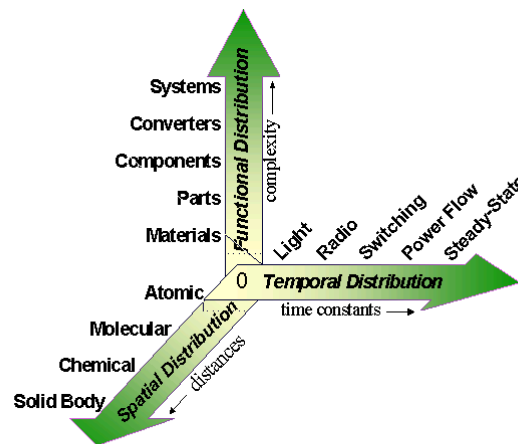



Figure 4.2. Dimensions of increasing levels of abstraction in analysis (decreasing model fidelity).

For the purpose of practical power electronics design, it is rarely necessary to model and analyze the physical phenomena at the basic sciences level, e.g. using quantum

mechanics. The mathematical methods within all physics-based disciplines in Figure 4.1 can be roughly grouped into the following three categories:

1. Partial differential equations for modeling spatially-distributed phenomena

2. Ordinary differential equations for modeling lumped-parameter systems (eliminating spatial dependence of variables)

3. Algebraic equations for modeling steady-state behavior of the systems (eliminating spatial and time dependences of variables)

Within each category, different levels of detail (i.e., model fidelity) can be assumed, and linearization can be used to simplify the description of the system around an operating point. Additionally, as the modeling of an object becomes less detailed, the models of several objects are combined into the models of more complex components and subsystems.

Today's CAD tools offer huge opportunities as well as challenges for the development of integrated design methodology [4-7]. Besides enabling complex analyses at unprecedented speeds, many tools incorporate an enormous amount of knowledge and empirically-verified expertise in their disciplines, which is extremely difficult and rarely possible to assemble in a functional design team. On the other hand, the existing software tools rarely "talk" to each other within the same discipline, not to mention among disciplines. Therefore, software integration is the second major effort directed towards the

implementation of integrated design methodology based on the model reduction approach, in order to provide efficient methods for linking existing software packages.

The proposed approach to improving the multidisciplinary aspects of design focuses on the development of effective methodologies for the following:

1. Integrating the well-known modeling and analysis techniques that already exist in different disciplines, at lower and more detailed levels of abstraction than algebraic modeling,

2. Automation of the model reduction and model-parameter extraction processes within each discipline,

3. Integration of the existing software tools for modeling, analysis, and design in different disciplines, through the automation of the analysis data exchange and the model parameter sharing via common databases,

4. Selection of appropriate levels of model and analysis fidelity in each discipline for different design optimization objectives.

The overall concept of the proposed integrated design methodology is schematically summarized in Figure 4.3. A detailed model of each discipline lies on the outer loop of the design process. Each discipline has a lumped parameter model in the inner loop, which is derived from a detailed model based on approximation. All these models are incorporated into the model database, through which data exchange is possible. It may not be practical to run all detailed simulations in all disciplines. However, by using the lumped parameter

model, it is quite possible to have a simulator that will take several disciplines into consideration. Based on this, design optimization can be achieved.

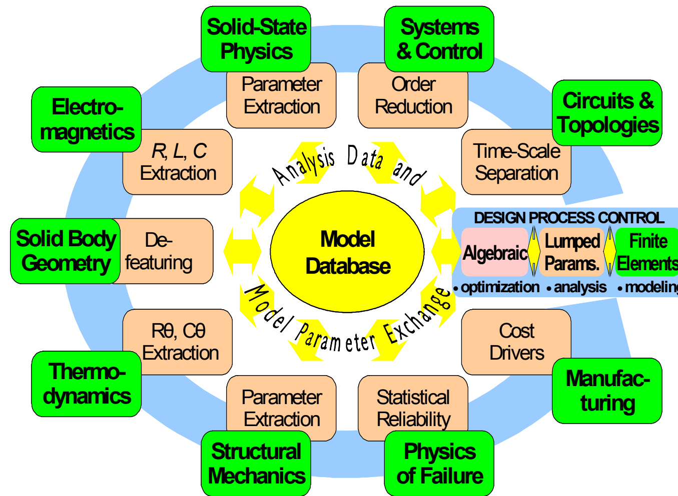


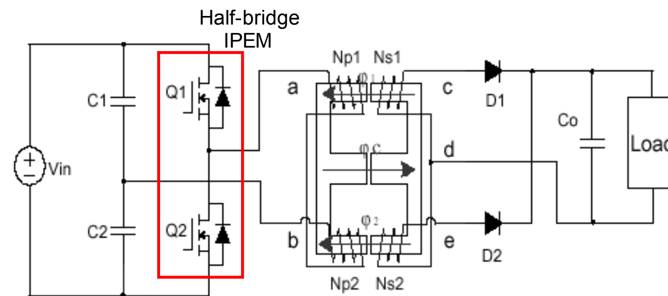

Figure 4.3. Schematic representation of the integrated design methodology.

## 4.2. Example of Multidisciplinary Issues in Integrated Module Design

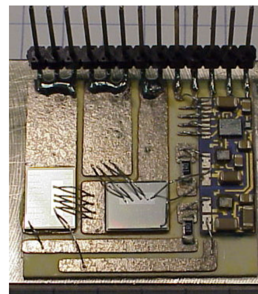
In order to illustrate the issues and procedures described above, let us consider the relatively simple example of designing a half-bridge integrated power electronics module (IPEM) for a DC-DC converter. The application is targeted at a 1 kW power module for computer server and low-end telecommunication systems. The DC-DC converter has 400 V DC input, provides a regulated 48 V bus, and operates in ZVS mode so that the MOSFET body diodes can be used instead of additional anti-parallel diodes [4-8]. It is designed using a modular approach, as shown in Figure 4.4(a).

This module, consisting of two MOSFETs in bare-die form and a hybrid gate driver, can be packaged by conventional wire-bond technology, as shown in Figure 4.4(b). Alternatively, a different packaging method, the "embedded power" method [4-9], can be adopted. As shown in Figure 4.4(c), the two bare chips of the MOSFETs are buried in a ceramic frame, and covered by a dielectric layer with etched holes over the aluminum pads of the chips. The power devices are interconnected to other circuits by metal deposition instead of bonded wire. The procedure for designing such a module, including layout, fabrication, and systems applications, provides an excellent example for the proposed integrated design methodology.

The design goals for such a module would usually include low electrical stress, low conducted electromagnetic interference (EMI), high thermal conductivity, high structural ruggedness, high power density, high reliability, and low cost. The design variables include component and material selection, geometrical layout, and interconnect method. The design constraints fall into two broad groups. The first group includes the usual inequality constraints related to the converter design, such as the maximum peak and average currents and voltages, switching frequency range, ambient temperature range, etc.; as well as the assortment of available components, materials, and packaging technologies, together with their associated physical limitations. The second group of the design constraints consists of the physical relationships that exist between the design goals, design variables, and the first group of constraints. These relationships are captured within the models that are used for the design, e.g. device models, models of the electromagnetic and thermal fields, structural stress models, etc.




(a)



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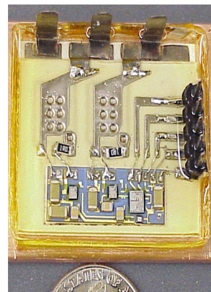


(c)

Figure 4.4. IPEM and IPEM-based converter: a) asymmetrical half-bridge DC-DC converter with integrated magnetics, b) wire-bond module, c) "embedded power" module.

For optimized design, the models must take multidisciplinary interactions into account. For example, the electrical characteristics of semiconductor devices are greatly influenced by the temperature distribution inside the module and the mutual thermal interaction

between multiple heat sources (mainly the semiconductor devices). The thermal behavior mostly depends on the geometry and the material properties of the isolating, conducting, and structural components within the module, which also define the structural (parasitic) impedances that determine the static and dynamic (overshoot) voltage stresses and electromagnetic compatibility. At the same time, the choice of the materials and the geometrical limitations are set by the manufacturing technology as well as initial and life-cycle structural integrity considerations.

The tradeoffs between quality and the difficulty of the design are mostly determined by the accuracy and complexity of the models describing these relationships, and by the features of the software tools used in the design, including their ability to share common data.

## 4.3. Software Integration Framework

There are several major aspects of software integration. The first is the exchange of simulation results between different commercial software packages and between different levels of analysis within the same package. For model reduction within the same discipline, data exchange can largely concentrate on parameter extraction and can be done using input/output file exchange. The second major aspect of software integration is the development of open standards for model (product) data exchange structures for power electronics systems. Such structures should enable centralized and coherent bookkeeping

of the component models and exchange of parameters between different levels and disciplines, which eliminates continuous data re-entry and hard-coded data transfer. The last major aspect is the issue of capturing the knowledge of the problem of space structure and guiding the search in the design space [4-10].

In an ideal situation, one would be able to easily integrate state-of-the-art software tools–in the example from Section III: mechanical CAD modeling, thermal analysis, electrical parameter extraction, and electrical circuit simulation–via freely-connected interfaces, and these would be controlled and executed by an external optimization system. Unfortunately, none of the available software systems yet support such a standardized set of interfaces [4-11].

STEP is an international standard (ISO 10303) for product data representation and exchange [4-12]. Its purpose is to provide a common form for unambiguous representation and exchange of product data among application processes throughout the life cycle of a product. STEP is a recognition of the fact that the representational needs of various domains differ, and it therefore supports a series of application protocols (APs) for different domains. Since almost all simulations share the same solid-body geometry and material information, automatic exchange of these data is essential. For geometry modeling, most mechanical CAD systems have their own native file format. Fortunately, STEP AP203 [4-13] file format (which describes only the information on the mechanical part of the data) is supported by most mechanical CAD systems, such as I-DEAS [4-14]. Some electrical CAD tools, like Maxwell Q3D [4-15], are adding the ability at least to read

the STEP AP203 files. STEP AP210 [4-16] is one of the latest STEP protocols, addressing the needs of electronic assembly, interconnection, and packaging design, but it is not currently supported by any of the major software tools.

For electric circuit description, SPICE netlist is most commonly used. Almost every electrical CAD tool can import and export in this format. However, there are some limitations with SPICE. New models can only be added to SPICE by subcircuit representation. In case where the subcircuit approach is insufficient, SPICE source code has to be modified, which is impossible for most SPICE-based simulators. Another popular circuit (and systems) simulation package, Saber [4-17], provides its native modeling language, MAST, but most library device models are encrypted, and therefore most of the systems descriptions cannot be translated into SPICE netlist.

Therefore, one usually has to resort to a mixture of rigidly connected interfaces, i.e. direct file transfer between the applications using proprietary file formats and custom-built translators. If all the file translators exist and each software tool can be controlled and executed in batch mode, it is possible for an external optimization tool to automate the design process to at least some extent, as will be shown in the example below.

### 4.3.1. Saber

Figure 4.5 shows the circuit schematic with dominant parasitic parameters. In order to control the execution of Saber, a batch file using Saber AIM language is created. Three

example AIM files are included in the Appendix. The first file describes the circuit netlist. The second batch file performs various simulations, including DC analysis, transient analysis, and so on. The third batch file extracts the results from the simulation data so that it can later be read by other software tools.

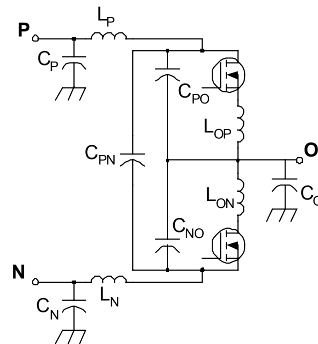



Figure 4.5. Circuit schematic with dominant parasitics

### 4.3.2. Maxwell Q3D

Figure 4.6 shows the Maxwell Q3D model of wire bonded IPEM. The geometry is imported from I-DEAS using STEP file format. A batch file also created for Maxwell Q3D to control its execution, using Ansoft's built-in macro language. An example of the batch file is also included in the appendix.

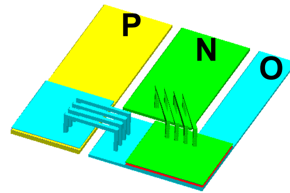



Figure 4.6. Maxwell Q3D model.

### 4.3.3. I-DEAS

I-DEAS was used for both geometry modeling and thermal simulation. Figure 4.7 shows the geometry model in I-DEAS. In order to facilitate the parameter study, Open I-DEAS was used to change the geometry according to design variables [4-18].

The Electronics System Cooling (ESC) function of I-DEAS is used to perform thermal simulation. Figure 4.8 shows one temperature distribution of IPEM.

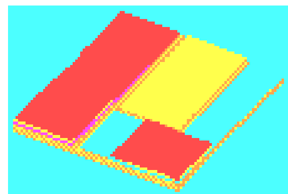


Figure 4.7. Geometry model in I-DEAS.

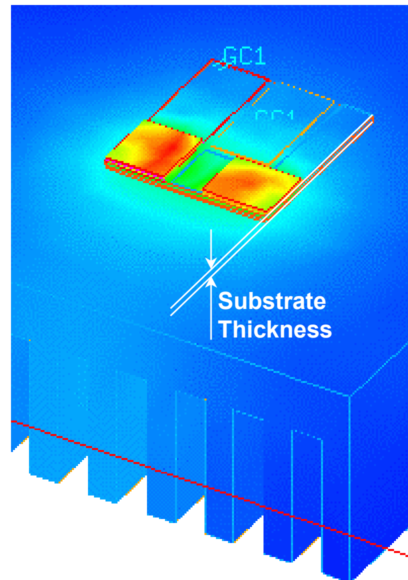



Figure 4.8. Thermal map obtained from I-DEAS ESC.

### 4.3.4. iSIGHT

The flowchart in Figure 4.9 shows an example of integrated analysis used for the parametric study of the tradeoffs between the EMI and thermal performance of the simple IPEM described in Section 4.2 [4-19]. In this example, the software tool iSIGHT [4-20] is used to integrate and manage the data exchange between all of the other software tools. The user inputs the solid-body geometry and material data describing the IPEM layout (Figure 4.4(b)) into a mechanical CAD software program such as I-DEAS (Figure 4.7), which is capable of exporting the geometry in a number of file formats and has an optional open architectural library that facilitates software integration.

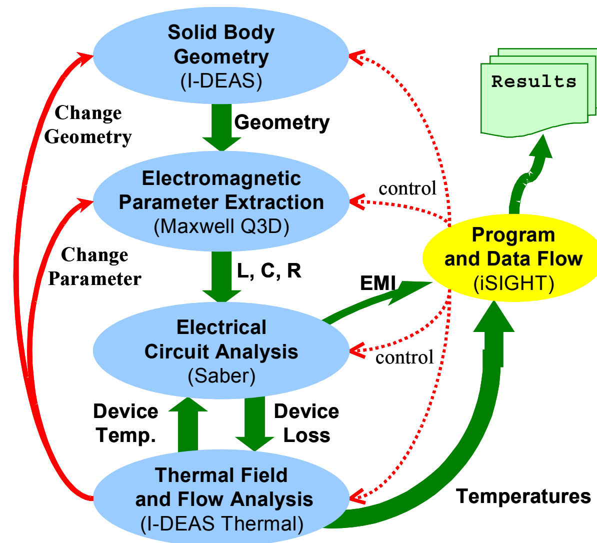



Figure 4.9. Flowchart of integrated electro-thermal parametric analysis example.

The same geometry and material data should be shared by the electromagnetic field and thermal analysis software packages. In this example, Maxwell Q3D is used to extract the electromagnetic lumped parameters, such as self and mutual inductances, capacitances, and AC and DC resistances of the IPEM layout (Figure 4.6). The extracted parameters are transferred as an equivalent circuit (Figure 4.5) into circuit simulation software such as Saber in order to perform transient or EMI and loss analysis. The thermal analysis is performed by I-DEAS' thermal package, Electrical System Cooling (ESC), using the same geometry and material data, and taking the device loss information from the circuit analysis to produce the temperature map within the IPEM, as shown in Figure 4.8.

The interaction between Saber and I-DEAS is managed by iSIGHT until the temperature and device losses converge. This kind of analysis enables the designer to evaluate the tradeoffs between the electrical and thermal performance at the subsystem

level, such as the dependence of the device junction temperature and the peak common-mode EMI current on the thickness of the ceramic substrate, as shown in Figure 4.10. The user can change the relative layout, size, and material of the structural parts, or even select a different heat sink size or fluid flow as necessary to achieve satisfactory results.

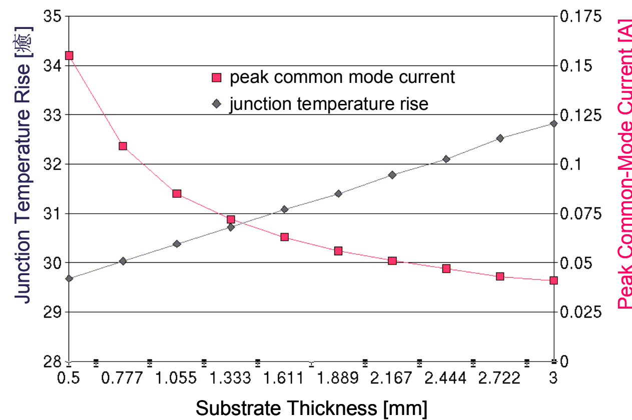



Figure 4.10. Tradeoff between the common-mode EMI current and MOSFET junction temperature.

In this example, Saber, Maxwell Q3D, and I-DEAS are separately controlled by batch files each written in their own macro languages. Then, iSIGHT is used to exchange data between these software tools by manipulating input and output files. Therefore, all the simulations must be done serially, which means that one simulation has to wait until the other stops. It may be more attractive to run several software tools simultaneously, in which case run-time data exchange mechanisms should be explored.

## 4.4. Model Reduction Techniques

The integrated study of even just the electromagnetic phenomena in the above simple example can be prohibitively complex. For example, there are no software tools that could simultaneously solve the Maxwell equations in a general three-dimensional (3D) time-varying case with non-homogeneous and possibly nonlinear materials in the presence of conductive, displacement, and diffusion currents. However, the analysis could be hugely simplified if the interaction of the electromagnetic fields within and outside the semiconductor devices can be considered weak, except for the voltage and current boundary conditions at the device surfaces. In that case, the semiconductor device modeling can be decoupled from the modeling of interconnect and isolation structures outside the devices.

### 4.4.1. Device Model Reduction

Over the last fifty years, there has been extensive research in the area of semiconductor device modeling, and numerous models of varying complexity are available in many software tools that can be used in the design of the manufacture of integrated circuits (ICs) [4-21]. In the power semiconductor device field, modeling the charge storage effect is the most challenging task, since there is generally no closed analytical solution for the nonlinear partial differential diffusion equation. Different approximation methods have been developed in order to construct compact physical models, from the simplest

functional model to more detailed lumped-parameter models and the most accurate numerical solutions for different applications [4-22]. In many cases, the compact device models provided by vendors can be used for the module, converter, and system-level simulation analyses [4-23].

### 4.4.2. EM Model Reduction

In the area of electrical modeling of interconnects and electronic packages, research has been mostly driven by the IC industry [4-24]. Normally these interconnects have a complex geometrical structure, for which the use of 2D simulation is not adequate to capture the critical properties. Full-field simulation of 3D Maxwell equations requires extensive computation, and sometimes shows poor convergence. The partial element equivalent circuits (PEEC) method uses Maxwell integral equations instead of differential equations, and calculates inductances, capacitances, and resistances analytically, based solely on the geometry and material information [4-25]. Such reduced order models are better suited to higher-level system simulations, or for instances when a large number of design iterations are involved [4-26]-[4-28]. Furthermore, different approximations can be used to eliminate circuit elements from the PEEC model, depending on which region of Figure 4.2 will be involved in the simulation, as shown in Figure 4.11. For example, (L, C, R, $\tau$) is the most detailed, full-wave PEEC model, which includes inductance (L), capacitance (C), resistance (R) and retardation ($\tau$). This full-wave PEEC becomes a (L, C, R) model when retardation can be neglected, i.e., when the wavelength of light is

considerably smaller than the dimensions of the modeled object and therefore the delays τ are very small.

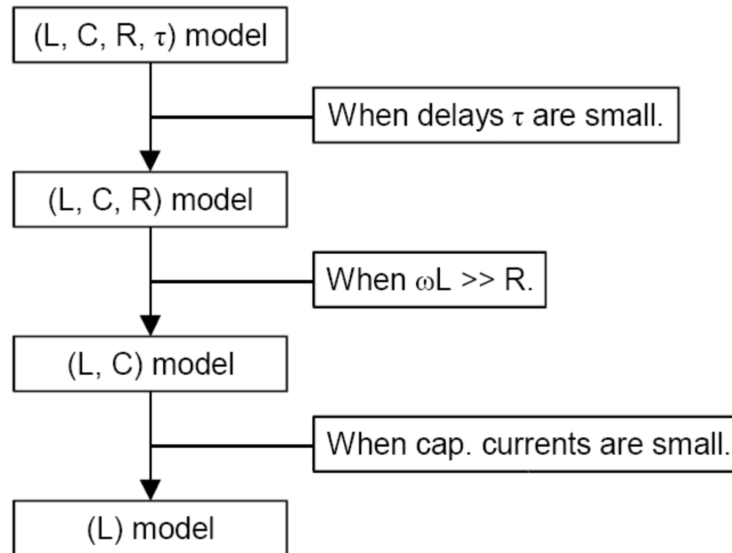



Figure 4.11. PEEC model reduction.

### 4.4.3. Magnetics Model Reduction

Magnetic components are not commercial, but custom-made devices. The physical design and winding structure have a great influence on the performance of the magnetic component. Therefore the model reduction in magnetics design is mostly based on their physical structure and operating frequency.

The reluctances-based model is the least accurate method of modeling. This model makes simplifications about geometry and flux distribution. For example, at low

frequencies, some electromagnetic field effects can be neglected, such as skin and proximity effects. The conductor resistance can be calculated under DC conditions, the leakage inductance can be estimated, and the parasitic capacitance can be neglected. The parameters of this model are not frequency-dependent. However, reluctance-based modeling can still be a good choice for low-frequency applications or speed-critical simulations.

The next most accurate method of modeling is the 1D model. This model is useful for concentric magnetic components (axial symmetry and windings are concentric coils which occupy the whole height of the core coil). In these geometries, the electromagnetic field depends only on radius. The advantage of this second approach is that high-frequency effects are taken into consideration for these simple structures. The limitation of 1D modeling is that it is not suitable for modeling more complex magnetic component geometries, such as planar transformers, in which windings are placed one above the other.

The third approach is the 2D/3D model. This model allows modeling of high-frequency effects as well as more complicated geometries. The modeling is done with the help of FEA tools. FEA tools allow the user to calculate the flux and current density in the magnetic component with fairly high accuracy. The FEA results are then post-processed in order to extract the parasitics of the magnetic component as a function of frequency. Figure 4.12 shows one example of this type of model[4-29]. The main inconvenience of this method it that dealing with FEA tools is not an easy matter. However, there are

commercial CAD tools such as PEmag [4-30], available to simplify this interaction. The full process of post-processing was presented in [4-29], [4-31], and [4-32].

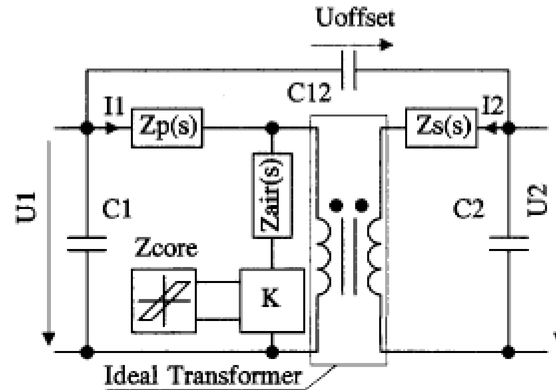



Figure 4.12. Two winding magnetic component model

There is also a method proposed [4-33] to obtain a geometric and frequency-dependent model of integrated magnetics, using 2D instead of 3D FEA solver. The main advantages of this approach are that all the geometrical and frequency effects are taken into account using 2D FEA solvers, while time consumption is much lower than using 3D solvers. A method called “Double 2D” was proposed in the paper. The basic idea is to run two 2D simulations in two different planes to account for the 3D effect, as shown in Figure 4.13.

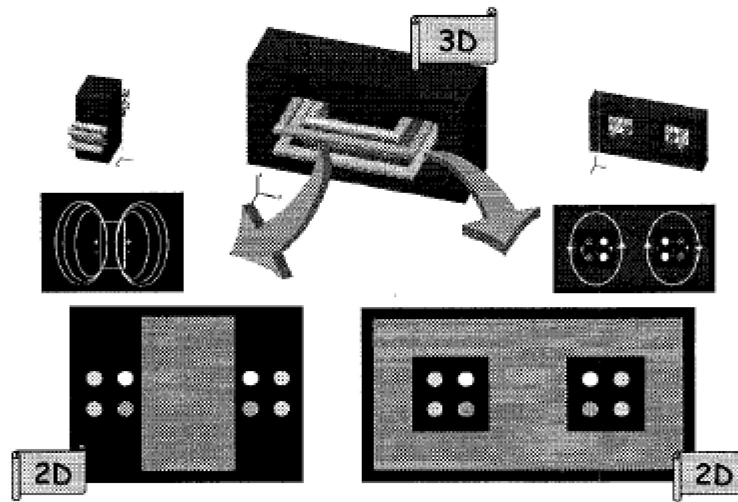



Figure 4.13. Study of 3D EE structure by means of two 2D simulations.

In practice, the losses in magnetic components give rise to significant temperature increases, which can lead to major changes in component behavior. There is a model of magnetic components presented in [4-34] which integrates a nonlinear model of hysteresis, electro-magnetic windings, and thermal behavior into a single model for use in circuit simulation of power electronics systems. It was also demonstrated that the approach for the electrical, magnetic and thermal domains is accurate across a variety of operating conditions, including static thermal conditions and dynamic self-heating.

### 4.4.4. Thermal Model Reduction

Thermal modeling of power electronic systems ranges from detailed semiconductor device / module analysis to overall system evaluation. Different levels of model reduction have also been developed in this area, ranging from thermal RLC equivalent circuit to full-

field Computational Fluid Dynamics (CFD) simulation [4-35]-[4-37]. While methods that allow extraction of thermal-equivalent RLC for simple geometry exist, no systematic approach has been published and no commercial code is currently available to perform systematic thermal parameter extraction. Therefore, it will usually be necessary to use some form of finite element methods for the analysis of the thermal effects.

## 4.5. Summary

An overall design framework with all the necessary types of analysis and their connections has been identified for the first time. An approach to the integration of multidisciplinary analysis and design in power electronics is described. The main goal of this approach is to enable effective analysis of the multidisciplinary interactions at higher levels of accuracy than can be achieved with the simplified algebraic models customarily used today. The major components of the approach are:

1. Integration of the well-known modeling and analysis techniques that already exist in different disciplines, and

2. Development of systematic techniques for model reduction and automated parameter extraction based on the spatial, temporal and functional distribution of physical phenomena.

The core methodology for achieving this goal is the efficient integration of commercially-available software CAD tools that are proven in different disciplines, based on the use and further development of the existing open standards for software integration.

A tradeoff between EMI and thermal performance has been chosen to demonstrate the integrated approach. Software integration involving Saber, Maxwell Q3D, I-DEAS and iSIGHT has been implemented for the first time. The presented rudimentary examples illustrate the feasibility of the proposed approach.

# Chapter 5. Integrated Electrical and Thermal Analysis and Design of IPEM

The objective of this effort was to develop and implement an integrated electro-thermal design strategy for the next generation of IPEM. This section is primarily focused on the electrical aspect of the design and the trade-off between electrical and thermal performance, while details of the thermal aspects are provided in [3-19].

## 5.1. Integrated Design Strategy

A two-step integrated design strategy was employed in the creation of a new IPEM design. First, the parasitic inductance and capacitance of the existing IPEM (identified as Gen-II.A) were analyzed using Maxwell Q3D Extractor, and then a number of new electrically-feasible layout improvements were proposed. The best of these was then selected and named Gen-II.B. The second step involved a detailed parametric study of the Gen-II.B layout to further refine the design, utilizing the integrated design methodology developed in the previous chapter. Several factors were investigated, including the type of material, the thickness of the DBC ceramic substrate, and the thickness of the heat spreader. The final design, Gen-II.C, was then based on the tradeoff between electrical, thermal and practical considerations.

## 5.2. Electrical and Thermal of IPEM

### 5.2.1. Geometry Modeling

The first step of the design methodology began with the development of a geometry model, which included the critical components of the Gen-II.A IPEM design. I-DEAS was selected for geometry modeling because 1) it provides a strong mechanical modeling and analysis environment, 2) it is extensively used in industry, and 3) it is capable of exporting geometry in a number of file formats (e.g., STEP, IGES). Figure 5.1 shows the 3D solid-body model developed in I-DEAS, which has all the geometry and material information for the IPEM. Table 5.1 lists the components used in this module.

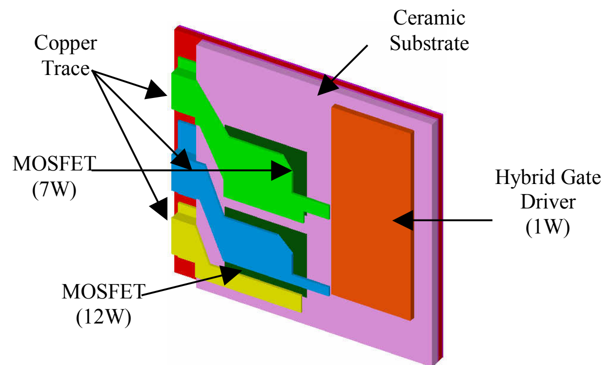



Figure 5.1 Geometry model of Gen-II.A IPEM in I-DEAS.

Table 5.1 Components Used in IPEM Module

| Part | Part Number/ Thickness | Description |
|---|---|---|
| MOSFET | IXFD26N50 | 500V/26A |
| Copper | 12mil | Top layer of DBC |
| $Al_2O_3$ | 25mil | Middle layer of DBC |
| Copper | 12mil | Bottom layer of DBC |
| $Al_2O_3$ | 35mil | Surrouding layer |
| Copper | 10mil | Deposited layer |

### 5.2.2. Electrical Modeling

The geometry model in I-DEAS then can be transported to Maxwell Q3D Extractor for electrical modeling. By translating the geometry directly between the different software packages, we can reduce the time spent on the design cycle and eliminate the possible error resulting from repeated manual data entry. Figure 5.2 shows the Gen-II.A IPEM model in Maxwell Q3D extractor.

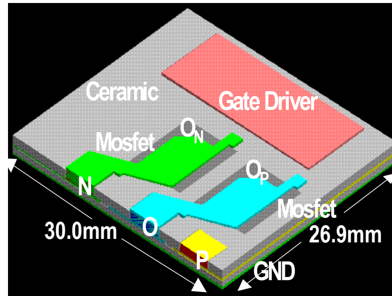



Figure 5.2 Maxwell model of Gen-II.A IPEM.

The equivalent circuit of the Gen-II.A IPEM–together with the passive components, sources and loads–was then entered into Saber. Transient simulations using the circuit shown in Figure 5.3, and an EMI analysis were performed to determine the electrical stress of the device and the common-mode EMI current.

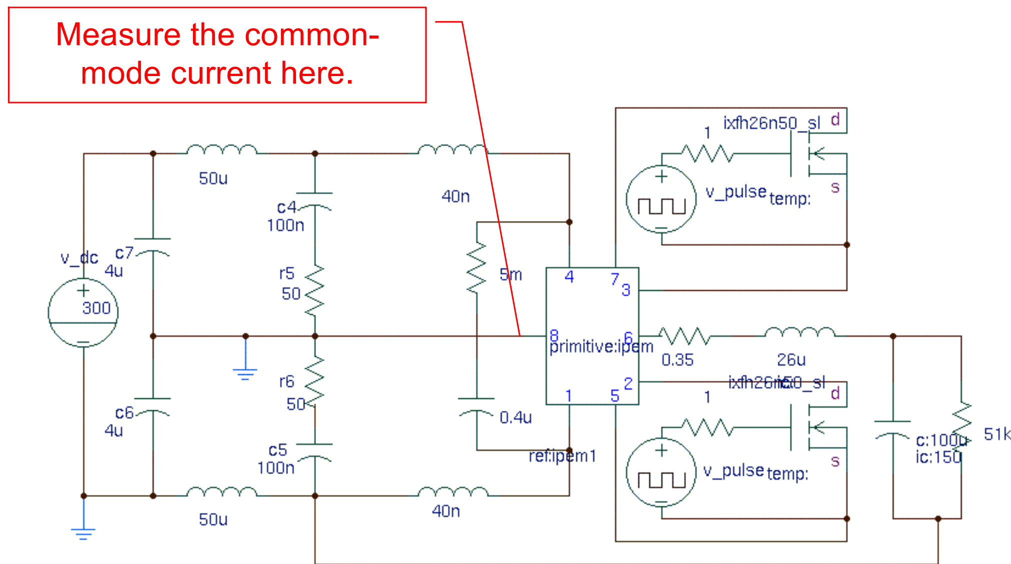



Figure 5.3 Simulation circuit in Saber.

A number of new layouts were then proposed to reduce the geometric footprint of the module and improve electrical performance. These layouts were evaluated in order to determine the best model in terms of the electrical performance, which was named Gen-II.B. To begin the second step of the design strategy, parametric studies were conducted to determine what the effects on electrical performance were of using a smaller copper trace area and varying the DBC ceramic layer thickness.

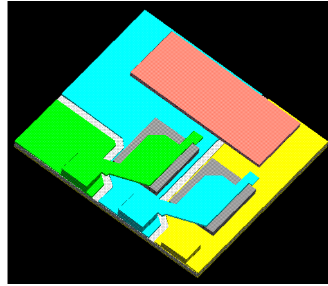
### 5.2.3. Thermal Modeling

The next step of the design strategy continued with a detailed thermal analysis of Gen-II.A and Gen-II.B based on the geometry model developed in the first step. The computational fluid dynamic (CFD) solver in I-DEAS, called Electrical System Cooling (ESC), was used to identify hot spots as well as predict steady-state temperature distributions within the module. A parametric study was performed to determine the effects of the type of material and the thickness of the ceramic substrate, as well as the thickness of the heat spreader on the thermal performance of the IPEM. Details of the thermal analyses are described in [3-19].

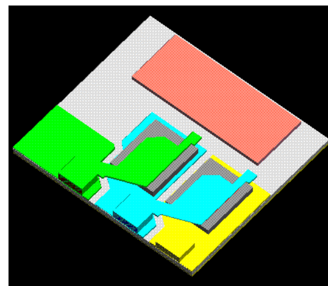
## 5.3. Results of the Electrical Analysis

The parasitic inductance and capacitance results from the Maxwell Q3D Extractor analysis on the Gen-II.A IPEM are discussed in Chapter 3.

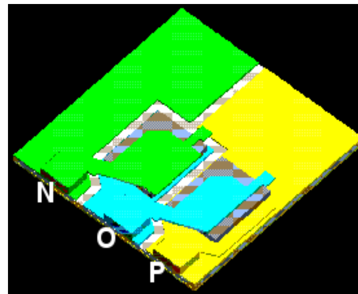
Based on this analysis of the Gen-II.A IPEM, a number of new layouts were proposed to reduce the geometric footprint of the module and improve electrical performance. Many of the proposed layouts involved a redesign of the gate driver. It was decided to not attempt such a redesign in this generation, and, instead to focus the optimization on other aspects of designing the IPEM. In the final analysis, Gen-II.B included a substantial reduction (by a factor of ~3) in the copper trace area and a 4 percent reduction in the geometric footprint, as shown in Figure 5.4.



(a) Gen-II.A



(b) Gen-II.B



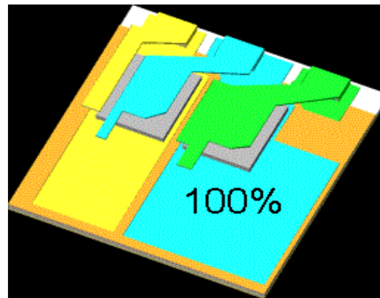

(c) Gen-II.B+

Figure 5.4 Gen-II.A(Initial ), Gen-II.B (with minimal P, N and O trace area) and Gen-II.B+ (with enlarged P and N trace area) IPEM models for Maxwell simulations (surrounding ceramic layer not shown).

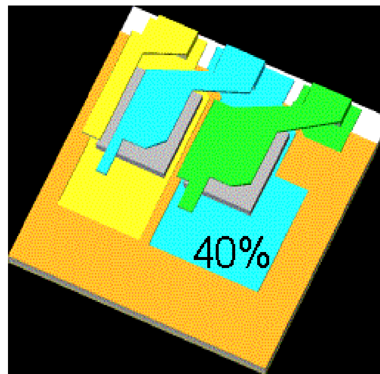
### 5.3.1. Effects of the DBC copper trace area

The effects of the smaller copper trace area were then evaluated in terms of minimizing the common-mode EMI current. Figure 5.5 shows the three typical cases for the copper trace area. The 100% case corresponds to Gen-II A, the 0% case corresponds to Gen-II B, and the 40% case represents the transition between them.

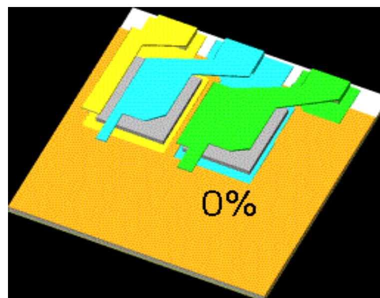
The software integration setup was used to perform the parametric study. Figure 5.6 shows the simulation results. It is very clear that, with a smaller copper trace, the common-mode EMI noise is greatly reduced. The impact on the thermal performance is minimal; less than 1°C in the junction temperature difference. Therefore, this Gen-II.B design is chosen for further study.




(a) Gen-II.A, 100% area case




(b) 40% area case




(b) Gen-II.B, 0% area case

Figure 5.5 Three typical cases for the copper trace area.

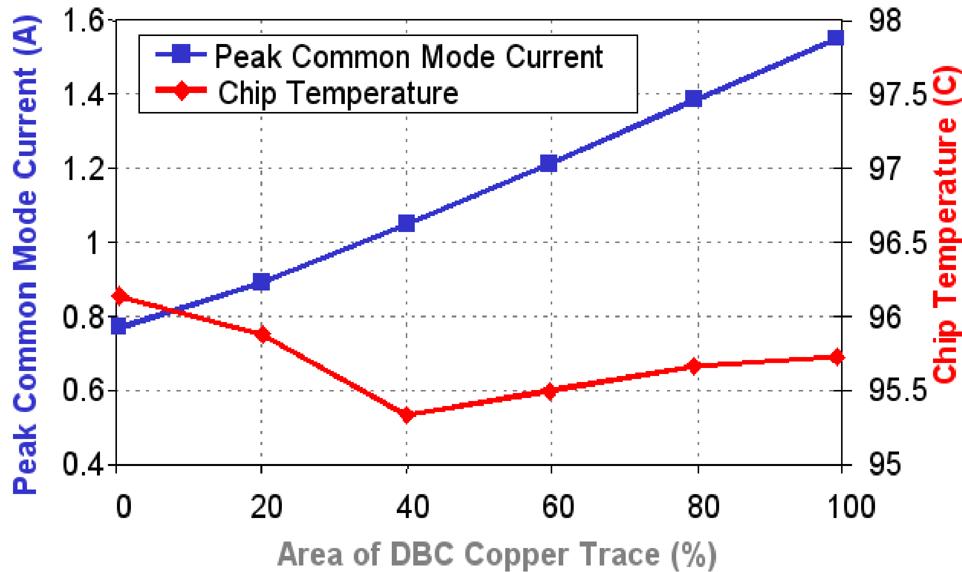



Figure 5.6 Trade-off between electrical and thermal performance for different DBC copper trace areas

### 5.3.2. Effects of DBC ceramic layer thickness

Similar parametric study was performed to evaluate the effects of varying the DBC ceramic layer thickness. The results are shown in Figure 5.7. The O-to-Ground capacitance decreases as the ceramic thickness increases, therefore decreasing the common-mode current and increasing electrical performance. However, the thermal resistance increases as the thickness increases; thus there is a trade-off between electrical and thermal performance. We chose a 25 mil thickness for our final design as it provided the balance needed. The choice of material ($Al_2O_3$ vs. AlN) also had a moderate effect: the use of AlN

decreased the common-mode current by approximately 10 percent, but it was not chosen due to its comparably high cost.

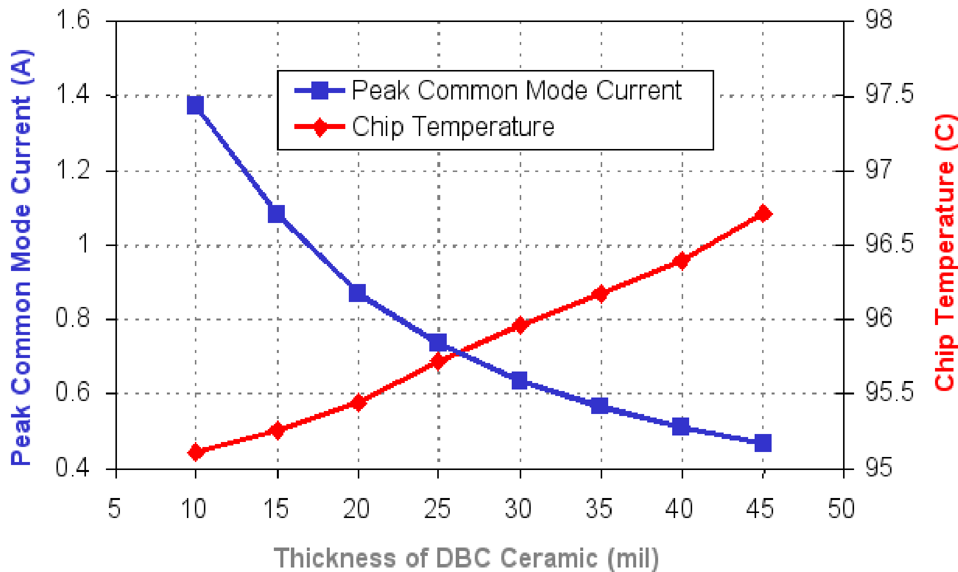



Figure 5.7 Trade-off between electrical and thermal performance for different DBC ceramic thicknesses.

### 5.3.3. Effect of Bus to Ground Capacitance

Our study also showed that larger capacitance from P to GND and from N to GND will actually help to reduce common-mode EMI current. The reason for this is that these capacitances are part of the bus filter cap, which will helps to localize the common EMI current. The Gen-II.B+ IPEM was proposed based on Gen II.B, but with an enlarged P and N trace area. As shown in Figure 5.4, although the Gen-II.B+ IPEM has the same O-to-GND capacitance as the Gen-II.B IPEM, the common-mode EMI current is at least 10%

less. Further study indicated that if we can embed more of these Y-type filter capacitances, we could further improve the common-mode EMI characteristics of our module. The simulation results are shown in Figure 5.8. We propose to investigate the possibility of using higher-permitivity material embedded in the IPEM to provide these Y-type filter capacitances.

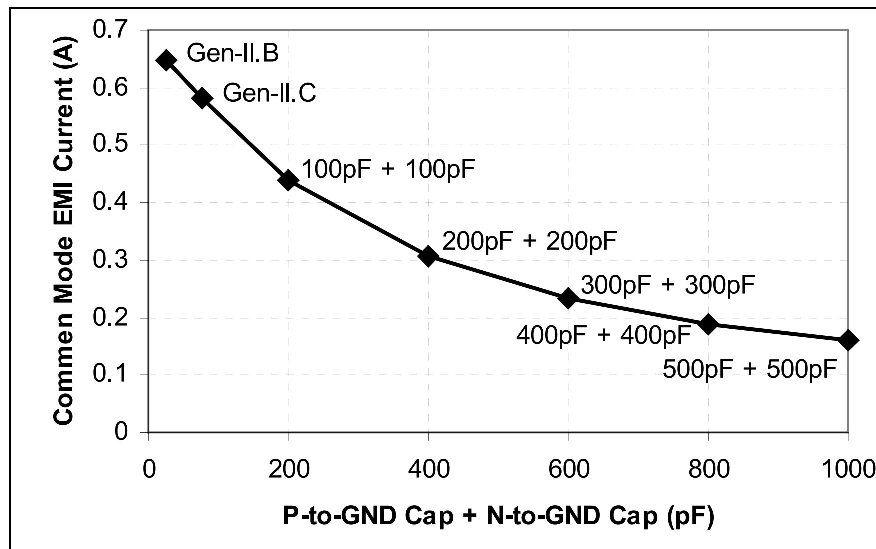



Figure 5.8 Effects of the Sum of P-to-GND and N-to-GND capacitance on common-mode EMI current.

Another interesting problem is the distribution of P to GND capacitance and N to GND capacitance while keeping the sum of the two constant. Figure 5.9 shows the effect of this distribution on the common-mode EMI. It can be seen from Figure 5.9 that the difference is less than 1%. Therefore, this distribution has no major effect on common-mode EMI.

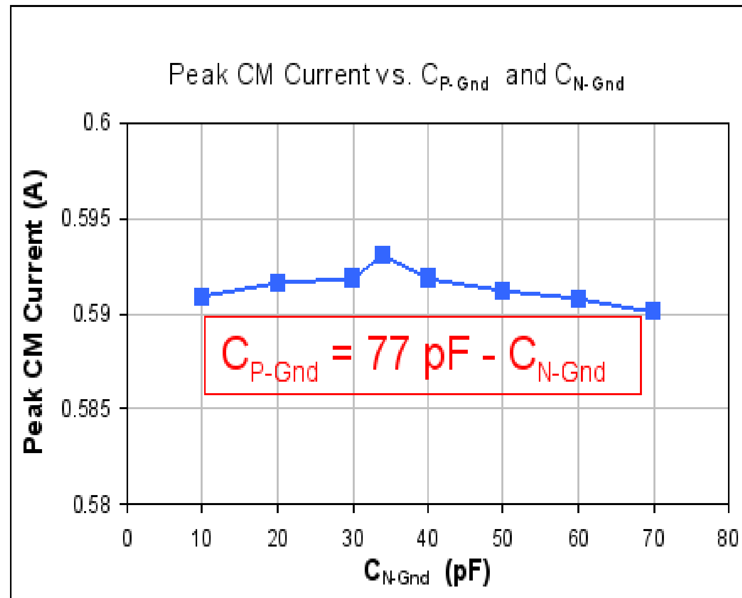



Figure 5.9 Effects of the distribution of P-to-GND and N-to-GND capacitance on common-mode EMI current.

### 5.3.4. Effect of Bus Capacitance

A bus capacitor was also added to reduce the voltage overshoot of the device during the switching period. As shown in Figure 5.10, the decoupling capacitor $C_{bus}$ is added between the interconnect inductance $L_{bus1}/L_{bus2}$ and package inductance $L_1/L_2$. Here "package inductance" refers to the parasitic inductance inside the power module, while "interconnect inductance" refers to the inductance of the interconnect wire from the module to the rest of the power converter. Since package inductances are typically smaller than interconnect inductances, especially in the case of embedded-power technology, the voltage overshoot can be greatly reduced with the help of a bus capacitor.

Table 5.2 and Table 5.3 list the simulated overshoot voltages with or without the bus capacitor with different package inductance and interconnect inductance values. It can be seen that the overshoot will mainly be determined by package inductances $L_1$ and $L_2$, but not interconnect inductances $L_{bus1}$ and $L_{bus2}$. Therefore, the "embedded-power" IPEM is not sensitive to the external interconnect inductance, since the voltage overshoot will be mainly determined by the internal package inductance, which is very small in this case.

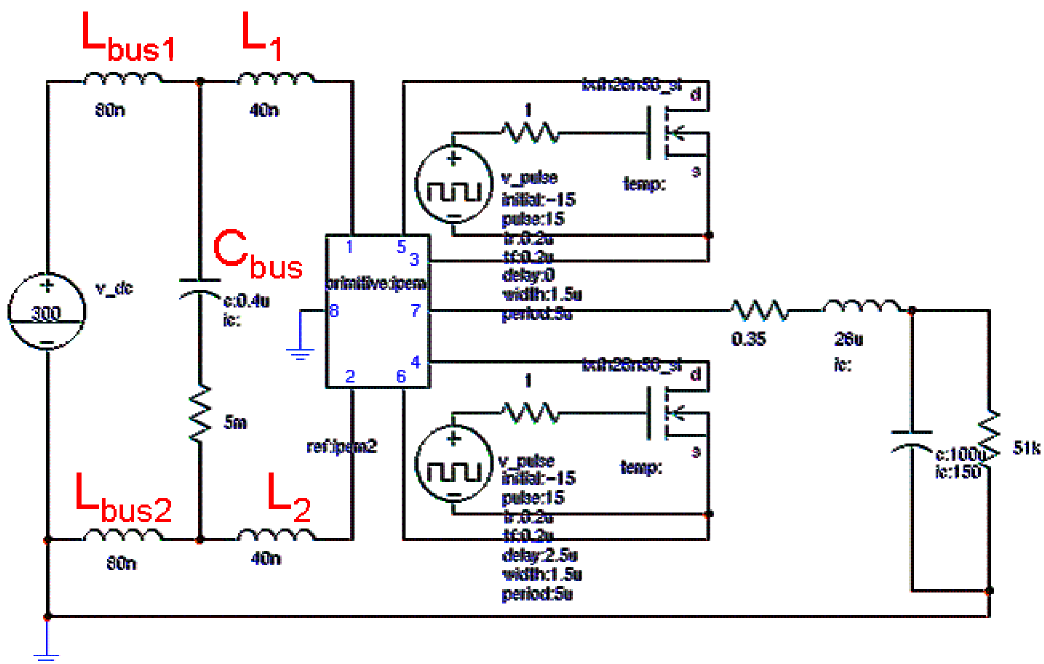



Figure 5.10 Saber simulation illustrating the effect bus capacitor.

Table 5.2 Overshoot voltage without the bus capacitor.

| $L_{total}$ | 2*20 nH | 2*40 nH | 2*80 nH |
|---|---|---|---|
| ΔV | 25 V | 71 V | 189 V |

Table 5.3 Overshoot voltage with bus capacitor.

| ΔV | | $L_1$ & $L_2$ | | |
|---|---|---|---|---|
| | | 2*20 nH | 2*40 nH | 2*80 nH |
| $L_{bus1}$ & $L_{bus2}$ | 2*20 nH | 5.3 V | 20 V | 67 V |
| | 2*40 nH | 8.2 V | 25 V | 72 V |
| | 2*80 nH | 8.8 V | 27 V | 74 V |

## 5.4. Results from the Thermal Analysis

A summary of the results from the thermal analysis is provided here; more details can be found in [3-19]. A thermal analysis was first conducted on the Gen-II.A and the Gen-II.B IPEMs using I-DEAS to determine the overall temperature distribution and the peak temperatures. The Gen-II.B design resulted in a maximum temperature increase of almost 4°C and an overall average increase of almost 3°C over the Gen-II.A design. Hence, although the reduction in the size of the footprint and the copper trace area in Gen-II.B increased electrical performance as noted previously, it decreased thermal performance.

The second phase of the thermal analysis involved a parametric study that identifies the critical factors in improving the thermal performance of Gen-II.B. It was found that using a thinner DBC ceramic layer, replacing $Al_2O_3$ with AlN as DBC ceramic layer material, and adding a heat spreader would result in lower peak temperature.

## 5.5. Design Selection

A two-step integrated design strategy was employed to improve the thermal and electrical performance of an IPEM design. The original design, Gen-II.A, consisted of 1) an IPEM module with a 26.9 mm x 30.0 mm footprint and an almost equivalent copper tracing area, 2) a 25 mil $Al_2O_3$ ceramic substrate layer, and 3) no heat spreader. The final design, named Gen-II.C, consisted of 1) an IPEM module with 4% reduction in the footprint, with minimal O trace area, maximal P/N trace area, and an added bus capacitor, 2) a 25 mil $Al_2O_3$ ceramic substrate layer, and 3) a 3 mm heat spreader.

In terms of electrical concerns, a bus capacitor was added to reduce the voltage overshoot of the semiconductor device. When the common-mode EMI noise for Gen II.A is compared to that of Gen II.C, as shown in Figure 5.11, a 3x reduction can be seen. It was also shown that increasing the DBC ceramic layer thickness from 25 to 40 mil could decrease the common-mode EMI current an additional 30%. However, this was not donebecause of cost considerations.

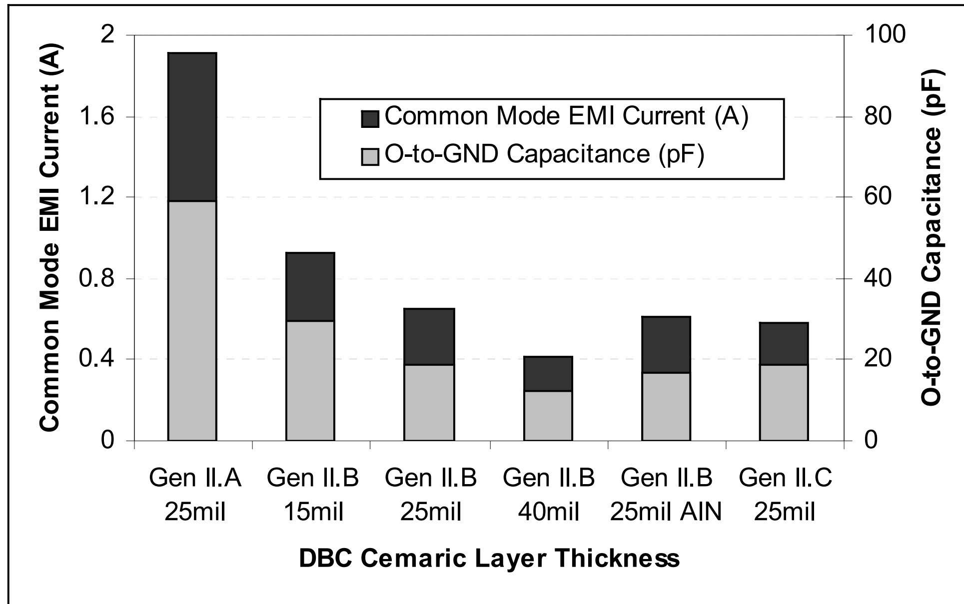



Figure 5.11 Parametric study of common-mode EMI current.

The thermal analysis demonstrated that the choice of material and the thickness of the DBC ceramic layer had only a moderate effect on the thermal performance, while the addition of the copper heat spreader had a significant effect on the thermal performance.

## 5.6. Summary

The DC/DC IPEM layout design is investigated and improved upon by using the integrated design methodology. Several examples of parametric study are presented. The first example shows the tradeoff between electrical and thermal performance for different DBC ceramic thicknesses. The next example looks at the common-mode EMI problem with different DBC copper layouts. It is found that in order to minimize common-mode

EMI noise, the copper trace area of the middle terminal O should be minimized. On the other side, the copper tracer area of the positive and negative buses should be maximized, which leads to the investigation of adding an embedded bus capacitor inside the DC/DC IPEM.

The final design of the DC/DC IPEM, Gen-II.C, provided a 70% reduction in the common mode current and 3°C reduction in the maximum temperature over Gen-II.A, therefore providing an increase in the overall performance.

# Chapter 6. Conclusion and Future Work

## 6.1. Conclusion

A new approach to the integration of the multidisciplinary analysis and design in power electronics is described. Two major benefits are expected from utilization of the proposed integrated design methodology. First, it will significantly speed up the design process and eliminate errors resulting from repeated manual data entry and information exchange. Second, the integrated design optimization will result in better utilization of materials and components and will possibly allow for the discovery of new paradigms in electronic power processing.

The major contributions are summarized as follows.

**Electro-thermal Parametric Study of Copper Trace**

First, in order to understand the basic relationship between electrical and thermal phenomena, the selfheating effect of a simple copper conductor–such as those found in a PCB layout–is modeled analytically, including the AC loss and different thermal boundary conditions. It is shown that for the deposited copper trace in an “embedded-power” IPEM, H = 0 is a reasonable assumption, while for DBC copper trace, a large H value must beassumed. Based on these models, the guidelines for copper trace design are proposed. For example, the minimal thickness of the copper tracer can be determined by using the

derived value and analyzing it at all frequencies. These design rules have been applied to the layout design of the IPEM, as discussed in Chapter 5.

**Electrical and Thermal Model of IPEM**

A complete electrical model is developed for both a DC/DC IPEM and a pfc IPEM. The parasitic inductance and capacitance are calculated by using Maxwell Q3D Extractor. The simulation results are then verified by the impedance measurements. The DC/DC IPEM is compared with discrete-module and traditional wire-bond IPEMs in terms of parasitic parameters. Because of the 3D structure of "embedded-power" IPEM, the inductance loop is much smaller than that of discrete-module or wire-bond IPEMs. Therefore, the parasitic inductance is much smaller, resulting in smaller electrical stress for the semiconductor devices during the switching action. Together with the thermal model, the electrical model lays the foundation for the integrated electrical and thermal analysis and design.

**Integrated Design Methodology**

The software integration framework is presented along with the software tools chosen for this study, including Saber for electrical circuit simulation, Maxwell Q3D Extractor for parameter extraction, and I-DEAS for geometry and thermal modeling. Each of these software tools is controlled via its own macro language files. iSIGHT is then used to

interface with these tools in order to achieve software integration. In order for these software tools to exchange geometry models, a STEP file is use to transfer the 3D solid model from I-DEAS to Maxwell Q3D Extractor.

### Integrated Electrical and Thermal Model and Analysis of IPEM

The DC/DC IPEM layout design is investigated and improved upon by using the integrated design methodology. Several examples of parametric study are presented. The first example shows the trade-off between electrical and thermal performance for different DBC ceramic thicknesses. The next example looks at the common-mode EMI problem with different DBC copper layouts. It is found that in order to minimize the common-mode EMI noise, the copper trace area of the middle terminal O should be minimized. On the other side, the copper tracer area of positive and negative buses should be maximized, which leads to the investigation of adding an embedded bus capacitor inside the DC/DC IPEM.

## 6.2. Future Work

Figure 6.1 shows the overall structure of the proposed integrated multidisciplinary design methodology. As this dissertation only covers a few blocks in the figure, namely “Circuits & Topologies”, “Electromagnetics with R, L, C Extraction”, and “Solid Body Geometry”, it is not only possible but necessary to include more disciplines for study in the

future. One area of interest is the thermal mechanical stress analysis. It uses the same geometry models as those currently used, but requires zooming in to a very fine detail level, and provides interesting tradeoffs.

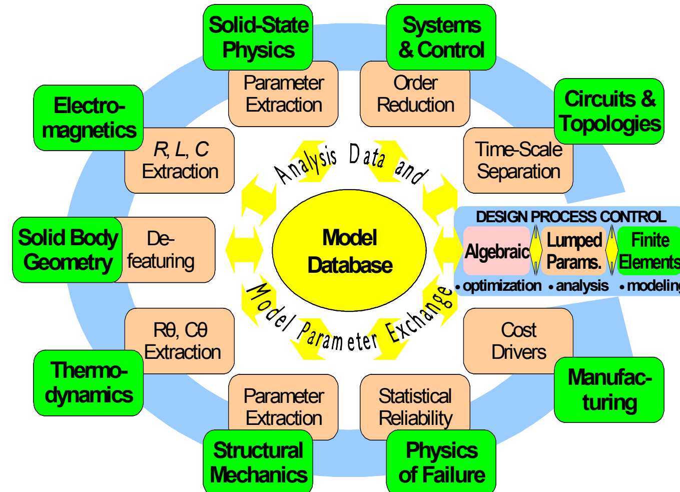



Figure 6.1. Overall structure of the integrated multidisciplinary design methodology.

Currently a model database is implemented by exchanging files using a standard file format. For example, we use STEP file to exchange geometry models between I-DEAS and Maxwell Q3D Extractor, and SPICE netlist to exchange circuit schematics between Maxwell Q3D and Saber. While there are some very preliminary results on the unified-model database based on STEP AP210, more work needs to be done on this area before it can be used in an actual design environment.

Thermal modeling of power electronic systems ranges from detailed semiconductor device / module analysis to overall system evaluation. Different levels of model reduction have also been developed in this area, ranging from thermal RLC-equivalent circuit

simulation to full-field Computational Fluid Dynamics (CFD) simulation. While methods that allow extraction of thermal-equivalent RLC for simple geometry exist, no systematic approach has been published and no commercial code is currently available to perform systematic thermal parameter extraction. Therefore, most of the time it is necessary to use some form of finite element methods for the analysis of thermal effects. However, it is not practical to run numerical optimization routines with each iteration requiring FEA. Therefore, a systematic approach to extract thermal parameters from the geometry, material information, and several runs of FEA simulation data is highly desirable.

Exploring RF models for an IPEM is also crucial to analyzing and predicting its EMI performance in a frequency range of 1MHz through 30MHz. Instead of trying to minimize all parasitic components, it is desirable that we use those parasitics to construct an embedded RF filter within the IPEM.

# Appendix: Case Study of Integrated Electrical and Thermal Analysis Using iSIGHT

## A.1. Case Structure.

```
/ipemtest                : Project home dir
  /macro                 : script files
    /IDEAS               : IDEAS
    /Maxwell       : Maxwell macro file
    /Saber               : Saber AIM file
  /data                  : data files
    /IDEAS               : IDEAS data file
      /stl               : from IDEAS to Maxwell
      /DEFALT_FE-STUDY   : IDEAS thermal analysis data
    /Maxwell       : Maxwell data file
    /Saber               : Saber data file
```

## A.2. Case Steup.

### Step 1: Input the geometry in IDEAS.

When modeling the IPEM module in IDEAS, we need the geometry information, including the heat sink, as well as material parameters. The parameters are used when we perform the thermal analysis using IDEAS ESC (Electrical System Cooling) function.

After the module has been modeled in IDEAS, as shown in Figure A.1, several parts are exported as an stl file, which can be read by Maxwell. Because of the limitations of the Maxwell translator, all of the parts (P, N, O, GND) have to be exported separately, i.e., one part per stl file. The stl files are located at ipemtest/data/IDEAS/stl.

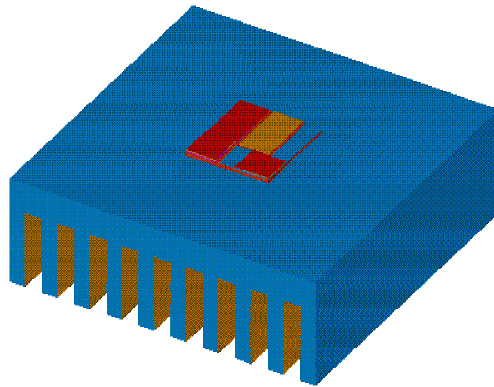


Figure A.1 IDEAS Geometry

**Step 2: From IDEAS to Maxwell Q3D Extractor.**

Maxwell provides a translator, which can read an stl file and save it as an sld file. The translator is called stl2sld. The translated sld files are also located at ipemtest/data/IDEAS/stl.

One problem we have met is that when the geometry is somewhat complicated, the translator may not be able to read the stl file. We have used the heal utility provided by Dr. Bohn to heal the stl file before it is translated.

Another problem is that this translator cannot recognize a given part's position. As a result, all of the parts (P, N, O, GND) are then centered at the origin of the coordination and overlap each other. We then have to move those parts manually.

Another problem with the translator includes the fact that only the geometry is translated, not the material information. In addition, we cannot import a surface, which will be needed when we specify the boundary condition later on in Maxwell Q3D Extractor.

**Step 3: Maxwell Q3D Extractor**

After we have the right geometry file, we simply follow the normal setup procedure in Maxwell Q3D Extractor. This includes:

- Setup material
- Setup conductor
- Setup boundary
- Setup solution
- Solve

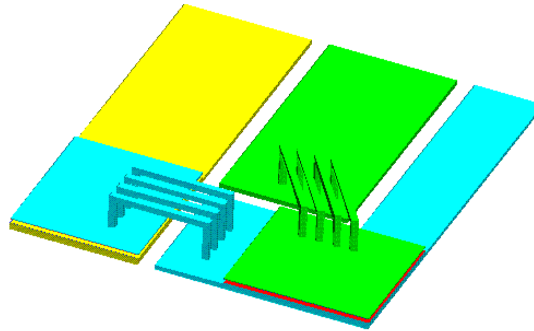


Figure A.2 Maxwell Q3D Extractor Model

The procedure can also be controlled by the macro language provided by Maxwell. An example file can be found at ipemtest/macro/Maxwell. It is also included in the appendix.

**Step 4: Export the RLC circuit to Saber.**

Results of the Maxwell Q3D Extractor are shown as the matrix of R, L, C. Maxwell can export the matrix as a PSPICE file. We used a tool provided by Analogy (Saber), which can translated PSPICE netlist to a Saber sin file. But in this case study, we just use iSIGHT to read the Maxwell result file and generate a Saber sin file, which in this instance is not too much work.

We also need to create a Saber symbol for this sin file if we want to use it in the Saber Sketch. Later when we change the layout, the symbol will stay same since the all the input and output pins will keep same.

### Step 5: Saber simulation

Before we can run the Saber simulation, we still need to create the circuit we want to simulate. We need to put all the source, load, and device models, as well as the layout parasitic model we just created in Step 4, into Saber as shown in Figure A.3. Then we can use an AIM script to control the running of Saber. An example script file is included in this appendix. After the simulation is finished, we can use Saber Scope to extract the result that we are interested in. This can also be done by using the script file, which is attached in this appendix as well.

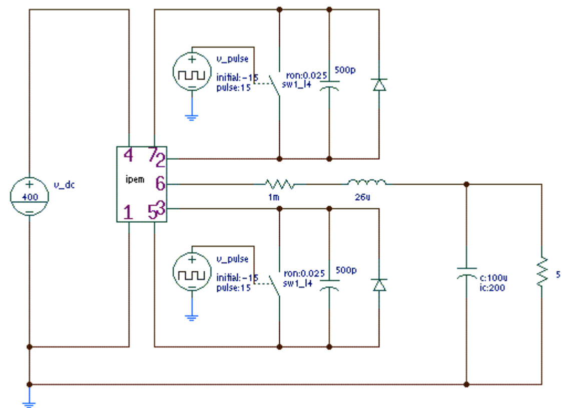



Figure A.3 Saber Schematic

### Step 6: Saber and IDEAS thermal

In the Saber Scope AIM script file, the power loss of these two MOSFETs is written into a file (ipemtest/data/saber/loss.txt). Other information, such as the voltage value, can

also be written into this file. Later we use iSIGHT to read this file and feed the loss into IDEAS thermal analysis.

Similarly, the temperature of the MOSFET is written into another file (ipemtest/data/IDEAS/Temperature.dat) by IDEAS thermal analysis. iSIGHT can then read this file and modify a given field in the Saber sin file, enabling us to take the device temperature into consideration in the Saber simulation.

**Step 7: IDEAS thermal analysis**

IDEAS thermal analysis is also controlled by a macro file, located at ipemtest/macro/IDEAS. There are three files. The first file, ModifyandSolve.prg, changed the thickness of the DBC ceramic layer. It also calls upon the second file, ModifyHeatSink,prg, to change the heat sink size according to a given requirement. Then it performs the finite-element thermal analysis. The temperature distribution, as an example, is shown in Figure A.4. The third file, GetResult.dat, is used to extract the device temperature after the FEA.

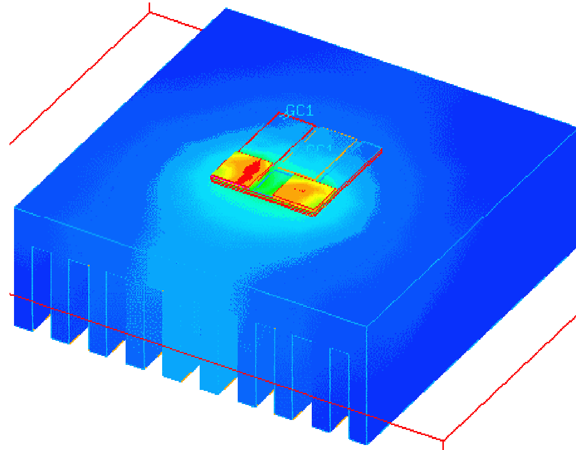


Figure A.4 IDEAS Thermal Model

**iSIGHT Setup**

After we manually go through all the analysis and write the control script file, we can use iSIGHT to automate the process and perform parametric analysis. That means we can change some design variables and let iSIGHT run simulation iterations.

Figure A.5 shows a typical setup in iSIGHT. Task 1 is the translation from IDEAS to Maxwell using the translator stl2sld. This task is only run once, and later when we change the thickness or heat sink size we don't need to go through these translations again.

Task 2 is the main part of the iteration. It begins with the Maxwell Q3D Extractor. One problem here is that we couldn't find a way to quit Maxwell through using a script file. Therefore we have to let iSIGHT kill this process after a certain time period.

Then we read the result file (dcind.lvl and cap.lvl) and generate the Saber sin file (ipem.sin).

Next, we run the Saber simulation; both transient analysis for loss and AC sweep for EMI current. Saber scope can then let us extract the result.

Finally, we use IDEAS ESC function to perform the thermal analysis. After the thermal analysis, we can then modify the Saber sin file (ipemtest.sin) to take the device temperature into account.

This ends one iteration. After this iteration, iSIGHT can modify the ceramic layer thickness or heat sink size to show the tradeoff between electrical and thermal performance.

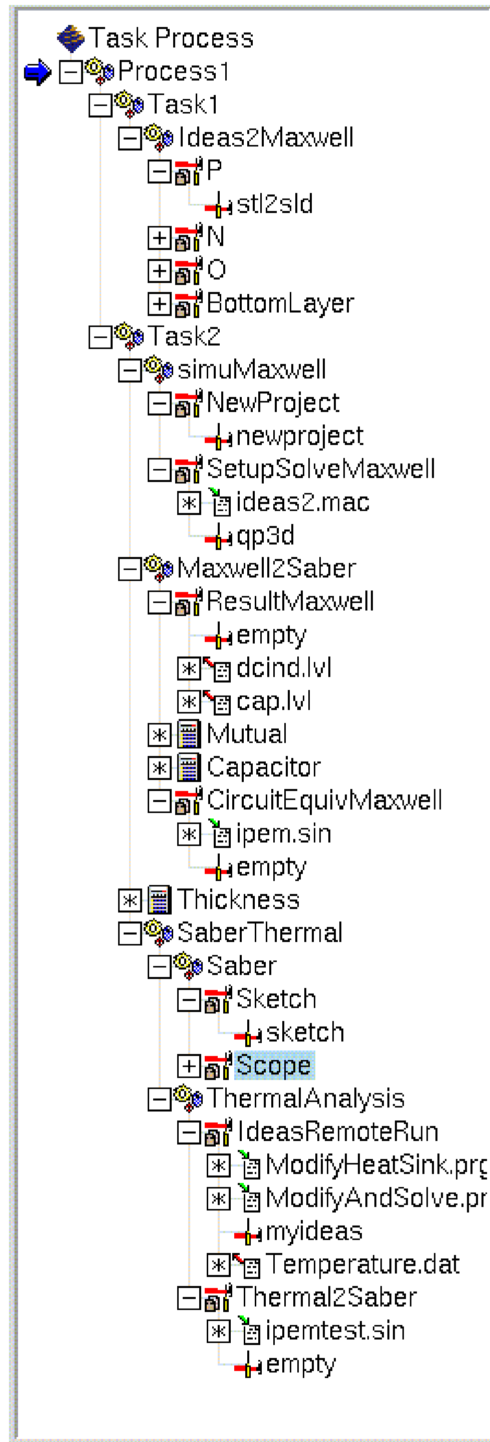



Figure A.5 iSIGHT Process Integration

## Appendix: Maxwell macro file

```
#UseCommandSet "Solution Setup"
#UseCommandSet "Inductance Solution Setup"
#UseCommandSet "qp3d"
#UseCommandSet "MaterialsKernel"
#UseCommandSet "Boundary Kernel"
#UseCommandSet "Default"
#UseCommandSet "mod3proj"
#UseCommandSet "Modeler3"
#UseCommandSet "mod3view"
#UseCommandSet "Generic Module"
#
# setup the requested parameter
#
UpdateRequest 1 1 1 0
#
# setup geometry
#
LaunchModeler
Select { "*" }
SelClear
# P
Read3d "/home/chenzhou/isight/ipemtest/data/IDEAS/stl/P_term.sld"
DetachFaces { "P_term:7" }
DetachFaces { "P_term:5" }
CoverSheets { "P_term" }
ReName "P_term1" "P_term_in"
ReName "P_term2" "P_term_out"
Save3d '*' '?v'
SaveSLD
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/P_term.sld"
# N
Read3d "/home/chenzhou/isight/ipemtest/data/IDEAS/stl/N_term.sld"
DetachFaces { "N_term:26" }
DetachFaces { "N_term:22" }
CoverSheets { "N_term" }
ReName "N_term1" "N_term_in"
ReName "N_term2" "N_term_out"
Save3d '*' '?v'
SaveSLD
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/N_term.sld"
# O
Read3d "/home/chenzhou/isight/ipemtest/data/IDEAS/stl/O_term.sld"
DetachFaces { "O_term:22" }
DetachFaces { "O_term:15" }
DetachFaces { "O_term:13" }
CoverSheets { "O_term" }
ReName "O_term1" "O_term_inP"
```

```
ReName "O_term2" "O_term_inN"
ReName "O_term3" "O_term_out"
Save3d '*' '?v'
SaveSLD
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/O_term.sld"
#BottomLayer
Read3d "/home/chenzhou/isight/ipemtest/data/IDEAS/stl/BottomLayer.sld"
ReName "Aluminum_Plate" "BottomLayer"
Save3d '*' '?v'
SaveSLD
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/BottomLayer.sld
"

# tt
new3d "*"
SetUnits "mm" "y"
Import3d
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/P_term.sld"
Import3d
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/N_term.sld"
Import3d
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/O_term.sld"
Import3d
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/BottomLayer.sld
"
Select { "*" }
Rotate 0 90
Rotate 2 90
DeSelect { "*" }
ReColor "P_term" 255 255 0
ReColor "P_term_in" 255 0 0
ReColor "P_term_out" 0 0 255
ReColor "N_term" 0 255 0
ReColor "N_term_in" 255 0 0
ReColor "N_term_out" 0 0 255
ReColor "O_term" 0 255 255
ReColor "O_term_inP" 255 0 0
ReColor "O_term_inN" 255 0 0
ReColor "O_term_out" 0 0 255
Select { "+O_term" "+O_term_inP" "+O_term_inN" "+O_term_out" }
Move <0, 6.7, 0>
DeSelect { "*" }
Select { "+N_term" "+N_term_in" "+N_term_out"}
Move <0, 11, 0>
DeSelect { "*" }
Select { "+P_term" "+P_term_in" "+P_term_out" }
Move <0, 0, -1.35>
DeSelect { "*" }
#BottomLayer
Select { "+BottomLayer" }
Move <0, 6.75000001, -1.8>
Move <0, 0, -2.445000>
```

```
DeSelect { "*" }
FitRegion 100 "n"
FitAllViews
Save3d
"/home/chenzhou/isight/ipemtest/data/Maxwell/ipemtest.pjt/ipemtest.sm3"
"av"
Exit
#
# setup material
#
LaunchMaterials
materialselect "copper"
materialassign {"P_term" "N_term" "O_term" "BottomLayer"} "OCS" {"0.0"
"0.0" "0.0"} {"0.0" "0.0" "0.0"}
saveMaterialDatabase "warn"
exitModule
#
# setup conductor
#
LaunchConductors
assignnet "P_term" "P_term"
assignnet "N_term" "N_term"
assignnet "O_term" "O_term"
saveModule
exitModule
#AutoDefineNet
#
# setup boundary
#
LaunchBoundaries
clearAllBnds
# P
setBoundary "source"
#PickFaceById "P_term" 1
select "P_term_in"
setBndName "P_in"
assignBoundary
ClearSelection
setBoundary "sink"
#PickFaceById "P_term" 3
select "P_term_out"
setBndName "P_out"
assignBoundary
ClearSelection
# N
setBoundary "source"
#PickFaceById "N_term" 26
select "N_term_in"
setBndName "N_in"
assignBoundary
ClearSelection
setBoundary "sink"
```

```
#PickFaceById "N_term" 30
select "N_term_out"
setBndName "N_out"
assignBoundary
ClearSelection
# O
setBoundary "source"
#PickFaceById "O_term" 75
select "O_term_inP"
setBndName "O_inP"
assignBoundary
ClearSelection
#PickFaceById "O_term" 82
select "O_term_inN"
setBndName "O_inN"
assignBoundary
ClearSelection
setBoundary "sink"
#PickFaceById "O_term" 84
select "O_term_out"
setBndName "O_out"
assignBoundary
ClearSelection
saveBnds
exitModule
#
# setup solution
#
SolnDCSetup
setCurrentSolnPrmsType "solnDCSetup"
SetSolveType 1
SetAdaptiveInfo 10 30 2 2
SetResidual 1E-05
SetMeshType "Initial" 0
SetInductanceSolveType 0
SetInductanceAdaptInfo 10 30 2 2
SaveSetup
SolnPrmsDone "Ok"
#
# solve
#
SolveDCRL
SolveCap
ExitModule 1
```

## Appendix: Saber sin file for the layout parasitic parameter

```
# The following statements are not supported by nspitos

# BEGIN ANSOFT HEADER
# node 1 P_term_P_in
# node 2 N_term_N_in
# node 3 O_term_O_inP
# node 4 O_term_O_inN
# node 5 P_term_Sink
# node 6 N_term_Sink
# node 7 O_term_Sink
# node 8 Ground_Bias
#   Format: PSpice
#    Model: 3D Lumped Model
#     Type: RLC
#  Project: ttnew
#      Cap: /home/cgence/Maxwell/default/macro/ttnew.pjt/cap.pjt/cap.lvl
#      Ind:
/home/cgence/Maxwell/default/macro/ttnew.pjt/dcind.pjt/dcind.lvl
#      Res:
/home/cgence/Maxwell/default/macro/ttnew.pjt/dcind.pjt/dcind.lvl
# END ANSOFT HEADER

template ipem 1 2 3 4 5 6 7 8
{
c.001  5 8 =  8.11916282980699e-13
c.002  6 8 =  6.131280098857e-13
c.003  7 8 =  8.98076656644001e-13
c._001__002  5 6 =  1.998577173383e-13
c._001__003  5 7 =  3.011550914881e-12
c._002__003  6 7 =  3.443624152458e-12
spv.001  1 9 =  dc=0
spv.002  2 10 =  dc=0
spv.003  3 11 =  dc=0
spv.004  4 12 =  dc=0
spv.005  8 17 =  dc=0
spl.001  9 13 =  5.682808228949e-09
spf._001l002  13 9 i(spv.002) =  0.455585583982626
spf._001l003  13 9 i(spv.003) =  -0.251713283718805
spf._001l004  13 9 i(spv.004) =  -0.250343978204964
spl.002  10 14 =  8.979771778799e-09
spf._002l001  14 10 i(spv.001) =  0.288315290123472
spf._002l003  14 10 i(spv.003) =  -0.344815702419569
spf._002l004  14 10 i(spv.004) =  -0.391380490138141
spl.003  11 15 =  1.185930814686e-08
spf._003l001  15 11 i(spv.001) =  -0.12061734987734
spf._003l002  15 11 i(spv.002) =  -0.261091648444419
spf._003l004  15 11 i(spv.004) =  0.67515567444008
```

```
spl.004  12 16 =  7.999421729609e-09
spf._004l001  16 12 i(spv.001) =  -0.177844957735531
spf._004l002  16 12 i(spv.002) =  -0.43934519255391
spf._004l003  16 12 i(spv.003) =  1.00093224997119
r.001  13 5 =  rnom=1.093985207906e-04
r.002  14 6 =  rnom=3.690841597611e-04
r.003  15 7 =  rnom=5.242017982115e-04
spf._003r004  7 15 i(spv.004) =  0.423248334182522
r.004  16 7 =  rnom=2.218685022144e-04
spf._004r003  7 16 i(spv.003) =  0.999995653524992
}
```

# Appendix: Saber Sketch aim file

```
# sketch.aim
# run as: /export/apps14/saber5.1/bin/sketch -script
/home/chenzhou/isight/ipemtest/macro/saber/sketch.aim ipemtest

# load schematic file
#SchMgr:SchDesign tt /home/cgence/isight/ttlisn

# load .sin file
Guide:LoadDesign -design
/home/chenzhou/isight/ipemtest/data/saber/ipemtest.sin

# dc analysis
Saber:Send {dc}

# tr analysis
Saber:Send {tr (monitor 300,tbegin 0u,tend 50u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}
Saber:Send {tr (monitor 300,tbegin 50u,tend 100u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}
Saber:Send {tr (monitor 300,tbegin 100u,tend 150u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}
Saber:Send {tr (monitor 300,tbegin 150u,tend 200u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}
Saber:Send {tr (monitor 300,tbegin 200u,tend 250u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}
Saber:Send {tr (monitor 300,tbegin 250u,tend 300u,trep dc,tripeqtrep
yes,tsmax 2n,tstep 1n}

# plot

Saber:Send {fft (xbegin 280u}

# exit
Saber:Send {exit}
```

# Appendix: Saber Scope AIM file

```
# scope.aim
# run as: /export/apps14/saber5.1/bin/scope -script
/home/chenzhou/isight/ipemtest/macro/saber/scope.aim

# define variable
set t1 253u
set t2 298u
set t3 253u
set t4 298u

# draw waveform
set pf [ScopeSigMgr:loadpffile
/home/chenzhou/isight/ipemtest/data/saber/ipemtest.tr]
set wf_v_top [pf:read $pf v_sw_top]
set wf_v_bottom [pf:read $pf v_sw_bottom]
set wf_v_out6 [pf:read $pf o_out_6]
set wf_i_top [pf:read $pf i_sw_top]
set wf_i_bottom [pf:read $pf i_sw_bottom]
GrXY:NewGraph
Graph addsignal $wf_v_top
Graph addsignal $wf_v_bottom
Graph addsignal $wf_v_out6
Graph sigconfig Signal1 -region 0
Graph sigconfig Signal2 -region 0
set overshoot [Measure:Overshoot $wf_v_out6]

# calculate energy
AimCalc
AimCalc:Enter $wf_v_top
AimCalc:Enter $wf_i_top
AimCalc:DoFunc multiply
AimCalc:DoFunc integ
AimCalc:GraphWaveform
AimCalc:Enter $wf_v_bottom
AimCalc:Enter $wf_i_bottom
AimCalc:DoFunc multiply
AimCalc:DoFunc integ
AimCalc:GraphWaveform
Graph sigconfig Signal4 -region 1
#set wflist [Graph itemselect all add]
#set wf_loss [lindex $wflist 0]
set wf_loss [Graph itemquery Signal3 -waveform]
set e1 [Measure:At $wf_loss $t1]
set e2 [Measure:At $wf_loss $t2]
set loss_top [expr ($e2-$e1)/($t2-$t1)]
#set wf_loss [lindex $wflist 1]
set wf_loss [Graph itemquery Signal3 -waveform]
```

```
set e3 [Measure:At $wf_loss $t3]
set e4 [Measure:At $wf_loss $t4]
set loss_bottom [expr ($e4-$e3)/($t4-$t3)]

# write file
set ofile [open /home/chenzhou/isight/ipemtest/data/saber/loss.txt w]
puts $ofile "begin"
puts $ofile "loss of top switch: $loss_top"
puts $ofile "loss of top switch: $loss_bottom"
puts $ofile "overshoot of output: $overshoot"
puts $ofile "peak of output: 1.3"
puts $ofile "end"
close $ofile

# fft
set pf [ScopeSigMgr:loadpffile
/home/chenzhou/isight/ipemtest/data/saber/ipemtest.fft]
set sp_vr1 [pf:read $pf vr1]
set sp_vr2 [pf:read $pf vr2]
GrXY:NewGraph
Graph sigconfig Signal1  -axis cphasedeg(y)
Graph sigconfig Signal2 -axis db(y)

AimCalc
AimCalc:Enter  $sp_vr1
AimCalc:Enter  $sp_vr2
AimCalc:DoFunc add
AimCalc:Enter 2
AimCalc:DoFunc divide
AimCalc:GraphWaveform
#set sp_vcmc [Graph itemquery Signal1 -waveform]
#Graph sigconfig Signal3 -region 1

exit
```

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