Chapter 5

Future Work and Conclusions

5.1 Improving the Comprehensive Etch Model

The comprehensive etch model presented in this thesis combines the effect of four geometric variables of the masking layer and etch time in order to determine the maximum depth and width of the channel that is etched. Despite the fact that the model form has been found to be accurate for two different deep reactive ion etchers, the model is still not accurate unless certain factors are held to a specific value. The biggest of these that changes between different mask designs is the amount of macro/microloading. As was shown after etching of the cooling chip, the etch rate of the entire wafer and specific features are dependent on the amount of substrate made available for etching. The relationship between the loading and the etch rate needs to be examined and be incorporated into the model. Initial data shows that there may be a linear scaling factor dependent on the percentage of exposed area compared to the mask design used for model development, but more data will have to be collected for this to be verified.

In addition, the etcher parameters influence the results of the model. Even though the form of the model fit accurately to data collected from two separate etchers at two different etch settings, there is not enough proof to determine that the model would apply for all etch parameter

combinations. The applicability of the model form should be examined in different DRIE tools at different settings. If the form of the model is found to apply in all cases, a calibration procedure can be developed to determine the exact model coefficients for each case.

5.2 Future Development of a Microprocessor Cooling Device

The work presented here offers proof that the three-dimensionally independent fabrication process utilizing RIE lag for microchannel fabrication is suitable for the design of microfluidic cooling chips for high-heat-flux thermal management. The channel geometry that was used for this study was not optimized for this task, and better results can be expected if the general geometry was optimized or the microchannels were enhanced with other internal structures to increase heat transfer ability. The first revision that can be made to the design is a reduction in the length of the channels. The meander channels here were three times longer than the length of the heated portion of the chip. The pressure drop over the chip for a given flow rate can be decreased significantly if single pass channels are used instead. This change comes at the expense of having a more variable temperature gradient over the chip. Having a uniform temperature distribution can be important during hot-spot cooling of different heat densities over the chip as uneven thermal expansion can damage the physical structure of the chip. The split-flow arrangement proposed by Kandlikar and Upadhye [72] can also further reduce the pressure drop over the chip for a given rate of heat flux.

In addition, the three-dimensionally independent etching capability of the fabrication process can be used to optimize heat transfer over the chip. Bau demonstrated that just changing the width of the channels over the channel length can decrease the maximum temperature over the chip or it can reduce the temperature variation over the chip, depending on the rate of change of width [62]. Although the aspect ratio cannot be increased past 1:1 using the model in this thesis, the influence of changing both width and depth over the channel length can be examined.

Decreasing the overall cross sectional area of a channel will increase the velocity of the fluid, increasing heat transfer over the channel length. There is likely an optimization scheme that can be used to determine the appropriate change in cross sectional dimensions to achieve a certain goal. These final dimensions can then be realized with the model presented in this thesis.

Despite the aspect ratio limitations of the fabrication process, other methods can be used to increase the heat transfer rate into the fluid. Since isotropic etching is used, the surface roughness of the bottom of the channel can be influenced by the spacing, s, between the openings of the mask pattern. Increasing the surface roughness of a channel will increase the heat transfer rate due to greater boundary sublayer interaction and increased surface area in contact with the cooling fluid. The spacing can also be increased so much that fins are created inside of the channel. If they are placed in a staggered array similar to the design used by Colgan et al. [44], heat transfer can also be improved.

Even without these improvements in heat transfer to the channels, the chip cannot be implemented as a useful microfluidic cooling device unless the chip is part of a closed-loop fluidic system. For the system to be portable and compact, a finite amount of coolant must be used. Thus, after the fluid is heated up, it must be cooled down before it can re-enter the chip to remove more heat. A heat exchanger will need to be implemented into the system for this purpose. Also, a pump will have to be used, rather than a pressurized accumulator, as was used in the open-loop system. A diaphragm pump is an option as it can provide the necessary flow rate at a high pressure, a hard requirement for most small liquid pumps to meet. Enough pressure must be supplied so that the coolant can overcome pressure losses in both the heated chip and the heat exchanger.

Another improvement that will have to be made before the system can become useful is an improved liquid entry and exit system for the chip. Currently, large ports are glued to the substrate for this purpose. Ideally, the distribution system will be integrated into the chip design and the entry ports will be much smaller than they currently are. In the chip's current state, flip-

chip packaging cannot be performed. If the entry system is to be incorporated on the front-side (circuit-side) of the wafer, a system similar to that presented by Dang et al. [35, 43] will have to be used to ensure minimal interference with the chip circuitry.

Lastly, buried channel sealing will have to be performed on the chip to reduce the thermal resistance of the chip and to allow the entire fabrication process to be complementary metal-oxide-semiconductor (CMOS) compatible. A layer of silicon oxynitride can be used for this purpose, sealing the small openings in the masking layer and coating the walls of the channel. One advantage of silicon oxynitride is that the stress in the deposited layer can be tuned [74]. A completely stress-free layer can be deposited to ensure mechanical robustness of the channels. Also, if the pressure from the water deforms the layer to where it may be damaged, an opposing stress can be created in the sealing layer during deposition to offset this potentially harmful deformation. Much work is needed to realistically implement any microfluidic cooling system, but the simplicity and versatility of the fabrication process presented here reduces the risk to the semiconductor device.

5.3 Conclusion

This thesis presents a model relating the depth and width of channels etched isotropically in silicon to geometric dimensions in the photolithographic mask pattern. This is the first such study to relate a mask pattern with five independent geometric variables as well as etch time to the dimensions of the resulting etched feature. The process allows for features to be etched in silicon with different cross sectional dimensions, both depth and width, in a single-mask process by utilizing RIE lag effects. Thus, in order to gain the most geometry variation over a single chip, the influence of RIE lag must be made as high as possible. For this purpose, an Alcatel AMS-100 DRIE system was characterized and etch parameters that increased the presence of RIE lag were determined. These were high pressure, coil power, and SF_6 flow rate. After characterization, the etcher could be used for three-dimensionally independent fabrication. In

order to accurately predict the etched depth and width based on the surface design, a mathematical model was found to relate the two. The equation for depth took the form of a modified Langmuir equation, and the width was found to be equal to the pattern width plus the depth of the channel, indicating isotropic RIE lag effects.

The model presented in this study is advantageous for bounded 3-D microstructure design because it allows for complex and simple structures to be fabricated using a single mask, saving time and money. The mask pattern also allows for easy sealing using wafer-to-wafer bonding or buried channel techniques. The design technique presented in this study is ideally applied to microfluidic networks, where channel junctions and changing channel cross sections, such as in nozzles, are commonly found. In addition, cavities with different sizes can be designed and fabricated on the same wafer as capillary channels measuring only a few micrometers in diameter. The model is an invaluable tool for complex microstructure design with the added benefit of saving resources by the use of a single mask.

This viability of this process for creating a microfluidic cooling device for thermal management of the next generation of microprocessors was also presented. A cooling chip composed of two microfluidic reservoirs connected by meander channels was fabricated on the back-side of a heated chip simulating the heat output of a microprocessor. By running water at 20°C through the chip in an open loop system, the ability to remove more than $100W/cm^2$ heat flux from the chip was demonstrated. Only 750μL/s flow rate was required for this task, consuming just 24mW. Also, comparison of the experimental results to CFD simulation indicated that the behavior of water through the microchannels on the chip can be predicted by conventional equations and simulation, as long as variable fluid properties with changing temperature are accounted for. The demonstration verified that a microprocessor cooling device can be fabricated directly on a microprocessor, while posing less risk to the system than conventional on-chip methods. With further investigation into the optimization of channel

geometry in three dimensions, enhanced heat transfer over other contemporary designs may result and the chip can be incorporated into a closed-loop, compact system.

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