Planar Magnetic Integration and Parasitic Effects for a 3 KW Bi-directional DC/DC Converter

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Abstract

Over the recent years many people have been trying to reduce the size and weight of magnetic components and thus the overall system [19]. One attempt at this is to increase the switching frequency of the system. However, this attempt has its limitations due to increased device switching losses. Device limitations usually confine this frequency to lower value than is desired.

An effective approach, reducing the size and weight is to use the planar magnetics for possible integration with the power circuit and thus eliminating the associated interconnections. Planar magnetics uses the printed circuit board as the windings. This will allow the magnetic component to be implemented into the circuit. The integration of the magnetic components and power circuit will decrease the number of connections, reduce the height, and ensure the parasitic repeatability. Having external connections can cause problems in the system. In this case the system must carry a large amount of current. The connections can cause heating from resistance and inductance of the connection. The planar approach also will decrease the height of the system. This is because the planar magnetic cores have a higher surface area with a decreased height. This can reduce the height of the system by 25 %- 50 % [19]. The parasitic repeatability is also a very important factor. In many cases the typology relies on the parasitic elements for energy storage. Since, the parasitic elements are mainly a result from the geometry of the system; and the planar system has the windings made from the printed circuit board, the parasitic elements will be very consistent through the manufacturing process. For topologies that rely on the parasitic elements for soft switching, the planar design can incorporate parasitic elements with the leakage components for the soft-switching requirement.

This thesis redefines the conventional term of leakage inductance as the sum of a set of lumped parasitic inductances and the transformer leakage inductance for the integrated planar magnetics and inverter power circuitry. For the conventional non-integrated transformer, either planar or non-planar, the leakage inductance is defined between two terminals of the transformer. However, for the integrated planar magnetics, the new lumped parasitic and leakage inductance should include the inverter switch and dc bus interconnections.

The transformer was first designed using a closed-form solution for a known geometry with different copper thickness. The calculated leakage inductance was then verified with finite element analysis and the impedance analyzer measurement. It was found that the theoretical calculation and the finite element analysis results agreed very well, but the measurement was more than one order of magnitude higher. This prompted the study of interconnect parasitics. With geometrical structure and proper termination and lumping, a set of parasitic inductances were defined, and the results were verified with measurements of both impedance analyzer and phase-shifted modulated full-bridge inverter testing.

In addition to parasitic inductance analysis, the flux distribution and associated thermal performance of the planar structure were also studied with finite element analysis. The resulting plots of flux distribution and temperature profile indicate the key locations of mechanical mounting and heat sinking. Overall the thesis covers essential design considerations in electrical, mechanical, and thermal aspects for the planar magnetics integration.

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Chapter 1. Introduction

The effective use of the magnetic components is essential to the successful operation of any switching power supply. It depends on the application to determine what the most important parameter that is to be controlled. In some cases, the most important parameter is the cost. In this case the planar design might not provide as much benefit as the wire wound transformer. In other cases, the parasitic repeatability and low profile is the most important parameter, the planar design is a better choice. In many cases the use of planar magnetics would not be beneficial to the implementation of the product. It was decided for this particular work that the planar design was needed to achieve the parasitic repeatability, weight, size, and thermal management encountered in its working environment.

1.1. Overview of the Converter System

This work investigated a 3 kW bi-directional DC-DC converter to be used in an automotive application. A bi-directional converter implies that the system can operate as both a boost converter and a buck converter, depending on the direction of power flow. Figure 1-1 shows the basic circuit diagram for the bi-directional converter [12] [14].

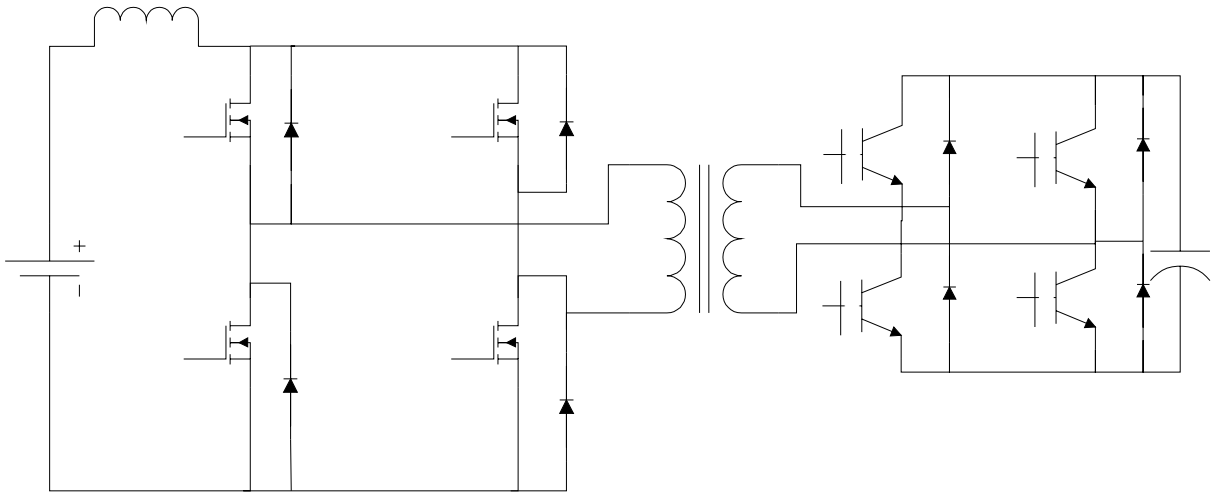


Figure 1-1. Bi-directional DC/DC converter

This typology is very useful as a battery charger to supplement an alternative energy source. A battery is added to an alternative energy systems because currently the alternative energy sources are very expensive. Therefore, they are sized to handle the continuous load, and the battery is sized to handle any transients in the system. This configuration will minimize the overall cost of the system. When the alternative energy source such as solar cells or a fuel cell is operating and the load is low, the battery can be charged. In this case the system will operate as buck converter. The inductor is used as a filter to ensure that the battery only receives a DC voltage and current. Figure 1-2 shows a schematic of the system operating in buck mode. However, when the load is higher than the alternative energy source can supply, then the battery can supply the extra energy required, and the system will operate in boost mode. This mode will transfer energy from the battery to the load.

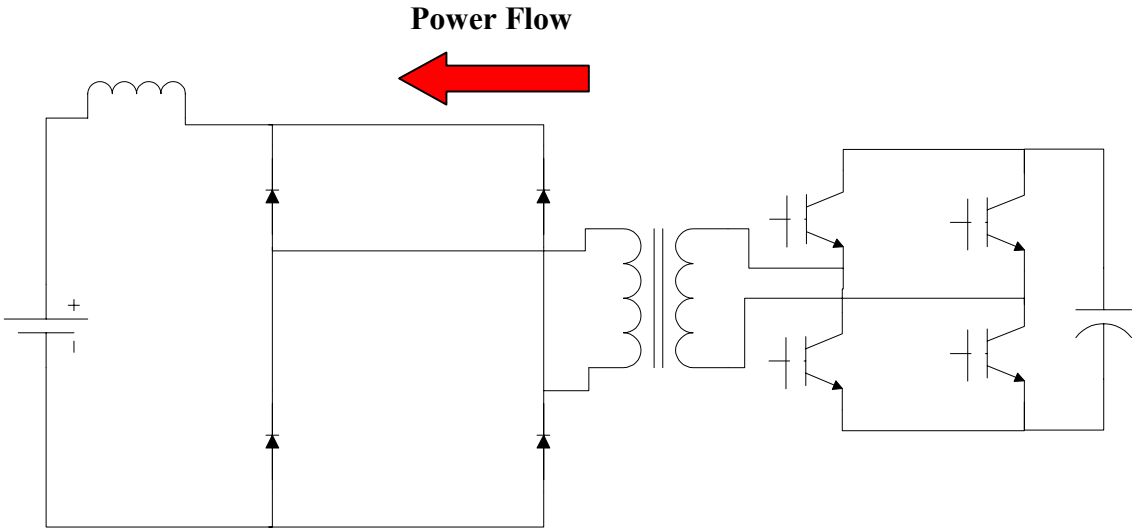


Figure 1-2. Buck Mode Operation

Figure 1-3 shows a schematic of the system operating in boost mode. In boost mode the inductor is used as the boost inductor. It should be noticed that during the startup condition the output capacitor behaves like a short-circuit, and there is a need to use a coupled inductor to operate the converter as a flyback converter, to help build up the capacitor voltage. The flyback converter operation will be disabled after the capacitor voltage is higher than the input voltage multiplied by the turns-ratio of the coupled inductor.

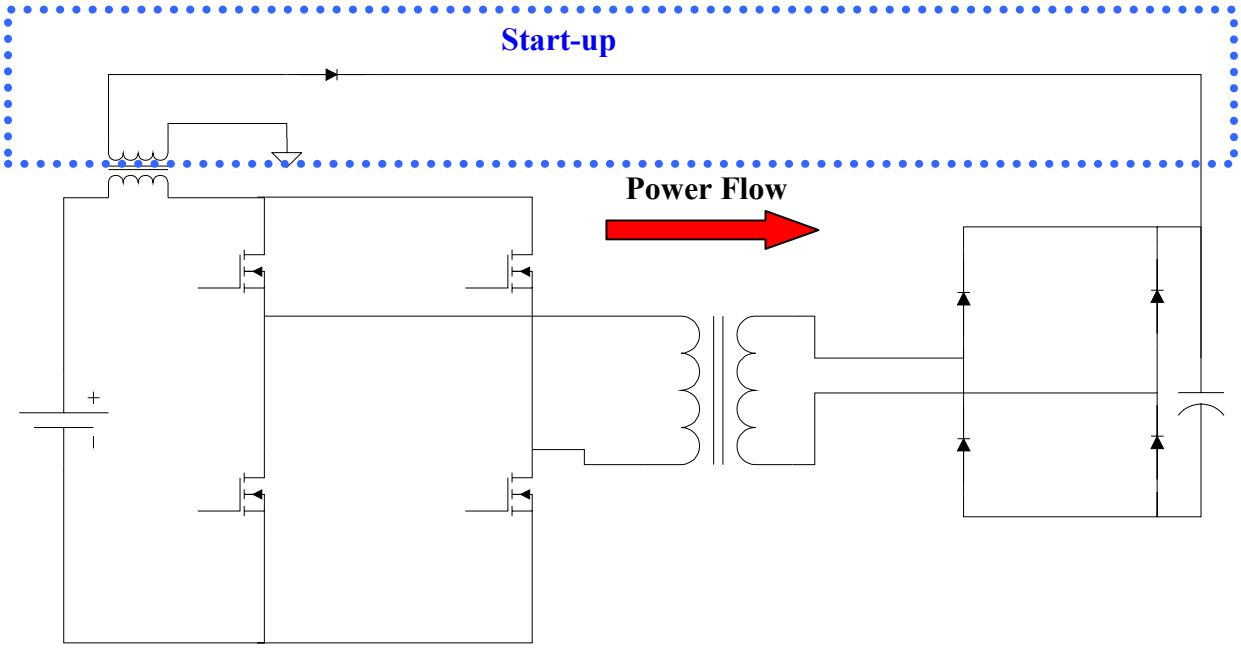


Figure 1-3. Boost Mode Operation

During both modes of operation the battery must be closely monitored. In the buck mode the battery should not be overcharged and during the boost mode the battery cannot sustain the load for an extended period of time.

The scope of the project is to design and integrate, the planar magnetics into the bi-directional converter, and not design a control scheme for battery protection.

1.2. Design Challenges

Since this work was to be implemented in an automotive application, the operating environment is much harsher than many other applications. These conditions can have adverse effects on the magnetic design and reliability. If the environment is not taken into account during the design process then the reliability of the system will be very low.

1.2.1. Temperature

The magnetic components were expected to operate at an ambient temperature of 85°C. This temperature causes many different problems in the design. First, the magnetic properties change with temperature. Figure 1-4 shows the B-H curve for 3C90 ferrite material made by Philips. This figure proves that the saturation flux density will decrease by 90 mT as the temperature changes from 25°C to 100°C. Since the ambient is 85°C, the maximum flux density that can be allowed has to be decreased to avoid saturation of the magnetic component.

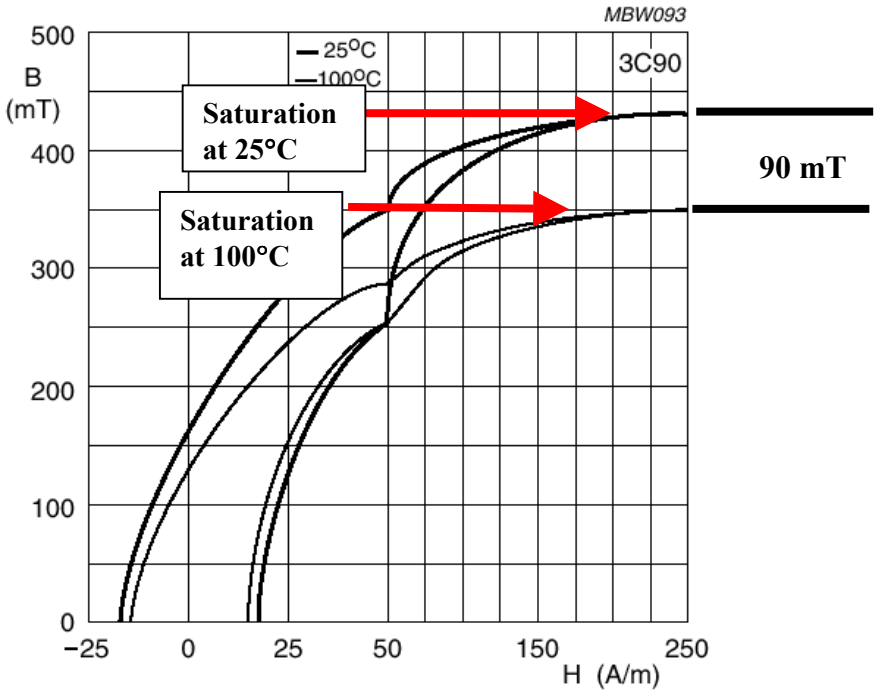


Figure 1-4. B-H curve for 3C90 ferrite

Another change in the ferrite material is the initial permeability of the material. Since the inductance is related to the permeability of the ferrite, the inductance will change as the

temperature changes. This not only affects the inductance of the inductor but also affects the leakage inductance of the transformer. Figure 1-5 shows how the initial permeability can change with temperature.

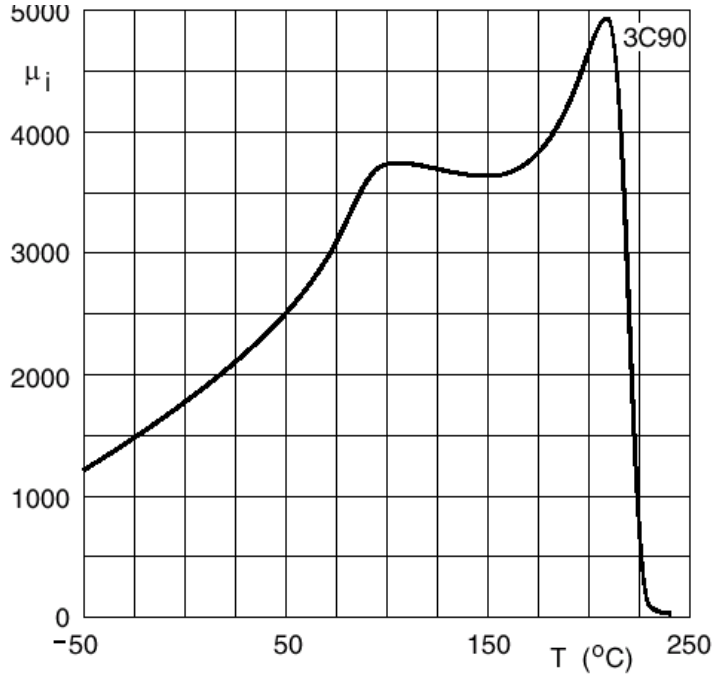


Figure 1-5. Permeability vs. Temperature

Since planar magnetics use the printed circuit board (PCB) as the windings, the breakdown temperature of the insulation material must also be considered. The insulation material is commonly rated by the glass transition temperature. This is the temperature at which the insulation material starts to change its properties. For that reason the system should not reach this temperature. Two different FR4 materials are currently being implemented in PCBs. The first is FR406, which has a glass transition temperature of 170 °C. The second is FR408, which has a glass transition temperature of 180°C. With an ambient temperature of 85°C it will take a temperature rise of 85°C-95°C to reach the glass transition temperature. The thermal expansion is another important factor to be considered to ensure a highly reliable system. FR4 has a very similar thermal expansion coefficient as copper. This implies that over time the printed circuit

board (PCB) will not separate due to the thermal cycles of the system. As the copper expands with heating the FR4 will also expand at nearly the same rate. If a different insulation material is used then the thermal expansion must be considered for long term reliability.

1.2.2. Vibration

The automotive environment is one with excessive vibration. The vibration must be considered in the mounting scheme, so the ferrite material does not crack. If the ferrite material cracks, then the inductance will be much different from what was designed. For the mounting to be successful the magnetic cores have to be securely fastened together and mounted to a heat sink. Also, the PCB should not be allowed to move freely inside the core. This presents a challenge for the inductor that must have a gap to achieve the required inductance.

1.2.3. Operating Conditions

The operation of the system will have large transients that could saturate the magnetic components. When the automobile is accelerating, the system will be required to supply a large amount of power to the load. During the coasting time the system will be able to return to a more manageable level. For this reason the worst case condition has to be found and then designed, to ensure the magnetic components will not saturate and cause the system to fail. Table 1-1 shows the predicted operational patterns of the system.

Table 1-1. System Operation

	Power Flow	**Vin**	**Vout**	**Max LV Current**	**Load Pattern**
Buck Mode	HV→LV	7- 16 V	200 – 450 V	150 A pk	Continuous
Boost Mode	LV→HV	7- 15 V	240– 450 V	350 A pk	5 s on → 5 s off

Chapter 2. Planar Transformer Design

2.1. Introduction

The planar transformer design resembles the standard transformer design in many aspects. The volt-seconds applied must not saturate the ferromagnetic material, during the worst-case condition. However, the copper design is slightly different, and the window utilization is also different. Since the copper used in the design is the PCB windings instead of copper wire, the insulation will be much thicker; therefore, the cooling requirement will be different. Another difference is the window utilization, which is the amount of area the copper fills the magnetic core. In a standard core this number must be much less than one to allow for manufacturing. In a planar design, the manufacturing process is easily repeated and the window utilization can be further extended if necessary.

Table 2-1 highlights the design specifications for the planar transformer. The planar transformer offers many benefits over the traditional transformer in size, weight, thermal management, and manufacturing. In order for the planar transformer, to exceed the traditional transformer, the number of copper layers the PCB uses must be minimized. To do this the primary number of turns is kept to one, therefore the secondary number of turns is fourteen. This deviates slightly from the traditional transformer design, which decides the number of turns after the core has been picked. A typical transformer design is to find an area product that uses the volt-second limit to ensure that the core does not saturate and the amount of window area needed to fit the copper wire. In the planar transformer this method does not give an optimal design. The main reason is that window area for the copper windings will be different in a planar transformer than a traditional transformer.

Table 2-1. Transformer design specifications

Turns ratio	1:14
Galvanic isolation	1800 Vac for 1 minute
Core temperature rise	15 °C
Winding temperature rise	20 °C
Heat sink temperature	85 °C
Leakage Inductance	5 μH from high side

Since this transformer operates in both boost and buck mode, the first step is to find the mode that has the highest rms current. This current will be used to design the copper thickness according to the given temperature rises in Table 2-1.

2.2. Boost Mode Operation

In boost mode the duty cycle is given by (1), and the rms current can be expressed as a function of the duty cycle, as shown in (2). [6]

$$D = 1 - N\frac{Vin}{Vout} \qquad (1)$$

The largest duty cycle results when Vin is minimum at 7 V and Vout is maximum at 450 V. Using N = 14 the highest duty cycle in boost mode is D = 0.782. Using (2) the rms current is obtained as 309 A. However, in boost mode the load has a profile with 5 second on and 5 second off. As long as the circuit does not reach the thermal steady state limit, during this time, the load duty cycle can also be taken into account. Given that copper has a high thermal conductivity, it will get hot during the time the load is on. However, the insulating material (FR4) has much lower thermal conductivity [13]. The result of the system is that only a slight change in temperature resulting from the load change. Figure 2-1 shows the thermal cycle of the transformer. As long as the ΔT is not too large, the transformer will not have a thermal breakdown. The limiting factor in the thermal breakdown is the FR4 material that is used as

insulation. FR406 has a glass transition temperature of 170 °C [10]. The glass transition temperature is the temperature that the material will start to change properties. FR408 has a glass transition temperature of 180°C [10]. Both of these materials are available as PCB insulation. The higher glass transition temperature will allow for a higher ΔT but the cost will also be higher. Equation (3) takes the load duty cycle, D_{load}, into account, which leads to the rms current in boost mode to be 219 A. Here D_{load} is assumed to be 0.5.

$$I_{rms} = I_{PK}\sqrt{D} \qquad (2)$$

$$I_{rms} = I_{PK}\sqrt{D_{Boost} * D_{load}} \qquad (3)$$

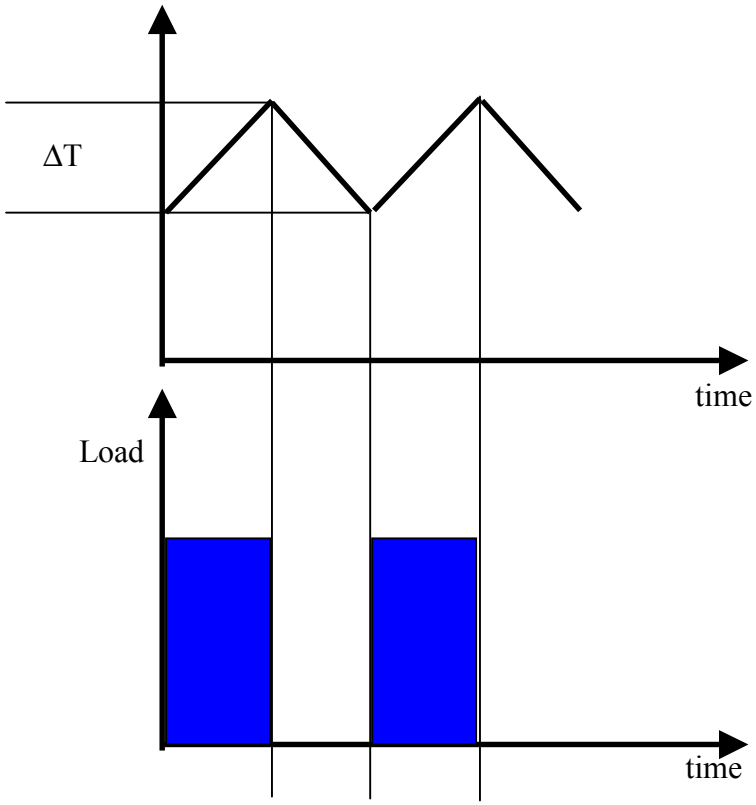


Figure 2-1. Thermal change with load

2.3. Buck Mode Operation:

The same procedure was used to find the worst case current during buck mode operation. The duty cycle for buck mode is given by equation (4) [6]. In buck mode the power is flowing from the high voltage side to the low voltage side. Therefore, Vin used in equation (4) is actually Vout given in Table 1-1. Also, Vout in equation (4) is actually Vin from Table 1-1. The highest duty cycle in buck mode will occur when the input voltage is minimum and the output voltage in maximum. Using the numbers from Table 1-1, the duty cycle will be greater than one. Because the buck mode operation occurs only when the bus voltage is sufficiently high, and the battery voltage is fully charged, it can be assumed that the minimum input voltage is 240 and the maximum output voltage is 15. With a turns-ratio of 14, the maximum buck mode duty cycle will be 0.875. Using equation (2) the worst-case rms current becomes 140 A. This analysis proves that during boost mode operation the current will be highest, and therefore the copper should be designed using the boost mode specifications.

$$D_{buck} = \frac{Vout}{Vin} N \qquad (4)$$

2.4. Skin Effect

Since, the converter is switching at 100 kHz and operating in a high current condition, the skin effect becomes a concern. Skin effect is caused by current that flows in a conductor, creates an eddy current. This eddy current creates flux that opposes the flux from the transformer current. The opposing flux tends to reduce the current density towards the center of the conductor and increases the current density at the outsides of the conductor [6]. If the skin effect is not taken into consideration, then the current density will become too high towards the outer edges of the conductor and results in excess heating and increased resistance [23]. Equation (5) shows the standard skin depth equation. The skin depth is how far the current will penetrate the conductor [6]. Using standard numbers for resistivity (@25°C) and permeability, the skin depth is 0.2 mm at 100 kHz. Since 1 oz/ft^2. of copper is 0.0014 inch thick, 0.2 mm

corresponds to 5.8 oz/ ft^2 of copper. From this analysis the copper weight should be limited to 6 oz/ft^2 if the switching frequency is kept at 100 kHz. If the copper weight is chosen above this, then the current will not utilize all of the copper area and therefore provide no additional benefit. Figure 2-2 shows the thickness of copper at different switching frequencies.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad \text{(m)} \qquad (5)$$

ρ = Resistivity of copper ($1.673 \times 10^{-8}\ \Omega$*m)
μ = Permeability $\mu_o * \mu_r$ ($4\pi \times 10^{-7}$ H/m)

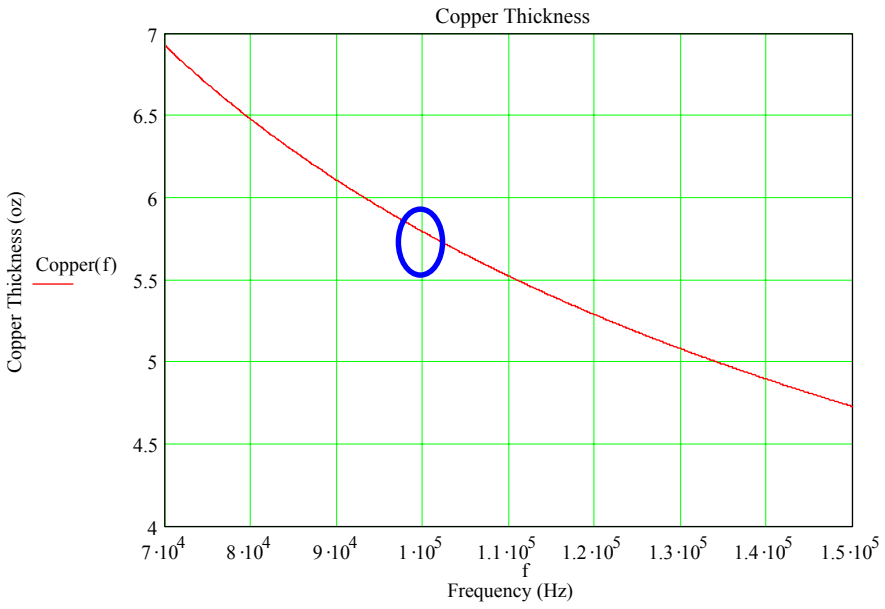


Figure 2-2. Copper weight vs. frequency

2.5. Copper Weight:

The copper weight for the rest of the design is limited to the 6 oz/ft^2 on each layer to utilize as much of the copper as possible. This copper weight limits the core selection and the transformer configuration. The 6 oz/ft^2 copper must have the current carrying capability for 219

A_{rms} (Boost Mode), for the given width. Using the empirical formulas shown in (6) and (7) the copper trace widths can be found [1].

$$CopperArea = \left(\frac{Irms}{k * t^{0.44}} \right)^{0.725} \quad (6)$$

$$TraceWidth = \frac{CopperArea}{CopperThickness} \quad (7)$$

k = 0.24 (internal layer)
k=0.48 (external layer)
t=temperature rise (°C)

An E58 planar core by Philips has a window width of 21.05 mm →0.829 in→ 829 mils. To allow for tolerances given by the PCB manufacturer, core manufacturer, and for the core to easily fit in the PCB, a window width of 725 mils was used for calculations. The primary is only one turn and the trace width is limited to a maximum of 725 mils. This width is still not wide enough to handle the required current. For this reason two transformer cores were used with the primary winding in parallel. This configuration will assume the current splits evenly between the two transformer cores. The current should splits evenly because using the PCB, very good symmetry can be achieved between the two transformer cores. Using equations (6) and (7), with the rms current of 219/2 = 109.5 A, the copper weight is found to be 18 oz/ ft^2. Because of PCB manufacturing limitations and skin depth requirements, the design splits the 18 oz/ft^2 in three layers of 6 oz/ft^2 [23]. All the three layers are connected together in a parallel configuration. Since the PCB integrates the transformer and the inverter, no vias were used to make this copper connection. Instead the through-hole pads from the MOSFETs were used. Using the MOSFET pads instead of vias will reduce the cost. Separating the layers will cause minor problems during maximum load operation. The problem that can arise during operation is that the current will not share equally among all three layers. This is due to the proximity and skin effect. The proximity effect will insure that the current does not distribute evenly. It has been found in [23] that using three parallel layers is better than having one thick layer. The reason is that the current density will be higher, closer to the high magnetic field region. The high magnetic field region is between the primary and secondary layers. This implies that the temperature of the inner layers will be hotter than the outer layers. However, 100 kHz is still a

relatively low frequency and the current distribution should not be a major concern. Using three separate layers is still more effective than using one layer of 18 oz copper.

The temperature rise used for this calculation was 30 °C and the required winding temperature rise given in Table 2-1 was 20 °C. The reason for this difference is that the formulas given in (6) and (7) are for circuit boards that are not attached to a heatsink. In this project, the PCB will be additionally cooled through the ferrite core to the heatsink. This additional cooling is accounted for in the 10 °C temperature rise that was used.

The secondary trace widths were found in a similar fashion. Since the secondary had 14 turns the space between the traces had to also be taken into account. Also, with the secondary, an even number of layers had to be used. This is because the windings would start from the outer portion of the core and wind towards the center. Once it has been wound to the center it must go down one layer and wind back towards the outer portion of the core to connect with other components in the circuit board. The secondary current is 14 times lower than the primary current (15.6 A). Using this lower current, the trace thickness is much easier to achieve on the secondary than the primary. For this reason the secondary windings are wound in series, unlike the primary windings, which are wound in parallel. Figure 2-3 further illustrates this point.

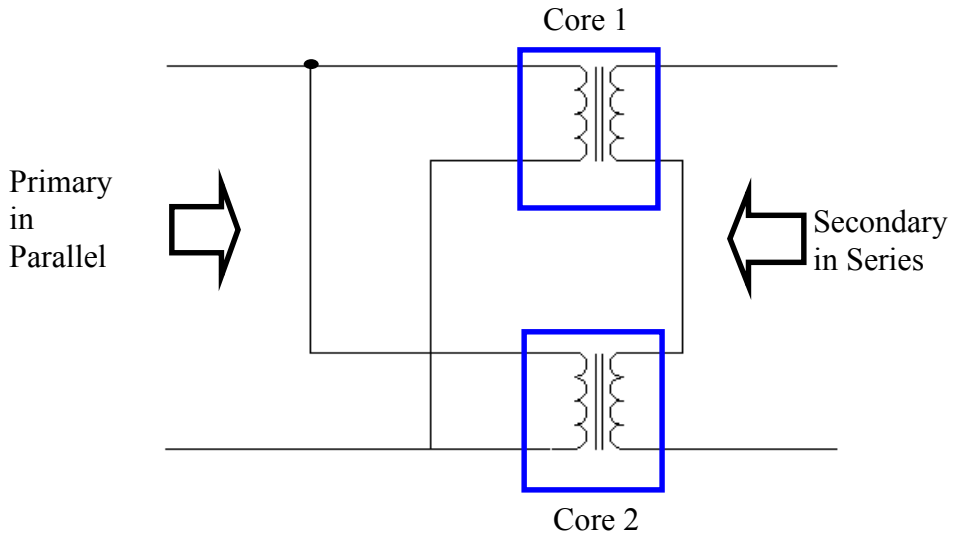


Figure 2-3. Schematic representation of transformer

According to the StrataFLEX heavy weight copper design manual the minimum spacing / trace width is 3 mils for each ounce of copper [25]. For 6 oz. copper the minimum spacing /

trace width is 18 mils. Having the secondary in series makes each transformer have 7 turns instead of 14, if two layers are used this makes 3.5 turns per layer. Again using equations (6) and (7) and taking into account the space between traces gives a trace width of 146 mils and 35 mils spacing between the traces. Table 2-2 shows a summary of the transformer calculations. For the transformer to operate, 5 layers of 6 oz copper are needed, three for the primary and two for the secondary.

Table 2-2. Copper weight conclusion

	Temperature Rise	Width	Copper Weight	Layers
Primary	30 °C	725 mils	6 oz/ft^2	3
Secondary	30 °C	146 mils	6 oz/ft^2	2

2.6. Copper Loss:

To approximate the efficiency of the system, the copper losses are taken into account for the transformer section only. Equation (8) shows the basic equation for the DC resistance as a function of the coil geometry. The DC losses are then I^2R_{DC}. The mean length per turn (MLT) is defined as the average length for all the turns on either the primary or the secondary. It was approximated to be 0.13 m for the primary and the secondary. The primary copper cross sectional area for 6 oz copper is $3.9\text{x}10^{-6}$ m^2, this is for each layer of the primary. The secondary copper cross sectional area for 6 oz copper is $7.912\text{x}10^{-7}$ m^2. Equation (8) gives a result for the primary resistance of 0.56 mΩ for each layer, and a secondary resistance of 19 mΩ. This is for 7 turns on the secondary and one turn on the primary. Since the transformer structure uses two transformers the other transformer must also be considered. The primary is in parallel so the resistance will be divided by three for each transformer and then divided by two for two transformers, the secondary is in series and therefore its resistance should be multiplied by two.

$$R_{DC} = \rho \frac{MLT}{CopperArea * N} \qquad (8)$$

ρ = resistivity of copper (Ω*m)
MLT=MeanLengthPerTurn (m)
CopperArea (m^2)
N = number of turns

The primary current in each layer is $\frac{219}{2*3}$ =36.5 A, which yields the copper loss for each layer of the primary to be 0.746 W. Considering three layers for each core, the loss sums to 2.238 W. For both cores, the total primary DC copper loss is 4.47 W. The secondary current is 15.6 A, and the loss for each core is 4.8 W. With two cores, the total DC loss for the secondary is 9.6 W. The AC resistance is more complicated and should be solved by using a finite element approach. An approximate formula is given in (9) [11]. The formula is given in Ω/ inch. To get the resistance we need to multiply by the mean length per turn and the number of turns. The 1.69 is a *fudge factor* that was based on experimental results. It accounts for proximity effect, at higher frequencies. A more accurate result can be obtained from finite element analysis. Using 0.146 mils for the secondary and 6 oz copper, the AC resistance at 100 kHz is 16 mΩ for the secondary for both transformers this is multiplied by two. Using 725 mils and 6 oz copper, the AC resistance of the primary is 0.4 mΩ for each layer the total primary resistance is divided by three for each core and then divided by two for the two transformers. The total resistance is the sum of the AC and DC resistance. Table 2-3 shows a summary of the different resistances and the total calculated resistance.

$$Rac(f) = \frac{\sqrt{\pi * \rho * \mu}\sqrt{f} * 1.69}{2 * (w + d)} \ (\Omega/\text{in}) \qquad (9)$$

w = width of trace (inch)
d= trace height (inch)
μ = $3.192*10^{-8}$ (Weber/amp/in)
ρ = $6.787*10^{-7}$ (Ω/in)

The copper losses are I^2R losses. For the primary the total loss is 7.7 W and the secondary is 17.3 W. This will be the loss at the maximum load condition.

Table 2-3. Calculated winding resistances

	R_{AC} @100 kHz (mΩ)	R_{AC} @100 kHz (mΩ)	R_{DC} (mΩ)	R_{DC} (mΩ)	Total (mΩ)
Primary	0.4 (perlayer)	0.0667 (total)	0.56 (per layer)	0.093	0.16
Secondary	16 (per transformer)	32 (total)	19 (per transformer)	38	70

2.7. Core Loss:

The core loss of the transformer is dependent on the material that the core is made from, the switching frequency, the flux density, and the volume of the core. Core loss can be directly related to the area of the hysteresis loop of the magnetic material [6]. Figure 2-4 shows an example of a hysteresis loop for a magnetic material. As the hysteresis loop becomes more square, the area of the loop decreases, this in return will decrease the core loss. Equation (10) shows a simple expression for the energy loss per cycle [6].

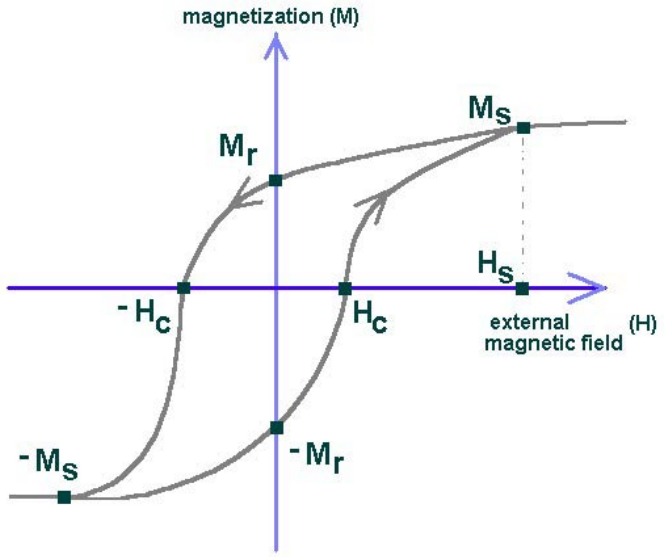


Figure 2-4. Hysteresis loop

Energy lost per cycle=core volume*area of B-H loop (10)

Equation (11) shows the basic formula for the core loss of a transformer. The constants A, α, and β all depend on the type of material that is used. This transformer was designed for Philips 3C90 material. For the EI58 core, the materials that are available are 3C90 and 3F3. 3C90 material does not provide the best core loss over all frequency ranges. This material is to be used for lower frequency applications. Philips recommends using 3C90 for frequencies up to 200 kHz and above 200 kHz 3F3 material should be used. The 3F3 is designed for up to 500 kHz. Both the 3F3 and the 3C90 material have similar core losses at 100 kHz. However, the 3F3 material is more expensive, for this reason the 3C90 was chosen to be the best material for this application. Table 2-4 shows a comparison of the 3F3 and 3C90 material. This table proves that the characteristics are very similar at 100 kHz.

Table 2-4. Material Comparison

Material	B_{sat} (mT) @25°C	B_{sat} (mT) @100°C	H_C (A/m)	P_V (kW/m^3) @100kHz, 100 mT
3C90	450	340	15	< 80
3F3	450	330	15	< 80

$$P_L = A * B^{\alpha} * f^{\beta} * V \qquad (11)$$

A= constant
B = flux density (G)
f= frequency (Hz)
V=volume (m^3)
α,β constants

The core loss graph was obtained from the materials data sheet and then the resultant core loss was multiplied times the volume. The relationship for the core loss is that it will increase with the frequency and volume. However, the maximum flux density will decrease as the frequency is increased, because of Faraday's law ($\Delta B = \frac{V\Delta t}{NA_E}$). Figure 2-5 shows the core loss for the EI58 configuration. This graph does include both transformer cores and the peak flux density is 2500 Gauss. This implies that if the transformer is not operating at maximum volt-seconds then the flux density will be decreased and the core loss will be decreased. The total core loss from the graph is 41.6 W at the maximum operating condition. If both the copper and core losses are considered the efficiency of the transformer should be 98% at full load.

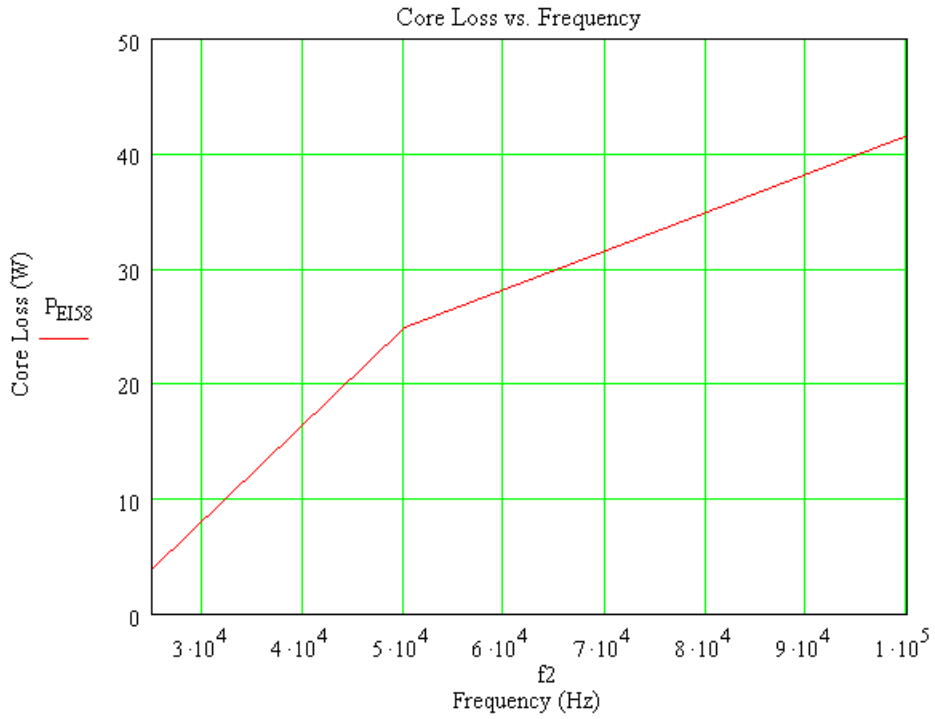


Figure 2-5. Core loss for EI configuration at 2500G

2.8. Flux Density:

The flux density is derived from Faraday's law and shown in (12) [6].

$$\Delta B = \frac{V\Delta t}{NA_E} \text{ (Tesla)} \qquad (12)$$

VΔt=voltseconds
N = number of turns
A_E = cross sectional area (m^2)

Since the transformer core is kept at 85°C the saturation flux density is decreased from the standard 25°C case. For the 3C90 material the saturation flux density is 3500 G at 100°C instead of 4400 G at 25°C. To prevent saturation of the transformer the design limited the maximum flux density to 2500 G (0.25 T).

2.8.1. Boost Mode

Figure 2-6 shows the voltage across the transformer and the current through the inductor during different switching states. The switching frequency was specified to be 100 kHz. This makes the volt-seconds across the transformer to be $\frac{(1-D)V_o}{Nf}$. Since the waveform across the transformer is a square wave, the volt-second is simply the voltage multiplied by the time. The worst case is when the duty cycle is minimum and the therefore the output voltage is minimum. Using equation (12) with the cross sectional area of 310 mm^2, the worst case flux density swing (ΔB) is 0.4646Tesla (4646 Gauss). The flux density swing is not as much of a concern as the maximum flux density. For the square wave operation this is ΔB/2 or 2323 Gauss. This is well below the design limit of 2500 G.

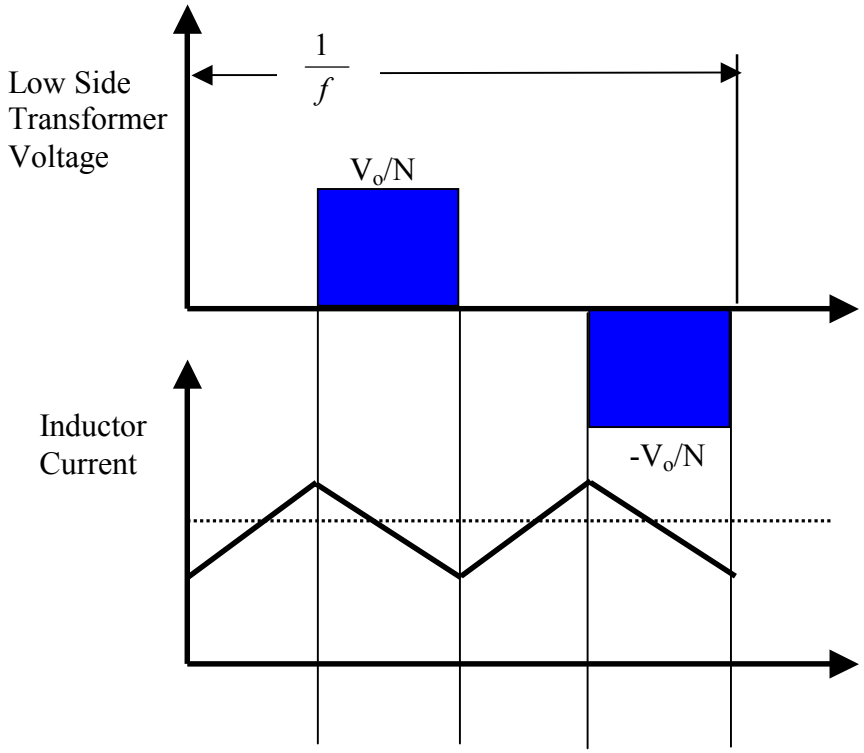


Figure 2-6. Boost mode waveforms

2.8.2. Buck Mode

Figure 2-7 shows the voltage across the transformer and the inductor current for different switching times. During buck mode operation the volt-second is Vin*D/f. For the primary Vin is actually Vout / N from Table 1-1. Given the specifications the worst case is when the output

voltage is 240 V, this results in a duty cycle of 0.875. Under this worst case the maximum flux density is 2117 G, which corresponds to a swing of 4234 G. This flux density is also below the design limit of 2500 G. During the boost mode operation the copper losses will be greater because the current will be much higher than in buck mode operation. Also, boost mode proved to have the highest flux density.

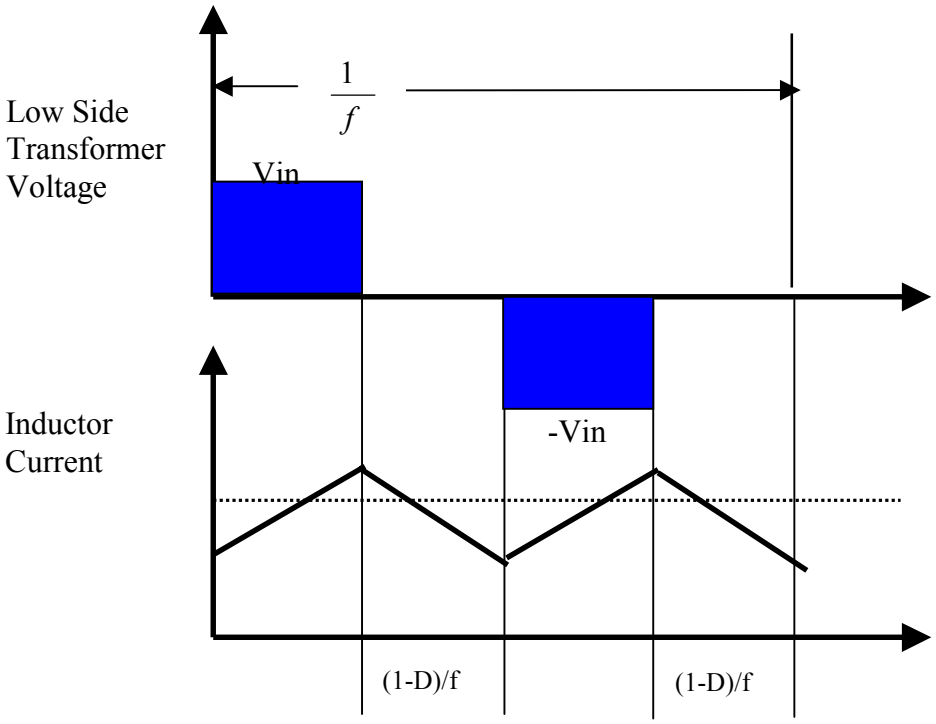


Figure 2-7. Waveforms for buck mode

2.9. Conclusion

The planar transformer design is similar to the traditional wire wound design procedure. The planar transformer design still has to obey both Faraday's and Ampere's law. However, the traditional design uses an area-product design method that does not apply to the planar condition. Also, the copper weight is chosen differently than the circular wire size, because of the cooling requirement. In a wire wound transformer the insulation is very thin. This makes it difficult for cooling reasons. The planar configuration keeps the copper planes separated from each other, which in return results in better cooling.

Since the converter operates as both a boost converter and a buck converter, both conditions must be considered in the design. With boost mode carrying a higher current, the copper weight was designed based on the converter operating in boost mode. The cross sectional area of the core was also considered during the boost mode operation. This is because the flux density is greatest during the boost mode operating condition.

Chapter 3. Parasitic and Leakage Inductance

3.1. Introduction

The leakage and parasitic inductances are often an undesirable component of the system. These inductances cause losses in the circuit that decreases the efficiency of the system. However, in this topology, soft switching was required. This implies that it can use the inductance to store energy, that permits zero voltage and zero current switching. It was shown in Table 2-1 that 5 μH of inductance measured from the secondary side of the transformer was needed to store enough energy for soft switching over the desired load range. It is imperative that this inductance is accurately measured to ensure the soft switching will occur.

3.2. Transformer Leakage Inductance

3.2.1. Theory

The flux that does not couple from the primary to the secondary, circulates within the transformer, this flux is termed leakage flux [6]. This flux creates an inductance according to equation (13). As the coupling between the primary and secondary decreases, the leakage flux increases and therefore the leakage inductance will increase. Figure 3-1 shows a model for the non-ideal transformer. The leakage inductance is represented by $L_{lk,}$ L_m is the magnetizing inductance and the last section is an ideal transformer (perfect coupling). This project specified 5 μH of leakage inductance measured from the secondary. Traditionally, planar transformers use an interleaved structure [29]. An interleaved PCB structure means that each layer of the primary is placed between secondary layers as shown in Figure 3-2 C. The interleaved structure will create the best coupling and therefore the lowest leakage inductance. In this design, because the requirement of high leakage inductance, the interleaved structure is excluded to ensure the leakage inductance is high as possible.

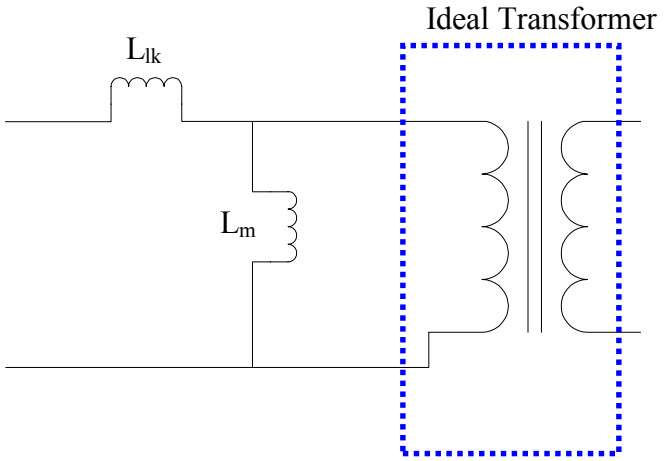


Figure 3-1 Non-ideal transformer model

$$L = \frac{\Phi}{I} \qquad (13)$$

ϕ = Flux (Weber)
I=Current (A)

3.2.2. PCB Layout

Figure 3-2 A shows the PCB layout configuration that was designed and tested. This configuration separates the primary from the secondary with an extra layer of insulation and copper that can be used to increase the leakage inductance. By separating the primary and secondary the coupling will decrease. The extra copper layer is used for the gate drive signals, which are separated from the transformer windings and only adds insulation between the primary and secondary of the transformer. The total distance between the primary and the secondary is referred to as the leakage layer. This structure can be estimated by the simpler structure shown in Figure 3-2 B. The estimated structure is not an exact representation. However, for the leakage inductance calculation it can give an accurate result

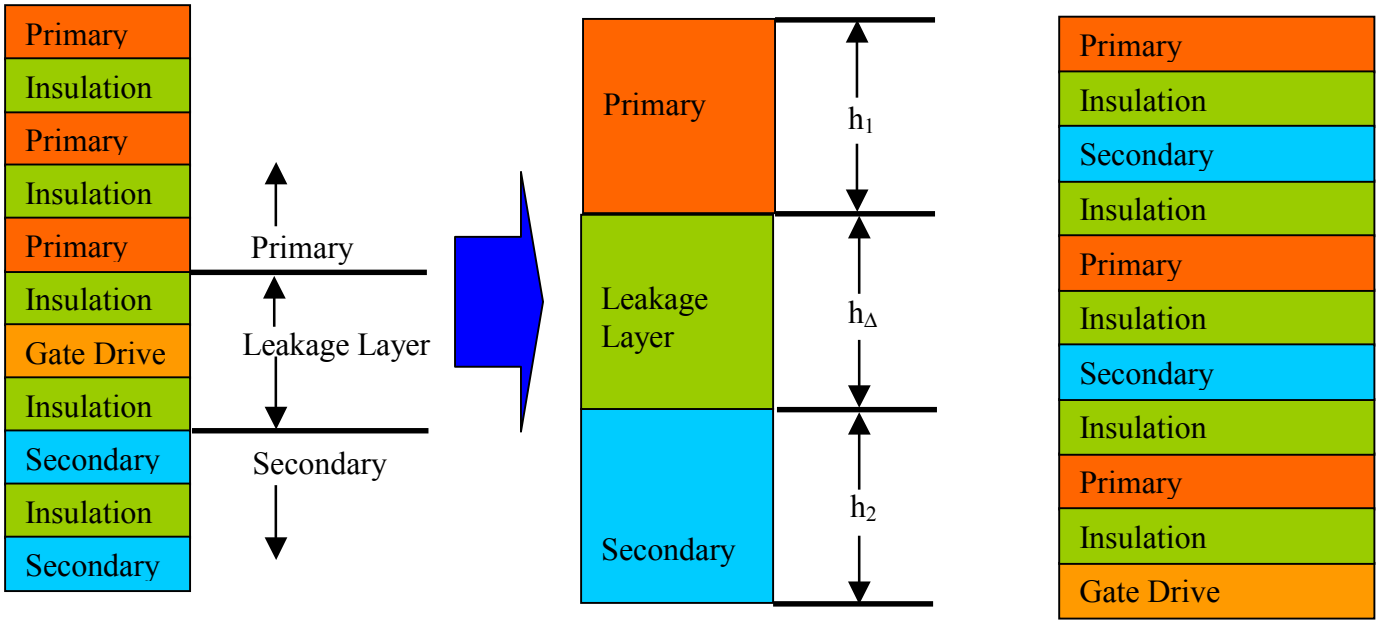


Figure 3-2. PCB layout configurations

3.3. Calculation

The leakage inductance is a result of energy storage in the transformer. In ideal transformers, no energy is stored and therefore the leakage inductance is zero. The energy storage in a transformer is given by equation (14) [21]. Figure 3-3 further describes the geometry of the transformer system.

$$EnergyStored = \frac{\mu_0}{2} \oint H^2 dx l_w b_w \qquad (14)$$

μ_0 = permeability of air (H/m)
H = field strength (A/m)
dx = thickness of winding (m)
l_w = mean length of winding (m)
b_w = winding breadth (m)

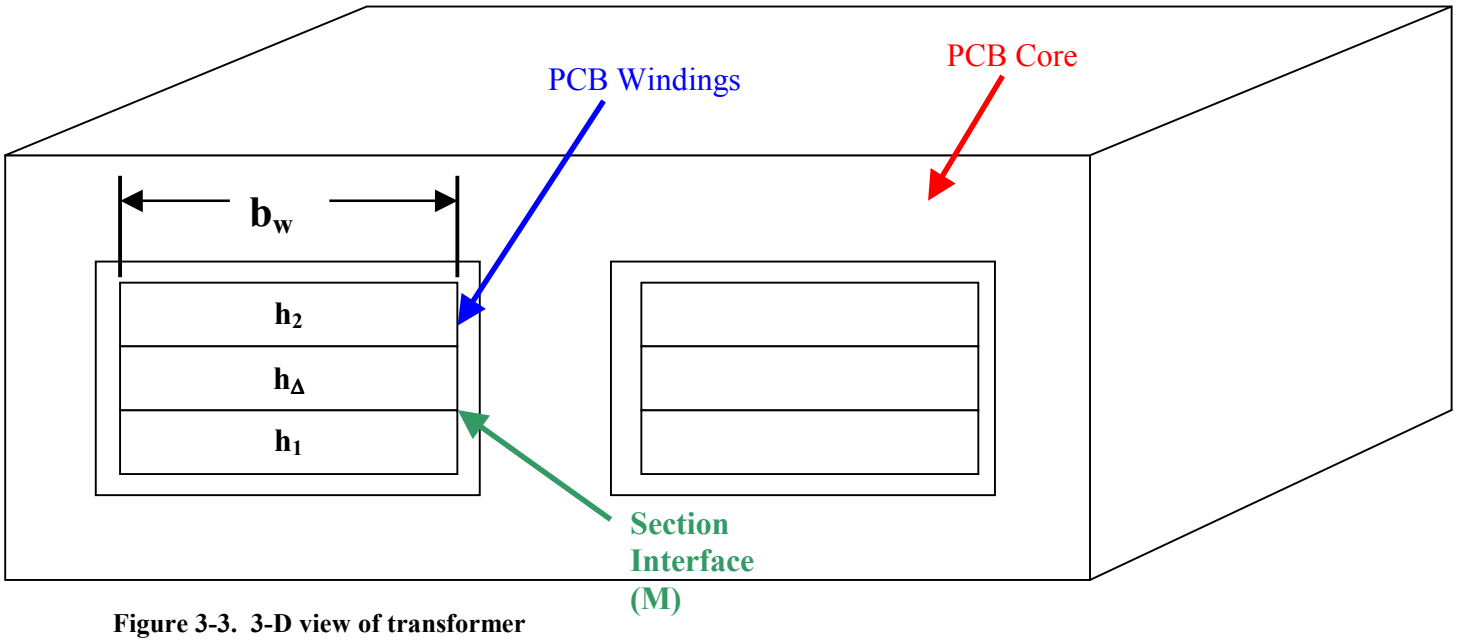


Figure 3-3. 3-D view of transformer

Equation (14) can be further broken down into the energy storage from the primary, secondary, and the leakage layer. This equation is shown in (15). Since the energy is stored in an equivalent inductance the equation is equal to 0.5*L*I^2. Setting (15) equal to this and simplifying, gives equation (16). Equation (16) is for a two winding structure. The formula would vary if more layers were constructed. For this case the PCB shown in Figure 3-2 A was estimated by Figure 3-2 B which only considers two windings.

$$EnergyStored = \frac{\mu_0 l_W b_W}{2}\left\{\int_0^{h_1}\left(\frac{N_1 I_1 x}{b_W h_1}\right)^2 dx + \left(\frac{N_1 I_1 x}{b_W}\right)^2 h_\Delta + \int_0^{h_2}\left(\frac{N_2 I_2 x}{b_W h_2}\right)^2 dx\right\} \quad (15)$$

N = number turns
I = current (A)
h = thickness (m)

$$L_{lk} = \mu_o N^2 \frac{l_w}{b_w}\left(\frac{h_1 + h_2}{3} + h_\Delta\right) \quad (16)$$

μ_o (H/m)
l_w = mean length of traces (m)
b_w = width of primary trace (m)

If an interleaved structure is used, then equation (15) simplifies to equation (17). In (17) M is the number of section interfaces. This is the number of times that the primary is mated against the secondary layer. Using the interleaved PCB shown in Figure 3-2 C the number of section interfaces is 4.

$$L_{lk} = \mu_o \frac{N^2 l_w}{M^2 b_w}\left(\frac{\sum h_i}{3} + \sum h_\Delta\right) \qquad (17)$$

μ_o (H/m)
l_w = mean length of traces (m)
b_w = width of primary trace (m)
M = number of section interfaces

In (16) h_1 and h_2 are taken as the copper thickness only, it does not include the insulation between the layers, the insulation will be considered in the h_Δ term. The ambiguous part of equation (16) is what to use for h_Δ, Figure 3-4 shows the leakage inductance as a function of the separation, h_Δ in mils. The three different curves represent three different copper weights. The red solid line is using 6 oz copper and 20 mil insulation between each layer. The blue dashed line represents 2 oz copper and 20 mil spacing between each layer. The green dado line represents 2 oz copper on the outer two layers, 0.5 oz copper on the inner four layers, and 3 mils for each insulation layer. This graph proves that the leakage inductance will change between the different copper weights. However, given a fixed copper weight the insulation could be changed to adjust the leakage inductance. Since the primary and secondary both have insulation between them, the effective h_Δ will be the leakage layer thickness plus the average for the insulation between primary layers and secondary layers. Table 3-1 shows the h_Δ that should be used for calculating the leakage inductance for each case. For instance, in the 2 oz copper case with 20 mils of insulation the h_Δ is 40 mils (leakage layer) of insulation between the primary and secondary then for the average of the primary will have the average of two layers of insulation $\left(\frac{20+20}{2}\right)$ plus the average of the insulation between the secondary windings $\left(\frac{20}{2}\right)$ plus one layer of copper from the secondary layer that is 2 oz weight and each oz is 1.4 mils thick, this gives a total of 72.8 mils.

Table 3-1. h_Δ for different cases

Case:	h_Δ (mils)
2 oz outer, 0.5 oz inner, 3 mils insulation	$3+3++0.5*1.4+\frac{3}{2}+\frac{3+3}{2}=11.2$
2 oz copper, 20 mils insulation	$20+20+1.4*2+\frac{20}{2}+\frac{20+20}{2}=72.8$
6 oz copper, 20 mils insulation	$20+20+1.4*6+\frac{20}{2}+\frac{20+20}{2}=78.4$
6 oz copper, 20 mils insulation, interleaved	20

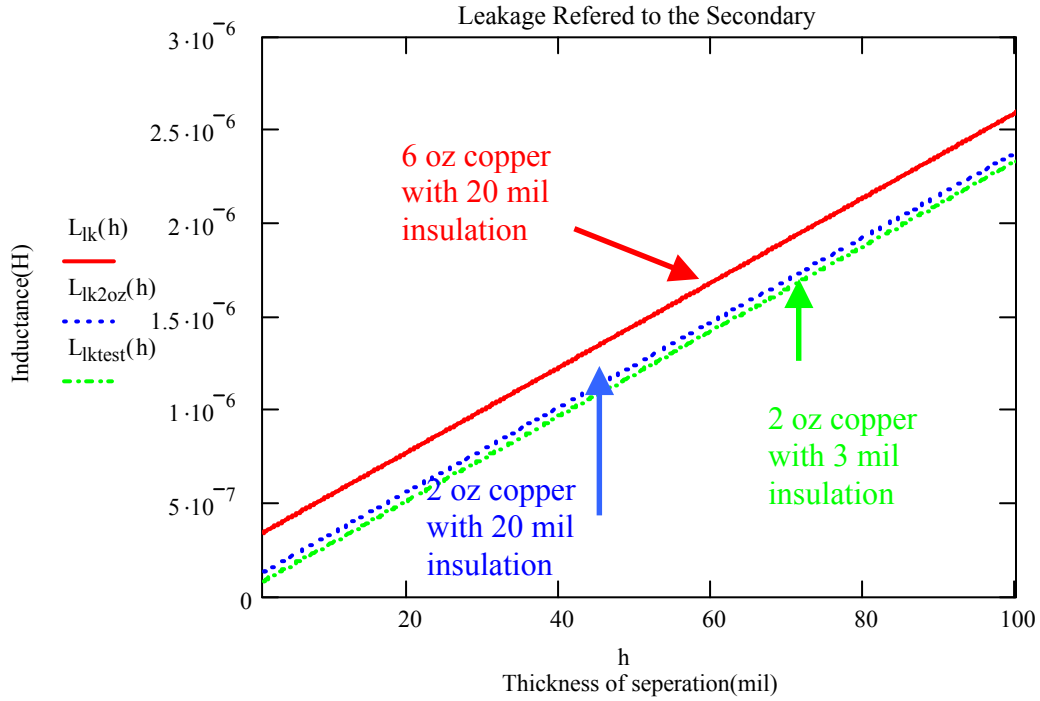


Figure 3-4 Leakage inductance calculated from the secondary

The final production PCB will be 6 oz copper with 20 mil insulation between each layer. Referring to equation (16) the leakage inductance is calculated to be 2.1 µH. This is below the design requirement of 5 µH. However, many estimations were used with this formula. To get a more accurate leakage inductance a finite element approach should be taken. Table 3-2 shows a summary for all the leakage inductances calculated at 100 kHz.

Table 3-2. Calculated leakage inductance

	Calculated Inductance (μH)
2 oz outer, 0.5 oz inner, 3 mils insulation	0.31
2 oz copper, 20 mils insulation	1.76
6 oz copper, 20 mils insulation	2.1
6 oz copper, 20 mils insulation, interleaved	0.134

3.4. Maxwell™ Modeling for the Transformer Leakage Inductance

3.4.1. Introduction

Maxwell software designed by Ansoft can be used to solve Maxwell's equations for both static and time varying fields with finite element analysis (FEM) method. The basic principle behind FEM is that it breaks up the problem into smaller sections, which are equilateral triangles. The fields can then be solved for 6 points on the triangle if a two dimensional problem is assumed. If a three-dimensional problem is used then the program will solve for ten points on the triangle. Equations (18)- (21) are the differential form of Maxwell's equations [2]. In these equations **B** is a vector representing the flux density, **E** is a vector representing the electric field, **D** is a vector that represents the electric flux density, finally **H** is a vector that represents the magnetic field intensity [2]. The first step in the process is to define a model that represents the transformer was chosen. Many different options are available. For this case a 2-D representation of the transformer. Although a more complete solution could be obtained from a 3-D simulation. However, the 3-D simulation is very time consuming and the precise solution is not always obtained. The problem with the 3-D simulation is that it must create many more triangles to solve the problem. Using the 3-D approach it might lose important accuracy of the fields between the windings. The advantage of the 3-D version is that it will model the sections of the transformer that are not covered by the ferrite core and the interconnection between the two cores.

$$\nabla X\vec{E} = -\frac{\partial \vec{B}}{\partial t} \quad (18)$$

$$\nabla X\vec{H} = J + \frac{\partial \vec{D}}{\partial t} \quad (19)$$

$$\nabla \bullet \vec{D} = \rho \quad (20)$$

$$\nabla \bullet \vec{B} = 0 \quad (21)$$

3.4.2. Define Simulation

It is very important to accurately reflect the problem of interest. Since a two-dimensional problem was simulated, it was important to reflect the three-dimensional problem in two-dimensional space, and still have an accurate representation. To do this the transformer first had to be modeled in such a way that the problem shows symmetry. Figure 3-5 shows a three-dimensional view of the transformer structure. The three-dimensional structure does have symmetry and can be accurately modeled if the transformer was split through the transformer core. The blue cut line represents the point at which the transformer was split. Using this separation point only one transformer is modeled at a time. This simulation will not show any interactions that might occur as a result of the transformer system. However, it will show important magnetic field properties.

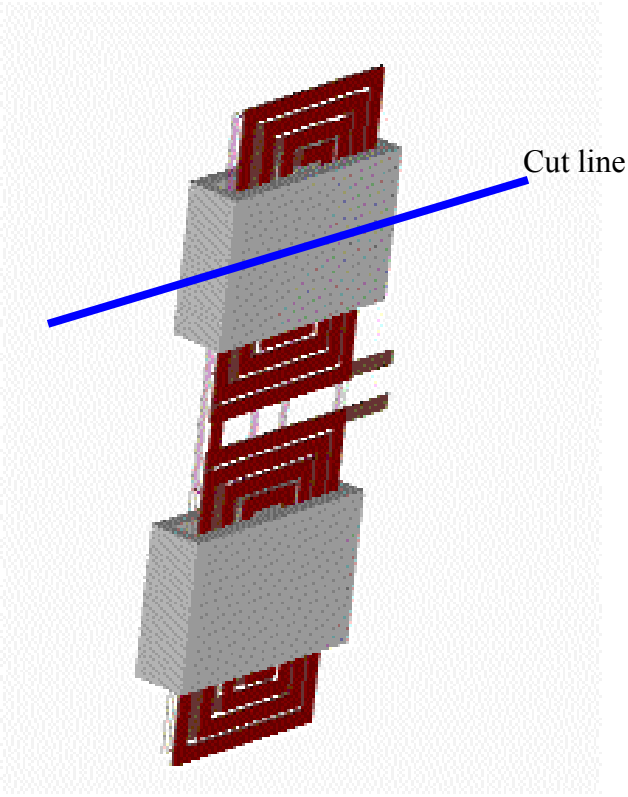


Figure 3-5. 3-D view of transformer

Using this scheme the calculations will assume that the transformer extends into infinity. Figure 3-6 shows the two-dimensional representation. In Figure 3-6 the gray area represents the ferrite core material, the green represents the insulation material, and the brown is a representation of the copper PCB traces. This is only a model of one core and it assumes that the core continues in the Z direction (into the page) for infinity.

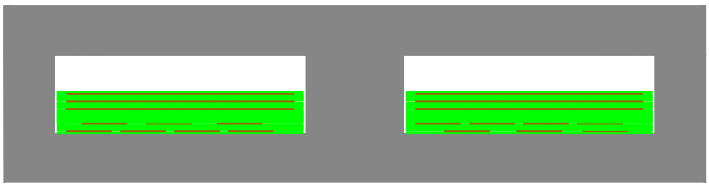


Figure 3-6. 2-D transformer model

Figure 3-7 shows a closer view of one section of the PCB core. The top three thin brown layers are the primary layers. They are 0.0028 in thick, which represents 2 oz/ ft^2 of copper. This Autocad representation of the PCB and ferrite core can then be imported into the Maxwell's software package for further analysis.

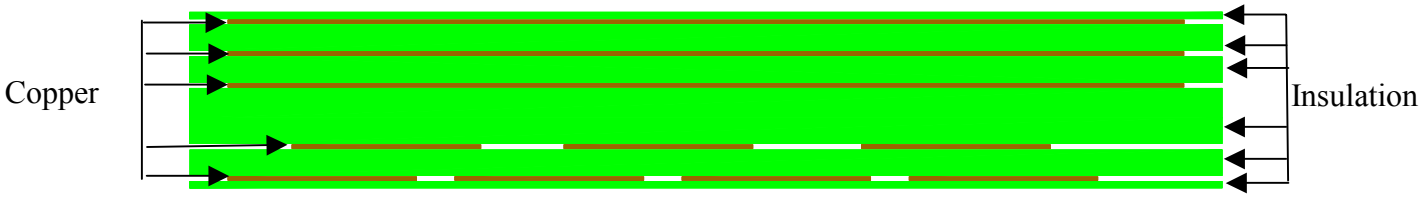


Figure 3-7. 2-D PCB model

Once the drawings have been accurately represented, it is important to accurately represent the transformer system. For this system, many different simulations methods are available to find the leakage inductance and field representations. One is the magnetostatic solver. This one assumes a constant source as the input and solves the magnetic field inside the design space. This method is not used because the most important parameters are a result of an AC input. Another method is the eddy current solver. This solver inputs a sinusoidal input at a specific frequency and again solves the magnetic fields within the system. Another section of Maxwell is called PEMag which can easily solve for the parasitic elements of the system. This method will assume that the system is symmetric in the X-direction and the Z-direction when it makes the calculations.

The materials used in the simulation must also be assigned. Here the 3C90 ferrite material from Philips is adopted. This material had to be defined so that the proper B-H characteristics were used in the simulations. Figure 3-8 shows the B-H curve that was entered into Maxwell..

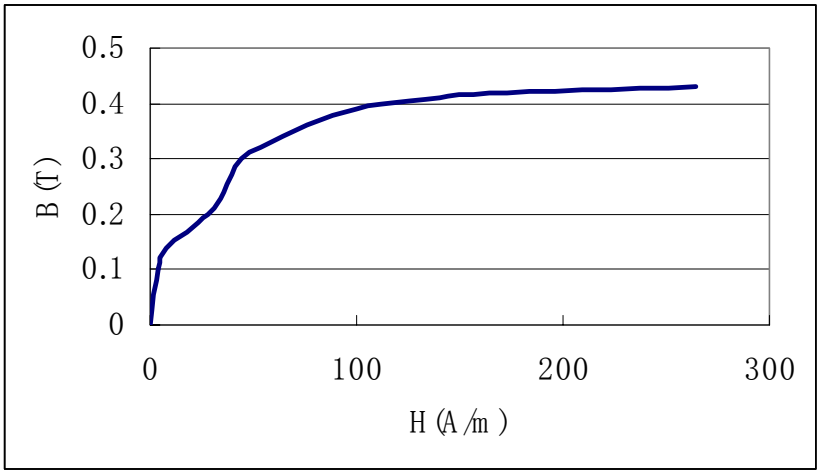


Figure 3-8. B-H for 3C90

3.4.3. Eddy Current Solver

The eddy current solver can be used for finding the AC fields at a certain frequency. Since the converter is operating at 100 kHz, this was the main frequency of interest. The input to the system is a sine wave instead of a square wave that the transformer will operate at. The result should be very similar between a sine wave and a square wave, and can be used as a good approximation. The correct mesh, which is aset of triangles used for calculation, is very important when simulating any finite element problem. If the mesh is too fine, then the simulation will take much too long. If the mesh is too coarse then the result will not be accurate enough. Figure 3-9 shows the mesh that was used for all the simulations. The mesh was refined in the area of the PCB traces and insulation. This is because the fields in this area need to be known with relatively good accuracy.

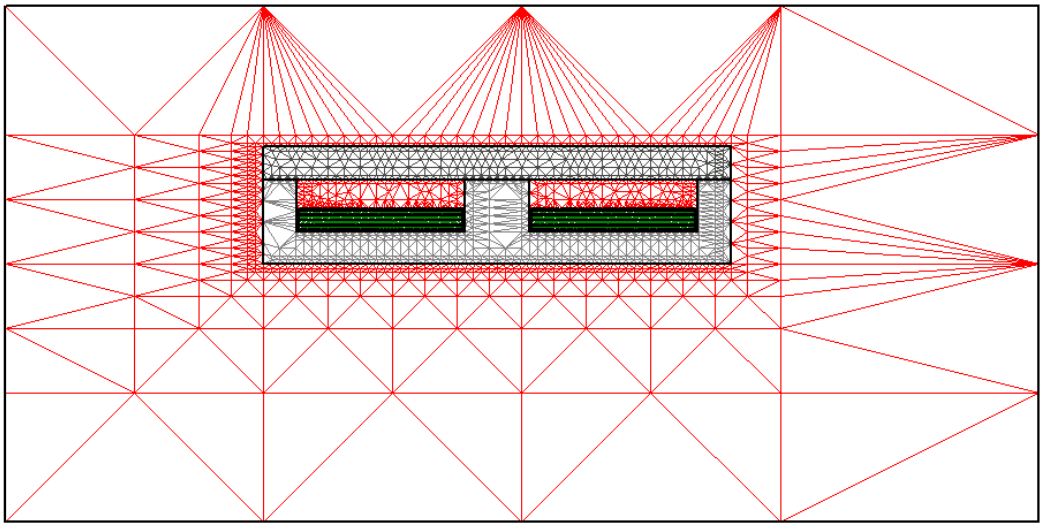


Figure 3-9. Mesh used in simulation

The main reason of the eddy current solver is to find the field intensities at different points in the core and windings. This will determine the current distributions, core hot spots, and many other transformer performance parameters. Figure 3-10 shows a contour plot of the flux inside of the transformer. The flux is both positive and negative. This is because the current is positive on the left side of the transformer and negative on the right side of the transformer. On the left side of Figure 3-10 the flux is in the positive direction and represented in red. On the right side of Figure 3-10 the flux is going in the opposite direction and represented in blue. The different shades of green represent near zero flux. This is the area outside of the core. It is desired that this flux is zero, because it can induce current in surrounding circuits. However, it is seen that the flux is very small outside of the core but not zero. The flux inside of the core is the greatest near the copper traces and decreases further away from these traces. This is because the flux is generated from the current flowing in the copper conductors.

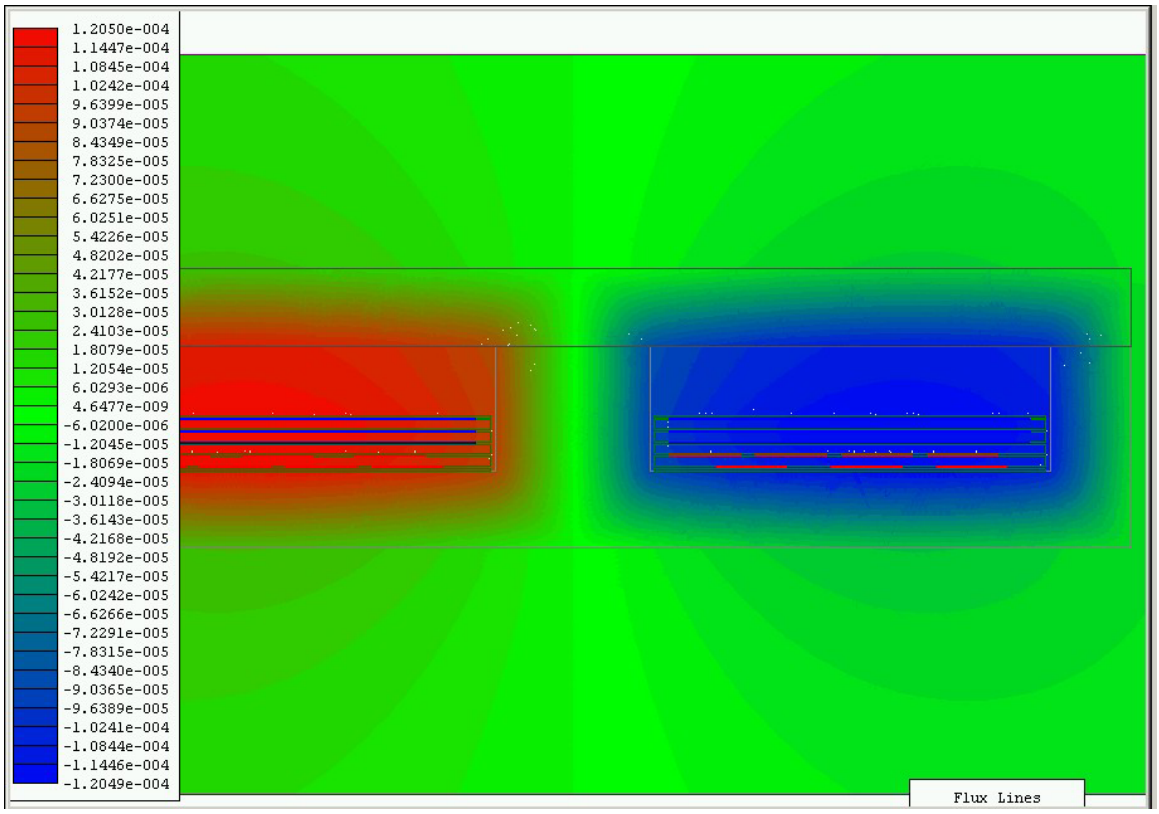


Figure 3-10. Flux Density

The magnitude of the flux density is another very important aspect of the transformer's performance. The flux density is directly related to the power loss of the transformer. Since, the power loss is also directly related to the temperature rise, the magnitude of the flux density can find the hot spots of the transformer. Figure 3-11 shows a contour plot of the flux density. This plot shows that the outer edges of the transformer and the center leg of the core will become the hottest parts of the transformer. These considerations should be taken into account when mounting the transformer. A mounting scheme should be devised in which the outer edges and the center should have ample force applied to the heatsink.

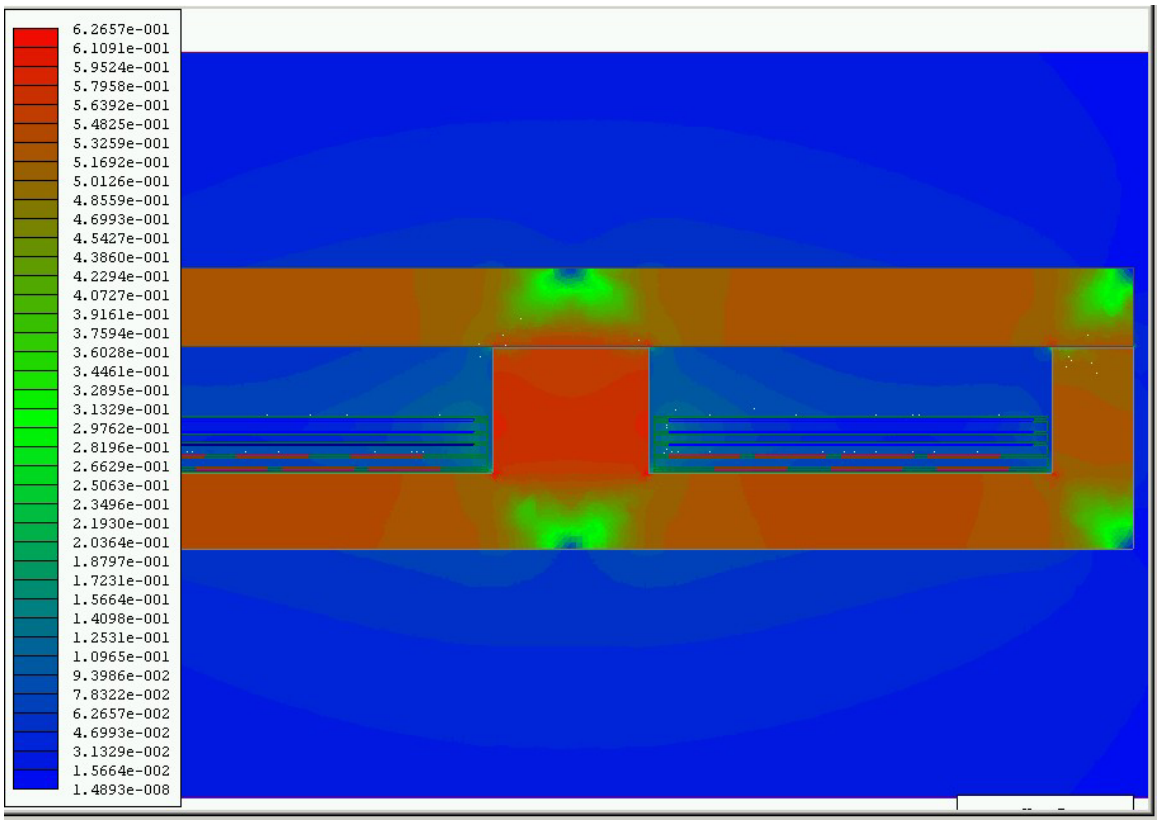


Figure 3-11. Magnitude of flux density

The final useful parameter of the eddy current solver is the magnitude of the H field. This parameter can be used to figure out the current distribution of the copper traces. The current distribution is essential to determine the heating of the PCB trace. One area of the trace carries all of the current then this area of the trace is much hotter and could break down the insulation in that area. Equation (22) shows that the current is related to the H field [6]. This implies that the greater the H field the greater the current will be in that area. Figure 3-12 shows a contour plot of the H-field.

Total current passing through interior of path = $\oint Hdl$ (22)

H=magnetic field intensity

If this plot is examined closely in the area around the copper planes, it can be seen that the H-field is higher at the outer edges of the PCB traces. This simulation did not input current into the secondary. If this were done, then it could be seen that the H-field would greater between the

primary and secondary layers. This implies that the current will be higher at the outer edges of the PCB traces and the traces that are closer to the primary-secondary border.

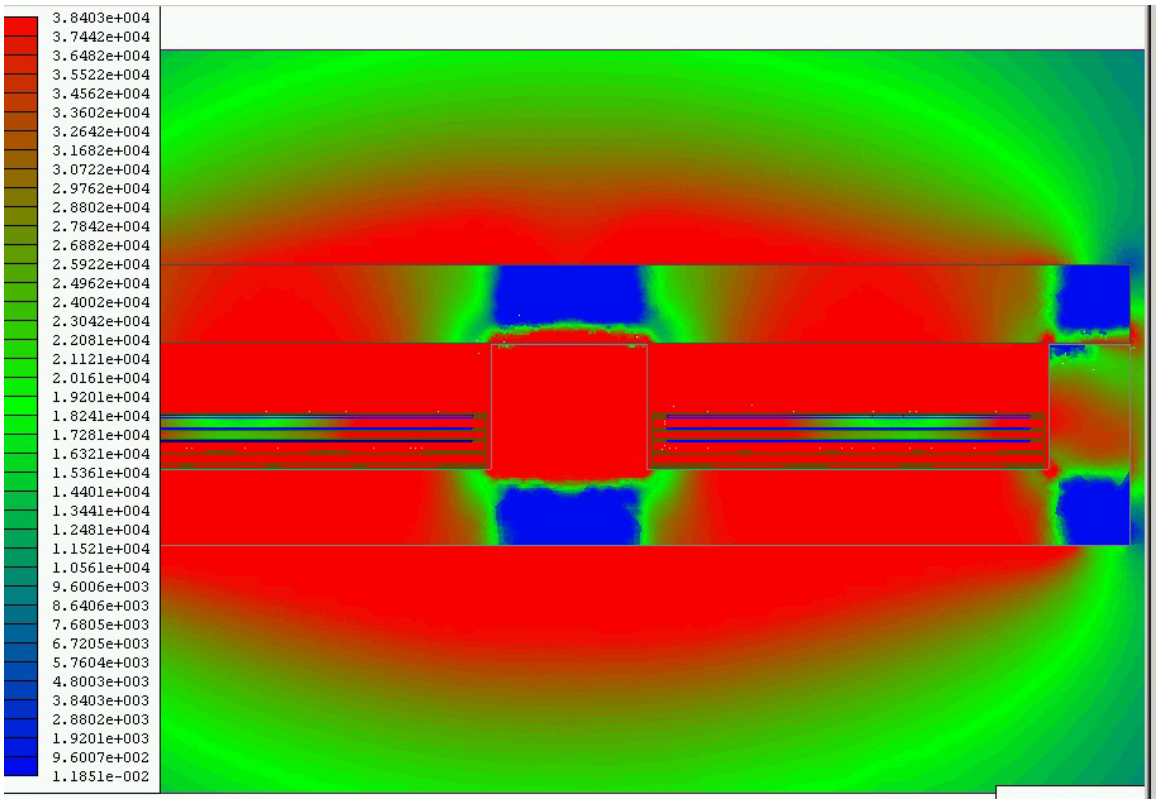


Figure 3-12. Magnitude of H-field

3.4.4. PEMag

PEMag is a section of Maxwell that is specifically designed for analysis of transformer and inductors. It assumes that the structure is symmetrical and can solve for inductances, capacitances, and resistances from the given structure. PEMag is simply an interface to the two-dimensional finite element solver that has the predefined equations for solving the inductances, capacitances, and resistances. This program sweeps through the desired frequencies to find the parasitic elements at each frequency point. The disadvantage with using this software package is that it assumes a symmetrical structure in both the X-direction and the Z-direction. Figure 3-13 shows a picture of the structure that was used in this simulation. Since the transformer does not have an even number of turns per layer, it is not symmetrical in the X direction. One side will have four turns on the top secondary layer and the other side will have three turns on the top

secondary layer. However, the structure is symmetrical in the Z-direction and this assumption is valid. One major advantage of this program is that it already has the manufacture's cores and material properties predefined. Figure 3-13 shows a figure of an EI58 core with 3C90 material. Since it assumes that the structure is symmetrical in the X-direction, two different simulations are conducted. The first one is with the bottom secondary layer having three turns and the top secondary having four turns. The second one is with the bottom secondary having four turns and the top secondary having three turns. The actual transformer that was built will have a leakage inductance that is in the middle of these two cases. This is because the transformer that is built will have three top turns on one side and four top turns on the other side.

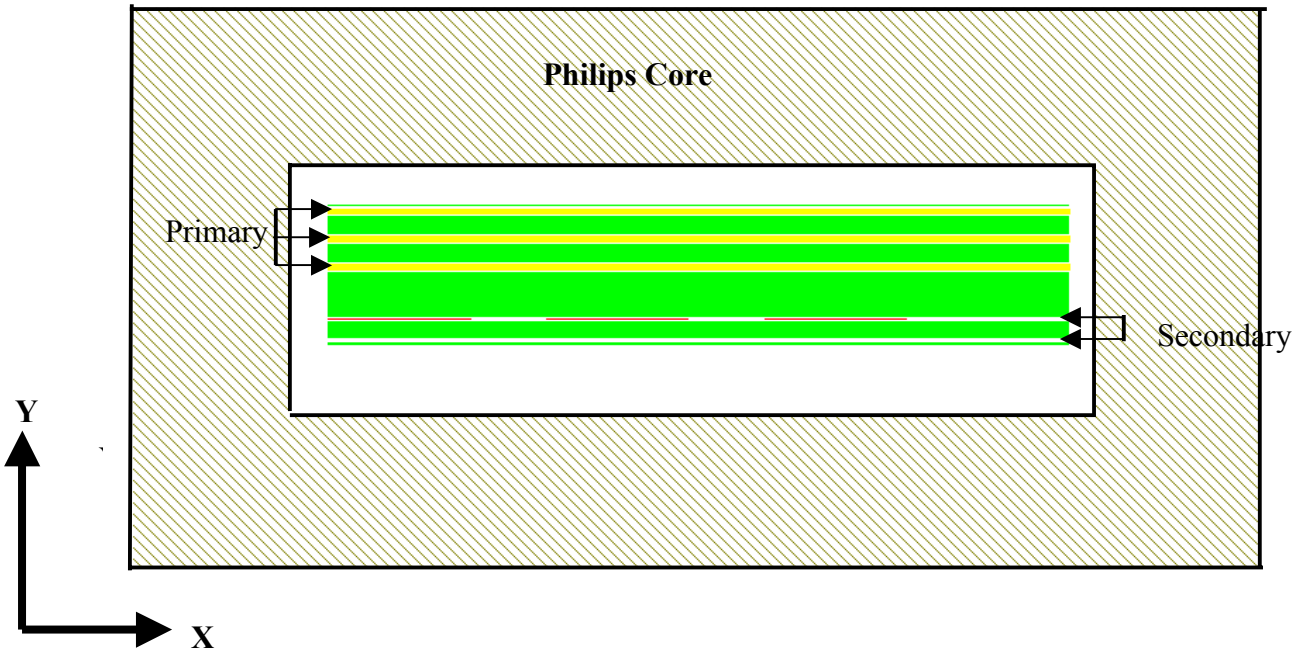


Figure 3-13. PEMag simulation figure

For the 2 oz copper case the leakage inductance was calculated for different simulations when the top secondary layer has three turns and when the top secondary layer has four turns. Figure 3-14 shows the simulation results along with the line for the calculated results. The simulation result is based on a two-dimensional field simulation. Llk1 represents the leakage inductance calculated when four traces were on the top secondary and three traces on the bottom secondary (Shown in Figure 3-15 A). Llk2 represents the leakage inductance with the top

secondary having three traces and the bottom secondary has four traces (Shown in Figure 3-15 B). The other designation is *Middle* and *Bottom* this specifies the placement of the PCB in the core. In the case that is denoted by *Middle* the PCB was placed in the middle of the window opening both in the vertical and horizontal positions. For the case denoted as *Bottom* the PCB was placed near the bottom of the window opening in the vertical position but still in the middle for the horizontal position. Noticing from Figure 3-14 the difference from the maximum simulation result and the minimum simulation result is 88 nH looking from the secondary side of the transformer. This gives an error of ±10% for the single transformer case. This is reasonable considering that that the error of the program is 5%. The blue line represents the calculated result that was explained in the transformer design section (Table 3-2). This gives a greater result that the finite element approach. This is reasonable because the calculation used a one-dimensional approach that lumped the primary together and the secondary together. The leakage was then computed based on the average spacing between the lumped primary and secondary. The lumping of the primary and secondary layers gives a reasonably accurate result. However, the two-dimensional finite element will consider more effects into the calculation. Also, from Figure 3-14 the Llk2 is greater than Llk1. This also is reasonable because Llk2 is the case that has the top secondary having three windings and the bottom secondary having four windings. This winding configuration will provide more leakage flux because the secondary does not have as much copper area on the layer that is closest to the primary. The lack of copper area allows more flux to escape and not couple from the primary to the secondary.

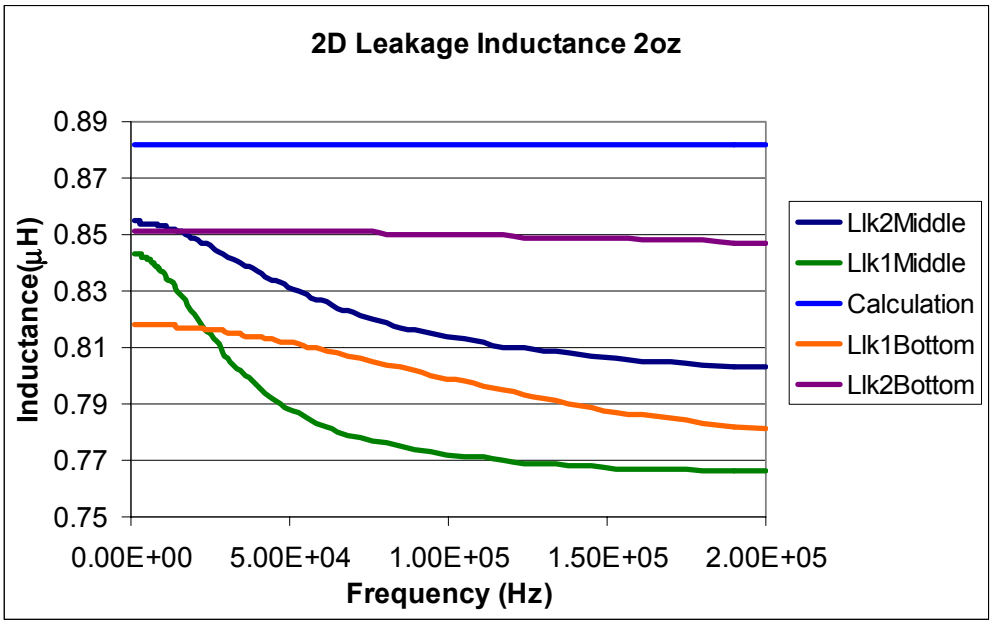
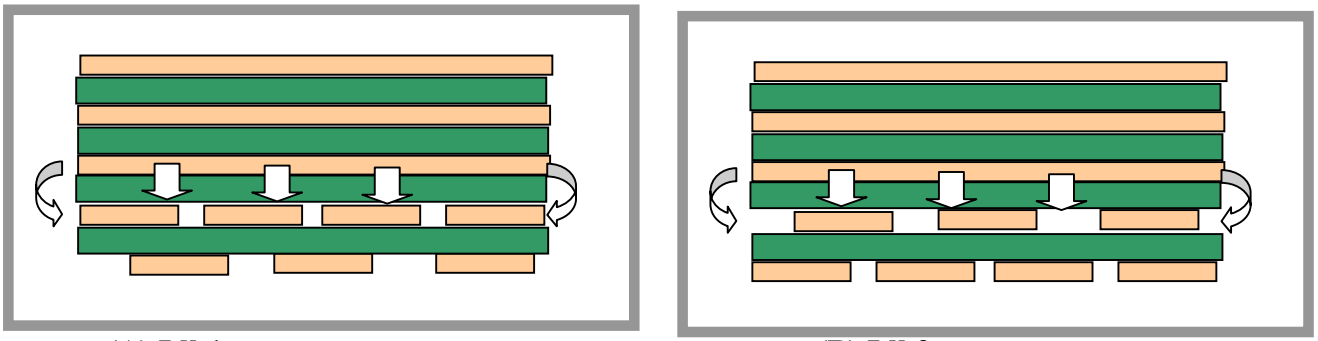


Figure 3-14. 2oz simulation results



(A) Llk1 **(B) Llk2**

Figure 3-15. Simulation structures

All of the above simulation results match relatively closely to the original lumped parameter model. The simulations were done with all of the primary layers connected in parallel. This implies that the current will distribute among these layers based only on the DC resistance. In the studied case, the windings are equal and the DC resistance is the same. If the DC resistance is the same then the current will share evenly. This is the same assumption that was made in the original calculation.

If all of the primary windings are separated and then shorted after the simulation has run, a better understanding of the current sharing and actual leakage inductance can be determined. As the previous section proved the inner layers will carry more current than the outer layers. Therefore the flux is higher for these sections. Figure 3-16 shows a graph of the leakage

inductance referred to the secondary side. The model is for Llk2 case (Figure 3-15 B) with the PCB in the middle of the window opening. Comparing Figure 3-14 with Figure 3-16 the low frequency leakage inductance is the same for the Llk2middle case. As the frequency starts to increase the leakage inductance will start to drop off faster for the case when the current does not distribute evenly. It is not a drastic change because the frequency is limited to 200 kHz, which is relatively low frequency. At 100 kHz the leakage inductance is only different by 7 nH. Given the tolerance of the calculation, this is an acceptable difference.

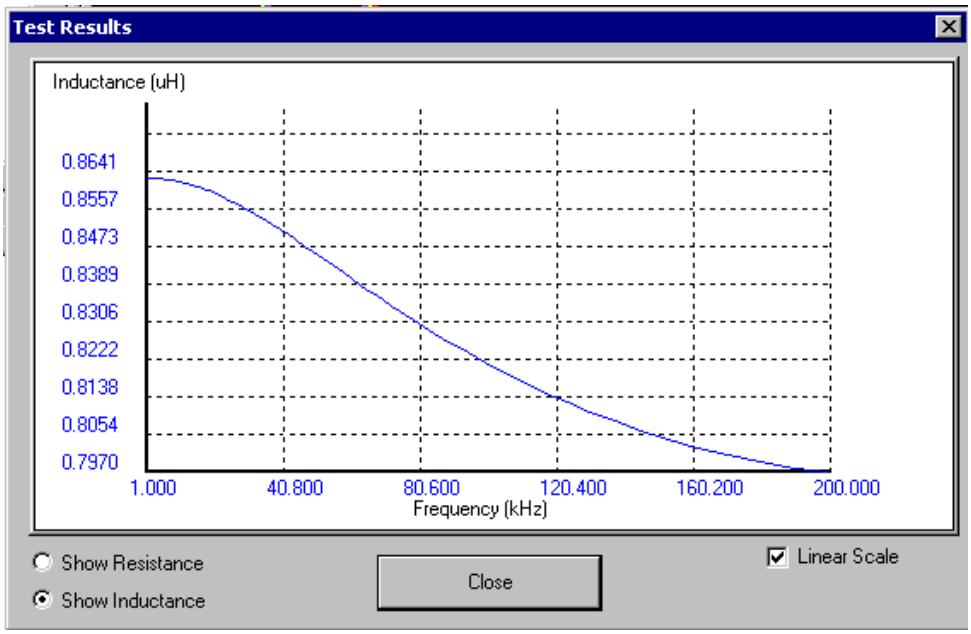


Figure 3-16. Leakage inductance when even current distribution is not assumed

3.4.5. Maxwell Simulation Conclusion

The eddy current solver has proven to be very valuable in observing the different field effects inside of the transformer. These effects can be used to better determine the temperature rise of both the copper traces and the ferrite core. Also the flux outside of the core can be useful in determining any radiated EMI that could induce noise on nearby components. The disadvantage of the eddy current solver is that it is not optimized for determining the parasitic elements of the transformer structure. For the parasitic elements, PEMag is much more convenient. PEMag solved for the leakage inductances and capacitances at the different

frequencies. The leakage inductance is the main parameter, and is proven to be very similar to the calculated result found in the previous chapter. This leakage inductance is only for one transformer. Since the secondary of the transformers are connected in series the total leakage inductance is doubled to form the total leakage inductance seen by the circuit.

3.5. Parasitic Inductance

3.5.1. Theory

The leakage inductance was measured by shorting the primary through the device's footprint in the PCB. This implies that included with the leakage inductance, the self-inductance of the traces was also included in the measurement. The trace inductance can be very significant. This is because the trace inductance is on the primary side and the specification (5 μH) was for the secondary side. This means that the trace inductance seen on the secondary side is multiplied by the turns ratio squared. In many cases this is not significant. However, in this design the turns ratio is large, and the reflected inductance could be significant. Since the turns ratio is 1:14, 1 nH of trace inductance on the primary is 0.2 μH on the secondary. Depending the way the leakage was measured different trace inductances will be included.

3.5.2. Inductance Source

Figure 3-17 shows a screen capture of the PCB that was designed and tested. L_1, L_2, L_3, L_4, L_X, L_{DC-} and L_{DC+} represent the lumped trace inductances that can be measured. The lumping method is based on the geometrical structure of the PCB traces. Unlike conventional definition of leakage inductance, which is normally referring to the transformer leakage inductance, it is obvious from the PCB capture that the circuit trace inductances can be far larger than the transformer leakage inductance. This figure also shows the device package, and that the device can be shorted by a very short copper strip from the drain of the MOSFET to the source of the MOSFET.

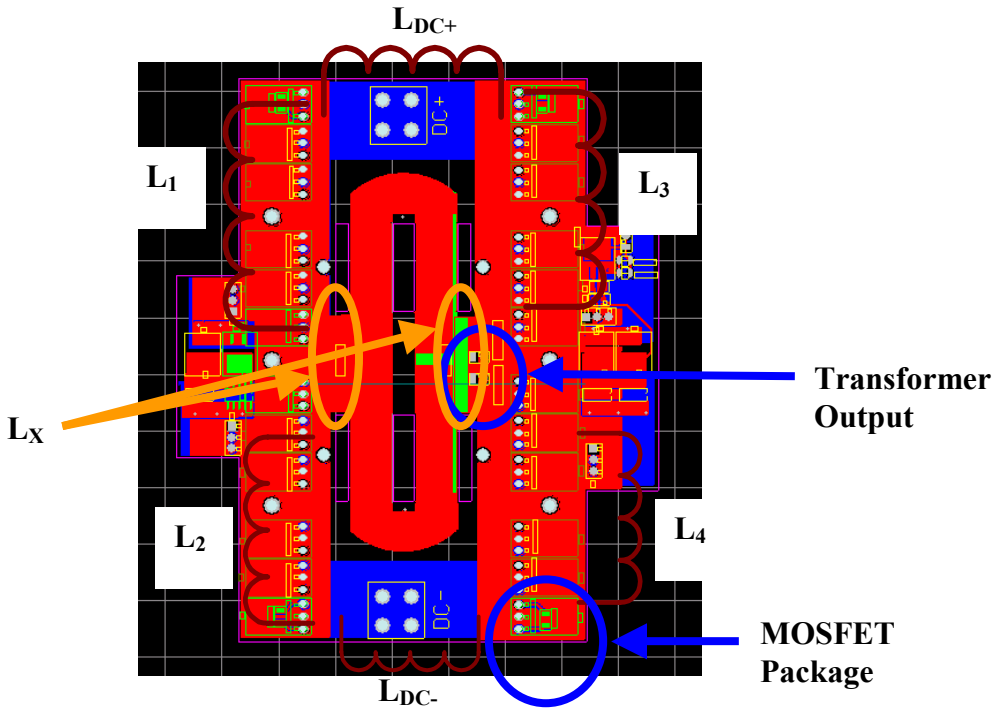


Figure 3-17. PCB Layout

Many different inducances make up these the trace inductances. Each of the many inductances can be added together to form an equivalent inducance that can be calculated or measured. Figure 3-18 A shows the complete parasitic inductance circuit. Since the circuit has 6 MOSFETs in parallel, each one will create a parasitic inductance that will be placed in the measurement. If the 6 parallel MOSFETs are considered as one, and the inductance from each section are lumped, the result can be shown in Figure 3-18 B. Figure 3-18 B shows that the equivalent circuit comprises of six different inductances. However, Figure 3-17 shows that the layout has symmetry among a center axis. That center axis is the center of the transformer. Since self inductance is only a function of the geometry, Figure 3-18 B can further be reduced with reasonable accuracy by simple geometrical calculation. With symetry of geometry it can be reasonably assumed that $L_1 \cong L_2$, $L_3 \cong L_4$, and $L_{DC+} \cong L_{DC-}$ [8]. Physically L_1, L_2, L_3, and L_4 represent lumped parasitic inductances of each device, which consist of six T0-247 MOSFETs; L_{DC+} and L_{DC-} represent parasitic inductances of the dc bus; and L_X represents the lumped interconnect parasitic inductance from the transformer to the ac terminal.

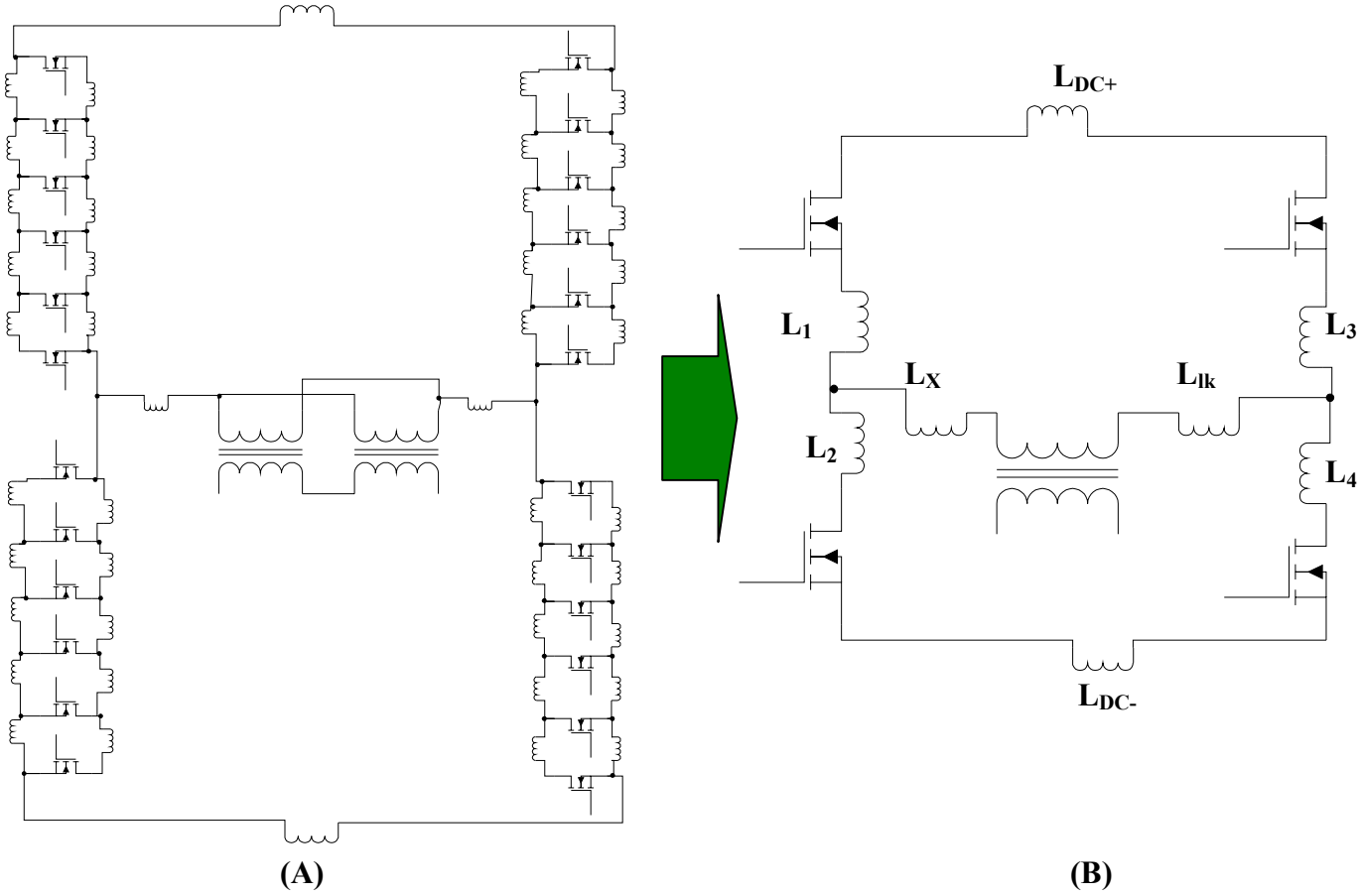


Figure 3-18. Schematic representation of parasitic inductance

3.5.3. Calculation

Using formulas given by [8] a mathematical calculation for the trace inductance can be found. The self inductance of a copper sheet is given in (23) . Inductance is dependent on the geometry of the structure but not on current [8] The widths of the L_2 and L_4 traces are 1.55 in., and the length is 7.4 in. The total thickness for the 2 oz. prototype this is 10 oz. To get L_2 and L_4 given in Figure 3-18 B the thickness can be obtained from three transformer primary layers in parallel, this gives 6 oz., plus the DC- is shorted to in input of the transformer which is 4 oz thick, this gives a total of 10 oz. The other section will be the L_{DC-} trace. This will be 4 oz of copper and 1.35 in wide and the length is 3 in. The calculation for L_X is 14 nH. If these inductance are reflected from the primary side of the transformer to the secondary side of the

transformer, each must be multiplied by the turns ration squared (14^2). The results of these calculations are shown in Table 3-3.

$$L = 0.002l\left(\ln\left(\frac{2l}{B+C}\right)+\frac{1}{2}-\ln(e)\right)(\mu H) \quad (23)$$

l = length(cm)
B = width (cm)
C = thickness(cm)
ln(e)=given in table depending on geometry
(0.00089)

Table 3-3. Calculated trace inductances

	L_1 (μH)	L_2(μH)	L_3(μH)	L_4(μH)	L_{DC-}(μH)	L_{DC+}(μH)	L_X (μH)
L calculated	7.9	7.6	7.9	7.6	6.5	6	2.74

3.6. Impedance Analyzer Measurements

3.6.1. Measurement Setup

Many different measurements were taken to try and isolate which inductances were measured. Since the measurements lumps all of the inductances together it becomes difficult to differentiate between L_1, L_2, L_3, L_4, L_X, L_{DC-}, L_{DC+}, and L_{lk}. The measurements can be manipulated to find the different inductances. The leakage inductance is measured from the secondary with the primary shorted. The primary was shorted by a short copper strip from the drain to source on the MOSFET package. Using this very short piece of copper the inductance added to the system is very little. For this reason the copper wire inductance is assumed to be zero and not effect the measurement result.

3.6.2. Equivalent circuits and measurement results

Figure 3-20 shows the first measurement structure and equivalent circuit. Figure 3-19 A shows the complete circuit and which MOSFETS were shorted. Figure 3-19 B shows the equivalent inductances that were measured, L_2, L_4, L_{DC-}, L_X, and L_{lk}. L_{lk} is considered the leakage inductance of the transformer. Table 3-4 summarizes the measurement results. The results listed in the table are taken at 100 kHz, which is the switching frequency of the transformer.

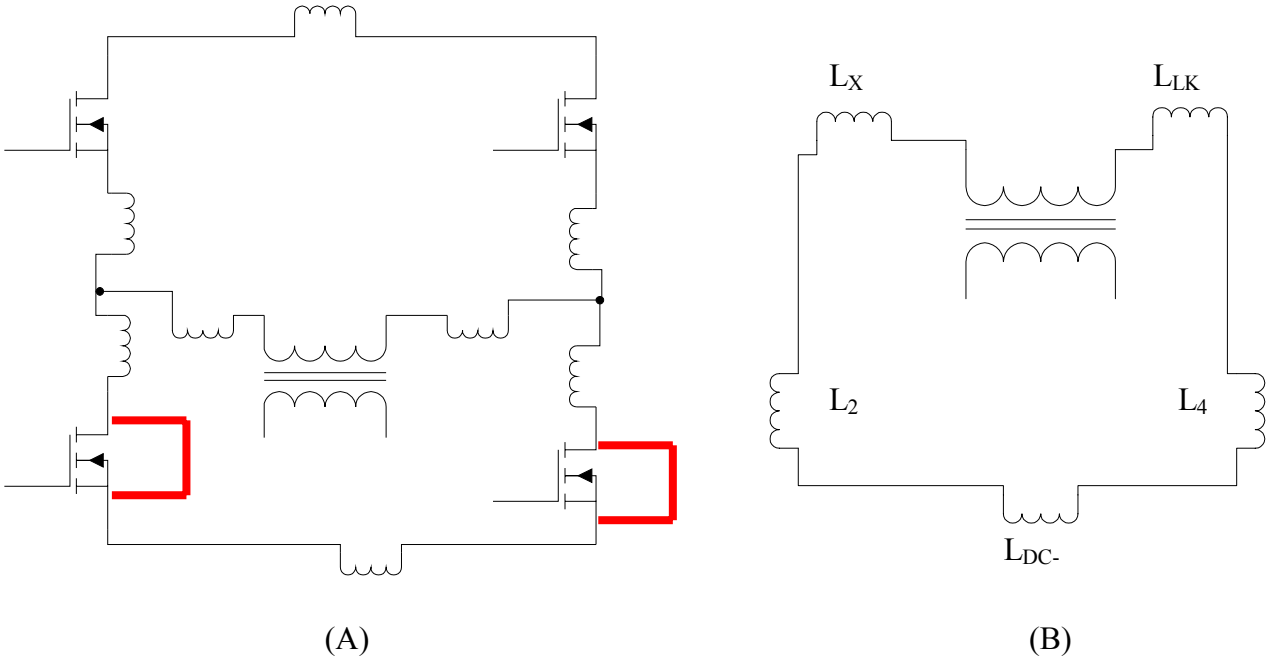


Figure 3-19. Measurement circuit 1

Figure 3-20 A shows the circuit configuration for measurement 2. Figure 3-20 B shows the equivalent inductance that was measured. The measured inductance will be L_1, L_2, L_X, L_{DC+}, and L_{lk}.

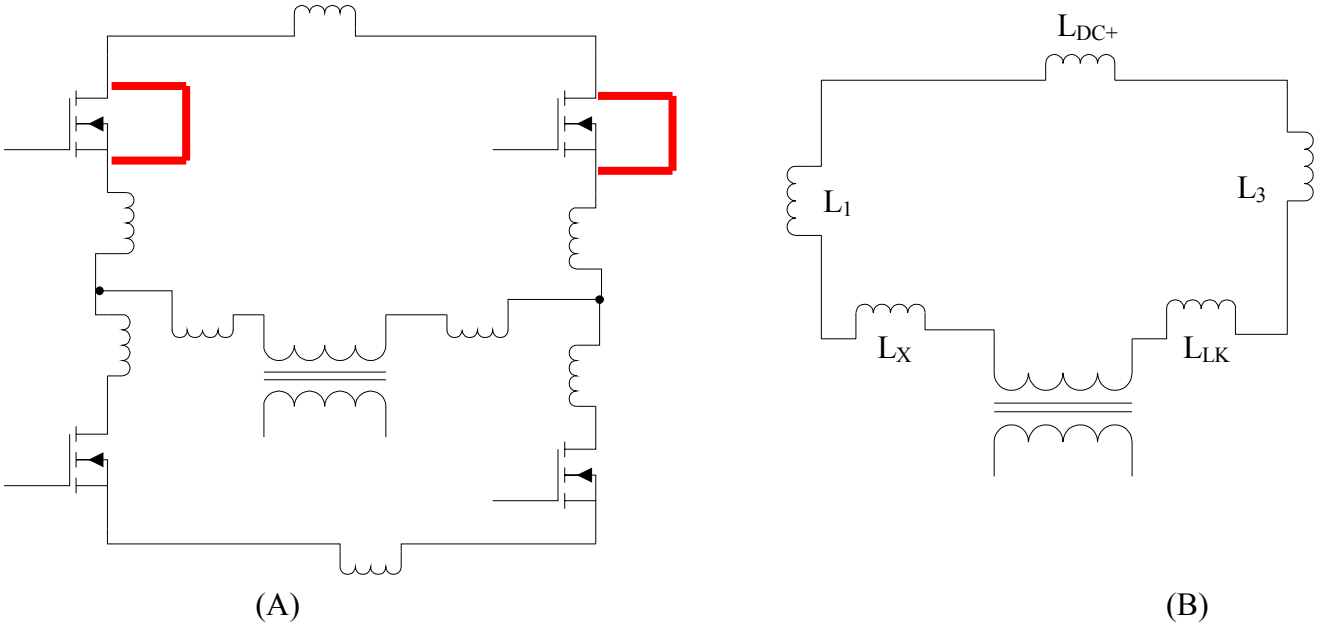


Figure 3-20. Measurement circuit 2

The final measurement was taken with all of the switches shorted. The reason for this measurement, is to obtain another equation that can be used to solve for the parasitic trace inductances. Figure 3-21 A shows the circuit configuration and Figure 3-21 B shows the equivalent inductance that was measured.

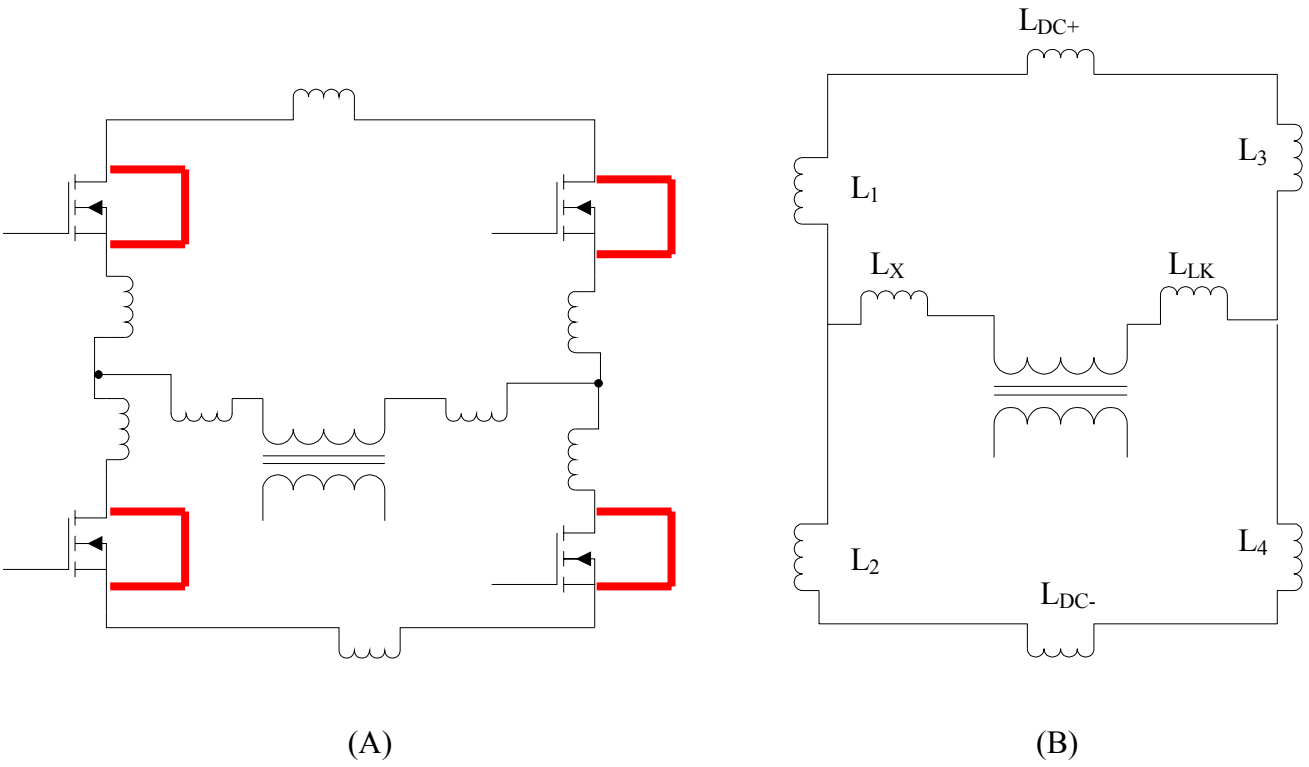


Figure 3-21. Equivalent circuit 3 for measuring the trace inductance

Table 3-4. Inductance measurements

Measurement Configuration	Measurement (µH)
1	26.9
2	25.5
3	16

The measurements shows that circuit configuration 1 and circuit configuration 2 show very similar inductance measurements. Both of which are much greater than the specification of 5

μH. However, circuit configuration 3 shows that the measured inductance is much lower than the other measurements.

3.6.3. Leakage Inductance derivation

Each measurement has a different combination of trace inductances that are found. From Table 3-3 it can been seen that the trace inductance for L_1, L_2, L_3, and L_4 are all very close to the same value. The only difference is a slight variation in length. If we assume that L_1, L_2, L_3, and L_4 are all equal (L) and that L_{DC-} and L_{DC+} are also equal (L_{DC}), a set of three equations with four unknowns can be found. Table 3-5 shows a list of the equations that are available. The problem with using this set of equations is that (25) and (26) are the same equation with two different answers. This is because L_1, L_2, L_3, and L_4 are not all the same and L_{DC-} and L_{DC+} are not exactly equal. Therefore the two different measurements are calculated to give two different answers. If we again make a lumped approximation by adding L, and L_{dc} together and L_{lk} and L_X together we can use equations (24) and (25) or (24) and (26) to solve for the parasitic trace inductance and the leakage inductance of the transformer. Knowing the value for each inductance is not relevant. However, it is useful to know how much of the inductance is created by the PCB traces and how much is from the transformer. Table 3-6 shows a summary of the leakage inductance and the trace inductance by using this method. Depending on which equations were used ((24) and (25) or (24) and (26)) the leakage inductance is varied by 0.9 μH and the trace inductance is varied by 1.8 μH. Referring to Table 3-3 $L_2 + L_4 + L_{DC-} = 21.7$ μH and $L_1 + L_4 + L_{DC+} = 21.8$ μH. The sums are equivalent to the trace inductance from Table 3-6. The theoretical calculations and the measurement results are very close and the small error can be a result from the measurement. Since the calculations for the trace inductance is very similar, the leakage inductance can be obtained by simply subtracted the value for L_X that was calculated in Table 3-3. The result for the leakage inductance of the transformer is then 1.46 μH – 2.36 μH. The calculated leakage inductance was 1.76 μH and the simulated leakage inductance was approximately 1.54-1.7 μH. The measured results are within the limits of the calculated results. The measured results still has a large variation and it is difficult to assign an exact number to the leakage inductance.

Table 3-5. Measurement equations

$(2L + L_{dc}) \| (2L + L_{dc}) + L_{lk} + L_X = 16\mu H$	(24)
$2L + L_{dc} + L_X + L_{LK} = 25.5\mu H$	(25)
$2L + L_{dc} + L_X + L_{LK} = 26.9\mu H$	(26)

Table 3-6. Inductances using different equations

Equations Used	**Trace Inductance (µH)**	**$L_{lk} + L_X$ (µH)**
(24) and (25)	20.4	5.1
(24) and (26)	22.2	4.2

If an interleaved winding structure is implemented, the leakage inductance can be greatly decreased while the efficiency of the transformer can be increased. According to the above observation the leakage inductance of the transformer is only a small portion of the inductance that is seen by the circuit. Most "conventionally defined" leakage inductance indeed come from "interconnect parasitic" but not transformer leakage. With the planar PCB layout, the transformer termination parasitic inductance is can be more than twice the leakage inductance, which is considered the maximum possible leakage by non-interleaving. Furthermore, the interconnect between devices, dc bus bars, and from devices to the transformer terminations can be one order of magnitude higher than the transformer leakage. Since the entire circuit interconnect sees much larger parasitic inductance, it may be worth designing the transformer with an interleaved structure to increase the efficiency while decreasing the temperature rise by better coupling between the primary and secondary of the transformer.

3.7. Circuit Simulation

3.7.1. Introduction

Physically measuring the leakage inductance has proven to be quite difficult. Since the transformer is integrated with the inverter, it is impossible to measure on the trace inductance and leakage inductance of the transformer directly. The impedance measurement proved that the leakage inductance was a combination of the leakage inductance of the transformer and parasitic inductances of the system. Since the leakage inductance is used for soft switching, it is important to figure out how the physical circuit will respond.

3.7.2. Theory

Many technical papers have been written on the leakage inductance effects with using a phase shifted full-bridge converter [28]. These papers discuss how the leakage inductance of the system affects the slope of the current. Figure 3-22 shows a schematic of the system that needs to be simulated. The phase shifted full bridge converter outputs a quasi-square wave signal. So instead of creating this converter, the simulation used a square wave input to the transformer. Figure 3-23 shows the switching waveforms for this system. During time interval T_1 the slope of the current will change proportionally with the input voltage and leakage inductance. The slope of the current will also be affected by any resistance that is in the system. As the resistance increases the slope will not be linear but exponential. For the simulation, zero resistance is assumed so a perfect linear relationship is achieved. This is not exactly the case for the physical circuit. The PCB traces will have a finite resistance and the slope will not be perfectly linear. However, the resistance will be very small and should not change the slope a large amount. During time interval T_2 the slope of the current will be affected by the leakage inductance and the filter inductance. Since the filter inductance is many orders of magnitude greater than the leakage inductance, it can be estimated that the slope is only affected by the filter inductance.

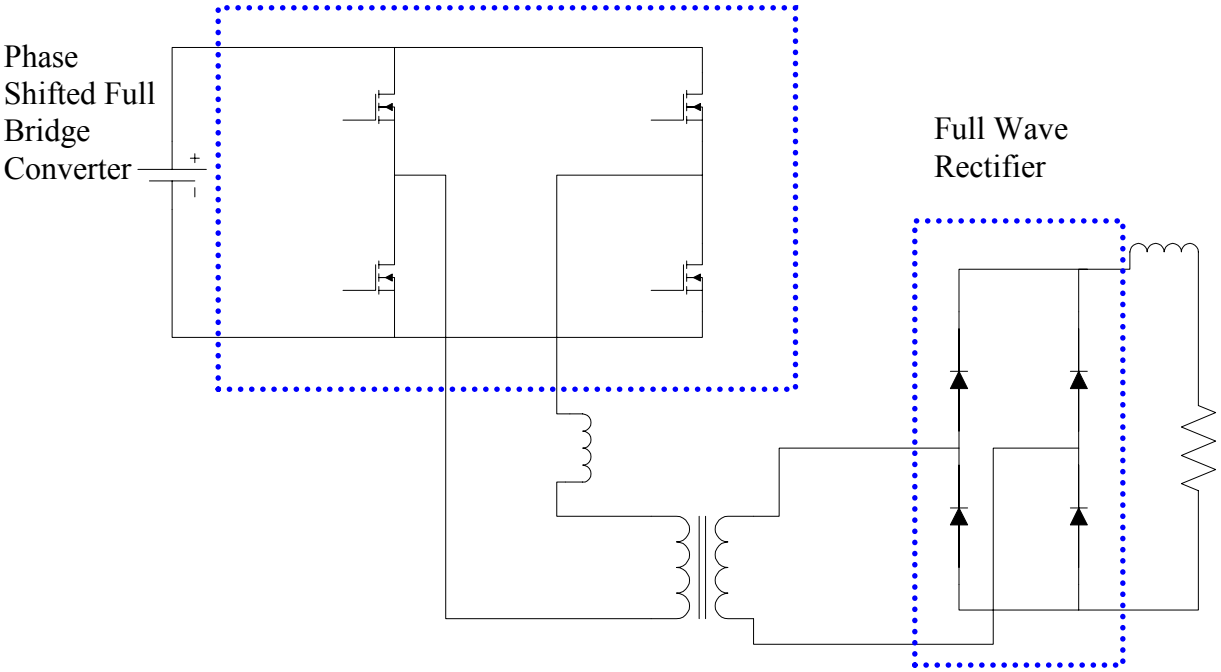


Figure 3-22. Simulation schematic

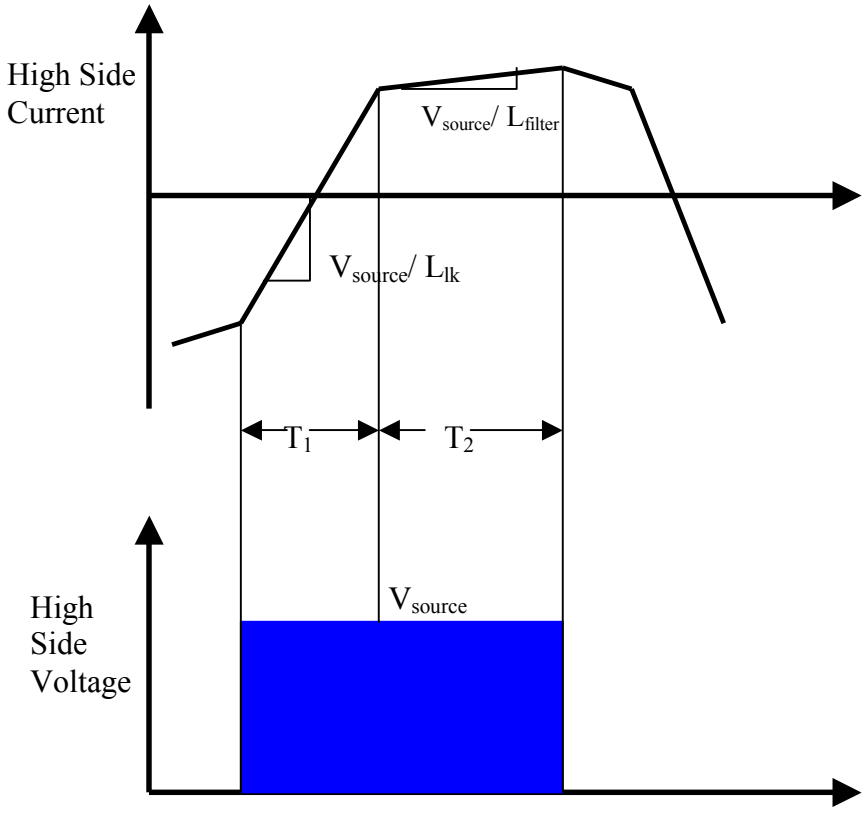


Figure 3-23. High side waveforms

From this simulation setup the transformer had to be accurately modeled. This was done by again using the finite element program, PEMag. This program can generate both a frequency domain and time domain model of the transformer. The model is created using the Saber™ MAST language. These models include all of the parasitic elements that the program calculates. This includes the leakage inductance, magnetizing inductance and the capacitances of the transformer. However, this is only for the transformer and does not include parasitic elements. Using the finite element model of the transformer and adding external trace inductances, the system can be accurately represented.

Figure 3-24 shows the Saber™ simulation schematic that was used. This schematic shows that the high side is connected in series and the low side is connected in parallel. The input waveform is a 100 kHz square wave with peak amplitude of 70 V. This is equivalent when the phase shifted full bridge has maximum duty cycle. A filter inductor was chosen to be arbitrarily 8μH. The filter inductor was to see the defining point between T_1 and T_2 in Figure 3-23. The rectifier is using the MBR2545 model. The voltage is drop is around 0.56 V when it is conducting. The figure shows two different transformer models. This is because PEMag can only represent symmetrical structures in both the X and Z directions. However, the transformer that was designed was not symmetrical in the X direction. One side had three turns and the other side had four turns. PEMag could not simulate this so to compensate, Transformer 1 was created with three turns on the top secondary and Transformer 2 was created with four turns on the top secondary. Doing this gave the net affect of the transformer system to equal to the one that was built.

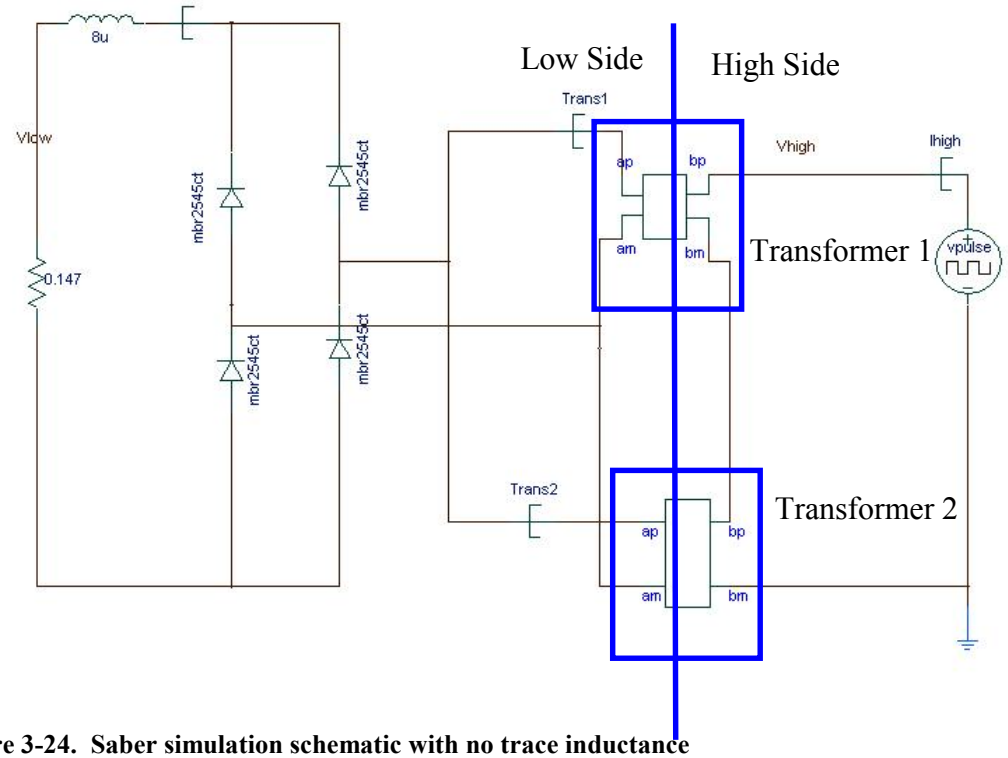


Figure 3-24. Saber simulation schematic with no trace inductance

Figure 3-25 shows the simulation results. The high side voltage is an ideal square wave with a 100 kHz frequency and a peak voltage of 70. The low side voltage is in phase with the high side but the level is decreased by the turns ratio. The low side voltage is 4.93 V. This shows that the turns ratio of 1:14 is achieved using the PEMag model. The current also matches the theoretical prediction shown in Figure 3-23. The current shows that two different slopes exist, the first one is a result of the leakage inductance and the second is a result of the filter inductance.

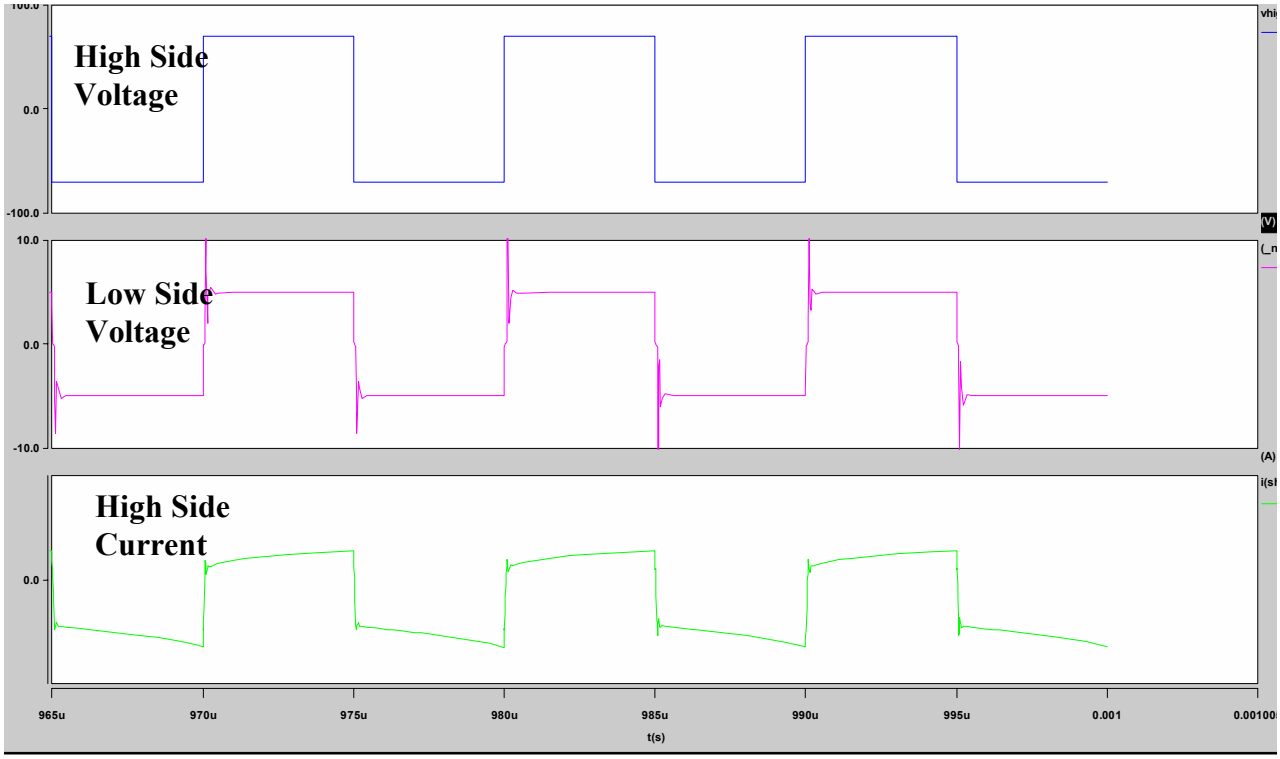


Figure 3-25. Saber simulation results with no trace inductance

Figure 3-26 shows the same waveforms as in Figure 3-25 but zoomed in further to see the slope of the high side current. The high side current in this simulation has a slope of 43.82×10^6 V/s. This is during the T_1 time from Figure 3-23. Using (27) the slope of the current is the voltage divided by the inductance. Since the major concern is the leakage inductance referring to the high side, the voltage is the high side voltage and the inductance will be referred to the high side. Using (27) the leakage inductance is 1.6 µH. Using the PEMag program the leakage inductance was found to be between 1.54 µH and 1.7 µH. This concludes that 1.6 µH is nearly in the middle of these values and that the slope can be used to determine the magnitude of the leakage inductance.

$$\frac{di}{dt} = \frac{V}{L} \qquad (27)$$

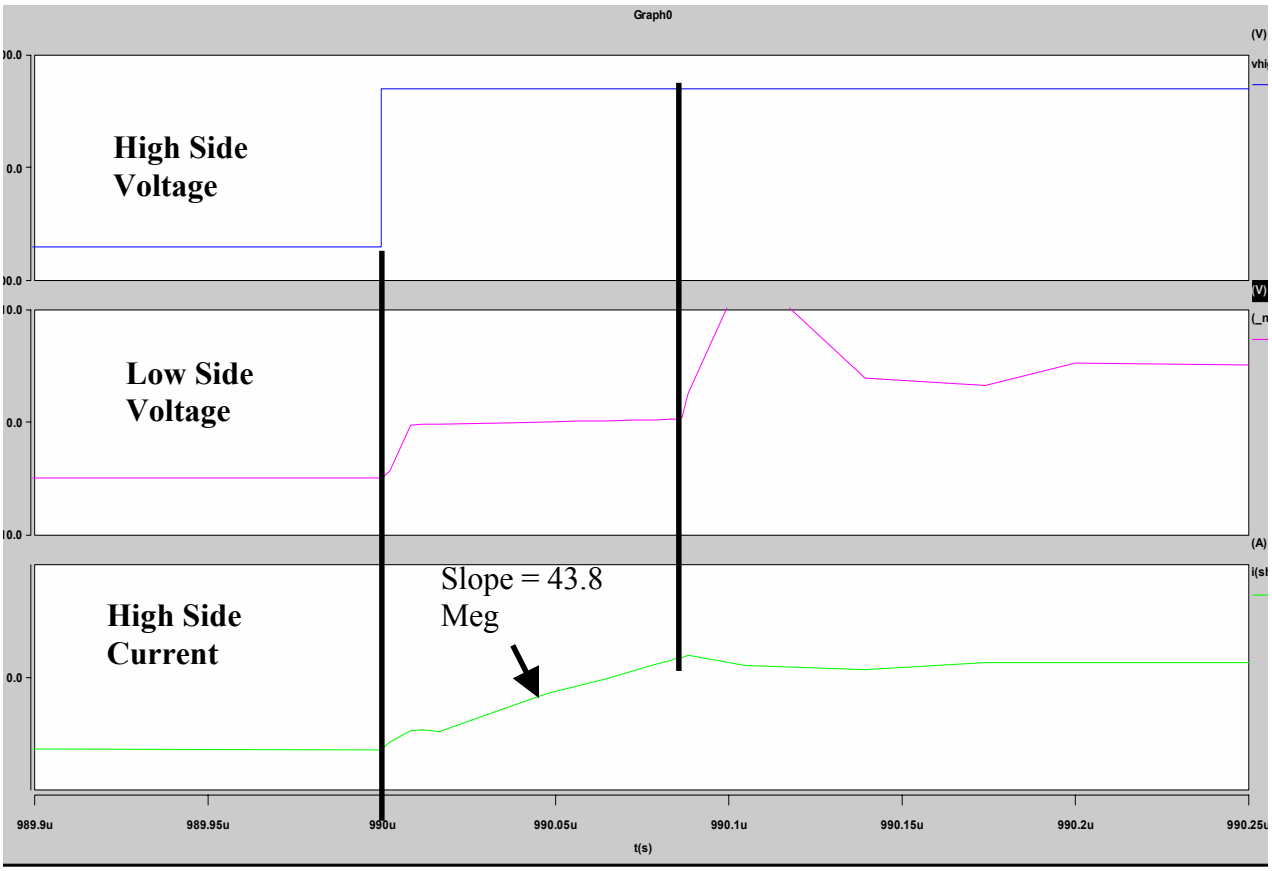


Figure 3-26. Saber simulation results with no trace inductance

If the parasitic inductances are added as a result of the trace inductances, the circuit would change to the one shown in Figure 3-27. The trace inductance values that are seen in the schematic are the same ones that were calculated using equation (23) and summarized in Table 3-3 . The result of this simulation is shown in Figure 3-29 and Figure 3-28. These simulation results show that the slope does change by adding the trace inductances in their proper places. The updated slope is 5.4105×10^6 V/s. Since the input voltage is 70 V the effective leakage inductance is calculated as 13 µH. This is below the measured result from the impedance analyzer but shows that the slope of the current does change as a result of adding trace inductance on the low side. During the time T_1 all of the diodes are shorted. The equivalent circuit is shown in Figure 3-21 and the impedance analyzer measurement was 16 µH for this situation. This difference is attributed to many different factors. One is that the turns ratio is not exactly 1:14, this is because of non-ideal coupling that exist in the transformer. Another is that the calculated trace inductances are probably not exactly the ones used for the simulations. The other factor is the current flow. The layout does not prove that the current will flow in the

middle to trace path. The trace inductances were calculated based on the current flowing the middle of the trace. All of these factors lead to the measurement not matching the simulation perfectly. However, the results are very close given the differences between the simulation and physical circuit.

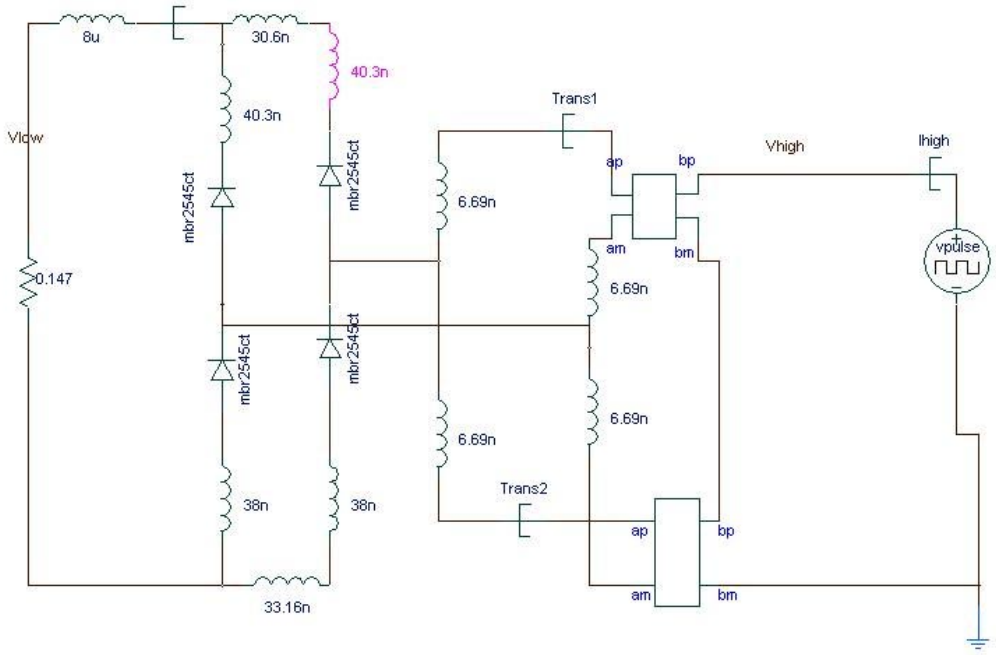


Figure 3-27. Saber schematic with trace inductance

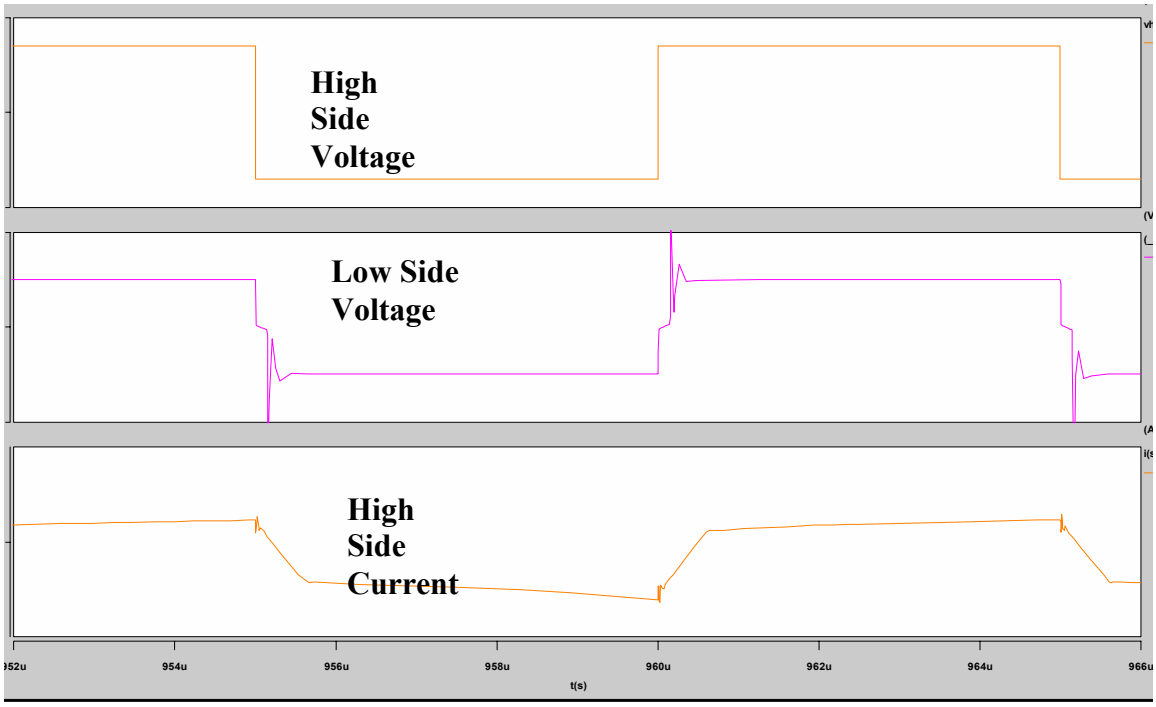


Figure 3-29. Saber results adding trace inductance

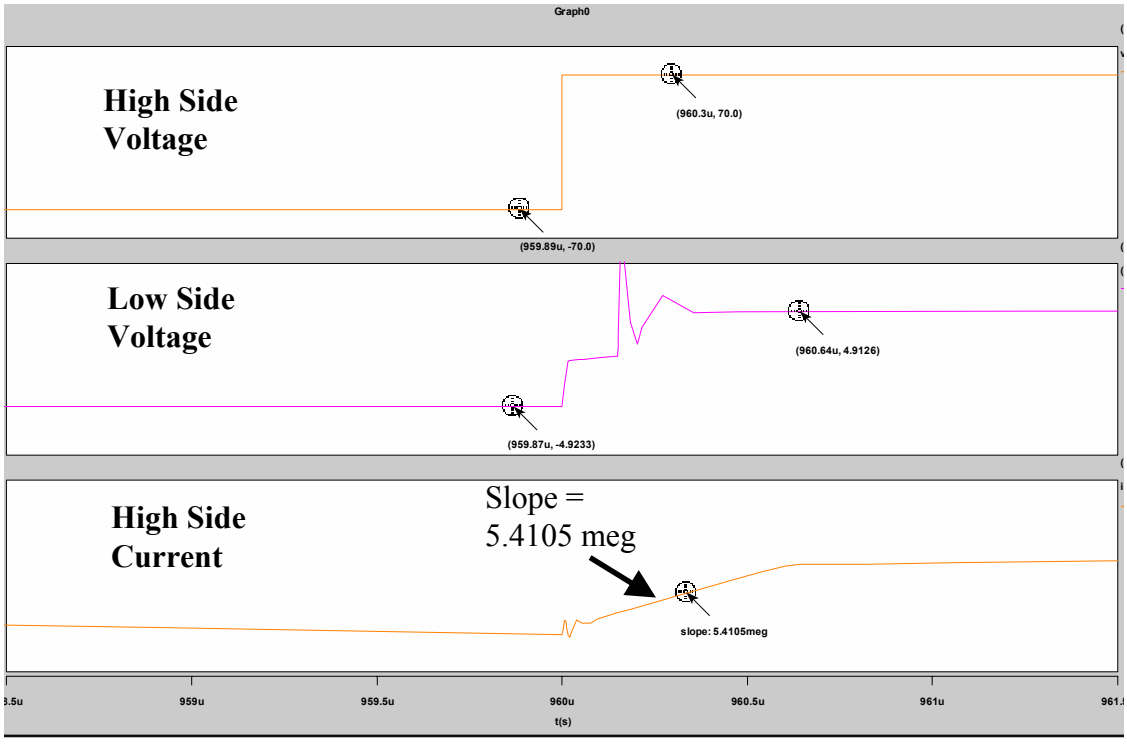


Figure 3-28. Saber simulation with trace inductance

3.7.3. Conclusion

The simulation results match very well with the theoretical prediction of the circuit operation. The simulation added insight into how the transformer system will operate in the physical circuit. Although the slope with the added trace inductances did not match the measurements taken from the impedance analyzer, they were relatively close.

3.8. Circuit Implementation

The same circuit that was used to simulate the effects of the leakage inductance was built. Figure 3-22 shows the circuit schematic. The diodes are the same that were in the simulation (MBR2545). The difference from the simulation to the circuit that was implemented was the use of a phase shifted full bridge converter. Figure 3-30 shows a picture of the measurement setup. The connection from the phase shifted front end to the transformer was made with a twisted pair of wires. This is because the twisted pair will reduce the inductance that is added to the system. The wire will add and extra inductance but it should be minimum compared to the leakage inductance. The phase shifted front-end is connected to the high side of the transformer system and the load and full wave rectifier is on the low side. This is the same situation that the Saber™ simulation used.

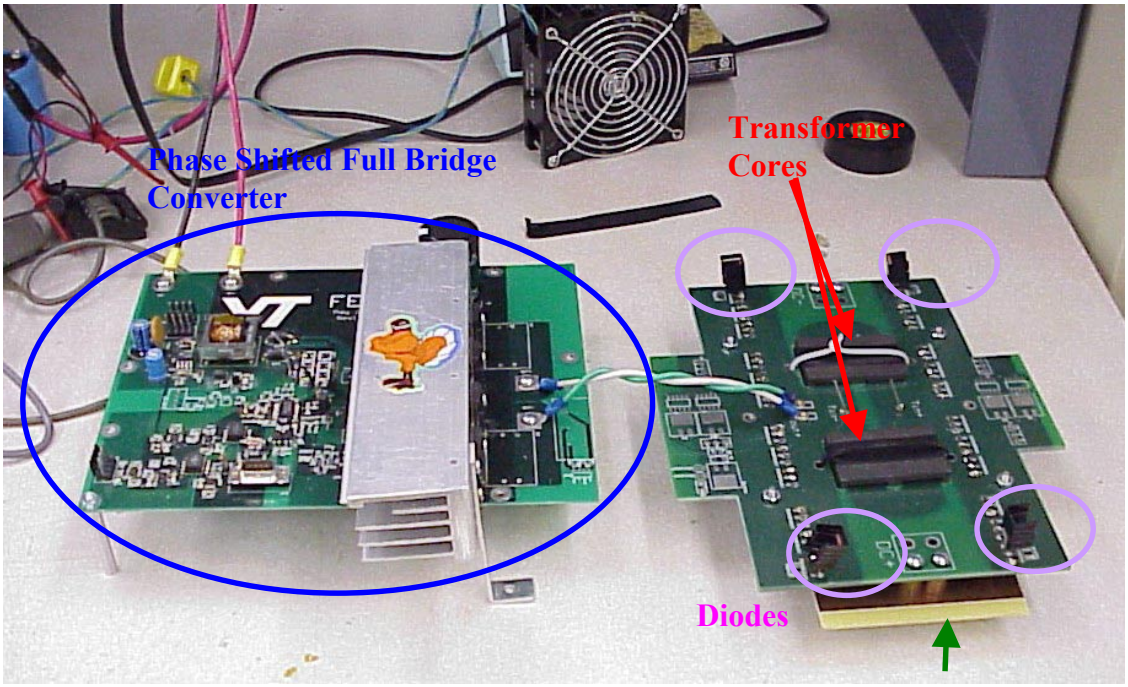


Figure 3-30. Measurement setup

Figure 3-31 shows the measurement from the oscilloscope. The input voltage is 52 V and the switching frequency is 100 kHz. The green waveform represents the input voltage measured directly across the high side of the transformer. The low side voltage shows that the voltage is approximately 3.6 V. The blue waveform is the high side current. The current shows that two distinct portions of the slope exist. The first is a result of the leakage inductance and the second is a result of the filter inductance. This slope can be measured to be 3.06×10^6. Since the input voltage is 52 V, equation (27) can be used to calculate the leakage inductance, and the results is 17µH. This number is slightly different from both the simulation results and the network analyzer. One of the reasons for this is the measurement noise. If different points were taken to find the slope, then the noise will vary the result. This variation will cause about 8% change in the slope or approximately a 1.4µH change in the leakage inductance calculation.

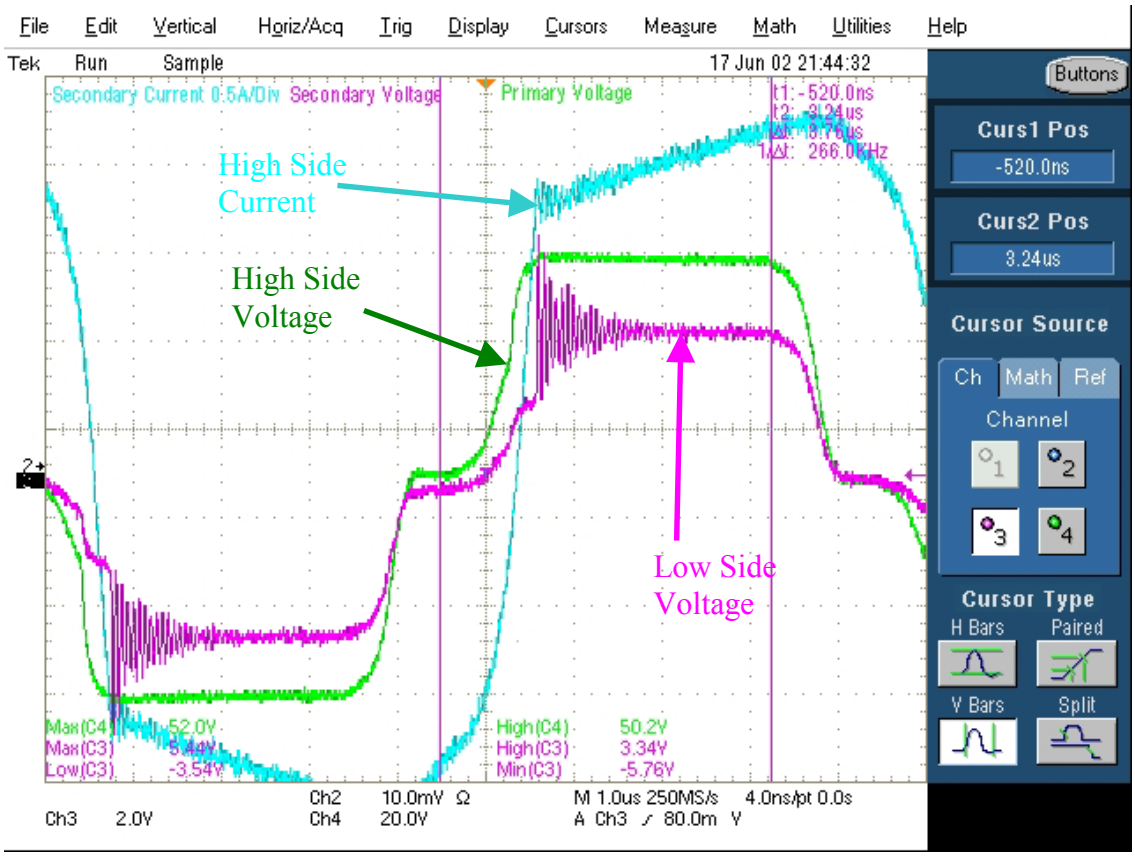


Figure 3-31. Measurement Waveforms

The next test was with decreasing the switching frequency to 89 kHz and increase the input voltage to 70 V. Reducing the frequency will allow the scope to take more data points with in a certain amount of time. The decrease in the switching frequency does not change the theory behind the measurement; it simply is trying to achieve a more accurate result. The higher voltage is to take multiple points and see the effect on the leakage inductance. Figure 3-32 shows the captured waveforms. The result is that the slope is 4.49×10^6. This leads to a leakage inductance of 15.6 µH. Once again the measurement has noise that will add error to the system.

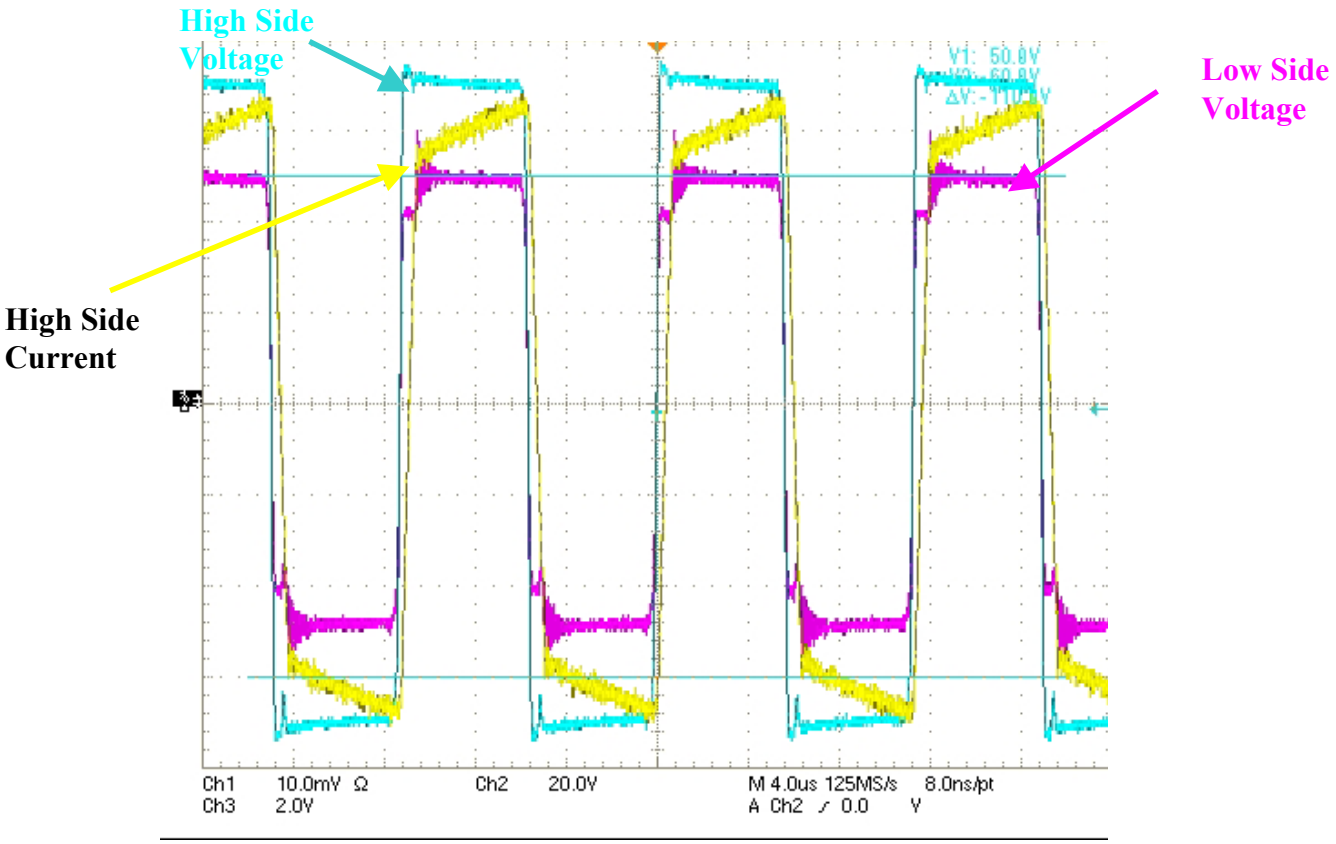


Figure 3-32. Measurement results for 89 kHz and 70 V input

To add another point to ensure that the leakage inductance measurement the switching frequency was decreased to 26 kHz and the input voltage was changed to 50 V. Figure 3-33 shows the measurement result. The slope is measured to be 3.26×10^6 V/s which results in a leakage inductance of 15.1 µH.

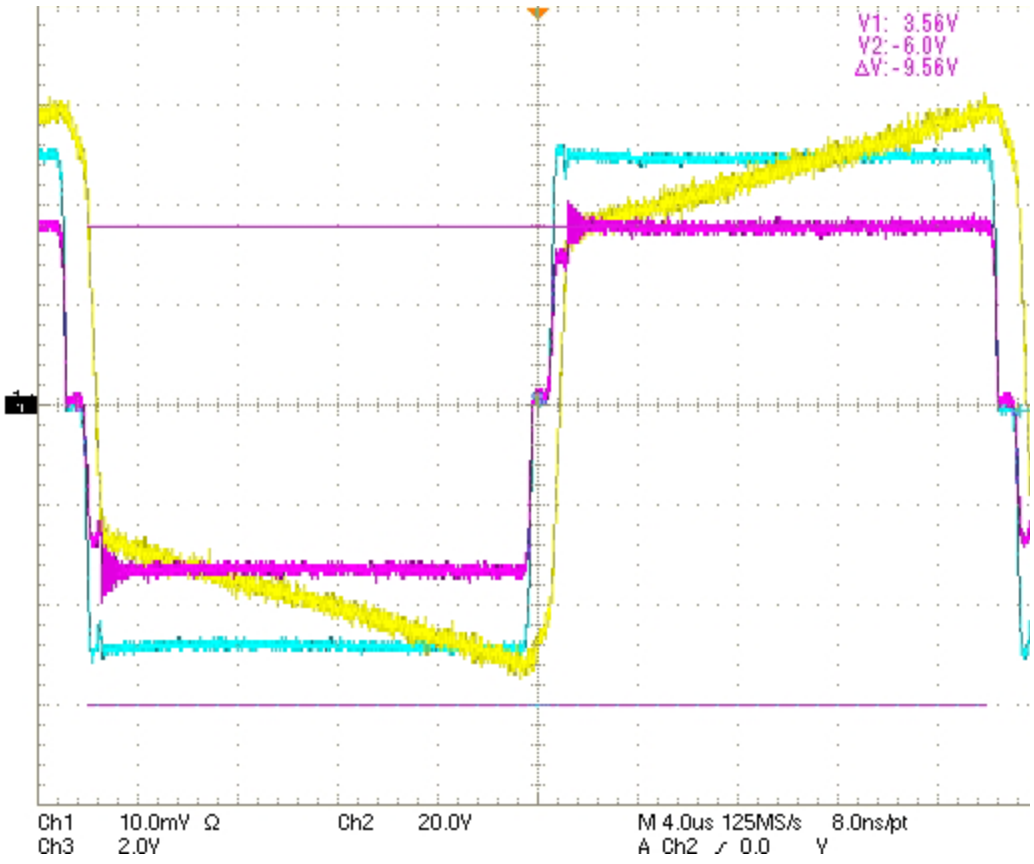


Figure 3-33. Measurement results for 26 kHz switching frequency and 50 V input

3.8.1. Conclusion

Table 3-7 shows the results and test conditions taken from the measurements. The maximum inductance is 17.6 µH and the minimum of 15.1 µH with a difference of 2.5 µH and an average of 16.2 µH. The results show that as the switching frequency increases, the noise becomes more significant and the measurement becomes more inaccurate. This is partially because the higher frequencies has more switching noise but also because the scope has a finite sampling frequency. Therefore as the frequency is decreased the scope is able to take more samples and get a more accurate result. The lower switching frequency has a more repeatable value around 15 µH.

Table 3-7. Measurement Results

Case	Input Voltage (V)	Switching Frequency (kHz)	Slope	Leakage Inductance (μ H)
1	52	100	$3.06x10^6$	17 μH
2	70	89	$4.49x10^6$	15.6 μH
3	50	89	$3.04x10^6$	16.5 μH
4	40	89	$2.27x10^6$	17.6 μH
5	60	26	$3.89x10^6$	15.4 μH
6	49.2	26	$3.26x10^6$	15.1 μH

3.9. Conclusion

The leakage inductance for the integrated structure is not easily measured. Since the turns ratio is 1:14 a very small trace inductance on the primary can become a significant inductance measured from the secondary. This is because the inductance on the primary is multiplied by the turns ratio squared (196). When this is considered the trace inductance, which is usually neglected, can become a significant portion of the measurement results. Since trace inductance is only a function of the geometry, and the layout has symmetry, and some of the inductances can be considered to be equal [8]. The structure is not perfectly symmetrical so this theory is not exactly correct. However, it will give accurate enough results for our purpose. Subtracting the trace inductance from the measurement results gives a relatively accurate result for the leakage inductance.

Chapter 4. Thermal Modeling

4.1. Introduction

The automotive environment requires that the ambient temperature of the system be 85 °C. This high temperature can cause many problems in the design stage. The ferrite material will change properties that affect the maximum flux density of the material. Also, the PCB design is also greatly affected by the thermal management. In the transformer design chapter, the PCB traces were designed according to an empirical formulas repeated in (28) and (29). In the transformer design chapter, I did not go into any derivation or proof of this formula. However, its accuracy is very important to the correct operation of the system. Since the glass transition temperature of the insulation material is relatively low, the PCB needs to have a well-designed heat distribution system.

$$CopperArea = \left(\frac{Irms}{k * t^{0.44}} \right)^{0.725} \quad (28)$$

$$TraceWidth = \frac{CopperArea}{CopperThickness} \quad (29)$$

k = 0.24 (internal layer)
k=0.48 (external layer)
t=30°C

4.2. Maxwell™ Modeling

Maxwell™ also has a program that can model the thermal properties of the system. Most engineers apply a one-dimensional model that is solely based on the thermal resistance of the system. Maxwell™, however uses a two dimensional model that not only determines the heat flow vertically but also determines the heat flow horizontally. The two-dimensional calculation will give much more accurate and realistic results. Again this thermal calculation is using finite element analysis and the mesh is very critical in achieving an accurate result. Figure 4-1 shows the mesh that was used for the finite element calculations. The mesh was made to give the minimum possible simulation time with the minimum error. For this simulation the mesh was refined around the PCB and core area.

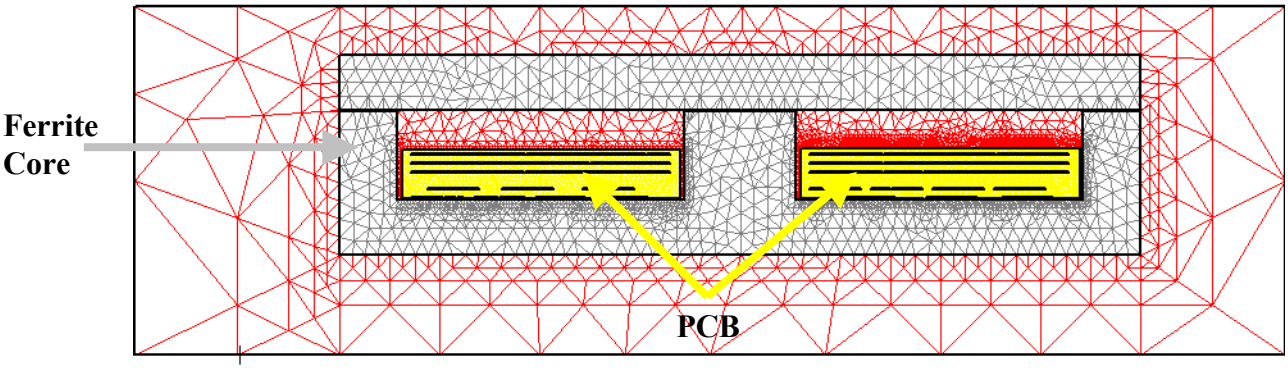


Figure 4-1. Mesh used for thermal analysis

The difficult part of using Maxwell™ for the thermal modeling is that the power losses of the PCB traces have to be found. These losses can be found by using the PEMag program that was explained in the Parasitic and Leakage Inductance chapter. In this chapter the resistance of the primary layers is 1.31 mΩ at 100 kHz. The secondary has a resistance of 141.91 mΩ at 100 kHz. These resistances reflect the case with 2 oz copper on every layer and 40 mils of spacing between the primary and secondary layers. If 50 Arms is used the power loss is 3.3 W for the primary and 7.24 W for the secondary. Table 4-1 summarizes the parameters used. The problem with this approach is that the resistance is assumed to be equally distributed among the three primary layers and current shares evenly among these layers. This is not the exact case because current will not evenly distribute between the three layers. Although this is not completely accurate it was proven in the Parasitic and Leakage inductance chapter that the current distribution is nearly equal at the 100 kHz switching frequency.

Table 4-1. 2 oz copper parameters

	Resistance (mΩ)	Current	Power Loss (W)
Primary	1.31	50 A	3.3 W
Secondary	141.91	7.14 A	7.24 W

Figure 4-2 shows the temperature distribution for the given simulation. The peak temperature of the system is 117 °C, and the ambient temperature is 85 °C. This gives a temperature change of 32 °C. The highest temperature of the system is near the center of the PCB as shown in Figure 4-3. This is because the insulation material has a relatively low thermal conductivity parameter. For the FR4 in this simulation the thermal conductivity is 0.27 W/m/K. This is much lower than the copper, which has 400 W/m/K thermal conductivity, and the 3C90 ferrite has 5.5 W/m/K thermal conductivity. This implies that the heat will not be able to escape from the inner layers of the PCB because it encounters more of the FR4 insulation material.

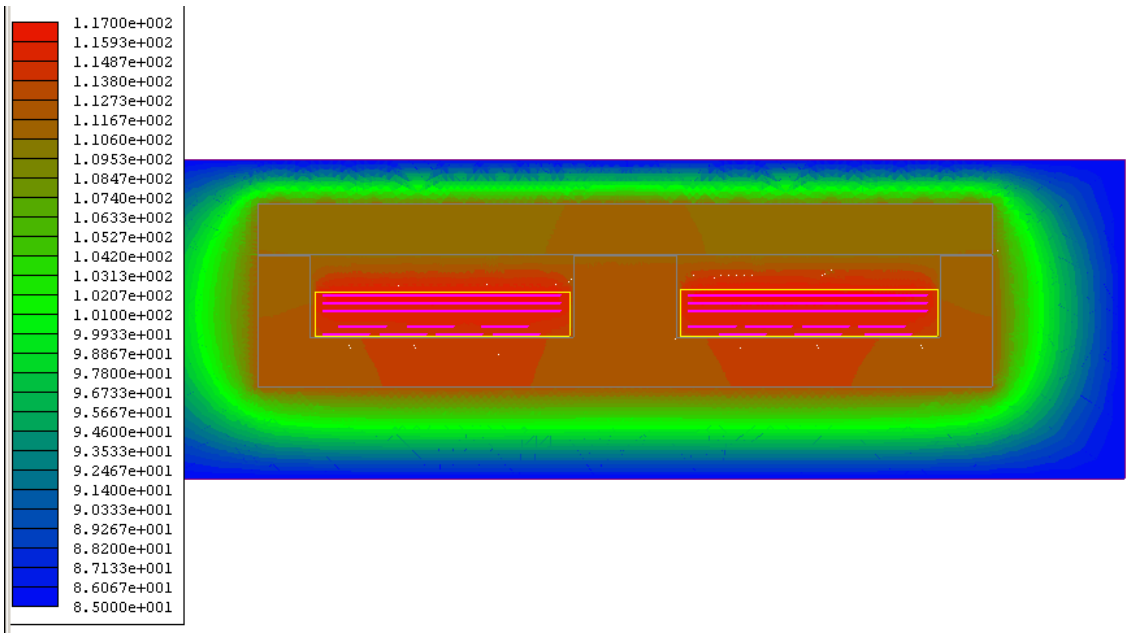


Figure 4-2. Temperature distribution

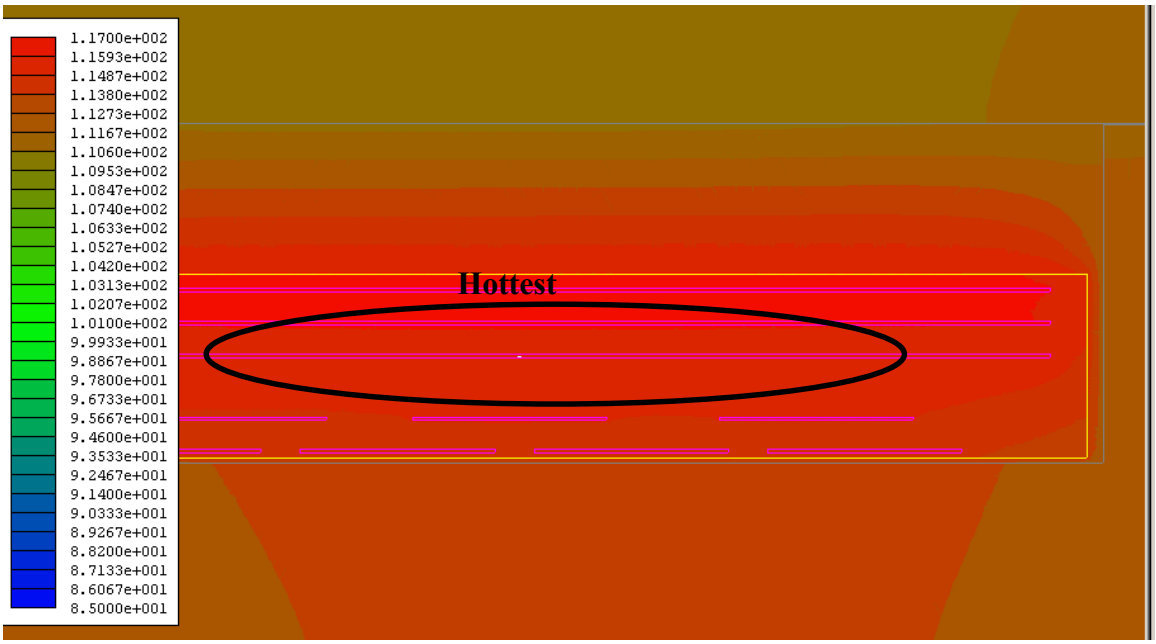


Figure 4-3. Temperature of PCB area

Figure 4-3 shows that the hottest area is closer to the top of the PCB than the bottom. This is because of the position of the PCB in the ferrite core window. For this simulation the PCB was placed near the bottom of the ferrite core. This means that the heat can travel through the ferrite core, which has a higher thermal conductivity than air. If the PCB was moved upward the hottest area would move downward. However, in the final mounting scheme the PCB will be firmly placed against the bottom of the ferrite core, and Figure 4-3 should give an accurate representation of the system.

If equations (28) and (29) are used, 2 oz copper will have a 30 °C temperature rise with 50 Arms on the input. This proves that the finite element analysis and the empirical formula match very well.

Another important aspect of this thermal modeling is the temperature gradient. This is the magnitude that the temperature changes from part to part. The higher the temperature gradient, the higher the difference in the temperatures for the different sections. Figure 4-4 shows a figure that shows the magnitude of the temperature gradient.

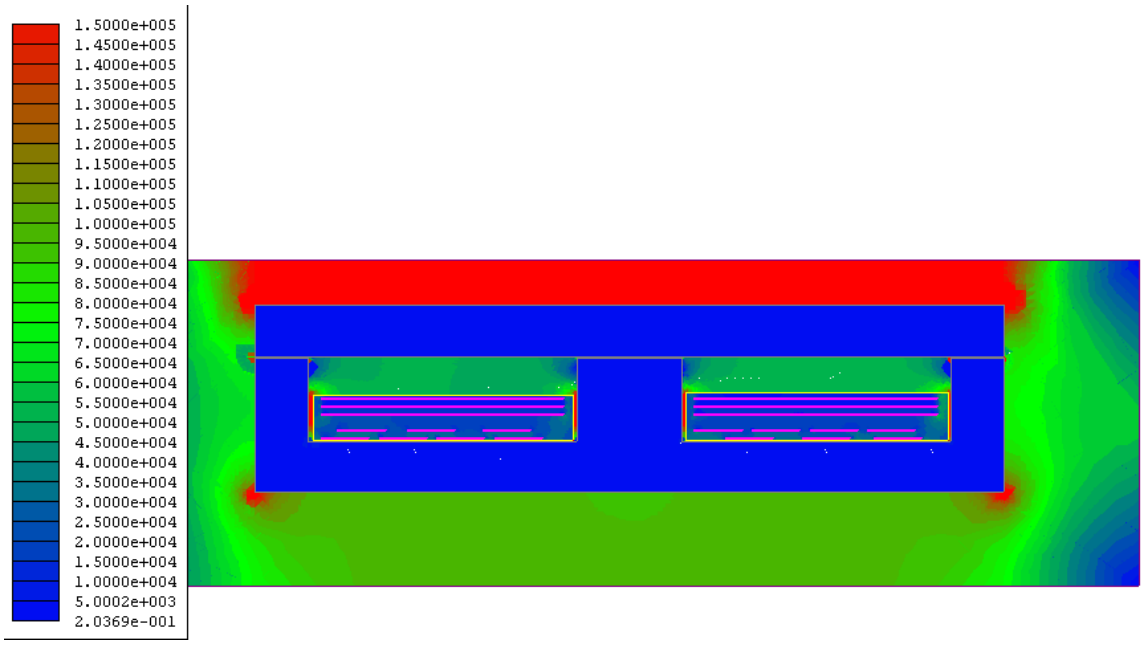


Figure 4-4. Temperature gradient

The temperature gradient shows that the temperature of the core and the insulation is evenly distributed. However, the interfaces with the insulation to the air or the core to air have a high temperature difference. This again is because of the differences in thermal conductivity.

Since the final PCB will be made of 6 oz copper, another simulation was run using the updated parameters. Table 4-2 shows the AC resistances found from PEMag at 100 kHz.

Table 4-2. 6oz copper parameters

	Resistance (mΩ)	**Current (A)**	**Power Loss (W)**
Primary	0.75	109	8.9
Secondary	59.64	15.57	3.6

Figure 4-5 shows the temperature for different sections of the transformer system. Once again the two-dimensional simulation results match the empirical formula very well. The calculation shows a 30 °C temperature rise, and the simulation shows a 34 °C temperature rise. Figure 4-6 shows the hottest portion of PCB is near the top.

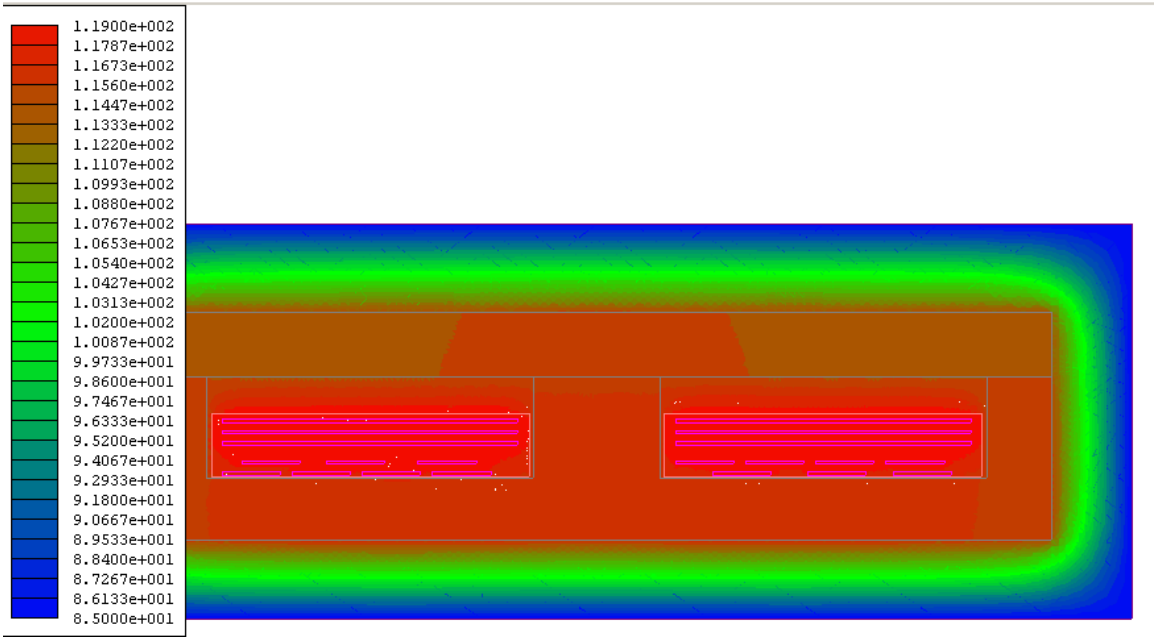


Figure 4-5. Temperature distribution for 6 oz copper

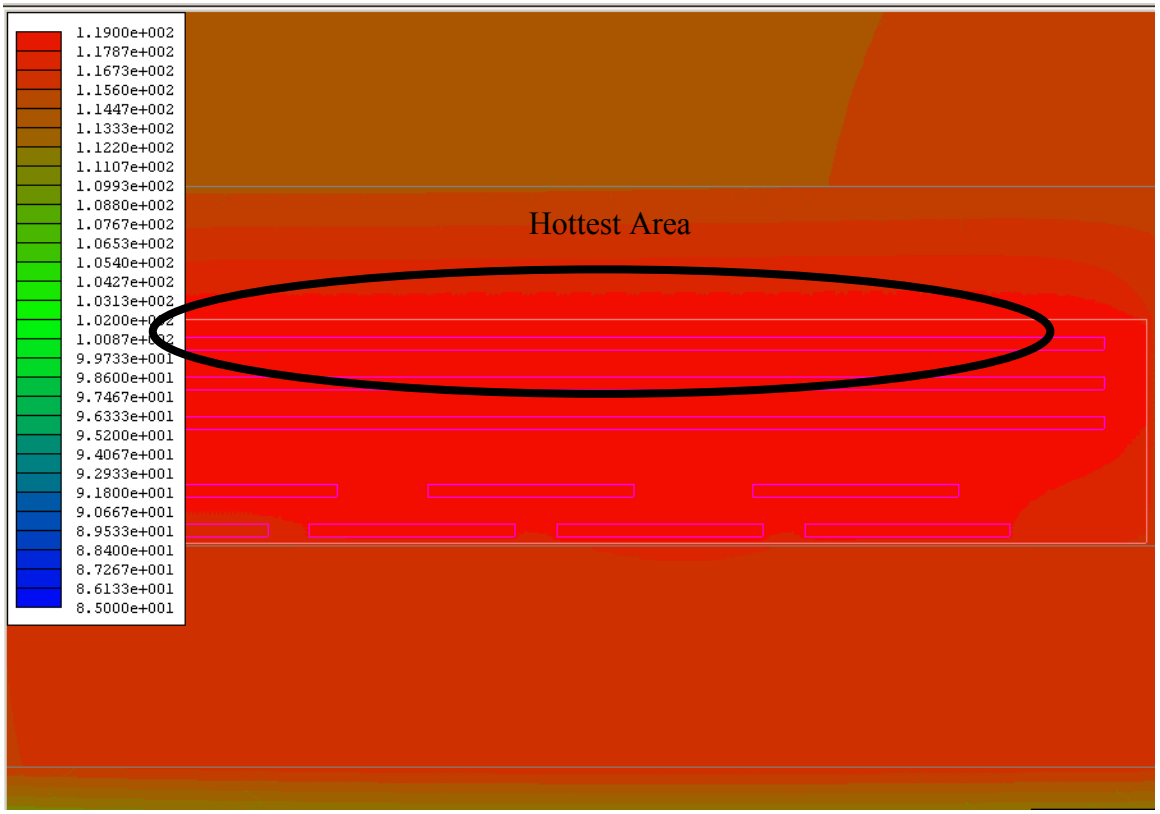


Figure 4-6. Temperature of PCB area

4.3. Conclusion

For both the 2oz and 6 oz copper case the empirical formula that was used to determine the PCB trace widths and copper weight match very well to the two-dimensional finite element approach. All of the above simulations are for simple air convection cooling. The air temperature for the simulations is kept at 85 °C. In the final system the transformer core will be mounted on a cooling plate that is kept at 85 °C. This will provide additional cooling for the core. This additional cooling will drop the PCB temperature within the limits specified for the transformer and inductor system.

Chapter 5. Inductor Design

5.1. Introduction

The planar inductor was originally going to be integrated into the same PCB as the transformer and inverter. This did not prove to be feasible after the preliminary design calculations. According to calculation, a high number of layers were needed to achieve the desired inductance. This implies that the inductance of each layer must be high, and thus a large core and its associated PCB core area is needed. Table 5-1 summarizes the design specifications for the inductor. This inductor slightly deviates from the traditional inductor design because it has a coupled winding. The secondary winding is used for startup during boost mode operation. In boost mode the output must be greater than the input. This means that the coupled winding will only need to be used for the first one minute, during startup. The planar inductor design is much like the traditional inductor design. The only differences are from the temperature rise calculations. Again the number of turns should be minimized to make the planar inductor cost effective.

Table 5-1. Planar inductor specifications

Inductance	1.5 μH @100 kHz switching frequency
Current	150 A continuous 350 A with a 50% load cycle
Peak Current	400 A
Turns ratio	1:14
Galvanic isolation	1800 Vac for 1 minute
Core temperature rise	15°C
Winding temperature rise	20°C

5.2. Core selection

The core selection is based on two properties of the inductor. The first is that the window width is wide enough to fit the copper area required to carry the current. The second requirement is that the core has enough cross sectional area so that the ferrite will not saturate during the worst-case operation. Two different cores seem to give reasonable results for this implementation. The first is the EE58 core made by Philips and the second is the EE64 core also made by Philips.

5.2.1. Winding Configuration

Although the transformer used an EI58 core, the EI configuration was not feasible for the inductor design because the number of layers required, exceeds the window height in the EI configuration. With the high current requirement of the inductor, two different winding configurations were looked at. The first winding method has the cores stacked in series. Figure 5-1 shows a representation of this method. The advantage of using this method is that the core area could be multiplied by the number of cores, and the inductance for the calculation would not change. The disadvantage of this configuration is that the window width has to have enough copper to carry the current of the inductor. This implies that many PCB layers would be placed in parallel to carry the required amount of current.

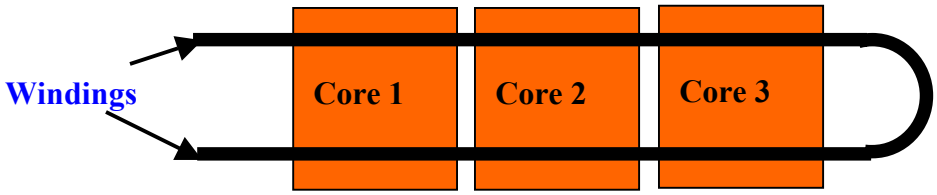


Figure 5-1. Series core configuration

The second winding method is to have the cores in parallel. The advantage of this method is that the current will be split between the cores; this will reduce the number of PCB layers that are placed in parallel. The disadvantage of this configuration is that it places inductors in parallel. Therefore each inductor must have a greater inductance. Figure 5-2 shows a representation of this method. Each core can represent a separate inductor.

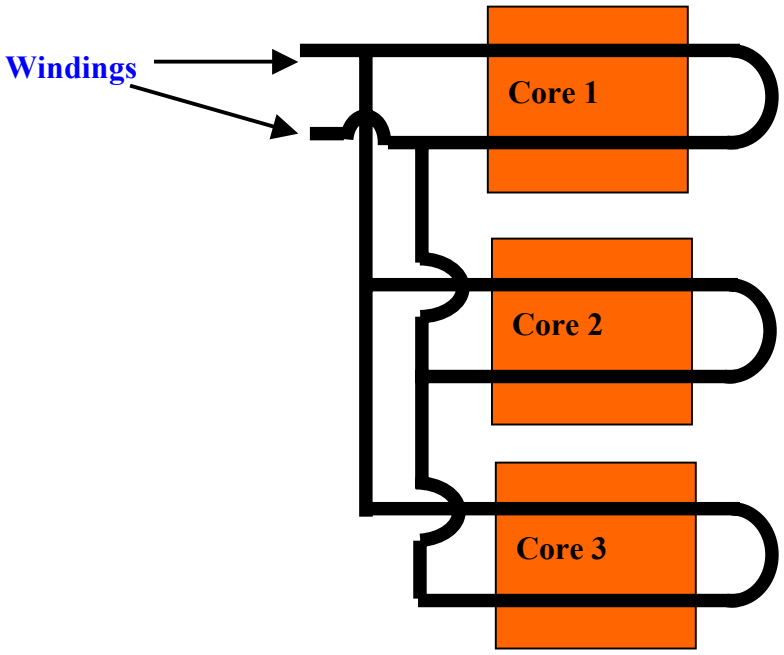


Figure 5-2. Parallel winding structure

Comparing the two different configurations and calculating the number of cores needed for both configurations, it was found that the number of cores required, were the same for both configurations. The series core configuration (Figure 5-1) will have a lower number of turns but the number of PCB layers in parallel is high. For the parallel configuration (Figure 5-2) the number of turns is higher but the number of PCB layers in parallel will be reduced. Given that both have advantages and disadvantages from the electrical standpoint, manufacturing of both configurations was looked at. For the series core configuration to work properly all of the cores have to be placed in series with no gap between the core stacks to avoid fringing effects. This is because the core should be viewed as one core, so that the cross sectional area can be multiplied by the number of cores in the system. Should this be done, the mounting of the cores can be quite difficult, because each core must be clamped to one another horizontally and then the core halves have to be clamped vertically. This mounting can be very difficult and problematic during vibrations. The parallel configuration is proven to be a better alternative from a mounting and electrical perspective. From this point on, the planar inductor winding configuration is assumed to be the parallel method shown in Figure 5-2.

5.3. EE58 Core

5.3.1. Turns

The EE58 core made by Philips has a 0.824in window opening, thus the maximum trace width for this window is 0.76 in., given manufacturing tolerances. If two cores are used then the inductance of each core must be 3.0 μH, and the peak current needs to be divided by two, if the current is assumed to split evenly between the two cores. To find the parameters for this configuration the gap length and the number of turns has to be calculated. Equation (30) shows the formula for the number of turns needed to achieve the inductance [6]. Given in Table 5-1 the peak current is limited to 400 A, if two cores are used this is reduced to 200 A, the inductance is 3.0 μH, the peak allowable flux density is 0.25 T, the core window area is 3.08 cm^2. Using (30) the number of turns is 7.8. Since this must be a whole number it is rounded to 8.

$$N = \frac{LI_{\max}}{B_{\max} A_C} 10^4 \qquad (30)$$

I_{max} = peak current (A)
L=desired inductance (H)
B_{max} = maximum allowed flux density (T)
A_C= core window area (cm^2)

Next, the gap length must be calculated. The equation for the gap length is shown in (31) [6]. Using the numbers for two EE58 cores the gap length is 7.8 mm. This is a significant portion of the center leg for the EE58 core. Philips offers standard gap length cores but the maximum gap length offered is 1.4 mm. Figure 5-4 shows the dimensions for the EE58 core. The center leg length is only 6.5 mm long. In an EE configuration the total leg length is only 13 mm, which makes the gap 60% of the total center leg length. Having this large of a gap length will cause the flux to fringe around the air gap. Figure 5-3 shows that as the flux fringes, it starts it does not take up the same area as the cross sectional area of the core.

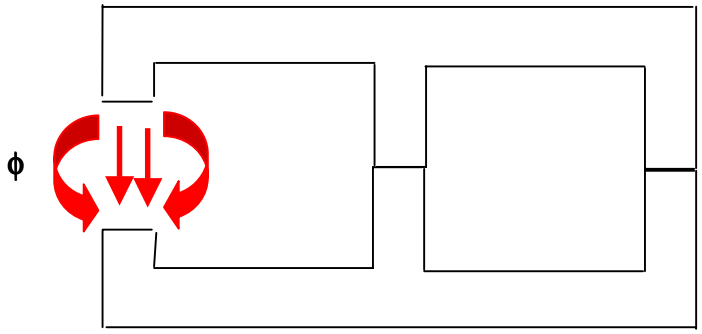


Figure 5-3. Flux fringing

$$\mathrm{lg} = \frac{\mu_0 L I_{\max}^2}{B_{\max}^2 A_C} 10^4 \ (\mathrm{m}) \qquad (31)$$

μ_0 = permeability of air (H/m)
L=inductance (H)
I_{max} = peak current (A)
B_{max} = peak flux density (T)
A_C = core window area (cm^2)

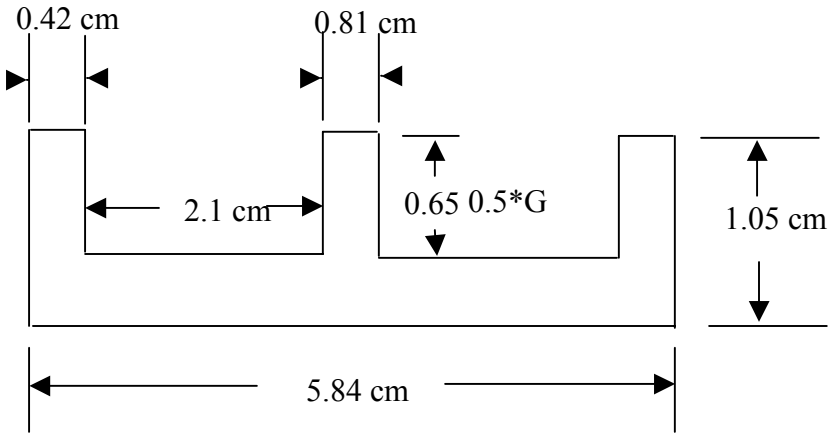


Figure 5-4. Philips E58 core

The above calculations assume that the fringing can be neglected; in this case the fringing cannot be ignored. To correct for this, the turns ratio must be recalculated to factor that the flux does not have the same cross sectional area as the core. Equation (32) shows the formula for the fringing flux [16]. Using the numbers for the EE58 core the fringing flux is 1.535. Using (

33) the corrected number of turns is 6.3 which must be rounded up to 7. The fringing flux decreased the number of turns by one from the original calculation.

$$F = 1 + \frac{l_g}{\sqrt{A_c}} \ln\left(\frac{2G}{l_g}\right) \qquad (32)$$

A_C = core window area (cm^2)
l_g = gap length (cm)
G = leg length (cm) see Figure 5-4

$$N_C = \frac{N}{\sqrt{F}} \qquad (33)$$

N= original turns calculation (from (30))
F= fringing flux

5.3.2. Copper Weight

The copper weight was found in exactly the same way as the transformer. Using the same equations, the copper weight needs to be 13 oz and 0.760 in width to have a 36°C temperature rise. This assumes that the inductor only has one turn per layer. Since the secondary only has to carry the current for a short period of time, the secondary windings can be made from 6 oz. copper. The skin effect is not as much of a concern with the inductor as it was with the transformer. This is because the inductor carries a DC current with a ripple. This means that a large percentage of the current is actually DC and not at a higher frequency. For this reason the copper weight can be greater than 6 oz, and still utilize all of the copper area. To find the width of the secondary the only consideration was if the windings could fit into the core. If 0.025 in is allowed between the traces, the width of each trace is 0.041 in. The secondary will make up 4 layers total and the primary will take 7 layers total (one turn per layer). The total layer count for the inductor using an EE58 core will be 11 layers.

5.4. EE64 Core

5.4.1. Turns

The EE64 core made by Philips offers another option for the inductor design. The method for calculating the turns and air gap is the exact same as for the EE58. The only difference is the core dimensions. Figure 5-5 shows the dimensions for the EE64 core. The advantage of using the EE64, is that it has a wider window opening and larger cross sectional area. If again two cores are used, the number of turns is 4.62. Rounding this up gives a total of 5 turns. Using (31) the gap length is 0.46 cm. This again is very large compared to the length of the center leg. The fringing effect cannot be ignored. Using equation (32), the fringing flux is 1.302 and using equation (33), the corrected number of turns is 4.053. The corrected number of turns is very close to 4, if 4 turns are used, the calculated inductance is lower than the requirement of 1.5 μH. If 5 turns is used the inductance will be greater than the 1.5 μH specification. Using four turns has the benefit of being able to eliminate a layer from the PCB and all of the vias associated with that layer. In addition, the PCB interconnect parasitic may contribute additional inductance that makes the total inductance to be equal to larger than 1.5 μH with 4 turns.. Table 5-2 shows a summary of the core choices.

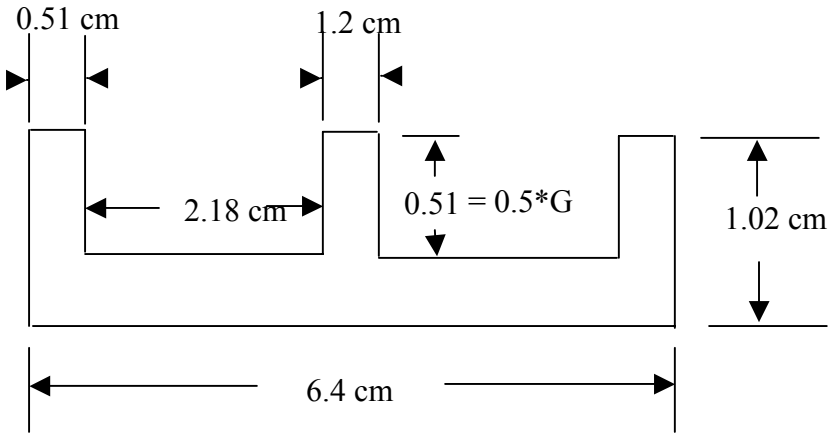


Figure 5-5. E64 Core

5.4.2. Copper Weight

The copper weight was computed the same way as for the EE58 core and transformer. Using these equations the copper weight should be 13 oz for the primary layers. This assumes a 34°C temperature rise. This is the same copper weight that can be used for the EE58 core with only a slightly lower temperature rise. Again, the secondary was only based on the number of windings that could fit into the window width and not on the temperature rise. If the primary is 5 turns then the secondary must be 70 turns. The width is 0.022 in with 0.025 in. space between each secondary trace. This will make the secondary of the inductor on two layers and the secondary of the two inductors in series. If only 4 turns are used for the primary then the secondary must have 56 turns. This makes the width of the trace 0.034 in with 0.025 in between each trace. For either case the secondary can be 6 oz. Copper, since it will only operate for a short period of time. Table 5-2 shows the summary of the core comparisons.

Table 5-2. Core summary

	EE58	EE64	EE64
Turns	7	4	5
Gap Length (mm)	7.8	4.6	4.6
% of total leg	60%	45%	45%
#Layers	11	6	7
Width of secondary trace (in)	0.041	0.034	0.022
Primary Copper weight (oz)	13	13	13
Temperature Rise Primary (°C)	36	34	34

5.5. Air Gap solutions

Since the air gap is very large, a couple of alternatives are proposed. First, the air gap can be distributed over all three legs of the transformer instead of just the center leg. This will

decrease the gap in each leg by 1/3. This method offers the benefit of not needing a custom cut core with the required gap length. Instead a transformer core (no air gap) can be used and a gap material can be placed between each of the legs of the transformer. The disadvantage of this is that the height of the core will be increased and the PCB will not fill as much of the window opening in the core.

Another alternative is adding a material in the gap that is slightly magnetic. The advantage of this is that the fringing can be reduced because the flux will have less resistance in a magnetic material than in a non-magnetic material. The problem is that the gap must be recalculated to accommodate for the new material. The first step is to find the effective permeability of the system. Using (34) the effective permeability of the core and gap system can be found as a function of the gap length. Figure 5-6 shows a graph of how the effective permeability changes with the gap length. This calculation was done using the relative permeability of 3C90 material being 1820, which is given in the datasheet. The relative permeability of the gap material is 9. The magnetic path length for the EE64 core is 80 mm.

$$\mu_e = \frac{\mu_{rcore}\mu_{rgap}(l_m + l_g)}{l_g\mu_{rcore} + l_m\mu_{rgap}} \qquad (34)$$

μ_{rcore} = relative permeability of core material
μ_{rgap} = relative permeability of material in gap
l_g = gap length (m)
l_m = magnetic path length (m)

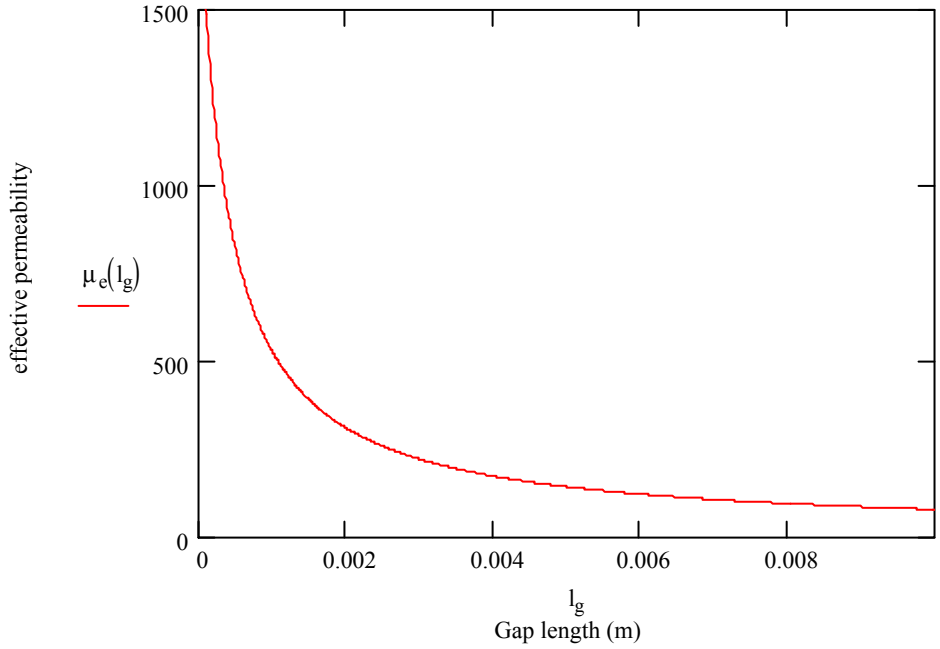


Figure 5-6. Effective permeability depending on gap length

The graph of the effective permeability shows that as the gap length gets large the effective permeability drops off very rapidly. From this the number of turns can be calculated. Equation (35) shows the formula used to calculate the number of turns. If the properties of the EE64 core are used the number of turns can be graphed as a function of the gap length. Figure 5-7 shows the result of this calculation. If the number of turns is kept the same, then the gap length will be 50 mm. This is much larger than the gap calculated for the case with no magnetic material added to the gap. The gap length is very close to the magnetic path length of the EE64 core. This may introduce substantial loss due to the filling material and reduce the utilization of the core.

$$N = \sqrt{\frac{Ll_m}{0.4\pi A_c \mu_e}} * 10^3 \qquad (35)$$

L= inductance (H)
l_m = magnetic path length (m)
A_c = core window area (m^2)
μ_e = effective permeability

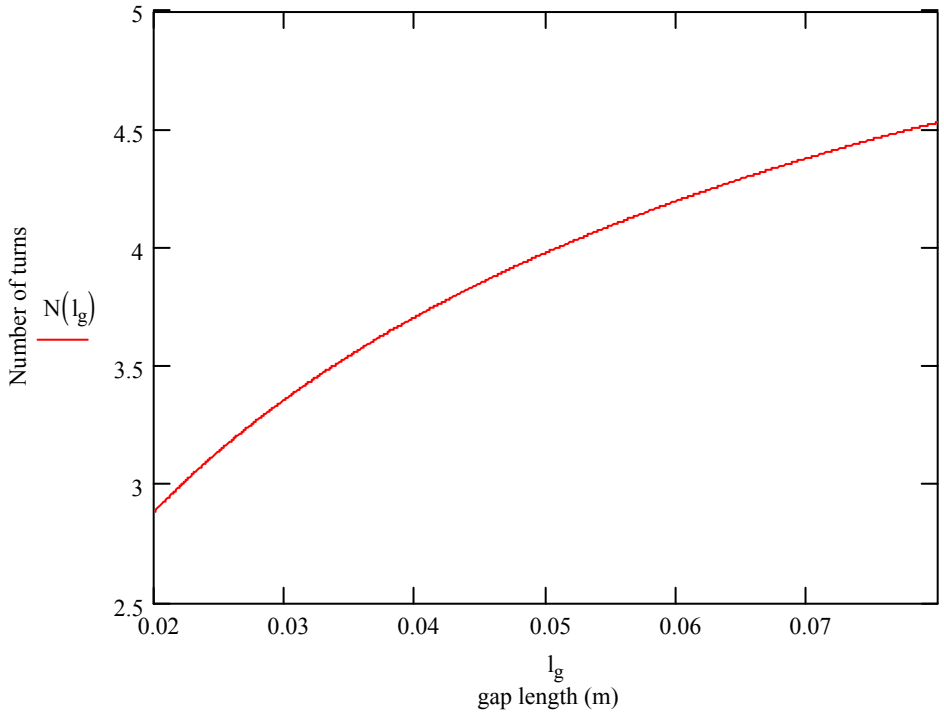


Figure 5-7. Number of turns versus gap length

Changing the gap material also affects the maximum flux density of the system. The previous calculations were for the relative permeability of the gap material being one. The relative permeability of the gap material must be considered. Equation (36) is very useful for finding the maximum flux density of the inductor. Since the effective permeability and the number of turns are dependent on the gap length, the maximum flux density is also a function of the gap length. Figure 5-8 shows a graph of how the maximum flux density changes with the gap length. Using the case with 4 turns the gap length is 50 mm, this makes the maximum flux density 2904 Gauss. This is greater than the set limit of 2500 Gauss. Although the flux density is greater than the limit, it is still within a reasonable limit and acceptable for normal operation.

$$B_{\max} = 0.4\pi \frac{\mu_e N I_{pk}}{l_m} (Gauss) \qquad (36)$$

μ_e = effective permeability
N=number of turns
I_{pk} = peak inductor current
l_m = magnetic path length (cm)

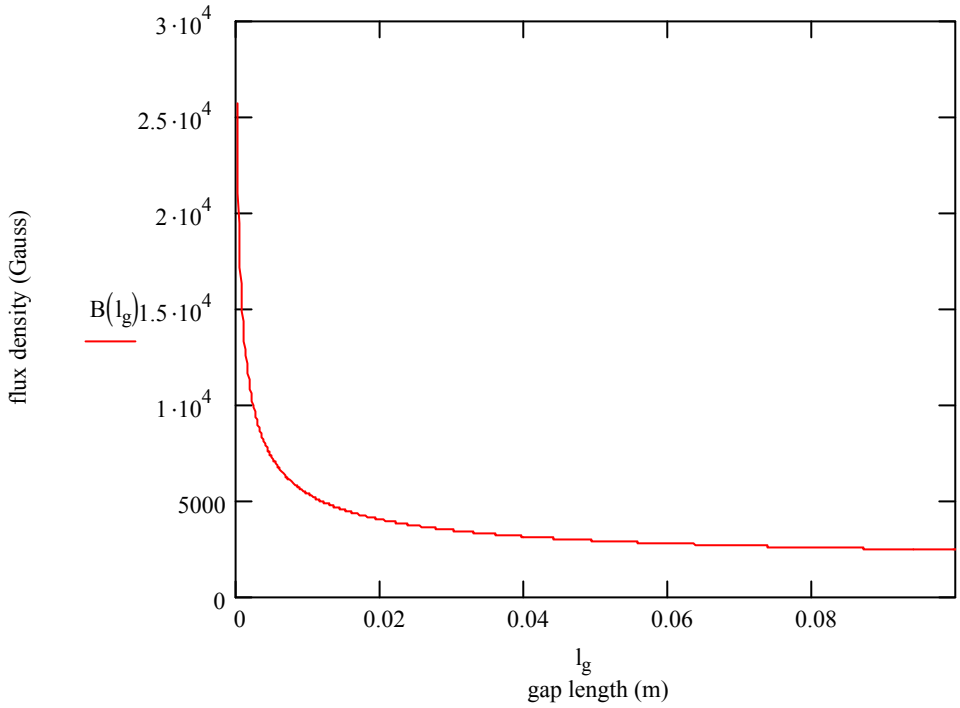


Figure 5-8. Maximum flux density as a function of gap length

5.6. Layout

The PCB layout of the inductor is shown in Figure 5-9. This layout is done for the EE64 core with 4 turns to make 3 µH of inductance per inductor. Two inductors are placed in parallel to create an effective inductance of 1.5 µH. The first four layers are for the inductor. It is wound with one layer taking up the entire window opening, and then the trace goes down one layer and is wound around the core to make four turns. The first four layers must use blind vias. This

means that the vias will only connect two layers. If the vias occupied more than two layers, then the windings would have to keep extending outward and the inductor could be very large.

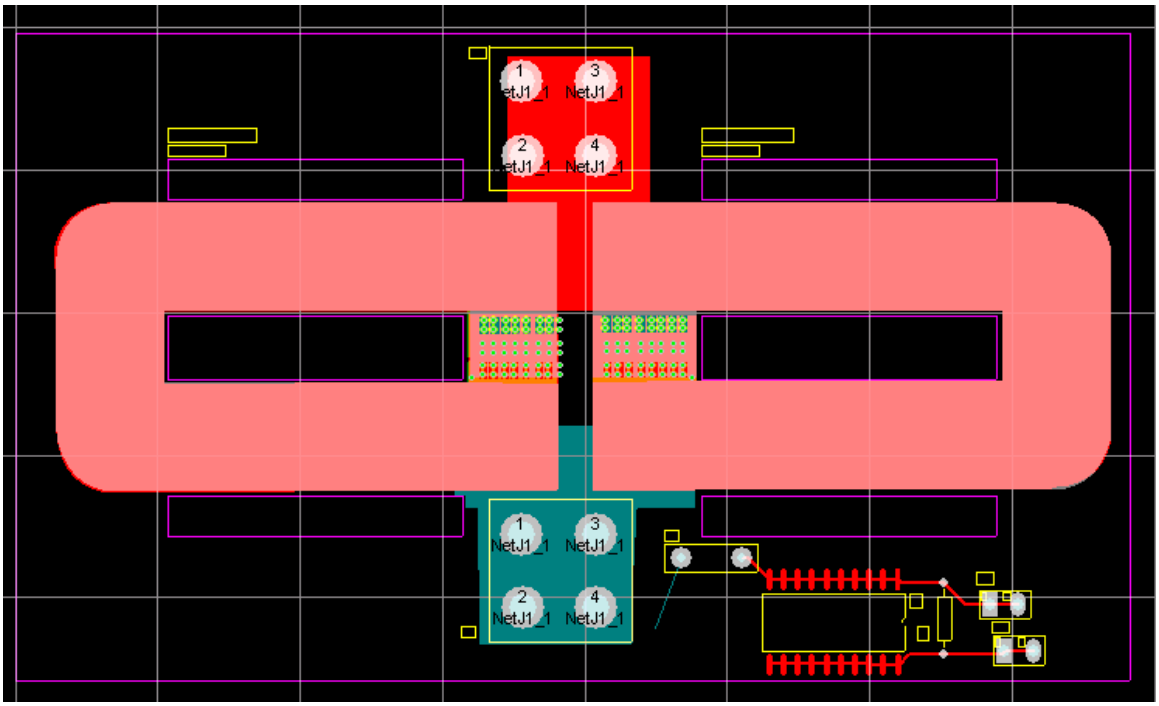


Figure 5-9. PCB layout for inductor

This inductor requires an auxiliary winding that is used for the startup operation. Since the inductor needs 4 turns, the secondary needs 14*4=56 turns. The secondary splits the windings between the two different inductors. Essentially the auxiliary winding needs to be wound in series. This makes 28 turns per inductor core, or 14 turns per layer for each inductor core. Figure 5-10 shows the winding configuration of the auxiliary windings.

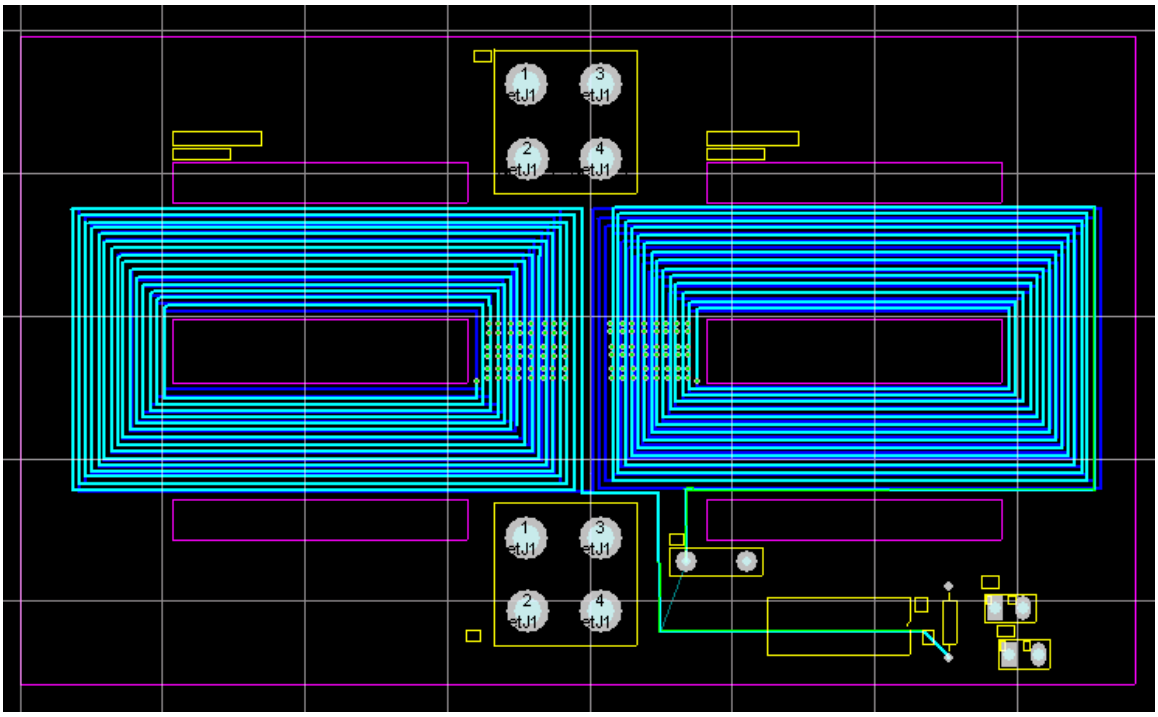


Figure 5-10. Auxiliary winding configuration

5.7. Conclusion

The inductor offered several design problems that were not encountered in the transformer design and therefore was placed on a separate PCB. The total number of layers for the inductor was kept at 6 but the copper weight was 13 oz for the top 4 layers and 6 oz for the bottom 2 layers. The copper weight was reduced on the lower two layers to reduce weight and design tolerances in the system. Since, the lower two layers hold the auxiliary windings and they only run for short period of time, thermal management is not a concern. The temperature rise for the inductor was calculated to be slightly above the specifications given in Table 5-1. This is because the inductor will be mounted to a heatsink and the calculations do not take this into account.

The final concern of the inductor was the air gap that was required. If the gap is only on one leg of the core then the gap is greater than 50% of the center leg length for the EE64 core. However, this gap can be distributed over the three legs to reduce the fringing from becoming a major problem. Another alternative is to add material to the gap that is slightly magnetic. The

problem with this is that the gap must be very large to have the same number of turns. The large gap will reduce the utilization of the window area and could cause manufacturing problems. Either method to achieve the gap is acceptable and meets the design requirements.

Chapter 6. Conclusions and Future Work

6.1. Conclusion

Planar magnetics are still in the stage that it is not beneficial to use in all applications. It does offer many advantages in thermal management, parasitic repeatability, and height requirements. However, the PCB can still be very costly. In this thesis the transformer's PCB was kept to six layers with no blind or buried vias. For this case the transformer can offer a competitive alternative to the traditional wire wound configuration. However, the inductor required 6 to 11 layers depending on the core that was chosen. It also required having 13 oz copper and many blind vias on every layer to carry the current. In this case the inductor has become more expensive using a planar design than the traditional wire wound configuration. Thus the integration to include the inductor in the entire planar magnetic and circuit integration remains questionable.

The research that this thesis presented focused on the design and implementation of planar magnetics in a 3 kW bi-directional DC/DC converter. Many technical papers have been written on how the planar transformer and inductor are designed and implemented. However, little work has been done in integrating the magnetic components into a system and showing the parasitic effects that the magnetic components have on the circuit's performance.

Using the network analyzer, finite element analysis and circuit implementation it has been proven that the interconnection and trace inductances from the DC/DC converter does affect the leakage inductance of the system. This system was originally designed ignoring the interconnection and trace inductances effects, but the measurement results proved that the interconnection and trace inductances were much greater than the leakage inductance of the transformer. In general the desired leakage inductance can be obtained by a closed form solution given the number of turns and geometrical arrangement. To obtain a high leakage inductance, the transformer does not need to interleave the primary and secondary layers. With an interleaved structure the transformer efficiency can be improved, but the leakage inductance will be lowered.

The interconnection and trace inductances cannot be obtained without knowing the geometrical structure. It was relevant in this design because the turns ratio of the transformer was high. This means that when these inductances are reflected from the low turns side to the high turns side, the value is greatly increased by the turns ratio squared. If a low turns ratio was used, then the reflected inductance would not be as substantial.

In this design a certain leakage inductance was needed for a soft switching application. For most other cases, especially with hard switching, a minimum leakage inductance is wanted, to decrease the loss of duty cycle. If this is the situation, then steps should be taken to try and reduce the inductance of the traces. The trace inductance can be reduced by increasing the copper weight, interleaving layers, and using wider traces.

This thesis redefines the conventional term of leakage inductance as the sum of a set of lumped parasitic inductances and the transformer leakage inductance for the integrated planar magnetics and inverter power circuitry. For the conventional non-integrated transformer, either planar or non-planar, the leakage inductance is defined between the two terminals of the transformer. However, for the integrated planar magnetics, the new lumped parasitic and leakage inductance should include the inverter switch and dc bus interconnections.

The transformer was first designed using a closed-form solution for a known geometry with different copper thickness. The calculated leakage inductance was then verified with the finite element analysis and the impedance analyzer measurement. It was found that the theoretical calculation and finite element analysis agreed very well, but the measurement result was more than one order of magnitude higher. This prompted the study of interconnect parasitics. With the geometrical structure and proper termination and lumping a set of parasitic inductances were defined. These inductances were verified with the impedance analyzer and the phase-shifted full bridge inverter testing.

In addition to parasitic inductance analysis, the flux distribution and associated thermal performance of the planar structure was also studied with finite element analysis. The resulting plots of the flux distribution and temperature profile indicate the key locations of mechanical

mounting and heat sinking. Overall the thesis covers the essential design considerations in electrical, thermal, and mechanical aspects of the planar magnetics integration.

6.2. Future Work

The next steps for the transformer is to complete the heavier weight copper PCB. The PCB tested was only a prototype that used a lower weight copper to measure the leakage inductance. Leakage inductance is not a large factor of the copper weight but will affect it a small amount. Then this PCB needs to be operated at full power to confirm both losses of the transformer and the thermal considerations for the PCB and transformer core. This will give a better relationship between the theoretical calculations and the circuit operation.

The planar inductor still has more work that needs to be done. The PCB for the inductor was not built for testing. To confirm the inductance and layout, a prototype should be made with a lower copper weight. This prototype can insure that the inductance and winding methodology is accurate. Then the final PCB should be constructed and tested at the full power level. This will give a better understanding of the losses and temperature rises of the system. The blind vias that were placed on the center layers of the PCB are usually hotter than the surrounding areas. This is because the current is forced through a smaller area than was originally calculated. It needs to be confirmed that these hot spots are not hot enough to cause problems.

The final consideration is the connection that is between the transformer / inverter board and the inductor board. A large amount of current will need to be carried between these two PCBs. If a poor connection is made, it could have a resistance producing a significant amount of heat. The design used four M4 size bolts that connect the PCBs together. However, the bolts and washers should be made in such a way that reduces the amount of resistance in the current path.

Appendix A Transformer Design

This file was designed to calculate all relavent parameters asscoiated with the 3kW/2kW bidirectional converter planar transformer.

Jeremy Ferrell, Troy Nergaard, Xudong Huang, Dr. Jason Lai
Virginia Tech; Center for Power Electronic Systems

Given Design Parameters. Reference figure 1 for notation

$Voutmin := 200$ Minimum output voltage.

$Voutmax := 450$ Maximum output voltage

$Vinmin := 7$ Minimum input voltage

$Vinmax := 16$ Maximum input voltage

$Iprimarymax_{boost} := 350$ Boost mode maximum current

$Iprimarymax_{buck} := 150$ Buck Mode maximum current

$N := 14$ Turns Ratio

$Np := 1$

Maximum Output Power

$Pomax_{boost} := 3000$

$Pomax_{buck} := 2000$

$Vt := \frac{Voutmax}{N}$ Max voltage across transformer on LV side

Duty Cycle Calculations

Boost Mode:

$Vinmin_{boost} := Vinmin$

$Vinmax_{boost} := 14.4$

$D_{boost} := 1 - N \cdot \frac{Vinmin_{boost}}{Voutmax}$ $D_{boost} = 0.782$ Duty cycle for boost mode Full Bridge Converter

$D_{load} := 0.5$ This represents the duty cycle of the load. Since in boost mode the load will be on for 5 seconds then off for 5 seconds.

Buck Mode:
In buck mode the power will be flowing in the opposite direction (Right to left in figure 1). The traditional conversion ratio for full bridge isolated buck converter is Vo/Vin=TurnsRatio*Duty.

$Vinmax_{buck} := Voutmax$ $Vinmax_{buck} = 450$ V

$Vinmin_{buck} := 230$ V Here 230 volts is used to calculate the worst case duty cycle.

$Voutmax_{buck} := Vinmax$ $Voutmax_{buck} = 16$ V

$D_{buck} := \frac{Voutmax_{buck}}{Vinmin_{buck}} \cdot N$ $D_{buck} = 0.974$

Worst Case Comparision

$Irmsprimary_{buck} := Iprimarymax_{buck} \cdot \sqrt{D_{buck}}$

$Irmsprimary_{buck} = 148.031$ Primary RMS Current for buck mode operation

$Irmsprimary_{boost} := Iprimarymax_{boost} \cdot \sqrt{D_{boost}}$

$Irmsprimary_{boost} = 309.552$ Primary RMS current for boost mode. Not including the load duty cycle.

Pick which is the worst case current condition

$$Irmsprimary := \begin{cases} Irmsprimary_{boost} \cdot \sqrt{D_{load}} & \text{if } Irmsprimary_{boost} \cdot \sqrt{D_{load}} \geq Irmsprimary_{buck} \\ Irmsprimary_{buck} & \text{otherwise} \end{cases}$$

$Irmsprimary = 218.886$ A

$Irmssecondary := \frac{Irmsprimary}{N}$ Seconary current of transformer

$Irmssecondary = 15.635$ A

Transformer Calculations

$Bmax := 2500\ G$ Maximum Allowed flux density. Gauss

$Jm := 300\ \frac{A}{cm^2}$ Current Density

$K := 0.5$ Fill Factor

$fsw := 100 \cdot 10^3\ Hz$ Switching Frequency

Area Product

$$Area := \frac{\left(D_{boost} \cdot 8.6 \cdot Iprimarymax_{boost} \cdot \sqrt{D_{boost}}\right) \cdot 100^4}{Jm \cdot K \cdot \frac{Bmax \cdot fsw \cdot 100^2}{10000}}$$

$Area = 5.553\ cm^4$

Power Loss in Transformer

Philips

3C90 material

This is the power loss for three given frequencies for 3C90 material from Philips at 2500 G

$P_{25k} := 0.1\ \frac{W}{cm^3}$

$P_{50k} := 0.6\ \frac{W}{cm^3}$

$P_{100k} := 1\ \frac{W}{cm^3}$

EE58 Core

$Ve := 24.6\ cm^3$ for EE combination

$Core_{E58} := 2$ Number of cores needed to avoid saturation

$$P_{E58} := \begin{pmatrix} 25000 & P_{25k} \cdot Ve \cdot Core_{E58} \\ 50000 & P_{50k} \cdot Ve \cdot Core_{E58} \\ 100000 & P_{100k} \cdot Ve \cdot Core_{E58} \end{pmatrix}$$

This is for 3C90 Material

$f2 := P_{E58}^{\langle 0 \rangle}$ $P_{E58} := P_{E58}^{\langle 1 \rangle}$

EI58 Core

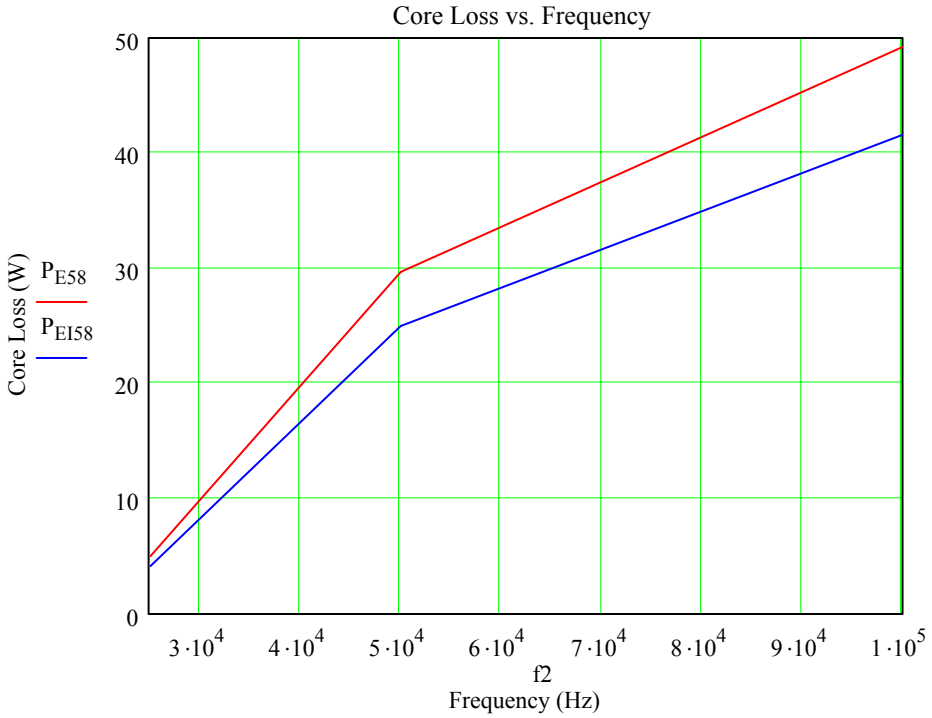
$Ve := 20.8 \ cm^3$

$Core_{EI58} := 2$ Number of cores needed to avoid saturation

$$P_{EI58} := \begin{pmatrix} 25000 & P_{25k} \cdot Ve \cdot Core_{E58} \\ 50000 & P_{50k} \cdot Ve \cdot Core_{E58} \\ 100000 & P_{100k} \cdot Ve \cdot Core_{E58} \end{pmatrix}$$

This is for 3C90 Material at 2500 G

$f2 := P_{EI58}^{\langle 0 \rangle}$ $P_{EI58} := P_{EI58}^{\langle 1 \rangle}$



Skin Depth

$\mu_0 := 4 \cdot \pi \cdot 10^{-7}$ Permeability of air (H/m)

$\mu_r := 1$ Relative Permeability of copper

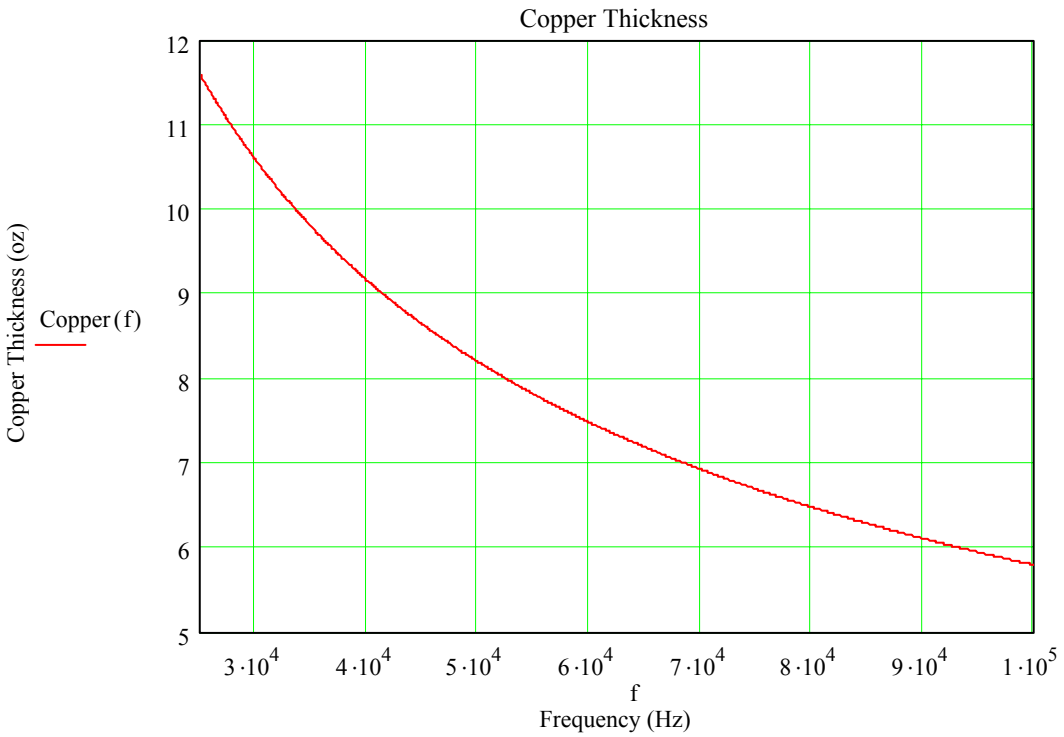
$\rho := 1.673 \cdot 10^{-8}$ Resistivity of copper (Ω*m)

$oz := 1.4$ 1 oz copper is 1.4 mils thick

$\delta(f) := \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu_r \cdot \mu_0}}$ m Skin Depth in meters

$\delta(f) := 1000 \cdot \frac{\delta(f)}{2.54}$ mils Skin Depth in mils

$Copper(f) := \frac{\delta(f)}{oz}$ Copper thickness in oz



PCB Trace Widths

$k := .024$ .048 for outerlayer or .024 for innerlayer

According to Park Nelco, which is the manufacturer of FR4 running at a temperature of 130 C is not a problem. This would be for the base FR4 material. Higher temperature FR4 materials are available.

$t := 30$ Temp rise in C

$tol := 7 \ mils$ Tolerance for thickness given by UPE

$oz := 1.4$ Thickness of 1oz copper in mils

According to UPE's design specifications the minimum spacing for internal layers that support 300-500 V should be greater than 10 mils. Also given UPE's specifications, 6 oz copper has a minimum conductor width and minimum spacing of 20 mils. The smaller the spacing between conductors the greater the interwinding capacitance. Strataflex has a minimum spacing of 25 mils for 8 oz copper.

$Space := 35 \ mils$ Spacing Between windings of secondary

$Layer_{secondary} := 2$ The number of layers required for the secondary windings

$Layer_{primary} := 3$ Number of primary layers

$Cores_{58} := 2$ Number of cores needed

E58 For the E58 core 820 mils is the minimum window width given Philips tolerances.

$W_{58} := 820 - 95 \ mil$

$W_{58} = 725 \ mil$

The 70 mils is for tolerance. UPE has 5 mil tolerance on the dimensions of the board (This times two). The minimum distance from copper plane to the edge of the board is 10 mils(This times 2). Then another 20 mils on each side so the board will fit easily into the core.

Since for the E58 core we will have two in parallel, the equivalent window area is doubled.

$W2_{58} := 2 \cdot W_{58}$

$$Aprimary := \left(\frac{Irmsprimary}{k \cdot t^{.44}} \right)^{\frac{1}{.725}}$$

$$Cp_{58} := \frac{Aprimary}{oz \cdot W2_{58}}$$ This assumes that the primary is a single turn

$Cp_{58} = 18.119 \quad oz$ This is the total copper weight needed for the primary to be one turn.

$$Cp58 := \frac{Cp_{58}}{Layer_{primary}}$$

$Layer_{primary} = 3$

$Cp58 = 6.04$ Copper Weight needed per layer for the given temperature rise

$t = 30 \quad C$ Temperature rise of the primary

Current Density

$$Jp := \frac{Irmsprimary}{Aprimary \cdot \left(\frac{25.4}{1000}\right)^2} \qquad Jp = 9.224 \quad \frac{A}{mm^2}$$

Turns per layer for two cores and the secondary windings are in series. This means that each core will have a 1:7 turns ratio and each layer will have 3.5 turns

$Turnsperlayer_s := 3.5$

$t := 35 \quad C$ Temperature rise for the secondary

$$Asecondary := \left(\frac{Irmssecondary}{k \cdot t^{.44}}\right)^{\frac{1}{.725}}$$

Current Density

$$Js := \frac{Irmssecondary}{Asecondary \cdot \left(\frac{25.4}{1000}\right)^2} \qquad Js = 27.561 \quad \frac{A}{mm^2}$$

The copper thickness on the secondary side is computed using the area needed for a specified temperature rise plus the amount of space required to fit the number of windings on each layer. This number is then divided by the width available by the core and then divided by the number of turns on each layer. This is because the secondary layer must support multiple windings.

$$Cs_{58} := \frac{Asecondary \cdot ceil(Turnsperlayer_s)}{W_{58} - ceil(Turnsperlayer_s) \cdot Space}$$

$Cs_{58} = 6.012 \quad oz$ Oz copper that should be chosen for secondary.

$$Wtrace_{58s} := \frac{W_{58} - Space \cdot ceil(Turnsperlayer_s)}{ceil(Turnsperlayer_s)}$$

Width of Secondary Turns. Using the weight of copper above.

$Wtrace_{58s} = 146.25$ mils

Copper Loss

$\rho := 6.587 \cdot 10^{-7}$ $\Omega \cdot in$ Resistivity of copper

$MLT_{58} := 5.146$ in Mean Length per turn(MLT)

$C_p := 6$ $C_s := 6$ Oz of Copper

$Width_{58p} := \frac{W_{58}}{1000}$ Covert mils to inches

$Width_{58s} := \frac{Wtrace_{58s}}{1000}$ Covert mils to inches

$Aw_{58p} := Width_{58p} \cdot C_p \cdot \frac{oz}{1000}$ in^2

$Aw_{58s} := Width_{58s} \cdot C_s \cdot \frac{oz}{1000}$ in^2

$$Rdc_{58p} := \rho \cdot \frac{MLT_{58}}{Aw_{58p}}$$

$Rdc_{58p} = 5.566 \times 10^{-4}$ Ω

$$Rdc_{58s} := \rho \cdot N \cdot \frac{MLT_{58}}{Aw_{58s}}$$

$Rdc_{58s} = 0.039$ Ω

AC Resistance

A valid assumption for the AC resitance is 20% of the DC resistance. This is given experience of people in the lab.

$AC := 0.2$

$Rac_{58p} := Rdc_{58p} \cdot AC$

$Rac_{58p} = 1.113 \times 10^{-4}$ Ω

$Rac_{58s} := Rdc_{58s} \cdot AC$

$Rac_{58s} = 7.726 \times 10^{-3}$ Ω

$$Pcopper_{58s} := Irmssecondary^{2} \cdot \left(Rdc_{58s} + Rac_{58s}\right)$$

$$Pcopper_{58s} = 11.331 \quad W$$

$$Pcopper_{58p} := Layer_{primary} \cdot Cores_{58} \left(\frac{Irmsprimary}{Layer_{primary} \cdot Cores_{58}} \right)^{2} \cdot \left(Rdc_{58p} + Rac_{58p}\right)$$

$$Pcopper_{58p} = 5.333 \quad W$$

Total losses; this is DC +AC copper losses and core loss at 100 kHz

$$Losses := Pcopper_{58p} + Pcopper_{58s} + P_{EI58_2}$$

$$Losses = 58.265 \quad W$$

$$Efficiency := \frac{3000\,100}{3000 + Losses}$$

$$Efficiency = 98.095 \quad \%$$

Height of PCB Core

$thick_{FR4} := 20$ mils Thickness of insulation material of PCB

$thick_{out} := 5$ mils Thickness of insulation on outer layers

$$PCBHeight := oz \cdot C_s \cdot Layer_{secondary} + C_p \cdot oz + 2 \cdot thick_{out} + thick_{FR4} \cdot \left(Layer_{primary} + Layer_{secondary} - 1\right)$$

$$PCBHeight = 115.2 \quad mils$$

Maximum PCB Height Given the tolerances provided by UPE. UPE's maximum thickness for a PCB is 250 mils

$$MaxPCB := PCBHeight + tol \cdot \left(Layer_{secondary} + Layer_{primary}\right)$$

$MaxPCB = 150.2$ mils Assuming 5 Layer board

Current Density for DC bus

$Wdc := 1000 \quad mils$ Minimum (Near mounting hole)

$Layers_{dc} := 2$

$Adc := Wdc \cdot 6 \cdot oz \cdot Layers_{dc}$

$$Jdc := \frac{Irmsprimary}{Adc \cdot \left(\frac{25.4}{1000}\right)^2} \qquad Jdc = 20.195 \quad \frac{A}{mm^2}$$

Leakage Inductance

$w := 0.018 \quad m$ Width of secondary trace

$MLT_{58} := 0.131 \quad m$ Mean length per turn for each core

Let Each of the thicknesses include the copper plus insulation

$C_s = 6 \quad oz \qquad Core_{EI58} = 2$

$C_p = 6 \quad oz$

$$L_{lk}(h) := \mu_0 \cdot \left(\frac{N}{Core_{EI58}}\right)^2 \cdot \frac{MLT_{58}}{w} \cdot \left[\frac{\left(C_p \cdot oz \cdot Layer_{primary} + C_s \cdot oz \cdot Layer_{secondary}\right)}{3} \cdot 2.54 \cdot 10^{-5} + h \cdot 2.54 \cdot 10^{-5}\right] \cdot Core_{EI58}$$

$$L_{lk}(48.4) = 1.421 \times 10^{-6}$$

$C_s := 2 \quad oz \qquad C_p := 2 \quad oz$

$$L_{lk2oz}(h) := \mu_0 \cdot \left(\frac{N}{Core_{EI58}}\right)^2 \cdot \frac{MLT_{58}}{w} \cdot \left[\frac{\left(C_p \cdot oz \cdot Layer_{primary} + C_s \cdot oz \cdot Layer_{secondary}\right)}{3} \cdot 2.54 \cdot 10^{-5} + h \cdot 2.54 \cdot 10^{-5}\right] \cdot Core_{EI58}$$

Prototype1 has 2 oz on the outter layers and 0.5 oz on the inner layers

$thick_{FR4} := 3 \quad mils$

$C_s := 1.25 \; oz \qquad C_p := 1 \quad oz$

$$L_{lktest}(h) := \mu_0 \cdot \left(\frac{N}{Core_{EI58}}\right)^2 \cdot \frac{MLT_{58}}{w} \cdot \left[\frac{\left(C_p \cdot oz \cdot Layer_{primary} + C_s \cdot oz \cdot Layer_{secondary}\right)}{3} \cdot 2.54 \cdot 10^{-5} + h \cdot 2.54 \cdot 10^{-5}\right] \cdot Core_{EI58}$$

Prototype 1

6.7 mils is from 2 layers of insulation between the primary and secondary, each is 3 mils. Also we have 1 layer of copper which is 0.5 oz=0.7mils

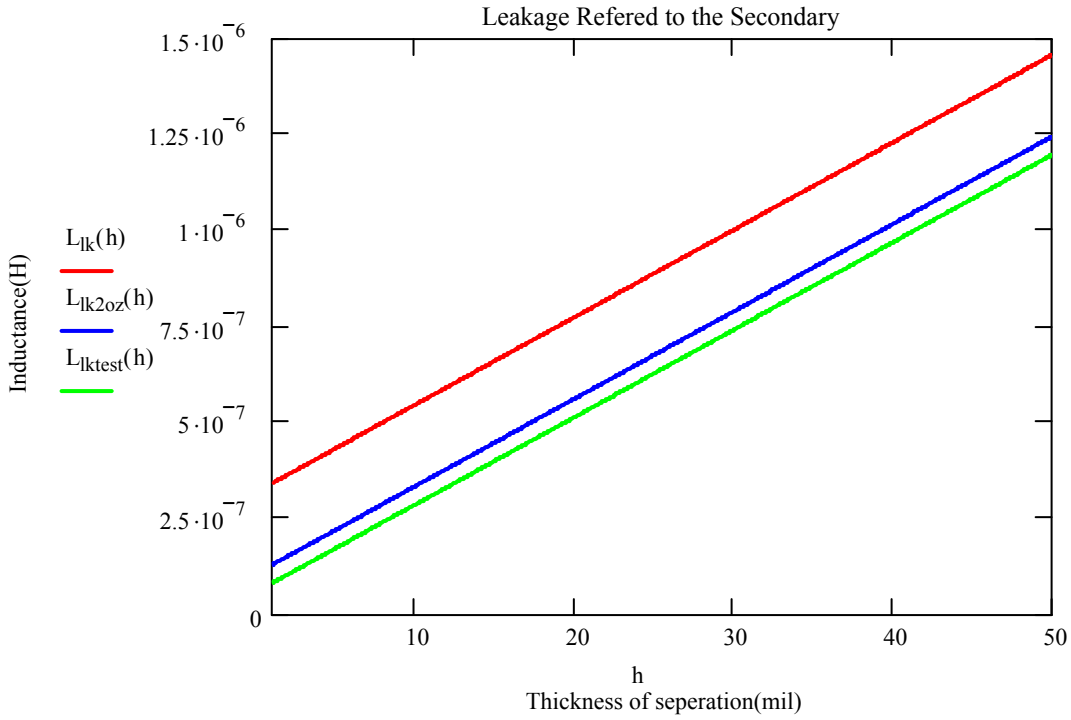
$$L_{lktest}(6.7) = 2.11\times 10^{-7}$$

Prototype 2

43 mils is from 2 layers of insulation between the primary and secondary, each is 20 mils. Also we have 1 layer of copper which is 2 oz=2.8mils

$$L_{lk2oz}(42.8) = 1.081\times 10^{-6}$$

m



Core Stats and Flux Density

EE58 :

$$Wa := \left(\frac{50 - 8.1}{2}\right)\cdot 2\cdot 6.5 \qquad Ae := 305 \quad mm^2 \qquad Wa = 272.35$$

$$AeWa := \frac{Ae\cdot Wa}{10^4} \qquad AeWa = 8.307 \quad cm^4$$

$$B_{E58}(f) := \frac{Vt}{4\cdot 10^{-8}\cdot \frac{Ae}{100}\cdot f\cdot Np\cdot Cores_{58}}$$ Flux Density for number of cores given

$$B_{E58}(100000) = 1.317\times 10^3 \quad G$$

Maximum height that PCB core can be. Given one core

$MaxHeight := 2\cdot 255$ mils

$MaxHeight = 510$ mils

$limit(f) := 2500$

EI58:

This uses of E and I core from Philips

$$Wa := \left(\frac{50 - 8.1}{2}\right)\cdot 6.5 \qquad Ae := 310 \quad mm^2 \qquad Wa = 136.175$$

$$AeWa := \frac{Ae\cdot Wa}{10^4} \qquad AeWa = 4.221 \quad cm^4$$

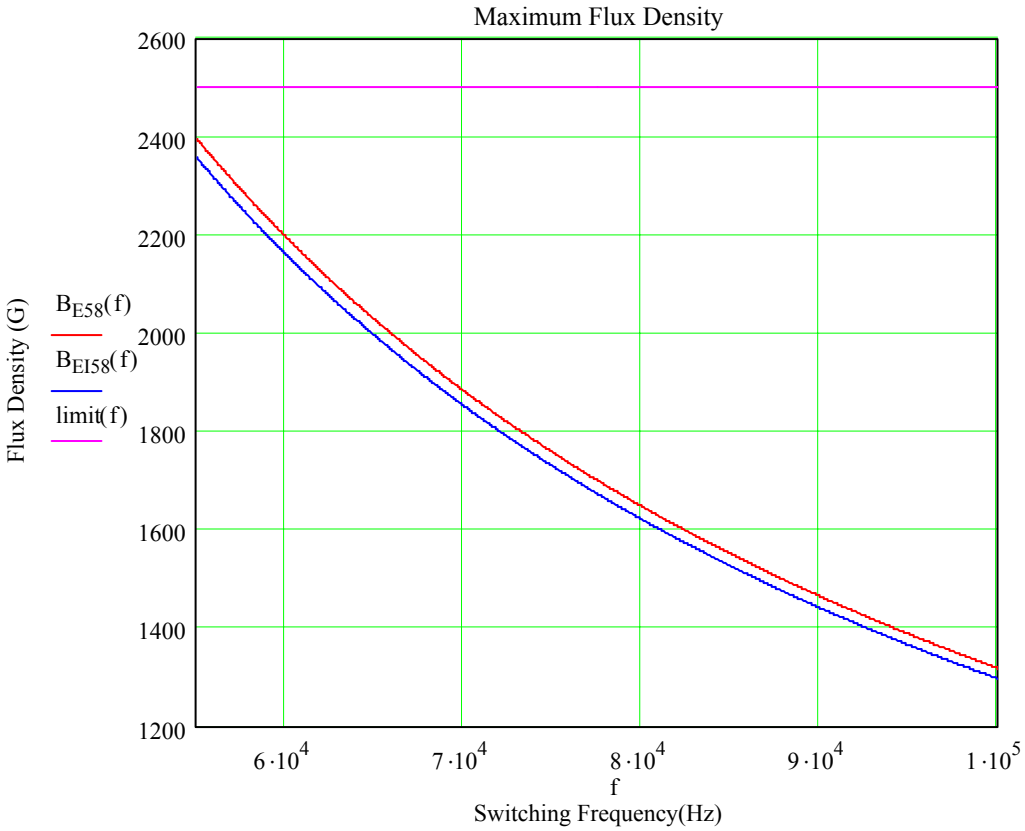
$$B_{EI58}(f) := \frac{Vt}{4 \cdot 10^{-8} \cdot \frac{Ae}{100} \cdot f \cdot Np \cdot Cores_{58}}$$

Flux Density for number of cores given

$$B_{EI58}(100000) = 1.296 \times 10^{3} \quad G$$

Maximum height that PCB core can be. Given one core

MaxHeight := 255 mils



Appendix B Parasitic Calculation

Formula obtained from Grover pg 35

$B := 1.55 \cdot 2.54$ cm Width of conductor

$C := 10 \cdot \frac{1.4 \cdot 2.54}{1000}$ cm thickness of conductor

$\frac{C}{B} = 9.032 \times 10^{-3}$

$l := (3.7) \cdot 2.54$ cm Length of conductor

Self Inductance of L2

$$L := 0.002 \cdot l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 0.039$ µH

$ReflectedL2 := L \cdot 14^2$

$ReflectedL2 = 7.565$ µH

Self Inductance of L4

$ReflectedL4 := ReflectedL2$

Self Inductance of L1

$l := (3.8) \cdot 2.54$ cm

$$L := 0.002 \cdot l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 0.04$ µH

$ReflectedL1 := L \cdot 14^2$

$ReflectedL1 = 7.87$ µH

Self Inductance of DC-

$l := (3.2) \cdot 2.54 \quad cm$ Length of conductor

$B := 1.35 \cdot 2.54 \quad cm$ Width of conductor

$C := 4 \cdot \frac{1.4 \cdot 2.54}{1000} \quad cm$ thickness of conductor

$$L := 0.002 \cdot l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 0.033 \quad \mu H$

$ReflectedLdc := L \cdot 14^2$

$ReflectedLdc = 6.535 \quad \mu H$

$(ReflectedL2 + ReflectedLdc + ReflectedL4) = 21.664 \quad \mu H$

Self Inductance of DC+

$l := (3.2) \cdot 2.54 \quad cm$ Length of conductor

$B := 1.6 \cdot 2.54 \quad cm$ Width of conductor

$C := 4 \cdot \frac{1.4 \cdot 2.54}{1000} \quad cm$ thickness of conductor

$$L := 0.002 \cdot l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 0.031 \quad \mu H$

$ReflectedLdc := L \cdot 14^2$

$ReflectedLdc = 5.996 \quad \mu H$

$(ReflectedL1 + ReflectedLdc + ReflectedL1) = 21.736$

Self inductance from the transformer not attached to the core

$l := (0.42) \cdot 2.54 \quad cm$ Length of conductor

$B := 0.7 \cdot 2.54 \quad cm$ Width of conductor

$C := 6 \cdot \frac{1.4 \cdot 2.54}{1000} \quad cm$ thickness of conductor

$$L := 0.002 l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 1.428 \times 10^{-3} \quad \mu H$

$$ReflectedLtrans := \frac{L \cdot 14^2}{2}$$

$ReflectedLtrans = 0.14 \quad \mu H$

Self inductance of the space between the two transformers

$l := (1.135) \cdot 2.54 \quad cm$ Length of conductor

$B := 1.7 \cdot 2.54 \quad cm$ Width of conductor

$C := 6 \cdot \frac{1.4 \cdot 2.54}{1000} \quad cm$ thickness of conductor

$$L := 0.002 l \cdot \left(\ln\left(\frac{2 \cdot l}{B + C} \right) + \frac{1}{2} - 0.00089 \right)$$

$L = 4.517 \times 10^{-3} \quad \mu H$

$$ReflectedLtrans := 2L \cdot 14^2$$

$ReflectedLtrans = 1.77 \quad \mu H$

Appendix C Inductor Design

Given Design Parameters.

$Voutmin := 200$	Minimum output voltage.
$Voutmax := 450$	Maximum output voltage
$Vinmin := 7$	Minimum input voltage
$Vinmax := 16$	Maximum input voltage
$Iprimarymax_{boost} := 350$	Boost mode maximum current
$Iprimarymax_{buck} := 150$	Buck Mode maximum current
$N := 14$	Turns Ratio
$Np := 1$	
$Pomax_{boost} := 3000$	Maximum Output Power
$Pomax_{buck} := 2000$	
$D_{boost} := 0.782$	Worst Case Duty Cycles
$D_{load} := 0.5$	

Philips Core E64

$cores := 2$	number of cores in parallel
$L(f) := \frac{cores \cdot 100000\, 1.5 \cdot 10^{-6}}{f}$ H	Inductance
$I_{Lpk} := \frac{400}{cores}$	Current
$I_{Lrms} := \frac{350 \cdot \sqrt{D_{boost}} \cdot \sqrt{D_{load}}}{cores}$	
$B_{max} := 0.25$ T	Max Flux Density (2500 G)
$k_u := 0.6$	Fill Factor
$J_m := 3 \cdot 10^6$ A /m^2	Current Density
$\mu_0 := 4\pi \cdot 10^{-7}$ H/m	Permeability of air
$\mu_r := 1$	Relative Permeability of copper
$\rho := 1.673 \cdot 10^{-8} \cdot \Omega \cdot m$	Resistivity of copper
$fs := 100000$	Switching Frequency

Area Product:

$$AreaProd := L(fs)\cdot\frac{I_{Lpk}\cdot I_{Lrms}}{k_u\cdot J_m\cdot B_{max}}\cdot 100^4 \qquad AreaProd = 14.59 \quad cm^4$$

Need A_c*W_a > AreaProd

Using 3C90 ferrite material

$Wa := 2.22 \quad cm^2$ window area

$A_c := 5.19 \quad cm^2$ area of core

$w_c := 5.08 \quad cm$ width of core $\qquad A_c\cdot Wa = 11.522 \quad cm^4$

$l_c := 2\cdot .0051 \quad m$ Center Leg Length(For EE combination)

Maximum height that PCB core can be. Given one core

$MaxHeight := 2\cdot 200 \quad mils$

$MaxHeight = 400 \quad mils$

Determine the Air Gap

Assuming lc >> lg

$$l_g := \frac{\mu_0\cdot L(fs)\cdot I_{Lpk}^2}{B_{max}^2\cdot A_c}\cdot 10^4 \qquad l_g = 4.649\times 10^{-3} \quad m$$

$$A_L := \frac{10\cdot B_{max}^2\cdot A_c^2}{L(fs)\cdot I_{Lpk}^2} \qquad A_L = 140.292 \quad \text{mH/1000 turns (watch units here)}$$

Percentage of gap to center leg length

$$Plc := \frac{l_g\cdot 100}{l_c} \quad \% \qquad Plc = 45.577 \quad \%$$

Number of Turns

$$N := \frac{L(fs)\cdot I_{Lpk}}{B_{max}\cdot A_c}\cdot 10^4 \qquad N = 4.624$$

Determine the Corrected Turns accounting for Fringing

$$F := 1 + \frac{l_g\cdot 100}{\sqrt{A_c}}\cdot \ln\left(2\cdot\frac{l_c}{l_g}\right)$$

$F = 1.302$

$$n := \frac{N}{\sqrt{F}} \qquad n = 4.053$$

$$N := \text{ceil}(n) \qquad N = 5$$

Determine Adjusted Inductance using new turns

$$Leq := \frac{N \cdot B_{max} \cdot A_c}{I_{Lpk} \cdot 10^4 \text{cores}} \qquad Leq = 1.622 \times 10^{-6}$$

Determine Flux Density

$$B := \frac{L(fs) \cdot I_{Lpk}}{A_c \cdot N} \cdot 10^8 \qquad B = 2.312 \times 10^3 \quad G$$

Determine the PCB

$$A_w := \frac{I_{Lrms}}{J_m} \qquad A_w = 3.648 \times 10^{-5} \quad m^2$$

$k := .024$ .048 for outerlayer or .024 for innerlayer

$t := 34$ Temp rise in C (using a max temp of 120 C, limited by the FR4)

$tol := 7 \quad mils$ Tolerance for thickness given by UPE

$oz := 1.4$ Thickness of 1oz copper in mils

$Wcir_{64} := 858 \quad mil$ Width of core window

$Cu := 13 \quad oz$ Copper weight

$Space := 3 \cdot Cu \quad mils$ Spacing Between windings of secondary

$$A_{pcb} := \left(\frac{I_{Lrms}}{k \cdot t^{.44}} \right)^{\frac{1}{.725}}$$

$$Wcir := \frac{A_{pcb}}{Cu \cdot oz} + 40$$

Need $Wcir = 759.878$ mil

$P_{Layersp} := 1$ Number of Parallel Layers

$$TurnperLayer_p := floor\left(\frac{Wcir_{64} - 40}{\frac{Wcir}{P_{Layersp}}}\right) \qquad TurnperLayer_p = 1$$

The 40 mils is for tolerance. 20 mil from the PCB to the core and 10 mil from the copper to the edge of the PCB on each side.

Skin effect

$$\delta(fs) := \sqrt{\frac{\rho}{\pi \cdot fs \cdot \mu_r \cdot \mu_0}}\ m$$ Skin Depth in meters

$$\delta(fs) := 100 \cdot \frac{1000\,\delta(fs)}{2.54}\ mils$$ Skin Depth in mils

$$Copper(fs) := \frac{\delta(fs)}{oz}$$ Copper thickness in oz

Copper Losses

$N := 4$

$N_p := N$ Number of primary turns

$$N_s := \frac{N_p \cdot 14}{cores}$$

$S_{Layerss} := 2$ Number of secondary layers in Series

$$TurnperLayer_s := \frac{N_s}{cores \cdot S_{Layerss}}$$

$$Irms_p := \frac{I_{Lrms}}{cores} \cdot A$$ $Irms_p = 54.714A$

$$Irms_s := \frac{Irms_p}{\frac{N_s}{N_p}}$$ $Irms_s = 7.816A$

$MLT_{64} := 5.69 \cdot in$ Estimated Mean Length per Turn

$C_p := Cu$ $C_s := 6$ Oz of Copper

Auxillary Winding

$Space := 25$

$$W_{aux} := \frac{Wcir_{64} \cdot S_{Layerss} - Space \cdot N_s - 70}{N_s}$$

$W_{aux} = 33.786$ mils

Board Thickness

$C_p = 13$

$C_s = 6$

$Insulation := 20$ $(Cu \cdot oz + 5) = 23.2$

$Layers := N \cdot P_{Layersp} + S_{Layerss}$ $Layers = 6$

$Thickness := N \cdot P_{Layersp} \cdot Cu \cdot oz + S_{Layerss} \cdot C_s \cdot oz + Insulation \cdot (Layers - 1)$

$Thickness = 189.6$ mils $MaxHeight = 400$ mils

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Vita

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During the summer of 1999 he worked for American Research Corporation of Virginia. During this time he designed, built and tested various analog and digital circuits. During the summer of 2000 he worked for Ford Motor Company. During his time at Ford Jeremy was responsible for the electrical system issues that were encountered during manufacturing on the Escape program.

In the fall of 2000 Jeremy entered into the 5 year B.S./ M.S. program at Virginia Polytechnic Institute. Also during the fall of 2000 he started doing research at the Center for Power Electronics System (CPES) under Dr. Jason Lai. He received his bachelors degree in May 2001 from Virginia Polytechnic Institute. Upon completion of his M.S. degree he will work full time for Northrop Grumman in Sykesville Maryland.