Electronics for a Versatile and Robust Retarding Potential Analyzer for use in Nano-Satellite Platforms

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ABSTRACT

A retarding potential analyzer (RPA) is an instrument that, when mounted on a satellite in low-Earth orbit, makes in-situ measurements of ion density, temperature and speed relative to the satellite frame. The instrument works by changing the voltage on one of a set of grids and measuring a corresponding current generated by ions flowing through the grid, generating a function of current vs. voltage called an I-V curve. Traditionally, the size and power requirements of retarding potential analyzers has limited their use to larger satellites. In this thesis, the electrical design and basic testing of a retarding potential analyzer for use on resource-limited cubesat platforms are described.

The mechanical design of the retarding potential analyzer is first described, and the requirements of the electrical design are presented. The electrical requirements are based on both the characteristics of the ionosphereic flight environment, and on the size and power requirements typical of the small cubesat platforms for which the instrument is intended.

The electrical hardware is then described in detail. The digital design is reviewed as well, including the instrument's operating modes, command and data structure, and timing scheme.

Test data showing the basic functionality of the instrument are then presented. Bench tests validate the design by confirming its ability to control voltages and measure small currents. End-to-end tests were also performed in a vacuum chamber to mimic the ionospheric environment. These data are presented to show the ability of the RPA to meet or exceed its design specifications.

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All photos by author, 2014.

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Chapter 1-History and Functionality of RPAs

Retarding potential analyzers (RPAs) have been used extensively over the last half-century on satellite missions designed to provide diagnostics of the thermal ion distribution in low-Earth orbit. The practical and theoretical underpinnings of the RPA technique have been well described in the literature[1-6], and RPA instruments have been successfully flown on a host of satellite missions[7-11]. Reasons for the popularity of RPAs include their relative simplicity and the large number of state variables that can be inferred from their measurements. When coupled with good velocity data and attitude knowledge for the spacecraft, analysis of the current-voltage characteristics produced by an RPA provides measurements of the overall plasma density, the ion temperature, the component of the ion velocity along the orbit-track, and the ratio of light ions (*e.g.*, He^+) to heavy ions (O^+, NO^+, *etc*.) in planetary ionospheres. Very few other single-sensor spacecraft instruments simultaneously measure such a large number of geophysically significant parameters.

Limited budgets for spaceflight experiments have constrained opportunities to fly large research satellites. In response to these pressures the space science community has begun to embrace the idea of flying smaller, cheaper satellite systems, which have been characterized as microsats (total mass less than 100 kg), nanosats (mass less than 10 kg), and picosats (mass less than 1 kg). Scientifically useful CubeSats[12] are typically in the nanosat class; they involve satellites that have standardized architectures and straightforward specifications to minimize cost and complexity. Both NASA and the NSF have recently created funded programs specifically for CubeSats, and have encouraged the space science community to use them for both scientific and educational purposes.

There have so far been scores of CubeSat launches, but no CubeSat mission has yet flown an RPA because the size, weight, power, and pointing requirements for well-established RPA designs are not commensurate with the CubeSat platform. Over the past two years our research group has addressed this issue by developing a versatile, robust, and fully functional RPA specifically for the CubeSat spacecraft bus architecture. For this thesis, I have designed and tested the electronic system that controls this Cubesat-compatible RPA. The electrical design includes both analog and digital hardware, performs in-flight measurements of a very small current and communicates with a satellite bus that relays data to ground.

A basic high-level diagram of an RPA is shown in Figure 1. The RPA concept is notably straightforward. The instrument is comprised of a series of flat, electrically conductive grids in a stacked parallel-plane configuration, where the normal to the grids is aligned in the direction of motion of the satellite (the ram direction). The number of grids in an RPA is a design variable, but it typically ranges from three to seven. Most of these grids are held at constant potentials, while one grid is driven by a positively-swept periodic voltage signal. Since the satellite velocity greatly exceeds the ion thermal velocities in low Earth orbit there will be a supersonic flux of ions through the aperture (outermost) grid, which is typically maintained at spacecraft ground.

Behind the aperture lies the grid with the swept voltage signal, which is called the retarding voltage (RV) grid. Its purpose is to set up a time-varying energy barrier to the incoming ions. When the RV grid voltage is at ground all of the incoming ions will pass through

it, hit a flat collector plate and be measured as a current, but as the RV grid voltage is swept to increasingly positive values fewer of the incident ions have sufficient energy to pass through, so the collected current is reduced. Each measurement made by an RPA is represented by a current-voltage (I-V) characteristic in which the collected current is plotted as a function of the retarding voltage. The I-V curves are essentially integrals of the Maxwellian distribution function that describes the thermal ion population, so by careful curve-fitting analysis the fundamental state variables of the plasma can be inferred.

Knudsen[2] gives an equation for the I-V curve produced by an ideal RPA flying at orbital speed through a plasma composed of multiple ionic constituents:

$$I = T_r A e v \cos\theta \sum_i n_i * \left[\frac{1}{2} + \frac{1}{2}\mathrm{erf}(k_i) + \frac{\exp(-k_i^2)}{2(\pi)^{\frac{1}{2}} a_i}\right],$$

where

$$k_i = a_i - b$$
$$a_i = \frac{v\cos\theta}{\alpha_i}$$
$$\alpha_i = \left(\frac{2kT^+}{m_i}\right)^{\frac{1}{2}}$$
$$b = \left(\frac{e(V+\varphi)}{kT^+}\right)^{\frac{1}{2}},$$

where T_r is the total fractional transmission of the grid stack, A is the aperture area, e is the charge of an ion, v is the magnitude of the relative velocity between the satellite and the mean velocity distribution of the ambient ions, θ is the angle between the normal to the RPA aperture and the spacecraft velocity vector, n_i is the ion concentration of the i^{th} constituent, m_i is the mass of the i^{th} ionic constituent and T^+ is the ion temperature. All the ion species are assumed to be in thermal equilibrium, so a single temperature applies to all constituents. V is the potential of the retarding grid relative to the spacecraft, and φ is the potential of the spacecraft relative to the plasma. The grids must be mounted on the spacecraft such that the normal to the grid plane points along the spacecraft velocity vector (in the ram direction). This minimizes the attenuation of the current due to the cos θ term in the above equation, so the current collected is proportional to the area of the aperture. An ideal I-V curve for a two-constituent plasma comprised of H^+ and O^+ is shown in Figure 2. Through curve fitting the ion concentration, temperature, and relative speed of the ions in the spacecraft frame can be inferred from these data.

Ions are collected on a plate referred to as the collector, which provides the current input to the RPA electronics. In addition, for this particular RPA, a suppressor grid held at negative potential sits behind the retarding grid to prevent electrons from escaping from the collector when it is hit by incoming fast-moving ions. One more grid, called the shield grid, sits between the suppressor and collector and is held at ground to prevent capacitive coupling between the suppressor grid and the collector when they are vibrating with respect to each other. The

purpose of the RPA electronics is to sweep the voltage on the RV grid, control the voltages on the suppressor and shield grids, and measure the collector current.

An additional aspect of the RPA is called a "senpot." A senpot is an exposed surface that can be used on the spacecraft to provide a stable reference voltage, which can serve as a biasing technique for the RPA or other in-situ measurement instruments[3]. This technique is useful to counter the effects of small spacecraft charging events, which can adversely affect the IV curve analysis[13]. The senpot technique therefore improves RPA performance in cases where the overall spacecraft ground reference undergoes changes due to geophysical events (e.g., aurora), photoelectron and secondary electron flux changes due to shading of conductive surfaces, and magnetic field aspect effects that hinder thermal ion and electron flux to the spacecraft. The senpot technique requires a small surface on the ram face of the satellite to be electrically isolated from the rest of the spacecraft. The potential of this surface is used as the ground reference for the RPA, rather than the overall spacecraft bus ground. For spacecraft that have a senpot surface the RPA is able to connect to and buffer this surface, effectively using the senpot reference as a floating ground.

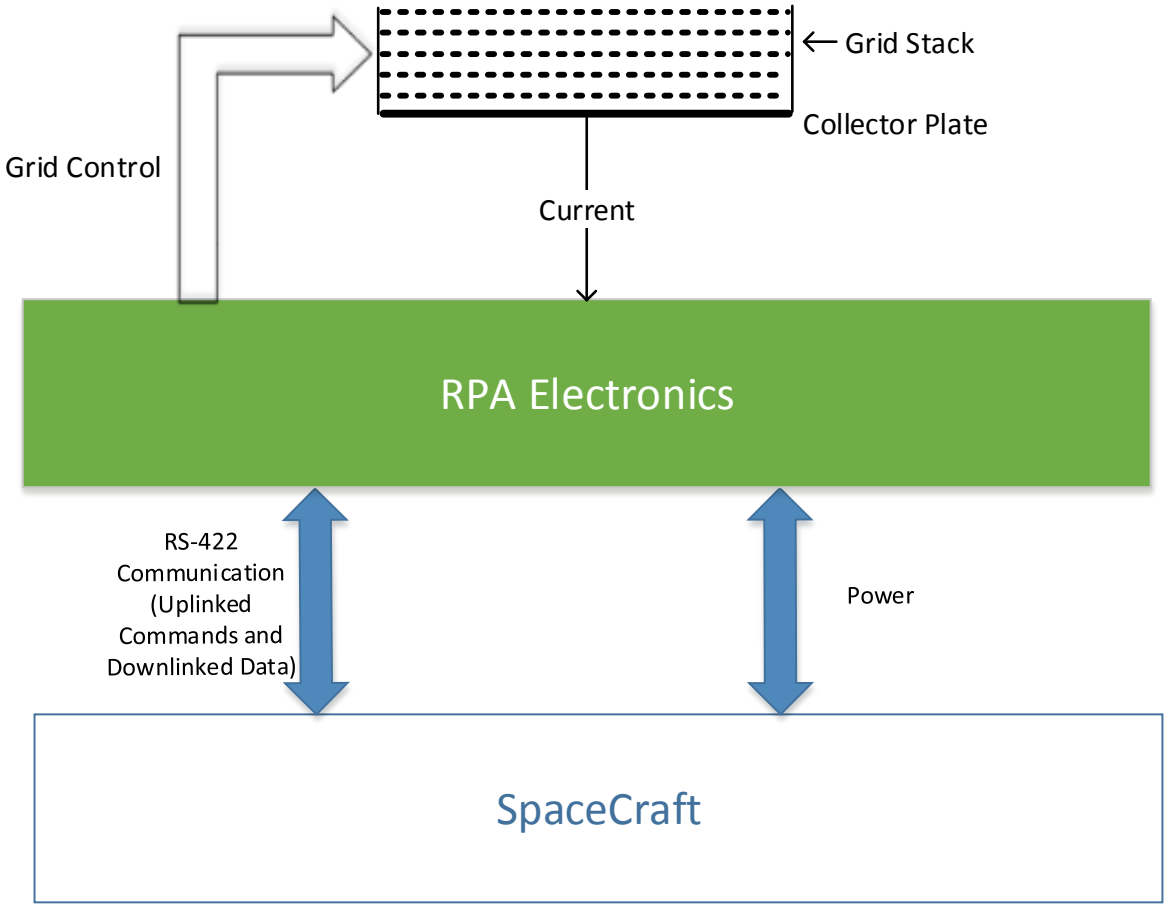

Figure 1: Overall block diagram for a satellite-borne RPA system.

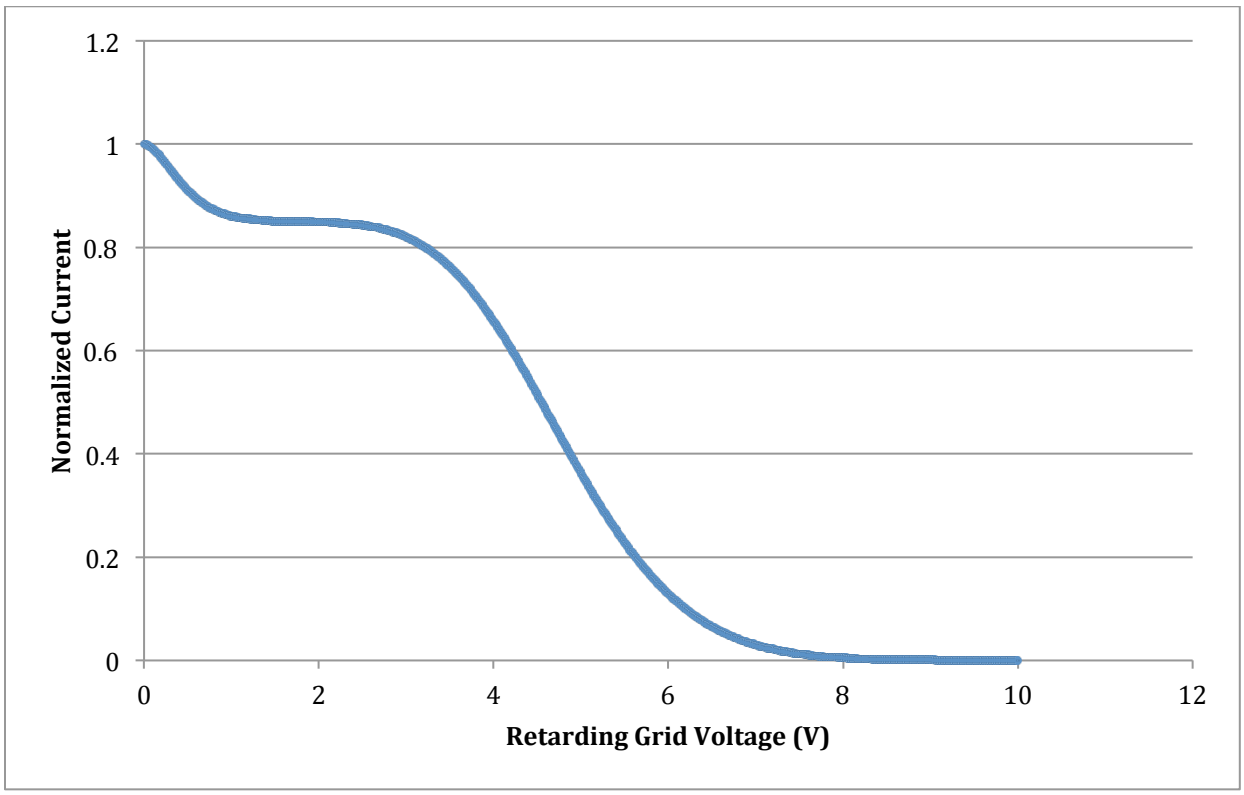

Figure 2: Idealized RPA curve for a typical two-constituent H^+/O^+ plasma in low Earth orbit.

Chapter 2-Requirements of the Cubesat RPA and Mechanical Design

The basic requirements of the RPA electronics are to control the voltage of the grids at the front of the instrument, to measure the current coming off of the collector corresponding to each voltage on the retarding grid, and to report the data back to the satellite data handling system. The mechanical RPA design dictates how many grids the RPA must control. The RPA must be able to set its grid voltages to some specific degree of accuracy, and it must accurately measure the collected ion current with some required precision. In addition, it is desired that the RPA be able to change the characteristics of its retarding voltage sweeps depending on commands that are sent to the satellite from ground, so that its performance can be optimized in flight for particular geophysical conditions. Consequently there must be some method of communication between the satellite bus and the instrument that allows it to receive and respond to commands in-flight. Lastly, there must be some electronics for buffering the senpot voltage.

A CAD model of the CubeSat RPA (CuRPA) sensor mechanical assembly is shown in Figure 3. There are five grids used within the CuRPA that the electronics must control. The outermost aperture grid, through which the ions first pass, is held at spacecraft ground. This ensures that the ion trajectories are not perturbed by electric fields near the aperture. The next grid can either be held at ground to serve as a second aperture grid, or its voltage can be swept and it can serve as a redundant retarding grid. This capability is to be controllable via command uplink. The third grid is the retarding grid, whose voltage must be swept to generate the IV curve that comprises a measurement set. The fourth grid is the suppressor grid, which must be held at a negative potential sufficient to prevent electrons from escaping the collector plate. The closest grid to the collector plate is the shield grid that prevents coupling between the suppressor and collector.

In order to be compatible with the cubesat platform, the mass of the CuRPA (including the sensor structure and electronics) is ≤ 0.4 kg, and the entire mechanical portion of the instrument is contained within a 7.7 x 7.7 x 2.6 cm volume. The design has been approached to enable easy and quick assembly of the sensor structure, including grid rotation and stack-up. After being aligned and fastened, the grids are connected to the CuRPA electronics via soldered lead wires.

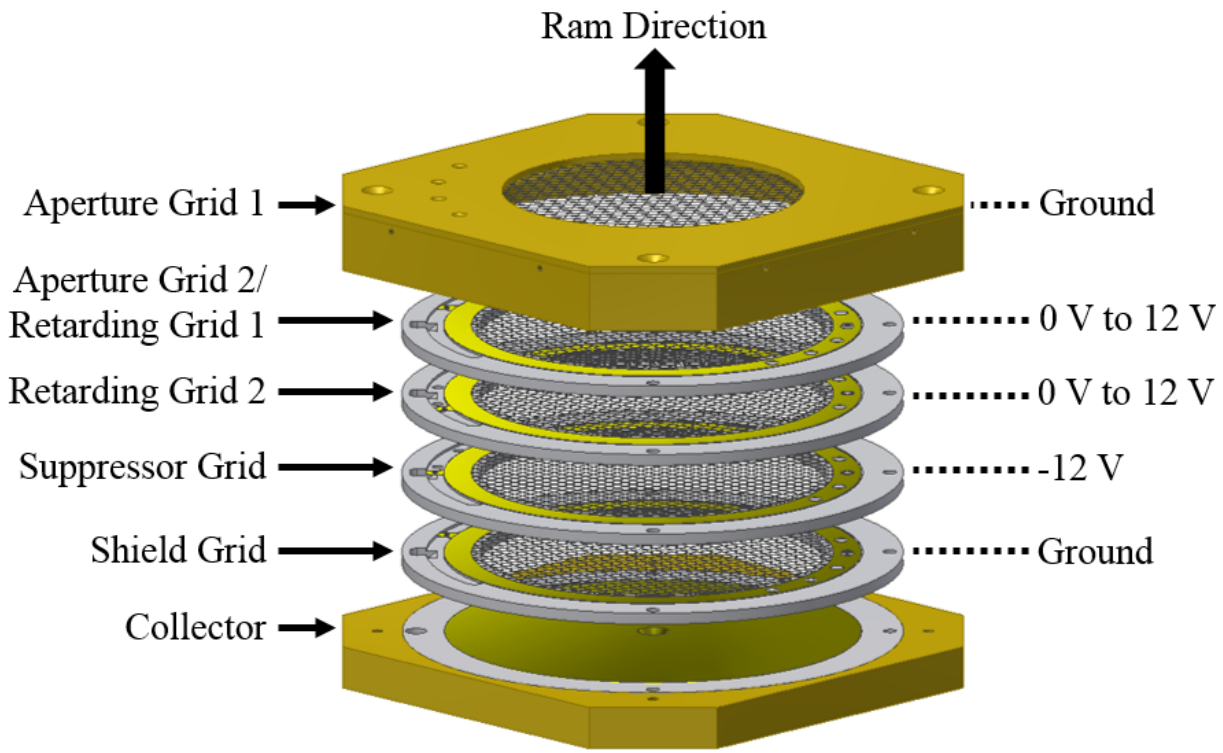

Figure 3: Mechanical assembly of the CuRPA sensor surface. The printed circuit boards housing the control and measurement electronics are located beneath the collector.

The specific requirements of the CuRPA electrical system, such as the range of currents that must be measured, the range of voltages that must be set on the grids, and the RV sweep rate come from a combination of scientific analysis of the properties of the F-region of the ionosphere, and knowledge of RPAs garnered from past missions. The requirements are summarized in Table 1. The current range is given by an estimate of the maximum collector current based on the density of ions in the ionosphere and their speed relative to the spacecraft. The relation is $I=\eta neVA$, where η is the transmission coefficient, n is the ion density, e is the electric charge, V is the speed of the ions relative to the spacecraft and A is the aperture area. The transmission coefficient of the CuRPA grid stack is about 0.35. In the region where the CuRPA will be flying, densities typically range up to ~5,000,000 ions/(cm^3), and the speed of the satellite and low drift velocities of the ions give a an ion speed of about 7.5 km/s in the satellite frame. The area of the aperture is 23.226 cm^2. This gives the requirement that the CuRPA must be able to measure a maximum of 5 μA of current from the collector. Instabilities in the ionosphere can sometimes create plasma depletions that result in densities of a few hundred ions per cubic centimeter; to capture these events the low end of the CuRPA sensitivity should be less than a nanoamp. Previous missions have shown that a reasonable accuracy in the current measurement is either 500 pA or 2.5%, whichever is greater for the current being measured.

A typical I-V curve like that shown in figure 2 shows a current approaching zero at a retarding grid voltage of around 10 V, so the retarding grid must be able to sweep up to 10 V to produce a complete I-V curve. The suppressor grid must have a large enough negative voltage to prevent secondary and photoelectrons from leaving the collector, since these effects would bias

the current measurement by artificially enhancing the measured positive current to the collector. A sufficient value to repel the electrons is -5 V, so the electronics must be able to drive the suppressor grid at or below this level. The RPA sweep must last 2 seconds or less and include at least 16 different current-voltage points along the I-V curve, so the CuRPA must be able to set the RV grid bias to at least 16 different voltages while measuring the corresponding current. Typical temperature values on satellites range from 5^{o} to 30^{o} C, so the CuRPA must be able to operate in this range, and to survive fluctuations over a somewhat larger range.

Parameter	Value
Measured Current Range	500 pA to 5 uA
Measured Current Accuracy	Greater of 500 pA or 2.5 %
Samples per I-V Curve	16 or More
I-V Curve Sweep Time	2 s or Less
Retarding Voltage Range	10 V or More
Suppressor Bias	-5 V or Less
Operating Temperature	-20^{o} to 75^{o} C

Table 1: Science-based requirements of the CuRPA.

The requirement for sweep flexibility adds much more complicated restraints to the CuRPA electrical design. Rather than taking one sample per I-V point, it is desired that several current samples be accumulated and averaged for better accuracy. While every sweep must have a minimum of 16 samples per I-V curve, it is desired that the number of points per sweep might be able to change in-flight. More points in a sweep leaves less time to oversample current points, so there is a trade-off between the oversampling of the current samples and the number of points per sweep. The voltages on the grids will ideally have flexibility as well. In an environment where the collector current approaches zero at a retarding grid voltage of 5 V, it is useless for half of the voltages in the sweep to be higher than 5 V, so it is desired that the voltage values be able to change based on uplinked commands. Furthermore, multiple schemes for changing the voltages are required in the RPA design. In addition to changing linearly with a constant step size, it is desired to have a mode where the retarding voltage stays the same for an entire sweep, which allows for higher spatial resolution in the ion density measurements. Also, as shown in Figure 2, the current changes more rapidly in the middle of the I-V curve and is relatively flat at the two ends. So it is desired to have a mode where the retarding voltage points increase nonlinearly such that they are concentrated in the middle of the voltage range, yielding more points in the middle of the I-V curve than at the ends. This results in better curve-fits during data analysis, and therefore more accurate temperature and velocity data. This flexibility in the on-orbit operation of the CuRPA requires some on-board storage of the retarding voltages for this "smart" sweep. Finally, it is desired to have two options regarding how the second retarding grid behaves: it should be able to sweep along with the first retarding grid, or it should be able to remain at ground for the entire sweep.

Based on these system constraints, an electrical design has been developed to control the grids, sample the collector current, and report the data back to the satellite data handling system.

Chapter 3-Electrical Schematic and Analog Design

A functional block diagram of the RPA electronics is shown in Figure 4 and detailed electrical schematics are shown in Appendix A. The main components of the electrical system controlling the CuRPA are a logarithmic transimpedance amplifier for converting the collector current into a voltage, an analog to digital converter (ADC) for digitizing this voltage, a digital to analog converter (DAC) for setting the voltages on the grids, and a field programmable gate array (FPGA) for controlling the converters and communicating with external electronics. The electrical section is broken physically into two separate boards; 1) a main board that contains power conditioning, external command and telemetry, housekeeping monitoring, signal conditioning and data acquisition, grid bias control, and overall system control, and 2) a daughterboard that contains a logarithmic current sensor that interfaces with the collector. The daughterboard is mounted on the main board, and power and signal measurements are transmitted between the two over a common connector. In accordance with the temperature requirement for normal satellite conditions, the operating range of the electronics is -20^{o} to 75^{o} C and the survival range is -40^{o} to 85^{o} C.

The board communicates with external electronics via a 115,200-baud UART (universal asynchronous receiver/transmitter). This is chosen because it is easy to implement in an FPGA, suitable for receiving byte-long commands and sending 16-bit samples, and because it allows the electronics of the CuRPA and the devices with which it communicates to run on separate clocks.

The transimpedance amplifier is mounted on a separate daughterboard to reduce noise and leakage current. Because the input currents from the collector may be quite small, any slight interference caused by capacitive coupling or currents leaking through the board substrate could make a measurable difference to the collector current. Because the digital communication electronics on the CuRPA can cause spikes through capacitive coupling, the daughterboard isolates the sensitive collector current input from the digital electronics.

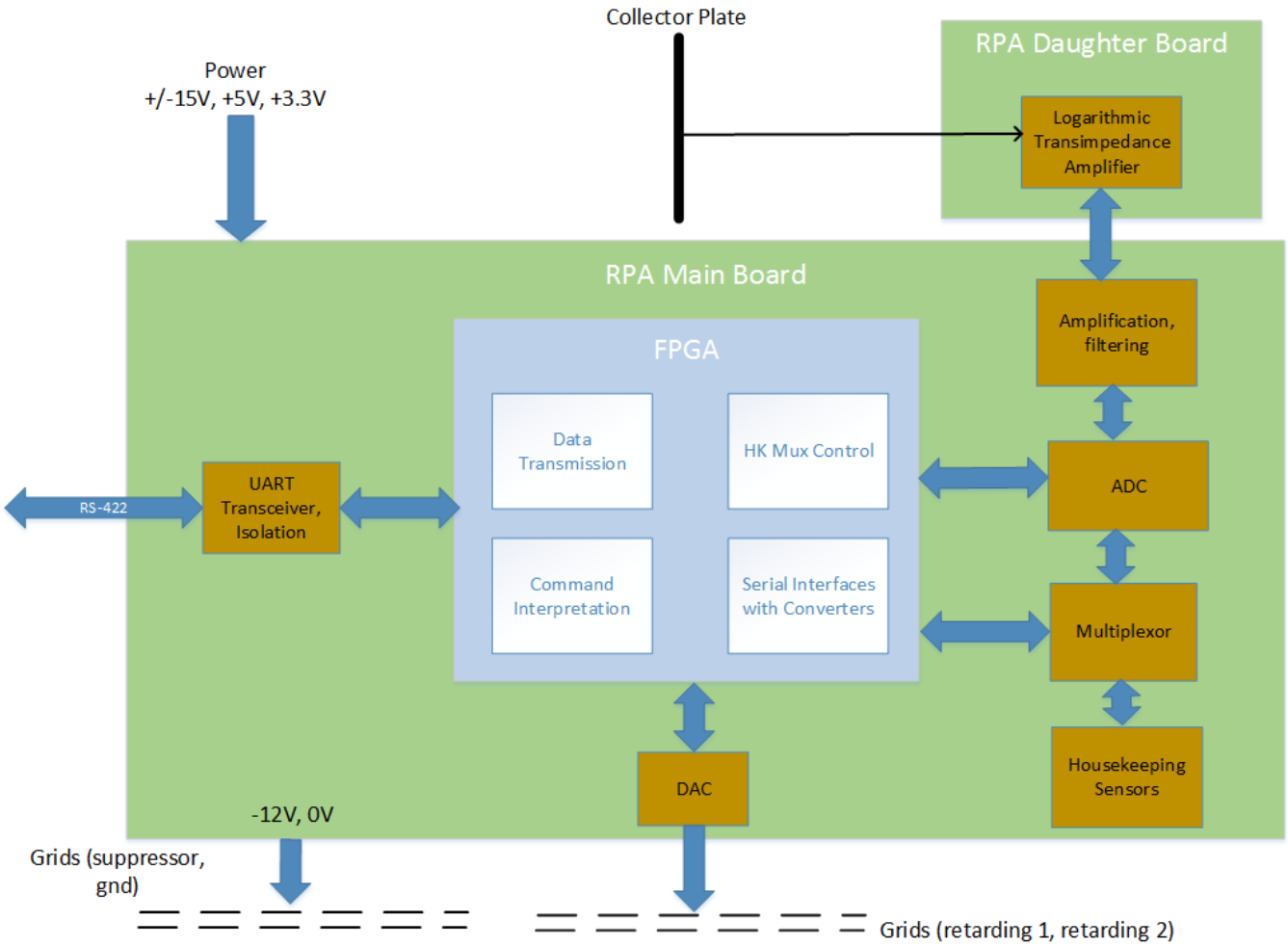

Figure 4: RPA Electronic Functional Block Diagram

Power Supplies and Communication

The CuRPA receives externally supplied 3.3, 5, separate ±5, and ±15 voltage buses for operation. These voltage buses are electrically isolated (> 1 MΩ DC) from the external source, locally filtered and conditioned, and then distributed throughout the main and daughter boards. The 3.3 and 5 V lines are used for the digital electronics blocks while the ±5 and ±15 V lines power the analog electronics. The power supplies come into the board on a 37-pin nano-D connector. Each power supply uses multiple lines, and ground lines run between the power supplies. Each line is filtered by a capacitor network, and the 3.3V line is additionally filtered by an RF bead because it can be very noisy due to the digital communication. In addition, an efficient DC-DC converter generates 1.5 V to run the FPGA core, and other voltage reference circuits generate 1.25 V and 2.5 V for biasing the analog electronics. In accordance with the requirements, all of the CuRPA system electronics dissipate ≤ 0.5 W of average power, making this design compatible with small spacecraft systems in which the orbit averaged power is typically on the order of a few watts.

The UART is implemented through an RS-422 connector. An onboard serial transceiver chip isolates the external lines magnetically and provides send and receive lines that are connected directly to the FPGA. This enables the CuRPA RS-422 connection to communicate with other systems without needing a common ground. The transceiver chip is directly connected to FPGA I/Os for passing UART signals. In addition, the FPGA controls when the send and receive sides of the transceiver are enabled.

Grid Control

The grid voltages are controlled by a four-channel 16-bit digital-to-analog converter (DAC) with an output range of 0-5 V. Each DAC output goes through a simple RC filter to minimize noise on the grids, and then is amplified by factor of 2.4 by a simple non-inverting opamp configuration. This makes the output voltage range 0-12V for each grid. In addition, the DAC output to the suppressor grid goes through an inverting stage, resulting in a suppressor grid voltage range of 0 to -12 V, surpassing the -5V requirement.

The DAC operates by serial interface with the FPGA, which is able to uniquely set the voltage on each grid. The serial interface is very simple, and a 10 MHz clock is used to transfer 16-bit values to the DAC. The chip includes a chip select line that remains high when the FPGA is not changing any grid voltage, and a power-on reset feature that sets all the grids to 0V when the CuRPA is powered on. One DAC transmission takes 2.8 μs (see Appendix C), an insignificant amount of time compared to a one second-long sweep.

Each grid is connected to a configurable jumper on the main CuRPA board that allows it to be set to some constant voltage rather than being controlled by the FPGA. When the fixed voltage option is selected on the jumper, each of those grids is connected through a resistive divider to the +15 V or -15 V (for the suppressor) power supply. For this specific application the suppressor grid is fixed at -12 V and is not controllable by the DAC.

Current Measurement

The logarithmic transimpedance amplifier is mounted on the daughterboard, and is connected to the main board through a shielded connector. To minimize leakage currents that might interfere with the very low expected current measurements, the wire carrying the input current from the collector plate is routed onto an insulating stand-off post on the daughterboard, and connected directly to the pin on the amplifier without contacting the board. The logarithmic amplifier chosen is the Texas Instruments LOG114, which outputs the logarithm of the ratio between the input current and a reference current, and produces a response of 0.35 V per decade of gain. It is able to accurately output current ratios at input currents ranging from 100 pA to 10 mA. The chip includes a 2.5 V reference voltage for setting the reference current by choosing a resistance. For the first flight version of the CuRPA the resistance chosen is 35.6 MΩ, which yields a reference of ~70 nA. The chip also includes an additional opamp for configuring another amplifier on the logarithmic output, with a gain of 2.34. The range in the output of that amplifier, which is connected to the main board, is then -2.5 V to 2.5 V, corresponding to a specified input current range of 100 pA to 50 μA. This is well-suited to the previously stated

current range requirement. A simulation of the LOG114 in the specified current range is included in Appendix A in the daughter board schematic, showing an output of -2.5 V to 2.5 V.

Originally, the LOG112 logarithmic amplifier was selected because its package type had pins that made wired connection of the collector current easier than on the LOG114. When the LOG112 response was examined with an oscilloscope, however, its response time was too slow for the 128-point CuRPA sweep. The maximum amount of time that it is possible to wait after updating the DAC before the ADC takes a value is about 6.35 ms, and the LOG112's response time is shown to be slightly too long (Figure 5). The log114, however, is a faster chip with a response time on the order of microseconds, a fraction of the LOG112's,.

The voltage output from the LOG114 chip on the daughter board is buffered, inverted and shifted up by 2.5 V on the main board so that its final range covers 0 to 5 V. It is then fed into a four-channel, 16-bit analog to digital converter (ADC), with a maximum sampling rate of 100 kHz. The voltage is also clamped by diodes to constrain it to a 0-5 V range at the input to the ADC. Fast-acting Shottky diodes with forward voltage drops of 0.35 V are used so the ADC input does not exceed its absolute maximum ratings when there are sudden spikes in voltage. When there is no current into the logarithmic amplifier its voltage output approaches -5V, which would cause an unsafe voltage at the input to the ADC if not clamped.

The ADC is controlled through a serial interface with the FPGA. The FPGA provides a (2.5 MHz) clock that both shifts a command in to the ADC and shifts out the 16-bit ADC sample. One ADC conversion takes 10.8 μs, with a maximum rate of about 80 kHz. The resolution of the ADC is 0.97 pA (0.01%) at the low end of the logarithmic range and 370 nA (0.7%) at the high end of the logarithmic range, in accordance with the accuracy requirement.

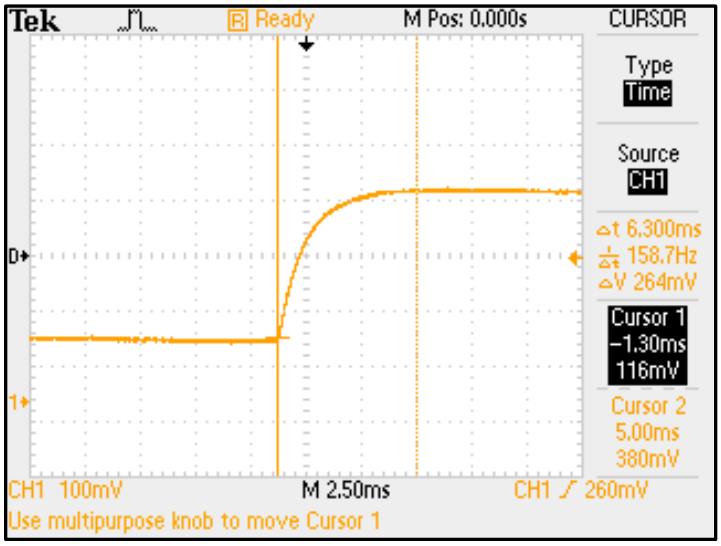

Figure 5: Step response of the LOG112.

Housekeeping Data - Monitoring

The multiple-channel ADC that monitors the logarithmic amplifier output also monitors the voltages on the retarding grid and the suppressor grid. In addition, eight values indicating

board status are routed through a multiplexer to another channel of the ADC. After the ADC takes a current measurement for each point in the sweep, it also takes a measurement of the retarding grid voltage before the voltage is set to a different level by the DAC, in order to verify the grid was at the expected voltage when the current measurement was taken. The suppressor grid voltage and housekeeping voltages are measured once per sweep before the sweep begins, just after the start bytes are sent. The eight housekeeping values measured are the voltage on the second retarding grid, the 3.3 V power supply, the temperature on the daughter board, three temperatures that are evenly distributed throughout the main board, the 5 V power supply and the 15 V power supply. The 5 V and 15 V power supplies are each put through a resistive voltage divider so they can be measured in the middle of the 0-5 V range of the ADC. The analog multiplexer is controlled by four outputs from the FPGA, so that the FPGA can control which channel of the multiplexer is being routed to the ADC. The temperature sensors are simple analog-output sensors that output 4 mV/K.

Senpot Buffer

The senpot surface voltage input is buffered by an instrumentation amplifier, filtered, buffered again and then returned back through the 37-pin power connector as senpot ground. The instrumentation amplifier provides voltage spike protection and has an extremely low input bias current to minimize interference with the senpot potential. The gain is selectable via one resistor. The senpot electronics are controlled by external power supplies. It is assumed that whatever is powering the CuRPA has the ability to select its ground lines as senpot ground with the SPGND line that is returned through the power connector. If the senpot functionality is not to be used, as in the LAICE satellite mission, the senpot electronics are powered down and the SPGND output is not used.

Chapter 4: FPGA Design

The integrity of IV curves can vary significantly for a given space experiment based on geophysical conditions, spacecraft charging, and gradual degradation of the orbit. These factors make it advantageous to have flexibility in how the samples are spaced throughout a single RV sweep. The RPA is therefore designed such that the voltage values applied to the retarding grid and the rate at which samples are taken are all programmable via uplinked commands. The retarding grid voltage values are programmable in-flight by a set of commands that control the number of points in a sweep and the voltages to which these points are set. The main functions of the FPGA are to receive uplinked commands that are relayed through the flight computer, control the timing of DAC and ADC conversions, and send data back through the satellite's communication systems.

Table 2 lists the parameters of the FPGA control that can change with every sweep depending on the uplinked control bytes. The uplinked commands indicate how the voltage on the retarding grid changes: whether it increases linearly throughout the sweep, remains constant throughout the sweep, or increases nonlinearly as a "smart" sweep designed to concentrate samples in areas where the collector current is changing most drastically. The number of current samples per sweep is also programmable. Based on how many points are in the sweep, the oversampling, or number of current measurements the RPA accumulates before averaging, changes. In addition, the amount of time that the RPA waits between updating the grid voltage and taking current samples changes depending on the number of points per sweep. Because the RPA performs one sweep per set of command bytes it receives, rather than continuously making measurements, it is easy to duty cycle the RPA performance by controlling when it receives start bytes.

Parameter	Number of Modes	Mode Descriptions
Sweep Voltage Setting	3	Default: Uniformly Spaced Points over 0-12V
		Smart: Voltage Samples Nonuniformly Spaced
		Ion Trap: Constant Retarding Grid Voltage
Points Per Sweep	3	32, 64 or 128
Oversampling	3	32 Points Per Sweep: 1024
		64 Points Per Sweep: 512
		128 Points Per Sweep: 128
Voltage on Second Retarding Grid	2	Hold at 0 Volts, or Update Synchronously with RG1
Wait Time Between Setting DAC and Measuring Current	2	32 or 64 Points Per Sweep: 12 ms
		128 Points Per Sweep: 6 ms

Table 2: CuRPA operating modes.

Communication

The FPGA is directly connected to transmit and receive lines that have been magnetically isolated by the transceiver chip from the differential pairs coming into the board. The FPGA is always able to receive bytes. An entity in the FPGA uses its 10 MHz clock to implement one of

a selectable number of baud rates, 115200 in this case. Bytes that are sent via UART to the FPGA are always stored in a 128-byte FIFO. In addition, a 128-byte FIFO is used to transmit bytes: to send data, the CuRPA loads bytes into the FIFO that are immediately transmitted on the UART. A flag indicates when either FIFO is full, though this error condition is unlikely to occur because bytes that are received are read and interpreted immediately. There is ample time between successive points in the RPA sweep for all four data bytes that comprise one point on the I-V curve (two for a 16-bit current sample and two for a 16-bit voltage sample) to be transmitted before the next point begins. In addition, the receive FIFO includes an output that encodes how many unread bytes are currently stored.

Command Bytes

There are five bytes sent to the CuRPA from the flight computer interface board every second. These bytes signify the start of a retarding grid sweep. Table 3 lists all of the bytes received at the start of a sweep. The first is a start byte, the next two are the 16-bit step size sent to control the DAC, the fourth is the number of points in the sweep, and the last is the mode-setting byte, which determines whether the retarding voltage is updated linearly, nonlinearly as in a "smart" sweep, or is held constant (ion trap mode).

In the case of a linearly increasing retarding voltage, the step size is simply added to the retarding voltage for each data point. In the ion trap mode where the retarding voltage is held constant, the grid is set to the value given in the step size bytes for the entire sweep. In the case of the "smart" sweep, the grid is set to pre-defined values that are stored in the FPGA. The number of points in a sweep can be 32, 64 or 128, surpassing the 16-point requirement. There are 128 pre-stored 16-bit voltage values for the smart sweep. In the case of a 64-point smart sweep, the retarding grid updates to every other one of these values, and in the case of the 32-point sweep it updates to every fourth value.

In addition, one bit in the mode byte selects whether the second retarding grid voltage is swept along with the first retarding grid, or whether it is set to 0 V. In the case of the ion trap mode where the retarding grid is not swept, this bit still selects whether the second retarding grid is held at the same potential as the first retarding grid or whether it is held at zero.
The sweep cadence is once per second, so each CuRPA voltage sweep must occur within this period, which is in accordance with the maximum two-second sweep time requirement. When the CuRPA is idle, a start byte (10101010) signifies to begin a sweep; any other byte sent to the CuRPA when it is idle will be read and ignored. Once it receives a start byte, the CuRPA waits until the FIFO count reads four, indicating that there are four bytes stored in the FIFO. It then reads these four status bytes and stores all the information pertinent to the sweep. While the FPGA is performing a sweep it ignores any other bytes that are sent to it, even a start byte, unless it is a byte signaling synchronous reset. A standard reading procedure to illustrate this functionality is shown in Appendix C.

Byte #	Byte	Purpose	Possible Values
1	Start	Signals Start of Sweep Commands	10101010
2	Step(15:8)	Functions either as the step size in a linear sweep, or retarding grid voltage in constant sweep. The 16-bit value corresponds to a voltage of which there are 2^{16} steps on a 0-12V scale. For example, if the step size were 512 (2^{16}/128), this would give equal steps for a 128-point sweep over the full 0-12V range.	Any
3	Step(7:0)		
4	Points Per Sweep	Define number of points in the following one-second sweep.	32, 64, 128
5	Mode(bits 0:1)	Specifies how the retarding grid voltage values in the sweep are incremented.	0: Linear Steps.
			1: Constant value.
			2: Pre-defined "smart" voltage values.
	Mode(bit 2)	Specifies whether RG2 voltage is swept with RG1 or whether RG2 remains at ground.	0: RG2 voltage is swept. 1: RG2 remains at ground.

Table 3: Command bytes uplinked to the CuRPA.

Serial Interfaces

The communication between the ADC and DAC converters and the FPGA is accomplished through serial interfaces. The FPGA sends 16-bit values to the DAC using the 10 MHz system clock. When it is time to update a grid voltage in a sweep, the FPGA sends a command to the DAC including the channel it is updating (which can be 0 for RG1 or 1 for RG2) and the 16-bit value to which it is updating. In the case of a linear step, the step size is added to this value after each point. In the case of the smart sweep, this becomes the next indexed value. A DAC command transmission is shown in Appendix C and takes 2.8 μs.

The FPGA also divides the clock by 4 to generate a 2.5 MHz clock to interface with the ADC, performing 16-bit conversions at a maximum rate of about 90 kHz. The FPGA sends an 8-bit command indicating which channel to sample. This 8-bit command is followed by 17 cycles of the 2.5 MHz system clock in which the ADC samples and transmits its input voltage. In total, an A/D conversion takes 10.8 μs and is shown in Appendix C. When the FPGA is accumulating current samples in each sweep point for the oversampling, or taking housekeeping samples, it begins the next ADC conversion just after clocking and accumulating the data from the previous sample.

Housekeeping Samples

Before the sweep begins, and after it has just read the five command bytes, the FPGA steps through all nine of the housekeeping values and sends them back through the UART. All of the housekeeping data are communicated through channel 3 of the ADC. The FPGA controls a multiplexer to specify which housekeeping word is selected, and sequentially reads all nine housekeeping samples. These samples specify various temperatures and voltage monitors, as shown in Table 4. It changes the multiplexer-select outputs and then takes a sample from ADC

channel 3, eight times, stepping through all the channels, to measure the temperatures and voltage monitors on the board. After reading the housekeeping data, the program samples ADC channel 2, the suppressor grid. Because there is a buffer between the analog-output multiplexer and the ADC housekeeping input, the FPGA waits 34 μs for the buffer to respond between changing the multiplexer-select bits and taking the ADC sample for each housekeeping value. Once all nine 16-bit housekeeping values have been taken and sent back through the UART, the RPA sweep begins. A housekeeping sampling procedure is shown in Appendix C.

Housekeeping Value	Expected Value
Temperature 1	1.189 (at room temp.)
Temperature 2	1.189 (at room temp.)
Temperature 3	1.189 (at room temp.)
Daughter Board Temperature	1.189 (at room temp.)
15VMon	1.922
5VMon	2.5
3.3VMon	2.877
Voltage on Retarding Grid 2	0
Output of DAC that Feeds Suppressor Grid (Not Used)	0

Table 4: Housekeeping values measured by the CuRPA.

Timing

The FPGA must be able to properly time the retarding voltage grid updates and current samples so there is enough time for the system to respond after the grid voltage is changed, while maximizing the current oversampling for the selected number of points per sweep. A diagram of the timing of a 128-point sweep is shown in Figure 6. To improve the fidelity of the measurements the current is oversampled by 1024, 512 and 128 for the 32-, 64- and 128-point sweeps, respectively. The oversampling must be a power of 2 to allow for easy division in the FPGA. These are the maximum oversampling ratios possible that allow an entire sweep to be performed within a 1-second period. Between setting the DAC and taking current samples for each point, the FPGA waits 6.35 ms for the 128-point sweep and 12 ms for 64- and 32-point sweeps. After the bytes are received, the nine housekeeping values are sampled, which takes about 373 μs. For each point in the sweep, the FPGA sends a command to the DAC telling it to set the retarding grid to the next voltage in the sweep. After setting the grid voltage, the FPGA waits for the logarithmic amplifier to respond. After 6.35 ms or 12 ms (depending on the number of points per sweep) the FPGA oversamples and averages current samples. When this is complete, it takes one sample of the voltage on the retarding grid (ADC channel 2), and then reconfigures for the next sample by setting the DAC (retarding voltage) to its new value. It repeats this process until it has taken as many points as were commanded by the start bytes. This takes a different amount of the time for each sweep: 993 ms for the 128-point sweep, 947 ms for the 64-point sweep and 738 ms for the 32-point sweep. The beginning of a 128-point smart sweep, and an entire 32-point sweep, are shown in the FPGA simulation in Appendix C.

Resets

Asynchronous reset is accomplished by a low pass filter on the 3.3V supply that rises slowly (approximately 0.6 s) and is routed through a set of Schmidt trigger inverters. When the RPA is turned on, the asynchronous reset input is held low until the filter rises, and the system is able to start up after resetting. In addition, a synchronous reset command can be sent to the CuRPA at any time, which will initiate a full reset of the system.

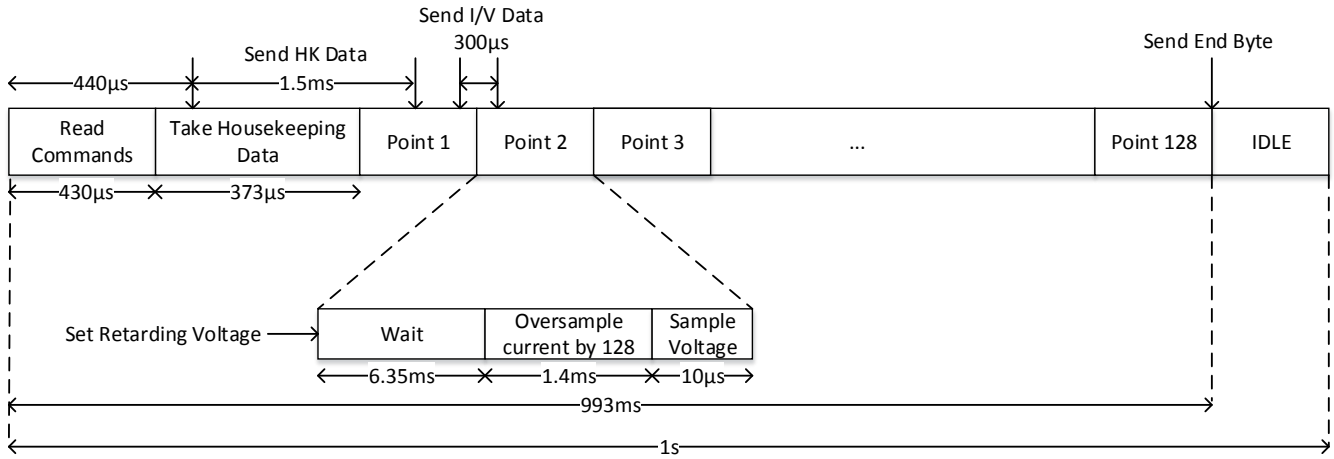

Figure 6: Timing diagram of 128-point CuRPA sweep

Chapter 5: Validation

Performance Summary

A photo of the assembled CuRPA board from the top view is shown in Figure 7. A summary of the CuRPA performance compared with its requirements, based on the specifications of its parts, is shown in Table 5. These parameters are for a specific mission scenario. It is easy to change several of the parameters given a different mission scenario. For instance, the sweep time and points per sweep can be changed easily by using a different FPGA design. The resolution can be improved by oversampling and averaging to add more bits of precision, or by using a different ADC. The voltage ranges of the grids and the suppressor can be changed by changing amplifier gains. The current range can be changed by adjusting the logarithmic amplifier bias current or adjusting the gain on the amplifier's output.

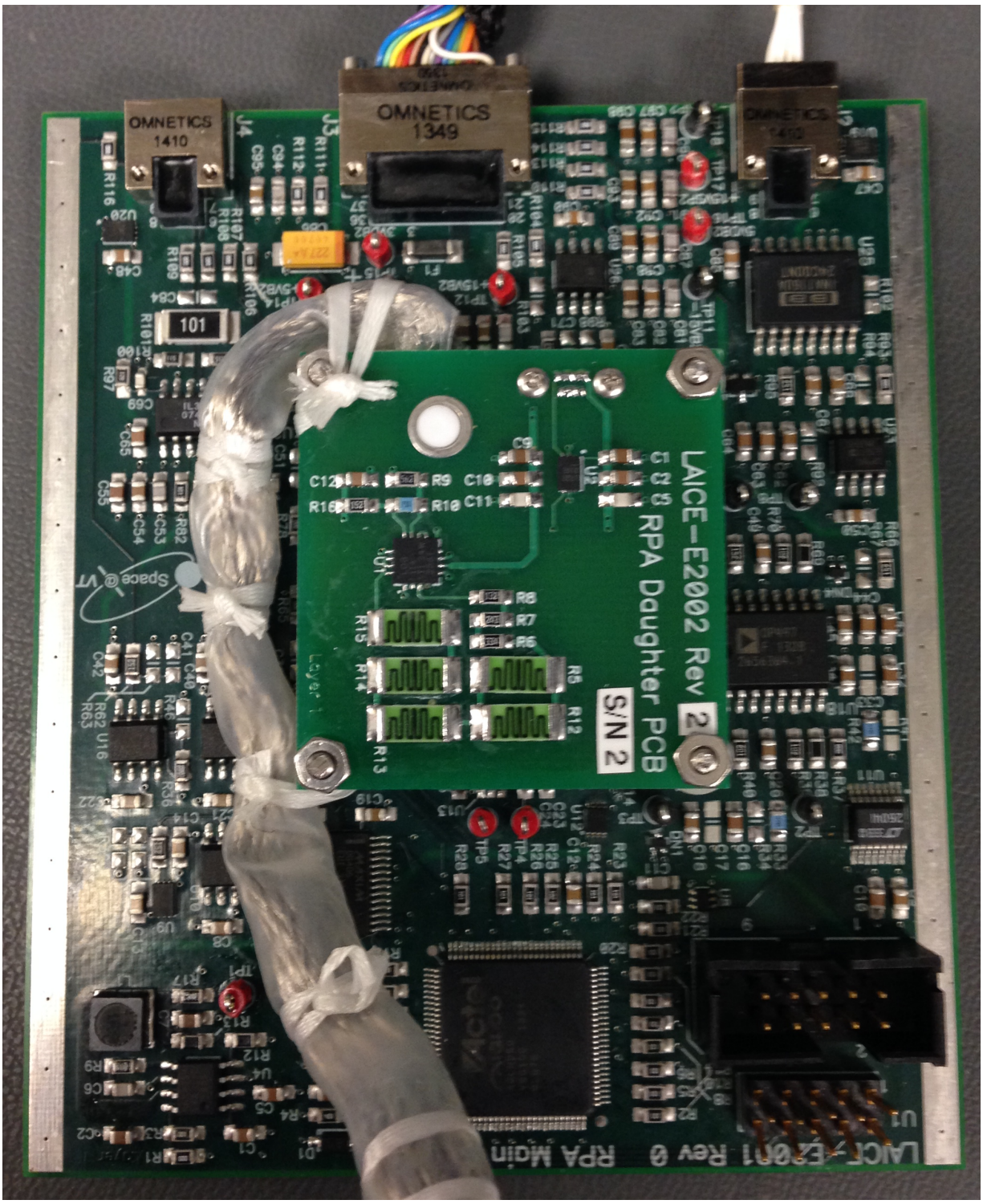

Figure 7: Photo of assembled RPA electronics boards from the top.

Parameter	Requirement	Specification
Measured Current Range	500 pA to 5 µA	100 pA to 50 µA
Measured Current Accuracy	Greater of 500pA or 2.5%	0.97pA to 370 nA (0.01%-0.7%)
Samples per I-V Curve	16 or More	128
I-V Curve Sweep Time	2 s or Less	1 s
Retarding Voltage Range	10V or More	12V
Suppressor Bias	-5V or Less	-12V
Dimensions	Less Than 9.5 cm x 9.5 cm x 5 cm	7.6 cm x 7.6 cm x 5.82 cm
Weight	Less than 0.5 kg	0.4 kg
Power	Less than 0.5 W	0.466 W
Operating Temperature	-20° C to 75° C	-20° C to 85° C

Table 5: Summary of CuRPA performance.

Bench Testing

The first testing that was performed on the main board was a bench test run-through to validate all the hardware and the FPGA. After the RPA was plugged in to power supplies, the external power supplies were verified on the board, and the 1.25 V and 1.5 V board-generated power supplies were verified. The amplifier between the daughter board output voltage and the ADC input was also verified, with the transfer function shown in Figure 8.

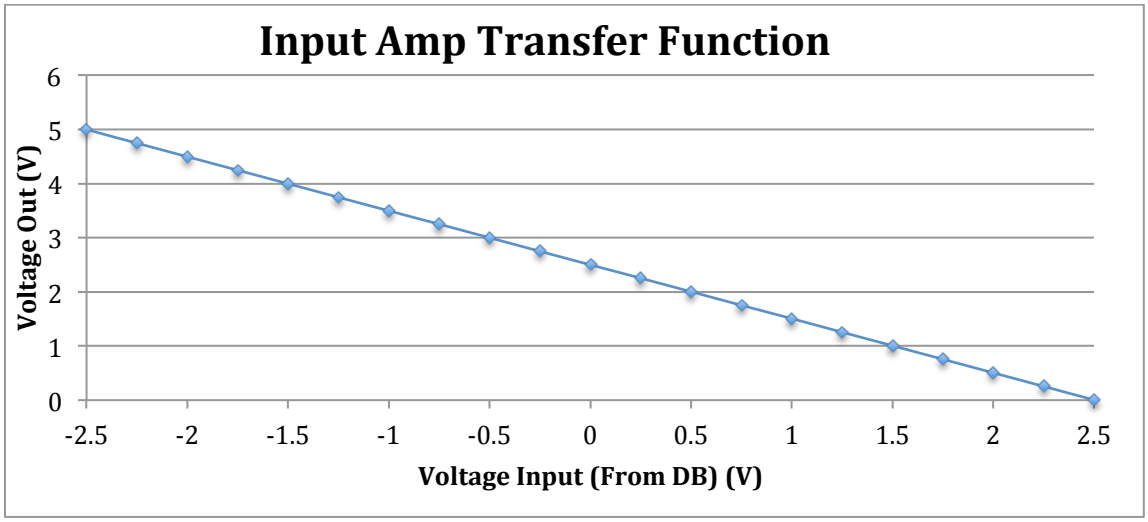

Figure 8: Transfer function of the input amplifier from the daughter board to the ADC.

The DAC, ADC and multiplexer were tested by loading the FPGA with a design specially made for debugging. With this FPGA design, individual UART commands were able to control each part on the board separately, rather than all the parts being controlled together as in one sweep. The ADC was tested by sending commands to sample different channels and return one 16-bit sample. Channel 0 was tested by changing the daughter board input voltage and reading the ADC measured values corresponding to each input. Channel 2 measured 0 V, which is correct because the suppressor grid is externally set in this case and not controlled by the DAC. Channel 3 of the ADC and the multiplexer were tested by commanding the FPGA to choose a channel by setting the multiplexer-select bits, and then measuring channel 3 of the ADC. The ADC measurements corresponded to the selected multiplexer output chosen by the FPGA. The DAC was tested by sending commands to write different 16-bit values to channel 0 or channel 1. ADC channel 1 was then tested by taking samples for different grid voltages set by the DAC. The grid voltage outputs were measured by an oscilloscope to show the rise time of the DAC outputs, which must be compliant with the 6.35 ms waiting time in the 128-point sweep. An oscilloscope capture of the grid voltage after the 0xFFFF is written to the DAC is shown in Figure 9. The figure shows that the voltage output of the grid rises to 12 V in about 2.5 ms.

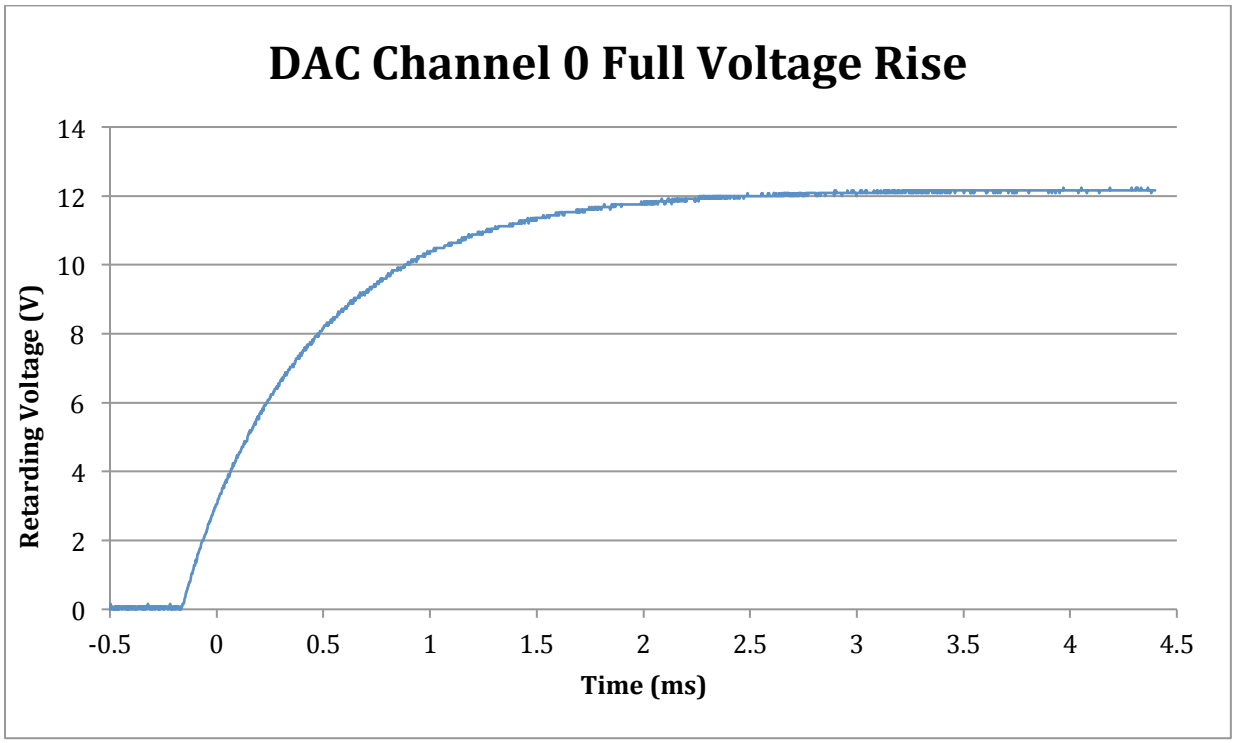

Figure 9: Grid voltage rising after values are written to the DAC.

After verifying the board functionality at the component level, the final FPGA design with sweep functionality was loaded onto the FPGA. For these tests, the daughter board voltage output was set to a constant voltage (-2.5 V or 0 V) and the daughter board temperature measurement output was set to 0 V. For all sweep modes an oscilloscope was used to capture the changing grid voltage in time. The data from each sweep were analyzed, and it was verified

that the current samples returned remained constant for each setting and corresponded to the value of the daughter board output voltage. This test also confirmed that the voltage values agreed with what was measured by the oscilloscope. Figures 10-21 show the linear and smart sweeps for all numbers of points, both the 0-5 V values measured on the CuRPA board during the sweep and the grid voltages measured independently by the oscilloscope.

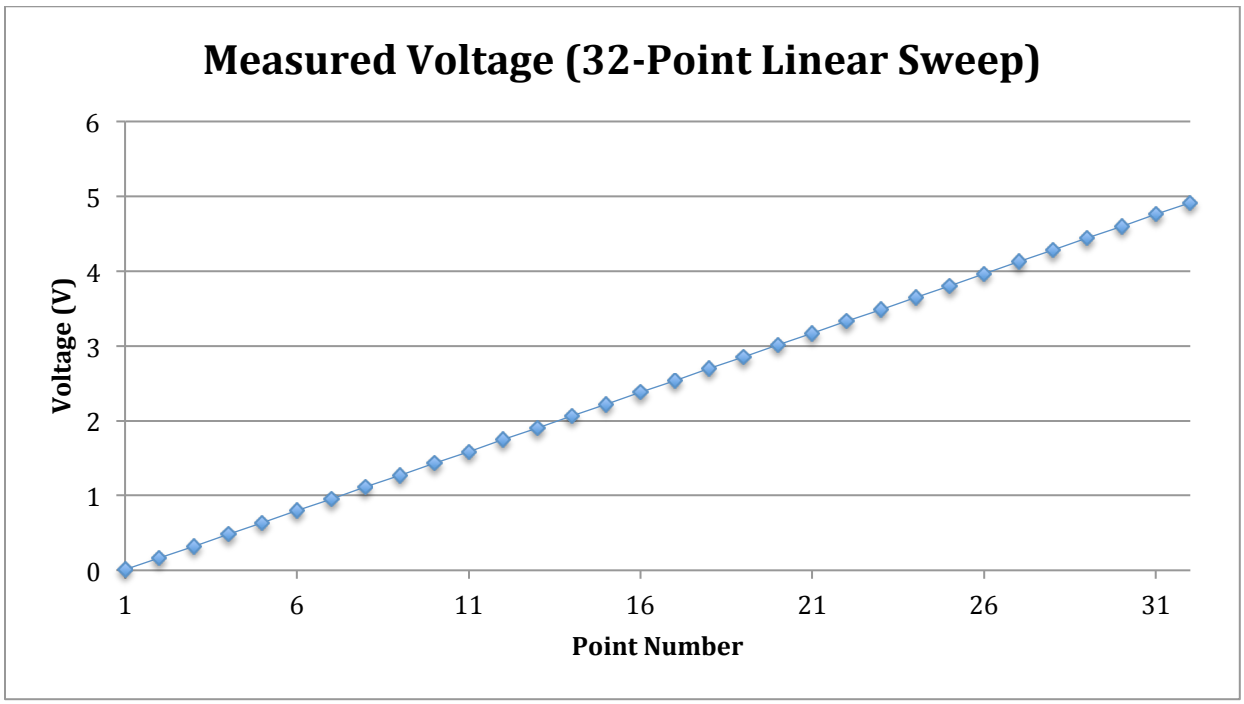

Figure 10: Voltage data from the circuit board during a 32-point linear sweep.

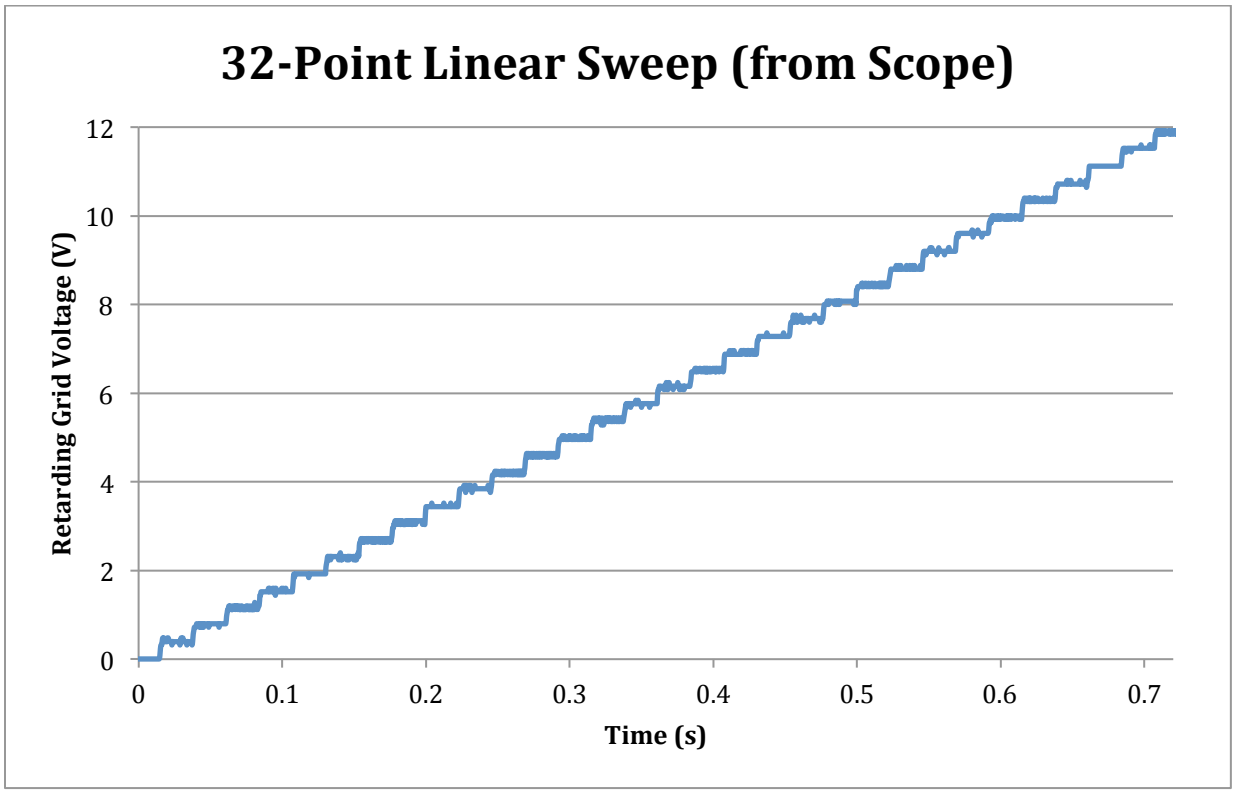

Figure 11: Oscilloscope measurements of retarding grid voltages during a 32-point linear sweep.

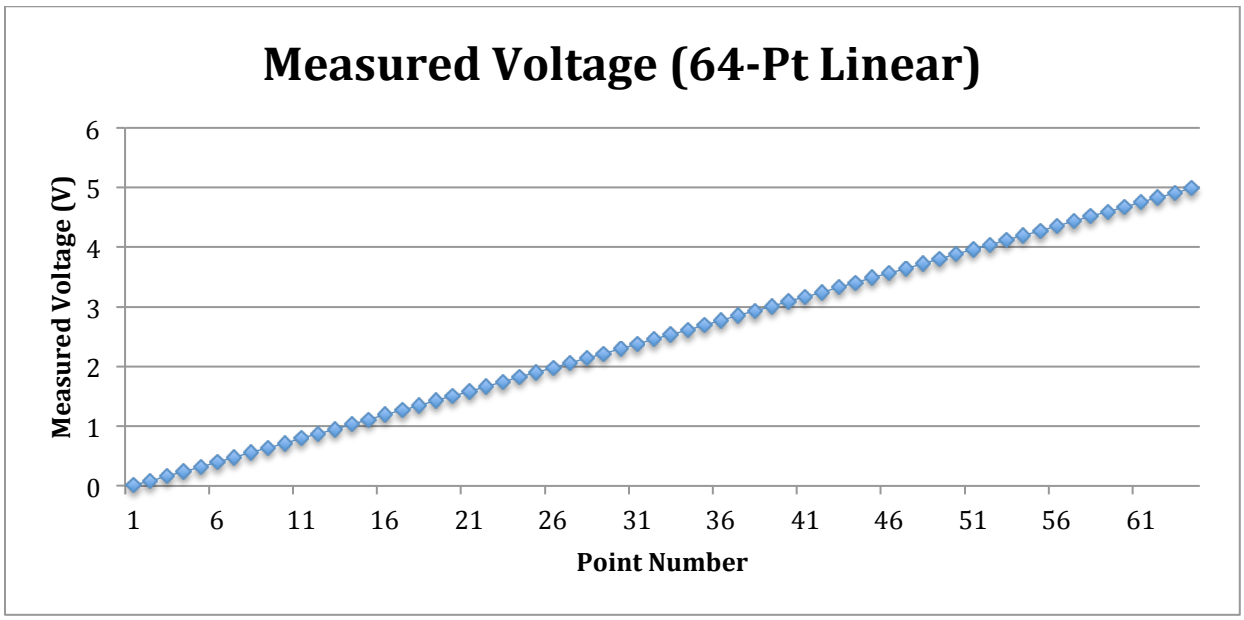

Figure 12: Voltage data from the circuit board during a 64-point linear sweep.

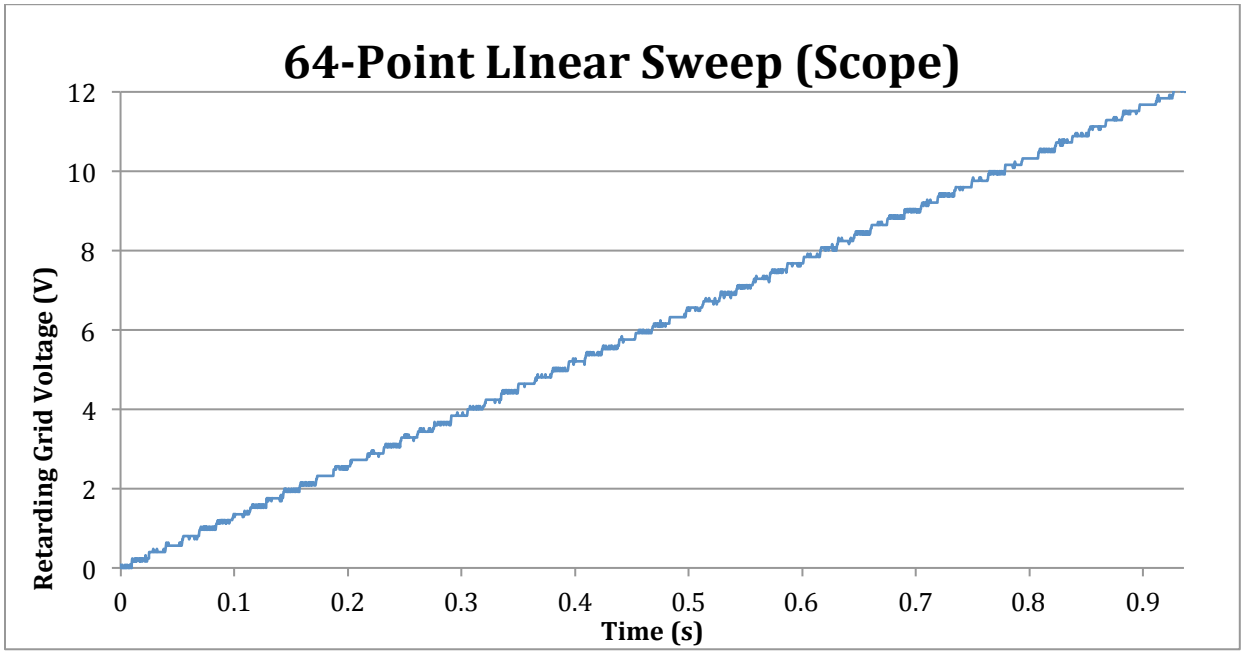

Figure 13: Oscilloscope measurements of retarding grid voltages during a 64-point linear sweep.

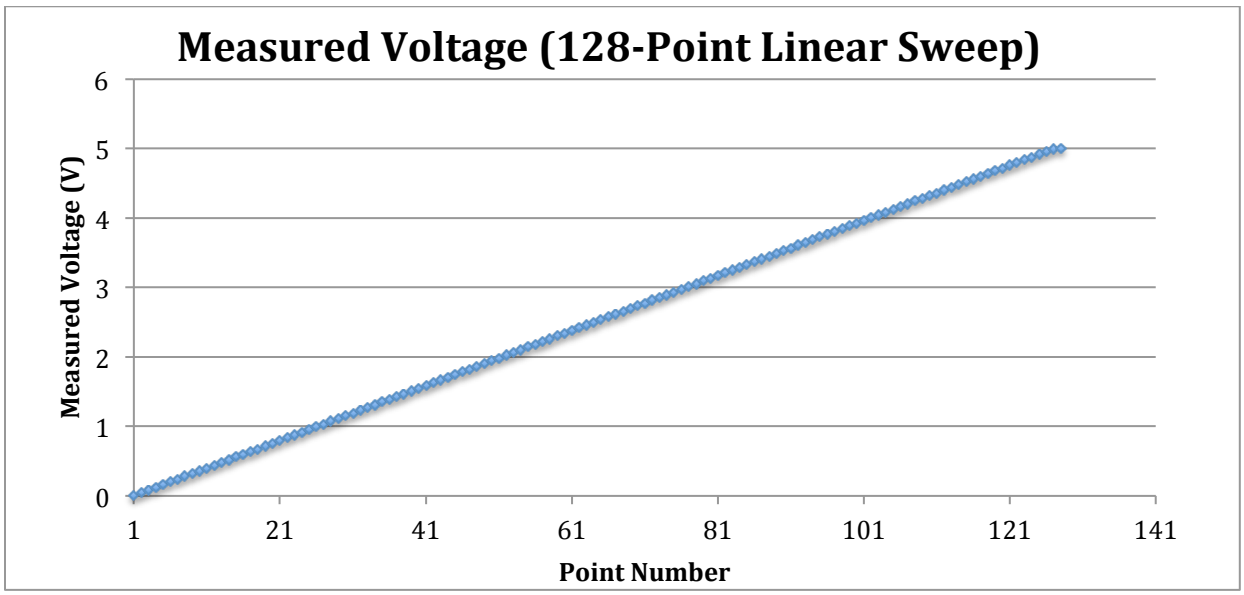

Figure 14: Voltage data from the circuit board during a 128-point linear sweep.

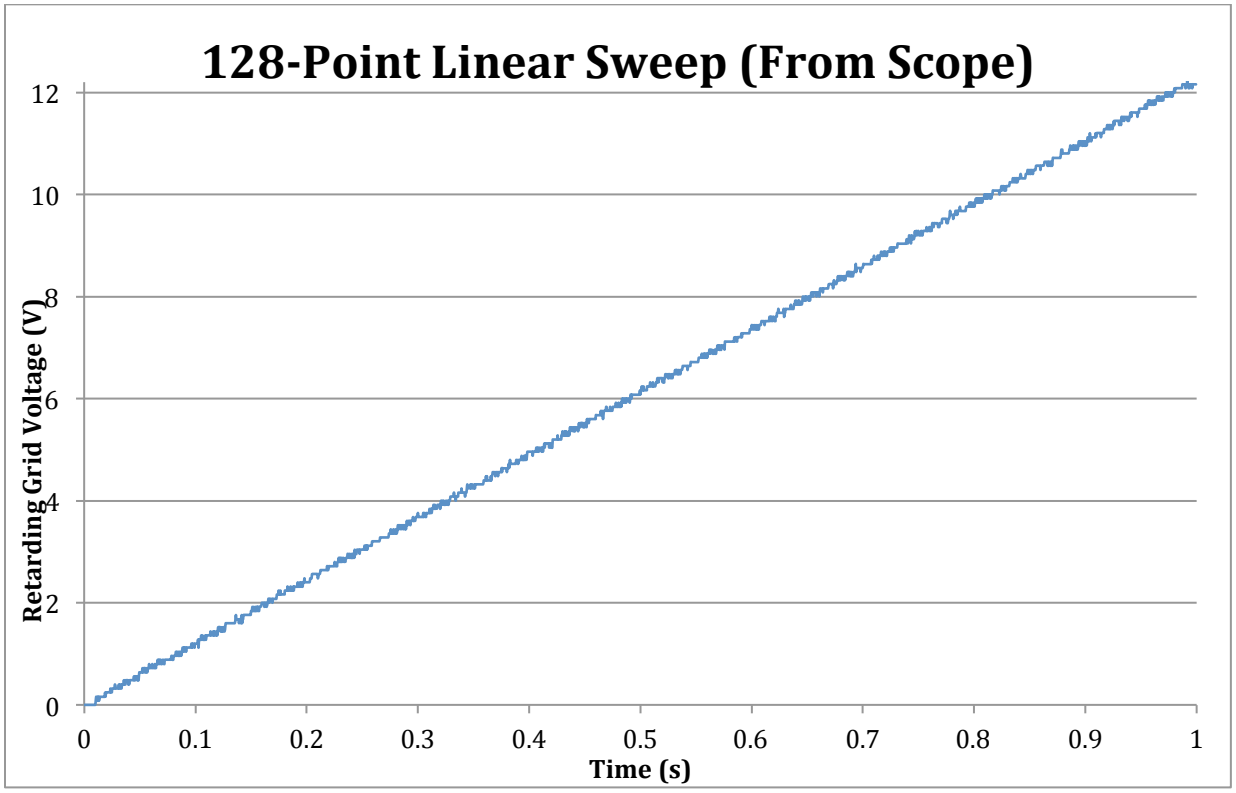

Figure 15: Oscilloscope measurements of the retarding grid voltage during a 128-point linear sweep.

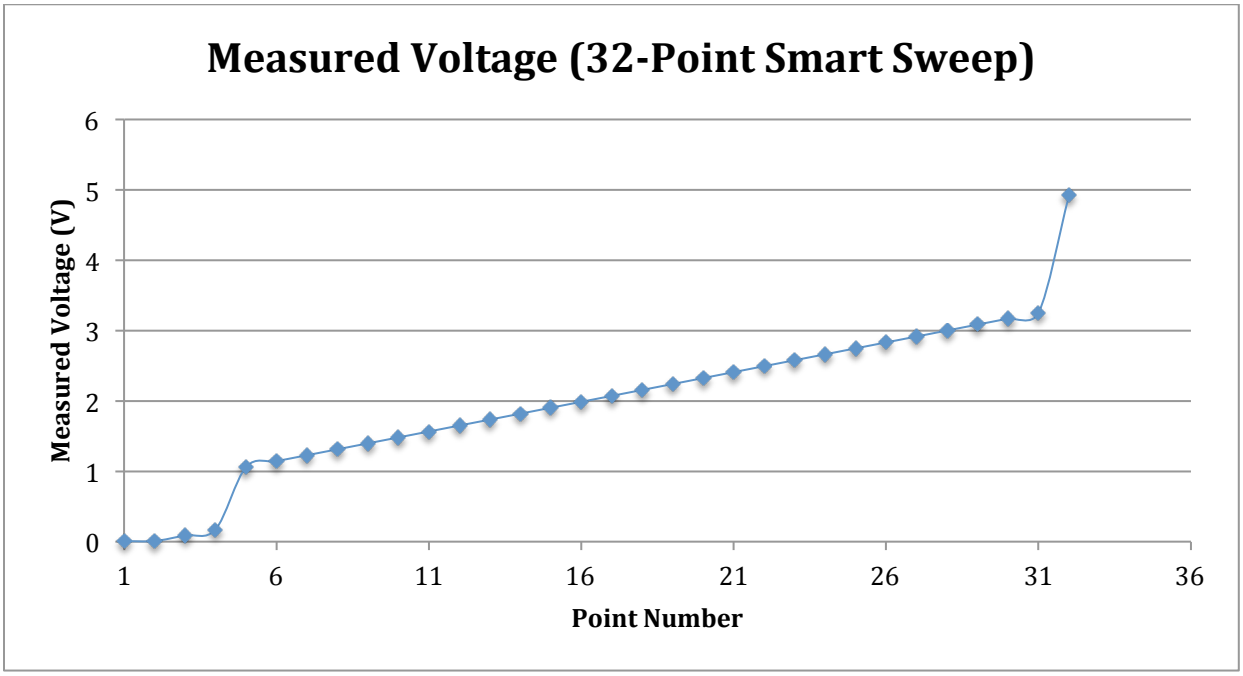

Figure 16: Voltage data from the circuit board during a 32-point "smart" sweep.

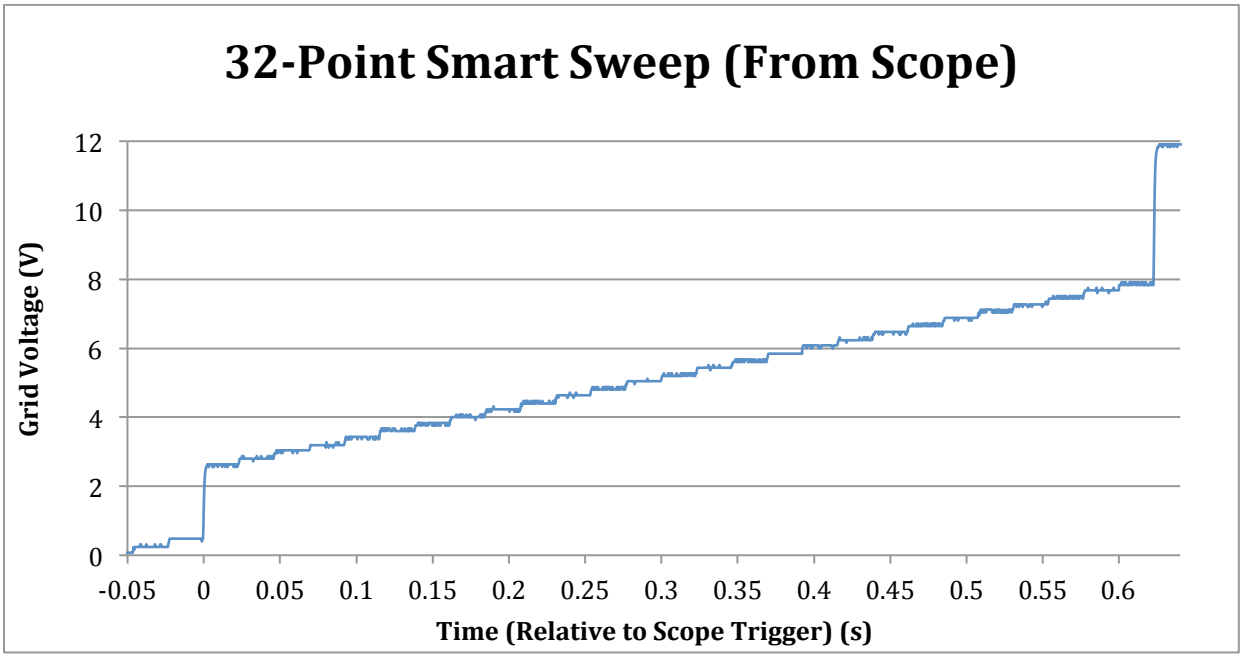

Figure 17: Oscilloscope measurements of the retarding grid voltage during a 32-point "smart" sweep.

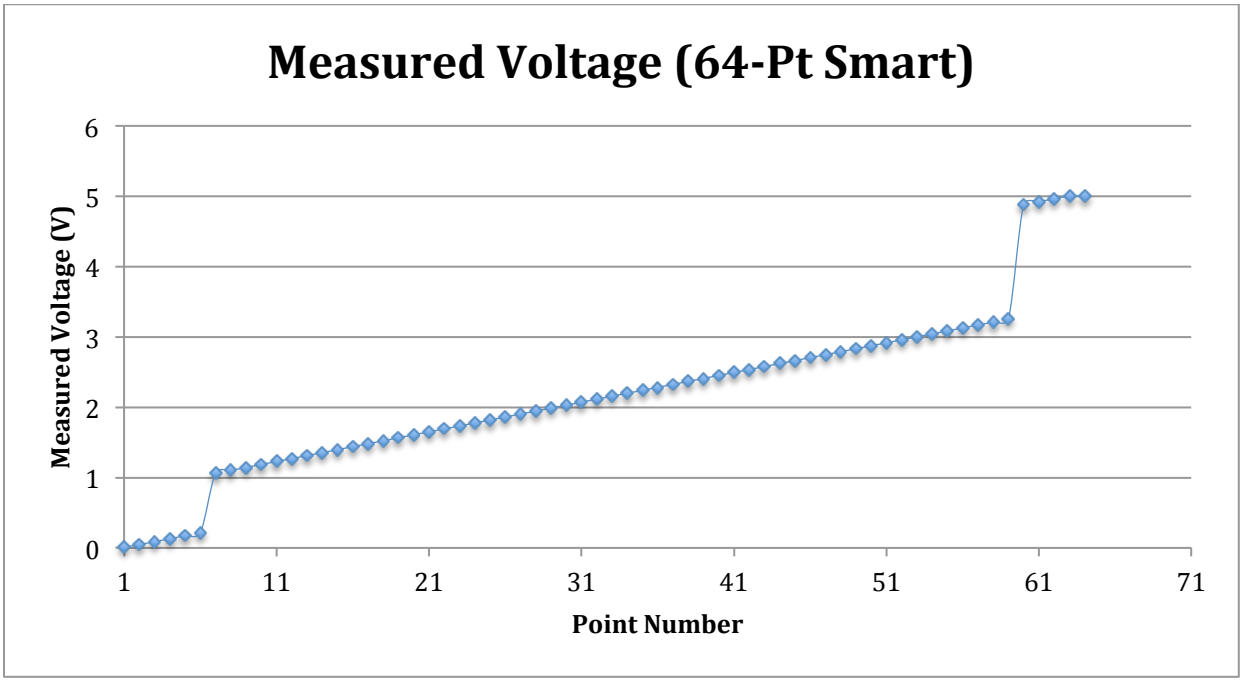

Figure 18: Voltage data from the circuit board during a 64-point "smart" sweep.

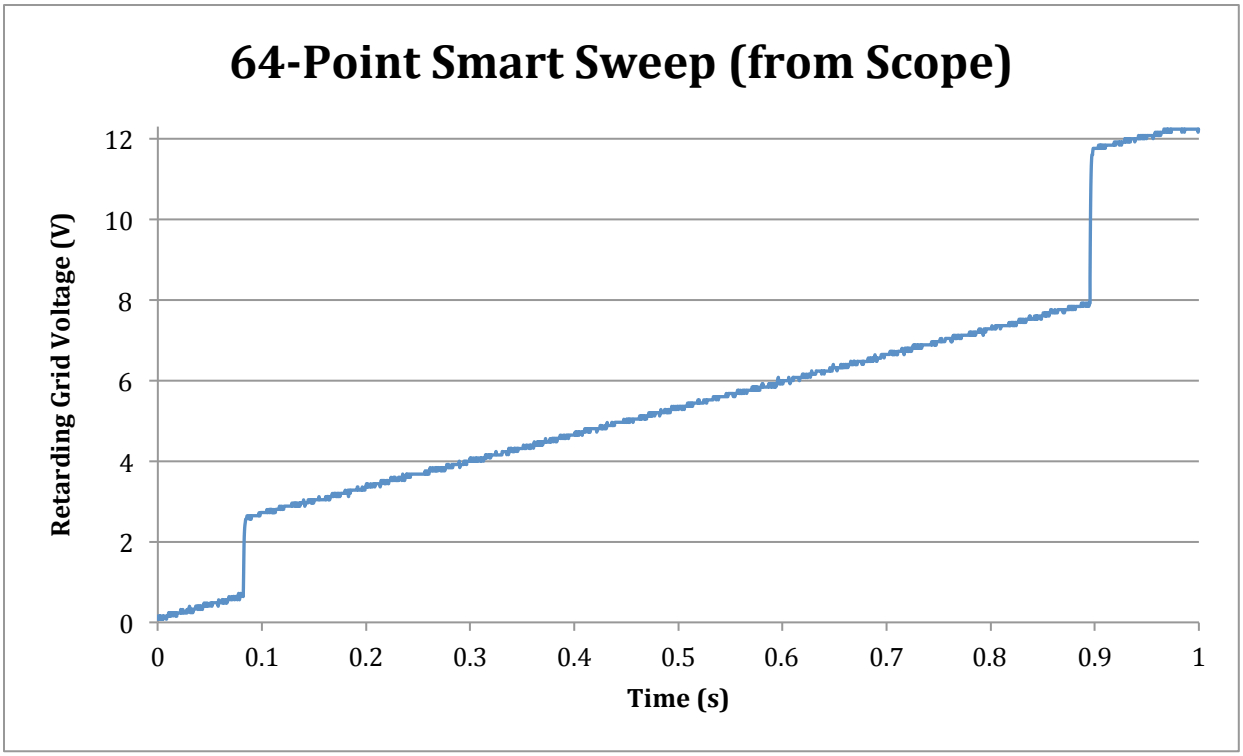

Figure 19: Oscilloscope measurements of the retarding grid voltage during a 64-point "smart" sweep.

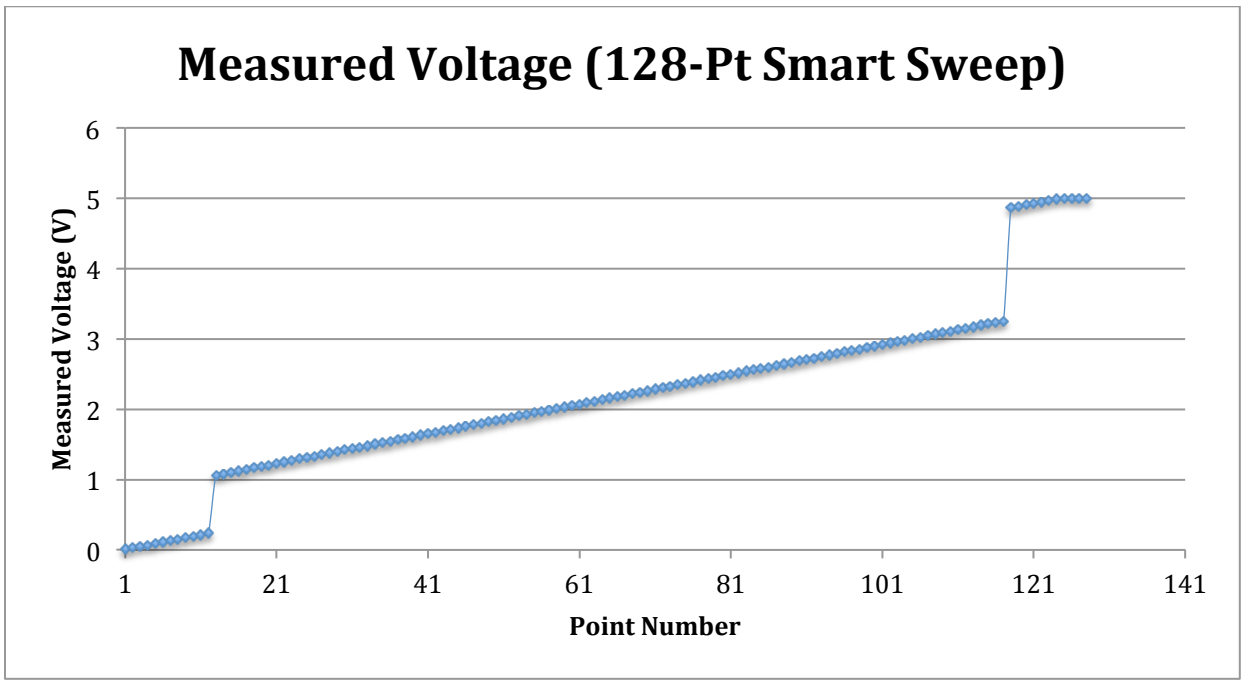

Figure 20: Voltage data from the retarding grid during a 128-point "smart" sweep.

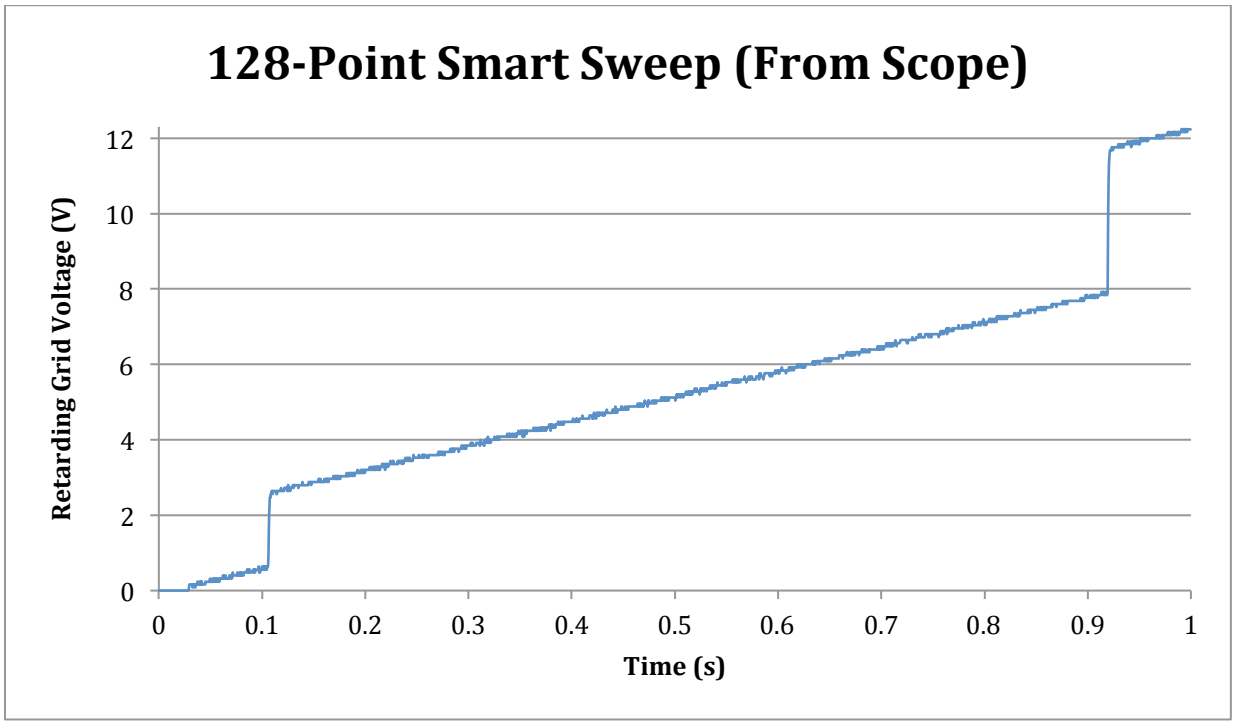

Figure 21: Oscilloscope measurements of the retarding grid voltage during a 128-point "smart" sweep.

The ion trap sweep settings were tested by sending commands to perform fixed-voltage ion trap sweeps with various retarding grid voltage settings and observing that the grid voltage remained constant at the expected value throughout the sweep. In addition, the functionality of

the select bit indicating whether to sweep the second retarding grid or set it to zero was tested by monitoring both grids for each setting.

The housekeeping values were verified as well. Some testing was required to find the amount of waiting time between changing the multiplexer select bits and taking the ADC sample, and 34 μs was selected as the smallest time that gave the buffer following the multiplexer enough time to respond before the sample was taken. Table 6 lists the measured and expected values of the housekeeping samples, which gave the same measurements in all the sweeps.

Housekeeping Value	Measured (V)	Deviation From Expected (V)
Temp1	1.197	0.008
Temp2	1.189	0
Temp3	1.190	0.001
DB Temp	0	0 (input grounded for this test)
15VMon	1.915	0.007
5VMon	2.54	0.04
3.3VMon	2.86	0.02
RG2	0.005	0.005
SG	0.024	0.024

Table 6: Measured housekeeping values and deviation from expected values.

Vacuum Testing

A diagram of the vacuum chamber test set-up for the CuRPA is shown in Figure 22, and a photo of the CuRPA and ion source inside of the chamber is shown in Figure 23. The vacuum chamber contains an ion source directed at the CuRPA grids. The CuRPA grids are connected to the main board for voltage control, and the collector plate is connected to the CuRPA daughter board. The power and communication lines of the CuRPA are wired through a connector in the wall of the vacuum chamber to external voltage sources and a computer for power and control. The voltage sources and computer emulate the spacecraft bus interface. Both the main board and daughter board are housed in the metal enclosure located beneath the CuRPA sensor, as can be seen in Figure 23.

The ion source in the vacuum chamber works by ionizing neutral gas with electrons that are emitted by filaments. The electrons from the filaments are electrostatically directed and travel towards a metal disc that is held at positive potential, which causes them to travel through neutral gas and ionize it. These ions are then repelled by the metal disc and flow through an opening out of the source. By changing the potentials within the source the distribution of

emitted ions can be controlled. The ion density can also be increased by increasing the pressure in the chamber.

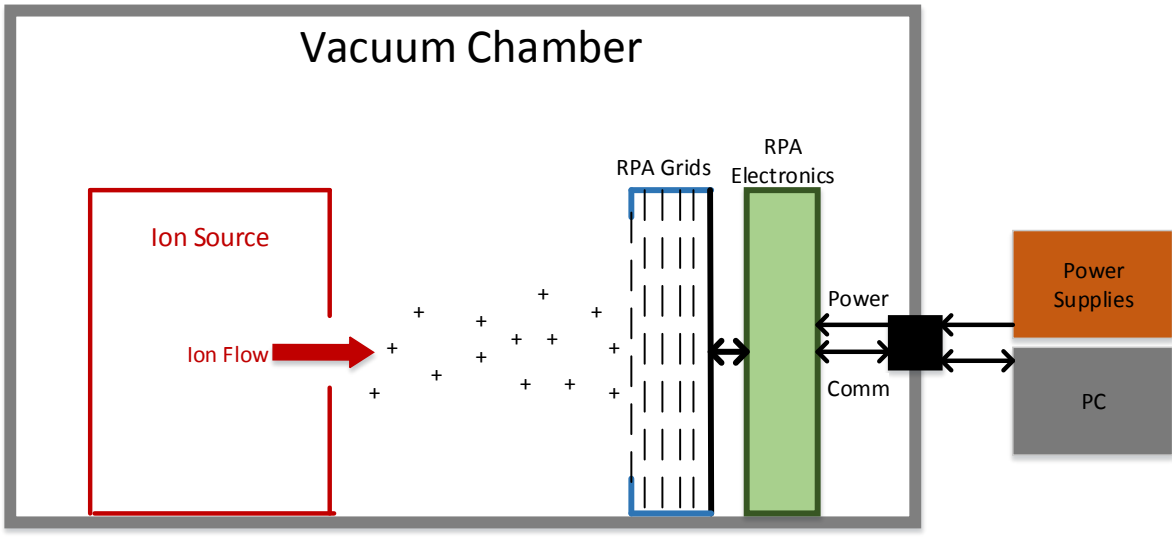

Figure 22: Vacuum chamber test set-up of the CuRPA.

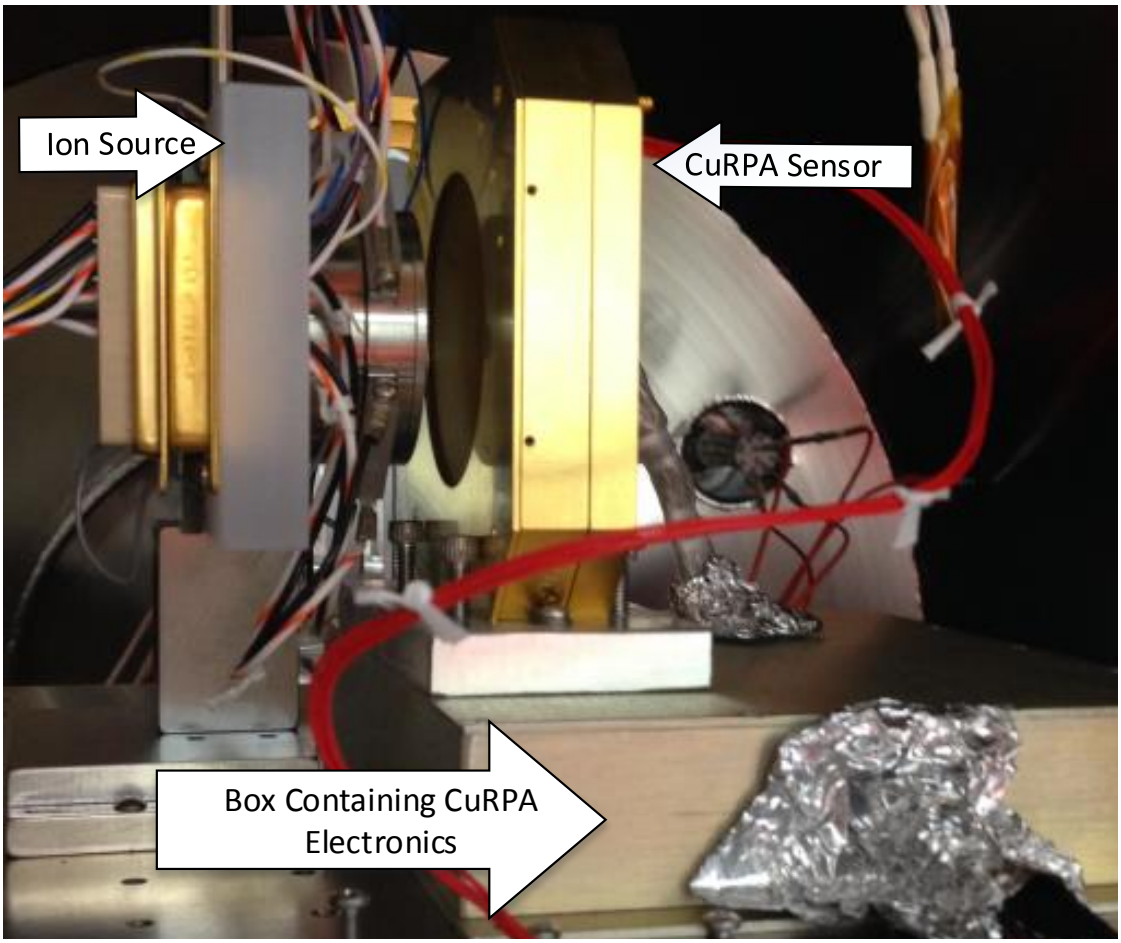

Figure 23: Photo of CuRPA in front of ion source inside of the chamber.

The first CuRPA sweep performed in the chamber was a 128-point linear sweep with a retarding voltage ranging from 0 to 12V with the ion source disabled. This test characterized the noise level of the CuRPA in the chamber without any current input to the instrument, indicating the noise level within the instrument. Figure 24 shows a graph of the 128 current measurements taken over the one-second sweep. Noise due to the instrument did not exceed 5 pA in the chamber.

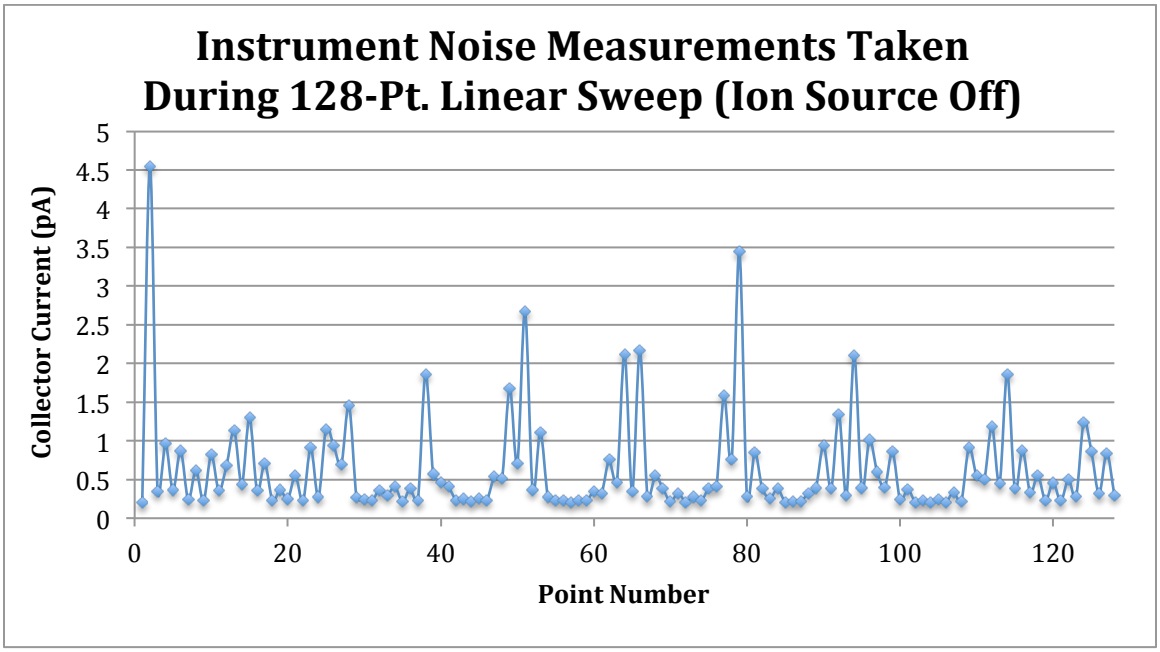

Figure 24: Currents measured during a 128-point 0-12 V linear sweep with the ion source off, indicating the noise level due to the CuRPA instrument alone.

The first test to validate functionality of the CuRPA was to measure the ion current emitted by the source for different pressures in the chamber. This was done by performing 128-point ion trap mode sweeps with the grid voltages set to 0V and averaging the 128 current measurements in each of those sweeps to provide a base measurement of the ion current for each chamber pressure. The suppressor was still held at -12V. Figure 25 shows the CuRPA current measurement for different pressures in the chamber. As expected, the measured current grows somewhat linearly with increasing chamber pressure. This indicated that the CuRPA was functional and able to capture ions and measure them as a current.

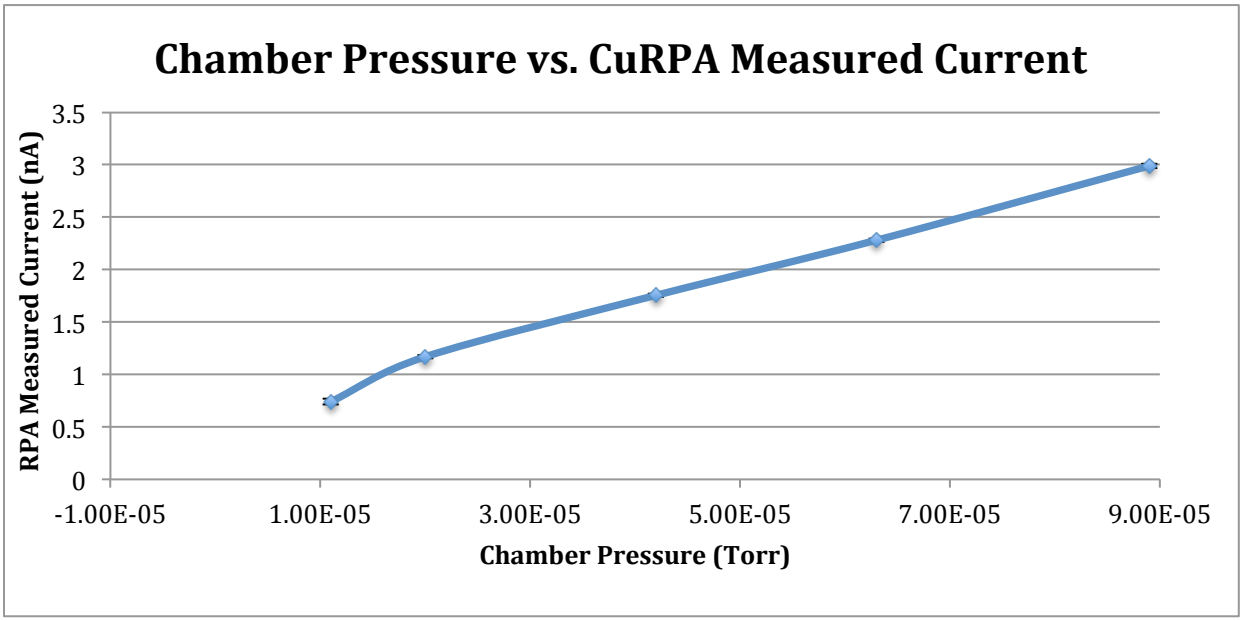

Figure 25: CuRPA current measurements (performed by taking the average current measured during a 128-point 0 V ion trap sweep) for different chamber pressures.

After basic functionality was verified, the CuRPA's ability to generate I-V curves was tested by running linear sweeps. The ions coming out of the source in the chamber were far lower in density and energy than the ions in the ionosphere would be if the CuRPA were on a satellite, so the retarding potential at which the current dropped in the curve was far lower than the 5-10 V range predicted in space. Initial tests showed the potential at which ions from the source were retarded to be around 60 mV. In addition, the distribution of ions emitted from the source caused them to have a much steeper drop-off than would be predicted by the Maxwellian distribution of ions in space. Figure 26 shows a representative 32-point linear sweep taken by the CuRPA in the chamber.

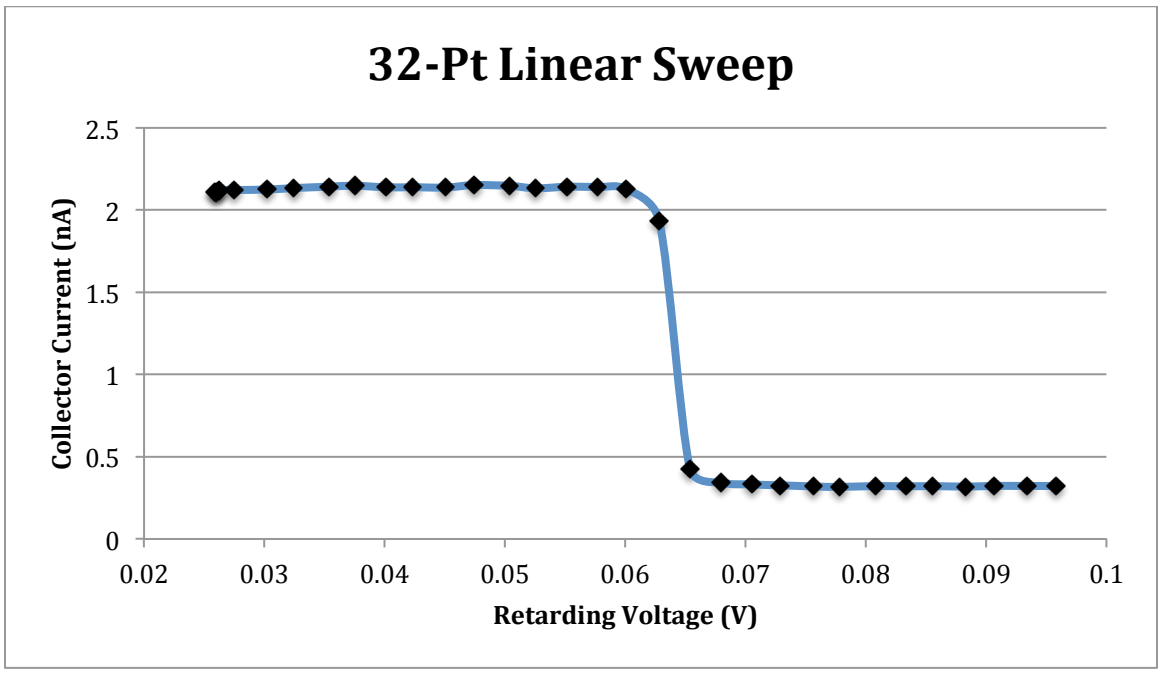

Figure 26: 32-Point linear sweep with retarding potential ranging from 0 to 0.08 V.

As evident from the I-V curve, the base level of current coming out of the ion source is slightly over 2 nA, and the ions get retarded at a potential slightly over 60 mV. The ~62 mV value at which ions are effectively retarded corresponds to an ion velocity into the aperture of ~650 m/s. The thermal velocity of the N_2^+ ions in the chamber is ~420 m/s. Thus in our chamber tests we have not simulated flight conditions accurately, which helps to explain the observed shape of the I-V curve. The ~300 pA current to which the I-V curve settles is a bias due to noise from the ion source. It is difficult to measure I-V points within the transition region during the 32-point sweep because it is so steep. The sweep modes with more points were better able to capture the transition region.

Figure 27 shows the I-V curve obtained by averaging the voltages and currents from eight 64-point linear sweeps.

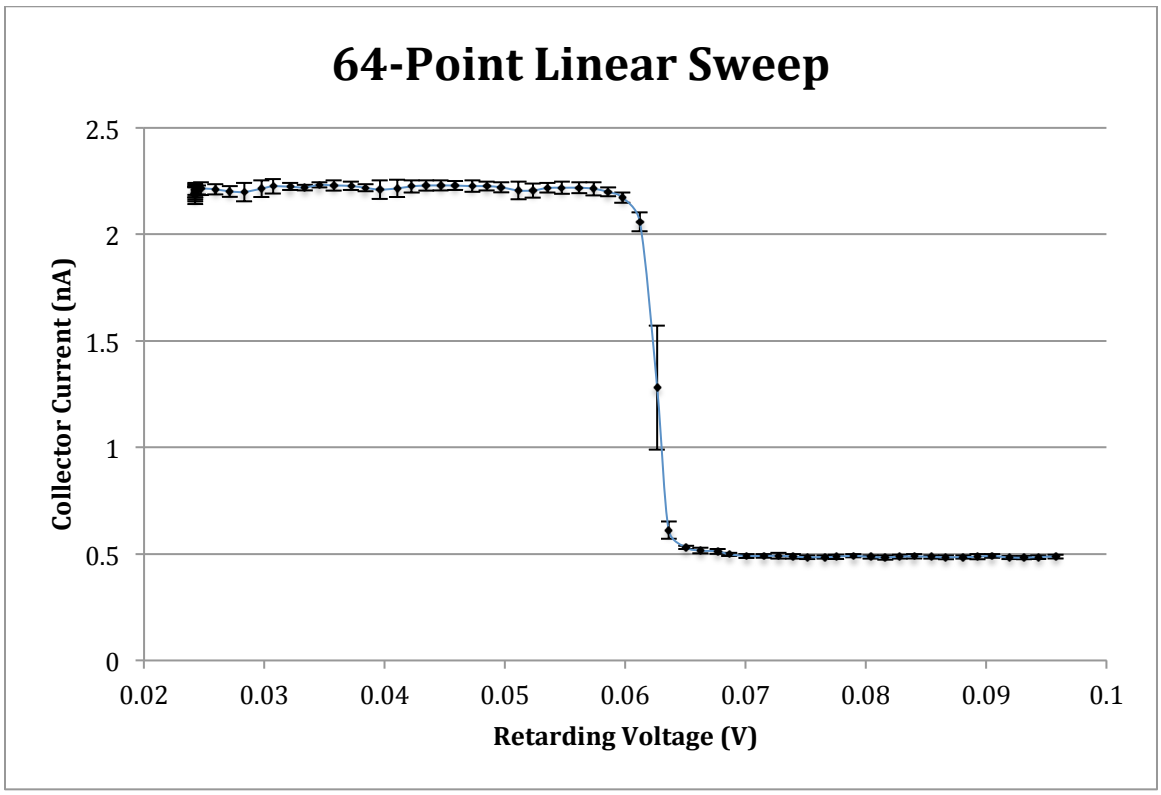

Figure 27: Average of eight 64-point linear sweeps from 0 to 0.09 V.

The error bars indicate the standard deviation of the measured current values across the eight 64-point sweeps. The standard deviation is high for the point in the middle of the transition range because the very slight differences in DAC output voltage between sweeps, due to normal amounts of noise and error, caused relatively large changes in current, because the slope of the I-V curve is so steep in that region.

Figure 28 shows the curve obtained by averaging five 128-point sweeps. It shows more points in the transition region, with the point in the middle having the greatest standard deviation, as explained above.

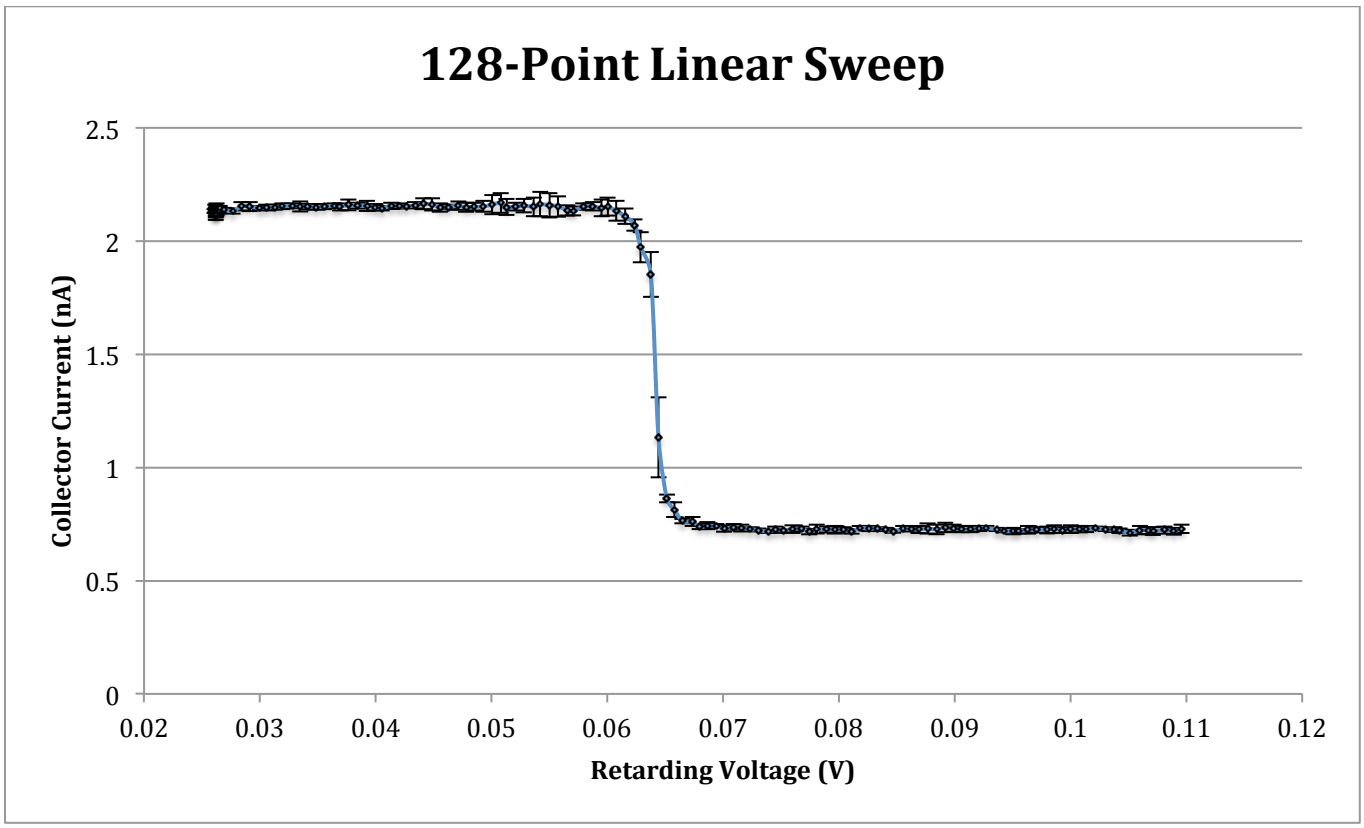

Figure 28: Average of five 128-point linear sweeps between 0 and 0.1 V.

The sweeps for all different numbers of points are very similar, and are reasonable I-V curves for conditions inside a chamber.

Chapter 6: Conclusions and Future Work

This thesis has detailed the electrical design of the first retarding potential analyzer for use in cubesats. Through both bench testing and vacuum testing, the basic functionality of the CuRPA was verified. The largest task to complete before this instrument can be used in flight is a full system calibration. The CuRPA was calibrated somewhat through bench testing, but tests need to be performed with a precision current source in a relatively noise-free environment before the error range of the CuRPA can be fully determined for all current inputs. Furthermore, the CuRPA needs to be tested with a more predictable ion source before it can be calibrated end-to-end.

One of the most important aspects of the CuRPA electrical design is that it is easily suited to many different specific applications. The current range, points per sweep, length of the sweep, and current oversampling ratio can all be easily changed depending on the mission scenario. A further test of the robustness of the CuRPA electronic design would be to change some of these parameters to make the CuRPA suitable for a different mission scenario and ensure that the CuRPA specifications hold.

Of course, the only way the CuRPA functionality can be fully verified is when the CuRPA is mounted on a satellite in the ionosphere. This is expected to occur in January 2016, when the CuRPA will see its first flight on the Lower Atmosphere Ionosphere Coupling Experiment (LAICE) cubesat.

References

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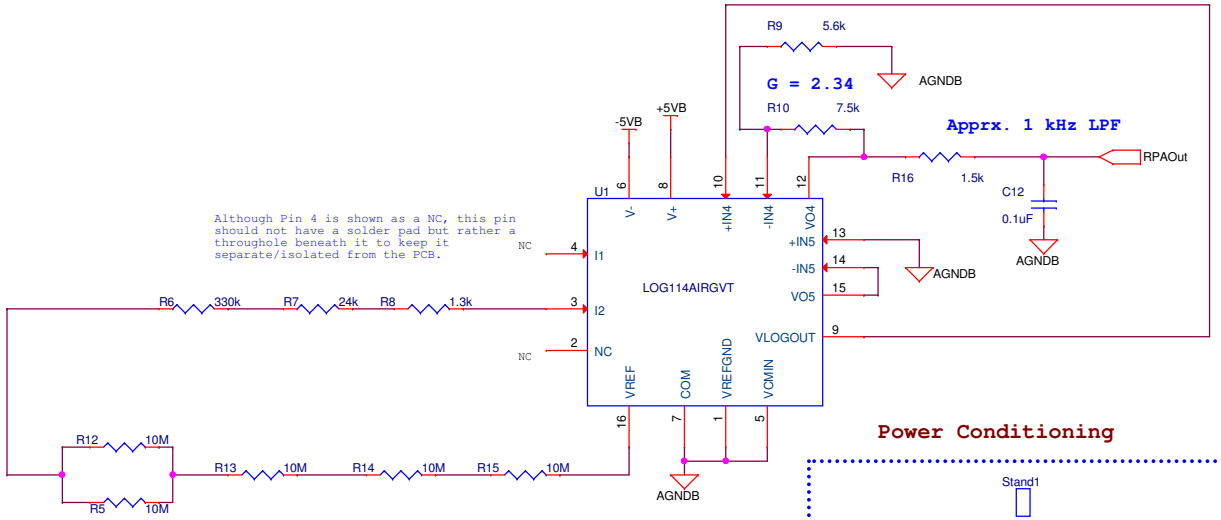
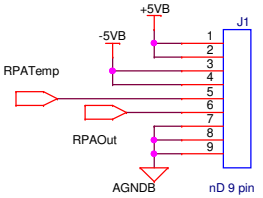
Appendix A: Schematics

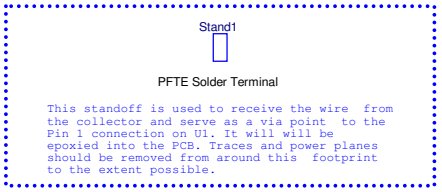
RPA Collector Transimpedance (I to V Log Amp) Transducer



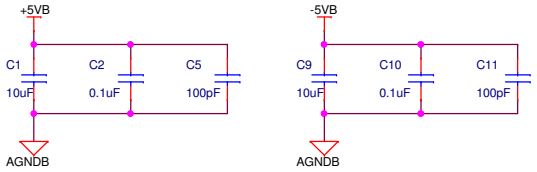
Power and Signal Connector Interface



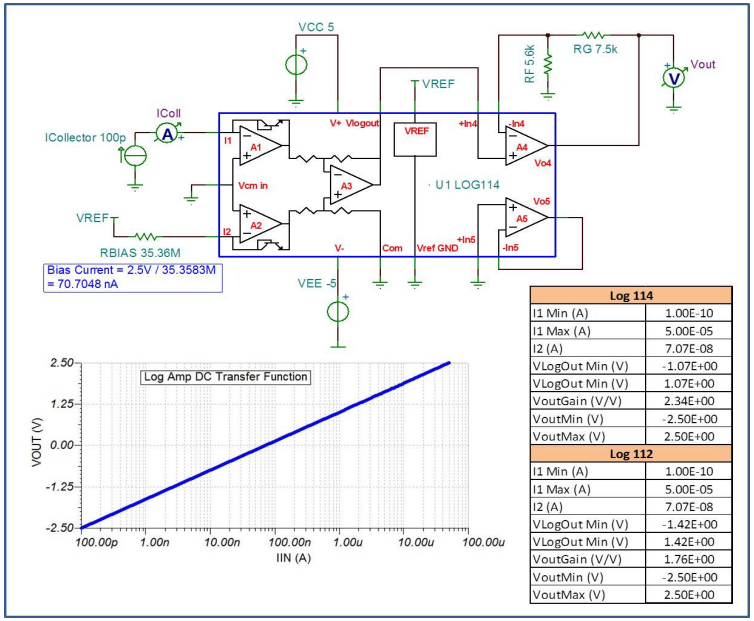
Power Conditioning



Power Conditioning



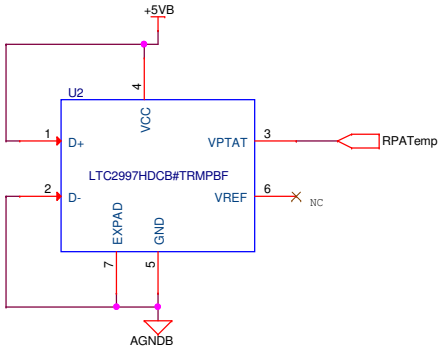
System DC Transfer Function Simulation



Log 114	
I1 Min (A)	1.00E-10
I1 Max (A)	5.00E-05
I2 (A)	7.07E-08
VLogOut Min (V)	-1.07E+00
VLogOut Min (V)	1.07E+00
VoutGain (V/V)	2.34E+00
VoutMin (V)	-2.50E+00
VoutMax (V)	2.50E+00

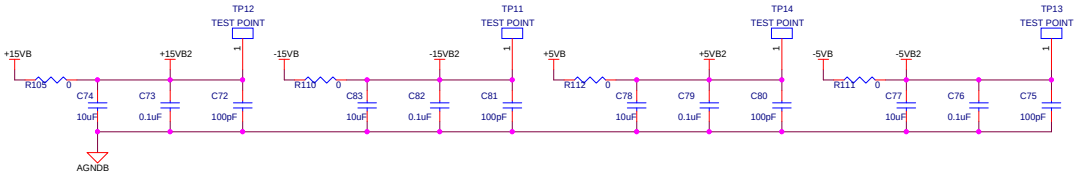
Log 112	
I1 Min (A)	1.00E-10
I1 Max (A)	5.00E-05
I2 (A)	7.07E-08
VLogOut Min (V)	-1.42E+00
VLogOut Min (V)	1.42E+00
VoutGain (V/V)	1.76E+00
VoutMin (V)	-2.50E+00
VoutMax (V)	2.50E+00

Temperature Sensor

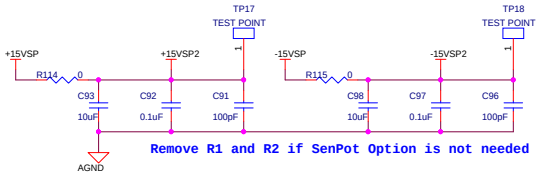


Title: RPA Daugther Board		
Size: B	Document Number: LAICE RPA DB 001	Rev: 1
Date: Sunday, February 23, 2014	Sheet 1 of 1	

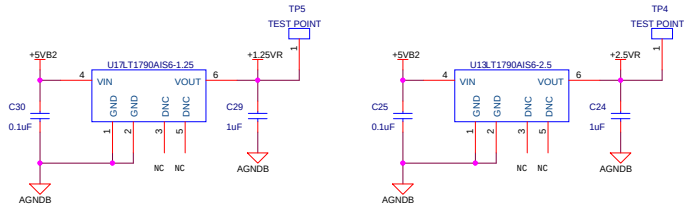
Power Conditioning - General Analog



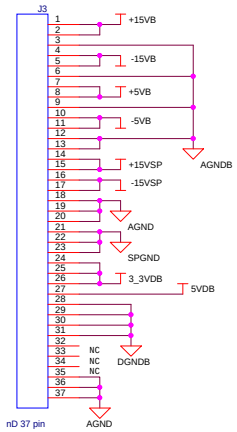
Power Conditioning - Optional SenPot Analog



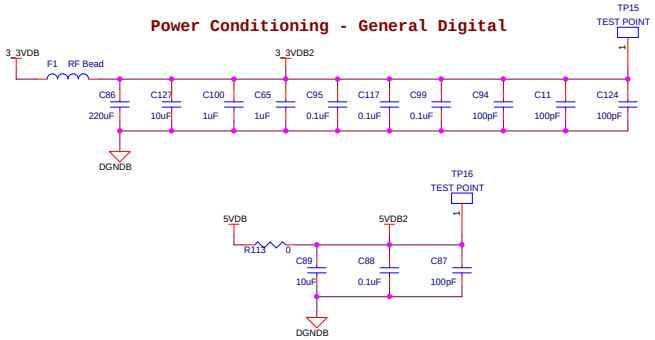
Remove R1 and R2 if SenPot Option is not needed



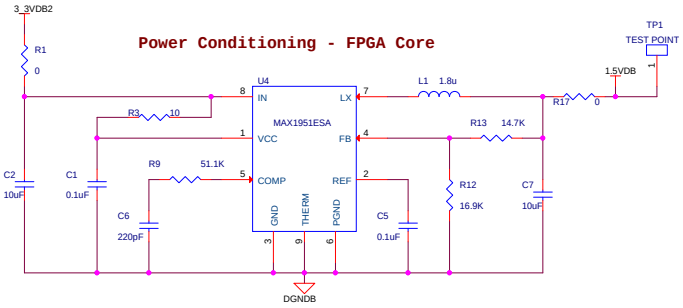
LIIB Power Connections



Power Conditioning - General Digital



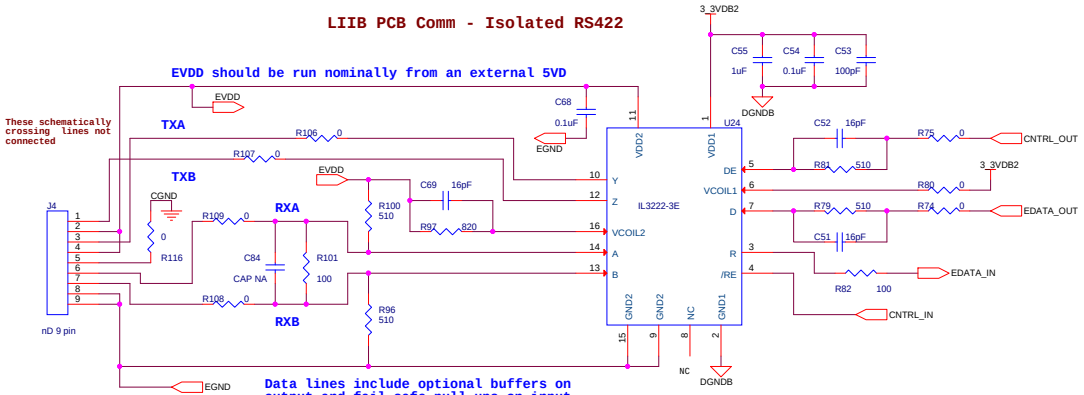
Power Conditioning - FPGA Core



Apply thermal expoxy between MAX1951 ("pin 9") and DGNDB thermal pad underneath part for improved thermal control

LIIB PCB Comm - Isolated RS422

EVDD should be run nominally from an external 5VD



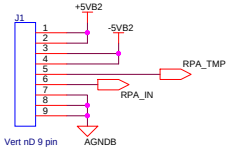
Create exposed pad for CGND coming off of J1 pin 5

CGND should be a full plane that is exposed at the board edges

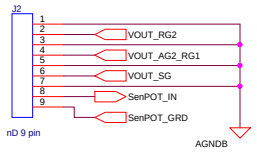
Data lines include optional buffers on output and fail safe pull ups on input differenatial lines

RS422 Buses are galvanically isolated via magnetoresive coupling sensor elements

Daugtherboard Connections



Sensor Grid and SenPOT Connections

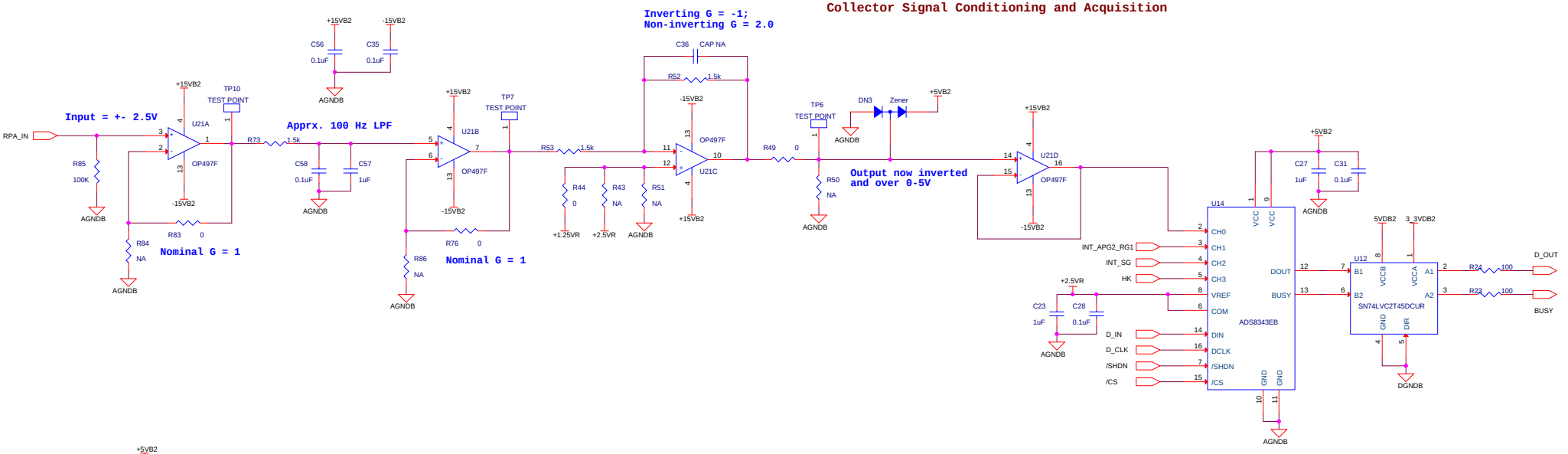


AGNDB lines for shielding of driven grids and for grids tied directly to ground

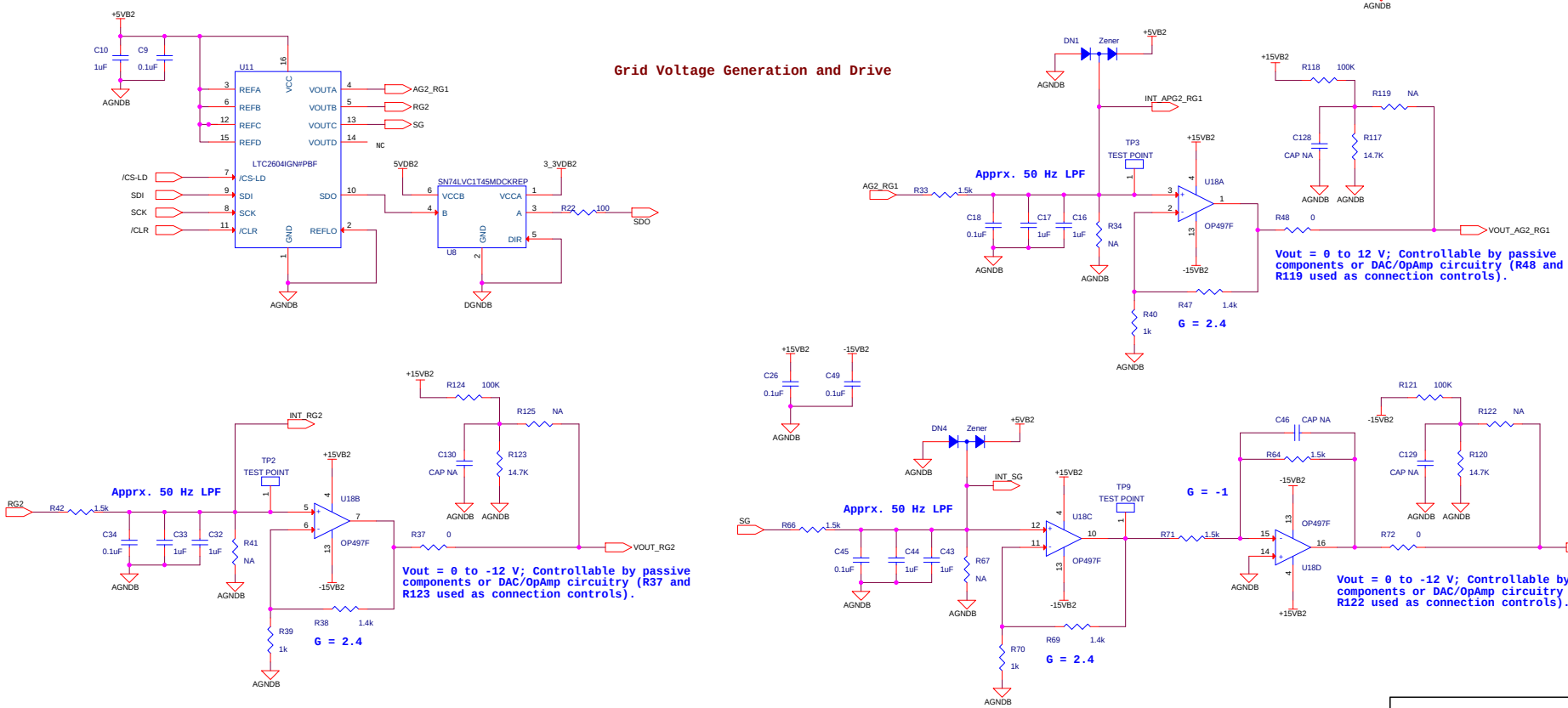
SenPOT_IN lines from sensor SenPOT surface

Title: RPA - Comm, Power, and Sensor Interfacing		
Size: C	Document Number: LAICE RPA MB 001	Rev: Orig
Date: Monday, November 25, 2013	Sheet 1 of 1	

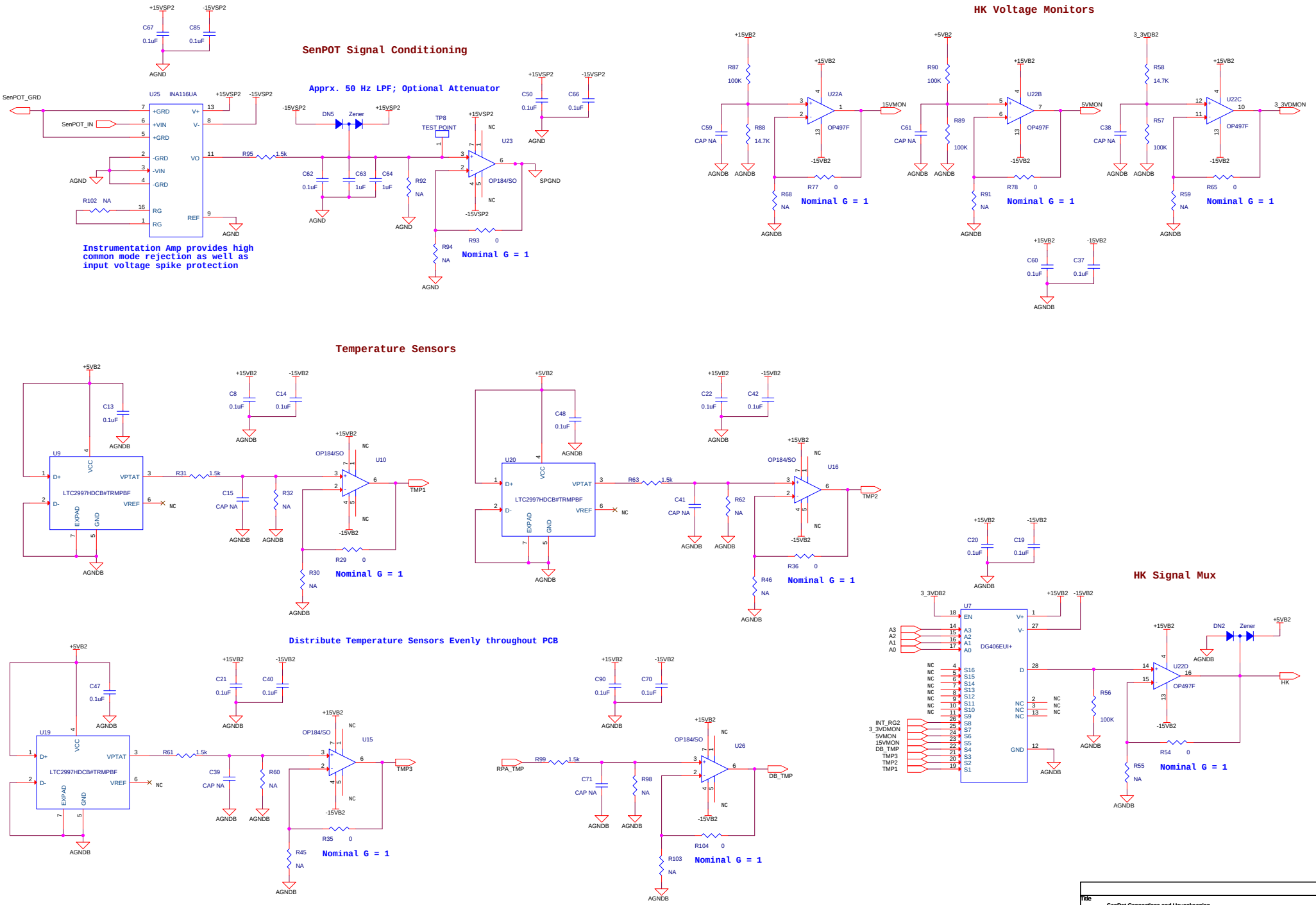
Collector Signal Conditioning and Acquisition

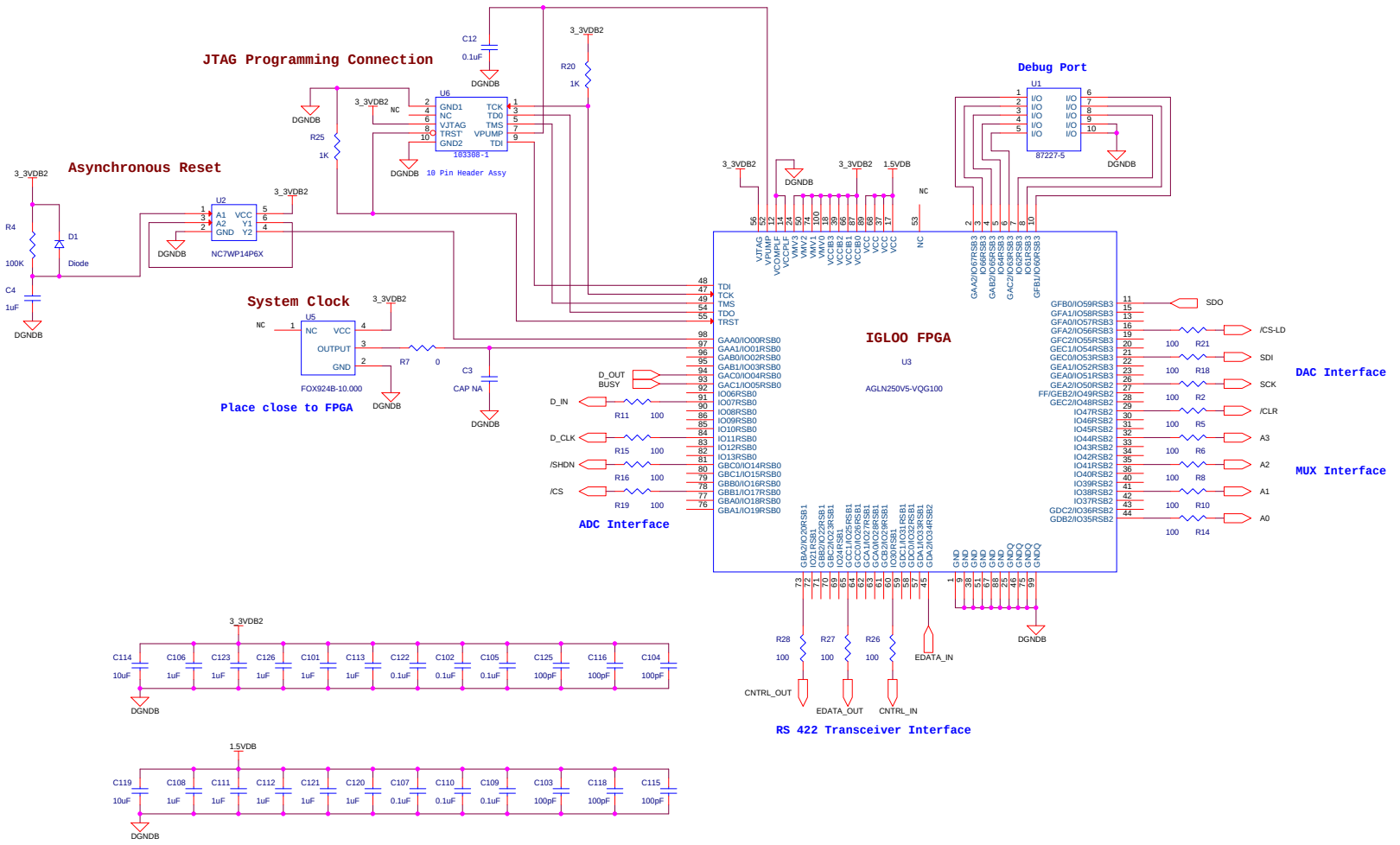


Grid Voltage Generation and Drive



Title	Signal Generation and Conditioning	
Size C	Document Number LAICE RPA MB 001	Rev Orig
Date: Monday, November 25, 2013	Sheet 1 of 1	


SenPOT Signal Conditioning
Apprx. 50 Hz LPF; Optional Attenuator
Instrumentation Amp provides high common mode rejection as well as input voltage spike protection
Nominal G = 1
HK Voltage Monitors
Temperature Sensors
Distribute Temperature Sensors Evenly throughout PCB
HK Signal Mux
SenPOT_GRD
SenPOT_IN
INA116UA
LTC2997HDCB#TRMPBF
OP184/SO
OP497F
DG406EUI+
Zener
15VMON
5VMON
3_3VDMON
TMP1
TMP2
TMP3
RPA_TMP
DB_TMP
HK
Title
SenPot Connections and Housekeeping
Size C
Document Number LAICE RPA MB 001
Rev Orig
Date: Tuesday, November 05, 2013
Sheet 1 of 1



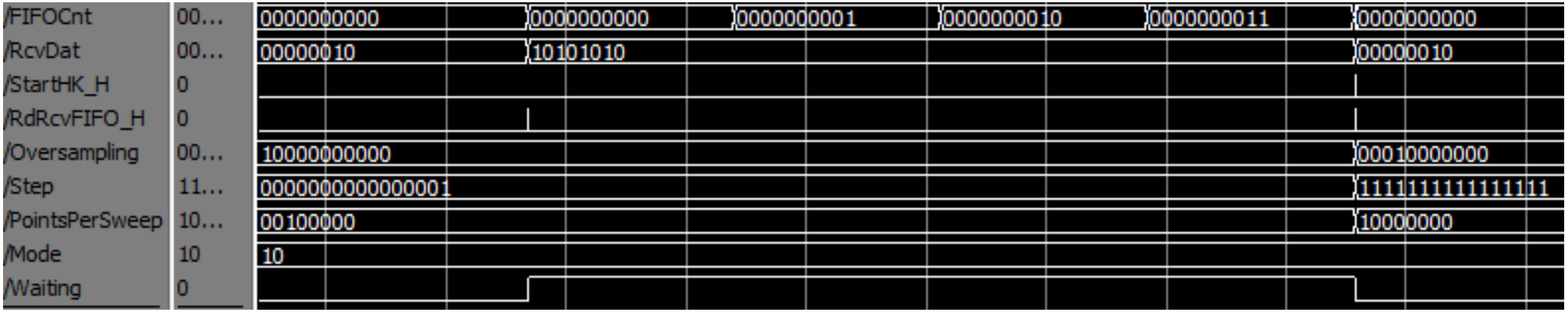
Title	FPGA/Digital Operations	
Size C	Document Number LAICE RPA MB 001	Rev Orig
Date: Tuesday, November 05, 2013	Sheet 1 of 1	

Appendix B: Parts List

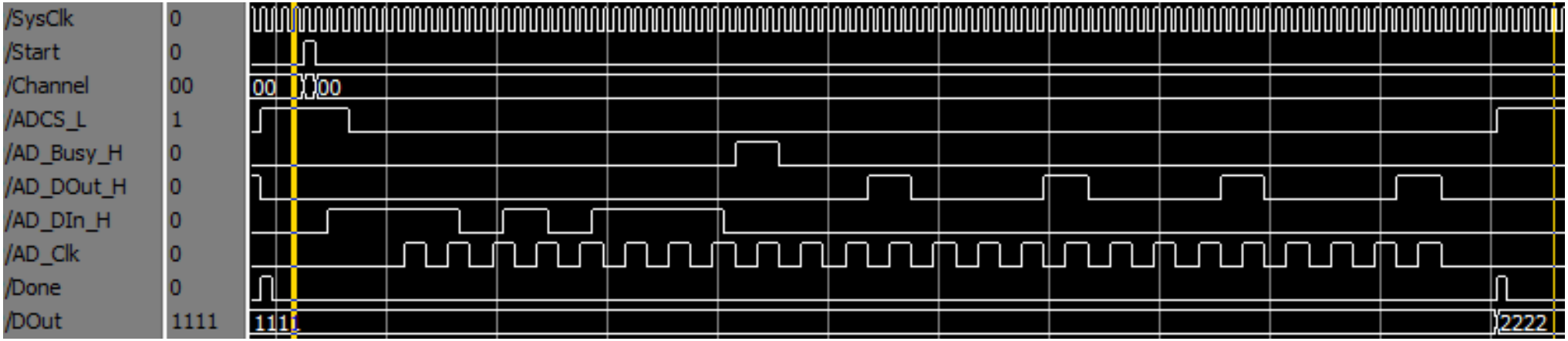
Daughter Board Parts					
Description	**Quantity**	**Reference**	**Package Type**	**Manufacturer**	**Manufacturer P/N**
10uF Cap	2	C1, C9	0805	TDK Corporation	C2012X5R1E106M125AB
0.1uF Cap	3	C2, C3, C10	0805	TDK Corporation	C2012X7R1E104M/0.85
100pF Cap	2	C5, C11	0805	TDK Corporation	C2012C0G2A101J100p
10pF Cap	1	C7	0805	TDK Corporation	C2012C0G1H100D
9-pin Connector	1	J1	nD 9 pin	Omnetics	A28500-009
10M Res	5	R5, R12, R13, R14, R15	2512	Stackpole Electronics Inc	HVCB2512BDE10M0
330k Res	1	R6	0805	Panasonic Electronic Components	ERA-6AEB334V
24k Res	1	R7	0805	Panasonic Electronic Components	ERA-6AEB243V
1.3k Res	1	R8	0805	Panasonic Electronic Components	ERA-6AEB132V
5.6k Res	1	R9	0805	Panasonic Electronic Components	ERA-6AEB562V
1.5k Res	1	R10	0805	Panasonic Electronic Components	ERA-6AEB152V
7.5k Res	1	R16	0805	Panasonic Electronic Components	ERA-6AEB752V
Standoff Post	1	Stand1	Standoff	Keystone Electronics	11320
Logarithmic Amplifier	1	U1	16-VQFN	Texas Instruments	LOG114AIRGVT
Temperature Sensor	1	U2	6-WFDFN Exposed Pad	Linear Technology	LTC2997HDCB#TRMPBF

Main Board Parts					
Description	**Quantity**	**Reference**	**PCB Footprint**	**Manufacturer**	**Manufacturer P/N**
0.1 uF Cap	54	C1,C5,C8,C9,C12,C13,C14,C18,C19,C20,C21,C22,C25,C26,C28,C30,C31,C34,C35,C37,C40,C42,C45,C47,C48,C49,C50,C54,C56,C58,C60,C62,C66,C67,C68,C70,C73,C76,C79,C82,C85,C88,C90,C92,C95,C97,C99,C102,C105,C107,C109,C110,C117,C122	C-CC0805	TDK Corporation	C2012X7R1E104M/0.85
10 uF Cap	12	C2,C7,C74,C77,C78,C83,C89,C93,C98,C114,C119,C127	C-CC0805	TDK Corporation	C2012X5R1E106M125AB
1 uF Cap	28	C4,C10,C16,C17,C23,C24,C27,C29,C32,C33,C43,C44,C55,C57,C63,C64,C65,C100,C101,C106,C108,C111,C112,C113,C120,C121,C123,C126	C-CC0805	TDK Corporation	C2012X7R1E105M085AB
220 pF Cap	1	C6	C-CC0805	TDK Corporation	CGJ4C2C0G2A221J060AA
100 pF Cap	17	C11,C53,C72,C75,C80,C81,C87,C91,C94,C96,C103,C104,C115,C116,C118,C124,C125	C-CC0805	TDK Corporation	CGA4C2C0G2A101J060AA
16 pF Cap	3	C51,C52,C69	C-CC0603	Kemet	C0603C160J5GACTU
220 uF Cap	1	C86	C-PCC6032	AVX Corporation	TLJF227M010R0300
5V Zener Diode	4	DN1,DN2,DN3,DN4	RB876-SC75	Rohm	RB876W
30V Zener Diode	1	DN5	SOT323	NXP Semiconductors	1PS70SB84
Rf Bead	1	F1	L-IND1806	Laird-Signal Integrity	LI1806E101R-10
nD Vertical Connector-to Daughter Board	1	J1	OMR-A29500-009	Omnetics	A29500-009
9-pin n-D Connectors-Com and Grids	2	J2,J4	OMN9-A29400	Omnetics	A29400-009
37-pin n-D Power Connector	1	J3	OMN37-A29400	Omnetics	A29400-037
1.8uH Ind	1	L1	L-IND-SRR4018	Wurth Elektronik	744043-0018
0-Ohm Res	34	R1,R7,R17,R29,R35,R36,R37,R44,R48,R49,R54,R65,R72,R74,R75,R76,R77,R78,R80,R83,R93,R104,R105,R106,R107,R108,R109,R110,R111,R112,R113,R114,R115,R116	R-CR0805	asonic Electronic Compone	ERJ-6GEY0R00V
100-Ohm Res	19	R2,R5,R6,R8,R10,R11,R14,R15,R16,R18,R19,R21,R22,R23,R24,R26,R27,R28,R82	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ101V
10-Ohm Res	1	R3	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ100V
100K Res	7	R4,R56,R87,R89,R118,R121,R124	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ104V
51.1K Res	1	R9	R-CR0805	asonic Electronic Compone	ERJ-6ENF5112V
16.9K Res	1	R12	R-CR0805	asonic Electronic Compone	ERA-6AEB1692V
14.7K Res	6	R13,R58,R88,R117,R120,R123	R-CR0805	asonic Electronic Compone	ERA-6AEB1472V
1K Res	2	R20,R25	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ102V
1.5K Res	13	R31,R33,R42,R52,R53,R61,R63,R64,R66,R71,R73,R95,R99	R-CR0805	asonic Electronic Compone	ERA-6AEB152V
1.4K Res	3	R38,R47,R69	R-CR0805	asonic Electronic Compone	ERA-6AEB1401V
1K Res	3	R39,R40,R70	R-CR0805	asonic Electronic Compone	ERA-6AEB102V
100K Res	1	R57	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ104V
510-Ohm Res	4	R79,R81,R96,R100	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ511V
100K Res	2	R85,R90	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ104V
820-Ohm Res	1	R97	R-CR0805	asonic Electronic Compone	ERJ-6GEYJ821V
100-Ohm Res	1	R101	R-CR2512	asonic Electronic Compone	ERJ-1TYJ101U
Test Point	18	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18	TP-KEY-5001	Keyston Electronics	5001
Debug Port-10-Pin Header	1	U1	HDR2X5	TE Connectivity	87227-5
Schmidt Trigger for Arst	1	U2	SC70-6	Fairchild	NC7WP14P6X
Actel Igloo FPGA	1	U3	TQFP100	ACTEL	AGLN250V5-VQG100
1.5V Power Reg.-FPGA Core	1	U4	SO8-TP	Maxim	MAX1951ESA+
Oscillator-10MHz, FPGA CLK	1	U5	Y-XTAL-FOX924B	Fox	FOX924B-10.000
JTAG Programming 10-Pin Header	1	U6	MX10-90708	TE Connectivity	103308-1
16-Input Analog Mux	1	U7	TSSOP28	Maxim	DG406EUI+
Voltage Level Shifter for DAC	1	U8	SC70-6	TI	SN74LVC1T45MDCKREP
Temperature Sensors	3	U9,U19,U20	DFN6	Linear Technology	LTC2997HDCB#TRMPBF
Operational Amplifiers	5	U10,U15,U16,U23,U26	SO8	Analog Devices	OP184ES
16-bit Four-channel DAC	1	U11	SSOP16N	Linear Tech	LTC2604IGN#PBF
Voltage Level Shifter for ADC	1	U12	US8	TI	SN74LVC2T45DCUR
2.5V Regulator	1	U13	SOT23-6	Linear Tech	LT1790AISG-2.5
16-bit 4-Channel ADC	1	U14	SSOP16N	TI	ADS8343EB
1.25V Regulator	1	U17	SOT23-6	Linear Tech	LT1790AISG-1.25
Operational Amplifier	3	U18,U21,U22	SOL16	Analog Devices	OP497FS
RS-422 Transceiver	1	U24	SO16	NVE	IL3222-3E
Instrumentation Amplifier	1	U25	SOL16	TI	INA116UA

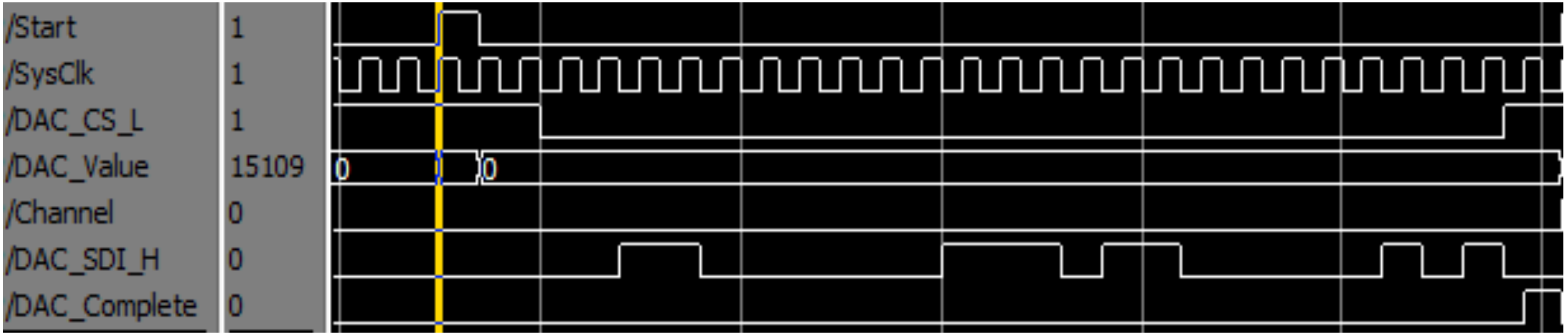
Appendix C: FPGA Simulations



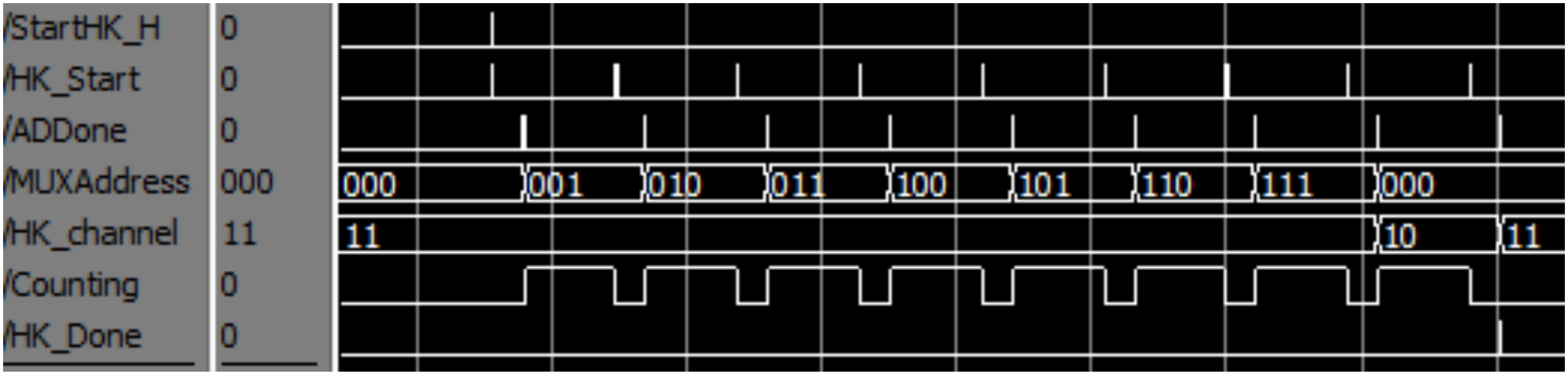
FIFO read operation: At the start of a sweep, if there is one byte in the receive FIFO, it reads it. When it is the start byte (10101010), the FPGA waits until four more bytes have been sent (indicated by the "Waiting" signal). Once four more bytes have been set, it reads them and resets the oversampling, step and points per sweep values. RdRcvFIFO_H is the signal that reads the FIFO, FIFOCnt is the number of bytes in the FIFO and RcvDat is the data after a byte is read. In this case, the points per sweep is changing from 32 to 128 which causes the oversampling to change from 1024 to 128. The step size changes as well though in this case it doesn't matter because the mode is set to smart sweep. Byte transmission takes about 430 µs.



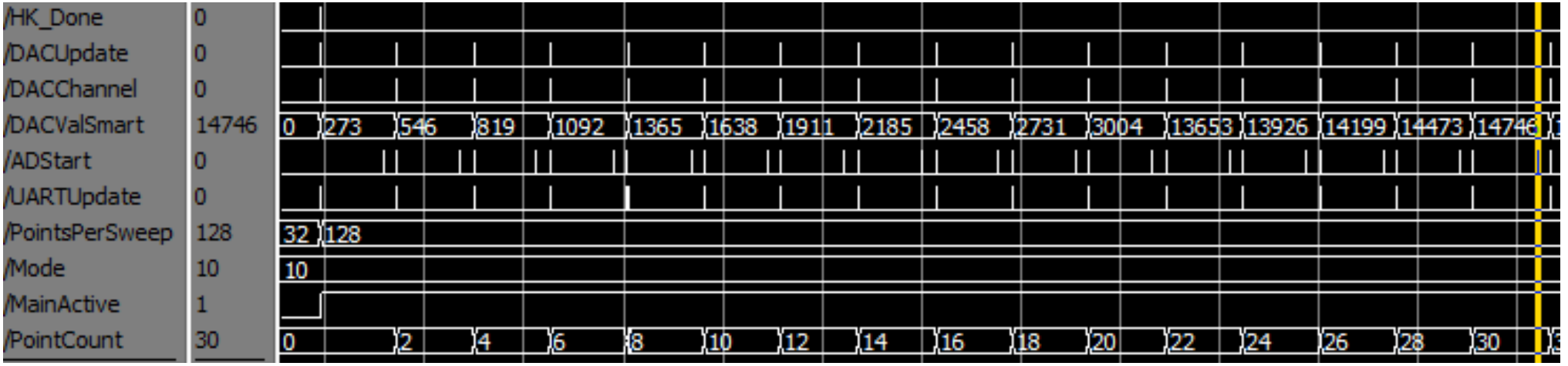
ADC Conversion: Command is shifted out and data is shifted in on AD_Clk, which has frequency 2.5 MHz. ADCS_L is low for the duration of the conversion. AD_DIn_H is the command being shifted out and AD_DOut_H is the data being shifted in. One conversion takes about 10.8 µs. In this case, the previously read data was 0x1111 and the data being read on this conversion is 0x2222.



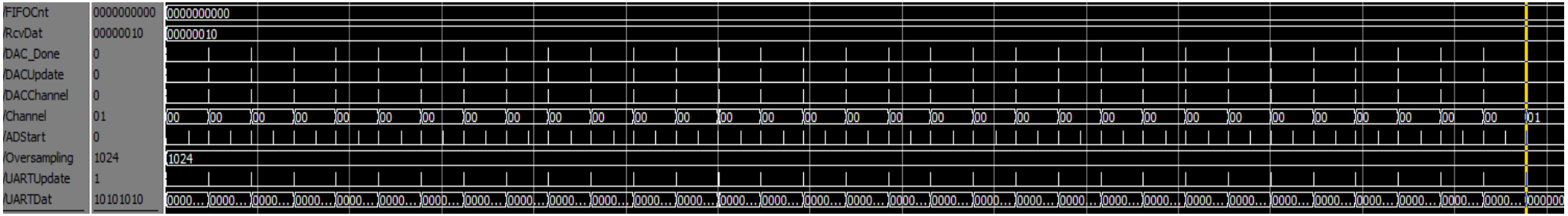
DAC Command: Data (the DAC_SDI_H signal) is shifted to the DAC on the system clock (10 MHz) and changes on the falling edge of the system clock. One DAC transmission takes about 2.8 µs. DAC_SDI_H is the command bit stream that is shifted out. Start and DAC_Value signal the start of a DAC command and the value to write to the DAC. In this case, the value is 15109 in decimal. DAC_Complete signifies that the command is finished being written. DAC_CS_L is low for the duration of the command being sent to the DAC.



Housekeeping: HK_Start and ADDone indicate the beginning and end of the ADC conversions. MuxAddress is the address sent to the mux, which is stepped through. HK_channel is the channel being sampled on the ADC, which is 3 for all the housekeeping samples and 2 when the suppressor grid is sampled at the end. "Counting" indicates when the system is waiting, which it does for 34 µs, between changing the mux selection and sampling the ADC, so the buffer has time to respond. All of the housekeeping samples take about 373 µs.



The beginning of a 128-point "smart" sweep. "HK_Done" signifies that the housekeeping data has all been taken and sent, and the sweep is ready to begin. "DACUpdate" signifies sending a DAC command. "DACValSmart" is the value (in decimal) being sent to the DAC on every update. ADStart signifies the beginning of an ADC sample being taken. 128 ADC samples are taken and averaged starting 6.35 ms after each DAC update. After this is complete, one more ADC sample is taken to sample the voltage of the retardeing grid. Once this is complete, the next point begins. UARTUpdate is a signal that writes to the transmit FIFO, which happens every time the ADC is done taking a sample. PointCount counts the number of ADC samples that have been taken-two per point, because current and voltage are both sampled on every point. When pointcount is twice the number of points per sweep minus one, all samples have been taken and the sweep is complete.



Complete 32-point smart sweep, taking about 738 ms. DACUpdate and ADStart indicate the starts of a grid voltage change and an ADC sample. The data going to the UART being 10101010 is the end byte and indicates the completion of the sweep.