Dynamic Characterization of Wide Bandgap Devices for Power Electronic System Integration

Lee Gill

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Alan J. Michaels, Chair
Virgilio A. Centeno
Christina DiMarino
Wayne A. Scales
Steve Southward

August 25, 2025
Blacksburg, Virginia

Keywords: wide bandgap, dynamic characterization, optimal system integration, reliability

Copyright 2025, Lee Gill

Dynamic Characterization of Wide Bandgap Devices for Power Electronic System Integration

Lee Gill

(ABSTRACT)

Wide Bandgap (WBG) devices offer significant performance advantages for next-generation power electronic systems. However, the dynamic stresses induced by application-specific conditions present limited physical and behavioral understanding, posing critical concerns for reliability and performance degradation. Therefore, this dissertation presents novel characterization methods, measurement techniques, and analytical frameworks to investigate dynamic switching stresses in WBG devices and the integration strategies to optimize power electronic system performance. The key state-of-the-art challenges and research gaps are identified related to dynamic stress effects throughout the system integration process of the WBG devices. An application-oriented converter stress characterization methodology is developed to evaluate the impact of dynamic operating stresses. Advanced measurement circuits and stress-induced performance evaluation techniques are designed to enable a deeper understanding of device behavior and facilitate maintenance or screening procedures. Lastly, multi-objective design optimization and lifetime performance evaluation of system-level WBG device integration are applied to demonstrate how dynamic stress insights can be leveraged to optimize overall system performance and develop novel operational lifetime prediction methodologies. This dissertation provides both a framework with a methodological and practical foundation for integrating WBG devices into high-performance, application-oriented power electronic systems by addressing key industry and research needs for improved characterization, measurement, reliability, and lifetime modeling.

Dynamic Characterization of Wide Bandgap Devices for Power Electronic System Integration

Lee Gill

(GENERAL AUDIENCE ABSTRACT)

Wide Bandgap (WBG) technologies can improve the performance of transportation electrification, energy storage systems, and grid-connected power systems by making them more efficient, robust, and reliable. However, when these devices are integrated into real-world applications, they face unique challenges; constantly changing operating conditions can strain their performance and shorten their lifetime. Also, traditional performance evaluation methods cannot fully capture the dynamics of WBG device integration challenges. This dissertation discusses developing new strategies to better understand how these advanced devices behave and how their integration is affected under practical operating conditions. It combines advanced measurement techniques, new ways to test and monitor device reliability, and methods to optimize the design process for these devices when deployed in real systems. By holistically investigating how dynamic stresses impact performance and reliability, this work helps engineers, designers, and manufacturers build better power electronic systems that fully extend the benefits of WBG technologies. Lastly, this research bridges the gap between what WBG devices are capable of in theory and how they perform in real-world applications, supporting more reliable and better integrated system as a whole.

Dedication

To my family,

whose fearless courage, steadfast perseverance,

and sacrificial love have laid the path for those who follow.

Acknowledgments

From the first passing thought of this academic journey to its final reflections, this path was never about self-aggrandizement; it has been a testament to growth through challenge, which deepened my intellectual curiosity, patience, and vulnerability, alongside an acknowledgment of my limitations. At journey's end, this work has come to fruition – not by my effort alone, but through the support of many to whom I owe deep gratitude and respect. You not only made this journey possible, but made it whole.

Over the past six years, Dr. Alan J. Michaels has been an instrumental guide. Even while navigating his own uncertainties, he has helped me bring this work to completion with compassion, encouragement, and patience. His mentorship has redefined my understanding of what the advisor–advisee relationship can be and broadened my perspective. Throughout this journey, I learned to pursue depth, to navigate complexity and ambiguity, and to strive for originality and innovation in my research, while also accepting the limits of my efforts and the importance of fulfillment beyond the work. At the same time, I am reminded that this journey does not define my career, nor does it diminish the essential parts of my life: family, friends, and the pursuits that make it whole. For these lessons, I offer my sincere gratitude and a deep bow of respect.

My thanks also extend to my committee, Dr. Virgilio A. Centeno, Dr. Christina DiMarino, Dr. Wayne A. Scales, and Dr. Steve Southward whose thoughtful critique and generous service helped ensure the rigor expected of doctoral work. I remain deeply grateful for their guidance and encouragement. I also would like to thank Sandia National Laboratories, Virginia Tech National Security Institute, and other federal and state government agencies whose support funded this dissertation research.

Lastly, who I have become and where I now stand are rooted in my parents' sacrifices. My mom's lifelong devotion to caring and building a better future for us has been a steady source of my strength and will always propel me forward. My dad, though as stubborn as a mule, taught me to dream boldly, even when a goal seems impossible, and to persevere in the face of unforgiving conditions. Though none of us is perfect, their example has left a lasting legacy in how I approach life's challenges, including this journey, and has shaped who I am, and where I stand today. While the completion of this work is only a small tribute of all they have provided me, I hope it brings them pride and pays homage to all the *shit* they have endured (pardon the language; no other word feels as honest).

As this phase of my life comes to a close, I remind myself to stay humble, selfless, and vulnerable, thanks to the many people who have influenced me. I will carry these values forward as I strive to keep growing and to lead with humility on whatever path comes next. For those who happened to read this personal digression, I welcome your challenge and accountability if I stray from these values as a leader. In the meantime, I'm going to slow down for just a bit (not for long) and catch up on the movies and shows I have missed on Netflix.

Contents

List of Figures xi

List of Tables xviii

1 Introduction 1

1.1 Motivation 1

1.2 Research Objectives and Main Contributions 4

1.2.1 Summary of Contributions 5

1.2.2 Journal Publications 7

1.2.3 Conference Publications 7

1.3 Dissertation Outline 9

2 Background and Literature Review 11

2.1 Background Information 11

2.1.1 WBG Material Properties and Performance Implications 11

2.1.2 Device Characterization Measurement Fundamentals 15

2.1.3 Optimization of Power Electronic System Performance 20

2.2 Challenges and Research Gaps 23

2.2.1 Dynamic Switching Environments on WBG Device Operation and Physical Mechanisms . . . 23

2.2.2 Advanced Characterization Measurement Techniques for WBG Device Performance and Qualification . . . 26

2.2.3 Multi-Objective Optimization of Power Electronic Systems and Predictive Lifetime Analysis . . . 30

2.3 Summary . . . 33

3 Dynamic Switching Stress Classification and Evaluation 34

3.1 Dynamic Stresses in Power Converters . . . 34

3.1.1 Stress Categories Based on Converter Topologies . . . 35

3.1.2 Review of Dynamic On-Resistance in GaN Devices . . . 39

3.2 Slew Rate Effects of Dynamic Stresses on Device Physics and Operation . . . 55

3.2.1 Effects on GaN HEMT Distributed Field Plate Structures . . . 55

3.2.2 Evaluation of Switching Slew Rates in Cascode GaN . . . 64

3.3 Summary . . . 74

4 Characterization Techniques and Qualification Analysis for WBG Integration 75

4.1 On-State Voltage Measurement Circuit Topology, Operation, and Performance 76

4.1.1 Technical Review of Prior State-of-the-Art . . . 80

4.1.2 Proposed Measurement Circuit Topology Analysis . . . 85

4.1.3 Design Considerations and Auxiliary Hardware 90
4.1.4 Discussion of Static and Dynamic Measurement Experimental Results 100
4.2 Screening and Inspection Analysis Based on Device Electrical Characteristics 110
4.2.1 Impact of Part Variability on Converter Performance 111
4.2.2 Non-Destructive Inspection Technique using Machine Learning 115
4.3 Automated Test System for WBG Dynamic Reliability Evaluation 121
4.3.1 Software Architecture Development 123
4.3.2 Hardware Design and Implementation 126
4.4 Summary 130

5 Optimization and Lifetime Analysis for Power Electronic Systems 133

5.1 Multi-Objective Optimization and Co-Design of Power Electronic Systems . 134
5.1.1 EV Traction Inverter for Efficiency, Volume, and Reliability 135
5.1.2 Co-Design Analysis of WBG Power Diodes with Operational Regimes 152
5.2 Dynamic Device Lifetime Estimation Methodologies 165
5.2.1 Real-Time Lifetime Prediction Using Hardware-in-the-Loop 166
5.2.2 Deep Neural Network Fusion Model for Lifetime Estimation 176
5.3 Summary 185

6 Conclusion and Outlook 186

6.1 Summary 186

6.2 Outlook 189

Appendices **192**

Appendix A Cascode Current Mirror Derivations **193**

A.1 Cascode Transfer Ratio Analysis 193

A.2 Cascode Output Impedance Analysis 196

Bibliography **202**

List of Figures

1.1 Hierarchical structure from materials to applications in power electronics . . 2

1.2 Research contributions across the power electronics hierarchy 5

2.1 Trade-off between R_{on} and V_{BR} in semiconductor materials 12

2.2 Characterization techniques for power devices: (a) static parameter extraction, (b) dynamic double pulse testing 18

2.3 Comparison of power electronics performance and trade-offs across application domains 21

2.4 Illustration of I–V differences between DC and pulsed modes in GaN HEMTs 25

2.5 Comparison of high-voltage switching and clipped-voltage waveforms in on-state 27

2.6 Measured part-to-part variations in GaN HEMT electrical characteristics . . 29

2.7 EV powertrain system with power electronics and supporting subsystems . . 31

3.1 Summary of power converter topologies with corresponding voltage and current stress waveforms 38

3.2 Charge trapping phenomena in GaN-on-Si with hot carrier and off-state mechanisms 43

3.3 Operational parameters affecting dynamic R_{on} in GaN HEMTs based on literature data 48

3.4 Drain field cage structure using resistive voltage divider network 57

3.5 Electric field profiles for various drain field cage (DFC) spacings and baseline field plate structure . . . 58

3.6 Drain field cage schematic and electric field analysis for varying tap spacing and thickness . . . 59

3.7 Schematic of DFC taps with V_n, $C_{\text{t-t}}$, $C_{\text{t-c}}$, and conduction/displacement currents . . . 60

3.8 Effect of passivation thickness on voltage drop and electric field in drain field cage structures . . . 62

3.9 Electric field profile in DFC structures under varying dV/dt at $V_{ds} = 500$ V . 64

3.10 Circuit topologies used for dynamic $R_{\text{DS(on)}}$ characterization and waveform analysis . . . 67

3.11 MPT setup with variable gate resistance and OVMC for dynamic $R_{\text{DS(on)}}$ measurement . . . 69

3.12 MPT waveforms showing gate signal, drain voltage, and current across five consecutive pulses . . . 70

3.13 Impact of $R_{g,on}$ variation on GaN voltage and current switching transients . 71

3.14 Effect of external gate resistance on voltage/current slew rates and turn-on switching losses . . . 72

3.15 Effect of gate resistance and voltage on normalized dynamic R_{on} in cascode GaN HEMT . . . 73

3.16 Normalized R_{on} compared against voltage for cascode GaN with $R_{g,on}$ variation and benchmark comparison . . . 74

4.1 Survey of on-state voltage measurement topologies in prior literature, including proposed method 81

4.2 Operating principle of proposed on-state voltage measurement circuit with current source and clamping 87

4.3 Schematic of PNP BJT cascode current mirror with labeled nodes and components 89

4.4 Operating modes of on-state voltage measurement circuit and final V_{cc}–R design trade-off 95

4.5 Temperature sensitivity and measurement error analysis for Schottky diode-based sensing 96

4.6 Effect of ΔI_{REF} on measurement accuracy at 75°C and $I_{\mathrm{ds}} = 40$ A 97

4.7 Proposed on-state voltage measurement with diode drop compensation and hardware prototype 99

4.8 Experimental setup and results for static ON-state voltage measurement using OVMC 102

4.9 Dynamic on-state voltage measurement setup and validation via experiment and simulation 104

4.10 Physical integration of OVMC for on-state voltage sensing in power converter setup 104

4.11 Dynamic performance of OVMC across DUT voltage, current, and switching waveform comparison 106

4.12 Performance comparison between proposed and commercial on-state voltage measurement circuits 109

4.13 On-resistance population statistics and PDF comparison across four different suppliers 113

4.14 Process for evaluating part-to-part device variability impact on converter performance 114

4.15 Mean and range of converter efficiency due to part variability in conduction and switching losses 115

4.16 Non-destructive small-signal test method and equivalent model for GaN devices 117

4.17 Time-domain gate-source voltage signals of GaN samples at 10 kHz showing part-to-part variation 117

4.18 K-means clustering results with elbow method and PCA-based cluster visualization 120

4.19 Comparison of CL.0 and CL.1 sample means to population mean with 90% CI for output, transfer, and capacitance characteristics. 121

4.20 Automated test system software architecture overview 124

4.21 Automated test system software workflow diagram 125

4.22 Automated test system electrical diagram, detailing connections between instruments 127

4.23 Safety sensors to verify absence of energy prior to opening an electrical enclosure 129

4.24 Fully assembled automated test racks for WBG dynamic reliability evaluation 130

5.1 EV drivetrain power electronics and control system model. 136

5.2 Vehicle dynamic and wheel model with physical parameters. 137

5.3 Comparison of T_e^* and T_e with annotated driving conditions and speed profiles 140

5.4 Volume trends of COTS film capacitors with respect to capacitance and stored energy 141

5.5 Thermal resistance modeling: (a) Cauer network, (b) empirical Z_θ vs. volume trend 143

5.6 IGBT and SiC lifetime analysis using fitted CIPS08-based models and experimental data 144

5.7 PLEC-Python multi-objective optimization process to integrate the EV model developed in `PLECS` and NSGA computation analysis through `pymoo` 146

5.8 US06 driving profile with periods of acceleration, deceleration, and cruising. . . . 147

5.9 Trade-off analysis of volume, average efficiency, and reliability across Pareto front projections 151

5.10 Optimization results of minimum power loss across blocking voltage and device technology 156

5.11 Power diode loss map showing switching losses and forward bias voltage characteristics 159

5.12 Circuit and waveform illustration for single-phase 3-level boost PFC 161

5.13 Voltage and current stress comparison between rectifying and freewheeling diodes 162

5.14 Simulation results for single-phase 3-level boost PFC showing THD, output voltage, and loss split 163

5.15 Efficiency density and loss contribution comparison for UWBG and WBG SBD and PIN diodes 164

5.16 Real-time lifetime processing framework via HIL multi-domain models and data processing strategy. 167

5.17 Three-phase induction motor drive system model in HIL to enable the junction temperature monitoring of the module highlighted in blue. 168

5.18 Example of time varying dynamic input torque stress profile over time for the three-phase induction motor model. 173

5.19 Junction temperature output response based on the torque demand profile from Figure. 5.18. 174

5.20 Real-time cumulative lifetime under two torque profiles with equal mean torque but differing dynamics. 175

5.21 Device characterization results showing median and IQR for static, leakage, capacitance, and switching behaviors across temperature and bias conditions. 177

5.22 Feature engineering process for converting raw measurements into ML-ready inputs using physics-based extraction, interpolation, and augmentation. . . . 178

5.23 Overview of data-to-model framework linking device characterization, surrogate modeling, simulation, and deep learning. 179

5.24 Proposed multi-modal deep learning model for lifetime prediction using raw and engineered features. 181

5.25 Comparison of lifetime prediction accuracy between baseline single-branch models and proposed fusion network. 183

5.26 Training and validation MSE and MAE as a function of epoch, illustrating progressive model convergence and generalization behavior. 184

A.1 Hybrid-π-based small-signal analysis of output resistance in cascode mirror . 197

List of Tables

2.1 Physical properties of wide bandgap semiconductors for power electronic applications in comparison to classic semiconductor materials. 13

3.1 Summary of converter topologies and electrical waveform categories. 40

3.2 Summary of five research themes related to $d\mathrm{R}_{\mathrm{DS(ON)}}$, providing descriptions and relevant literature. 54

3.3 Summary of circuit topologies for $d\mathrm{R}_{\mathrm{DS(ON)}}$ characterization. 65

4.1 Device Characterization topics evaluated through ON-resistance measurements. 78

4.2 Advantages and disadvantages of state-of-the-art ON-state voltage measurement circuit topologies. 82

4.3 Summary of Euclidean distances of V_{gs} output response at different excitation frequencies, along with principal component projections. 119

5.1 Electric Vehicle System Model Parameters 139

5.2 Linear fit parameters for different capacitor voltage ranges. 142

5.3 Power-law coefficients for different flow rate ranges. 143

5.4 Power cycling model coefficients for SiC and IGBT devices for $\Delta T \leq 50°\mathrm{C}$. . 144

5.5 Time and relative weights of driving conditions. 148

List of Abbreviations

2DEG Two-Dimensional Electron Gas

AC Alternating Current

ADC Analog-to-Digital Converter

AEC Automotive Electronics Council

AI Artificial Intelligence

Al Aluminium

AlN Aluminium Nitride

BJT Bipolar Junction Transistor

BV Breakdown Voltage

C-V Capacitance-Voltage

CCM Continuous Conduction Mode

CI Confidence Interval

CNN Convolutional Neural Network

CoG Center of Gravity

COTS Commercial Off-The-Shelf

CPU Central Processing Unit

CTE Coefficient of Thermal Expansion

DC Direct Current

DCM Discontinuous Conduction Mode

DFC Drain Field Cage

DL Deep Learning

DLTS Deep-Level Transient Spectroscopy

DNN Deep Neural Network

DPT Double-Pulse Test

DUT Device-Under-Test

EMC Electromagnetic Compatibility

EMI Electromagnetic Interference

EPA Environmental Protection Agency

EV Electric Vehicle

FAIR Findable, Accessible, Interoperable, and Reusable

FET Field-Effect Transistor

FOM Figure of Merit

FPGA Field Programmable Gate Arrays

GA Genetic Algorithm

GaN Gallium Nitride

GaO Gallium Oxide

GIT Gate Injection Transistor

GPM Gallons per minute

GPU Graphics Processing Unit

HAST Highly Accelerated Stress Test

HEMT High Electron Mobility Transistor

HIL Hardware-in-the-Loop

HTGB High-Temperature Gate Bias

HTRB High-Temperature Reverse Bias

HV High Voltage

I-V Current-Voltage

I/O Input and Output

IEC International Electrotechnical Commission

IGBT Insulated-Gate Bipolar Transistors

IoT Internet of Things

IQR Interquartile Range

JBS Junction Barrier Schottky

JEDEC Joint Electron Device Engineering Council

L-C Inductive-Capacitive

L-R Inductive-Resistive

ML Machine Learning

MLP Multilayer Perceptron

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor

MPC Model Predictive Control

MPS Merged Pin Schottky

MPT Multiple Pulse Test

MSE Mean squared error

OVMC On-state Voltage Measurement Circuit

PCA Principal Component Analysis

PCB Printed Circuit Board

PDF Probability Density Functions

PDU Power Distribution Unit

PFC Power Factor Correction

PMSM Permanent Magnet Synchronous Machine

ReLU Rectified Linear Unit

RMSE Root Mean Squared Error

RMS Root Mean Square

RUL Remaining Useful Life

SBD Schottky Barrier Diode

SCL Space-Charge Limited

SiC Silicon Carbide

Si Silicon

SOA State-of-the-Art

SPICE Simulation Program with Integrated Circuit Emphasis

SSE Sum of Squared Error

SVM Space-Vector Modulator

TCAD Technology Computer Aided Design

TCM Triangular Current Mode

THD Total Harmonic Distortion

UID Unintentionally Doped

UI User Interface

UPS Uninterruptible Power Supply

UWBG Ultra Wide Bandgap

VSD Variable Speed Drive

VSI Voltage Source Inverter

WBG Wide Bandgap

ZCS Zero Current Switching

ZVS Zero Voltage Switching

Chapter 1

Introduction

This chapter introduces the motivation for this dissertation research efforts by demonstrating the need for new evaluation studies that enable the seamless integration of Wide Bandgap (WBG) devices into power electronic applications, with a focus on physical understanding of the devices, development of measurement techniques, device lifetime prediction methodologies, and optimal system integration under dynamic operating conditions. It outlines the specific research objectives across key focus areas and summarizes the main contributions that address the challenges within each topic area while referencing relevant publications resulting from this work. Lastly, it provides an overview of the dissertation structure to guide the reader through the progression of topics covered in the subsequent chapters.

1.1 Motivation

Power electronic systems enable energy conversion across diverse applications, including electric vehicles (EVs), energy storage systems, industrial motor drives, and advanced grid interfaces [1, 2, 3]. These systems are inherently hierarchical in nature, as illustrated in Figure 2.1, and are built from fundamental materials, such as semiconductors, conductors, insulators, dielectrics, and magnetic materials, that are fabricated into components like devices, capacitors, inductors, transformers, and packaging modules. These components are then assembled into functional subsystems through appropriate topologies and modular de-

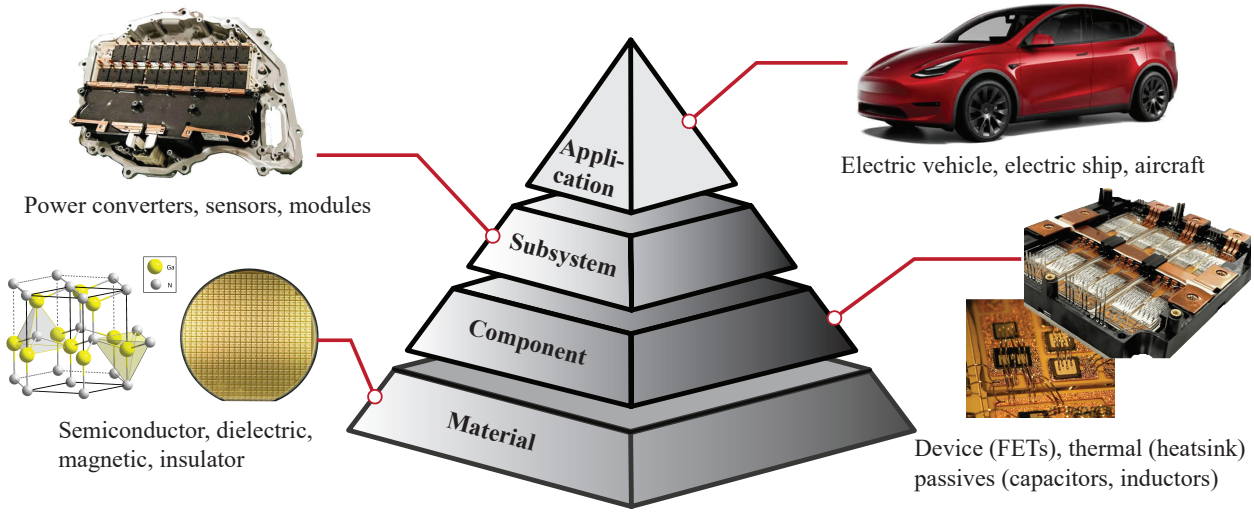


Figure 1.1: Hierarchical framework of a power electronic system, from fundamental materials through components and subsystems to end-use applications.

signs before being integrated into end-use applications. Across each level of this hierarchical integration chain from intrinsic material properties to system-level operating conditions, critical design and implementation considerations play an important role in determining optimal system performance.

The end-use application, whether it involves transportation electrification, energy storage, or grid-interfacing technologies, ultimately defines the system-level requirements and underlying operating conditions that manage how materials, devices, and subsystems interact altogether. Dynamic load profiles, fluctuating input conditions, and varying temperature environments contribute to complex electrical and thermal stresses that can largely affect device behavior and system performance over time. To achieve optimal integration and ensure the highest system performance, a comprehensive framework for dynamic characterization and advanced integration is needed [4].

At the material level, understanding the intrinsic properties and dynamic behavior of advanced semiconductor materials is critical to understanding material degradation mechnisms and reliability. WBG materials, such as Gallium Nitride (GaN) and Silicon Carbide (SiC)

provide higher critical electric fields, improved thermal conductivity, and wider energy bandgaps compared to conventional silicon (Si) [5, 6, 7]. However, to fully realize these benefits in practical, yet complex systems, it is necessary to characterize how material properties respond under dynamic electrical or thermal operating conditions, such as time-varying electric fields and different switching transition slew rates, which can directly influence generation of charge traps and hot carriers that could impede the material performance over time.

At the component level, these advanced materials are fabricated into discrete power devices, such as diodes, the metal–oxide–semiconductor field-effect transistors (MOSFETs), and high-electron-mobility transistors (HEMTs) [8]. In practical power electronic circuits, devices are subjected to rapidly changing voltage and current transients, high switching slew rates, and repetitive stress cycles that can trigger non-ideal effects such as dynamic on-resistance, increased switching losses, and localized heating. These dynamic stresses can interact with material-level phenomena, leading to shifts in device characteristics, such as threshold voltage, Miller plateau, on-resistance, and junction capacitance hysteresis [9, 10, 11, 12, 13, 14]. Therefore, accurate measurement and evaluation techniques of device characteristic parameters under application-oriented, time-varying operating or storage conditions are essential to ensure predictable performance and long-term reliability when these devices are integrated into higher-level subsystems.

At the subsystem level, individual power devices or modules are interconnected through circuit topologies, along with other passive and active components [15], to achieve the required functionality for the end-use application. In practical systems, these subsystems operate under complex switching sequences, modular interactions, and variable load conditions that can amplify electrical and thermal stresses [16]. Such dynamic effects can propagate through the subsystem and influence loss distribution and thermal performance, ultimately impact-

ing overall system efficiency and operational lifetime [17]. Therefore, it is important to develop system-level optimization strategies and performance evaluation frameworks that holistically capture these interactions while providing reliable lifetime prediction for these power electronic systems.

In essence, for the integration of fundamental materials into system architectures, there is a clear need for advanced evaluation studies that enables and integrates dynamic stress characterization, advanced measurement techniques, and system-level optimization and lifetime analysis. By developing appropriate simulation, modeling, measurement, and analytical techniques that allow a deeper understanding of WBG device behavior and its integration under system-level operating conditions, designers and manufacturers can better adapt to design changes, predict failure mechanisms, optimize converter designs, and extend the operational lifetime of power electronic systems. Hence, this dissertation is motivated by this exact need to bridge the gap between theoretical device capabilities and real-world system performance. By presenting an integrated approach that combines the three separate topics of dynamic switching stress evaluation, advanced measurement and monitoring circuits, and performance optimization strategies, this dissertation provides direct contributions to practical methodologies for more reliable, robust, and efficient integration of WBG devices into next-generation power electronic applications.

1.2 Research Objectives and Main Contributions

The overarching objective of this dissertation is to develop evaluation strategoes for dynamic stress characterization, advanced measurement techniques, and optimal performance with reliability assessment under application-oriented conditions. The main contributions of the overall dissertation are summarized in Subsection 1.2.1 and also visually in Figure. 1.2, with

the corresponding journal and conference publications referenced in Subsection 1.2.2 and Subsection 1.2.3, respectively.

1.2.1 Summary of Contributions

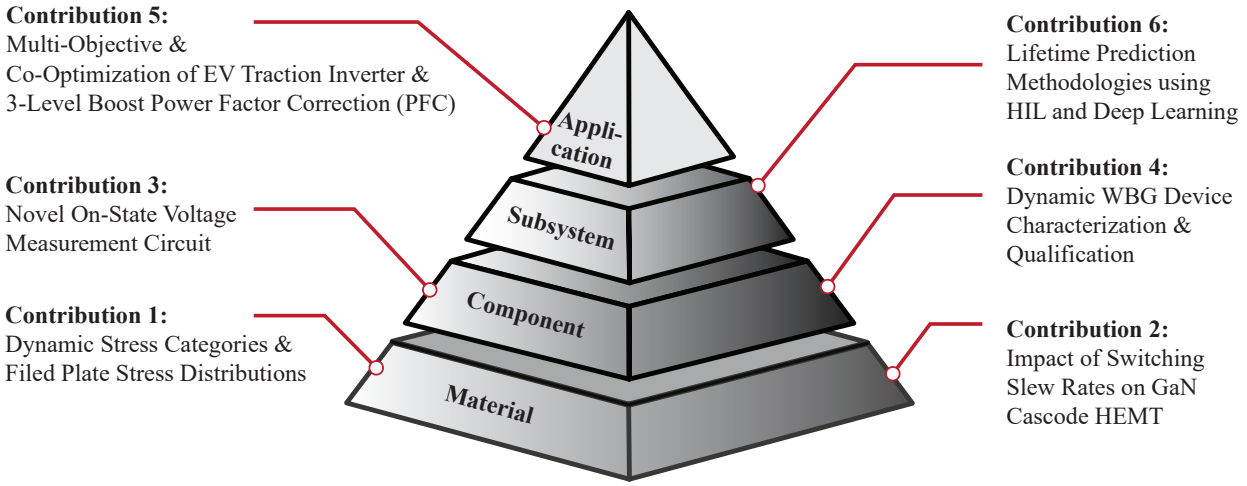


Figure 1.2: Summary of main research contributions mapped to the corresponding levels of the power electronics hierarchical framework, from material to application.

- **Contribution 1:** Classification of dynamic stress modes across converter topologies, emphasizing how time-varying switching behavior induces distinct electric field distributions beyond the scope of conventional static or DC-based evaluations. In-depth simulation studies illustrate the effects of varying voltage stress slew rates on electric field distribution along field plates in GaN HEMTs [J1].

- **Contribution 2:** Comprehensive analysis of the impact of switching slew rates on dynamic on-resistance behavior and charge trapping mechanisms in GaN cascode devices, using multiple pulse test (MPT) measurements and a TCAD model to gain fundamental understanding into device physics and operational behavior [J4, C7].

- **Contribution 3:** Development of a novel on-state voltage measurement circuit based on a cascode current mirror topology, enabling high-resolution, temperature- and load-immune measurements for WBG devices with in-situ health monitoring capability. The approach includes detailed derivation and analysis of large- and small-signal models and demonstrates high accuracy and dynamic response across a wide range of operating conditions, validated through both simulation and hardware experiments [J2, C3].

- **Contribution 4:** Evaluation of dynamic device characteristics, performance, and qualification, including the impact of inherent part-to-part variations on power conversion behavior. Non-destructive screening techniques, such as principal component analysis (PCA) and machine learning to correlate static and dynamic parameters across device populations. A flexible, reconfigurable test platform to realize rapid assessment of device dynamic behaviors and their impact on system-level reliability [J5, C5, C6].

- **Contribution 5:** Demonstration of multi-objective system-level design optimization for integrating WBG devices into power electronic systems. Multiple applications, including EV traction inverters and power factor correction (PFC) circuits, are used to analyze electrical and thermal behaviors under dynamic conditions and to optimize trade-offs among loss, volume, reliability, and other key performance metrics [C1, C2, C4, C9].

- **Contribution 6:** Development of unique lifetime prediction methodologies for WBG device integration under dynamic operating conditions. This includes a real-time lifetime monitoring framework using Hardware-in-the-Loop (HIL) to predict remaining useful life based on continuous tracking of operational time and cumulative stress. In addition, an AI-enabled deep learning (DL) fusion network incorporates practical device behaviors and multi-modal, high-dimensional data from dynamic characterization to improve prediction accuracy, support maintenance scheduling and operational

reliability, and extend device service life in critical power applications [J3, C8].

1.2.2 Journal Publications

[J1] L. Gill, S. DasGupta, J. C. Neely, R. J. Kaplar and A. J. Michaels, "A Review of GaN HEMT Dynamic ON-Resistance and Dynamic Stress Effects on Field Distribution," in *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 517–537, Jan. 2024, doi: 10.1109/TPEL.2023.3318182.

[J2] L. Gill, L. A. G. Rodriguez, R. Kaplar and A. J. Michaels, "Novel On-State Voltage Measurement Circuit Topology, Operation, and Performance for High-Voltage Wide Bandgap Devices," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2025.3583677

[J3] L. Gill, J. Actor, M. Negoita, G. -S. Seo and A. Michaels, "Multi-Modal Deep Neural Network Fusion Model for Device Lifetime Estimation Using High-Dimensional Characterization Data," in *IEEE Transactions on Power Electronics*, under review, July 2025.

[J4] L. Gill, L. A. Garcia Rodriguez, N. Negoita, R. Kaplar, and A. J. Michaels, "Evaluation of Switching Slew Rates on Dynamic ON-Resistance in Cascode GaN HEMTs Using Multiple Pulse Test," in *IEEE Transactions on Industry Applications*, under review, August 2025.

[J5] L. Gill, B. Rummel, C. Davis, R. J. Kaplar and A. J. Michaels, "Development of Automated Test System for Evaluation of Wide Bandgap Device Integration Reliability," in *IEEE Transactions on Instrumentation and Measurement*, in preparation, August 2025.

1.2.3 Conference Publications

[C1] L. Gill, J. C. Neely, L. J. Rashkin, J. D. Flicker and R. J. Kaplar, "Co-Optimization of Boost Converter Reliability and Volumetric Power Density Using Genetic Algorithm," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 5302-5309, doi: 10.1109/ECCE44975.2020.9235716.

[C2] L. Gill, L. Rashkin, L. Yates, J. Neely and R. Kaplar, "Multi-Objective Parametric Anal-

ysis of EV Traction Inverter between Reliability and Efficiency," *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, 2023, pp. 3174-3181, doi: 10.1109/APEC43580.2023.10131644.

[C3] L. Gill, L. A. Garcia Rodriguez, J. Mueller, R. Kaplar and A. J. Michaels, "Novel Dynamic ON-Resistance Measurement Circuit Topology, Operation, and Performance for High Voltage GaN Power HEMTs," *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, Nashville, TN, USA, 2023, pp. 5398-5405, doi: 10.1109/ECCE53617.2023.10362641.

[C4] L. Gill, J. Shoemaker, J. Flicker, S. Goodnick, R. Kaplar and A. Michaels, "Co-optimization Design and Analysis of WBG and UWBG Power Diodes with Operational Regimes," *2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, Charlotte, NC, USA, 2023, pp. 1-6, doi: 10.1109/WiPDA58524.2023.10382225.

[C5] L. Gill, J. Actor, R. J. Kaplar and A. J. Michaels, "Machine Learning Based Non-Intrusive Inspection Technique to Quantify GaN HEMT Characteristics," *2023 IEEE Design Methodologies Conference (DMC)*, Miami, FL, USA, 2023, pp. 1-6, doi: 10.1109/DMC58182.2023.10412423.

[C6] L. Gill, M. Smith, L. Yates, G. -S. Seo and A. J. Michaels, "Evaluation of Converter Performance Considering Static and Dynamic Device Part-to-Part Variability," *2024 IEEE Design Methodologies Conference (DMC)*, Grenoble, France, 2024, pp. 1-7, doi: 10.1109/DMC62632.2024.10812119.

[C7] L. Gill, L. A. G. Rodriguez, M. Negoita, S. DasGupta, R. Kaplar and A. J. Michaels, "Impact of External Gate Resistance on Dynamic ON-Resistance Behavior in GaN HEMTs Using Multiple Pulse Test," *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 2024, pp. 6771-6776, doi: 10.1109/ECCE55643.2024.10861353.

[C8] L. Gill, G. -S. Seo and A. J. Michaels, 'Real-Time Lifetime Prediction of Semiconductor Devices Using Hardware-in-the-Loop," *IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society*, Chicago, IL, USA, 2024, pp. 1-6, doi: 10.1109/IECON55916.2024.10905496.

[C9] L. Gill, J. C. Neely, L. Yates, R. J. Kaplar, and A. J. Michaels, "Multi-Objective Design Optimization of EV Inverter for Efficiency, Volume, and Reliability," *IEEE Transportation Electrification Conference and Expo (ITEC)*, Anaheim, CA, USA, 2025, pp. 1-6, doi: 10.1109/IECON55916.2024.10905496.

1.3 Dissertation Outline

This dissertation is structured in six chapters, with each chapter providing in-depth analysis related to the objectives and challenges identified in Section 1.2. Interdependencies between chapters have been minimized to ensure that each chapter can be read independently for the reader.

- **Chapter 2:** This chapter provides background information and a comprehensive literature review. It summarizes the fundamental principles of WBG device integration for high-performance power electronic systems. The current state-of-the-art in dynamic stress characterization, advanced measurement techniques, and optimal performance and lifetime analysis is described in detail, along with the key challenges and research gaps that motivate the work presented in this dissertation.

- **Chapter 3:** This chapter focuses on the classification and evaluation of dynamic switching stresses present in practical power conversion topologies. It establishes a systematic framework for classifying voltage and current stress profiles based on converter architecture, control strategies, and switching conditions. In-depth analysis is provided regarding how switching transition slew rates give rise to distinct electric field distributions—phenomena not captured by conventional static or DC-based assessments. Moreover. complementary experimental studies using multiple pulse testing (MPT) characterize the effect of switching dynamics on dynamic ON-resistance and charge trapping mechanisms in GaN cascode devices.

- **Chapter 4:** This chapter demonstrates the development of advanced measurement techniques to enable the seamless integration of WBG devices into practical systems. It presents the design and implementation of a novel on-state voltage measurement circuit, non-destructive inspection methods, and an automated test system for long-term,

continuous switching reliability evaluation. These techniques enable high-performance, real-time monitoring of key health and screening indicators to better understand device behavior and operation under dynamic stress conditions.

- **Chapter 5:** This chapter introduces optimal performance analysis and lifetime prediction techniques for integrated power electronic systems. It presents multi-objective design optimization using a genetic algorithm for an electric vehicle (EV) traction inverter, as well as lifetime prediction methods based on practical dynamic stress conditions of the integrated devices and the overall system. These techniques leverage artificial intelligence (AI) to aid the optimization process and to account for expected performance shifts under varying stresses and the diverse device behaviors revealed through dynamic characterization.

- **Chapter 6:** This chapter concludes the dissertation by summarizing the key findings and contributions. It also discusses the broader implications of the developed evaluation strategies for WBG device integration and outlines potential directions for future research.

Chapter 2

Background and Literature Review

2.1 Background Information

This section provides essential background information to establish the foundation information for the research presented in this dissertation. The background information on three key areas is presented, including the fundamental properties of WBG semiconductor materials and their impact on device performance, device characterization measurement techniques, and system-level optimization approaches in power electronic applications. By reviewing current practices as well as recent advancements, this chapter lays the groundwork for the challenges, limitations, and existing research gaps associated with each area to be further discussed in Section 2.2.

2.1.1 WBG Material Properties and Performance Implications

Advanced wide bandgap (WBG) semiconductor materials and WBG-based power devices are considered as key enabling technologies for next-generation, high-performance power electronic systems [19]. Si devices are approaching their theoretical physical limits, which constrains further improvements in system performance [5, 20, 21]. In contrast, WBG materials exhibit much superior intrinsic properties that translate to enhanced device- and system-level performance. The unique combination of wider bandgap energy, higher criti-

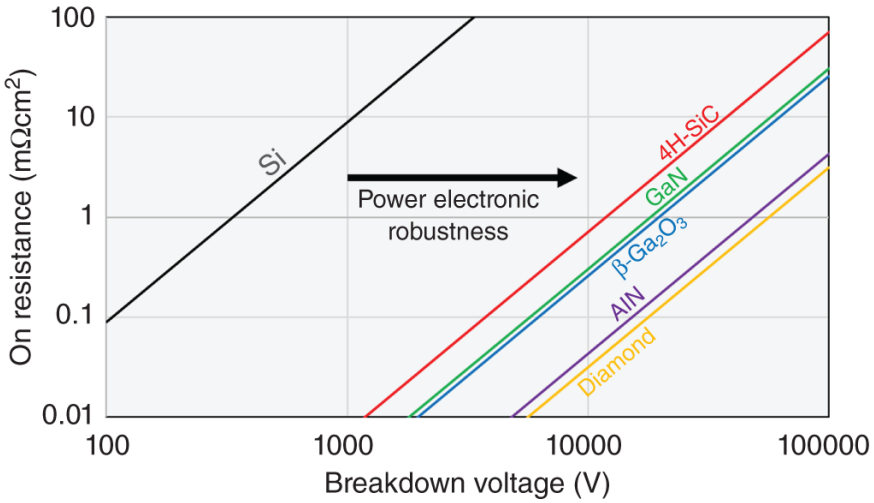


Figure 2.1: Relation of the on-resistance and the breakdown voltage of various power semiconductor device materials [18].

cal electric field strength, improved thermal conductivity, and faster carrier mobility allows WBG-based devices to operate at higher voltages, elevated temperatures, and increased switching frequencies, resulting in increased power density, reduced system volume, and improved overall efficiency [22, 23].

One of the advantageous characteristics of WBG materials is their larger bandgap energy relative to Si. For instance, 4H-SiC exhibits a bandgap of approximately 3.26 eV and GaN around 3.4 eV, compared to Si's 1.12 eV. AlN reaches even higher, with a bandgap of about 6.2 eV, as shown in Table 2.1. This wider bandgap allows devices to sustain higher electric fields before breakdown occurs while enabling thinner drift layers and lower on-state resistance. Another critical advantage is that the critical electric field strength of WBG materials is an order of magnitude greater than that of Si. SiC has a critical electric field of approximately 3 MV/cm and GaN about 4 MV/cm, compared to Si's relatively low value of 0.3 MV/cm. This key characteristic allows WBG devices to block higher voltages with a reduced chip area, which is essential to develop compact, high-efficiency designs.

Moreover, thermal conductivity is another important factor that differentiates WBG mate-

Table 2.1: Physical properties of wide bandgap semiconductors for power electronic applications in comparison to classic semiconductor materials.

	4H-SiC	GaN	AlN	β-Ga_2O_3	C	Si
Lattice parameter (Å)	$a = 3.08$	$a = 3.19$	$a = 3.11$	$a = 12.23$	3.57	5.43
Crystal Structure	Hexagonal	Hexagonal	Hexagonal	$b = 3.04$	Cubic	Cubic
				$c = 5.80$		
				$\beta = 103.7°$		
				Monoclinic		
E_G (eV)	3.2	3.44	6.2	4.8	5.5	1.1
E_B (10^5 V/cm)	30	40	150	80	100	3
ε	9.7	10.4	9.1	10	5.7	11.9
λ (W/cm/K)	3–5	1.3	2.9	0.23	20	1.5
v_S (10^7 cm/s)	2.5	2.5	$2.5^{approx.}$	2	2.7	1
μ_n (cm^2/V/s)	<900	<1000	300	250	<2200	1400
E_D (meV)	60 (N)	22 (Si)	90–250 (Si)	20–30 (Sn)		45 (P)
E_A (meV)	250 (Al)	160 (Mg)	500 (Mg)		400 (B)	44 (B)
T_S (°C)	2830	2500	3000	1740	3900	1420
Doping capability	n-type^{med}	n-type^{med}	n-type^{high}	n-type^{med}	n-type difficult	n-type
	p-type^{high}	p-type^{high}	p-type difficult	No p-type	p-type^{high}	p-type
Baliga FOM	500	1100	8100	1350	11,000	1
Johnson FOM	25	31	75	40	68	1

rials apart from the conventional semiconductor materials. SiC has a thermal conductivity in the range of 3–5 $W/cm \cdot K$, more than three times that of Si (1.5 $W/cm \cdot K$). GaN's bulk thermal conductivity is similar to that of Si (1.3 $W/cm \cdot K$) and AlN has a relatively high value, approximately 2.9 $W/cm \cdot K$. Diamond exhibits thermal conductivity of about 20 $W/cm \cdot K$. Thermal conductivity is an important aspect to facilitate more effective heat dissipation and management during high-power operation of power electronic systems. Thus, using WBG materials can thereby reduce cooling requirements and enhancing device reliability.

Carrier mobility and saturation velocity also play critical roles in determining the switching performance of WBG-based devices. Si has an electron mobility of approximately 1400 $cm^2/V \cdot s$, which historically contributed to its wide adoption in switch-mode power conversion applications. GaN demonstrates a higher electron mobility of about 2000 $cm^2/V \cdot s$, while diamond reaches up to 2200 $cm^2/V \cdot s$. The saturation velocity, which limits how quickly charge carriers can move through the material, is also higher in WBG materials compared to that of Si. Most WBG semiconductors, including SiC, GaN, and AlN, exhibit saturation velocities of around 2.5×10 cm/s, compared to Si's 1×10 cm/s. Hence, the combination of high electron mobility and high saturation velocity enables WBG devices to operate at higher switching frequencies and fast switching speed with lower energy losses.

The theoretical performance comparison of semiconductor materials for power conversion applications can be quantified using figures of merit (FOMs). Baliga's FOM combines dielectric constant, electron mobility, and critical electric field strength [24], while Johnson's FOM incorporates saturation velocity and critical electric field [25]. For instance, SiC and GaN exhibit Baliga's FOM values approximately 500× and 1100× that of Si, respectively, and Johnson's FOM values of about 25× and 31×, respectively. Materials such as AlN and diamond demonstrate higher theoretical relative Baliga FOMs, which are 8100× and

11,000×, respectively, showing promising potential for superior performance with the assumption that significant material and processing challenges can be addressed.

In summary, the intrinsic properties of WBG semiconductors provide a strong foundation for further advancements in power electronics. By utilizing higher voltage blocking capabilities, faster switching speeds, enhanced thermal performance, and increased power densities, WBG-based power conversion systems are well-suited to meet the demands of electrification, including electric mobility, energy storage integration, advanced grid systems, and aerospace and defense technologies. However, fully realizing these benefits requires overcoming material quality, fabrication, and reliability challenges through extended research in material processing, device fabrication, advanced converter design, packaging, and comprehensive dynamic characteristic understanding.

2.1.2 Device Characterization Measurement Fundamentals

WBG power devices exhibit distinct material and device-level characteristics compared to their Si counterparts, including higher breakdown voltages, faster switching speeds, and improved thermal performance. However, these benefits make WBG devices more sensitive to parasitic effects, dynamic degradation mechanisms, and manufacturing process complexities. Consequently, specialized measurement techniques and high-precision instrumentation are required to accurately capture their electrical and thermal behaviors under both static and dynamic conditions [26, 27, 28]. Comprehensive characterization is crucial to ensure that devices meet the specifications and qualification requirements when inserted into power conversion applications.

Static characterization measurements are the basis for extracting key device electrical parameters, performing quality assurance, screening for part-to-part variation, and product

qualification. Static tests are conducted under steady-state conditions using curve tracers, semiconductor parameter analyzers, or pulsed current and voltage (IV) systems to minimize self-heating effects. Important pulsed static characterization tests include output characteristics (I_D-V_{DS}), transfer characteristics (I_D-V_{GS}), threshold voltage (V_{TH}), on-state resistance (R_{ON}), breakdown voltage (BV_{DS}), gate leakage current (I_{GSS}), drain leakage current (I_{DSS}), and capacitance-voltage (C-V) measurements [29]. Some of these measurements are tested under different ambient temperatures to extract the temperature-sensitive electrical parameters [30, 31].

Transfer characteristics evaluate the device's gate control and conduction behavior by establishing the relationship between gate-source voltage (V_{GS}) and drain current (I_D) at a fixed drain-source voltage (V_{DS}). Such a measurement type is important in determining the threshold voltage (V_{TH}), which defines the gate voltage level required to turn the device from the OFF state to the conducting ON state. Any shift in V_{TH} over time has been used to indicate gate oxide degradation or interface trap generation, which are relevant failure modes for SiC MOSFETs [32, 33, 34, 35].

Output characteristics are measured as a family of I_D-V_{DS} curves at multiple gate-source voltages. These curves indicate how the drain current varies with the applied drain-source voltage throughout the linear and saturation regions. This characteristic defines the device's current-carrying capacity and how it affects conduction losses [36]. Moreover, the slope of the output characteristic curve in the linear region is used to extract the on-state resistance (R_{ON}), which is a critical parameter for conduction loss estimation, thermal design, and device state-of-health indicator [37, 38].

Breakdown voltage and leakage current measurements evaluate the device's ability to withstand high voltages without significant leakage current during the blocking or OFF state. This is a key parameter of WBG devices due to their high critical electric fields. Any devia-

tion from the specified breakdown voltage or an abnormal increase in leakage current indicate material defects, surface imperfections, or degradation mechanisms that may accelerate failure under sustained or switching high-voltage stress [39, 40]. Moreover, compromised devices pose safety concerns for the high-voltage power electronic systems. Therefore, precise characterization of these parameters ensures long-term device performance, degradation states, and reliability in high-voltage applications [41, 42, 43].

Capacitance-Voltage (C-V) measurements are important for switching power devices because these parameters provide detailed intrinsic device capacitance characteristics that affect dynamic switching performance. Key parameters include input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}), where they dictate the gate drive energy requirements, switching speed, susceptibility to cross-talk, and overall system efficiency from the charging and discharging of the stored energy [44, 45]. By measuring these capacitances across a range of drain-source and gate-source voltages, non-linear capacitance behavior and gate charge accumulation can be captured [46, 47]. Monitoring of these elements can be used to understand the influence of interfacial traps or charge spillover effects at high frequencies, leading to increased noise, performance degradation, and reliability issues [48]. The capacitance characterization is essential for accurate circuit modeling and simulation, as it determines the extent of Miller effect-induced delays, switching losses, and potential oscillatory behavior in high dv/dt environments typical of WBG devices [49, 50].

To complement static measurements, dynamic characterization techniques are employed to evaluate device behavior under switching and thermal conditions. These methods focus on measuring switching losses, transient voltage and current waveforms, dynamic or static R_{ON} behavior, reverse recovery characteristics, and parasitic effects that influence efficiency, power density, and electromagnetic compatibility that impact circuit performance at high frequencies and voltages [51, 52]. Figure 2.2 illustrates the typical approaches for device

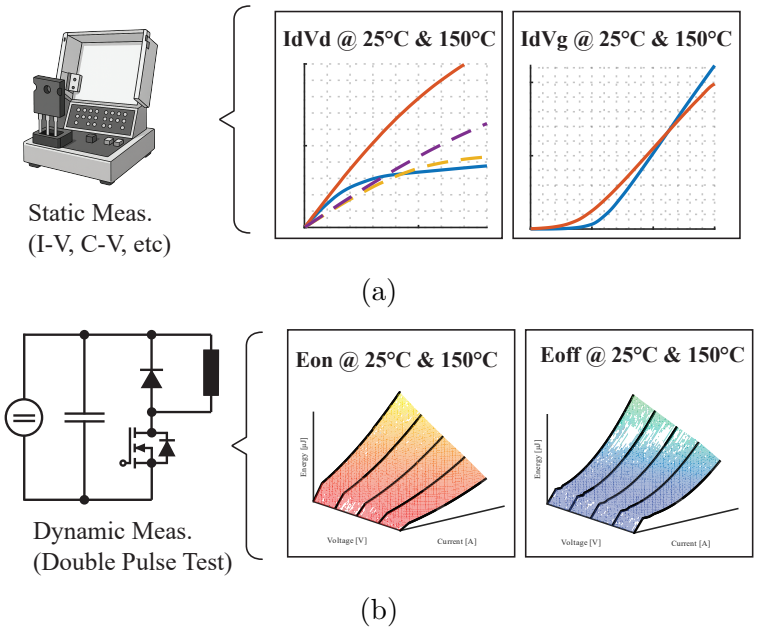


Figure 2.2: Overview of power device characterization methods: (a) static characterization using voltage and current sweeps to extract device-level parameters such as I_D-V_{DS}, I_D-V_{GS}, I_{GSS}, and C-V curves; and (b) dynamic characterization using an inductive-load double pulse test (DPT) to evaluate switching energy losses and transient behavior.

characterization methods, including static parameter extraction, as depicted in Figure 2.2(a) and dynamic performance analysis through an inductive load switching test, shown in Figure 2.2(b).

The double-pulse test (DPT) is a widely accepted approach for quantifying switching losses and transient waveforms under controlled inductive load conditions [53, 54]. Through a energy storing inductor, a desired current level during the first pulse is achieved, and the second pulse interrupts the current path, enabling measurement of turn-on and turn-off switching behaviors of the device [55]. By adjusting voltage and current levels, the DPT can emulate different converter operating points while obtaining switching energy, voltage overshoots, and di/dt and dv/dt effects [56].

Building on the DPT, advanced techniques such as multi-pulse tests [57], unclamped or clamped inductive switching setups [58, 59], and other measurement configurations [60,

61, 62, 63] are further employed to study losses and other stress effects, such as dynamic R_{ON} [64] and C_{oss} losses [65, 66]. These measurements are important when evaluating the devices' baseline losses, short-circuit handling robustness, heat management, and over-voltage ruggedness in switching conditions [67, 68, 69]. Furthermore, observation in parameter drifts after applying stresses like repeated switching allows understanding of long-term reliability and degradation mechanisms. In addition, HIL systems through integration of high fidelity device models can also be applied to investigate the device characterization and behavior impacting actual converter circuits' control dynamics in real-time, which bench-top tests may not be able to simulate and accelerate in a timely manner [70, 71, 72, 73].

Beyond capturing electrical transients, dynamic characterization also encompasses thermal and electrothermal interactions, which are closely coupled with switching behavior in WBG devices. Transient thermal impedance characteristic measurement [74, 75] and real-time monitoring of junction temperature during switching cycles [76, 77, 78] are important in understanding how heat generation and dissipation, and partial discharge can exacerbate dynamic degradation mechanisms, and affect the reliability of packaging materials and interconnects like solder joints [79, 80, 81], wire bonds [80, 82, 83, 84, 85], and insulation materials [86, 87, 88, 89].

In summary, dynamic characterization bridges the gap between static parameter measurements and the complex, real-world operating conditions under which WBG power devices experience. By measuring transient switching behavior, electrothermal interactions, stress effects, and material degradation, dynamic testing ensures seamless integration of WBG materials in practical, high-performance power electronic systems.

2.1.3 Optimization of Power Electronic System Performance

As power electronic systems become more integrated into critical infrastructures, such as grid interfaces, datacenters, and industrial power conversion, the demand for higher efficiency, compact integration, and reliable operation continues to increase. System performance depends not only on the intrinsic properties of WBG devices, but also on how effectively these devices and modules are integrated, controlled, and managed within the overall system architecture [90, 91, 92]. Optimization of system-level performance is therefore a complex challenge that requires a comprehensive understanding of electrical, thermal, mechanical, and control interactions through a holistic co-design approach that balances efficiency, power density, electromagnetic compatibility (EMC), and long-term reliability [93, 94, 95, 96, 97]. Moreover, performance objectives and trade-off considerations vary depending on the specific requirements and operating conditions of each application, as illustrated in Figure 2.3.

WBG-based power converters can achieve substantial gains in system-level efficiency through reduced conduction and switching losses, allowing higher-frequency operation and ability to reduce passive components. Efficiency can be further optimized through implementing different conversion stages while maintaining regulation over a wide range of input voltage conditions and varying load profiles, from light-load standby operation to full-load output [98, 99, 100]. Moreover, modular converter designs, such as multi-level inverters or interleaved phases, help distribute current stress and allow for phase shedding at light loads, which improves partial-load efficiency and reduces losses [101, 101, 102, 103, 104]. Other techniques include soft-switching schemes, such as zero-voltage switching (ZVS) or zero-current switching (ZCS), and resonant topologies to further minimize loss during switching transitions [93, 105, 106, 107].

Power density is another key performance metric driven by the high-frequency switching ca-

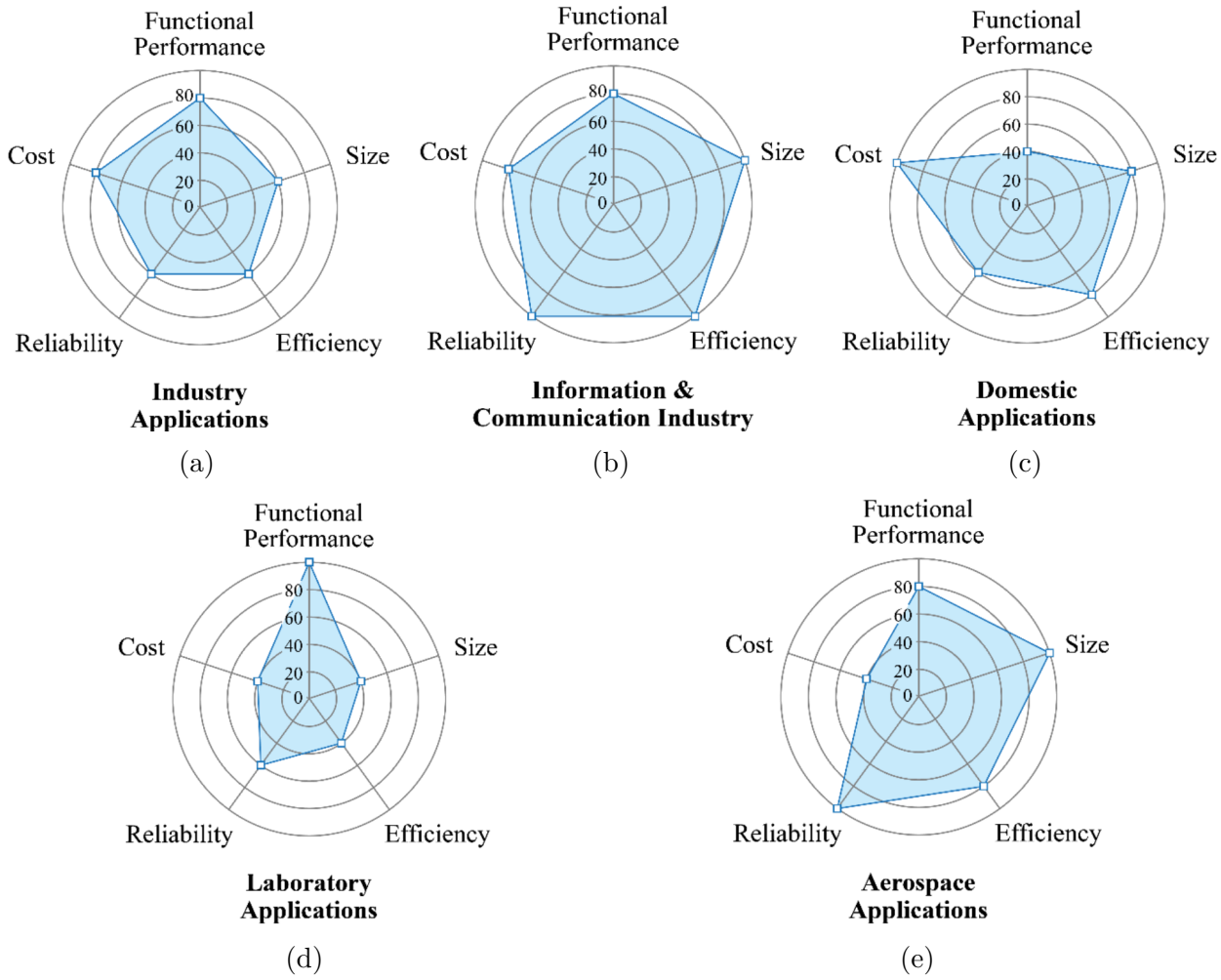


Figure 2.3: Comparison of functional performance and trade-offs across different application scenarios, illustrating: (a) industry applications, (b) information & communication industry, (c) domestic applications, (d) laboratory applications, and (e) aerospace applications [108].

pability of WBG devices. Higher switching frequencies allow for reduced passive component sizes and more compact layouts [109, 110]. High-frequency transformers, planar magnetics, and air-core transformers are integrated with WBG-based converters to maintain high efficiency while supporting galvanic isolation and compact form factors [111, 112, 113].

At the control level, advanced digital techniques such as model predictive control (MPC), adaptive modulation, machine learning, and dead-time optimization are critical for achieving the desired switching and stability dynamics of novel topologies and modular architec-

tures [114, 115, 116, 117]. These control schemes adjust switching behavior based on analog or digital feedback from output voltage and current ripple measurements to improve overall performance [114, 118, 119, 120].

Reliability and lifetime remain critical metrics when optimizing system performance with WBG devices. While higher junction temperatures and faster switching operation enhance power density performance, poor design and selection of heat sinks, thermal interface materials, and active thermal management can accelerate degradation in packaging materials, interconnects, and interfaces [121, 122, 123, 124]. Power cycling, thermal cycling, and high-frequency stress testing data can be used to predict wear-out mechanisms like die-attach delamination, wire bond lift-off, or solder fatigue, enabling reliability-optimized power electronic systems [125, 126, 127, 128, 129, 130].

With the tightly interconnected nature of these performance metrics in power electronic systems, multi-objective trade-off strategies are essential for achieving balanced system optimization. These metrics present competing objectives, since improving one objective can negatively impact another. For example, increasing switching frequency can enhance power density via reduced passive component size, but may worsen electromagnetic interference (EMI) emissions and thermal constraints. In contrast, operating at lower switching frequencies can increase efficiency and alleviate stringent thermal management but increase overall system volume [131, 132, 133]. Multi-objective optimization frameworks, such as Pareto front analysis and evolutionary algorithms, provide a systematic way to evaluate and quantify these trade-offs [95, 134, 135, 136].

In summary, the optimization of system performance for WBG power electronic applications is a complex, multi-domain challenge. By systematically connecting detailed device characterization to various domains of power electronic system, such as electrical, thermal, mechanical, and control, co-optimized designs for next-generation power converters that de-

liver superior efficiency, higher power density, enhanced EMI performance, and extended operational lifetime can be realized.

2.2 Challenges and Research Gaps

This section outlines three key research gaps that remain in WBG technology. First of all, there are knowledge gaps in the dynamic behavior of WBG devices, such as field-induced charge trapping and performance shifts under fast switching. Second, existing measurement and qualification methods are inadequate for capturing WBG devices' high-speed switching phenomena or enabling accurate in-situ monitoring. Third, system-level design lacks predictive, multi-objective co-optimization strategies that incorporate real-time lifetime modeling. These challenges are discussed in Subsections 2.2.1, 2.2.2, and 2.2.3.

2.2.1 Dynamic Switching Environments on WBG Device Operation and Physical Mechanisms

While the fundamental material properties of WBG materials can enable superior device-level performance, the full potential realization in practical applications is constrained by complex physical phenomena caused by dynamic switching conditions. Unlike idealized DC or static operation scenarios, high-frequency, time-varying AC or pulsed switching waveforms subject the devices to rapidly changing electric and magnetic fields, which generate dynamic charge transport and trapping mechanisms [137, 138, 139]. As a result, non-DC biased or pulsed stress conditions pose unique challenges that traditional static models cannot replicate and capture the unique physical phenomenon of WBG materials in harsh switching environments [140, 141].

For instance, in AlGaN/GaN HEMTs, surface states, interface traps, and defects within heterostructures or at field plates interact with time-varying electric fields during dynamic switching. The spatial distribution and temporal evolution of electric fields within GaN HEMTs or cascode configurations are affected by the applied voltage and current waveforms, including pulse duration, slew rates, and transient oscillations. During fast switching transients, localized electric field peaks can form at critical regions and these localized fields can exceed the maximum operating limits, leading to a potential underestimation of failure risks in switching converter operation.

These dynamic electric field interactions cause charge trapping and detrapping mechanisms, which influences I-V characteristic shifts, efficiency degradation, thermal overstress, and cumulative impacts on both short-term performance and long-term reliability. Although static characteristics appear stable under standard DC bias conditions, dynamic shifts can occur depending on various factors, including switching speed, duty cycle, and waveform shapes. To illustrate this fundamental phenomenon, Figure 2.4 compares the I-V characteristics under DC and pulsed bias conditions, highlighting the effects of charge trapping in AlGaN/GaN HEMT structures with the conventional fabrication process as well as fluorine ion implantation in the thin AlGaN barrier layer (FBL) and the SiN_x passivation layer (FPL HEMT) [142].

Furthermore, advanced power conversion systems employ topologies that introduce diverse dynamic stress profiles, which vary largely with switching states, control strategies, and changing source or load conditions. As a result, a single static test condition cannot represent the full aspect of varying dynamic stresses that WBG devices encounter in practical applications. This research gap highlights the need for systematic frameworks to classify and analyze these varying operating conditions, and how switching effects, in particular, slew rates play a critical role in governing the underlying physical mechanisms and influence

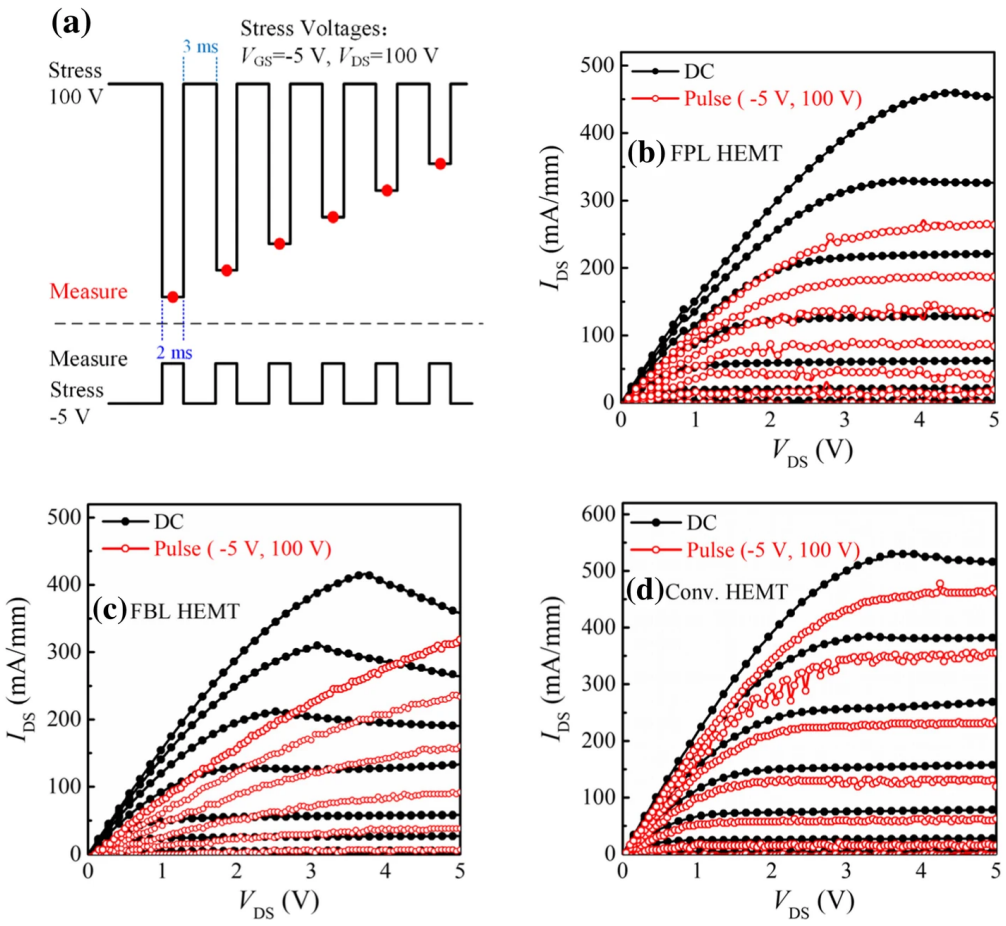


Figure 2.4: Illustration of different GaN I-V performance comparison between DC and pulsed: (a) schematic depicting the stress voltage of the pulsed I_D-V_{DS} measurements, (b) I_D-V_{DS} with FPL HEMT, (c) I_D-V_{DS} with FBL HEMT, and (d) I_D-V_{DS} with Conv. HEMT (VGS=−4 0 V; step: 0.5 V) [142]

the trapping to impact the dynamic on-state behavior of WBG devices over different rates of switching transients.

To address these challenges, Section 3.2 explores how dynamic stresses exhibit across representative power converter topologies while Section 3.3 examines the fundamental effects of switching slew rates from both a device physics and electrical performance perspective. Through the introduction of an in-depth classification of switching categories as well as both device physics simulation results and experimental results on the effects of high-field switch-

ing slew rates, Chapter 3 overall aims to bridge the gap between the theoretical device- or material-level performance and the practical operational behavior of WBG devices under realistic dynamic conditions.

2.2.2 Advanced Characterization Measurement Techniques for WBG Device Performance and Qualification

While WBG devices offer competitive advantages as laid out in Subsection 2.1.2, several technical challenges and research gaps continue to exist, hindering their effective qualification and widespread adoption in advanced power electronic systems. These challenges include the need for higher-quality measurement capabilities, advancement of specialized techniques for robust device qualification, and the development of automated, flexible test systems that can leverage large datasets for long-term reliability evaluation, potentially integrated with AI-driven analytics or digital engineering.

One fundamental challenge is achieving extremely high-quality measurement of device parameters under switching stresses, which is essential for evaluating WBG device performance in switch-mode power applications. From a performance evaluation perspective, this requires high-resolution, low-noise measurement of dynamic electrical parameters, such as on-state voltage drops under different operating conditions [140, 141]. This parameter is a key indicator of device state-of-health, including static and dynamic on-resistance shifts [64, 76, 124, 143, 144, 145, 146, 147]. However, conventional measurement circuit designs introduce challenges and limitation in measurement uncertainties, parasitic ringing, and noise, caused by very fast switching transitions and high dv/dt and di/dt rates that characterize WBG devices. Furthermore, standard off-the-shelf voltage and current sensing probes introduce measurement-induced perturbations, and further degrade data quality and

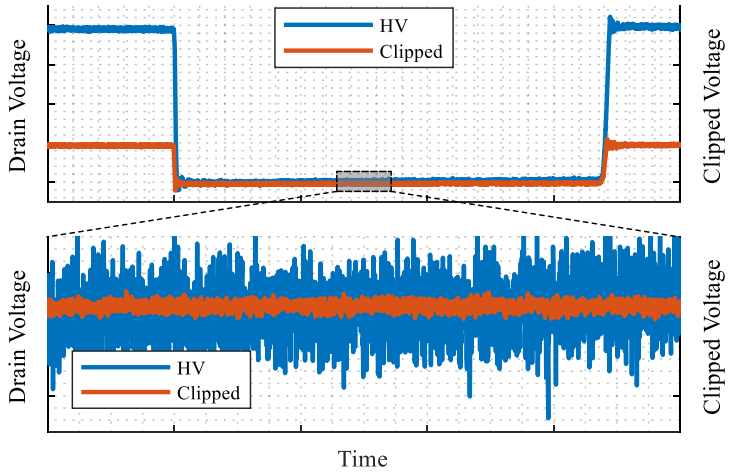


Figure 2.5: Illustration of high-voltage switching waveform and clipped-voltage waveform measurement. The bottom panel depicts a close-up view of the two waveforms in the on-state and highlights the lower resolution of the high-voltage switching waveform compared to the higher resolution data for the clipped voltage measurement, which allows for a more accurate estimation of on-resistance during the conduction state.

accuracy.

For instance, to enable high resolution of detailed on-state measurement betweem switching states, a clipper circuit is required to limit the high-voltage signal during the off-state while providing a high-resolution measurement capability during the on-state. Figure 2.5 illustrates the measurement challenge when a high-voltage switching waveform results in poor resolution quality and low accuracy of data, whereas the clipped voltage waveform provides higher resolution due to a smaller voltage peak required for the probe to measure, thereby increasing accuracy of the on-state voltage. Therefore, advanced circuit designs and measurement methodologies are required to isolate device behavior from irrelevant test setup artifacts while only retaining the relevant device parameter information. Moreover, addressing these limitations lead to integration of in-situ monitoring techniques that capture transient switching behaviors and degradation effects over a long period of time.

The second key challenge is advancing measurement techniques for device technology qualification, ideally through non-destructive screening methods and robust production acceptance

testing frameworks. Significant hurdles are encountered during the manufacturing and fabrication of WBG devices, especially as manufacturers try to increase wafer sizes to reduce unit costs and improve economies of scale. These elements contribute to added complexity to maintaining high yield and consistent device quality [148, 149]. Other challenges include improving crystal growth processes, controlling defect densities, and managing processing temperatures [150, 151].

These fabrication challenges directly impact the uniformity and reliability of the fabricated devices. While conventional static screening tests can detect major defects or obvious outliers [152], they cannot predict how subtle variations introduced during processing influence dynamic switching behavior, thermal impedance, or circuit-level performance once the devices are integrated into actual converter systems. As production volumes scale up, these issues can lead to uneven current sharing, increased power loss, or unexpected reliability failures when multiple devices operate in parallel within modules or stacks [153, 154, 155, 156].

Hence, to strengthen confidence in WBG device acceptance across varying production lots, it is essential to integrate dynamic screening and qualification processes that can detect latent defects and process-induced variations. Figure. 2.6 illustrates part variability of WBG device characterization measurements across the sample population, highlighting large sample deviations from the overall population mean. Establishing advanced, non-destructive screening strategies that capture both static and dynamic characteristics is required to ensure consistent device quality and performance margins [157].

A final challenge is the development of test automation capabilities that support repeatable, long-term reliability and robustness of WBG devices under realistic dynamic operating conditions. While established semiconductor standards, such as Automotive Electronics Council (AEC)-Q101 for automotive qualification [158], Joint Electron Device Engineering Council (JEDEC) JESD22-A104 for temperature cycling [159], JESD22-A122 for power cycling [160],

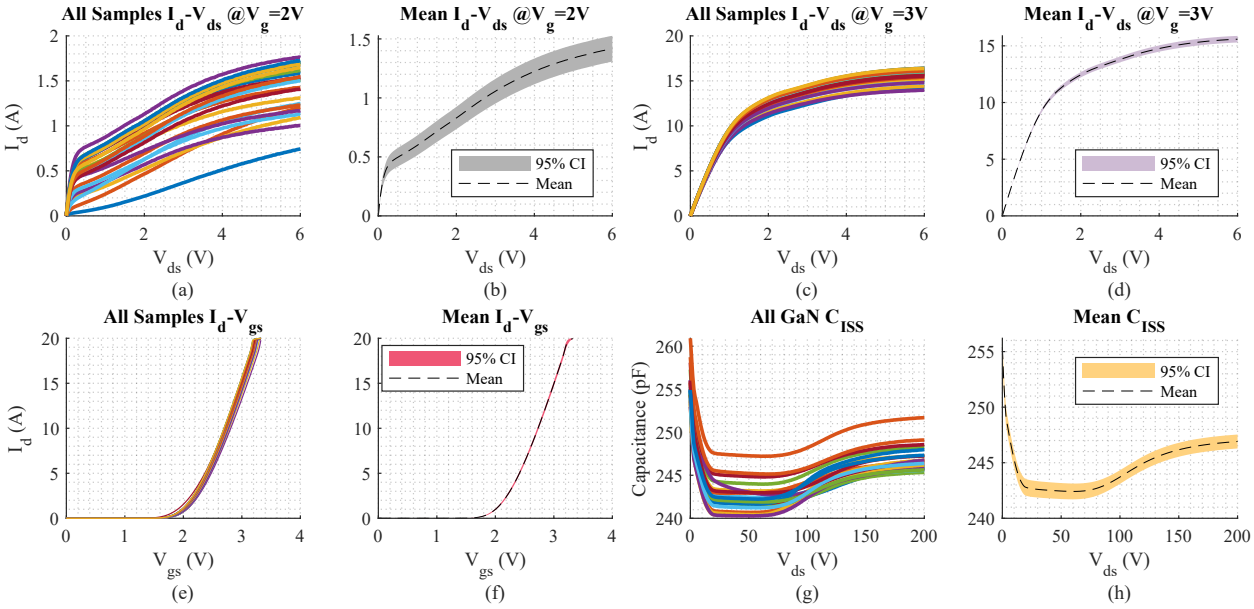


Figure 2.6: Measured part-to-part variations of GaN HEMTs: (a) all device sample output characteristic, $I_{\mathrm{D}}-V_{\mathrm{DS}}$ at $V_{\mathrm{GS}} = 2$ V , (b) population mean and 95% CI of $I_{\mathrm{D}}-V_{\mathrm{DS}}$ at $V_{\mathrm{GS}} = 2$ V , (c) all device sample output characteristic, $I_{\mathrm{D}}-V_{\mathrm{DS}}$ at $V_{\mathrm{GS}} = 3$ V , (d) population mean and 95% CI of Id −Vds at $V_{\mathrm{GS}} = 3$ V , (e) all device sample transfer characteristics, $I_{\mathrm{D}}-V_{\mathrm{DS}}$, (f) population mean and 95% CI of $I_{\mathrm{D}}-V_{\mathrm{GS}}$, (g) input capacitance, C_{iss} of all device samples, and (h) mean and 95% CI of C_{iss}.

JESD22-A110 for Highly Accelerated Stress Test (HAST) [161], JESD22-A108 for bias and operating life [162], and International Electrotechnical Commission (IEC) 61000-4-5 for surge immunity [163], provide baseline qualification guidelines, the demanding application environment of WBG necessitates the evaluation across the full spectrum of stress conditions. Thus, to understand the operational limits, degradation behavior, and failure mechanisms of WBG technologies, there is a growing need to go beyond the well-established standardized test protocols like AEC, JEDEC, and IEC.

In short, the absence of standardized dynamic test methods and universally accepted metrics for WBG devices poses an industry-wide barrier. Ensuring measurement repeatability, cross-laboratory consistency, and correlation with real-world field performance becomes essential for WBG technology qualification . Addressing this gap requires a development of

highly flexible and customizable test platforms capable of evaluating a range of converter topologies and operating scenarios. Furthermore, by enabling structured and comprehensive data acquisition, the testing platform should provide a foundation for integrating machine learning approaches aligned with FAIR (Findable, Accessible, Interoperable, Reusable) data principles [164, 165, 166].

Chapter 4 addresses these challenges by presenting the development of a novel measurement circuit topology, non-destructive screening technique for WBG parts, and an automated dynamic test platform that enables high-voltage, high-power WBG device characteristics and the integrated system performance. Section 4.2 focuses on the design, modeling, and validation of the novel circuit topology for high-precision on-state voltage measurement. Section 4.3 introduces the impact of the part-to-part variability in converter performance along with a dynamic screening methodology to quantify the part variability across devices. Section 4.4 details the development of the automated test architecture designed for both short- and long-term reliability evaluation under realistic switching conditions.

2.2.3 Multi-Objective Optimization of Power Electronic Systems and Predictive Lifetime Analysis

Achieving optimal system-level design in power electronic systems requires careful coordination among electrical, thermal, mechanical, and control domains. These interactions introduce complex trade-offs between key performance objectives such as efficiency, power density, and reliability [167]. Addressing these trade-offs demands not only cross-domain knowledge, but also a well-structured co-design process. In addition, predicting the lifetime behavior of WBG devices under application-specific operating conditions remains a technical gap.

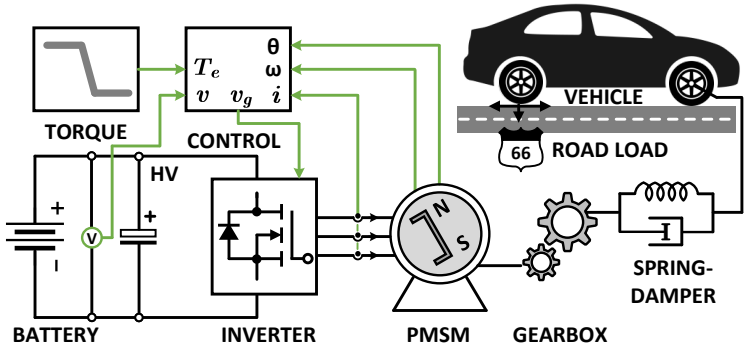


Figure 2.7: Electric vehicle powertrain system diagram with power electronics, control, mechanical, and energy storage subsystems.

The first challenge is in developing multi-objective optimization methodologies for complex power electronic systems. Conventional approaches target isolated performance metrics, such as minimizing magnetic losses or reducing heatsink volume [168, 169, 170] without fully accounting for cross-domain interactions involving material properties, application dynamics, and control strategies. This lack of comprehensive perspective results in suboptimal designs that meet one objective while compromising others.

Effective system-level co-optimization requires an integrated understanding of different device technologies (e.g., IGBT, SiC MOSFET, GaN HEMT), magnetic core materials (e.g., ferrite, silicon steel, amorphous alloys), thermal management schemes (e.g., fan speed control, liquid cold plate flow rates), and energy storage components (e.g., ceramic, film, or electrolytic capacitors). Moreover, electrical design parameters, such as switching frequency, DC-link capacitance, filter inductance, and voltage regulation constraints including ripple and transient response, should be considered holistically. Figure 2.7 shows various components integrated into an EV power system. The component constituents and design factors should be evaluated under varying load conditions to ensure optimal performance considering the system's full operating range of the entire driving cycle.

The next challenge involves the development of lifetime prediction methodologies that accu-

rately reflect real device characteristics and their associated operating conditions. Traditional reliability qualification techniques, such as power cycling, HTRB (High-Temperature Reverse Bias), or HTGB (High-Temperature Gate Bias) [171, 172], are static in nature. While these static tests reveal specific failure modes or degradation mechanisms, there are limitations in interconnecting the static-biased-driven failures with the dynamic electrical and thermal stresses encountered during actual converter operation. Furthermore, they lack the ability to assess the device's state-of-health in real time, which is essential for field-deployable power electronics.

Addressing this gap requires real-time lifetime monitoring frameworks capable of capturing and interpreting cumulative device stress in-situ. Continuous tracking of key stressors, such as junction temperature, switching energy, and other relevant device parameters, is essential for estimating the remaining useful life (RUL) of power devices. HIL environments offer a promising platform for this purpose, as they can emulate dynamic converter operating conditions [173, 174, 175, 176] while integrating lifetime information [177, 178, 179]. The validation and refinement of lifetime estimation techniques can be investigated through HIL prior to field deployment. Therefore, a real-time lifetime estimation of power devices in HIL environments is necessary to facilitate early detection of failure precursors, support predictive maintenance strategies, and ultimately reduce system downtime while extending the operational lifetime of power electronic systems.

Lastly, WBG device lifetime data can consist of various data types, including high-dimensional baseline characterization data, time-series switching waveforms, and intermittent temperature data. Processing of the characterization of large volumes of data across electrical waveforms, thermal maps, reliability, and switching loss profiles by manual or statical model fitting becomes infeasible and ineffective [180]. Therefore, AI-enabled techniques, such as deep learning models, especially those that integrate multiple data modalities (e.g., CNNs for

waveform patterns, MLPs for scalar features), can extract subtle part variation or degradation signatures, forecast device failures, and support predictive lifetime modeling. However, integrating such models into practical converter systems requires careful data management, interpretability analysis, and architecture design [181, 182].

Chapter 5 addresses these challenges by introducing a comprehensive methodology for multi-objective optimization and lifetime prediction in WBG-based converters. Section 5.2 presents co-simulation models and Pareto front analysis applied to EV traction inverter and PFC use cases through design trade-offs between loss, volume, and reliability. Section 5.3 introduces a real-time HIL framework for RUL estimation under varying load conditions. Section **??** explores a deep learning fusion network trained on high-dimensional datasets to predict device lifetime.

2.3 Summary

This chapter established the background of the dissertation by examining relevant literature and state-of-the-art technologies across each topic area. It identified key challenges and existing research gaps, in particular related to the material- and device-level physical impacts of harsh switching conditions, dynamic stress characterization through device parameter measurement, lifetime prediction, and reliability qualification frameworks. These gaps form the foundation for the research objectives, methodologies, and technical contributions presented in the subsequent chapters.

Chapter 3

Dynamic Switching Stress Classification and Evaluation

This chapter focuses on the classification and evaluation of dynamic switching stresses encountered in practical power conversion topologies. Section 3.1 introduces various categories of dynamic stresses in power converters, including characteristics of switching voltage levels, current waveform shapes, and switching schemes such as hard- or soft-switching. A systematic framework is developed to classify voltage and current stress signatures based on converter architecture, control strategy, and operating conditions. Moreover, Section 3.2 presents a detailed analysis of how dynamic stresses, in particular, switching slew rates, induce distinct electric field distributions within the device structure, which are not accurately captured by conventional static or DC-based assessments.

3.1 Dynamic Stresses in Power Converters

Dynamic switching stresses vary greatly across converter topologies, depending on switching node configurations, control schemes, and operating conditions. Subsection 3.1.1 categorizes these stress profiles with respect to typical power converter architectures. Moreover, in GaN HEMTs, dynamic stresses can induce pronounced effects due to hot carrier injection and charge trapping, leading to the phenomenon of dynamic on-resistance during switch-

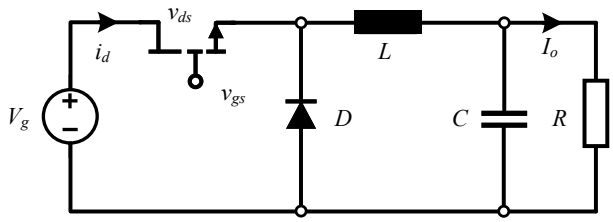
ing transitions. Therefore, Subsection 3.1.2 presents a comprehensive literature review to provide in-depth analysis into the physical mechanisms and behavioral implications of this phenomenon.

3.1.1 Stress Categories Based on Converter Topologies

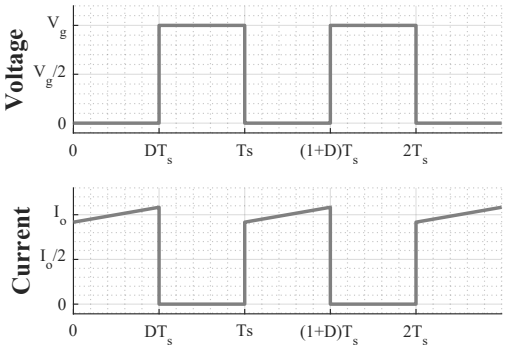
A complete and accurate understanding of device switching conditions under practical operating modes is essential to evaluate the impact of dynamic stresses as well as to optimize the power conversion circuit design. For example, the drain current during the conduction interval can exhibit varying waveforms, such as trapezoidal, triangular, or sinusoidal, depending on the mode of operation, including continuous conduction mode (CCM), discontinuous conduction mode (DCM), or based on the specific converter topology. Parameters such as current ripple, load current, and duty cycle further influence the current profile and associated charge trapping behavior. Furthermore, both the magnitude and shape of the switching voltage can play a critical role in the evolution of the physical behaviors of the device. Thus, distinct converter topologies impose unique electrical stress profiles on the device, leading to unique degradation mechanisms.

Figure 3.1 illustrates several classes of practical power conversion circuit topologies that are suitable for WBG devices. For each topology, key operational characteristics, such as device voltage and current stress profiles, are illustrated.

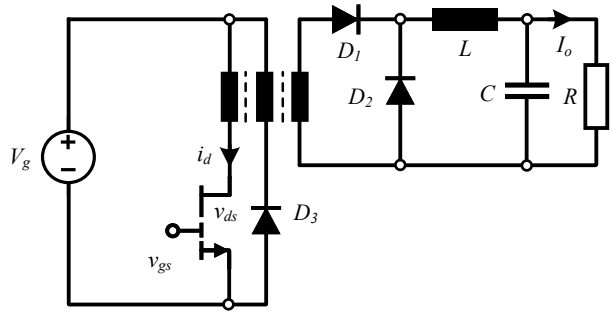
One example is the asynchronous buck converter, shown in Figure. 3.1(a), a fundamental DC–DC step-down topology that regulates a lower output voltage using passive energy storage components. As depicted in Figure 3.1(b), the voltage stress in this topology typically follows a two-level waveform, while the corresponding current waveform resembles a trapezoidal profile.


v_{ds}
i_d
L
I_o
v_{gs}
V_g
D
C
R

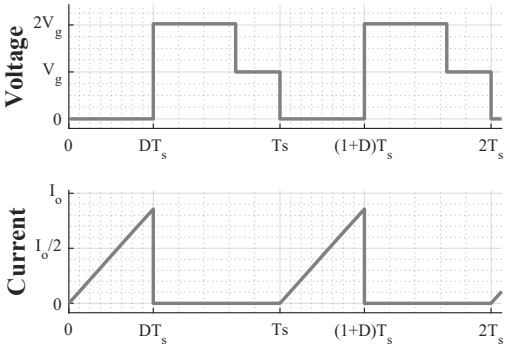
(a)


Voltage
V_g
$V_g/2$
0
0
DT_s
Ts
$(1+D)T_s$
$2T_s$
Current
I_o
$I_o/2$
0
0
DT_s
Ts
$(1+D)T_s$
$2T_s$

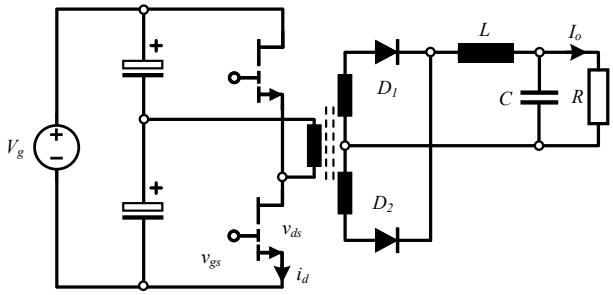
(b)


D_1
L
I_o
D_2
C
R
V_g
i_d
v_{ds}
D_3
v_{gs}

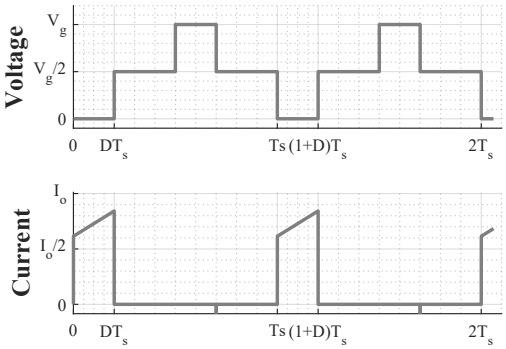
(c)


Voltage
$2V_g$
V_g
0
0
DT_s
Ts
$(1+D)T_s$
$2T_s$
Current
I_o
$I_o/2$
0
0
DT_s
Ts
$(1+D)T_s$
$2T_s$

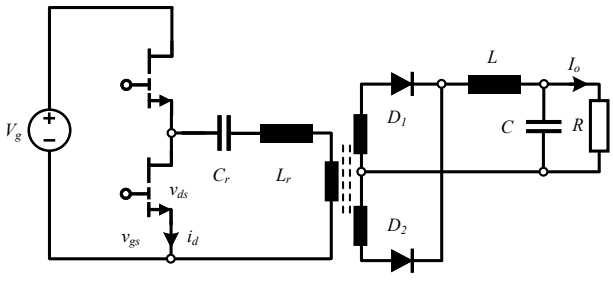
(d)


L
I_o
D_1
C
R
V_g
D_2
v_{ds}
v_{gs}
i_d

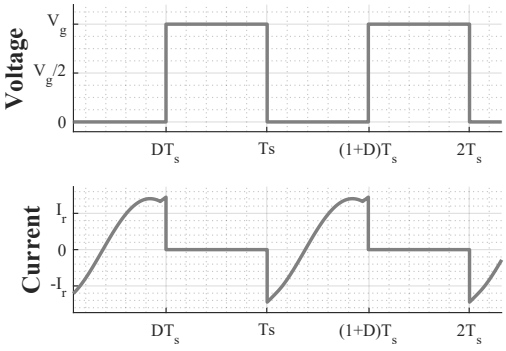
(e)


Voltage
V_g
$V_g/2$
0
0
DT_s
Ts $(1+D)T_s$
$2T_s$
Current
I_o
$I_o/2$
0
0
DT_s
Ts $(1+D)T_s$
$2T_s$

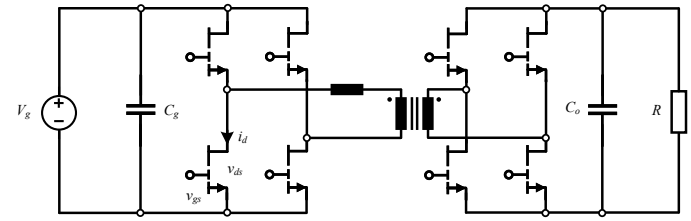
(f)


L
I_o
D_1
C
R
V_g
C_r
L_r
v_{ds}
v_{gs}
i_d
D_2

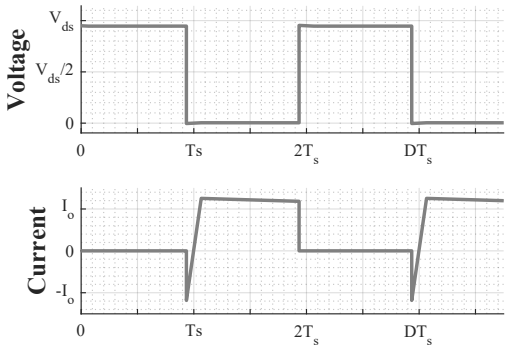
(g)


Voltage
V_g
$V_g/2$
0
DT_s
Ts
$(1+D)T_s$
$2T_s$
Current
I_r
0
$-I_r$
DT_s
Ts
$(1+D)T_s$
$2T_s$

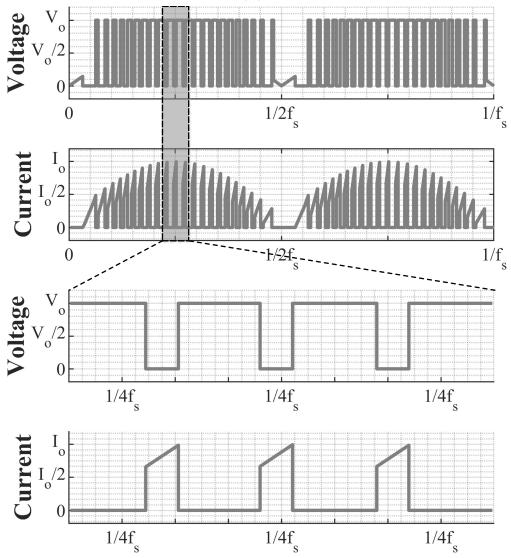
(h)


V_g
C_g
i_d
v_{ds}
v_{gs}
C_o
R

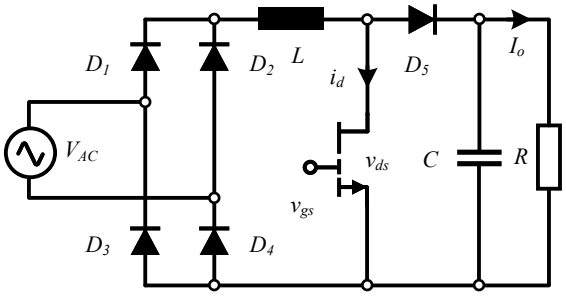
(i)


Voltage
V_{ds}
$V_{ds}/2$
0
Ts
$2T_s$
DT_s
Current
I_o
$-I_o$

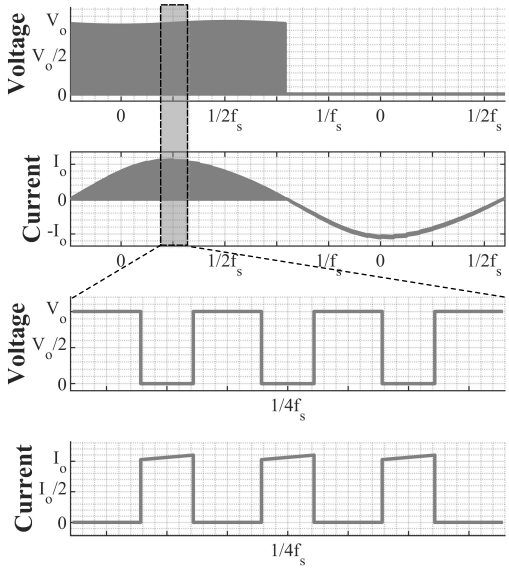
(j)


Voltage
V_o
$V_o/2$
$1/2f_s$
$1/f_s$
Current
I_o
$I_o/2$
$1/4f_s$

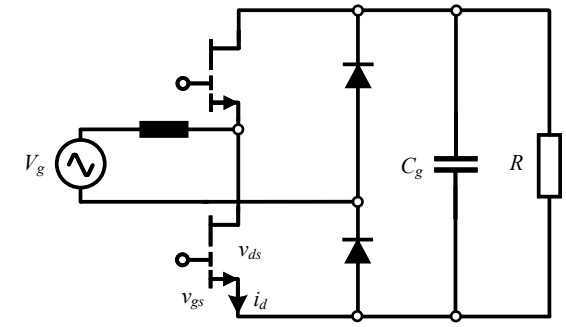
(l)


D_1
D_2
L
i_d
D_5
I_o
V_{AC}
v_{ds}
C
R
v_{gs}
D_3
D_4

(k)


Voltage
V_o
$V_o/2$
$1/2f_s$
$1/f_s$
Current
I_o
$-I_o$
$1/4f_s$

(n)


V_g
C_g
R
v_{ds}
v_{gs}
i_d

(m)

Figure 3.1: Summary of power converter topologies and corresponding voltage/current stress waveforms: (a) Buck Converter, (b) Buck Waveforms, (c) Forward Converter, (d) Forward Waveforms, (e) Half-Bridge, (f) Half-Bridge Waveforms, (g) LLC Resonant, (h) Resonant Waveforms, (i) Dual Active Bridge, (j) DAB Waveforms, (k) Boost PFC, (l) Boost PFC Waveforms, (m) Bridgeless Totem-Pole PFC, and (n) Bridgeless PFC Waveforms.

A forward converter, shown in Figure. 3.1(c), is a DC–DC topology that enables both voltage transformation and galvanic isolation between input and load. As illustrated in Figure 3.1(d), the voltage stress on the switching device exhibits a three-level waveform, while the corresponding current stress profile follows a triangular shape.

The half-bridge and LLC resonant converters, depicted in Figure 3.1(e) and Figure. 3.1(g), respectively, are also isolated DC–DC converters capable of stepping the output voltage either above or below the input level. These topologies utilize a transformer to achieve voltage conversion and isolation. In the case of the half-bridge converter, the device experiences a three-level voltage stress and a trapezoidal current waveform, as shown in Figure. 3.1(f).

The LLC resonant converter employs a resonant network, which is often referred to as a resonant tank, to enable power transfer. Due to its resonant operation, the current stress waveform is sinusoidal in nature, while the voltage stress remains a two-level profile, as illustrated in Figure. 3.1(h).

Lastly, the boost power factor correction (PFC) converter, shown in Figure. 3.1(i), is an AC–DC topology designed to shape the input current to be in phase with the input voltage. The corresponding voltage and current stress profiles are depicted in Figure. 3.1(j), where the voltage exhibits a continuous two-level waveform. The device current typically follows a low-frequency sinusoidal envelope, with a trapezoidal or constant shape within individual switching cycles.

While many other converter topologies and associated stress profiles exist, the examples

provided in Figure. 3.1 represent a representative subset of practical architectures and their corresponding device-level electrical stress characteristics.

Table 3.1 categorizes representative circuit topologies according to key attributes. These include conversion type (DC–DC, AC–DC, DC–AC, or AC–AC), bridge configuration (where "bridgeless" denotes single-transistor implementations and "bridge-based" refers to half- or full-bridge structures), voltage and current stress profiles (e.g., two-level or three-level voltage, and triangular, trapezoidal, or sinusoidal current waveforms), electrical isolation (isolated vs. non-isolated), and switching mode (hard vs. soft switching).

While Table 3.1 highlights widely used architectures, application-specific topologies not included here should be analyzed similarly by identifying their operational mission profiles and switching sequences, which may introduce unique stress conditions depending on control strategy and waveform characteristics. Furthermore, prior studies have largely overlooked how topology-specific factors, such as voltage waveform shape, current profile, and conversion class, affect dynamic device behavior. Therefore, a comprehensive characterization approach that evaluates dynamic stress behavior and degradation mechanisms of WBG devices, especially in GaN HEMTs under application-relevant waveform conditions and varying stress levels is essential.

3.1.2 Review of Dynamic On-Resistance in GaN Devices

As WBG technology continues to evolve, GaN devices still face key operational challenges [183, 184]. One of the most critical issues is the increase in on-state resistance during switching transitions, known as dynamic on-resistance ($d\mathrm{R}_{\mathrm{DS(ON)}}$), or "current collapse" [185]. This phenomenon describes a reduction in drain current due to transient charge trapping, resulting in an elevated on-resistance compared to the device's steady-state DC value. The

Table 3.1: Summary of converter topologies and electrical waveform categories.

Topology	**Conversion**	**Bridge Type**	**Voltage Waveform**	**Current Waveform**	**Isolation**	**Switching Mode**
Buck	DC–DC	Bridgeless	2-level	Trapezoidal	Non-isolated	Hard
Boost	DC–DC	Bridgeless	2-level	Trapezoidal	Non-isolated	Hard
Buck-Boost	DC–DC	Bridgeless	2-level	Trapezoidal	Non-isolated	Hard
Flyback	DC–DC	Bridgeless	2-level	Trapezoidal	Isolated	Hard
Forward	DC–DC	Bridgeless	3-level	Triangular	Isolated	Soft (ZCS)
Boost PFC	AC–DC	Bridgeless	2-level	Trapezoidal	Non-isolated	Hard
Push-Pull	DC–DC	Bridgeless	3-level	Trapezoidal	Isolated	Hard
Half-Bridge	DC–DC	Half-Bridge	3-level	Trapezoidal	Isolated	Hard
Full-Bridge	DC–DC	Full-Bridge	3-level	Trapezoidal	Isolated	Hard
Totem-Pole PFC	AC–DC	Half-Bridge	2-level	Trapezoidal	Non-isolated	Hard
Three-Phase VSI	DC–AC	Half-Bridge	2-level	Trapezoidal	Non-isolated	Hard
Single-Phase VSI	DC–AC	Full-Bridge	2-level	Trapezoidal	Non-isolated	Hard
Half-Bridge LC-SLR	DC–DC	Half-Bridge	2-level	Sinusoidal	Non-isolated	Soft (ZVS/ZCS)
Half-Bridge LLC	DC–DC	Half-Bridge	2-level	Sinusoidal	Isolated	Soft (ZVS/ZCS)
Dual Active Bridge	DC–DC	Full-Bridge	2-level	Trapezoidal	Isolated	Soft (ZVS)

primary mechanism underlying $d\mathrm{R}_{\mathrm{DS(ON)}}$ is electron capture and emission within trap states distributed across different device layers, as confirmed by deep-level transient spectroscopy (DLTS), photoionization studies, and numerical simulations [186, 187, 188, 189].

In power-switching applications, this dynamic behavior has a direct impact on converter efficiency and thermal management, particularly due to increased R_{ON}-induced self-heating [190, 191, 192, 193]. Recent studies using TCAD simulations and experimental validation have identified key operating parameters, such as voltage, current levels, and temperature, that influence the onset and severity of dynamic on-resistance.

Hence, this subsection provides a focused literature review of dynamic on-resistance in GaN HEMTs. It examines the physical mechanisms, contributing factors, and implications of $d\mathrm{R}_{\mathrm{DS(ON)}}$ on power converter performance, while also identifying limitations of conventional characterization approaches.

Several distinct research domains have been studied related to dynamic on-resistance. This subsection organizes the literature into five key thematic areas: (1) physics-based investigations that explore the fundamental mechanisms and material-level origins of $d\mathrm{R}_{\mathrm{DS(ON)}}$; (2) evaluation of critical operational parameters, including electrical bias conditions and external influences such as temperature and radiation; (3) development of high-speed, accurate measurement techniques and standardized test configurations; (4) device- and circuit-level modeling and simulation approaches for analyzing dynamic behavior; and (5) proposed mitigation strategies to suppress or minimize the effects of $d\mathrm{R}_{\mathrm{DS(ON)}}$ during switching operation. The remainder of this subsection provides a detailed review of each of these research areas.

To understand the fundamental mechanisms of the dynamic on-resistance phenomenon, a review of prior literature demonstrated that it originates from the trapping or accumulation of electrons in unintended regions of the GaN device structure, such as the surface, AlGaN

barrier, passivation layer, or buffer. The presence of net-negative trapped charge depletes the nominal electron density in the two-dimensional electron gas (2DEG) channel to preserve charge neutrality. This reduction in free carriers decreases the drain current and momentarily increases $R_{DS(ON)}$ above its steady-state DC value [194]. Two primary mechanisms contribute to this behavior: (i) ionization of trap states due to buffer depletion, which results in electron injection toward the buffer under high drain bias during the off-state [138, 195]; and (ii) generation of hot electrons in the buffer during semi-on or hard-switching conditions [192, 196]. These mechanisms and their associated charge trapping regions are illustrated in Figure. 3.2.

The first mechanism, which is off-state induced trapping, is driven by the ionization of deep-level acceptors in the buffer layer when a high electric field is applied between the drain and source/gate terminals. This field promotes both surface and buffer trapping, reducing channel conductivity upon return to the on-state [197, 198], as shown in Figure. 3.2(a). Positive substrate biasing can mitigate vertical trapping in the buffer but may enhance surface trapping due to increased lateral electric field near the gate-drain region. However, in most power GaN HEMT implementations, the substrate is electrically tied to the source either internally or externally, making the combined effects of buffer and surface trapping relevant in practical converter applications.

On the other hand, the hot-electron-induced trapping mechanism, illustrated in Figure 3.2(b), occurs when charge carriers gain excess kinetic energy under high electric field stress. These energetic electrons, often generated during fast switching transients, can be injected into various regions of the device structure, including the surface dielectric near the gate and drain, the buffer layer, and the channel itself. This mechanism is primarily triggered under hard-switching conditions, where high drain voltage and high current density are simultaneously present, resulting in high electric fields and large carrier injection rates [198, 199].

Hard-switching is characterized by the overlap of voltage and current during the switching transition [200], which significantly enhances hot-electron acceleration and correlates strongly with increased charge trapping.

In addition, the accumulation of trapped charges near the gate-drain access region can form a so-called "virtual gate," which extends the depletion region into the channel. This effect can result in a positive threshold voltage shift (V_{th}), effectively reducing channel conductivity during the next switching cycle [201, 202]. The amount of trapped charge effect is strongly dependent on the electric field strength in the gate-drain region [203]. As the extended depletion reduces surface leakage current, it also alters charge trapping and detrapping transients. Even in passivated devices, the dielectric-semiconductor interface can serve as a trap site for hot electrons. In these cases, the resulting negatively charged virtual gate resembles the behavior observed in unpassivated devices.

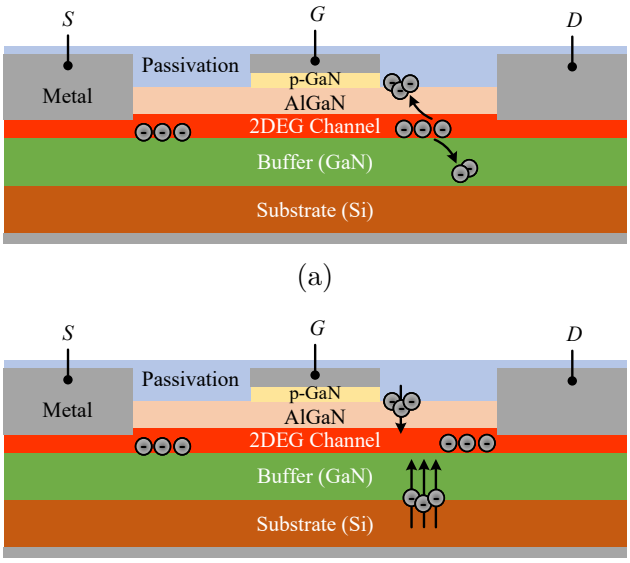


Figure 3.2: Illustration of charge trapping in a simplified GaN-on-Si cross section: (a) trapped hot electrons in the dielectric layer along the surface and/or buffer; (b) off-state traps due to ionization of charges from the surface and/or buffer.

Furthermore, the conductivity of the buffer and the carbon compensation ratio in the GaN epitaxial layer play significant roles in current collapse behavior. Hole transport within the carbon-doped GaN (GaN:C) buffer has been identified as a key leakage mechanism associated with bulk trapping [204, 205]. These vertical leakage paths are imporant for understanding the dynamic behavior and current collapse in GaN HEMTs [206]. Lastly, buffer layer composition can also affect $d\mathrm{R}_{\mathrm{DS(ON)}}$. Buffers with high breakdown strength or intentional acceptor doping (e.g., carbon or iron) may exhibit greater dispersion due to increased trap density, while undoped or semi-insulating buffers with lower breakdown fields can exhibit reduced dynamic resistance degradation [207].

The second review area is the evaluation of operational parameters. Several key operational and environmental parameters have been shown to influence charge trapping in GaN devices, contributing to dynamic on-resistance ($d\mathrm{R}_{\mathrm{DS(ON)}}$) with varying severity. Prior studies using both simulation and experimental methods have validated that these parameters significantly impact the extent of charge trapping and resulting degradation in device performance.

In the electrical domain, critical operational parameters include – blocking voltage (V_d), drain current (I_d), switching frequency (f_s) or switching period (T_s), duty cycle (D), gate voltage (V_g), voltage and current slew rates (dV_d/dt and dI_d/dt), and switching conditions (i.e., hard- vs. soft-switching). Environmental influences, such as junction temperature (T_j) and radiation exposure, also play a role in amplfying the trapping behavior.

The magnitude of the drain bias or blocking voltage, V_d, and the blocking time during off-state, T_{OFF}, have repeatedly shown to play a critical role in generation of trapped charges from a concentration of high electric field [192, 197, 208, 209]. According to [57, 197, 208, 209], a monotonic increase of $d\mathrm{R}_{\mathrm{DS(ON)}}$ has been shown in relation to increased blocking voltage or drain bias. The buffer leakage current is the main source of the charge trapping. With increased voltage amplitude or electric field, the leakage current and the number of trapped

charges are elevated, and these effects are more pronounced in a hard-switching condition and on devices with a normally-off p-gate structure with no additional structural variation to interfere with the trapping phenomena, such as gate injection transistors (GITs). Moreover, the charge-trapping effect is dependent on the stress time or the soak time due to the time dependence on trapping [210, 211]. $d\mathrm{R}_{\mathrm{DS(ON)}}$ increases monotonically over stress time, though it was observed that the soak time of micro-second (μs) range had much reduced impact than that of second (s) range during the blocking period.

The trapping mechanisms differ between the hard-switching and the soft-switching conditions. The charge storage in buffer traps is related to the generation of the hole injection during the hard-switching transition effects, while this mechanism doesn't apply to a soft-switching event. Indeed, [57, 199, 200, 208, 212, 213] have all investigated the effects of the hard-switching and the soft-switching operations related to $d\mathrm{R}_{\mathrm{DS(ON)}}$. The experimental results from the references have shown a consistent relationship with the hard-switching case inducing stronger trapping effects from the hot electron generation as opposed to the significantly reduced impact from the soft-switching conditions. Meneghini *et al.* [198] noted a 24% increase of $\mathrm{R}_{\mathrm{DS(ON)}}$ when normalized to DC state on-resistance during the hard-switching compared to the soft-switching. Li *et al.* [57] shows a monotonic increase of $d\mathrm{R}_{\mathrm{DS(ON)}}$ over the magnitude of the voltage stress on the drain, V_d for both the hard-switching and the soft-switching cases as well as for both the double-pulse-based and multiple-pulses set-ups.

Higher magnitude of drain current, I_d, and increased slew rate, dI_d/dt, can affect trapping efficacy. While the magnitude of degradation in trapping is dependent on details of the device structure which affect electron distribution and trap properties (density, energy levels and cross sections), increased drain current and hence, increased electron density is universally understood to increase trapping rates. This is particularly true in the hard-switching case where the voltage and current transitions overlap. The studies conducted in [212, 213]

investigated the effects of the switching conditions and the current direction, including the reversed current condition based on a full- or H-bridge configuration. The soft-switching forward current shows a slightly higher increase of $d\mathrm{R}_{\mathrm{DS(ON)}}$ in contrast to the reverse current direction. Geng *et al.* [214] have studied the impact of load current for both hard- and soft-switching. $d\mathrm{R}_{\mathrm{DS(ON)}}$ increases with the load current in both the switching schemes; the effect is more noticeable for the hard-switching condition. Greater impact of hard-switching with varying load current as seen in [215] is largely due to hot-electron injection resulting from overlap of high voltage and high current during switching transitions. On the other hand, soft-switching operation with increased load current can cause self-heating rather than trapping effects, which could be the dominant cause for the observed changes with $d\mathrm{R}_{\mathrm{DS(ON)}}$.

Switching frequency can impact the time constants of trapping and de-trapping mechanisms. The impact of high switching frequency on trapping has been shown experimentally in [216] that $d\mathrm{R}_{\mathrm{DS(ON)}}$ increases monotonically over a switching frequency up to of 2 MHz. After a certain frequency, a substantial reduction in rate of change in $d\mathrm{R}_{\mathrm{DS(ON)}}$ compared to the DC state at higher multi-MHz frequencies is observed. This asymptotic behavior can be explained by the trapping and de-trapping time constants, which can be much slower than a MHz range of switching frequency. The time constant of µs is observed in [216], whereas milli-second (ms) range is proposed in [198].

Temperature plays a role in $d\mathrm{R}_{\mathrm{DS(ON)}}$; yet, there is conflicting information in literature as described in [208]. First of all, a monotonic increase in $d\mathrm{R}_{\mathrm{DS(ON)}}$ with increased blocking voltage at an elevated temperature has been documented in [202, 217, 218]. Yet, weaker $d\mathrm{R}_{\mathrm{DS(ON)}}$ effects on increased temperature can be observed in [190] due to the effects of the average energy of hot electrons decreasing from the increased scattering with the lattice. The temperature effect can be also largely reduced in a soft-switching condition as the zero-voltage-switching (ZVS) transitions do not exhibit any generation of hot electrons and

dominated by the off-state trapping, resulting in lower magnitude of the trapping effects with soft switching compared to hard switching at the same electrical and thermal stress conditions. Moreover, [208, 216] both show an increase of $d\mathrm{R}_{\mathrm{DS(ON)}}$ with increased frequency (up to hundreds of kHz) was observed, but does not monotonically increase at higher frequencies (multi-MHz). With increased switching frequency, both the on- and off-time are reduced, influencing the trapping and detrapping response or time constants. Depending on the test setup, operation conditions, normalization factor, and device under test, the experimental results and temperature effects could be different and inconsistent between papers, which highlights the importance of methodical temperature-controlled experiments and consistent measurements during steady-state operation.

To provide a brief summary of the operational and environmental parameter effects on $d\mathrm{R}_{\mathrm{DS(ON)}}$ quantitatively, Figure. 3.3 shows a selected number of the discussed parameters organized by the known stressor and its impact on $d\mathrm{R}_{\mathrm{DS(ON)}}$ compared to the static $\mathrm{R}_{\mathrm{DS(ON)}}$ in each subplot. The drain current relationship of normally-on GaN HMET to $d\mathrm{R}_{\mathrm{DS(ON)}}$ was extracted from [219]. The data indicate a monotonic increase over higher current, but at a faster rate for elevated temperature of 150°C at different measurement times (500ns and 2.5μs). The drain voltage relationship extracted in [57] also provides a monotonic behavior under hard switching condition with increasing voltage stress with more pronounced increase for the 1 MHz as opposed to the 250 kHz and 500 kHz case. The temperature relationship from [208] is also provided; $d\mathrm{R}_{\mathrm{DS(ON)}}$ increases monotonically with higher voltage bias under hard-switching condition up to nearly 50°C. However, a non-monotonic relationship of decreasing $d\mathrm{R}_{\mathrm{DS(ON)}}$ is shown at higher temperatures due to reduced hot-electron trapping. Repetitive switching cycles to $d\mathrm{R}_{\mathrm{DS(ON)}}$ degradation has been studied and a part of the results was extracted from [220]. High drain bias stress directly induce current collapse during off-state process and contributes to $d\mathrm{R}_{\mathrm{DS(ON)}}$ degradation during repetitive hard-switching

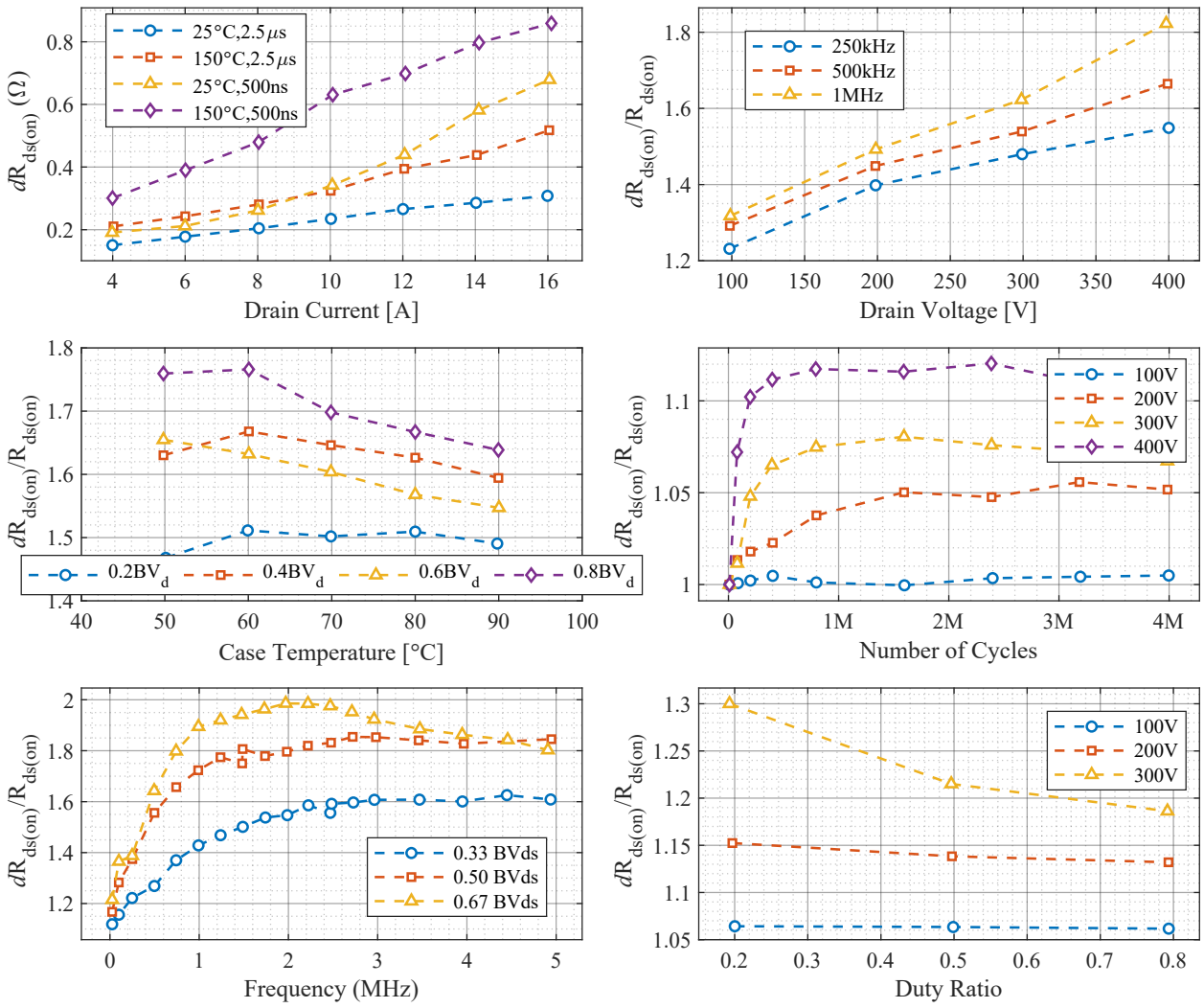


Figure 3.3: Various operational parameters reported in literature that affect dynamic ON-resistance in power GaN HEMTs. Individual plots were regenerated from prior studies, and careful interpretation is required based on the tested GaN device technology, experimental setup, test conditions, and measurement method. Data on drain current, voltage, case temperature, number of cycles, frequency, and duty ratio were extracted from [219], [57], [208], [220], [221], and [222], respectively.

procedure. The multi-MHz frequency relationship from [221] shows $d\mathrm{R}_{\mathrm{DS(ON)}}$ a monotonic increase up to 2 MHz and stay flat at higher mult-MHz frequencies due to shortened trapping and detrapping times. Lastly, the duty ratio bias data from [222] describes decreasing $d\mathrm{R}_{\mathrm{DS(ON)}}$ over increased duty ratio because of the shortened trapping time period with longer on time, leading to more detrapping to take place.

The third research topic is the development of dynamic on-resistance measurement techniques. To enable high resolution on-resistance data collection during the conduction state, a clipping circuit is often deployed with a combination of passive and active elements, which offsets the high voltage range to a much lower or acceptable voltage range, while preventing measurement errors and signal distortions caused by clipping from the instrument. A variety of clipping techniques have been observed in literature. Yang *et al.* [223] and Lei *et al.* [224] provide a comprehensive comparison analysis and review of several clipping circuits found in prior art, describing the operation, performance, and limitations to the existing measurement circuits. Guacci *et al.* [225] shows another novel approach to the clamping circuit along with the design and calibration process to enable high accuracy ($\pm 2\%$), bandwidth (> 50 MHz), and dynamic responses (< 50 ns) while providing a 50 Ω termination, which eliminates the need for any additional probing accessory when interfacing the acquisition system.

Along with high accuracy sensing techniques, the experimental setup of $d\mathrm{R}_{\mathrm{DS(ON)}}$ characterization can be categorized into wafer-level and board-level tests. The pulsed I–V measurements can be performed at an on-wafer level to analyze the trapping mechanism with a certain epi-structure and process optimization-variation [192]. In [226], various surface and border traps across a broad timescale were tested on wafer-level pulsed I–V tests. Moens *et al.* [209] have presented a strong positive correlation between the ionization of buffer traps by injection of electrons from the Si substrate and $d\mathrm{R}_{\mathrm{DS(ON)}}$. The paper also explores different Carbon (C) doping profiles in the epi layers to reduce the substrate buffer leakage,

which were experimented on wafer-level tests. Rossetto *et al.* [190] have studied the role of hot-electron effects under soft-switching and hard-switching conditions also on a wafer-level measurement setup.

Li et al. [57] shows that a wafer-level measurement system to perform I-V characterization can be developed in such a way that eliminates any potential external factors and defects introduced from the packaging process. For continuous operation, Barbato *et al.* [193] developed a novel boost converter system to investigate on-wafer level dynamic properties of GaN in hard-switching application conditions. However, these on-wafer level set-ups and measurements can be costly and do not exemplify in-application uses with the second order effects from the board and interface parasitics. In addition, the semiconductor devices used for power converters are packaged in various form factors to enhance the usability and safety of the transistors.

On the other hand, a board-level evaluation can be performed with pulsed based testing, such as double-pulse tester (DPT) or continuous testing like using the boost converter configuration [197, 208, 227]. In fact, there are many circuit topologies that can be used to characterize $d\mathrm{R}_{\mathrm{DS(ON)}}$ under various switching conditions and operational parameters, including off-state time, off-state voltage, temperature, switching frequency, duty cycle, on-state current, and on-state gate voltage, number of pulses or continuous operation.

The standardization of experimental setup and data collection to evaluate $d\mathrm{R}_{\mathrm{DS(ON)}}$ has been discussed in [227, 228]. Foulkes *et al.* developed a process to enable an extensive characterization of $d\mathrm{R}_{\mathrm{DS(ON)}}$ via a factorial measurement scheme involving various test parameters, including drain current, voltage stress magnitude, voltage stress time, and junction temperature, all of which were controlled independently [227].

The fourth area is the modeling and simulation approaches for analyzing dynamic behavior.

For example, Koudymov *et al.* [229, 230] provides a compact analytical model of current collapse in GaN HEMTs. The model accounted for velocity saturation effects and trapped regions of the device while using a minimal number of fitting parameters, requiring physical parameters to describe velocity-field dependence of the carriers. Morevoer, a virtual gate-drain current model is developed for AlGaN/GaN HEMT with dependency of trap on field plate [231]. The model is based on the shallow surface traps from the lateral electric field distribution. Gauss Law's is used to establish the relativity between the trap charges and electric field. This model shows influence of field plate length on current collapse, virtual gate, and sheet carrier density. Wang *et al.* [232] presented large signal equivalent circuit modeling of electrothermal effects on AlGaN/GaN HEMTs. Current collapse due to self-heating and ambient temperature effects was analyzed and modelled with a temperature-dependent thermal resistance and thermal capacitance sub-circuits. Numerical finite-element method was used to extract appropriate thermal parameters of the device representation.

Another popular modeling approach shown in literature is a simple curve fitting with non-linear regression to the experimental dataset. For instance, in [233], an exponential expression was used to produce a trend line of the data points of $d\mathrm{R}_{\mathrm{DS(ON)}}$. Both the fast and slow detrapping time constants were modeled based on the effects driven by switching frequency and blocking voltage. Li *et al.* [234, 235, 236] provided a compact model with a behavioral voltage source at the drain or gate terminal to incorporate the trapping effects via RC networks. In [234], the GaN transistor's dynamic resistance is modeled through a gate voltage modulation. This was accomplished by adding a voltage compensation, V_{comp}, in the device gate terminal. V_{comp} is made up of several RC units to display the transients and dynamics of on-resistance by extracting different trapping and de-trapping time constants from a fitting function to the measured dataset. In [235, 236], the authors have improved the model by providing a voltage compensation at the drain terminal. A behavioral voltage source, V_{comp}

represents the voltage drop on the increased dynamic resistance during the conduction state and is realized by RC cells.

To better design and understand the physical behaviors of GaN devices in particular applications, a physics-based model is often required along with the accurate device design parameters such as: geometry, spacing between electrodes, and geometry of field plates to construct a reliable simulation platform. The authors in [237] showed an iterative design process to validate the model implementation to practical power converter operations. Such a physical compact model development process of GaN HEMTs can be used to investigate charge trapping effects, which can be specifically further characterized based on the location of the traps, such as surface states, barrier traps, interface traps, and buffer/substrate traps. Syamal *et al.* [238] provided a comprehensive and scalable trap-charge model for the GaN HEMT DC and pulsed I–V characteristics. The model captures the effects of gate and drain quiescent biases as well as the stress duration in the off-state.

Last but not least, the fifth topic is the investigation of mitigation strategies to combat dynamic on-resistance. In order to attenuate its effects, largely induced by the charge storage via surface and bulk traps, there have been various approaches and novel solutions to minimize or mitigate different charge trapping mechanisms. For its close dependency on the structural variability, such as defects, compositions, and architecture, $d\mathrm{R}_{\mathrm{DS(ON)}}$ can be controlled and alleviated by implementing counteracting measures to inhibit potential trapping state formation.

Utilization of multiple field plates over insulators was found to be effective in increasing the device breakdown voltage with no dispersion [239]. Indeed, with the mitigation of electrical field crowding, the surface traps can be largely be prevented with incorporation of multiple electric field plates and an optimized configuration of field plates along with epitaxial layer quality could improve the $d\mathrm{R}_{\mathrm{DS(ON)}}$ characteristics. For instance, Chu *et al.* [240] incorpo-

rated multiple field plates – one plate connected to the gate electrode and two field plates connected to the source electrode. Such a configuration of field plates not only enabled a high breakdown voltage rating, but also resulted in lower dynamic on-resistance at high-voltage operation.

As discussed in [204, 206], providing a leakage path for a source of holes over the gate to drain gap and by ensuring the resistivity increases from top to bottom in the epitaxial layer structure can help suppress accumulation of bulk negative charges. This can be achieved by controlling the leakage and resistivity of the unintentionally doped (UID) GaN layer by modulating conductivity and a combination of epitaxial growth and processing conditions. The substrate deep depletion can be generated by making the entire epitaxy sufficiently leaky to ensure suppression of inversion charges [206].

A normally-off GaN HEMT using conductivity modulation, known as a gate injection transistor (GIT) utilizes hole-injection from the p-AlGaN to the AlGaN/GaN hetero-junction. The accumulated electrons are drain biased with high mobility, while the injected holes keep charge neutrality at the channel around the gate due to lower hole mobility magnitude. This conductivity modulation maintains the drain current with increased the electron density in the channel and consequently prevents current collapse [241].

To concisely summarize the aforementioned research topics surrounding $d\mathrm{R}_{\mathrm{DS(ON)}}$, Table 3.2 provides a succinct description and relevant literature references for each topic.

Table 3.2: Summary of five research themes related to $d\mathrm{R}_{\mathrm{DS(ON)}}$, providing descriptions and relevant literature.

Theme	**Description**	**References**
Physical Origins	Explanation of the physical origins of $d\mathrm{R}_{\mathrm{DS(ON)}}$ and theoretical understanding of various trapping states and their effects. Highlights fundamental mechanisms and how they impact device operation.	[185, 186, 187, 189, 192, 194, 195, 196, 197, 198, 200, 203, 226]
Operational / Environmental Parameters	Describes device- and circuit-level factors such as voltage, current, frequency, duty cycle, temperature, and radiation, and how they affect trapping mechanisms and the resulting dynamic resistance behavior.	[57, 138, 192, 197, 199, 200, 208, 209, 212, 213, 215]
Measurement, Topologies, and Standards	Covers advancements in measurement techniques and standardized methods to evaluate $d\mathrm{R}_{\mathrm{DS(ON)}}$, including circuit-level and on-wafer tests and topology-specific testbeds.	[57, 188, 189, 190, 192, 193, 197, 208, 223, 224, 225, 226, 227]
Simulation and Modeling Techniques	Discusses simulation approaches including TCAD, SPICE, and analytical/behavioral modeling to predict dynamic ON-resistance and replicate trapping behavior under various operating conditions.	[229, 230, 233, 234, 235, 236, 237, 238]
Mitigation Strategies	Highlights design and control strategies to reduce or eliminate the impact of trapping, including structural modifications, buffer layers, and circuit-level compensation techniques.	[204, 206, 233, 234, 235, 239, 240, 241]

3.2 Slew Rate Effects of Dynamic Stresses on Device Physics and Operation

A significant challenge in GaN device research is the inadequate representation dynamic stresses, induced by fast-switching operating conditions. Conventional approaches do not account for high-frequency, high-slew-rate transients that alter internal electric field distributions and exacerbate charge trapping. These effects are not captured under static or quasi-static analysis conditions.

To address these limitations, this section introduces a dynamic framework for evaluating the impact of switching slew rates on device-level physical behavior. Emphasis is placed on understanding how different switching slew rates influence internal field profiles, leakage paths, and reliability-critical mechanisms, as described in Subsections 3.2.1. Subsection 3.2.2 focuses on the evaluation of transient behavior impact on charge trapping and dynamic on-resistance in cascode GaN configurations.

3.2.1 Effects on GaN HEMT Distributed Field Plate Structures

It is necessary to account for dynamic stress conditions encountered in power conversion environments when evaluating the performance and reliability of GaN devices. Unlike static or DC analyses, dynamic evaluation captures the time-varying electric field and current density distributions that more accurately reflect real converter operating scenarios. These field distributions play an important role in determining the fundamental reliability of a given device technology. However, conventional approaches largely focused on mitigating well-understood static stress mechanisms, without fully addressing the implications of high-frequency, dynamic switching stressors [239, 242, 243, 244].

In this subsection, dynamic operating conditions in AlGaN/GaN HEMTs are analyzed under varying switching slew rates (i.e., dv/dt) at high-voltage operation. The focus is not only on the severity of dynamic stress but also on its interaction with device architectures designed for high breakdown voltage. Technology computer aided design (TCAD) simulations are conducted on GaN HEMT field plate structures that incorporate features suitable for high-power scaling.

As a representative case, distributed field plate architectures are investigated to highlight the importance of accounting for dynamic stress in GaN HEMT performance. Field distribution and internal leakage paths are examined to evaluate trapping mechanisms, particularly buffer leakage current, which is can be a key contributor to charge trapping phenomena [206]. Since dynamic on-resistance is closely tied to channel electron acceleration under localized electric field intensification [245], field plate architectural studies become essential to investigate.

The proposed resistive field structures described in Figure. 3.4 greatly improve electric field uniformity with reduced peak electric field intensity across the device structure. This has been achieved by inserting highly resistive elements, denoted as R between the source and drain. There are taps placed at regular intervals to specify a gradually varying voltage boundary condition at the top surface of the passivation layer throughout the access region. To realize such a structure, this could be accomplished by selectively etching the epitaxial GaN away in a region along the edge of the die to expose the high resistivity silicon and fabricate a resistor of very high value using implant doping. The resistor contacts may be routed to the individual device fingers using vias and a two metal level scheme. This multi-contact voltage-distributed field control scheme is hereinafter referred as the field cage.

Figure. 3.5 illustrates the electric field profiles of the novel structure with different variations and the conventional 3-field plate approach. The novel resistive field structures have been varied with five field cage taps and varying tap distances, d_{tap}, between the edges of each tap

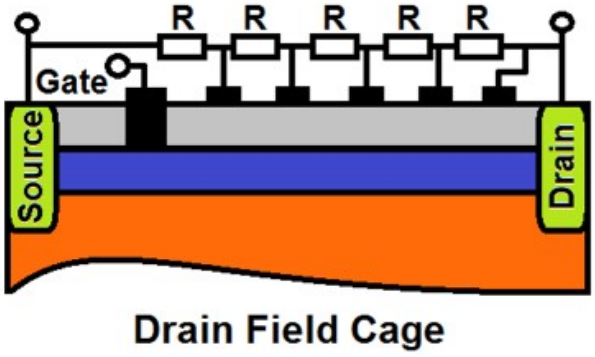


Figure 3.4: Schematic showing the drain field cage structure using resistive voltage divider network. There are taps that connect the resistive voltage divider elements to the passivation surface.

of 50, 100, and 400 nm. A large value of resistance is necessary, such as 1 GΩ to connect the consecutive taps since a small resistance would result in excessively large power dissipation from increased leakage current through the field cage resistors due to the large OFF-state blocking voltage. The simulation model of the drain field cage (DFC) was constructed with the tap pitch of 1 μm, which is the distance between the centers of two consecutive taps. By making the taps thinner, the distance between the edges of 2 taps (d_{tap}) is increased. Thus, a smaller d_{tap} corresponds to a thicker tap. The first tap is kept at a constant distance (1 μm) from the gate edge for all cases. As d_{tap} is increased from 50 nm to 400 nm, the electric field peak associated with taps T1 through T5 are greatly reduced and a very uniform electric field distribution is achieved. Although the peak associated with the gate remains invariant because of the fixed distance between the edge of the gate and T1, this field peak does not increase in magnitude with increasing V_{ds} beyond ∼50 V.

In addition, Figure. 3.5 represents a DC analysis with no variations in electric fields over time. This suggests that drain field cage with thinner or larger d_{tap} is more effective in distributing the electric field with less peak field intensity than the thicker or smaller d_{tap} structure. Therefore, larger d_{tap}, such as d_{tap} = 400 nm should be the design strategy for achieving better field control, larger breakdown voltage, and higher reliability for HEMTs.

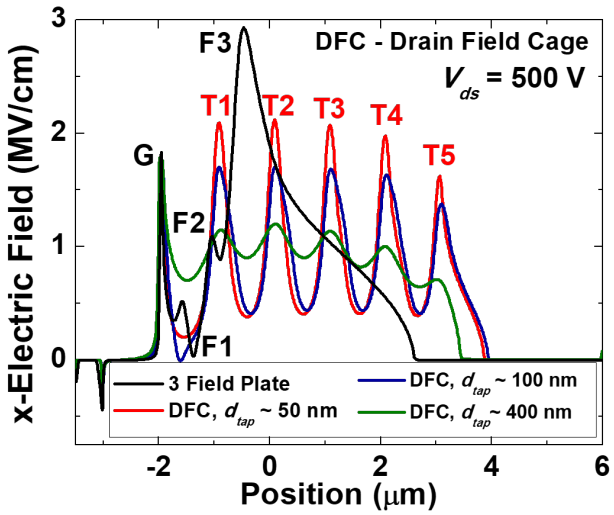


Figure 3.5: Electric field profiles from source to drain of $V_{ds} = 500V$ (DC) for a structure with three differently-spaced drain field cages (DFC) with the distance between the edges of the consecutive taps (d_{tap}) = 50, 100, and 400 nm as well as a structure with three field plates spaced horizontally by 250 nm, which is the same as black curve in Figure. **??**(c) and included as a baseline comparison. The tap pitch distance between the center of the field taps is 1 μm and the passivation thickness, h_{pass} is 100 nm for all of the structures above. The resistance between the consecutive taps, R for all DFC cases is equal to 1 GΩ.

However, it is crucial to consider the dynamic modes of operation, such as fast switching speed (i.e. high dv/dt) because it's an aspect that is of great importance for power switching device performance, including efficiency and electromagnetic interference (EMI) or cross-talk and the conventional analysis of pure DC characterization can severely limit the device performance without carefully studying the intended or wide dynamic operation regime.

To further highlight the importance of the dynmaic effects from an AC analysis, Figure. 3.6 shows the comparison between the electric field control for devices with d_{tap}=100 nm (thicker tap) and d_{tap}=400 nm (thinner tap). The drain voltage is ramped up from 0 to 500 V over a period of 5 ns, resulting in dV/dt = 100 V/ns. Figure. 3.6(a) denotes appropriate variables for the resistors, taps, and voltage terminals within the device structure. As a measure of uniformity of the electric field distribution, the voltage difference between the consecutive field cage taps as a fraction of the total V_{ds} (i.e., $(V_n - V_{n+1})/V_{ds}$) is plotted in Figure. 3.6(b)

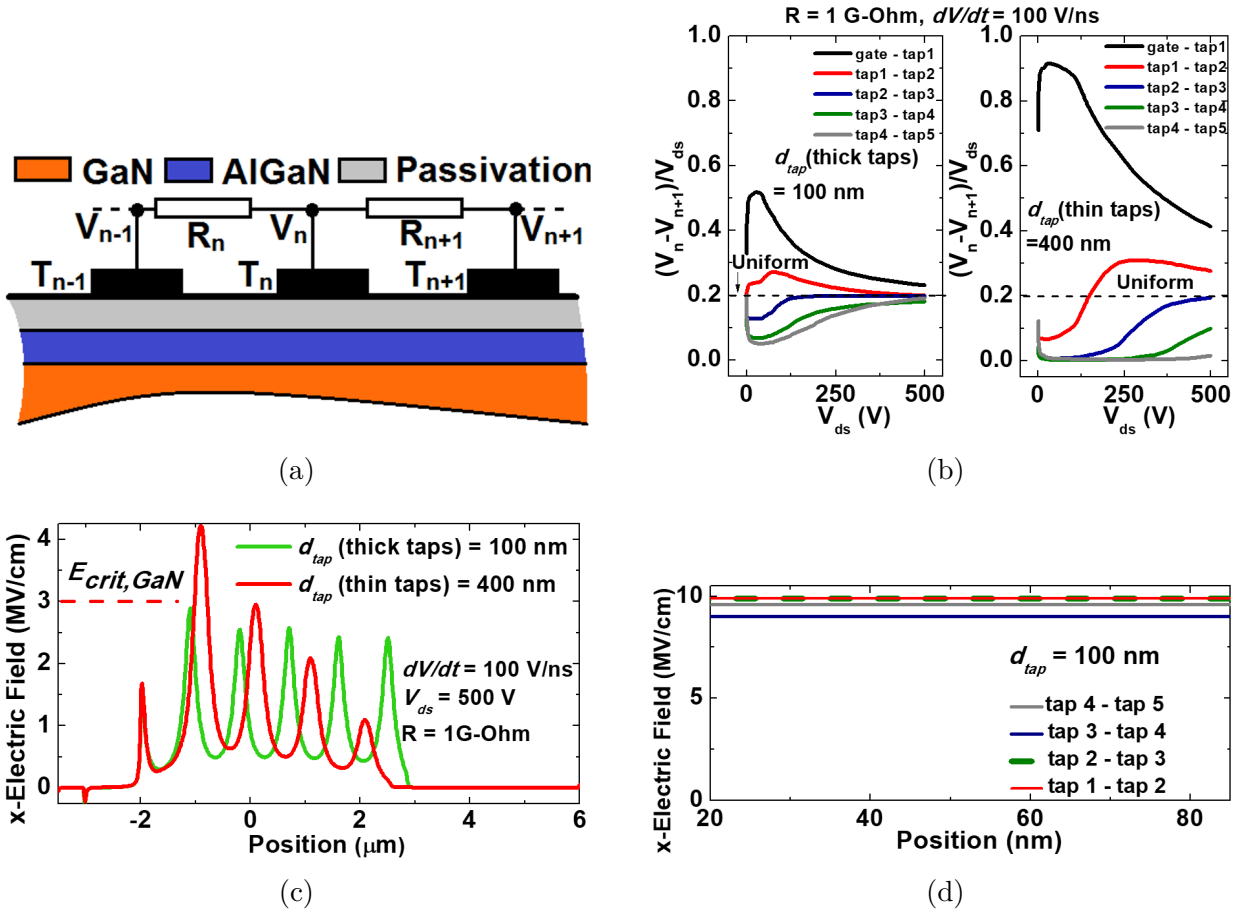


Figure 3.6: (a) Schematic of drain field cage with three field cage taps, T_{n-1}, T_n, and T_{n+1} with voltage terminals measured at V_{n-1}, V_n, and V_{n+1}. All $R_n = R = 1$ GΩ. (b) Voltage difference between consecutive taps with respect to $V_{\rm ds}$ as a measure of electric field uniformity for both thick and thin taps. (c) Electric field profile from source to drain for $V_{\rm ds} = 500$ V ($dV/dt = 100$ V/ns) for structures with tap pitch of 1 μm and $d_{\rm tap}$ of 100 and 400 nm. (d) Horizontal electric field at the surface of the dielectric passivation between consecutive taps for the $d_{\rm tap} = 100$ nm case. Passivation thickness $h_{\rm pass} = 100$ nm for all structures.

for both the thick, d_{tap}=100 nm and thin taps, d_{tap}=400 nm. Both tap thicknesses show that the tap voltage distribution is initially non-uniform, but becomes more uniform as the voltage ramp proceeds, approaching the dashed black line at $(V_n - V_{n+1})/V_{ds} = 0.2$ for a 5 tap structure, corresponding to the exact same voltage difference between all consecutive taps. The improvement in the tap voltage and hence the electric field uniformity at high voltage makes the field cage scheme a promising one for achieving breakdown voltage scalability.

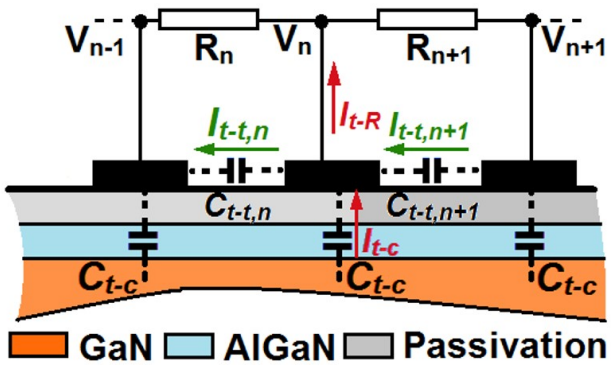


Figure 3.7: Schematic drawing of three consecutive field cage taps with voltages V_{n-1}, V_n, and V_{n+1}, as well as the parasitic capacitances $C_{\text{t-t},n}$, $C_{\text{t-t},n+1}$, and $C_{\text{t-c}}$ associated with the taps. Conduction and displacement current components are also illustrated.

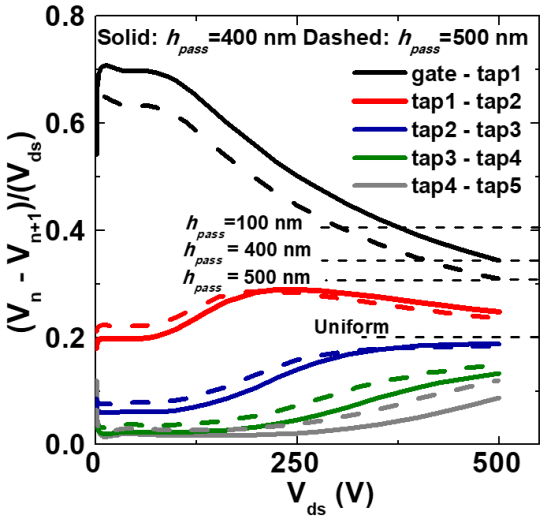
However, contrary to the DC behavior, the thin taps at high dV/dt show a much higher peak voltage at the tap nearest to the gate; the peak intensity well exceeds the published $E_{crit,GaN}$ as noted in Figure. 3.6(c). On the other hand, the thick tap solution with d_{tap} of 100 nm shows better field distribution with no peak field intensity exceeding that of GaN. This result suggests that having thicker taps is the better option since it keeps the field below the critical value for both DC as seen in Figure. 3.5 and AC or high dV/dt shown in Figure. 3.6(c).

In spite of the benefits provided by the thick taps in regards to reduced peak electric field below $E_{crit,GaN}$ when compared to the thin taps, care must be taken as the electric field is still fairly spiked close to $E_{crit,GaN}$ at the taps. More importantly, the thick taps lead to extremely high electric field in the device passivation that puts the passivation at the risk of dielectric breakdown. Figure. 3.6(d) plots the electric field at the surface of the passivation between the consecutive taps for the d_{tap}=100 nm case. Clearly, the electric field of ~10 MV/cm can cause severe concerns for the reliability of the dielectric as it could lead to a complete dielectric breakdown. Therefore, for the field cage to work effectively at high dV/dt, it is necessary to improve the field distribution while using thin taps to maintain large enough d_{tap}.

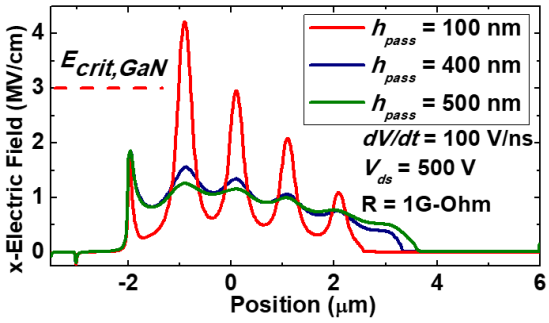
The results shown in Figure. 3.6 provide major contributions in understanding the operation of the field cage and optimizing the structure for high-frequency operation. In DC operation, both thin and thick tap devices show superior voltage distribution along the taps across the entire range of voltages from 0 to 500 V. This indicates that a uniform electric field distribution is favored using thinner taps in the absence of displacement currents, which appear only for non-zero dV/dt. Yet, the introduction of displacement currents in the structure makes the tap voltage distribution highly unequal as observed in Figure. 3.6(b). Nevertheless, the non-uniform tap voltage distribution for the thin tap ($d_{tap} = 400$ nm) device can be understood by analyzing the parasitic capacitances within the device structure.

Figure. 3.7 shows the displacement current components of the drain field cage with three taps. The taps are equally spaced from one another and the cage resistances are equal, which makes the displacement currents of $I_{t-t,n}$ and $I_{t-t,n+1}$ roughly equal if there is no significant contribution from I_{t-c}. However, if the tap-to-channel capacitance, C_{t-c} is large enough, the I_{t-c} contribution can be significant compared to $I_{t-t,n}$. The current I_{t-c} distributes itself between the parallel impedances of tap-to-tap capacitance, $C_{t-t,n}$ and the resistance, R_n. At high frequency and high cage resistance, the impedance of $C_{t-t,n}$ decreases to a much lower value than R_n, which results in most of the current I_{t-c} flowing through $C_{t-t,n}$ and hence, making $I_{t-t,n}$ and $I_{t-t,n+1}$ unequal.

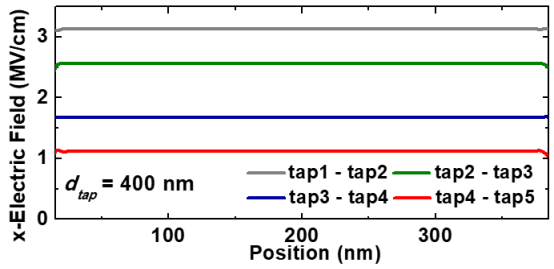
Consequently, $V_n - V_{n-1}$ and $V_{n+1} - V_n$ become unequal and the field cage cannot maintain a uniform electric field distribution. I_{t-c} can be reduced with smaller C_{t-c} and one way this can be achieved is by increasing the passivation thickness. Figure. 3.8 shows the results for the electric field distribution and the voltage difference between the consecutive taps as a ratio of the total V_{ds} with increased passivation thicknesses of 400 and 500 nm. The corresponding results were compared to the 100 nm case described in Figure. 3.6(c) with d_{tap}=400 nm. Figure. 3.8(a) shows the measure of uniformity, $(V_{gate} - V_{tap1})/V_{ds}$ at V_{ds} of 500 V at the



(a)



(b)



(c)

Figure 3.8: (a) Voltage difference between consecutive taps with respect to $V_{\mathrm{ds}} = 500$ V for $h_{\mathrm{pass}} = 400$ nm (solid line) and $h_{\mathrm{pass}} = 500$ nm (dashed line); (b) electric field profile from source to drain for $V_{\mathrm{ds}} = 500$ V or $dV/dt = 100$ V/ns for a drain field cage with tap pitch of 1 μm and $d_{\mathrm{tap}} = 400$ nm. The red curve shows a comparison device with $h_{\mathrm{pass}} = 100$ nm; (c) horizontal electric field at the surface of the passivation layer between consecutive taps for $d_{\mathrm{tap}} = 400$ nm.

end of the 5 ns ramp with the smaller dashed lines representing the different passivation thicknesses (100, 400 and 500 nm). As Figure. 3.8(a) shows, even for a passivation thickness of 500 nm, the voltage difference between the gate and tap1 or T1 is ∼0.3 V_{ds} (the voltage difference should be 0.2 V_{ds} in the ideal case for a 5 tap structure (corresponding to the exact same voltage difference between all consecutive taps) as shown by the dashed line marked "uniform" on Figure. 3.8(a). Thus, there is headroom for even more improvement in the electric field uniformity by further increasing the passivation thickness, and as shown in Figure. 3.8(b) increasing the passivation thickness drastically improves the electric field uniformity.

It can be clearly seen that the electric field with the high passivation thickness of 400 and 500 nm is uniform across the device with much reduced peak intensity compared to the thin-passivation case of 100 nm from Figure. 3.6(d). Figure. 3.8(c) plots the electric field at the surface of the passivation layer between the consecutive taps for the device with d_{tap}=400 nm and the passivation thickness, h_{pass} of 400 nm. These plots suggest not only excellent uniformity of electric field in the GaN channel for both DC in Figure. 3.5 and dV/dt=100 V/ns in Figure. 3.8(b), but also low electric field in the passivation dielectric achieved by implementing a field cage with R=1 GΩ and optimizing the tap-to-channel capacitance, C_{t-c} through adjusting the passivation thickness, h_{pass} and the tap-to-tap capacitance, C_{t-t} through adjusting the tap thickness, d_{tap}.

An optimized drain field cage design is shown in Figure. 3.9 with d_{tap} of 400 nm, h_{pass} of 400 nm, R of 1 GΩ, and applied bias of 500 V. An excellent uniform electric field with reduced peak intensities across the device structure can be seen for different slew rates of 1, 10, and 100 V/ns. Electric field uniformity is well maintained for smaller and more realistic ramp rates such as 1 and 10 V/ns, which are close to the nominal operating conditions of commercial devices [246, 247]. Though 100 V/ns is relatively a high ramp rate in reverse

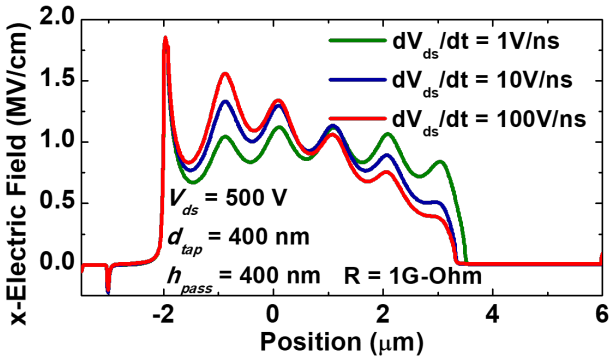


Figure 3.9: Electric field profile from source to drain for V_{ds} of 500 V for drain field cage with tap pitch of 1 μm, d_{tap} of 400 nm, and h_{pass} of 400 nm for dV/dt = 1, 10, and 100 V/ns.

recovery compared to any commercial device with V_{br} of ∼500 V, a uniform electric field profile can still be established with the optimized drain field cage structure. It is important to note that the passivation thickness required is dependent on the desirable frequency of operation or specific to power converter applications and specifications and therefore, the optimal design process should include the evaluation of the target applications' dynamic stress characteristics.

Lastly, the overall results through TCAD simulation analysis have demonstrated the critical importance of examining dynamic operating conditions similar to the practical power converter operations in an experimental scenario. Such inclusion of dynamic effects not only ensures the device design and operations for the best possible breakdown voltage and reliability, but also reduces the effects of dynamic ON-resistance due to its direct relationship of charge trapping to peak electric field and uniformity.

3.2.2 Evaluation of Switching Slew Rates in Cascode GaN

This subsection investigates the impact of switching slew rates on the performance of cascode GaN devices through experimental evaluation. To properly assess slew rate effects on charge

trapping, it is important to select an appropriate test topology, as each configuration presents trade-offs in terms of stress conditions and waveform characteristics. Specific classes of commonly used topologies to test dynamic on-resistance are summarized in Table 3.3.

Various pulse testing methodologies such as single pulse [228], double pulse [248, 249], multiple pulse [57, 250], and continuous operation [146, 251, 252] have been employed in prior literature. Each method offers unique stress characteristic for capturing dynamic on-resistance. For instance, single pulse testing involves applying a long-duration off-state stress before measuring the on-resistance of the device under test (DUT). This method is straightforward and provides a quick snapshot of the effects on on-resistance based on the high-voltage stress duration. It is simple and imposes minimal thermal stress on the device. However, it may not fully capture the hard-switching ON and OFF transient behaviors.

Double pulse test (DPT) extends the single pulse methodology by introducing a second pulse after a defined delay. This approach, typically used for characterizing switching losses of a power device, allows for the observation of the device's recovery characteristics and

Table 3.3: Summary of circuit topologies for $d\mathrm{R}_{\mathrm{DS(ON)}}$ characterization.

ID	Circuit Topology Basis	Switching Condition	References
(a)	Double Pulse Test (DPT)	Hard-Switching	[192, 202, 208, 218, 219, 253, 254, 255, 256, 257]
(b)	Inductive-Resistive (L-R) DPT	Hard-Switching	[214, 218, 258]
(c)	Clamped Inductive	Hard-Switching	[208, 222, 259, 260]
(d)	Pulsed I-V	Soft-Switching	[227, 228, 261]
(e)	Buck Converter	Soft-Switching	[208, 210, 259, 260]
(f)	Boost Converter	Hard-Switching	[210, 262]
(g)	L-C Resonant	Soft-Switching	[199, 263]
(h)	Triangular Current Mode (TCM)	Soft-Switching	[57, 225]
(i)	Trapezoidal Current Mode (TZCM)	Hard-/Soft-Switching	[212, 234, 250]

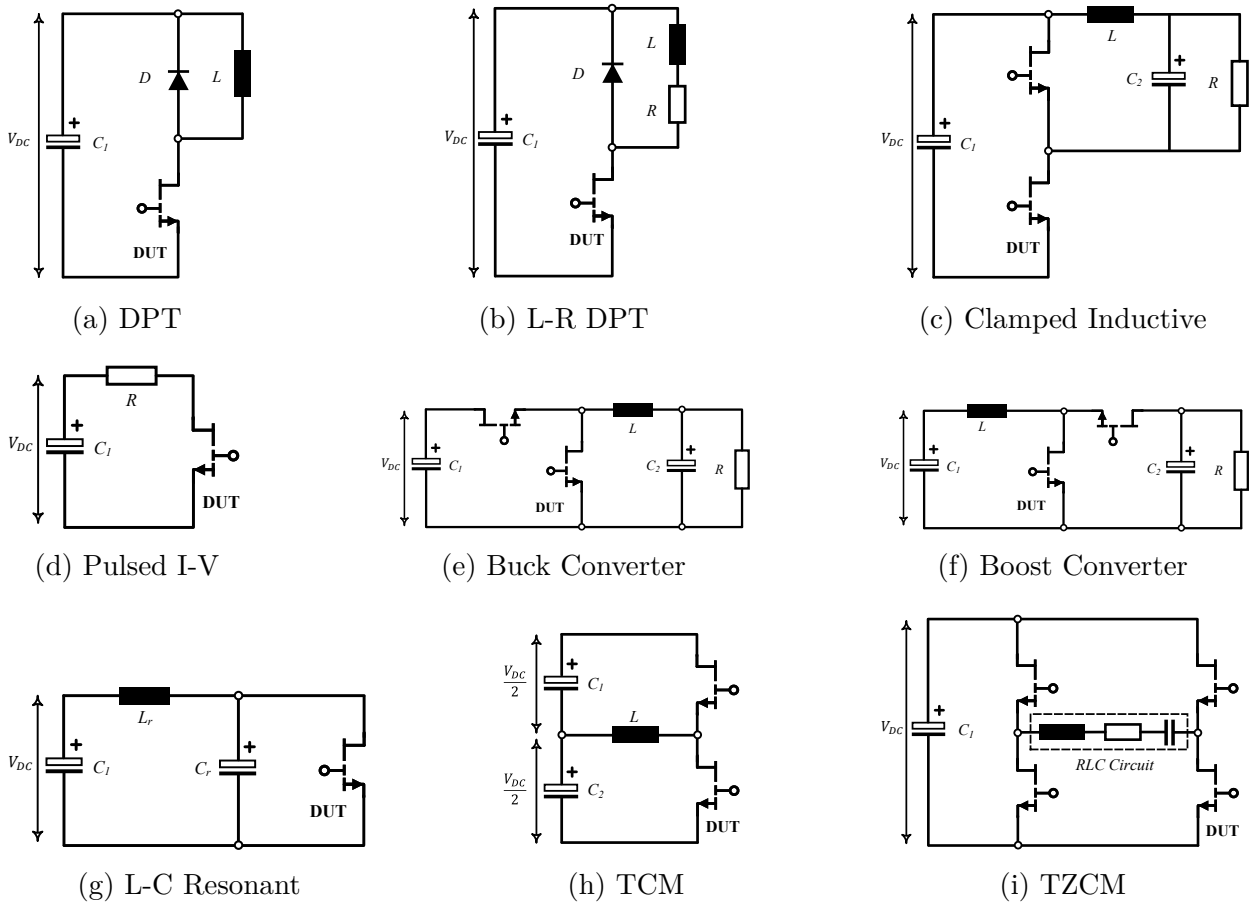
the impact of charge trapping and detrapping phenomena. The first pulse sets the initial conditions by ramping up the load current to a desired level for the device whereas the second pulse characterizes the device's response, capturing both the ON and OFF switching transient behaviors under the effects of short-term stress. However, it still may not fully represent the device's performance under continuous or repetitive stress conditions.

Multiple pulse testing (MPT) involves applying a series of pulses to the DUT, with each pulse separated by a specific interval. This method provides a more comprehensive assessment of the device's intended operating conditions where the device is subjected to repetitive switching events. Multiple pulse testing can reveal cumulative effects, including charge trapping based on the pulse width, current, and repetition numbers. By varying the pulse characteristics, this methodology provides a simple yet insightful information about the device's behavior under different stress scenarios.

Continuous operation testing subjects the GaN DUT to a repetitive operational signal over an extended period of time. This method is the most representative of the device's practical applications as it closely simulates the continuous switching and thermal cycling experienced by the device in such power applications. However, it is difficult to decouple the dynamics of the critical parameters like blocking voltage, frequency, and switching speed from the thermal management of the device.

Moreover, for the topologies that allow continuous switching operation of GaN, self-heating effect leads to thermal stress on the device, potentially raising the junction temperature. Elevated temperatures can further enhance the activation of trap states within the device and as these traps become more active, this in turn affects dynamic on-resistance.

Figure 3.10(a)–(i) presents representative schematic diagrams and the fundamental circuit structures used to evaluate dynamic on-resistance under various switching conditions. For



(a) DPT (b) L-R DPT (c) Clamped Inductive

(d) Pulsed I-V (e) Buck Converter (f) Boost Converter

(g) L-C Resonant (h) TCM (i) TZCM

Figure 3.10: Circuit topologies for $d\mathrm{R}_{\mathrm{DS(ON)}}$ characterization: (a) Double Pulse Test (DPT), (b) Inductive-Resistive (L-R) DPT, (c) Clamped Inductive, (d) Pulsed I-V, (e) Buck Converter, (f) Boost Converter, (g) L-C Resonant, (h) Triangular Current Mode (TCM), (i) Trapezoidal Current Mode (TZCM).

instance, Figure. 3.10(a) has been developed and employed in [192, 202, 218, 219, 253, 253, 254, 255]. To simulate continuous operation of GaN devices, the JEDEC Standard - JEP173: "Dynamic on-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices" [264] provides unofficial guidelines to test GaN devices under hard- and soft-switching. The hard-switching can be simulated with the inductive-resistive (L-R) load DPT architecture [214, 218, 258] illustrated in Figure. 3.10(b), whereas the soft-switching test case can be replicated using the pulsed current and voltage (I-V) method in Figure. 3.10(d) [256, 258, 261, 265].

Other topologies include the clamped inductive, buck, boost, L-C resonant, half-bridge based triangular current mode (TCM), and full-bridge based trapezoidal current mode (TZCM) configurations – shown in Figure. 3.10(c), Figure. 3.10(e), Figure. 3.10(f), Figure. 3.10(g), Figure. 3.10(h), Figure. 3.10(i), respectively – that are suited to evaluate $d\mathrm{R}_{\mathrm{DS(ON)}}$ in various modes of switching operation. For instance, TCM waveforms can be reproduced to replicate soft-switching cases [57]. Resonance based topologies can be developed to simulate current waveforms under resonant converter operations [199, 250, 263]. Full bridge based topology in Figure. 3.10(i) can be used to reproduce trapezoidal current waveforms by varying the delay time to test both the forward and reverse condition along with the hard- and soft-switching operation [213].

Despite the range of test topologies explored, the MPT demonstrated a favorable balance between controllability and reduced self-heating. In particular, the MPT architecture provides a flexible solution to explore the effects of slow switching from external control parameter, such as the gate resistance, which primarily influences the switching transients rather than thermal effects in pulsed operation. The absence of significant self-heating reduces the impact of temperature-induced trapping. Therefore, MPT was selected to closely replicate the operating conditions of commercial 650 V cascode GaN HEMTs to enable accurate evaluation of slew rate impact on dynamic on-resistance.

Figure. 3.11 illustrates the MPT schematic that was used to apply various pulse conditions and external resistances to understand how such parameters influence the GaN HEMT's trapping. The on-state Voltage Measurement Circuit (OVMC) is used to measure the on-resistance of the DUT during each conduction state. Note that five consecutive pulses were determined to be a suitable test case based on the impact of varying pulse numbers on hard-switching conditions, as referenced in [57]. To control switching slew rates in experiments, different gate resistance values can be used to shape the switching transition, directly influ-

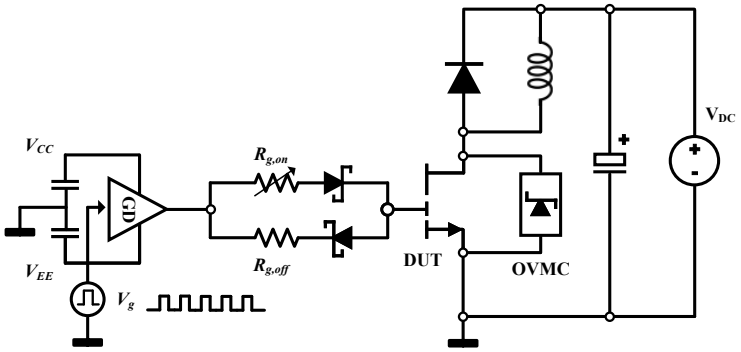


Figure 3.11: Schematic of the Multiple Pulse Test (MPT) setup with variable $R_{g,on}$ to apply different external gate resistance values under specific multiple pulse test conditions. The ON-state Voltage Measurement Circuit (OVMC) captures the ON-state voltage to determine the dynamic ON-resistance during each conduction state.

encing both switching losses and the associated energy and time available for charge trapping phenomena [218].

Figure. 3.12 shows the MPT test case pulse characteristics for 300 V, where each on-state pulse width is fixed at 20 μs and the off-state pulse width fixed at 150 μs. However, varying on-state widths are applied for different voltage levels to maintain a consistent load current across the test cases while keeping the off-state pulse width at 150 μs. Moreover, another test case at 2 μs off-state pulse width was conducted to understand the pulse width dependency.

The external gate resistance during turn-ON ($R_{g,on}$) was varied across a range of values: 5 Ω, 10 Ω, 15 Ω, 21 Ω, 30 Ω, and 47 Ω. As discussed in the previous sections, gate resistance plays an important role in influencing the switching dynamics of GaN HEMT devices. The experimental results, depicted in Figure. 3.13, illustrate these effects. Notably, lower gate resistance values correlate with faster switching speeds, which are accompanied by increased oscillations during the switching transitions. In contrast, as the gate resistance increases, the switching speed decreases, and the oscillatory behavior becomes less pronounced.

Figure. 3.14 presents the effects of varying external gate resistance on the voltage slew rate, current slew rate, and associated switching losses. Figure. 3.14(a) and Figure. 3.14(b) show

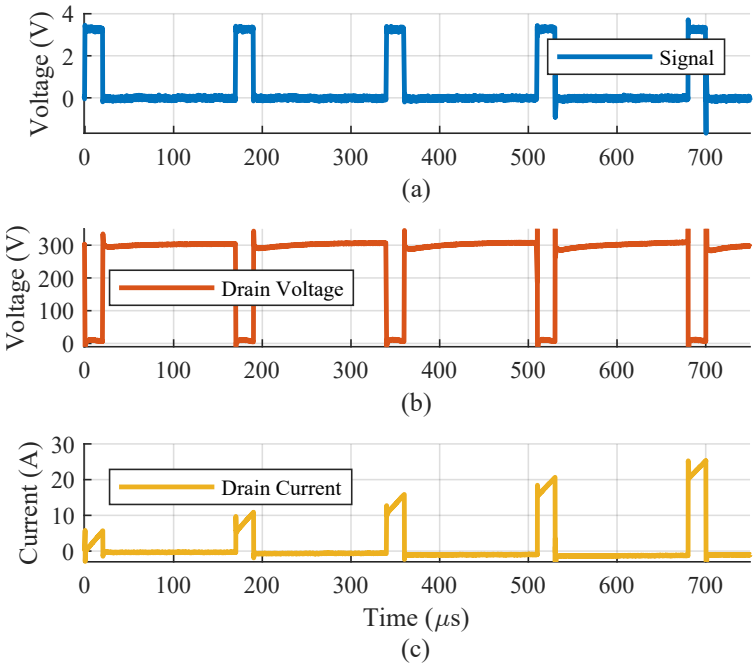


Figure 3.12: MPT waveforms illustrating five consecutive pulses with 20 μs on and 150 μs off with: (a) MPT gating signal applied to the device's gate, (b) drain voltage switching waveforms with 300 V stress, and (c) drain current switching waveform of different current ranges during each pulse duration.

a distinct correlation between gate resistance and the slew rates of both voltage and current during the turn-ON transition, with these parameters exhibiting a linear relationship as gate resistance changes. This behavior has a direct impact on switching losses, which are observed to increase with higher gate resistance values as seen in Figure. 3.14(c).

For the cascode GaN HEMT, a slight increase in turn-ON energy loss, E_{ON}, is observed with increased gate resistance, likely due to the extended duration of the transition period, resulting in more overlap of voltage and current. These increases in switching losses not only affect the efficiency of the power converter but can also contribute to thermal stress within the device, potentially impacting the trapping phenomenon. However, in this study, the impact of self-heating from the increased switching loss is minimal, and the additional loss generated from increased gate resistance is expected to be small, considering the pulse

duration and the thermal characteristic impedance of the device with a small increase (±5%) in the turn-ON energy loss.

Based on the experimental setup illustrated in Figure. 3.11, the external gate resistance was varied between 5 Ω and 47 Ω, and the drain voltage was adjusted from 100 V to 600 V to analyze the combined effects of these parameters on dynamic on-resistance. Figure. 3.15 presents

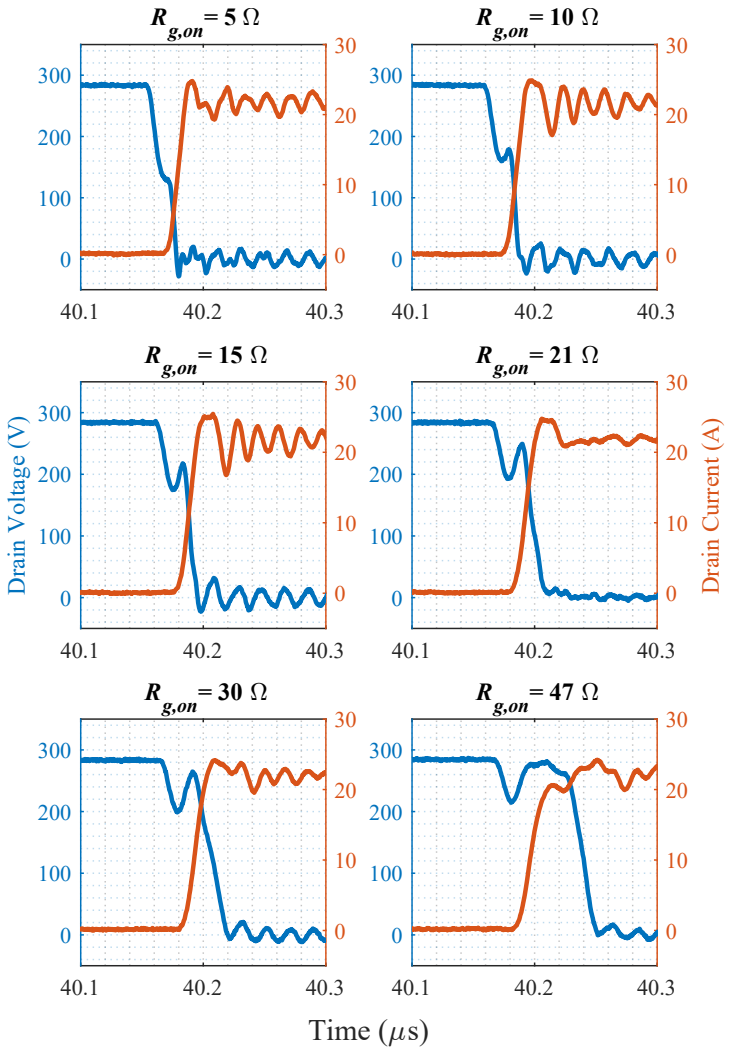


Figure 3.13: Effects of external gate resistance, $R_{g,on}$ on GaN device voltage and current switching transients. The gate resistance value is varied between 5 Ω, 10 Ω, 15 Ω, 21 Ω, 30 Ω, and 47 Ω. The left y-axis is the drain voltage in volts, the right y-axis is the drain current in amps, and the x-axis is the time in μs.

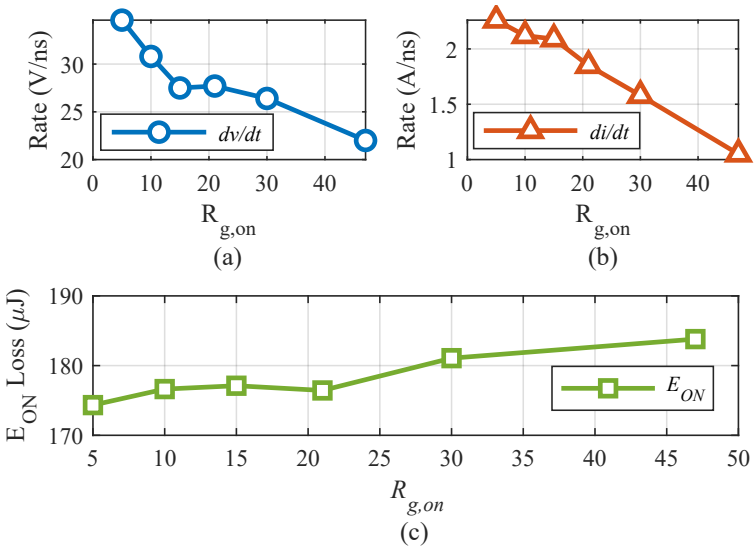


Figure 3.14: Relationship between external gate resistance and: (a) voltage slew rate, (b) current slew rate, and (c) switching losses during turn-ON switching transition.

the experimental findings, comparing the impact of external gate resistance on dynamic on-resistance in the cascode GaN HEMT. The dynamic on-resistance values have been normalized against the static or DC on-resistance measured at room temperature (R_{ON}(dc,25°C) to ensure a direct comparison.

The cascode GaN device exhibits a response that is dependent on both voltage and gate resistance. While increasing external gate resistance results in a slight increase in dynamic ON-resistance, with the effects being slightly more pronounced at higher voltages, the overall impact remains relatively modest within the tested range. This indicates that, for this specific cascode GaN device, gate resistance may influence dynamic ON-resistance but does not appear to be the dominant factor.

However, the impact of the drain voltage on dynamic on-resistance is more noticeable in the cascode GaN device as shown in Figure. 3.16. As the drain voltage increases, the dynamic on-resistance exhibits a more elevated impact, highlighting voltage stress as a critical factor influencing the dynamic behavior of GaN HEMTs. The impact is highest at around 150

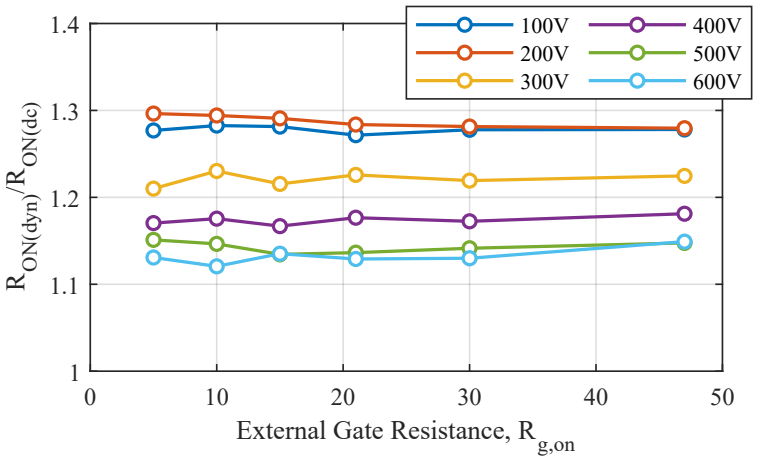


Figure 3.15: Experimental results illustrating the effects of external gate resistance and voltage on dynamic on-resistance, normalized to the static on-resistance for cascode GaN HEMT.

V and gradually decreases as the voltage increases, as is also observed in prior literature [57, 252]. This voltage dependency suggests that cascode GaN devices can be susceptible to charge trapping effects, which in turn increases the dynamic on-resistance following the trend shown in Figure. 3.16.

When comparing the experimental results of both Schottky gate p-GaN and cascode GaN HEMTs under hard-switching conditions [266], a slightly elevated response is observed between 100 V and 150 V, although results for higher voltages are well-aligned with the literature. Furthermore, the results show minimal changes between the $R_{g,on} = 5\Omega$ and $R_{g,on} = 47\Omega$ cases.

Despite variations in turn-on gate resistance demonstrating an increase in dynamic on-resistance through a DPT [267], this study provides a MPT-based setup that ensures hard-switching operation with minimal self-heating effects on the cascode GaN DUT. Even though the energy loss through the device can be used to deduce a relationship between dynamic on-resistance and the generation of hot electrons from continuous operation, changes in slew rates are not a major concern in this multiple pulse test for a cascode GaN HEMT.

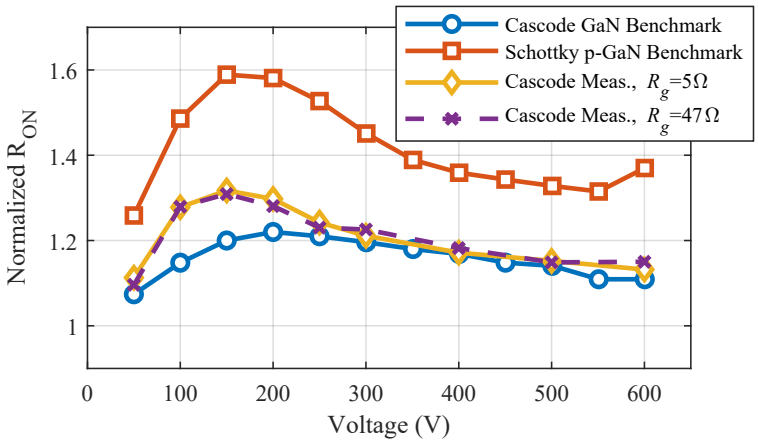


Figure 3.16: Experimental results showing the effect of the applied voltage on normalized ON-resistance for cascode GaN HEMT measured with $R_{g,on} = 5\Omega$ and $R_{g,on} = 47\Omega$ and comparison against the cascode GaN benchmark [266] and Schottky gate p-GaN benchmark [266].

3.3 Summary

This chapter examined the effects of dynamic switching stress on GaN HEMTs, with a particular focus on how electric field distributions and switching conditions influence device reliability and how slew rates impact on-resistance behavior on GaN cascode. In Section 3.1, distributed resistive field plate designs were shown to enhance field uniformity and reduce peak electric fields, further improving robustness under high-voltage operation through TCAD-based analysis studies.

Section 3.2 presented an experimental evaluation of the impact of switching slew rates on dynamic on-resistance in commercial 650 V cascode GaN HEMTs. Multiple test topologies were reviewed and compared, with the multiple pulse test (MPT) selected for its ability to replicate practical switching behavior while minimizing self-heating. Experimental results demonstrated that while switching slew rate has a measurable effect on switching loss and oscillations, its impact on dynamic on-resistance on the cascode structure remains modest within the tested range.

Chapter 4

Characterization Techniques and Qualification Analysis for WBG Integration

WBG device integration into high-performance systems requires comprehensive device characteristics through precise and reliable measurement techniques. Thus, it is important to develop specialized diagnostic and qualification tools. This chapter addresses these needs by introducing advanced, non-destructive measurement and evaluation methodologies tailored to the operational context of WBG devices.

Section 4.1 details the development of an on-state voltage measurement circuit specifically designed to capture the on-state voltage of WBG devices under fast-switching conditions. Section 4.2 introduces non-destructive inspection techniques for structural and electrical evaluation of GaN HEMTs, including methods for detecting degradation signatures without interfering with device functionality. Lastly, Section 4.3 outlines the architecture and workflow of a fully automated test system capable of executing long-duration, switching-based stress protocols for dynamic reliability analysis. These tools provide a robust framework for monitoring, screening, and qualifying WBG devices for deployment in real-world power conversion systems.

4.1 On-State Voltage Measurement Circuit Topology, Operation, and Performance

The measurement of on-resistance, defined as the resistance between the drain and source of a transistor when the device is in the on state, is an important parameter to monitor to understand various aspects of device performance, reliability, efficiency, and the overall health of semiconductor devices. Accurate measurement of this parameter is particularly important for WBG semiconductor devices, which exhibit much lower specific on-resistance at a given breakdown voltage due to their high critical-field characteristics and superior channel mobility compared to Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) [268, 269]. Monitoring on-resistance provides helpful insights into a device's thermoelectric performance, state of health, physical phenomena, and informed design for system optimization, making it an essential parameter for further improving semiconductor test and measurement technology [77, 121, 270].

For instance, evaluating the thermoelectric performance of semiconductor devices involves analyzing factors such as efficiency, power loss, and heat dissipation, especially for power module packaging [271]. Accurate measurement of on-resistance is important for understanding these aspects because on-resistance directly impacts the amount of heat generated within the device during current conduction. In addition, precise measurement of this parameter ensures that the devices operate within safe temperature limits [272].

Also, on-resistance is a correlated indicator of the device's health condition; any significant changes can signal degradation or impending failure [273]. Therefore, monitoring on-resistance allows for health assessments of semiconductor devices through in-situ observation, enabling the estimation of potential failures, aging, and overall device lifetime [274, 275]. Real-time monitoring of on-resistance through the Internet of Things (IoT) offers a pow-

erful tool for capturing the long-term degradation behavior of semiconductor devices [276]. If it can be processed in real-time, the measurement of on-resistance can enable predictive maintenance, allowing for timely interventions before catastrophic failures occur, thereby reducing downtime and maintenance costs [275].

In addition, on-resistance measurement can be used to relate intrinsic properties of the materials used in semiconductor devices. In particular, GaN high-electron-mobility transistors (HEMTs) suffer from a parasitic phenomenon of increased on-state resistance during a switching event from its DC or steady-state value, known as dynamic on-resistance or current collapse [198, 277, 278, 279]. This phenomenon exhibits elevated on-resistance compared to the DC on-resistance during the conduction state after a switching transition. The severity of the trapping is significantly impacted by various operational and environmental parameters [57, 146]. Hence, the on-state resistance characteristic helps explain phenomena such as charge trapping, dynamic on-resistance performance [280], and mechanical stresses from thermal cycling [281].

For packaged power modules based on Silicon Carbide (SiC) and IGBTs, the measurement of on-resistance reveals the impacts of thermal cycling stress caused by the Coefficient of Thermal Expansion (CTE) mismatch on wire bond integrity, indicating potential degradation [282]. These measurements enable a deeper understanding of device physics fundamentals, the assessment of degradation mechanisms under operational conditions, and the development of improved packaging techniques to enhance device longevity.

Lastly, device performance and trade-off studies are facilitated by understanding the materials' on-resistance, particularly through the use of Figures of Merit (FOM) [283]. This parameter is used to compare the performance of different device materials and architectures [284]. WBG-based devices are often evaluated against traditional Si devices using on-resistance to highlight their superior performance in high-power, high-frequency switch-

Table 4.1: Device Characterization topics evaluated through ON-resistance measurements.

Characteristic	**General Description**	**References**
Thermoelectrical Performance	Analysis of power loss, heat dissipation, and safe operating area limits to evaluate thermal and electrical reliability.	[272, 280, 286, 287]
Health Monitoring	In-situ observation methods to assess aging, predict failure modes, and estimate remaining useful life or maintenance intervals.	[13, 37, 77]
Device Physics	Investigation of material-level behavior, defect-induced trapping, and physical stress phenomena affecting conduction behavior.	[198, 277, 278, 279, 282, 288]
Device FOM / Optimization	Evaluation of Figure-of-Merit (FOM), trade-offs in performance metrics, and design-oriented optimization strategies.	[24, 283, 284, 285, 289, 290]

mode power applications [285]. Thus, it is a key metric for optimizing device design while investigating the best balance of conductivity, thermal management, and breakdown voltage for overall device performance and efficiency. Table 4.1 summarizes the roles of on-resistance in relation to several characteristics of semiconductor devices. The table also provides relevant citations for each of the four characteristics: thermoelectrical performance, health monitoring, device physics, and device FOM.

In this section, a novel cascode current-mirror-based on-state voltage measurement circuit (OVMC) topology is proposed. Accurate, reliable, repeatable, and responsive measurement of on-resistance is a paramount task due to its relevance to the reasons previously described. However, the development of an accurate and reliable sensing methodology for on-state voltage or on-resistance measurement is not trivial [291, 292]; the difficulty of sensing on-state resistance through measuring the device current and voltage (i.e., Ohm's Law) is augmented when high-voltage operation causes an overdrive of the oscilloscope or acquisition system. Offsetting and expanding a portion of the waveform over a wider range can drive the sampling or acquisition window beyond the dynamic range of the amplifiers and analog-to-digital con-

verters (ADC). This causes the scope's amplifier to saturate and recover from its overdriven condition, resulting in distortions and preventing accurate measurement of the on-state voltage. Furthermore, the dynamic range of the probe, which is the ratio of the largest to the smallest values of a signal, is based on the resolution of the ADC that samples and converts the measured analog data into digitized data [293]. A challenge exists when the on-state cannot be adequately captured with a limited number of available bits to sample waveforms during the high-voltage operation of GaN HEMT.

To enable high resolution of detailed on-resistance data during the conduction state, maintaining a usable effective number of bits during the on-state to boost vertical resolution is critical. This can be implemented through the use of an on-state voltage circuit that clips off and limits the high-voltage signal during the off-state while providing a high-resolution measurement capability during the on-state.

To cope with the aforementioned on-state voltage measurement challenge, this work presents a novel circuit topology, detailing its operation and performance based on various operational conditions, highlighting the circuit's sensing capability over a wide range of switching characteristics using high-voltage WBG devices. The proposed circuit is designed based on a cascode current mirror, which ensures a steady current to minimize measurement sensitivity to the device under test (DUT) operation. This configuration enables high-resolution measurements due to the damping of the measurement peaks during the switching transitions.

Subsection 4.1.1 provides an extensive review of prior methodologies and their limitations in high-speed power applications. Subsection 4.1.2 details the design and operational principles of the proposed measurement circuit with the derivation of the large signal model of the proposed circuit networks. Subsection 4.1.3 covers practical implementation aspects and design consideration, including probe placement, feasible design regions, and sensitivity analysis for temperatures. Lastly, Subsection 4.1.4 presents a comparative analysis of exper-

imental results obtained from static and dynamic switching tests, highlighting the circuit's performance while showing its comparison to that of COTS.

4.1.1 Technical Review of Prior State-of-the-Art

A variety of clipping or on-state voltage circuits have been surveyed in the literature. Figure. 4.1 shows various clipping circuits found in prior art, and Table 4.2 describes each circuit's key benefits as well as its limitations. To provide a performance comparison metric, it is noteworthy to highlight several important aspects of the measurement requirements for WBG transistors: (a) fast dynamic response with small measurement delay, (b) non-loading effects on the device turn-on or turn-off speed, (c) independence from temperature and load currents, (d) small measurement accuracy error, (e) minimal overshoot and undershoot to prevent probe overdrive and maintain high resolution, (f) high bandwidth, and (g) in-situ measurement capability to enable high-voltage continuous switching operation.

Figure. 4.1(a) topology uses a Zener diode as a peak clipper configuration [294]. During the blocking state, the Zener diode clamps the high-voltage drain bias to a lower clamping voltage level while allowing on-state voltage measurement during the conduction state. The main advantage of this Zener peak clipper circuit is its low part count requirement, making it a simple, low-cost design. However, a resistor is required with the Zener diode to limit the current during the high-voltage blocking state. Moreover, the RC time constant of the element network between the resistor and the parasitic capacitances of the diodes causes a significant measurement delay, which provides insufficient bandwidth for high-frequency switching operation.

Figure. 4.1(b), as introduced in [295], deploys a normally-on transistor to block the high-voltage drain bias during the off state. During the off transition, the voltage potential of

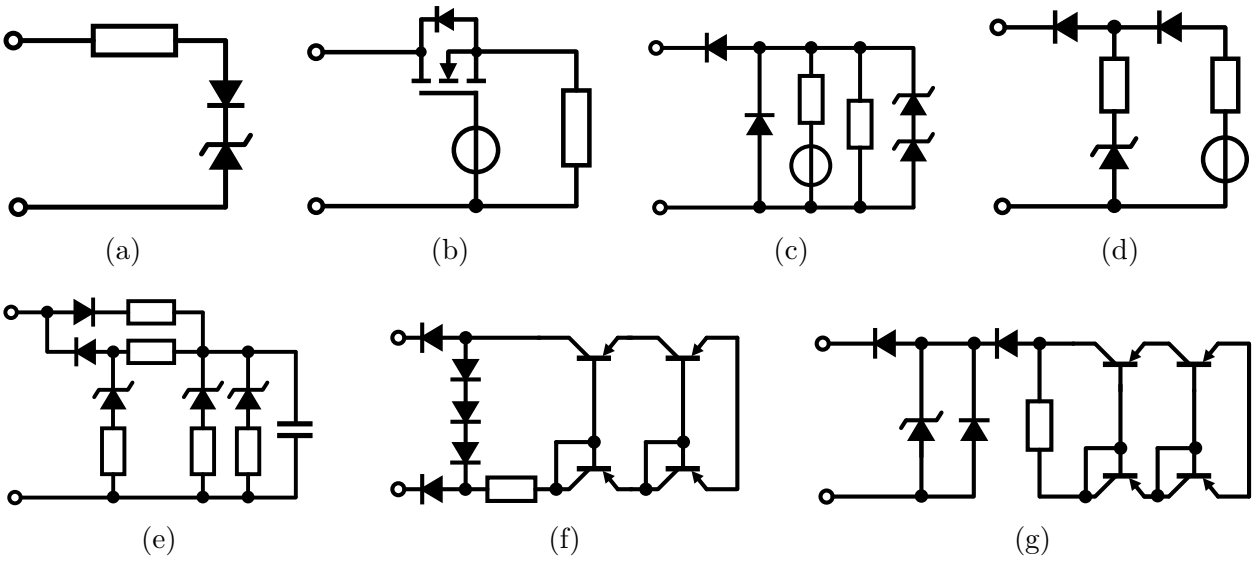


Figure 4.1: Survey of ON-state voltage measurement topologies from prior literature: (a) Zener-based, (b) MOSFET-based, (c) Resistive divider-based, (d) Dual diode-based, (e) Capacitor charge-based, (f) Current mirror-based, (g) Current source-based (proposed).

the source terminal increases, dropping the gate-source voltage nodes below the threshold voltage of the transistor and subsequently turning off the device. On the other hand, when the DUT turns on, the source terminal of the transistor decreases, causing the gate-source voltage to become higher than the threshold voltage, which subsequently turns on the device to allow on-state voltage measurement. Like Figure. 4.1(a), this circuit provides a simple design and operation. However, a large voltage overshoot can occur during the switching transitions due to the junction capacitance of the normally-on transistor, potentially causing probe overdrive, low resolution measurement, and low accuracy. The normally-on transistor also requires a high-voltage blocking capability to ensure safe operation when this circuit is used for high-voltage GaN HEMTs or SiC MOSFETs.

Figure. 4.1(c), described in [267], implements a resistive divider network along with a voltage source to provide a clamping voltage bias during the blocking state. The clamping voltage also provides a forward voltage bias for the high-voltage blocking diode during the DUT on-state, which allows for the measurement of the on-state resistance. The main advantage

Table 4.2: Advantages and disadvantages of state-of-the-art ON-state voltage measurement circuit topologies.

ID	Reference	Advantages	Disadvantages
(a)	[294]	Simple configuration Low part count and cost Small voltage overshoot	Requires resistor tuning for Zener power dissipation Large RC time constant causes delay Challenging for high-frequency operation
(b)	[295]	Simple and cost-effective Low component count	Large blocking voltage requirement for MOSFET Requires R tuning based on C_{oss} Measurement delay due to tuning
(c)	[267]	Immune to RC delay Fast response	Requires power supply for biasing Limited operation range due to R tuning Sensitive to transients; possible overshoot
(d)	[296]	No RC time constant dependency Fast dynamic response Compensates diode voltage accurately	Requires differential sensing Needs external bias and current-limiting resistor Susceptible to transient-induced overshoot
(e)	[297]	No external power supply required No differential probe needed	RC element tuning required Limited DUT voltage/current range
(f)	[298]	Fast and RC-independent response Suitable for wide DUT operation range	Requires differential sensing High part count Added current source losses
(g)	Proposed [299]	Fast response with minimal overshoot No differential probe needed Supports wide operating conditions	Requires power supply for current source Careful current mirror selection needed Added losses from current source

of this circuit is its fast sensing speed measurement capability through the diode discharge path during the DUT switching transitions. However, the disadvantages include the need for careful tuning of the resistive voltage divider network and Zener diodes to prevent large voltage spikes during the switching transitions. Furthermore, the design can be limited to a small range of load current operation, as it is constrained by the resistor selection.

Figure. 4.1(d) from [296] is implemented with two identical diodes configured in series at the input. During the DUT off-state, the Zener diode provides the clamping voltage bias, whereas the on-state bias is set by the power supply with a resistor. By characterizing one of the two identical diodes, the blocking diode voltage drop caused during the DUT on-state can be calculated and subtracted indirectly without having to sense the high-voltage node. Although this method provides precise and high-bandwidth measurement capability with a 50 Ω termination, it requires the use of a differential voltage measurement sensing mechanism. Such a mechanism, like a differential amplifier, is necessary to accurately subtract the diode voltage drop. Moreover, manufacturing variations can occur from part to part, necessitating an electrical characterization screening to ensure that the two components exhibit the same electrical behavior [300].

Figure. 4.1(e), which was developed in [297, 301], operates with a capacitor charging and discharging mechanism. When the DUT turns off, the capacitor charges via the turn-off path diode up to the Zener voltage. This action establishes the clamping voltage necessary for the high-voltage drain bias. When the DUT turns on, the capacitor discharges through the turn-on path diode while providing a voltage reference for the on-state voltage measurement. This topology does not require a voltage supply to bias the blocking diodes. However, the circuit is prone to potentially large voltage spikes during the DUT switching transients, causing measurement overdrive. Moreover, the design requirements for charging and discharging are based on the switching voltage and current of the DUT, which requires precise tuning of

the RC network and consequently restricts the operational range of the DUT to a narrow spectrum.

Figure. 4.1(f) shows a current mirror-based on-resistance measurement circuit design [298]. High-voltage diodes are used to block the drain bias during the DUT off state while clipping the high voltage to a clamping voltage level determined by the number of diodes placed in series. When the DUT is on, the current mirror allows current to flow through the high-voltage diodes, providing high-resolution measurement of on-state voltage. This circuit provides high bandwidth, small measurement delay, and low noise measurement of on-state voltage. However, a differential probe is required across the clamping diodes, making the measurement dependent on the probe selection and its specifications, such as common-mode noise rejection. In addition, a large number of parts are required, making it less ideal for a simplistic design.

Figure. 4.1(g) shows a preview of the proposed topology, which uses a PNP current source to drive fixed ON-OFF current amplitudes through two identical diodes [299]. Though a more detailed operation principle is described in the next section, this circuit provides fast dynamic measurement with high sensing speed, no requirement of an active probe for the diode voltage drop compensation, small voltage overshoot and undershoot, and independent from the DUT operational parameters, allowing a wide operational range across switching frequency, blocking voltage, and load current. Furthermore, a voltage compensation network is incorporated to subtract the voltage drop across the viewing diode. This network includes a 50 Ω termination connection to the measurement scope, which enables high-bandwidth measurements without the bandwidth limitations of the probe selection.

While Table 4.2 does not provide a comprehensive enumeration, it presents a broad technical overview of the prevalent techniques employed for on-state voltage measurement. Other unique topologies can also be referenced [228, 250, 252, 302, 303, 304, 305].

4.1.2 Proposed Measurement Circuit Topology Analysis

The proposed novel on-resistance measurement circuit improves upon the shortcomings of prior art while combining the benefits and important characteristics observed in the state-of-the-art measurement techniques explored in Table 4.2. Figure. 4.2(a) shows the configuration of the novel measurement circuit for the DUT. The circuit topology employs a PNP cascode current mirror framework. The current mirror is configured in such a way that it eliminates the floating ground reference issue encountered in [298]. With the proposed circuit, the clipped on-state measurement, v_m can be measured referenced at the same ground point as the DUT source. In other words, the probe ground reference is at the same node as the DUT for measuring both v_{gs}, v_{ds}, and v_m, which is sensed across the Zener diode, D_Z. This configuration eliminates the necessity for a differential probe when measuring the on-state of the low-side DUT. Lastly, the Schottky diode, D_S, is used to facilitate the discharge path for the blocking diode's parasitic capacitance, enabling fast sensing speed.

This circuit also uses two identical blocking diodes: one diode denoted as D_b to block the high-voltage bias from the DUT and another biasing diode, D_m, to mirror the voltage drop of the blocking diode. The blocking diode should be rated high enough to withstand the high-voltage drain bias of the DUT, whereas the mirroring diode is the same as D_b but is used as the voltage compensation reference diode to mirror the blocking diode and calculate the voltage drop across it during the on-state. This current-driven methodology eliminates the need to sense the diode voltage with a differential operational amplifier design, as suggested in [296], due to a fixed, non-varying current set-point that is independent of the DUT load conditions. Moreover, it can provide a steady reference voltage regardless of the DUT current magnitude.

To regulate the sensitivity of the diode voltage bias to temperature fluctuations, careful se-

lection of the operating current amplitude, aligned with a point on the forward characteristic graph that reduces the impact of temperature changes on the voltage drop across the diodes, results in optimal operating conditions. This approach ensures that the voltage drop across the diodes remains relatively stable, even in the face of temperature variations.

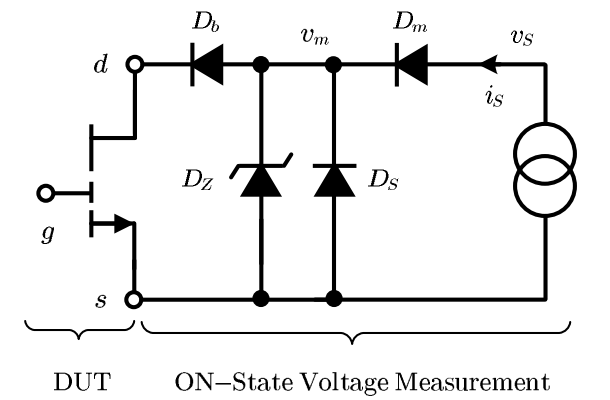
Figure. 4.2(b) illustrates the on-state current source path, I_s, and its operation through the diodes, D_b and D_m, which biases them at the same forward voltage drop condition: $v_{D_b}(\text{ON}) = v_{D_m}(\text{ON}) = V_F$. Here, on defines the state when the DUT is on, and vice versa for off (i.e., $v_{D_b}(\text{OFF}) = v_{D_m}(\text{OFF}) = V_F'$), which can be shown in Figure. 4.2(c). Figure. 4.2(c) describes the large-signal steady-state operation of the proposed circuit during the DUT off state. The high-voltage drain bias is blocked by D_b, and the voltage is clamped to the Zener voltage, V_Z, which allows high-resolution on-state voltage measurement. In this stage, the current source will change to a smaller value, I_s', based on the off-state voltage potential at V_S', which includes the diode Zener voltage bias.

To properly understand the operating principles of the on-state current measurement circuit, the voltage potential, v_S, during the DUT on and off states needs to be calculated. The steady-state value at the node v_s changes from V_s to V_s' when the DUT is on or off as follows:

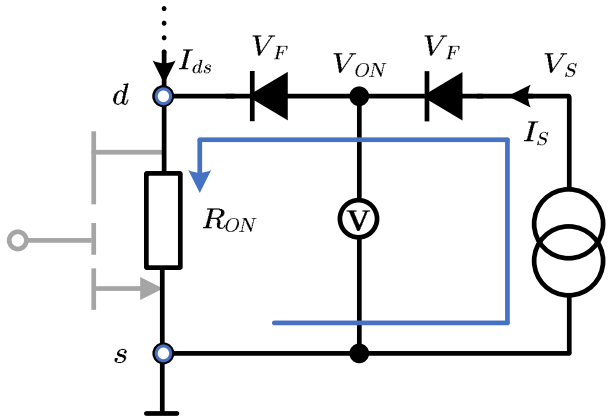
$$v_s = \begin{cases} V_s = 2V_F + (I_{ds} + I_s)R_{ON}, & \text{DUT is on,} \\ V_s' = V_Z + V_F', & \text{DUT is off,} \end{cases} \tag{4.1}$$

where I_{ds} is the actual on-state current through the drain and source of the DUT. The forward voltage drop of the diode during the on-state is denoted as $V_F = v_F(I_s)$, whereas the off-state forward voltage drop is expressed as $V_F' = v_F(I_s')$, depending on the current of the mirror source. The forward voltage drop of the diode can be calculated using the expression shown in (4.2):

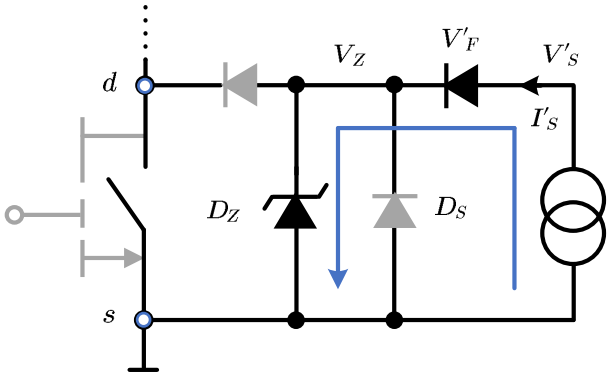
$$v_F = N \cdot V_T \ln\left(1 + \frac{i_s}{I_{sat,D}}\right), \tag{4.2}$$



(a)



(b)



(c)

Figure 4.2: Operating principle of the proposed ON-state voltage measurement circuit: (a) measurement configuration with the DUT, (b) ON-state voltage measurement biased by the current source when the DUT is ON, and (c) OFF-state voltage clamped by the Zener diode, including the current source path.

where N is the diode ideality factor, V_T is the thermal voltage, and $I_{sat,D}$ is the saturation current of the diode. The measured drain voltage, V_{ds}, is impacted by the current mirror source, i_s, as it flows through the channel in addition to the load current, I_{ds}. Therefore, V_{ds} is equal to the additional voltage drop from the added current mirror across the device on-resistance (i.e., $V_{ds} = (I_{ds} + I_s) \times R_{ON}$).

Using the equations expressed in (4.1) and (4.2), the on-resistance, R_{ON}, can be determined by measuring the voltage potential at v_m and subtracting the diode drop, v_F, while dividing by the total current seen by the device. This relationship is expressed in (4.3).

$$R_{ON} = \frac{V_m - v_F(I_s)}{I_{ds} + I_s}. \tag{4.3}$$

However, an accurate measurement of R_{ON} is achieved by monitoring the diode forward bias, which is dictated by the current source magnitude. The optimal on-state value of the current mirror, I_s, requires careful tuning and consideration of various design parameters, which are further described in the next section. Once I_s is selected, the off-state current source magnitude, I_s', can be determined by V_s' as expressed in (4.4), where V_Z is the voltage of Zener diode D_Z.

$$V_s' = V_Z + V_F'. \tag{4.4}$$

Note that I_s' will flow through D_Z, as denoted in Figure. 4.2(c). The selection criteria for D_Z should be based on the power dissipation caused by I_s'.

The proposed on-resistance or on-state measurement circuit (OVMC) employs a current source to drive the measurement circuitry via a cascode current mirror configuration, as depicted in Figure. 4.3. This particular topology is designed to enhance current matching, improve precision, and increase output impedance. The cascode current mirror is configured

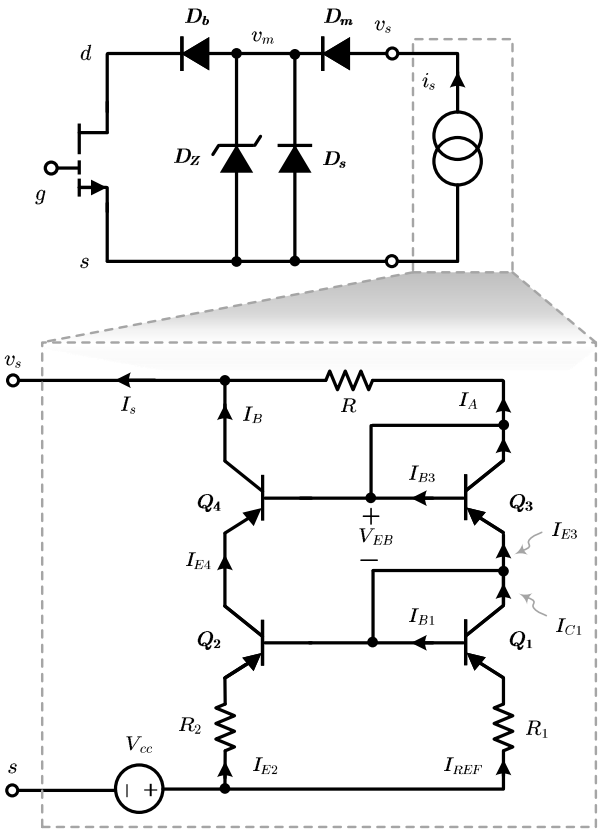


Figure 4.3: Schematic of a PNP BJT cascode current mirror topology, showing both passive and active components. Key signal nodes are labeled to support further circuit-level analysis.

using four PNP Bipolar Junction Transistors (BJTs): Q_1 and Q_2 as the current mirror transistors, and Q_3 and Q_4 as the cascode transistors.

A current mirror is a circuit designed to replicate (or mirror) the current flowing through one active device (Q_1) by controlling the current in another active device (Q_2) within the circuit. Such an arrangement can be beneficial as it maintains the output current constant irrespective of loading conditions. In the context of the current mirror, the cascode configuration, which is a two-stage amplifier, increases the output resistance and bandwidth compared to a single-transistor topology.

Schematically, the bases of Q_1 and Q_2 are tied together. Furthermore, Q_1 and Q_2 are configured such that the base of Q_1 is connected to its collector, making it diode-connected. In

this configuration, Q_1 sets the reference current, which is then mirrored by Q_2. The emitters of Q_1 and Q_2 are connected to the power supply V_{cc} through the emitter resistors R_1 and R_2, respectively. These resistors are distributed across each branch of the current mirror, providing improved control over the individual branch currents and thereby enhancing thermal stability [294, 306]. R_1 and R_2 set the desired amplitude of the current mirror to bias the blocking diodes.

Q_3 and Q_4 are configured as cascode transistors to enhance the performance of the current mirror formed by Q_1 and Q_2. The emitters of Q_3 and Q_4 are connected to the collectors of Q_1 and Q_2, respectively. The bases of Q_3 and Q_4 are tied together and connected through a tuning resistor R to the voltage reference or common node denoted as v_s, where the DUT and the blocking diodes, D_b and D_m, are connected. The voltage bias at this node, v_s, can vary based on the DUT's ON-OFF switching operation, causing the magnitude of the current source to fluctuate during the on and off periods.

4.1.3 Design Considerations and Auxiliary Hardware

The reference current I_{REF} of the current mirror is a critical design parameter that must be carefully selected. This parameter is influenced by several factors, including the supply voltage V_{cc} and the resistance R, which together define the operating point of the current sensing circuit. A step-by-step derivation of I_{REF} in terms of the design parameters V_{cc} and R is provided in greater detail for both on and off states. During this analysis, an equivalent resistance R_{eq} is introduced, which represents the combination of R_1 and R, defined as $R_{eq} = R + R_1$.

The voltage bias at v_s, when the device operates from on to off and vice versa, is expressed according to (4.1). The equation involving v_s depends on the diode forward voltage, V_F, the

device current, I_{ds}, and device on-resistance, R_{ON}, while the diode forward voltage, V_F, and Zener diode voltage, V_Z, are relevant for the off state.

For the case when the DUT is on, (4.1) for on can be equated with (4.5) along with the diode forward bias (V_F) and the emitter-base voltage drop of the PNP BJTs (V_{EB}), which are expressed as (4.6)-(4.7), respectively:

$$v_s = V_{cc} - 2V_{EB} - I_{\text{REF}} R_{eq}, \tag{4.5}$$

$$V_F = N \cdot V_T \ln\left(\frac{2I_{\text{REF}}}{I_{sat,D}}\right), \tag{4.6}$$

$$V_{EB} = V_T \ln\left(\frac{I_{\text{REF}}}{I_{sat,B}}\right). \tag{4.7}$$

The on state equation involving I_{REF} as a function of V_{cc} and R_{eq} is expressed as (4.8) when V_F and V_{EB} are substituted with (4.6) and (4.7):

$$\begin{aligned} V_{cc} - I_{ds}R_{\text{ON}} - I_{\text{REF}}(R_{\text{eq}} + 2R_{\text{ON}}) = \\ 2V_T \ln\left(\frac{2^N I_{\text{REF}}^{N-1} I_{\text{sat,B}}}{I_{\text{sat,D}}^N}\right). \end{aligned} \tag{4.8}$$

To solve for I_{REF} in terms of V_{cc} and R_{eq}, I_{REF} must be isolated by rearranging the terms. Moreover, $V_{\text{eq,ON}}$ is defined as a variable expressing (4.9) to facilitate further factoring and simplification throughout the derivation process.

$$V_{\text{eq,ON}} = V_{cc} - I_{ds}R_{\text{ON}} - 2V_T \ln\left(\frac{2^N I_{\text{sat,B}}}{I_{\text{sat,D}}^N}\right). \tag{4.9}$$

Using $V_{\text{eq,ON}}$, the expression (4.8) can be further simplified to (4.10):

$$\ln(I_{\text{REF}}) = \frac{V_{\text{eq,ON}} - I_{\text{REF}}(R_{\text{eq}} + 2R_{\text{ON}})}{2V_T(N-1)}. \tag{4.10}$$

By applying the exponential function with base e to both sides of (4.10), a new equation is established, as expressed in (4.11):

$$I_{\text{REF}} \exp\left(\frac{I_{\text{REF}}(R_{\text{eq}} + 2R_{\text{ON}})}{2V_T(N-1)}\right) = \exp\left(\frac{V_{\text{eq,ON}}}{2V_T(N-1)}\right). \tag{4.11}$$

Since I_{REF} variable appears both in the base and the exponent, the Lambert W function, denoted as $W(z)$ is employed to solve equations involving exponentials and to handle the transcendental equations, allowing for the analytical determination of parameters such as I_{REF}. The Lambert W function is defined as:

$$\begin{aligned} xe^x &= z, \\ x &= W(z). \end{aligned} \tag{4.12}$$

By defining both x and z as follows:

$$x = \frac{I_{\text{REF}}(R_{\text{eq}} + 2R_{\text{ON}})}{2V_T(N-1)},$$

$$z = \exp\left(\frac{V_{\text{eq,ON}}}{2V_T(N-1)}\right).$$

The final expression can be derived in (4.13) by applying the Lambert W function:

$$I_{\text{REF}} = \frac{2V_T(N-1)}{R_{\text{eq}} + 2R_{\text{ON}}} W\left(\frac{R_{\text{eq}} + 2R_{\text{ON}}}{2V_T(N-1)} e^{\frac{V_{\text{eq,ON}}}{2V_T(N-1)}}\right). \tag{4.13}$$

A symbolic solution for I_{REF} using the Lambert W function is derived, providing a comprehensive approach to solving transcendental equations based on the variables involved, including V_{cc}, R_{eq}, and other constants.

Similarly, for the off state, (4.1) for off can be equated with (4.5) along with the diode forward bias (V_F), the emitter-base voltage drop of the PNP BJTs (V_{EB}), and the Zener voltage, (V_Z), which are expressed as (4.6)-(4.7), respectively. The off-state equation for (I_{REF}) can be expressed as (4.14):

$$V_{\mathrm{cc}} - I_{\mathrm{REF}} R_{\mathrm{eq}} - V_Z = V_T \ln\left(\frac{2^N I_{\mathrm{REF}}^{N+2}}{I_{\mathrm{sat,D}}^N I_{\mathrm{sat,B}}^2}\right). \tag{4.14}$$

$V_{\mathrm{eq,OFF}}$ is defined as a variable, expressed in (4.15), to facilitate the factoring and simplification throughout the derivation process.

$$V_{\mathrm{eq,OFF}} = V_{\mathrm{cc}} - V_Z - V_T \ln\left(\frac{2^N}{I_{\mathrm{sat,D}}^N I_{\mathrm{sat,B}}^2}\right). \tag{4.15}$$

Using $V_{\mathrm{eq,OFF}}$ and by applying the exponential function with base e to both sides of (4.15), the new equation is further simplified and established as expressed in (4.16):

$$I_{\mathrm{REF}} \exp\left(\frac{I_{\mathrm{REF}} R_{\mathrm{eq}}}{V_T(N+2)}\right) = \exp\left(\frac{V_{\mathrm{eq,OFF}}}{V_T(N+2)}\right). \tag{4.16}$$

By defining both x and z as follow and applying the Lambert W function:

$$x = \frac{I_{\mathrm{REF}} R_{\mathrm{eq}}}{V_T(N+2)},$$

$$z = \exp\left(\frac{A}{V_T(N+2)}\right).$$

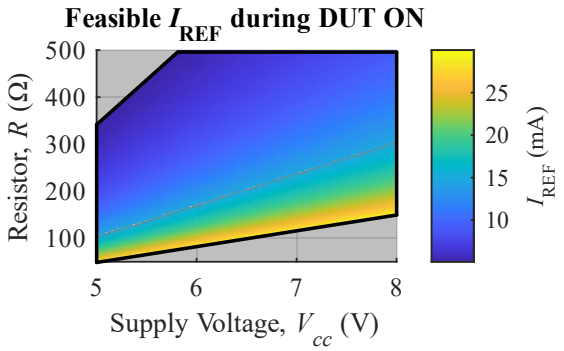
The final expression of I_{REF} for the off state can be derived and expressed as (4.17):

$$I_{\mathrm{REF}} = \frac{V_T(N+2)}{R_{\mathrm{eq}}} W\left(\frac{R_{\mathrm{eq}}}{V_T(N+2)} e^{\frac{V_{\mathrm{eq,OFF}}}{V_T(N+2)}}\right). \tag{4.17}$$

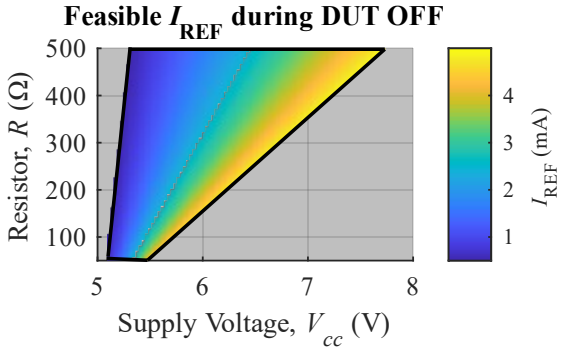
Now that I_{REF} for both the on and off states has been expressed in terms of the design parameters—supply voltage V_{cc} and the equivalent resistance R_{eq}—a multi-dimensional graph can be generated by varying the values of these design variables. This allows for the identification of the feasible operating region for desirable parameter combinations.

For instance, Figure. 4.4 shows the reference current based on selections of different supply voltage and resistor values. Figure. 4.4(a) illustrates the feasible operating area for the reference current I_{REF} when DUT is on, whereas Figure. 4.4(b) shows the feasible operating area for the reference current when DUT is off. Note that the reference current should be of a smaller value in the off state compared to the on state. Moreover, the grey shaded area represents the design null space. Figure. 4.4(c) depicts the intersection of the areas shown in Figure. 4.4(a) and Figure. 4.4(b), illustrating the final feasible operating area for different possible combinations of the supply voltage and resistor values, represented by the region around the contour lines.

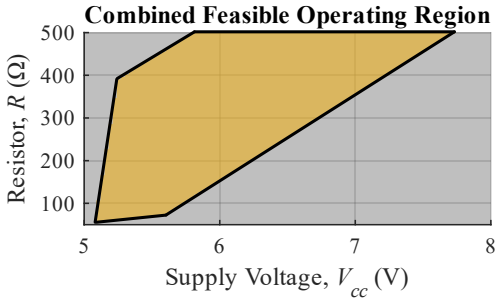
The accuracy of the proposed on-state voltage measurement circuit depends largely on ensuring that the two sensing diodes exhibit identical forward-voltage drops, such that $V_{D_m} = V_{D_b}$. However, in practice, small mismatches can arise due to reference current imbalances, manufacturing tolerances, and junction temperature differences (T_{D_m} and T_{D_b}). These factors introduce variations in the voltage drops across the diodes. In practice, the forward bias of D_b can experience a higher junction temperature than D_m because it is subjected to a wider range of voltage inputs and is physically closer to the DUT. This proximity can cause additional heat coupling to D_b due to power dissipation within the DUT.



(a)



(b)



(c)

Figure 4.4: Feasible operating regions for the ON-state voltage measurement circuit: (a) when the DUT is ON, (b) when the DUT is OFF, and (c) final design selection between V_{cc} and R.

To mitigate these effects, the measurement circuit can be designed such that the diodes operate in a region of the I-V characteristic with reduced temperature sensitivity, which is typically at higher current levels [252]. However, operating at higher currents to reduce temperature sensitivity introduces additional conduction losses in the DUT. This effect is

particularly significant for low-current-rated DUTs, where the increased power dissipation can lead to a higher junction temperature. Another mitigation strategy is to optimize the physical layout to enhance thermal coupling between the diodes [282].

Given the inevitable temperature sensitivity arising from manufacturing tolerances and physical layout, a quantification study of the measurement error based on temperature sensitivity is essential. For instance, the expected measurement error due to temperature mismatch between the two diodes can be estimated. In this circuit, the Schottky diode exhibits a temperature coefficient of approximately 1.5 mV/°C at a reference current of $I_{\text{REF}} = 20$ mA, as illustrated in Figure. 4.5(a). Although not shown, the temperature coefficient remains relatively stable up to a forward current of 200 mA, beyond which it sharply decreases. If the junction temperature difference between D_m and D_b is $\Delta T = T_{D_m} - T_{D_b} = \pm 5$°C, the resulting relative measurement error can be evaluated as a function of the DUT current,

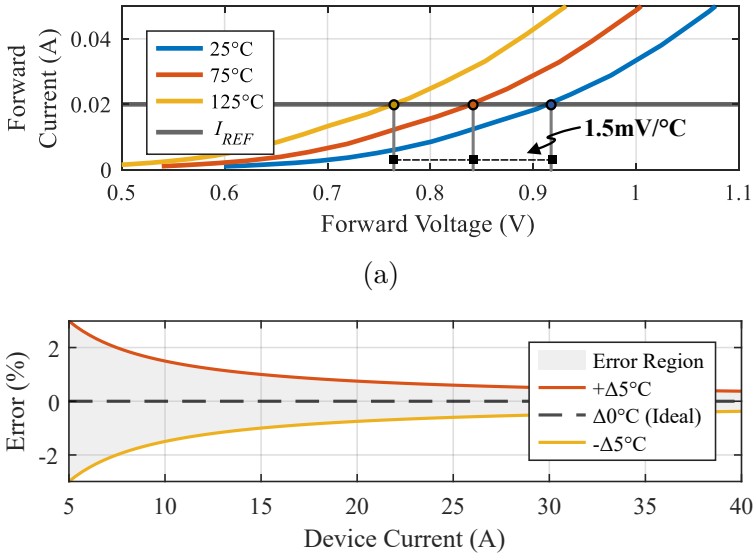


Figure 4.5: Temperature sensitivity analysis: (a) Schottky diode I–V characteristics from 25°C to 125°C, demonstrating a stable temperature coefficient of 1.5 mV/°C across varying current levels, with degradation beyond 200 mA (not shown); (b) resulting measurement error for a junction temperature deviation of ±5°C, which decreases from ±2% at 5 A to ±0.35% at 40 A.

as shown in Figure. 4.5(b). The results indicate that the error decreases exponentially as the DUT current increases, while reaching less than ±1% when the device current exceeds 15 A. This chart estimates potential measurement errors for appropriate compensation or design adjustments based on temperature sensitivity to ensure accurate on-state voltage measurements.

Mismatch or fluctuations in the reference current flowing through D_b and D_m can arise due to factors similar to those discussed earlier, including manufacturing variations and leakage paths through D_Z. To analyze the impact of such fluctuations on measurement accuracy, the percentage measurement error is studied as a function of the reference current mismatch (ΔI_{REF}) relative to the nominal reference current. Figure. 4.6 illustrates the relative error across different ΔI_{REF} percentages for nominal reference current conditions of 5, 20, 50, and 100 mA. It is observed that a negative ΔI_{REF} results in a higher measurement error compared to a positive ΔI_{REF}. This effect is due to the non-linearity of the diode's I-V characteristic, where lower currents exhibit greater variations in diode voltage compared to higher current levels. Furthermore, the relative error changes non-monotonically as the nominal reference current increases from 5 mA to 100 mA, further highlighting the influence of diode non-linearity on measurement accuracy. However, for all test cases, if the reference current mismatch remains within ±10%, the expected relative measurement error remains

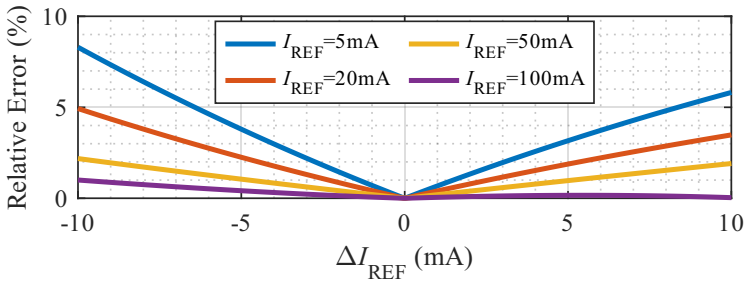


Figure 4.6: Percentage measurement error as a function of ΔI_{REF}, evaluated across different reference current levels (5 mA, 20 mA, 50 mA, and 100 mA) at an operating temperature of 75°C and device current $I_{\text{ds}} = 40$ A.

below 1.5%.

To accurately determine the on-state voltage of a device, it is essential to account for the voltage drop across the diode, denoted as V_F. This adjustment involves subtracting V_F from the measured voltage V_m as expressed in (4.18).

$$v_{ds} = v_m - v_F. \tag{4.18}$$

This subtraction can be performed manually by adjusting the measurement voltage and subtracting the pre-determined diode voltage bias V_F. However, this manual process requires additional mathematical operations within the measurement instrument, such as the oscilloscope's math function for real-time monitoring or post-processing for offline analysis.

To streamline the measurement process and reduce the need for an additional post-processing step, an alternative approach involves using an analog differential operational amplifier for compensation. This method dynamically compensates for the diode drop using an operational amplifier that adjusts its output based on the v_m and v_s measurements, thereby maintaining the accuracy of the forward voltage drop measurement under varying operating conditions. The voltage bias compensation circuit employs a high-bandwidth differential operational amplifier network with a feedback mechanism that includes a feedback resistor (R_F).

Figure. 4.7(a) illustrates the forward voltage drop compensation network implemented with the operational amplifier network, whereas Figure. 4.7(b) shows the hardware implementation of the measurement circuit. The output of the network includes a 50 Ω output resistor to match the 50 Ω load. In other words, the inclusion of the 50 Ω resistor at the termination ensures impedance matching with the load, coaxial cables, and the 50 Ω input of measurement equipment like oscilloscopes. This minimizes signal reflections, maintains a

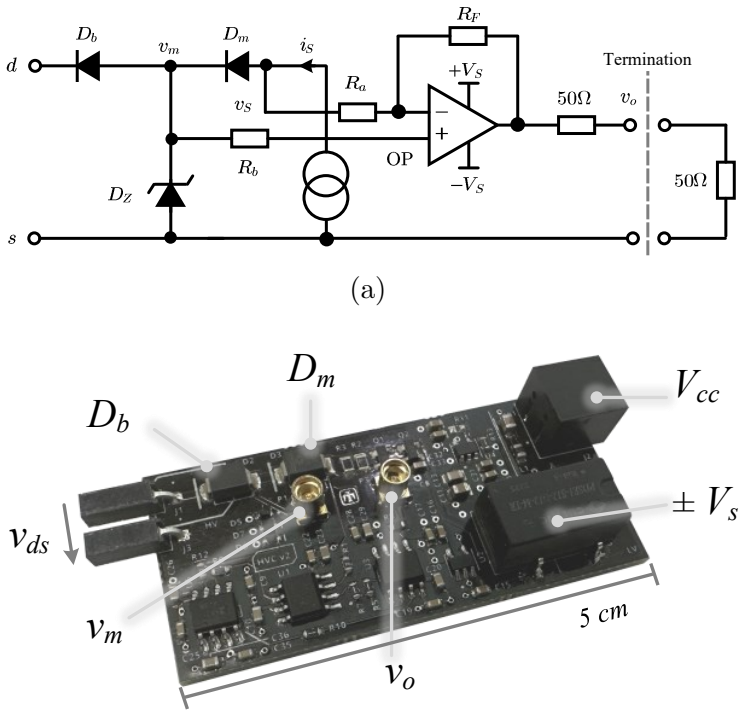


Figure 4.7: Proposed measurement implementation: (a) schematic of the diode drop compensation network using a differential operational amplifier to measure the ON-state voltage, and (b) annotated image of the hardware prototype with key voltage measurement points.

flat frequency response, and maximizes signal power transfer. High-frequency measurements benefit significantly from this design, as it avoids issues like long settling times and signal distortion commonly seen with high-impedance probes. Moreover, the operational amplifier used in the circuit provides the necessary current and bandwidth to support the 50 Ω termination without degrading performance.

It is important to note that the compensation network formed by the input resistors (R_a and R_b) along with the feedback resistor (R_F) does not conform to the standard non-inverting operational amplifier configuration. The absence of a resistor connected from the non-inverting input terminal to ground modifies the gain equation, which can be expressed as shown in (4.19):

$$v_o = v_m - \frac{R_F}{R_a}\left(v_s - v_m\right). \tag{4.19}$$

If $R_a = R_b$, (4.19) simplifies to (4.20), which represents the desired on-state voltage of the device, v_{ds}:

$$v_o = 2v_m - v_s = v_{ds}. \tag{4.20}$$

With this simple circuit modification, the operational amplifier output performs the subtraction of V_F and calculates the actual device on-state voltage.

Moreover, the positive and negative supply rails of the operational amplifier ($+V_S$ and $-V_S$) can be derived from an isolated power supply. This isolation enhances the safety and integrity of measurements in high-voltage applications, especially when measuring the high-side device with a floating ground. However, utilizing this setup requires an active differential probe or an isolated channel for the measurement instrument. By incorporating this compensation network, the diode's forward voltage drop can be dynamically calculated based on the sourced current from the current mirror. This measurement can be used along with the direct measurement at v_m to ensure proper compensation of the diode voltage and sufficient bandwidth measurement under various operational conditions.

4.1.4 Discussion of Static and Dynamic Measurement Experimental Results

The static measurement performance is an important aspect of the OVMC operation, as it requires precise measurement when the device is in the on state. Figure. 4.8(a) illustrates

the experimental setup used to measure the steady-state voltage across the resistor and to compare the OVMC performance against the ideal voltage measurement. This setup involves providing a current pulse through a high-precision load resistor and measuring the voltage across it using both a high-precision probe and the proposed OVMC. By comparing the voltage measurements from the two probes, the performance of the proposed circuit can be quantified.

Using the experimental setup shown in Figure. 4.8(a), the circuit's accuracy was evaluated over a range of current and load resistance values. The current pulse simulates the load current through the device, while the resistor R acts as the on-state resistance of the DUT. The resistance values were varied between 50 mΩ, 100 mΩ, and 500 mΩ for each current pulse condition to capture a wide range of representative device resistances. Similarly, pulse current amplitudes were generated up to 10 A to represent the load current through the device.

Figure. 4.8(b) illustrates the steady-state measurement accuracy in the μs time domain across different current levels. The test current levels were 1 A, 5 A, and 10 A. The gray lines show the actual expected measurements, whereas the colored lines represent the measurement data from the OVMC. It can be observed that when the actual voltage measurements across the resistor are compared against the experimental results, the OVMC measurements show consistent matching with the actual values over the entire measurement time period and across a range of current amplitudes. This indicates that the forward voltage drop of the blocking diode, D_b, has been accurately subtracted via the voltage compensation network across the mirrored diode, D_m.

Figure. 4.8(c) depicts the measurement comparison between the ideal and the proposed OVMC experimental results across different current and resistance values. For the static measurements, the proposed circuit ensures a consistent measurement reading of up to 99%

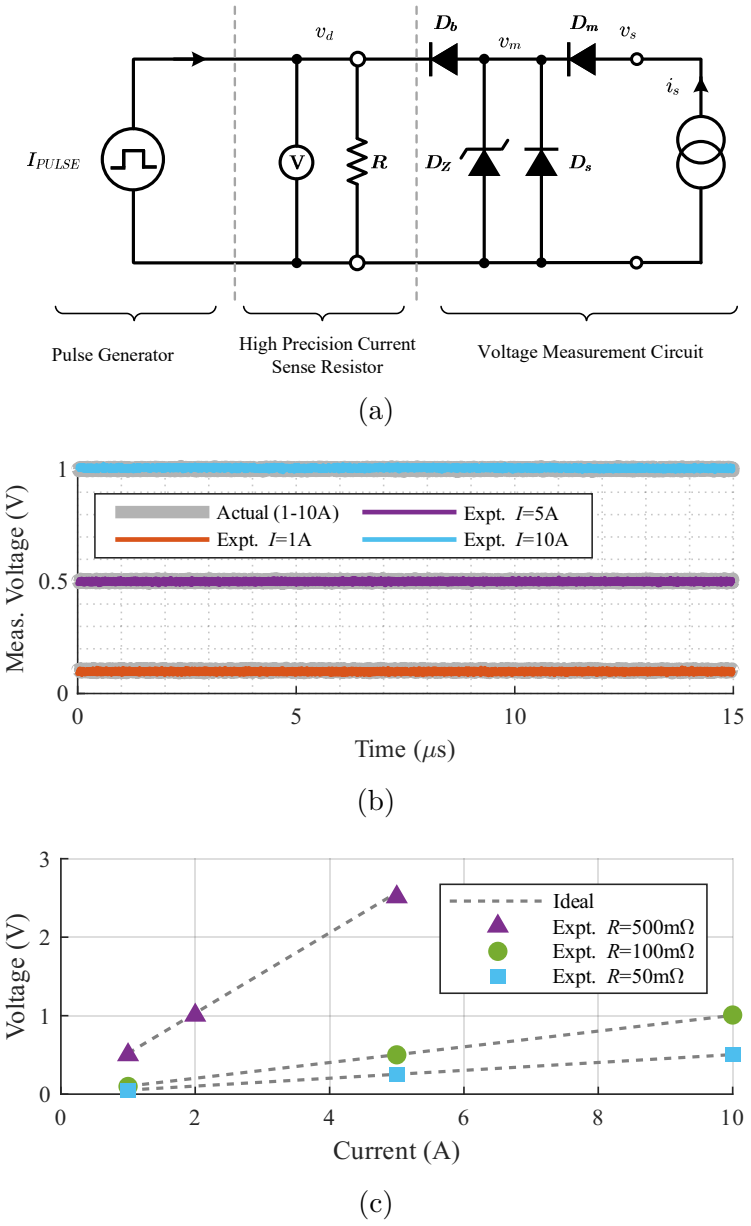


Figure 4.8: Static ON-state voltage measurement experimental results: (a) current pulse-based setup using a high-precision sense resistor R followed by the OVMC circuit, (b) steady-state voltage comparison across 1–10 A pulse amplitudes at $R = 100$ mΩ, and (c) measurement accuracy comparison across varying current and resistance values.

accuracy across various resistance and current values.

Dynamic on-state voltage measurements are performed in situ, capturing the behavior of the DUT while it operates in its intended switching environment. This method differs from static

measurements, as it subjects the DUT to the actual dynamic stresses encountered during operation, providing a more accurate representation of its performance. The schematic illustrating the integration of the voltage measurement circuit with the power converter for dynamic testing, as well as the method for capturing the on-state voltage of the DUT during active switching—where the DUT operates within the power conversion circuit—is shown in Figure. 4.9(a). The DUT used in these dynamic experiments is a 650 V, 55 A, and 55 mΩ SiC MOSFET from GeneSiC (i.e., G3F60MT06K) [307].

Figure. 4.9(b) illustrates a comparison between the device's measured voltage, the current from the current source, and the output from the on-state voltage measurement circuit, presenting both experimental and simulated converter switching waveforms. There is good agreement between the experimental data and simulation results, validating the theoretical operation of the proposed circuit while demonstrating its ability to accurately measure the on-state voltage during switching.

Figure. 4.10 illustrates the physical integration of the measurement circuit with the DUT in the power converter. The circuit's receptacle is designed to accommodate 5.09 mm (0.200") wide square header pins, ensuring compatibility with standard isolated measurement systems used by various probe manufacturers, including systems such as the Tektronix IsoVu™ [308] and the FireFly® series from PMK [309]. For through-hole packaged DUTs, the measurement circuit can be modified for direct connection, while for surface-mount parts, properly rated sensing connection pins, such as wide square header pins, offer integration flexibility.

Using the test setup described in both Figure. 4.9 and Figure. 4.10, the proposed measurement circuit has undergone testing across a variety of operating conditions to ensure its accuracy and precision, as well as to assess any potential loading effects across different DUT voltage and current ranges. Figure. 4.11(a) presents switching waveforms at 200 V and 400 V, along with the measured on-resistance, normalized to the static on-resistance

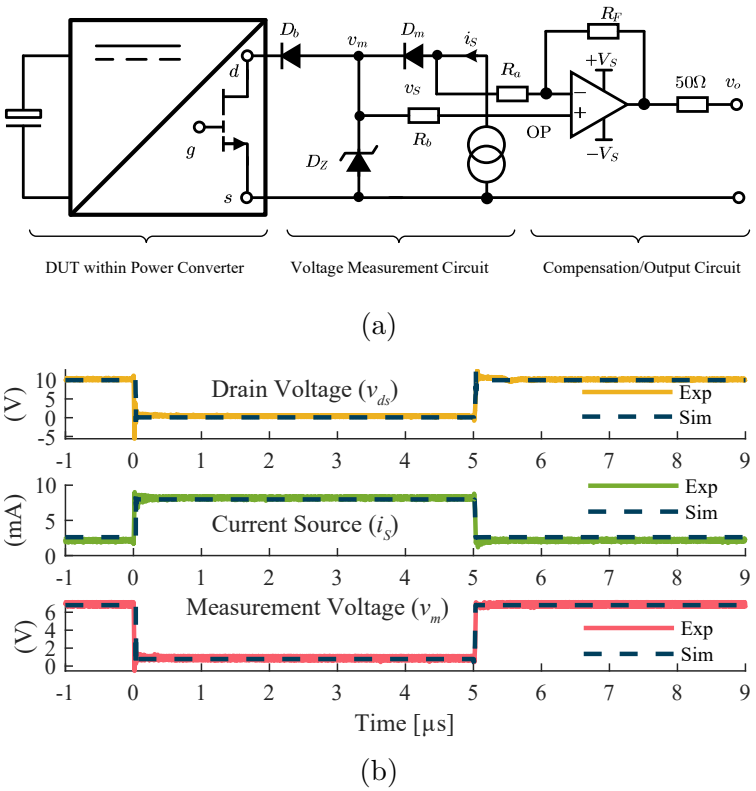


Figure 4.9: Dynamic ON-state voltage measurement: (a) schematic of the experimental setup with the OVMC integrated into a power converter, and (b) comparison of experimental and simulation results, validating circuit operation.

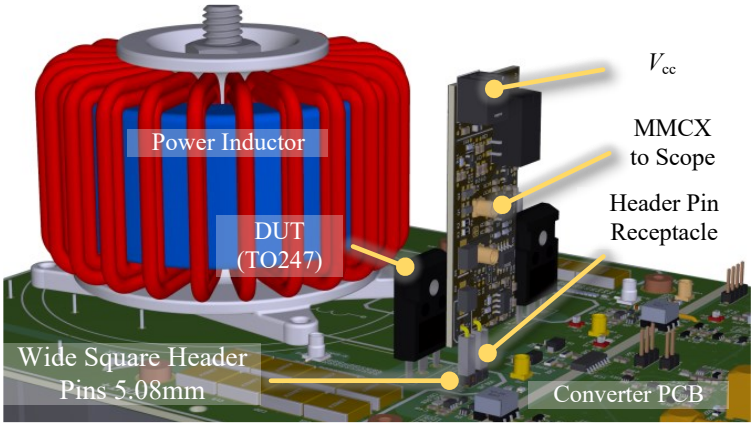


Figure 4.10: Physical integration of the OVMC to measure the ON-state voltage of the DUT within the power converter using 5.08 mm wide square header pins.

for comparison. The captured on-state voltage measurement was divided by the device current to compute the displayed on-resistance. It can be observed that the measurements are

consistent across the tested voltage conditions.

Figure. 4.11(b) shows the results of measurements taken at varying device currents—5 A, 10 A, 13 A, and 15 A—where the values are averaged over the current ramp. In each test condition, the on-state voltage was accurately captured by the measurement circuit, resulting in accurate on-resistance measurements. The results indicate that there is measurement consistency across different DUT current conditions.

Lastly, the potential loading effects of the proposed measurement circuit were evaluated by comparing the switching waveforms of the DUT with and without the measurement circuit in place. This analysis is important as the measurement circuit requires seamless integration into the converter without introducing significant loading effects that could adversely affect the overall performance of the converter. Figure. 4.11(c) presents the turn-on and turn-off transition waveforms for both 200 V and 400 V test conditions. It demonstrates that the presence of the measurement circuit does not introduce any noticeable impact on the DUT's switching behavior, such as slew rate and ringing. The experimental results confirm the proposed circuit's suitability for dynamic measurements without degrading device operation.

To ensure a focused evaluation of the proposed measurement circuit's performance, all testing was conducted using SiC devices. A fair assessment of the circuit's capability is critical in accurately capturing ON-state voltage and resistance without obscuring the effects of varying voltage and current due to potential material-dependent influences. GaN devices, in particular, exhibit distinct dynamic ON-resistance behavior that is highly dependent on specific device structures and operating conditions. A comprehensive analysis of GaN would therefore require a more extensive investigation beyond the scope of this work. Therefore, only SiC data are presented to provide a controlled and consistent assessment of the measurement circuit's accuracy and overall performance.

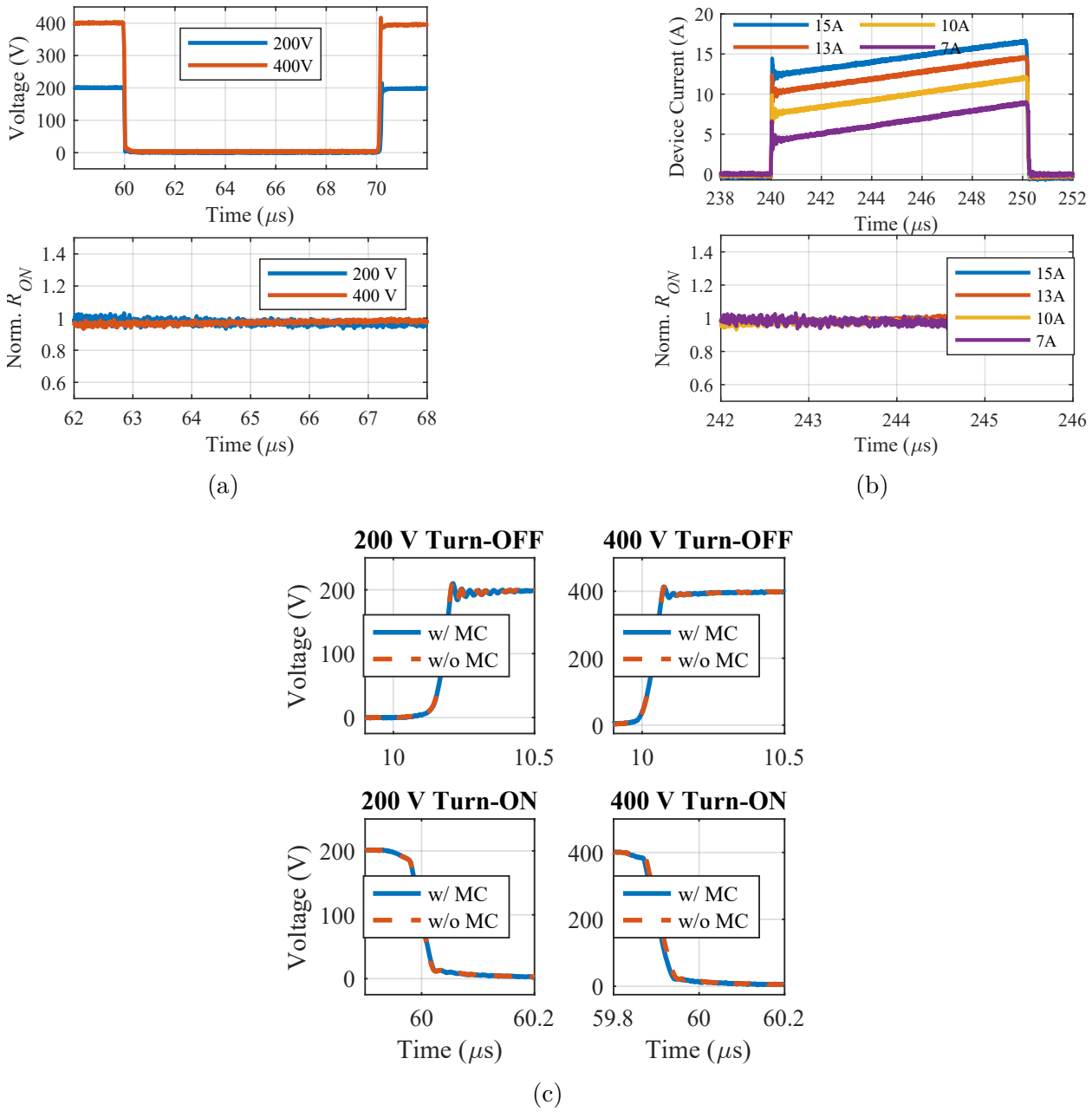


Figure 4.11: Dynamic performance comparison using the proposed OVMC: (a) across different DUT voltages, (b) across different DUT current levels, and (c) comparison of turn-ON and turn-OFF waveforms with and without the measurement circuit, showing minimal impact on DUT slew rate and ringing.

The measurement resolution is influenced by the minimum and maximum values captured during the waveform acquisition period. Achieving high-resolution measurements is paramount,

particularly when the DUT's on-resistance is very low. Therefore, it is essential to benchmark the resolution of the proposed circuit against a Commercial Off-The-Shelf (COTS) solution. Figure. 4.12(a) illustrates the measured on-resistance obtained from both the proposed circuit and the COTS (CLP1500V15A1) circuit [310]. The COTS circuit has configurable fixed clipping ranges of 2 V and 12 V, which constrain the dynamic range and limit resolution based on the expected on-state voltage. The proposed circuit achieves approximately three times higher resolution than the COTS solution, due to its narrower measurement window range, as reflected in the peak-to-peak performance. Figure. 4.12(b) compares the maximum voltage undershoot and overshoot for each circuit with the COTS' measurement clipping voltage of 2 V. The proposed circuit demonstrates superior measurement capability, with a minimum-to-maximum voltage range of approximately 4.1 V, compared to 5.6 V for the COTS circuit. This 1.5 V difference translates into a significantly higher resolution for the proposed circuit, resulting in a more precise measurement compared to the COTS solution, as can be seen in Figure. 4.12(a).

Figure. 4.12(c)-(d) illustrate the DUT's voltage and current slew rate performance, respectively, highlighting the effect of the measurement circuit on the DUT's switching behavior. The experiments were conducted under three conditions: without any measurement circuit, with the proposed measurement circuit, and with the COTS measurement circuit. The results indicate that the proposed circuit has minimal to no loading impact on the DUT, whereas the COTS measurement circuit exhibits a higher impact on the DUT's switching performance. Figure. 4.12(e) compares the measurement speed of the proposed circuit with that of the COTS circuit, which was operated in the 12 V clipping range due to the DUT current and the transient current peaks exceeding the limits of the 2 V setting. The proposed solution operates at a clipping setting of 4 V, allowing for much higher resolution for higher current levels and potential transient peaks, while achieving a settling time that is at least

40 ns faster than the COTS circuit. The gate resistance value, R_g, was varied from 5 Ω to 15 Ω to adjust the turn-on speed, allowing for an evaluation of the measurement circuit's performance across different DUT switching speeds.

By employing a cascode current mirror configuration and a clipping circuit for high-resolution measurements during the ON-state, the proposed approach effectively addresses key challenges such as measurement accuracy, resolution, and response speed. The circuit was validated both statically and dynamically across a wide range of operating conditions, demonstrating higher resolution performance in comparison to Commercial Off-The-Shelf (COTS) solutions, as well as reduced voltage overshoot and undershoot, minimal loading effects, and high precision. Due to minimal loading impact, integration of the circuit into high-voltage conversion systems can be achieved without degrading the system or the device's switching performance, making it suitable for in-situ health monitoring of WBG semiconductors.

However, the limitations of the proposed circuit include a higher parts count compared to the topologies described in Figure. 4.1(a)-(d), as well as the need for careful selection and tuning of the current mirror configuration. Moreover, there is a potential performance degradation due to variations in the characteristics of the diodes and BJTs. It's important to note that mitigation strategies have been introduced and discussed extensively to address these challenges.

The overall circuit performance can be highlighted for its potential applications in monitoring device degradation and predicting failure, which can provide significant benefits for enhancing the reliability and longevity of semiconductor devices in power electronics. Moreover, real-time monitoring of on-resistance can serve as an indicator of the state of health of WBG devices and as a diagnostic precursor to device aging and failure.

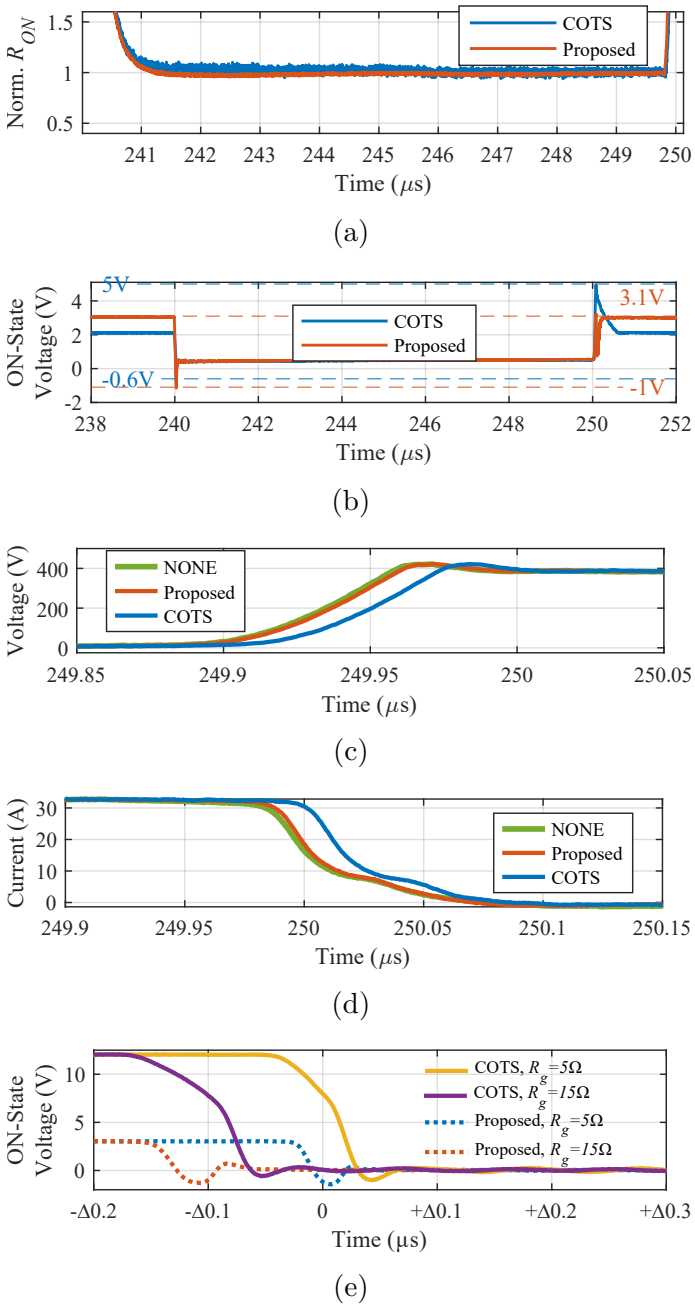


Figure 4.12: Experimental comparison of the proposed measurement circuit against a commercial off-the-shelf (COTS) solution, showing: (a) measurement accuracy and resolution, (b) minimum and maximum measured voltage peaks, (c) impact on voltage slew rate during turn-OFF, (d) impact on current slew rate during turn-OFF, and (e) ON-state voltage settling behavior across different gate resistances R_g.

4.2 Screening and Inspection Analysis Based on Device Electrical Characteristics

This section introduces the quantification and inspection analysis of part-to-part electrical variability in semiconductor devices and its impact on converter performance. WBG devices are susceptible to part variability due to complex fabrication processes and material-level inconsistencies, which can lead to significant deviations in conduction loss, switching behavior, and system-level integration inconsistencies.

Subsection 4.2.1 presents a statistical analysis of over 120 high-voltage WBG transistors sourced from multiple suppliers, showing measurable variation in both static and dynamic electrical characteristics. These device-level variations are incorporated into converter simulations through an automated model generation and evaluation process, illustrating the impact on efficiency and worst-case performance outcomes under realistic component selection scenarios.

Subsection 4.2.2 introduces a non-destructive inspection methodology based on small-signal gate excitation and unsupervised machine learning to identify representative devices from a broader population. Principal component analysis (PCA) is applied to reduce the dimensionality of extracted waveform features, followed by K-means clustering to group devices based on electrical similarity. This data-driven screening process allows the selection of devices that closely reflect population-mean behavior without subjecting them to stress or degradation, supporting robust converter design in the presence of manufacturing-induced variability.

4.2.1 Impact of Part Variability on Converter Performance

The recent adoption of WBG semiconductor materials has highlighted the importance of quality assurance, managing part-to-part variability in advanced, mission-critical power electronic systems. WBG materials present unique variability challenges due to specialized fabrication requirements. Small discrepancies in fabrication parameters such as channel thickness and defect density can influence carrier mobility and switching dynamics [278], potentially leading to substantial deviations in the electrical performance, such as efficiency, and reliability of converters, particularly under varied operating conditions.

Therefore, a methodology is presented that incorporates extensive experimental device characterization data into converter models in simulation through an automated process of compact model generation that accurately represents manufacturing variability. This approach utilizes empirical data from thorough device characterization processes to capture and quantify manufacturing-induced variations in both static and dynamic device characteristics. By converting all device data into XML-formatted models, the methodology enables comprehensive performance by sweeping across all characterized devices when integrated into a converter, which provides a realistic predictive performance range rather than idealized, fixed values. This holistic modeling approach can result in a more accurate representation of converter performance, effectively accounting for real-world manufacturing variability across diverse operating scenarios.

Part-to-part variation is an inherent aspect of the manufacturing process, making it essential to quantify the range of variation to assess its severity and potential impact on converter performance. In this study, over 120 high-voltage WBG field-effect transistors (FETs) have been characterized and the experiment results show clear variation observed in nominally identical devices. The remainder of this section describes a comprehensive analysis of both

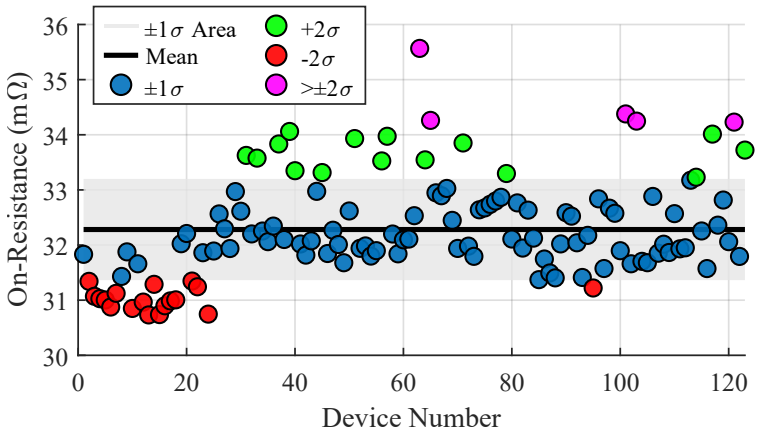
static and dynamic device characteristics through detailed characterization studies.

From the output characteristic of $V_g = 10$ V, Figure. 4.13(a) was generated and it shows the ON-resistance across a population of over 120 high-voltage WBG field-effect transistors (FETs). The population mean of ON-resistance is indicated by a solid line, with the shaded region corresponding to ± 1 standard deviation ($\pm 1\sigma$) shown to highlight the extent of deviation within the device population.

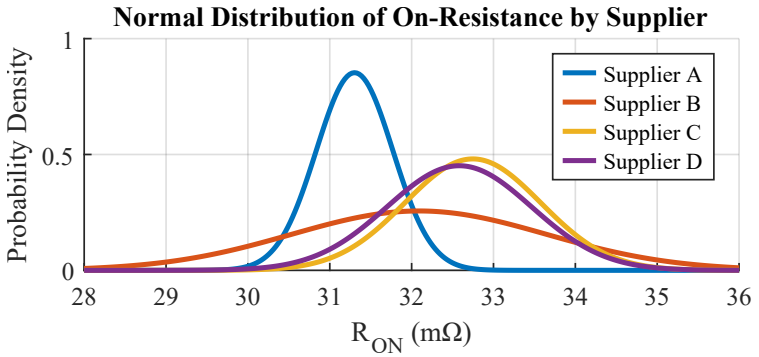
Expanding the analysis to include lot-to-lot variability, Figure. 4.13(b) presents the probability density functions (PDFs) of ON-resistance within the device population, which consists of components from four different suppliers (denoted A, B, C, and D to maintain anonymity). While the mean ON-resistance for each supplier remains within a narrow range (31 to 33 mΩ), the standard deviation varies from 0.46 mΩ to 1.56 mΩ, indicating considerable variability and differences in manufacturing consistency among suppliers.

The measured static and analyzed dynamic data can be incorporated into device simulation models, such as Simulation Program with Integrated Circuit Emphasis (SPICE) models or look-up table-based models, to examine the impact of variability on converter operation, with device models embedding both part-to-part and lot-to-lot variability. This approach enables more comprehensive predictions of power loss and thermal behavior under diverse operating conditions.

Using the static device measurement data and analyzed dynamic characteristic data, simulation models are developed to evaluate the impact of device variability on converter performance metrics, especially converter efficiency. Figure. 4.14 visually depicts the overall integration process. In this workflow, the measurement data for each device (D_i) is imported into a function, f_1, which represents static measurement data. This function is called to generate dynamic switching loss information, which gets stored in f_2. Subsequently, f_3



(a)



(b)

Figure 4.13: On-resistance measurements of the device population, illustrated with the population mean represented by a solid line and the shaded region indicating ±1 standard deviation (σ). The color scheme indicates whether the data points fall within $\pm 1\sigma$, $+2\sigma$, -2σ or greater than or equal to $\pm 2\sigma$ and (b) Probability density functions of ON-resistance measurements from four different suppliers, illustrating distinct means and standard deviations across vendors.

integrates device models from both f_1 and f_2 to calculate converter performance metrics, with efficiency as the primary focus. When multiple devices are required, a random selection is made from the device population using (4.21), reflecting real-world practices of randomly selecting devices from a production batch to ensure a fair representativeness of part-to-part variability.

$$\{S_i\}_{i=1}^{n} = \sum_{i=1}^{n} D_{j(i)} \quad \text{where } j(i) \sim \text{Uniform}(1, m) \tag{4.21}$$

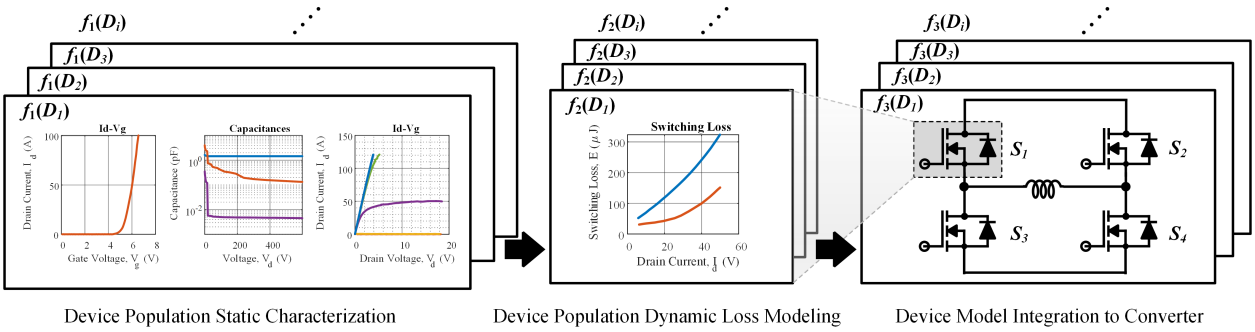


Figure 4.14: Proposed process for evaluating the impact of device part variability on converter performance, based on device models developed from measured static and dynamic characteristics of the device population.

where $\{S_i\}_{i=1}^{n}$ represents the set of all switches in the converter, $D_{j(i)}$ is the device randomly assigned to the i-th switch, $j(i)$ is an index selected from a uniform distribution over $\{1, 2, \ldots, m\}$, m is the total number of devices in the population, and n is the total number of switches.

Figure. 4.15 presents simulation results for the efficiency of a buck converter, obtained by iteratively integrating individual device models into the converter model. The figure shows the mean efficiency and the min-max range across the full power range. Due to variations in device characteristics, the min-max efficiency envelope exhibits notable patterns, with the efficiency spread widening as power levels increase. For instance, around 25 kW, the min-max efficiency range spans more than 3%, which is resulted from the influence of higher loss devices affecting the converter efficiency. This trend of increasing discrepancy in the min-max range with rising power levels is primarily due to greater part-to-part variability in losses at higher currents. This results in an expanded min-max efficiency range at higher power levels compared to lower power levels, where the energy loss between parts is approximately $\Delta 20\%$ from the mean.

Nevertheless, the mean efficiency closely follows the maximum efficiency curve, indicating that a small subset of devices with higher losses significantly contributes to the formation

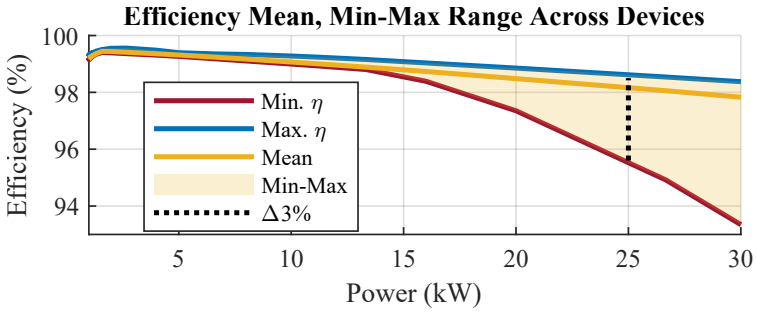


Figure 4.15: Converter efficiency across varying power levels, showing mean and min–max ranges derived from conduction and switching losses over the device population. The shaded band reflects the full efficiency spread, while the solid curve represents the average. A vertical marker indicates a 3% efficiency delta, emphasizing the performance impact of device selection.

of the minimum efficiency curve. It is essential to recognize that, due to randomness and device variability within the population, a randomly selected device may result in lower-than-expected efficiency as illustrated in Figure. 4.15. Therefore, if a converter population yields higher or lower efficiency than anticipated, part-to-part variability should be considered a potential contributing factor to these deviations.

In short, this analysis highlights the impact of device part variability on converter efficiency, highlighting the importance of accounting for such variability when designing and simulating converter performance. By capturing a realistic range of device behavior, the model provides information in regards to efficiency expectations and worst-case scenarios, allowing for more robust converter design and performance forecasting.

4.2.2 Non-Destructive Inspection Technique using Machine Learning

To establish a methodology that ensures a selection of devices representing the true population mean within an appropriate confidence interval (CI) without running the risk of damaging or stressing the material characteristics, an enhanced screening approach with

a non-intrusive perturbation signal is proposed. This method correlates the measurement outputs to the bulk effects of the transistors, such as the transfer, output, and capacitance characteristics, through machine learning (ML).

The electrical characteristic measurements of the GaN transistor samples exhibit varying degrees of part-to-part variability across key test parameters. Performing these measurements poses several challenges; they are not only resource- and time-intensive, but also prone to inducing degradation, as the devices must be biased at or above their rated voltage and current to evaluate margin requirements and safe operating limits. Moreover, in-situ monitoring of device state-of-health—such as degradation during operation—can be difficult due to system downtime, maintenance costs, and risks of damaging auxiliary components connected to the transistor.

To address these challenges, a simple small-signal injection method, as shown in Figure. 4.16(a), is proposed to correlate the gate response with the bulk electrical characteristics of the population. Inspired by the power spectrum analysis approach [311], fixed V_g ON-OFF gate signals of 0–5 V are applied with varying switching frequencies (f_s) of 10 kHz, 50 kHz, 100 kHz, and 500 kHz. The gate current is limited such that the devices do not fully switch ON or OFF, thereby allowing extraction of information related to the device and packaging parasitic network, as illustrated in Figure. 4.16(b).

Figure. 4.17 shows the excitation response output signal measured at the gate-source terminals for every GaN sample in the time domain. Upon analyzing the waveforms between samples, the overshoot, settling time, steady-state response, and switching on-off transitions are subtle in differences, which makes the part-to-part evaluation comparison difficult for the devices' electrical performance in both static and dynamic characteristics. Note that only 10 kHz output signals are shown in Figure. 4.17.

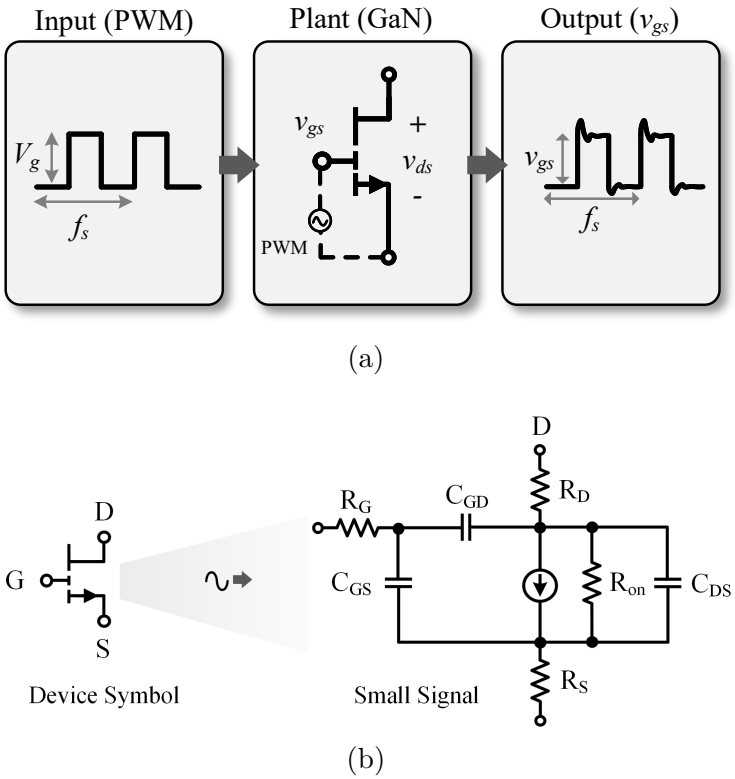


Figure 4.16: The non-destructive test methodology describing: (a) small signal excitation injection and the output signal measurement across the gate-source terminals on the GaN device and (b) illustration of the device small signal model with parasitic elements in the device, contributing to higher order effects.

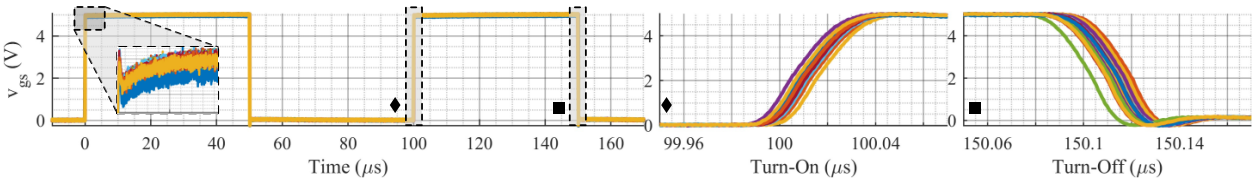


Figure 4.17: The gate-source output voltage signals of all GaN samples with the switching frequency of 10 kHz, illustrated in time domain. There are subtle changes from part-to-part in terms of the high and low voltage levels at steady-state as well as the turn-ON and turn-OFF switching transitions, which the appropriate intervals are denoted by '♦' and '■', respectively. However, it is difficult to relate the small signal excitation response signals to the transistor electrical specifications and characteristics.

To process the time-series feature of the dataset to numerical data type, the sample time-series mean across the entire measurement period, which is denoted as $\tilde{x}$, was calculated for each frequency test condition for each GaN device. Then the euclidean distance to the

sample population measurement mean, $d\ |_{\tilde{x}}$, was determined across the measurement size. The mean euclidean distance, expressed in (4.22), was calculated for each GaN device sample.

$$d\ |_{\tilde{x}} = \sqrt{\sum_{i=1}^{m}(x_i - \tilde{x}_i)^2} \tag{4.22}$$

The Euclidean distance data was also further processed through the min-max normalization scaling to perform a linear transformation of between the datasets. However, with several dimensions of the dataset, it can be difficult to down select the features that provide the most effective and representative characteristics of the sample population, especially when the coefficient of determination (R2) score is not very distinctive between the features. Therefore, the principal component analysis (PCA) algorithm was used for dimensional reduction between the feature dimensions. The PCA minimizes the mean squared distance between the dataset and the projected hyperplanes with the maximum variance. Such a transformation allows reduction of dimensional to d dimensions, defined by the first d principal components [312, 313]. The first two principal components were used to project the dataset to the 2D plane while preserving a large part of the dataset's variance. Table 4.3 shows a summary of the post-processed Euclidean distance on the GaN sample population along with the first two PCA components. Note that only the data of the first 10 samples are shown.

The main objective of the proposed inspection technique is to extract key electrical specifications using a non-intrusive small excitation signal, without requiring labeled data for the device samples. In the absence of prior knowledge or a representative dataset, identifying groups with similar electrical behaviors is essential. To enable this, an unsupervised clustering technique is employed to group data points based on similar features [314]. The K-Means algorithm [315] is used to train and cluster the data samples from a d-dimensional dataset derived through principal component analysis (PCA).

To determine the optimal number of clusters k, the Elbow Method [316] is applied. This technique helps identify the appropriate number of centroids for the K-Means algorithm by analyzing the sum of squared error (SSE) which quantifies the total variance within each cluster. The optimal number of clusters corresponds to the point where adding more centroids results in a diminishing return in inertia reduction, forming an inflection or "elbow" in the plot. Figure. 4.18(a) shows the elbow plot of varying cluster sizes and their respective SSE values. Based on this analysis, the optimal number of clusters is selected as $k = 2$. Figure. 4.18(b) illustrates the resulting clustering on a 2D projection of the first two principal components, clearly showing two distinct cluster groups: Cluster 0 (CL.0) and Cluster 1 (CL.1), each centered around their respective centroids.

With the dataset partitioned into two clusters, further analysis is performed to evaluate how closely each cluster's mean electrical characteristics align with the overall device population. Figure. 4.19(a) shows the output characteristics of each cluster at $V_{\mathrm{GS}} = 2$ V compared to the sample population mean and its 90% confidence interval (CI). The average characteristics of CL.0 are observed to be closer to the population mean than those of CL.1. Furthermore,

Table 4.3: Summary of Euclidean distances of V_{gs} output response at different excitation frequencies, along with principal component projections.

ID	**10 kHz**	**50 kHz**	**100 kHz**	**500 kHz**	**PCA1**	**PCA2**
1	3.578	1.141	0.693	0.394	−0.123	−0.088
2	2.600	1.193	0.882	0.427	−0.276	0.047
3	2.819	1.187	0.697	0.430	−0.209	−0.234
4	2.589	1.078	0.720	0.377	−0.320	−0.015
5	2.976	1.212	0.798	0.366	−0.214	−0.007
6	2.714	1.161	0.825	0.337	−0.303	0.098
7	3.163	1.220	0.759	0.363	−0.176	−0.082
8	2.795	1.224	0.724	0.459	−0.165	−0.276
9	3.904	1.112	0.807	0.384	−0.088	0.163
10	3.878	1.189	0.757	0.345	−0.089	0.044
⋮	⋮	⋮	⋮	⋮	⋮	⋮

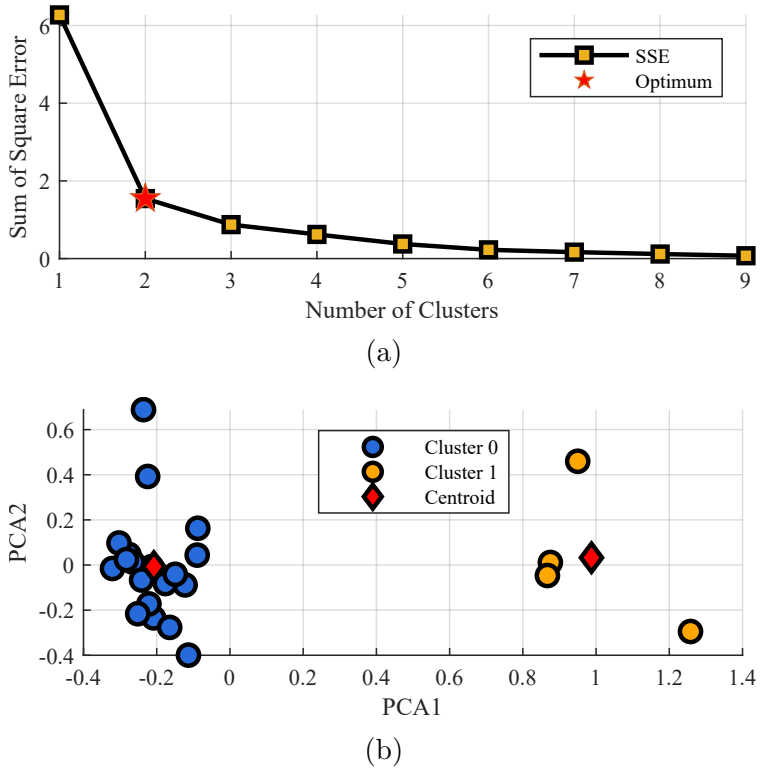


Figure 4.18: K-means clustering results based on: (a) selection of the optimum number of clusters at the inflexion point from the elbow plot and (b) the clustering results with k=2 along the PCA1 and PCA2 dimensions.

CL.0 samples remain within the 95% CI of the population. This trend is reaffirmed in Figure. 4.19(b), which also shows that CL.0 has a smaller Euclidean distance to the population mean while maintaining 95% CI bounds.

Figure. 4.19(c) presents the transfer characteristics, comparing the mean responses of both clusters to the full dataset. Again, the CL.0 mean closely tracks the overall population behavior. Figure. 4.19(d) illustrates the input capacitance characteristics, where the CL.0 mean also demonstrates a smaller deviation from the population mean compared to CL.1.

The root mean squared error (RMSE) is used as a quantitative metric to evaluate the deviation of each cluster's average response from the true population mean. For all test conditions, the RMSE or Cluster 0 is smaller than Cluster 1. Therefore, a proper selection of representa-

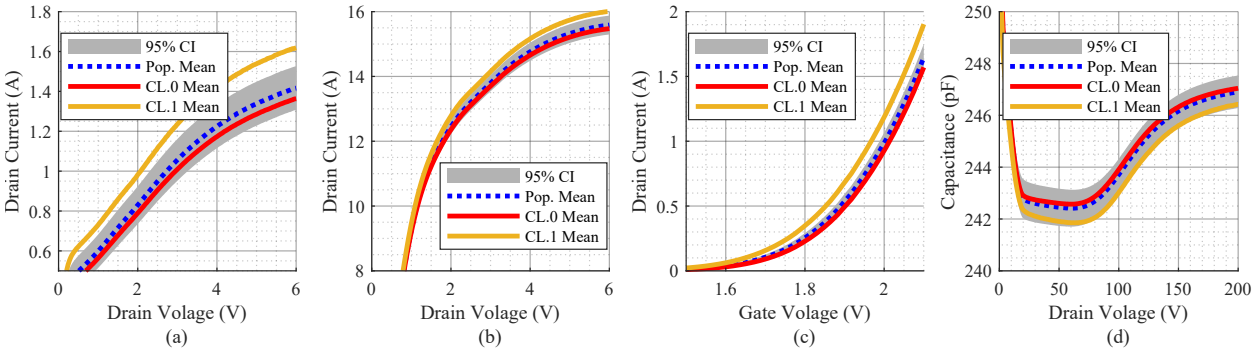


Figure 4.19: The comparison of the sample mean of Cluster 0 (CL.0) and Cluster 1 (CL.1) to the population mean with 90% CI for: (a) output characteristic @ V_{gs}=2V, (b) output characteristic @ V_{gs}=3V, (c) transfer characteristic, and (d) input capacitance characteristic, C_{iss}.

tive sample population to the true population mean in regards to the electrical specifications can be accomplished by the proposed characterization and the derived cluster model. However, it is important to accompany the method with other statistical and machine learning models to ensure and validate the effectiveness of the model while assessing overfitting. It is important to correlate the clusters to reliability or circuit performance.

4.3 Automated Test System for WBG Dynamic Reliability Evaluation

Implementing an automated testbed capable of enabling repeatable, safety-driven, long-duration dynamic reliability assessments of WBG power devices and their integrated systems under harsh switching stress conditions presents significant challenges. Such a system requires seamless integration between software and hardware to ensure coordinated control and command execution. Given the intrinsic characteristics of WBG devices, the test platform requires a capability to support high-voltage and high-power operation while maintaining robust safety protection mechanisms. Furthermore, to accurately assess long-term reliability,

the system must provide precise control, high-resolution data acquisition, long-term data storage, and dynamic environmental condition management throughout accelerated stress testing.

Subsection 4.3.1 outlines the software architecture and control framework developed to manage automated test operations. The platform incorporates several core components, including the user interface loop, supervisory loop, scheduler loop, global error handler, polling loop, and data display/processing loop, which together enable seamless configuration of test parameters, control of the power stage, and automation of test sequences for extended-duration experiments. The software's key functionalities include scheduling multiple-pulse stress patterns, real-time monitoring of switching waveforms, automated data logging, fault detection, and safe system shutdown protocols. The software was designed with scalability and adaptability, allowing accommodation of different device types, test conditions, and reliability standards.

Subsection 4.3.2 presents the schematic diagrams, instrumentation connection layouts, emergency operation procedures, and the configuration of the fully assembled test racks. The hardware platform includes the high-voltage, high-speed switching testbed; measurement instrumentation for capturing high-bandwidth switching waveforms; safety interlocks; and thermal management subsystems. The physical integration of various components, which encompasses cabling, grounding, safety feature implementation, and ergonomic considerations, is documented as it is a critical step in ensuring the safe and reliable operation of the test system.

4.3.1 Software Architecture Development

The software architecture is designed as a series of parallel modules to ensure modularity, self-containment, and interoperability throughout program execution. This modular approach prevents subsystem dependencies from influencing execution speed, error reporting, and error handling. A hierarchical structure manages the system software and communication paths to prevent from conflicting instructions. For reliable, robust, and efficient test execution, each software module maintains a defined and isolated role, minimizing interference and conflict between tasks.

Figure. 4.20 provides an overview of the software architecture, illustrating the hierarchy and data flow between software subsystems. What is integral to the architecture is the Supervisor Loop, which only receives instructions from the User Interface (UI) and the Global Error Handler. All subsystems report errors to the Global Error Handler, which immediately notifies the Supervisor Loop for fault management.

The UI Event Handler remains idle except when retrieving UI events such as front panel button presses. Upon event detection, it offloads these events to the Supervisor Loop for immediate processing. The UI Event Handler is void of logic or processing capabilities, functioning strictly as an event intermediary.

The Polling Loop manages low-bandwidth periodic tasks, including updating system clocks, test timers, monitoring error events, and maintaining system-level indicators. It handles these benign tasks without decision-making responsibilities, minimizing its system impact.

Global System Status information is stored and maintained to track overall software state, such as Idle, Running, or System Fault/Error conditions. Subsystems utilize these global parameters to adapt their operational states. For example, the Data Loop, programmed for periodic logging during the Running state, remains inactive during Idle and resumes logging

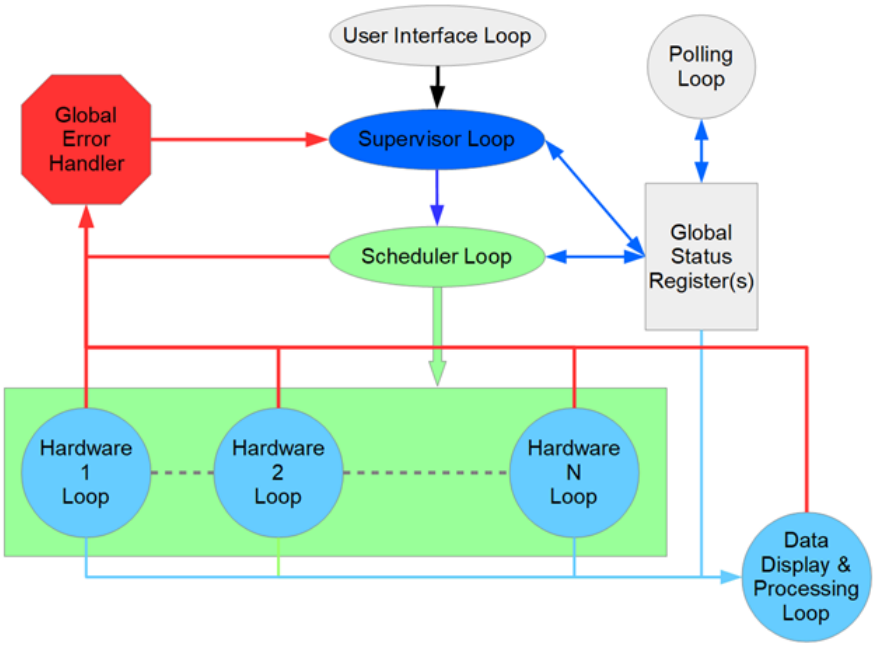


Figure 4.20: Automated test system software architecture overview

upon state transition.

The Supervisor Loop directs the Scheduler Loop, which coordinates all Hardware Loops and manages test sequencing. Data generated by the Hardware Loops is processed by the Data Display and Processing Loop. It also contains the system's logic. Designed for idle status except when actively directing subsystem processes, it handles incoming UI and error events to maintain system integrity.

Dialog boxes, which create blocking conditions, are initiated by the Supervisor Loop and only when the system and hardware are idle. The architecture mandates that dialog boxes or UI events should not impede the Supervisor Loop's responsiveness. Therefore, actions such as launching an Instrument Configuration Panel or pressing an Exit button are conditionally permitted, based on system state.

System-level decision-making, including capturing and distributing configuration information for instruments and test scheduling, is mainly managed by the Supervisor Loop. Con-

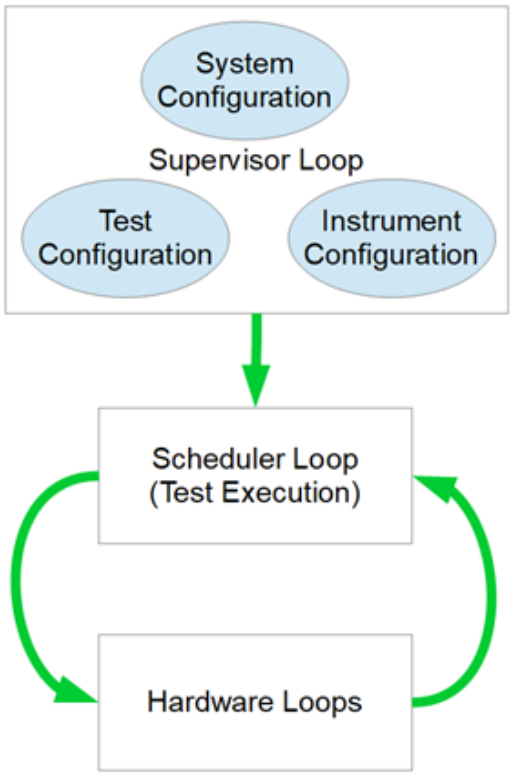


Figure 4.21: Automated test system software workflow diagram

figuration data is communicated via a Queued Message Handler to respective subsystem loops. As demonstrated in Figure. 4.21, system configuration occurs during the Idle state, ensuring readiness prior to test initiation. Captured configuration data, whether entered through configuration panels, front panel controls, or other interfaces, is organized into modular clusters or structures, facilitating efficient retrieval and usage throughout software operations.

The Scheduler manages test scheduling, timing, execution, and instrument interactions. Upon receiving the instrument and test configurations from the Supervisor, the Scheduler remains idle until activated to execute scheduled test events. Once the operator initiates a test, the Scheduler activates, leveraging the provided configurations to execute predefined test scripts.

While the Supervisor serves as the central coordinator for overall system activities, the Scheduler operates as an intermediate manager, mainly dedicated to performing configured test tasks. During test execution, the Scheduler takes full responsibility for test-related processes, allowing the Supervisor to remain idle and responsive only to user interactions (e.g., stop commands) or system error events. Upon test completion, whether by operator intervention or the successful conclusion of the test duration, the Scheduler concludes all activities, ensuring the system returns to an idle and stable state.

4.3.2 Hardware Design and Implementation

Physical development of the automated test system dedicated to evaluating degradation and reliability of WBG power semiconductors is a challenging task. The system needs to be designed to be highly modular, customizable, and adaptable to conduct high-frequency, high-voltage, high-power switching stress testing, while closely replicating demanding environments for power converter applications. Moreover, robust safety hardware measures should guarantee secure test operations, even under the most hazardous conditions.

The electrical diagram of the test system integration is illustrated in Figure. 4.22. Two modular 42U server racks are employed to house the majority of test equipment. One rack contains low-voltage, non-hazardous instrumentation, while the other is dedicated to high-voltage, stored-energy elements. This separation enhances operational safety and simplifies maintenance procedures. The rack infrastructure is carefully designed to manage airflow optimization, and cable management provisions for low-noise signal paths. Power distribution units (PDUs) are configured to accommodate the varying voltage and current requirements of different subsystems, including a 208 V/30 A PDU for the line-voltage instruments and a custom 480 V/100 A PDU for high-power sources and loads. An uninterruptible power

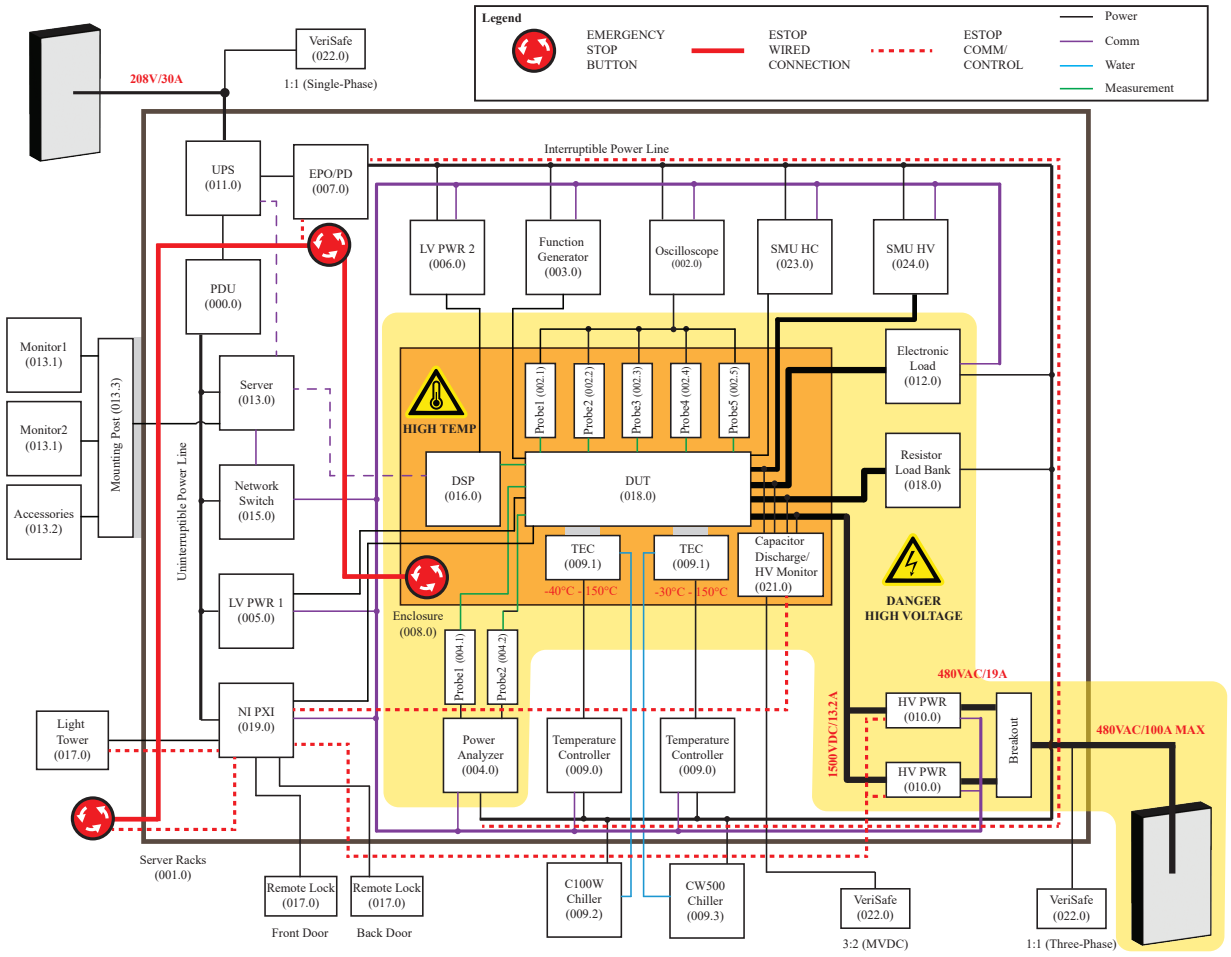


Figure 4.22: Automated test system electrical diagram, detailing connections between instruments

supply (UPS) provides backup power to maintain operational continuity and data integrity during grid disturbances.

High-bandwidth measurement capability is provided by digitizers, such as mixed-signal oscilloscope, equipped with a comprehensive set of high-voltage, high-current, and general-purpose probes. This configuration enables accurate capture of sub-nanosecond switching transients critical for characterizing WBG device dynamics. A function generator is used for precision gate drive or auxiliary stimulus generation, while a multi-channel, high-accuracy power analyzer allows real-time measurement of conversion efficiency, power quality, and

losses driven by the magnetic and semiconductor operation.

The power delivery architecture includes programmable low-voltage power supplies for control and bias circuits, and high-voltage programmable DC sources, delivering up to 40 kW total output power for stressing the system or devices under specified converter-level voltages and currents. A programmable electronic load supports dynamic load profiles to replicate application-specific duty cycles.

Thermal control for the Device-Under-Test (DUT) is achieved using precision temperature controllers complemented with thermoelectric chucks and liquid chillers. This arrangement allows fine regulation of device junction and case temperatures over a wide range, enabling controlled thermal cycling and accelerated aging tests that reproduce thermo-mechanical stress conditions.

System control and automation are implemented using FPGA-based real-time controllers for the execution of test sequences. Multifunction I/O modules are integrated for signal acquisition and thermal monitoring. A data acquisition unit supports both slow and high-speed logging requirements. A dedicated control server hosts the automation software, enabling remote operation, experiment scheduling, and real-time monitoring.

All instruments and control modules are networked via managed Ethernet switches to ensure high-speed data transfer, precise synchronization between measurement channels, and secure remote accessibility.

Lastly, the incorporation of essential safety features into the automated test system is essential to ensure safe operation during all test procedures and to effectively mitigate potential risks and hazards. Safety is maintained through an emergency power-off and power distribution system, safety light towers, remote access locks, absence-of-voltage verification devices, and a dedicated capacitor discharge circuit. The safety sensing with VeriSafe devices is im-

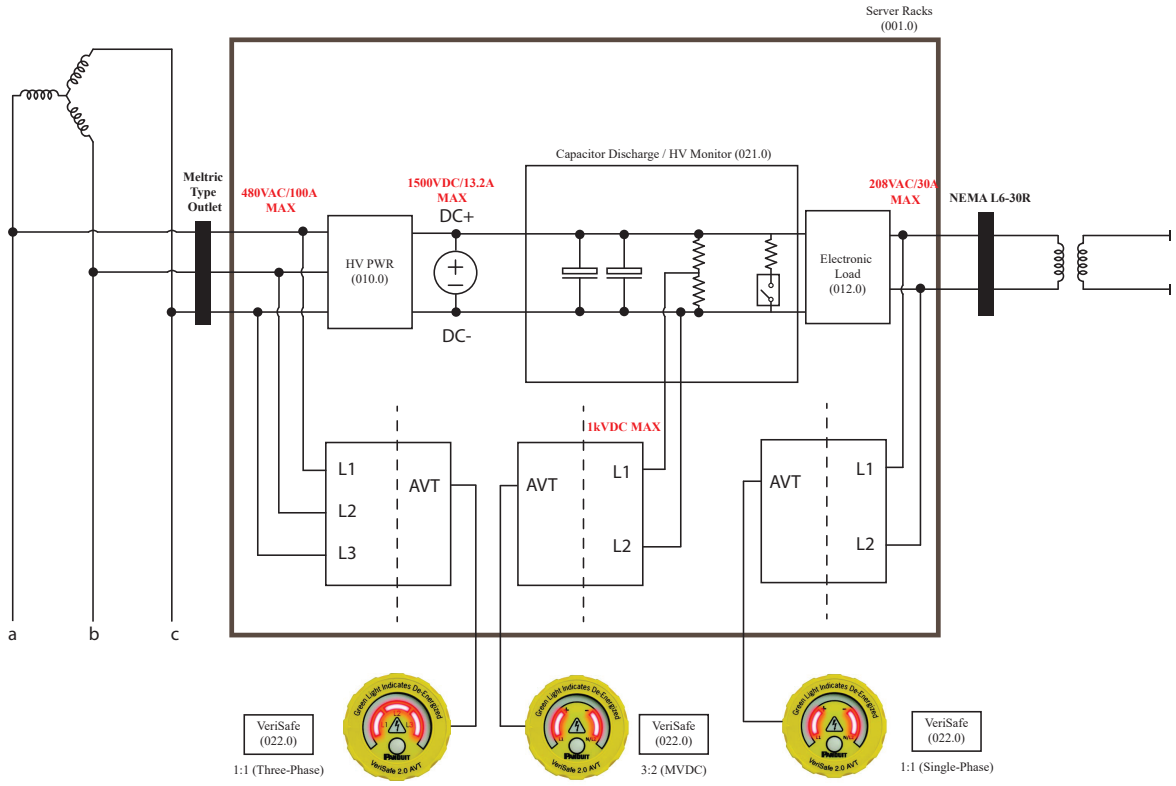


Figure 4.23: Safety sensors to verify absence of energy prior to opening an electrical enclosure

plemented across all energy sources, including 208 V/30 A, 480 V/100 A, 1500 V/13.2 A supplies, and capacitor-based stored energy as illustrated in Figure. 4.23. This ensures that hazardous voltages and residual energy are fully dissipated prior to operator access. In addition, the rack enclosure provides physical isolation of high-voltage nodes, and all hardware interlocks meet or exceed relevant industrial safety standards.

Figure 4.24 presents the fully assembled automated test racks developed for dynamic reliability evaluation of WBG power devices. The configuration integrates high-voltage and low-voltage instrumentation, programmable power sources, precision measurement equipment,



Figure 4.24: Fully assembled automated test racks for WBG dynamic reliability evaluation

thermal management subsystems, and safety interlocks within two modular 42U enclosures. The physical layout provides a compact, organized, and application-representative platform for executing accelerated stress tests under controlled electrical and thermal environments.

4.4 Summary

This chapter presented a suite of advanced characterization techniques, qualification methodologies, and testing capabilities designed to address the measurement accuracy, screening

robustness, and dynamic reliability assessment requirements for WBG device integration.

Section 4.1 detailed a novel cascode current-mirror–based OVMC developed to overcome the resolution and dynamic range limitations of conventional sensing approaches under high-voltage, fast-switching operation. The proposed topology enables precise and accurate extraction of on-resistance by clipping off the off-state waveform while preserving high vertical resolution during the conduction interval. This technique mitigates the oscilloscope amplifier saturation and ADC quantization effects.

Section 4.2 introduced a non-destructive inspection and screening methodology for quantifying and managing part-to-part variability in GaN HEMTs without inducing material degradation or requiring destructive testing. Statistical evaluation of a large device population showed measurable electrical dispersion in static and dynamic parameters, which showed greater than 3% system-level efficiency deviation through converter-level simulations. Leveraging small-signal gate excitation, principal component analysis (PCA), and K-means clustering, the non-destructive screening method enabled rapid identification of population-representative devices for device characteristic cluster identification.

Section 4.3 described the design and deployment of a fully automated, high-voltage dynamic reliability test platform. The system integrates modular hardware and software control loops to execute long-duration, switching-based stress profiles with real-time monitoring, automated fault handling, and safety interlocks. Its architecture supports flexible adaptation to various device types and stress profiles while inducing environments for accelerated lifetime evaluation.

These techniques and testing capabilities establish a comprehensive framework for WBG device characterization, screening, and qualification under dynamic operating stresses. By combining high-fidelity measurement, data-driven device selection, and automated long-term

reliability testing, the approaches developed in this chapter support more reliable, efficient, and application-ready deployment of WBG power semiconductors.

Chapter 5

Optimization and Lifetime Analysis for Power Electronic Systems

This chapter focuses on system-level co-design strategies that address the complex interdependencies among electrical, thermal, and reliability behaviors in WBG-based power electronic systems. In addition, it explores advanced lifetime analysis techniques, including real-time computation and machine learning, to assess and predict long-term device and system performance.

Section 5.1 introduces a multi-objective design optimization framework that integrates the unique characteristics of WBG devices into the converter-level design process. This framework enables simultaneous optimization of key performance metrics, such as conduction and switching losses, converter volume, thermal stress, and projected device lifetime, to support informed trade-off decisions.

Section 5.2 focuses on lifetime performance evaluation and predictive modeling. It presents methodologies to quantify long-term system reliability by leveraging physics-of-failure mechanisms and empirical stress-response data. The section utilizes a range of techniques, from real-time analytical models based on junction temperature and power cycling, to machine learning-based approaches that enable data-driven lifetime prediction.

5.1 Multi-Objective Optimization and Co-Design of Power Electronic Systems

This section presents multi-objective optimization and co-design methodologies for power electronic systems. Conventional design processes treat performance objectives and material properties independently from the converter operational conditions, potentially leading to suboptimal trade-offs when integrating WBG and UWBG devices. Therefore, developing integrated frameworks that capture the coupled relationships between material properties and converter behaviors is critical to enable informed design decisions that account for complex interdependencies.

Subsection 5.1.1 details the multi-objective optimization of an EV traction inverter between efficiency, converter volume, and lifetime reliability. This approach models the EV drivetrain as a multi-domain system comprising battery modules, traction inverter, motor, and transmission, with interactions ranging from electrical and thermal to mechanical domains. By integrating converter-level performance models with thermal stress and degradation models, the study identifies optimal operating parameters to achieve high efficiency, compact size, and long-term durability under dynamic driving profiles.

Subsection 5.1.2 focuses on co-design analysis of WBG and UWBG power diodes within representative operational regimes. The methodology evaluates device FOM in the context of future-looking high voltage converter applications. The study considers constraints such as switching frequency, blocking voltage, and current-handling capacity. A physics-based optimization engine selects drift region dimensions and doping concentrations to minimize total power dissipation while ensuring target breakdown voltage and conduction characteristics. This integrated device-to-converter evaluation enables material selection aligned with system-level performance objectives.

5.1.1 EV Traction Inverter for Efficiency, Volume, and Reliability

The EV drivetrain comprises several interconnected subsystems, including the battery modules, traction inverter, electric motor, and mechanical transmission. As illustrated in Figure. 2.7, these components form a coupled multi-domain system, where electrical, mechanical, and thermal dynamics interact to influence overall performance.

The electric motor produces power and drives the wheels by applying torque on the rotor through the rotor shaft. The rotor shaft connects the wheel axle through the transmission components, including a single-speed gearbox. Each drivetrain sub-system has been modeled with appropriate physical parameters to ensure high-fidelity characteristics of an EV drivetrain system.

There are several motor types that are used in EVs – synchronous motors like permanent-magnet motors and asynchronous or induction motors. In this EV model, a three-phase wye-connected permanent magnet synchronous machine (PMSM) is used. The motor parameters, including stator inductance, stator resistance, flux induced by magnets, number of pole pairs, inertia, friction coefficient, etc have been modeled based on approximated physical parameters of the Nissan Leaf electric vehicle motor [317].

Within the EV system, the traction inverter plays a critical role in converting DC voltage from the battery modules into three-phase AC signals for the electric motor [318]. The power electronic and control system for the traction inverter, represented in Figure. 5.1 illustrates an inverter model with a motor controller. The battery pack is modeled with an ideal DC voltage source. The battery voltage is set as a variable so that it can be changed to a desirable value during the optimization process. The battery is connected to a two-level voltage source inverter through a DC-link capacitor. The inverter model allows a selection of power modules of different material properties, such as Si-IGBT or SiC with user-specified

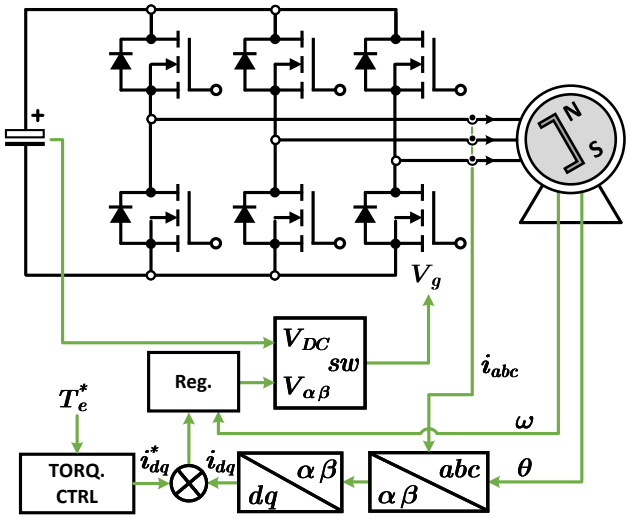


Figure 5.1: EV drivetrain power electronics and control system model.

or manufacturer provided loss characteristics.

A field-oriented current controller is used to implement a closed-loop feedback control of torque demand as current setpoints in the rotor reference frame through the digital synchronous frame regulator as described in [319]. A desired torque setpoint, which is the driving torque profile is converted to the current setpoints in the dq reference frame (i_{dq}^*) through a torque controller. The current setpoints along with the PMSM stator currents, $i_{\alpha\beta}$, PMSM rotor position or mechanical angle (θ), rotor mechanical speed (ω_s), and the battery voltage (V_{bat}) are measured for the regulator to generate appropriate voltage setpoints in the $\alpha\beta$ referance frame ($v_{\alpha\beta}^*$), which are converted into the gate switching signals (V_g) for the inverter power modules through a space-vector modulator (SVM).

Furthermore, the heatsink component is attached to the inverter model to provide a proper thermal management of the power modules. The thermal management system maintains a proper operating temperature range of the power module. The cold plate elements are modeled by utilizing a compact model of a Cauer based thermal impedance chain. The thermal network consists of multiple impedances of resistor-capacitor pairs to represent thermal inter-

faces of different material properties in the cold plate thermal management system. Such an electro-thermal model provide an accurate temperature rise profile based on the EV driving cycle that can be used to ensure the power module operation within the device safe operating area (SOA) as well as the reliability calculation based on power cycling experimental data of various materials.

The transmission transfers mechanical power from the motor to the wheels. This transmission model consists of a gearbox and the rotor shaft. The single-speed gearbox is modeled with two shafts rotating with a fixed gearbox ratio. The shaft dynamics are modeled with a linear spring characteristic ($\tau = -c \cdot \Delta\theta$) in a rotational system to represent the shaft stiffness as well as viscous friction of the shaft damping factor represented with a translational damper ($F = -D \cdot v$).

The rotor applies torque on the wheel axle and converts it to a traction force. The wheel axle model consists of both the front and rear wheels that are represented as a lumped rotational mass with fixed inertia and rotating wheel friction. The wheel rotational speed and the vehicular translational speed are calculated based on the radius of the wheel, mass, and initial rotational and translational speed [320]. The traction force is applied to the vehicle front wheels based on the normal force on axle and the measured vehicle and tire speed. Lastly, the tire slip is modelled based on a traction or longitudinal force using Pacejka's

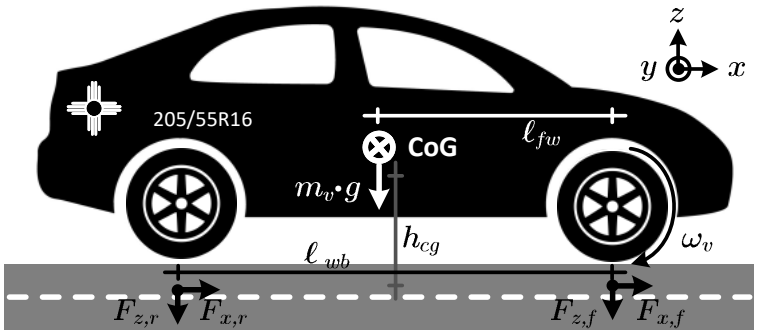


Figure 5.2: Vehicle dynamic and wheel model with physical parameters.

Magic Formula [321], expressed in (5.1):

$$F_x = D \cdot \sin(C \cdot \arctan(B \cdot \kappa - E(B \cdot \kappa - \arctan(B\kappa))) \tag{5.1}$$

where κ is the tire slip and B, C, D and E are Magic Formula dimensionless coefficients from semi empirical data. The vehicle dynamic parameters and appropriate physical variables of the wheel model are shown in Figure. 5.2.

The vehicle is commanded with a driving profile with a set torque demand curve. Figure. 5.3 shows the motor torque applied on the vehicular system over a duration of 60 seconds in driving time compared with the actual motor torque, motor speed, and vehicle speed, respectively. A sudden, yet constant torque demand set point of 200 Nm is applied from $t = 0$ to $t = 10$ seconds, accelerating the vehicle from a standstill. Starting from $t = 10$ to $t = 40$ seconds, the torque demand gradually and linearly decreases to 100 Nm and stays constant at 100 Nm from $t = 40$ to the end of the cycle at $t = 60$ seconds.

The vehicle speed is defined as accelerating from $t = 0$ to $t = 30$ until it reaches its top speed of 48 miles per hour (mph). The vehicle is considered cruising for 10 seconds between $t = 30$ to $t = 40$ seconds with more or less the same speed. Then the vehicle begins to decelerate from $t = 40$ to $t = 60$ seconds. These driving condition categories are properly annotated as *accel, decel*, and *cruise* in Figure. 5.3. These categories are paramount when determining the weighted averages of the inverter efficiency and reliability as higher stresses are expected during the acceleration phase and therefore, the impact in each time interval should be factored in with proper weights. Table 5.1 provides a summary of the EV system model with physical design parameters used to build and simulate the EV model.

The required DC-link capacitance is influenced by the inverter's operating conditions, particularly the output current, battery voltage, switching frequency, modulation index, and

Table 5.1: Electric Vehicle System Model Parameters

System	Parameter	Description	Value
Motor	R_s	Stator Resistance	5mΩ
	L_d L_q	Stator Inductance	260μH
	$\varphi^{'}$	Induced Magnetic Flux	0.05Wb
	p	Pole Pairs	4
	J_m	Combined Inertia	0.015 kg·m^2
Transmission	g	Gear Ratio	3
	c	Spring Constant	1636 Nm/rad
	D	Damper Constant	18 Nm/rad
Power Electronics	V_{bat}	Battery Voltage	400 V*
	f_{sw}	Switching Frequency	10 kHz*
	$R_{g,on}, R_{g,off}$	External Gate Turn-ON/OFF	2 Ω
	C_{Link}	DC-Link	3 mF
	PM	Power Module	CAB450M12XM3*
2-Axle Wheel	m_v	Vehicle Curb Weight	1543 kg
	ℓ_{wb}	Vehicle Wheelbase	2.7 m
	ℓ_{fw}	Front Wheel to Center of Gravity (CoG)	1.6 m
	h_{cg}	Vehicle Center of Gravity (CoG) Height	0.55 m
	$Tire$	Tire Size	205/55R16
	m_w	Tire/Wheel Weight	13.6 kg
	F_w	Wheel Friction	20 Nm
Driving Condition	F_{brk}	Breakaway Friction Force	10 N
	F_C	Coulomb Friction Force	10 N
	c_v	Viscous Road Load Coefficient	50 Ns/m
	P_d	Driving Profile	Figure. 5.3

*Sample nominal operation design value.

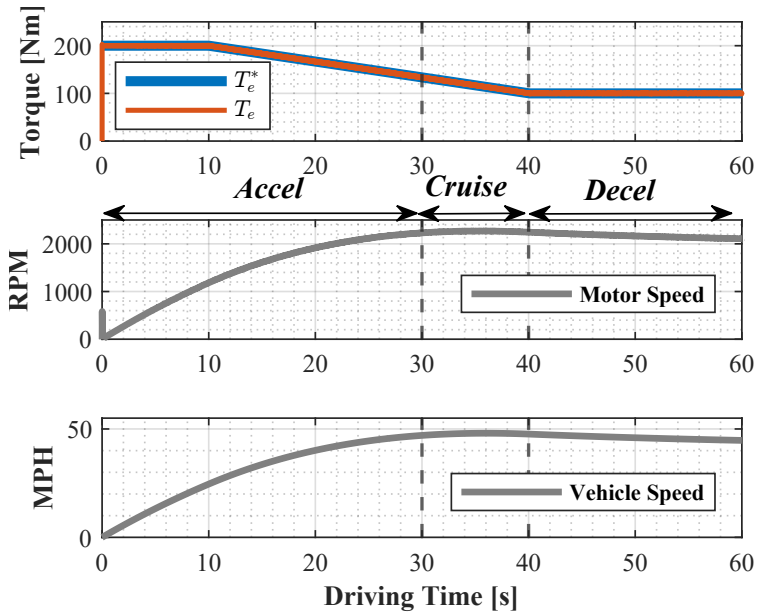


Figure 5.3: Driving profile shown as torque demand setpoint (T_e^*) compared to actual motor torque (T_e), motor speed, and vehicle speed along with the driving condition annotated for each time interval.

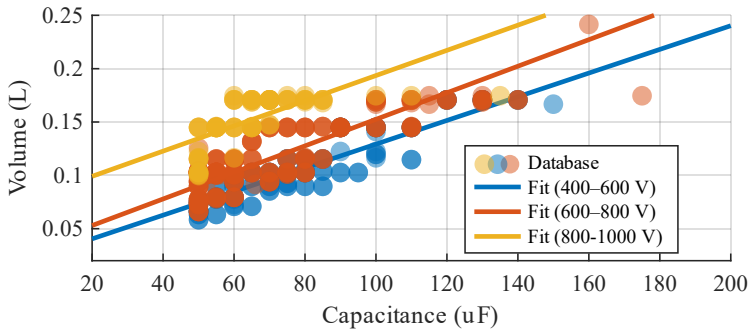
allowable DC bus ripple. The RMS current stress on the DC-link capacitor can be expressed in closed form as shown in (5.2), following the analytical derivation in [322]:

$$I_{\mathrm{c,rms}} = I_{\mathrm{n,rms}} \sqrt{2M \left(\frac{\sqrt{3}}{4\pi} + \cos^2 \phi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right)} \tag{5.2}$$

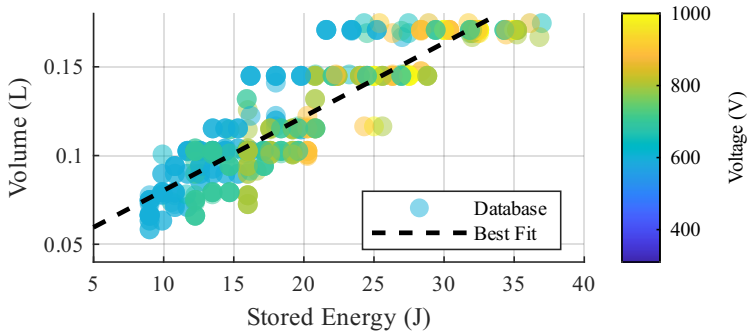
where $I_{\mathrm{n,rms}}$ is the RMS output phase current, M is the modulation index ($M = 2V/V_{\mathrm{dc}}$), and ϕ is the power factor angle. The modulation index is a function of the output voltage relative to the DC-link voltage and increases as battery voltage decreases.

The required or minimum DC-link capacitance to maintain a specified peak-to-peak ripple voltage ΔV_{dc} is approximated by the expression in (5.3).

$$C_{\mathrm{dc}} = \frac{I_{\mathrm{c,rms}}}{k \cdot f_{\mathrm{s}} \cdot \Delta V_{\mathrm{dc}}} \tag{5.3}$$



(a)



(b)

Figure 5.4: Scatter plots of commercial-off-the-shelf (COTS) film capacitors with linear regression fits, $y = \alpha x + \beta$, illustrating: (a) Volume vs. Capacitance categorized by voltage range and (b) Volume vs. Stored Energy, $E = \frac{1}{2}CV^2$.

where f_s is the inverter switching frequency, and k is a ripple coefficient dependent on the control method and power factor [323, 324].

To relate capacitance to physical volume constraints, an empirical analysis was conducted on a dataset of commercial-off-the-shelf (COTS) film capacitors. Capacitors were categorized based on rated voltage, capacitance, and package dimensions. Based on the exhaustive search, the linear regression curve fits ($y = \alpha x + \beta$) have been identified based on the relationship of capacitance and volume across different ranges of voltage ratings and between stored energy $E = \frac{1}{2}CV^2$ and volume. The scatter plots and resulting fits based on different ranges of voltage ratings and stored energy are shown in Figure. 5.4(a) and Figure. 5.4(b), respectively.

Table 5.2: Linear fit parameters for different capacitor voltage ranges.

Voltage Range (V)	$\boldsymbol{\alpha}$	$\boldsymbol{\beta}$	$\boldsymbol{R^2}$
400–600	1109.93	18269.77	0.81
600–800	1244.37	28076.75	0.84
800–1000	1180.84	75465.93	0.84
CV^2 (All)	0.0042	30.88	0.86

The regression coefficients for the three voltage ranges are provided in Table 5.2. These linear fit models are used to estimate the total volume of the capacitor given energy or capacitance-voltage requirements determined from inverter system-level design constraints.

The required heatsink volume is estimated by analyzing the thermal network of the power module and cold plate, represented using a lumped-parameter Cauer model, which is exhibited in Figure. 5.5(a). The thermal impedance from junction to ambient can be modeled for n stages as expressed in (5.4).

$$Z_\theta(s) = \sum_{i=1}^{n} \frac{R_i}{1 + sR_iC_i} \tag{5.4}$$

This gives the Laplace-domain transfer function relating power dissipation $P_d(s)$ to junction temperature $T_j(s)$, shown in (5.5).

$$T_j(s) = Z_\theta(s) \cdot P_d(s) \tag{5.5}$$

where P_d is the power dissipation of the device and T_a is the ambient or coolant temperature. For the state-space expressions and the resultant matrices are detailed in [325, 326].

To estimate heatsink volume and using similar approach to the capacitor sizing, a commercial database of COTS cold plates was analyzed. Thermal resistance values (Z_θ) were compared against physical volume and flow rate. The volume–resistance relationship was modeled

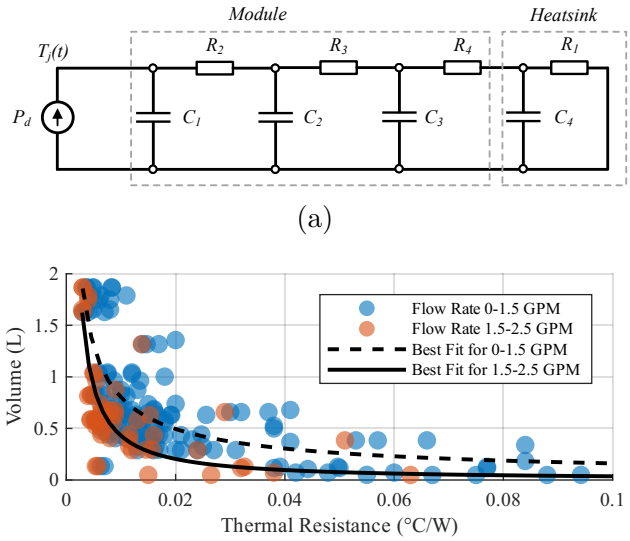


Figure 5.5: (a) Thermal model representation of power module and heatsink using Cauer network and (b) volume–thermal resistance correlation based on commercial cold plate data using power-law curve fitting ($Z_\theta = a \cdot V^b$).

Table 5.3: Power-law coefficients for different flow rate ranges.

Flow Rate Range (GPM)	$\boldsymbol{a}$	$\boldsymbol{b}$	$\boldsymbol{R^2}$
0–1.5	32346.93	−0.697	0.57
1.5–2.5	3040.46	−1.075	0.61

using a power-law fit of the form, $Z_\theta = a \cdot V^b$.

The scatter plot of available COTS cold plate options with different flow rate ranges along with the best cure fitting to two categories of flow rates, between 0 and 1.5 GPM and 1.5-2.5 GPM is illustrated in Figure. 5.5(b). The coefficients of the best fit for flow rate ranges are shown in Table 5.3.

The reliability of power semiconductor modules is largely influenced by thermal stress conditions, including junction temperature swing ΔT_j, mean junction temperature T_{mean}, pulse width, and peak temperature [327]. These factors contribute to degradation mechanisms

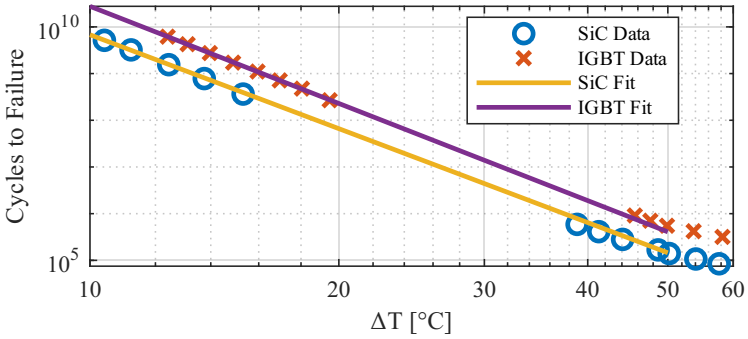


Figure 5.6: Cycle-to-failure data for IGBT and SiC power modules from [327], along with fitted lifetime models based on the simplified CIPS08 expression (5.6).

Table 5.4: Power cycling model coefficients for SiC and IGBT devices for $\Delta T \leq 50°C$.

Device Type	K'	β_1	β_2 (eV)
SiC	8.40×10^8	6.68	0.621
IGBT	6.66×10^8	6.91	0.603

such as solder fatigue and bond wire lift-off—well-established failure modes in both silicon (IGBT) and silicon carbide (SiC) inverter modules [328, 329].

Different semiconductor technologies exhibit varying aging behaviors due to material properties and thermal limitations [327, 330]. Figure. 5.6 presents the cycles to failure data presented in [327] along with fitted curve for both SiC and IGBT modules.

To model the expected number of thermal cycles to failure, simplified CIPS08-type lifetime model is used to capture the effect of junction temperature swing and cycles to failure as expressed in (5.6). Moreover, Table 5.4 summarizes these coefficients extracted from published power cycling data.

$$N_f \propto K' \cdot (\Delta T)^{-\beta_1} \cdot \exp\left(\frac{\beta_2}{k_b \cdot T_{\text{mean}}}\right) \tag{5.6}$$

To convert cycle-to-failure predictions into inverter-level reliability metrics for EVs, automo-

tive usage standards such as GMW3172 and CS-00056 have been used as references for such a conversion. These standards define vehicle usage assumptions in terms of daily drive time and total annual mileage, allowing conversion of thermal stress accumulation into "miles to failure" for the inverter design qualification. Using these objective functions identified above, an optimization problem can be developed and explored.

In the context of EV traction inverter design, where thermal, electrical, and volumetric considerations are tightly coupled, a multi-objective genetic algorithm (GA) is well-suited to explore trade-offs among competing design goals. The GA is an evolutionary optimization technique inspired by the process of natural selection. In each generation, a GA develops a population of candidate solutions through genetic operations such as selection, crossover, and mutation. This population-based strategy is effective for exploring large, high-dimensional design spaces with nonlinear constraints and multiple conflicting objectives. In this study, the non-dominated sorting genetic algorithm II (NSGA-II) [331] is employed to perform multi-objective optimization.

The dynamic behavior of the EV system, inclduing the power electronics system, is modeled using `PLECS` [332], a simulation platform that supports detailed co-simulation of electrical switching dynamics, thermal behavior, and mechanical drivetrain interactions. Within each optimization iteration, `PLECS` is used to evaluate the inverter's cycle-by-cycle switching behavior over a specific drive cycle. The simulation outputs include the junction temperature profile of the power modules, switching losses, and instantaneous efficiency. These time-domain outputs are post-processed to compute weighted average inverter efficiency, reliability metrics based on thermal cycling damage, and total hardware volume.

The optimization is performed using the open-source Python-based framework `pymoo` [333], which handles population evolution, objective function evaluation, and Pareto front extraction. `pymoo` manages the gene space consisting of design variables including switching fre-

quency, DC-link capacitance, battery voltage, and thermal interface selection.

For each candidate solution, the framework initiates a full simulation in PLECS, extracts relevant metrics, and computes objective functions offline in Python. Similar methods have been successfully applied in prior works involving mission-profile-driven design and inverter reliability optimization between reliability and efficiency.

Figure. 5.7 describes the software integration workflow between pymoo and PLECS, linked through Python to enable a seamless integration between the EV simulation and computation of the simulation results.

In order to establish the average converter efficiency and reliability, it is necessary to simulate the behavior of the inverter under a wide range of operating conditions and driving cycles, which include periods of acceleration, deceleration, and cruising. Because the drivetrain system behaves vastly different between these driving conditions, it requires a weighted average efficiency and reliability computation scheme to represent the overall performance. Finding proper weights for these cases is crucial as it affects both the scaling of the average efficiency and reliability calculation. Therefore, to standardize the scaling factor to a normal driving cycle of vehicles, the EPA provided driving profile US06/Supplemental FTP [334] was selected to represent a mix of highway and city driving over 600 seconds.

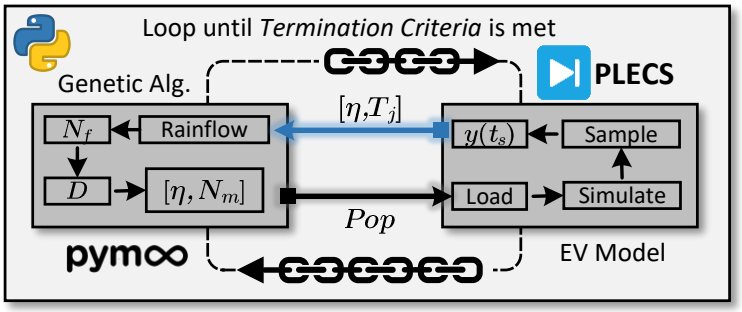


Figure 5.7: PLEC-Python multi-objective optimization process to integrate the EV model developed in PLECS and NSGA computation analysis through pymoo

From the US06 drive profile, which is represented with a grey solid line in Figure. 5.8, the acceleration and deceleration intervals were determined by calculating the derivative of the speed. If the derivative of the speed in a time step was more than 15% of the max and positive, it was determined to be acceleration, 15% of the max and negative was determined to be deceleration, at 0 mph speed determined to be idling, and anything else determined to be cruising.

Figure. 5.8 illustrates the periods determined to be acceleration, deceleration or cruising of the vehicle. There were 45 seconds spent at a stop or idling that were ignored for the efficiency and reliability calculations since no power is being fed through the traction inverter. This gives the relative weights, w_{P_d} shown in Table 5.5 for each driving condition, P_d.

The stress accumulation was segmented to each driving condition and the accumulated damage on the power modules was estimated by summing the individual damage ratio to the total cycles in each temperate cycle range, as expressed in (5.7).

$$D_{P_d} = \sum_{i=1}^{k} \frac{n_i}{N_{f,i}} \tag{5.7}$$

where k, n_i, and $N_{f,i}$ are the total number of stress levels, the number of cycles or occurrences at stress level i, and the number of cycles to failure at stress level i, respectively.

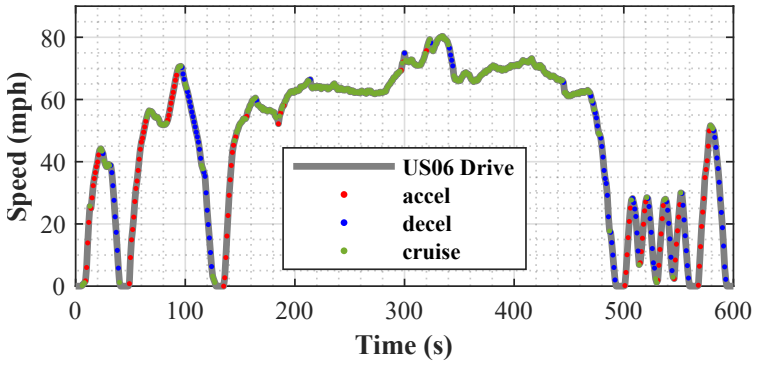


Figure 5.8: US06 driving profile with periods of acceleration, deceleration, and cruising.

The total weighted average converter efficiency, expressed in (5.8) and reliability in (5.10) are therefore defined to be equal to the weighted sum of the efficiencies and failure cycles of the inverter during the acceleration, deceleration, and cruise conditions. This allows for a much shorter driving profile to be used during the simulation, which is necessary to limit the processing needed during the optimization.

$$\eta_{avg} = \sum^{P_d} \eta_{P_d} \cdot w_{P_d}, P_d \in \{accel, decel, cruise\} \tag{5.8}$$

$$\Lambda_{avg}^{-1} = \sum^{P_d} D_{P_d} \cdot w_{P_d}, P_d \in \{accel, decel, cruise\} \tag{5.9}$$

$$N_{m,avg} = \sigma_{us06} \cdot \Lambda_{avg}^{-1} \cdot d_{tot} \tag{5.10}$$

The total miles to failure, $N_{m,avg}$ can be derived using (5.10), which takes the total weighted failure rate across different driving conditions in (5.9), the total distance that the vehicle was driven, d_{tot}, and the normalization factor, σ_{us06} based on the US06 drive profile to ensure consistency with the user-defined driving cycle with the the applied weights, w_{P_d} from the US06 driving profile, including the ratio of the driving time duration between the actual and US06.

Table 5.5: Time and relative weights of driving conditions.

Driving Condition [P_d]	**Time (s)**	**Weighting (%) [w_{P_d}]**
Acceleration [*accel*]	90	16.22%
Deceleration [*decel*]	99	17.84%
Cruise [*cruise*]	366	65.95%
Total	555	100%

Algorithm 1 Fitness Evaluation for Multi-Objective Inverter

Require: Initial population $P_0 = \{x_1, x_2, ..., x_n\}$ with genes: switching frequency, DC voltage, capacitance, etc.
Ensure: $F(P_0) = [F_\eta, F_V, F_\lambda]$ for each individual
  for each individual $x_i \in P_0$ **do**
    Configure inverter model in PLECS using parameters x_i
    Simulate drive cycle to extract $T_j(t)$ and $\eta(t)$
    Compute average efficiency and reliability: η_{avg} and λ_{avg}
    Calculate total hardware volume from curve-fit models for heatsink and DC-link capacitor
    Assign fitness vector $F(x_i) = [\eta_{\text{avg}}, V_{\text{tot}}, \lambda_{\text{avg}}]$
  end for
  return $F(P_0)$ to NSGA-II for non-dominated sorting and next-generation evolution

Algorithm 1 describes the co-simulation loop between `PLECS` and Python and optimization fitness function with three objectives, which maximizes average inverter efficiency, F_η, minimizes total critical component volume (capacitor and heatsink), F_V, and maximizes reliability, F_λ.

Figure. 5.9(a) illustrates the trade-off between the critical inverter component volume and reliability. It is evident that higher reliability values are generally associated with increased component volume. This trend is attributed to the use of larger heatsinks and capacitors that reduce junction temperature swings and ripple. A cluster of points with lower volume (< 1.5L) shows significant spread in reliability, indicating sensitivity to thermal and electrical design choices in this compact regime. Moreover, the lower the switching frequency the higher the reliability due to reduced switching losses and lower junction temperature variation in the power modules.

Figure. 5.9(b) shows the volume-efficiency trade-off. High efficiency values ($> 98.5\%$) are observed across a range of volumes, but particularly cluster toward low-to-moderate volume designs. Lower volume designs (< 1.0L) tend to have wider efficiency variance, and fewer fall within the Pareto-optimal front, suggesting that aggressive miniaturization often comes at

the cost of switching and conduction losses. This behavior is further supported by the observation that higher switching frequency configurations tend to yield lower average efficiency, while lower-frequency designs typically achieve higher average efficiency, though there are designs that produce lower total volume with lower switching frequency.

Figure. 5.9(c) highlights the relationship between reliability and efficiency. A clear positive correlation exists, particularly within the Pareto-optimal region. Higher reliability designs ($> 150,000$miles) generally exhibit efficiencies above 97.5%, indicating that efficient thermal management strategies with larger heatsink designs or lower switching frequencies benefit both objectives. However, a small set of solutions shows extreme reliability at the expense of efficiency, reflecting overly conservative designs with very low junction temperature rise but reduced performance. Lastly, this behavior is further explained by the observation that lower switching frequency designs yield both higher average efficiency and reliability.

These results demonstrate the importance of considering all three objectives during inverter design. The Pareto front allows designers to select among a family of equally optimal solutions depending on the preference, such as compactness for size-constrained platforms, efficiency for range-sensitive applications, or reliability for mission-critical use cases.

The resulting Pareto frontiers showed trade-offs between these competing objectives; higher reliability was generally associated with increased volume due to enhanced thermal management, while maximum efficiency clustered around low-to-moderate volume designs. Compact designs were shown to be more sensitive to parameter selection, with greater variation in reliability and performance. These insights offer a comprehensive way for selecting optimal inverter design parameters that align with application-specific constraints, such as range, density, or longevity requirements.

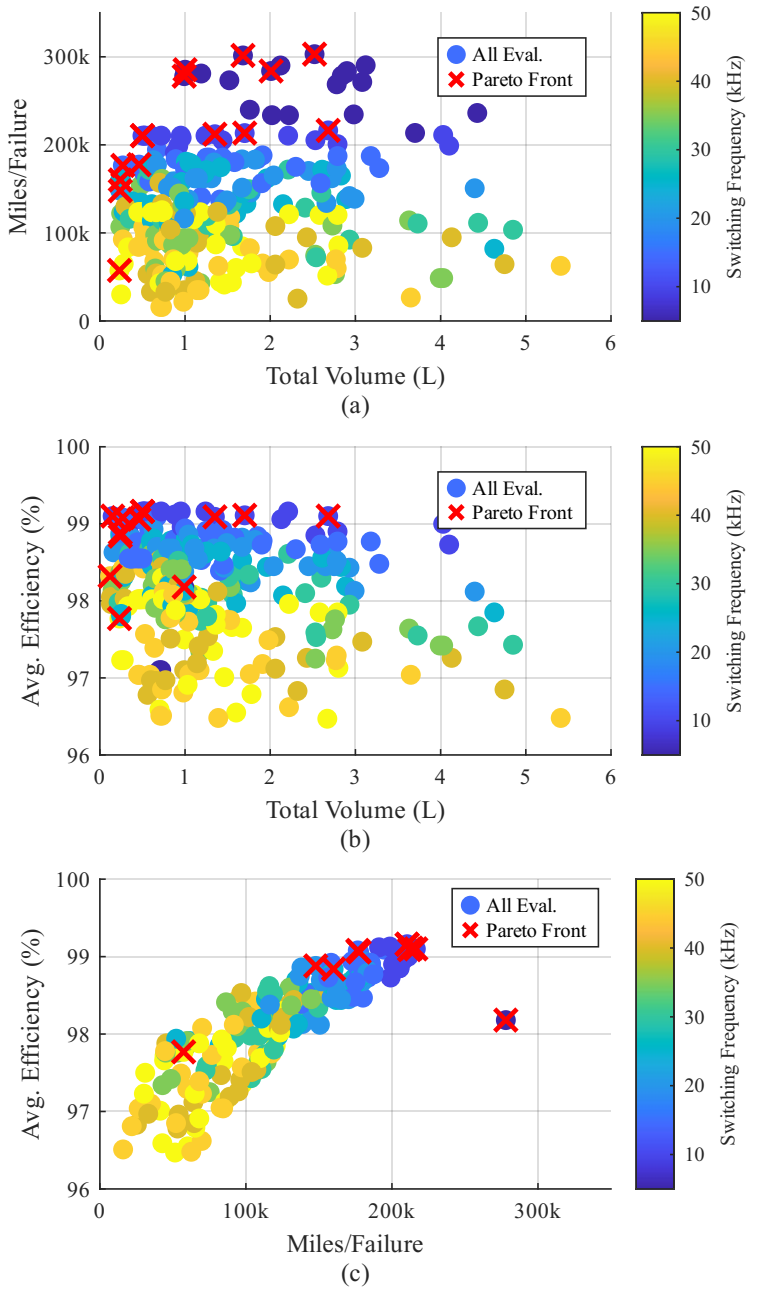


Figure 5.9: Pareto front projections showing trade-offs among total volume, average efficiency, and reliability and color coded by switching frequency, describing: (a) miles before failure and total volume, (b) average efficiency and total volume, and (c) average efficiency and miles before failure.

5.1.2 Co-Design Analysis of WBG Power Diodes with Operational Regimes

An integral aspect of co-design approach for WBG power devices is the assessment of the Figures of Merit (FOM). The decision to insert devices into end-use power electronic frameworks should be based on the overarching system-level advantages offered by a device under specific operational regimes, such as switching frequency, hold-off voltage, and current-handling capability. Given their elevated ionization thresholds and substantial critical fields, UWBG devices need lower doping levels and thinner drift regions compared to their WBG counterparts to achieve similar breakdown voltages.

Therefore, this subsection demonstrates an advanced power diode optimization process and converter integration analysis, in which the optimization tool takes system operational metrics, selects device drift region dimensions and doping concentrations to optimize system power dissipation, based on models suited for diverse material systems and device architectures. PiN and Schottky diodes have been evaluated, attributed to their inherent simplicity. The optimization algorithm has factored important effects, like the Mott-Gurney conduction and incomplete dopant ionization phenomena.

Moreover, emerging from the device optimization process are distinct loss characteristics for diverse materials and diode configurations. These characteristics are compared in their performance within the context of a single-phase 3-level boost power factor correction (PFC) topology. The details of the device design optimization and the findings from the optimization development are discussed.

During system operation, the power dissipation in a diode is composed of three parts: static power dissipation due to conduction loss or reverse leakage current, dynamic power dissipation due to switching, and power loss due to displacement currents as expressed in (5.11):

$$P_{\text{loss}} = P_{\text{static}} + P_{\text{dynamic}} + P_{\text{displacement}} \tag{5.11}$$

The static power dissipation, P_{static}, is composed of power dissipated in the blocking state and in the conduction state along with the reverse power dissipation, which is the product of the required system-level blocking voltage (V_{reverse}), the leakage current density (J_{reverse}), and fractional amount of time in the off-state, $1 - D$. This expression is shown in (5.12).

$$P_{\text{static}} = J_{\text{reverse}} \cdot V_{\text{reverse}} \cdot (1 - D) + P_{\text{forward}} \tag{5.12}$$

The reverse bias, V_{reverse}, is constrained by the doping and drift thickness-dependent breakdown voltage of the device and the breakdown voltage is computed according to whether the diode is in non-punch-through configuration (the depletion width x_d is less than the device thickness t_{drift}) or punch-through configuration in (5.13):

$$V_{\text{breakdown}} = \begin{cases} \frac{\epsilon_s \cdot E_{\text{crit}}^2}{2qN} & \text{for } x_d \leq t_{\text{drift}} \\ E_{\text{crit}} \cdot t_{\text{drift}} - \frac{qNt_{\text{drift}}^2}{2\epsilon_s} & \text{for } x_d > t_{\text{drift}} \end{cases} \tag{5.13}$$

The critical field is calculated according to the method described in [335, 336]. By setting the carrier multiplication integral equal to unity, the fraction of ionized carriers diverges.

To calculate power dissipation in the conduction mode, it is determined if the given material, device thickness, and doping concentration would demonstrate space-charge limited (SCL) current according to the method described in [337]. SCL effects are assumed to take place if the drift thickness of the device falls within the interval defined by (5.14):

$$0.1\ \mu m \leq t_{\text{drift}} \leq \sqrt{\frac{\varepsilon_s (V_{\text{SCL}} + V_{\text{turn-on}})}{q \cdot n}} \tag{5.14}$$

where V_{SCL} is the bias drop across the device due to the space-charge limited current, calculated self-consistently with (5.14) and (5.15):

$$V_{\text{SCL}} = \sqrt{\frac{8}{9} \frac{J_{\text{forward}} \cdot t_{\text{drift}}^3}{\mu \cdot \varepsilon_s}} \tag{5.15}$$

μ is the mobility for the given doping concentration and electric field. n is the density of free carriers (electrons for n-type devices and holes for p-type), computed by self-consistently solving for the Fermi level and the free charge density that simultaneously satisfy (5.16)-(5.17):

$$n = \frac{N}{1 + g_D \exp\left(\frac{q(E_F - E_D)}{kT}\right)} \tag{5.16}$$

$$n = N_c \int_0^\infty \frac{(E - E_c)^{0.5}\, dE}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{5.17}$$

The on-state resistance is primarily a function of the device thickness (t_{drift}), free carrier concentration (n), carrier mobilities (μ_n, μ_p), and the minority carrier concentration (holes for all materials except Diamond). The average minority-carrier concentration is equal to the ratio of the stored charge in the device drift region [338]. Since the stored charge, found by integrating the distribution of injected carriers, is equal to the product of the forward current density J_{forward} and the blocking layer ambipolar lifetime τ, which reduces to (5.18).

$$R_{\text{on}} = \frac{t_{\text{drift}}}{q\,(\mu_n \cdot n) + \frac{q(\mu_n + \mu_p) J_{\text{forward}} \cdot \tau}{t_{\text{drift}}}} \tag{5.18}$$

The dynamic power dissipation is equal to the frequency of switching, f, multiplied by the sum of energies dissipated in the on (E_{on}) and off (E_{off}) transitions. The stored charge per unit area is the product of the forward current density and the ambipolar lifetime. This reduces the dynamic power dissipation to (5.19).

$$P_{\text{dynamic}} \approx V_{\text{reverse}} \cdot J_{\text{forward}} \cdot \tau \tag{5.19}$$

Finally, each switching event induces a displacement current proportional to the capacitance of the diode and the rate of change of the bias in the transition, dV/dt. By integrating the product of the voltage and current over the voltage range V_{forward} to $-V_{\text{reverse}}$, the power dissipation per switch event due to this effect can be determined. This must be multiplied by twice the switching frequency to get the total power displacement. By assuming $V_{\text{forward}} \approx V_{on}$, and inserting the classical equation for PN-junction capacitance, the displacement power can be described by (5.20):

$$P_{\text{displacement}} = \frac{f}{3}\sqrt{\frac{qN_d\varepsilon_s}{2}}\left(V_{\text{on}} + V_{\text{reverse}}\right)^{\frac{3}{2}} \tag{5.20}$$

There are several device types that are considered in this study. This includes the operation of PiN, Schottky, and MPS diodes. The simplest type of diode is a simple PiN diode. It is composed of an n-doped region in contact with a p-doped region, both uniformly doped. In the forward conduction regime, PiN diodes exhibit high turn-on voltage due to the built-in voltage of the PiN junction. For the purposes of the optimization tool, it is assumed that the built-in voltage is equal to the bandgap of the material comprising the junction. In the reverse blocking regime, PiN diodes are characterized by low leakage currents, as the thermal generation/recombination process is the only source of free carriers. For simplicity,

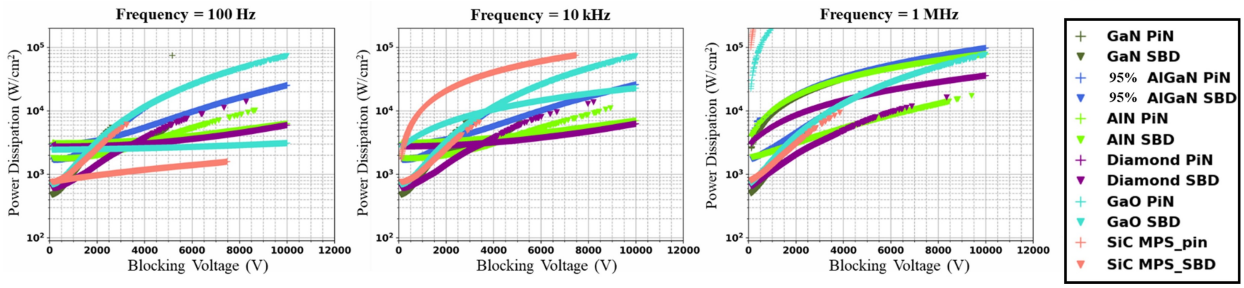


Figure 5.10: Minimum power dissipation results from the optimization across blocking voltage with different device materials and types. Figures are generated at different switching frequencies (100 Hz, 10 kHz, and 1 MHz), all at room temperature.

the optimization tool calculates the reverse leakage current density of PiN diodes to be 1 pA/V.

A Schottky barrier diode (SBD) is characterized by lower turn-on voltage, but higher reverse current leakage compared to the PiN diode. The turn-on voltage is determined by the Schottky barrier height between the semiconductor and the metal contact (φ), subject to field-induced barrier lowering from the initial barrier height (φ_0) due to image charges. This effect is modeled with (5.21) where E_{max} is the maximum value of the electric field across the semiconductor/metal interface and is described by (5.22)

$$\varphi = \varphi_0 - \sqrt{\frac{qE_{\max}}{4\pi\varepsilon_s}} \tag{5.21}$$

$$E_{\max} = \sqrt{\frac{2qN(\varphi_0 - V_{\text{reverse}})}{\varepsilon_s}} \tag{5.22}$$

In the reverse blocking regime, leakage current is driven by thermionic emission (J_{TE}) over the Schottky barrier (dominant at high temperatures), tunneling of carriers through the barrier via field emission (J_{FE}, dominant at very low temperatures), and thermal-assisted thermionic field emission of carriers (J_{TFE}, dominant at mid-range temperatures and higher

doping levels). Unlike a PiN diode, the SBD is a majority-carrier device. Therefore SBDs do not exhibit reverse recovery from turn-off and effectively have a negligible carrier lifetime. While this is advantageous in high-frequency switching since dynamic power dissipation is negligible, it comes at the cost of eliminating conductivity modulation in forward conduction, increasing R_{on} compared to PiN diodes.

Lastly, the MPS diode consists of interdigitated regions containing Schottky barriers and PiN junctions. In blocking mode, the MPS diode acts much like a PiN diode, with very low reverse current leakage. However, in forward conducting mode, either the Schottky barrier (JBS mode) or the PiN junction (MPS mode) may be the primary conduction pathway depending on the magnitude of the applied voltage. JBS mode will have lower dynamic power dissipation due to the lack of minority carriers, while MPS mode will exhibit conductivity modulation due to the presence of minority carriers. Optimizing a device with two possible conduction modes will yield instabilities in the numerical computation, as the optimization will tend to oscillate between metastable local minima. In order to avoid this oscillation, the MPS device was optimized as two separate devices (one in JBS mode and one in MPS mode) and the minimum power dissipation between each mode was chosen.

Algorithm 2 Optimization for Minimizing Power Dissipation

Require: Device type, Material, V_R, J_F, f_s, D, Temperature (K)
Ensure: Optimal t_{drift} and N_d
1: *Initialization:* Set initial values for diode thickness t_{drift} and doping concentration N_d
2: *Loop Process:*
3: **for** each iteration until convergence or satisfaction **do**
4: Adjust t_{drift} and N_d to minimize power dissipation
5: Ensure constraints:
1. $V_R \leq \frac{1}{2} V_{BR}$
2. $0.1\,\mu\text{m} \leq t_{\text{drift}} \leq 100\,\mu\text{m}$
3. $10^{15}\,\text{cm}^{-3} \leq N_d \leq 10^{17}\,\text{cm}^{-3}$
6: **end for**
7: **return** Optimal t_{drift} and N_d

The optimization tool developed for UWBG devices is an advancement of the work described in [335, 338]. The process flow of this optimization tool is described in Algorithm 2. For a given device type and material, a mobility model is used to determine carrier mobilities at a given temperature, doping level, and electric field. For some materials, this mobility model is computed from various scattering contributions, while for the rest of the materials empirical models available in the literature are used instead. The operational parameters of the diode in the system are the reverse operating bias, forward current density, switching frequency, duty cycle, and device operational temperature. The critical fields are tabulated for various values of doping concentration and device thickness using the method described before. The optimization program then minimizes power dissipation in the system by altering device drift region thickness and doping concentration subject to the constraint that device breakdown is greater than or equal to twice the required blocking voltage. By iterating across all available system operating parameters, it is possible to develop a map in system operating space and determine which devices/materials produce the lowest power loss for any given system operational point based on materials properties.

Figure. 5.10 illustrates the outcomes of the optimization program for diverse device materials and types at switching frequencies of 100 Hz, 10 kHz, and 1 MHz. The program assesses the power dissipation per unit area in relation to the blocking voltage, specifically for SiC MPS diodes, while PiN and Schottky diodes are evaluated for all other materials.

The simulation results show the optimal material and device type that yields the minimal power dissipation for each switching frequency and reverse bias condition. For instance, at 10 kHz frequency, GaN SBDs are the optimal choice for voltages below 500 V. Diamond SBDs are favored in the 500 V to 3.1 kV range, AlN SBDs from 3.1 kV to 4.1 kV, and diamond PiN diodes are preferred between 4.1 kV and 10 kV. It's pertinent to highlight that the optimization tool encounters challenges in discerning solutions at extreme reverse bias

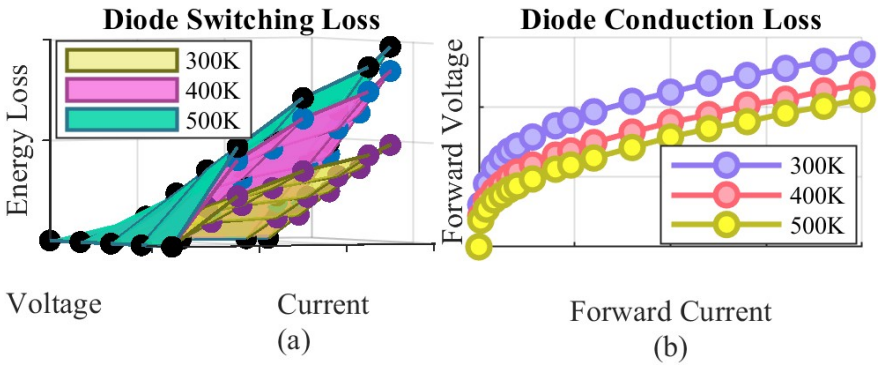


Figure 5.11: The power diode loss map delineates: (a) switching losses, encompassing contributions from P_{static}, P_{dynamic}, and $P_{\text{displacement}}$, when relevant, and (b) the forward bias voltage derived from the forward current characteristics.

levels and switching frequencies, shown from the absence of SiC PiN-mode MPS data points exceeding 7.5 kV at 100 Hz. The tool does not make extrapolations beyond the highest logged solution for a particular material and device category, leading to the selection of β-Ga2O3 PiN diodes as the optimal choice above 7.5 kV in this instance.

The optimization tool is also suitable for considering several other metrics. For example, the switching and conduction loss traits are depicted in Figure. 5.11. Heat maps that showcase optimized doping concentrations, drift thicknesses, and the resultant unipolar figure of merit, denoted as $VB^2/R_{on,sp}$, can be also produced.

To evaluate the optimized WBG and UWBG device loss characteristics, the single-phase 3-level boost power factor correction (PFC) topology [339] was used in various current and frequency operation regimes. Such a topology is selected due to its usage of a full-bridge diode configuration in the front end along with the boost conversion stage to address the challenges of power quality and efficiency in single-phase power systems. The topology produces three voltage levels from a single-phase input, thereby enhancing the power factor and reducing total harmonic distortion (THD), especially at high power levels. The intermediate voltage level allows for smoother transitions between voltage states, resulting in reduced

voltage stress on components and minimized switching losses. Consequently, the circuit can operate at higher frequencies, leading to a better assessment and comparison of the switching frequency impacts on the WBG and UWBG power diodes.

Figure. 5.12 depicts the single-phase 3-level boost PFC circuit topology, with associated input and output waveforms. The input waveform, originally sinusoidal, becomes full-wave rectified post the diode bridge. This transformation produces a pulsating DC voltage, with the PFC-induced input current waveform closely mirroring the voltage waveform for a high power factor. Ideally, when waveforms are in phase, it indicates a near-unity power factor.

Through the diode bridge ($D_1 - D_4$), the inductor current waveform can vary based on the control strategy. Freewheeling diodes ($D_5 - D_6$) conduct during the primary switch's off periods. With switches deactivating via a phase shift, the inductor current is routed through the freewheeling diode, producing a pulsed waveform synchronized with the rectified input voltage at v_g.

The output voltage of the 3-level boost PFC is a DC voltage with a value higher than the input voltage and through the output capacitors the output voltage pulsations are smoothened out to a DC characteristic.

The rectifying diode bridge ($D_1 - D_4$) and the freewheeling diodes ($D_5 - D_6$) experience distinct voltage and current stress profiles in the PFC converter due to their respective roles. Figure. 5.13 showcases the voltage and current behaviors across these diodes. Rectifying diodes, synchronized by the PFC to align current and voltage phase, experience only conduction losses during their on-state, eliminating switching losses. Conversely, the freewheeling diodes, influenced by the voltage and current pulsations from the boost converter switches, are subject to both switching and conduction losses. These dynamics, while unique, are pivotal in assessing total losses and differentiating between switching and conduction

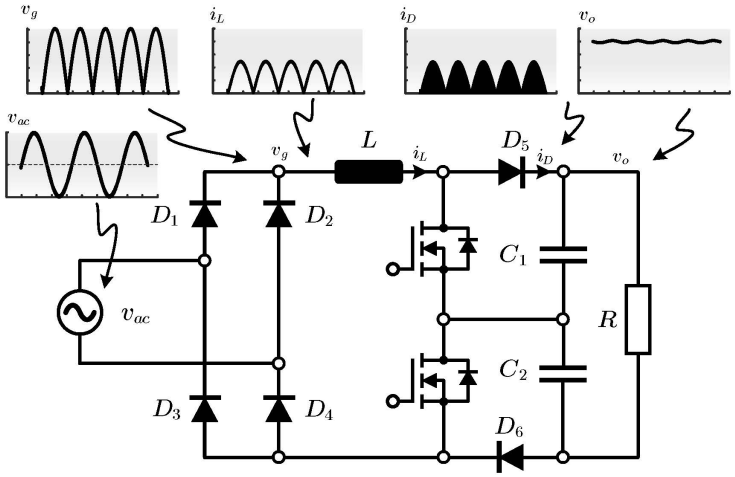


Figure 5.12: Single-phase 3-level boost PFC circuit schematic and illustration of important current and voltage waveforms at different nodes in the converter.

contributions.

The loss characteristics of both UWBG and WBG devices, as depicted in Figure. 5.11, were integrated into the diode models with proper loss calculation. Following this integration, the single-phase 3-level boost PFC converter was used to evaluate the loss performance over different device materials and types. The PFC simulation circuit maintains a power factor of less than 5% for all test cases in order to comply with the international power quality standards. Moreover, by ensuring this low power factor, the converter operation reduces potential electronic interference, prompting smoother interactions with other electronic systems and significantly diminishing the strain on the power grid infrastructure.

Figure. 5.14 shows the output of the simulation model, highlighting the input voltage and current waveforms, boosted output voltage, and the power loss characteristics from both the conduction and switching of the diodes. Note that the conduction loss closely follows the rectified positive half-cycle input current waveform as the rectifying diodes account most of the conduction loss whereas the switching loss is induced from the pulsating voltage and current through the freewheeling diodes of the boost PFC.

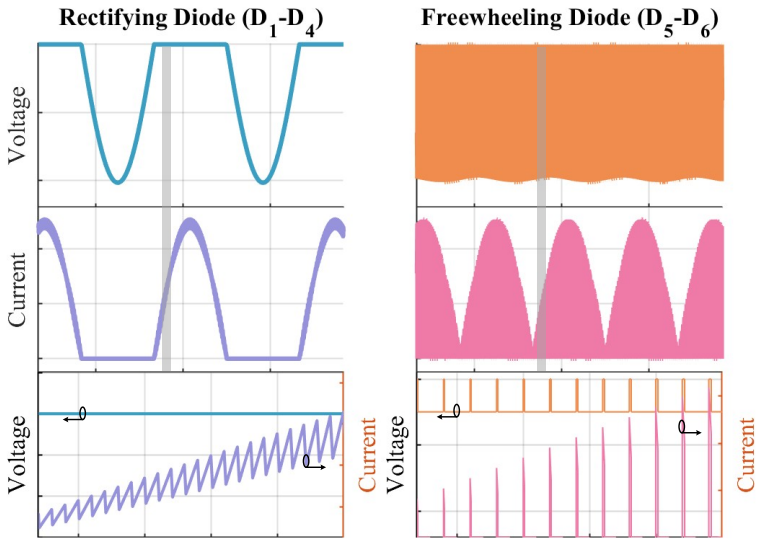


Figure 5.13: The voltage and current stress waveforms differ between the rectifying and freewheeling diodes. Rectifying diodes primarily incur conduction loss as they conduct the input current during zero voltage. In contrast, freewheeling diodes experience both conduction and switching losses, the latter arising from the hard-switching dynamics imposed by the converter switches. The bottom panels provide a magnified view of the voltage and current waveforms, focusing on the areas highlighted by the lightly shaded regions.

Utilizing the simulation model with distinct device loss characteristics, a detailed analysis of the converter's performance was analyzed over various current densities and switching frequencies. Figure. 5.15 provides a comprehensive parametric analysis, mapping out the interplay between different current densities and switching frequencies across a range of materials and device types.

Observations from Figure. 5.15(a) illustrate the efficiency density against varied current densities. Furthermore, it contrasts the contributions of conduction and switching losses relative to the converter's total loss at a benchmark of 1000A/cm^2. A notable observation is the superiority of diamond in this analysis, which exhibits minimal conduction loss contributions, especially at elevated current densities. In parallel, both GaN and GaO present a noteworthy and similar trend, demonstrating analogous efficiency density performances across current densities.

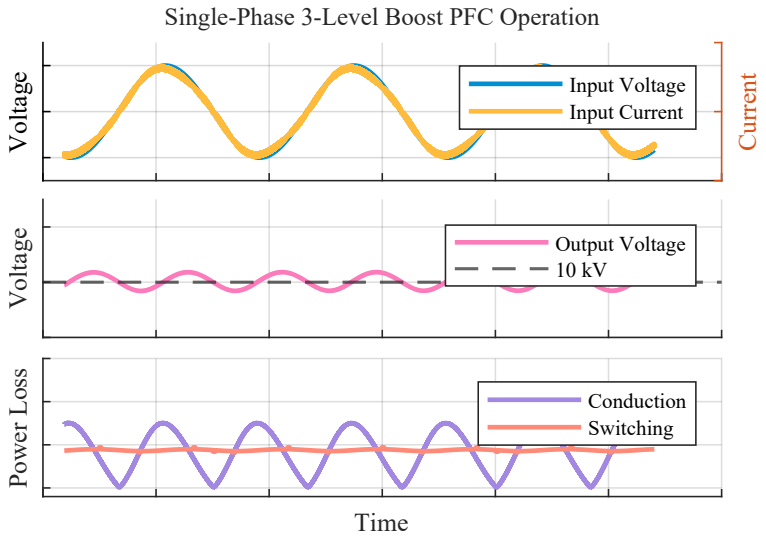


Figure 5.14: Single-phase 3-level boost PFC simulation results, illustrating ≤5% THD, 10 kV desired output voltage with small ripple, and power loss comparison between the conduction and switching loss of the power diodes.

The parametric assessment of PIN diodes, as depicted in Figure. 5.15(b), shows comparable high efficiency density performance between AlGaN, Diamond, and GaN materials whereas GaO and SiC show increasing impacts from the switching loss characteristics. Furthermore, Figure. 5.15(c) and (d) show the switching frequency analysis between different device materials for SBD and PIN diodes, respectively. With increasing switching frequency, the efficiency density is reduced with the impact of insignificant switching loss contributions, though for the SBD the switching losses still account for ≤1% for each device material in Figure. 5.15(c). However, the switching losses become the majority of the loss contributions the switching frequency increases as illustrated in Figure. 5.15(d). Note that the loss contributions of SiC is only partially shown in order to show proper scaling for the rest of the devices.

In summary, the presented analyses provide operational dynamics of various materials and device types under different conditions, underscoring the intricate balance between efficiency, conduction, and switching losses between device materials and types.

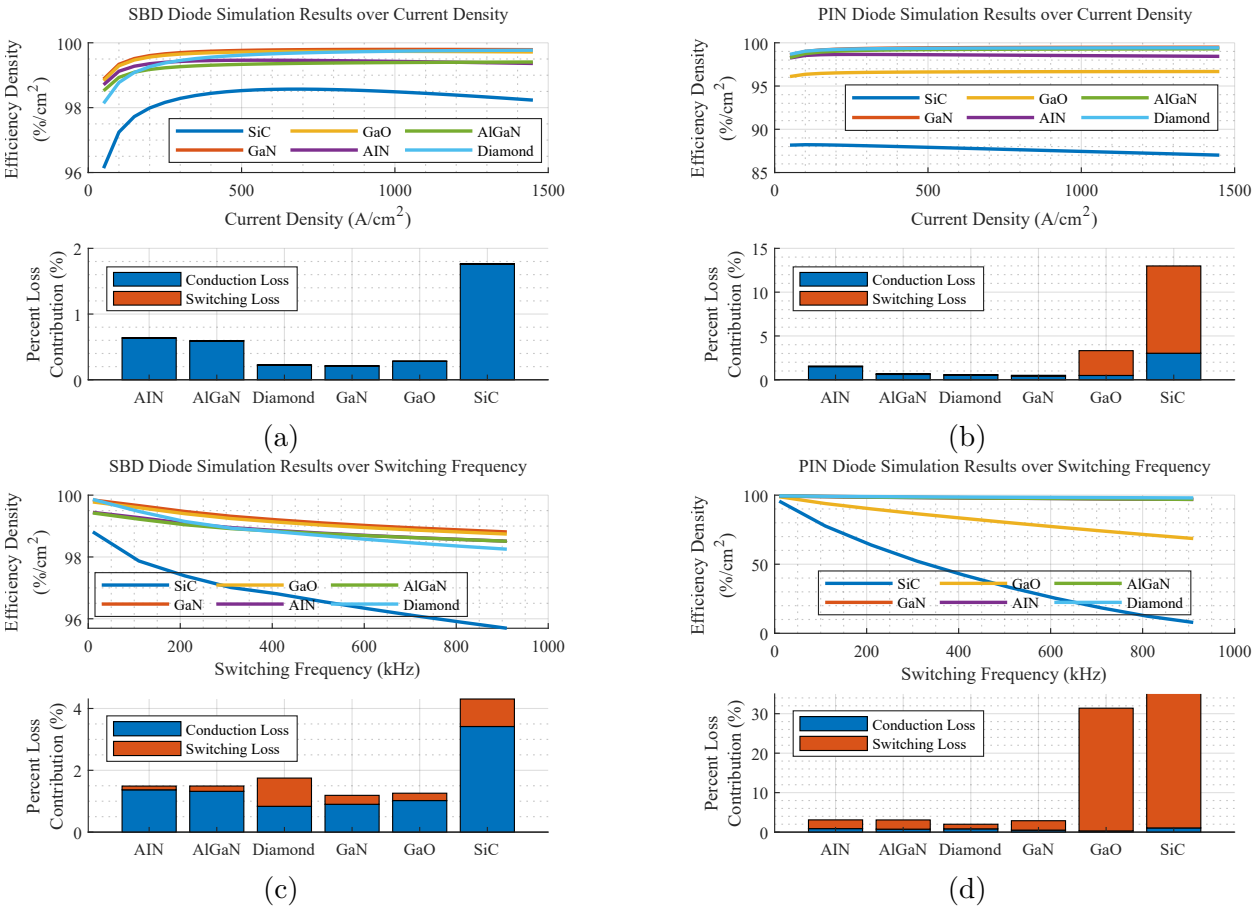


Figure 5.15: Analysis of efficiency density and power loss contribution comparison between different UWBG and WBG device materials and types. (a) depicts the efficiency density (%/cm^2) over current density (A/cm^2) between UWBG and WBG materials for the SBD diode construction along with the percentage loss contributions in regards to the total powre loss whereas (b) shows the results for the PIN diodes. (c) and (d) illustrate the results across different switching frequencies for SBD and PIN, respectively.

The results reveal optimal diode materials and designs across varied switching frequencies and blocking voltages at a temperature of 300 K and a forward current density of 1000 A/cm^2. The simulation studies assess the devices' performance when employed as rectifying diodes in a full-wave rectifier and as freewheeling diodes in a boost converter, collectively configured for PFC operation. The outcomes highlight the synergy achieved through a co-design approach, optimizing devices for specific parameters while enhancing converter performance across broader operational domains.

Future endeavors should encompass thermal interactions between the die and package, development of accurate thermal models for circuit simulations, and exploration of diverse diode combinations to ensure optimal performance in desired circuit configurations while evaluating the materials' FOM [283, 285].

5.2 Dynamic Device Lifetime Estimation Methodologies

This section presents methodologies for dynamic device lifetime estimation that leverage real-time monitoring and data-driven modeling to enhance predictive accuracy and operational reliability. Conventional lifetime assessment approaches rely on simplified prediction models, which cannot capture evolving stress conditions and device dynamics arising from material property variations or characteristic drift. The focus in this section is on enabling continuous health assessment and AI-driven prediction capabilities in systems employing WBG devices.

Subsection 5.2.1 details a HIL–based real-time lifetime prediction framework. This approach integrates live operational data from FET-based power modules with coupled electrical–thermal models to evaluate the remaining useful life (RUL) under dynamically changing stress conditions. By continuously monitoring junction temperature from dynamically changing load profiles, the framework enables historical performance tracking and periodic model updates. This capability improves prediction accuracy compared to the static lifetime prediction calculation.

Subsection 5.2.2 introduces a deep neural network fusion model for lifetime estimation using multi-modal device datasets. The model combines scalar parameters, such as threshold voltage, on-resistance, and capacitances, with sequential waveform data from dynamic switching

and thermal measurements. By learning from these heterogeneous inputs, the fusion network captures complex dependencies between electrical performance, thermal response, and process-induced variability. This approach addresses the limitations of conventional physics-based models, which overlook environmental influences and higher-order interactions. This also demonstrates its potential use case for enhancing predictive capability for estimating device lifetime.

5.2.1 Real-Time Lifetime Prediction Using Hardware-in-the-Loop

Improved health monitoring techniques are necessary to evaluate dynamic performances of the FET-integrated electrical systems. By advancing the capability to monitor the real-time condition of these devices, proactive maintenance and service initiatives can be prioritized, which prevent failures, extend service life, and optimize overall system performance.

However, there is a gap persists in the topic of real-time health monitoring and predictive maintenance. Conventional monitoring methods predominantly rely on simulated estimation, intermittent testing, evaluation of lifetime from a static profile, and limited accelerated aging test conditions [270, 340], which is limited in capturing more complicated failure precursors in environments seen by the device application use cases. This limitation often results in delayed responses to critical failure, potentially compromising the system integrity and state of health. Moreover, traditional models demonstrate limited predictive accuracy as they fail to account real-time thermal behaviors under dynamically changing stresses, thereby diminishing their practical utility [341]. In addition, the integration of digital twin technologies with real-time hardware environments remains underexplored, which could otherwise substantially enhance predictive maintenance capabilities. Therefore capturing of continuous data and predicting failures proactively are important capabilities that can be

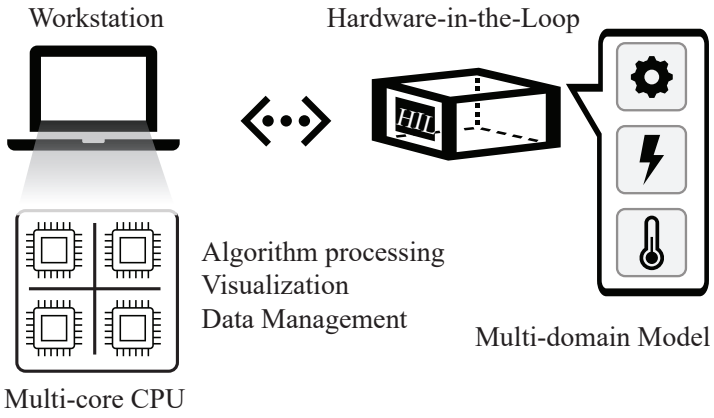


Figure 5.16: Real-time lifetime processing framework via HIL multi-domain models and data processing strategy.

researched in the field of remaining useful life [342].

There has been more focus on developing digital twins in semiconductor testing and monitoring [343]. For instance, Wang et al., [126], discussed the prospects of digital twins in predictive maintenance, but also highlighted the challenges related to real-time data synchronization and scalability across different applications. Similarly, research by Fan et al [344] underscored the necessity for models that simultaneously address electrical and thermal parameters. However, these studies often do not manifest into practical, scalable solutions for real-time monitoring and typically neglect the integration of comprehensive thermoelectric models within a Hardware-in-the-Loop (HIL) framework.

Thus, it is critical to establish an effective HIL framework that monitors the system's health through a model that encapsulates both the electrical and thermal dynamics of FETs. The proposed framework supports assessment of time-vayring dynamic stress conditions and offers a historical evaluation of the FET or module's lifetime, enabling real-time health status, calculation of remaining useful life, and proactive maintenance strategies.

The HIL framework, depicted in Figure. 5.16, is configured for this study, allowing simulation

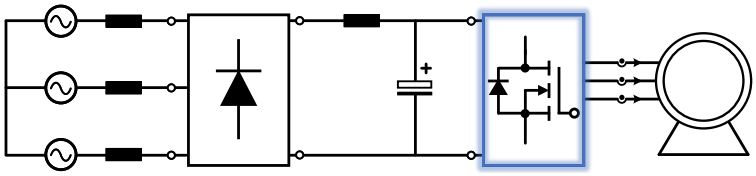


Figure 5.17: Three-phase induction motor drive system model in HIL to enable the junction temperature monitoring of the module highlighted in blue.

and analysis of complex, multi-domain system model behaviors under realistic and dynamic operational conditions. This architecture integrates several high-fidelity thermoelectric components in HIL environment for real-time simulation. The HIL hardware, equipped with high-speed computing capabilities, manages the multi-domain models, which encompasses electrical, thermal, mechanical, and control characteristics, that are critical for replicating intricate system model interactions through employing advanced solver capabilities to ensure accurate emulation of physical behaviors [345].

A server equipped with a multi-core central processing unit (CPU) handles the computational demands, overseeing data processing, real-time lifetime computation algorithms, and visualization tasks in the back-end. This ensures a well-structured flow of information and efficient data management throughout the HIL real-time operation. The server manages the simulation setup and data acquisition, dynamically monitoring and adjusting the model parameters as needed. It also captures the streaming signals of interest for further analysis.

This HIL framework is also designed for adaptability, using scripting languages like Python to automate and refine simulations and data handling processes. This not only satisfies current requirements but also provides scalability to accommodate future expansions, such as Power Hardware-in-the-Loop (PHIL) and enables the simulation of more extensive and real complex physical systems. This framework offers a solution adaptable to a wide range of applications.

Having established the comprehensive infrastructure of the real-time HIL framework, a de-

Algorithm 3 Real-time Lifetime Estimation in HIL Simulation

Initialize $D_{total} = 0$, $N_{f,hist} = 0$
Load or initialize historical temperature data
procedure Dynamic_Lifetime($dynamic$, t)
    Load dynamic temperature data from $dynamic$
    Append and save updated historical data, $aggregate$
    Calculate Rainflow (n) cycles over t
    for each Rainflow cycle, n_i **do**
        Compute Miner's Rule stress, $D = \sum \left(\frac{n_i}{\sigma_i}\right)$
        Compute $N_{f,dyn}$
    end for
    Output $N_{f,dyn}$ and D
end procedure
procedure Aggregate_Lifetime(D, j, t)
    Calculate $N_{f,hist}$ based on D, j
    Output $N_{f,hist}$
end procedure
procedure Run_Simulation($vars$, $num_segments$)
    Initialize model with simulation variables, $vars$
    Start simulation
    for $j = 1$ to $num_segments$ **do**
        Capture dynamic data, $dynamic$ over t
        Calculate_Lifetime($dynamic$, t)
        Aggregate_Lifetime(D_{total}, j, t)
        Update plots based on $N_{f,hist}$
    end for
    Stop simulation, unload model
    Finalize logging
end procedure

tailed system model incorporating appropriate electrical and thermal characteristics was developed. This model, illustrated in Figure. 5.17, illustrates a three-phase variable speed drive (VSD) system. This setup is configured to control the speed and torque of an induction motor through a modulation scheme, while incorporating additional components like the diode bridge rectifier and the three-phase inverter, which are the sub-elements for the motor's intended functionality.

The front end of the VSD system features a diode bridge rectifier, which converts incoming three-phase AC power into quasi-rectified DC voltage. This rectifier, composed of six diodes arranged in a bridge configuration, ensures full-wave rectification. The DC output is then stabilized in a DC link, which includes filtering components that smooth the DC signal, reduce ripple voltages, and provide a stable output for the inverter stage.

The DC power is transformed back to AC by the three-phase inverter, which regulates the induction motor's performance. This inverter, employing high-frequency switching of power semiconductor devices like IGBTs or MOSFETs, synthesizes AC output from DC input. By varying the frequency and amplitude of this output, the inverter controls the motor's speed and torque under different load conditions.

The development of the lifetime monitoring algorithm within the HIL framework, presented in Algorithm 3, is constructed to enable real-time assessment of semiconductor power modules under diverse simulated conditions. The dynamic and aggregated lifetime calculation algorithm, as a core component of the proposed architecture, integrates data acquisition, processing, and analysis functionalities to calculate the expected operational lifetime of the modules from the acquired data of the HIL simulation.

The algorithm ensures synchronization of all system components, enabling direct access to essential signals of interest, such as historical junction temperature data and other components' thermal or electrical characteristics. It captures the operational parameters at predefined intervals and stores this data for subsequent detailed analysis. This continuous data capture is a critical aspect of this study, as it allows for real-time monitoring of the device's response to simulated conditions, laying the evolving dataset for all subsequent analyses.

This methodology utilizes techniques to process the captured data and predict the lifetime of semiconductor devices. Employing principles of fatigue analysis [346], the algorithm eval-

uates how fluctuations in operational conditions impact the longevity of the modules. It calculates cumulative damage over time [347] and leverages these calculations to estimate the device's mean time to failure [348, 349, 350]. This involves aggregating data across multiple operational cycles and applying the algorithm to forecast the point of failure based on observed stress patterns.

The lifetime estimation process quantifies the stress and damage for each cycle, expressed as σ_i and D_i in (5.23) and (5.24), respectively. It also computes the dynamic lifetime for each data segment, $N_{f,dyn}$, and the aggregate lifetime, $N_{f,hist}$, across all segments. These computations are expressed in (5.25) and (5.26) and critical for assessing remaining useful lifetime.

The stress (σ_i) for each cycle i is calculated based on the mean junction temperature and temperature range experienced during the cycle as follows [349]:

$$\sigma_i = 1.017^{\left(125-\overline{T}_i-\frac{\Delta T_i}{2}\right)^{1.16}} \times 8.2 \cdot 10^{14} \times (\Delta T_i)^{-5.28} \tag{5.23}$$

where $\overline{T}_i$ is the mean junction temperature and ΔT_i is the junction temperature range for cycle i.

The fatigue damage (D_i) for each cycle i is calculated using Miner's Rule [351], which involves the summation of damage indices for each cycle:

$$D = \sum_{i=1}^{k} \frac{n_i}{\sigma_i} \tag{5.24}$$

where n_i is the number of occurrences of cycle i and σ_i is the stress corresponding to cycle i, calculated using the stress equation provided in (5.23).

The dynamic lifetime ($N_{f,dyn}$) for each segment is computed by summing the damages of all

cycles within that segment and converting this to years:

$$N_{f,dyn} = \frac{\tau}{D \times \gamma} \tag{5.25}$$

where D is the total damage computed across all cycles within the segment, τ is the average cycle duration in seconds, and γ is the conversion factor for converting seconds into years.

The historical or aggregate lifetime ($N_{f,hist}$) is updated after each segment by averaging the dynamic lifetimes over the aggregated segments:

$$N_{f,hist} = \sum_{j=1}^{m} N_{f,dyn,j}/m \tag{5.26}$$

where m is the number of segments processed so far, and $Nf_{dyn,j}$ is the dynamic lifetime calculated for the current segment j.

To facilitate monitoring and analysis, the algorithm incorporates visualization tools that graphically depict the data and the outcomes of the lifetime predictions. These visual outputs enable quick assessments of the device's performance, highlighting any significant degradation over time while potentially signaling the need for service maintenance or replacement for the device or module.

This algorithm not only provides the predictive capabilities of the system, but also ensures that the device testing and validation processes closely mirror real operational conditions. By considering the historical behavior of the stresses endured by the modules, it enhances the credibility and accuracy of the predictions.

The developed real-time HIL framework, coupled with Algorithm 3, accommodates time-varying input signals to the model within the HIL environment. Figure. 5.18 illustrates an example of an externally controlled torque demand profile applied to the HIL model.

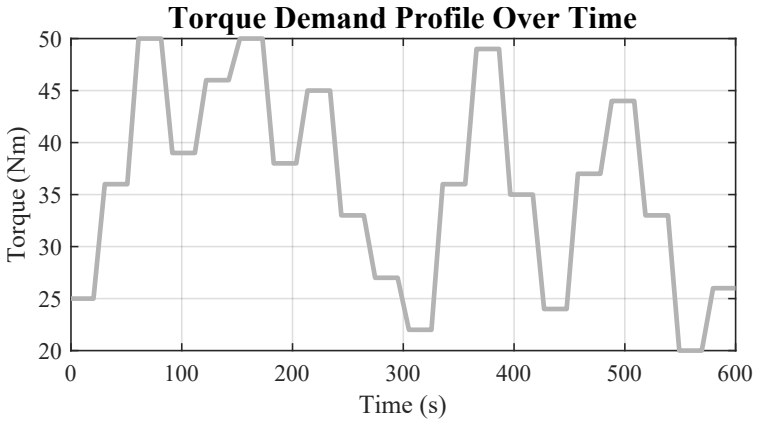


Figure 5.18: Example of time varying dynamic input torque stress profile over time for the three-phase induction motor model.

Based on torque demands, the system model responds by adjusting the module gating signals according to the set demand point within the control modulation scheme. The torque change directly influences the electrical loss characteristics, which affect the thermal dynamics of the module-to-thermal network. The junction temperature of the module varies, as shown in Figure. 5.19, demonstrating fluctuations ranging from low to high frequencies. The overall trend in junction temperature is predominantly influenced by the demanded torque, with high-frequency cycles primarily resulting from fast switching behaviors and the associated losses incurred through switching and conduction.

Having established a logical framework, a thorough comparison study of two different torque demand profiles has been studied and presented. Figure. 5.20 illustrates the torque demand profiles, one showing significant fluctuation over time whereas the other showing a steady, fixed value over time. Even though the two torque profiles have the same mean, it can be observed that Profile 1 demonstrates more severe temperature fluctuation than that of Profile 2, leading to lower lifetime due to higher cumulative damage over time. This visual representation allows for a direct comparison between the torque applied and the resulting impacts on the semiconductor device's aggregated lifetime. The graph reveals that a higher

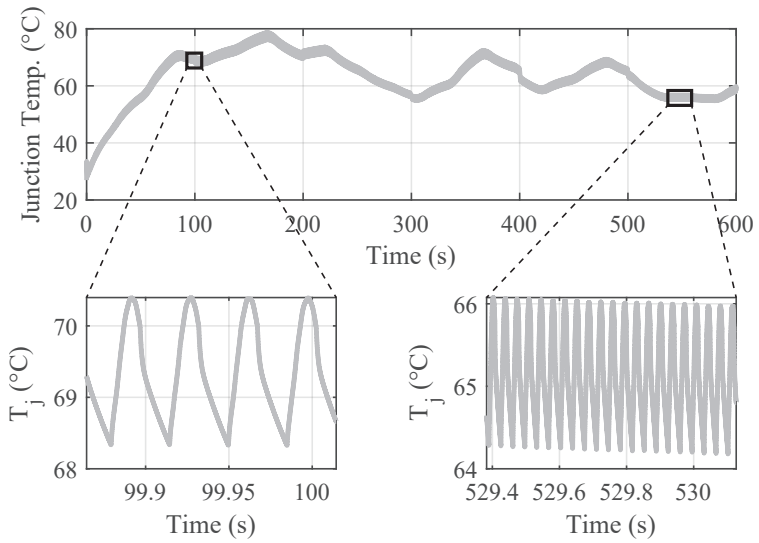


Figure 5.19: Junction temperature output response based on the torque demand profile from Figure. 5.18.

ΔT and $\overline{T}$ value correlates with a reduction in the cumulative lifetime during that specific period as it can be seen in (5.23). This is attributed to the increased operational stress on the module, elevating the mean junction temperature and the frequency of peak-to-peak temperature cycles.

In contrast, a steady trend in torque demand can be associated with an increase in the cumulative lifetime. This improvement is due to reduced stress on the module, leading to lower mean junction temperatures and fewer temperature fluctuations during such periods. These trends, though general, can be used to see the impact of a step-change to the cumulative time as well as to understand how other variations in operational demands affect the longevity and reliability of semiconductor devices.

This proposed approach can enable a more comprehensive evaluation of the aggregate lifetime calculation's sensitivity as more historical data becomes available. The analysis can be used to consider other various approaches, including the application of an exponential weighting to recent data, enhancing the accuracy of the lifetime calculations [352].

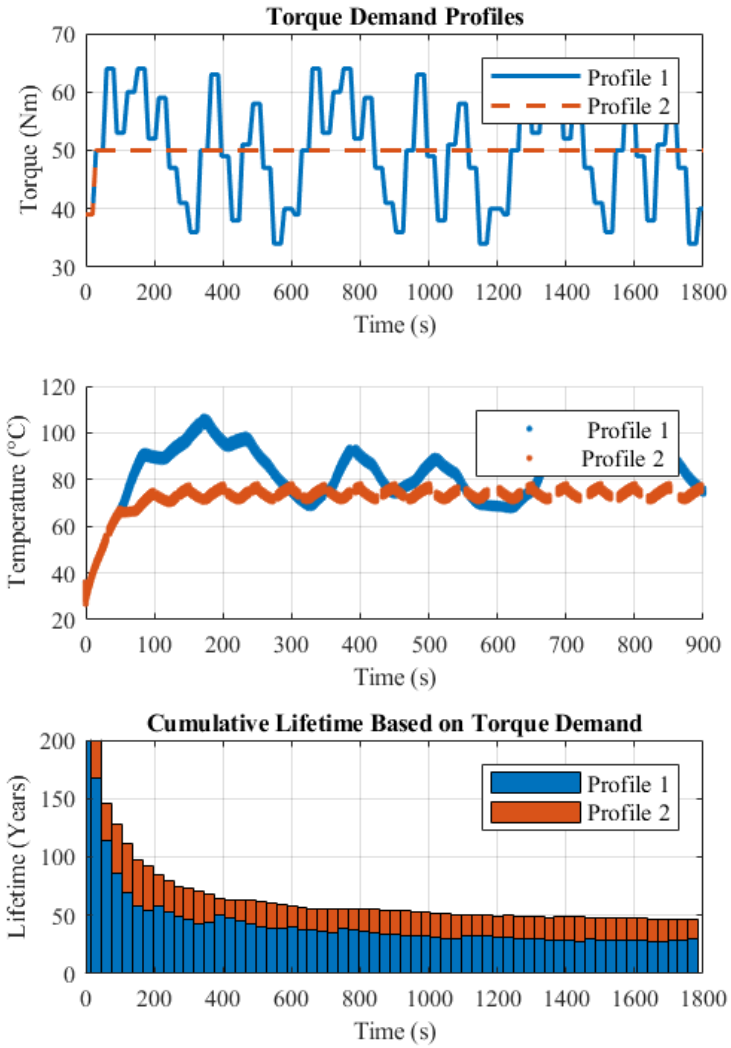


Figure 5.20: Real-time cumulative lifetime calculation based on two different different torque profiles. Profile 1 shows more fluctuating torque profile whereas Profile 2 is steady throughout the entire simulation duration of 30 minutes. The mean torque over time is the same for both profiles yet there are distinguishable differences in both temperature and cumulative lifetime calculation.

The algorithm can be configured to provide real-time feedback on the device's status and health, enabling immediate adjustments to simulation parameters if necessary. This capability ensures that the testing and validation processes remain as close to real operational conditions as possible, thereby enhancing the predictive maintenance strategies and extending the service life of semiconductor devices.

By integrating machine learning into the HIL framework, the predictive maintenance system can achieve greater accuracy, adaptability, and foresight in maintaining semiconductor devices. This advancement can enhance the accuracy and timeliness of failures with these critical components while highlighting the need for automation in electronic system diagnostics and maintenance [353, 354].

5.2.2 Deep Neural Network Fusion Model for Lifetime Estimation

Power devices require extensive characterization across electrical and thermal domains to meet qualification standards (e.g., AEC-Q100). These measurements range across steady-state and dynamic conditions, producing diverse datasets such as static I-V sweeps, switching transients, and temperature-dependent behavior. While only subsets of these measurements are included in the manufacturer datasheet, an active datasheet would provide more detailed and higher-dimensional specifications and characteristics of the device.

Furthermore, conventional compact or physics-based models often rely on simplified parameter sets and cannot capture the full extent of device variability. Such models typically omit metadata and secondary influences like test setup, handling, and operator-induced variability. Though not directly linked to device physics, external environmental factors can affect the measurements. In fact, process-induced variations, material inconsistencies, and uncontrolled environmental exposures can lead to unmodeled system-level performance shifts [355].

These limitations motivate the use of data-driven modeling techniques capable of learning from high-dimensional, multi-modal datasets that include both scalar descriptors and measurement sequences. Deep learning models have demonstrated promising potential in core loss modeling in magnetic components [356, 357], lithium-ion battery state-of-charge

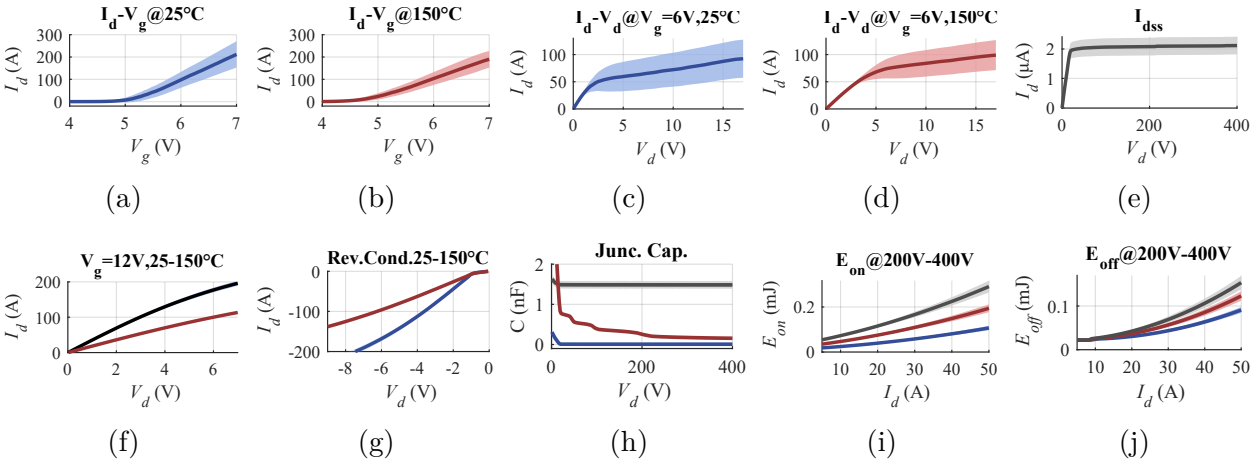


Figure 5.21: Device static and dynamic characterization measurement results showing the population median (solid line) and interquartile range (IQR) (shaded region): (a) transfer characteristic (I_d–V_g) at 25, (b) I_d–V_g at 150, (c) output characteristic (I_d–V_d) at $V_g = 6$ V and 25, (d) I_d–V_d at $V_g = 6$ V and 150, (e) drain-to-source leakage current (I_{dss}) from V_d of 0 V to 400 V, (f) I_d–V_d at $V_g = 12$ V and 25, (g) I_d–V_d at $V_g = 12$ V and 150, (h) junction capacitances (C_{iss}, C_{oss}, C_{rss}), (i) turn-on switching loss (E_{ON}) at V_d of 200 V, 300 V, and 400 V with drain current ranging from 0 A to 50 A, and (j) turn-off switching loss (E_{OFF}) under the same conditions as (i).

estimation [358, 359], and characteristic prediction in FETs [360, 361], and reliability of solder joints [362]. However, there remains challenges with the integration of multi-modal measurements with embedded process variability from a sample population.

The acquired dataset comprises both static and dynamic electrical measurements across different temperatures and operational voltage or current conditions. These tests include drain-to-source leakage current (I_{dss}), input capacitance (C_{iss}), output capacitance (C_{oss}), reverse transfer capacitance (C_{rss}), turn-on and turn-OFF switching energies (E_{ON}, E_{OFF}), as well as static output (I_d-V_d), transfer (I_d-V_g), and reverse conduction characteristics (I_s-V_s) at both 25°C and 150°C. The junction-to-case thermal resistance ($R_{\theta JC}$) was also extracted to evaluate thermal characteristic. Representative static and dynamic measurement results are summarized in Figure. 5.21. This highlights the diversity and range of the measured parameters across over 150 device samples with real-world variability due to process dispersion

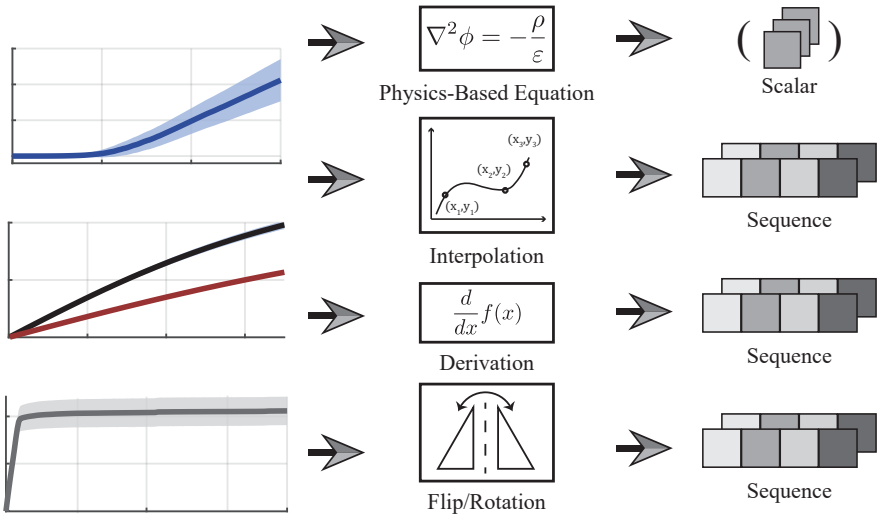


Figure 5.22: Illustration of the feature engineering process to transform raw measurement data into machine learning–input features through applying physics-based equations to extract device parameters (e.g., Q_{oss}, V_{mil}, R_{ON}, V_{th}), interpolating raw data for uniform sampling, computing derivatives of discrete measurements, and augmenting data via axis flipping and rotation.

and material inconsistencies.

To enhance data diversity and improve generalization during model training, the measurements were transformed into structured input features through a multi-stage feature engineering process as illustrated in Figure. 5.22. First, physics-based equations were applied to the measurements to derive additional relevant parameters such as output charge (Q_{oss}), reverse recovery charge (Q_{rr}), threshold voltage (V_{th}), and on-state resistance (R_{ON}). In addition, interpolation was performed across the dataset to realize uniform sampling resolution across all samples for consistent neural network input dimension formatting. To capture hidden inflection characteristics and amplify subtle variations, numerical derivatives (e.g., di/dv, d^2i/dv^2) were computed from discrete measurements. Lastly, data augmentation techniques such as axis flipping (e.g., mirroring I-V curves) and rotation were applied to generate synthetic samples and to allow alternate sequence representations such as transforming voltage-based curves to current-based.

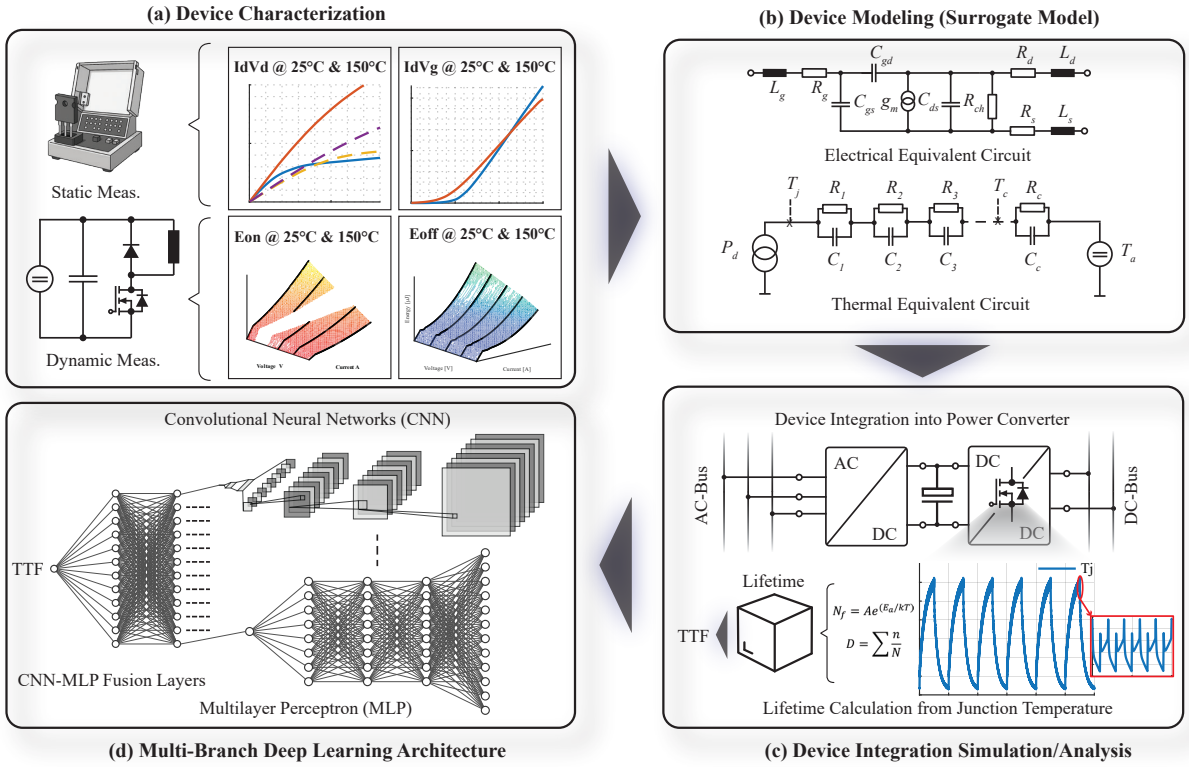


Figure 5.23: Overview of the proposed data-to-model framework to illustrate the process between device characterization, surrogate model development, converter-level simulation for lifetime estimation, and multi-branch deep learning model development.

The proposed data-to-model framework integrates multi-domain device characterization, surrogate modeling, converter-level simulation with lifetime evaluation, and machine learning model development. As illustrated in Figure. 5.23, the workflow steps through the following stages, including (a) comprehensive static and dynamic electrical parameters are measured under multiple operating conditions across a device population, capturing variability from manufacturing processes and material inconsistencies, (b) based on these measurements, electrical and thermal surrogate models are developed within a simulation environment to replicate actual device behavior while embedding the observed variability, (c) the surrogate models are then integrated into system-level power converter simulations to estimate mission-profile–dependent junction temperature (T_j) waveforms, which are used to com-

pute lifetime estimates using physics-of-failure models [363] and fatigue modeling including Coffin-Manson–based cycle-to-failure calculations and rainflow counting for damage accumulation [364], and (d) the input features derived from experimental measurements and output lifetime labels generated through simulation are used to train a multi-branch deep neural network. This framework processes heterogeneous data modalities and learns nonlinear mappings from high-dimensional feature spaces to low-dimension scalar values, thereby correlating baseline behaviors to predicted lifetime. Once trained, the model eliminates the need for repeated model development and converter-level simulations to extract junction temperatures. Thus, it can be deployed as an inference-based quality control tool that correlates unique measured device characteristics with expected lifetime or remaining useful life (RUL) prediction.

The proposed architecture, depicted in Figure. 5.24, merges two heterogeneous input modalities of sequence data and scalar features. The sequence data is interpolated using a Lagrange interpolant down to a uniform 100-timestep representation. These signals are stacked into a block of features as independent channels and processed through 3 1D-convolution layers with ReLU activations using a window size of 7 for the convolution kernel, with no padding. These choices were determined through an ablation study that balances model expressiveness and computational efficiency.

In parallel, scalars are stacked into a vector and passed through a MLP with two hidden layers with ReLU activations. The outputs of the CNN and MLP branches are concatenated and passed through an additional MLP layer and a final weight matrix to produce the lifetime prediction, which is described in Algorithm 4. These choices have shown effective learning outcomes even on limited datasets, offering a lightweight alternative to more data-intensive attention-based architectures.

Training was performed on a single NVIDIA A100-SMX4 GPU (40 GB) using Adam opti-

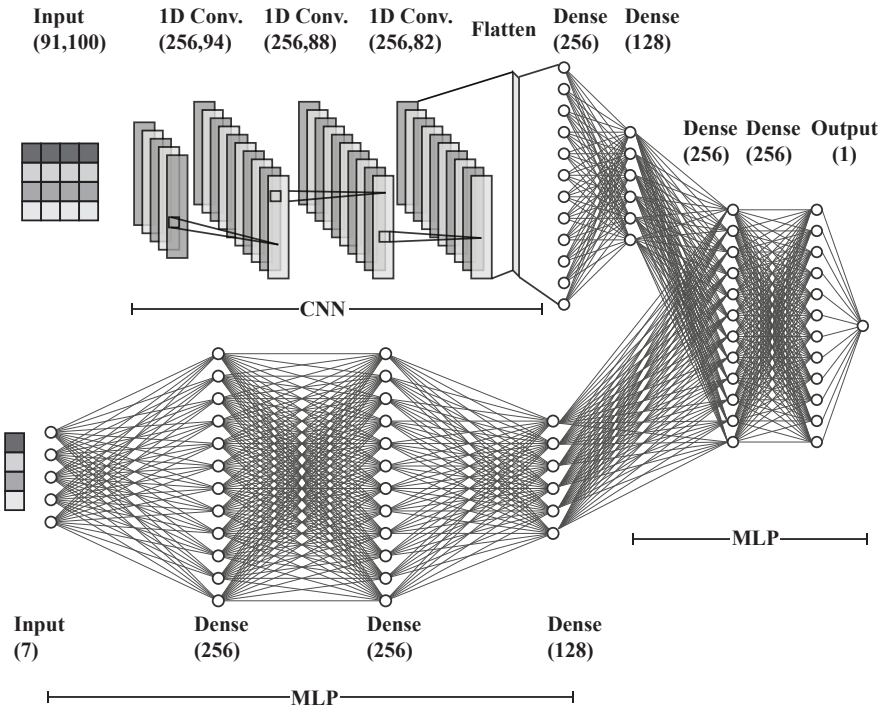


Figure 5.24: Proposed multi-modal deep neural network fusion model for predicting device lifetime based on raw measurement data and engineered features derived through the feature engineering pipeline.

mizer with a learning rate of 0.0001 over 100,000 epochs, and the batch size was set equal to the entire training data.

Figure. 5.25(a) illustrates the baseline performance using single-modality inputs, which only uses either the scalar features through the MLP or the sequence data through the CNN. The resulting scatter plots include error bars representing the semi-interquartile range (IQR/2) to capture feature-level dispersion. The single-modality model achieved a median MSE of 1.54 on the training set and 74.7 on the test set, which indicated limited generalization when relying on isolated data sources.

Figure. 5.25(b) presents the results from the proposed multi-feature deep fusion network, which integrates 91 interpolated sequence features and 7 scalar features. The proposed configuration yielded an MSE of 0.12 on the training set and 2.06 on the test set, >30× en-

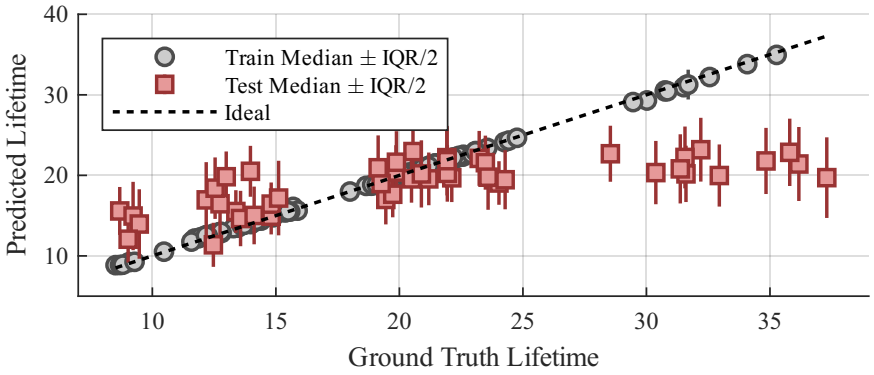
Algorithm 4 Multi-Modal CNN–MLP Fusion Network Model

// Convolutional Neural Network Branch
$\mathbf{h}^{(0)} \leftarrow \mathbf{x}_{\text{seq}} \in \mathbb{R}^{T \times D}$
for $l = 1$ to L_c **do** ▷ number of CNN layers
  for $i = 0$ to $T_l - k$ **do**
    $y_i^{(l)} \leftarrow \sum_{j=0}^{k-1} \mathbf{h}^{(l-1)}[i+j] \cdot \boldsymbol{\omega}_j^{(l)}$
    $z_i^{(l)} \leftarrow \text{ReLU}(y_i^{(l)})$
  end for
  $\mathbf{h}^{(l)} \leftarrow [z_0^{(l)}, \ldots, z_{T_l-k}^{(l)}]$
end for
$\mathbf{z}_{\text{CNN}} \leftarrow \sigma(\mathbf{W}_{\text{cnn}} \cdot \text{Flatten}(\mathbf{h}^{(L_c)}) + \mathbf{b}_{\text{cnn}})$
// Multilayer Perceptron Branch
$\mathbf{h}^{(0)} \leftarrow \mathbf{x}_{\text{scalar}} \in \mathbb{R}^{S}$
for $l = 1$ to L_m **do** ▷ number of MLP layers
  $\mathbf{h}^{(l)} \leftarrow \sigma(\mathbf{W}^{(l)} \cdot \mathbf{h}^{(l-1)} + \mathbf{b}^{(l)})$
end for
$\mathbf{z}_{\text{MLP}} \leftarrow \mathbf{h}^{(L_m)}$
// Multi-Modality Fusion MLP Branch
$\mathbf{z}_{\text{fused}} \leftarrow [\mathbf{z}_{\text{CNN}} \,||\, \mathbf{z}_{\text{MLP}}]$
$\mathbf{h}_{\text{fused}} \leftarrow \sigma(\mathbf{W}_f \cdot \mathbf{z}_{\text{fused}} + \mathbf{b}_f)$
$\hat{y} \leftarrow \mathbf{W}_o \cdot \mathbf{h}_{\text{fused}} + \mathbf{b}_o$
return $\hat{y}$

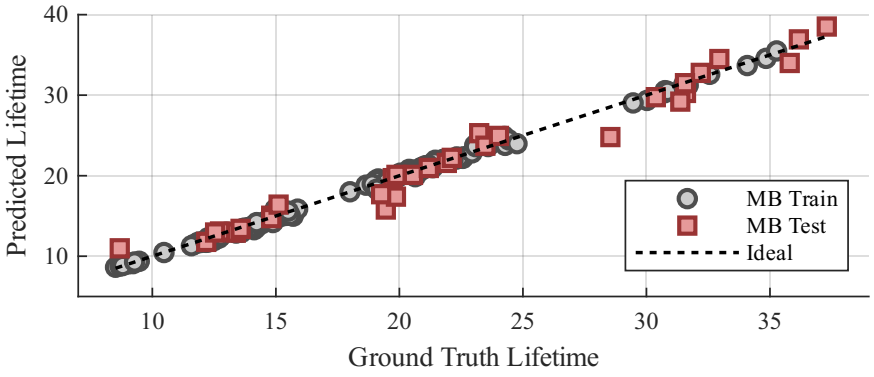
hancement over the single-modality in the device lifetime prediction. The reduction in test and train error illustrates the proposed model's ability to generalize across high-dimensional, heterogeneous inputs and capture complex relationships between device behavior and predicted lifetime.

This fusion-based approach not only outperforms single-branch architectures but also enables inference-driven lifetime prediction from standard characterization data.

Fig. 5.26 shows model training performance across epochs. Fig. 5.26(a) illustrates the MSE performance and Fig. 5.26(b) depicts the MAE performance for both the training and validation sets. In both metrics, the losses decrease steadily and the validation curves track the training curves without late-epoch divergence, indicating effective regularization rather



(a)

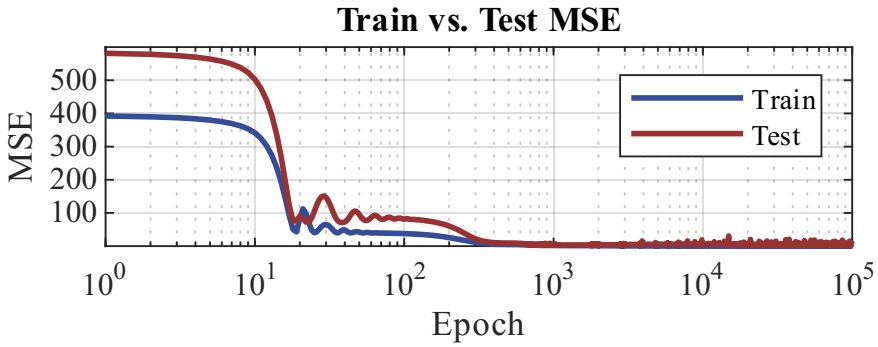


(b)

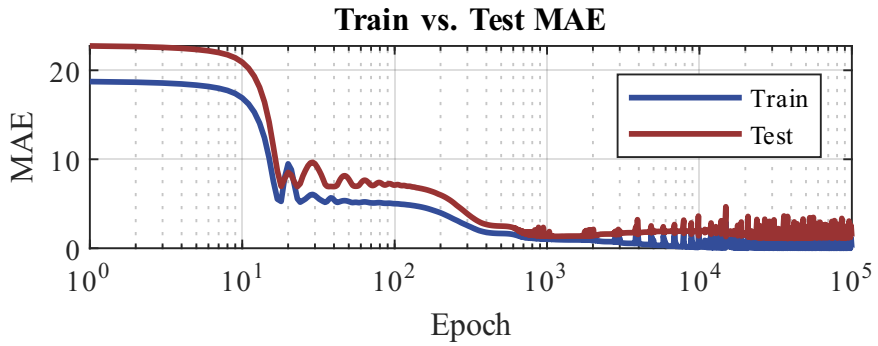
Figure 5.25: Comparison of lifetime prediction performance: (a) baseline results using single-branch models using CNN for sequence data and MLP for scalar features with median errors and IQRs across all features and (b) improved accuracy using the proposed multi-branch fusion network combining CNN and MLP inputs

than memorization. Residuals are approximately zero-mean across the label range with reduced variance for the fusion model, and high-magnitude outliers are substantially fewer than in the single-modality baseline. This suggests that the proposed architecture and training procedure are well conditioned, with sufficient capacity and regularization to ensure stable convergence and strong generalization to unseen devices and operating conditions.

These results indicate that sequence morphology captures switching/thermal dynamics not recoverable from scalar features alone, while physics-aware scalars provide complementary low-dimensional structure that aids learning in limited-data regimes. Consequently, the fu-



(a)



(b)

Figure 5.26: Training and validation mean squared error (MSE), shown in (a) and mean absolute error (MAE) illustrated in (b) as a function of epoch. The decreasing test losses demonstrate progressive model convergence and generalization behavior.

sion model's accuracy and calibration enable inference-time lifetime prediction directly from standard characterization data, removing the need to rebuild surrogates or rerun converter-level simulations for each new part. In rapid prototyping, this provides an immediate mapping from baseline device measurements to converter-level lifetime under specified mission profiles, supporting inspection screening and sensitivity analyses, which can significantly shorten iteration cycles for device production and system-level integration.

Several natural extensions of this work include real-time degradation signals, where the model integrates in situ observables (e.g., drift in $E_{\text{on/off}}$, R_{ON}, V_{th}, gate leakage, and off-state I_{DSS}). These signal streams can be fused with the device baseline measurements to deliver

rolling RUL estimates and enable prognostics and health management during operation. Moreover, uncertainty and risk studies can be performed with predictive intervals that are strengthened through heteroscedastic likelihoods or quantile regression and calibrated via conformal prediction with finite-sample coverage. Integrating systematic test-to-failure tests (e.g., accelerated power cycling, HTRB/H3TRB) into the training and validation loop will improve lifetime labels to ground truth, validate physics-of-failure assumptions, and surface predictive features not captured by current surrogates and prediction capabilities.

5.3 Summary

This chapter presented several integrated framework and analyses for optimization and lifetime analysis of power electronic systems employing high performance WBG devices. A multi-objective optimization methodology via genetic algorithm was used to optimize electrical efficiency, converter volume, thermal performance, and projected device lifetime. The approach was demonstrated on traction inverter and its design parameters. Moreover, high-voltage diode co-design study based on operating regime was demonstrated to link the UWBG and WBG device-level characteristics with converter-level performance metrics through detailed physics-based models.

Advanced lifetime analysis techniques were explored; one approach enabled the estimation of RUL of power devices based on the real-time junction temperature monitoring signals acquired by the hardware-in-the-loop (HIL). In addition, multi-modal deep learning approach demonstrated improved lifetime prediction compared to the single modal approaches. The methodologies outlined in this chapter provide innovative ways to optimize WBG device properties and characteristics based on their converter application behaviors and environments.

Chapter 6

Conclusion and Outlook

This chapter summarizes the research objectives, proposed approaches, and key findings presented in Chapters 2–5, and discusses their implications for the seamless integration of WBG devices into high-performance power electronic systems. Section 6.1 provides a comprehensive overview of the contributions, methodologies, and results, highlighting how the proposed approaches address the limitations identified in the introductory and background discussions of Chapter 1 and Chapter 2. Section 6.2 outlines prospective research directions and potential extensions of the work presented in this dissertation by identifying opportunities to adapt the developed techniques to emerging technologies and broaden the application scope.

6.1 Summary

This dissertation addressed the challenges of integrating WBG semiconductor devices into high-performance power electronic systems by advancing the physical and electrical understanding of device behavior, developing specialized measurement, inspection, and qualification techniques, optimizing device design and operating parameters in the context of converter-level performance and behavior, and introducing both HIL and AI-driven predictive modeling capabilities for reliability assessment. The research contributions encompass device-level characterization, converter-level stress evaluation, and system-level co-design

and optimization.

Chapter 1 outlined the motivation and objectives of this dissertation by demonstrating the need for improved modeling, characterization, optimization, and reliability evaluation methodologies to enable the seamless integration of WBG devices into power electronic applications. It summarized the main contributions that address the identified challenges across material, component, subsystem, and system levels, with specific references to relevant publications associated with each body of work.

Chapter 2 provided the background and literature review to guide the research presented in this dissertation. It examined three core areas: the fundamental properties of WBG materials and their implications for device performance, advanced characterization and measurement techniques, and system-level optimization strategies for power electronic applications. The chapter reviewed SOA approaches to device modeling, measurement, screening and qualification, optimization, and lifetime prediction, highlighting their limitations in capturing the effects of dynamic stress conditions induced by WBG switching waveforms. Such stresses that are characterized by rapid voltage and current slew rates, AC operational modes, and complex interactions with source and load dynamics, pose distinct internal and external reliability challenges. The discussion established that improved modeling frameworks, advanced hardware capabilities, integrated optimization analyses, and lifetime prediction capabilities are required to enhance understanding of device physical behavior, dynamic measurement characteristics, and converter-level operating conditions.

Chapter 3 presented the classification and evaluation of dynamic switching stresses across various power conversion topologies, as summarized in Table 3.1 by converter class, switching voltage levels, current waveform shapes, and switching schemes (e.g., hard- vs. soft-switching). GaN HEMT device structures were examined in detail, as dynamic stress conditions can exacerbate hot-carrier injection and charge trapping, leading to measurable in-

creases in dynamic on-resistance during switching transitions. An extensive literature review showed that these degradation mechanisms are quantitatively linked to waveform characteristics such as voltage and current magnitudes, switching frequency, stress duration, and environmental conditions including temperature and radiation exposure, as illustrated in Figure 3.3. The DFC structure, shown in Figure 3.4, was analyzed to illustrate how increased slew rates intensify localized electric fields across field plates, accelerating degradation mechanisms. These results demonstrate that dynamic stresses produce non-uniform electric field distributions within the device structure, which are the effects that static or DC-based assessments do not capture.

Chapter 4 introduced advanced characterization, screening, and qualification methodologies to enable precise, non-destructive evaluation of WBG devices under application-relevant conditions. The proposed OVMC topology allows high-fidelity V_{ON} capture during fast-switching transients without saturating measurement instrumentation, resulting in 99% measurement accuracy, a 2× increase in resolution, and a 40 ns reduction in response time. Furthermore, a non-destructive inspection framework for GaN HEMTs was developed using small-signal gate excitation combined with PCA and k-means clustering to classify device populations based on structural and electrical response signatures. This approach achieved group identification within a 95% CI across all device characteristics, potentially mitigating up to 3% efficiency deviation caused by inherent device-to-device variability. Lastly, a flexible, scalable, and adaptable automated test system was designed to execute long-duration, high-speed switching stress protocols with real-time monitoring and data logging, enabling enhanced WBG reliability assessment under dynamic stress conditions, which are representative of high-performance power electronic system environments.

Chapter 5 focused on system-level co-design and optimization strategies, along with advanced lifetime analysis methodologies, for WBG-based power electronic systems. A multi-

objective optimization framework integrating WBG device characteristics into EV traction inverter design demonstrated up to a 98% efficiency while maintaining a projected lifetime of 300,000 miles and a total converter volume of $\leq$1 L. A HIL–based real-time lifetime estimation framework was developed to enable RUL prediction, detecting a 5% RUL difference between two mission profiles with the same average torque demand, an outcome that would not be challenging to quantify without HIL-based algorithm computation. In addition, a DNN fusion model combining scalar parameters with sequential switching and thermal waveforms improved lifetime prediction improvement of up to 30$\times$ in test MSE compared to baseline single-branch models.

6.2 Outlook

While this dissertation has made significant advances in modeling, characterization, and lifetime prediction of WBG devices, several promising directions remain for future work:

- **Physics-Informed Digital Twin Modeling of Dynamic On-Resistance:** Future research direction can focus on developing a physics-informed digital twin of the underlying physical phenomena to model and predict the evolution of trapping effects and long-term degradation under complex operating conditions. This digital twin approach will integrate first-principles device physics, such as electrothermal coupling, trap kinetics, and surface/buffer charge dynamics, with data-driven learning models [354, 365] trained on extensive experimental datasets obtained from both controlled stress tests and application-representative mission profiles. The main benefit of this approach will be its ability to deliver high-fidelity behavior modeling and predictions of dynamic on-resistance behavior across diverse operating scenarios. This approach can ultimately reduce the need for overly conservative design margins, supporting the development of

mitigation strategies, and strengthening the overall reliability of the converter.

- **Deep Learning–Based Lifetime Uncertainty Quantification:** Developing a deep learning framework that predicts device or converter lifetime while quantifying the uncertainty of those predictions under a set of defined operating conditions can be proposed. Building upon recent advances in probabilistic deep learning and operator learning [366, 367], this approach can integrate Bayesian neural networks, ensemble methods, and mixture distribution modeling to capture both epistemic (model-related) and aleatory (data-related) uncertainties. Multi-modal degradation signals, including threshold voltage shift, thermal cycling data, dynamic switching waveforms, and mission-profile histories, will be mapped to probability distributions over lifetime metrics rather than single point estimates. To ensure physically meaningful confidence bounds, the architecture will embed stress–lifetime acceleration laws, electrothermal coupling models, and trap kinetics as inductive biases. Methods such as mixture location–scale distributions [368] can be explored to handle multiple degradation modes without explicit failure-mode labeling. Furthermore, Deep Operator Networks (DeepONets) [369] can be employed to learn the mapping from complete degradation histories to lifetime distribution parameters, enabling nonlinear relationship across mission profiles and device types.

- **Standardization of WBG Test Protocols:** Ongoing standardization within the JEDEC JC-70 Wide Bandgap Power Electronic Conversion Semiconductors committee [370], which consists of subcommittees JC-70.1 for GaN and JC-70.2 for SiC, seeks to incorporate the latest, results-driven methods to deliver consistent test, characterization, and qualification practices for WBG devices. Current variation in test circuit topology, stress waveform definition, and failure criteria still brings significant challenges for consistent comparison and reliable extrapolation across different device struc-

tural types and end-use applications. Building on this dissertation's contributions on dynamic stress evaluation methodologies, unified protocols can be developed to characterize transient reliability in WBG devices [371, 372]. Dynamic switching stresses, such as voltage overshoot, high dv/dt and di/dt, and resonant ringing, can induce peak electric field crowding, accelerate trapping, and exacerbate degradation in field-control structures (e.g., field plates) and dielectric layers. However, existing test practices for evaluating these effects vary widely in circuit topology, stress waveform definition, and failure criteria, resulting in inconsistent reliability data and limited comparability for cross-referencing. Thus, a standardized protocol defining application-relevant transient stress conditions, along with measurement timing, resolution requirements, and reporting guidelines, would improve reproducibility and ensure results are representative. The protocol should account for device-to-device variability from manufacturing tolerances, handling, and storage to further support reproducible and representative procedure.

Appendices

Appendix A

Cascode Current Mirror Derivations

A.1 Cascode Transfer Ratio Analysis

a detailed current output transfer ratio analysis of the current mirror circuit is presented. Calculating the current transfer ratio, denoted as K, is critical, as the transfer ratio defines the relationship between the reference current (I_{REF}) and the output current (I_s), which is essential for predicting the behavior and precision of the current mirror. This analysis can provide a theoretical understanding of how the circuit replicates the reference current in the output branch, ensuring that the output current meets the desired specifications to drive the measurement circuit.

In the subsequent analysis, we operate under the assumption that all BJT transistors are biased in their active region. This operational state is governed by the following equations:

$$V_{EB} > 0,$$

$$V_{CB} < 0,$$

$$I_E = I_{sat,B}\left(e^{\frac{V_{EB}}{V_T}} - 1\right),$$

where $I_{sat,B}$ is the BJT saturation current and V_T is the thermal voltage ($V_T \approx 26$ mV at room temperature).

To find the current transfer ratio K, the two separate branches of current paths, denoted as I_A and I_B, need to be calculated in terms of the reference current I_{REF}. The emitter, base, and collector currents of Q_1 and Q_3 can be determined using (A.1)-(A.3) to derive I_A, expressed in (A.4):

$$I_{E_1} = I_{\text{REF}} = I_{C_1}\left(1 + \frac{1}{\beta}\right), \tag{A.1}$$

$$I_{E_3} = I_{C_1} + \frac{2I_{C_1}}{\beta} = I_{C_1}\left(1 + \frac{2}{\beta}\right), \tag{A.2}$$

$$I_{C_3} = \frac{I_{E_3}}{1 + \frac{1}{\beta}} = \frac{I_{C_1}\left(1 + \frac{2}{\beta}\right)}{1 + \frac{1}{\beta}}, \tag{A.3}$$

$$I_A = I_{C_3}\left(1 + \frac{2}{\beta}\right) = \frac{I_{C_1}\left(1 + \frac{2}{\beta}\right)^2}{1 + \frac{1}{\beta}} = \frac{I_{\text{REF}}\left(1 + \frac{2}{\beta}\right)^2}{\left(1 + \frac{1}{\beta}\right)^2}. \tag{A.4}$$

Similarly, the I_B current branch can be determined by calculating the base, emitter, and collector currents of Q_2 and Q_4. In the cascode current mirror configuration with PNP transistors, the emitter current of transistor Q_2 (I_{E_2}) is approximately equal to the reference current (I_{REF}):

$$I_{E_2} = I_{E_1} \approx I_{\text{REF}}. \tag{A.5}$$

This relationship, expressed in (A.5), arises because Q_1 is diode-connected, setting a stable reference current. The precise matching of the device parameters and the high output impedance provided by the cascode configuration should minimize the impact of variations in the load and ensure that the reference current is accurately mirrored by the subsequent

transistors. Thus, the emitter current I_{E_2} closely follows I_{REF}, maintaining the desired current transfer characteristics of the circuit. Therefore, assuming matched transistors and carefully neglecting second-order effects, the current through Q_1 mirrors the reference current through Q_2.

Based on the similar analysis provided for I_A, the current through the branch I_B can be derived by determining the collector current of Q_2 (I_{C_2}) as expressed in (A.6) and (A.7):

$$I_{C_2} = \frac{I_{\text{REF}}}{1 + \frac{1}{\beta}}, \tag{A.6}$$

$$I_B = I_{C_2}\left(1 + \frac{1}{\beta}\right) = \frac{I_{\text{REF}}}{\left(1 + \frac{1}{\beta}\right)^2}. \tag{A.7}$$

The output current (I_s) is the sum of I_A and I_B and by substituting the equations for I_A and I_B in (A.4) and (A.7) respectively, the output current can be expressed in (A.8):

$$I_s = I_A + I_B = \frac{I_{\text{REF}}\left(1 + \frac{2}{\beta}\right)^2}{\left(1 + \frac{1}{\beta}\right)^2} + \frac{I_{\text{REF}}}{\left(1 + \frac{1}{\beta}\right)^2}. \tag{A.8}$$

The output current relative to the reference current is:

$$K = \frac{I_s}{I_{\text{REF}}} = \frac{\left(1 + \frac{2}{\beta}\right)^2 + 1}{\left(1 + \frac{1}{\beta}\right)^2} = 2\left(1 + \frac{1}{(\beta + 1)^2}\right). \tag{A.9}$$

Assuming $1/(\beta + 1)^2 \approx 0$, this equation confirms that the output current is approximately twice ($K = 2$) the reference current. Moreover, from (A.9), it can be deduced that this configuration theoretically eliminates the effect of the current gain, β, when using a typical

β value of 100 or greater, whereas other current mirror configurations can be impacted by current gain dependence as well as sensitivity. For instance, in this configuration, when $\beta = 100$, the output current is only impacted by less than 0.02% of the reference current.

The reference current, I_{REF}, is determined by the resistors R and R_1, the supply voltage V_{cc}, the voltage at the load node v_s, and the emitter-base voltage drops (V_{EB}) of the PNP BJT transistors. I_{REF} can be mathematically formulated as follows:

$$I_{\text{REF}} = \frac{V_{cc} - v_s - 2V_{EB}}{R + R_1}. \tag{A.10}$$

A.2 Cascode Output Impedance Analysis

The small-signal output impedance, $r_x = v_x/i_x$, of the cascode current mirror can be derived by considering the small-signal parameters of the transistors, such as the transconductance (g_m), the input impedance looking into the base (r_π), and the output resistance (r_o). These parameters play a key role in defining the overall impedance, as they influence how the transistors respond to small-signal variations in the circuit.

The equations expressed in (A.11)-(A.15) describe Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) around various nodes in the equivalent small-signal model shown in Fig. A.1. To derive the overall output impedance of the circuit, isolating the i_x and v_x variables is required through further algebraic manipulation. This involves combining and rearranging the equations to factor out these variables, ultimately allowing us to derive the expression for the small-signal output impedance, r_x.

First, the current at nodes i_x, i_2, and i_4, as illustrated in Fig. A.1(a), are expressed by the following equations (A.11) to (A.14):

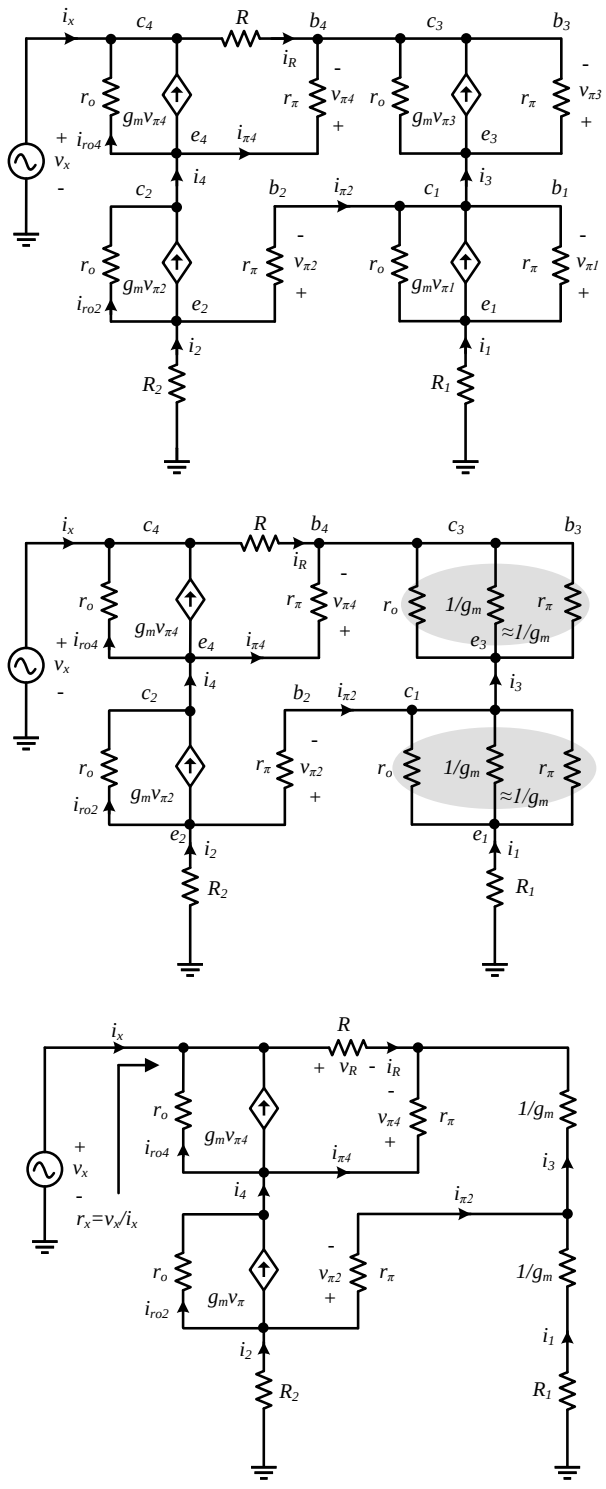


Figure A.1: Small-signal analysis of the proposed cascode current mirror: (a) output resistance model using hybrid-π small-signal representation, (b) intermediate reduced network, and (c) final equivalent output impedance circuit.

$$i_x = i_3 + i_4, \tag{A.11}$$

$$i_4 = g_m v_{\pi 4} + i_{\pi 4} = i_{\pi 4}(g_m r_\pi + 1), \tag{A.12}$$

$$i_{\pi 4} = -i_R - i_3, \tag{A.13}$$

$$i_2 = v_{\pi 2}\left(g_m + \frac{1}{r_\pi}\right), \tag{A.14}$$

$$v_{\pi 2} = -i_2 R_2 + \left(\frac{1}{g_m + 1/r_\pi} + R_1\right) i_1. \tag{A.15}$$

Substituting $v_{\pi 2}$ from (A.15) into (A.14) results in the expression shown in (A.16):

$$i_2 = \left(g_m + \frac{1}{r_\pi}\right)\left(-i_2 R_2 + \left(\frac{1}{g_m} + R_1\right) i_1\right). \tag{A.16}$$

Rearranging the terms to solve for i_2/i_1, the following expression is obtained:

$$\frac{i_2}{i_1} = \frac{1 + \left(g_m + \frac{1}{r_\pi}\right) R_1}{1 + \left(g_m + \frac{1}{r_\pi}\right) R_2}, \tag{A.17}$$

which can be simplified to (A.18) under the assumption that $1/g_m \ll r_\pi$:

$$\frac{i_2}{i_1} \approx \frac{R_1}{R_2}. \tag{A.18}$$

If $R_1 = R_2$, then $i_1 = i_2$.

A similar process can be applied to relate i_3 and i_4 using the current $i_{\pi 2}$ as shown in equations (A.19)-(A.20):

$$i_3 = i_4 + 2i_{\pi 2}, \tag{A.19}$$

$$\begin{aligned} v_{\pi 2} &= -R_2 i_2 + i_1 \left(R_1 + \frac{1}{g_m} \right) \\ &= i_2 \left(R_1 - R_2 + \frac{1}{g_m} \right) = i_{\pi 2} r_{\pi 2}. \end{aligned} \tag{A.20}$$

If $R_1 = R_2$, then (A.20) can be rearranged as:

$$\frac{i_{\pi 2}}{i_2} = \frac{1/g_m}{r_{\pi 2}}, \tag{A.21}$$

where $i_{\pi 2} \approx 0$ under the assumption that $1/g_m \ll r_\pi$, which simplifies (A.20) to the following expression:

$$i_3 = i_4. \tag{A.22}$$

Now, combining the relationships from (A.12) and (A.13) for i_4 and i_R, (A.23) can be obtained as follows:

$$i_4 = -(i_4 + i_R)(g_m r_\pi + 1). \tag{A.23}$$

The expression (A.23) can be further simplified to solve for i_4/i_R as illustrated in (A.25):

$$i_4(g_m r_\pi + 2) = -i_R(g_m r_\pi + 1), \tag{A.24}$$

$$\frac{i_4}{i_R} = -\frac{(g_m r_\pi + 1)}{(g_m r_\pi + 2)} \approx -1. \tag{A.25}$$

Since $i_4/i_R = -1$, the following expression can be used to calculate the voltage v_x in terms of i_3:

$$\begin{aligned} v_x &= i_R R - i_3 \left(\frac{2}{g_m} + R_1 \right) \\ &= -i_3 R - i_3 \left(\frac{2}{g_m} + R_1 \right) \\ &= -i_3 \left(R + R_1 + \frac{2}{g_m} \right). \end{aligned} \tag{A.26}$$

For the total current i_x, the equation in (A.11) can be simplified to (A.27) since $i_3 = i_4$:

$$i_x = -2i_3. \tag{A.27}$$

Now, by solving for i_3 from (A.27) and substituting it into (A.26), the following expression for v_x as a function of i_x is found:

$$v_x = \frac{i_x}{2} \left(\frac{2}{g_m} + R_1 + R \right). \tag{A.28}$$

Finally, the output impedance Z_{out} is given by:

$$Z_{out} = \frac{v_x}{i_x} = \frac{\left(\frac{2}{g_m} + R_1 + R \right)}{2}, \tag{A.29}$$

$$Z_{out} = \frac{1}{g_m} + \frac{R_1 + R}{2} \approx \frac{R_1 + R}{2}. \tag{A.30}$$

The resistors R and R_1 are not only used to set the amplitude of the current source but also to increase the impedance of the network, thereby minimizing the impact of device operation on measurement performance. In addition, R_1 and R_2 can be tuned individually to compensate for variations in the physical device.

Bibliography

[1] J.M. Carrasco, L.G. Franquelo, J.T. Bialasiewicz, E. Galvan, R.C. PortilloGuisado, M.A.M. Prats, J.I. Leon, and N. Moreno-Alfonso. Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey. *IEEE Transactions on Industrial Electronics*, 53(4):1002–1016, 2006. doi: 10.1109/TIE.2006.878356.

[2] B.K. Bose. Power electronics-A Technology Review. *Proceedings of the IEEE*, 80(8): 1303–1334, 1992. doi: 10.1109/5.158603.

[3] Guishi Wang, Georgios Konstantinou, Christopher D. Townsend, Josep Pou, Sergio Vazquez, Georgios D. Demetriades, and Vassilios Georgios Agelidis. A Review of Power Electronics for Grid Connection of Utility-Scale Battery Energy Storage Systems. *IEEE Transactions on Sustainable Energy*, 7(4):1778–1790, 2016. doi: 10.1109/TSTE.2016.2586941.

[4] Jacobus Daniel van Wyk and Fred C. Lee. On a Future for Power Electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 1(2):59–72, 2013. doi: 10.1109/JESTPE.2013.2271499.

[5] José Millán, Philippe Godignon, Xavier Perpiñà, Amador Pérez-Tomás, and José Rebollo. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Transactions on Power Electronics*, 29(5):2155–2163, 2014. doi: 10.1109/TPEL.2013.2268900.

[6] Xu She, Alex Q. Huang, Óscar Lucía, and Burak Ozpineci. Review of Silicon Carbide Power Devices and Their Applications. *IEEE Transactions on Industrial Electronics*, 64(10):8193–8205, 2017. doi: 10.1109/TIE.2017.2652401.

[7] John G. Kassakian and Thomas M. Jahns. Evolving and Emerging Applications of Power Electronics in Systems. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 1(2):47–58, 2013. doi: 10.1109/JESTPE.2013.2271111.

[8] B. Jayant Baliga. *Fundamentals of Power Semiconductor Devices*. Springer Cham, 2 edition, 2019. ISBN 978-3-319-93987-2. doi: 10.1007/978-3-319-93988-9.

[9] Zuoheng Jiang, Lingling Li, Chengcai Wang, Junlei Zhao, and Mengyuan Hua. Gate-Bias Induced Threshold Voltage (VTH) Instability in P-N Junction/AlGaN/-GaN HEMT. *IEEE Transactions on Electron Devices*, 69(7):3654–3659, 2022. doi: 10.1109/TED.2022.3177397.

[10] Haoze Luo, Francesco Iannuzzo, and Marcello Turnaturi. Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(2):1657–1667, 2020. doi: 10.1109/JESTPE.2019.2894717.

[11] Ze Ni, Yanchao Li, Xiaofeng Lyu, Om Prakash Yadav, and Dong Cao. Miller Plateau As an Indicator of SiC MOSFET Gate Oxide Degradation. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1280–1287, 2018. doi: 10.1109/APEC.2018.8341181.

[12] Boyi Zhang and Shuo Wang. Miller Capacitance Cancellation to Improve SiC MOSFET's Performance in a Phase-Leg Configuration. *IEEE Transactions on Power Electronics*, 36(12):14195–14206, 2021. doi: 10.1109/TPEL.2021.3090080.

[13] Qinghao Zhang and Pinjia Zhang. A Novel Model of the Aging Effect on the ON-State Resistance of SiC Power MOSFETs for High-Accuracy Package-Related Aging Evaluation. *IEEE Transactions on Industrial Electronics*, 70(9):9495–9504, 2023. doi: 10.1109/TIE.2022.3212405.

[14] Jaume Roig and Filip Bauwens. Origin of Anomalous C_{OSS} Hysteresis in Resonant Converters With Superjunction FETs. *IEEE Transactions on Electron Devices*, 62(9): 3092–3094, 2015. doi: 10.1109/TED.2015.2455072.

[15] Lisheng Wang, Wenbo Wang, Raymond J. E. Hueting, Gert Rietveld, and Jan Abraham Ferreira. Review of Topside Interconnections for Wide Bandgap Power Semiconductor Packaging. *IEEE Transactions on Power Electronics*, 38(1):472–490, 2023. doi: 10.1109/TPEL.2022.3200469.

[16] Ange-Christian Iradukunda, David R. Huitink, and Fang Luo. A Review of Advanced Thermal Management Solutions and the Implications for Integration in High-Voltage Packages. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(1): 256–271, 2020. doi: 10.1109/JESTPE.2019.2953102.

[17] Keijo Jacobs, Mietek Bakowski, Per Ranstad, and Hans-Peter Nee. Static and Dynamic Performance of Charge-Carrier Lifetime-Tailored High-Voltage SiC p-i-n Diodes With Capacitively Assisted Switching. *IEEE Transactions on Power Electronics*, 37(10): 12065–12079, 2022. doi: 10.1109/TPEL.2022.3172666.

[18] Peter Wellmann, Noboru Ohtani, and Roland Rupp, editors. *Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications*. John Wiley Sons, Ltd, 2021. ISBN 9783527346714. doi: 10.1002/9783527824724.

[19] Juergen Biela, Mario Schweizer, Stefan Waffler, and Johann W. Kolar. SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors. *IEEE Transactions on Industrial Electronics*, 58(7):2872–2882, 2011. doi: 10.1109/TIE.2010.2072896.

[20] Kasunaidu Vechalapu, Subhashish Bhattacharya, Edward Van Brunt, Sei-Hyung Ryu, Dave Grider, and John W. Palmour. Comparative Evaluation of 15-kV SiC MOSFET

and 15-kV SiC IGBT for Medium-Voltage Converter Under the Same dv/dt Conditions. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):469–489, 2017. doi: 10.1109/JESTPE.2016.2620991.

[21] Noriyuki Iwamuro and Thomas Laska. IGBT History, State-of-the-Art, and Future Prospects. *IEEE Transactions on Electron Devices*, 64(3):741–752, 2017. doi: 10.1109/TED.2017.2654599.

[22] Edward A. Jones, Fei Fred Wang, and Daniel Costinett. Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(3):707–719, 2016. doi: 10.1109/JESTPE.2016.2582685.

[23] M. Buffolo, D. Favero, A. Marcuzzi, C. De Santi, G. Meneghesso, E. Zanoni, and M. Meneghini. Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives. *IEEE Transactions on Electron Devices*, 71(3):1344–1355, 2024. doi: 10.1109/TED.2023.3346369.

[24] B.J. Baliga. Power Semiconductor Device Figure of Merit for High-Frequency Applications. *IEEE Electron Device Letters*, 10(10):455–457, 1989. doi: 10.1109/55.43098.

[25] E. Johnson. Physical Limitations on Frequency and Power Parameters of Transistors. In *1958 IRE International Convention Record*, volume 13, pages 27–34, 1965. doi: 10.1109/IRECON.1965.1147520.

[26] T. McNutt, A. Hefner, A. Mantooth, D. Berning, and Sei-Hyung Ryu. Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence. In *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, volume 1, pages 217–226 vol.1, 2003. doi: 10.1109/PESC.2003.1218298.

[27] Hiroyuki Sakairi, Tatsuya Yanagi, Hirotaka Otake, Naotaka Kuroda, and Hiroaki Tanigawa. Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior Over Wide Voltage and Current Ranges. *IEEE Transactions on Power Electronics*, 33(9):7314–7325, 2018. doi: 10.1109/TPEL.2017.2764632.

[28] Renze Yu, Saeed Jahdi, Phil Mellor, Li Liu, Juefei Yang, Chengjun Shen, Olayiwola Alatise, and Jose Ortiz-Gonzalez. Degradation Analysis of Planar, Symmetrical and Asymmetrical Trench SiC MOSFETs Under Repetitive Short Circuit Impulses. *IEEE Transactions on Power Electronics*, 38(9):10933–10946, 2023. doi: 10.1109/TPEL.2023.3290387.

[29] Fei Wang, Zheyu Zhang, and Edward A. Jones. *Characterization of Wide Bandgap Power Semiconductor Devices*, volume 128. The Institution of Engineering and Technology, Stevenage, 1 edition, 2018. doi: 10.1049/PBPO128E.

[30] Yvan Avenas, Laurent Dupont, and Zoubir Khatir. Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review. *IEEE Transactions on Power Electronics*, 27(6):3081–3092, 2012. doi: 10.1109/TPEL.2011.2178433.

[31] Xiaohui Lu, Laili Wang, Qingshou Yang, Fengtao Yang, Yongmei Gan, and Hong Zhang. Investigation and Comparison of Temperature-Sensitive Electrical Parameters of SiC mosfet at Extremely High Temperatures. *IEEE Transactions on Power Electronics*, 38(8):9660–9672, 2023. doi: 10.1109/TPEL.2023.3267472.

[32] Ujjwal Karki, Nomar S. González-Santini, and Fang Z. Peng. Effect of Gate-Oxide Degradation on Electrical Parameters of Silicon Carbide MOSFETs. *IEEE Transactions on Electron Devices*, 67(6):2544–2552, 2020. doi: 10.1109/TED.2020.2990128.

[33] Thanh-That Nguyen, Ashraf Ahmed, T. V. Thang, and Joung-Hu Park. Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation. *IEEE Transactions on Power Electronics*, 30(5):2445–2455, 2015. doi: 10.1109/TPEL.2014.2353417.

[34] Ujjwal Karki and Fang Zheng Peng. Effect of Gate-Oxide Degradation on Electrical Parameters of Power MOSFETs. *IEEE Transactions on Power Electronics*, 33(12): 10764–10773, 2018. doi: 10.1109/TPEL.2018.2801848.

[35] Rémy Ouaida, Maxime Berthou, Javier León, Xavier Perpiñà, Sebastien Oge, Pierre Brosselard, and Charles Joubert. Gate Oxide Degradation of SiC MOSFET in Switching Conditions. *IEEE Electron Device Letters*, 35(12):1284–1286, 2014. doi: 10.1109/LED.2014.2361674.

[36] Yohei Nakamura, Naotaka Kuroda, Tatsuya Yanagi, Hiroyuki Sakairi, and Ken Nakahara. High-Voltage and High-Current Id–Vds Measurement Method for Power Transistors Improved by Reducing Self-Heating. *IEEE Electron Device Letters*, 41(4):581–584, 2020. doi: 10.1109/LED.2020.2974492.

[37] Henry A. Martin, Edsger C. P. Smits, René H. Poelma, Willem D. van Driel, and GuoQi Zhang. Online Condition Monitoring Methodology for Power Electronics Package Reliability Assessment. *IEEE Transactions on Power Electronics*, 39(4):4725–4734, 2024. doi: 10.1109/TPEL.2024.3352747.

[38] Qinghao Zhang, Geye Lu, Yanyong Yang, and Pinjia Zhang. A High-Frequency Online Junction Temperature Monitoring Method for SiC MOSFETs Based on On-State Resistance With Aging Compensation. *IEEE Transactions on Industrial Electronics*, 70(7):7393–7405, 2023. doi: 10.1109/TIE.2022.3204948.

[39] Tatsuya Nishiwaki, Shunsuke Katoh, Kenya Kobayashi, and Yoshitaka Hokomoto. Breakdown Voltage Instability Mechanism and Improving Ruggedness in Trench Field

Plate Power MOSFET. In *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 215–218, 2016. doi: 10.1109/ISPSD.2016.7520816.

[40] Jone F. Chen, J. R. Lee, Kuo-Ming Wu, Tsung-Yi Huang, C. M. Liu, and S. L. Hsu. off-State Avalanche-Breakdown-Induced On-Resistance Degradation in Lateral DMOS Transistors. *IEEE Electron Device Letters*, 28(11):1033–1035, 2007. doi: 10.1109/LED.2007.907416.

[41] Hengyu Yu, Michael Jin, Nikhil Bhardwaj, Limeng Shi, Monikuntala Bhattacharya, Jiashu Qian, Shiva Houshmand, and Anant K. Agarwal. Characterization and Analysis of Degradation for 1.2-kV Rated SiC Trench MOSFETs Under Repetitive Switching Impulses. *IEEE Transactions on Electron Devices*, 71(11):6897–6903, 2024. doi: 10.1109/TED.2024.3454022.

[42] Jiaxing Wei, Siyang Liu, Lanlan Yang, Lizhi Tang, Rongcheng Lou, Ting Li, Jiong Fang, Sheng Li, Chi Zhang, and Weifeng Sun. Investigations on the Degradations of Double-Trench SiC Power MOSFETs Under Repetitive Avalanche Stress. *IEEE Transactions on Electron Devices*, 66(1):546–552, 2019. doi: 10.1109/TED.2018.2875080.

[43] Xiaochuan Deng, Wei Huang, Xu Li, Xuan Li, Chao Chen, Yi Wen, Jiawei Ding, Wanjun Chen, Yongkui Sun, and Bo Zhang. Investigation of Failure Mechanisms of 1200 V Rated Trench SiC MOSFETs Under Repetitive Avalanche Stress. *IEEE Transactions on Power Electronics*, 37(9):10562–10571, 2022. doi: 10.1109/TPEL.2022.3163930.

[44] Roger Stark, Alexander Tsibizov, Neha Nain, Ulrike Grossner, and Ivana Kovacevic-Badstuebner. Accuracy of Three Interterminal Capacitance Models for SiC Power MOSFETs Under Fast Switching. *IEEE Transactions on Power Electronics*, 36(8):9398–9410, 2021. doi: 10.1109/TPEL.2021.3053330.

[45] Nirmana Perera, Armin Jafari, Reza Soleimanzadeh, Nicolas Bollier, Sunil Gamini Abeyratne, and Elison Matioli. Hard-Switching Losses in Power FETs: The Role of Output Capacitance. *IEEE Transactions on Power Electronics*, 37(7):7604–7616, 2022. doi: 10.1109/TPEL.2021.3130831.

[46] Roger Stark, Alexander Tsibizov, Ivana Kovacevic-Badstuebner, Thomas Ziemann, and Ulrike Grossner. Gate Capacitance Characterization of Silicon Carbide and Silicon Power MOSFETs Revisited. *IEEE Transactions on Power Electronics*, 37(9):10572–10584, 2022. doi: 10.1109/TPEL.2022.3164360.

[47] Yasushige Mukunoki, Yuta Nakamura, Kentaro Konno, Takeshi Horiguchi, Yasushi Nakayama, Akinori Nishizawa, Masaki Kuzumoto, and Hirofumi Akagi. Modeling of a Silicon-Carbide MOSFET With Focus on Internal Stray Capacitances and Inductances, and Its Verification. *IEEE Transactions on Industry Applications*, 54(3):2588–2597, 2018. doi: 10.1109/TIA.2018.2796587.

[48] Wadia Jouha, Mohamed Masmoudi, Ahmed El Oualkadi, Eric Joubert, and Pascal Dherbécourt. Physical Study of SiC Power MOSFETs Towards HTRB Stress Based on C-V Characteristics. *IEEE Transactions on Device and Materials Reliability*, 20 (3):506–511, 2020. doi: 10.1109/TDMR.2020.2999029.

[49] Salvatore Race, Ivana Kovacevic-Badstuebner, Michel Nagel, Alexander Tsibizov, Roger Stark, Dan Popescu, Bogdan Popescu, and Ulrike Grossner. Frequency-Dependent Internal Gate Resistance of SiC Power MOSFETs. *IEEE Transactions on Electron Devices*, 71(12):7709–7715, 2024. doi: 10.1109/TED.2024.3488684.

[50] Yumeng Cai, Peng Sun, Cong Chen, Yuankui Zhang, Zhibin Zhao, Xuebao Li, Lei Qi, Zhong Chen, and Hans-Peter Nee. Investigation on Gate Oxide Degradation of SiC

MOSFET in Switching Operation. *IEEE Transactions on Power Electronics*, 39(8): 9565–9578, 2024. doi: 10.1109/TPEL.2024.3392974.

[51] Jian Chen, Xiong Du, Quanming Luo, Xinyue Zhang, Pengju Sun, and Lin Zhou. A Review of Switching Oscillations of Wide Bandgap Semiconductor Devices. *IEEE Transactions on Power Electronics*, 35(12):13182–13199, 2020. doi: 10.1109/TPEL.2020.2995778.

[52] Yuancheng Ren, Ming Xu, Jinghai Zhou, and F.C. Lee. Analytical Loss Model of Power MOSFET. *IEEE Transactions on Power Electronics*, 21(2):310–319, 2006. doi: 10.1109/TPEL.2005.869743.

[53] Zheng Chen, Yiying Yao, Dushan Boroyevich, Khai D. T. Ngo, Paolo Mattavelli, and Kaushik Rajashekara. A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications. *IEEE Transactions on Power Electronics*, 29(5):2307–2320, 2014. doi: 10.1109/TPEL.2013.2283245.

[54] Yushan Liu, Jianyu Cao, and Xiao Li. Switching Loss Model for Fast-Switching GaN HEMT in Half-Bridge Circuit Considering Parasitic Inductance and Temperature Effect. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 71(12):6128–6137, 2024. doi: 10.1109/TCSI.2024.3480951.

[55] Miguel Rodríguez, Alberto Rodríguez, Pablo Fernández Miaja, Diego González Lamar, and Javier Sebastián Zúniga. An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model. *IEEE Transactions on Power Electronics*, 25(6):1626–1640, 2010. doi: 10.1109/TPEL.2010.2040852.

[56] Zheyu Zhang, Ben Guo, and Fei Wang. Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices. *IEEE Transactions on Power Electronics*, 34(9):9082–9094, 2019. doi: 10.1109/TPEL.2018.2883454.

[57] Rui Li, Xinke Wu, Shu Yang, and Kuang Sheng. Dynamic on-State Resistance Test and Evaluation of GaN Power Devices Under Hard- and Soft-Switching Conditions by Double and Multiple Pulses. *IEEE Transactions on Power Electronics*, 34(2):1044–1053, 2019. doi: 10.1109/TPEL.2018.2844302.

[58] Qihao Song, Ruizhe Zhang, Joseph P. Kozak, Jingcun Liu, Qiang Li, and Yuhao Zhang. Robustness of Cascode GaN HEMTs in Unclamped Inductive Switching. *IEEE Transactions on Power Electronics*, 37(4):4148–4160, 2022. doi: 10.1109/TPEL.2021.3122740.

[59] Olayiwola Alatise, Ian Kennedy, George Petkos, Keith Heppenstall, Khalid Khan, Jim Parkin, Adrian Koh, and Philip Rutter. The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low-Voltage Trench Power nMOSFETs. *IEEE Transactions on Electron Devices*, 57(7):1651–1658, 2010. doi: 10.1109/TED.2010.2049062.

[60] Mattia Guacci, Jon Azurza Anderson, Kessy L. Pally, Dominik Bortis, Johann W. Kolar, Matthias J. Kasper, Juan Sanchez, and Gerald Deboy. Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(3):2238–2254, 2020. doi: 10.1109/JESTPE.2019.2944268.

[61] Tong Yao and Rajapandian Ayyanar. A Multifunctional Double Pulse Tester for Cascode GaN Devices. *IEEE Transactions on Industrial Electronics*, 64(11):9023–9031, 2017. doi: 10.1109/TIE.2017.2694381.

[62] Mattia Guacci, Morris Heller, Dominik Neumayr, Dominik Bortis, Johann W. Kolar, Gerald Deboy, Clemens Ostermaier, and Oliver Häberlen. On the Origin of the C_{oss}

-Losses in Soft-Switching GaN-on-Si Power HEMTs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(2):679–694, 2019. doi: 10.1109/JESTPE.2018.2885442.

[63] Anup Anurag, Sayan Acharya, and Subhashish Bhattacharya. An Accurate Calorimetric Loss Measurement Method for SiC MOSFETs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(2):1644–1656, 2020. doi: 10.1109/JESTPE.2019.2920935.

[64] Shu Yang, Shaowen Han, Kuang Sheng, and Kevin J. Chen. Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(3):1425–1439, 2019. doi: 10.1109/JESTPE.2019.2925117.

[65] Zikang Tong, Grayson Zulauf, Jiale Xu, James D. Plummer, and Juan Rivas-Davila. Output Capacitance Loss Characterization of Silicon Carbide Schottky Diodes. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(2):865–878, 2019. doi: 10.1109/JESTPE.2019.2904290.

[66] Grayson Zulauf, Sanghyeon Park, Wei Liang, Kawin North Surakitbovorn, and Juan Rivas-Davila. COSS Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters. *IEEE Transactions on Power Electronics*, 33(12):10748–10763, 2018. doi: 10.1109/TPEL.2018.2800533.

[67] Ruizhe Zhang, Joseph P. Kozak, Ming Xiao, Jingcun Liu, and Yuhao Zhang. Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs. *IEEE Transactions on Power Electronics*, 35(12):13409–13419, 2020. doi: 10.1109/TPEL.2020.2993982.

[68] Siyang Liu, Sheng Li, Chi Zhang, Ningbo Li, Xinyi Tao, Chen Ge, Le Qian, Shuxuan Xin, and Weifeng Sun. Single Pulse Unclamped-Inductive-Switching Induced Failure

and Analysis for 650 V p-GaN HEMT. *IEEE Transactions on Power Electronics*, 35 (11):11328–11331, 2020. doi: 10.1109/TPEL.2020.2988976.

[69] Peng Xue, Luca Maresca, Michele Riccio, Giovanni Breglio, and Andrea Irace. Investigation on the Short-Circuit Oscillation of Cascode GaN HEMTs. *IEEE Transactions on Power Electronics*, 35(6):6292–6300, 2020. doi: 10.1109/TPEL.2019.2947274.

[70] Mohammad Rajabi Nasab, Roberto Cometa, Sergio Bruno, Giovanni Giannoccaro, and Massimo la Scala. Power Systems Simulation and Analysis: A Review on Current Applications and Future Trends in DRTS of Grid-Connected Technologies. *IEEE Access*, 12:121320–121345, 2024. doi: 10.1109/ACCESS.2024.3452468.

[71] Xavier Guillaud, M. Omar Faruque, Alexandre Teninge, Ali Hasan Hariri, Luigi Vanfretti, Mario Paolone, Venkata Dinavahi, Pinaki Mitra, Georg Lauss, Christian Dufour, Paul Forsyth, Anurag K. Srivastava, Kai Strunz, Thomas Strasser, and Ali Davoudi. Applications of Real-Time Simulation Technologies in Power and Energy Systems. *IEEE Power and Energy Technology Systems Journal*, 2(3):103–115, 2015. doi: 10.1109/JPETS.2015.2445296.

[72] Georg Lauss, Zhiwang Feng, Mazheruddin H. Syed, Alkistis Kontou, Antonio De Paola, Alexandros Paspatis, and Panos Kotsampopoulos. A Framework for Sensitivity Analysis of Real-Time Power Hardware-in-the-Loop (PHIL) Systems. *IEEE Access*, 10: 101305–101318, 2022. doi: 10.1109/ACCESS.2022.3206780.

[73] M. D. Omar Faruque, Thomas Strasser, Georg Lauss, Vahid Jalili-Marandi, Paul Forsyth, Christian Dufour, Venkata Dinavahi, Antonello Monti, Panos Kotsampopoulos, Juan A. Martinez, Kai Strunz, Maryam Saeedifard, Xiaoyu Wang, David Shearer, and Mario Paolone. Real-Time Simulation Technologies for Power Systems Design,

Testing, and Analysis. *IEEE Power and Energy Technology Systems Journal*, 2(2): 63–73, 2015. doi: 10.1109/JPETS.2015.2427370.

[74] Huimin Wang, Zongyao Zhou, Zhiliang Xu, Xinglai Ge, Yongheng Yang, Yi Zhang, Bo Yao, and Dong Xie. A Thermal Network Model for Multichip Power Modules Enabling to Characterize the Thermal Coupling Effects. *IEEE Transactions on Power Electronics*, 39(5):6225–6245, 2024. doi: 10.1109/TPEL.2024.3355207.

[75] Simon Lineykin and Shmuel Ben-Yaakov. Modeling and Analysis of Thermoelectric Modules. *IEEE Transactions on Industry Applications*, 43(2):505–512, 2007. doi: 10.1109/TIA.2006.889813.

[76] Yvan Avenas, Laurent Dupont, Nick Baker, Henri Zara, and Franck Barruel. Condition Monitoring: A Decade of Proposed Techniques. *IEEE Industrial Electronics Magazine*, 9(4):22–36, 2015. doi: 10.1109/MIE.2015.2481564.

[77] Shaoyong Yang, Dawei Xiang, Angus Bryant, Philip Mawby, Li Ran, and Peter Tavner. Condition Monitoring for Device Reliability in Power Electronic Converters: A Review. *IEEE Transactions on Power Electronics*, 25(11):2734–2752, 2010. doi: 10.1109/TPEL.2010.2049377.

[78] Hyunseok Oh, Bongtae Han, Patrick McCluskey, Changwoon Han, and Byeng D. Youn. Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review. *IEEE Transactions on Power Electronics*, 30(5):2413–2426, 2015. doi: 10.1109/TPEL.2014.2346485.

[79] Yongle Huang, Yifei Luo, Fei Xiao, Binli Liu, and Xin Tang. Evaluation of the Degradation in Electrothermal Characteristics of IGBTs During Thermal Cycling Cocaused by Solder Cracking and Al-Wires Lifting-Off Based on Iterative Looping. *IEEE Transactions on Power Electronics*, 38(2):1768–1778, 2023. doi: 10.1109/TPEL.2022.3209331.

[80] Wenzhao Liu, Dao Zhou, Francesco Iannuzzo, Michael Hartmann, and Frede Blaabjerg. Separation and Validation of Bond-Wire and Solder Layer Failure Modes in IGBT Modules. *IEEE Transactions on Industry Applications*, 58(2):2324–2331, 2022. doi: 10.1109/TIA.2022.3141034.

[81] Ui-Min Choi, Frede Blaabjerg, and Kyo-Beum Lee. Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems. *IEEE Transactions on Power Electronics*, 30(5):2517–2533, 2015. doi: 10.1109/TPEL.2014.2373390.

[82] Zongyuan Dai, Xinglai Ge, Chunxu Lin, Huimin Wang, Zhiliang Xu, and Gengle Liang. A Bond Wire Aging Monitoring Method for IGBT Modules Based on Bond Wire Degradation Voltage. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 12(6):5534–5543, 2024. doi: 10.1109/JESTPE.2024.3476374.

[83] Yongle Huang, Yingjie Jia, Yifei Luo, Fei Xiao, and Binli Liu. Lifting-Off of Al Bonding Wires in IGBT Modules Under Power Cycling: Failure Mechanism and Lifetime Model. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(3):3162–3173, 2020. doi: 10.1109/JESTPE.2019.2924241.

[84] Wei Kexin, Du Mingxing, Xie Linlin, and Li Jian. Study of Bonding Wire Failure Effects on External Measurable Signals of IGBT Module. *IEEE Transactions on Device and Materials Reliability*, 14(1):83–89, 2014. doi: 10.1109/TDMR.2012.2200485.

[85] Chunming Tu, Haoliang Xu, Biao Xiao, Jiwu Lu, Qi Guo, and Liu Long. Research on the Influence of Bond Wire Lift-Off Position on the Electro-Thermal Characteristics of IGBT. *IEEE Transactions on Electron Devices*, 69(3):1271–1278, 2022. doi: 10.1109/TED.2022.3140689.

[86] Yue Xu, Joshua Stewart, He Song, Li Cheng, Igor Cvetkovic, Rolando Burgos, and Dushan Boroyevich. High Power Density Medium-Voltage Converter Integration via

Electric Field Management. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(1):895–905, 2022. doi: 10.1109/JESTPE.2021.3107343.

[87] Zhicheng Guo and Alex Q. Huang. Characterizations of Partial Discharge in Modern Power Electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 12(6):5705–5714, 2024. doi: 10.1109/JESTPE.2024.3417803.

[88] Joshua Stewart, Igor Cvetkovic, and Rolando Burgos. Design and Analysis of a 24 k V PCB Bus for the Low Impedance Interconnect of a Multiphase PEBB- Based Converter. In *2022 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, pages 41–44, 2022. doi: 10.1109/IPMHVC51093.2022.10099391.

[89] Joshua Stewart, Yue Xu, Rolando Burgos, and Mona Ghassemi. Design of a Multilayer PCB Bus for Medium Voltage DC Converters. In *2019 IEEE Electric Ship Technologies Symposium (ESTS)*, pages 329–336, 2019. doi: 10.1109/ESTS.2019.8847737.

[90] Johann W. Kolar and Thomas Friedli. The Essence of Three-Phase PFC Rectifier Systems—Part I. *IEEE Transactions on Power Electronics*, 28(1):176–198, 2013. doi: 10.1109/TPEL.2012.2197867.

[91] Thomas Friedli, Michael Hartmann, and Johann W. Kolar. The Essence of Three-Phase PFC Rectifier Systems—Part II. *IEEE Transactions on Power Electronics*, 29 (2):543–560, 2014. doi: 10.1109/TPEL.2013.2258472.

[92] Lee Empringham, Johann W. Kolar, Jose Rodriguez, Pat W. Wheeler, and Jon C. Clare. Technological Issues and Industrial Application of Matrix Converters: A Review. *IEEE Transactions on Industrial Electronics*, 60(10):4260–4271, 2013. doi: 10.1109/TIE.2012.2216231.

[93] Florian Krismer and Johann W. Kolar. Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications. *IEEE Transactions on Industrial Electronics*, 59(7):2745–2760, 2012. doi: 10.1109/TIE.2011.2112312.

[94] Ziheng Xiao, Yu Jiang, Fei Deng, Zhigang Yao, and Yi Tang. A Data-Driven Control Parameters Optimization Method for Dual Active Bridge Converters. *IEEE Transactions on Industrial Electronics*, 71(11):14054–14066, 2024. doi: 10.1109/TIE.2024.3370950.

[95] Swaminathan Balachandran and Fred C.y. Lee. Algorithms for Power Converter Design Optimization. *IEEE Transactions on Aerospace and Electronic Systems*, AES-17(3):422–432, 1981. doi: 10.1109/TAES.1981.309070.

[96] Susana Estefany De León-Aldaco, Hugo Calleja, and Jesús Aguayo Alquicira. Metaheuristic Optimization Methods Applied to Power Converters: A Review. *IEEE Transactions on Power Electronics*, 30(12):6791–6803, 2015. doi: 10.1109/TPEL.2015.2397311.

[97] S. Busquets-Monge, J.-C. Crebier, S. Ragon, E. Hertz, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D.K. Lindner. Design of a boost power factor correction converter using optimization techniques. *IEEE Transactions on Power Electronics*, 19(6):1388–1396, 2004. doi: 10.1109/TPEL.2004.836638.

[98] Ruiyang Yu, Bryan Man Hay Pong, Bingo Wing-Kuen Ling, and James Lam. Two-Stage Optimization Method for Efficient Power Converter Design Including Light Load Operation. *IEEE Transactions on Power Electronics*, 27(3):1327–1337, 2012. doi: 10.1109/TPEL.2011.2114676.

[99] Ha-Min Park, Hyung-Woo Lee, Chan-Bae Park, Jae-Bum Lee, Jin-Chul Kim, and Ju Lee. Analysis and Design of a 50-kW Two Stage Converters for EV Fast Charger

With High Efficiency and Wide Output Voltage of 150–1000 V. *IEEE Access*, 13: 37182–37197, 2025. doi: 10.1109/ACCESS.2025.3544277.

[100] Mohamed H. Ahmed, Fred C. Lee, and Qiang Li. Two-Stage 48-V VRM With Intermediate Bus Voltage Optimization for Data Centers. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(1):702–715, 2021. doi: 10.1109/JESTPE.2020.2976107.

[101] Daniel H. Zhou and Minjie Chen. Balancing Flying Capacitor Multilevel Converters With Coupled Inductors: Multiresonant Dynamics. *IEEE Transactions on Power Electronics*, 40(5):6578–6592, 2025. doi: 10.1109/TPEL.2025.3526131.

[102] Pit-Leong Wong, Peng Xu, P. Yang, and F.C. Lee. Performance Improvements of Interleaving VRMs with Coupling Inductors. *IEEE Transactions on Power Electronics*, 16(4):499–507, 2001. doi: 10.1109/63.931059.

[103] Tao Jiang, Shaozhe Zhang, Chunhui Yang, Qi Xin, Jiahao Liang, and Xiaotao Han. A Ripple Compensation Auxiliary Half-Bridge for Coupled Inductor Multiphase Buck Converter. *IEEE Transactions on Power Electronics*, 40(7):9452–9462, 2025. doi: 10.1109/TPEL.2025.3546237.

[104] Po-Wa Lee, Yim-Shu Lee, D.K.W. Cheng, and Xiu-Cheng Liu. Steady-State Analysis of an Interleaved Boost Converter with Coupled Inductors. *IEEE Transactions on Industrial Electronics*, 47(4):787–795, 2000. doi: 10.1109/41.857959.

[105] Feng Jin, Tianlong Yuan, Ahmed Nabih, and Qiang Li. Efficient Integrated Magnetics With Winding Cancellation Technique to Reduce Common-Mode EMI Noise for a Single-Phase CLLC Converter. *IEEE Transactions on Power Electronics*, 39(11): 14758–14774, 2024. doi: 10.1109/TPEL.2024.3436044.

[106] Feng Jin, Ahmed Nabih, Tianlong Yuan, and Qiang Li. A High-Efficiency High-Density Three-Phase CLLC Resonant Converter With a Universally Derived Three-Phase Integrated Transformer for On-Board-Charger Application. *IEEE Transactions on Power Electronics*, 39(4):4350–4366, 2024. doi: 10.1109/TPEL.2024.3354679.

[107] Ahmed Nabih and Qiang Li. A Method to Embed Resonant Inductor Into PCB Matrix Transformer for High-Density Resonant Converters. *IEEE Transactions on Power Electronics*, 39(2):2385–2400, 2024. doi: 10.1109/TPEL.2023.3330974.

[108] Johann W. Kolar. Power Electronics — The Key Enabler of Future Energy Systems. Technical report, NSF Workshop on Power Electronics, 2016. Available at: https://www.ams-publications.ee.ethz.ch/uploads/tx_ethpublications/workshop_publications/__Kolar_NSF_Workshop_Power_Electronics_2016_FINALFINALFINAL_081116.pdf.

[109] Yan-Fei Liu and Don Tan. A Discussion on Ultrahigh Efficiency and Ultrahigh Power Density DC–DC Converter Technologies. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(3):2457–2468, 2023. doi: 10.1109/JESTPE.2023.3239516.

[110] Song Ding, Chunyan Nie, Qi Liu, Qinsong Qian, and Weifeng Sun. High Efficiency High Power Density Bidirectional Non-Isolated LLC Converter With Transformer-Coupled Gate Driver for 48 V MHEV. *IEEE Open Journal of Power Electronics*, 6:747–760, 2025. doi: 10.1109/OJPEL.2025.3561221.

[111] Longyang Yu, Wei Mu, Shenglei Zhao, Xiufeng Song, Yue Hao, and Jincheng Zhang. A 3-D GaN-Based PoL Converters Based on the Planar Magnetic Component With Distributed Air Gap and High Thermal Conductivity. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 13(1):880–891, 2025. doi: 10.1109/JESTPE.2024.3486001.

[112] Daniel H. Zhou, Janko Čeliković, Dragan Maksimović, and Minjie Chen. Balancing Multiphase FCML Converters With Coupled Inductors: Modeling, Analysis, Limitations. *IEEE Transactions on Power Electronics*, 39(8):9268–9291, 2024. doi: 10.1109/TPEL.2024.3393861.

[113] Shan Yin, Xiong Xin, Runze Wang, Minghai Dong, Jinshu Lin, Yunfei Gu, and Hui Li. A 1-MHz GaN-Based *LCLC* Resonant Step-Up Converter With Air-Core Transformer for Satellite Electric Propulsion Application. *IEEE Transactions on Industrial Electronics*, 69(11):11035–11045, 2022. doi: 10.1109/TIE.2021.3121711.

[114] Pei-Jung Yang, Chun-Hsun Wu, Che-Yen Yeh, and Le-Ren Chang-Chien. Digital Adaptive On-Time and Transient-Optimized Ripple Controlled Buck Converter. *IEEE Access*, 11:135351–135364, 2023. doi: 10.1109/ACCESS.2023.3336013.

[115] Richard Redl and Jian Sun. Ripple-Based Control of Switching Regulators—An Overview. *IEEE Transactions on Power Electronics*, 24(12):2669–2680, 2009. doi: 10.1109/TPEL.2009.2032657.

[116] Haihong Qin, Xiaoxue Zheng, Wenlu Wang, and Qian Xun. A Novel Adaptive Dead-Time Control Method for GaN-Based Motor Drives. *IEEE Transactions on Energy Conversion*, 40(1):258–269, 2025. doi: 10.1109/TEC.2024.3431940.

[117] Meysam Gheisarnejad and Mohammad Hassan Khooban. IoT-Based DC/DC Deep Learning Power Converter Control: Real-Time Implementation. *IEEE Transactions on Power Electronics*, 35(12):13621–13630, 2020. doi: 10.1109/TPEL.2020.2993635.

[118] Wei-Chung Chen, Hsin-Chieh Chen, Meng-Wei Chien, Ying-Wei Chou, Ke-Horng Chen, Ying-Hsi Lin, Tsung-Yen Tsai, Shian-Ru Lin, and Chao-Cheng Lee. Pseudo-Constant Switching Frequency in On-Time Controlled Buck Converter with Predicting

Correction Techniques. *IEEE Transactions on Power Electronics*, 31(5):3650–3662, 2016. doi: 10.1109/TPEL.2015.2457571.

[119] Guohua Zhou, Guihua Mao, Hongbo Zhao, Shuhan Zhou, and Paolo Mattavelli. Digital Average-Ripple-Based Control Techniques for Switching Converters With Fast Transient Performance. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(1):89–101, 2021. doi: 10.1109/JESTPE.2020.2964268.

[120] Luca Corradini, Alessandro Costabeber, Paolo Mattavelli, and Stefano Saggini. Parameter-Independent Time-Optimal Digital Control for Point-of-Load Converters. *IEEE Transactions on Power Electronics*, 24(10):2235–2248, 2009. doi: 10.1109/TPEL.2009.2022397.

[121] Farzad Hosseinabadi, Sajib Chakraborty, Sachin Kumar Bhoi, Guenter Prochart, Dino Hrvanovic, and Omar Hegazy. A Comprehensive Overview of Reliability Assessment Strategies and Testing of Power Electronics Converters. *IEEE Open Journal of Power Electronics*, 5:473–512, 2024. doi: 10.1109/OJPEL.2024.3379294.

[122] Shi Pu, Fei Yang, Bhanu Teja Vankayalapati, and Bilal Akin. Aging Mechanisms and Accelerated Lifetime Tests for SiC MOSFETs: An Overview. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(1):1232–1254, 2022. doi: 10.1109/JESTPE.2021.3110476.

[123] Abu Hanif, Yuechuan Yu, Douglas DeVoto, and Faisal Khan. A Comprehensive Review Toward the State-of-the-Art in Failure and Lifetime Predictions of Power Electronic Devices. *IEEE Transactions on Power Electronics*, 34(5):4729–4746, 2019. doi: 10.1109/TPEL.2018.2860587.

[124] Ze Ni, Xiaofeng Lyu, Om Prakash Yadav, Brij N. Singh, Sheng Zheng, and Dong Cao. Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters.

IEEE Transactions on Power Electronics, 35(8):7765–7794, 2020. doi: 10.1109/TPEL.2019.2962503.

[125] Saeed Rahimpour, Hadi Tarzamni, Naser Vosoughi Kurdkandi, Oleksandr Husev, Dmitri Vinnikov, and Farzad Tahami. An Overview of Lifetime Management of Power Electronic Converters. *IEEE Access*, 10:109688–109711, 2022. doi: 10.1109/ACCESS.2022.3214320.

[126] Huai Wang and Frede Blaabjerg. Power Electronics Reliability: State of the Art and Outlook. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(6):6476–6493, 2021. doi: 10.1109/JESTPE.2020.3037161.

[127] Jiahui Jiang, Saeed Peyghami, Colin Coates, and Frede Blaabjerg. A Decentralized Reliability-Enhanced Power Sharing Strategy for PV-Based Microgrids. *IEEE Transactions on Power Electronics*, 36(6):7281–7293, 2021. doi: 10.1109/TPEL.2020.3040991.

[128] Mostafa Abarzadeh, Saeed Peyghami, Kamal Al-Haddad, Nathan Weise, Liuchen Chang, and Frede Blaabjerg. Reliability and Performance Improvement of PUC Converter Using a New Single-Carrier Sensor-Less PWM Method With Pseudo Reference Functions. *IEEE Transactions on Power Electronics*, 36(5):6092–6105, 2021. doi: 10.1109/TPEL.2020.3030698.

[129] Saeed Peyghami, Frede Blaabjerg, and Peter Palensky. Incorporating Power Electronic Converters Reliability Into Modern Power System Reliability Analysis. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(2):1668–1681, 2021. doi: 10.1109/JESTPE.2020.2967216.

[130] Saeed Peyghami, Zhongxu Wang, and Frede Blaabjerg. A Guideline for Reliability Prediction in Power Electronic Converters. *IEEE Transactions on Power Electronics*, 35(10):10958–10968, 2020. doi: 10.1109/TPEL.2020.2981933.

[131] Luc Imperiali, David Menzi, Johann W. Kolar, and Jonas Huber. Multi-Objective Minimization of Life-Cycle Environmental Impacts of Three-Phase AC-DC Converter Building Blocks. In *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2994–3004, 2024. doi: 10.1109/APEC48139.2024.10509190.

[132] Thomas Guillod, Panteleimon Papamanolis, and Johann W. Kolar. Artificial Neural Network (ANN) Based Fast and Accurate Inductor Modeling and Design. *IEEE Open Journal of Power Electronics*, 1:284–299, 2020. doi: 10.1109/OJPEL.2020.3012777.

[133] Ian Laird, Xibo Yuan, James Scoltock, and Andrew J. Forsyth. A Design Optimization Tool for Maximizing the Power Density of 3-Phase DC–AC Converters Using Silicon Carbide (SiC) Devices. *IEEE Transactions on Power Electronics*, 33(4):2913–2932, 2018. doi: 10.1109/TPEL.2017.2705805.

[134] Andrija Stupar, Timothy McRae, Nenad Vukadinović, Aleksandar Prodić, and Josh A. Taylor. Multi-Objective Optimization of Multi-Level DC–DC Converters Using Geometric Programming. *IEEE Transactions on Power Electronics*, 34(12):11912–11939, 2019. doi: 10.1109/TPEL.2019.2908826.

[135] Ralph M. Burkart and Johann W. Kolar. Comparative η– ρ– σ Pareto Optimization of Si and SiC Multilevel Dual-Active-Bridge Topologies With Wide Input Voltage Range. *IEEE Transactions on Power Electronics*, 32(7):5258–5270, 2017. doi: 10.1109/TPEL.2016.2614139.

[136] J. W. Kolar, J. Biela, and J. Minibock. Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2In *2009 IEEE 6th International Power Electronics and Motion Control Conference*, pages 1–21, 2009. doi: 10.1109/IPEMC.2009.5289336.

[137] Peng Huang, Matthew D. Smith, Michael J. Uren, Zequan Chen, Benoit Bakeroot, Anurag Vohra, Stefaan Decoutere, and Martin Kuball. Charge Transport in GaN High Electron Mobility Transistor With Positive Substrate Bias. *IEEE Transactions on Electron Devices*, 72(7):3483–3488, 2025. doi: 10.1109/TED.2025.3571004.

[138] Shu Yang, Chunhua Zhou, Shaowen Han, Jin Wei, Kuang Sheng, and Kevin J. Chen. Impact of Substrate Bias Polarity on Buffer-Related Current Collapse in AlGaN/GaN-on-Si Power Devices. *IEEE Transactions on Electron Devices*, 64(12):5048–5056, 2017. doi: 10.1109/TED.2017.2764527.

[139] Keiichi Omika, Yasunori Tateno, Tsuyoshi Kouchi, Tsutomu Komatani, Seiji Yaegassi, Keiichi Yui, Ken Nakata, Naoka Nagamura, Masato Kotsugi, Koji Horiba, Masaharu Oshima, Maki Suemitsu, and Hirokazu Fukidome. Operation Mechanism of GaN-based Transistors Elucidated by Element-Specific X-ray Nanospectroscopy. *Scientific Reports*, 8(1):13268, 2018. ISSN 2045-2322. doi: 10.1038/s41598-018-31485-4.

[140] Zhen-Hong Huang, Shun-Wei Tang, Chao-Ta Fan, Ming-Cheng Lin, and Tian-Li Wu. Dynamic On-Resistance Stability of SiC and GaN Power Devices during High-Frequency (100–300 kHz) Hard Switching and Zero Voltage Switching Operations. *Microelectronics Reliability*, 145:114983, 2023. ISSN 0026-2714. doi: https://doi.org/10.1016/j.microrel.2023.114983. URL https://www.sciencedirect.com/science/article/pii/S0026271423000835.

[141] Yuru Wang, Gang Lyu, Jin Wei, Zheyang Zheng, Jiabei He, Jiacheng Lei, and Kevin J. Chen. Characterization of Static and Dynamic Behavior of 1200 V Normally off GaN/SiC Cascode Devices. *IEEE Transactions on Industrial Electronics*, 67(12): 10284–10294, 2020. doi: 10.1109/TIE.2019.2959512.

[142] Chao Yang, Xiaorong Luo, Tao Sun, Anbang Zhang, Dongfa Ouyang, Siyu Deng,

Jie Wei, and Bo Zhang. High Breakdown Voltage and Low Dynamic ON-Resistance AlGaN/GaN HEMT with Fluorine Ion Implantation in SiN_x Passivation Layer. *Nanoscale Research Letters*, 14(1):191, 2019. ISSN 1556-276X. doi: 10.1186/s11671-019-3025-8. URL https://doi.org/10.1186/s11671-019-3025-8.

[143] Mingxing Du, Jinlei Xin, Hongbin Wang, and Ziwei Ouyang. Aging Diagnosis of Bond Wire Using On-State Drain-Source Voltage Separation for SiC MOSFET. *IEEE Transactions on Device and Materials Reliability*, 21(1):41–47, 2021. doi: 10.1109/TDMR.2020.3047419.

[144] Zibo Chen, Chen Chen, and Alex Q. Huang. Driver Integrated Online Rds-on Monitoring Method for SiC Power Converters. In *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 01–07, 2022. doi: 10.1109/ECCE50734.2022.9947617.

[145] Furkan Karakaya, Anuj Maheshwari, Arijit Banerjee, and John S. Donnal. An Approach for Online Estimation of On-State Resistance in SiC MOSFETs Without Current Measurement. *IEEE Transactions on Power Electronics*, 38(9):11463–11473, 2023. doi: 10.1109/TPEL.2023.3282585.

[146] Grayson Zulauf, Mattia Guacci, and Johann W. Kolar. Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks. *IEEE Transactions on Power Electronics*, 35(6):5581–5588, 2020. doi: 10.1109/TPEL.2019.2955656.

[147] R. Vetury, N.Q. Zhang, S. Keller, and U.K. Mishra. The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs. *IEEE Transactions on Electron Devices*, 48(3):560–566, 2001. doi: 10.1109/16.906451.

[148] Brett Setera and Aristos Christou. Challenges of overcoming defects in wide bandgap

semiconductor power electronics. *Electronics*, 11(1), 2022. ISSN 2079-9292. doi: 10.3390/electronics11010010. URL https://www.mdpi.com/2079-9292/11/1/10.

[149] Ghulam Akbar, Alessio Di Fatta, Giuseppe Rizzo, Guido Ala, Pietro Romano, and Antonino Imburgia. Comprehensive review of wide-bandgap (wbg) devices: Sic mosfet and its failure modes affecting reliability. *Physchem*, 5(1), 2025. ISSN 2673-7167. doi: 10.3390/physchem5010010. URL https://www.mdpi.com/2673-7167/5/1/10.

[150] Houqiang Fu, Xuanqi Huang, Hong Chen, Zhijian Lu, and Yuji Zhao. Fabrication and Characterization of Ultra-wide Bandgap AlN-Based Schottky Diodes on Sapphire by MOCVD. *IEEE Journal of the Electron Devices Society*, 5(6):518–524, 2017. doi: 10.1109/JEDS.2017.2751554.

[151] Krishna Shenai. Manufacturing Challenges in Wide Band Gap (WBG) Power Electronics. *ECS Transactions*, 58(4):301, aug 2013. doi: 10.1149/05804.0301ecst. URL https://dx.doi.org/10.1149/05804.0301ecst.

[152] Po-Chih Chen, Wen-Chien Miao, Tanveer Ahmed, Yi-Yu Pan, Chun-Liang Lin, Shih-Chen Chen, Hao-Chung Kuo, Bing-Yue Tsui, and Der-Hsien Lien. Defect Inspection Techniques in SiC. *Nanoscale Research Letters*, 17(1):30, 2022. ISSN 1556-276X. doi: 10.1186/s11671-022-03672-w. URL https://doi.org/10.1186/s11671-022-03672-w.

[153] Lei Tang, Huaping Jiang, Ruijin Liao, Yihan Huang, Xiaohan Zhong, Xiaowei Qi, Li Liu, and Quan Zhang. Impact of the Threshold Dispersity Evolution on the Current Sharing of Parallel SiC MOSFETs. *IEEE Transactions on Power Electronics*, 39(5): 6312–6326, 2024. doi: 10.1109/TPEL.2024.3368337.

[154] Yohei Nakamura, Michihiro Shintani, and Takashi Sato. Dominant Model Parameter Extraction for Analyzing Current Imbalance in Parallel Connected SiC MOSFETs. In

2021 IEEE Energy Conversion Congress and Exposition (ECCE), pages 5622–5628, 2021. doi: 10.1109/ECCE47101.2021.9595345.

[155] Bin Zhao, Qiuping Yu, Peng Sun, Yumeng Cai, and Zhibin Zhao. Device Screening Strategy for Suppressing Current Imbalance in Parallel-Connected SiC MOSFETs. *IEEE Transactions on Device and Materials Reliability*, 21(4):556–568, 2021. doi: 10.1109/TDMR.2021.3116458.

[156] Zheng Zeng, Xin Zhang, and Xiaoling Li. Layout-Dominated Dynamic Current Imbalance in Multichip Power Module: Mechanism Modeling and Comparative Evaluation. *IEEE Transactions on Power Electronics*, 34(11):11199–11214, 2019. doi: 10.1109/TPEL.2019.2900497.

[157] R. Ladbury and J.L. Gorelick. Statistical Methods for Large Flight Lots and Ultra-High Reliability Applications. *IEEE Transactions on Nuclear Science*, 52(6):2630–2637, 2005. doi: 10.1109/TNS.2005.861080.

[158] Automotive Electronics Council (AEC). *AEC-Q101: Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors*. Automotive Electronics Council, 2023. URL http://www.aecouncil.com/Documents/AEC_Q101_Rev_E_Base_Document.pdf. Revision E.

[159] JEDEC Solid State Technology Association. *JESD22-A104F.01: Temperature Cycling*. JEDEC Solid State Technology Association, 2023. URL https://www.jedec.org/standards-documents/docs/jesd-22-a104e. Revision F.

[160] JEDEC Solid State Technology Association. *JESD22-A122B: Power Cycling*. JEDEC Solid State Technology Association, 2023. URL https://www.jedec.org/standards-documents/docs/jesd-22-a122.

[161] JEDEC Solid State Technology Association. *JESD22-A110E.01: Highly Accelerated Temperature and Humidity Stress Test (HAST)*. JEDEC Solid State Technology Association, May 2021. URL https://www.jedec.org/standards-documents/docs/jesd-22-a110c.

[162] JEDEC Solid State Technology Association. *JESD22-A108G: Temperature, Bias, and Operating Life*. JEDEC Solid State Technology Association, November 2022. URL https://www.jedec.org/sites/default/files/docs/22A108D.pdf.

[163] International Electrotechnical Commission. *IEC 61000-4-5: Electromagnetic Compatibility (EMC) – Part 4-5: Testing and Measurement Techniques – Surge Immunity Test*. International Electrotechnical Commission (IEC), 2014. URL https://webstore.iec.ch/en/publication/4223. Edition 3.0.

[164] Robert Allen and David Hartland. FAIR in Practice - Jisc Report on the Findable Accessible Interoperable and Reuseable Data Principles, May 2018. URL https://doi.org/10.5281/zenodo.1245568.

[165] Anna-Lena Lamprecht, Leyla Garcia, Mateusz Kuzak, Carlos Martinez, Ricardo Arcila, Eva Martin Del Pico, Victoria Dominguez Del Angel, Stephanie van de Sandt, Jon Ison, Paula Andrea Martinez, Peter McQuilton, Alfonso Valencia, Jennifer Harrow, Fotis Psomopoulos, Josep Ll. Gelpi, Neil Chue Hong, Carole Goble, and Salvador Capella-Gutierrez. Towards FAIR principles for research software. *Data Science*, 3(1): 37–59, 2020. doi: 10.3233/DS-190026. URL https://doi.org/10.3233/DS-190026.

[166] Michelle Barker, Neil P. Chue Hong, Daniel S. Katz, Anna-Lena Lamprecht, Carlos Martinez-Ortiz, Fotis Psomopoulos, Jennifer Harrow, Leyla Jael Castro, Morane Gruenpeter, Paula Andrea Martinez, and Tom Honeyman. Introducing the FAIR Prin-

ciples for Research Software. *Scientific Data*, 9(1):622, 2022. ISSN 2052-4463. doi: 10.1038/s41597-022-01710-x. URL https://doi.org/10.1038/s41597-022-01710-x.

[167] Emre Gurpinar and Alberto Castellazzi. Tradeoff Study of Heat Sink and Output Filter Volume in a GaN HEMT Based Single-Phase Inverter. *IEEE Transactions on Power Electronics*, 33(6):5226–5239, 2018. doi: 10.1109/TPEL.2017.2730038.

[168] Panteleimon Papamanolis, Thomas Guillod, Florian Krismer, and Johann W. Kolar. Minimum Loss Operation and Optimal Design of High-Frequency Inductors for Defined Core and Litz Wire. *IEEE Open Journal of Power Electronics*, 1:469–487, 2020. doi: 10.1109/OJPEL.2020.3027452.

[169] Shajjad Chowdhury, Emre Gurpinar, and Burak Ozpineci. Capacitor Technologies: Characterization, Selection, and Packaging for Next-Generation Power Electronics Applications. *IEEE Transactions on Transportation Electrification*, 8(2):2710–2720, 2022. doi: 10.1109/TTE.2021.3139806.

[170] Emre Gurpinar, Raj Sahu, and Burak Ozpineci. Heat Sink Design for WBG Power Modules Based on Fourier Series and Evolutionary Multi-Objective Multi-Physics Optimization. *IEEE Open Journal of Power Electronics*, 2:559–569, 2021. doi: 10.1109/OJPEL.2021.3119518.

[171] Aivars J. Lelis, Daniel Habersat, Ronald Green, Aderinto Ogunniyi, Moshe Gurfinkel, John Suehle, and Neil Goldsman. Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements. *IEEE Transactions on Electron Devices*, 55(8):1835–1840, 2008. doi: 10.1109/TED.2008.926672.

[172] Yutong Shen, Zhiyuan He, Yijun Shi, Hao Niu, Yuan Chen, Chang Liu, Yiqiang Chen, Zongqi Cai, Guoguang Lu, and Xianying Dai. Time-Dependent Degradation Mechanism of 1.2 kV SiC MOSFET Under Long-Term High-Temperature Gate

Bias Stress. *IEEE Transactions on Electron Devices*, 70(3):1162–1167, 2023. doi: 10.1109/TED.2022.3213774.

[173] Hao Bai, Chen Liu, Rui Ma, Damien Paire, and Fei Gao. Device-level Modelling and FPGA-based Real-time Simulation of the Power Electronic System in Fuel Cell Electric Vehicle. *IET Power Electronics*, 12:3479–3487, 2019. doi: 10.1049/iet-pel.2019.0101. URL https://digital-library.theiet.org/doi/abs/10.1049/iet-pel.2019.0101.

[174] Tian Liang and Venkata Dinavahi. Real-Time Device-Level Simulation of MMC-Based MVDC Traction Power System on MPSoC. *IEEE Transactions on Transportation Electrification*, 4(2):626–641, 2018. doi: 10.1109/TTE.2018.2823059.

[175] Zhuoxuan Shen and Venkata Dinavahi. Real-Time Device-Level Transient Electrothermal Model for Modular Multilevel Converter on FPGA. *IEEE Transactions on Power Electronics*, 31(9):6155–6168, 2016. doi: 10.1109/TPEL.2015.2503281.

[176] Hao Bai, Chen Liu, Akshay Kumar Rathore, Damien Paire, and Fei Gao. An FPGA-Based IGBT Behavioral Model With High Transient Resolution for Real-Time Simulation of Power Electronic Circuits. *IEEE Transactions on Industrial Electronics*, 66 (8):6581–6591, 2019. doi: 10.1109/TIE.2018.2870354.

[177] Rok Tavčar, Gabriela Maria Bordignon, Raúl Santiago Muñoz-Aguilar, and Peter Zajec. Enhancing Power Module Lifespan Through Power Distribution Approaches in a Three-Phase Interleaved DC/DC Converter. *IEEE Access*, 11:96784–96796, 2023. doi: 10.1109/ACCESS.2023.3311894.

[178] Abraham Marquez, Jose I. Leon, Sergio Vazquez, Leopoldo G. Franquelo, Giampaolo Buticchi, and Marco Liserre. Power Device Lifetime Extension of Dc-Dc Interleaved

Converters via Power Routing. In *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, pages 5332–5337, 2018. doi: 10.1109/IECON.2018.8592912.

[179] Sajib Chakraborty, Mohammed Mahedi Hasan, McGahan Paul, Dai-Duong Tran, Thomas Geury, Pooya Davari, Frede Blaabjerg, Mohamed El Baghdadi, and Omar Hegazy. Real-Life Mission Profile-Oriented Lifetime Estimation of a SiC Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(5):5142–5167, 2022. doi: 10.1109/JESTPE.2021.3083198.

[180] Marko Grebovic, Luka Filipovic, Ivana Katnic, Milica Vukotic, and Tomo Popovic. Overcoming Limitations of Statistical Methods with Artificial Neural Networks. In *2022 International Arab Conference on Information Technology (ACIT)*, pages 1–6, 2022. doi: 10.1109/ACIT57182.2022.9994218.

[181] Davide Anguita, Alessandro Ghio, Noemi Greco, Luca Oneto, and Sandro Ridella. Model Selection for Support Vector Machines: Advantages and Disadvantages of the Machine Learning Theory. In *The 2010 International Joint Conference on Neural Networks (IJCNN)*, pages 1–8, 2010. doi: 10.1109/IJCNN.2010.5596450.

[182] Iqbal H. Sarker. Machine Learning: Algorithms, Real-World Applications and Research Directions. *SN Computer Science*, 2(3):160, 2021. ISSN 2661-8907. doi: 10.1007/s42979-021-00592-x. URL https://doi.org/10.1007/s42979-021-00592-x. Review article. PMID: 33778771.

[183] Ander Udabe, Igor Baraia-Etxaburu, and David Garrido Diez. Gallium Nitride Power Devices: A State of the Art Review. *IEEE Access*, 11:48628–48650, 2023. doi: 10.1109/ACCESS.2023.3277200.

[184] Joseph Peter Kozak, Ruizhe Zhang, Matthew Porter, Qihao Song, Jingcun Liu, Bixuan Wang, Rudy Wang, Wataru Saito, and Yuhao Zhang. Stability, Reliability, and Robustness of GaN Power Devices: A Review. *IEEE Transactions on Power Electronics*, 38(7):8442–8471, 2023. doi: 10.1109/TPEL.2023.3266365.

[185] S.C. Binari, P.B. Klein, and T.E. Kazior. Trapping Effects in GaN and SiC Microwave FETs. *Proceedings of the IEEE*, 90(6):1048–1058, 2002. doi: 10.1109/JPROC.2002.1021569.

[186] T. Okino, M. Ochiai, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani. Drain Current DLTS of AlGaN-GaN MIS-HEMTs. *IEEE Electron Device Letters*, 25(8): 523–525, August 2004. ISSN 1558-0563. doi: 10.1109/LED.2004.832788.

[187] Mustapha Faqir, Giovanni Verzellesi, Alessandro Chini, Fausto Fantini, Francesca Danesin, Gaudenzio Meneghesso, Enrico Zanoni, and Christian Dua. Mechanisms of RF Current Collapse in AlGaN–GaN High Electron Mobility Transistors. *IEEE Transactions on Device and Materials Reliability*, 8(2):240–247, June 2008. ISSN 1558-2574. doi: 10.1109/TDMR.2008.922017.

[188] Jungwoo Joh and Jesús A. del Alamo. A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors. *IEEE Transactions on Electron Devices*, 58(1):132–140, January 2011. ISSN 1557-9646. doi: 10.1109/TED.2010.2087339.

[189] P. B. Klein and S. C. Binari. Photoionization Spectroscopy of Deep Defects Responsible for Current Collapse in Nitride-Based Field Effect Transistors. *Journal of Physics: Condensed Matter*, 15(44):R1641–R1667, October 2003. ISSN 0953-8984. doi: 10.1088/0953-8984/15/44/R01.

[190] I. Rossetto, M. Meneghini, A. Tajalli, S. Dalcanale, C. De Santi, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso. Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs. *IEEE Transactions on Electron Devices*, 64(9): 3734–3739, September 2017. ISSN 1557-9646. doi: 10.1109/TED.2017.2728785.

[191] Donghyun Jin and Jesús A. del Alamo. Methodology for the Study of Dynamic ON-Resistance in High-Voltage GaN Field-Effect Transistors. *IEEE Transactions on Electron Devices*, 60(10):3190–3196, October 2013. ISSN 1557-9646. doi: 10.1109/TED.2013.2274477.

[192] Shu Yang, Shaowen Han, Kuang Sheng, and Kevin J. Chen. Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(3):1425–1439, September 2019. ISSN 2168-6785. doi: 10.1109/JESTPE.2019.2925117.

[193] Alessandro Barbato, Marco Barbato, Matteo Meneghini, Marco Silvestri, Thomas Detzel, Oliver Haeberlen, Giorgio Spiazzi, Gaudenzio Meneghesso, and Enrico Zanoni. Fast System to Measure the Dynamic On-Resistance of on-Wafer 600 V Normally off GaN HEMTs in Hard-Switching Application Conditions. *IET Power Electronics*, 13(11): 2390–2397. ISSN 1755-4543. doi: 10.1049/iet-pel.2019.1455.

[194] M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. Van Hove, T.-L. Wu, S. Decoutere, G. Meneghesso, and E. Zanoni. Trapping in GaN-based Metal-Insulator-Semiconductor Transistors: Role of High Drain Bias and Hot Electrons. *Applied Physics Letters*, 104 (14):143505, April 2014. doi: 10.1063/1.4869680.

[195] Chunhua Zhou, Qimeng Jiang, Sen Huang, and Kevin J. Chen. Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices. *IEEE Electron Device Letters*, 33(8):1132–1134, 2012. doi: 10.1109/LED.2012.2200874.

[196] G Meneghesso, M Meneghini, I Rossetto, D Bisi, S Stoffels, M Van Hove, S Decoutere, and E Zanoni. Reliability and Parasitic Issues in GaN-based Power HEMTs: A Review. *Semiconductor Science and Technology*, 31(9):093004, aug 2016. doi: 10.1088/0268-1242/31/9/093004.

[197] Davide Bisi, Matteo Meneghini, Fabio Alessio Marino, Denis Marcon, Steve Stoffels, Marleen Van Hove, Stefaan Decoutere, Gaudenzio Meneghesso, and Enrico Zanoni. Kinetics of Buffer-Related RON-Increase in GaN-on-Silicon MIS-HEMTs. *IEEE Electron Device Letters*, 35(10):1004–1006, 2014. doi: 10.1109/LED.2014.2344439.

[198] Matteo Meneghini, Piet Vanmeerbeek, Riccardo Silvestri, Stefano Dalcanale, Abhishek Banerjee, Davide Bisi, Enrico Zanoni, Gaudenzio Meneghesso, and Peter Moens. Temperature-Dependent Dynamic R_{ON} in GaN-Based MIS-HEMTs: Role of Surface Traps and Buffer Leakage. *IEEE Transactions on Electron Devices*, 62(3):782–787, 2015. doi: 10.1109/TED.2014.2386391.

[199] Bin Lu, Tomas Palacios, Dilip Risbud, Sandeep Bahl, and David I. Anderson. Extraction of Dynamic On-Resistance in GaN Transistors: Under Soft- and Hard-Switching Conditions. In *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 1–4, October 2011. doi: 10.1109/CSICS.2011.6062461.

[200] Ke Li, Paul Evans, and Mark Johnson. SiC and GaN Power Transistors Switching Energy Evaluation in Hard and Soft Switching Conditions. In *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 123–128, 2016. doi: 10.1109/WiPDA.2016.7799922.

[201] Jiabei He, Gaofei Tang, and Kevin J. Chen. VTH Instability of p -GaN Gate HEMTs Under Static and Dynamic Gate Stress. *IEEE Electron Device Letters*, 39(10):1576–1579, 2018. doi: 10.1109/LED.2018.2867938.

[202] Hanxing Wang, Jin Wei, Ruiliang Xie, Cheng Liu, Gaofei Tang, and Kevin J. Chen. Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations. *IEEE Transactions on Power Electronics*, 32(7):5539–5549, 2017. doi: 10.1109/TPEL.2016.2610460.

[203] R. Vetury, N.Q. Zhang, S. Keller, and U.K. Mishra. The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs. *IEEE Transactions on Electron Devices*, 48(3):560–566, March 2001. ISSN 1557-9646. doi: 10.1109/16.906451.

[204] Michael J. Uren, Serge Karboyan, Indranil Chatterjee, Alexander Pooth, Peter Moens, Abhishek Banerjee, and Martin Kuball. "Leaky Dielectric" Model for the Suppression of Dynamic R_{on} in Carbon-Doped AlGaN/GaN HEMTs. *IEEE Transactions on Electron Devices*, 64(7):2826–2834, July 2017. ISSN 1557-9646. doi: 10.1109/TED.2017.2706090.

[205] Michael J. Uren, Marco Silvestri, Markus Cäsar, Godefridus Adrianus Maria Hurkx, Jeroen A. Croon, Jan Šonský, and Martin Kuball. Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths. *IEEE Electron Device Letters*, 35(3):327–329, March 2014. ISSN 1558-0563. doi: 10.1109/LED.2013.2297626.

[206] Hareesh Chandrasekar, Michael J. Uren, Abdalla Eblabla, Hassan Hirshy, Michael A. Casbon, Paul J. Tasker, Khaled Elgaid, and Martin Kuball. Buffer-Induced Current Collapse in GaN HEMTs on Highly Resistive Si Substrates. *IEEE Electron Device Letters*, 39(10):1556–1559, October 2018. ISSN 1558-0563. doi: 10.1109/LED.2018.2864562.

[207] Oliver Hilt, Eldad Bahat-Treidel, Eunjung Cho, Sebastian Singwald, and Joachim Würfl. Impact of Buffer Composition on the Dynamic On-State Resistance of High-Voltage AlGaN/GaN HFETs. In *2012 24th International Symposium on Power Semi-*

conductor Devices and ICs, pages 345–348, June 2012. doi: 10.1109/ISPSD.2012.6229092.

[208] Grayson Zulauf, Mattia Guacci, and Johann W. Kolar. Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks. *IEEE Transactions on Power Electronics*, 35(6):5581–5588, June 2020. ISSN 1941-0107. doi: 10.1109/TPEL.2019.2955656.

[209] P. Moens, P. Vanmeerbeek, A. Banerjee, J. Guo, C. Liu, P. Coppens, A. Salih, M. Tack, M. Caesar, M. J. Uren, M. Kuball, M. Meneghini, G. Meneghesso, and E. Zanoni. On the Impact of Carbon-Doping on the Dynamic Ron and off-State Leakage Current of 650V GaN Power Devices. In *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, pages 37–40, May 2015. doi: 10.1109/ISPSD.2015.7123383.

[210] Ruoyu Hou, Yanfeng Shen, Hui Zhao, Hao Hu, Juncheng Lu, and Teng Long. Power Loss Characterization and Modeling for GaN-Based Hard-Switching Half-Bridges Considering Dynamic on-State Resistance. *IEEE Transactions on Transportation Electrification*, 6(2):540–553, 2020. doi: 10.1109/TTE.2020.2989036.

[211] Ruoyu Hou and Juncheng Lu. The Effect of Dynamic On-State Resistance to System Losses in GaN-based Hard-Switching Applications. In *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–7, 2019.

[212] Tianyu Zhao, Rolando Burgos, and Jing Xu. Dynamic ON-Resistance Characterization of GaN HEMT Under Soft-Switching Condition. In *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 246–249, 2021. doi: 10.1109/WiPDA49284.2021.9645123.

[213] Ke Li, Arnaud Videt, Nadir Idir, Paul Leonard Evans, and Christopher Mark Johnson. Accurate Measurement of Dynamic On-State Resistances of GaN Devices Under Reverse and Forward Conduction in High Frequency Power Converter. *IEEE Transactions on Power Electronics*, 35(9):9650–9660, September 2020. ISSN 1941-0107. doi: 10.1109/TPEL.2019.2961604.

[214] Xiaomeng Geng, Carsten Kuring, Marvin Tannhaeuser, and Sibylle Dieckerhoff. Experimental Evaluation and Analysis of Dynamic On-Resistance in Hard- and Soft-switching Operation of a GaN GIT. In *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2020.

[215] A.P. Karmarkar, Bongim Jun, D.M. Fleetwood, R.D. Schrimpf, R.A. Weller, B.D. White, L.J. Brillson, and U.K. Mishra. Proton Irradiation Effects on GaN-based High Electron-Mobility Transistors with Si-doped Al/sub x/Ga/sub 1-x/N and Thick GaN Cap Layers. *IEEE Transactions on Nuclear Science*, 51(6):3801–3806, 2004. doi: 10.1109/TNS.2004.839199.

[216] Grayson Zulauf, Mattia Guacci, Juan M. Rivas-Davila, and Johann W. Kolar. The Impact of Multi-MHz Switching Frequencies on Dynamic On-Resistance in GaN-on-Si HEMTs. *IEEE Open Journal of Power Electronics*, 1:210–215, 2020. ISSN 2644-1314. doi: 10.1109/OJPEL.2020.3005879.

[217] Tommaso Cappello, Alberto Santarelli, and Corrado Florian. Dynamic RON Characterization Technique for the Evaluation of Thermal and Off-State Voltage Stress of GaN Switches. *IEEE Transactions on Power Electronics*, 33(4):3386–3398, 2018. doi: 10.1109/TPEL.2017.2710281.

[218] Carsten Kuring, Marvin Tannhaeuser, and Sibylle Dieckerhoff. Improvements on Dy-

namic On-State Resistance in Normally-off GaN HEMTs. In *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2019.

[219] Nasser Badawi, Oliver Hilt, Eldad Bahat-Treidel, Jan Böcker, Joachim Würfl, and Sibylle Dieckerhoff. Investigation of the Dynamic On-State Resistance of 600 V Normally-Off and Normally-On GaN HEMTs. *IEEE Transactions on Industry Applications*, 52(6):4955–4964, 2016. doi: 10.1109/TIA.2016.2585564.

[220] Chi Zhang, Siyang Liu, Sheng Li, Yanfeng Ma, Weihao Lu, Jingwen Huang, Weifeng Sun, Zhuo Yang, Yuanzheng Zhu, and Lihua Ni. Investigation on the Degradation Mechanism for GaN Cascode Device Under Repetitive Hard-Switching Stress. *IEEE Transactions on Power Electronics*, 37(5):6009–6017, 2022. doi: 10.1109/TPEL.2021.3125428.

[221] Grayson Zulauf, Mattia Guacci, Juan M. Rivas-Davila, and Johann W. Kolar. The Impact of Multi-MHz Switching Frequencies on Dynamic On-Resistance in GaN-on-Si HEMTs. *IEEE Open Journal of Power Electronics*, 1:210–215, 2020. doi: 10.1109/OJPEL.2020.3005879.

[222] Yichen Cai, Andrew J. Forsyth, and Rebecca Todd. Impact of GaN HEMT dynamic On-state Resistance on Converter Performance. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1689–1694, 2017. doi: 10.1109/APEC.2017.7930926.

[223] Fei Yang, Chi Xu, and Bilal Akin. Experimental Evaluation and Analysis of Switching Transient's Effect on Dynamic on-Resistance in GaN HEMTs. *IEEE Transactions on Power Electronics*, 34(10):10121–10135, October 2019. ISSN 1941-0107. doi: 10.1109/TPEL.2019.2890874.

[224] Jianming Lei, Rui Wang, Guo Yang, Jin Wang, Fulong Jiang, Dunjun Chen, Hai Lu, Rong Zhang, and Youdou Zheng. Precise Extraction of Dynamic Rdson Under High Frequency and High Voltage by a Double-Diode-Isolation Method. *IEEE Journal of the Electron Devices Society*, 7:690–695, 2019. ISSN 2168-6734. doi: 10.1109/JEDS.2019.2927608.

[225] Mattia Guacci, Dominik Bortis, and Johann W. Kolar. On-State Voltage Measurement of Fast Switching Power Semiconductors. *CPSS Transactions on Power Electronics and Applications*, 3(2):163–176, June 2018. ISSN 2475-742X. doi: 10.24295/CPSSTPEA.2018.00016.

[226] Donghyun Jin and Jesús A. del Alamo. Mechanisms Responsible for Dynamic ON-resistance in GaN High-Voltage HEMTs. In *2012 24th International Symposium on Power Semiconductor Devices and ICs*, pages 333–336, 2012. doi: 10.1109/ISPSD.2012.6229089.

[227] Thomas Foulkes, Tomas Modeer, and Robert C. N. Pilawa-Podgurski. Developing a Standardized Method for Measuring and Quantifying Dynamic On-State Resistance via a Survey of Low Voltage GaN HEMTs. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2717–2724, March 2018. doi: 10.1109/APEC.2018.8341401.

[228] Thomas Foulkes, Tomas Modeer, and Robert C. N. Pilawa-Podgurski. Quantifying Dynamic On-State Resistance of GaN HEMTs for Power Converter Design via a Survey of Low and High Voltage Devices. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(4):4036–4049, 2021. doi: 10.1109/JESTPE.2020.3024930.

[229] Alexei Koudymov, Michael S. Shur, Grigory Simin, Kanin Chu, P. C. Chao, Cathy Lee, Jose Jimenez, and Anthony Balistreri. Analytical HFET I– V Model in Presence

of Current Collapse. *IEEE Transactions on Electron Devices*, 55(3):712–720, 2008. doi: 10.1109/TED.2007.915092.

[230] A. Koudymov, M. S. Shur, and G. Simin. Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *IEEE Electron Device Letters*, 28(5):332–335, 2007. doi: 10.1109/LED.2007.895389.

[231] D. Godfrey, D. Nirmal, L. Arivazhagan, D. Godwinraj, N. Mohan Kumar, Yulin Chen, and Wenkuan Yeh. Current Collapse Degradation in GaN High Electron Mobility Transistor by Virtual Gate. *Microelectronics Journal*, 118:105293, 2021. ISSN 0026-2692. doi: https://doi.org/10.1016/j.mejo.2021.105293.

[232] Changsi Wang, Yuehang Xu, Xuming Yu, Chunjiang Ren, Zhensheng Wang, Haiyan Lu, Tangsheng Chen, Bin Zhang, and Ruimin Xu. An Electrothermal Model for Empirical Large- Signal Modeling of AlGaN/GaN HEMTs Including Self-Heating and Ambient Temperature Effects. *IEEE Transactions on Microwave Theory and Techniques*, 62(12):2878–2887, 2014. doi: 10.1109/TMTT.2014.2364821.

[233] Benedikt Kohlhepp, Daniel Kübrich, and Thomas Dürbaum. Measuring and Modeling of Dynamic On-State Resistance of GaN-HEMTs. In *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, pages P.1–P.10, 2019. doi: 10.23919/EPE.2019.8915553.

[234] Ke Li, Paul Leonard Evans, and Christopher Mark Johnson. Characterisation and Modeling of Gallium Nitride Power Semiconductor Devices Dynamic On-State Resistance. *IEEE Transactions on Power Electronics*, 33(6):5262–5273, 2018. doi: 10.1109/TPEL.2017.2730260.

[235] Ke Li, Arnaud Videt, Nadir Idir, Paul Evans, and Mark Johnson. Modelling GaN-HEMT Dynamic ON-state Resistance in High Frequency Power Converter. In *2020*

IEEE Applied Power Electronics Conference and Exposition (APEC), pages 1949–1955, 2020. doi: 10.1109/APEC39645.2020.9124513.

[236] Ke Li, Paul Leonard Evans, Christopher Mark Johnson, Arnaud Videt, and Nadir Idir. A GaN-HEMT Compact Model Including Dynamic RDSon Effect for Power Electronics Converters. *Energies*, 14(8), 2021. ISSN 1996-1073. doi: 10.3390/en14082092.

[237] Dejana Čučak, Miroslav Vasić, Oscar García, Jesús Angel Oliver, Pedro Alou, José Antonio Cobos, Ashu Wang, Sara Martín-Horcajo, Maria Fatima Romero, and Fernando Calle. Physics-Based Analytical Model for Input, Output, and Reverse Capacitance of a GaN HEMT With the Field-Plate Structure. *IEEE Transactions on Power Electronics*, 32(3):2189–2202, 2017. doi: 10.1109/TPEL.2016.2569404.

[238] Binit Syamal, Xing Zhou, Siau Ben Chiah, Anand M. Jesudas, Subramaniam Arulkumaran, and Geok Ing Ng. A Comprehensive Compact Model for GaN HEMTs, Including Quasi-Steady-State and Transient Trap-Charge Effects. *IEEE Transactions on Electron Devices*, 63(4):1478–1485, 2016. doi: 10.1109/TED.2016.2533165.

[239] Huili Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U.K. Mishra. High Breakdown Voltage AlGaN-GaN HEMTs Achieved by Multiple Field Plates. *IEEE Electron Device Letters*, 25(4):161–163, April 2004. ISSN 1558-0563. doi: 10.1109/LED.2004.824845.

[240] Rongming Chu, Andrea Corrion, Mary Chen, Ray Li, Danny Wong, Daniel Zehnder, Brian Hughes, and Karim Boutros. 1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance. *IEEE Electron Device Letters*, 32(5): 632–634, May 2011. ISSN 1558-0563. doi: 10.1109/LED.2011.2118190.

[241] Yasuhiro Uemoto, Masahiro Hikita, Hiroaki Ueno, Hisayoshi Matsuo, Hidetoshi Ishida, Manabu Yanagihara, Tetsuzo Ueda, Tsuyoshi Tanaka, and Daisuke Ueda. Gate Injec-

tion Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation. *IEEE Transactions on Electron Devices*, 54(12):3393–3399, 2007. doi: 10.1109/TED.2007.908601.

[242] Y.-F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavarkar, T. Wisleder, U.K. Mishra, and P. Parikh. 30-W/mm GaN HEMTs by Field Plate Optimization. *IEEE Electron Device Letters*, 25(3):117–119, 2004. doi: 10.1109/LED.2003.822667.

[243] Shreepad Karmalkar and Umesh K. Mishra. Very High Voltage AlGaN/GaN High Electron Mobility Transistors Using a Field Plate Deposited on a Stepped Insulator. *Solid-State Electronics*, 45(9):1645–1652, 2001. ISSN 0038-1101. doi: https://doi.org/10.1016/S0038-1101(01)00158-7.

[244] S. Karmalkar, M.S. Shur, G. Simin, and M.A. Khan. Field-Plate Engineering for HFETs. *IEEE Transactions on Electron Devices*, 52(12):2534–2540, 2005. doi: 10.1109/TED.2005.859568.

[245] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, T. Domon, I. Omura, and M. Yamaguchi. 380v/1.9A GaN power-HEMT: Current Collapse Phenomena Under High Applied Voltage and Demonstration of 27.1 MHz Class-E Amplifier. In *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, pages 586–589, 2005. doi: 10.1109/IEDM.2005.1609415.

[246] Bingyao Sun, Rolando Burgos, Xuning Zhang, and Dushan Boroyevich. Active dv/dt Control of 600V GaN Transistors. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, 2016. doi: 10.1109/ECCE.2016.7854818.

[247] Xiucheng Huang, Zhengyang Liu, Qiang Li, and Fred C. Lee. Evaluation and Application of 600 V GaN HEMT in Cascode Structure. *IEEE Transactions on Power Electronics*, 29(5):2453–2461, 2014. doi: 10.1109/TPEL.2013.2276127.

[248] Shaocheng Li, Shu Yang, Shaowen Han, and Kuang Sheng. Investigation of Temperature-Dependent Dynamic RON of GaN HEMT with Hybrid-Drain under Hard and Soft Switching. In *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 306–309, 2020. doi: 10.1109/ISPSD46842.2020.9170048.

[249] Zonglun Xie, Xinke Wu, Zezheng Dong, Jiahui Sun, Kuang Sheng, and Kevin J. Chen. Dynamic On-Resistance Characterization of GaN Power HEMTs Under Forward/Reverse Conduction Using Multigroup Double Pulse Test. *IEEE Transactions on Power Electronics*, 39(2):1963–1967, 2024. doi: 10.1109/TPEL.2023.3331891.

[250] Rustam Kumar, Arnab Sarkar, Sandeep Anand, Amit Verma, and Tian-Li Wu. H-Bridge Derived Topology for Dynamic On-Resistance Evaluation in Power GaN HEMTs. *IEEE Transactions on Industrial Electronics*, 70(2):1532–1541, 2023. doi: 10.1109/TIE.2022.3161822.

[251] Nasser Badawi, Oliver Hilt, Eldad Behat-Treidel, Jan Böcker, Joachim Würfl, and Sibylle Dieckerhoff. Investigation of the Dynamic On-State Resistance of 600V Normally-off and Normally-on GaN HEMTs. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 913–919, 2015. doi: 10.1109/ECCE.2015.7309785.

[252] Hongkeng Zhu and Elison Matioli. Accurate Measurement of Dynamic ON-Resistance in GaN Transistors at Steady-State. *IEEE Transactions on Power Electronics*, 38(7):8045–8050, 2023. doi: 10.1109/TPEL.2023.3268890.

[253] Wei Wang, Yan Liang, Minghui Zhang, Fang Lin, Feng Wen, and Hongxing Wang. Mechanism Analysis of Dynamic On-State Resistance Degradation for a Commercial

GaN HEMT Using Double Pulse Test. *Electronics*, 10(10), 2021. ISSN 2079-9292. doi: 10.3390/electronics10101202.

[254] Edward A. Jones and Alejandro Pozo. Hard-Switching Dynamic Rds,on Characterization of a GaN FET with an Active GaN-Based Clamping Circuit. In *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2757–2763, 2019. doi: 10.1109/APEC.2019.8722177.

[255] Carsten Kuring, Kornelius Tetzner, Andreas Popp, Sören Heucke, Oliver Hilt, Saud Bin Anooz, Joachim Würfl, and Sibylle Dieckerhoff. Switching Behavior and Dynamic On-resistance of Lateral -Ga2 O3 MOSFETs up to 400 V. In *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 52–57, 2021. doi: 10.1109/WiPDA49284.2021.9645079.

[256] Alberto Santarelli, Rafael Cignani, Daniel Niessen, Pier Andrea Traverso, and Fabio Filicori. New Pulsed Measurement Setup for GaN and GaAs FETs Characterization. *International Journal of Microwave and Wireless Technologies*, 4(3):387–397, 2012. doi: 10.1017/S1759078712000335.

[257] Shaowen Han, Shu Yang, Rui Li, Xinke Wu, and Kuang Sheng. Current-Collapse-Free and Fast Reverse Recovery Performance in Vertical GaN-on-GaN Schottky Barrier Diode. *IEEE Transactions on Power Electronics*, 34(6):5012–5018, 2019. doi: 10.1109/TPEL.2018.2876444.

[258] *Guideline to Specify a Transient Off-State Withstand Voltage Robustness Indicator in Datasheets for Lateral GaN Power Conversion Devices, Version 1.0 | JEDEC.*

[259] Benedikt Kohlhepp, Daniel Kübrich, Marvin Tannhäuser, Andreas Hoffmann, and Thomas Dürbaum. Test Setup for Dynamic ON-State Resistance Measurement of

High- and Low-Voltage GaN-HEMTs Under Hard and Soft Switching Operations. *IEEE Transactions on Instrumentation and Measurement*, 69(10):7740–7751, 2020. doi: 10.1109/TIM.2020.2985186.

[260] Benedikt Kohlhepp, Carsten Kuring, Stefan Peller, and Daniel Kübrich. Measurement of Dynamic On-State Resistance of High-Voltage GaN-HEMTs under Real Application Conditions. In *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, pages 1–10, 2020. doi: 10.23919/EPE20ECCEEurope43536.2020.9215744.

[261] Alberto Santarelli, Rafael Cignani, Gian Piero Gibiino, Daniel Niessen, Pier Andrea Traverso, Corrado Florian, Dominique M. M. P. Schreurs, and Fabio Filicori. A Double-Pulse Technique for the Dynamic I/V Characterization of GaN FETs. *IEEE Microwave and Wireless Components Letters*, 24(2):132–134, 2014. doi: 10.1109/LMWC.2013.2290216.

[262] Wataru Saito, Tomohiro Nitta, Yorito Kakiuchi, Yasunobu Saito, Kunio Tsuda, Ichiro Omura, and Masakazu Yamaguchi. A 120-W Boost Converter Operation Using a High-Voltage GaN-HEMT. *IEEE Electron Device Letters*, 29(1):8–10, 2008. doi: 10.1109/LED.2007.910796.

[263] Bryson J. Galapon, Alex J. Hanson, and David J. Perreault. Measuring Dynamic On Resistance in GaN Transistors at MHz Frequencies. In *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–8, 2018. doi: 10.1109/COMPEL.2018.8460051.

[264] *Dynamic On-resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices, Version 1.0 | JEDEC*.

[265] Carlos Bernal, Manuel Jimenez, and Fabio Andrade. Evaluating the JEDEC Standard JEP173, Dynamic RDSON Test Method for GaN HEMTs. In *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4, October 2020. doi: 10.1109/ISCAS45731.2020.9181147.

[266] Device Dynamics Lab. Device Dynamics Lab. https://devicedynamicslab.com/, 2024. Accessed: 2024-01-27.

[267] Fei Yang, Chi Xu, and Bilal Akin. Experimental Evaluation and Analysis of Switching Transient's Effect on Dynamic on-Resistance in GaN HEMTs. *IEEE Transactions on Power Electronics*, 34(10):10121–10135, 2019. doi: 10.1109/TPEL.2019.2890874.

[268] José Millán, Philippe Godignon, Xavier Perpiñà, Amador Pérez-Tomás, and José Rebollo. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Transactions on Power Electronics*, 29(5):2155–2163, 2014. doi: 10.1109/TPEL.2013.2268900.

[269] H. Alan Mantooth, Michael D. Glover, and Paul Shepherd. Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(3):374–385, 2014. doi: 10.1109/JESTPE.2014.2313511.

[270] Ahmed Abuelnaga, Mehdi Narimani, and Amir Sajjad Bahman. A Review on IGBT Module Failure Modes and Lifetime Testing. *IEEE Access*, 9:9643–9663, 2021. doi: 10.1109/ACCESS.2021.3049738.

[271] Xin Yang, Siwei Xu, Ke Heng, and Xinlong Wu. Distributed Thermal Modeling for Power Devices and Modules With Equivalent Heat Flow Path Extraction. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(6):5863–5876, 2023. doi: 10.1109/JESTPE.2023.3321210.

[272] B. Jayant Baliga. Power MOSFETs. In *Fundamentals of Power Semiconductor Devices*, pages 283–520. Springer International Publishing, 2nd edition, 2019. ISBN 978-3-319-93988-9. doi: 10.1007/978-3-319-93988-9_6.

[273] Enes Ugur, Fei Yang, Shi Pu, Shuai Zhao, and Bilal Akin. Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling. *IEEE Transactions on Industry Applications*, 55(3):2858–2867, 2019. doi: 10.1109/TIA.2019.2891214.

[274] José R. Celaya, Abhinav Saxena, Sankalita Saha, Vladislav Vashchenko, and Kai Goebel. Prognostics of Power MOSFET. In *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, pages 160–163, 2011. doi: 10.1109/ISPSD.2011.5890815.

[275] Ruizhe Zhang, Ricardo Garcia, Robert Strittmatter, Yuhao Zhang, and Shengke Zhang. In-situ RDS(on) Characterization and Lifetime Projection of GaN HEMTs Under Repetitive Overvoltage Switching. *IEEE Transactions on Power Electronics*, 38(9):10589–10594, 2023. doi: 10.1109/TPEL.2023.3290117.

[276] Antonio Griffo, Jiabin Wang, Kalhana Colombage, and Tamer Kamel. Real-Time Measurement of Temperature Sensitive Electrical Parameters in SiC Power MOSFETs. *IEEE Transactions on Industrial Electronics*, 65(3):2663–2671, 2018. doi: 10.1109/TIE.2017.2739687.

[277] Shu Yang, Shaowen Han, Kuang Sheng, and Kevin J. Chen. Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(3):1425–1439, 2019. doi: 10.1109/JESTPE.2019.2925117.

[278] Hanxing Wang, Jin Wei, Ruiliang Xie, Cheng Liu, Gaofei Tang, and Kevin J. Chen. Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations. *IEEE Transactions on Power Electronics*, 32(7):5539–5549, 2017. doi: 10.1109/TPEL.2016.2610460.

[279] I. Rossetto, M. Meneghini, A. Tajalli, S. Dalcanale, C. De Santi, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso. Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs. *IEEE Transactions on Electron Devices*, 64(9): 3734–3739, 2017. doi: 10.1109/TED.2017.2728785.

[280] Armin Jafari, Mohammad Samizadeh Nikoo, Nirmana Perera, Halil Kerim Yildirim, Furkan Karakaya, Reza Soleimanzadeh, and Elison Matioli. Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies. *IEEE Transactions on Power Electronics*, 35(12):12595–12600, 2020. doi: 10.1109/TPEL.2020.2990628.

[281] Hussain Sayed, Gnana Sambandam Kulothungan, and Harish S. Krishnamoorthy. Characterization of GaN HEMTs' Aging Precursors and Activation Energy Under a Wide Range of Thermal Cycling Tests. *IEEE Open Journal of the Industrial Electronics Society*, 4:123–134, 2023. doi: 10.1109/OJIES.2023.3267004.

[282] Furkan Karakaya, Anuj Maheshwari, Arijit Banerjee, John S. Donnal, Adam J. Morgan, and Woongje Sung. In-Situ Detection of Bond Wire Lift-Off Events in Operational SiC MOSFETs. *IEEE Transactions on Power Electronics*, pages 1–14, 2024. doi: 10.1109/TPEL.2024.3446750.

[283] Krishna Shenai. The Figure of Merit of a Semiconductor Power Electronics Switch. *IEEE Transactions on Electron Devices*, 65(10):4216–4224, 2018. doi: 10.1109/TED.2018.2866360.

[284] A.Q. Huang. New Unipolar Switching Power Device Figures of Merit. *IEEE Electron Device Letters*, 25(5):298–301, 2004. doi: 10.1109/LED.2004.826533.

[285] Davide Cittanti, Enrico Vico, and Iustin Radu Bojoi. New FOM-Based Performance Evaluation of 600/650 V SiC and GaN Semiconductors for Next-Generation EV Drives. *IEEE Access*, 10:51693–51707, 2022. doi: 10.1109/ACCESS.2022.3174777.

[286] Paula Diaz Reigosa, Francesco Iannuzzo, Haoze Luo, and Frede Blaabjerg. A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules. *IEEE Transactions on Industry Applications*, 53(3):2880–2887, 2017. doi: 10.1109/TIA.2016.2628895.

[287] Alberto Castellazzi. Comprehensive Compact Models for the Circuit Simulation of Multichip Power Modules. *IEEE Transactions on Power Electronics*, 25(5):1251–1264, 2010. doi: 10.1109/TPEL.2009.2036728.

[288] Diang Xing, Boxue Hu, Minseok Kang, Yue Zhang, Suvendu Nayak, Jin Wang, and Anant K. Agarwal. 1200-V SiC MOSFET Short-Circuit Ruggedness Evaluation and Methods to Improve Withstand Time. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(5):5059–5069, 2022. doi: 10.1109/JESTPE.2022.3144995.

[289] Hongfang Wang, Fred Wang, and Junhong Zhang. Power Semiconductor Device Figure of Merit for High-Power-Density Converter Design Applications. *IEEE Transactions on Electron Devices*, 55(1):466–470, 2008. doi: 10.1109/TED.2007.910573.

[290] K Shenai. High-Density Power Conversion and Wide-Bandgap Semiconductor Power Electronics Switching Devices. *Proceedings of the IEEE*, 107(12):2308–2326, 2019. doi: 10.1109/JPROC.2019.2948554.

[291] Zheng Zeng, Jin Wang, Liang Wang, Yue Yu, and Kaihong Ou. Inaccurate Switching

Loss Measurement of SiC MOSFET Caused by Probes: Modelization, Characterization, and Validation. *IEEE Transactions on Instrumentation and Measurement*, 70: 1–14, 2021. doi: 10.1109/TIM.2020.3024356.

[292] David Garrido, Igor Baraia-Etxaburu, Joseba Arza, and Manex Barrenetxea. Simple and Affordable Method for Fast Transient Measurements of SiC Devices. *IEEE Transactions on Power Electronics*, 35(3):2933–2942, 2020. doi: 10.1109/TPEL.2019.2924358.

[293] Ken Johnson and David Maliniak. Oscilloscope Probes for Power Electronics: Be Sure to Choose the Right Probe for Accurate Measurements. *IEEE Power Electronics Magazine*, 5(1):37–44, 2018. doi: 10.1109/MPEL.2017.2782399.

[294] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits*. Oxford University Press, eighth edition, 2019.

[295] Yoshiaki Nozaki, Hiroshi Kawamura, John Kevin Twynam, and Masatomo Hasegawa. Voltage Clamp Circuit and Semiconductor Device, U.S. Patent US 2008/0309355A1, Dec. 2008.

[296] Mattia Guacci, Dominik Bortis, and Johann W. Kolar. On-state Voltage Measurement of Fast Switching Power Semiconductors. *CPSS Transactions on Power Electronics and Applications*, 3(2):163–176, 2018. doi: 10.24295/CPSSTPEA.2018.00016.

[297] Nasser Badawi and Sibylle Dieckerhoff. A new Method for Dynamic Ron Extraction of GaN Power HEMTs. In *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–6, 2015.

[298] Ratmir Gelagaev, Pieter Jacqmaer, and Johan Driesen. A Fast Voltage Clamp Circuit

for the Accurate Measurement of the Dynamic ON-Resistance of Power Transistors. *IEEE Transactions on Industrial Electronics*, 62(2):1241–1250, 2015. doi: 10.1109/TIE.2014.2349876.

[299] Lee Gill, Luciano Andres Garcia Rodriguez, Jacob Mueller, Robert Kaplar, and Alan J. Michaels. Novel Dynamic ON-Resistance Measurement Circuit Topology, Operation, and Performance for High Voltage GaN Power HEMTs. In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 5398–5405, 2023. doi: 10.1109/ECCE53617.2023.10362641.

[300] Lee Gill, Jonas Actor, Robert J. Kaplar, and Alan J. Michaels. Machine Learning Based Non-Intrusive Inspection Technique to Quantify GaN HEMT Characteristics. In *2023 IEEE Design Methodologies Conference (DMC)*, pages 1–6, 2023. doi: 10.1109/DMC58182.2023.10412423.

[301] Nasser Badawi, Oliver Hilt, Eldad Bahat-Treidel, Jan Böcker, Joachim Würfl, and Sibylle Dieckerhoff. Investigation of the Dynamic On-State Resistance of 600 V Normally-Off and Normally-On GaN HEMTs. *IEEE Transactions on Industry Applications*, 52(6):4955–4964, 2016. doi: 10.1109/TIA.2016.2585564.

[302] Bin Lu, Tomas Palacios, Dilip Risbud, Sandeep Bahl, and David I. Anderson. Extraction of Dynamic On-Resistance in GaN Transistors: Under Soft- and Hard-Switching Conditions. In *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 1–4, 2011. doi: 10.1109/CSICS.2011.6062461.

[303] Alessandro Barbato, Marco Barbato, Matteo Meneghini, Marco Silvestri, Thomas Detzel, Oliver Haeberlen, Giorgio Spiazzi, Gaudenzio Meneghesso, and Enrico Zanoni. Fast System to measure the dynamic on-resistance of on-wafer 600 V normally off

GaN HEMTs in hard-switching application conditions. *IET Power Electronics*, 13 (11):2390–2397, 2020. doi: https://doi.org/10.1049/iet-pel.2019.1455.

[304] Nicola Modolo, Carlo De Santi, Andrea Minetto, Luca Sayadi, Sebastien Sicre, Gerhard Prechtl, Gaudenzio Meneghesso, Enrico Zanoni, and Matteo Meneghini. Cumulative Hot-Electron Trapping in GaN-Based Power HEMTs Observed by an Ultrafast (10 V/Ns) On-Wafer Methodology. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(5):5019–5026, 2022. doi: 10.1109/JESTPE.2021.3077127.

[305] Pedro Javier Martínez, Pablo Fernández Miaja, Enrique Maset, and Juan Rodríguez. A Test Circuit for GaN HEMTs Dynamic R_{ON} Characterization in Power Electronics Applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7 (3):1456–1464, 2019. doi: 10.1109/JESTPE.2019.2912130.

[306] Byung-Do Yang, Jang-Su Kim, Jin-Kuk Yun, Yong-Kyu Lee, and Jee-Sue Lee. A highly Accurate BiCMOS Cascode Current Mirror for Wide Output Voltage Range. In *2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2314–2317, 2008. doi: 10.1109/ISCAS.2008.4541917.

[307] GeneSiC. G3F60MT06K Datasheet, 2024. URL https://navitassemi.com/wp-content/plugins/gb-navitas-stock-checker/product_files/G3F60MT06K.pdf. Accessed: 2025-01-16.

[308] Tektronix, Inc. IsoVu Generation 2 Technology White Paper, 2020. URL https://www.tek.com/en/documents/whitepaper/isovu-generation-2-technology-white-paper. Accessed: 2025-01-16.

[309] PMK Mess- & Kommunikationstechnik GmbH. FireFly® Datasheet, 2024. URL https://www.pmk.de/files/downloads/FireFly%C2%AE%20Datasheet.pdf. Accessed: 2025-01-16.

[310] Springburo. The Clipper CLP1500V15A1 Measurement Probe. https://www.saelig.com/product/MFR00150001.htm, 2025. Accessed: April 15, 2025.

[311] *Power Spectrum Analysis*, volume ISTFA 2017: Conference Proceedings from the 43rd International Symposium for Testing and Failure Analysis of *International Symposium for Testing and Failure Analysis*, 11 2017. doi: 10.31399/asm.cp.istfa2017p0073. URL https://doi.org/10.31399/asm.cp.istfa2017p0073.

[312] B. Moore. Principal Component Analysis in Linear Systems: Controllability, Observability, and Model Reduction. *IEEE Transactions on Automatic Control*, 26(1):17–32, 1981. doi: 10.1109/TAC.1981.1102568.

[313] Fengxi Song, Zhongwei Guo, and Dayong Mei. Feature Selection Using Principal Component Analysis. In *2010 International Conference on System Science, Engineering Design and Manufacturing Informatization*, volume 1, pages 27–30, 2010. doi: 10.1109/ICSEM.2010.14.

[314] Yaguo Lei, Feng Jia, Jing Lin, Saibo Xing, and Steven X. Ding. An Intelligent Fault Diagnosis Method Using Unsupervised Feature Learning Towards Mechanical Big Data. *IEEE Transactions on Industrial Electronics*, 63(5):3137–3147, 2016. doi: 10.1109/TIE.2016.2519325.

[315] S. Lloyd. Least Squares Quantization in PCM. *IEEE Transactions on Information Theory*, 28(2):129–137, 1982. doi: 10.1109/TIT.1982.1056489.

[316] Chunhui Yuan and Haitao Yang. Research on k-value selection method of k-means clustering algorithm. *J*, 2(2):226–235, 2019. ISSN 2571-8800. doi: 10.3390/j2020016. URL https://www.mdpi.com/2571-8800/2/2/16.

[317] Shunji Oki, Shigeaki Ishikawa, and Takeshi Ikemi. Development of High-Power and

High-Efficiency Motor for a Newly Developed Electric Vehicle. *SAE International Journal of Alternative Powertrains*, 1(1):104–111, 2012. ISSN 21674191, 21674205.

[318] John Reimers, Lea Dorn-Gomba, Christopher Mak, and Ali Emadi. Automotive Traction Inverters: Current Status and Future Trends. *IEEE Transactions on Vehicular Technology*, 68(4):3337–3350, 2019. doi: 10.1109/TVT.2019.2897899.

[319] F. Briz, A. Diez, M.W. Degner, and R.D. Lorenz. Current and Flux Regulation in Field-Weakening Operation of Induction Motors. *IEEE Transactions on Industry Applications*, 37(1):42–50, 2001. doi: 10.1109/28.903125.

[320] R.N. Jazar. *Vehicle Dynamics: Theory and Application*. 2nd. Springer New York, 2013. ISBN 9781461485445.

[321] Hans B. Pacejka. Chapter 4 - Semi-Empirical Tire Models. In Hans B. Pacejka, editor, *Tire and Vehicle Dynamics (Third Edition)*, pages 149–209. Butterworth-Heinemann, Oxford, third edition edition, 2012. ISBN 978-0-08-097016-5. doi: https://doi.org/10.1016/B978-0-08-097016-5.00004-8.

[322] J.W. Kolar, T.M. Wolbank, and M. Schrodl. Analytical Calculation of the RMS Current Stress on the DC Link Capacitor of Voltage DC Link PWM Converter Systems. In *1999. Ninth International Conference on Electrical Machines and Drives (Conf. Publ. No. 468)*, pages 81–89, 1999. doi: 10.1049/cp:19990995.

[323] Tianyu Chen, Sen Li, and Babak Fahimi. Analysis of DC-Link Voltage Ripple in Voltage Source Inverters without Electrolytic Capacitor. In *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, pages 1041–1048, 2018. doi: 10.1109/IECON.2018.8591719.

[324] Milad Bahrami-Fard, Tianyu Chen, Ethan Alejandro Winchell, and Babak Fahimi.

Integrated Induction Motor Drive for Variable Speed Industrial Applications. *IEEE Transactions on Power Electronics*, 40(5):7176–7188, 2025. doi: 10.1109/TPEL.2025.3532880.

[325] Qi Li, Shi Cheng, Yonghe Chen, Jian Ye, Xianwen Cui, and Pei Li. Study on Cauer Thermal Network Model Considering Bidirectional Heat Transfer. *IEEE Access*, 12: 90525–90534, 2024. doi: 10.1109/ACCESS.2024.3419921.

[326] Xin Yang, Ke Heng, Xingyu Dai, Xinlong Wu, and Guoyou Liu. A Temperature-Dependent Cauer Model Simulation of IGBT Module With Analytical Thermal Impedance Characterization. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(3):3055–3065, 2022. doi: 10.1109/JESTPE.2021.3128017.

[327] Reinhold Bayerer, Tobias Herrmann, Thomas Licht, Josef Lutz, and Marco Feller. Model for Power Cycling lifetime of IGBT Modules - Various Factors Influencing Lifetime. In *5th International Conference on Integrated Power Electronics Systems*, pages 1–6, 2008.

[328] Ke Ma, Huai Wang, and Frede Blaabjerg. New Approaches to Reliability Assessment: Using Physics-of-Failure for Prediction and Design in Power Electronics Systems. *IEEE Power Electronics Magazine*, 3(4):28–41, 2016. doi: 10.1109/MPEL.2016.2615277.

[329] Ke Ma, Ui-Min Choi, and Frede Blaabjerg. Prediction and Validation of Wear-Out Reliability Metrics for Power Semiconductor Devices With Mission Profiles in Motor Drive Application. *IEEE Transactions on Power Electronics*, 33(11):9843–9853, 2018. doi: 10.1109/TPEL.2018.2798585.

[330] Ivana Kovacevic-Badstuebner, Elena Mengotti, Philipp Natzke, Salvatore Race, Enea Bianda, Joni Jormanainen, and Ulrike Grossner. Power Cycling of Sintered SiC Power

MOSFET Baseplate-less Modules with Aluminum Oxide and Silicon Nitride Substrates. In *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 60–63, 2023. doi: 10.1109/ISPSD57135.2023.10147471.

[331] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan. A fast and Elitist Multi-Objective Genetic Algorithm: NSGA-II. *IEEE Transactions on Evolutionary Computation*, 6(2): 182–197, 2002. doi: 10.1109/4235.996017.

[332] J.H. Allmeling and W.P. Hammer. PLECS-piece-wise Linear Electrical Circuit Simulation for Simulink. In *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No.99TH8475)*, volume 1, pages 355–360 vol.1, 1999. doi: 10.1109/PEDS.1999.794588.

[333] Julian Blank and Kalyanmoy Deb. Pymoo: Multi-Objective Optimization in Python. *IEEE Access*, 8:89497–89509, 2020. doi: 10.1109/ACCESS.2020.2990567.

[334] US Environmental Protection Agency (EPA). Dynamometer Drive Schedules. URL https://www.epa.gov/vehicle-and-fuel-emissions-testing/dynamometer-drive-schedules.

[335] James A. Cooper and Dallas T. Morisette. Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC. *IEEE Electron Device Letters*, 41(6):892–895, 2020. doi: 10.1109/LED.2020.2987282.

[336] D.T. Morisette and J.A. Cooper. Theoretical Comparison of SiC PiN and Schottky Diodes based on Power Dissipation Considerations. *IEEE Transactions on Electron Devices*, 49(9):1657–1664, 2002. doi: 10.1109/TED.2002.801290.

[337] Harshad Surdi, Franz A. M. Koeck, Mohammad Faizan Ahmad, Trevor J. Thornton, Robert J. Nemanich, and Stephen M. Goodnick. Demonstration and Analysis of Ul-

trahigh Forward Current Density Diamond Diodes. *IEEE Transactions on Electron Devices*, 69(1):254–261, 2022. doi: 10.1109/TED.2021.3125914.

[338] Jack Flicker and Robert Kaplar. Design Optimization of GaN Vertical Power Diodes and Comparison to Si and SiC. In *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 31–38, 2017. doi: 10.1109/WiPDA.2017.8170498.

[339] André De Bastiani Lange, Thiago Batista Soeiro, Márcio Silveira Ortmann, and Marcelo Lobo Heldwein. Three-Level Single-Phase Bridgeless PFC Rectifiers. *IEEE Transactions on Power Electronics*, 30(6):2935–2949, 2015. doi: 10.1109/TPEL.2014.2322314.

[340] Lakshmi Reddy GopiReddy, Leon M. Tolbert, Burak Ozpineci, and João O. P. Pinto. Rainflow Algorithm-Based Lifetime Estimation of Power Semiconductors in Utility Applications. *IEEE Transactions on Industry Applications*, 51(4):3368–3375, 2015. doi: 10.1109/TIA.2015.2407055.

[341] Ke Ma, Amir Sajjad Bahman, Szymon Beczkowski, and Frede Blaabjerg. Complete Loss and Thermal Model of Power Semiconductors Including Device Rating Information. *IEEE Transactions on Power Electronics*, 30(5):2556–2569, 2015. doi: 10.1109/TPEL.2014.2352341.

[342] Abraham Marquez Alcaide, Giampaolo Buticchi, Andrii Chub, and Luca Dalessandro. Design and Control for High-Reliability Power Electronics: State-of-the-Art and Future Trends. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, 5(1):50–61, 2024. doi: 10.1109/JESTIE.2023.3287513.

[343] Haoyu Chen, Zhenbin Zhang, Petros Karamanakos, and Jose Rodriguez. Digital Twin Techniques for Power Electronics-Based Energy Conversion Systems: A Survey of

Concepts, Application Scenarios, Future Challenges, and Trends. *IEEE Industrial Electronics Magazine*, 17(2):20–36, 2023. doi: 10.1109/MIE.2022.3216719.

[344] Junchong Fan, Dihao Ma, Jin Wang, Madhu Chinthavali, and R. S. K. Moorthy. Real-time Condition Monitoring of Power Modules in Grid-tied Power Converter. In *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–6, 2022. doi: 10.1109/ECCE50734.2022.9947453.

[345] Georg Lauss and Kai Strunz. Accurate and Stable Hardware-in-the-Loop (HIL) Real-Time Simulation of Integrated Power Electronics and Power Systems. *IEEE Transactions on Power Electronics*, 36(9):10920–10932, 2021. doi: 10.1109/TPEL.2020.3040071.

[346] Alessandro Vaccaro and Paolo Magnone. Influence of Power Cycling Test Methodology on the Applicability of the Linear Damage Accumulation Rule for the Lifetime Estimation in Power Devices. *IEEE Transactions on Power Electronics*, 38(5):6545–6554, 2023. doi: 10.1109/TPEL.2023.3242314.

[347] Ling-Ling Li, Jia-Qi Liu, Ming-Lang Tseng, Xin-Bao Zhang, and Kuo-Jui Wu. Predicting the Power Module Cumulative Damage Degree in New Energy Vehicle: Improved Manson Model. *Journal of Cleaner Production*, 374:133945, 2022. ISSN 0959-6526. doi: https://doi.org/10.1016/j.jclepro.2022.133945. URL https://www.sciencedirect.com/science/article/pii/S095965262203517X.

[348] Frede Blaabjerg, Huai Wang, Ionut Vernica, Bochen Liu, and Pooya Davari. Reliability of Power Electronic Systems for EV/HEV Applications. *Proceedings of the IEEE*, 109 (6):1060–1076, 2021. doi: 10.1109/JPROC.2020.3031041.

[349] Ke Ma, Marco Liserre, Frede Blaabjerg, and Tamas Kerekes. Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power

Converter. *IEEE Transactions on Power Electronics*, 30(2):590–602, 2015. doi: 10.1109/TPEL.2014.2312335.

[350] Bo Wang, Jie Cai, Xiong Du, and Luowei Zhou. Review of Power Semiconductor Device Reliability for Power Converters. *CPSS Transactions on Power Electronics and Applications*, 2(2):101–117, 2017. doi: 10.24295/CPSSTPEA.2017.00011.

[351] Milton A. Miner. Cumulative Damage in Fatigue. *Journal of Applied Mechanics*, 12(3):A159–A164, 03 2021. ISSN 0021-8936. doi: 10.1115/1.4009458. URL https://doi.org/10.1115/1.4009458.

[352] William J. Owen. An Exponential Damage Model for Strength of Fibrous Composite Materials. *IEEE Transactions on Reliability*, 56(3):459–463, 2007. doi: 10.1109/TR.2007.903353.

[353] Zhenghua Chen, Min Wu, Rui Zhao, Feri Guretno, Ruqiang Yan, and Xiaoli Li. Machine Remaining Useful Life Prediction via an Attention-Based Deep Learning Approach. *IEEE Transactions on Industrial Electronics*, 68(3):2521–2531, 2021. doi: 10.1109/TIE.2020.2972443.

[354] Youssof Fassi, Vincent Heiries, Jerome Boutet, and Sebastien Boisseau. Toward Physics-Informed Machine-Learning-Based Predictive Maintenance for Power Converters—A Review. *IEEE Transactions on Power Electronics*, 39(2):2692–2720, 2024. doi: 10.1109/TPEL.2023.3328438.

[355] Lee Gill, Michael Smith, Luke Yates, Gab-Su Seo, and Alan J. Michaels. Evaluation of Converter Performance Considering Static and Dynamic Device Part-to-Part Variability. In *2024 IEEE Design Methodologies Conference (DMC)*, pages 1–7, 2024. doi: 10.1109/DMC62632.2024.10812119.

[356] Haoran Li, Diego Serrano, Thomas Guillod, Shukai Wang, Evan Dogariu, Andrew Nadler, Min Luo, Vineet Bansal, Niraj K. Jha, Yuxin Chen, Charles R. Sullivan, and Minjie Chen. How MagNet: Machine Learning Framework for Modeling Power Magnetic Material Characteristics. *IEEE Transactions on Power Electronics*, 38(12): 15829–15853, 2023. doi: 10.1109/TPEL.2023.3309232.

[357] Wilhelm Kirchgässner, Nikolas Förster, Till Piepenbrock, Oliver Schweins, and Oliver Wallscheid. HARDCORE: H-Field and Power Loss Estimation for Arbitrary Waveforms With Residual, Dilated Convolutional Neural Networks in Ferrite Cores. *IEEE Transactions on Power Electronics*, 40(2):3326–3335, 2025. doi: 10.1109/TPEL.2024.3488174.

[358] Dickson N. T. How, M. A. Hannan, M. S. Hossain Lipu, and Pin Jern Ker. State of Charge Estimation for Lithium-Ion Batteries Using Model-Based and Data-Driven Methods: A Review. *IEEE Access*, 7:136116–136136, 2019. doi: 10.1109/ACCESS.2019.2942213.

[359] M. A. Hannan, D. N. T. How, M. S. Hossain Lipu, Pin Jern Ker, Z. Y. Dong, M. Mansur, and Frede Blaabjerg. SOC Estimation of Li-ion Batteries With Learning Rate-Optimized Deep Fully Convolutional Network. *IEEE Transactions on Power Electronics*, 36(7):7349–7353, 2021. doi: 10.1109/TPEL.2020.3041876.

[360] Zeheng Wang, Liang Li, Ross C. C. Leon, Jinlin Yang, Junjie Shi, Timothy van der Laan, and Muhammad Usman. Improving Semiconductor Device Modeling for Electronic Design Automation by Machine Learning Techniques. *IEEE Transactions on Electron Devices*, 71(1):263–271, 2024. doi: 10.1109/TED.2023.3307051.

[361] Saeed Peyghami, Tomislav Dragicevic, and Frede Blaabjerg. Intelligent Long-Term

Performance Analysis in Power Electronics Systems. *Scientific Reports*, 11(1):7557, 2021. ISSN 2045-2322. doi: 10.1038/s41598-021-87165-3.

[362] Vahid Samavatian, Mahmud Fotuhi-Firuzabad, Majid Samavatian, Payman Dehghanian, and Frede Blaabjerg. Correlation-driven Machine Learning for Accelerated Reliability Assessment of Solder Joints in Electronics. *Scientific Reports*, 10(1):14821, 2020. ISSN 2045-2322. doi: 10.1038/s41598-020-71926-7.

[363] Ivana Kovacevic-Badstuebner, Elena Mengotti, Philipp Natzke, Enea Bianda, Salvatore Race, Matthias Schuepbach, Christoph Kenel, Denis Musella, Joni Jormanainen, and Ulrike Grossner. Comparative Study on Power Cycling Capabilities of SiC Power MOSFET and Si IGBT Baseplate-Less Power Modules. In *2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 518–521, 2024. doi: 10.1109/ISPSD59661.2024.10579629.

[364] Huai Wang, Marco Liserre, Frede Blaabjerg, Peter de Place Rimmen, John B. Jacobsen, Thorkild Kvisgaard, and Jørn Landkildehus. Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(1):97–114, 2014. doi: 10.1109/JESTPE.2013.2290282.

[365] Pratikhya Raut, Deepak Kumar Panda, and Amit Kumar Goyal. A Comprehensive Review on Next-Generation Modeling and Optimization for Semiconductor Devices. *IEEE Access*, 13:123724–123742, 2025. doi: 10.1109/ACCESS.2025.3587721.

[366] Gaige Chen, Xiaoyu Hao, Jun Huang, Hongbo Ma, Xianzhi Wang, and Xianguang Kong. A Remaining Useful Life Prediction Method for Insulated-Gate Bipolar Transistor Based on Deep Fusion of Nonlinear Features From Multisource Data. *IEEE Sensors Journal*, 24(22):37531–37543, 2024. doi: 10.1109/JSEN.2024.3471675.

[367] Jinxiao Wei, Fengrui Liang, Hao Feng, and Li Ran. Condition Monitoring of Discrete Power Devices: A Data-Driven Approach With Stress Quantification and Mold Temperature Sensing. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 12(3):2569–2579, 2024. doi: 10.1109/JESTPE.2024.3387652.

[368] Yuqi Su and Xiaolei Fang. Deep Learning-Based Residual Useful Lifetime Prediction for Assets with Uncertain Failure Modes, 2025. URL https://arxiv.org/abs/2405.06068.

[369] Lu Lu, Pengzhan Jin, Guofei Pang, Zhongqiang Zhang, and George Em Karniadakis. Learning nonlinear operators via DeepONet based on the universal approximation theorem of operators. *Nature Machine Intelligence*, 3(3):218–229, March 2021. ISSN 2522-5839. doi: 10.1038/s42256-021-00302-5. URL http://dx.doi.org/10.1038/s42256-021-00302-5.

[370] Ashok Bindra. JEDEC JC-70 Issues Guidelines for Testing and Evaluating WBG Devices [Happenings]. *IEEE Power Electronics Magazine*, 7(3):14–16, 2020. doi: 10.1109/MPEL.2020.3011094.

[371] Yijun Shi, Wanjun Chen, Xingtao Cui, Maoling Li, Chao Liu, Yun Xia, Jia Li, Fangzhou Wang, Yajie Xin, Qi Zhou, Xiaochuan Deng, Zhaoji Li, and Bo Zhang. Investigation on the Long-Term Reliability of High-Voltage p-GaN HEMT by Repetitively Transient Overcurrent. *IEEE Transactions on Electron Devices*, 65(12):5322–5328, 2018. doi: 10.1109/TED.2018.2873802.

[372] Sandeep R. Bahl, Francisco Baltazar, and Yong Xie. A Generalized Approach to Determine the Switching Lifetime of a GaN FET. In *2020 IEEE International Reliability Physics Symposium (IRPS)*, pages 1–6, 2020. doi: 10.1109/IRPS45951.2020.9129631.