High Frequency GaN Characterization and Design Considerations

Xiucheng Huang

Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Fred C. Lee, Chair
Qiang Li
Dong S. Ha
Jaime De La Ree
Alfred L. Wicks

Sep 6th, 2016
Blacksburg, Virginia

Keywords: Gallium nitride, high frequency, high density, soft-switching, gate drive, PCB integration, EMI

High Frequency GaN Characterization and Design Considerations

Xiucheng Huang

ABSTRACT

The future power conversion system not only must meet the characteristics demanded by the load, but also have to achieve high power density with high efficiency, high ambient temperature, and high reliability. Density and efficiency are two key drivers and metrics for the advancement of power conversion technologies.

Generally speaking, a high performance active device is the first force to push power density to meet the requirement of modern systems. Silicon has been a dominant material in power management since the late 1950s. However, due to continuous device optimizations and improvements in the production process, the material properties of silicon have increasingly become the limiting factor. Workarounds like the super junction stretch the limits but usually at substantial cost.

The use of gallium nitride devices is gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load (POL) converters, off-line switching power supplies, battery chargers and motor drives. GaN devices have a much lower gate charge and lower output capacitance than silicon MOSFETs and, therefore, are capable of operating at a switching frequency 10 times greater. This can significantly impact the power density of power converters, their form factor, and even current design and manufacturing practices. To realize the benefits of GaN devices resulting from significantly higher operating frequencies, a number of issues have to be addressed, such as converter topology, soft-switching technique, high frequency gate driver, high frequency magnetics, packaging, control, and thermal management.

This work studies the insight switching characteristics of high-voltage GaN devices including some specific issues related to the cascode GaN. The package impact on the switching performance and device reliability will be illustrated in details. A stack-die package is proposed for cascode GaN devices to minimize the impact of package parasitic inductance on switching transition. Comparison of hard-switching and soft-switching operation is carried based on device model and experiments, which shows the necessity of soft-switching for GaN devices at high frequency.

This work also addresses high dv/dt and di/dt related gate drive issues associated with the higher switching speed of GaN devices. Particularly, the conventional driving solution could fail on the high side switch in a half-bridge configuration due to relative large common-mode noise current. Two simple and effective driving methods are proposed to improve noise immunity and maintain high driving speed.

Finally, this work illustrates the utilization of GaN in an emerging application, high density AC-DC adapter. Many design considerations are presented in detail. The GaN-based adapter is capable of operating at 1-2 MHz frequency with an improved efficiency up to 94%. Several design examples at different power levels, with a power density in the range of 20~35W/in^3, which is a three-fold improvement over the state-of-the-art product, are successfully demonstrated.

In conclusion, this work is focus on the characterization, and evaluation of GaN devices. Packaging, high frequency driving and soft-switching technique are addressed to fully explore the potential of GaN devices. High density adapters are demonstrated to show the advance of GaN device and its impact on system design.

High Frequency GaN Characterization and Design Considerations

Xiucheng Huang

GENERAL AUDIENCE ABSTRACT

This work is focus on the characterization, evaluation and application of new wide-band-gap semiconductor devices – GaN devices. Due to superior physics property compared to existing semiconductor material, GaN device is able to switch at much higher frequency and this brings significant impact on the field of power electronics. The potential impact of GaN goes beyond the simple measures of efficiency and power density. It is feasible to design a system with a more integrated approach at higher frequency, and therefore, it is easier for automated manufacturing. This will bring significant cost reductions in power electronics equipment and unearth numerous new applications which have been previously precluded due to high cost.

To realize the benefits of GaN devices resulting from significantly higher operating frequencies, a number of issues have to be addressed, such as device packaging, power converter topology, thermal management, high frequency magnetics and system control. This dissertation discusses the most critical issues related to GaN devices with proper solutions. A practical design example of AC-DC adapter is demonstrated with much improved efficiency, density and manufacturability.

To My Family:

My parents: Hongkun Huang and Baozhen Weng

My Parents in law: Yongjie Du and Yimin Tian

My wife: Weijing Du

My daughter: Bella Huang

Acknowledgments

With sincere appreciation in my heart, I would like to thank my advisor, Dr. Fred Lee, for his guidance, encouragement, and support during the past five years. It is him who shows me the strength and right way to do research and pursue the beauty of power electronics. His rigorous research attitude and logical way of thinking have been a great value for me. I believe everything I've learned from Dr. Lee will benefit my future career.

I would also like to thank Dr. Qiang Li for his valuable guidance during my research. I still remember the weekly individual meeting with him when I just join CPES and it was so important to help me build the initial skill set and explore the right research area. He is more than a professor to me, but a model that I want to follow in the past and the future.

Moreover, with sincere gratitude, I would thank Dr. Fred Lee, Ms. Lee, Dr. Qiang Li and Ms. Luman Chen for their selfless help when my wife is in the period of confinement. They help us to get through the difficulty and this precious memory will bear in mind forever.

It is an honor for me to have Professor Dong S. Ha, Professor Jaime De La Ree and Professor Alfred L. Wicks as my committee members. I am truly thankful to them for all comments from different technical perspective which would broad my knowledge significantly.

It is fortunate to study GaN devices, which are considered to have significant impact on power electronics, since I came to CPES. It is even more fortunate to have my colleague and friend, Zhengyang Liu. We work together from day one and explore the unknown knowledge about GaN devices. We have faced tons of difficulties when we conducted

research without much of reference, but we never gave up. “No pain, no gain”, and I understood these words deeply in my heart. I am also especially indebted to my colleagues in the GaN Group. We have many valuable discussions during day and night. Many of the ideas in this work are inspired by casual talk. I would like to thank all the members of our teams: Dr.Wenli Zhang, Dr. David Reusch, Dr. Mingkai Mu, Mr. Alex Ji, Mr. Yucheng, Mr. Chao Fei, Mr. Bin Li, Mr. Shishuo Zhao, Mr. Junjie Feng, Mr. Zhengrong Huang, Mr. Tao Liu.

I would also like to thank colleagues in the power management consortium (PMC) of CPES. It has been a great pleasure to work with the talented, creative, helpful and dedicated colleagues. Dr. Yingyi Yan, Dr. Weiyi Feng, Dr. Yipeng Su, Dr. Shuilin Tian, Dr. Pei-Hsin Liu, Dr.Dongbin Hou, Mr. Wei Zhang, Mr. Li Jiang, Mr. Syed Bari, Mr. Xuebin Chen Mr. Zhongsheng Cao, Mr. Xuebing Chen, Ms. Virginia Li, Mr. Mohamed Ahmed.

My thanks also go to all of the other students I have met in CPES. It is precious memory to live and work with them in the past five years. Many visiting scholars have brought their expertise and valuable discussion during my research. Dr. Li Wang, Dr Xin Ming, Dr. Yan-Cun Li, Dr. Kenichiro Tanaka, Dr.Shuojie She, Mr. Chaofeng Cai. Thank you for the help and friendship.

I would also like to thank all the wonderful staffs in CPES: Ms. Linda Gallagher, Ms. Teresa Shaw, Ms. Teresa Rose, Ms. Marianne Hawthorne, Ms. Linda Long, Mr. Doug Sterk and Mr. David Gilham for their support and help over the past six years.

With much love and gratitude, I want to thank my parents: Hongkun Huang and Baozhen Weng; my parents in law: Yongjie Du, Yimin Tian; who have always been there with their love and support.

Finally but not the least, I would like to thank my wife Weijing Du and my daughter Bella Huang. You are always the special one and mean a lot to me. I want to be with you all my life.

The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006521 with North Carolina State University, PowerAmerica Institute. This work was also supported in part by PMC at CPES: Chicony Power, CSR Zhuzhou Institute Co., Ltd., Delta Electronics, Huawei Technologies, Infineon Technologies, Inventronics Inc, Linear Technology, Murata Manufacturing Co., Ltd., NEC TOKIN Corporation, NXP Semiconductors, ON Semiconductor, Panasonic Corporation, Richtek Technology, Sonos, Texas Instruments.

This work was conducted with the use of GaN device samples by EPC, Navitas, Panasonic, and Transphorm of the CPES Industry Consortium Program.

Disclaimer

The information, data, or work presented herein was funded in part by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United

States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Table of Contents

Chapter 1. Introduction 1

1.1 Background and Motivation...1

1.2 Overview of GaN Power Devices..3

1.2.1 Why GaN...3

1.2.2 Enhancement Mode and Depletion Mode GaN Devices.............................6

1.2.3 Steady-state Characteristics of 600V GaN Devices 9

1.2.4 Reverse Conduction of GaN Devices...10

1.3 Challenges of GaN devices 11

1.3.1 Switching Characteristics 12

1.3.2 Package Impact on Switching Behavior and Gate Reliability 13

1.3.3 High dv/dt and di/dt...13

1.4 Impact of GaN Devices on System Level Design.....................................14

1.4.1 High Frequency Magnetics 14

1.4.2 High Frequency EMI..15

1.4.3 High Frequency control..15

1.5 GaN Based Applications...16

1.6 Dissertation Outline 16

Chapter 2. Switching Characterization of GaN Devices....................... 18

2.1 Switching Loss Mechanism Analysis of GaN Devices 18

2.1.1 GaN device loss model 18

2.1.2 Turn-on transition 25

2.1.3 Turn-off transition 28

2.2 Packaging Impact on Switching Loss 32

2.3 Special Issues in Cascode GaN Devices 38

2.3.1 Si MOSFET Avalanche 39

2.3.2 GaN Internal Switching Loss 41

2.3.3 Failure I: Internal GaN Gate Ringing 45

2.3.4 Failure II: Divergent Oscillation at High Current Turn-off Condition 46

2.3.5 Proposed Solution: Better Package and Charge Balance 50

2.4 Conclusion 65

Chapter 3. Design Considerations for GaN Devices 66

3.1 Soft-switching or hard-switching 66

3.2 High Frequency Gate Drive 74

3.2.1 The di/dt Issue and Solutions 76

3.2.2 The dv/dt Issue (Common mode Noise Current) and Solutions 78

3.4 Conclusion 86

Chapter 4. System Design of GaN Based AC-DC Adapters 87

4.1 State-of-the-art Practice 87

4.2 MHz Active Clamp Flyback Converter for Adapters Po < 75W 91

4.2.1 Soft-switching with Active Clamping Circuit 91

4.2.2 MHz Flyback Transformer 96

4.2.3 MHz Flyback Converter EMI Characterization and Filter Design 107

4.2.4 High Frequency Control of Active Clamp Flyback Converter 119

4.2.5 Experiments Results and Discussion...127

4.3 Universal adapter design for a wide power range 132

4.3.1 System Structure of Proposed Universal Adapter 133

4.3.2 First Stage: Totem-pole Bridgeless Rectifier with Harmonic Injection 134

4.3.3 Second Stage: LLC-DCX 143

4.3.4 Experiment Results and Discussion 147

4.4 Conclusion 155

Chapter 5. Conclusion and Future Work 157

5.1 Conclusion 157

5.2 Future Work 159

Appendix A. GaN Analytical Loss Model 160

Appendix B. GaN Converter with Inverse Coupled Inductor 193

References 219

List of Figures

Figure 1.1 Roadmap of Intel microprocessors....................1

Figure 1.2 Specific on-resistance vs breakdown voltage for Si, SiC, GaN....................5

Figure 1.3 Basic structure of GaN device....................7

Figure 1.4 Basic structure of d-mode GaN device, (a) on state, (b) off state....................7

Figure 1.5 Cascode GaN: a d-mode GaN in series with a low voltage Si MOSFET....................8

Figure 1.6 Basic structure of enhancement mode GaN device, (a) on state, (b) off state....................8

Figure 1.7 Reverse conduction of e-mode GaN devices: (a) e-mode GaN, (b) cascode GaN.......10

Figure 1.8 Hard-switching turn-on transient of GaN device....................12

Figure 2.1 Packaging parasitics of a cascode GaN device....................19

Figure 2.2 Comparison of switching waveforms w/ original model and modified model....................20

Figure 2.3 Equivalent circuit during the first stage of turn on transition....................21

Figure 2.4 Model validation with double-pulse-test circuit: (a) diagram, (b) prototype....................24

Figure 2.5 Turn on/off waveforms comparisons (Blue line: experiment, red line: analytical model) (a) Turn on @10A, (b) Turn off@10A....................24

Figure 2.6 Efficiency comparison between experimental and calculation results based on proposed model....................25

Figure 2.7 Hard-switching turn-on waveforms....................26

Figure 2.8 Turn-on switching loss of different GaN devices....................28

Figure 2.9 Hard-switching turn-off waveforms....................29

Figure 2.10 Turn-off mechanism of different types of GaN devices: (a) e-mode, (b) cascode......30

Figure 2.11 Turn-off switching loss of different GaN devices....................31

Figure 2.12 Comparison of turn-off switching loss: GaN vs. Si....................32

Figure 2.13 Package and related inductance of 600V e-mode GaN devices: (a) Packages for 600V e-mode GaN, (b) Package related inductance....................33

Figure 2.14 Turn-on transition of different packages....................34

Figure 2.15 Turn-off transition of different packages 34

Figure 2.16 Switching energy of different package 35

Figure 2.17 Two different packages for cascode GaN devices: (a) To 220 Package, (b) Stack die package 36

Figure 2.18 Two packages related parasitic inductance: (a) TO220 package, (b) Stack-die package 37

Figure 2.19 Turn-on waveform comparison between (a) TO-220 package, and (b) Stack-die package 37

Figure 2.20 Switching energy comparison of different packages 38

Figure 2.21 Boost converter with cascode GaN device 38

Figure 2.22 Two possible turn-off transition of cascode GaN devices 39

Figure 2.23 Si MOSFET reaches avalanche during turn-off transition 40

Figure 2.24 Two possible ZVS turn-on transition of cascode GaN devices 42

Figure 2.25 GaN internal switching loss during ZVS turn-on transition 42

Figure 2.26 The relationship of internal turn-on switching loss and mismatch charge 44

Figure 2.27 GaN gate breakdown due to parasitic ringing during turn-off transition: (a) di/dt loop during turn-off transition, (b) Key waveforms during turn-off transition 45

Figure 2.28 Illustration of divergent oscillation 47

Figure 2.29 Equivalent circuits during oscillation period 48

Figure 2.30 GaN gate voltage spike elimination with stack-die package 51

Figure 2.31 Adding an extra capacitor in cascode GaN devices 52

Figure 2.32 Impact of an extra capacitor on turn-off switching loss 53

Figure 2.33 Chip-on-chip package for cascode GaN device with an extra capacitor 54

Figure 2.34 Experimental waveforms without external capacitor 55

Figure 2.35 Experimental waveform with external capacitor 56

Figure 2.36 Two possible packaging approach with C_X 58

Figure 2.37 Equivalent circuit of two different packaging approaches 59

Figure 2.38 Current distribution in different packages...60

Figure 2.39 Prototypes of two different packaging approaches 61

Figure 2.40 Experimental results with different packaging approaches (a) Packag-ing A and B without C_X (b) Packaging A with C_X (c) Packaging B with C_X 63

Figure 2.41 Experiment with packaging B, without shunt resistance 63

Figure 2.42 Half bridge module of cascode GaN devices with packaging B approach 64

Figure 2.43 Experiment with half bridge module of cascode GaN devices with packaging B approach 64

Figure 3.1 Hard-switching turn-on transient of GaN device with severe parasitic ringing............67

Figure 3.2 Hard-switching turn-on transient of GaN device with less parasitic ringing by slowing down switching speed 67

Figure 3.3 Hard-switching turn-on energy vs. R_g...68

Figure 3.4 CRM operation principle 69

Figure 3.5 Hard-switching vs. CRM soft-switching..70

Figure 3.6 Loss breakdown at 6A...70

Figure 3.7 4-phase bidirectional buck/boost converter for energy storage system 71

Figure 3.8 Comparison of GaN-based prototype and Si IGBT-based prototype...........................72

Figure 3.9 5 MHz converter with the cascode GaN switch 73

Figure 3.10 Loss breakdown of 5 MHz CRM boost converter with cascode GaN device............74

Figure 3.11 Turn-off transition with different gate resistance...75

Figure 3.12 Turn-off energy with different gate resistance 75

Figure 3.13 High dv/dt and di/dt induced by GaN devices: (a) Si MOSFET, (b) GaN switch 76

Figure 3.14 di/dt impact on gate drive loop..77

Figure 3.15 High di/dt induces voltage on the gate 77

Figure 3.16 Smaller voltage spike with less CSI 78

Figure 3.17 High dv/dt causes common-mode current across parasitic capacitance of level shifter or isola-tor (cascode GaN is used as an example) 79

Figure 3.18 High dv/dt deteriorates the PWM signal 79

Figure 3.19 Proposed high side gate drive circuit 81

Figure 3.20 PCB layout impact on dv/dt immunity for high side driver 82

Figure 3.21 Experimental waveform of improved dv/dt immunity for high side driver 82

Figure 3.22 Conventional driving transformer is susceptible to noise due to large parasitic capacitance 83

Figure 3.23 Novel driving transformer with shielding 84

Figure 3.24 Proposed driving transformer with shielding 85

Figure 3.25 Comparison of driving transformer: (a) w/o shielding, (b) w/ shielding 85

Figure 4.1 Applications of AC-DC adapter 88

Figure 4.2 Adapter market information Figure 4.2 [D.1] 88

Figure 4.3 State-of-the-art AC-DC adapters 89

Figure 4.4 Inside the Apple adapter 90

Figure 4.5 Theoretical limit of power density vs. efficiency (max 95℃ with plastic case) 91

Figure 4.6 Conventional flyback vs. Active clamp flyback 92

Figure 4.7 Key waveforms of two flyback topology operating at 1MHz 93

Figure 4.8 Comparison of ideal transformer winding current 94

Figure 4.9 Time-domain winding loss of two flyback topologies (red solid line: conventional flyback; blue dash line: active clamp flyback) 94

Figure 4.10 Impact of clamping capacitor on primary and secondary current waveforms 96

Figure 4.11 Impact of clamping capacitor on converter loss 96

Figure 4.12 Comparison of core loss density of different core material 98

Figure 4.13 ER core shape for MHz design 99

Figure 4.14 Core loss density vs. N_S 100

Figure 4.15 Cross section view of the transformer winding (red line represents primary winding, blue line represents secondary winding) 100

Figure 4.16 Relationship of winding loss and distance between winding and air gap 101

Figure 4.17 Impact of turns ratio on converter current....102

Figure 4.18 Related loss vs. transformer parameters....103

Figure 4.19 Flyback transformer winding structure with shielding 105

Figure 4.20 Flyback transformer with shielding 105

Figure 4.21 3D FEA simulation of flyback transformer with and without shielding layer....106

Figure 4.22 Integrated shielding layer as the primary winding....107

Figure 4.23 EMI noise propagation path of active clamp flyback converter 109

Figure 4.24 DM noise of switching frequency using zero-span mode in spectrum analyzer....110

Figure 4.25 Diode bridge voltage waveforms in line cycle....111

Figure 4.26 Diode bridge voltage waveform at t_1 instant....111

Figure 4.27 Diode junction capacitance characteristics 112

Figure 4.28 CM noise current in L line and N line....112

Figure 4.29 CM noise propagation path with shielding 113

Figure 4.30 Detailed diode-bridge voltage waveform and CM noise current in L line and N line right after diode bridge is off....114

Figure 4.31 EMI noise measurement....115

Figure 4.32 DM noise of switching frequency using zero-span mode in spectrum analyzer....116

Figure 4.33 EMI filter for conventional adapter application....117

Figure 4.34 One-stage EMI filter for MHz flyback converter....118

Figure 4.35 Choke material comparison 119

Figure 4.36 Picture of CM/DM choke for MHz flyback converter....119

Figure 4.37 Control of MHz active clamp flyback converter for adapter application....121

Figure 4.38 Trajectory analysis of resonance in active clamp flyback converter........................122
Figure 4.39 Conventional ZVS detection using auxiliary winding voltage 124
Figure 4.40 Proposed ZVS detection method..125
Figure 4.41 Proposed DCM clamp method [D.25] 126
Figure 4.42 Three prototypes employs MHz active clamp flyback topology 127
Figure 4.43 Experimental waveforms of different ZVS detection method 128
Figure 4.44 65W prototype experiment waveforms 129
Figure 4.45 Experimental waveforms of proposed DCM clamp method...................................130
Figure 4.46 Prototype EMI noise measurement with and without filter 131
Figure 4.47 Efficiency comparison of the prototype and state-of-the-art products....................132
Figure 4.48 Universal two-stage structure for adapters using a wide power range.....................134
Figure 4.49 Impact of harmonic injection on input power for below 75W adapters..................136
Figure 4.50 Relationship of bus cap reduction with harmonic injection 137
Figure 4.51 Relationship of first stage efficiency with harmonic injection 138
Figure 4.52 Impact of harmonic injection on input power for adapters above 75W 139
Figure 4.53 Bus capacitance reduction with harmonics injection 140
Figure 4.54 Impact of harmonic injection on switching frequency..141
Figure 4.55 Impact of harmonic injection on EMI noise spectrum..143
Figure 4.57 Key waveforms of LLC converter operating at Fs=Fo 144
Figure 4.58 PCB winding based LLC-DCX transformer integrated SR and caps 145
Figure 4.59 Transformer loss vs. core radius r and window width c..146
Figure 4.60 Transformer and footprint tradeoff 147
Figure 4.61 Two-stage prototypes..148
Figure 4.62 Key waveforms of totem-pole rectifier 150
Figure 4.63 Cap reduction/voltage ripple reduction with harmonic injection in 65W prototype.151

Figure 4.64 Cap reduction/voltage ripple reduction with harmonic injection in 150W prototype....152
Figure 4.65 One-stage filter for proposed 150W 2-stage adapter 152
Figure 4.66 EMI measurement results of 150W prototype 153
Figure 4.67 Measured efficiency of proposed 2-stage adapters 154
Figure 4.68 Achievement of higher density and higher efficiency adapter....155

Appendix A

Figure.A 1 Piecewise linear approximation of the conventional loss model 160
Figure.A 2 Package of a cascode GaN 163
Figure.A 3 Equivalent cascode GaN transistor including parasitic inductors and capacitors 165
Figure.A 4 Simplified equivalent circuit to analyze switching loss of cascode GaN transistor...166
Figure.A 5 Equivalent circuit during turn on Stage I 167
Figure.A 6 Equivalent circuit during turn on Stage II....168
Figure.A 7 Further simplified equivalent circuit during turn on Stage II....169
Figure.A 8 Equivalent circuit during turn on Stage III....171
Figure.A 9 Equivalent circuit during turn on Stage V....174
Figure.A 10 Equivalent circuit during turn on Stage VI 176
Figure.A 11 Equivalent circuit during turn off Stage I....177
Figure.A 12 Equivalent circuit during turn off Stage II 179
Figure.A 13 Equivalent circuit during turn off Stage III....181
Figure.A 14 Equivalent circuit during turn off Stage IV....183
Figure.A 15 Further simplified equivalent circuit during turn off Stage IV 183
Figure.A 16 Model validation with double-pulse-test circuit: (a) diagram, (b) prototype 186
Figure.A 17 Turn on/off waveforms comparisons (Blue line: experiment, red line: analytical model) (a) Turn on @10A, (b) Turn off@10A....187

Figure.A 18 Efficiency comparison between experimental and calculation results based on proposed model 189

Figure.A 19 Efficiency comparison between experimental results and calculation results based on proposed model 190

Figure.A 20 Buck converter loss breakdown based on proposed loss model 191

Appendix B

Figure B. 1 Bidirectional buck/boost converter....195

Figure B. 2 Key waveforms of CRM operation for buck/boost converter 195

Figure B. 3 Relationship between T_r and T_s in CRM 197

Figure B. 4 Inductor current rms value increases with frequency in CRM 197

Figure B. 5 CRM operation experimental waveforms at 5MHz 197

Figure B. 6 Interleaved buck/boost converter with inverse coupled inductor 198

Figure B. 7 Key waveforms of CRM with coupled inductor considering resonant period 200

Figure B. 8 Equivalent inductance derivation via equivalent circuit @D<0.5 (a) Initial circuit during resonant period (b) Decoupled inductor (c) Circuit derivation with Norton's Theorem (d) Circuit derivation with Thevenin's Theorem 202

Figure B. 9 Equivalent inductance derivation via equivalent circuit @D>0.5 (a) Initial circuit during resonant period (b) Decoupled inductor (c) Circuit derivation with Norton's Theorem (d) Circuit derivation with Thevenin's Theorem 204

Figure B. 10 Reduction of resonant inductance with different coupling coefficient and voltage gain 207

Figure B. 11 Reduction of resonant period with different coupling coefficient and voltage gain207

Figure B. 12 Reduction of inductor current rms value with coupled inductor 208

Figure B. 13 Coupled inductor modifies CRM operation 209

Figure B. 14 Comparison of coupled and non-coupled inductor....212

Figure B. 15 Experimental waveforms of CRM operation with non-coupled inductor 214

Figure B. 16 Experimental waveforms of CRM operation with coupled inductor 216

Figure B. 17 Loss breakdown of two-phase buck direction at full load.......................................217

Figure B. 18 Efficiency comparison over wide load range of buck direction.............................217

List of Tables

Table 1.1 Material properties of GaN, SiC, and Si 4

Table 1.2 Device parameter comparison 9

Table 2.1 Parasitic inductance of package and PCB layout 23

Table 2.2 Package-related parasitic inductance values 33

Table 2.3 Parasitic inductance of different packaging 59

Table 3.1 Commercial high side gate driver 80

Table 4.1 High frequency Core Material Comparison 97

Table 4.2 Parameters of the one-stage EMI filter 118

Table 4.3 Parameters of the EMI filter for 150W prototype 152

Appendix B

Table B. 1 Coupled inductor equivalent inductance[15] 200

Table B. 2 Comparison between non-coupled inductor and inverse coupled inductor 205

Chapter 1. Introduction

This chapter presents the motivations, objectives and overview of this dissertation. The advantages and challenge of gallium nitride (GaN) devices are described and the potential applications are investigated. A review in this field is provided, followed by the dissertation outline and the scope of research.

1.1 Background and Motivation

IT industry is growing rapidly in the last three decades. The microprocessors, which is also known as the central processing unit or CPU, are the key component in most of the applications such as computer systems and portable devices. To achieve better performance, more transistors are being integrated into the microprocessor.

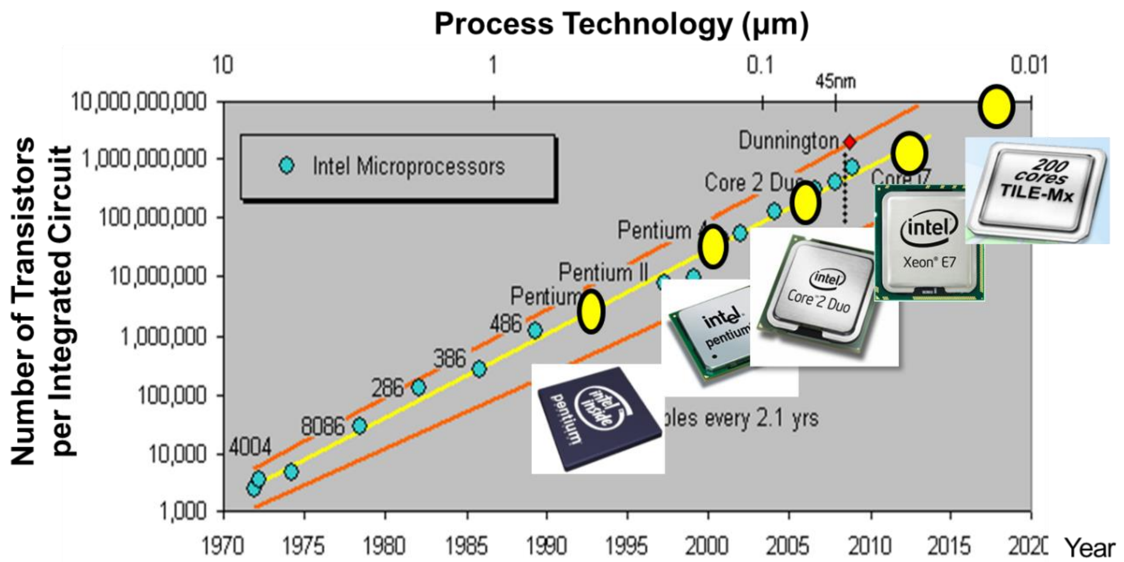


Figure 1.1 Roadmap of Intel microprocessors

Figure 1.1 shows the CPU integrated transistor counts against the dates of introduction. The yellow line is the exponential growth with transistor counts doubling every two years, which is known as the Moore's law. Since the introduction of the high performance Pentium series CPU in the middle of 90s, Intel is still able to follow Moore's law up to date. It is even exciting that Tilera corp., another CPU manufacturer, announced that they are developing 200 cores processor in one chip. The advance of the processor has significant impact on the electronics equipment. It is noticeable that the progress of all forms of mobile devices are progressing at an amazing rate with ever increasing performances and shrinking in size and weight, while their power supply counterparts are bulky with meager power density. For example, the latest MacBook Air laptop is more than 10 times faster than the first generation and its weight reduces to 2.4lb now, while the accompanying 45W adapter remains the same form factor and it weighs 0.4lb. Moreover, the manufacturing and the assembly process for adapter remains labor-intensive.

High performance active semiconductor devices have always been the first force to improve efficiency and power density of modern power conversion system. Since its introduction in the mid-1970s, the silicon (Si) MOSFET, with its greater switching behavior, has replaced the bipolar transistor. To date, the Si MOSFET has been optimized up to its theoretical limit, even beyond the limit, e.g. super junction devices and IGBTs [A.1], [A.2]. The device optimization innovations may continue for quite some time and certainly will be able to leverage the low cost structure of the power MOSFET and know-how of a well-educated base of designers who have learned to squeeze every ounce of performance out of their power conversion circuits and systems [A.3].

The Si MOSFET devices switching loss (majorly turn-on loss) can be further reduced

with soft-switching technique. However, the gate drive loss, turn-off switching loss and circulating conduction loss for soft-switching are still excessive, which limit the switching frequency to few hundreds of kilohertz (kHz) in most applications.

The GaN power devices first appeared in about 2004 and are designed for radio frequency (RF) amplifier [A.4]. Even though GaN devices are still in the early stage, the figure of merit (FOM) improves significantly with 10 years development, and they are far better than the state-of-the-art Si MOSFETs. GaN devices are capable to operate at a switching frequency 10 times higher than Si MOSFET, and therefore, this can significantly impact the power density of power converters, their form factor, and even current design and manufacturing practices.

To realize the benefits of GaN devices resulting from significantly higher operating frequencies, a number of issues have to be addressed, such as converter topology, soft-switching technique, gate driver, high frequency magnetics, packaging, control, and thermal management. Some of the key issues are recognized by the author and are addressed in this work.

1.2 Overview of GaN Power Devices

1.2.1 Why GaN

The advance of GaN devices stems from the basic physical properties of GaN material compared with other semiconductor material, such as Si and SiC. Table 1.1 identifies the key electrical properties of the three materials which have been considered as the success candidate in power electronics field [A.3], [A.5]. It is worthwhile to point out that 4H-SiC is dominant polytype among all SiC polytypes due to identical mobilities in the two planes

of the semiconductor [A.6].

Table 1.1 Material properties of GaN, SiC, and Si

Properties	**GaN**	**4H-SiC**	**Si**
Bandgap, E_g (eV)	3.39	3.26	1.12
Breakdown field, E_{crit} (MV/cm)	3.3	2.2	0.23
Saturated drift velocity, Vs (10^7cm/s)	2.5	2.0	1.0
Electron mobility, μ_n (cm^2/Vs)	2000*	650	1500
Thermal conductivity, λ (W/cm·K)	1.3	1.5	3.8

GaN and SiC have much higher bandgap energy which means capability of higher temperature operation. GaN has highest electrical breakdown field which results in power devices with higher breakdown voltage. Consequently, the die of power devices could be smaller with given breakdown voltage. The drift velocity of GaN is more than twice the drift velocity of Si, therefore, it is expected that GaN devices could be switched at higher frequencies than their Si counterparts.

More vivid way of translating these basic crystal parameters into a comparison of device performance is to calculate the best theoretical performance that could be achieved in each of these candidates. The theoretical on-resistance of each candidate can be calculated as [A.5]

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_s \mu_n E_{crit}^3} \tag{1.1}$$

where V_{BR} is desired breakdown voltage, ε_s is the dielectric constant, E_{crit} is the electric breakdown field and μ_n is the electron mobility. This equation can be plotted as shown in Figure 1.2. The theoretical limit of GaN is at least three order of magnitude lower than that of Si.

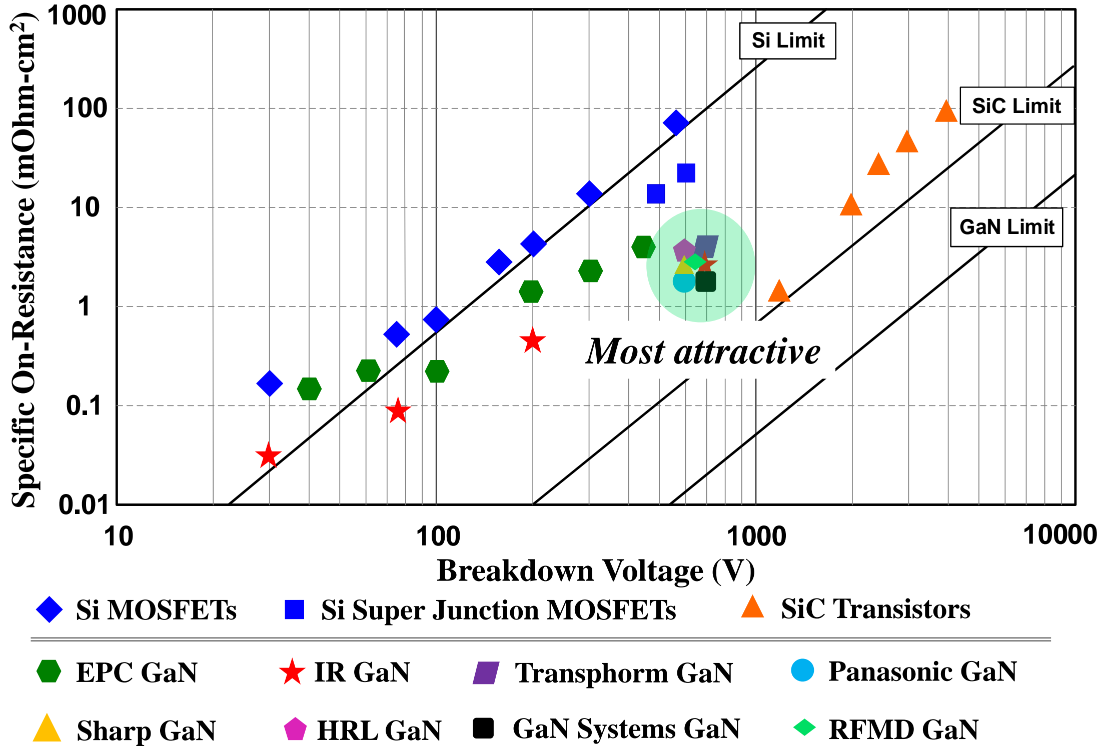


Figure 1.2 Specific on-resistance vs breakdown voltage for Si, SiC, GaN

Due to continuous device optimization and improvement in the production process, the Si devices are very close to the theoretical limit. Workarounds like the super junction stretch the limits but usually at substantial cost. SiC devices are booming since late 1990s and they are majorly targeting at high-voltage and high-temperature applications due to high critical field and thermal conductivity [A.7], [A.8]. The commercial SiC device are typically rated higher than 1.2 kV with maximum 200℃ junction temperature. Another

concern about SiC devices is the cost which prevents wide adoption of SiC in IT industry and consumer electronics.

The first generation of GaN HEMTs, which target at the field of power electronics, have proved that the GaN HEMT has a superior relationship between the on resistance and breakdown voltage than the Si MOSFET due to a higher electrical field strength and enhanced mobility of electrons in the two dimensional electron gas (2DEG) [A.9]. This translates into a GaN HEMT with a smaller die size for a given R_{ds_on} and breakdown voltage which directly increases power density. Among all the voltage rating GaN devices, 600V parts are deemed to be most attractive to device manufacturers, which reflects a huge market of AC-DC and DC-DC power supplies for a wide range applications. The research in this work is also focus on 600V GaN devices and the applications for high efficiency and high density power conversion.

1.2.2 Enhancement Mode and Depletion Mode GaN Devices

Figure 1.3 shows the typical GaN device structure including the 2DEG at the junction of the AlGaN-GaN boundary in which the electrons have extremely high mobility that produces the low on resistance [A.3]. According to different gate structure, GaN devices can be divided into two categories, depletion-mode (d-mode) and enhancement-mode (e-mode) GaN device.

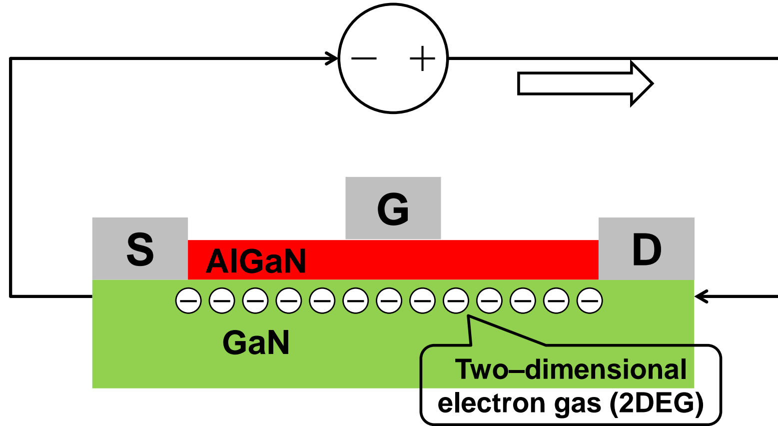
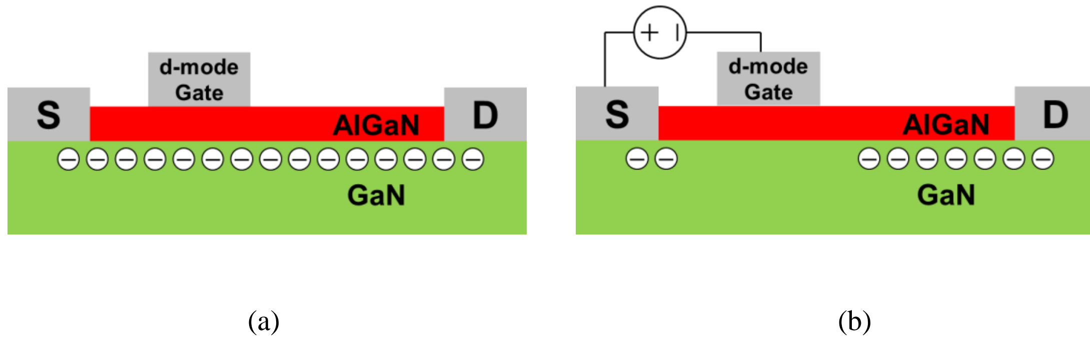


Figure 1.3 Basic structure of GaN device

The d-mode GaN is more nature based on the GaN device crystal structure [A.5]. The device is normally on without applied gate voltage, as shown in Figure 1.4 (a). A negative voltage is necessary to turn off the d-mode GaN device, which makes it inconvenient for circuit design especially at the power converter startup period. To solve this issue, a low voltage Si MOSFET is used in series to drive the GaN device which is well known as cascode structure, and is shown in Figure 1.5 [A.10].



(a) (b)

Figure 1.4 Basic structure of d-mode GaN device, (a) on state, (b) off state

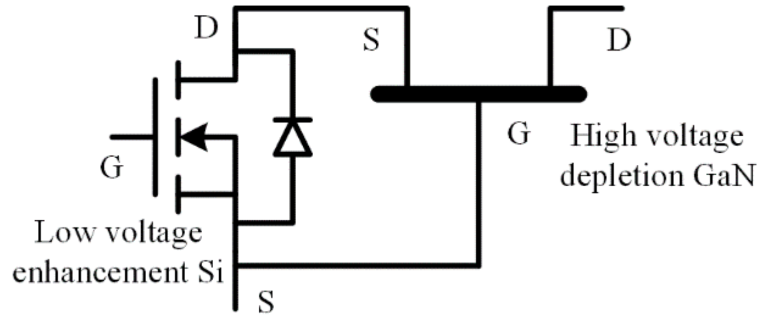
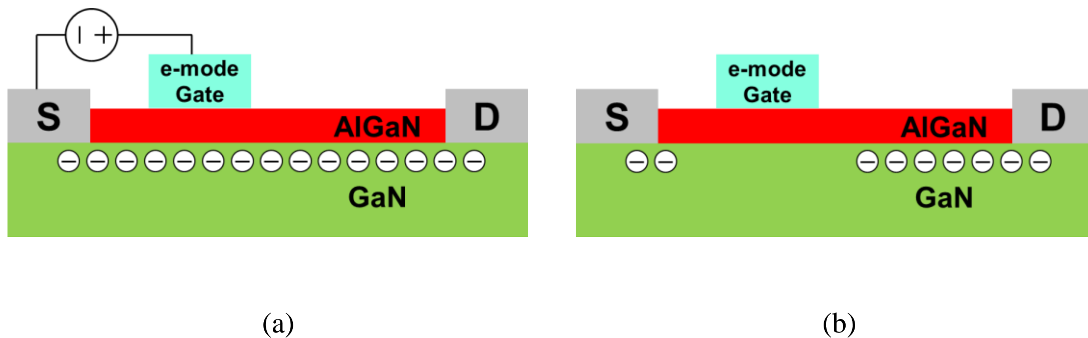


Figure 1.5 Cascode GaN: a d-mode GaN in series with a low voltage Si MOSFET

On the other hand, several techniques have been developed to provide a built-in modification of the 2DEG at the gate electrode. There are three popular gate structures that have been used to create e-mode GaN device: recessed gate [A.11], implanted gate [A.12], and pGaN gate [A.13][A.14]. Different from the d-mode GaN device, the e-mode GaN device is in off state if no external V_{gs} applied, while it is turned on with a positive V_{gs}, as shown in Figure 1.6. One of the desirable common features for e-mode GaN devices is gate overdrive protection. The driving safety margin of commercial available e-mode GaN is quite small, which requires a dedicated gate drive design [A.15], [A.16], [A.17].



(a) (b)

Figure 1.6 Basic structure of enhancement mode GaN device, (a) on state, (b) off state

1.2.3 Steady-state Characteristics of 600V GaN Devices

Table 1.2 lists commercial available GaN devices and a state-of-the-art Si MOSFET with similar on resistance. The devices parameters clearly show that GaN devices have much smaller Q_g (4~10 times reduction) and C_{oss} (2~6 times reduction), which indicates higher frequency operation capability. It is interesting to notice that commercial available e-mode GaN device has better parameters than d-mode GaN in cascode configuration. To the best of the author's knowledge, it is possibly caused by different manufactory process.

As listed in table 1.2, e-mode GaN has lower threshold voltage compared to cascode GaN which actually is a Si MOSFET gate. The required gate drive voltage of e-mode GaN to fully turn on the device is very close to the maximum allowed gate voltage, while cascode GaN has a larger driving safety margin due to Si MOSFET gate.

Table 1.2 Device parameter comparison

	E-Mode GaN		Cascode GaN		Si MOSFET
	Panasonic	GaN Systems	Infineon / IR	Transphorm	Infineon
	PGA26E19	GS66504P	XIRGAN60S002	TPH3206	IPX60R165CP
R_{ds_on} (mΩ)	154	110	135	150	150
C_{oss_tr} (pF)	34	72	84	105	220
Q_g (nC)	4	3.3	8.8	6.2	39
V_{GS_max} (V)	-10~4.5	±10	±20	±18	±20
V_{TH} (V)	1.2	1.6	5	2.1	3
Required V_{GS} (V)	3	7	10	8	10
I_{DSS} (μA)	35	200	115	8	10

Another critical parameter is leakage current (I_{DSS}), which is a significant source of power loss at light load or standby condition. The GaN device from Transphorm has a smaller leakage current even compared with Si MOSFET. The GaN devices from other manufacturers have larger leakage current. The data is a sign of the relative immaturity of GaN technology. It is believed that GaN devices will mature to the point where the leakage current is well controlled.

1.2.4 Reverse Conduction of GaN Devices

GaN devices have the bi-directional current flow capability in nature due to physical structure. While the reverse conduction principle of e-mode and cascode GaN devices are different.

E-mode GaN can conduct in the reverse direction when the drain voltage is lower than the gate by at least V_{TH}, as shown in Figure 1.7 (a). The voltage drop V_{SD} is determined by the reverse current I_{SD}, transconduction g_m, threshold voltage V_{TH}, and applied gate-source voltage V_{GS}, as given by (1.2). It is obvious that V_{SD} increase with I_{SD} and the first term is considerable even at low current due to the non-linearity of g_m. It should be pointed out that V_{SD} increases significantly if $V_{GS(off)}$ has initial negative bias in off state.

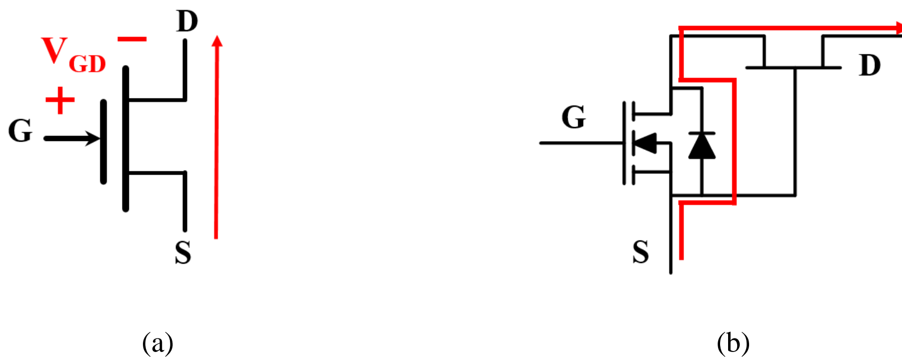


Figure 1.7 Reverse conduction of e-mode GaN devices: (a) e-mode GaN, (b) cascode GaN

$$V_{SD} = \frac{I_{SD}}{g_m} + V_{TH} - V_{GS(off)} \tag{1.2}$$

The cascode GaN has a different mechanism of reverse conduction. The body diode of Si MOSFET is conducting the reverse current and the GaN gate-source voltage is clamped by the diode forward voltage drop. The d-mode GaN is fully turned on and the GaN on resistance is added to the total voltage drop of reverse conduction, which is given in (1.3).

$$V_{SD} = V_{bd_Si} + I_{SD} \cdot R_{DS_GaN} \tag{1.3}$$

The voltage drop of cascode GaN is slightly lower than e-mode GaN due to different mechanism. However, they are both higher than Si MOSFET and they may lead a higher conduction loss in certain power conversion circuits. This issue can be partially solved by optimizing dead-time [A.18], [A.19].

1.3 Challenges of GaN devices

The GaN devices parameters are so superb and it may lead an illusion to circuit designer that the circuit performance can be significantly improved by simply plugging and replacing Si MOSFET. However, researchers found out that the circuit performance may be worse or even not work with GaN devices without deeply understanding the technical challenges raised by GaN [A.20]. These challenges includes dynamic switching behavior, packaging impact and high frequency gate driver, etc.

1.3.1 Switching Characteristics

The switching speed of GaN devices are extremely fast that create significant parasitic ringing in hard-switching condition, as shown in Figure 1.8. High frequency ringing causes significant power loss as well as severe EMI noise. Soft-switching should be investigated both from loss and noise perspective.

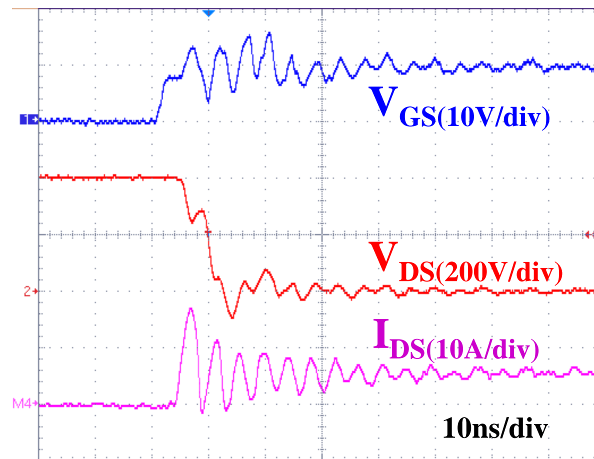


Figure 1.8 Hard-switching turn-on transient of GaN device

The cascode GaN devices have special switching characteristics due to two-discrete dies in one package. The interaction between the d-mode GaN and the low voltage Si MOSFET may induces undesired features, such as Si MOSFET reaches avalanche during turn-off transition, and d-mode GaN device loses zero-voltage turn-on condition internally during soft-switching turn-on process in every switching cycle. The worst occasion is that the cascode GaN may be subject to divergent oscillation under high-current turn-off condition. These phenomenon should be carefully studied to improve switching performance and avoid device failure.

1.3.2 Package Impact on Switching Behavior and Gate Reliability

The impact of device packaging has been studied in depth on Si MOSFET, SiC, and low voltage eGaN FET [A.20], [A.22], [A.23]. Package becomes very important to GaN devices with high switching speed. The package parasitic may hinder the switching transition and even generates severe ringing which can destroy the device [A.21]. However, some of the GaN devices manufacturers, who seek for simple replacement of Si devices, are still fabricating devices with long-lead through-hole package.

The common source inductance, which is defined as the inductor shared by the power loop and driving loop has a significant inpact on the switching loss. The power loop inductance plays an important role on the voltage and current ringing after the switching transition. The high voltage e-mode GaN is similar to Si MOSFET or SiC devices in terms of packaging structure, but with much higher switching speed. The cascode GaN has two dies in one package which introduces more package related parasitic inductance. It is essential to investigate the package of GaN for both e-mode GaN and cascode GaN devices to achieve minimum switching loss and less parasitic ringing.

1.3.3 High dv/dt and di/dt

GaN devices have a much lower gate charge and lower output capacitance than Si MOSFETs and, therefore, dv/dt and di/dt during switching transition is 3-5 times higher than that of Si MOSFETs.

Di/dt may induce an opposing voltage drop on the common source inductance which prevents either turn-on or turn-off from the gate drive circuit. It is strongly related to devices packaging and PCB layout. Dv/dt can couple through any parasitic capacitance

from switching node to ground. It may interference input PWM signal and cause false on/off issue. These issues have to be addressed to avoid becoming a limiting factor on circuit design.

1.4 Impact of GaN Devices on System Level Design

The potential impact of GaN goes beyond the simple measures of efficiency and power density. It is feasible to design a system with a more integrated approach at higher frequencies, and therefore, it is easier for automated manufacturing. This will bring significant cost reductions in power electronics equipment and unearth numerous new applications which have been previously precluded due to high cost.

1.4.1 High Frequency Magnetics

The traditional magnetic design is in hand-made fashion which is intensive labor involved manufacturing process. The cost is a concern and the parameter variation is another circuit design issue. PCB winding based transformer is only feasible when the switching frequency is over several hundreds of kHz due to less turns number and smaller core size. The leakage inductance and parasitic capacitance of transformer can be well controlled by PCB manufacture.

Generally speaking, GaN offers an opportunity to design the high frequency magnetics in a different way. Some key factors requires to be taken into considerations, such as high frequency core material, winding structure and fringing effect [A.24], [A.25], [A.26].

1.4.2 High Frequency EMI

GaN devices are double-edged sword from EMI perspective. High switching speed creates high dv/dt which increases the common-mode noise and corresponding filter size. High switching frequency, however, increases the corner frequency of the EMI filter, which reduces the EMI filter size. The concern is generally true with the system that is constructed with traditional magnetic design. However, the common mode noise can be significantly reduced by CPES developed balance technique [A.27], [A.28] and shielding technique [A.29]. The implementation of advanced EMI reduction technique and related system impact should be carefully investigated in different applications. In addition, the EMI filter structure and core material are crucial to achieve optimal performance, which should be carefully studied.

1.4.3 High Frequency control

To realize MHz frequency operation, the high frequency control is one of the most important factors, especially in soft-switching operation. It is crucial to detect soft-switching condition with minimal delay and generates precise PWM signal accordingly. There is no commercial control chip for front-end application that can operates above 1MHz. It is meaningful to implement the high frequency control concept with low-cost micro-controllers, which can be integrated to analog or mixed analog-digital control chip later on.

1.5 GaN Based Applications

GaN devices are already making inroads which stem directly from the improvements in figure of merits (FOM) over Si MOSFET. The applications includes point-of-load converters [A.18], [A.19], [A.20], [A.30], [A.31], class-D audio amplification [A.32], power factor correction [A.33][A.34][A.35][A.36], bus converter [A.37], motor drive [A.38], and PV inverters [A.39]. Additionally, GaN devices enable new applications that are not possible with Si MOSFET, such as envelope tracking [A.40], high frequency wireless power transfer [A.41] and LiDAR [A.3].

One of the biggest market of power supplies, in both volume and revenue, is the ac-dc adapter/charger for consumer electronics. The market is projected to surpass $8 billion in 2015 and reach $9 billion by 2018; with much of this growth being driven by smart phones, tablets and a number of emerging applications. The adapter is strongly driven by efficiency and power density for all forms of portable electronics. Most adapters only operate at relatively low frequencies (<100 kHz), with state-of-the-art efficiency up to 91.5%. However, low-frequency operation limits the adapter power density to 6-9 W/in^3. The emerging GaN device is deemed a game-changing device in this particular application, with improved efficiency and significant size reduction. Systematic design of adapters with different output power will be illustrated in this work to show the advance of GaN devices and the impact on system level.

1.6 Dissertation Outline

Taking into account the challenges associated with GaN devices as well as the impact

on system level design practice, several issues have been addressed in this dissertation.

Chapter 1: Research background, motivation, and literature review.

Chapter 2: Switching characterization of GaN devices, including packaging impact and special issues in cascode GaN devices. The switching loss mechanism of both e-mode and cascode GaN devices will first be explained and compared; then the package impact on switching performance of GaN device will be illustrated in details. The special issues in cascade GaN devices caused by capacitance mismatch are analyzed in detail and corresponding solutions are validated with numerous experiments.

Chapter 3: Design considerations of GaN devices. A thorough comparison of hard-switching and soft-switching is made which indicates that GaN devices still need soft-switching to fully explore potential. High frequency gate drive design for GaN devices to achieve high switching speed and handle high dv/dt and di/dt is presented.

Chapter 4: Application of GaN devices in AC-DC adapters. It will focus on the topology, high frequency transformer design, EMI characterization and high frequency control (majorly for ZVS achievement).

Chapter 5: Conclusion and future work.

Chapter 2. Switching Characterization of GaN Devices

Understand the switching characteristics of GaN switches, is essential to use GaN devices in circuit design correctly and efficiently. In this chapter, the switching loss mechanism of both e-mode and cascode GaN will first be explained and compared; then the package impact on switching performance of GaN device will be illustrated in details; finally, the special issues of cascode GaN devices are discussed and proposed solution is validated by experiments.

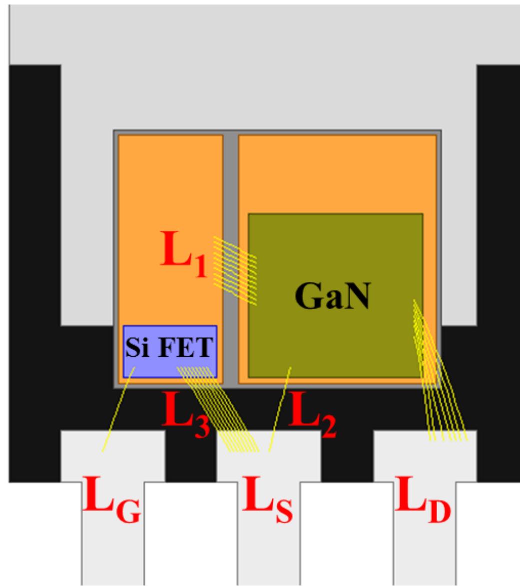
2.1 Switching Loss Mechanism Analysis of GaN Devices

2.1.1 GaN device loss model

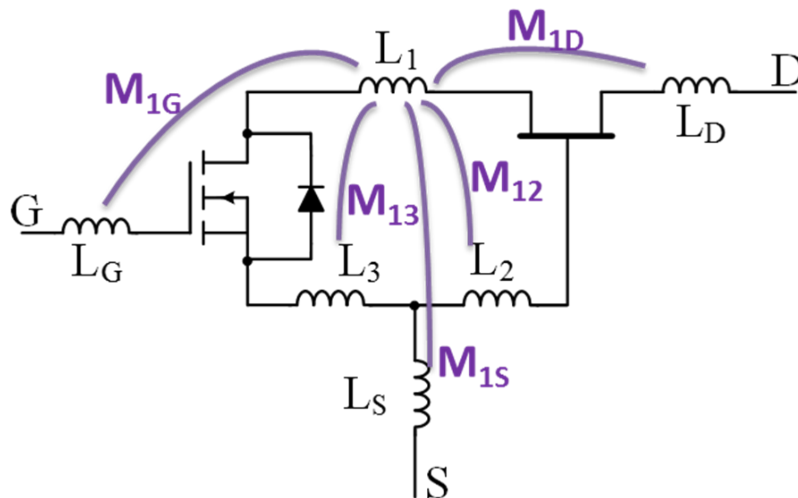
The fast switching ability of GaN devices will certainly reduce switching related loss compared to Si MOSFET. However, the switching voltage and current have more ringing due to high dv/dt and di/dt across the parasitics, shown in Figure 1.8, which may generate additional loss. More importantly, the switching loss analysis is highly desirable for predicting maximum device junction temperature and overall power converter efficiency.

Device manufacturer usually provides a Pspice based simulation model for simple circuit level simulation. However, this kind of model is lack of accuracy in terms of neglecting packaging and PCB layout related parasitic inductance. Taking a cascode GaN device from Transphorm as an example, the package introduces six pieces of parasitic inductance as shown in Figure 2.1. Moreover, as the currents with fast transitions are

confined in such a small area, the coupling effects between different conductors are significant. The coupling coefficients of L_1 with the other inductances are labeled in Figure 2.1(b). The methodology of parasitic inductance extraction of the cascode GaN device is summarized in [B.1].



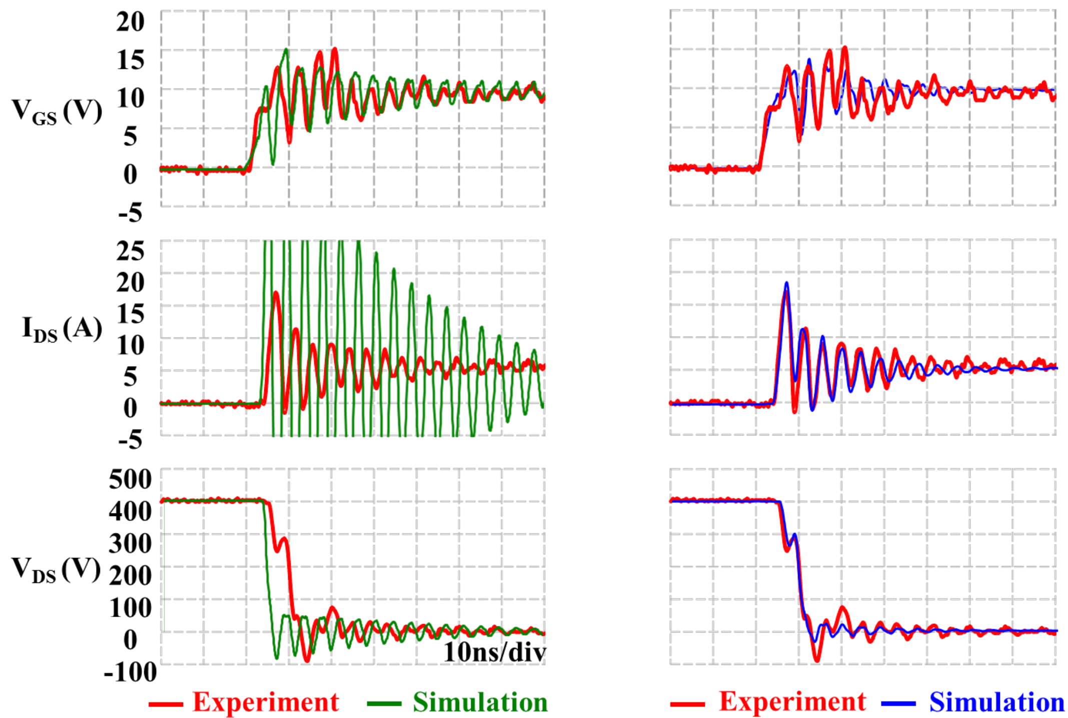
(a) Simplified bonding diagram of a cascode GaN device



(b) Equivalent circuit of cascode GaN considering all parasitic inductance

Figure 2.1 Packaging parasitics of a cascode GaN device

The comparison of switching waveforms based on manufacturer original model and modified model are shown in Figure 2.2. It clearly shows that the voltage and current ringing amplitude and slew rate are completely misaligned. It indicates the inaccuracy of the system parasitics, which include the device parasitics. With parasitic extraction of the device and PCB layout, the model presented in Figure 2.2(b) can effectively reproduce the experimental waveforms.



(a) Manufacturer original model (b) Modified model

Figure 2.2 Comparison of switching waveforms w/ original model and modified model

The author has also developed a mathematical based analytical model [B.2], which is based on device physical parameters listed in datasheet. It is independent of Pspice simulation model and can be applied to any devices. Moreover, analytical model separate

transition into several sub-stages, which helps engineers to better understand the physical meaning of device operation.

In order to show the derivation process of analytical model, the first stage of turn on transition of a cascode GaN in a buck converter is shown in Figure 2.3. More details about GaN device analytical loss model are illustrated in Appendix I. When the gate voltage V_G is applied, the resultant gate current charges the gate-source equivalent capacitance. In fact, C_{GS_Si} is much larger than any of the other capacitors in the cascode GaN transistor, thus the majority of the gate current charges C_{GS_Si}. As the GaN and silicon MOSFET are open circuit, almost no drain current flows into this circuit. During this period, the power stage does not change and current source I_L keeps flowing through D_b. Based on the equivalent circuit, the following equations are obtained:

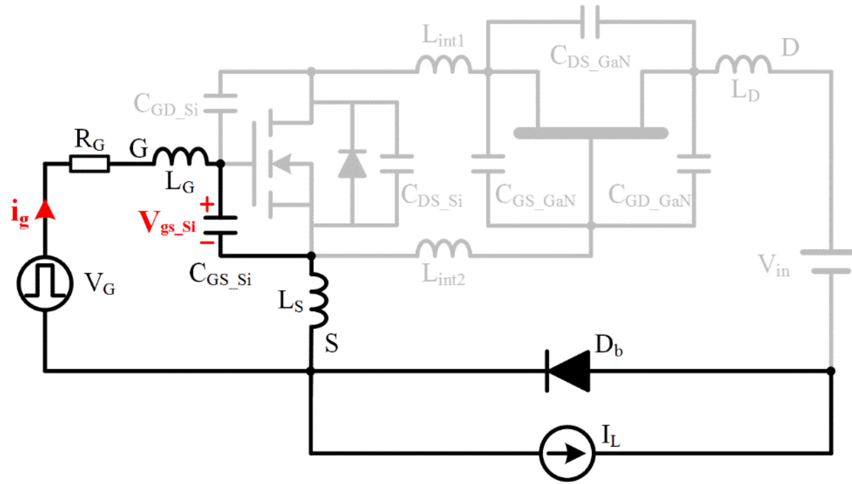


Figure 2.3 Equivalent circuit during the first stage of turn on transition

$$V_G = (L_G + L_S)\frac{di_g}{dt} + R_G \cdot i_g + v_{gs_Si} \tag{2.1}$$

$$i_g = C_{GS_Si}\frac{dv_{gs_Si}}{dt} \tag{2.2}$$

The Laplace and inverse Laplace transforms are applied to solve the differential equations. The silicon MOSFET gate-source voltage $v_{gs_Si}(t)$ is shown below. This stage ends when v_{gs_Si} reaches the threshold voltage of silicon MOSFET V_{TH_Si}.

$$v_{gs_Si}(s) = \frac{1}{s} \cdot \frac{V_G}{s^2 \cdot (L_G + L_S) C_{GS_Si} + s \cdot R_G C_{GS_Si} + 1} \tag{2.3}$$

$$v_{gs_Si}(t) = V_G \cdot \left(1 - \frac{s_{11} e^{s_{12} t} - s_{12} e^{s_{11} t}}{s_{11} - s_{12}}\right) \tag{2.4}$$

where $s_{11} = \sqrt{\frac{1}{4}\left(\frac{R_G}{L_G + L_S}\right)^2 - \frac{1}{(L_G + L_S) C_{GS_Si}}} - \frac{R_G}{2(L_G + L_S)}$, $s_{12} = -\sqrt{\frac{1}{4}\left(\frac{R_G}{L_G + L_S}\right)^2 - \frac{1}{(L_G + L_S) C_{GS_Si}}} - \frac{R_G}{2(L_G + L_S)}$.

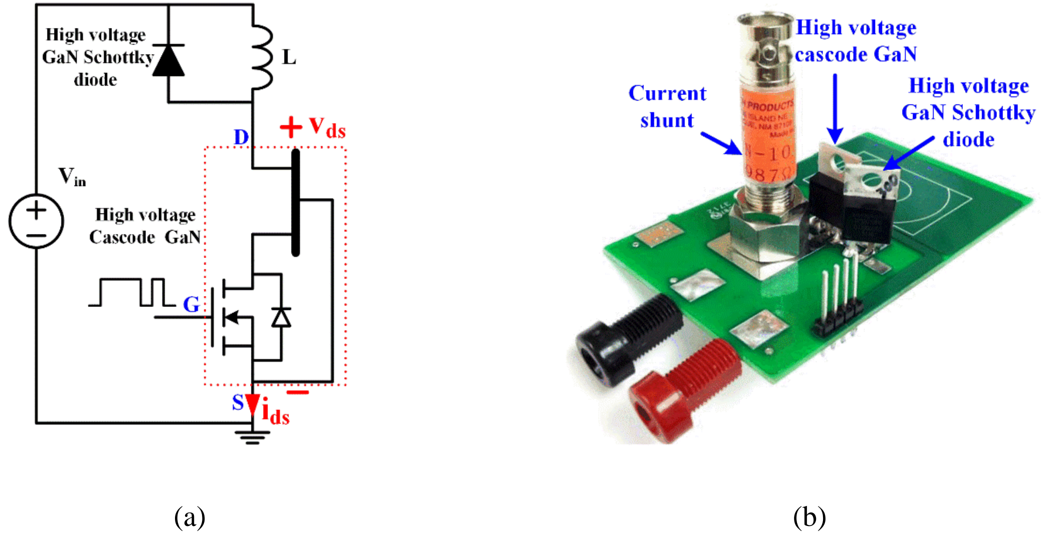
In order to verify the analytical model, two sets of experiments are carried out: a double-pulse test to compare the waveforms, and a buck converter to validate the switching loss. Common sense would dictate that the common source inductance, which is defined as the inductor shared by the power loop and driving loop, has a significant impact on the switching loss. In addition, the power loop inductance plays an important role in the switching performance. Therefore, the PCB is designed to eliminate the common source inductance (excluding package inductance) and to minimize the power loop inductance. The package and layout inductance are extracted from Ansoft Q3D FEA simulation and the value is summarized in Table 2.1. The PCB layout parasitic inductance is lumped together as two parts: one is the driving loop inductance, and the other is power loop inductance. The double pulse test circuit has larger power loop inductance since the current shunt introduces extra inductance and the PCB layout adds more inductance to accommodate the current shunt.

Table 2.1 Parasitic inductance of package and PCB layout

	L_{Dri_Loop}	L_{Power_Loop}
Double-pulse test	3.3nH	7.7nH
Buck Converter	3.3nH	3.7nH

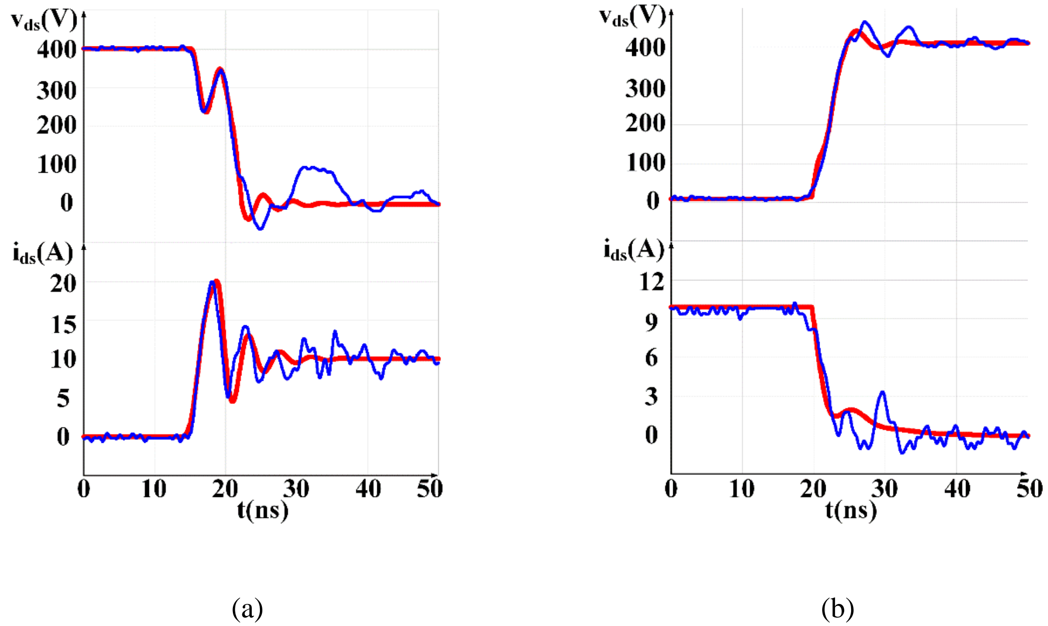
Figure 2.4 shows the double-pulse-test circuit diagram and prototype. The main switch is a 600V cascode GaN transistor, and terminal voltage v_{ds} and current i_{ds} are recorded to compare with the calculation results. The freewheeling diode is a 600V GaN Schottky diode with no reverse recovery charge. Both of these GaN devices are from Transphorm Inc. The current waveform is measured by a coaxial shunt resister with high bandwidth and minimized parasitic inductance.

Figure 2.5 shows waveform comparisons between the double-pulse-test and the calculated results of the proposed analytical model during the transition period. The figure clearly shows that the analytical model can match with the experiments on the voltage and current slope, as well as the magnitude and main transition time. The oscillation frequency and damping effect have some differences due to inaccurate high frequency parasitic inductance and AC resistance. As the value of the parasitic inductance and AC resistance is influenced by several factors, including conductor position, current direction and oscillation frequency, which are difficult to be predicted



(a) (b)

Figure 2.4 Model validation with double-pulse-test circuit: (a) diagram, (b) prototype



(a) (b)

Figure 2.5 Turn on/off waveforms comparisons (Blue line: experiment, red line: analytical model)

(a) Turn on @10A, (b) Turn off@10A

The second method used to validate the accuracy of the proposed analytical model is to observe the converter efficiency over a wide load range. A 500 kHz 380V/200V continues current mode (CCM) buck converter is built using a cascode GaN transistor as

the top and bottom switch. In the calculation terms, the inductor loss is measured by Mu's method [B.3]. The conduction loss is calculated based on the steady state current and on-resistance, which takes the temperature coefficient into consideration. The driving loss can be approximately calculated as:

$$P_{dri}(t) = Q_g V_G F_s \tag{2.5}$$

Figure 2.6 shows the converter efficiency comparison between the experimental results and the calculation results based on the proposed model. The calculated efficiency matches well with the experimental results over a wide load range. The difference is within 0.1%.

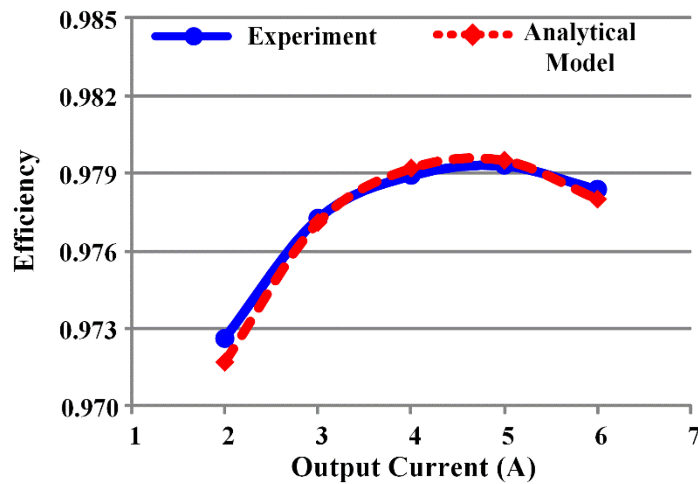


Figure 2.6 Efficiency comparison between experimental and calculation results based on proposed model

As the accuracy of the model is validated by numerous experimental results, then the model can be applied to analyze the switching loss mechanism of GaN devices.

2.1.2 Turn-on transition

It is noticed that the switching behavior of e-mode GaN switches is quite similar with

Si MOSFET except for the much higher switching speed. The detailed analysis can refer to literature [B.4]. On the other hand, the study on the switching behavior of cascode GaN is less comprehensive. To better illustrate the switching loss mechanism of the cascode GaN switch, typical turn-on switching waveforms of the control switch in a half-bridge configuration based circuit, which are derived from the device model, are shown in Figure 2.7.

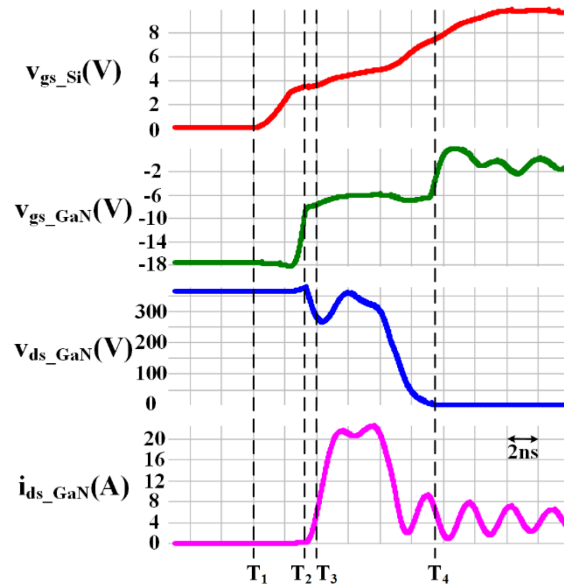


Figure 2.7 Hard-switching turn-on waveforms

V_{gs_Si} is the gate-source voltage of the low voltage silicon MOSFET in the cascode structure. The other three waveforms are the gate-source voltage, drain-source voltage and drain-source current of the GaN HEMT in the cascode structure. The switching loss of the low voltage silicon MOSFET is negligible, which is true in this condition. At T_1 instant, the gate voltage is applied to the silicon MOSFET. Then V_{gs_Si} is charged up and the channel becomes conductive. The gate-source voltage of the GaN HEMT which is in reverse parallel with the drain-source voltage of the silicon MOSFET, is charged towards

the threshold voltage. At T_2 instant, the GaN HEMT is conductive and i_{ds_GaN} starts to increase. At T_3 instant, the GaN HEMT current reaches the inductor current and then the GaN HEMT current supports both inductor current and reverse recovery charge current of free-wheeling switch during T_3 to T_4. During this period, the current overshoot is huge and it may saturates the channel as the GaN HEMT is not yet fully turned on in normal cases. Therefore, V_{ds_GaN} increases instead of decreases in the first half of this stage. In fact, this phenomenon can also be observed with standalone switch under high voltage test condition [B.5], [B.6]. Eventually the voltage across free-wheeling switch is charged up with the overshoot current of the control switch, and this allows the V_{ds_GaN} to be decreased to zero. The integral of voltage and current during the turn-on transition generates switching loss, which is in the magnitude of tens of uJ. This becomes significant at MHz frequency operation. It is worthwhile to point that the cascode GaN switch has some reverse recovery charge due to the series low voltage silicon MOSFET. However, the value of this charge is at least two orders of magnitude less than the comparable high voltage silicon MOSFET that has a similar on-resistance.

The turn-on switching loss of different GaN devices, which are listed in table 1.2, are shown in Figure 2.8. The loss curves delivers two messages. First, the turn-on switching loss of cascode GaN is higher than e-mode GaN due to low voltage Si MOSFET body diode Q_{rr} effect. Secondly, the turn-on switching loss is in a range of few tens of uJ, which is few tens of watts if the switching frequency is 1MHz. The huge turn-on switching loss is definitely an enemy to further push frequency.

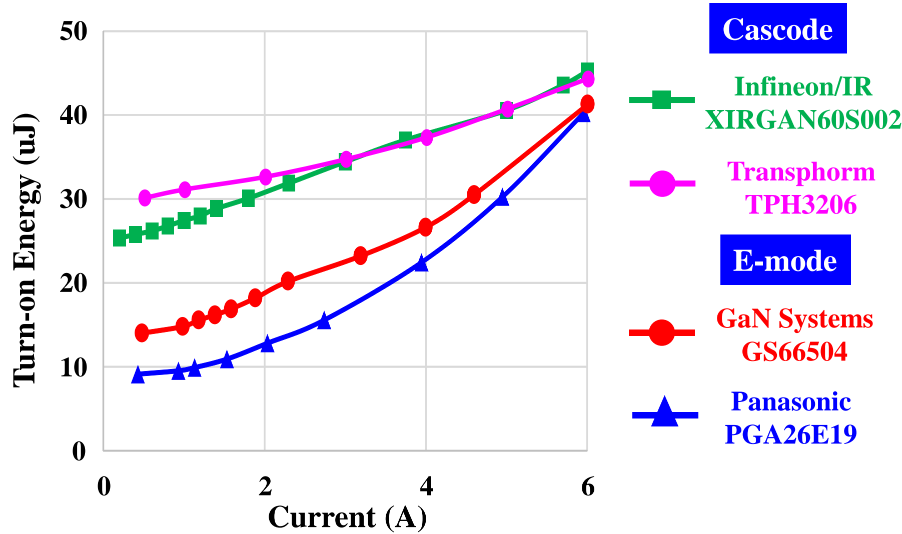


Figure 2.8 Turn-on switching loss of different GaN devices

2.1.3 Turn-off transition

The key waveforms for control switch turn-off transition is shown in Figure 2.9. At T_1 instant, the gate driving signal is removed, and then the silicon MOSFET gradually enters the saturation region. The drain-source voltage of silicon MOSFET increases which also means v_{gs_GaN} decreases. At T_2 instant, the GaN HEMT enters the saturation region and the channel current starts to decrease and V_{ds_GaN} starts to increase. Because of the internal current source turn off mechanism, which is unique to cascode structure, V_{gs_GaN} shortly drops below the pinch off value at T_3 [B.2]. Then the rest of the terminal current charges the C_{oss} and consequently V_{ds_GaN} rises to the steady state value. The inductor current transfers from the control switch to the free-wheeling switch. It clearly shows that the voltage and current transition time is short and the energy dissipation is about 0.2uJ. This value is extremely small compared to the same level Si MOSFET which is typically larger than 5uJ. During the turn off transition, the low voltage silicon MOSFET dissipates about

0.2uJ energy.

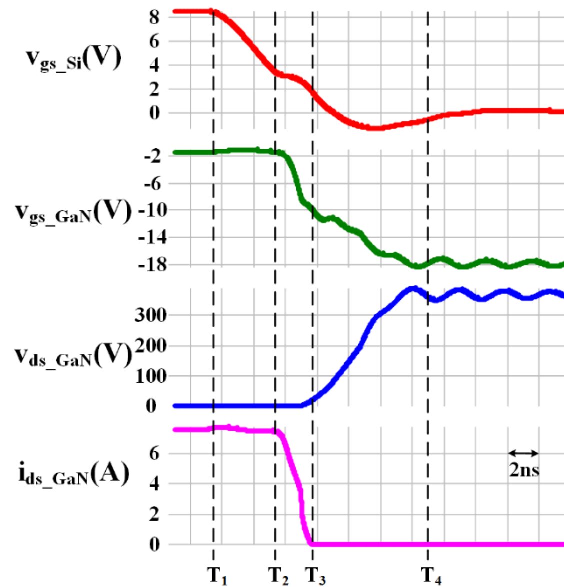


Figure 2.9 Hard-switching turn-off waveforms

Even though e-mode GaN can achieve fast turn-off as well and the terminal waveforms look very similar, the insight turn-off mechanisms are different from each other. Figure 2.10 compares the basic principle of turn-off transitions for two types of GaN devices. For e-mode GaN devices, the gate discharging current is limited by gate driver circuit. In addition, the current charging miller capacitance (C_{gd}) also flows into driving circuit, which further decrease the gate discharging current. This phenomenon is well known as miller effect [B.7].

For cascode GaN devices, the GaN gate discharging current is provided by power loop, which is relatively larger than external gate drive current. It can be considered as a constant current source to discharge gate voltage, which usually helps to reduce the switching loss [B.8], [B.9]. Moreover, the current charging miller capacitance C_{gd} directly flows to source

terminal, which bypasses C_{gs}. These unique features of cascode GaN make the turn-off loss extremely small and not sensitive to the turn-off current.

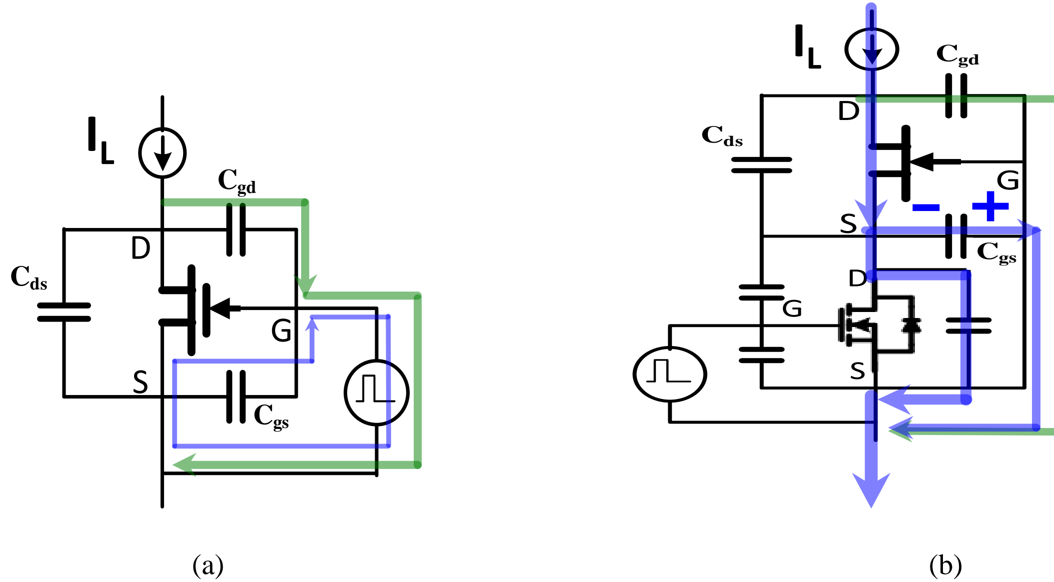


Figure 2.10 Turn-off mechanism of different types of GaN devices: (a) e-mode, (b) cascode

The turn-off switching loss of different GaN devices are shown in Figure 2.11. At lower turn-off current condition, all GaN devices can achieve very small turn-off loss. As the current increases, the turn-off loss of e-mode GaN devices increases due to stronger miller effect. However, the turn-off loss of cascode GaN is almost constant over wide current range.

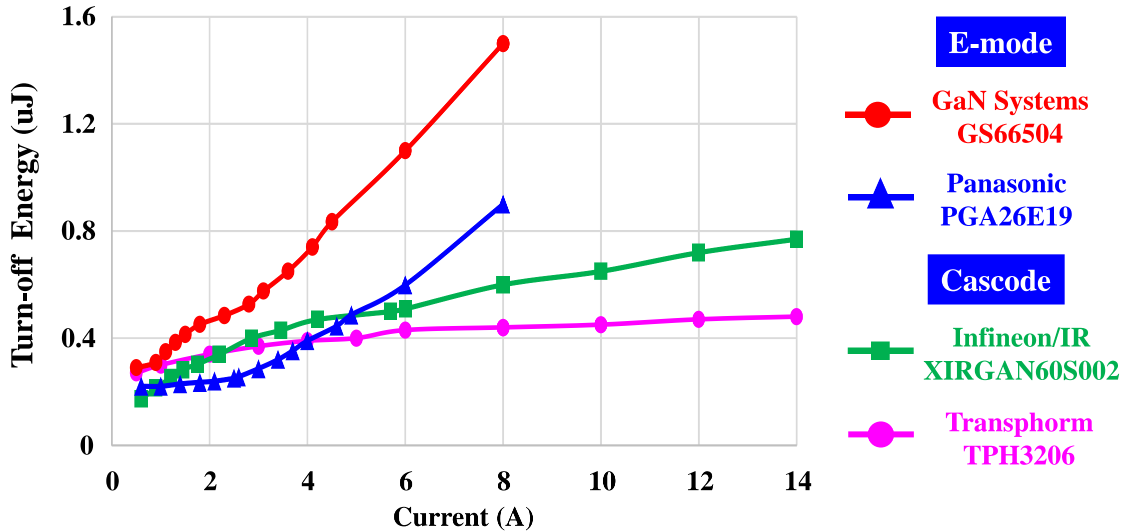


Figure 2.11 Turn-off switching loss of different GaN devices

It is interesting to find out that the turn-on switching loss is dominant and it may generates above 10W at 500kHz operation. On the other hand, the turn-off switching loss is negligible compared to turn-on loss, which indicates that zero-voltage-switching (ZVS) is desired to fully exploit the potential of the GaN switches. More detailed analysis will be presented in chapter 3.

It is worthwhile to point out that the turn-off switching loss of GaN devices is much smaller than state-of-the-art Si MOSFET. Figure 2.12 compares the turn-off switching loss of GaN switch and Si MOSFET based on double-pulse test circuit. The part number of GaN switch is TPH3206 which is cascode GaN. The part number of Si MOSFET is FCP13NF0 from Fairchild. It is obvious that the turn-off loss of Si MOSFET significantly increases with current due to miller effect and it is much higher than GaN devices.

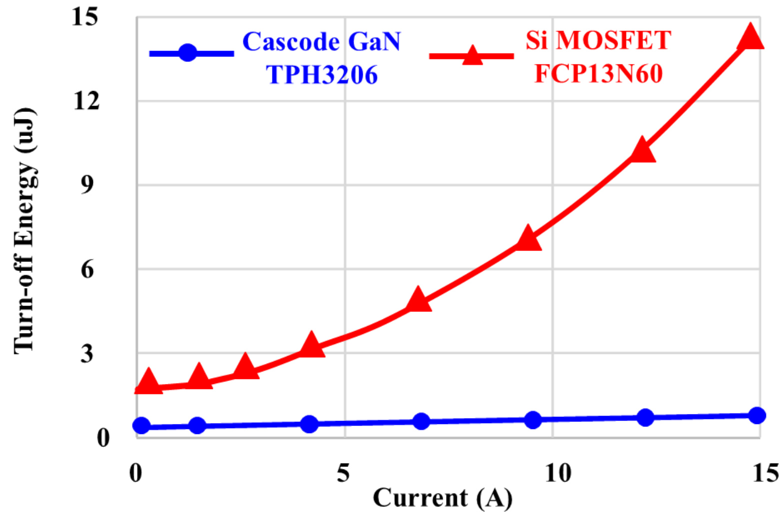
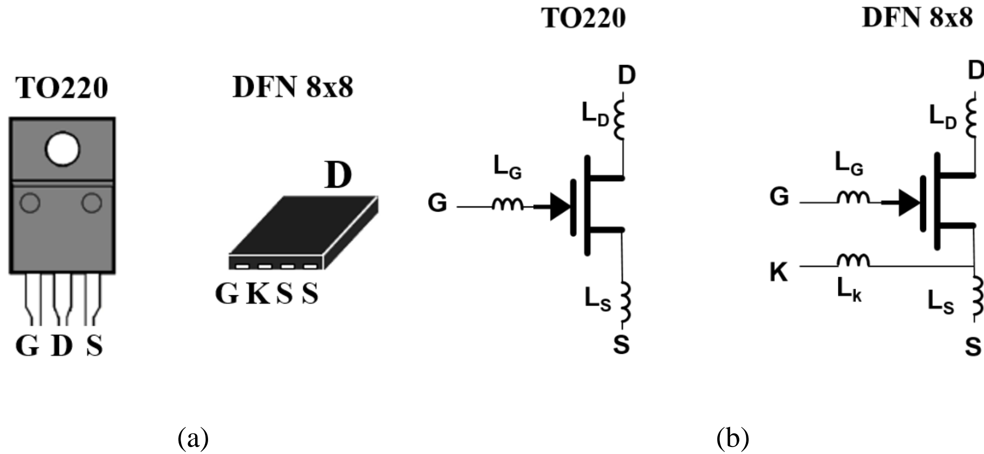


Figure 2.12 Comparison of turn-off switching loss: GaN vs. Si

2.2 Packaging Impact on Switching Loss

The switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition. Unfortunately, not every GaN devices manufacturer has realized the importance of packaging. Up to date, there is variety of packages for 600V GaN switches. TO220 and DFN packages are used for 600V Panasonic e-mode GaN devices [B.10], [B.11]. Figure 2.13 shows the package-related parasitic inductance and the value is listed in Table 2.2 which are extracted by FEA simulation in Ansoft Q3D. With Kelvin connection, the DFN package is able to decouple the power loop and driving loop, and therefore it can minimize the common source inductance. Moreover, the inductance of DFN package is much smaller than TO220 package due to shorter wire bonding length, which also helps to reduce the loss and ringing issue. It should be noticed that GaN Systems, which is another e-mode GaN manufacturer, employs the chip-scale embedded package

and the parasitic inductance is even smaller than Panasonic DFN package. The benefit of improved package is similar to the DFN over through hole package, which will not be repeated here.



(a) (b)

Figure 2.13 Package and related inductance of 600V e-mode GaN devices: (a) Packages for 600V e-mode GaN, (b) Package related inductance

Table 2.2 Package-related parasitic inductance values

	L_G	L_D	L_S	L_K
TO-220	3.6nH	2.3nH	3.9nH	N/A
PQFN	2.4nH	1.3nH	0.9nH	1.3nH

The key experimental waveforms with two different packages are shown in Figure 2.14 and Figure 2.15. For the turn-on transition, the voltage and current slew rate of DFN package is much larger than that of TO220 package due to smaller common source inductance and loop inductance. As a result, the turn-on energy of DFN package is much smaller than TO220 package as shown in Figure 2.16. For the turn-off transition, a severe ringing occurred in TO220 package. The false turn-on is observed at high current turn-off

condition as shown in Figure 2.15, and therefore, the turn-off energy of TO220 package increases dramatically with turn-off current.

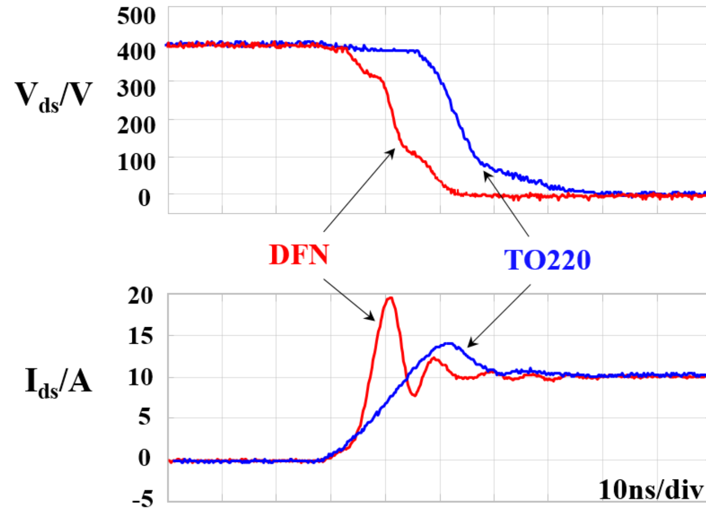


Figure 2.14 Turn-on transition of different packages

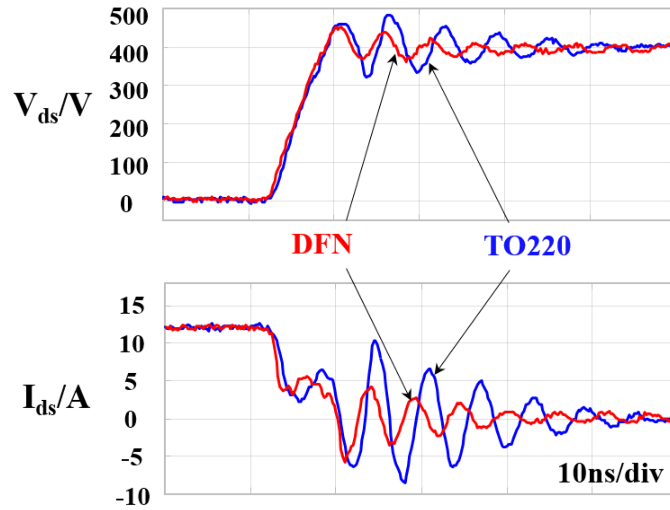


Figure 2.15 Turn-off transition of different packages

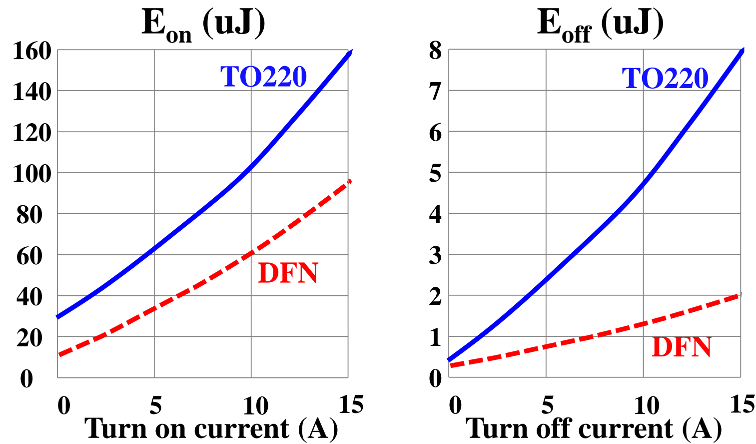
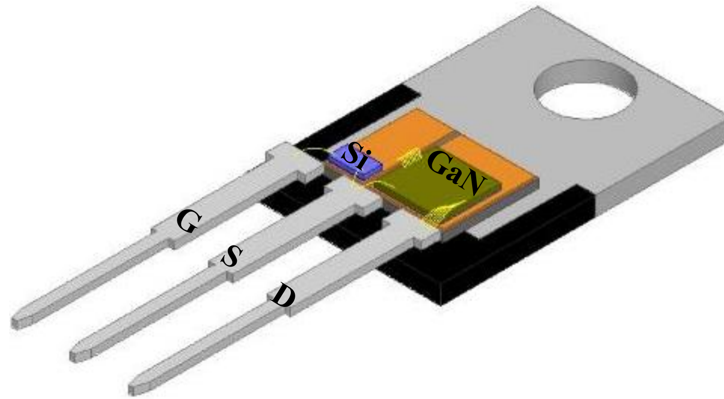


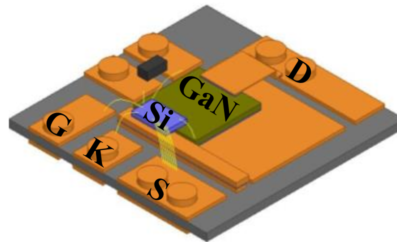
Figure 2.16 Switching energy of different package

Different from e-mode GaN, cascode GaN devices has relative complicated parasitic inductance distribution due to two dies package. Figure 2.17 shows two different packages for cascode GaN devices and the corresponding parasitic inductance is marked in Figure 2.18. One is TO220 package provide by Transphorm, the other one is stack-die package which is proposed and fabricated in CPES. The d-mode GaN die and Si MOSFET die are mounted side by side in TO220 package and inter-connection creates additional three parasitic inductance. In the stack die package, the Si MOSFET is mounted on top of the GaN die which eliminates two internal inductance. The connection between GaN gate and Si source still uses wire bonding which is less important due to smaller current and di/dt. In addition, stack die package provides a kelvin connection to decouple the power loop and driving loop, which can significantly reduce the switching loss. The turn-on waveforms under 400V/5A condition in a double-pulse-test circuit are shown in Figure 2.19. The dv/dt increases from 90V/ns to 130V/ns due to reduced parasitic inductance. The main transition period reduces to 4ns. The measured switching energy comparison of these two packages

is shown in Figure 2.20 which shows that stack-die package reduces turn-on switching loss by half.

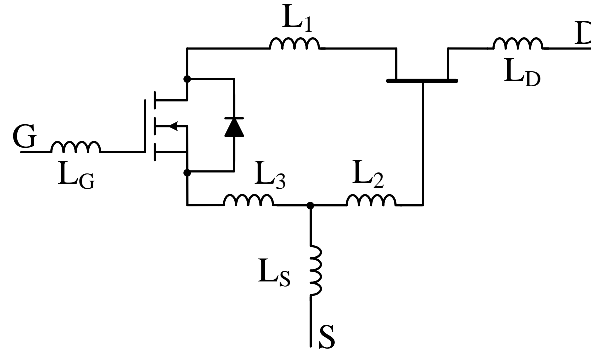


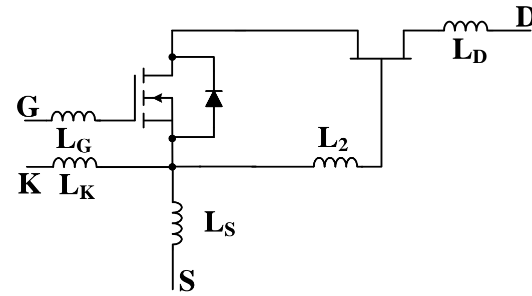
(a)



(b)

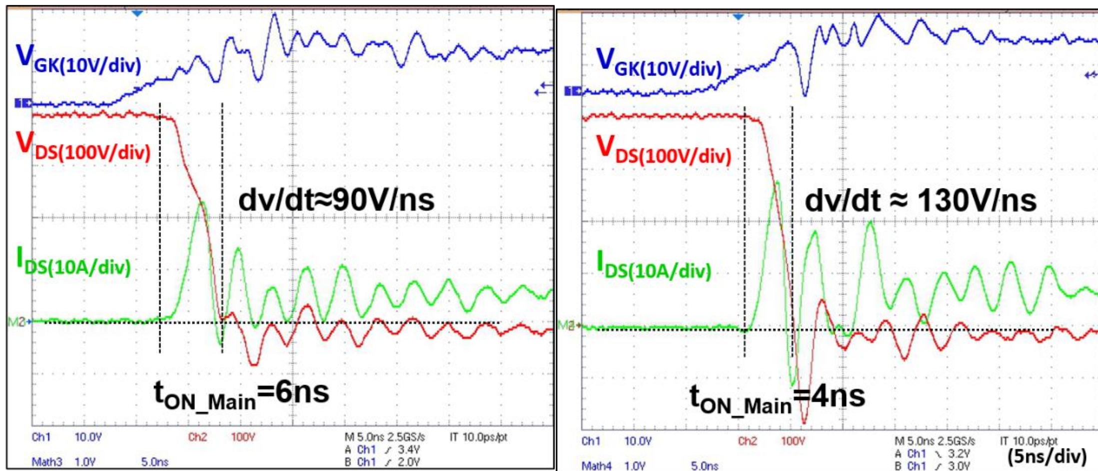
Figure 2.17 Two different packages for cascode GaN devices: (a) To 220 Package, (b) Stack die package





(a) (b)

Figure 2.18 Two packages related parasitic inductance: (a) TO220 package, (b) Stack-die package



(a) (b)

Figure 2.19 Turn-on waveform comparison between (a) TO-220 package, and (b) Stack-die package

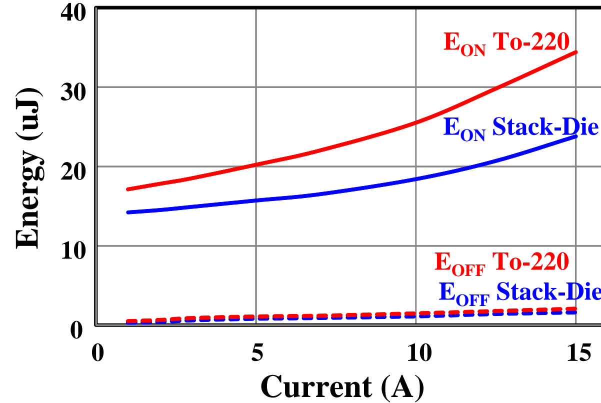


Figure 2.20 Switching energy comparison of different packages

2.3 Special Issues in Cascode GaN Devices

The cascode structure is usually applied to a d-mode GaN device and makes it a normally-off device. However, the interaction between the high-voltage d-mode GaN and the low-voltage Si MOSFET may induce undesired features. The inter-connection related parasitic inductance and junction capacitor ratio between the MOSFET and the d-mode GaN switch should be designed properly to avoid reliability issues and improve switching performance.

To analyze the interaction of a cascode GaN device, a boost converter is used as an example. The bottom switch is the cascode GaN device shown in Figure 2.21.

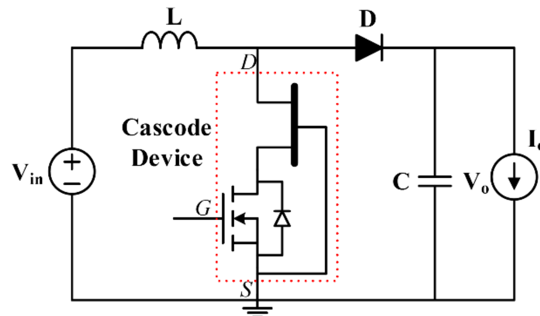


Figure 2.21 Boost converter with cascode GaN device

2.3.1 Si MOSFET Avalanche

The voltage distribution between the GaN switch and the Si MOSFET during the turn-off transition is largely determined by the junction capacitor charge. There are two possible turn-off transitions in the cascode GaN device, which are shown in Figure 2.22. The waveforms are derived from simulation models of two different cascode GaN devices.

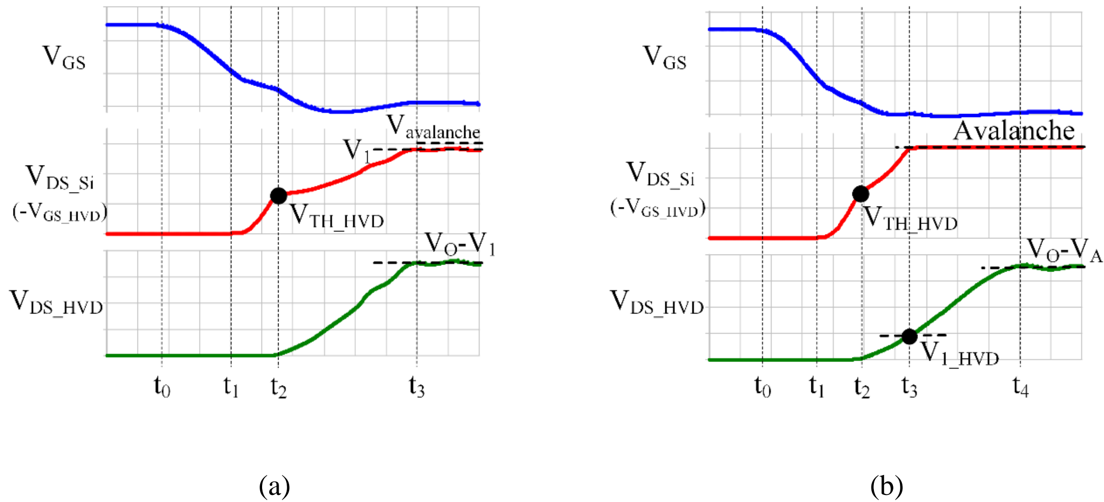
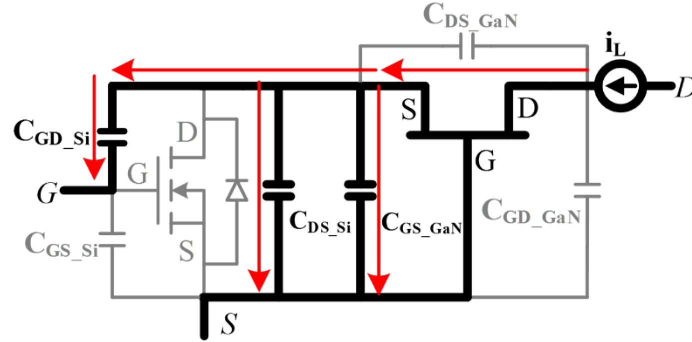


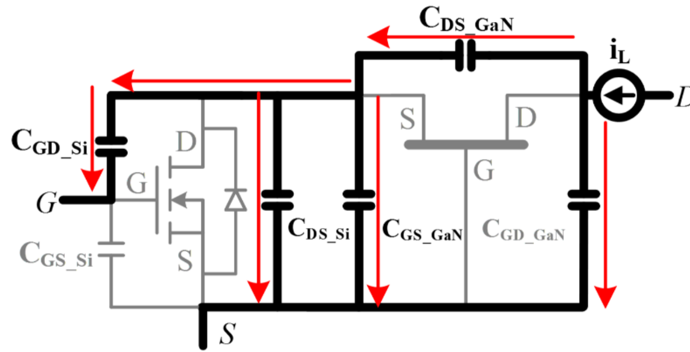
Figure 2.22 Two possible turn-off transition of cascode GaN devices

V_{GS} is the gate signal applied on the gate-source terminal of the cascode GaN device. V_{DS_Si} and V_{DS_GaN} are the drain-source voltage of the Si MOSFET and GaN switch, accordingly. It is apparent that the gate-source voltage of the GaN switch is the same as the drain-source voltage of the Si MOSFET with reverse polarity. The difference in waveforms between these two cascode devices is determined by whether the Si MOSFET is driven to avalanche. The definition of a well-matched cascode GaN device is that the charge stored in c_{DS_GaN} is lower than the charge stored in C_{OSS_Si} and C_{GS_GaN}, where C_{OSS_Si} is the sum of C_{DS_Si} and C_{GD_Si}. Similarly, a mismatched cascode GaN device means the charge of C_{DS_GaN} is larger than the charge of C_{OSS_Si} and C_{GS_GaN}. To better illustrate the voltage distribution process, the equivalent circuits during t_1-t_4 are shown in Figure

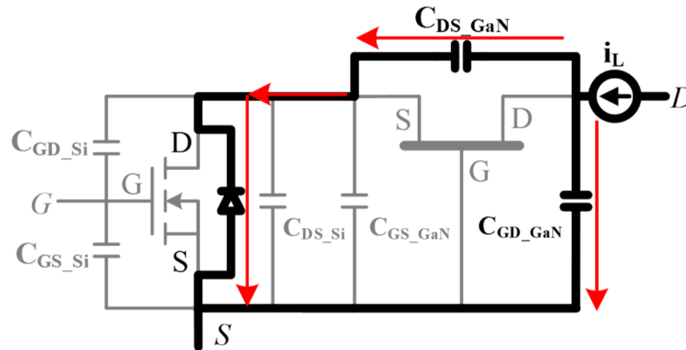
2.23. The stage III equivalent circuit only exists in the mismatched cascode GaN device. The inductor current is treated as a current source during the turn-off transition period.



(a) Stage I: t_1-t_2



(b) Stage II: t_2-t_3



(c) Stage III: t_3-t_4

Figure 2.23 Si MOSFET reaches avalanche during turn-off transition

The turn-off signal is applied to the gate terminal of the Si MOSFET at t_0, and the MOSFET channel is turned off at t_1. Then C_{OSS_Si} and C_{GS_GaN} are charged in parallel

through the channel of the GaN switch until the source-gate voltage of the GaN switch rises to its threshold voltage V_{TH_GaN} at t_2. Then the GaN switch is turned off, and C_{DS_GaN} is charged in series with C_{OSS_Si} and C_{GS_GaN}. The charging path through C_{GD_GaN} has no impact on the voltage distribution between the GaN switch and the Si MOSFET. For a well-matched cascode device, the terminal current charges these capacitors until the voltage reaches steady state. V_{DS_Si} reaches V_1, which is lower than avalanche value V_{av}, and V_{DS_GaN} rises to V_O-V_1. The turn-off transition is completed at t_3.

For a mismatched cascode GaN device, V_{DS_Si} is driven to avalanche at t_3, while V_{DS_GaN} only rises to V_{1_GaN}, which is quite a bit lower than the steady state value. During Stage II, the total amount of charge stored in C_{OSS_Si} and C_{GS_GaN} is defined as Q_{II}. There is the same amount of charge stored in C_{DS_GaN}, since they are in series on the current path. During Stage III, the Si MOSFET stays in the avalanche region. C_{DS_GaN} is charged independently through the avalanche path as shown in Figure 2.23(c), and the V_{DS_GaN} rises from V_{1_GaN} to the steady state value. The total amount of charge stored in C_{DS_GaN} during Stage III is defined as Q_{III}. The same charge flows through the avalanche path, which causes additional loss in every switching cycle. This part of the loss is defined as P_{av} and can be quantified as (2.2), where f_s is the switching frequency.

$$P_{av} = V_{av} \times Q_{III} \times f_s \tag{2.6}$$

P_{av} is proportional to the switching frequency, which is undesired at high frequency.

2.3.2 GaN Internal Switching Loss

Similar to the turn-off transition, there are two possible ZVS turn-on transitions in a cascode GaN device, which are shown in Figure 2.24. The negative inductor current is used

to discharge the junction capacitors to achieve ZVS. The waveform difference between these two cascode devices is whether the V_{DS_GaN} drops to zero when V_{DS_Si} drops to V_{TH_GaN}. The equivalent circuits are shown in Figure 2.25. The mismatched device has one more stage than the well-matched case.

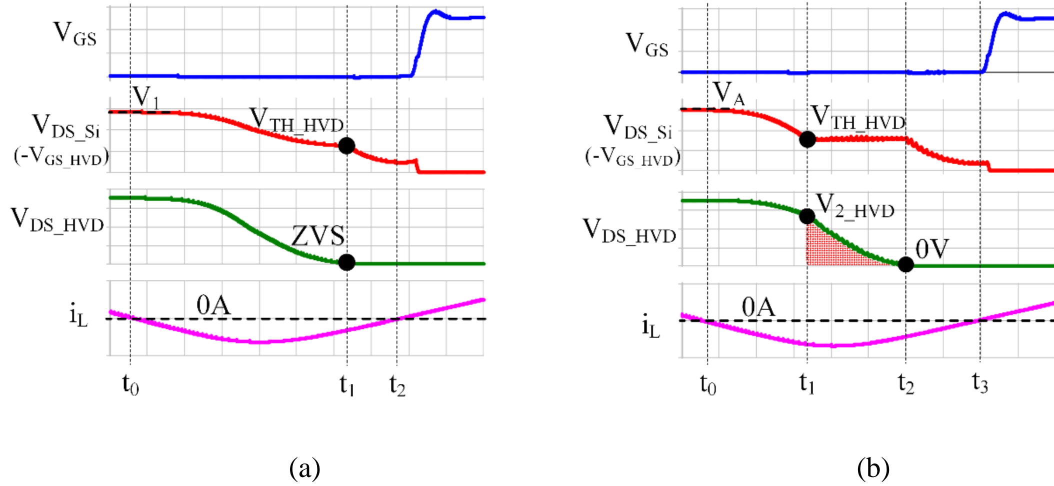


Figure 2.24 Two possible ZVS turn-on transition of cascode GaN devices

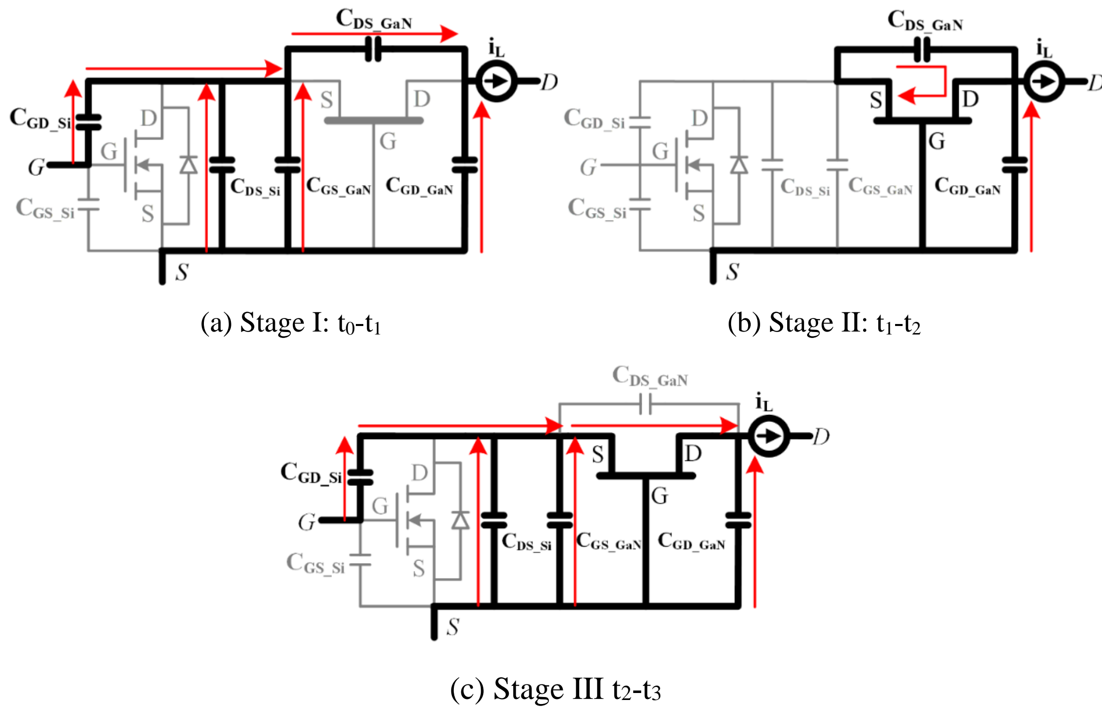


Figure 2.25 GaN internal switching loss during ZVS turn-on transition

At t_0, the negative inductor current begins to discharge the junction capacitors. C_{DS_GaN} is discharged in series with C_{OSS_Si} and C_{GS_GaN} from the initial condition. For the well-matched cascode device, V_{DS_Si} decreases from initial value V_1 to V_{TH_GaN} at t_1. Meanwhile, V_{DS_GaN} drops from initial value V_O-V_1 to zero due to the charge balance. This stage is the reverse process of voltage distribution during the turn-off transition. The total amount of charge stored in C_{DS_GaN} as well as C_{OSS_Si} and C_{GS_GaN} is completely recycled to the input source. After V_{DS_Si} reaches V_{TH_GaN}, GaN switch is turned on and the remaining charge stored in C_{OSS_Si} and C_{GS_GaN} is continuously discharged by the inductor current as shown in Figure 2.25(c).

For a mismatched cascode device, since the charge stored in the GaN switch is much larger than the charge stored in the Si MOSFET, V_{DS_GaN} only decreases to V_{2_GaN} when V_{DS_Si} decreases to V_{TH_GaN} at t_1. The total charge being discharged during Stage I is Q_{II} which is exactly the charge stored during the turn-off in Stage II.

After V_{DS_Si} decreases to V_{TH_GaN}, the channel of the GaN switch begins to conduct during Stage II, as shown in Figure 2.25(b). The remaining charge of C_{DS_GaN} which is Q_{III}, is dissipated through the channel directly, and this induces additional turn-on loss that is proportional to the switching frequency. During Stage II, the voltage decrease slopes of C_{DS_GaN} and C_{GD_GaN} are consistent. The majority of the inductor current flows through C_{GD_GaN}, and the circuit satisfies the following equations:

$$\begin{cases} v_{DS_GaN} + v_{DS_Si} = v_{GD_GaN} \\ C_{GD_GaN} \dfrac{dv_{GD_GaN}}{dt} = i_L \\ C_{DS_GaN} \dfrac{dv_{DS_GaN}}{dt} = g_{f_GaN}(-v_{DS_Si} - V_{TH_GaN}) \end{cases} \tag{2.7}$$

where g_{f_GaN} is the transconductance of GaN switch.

A small decrease in V_{DS_Si} results in a large increase of the GaN switch displace current, which leads to a fast voltage decrease slope. Therefore, V_{DS_Si} stays almost constant during this stage to maintain a consistent voltage slope, which is shown in Figure 2.24(b). The waveform of V_{DS_GaN} makes the terminal waveform of the cascode GaN device appear to have ZVS turn-on. However, part of the energy stored in C_{DS_GaN} is actually dissipated internally due to a mismatch in charge. This phenomenon always occurs, no matter what kind of ZVS techniques are applied. The internal switching loss is related to the mismatch charge, and Figure 2.26 shows the relationship, which is derived from simulation. For the cascode GaN device used in experiments shown in next section, the GaN device rating is 600V/12A and the Si MOSFET rating is 30V/11A. The mismatch charge is around 10.5nC.

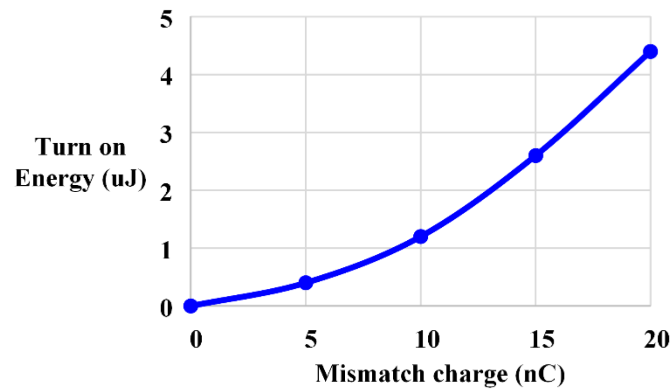


Figure 2.26 The relationship of internal turn-on switching loss and mismatch charge

Overall, the junction capacitance mismatch of the Si MOSFET and the GaN switch in a cascode structure will cause the Si MOSFET to reach avalanche and lose ZVS of the GaN switch even when a ZVS technique is applied. The avalanche loss and internal GaN switch turn-on loss are proportional to the switching frequency and related to mismatched charge. These prevent the cascode GaN device from being applicable to MHz frequency

applications, and the additional power loss may impact the thermal condition of the device. Therefore, this issue must be solved for reasons of both efficiency and reliability.

2.3.3 Failure I: Internal GaN Gate Ringing

Even soft-switching can eliminate the turn-on switching loss, the device failure is still observed with clean external waveform. The GaN gate breakdown is illustrated in Figure 2.27. For example, if the drain-source breakdown voltage of a Si MOSFET is 30V, and the gate-source breakdown voltage of a GaN is -35V, then the avalanche of the Si MOSFET, which clamps the V_{DS_Si} at 30V, acts like a last defense to protect against gate breakdown of the GaN.

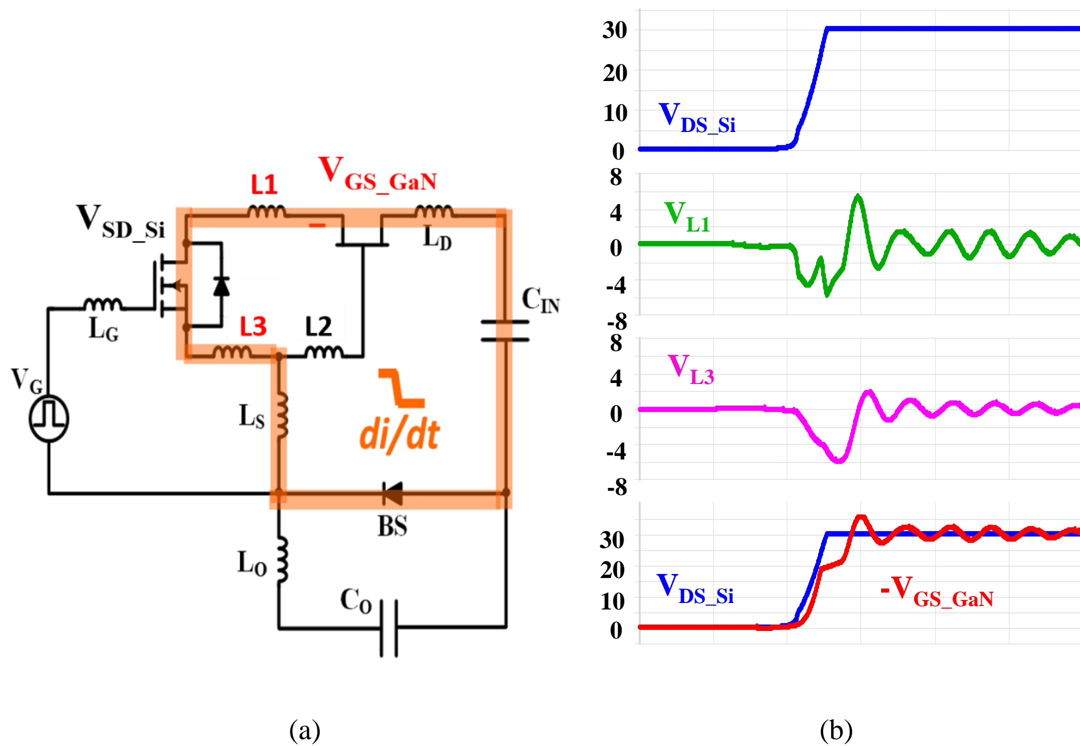


Figure 2.27 GaN gate breakdown due to parasitic ringing during turn-off transition: (a) di/dt loop during turn-off transition, (b) Key waveforms during turn-off transition

The insurance offered by the Si MOSFET fails due to high di/dt and package-related parasitic inductance. During the turn-off transition, voltage spike on GaN gate is observed due to parasitic ringing, and the amplitude is determined by (2.4).

$$V_{GS_GaN} = -(V_{DS_{Si}} + V_{L1} + V_{L3} + V_{L2}) \tag{2.8}$$

V_{L1} and V_{L3} contribute most to the parasitic ringing since the power loop current flows through the inductance. Even V_{DS_Si} is clamped to 30V, V_{GS_GaN} reaches the maximum breakdown voltage easily. The parasitic ringing amplitude increases with current and the GaN gate confronts the ringing in every switching cycle.

2.3.4 Failure II: Divergent Oscillation at High Current Turn-off Condition

The capacitance mismatch may cause the cascode GaN to have divergent oscillation issue under high-current turn-off condition. The voltage ringing formed by the loop inductance and junction capacitors may exceed the threshold to trigger the GaN's internal turn-on mechanism as illustrated in section 2.3.2, and therefore leads to divergent oscillation.

The turn-off process of a capacitance mismatched cascade GaN switch is the same as that shown in Figure 2.22 (b). V_{DS_Si} reaches avalanche, while V_{DS_GaN} only increases to V_{1_GaN}. Then the Si MOSFET stays in the avalanche region, and V_{DS_GaN} is charged up to the peak value V_{peak} through the avalanche path.

After V_{DS_GaN} reaches V_{peak}, the turn-off transition period is over, and the junction capacitance of the cascode GaN device oscillates with loop inductance L_P. The initial voltages of V_{DS_GaN} and V_{DS_Si} are V_{peak} and V_{av}, respectively. The initial oscillation current of L_P is 0A. The ideal oscillation waveforms of V_{DS_GaN} and i_{Lp} without considering the

damping effect are the dashed curves shown in Figure 2.28. The ideal oscillation amplitude is V_{peak}. The detailed operation can be described as follows:

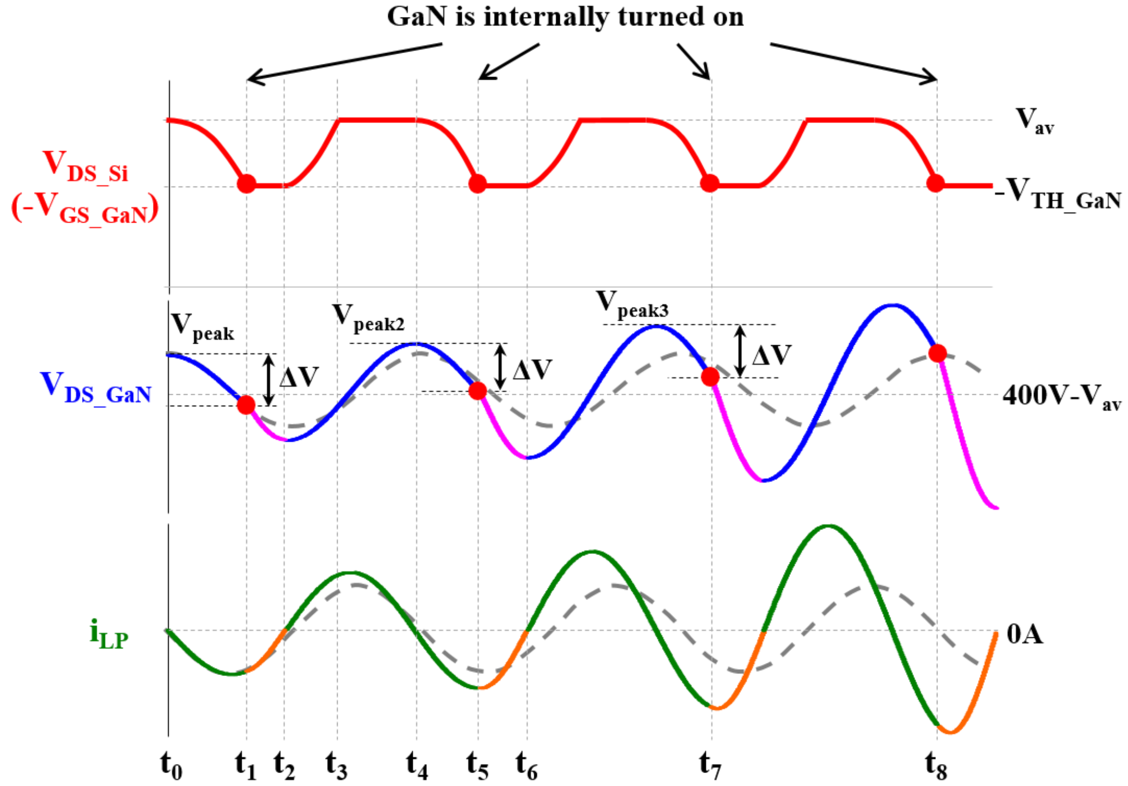
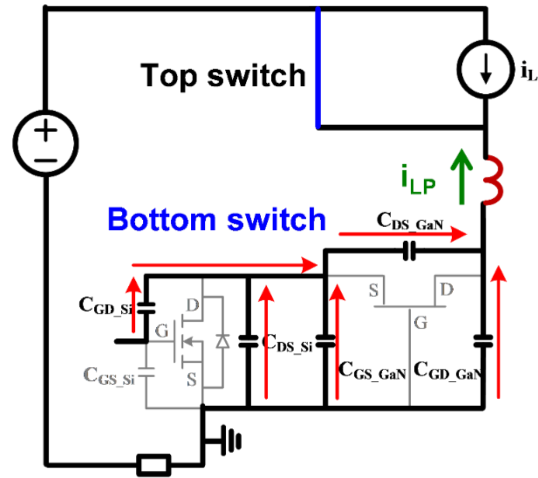


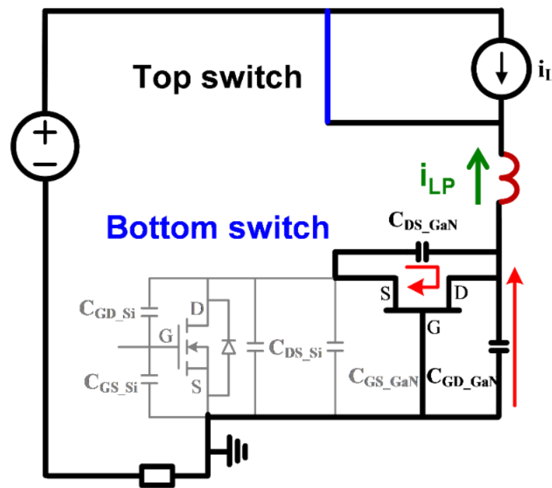
Figure 2.28 Illustration of divergent oscillation

[t_0-t_1]: L_P resonates with two capacitance branches. Branch I is C_{DS_GaN} in series with C_{OSS_Si} and C_{GS_GaN}. Equivalent capacitance value of this branch C_{equ} is shown in equation (2.5). Branch II is C_{GD_GaN}. The equivalent circuit of this period is shown in Figure 2.29(a). C_{DS_GaN} is discharged in series with C_{OSS_Si} and C_{GS_GaN} by part of the loop inductance current i_{LP} during this stage, and very similar to the stage I of ZVS turn-on process shown in Figure 2.25(a). State equations of this period is shown in equation (2.6), in which V_{DS} is the drain-source terminal voltage of bottom switch, and R_L is the total loop resistance including on-resistance of top switch and current shunt. With large enough ringing

amplitude, at t_1 instant, V_{DS_Si} reaches $-V_{TH_GaN}$, while V_{DS_GaN} only drops ΔV, which is smaller than the ideal resonant peak-peak amplitude. The charge removed in capacitance branch I during this stage is Q_{II} which is the same charge stored during stage II of turn-off process mentioned above.



(a) t_0-t_1 equivalent circuit



(b) t_1-t_2 equivalent circuit

Figure 2.29 Equivalent circuits during oscillation period

$$C_{equ} = \frac{(C_{OSS_Si}+C_{GS_GaN})\cdot C_{DS_GaN}}{C_{OSS_Si}+C_{GS_GaN}+C_{DS_GaN}} \tag{2.9}$$

$$\begin{cases} \left(C_{equ} + C_{GD_GaN}\right) \cdot \frac{dV_{DS}}{dt} = i_{LP} \\ V_{in} - L_P \cdot \frac{di_{LP}}{dt} - i_{LP} \cdot R_L = V_{DS} \\ V_{DS} = V_{GD_GaN} \end{cases} \tag{2.10}$$

[t_1-t_2]: After t_1, GaN is internally turned on and C_{DS_GaN} is bypassed by the GaN channel directly. Therefore, the loop inductance L_P only resonates with C_{GD_GaN}, and the equivalent circuit is shown in Figure 2.29(b). State equations of this period is shown in equation (2.7). The resonant period is reduced due to the smaller capacitance, and characteristic impedance becomes larger. With the same current and voltage initial conditions at t_1, larger characteristic impedance means larger resonant amplitude of capacitance voltage. So, the voltage drop of V_{DS} increases compared with ideal case. V_{GS_GaN} remains almost constant during this stage with the same reason described in section 2.3.2. Although C_{DS_GaN} does not participate in oscillation during this stage, V_{DS_GaN} and V_{GD_GaN} still satisfy the KVL law, which is shown in equation (2.8). Therefore, the voltage drop of V_{DS_GaN} is also larger than the ideal case. At t_2, i_{Lp} reaches 0A, and V_{DS_GaN} reaches the valley point.

$$\begin{cases} C_{GD_GaN} \cdot \frac{dV_{DS}}{dt} = i_{LP} \\ V_{in} - L_P \cdot \frac{di_{LP}}{dt} - i_{LP} \cdot R_L = V_{DS} \end{cases} \tag{2.11}$$

$$V_{DS_GaN} = V_{GD_GaN} - \left|V_{TH_GaN}\right| = V_{DS} - \left|V_{TH_GaN}\right| \tag{2.12}$$

[t_2-t_3]: After t_2, the next oscillation period starts. The values of V_{DS_Si}, V_{DS_GaN} and i_{Lp} at t_2 become the initial conditions of the next oscillation cycle. It should be noted that the initial condition of V_{DS_GaN} is lower than the ideal case. V_{DS_Si} reaches avalanche at t_3, and the charge stored in C_{DS_GaN} during this period is ΔQ, which is the same as the charge removed during t_0 to t_1.

[t_3-t_4]: V_{DS_Si} stays in the avalanche region and V_{DS_GaN} continues to increase until it reaches the peak value V_{peak2}. V_{peak2} should be larger than V_{peak} due to the initial conditions. Similarly, the resonant current is also greater than in the ideal case.

[t_4-t_5]: This stage is similar to stage [t_0-t_1]. V_{DS_Si} and V_{DS_GaN} decrease simultaneously, and V_{DS_Si} reaches V_{TH_GaN} when ΔQ is removed by resonant current at t_5. GaN is internally turned on earlier than in stage [t_0-t_1] since V_{peak2} is higher than V_{peak}. This allows more resonant current to discharge C_{GD_GaN} in the next stage, and therefore V_{DS_GaN} drops to an even lower value. As a result, in the following oscillation periods, the GaN is internally turned on in every cycle and each turn-on instant is earlier than in the previous cycle. The ringing amplitudes of V_{DS_GaN} and i_{Lp} increase with each cycle, and the oscillation eventually becomes divergent.

Divergent oscillation is fatal to cascode GaN devices and it limits the high current capability of cascode GaN devices.

2.3.5 Proposed Solution: Better Package and Charge Balance

The two key factors to the four issues mentioned above are package parasitic inductance and the capacitance mismatch between the Si MOSFET and GaN in the cascode configuration. The stack die package is proposed to minimize the inter-connection

parasitics and avoid the gate breakdown. The experimental waveforms are shown in Figure 2.30. The stack die package is referred to Figure 2.17(b). The waveform clearly shows that V_{GS_GaN} is clamped to -30V, which is the avalanche voltage of Si MOSFET. It protects the GaN gate whose breakdown voltage is -35V.

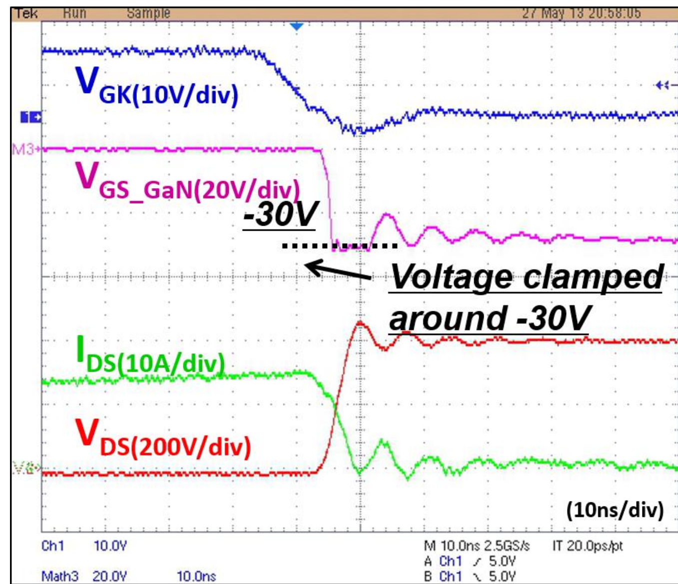


Figure 2.30 GaN gate voltage spike elimination with stack-die package

The most straightforward method to prevent the Si MOSFET from reaching avalanche is to select an appropriate Si MOSFET with a larger junction capacitance according to the junction capacitance of the GaN switch. However, the total gate charge of the Si MOSFET will also increase, which will increase the driving loss significantly at high frequency. Moreover, the increase of C_{GD_Si} will elongate the Si MOSFET turn-off transition and increase switching loss due to a strong miller effect. Therefore, changing Si MOSFET is not the most effective solution.

Based on aforementioned analysis, the total mismatch charge in the cascode device is Q_{III}. Therefore, an additional capacitance C_X is added in parallel with the drain-source

terminals of the Si MOSFET to compensate the charge mismatch, as shown in Figure 2.31. The required minimum value of C_X should guarantee that C_{DS_GaN} achieves its steady-state voltage before the Si MOSFET reaches avalanche. Therefore, the expression of C_X is as follows:

$$C_X \geq \frac{Q_{III}}{V_{av} - V_{TH_GaN}} \tag{2.13}$$

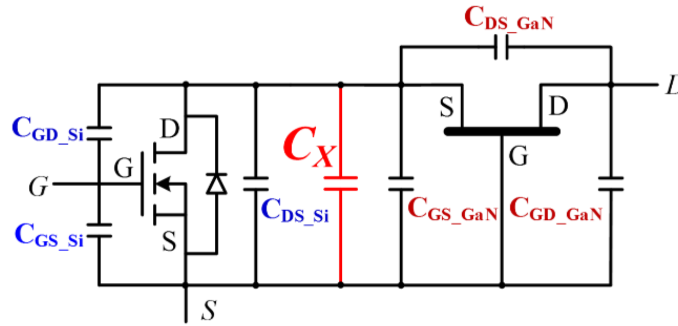


Figure 2.31 Adding an extra capacitor in cascode GaN devices

Paralleling C_X between the drain-source terminals of the Si MOSFET will not increase its driving loss, and the turn off loss is still very small due to the merit of the cascode structure, as mentioned in section 2.1.3. The impact of an extra capacitor on the turn-off loss is shown in Figure 2.32 which is derived from simulation. The cascode GaN used in the simulation is same with the one used in the experiment shown later on. The GaN device rating is 600V/12A and the Si MOSFET rating is 30V/11A. The mismatch charge is around 10.5nC. The turn off current is 10A and turn off steady-state voltage is 380V in the simulation. The data indicates a little increase in turn off loss due to this extra capacitor.

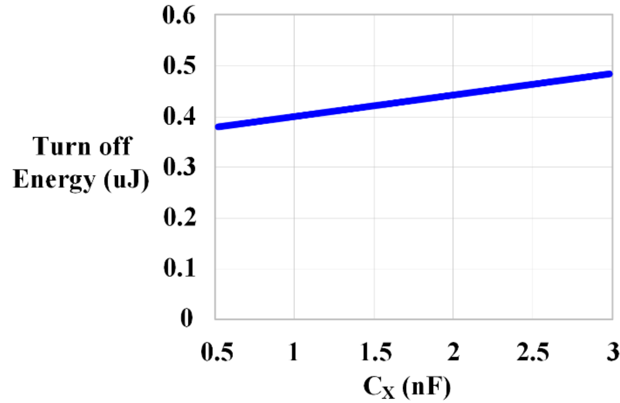


Figure 2.32 Impact of an extra capacitor on turn-off switching loss

The proposed solution is a simple and effective way to compensate the mismatch charge of the Si MOSFET and the GaN switch, and it is convenient for mass production. It is noticed that the aforementioned issues may not occur at low voltage condition, such as below 200V application. The proposed solution may slow down the device switching speed, but with very limited increase of turn off switching loss.

To easily integrate an extra capacitor into the cascode device, a chip-on-chip package is fabricated, as shown in Figure 2.33. The 600V normally-on GaN chip is provided by Transphorm Inc. The threshold voltage is around -15V and the maximum source-gate voltage is around -35V. Therefore a 30V Si MOSFET is selected to control the on/off state of the GaN as well as to protect the GaN gate by clamping the source-gate voltage of the GaN to the avalanche value of the Si MOSFET, which is 30V. Another criterion for choosing the Si MOSFET is to minimize the driving loss at high frequency. Therefore the junction capacitance of this 30V Si MOSFET is usually small, and the charge of the GaN and the Si MOSFET are mismatched. The estimated mismatch charge is about 10nC, and therefore, an 800pF capacitor is added according to (2.9). The comparisons of the behavior of cascode GaN device in a CRM boost converter with and without an extra capacitor

during the turn-on and turn-off transition are shown in Figure 2.34 and Figure 2.35.

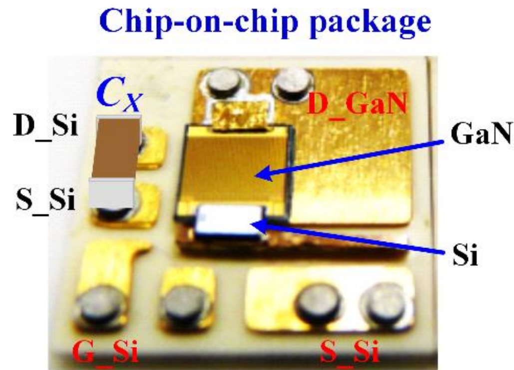
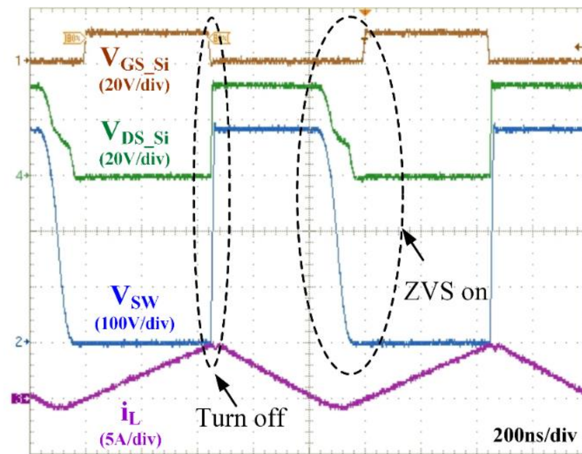
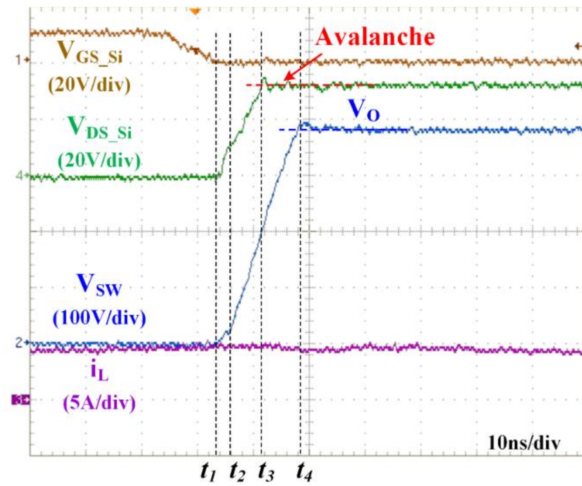
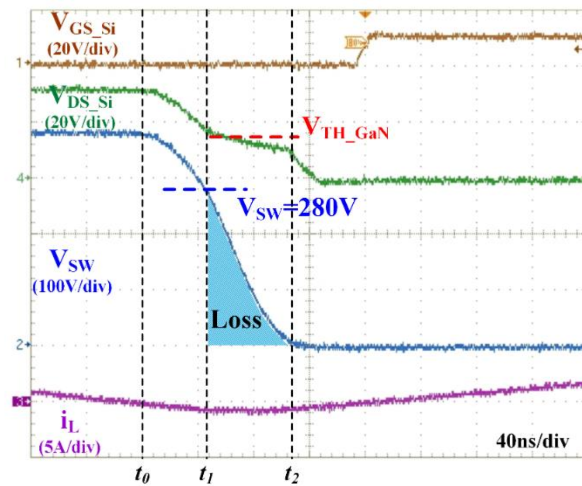


Figure 2.33 Chip-on-chip package for cascode GaN device with an extra capacitor



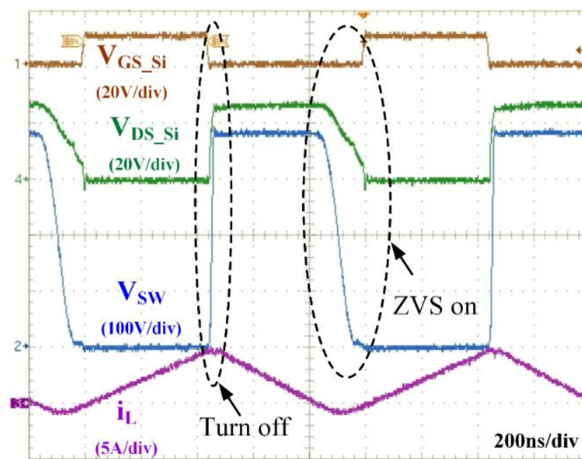
(a) Steady-state waveforms



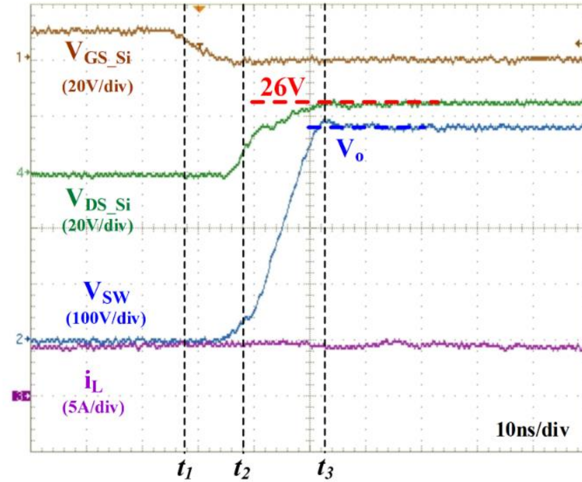


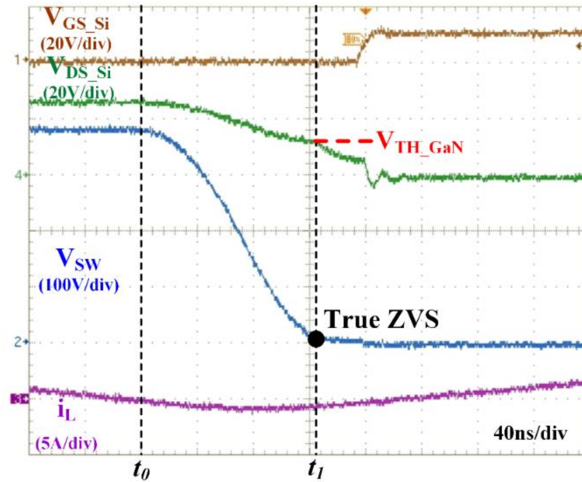
(b) Detailed turn off transition (c) Detailed turn-on transition

Figure 2.34 Experimental waveforms without external capacitor



(a) steady-state waveforms





(b) Detailed turn-off transition (c) Detailed ZVS turn-on transition

Figure 2.35 Experimental waveform with external capacitor

Figure 2.34 shows the experimental waveform without adding the extra capacitor. Figure 2.34(b) and Figure 2.34(c) show the detailed turn off and ZVS turn on transition, respectively. V_{SW} is the terminal voltage across the cascode GaN device. During the turn-off transition, V_{DS}_Si reaches avalanche at t_3, while the terminal voltage V_{SW} only rises to 170V. After t_3, C_{DS_GaN} is continuously charged through the avalanched path until V_{SW} reaches V_O at time t_4. The mismatch charge is about 10.5nC in this cascode GaN device.

According to (2.2), the avalanche loss P_{av} is 0.315W at 1MHz. This part of the loss is considerable at high frequency.

During the ZVS turn-on transition, V_{DS_Si} decreases to V_{TH_GaN} at t_1, while the terminal voltage only drops to around 280V. The remaining energy stored in C_{DS_GaN} is dissipated through the GaN channel. The internal non-ZVS loss is estimated to be about 1.2W at 1MHZ. Therefore, the total power loss caused by junction capacitor mismatch in this cascode GaN device is about 1.5W at 1MHz.

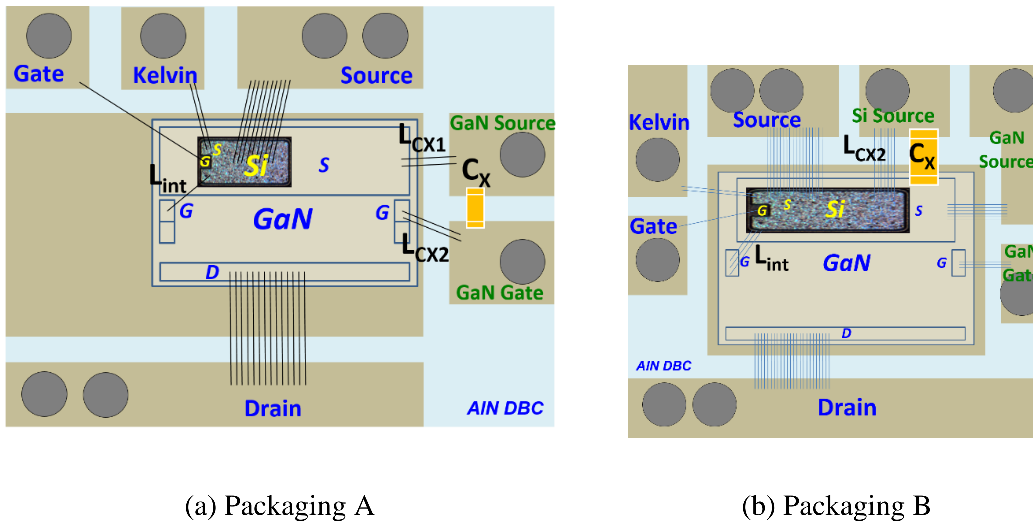
Figure 2.35 shows the experimental waveform with the extra capacitor. Figure 2.35(b) and Figure 2.35(c) show the detailed turn-off and ZVS turn-on transition, respectively. Figure 2.35(b) shows that V_{DS_Si} rises to 26V when the terminal voltage reaches steady state condition. Therefore, adding this capacitor can effectively avoid Si MOSFET reaching avalanche. Figure 2.35(c) shows that the terminal voltage drops to nearly zero when V_{DS_Si} drops to V_{TH_GaN}. Therefore, real ZVS can be achieved for the cascode GaN device by adding this capacitor.

It is worthwhile to point out that the extra capacitor does not impact the driving loss based on the loss measured from the driving circuit. Moreover, the total loss reduction of the prototype with the extra capacitor is about 1.5W at 1MHz, which can match with the estimated loss induced by avalanche and internal non-ZVS issues. The loss reduction also indicates that the increase in turn off loss due to the extra capacitor is negligible.

One way to avoid the divergent oscillation is to parallel RC snubber circuit to suppress the voltage spike and damp the parasitic ringing which is a common practice for devices switching at high current. However, the power dissipation on the RC snubber circuit is

around over few uJ which is not acceptable for the switching frequency above few hundreds of kHz.

A fundamental solution to compensate the capacitance mismatch should be adding an additional capacitor C_X. Ideally, V_{SG_GaN} is equal to V_{CX} as well as V_{DS_Si} after capacitance compensation. However, integrating C_X in the cascode package always creates parasitic inductance which induces parasitic ringing internally. The parasitic inductance and the position of C_X are critical to achieve optimal performance. Figure 2.36 shows two possible packaging diagram which integrating the capacitor C_X.

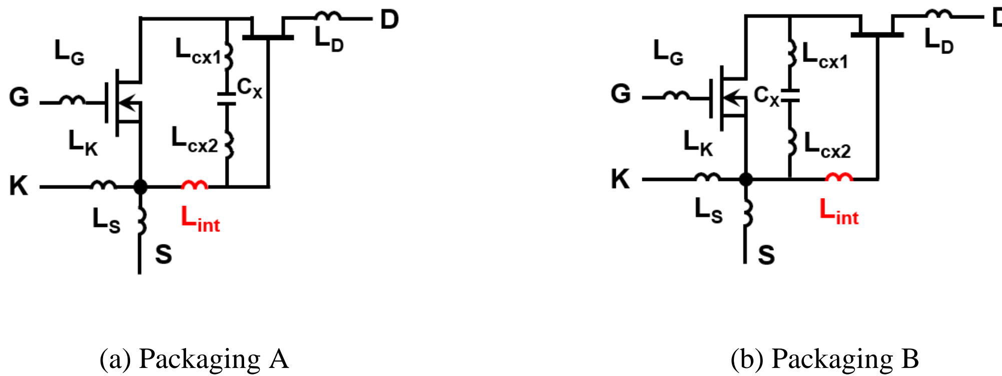


(a) Packaging A (b) Packaging B

Figure 2.36 Two possible packaging approach with C_X

The Si MOSFET is on top of GaN switch source pad in order to reduce inter-connect parasitic inductance. The C_X is on side of GaN switch in packaging A and on top of GaN switch source pad in packaging B, respectively. As shown in the diagram of packaging A, one terminal of the external capacitor C_X is connected to GaN source pad through L_{CX1}. The other terminal is connected to one of the GaN switch gate pad through wire bonding, and then connected to the source pad of Si MOSFET through the other gate pad of GaN

switch for easy wire bonding consideration. L_{CX2} is consisted of two parts; one is the wire between C_X and gate pad, and the other is the two gate connection inside the GaN switch. Actually the packaging A is used to demonstrate the benefits of the proposed solution in literature. In packaging B, one terminal of C_X is connected directly to the source pad of GaN switch, and the other terminal is connected to the source pad of Si MOSFET through L_{CX2}. The equivalent circuit considering the parasitic inductance is shown in Figure 2.37. The parasitic inductance of these two packaging approaches are listed in Table 2.3 which are derived based on Ansoft Q3D FEA simulation. It shows that packaging B has smaller parasitic inductance.



(a) Packaging A (b) Packaging B

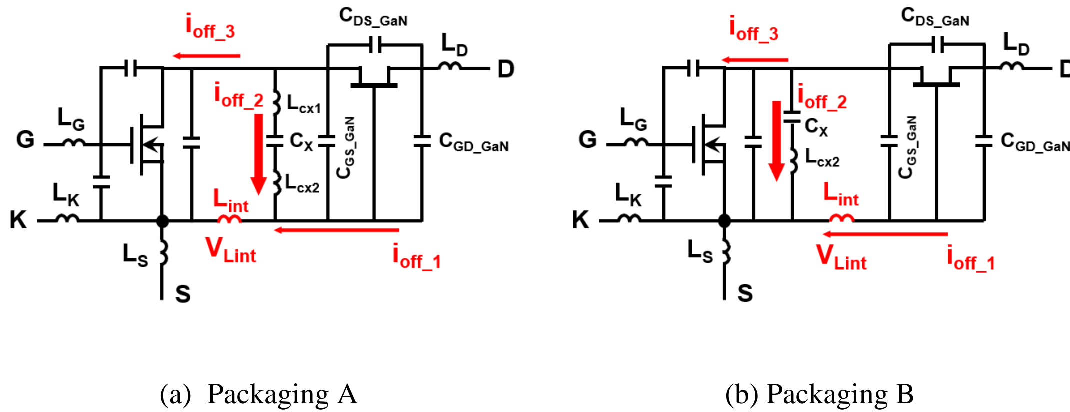
Figure 2.37 Equivalent circuit of two different packaging approaches

Table 2.3 Parasitic inductance of different packaging

	Packaging A	Packaging B
L_{int}	1.0nH	1.0nH
L_{CX1}	1.0nH	N/A
L_{CX2}	2.1nH	1.0nH

It is noticed that V_{SG_GaN} is the sum of V_{DS_Si} and V_{Lint} which is the voltage across L_{int}. Therefore, the parasitic ringing on V_{SG_GaN} can be significantly reduced by minimizing

V_{Lint}. The amplitude of V_{Lint} is determined by the current flowing through L_{int}. The two packages put C_X in different positions and therefore result in different current flowing through the L_{int}. In packaging A, C_X is on the right side of L_{int}. During turn-off transition, i_{off_1} and i_{off_2} flow through L_{int} which is shown in Figure 2.38(a). i_{off_1} is the turn-off current flowing through C_{GD_GaN} and C_{GS_GaN}. i_{off_2} is the current charging C_X,. i_{off_3} is the current flowing through Si MOSFET branch. The amplitudes of three current are determined by impedance. C_X value is typically much larger than any other junction capacitance, therefore, i_{off_2} is much higher than i_{off_3}. It is worthwhile to point out that C_{DS_GaN} is typically much larger than C_{GD_GaN} at high voltage range due to the nonlinear characteristic of GaN junction capacitances. As a result, i_{off_2} is also much larger than i_{off_1}. In packaging B, C_X is on the left side of L_{int}. Only i_{off_1} flows through L_{int} during turn-off period, while i_{off_2} directly flow to the source of Si MOSFET. Equivalent circuit is shown in Figure 2.38(b). It is obvious that packaging B reduces the current flowing through L_{int} which induces less voltage drop V_{Lint}.



(a) Packaging A (b) Packaging B

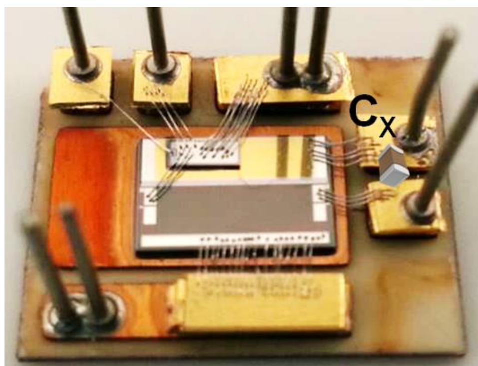
Figure 2.38 Current distribution in different packages

Moreover, smaller parasitic inductance also helps to reduce the current flowing through L_{int}. As mentioned above, the current distributions of i_{off_1}, i_{off_2} and i_{off_3} are

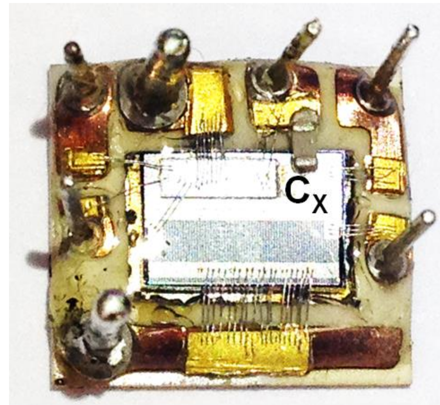
determined by impedance. In packaging B approach, minimizing C_X and L_{CX2} branch impedance increases i_{off_2} and reduces i_{off_1}. As a result, V_{Lint} is further reduced by inductance reduction.

Overall, packaging B bypasses the majority of turn-off current by good position and small parasitic inductance. Smaller V_{Lint} results in smaller resonant amplitude in the GaN gate loop, and as a result, V_{GS_GaN} is far from turn-on threshold value which is the trigger of divergent oscillation. Packaging B approach is preferred for cascode GaN operating at high current turn-off condition.

To validate the analysis of divergent oscillation and the proposed solution for cascode GaN device, two cascode GaN devices are fabricated with the two packaging diagram mentioned above, as shown in Figure 2.39. The 600V normally-on GaN switch with 35A continuous current capability is provided by Transphorm Inc. The threshold voltage is around -20V and the maximum source-gate voltage is around -40V. Therefore a 30V Si MOSFET is selected to control the on/off state of the GaN.



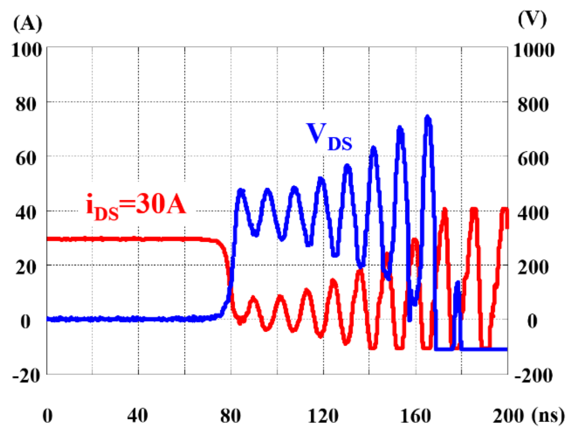
(a)Packaging A



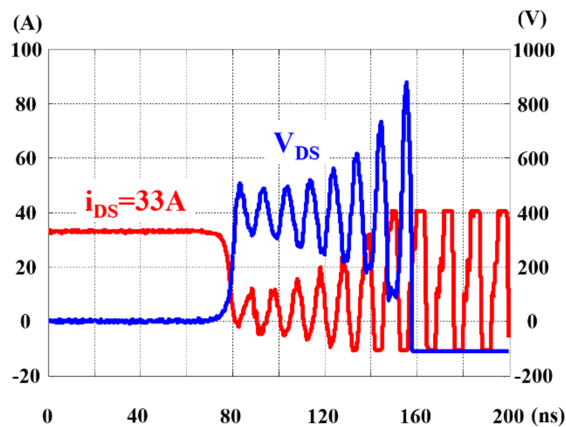
(b)Packaging B

Figure 2.39 Prototypes of two different packaging approaches

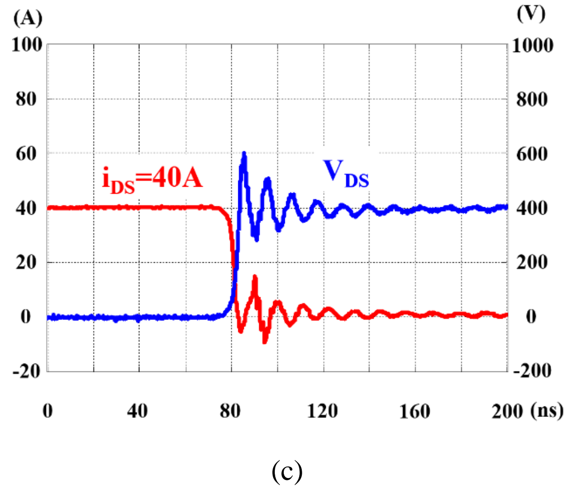
The evaluation of high current turn-off condition is carried on double-pulse-test circuit. Input voltage is 400V. Figure 2.40 shows the experimental waveforms of different packaging approaches. Figure 2.40(a) shows that the packaging A and B without C_X occurs divergent oscillation at 30A turn-off condition. The packaging A with C_X can switch to slightly higher turn-off current, but it still occurs divergent oscillation at 33A turn-off condition as shown in Figure 2.40(b). The major reason is the position of C_X as mentioned in section III. The prototype using packaging B approach can successfully switch under 40A turn-off condition without oscillation as shown in Figure 2.40(c).



(a)



(b)



(c)

Figure 2.40 Experimental results with different packaging approaches (a) Packag-ing A and B without C_X (b) Packaging A with C_X (c) Packaging B with C_X

It is noticed that the voltage spike is close to 600V due to relatively large power loop inductance in order to accommodate the shunt resistance (SSDN-10, T&M Research Products Inc.) on the PCB board. The turn-off current can go up to 48A by removing the shunt resistance as shown in Figure 2.41. The red curve is the inductor current. The parasitic ringing period reduces from 12ns to 8.5ns based on Figure 2.40(c) and Figure 2.41. It indicates about 50% reduction in the power loop inductance by removing the shunt resistance. The voltage spike is about 570V.

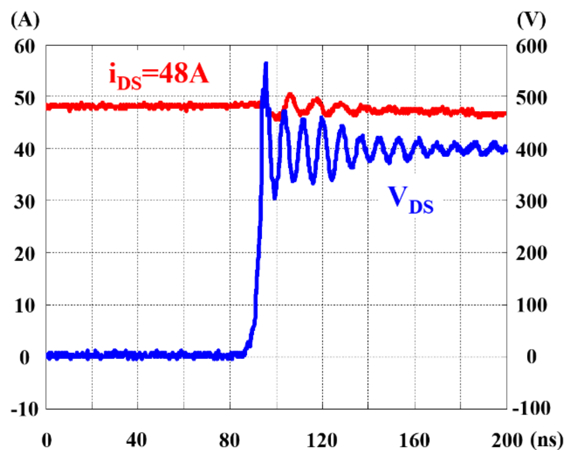


Figure 2.41 Experiment with packaging B, without shunt resistance

In order to further reduce the power loop inductance, a half-bridge module is fabricated, as shown in Figure 2.42. The loop inductance reduces about 50% compared to the one with two discrete devices. The devices are capable to switch at 54A turn-off current, as shown in Figure 2.43. The proposed solution of adding C_X at right position can significantly extend the high turn-off current capability.

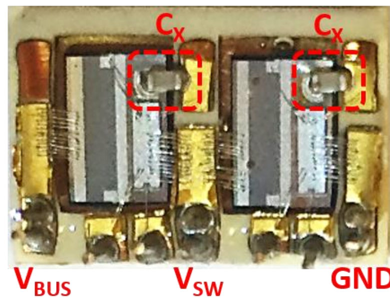


Figure 2.42 Half bridge module of cascode GaN devices with packaging B approach

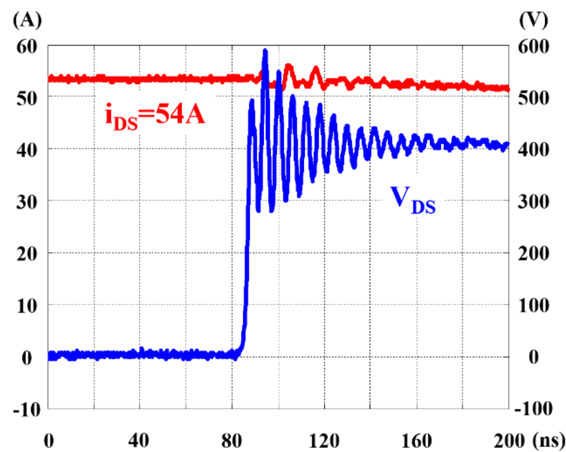


Figure 2.43 Experiment with half bridge module of cascode GaN devices with packaging B approach

2.4 Conclusion

This chapter presents the switching characteristics of 600V GaN devices. The switching loss mechanism of cascode GaN are analyzed in detail. Packaging becomes critical due to high switching speed of GaN devices. Some issues related to cascode GaN devices are discussed in detail, including Si avalanche, GaN internal switching loss GaN gate breakdown, and divergent oscillation. The fundamental reason for the issues are packaging parasitic and mismatched capacitance. The proposed package integrating the external capacitor can solve all the problems and therefore improves the cascode GaN device significantly.

Chapter 3. Design Considerations for GaN Devices

The GaN devices parameters are so superb and it may lead an illusion to circuit designer that the circuit performance can be significantly improved by simply plugging and replacing Si MOSFET. It is has been reported that small gain can be achieved with simple replacement [C.1]-[C.6]. However, researchers found out that the circuit performance may be worse or even not work with GaN devices without deeply understanding the technical challenges raised by GaN [C.7]. This chapter will discuss the design consideration for GaN devices including the comparison of hard-switching and soft-switching, high frequency gate drive with high di/dt and dv/dt immunity.

3.1 Soft-switching or hard-switching

It is no doubt that the switching performance of GaN devices are much better than Si MOSFET and GaN devices enable half-bridge based topology operating under hard-switching condition, such as totem-pole PFC [C.8] - [C.10]. It is noticed that reference [C.8] and [C.9] are provided by GaN device manufacturers, and the system operation frequency is below 100kHz. However, it is questionable that hard-switching is preferred for GaN devices from loss and noise perspective. Figure 3.1 shows the hard-switching waveforms of a 600V GaN device with surface mount package which is considered with minimal parasitic inductance. The drain-source voltage and current contains severe high frequency (>100MHz) ringing and overlaps with each other for a long period (>10ns) which generates huge loss. The high frequency ringing is also observed at the device gate which majorly couples through the gate-drain capacitance. In order to avoid false trigger issue,

the devices switching speed has to be slowed down significantly, usually by enlarging the gate resistance, as shown in Figure 3.2.

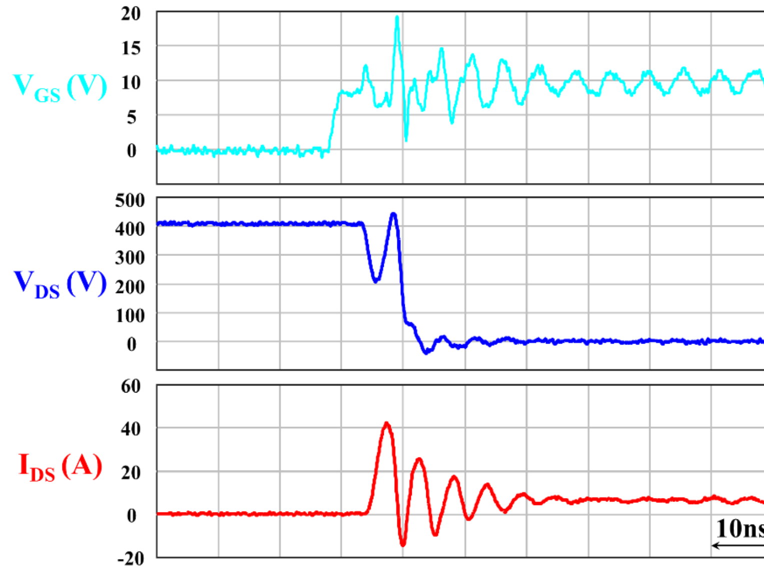


Figure 3.1 Hard-switching turn-on transient of GaN device with severe parasitic ringing

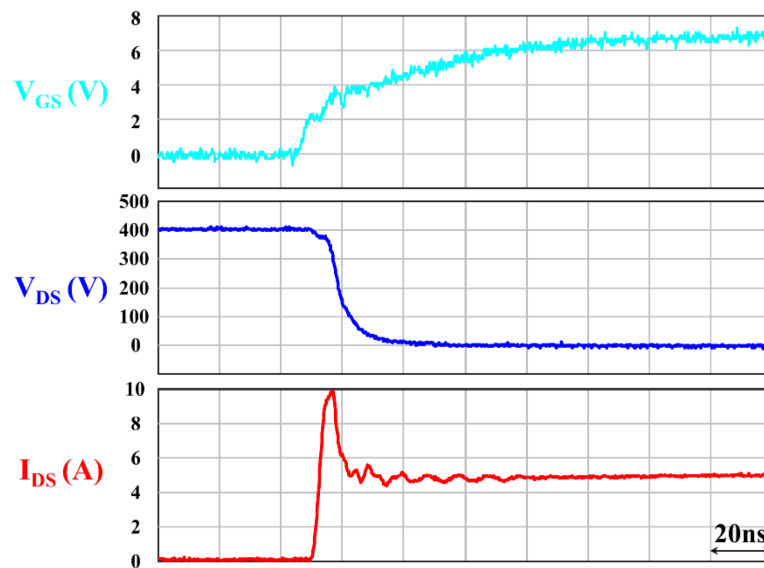


Figure 3.2 Hard-switching turn-on transient of GaN device with less parasitic ringing by slowing down switching speed

It clearly shows that the slew rate of drain-source voltage is much reduced and only current has a single overshoot due to junction capacitor charge of the free-wheeling switch. The gate voltage rises to steady-state value gradually without disturbance. However, the transition time increases from 10ns to 30ns and the switching energy loss increases more than twice of the one shown in Figure 3.1. The relationship between the turn-on switching loss and switching speed, which is actually controlled by gate resistance, is shown in Figure 3.3. No matter what is the value of gate resistance, the turn-on switching energy is way above 20uJ, which is 10W switching loss at 500kHz operation.

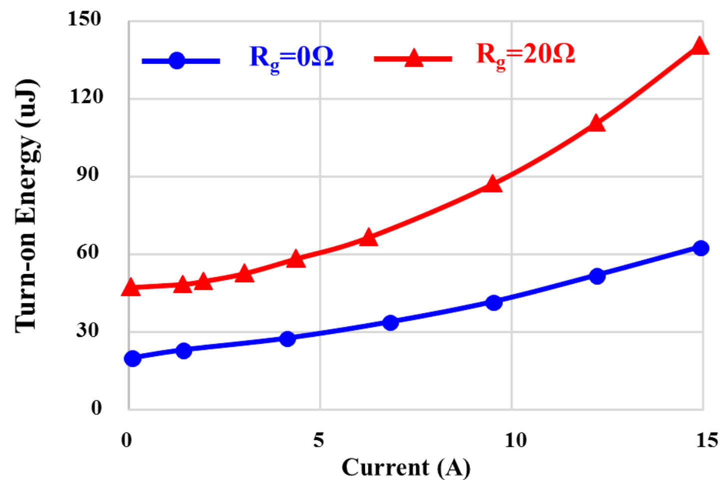


Figure 3.3 Hard-switching turn-on energy vs. R_g

It is obvious that hard-switching turn-on cannot achieve both lower loss and less noise simultaneously. On the other hand, soft-switching turn-on can gain both with minor penalty of increased conduction loss. For PWM converter, critical current mode (CRM) operation is the most simple and effective way to achieve zero-voltage-switching (ZVS) turn-on and is widely used in medium-low power applications.

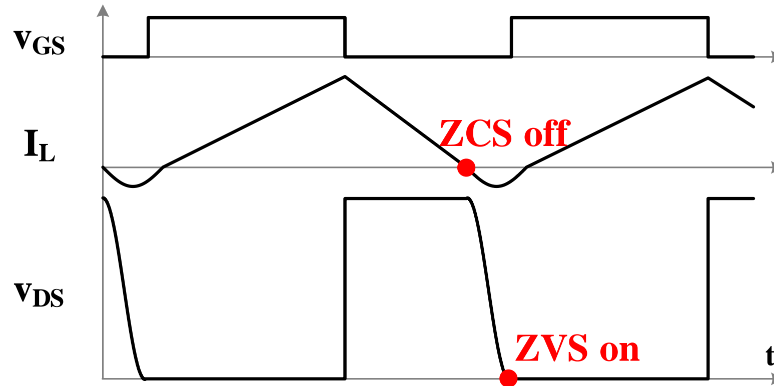


Figure 3.4 CRM operation principle

As shown in Figure 3.4, the CRM could achieve ZVS turn-on for the control switch and zero-current-switching (ZCS) turn-off for the free-wheeling switch. The disadvantage of the CRM operation is that the peak inductor current is more than twice of the load current, this may increase the turn-off switching loss and the conduction loss of devices and inductor. However, the turn-off switching loss of GaN devices are extremely small, as demonstrated in Figure 2.11, typically lower than few uJ. Moreover, the root-mean-square (rms) value of a triangular waveform current is only 15% higher than a pure DC current with same DC value based on mathematical results. That means the maximum increase of conduction loss with CRM operation is 33%. Therefore, CRM operation can be easily justified in the applications that the saved switching loss is much higher than the increased conduction loss plus turn-off switching loss.

Figure 3.5 shows the comparison of the efficiency of hard-switching and CRM soft-switching 400V/200V GaN based buck converter. The switching frequency at 6A output is designed to be 500 kHz. It clearly shows that CRM soft-switching achieves 1% higher efficiency over all load range. The loss breakdown at 6A output is shown in Figure 3.6. The highest loss bar is completely eliminated by soft-switching. The conduction loss and

the turn-off switching loss only increases a little bit as predicted above. The experimental results indicates that soft-switching benefits GaN devices significantly.

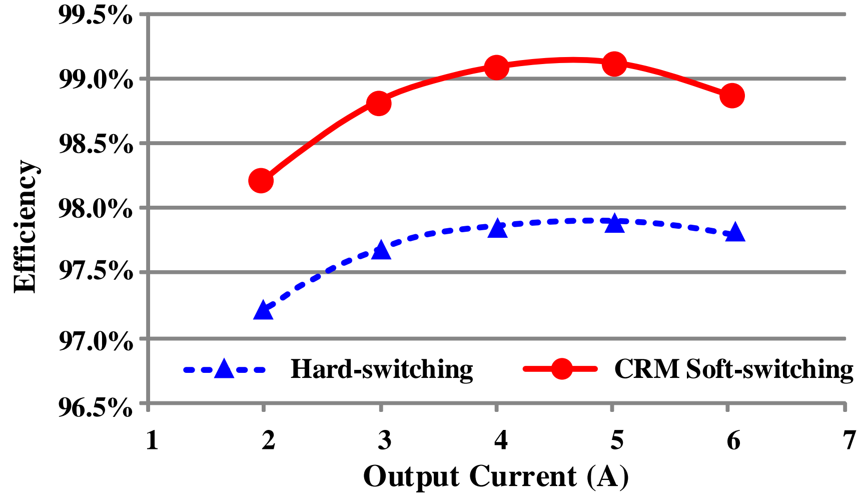


Figure 3.5 Hard-switching vs. CRM soft-switching

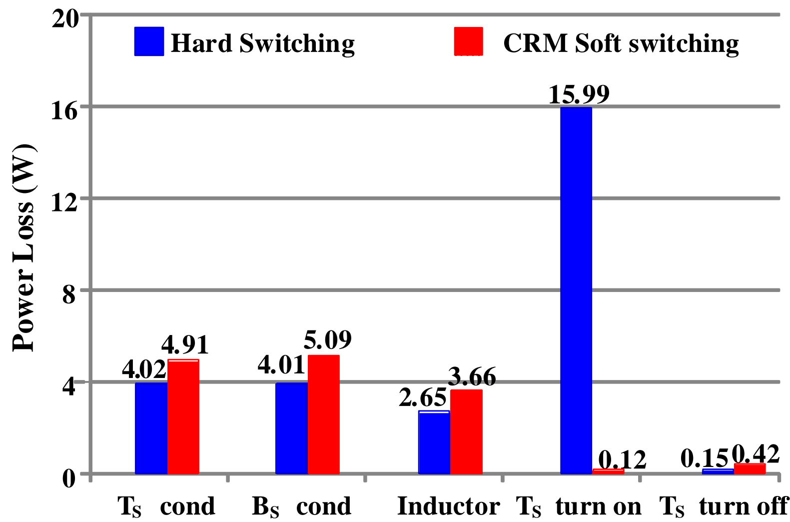


Figure 3.6 Loss breakdown at 6A

A fully functional GaN-based 6kW bidirectional buck/boost converter operating at CRM mode with 1MHz and above switching frequency are built for energy storage systems. The simplified system structure is shown in Figure 3.7.

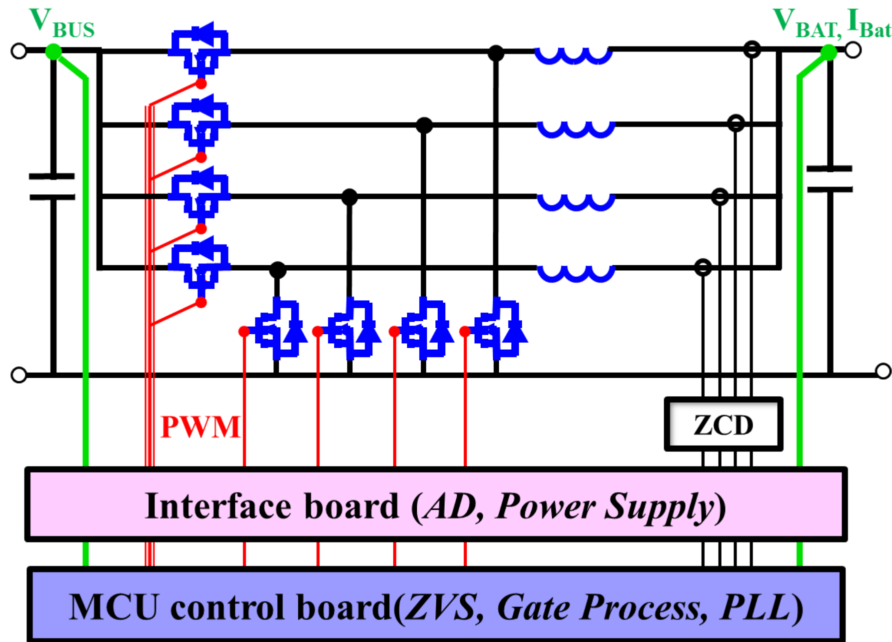
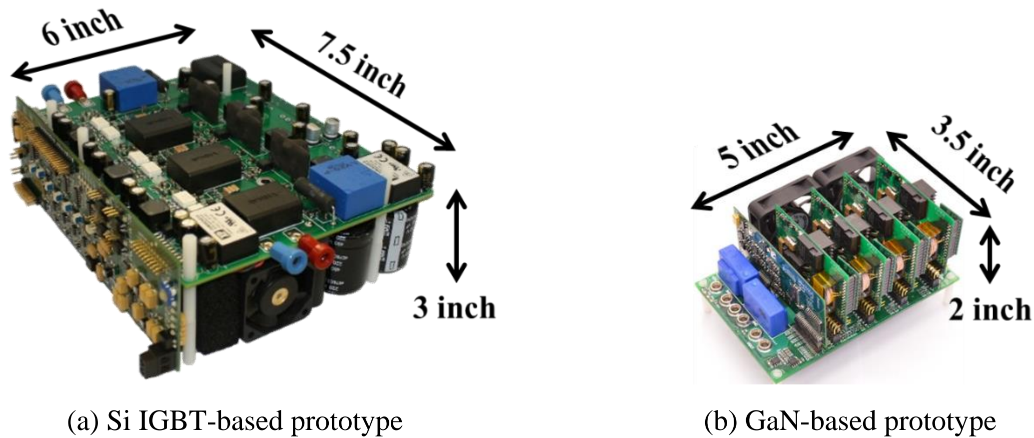


Figure 3.7 4-phase bidirectional buck/boost converter for energy storage system

As a point of efficiency and density comparison, a Si IGBT based prototype, which operates at 20kHz switching frequency is shown in [C.11]. Both prototypes can achieve 99% efficiency, while GaN-based prototype can achieve much higher power density. The power density is 170W/in^3, which is at least 4 times higher than the Si IGBT based solution. Most of the space is occupied by electrical fan and signal sensor, such as bulky voltage hall sensor, which can not be shrunk by pushing frequency.



(a) Si IGBT-based prototype (b) GaN-based prototype

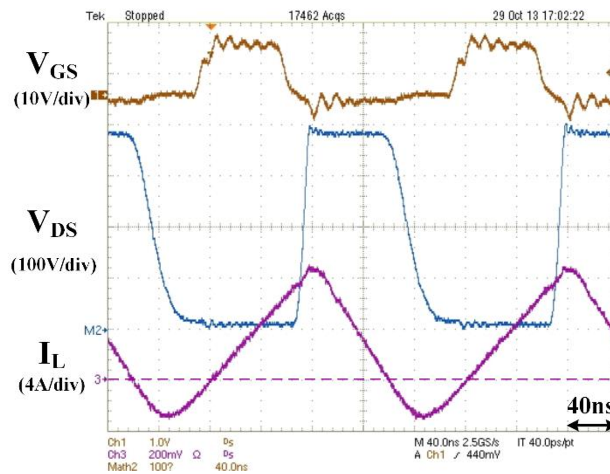
Figure 3.8 Comparison of GaN-based prototype and Si IGBT-based prototype

The soft-switching characteristic of the bidirectional buck/boost converter can be further enhanced by coupling the inductors in an inverse manner [C.12]. The inverse coupled inductor extends the ZVS region and reduces circulating energy, which is highly preferred at high frequency operation. The gain of efficiency at 1MHz condition is around 0.3%. Moreover, the coupled inductor saves 50% footprint and 25% volume compared with two non-coupled inductors The details of the impact of inverse coupled inductor on the high frequency converter are illustrated in the Appendix II.

In order to further improve the power density of the bidirectional converter, the switching frequency is the key catalyst. The conventional through hole packaged GaN device generates significant loss at higher frequency due to package related parasitics. The stack-die packaged cascode GaN device is employed and is able to operate at 5MHz switching frequency, as shown in Figure 3.9. The drain-source voltage decreases to zero due to the natural resonance formed by the inductor and junction capacitor. The converter can achieve 98% efficiency and 1000 W/in^3 power density at 600W output conditions. The loss breakdown at 600W output condition is shown in Figure 3.10. The largest share of the

loss part is the inductor winding loss, which occurs due to the skin effect and fringe effect, and can be measured using Mu's method described in [C.13].

(a) Prototype of 5 MHz converter with stack-die packaged cascode GaN switch



(b) Experiment waveforms

Figure 3.9 5 MHz converter with the cascode GaN switch

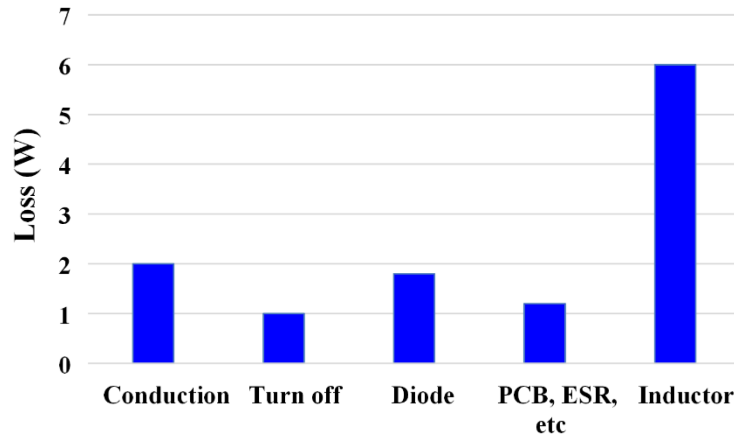


Figure 3.10 Loss breakdown of 5 MHz CRM boost converter with cascode GaN device

3.2 High Frequency Gate Drive

One of the advantage of GaN devices over Si MOSFET is lower turn-off switching loss as shown in Figure 2.12 and it is achieved by higher switching speed capability. With better device parameter and packaging, the external gate drive circuit is crucial to achieve high switching speed. Since ZVS turn-on is preferred for all GaN devices to eliminate huge turn-on loss, the gate drive circuit design should be more focused on turn-off transition.

The gate resistance plays an important role in the GaN devices turn-off switching loss, especially for e-mode GaN devices. The gate resistance limits the gate discharging current and therefore slow down the drain-source voltage and current transition as shown in Figure 3.11. As a result, the turn-off energy reduces significantly with 0Ω gate resistance as shown in Figure 3.12.

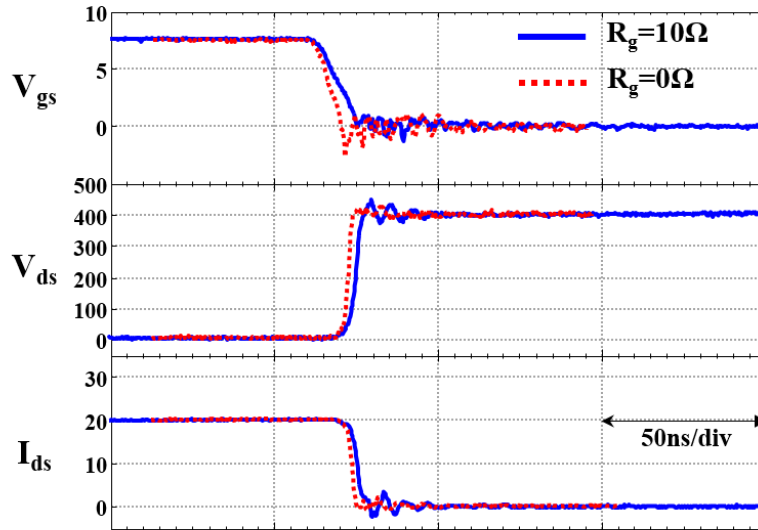


Figure 3.11 Turn-off transition with different gate resistance

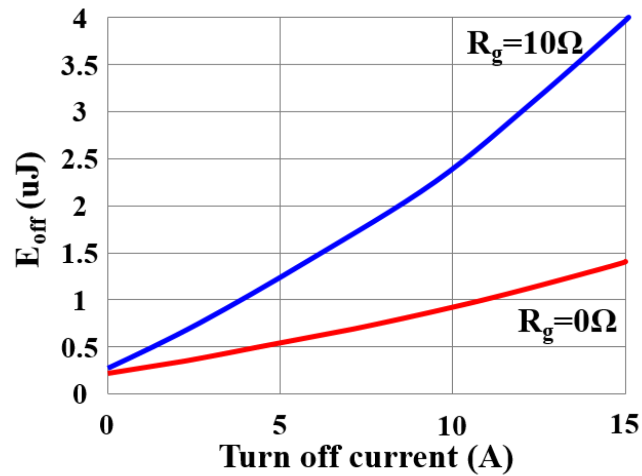


Figure 3.12 Turn-off energy with different gate resistance

It should be mentioned that the external gate resistor is less effective in a cascode GaN since the GaN actually is controlled by internal Si MOSFET. A resistor can be integrated into the package, which is connected between the GaN gate and Si source, to control the switching speed of a cascode GaN device.

In general, small R_g is preferred to reduce the turn-off switching loss. Some undershoot on the gate is allowed by most of GaN devices. However, special care should be taken to avoid the subsequent positive gate voltage ringing beyond de gate threshold of the device. Therefore, the gate driving loop inductance should be designed as low as possible.

By using a GaN device in MHz applications, especially when critical conduction mode (CRM) is used to achieve soft-switching, high-current turn-off can induce high dv/dt and di/dt issues. As illustrated in Figure 3.13, the dv/dt and di/dt of GaN based converter is 3~6 times higher than Si based converter. It is obvious that higher di/dt and dv/dt bring new challenge to the gate drive design.

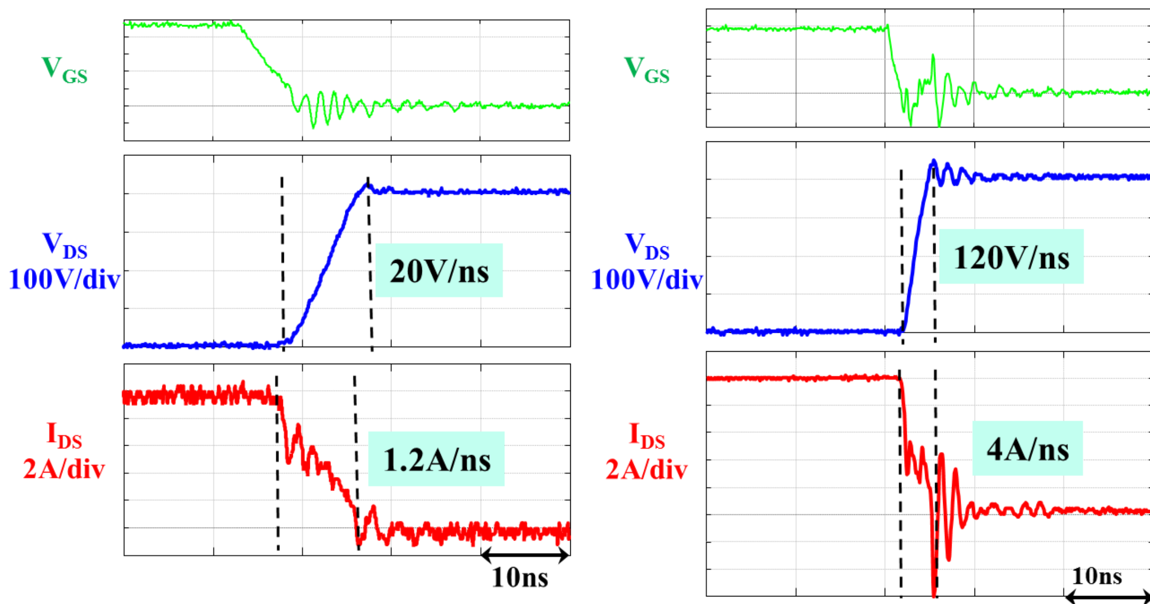


Figure 3.13 High dv/dt and di/dt induced by GaN devices: (a) Si MOSFET, (b) GaN switch

3.2.1 The di/dt Issue and Solutions

When the GaN switch is turned off, the falling di/dt slope induces negative voltage on the CSI. This negative voltage will induce an opposing voltage across the gate-source of the GaN, which is intended to turn on the device. Figure 3.14 shows an example of a buck

converter with cascode GaN switches in TO220 package. The total common source inductance L_S consists of the common-source inductance in the device package and the parasitic inductance of the PCB trace. When the high side switch is turned off, the high di/dt will induce inverse voltage on L_S. A 5V spike appears on the terminal of the top switch gate signal, as shown in Figure 3.15. This spike may spur a false turn-on of the device if the internal gate signal reaches its threshold voltage and causes shoot through.

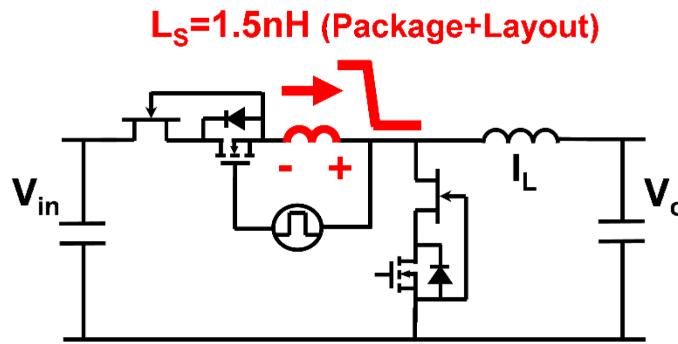


Figure 3.14 di/dt impact on gate drive loop

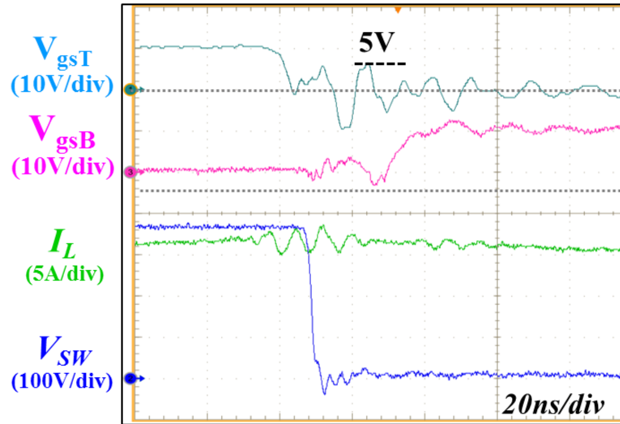


Figure 3.15 High di/dt induces voltage on the gate

The best way to improve the di/dt immunity is to minimize common-source inductance by improving packaging and the PCB layout. Separating the gate and power loops with a

Kelvin connection is helpful to reduce the inductance. The internal source inductance of the GaN device also should be minimized. Figure 3.16 shows the experimental waveforms of the same device but with stack-die package, shown in Figure 2.17(b). The voltage spike is significantly suppressed which is lower than 1V.

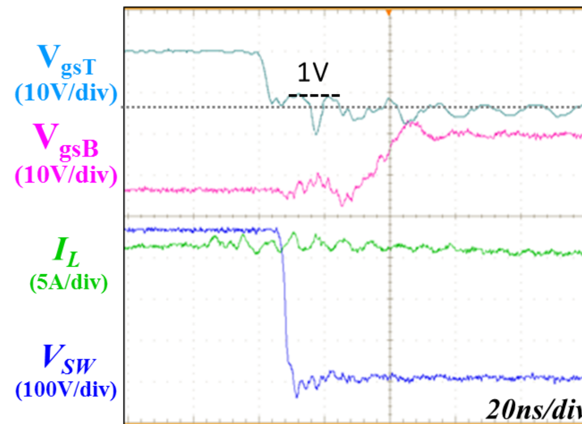


Figure 3.16 Smaller voltage spike with less CSI

3.2.2 The dv/dt Issue (Common mode Noise Current) and Solutions

The dv/dt related driving issue is more complicated and difficult than the di/dt problem. It usually happens to the high side device in a half-bridge configured converter during high positive or negative switch-node dv/dt. Parasitic capacitance of the high side driver is a high-frequency noise path for the common-mode current generated by the switch-node dv/dt. For a positive dv/dt event, the high-voltage slew rate across capacitor C_{IO} generates the common-mode current which flows in the loops, as shown in Figure 3.17. This common-mode current causes ground bounce on the PWM input side and can cause changes in the logic state. For a negative dv/dt event, the common-mode current flows clockwise and can deteriorate the PWM signal, as shown in Figure 3.18. With GaN transistors, the slew rates are likely to be above hundreds of volts per nanosecond. This issue requires immediate

addressed to avoid becoming a limiting factor on the circuit performance. It is common to all GaN devices applications that have a high side floating device.

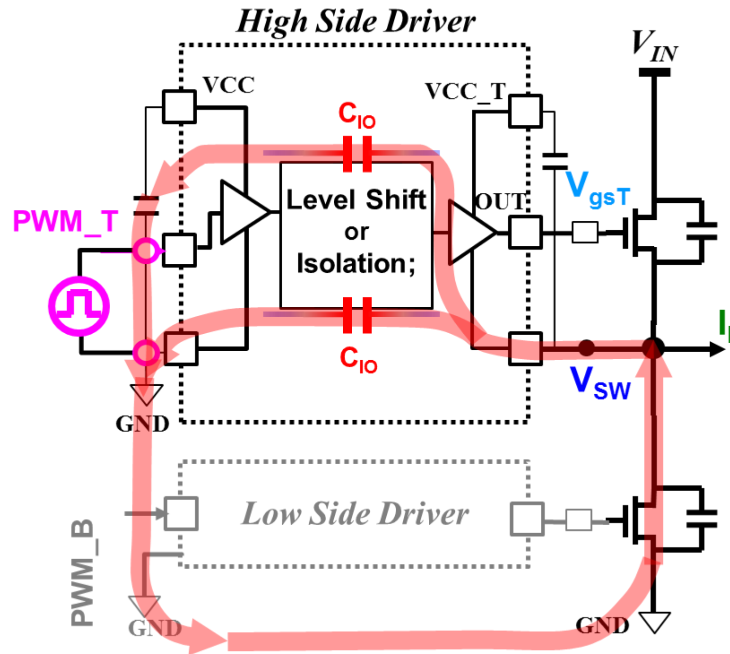


Figure 3.17 High dv/dt causes common-mode current across parasitic capacitance of level shifter or isola-tor (cascode GaN is used as an example)

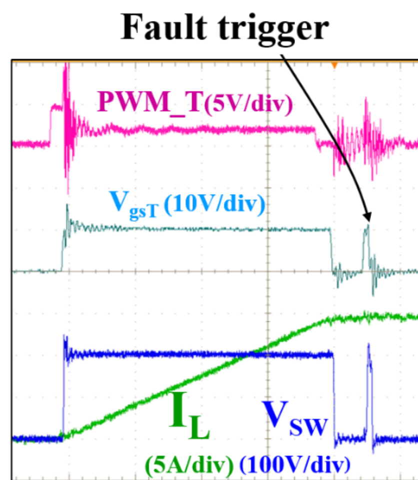


Figure 3.18 High dv/dt deteriorates the PWM signal

In most cases, a level shifter or isolated driver are used for the high side driver, which are summarized in table 3.1. Bootstrap IC has been widely used in Si MOSFET based converter for decades. The dv/dt immunity is high but the propagation delay is too long due to the internal high voltage transistor. It is not suitable for GaN based converter which operates at very high frequency and requires small propagation delay. The commercial driving transformer and optocoupler are easily susceptible to dv/dt noise due to large parasitic capacitance.

Table 3.1 Commercial high side gate driver

	Part #	dv/dt immunity (V/ns)	propagation delay (ns)
Bootstrap IC	NCP5181 [C.14]	100	110
Driving transformer	TLA-3T106 [C.15]	<30	<20
Optocoupler	ACPL-38JT [C.16]	30	150
Inductive digital isolator	Adum1100 [C.17]	>100	15
Capacitive digital isolator	ISO721 [C.18]	>100	17

There are two types of digital isolator based on the primary to secondary coupling mechanism, namely inductive coupling and capacitive coupling. Both of them have very low parasitic capacitance and the dv/dt immunity is higher than 100V/ns. Moreover, the propagation delay is less than 20ns which make it suitable for GaN application.

The power for the high side digital isolator usually comes from an isolated power supply module. However, the isolated power supply is bulky and more importantly susceptible to noise due to relative large capacitance. For instance, the parasitic capacitance of JHM0624S15 from XP power [C.19] which is considered as the state-of-the-art product,

is 20pF. In order to reduce the parasitic capacitance and simplify the power supply for the high side driver, a high voltage bootstrap diode can be used, as shown in Figure 3.19. The junction capacitance is usually lower than 5pF at high voltage, but it is still the major noise current path. In order to lock the noise current in a small loop, it is necessary to put the Vcc decoupling capacitor as close to the bootstrap diode and dv/dt noise source ground as possible. To further improve the dv/dt immunity, a RC filter and a negative bias circuit can be used at the input PWM terminal.

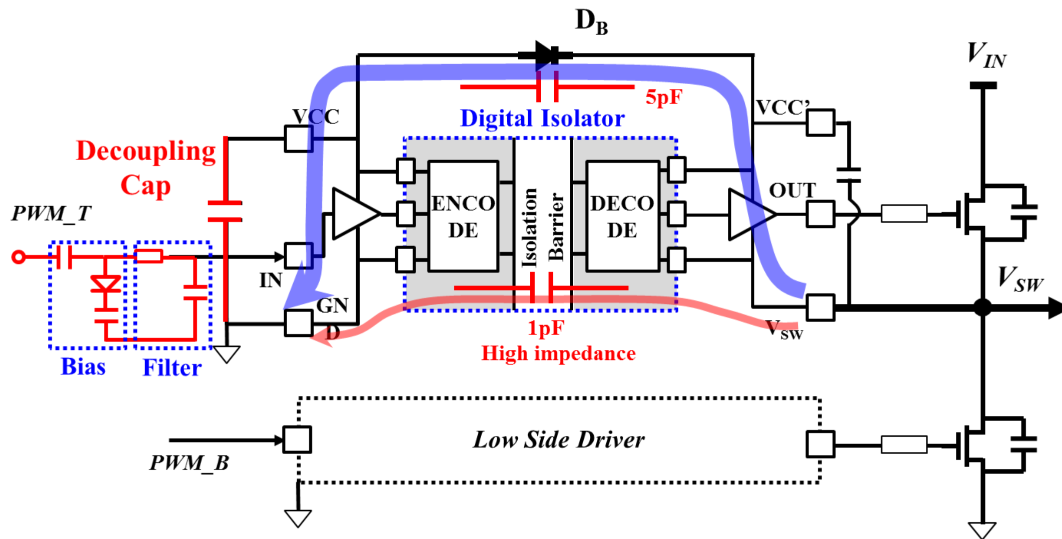


Figure 3.19 Proposed high side gate drive circuit

The PCB layout also plays an important role in improving the dv/dt immunity for the high side driver. As shown in Figure 3.20, if the switching node panel is overlapped with GND panel, a parasitic capacitance C_{IO} will be induced and paralleled between primary and secondary side of the digital isolator. Noise will be easily coupled through this path, and the dv/dt immunity of high side driver will be largely decreased. Avoiding PCB layout overlap between the ground and the high side can effectively reduce the parasitic capacitance. The experimental waveforms resulting from the improved driving circuit and

PCB layout are shown in Figure 3.21. The voltage ringing on the PWM signal is minimized, and the dv/dt immunity is over 120V/ns.

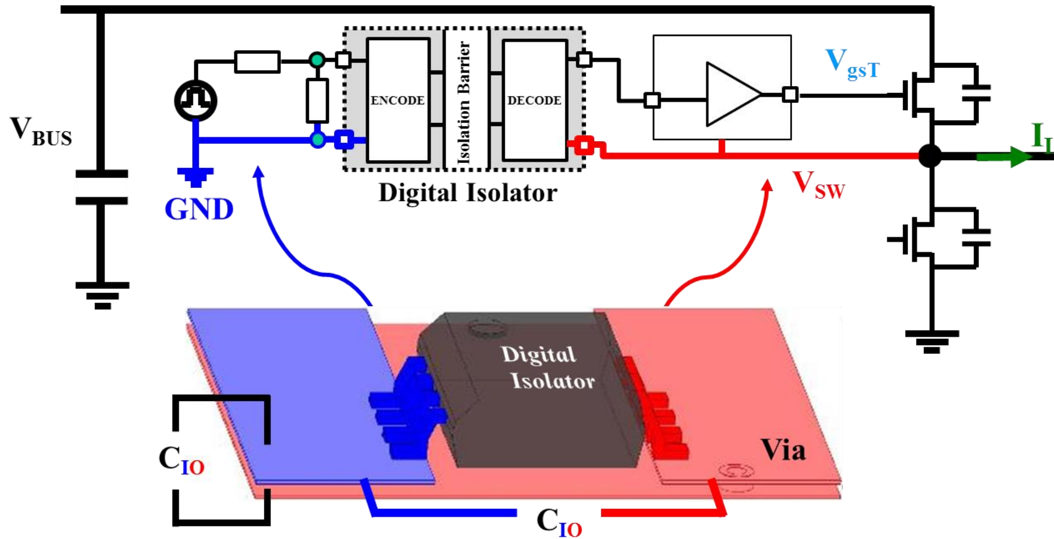


Figure 3.20 PCB layout impact on dv/dt immunity for high side driver

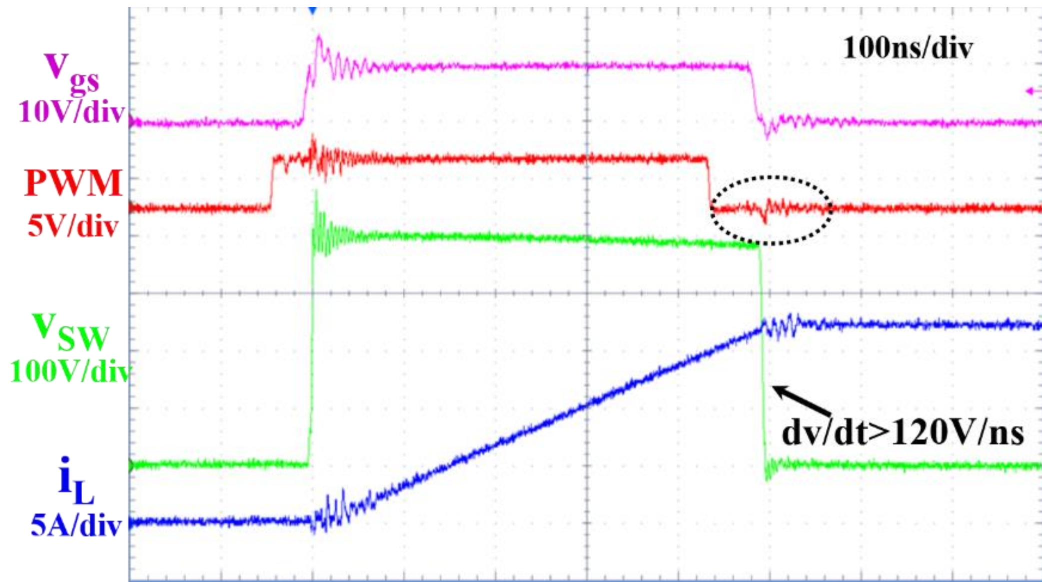


Figure 3.21 Experimental waveform of improved dv/dt immunity for high side driver

It has been mentioned above that the commercial driving transformer cannot be applied to GaN devices due to low dv/dt immunity. The major cause is the parasitic capacitance between the signal side and switch-node, as shown in Figure 3.22. The value is around few tens of pF for most of the commercial driving transformer, and this is indeed a low impedance path for the high dv/dt noise current.

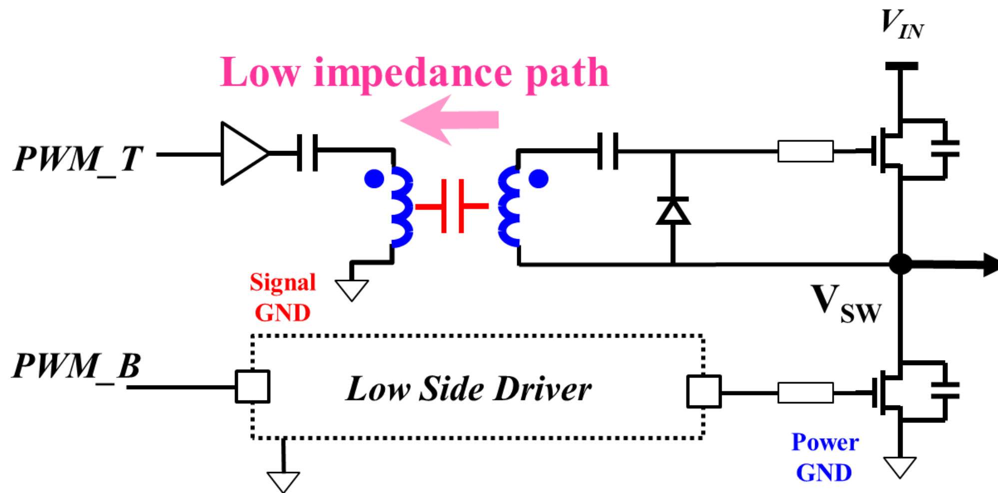


Figure 3.22 Conventional driving transformer is susceptible to noise due to large parasitic capacitance

In order to bypass the noise current, a novel shielding technique is integrated in the driving transformer, as shown in Figure 3.23. The shielding layer is inserted between the primary and secondary winding and one terminal is connected to the power ground, which is also the noise source ground. The shielding layer and secondary winding induces inter-winding capacitor and the noise current can easily go through the capacitance and travel to the shielding layer. Since the shielding layer is connected to the noise source ground, it is a low impedance path for the noise current. The majority of noise current will flow through in the loop, marked in Figure 3.23. The shielding layer also induces capacitor with the

primary winding, however, the impedance of the capacitance is much higher than the other path which is direct copper connection. Negligible noise current can flow through the capacitor boundary. This is true when the main frequency of the noise current is lower than few GHz, which is practical for GaN devices.

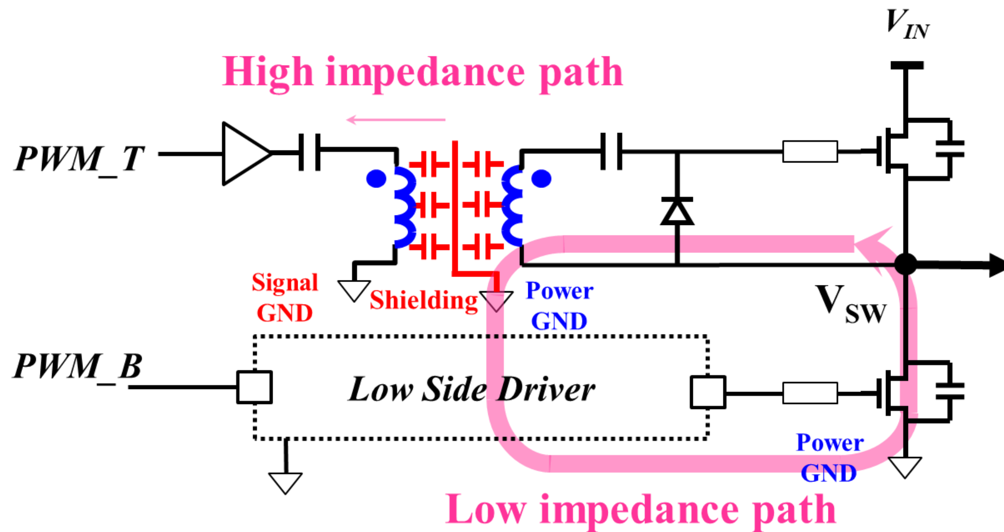


Figure 3.23 Novel driving transformer with shielding

To verify the proposed high side driving method, a driving transformer with shielding is designed for a 500kHz buck converter. The core size is small due to high frequency operation, a planar ER11/5 is chosen. PCB winding is implemented to simplify the winding design. Only three layers of PCB is necessary to fulfill the function of the proposed method, as shown in Figure 3.24.

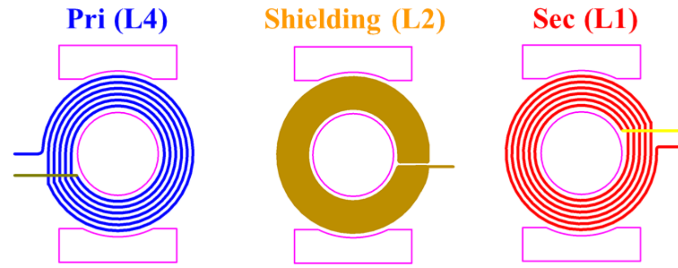


Figure 3.24 Proposed driving transformer with shielding

The core loss the driving transformer is less than 10mW at 500kHz. The maximum magnetizing current is 80mA and corresponding winding loss is negligible. The experimental waveform comparison is shown in Figure 3.25. The glitch came out at the PWM signal when the dv/dt only rises to 35V/ns in the case without shielding. On the other hand, the noise at the PWM signal is less than 100mV with shielding when the dv/dt is 100V/ns. The dv/dt immunity of the driving transformer is significantly improved by novel shielding technique. Moreover, auxiliary power supply, either form external or bootstrap diode, is not needed for the high-side device with driving transformer approach, which can further simplify the system design.

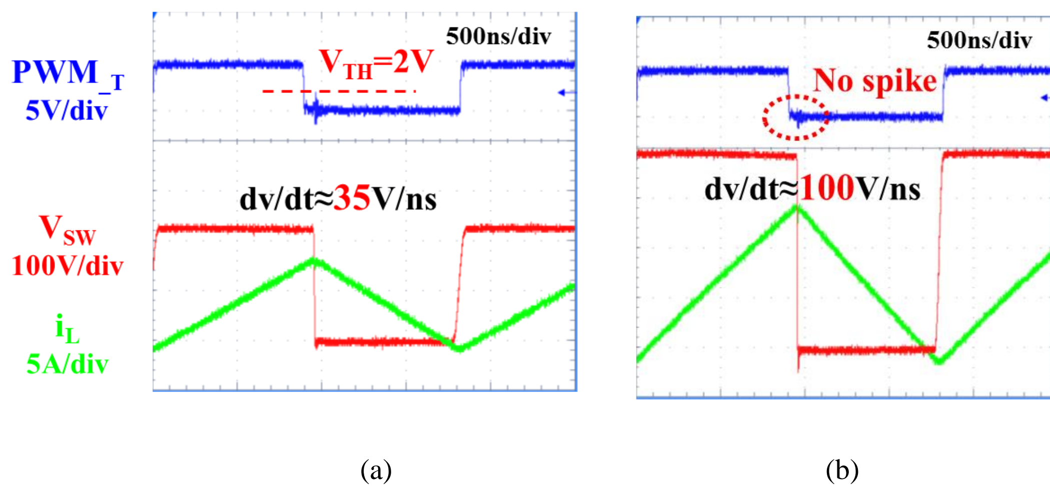


Figure 3.25 Comparison of driving transformer: (a) w/o shielding, (b) w/ shielding

3.4 Conclusion

This chapter presents the design considerations for GaN devices, including the comparison of hard-switching and soft-switching, and high frequency gate drive for GaN devices. Numerous experimental data validates that soft-switching significantly benefits GaN devices from both efficiency and noise perspective. The fast switching speed of GaN devices raises di/dt and dv/dt related gate drive challenge. The best way to solve the di/dt related issue is to minimize device package and PCB layout parasitic inductance, while olution for dv/dt requires minimal parasitic capacitance between high side and signal ground as well as minimize input impedance. Two different methods are proposed and both of them can operate properly under very high dv/dt condition. Choice can be made according to different system application.

Chapter 4. System Design of GaN Based AC-DC Adapters

This chapter presents high frequency, high efficiency and high power density design of AC-DC adapter. GaN devices are deemed as a game changing device in this particular application with improved efficiency and significant size reduction. Detailed design considerations, such as magnetics, EMI, etc., will be illustrated. Few prototypes designs at 25W, 45W, 65W, 150W will be shown to demonstrate the strength of GaN devices and the impact of the system design.

4.1 State-of-the-art Practice

One of the biggest market of power supplies, in both volume and revenue, is the ac-dc adapter/charger for consumer electronics, including laptop, tablet, smart phone, mobile devices, game console, printer, and stereo sound-bars, etc., as shown in Figure 4.1. The market has surpassed $8 billion in 2015 and is projected to reach $9 billion by 2018; with much of this growth being driven by smart phones, tablets and emerging applications [D.1], as shown in Figure 4.2.

Figure 4.1 Applications of AC-DC adapter

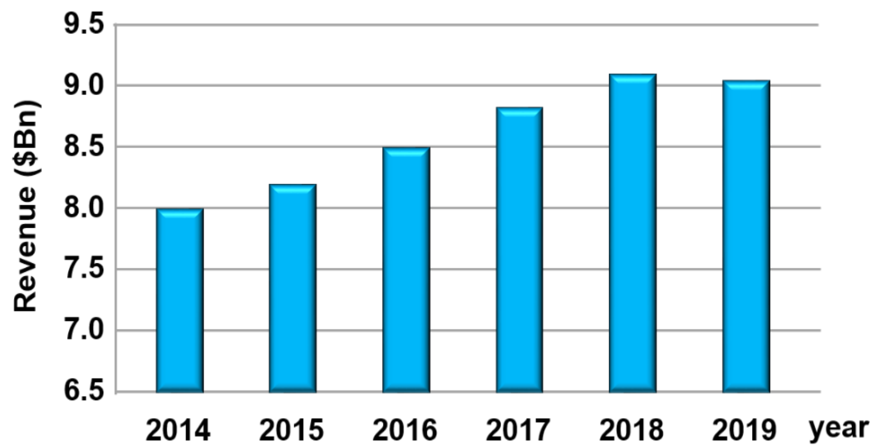


Figure 4.2 Adapter market information Figure 4.2 [D.1]

Adapters are cost-driven and customized for every generation of mobile devices, each with very short product cycle. Disposal of these out-of-date adapters becomes an environmental concern. While the progress of all forms of mobile devices are progressing at an amazing rate with ever in-creasing performances and shrinking in size and weight, their adapter counterparts are bulky with meager power density at 5-12 W/in^3.

Figure 4.3 lists the state-of-the-art AC-DC adapters which are in mass production. Today, most of the adapters are operating at relatively low frequencies (<100 kHz) and with efficiency below 92%. For example, the MacBook Air laptop now weighs less than 2.4 lbs, while the accompanying 45W adapter still weighs 0.41 lbs, and the manufacturing and the assembly process for adapter remains labor-intensive. The internal image from a teardown Apple adapter is shown in Figure 4.4. It clearly shows that the most of the components have to be inserted on the PCB manually. In particular, the power transformer (with yellow mask) is in a hand-made fashion. The parasitics are hard to control and the parameters varies from piece by piece, which make it the most challenging part for the system designer.

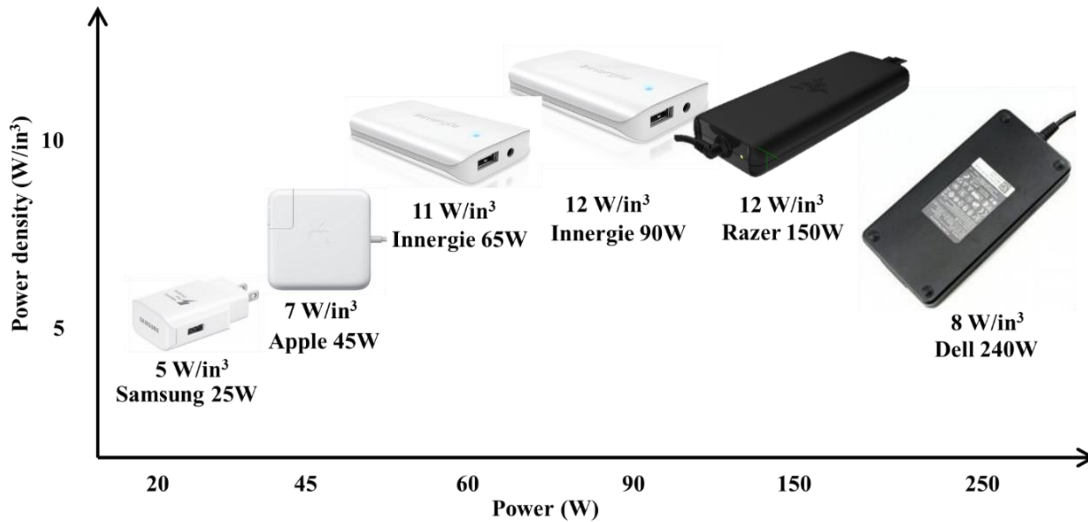


Figure 4.3 State-of-the-art AC-DC adapters

Figure 4.4 Inside the Apple adapter

It is important to note that the power density for adapters is ultimately thermally limited. The maximum allowed adapter surface temperature for safety is 95°C with a plastic case and 70°C with a metal case [D.2]. Furthermore, most of the products are further derated for surface temperatures at 70°C plus to avoid excess surface heat. Based on a 95°C surface temperature, the theoretical relationship between power density and efficiency can be calibrated based on thermal simulation and the results are shown in Figure 4.5. The adapter is assumed to be composed by two boxes and the form factor is similar to Apple adapter. The dark grey color box is the power converter and it is surrounded by light grey box which is the plastic case. The heat is assumed to be uniformly distributed inside the box. It is natural cooling condition and the surface convection coefficient is around 6~8 W/m^2 °C. The simulated curve indicates that the power density improvement has to be accomplished with efficiency improvement simultaneously. The state-of-the-art products are also plotted on the curve and the stars imply that current products are all far below their theoretical limits.

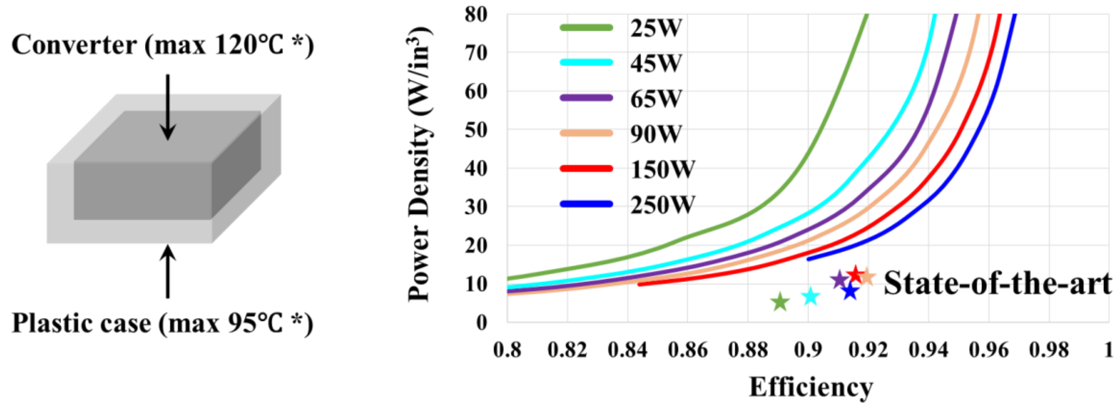


Figure 4.5 Theoretical limit of power density vs. efficiency (max 95℃ with plastic case)

High efficiency and high frequency are the catalysts for size reduction. The emerging GaN device, with much improved figures of merit, opens the door for an operating frequency well into the MHz range. The research goal is to achieve a power density up to 30~40W/in^3 by increasing frequency up to 10 times of current practice, along with significant efficiency improvements.

4.2 MHz Active Clamp Flyback Converter for Adapters Po < 75W

Flyback converters are dominant topology for low power offline application due to its simplicity and low cost. Several literatures have demonstrated flyback converter with GaN devices operating over 1MHz in order to reduce passive components volume [D.3]~ [D.6]. However, traditional flyback converter has to be improved to achieve high efficiency at high frequency, including the soft-switching technique, high frequency transformer design and the EMI characterization and filter design.

4.2.1 Soft-switching with Active Clamping Circuit

Figure 4.6 shows the circuit configuration of the conventional flyback and active clamp flyback converter. The basic operation principle of these two converter are well-known to power electronics researchers/engineers, which will not be discussed in this work. The conventional flyback converter usually operates in CRM mode to minimize turn-on switching loss, and this approach works fine at low frequency (200kHz). However, the topology should be re-evaluated at high frequency, namely 1MHz.

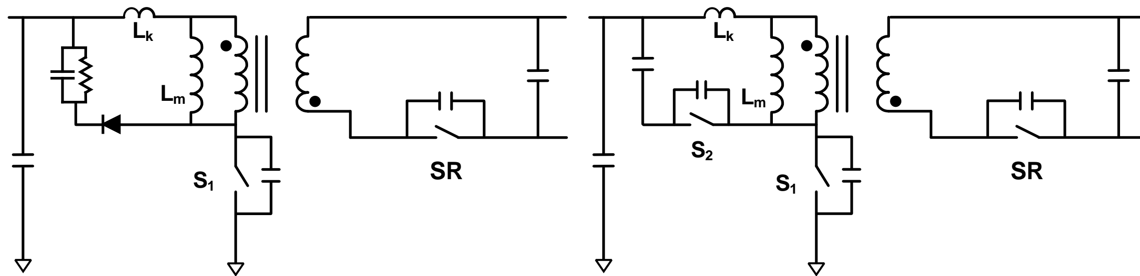
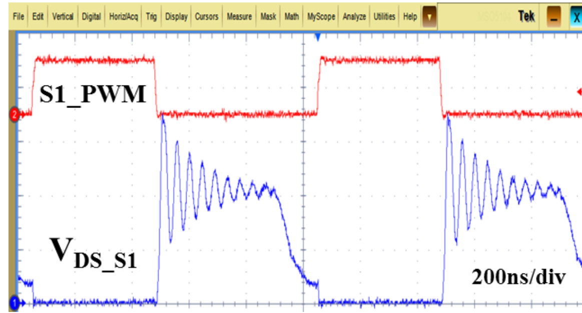


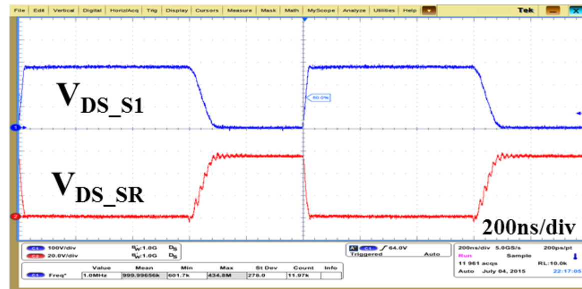
Figure 4.6 Conventional flyback vs. Active clamp flyback

The key switching waveforms of these two topology operating at 1MHz are shown in Figure 4.7. The conventional flyback uses RCD clamp circuit to dissipate the leakage energy and suppress the voltage spike when the main switch is off. However, the leakage energy loss is proportional to the switching frequency and it is quite considerable at MHz frequency range. Moreover, the voltage ringing causes high voltage slew rate which has significant impact on EMI noise, especially at 10~30MHz range. It clearly shows that the parasitic ringing during the switch off period is huge at 1MHz. Furthermore, CRM mode operation can only achieve valley switching and can’t achieve ZVS for the main switch at high line input condition, which we have illustrated the importance of ZVS on GaN devices at high frequency. On the other hand, active clamp flyback can clamp the voltage without any ringing as shown in Figure 4.7(b) and recycle the transformer leakage energy which

can be used to realize ZVS for the main switch. Different from low frequency operation, leakage inductance energy is not sufficient to realize ZVS for the main switch at 1MHz. The magnetizing current need to reverse direction to help achieve ZVS.



(a) Conventional flyback operate in CRM mode

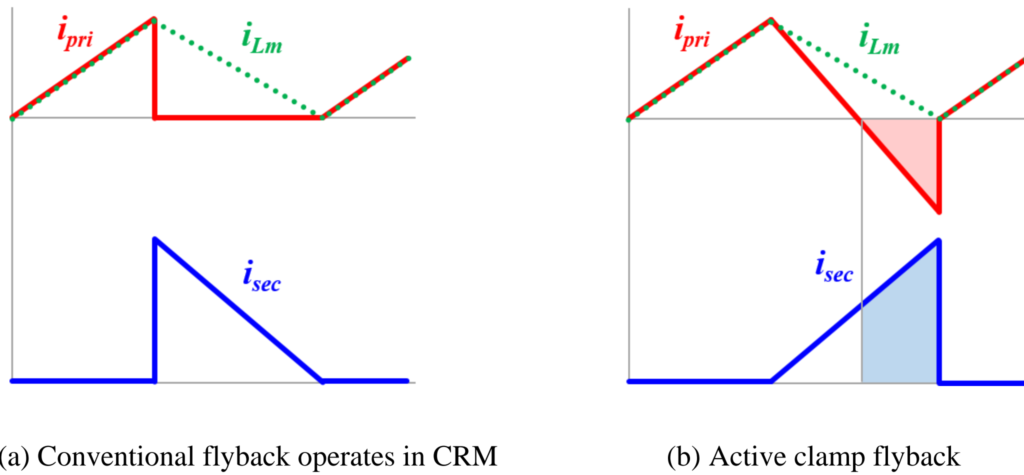


(b) Acitve clamp flyback

Figure 4.7 Key waveforms of two flyback topology operating at 1MHz

In addition to the common knowledge on the active clamp flyback converter, it is interesting to find out that the active clamp circuit modifies the transformer behavior. Figure 4.8 shows the ideal transformer winding current comparison of the traditional flyback and active clamp flyback converter. It is well-known that the conventional flyback transformer is actually an inductor with two windings conducting current in different time period. There is no flux cancellation and therefore the winding loss is typically large. However, there is flux cancellation effect in active clamp flyback transformer marked as the shaded zone in

Figure 4.8(b). When the primary current goes negative, the magnetic field strength is reduced and the current can be more evenly distributed in the winding. The time-domain winding loss of these two flyback topologies is shown in Figure 4.9 based on FEA simulation, and the loss reduction is about 20% with active clamp flyback.



(a) Conventional flyback operates in CRM (b) Active clamp flyback

Figure 4.8 Comparison of ideal transformer winding current

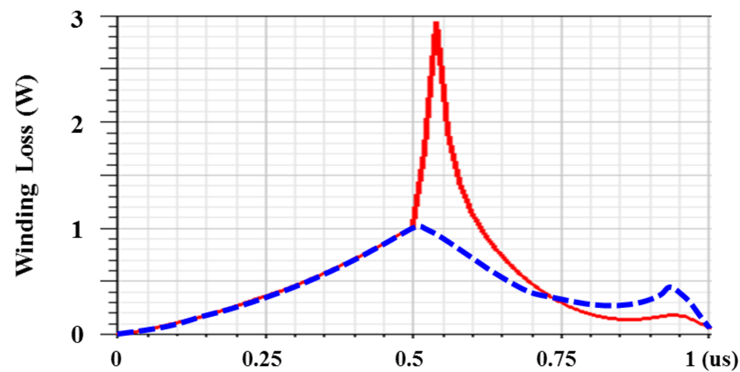


Figure 4.9 Time-domain winding loss of two flyback topologies (red solid line: conventional flyback; blue dash line: active clamp flyback)

All of these features mentioned above results in higher efficiency and lower noise which makes active clamp flyback topology very suitable for high density adapter application.

The clamping capacitance impacts the resonant frequency as well as the initial condition of the resonant tank. As a result, it determines the current waveforms of the resonant tank and the secondary side. Figure 4.10 shows the simulated current waveforms considering all the parasitics at 90Vac input and 65W output power condition. With smaller C_{clamp}, half of the resonant period formed by L_k and C_{clamp} is close to the main switch Sw off period. i_{Lk} is close to i_{Lm} when clamping switch is turn off, which means the turn off current of clamping switch is small. On the other hand, the current ripple of i_{Lk} is large due to the complete resonant. The secondary side current i_{SR} is the difference between i_{Lm} and i_{Lk}, and therefore, i_{SR} also has large ripple. On the contrast, the turn off current of clamping switch increases with larger C_{clamp}, while the current ripple of both primary and secondary side reduces significantly. Figure 4.11 summarizes the impact of C_{clamp} on the related converter power loss. It shows that increasing C_{clamp} in the range of below 100nF significantly reduces the conduction loss and slightly increases the turn off switching loss. Therefore, the total C_{clamp} related loss reduces with larger capacitance. Further increasing C_{clamp} has diminish return in terms of power loss reduction, but the penalty is larger size and relatively slow dynamic performance. Overall, 100nF is preferred in the converter design from lower loss, smaller size and faster dynamic perspective.

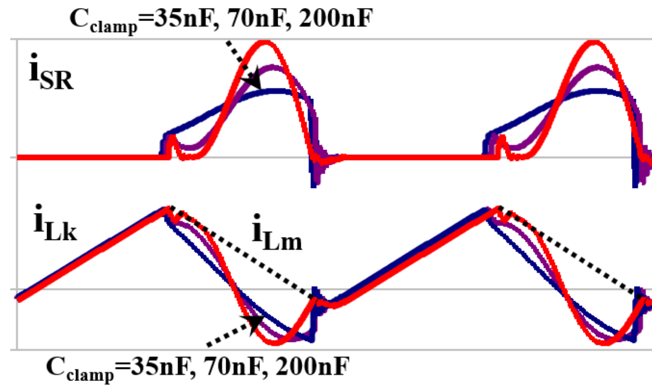


Figure 4.10 Impact of clamping capacitor on primary and secondary current waveforms

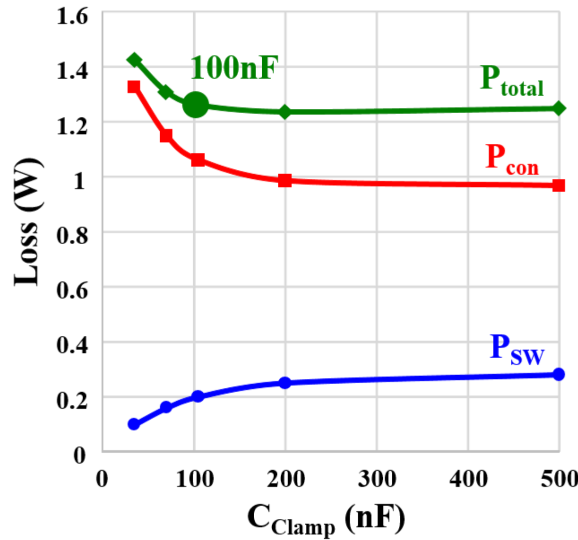


Figure 4.11 Impact of clamping capacitor on converter loss

4.2.2 MHz Flyback Transformer

The traditional low frequency flyback transformer is typically in a hand-made fashion with solid wire. The parasitics are hard to control and the parameters varies from piece by piece. It is also difficult to implement shielding layer in order to reduce common-mode noise. PCB winding based transformer is practical when the switching frequency is close to MHz. It is easier to control the parasitics and also more standardized for automation

manufacture. Shielding layer can be easily added using some of the PCB layer [D.9]. On the other hand, transformer loss is the major part of flyback converter total loss. The design target is to minimize the loss within 3% of total adapter output power. Some key design points are discussed in this section. The optimization process shown below takes a 65W adapter as an example and it is based on $90V_{ac}$ input which is considered as the worst case.

A. High frequency *core material and core shape*

It is critical to select a proper core material for MHz operation. Table 4.1 lists the candidate core materials for MHz operation. The core loss data from datasheets are measured under sinusoid excitation without DC bias. However, the voltage waveform across the active clamp flyback transformer is rectangular shape which will impact the core loss data significantly. Figure 4.12 shows the measured core loss under 1MHz rectangular voltage excitation using Mu's method [D.10], [D.11]. It clearly shows that the core loss data is different from the data listed in Table 4.1. The measured data indicates that ML90S has minimal loss at 1MHz with B_m lower than 100mT.

Table 4.1 High frequency Core Material Comparison

	3F45	N49	P61	ML90S
Initial Permeability	900	1500	900	900
Core Loss (kW/m^3) 1MHz, 50mT	300	400	150	200
Core Loss (kW/m^3) 1MHz, 100mT	1600	2300	3000	4000

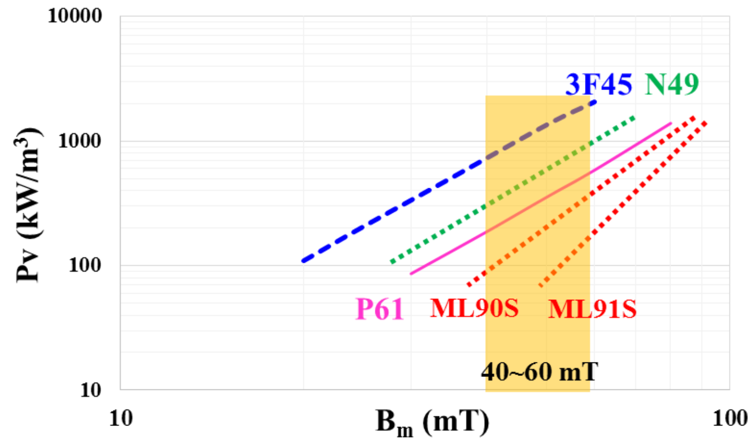


Figure 4.12 Comparison of core loss density of different core material

It is expected that 1MHz frequency operation can reduce the transformer size significantly. In fact the core size and wind turns are determined by the voltage-second as well as optimized flux density. It can be expressed as:

$$N_S \cdot Ae = \frac{V_O \cdot (1-D)}{2 \cdot \Delta B \cdot f_s} \tag{4.1}$$

For conventional flyback which operating at 65kHz, the reasonable peak flux density is around 150mT. While for 1MHz active clamp flyback, the flux density should be reduced to 60mT in order to make the core loss density in the range of few kW/m^3. Therefore, the term $N_s \cdot A_e$ at 1MHz, which reflects the size of transformer, can only reduce to 5 times smaller than that of 65kHz. The size reduction is still significant though it is not proportion to the frequency.

A good core shape for a planar transformer is shown in Figure 4.13. The cross section area should large enough to reduce the winding turns number as well as the flux density. The winding window should be large enough to reduce the resistance. The core should cover the winding as much as possible to minimize the stray field and EMI, improves heat

dissipation. A round center leg minimizes the winding length and avoid current crowding at the corner of a rectangular leg. The detailed parameter optimization will be presented in the next few sections.

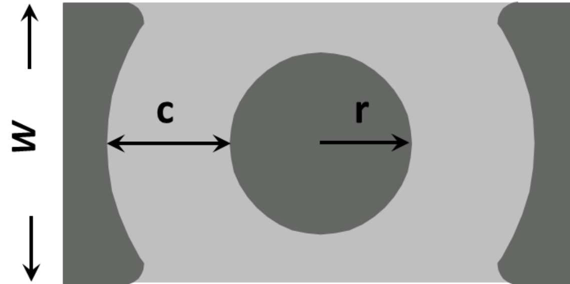


Figure 4.13 ER core shape for MHz design

B. Secondary side turns number*: N_S*

The voltage second of the flyback transformer significantly reduced when the switching frequency increased to MHz range. The flux density of core is determined by voltage second and cross section area as well as the transformer turns number, as shown in (4.1). Since the output voltage is constant, it is used to calculate the voltage second of the active clamp flyback transformer. Accordingly, the relationship between core loss density and turns number is shown in Figure 4.14 based on ML90S core material. The cross section area sweeps from 40mm^2 to 60mm^2 which can be considered as a reasonable range from both loss and volume perspective. It clearly shows that the core loss density is too high for N_S=1 case even Ae=60mm^2. The calculated core loss is over 1W which is unacceptable in 65W adapter application. The core loss density of N_S=2 case is in the range of 200~600 kW/m^3 with reasonable Ae. This is more practical and be chosen for the converter design.

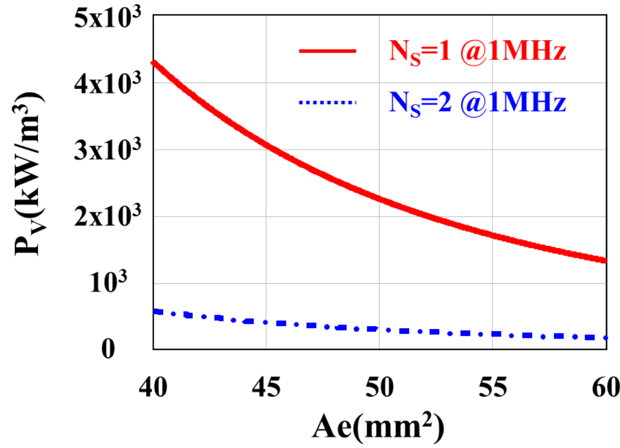


Figure 4.14 Core loss density vs. N_S

C. Turns ratio N_p:N_s, Core cross section *area Ae, and winding window width c*

It is difficult to optimize the flyback transformer parameters based on the conventional method which is aiming ideal transformer. Flyback transformer is actually a two winding inductor and the flux distribution in the conductor is non-uniform and can't be considered as a one-dimensional field [D.12]. The best way to find the optimal design is to utilize the systematic simulation based on Ansoft 2D FEA tool. It is common sense that the air gap induces fringing loss on the adjacent winding. This part of loss is irrelevant to the transformer parameters and it can be minimized by slightly increase the distance between winding and air gap, as shown in Figure 4.15.

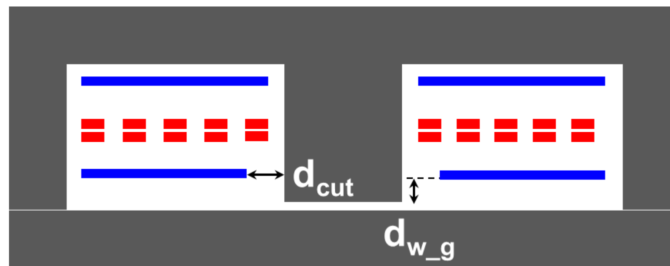


Figure 4.15 Cross section view of the transformer winding (red line represents primary winding, blue line represents secondary winding)

The relationship of winding loss and the distance is shown in Figure 4.16, where d_{cut} and d_{w_g} stands for horizontal and vertical distance between winding and the air gap, respectively. It is obvious that increasing vertical distance definitely can reduce the winding loss but the benifit becomes small at $d_{w_g} > 3\ l_{air_gap}$. On the other hand, there is a minimal loss point over different horizontal distance. Larger d_{cut} results in narrower width for the winding and consequently leads to a larger loss. From the loss curve, it implies that $d_{cut} \approx 3\ l_{air_gap}$ is the optimal point lowest loss, and the yellow dot is the design point. These two parameters are fixed in the simulation which aims to find out the optimal design for other parameters.

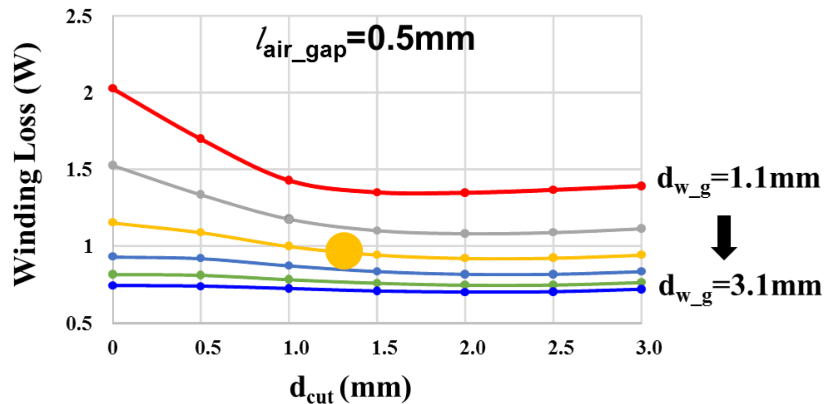


Figure 4.16 Relationship of winding loss and distance between winding and air gap

The transformer turns ratio has several impacts on the converter design. The voltage stress of primary and secondary switch is determined by turns ratio. The voltage rating of available high voltage GaN switch that usemd as the primary switch is 600V, and this sets the maximum turns ratio to be 7 with 15% margin. The secondary GaN switch can select 100~200V eGaN according to the turns ratio. The transformer turns ratio also impacts the root mean square (rms) value of primary and secondary current as well as the duty cycle of

primary and secondary switch. The rms value of the primary and secondary side current are plotted in Figure 4.17. It shows that the primary current decreases with larger turns ratio since the primary side main switch duty cycle increases. On the contrary, the secondary side current increases with larger turns ratio.

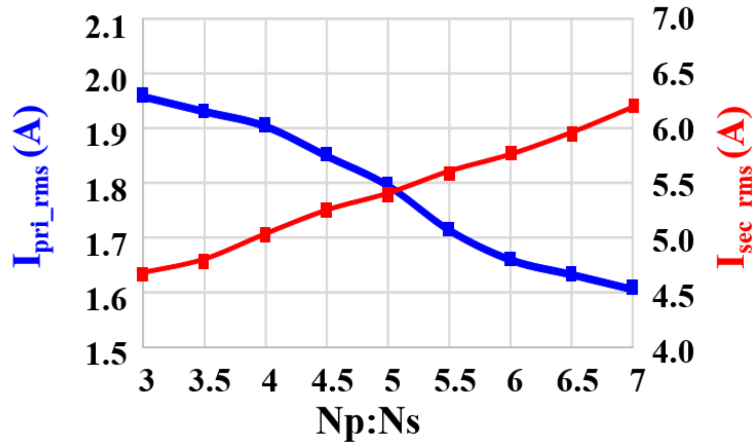


Figure 4.17 Impact of turns ratio on converter current

In addition to the impact on the primary and secondary current, the turns ratio also impacts the core loss and winding loss. The core loss reduces with larger turns ratio since the duty cycle of secondary side reduces which results in a reduction of voltage second applied to the transformer. On the other hand, the primary winding length will increase while primary winding width will decrease with larger turns ration and given secondary winding turns to be 2.

The cross section area Ae and winding window width c also impacts the core volume and the length of winding. In general, the core loss reduces when Ae increases since the impact of ΔB reduction is overwhelming than the increase of core volume. However, the winding loss increases with larger Ae due to increased winding length. The winding

window width has similar impact on the core loss and winding loss. In order to find out the optimal combination of transformer parameters, a systematic simulations are carried out based on the similar drawing shown in . By considering all the parameters mentioned above, a 3-D image presents the relationship of related loss and the transformer parameters, as shown in Figure 4.18. The related loss includes core loss, winding loss and device conduction loss. The X-axis is cross section area Ae, and the Y-axis is the window width C. The surface of the loss drawing varies with another variable which is transformer turns ratio. The core width W has negligible influence on the total loss based on the simulation result. The optimal design point is at the turns ratio equals 10:2, cross section area Ae ≈ 48mm^2, and the winding window width ≈ 6.2mm. The standard core shape ER23/3/6/13 has the similar parameters with the desired value and it is used in this converter design.

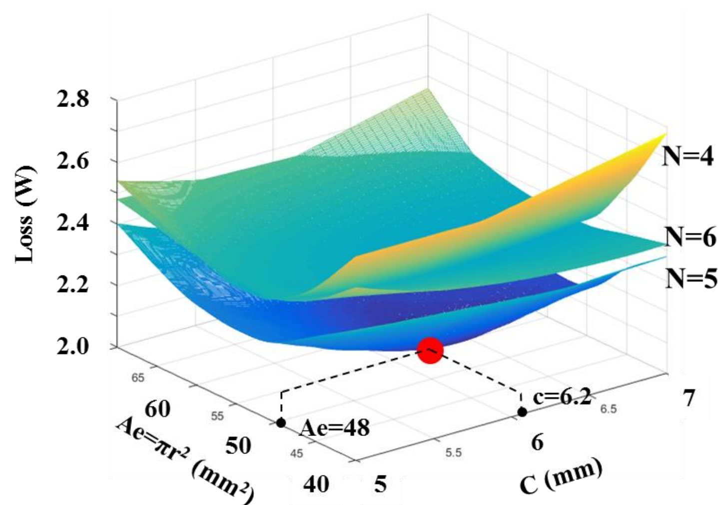
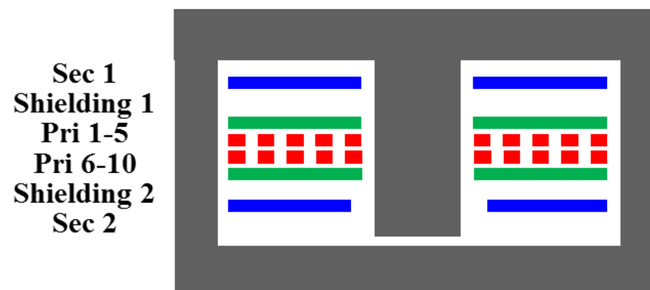


Figure 4.18 Related loss vs. transformer parameters

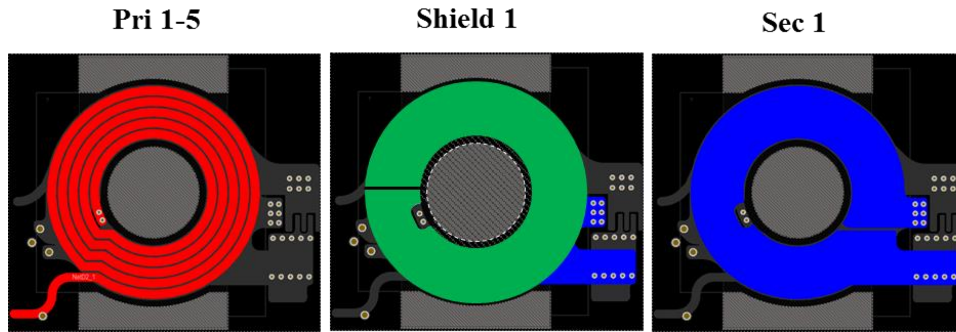
D. Integrate shielding *layer*

The parasitic capacitance between the primary winding and secondary winding is the major propagation path for common-mode noise. The most convenient way to block the

noise is to insert shielding layer between each other [D.13]. The drawback of this method is that it prevents a more efficient winding structure, such as sandwich pattern winding, and as a result, the leakage inductance and winding loss of the transformer with shielding layer increased significantly. However, this contradictory can be solved when the secondary winding turns number reduces to two and be split into two layers in the PCB. The novel shielding layer can be easily implemented in the PCB winding as shown in Figure 4.19. Figure 4.20 shows the circuit diagram of flyback converter with shielding. The shielding is connected to the primary ground. Therefore the CM noise current coming from the primary noise source is circulating within the primary side. To block the noise flow through shielding to secondary winding or reverse direction, the shielding layer should have same voltage potential as the secondary winding. A simple way is to make the shielding layer exactly the same as the secondary winding. The same polarity point of the transformer, marked as the big dot in Figure 4.20, should be connected to either steady voltage point such as V_{bus}, GND, and V_o, or to the bouncing point such as device drain terminal at the same time. Rotating the shielding layer with any angle creates displacement current circulating between secondary winding and shielding, but it does not create CM current from either side [D.9].



(a) Transformer winding cross section view



(b) Detailed PCB layout view

Figure 4.19 Flyback transformer winding structure with shielding

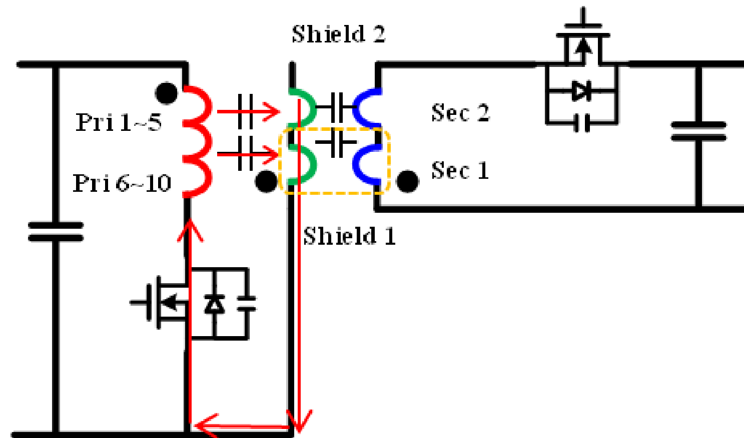


Figure 4.20 Flyback transformer with shielding

One of the general concern of adding shielding layer to the flyback transformer is the winding loss. The 3D FEA simulation is carried out to evaluate the impact of the shielding layer on the total transformer winding loss as shown in Figure 4.21. It shows that the current distribution in the primary and secondary winding almost remains the same and the current density in shielding layer is also very small. The total winding loss with the shielding layer is 1.35W and it is only 0.05W larger than the case without shielding layer, which is negligible loss increase.

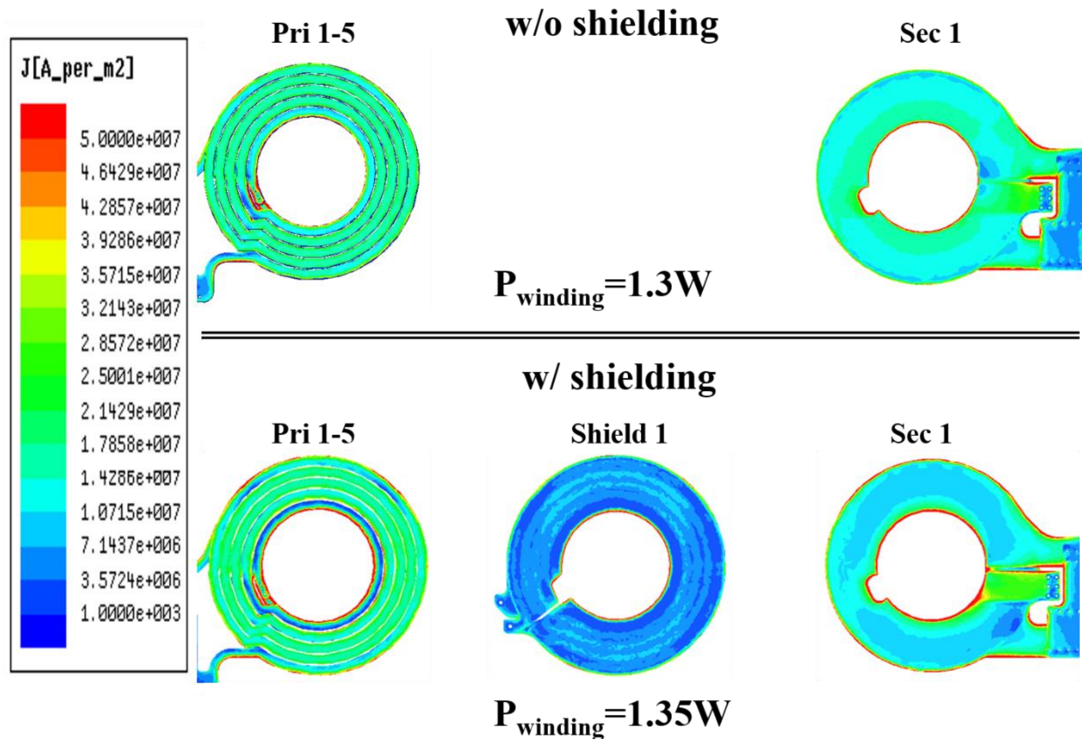


Figure 4.21 3D FEA simulation of flyback transformer with and without shielding layer

The shielding layer can be further integrated and serves as the first two turns of primary winding based on winding cancelation method [D.14], [D.15], as shown in Figure 4.22. As a result, the number of turns in each primary winding layer reduces from five to four and the width of the copper trace increases by 20%. Over 13% winding loss reduction compared with separated shielding is achieved based on FEA simulation result.

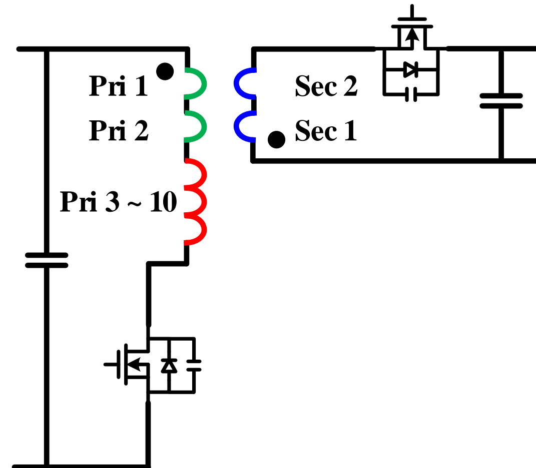


Figure 4.22 Integrated shielding layer as the primary winding

To summarize the flyback transformer design, the ML90S from Hitachi is chosen for the core material; ER23/3.6/13 core shape is selected with optimized cross section area and winding window width; the primary to secondary winding turns ratio is 10:2; the shielding layer is integrated in the PCB winding with negligible increase of total winding loss.

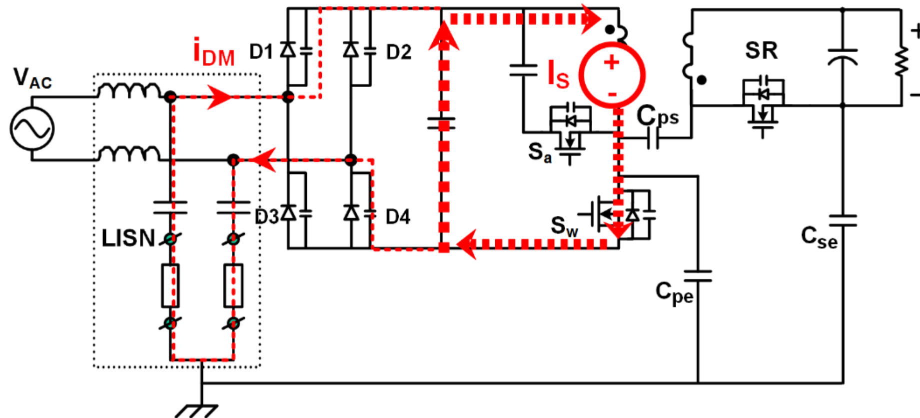
4.2.3 MHz Flyback Converter EMI Characterization and Filter Design

A. Analysis *of CM/DM noise and transformation mechanism*

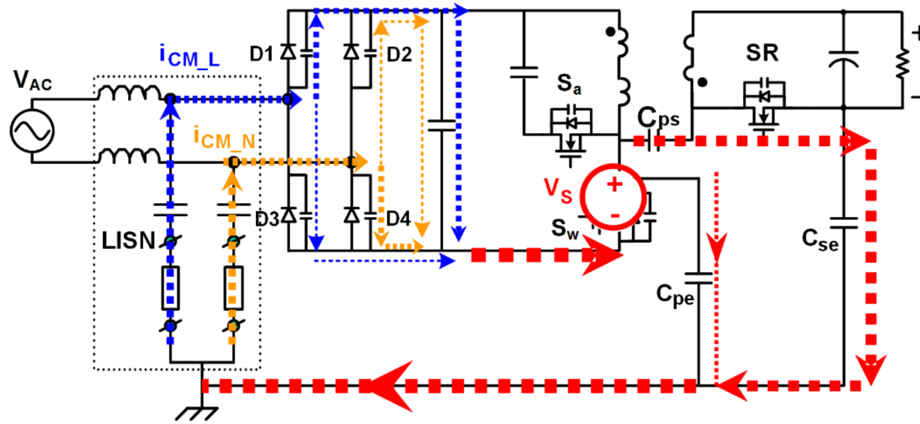
The modeling and analysis of conducted EMI noise of flyback front-end converter are illustrated in [D.16]-[D.19]. The common-mode (CM) noise is majorly coupled through the parasitic capacitance of the transformer and the differential-mode (DM) noise is determined by switching current ripple and input impedance. Except for the CM and DM noise, there is additional mixed-mode noise which is transformed from unbalanced CM current. This mix-mode noise also contributes to the total DM noise when it is measured using spectrum separator. While the mix-mode noise phenomenon has been described and

some analysis are reported in their studies, the fundamental mechanism by which the unbalanced current is induced has not been revealed.

To better understand the CM/DM transformation mechanism, the DM and CM noise propagation path of flyback converter is shown in Figure 4.23. The DM noise source is the switching current ripple of the transformer primary winding, which is represented as I_S. Majority of the noise current is bypassed by DC bus capacitor and the remaining noise current flows through the diode bridge (either diode or junction capacitance) and Line Impedance Stabilization Network (LISN). The portion of these two paths is determined by impedance. The primary switches induce high dv/dt which dominates the overall CM noise magnitude, and it is represented as a noise source V_S. Compared to the primary to the power earth parasitic capacitance C_{PE}, the interwinding capacitance of the flyback transformer C_{PS} and the secondary ground to power earth parasitic capacitance C_{SE} are much larger and it is the major coupling path of the CM noise. The CM noise current flow through the LISN, diode bridge (either diode or junction capacitance), and back to the noise source.



(a) DM noise propagation path



(b) CM noise propagation path

Figure 4.23 EMI noise propagation path of active clamp flyback converter

It has been identified that CM/DM noise transformation occurs when the diode-bridge is off [D.16], [D.19]. Using zero-span mode of a spectrum analyzer, the magnitude of a selected EMI frequency can be displayed with respect to time [D.16]. Figure 4.24 shows the time-domain waveform of the switching frequency noise in spectrum analyzer based on a 65W MHz flyback front-end converter. The diode bridge on and off interval are clearly marked. The magnitude of DM noise in diode-on interval was expected to be higher than diode-off interval due to lower impedance when diode is on. However, the measured DM noise magnitude in diode-off interval is much higher than diode-on interval, especially in the short period right after or before diode is on. The explanation of CM/DM noise transformation in [D.16], [D.17], [D.19] is that one of the four diode is forward bias by CM current and causes CM noise path impedance unbalance. This is actually not an accurate description, the fundamental reason of this phenomenon is illustrated as follows.

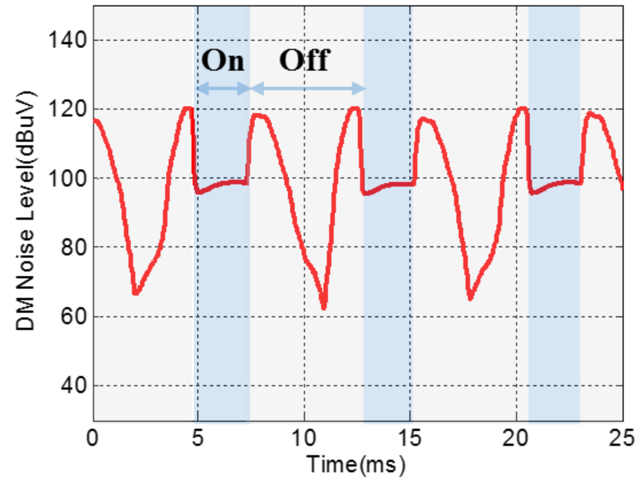


Figure 4.24 DM noise of switching frequency using zero-span mode in spectrum analyzer

As mentioned above, the majority of CM noise current flows through Cps and Cse to earth and LISN. Then the CM noise current go through L and N lines separately. The L line current goes through the junction capacitors of D1 and D3 during the diode-off period. Similarly, the N line current goes through D2 and D4 junction capacitors, and then the two current merges together back to the noise source.

Since the CM noise current is induced by switch in every switching cycle, there is switching frequency current charging and discharging the junction capacitors of the diode bridge, and the high frequency voltage ripple of diode voltage is observed during diode off period, as shown in Figure 4.25. The zoom in waveform at t_1 instant at where the diode bridge is just off during positive line cycle is shown in Figure 4.26. The voltage ripple induced by CM noise current is about 10V. As shown in Figure 4.26, V_{D1} and V_{D4} are much smaller than V_{D2} and V_{D3} at t_1 instant, therefore, the impedance of junction capacitor of D1 and D4 is much lower compared with D2 and D3 according to the nonlinearity of diode junction capacitance relationship with reverse voltage which is shown in Figure 4.27 [D.20]. As a result, the CM noise current mainly go through D1 and D4. More importantly, the

10V voltage ripple impacts the junction capacitance significantly when the reverse voltage is low according to Figure 4.27. In other words, there is a great discrepancy between the impedance of junction capacitance of D1 and D4 due to nonlinear junction capacitance.

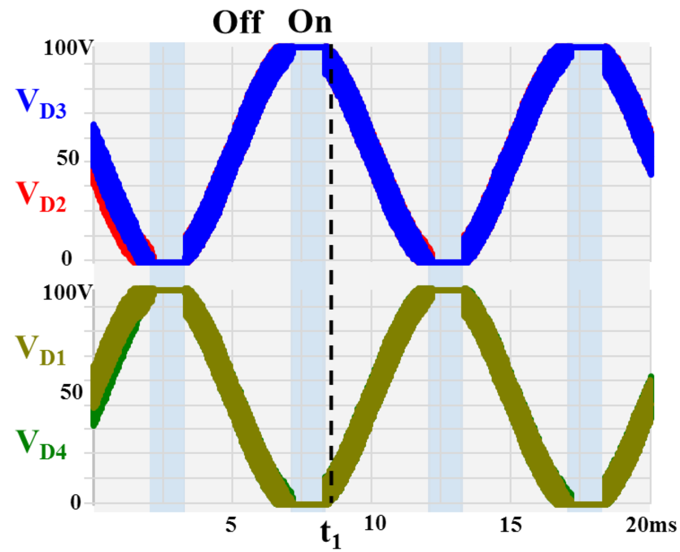


Figure 4.25 Diode bridge voltage waveforms in line cycle

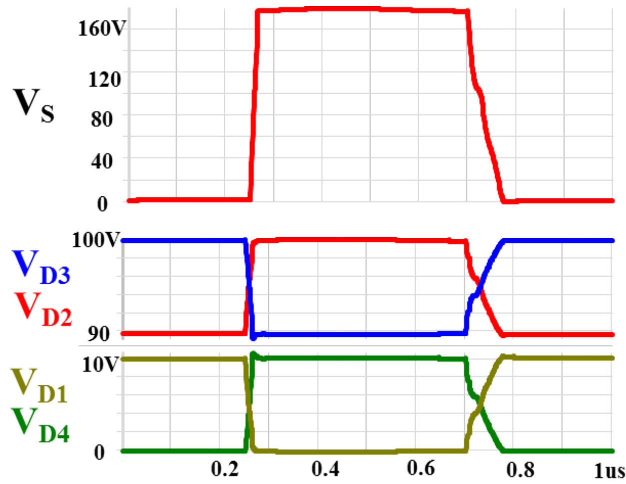


Figure 4.26 Diode bridge voltage waveform at t_1 instant

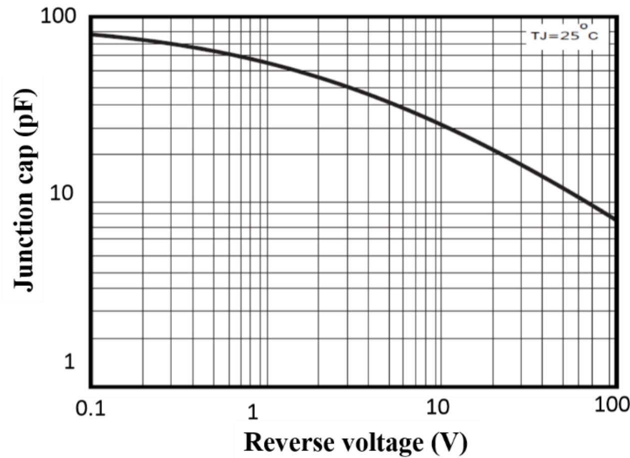


Figure 4.27 Diode junction capacitance characteristics

Consequently, the CM noise current in line L and N is different due to unbalanced impedance, as illustrated by Figure 4.28. The difference between CM noise current in L line and N line can be measured as DM noise, which means CM noise transformed into DM noise in such a manner. The impedance of diode junction capacitance is more balanced in the middle of diode-off period, therefore the magnitude of DM noise gradually reduces due to less CM/DM transformation.

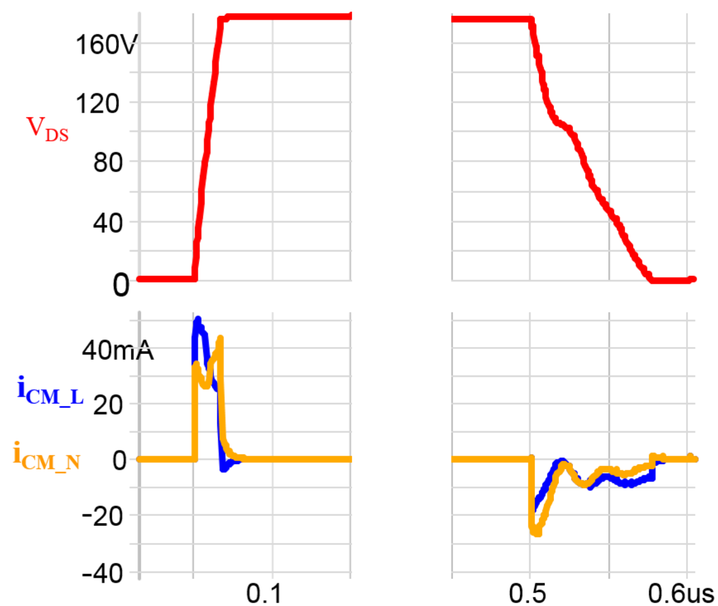


Figure 4.28 CM noise current in L line and N line

It is obvious that the DM filter will be overdesigned according to Fig. 2 without understanding the mechanism of CM/DM noise transformation.

B. Impact of shielding on CM/DM noise

The CM noise propagation path with shielding is shown in Figure 4.29. The CM noise current path through interwinding capacitance is cut off and the amplitude of the remaining noise current is small due to small parasitic capacitance C_{pe}. As a result, the magnitude of the DM noise which is transformed from CM noise is reduced. Moreover, the switching frequency voltage ripple of diode in diode-off period caused by CM noise current also decreases. The difference of junction capacitance of diode is much smaller and this makes the impedance more balanced.

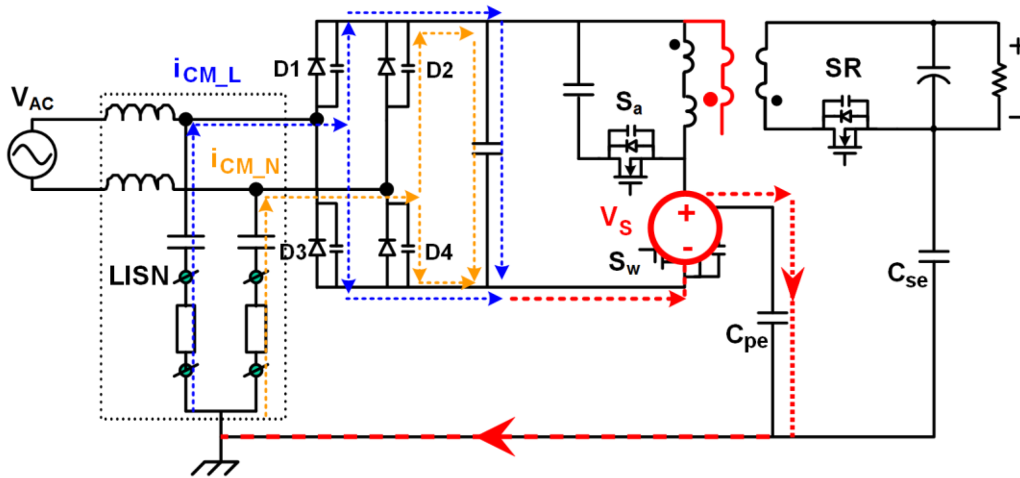


Figure 4.29 CM noise propagation path with shielding

The detailed switching frequency ripple on diode-bridge is shown in Figure 4.30. The magnitude of the voltage ripple is reduced to 0.5V. The L line and N line CM noise current reduces to 3mA and the difference becomes very small due to more balanced impedance.

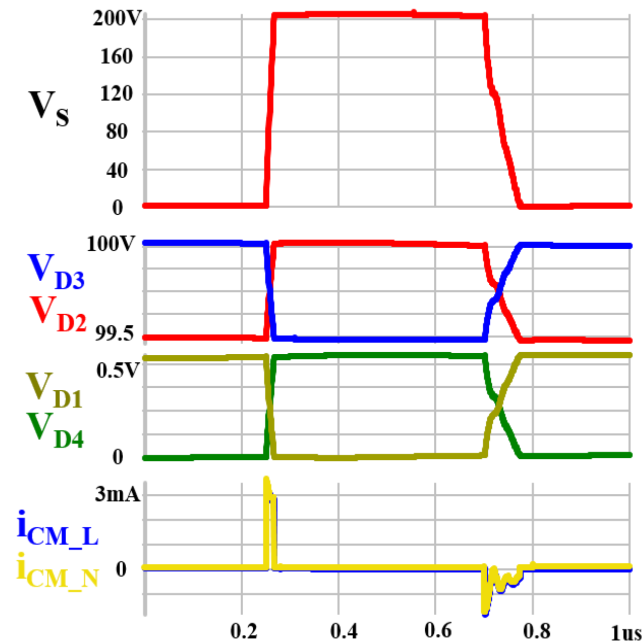
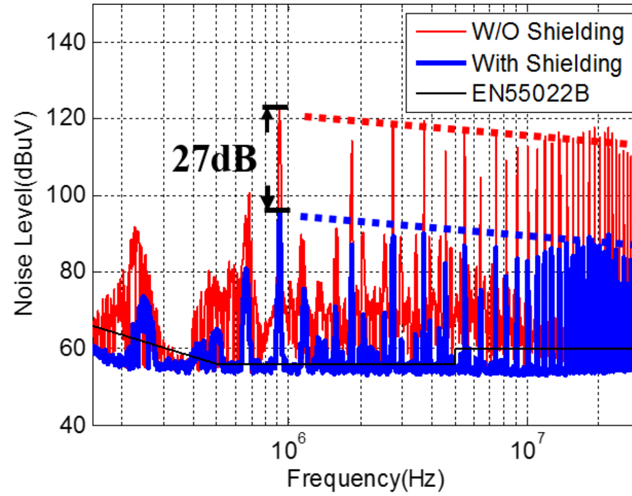
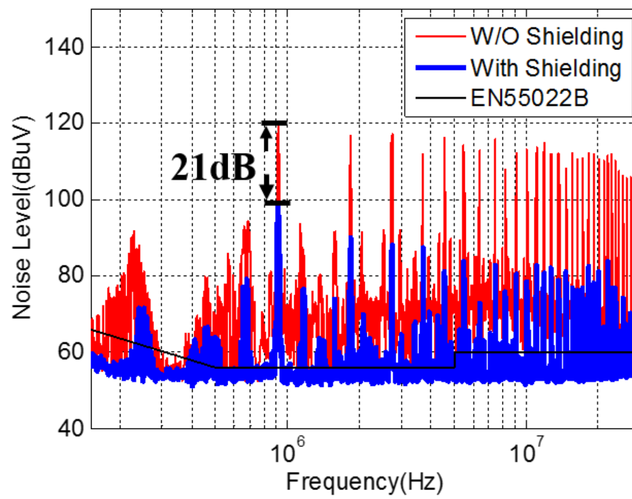


Figure 4.30 Detailed diode-bridge voltage waveform and CM noise current in L line and N line right after diode bridge is off

The measured CM/DM noise with shielding is shown in Figure 4.31. The CM noise reduces by 27dB at switching frequency and the shielding is effective in the whole testing frequency range (up to 30MHz). This is an important feature since the high frequency noise is difficult to be attenuated by filters due to the poor characteristic of filter at that frequency range. The DM noise reduces by 20dB at all frequency range due to less CM noise and CM/DM transformation. As illustrated by the time-domain waveform shown in Figure 4.32, DM noise in diode-off interval is smaller than diode on interval.



(a) CM noise measurement w/ and w/o shielding



(b) DM noise measurement w/ and w/o shielding

Figure 4.31 EMI noise measurement

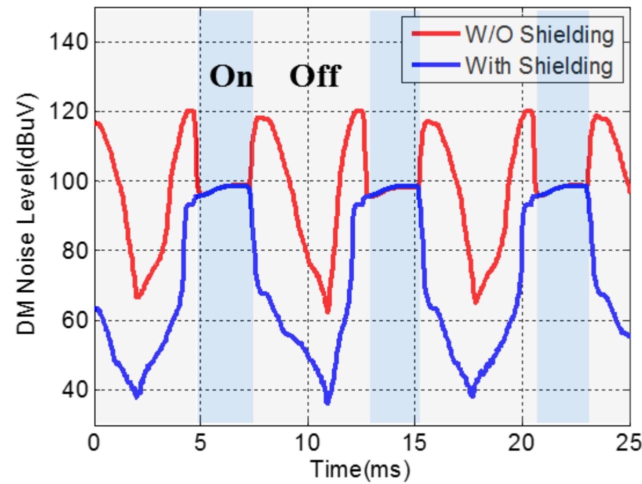
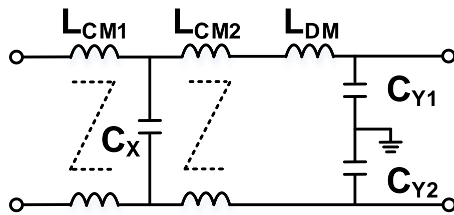


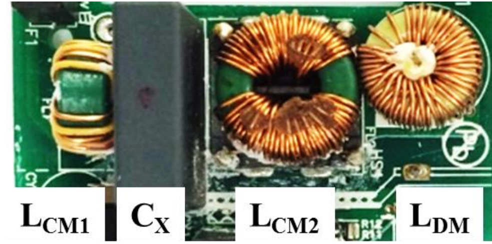
Figure 4.32 DM noise of switching frequency using zero-span mode in spectrum analyzer

C. High frequency *EMI filter design*

The typical EMI filter for adapter application is shown in Figure 4.33. L_{CM2} is the major CM choke with large number of turns to attenuate the switching frequency and harmonic frequency noise. The parasitic capacitance of the L_{CM2} is relatively large and the high frequency impedance characteristic turns to be capacitive. L_{CM1} is usually made in a small toroid core with few turns to deal with very high frequency range (10MHz~30MHz) CM noise. The leakage inductance of L_{CM1} and L_{CM2} is not sufficient to attenuate the DM noise due to low switching frequency. An additional L_{DM} is required to suppress the DM noise. Therefore, three chokes in total are needed to attenuate the total EMI noise which makes the EMI filter quite large. Generally speaking, the EMI filer occupies at least one fourth of the total system volume, and dissipates about 1% to total input power on the choke windings.



(a) Two-stage filter



(b) Filter image of 65W adapter product

Figure 4.33 EMI filter for conventional adapter application

It is always true that the desired corner frequency of the CM and DM filter increases with switching frequency when switching frequency is higher than 150kHz. The corner frequency can be calculated by the desired attenuation at switching frequency according to the conducted EMI standard EN55022B. Due to MHz operation and effectiveness of the designed shielding layer, the simple one-stage filter can be used to attenuate the total EMI noise, as shown in Figure 4.34. It is assumed that the attenuation of the one-stage filter is 40dB/dec after the corner frequency. Based on the measurement results shown in Figure 4.31, the corner frequency of CM and DM increases to around 100kHz which is much higher than current industry practice. The maximum Y-cap that can be used is limited by the leakage current defined in IEC60950. Two 1nF Y-cap is used in the prototype design. Then L_{CM} can be calculated according to the CM filter corner frequency. L_{DM} is the leakage inductance of CM choke and C_X is calculated based on DM filter corner frequency. The parameters of the EMI filter is summarized in Table 4.2.

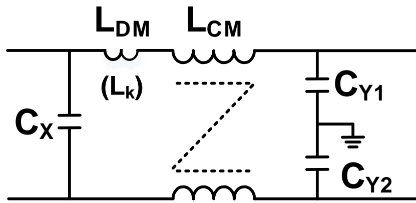


Figure 4.34 One-stage EMI filter for MHz flyback converter

Table 4.2 Parameters of the one-stage EMI filter

Parameters	L_{CM}	L_{DM}	C_{Y1}=C_{Y2}	C_X
Value	1.4mH	0.03mH	1nF	130nF

The conventional core materials for CM/DM chokes have high permeability at few hundreds of kHz and drops sharply at frequency above 500kHz marked as the black curve in Figure 4.35. 3E6 from Ferroxcube is one example of this kind of material. They are good enough for the converter operates below few hundreds of kHz. However, these kinds of materials are not suitable for MHz application. The desired features for high frequency chokes includes relative high initial permeability and relative stable permeability over the frequency range from 1MHz to 5MHz, which is marked as the yellow zone. Few candidates have high permeability in this frequency range. The ferrite materials 3D3 (available off the shelf) is chosen for the prototype validation.

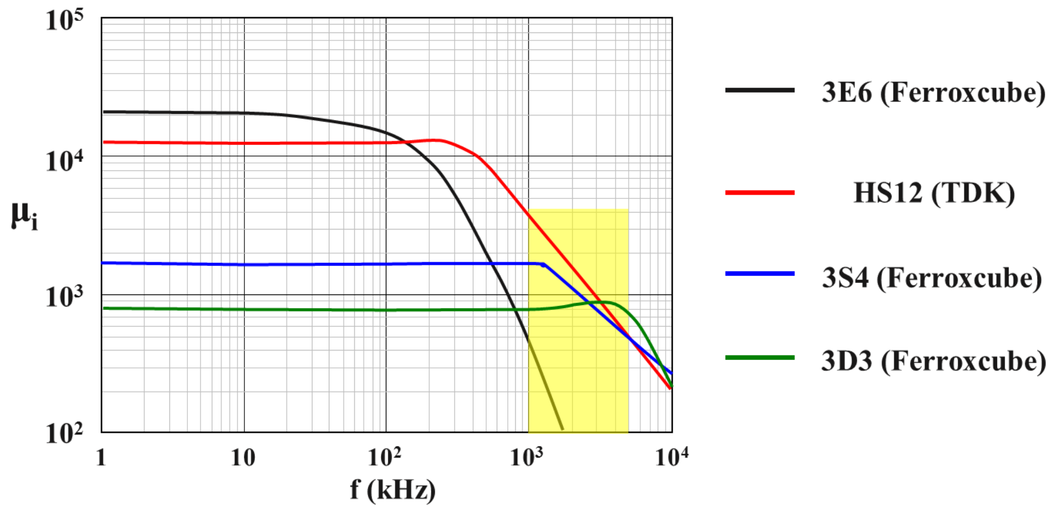


Figure 4.35 Choke material comparison

To reduce the volume and footprint of the EMI filter, a smaller toroid core is preferred. Two stacked TC9.5/4.8/3.2 toroid cores are selected. The turns number for each winding is 40 and AWG 28 solid wire is used for the two windings. The basic parameters are listed in Table 4.2. The parasitic capacitance is around 15pF which is acceptable in this design. The prototype of the CM/DM choke is shown in Figure 4.36. The volume is 10 x 10 x 10 mm^3.

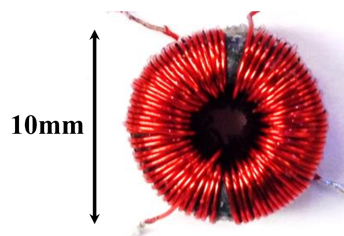
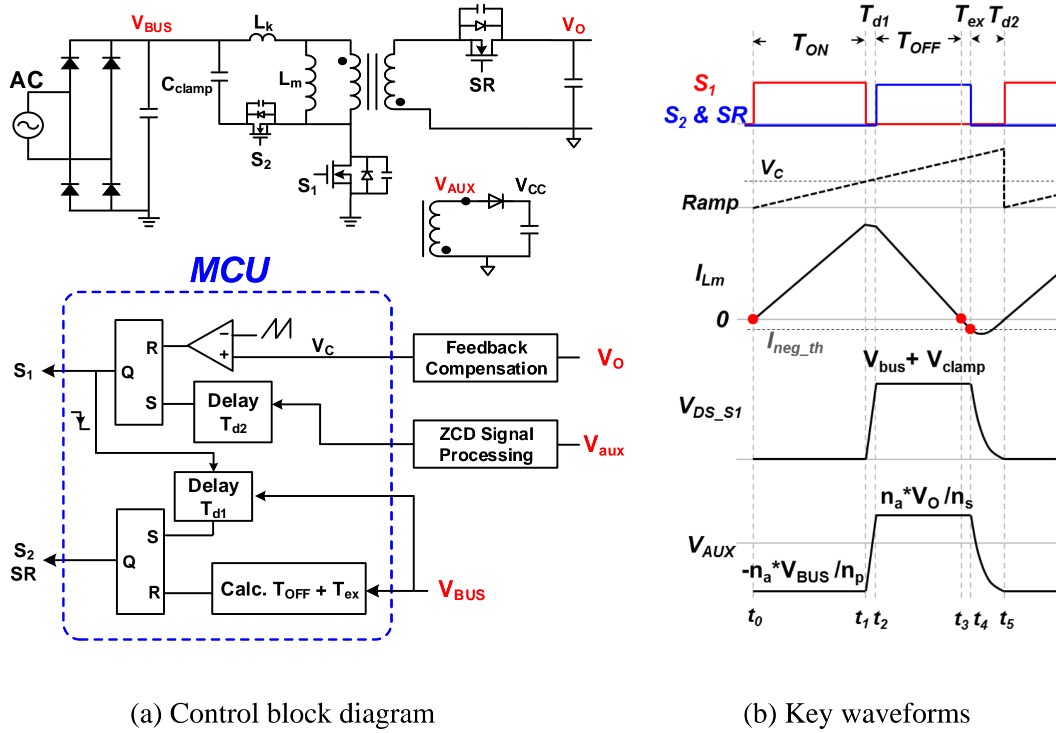


Figure 4.36 Picture of CM/DM choke for MHz flyback converter

4.2.4 High Frequency Control of Active Clamp Flyback Converter

High frequency operation requires dedicated control to achieve ZVS and time control among different switches. It is also important to have a proper control to deal with the

challenge of light load efficiency and standby power loss. Unfortunately, there is no commercial analog controller to support 1MHz switching frequency. Low cost microcontroller (MCU) has been used in adapter application, such as 29W adapter for new MacBook laptop. MCU provides voltage/current regulation and communication function which is now the trend of new generation of adapters. MCU also shows good performance at few MHz switching frequency in terms of calculation capability and capture of ZVS transition [D.24]. In order to demonstrate the advance of GaN devices and 1MHz system design, low cost MCU TMS320F28027 from Texas Instruments is employed to realize close loop control. The clock frequency of this MCU is 60MHz and it is impossible to complete real-time calculation, sensing with a switching period, namely 1us as of 1MHz switching frequency. It is practical to update calculation and sensing results in few switching period, e.g. 5~10 switching period. It is fare fast when the switching frequency is around 1MHz.



(a) Control block diagram (b) Key waveforms

Figure 4.37 Control of MHz active clamp flyback converter for adapter application

The control diagram is shown in Figure 4.37, as well as the key waveforms. The on-time of the main switch is determined by the output voltage feedback and the internal ramp of MCU. After the main switch is off, the clamping switch is turned on with ZVS after a preset delay T_{d1}, which is given in the following equation:

$$T_{d1} = \frac{2 \cdot C_{OSS} \cdot L}{T_{on}} \cdot \left(1 + \frac{V_{clamp}}{V_{BUS}}\right) \tag{4.2}$$

T_{d1} is related to the peak voltage and turn off current. It is obvious that T_{d1} need to vary with different load and input condition

Then the off time, which is the time period that magnetizing current decrease from peak to zero, can be calculated based on input, output voltage and on time, as shown in

$$T_{off} = \frac{V_{BUS} \cdot T_{on}}{n \cdot V_O} \tag{4.3}$$

In order to achieve zero-voltage switching for the primary switch, either the extra on time of the clamp switch or the dean-time T_{d2} should be carefully designed. There are two possible ZVS conditions, which depend on the input line voltage. When the input voltage is lower than secondary reflected voltage NVo, ZVS can be achieved naturally and T_{d2} is around half of the resonant period which is formed by L_m and C_{oss}. When the line voltage is higher than NVo, an extra on time of clamp switching is required to build negative current. The calculation can be vivid illustrated by resonant trajectory, as shown in Figure 4.38.

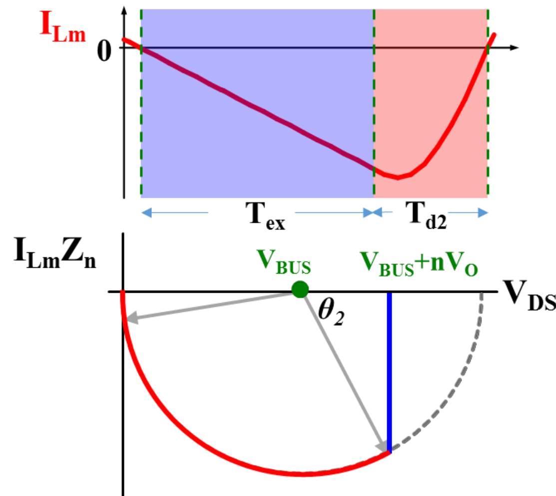


Figure 4.38 Trajectory analysis of resonance in active clamp flyback converter

The intial negative current is determined by the angular, indicated as θ_2 and it can be calculated as follows.

$$\theta_2 = \cos^{-1}\frac{nV_o}{V_{BUS}} \tag{4.4}$$

Then the extra on time of clamp switch can be derived based on θ_2 and resonant period formed by L_m and C_{oss}.

$$T_{ex} = \tan\theta_2 \cdot \sqrt{L_m \cdot 2C_{OSS}} \tag{4.5}$$

After clamp switch is turned off, the magnetizing inductance resonates with junction capacitors of main switch and clamp switch. ZVS of main switch can be realized after a short delay, which is given as follows.

$$T_{d2} = (\pi - \theta_2) \cdot \sqrt{L_m \cdot 2C_{OSS}} \tag{4.6}$$

It is noticed that the synchronous rectifier gate signal can be the same as the active clamp signal as long as the clamp capacitance is greater than 100nF, as shown in Figure 4.10.

Even though ZVS can be realized with accurate calculation, hardware based detection method is still desired to guarantee ZVS achievement, especially during start-up and load transient condition. Conventional detection method of ZVS achievement is based on the zero crossing point of auxiliary winding voltage. After a quarter of resonant period delay, the main switch can achieve valley switching (ZVS at low line input). This method works fine at low frequency since the resonant period is usually longer than few hundreds of nanosecond. However, it may lose ZVS at 1MHz frequency with digital control, as illustrated in Figure 4.39.

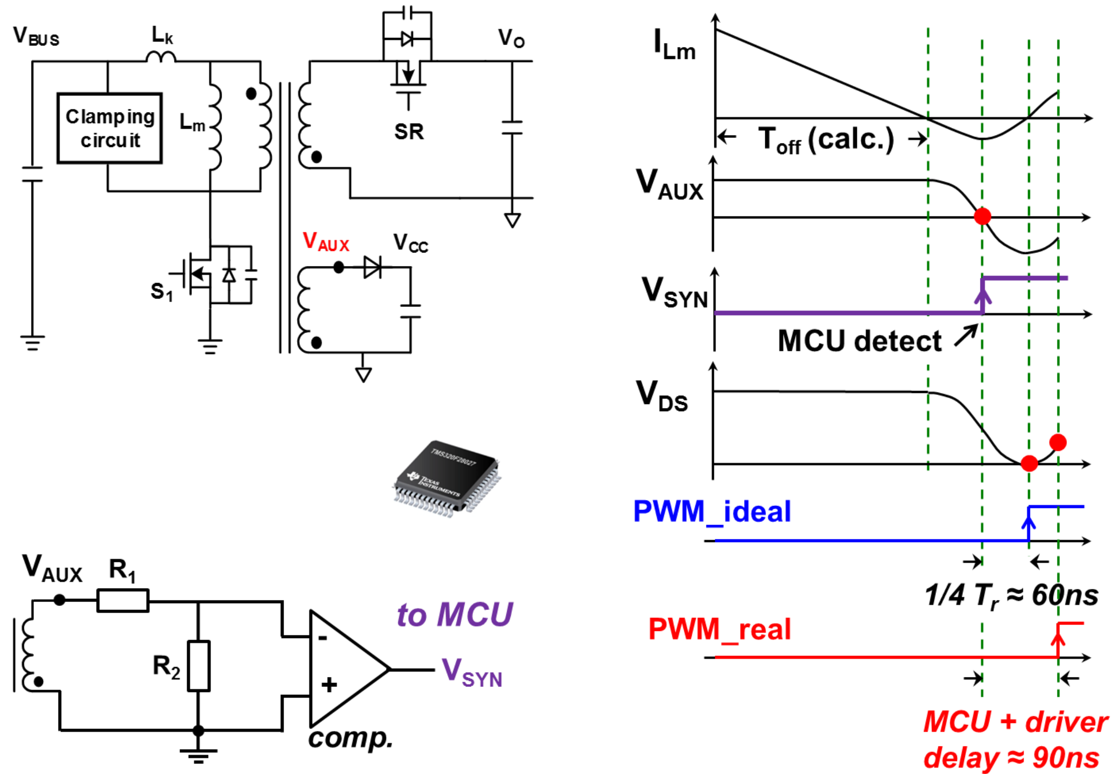


Figure 4.39 Conventional ZVS detection using auxiliary winding voltage

The auxiliary winding voltage is sensed by MCU with a voltage divider, and it is compared with zero reference and generate a V_{syn} signal. MCU is supposed to deliver PWM signal after a 60ns delay (considering processing time and gate driver delay) at the zero-voltage instant. However, the PWM is actually send to the gate 90ns after V_{syn} signal. The drain-source voltage rises back and induces turn-on switching due to too much delay. The issue is obviously newly raised by high frequency operation, but it can be relieved by the proposed method, which is demonstrated in Figure 4.40.

The proposed method is still based on the auxiliary winding voltage, but with a paralleled RC branch as shown in Figure 4.40. Instead of sensing the voltage of the divider, the voltage across the R_3 is send to MCU. As long as the voltage across the auxiliary

winding changes, for example, from high to low, the voltage across R3 and C1 also changes simultaneously. As a result, a current is induced in the RC branch and the voltage across R_3 immediately drops to negative voltage which is clamped by the diode. V_{syn} is generated right after the instant that V_{c-} goes to negative, which is almost the same time instant that V_{aux} drops. By sensing the RC branch voltage, it allows around 110ns delay, which is sufficient for MCU processing time and gate driver propagation delay at 1MHz switching frequency.

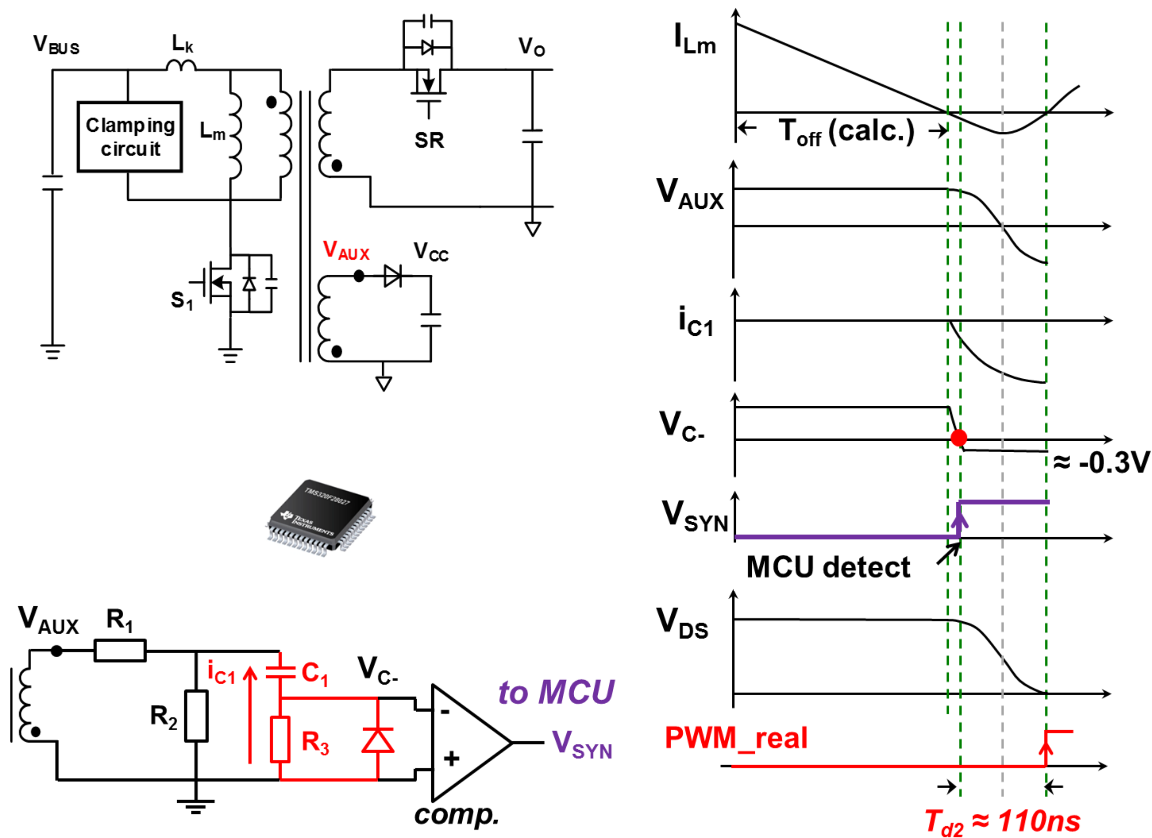


Figure 4.40 Proposed ZVS detection method

Another challenge of MHz operation of active clamp flyback converter is the light load efficiency optimization. The efficiency drops dramatically at light load condition with conventional control strategy, which is fixed frequency complementary control. The

circulating energy increases significantly at light load and thus increases the system conduction loss. On the other hand, the switching frequency increases significantly at light load condition due to the nature of CRM operation, as shown in Figure 4.37(b). The turn-off switching loss and driving loss increase proportionally with switching frequency, and therefore, the converter efficiency also drops sharply at light load.

In order to solve the light load efficiency issue, a novel control strategy is proposed in [D.25], and the key waveforms are shown in Figure 4.41. In the proposed control method, the auxiliary switch is turned on for a short time before the main switch is turned on. The leakage inductance energy is still recycled by the clamp capacitor and it is used to help achieve the soft switching of the main switch. However, it avoids the circulating energy in the resonant tank compared to the conventional complementary control method. Furthermore, the proposed control scheme can be adopted to variable frequency control to reduce the frequency related loss and improve light load efficiency.

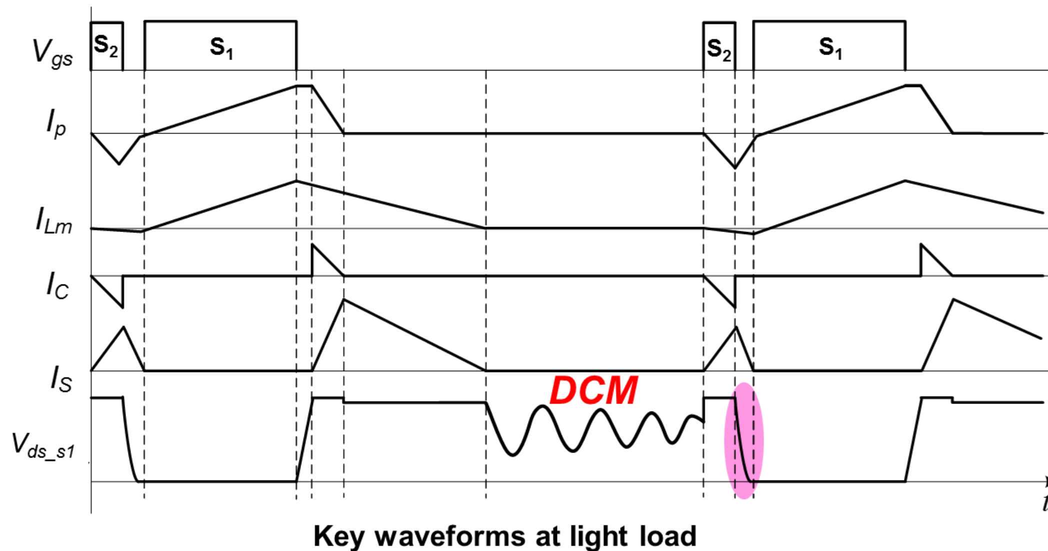
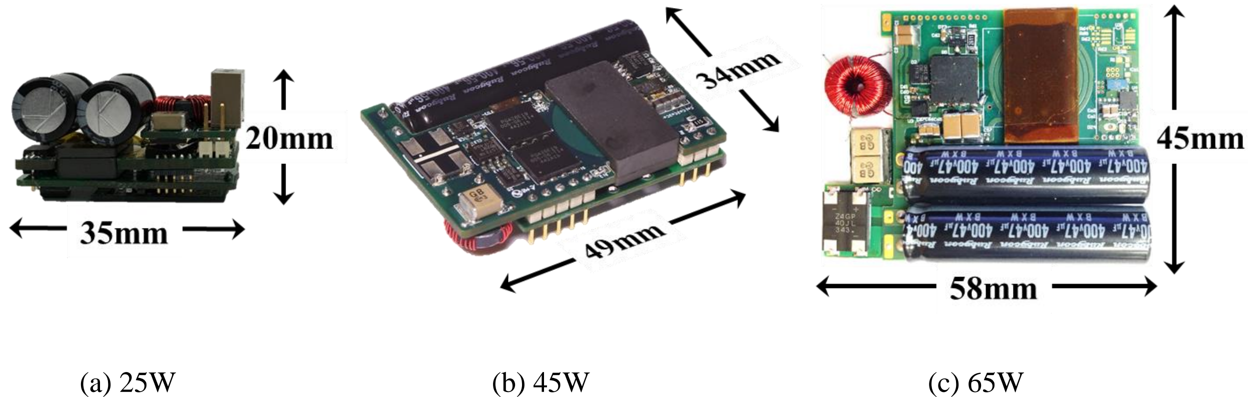


Figure 4.41 Proposed DCM clamp method [D.25]

4.2.5 Experiments Results and Discussion

In order to verify the feasibility of MHz active clamp flyback converter design, three prototypes with 25W, 45W, and 65W output are developed as shown in Figure 4.42.



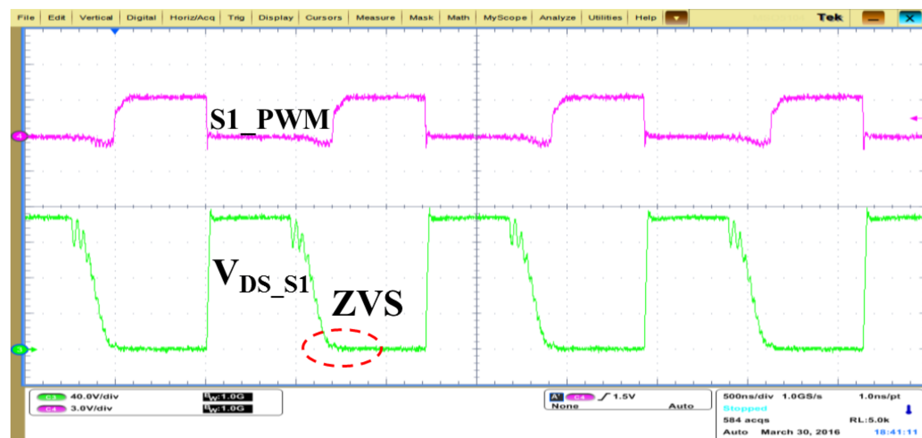
(a) 25W (b) 45W (c) 65W

Figure 4.42 Three prototypes employs MHz active clamp flyback topology

Both primary and secondary switches uses GaN devices to reduce conduction and switching losses. Three different 600V GaN devices are applied as the primary main switch and active clamp switch in different power prototypes. The 150V eGaN from EPC is used as the synchronous rectifier. The transformer of each prototype is implemented with 6 layer PCB as shown in Figure 4.19. The power density excludes the case for each prototype is 30W/in^3, 44W/in^3, and 41W/in^3, respectively. They are at least three times higher than the state-of-the-art products.

Figure 4.44 shows the key experimental waveforms to compare the different ZVS detection method based on 65W prototype. It clearly shows that ZVS is lost with conventional ZVS detection method. The ring back voltage induces around 0.3W at 1MHz switching frequency. ZVS can be achieved with proposed detection method, as shown in Figure 4.43(b). It eliminates the turn-on switching loss and reduces the noise as well.

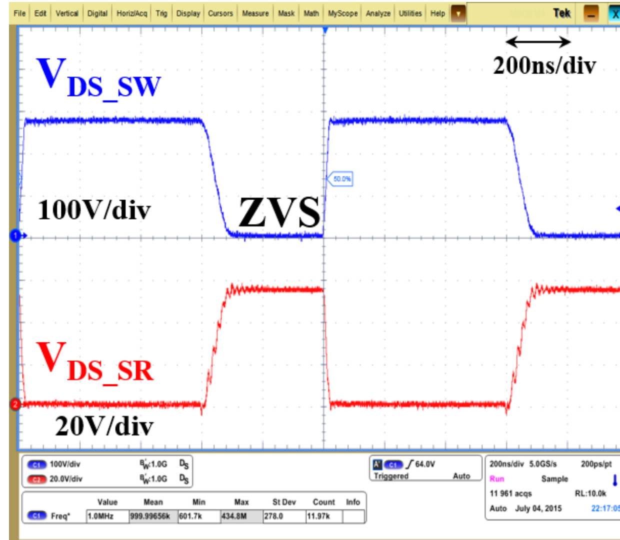
(a) Conventional ZVS detection method



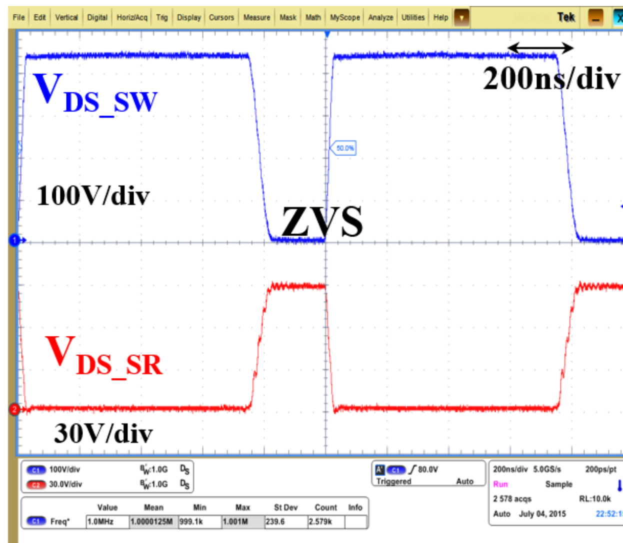
(b) Proposed ZVS detection method

Figure 4.43 Experimental waveforms of different ZVS detection method

Figure 4.44 shows the key waveforms at low line and high line input condition. The voltage across the primary and secondary switches are quite clean, and ZVS can be achieved over wide input range. The experimental waveforms of the other two prototypes are similar to 65W.



(a) Key waveforms at 110V_{AC}

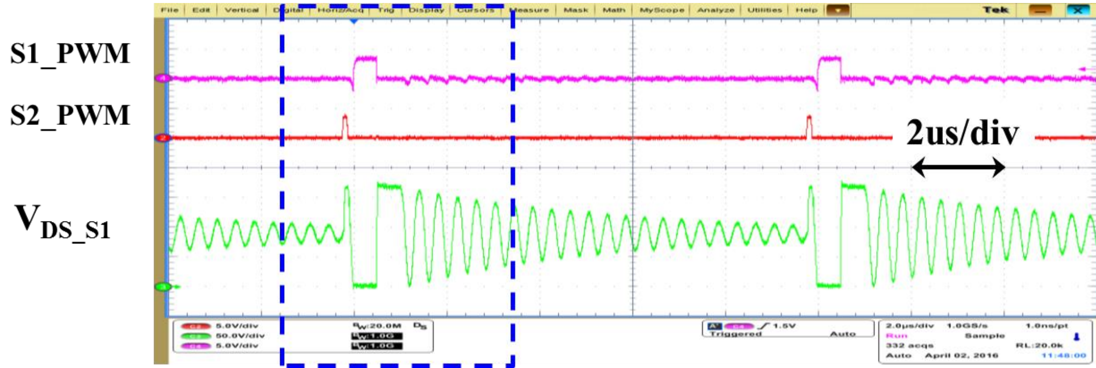


(b) Key waveforms at 230V_{AC}

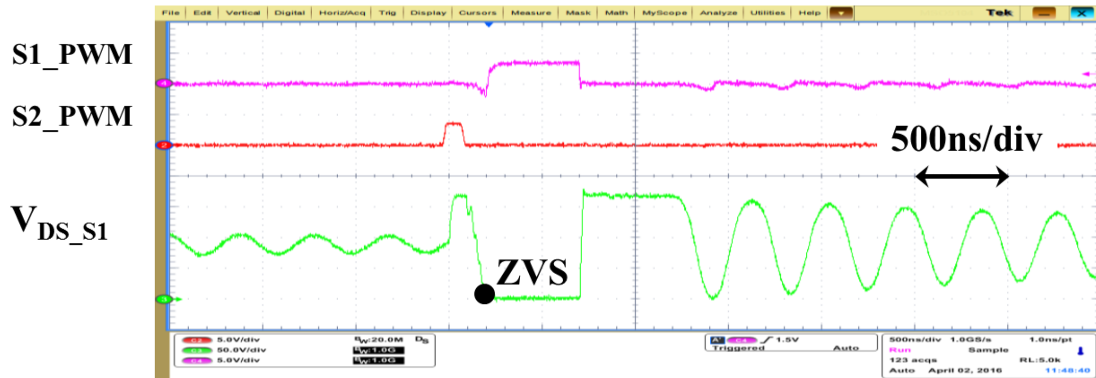
Figure 4.44 65W prototype experiment waveforms

Figure 4.44 shows the key waveforms at light load condition. The DCM clamp method is adopted in order to reduce switching frequency as well as reduce circulating energy. The switching frequency reduces to 100kHz at 10% load. ZVS is stilled achieved by this control

strategy. The efficiency of proposed method at 10% load is higher than 80%, while it is below 60% with conventional control method.



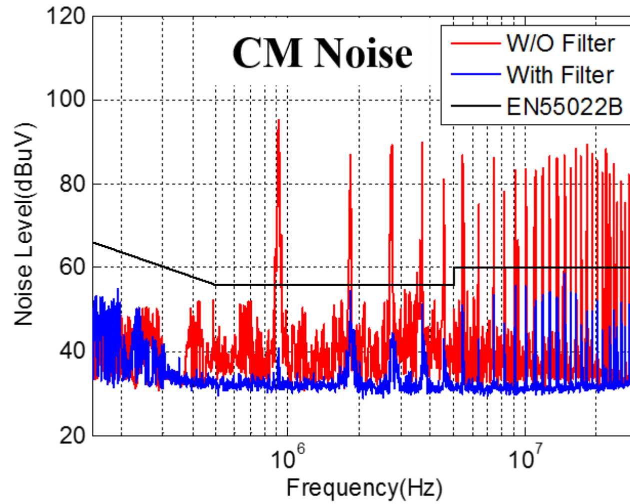
(a) Proposed DCM clamp method to improve light load efficiency



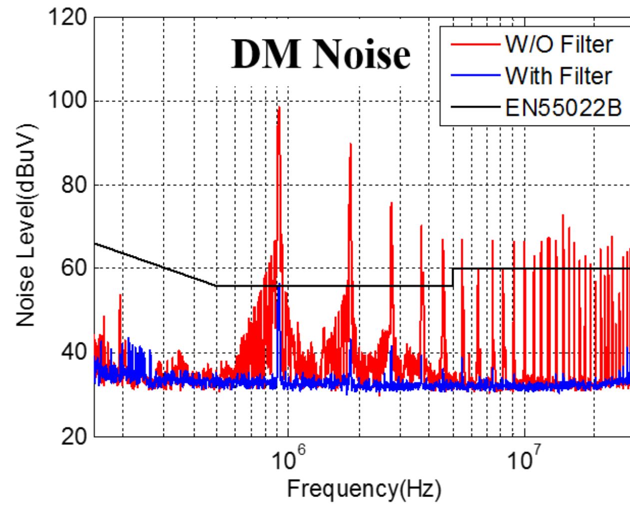
(b) Details of ZVS achievement with DCM clamp

Figure 4.45 Experimental waveforms of proposed DCM clamp method

Figure 4.46 shows the CM/DM noise spectrum with peak mode measurement under 110V_{AC} input full load output condition which is the worst case for the prototype design. The red curves are the results with shielding but without filters. The blue curves are the final results with EMI filter. It clearly shows that the blue curves are already lower than the quasi-peak standard.



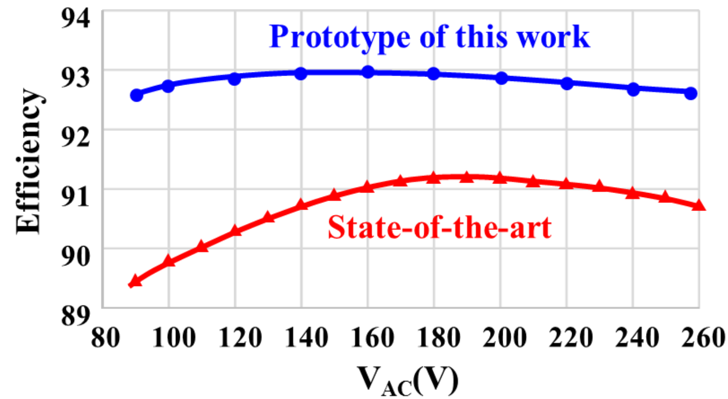
(a) CM noise measurement



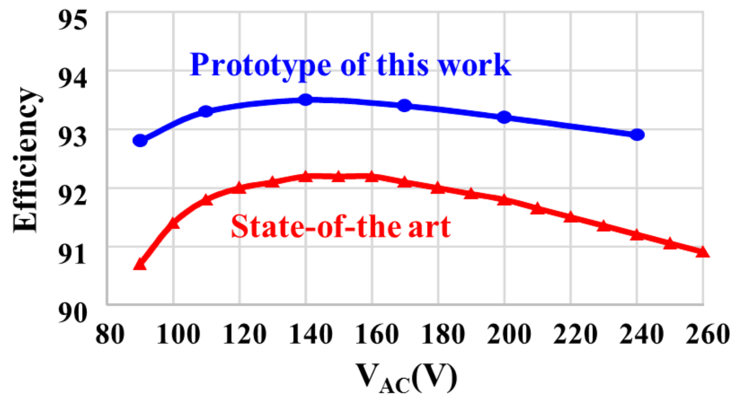
(b) DM noise measurement

Figure 4.46 Prototype EMI noise measurement with and without filter

The measured full load efficiency of 45W and 65W prototype over wide input range is shown in Figure 4.47. The efficiency of 25W prototype at low line full load condition is 91.5%. The efficiency of all three prototypes are 1~2% higher than the state-of-the-art product. It is worthwhile to point out that the power density improvement is accompanied with efficiency improvement due to thermal restriction.



(a) 45W prototype



(b) 65W prototype

Figure 4.47 Efficiency comparison of the prototype and state-of-the-art products

4.3 Universal adapter design for a wide power range

Even though active clamp flyback topology can achieved much higher efficiency and density compared to the state-of-the-art products, there is still room for further improvements. The areas that need improvements include:

1) The bulky electrolytic capacitor occupies more than 40% of the total volume.

2) The diode bridge consumes more than 2% of the total input power.

3) The intrinsic higher transformer winding losses that occur due to the nature of the flyback converter, especially at MHz frequencies.

4) Flyback converter is only suitable for power below 75W where power factor correction is not required.

Topologies for higher-power adapters are numerous. The current practice is to first choose a topology for a given application and optimize its performance. Standardization of the topology for a wide range of power levels and applications is highly desirable for future endeavors. Furthermore, due to the competitive nature of the products, improvements in efficiency and power density have to be achieved without a significant impact on the cost. With that in mind, the proposed universal adapter design to be developed in this work aims at achieving a power density of up to4/in3 along with significant efficiency improvements.

4.3.1 System Structure of Proposed Universal Adapter

The proposed system structure of universal adapter is based on a two-stage approach, as illustrated in Figure 4.48. The first stage is a bridgeless totem-pole rectifier, where the diode bridge is replaced by active switches with an efficiency improvement around 0.5~1%. This topology is not practical for silicon devices due to its excessive switching losses and body diode losses. However, it is deemed very effective for GaN devices operating in the multi-megahertz range [D.21]. The first stage serves another two important functions. One is the output voltage regulation, and the other is input harmonic current injection. The major burden of output voltage regulation is shifted to the first stage, and the output ripple requirement is also applied to the bus voltage ripple. Due to the strict ripple requirement, the bus capacitor is usually large. However, line-frequency harmonics can be injected in a

manner that can reduce the bulk capacitor. The second stage is the unregulated or semi-regulated LLC resonant converter, which has been demonstrated as one of the most efficient topologies for high frequency applications [D.22]. The LLC converter always operates at the resonant frequency, in such a way, it features ZVS on the primary side switches while ZCS for secondary rectifiers. The anticipated efficiency of the second stage is above 98% at 1MHz switching frequency.

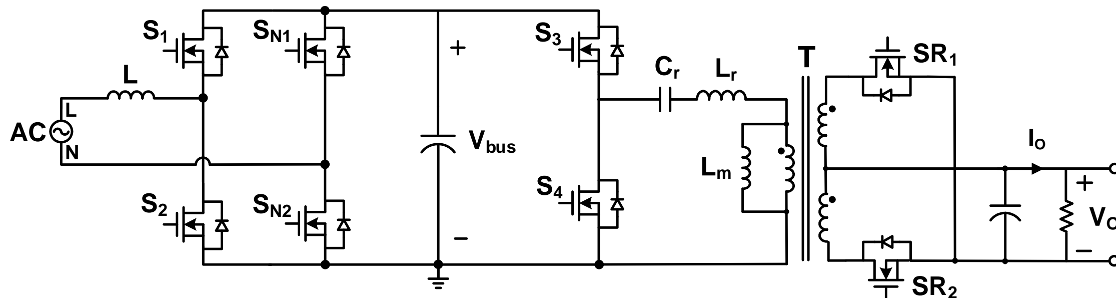


Figure 4.48 Universal two-stage structure for adapters using a wide power range

4.3.2 First Stage: Totem-pole Bridgeless Rectifier with Harmonic Injection

The totem-pole bridgeless rectifier has been proven as the most efficient topology with the least component count [D.21]. For MHz operation, CPES demonstrated that zero-voltage switching (ZVS) is deemed necessary to eliminate the excessive turn-on switching loss. Furthermore, ZVS can also alleviate switching noises associated with high dv/dt. The CRM mode operation was adopted to achieve ZVS. However, when the input volt-age is higher than 0.5 Vbus, ZVS cannot be realized fully. To achieve ZVS in the high line, the bridgeless rectifier has to operate in reverse-conduction mode for a brief interval. Controlling the timing is critical to avoid excessive circulating current, as illustrated in detail in [D.21].

One of the important benefits of the proposed two-stage approach is that when the first stage is operated with a certain amount of harmonic current injection, the bus capacitance can be reduced significantly. The harmonic current injection can be used both below 75W and above 75W. The strategy of harmonic current injection is different between below and above 75W adapter which is majorly restricted by the harmonic standard IEC611000-3-2.

For the adapters power below 75W which doesn't require high power factor and low total harmonic distortion (THD), and thus larger magnitude and higher orders of harmonic currents can be injected to help reduce the bus capacitance. The basic principle and relationship between harmonic injection and bus capacitance reduction are shown as below.

To consider the harmonic currents, the input line current can be expressed as

$$i_{ac}(t) = \sum_{n=1}^{k} I_{mn} \sin(\omega t) \tag{4.7}$$

where I_{mn} is the amplitude of the nth harmonic current, ω is the angular frequency of the AC input, n is the harmonic order, and k is a constant to express the highest harmonic order.

The instantaneous input power is the product of input $v_{ac}(t)$ and $i_{ac}(t)$, which is

$$p_{acn}(t) = V_m \sin(\omega t) \sum_{n=1}^{k} I_{mn} \sin(\omega t) \tag{4.8}$$

where V_m is the amplitude of the line voltage source.

According to equation (4.x), the instantaneous input power with different combination of harmonic currents injection can be calculated. The instantaneous input power without harmonic injection can be expressed as

$$p_{ac_1}(t) = V_m [I_{m1} \frac{1-\cos(2\omega t)}{2}] \tag{4.9}$$

Similarly, the instantaneous input power with injection of only third-order harmonic current can be described as

$$p_{ac_1+3}(t) = V_m[I_{m1}\frac{1-\cos(2\omega t)}{2} + I_{m3}\frac{\cos(2\omega t)-\cos(4\omega t)}{2}] \quad (4.10)$$

If I_{m1} is equal to I_{m3}, then equation (4.X) can be rewritten as

$$p_{ac_1+3}(t) = V_m[I_{m1}\frac{1-\cos(4\omega t)}{2}] \quad (4.11)$$

It is obvious that the frequency of the input power increases from double line frequency to 4th line frequency as shown in Figure 4.49.

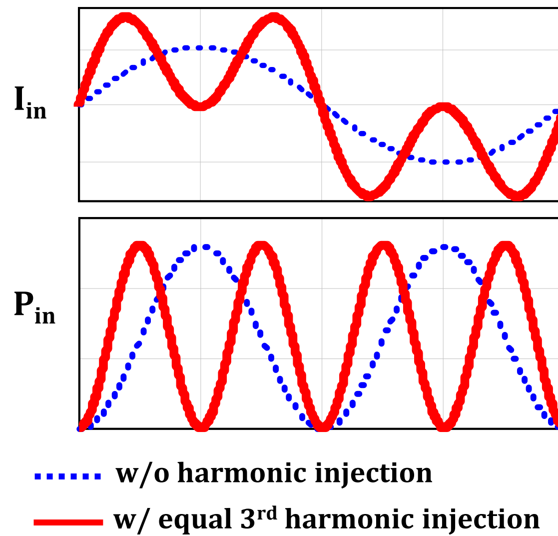


Figure 4.49 Impact of harmonic injection on input power for below 75W adapters

If inject more high order harmonics with same magnitude with I_{m1}, then the instantaneous input power can be calculated as

$$p_{ac_1+\cdots+n}(t) = V_m\{I_{m1}\frac{1-\cos[(n+1)\omega t]}{2}\} \quad (4.12)$$

From equation (4.X), it can be seen that all the harmonic components less than $(n+1)^{th}$ order would be eliminated with injecting same magnitude current up to n^{th} order. It is obvious that the bus capacitance reduces with higher input power frequency. The relationship of cap reduction with harmonic injection up to 7th order based on the 65W adapter is shown in Figure 4.50. More than 70% bus cap reduction is expected with only 3rd harmonic current injection compared to active clamp flyback approach.

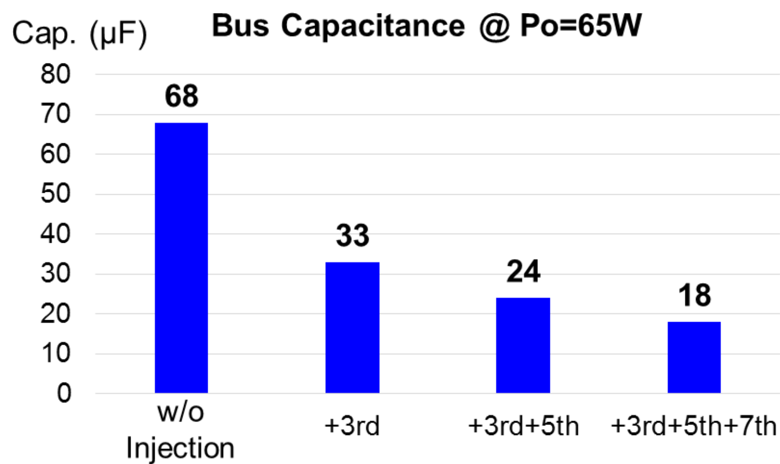


Figure 4.50 Relationship of bus cap reduction with harmonic injection

The disadvantage of harmonic injection is the increase of conduction loss on inductor and semiconductor devices. Figure 4.51 shows the efficiency analysis of the first stage with different harmonic injection. Generally speaking, efficiency drops 1% with every higher order harmonic current been injected. Inject only 3rd harmonic is preferred in 65W adapter de-sign for both efficiency and density considerations.

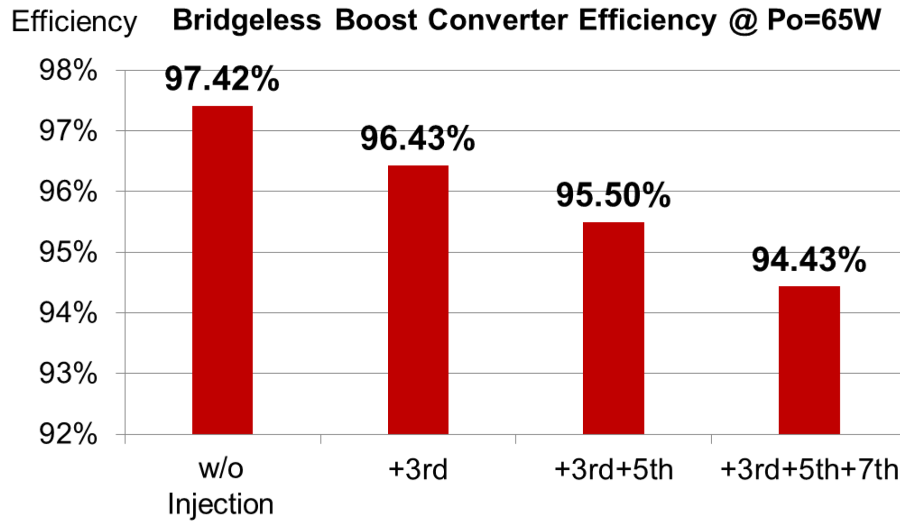


Figure 4.51 Relationship of first stage efficiency with harmonic injection

For the adapters power above 75W which are belong to class D equipment, the input current should meet IEC61000 3-2 standard. However, there is still room for mild harmonic injection in order to reduce the bus capacitor, as shown in Figure 4.52. The input current is modified from sinusoid shape to trapezoid shape. The input delivers less power at peak point but more power near the zero-crossing area. This control strategy helps to reduce the pulsation of the input power and therefore reduce the bus cap. Actually the magnitude of the harmonic current can be controlled following the standard with reasonable margin. The similar concept has been applied to LED lighting application in order to eliminate the electrolytic capacitor [D.23].

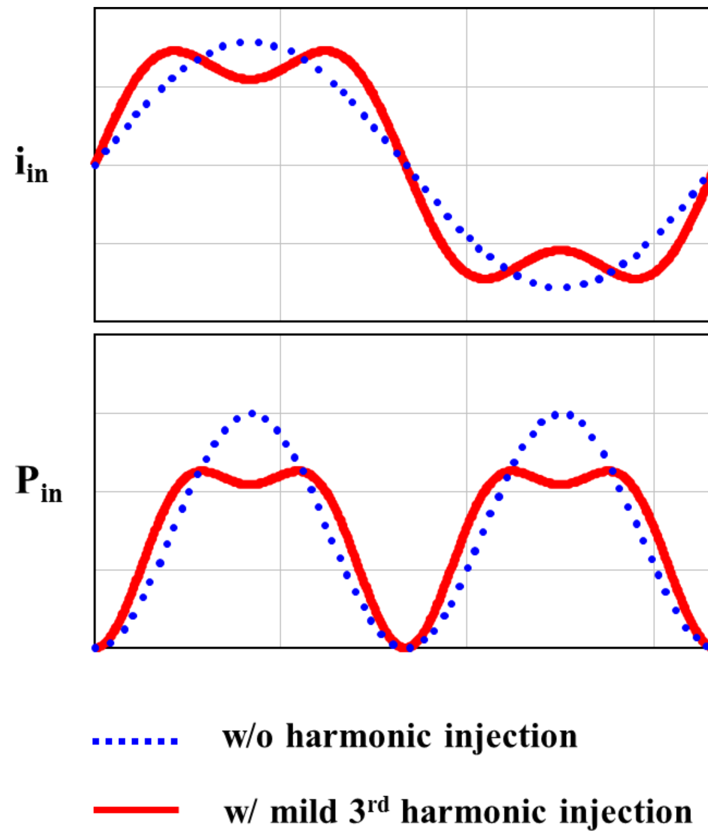


Figure 4.52 Impact of harmonic injection on input power for adapters above 75W

Figure 4.53 shows the bulk capacitors reduction with harmonics injection based on a 150W adapter. It is expected about 25% bus capacitor reduction with only 3rd harmonic injection. Injecting more high order harmonics will slightly reduce capacitance since the allowed injection magnitude of higher order harmonics becomes much smaller according the standard.

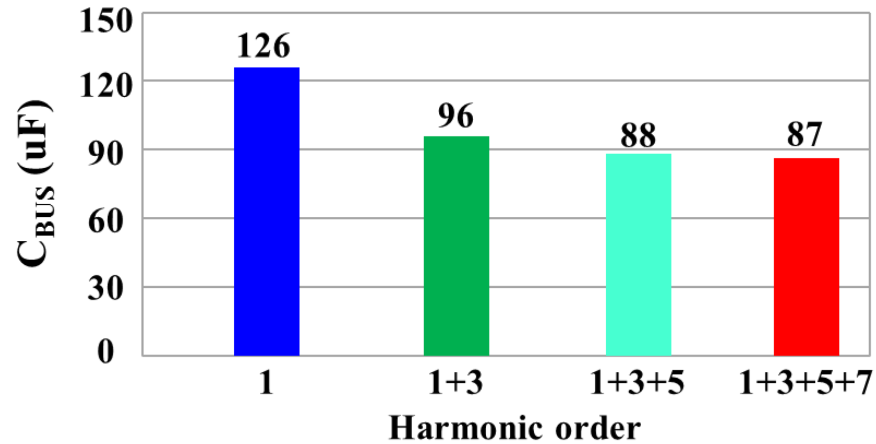


Figure 4.53 Bus capacitance reduction with harmonics injection

The harmonic current injection also impacts the switching frequency over line cycle, which is illustrated in Figure 4.54. With higher order harmonic injected to the rectifier stage, the switching frequency at zero crossing period drops significantly. The switching related loss slightly reduces. However, EMI noise spectrum varies with different harmonic injection and it determines the filter design. Figure 4.55 shows the simulation result comparison of DM noise spectrum among different harmonic injection condition. For the case without harmonic injection, the corner frequency is determined by the 1MHz switching noise if one-stage filter is applied, which provide 40dB/dec attenuation. For the case with only 3rd harmonic injection case, the switching frequency at middle line point slightly increases, but the current amplitude reduces compared with no harmonic injection. As a result, the noise amplitude also reduces. The worst case of noise occurs at the peak current region at where the switching frequency is around 650kHz. The corner frequency of the filter is determined by the noise at this frequency, and it is quite similar with no harmonic injection case. For harmonic injection up to 7th case, more power is desired to be delivered near the zero-crossing period and as a result, more lower switching frequency

noise occurs at this region. The corner frequency is determined by 350kHz, which occurs near zero crossing period. The corner frequency is definitely much lower than the case with only 3rd harmonic injection, which means the filter size is much larger.

Overall, only 3rd harmonic injection is applied taking consideration of bulky capacitor reduction and EMI filter size.

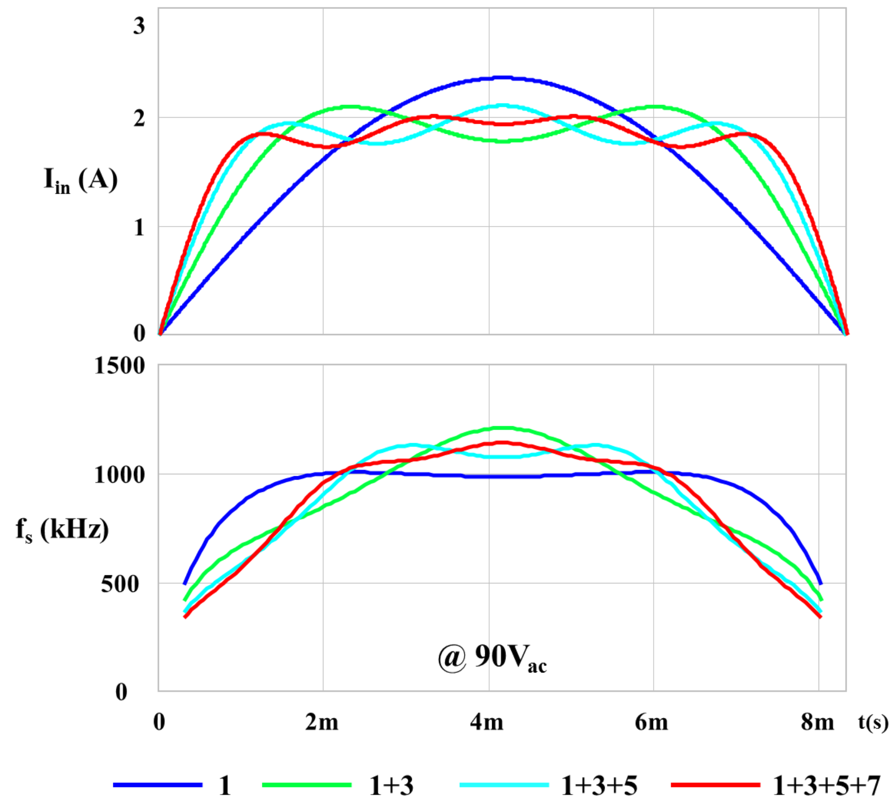
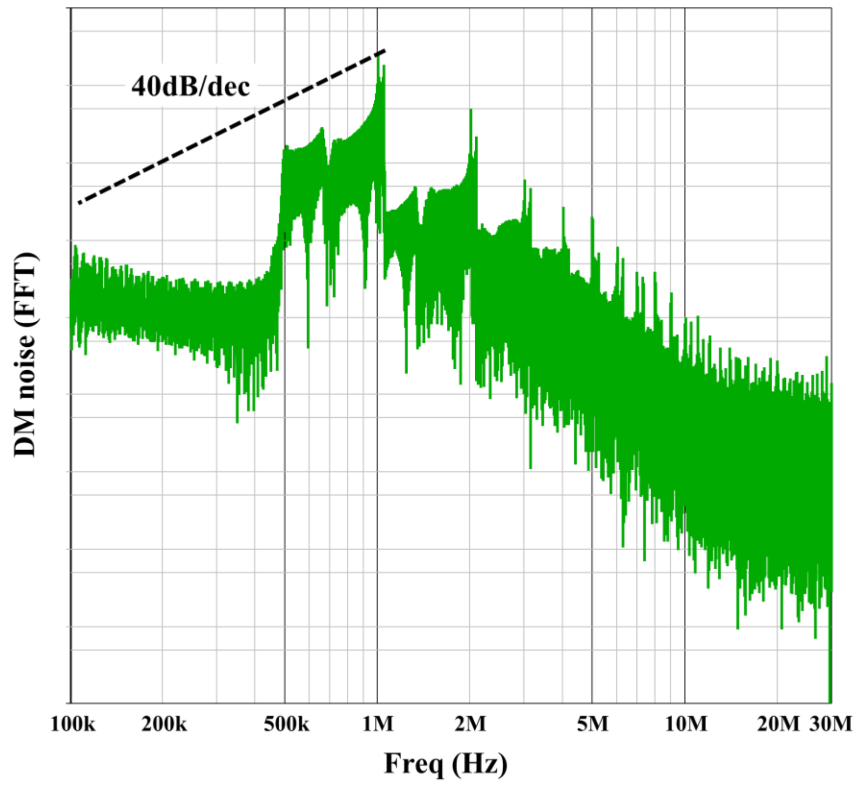
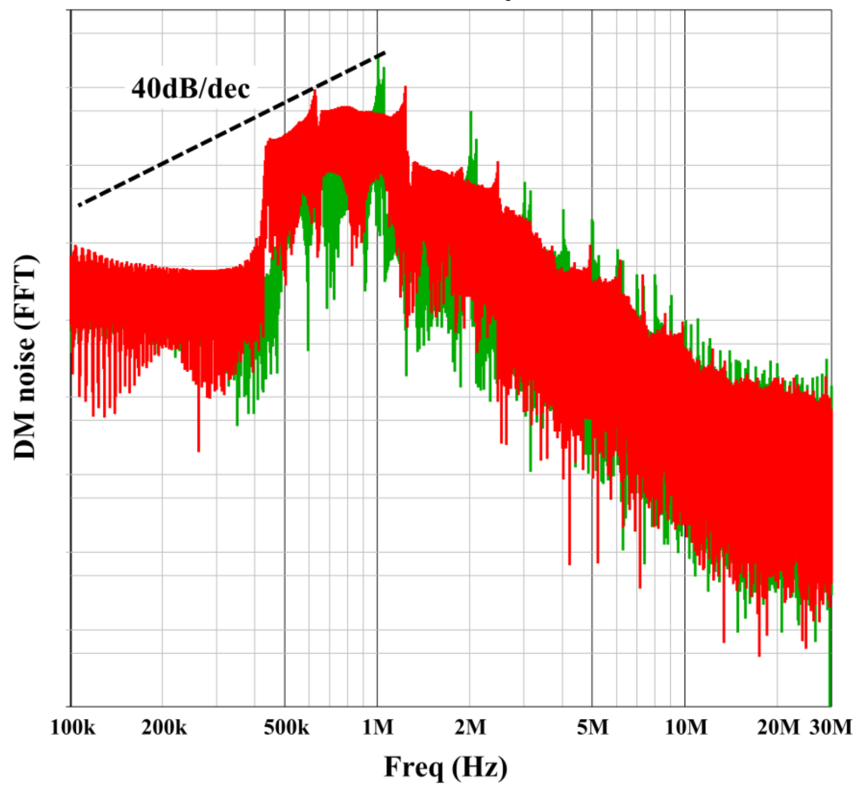


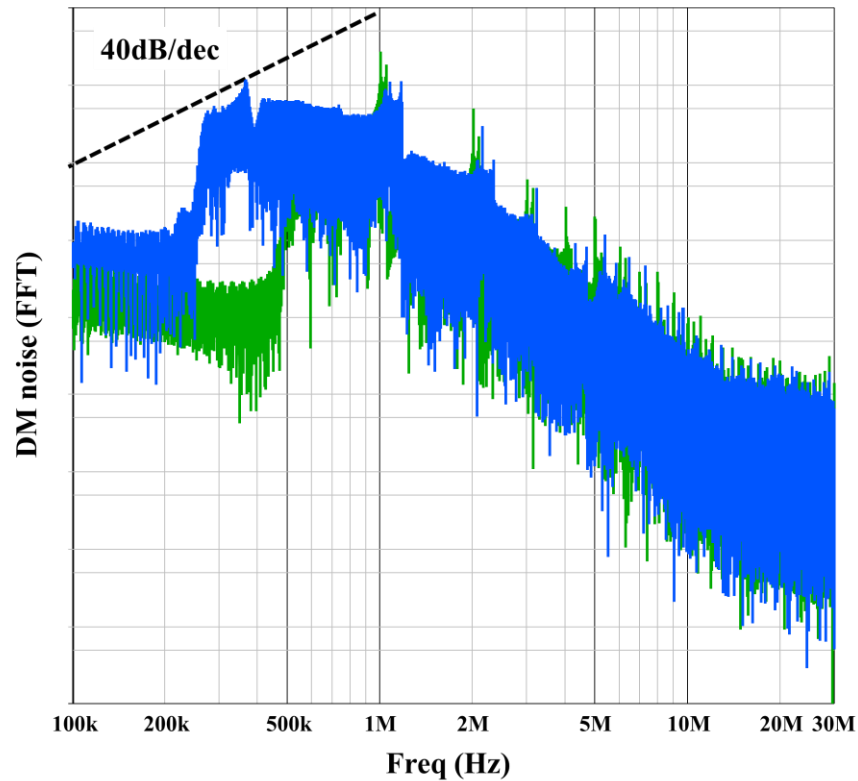
Figure 4.54 Impact of harmonic injection on switching frequency



(a) w/o harmonic injection



(b) with 3rd harmonic injection (green: no harmonic injection; red: 3rd harmonic injection)



(c) with 3rd, 5th, 7th harmonic injection (green: no harmonic injection; blue: 3rd+5th+7th harmonic injection)

Figure 4.55 Impact of harmonic injection on EMI noise spectrum

4.3.3 Second Stage: LLC-DCX

When the switching frequency is equal to the resonant frequency (including the dead-time), the LLC converter is at its most efficient operating point, as shown in Figure 4.56. The primary switches achieve ZVS and the synchronous rectifiers achieve ZCS. Therefore, the body diode conduction and reverse-recovery losses for the synchronous rectifiers are eliminated. Moreover, the driving signal of the synchronous rectifier can be synchronized with primary signal.

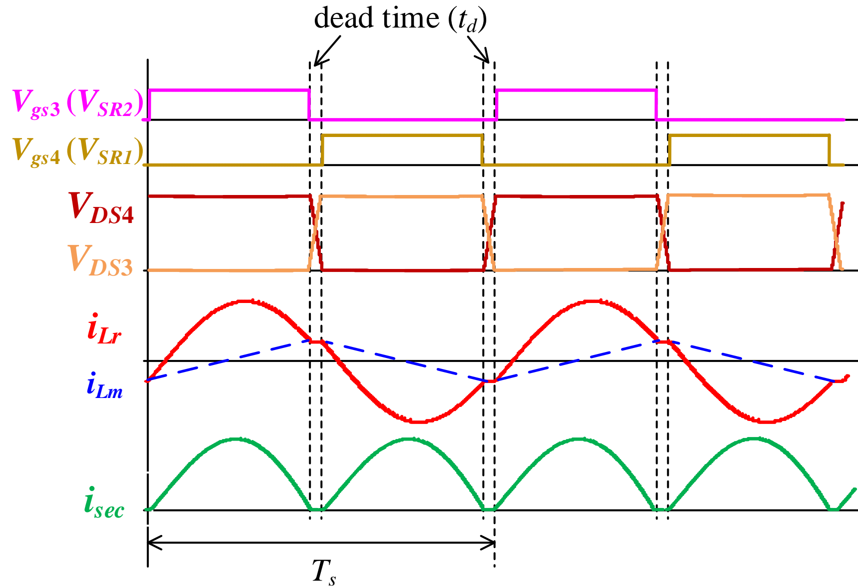


Figure 4.56 Key waveforms of LLC converter operating at Fs=Fo

The normalized voltage gain of LLC-DCX operates at resonant frequency is 1. The output voltage of adapter is typically 20V, and the output voltage of totem-pole rectifier is usually around 400V, therefore the turns ratio of LLC-DCX transformer is 10 with a center-tap structure, which is preferred in adapter application. A design example of 150W LLC-DCX transformer is illustrated to show the optimization procedure.

LLC-DCX transformer is implemented using PCB winding for efficiency, density and easy automation consideration. A customized ER shape core is applied in this design due to the similar reason mentioned in section 4.2.2. The core material is ML91S from Hitachi Metal, which has lowest core loss density at 1MHz frequency. SR devices and output capacitors are integrated into the secondary windings, as shown in Figure 4.57, in order to eliminate termination related winding losses and via loss and to reduce leakage inductance [D.22]. The winding structure is similar to the flyback transformer shown in Figure 4.19 (a). Two shielding layers are added to block the CM noise.

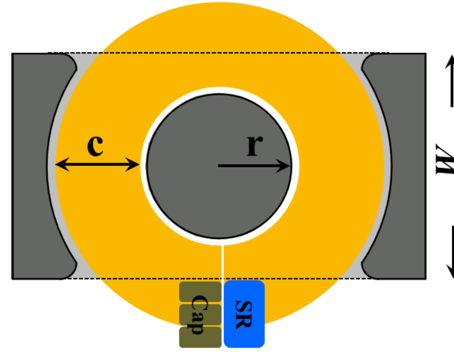


Figure 4.57 PCB winding based LLC-DCX transformer integrated SR and caps

The parameters of core determines the core loss and winding loss. The core loss can be derived from core loss density data and core volume. The winding loss can be derived based on the transformer eddy current model in [D.26]. The winding thickness is 2oz for all layers, which is the optimal value for 1MHz switching frequency based on FEA 3D simulation results.

The total transformer loss versus different parameters could be plotted as shown in Figure 4.58. The X-axis is the center leg radius r which reflects the cross-section area, the Y-axis is the winding window width c. Each solid line represents a given total transformer loss, while each dash line represents a given footprint. The loss curve and the footprint curve certainly have a tangential point, which are represents as the big dot in Figure 4.58. These dots represent the optimum designs, which have the lowest loss for a given footprint or the minimum footprint for a given loss.

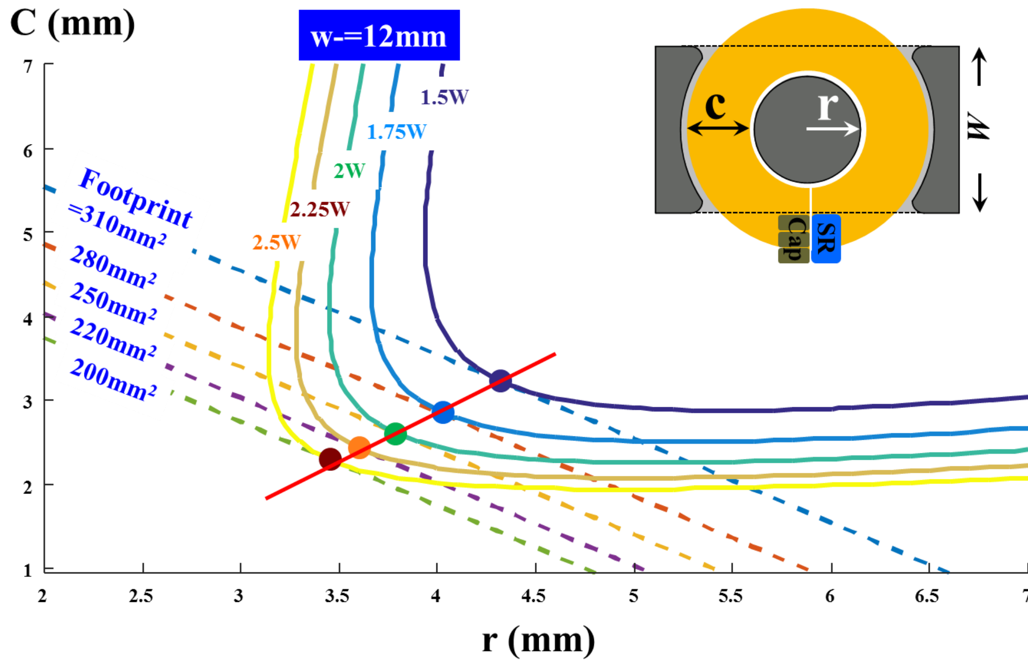


Figure 4.58 Transformer loss vs. core radius r and window width c

If plot these optimum design points in a graph of loss versus footprint, we get Figure 4.59. The optimum loss curve slightly shifts to smaller footprint with wider core width. Further increase core width will reduce the thickness of the outer leg, which increase the manufacturer difficulties. It is not necessary to select the lowest loss design. Instead, it is common to sacrifice a little loss to save footprint. In this application, the design around 300mm^2 is a reasonable tradeoff in terms of loss and footprint. Then the parameters of the core can be settled down as r =4.8mm, c =3.2mm, w =14mm.

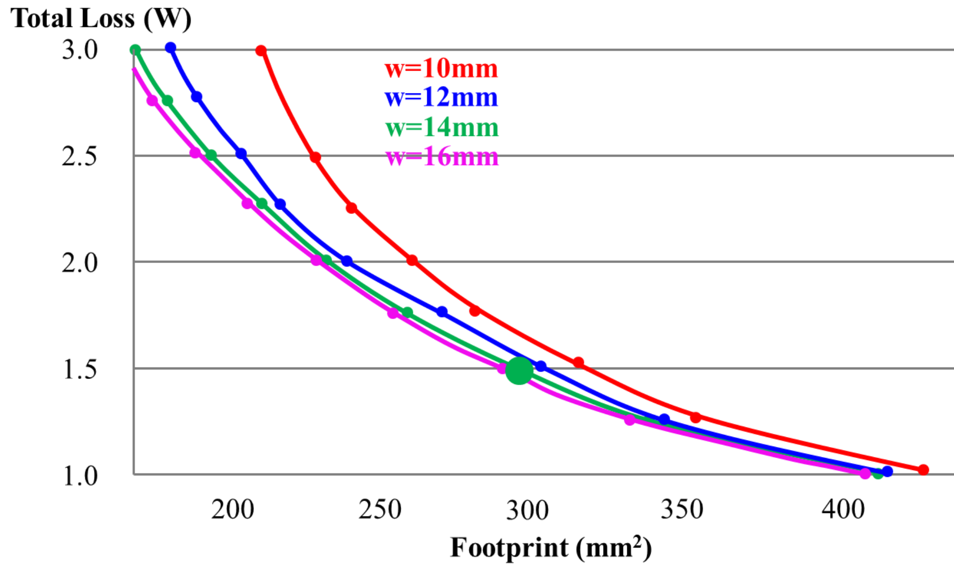
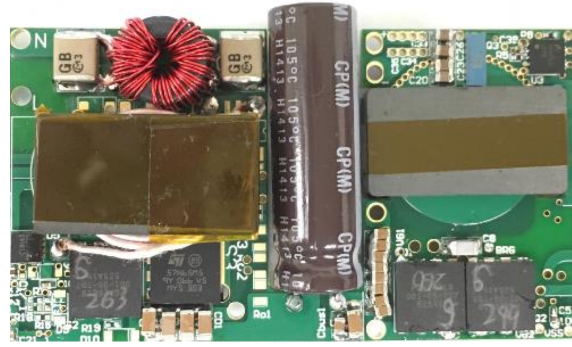


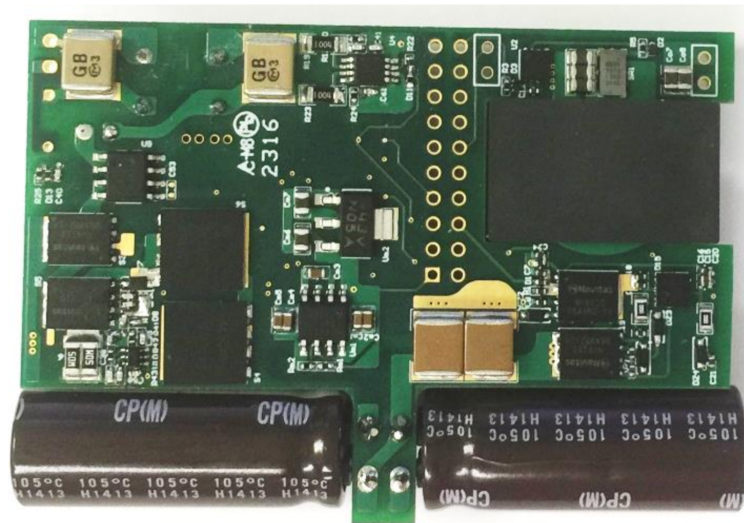
Figure 4.59 Transformer and footprint tradeoff

4.3.4 Experiment Results and Discussion

To verify the analysis and show the benefits of two-stage approach over flyback approach, two prototypes are built with GaN devices and operates at 1MHz and above, as shown in Figure 4.60. 600V GaN devices PGA26E19 from Panasonic are used in 65W prototype due to its best figure-of-merit. 600V GaN devices NV6115 from Navitas are used in 150W prototype due to its smallest footprint with integrated gate driver. 60V/2.6mΩ EPC2031 from EPC is used as the SR in both prototypes. The system is controlled by microcontroller TMS320F28027 from Texas Instruments with 60MHz clock frequency.



(a) 65W



(b) 150W

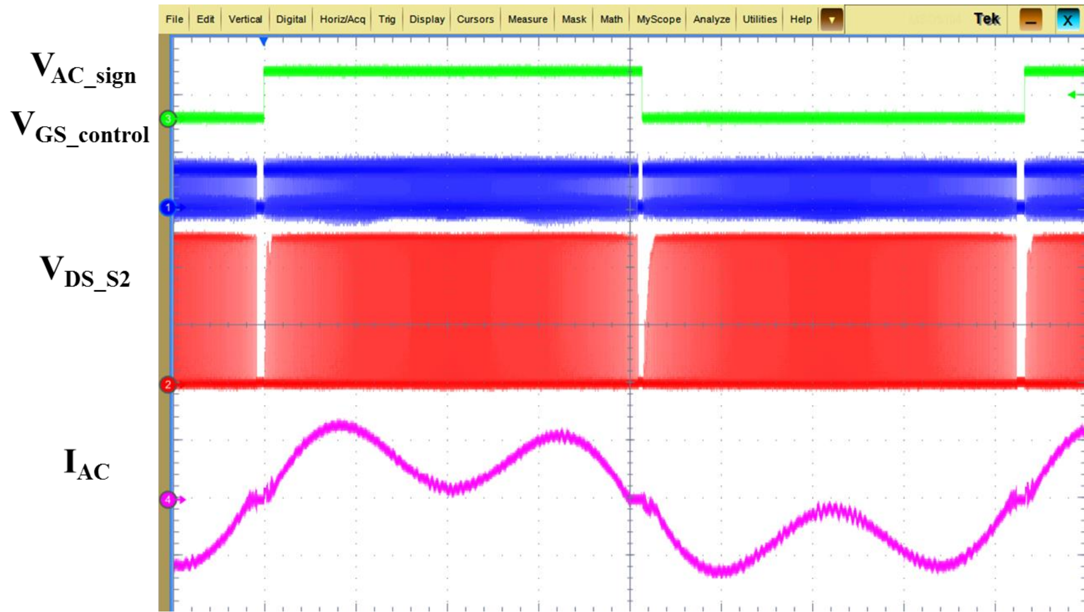
Figure 4.60 Two-stage prototypes

The key waveforms of the first-stage in two prototypes are shown in Figure 4.61. For 65W prototype, equal 3rd harmonic current is injected in order to eliminate double line frequency input power. The comparison of output voltage ripple with given bus capacitor (33uF) is shown in Figure 4.62. The output ripple requirement for adapter application is typically 1%, which means the bus voltage peak-peak ripple should be lower than 8V in the proposed two-stage solution. The ripple in the control strategy without harmonic

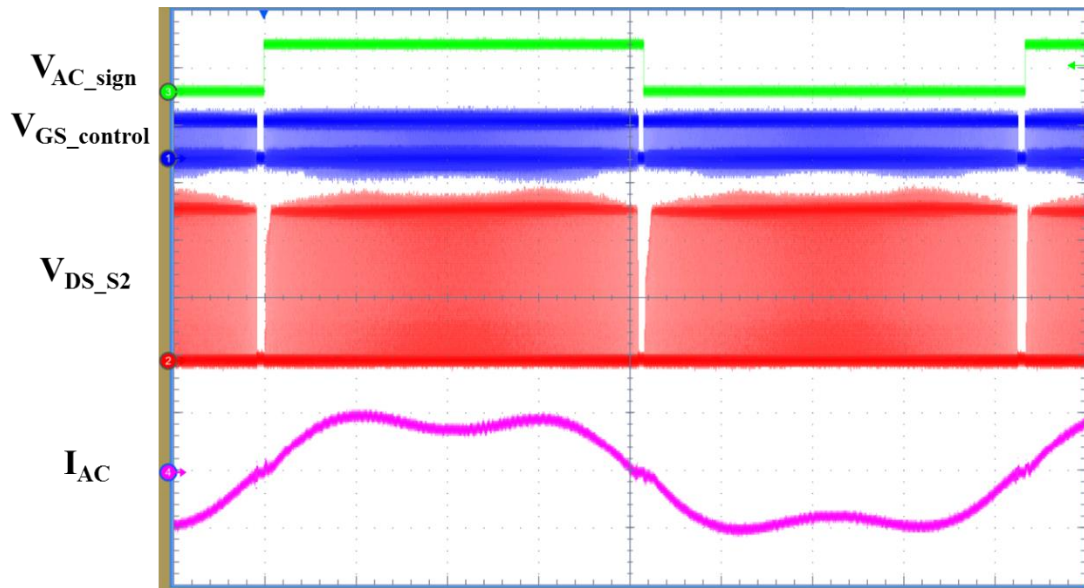
injection reaches 16V, which definitely requires the second stage has regulation ability. With equal 3rd harmonic injection, the experiment waveforms clearly shows that the double line frequency ripple is eliminated and only 4th line frequency is left, and therefore, the voltage ripple reduces to 8V, which just meet the design goal.

For 150W prototype, certain allowed 3rd harmonic current, which is determined by the IEC61000-3-2, is injected to help reduce bus capacitor. The measured power factor with 3rd harmonic injection is 96% and total harmonic distortion (THD) is 27%. The rms value of 3rd harmonic current is 0.45A, which is lower than the maximum allowed value 0.51A. The comparison of the output voltage ripple with given bus capacitor (100uF) is shown in Figure 4.63. The ripple in the control strategy without harmonic injection reaches 10V, while the ripple with harmonic injection reduces to 8V, which meet the ripple design requirement.

The output voltage ripple reduction with given bus capacitor can also translate to bus capacitor reduction with given ripple. Based on certain calculation, the bus capacitor can be reduced up to 70% with equal 3rd harmonic injection for adapters below 75W. For power levels above 75W, the bus capacitor can be reduced up to 25% with maximum allowed 3rd harmonic injection.

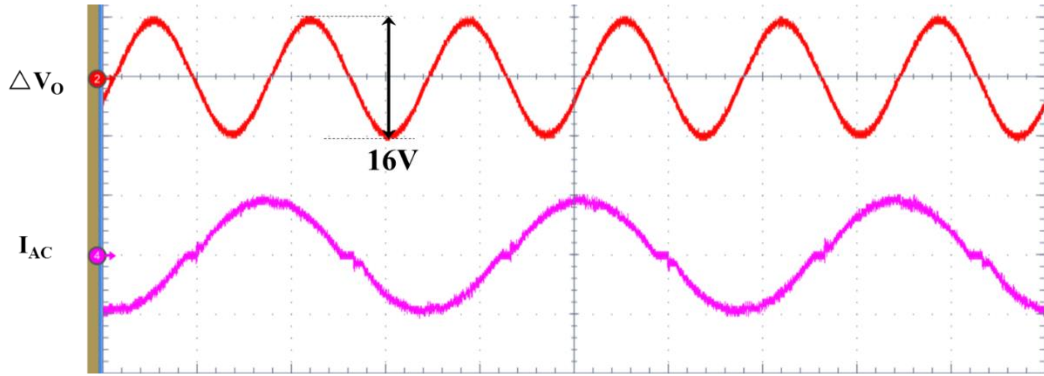


(a) 65W prototype with equal 3rd harmonic injection

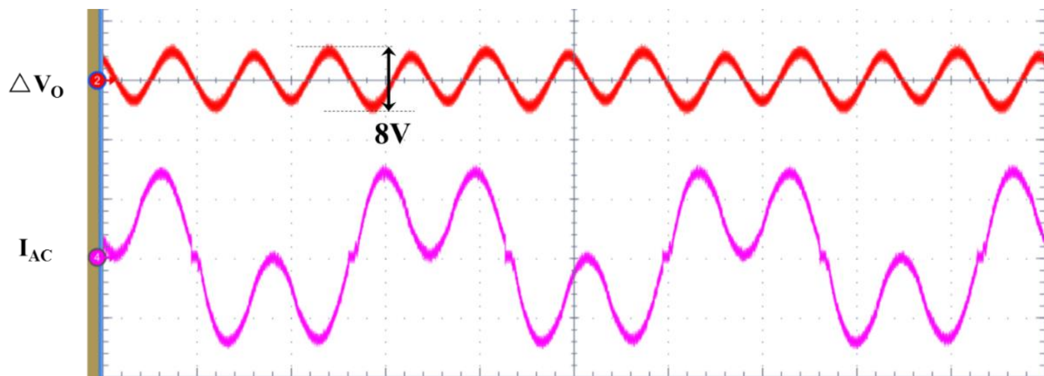


(b) 150W prototype with mild 3rd harmonic injection

Figure 4.61 Key waveforms of totem-pole rectifier

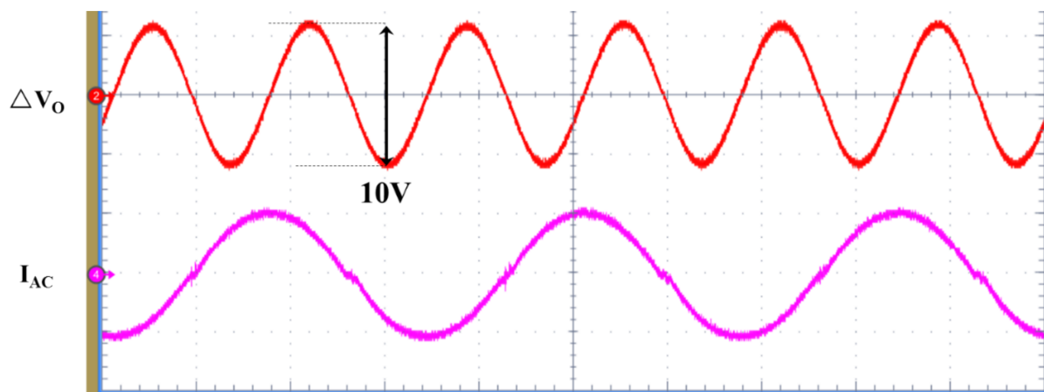


(a) w/o harmonic injection

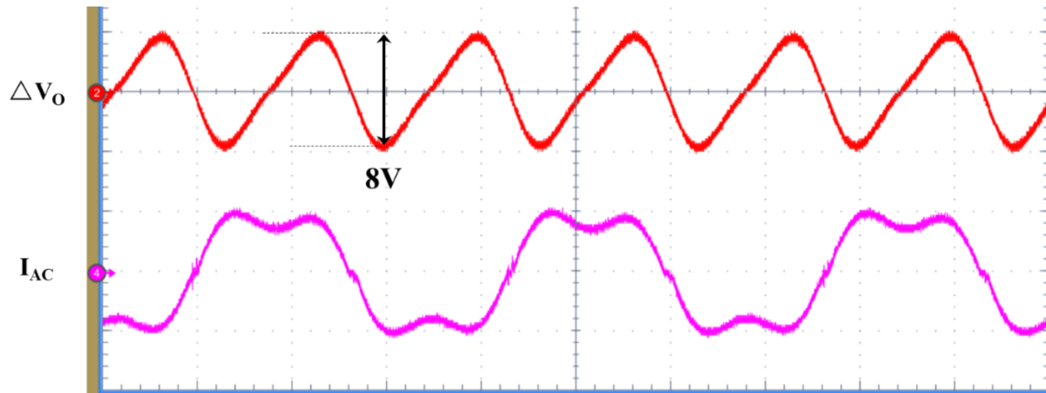


(b) w/ equal 3rd harmonic injection

Figure 4.62 Cap reduction/voltage ripple reduction with harmonic injection in 65W prototype



(a) w/o harmonic injection



(b) w/ mild 3rd harmonic injection

Figure 4.63 Cap reduction/voltage ripple reduction with harmonic injection in 150W prototype

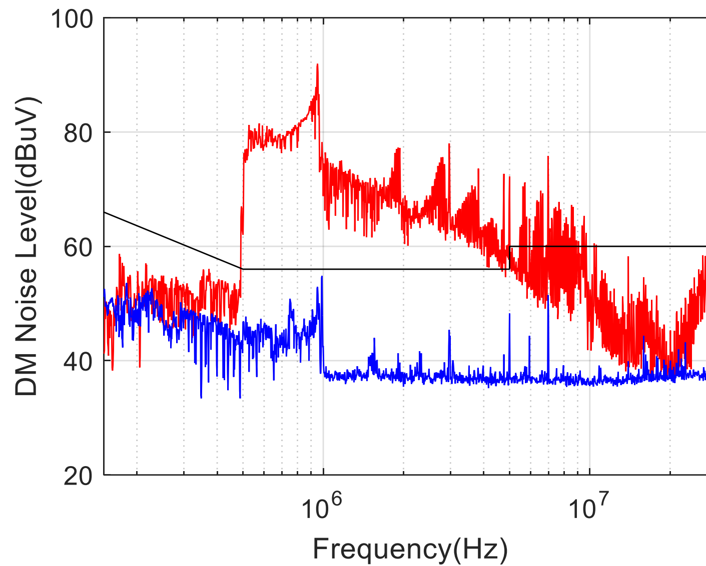
With the help of MHz switching frequency, soft-switching operation and shielding technique, one-stage filter can be applied to attenuate EMI noise. The filter structure is same as the one shown in Figure 4.34. A filter design based on 150W prototype is shown in Figure 4.64, and the parameters are listed in Table 4.3. Y-cap is connected between the primary ground and secondary ground, which is equivalent to the structure shown in Figure 4.34.

Figure 4.64 One-stage filter for proposed 150W 2-stage adapter

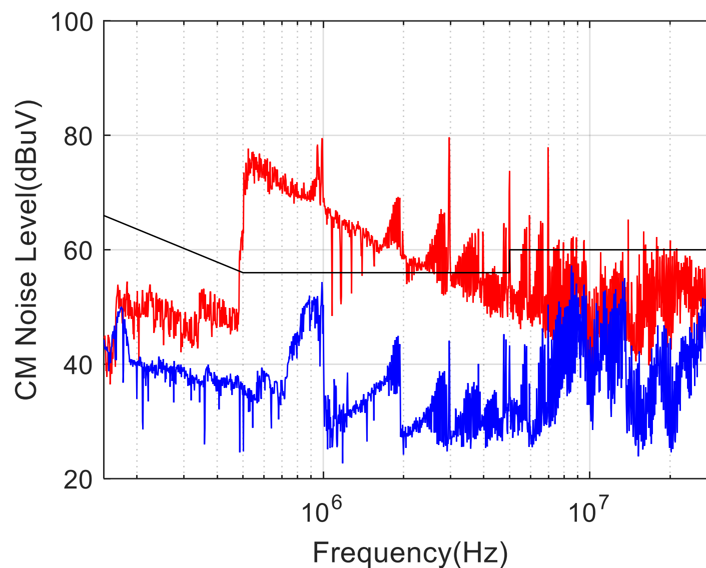
Table 4.3 Parameters of the EMI filter for 150W prototype

Parameters	L_{CM}	L_{DM}	$C_{Y1}=C_{Y2}$	C_X
Value	0.9mH	0.03mH	1nF	470nF

Figure 4.65 shows the CM/DM noise spectrum with peak mode measurement under $110V_{AC}$ input full load output condition which is the worst case for the prototype design. The red curves are the results without filters. The blue curves are the final results with EMI filter. It clearly shows that the blue curves are already lower than the quasi-peak standard.



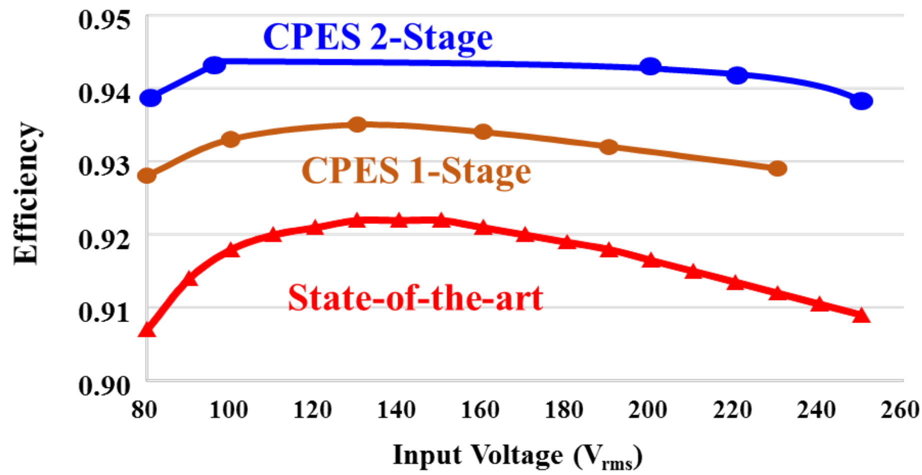
(a) DM noise (red line: w/o filter; blue line: w/ filter)



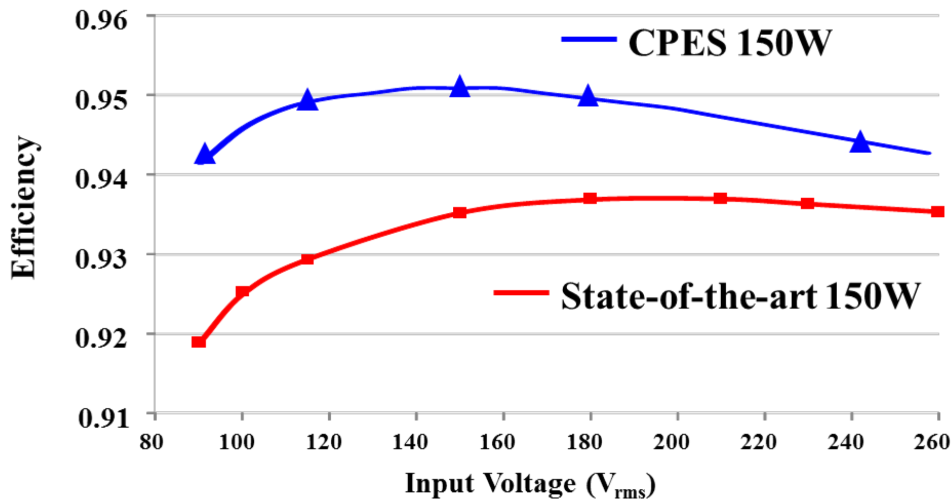
(b) CM noise (red line: w/o filter; blue line: w/ filter)

Figure 4.65 EMI measurement results of 150W prototype

The measured efficiency of the two prototypes over input line voltage are shown in Figure 4.66. It clearly shows that the proposed 2-stage solution have superior efficiency to the state-of-the-art of industry products. It is also significantly improved when compared to the active-clamp flyback approach for 65W adapter.



(a) 65W



(b) 150W

Figure 4.66 Measured efficiency of proposed 2-stage adapters

The power density is 28W/in^3 and 35W/in^3 for 65W and 150W prototype, respectively. The power density of 2-stage 65W prototype is slightly higher than active-clamp flyback approach due to bus cap reduction. If map the few design examples demonstrated in this work into the power density and efficiency figure, shown in Figure 4.67, the power density and efficiency are much higher than current practice and the they are much closer to the thermal limit.

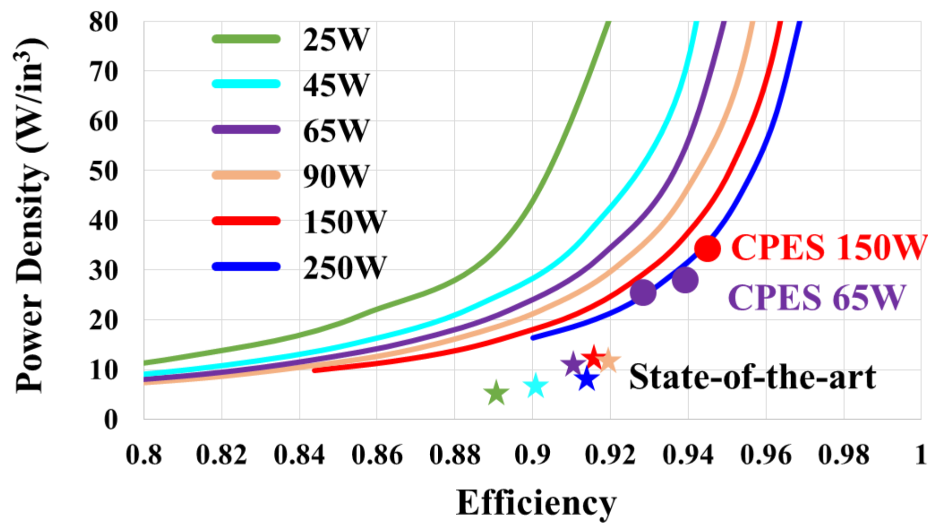


Figure 4.67 Achievement of higher density and higher efficiency adapter

4.4 Conclusion

This chapter presents the design consideration of high density and high efficiency AC-DC adapters. Two different approaches including active-clamp flyback and novel two-stage structure are illustrated in detail. Each design procedure targets at minimal power loss as well as smaller size. The PCB winding based transformer has the advantage of high density, controllable parasitics, and easy integration of shielding. High frequency control strategy is proposed to achieve soft-switching and minimize propagation delay. Harmonic

injection is employed to reduce bus capacitor in two-stage approach. Few design prototypes verify the feasibility of the system design. With high frequency operation and dedicated design, much higher density and higher efficiency are achieved compared with state of art product. More importantly, all the designs presented in this work aim at removing labor content completely or partially in the manufacturing process, which has significant impact on the industry.

Chapter 5. Conclusion and Future Work

5.1 Conclusion

The future power conversion system not only must meet the characteristics demanded by the load, but also have to achieve high power density with high efficiency, high ambient temperature, and high reliability. Density and efficiency are two key drivers and metrics for the advancement of power conversion technologies. Generally speaking, a high performance active device is the first force to push power density to meet the requirement of modern systems. Silicon has been a dominant material in power management since the late 1950s. However, due to continuous device optimizations and improvements in the production process, the material properties of silicon have increasingly become the limiting factor. Workarounds like the super junction stretch the limits but usually at substantial cost.

The use of gallium nitride devices is gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load (POL) converters, off-line switching power supplies, battery chargers and motor drives. GaN devices have a much lower gate charge and lower output capacitance than silicon MOSFETs and, therefore, are capable of operating at a switching frequency 10 times greater. This can significantly impact the power density of power converters, their form factor, and even current design and manufacturing practices. To realize the benefits of GaN devices resulting from significantly higher operating frequencies, a number of issues have to be addressed, such as converter topology, soft-switching technique, high frequency gate driver, high frequency magnetics, packaging, control, and thermal management.

This work studies the insight switching characteristics of high-voltage GaN devices including some specific issues related to the cascode GaN. Mathematical model and Pspice based simulation model for GaN devices are built, verified and serve as a tool to help analyze the switching behavior of different GaN devices under different condition. The models also help to understand the impact of package parasitic on the switching performance and device reliability. The interaction between the two devices in a cascode GaN may result in undesired features, such as Si reaching avalanche, GaN losing ZVS and divergent oscillation. A stack-die package with integrated capacitor is proposed for cascode GaN devices to minimize the impact of package parasitic inductance on switching transition and solve the issues mentioned above. Comparison of hard-switching and soft-switching operation is carried based on device model and experiments, which shows the necessity of soft-switching for GaN devices at high frequencies.

This work also addresses high dv/dt and di/dt related gate drive issues associated with the higher switching speed of GaN devices. Particularly, the conventional driving solution could fail on the high side switch in a half-bridge configuration due to relative large common-mode noise current. Two simple and effective driving methods are proposed to improve noise immunity and maintain high driving speed.

Finally, this work illustrates the utilization of GaN in an emerging application, high density AC-DC adapter. A novel 2-stage structure is proposed to achieve high efficiency and density over a wide power level. Many design considerations are presented in detail. The GaN-based adapter is capable of operating at 1-2 MHz frequencies with an improved efficiency up to 94%. Several design examples at different power levels , with a power density in the range of 20~35W/in^3, which is a three-fold improvement over the state-of-

the-art product, are successfully demonstrated. It is worthwhile to point out that the transformers in all design are implemented with PCB winding, which is aiming at highly automation with reduced labor content.

In conclusion, this work is focus on the characterization, and evaluation of GaN devices. packaging, high frequency driving and soft-switching technique are addressed to fully explore the potential of GaN devices. High density adapters are demonstrated to show the advance of GaN device and its big impact on system design.

5.2 Future Work

The emerging GaN devices shows promising future in AC-DC front-end converter. Following this research there are still some remaining research opportunity can be further explored that are related to this work.

1. Optimize the switching frequency that can achieve both high efficiency and density. 1MHz is a reasonable starting point for this research but not necessary be the optimal option. It could be systematically evaluated from converter loss, passive components size, EMI filter, thermal management, control feasibility aspect.
2. Integration of high frequency inductor and EMI filter can completely remove labor and enable fully automation, which could result in cost reduction and improvement of equipment reliability.
3. Wide load range and input range efficiency optimization can be achieved by different control strategy. It is possible to define a such power management IC via cooperation with industry.

Appendix A. GaN Analytical Loss Model

An accurate loss model that estimates switching loss is highly desirable for predicting maximum junction temperatures and overall power converter efficiency. One of the most popular analytical loss models is the piecewise linear model presented in [E.1], which is shown in Figure.A 1. This model enables simple and rapid estimation of switching loss, however, it doesn't take into consideration the parasitic inductances and nonlinearity of the junction capacitors of the device. Therefore, the result generally doesn't match the experimental results very well, especially for high frequency applications.

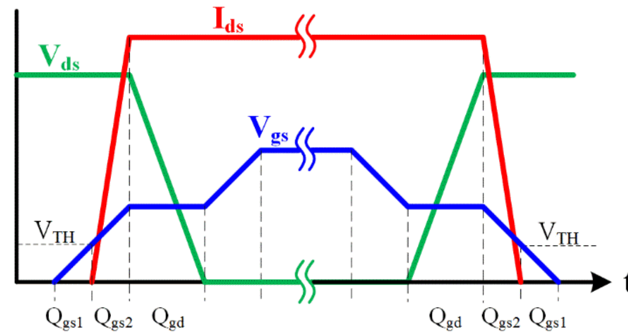


Figure.A 1 Piecewise linear approximation of the conventional loss model

More comprehensive analytical loss models for voltage source drive are presented in [E.2] and [E.3], and models for current source drive are presented in [E.4] and [E.5]. It should be noted that a current source drive could reduce the switching transition time and improve converter efficiency. However, driver circuit design and control are more complex, and haven't yet been widely used in industrial applications. These models consider the nonlinearity of the junction capacitor and parasitic inductance, particularly the common source inductor, which is defined as the inductor shared by the power loop and driver loop.

The switching processes are well defined, and the switching loss is obtained by solving the equivalent circuit for each switching transition. The experimental results prove that these models are more accurate than the piecewise model, especially during high frequency operation. However, the transconductance is assumed to be constant over the entire switching transition in these models, which introduces some inaccuracy of the waveforms and efficiencies.

Nevertheless, all of these analytical models are designed to estimate the power loss of MOSFETs that usually operate at a voltage lower than 40V. The research on analyzing the switching loss of high voltage devices is less comprehensive. The switching process is more complex than in low voltage devices, due to the impact of higher dv/dt and di/dt across the parasitics. The most popular way to estimate the switching loss of high voltage devices is based on measurement [E.6]-[E.10]. Some high voltage device manufacturers provide values for the turn on energy (E_{on}) and turn off energy (E_{off}) dissipation on the datasheet using double-pulse-test results [E.11]. The basic concept behind this kind of measurement is to capture the waveforms in the working prototype and calculate the switching loss. However, the current probes introduce a substantial delay in the waveforms, typically a few nanoseconds. This delay can be estimated and a proper correction introduced, but for fast switching circuits (capable of traversing from rail to rail in a few nanoseconds) the error will remain huge. On the other hand, the E_{on} / E_{off} obtained from a double-pulse-test only apply with certain test conditions, including particular PCB parasitic inductances, drivers with certain capabilities, certain characteristics of free-wheeling diodes, etc. Therefore, an analytical model is required to predict switch performance and understand how these parameters impact the switching loss.

High voltage GaN HEMTs can be categorized into normally-on (depletion mode) and normally-off (enhancement mode) device. The switching behavior of e-mode GaN device is similar to Si MOSFET despite of faster switching transition. One of the desirable features for enhancement mode high voltage GaN HEMTs is gate overdrive protection. When the switch is turned on, the Schottky gate of the GaN HEMT is usually switched beyond the forward turn on voltage to obtain the minimum on resistance. Due to the exponential current/voltage characteristic beyond the forward turn on voltage, small increases in the forward bias could result in excessive gate current, which may lead to device failure [E.12]. In depletion mode high voltage GaN HEMTs, the driving voltage can be extended to -30-2V and -5V is required to fully turn on, which provides a sufficient safety driving margin. To easily apply a depletion mode GaN HEMT in circuit design, a low voltage silicon MOSFET is used in series to drive the GaN HEMT, which is well known as cascode structure [E.13]. The on/off state of the low voltage silicon MOSFET controls the on/off status of the high voltage GaN HEMT. Besides the basic principle of cascode configuration, the interaction between these two devices determines the switching transition and implies the criteria of how to select a low voltage silicon MOSFET according to the high voltage GaN HEMT to avoid avalanche and optimize efficiency. Therefore, this configuration needs to be analyzed mathematically in order to more accurately predict and optimize the cascode GaN transistor.

This appendix aims to analyze the switching loss of high voltage cascode GaN transistors with mathematical approach. The proposed model considers the package and PCB parasitic inductances, as well as the nonlinearity of the junction capacitors and the transconductance of the cascode GaN transistor. The switching loss is obtained by solving

the equivalent circuits during switching transition. The model is easy to understand and provides a deep insight into the switching process.

I. Basis of The Model

The proposed analytical model includes the most relevant parameters in actual cascode GaN transistor: parasitic inductors and capacitors, and nonlinear transconductance. The package of a cascode GaN device is shown in Figure.A 2. In addition to the lead parasitic inductors, the interconnections between the GaN HEMT and silicon MOSFET also contribute to the total parasitic inductors. Current packaging technology can minimize these inductances as low as nH level. This progress makes the layout of the PCB even more critical, because this part can easily induce nH level parasitic inductance. Both the package and PCB parasitic inductances have a significant impact on the switching transition.

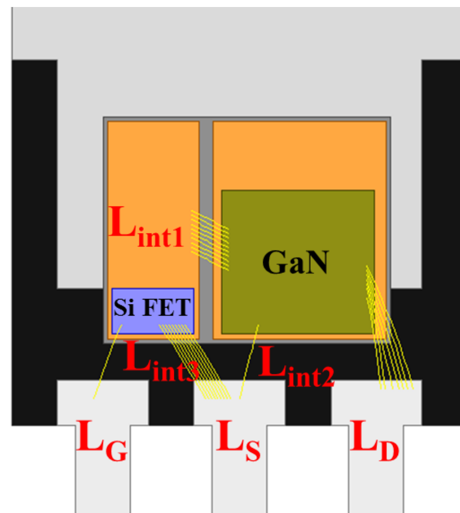


Figure.A 2 Package of a cascode GaN

The junction capacitors of the GaN HEMT and silicon MOSFET also impact the switching performance. There are three intrinsic capacitors in both devices: the gate-source capacitor, the gate-drain capacitor and the drain-source capacitor. As both the drain-source

capacitor and the gate-drain capacitor are associated with reverse a biased p-n junction, they change with the applied voltage. This nonlinearity of capacitance versus the voltage can be modeled as:

$$C(v) = C_0 \cdot f(v) \tag{A.1}$$

where C_0 is the 0V capacitance and f(v) can be extracted from the device datasheet using curve fitting. The gate-source capacitor remains nearly constant regardless of the applied voltage.

The third important parameter is transconductance g_m, representing the incremental change of channel current over incremental of change of the gate-source voltage, which determines the voltage and current transition period, along with the other two parameters mentioned above. Based on the physical definition, g_m is a nearly linear function of the gate-source voltage shown in (2), regardless of the channel length modulation effect when the drain-source voltage is larger than the gate-source voltage, which is practically true during the transition period.

$$g_m(v_{gs}) = k \cdot (v_{gs} - v_{TH}) \tag{A.2}$$

The value for k in (A.2) is derived from the device datasheet. This linear function can be applied for both low voltage silicon MOSFETs and high voltage GaN HEMTs in cascode configuration.

It should be noted that mathematically applying nonlinear capacitance and transconductance makes calculation very complicated. However, it is reasonable to derive an equivalent value during each transition, as long as the approximate voltage range is known, even though this would sacrifice a little accuracy.

Figure.A 3 shows the equivalent circuit for a high voltage GaN transistor in cascode configuration considering the parasitic inductors and capacitors. L_{int3} is combined with L_S for simplification. L_G, L_S, and L_D represent the package bonding and terminal lead parasitic inductors. L_{int1} and L_{int2} represent the interconnection bonding parasitic inductors. The interconnection resistor and the internal resistor of the GaN HEMT gate are not represented in the figure, but they are considered for the turn on/off transition analysis if necessary.

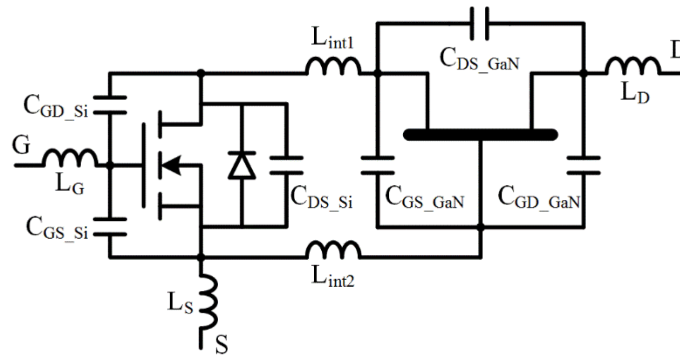


Figure.A 3 Equivalent cascode GaN transistor including parasitic inductors and capacitors

To analyze the switching loss, a simple buck converter is used as an example. A diode is used as the bottom switch, and the parameters of the diode represent whatever electric characteristics occur in the real case. The inductor current is treated as a current source during the transition time. The final circuit model used to analyze the cascode GaN transistor switching loss is shown in Figure.A 4. The PCB parasitic inductors are in series with the terminal lead inductors, and thus combined as a single element. The gate resistance R_G is made up of the gate driver output resistance and internal resistance of the low voltage silicon MOSFET due to gate contact. The simplified equivalent circuit in Figure.A 4 is also suitable for analyzing the device behaviors during the transition period for other bridge configuration based topologies, such as boost, buck-boost.

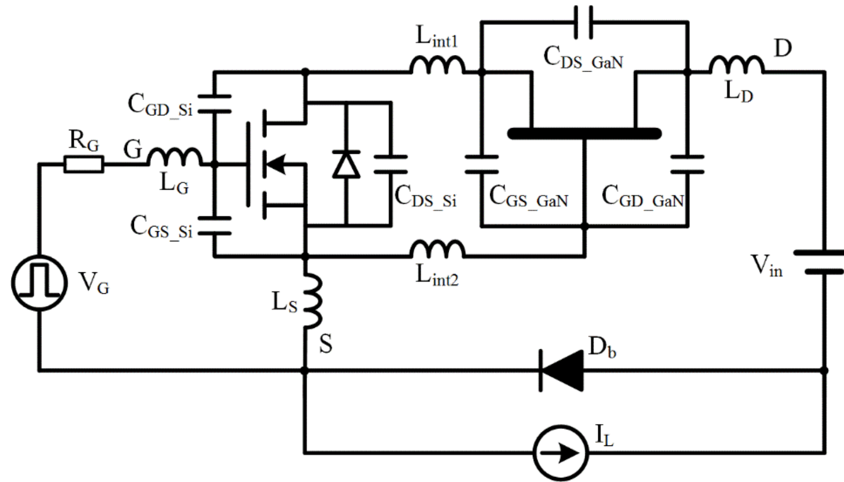


Figure.A 4 Simplified equivalent circuit to analyze switching loss of cascode GaN transistor

II. Turn on Transition

Before the cascode GaN transistor is turned on, the inductor current I_L flows through freewheeling diode D_b and the voltage V_{in} is applied to the cascode GaN transistor. The turn on transition can be divided into six stages which are analyzed in the following sections.

A. Stage I: Silicon MOSFET delay period

When the gate voltage V_G is applied, the resultant gate current charges the gate-source equivalent capacitance. In fact, C_{GS_Si} is much larger than any of the other capacitors in the cascode GaN transistor, thus the majority of the gate current charges C_{GS_Si}. As the GaN and silicon MOSFET are open circuit, almost no drain current flows into this circuit. The equivalent circuit is shown in Figure.A 5. During this period, the power stage does not change and current source I_L keeps flowing through D_b. From the circuit in Fig. 6, the following equations are obtained:

$$V_G = (L_G + L_S)\frac{di_g}{dt} + R_G \cdot i_g + v_{gs_Si} \tag{A.3}$$

$$i_g = C_{GS_Si}\frac{dv_{gs_Si}}{dt} \tag{A.4}$$

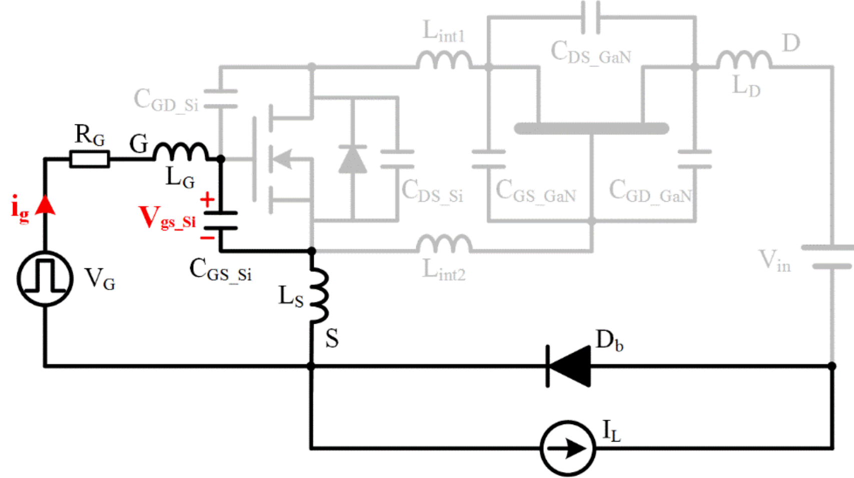


Figure.A 5 Equivalent circuit during turn on Stage I

The Laplace and inverse Laplace transforms are applied to solve the differential equations. The silicon MOSFET gate-source voltage $v_{gs_Si}(t)$ is shown below. This stage ends when v_{gs_Si} reaches the threshold voltage of silicon MOSFET V_{TH_Si}.

$$v_{gs_Si}(s) = \frac{1}{s} \cdot \frac{V_G}{s^2 \cdot (L_G + L_S) C_{GS_Si} + s \cdot R_G C_{GS_Si} + 1} \tag{A.5}$$

$$v_{gs_Si}(t) = V_G \cdot \left(1 - \frac{s_{11} e^{s_{12} t} - s_{12} e^{s_{11} t}}{s_{11} - s_{12}}\right) \tag{A.6}$$

where $s_{11} = \sqrt{\frac{1}{4}\left(\frac{R_G}{L_G + L_S}\right)^2 - \frac{1}{(L_G + L_S) C_{GS_Si}}} - \frac{R_G}{2(L_G + L_S)}$, $s_{12} = -\sqrt{\frac{1}{4}\left(\frac{R_G}{L_G + L_S}\right)^2 - \frac{1}{(L_G + L_S) C_{GS_Si}}} - \frac{R_G}{2(L_G + L_S)}$.

As the GaN and silicon MOSFET are not activated, the only power loss during this period are the losses in the gate drive circuit, which are included as a separate term in the final loss calculation.

B. Stage II: Silicon MOSFET drain-source voltage falling (GaN gate-source voltage rising)

When v_{gs_Si} reaches V_{TH_Si}, the MOSFET channel starts conducting and being controlled by v_{gs_Si}. Silicon MOSFET capacitors C_{DS_Si} and C_{GD_Si} are discharged by channel current i_{ch_Si}. In parallel to C_{DS_Si}, gate-source capacitor C_{GS_GaN} of the GaN HEMT is also discharged with a phase delay induced by the interconnection parasitic inductors. As the GaN HEMT is still not activated, there is no current flowing through cascode GaN transistor. The equivalent circuit is shown in Figure.A 6. The interconnection inductances only impact the phase delay of v_{gs_GaN} which can be compensated, but the inductances make the circuit order too high for mathematical solution. Therefore, an even more simplified circuit is shown in Figure.A 7. The internal inductances are removed, and an extra phase delay can be purposely added when calculating v_{gs_GaN}.

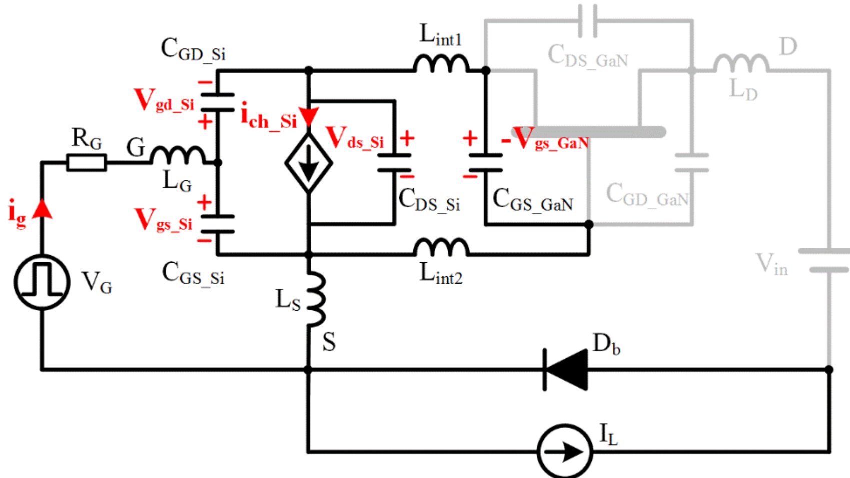


Figure.A 6 Equivalent circuit during turn on Stage II

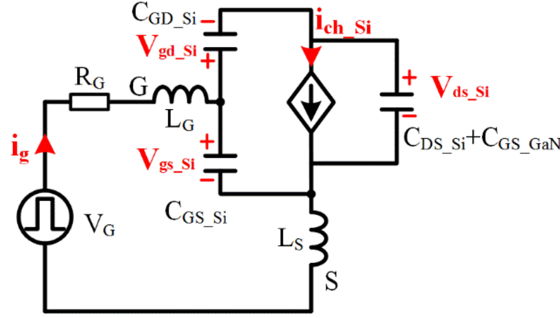


Figure.A 7 Further simplified equivalent circuit during turn on Stage II

From the Figure.A 7, the following key equations are obtained:

$$V_G = (L_G + L_S)\frac{di_g}{dt} + R_G \cdot i_g + v_{gs_Si} \tag{A.7}$$

$$i_g = C_{GS_Si}\frac{dv_{gs_Si}}{dt} + C_{GD_Si}\frac{d(v_{gs_Si} - v_{ds_Si})}{dt} \tag{A.8}$$

$$g_{m_Si}(v_{gs_Si} - V_{TH_Si}) = C_{GD_Si}\frac{d(v_{gs_Si} - v_{ds_Si})}{dt} - \left(C_{DS_Si} + C_{GS_GaN}\right)\frac{dv_{ds_Si}}{dt} \tag{A.9}$$

The expression of $v_{gs_Si}(t)$ is derived following the same procedure as that used for Stage I.

$$v_{gs_Si}(s) = \frac{1}{s} \cdot \frac{c_1 s^2 + d_1 s + e_1}{s^2 + a_1 s + b_1} \tag{A.9}$$

$$v_{gs_Si}(t) = \frac{c_1 s_{21}^2 + d_1 s_{21} + e_1}{(s_{21} - s_{22})s_{21}} e^{s_{21}t} + \frac{c_1 s_{22}^2 + d_1 s_{22} + e_1}{(s_{22} - s_{21})s_{22}} e^{s_{22}t} + \frac{e_1}{b_1} \tag{A.10}$$

where $s_{21} = \frac{-a_1 + \sqrt{a_1^2 - 4b_1}}{2}$, $s_{22} = \frac{-a_1 - \sqrt{a_1^2 - 4b_1}}{2}$, $a_1 = \frac{R_G C_{eq1} + R_G L_{eq1} K_I / C_{eq1}}{L_{eq1} C_{eq1}}$,

$b_1 = \frac{1 + R_G K_I}{L_{eq1} C_{eq1}}$, $c_1 = V_{TH_Si}$, $d_1 = \frac{(R_G C_{eq1} + L_{eq1} K_I) V_{TH_Si} + L_{eq1} i_{g_I}}{L_{eq1} C_{eq1}}$, $e_1 =$

$\frac{V_G+V_{TH_Si}R_GK_I}{L_{eq1}C_{eq1}}$, $L_{eq1}=L_G+L_S$, $C_{eq1}=C_{GS_Si}+\frac{C_{GD_Si}(C_{DS_Si}+C_{GS_GaN})}{C_{GD_Si}+(C_{DS_Si}+C_{GS_GaN})}$, $K_I=\frac{g_{m_Si}C_{GD_Si}}{C_{GD_Si}+(C_{DS_Si}+C_{GS_GaN})}$

Accordingly, $v_{ds_Si}(t)$ can be calculated along with other variables. $v_{gs_GaN}(t)$ can be obtained from $v_{ds_Si}(t)$ with a given phase delay, which is determined by LC values. This stage ends when v_{gs_GaN} reaches the threshold voltage of the GaN HEMT. During this stage, the silicon MOSFET channel conducts and consumes energy stored in C_{GD_Si} and $C_{DS_Si}+C_{GS_GaN}$. The power loss can be calculated as:

$$P_{sw_on_II}(t)=\int_{I}^{II}v_{ds_Si}(t)\cdot i_{ch_Si}(t)dt \tag{A.11}$$

It should be noted that inductor current I_L still flows through freewheeling diode D_b, and the terminal voltage of cascode GaN transistor is clamped at V_{in}. Therefore, the drain-source voltage of the GaN HEMT rises a little due to the decrease in v_{ds_Si}.

C. Stage III: GaN channel current rising

When v_{gs_GaN} reaches V_{TH_GaN}, the GaN HEMT channel starts conducting and GaN HEMT capacitors C_{DS_GaN} and C_{GD_GaN} are discharged by channel current i_{ch_GaN} which causes drain-source voltage v_{ds_GaN} to fall. As the bottom switch still conducts current, the voltage across the bottom switch is zero. Therefore, the voltage difference between V_{in} and v_{ds_GaN} is automatically applied on the power loop inductance and forces the cascode GaN transistor terminal current i_{Ld} to increase. As a result, the inductor current I_L begins to transfer from bottom switch D_b to the top switch. In practice, R_G is reasonably small, and v_{gs_Si} keeps increasing. Thus, v_{ds_Si} shortly decreases to zero, and the silicon MOSFET can be considered as operating in saturate region. The value of v_{gs_GaN} is now determined by

the Miller effect of the GaN HEMT, and interconnection inductor L_{int1} now becomes a common source inductor of the GaN HEMT and should be taken into consideration. Therefore, the silicon MOSFET and the GaN HEMT can be decoupled, as the silicon MOSFET has little influence on the rest of the switching process of the GaN HEMT. The equivalent circuit is shown in Figure.A 8, from which the following key equations are obtained.

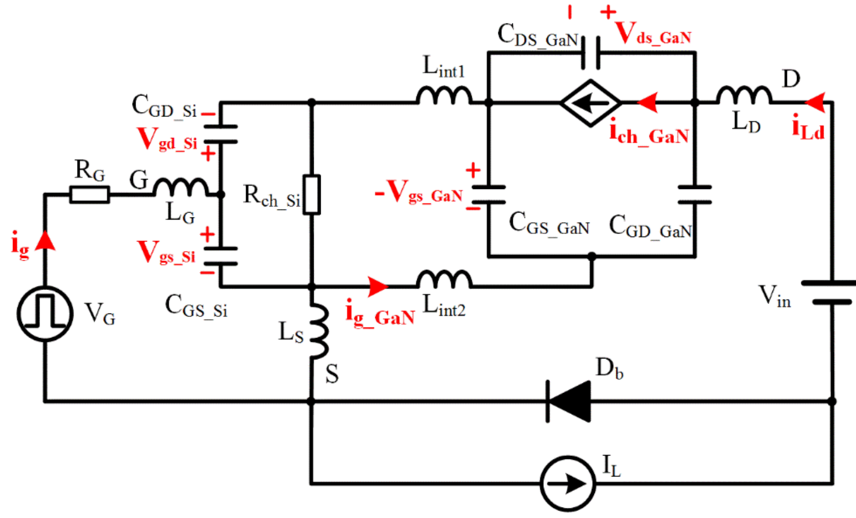


Figure.A 8 Equivalent circuit during turn on Stage III

$$v_{gs_GaN} + (L_{int1} + L_{int2})\frac{di_{g_GaN}}{dt} + L_{in1} \cdot \frac{di_{Ld}}{dt} + R_{ch_Si}\left(i_{g_GaN} + i_{Ld}\right) = 0$$

(A.12)

$$i_{g_GaN} = C_{GS_GaN}\frac{dv_{gs_GaN}}{dt} + C_{GD_GaN}\frac{d(v_{gs_GaN} - v_{ds_GaN})}{dt} \quad (A.13)$$

$$g_{m_GaN}(v_{gs_GaN} - V_{TH_GaN}) = C_{GD_GaN}\frac{d(v_{gs_GaN} - v_{ds_GaN})}{dt} - C_{DS_GaN}\frac{dv_{ds_GaN}}{dt} + i_{Ld}$$

(A.14)

$$(L_D + L_S + L_{int1})\frac{di_{Ld}}{dt} + L_{int1}\frac{di_{g_GaN}}{dt} + v_{ds_GaN} + R_{ch_Si}(i_{g_GaN} + i_{Ld}) = V_{in}$$

(A.15)

The expressions of $v_{gs_GaN}(s)$ and $v_{ds_GaN}(s)$ can be derived from (9)-(12), as shown below.

$$v_{gs_GaN}(s) = \frac{y_1(s)z_2(s) - y_2(s)z_1(s)}{x_1(s)y_2(s) - x_2(s)y_1(s)} \quad \text{(A.16)}$$

$$v_{ds_GaN}(s) = \frac{x_2(s)z_1(s) - x_1(s)z_2(s)}{x_1(s)y_2(s) - x_2(s)y_1(s)} \quad \text{(A.17)}$$

where $x_1(s) = s^2[(L_{int1} + L_{int2})C_{GS_GaN} + L_{int2}C_{GD_GaN}] + s(g_{m_GaN}L_{int1} + R_{ch_Si}C_{GS_GaN}) + g_{m_GaN}R_{ch_Si} + 1$, $y_1(s) = s^2(L_{int1}C_{DS_GaN} - L_{int2}C_{GD_GaN}) + sR_{ch_Si}C_{GD_GaN}$,

$z_1(s) = s[A_1(s)(L_{int1} + L_{int2}) - B_1(s)L_{int1}] + [A_1(s) - B_1(s)]R_{ch_Si} - (L_{int1} + L_{int2})I_{g_GaN_II}$, $x_2(s) = s^2[L_{int1}C_{GS_GaN} - (L_D + L_S)C_{GD_GaN}] + s[g_{m_GaN}(L_{int1} + L_D + L_S) + R_{ch_Si}C_{GS_GaN})] + g_{m_GaN}R_{ch_Si}$,

$y_2(s) = s^2[(L_{int1} + L_D + L_S)(C_{DS_GaN} + C_{GD_GaN}) - L_{int1}C_{GD_GaN})] + sR_{ch_Si}C_{DS_GaN} + 1$,

$z_2(s) = s[A_1(s)L_{int1} - B_1(s)(L_{int1} + L_D + L_S)] + [A_1(s) - B_1(s)]R_{ch_Si} - L_{int1}I_{g_GaN_II} - V_{in}/s$, $A_1(s) = C_{GD_GaN}(V_{in} + V_{TH_GaN}) - (C_{GS_GaN} + C_{GD_GaN})V_{TH_GaN}$,

$B_1(s) = (C_{GD_GaN} + C_{DS_GaN})(V_{in} + V_{TH_GaN}) - C_{GD_GaN}V_{TH_GaN} + g_{m_GaN}V_{TH_GaN}/s$

As there are four independent state variables in equation (A.16)-(A.17), the frequency domain expressions are fourth order. Math tools are employed to derive the time domain

solutions. Accordingly, cascode GaN transistor terminal current i_{Ld} can be calculated. This stage ends when i_{Ld} reaches inductor current I_L. In normal cases, i_{Ld} increases to I_L very quickly due to small loop inductances and v_{ds_GaN} drops a little. During this stage, the main switching loss comes from the GaN HEMT and can be calculated as:

$$P_{sw_on_III}(t) = \int_{II}^{III} v_{ds_GaN}(t) \cdot i_{ch_GaN}(t)dt \tag{A.18}$$

D. Stage IV: Bottom switch reverse recovery

When i_{Ld} reaches I_L, the reverse recovery period begins. The bottom switch cannot block the reverse voltage until a certain amount of charge has been removed from its junction. The equivalent circuit and key equations of this stage are same as in Stage III, but with different initial conditions. v_{ds_GaN} continue to decrease, and the voltage difference between V_{in} and v_{ds_GaN} becomes even larger. Therefore, the top switch current i_{Ld} increases rapidly and this large di/dt across the parasitic inductor L_{int1} slows the increase of v_{gs_GaN} and consequently saturates the GaN HEMT channel before the bottom switch reverse recovery is complete. Therefore, v_{ds_GaN} increases rather than decreases near the end of this stage. In fact, this phenomenon can also be observed with standalone switch under high voltage double-pulse-test conditions [E.6] and [E.7]. This stage ends when the bottom switch reverse recovery is complete.

It should be mentioned that bipolar Si high voltage active switches or diodes have reverse recovery charge (Q_{rr}), but unipolar wide band gap semiconductors such as SiC or GaN device does not have. If the bottom switch doesn't have Q_{rr}, the analysis directly jumps into Stage V: the GaN drain-source voltage falls to zero. Otherwise, the power loss during this stage can be calculated as:

$$P_{sw_on_IV}(t) = \int_{III}^{IV} v_{ds_GaN}(t) \cdot i_{ch_GaN}(t)dt \tag{A.19}$$

E. Stage V: GaN drain-source voltage falling

When reverse recovery is complete, the bottom switch is able to block voltage. During this stage, part of the top switch current provides the inductor current I_L and additional current charges the junction capacitors of the bottom switch. As the voltage across bottom switch V_{Db} rises, the top switch GaN HEMT drain-source voltage eventually decreases. The equivalent circuit is shown in Figure.A 9, and key equations different from stage III and stage IV are shown below.

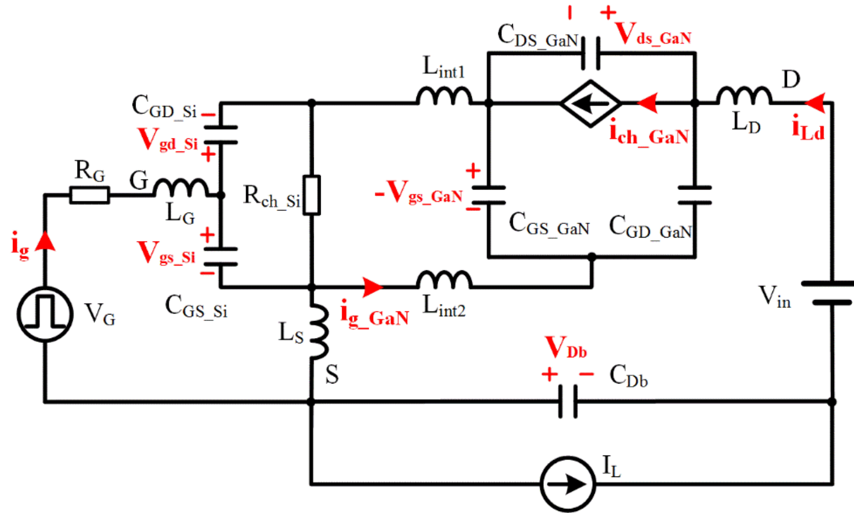


Figure.A 9 Equivalent circuit during turn on Stage V

$$(L_D + L_S + L_{int1})\frac{di_{Ld}}{dt} + L_{int1}\frac{di_{g_GaN}}{dt} + v_{ds_GaN} + R_{ch_Si}(i_{g_GaN} + i_{Ld}) + V_{Db} = V_{in} \tag{A. 20}$$

$$i_{Ld} = I_L + C_{Db}\frac{dv_{Db}}{dt} \tag{A.21}$$

The expression of $v_{ds_GaN}(s)$ is shown below. All other variables can be calculated accordingly.

$$v_{ds_GaN}(s) = \frac{x_2'(s)z_1'(s) - x_1'(s)z_2'(s)}{x_1'(s)y_2'(s) - x_2'(s)y_1'(s)} \tag{A.22}$$

where $x_1'(s) = x_1(s)$, $y_1'(s) = y_1(s)$, $z_1'(s) = s[A_1'(s)(L_{int1} + L_{int2}) - B_1'(s)L_{int1}] + [A_1'(s) - B_1'(s)]R_{ch_Si} - (L_{int1} + L_{int2})I_{g_GaN_IV} - L_{int1}i_{Ld_IV}$,

$x_2'(s) = s^2[L_{int1}C_{GS_GaN} - (L_D + L_S)C_{GD_GaN}] + s[g_{m_GaN}(L_{int1} + L_D + L_S) + R_{ch_Si}C_{GS_GaN})] + g_{m_GaN}/sC_{Db} - C_{GD_GaN}/C_{Db}$,

$y_2'(s) = s^2[(L_{int1} + L_D + L_S)(C_{DS_GaN} + C_{GD_GaN}) - L_{int1}C_{GD_GaN})] + sR_{ch_Si}C_{DS_GaN} + (C_{GD_GaN} + C_{DS_GaN})/C_{Db} + 1$,

$z_2'(s) = s[A_1'(s)L_{int1} - B_1'(s)(L_{int1} + L_D + L_S)] + [A_1'(s) - B_1'(s)]R_{ch_Si} + I_L/s^2C_{Db} - L_{int1}I_{g_GaN_IV} - V_{in}/s - (L_{int1} + L_D + L_S)i_{Ld_IV} - B_1'(s)/sC_{Db}$,,

$A_1'(s) = C_{GD_GaN}v_{ds_GaN_IV} - (C_{GS_GaN} + C_{GD_GaN})v_{gs_GaN_IV}$,

$B_1'(s) = (C_{GD_GaN} + C_{DS_GaN})v_{ds_GaN_IV} - C_{GD_GaN}v_{gs_GaN_IV} + g_{m_GaN}V_{TH_GaN}/s$

This stage ends when v_{ds_GaN} decreases to zero, and the overshoot current of the top switch goes back to inductor current I_L with a small ringing, which is lossless. At this point, the voltage and current transition is over, and the switching loss in this stage can be calculated as:

$$P_{sw_on_V}(t) = \int_{IV}^{V} v_{ds_GaN}(t) \cdot i_{ch_GaN}(t)dt \tag{A.23}$$

F. Stage VI: Remaining gate charging

After v_{ds_GaN} decreases to zero, v_{gs_GaN} continues increasing until it reaches 0. Meantime, v_{gs_Si} exponentially increases until it reaches V_G. The equivalent circuit is shown in Figure.A 10.

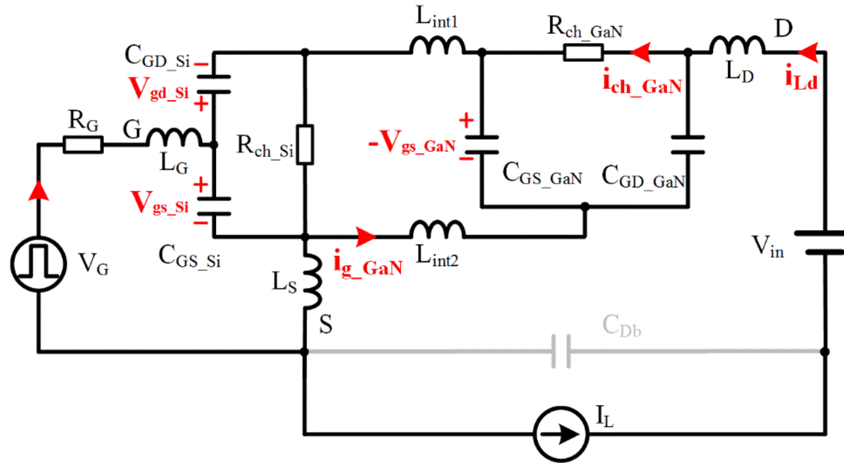


Figure.A 10 Equivalent circuit during turn on Stage VI

During this stage, the on-resistance is influenced by the gate-source voltage of GaN HEMT. After the cascode GaN transistor is fully turned on, the calculation of the conduction loss is a function of the steady state current and the on-resistance of cascode transistor, which should take the temperature coefficient into consideration.

III. Turn off Transition

Before the cascode GaN transistor is turned off, the inductor current I_L flows through the top switch and V_{in} is applied to the freewheeling diode. The turn off transition can be divided into five stages which are analyzed in the following sections.

A. Stage I: Silicon MOSFET delay period

When the gate drive circuit output is a low voltage, typically 0V, the gate-source equivalent capacitor of the silicon MOSFET is discharged. The equivalent circuit is shown in Figure.A 11, and key equations follow.

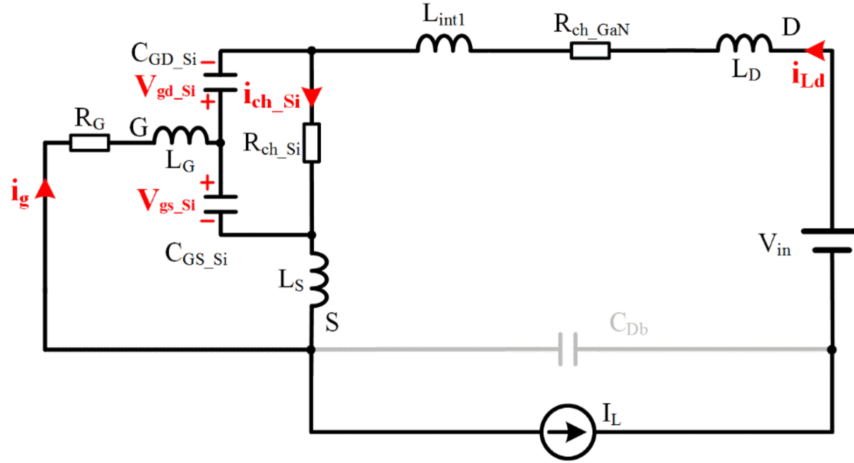


Figure.A 11 Equivalent circuit during turn off Stage I

$$0 = (L_G + L_S)\frac{di_g}{dt} + R_G \cdot i_g + v_{gs_Si} \tag{A.24}$$

$$i_g = (C_{GS_Si} + C_{GS_Si})\frac{dv_{gs_Si}}{dt} \tag{A.25}$$

The silicon MOSFET gate-source voltage $v_{gs_Si}(t)$ is derived through Laplace and inverse Laplace transforms, as shown below.

$$v_{gs_Si}(s) = \frac{v_{gs_Si_0}}{s^2 \cdot (L_G + L_S)(C_{GS_Si} + C_{GD_Si}) + s \cdot R_G(C_{GS_Si} + C_{GD_Si}) + 1} \tag{A.26}$$

$$v_{gs_Si}(t) = \frac{[s_{11} + R_G/(L_G + L_S)]v_{gs_Si_0}}{s_{11} - s_{12}} e^{s_{11}t} - \frac{[s_{12} + R_G/(L_G + L_S)]v_{gs_Si_0}}{s_{12} - s_{11}} e^{s_{12}t} \tag{A.27}$$

Where $s_{11} = \sqrt{\frac{1}{4}(\frac{R_G}{L_G + L_S})^2 - \frac{1}{(L_G + L_S)(C_{GS_Si} + C_{GD_Si})}} - \frac{R_G}{2(L_G + L_S)}$,

$$s_{12} = -\sqrt{\frac{1}{4}\left(\frac{R_G}{L_G+L_S}\right)^2 - \frac{1}{(L_G+L_S)(C_{GS_Si}+C_{GD_Si})}} - \frac{R_G}{2(L_G+L_S)},$$

The stage ends when the silicon MOSFET enters the saturation region, where the following equation is satisfied:

$$g_{m_Si}(v_{gs_Si} - v_{TH_Si}) = I_L \quad \text{(A.28)}$$

The drain-source voltage of the silicon MOSFET increases a little bit due to increased channel on-resistance but the GaN HEMT is still fully turned on, thus the switching loss during this stage is neglected. The losses in the gate drive circuit are included as a separate term in the final loss calculation which is the same as the turn on transition.

B. Stage II: Silicon MOSFET drain-source voltage rising (GaN gate-source voltage falling)

As v_{gs_Si} continues to decrease, the silicon MOSFET channel saturation current is less than the inductor current I_L. The excess current charges the silicon MOSFET drain-source equivalent capacitors, and drain-source voltage v_{ds_Si} increases. As the C_{GS_GaN} is parallel with C_{DS_Si} with interconnection inductors, the GaN HEMT gate-source voltage v_{gs_GaN} follows v_{ds_Si} with phase delay as the turn on transition. The equivalent circuit is shown in Figure.A 12, and key equations follow.

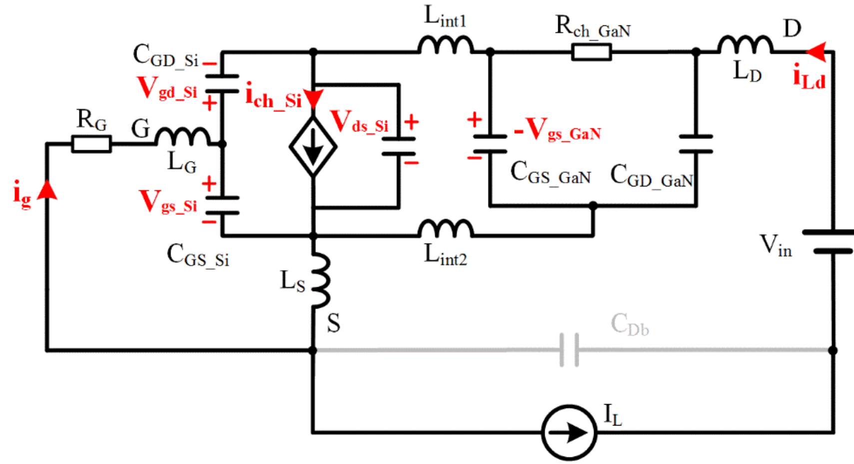


Figure.A 12 Equivalent circuit during turn off Stage II

$$0 = (L_G + L_S)\frac{di_g}{dt} + R_G \cdot i_g + v_{gs_Si} \tag{A.29}$$

$$i_g = C_{GS_Si}\frac{dv_{gs_Si}}{dt} + C_{GD_Si}\frac{d(v_{gs_Si} - v_{ds_Si})}{dt} \tag{A.30}$$

$$g_{m_Si}(v_{gs_Si} - V_{TH_Si}) = C_{GD_Si}\frac{d(v_{gs_Si} - v_{ds_Si})}{dt} - (C_{DS_Si} + C_{GS_GaN})\frac{dv_{ds_Si}}{dt} + I_L \tag{A.31}$$

The expression of $v_{ds_Si}(t)$ is shown below. Accordingly, $v_{gs_GaN}(t)$ can be calculated along with other variables in the equivalent circuit.

$$v_{gs_Si}(s) = \frac{1}{s} \cdot \frac{c_2 s^2 + d_2 s + e_2}{s^2 + a_2 s + b_2} \tag{A.32}$$

$$v_{gs_Si}(t) = \frac{c_2 s_{21}^2 + d_2 s_{21} + e_2}{(s_{21} - s_{22})s_{21}} e^{s_{21}t} + \frac{c_2 s_{22}^2 + d_2 s_{22} + e_2}{(s_{22} - s_{21})s_{22}} e^{s_{22}t} + \frac{e_2}{b_2} \tag{A.33}$$

where $s_{21} = \frac{-a_2+\sqrt{a_2^2-4b_2}}{2}$, $s_{22} = \frac{-a_2-\sqrt{a_2^2-4b_2}}{2}$, $a_2 = \frac{R_G C_{eq2}+L_{eq2}K_{II}}{L_{eq2}C_{eq2}}$, $b_2 = \frac{1+R_G K_{II}}{L_{eq2}C_{eq2}}$, $c_2 = v_{gs_Si_I}$ $d_2 = \frac{(R_G C_{eq2}+L_{eq2}K_{II})V_{TH_Si}+L_{eq2}i_{g_I}+L_{eq2}I_L K_{II}/g_{m_Si}}{L_{eq2}C_{eq2}}$, $e_2 = \frac{R_G K_{II}V_{TH_Si}+R_G K_{II}I_L/g_{m_Si}}{L_{eq2}C_{eq2}}$, $L_{eq2} = L_G + L_S$, $C_{eq2} = C_{GS_Si} + \frac{C_{GD_Si}(C_{DS_Si}+C_{GS_GaN})}{C_{GD_Si}+(C_{DS_Si}+C_{GS_GaN})}$, $K_{II} = \frac{g_{m_Si}C_{GD_Si}}{C_{GD_Si}+(C_{DS_Si}+C_{GS_GaN})}$

This stage ends when v_{gs_GaN} reaches the value at which the GaN HEMT enters the saturation region and the following equation is satisfied:

$$g_{m_GaN}(v_{gs_GaN} - v_{TH_GaN}) = I_L \tag{A.34}$$

During this stage, the switching loss of the silicon MOSFET can be calculated as:

$$P_{sw_off_II}(t) = \int_I^{II} v_{ds_Si}(t) \cdot i_{ch_Si}(t)dt \tag{A.35}$$

As v_{gs_GaN} decreases, v_{ds_GaN} increases a little bit due to increased channel on-resistance, but the switching loss of the GaN HEMT during this stage is negligible.

C. Stage III: GaN channel current decreasing

As the gate-source voltage of the GaN HEMT continues to decrease, the channel saturation current is less than inductor current I_L. The excess current charges the drain-source equivalent capacitors and v_{ds_GaN} increases. Meanwhile, the voltage across the freewheeling diode decreases and the displacement current of the junction capacitor also makes up the inductor current I_L. In normal cases, the silicon MOSFET gate-source voltage v_{gs_Si} decreases below the threshold voltage after Stage II. Thus, the silicon MOSFET can be considered as a nonlinear capacitor in parallel with C_{GS_GaN} and the gate drive circuit operates independently: v_{gs_Si} continues to decrease until it reaches zero. The terminal current i_{Ld} keeps charging the capacitors C_{DS_Si}, C_{GD_Si} and discharging C_{GS_GaN}, Thus,

v_{ds_Si} increases rapidly, and accordingly v_{gs_GaN} decreases very quickly. The intrinsic current source driving mechanism shortens the GaN HEMT channel current falling time, which is unique to the cascode configuration. The equivalent circuit during turn off Stage III is shown in Figure.A 13, and key equations follow.

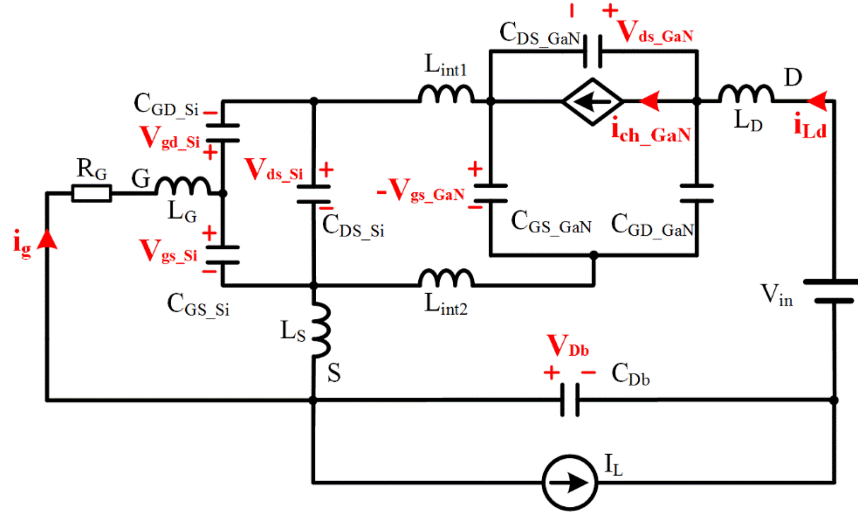


Figure.A 13 Equivalent circuit during turn off Stage III

$$i_{Ld} = I_L + C_{Db}\frac{dv_{Db}}{dt} \tag{A.36}$$

$$(L_D + L_S)\frac{di_{Ld}}{dt} + v_{ds_GaN} - v_{gs_GaN} + v_{Db} = V_{in} \tag{A.37}$$

$$(C_{GS_GaN} + C_{DS_Si} + C_{GD_Si})\ \frac{dv_{gs_GaN}}{dt} + C_{GD_GaN}\frac{d(v_{gs_GaN} - v_{ds_GaN})}{dt} = -i_{Ld} \tag{A.38}$$

$$g_{m_GaN}(v_{gs_GaN} - V_{TH_GaN}) = C_{GD_GaN}\frac{d(v_{gs_GaN} - v_{ds_GaN})}{dt} - C_{DS_GaN}\ \frac{dv_{ds_GaN}}{dt} + i_{Ld} \tag{A.39}$$

The expression of $v_{gs_GaN}(s)$ is shown below and all other variables can be calculated accordingly.

$$v_{gs_GaN}(s) = \frac{y_1(s)z_2(s)-y_2(s)z_1(s)}{x_1(s)y_2(s)-x_2(s)y_1(s)} \tag{A.40}$$

where $x_1(s) = s[s^2(L_D + L_S)C_{Db} + 1](C_{GS_GaN} + C_{GD_Si} + C_{DS_Si}) + sC_{Db}$,

$y_1(s) = -s[s^2(L_D + L_S)C_{Db} + 1]C_{GD_GaN} - sC_{Db}$,

$z_1(s) = -A_2(s)[s^2(L_D + L_S)C_{Db} + 1] + sC_{Db}B_2(s)$,

$x_2(s) = g_{m_GaN} + sC_{GD_GaN}$, $y_2(s) = sC_{DS_GaN}$, $z_2(s) = -A_2(s) - C_2(s)$,

$A_2(s) = (C_{GS_GaN} + C_{GD_GaN} + C_{DS_Si} + C_{GD_Si})v_{gs_GaN_II} + C_{Db}v_{Db_II} -$

$C_{GD_GaN}v_{ds_GaN_II} - I_L/s$, $B_2(s) = s(L_D + L_S)C_{Db}v_{Db_II} + (L_D + L_S)(i_{Ld_II} - I_L) +$

V_{in}/s,

$$C_2(s) = C_{GD_GaN}(v_{ds_GaN_II} - v_{gs_GaN_II}) + C_{DS_GaN}v_{ds_GaN_II} - C_{Db}v_{Db_II} + (I_L + g_{m_GaN})/s$$

Stage III ends when the GaN HEMT channel is totally shun down. In practice, the GaN HEMT channel current decreases from inductor current I_L to zero very quickly, due to the intrinsic current source turns off this device. The drain-source voltage of the GaN HEMT rises a little during the short transition. Thus, this mechanism makes the turn off switching loss quite minimal, and it can be calculated as:

$$P_{sw_off_III}(t) = \int_{II}^{III} v_{ds_GaN}(t) \cdot i_{ch_GaN}(t)dt \tag{A.41}$$

D. Stage IV: GaN drain-source voltage rising

After the gate-source voltage of the GaN HEMT drops below the threshold value, the channel is totally shut down. The remaining top switch current keeps charging the junction capacitors of the cascode GaN transistor. Meanwhile, the voltage across the freewheeling

diode decreases, and the inductor current transfers from the top switch to the bottom switch. The equivalent circuit during turn off Stage IV is shown in Figure.A 14. In fact, the voltage across the interconnection inductance has no significant impact during this stage, but it makes the circuit order too high for a mathematical solution. Therefore, an even more simplified circuit is shown in Figure.A 15 with internal parasitic inductors removed. The key equations different from stage III are shown below.

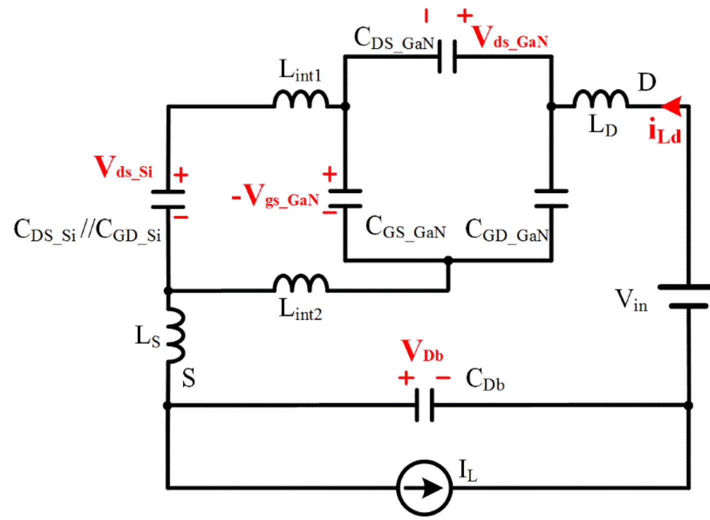


Figure.A 14 Equivalent circuit during turn off Stage IV

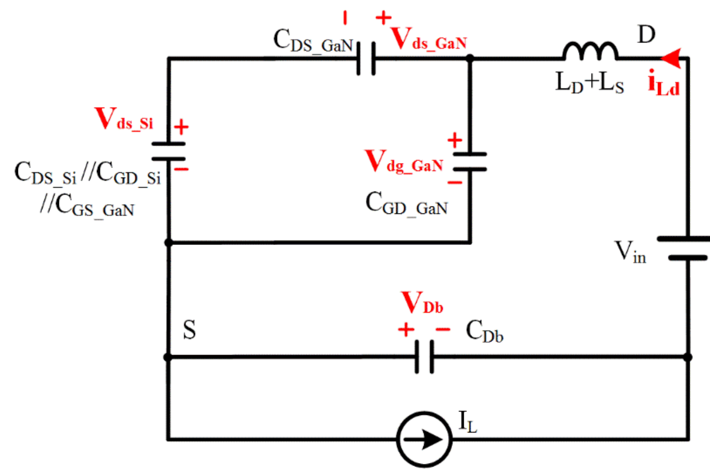


Figure.A 15 Further simplified equivalent circuit during turn off Stage IV

$$i_{Ld} = C_{GD_GaN}\frac{d(v_{ds_GaN}+v_{ds_Si})}{dt} + C_{DS_GaN}\frac{dv_{ds_GaN}}{dt} \tag{A.42}$$

$$(C_{DS_Si} + C_{GD_Si} + C_{GS_GaN})\frac{dv_{ds_Si}}{dt} = C_{DS_GaN}\frac{dv_{ds_GaN}}{dt} \tag{A.43}$$

The expression of $v_{ds_GaN}(s)$ is shown below and all other variables can be calculated accordingly.

$$v_{ds_GaN}(s) = \frac{x_2'(s)z_1'(s)-x_1'(s)z_2'(s)}{x_1'(s)y_2'(s)-x_2'(s)y_1'(s)} \tag{A.44}$$

where $x_1'(s) = s[s^2(L_D + L_S)C_{Db} + sR_GC_{Db} + 1]C_{GD_GaN} + sC_{Db}$,

$y_1'(s) = s[s^2(L_D + L_S)C_{Db} + sR_GC_{Db} + 1](C_{GD_GaN} + C_{DS_GaN}) + sC_{Db}$,

$z_1'(s) = -[s^2(L_D + L_S)C_{Db} + 1][C_{DS_GaN}v_{ds_GaN_III} + C_{GD_GaN}(v_{ds_GaN_III} +$

$v_{ds_Si_III})] - s(L_D + L_S)C_{Db}i_{Ld_III} - I_L/s - C_{Db}(V_{in} - v_{Db_III})$,

$x_2'(s) = s(C_{GS_GaN} + C_{GD_Si} + C_{DS_Si})$, $y_2'(s) = -sC_{DS_GaN}$,

$z_2'(s) = C_{DS_GaN}v_{ds_GaN_III} - (C_{GS_GaN} + C_{GD_Si} + C_{DS_Si})v_{ds_Si_III}$

The stage ends when voltage across the bottom switch decreases to zero and the freewheeling diode is forward biased. In normal cases, top switch current i_{Ld} decreases to nearly zero during this stage. Thus, the remaining energy of the parasitic inductors is very small and the overshoot of voltage across the cascode GaN transistor is very small. This is also true for high voltage silicon MOSFETs, as long as the parasitic inductance is reasonably small. The switching loss during this stage can be calculated by the energy dissipated in the loop resistance, and in practice is very small.

$$P_{sw_off_IV}(t) = \int_{III}^{IV} R_{loop}\cdot i_{ch_GaN}^2(t)dt \tag{A.45}$$

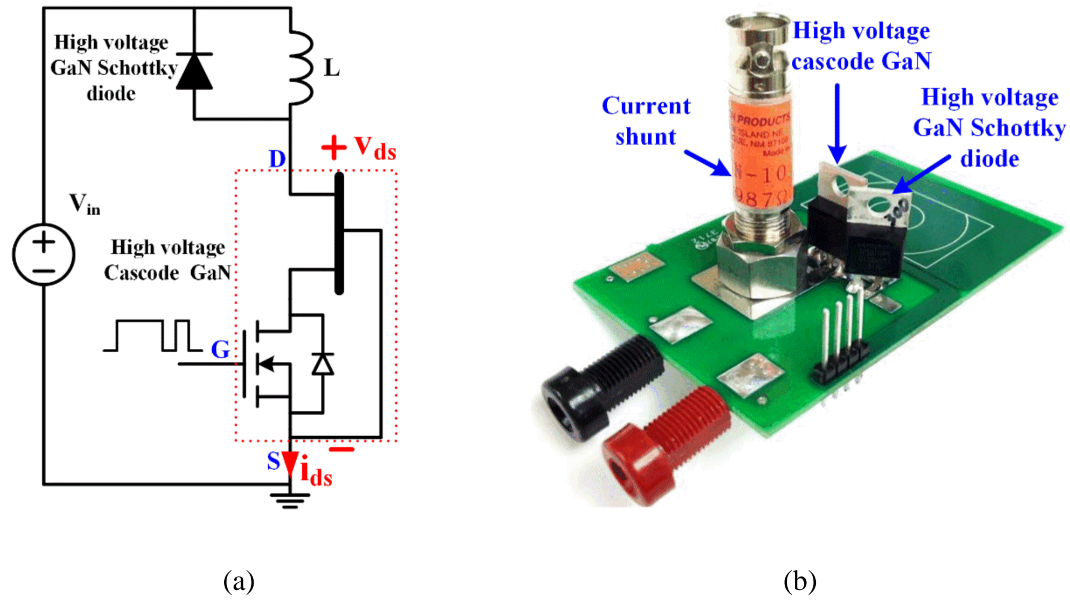
After the cascode GaN transistor is fully turned off, inductor current I_L flows through the freewheeling diode. The conduction loss is a function of the steady state current and the forward voltage, which should take the temperature coefficient into consideration.

V. Experimental Results Verifications and Discussions

In order to verify this analytical model, two sets of experiments are carried out: a double-pulse-test (DPT) to compare the waveforms, and a buck converter to validate the switching loss.

A. Double-pulse-test waveforms verification

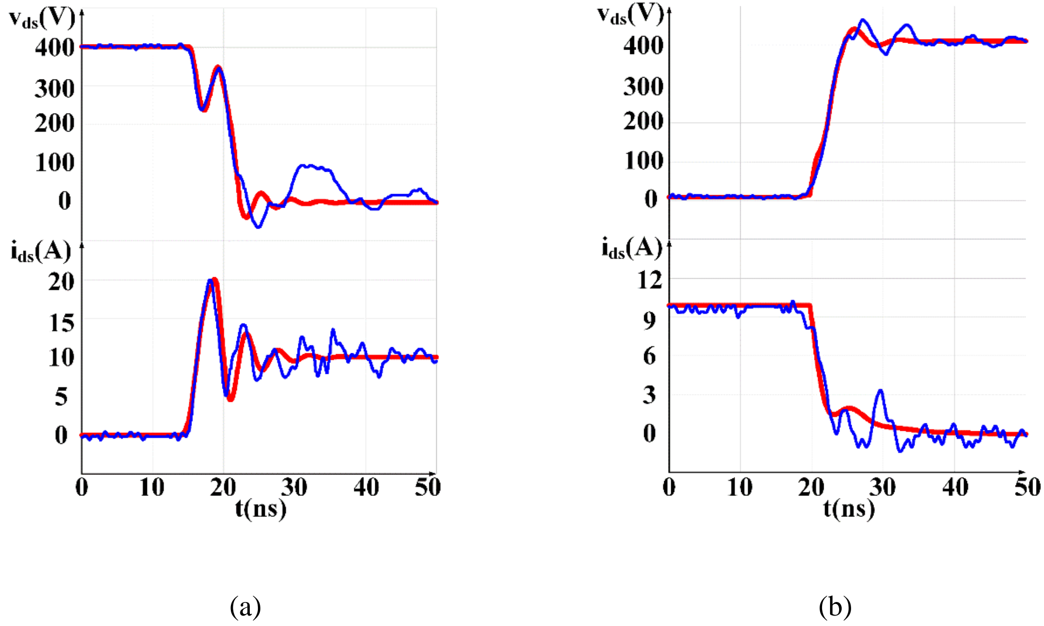
Figure.A 16 shows the DPT circuit diagram and prototype, respectively. The main switch is a high voltage cascode GaN transistor, and terminal voltage v_{ds} and current i_{ds} are recorded to compare with the calculation results. The freewheeling diode is a high voltage GaN diode with no reverse recovery charge. Both of these GaN devices are from Transphorm. The current waveform is measured by a coaxial shunt resister with high bandwidth and minimized parasitic inductance.



(a) (b)

Figure.A 16 Model validation with double-pulse-test circuit: (a) diagram, (b) prototype

Figure.A 17 shows waveform comparisons between the double-pulse-test and the calculated results of the proposed analytical model during the transition period. The figure clearly shows that the analytical model can match with the experiments on the voltage and current slope, as well as the magnitude and main transition time. The oscillation frequency and damping effect have some differences due to inaccurate high frequency parasitic inductance and AC resistance. As the value of the parasitic inductance and AC resistance is influenced by several factors, including conductor position, current direction and oscillation frequency, which are difficult to be predicted.



(a) (b)

Figure.A 17 Turn on/off waveforms comparisons (Blue line: experiment, red line: analytical model) (a) Turn on @10A, (b) Turn off@10A

Based on the experiment and analytical model waveforms, the energy dissipation is calculated by integrating drain to source voltage and drain to source current. The turn on energy is calculated as about 23uJ at 10A condition, and accordingly 4uJ for the turn off transition. It is important to note that during the turn on process, the energy stored in C_{DS}+C_{GD} is dissipated by the channel which cannot be observed from the terminal waveforms. Therefore, the turn on loss derived from waveform is underestimated, since it should include the energy stored in C_{DS}+C_{GD}. On the other hand, during the turn off process, some of the terminal current charges C_{DS}+C_{GD} and the energy is stored in the junction capacitors. Thus, the turn off loss derived from waveforms is overestimated which should deduct the energy stored in C_{DS}+C_{GD}. Both the experiments and proposed model show that the turn on loss dominates the total switching loss under hard-switching conditions.

Furthermore, the turn on loss increases significantly if the freewheeling diode has a reverse recovery charge, because both the current overshoot and transition time will increase.

B. Buck converter efficiency verification

The second method used to validate the accuracy of the proposed analytical model is to observe the converter efficiency over a wide load range. A 500 kHz 380V/200V buck converter is built using a cascode GaN transistor as the top and bottom switch. In the calculation terms, the inductor loss is measured by Mu's method [E.14]. The conduction loss is calculated based on the steady state current and on-resistance, which takes the temperature coefficient into consideration. The driving loss can be approximately calculated as

$$P_{dri}(t) = Q_g V_G F_s \tag{A.46}$$

Figure.A 18 shows the converter efficiency comparison between the experimental results and the calculation results based on the proposed model. The calculated efficiency matches well with the experimental results over a wide load range. The difference is within 0.1%.

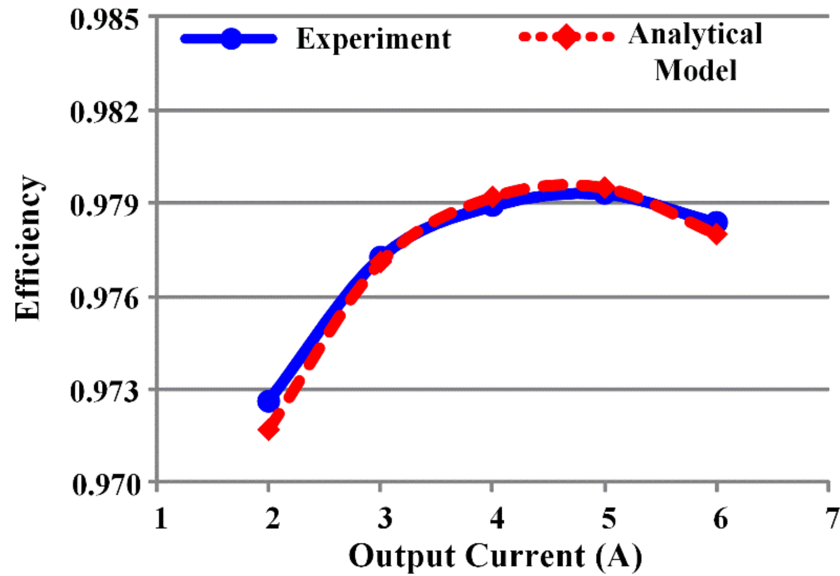


Figure.A 18 Efficiency comparison between experimental and calculation results based on proposed model

To further validate the accuracy of this model, the buck converter is purposely operated at critical model (CRM) to eliminate the turn on switching loss (as in this input-output condition, the top switch can achieve zero-voltage-switching turn on without switching loss). The switching frequency at full load is set as 500 kHz, and increases to 1.2 MHz at light load. The converter efficiency is tested, and the results are shown in Figure.A 19 along with the calculation results based on the proposed model. The figure clearly shows that the analytical model closely matches with the experimental results.

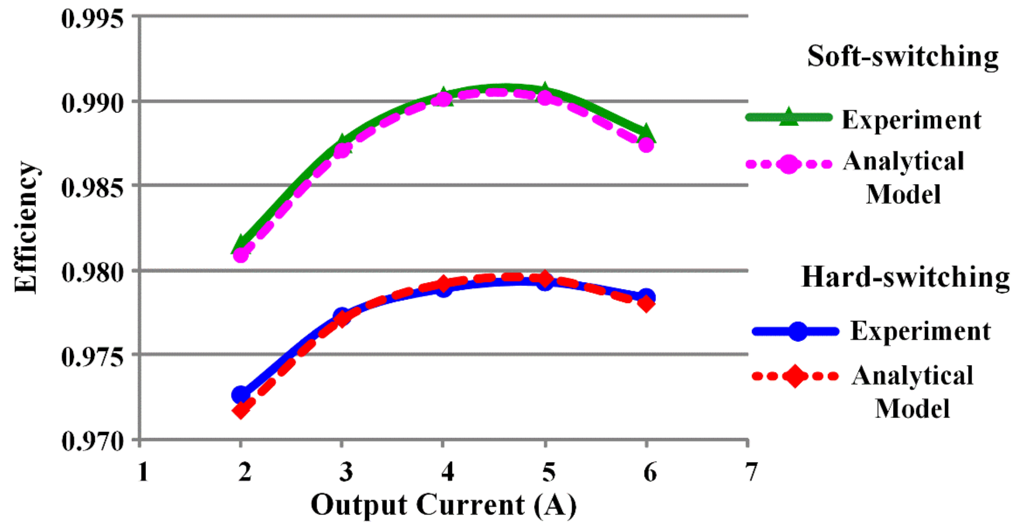


Figure.A 19 Efficiency comparison between experimental results and calculation results based on proposed model

As the analytical model can match with the experiments for both hard-switching and soft-switching conditions over a wide load range, the proposed model is applied to analyze the loss breakdown of the buck converter at 6A output condition, as shown in Figure.A 20. The results verify that the turn on loss is dominant in total switching loss under hard-switching conditions. However, under soft-switching operation, turn on loss is minimized, and there is consequently some conduction loss. It should be noted that the turn off loss remains low even when the turn off current doubles. This characteristic makes the cascode GaN transistor very suitable for high frequency operation as long as zero-voltage-switching turn on is achieved.

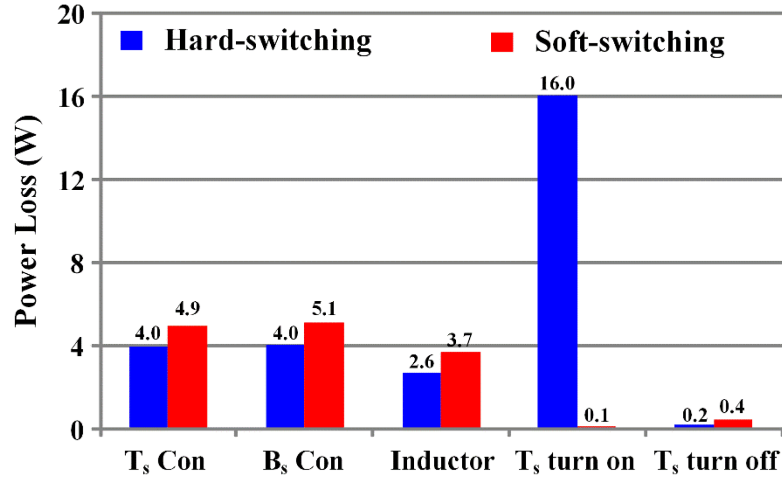


Figure.A 20 Buck converter loss breakdown based on proposed loss model

This appendix presents a new analytical loss model for a high voltage cascode GaN device. The model considers the parasitic inductance and the nonlinearity of the capacitors and transconductance. The turn on/off processes are illustrated using a simplified equivalent circuit for each transition. The accuracy of the proposed model is validated by numerous experimental results.

It is worth pointing out that, both the results from analytical model and experiments show that the turn on loss dominates the total switching loss under high voltage hard-switching conditions, which is quite different from the loss characteristics under low voltage conditions. The main reason for this disparity is that extra current is required to charge the bottom switch junction capacitors (Q_{coss}) or reverse recovery charge (Q_{rr}) under hard-switching, high voltage conditions, while the drain-source voltage remains high. This applies to bridge configuration based converters such as buck, boost, and buck-boost. On the other hand, the turn off loss is negligible due to the intrinsic current source driving mechanism which is unique to the cascode configuration. This characteristic makes the

cascode GaN transistor very suitable for high frequency operation as long as zero-voltage-switching turn on is achieved which is verified by the soft-switching experimental results.

Appendix B. GaN Converter with Inverse Coupled Inductor

The bidirectional buck/boost converter is widely used in the power electronics system due to its simplicity and high efficiency, such as the on board charger/discharger for plug-in hybrid electric vehicles [F.1]-[F.3], and the interfaced converter for the energy storage systems[F.4] and [F.5]. Conventional silicon device based bidirectional buck/boost converters are usually intended to be operated in discontinuous current mode (DCM) in order to alleviate reverse recovery issues and to use a small inductor. However, the DCM operation greatly increases turn-off loss because the main switch is turned off at least twice of the load current. As a result, the switching frequency can barely be pushed to hundreds of kilo-hertz due to power loss considerations.

Critical current mode (CRM) operation is the most simple and effective way to achieve ZVS, and is widely used in medium-low power applications [F.6]-[F.8]. CRM operation introduces a large current ripple, which is at least twice of the load current. It is necessary to interleave multiple phases to cancel the switching frequency current ripple and lead to a smaller EMI filter. However, the ZVS range of the CRM dc-dc converter is determined by the input and output voltage, which will significantly impact switching loss at high frequency. Furthermore, the resonant period formed by the inductor and device junction capacitors is too long at high frequency, which leads to a large circulating energy. The limitations of CRM operation at high frequency are discussed in Section I.

The concept of the coupled inductor has been applied successfully in interleaved voltage regular modules for the improvement of the efficiency and transient response [F.9]. The inverse coupled inductor has also been evaluated in the interleaved CRM boost PFC

converter which aims to reduce magnetic volume [F.10]. However, the impact of the coupled inductor on the behavior of the converter during the resonant period, which is unique to CRM operation, has not yet been analyzed.

This appendix aims to analyze the behavior of interleaved buck/boost converter with an inverse coupled inductor operating in CRM. The derivation of the equivalent inductance of the inverse coupled inductor in CRM is illustrated in Section II. The benefits of the inverse coupled inductor in CRM is analyzed in Section III, including resonant period reduction, and an improvement in ZVS range and circulating energy. Finally, the theoretical analysis is validated by experimental results.

I. Limitations of CRM Operation at High Frequency

When the bidirectional buck/boost converter, which is shown in Figure B. 1, operates in CRM, it can achieve zero current turn-on for the main switch and zero current turn-off of the free-wheeling switch, thus avoiding reverse recovery problems. Switch Ts is the main switch in the buck direction, while Bs is the main switch in the boost direction. If the main switch turn-on instant is set to exactly half the resonant period after the inductor current crosses zero via any zero-current detection technique, the switch achieves minimum voltage turn on. Figure B. 2Fig. 2 shows the key CRM operation waveforms for both buck operation and boost operation.

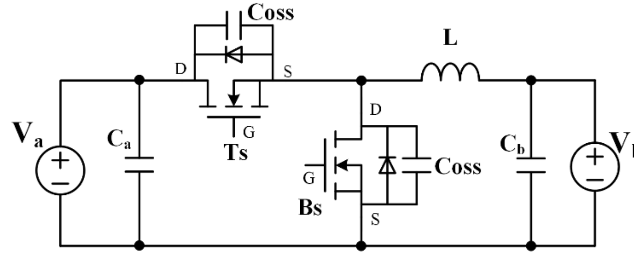
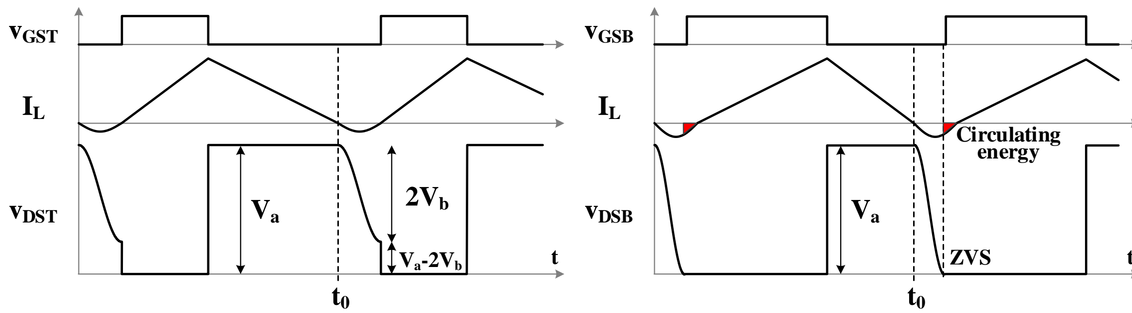


Figure B. 1 Bidirectional buck/boost converter



(a) buck direction (b) boost direction

Figure B. 2 Key waveforms of CRM operation for buck/boost converter

v_{DST} and v_{DSB} are the drain-source voltage of Ts and Bs, respectively. The inductor current crosses zero at t_0 and then the inductor oscillates with the junction capacitors of the two devices. It is easy to derive the voltage oscillation peak-to-peak amplitude for both directions, which is $2*V_b$ for the buck direction and $2*(V_a-V_b)$ for the boost direction. Fig. 2 shows a 380V to 150V conversion as an example. The main switch Ts is turned on at the valley point, which is 80V (V_a-$2*V_b$) in the buck direction. The main switch Bs in the boost direction can easily achieve ZVS since the resonant amplitude $2*(V_a-V_b)$ is larger than the device initial voltage, which is V_a. The extra circulating energy is marked by the red shadow region Therefore, one direction will lose ZVS and the other direction will have extra circulating energy except for the special case where V_a is exactly twice V_b. The

switching loss and circulating energy will increase with the frequency, which will deteriorate the efficiency significantly at high frequency.

Another limiting factor of CRM operation at high frequency is the resonant time T_r, which is half of the resonant period formed by L and the junction capacitors of the devices, which is expressed as (B.1):

$$T_r = \pi \cdot \sqrt{L \cdot 2C_{OSS}} \quad \text{(B.1)}$$

During the resonant period, the charge stored in the junction capacitor of the main switch is recycled to the source, while the same amount of charge is stored in the junction capacitor of the free-wheeling switch. Therefore, the negative charge of the inductor current, which does not transfer energy to the output, is constant no matter what the switching frequency is. Figure B. 3 shows the trend that T_r/T_s increases with the switching frequency. As a result, the rms value of the inductor current will increase with the switching frequency as shown in Figure B. 4, whereas the output current remains same at different switching frequency. Both of these two curves are derived from simulation. At 5MHz, the resonant period occupies 28% of the total switching period, and the rms value of inductor current is 1.57 times the output current. Figure B. 5 shows a 5MHZ experiment waveform with the resonant period clearly marked.

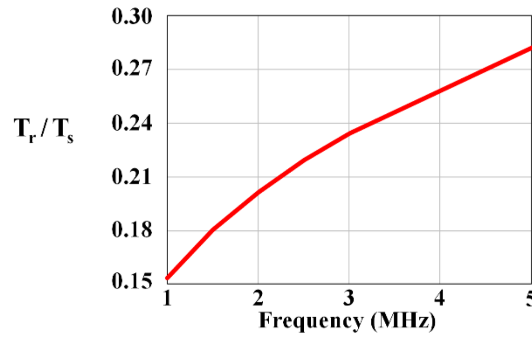


Figure B. 3 Relationship between T_r and T_s in CRM

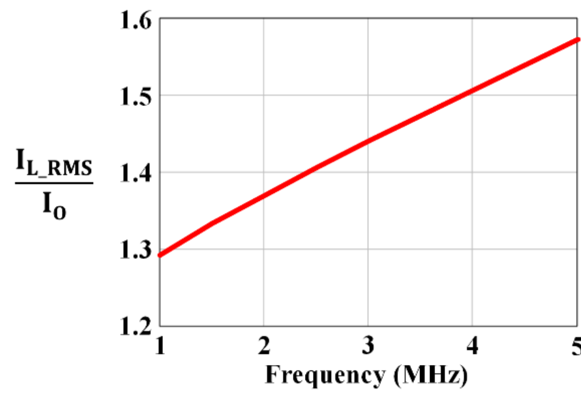


Figure B. 4 Inductor current rms value increases with frequency in CRM

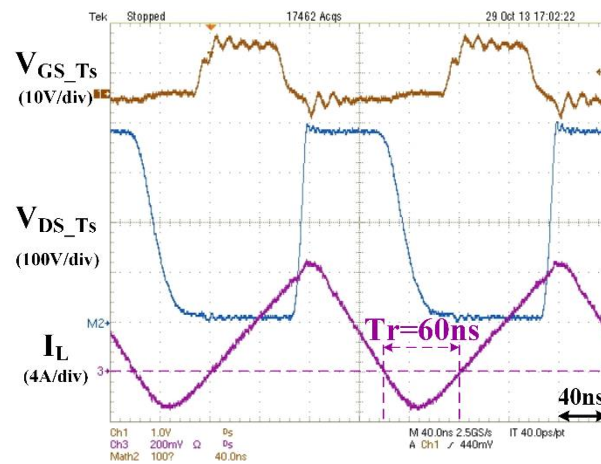


Figure B. 5 CRM operation experimental waveforms at 5MHz

One way to solve the limitations of conventional CRM operation is to utilize the quasi-square-wave soft-switching technique [F.11] and [F.12]. However, the negative portion of the inductor current grows larger under light load conditions, which will significantly deteriorate the converter efficiency. Another solution is to use a coupled inductor to improve the CRM performance, including ZVS range extension/circulating energy reduction and resonant period reduction. This process is analyzed in detail in Sections II and III.

II. Equivalent Inductance Derivation at CRM

The interleaved bidirectional buck/boost converter with inverse coupled inductor is shown in Figure B. 6. For simplicity, the two self-inductances are considered to be the same (L_1=L_2=L). The inverse coupled mutual inductance M is usually expressed as:

$$M = k \cdot L\,,\ k < 0 \tag{B.2}$$

where k is coupling coefficient.

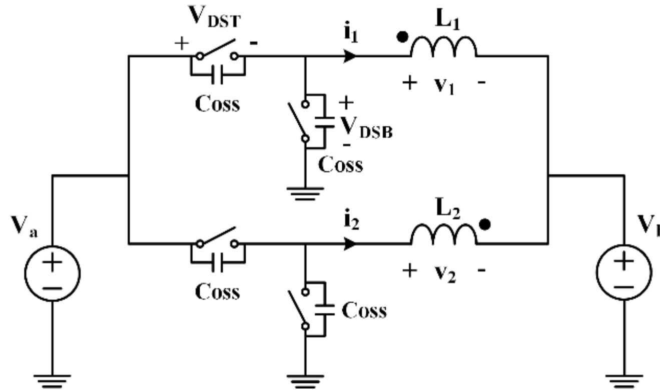
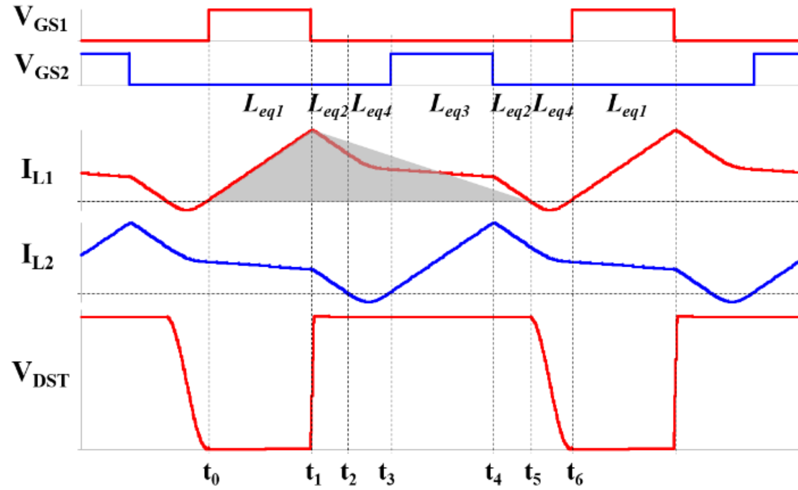


Figure B. 6 Interleaved buck/boost converter with inverse coupled inductor

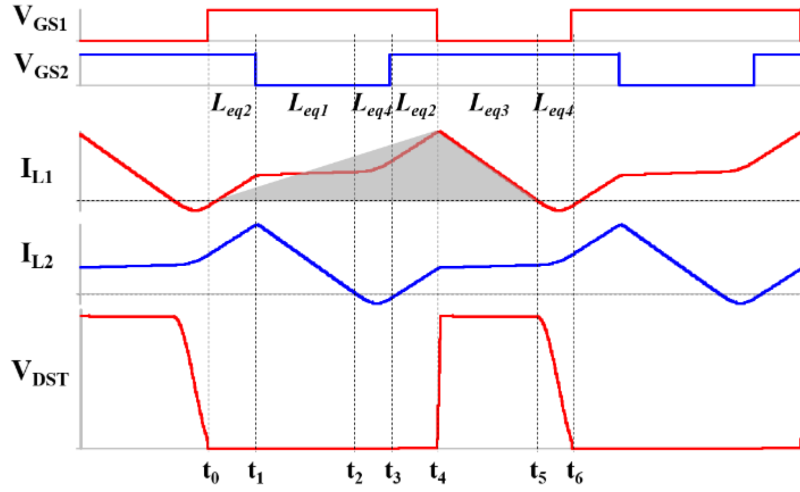
The analysis of the inverse coupled inductor in continuous current mode (CCM) operation is illustrated in [F.9]. For CRM operation, there are two more resonant periods

in each switching cycle than in CCM operation. The derivation of the equivalent inductance in CRM operation is shown below. The analysis of boost direction is a duplicate of the buck direction analysis.

The key waveforms for D<0.5 is shown in Figure B. 7(a), where D is the duty cycle. For the buck direction, $D=V_b/V_a$. There are six time intervals in one switching cycle. The time intervals t_0-t_1, t_1-t_2, t_3-t_4, and t_4-t_5 are the same with a conventional two phase buck converter with a coupled inductor. The time intervals t_2-t_3 and t_5-t_6 are the resonant periods that are different from the previous analysis. The derivation of the equivalent inductance during t_0-t_1, t_1-t_2, t_3-t_4, and t_4-t_5 can be found in [F.9], which is summarized in Table B.1. This paper focuses on analyzing the coupled inductor behavior during the resonant period.



(a) D<0.5



(b) D>0.5

Figure B. 7 Key waveforms of CRM with coupled inductor considering resonant period

Table B. 1 Coupled inductor equivalent inductance[15]

L_{eq1}	L_{eq2}	L_{eq3}
$\frac{L^2-M^2}{L+\frac{D}{D'}M}$	$(L+M)$	$\frac{L^2-M^2}{L+\frac{D'}{D}M}$

$* D' = 1 - D$

The basic equation for the coupled inductor is:

$$\begin{cases} v_1 = L \cdot \frac{di_1}{dt} + M \cdot \frac{di_2}{dt} \\ v_2 = L \cdot \frac{di_2}{dt} + M \cdot \frac{di_1}{dt} \end{cases} \tag{B.3}$$

where v_1, v_2 and i_1, i_2 are as marked in Figure B. 6.

During t_5 to t_6, the Phase 1 inductor current drops to zero, and then resonates with the junction capacitors of the two devices, while the Phase 2 inductor is still free-wheeling through the bottom switch. The voltage across the two inductors can be expressed as:

$$v_1=v_{DSB}-V_b,\ v_2=-V_b \tag{B.4}$$

Meanwhile, the Phase 1 inductor current is related to the charge and discharge current of the two junction capacitors, which can be expressed as:

$$i_1 = -2C_{OSS} \cdot \frac{dv_{DSB}}{dt} \tag{B.5}$$

Substituting v_1, v_2, and i_1 into (B.3), (B.3) can be rewritten as follows:

$$(L - \frac{M^2}{L}) \cdot 2C_{OSS} \cdot \frac{d^2 v_{DSB}}{dt^2} + v_{DSB} = V_b(1 - \frac{M}{L}) \tag{B.6}$$

This is a two-order system from which we can define the equivalent resonant inductance mathematically,

$$L_{eq4} = L - \frac{M^2}{L} \tag{B.7}$$

To better understand the meaning of the equivalent resonant inductance, the derivation process based on the equivalent circuit is also demonstrated in Figure B. 8. Figure B. 8 (a) shows the original circuit with a coupled inductor during the resonant period. Figure B. 8 (b) shows the equivalent circuit with decoupled inductors. The voltage source V_a is neglected since it only impacts the initial value. Based on Norton's Theorem, the voltage source V_b in series with the inductor M can be replaced by a current source in parallel with an inductor as shown in Figure B. 8 (c). Then based on Thevenin's Theorem, the current source in parallel with an inductor can be represented as a voltage source in series with an

inductor, as shown in Figure B. 8 (d). Therefore, the equivalent inductance derived from the circuit is same with mathematic derivation.

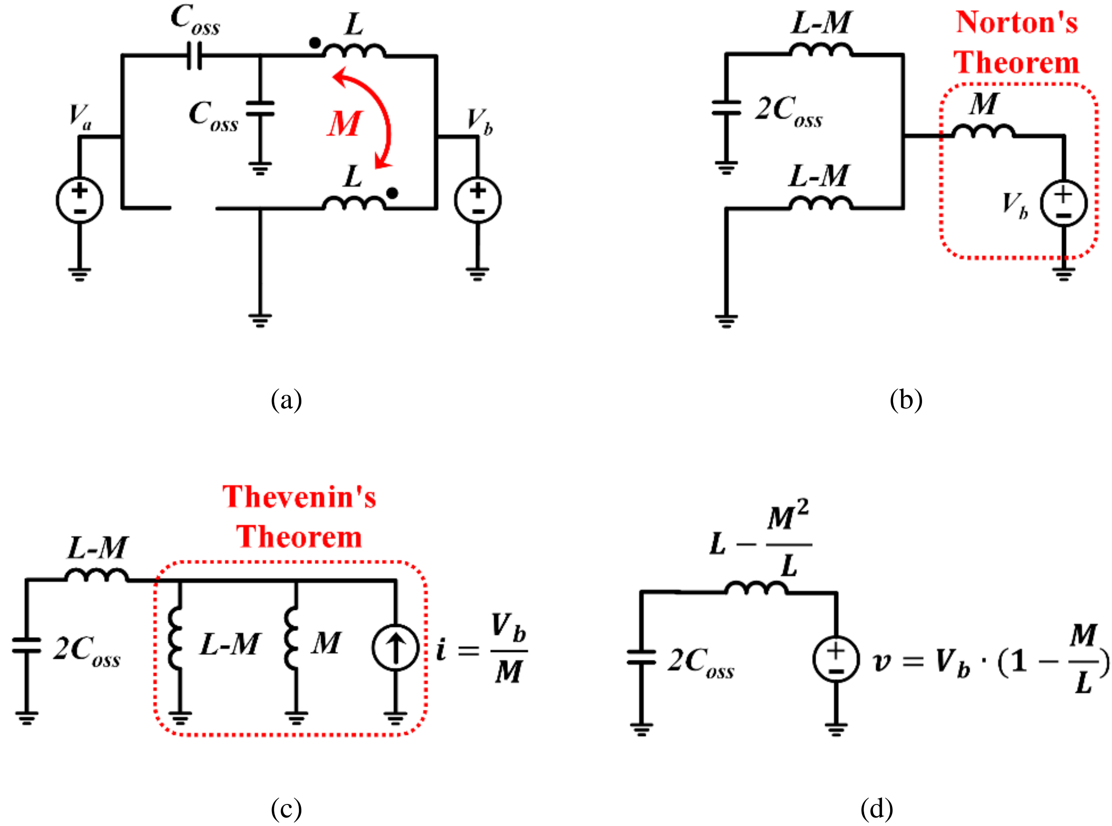


Figure B. 8 Equivalent inductance derivation via equivalent circuit @D<0.5 (a) Initial circuit during resonant period (b) Decoupled inductor (c) Circuit derivation with Norton's Theorem (d) Circuit derivation with Thevenin's Theorem

The aforementioned equivalent inductance derivation is focused on Phase 1. Following the same process, the equivalent inductance for Phase 2 can also be obtained. Even though the Phase 2 is on the free-wheeling period, the resonant current in Phase 1 will be reflected to Phase 2 due to the coupling effect. Therefore, the current waveform of phase 2 shown in Figure B. 7(a) during t_5-t_6 is part of the sinusoid shape.

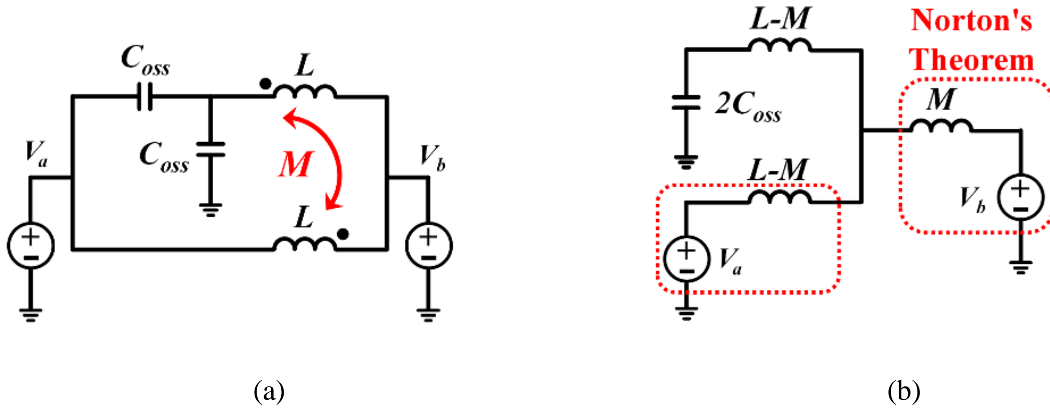
According to (B.6), the voltage waveform v_{DST} during the resonant period could be derived as follows:

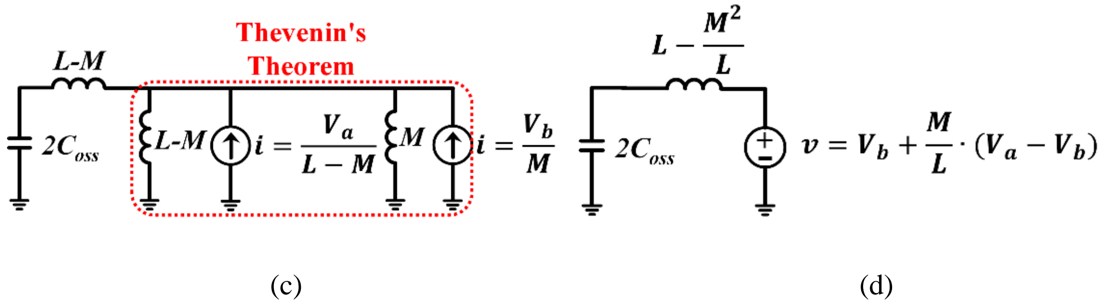
$$v_{DST} = V_a - V_b \cdot \left(1 - \frac{M}{L}\right) \cdot [1 - \cos(\frac{t}{\sqrt{(L-\frac{M^2}{L})\cdot 2C_{OSS}}})] \quad \text{(B.8)}$$

It is evident that the resonant amplitude is related to the mutual inductance. Therefore, the inverse coupled inductor modifies the converter behavior in CRM.

The same process can be applied when D>0.5. The key waveforms for the D>0.5 condition are shown in Figure B. 7(b). The equivalent circuit is shown in Figure B. 9 with detailed derivation steps. The equivalent inductance during resonant period is also $L - \frac{M^2}{L}$ when D>0.5. The voltage v_{DST} can be derived as:

$$v_{DST} = V_a - [V_b + \frac{M}{L} \cdot (V_a - V_b)] \cdot [1 - \cos(\frac{t}{\sqrt{(L-\frac{M^2}{L})\cdot 2C_{OSS}}})] \quad \text{(B.9)}$$





(c) (d)

Figure B. 9 Equivalent inductance derivation via equivalent circuit @D>0.5 (a) Initial circuit during resonant period (b) Decoupled inductor (c) Circuit derivation with Norton's Theorem (d) Circuit derivation with Thevenin's Theorem

The derivation of the equivalent inductance in the boost direction is identical to the process of the buck direction, which will not be repeated here. The key equation to describe v_{DSB} during the resonant period is shown below. It indicates that the equivalent resonant inductance for the boost direction is also $L-\frac{M^2}{L}$.

$$\begin{cases} v_{DSB} = V_a - \left[V_a - V_b\cdot\left(1-\frac{M}{L}\right)\right]\cdot\left[1-\cos\left(\frac{t}{\sqrt{(L-\frac{M^2}{L})\cdot 2C_{OSS}}}\right)\right], & \frac{V_b}{V_a} < 0.5 \\ v_{DSB} = V_a - (V_a - V_b)\cdot\left(1-\frac{M}{L}\right)\cdot\left[1-\cos\left(\frac{t}{\sqrt{(L-\frac{M^2}{L})\cdot 2C_{OSS}}}\right)\right], & \frac{V_b}{V_a} > 0.5 \end{cases} \tag{B.10}$$

Table B.2 summarizes the major difference between the non-coupled and inverse coupled inductors for both directions. The impact of the coupled inductor on the CRM operation is analyzed in Section IV.

Table B. 2 Comparison between non-coupled inductor and inverse coupled inductor

<table>
<tr><td rowspan="3"></td><td colspan="2">Resonant inductance</td><td colspan="3">Resonant amplitude</td></tr>
<tr><td rowspan="2">Non-coupled</td><td rowspan="2">Inverse coupled</td><td rowspan="2">Non-coupled</td><td colspan="2">Inverse coupled</td></tr>
<tr><td>$V_b<0.5V_a$</td><td>$V_b>0.5V_a$</td></tr>
<tr><td>Buck</td><td>L</td><td>$L-\frac{M^2}{L}$</td><td>V_b</td><td>$V_b\cdot\left(1-\frac{M}{L}\right)$</td><td>$V_b+\frac{M}{L}\cdot(V_a-V_b)$</td></tr>
<tr><td>boost</td><td>L</td><td>$L-\frac{M^2}{L}$</td><td>V_a-V_b</td><td>$V_a-V_b\cdot\left(1-\frac{M}{L}\right)$</td><td>$(V_a-V_b)\cdot\left(1-\frac{M}{L}\right)$</td></tr>
</table>

III. Benefits of Inverse Coupled Inductor at CRM Operation

A. Reduction of resonant period

As shown in Figure B. 7(a), the current decay slope are the same during [t_1-t_2] and [t_4-t_5], and the time intervals of [t_1-t_2] and [t_4-t_5] are the same, so the area between the current waveform and the time axis is equal to the shaded area. This principle also is true when D>0.5, which is shown in Figure B. 7(b). Hence, same as the non-coupled case, the peak current of each phase of the coupled inductor is approximately twice of its average value, if the negative current is ignored.

For the coupled inductor case, it is apparent that L_{eq1} and L_{eq3}, determine the peak value of the inductor current when D<0.5 and D>0.5, respectively. For a non-coupled inductor, each phase inductance L_{nc} determines the peak inductor current. To get the same

average inductor current, L_{eq1} and L_{eq3} should be the same as L_{nc} when D<0.5 and D>0.5, respectively, which is expressed as follows:

$$\begin{cases} \mathrm{L_{nc}} = \mathrm{L_{eq1}} = \mathrm{L} \cdot \frac{1-\mathrm{k}^2}{1+\frac{\mathrm{D}}{\mathrm{D}'}\mathrm{k}} & D < 0.5 \\ \mathrm{L_{nc}} = \mathrm{L_{eq3}} = \mathrm{L} \cdot \frac{1-\mathrm{k}^2}{1+\frac{\mathrm{D}'}{\mathrm{D}}\mathrm{k}} & D > 0.5 \end{cases} \tag{B.11}$$

As the equivalent resonant inductance with a coupled inductor is $L_{eq4} = L - \frac{M^2}{L}$ which can be rewritten as $L_{eq4} = \mathrm{L}(1-\alpha^2)$, the relation between L_{eq4} and L_{nc} can be expressed as:

$$\begin{cases} \mathrm{L_{eq4}} = \mathrm{L}_{nc} \cdot (1 + \frac{\mathrm{D}}{\mathrm{D}'}\mathrm{k}) & D < 0.5 \\ \mathrm{L_{eq4}} = \mathrm{L}_{nc} \cdot (1 + \frac{\mathrm{D}'}{\mathrm{D}}\mathrm{k}) & D > 0.5 \end{cases} \tag{B.12}$$

The inverse coupling coefficient k is negative which means the equivalent resonant inductance of a coupled inductor is always smaller than a non-coupled inductor. As shown in Figure B. 10, the equivalent resonant inductance decreases with the coupling coefficient and reaches the lowest value when D=0.5. Accordingly, the resonant period with coupled inductor is also reduced compared to non-coupled case as shown in Figure B. 11.

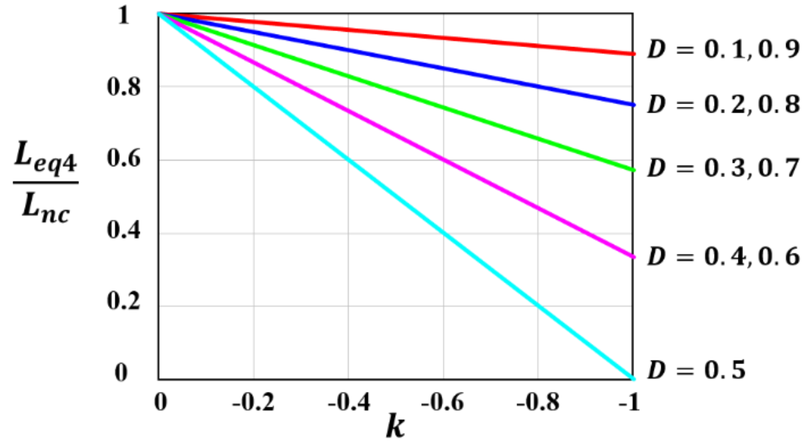


Figure B. 10 Reduction of resonant inductance with different coupling coefficient and voltage gain

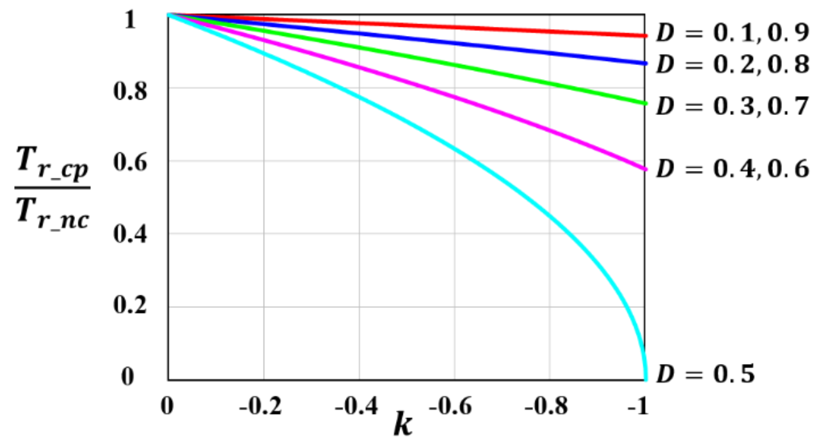


Figure B. 11 Reduction of resonant period with different coupling coefficient and voltage gain

The portion of transferring energy increases with the reduction of the resonant period in CRM, which leads to a reduction of conduction loss. Figure B. 12 shows the theoretical calculation results of the rms value reduction of the inductor current when D=0.6, k=-0.4. The bottom curve shows a 5% reduction of inductor current when using a coupled inductor rather than a non-coupled inductor at 5MHz, as well as a 10% reduction of the converter conduction loss.

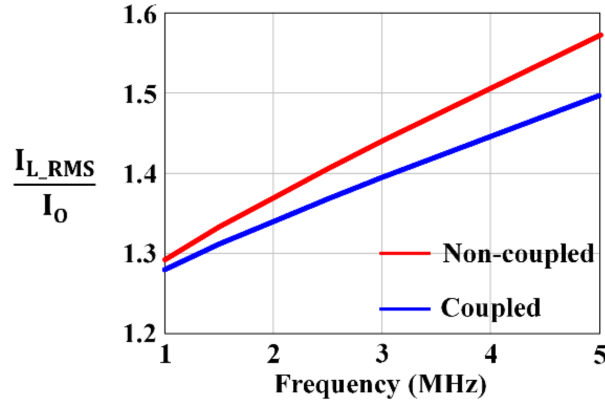


Figure B. 12 Reduction of inductor current rms value with coupled inductor

B. Extension of ZVS range when D<0.5 or reduction of circulating energy when D>0.5

For a bi-directional buck/boost converter with a non-coupled inductor operating in CRM, one of the directions operates at D<0.5 and switches at the valley point, as shown in Figure B. 2(a), while the other direction operates at D>0.5 and can achieve ZVS easily with extra circulating energy. Even valley switching minimizes the turn-on switching loss, the remaining energy stored in the junction capacitor is still considerable at MHz switching frequency. A similar argument can also be applied to the circulating energy as this part of the power loss is a linear function of the switching frequency.

However, the inverse coupled inductor can modify the converter behavior during the resonant period. As shown in Table II in Section III, the resonant amplitude with an inverse coupled inductor is different from the resonant amplitude with a non-coupled inductor. Taking a V_a=380V, and V_b=150V conversion as an example, in the buck direction, ZVS cannot be achieved with a non-coupled inductor operating in CRM since V_b is smaller than $0.5V_a$. However, ZVS can be achieved with an inverse coupled inductor as long as the coupling coefficient is in the range of $-1< k<-0.3$ and makes $V_b \cdot (1-k)$ greater than $0.5V_a$.

In the boost direction, ZVS can be easily achieved with a non-coupled inductor with extra circulating energy since the resonant amplitude V_a-V_b is greater than $0.5V_a$. While the coupled inductor reduces the resonant amplitude to $[V_a - V_b \cdot \left(1 - \frac{M}{L}\right)]$. ZVS still can be achieved as long as k is in the range of -1< k<-0.3. Therefore, designing coupling coefficient to be around -0.3 is most beneficial for both directions.

Figure B. 13 summarizes the benefit of the ZVS range extension and circulating energy reduction with an inverse coupled inductor. The solid line is the ZVS boundary condition, which is the most desired operation point. Regions I and III represent valley switching for the buck direction, while they represent ZVS with circulating energy for the boost direction. Regions II and IV represent ZVS with circulating energy for the buck direction but valley switching for the boost direction. If the operation point is close to the ZVS boundary line, there is smaller turn-on switching loss in one direction and smaller circulating energy in the other direction.

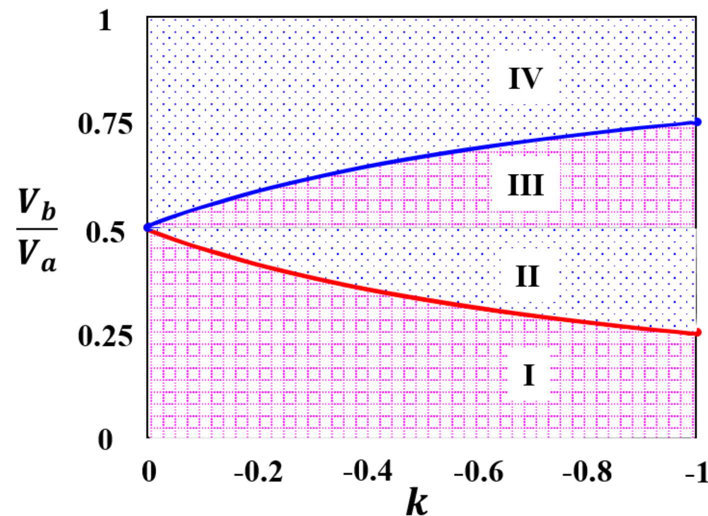


Figure B. 13 Coupled inductor modifies CRM operation

For the non-coupled inductor case, the only ZVS boundary point for both directions is $\frac{V_b}{V_a}$=0.5. For the inverse coupled inductor case, the ZVS boundary is stretched to two lines. When the voltage gain ratio $\frac{V_b}{V_a}$ is between 0.25 and <0.75, the operation point can be located on the ZVS boundary line at certain coupling coefficients, as shown in Figure B. 13. When $\frac{V_b}{V_a}$ is <0.25 or >0.75, the operation point moves to Regions I and IV. However, the operation point is much closer to the ZVS boundary line than in the non-coupled condition. This indicates a reduction of turn-on switching loss and circulating energy. Over all, the inverse coupled inductor improves the converter performance in CRM operation.

When apply inverse coupled inductor in high frequency two phase interleaved CRM PFC converter, the aforementioned benefits will definitely improve the converter efficiency. Take the two phase CRM totem-pole PFC, which is discussed in [F.6], as an example. The non-ZVS valley switching is inevitable with non-coupled inductor when the input voltage is higher than half of the output voltage, which causes a considerable switching loss at high frequency. On the other hand, ZVS could be easily achieved with extra circulating current when the input voltage is lower than half of the output voltage, which causes the additional conduction loss. With inverse coupled inductor, the non-ZVS valley switching region will be narrowed and the circulating current would be reduced since the operation point is moving closer to the ZVS boundary line as illustrated in Figure B. 13. Therefore it takes less effort to achieve ZVS by operating at QSW mode [F.6]. Moreover, QSW mode cannot solve the circulating current problem.

IV. Experimental Results and Discussions

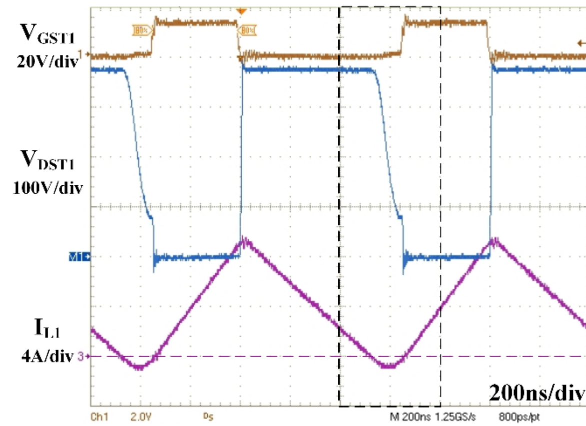
To validate the benefit of the converter operating in CRM with inverse coupled inductor, a 380V-150V two-phase interleaved CRM buck/boost converter is built. The output current is 8A for the buck direction and 3A for the boost direction. The converter can operate with both an inverse coupled inductor and a non-coupled inductor for comparison. The 600V GaN HEMT from Transphorm is used as the active switch, since the turn off switching loss is negligible, which means it is suitable for CRM operation and can be pushed to very high frequency. The switching frequency is set to be 1MHz at full load condition to reduce the size of the passive components. An UI-shaped core with 3F45 material is used in the prototype, and the air gap is fine tune to achieve a certain coupling coefficient. Two ER23 core with 3F45 material are used as the non-coupled inductors for comparison. The prototype is shown in Figure B. 14. The coupled inductor saves 50% footprint and 25% volume compared with two non-coupled inductors. The design and optimization of the coupled inductor is a complex process which is not addressed in this appendix. The experiments shown below only focus on the analysis illustrated in Sections II and III.

Figure B. 14 Comparison of coupled and non-coupled inductor

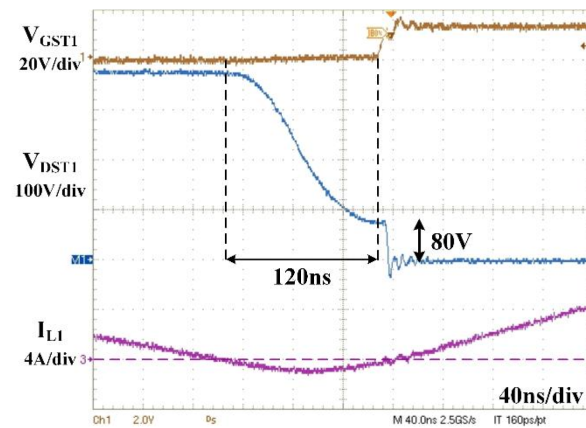
The steady state inductance for the non-coupled inductor is 8uH, and determines the peak current and output current. For the inverse coupled inductor case, L_{eq1} and L_{eq3}, determine the peak and average values of the inductor current in the buck direction and boost direction, respectively. The Table B.1 shows the relationship between these two inductors and the self-inductance, coupling coefficient and duty cycle. In the prototype, the self-inductance is 8uH, and the coupling coefficient is -0.4.

Figure B. 15 shows the bidirectional waveforms with a non-coupled inductor. The detailed waveforms during the resonant period for the buck and boost direction are shown in Figure B. 15(b) and Figure B. 15(d), respectively. As the voltage conversion ratio has been set from 380V to 150V, the buck direction loses ZVS and the boost direction achieves ZVS with extra circulating energy, as marked in the figure. In the buck direction, the main switch is turned on at 80V, which means there is an approximately 1W turn-on switching loss at 1MHz. In the boost direction, the circulating energy induces roughly 0.5W extra conduction loss at 1MHz. The resonant period of the buck direction measured from the

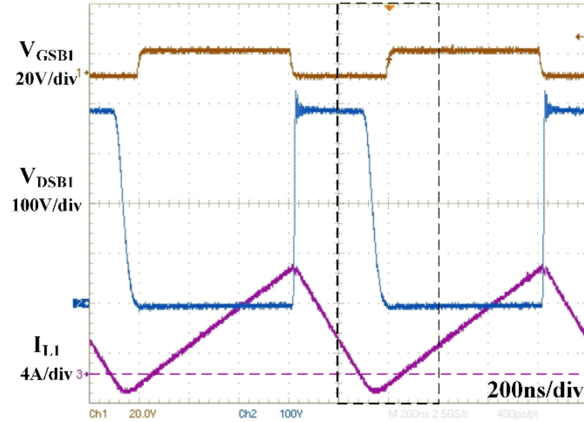
waveform is about 120ns. It is shorter in the boost direction since the inductor voltage is clamped by V_b after the main switch achieves ZVS. The rms value of inductor current is 5.2A for both direction.



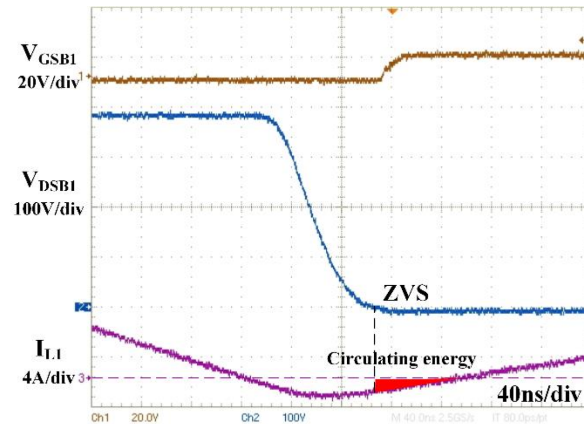
(a) Buck direction



(b) detailed resonant period



(c) Boost direction

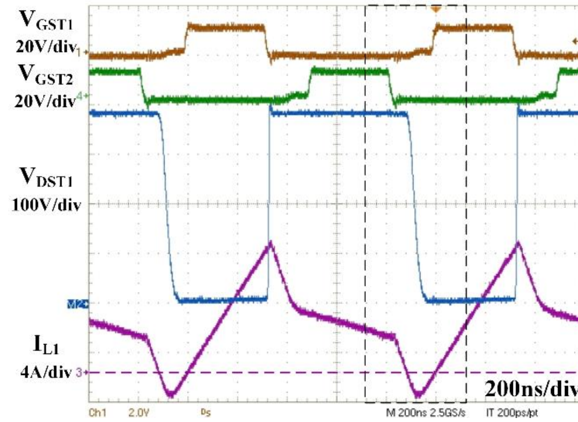


(d) detailed resonant period

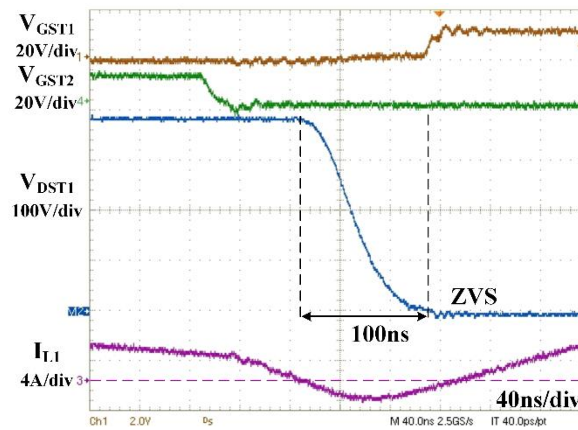
Figure B. 15 Experimental waveforms of CRM operation with non-coupled inductor

Fig. 16 shows the bidirectional waveforms with an inverse coupled inductor. The detailed waveforms during resonant period for the buck and boost direction are shown in Fig. 16(b) and Fig. 16(d), respectively. Fig. 16 clearly shows the ZVS achievement for the buck direction and a circulating energy reduction for the boost direction with a coupled inductor. The theoretical resonant period reduction according to Fig. 11 is about 15% with a coupled inductor. The resonant period measured from the waveform is about 100ns, which matches with the theoretical analysis. The rms value of inductor current is 5A for

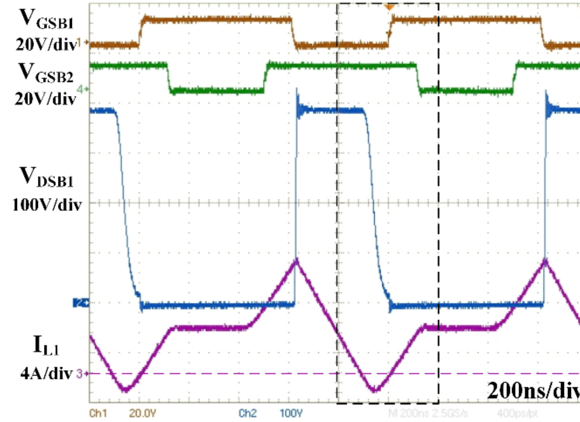
both direction, which reduces 4% compared with non-coupled case. The measured efficiency at full load output with a coupled inductor for both direction is 98.5%.



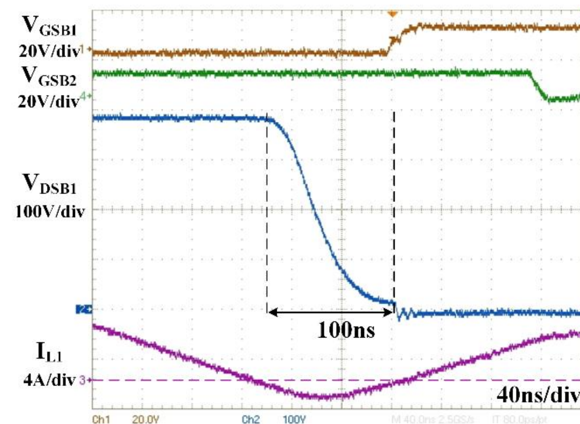
(a) buck direction



(b) detailed resonant period



(c) boost direction



(d) detailed resonant period

Figure B. 16 Experimental waveforms of CRM operation with coupled inductor

The loss breakdown of two-phase buck direction at full load is shown in Figure B. 17. It clearly shows that the coupled inductor eliminates the turn on switching loss by ZVS range extension. Moreover, coupled inductor slightly reduce the conduction loss due to small reduction of rms current as mentioned in Figure B. 12. Core loss is also reduced with coupled inductor since core volume can be shrink due to certain DC flux cancelation. Overall, coupled inductor saves about 4W power loss and improves efficiency by 0.3% at full load condition. It should be pointed out that the inductor is not optimized in terms of losses, and therefore, there is still room to improve the efficiency.

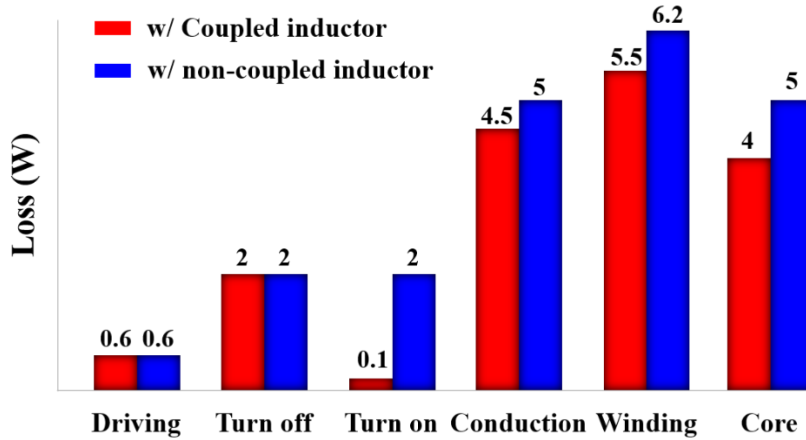


Figure B. 17 Loss breakdown of two-phase buck direction at full load

The full load range efficiency of buck direction is shown in Figure B. 18. The efficiency of boost direction is similar. The switching frequency increases when the load current reduces due to the nature of CRM operation. The switching related loss becomes the dominant part at light load condition. Therefore, the coupled inductor saves more loss at light load and the efficiency improvement is over 2%.

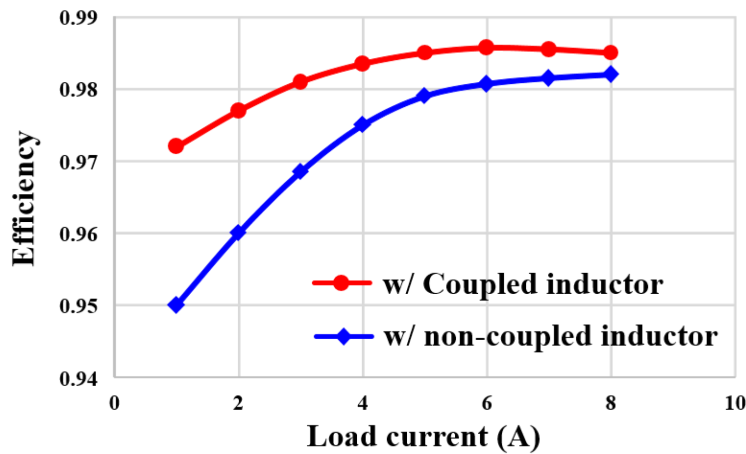


Figure B. 18 Efficiency comparison over wide load range of buck direction

This appendix aims to analyze the benefits of the inverse coupled inductors in CRM operation based on a 1MHz interleaved buck/boost converter with GaN devices. The converter behavior during the resonant period is improved with an inverse coupled inductor. There is a reduction of the resonant period, an extension of the ZVS range when $D<0.5$ and a reduction of the circulating energy when $D>0.5$. All of these characteristics are beneficial for high frequency operation in terms of conduction and switching loss reduction. The coupled inductor prototype efficiency is 98.5% at 1MHz, which is 0.3% higher than the efficiency of the non-coupled inductor, which validate the theoretical analysis

Though this is not covered in this dissertation, it is worth pointing out that the coupled inductor provides a potential opportunity for magnetic integration. With DC flux cancellation, the coupled inductor could be further integrated, which would increase the power density.

References

A. Introduction

[A.1] N. Kaminski, "State of the art and the future of wide band-gap devices," *in Proc. IEEE Power Electronics and Applications*, 2009, pp. 1–9.

[A.2] Infineon, "CoolMOSTM C6 Mastering the art of slowness," Application note, Dec. 2009.

[A.3] A. Lidow, J. Strydom, M. D. Rooij, and D. Reusch, GaN Transistors for Efficient Power Conversion, 2nd Edition, Wiley, 2014.

[A.4] E. Mitani, H. Haematsu, et al. "Mass production of high voltage GaAs and GaN devices," *CS Mantech Conference*, Vancouver B. C., Canada, Apr.24-27, 2006.

[A.5] U. K. Mishra, P. Parikh, and Y. Wu, "AlGaN/GaN HEMTs - an overview of device operation and applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp.1022-1031, Jun. 2002.

[A.6] B. Ozpineci, and L. M. Tolbert. Comparison of wide-bandgap semiconductors for power electronics applications. United States. Department of Energy, 2004.

[A.7] C. E. Weitzel, J. W. Palmour,C. H. et al., "Silicon carbide high-power devices," *IEEE Trans. on Electron Devices*, vol.43, no.10, pp.1732-1741, Oct. 1996.

[A.8] J. A. Cooper, M. R. Melloch, et al. "Status and prospects for SiC power MOSFETs," *IEEE Trans. on Electron Devices*, vol.49, no.4, pp.658-664, Apr. 2002.

[A.9] M. A. Khan, G. Simin, S. G. Pytel, A. Monti, E. Santi, and J. L. Hudgins, "New developments in gallium nitride and the impact on power electronics," *in Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 15–26.

[A.10] B. J. Baliga, and M. S. Adler, "Composite Circuit for Power Semiconductor Switching," European Patent EP 0063749 B1, 1982.

[A.11] W. B. Lanford, T. Tanaka, Y. Otoke, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," in *Electronics Letters*, vol. 41, no. 7, pp. 449-450, 31 March 2005.

[A.12] Y. Cai, Y. Zhou, K. M. Lau and K. J. Chen, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode," *in IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2207-2215, Sep. 2006.

[A.13] S. Davis, "Enhancement mode gallium nitride MOSFET delivers impressive performance," *Power Electronics Technology*, Mar, 2010.

[A.14] X. Hu, G. Simin, J. Yang, M. Asif Khan, R. Gaska and M. S. Shur, "Enhancement mode

AlGaN/GaN HFET with selectively grown pn junction gate," *in Electronics Letters*, vol. 36, no. 8, pp. 753-754, 13 Apr 2000.

[A.15] Panasonic, "PGA26E08BV - 600V/15A GaN Power Transistor," Panasonic datasheet, available from http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/#products-document.

[A.16] GaN Systems, "GS66504B – 650V E-mode GaN transistor," GaN Systems datasheet, avai;able from http://www.gansystems.com/gs66504b.php.

[A.17] Efficient Power Conversion, "EPC2001-Enhancement-mode Power Transistor," EPC2001 datasheet, available from http://epc-co.com/epc/Products/eGaNFETsandICs/EPC2001C.aspx.

[A.18] D. Reusch, F. C. Lee, D. Gilham, and Y. Su, "Optimization of a high density gallium nitride based non-isolated point of load module," *in Proc. IEEE ECCE*, 2012, pp. 2914-2920.

[A.19] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated gallium-nitride-based point of load module design," IEEE Trans. on Power Electron., vol.28, no.9, pp.4216-4226, Sep. 2013.

[A.20] D. Reusch, D. Gilham, Y. Su, and F. C. Lee, "Gallium Nitride based 3D integrated non-isolated point of load module," in proc. IEEE APEC, 2012, pp. 38-45.

[A.21] Z. Liu, X. Huang, W. Zhang, F.C. Lee, and Q. Li, "Evaluation of high-voltage cascode GaN HEMT in different packages," in proc. IEEE APEC, 2014, pp.168-173.

[A.22] Y, Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 310-319, Mar. 2006.

[A.23] Z. Chen; Y. Yao; B. Dushan.; K. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," IEEE Trans. Power Electron., vol.29, no.5, pp.2307-2320, May. 2014.

[A.24] M. Mu, and F.C. Lee, "Comparison and optimization of high frequency inductors for critical model GaN converter operating at 1MHz," Power Electronics and Application Conference and Exposition (PEAC), vol., no., pp.1363-1368, 2014.

[A.25] D. Huang, A. Ji, and F. C. Lee, "LLC resonant converter with matrix transformer," *IEEE Trans. on Power Electron.*, vol. 29, no. 8, pp.4339-4347, Aug. 2014.

[A.26] D. Fu, F. C. Lee, and S. Wang, "Investigation on transformer design of high frequency high efficiency dc-dc converters," in proc. IEEE APEC, pp.940-947, 2010.

[A.27] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," IEEE Trans. on Power Electron., vol.22, no.4, pp.1410-1416, Jul. 2007.

[A.28] Y. Yang, M. Mu, Z. Liu, F. C. Lee, and Q. Li, "Common Mode EMI Reduction Technique for Interleaved MHz Critical Mode PFC Converter with Coupled Inductor," in Proc. IEEE

ECCE. Sep. 2015

[A.29] Y. Yang; D. Huang; F C. Lee; and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters," in proc.IEEE ECCE, 2013, pp.4149-4153.

[A.30] F. C. Lee, and Q. Li, "High-frequency integrated Point-of-Load converters: overview," IEEE Trans. on Power Electron., vol.28, no.9, pp.4127-4136, Sep. 2013.

[A.31] D. Reusch, and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," IEEE Trans. on Power Electron., vol.29, no.4, pp.2008-2015, Apr. 2014.

[A.32] Efficient Power Conversion Corporation, "Development board EPC9106 quick start guide-150W/8Ω class-D amplifier," http://epc-co.com/epc/documents/guides/EPC9106_qsg.PDF.

[A.33] L. Zhou, Y-F. Wu, and U. Mishra, "True Bridgeless Totem-pole PFC based on GaN HEMTs", PCIM Europe 2013, pp.1017-1022.

[A.34] Z. Liu, X. Huang, M. Mu, Y. Yang, F.C. Lee, and Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," in Proc. IEEE ECCE. 2014, pp.611-616.

[A.35] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," in proc. IEEE ECCE, pp.682-688, 2015.

[A.36] L. Xue, Z. Shen, D. Boroyevich, and P. Mattavelli, "GaN-based high frequency totem-pole bridgeless PFC design with digital implementation," in proc IEEE APEC, pp.759-766, 2015.

[A.37] D. Reusch, and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC–DC converters," IEEE Trans. on Power Electron., vol.30, no.9, pp.5151-5158, Sep. 2015.

[A.38] Y-F. Wu, D. Kebort, et al. "High-frequency, GaN diode-free motor drive inverter with pure sine wave output," PCIM Europe, pp. 76-83, 2012.

[A.39] C. Blake, "GaN power devices slash size, raise efficiency of 4kW solar inverter," How2power Today, exclusive technology feature.

[A.40] J. Strydom, "eGaN® FET – Silicon Power Shoot-out Volume 8: Envelope Tracking," Power Electronics Magazine.

[A.41] M. D. Rooij, Wireless Power Handbook – A Supplement to GaN Transistors for Efficiency Power Conversion, 2nd Edition, 2015.

[A.42] O. Hegazy, R. Rarrero, J. V. Mierlo, P. Lataire, N. Omar, and T. Coosemans, "An advanced power electronics interface for electric vehicles applications," *IEEE Trans. on Power Electron.*, vol. 28, no. 12, pp.5508-5521, Dec. 2013.

[A.43] M. A. Khan, A. Ahmed, I. Husain, Y. Sozer, and M. Badawy, "Performance analysis of

bidirectional DC-DC converters for electric vehicles," *IEEE Trans. on Ind. Applications*, vol. 51, no. 4, pp.3442-3452, Jul/Aug. 2015.

[A.44] H. F. Ahmed, H. Cha, S. Kim, D. Kim, and H. Kim, "Wide load range efficiency improvement of a high-power-density bidirectional DC-DC converter using an MR fluid-gap inductor," *IEEE Trans. on Ind. Applications*, vol. 51, no. 4, pp.3216-3226, Jul/Aug. 2015.

[A.45] W. Zhang, D. Dong, I. Cvetkovic, F. C. Lee, and D. Boroyevich, "Lithium-based energy storage management for DC distributed renewable energy system," *in Proc. IEEE ECCE*, 2011, pp. 3270-3277.

[A.46] J. Baek, W. Choi, and B. Cho, "Digital adaptive frequency modulation for bidirectional DC-DC converter," *IEEE Trans. on Industry Electron*., vol. 60, no. 11, pp.5167-5176, Nov. 2013.

[A.47] Y. Yang, M. Mu, Z. Liu, F. C. Lee, and Q. Li, "Common mode EMI reduction technique for interleaved MHz critical mode PFC converter with coupled inductor," in Proc. IEEE ECCE. Sep. 2015

B. Switching Characterization of GaN Devices

[B.1] Z. Liu, X. Huang, F.C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. on Power Electron.*, vol.29, no.4, pp.1977-1985, Apr. 2014.

[B.2] X. Huang; Q. Li; Z. Liu, and F.C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. on Power Electron.* vol.29, no.5, pp.2208-2219, May 2014.

[B.3] M. Mu, F. C. Lee, Q. Li, D. Gillham, and K. Ngo, "A high frequency core loss measurement method for arbitrary excitations," in proc. IEEE Applied Power Electronics Conference, 2011, pp 157-162.

[B.4] D. Reusch, "High frequency, high power density integrated point of load and bus converters," Ph.D Dissertation, Dept. of Electrical Engineering, Virginia Tech, Blacksburg, USA, 2012.

[B.5] S. Young, and W. Choi, "Switching loss estimation of high voltage power MOSFET in power factor correction pre-regulator," *in proc.IEEE Applied Power Electronics Conference*, 2011, pp 463- 467.

[B.6] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "Evaluation of SiC MOSFETs for a high efficiency three-phase Buck rectifier," *in proc.IEEE Applied Power Electronics Conference*, 2012, pp 1762-1769.

[B.7] J. Boehmer, J. Schumann, and H. Eckel, "Effect of the miller-capacitance during switching transients of IGBT and MOSFET," *in proc IEEE EPE*, pp.LS6d.3-1-LS6d.3-5, 2012.

[B.8] Z. Zhang, W. Eberle, Z. Yang, P. C. Sen, and Y. F. Liu, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 653-666, Mar. 2008.

[B.9] J. Fu, Z. Zhang, Y. Liu, and P. C. Sen, "MOSFET switching loss model and optimal design of a current source driver considering the current diversion problem," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 998-1012, Mar. 2008.

[B.10] Panasonic, "PGA26E08BV - 600V/15A GaN Power Transistor," Panasonic datasheet, available from http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/#products-document.

[B.11] Panasonic, "PGA26C09DV - 600V/15A GaN Power Transistor," Panasonic datasheet, available from http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/#products-document.

C. Switching Characterization of GaN Devices

[C.1] T. Morita et al., "99.3% Efficiency of three-phase inverter for motor drive using GaN-based Gate Injection Transistors," *in proc. IEEE APEC*, 2011, pp. 481-484.

[C.2] Y. F. Wu, "Paralleling high-speed GaN power HEMTs for quadrupled power output," *in proc. IEEE APEC,* 2013, pp. 211-214.

[C.3] H. Nakao et al., "2.5-kW power supply unit with semi-bridgeless PFC designed for GaN-HEMT," *in proc. IEEE APEC,* 2013, pp. 3232-3235.

[C.4] L. Zhou, Y. Wu, J. Honea and Z. Wang, "High-efficiency True Bridgeless Totem Pole PFC based on GaN HEMT: Design Challenges and Cost-effective Solution," PCIM Europe 2015, pp. 1-8.

[C.5] Zhehui Guo, Xiaoyong Ren, Qianhong Chen, Zhiliang Zhang and Xinbo Ruan, "Investigation of the MHz switching frequency PFC converter based on high-voltage GaN HEMT," Future Energy Electronics Conference (IFEEC), 2015 IEEE 2nd International, Taipei, 2015, pp. 1-6.

[C.6] S. Mao, R. Ramabhadran, J. Popovic and J. A. Ferreira, "Investigation of CCM boost PFC converter efficiency improvement with 600V wide band-gap power semiconductor devices," *in proc. IEEE ECCE,* 2015, pp. 388-395.

[C.7] D. Reusch, D. Gilham, Y. Su, and F. C. Lee, "Gallium Nitride based 3D integrated non-isolated point of load module," in proc. IEEE APEC, 2012, pp. 38-45.

[C.8] Infineon 2.5kW PFC, available on http://www.infineon.com/dgdl/Infineon- Presentation _ GalliumNitride _ GaNApplications_SeminarAPEC2015-AP-v01_00-EN.pdf?fileId= 5546d4624bcaebcf014c2c265e69007e

[C.9] Transphorm 1kW PFC, available on

http://www.transphormusa.com/sites/default/files/public/ Totem-Pole-PFC_TDPS500E2C1_0.pdf

[C.10] Delta Electronics 6.6kW on-board charger, available on http://energy.gov/sites/prod/files/2016 /06/f32 /edt067_zhu_2016_o_web.pdf

[C.11] W. Zhang, D. Dong, I. Cvetkovic, F. C. Lee, and D. Boroyevich, "Lithium-based energy storage management for DC distributed renewable energy system," *in Proc. IEEE ECCE*, 2011, pp. 3270-3277.

[C.12] X. Huang, F. C. Lee, Q. Li and W. Du, "High-frequency high-efficiency GaN-based interleaved CRM bidirectional buck/boost converter with inverse coupled inductor," *IEEE Trans. on Power Electron.,* vol. 31, no. 6, pp. 4343-4352, June 2016.

[C.13] M. Mu, F. C. Lee, Q. Li, D. Gillham, and K. Ngo, "A high frequency core loss measurement method for arbitrary excitations," in proc. IEEE Applied Power Electronics Conference, 2011, pp 157-162.

[C.14] NCP5181, available on http://www.onsemi.com/pub_link/Collateral/NCP5181-D.PDF

[C.15] TLA-3T106 available on http://media.digikey.com/pdf/Data%20Sheets/TDK%20PDFs/TLA, ALT_Rev.July 2012.pdf

[C.16] ACPL-38JT available on http://www.avagotech.com/docs/AV02-2546EN

[C.17] Adum1100, available on http://www.analog.com/media/en/technical-documentation/data-sheets/ADUM1100.pdf

[C.18] ISO721, available on http://www.ti.com/lit/ds/symlink/iso722.pdf

[C.19] JHM0624S15, available on http://www.xppower.com/pdfs/SF_JHM03-06.pdf

D. System design of GaN-based AC-DC adapters

[D.1] External power adapters and chargers report-2015, IHS Technology.

[D.2] Information technology equipment-safety-part 1: general requirements, International Electrotech-nical Commission.

[D.3] X. Huang, W. Du, F. C. Lee, and Q. Li, "A novel driving scheme for synchronous rectifier in MHz CRM flyback converter with GaN devices, " *in proc. IEEE ECCE*, 2015, pp 5089-5095.

[D.4] Z. Zhang, K. D. T. Ngo, and J. L. Nilles, "A 30-W flyback converter operating at 5 MHz," *in proc.IEEE APEC*, 2014, pp 1415-1421.

[D.5] T. Labella, B. York, C. Hutchens, and J. S. Lai, "Dead time optimization through loss analysis of an active-clamp flyback converter utilizing GaN devices," *in proc.IEEE ECCE*, 2012, pp 3882-3889.

[D.6] H. Jia, O. A. Rahman, K. Padmanabhan, P. Shea, I. Batarseh, and Z. J. Shen, "MHz-frequency operation of flyback converter with monolithic self-synchronized rectifier (SSR)," *in proc.IEEE INTELEC*, 2010, pp 1-6.

[D.7] C. T. Choi, C. K. Li, and S. K. Kok, "Control of an active clamp discontinuous conduction mode flyback converter," *in Proc. IEEE Power Electronics and Drive Systems Conf.*, 1999, vol. 2, pp. 1120-1123.

[D.8] Robert Watson, Fred C. Lee, and Guichao Hua, "Utilization of an Active-Clamp Circuit to achieve Soft Switching in Flyback Converters," *IEEE Trans. Power Electronics*, vol.11, pp162-169, Jan. 1996.

[D.9] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Analysis and reduction of common mode EMI noise for resonant converters," in proc. IEEE APEC, 2014, pp 566-571.

[D.10] M. Mu, F. C. Lee, "A new core loss model for rectangular AC voltages," in proc. IEEE ECCE, 2014, pp 5214-5220.

[D.11] M. Mu, F. C. Lee, Q. Li, D. Gillham, and K. Ngo, "A high frequency core loss measurement method for arbitrary excitations," in proc. IEEE Applied Power Electronics Conference, 2011, pp 157-162.

[D.12] P. L. Dowell, "Effects of eddy currents in transformer windings," *in Electrical Engineers, Proceedings of the Institution of*, vol. 113, no. 8, pp. 1387-1394, August 1966.

[D.13] L. Hyvönen, “Electrically decoupled integrated transformer having at least one grounded electric shield,” U.S. Patent US7733205 B2, 2010.

[D.14] P. Kong and F. C. Lee, “Transformer structure and its effects on common mode EMI in isolated power converters,” *in Proc. IEEE APEC*, 2010, pp. 1424–1429.

[D.15] L. Xie, X. Ruan, Q. Ji and Z. Ye, "Shielding-Cancelation Technique for Suppressing Common-Mode EMI in Isolated Power Converters," *in IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2814-2822, May 2015.

[D.16] D. Zhang; D. Chen; D. Sable, "Non-intrinsic differential mode noise caused by ground current in an off-line power supply," *in IEEE PESC*, 1998, pp.1131-1133

[D.17] S. Qu; D. Chen, "Mixed-mode EMI noise and its implications to filter design in offline switching power supplies," *IEEE Trans. on , Power Electron.*, vol.17, no.4, pp.502-507, Jul. 2002

[D.18] J. Meng, W. Ma, "A new technique for modeling and analysis of mixed-mode conducted EMI noise," *IEEE Trans. on Power Electron.*, vol. 19, no. 6, pp.1679-1687, Nov. 2004.

[D.19] H. Hsieh; J. Li; D. Chen, "Effects of X Capacitors on EMI Filter Effectiveness," *IEEE Trans on Ind. Electron.*, vol.55, no.2, pp.949-955, Feb. 2008.

[D.20] Comchip SMD Diode Specialist, "Low VF SMD Bridge Rectifiers" Z4DGP4046L-HF datasheet.

[D.21] Z. Liu, F. C. Lee, Q. Li and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799-807, Sept. 2016.

[D.22] D. Huang, A. Ji, and F. C. Lee, "LLC resonant converter with matrix transformer," IEEE Trans. on Power Electron., vol. 29, no. 8, pp.4339-4347, Aug. 2014.

[D.23] L. Gu, X. Ruan, M. Xu, and K. Yao, “Means of eliminating electrolytic capacitor in AC/DC power sup-plies for LED lighting,” *IEEE Trans. on Power Electron.,* vol. 24, no. 5, pp. 1399-1408, May 2009.

[D.24] Z. Liu, Z. Huang, F. C. Lee and Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 808-814, Sept. 2016.

[D.25] J. Zhang, X. Huang, X. Wu, and Z. Qian, "A high efficiency flyback covnerter with new active clamp technique," *IEEE Trans. Power Electronics*, vol.25, No. 7, pp1775-1785, Jul. 2010.

[D.26] P. L. Dowell, "Effects of eddy currents in transformer windings," *Electrical Engineers, Proceedings of the Institution of*, vol.113, no.8, pp.1387-1394, Aug. 1966.

E. Appendix A

[E.1] L. Spaziani, "A study of MOSFET performance in processor targeted buck and synchronous rectifier buck converters," in proc. High frequency Power Conversion, 1996, pp. 123-137.

[E.2] Y, Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 310-319, Mar. 2006.

[E.3] M. Rodriguez, A. Rodriguez, P. F. Miaja, D. G. Lamar, and J. S. Zuniga, "An insight into the switching process of power MOSFETs: an improved analytical losses model," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1626-1640, Jun. 2010.

[E.4] Z. Zhang, W. Eberle, Z. Yang, P. C. Sen, and Y. F. Liu, "Optimal design of resonant gate driver for buck converter based on a new analytical loss model," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 653-666, Mar. 2008.

[E.5] J. Fu, Z. Zhang, Y. Liu, and P. C. Sen, "MOSFET switching loss model and optimal design of a current source driver considering the current diversion problem," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 998-1012, Mar. 2008.

[E.6] J. B. Witcher, "Methodology for switching characterization of power devices and

modules," M.S. thesis, Dept. Electrical Eng., Virginia Tech., Blacksburg, USA, 2002.

[E.7] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," M.S. thesis, Dept. Electrical Eng., Virginia Tech., Blacksburg, USA, 2009.

[E.8] S. Young, and W. Choi, "Switching loss estimation of high voltage power MOSFET in power factor correction pre-regulator," in proc.IEEE Applied Power Electronics Conference, 2011, pp 463- 467.

[E.9] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "Evaluation of SiC MOSFETs for a high efficiency three-phase Buck rectifier," in proc.IEEE Applied Power Electronics Conference, 2012, pp 1762-1769.

[E.10] O. Mostaghimi, N. Wright, and A. Horsfall. "Design and performance evaluation of SiC based DC-DC converter for PV applications," in proc.IEEE Energy Conversion Congress and Exposition, 2012, pp 3956-3963.

[E.11] Silicon carbide enhancement-mode junction field effect transistor and recommendation for use. Application note, available: www.SemiSouth.com

[E.12] A. Lidow, J. Strydom, M. D. Rooij, and Y. Ma, GaN Transistors for Efficient Power Conversion. Power Conversion Publications, 2011, ch. 1.

[E.13] B. J. Baliga, and M. S. Adler, "Composite Circuit for Power Semiconductor Switching," European Patent EP 0063749 B1, 1982.

[E.14] M. Mu, F. C. Lee, Q. Li, D. Gillham, and K. Ngo, "A high frequency core loss measurement method for arbitrary excitations," in proc. IEEE Applied Power Electronics Conference, 2011, pp 157-162.

F. Appendix B

[F.1] O. Hegazy, R. Rarrero, J. V. Mierlo, P. Lataire, N. Omar, and T. Coosemans, "An advanced power electronics interface for electric vehicles applications," IEEE Trans. on Power Electron., vol. 28, no. 12, pp.5508-5521, Dec. 2013.

[F.2] M. A. Khan, A. Ahmed, I. Husain, Y. Sozer, and M. Badawy, "Performance analysis of bidirectional DC-DC converters for electric vehicles," IEEE Trans. on Ind. Applications, vol. 51, no. 4, pp.3442-3452, Jul/Aug. 2015.

[F.3] H. F. Ahmed, H. Cha, S. Kim, D. Kim, and H. Kim, "Wide load range efficiency improvement of a high-power-density bidirectional DC-DC converter using an MR fluid-gap inductor," IEEE Trans. on Ind. Applications, vol. 51, no. 4, pp.3216-3226, Jul/Aug. 2015.

[F.4] W. Zhang, D. Dong, I. Cvetkovic, F. C. Lee, and D. Boroyevich, "Lithium-based energy storage management for DC distributed renewable energy system," in Proc. IEEE Energy Conversion Congress & Expo., 2011, pp. 3270-3277.

[F.5] J. Baek, W. Choi, and B. Cho, "Digital adaptive frequency modulation for bidirectional DC-DC converter," IEEE Trans. on Industry Electron., vol. 60, no. 11, pp.5167-5176, Nov. 2013.

[F.6] Z. Liu, X. Huang, M. Mu, Y. Yang, F. C. Lee, and Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," *in proc. IEEE ECCE*, 2014, pp 611-616.

[F.7] X. Huang, Z. Liu, F. C. Lee, and Q. Li, "Characterization and enhancement of high-voltage cascode GaN devices," *IEEE Trans. on Electron Devices.*, vol. 62, no. 2, pp.270-277, Feb. 2015.

[F.8] X. Huang, Z. Liu, Q. Li, and F C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. on Power Electron*., vol. 29, no. 5, pp.2453-2461, May. 2014.

[F.9] P. Wong, Q. Wu, P. Xu, Y. Bo, and F. C. Lee, "Investigating coupling inductors in the interleaving QSW VRM," *in proc. IEEE APEC*, 2000, pp 973-978.

[F.10] F. Wang, X. Ruan, Y. Yang, and Z. Ye, "Interleaved critical current mode boost PFC converter with coupled inductor," *IEEE Trans. Power Electron*., vol. 26, no. 9, pp. 2404-2413, Sep 2011.

[F.11] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 183-191, Apr 1988.

[F.12] G. Hua, and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Trans. Ind. Electron.,* vol. 42, no. 6, pp. 595-603, Dec 1995.