SMALL-SIGNAL ANALYSIS OF PARALLEL POWER CONVERTERS

by

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(ABSTRACT)

A small-signal analysis and modelling approach is developed for parallel power converter modules. The small-signal model of parallel buck converter modules is developed in detail to demonstrate the modelling approach. It is shown that a multiple power converter module system can be reduced to an equivalent single-module system to facilitate system analysis and design.

Different forms of current-mode control and their applications to single and multiple modules are discussed. Detailed procedures are then developed for the design of a current-mode control circuit for single or multiple power converter modules. The applications of the design procedures and the analysis results are demonstrated for several converter design examples.

The use of a secondary output filter on the output of power converters is discussed. The effect of this filter and its interaction with the stability and closed-loop performance of the converter are analyzed in detail.

ACKNOWLEDGEMENTS

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Chapter 1

Introduction

In recent years, rapid advances in the field of computer hardware have led to increased requirements of the computer power systems. Packaging densities and integrated circuit speeds have increased dramatically, with corresponding reductions in voltage level and increases in power. Specifications for power supply outputs in the range of 1-2 volts at several thousand amperes, with less than 5mV of switching ripple and noise, will soon be required for large computer systems.

With these increases in speed and density, many more users have become increasingly dependent upon computers, and frequent system down-time due to hardware failures are no longer acceptable. Since high current, off-line switching converters operate with their switching devices at high stress levels, they are frequently the cause of system failures. Even with conservative designs, power supply failures are aggravated by power-line anomalies and, with no backup power system available, will cause the system to crash. With the increased demands on high power levels, and the need for high reliability the use of a single power module to supply the needs of a large computer system is becoming quite impractical. The high stress levels on the semiconductor devices cannot be reduced without compromising the power density of the supply; so, it is desirable to design a power system with some redundancy to allow continued power output with limited device failure.

Fortunately, recent advances in switch-mode power supply control technology have made this possible. The use of current-mode control allows

a single power supply module to be replaced with several power modules, each supplying an equal amount of the load current. With the addition of extra modules, the peak stress within each may be reduced and some redundancy may be built into the system. This scheme provides numerous advantages:

- If a semiconductor device fails in one of the power modules, the remaining modules may provide the required additional power and the failed module may be replaced without loss of output.

- Each individual module can be built at a sufficiently low power level, therefore paralleling devices within the module is unnecessary.

- By arranging the switching sequence of the modules appropriately, the input and output ripple current can be dramatically reduced. This is essential for low noise requirements, and the use of this scheme will allow a smaller output filter with faster transient response.

- A single power module design may be used for many different applications, the power level of each application determining the number of modules to be used in parallel.

These features and the dc characteristics of parallel power modules are generally well understood. However, the small-signal characteristics of such a system have not yet been investigated, and stability and closed-loop performance characteristics are not well understood. This

lack of analysis and understanding of how to design the feedback loop of such parallel module systems have restricted their use.

The main purpose of this thesis is to characterize the small-signal performance of parallel power converter modules. In Chapter 2, the small-signal transfer functions for the block diagram representation of the parallel power module system are derived for an arbitrary number of power modules. The loop gains which may be defined for a parallel power module system are derived from the transfer functions in Chapter 3. Chapter 4 discusses the different types of current-mode control available for parallel modules. The advantages and disadvantages of these schemes are discussed and control methods for applications are suggested.

Early work on current-mode control developed specific design guidelines for the design of the power converter control loop. These procedures allowed the control to be designed in a non-iterative manner to satisfy all small-signal design specifications concurrently. Chapters 5 and 6 extend these design procedures to allow the use of similar procedures for different current-mode control schemes and for the design of control loops for multiple parallel modules.

Since the use of parallel power modules is often required for very low output noise, the use of a secondary output filter on the power supply output is considered in detail in Chapter 7. Design guidelines are given to allow the use of a secondary LC filter to give maximum noise attenuation without sacrificing stability or output impedance characteristics. This analysis is applicable to single or multiple modules.

To illustrate the concepts developed in earlier sections, Chapter 8 contains design examples for different power stage configurations showing how the control loop may be designed for specified performance criteria.

An example of a secondary output filter design is also given. Conclusions are presented in Chapter 9.

Chapter 2

Small-Signal Model for Parallel Power Modules

In this chapter, the small-signal model for k parallel buck power modules is developed. It can be seen from Figure 2.3 that, neglecting second-order effects, this is a k+1 order system with a single output capacitor common to each of the power modules. The only assumption made about the power stages is that each module has an identical inductor with the same equivalent series resistance. The analysis does not depend on the input voltages or the duty cycles of each module being equal. Such a generalization is possible for the buck converter due to the invariant A matrix under all switching conditions.

For the boost and buck/boost converters, the analysis only yields manageable results if the modules are restricted to common inputs due to the variable A matrix. This analysis is not included here.

The ultimate goal of the small-signal analysis is the reduction of the complexity of the generalized k+1 order system to a smaller equivalent system for which design and analysis steps may be developed.

2.1 Effect of Switching Sequencing on Small-Signal Performance

When using a power stage constructed of parallel modules, the design freedom exists to switch the power modules with different timing permutations. The power switches may be operated synchronously and all turned on at the same time, or synchronously but out of step with each other. Alternatively, they may be operated asynchronously. The effect of the mode

of operation on large-signal performance, especially the output and input ripple, can be quite dramatic. In some cases, the timing may be arranged so that the inductor ripple currents cancel at the output, allowing for a much smaller output capacitor and a faster transient response. Similar improvements can be made for the input ripple current.

The purpose of this section is to demonstrate the effect of the power stage switching sequence on the small-signal characteristics of the power supply. If the small-signal characteristics are shown to be unaffected by the switching sequence, the sequence may be arranged to produce the optimum large-signal characteristics.

Figure 2.1 shows the circuit diagram for two parallel power modules. When both switches are closed, it can easily be shown that the state equations for the system are given by:

$$\dot{x} = Ax + b_1 v_{g1} + b_2 v_{g2}$$

where

$$A = \begin{bmatrix} -R_e/L & -R_c/L & -1/L \\ -R_c/L & -R_e/L & -1/L \\ 1/C & 1/C & 1/CR_L \end{bmatrix} \quad b_1 = \begin{bmatrix} 1/L \\ 0 \\ 0 \end{bmatrix} \quad b_2 = \begin{bmatrix} 0 \\ 1/L \\ 0 \end{bmatrix}$$

$R_e = R_c + R_1$ and R_c, $R_1 \ll R_L$.

During the time when only switch 1 is closed, the state equations are:

$$\dot{x} = Ax + b_1 v_{g1}$$

and when only switch 2 is closed,

$$\dot{x} = Ax + b_2 v_{g2}$$

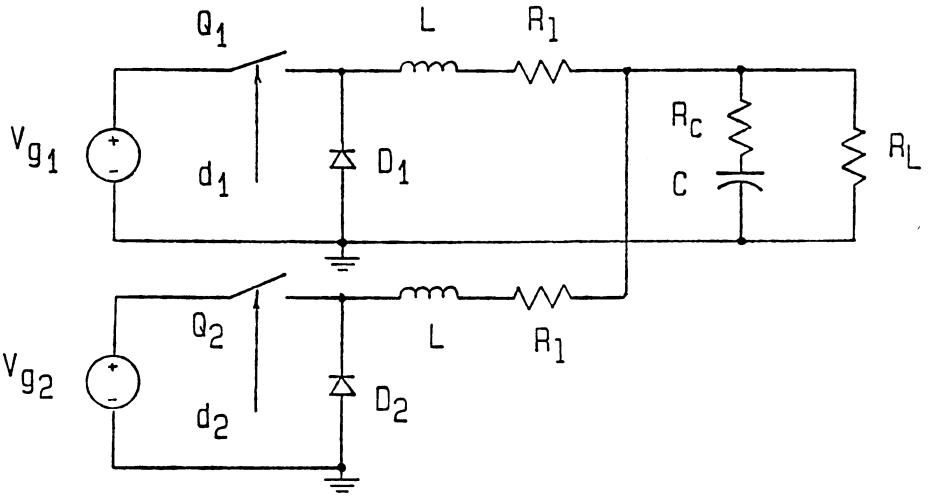


Figure 2.1: Circuit Diagram for Two Parallel Buck Converter Modules.

Figure 2.2 shows two possible switching sequences of the two parallel power stages. In the first diagram, the switching is synchronized, and the two power switches are closed at the same time by a common clock. In the second diagram, the power stages are controlled by a common clock, but the turn-on of the switch is delayed by a fixed time for one of the power stages. Although these diagrams show a specific sequence, they may be assumed to be general since any of the time intervals may have a negative value.

In the first diagram, the duty cycle of the first converter is $d_1 = (t_1 + t_2)/t_s$, where t_s is the period of the switching frequency. The duty cycle of the second power stage is $d_2 = t_1/t_s$. The state equations for the different time intervals are:

$$\dot{x} = Ax + b_1 v_{g1} + b_2 v_{g2} \qquad t < t_1$$

$$\dot{x} = Ax + b_1 v_{g1} \qquad t_1 < t < t_1 + t_2$$

$$\dot{x} = Ax \qquad t_1 + t_2 < t < t_s$$

We can now carry out the step of state-space averaging which gives the result:

$$\dot{x} = Ax + t_1/t_s(b_1 v_{g1} + b_2 v_{g2}) + t_2/t_s(b_1 v_{g1})$$

$$= Ax + d_1 b_1 v_{g1} + d_2 b_2 v_{g2}$$

Consider the second diagram. In this case, the duty cycle of the first power stage is $d_1 = (t_1 + t_2)/t_s$, and the duty cycle of the second power stage is $d_2 = (t_2 + t_1)/t_s$. For this case, the state equations for the different time intervals are:

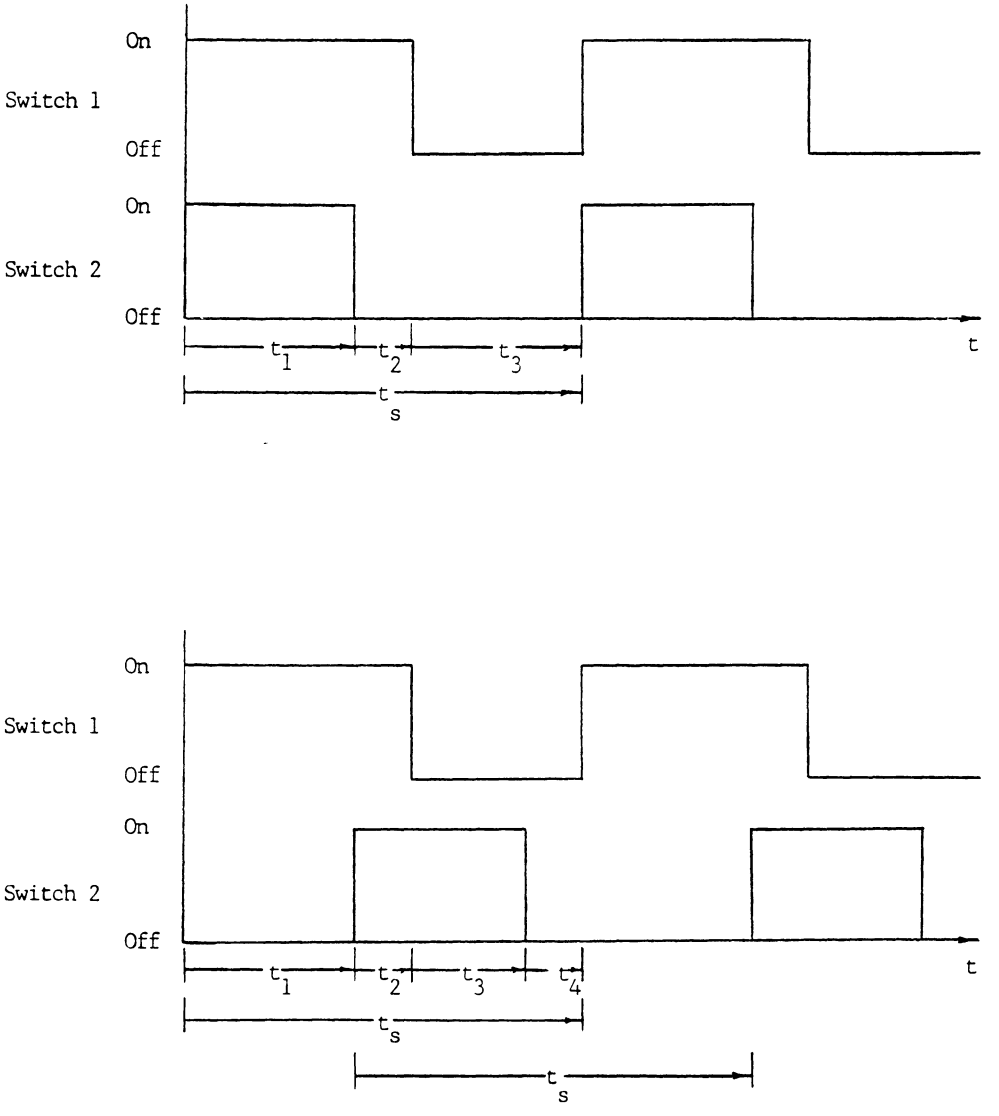


Figure 2.2: Possible Synchronized Switching Sequences for Two Parallel Buck Converter Modules.

$$\dot{x} = Ax + b_1 v_{g1} \qquad t < t_1$$

$$\dot{x} = Ax + b_1 v_{g1} + b_2 v_{g2} \qquad t_1 < t < t_1 + t_2$$

$$\dot{x} = Ax + b_2 v_{g2} \qquad t_1 + t_2 < t < t_1 + t_2 + t_1$$

$$\dot{x} = Ax \qquad t_1 + t_2 + t_1 < t < t_s$$

Averaging these equations:

$$\dot{x} = Ax + t_1/t_s(b_1 v_{g1}) + t_2/t_s(b_1 v_{g1} + b_2 v_{g2}) + t_1/t_s(b_2 v_{g2})$$
$$= Ax + d_1 b_1 v_{g1} + d_2 b_2 v_{g2}$$

Notice that this result is identical to the case of synchronized switching. The small-signal behavior of the system is, therefore, independent of the switching sequence of the power stages. If the power stages are driven by separate clocks, the small-signal behavior is also unaffected if the frequencies of the clocks are approximately equal. This mode of operation is undesirable from a large-signal point of view since the asynchronous clocks will cause a beating of the output ripple amplitude as they switch in and out of phase with each other.

For the buck converter, this desirable result is obtained because the plant matrix for the on and off times is the same. For the boost and buck-boost converters, the sequence of switching does have a small effect on the damping of the output filter.

2.2 Small-Signal Transfer Function Analysis

The circuit diagram for k parallel buck converters is shown in Figure 2.3, where the circuit parameter variables are defined for the analysis below.

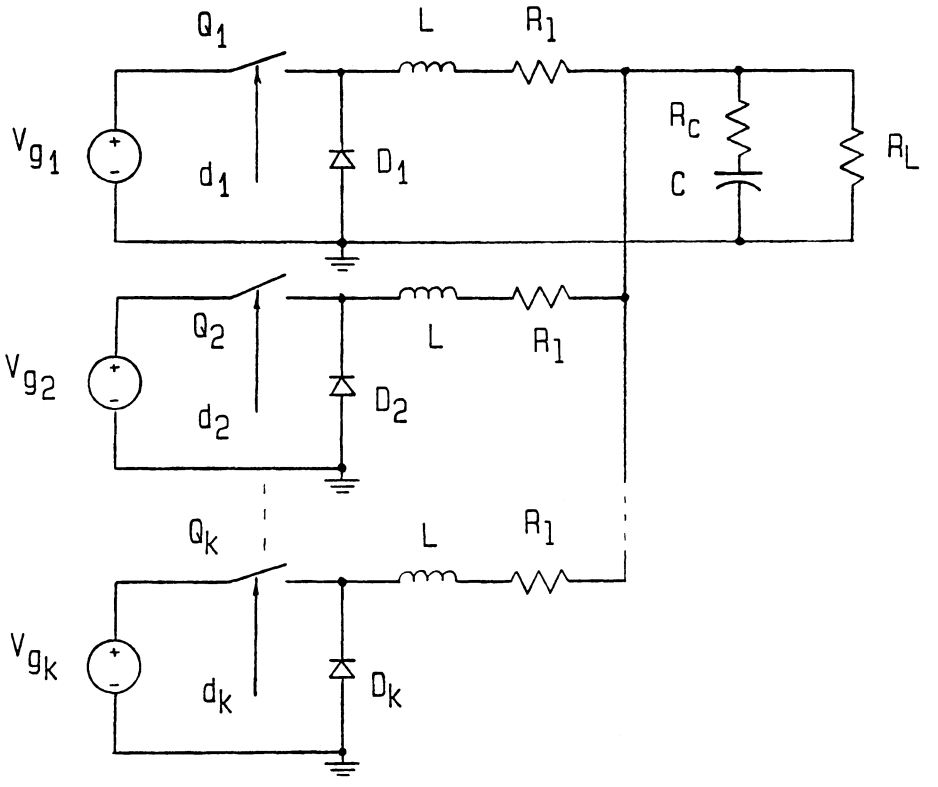


Figure 2.3: Circuit Diagram for k Parallel Buck Converter Modules.

For k parallel buck converter power stages, it can easily be shown that the small-signal state equation, after averaging, perturbation and linearization is:

$$\begin{aligned} \dot{x} &= Ax + b_{v1}v_{g1} + \ldots + b_{vk}v_{gk} + b_1 d_1 + \ldots + b_k d_k \\ v_o &= Cx \end{aligned} \qquad (2.1)$$

where

$$x = [\, i_{11} \quad i_{12} \quad i_{13} \ldots i_{1k} \quad v_c \,]^t$$

$$A = \begin{bmatrix} -R_e/L & -R_c/L & -R_c/L \ldots -R_c/L & -1/L \\ -R_c/L & -R_e/L & -R_c/L \ldots -R_c/L & -1/L \\ -R_c/L & -R_c/L & -R_e/L \ldots -R_c/L & -1/L \\ \vdots & \vdots & \vdots \quad \vdots & \vdots \\ -R_c/L & -R_c/L & -R_c/L \ldots -R_e/L & -1/L \\ 1/C & 1/C & 1/C \ldots 1/C & 1/CR_L \end{bmatrix} (k+1 \times k+1)$$

$$b_{vi} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ D_i/L \\ 0 \\ \vdots \\ 0 \end{bmatrix} \longleftarrow \text{row } i \longrightarrow \quad b_i = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ V_{gi}/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} R_c & R_c \ldots R_c & 1 \end{bmatrix}$$

The corresponding small-signal block diagram for k parallel buck converters is shown in Figure 2.4. Each of the gain blocks, F_1 - F_6, are defined as the following transfer functions:

F_1 = Input-to-Output Transfer Function = v_o/v_{gi}

F_2 = Duty-Cycle-to-Output Transfer Function = v_o/d_i

F_3 = Input-to-Inductor-Current Transfer Function = i_{li}/v_{gi}

F_4 = Duty-Cycle-to-Inductor-Current Transfer Function = i_{li}/d_i

F_5 = Duty-Cycle-to-Inductor-Current Transfer Function = i_{li}/d_j

F_6 = Input-to-Inductor-Current-Transfer Function = i_{li}/v_{gk}

Transfer function blocks F_i and F_v represent the current and voltage compensations, respectively. F_m is the gain of the pulse modulator. Each of these design blocks will be discussed in detail later.

The transfer functions may be evaluated by the Laplace transformation and rearrangement of Equation 2.1. The derivation of transfer functions F_1 - F_6 is presented in Appendix A. The results of the analysis are as follows:

$$F_1 = v_o/v_{gi} = \frac{D_i}{L} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left(\frac{R_e'}{L} + \frac{1}{CR_L}\right) + \frac{k}{LC}\right)} \qquad (2.2)$$

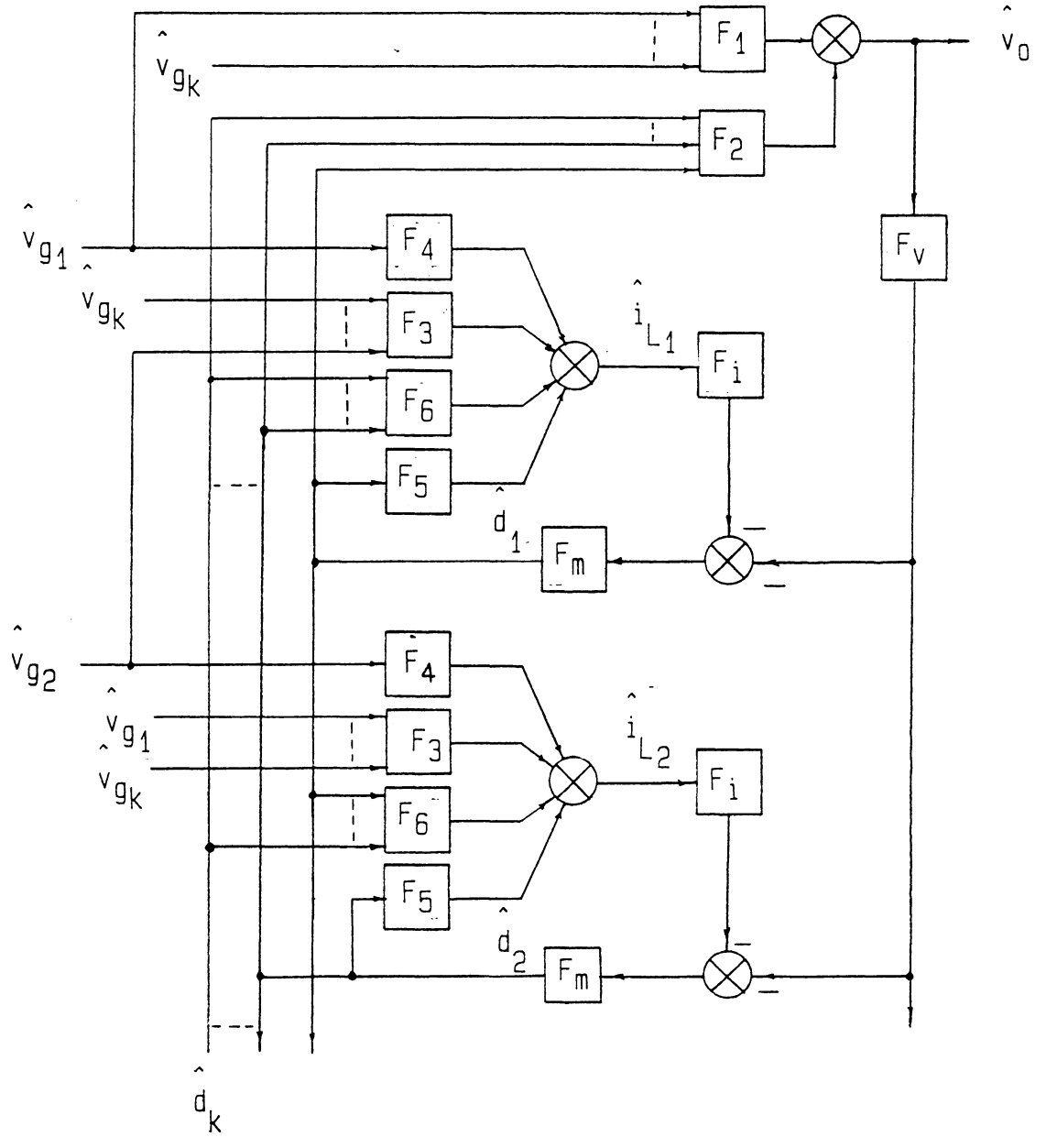


Figure 2.4: Small-Signal Block Diagram for k Parallel Buck Converter Modules.

$$F_2 = v_o/d_i = \frac{V_{gi}}{L} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)} \tag{2.3}$$

$$F_3 = i_{li}/v_{gi} = \frac{D_i}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{(k-1)}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)} \tag{2.4}$$

$$F_4 = i_{li}/d_i = \frac{V_{gi}}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{(k-1)}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)} \tag{2.5}$$

$$F_5 = i_{li}/d_k = \frac{-V_{gk}}{L} \frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)} \tag{2.6}$$

$$F_6 = i_{li}/v_{gk} = \frac{-D_k}{L} \frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)} \tag{2.7}$$

where $R_e' = R_1 + kR_c$ and $R_e'' = R_1 + (k-1)R_c$

2.3 Conclusions

In this chapter, it has been shown that the switching sequence of the buck converter modules has no effect on the small-signal model obtained using state-space averaging analysis techniques. Also, the power stage transfer functions have been derived for k parallel buck modules. In deriving these transfer functions, no assumptions have been made about the type of control used or that the input voltages have any relationship to each other. The only assumption made concerning the power stages is that the inductors of each power stage are equal, with equal equivalent series resistance. It is interesting to note that for the k+1 order system, none of the derived transfer functions is greater than third order. It is shown later for the special case where the power modules operate from the same source, that the system can be reduced to a second-order case with the appropriate control scheme.

Chapter 3

Loop Gain of Multi-Loop-Controlled Parallel Power Modules

To evaluate the small-signal characteristics of the parallel power modules, the open-loop gain of the system must be examined. Closed-loop characteristics of the output impedance and the audiosusceptibility as well as the system stability are dependent upon the open-loop gain.

In this chapter, various loop gains of the multi-loop controlled parallel module system are examined and compared to the corresponding loop gains of a single module. The loop gains of multi-module and single-module systems are related. The well-understood design tools for single module power supplies can, therefore, be used with modifications for the multiple modules.

3.1 Loop Gain of a Single Power Module with Multi-Loop Control

Before analyzing the loop gains of parallel modules, the loop gains of a single-module, multi-loop controlled converter are considered. The transfer-function block diagram for the single-module buck converter is shown in Figure 3.1. There are three possible choices for measurement of loop gain, denoted by a, b and c on the block diagram. The third choice, c, is not a practical one, since for the present known methods of implementing current-mode control, the loop gain cannot be measured at this point.

The first choice of loop gain, T_1, measured at point a can be expressed as:

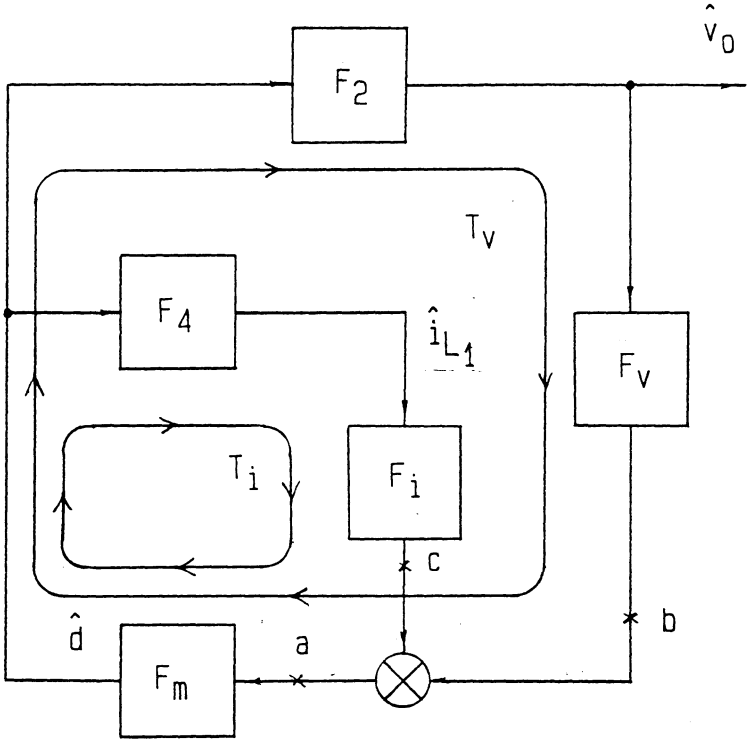


Figure 3.1: Small-Signal Block Diagram for Single Buck Converter Module.

$$T_1 = T_v + T_i \tag{3.1}$$

where

$$T_v = F_m F_2 F_v$$

$$T_i = F_m F_i F_4$$

It can be seen that the expression for the loop gain at this point is composed of two factors; the first is due to the voltage-compensation loop, T_v, and the second is due to the current-compensation loop, T_i.

A second loop gain, T_2, can be measured at point b. In this case, the loop gain can be expressed as:

$$T_2 = \frac{T_v}{1 + T_i} \tag{3.2}$$

Again, this loop gain is composed of the same two factors, T_v and T_i, merely arranged in a different form.

Instead of considering either of the loop gains T_1 or T_2 as a basis for comparison of the multiple-module and single-module systems, the components of these loops, T_i and T_v, are compared. The closed-loop characteristics of the system may also be expressed by these loop-gain components. This is discussed in more detail in Chapter 4 where the properties of the current loop are considered. Further discussions of loop gains T_1 and T_2 are given in References [2]-[4].

In order to compare the systems with multiple modules and a single module, components T_i and T_v are analyzed. If the relationship between these loop gains for parallel modules and a single module can be derived, then the system can be properly characterized and designed.

3.2 Loop Analysis of Multiple Converters

In the following analysis, the voltage-loop gain, T_v, of the multiple modules is derived and compared to that of a single module. Also, a loop gain analogous to that of the current-loop gain, T_i, is derived for the multiple modules and compared to that of the single module.

The small-signal block diagram for k parallel buck power modules is shown in Figure 3.2. For the derivation of loop gains, the input voltage perturbation is assumed to be zero; so, gain blocks F_1, F_3 and F_6, shown in Figure 2.4, do not affect the loop gain and are not included here.

For most practical applications of parallel modules, each of the modules operate from equal dc bus voltages, whether it is derived from a common dc input bus or a common ac line rectified to form individual busses. The analysis, therefore, assumes a common input voltage for each module. If the modules operate from dc busses of different values, it can be shown that the resulting system can be made equivalent that with equal input voltages if the difference is known to be constant. This is discussed in Appendix B.

For the case of k parallel converters with unequal input voltages, the analysis of the loop gains becomes intractable and offers no insight to the problem. A system with two modules operating from unequal input

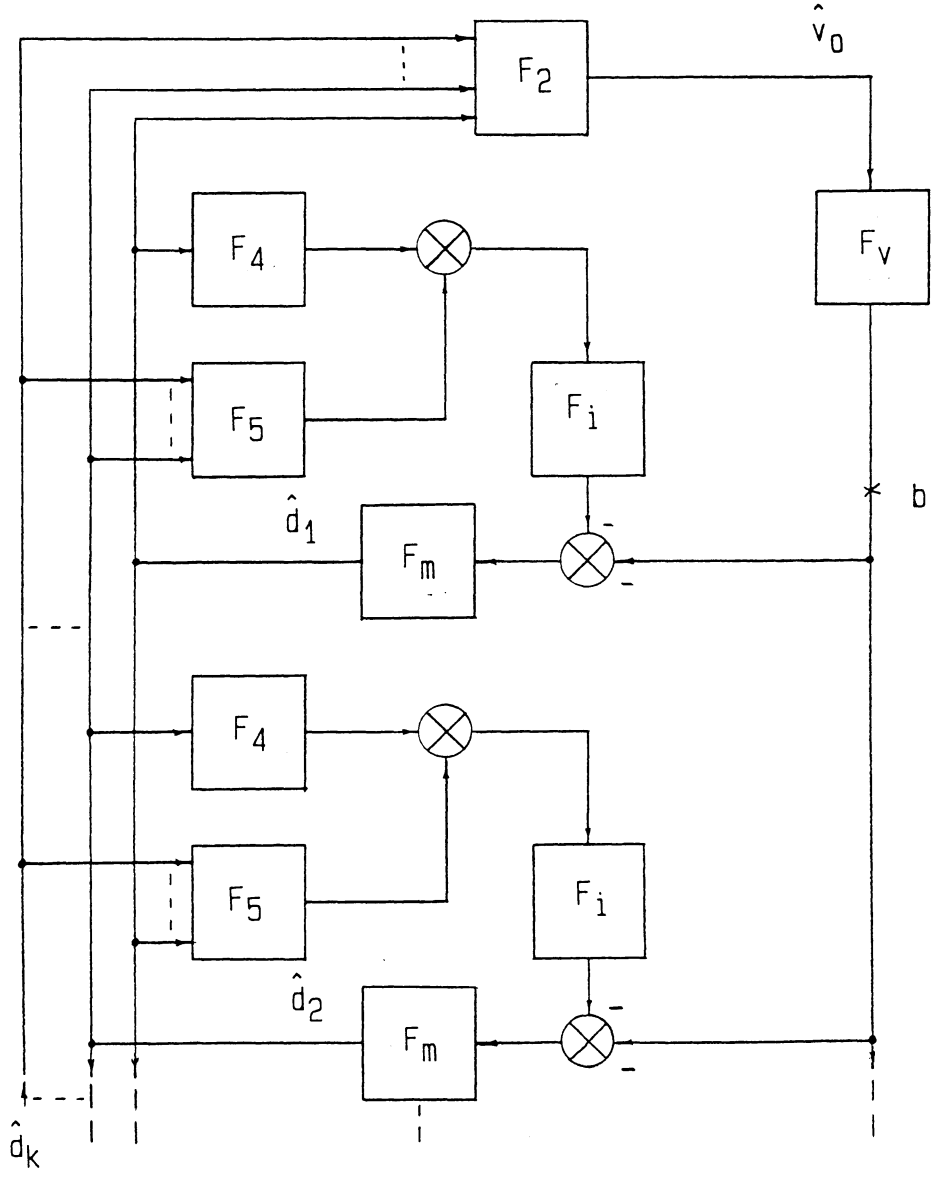


Figure 3.2: Small-Signal Block Diagram for Loop Gain Determination of k Parallel Buck Converter Modules.

In Figure 3.2, a loop gain measured at point b is analogous to that measured at point b in Figure 3.1 for the single module. It is apparent that a point analogous to point a in Figure 3.1 cannot be defined for the parallel module block diagram. (Similarly, loop gain T_1 cannot be identified and measured directly for parallel modules.) Also, when the outer voltage loop is opened, the current-loop gain, T_i, cannot be readily identified.

In analyzing the loop gain at point b for the multiple module case, an expression may be obtained of the form:

$$T_2 = \frac{T_v'}{1 + F(s)} \tag{3.3}$$

Comparison of Equations 3.2 and 3.3 allows the definition of an 'equivalent' current-loop gain for the parallel modules ($T_i = F(s)$), and this may be compared to that of the single module. Also, the voltage-loop gain, T_v', for the parallel modules can be compared to that of the single module, T_v.

The analysis of k parallel converters for the loop gain at b is presented in Appendix B. The resulting loop gain is:

$$T_2 = \frac{kF_m F_2 F_v}{1 + F_m F_i [F_4 + (k-1)F_5]} \tag{3.4}$$

Recognizing that the numerator contains gain blocks found in the voltage loop expression of a single converter, the voltage loop gain, T_v, of the parallel modules is then:

$$T_v = kF_2 F_v F_m$$

The equivalent current-loop gain for the parallel modules is:

$$T_i = F_m F_i [F_4 + (k-1)F_5]$$

Substituting the expressions for the transfer-function blocks, it is shown in Appendix B that the voltage-loop gain can be written as:

$$T_v = F_m F_v \frac{V_g}{L'} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)} \tag{3.5}$$

where $L' = L/k$ and $R_{11} = R_1/k$

It is also shown that the equivalent current-loop gain for the parallel converter modules is approximated by:

$$T_i = F_m F_i \frac{V_g}{kL'} \frac{\left(s + \frac{1}{CR_L}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)} \tag{3.6}$$

It can be seen from equation 3.5 that the voltage loop gain for k converters is the same as that for a single module with inductance $L' = L/k$ and $R_{11} = R_1/k$ (i.e. the values obtained by paralleling the inductors) with the exception of the leading gain term, $F_m F_v$. (Since the value of the modulator gain F_m depends upon the value of the inductance for the current-mode control, it will be different when evaluated for a single inductor or parallel inductances.) The analysis of F_m is presented in detail in Chapter 4 when different control schemes are considered.

From the expression for the current-loop gain in Equation 3.6, it can be seen that the expression is the same as that for a single module with a parallel inductance value with the exception of the leading term, $F_m F_i/k$.

It is apparent that the system with parallel modules can be reduced to an equivalent system with a single module if appropriate adjustments in the gains of F_m, F_i and F_v are made. The procedure for this is presented in Chapter 4.

3.3 Analysis of Two Converters with Different Input Voltages

In the second section of Appendix B, the analysis of the loop gain at point b is presented for the case where two converter modules have different input voltages. The different input voltages affects the gain blocks F_2, F_4 and F_5, as shown in Figure 3.3, multiplying each by m. Manipulation of the block diagram allows this gain to be shifted to gain block F_m for the second modulator. The overall effect of the input voltage may then be considered to be equivalent to a change in the gain of the modulator gain block F_m only. This allows the possibility of nullifying the effect of different input voltages by adjusting the gain of the modulator blocks with the addition of suitable external ramps.

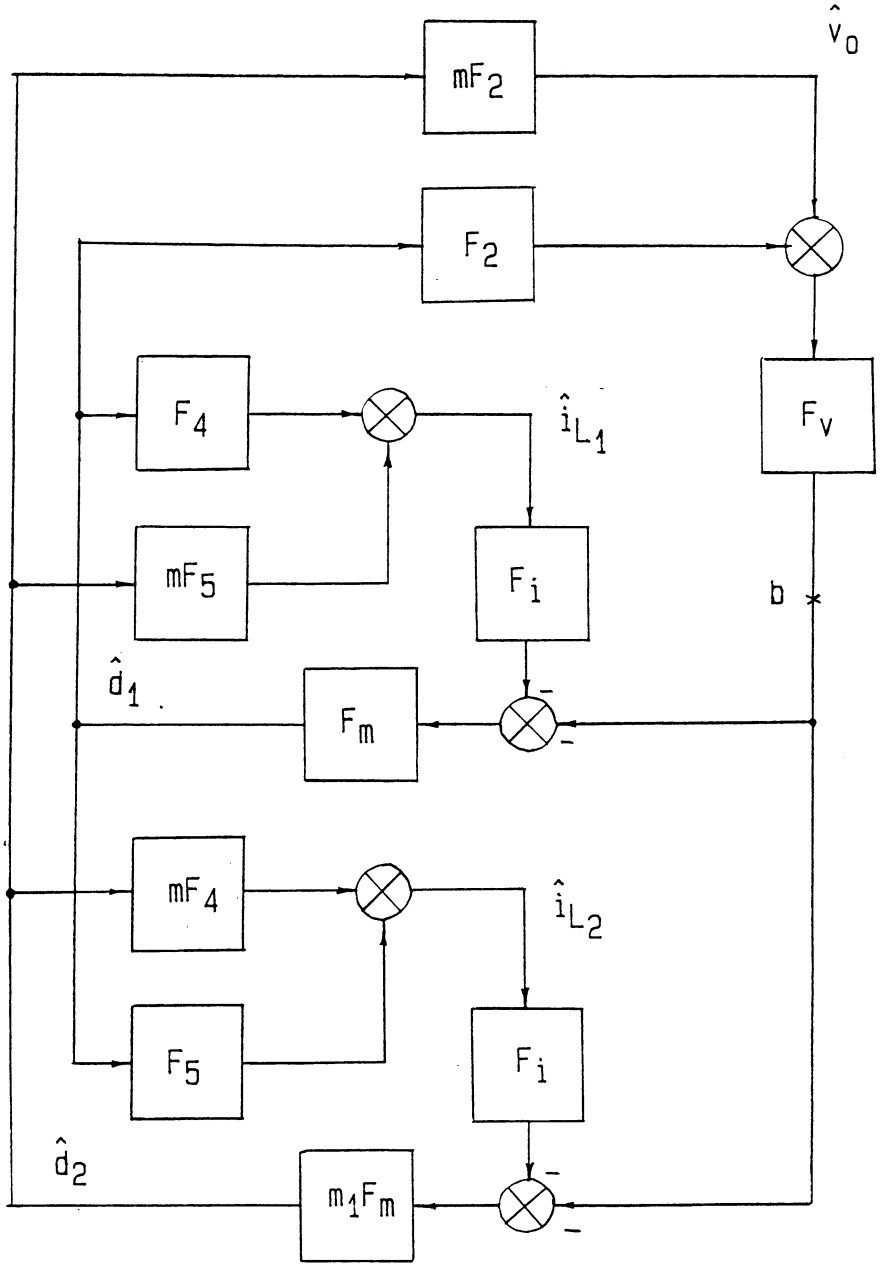


Figure 3.3: Small-Signal Block Diagram for Loop Gain Determination of Two Parallel Buck Converter Modules with Different Input Voltages.

In certain applications, the disparity in input voltages may not be known or the addition of external ramps may be an unwanted complication to the circuit. It is shown in Appendix B that the high frequency behavior of the current-loop gain is only changed by a small amount for large differences in the input voltage sources when the gains of the modulators are not adjusted. The purpose of the analysis of two different converters is to show that, for reasonable differences in input voltage, the effect will be insignificant especially when the control system is properly designed for the current loop to be dominant at high frequency. It is shown that even for a large disparity in input voltages, the equivalent current gain for the two converter modules has an additional pole-zero pair added. Since the zero occurs at a frequency before that of the pole, there are no detrimental effects due to the disparity in input voltages.

3.4 Conclusions

For the parallel buck converter modules with equal input voltages, the current- and voltage-loop gains are identical to those of a single module with an inductance value equal to 1/k times the inductance of each individual module, with the exception of the pulse-modulator gain, and the current-compensation gain. If these gains are properly adjusted, the problem of designing the control for the multiple modules can be reduced to that of designing for a single module.

For parallel converters with unequal input voltages, stability and other performance characteristics will not change significantly when the control loops are properly designed with the voltage loop dominating at

low frequencies and the current loop dominating at high frequencies. In following the control circuit design procedures given in Chapter 5, deviations in the input voltages will not cause any serious problems.

Chapter 4

Current-Mode Control of Multiple Power Modules

For the use of multiple parallel modules to be successful, some form of current-mode control must be used to ensure the modules share the current equally. Current-mode control has two important properties which allow for enhanced regulator performance: firstly, it provides the desired sharing of current and inherent peak current protection. This purpose is well-understood and implemented by most designers. The second feature is a high-bandwidth second feedback loop which allows for enhanced small-signal performance and improved system stability. This is especially important for systems with right-hand-plane zeros (boost and buck-boost) or when using a second LC filter on the output of a power supply.

In this chapter, the small-signal aspects of two forms of current-mode control are considered. It is shown that the desirable small-signal characteristics can be lost when applying current-injection control to a practical buck regulator circuit leading to instability. A control scheme is proposed to overcome these problems while retaining the current sharing property of the control.

4.1 Current-Injection Control

The basic approach of current-mode control is to sense the inductor current state and compare this to an error voltage to regulate the duty cycle of the power switch. For an ideal switched-mode converter, the

inductor current is equal to (or proportional to, with transformer isolation) the current flowing in the power switch. To protect the power switch, the instantaneous current is usually sensed by a current transformer and resistor and compared to a fixed voltage in order to achieve current limiting. Current-injection control (CIC) compares this waveform with an error voltage (clamped to an upper limit to preserve current limiting) to achieve current-mode control.

The circuit diagram for a CIC buck regulator is shown in Figure 4.1. In this circuit, the switch current is sensed by the current transformer and resistor R_w and compared to the error voltage generated by the feedback network. (Multiple buck regulator modules employ the same scheme but share a common error voltage reference, v_e, to force the peak currents in each of the modules to be equal.)

The small-signal block diagram of Figure 3.1 shows the effect of the use of current-mode control on the system. A second feedback loop, T_i, is introduced by the current feedback network which can have dramatic effects upon the small-signal characteristics of the power system. The loop gain expression for this current loop is given by:

$$T_i = F_m F_4 F_i \tag{4.1}$$

For the case of current-injection control, the current-sense gain block, F_i, is a dc gain expression:

$$F_i = \frac{R_w}{n_c}$$

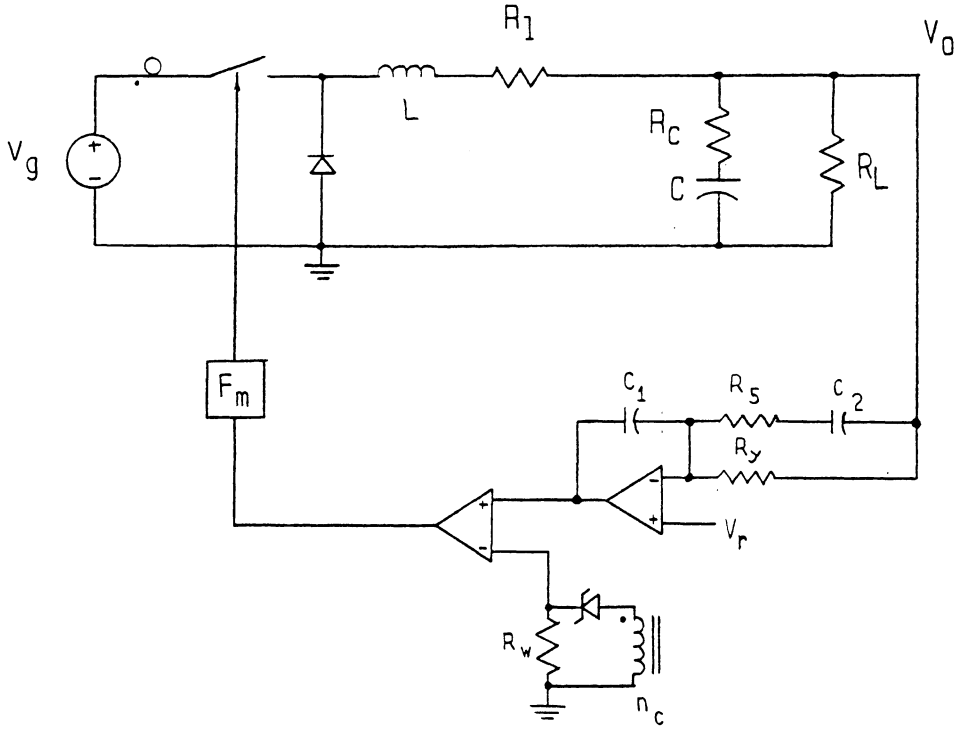


Figure 4.1: CIC-Controlled Buck Converter Circuit, Showing Required Feedback Components.

Loop gain F_4 is as derived in Chapter 2, and F_m is the gain of the pulse-width-modulator (PWM) The current-loop gain significantly affects the small-signal characteristics of the system and should, therefore, be considered as carefully as the voltage-loop gain compensation, T_v.

4.2 Properties of the Current-Loop Gain

The expression for the current-loop gain is given in Equation 4.1. F_m is the duty-cycle modulation gain given by:

$$F_m = \frac{2}{T_p} \frac{1}{(S_n - S_f + 2S_e)} \tag{4.2}$$

where S_n and S_f are the slopes of the current-sense waveform during on and off-times, respectively, of the power switch. An external ramp, Se, similar to that used for a conventional PWM controller, is required to stabilize the system for higher duty cycles.

Several observations can be made about the current-sense loop gain, T_i: firstly, since the gain of F_i is directly proportional to the gain of the current-sense network, and the gain of F_m is inversely proportional to the slopes of the current-sense waveform, the overall gain T_i is independent of current-sense network parameters. The only control over the current loop is through the use of an external ramp which can only serve to decrease the gain.

Without the addition of an external ramp, the bandwidth of the current loop, T_i, is very large, in excess of half of the switching frequency. Also, for practical circuit designs, it can be seen from the expression for F_4 that the phase of the current loop is approximately -90

degrees for frequencies above the resonant frequency. This makes stabilizing the system much simpler. The system loop gain defined as T_1 in Figure 3.1 is given by:

$$T_1 = T_v + T_i$$

It is apparent that for frequencies where the magnitude of the voltage-loop gain is less than that of the current-loop gain, the phase of T_1 will be that of the current loop, -90 degrees at frequencies above resonance. The gain of T_v should, therefore, be reduced below that of T_i before the crossover of T_1 to utilize the stabilizing effects of T_i. If this is done, any right-hand plane zeros or secondary filter poles of T_v occurring after the point where $|T_v| = |T_i|$ will not cause instability. If we make T_i as large as possible, T_v can also be increased to a higher value resulting in improved system performance.

Observation of loop gain T_2 leads to the same conclusions in a more indirect manner:

$$T_2 = \frac{T_v}{1 + T_i}$$

At frequencies beyond the resonant frequency and below the crossover of the current loop, the effect of the -90 degree phase of T_i is to boost the phase of T_2 by +90 degrees. Hence, the maximum benefit is derived from T_i if its crossover is as high as possible. Also, T_2 should be crossed over whilst $|T_i|$ is significantly larger than 1 to use the phase boost from the current loop to stabilize the system. This corresponds to reducing loop gain T_v below that of T_i before T_i crosses over.

4.3 Effect of Current Loop on Closed-Loop System Performance

The closed-loop performance measurements of audiosusceptibility and output impedance are critical parameters for a power system, since they are a good measure of how good a voltage source the system is. The effect of the current loop in improving these performance measures is, therefore, just as important as its stabilizing effects upon the loop gain.

The closed-loop input-output attenuation, or audiosusceptibility, of the buck converter is given by:

$$K_a = \frac{F_1}{1 + T_1} \tag{4.3}$$

$$= \frac{F_1}{1 + T_i + T_v} \tag{4.4}$$

where F_1 is the open-loop input-output transfer function as given in Chapter 2.

The effect of the gain of T_i is, therefore, significant in the attenuation of noise from input-to-output. The gain of T_v at higher frequencies can be reduced for stability, whilst retaining good noise rejection. If T_i is reduced to a small value, the bandwidth of T_v must significantly increase to obtain the same noise attenuation. This can be difficult to achieve while maintaining stability for boost and buck/boost converters or systems with a second LC filter.

From the small-signal block diagram of the buck converter, closed-loop output impedance can be derived to obtain:

$$Z_o(s) = \frac{Z_p(s) + T_i \left[\dfrac{R_L\left(sR_c + \dfrac{1}{C}\right)}{sR_L + \dfrac{1}{C}} \right]}{1 + T_v + T_i} \tag{4.5}$$

where $Z_p(s)$ is the open-loop output impedance.

From Equation 4.5 it can be seen that for the case when $|T_i| >> 1$, the expression for the output impedance can be simplified to give:

$$Z_o(s) = \frac{T_i \, Z_1}{T_i + T_v} \tag{4.6}$$

where Z_1 is the impedance of the load in parallel with the output capacitor.

It can be seen from Equation 4.6 that the output impedance no longer depends upon the filter of the power stage when $|T_i| >> 1$, but upon the load impedance and output capacitor only. This is consistent with the concept of the current-mode control creating a current source from the inductor.

It can also be seen from Equation 4.6 that when $|T_v| > |T_i|$ the output impedance can be approximated by:

$$Z_o(s) = \frac{T_i}{T_v} \, Z_1 \tag{4.7}$$

It would appear from the Equation 4.7 that a large value of T_i actually increases the output impedance. However, when T_i is increased,

T_v may also be increased by the same amount whilst retaining the same stability performance. It should be also noted that the output impedance does not demonstrate resonant peaking whilst the current-loop gain is large, thereby reducing the peak value of output impedance that would be obtained with single loop control. A large gain of T_i is, therefore, desirable from stability and all closed-loop performance standpoints.

4.4 Second-Order Effects on Current-Loop Gain for CIC

The circuit diagram for a transformer-isolated buck converter is shown in Figure 4.2. Assuming ideal circuit elements, the switch current sensed by the current-sense transformer is equal to the inductor current multiplied by the turns ratio. The sensed current waveform is shown in Figure 4.3.

Figure 4.4 shows the same circuit, but including the parasitic elements of the power transformer and some other circuit elements. The switch current is now equal to the inductor current plus the currents through the other parasitic elements, as shown in the circuit diagram. The resulting current-sense waveform is shown in Figure 4.5.

There are several components of this non-ideal waveform which cause significant problems with the implementation of CIC. Firstly, for a large, dc output, low-noise supply, the dc portion of the waveform is large compared to the ramp used for control purposes. When scaling the waveform for use at the logic voltage levels of the control circuit, the ramp at the top of the waveform may be very small, and the system will be very noise sensitive.

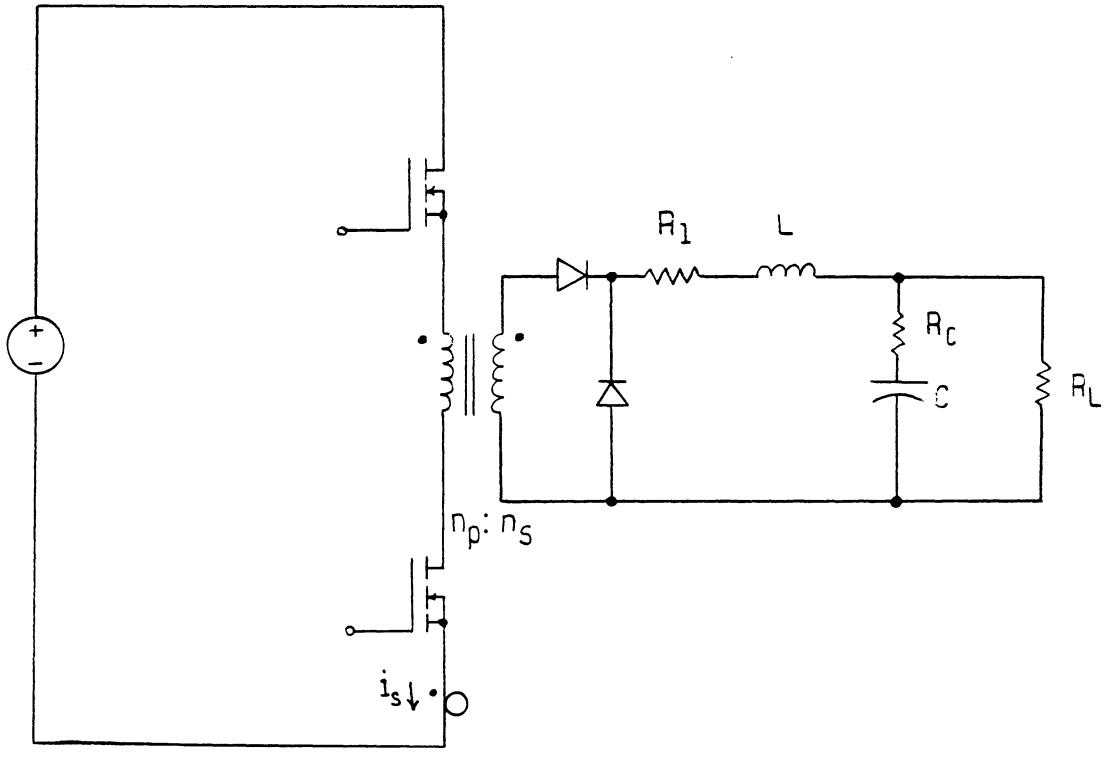


Figure 4.2: Transformer-Isolated Buck Circuit (Forward Converter) without Second-Order Parasitic Elements.

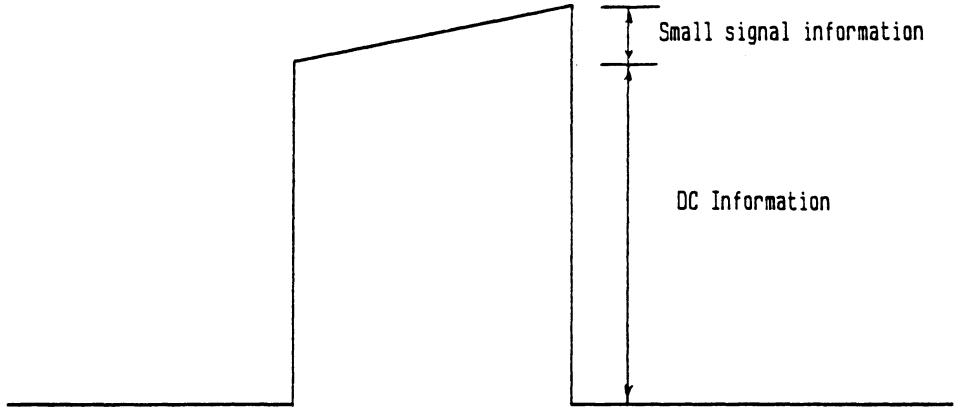


Figure 4.3: Ideal Control Waveform for CIC Control of Buck Converter Circuit.

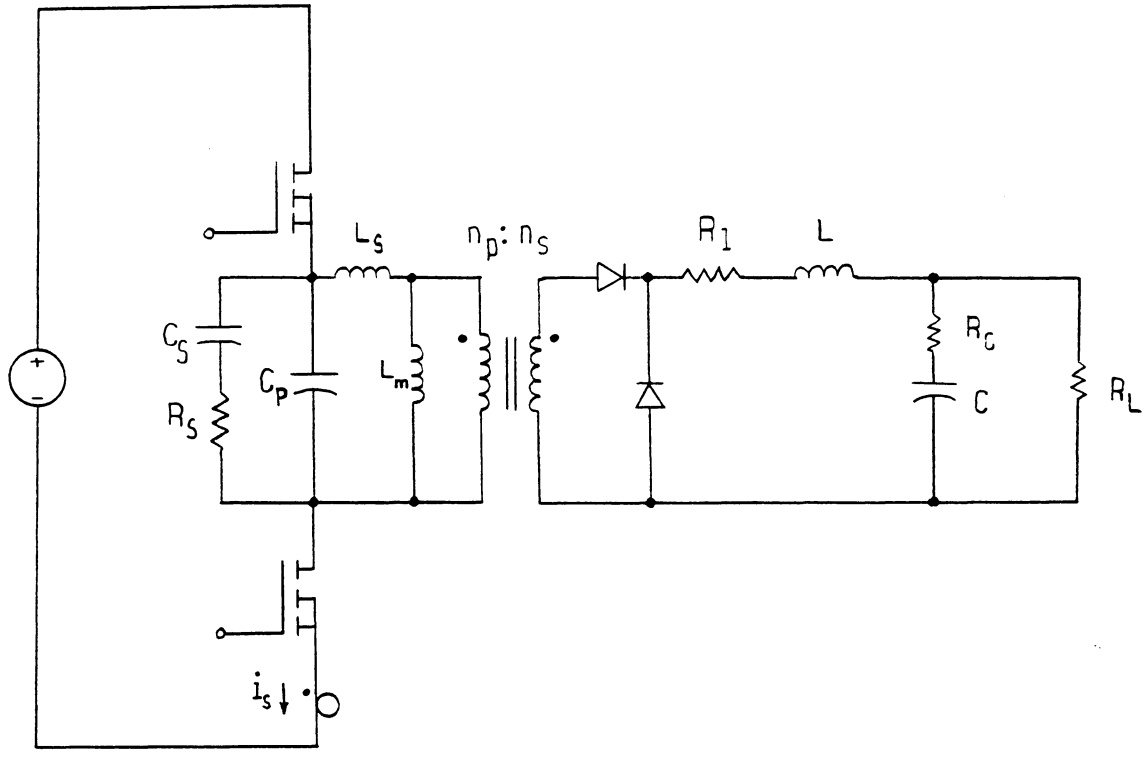


Figure 4.4: Transformer-Isolated Buck Circuit (Forward Converter) Including Second-Order Parasitic Elements and Snubber Components. (Core Reset Components not shown)

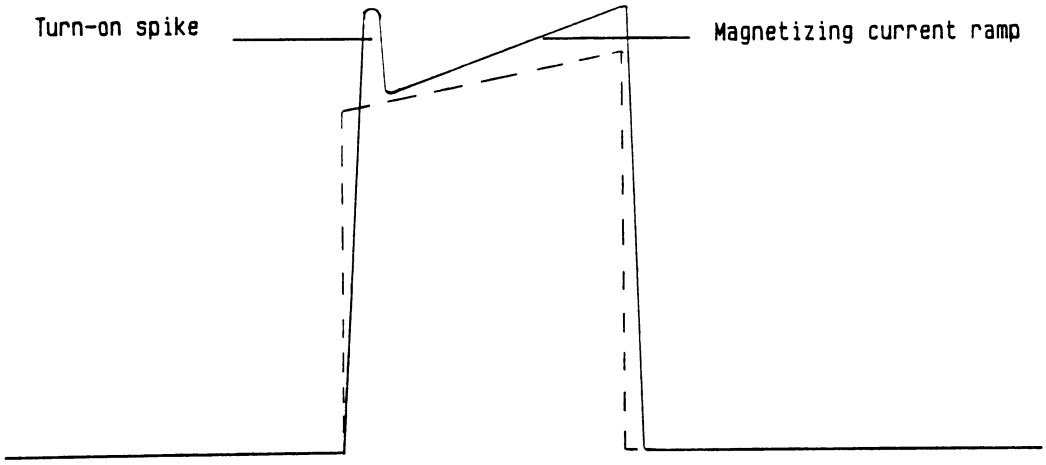


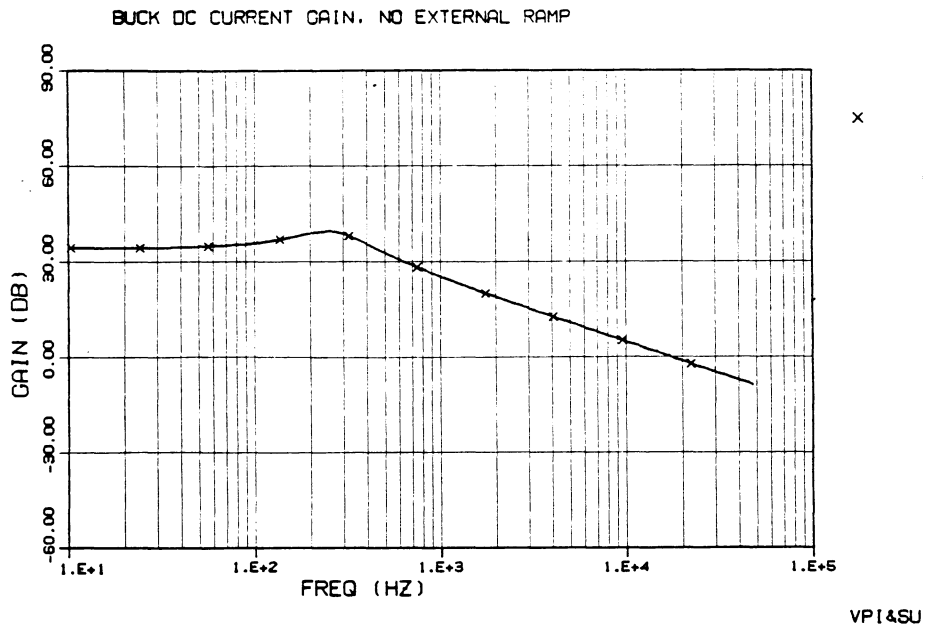
Figure 4.5: Control Waveform for CIC Control of Buck Converter Circuit, Showing Effects of Second-Order Elements.

A second problem is the spike at the beginning of the turn-on. In order to eliminate the effect of the turn-on spike and the sensitivity of the small ramp, an external ramp must be added. This will reduce the current-loop gain significantly often causing instability.

A third effect is that of the magnetizing inductance which effectively adds a constant slope to the control signal. This effect cannot be distinguished from the observed waveform, but it can significantly reduce the gain of the current loop.

The result of all these second-order effects is demonstrated for a real case of a transformer-isolated buck converter. Figures 4.6 through 4.8 show the current, voltage and loop gain T_1 of the system before the second-order effects are considered. It can be seen that the loop gain has high bandwidth and an excellent stability margin.

The frequency responses of Figures 4.9 and 4.10 show the same system with the inclusion of second-order effects and the addition of an external ramp to eliminate the noise problems. The gain of the voltage loop is kept constant to keep the noise rejection performance as before. It can be seen that the current loop gain has been drastically reduced, resulting in a marginally stable system. The addition of a second filter and the inclusion of other second order effects such as switch delays will certainly cause instability, and the system performance must be severely degraded to maintain stability.



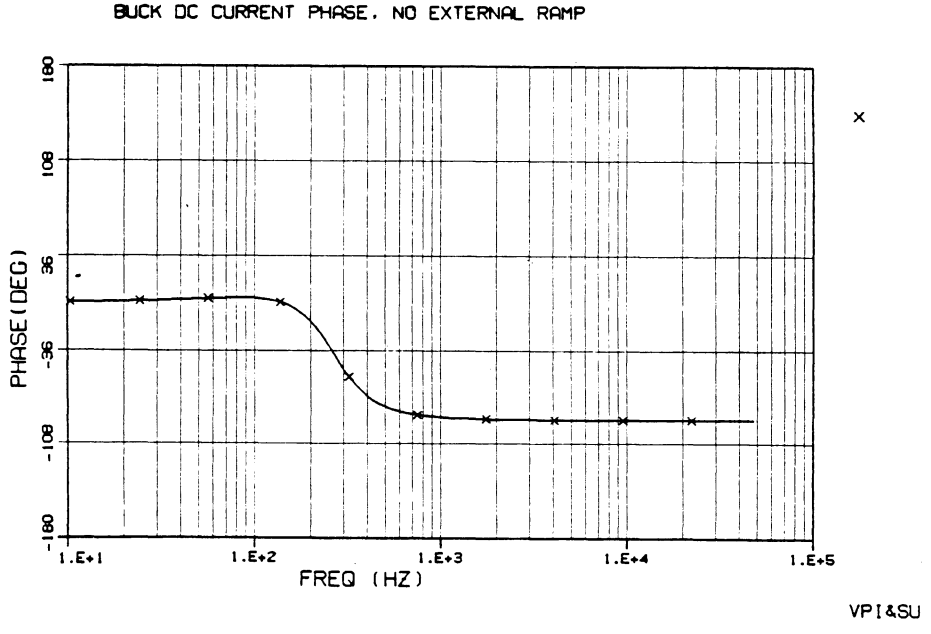


Figure 4.6: Buck Converter Circuit with CIC Control. Current Loop Gain, T_i for Ideal Circuit Elements.

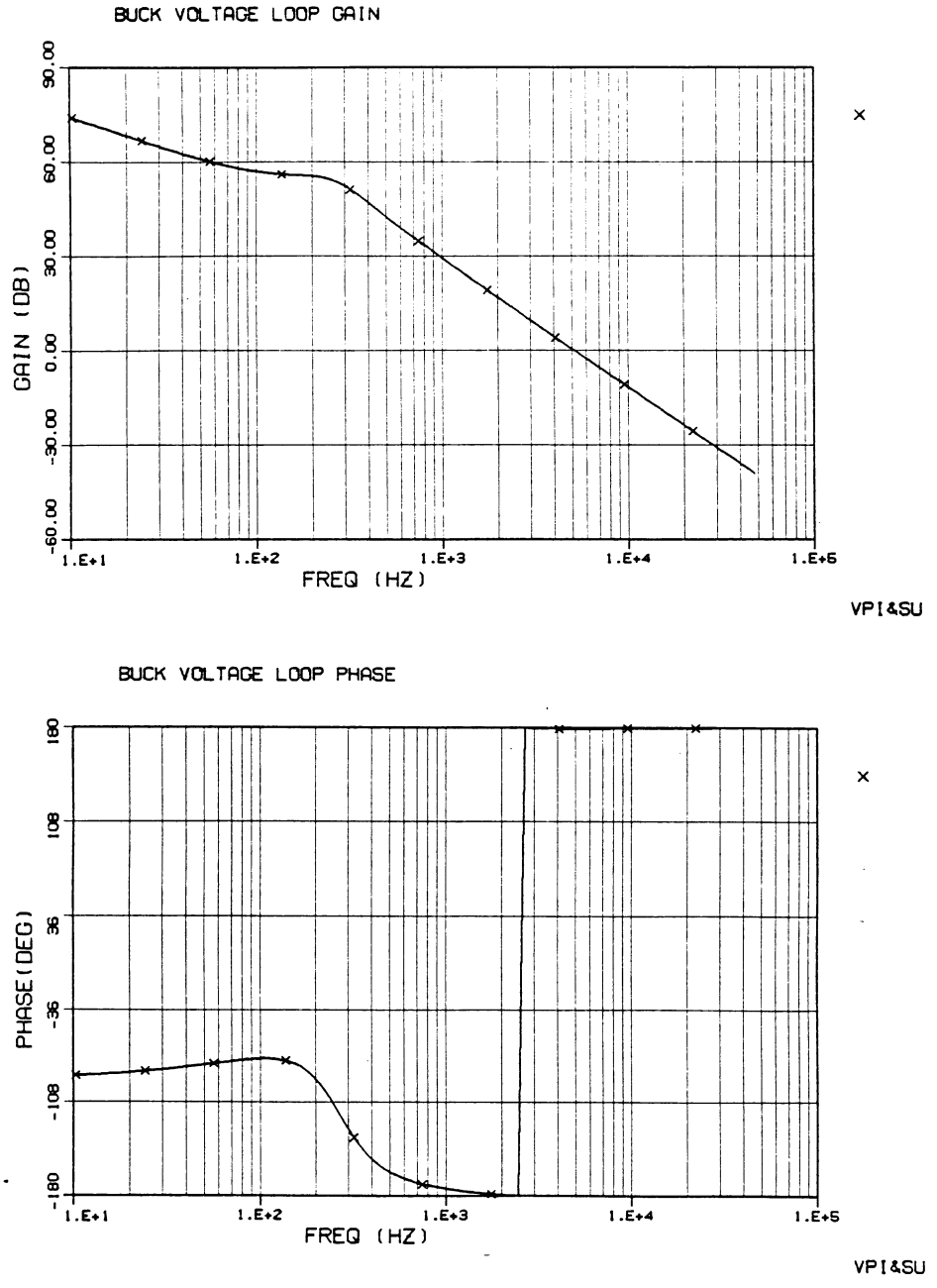


Figure 4.7: Buck Converter Circuit with CIC Control. Voltage Loop Gain, T_v for Ideal Circuit Elements.

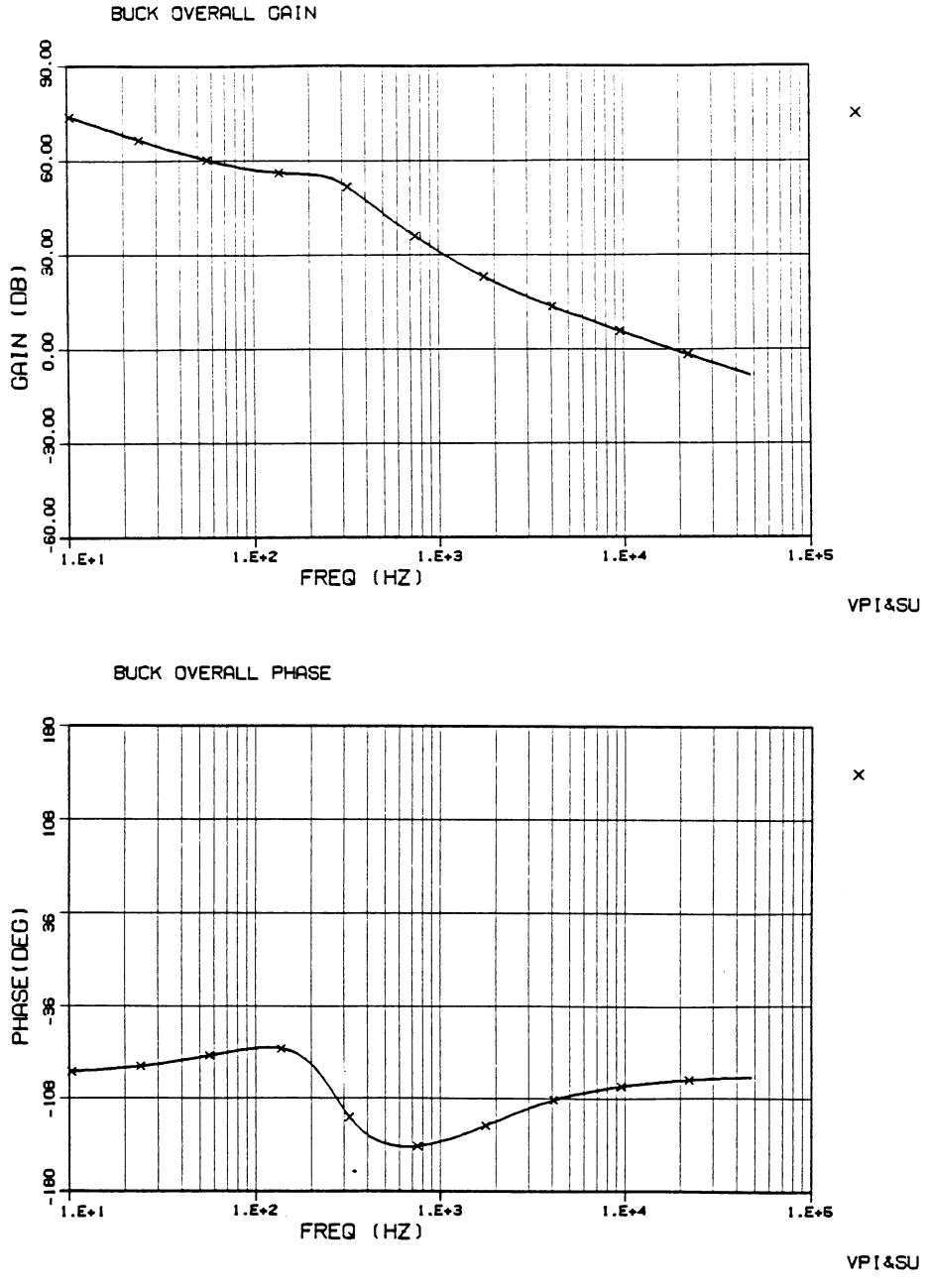


Figure 4.8: Buck Converter Circuit with CIC Control. Open Loop Gain, T_1 for Ideal Circuit Elements.

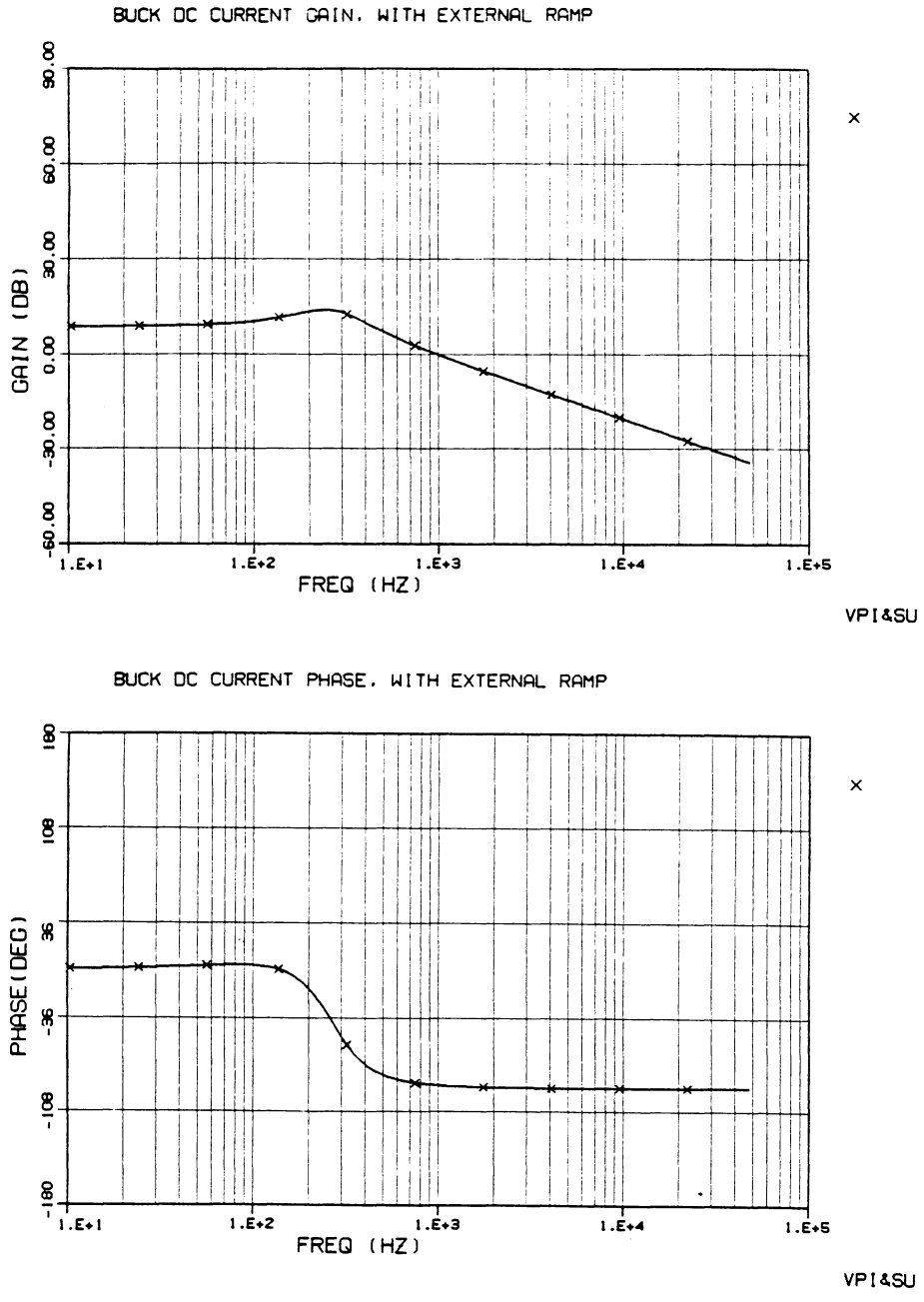


Figure 4.9: Buck Converter Circuit with CIC Control. Current Loop Gain, T_i for Non-Ideal Circuit Elements and External Ramp.

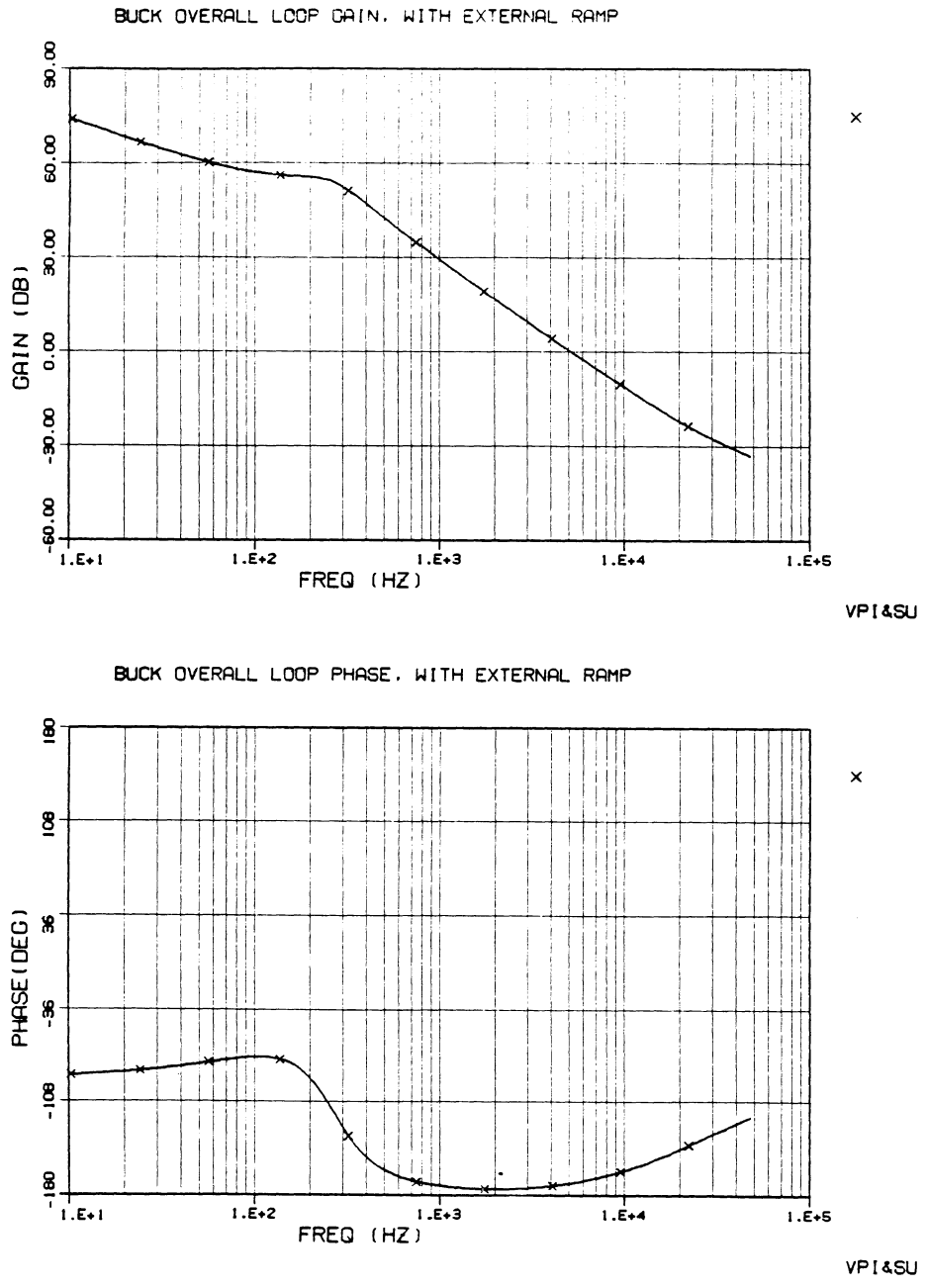


Figure 4.10: Buck Converter Circuit with CIC Control. Open Loop Gain, T_1 for Non-Ideal Circuit Elements and External Ramp.

4.5 Standard Control Module Implementation of Current-Mode Control

A second method of achieving current-mode control is with the standard control module (SCM) [1]. The circuit diagram of this type of control is illustrated in Figure 4.11. Instead of sensing the switch current, the inductor voltage is sensed with a secondary winding and integrated through R_4 and C_1 to reconstruct the inductor current. There are several advantages and disadvantages of this control scheme.

Since the inductor current is reconstructed with an op-amp integrator, the dc information about the level of the inductor current is lost. A separate network is required to limit the switch current and to allow for current sharing. On the other hand, the absence of the dc portion of the current eliminates the problem of a large dc-ramp ratio experienced with CIC, and the control ramp may be made large to eliminate any noise susceptibility problems.

Since the inductor voltage is sensed directly across the inductor, the waveform used for control purposes is unaffected by current spikes due to stray capacitances and the external ramp caused by the transformer magnetizing current. The gain of the current loop need not, therefore, be degraded by the addition of an external ramp.

For these reasons, SCM is superior to CIC in high-current applications with transformer isolation for a single module. Notice that for the single module, the only additional components required to implement SCM are a secondary winding on the inductor and a resistor, R_4.

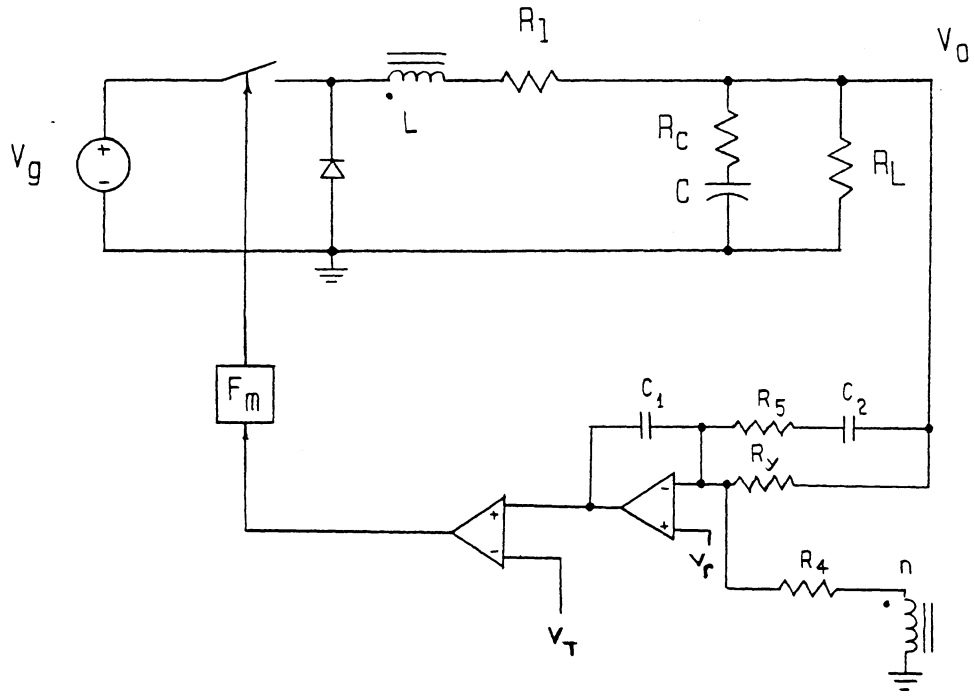


Figure 4.11: SCM-Controlled Buck Converter Circuit, Showing Required Feedback Components.

4.6 Combined SCM/CIC for Control of Multiple Modules

A combination of SCM/CIC may be used for the control of parallel modules. In this scheme, the dc portion of the switch current is summed with the ramp from the SCM scheme, as shown in Figure 4.12. For multiple modules, a separate op-amp is required to integrate the current, and a resistor must be placed across the integrated capacitor to prevent any dc offset from the integrator. The control waveforms for this circuit are shown in Figure 4.13.

The effect of the resistor across the integrator for the SCM is to compensate the current-loop gain block, F_i. If F_i is the gain of this block without the resistor, then the new gain is:

$$F_i' = \frac{s}{\left(s + \frac{1}{C_1 R_6}\right)} F_i \qquad (4.8)$$

In designing the control loop, the pole of this function should be placed at a frequency below where the voltage loop $|T_v| >> |T_i|$. In this case, loop gain T_1 of Equation 3.1 is unaffected by the addition of the pole. The audiosusceptibility in Equation 4.4 is then also unaffected by this compensation.

The equation for loop gain T_2 is affected by the presence of this pole:

$$T_2 = \frac{T_v}{1 + T_i} = \frac{T_v}{T_i} \quad \text{when } |T_i| >> 1$$

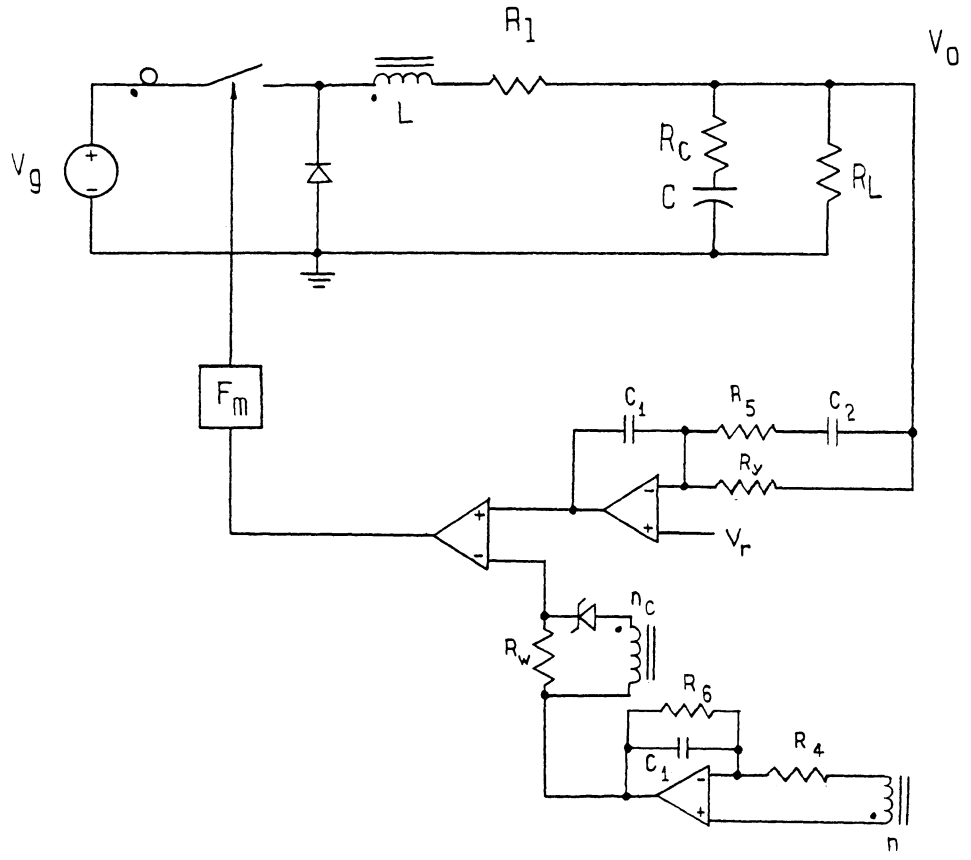


Figure 4.12: SCM/CIC-Controlled Buck Converter Circuit, Showing Required Feedback Components.

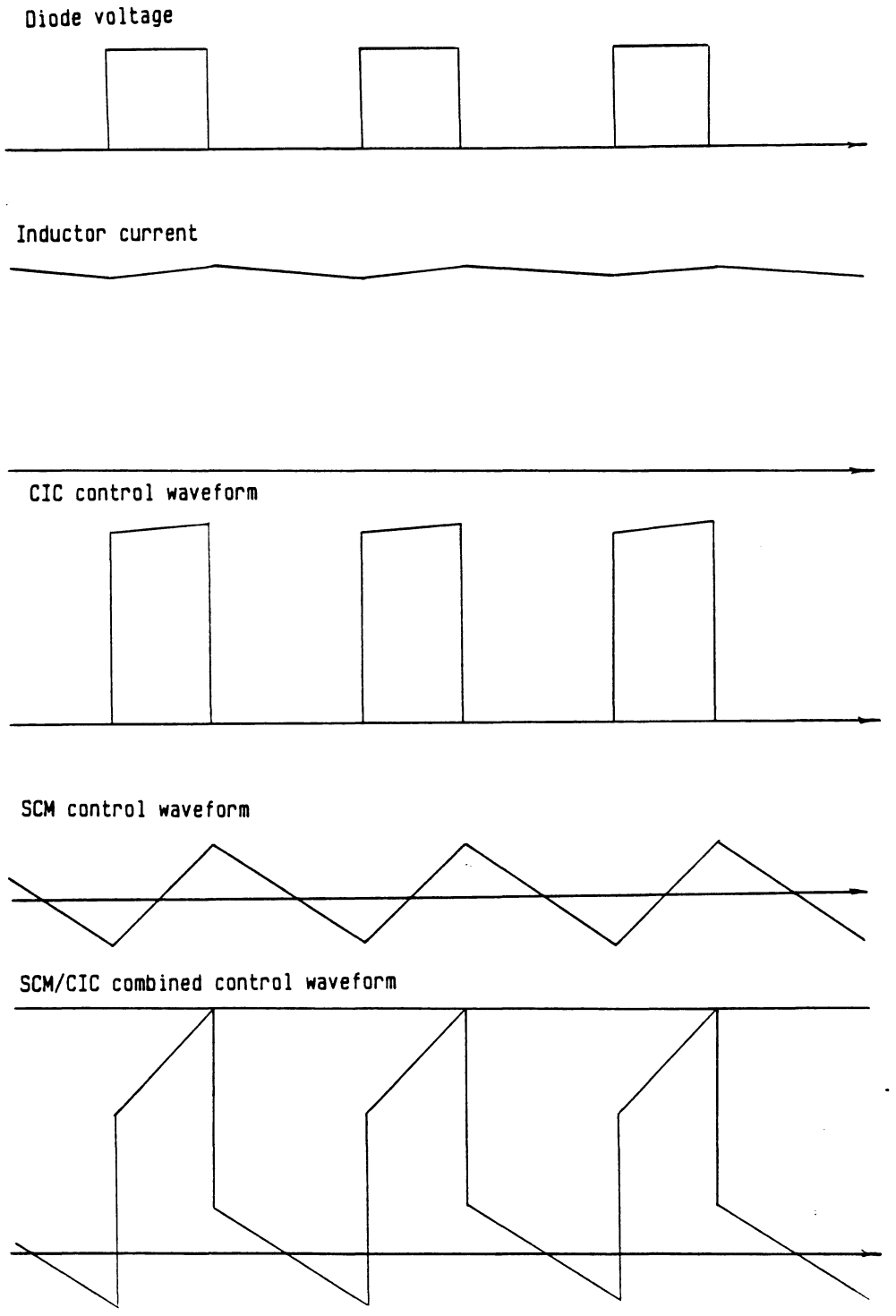


Figure 4.13: Control Waveform for Combined SCM/CIC Control of Buck Converter Circuit.

Since the effect of the resistor is to introduce a zero-pole gain into T_i, at frequencies below the pole, the phase of the current loop will be increased by 90 degrees. Correspondingly, the phase of T_2 will be decreased by 90 degrees. However, if the pole is placed well below the crossover of T_2, this effect will only be upon the conditional stability of T_2, and the system will not be unstable. The effect of the placement of the pole of the integrator on loop gain T_2 is shown in Design example 2 in Chapter 8.

It can also be seen from Equation 4.7 that the gain of the output impedance is decreased at frequencies below the pole and the effect of the pole is to improve the output impedance response. This effect is also demonstrated in Design example 2 of Chapter 8.

The effect of adding SCM to the previous example of the transformer-isolated buck converter is shown in Figures 4.14 through 4.16. It can be seen that the current-loop gain T_i is restored to its value before the second-order effects are added and this control scheme is indeed useful.

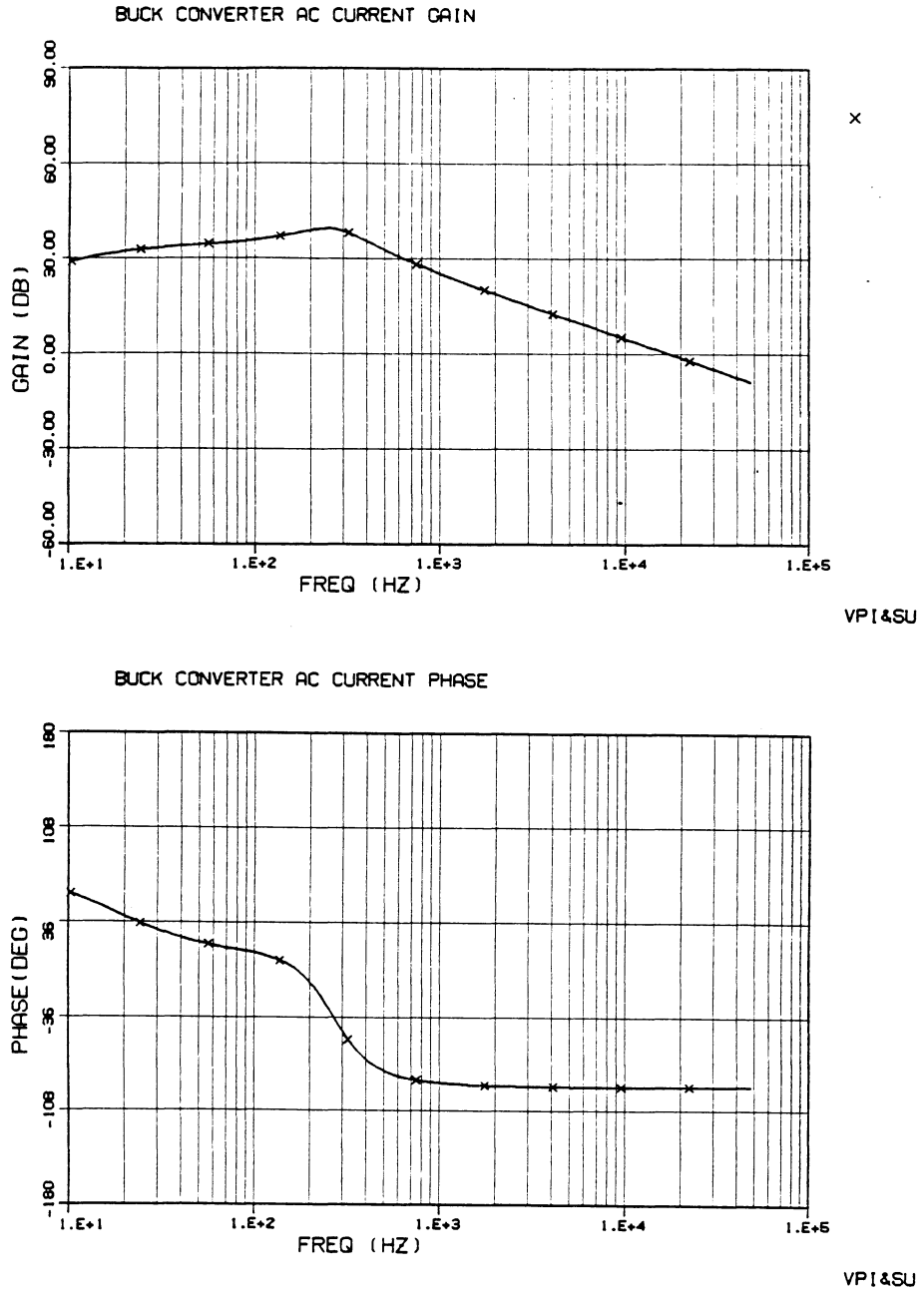


Figure 4.14: Buck Converter Circuit with SCM/CIC Control. SCM Component of Current Loop Gain, T_i.

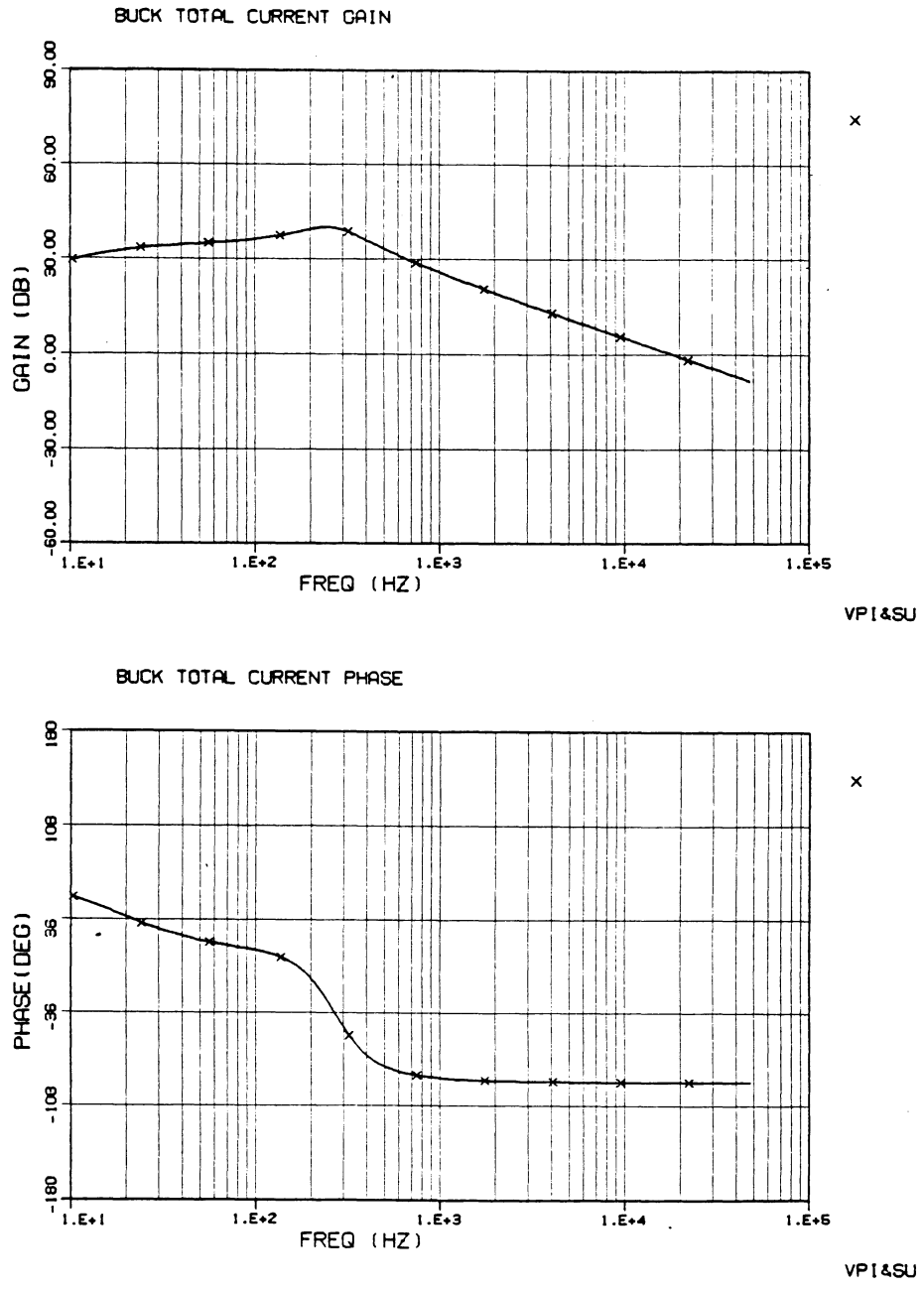


Figure 4.15: Buck Converter Circuit with SCM/CIC Control. Combined Current Loop Gain, T_i.

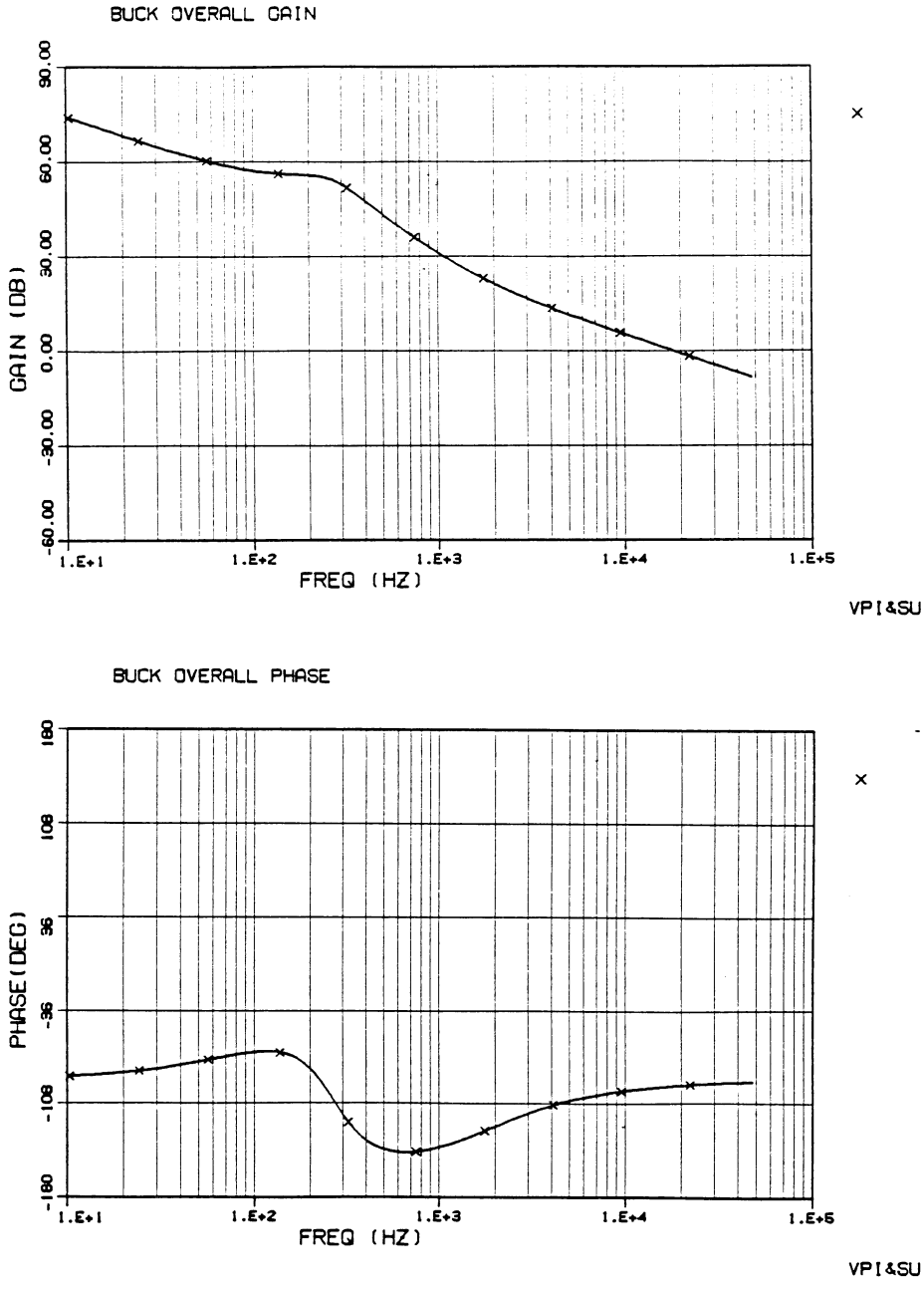


Figure 4.16: Buck Converter Circuit with SCM/CIC Control. Open Loop Gain, T_1.

4.7 Conclusions

It is shown in this chapter that different implementations of current-mode control (SCM and CIC) offer distinct advantages, and the benefits of both schemes can be combined to control multiple parallel modules. For single converter modules, the use of SCM is recommended over that of CIC since its additional component count is minimal, and the noise problems inherent to CIC are eliminated. This is especially true for high power applications.

Design procedures for the implementation of SCM, CIC or a combination SCM/CIC will be developed in the next two chapters, allowing for a single step-by-step procedure for a reliable and predictable system.

Chapter 5

SCM/CIC Design for Parallel Power Modules

The loop gains, T_i and T_v, for parallel power modules were derived in Chapter 3. Comparison of these expressions with those for a single module with k inductors in parallel shows that they are identical with the exception of a dc gain term due to the differing values of F_m and F_i, evaluated for the two different cases. These gains may depend on the value of the inductor for the power stage and will be different if sensing the current through individual inductors, as for the parallel modules, or through a lumped parallel inductance, as with the equivalent single power stage.

In this chapter, the gains of F_m and F_i are considered for the possible current-mode control schemes and unified with the definition of a control time constant for the current loop. The gains of the current and voltage loops for the single and multiple modules can then be analyzed for all three control schemes and compared. It is then demonstrated that the current-loop gain of the multiple modules may be made equal to that of the single module, merely by adjusting the external compensation ramp of the pulse-width modulator. The voltage-loop gain may also be made identical to that of the single module since its gain may be adjusted arbitrarily. When the open-loop parameters of the equivalent single and multiple modules are made identical, it can be easily demonstrated that the closed-loop characteristics are also the same.

Step-by-step design procedures were given for the control of a single power stage module using SCM [1]. Following the analysis of this chapter, these design procedures may be extended for the design of any of the

current-mode control schemes discussed and for the use of single or multiple power modules.

5.1 Loop Gains for Parallel Power Modules

In Chapter 3 the voltage-loop gain transfer function was derived for the buck converter to obtain:

$$T_v = F_m F_v F_2'$$

$$= F_m F_v \frac{V_g}{L'} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)} \qquad (5.1)$$

where $L' = L/k$ and $R_{11} = R_1/k$.

The above expression for F_2' is the same as the duty-cycle-to-output-voltage transfer function for a single converter with k parallel inductors, each of value L and equivalent series resistance R_1. The gain F_m, however, is the pulse-modulator gain evaluated for the individual inductor of each power stage, since each has its own feedback network. The voltage-compensation gain is F_v which may be selected arbitrarily.

For a single module with k parallel inductors, the voltage-loop gain is:

$$T_v' = F_m' F_v' F_2' \qquad (5.2)$$

where F_m' is the pulse-modulator gain evaluated using the inductance of k inductors in parallel. The compensation-voltage gain F_v' may be optimized using the procedures given in Reference [1]. If the voltage gain F_v of the k parallel modules is adjusted such that $F_m F_v = F_m' F_v'$, the voltage-loop gain of the parallel module system can be made identical to that of a single module system.

The equivalent current-loop gain for k converter modules was derived in Chapter 3 to obtain:

$$T_i = F_m F_i F_{ac}'/k \tag{5.3}$$

$$= F_m F_i \frac{V_g}{kL'} \frac{\left(s + \frac{1}{CR_L}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)}$$

The expression for F_{ac}' is equal to the duty-cycle-to-inductor-current transfer function for a single power module with k parallel inductors. The expressions for F_m and F_i are again those for each individual module. The current-loop gain for a single converter with a parallel inductance is:

$$T_i' = F_m' F_i' F_{ac}' \tag{5.4}$$

Comparison of Equations 5.3 and 5.4 shows that the current-loop gain for the parallel modules differs from that of the equivalent single module by a dc gain term. It can also be seen from these equations that, if the

gain of the pulse modulator can be adjusted such that $F_m F_i/k = F_m{}'Fi'$, the current-loop gains for the two systems are then identical.

5.2 Design Unification

To derive a procedure for simplifying the design of the multiple-module control loop as outlined above, the expressions for F_m and F_i must be examined to see how they are affected by the inductance value. In the following analysis, definitions are made to unify the three types of current-mode control, with the definition of a current-loop time constant to be used for analysis in place of circuit components. With these definitions, the comparison of the gains of multiple and single modules is simplified, and design procedures may be developed later for any of the control schemes.

To achieve these goals, first, the current sense gain block, F_i, is examined. For SCM, CIC or combined SCM/CIC control, the current-loop gain block is given by the following expressions, where the circuit elements are those defined in Figures 4.1, 4.11 and 4.12 for the appropriate control scheme:

$$F_i = \frac{nL}{R_4 C_1} \qquad \text{for SCM.} \tag{5.5}$$

$$F_i = \frac{R_w}{n_c} \qquad \text{for CIC.} \tag{5.6}$$

$$F_i = \frac{R_w}{n_c} + \frac{nL}{R_4 C_1} \qquad \text{for CIC/SCM.} \tag{5.7}$$

In order to have just a single expression for F_i, the following definitions are made:

$$\tau_{scm} = \frac{R_4 C_1}{n} \tag{5.8}$$

$$\tau_{cic} = \frac{n_c L}{R_w} \tag{5.9}$$

$$\tau_m = \tau_{scm} \qquad \text{for SCM} \tag{5.10}$$

$$\tau_m = \tau_{cic} \qquad \text{for CIC} \tag{5.11}$$

$$\tau_m = (1/\tau_{cic} + 1/\tau_{scm})^{-1} \qquad \text{for CIC/SCM} \tag{5.12}$$

With the above definitions, the current-sense gain block is now a single expression for all three control schemes:

$$F_i = \frac{L}{\tau_m} \tag{5.13}$$

A physical interpretation of the above definitions helps to show the intent of this approach. The time constant τ_m, defined above, determines the slope of the ramp of the control waveform for each of the control schemes. If τ_m is fixed from one control scheme to the next, then the current sense ramp used in the feedback is identical for all cases. This

is illustrated in Figure 5.1. It is intuitive that if the feedback waveform is the same for each control scheme, neglecting the dc portion of the waveform, then the small-signal characteristics will also be identical. By using the parameter τ_m to represent the control characteristics for the current loop, a general design procedure can be developed.

Next, the gain of the pulse-width-modulator block is considered. For constant frequency operation, the pulse-modulator gain is:

$$F_m = \frac{2}{T_p} \frac{1}{(S_n - S_f + 2S_e)} \tag{5.14}$$

The slopes of the control ramp, S_n and S_f, are determined by the power stage and the control parameter time constant τ_m. It can be demonstrated that the pulse-width-modulator gain block, F_m, can be written as:

$$F_m = \frac{2\tau_m}{M} \tag{5.15}$$

where, for the buck converter,

$$M = V_g(1-2D)T_p + 2S_e T_p \tau_m \tag{5.16}$$

From Equations 5.13 and 5.15, the current-loop gain expression can now be written as:

$$T_i = F_m F_i F_{ac}'/k = \frac{2\tau_m}{M} \frac{L}{\tau_m} \frac{F_{ac}'}{k}$$

$$= \frac{2L/k}{M} F_{ac}' = \frac{2L'}{M} F_{ac}'$$

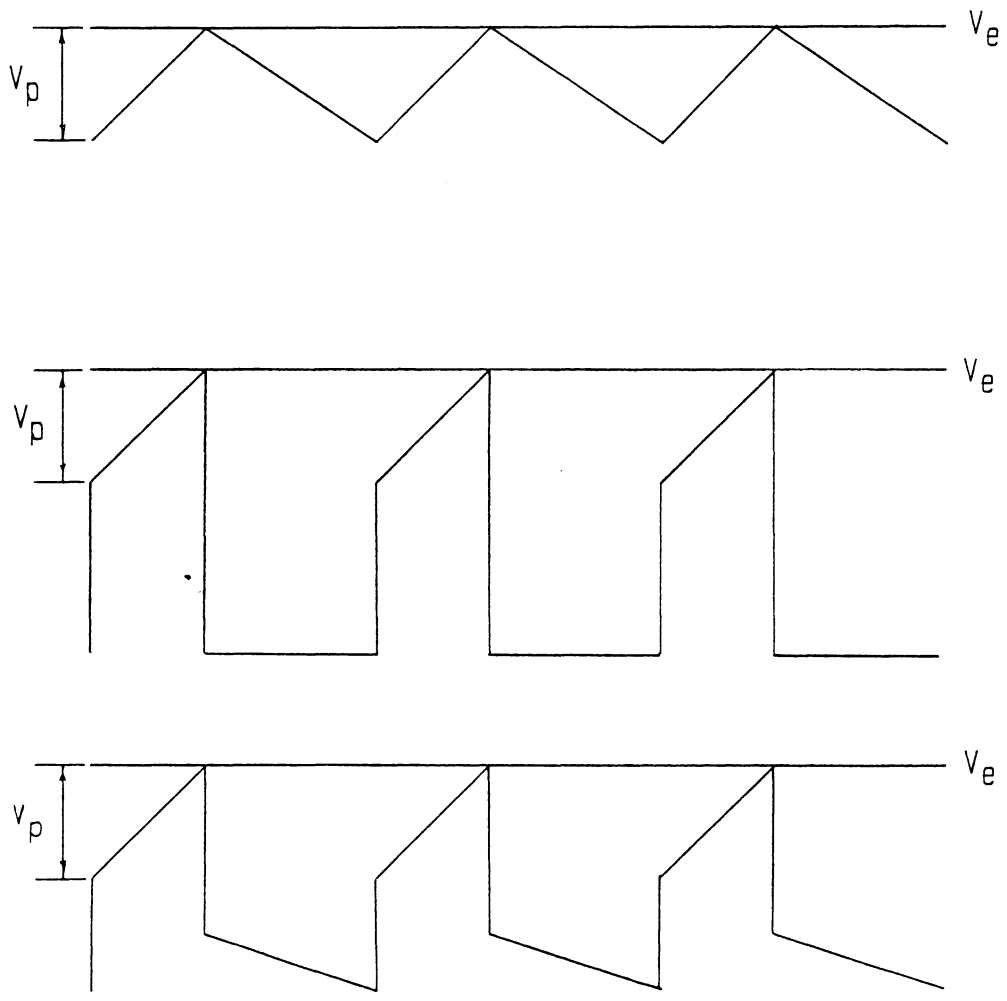


Figure 5.1: SCM, CIC and Combined SCM/CIC Control Waveforms with Identical Time Constant τ_m for Identical Small-Signal Performance. Each Waveform has the Same Peak Amplitude, V_p.

The above expression for T_i is identical to the current-loop gain for an equivalent single module, with the exception of the value of M. As shown in Equation 5.16, M is a function of the input voltage, duty cycle and switching frequency (all independent of the number of modules), and a term dependent on the value of the added external ramp and the time constant of the current loop, τ_m. For the single module, the gain of the pulse modulator is adjusted to avoid instability with the addition of an external ramp, S_e'. The time constant of the current loop for the single module is τ_m'. If the slope of the external ramp added to the multiple-module control, S_e, is scaled such that $S_e = S_e'\tau_m'/\tau_m$, the value of M is equal for the multiple and single modules, and the current-loop gains are identical:

$$T_i = \frac{2L'}{M'} F_{ac}' \quad \text{where } M' = V_g(1-2D)T_p + 2S_e T_p \tau_m'$$

$$= \frac{2\tau_m'}{M'} \frac{L'}{\tau_m} F_{ac}'$$

$$= F_m' F_i' F_{ac}'$$

Hence, by merely adjusting the slope of the external ramp, S_e, the current-loop gain, T_i, for k parallel modules can be made identical to that of the equivalent single power stage module with k parallel inductors. (An intuitive explanation may be given for this approach: considering the case of the multiple modules with CIC, the slope of the current-sense waveform is less than that of a single module with k par-

allel inductors using the same feedback network, since the slope decreases with larger inductance. The value of the external ramp to be added to obtain the same control characteristics of the current loop is correspondingly reduced by the same amount. This amount is given by τ_m'/τ_m, since this is the ratio of the slopes for the two cases.)

Next, the voltage-loop gain of the k parallel modules is evaluated. From Equations 5.1 and 5.15, the voltage-loop gain for the parallel modules can be written as:

$$T_v = F_m F_v F_2' = \frac{2\tau_m}{M} F_v F_2'$$

$$= \frac{2\tau_m'}{M} \frac{\tau_m}{\tau_m'} F_v F_2'$$

If the external ramp is scaled, as for the current loop above,

$$T_v = \frac{2\tau_m'}{M'} \frac{\tau_m}{\tau_m'} F_v F_2'$$

$$= F_m' \frac{\tau_m}{\tau_m'} F_v F_2'$$

If the voltage loop is now scaled by τ_m'/τ_m to give F_v', then:

$$T_v = F_m' F_v' F_2'$$

This is exactly the expression for the voltage-loop gain of a single power module with k parallel inductors.

The design of the control loop of k parallel power stages is now very simple. The system is treated as though it were a single power module, and the design procedures presented in Reference [1] can be applied directly. The external ramp which would be added to stabilize the single module is then reduced by a factor τ_m'/τ_m. (Note that if pure SCM were used, this would be unity. For parallel power stages, SCM cannot be used alone and hence this quantity is less than one.) The gain of the voltage-compensation network is also reduced by the same factor. The resulting multi-module system will then have exactly the same small-signal characteristics as the single module.

5.3 Conclusions

The above analysis shows how the k parallel module power system can be reduced to a design case of just a single module with an equivalent inductance equal to that of the k inductors in parallel. A single, unified design procedure, similar to that in Reference [1] can now be given for the design of single or multiple modules using SCM, CIC or combined SCM/CIC for the buck converter.

The analysis of the different control schemes are also directly applicable to the boost and buck-boost converters and, although the parallel power stages of these converters are not analyzed here, similar results are expected. Design procedures for all three types of power stages are, therefore, included for completeness.

Chapter 6

Control Circuit Design Procedures

In Reference [1], it was shown that the design of the control circuit for the three basic types of converter could be performed in a single, non-iterative manner to concurrently satisfy design specifications of stability, output impedance, step-load response and audiosusceptibility. This was achieved using the SCM scheme for a single converter. Furthermore, it was shown that this scheme of control was sufficient to optimize small-signal performance of the converter, and a more complex voltage-loop feedback circuit is neither necessary nor desirable. This is contrary to the approach of most designers and has not gained great acceptance due to the complexity of the analysis and difficulty of implementing the design procedures in the handbook.

The following design procedure extends the procedure developed in Reference [1] to allow the use of SCM, CIC or combined SCM/CIC for either single or multiple power modules. The procedure also clarifies some of the design steps such as the addition of an external ramp to the pulse modulator and the choice of current-loop control circuit components.

The design steps which are common to the SCM Handbook are given below for completeness, but the derivation of the design equations is not shown here. Although the design steps appear to be quite lengthy and involved, they are actually easy to use and are very amenable to automation through a computer program.

The derivation of the design steps after the unification of the different control schemes for multiple and single modules is explained

in detail in Reference [1]. It is not intended that the user be familiar with these derivations to use the results.

6.1 Design Procedures

The starting point for the design procedure is an equivalent buck, boost or buck-boost converter with equivalent circuit elements as shown in Figures 6.1 through 6.3. In each diagram with k converter modules, k can be equal to one for the single converter module. In each of the converter circuit diagrams, there is an allowance for transformer isolation. This is not restricted to the buck-boost converter. The converter circuit diagrams can, in most cases, be derived from the actual power stage circuit which may, for example, be a full-bridge buck converter rather than the forward converter model shown.

6.2 Power Stage Circuit Elements

L = Inductor value (Secondary inductance for the buck-boost)

C = Output Filter Capacitor

R_c = Output Filter Capacitor ESR

R_l = Inductor ESR

V_g = Input voltage (Source voltage V_s reduced to secondary.)

V_o = Output Voltage

n_p/n_s = Transformer Turns Ratio

D = Duty Cycle

k = Number of Power Modules

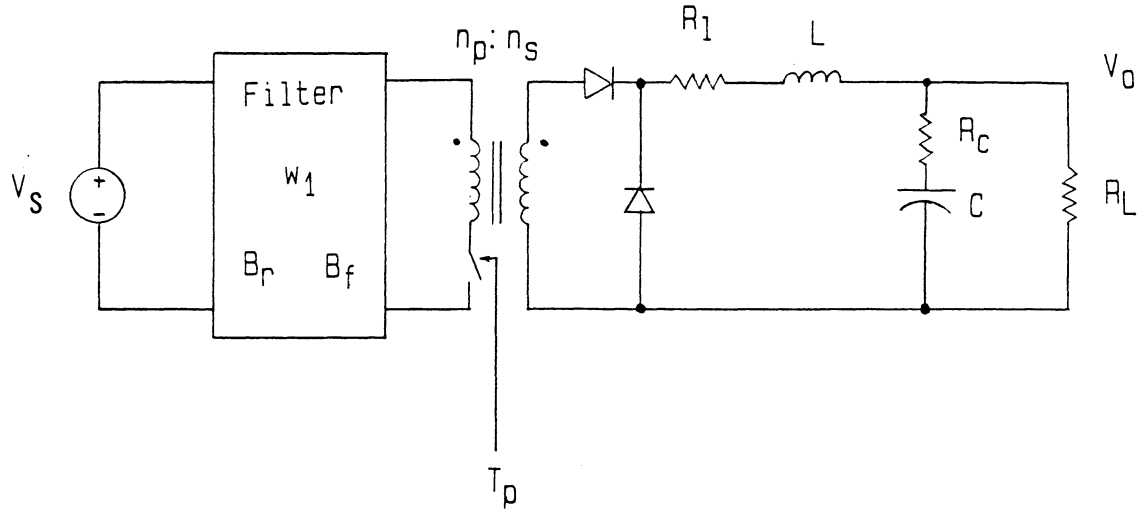


Figure 6.1: Equivalent Power Stage Components for a Transformer-Isolated Buck Regulator with Input Filter.

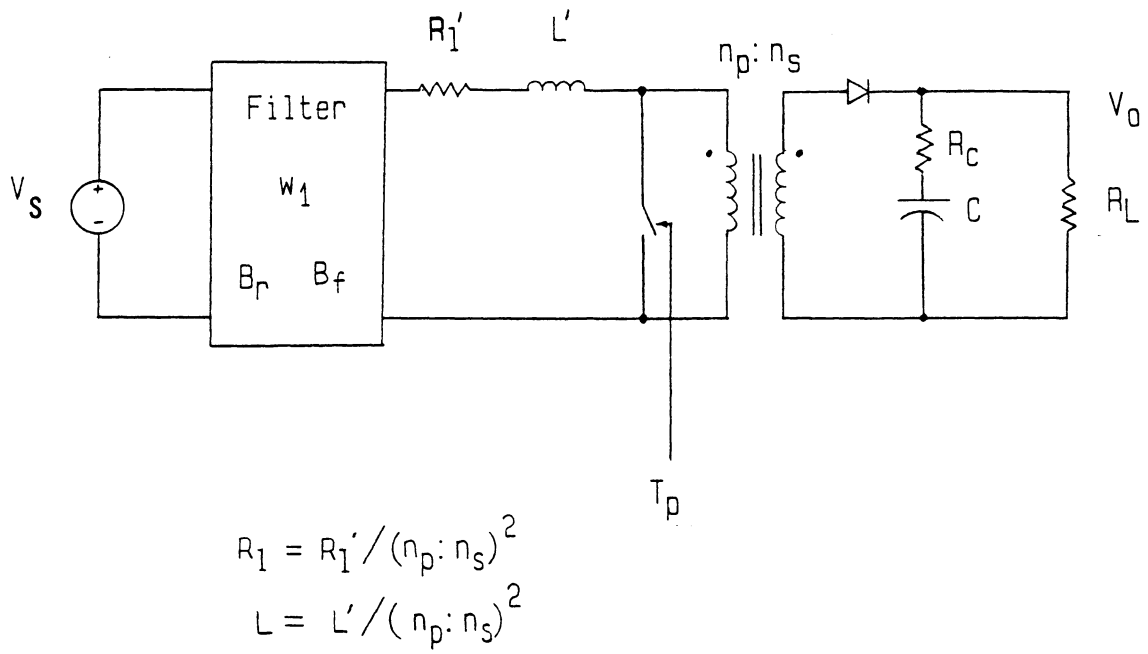


Figure 6.2: Equivalent Power Stage Components for a Transformer-Isolated Boost Regulator with Input Filter.

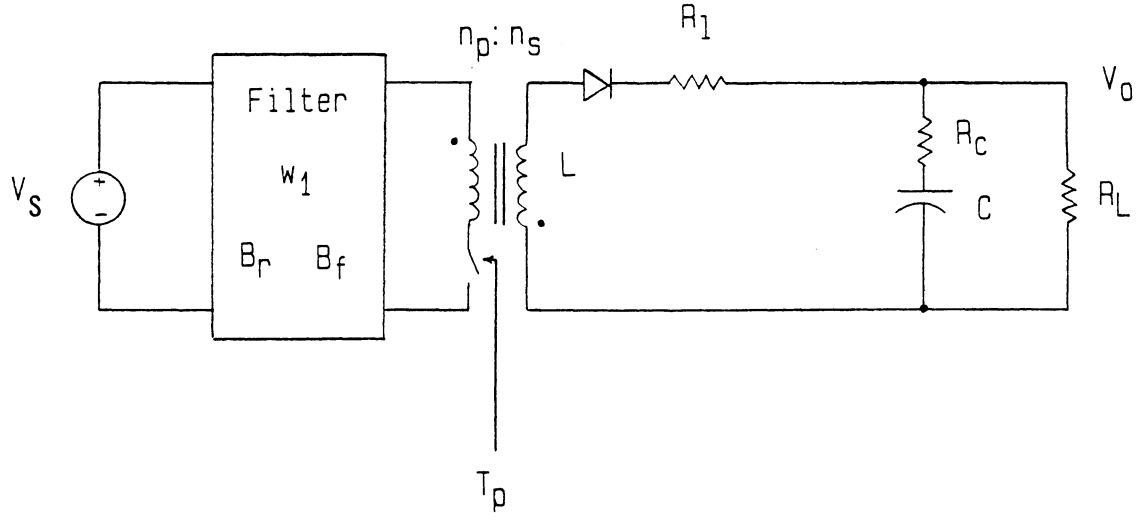


Figure 6.3: Equivalent Power Stage Components for a Transformer-Isolated Buck/Boost Regulator with Input Filter.

R_L = Load Resistance

ω_1 = Input Filter Resonant Frequency

B_f = Peaking of Input Filter at ω_1

B_r = Output Impedance of Input Filter at ω_1

6.3 Design Specifications

Stability Margin

Input-Output Attenuation

Output Impedance

Step-Load Output Voltage Peaking

Transient Response Settling Time

6.4 Design Outputs

R_y	R_5	C_1	R_2	Voltage Loop Control Components
R_w	n_c			CIC Current Loop Control Components
R_4	n	R_6		SCM Current Loop Control Components
S_e				Pulse Modulator External Stabilizing Ramp

6.5 Design Procedure Overview

1) Select control scheme to be used. Recommendations, based on the discussion of Chapter 4 are:

	Single Module	Multiple Modules
Large dc/Ripple Current	SCM	SCM/CIC
Small dc/Ripple Current	CIC	CIC
Transformer-Isolated High Performance	SCM	SCM/CIC
Transformer-Isolated Low Cost	CIC	SCM/CIC

2) Design current-loop time constant τ_m to give sufficient ramp for noise immunity and predictable performance.

3) Design pulse-modulator external ramp slope, S_e, to reduce gain of current loop as duty cycle approaches 0.5.

4) Evaluate design parameters to be used for calculations during the design procedure.

5) Check that input filter interaction will not cause stability problems.

6) Design zeroes of loop gain to satisfy design specifications and give best performance.

7) Choose voltage loop feedback components.

8) Choose current loop feedback components.

6.6 Detailed Design Procedure

1) Select control to be used.

2) Select τ_m to give desired ramp height, V_p. Design equations are as follows:

SCM or CIC:

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} \qquad \text{Buck} \qquad (6.1)$$

$$\tau_m = \frac{V_g DT_p}{V_p} \qquad \text{Boost, Buck/boost} \qquad (6.2)$$

Combined SCM/CIC:

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} \qquad \text{Buck} \qquad (6.3)$$

$$\tau_m = \frac{V_g DT_p}{V_p} \qquad \text{Boost, Buck/boost} \qquad (6.4)$$

$$\tau_{cic} = \frac{LV_o}{kV_m R_L} \qquad \text{Buck} \qquad (6.5)$$

$$\tau_{cic} = \frac{LV_o}{kV_m D' R_L} \qquad \text{Boost, Buck/boost} \qquad (6.6)$$

where V_m is the maximum allowable comparator input.

$$\tau_{scm} = (1/\tau_m - 1/\tau_{cic})^{-1} \qquad (6.7)$$

3) Choose external ramp slope to stabilize converter over full duty cycle range. The high frequency asymptote of the open-loop gain, T_1, for all three converters is approximated by:

$$T(s) = \frac{K_1}{s} \qquad (6.8)$$

where:

$$K_1 = \frac{2V_g}{M} \qquad M = V_g(1-2D)T_p + 2S_e T_p \tau_m \qquad \text{Buck}$$

$$K_1 = \frac{2V_g}{D'M} \qquad M = V_g(2-1/D')T_p + 2S_e T_p \tau_m \qquad \text{Boost}$$

$$K_1 = \frac{2V_g}{D'M} \qquad M = V_g(1-D/D')T_p + 2S_e T_p \tau_m \qquad \text{Buck/boost}$$

As the duty cycle of the constant-frequency converter approaches 50%, the pulse-width-modulator gain becomes very large, and may cause instability. The addition of an external ramp reduces this gain and extends the operating range beyond 50% duty cycle. The open-loop gain

expressions above may be used to formulate a precise guideline for the choice of the external ramp.

If the maximum duty cycle results in a crossover frequency of less than two-thirds the switching frequency, no external ramp is added. This occurs at a 25% duty cycle for all three converters. For a greater duty cycle, an external ramp is added to reduce the crossover to half of the switching frequency. The design equations given below may be used to design the external ramp. The value of the slope to be added will prevent the high frequency crossover from exceeding two-thirds of the switching frequency. By adding the following ramp slopes, the 50% instability problem is eliminated without significant deterioration of the small-signal performance.

If $D < 0.25$, then $S_e = 0$. Else:

$$S_e = V_g(D-0.182)/\tau_m \qquad \text{Buck} \qquad (6.9)$$

$$S_e = V_g(D-0.182)/D'\tau_m \qquad \text{Boost, Buck/boost} \qquad (6.10)$$

4) Evaluate design parameters according to the following equations:

Buck Converter:

$$L_e = L/k$$

$$\omega_0 = 1/\sqrt{L_e C}$$

$$\tau_{z1} = CR_c$$

$$A_1 = 1$$

$$A_2 = 0$$

$$M = V_g(1-2D) + 2S_eT_p\tau_m$$

$$K_1 = 2V_g/M$$

$$K_2 = D$$

$$\mu = n_p/n_s \; 1/D$$

Boost Converter:

$$L_e = L/kD'^2$$

$$\omega_0 = 1/\sqrt{L_eC}$$

$$\tau_{z1} = CR_c$$

$$R_e = R_l/D'^2$$

$$R_{ce} = R_c/D'^2$$

$$R_{eq} = R_e + R_{ce} - R_c$$

$$\zeta = 1/2\omega_0 \; (1/CR_L + (R_e + R_{ce})/L_e)$$

$$A_1 = 1 - R_{eq}/R_L + 2\zeta\omega_0L_e/R_L - (L_e\omega_0/R_L)^2 = 1$$

$$A_2 = 1/CR_L$$

$$K_1 = 2V_g/D'M$$

$$K_2 = D/D' \; (1 + 2V_gL_e/R_LM)$$

$$\mu = n_p/n_s \; D'$$

Buck-boost Converter:

$$L_e = L/kD'^2$$

$$\omega_0 = 1/\sqrt{L_eC}$$

$$\tau_{z1} = CR_c$$

$$R_e = R_l/D'^2$$

$$R_{ce} = R_c/D'^2$$

$$R_{eq} = R_e + R_{ce} - R_c$$

$$\zeta = 1/2\omega_0 \, (1/CR_L + (R_e + R_{ce})/L_e)$$

$$A_1 = 1 - DR_{eq}/R_L + 2\zeta\omega_0 DL_e/R_L - D(L_e\omega_0/R_L)^2 = 1$$

$$A_2 = D/CR_L$$

$$K_1 = 2V_g/D'M$$

$$K_2 = D/D' \, (1 + 2V_g DL_e/R_L M)$$

$$\mu = n_p/n_s \, D'/D$$

5) Check to make sure filter interaction will not affect stability significantly. The forward peaking of the input filter is B_r at its resonant frequency, ω_1. If the following inequality is satisfied, the filter will not affect stability:

$$B_r << \mu^2 R_L \tag{6.11}$$

6) Design zeros of loop gain to satisfy design requirements:

τ_s Settling time

K_a Audiosusceptibility

K_o Output Impedance

K_{op} Output Peaking

Upper Limit of s_{01}

The open-loop gain asymptotes are shown in Figure 6.4, defining the zeroes of the loop gain, s_{01} and s_{02}.

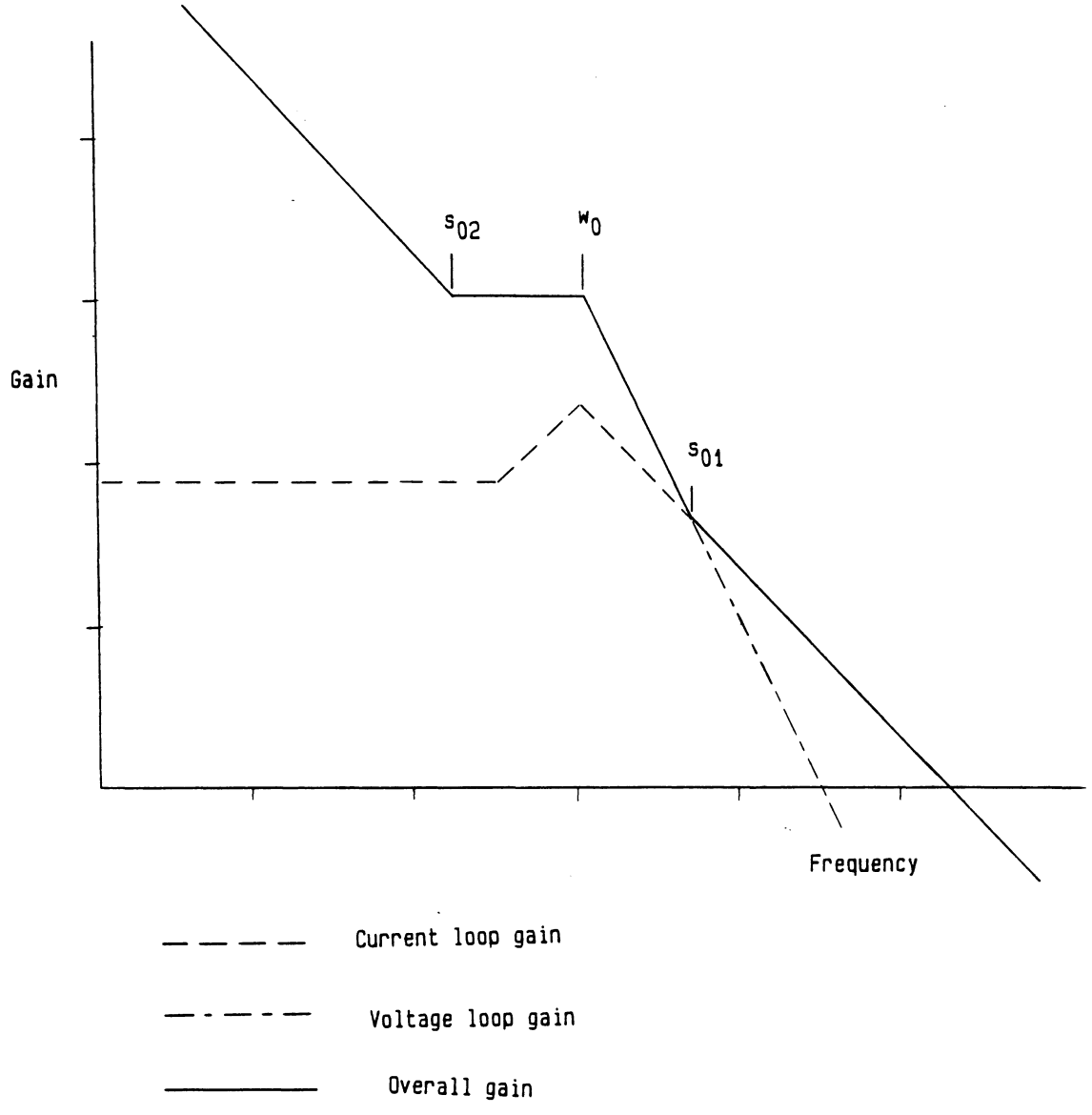


Figure 6.4 : Open Loop Gain (T_1) Asymptotes Showing Relationships between Current Loop Gain, Voltage Loop Gain, Overall Loop Gain and the Zeros s_{01} and s_{02}.

In order to prevent peaking of the output impedance and audiosusceptibility constraint at high frequency, the upper limit on s_{01} is:

$$s_{01} < \frac{1}{\omega_0 \tau_{z1}} \tag{6.12}$$

A second restriction on the upper limit of s_{01} must be applied for the boost and the buck/boost converter. The value of this zero must be significantly less than the right-hand plane zero of the power stage.

$$s_{01} << \frac{R_L}{\omega_0 L_e} \qquad \text{Boost} \tag{6.13}$$

$$s_{01} << \frac{R_L}{\omega_0 D L_e} \qquad \text{Buck/Boost} \tag{6.14}$$

As a general guideline, s_{01} should be less than half of the value of the right hand plane zero.

Audiosusceptibility Specification

The required input-output attenuation is K_a. Since the input signal is also attenuated by the turns ratio n_p/n_s, we define audiosusceptibility K_a' as:

$$K_a' = K_a \, n_p/n_s \qquad \text{without an input filter.} \tag{6.15}$$

$$K_a' = K_a \left[1 - \frac{B_r}{\mu^2 R_L} \right] \frac{n_p/n_s}{B_f} \quad \text{with an input filter.} \qquad (6.16)$$

To meet the design specifications, the minimum value of s_{01} is:

$$s_{01} > \frac{K_3 \omega_0}{K_a' - K_3 A_2} \qquad \text{where } K_3 = \frac{K_2}{K_1 A_1} \qquad (6.17)$$

The minimum value of s_{01} is not allowed to exceed the maximum value defined previously. If this happens, the audiosusceptibility constraint cannot be met, and it must be revised.

Output Impedance Specification

The specified maximum output impedance is K_o. The minimum value of s_{01} required to achieve this value is:

$$s_{01} > \frac{\omega_0 L_e/A_1}{K_o - L_e A_2/A_1} \qquad (6.18)$$

Output peaking Specification

K_{op} is the specified maximum change in output voltage for a given step output current. The minimum value of s_{01} required to achieve this is:

$$s_{01} > \frac{\omega_0 L_e/A_1 R_L}{K_{op} - L_e A_2/A_1 R_L} \qquad (6.19)$$

Settling Time Constraint

The specified output settling time is τ_s for an input or output perturbation response. The settling time is determined by the value of s_{02}. The minimum value of s_{02} required to achieve the specification is:

$$s_{02} > \frac{1}{\omega_0 \tau_s} \tag{6.20}$$

Note: settling time cannot be specified to be less than the time constant of the filter.

Range of Design Parameters τ_{z2}' and α'

The range of the zero s_{02} is determined by the settling time constraint. A value of s_{02} towards the low end of the allowable range is selected, and τ_{z2}' is then given by:

$$\tau_{z2}' = \frac{1}{\omega_0 s_{02}} \tag{6.21}$$

The range of s_{01} is given by the audiosusceptibility, output impedance and output peaking constraints, and by the upper bound constraint for no high frequency peaking and right-hand plane zero.

The variables α', τ_{z2}' and s_{02} are related by:

$$s_{01} = \alpha' \omega_0 \tau_{z2}' \tag{6.22}$$

The range for α' is then given by:

$$\frac{s_{01min}}{\omega_0 \tau_{z2}'} > \alpha' > \frac{s_{01max}}{\omega_0 \tau_{z2}'} \tag{6.23}$$

Standardized curves for values of τ_{z2}' and α' are given in Appendix D. The gain of the curves is normalized by:

$$\frac{K_1 \alpha}{\omega_0 \alpha'} \tag{6.24}$$

The frequency scale is normalized to ω_0. A desired curve is now selected from the family of curves for the chosen τ_{z2}'.

7) Voltage Loop Component Design

The optimum values of α' and τ_{z2}' have been selected. The corresponding values of variables α and τ_{z2} are related by:

$$\tau_{z2} = \tau_{z2}' \tag{6.25}$$

$$\alpha = \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}'} \tag{6.26}$$

The voltage loop control components can now be found from the following equations:

$$C_1 R_y = \frac{\tau_m}{\alpha} \qquad \text{Buck} \tag{6.27}$$

$$C_1 R_y = \frac{\tau_m}{D' \alpha} \qquad \text{Boost, Buck/boost} \tag{6.28}$$

$$C_2 = (\tau_{z2} - \tau_{z1})/R_y \tag{6.29}$$

$$R_5 = \tau_{z1}/C_2 \tag{6.30}$$

There are four unknowns in three equations. Capacitor C_1 can be picked arbitrarily, and the values of the other components are then fixed by the above equations.

8) Current Loop Component Design

For SCM, the component values are related by:

$$\tau_m = \frac{R_4 C_1}{n} \tag{6.31}$$

If resistor R_6 is used, for best results, it is chosen by:

$$\frac{\omega_0 s_{01}}{5} < \frac{1}{C_1 R_6} < \frac{\omega_0 s_{01}}{3} \tag{6.32}$$

For CIC, the components are related by:

$$\tau_m = \frac{n_c L}{R_w} n_p/n_s \tag{6.33}$$

For combined SCM/CIC:

$$\tau_{scm} = \frac{R_4 C_1}{n} \tag{6.34}$$

$$\tau_{cic} = \frac{n_c L}{R_w} n_p/n_s \qquad (6.35)$$

6.7 Conclusions

Design procedures have been developed for the control components of a SCM, CIC or combined SCM/CIC of single or multiple power modules. The design procedure assumes a fixed control-compensation network which has been shown to be adequate for concurrently satisfying design specifications of output impedance, audiosusceptibility, transient response and stability margin. The step-by-step design procedure clearly defines the necessary components required for a good design, yet allows the designer the freedom of trading off several design characteristics when choosing the parameter α' to select the desired stability margin.

These design procedures have been developed with the ultimate goal of automating the calculations on a small computer, enabling the designer to rapidly design the control system of a given power converter and realize the limits of a given power stage. When the system is automated, more extensive curves of loop gains and other small-signal performances may be plotted by the computer and used to select the optimum design parameters.

Examples of how to use the design procedures are given in Chapter 8 with the resulting small-signal performance simulations. Examples are presented for single and multiple converters controlled with SCM, CIC and SCM/CIC, showing that the small-signal performance may indeed

be identical for different control schemes and for power stages constructed from multiple modules.

Chapter 7

Secondary Output Filter

Today's switching power supplies for computer systems frequently have very high output-current requirements together with very low output ripple and noise specifications. The corresponding high amplitude pulsating current waveforms in the circuit produce stray magnetic fields which couple into the output voltage bus. The main power inductor is designed primarily for filtering of the switching frequency ripple, and, since the high frequency noise may be at 10 Mhz or higher, it is difficult to remove with a single stage filter. In many designs, therefore, it is necessary to add a second-order LC filter at the output of the power supply. Since this filter often has its resonant frequency well below the switching frequency of the power supply, it can drastically affect the control loop stability, especially for single-loop feedback systems.

The second output filter is often designed with little or no analysis - a typical design approach is to split the output capacitor in two and place a toroid on the bus bar between the capacitors to provide the second stage filter. Alternatively, cabling inductance and parasitic load capacitance are used to build the second filter stage. The purpose of this chapter is to analyze the characteristics of the second stage filter for the buck converter and to produce basic guidelines for the design of an effective noise filter. Also, it will be shown that SCM or CIC are sufficient to stabilize the system if the second filter is properly designed, providing all of the stable, high performance characteristics of the power supply without the second filter.

7.1 Secondary Filter Circuit

The equivalent circuit of a buck converter with a secondary output filter is shown in Figure 7.1. The secondary inductance may consist of an internal element to the supply, cabling to the load or some kind of common-mode toroid. It is apparent that this circuit is a fourth-order system and the control-to-output-voltage transfer function may have up to 360 degrees phase delay, presenting a formidable problem to the control system designer. However, if the following criteria are satisfied for the system, SCM or CIC may be effectively used to stabilize the system:

- The duty-cycle-to-inductor-current transfer function (Current Loop) retains essentially the same form as for the single filter power supply; that is, approximately a first-order transfer function with the single pole characteristic after the power supply resonant frequency.

- The poles and zeros of the second output filter do not significantly change the gain and phase characteristics of the duty-cycle-to-output-voltage gain until after the current loop becomes dominant. (Beyond s_{01} in SCM design terms.)

- The secondary output filter is sufficiently damped so that the voltage-loop transfer function does not peak to a value close to the current loop.

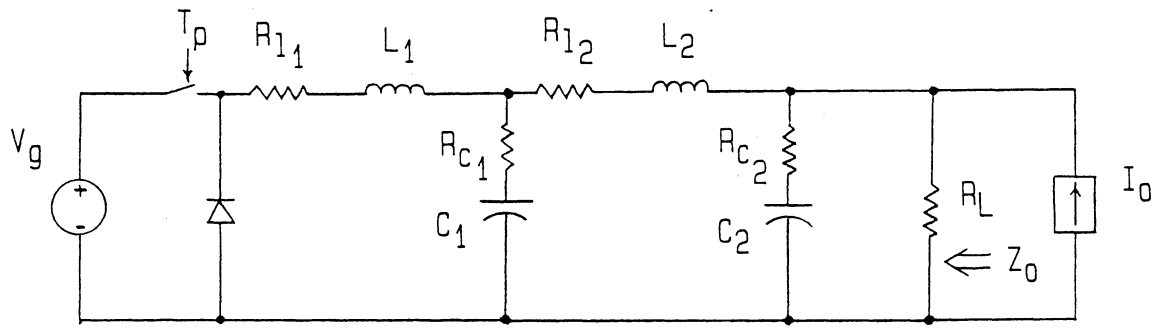


Figure 7.1: Buck Converter Circuit with Secondary LC Output Filter.

To show that these criteria can be met for a well-designed filter, the circuit of Figure 7.1 must be analyzed in detail.

7.2 Secondary Filter Analysis

The averaged, state-space equations for the circuit of Figure 7.1 are as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ v_{C_1} \\ i_{L_2} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} \frac{-R_{c1}}{L_1} & \frac{-1}{L_1} & \frac{R_{c1}}{L_1} & 0 \\ \frac{1}{C_1} & 0 & \frac{-1}{C_1} & 0 \\ \frac{R_{c1}}{L_2} & \frac{1}{L_2} & \frac{-(R_{c1}+R_{c2})}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{C_2 R_L} \end{bmatrix} x + \begin{bmatrix} \frac{V_g}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} d$$

$$\dot{x} = A\,x + B\,d$$

The duty-cycle-to-inductor-current transfer function is given by:

$$\frac{i_{L_1}(s)}{d(s)} = [1 \quad 0 \quad 0 \quad 0]\,(sI-A)^{-1}B$$

and the duty-cycle-to-output-voltage transfer function by:

$$\frac{v_o(s)}{d(s)} = [0 \quad 0 \quad R_{c2} \quad 1]\,(sI - A)^{-1}B$$

It should be noted that the parasitic resistance of the inductors is assumed to be zero. Since these resistances are usually an order of magnitude less than the equivalent series resistance of the output capacitors, the effect of this omission is negligible. Before the above

expressions are evaluated, one assumption is made about the circuit design: the main filter inductor L_1 should be considerably larger than the secondary inductor, L_2. This is certainly a reasonable restriction since L_1 is designed for switching frequency attenuation and L_2 is either a parasitic inductance or designed for high frequency noise attenuation. Without this assumption, the analysis becomes intractable. The usual assumption for switching regulators, that R_{c1} and R_{c2} are much smaller than R_L, is also made.

The duty-cycle-to-inductor-current transfer function is:

$$\frac{i_{L_1}(s)}{d(s)} = V_g \frac{\left(s^3 + s^2\left[\frac{R_e}{L_2} + \frac{1}{C_2R_L}\right] + s\left[\frac{1}{L_2C_2} + \frac{1}{L_2C_1}\right] + \frac{1}{L_2C_1C_2R_L}\right)}{D(s)} \quad (7.1)$$

where the denominator is given by:

$$D(s) = s^4 + s^3\left[\frac{R_e}{L_2} + \frac{1}{C_2R_L}\right] + s^2\left[\frac{R_{c1}R_{c1}}{L_1L_2} + \frac{1}{L_2C_1} + \frac{1}{L_2C_2}\right]$$

$$+ s\left[\frac{R_{c1}}{L_1L_2C_2} + \frac{R_{c2}}{L_1L_2C_1} + \frac{1}{L_2C_1C_2R_L}\right] + \frac{1}{L_1L_2C_1C_2} \quad (7.2)$$

The duty-cycle-to-output-voltage is given by:

$$\frac{V_o(s)}{d(s)} = V_g \frac{\left(\frac{R_{c1}R_{c2}}{L_1L_2}s^2 + s\left[\frac{1}{C_1R_{c1}} + \frac{1}{C_2R_{c2}}\right] + \frac{1}{C_1R_{c1}C_2R_{c2}}\right)}{D(s)} \quad (7.3)$$

To gain some insight to these expressions, it is instructive to first examine the determinant of (sI-A). The parasitic resistances R_{c1} and R_{c2},

and the load resistance R_L serve to damp the circuit, but will not significantly affect the resonant frequencies of the output filter. In order to determine these resonant frequencies, the determinant is evaluated with $R_{c1} = R_{c2} = 0$ and $R_L = \infty$. Then, again assuming $L_1 >> L_2$,

$$D(s) = s^4 + s^2\left[\frac{1}{L_2C_1} + \frac{1}{L_2C_2}\right] + \frac{1}{L_1L_2C_1C_2}$$

$$= \left[s^2 + \frac{1}{L_1(C_1+C_2)}\right]\left[s^2 + \frac{1}{L_2C_1} + \frac{1}{L_2C_2}\right] \qquad (7.4)$$

This shows immediately the resonant frequencies of the circuit. The low frequency resonance, ω1, and the high frequency resonance, ω2, are given by:

$$\omega_1 = \frac{1}{\sqrt{L_1(C_1+C_2)}} \qquad \omega_2 = \frac{1}{\sqrt{L_2C_s}} \qquad (7.5)$$

where C_s is the series combination of C_1 and C_2.

As stated before, L_1 is considerably larger than L_2, and for most practical designs, 'considerably larger' means about 10 times larger. For a stable control loop design, the second filter resonance must occur at a frequency well beyond the point where the current loop is dominant. This occurs at a frequency somewhat above the first resonance. (Denoted by s_{01} in SCM design terms.) For a good system design, therefore, ω2 >> ω1. This can be achieved by separation of the capacitor values.

The transfer functions of Equations 7.1 and 7.3 will, therefore, be analyzed for the conditions where $C_1 >> C_2$, or for $C_2 >> C_1$. For each of these two conditions, it will be possible to factor the transfer

functions and separate the effect of the two filter resonant frequencies. Design rules can then be established for either of these two cases. If neither of these inequalities is satisfied, a reasonable factorization cannot be achieved. However, it is apparent that the resonant frequencies will still be approximated by the equations of (7.5), and the damping of the two filter resonances will lie somewhere between the case for $C_1 >> C_2$ and for $C_2 >> C_1$. In most cases, the condition that one of the capacitors is larger than the other can usually be achieved. The problem of how to select capacitors C_1 and C_2 for designs where the values can be controlled will be presented later in this chapter.

7.3.1 Duty-Cycle-to-Inductor-Current Transfer Function for $C_1 >> C_2$

If $C_1 >> C_2$, the denominator of the transfer functions for the voltage and current gains is approximated by:

$$D(s) = s^4 + s^3\left[\frac{R_e}{L_2} + \frac{1}{C_2R_L}\right] + s^2\left[\frac{R_{c1}R_{c2}}{L_1L_2} + \frac{1}{L_2C_2}\right]$$

$$+ s\left[\frac{R_{c1}}{L_1L_2C_2} + \frac{1}{L_2C_1C_2R_L}\right] + \frac{1}{L_1L_2C_1C_2} \quad (7.6)$$

This expression may be approximately factored by:

$$D(s)= \left(s^2+ s\left[\frac{R_{c1}}{L_2} + \frac{1}{C_1R_L}\right]+ \frac{1}{L_1C_1}\right)\left(s^2+ s\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2R_L}\right]+ \frac{1}{L_2C_2}\right) \quad (7.7)$$

The expansion of the above expression will give a small discrepancy in the s^2 term of D(s). This discrepancy will be very small for most

practical designs, and for all designs, will not significantly affect the expression for frequencies well above the first resonance. Since the primary importance of this factorization will be in determining the peaking of the voltage loop at the second resonant frequency, the discrepancy is irrelevant.

The duty-cycle-to-inductor-current transfer function when $C_1 >> C_2$ is given by:

$$\frac{i_L(s)}{d(s)} = \frac{s^3 + s^2\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2R_L}\right] + s\frac{1}{L_2C_2} + \frac{1}{L_2C_1C_2R_L}}{D(s)} \qquad (7.8)$$

This expression can also be factored, with similar arguments to that of the denominator factorization to give:

$$\frac{i_{L_1}(s)}{d(s)} = \frac{\frac{V_g}{L_1}\left(s + \frac{1}{C_1R_L}\right)\left(s^2 + s\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2R_L}\right] + \frac{1}{L_2C_2}\right)}{D(s)} \qquad (7.9)$$

Cancellation of numerator and denominator terms gives:

$$\frac{i_{L_1}(s)}{d(s)} = \frac{V_g}{L_1}\frac{\left(s + \frac{1}{C_1R_L}\right)}{\left(s^2 + s\left[\frac{R_{c1}}{L_2} + \frac{1}{C_1R_L}\right] + \frac{1}{L_1C_1}\right)} \qquad (7.10)$$

In cancelling the corresponding parts of the numerator and denominator, as above, the effects of the approximations in factoring the numerator and denominator are also cancelled.

Expression (7.10) for the current-loop gain is now equal to the expression for the current-loop gain for a buck converter with a single

output filter consisting of inductor value L_1 and capacitor value C_1. Hence, the first condition for a stable feedback loop is indeed met for the case when $C_1 >> C_2$; the control-to-inductor-current transfer function has retained its form with the addition of the second stage filter, and is actually independent of the second stage filter parameters.

7.3.2 Duty-Cycle-to-Output-Voltage Transfer Function for $C_1 >> C_2$

The voltage-loop transfer function in Equation (7.3) can be factored to give:

$$\frac{V_o(s)}{d(s)} = \frac{V_g \frac{R_{c1}R_{c2}}{L_1L_2}\left(s + \frac{1}{C_1R_{c1}}\right)\left(s + \frac{1}{C_2R_{c2}}\right)}{D(s)} \qquad (7.11)$$

$$= \frac{V_g R_{c1}\left(s + \frac{1}{C_1R_{c1}}\right) R_{c2}\left(s + \frac{1}{C_2R_{c2}}\right)}{L_1\left(s^2 + s\left[\frac{R_{c1}}{L_1} + \frac{1}{C_1R_L}\right] + \frac{1}{L_1C_1}\right) L_2\left(s^2 + s\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2R_L}\right] + \frac{1}{L_2C_2}\right)}$$

Notice that the first part of the transfer function is equal to the transfer function for the voltage gain of a buck power stage with just a single stage filter. The effects of the second order filter are shown by the second part of the expression. Since the numerator contains just a single-order zero, the peaking of this transfer function is given by the quality factor of the denominator expression of the second part of Equation 7.11. It can be seen that the peaking of the second filter is determined by:

$$Q = \frac{\omega_2}{\left(\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2 R_L}\right)} \qquad \text{where } \omega_2 = \frac{1}{\sqrt{L_2 C_2}} \tag{7.12}$$

If the second output filter is designed so that Equation 7.12 gives a value of Q to be one or less, the third condition for a stable control loop design is satisfied. It will be shown in the design examples of Chapter 8 that the second output filter will be well damped due to the ESR of the capacitors and the above requirement on Q will not severely limit the design of the second stage output filter.

For the case where $C_1 >> C_2$, therefore, it is demonstrated that the control loop is not significantly affected if the second stage output filter is properly designed and damped.The second design case for $C_2 >> C_1$ will now be considered.

7.3.3 Duty-Cycle-to-Inductor-Current Transfer Function for $C_2 >> C_1$

If $C_2 >> C_1$, the denominator of the transfer functions for the voltage and current gains is approximated by:

$$D(s) = s^4 + s^3\left[\frac{R_{c1}+R_{c2}}{L_1} + \frac{1}{C_2R_L}\right] + s^2\left[\frac{R_{c1}R_{c2}}{L_1L_2} + \frac{1}{L_2C_1}\right]$$

$$+ s\left[\frac{R_{c1}}{L_1L_2C_1} + \frac{1}{L_2C_1C_2R_L}\right] + \frac{1}{L_1L_2C_1C_2}$$

This expression may be approximately factored by:

$$D(s) = \left(s^2 + s\left[\frac{R_{c2}}{L_1} + \frac{1}{C_2R_L}\right] + \frac{1}{L_1C_2}\right)\left(s^2 + s\,\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{L_2C_1}\right) \quad (7.13)$$

As in the previous case, the expansion of this expression will give a small discrepancy in the s^2 term of D(s).

The duty-cycle-to-inductor-current transfer function when $C_2 >> C_1$ is given by:

$$\frac{i_{L_1}(s)}{d(s)} = \frac{s^3 + s^2\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2R_L}\right] + s\,\frac{1}{L_2C_1} + \frac{1}{L_2C_1C_2R_L}}{D(s)}$$

This expression can also be approximately factored to give:

$$\frac{i_{L_1}(s)}{d(s)} = \frac{\frac{V_g}{L_1}\left(s + \frac{1}{C_2R_L}\right)\left(s^2 + s\,\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{L_2C_1}\right)}{D(s)}$$

$$= \frac{\frac{V_g}{L_1}\left(s + \frac{1}{C_2R_L}\right)}{\left(s^2 + s\left[\frac{R_{c1}}{L_1} + \frac{1}{C_2R_L}\right] + \frac{1}{L_1C_2}\right)} \quad (7.14)$$

Expression 7.14 for the current-loop gain is again equal to the expression for the current-loop gain for a buck converter, this time with a single output filter consisting of inductor value L_1 and capacitor value C_2. Hence, the first condition for a stable feedback loop is also met for the case when $C_2 >> C_1$ and the current gain is not affected by the second stage output filter.

7.3.4 Duty-Cycle-to-Output-Voltage Transfer Function for $C_2 >> C_1$

The voltage-loop transfer function can be factored to give:

$$\frac{V_o(s)}{d(s)} = \frac{V_g \frac{R_{c1}R_{c2}}{L_1L_2}\left(s + \frac{1}{C_1R_{c1}}\right)\left(s + \frac{1}{C_2R_{c2}}\right)}{D(s)}$$

$$= \frac{V_g \frac{R_{c1}}{L_1}\left(s + \frac{1}{C_2R_{c2}}\right) \frac{R_{c2}}{L_2}\left(s + \frac{1}{C_2R_{c2}}\right)}{\left(s^2 + s\left[\frac{R_{c1}}{L_1} + \frac{1}{C_2R_L}\right] + \frac{1}{L_1C_2}\right)\left(s^2 + s\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{L_2C_1}\right)} \quad (7.15)$$

Notice that the first part of the transfer function is again equal to the transfer function for the voltage gain of a buck power stage with just a single stage filter consisting of L_1 and C_2. The effects of the second-order filter (L_2 and C_1 inserted between the main power filter), are shown by the second part of the expression. Since the numerator contains just a single-order zero, the peaking of this transfer function is given by the quality factor of the denominator expression of the second part of Equation 7.15. It can be seen that the peaking of the second filter is determined for the case where $C_2 >> C_1$ by:

$$Q = \frac{\omega_2 L_2}{R_{c1}+R_{c2}} \qquad \text{where } \omega_2 = \frac{1}{\sqrt{L_2 C_1}} \tag{7.16}$$

In the case where $C_2 >> C_1$, the secondary resonance is less damped than for the case where $C_1 >> C_2$. However, if the second filter is again designed to give a Q of less than one, the system will retain all of its stable properties.

7.4 Output Impedance Peaking Due to Secondary Filter

It has been shown so far that the control loop with a secondary filter will not be significantly affected when the filter is properly designed, and the restriction on the Q of the second filter for control loop purposes also will prevent peaking of the audiosusceptibility of the regulator. The only small-signal effect that remains to be analyzed with a second-order filter is that of the output impedance.

It has been shown that the first resonance occurs at the frequency determined by inductor L_1 and the parallel combination of capacitors C_1 and C_2. The second resonance occurs at a frequency determined by inductor L_2 and the series combination of the capacitors. Since any peaking of the output impedance due to the second filter will occur at the second resonant frequency and L_1 is in parallel with C_1 for output impedance analysis, the impedance of C_1 will be much less than that of L_1 and the first inductor may be omitted from the circuit. The expressions for the output impedance will then be only third only for the high-frequency peaking effect.

Referring to the circuit diagram of Figure 7.1, the output impedance can be found from:

$$\frac{d}{dt}\begin{bmatrix} v_{C_1} \\ i_{L_2} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{C_1} & 0 \\ \frac{1}{L_2} & \frac{-(R_{c1}+R_{c2})}{L_2} & \frac{-1}{L_2} \\ 0 & \frac{-1}{C_2} & \frac{1}{C_2 R_L} \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{C_2} \end{bmatrix} I_o$$

$$\dot{x} = A \quad x + B \quad I_o$$

Then the output impedance, $Z_o(s)$, is given by:

$$Z_o(s) = [0 \quad R_{c2} \quad 1] \; (sI-A)^{-1}B + R_{c2}$$

$$= \frac{R_{c2}\left(s^3 + s^2\left[\frac{1}{C_2 R_{c2}} + \frac{R_{c1}+R_{c2}}{L_2}\right] + s\left[\frac{R_{c1}}{L_2 C_2 R_{c2}} + \frac{1}{L_2 C_2} + \frac{1}{L_2 C_1}\right] + \frac{1}{L_2 C_1 C_2 R_c}\right)}{s^3 + s^2\left[\frac{1}{C_2 R_L} + \frac{R_{c1}+R_{c2}}{L_2}\right] + s\left[\frac{1}{L_2 C_2} + \frac{1}{L_2 C_1}\right] + \frac{1}{L_2 C_1 C_2 R_L}} \quad (7.17)$$

When $C_1 >> C_2$, this expression may be approximately factored:

$$Z_o(s) = \frac{R_{c2}\left(s + \frac{1}{C_1 R_{c2}}\right)\left(s^2 + s\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2 R_{c2}}\right] + \frac{1}{L_2 C_2}\right)}{\left(s + \frac{1}{C_1 R_L}\right)\left(s^2 + s\left[\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{C_2 R_L}\right] + \frac{1}{L_2 C_2}\right)} \quad (7.18)$$

And for the case where $C_2 >> C_1$, Equation 7.18 may be approximately factored to give:

$$Z_o(s) = R_{c2}\frac{\left(s + \frac{1}{C_2 R_{c2}}\right)\left(s^2 + s\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{L_2 C_2}\right)}{\left(s + \frac{1}{C_1 R_L}\right)\left(s^2 + s\frac{R_{c1}+R_{c2}}{L_2} + \frac{1}{L_2 C_2}\right)}$$

$$= R_{c2} \frac{\left(s + \frac{1}{C_2 R_{c2}}\right)}{\left(s + \frac{1}{C_1 R_L}\right)} \qquad (7.19)$$

It can be seen from Equation 7.19, for $C_2 >> C_1$, cancellation of the numerator and denominator occurs, and there is no output impedance peaking due to the second-order filter. However, for the case where $C_1 >> C_2$, this cancellation is not possible, and a peaking will occur due to the higher damping term in the numerator of the second-order part of Equation 7.17. At the second resonant frequency, the peaking of the output impedance is given by:

$C_2 >> C_1$ No output impedance peaking

$$C_1 >> C_2 \quad Z_o(s)max = \frac{R_{c2}[(R_{c1}+R_{c2})/L_2 + 1/C_2 R_c]}{[(R_{c1}+R_{c2})/L_2 + 1/C_2 R_L]}$$

7.5 Further Secondary Filter Design Considerations

It has been shown in the foregoing analysis that it is preferable to design a secondary output filter with the larger capacitor located at the output of the supply. This will prevent any peaking of the output impedance characteristic at the higher resonant frequency. It is also important that C_2 be the larger capacitor for another reason: the second resonant frequency must be maintained at a value well above the point where the current loop is dominant. This second resonance is a sensitive function of the smaller capacitor and a far less sensitive function of

the larger capacitor. If the second capacitance is made to be the smaller one, the second resonance will be sensitive to any load capacitance variations.

If the second capacitor is made large, however, not only will the power supply be insensitive to changes of the second resonant frequency, but the control-loop adaptive effect will compensate for the load capacitor changes. If possible, therefore, capacitor C_2 should be made larger than C_1.

In some cases, the second output filter is constructed of cabling impedance and load board capacitance. In this case, the design approach should be to either limit the amount of load capacitance and make C_1 the larger capacitor or to make C_1 small and place a large capacitance at the load. This may be contrary to conventional design approaches to this problem, but it will produce the best results.

With these and other design considerations in mind, some design guidelines can now be given for the second-order filter.

7.5 Secondary Filter Design Guidelines

1) Design the main power inductor and larger capacitor value as for a single output filter.

2) Design the SCM or CIC loop as for a single output filter power supply. To allow the greatest freedom of choice of the secondary filter, choose the value of s_{01} towards the lower end of the range.

3) The second output filter inductor should be bounded by the inequality $L_2 << L_1$. The value of L_2 should not exceed about one-tenth of the value of L_1.

4) Determine the value of the smaller capacitor to give a resonant frequency which is greater than s_{01}. (At least three times greater, as a rule of thumb). This is an absolute upper bound on the smaller capacitor value and should not be exceeded if stability is to be maintained. This is especially important to remember when the smaller capacitor has to be C_2.

5) Within the above constraints, design the second output filter to give the desired noise attenuation.

6) For the chosen values of the smaller capacitor and L_2, check the equations for the damping of the second filter resonance to make sure the Q does not exceed one. If it does exceed one, some noise attenuation may have to be compromised to maintain stability.

7) If C_2 is the smaller capacitor, check the equation for output impedance peaking to make sure that this will not seriously degrade the performance of the power supply. If C_1 is the smaller, there will be no output impedance peaking.

7.7 Conclusions

It has been shown in this chapter that a properly designed second output filter will not affect the stability of the SCM or CIC loop. This is true because the ac loop gain of the converter is independent of any second output filter parameters, and the dc loop gain is affected only after the ac loop gain has become dominant.

The second output filter resonance must be damped to give a low Q (assuming that the resonance is below the switching frequency). It will be shown in one of the design examples that the second filter will be damped sufficiently by the ESR of the capacitors in most practical applications, and it will not be necessary to add external damping resistance or to compromise the filter design to meet this requirement.

If possible, the second capacitor, C_2, should be chosen as the larger capacitor, since there will be no peaking of the output impedance for this case. If C_1 is larger, the output impedance peaking may be quite severe. Also, the second resonance will be independent of load capacitance changes.

The second resonance is more damped for the case when C_1 is the larger capacitor. If the values of capacitance are close together, the damping term for $C_2 >> C_1$ should be used to produce a more conservative design.

Chapter 8

Design Examples

The following design examples illustrate the use of the design procedures developed in Chapter 6. The first example is a single buck module using CIC to achieve the given design specifications of stability, output impedance, audiosusceptibility and settling time. This example demonstrates the extension of the SCM design procedure developed to cover CIC, and shows how the external ramp should be chosen.

The second example uses SCM on the same power stage as example 1. For the case where no resistor is placed across the current loop integrator, it is shown that the small-signal performances of SCM and CIC are identical. The effect of the addition of the resistor and the placement of the pole of the subsequent pole-zero pair are demonstrated in this example.

Example 3 illustrates how the same power stage may be constructed from three parallel modules and controlled with CIC to obtain the same small-signal performance as for the single module case. This shows that all of the advantages of modularity may be achieved without compromising the small-signal performance.

The fourth example uses a combination SCM/CIC scheme to control the same three modules as Example 3. This demonstrates how the noise performance of the system can be reduced with the addition of the SCM loop. Although the control circuit now has more degrees of freedom, the design procedure remains extremely straightforward.

The final example is a different power stage, constructed of five modules in parallel, with a combination SCM/CIC scheme. A second LC filter

is added to the output of the supply to show how this should be designed to achieve the maximum additional noise attenuation without compromising any of the small-signal characteristics.

8.1 Design Example 1 - Buck Converter, Single Module

Power Stage Parameters

$L = 1.7\ \mu H$	$V_s = 300\ v$	$V_g = 15\ v$
$C = 14000\ \mu F$	$V_o = 3.6\ v$	
$R_c = 2\ mOhm$	$T_p = 28\ \mu s$	
$R_L = 18\ mOhm$	$n_p/n_s = 20$	
$D = 0.30$ (measured)		

1) Use CIC.

2) Select desired ramp amplitude, $V_p = 0.75\ v$. From Equation 6.1,

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} = 1.4 \times 10^{-4}$$

3) Design external ramp for minimum input voltage.

$V_{gmin} = 10\ v$ (200v source) $D = 0.41$

From Equation 6.9,

$$S_e = V_g(D-0.182)/\tau_m = 1.8 \times 10^4$$

4) Evaluate buck parameters.

$L_e = L/k = 1.7\ \mu H$

$\omega_0 = 1/\sqrt{L_e C} = 6500$ rad/s

$\tau_{z1} = CR_c = 2.8 \times 10^{-5}$

$A_1 = 1$

$A_2 = 0$

$M = V_g(1-2D)T_p + 2S_e T_p \tau_m = 3 \times 10^{-4}$

$K_1 = 2V_g / M = 10^5$

$K_2 = D = 0.3$

5) No input filter.

6) Design specifications:

Transient response settling time	$\tau_s = 0.5$ ms
Output impedance < 15 mOhm	$K_o = 0.015$
Output peaking 3% for 10% step load	$K_{op} = 0.3$
Audiosusceptibility (30v input step causes 10 mV output disturbance.)	$K_a = 3.33 \times 10^{-4}$

Upper limit on s_{01}, from Equation 6.12

$$s_{01} < \frac{1}{\omega_0 \tau_{z1}} \qquad s_{01} < 5.6$$

Audiosusceptibility, from Equation 6.17:

$$K_a' = K_a n_p/n_s = 6.7 \times 10^{-3}$$

$$s_{01} > \frac{K_3\ \omega_0}{K_a' - K_3 A_2} = 3 \qquad s_{01} > 3$$

Output impedance, from Equation 6.18:

$$s_{01} > \frac{\omega_0\ L_e/A_1}{K_o - L_e\ A_2/A_1} = 0.74 \qquad s_{01} > 0.74$$

Output peaking, from Equation 6.19:

$$s_{01} > \frac{\omega_0\ L_e/A_1\ R_L}{K_{op} - L_e\ A_2/A_1\ R_L} = 0.2 \qquad s_{01} > 0.2$$

Settling time, from Equation 6.20:

$$s_{02} > \frac{1}{\omega_0\ \tau_s} = 0.3 \qquad s_{02} > 0.3$$

Choose value of s_{02}:

$$0.3 < s_{02} < 1$$

Select value of s_{02} towards low end of range:

$$s_{02} = 0.4$$

Then, from Equation 6.21:

$$\tau_{z2}' = \frac{1}{\omega_0 s_{02}} = 3.8 \times 10^{-4} \quad \text{and} \quad \omega_0 \tau_{z2}' = 2.5$$

Range of α', from Equation 6.23:

$$\frac{s_{01min}}{\omega_0 \tau_{z2}'} > \alpha' > \frac{s_{01max}}{\omega_0 \tau_{z2}'} \qquad 1.2 < \alpha' < 2.25$$

Use curves from Appendix D to select the value of α'. The curve with the closest value to the selected $\omega_0\tau_{z2}'$ is used to select the value of α', in this case, the curve for $\omega_0\tau_{z2}' = 3$ is used. The gain of the curves are normalized to $20\log(K_1/\omega_0) = 23.8$ dB. Picking $\alpha' = 2$ gives a cross-over frequency of $15\omega_0 = 15.5$ kHz and a phase margin of 70 degrees.

7) Design voltage-loop components.

$$\tau_{z2} = \tau_{z2}'$$

$$\alpha = \frac{A_1\alpha'}{1 + A_2\alpha'\tau_{z2}'}$$

$$C_1R_y = \frac{\tau_m}{\alpha} = 0.65 \times 10^{-4}$$

C_1 may be selected arbitrarily.

$C_1 = 0.01$ µF

$R_y = 6.5$k

Other components are then constrained by the following equations:

$$C_2 = (\tau_{z2} - \tau_{z1})/R_y = 0.06 \text{ µF}$$

$$R_5 = \tau_{z1}/C_2 = 470 \text{ ohm}$$

8) Design current-loop components. From Equation 6.33

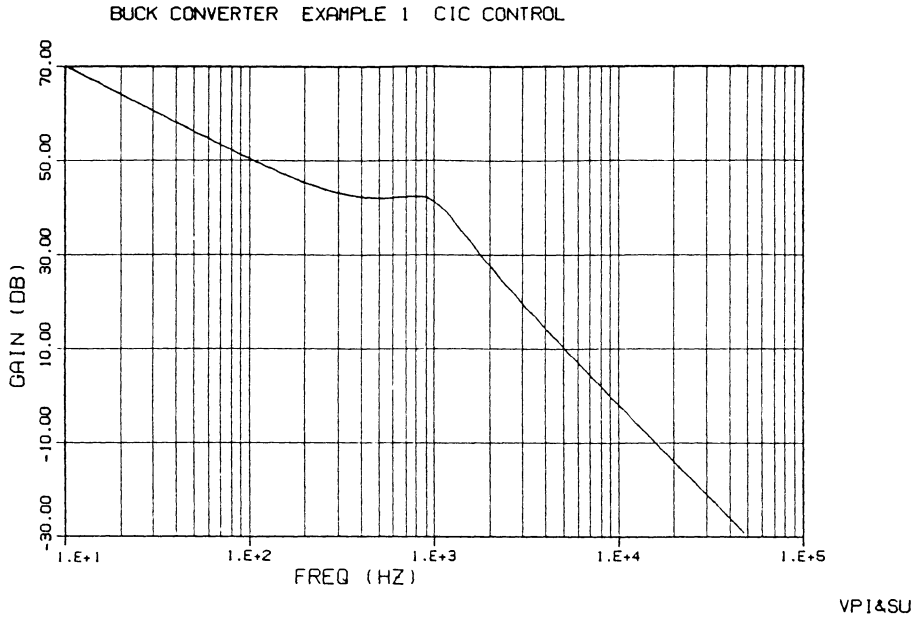
$$\tau_m = \frac{n_c L}{R_w} n_p/n_s$$

Number of turns of current transformer may be selected arbitrarily. Sense resistor is then constrained.

$n_c = 200$

$R_w = 51$ ohm

The design of the control system is now complete. Using these calculated values, the small-signal characteristics were simulated with the computer model described in Appendix C. The results for loop gain, output impedance and audiosusceptibility are shown in Figures 8.1 through 8.5. It can be seen from these curves that all of the design objectives have been met or surpassed. The design objective of settling time can be verified from a large-signal simulation. The maximum value of the output impedance characteristic guarantees that the step-load peaking specification is satisfied.



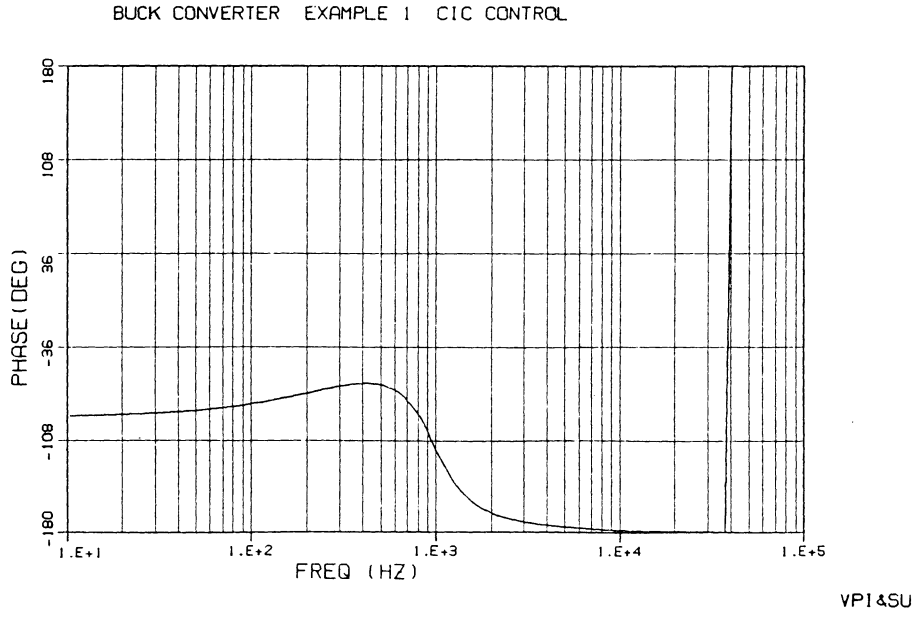
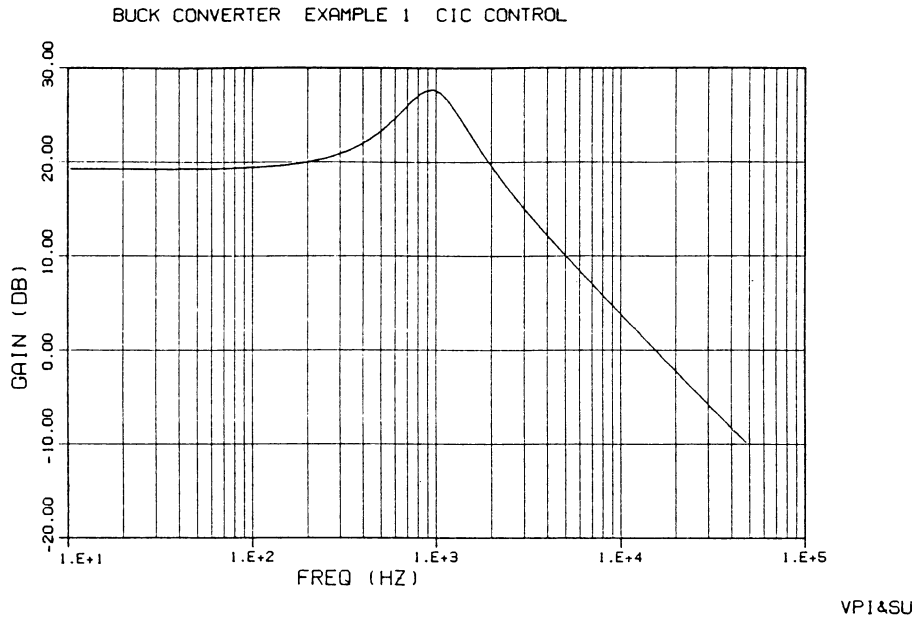


Figure 8.1: Design Example 1 - Single Module Buck Converter with CIC Control. Voltage Loop Gain, T_v.



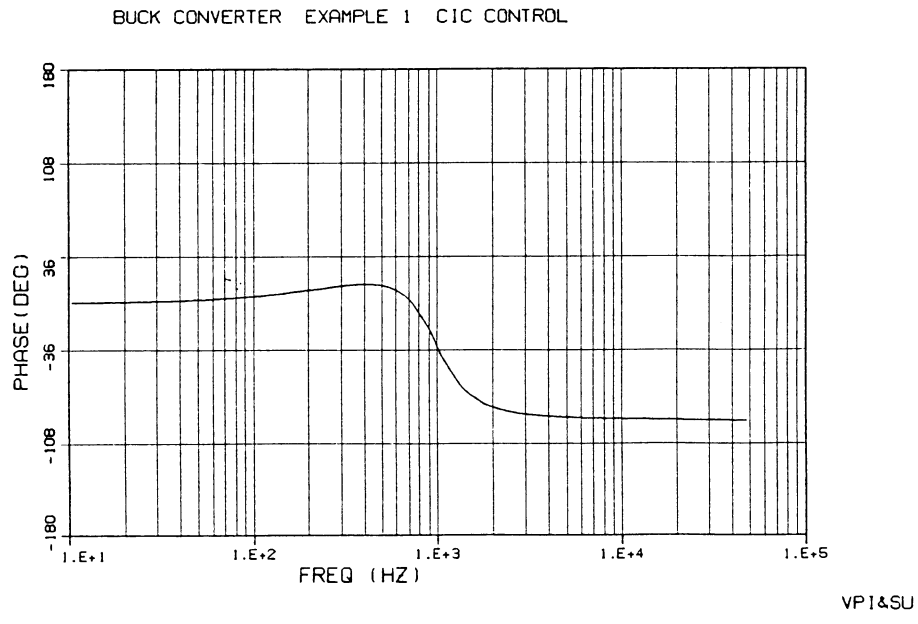
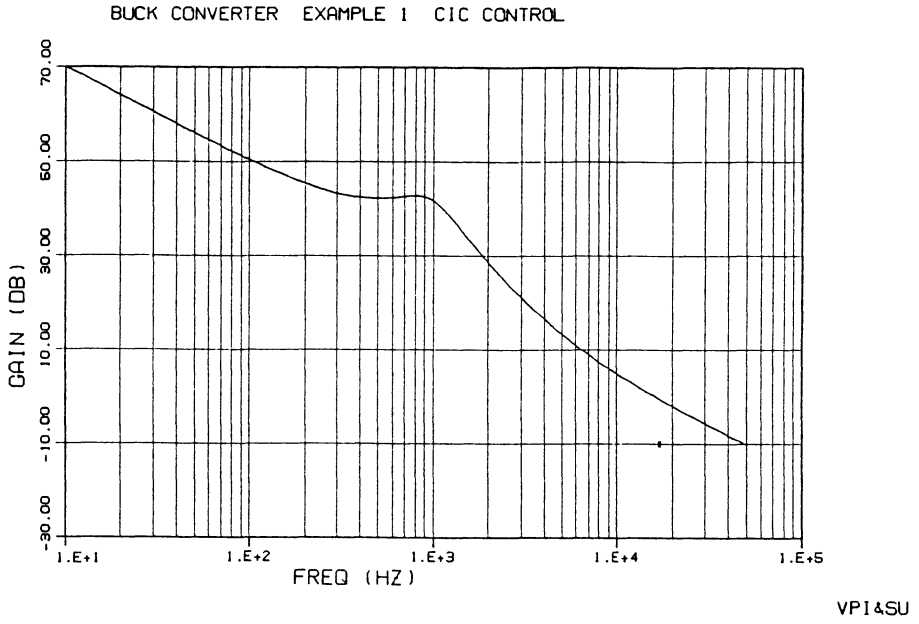


Figure 8.2: Design Example 1 - Single Module Buck Converter with CIC Control. Current Loop Gain, T_i.



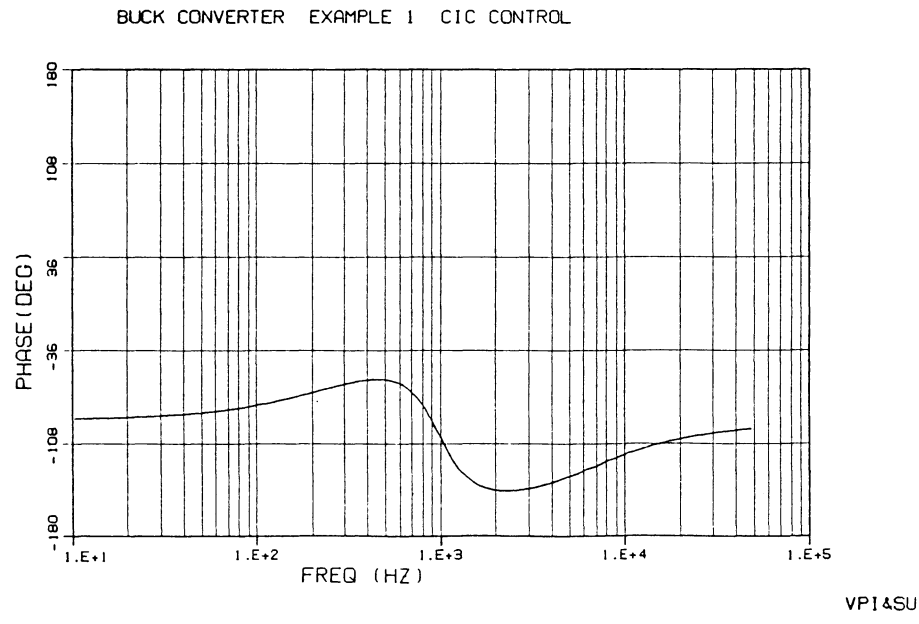
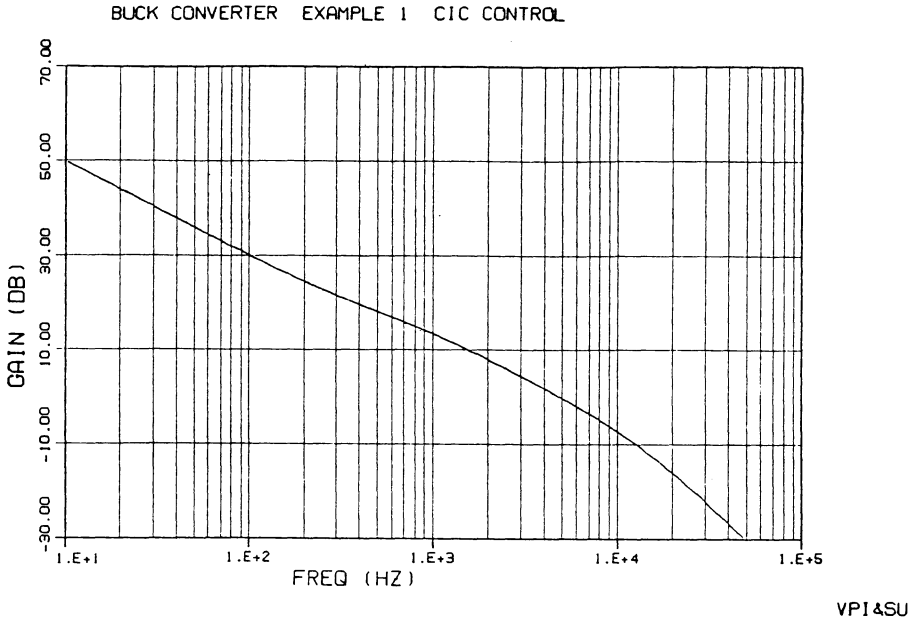


Figure 8.3: Design Example 1 - Single Module Buck Converter with CIC Control. Loop Gain, T_1.



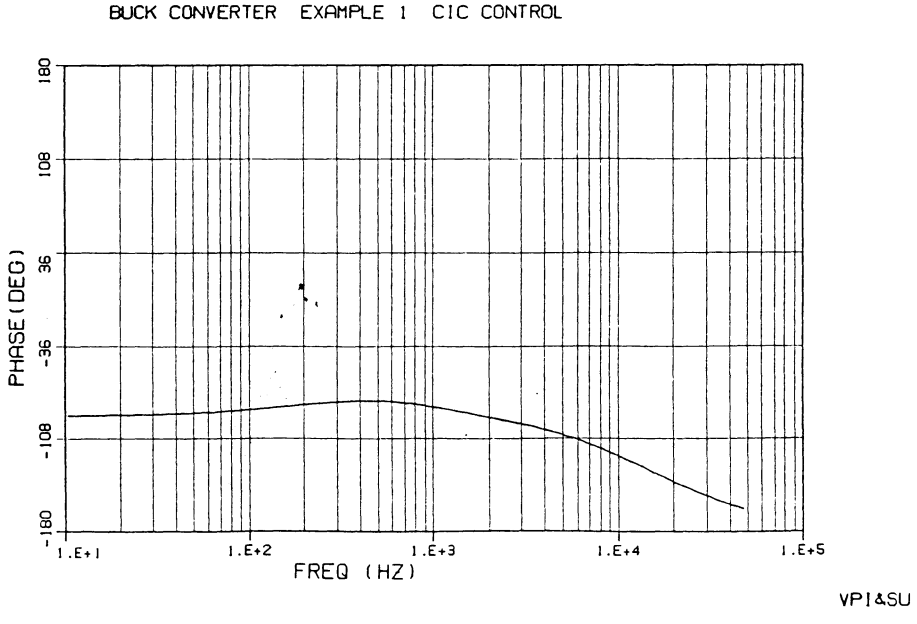
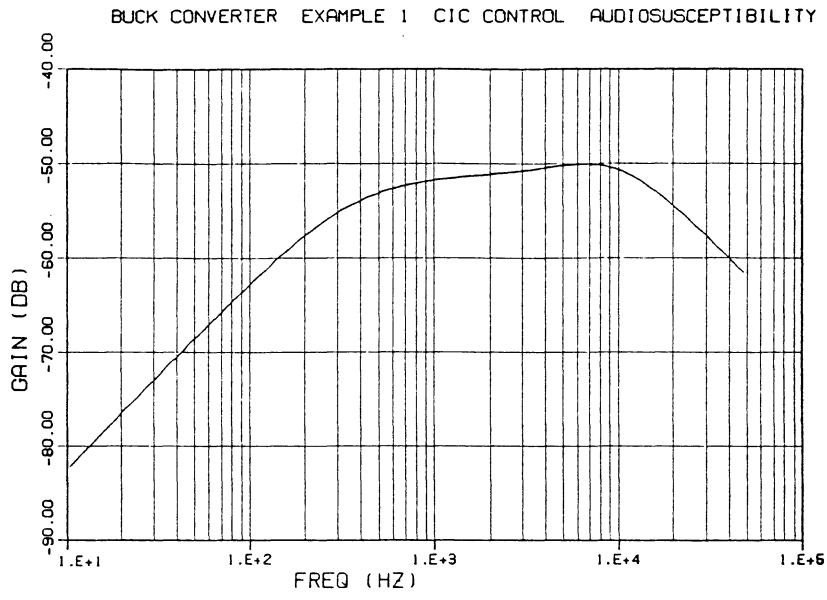


Figure 8.4: Design Example 1 - Single Module Buck Converter with CIC Control. Loop Gain, T_2.



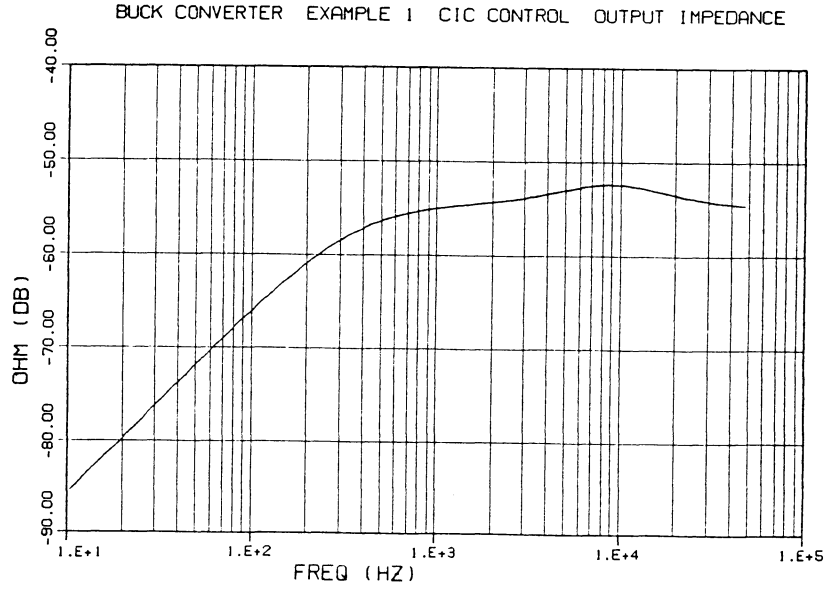


Figure 8.5: Design Example 1 - Single Module Buck Converter with CIC Control. Audiosusceptibility and Output Impedance.

8.2 Design Example 2 - Buck Converter, Single Module

Power stage parameters - same as example 1.

1) Use SCM.

2) - 7) Steps are identical to CIC, example 1.

8) Design current-loop components. From Equation 6.31:

$$\tau_m = \frac{R_4 C_1}{n} = 1.3 \times 10^{-4}$$

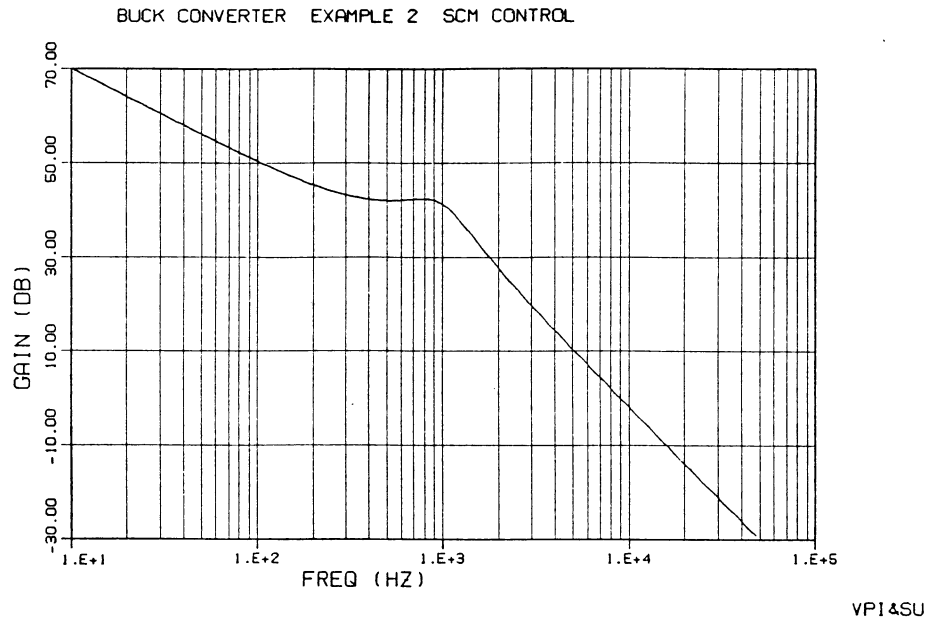
Number of inductor sense turns may be selected arbitrarily. Resistor R_4 is then constrained by the above equation.

$n = 1$

$R_4 = 13$ k

As discussed in Chapter 4, an additional design freedom exists to add a resistor across the integrator capacitor for the current loop of SCM. The pole of the resulting pole-zero pair was placed at several different values ranging from 0 (normal SCM circuit) to s_{01}, to see the effect on the small-signal performance. The small-signal characteristics were simulated, and the results are shown in Figures 8.6 through 8.10. The curves for the placement of the SCM pole at zero show that the small signal characteristics are identical for SCM and CIC. It can be seen that the loop gain begins to degrade as this pole is moved out towards s_{01},

causing a dip in the gain and subsequent peaking of the audiosusceptibility and output impedance characteristics. The beneficial effects of this pole on the output impedance at lower frequencies is clearly shown. A compromised value of this pole should be selected to give improved low frequency output impedance without degrading high frequency characteristics. A value between $s_{01}/5$ and $s_{01}/3$ is suggested.



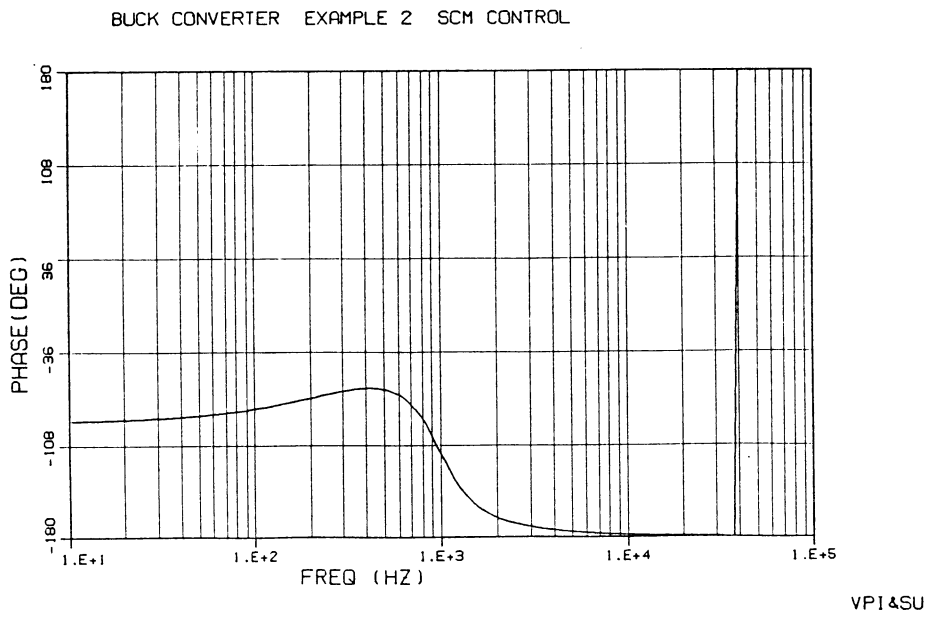
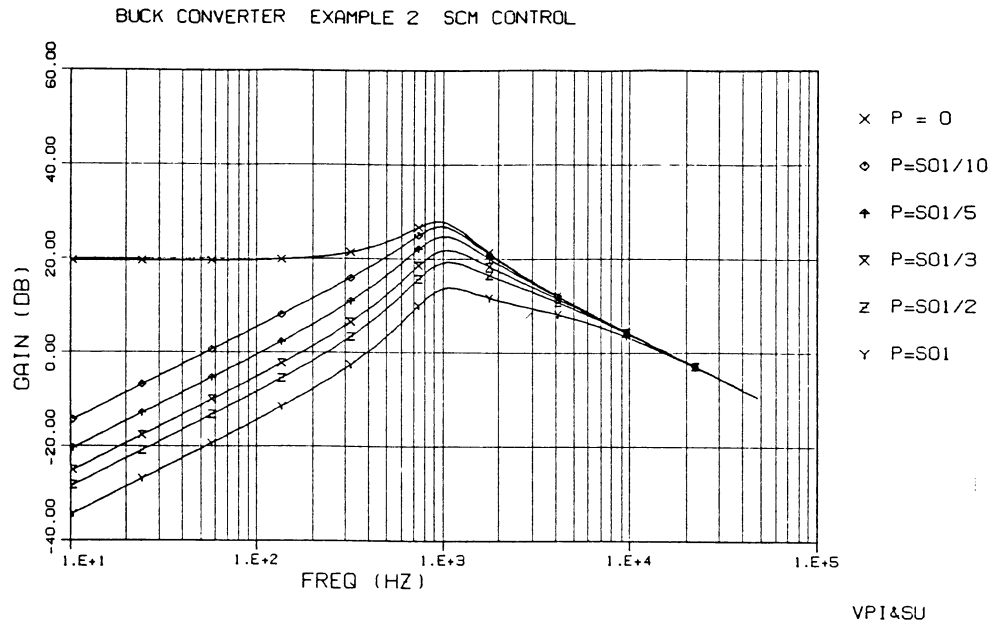


Figure 8.6: Design Example 2 - Single Module Buck Converter with SCM Control. Voltage Loop Gain, T_v.



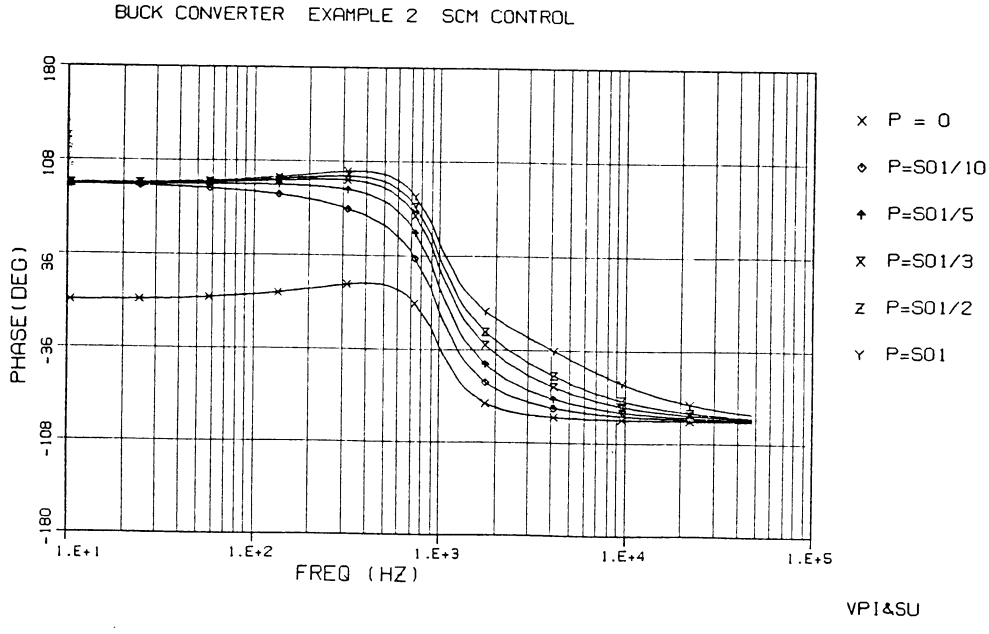
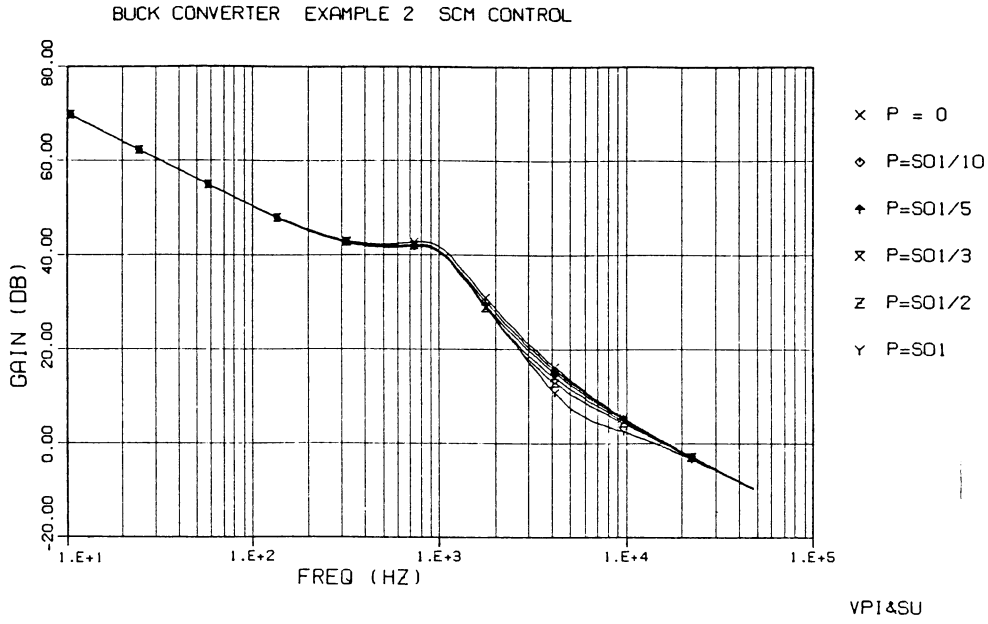


Figure 8.7: Design Example 2 - Single Module Buck Converter with SCM Control. Current Loop Gain, T_i.



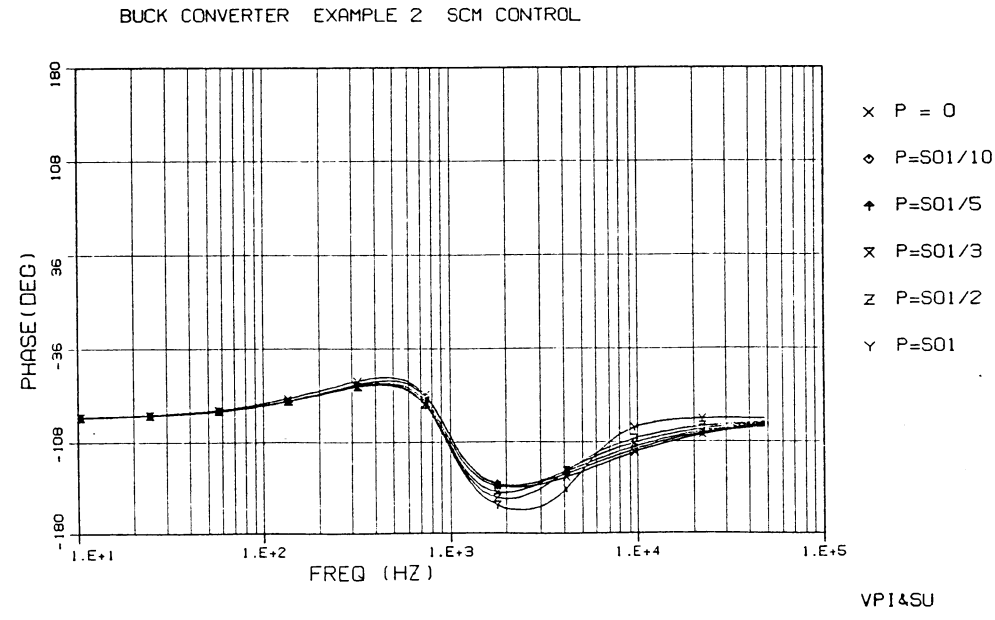
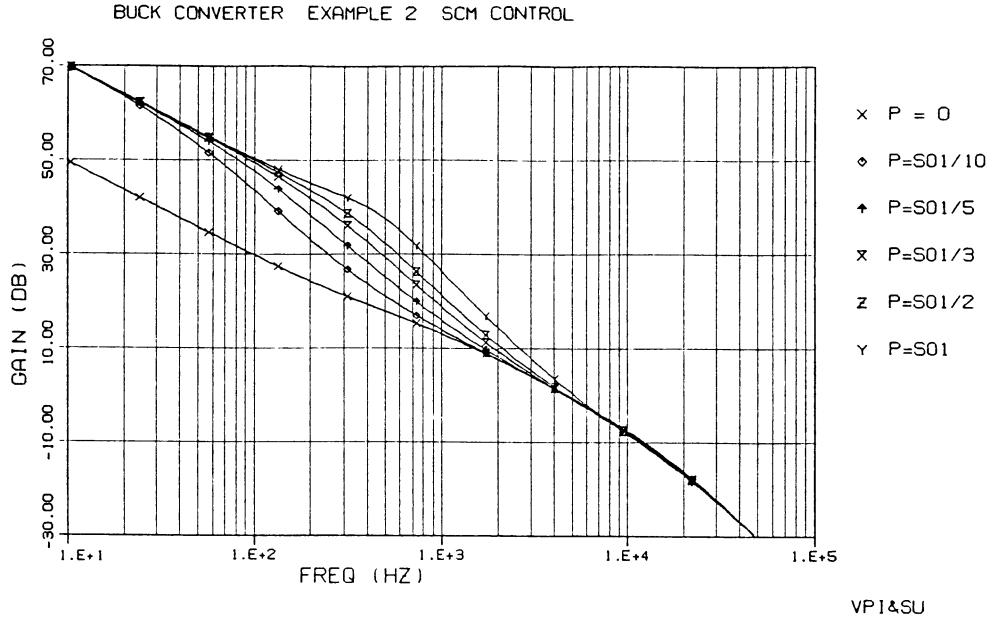


Figure 8.8: Design Example 2 - Single Module Buck Converter with SCM Control. Loop Gain, T_1.



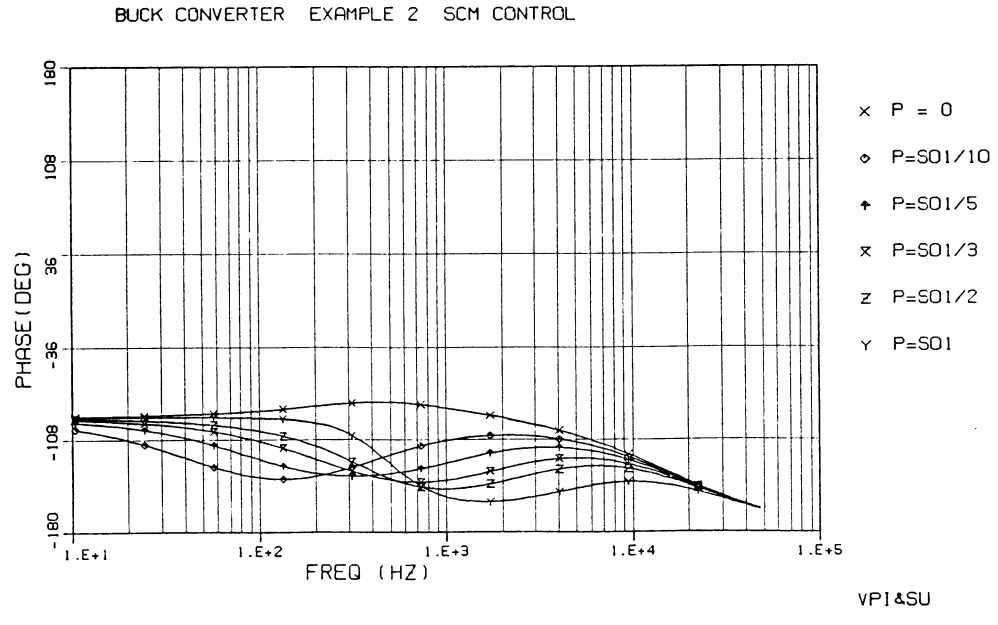
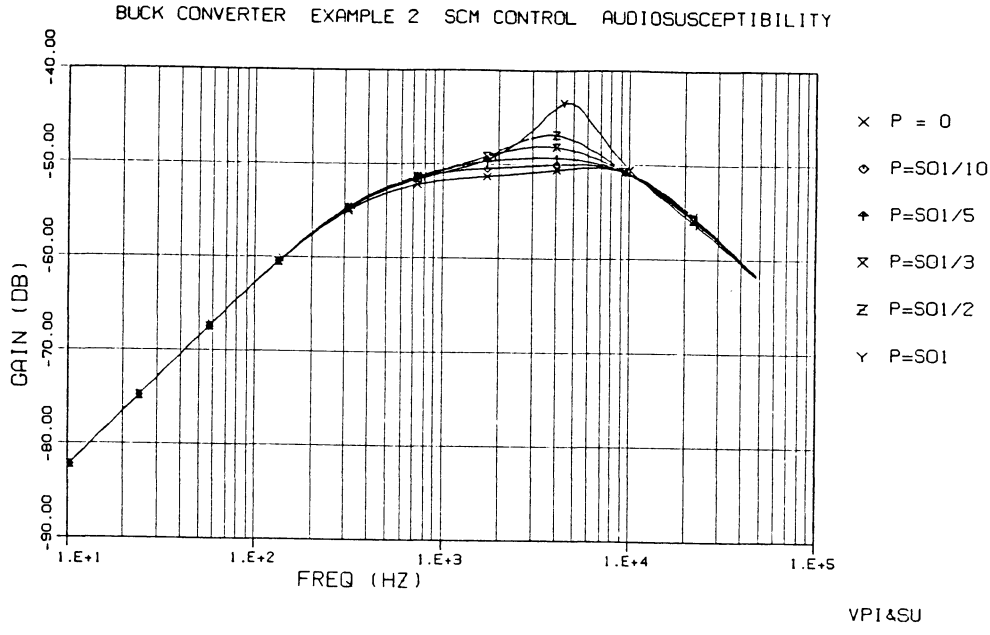


Figure 8.9: Design Example 2 - Single Module Buck Converter with SCM Control. Loop Gain, T_2.



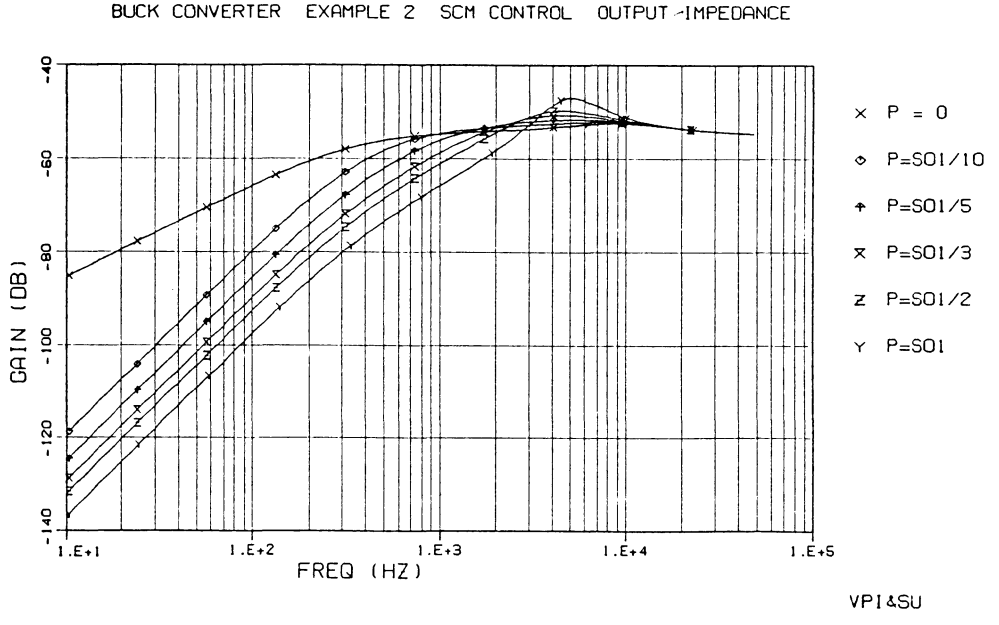


Figure 8.10: Design Example 2 - Single Module Buck Converter with SCM Control. Audiosusceptibility and Output Impedance.

8.3 Design Example 3 - Buck Converter, 3 Parallel Modules

Power Stage Parameters - same as Example 1 except:

$L = 5.1\ \mu H$

$k = 3$ (3 modules used to achieve same effective power stage)

1) Use CIC.

2) Select desired ramp amplitude, $V_p = 0.25$ v.

From Equation 6.1,

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} = 4 \times 10^{-4}$$

3) Design external ramp for minimum input voltage.

$V_{gmin} = 10$ v (200v source) $D = 0.41$

From Equation 6.9,

$$S_e = V_g(D-0.182)/\tau_m = 0.6 \times 10^4$$

4) Evaluate buck parameters.

$L_e = L/k = 1.7\ \mu H$

$\omega_0 = 1/\sqrt{L_e C} = 6500$ rad/s

$\tau_{z1} = CR_c = 2.8 \times 10^{-5}$

$A_1 = 1$

$A_2 = 0$

$M = V_g(1-2D)T_p + 2S_eT_p\tau_m = 3 \times 10^{-4}$

$$K_1 = 2V_g / M = 10^5$$

$$K_2 = D = 0.3$$

5) - 6) Steps are identical to Example 1.

7) Design voltage-loop components.

$$\tau_{z2} = \tau_{z2}'$$

$$\alpha = \frac{A_1\alpha'}{1 + A_2\alpha'\tau_{z2}'} = \alpha'$$

$$C_1R_y = \frac{\tau_m}{\alpha} = 0.65 \times 10^{-4}$$

Capacitor C_1 may be selected arbitrarily. Other components are then constrained by the following equations:

$$C_1 = 0.03\ \mu F$$

$$R_y = 6.5\ k$$

$$C_2 = (\tau_{z2} - \tau_{z1})/R_y = 0.06\ \mu F$$

$$R_5 = \tau_{z1}/C_2 = 470\ ohm$$

$$C_2 = 0.06\ \mu F$$

$$R_5 = 470\ ohm$$

8) Design current-loop components. From Equation 6.33:

$$\tau_m = \frac{n_c L}{R_w} n_p/n_s$$

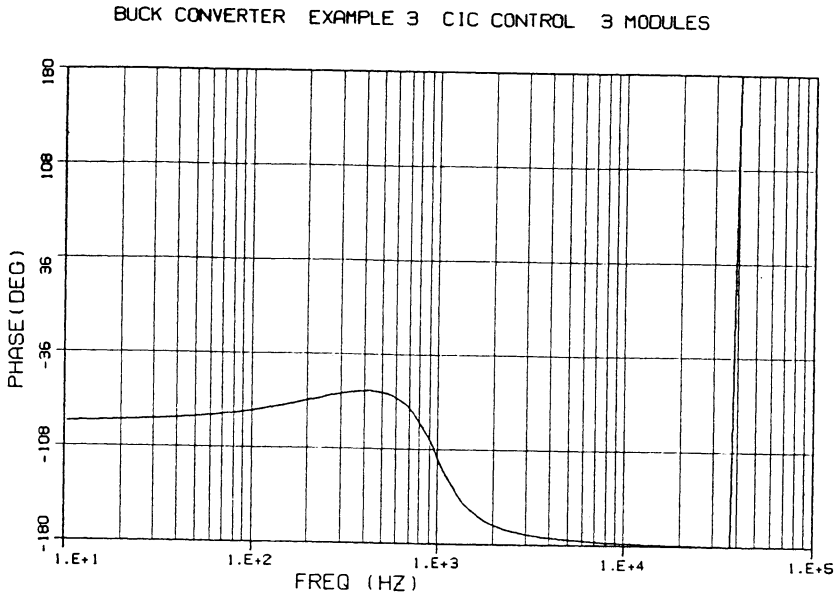
Number of turns of current transformer may be selected arbitrarily. Sense resistor is then constrained.

$n_c = 200$

$R_w = 51$ ohm

(Notice that the only changes in the control circuit are in the value of the added external ramp and the voltage feedback capacitor, C_1.)

The small-signal characteristics for this example are shown in Figures 8.11 through 8.15. These characteristics are identical to those of Example 1, showing that modularity may be achieved without compromising the small-signal performance.



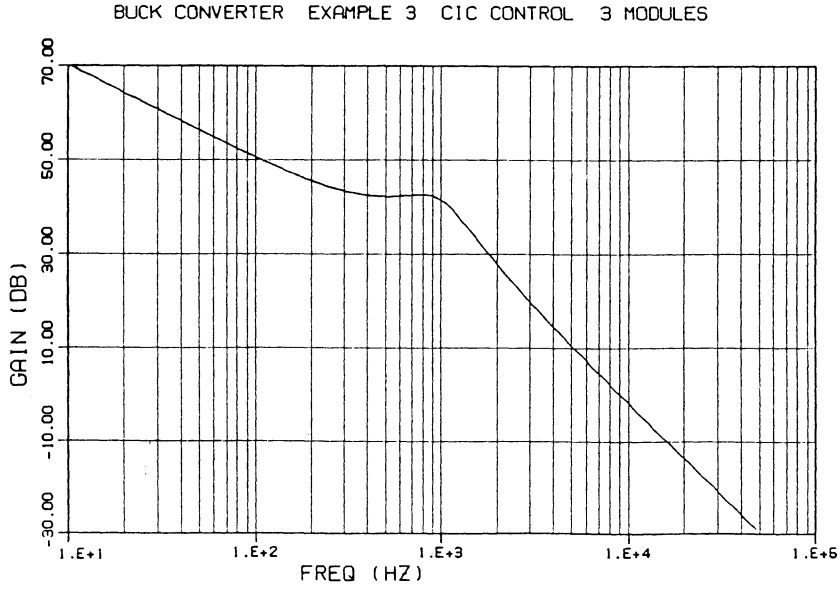
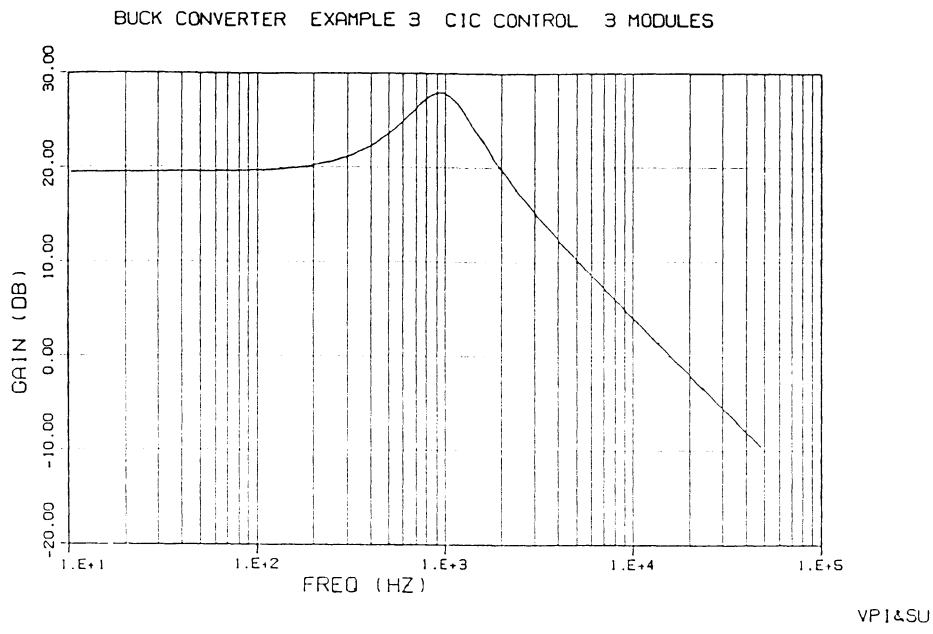


Figure 8.11: Design Example 3 - Buck Converter, 3 Parallel Modules with CIC Control. Voltage Loop Gain, T_v.



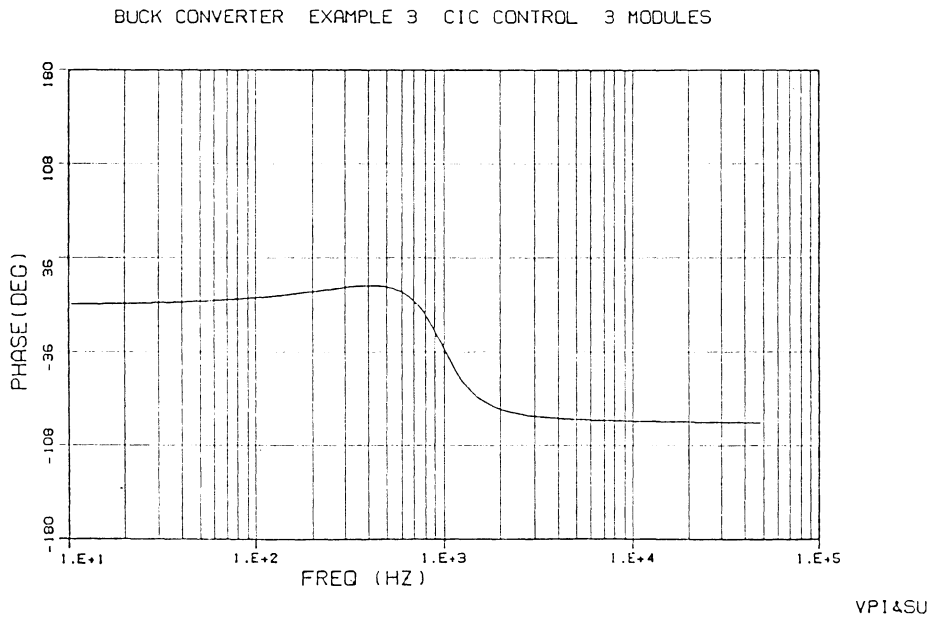
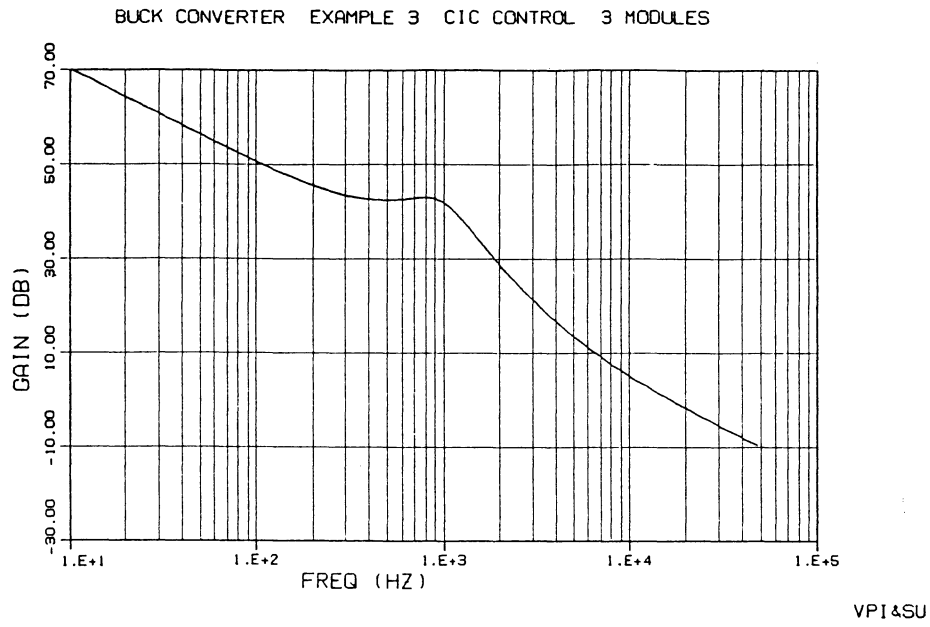


Figure 8.12: Design Example 3 - Buck Converter, 3 Parallel Modules with CIC Control. Current Loop Gain, T_i.



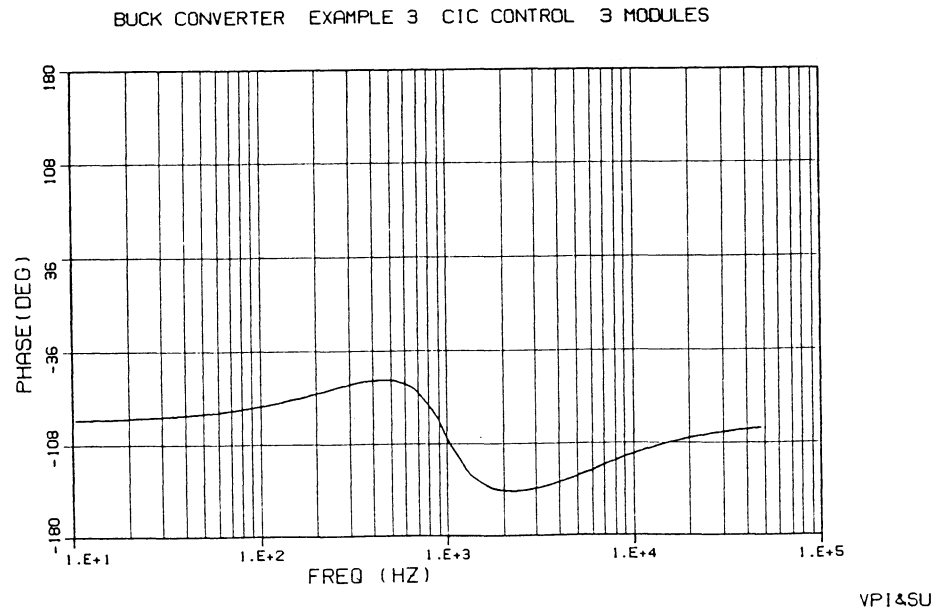
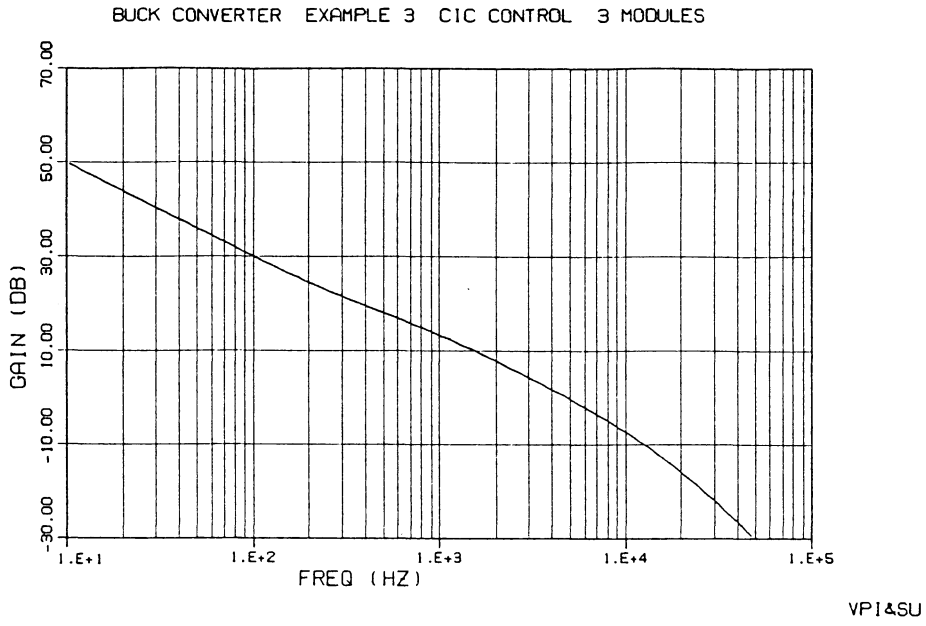


Figure 8.13: Design Example 3 - Buck Converter, 3 Parallel Modules with CIC Control. Loop Gain, T_1.



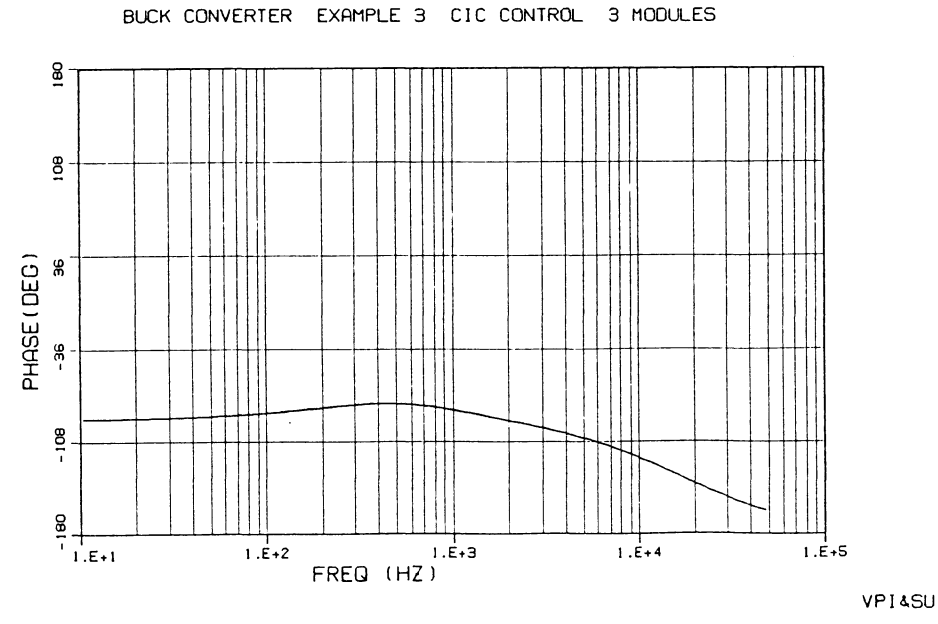
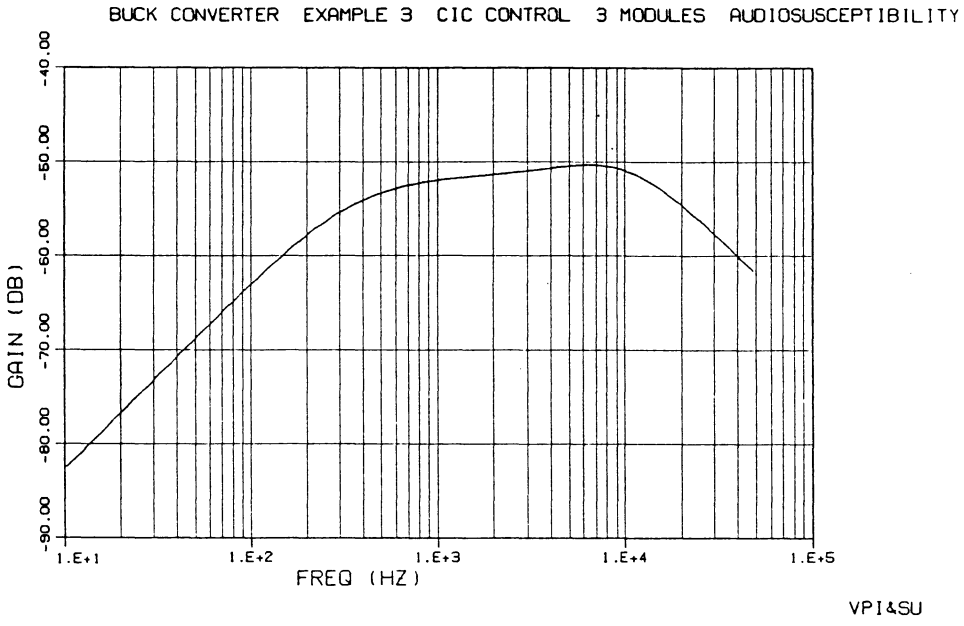


Figure 8.14 Design Example 3 - Buck Converter, 3 Parallel Modules with CIC Control. Loop Gain, T_2.



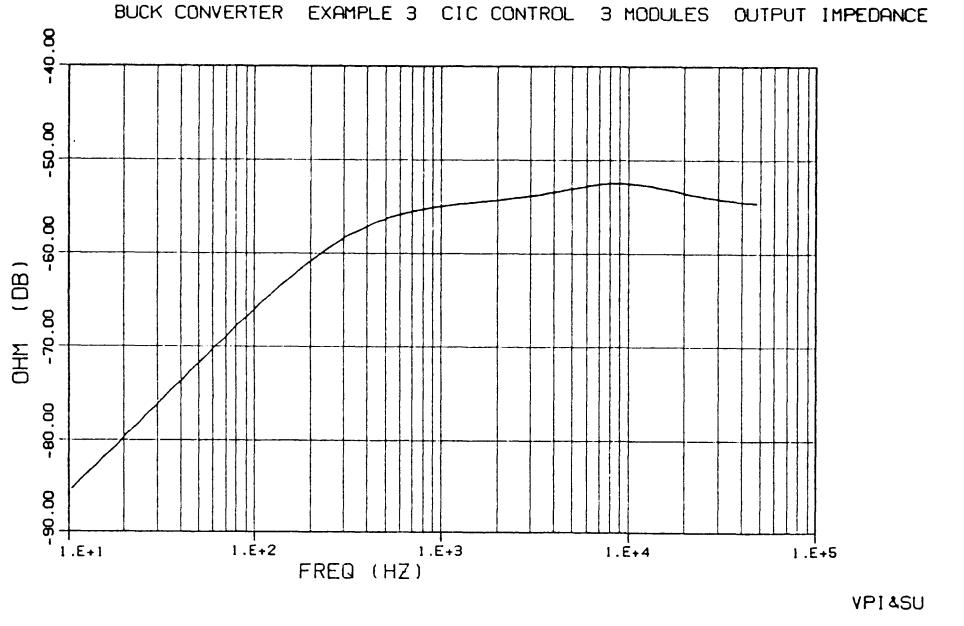


Figure 8.15: Design Example 3 - Buck Converter, 3 Parallel Modules with CIC Control. Audiosusceptibility and Output Impedance.

8.4 Design Example 4 - Buck Converter, 3 Parallel Modules

Power Stage Parameters - same as Example 3.

1) Use SCM/CIC. Use same current-sense network as for Example 3.

2) Select desired ramp amplitude, V_p = 1 v.

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} = 1 \times 10^{-4}$$

From Equation 6.35:

$$\tau_{cic} = \frac{n_c L}{R_w} n_p/n_s = 1 \times 10^{-4}$$

From Equation 6.7,

$$\tau_{scm} = (1/\tau_m - 1/\tau_{cic})^{-1} = 1.3 \times 10^{-4}$$

3) Design external ramp for minimum input voltage.

V_{gmin} = 10 v (200v source) D = 0.41

$$S_e = V_g(D-0.182)/\tau_m = 2.3 \times 10^4$$

4) Evaluate buck parameters.

$L_e = L/k = 1.7\ \mu H$

$\omega_0 = 1/\sqrt{L_e C} = 6500$ rad/s

$\tau_{z1} = CR_c = 2.8 \times 10^{-5}$

$A_1 = 1$

$A_2 = 0$

$M = V_g(1-2D)T_p + 2S_e T_p \tau_m = 3 \times 10^{-4}$

$K_1 = 2V_g / M = 10^5$

$K_2 = D = 0.3$

5) - 6) Steps same as Example 1.

7) Design voltage-loop components.

$$\tau_{z2} = \tau_{z2}'$$

$$\alpha = \frac{A_1\alpha'}{1 + A_2\alpha'\tau_{z2}'} = \alpha'$$

$$C_1 R_y = \frac{\tau_m}{\alpha} = 0.65 \times 10^{-4}$$

C_1 may be selected arbitrarily. Other components are then constrained by the following equations:

$C_1 = 8000$ pF

$R_y = 6.5$ k

$$C_2 = (\tau_{z2} - \tau_{z1})/R_y = 0.06\ \mu F$$

$$R_5 = \tau_{z1}/C_2 \quad = 470 \text{ ohm}$$

$C_2 = 0.06\ \mu F$

$R_5 = 470$ ohm

8) Design current-loop components.

CIC loop:

$$\tau_m = \frac{n_c L}{R_w} n_p/n_s$$

$n_c = 200$

$R_w = 51$ ohm (same components as Example 3)

SCM loop:

$$\tau_m = \frac{R_4 C_1}{n} \quad = 1.3 \times 10^{-4}$$

Number of inductor sense turns may be selected arbitrarily.

Resistor R_4 is then constrained by the above equation.

$n = 1$

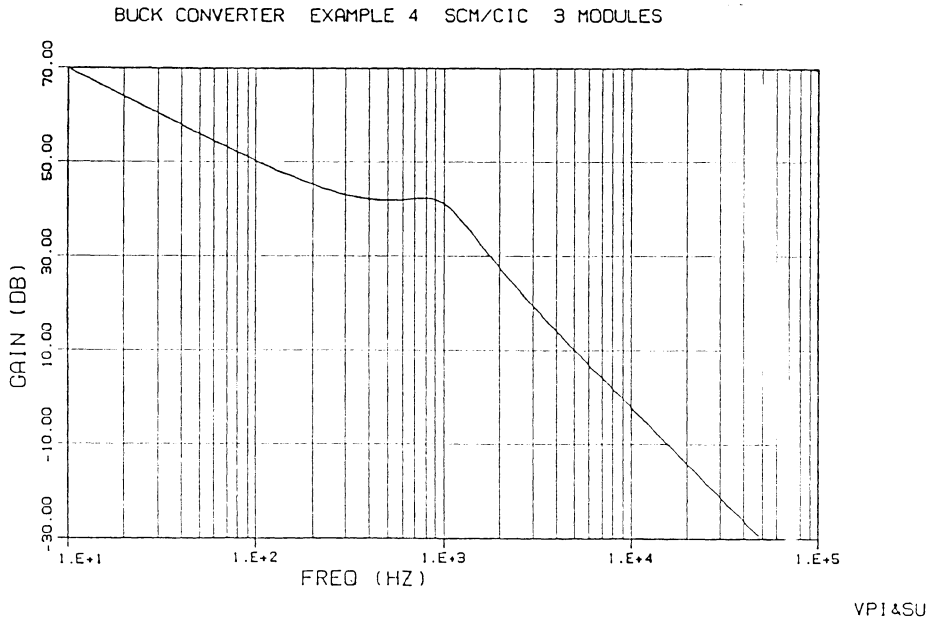
$R_4 = 16.2$ k

SCM pole is placed at $s_{01}/5$

$s_{01} = 3250$ rad/s so $1/C_1R_6 = 3250/5$

R_6 = 190 k.

The small-signal simulation results for this design are shown in Figures 8.16 through 8.22. The different components of the current-loop gain are illustrated. The small-signal simulations show that the performance is identical to the previous examples, but the system has improved noise immunity due to the extra current ramp from the SCM loop.



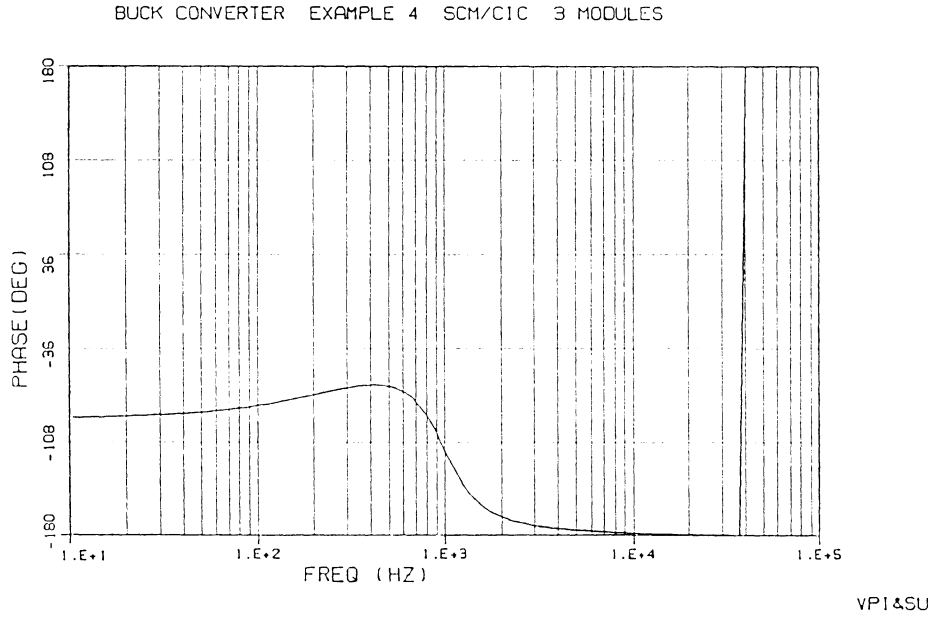
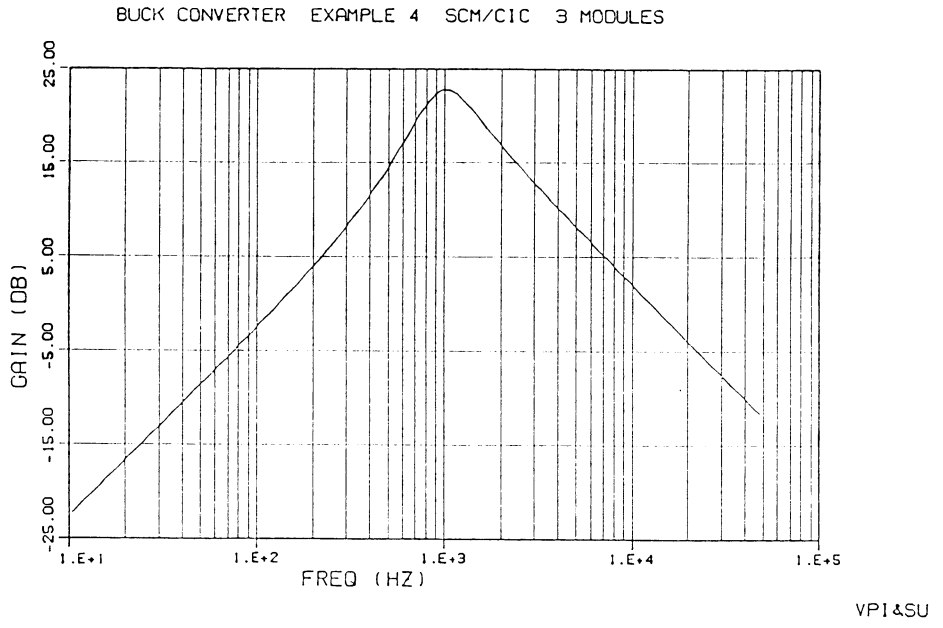


Figure 8.16: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. Voltage Loop Gain, T_v.



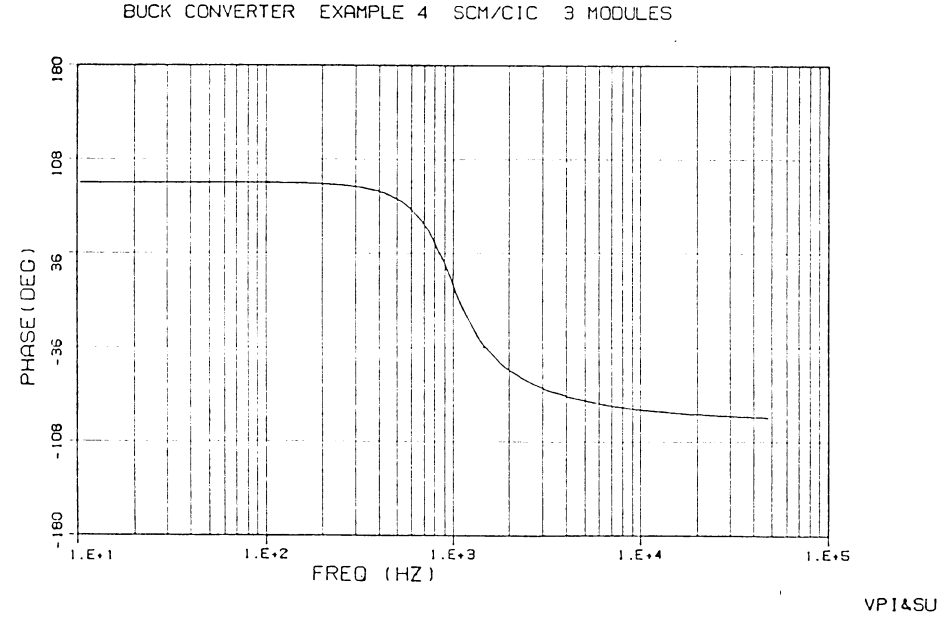
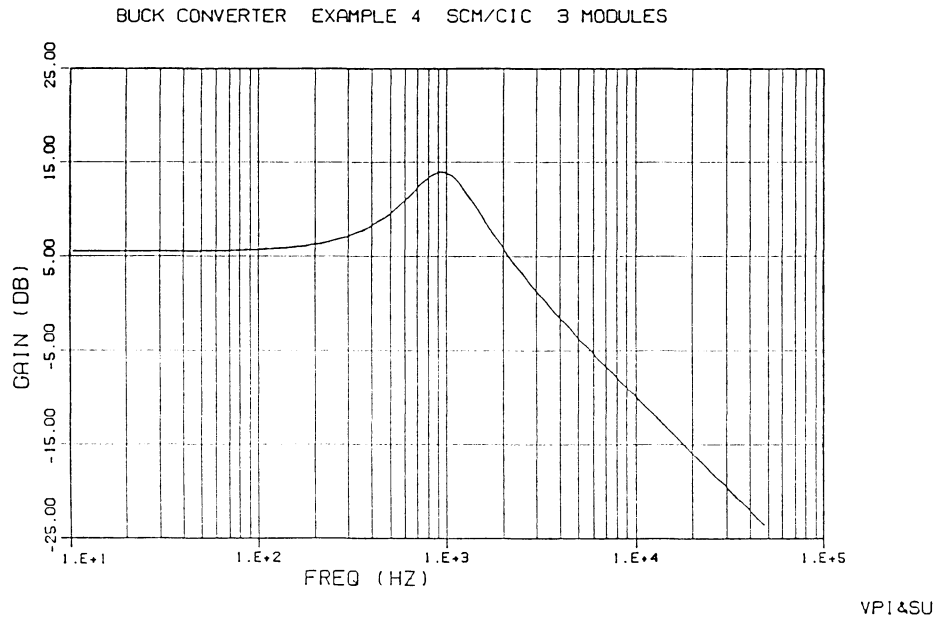


Figure 8.17: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. SCM Component of Current Loop Gain.



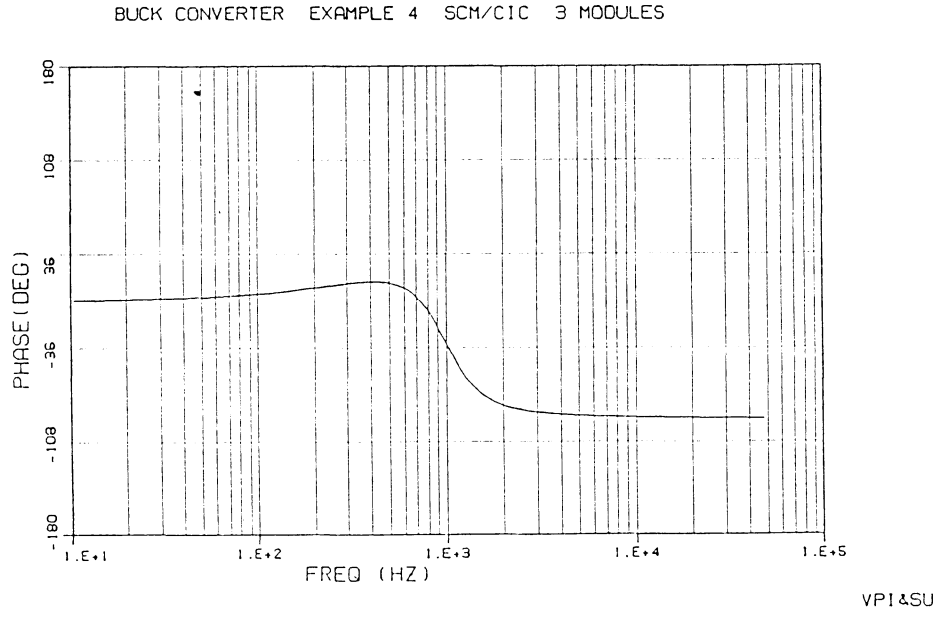
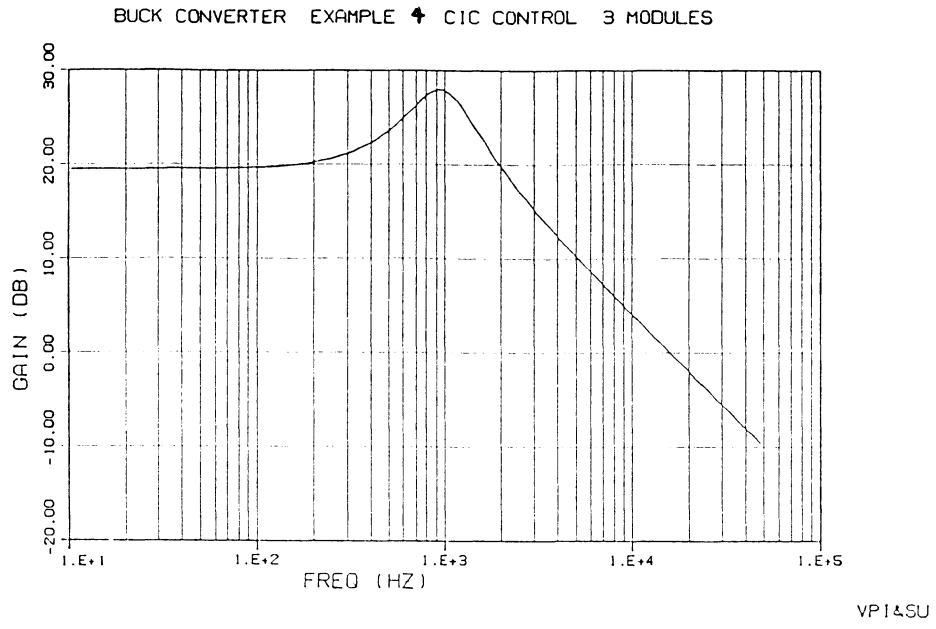


Figure 8.18: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. CIC Component of Current Loop Gain.



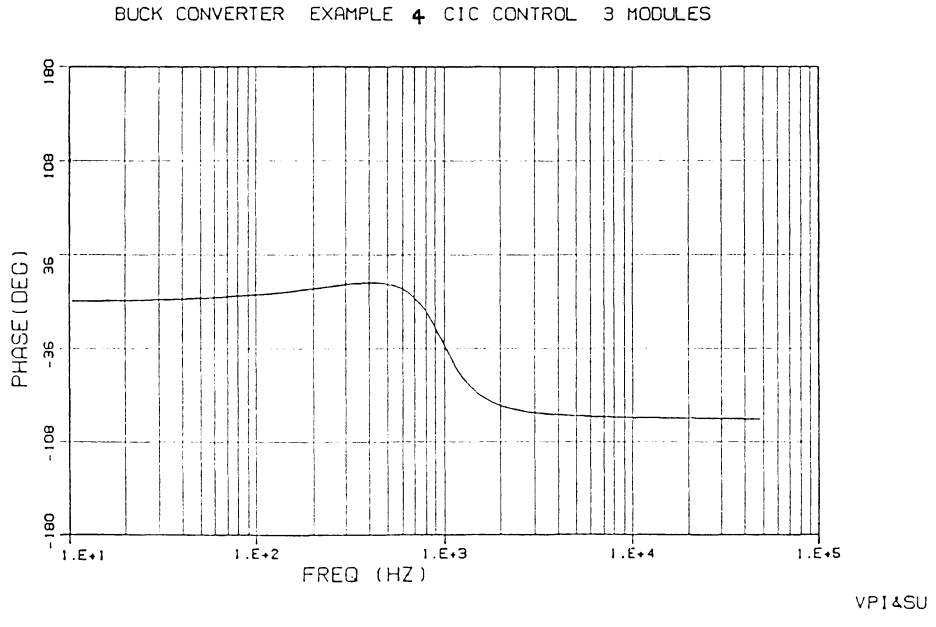


Figure 8.19: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. Total Current Loop Gain, T_i.

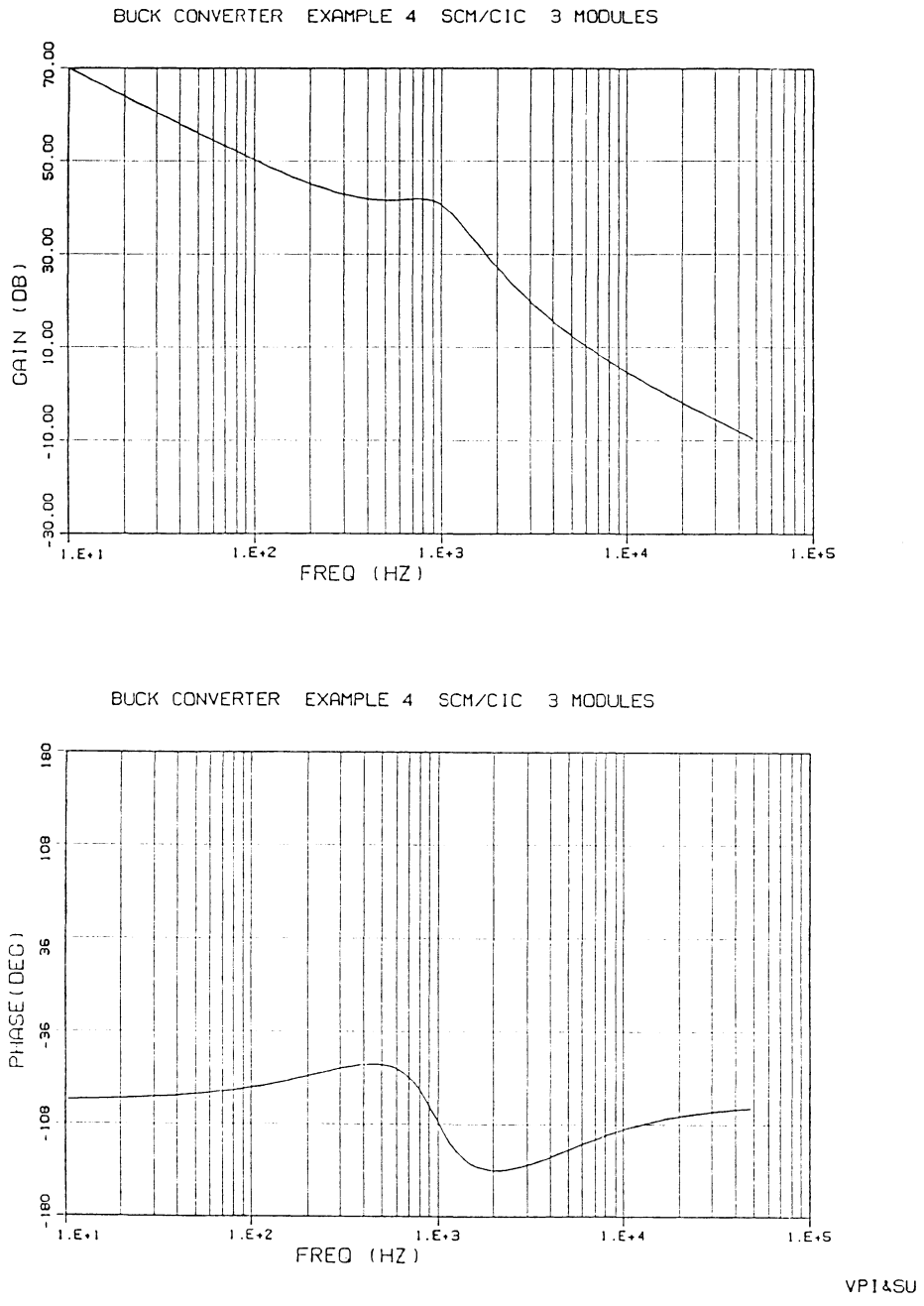
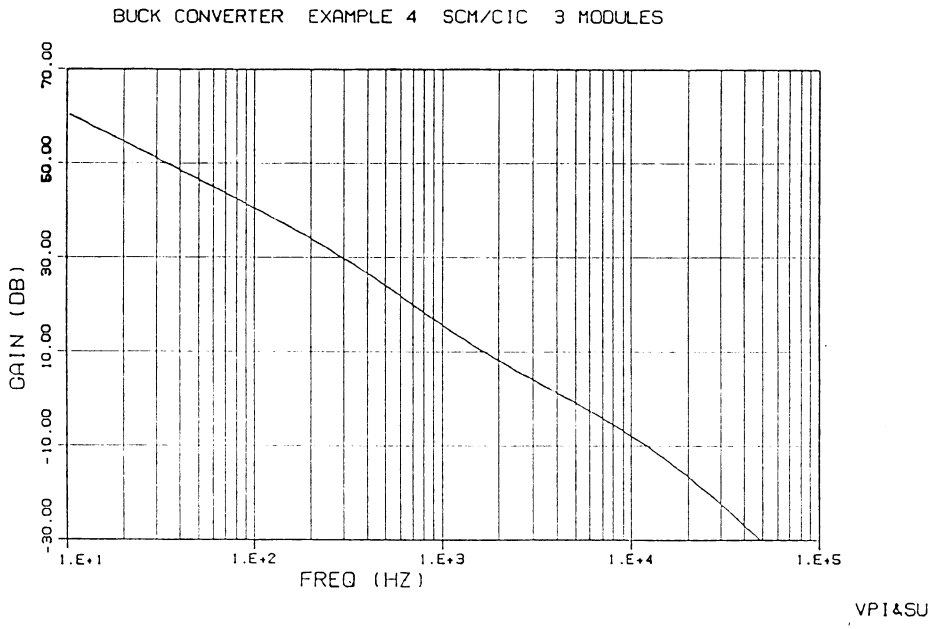


Figure 8.20: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. Loop Gain, T_1.



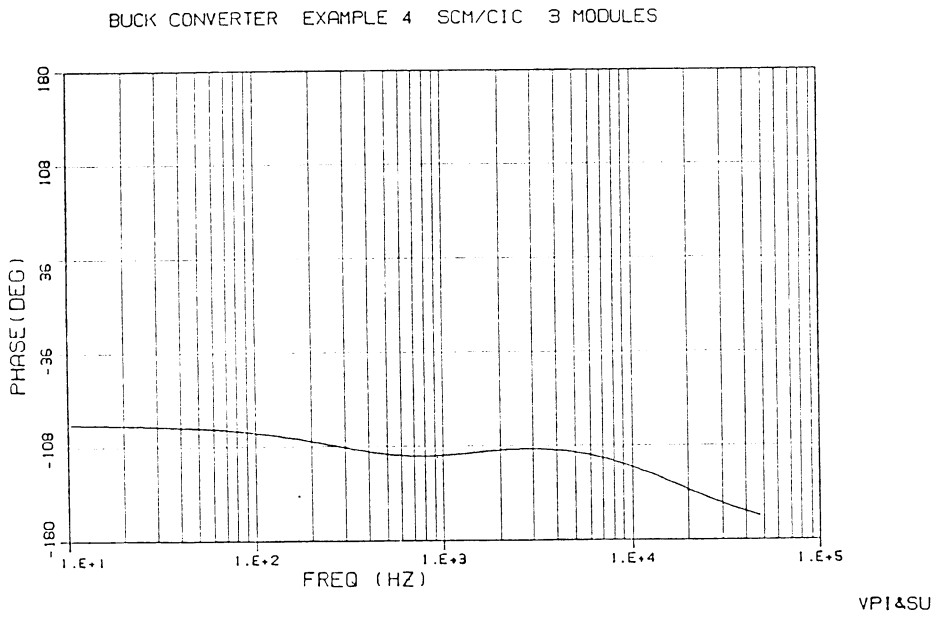
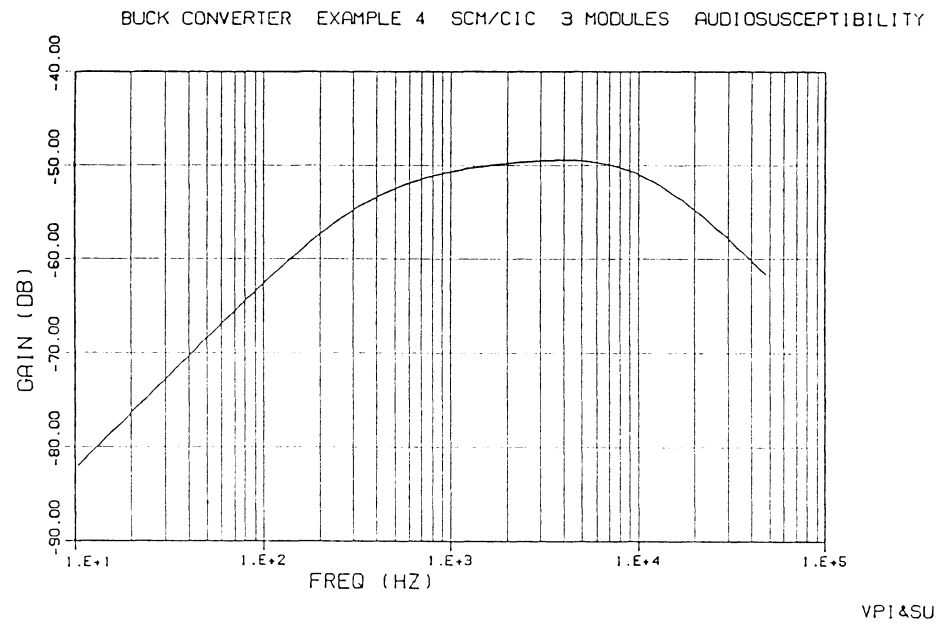


Figure 8.21 Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. Loop Gain, T_2.



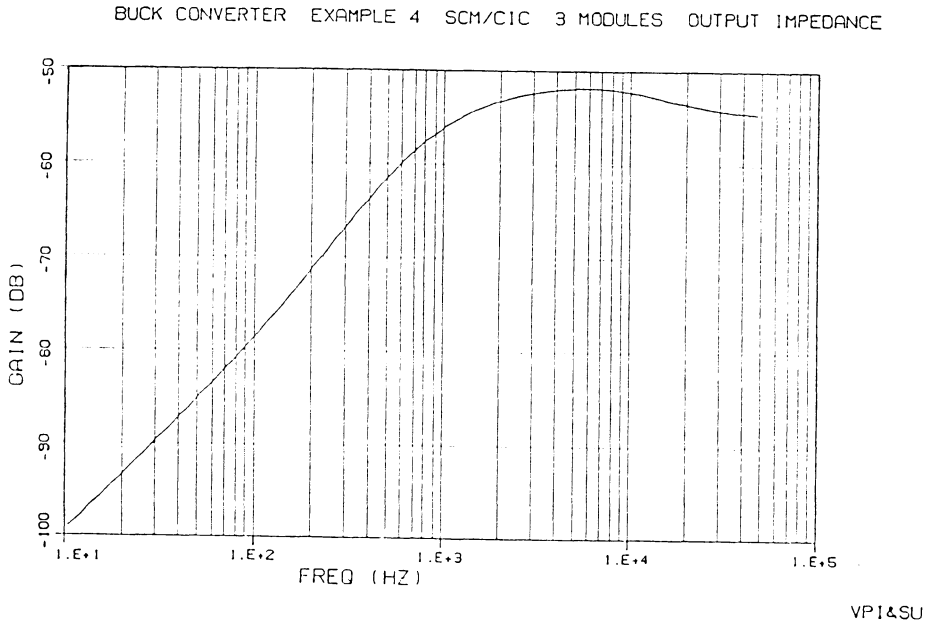


Figure 8.22: Design Example 4 - Buck Converter, 3 Parallel Modules with SCM/CIC Control. Audiosusceptibility and Output Impedance.

8.5.1 Design Example 5 - Buck Converter, 5 Modules, Secondary Filter

Power Stage Parameters

$L = 10\ \mu H$	$V_s = 300$ v	$V_g = 15$ v
$C = 36000\ \mu F$	$V_o = 3.6$ v	
$R_c = 2$ mOhm	$T_p = 28\ \mu s$	
$R_L = 7.2$ mOhm	$n_p/n_s = 20$	
$D = 0.30$ (measured)	$I_o = 500$ A	

Control is first designed without a secondary filter. For this part of the design, to be consistent with the control-loop design procedures, the power inductor is named L and the output capacitor C. These will be re-defined when the secondary filter is added after the control-loop design.

1) Use SCM/CIC.

2) Select desired ramp amplitude, $V_p = 1$ v.

From Equation 6.1,

$$\tau_m = \frac{(V_g - V_o)DT_p}{V_p} = 1.4 \times 10^{-4}$$

Maximum value of CIC signal, $V_m = 5$ v, due to comparator limits. From Equation 6.5:

$$\tau_{cic} = \frac{LV_o}{kV_m R_L} = 2 \times 10^{-4}$$

$$\tau_{scm} = (1/\tau_m - 1/\tau_{cic})^{-1} = 2 \times 10^{-4}$$

3) Design external ramp for minimum input voltage.

V_{gmin} = 9 v (180v source) D = 0.48

From Equation 6.9:

$$S_e = V_g(D-0.182)/\tau_m = 2.7 \times 10^4$$

4) Evaluate buck parameters.

$L_e = L/k = 2.0\ \mu H$

$\omega_0 = 1/\sqrt{L_e C} = 3726$ rad/s

$\tau_{z1} = CR_c = 7.2 \times 10^{-5}$

$A_1 = 1$

$A_2 = 0$

$M = V_g(1-2D)T_p + 2S_e T_p \tau_m = 3.2 \times 10^{-4}$

$K_1 = 2V_g / M = 9.4 \times 10^4$

$K_2 = D = 0.3$

5) No input filter.

6) Design specifications:

Transient response settling time	$\tau_s = 0.5$ ms
Output impedance < 8 mOhm	$K_o = 0.008$
Output peaking 5% for 10% step load	$K_{op} = 0.5$
Audiosusceptibility 30v input step causes 10 mV output disturbance	$K_a = 3.33 \times 10^{-4}$

Upper limit on s_{01}:

$$s_{01} < \frac{1}{\omega_0 \tau_{z1}} = 3.7 \qquad s_{01} < 3.7$$

Audiosusceptibility:

$$K_a' = K_a \, n_p/n_s = 6.7 \times 10^{-3}$$

$$s_{01} > \frac{K_3 \omega_0}{K_a' - K_3 A_2} = 1.8 \qquad s_{01} > 1.8$$

Output impedance:

$$s_{01} > \frac{\omega_0 L_e/A_1}{K_o - L_e A_2/A_1} = 0.93 \qquad s_{01} > 0.93$$

Output peaking:

$$s_{01} > \frac{\omega_0 L_e/A_1 R_L}{K_{op} - L_e A_2/A_1 R_L} = 2.1 \qquad s_{01} > 2.1$$

Settling time:

$$s_{02} > \frac{1}{\omega_0 \tau_s} = 0.54 \qquad s_{02} > 0.54$$

Choose value of s_{02}:

$$0.54 < s_{02} < 1$$

Select value of s_{02} towards low end of range:

$$s_{02} = 0.6$$

Then

$$\tau_{z2}' = \frac{1}{\omega_0 s_{02}} = 4.4 \times 10^{-4} \quad \text{and} \quad \omega_0\tau_{z2}' = 1.67$$

The range for α' is then given by:

$$\frac{s_{01min}}{\omega_0\tau_{z2}'} > \alpha' > \frac{s_{01max}}{\omega_0\tau_{z2}'} \qquad 1.2 < \alpha' < 2.2$$

Use curves from Appendix D to select the value of α'. In this case, the curve for $\omega_0\tau_{z2}' = 2$ is used to select the value of α'.

Picking $\alpha' = 1.5$ gives a crossover frequency of $20\omega_0 = 12$ kHz and a phase margin of 80 degrees.

7) Design voltage-loop components.

$$\tau_{z2} = \tau_{z2}'$$

$$\alpha = \frac{A_1\alpha'}{1 + A_2\alpha'\tau_{z2}'} = \alpha'$$

The voltage-loop control components can now be found from:

$$C_1 R_y = \frac{\tau_m}{\alpha}$$

C_1 may be selected arbitrarily.

$C_1 = 0.01\ \mu F$

$R_y = 6.7\ k$

Other components are then constrained by:

$$C_2 = (\tau_{z2} - \tau_{z1})/R_y$$

$$R_5 = \tau_{z1}/C_2$$

$C_2 = 0.056\ \mu F$

$R_5 = 1.3\ k$

8) Design current-loop components.

$$\tau_{cic} = \frac{n_c L}{R_w} n_p/n_s = 2 \times 10^{-4}$$

Number of turns of current transformer may be selected arbitrarily.

Sense resistor is then constrained.

$n_c = 200$

$R_w = 200$ ohm

SCM loop:

$$\tau_{scm} = \frac{R_4 C_1}{n} = 2 \times 10^{-4}$$

Number of inductor sense turns may be selected arbitrarily. Resistor R_4 is then constrained by the above equation.

$n = 1$

$R_4 = 20$ k

SCM pole is placed at $s_{01}/3$

$R_6 = 30$ k.

8.5.2 Secondary Output Filter Design

The design guidelines for the second stage output filter were developed in Chapter 7. In Chapter 7, the filter components were labelled according to Figure 7.1, with inductor L_1 representing the main power inductor, and C_2 the main filter capacitor for the optimum design. The power inductor for this example is, therefore, referred to as L_1 and the filter capacitor as C_2. (Note that C_1 and C_2 should not be confused with the control-loop components.

The schematic for the output stage of the parallel converters is shown in Figure 7.1 with the additional second-order filter. The components to be designed for this circuit are L_2, C_1 and R_{c1}. For high-frequency noise attenuation, the ESR of the capacitors become the dominant impedance, and R_{c1} must be selected to be a low value. The value of the ESR of the capacitor is assumed to be 2 mOhm. In order

that the first stage of the filter attenuates as much as possible at the switching frequency, a lower bound may then be determined for the capacitor, C_1.

$$C_1 > \frac{1}{2\pi f_s R_{c1}} \qquad C_1 > 2200\ \mu F.$$

From the discussion of Chapter 7, it is also required that $C_1 < C_2$ for the best filter design. Hence, the range of C_1 is:

$$2200\ \mu F < C_1 < 36000\ \mu F$$

The second filter inductance, L_2, should be designed to be significantly less than L_1. The second filter resonance is then given by:

$$\omega_{02} = \frac{1}{\sqrt{L_2 C_s}} \qquad \text{where } C_s = \frac{C_1 C_2}{C_1 + C_2}$$

In order to minimize the effect of the second filter on system stability, the second filter resonance should occur at a frequency above s_{01}, where the current loop dominates the voltage loop. Hence, we require

$$\omega_{02} >> s_{01} \qquad \omega_{02} >> 9300\ \text{rad/s}$$

If the second resonant frequency is picked to be five times larger than s_{01} and if C_1 is selected to be its minimum value of 2200 μF, L_2 can then be determined:

$$L_2 = 190 \text{ nH}$$

A second requirement for the filter not to significantly affect the stability is that its Q factor should be low. For the previously selected values:

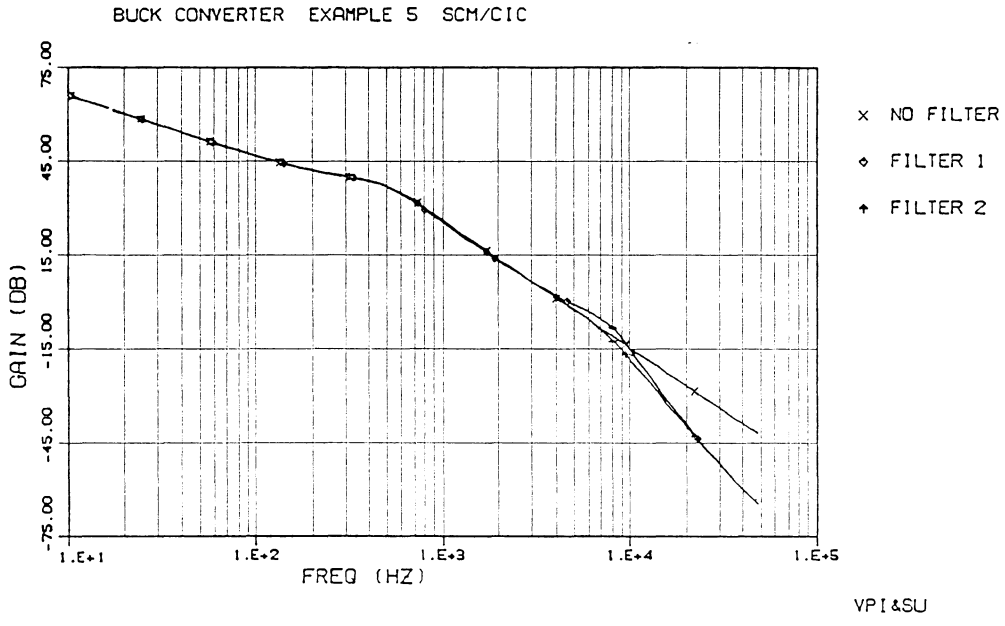
$$Q = \frac{\omega_{02} L_2}{R} = 2.5 \qquad \text{where } R = R_{c1} + R_{c2}$$

This is an unacceptably large value and some attenuation must be sacrificed to achieve a more stable system. If L_2 is reduced to 100 nH and C_1 is increased to 4400 μF, the second resonant frequency remains unchanged and the Q is reduced to 1.25. This is an acceptable value.

With these design values, the attenuation at the switching frequency due to the second filter is -20 dB. If the switching of the five power modules is overlapped, the output ripple frequency is five times the switching frequency and the ripple reduction is even more dramatic. The small-signal characteristics of this system are shown in Figures 8.23 through 8.29. Three sets of curves are shown for each plot: the first corresponds to the five modules without a second output filter; the second shows the response for the filter as designed above (filter 1), and the third is the same filter with capacitors C_2 and C_1 interchanged.

Comparison of the case with no filter and filter 1 shows that the filter causes a slight dip in the loop gain (but not stability problems) and a corresponding peak in the audiosusceptibility. The output impedance is actually reduced with the second filter.

The plots for filter 2 confirm the predictions of Chapter 7, showing a significant peaking of the output impedance. From the small-signal point of view, it is desirable that the filter 1 configuration be used.



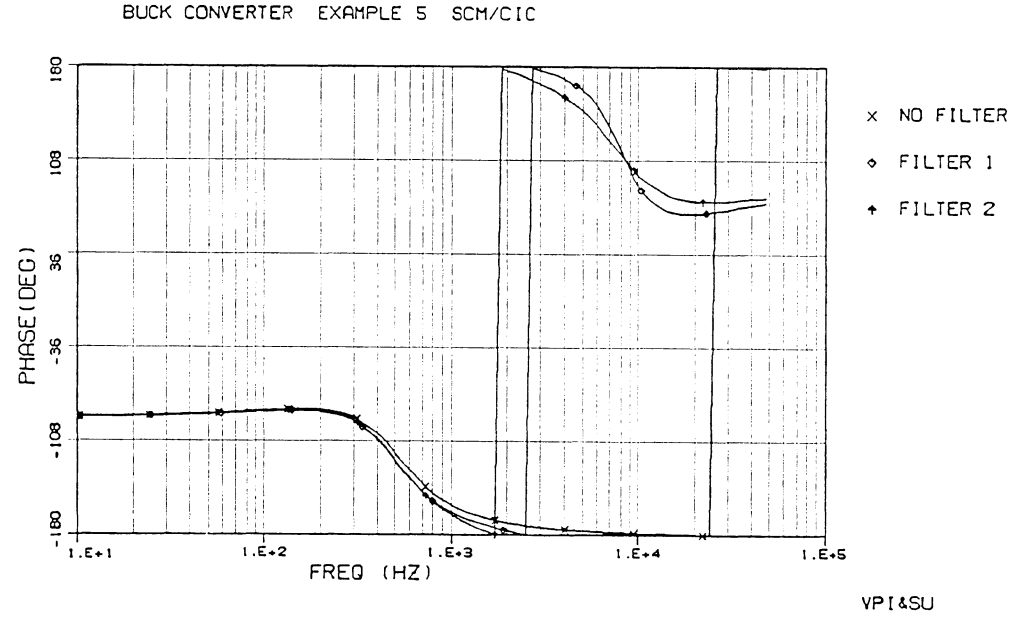
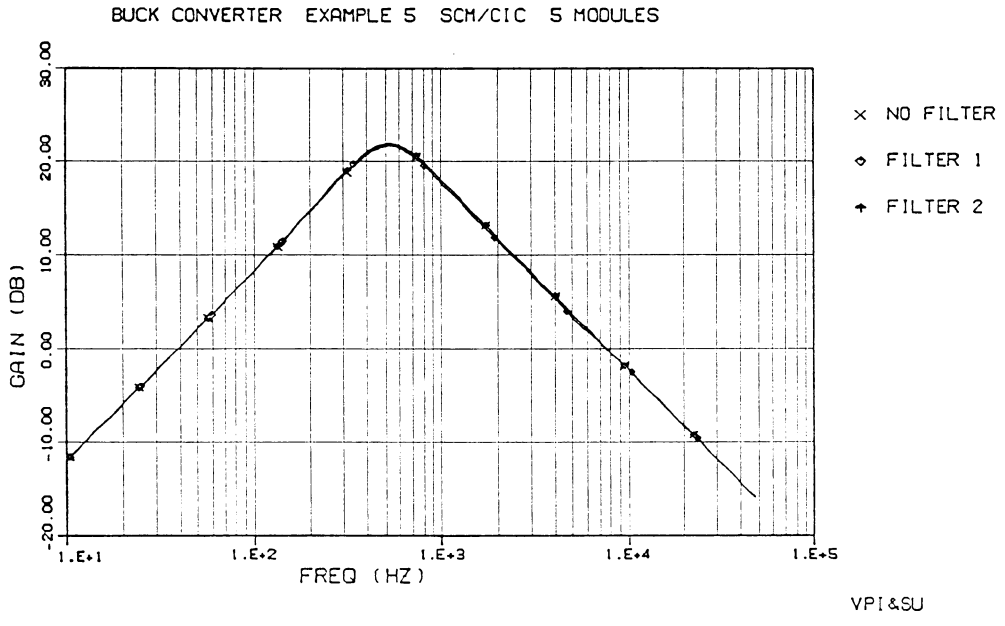


Figure 8.23: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. Voltage Loop Gain, T_v.



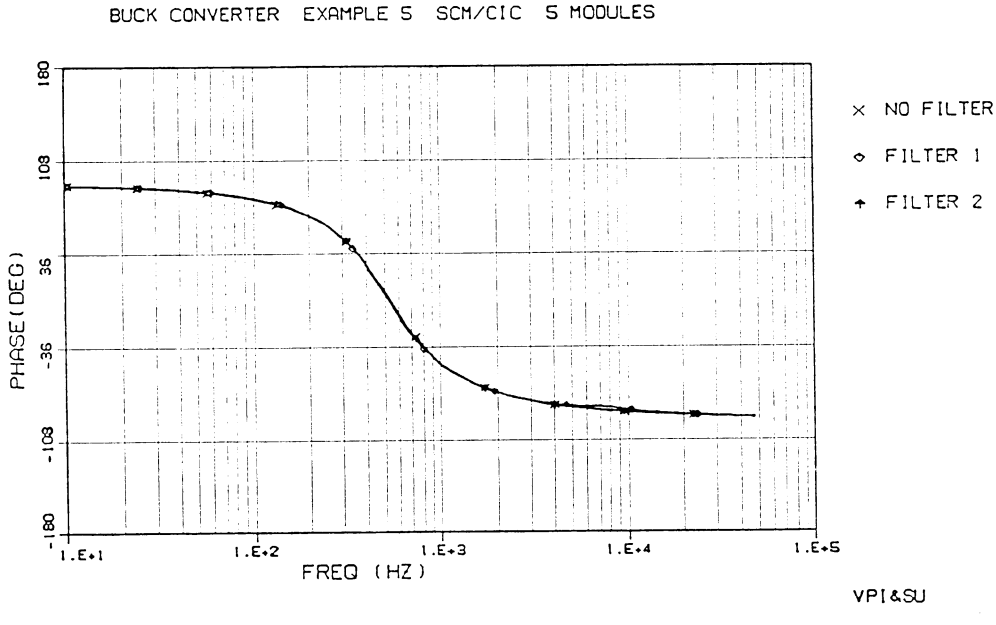
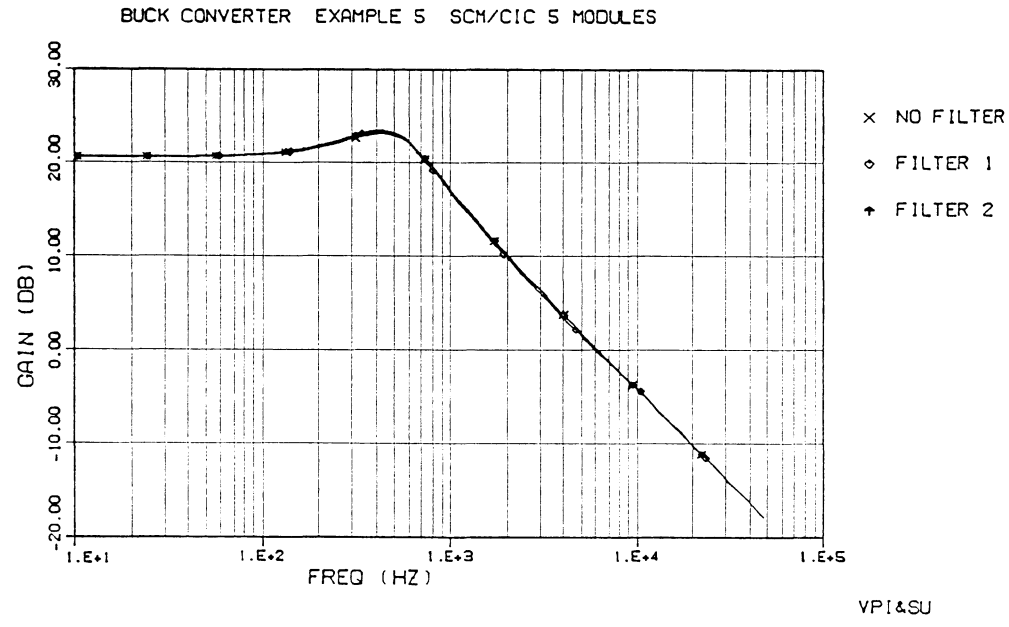


Figure 8.24: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. SCM Component of Current Loop Gain.



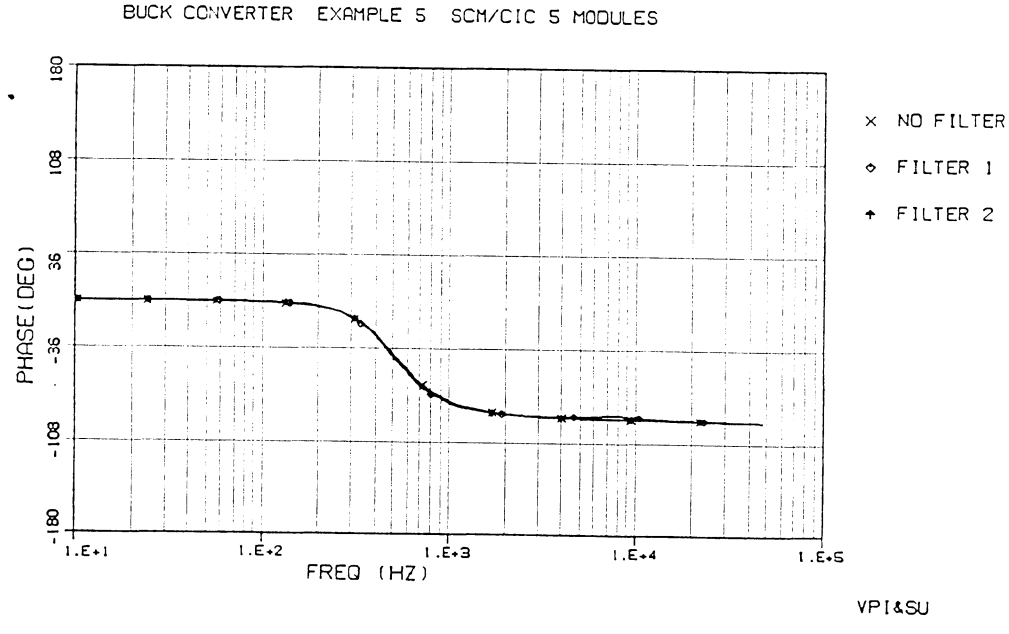


Figure 8.25: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. CIC Component of Current Loop Gain.

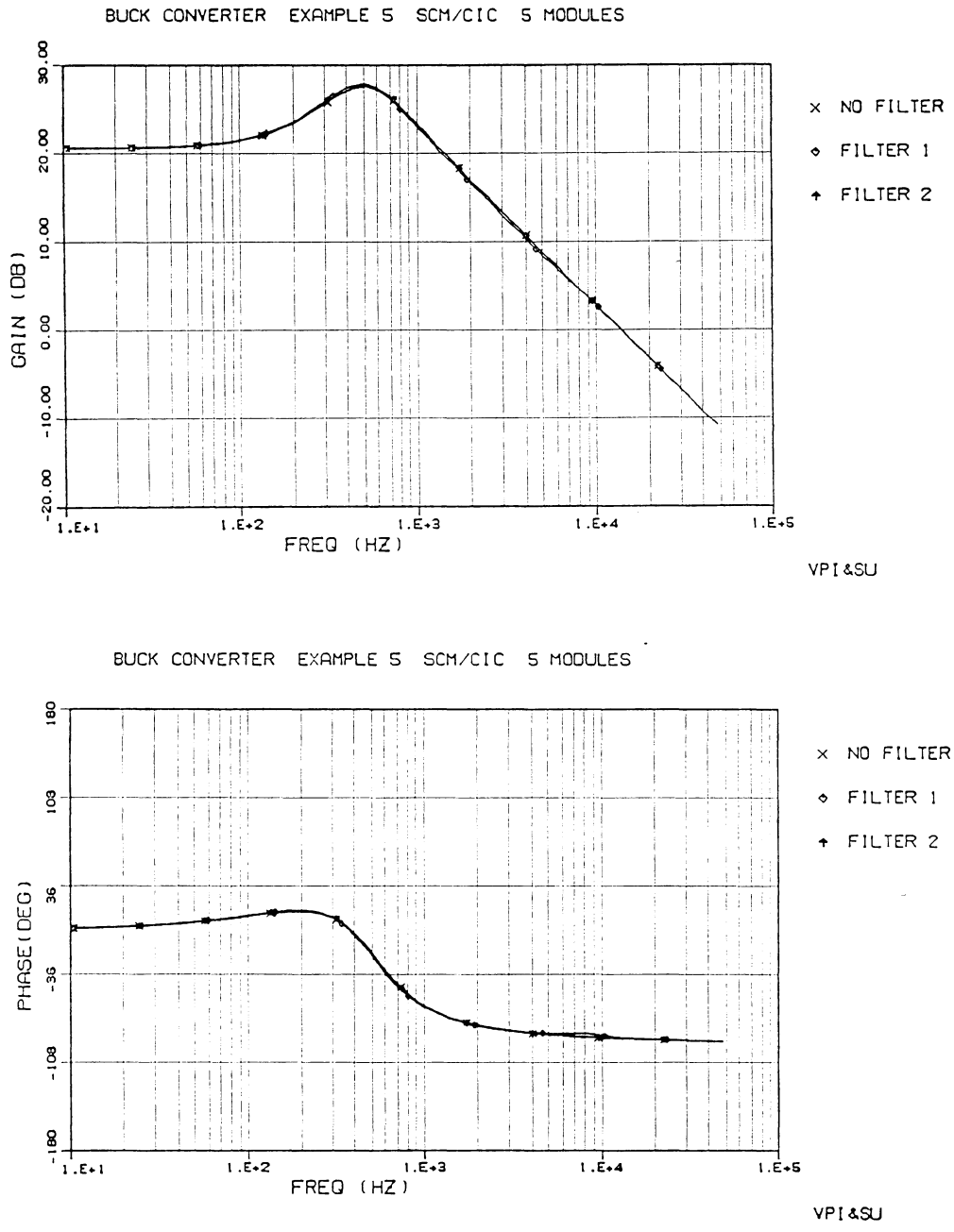
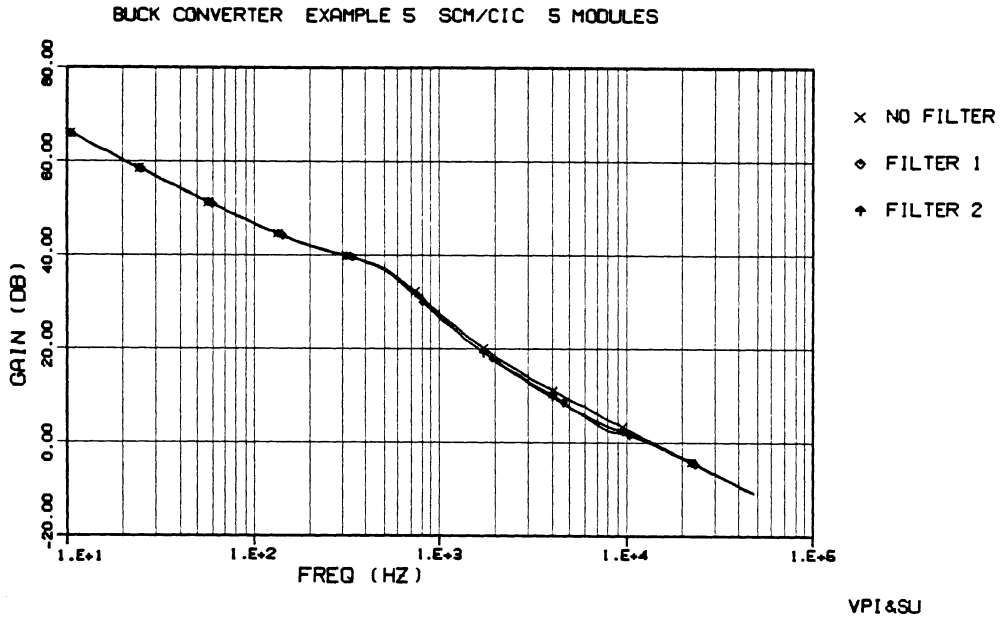


Figure 8.26: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. Total Current Loop Gain, T_i.



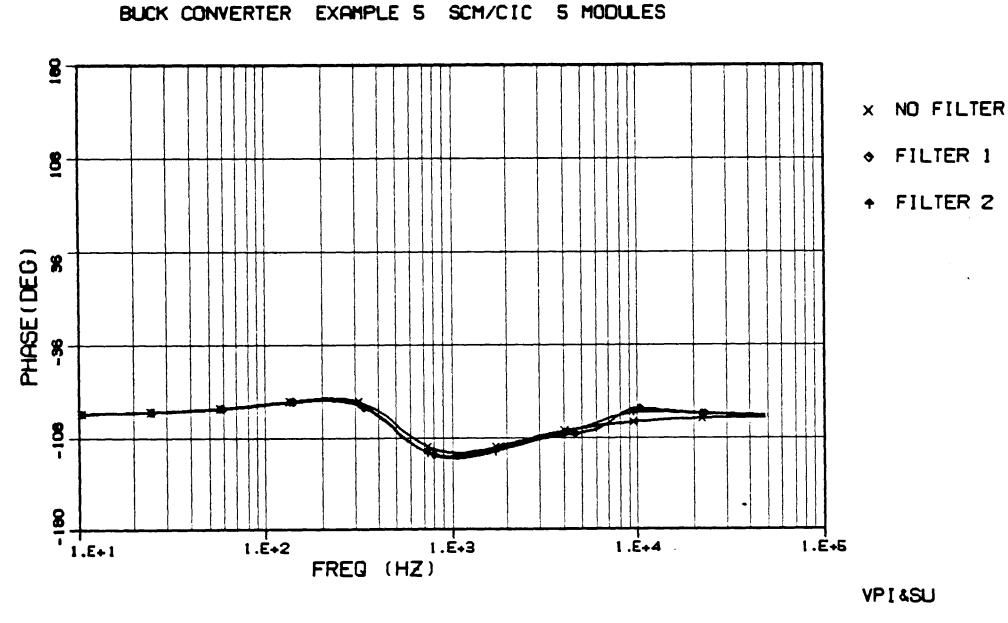
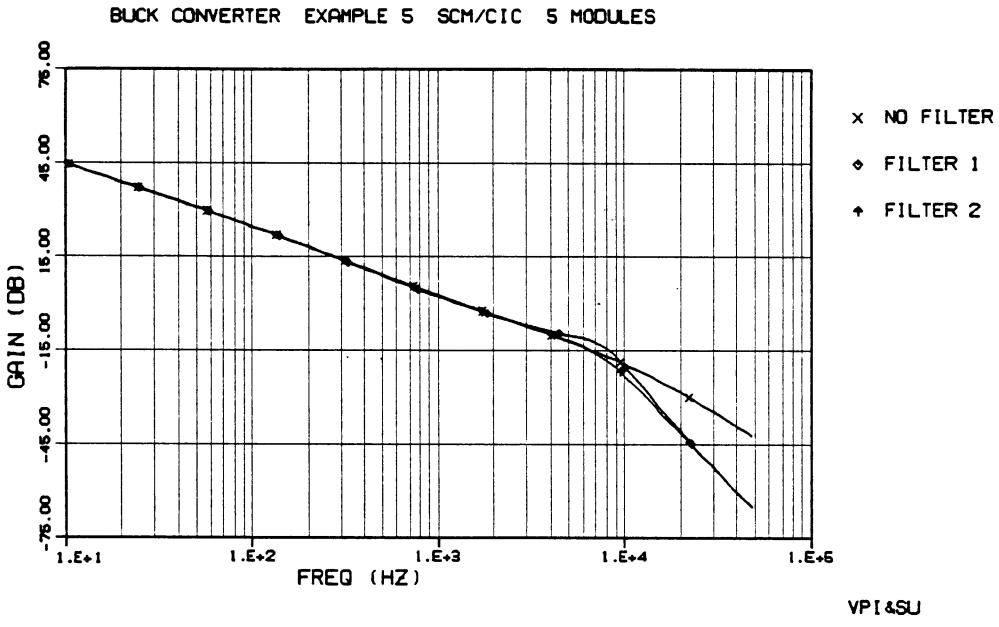


Figure 8.27: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. Loop Gain, T_1.



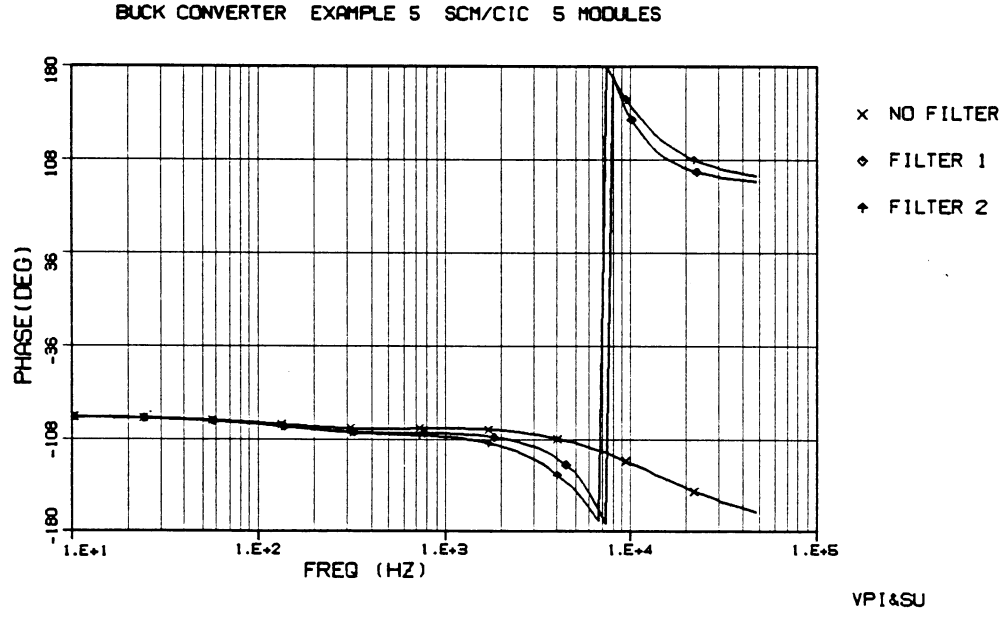
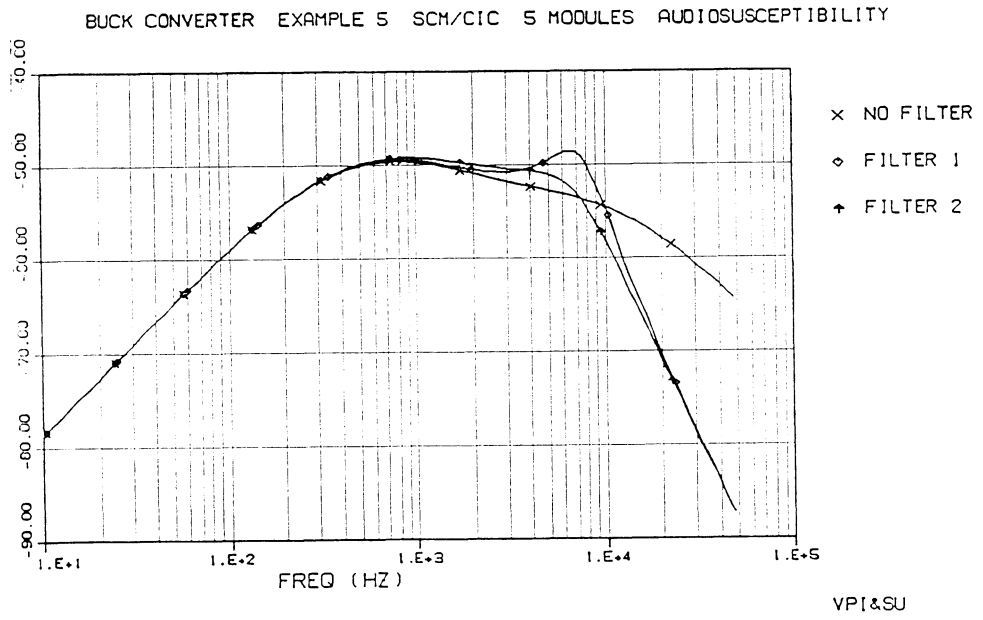


Figure 8.28 Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. Loop Gain, T_2.



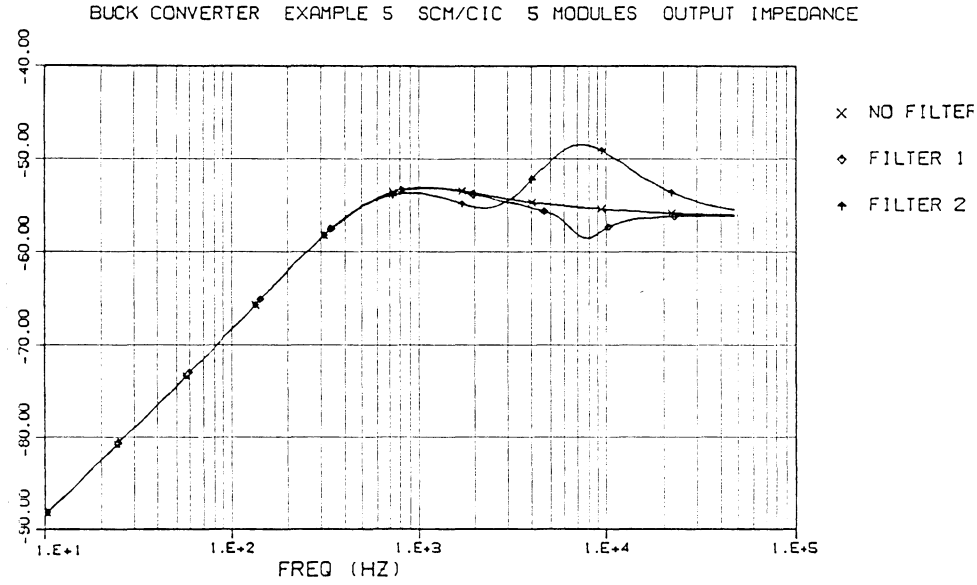


Figure 8.29: Design Example 5 - Buck Converter, 5 Parallel Modules with SCM/CIC Control. Audiosusceptibility and Output Impedance.

8.6 Conclusions

The design examples presented in this chapter show the procedures for SCM, CIC and SCM/CIC design for single or multiple modules are actually straightforward. Although the design procedures may appear somewhat tedious, it should be apparent that the use of this approach is far quicker and more productive than the customary trial and error approach to design. It can also be seen that the design procedures are very amenable to computer automation, leaving the burden of the tedious calculation to the computer. The designer's role is then in the intelligent choice of design specifications and in the trade-off of stability and other small-signal performance measures.

Chapter 9

Conclusions

In this thesis, the small-signal model has been developed for an arbitrary number of parallel buck power modules. Loop gains of the resulting power system have been defined and analyzed to investigate the stability issue of parallel power modules. The analysis procedures developed for the transfer function and loop gain derivations are directly applicable to boost, buck/boost and other types of converters, and similar results are to be expected.

It has been shown that the small-signal performance of the parallel buck converter modules is independent of the switching sequence of each module (assuming constant frequency operation). It has also been demonstrated that the system stability is relatively insensitive to input voltage variations between each of the different modules when using current-mode control.

Different forms of current-mode control, SCM and CIC, have been analyzed and compared to show their similarities and differences in terms of both small-signal performance and practical application. A new control scheme is proposed for high-current, parallel power modules which combines the merits of both types of current-mode control. For single module, high-current applications, it has been shown that the use of SCM, with auxiliary current limiting, is preferable to obtain the best small-signal performance.

With the relationships between the different control schemes analyzed and understood, simple definitions have been made to allow the unification of design procedures to be used for SCM, CIC or combined

SCM/CIC for single or parallel power converter modules. These design procedures also offer guidance in the choice of an external ramp and choice of the current-loop components.

The effects of a secondary LC filter used on the output of the power stage have been analyzed in detail, leading to an optimal design approach for the filter. The filter components may then be chosen to give maximum attenuation without sacrificing stability of the system or compromising the output impedance. The results obtained for the secondary filter are directly applicable to other power stage topologies.

The use of the control-loop design procedures have been demonstrated with some practical examples, and the resulting small-signal results obtained from the analysis program confirm the transfer function and loop gain analysis developed earlier in the thesis. The examples also demonstrate the use of the different current-mode control schemes and show how a power stage may be constructed from parallel power modules without changing the small-signal performance.

Suggestions for Future Work

Further analysis work is required to fully characterize the use of parallel modules for other power stage topologies and for different duty-cycle modulation control schemes.

Large-signal verification of the results obtained and of the design procedures is required to demonstrate the performance. (Some of this work verifying the design examples developed in this thesis, has been performed under a grant from IBM, Poughkeepsie.) Hardware implementation and ver-

ification of the small- and large-signal simulation measurements is also desirable.

The design procedures developed require familiarity with their derivation and are somewhat tedious to use. Programming of these results into a computer is a fairly straightforward task which would provide a valuable design tool for power supply engineers. (This is an on-going project with IBM, Endicott.)

Appendix A

Small-Signal Transfer Functions for Parallel Buck Modules

A.1 Evaluation of $(sI-A)^{-1}$ for k Parallel Buck Modules

The A matrix for k parallel buck power converters is a (k+1) by (k+1) matrix as given below.

$$A = \begin{bmatrix} -R_e/L & -R_c/L & -R_c/L & \cdots & -R_c/L & -1/L \\ -R_c/L & -R_e/L & -R_c/L & \cdots & -R_c/L & -1/L \\ -R_c/L & -R_c/L & -R_e/L & \cdots & -R_c/L & -1/L \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ -R_c/L & -R_c/L & -R_c/L & \cdots & -R_e/L & -1/L \\ 1/C & 1/C & 1/C & \cdots & 1/C & -1/CR_L \end{bmatrix}$$

We need to find the matrix $(sI-A)^{-1}$ in order to evaluate the system transfer functions.

$$(sI - A) = \begin{bmatrix} s+R_e/L & R_c/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & s+R_e/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & R_c/L & s+R_e/L & \cdots & R_c/L & 1/L \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ R_c/L & R_c/L & R_c/L & \cdots & s+R_e/L & 1/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & s+1/CR_L \end{bmatrix}$$

The first task is to find the determinant of the matrix (sI-A). In order to simplify this procedure, we first subtract the second row of the matrix from the first, the third row from the second, up to subtracting the (k-1) row from the (k-2) row. The determinant is then equal to:

$$\begin{vmatrix} s+R_1/L & -(s+R_1/L) & 0 & \cdots & 0 & 0 \\ 0 & s+R_1/L & -(s+R_1/L) & \cdots & 0 & 0 \\ 0 & 0 & s+R_1/L & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 0 & 0 & 0 & s+R_1/L & -(s+R_1/L) & 0 \\ R_c/L & R_c/L & R_c/L & \cdots & s+R_e/L & 1/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & s+1/CR_L \end{vmatrix}$$

Now we add the first column to the second column, the resulting second column to the third column, up to adding the (k-2) column to the (k-1) column. The resulting determinant is then:

$$\begin{vmatrix} s+R_1/L & 0 & 0 & \cdots & 0 & 0 \\ 0 & s+R_1/L & 0 & \cdots & 0 & 0 \\ 0 & 0 & s+R_1/L & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 0 & 0 & 0 & s+R_1/L & 0 & 0 \\ R_c/L & 2R_c/L & 3R_c/L & \cdots & s+R_e'/L & 1/L \\ -1/C & -2/C & -3/C & \cdots & -k/C & s+1/CR_L \end{vmatrix}$$

where $R_e' = R_1 + kR_c$

The value of this determinant can now be evaluated by inspection:

$$\det(sI-A) = \left(s + \frac{R_1}{L}\right)^{k-1} \left(s + \frac{R_e'}{L}\right)\left(s + \frac{1}{CR_L} + \frac{k}{LC}\right)$$

Assuming that $R_e' << kR_L$, this can be simplified to:

$$\det(sI-A) = \left(s + \frac{R_1}{L}\right)^{k-1} \left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)$$

We now need to determine the cofactors of (sI-A). Since the last row of the B matrix will always be zero for the buck converter, it is not necessary to evaluate the last column of $(sI-A)^{-1}$, and hence the last row of cofactors need not be found. Also, since the (sI-A) matrix is highly symmetrical, inspection of its form shows that there will only be three different values for all of the cofactors, equal to either $cof_{11}(sI-A)$, $cof_{12}(sI-A)$, and $cof_{1k+1}(sI-A)$. The other cofactors are related by:

$$cof_{ij} = cof_{12} \qquad \text{for every } j = i \text{ and } i, j < k + 1$$

$$cof_{ii} = cof_{11} \qquad \text{for every } i < k + 1$$

$$cof_{ik+1} = cof_{1k+1} \qquad \text{for every } i < k + 1$$

The next task is to determine the values of the three cofactors $cof_{12}(sI-A)$, $cof_{11}(sI-A)$ and $cof_{1k+1}(sI-A)$.

The value of the $cof_{11}(sI-A)$ is given by the value of the determinant of the following k x k matrix:

$$\begin{vmatrix} s+R_e/L & R_c/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & s+R_e/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & R_c/L & s+R_e/L & \cdots & R_c/L & 1/L \\ \cdot & \cdot & \cdot & & \cdot & \cdot \\ \cdot & \cdot & \cdot & & \cdot & \cdot \\ R_c/L & R_c/L & R_c/L & \cdots & s+R_e/L & 1/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & s+1/CR_L \end{vmatrix}$$

Notice that this determinant is exactly the same as the determinant of (sI-A), except that the order of the matrix is reduced by 1. Hence, the value of this cofactor can immediately be written as:

$$\text{cof}_{11} = \left(s + \frac{R_1}{L}\right)^{k-2} \left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}\right)$$

where $R_e'' = R_1 + (k-1)R_c$

The value of $\text{cof}_{12}(sI-A)$ is given by the value of the determinant of the following k x k matrix:

$$\text{cof}_{12} = - \begin{vmatrix} R_c/L & R_c/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & s+R_e/L & R_c/L & \cdots & R_c/L & 1/L \\ R_c/L & R_c/L & s+R_e/L & \cdots & R_c/L & 1/L \\ \cdot & \cdot & \cdot & & \cdot & \cdot \\ \cdot & \cdot & \cdot & & \cdot & \cdot \\ R_c/L & R_c/L & R_c/L & \cdots & s+R_e/L & 1/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & s+1/CR_L \end{vmatrix}$$

Using similar reduction techniques as before, this can be simplified as:

$$\text{cof}_{12} = -\begin{vmatrix} 0 & -(s+R_1/L) & 0 & \cdots & 0 & 0 \\ 0 & 0 & -(s+R_1/L) & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -(s+R_1/L) & 0 \\ R_c/L & R_c/L & R_c/L & \cdots & s+R_e/L & 1/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & s+1/CR_L \end{vmatrix}$$

If we let $a = s+R_1/L$, the value of this determinant is then:

$$\text{cof}_{12} = -[(-1)^k \frac{R_c}{L}(s + \frac{1}{CR_L})(-a)^{k-2}\frac{1}{L} + (-1)^{k-1}(\frac{-1}{LC})(-a)^{k-2}]$$

$$= -a^{k-2}(s + \frac{1}{CR_L})\frac{R_c}{L} + \frac{1}{LC}$$

Assuming $R_c << R_L$ and substituting for a, we obtain:

$$\text{cof}_{12} = -(s + \frac{R_1}{L})^{k-2}(s\frac{R_c}{L} + \frac{1}{LC})$$

The value of $cof_{1k+1}(sI-A)$ is given by the value of the determinant of the following k x k matrix:

$$\begin{vmatrix} R_c/L & s+R_e/L & R_c/L & \cdots & R_c/L & R_c/L \\ R_c/L & R_c/L & s+R_e/L & \cdots & R_c/L & R_c/L \\ R_c/L & R_c/L & R_c/L & \cdots & R_c/L & R_c/L \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ R_c/L & R_c/L & R_c/L & \cdots & R_c/L & s+R_e/L \\ -1/C & -1/C & -1/C & \cdots & -1/C & -1/C \end{vmatrix}$$

Using similar reduction techniques as before, this can be simplified as:

$$cof_{1k+1}=(-1)^k \begin{vmatrix} 0 & s+R_1/L & 0 & \cdots & 0 & 0 \\ 0 & 0 & s+R_1/L & \cdots & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & s+R_1/L & 0 \\ R_c/L & R_c/L & 2R_c/L & \cdots & (k-2)R_c/L & s+R_e''/L \\ -1/C & -1/C & -2/C & \cdots & -(k-2)/C & -(k-1)/C \end{vmatrix}$$

Again, letting $a = s+R_1/L$, the value of this cofactor is:

$$cof_{1k+1} = (-1)^k \frac{R_c}{LC} (-1)^k a^{k-2}(-1)(k-1) + (-1)^{k-1} \frac{-1}{C} a^{k-2}(s + \frac{R_e''}{L})$$

$$= a^{k-2} \left[-\frac{R_c}{LC}(k-1) + \frac{s}{C} + \frac{R_e''}{LC} \right]$$

$$= a^{k-2} \left[-\frac{R_c}{LC}(k-1) + \frac{s}{C} + \frac{R_1}{LC} + \frac{R_c}{LC}(k-1) \right]$$

$$= \left(s + \frac{R_1}{L}\right)^{k-2} \left(s\frac{1}{C} + \frac{R_1}{LC}\right)$$

$$= \frac{1}{C}\left(s + \frac{R_1}{L}\right)^{k-1}$$

We now know all of the required cofactors of (sI-A) to be able to find the transfer functions, and after cancelling common terms in the cofactors and determinant, $(sI-A)^{-1}$ can be written as:

$$(sI-A)^{-1} = 1/D(s) \begin{bmatrix} a_{11} & a_{12} & a_{12} & \cdots & a_{12} & x \\ a_{12} & a_{11} & a_{12} & \cdots & a_{12} & x \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ a_{12} & a_{12} & a_{12} & \cdots & a_{11} & x \\ a_{1k+1} & a_{1k+1} & a_{1k+1} & \cdots & a_{1k+1} & x \end{bmatrix}$$

where $$a_{11} = s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}$$

$$a_{12} = -s\frac{R_c}{L} + \frac{1}{LC}$$

$$a_{1k+1} = \frac{1}{C}s + \frac{R_1}{L}$$

$$D(s) = \left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)$$

x values are not needed and undetermined.

A.2 Evaluation of Transfer Function Blocks

A.2.1 Input-to-Output Transfer Function, v_o/v_{gi}

The transfer function for the ith-input-to-output is given by:

$$\frac{v_o}{v_{gi}} = C(sI-A)^{-1}B$$

where $C = \begin{bmatrix} R_c & R_c & \cdots & R_c & 1 \end{bmatrix}$ $\quad B = \begin{bmatrix} D_i/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$

$$(sI-A)^{-1}B = D_i/L \; \frac{\begin{bmatrix} s^2+s(R_e''/L+1/CR_L)+(k-1)/LC \\ -sR_c/L + 1/LC \\ \vdots \\ -sR_c/L + 1/LC \\ 1/C\,(s + R_1/L) \end{bmatrix}}{D(s)}$$

$$C(sI-A)^{-1}B = \frac{D_i}{L}\frac{\left(R_c\, s^2+s\left[\frac{R_e}{L}+\frac{1}{CR_L}\right]+\frac{(k-1)}{LC} - (k-1)\left[s\,\frac{R_c}{L}+\frac{1}{LC}+\frac{s}{C}+\frac{R_1}{L}\right]\right)}{D(s)}$$

$$= \frac{D_i}{L}\frac{\left(R_c\, s^2 + s\left[\frac{R_cR_1}{L}+\frac{1}{C}\right]+\frac{R_1}{LC}\right)}{D(s)}$$

$$= \frac{D_i}{L} \frac{\left(s + \frac{R_1}{L}\right)\left(sR_c + \frac{1}{C}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

Hence, $$\frac{v_o}{v_{gi}} = \frac{D_i}{L} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

A.2.2 Input-to-Inductor-Current Transfer Function, i_{li}/v_{gi}

By nature of the symmetry of the circuit, all of the inductor currents will have the same input-to-output and duty-cycle-to-output transfer functions as each other. Hence, the transfer function, i_{li}/v_{gi}, will be equal to i_{l1}/v_{g1} for all i.

The ith-input-to-ith-inductor-current transfer function is given by:

$$i_{li}/v_{gi} = C(sI-A)^{-1}B$$

where $C = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \end{bmatrix}$ $B = \begin{bmatrix} D_i/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$

$$C(sI-A)^{-1}B = \frac{D_i}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}\right)}{D(s)}$$

Hence, $$\frac{i_{li}}{v_{gi}} = \frac{D_i}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

A.2.3 Input-to-Inductor-Current Transfer Function, i_{li}/V_{gj}.

The transfer function for the jth-input-to-ith-inductor-current, where i = j, is given by:

$$\frac{i_{li}}{V_{gj}} = C(sI-A)^{-1}B$$

where $C = \begin{bmatrix} 1 & 0 & \ldots & 0 & 0 \end{bmatrix}$ $B = \begin{bmatrix} 0 \\ Dj/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$

$$C(sI-A)^{-1}B = \frac{-D_j}{L} \frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{D(s)}$$

Hence, $$\frac{i_{li}}{v_{gj}} = \frac{-D_j}{L} \frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

A.2.4 Duty-Cycle-to-Output Transfer Function, v_o/d_i.

The transfer function for the ith-duty-cycle-to-output is given by:

$$\frac{v_o}{d_i} = C(sI-A)^{-1}B$$

where $C = \begin{bmatrix} R_c & R_c & \cdots & R_c & 1 \end{bmatrix}$ $B = \begin{bmatrix} V_{gi}/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$

$$(sI-A)^{-1}B = \frac{V_{gi}}{L} \frac{\begin{bmatrix} (s^2+s(R_e''/L + 1/CR_L)+(k-1)/LC) \\ - sR_c/L + 1/LC \\ \vdots \\ - sR_c/L + 1/LC \\ 1/C(s + R_1/L) \end{bmatrix}}{D(s)}$$

$$C(sI-A)^{-1}B = \frac{V_{gi}}{L} \frac{\left(R_c\, s^2+s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right]+ \frac{(k-1)}{LC}-(k-1)\left[s\,\frac{R_c}{L} + \frac{1}{LC}\right]+\left[\frac{s}{C} + \frac{R_1}{L}\right]\right)}{D(s)}$$

$$= \frac{V_{gi}}{L} \frac{\left(R_c\, s^2 + s\left[\frac{R_cR_1}{L} + \frac{1}{C}\right]+\frac{R_1}{LC}\right)}{D(s)}$$

$$= \frac{V_{gi}}{L} \frac{\left(s + \frac{R_1}{L}\right)\left(sR_c + \frac{1}{C}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

Hence, $$\frac{v_o}{d_i} = \frac{D_i}{L} \frac{\left(R_c s + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

A.2.5 Duty-Cycle-to-Inductor-Current Transfer Function, i_{li}/d_i.

The transfer function for the ith-duty-cycle-to-ith-inductor-current is given by:

$$\frac{i_{li}}{d_i} = C(sI-A)^{-1}B$$

where $\left[C = 1 \quad 0 \quad . \quad . \quad . \quad . \quad 0 \quad 0\right]$ $\quad B = \begin{bmatrix} V_{gi}/L \\ 0 \\ . \\ . \\ 0 \end{bmatrix}$

$$C(sI-A)^{-1}B = \frac{V_{gi}}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}\right)}{D(s)}$$

Hence, $$\frac{i_{li}}{v_{gj}} = \frac{V_{gi}}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{k-1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

A.2.6 Duty-Cycle-to-Inductor-Current Transfer Function, i_{li}/d_j.

The transfer function for the jth-duty-cycle-to-ith-inductor-current, where i = j, is given by:

$$\frac{i_{li}}{d_j} = C(sI-A)^{-1}B$$

where $C = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \end{bmatrix}$ $B = \begin{bmatrix} 0 \\ V_{gj}/L \\ 0 \\ \vdots \\ 0 \end{bmatrix}$

$$C(sI-A)^{-1}B = \frac{-V_{gj}}{L}\frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{D(s)}$$

Hence, $$\frac{i_{li}}{d_j} = \frac{-V_{gj}}{L}\frac{\left(s\frac{R_c}{L} + \frac{1}{LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

APPENDIX B

Loop Gain Derivation for k Parallel Buck Modules

The block diagram for k parallel buck converter modules is given in Figure 2.1. For the loop gain derivation, the input perturbation v_g is zero; so, the gain blocks F_2, F_3 and F_6 are not shown on this diagram. In order to derive the expressions for the voltage-loop gain, T_v, and the equivalent current-loop gain, T_i, for the parallel modules, loop gain T_2 at point b on the diagram is evaluated, where:

$$T_2 = \frac{T_v}{1 + T_i}$$

The loop gain, T_2, is given by the gain -y/x as shown on the block diagram. The value of y is given by:

$$y = F_v F_2 \sum_{i=1}^{k} d_i \tag{B.1}$$

and the duty-cycle perturbations are given by:

$$d_1 = -F_m\, x + F_i F_4 d_1 + F_i F_5 \sum_{i=2}^{k} d_i$$

$$\vdots \qquad\qquad \vdots$$

$$d_j = -F_m\, x + F_i F_4 d_j + F_i F_5 \sum_{\substack{i=1 \\ i \neq j}}^{k} d_i$$

$$\vdots \qquad\qquad \vdots$$

$$\dot{d}_k = -F_m x + F_i F_4 d_k + F_i F_5 \sum_{i=1}^{k-1} d_i$$

Adding the duty cycles together gives:

$$\sum_{i=1}^{k} d_i = -F_m kx + F_i F_4 \sum_{i=1}^{k} d_i + (k-1) F_i F_5 \sum_{i=1}^{k} d_i$$

$$\sum_{i=1}^{k} d_i [1 + F_m F_i (F_4 + (k-1)F_5)] = -F_m kx$$

so

$$\sum_{i=1}^{k} d_i = \frac{-F_m}{1 + F_m F_i [F_4 + (k-1)F_5]} \qquad (B.2)$$

Substituting (B.2) into (B.1) gives:

$$y = \frac{-F_v F_2 F_m kx}{1 + F_m F_i [F_4 + (k-1)F_5]}$$

Loop gain T_2 can then be expressed as:

$$T_2 = -y/x = \frac{kF_m F_2 F_v}{1 + F_m F_i [F_4 + (k-1)F_5]}$$

Substituting for the transfer function F_2, the numerator of this expression becomes:

$$kF_mF_2F_v = F_mF_v\frac{kV_g}{L}\frac{\left(R_cs + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

If we let $L' = L/k$ and $R_{11} = R_1/k$

$$kF_mF_2F_v = F_mF_v\frac{V_g}{L'}\frac{\left(R_cs + \frac{1}{C}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)} \quad (B.3)$$

This is similar to the expression for the voltage-loop gain which is obtained for a single module with an equivalent inductance L/k and equivalent resistance R_1/k. However, modulator gain F_m is evaluated for the inductance of each of the individual modules and not that of the equivalent single power stage. The gain of F_m may be a function of inductance value depending on the type of control being used. For k converters, voltage-loop gain T_v is, therefore, defined as:

$$T_v = kF_mF_vF_2 \quad (B.4)$$

The loop gain at b can then be written as:

$$T_2 = \frac{T_v}{1 + F_mF_i[F_4 + (k-1)F_5]}$$

From the form of this equation, the equivalent current-loop gain can be written as:

$$T_i = F_m F_i [F_4 + (k-1)F_5]$$

$$= F_m F_i \frac{V_g}{L} \frac{\left(s^2 + s\left[\frac{R_e''}{L} + \frac{1}{CR_L}\right] + \frac{(k-1)}{LC} - (k-1)\left[s\frac{R_c}{L} + \frac{1}{LC}\right]\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

$$= F_m F_i \frac{V_g}{L} \frac{\left(s^2 + s\left[\frac{R_1}{L} + \frac{1}{CR_L}\right]\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

For frequencies well above $R_1/(R_L\sqrt{LC})$, this can be approximated by:

$$T_i = F_m F_i \frac{V_g}{L} \frac{\left(s^2 + s\left[\frac{R_1}{L} + \frac{1}{CR_L}\right] + \frac{R_1}{R_L LC}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

$$= F_m F_i \frac{V_g}{L} \frac{\left(s + \frac{R_1}{L}\right)\left(s + \frac{1}{CR_L}\right)}{\left(s + \frac{R_1}{L}\right)\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

$$= F_m F_i \frac{V_g}{L} \frac{\left(s + \frac{1}{CR_L}\right)}{\left(s^2 + s\left[\frac{R_e'}{L} + \frac{1}{CR_L}\right] + \frac{k}{LC}\right)}$$

$$= F_m F_i \frac{V_g}{kL'} \frac{\left(s + \frac{1}{CR_L}\right)}{\left(s^2 + s\left[\frac{R_{11} + R_c}{L'} + \frac{1}{CR_L}\right] + \frac{1}{L'C}\right)} \qquad (B.5)$$

This is the same expression obtained for the current-loop gain of a single module with k parallel inductors, with the exception of the lead coefficient, $F_m F_i/k$.

B.2 Loop Gain of Two Converters with Different Input Voltages

The transfer-function block diagram for two converters is shown in Figure 3.3. The input voltage of the first converter is assumed to be V_g, and that of the second converter to be $V_{g1} = mV_g$ where m is an arbitrary constant. From the expressions for F_2, F_4, and F_5 derived in Appendix A, the effect on each of these transfer functions is direct multiplication by the value of m. The transfer-function blocks affected by the different input voltages are marked on the block diagram. The gain of F_m for the second converter is also affected by the input voltage, and this is changed by a factor m_1, the value of which depends on the type of control being used.

The small-signal block diagram may be manipulated to take into account the input voltage differences with a single factor K multiplying the pulse-modulator gain, F_m, where $K = mm_1$.

If the disparity in input voltages is known to be a constant for a given system design (as may be the case for parallel power converters operating from different power sources such as a battery and a solar array) the effect on the overall loop gain can be nulled by adjusting the modulator gain of each power module such that K = 1. The difference in input voltages will then have no effect on the loop gains of the system.

If the gains of F_m are not adjusted, the loop gain analysis at b can proceed in a similar manner as before. The loop gain at point b is given by $T_2 = -y/x$. the value of y is:

$$y = F_v F_2 (d_1 + d_2) \tag{B.6}$$

Duty cycles d_1 and d_2 are given by:

$$d_1 = -F_m(F_i F_4 d_1 + F_i F_5 d_2 + x)$$

$$d_2 = -KF_m(F_i F_4 d_2 + F_i F_5 d_1 + x)$$

Rearranging,

$$d_1(1 + F_m F_i F_4) = -F_m(F_i F_5 d_2 + x)$$

$$d_2(1 + KF_m F_i F_4) = -KF_m(F_i F_5 d_2 + x)$$

Letting $T_4 = F_m F_i F_4$ and $T_5 = F_m F_i F_5$, then:

$$d_1 = \frac{-T_5 d_2 - F_m x}{1 + T_4} \tag{B.7}$$

$$d_2 = \frac{-KT_5 d_1 - KF_m x}{1 + KT_4} \tag{B.8}$$

Letting $K_1 = 1/K$, then:

$$d_2 = \frac{-T_5 d_1 - F_m x}{K_1 + T_4}$$

Substituting for d_2 in Equation B.7:

$$d_1 = \frac{-T_5}{1 + T_4}\left(\frac{-T_5\, d_1 - F_m x}{K_1 + T_4}\right) - \frac{F_m x}{1 + T_4}$$

Rearranging and simplifying, we obtain:

$$d_1 = \frac{F_m[T_5 - (K_1 + T_4)]x}{(1 + T_4)(K_1 + T_4) - T_5^2} \qquad (B.9)$$

Similarly, d_2 can be derived to obtain:

$$d_2 = \frac{F_m[T_5 - (1 + T_4)]x}{(K_1 + T_4)(1 + T_4) - T_5^2} \qquad (B.10)$$

Adding (B.9) and (B.10), and substituting into (B.6):

$$y = \frac{F_m F_2 F_v[T_5 - (K_1 + T_4) + T_5 - (1 + T_4)]\, x}{(K_1 + T_4)(1 + T_4) - T_5^2}$$

$$= \frac{F_m F_2 F_v[2(T_5 - T_4) - (K_1 + 1)]}{K_1 + (K_1 + 1)T_4 + T_4^2 - T_5^2}$$

$$= \frac{F_m F_2 F_v \quad [2(T_5 - T_4) - (K_1 + 1)]}{[K_1 + (K_1 + 1)T_4 + T_4^2 - T_5^2]}$$

The voltage-loop gain for the two parallel converters is given by

$$T_v = (1 + 1/K_1)\, F_m F_v F_2 \tag{B.11}$$

and since $T_2 = -y/x$, the loop gain may be expressed as:

$$T_2 = T_v \frac{[2(T_4 - T_5) + (K_1 + 1)]}{[K_1 + (K_1 + 1)T_4 + T_4^2 - T_5^2][1 + 1/K_1]}$$

The equivalent current-loop gain for the two converters may then be found from:

$$1 + T_i = \frac{[K_1 + (K_1 + 1)T_4 + T_4^2 - T_5^2][1 + 1/K_1]}{2(T_4 - T_5) + (K_1 + 1)}$$

expanding and simplifying, we obtain:

$$T_i = \frac{T_4(1 + KT_4 + K^2 + K^2T_4) - T_5K(2 - T_5 - KT_5)}{1 + K + 2KT_4 - 2KT_5} \tag{B.12}$$

Further reduction of this expression cannot be done for an arbitrary K. For the special case of K = 1 (i.e. equal input voltages, or gains adjusted to nullify the effect of different of different input voltages) the expression reduces as expected:

$$T_i = \frac{T_4\ (1 + T_4 + 1 + T_4) + T_5(2 - T_5 - T_5)}{1 + 1 + 2T_4 - 2T_5}$$

$$= \frac{T_4(2 + 2T_4) + T_5(2 - 2T_5)}{2 + 2T_4 - 2T_5}$$

$$= \frac{T_4 + T_4^2 + T_5 - T_5^2}{1 + T_4 - T_5}$$

$$= \frac{(T_4 + T_5)(1 + T_4 - T_5)}{(1 + T_4 - T_5)}$$

$$= T_4 + T_5$$

B.3 High-Frequency Behavior of Current Loop Gain

The expression for current-loop gain in Equation B.12 can be simplified by making some further assumptions. As discussed in the chapter on control loop design, the importance of the current loop lies in the higher frequency area greater than the resonant frequency of the power supply filter. Below the resonant frequency, the voltage-feedback loop gain, T_v, is much larger than the current-loop gain. The important properties of the current-loop gain are its high frequency crossover and its 90 degree phase at frequencies above the resonant frequency.

From the expressions of T_4 and T_5, some approximations can be made for higher operating frequencies.

For $s > w0$, $T_5 << T_4$ and $T_4 = A/s$

Hence, for high frequency, Equation B.12 can be simplified to give:

$$T_i = \frac{T_4(1 + KT_4 + K^2 + K^2T_4)}{1 + K + 2KT_4}$$

$$= \frac{T_4[(1 + K^2) + T_4(K + K^2)]}{1 + K + 2KT_4} \qquad (B.13)$$

Picking the extreme value for K of 4, which is unlikely to be exceeded in a practical application,

$$T_i = \frac{T_4(1 + 4A/s + 16 + 16A/s)}{(1 + 4 + 8A/s)}$$

$$= T_4\frac{(17 + 20A/s)}{(5 + 8A/s)}$$

$$= 3.4\ T_4\ \frac{(s + 1.18A)}{(s + 1.6A)}$$

It can be seen from this expression that the effect of increasing the gain of F_m by a factor of 4 is that the current gain is increased and a

closely-spaced pole-zero pair is introduced. The magnitude of the voltage-loop gain is also increased, in this example by a factor of 2.5 over that of the two modules with equal input voltages. This analysis shows that the high frequency characteristics of the closely spaced pole-zero pair will not affect the characteristics of the current loop significantly, and if such a second-order effect exists, it is not detrimental since the zero occurs before the pole providing a slight increase in phase margin.

APPENDIX C

EASY5 Computer Model for Small-Signal Analysis of Parallel Power Modules

The computer package used to perform the small-signal analysis of the parallel power modules was the EASY5 package. Detailed descriptions of this software package may be found in Reference [5] and a presentation of the two-port model generation approach for the switching converter cell and other macros used in the model definition may be found in Reference [6].

Figure C.1 shows the EASY5 model block diagram for the first converter module with input filter, output filter and load. Summing blocks are used to allow the connections of subsequent power modules, shown in the block diagrams of Figures C.2 through C.5. The model generation data file used to generate this system is given below, followed by the data file used to generate the plots of the Design Example 5 in Chapter 8. (Five buck power modules with a secondary filter, Filter 1 configuration.)

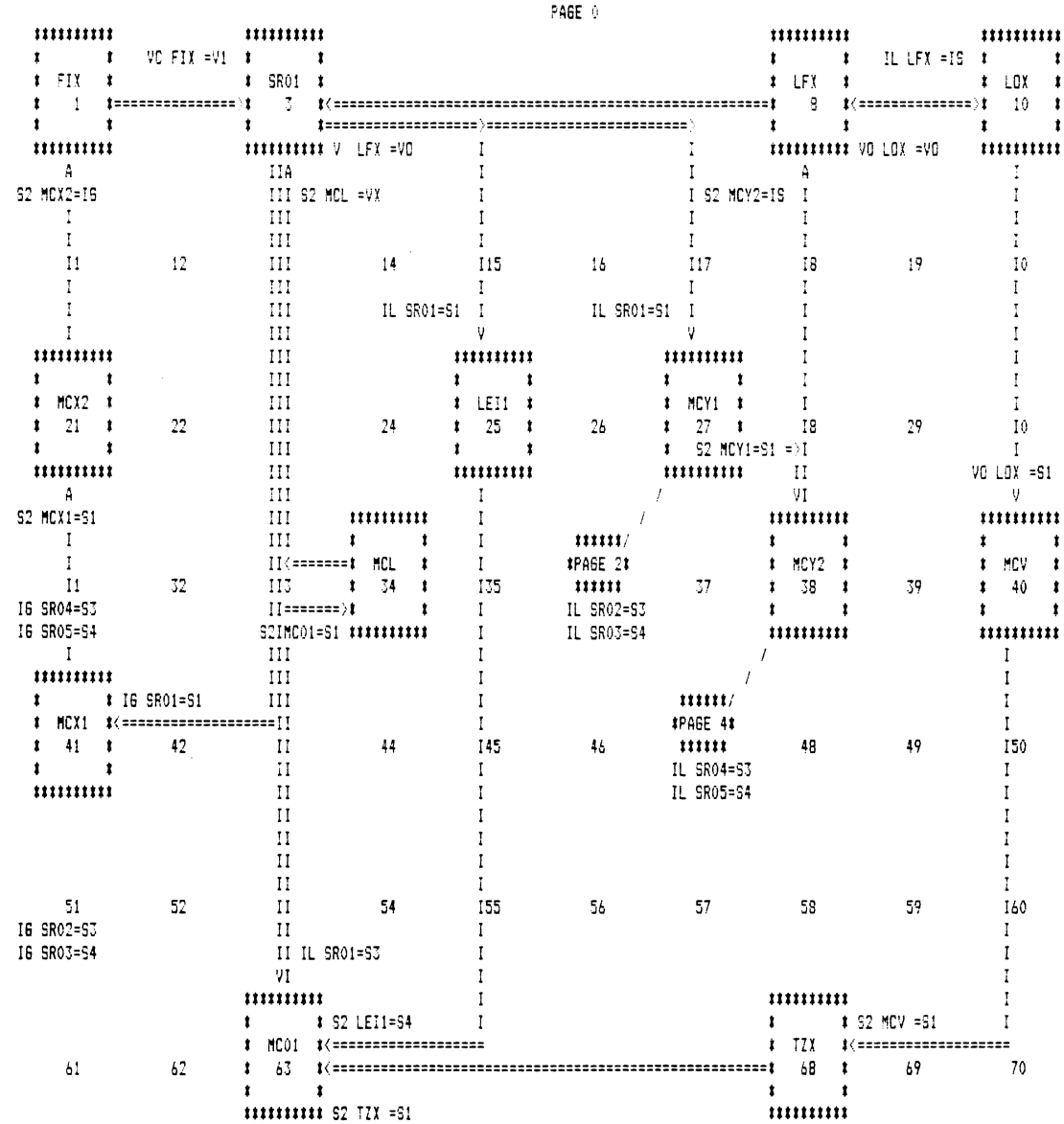


Figure C.1: EASY5 Block Diagram for Small-Signal Analysis of Parallel Buck Power Modules. First Power Module, with Input Filter, Output Filter, Load and Summing Blocks for Subsequent Modules.

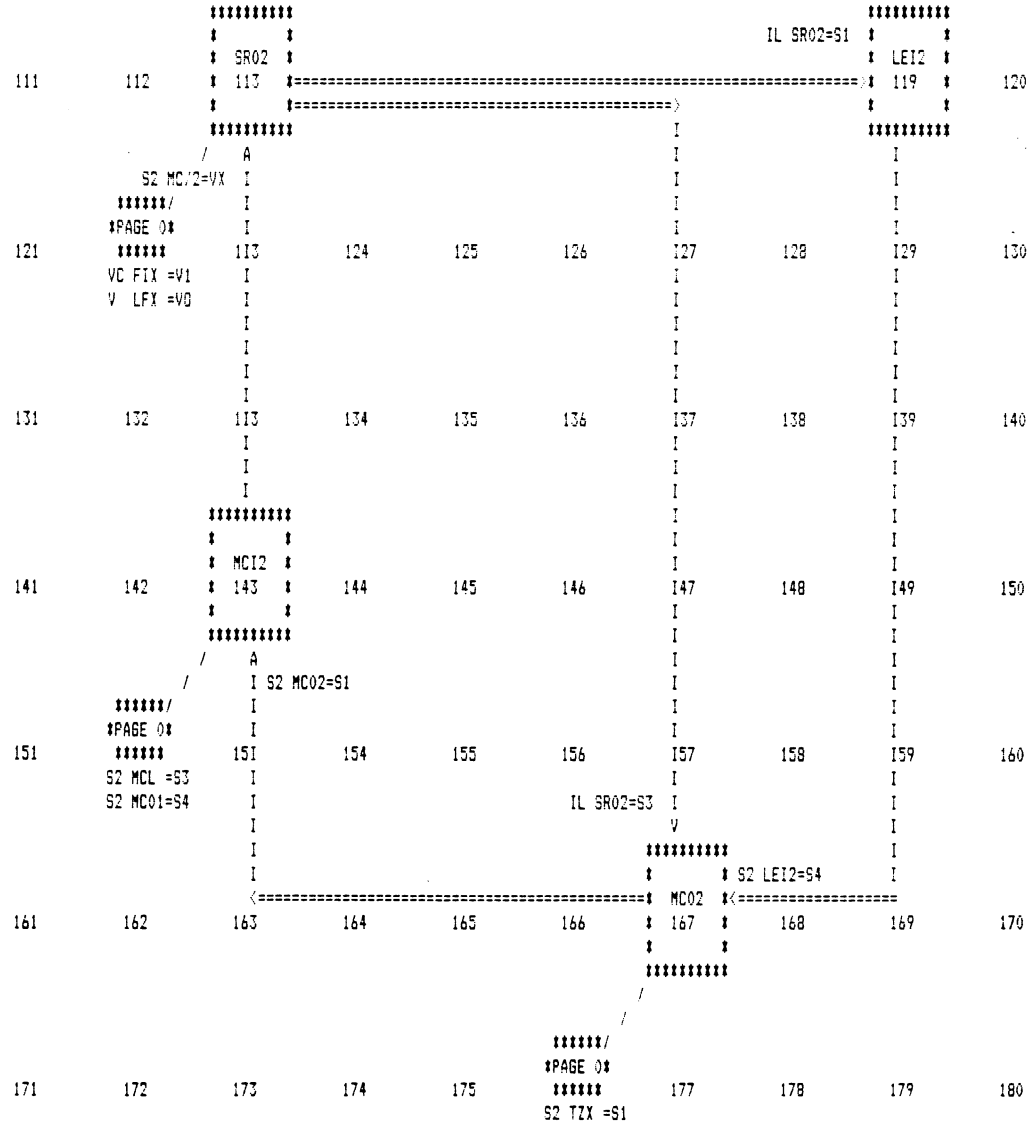


Figure C.2: EASY5 Block Diagram, Second Converter Module with Current-Mode Control Blocks.

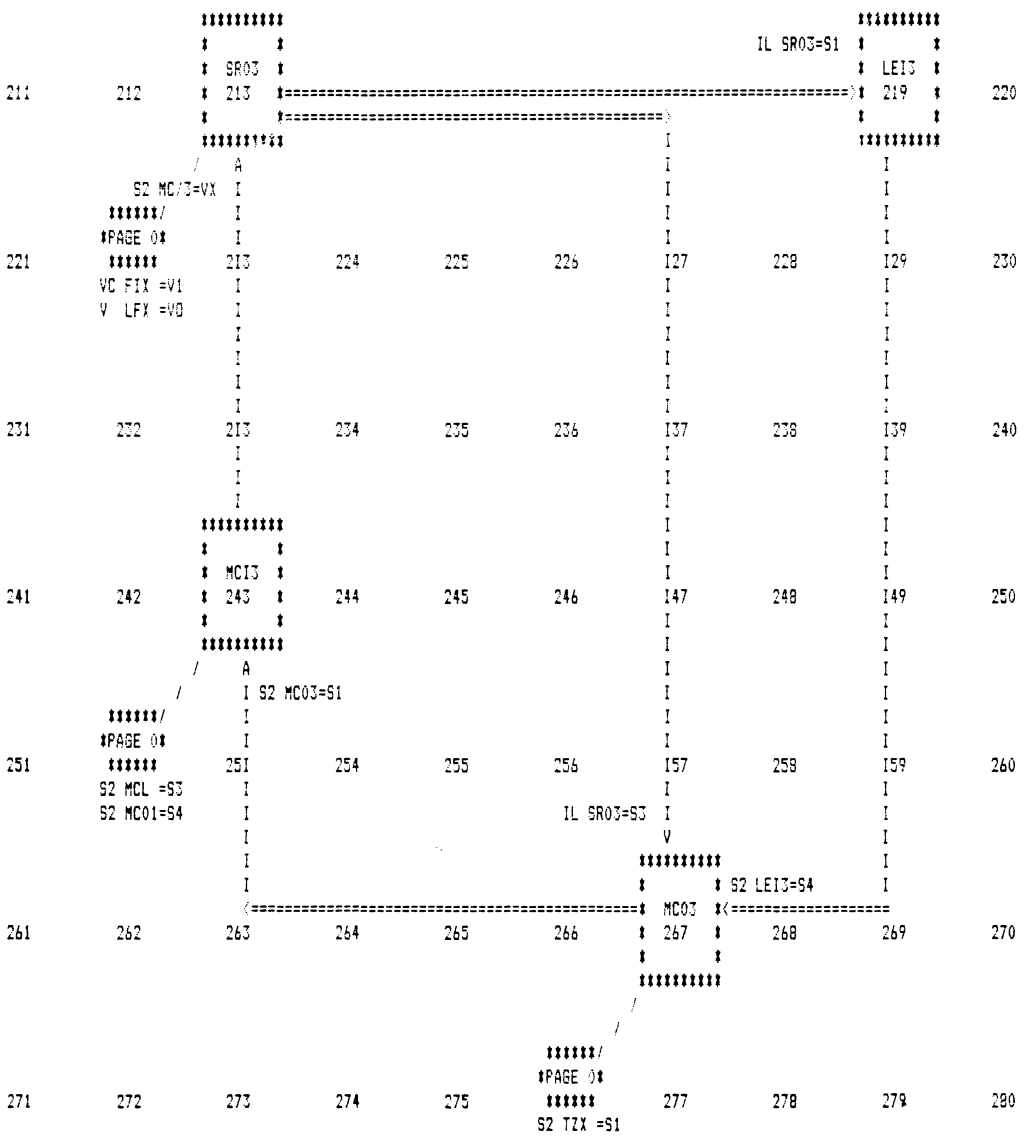


Figure C.3: EASY5 Block Diagram, Third Converter Module with Current-Mode Control Blocks.

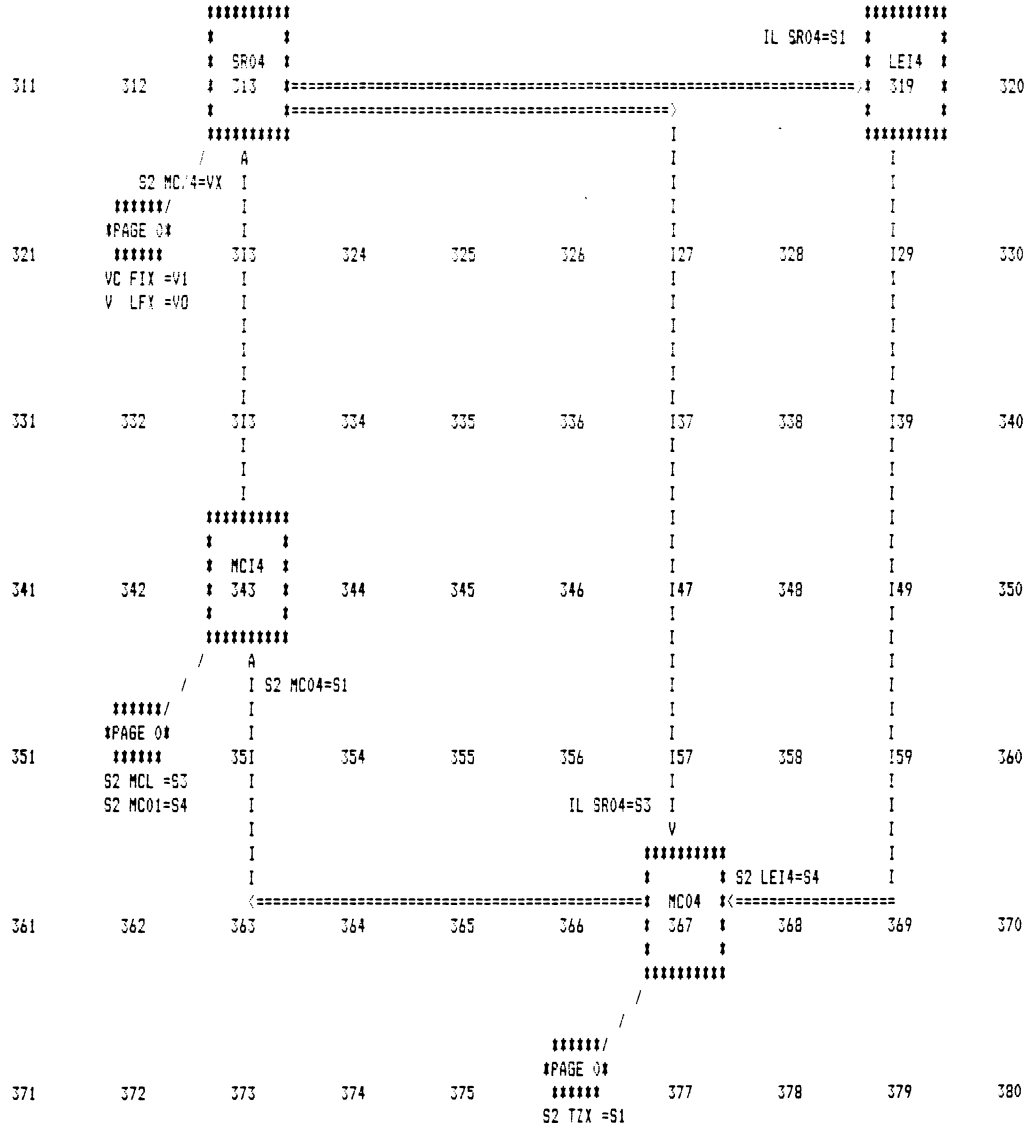


Figure C.4: EASY5 Block Diagram, Fourth Converter Module with Current-Mode Control Blocks.

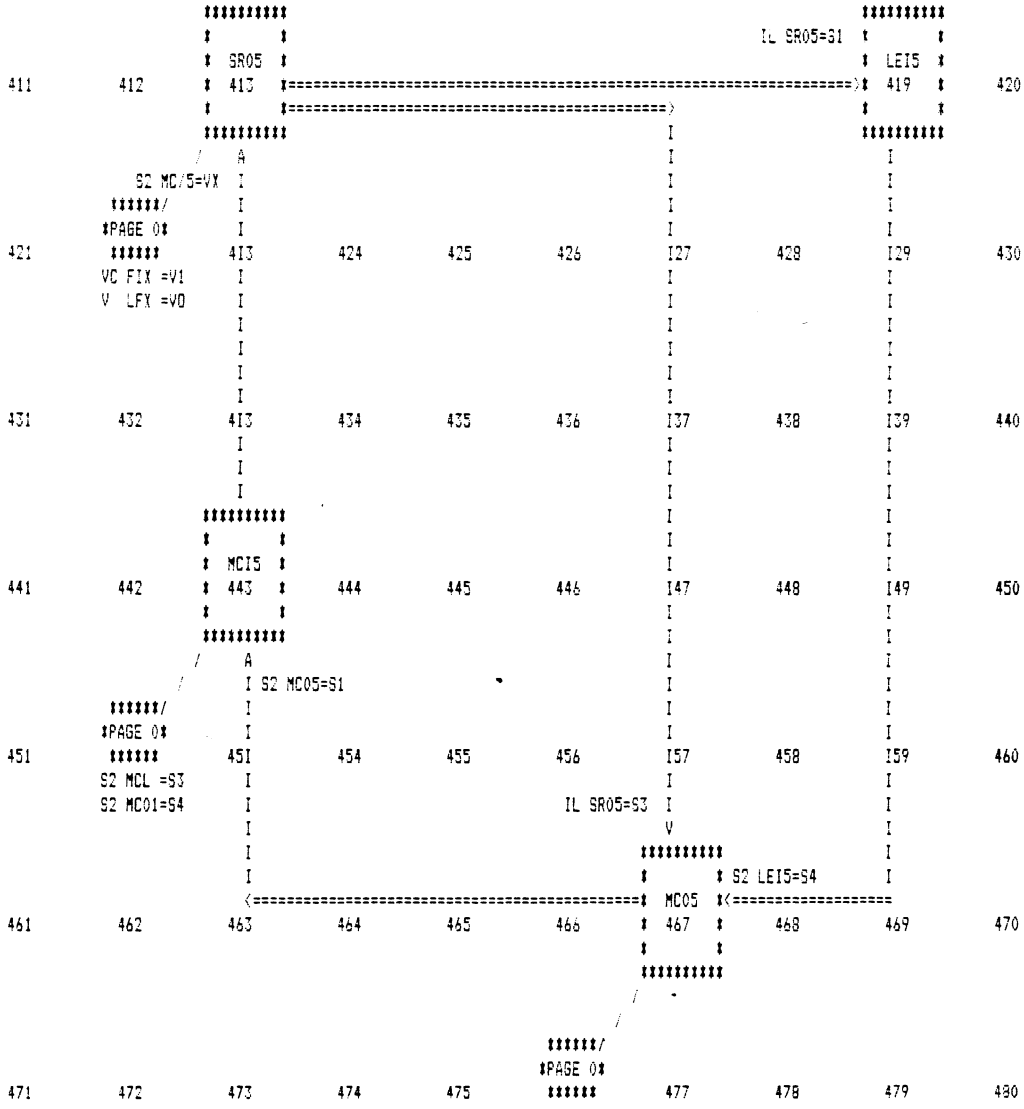


Figure C.5: EASY5 Block Diagram, Fifth Converter Module with Current-Mode Control Blocks.

```
PHASE 1. MODEL DESCRIPTION FILE INTERPRETATION PHASE
MACRO FILE NAME = MACROS

*****************************************************************************
** Define input filter macro. Present configuration is simple **
** undamped LC circuit.                                       **
*****************************************************************************

DEFINE MACRO   = FI
MACRO INPUTS   = VG     IG     L     C
MACRO OUTPUTS  = IL     VC
MACRO CODE
MACRO STOP SORT
MACRO DERIVATIVE,  IL FI-- = (VG FI-- - VC FI--)/L  FI--
MACRO DERIVATIVE,  VC FI-- = (IL FI-- - IG FI--)/C  FI--
MACRO RESUME SORT
END OF MACRO


*****************************************************************************
** Define switching regulator macro. SR--
** Inputs to macro:  L   Inductor
**                   VX  Duty cycle
**                   R   Load resistance
**                   N   Number of modules in parallel
**                   V1  Input voltage
**                   V1S Steady state input voltage
**                   VCS Steady state capacitor voltage
**                   VO  Output voltage of regulator macro
**
** Outputs of macro: IL  Inductor current
**                   IG  Input current
**                   ILS Steady state output current
*****************************************************************************
DEFINE MACRO  = SR
MACRO INPUTS  = L     VX    R     N     V1    V1S   VCS   VO
MACRO OUTPUTS = IL    IG    ILS
MACRO CODE
MACRO STOP SORT

               D = VCSSR-- / V1SSR--
               ILSSR-- = VCSSR-- / R  SR-- / N  SR--
               IG SR-- = D * IL SR-- + ILSSR-- * VX SR--
MACRO DERIVATIVE, IL SR-- = (-VO SR-- + V1 SR-- * D + V1SSR-- * VX SR--)
     & / L  SR--
MACRO RESUME SORT
END OF MACRO
```

```
*******************************************************************************
** Define second output filter stage macro.
** Inputs to macro:  IS   Current from power stages
**                   C    Filter capacitor
**                   L    Filter Inductor
**                   Rc   Capacitor ESR
**                   Rl   Inductor resistance
**                   VO   Output voltage of load block
** Outputs of macro: VC   Capacitor voltage
**                   IL   Inductor current
**                   V    Output voltage (with ESR)
**
*******************************************************************************
DEFINE MACRO  = LF
MACRO INPUTS  = IS    C     L     RC    RL    VO
MACRO OUTPUTS = VC    IL    V
MACRO CODE
MACRO STOP SORT
                V  LF-- = VC LF-- + RC LF-- * (IS LF-- - IL LF--)
MACRO DERIVATIVE, VC LF-- = (IS LF-- - IL LF--) / C  LF--
MACRO DERIVATIVE, IL LF-- = (VC LF-- + IS LF-- * RC LF--
     & -IL LF-- * (RC LF-- + RL LF--) - VO LF--)/L  LF--
MACRO RESUME SORT
END OF MACRO

*******************************************************************************
** Define output load macro.
** Inputs to macro:   IS   Total current into load
**                    C    Output filter capacitor
**                    Rc   Capacitor ESR
**                    R    Load resistor
**                    IO   Output current source
** Outputs of macro:  VC   Capacitor voltage
**                    VO   Load voltage
*******************************************************************************
DEFINE MACRO = LO
MACRO INPUTS  = IS    C     RC    R     IO
MACRO OUTPUTS = VC    VO
MACRO CODE
MACRO STOP SORT
                VO LO-- = VC LO-- + (R  LO-- * (IS LO-- + IO LO--)
     & - VC LO--) * RC LO-- / (RC LO-- + R  LO--)
MACRO DERIVATIVE, VC LO-- = (R  LO-- * (IS LO-- + IO LO--) - VC LO--)
     & / (C  LO-- * (RC LO-- + R  LO--))
MACRO RESUME SORT
END OF MACRO
```

```
*****************************************************************************
** Begin model definition.
*****************************************************************************
MODEL DESCRIPTION
LOCATION = 1    FIX    INPUTS = MCX2(S,2=IG)
LOCATION = 41   MCX1   INPUTS = SR01(IG=S,1),SR02(IG=S,3),SR03(IG=S,4)
LOCATION = 21   MCX2   INPUTS = MCX1(S,2=S,1),SR04(IG=S,3),SR05(IG=S,4)
LOCATION = 3    SR01   INPUTS = FIX(VC=V1),LFX(V=VO), MCL(S,2=VX)
LOCATION = 34   MCL      INPUTS = MC01(S,2=S,1)
LOCATION = 40   MCV      INPUTS = LOX(VO=S,1)
LOCATION = 27   MCY1     INPUTS = SR01(IL=S,1),SR02(IL=S,3),SR03(IL=S,4)
LOCATION = 38   MCY2     INPUTS = MCY1(S,2=S,1),SR04(IL=S,3),SR05(IL=S,4)
LOCATION = 25   LEI1     INPUTS = SR01(IL=S,1)
LOCATION = 8    LFX      INPUTS = MCY2(S,2=IS),LOX(VO=VO)
LOCATION = 10   LOX      INPUTS = LFX(IL=IS)
LOCATION = 68   TZX      INPUTS = MCV(S,2=S,1)
LOCATION = 63   MC01     INPUTS = TZX(S,2=S,1),SR01(IL=S,3),LEI1(S,2=S,4)

LOCATION = 113  SR02     INPUTS = FIX(VC=V1), LFX(V=VO),MCI2(S,2=VX)
LOCATION = 119  LEI2     INPUTS = SR02(IL=S,1)
LOCATION = 167  MC02     INPUTS = TZX(S,2=S,1),SR02(IL =S,3),LEI2(S,2=S,4)
LOCATION = 143  MCI2     INPUTS = MC02(S,2=S,1),MCL(S,2=S,3),MC01(S,2=S,4)

LOCATION = 213  SR03     INPUTS = FIX(VC=V1), LFX(V=VO),MCI3(S,2=VX)
LOCATION = 219  LEI3     INPUTS = SR03(IL=S,1)
LOCATION = 267  MC03     INPUTS = TZX(S,2=S,1),SR03(IL=S,3),LEI3(S,2=S,4)
LOCATION = 243  MCI3     INPUTS = MC03(S,2=S,1),MCL(S,2=S,3),MC01(S,2=S,4)

LOCATION = 313  SR04     INPUTS = FIX(VC=V1), LFX(V=VO),MCI4(S,2=VX)
LOCATION = 319  LEI4     INPUTS = SR04(IL=S,1)
LOCATION = 367  MC04     INPUTS = TZX(S,2=S,1),SR04(IL=S,3),LEI4(S,2=S,4)
LOCATION = 343  MCI4     INPUTS = MC04(S,2=S,1),MCL(S,2=S,3),MC01(S,2=S,4)

LOCATION = 413  SR05     INPUTS = FIX(VC=V1), LFX(V = VO),MCI5(S,2=VX)
LOCATION = 419  LEI5     INPUTS = SR05(IL=S,1)
LOCATION = 467  MC05     INPUTS = TZX(S,2=S,1),SR05(IL=S,3),LEI5(S,2=S,4)
LOCATION = 443  MCI5     INPUTS = MC05(S,2=S,1),MCL(S,2=S,3),MC01(S,2=S,4)

END OF MODEL
```

```
*********************************************************************************
** Buck converter model data, example 5. CIC/SCM design, 5 modules.   **
*********************************************************************************
TITLE BUCK CONVERTER EXAMPLE 5  SCM/CIC CONTROL  5 MODULES, SECOND FILTER

INITIAL CONDITIONS
IL FIX = 100
VC FIX = 15
IL SR01 = 100
IL SR02 = 100
IL SR03 = 100
IL SR04 = 100
IL SR05 = 100
VC LOX  = 3.6
X1 TZX  = 0
X2 TZX  = 0

PARAMETER VALUES
IO LOX = 0.0

*********************************************************************************
** Input filter parameter values. Input filter consists of simply LC  **
** circuit. (Dummy values).                                           **
*********************************************************************************
VG FIX = 15      L  FIX = 1.0E-08      C  FIX = 1.0E-08

*********************************************************************************
** MCX- form the sum of the input currents. To connect parallel module**
** set C1, C2, C3 to 1, to disconnect module, set to 0. (C4 always 0) **
** MCY- forms the sum of the output currents. Values should be the    **
** same as for MCX-                                                   **
** N is the number of converters in parallel.                         **
*********************************************************************************
C1 MCX1 = 1.0    C2 MCX1 = 1.0      C3 MCX1 = 1.0      C4 MCX1 = 0.0
C1 MCX2 = 1.0    C2 MCX2 = 1.0      C3 MCX2 = 1.0      C4 MCX2 = 0.0
C1 MCY1 = 1.0    C2 MCY1 = 1.0      C3 MCY1 = 1.0      C4 MCY1 = 0.0
C1 MCY2 = 1.0    C2 MCY2 = 1.0      C3 MCY2 = 1.0      C4 MCY2 = 0.0
N  SR01 = 5
N  SR02 = 5
N  SR03 = 5
N  SR04 = 5
N  SR05 = 5

*********************************************************************************
** Switching regulator values: VCS is steady state capacitor voltage, **
** V1S is steady state input voltage.                                 **
*********************************************************************************
V1SSR01 = 15.0     VCSSR01 = 3.6      L  SR01 = 10.0 E-06
V1SSR02 = 15.0     VCSSR02 = 3.6      L  SR02 = 10.0 E-06
V1SSR03 = 15.0     VCSSR03 = 3.6      L  SR03 = 10.0 E-06
V1SSR04 = 15.0     VCSSR04 = 3.6      L  SR04 = 10.0 E-06
V1SSR05 = 15.0     VCSSR05 = 3.6      L  SR05 = 10.0 E-06
```

```
*****************************************************************************
** Output load current is set by changing load resistance below            **
*****************************************************************************
R  LOX  = 0.0072
R  SR01 = 0.0072
R  SR02 = 0.0072
R  SR03 = 0.0072
R  SR04 = 0.0072
R  SR05 = 0.0072

*****************************************************************************
** Output capacitor value, with ESR                                        **
*****************************************************************************
C  LOX = 36000E-06       RC LOX = 0.002

*****************************************************************************
** Secondary output filter parameter values                                **
*****************************************************************************
C  LFX = 4400E-06      RC LFX = 0.002      L  LFX = 1.0E-07      RL LFX = 1.0E-5

*****************************************************************************
** MC-- is the modulator gain block for each module. Ther are three        **
** inputs, one for the voltage loop, one for an SCM loop, and one for      **
** a CIC loop.                                                             **
**              C1 = Voltage loop gain    = -Fm                            **
**              C2 = CIC loop gain        = -Fm * Rw/n'                    **
**              C3 = SCM loop gain        = -Fm                            **
*****************************************************************************
C1 MC01 = -0.514   C2 MC01 = -0.0257   C3 MC01 = -0.514   C4 MC01 = 0.0
C1 MC02 = -0.514   C2 MC02 = -0.0257   C3 MC02 = -0.514   C4 MC02 = 0.0
C1 MC03 = -0.514   C2 MC03 = -0.0257   C3 MC03 = -0.514   C4 MC03 = 0.0
C1 MC04 = -0.514   C2 MC04 = -0.0257   C3 MC04 = -0.514   C4 MC04 = 0.0
C1 MC05 = -0.514   C2 MC05 = -0.0257   C3 MC05 = -0.514   C4 MC05 = 0.0

*****************************************************************************
** LEI- is the transfer function of the SCM compensation.                  **
*****************************************************************************
GAILEI1 = 0.0625     Z0 LEI1 = 0.0      P0 LEI1 = 3.3 E03
GAILEI2 = 0.0625     Z0 LEI2 = 0.0      P0 LEI2 = 3.3 E03
GAILEI3 = 0.0625     Z0 LEI3 = 0.0      P0 LEI3 = 3.3 E03
GAILEI4 = 0.0625     Z0 LEI4 = 0.0      P0 LEI4 = 3.3 E03
GAILEI5 = 0.0625     Z0 LEI5 = 0.0      P0 LEI5 = 3.3 E03

*****************************************************************************
** TZX is the voltage compensation transfer function.                      **
*****************************************************************************
Z2 TZX = 0.0          Z1 TZX = 1.21 E05     Z0 TZX = 2.32 E08
P1 TZX = 1.39 E04     P0 TZX = 0.0
```

```
*****************************************************************************
** MCV allows the voltage loop to be broken, and the outer loop T2    **
** to be measured. All other loops should be closed, with the         **
** values for MCV gains:                                              **
** C1 MCV = 0.0     C2 MCV = -1.0                                     **
** TF INPUT = S3 MCV     TF OUTPUT = VO LOX                          **
**                                                                    **
** If this loop is to be closed, use                                  **
** C1 MCV = 1.0     C2 MCV = 0.0                                      **
*****************************************************************************
C1 MCV = 1.0      C2 MCV = 0.0      C3 MCV = 0.0      C4 MCV = 0.0

*****************************************************************************
** MCL allows the overall loop to be broken. To measure loop gains:   **
** C1 MCL = 0.0     C2 MCL = -1.0                                     **
** TF INPUT = S3 MCL     TF OUTPUT = S2 MC01                         **
**                                                                    **
** To make closed loop measurements:                                  **
** C1 MCL = 1.0     C2 MCL = 0.0                                      **
*****************************************************************************
C1 MCL = 1.0     C2 MCL = 0.0     C3 MCL = 0.0     C4 MCL = 0.0

*****************************************************************************
** MCI- allows the signal injection into the slave power supplies, in **
** order to measure the loop gain of parallel power modules. To       **
** measure open loop gains:                                           **
** C1 MCI- = 1.0     C2 MCI- = 1.0    C3 MCI- =  -1.0                 **
**                                                                    **
** For closed loop measurements:                                      **
** C1 MCI- = 1.0     C2 MCI- = 0.0     C3 MCI- = 0.0                  **
*****************************************************************************
C1 MCI2 = 1.0     C2 MCI2 = 0.0     C3 MCI2 = 0.0     C4 MCI2 = 0.0
C1 MCI3 = 1.0     C2 MCI3 = 0.0     C3 MCI3 = 0.0     C4 MCI3 = 0.0
C1 MCI4 = 1.0     C2 MCI4 = 0.0     C3 MCI4 = 0.0     C4 MCI4 = 0.0
C1 MCI5 = 1.0     C2 MCI5 = 0.0     C3 MCI5 = 0.0     C4 MCI5 = 0.0


*****************************************************************************
** End of model parameter inputs.                                     **
*****************************************************************************
ONLINE PLOTS
PRINTER PLOTS
TF MANUAL SCALES
FREQ MIN = 65.0
FREQ MAX = 3.0E05
```

```
*********************************************************************************
** Open loop gain measurements. Voltage loop, SCM loop or CIC loop are**
** selected by changing the gains of MC0-.                                     **
*********************************************************************************
PARAMETER VALUES
C1 MC01 = -0.514      C2 MC01 = 0.0      C3 MC01 = 0.0
C1 MC02 = -0.514      C2 MC02 = 0.0      C3 MC02 = 0.0
C1 MC03 = -0.514      C2 MC03 = 0.0      C3 MC03 = 0.0
C1 MC04 = -0.514      C2 MC04 = 0.0      C3 MC04 = 0.0
C1 MC05 = -0.514      C2 MC05 = 0.0      C3 MC05 = 0.0
C1 MCL = 0.0       C2 MCL = -1.0
C1 MCI2 = 1.0      C2 MCI2 = 1.0      C3 MCI2 = -1.0
C1 MCI3 = 1.0      C2 MCI3 = 1.0      C3 MCI3 = -1.0
C1 MCI4 = 1.0      C2 MCI4 = 1.0      C3 MCI4 = -1.0
C1 MCI5 = 1.0      C2 MCI5 = 1.0      C3 MCI5 = -1.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = S3 MCL       TF OUTPUT = S2 MC01
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  LOOP GAIN Tv
TRANSFER FUNCTION

PARAMETER VALUES
C1 MC01 = 0.0      C2 MC01 = -0.0257      C3 MC01 = 0.0
C1 MC02 = 0.0      C2 MC02 = -0.0257      C3 MC02 = 0.0
C1 MC03 = 0.0      C2 MC03 = -0.0257      C3 MC03 = 0.0
C1 MC04 = 0.0      C2 MC04 = -0.0257      C3 MC04 = 0.0
C1 MC05 = 0.0      C2 MC05 = -0.0257      C3 MC05 = 0.0
C1 MCL = 0.0       C2 MCL = -1.0
C1 MCI2 = 1.0      C2 MCI2 = 1.0      C3 MCI2 = -1.0
C1 MCI3 = 1.0      C2 MCI3 = 1.0      C3 MCI3 = -1.0
C1 MCI4 = 1.0      C2 MCI4 = 1.0      C3 MCI4 = -1.0
C1 MCI5 = 1.0      C2 MCI5 = 1.0      C3 MCI5 = -1.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = S3 MCL       TF OUTPUT = S2 MC01
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  CIC LOOP GAIN
TRANSFER FUNCTION

PARAMETER VALUES
C1 MC01 = 0.0      C2 MC01 = 0.0      C3 MC01 = -0.514
C1 MC02 = 0.0      C2 MC02 = 0.0      C3 MC02 = -0.514
C1 MC03 = 0.0      C2 MC03 = 0.0      C3 MC03 = -0.514
C1 MC04 = 0.0      C2 MC04 = 0.0      C3 MC04 = -0.514
C1 MC05 = 0.0      C2 MC05 = 0.0      C3 MC05 = -0.514
C1 MCL = 0.0       C2 MCL = -1.0
C1 MCI2 = 1.0      C2 MCI2 = 1.0      C3 MCI2 = -1.0
C1 MCI3 = 1.0      C2 MCI3 = 1.0      C3 MCI3 = -1.0
C1 MCI4 = 1.0      C2 MCI4 = 1.0      C3 MCI4 = -1.0
C1 MCI5 = 1.0      C2 MCI5 = 1.0      C3 MCI5 = -1.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = S3 MCL       TF OUTPUT = S2 MC01
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  SCM LOOP GAIN
TRANSFER FUNCTION
```

```
PARAMETER VALUES
C1 MC01 = -0.0      C2 MC01 = -0.0257      C3 MC01 = -0.514
C1 MC02 = -0.0      C2 MC02 = -0.0257      C3 MC02 = -0.514
C1 MC03 = -0.0      C2 MC03 = -0.0257      C3 MC03 = -0.514
C1 MC04 = -0.0      C2 MC04 = -0.0257      C3 MC04 = -0.514
C1 MC05 = -0.0      C2 MC05 = -0.0257      C3 MC05 = -0.514
C1 MCI2 = 1.0      C2 MCI2 = 1.0      C3 MCI2 = -1.0
C1 MCI3 = 1.0      C2 MCI3 = 1.0      C3 MCI3 = -1.0
C1 MCI4 = 1.0      C2 MCI4 = 1.0      C3 MCI4 = -1.0
C1 MCI5 = 1.0      C2 MCI5 = 1.0      C3 MCI5 = -1.0
C1 MCL = 0.0       C2 MCL = -1.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = S3 MCL       TF OUTPUT = S2 MC01
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  CURRENT LOOP
TRANSFER FUNCTION

PARAMETER VALUES
C1 MC01 = -0.514      C2 MC01 = -0.0257      C3 MC01 = -0.514
C1 MC02 = -0.514      C2 MC02 = -0.0257      C3 MC02 = -0.514
C1 MC03 = -0.514      C2 MC03 = -0.0257      C3 MC03 = -0.514
C1 MC04 = -0.514      C2 MC04 = -0.0257      C3 MC04 = -0.514
C1 MC05 = -0.514      C2 MC05 = -0.0257      C3 MC05 = -0.514
C1 MCI2 = 1.0      C2 MCI2 = 1.0      C3 MCI2 = -1.0
C1 MCI3 = 1.0      C2 MCI3 = 1.0      C3 MCI3 = -1.0
C1 MCI4 = 1.0      C2 MCI4 = 1.0      C3 MCI4 = -1.0
C1 MCI5 = 1.0      C2 MCI5 = 1.0      C3 MCI5 = -1.0
C1 MCL = 0.0       C2 MCL = -1.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = S3 MCL       TF OUTPUT = S2 MC01
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5MODULES  LOOP GAIN T1
TRANSFER FUNCTION

PARAMETER VALUES
C1 MC01 = -0.514      C2 MC01 = -0.0257      C3 MC01 = -0.514
C1 MC02 = -0.514      C2 MC02 = -0.0257      C3 MC02 = -0.514
C1 MC03 = -0.514      C2 MC03 = -0.0257      C3 MC03 = -0.514
C1 MC04 = -0.514      C2 MC04 = -0.0257      C3 MC04 = -0.514
C1 MC05 = -0.514      C2 MC05 = -0.0257      C3 MC05 = -0.514
C1 MCL =  1.0      C2 MCL = 0.0
C1 MCI2 = 1.0      C2 MCI2 = 0.0      C3 MCI2 = 0.0
C1 MCI3 = 1.0      C2 MCI3 = 0.0      C3 MCI3 = 0.0
C1 MCI4 = 1.0      C2 MCI4 = 0.0      C3 MCI4 = 0.0
C1 MCI5 = 1.0      C2 MCI5 = 0.0      C3 MCI5 = 0.0
C1 MCV = 0.0       C2 MCV  = -1.0
TF INPUT = S3 MCV       TF OUTPUT = VO LOX
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  LOOP GAIN T2
TRANSFER FUNCTION
```

```
**********************************************************************************
** Closed loop measurements.                                                    **
**********************************************************************************
PARAMETER VALUES
C1 MC01 = -0.514      C2 MC01 = -0.0257      C3 MC01 = -0.514
C1 MC02 = -0.514      C2 MC02 = -0.0257      C3 MC02 = -0.514
C1 MC03 = -0.514      C2 MC03 = -0.0257      C3 MC03 = -0.514
C1 MC04 = -0.514      C2 MC04 = -0.0257      C3 MC04 = -0.514
C1 MC05 = -0.514      C2 MC05 = -0.0257      C3 MC05 = -0.514
C1 MCL =  1.0      C2 MCL = 0.0
C1 MCI2 = 1.0      C2 MCI2 = 0.0      C3 MCI2 = 0.0
C1 MCI3 = 1.0      C2 MCI3 = 0.0      C3 MCI3 = 0.0
C1 MCI4 = 1.0      C2 MCI4 = 0.0      C3 MCI4 = 0.0
C1 MCI5 = 1.0      C2 MCI5 = 0.0      C3 MCI5 = 0.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = VG FIX      TF OUTPUT = VO LOX
TITLE    BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  AUDIO
TRANSFER FUNCTION


PARAMETER VALUES
C1 MC01 = -0.514      C2 MC01 = -0.0257      C3 MC01 = -0.514
C1 MC02 = -0.514      C2 MC02 = -0.0257      C3 MC02 = -0.514
C1 MC03 = -0.514      C2 MC03 = -0.0257      C3 MC03 = -0.514
C1 MC04 = -0.514      C2 MC04 = -0.0257      C3 MC04 = -0.514
C1 MC05 = -0.514      C2 MC05 = -0.0257      C3 MC05 = -0.514
C1 MCL =  1.0      C2 MCL = 0.0
C1 MCI2 = 1.0      C2 MCI2 = 0.0      C3 MCI2 = 0.0
C1 MCI3 = 1.0      C2 MCI3 = 0.0      C3 MCI3 = 0.0
C1 MCI4 = 1.0      C2 MCI4 = 0.0      C3 MCI4 = 0.0
C1 MCI5 = 1.0      C2 MCI5 = 0.0      C3 MCI5 = 0.0
C1 MCV = 1.0       C2 MCV  = 0.0
TF INPUT = IO LOX      TF OUTPUT = VO LOX
TITLE BUCK CONVERTER  EXAMPLE 6  SCM/CIC CONTROL 5 MODULES  ZOUT
TRANSFER FUNCTION
```

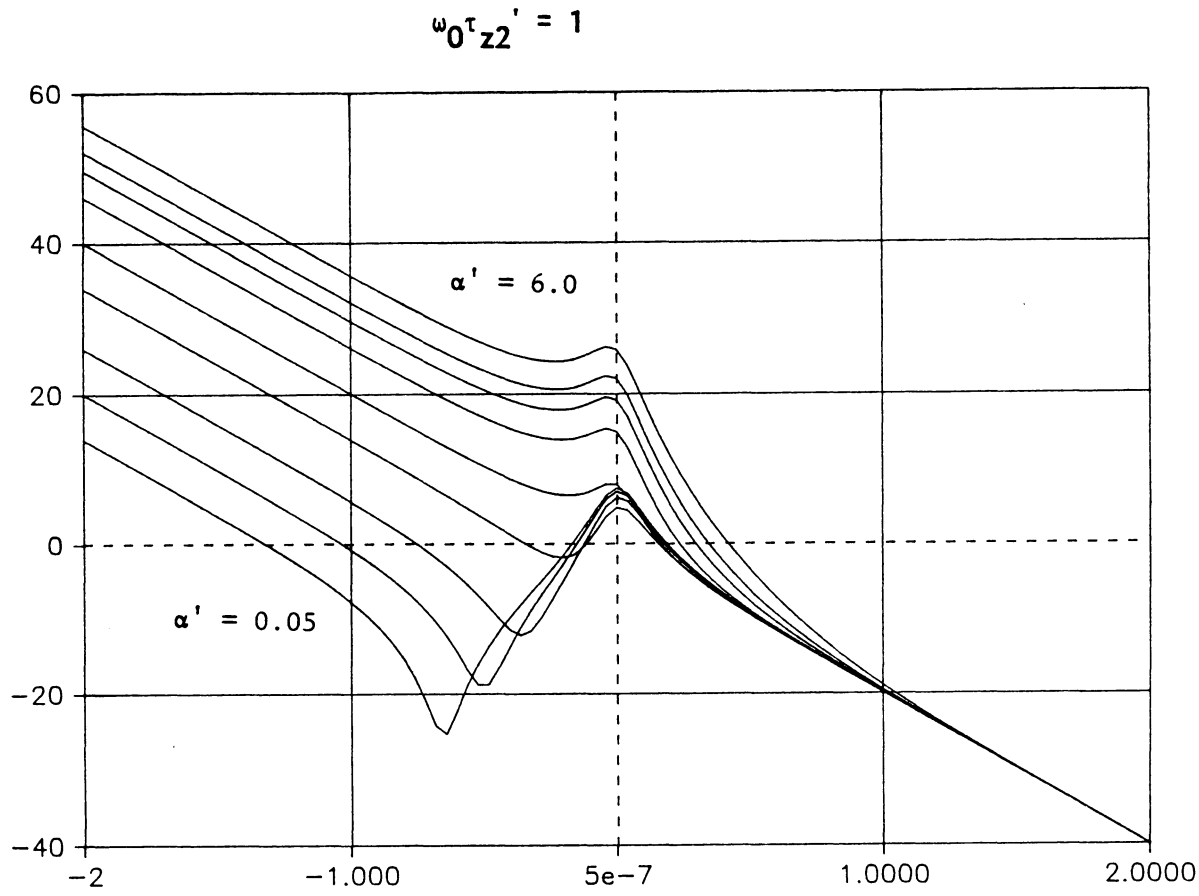
APPENDIX D

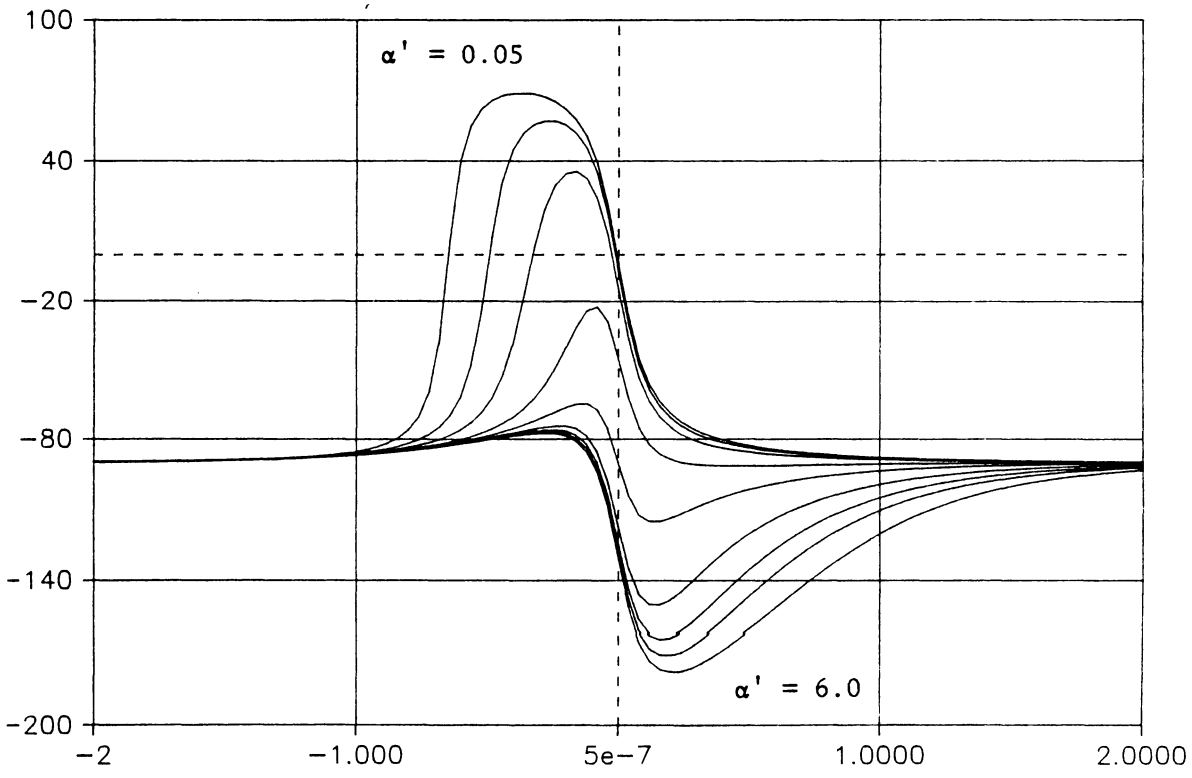
Normalized Loop Gain and Phase Curves for Control Design

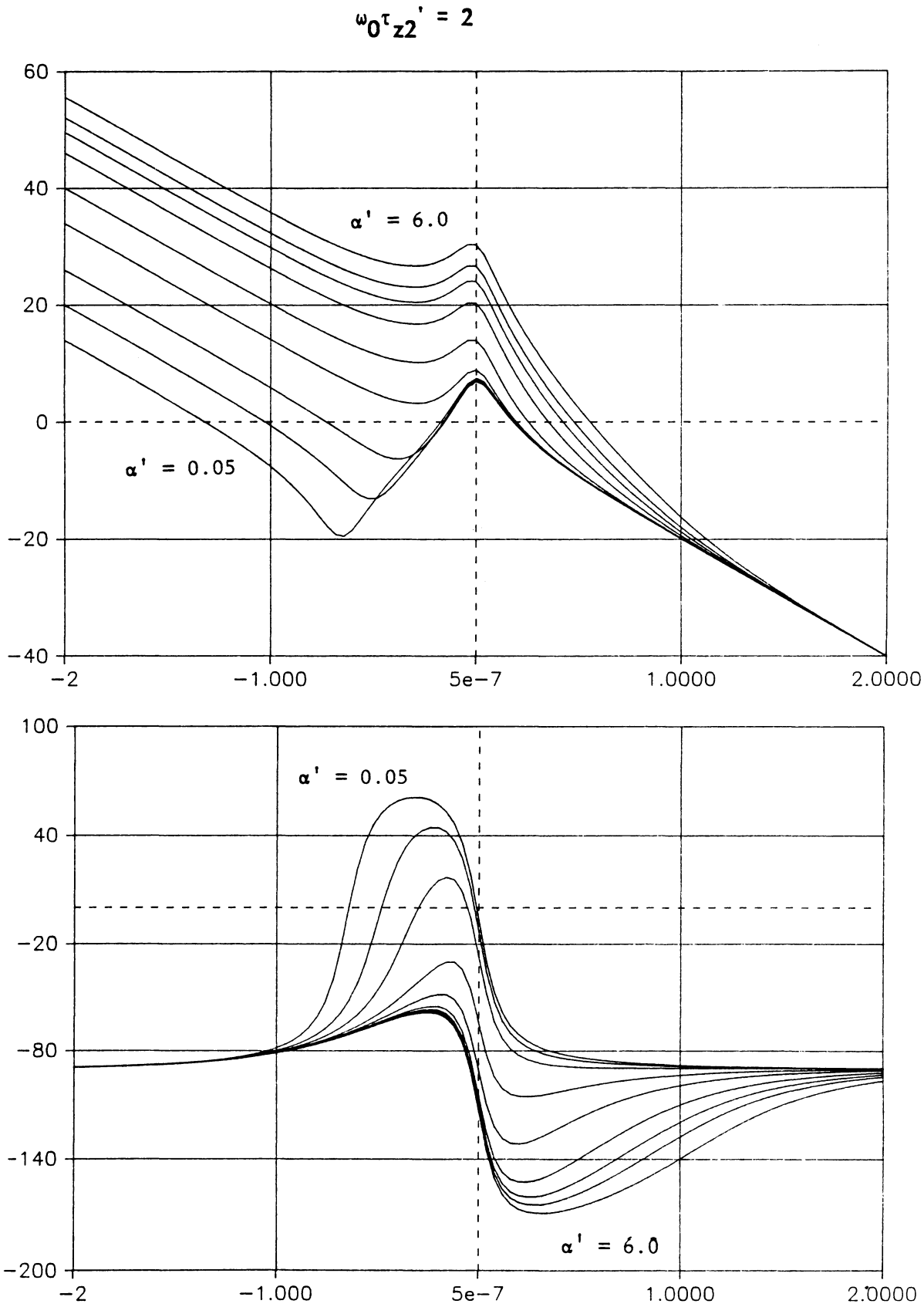
The curves in this appendix are intended for use with the design procedures of Chapter 6. After selection of the zero s_{02} in the design procedures, the quantity $\omega_0\tau_{z2}'$ may be calculated as described in Chapter 6. Curves are presented here for values of $\omega_0\tau_{z2}'$ from 1 to 10, and the set of curves corresponding to the closest value should be used. The gain of the curves is normalized as described in the design procedures, and the frequency is normalized to the resonant frequency, ω_0. From this set of curves, the desired value of α' may be selected from within the allowable range calculated during the design procedures.

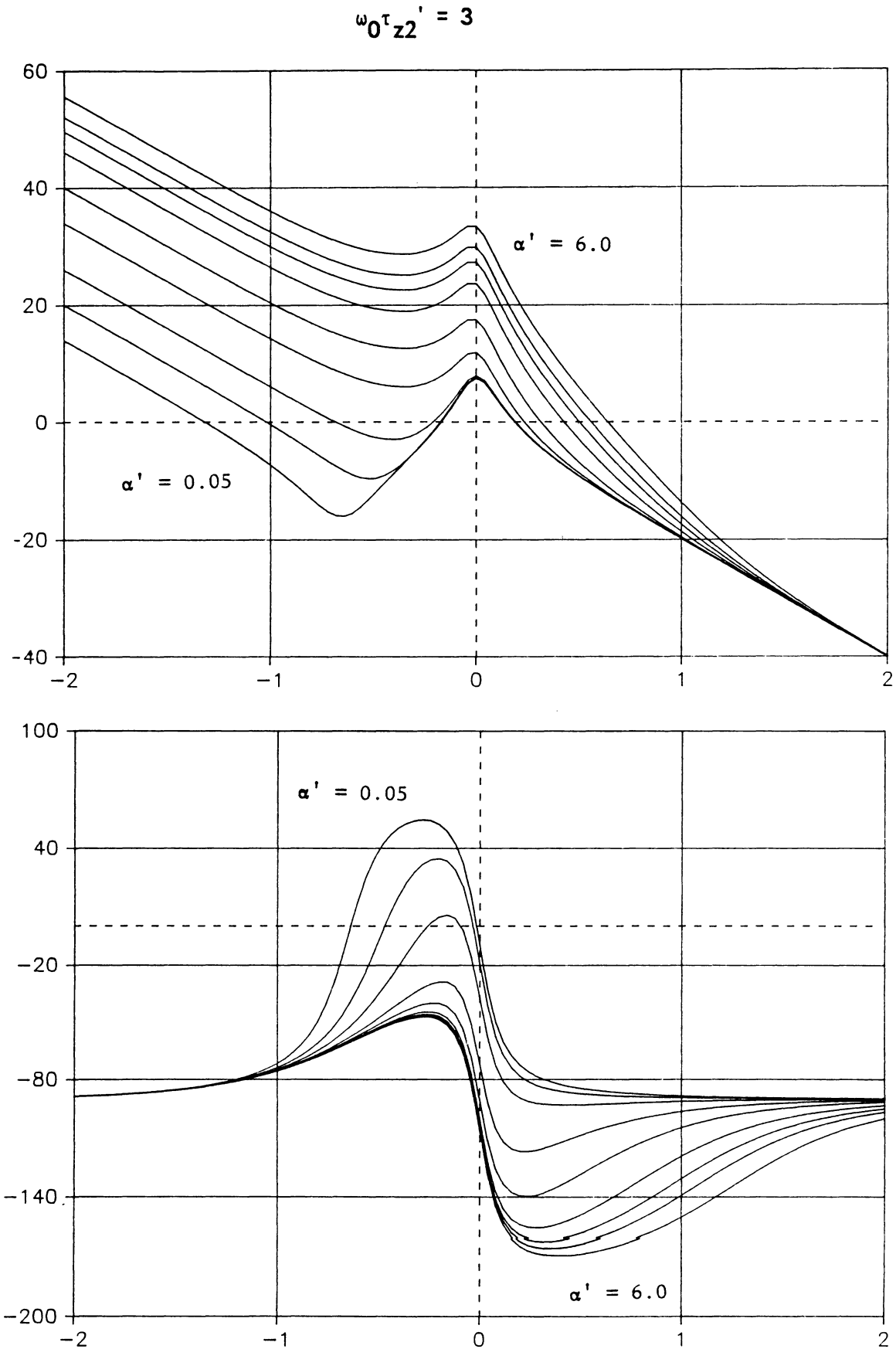
The damping coefficient, ζ, used to plot these curves was chosen to be 0.2. Few practical power supplies will have a lower damping factor than this, and the effect of an increased damping factor is to improve the phase margin for any choice of α'.

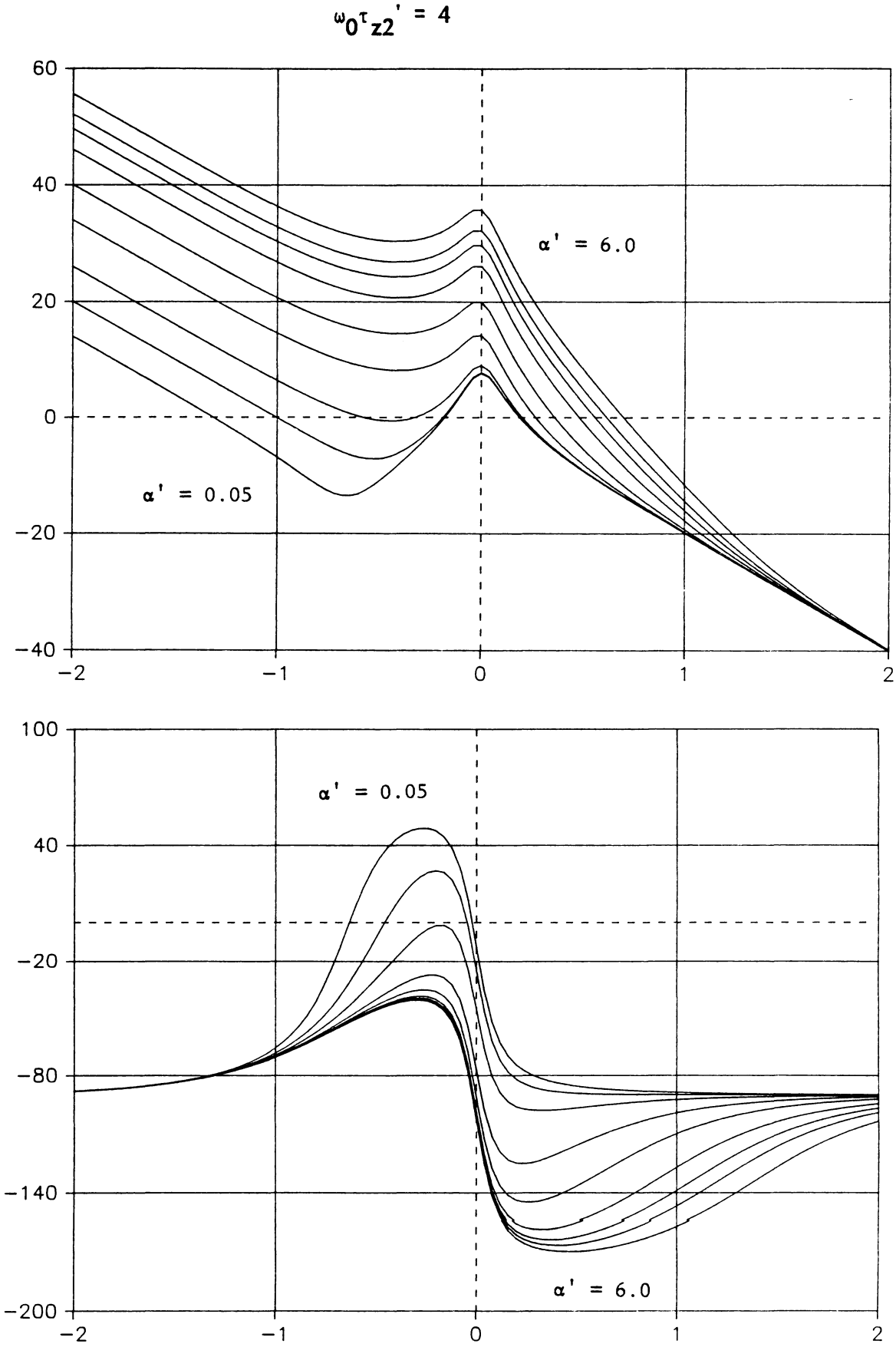
The values of α', beginning with the lowermost gain curve (and, correspondingly, the uppermost phase curve), are 0.05, 0.1, 0.2, 0.5, 1.0, 2.0, 3.0, 4.0, and 6.0.

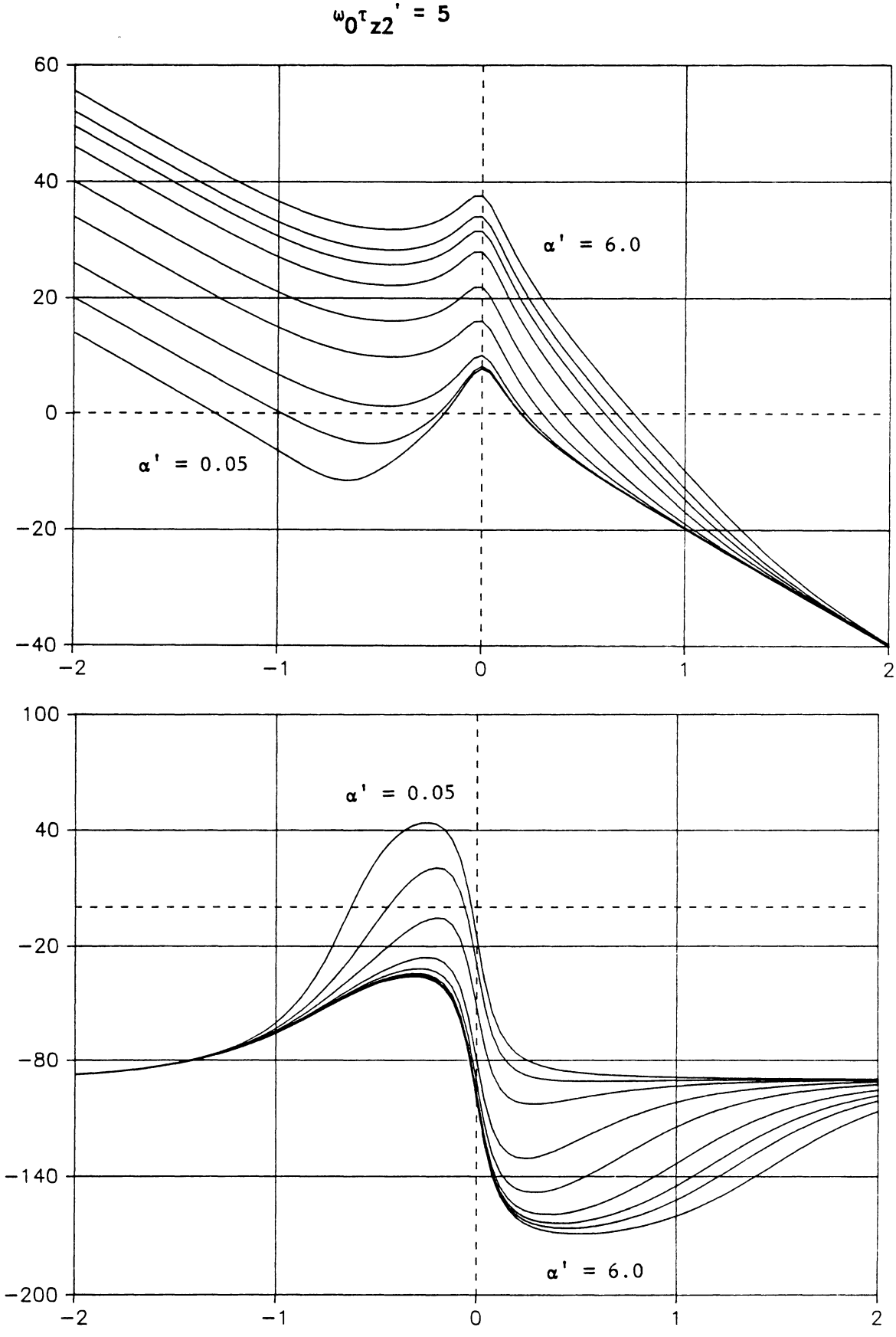

$\omega_0\tau_{z2}' = 1$
60
40
20
0
−20
−40
α' = 6.0
α' = 0.05
−2
−1.000
5e−7
1.0000
2.0000

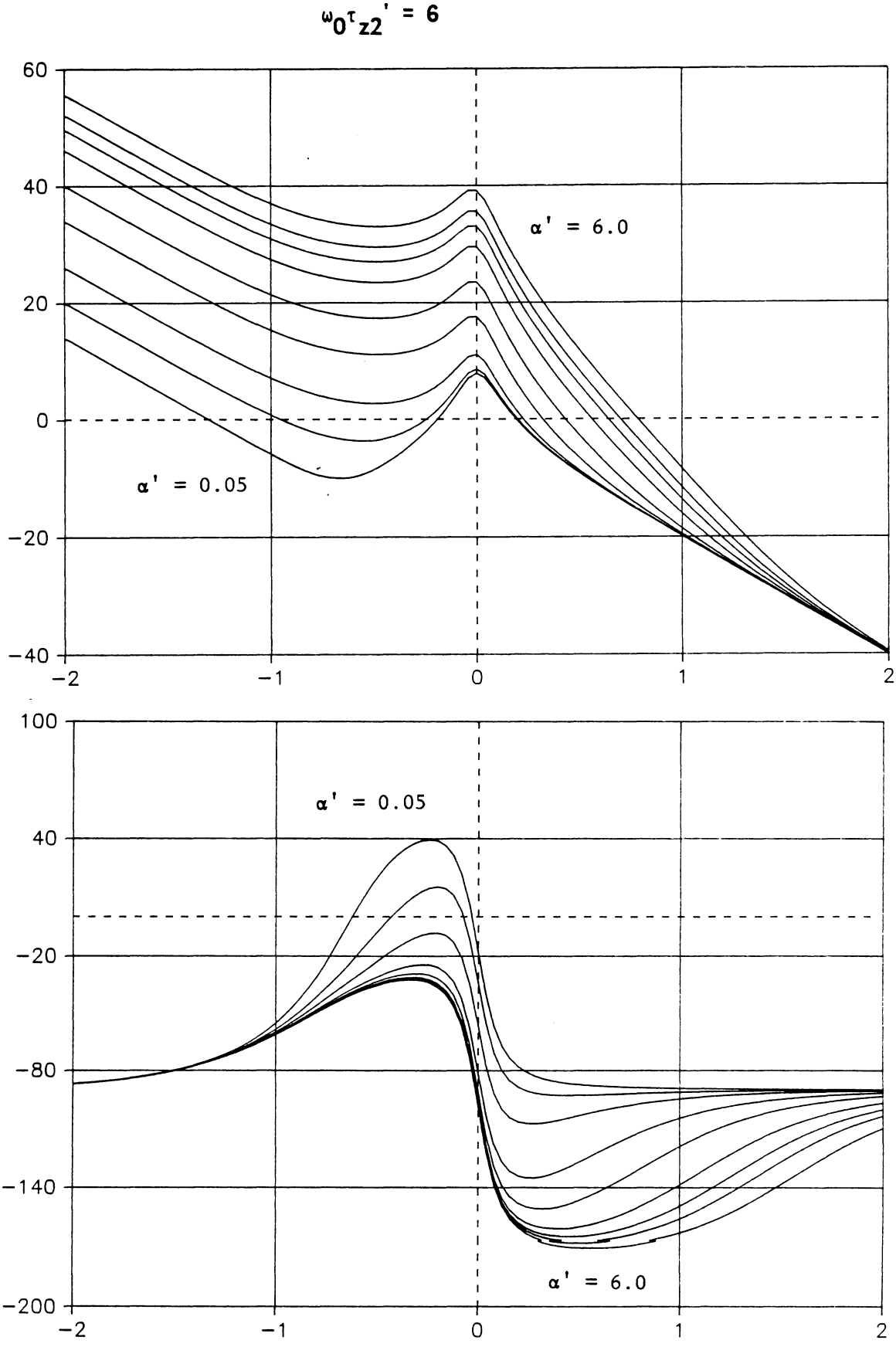

100
40
−20
−80
−140
−200
α' = 0.05
α' = 6.0
−2
−1.000
5e−7
1.0000
2.0000


$\omega_0\tau_{z2}' = 2$
60
40
20
0
−20
−40
α' = 6.0
α' = 0.05
−2
−1.000
5e−7
1.0000
2.0000
100
40
−20
−80
−140
−200
α' = 0.05
α' = 6.0
−2
−1.000
5e−7
1.0000
2.0000

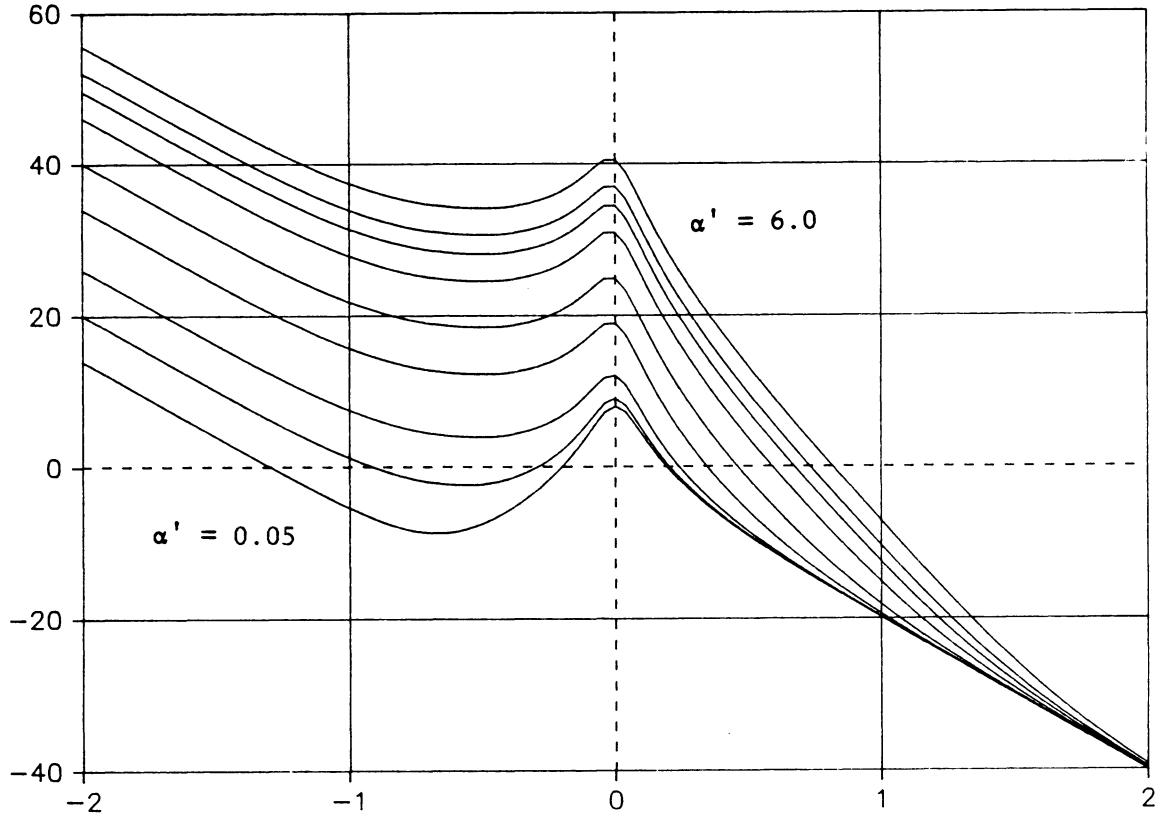

$\omega_0\tau_{z2}' = 3$
60
40
20
0
-20
-40
-2
-1
0
1
2
α' = 6.0
α' = 0.05
100
40
-20
-80
-140
-200
α' = 0.05
α' = 6.0

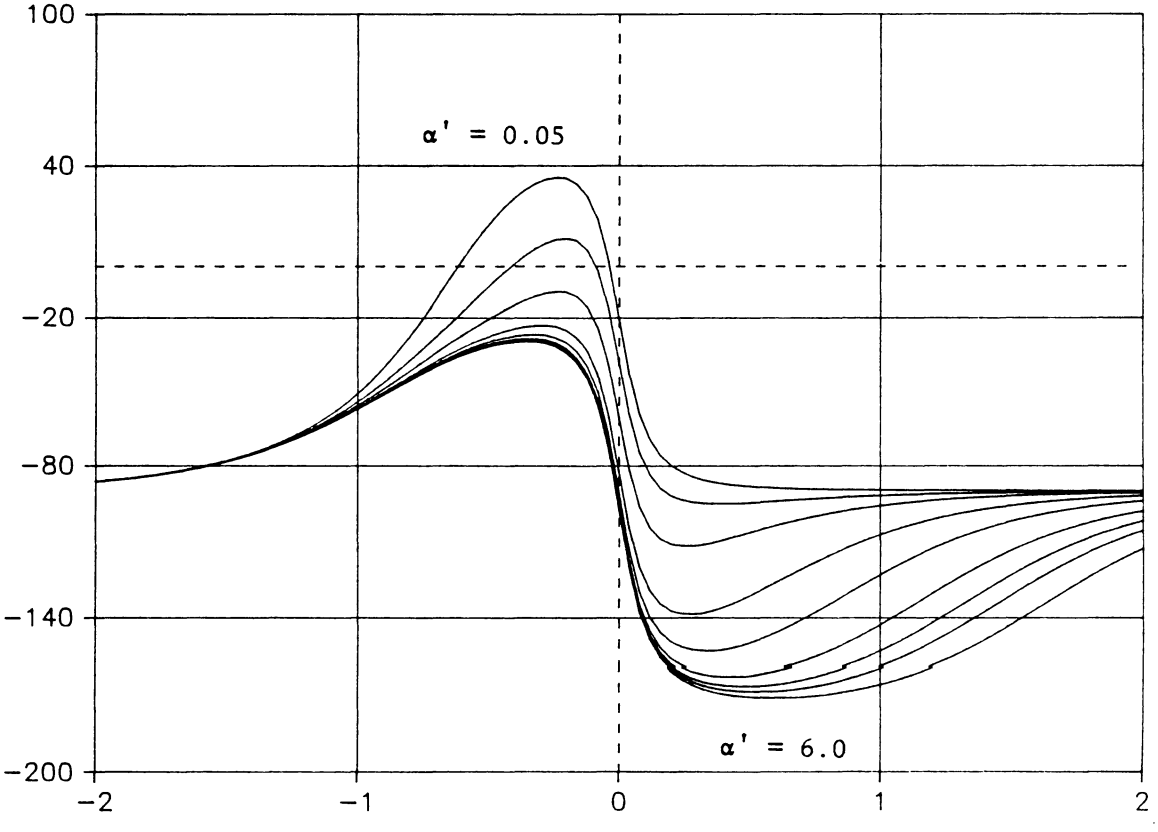

$\omega_0\tau_{z2}' = 4$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
−2
−1
0
1
2
α' = 0.05
α' = 6.0

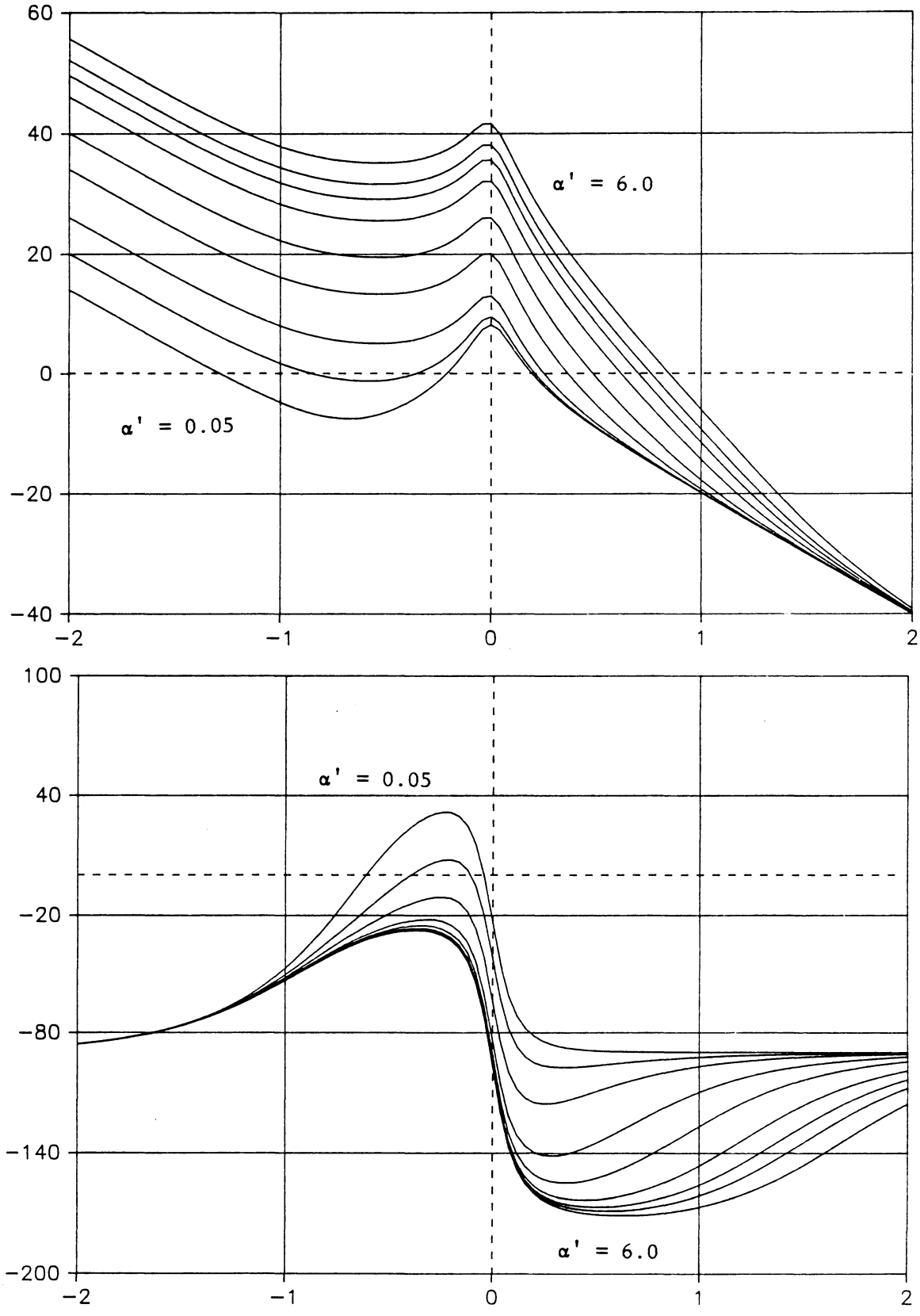

$\omega_0\tau_{z2}' = 5$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
α' = 0.05
α' = 6.0

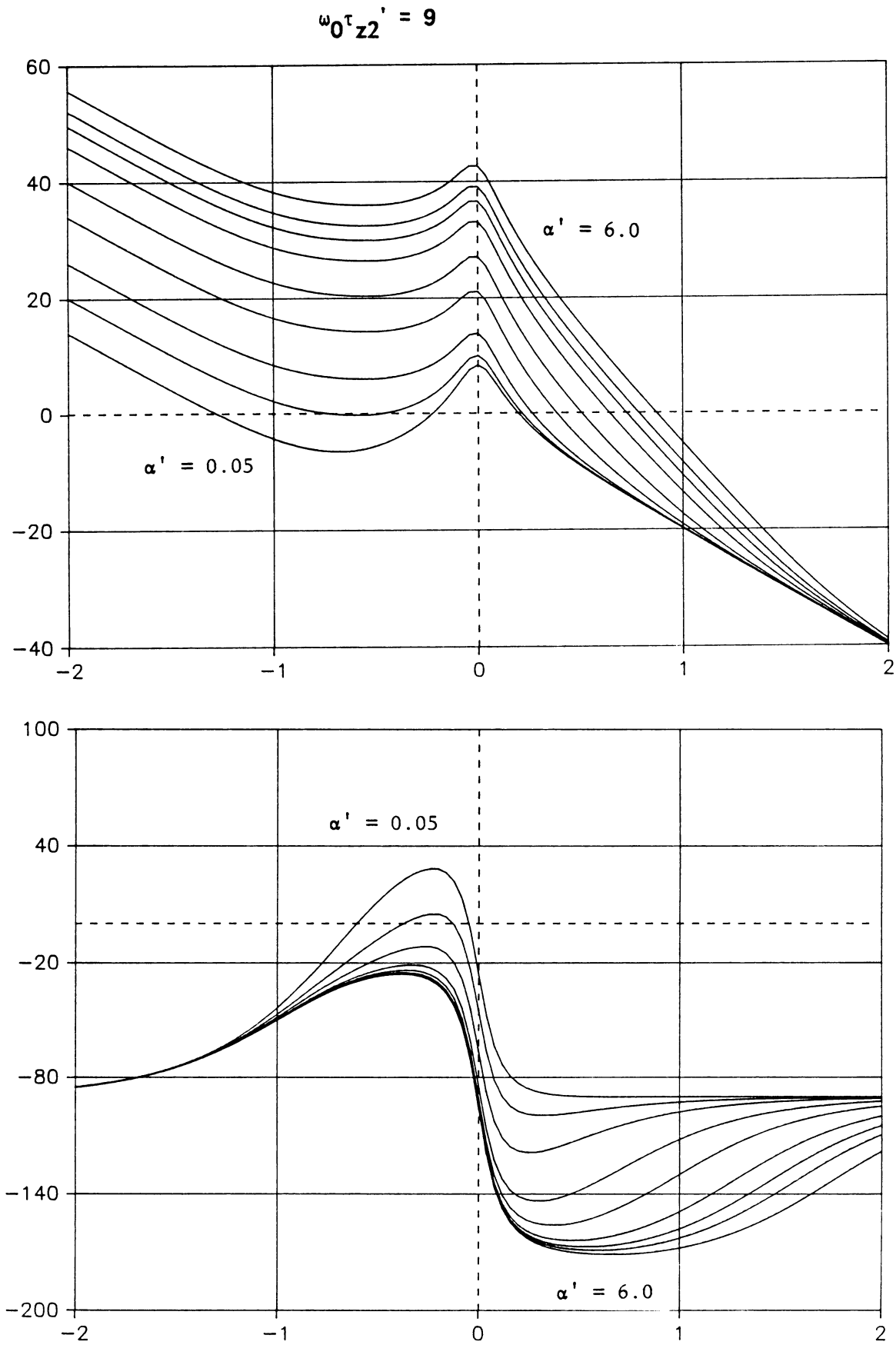

$\omega_0\tau_{z2}' = 6$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
α' = 0.05
α' = 6.0

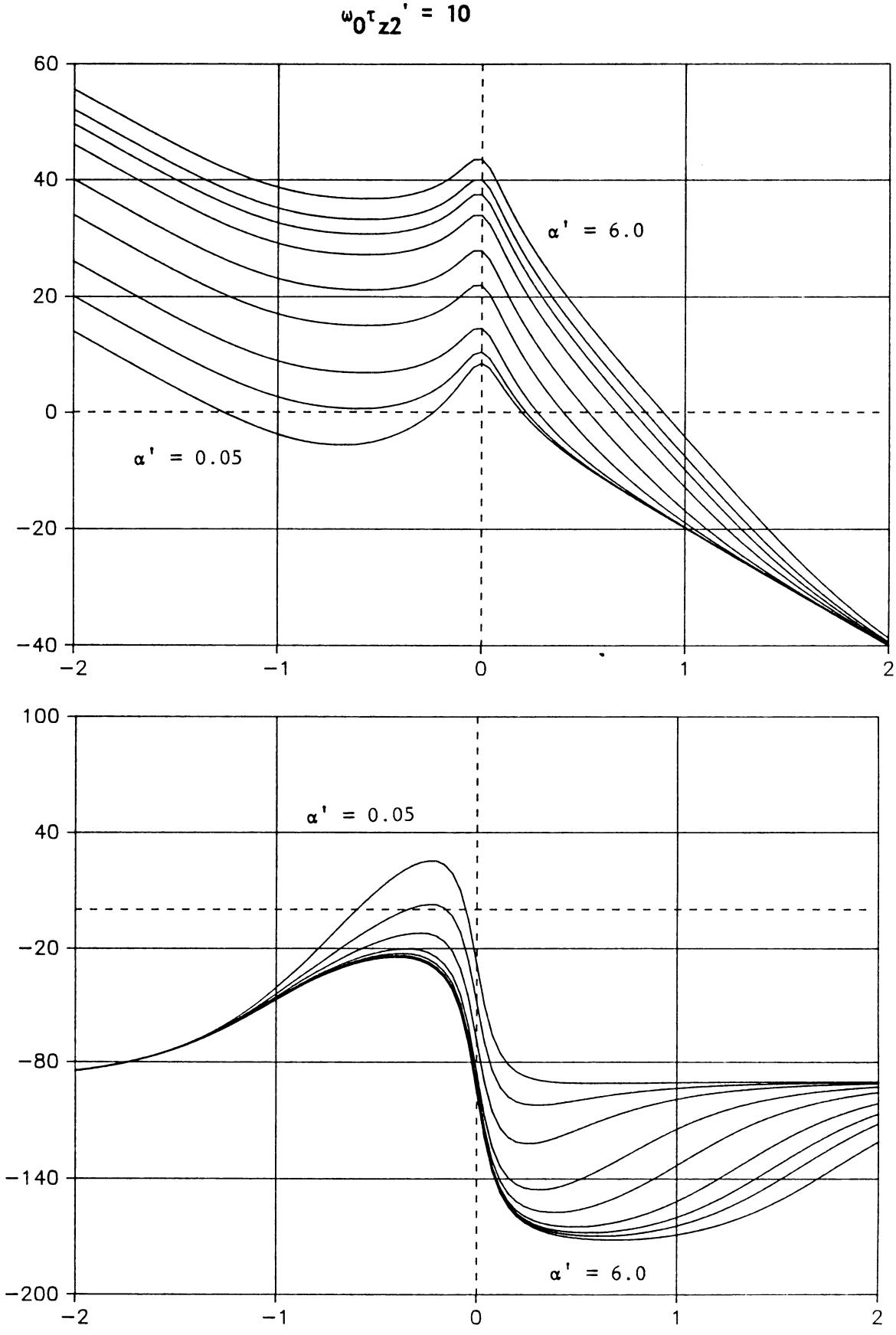
$\omega_0 \tau_{z2}' = 7$






$\omega_0\tau_{z2}' = 8$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
−2
−1
0
1
2
α' = 0.05
α' = 6.0


$\omega_0\tau_{z2}' = 9$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
α' = 0.05
α' = 6.0


$\omega_0\tau_{z2}' = 10$
60
40
20
0
−20
−40
−2
−1
0
1
2
α' = 6.0
α' = 0.05
100
40
−20
−80
−140
−200
−2
−1
0
1
2
α' = 0.05
α' = 6.0

REFERENCES

[1] F.C. Lee, M.F. Mahmoud, Y. Yu, "Design Handbook for a Standardized Control Module for DC-to-DC Converters", Volumes I and II, NASA Contract NAS-3-20102, April, 1980.

[2] B.H. Cho, F.C. Lee, "Measurement of Loop Gain with the Digital Modulator", IEEE Power Electronics Specialists Conference, June 18-21, 1984.

[3] Z.D. Fang, T.H. Lee, F.C. Lee, "Some Design Considerations of Switching Regulators Employing Current-Injected Control", PCI/Motorcon, April, 1983. Conference, June 18-21, 1984.

[4] R.D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming", IEEE Power Electronics Specialists Conference, Toulouse, France, June 24-28, 1985.

[5] Boeing Computer Services Company, " MAINSTREAM-EKS EASY5 Dynamic Analysis System User's Guide", April, 1983.

[6] B.H. Cho, "Modelling and Analysis of Spacecraft Power Systems", PhD Dissertation, Virginia Polytechnic Institute and State University, October, 1985.

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