COLLISION STUDY FOR THE ONE-WAY IVDS CHANNEL

by

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Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

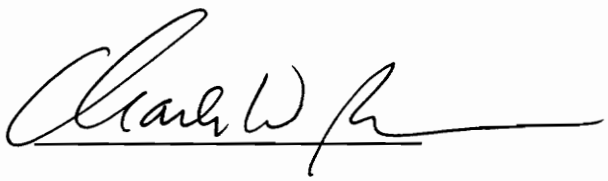
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

APPROVED:



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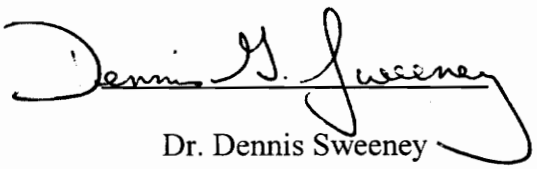

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August, 1996

Blacksburg, Virginia

Key Words: *capture, jamming margin, process gain, autocorrelation, collision*

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(ABSTRACT)

A collision study is performed to compare the interference rejection characteristics of two spread spectrum receivers, one employing a sliding correlator and the other using a more sophisticated matched filter design. The testing involves using two similar transmitters, one acting a the jammer, to test the collision dynamics of each receiver. Packet data from both transmitters contain identical spreading codes. Data from the testing is analyzed and the receivers' *jamming margin*, *capture*, and *process gain* qualities are compared as to which system best optimizes a one-way channel.

Motivation for the collision study stems from researching a one-way communication link for the Interactive Video Data Service (IVDS) project currently being developed by the Center for Wireless Telecommunications (CWT) at Virginia Tech. A novel retransmission technique has previously been developed which discusses the probability of packet collisions on the channel and uses a computer program to simulate the channel model. This thesis will provide more information as to what happens in packet collisions as well as determine which receiver type offers the greatest interference rejection.

Acknowledgments

I would like to express my gratitude and appreciation for my advisor, Dr. Bostian. As both an undergraduate and a graduate, I was fortunate to have Dr. Bostian as professor. Through his commitment and devotion as a teacher he has proven himself to be more than just an advisor, but a role model as well. Without his guidance, this work would never been accomplished.

I would like to thank Dr. Dennis Sweeney and Dr. Timothy Pratt for serving on my committee, and for their valuable guidance through my career here at Virginia Tech.

I would also like to thank my friends and co-workers, Boris Davidson, Todd Goedde, Raza Shah, for their time and efforts in helping me. Special thanks to Ph.D. candidate, Boris Davidson, who often served as a second advisor.

I would like to thank the Virginia Tech Corps of Cadets and Army ROTC for allowing time to do this research as well as assisting my funding.

Finally, I would like to thank my family-my parents, James and Sally, my sisters, Tracy and Catie, and my girlfriend, Amy. They have always been a source of love, encouragement, and support. I dedicate this work to them.

This work was supported by Interactive Return Service, Inc. and the Virginia Center of Innovative Technology.

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Figures and Tables

1.0 INTRODUCTION

The field of personal wireless communications is expanding rapidly as a result of advances in digital communications, portable computers, cellular networks, wireless LAN's, and personal communication systems[7]. New protocols and multiple access techniques have been developed to accommodate the growing number of users utilizing these systems. The goal of each strategy is to maximize channel reliability and to support the greatest possible number of customers.

A new protocol for a one-way direct sequence spread spectrum channel is implemented for the Interactive Video Data Service (IVDS). IVDS allows a consumer to order a product or service advertised on television using a small "remote control" sized transmitter. The transmitter receives or "hears" data encoded in the television's audio signal. Subsequently, the transmitter sends the product information along with an identification number, the combination constitutes a packet, over a wireless channel to a local repeater station. Unlike most multiple access techniques, such as ALOHA[2], the transmitter receives no acknowledgment from a local repeater. Instead, the transmitter relies on sending multiple retransmissions to guarantee message arrival. This protocol is sometimes referred to as "send and pray."

The effectiveness of the one-way channel depends on the retransmission strategy. In this protocol, the transmitter sends multiple retransmissions within a 30 second time period. This time period is divided into several subintervals in which the retransmissions are randomly slotted. This retransmission strategy is discussed in greater detail in [5]. Once an error free packet is received, all retransmissions of the packet are ignored and discarded.

This type of communication system has many advantages. Unlike ALOHA, slotted-ALOHA, and Packet Reservation Multiple Access(PRMA)[2,6], the receiver is unable to relay any kind of acknowledgment or tell the transmitter when a time slot is available. Thus, the channel's transmitter is cheaper and smaller than those implementing

bi-directional multiple access channels. The absence of a return path from the receiver makes a one-way communication system more efficient.

Because of the nature of such a channel, it is important to study the effects of colliding packets at the receiver. A previous paper [5] has described the theoretical aspects of the channel and derived a closed form expression describing the probability of collision. Therefore, this thesis will focus specifically on what happens at the receiver when a collision occurs. In a best case scenario, the receiver is capable of receiving one uncorrupted data packet from a collision. In the worst case scenario, the receiver loses all data from the packets in a collision. The goal of this thesis is to test two different types of direct sequence spread spectrum receivers, coherent and noncoherent, to determine conditions under which one uncorrupted packet will be received in a collision. Collision will be described as the condition in which the receiver acquires one signal and is "hit" by another signal while still processing the first. In the final analysis, the two separate systems will be evaluated, compared, and contrasted to determine which is best suited for this particular communication channel.

2.0 IVDS OVERVIEW AND BACKGROUND

Mr. Fernando Morales, founder and CEO of Interactive Return Service, Inc.(IRS), began funding the Virginia Tech Center for Wireless Telecommunication(CWT) to work on a proposed IVDS system in January 1994. The goal of the project was to develop a prototype commercial system incorporating a small hand held transmitter for interactive use with current televisions[5]. These transmitters would require no connections or special add-on box to the TV. Instead, product information would be embedded in an interactive commercial's audio channel. Upon a user's request, the transmitter would demodulate this audio code and send the product data over a wireless path to a local repeater station. From the local repeater, information would then pass through a Cellular Digital Packet Data (CDPD) modem to the main processing station where the order is processed. Initially, the project required CWT to research and develop the hand held user unit (the project name for the transmitter), the local area repeater unit, the audio code modulator and demodulator, and a remote video mouse. The requirement for a video mouse was later removed and a bar code reader option was introduced.

CWT assigned work on the project to four research groups: the Audio Code Group, the Controls Group, the Antennas Group, and the Radio Frequency (RF) Group. The Audio Code Group focused on embedding a special product code into a television commercial and worked on the Digital Signal Processing (DSP) code and filtering to detect the code. The group was successful in detecting the code at three separate audio frequencies.

The Antennas Group researched antennas that could possibly fit inside a small remote control size transmitter. A prototype antenna was developed using an inverted F type design, which is basically a small plate fed over a ground plane.

The Controls Group was responsible for developing the software for both the user unit and the local area repeater. The user unit software enables the audio demodulator or bar code scanner, processes the information into a prescribed format, and controls the RF

transmission and random retransmissions. The repeater software receives the data, processes the information by checking for errors, compares retransmissions and discards duplicate messages, and sends the information to the central processor by way of a CDPD modem. In addition, the Controls Group also integrated the bar code reader into the transmitter.

The goal of the RF Group was to develop a wireless channel model to replicate accurately the IVDS system. By determining the best random access technique and modulation, the group then simulated the channel reliability and performed initial propagation tests. From this point, the group developed a "stand alone" breadboard for the system prototype. This thesis will cover topics relevant to channel reliability by testing these "stand alone" prototypes.

The finished system envisions a user picking up a small remote control device, listening to a commercial for a desired product, and pushing the button to order the product. Verification of the order would be displayed on a PC at the "home station" connected to the local repeaters through CDPD modems.

2.1 The RF Channel

The novel approach of using a one way direct sequence spread spectrum communication system to implement the IVDS channel model was researched by the RF group. Again, the goal of such a system is to allow for inexpensive transmitter circuitry and increased user throughput. IVDS will use a random access technique in which the user unit retransmits the original message a specified number of times randomly within a set time interval. The channel model is well outlined in "A Novel Retransmission Technique for One-Way Packet Communications[5]." This paper discusses the probability of successful packet arrival rates within a probabilistic traffic model. The paper's simulation maximizes the number of successful message transmissions versus the number of retransmissions for set message arrival rates. The simulation shows that at higher arrival rates, fewer retransmissions are needed to maximize the message success rate since the

channel becomes saturated with retransmissions colliding with original messages. The simulation model considers that in a collision the entire data packet is lost. This thesis will consider additional improvements to the present channel simulation program by explaining what actually happens in a packet collision and providing data for a better channel model.

2.2 IVDS Proof of Concept

One of the initial tasks for the RF group was to give a small proof of concept demonstration on the propagation properties of the IVDS channel. The goal was simply to measure received power levels at different locations specified distances from the transmitter. The transmitter was tested in two different indoor environments: a mobile trailer, made of aluminum, and the Virginia Tech Satellite Tracking Station, which is structured much like a typical brick home. The measurements assisted the group in determining the power budget for the system as well as establishing the potential range of the system.

The test was conducted by making spectrum analyzer power measurements at 9 different locations around Blacksburg, three of each at approximately a quarter mile (0.405 km), half mile (0.810 km), and mile (1.62 km) from the transmitter. The spectrum analyzer was connected to a 6 dB collinear antenna, and multiple power level measurements were taken at each site by moving the antenna a few feet in each direction. These tests were repeated after moving the transmitter to its alternate site in the Tracking Station. The transmitter was made up of a signal generator, a power amplifier, and a quarter wave monopole antenna. The Effective Isotropically Radiated Power (EIRP) of the transmitter was 0.5 watts or 27 dBm.

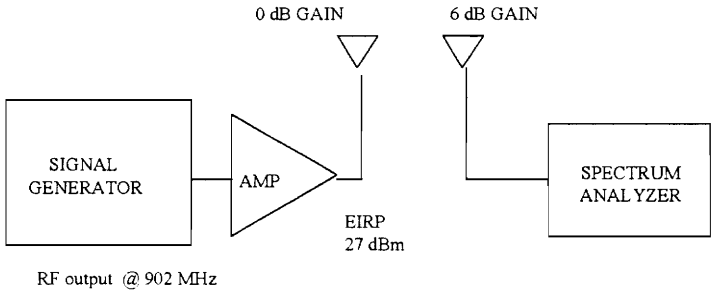

Figure 2.1 Proof of Concept Test Set Up

The results of the Proof of Concept Test are given in Tables 2.1 and 2.2 below. Path loss measurements are calculated by adding 27 dB to the received power measurement of the spectrum analyzer to account for the EIRP of the transmitter and 6 dB for the gain of the receiving antenna. EIRP is calculated by

$$EIRP(dBm) = P_{transmitter}(dBm) + P_{transmit\ antenna}(dB). \qquad [1]$$

Table 2.1 Path Loss as a Function of Distance Between Transmitter and Receiver (TX in Tracking Station)

SITE	DISTANCE(mi)	DISTANCE(m)	PATH LOSS(dB)
1	0.25	405	-132
2	0.25	405	-146
3	0.25	405	-127
4	0.50	810	-132
5	0.50	810	-169
6	0.50	810	-149
7	1.00	1620	-178
8	1.00	1620	-148
9	1.00	1620	-145

Table 2.2 Path Loss as a Function of Distance Between Transmitter and Receiver (TX in Mobile Trailer)

SITE	DISTANCE(mi)	DISTANCE(m)	PATH LOSS(dB)
1	0.25	405	-129
2	0.25	405	-149
3	0.25	405	-131
4	0.50	810	-144
5	0.50	810	-157
6	0.50	810	-151
7	1.00	1620	-178
8	1.00	1620	-155
9	1.00	1620	-157

Results from this test show that at similar distances, a local IVDS repeater will encounter a broad range of power levels in incoming messages. Taking into account that the repeater units will be stationed in the vicinity of multiple users, each a different distance away and each experiencing a different wireless path to the repeater, incoming messages can vary as much as 10-30 dB in signal power. The sites used in the Proof of Concept Test were located along roadsides in Blacksburg, Va. The sites located around the Virginia Tech campus(Sites 2, 5, and 7) experienced a greater path loss than those sites located in rural areas. These campus sites gave some indication of how the system will perform in an urban environment. Such variation may allow one user's signal to dominate others since it experiences the least amount of path loss. This same variation may allow one data packet to arrive uncorrupted even after a collision with another packet.

3.0 THEORY

In this chapter, the necessary theoretical background is introduced to provide a reference for later chapters. The first section focuses on spread spectrum techniques pertaining to the thesis. A general overview is provided as well as a discussion of the theory behind spreading data over a wideband channel. The second section introduces the interference measures used to evaluate the performance two types of receivers tested in the thesis. The final section describes the different correlation and modulation techniques used by the two receivers.

3.1 Spread Spectrum Communications

Using spread spectrum communication has many advantages: spectrum sharing, selective addressing capability, code division multiple access, low-density power spectra for signal hiding, message screening from eavesdroppers, high resolution ranging, and interference rejection. The property of interest for this thesis is its interference rejection capability. This subchapter provides some background on how a spread spectrum system performs.

3.1.1 Overview

A spread spectrum system is one that transmits messages using bandwidth much wider than the minimum required by the information being sent. Spreading messages into wider bandwidths is accomplished by modulating the messages with a wideband encoding signal. Shannon's channel capacity equation forms a basis for the spread spectrum technology and is expressed by,

$$C = W \bullet \log_2\left(1 + \frac{S}{N}\right) \qquad [2]$$

where C is the capacity in bits per second, W is the bandwidth in hertz, N is the noise power, and S is the signal power. By using logarithmic expansion, the equation simplifies to

$$\frac{N}{S} \approx \frac{W}{C} \qquad [3]$$

From the above equation, it is determined that for any set noise-to-signal ratio, the information-error rate may be lowered by increasing the transmission bandwidth.

The spectrum of a spread message appear as a *sinc* (sin x / x) *squared* function on the spectrum analyzer. The main lobe of the *sinc squared* function defines the transmission bandwidth of the spread signal. In the time domain, the sinc function appears as a rectangular pulse, and the sinc squared appears as a triangular pulse.

3.1.2 PN Sequences and Maximal Length Codes

The purposes for using codes in spread spectrum communication systems are to offer greater protection against interference, secure messages for privacy, and reduce the effect of interference and noise in a communication channel. The code "spreads" a message into a wider transmission bandwidth which, as previously described, improves the signal-to-interference characteristics of the channel. Pseudonoise (PN) codes or pseudorandom codes are most often used in spread spectrum systems. A pseudonoise or pseudorandom sequence is a binary sequence that has an autocorrelation resembling white noise. These sequences also have very low crosscorrelation between any two of them. The PN sequence controls a spread spectrum communication system by acting as a multiplier for the baseband data. Pulses of the PN waveform are called chips. The code clock determines the chipping rate or the rate at which these chips are generated. The multiplication by the PN waveform spreads the baseband data into a wider baseband data stream at the chipping rate. Modulation of this stream by the RF carrier produces the double sideband spectrum. At the receiver, multiplication by the locally generated PN

code effectively despreads the message. After that, the message is BPSK or DPSK demodulated and restored to baseband.

Most communications systems employ a maximum (or maximal in [1]) length PN code. A maximum length code is the longest code that can be generated by the shift register or delay elements of length *n*. The number of chips in a maximal length code is determined by $2^N - 1$, where N is the number of stages in the shift register or delay elements. These PN sequences have nearly identical numbers of ones and zeros, within one chip.

There are many advantages in using a maximal length code. As mentioned previously, the PN sequence will generally have an autocorrelation resembling white noise. Autocorrelation is the measure of the similarity between a signal and its phase shifted replica. The autocorrelation integral is defined by

$$\Psi(\tau) = \int_{-\infty}^{\infty} f(t) f(t-\tau) dt \qquad [4]$$

where f (t) is the PN sequence. The autocorrelation function is the time domain representation of the pulse spectral density (PSD) function in the frequency domain. For maximal length sequences, their correlation is -1 except in the area of 0 plus or minus 1 phase shift. At zero phase difference, the correlation integral becomes positive and real. Since positive autocorrelation occurs only when the signal and its replica are in phase, maximal length codes have the optimum autocorrelation. In a receiver, the incoming PN code is correlated with its stored replica. When the autocorrelation value peaks, the two code are in phase.

Cross-correlation is the measure of similarity between two different signals. The cross-correlation integral is defined by

$$\Psi_{CROSS}(\tau) = \int_{-\infty}^{\infty} f(t) g(t-\tau) dt \quad , \qquad [5]$$

where f (t) is the incoming PN sequence and g (t) is the receiver's PN code. Low cross-correlation characteristics of maximal length codes block out incoming signals with different spreading codes. Cross-correlation is important in multiple access since many

users may be operating on the same frequencies. Low cross-correlation provides isolation from foreign systems using separate codes in the same frequency band. Maximal length codes do not have the optimal cross-correlation of orthogonal codes.

3.1.3 Direct Sequence Spread Spectrum Systems and CDMA

Direct sequence spread spectrum communication (DS-SS) systems employ pseudonoise sequences to transmit wireless data packets using a single carrier frequency. By using different PN codes, multiple systems work simultaneously with little or no interference problems. This type of multiple access is called Code Division Multiple Access (CDMA) and has become very popular for mobile, cellular, and personal communications[2,3]. IVDS uses many features of CDMA to operate over its four channels. While IVDS does not actually use CDMA, the system is based on using four different codes on adjacent channels. Figure 3.1 is a simple block diagram of a DS-SS system with binary phase modulation.

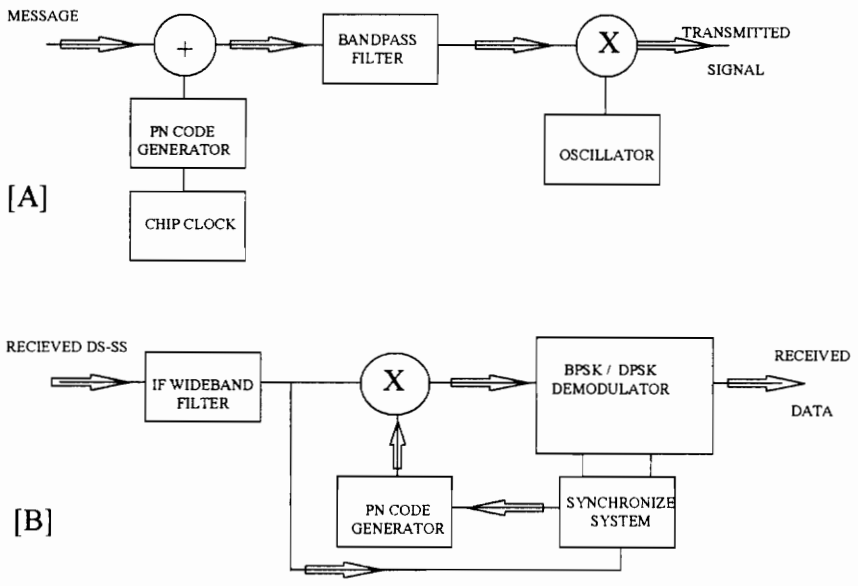

Figure 3.1 DS-SS Transmitter [A] and Receiver [B] Block Diagrams

3.2 Interference Rejection

This section focuses on interference rejection. The terms defined in this section will gauge the two receivers' collision performance. *Process gain* describes the system's gain due to spreading into a wider bandwidth; *jamming margin* defines a system's interference performance; *capture* and *near-far effects* explain the receiver's reaction to multiple inbound messages. Of these sections, the jamming margin section is the most important to the thesis because it best characterizes interference rejection.

3.2.1 Process Gain

The process gain is described as the dB difference between a processor's output and input signal-to-noise ratios. For a spread spectrum system, the process gain may be calculated by,

$$G_P = \frac{BW_{RF}}{R_{INFO}} \qquad [6]$$

where the RF bandwidth is the bandwidth of the transmitted spread spectrum signal and the information rate is the baseband channel data rate. Process gain values express a system's capability to suppress in-band interference. Since this gain is determined directly from the ratio of the two bandwidths, the RF and the information, it is not the best measure of a system's interference rejection. In general, process gain calculations will best describe a system's performance in the presence of simple in-band thermal noise. The process gain equation neglects system losses, such as ohmic losses, which will also effect a receiver's performance. For this thesis, process gain will used when considering the jamming margin.

3.2.2 Jamming Margin

While process gain will be used to characterize a system's performance by utilizing a bandwidth greater than the information bandwidth, jamming margin will be used to evaluate a receiver's capability to reject interference. Jamming margin expresses performance in hostile environments in which a processor may be faced with an interfering signal having greater power than the desired signal. The jamming margin is given by,

$$M_j = G_p - \left[L_{sys} + \left(\frac{S}{N} \right)_{out} \right] \text{ (in dB)}, \qquad [7]$$

where G_p is the process gain, L_{sys} is the system implementation losses, and $(S/N)_{out}$ is the minimum acceptable signal-to-noise ratio at the information output. For example, a system with a 29 dB process gain, minimum $(S/N)_{out}$ of 12 dB, and system losses of 2 dB will have a jamming margin of 15 dB (M_j). The receiver cannot operate in the presence of an interferer 15 dB (or more) above the desired signal. Jamming margin is more useful than process gain since these values include losses inherent in any real system. A system's jamming margin will always be less than its process gain. However, the jamming margin is harder to determine since system loss must be measured.

From the jamming margin equation, the output signal-to-noise ratio may be derived for the case in which the jammer power dominates the desired signal. The equation is given by,

$$\left(\frac{S}{N} \right)_{out} = G_p - \frac{J}{S} \text{ (in dB)}, \qquad [8]$$

where J is the power level of the jamming signal, S, the power level of the desired signal. The output S/N ratio is important because it will be used in later chapters to relate bit error rates (BER) and message error rates (MER) to jammer powers. For this thesis, a jammer or interferer will be defined as any signal within the receiver bandwidth with identical modulation and spreading code as the desired signal. This definition is different from typical jammer definition found in [1]. In [1], a jammer is described as any signal

within the receiver bandwidth and [1] usually referred in its examples to a continuous wave (CW) jamming signal.

3.2.2 Capture Effect

The behavior of colliding packets and collision studies have been widely reported in the literature. Most studies involve multiple signals transmitted by different users to arrive at a common receiver at different power levels[6]. The capture effect occurs when the receiver successfully "captures" the strongest signal in the presence of many others.

Most of the early research on the capture effect revolved around FM packet radio. Interest has resurged with wireless mobile communications research. The mobile environment is replete with multiple messages competing for a receiver. The research on the capture effect in the mobile environment considers several cases involving different traffic models, random access protocols, and retransmission strategies. Perhaps the best comparison to the one-way channel discussed in this thesis is the initial capture model described in [6] involving a mobile radio channel utilizing slotted ALOHA. The system model describes the received power as

$$P_R = R^2 e^E K r^{-n} P_T \qquad [9]$$

where R is a Rayleigh distributed random variable with unit power, e^E accounts for the shadowing (E is Gaussian with zero mean and variance). $K r^{-n}$ represents the constant for deterministic loss and P_T is the power transmitted. The model then describes the instantaneous signal to noise ratio as

$$SNR = \frac{P_{R0}}{P_N + \sum_1^k P_{Ri}} = \frac{R_0^2 e^{E0}}{W + \sum_1^k R_i^2 e^{Ei} \left(\frac{r_i}{r_0} \right)^n} \qquad [10]$$

where subscript 0 is used for the intended user, W is the background noise power (kTB), and r is the distance from the receiver. The model neglects the effect of noise since the

noise power is significantly less than interference power in the multiple access scenario. This simplifies the SNR to a ratio of the desired signal power to the summation of interference powers. The outage is defined as the event that the S/N falls below a predetermined threshold, *b*, sometimes called the capture ratio[6]. Assuming that a user's packet is unrecoverable during an outage condition, the probability of successfully transmitting a packet is

$$P_s = P[SNR > b] \qquad [11]$$

or simply the probability of success is determined by the probability of the SNR being above the threshold, represented in the equation (11) by *b*. This probability is defined for a user at distance *ro* from a receiver by

$$P_s(r_0) = P\left[P_{R0} > b\sum_1^k P_{Ri}\right] = P\left[R_0^2 > b\sum_1^k R_i^2 e^{Ei-E0}\left(\frac{r_i}{r_0}\right)^{-n}\right] \qquad [12]$$

where the relation of distances between interferer and desired signal is implicitly shown.

The statistical model for the IVDS one-way channel, described in [5], shows that the likelihood of a desired signal colliding with more than one interfering message is **significantly** smaller than the probability of just one interference signal colliding with the desired signal. Thus, for this channel, the summation falls out of the equation to become

$$P_s(r_0) = P[P_{R0} > b\,P_{Ri}] \qquad [13]$$

where now the probability of a successful packet transmission relies on the ratio of received powers.

3.2.3 Near-Far Effect

The capture effect resembles another phenomenon also referred to in literature as the near-far effect. Near-far effect describes the case of multiple transmitters sending equal power signals to a common receiver; the closest transmitter with the smallest path loss will be captured by the receiver. For example, the Proof of Concept Test discussed in

Chapter 2 showed how received power levels were generally higher when the distance between receiver and transmitter was smaller. Thus, path loss at the shorter ranges was smaller. The near-far phenomenon would describe why a user at the shorter range may dominate the user at the greater range where both are competing for the same receiver.

3.3 Correlator Types and Modulation Techniques

This section is dedicated to describing the different modulation techniques and correlator types used by the two systems to be tested. One receiver must acquire phase lock to the transmitted signal while the other relies on asynchronous detection. These differences in the demodulation and the type of correlator used will be important later when analyzing the results of the collision tests. Important concepts in this section include PN lock or acquisition time, coherent (synchronous) versus noncoherent (asynchronous) detection, and basic receiver topologies.

3.3.1 Modulation Techniques

In a direct sequence system, the encoding signal is used to modulate a carrier. Phase-shift keying is most often used to toggle the carrier phase to represent a digital one or zero. The two modulation types seen in this paper are Binary Phase-Shift Keying (BPSK) and Differential Phase-Shift Keying (DPSK). BPSK is used by the Loral receiver whereas the Grayson receiver uses DPSK. These two receivers are compared in this thesis and will be described in detail in following chapters (see Chapter 4).

In BPSK, the carrier signal is switched between two phase values separated by 180 degrees which represent a binary one or zero. Setting the carrier amplitude to some A_c and the energy per bit as

$$E_b = \frac{1}{2} A_c^2 T_b \quad , \qquad [14]$$

the BPSK signal can be represented as either

$$S_{BPSK} = \sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c + \theta_c\right), 0 \le t \le T_b \qquad \text{(binary 1)} \qquad [15]$$

or

$$S_{BPSK} = \sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c + \pi + \theta_c\right), 0 \le t \le T_b \quad \text{(binary 0).} \qquad [16]$$

A BPSK receiver that uses coherent demodulation requires knowledge of both phase and frequency of the incoming carrier. Often this is accomplished by using a phase locked loop at the receiver. A second method of coherent demodulation uses a square law device used to generate an amplitude modulated sinusoid at twice the carrier frequency. A frequency divider then recreates the waveform. Next a multiplier mixes the output of the divider and the original signal and sends the resulting signal into an integrate and dump filter. From this filter, the signal is sent to a decision circuit to determine whether a one or zero was transmitted. The diagram below illustrates such a BPSK receiver.

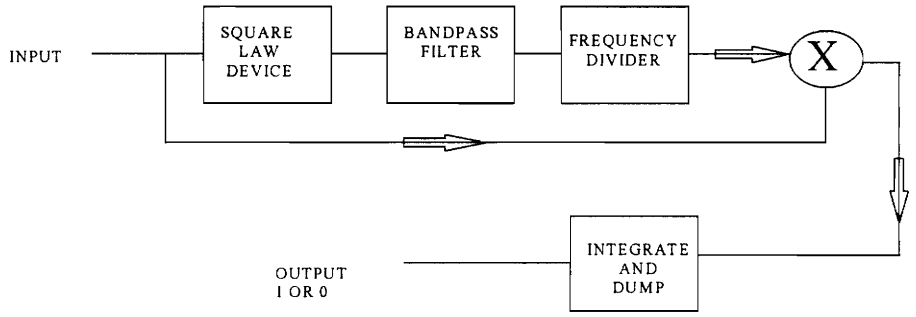

Figure 3.2 BPSK Receiver Block Diagram

Unlike BPSK, Differential Phase Shift Keying (DPSK) is a noncoherent modulation which requires no absolute phase reference at the receiver. This type of receiver is cheaper and less complex than its coherent counterpart. At the transmitter, the DPSK message is differentially encoded then modulated using a BPSK modulator. The differentially coded sequence $\{d_k\}$ is generated from the input binary sequence $\{m_k\}$ by complementing the modulo-2 sum of m_k and d_{k-1}. [3]. The resulting differential signal becomes a function of the input binary sequence and the previous differential symbol. The relationship can be represented by

$$d_k = \overline{m_k \oplus d_{k-1}} \qquad [17]$$

At the receiver, the original message is demodulated by using the complimentary process. The Figure 3.3 shows a DPSK transmitter and receiver.

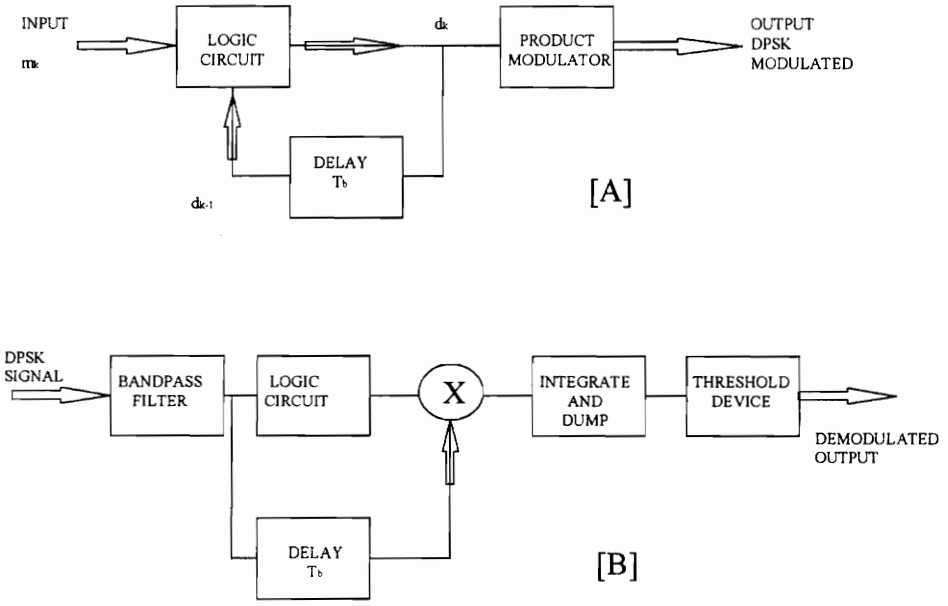

Figure 3.3 DPSK Transmitter [A] and Receiver [B]

Comparing the two modulations, referencing Couch's Fig. 7-14[2] or Figure 3.4 in this thesis, the error performance shows that BPSK is only slightly better than DPSK. For the same error probability, DPSK signaling requires about 1 dB of additional E_b/N_o (energy per bit / noise energy) than its BPSK counterpart for similar performance.

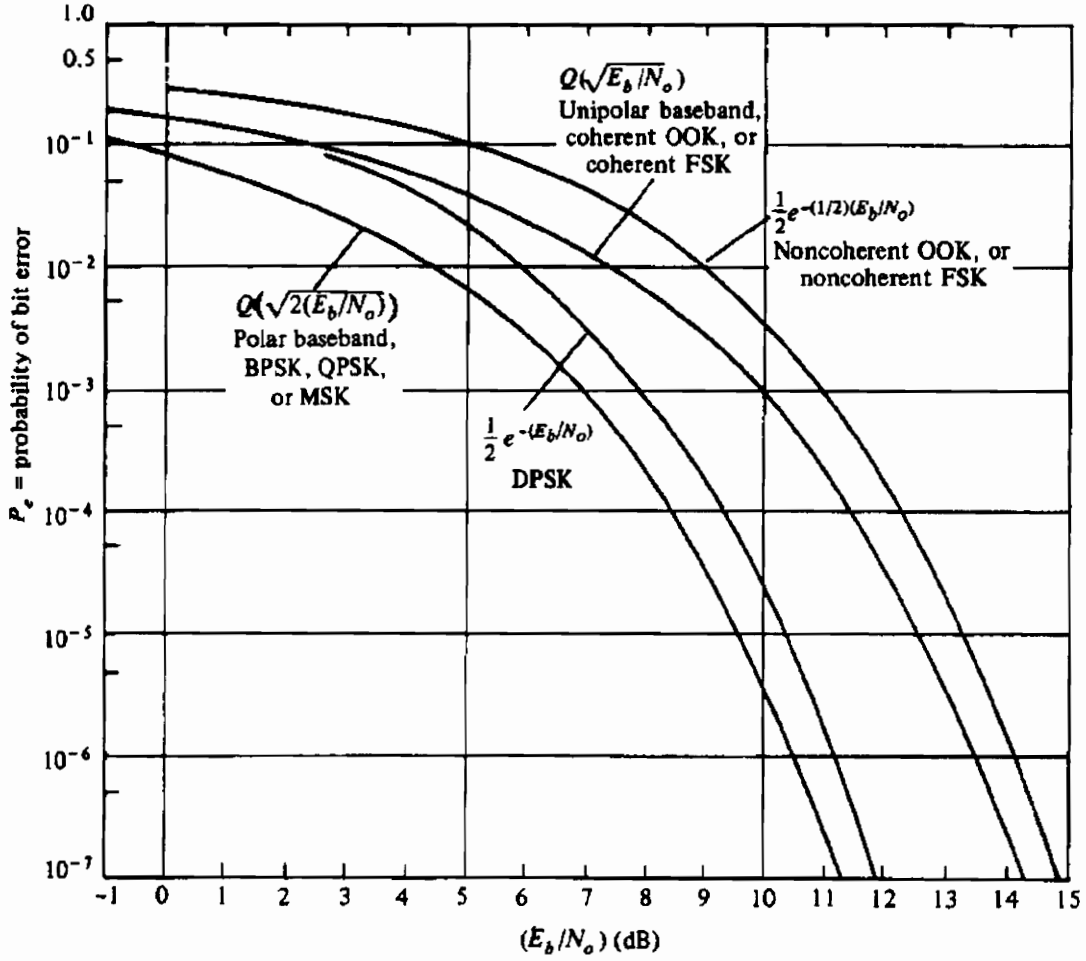

FIGURE 7-14 Comparison of the probability of bit error for several digital signaling schemes.

Figure 3.4 Modulation Comparisons [2]

In practice, DPSK is used more often since the DPSK receiver requires no carrier synchronization circuit.

3.3.2 Receiver Synchronization

Synchronization is the process that allows the receiver to lock on to the code of a spread spectrum packet. Locking onto the phase of the received code, the receiver may demodulate and despread the packet, leaving the valid baseband data to be read. Two types of synchronization pertinent to this paper are "sliding" correlator synchronization and matched filter synchronization.

The simplest correlator, the "sliding" correlator, obtains synchronization by operating its code-sequence generator at a slower or faster rate than the transmitter's code generator. This allows the two codes to "slide" by one another until the receiver code comes in phase with the transmitter code. This condition is referred to as a PN lock. Once lock is achieved, the receive clock signal is changed to match the transmitter's clock signal. This is a coherent process since it requires the demodulator to acquire phase lock to the carrier as well as PN lock to the transmitter's signal. The simplicity of such correlators lies in shifting the receiver's code clock at a different rate. Figure 3.5 illustrates the synchronization steps for this type of correlator.

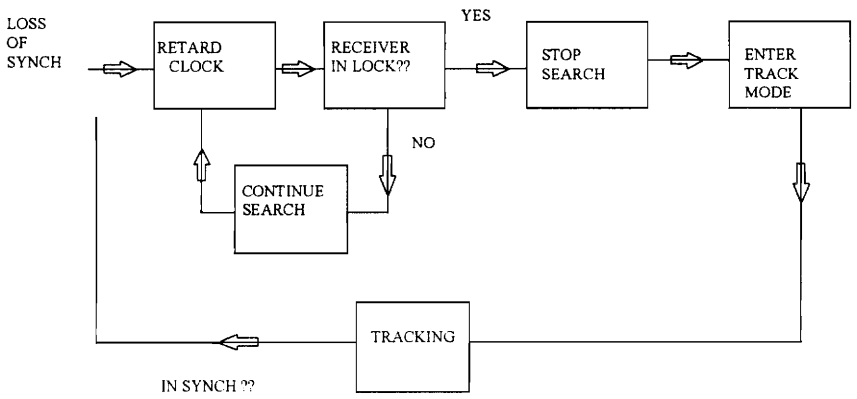

Figure 3.5 Sliding Correlator Block Diagram

The disadvantage of the sliding correlator is its long lock time. The process by which the receiver code generator comes into phase with the incoming signal is stochastic. Correlator lock or PN lock time is dependent on the system's chip rate. For synchronization, the correlator may have to "see" the PN sequence a set number of times before acquiring a PN lock. Thus, the first few bits to be received are usually lost. Therefore, incoming messages must have a preamble or buffer header equal to the longest possible synchronization time.

The matched filter synchronizer is the second correlator discussed in this thesis. The matched filter is composed of multiple delay elements also called taps. The Figure 3.6 is a block diagram of a baseband digital matched filter.

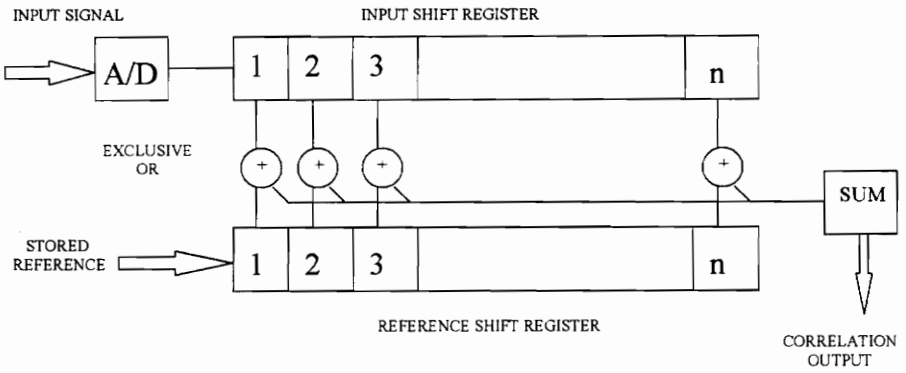

Figure 3.6 Baseband Digital Matched Filter

The matched filter correlator sums the input sequence with a stored reference at each bit in the shift register. Sums from each tap are again summed and compared to a set threshold value at the output to the correlator. Correlation occurs when the sums exceed a set threshold, representing the peak cross correlation. From this threshold point, the message is despread.

The matched filter is more efficient than a sliding correlator since it can theoretically achieve PN lock with the first bit of message information. Lock times and long preambles are not an issue. However, the matched filter circuitry is more complex than that of the "sliding" correlator.

4.0 EQUIPMENT

This chapter will discuss the two types of receivers used for the collision study. The testing was conducted in two separate phases. The first phase tested the Loral Spread Spectrum Evaluation System's collision characteristics while the second phase focuses on the Grayson Equipment. The purpose of this chapter is to analyze each receiver to achieve a full understanding of how data packets are processed. The previous chapter describes the general operation of the two receiver types, but this chapter will go into specific function blocks of each receiver.

4.1 LORAL Equipment

The EB-100 Digital Spread Spectrum Evaluation System designed by UNISYS, now LORAL, bases its architecture on the PA-100 Spread Spectrum Demodulator and XILINX Field Programmable Gate Array. The PA-100 is an Application Specific Integrated Circuit(ASIC) used in satellite modems, personal communication systems, wireless networks, and cellular radio. The PA-100 is very comprehensive and includes all major subsystems required for a spread spectrum receiver, including chip and data rate matched filtering, automatic gain control, carrier frequency and phase recovery, chip and data rate timing recovery, PN code acquisition and tracking, and data recovery[4]. By setting the dipswitches on the evaluation boards, the transmitter/receiver pair may be set for different chipping rates, data rates, and modulation schemes. The basic functionality of the chip for spread spectrum use includes despreading and demodulation, carrier recovery, PN code detection and tracking, synchronization, and automatic gain control. The EB-100 Spread Spectrum System is capable of using four data rates, two chipping rates, and two types of BPSK spreading, differential and non-differential. The boards are able to use any combination of data rates and chipping rates since the clocks are programmable.

The EB-100 transmitter is controlled by an Intel 8751 Microprocessor that reads the input dipswitches and executes routines with the XILINX to encode and modulate data entering from the serial port. One drawback to the transmitter is that the spreading code is always transmitted even if no serial inputs are present. Thus, it is difficult to determine on a spectrum analyzer when a message is being transmitted. In the next section, a circuit is discussed that corrects the problem of always transmitting. The EB-100 receiver is likewise controlled by an Intel 8751 microprocessor that enables and loads the despreading code into the PA-100 chip.

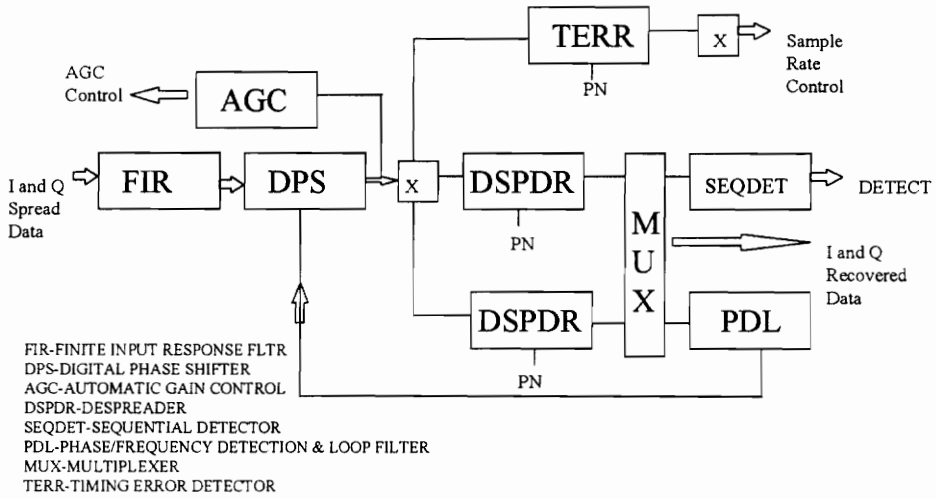

Figure 4.1 PA-100 Block Diagram

4.1.1 EB-100 Receiver \ PA-100 Spread Spectrum Chip

The PA-100 chip performs many of the functional blocks that make up the EB-100 receiver. The first block is the Finite Impulse Response (FIR) and DC removal filters. The single-tap FIR filter removes intersymbol interference caused by pre-sampling filters. The DC removal filter simply removes all DC content from the input signal.

Another block realized inside the PA-100 is the Digital Phase Shifter(DPS). The function of the DPS is to perform the complex rotation of the vector formed by the I and Q channels, or in the BPSK mode only the I channel (the 90 degree shifted Q channel is unused) . The rotation is controlled and determined by an 8-bit phase command received from the phase loop filter.

After a signal passes through the first two blocks, it is sampled by an Automatic Gain Control (AGC) block. The AGC circuit computes the sum of the outputs from the DPS, compares the sum to a reference level, and accumulates and scales the difference. The output of the AGC is a 12-bit control word that is used to control an external variable gain amplifier that adjusts the input signal level. The AGC block also has circuitry to detect a saturation condition that may be used to override the normal operation. Basically, this block equalizes the input signal power by controlling the input amplifier. The AGC acts like a signal conditioner for the next block.

After the AGC block, the signal goes into the despreaders (DSPRDs). The despreaders remove the PN codes from the I and Q channels from the incoming signal. The two channel despreading occurs by eXclusive ORing (XOR) the I data with the A PN code and the Q data with the B PN code (A and B symbolize separate codes). This process describes Quadrature Phase Shift Keying (QPSK) demodulation. For the BPSK case, only the I channel is used. Before XORing the proper codes with the incoming signal, the despreaders must first wait for the sequential detectors to achieve a PN lock.

The sequential detector (SEQDET) consists of data removal circuits, a bias subtractor, a correlation accumulator, timer, and an acquisition/tracking controller[4]. During acquisition, the correlation accumulator is set to a positive value while the output is tracked by the acquisition controller. Once the output from the accumulator goes negative, the local PN code is "slipped" to allow code synchronization. This process is repeated after a set amount of delay. If the correlator output remains high until the timer expires, the detect signal goes high. After code detection, the accumulator is initialized to a negative value, and the output is monitored at intervals set by the timer. If the

accumulator output is positive, correlation is assumed. If the accumulator output is negative, loss of correlation is assumed. The acquisition/tracking controller resets the PN DETECT flag and attempts to reacquire the PN detection.

After another accumulator, scale, and dump block, the signal enters the Phase Loop Filter (PDL in Figure 4.1, which means Phase Detect Loop). The PLF is a first-order digital filter used to form a carrier recovery loop. The output of this filter is used to control the DPS using a byte command. This block is necessary to achieve Phase lock for coherent detection.

The Timing Error Detector (TERR) also processes pre-accumulator outputs. Much like the despreaders, the TERR despreads synchronized PN code. When the output is non-zero, the detector uses the non-zero mean to estimate the polarity and magnitude of the timing error[4]. This block helps control the timer irregularities and sample rate control.

4.3 GRAYSON Equipment

The equipment used for Phase II will be referred to as the Grayson equipment since the receiver is based on the Wireless Measurement Instrument (WMI) that was designed and built by Grayson Electronics. The transmitter-receiver pair for this phase make up the prototype design for IVDS .

The prototype transmitter was designed by combining multiple evaluation boards. The main components of the transmitter prototype are the Analog Devices ADSP-2181 DSP chip, the Motorola MC145190 Phase-Locked Loop Frequency Synthesis Chip, and the Maxim 2402 Amplifier/Transmitter. The supporting evaluation boards for each of these three components implemented the design of a working transmitter.

The ADSP-2181 DSP chip is supported by the ADSP-2181 EZ-KIT LITE Evaluation Board (EVB). The EVB has two serial ports. One of the ports is dedicated to a CODEC chip that will be used on the transmitter to process the audio encoded commercial messages (this is a separate IVDS project). The second serial port allows

the user to download programs from a PC using software that comes with the EVB. In addition, the EVB adds an EPROM to store program information.

The ADSP-2181 DSP chip itself is very powerful. The chip executes all instruction codes in single clock cycle of only 30 nanoseconds. The architecture is based on using 16 bit words for data memory and 24 bit words for program memory. In addition to its two serial ports, it also has 8 programmable input/output pins that can be addressed individually, or as a group, or as one 8 bit parallel port.

For the transmitter, the DSP chip is used to generate the differential coding and spreading code for a given message. This is done in the software programming that uses the XOR function to add the proper differential coding. As for the spreading code, it is applied to every data bit in the message to encode the given message properly. There were 50 code bits per every data bit in the modulated message. The chip provides the modulated data to the Maxim transmitter (described later in this section) in finished form. At the same time, the DSP chip also loads the correct divide ratios into the frequency synthesizer chip through serial communication.

The Motorola MC145190 Evaluation Kit(EVK) contains the MC145190 PLL Frequency Synthesis chip as well as an area for the Voltage Controlled Oscillator (VCO). A 25D serial connector allows the MC145190 chip to be loaded serially from a PC or the ADSP-2181 DSP chip's serial port. In order to set the chip to a specified frequency, the proper divide ratios must be entered into the chips R, A, and N registers. A frequency synthesis chip relies on these registers to provide the output frequency by this relationship:

$$f_{out} = \frac{f_{ref}}{R}(64 \bullet N + A) \qquad [18]$$

The reference frequency is given on the EVK by a 10 MHz crystal. The MC145190 is loaded by addressing three registers serially. These are the C, R, and A registers. The A register is actually a combination of the normal A and N registers used by frequency synthesis chips. The R register is for R divide values, but the C register is simply a control register for the chip. To load these registers, the DSP chip provides three serial outputs:

Enable, Data, and Clock. The MC145190 chip required a turn on or enable signal to tell it to receive data. Data is latched on the falling edge of the clock signal, which is also supplied serially by the DSP chip. Loading all registers takes three data bytes from the DSP, serially loaded on three separate output pins. Once the DSP sets the synthesizer, the synthesizer locks the VCO at the desired frequency, establishing a specified carrier.

The Maxim 2402 EVB is simply made of the transmitter chip, a few bias circuits, power pads, and SMA connectors. The Maxim chip mixes the output of the VCO with the modulated output data from the DSP chip. It is also a power amplifier for the spread message capable of 100 mW output or 20 dBm. The Figure 4.2 is a connection diagram for the prototype transmitter.

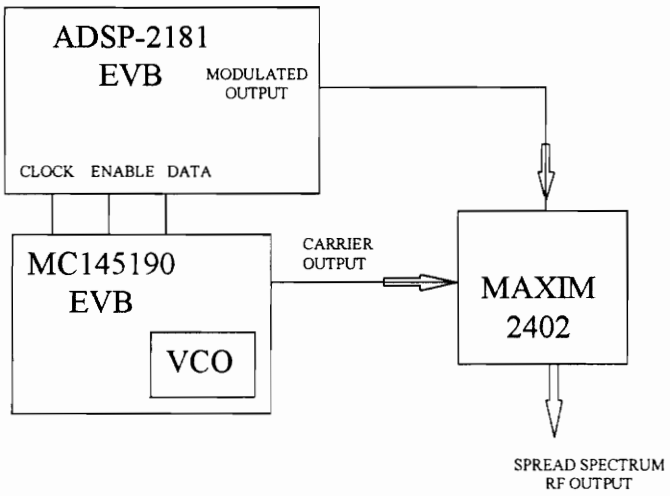

Figure 4.2 IVDS Prototype Transmitter Connection Diagram

4.3.1 Grayson Receiver

The Wireless Measurement Instrument (WMI) chassis, a product designed and manufactured by Grayson Electronics, and motherboard combined with a special decoder

board supporting the STEL-2000 spread spectrum demodulator chip and superheterodyne radio receiver make up the prototype IVDS receiver. Much of the WMI material is proprietary and therefore will not be discussed in great detail. The basic WMI motherboard and KERNEL software supported a Motorola 68HC306 Microprocessor which in turn controlled numerous Motorola 68HC05 Microprocessors. Four 68HC05 Microprocessors control decoder board inputs. The combined WMI KERNEL and CWT in-house software allowed the WMI to queue messages from each of the four decoder boards, run Cyclic Redundancy Checks (CRC) on each message, eliminate redundant messages, and communicate serially to a PC.

The superheterodyne radio receiver downconverted the incoming 900 MHz messages to 20 MHz. The radio is tuned to the desired frequency by the Dallas DS80C320 Microprocessor (based on the Intel 8051 8-bit microprocessor) on the decoder board. The Dallas chip also loads the STEL-2000 chip with the proper despreading code.

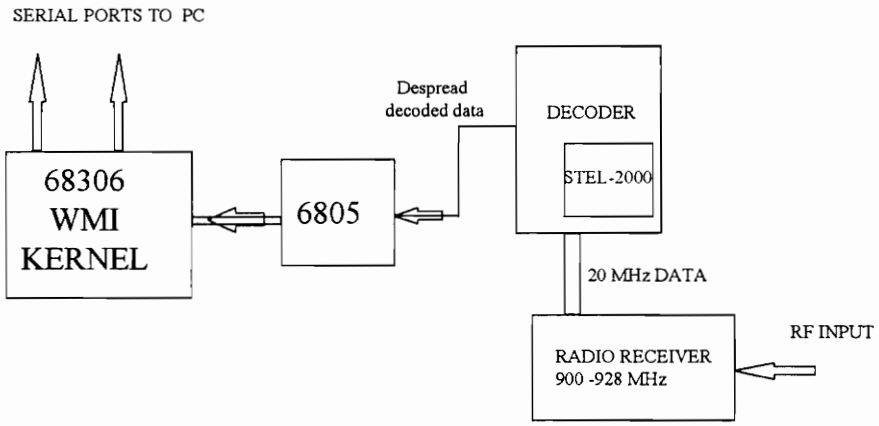

Figure 4.3 IVDS Prototype Receiver Block Diagram

4.3.1.1 Grayson Receiver / STEL-2000A Spread Spectrum Chip

The Zilog STEL-2000A Spread Spectrum Chip performs all digital signal processing required to implement a direct sequence spread spectrum receiver. The STEL-2000A's functional blocks include a digital downconverter, a PN matched filter, and a DPSK demodulator.

The first functional block an input encounters as it enters the STEL-2000A is the Digital Downconverter. Input signals are passed from the radio receiver at the 20 MHz IF. A Numerically Controlled Oscillator (NCO) is the local oscillator. The NCO also has a frequency tracking loop that accurately converts the IF signal to baseband. In Quadrature Sampling Mode, two Analog-to-Digital Converters (ADCs) provide both I and Q input signals. In Direct IF Sampling Mode, only one ADC is used to provide the I channel data. The output of the ADC is then fed into an integrate and dump filter.

Following the integrate and dump operation, the signal enters the PN Matched Filter block of the STEL-2000A chip. The filter is a programmable 64-tap PN matched filter. Thus, the PN sequence is limited to 64 bit code or smaller. The filter coefficients may be programmed to accommodate two separate PN codes, one for the Acquisition/Preamble Registers and one for the Data Symbol Code Coefficient Registers. The receiver is set up in acquisition mode and the filter registers are loaded with the Acquisition \ Preamble Coefficients. Once the preamble is successfully detected, the chip automatically switches the register contents to the Data Symbol Code Coefficients. A Front End Processor (FEP) averages the incoming samples over the chip period by summing each consecutive sample. The FEP then provides a 3-bit output word that represents each bit of data entering the delay line. The delay line consists of 64 multipliers that multiply the 3-bit word by 0, 1, or -1 according to the stored PN coefficient in its respective register. These delay line products are then added in the I adder (and Q adder for QPSK modulation) to form the sum of products. This sum represents the complex cross correlation factor. The operation is realized by the following equation:

$$OUTPUT_I = \sum_{n=1}^{n=64} Data_{n(I)} * Coefficient_{n(I)} \qquad [19]$$

The output of the I (and Q) in 10-bit format is sent to the Power Detector which computes the magnitude of the I (and Q) channel correlation. The Power Detector sends another 10-bit word to the Symbol Tracking Processor. This 10-bit word represents the power level of the correlated signal over the chip period. This output power reach a maximum level once per chip period when the PN code of the incoming signal and the stored PN code are aligned. At this peak power, the I (and Q) channel is optimally despread. This signal power is compared to a stored threshold located in a user programmable register. A symbol clock pulse is generated each time the correlation output exceeds the threshold. Two threshold values are stored in the threshold register, one value for the Acquisition \ Preamble Threshold and one for the Data Symbol Threshold.

To remove the differential encoding, the Differential Demodulator calculates the dot and cross products of the I and Q channels. For BPSK, the demodulator calculates only the dot product. Dot and cross products are calculated by the equations below.

$$\begin{aligned} Dot(k) &= I_k I_{k-1} + Q_k Q_{k-1} \\ Cross(k) &= Q_k I_{k-1} - Q_{k-1} I_k \end{aligned} \qquad [20,21]$$

Differential coding of the source data implies that an absolute phase reference is not required, thus knowledge of the phase shift between successive symbols is derived from the dot and cross products [8].

The following diagram illustrates the functionality of the STEL-2000A receiver chip.

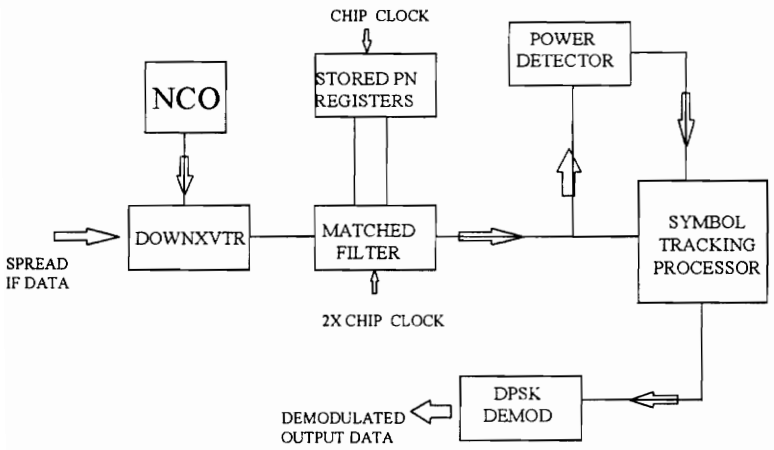

Figure 4.4 STEL-2000A Receiver Block Diagram

5.0 PHASE I TESTING

This chapter describes the first phase of testing. The first section explains the equipment set up which involved additional hardware and assembly programming for control. The following sections give some examples of the messages generated for the test. Both of these sections are relevant to the validity of the test since the testing is trying to replicate IVDS collisions. The chapter will then switch focus from the actual hardware and software description to calculating bit and message error rates. Error rate data will be used in Chapter 7 to compare the performance of the two types of receiver.

5.1 Phase I Setup

The first phase of collision testing involved the Loral Digital Spread Spectrum Evaluation System along with a PC, two Motorola 68HC11s, two variable attenuators, a 3 dB coupler, and a switching circuit. The goal of this phase was to study the receiver performance in a closed loop environment in which a desired signal is initially received and then "collided" with a similar co-channel interference signal of variable power. Tests were performed using multiple jammer and desired signal powers, exploiting the full dynamic range of the Loral receiver. The area of interest for the tests is the point at which the jammer power begins to cause significant message errors.

The strategy used for this phase of testing was to transmit continuous data packets from one transmitter while switching the second transmitter on at the beginning of each new message. The receiver will have initially captured the desired signal and locked on to both its phase and PN sequence before the interference signal is transmitted. This testing strategy insures that the receiver has first locked on to the primary transmitter or to the desired signal. It then tests the receiver's capability to reject the jamming signal during packet transmission. Figure 5.1 explains the message format used for this testing strategy.

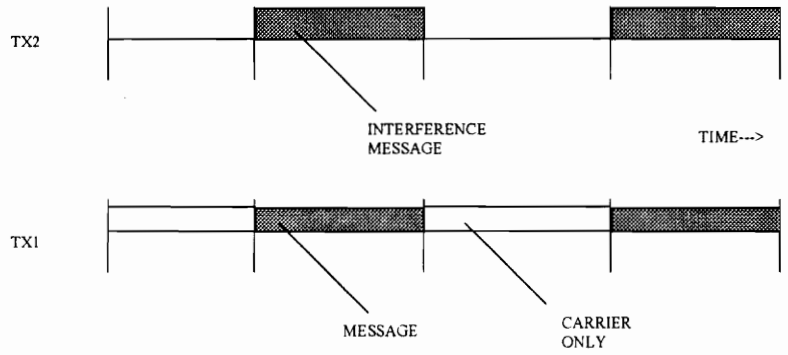

Figure 5.1 Message Transmission Strategy

To implement this message transmission strategy, two separate Motorola 68HC11 microprocessor evaluation boards were programmed. The first HC11 was programmed to control the switching of both transmitters' carriers. Since the Loral transmitters were designed to transmit the PN sequence at all times, it was important to modify the circuit board to switch the jamming transmitter on and off. Upon starting the program, the microprocessor would enable the primary transmitter's carrier for a short duration, approximately 6 ms. This would allow the receiver ample time to lock on to the PN and phase reference of the primary transmitter. After this brief delay, the HC11 would enable the jamming transmitter carrier and begin sending packets of data to the primary transmitter. Subsequently, the jammer transmitter would receive messages from the second HC11, which is continuously transmitting a jammer message. Data packets from the HC11 were sent to the transmitters at 9600 bits per second (bps). Each packet was 7 bytes long. The number of bytes was chosen to simulate the IVDS message, which is 23

bytes long at 40 kbps. Seven bytes at 9600 bps and 23 bytes at 40 kbps have roughly the same **message length** of about **4 ms**. At the conclusion of each packet transmission, the first HC11 would disable the jammer transmitter's carrier and wait for a small time delay. The first HC11 was programmed to repeat the process of switching the jammer on, sending a data packet, turning the jammer off, delaying, and restarting 1000 times.

The HC11 used a special switching circuit added to the Loral transmitters that is wired into the HC11's BPORT, a simple 8 bit parallel output port. Toggling an output pin on the BPORT of the HC11 allowed the microprocessor to control the switching of both transmitters. The circuit diagram in Figure 5.2 describes the switching circuit. The HC11 would send a high bit (logic 5V) to provide D1 a path to ground, turning off Q1 and turning on Q2, which enables the transmitter. A low bit (logic 0) would turn off Q3 and Q2, turn on Q1, and disable the transmitter.

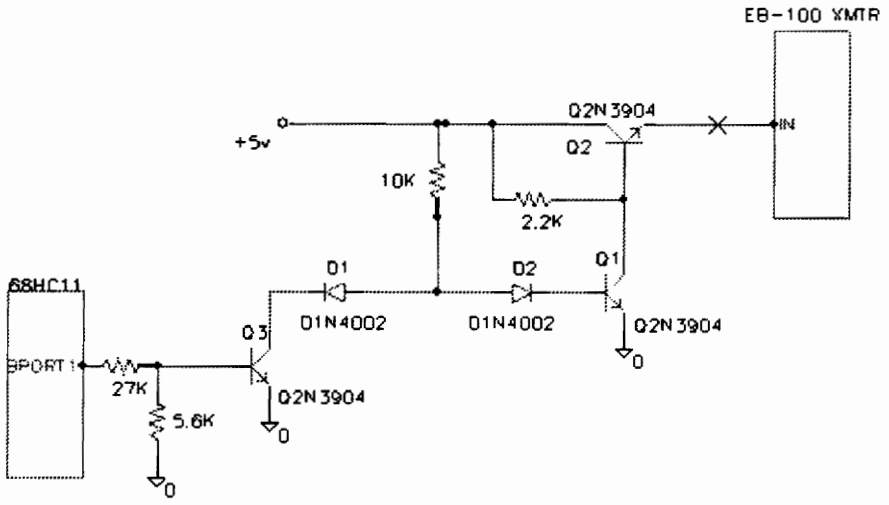

Figure 5.2 Switching Circuit

In this test, both Loral transmitters are set in the same mode of operation. Both are set to operate at 8 Mcps spreading and 9600 baud, corresponding to a process gain of 29 dB. Both transmitters are connected to Hewlett-Packard variable attenuators via

coaxial cables with BNC connectors. From the attenuators, each output is then connected to the 3dB coupler. The coupler output is connected to the receiver, using coaxial cable with BNC connectors.

The receiver is connected to the PC through COM2. By using the "log" command in KERMIT software, the PC can capture each testing session. KERMIT stores the session in a data file that can be viewed by using a text editor or word processor.

Approximately 500 data files were created in Phase I, each data file containing around 1000 data packets. The files were labeled by the trial number, the power level of the primary transmitter, and the relative power level of the jammer transmitter. There were 5 trials labeled A, B, C, D, and E. The power level of the primary signal was varied from -45 dBm, the highest power, to -85 dBm, the lowest power, in increments of 5 dB. The relative jammer power was varied from having equal power, 0 dB difference, to having 100 times the desired signal power, 20 dB, in increments of 2 dB.

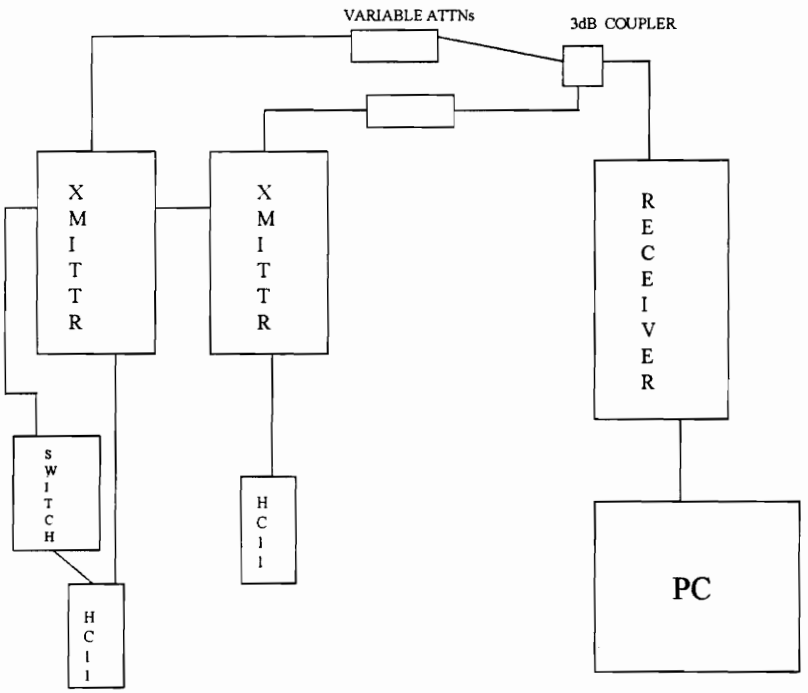

Figure 5.3 Phase I Set Up for Loral Equipment

5.2 Test Messages

The following is a sample of a test message described in the previous subchapter that arrived uncorrupted at the receiver.

ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst
ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst
ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst
ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst ahtst

Compare this file to the test message with multiple bit and message errors below.

ahtst ahtst ahtst axtst a~>-w ah□st ahtst a~tst aztwt ahvst ahtst al|t ah{.w ahtst ah}□w ahtst aht{t ahtst
al:.w aht>w ahu.w ah~st ahvwt ahtst ahtst ax:wt ahtst ah}ut aht□w ahtwv a|□st ahtst ahtst ah:o] al|w
ah}st ahtwt ah_.w ahtst ahust ahtst ahu{t ahtst aht.w ahtqt aht□r ahv{t ahtst ah}st ahtwt axtst ahtsv ahust
ahuQ□ aht{t ahtst ahtst ahtsv ahz□w ahtQ□ aht>w a|~st ahtwt ah{.w ahtst alu~w aht{t ah{?w ahtst ahtst

The corrupted file has multiple bit and message errors. Since KERMIT was used to log the test messages, it converts all binary data to its ASCII equivalent. In some cases, a bit error occurs and changes what was meant to be a printable character into the small squares that seem to appear in corrupt packets. This merely represents a non-printable character. The actual binary equivalent is still readable.

5.3 Output Files

Output files were generated by using a C program which inputs the received test message and calculates bit error and message error information. For each of the 500 received test message files, a corresponding output file was generated. Figure 5.4 is an example of a typical output file.

Message error distribution
total # of messages with 1 byte error : 211
total # of messages with 2 byte errors: 110
total # of messages with 3 byte errors: 80
total # of messages with 4 byte errors: 22
total # of messages with 5 byte errors: 0

Byte error distribution

total # of bytes with 1 bit error	: 286
total # of bytes with 2 bit errors	: 201
total # of bytes with 3 bit errors	: 105
total # of bytes with 4 bit errors	: 67
total # of bytes with 5 bit errors	: 92
total # of bytes with 6 bit errors	: 1
total # of bytes with 7 bit errors	: 0
total # of bytes with 8 bit errors	: 7

********** TOTALS **********

total # of messages	: 999
total # of wrong messages	: 423
message error rate	: 0.42342
total # of wrong bytes	: 759
total # of wrong bits	: 1793
bit error rate	: 0.03739

Figure 5.4 Sample Output File

5.4 Bit Error Rate

As seen in Figure 5.4, the C program calculated the overall bit error rate for each file. After generating these files, the bit error rate data was incorporated into a MathCad file to find the Mean Bit Error Rate for each power level. However, the bit error rate is not the most objective gauge for the two receivers under testing. The thesis concentrates on comparing Message Error Rates (MER) instead because in Phase II, the jammer and desired packets are not synchronously transmitted at the same time. In Phase II, the first 6 bytes will always be received before the jammer packet collides.

5.5 Message Error Rate

The Mean Message Error Rate was calculated for each receiver power level. The MER data represents the most subjective data collected in the testing phases which will be used later in the comparison study. MER was calculated by taking the percentage of total received messages compared to received corrupt messages. Mean values were derived by averaging the five MER values at each receiver power level. The following figures

represent the mean MER found in the Phase I Testing. Each graph plots the MER versus power of the interferer signal over a 20 dB scale X-axis. Analysis of the data is given in Chapter 7.

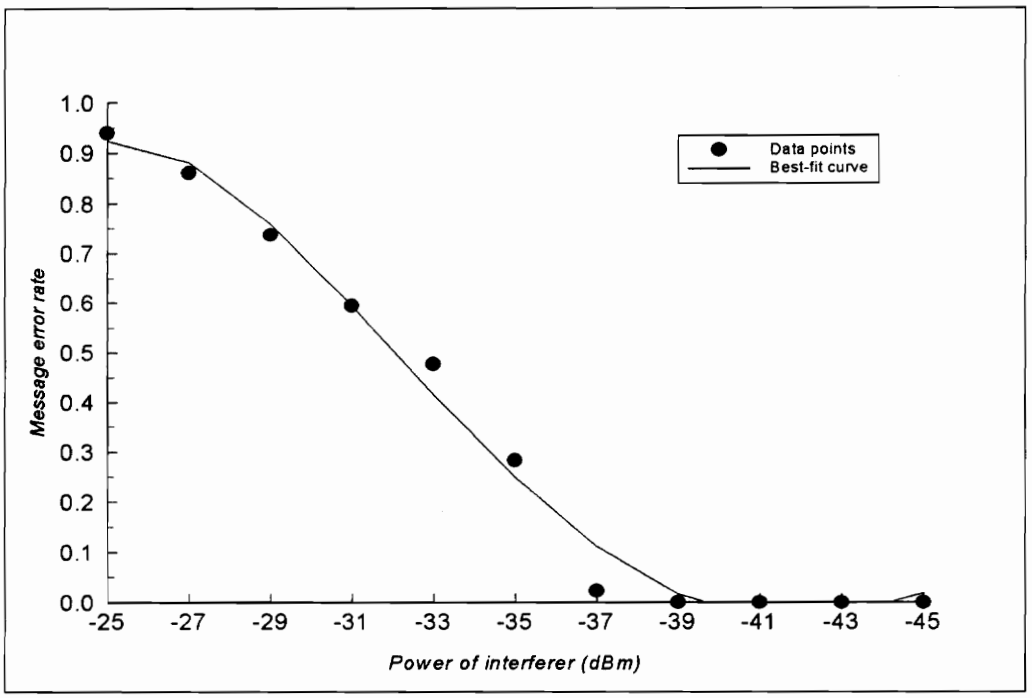

Figure 5.5 - Message error rate vs. interferer power for message power = - 45 dBm.

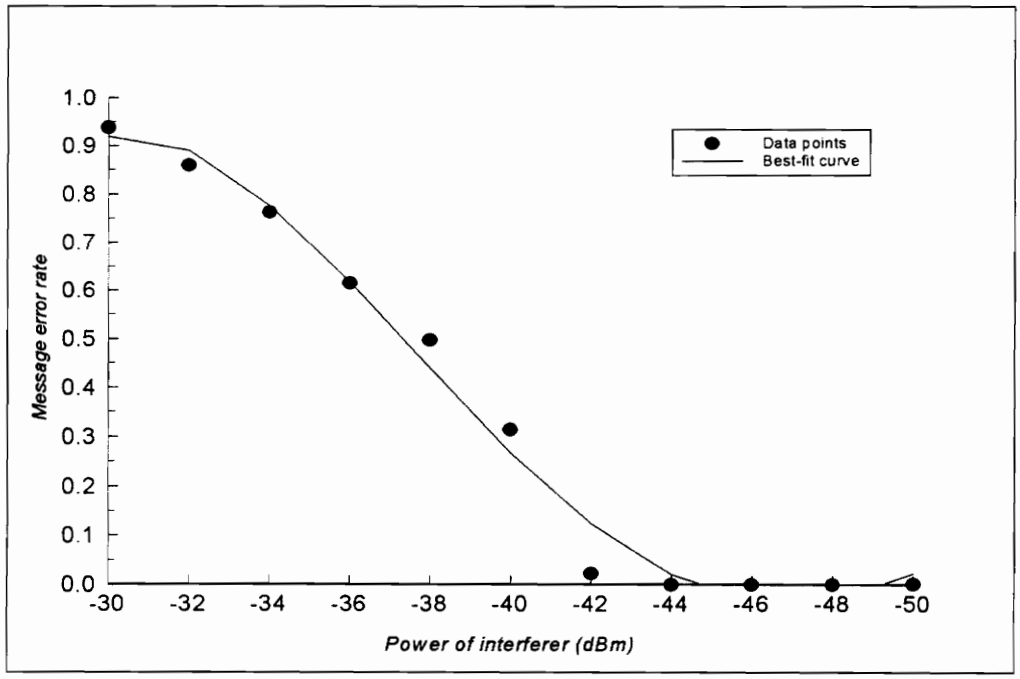

Figure 5.6 - Message error rate vs. interferer power for message power = - 50 dBm.

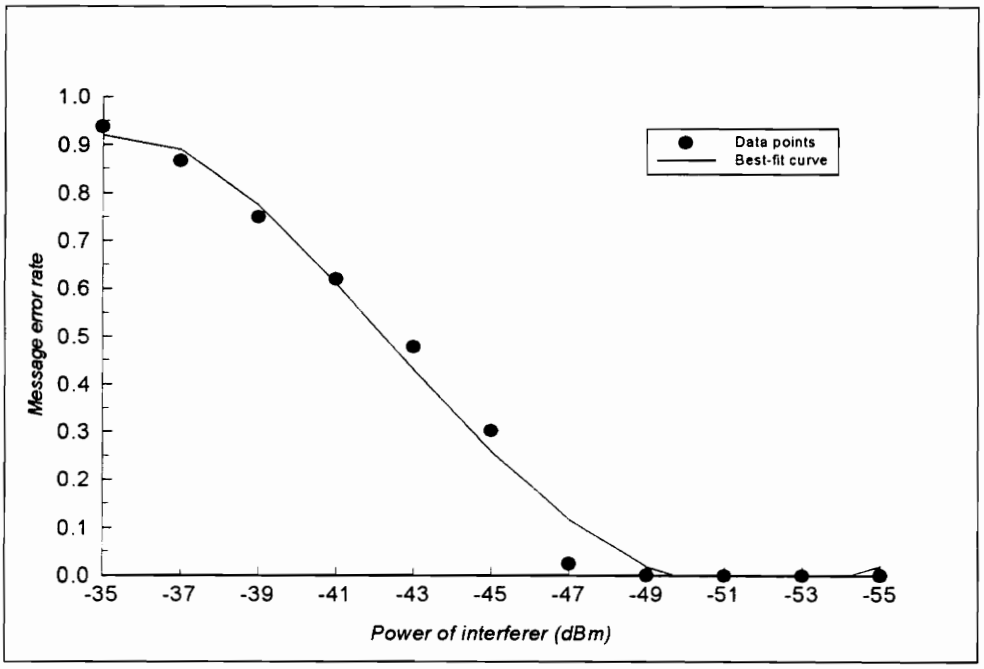

Figure 5.7 - Message error rate vs. interferer power for message power = - 55 dBm.

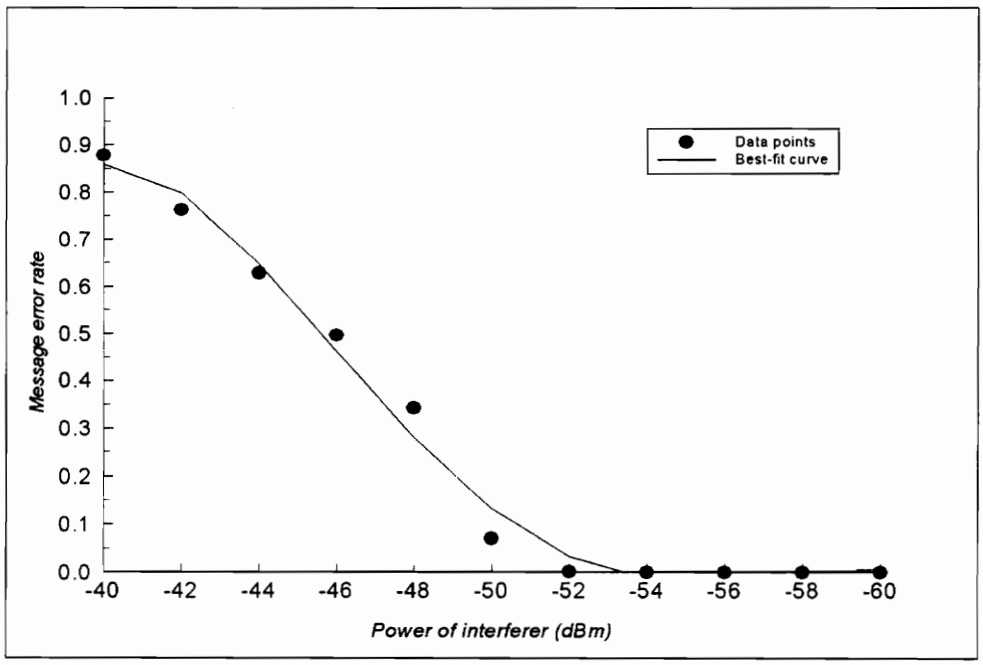

Figure 5.8 - Message error rate vs. interferer power for message power = - 60 dBm.

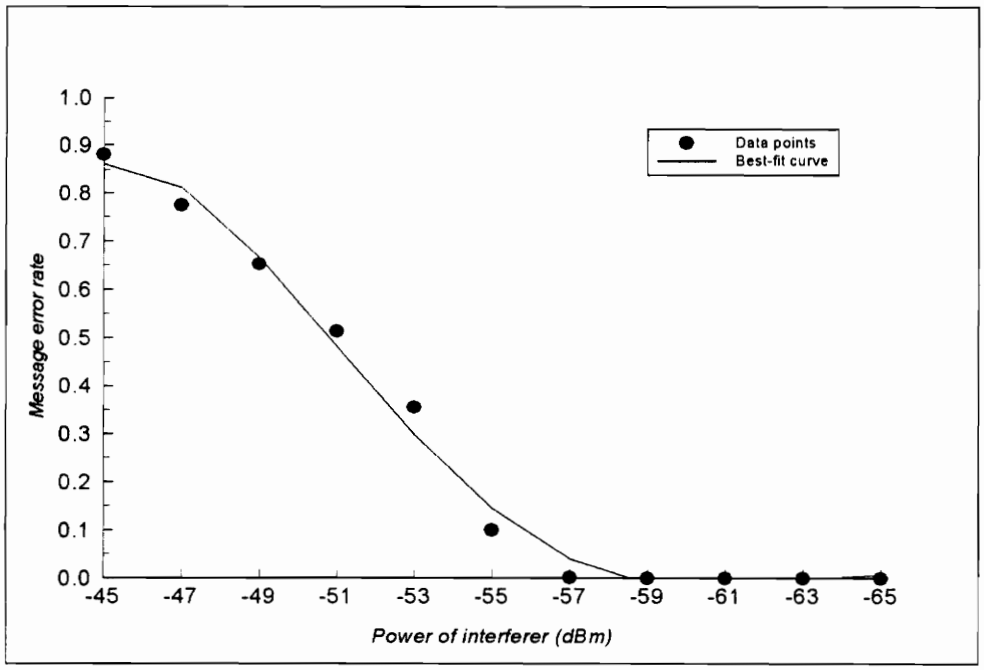

Figure 5.9 - Message error rate vs. interferer power for message power = - 65 dBm.

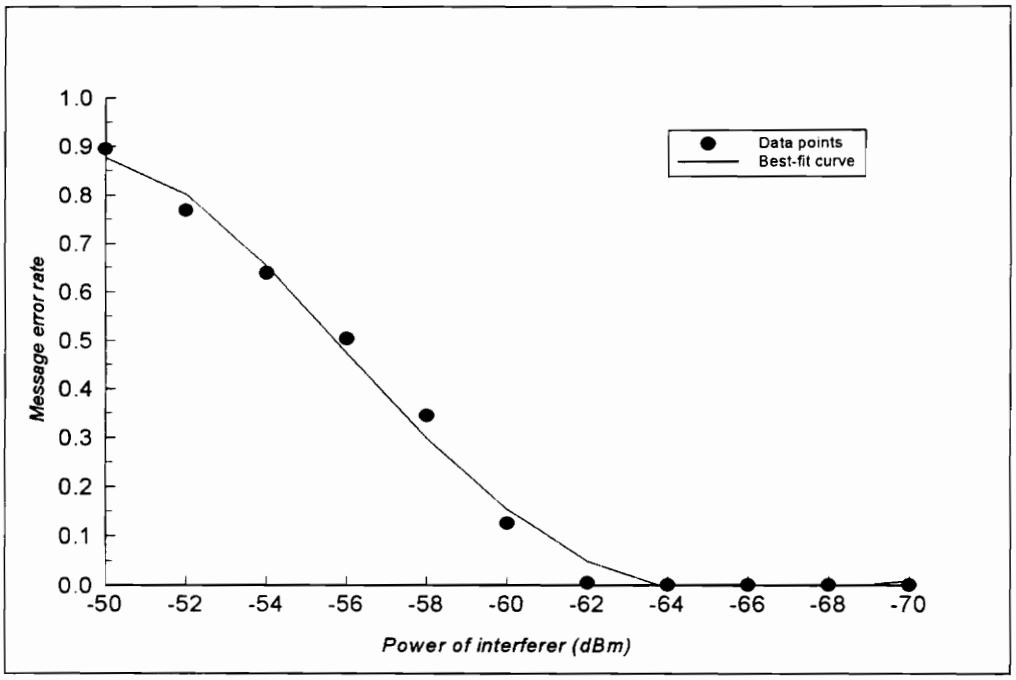

Figure 5.10 - Message error rate vs. interferer power for message power = - 70 dBm.

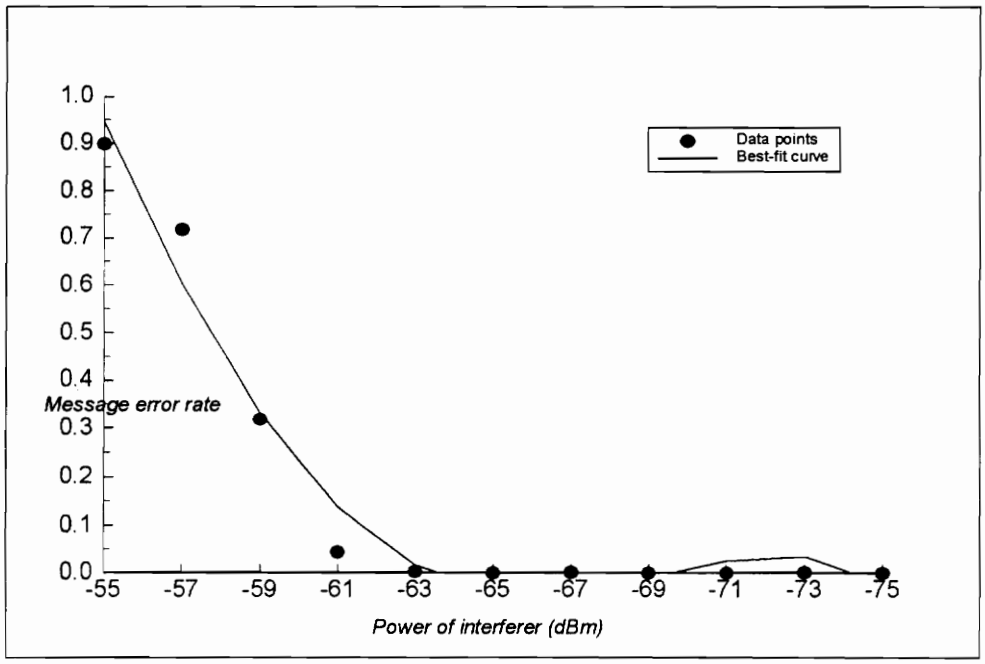

Figure 5.11- Message error rate vs. interferer power for message power = - 75 dBm.

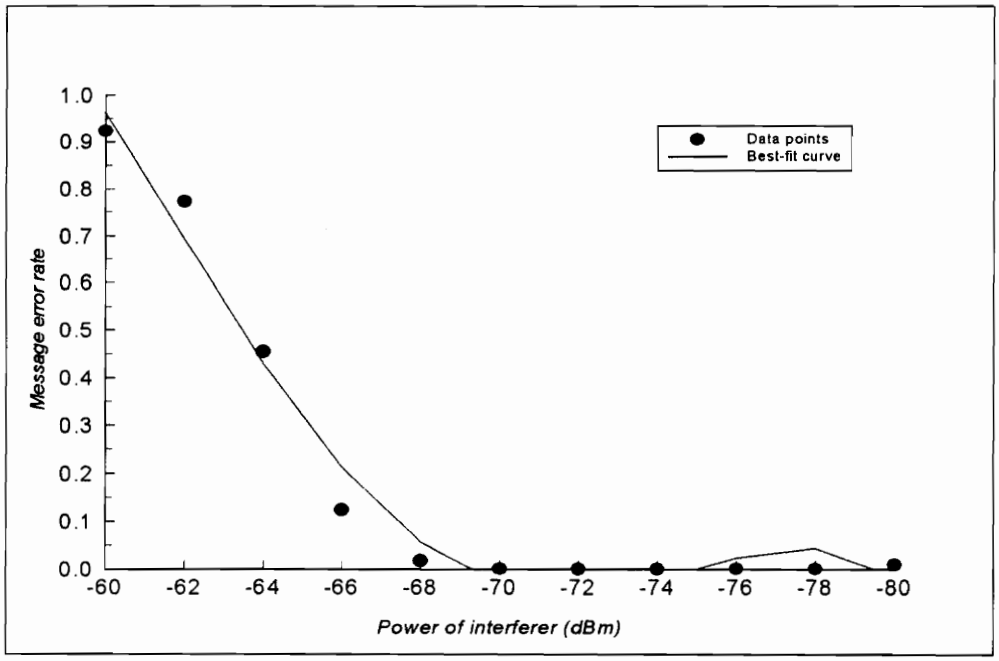

Figure 5.12 - Message error rate vs. interferer power for message power = - 80 dBm.

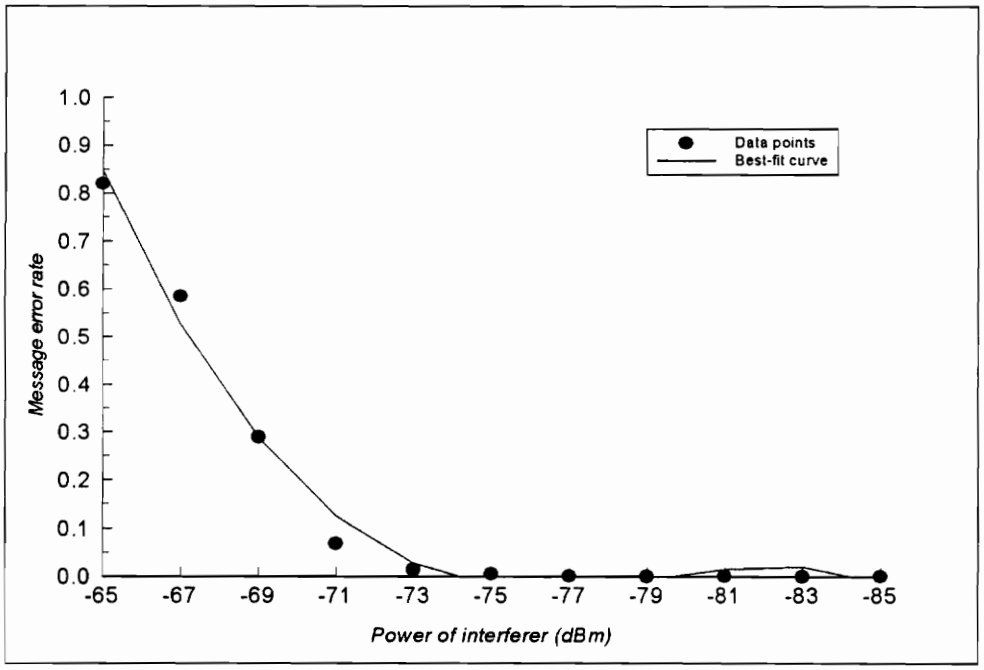

Figure 5.13 - Message error rate vs. interferer power for message power = - 85 dBm.

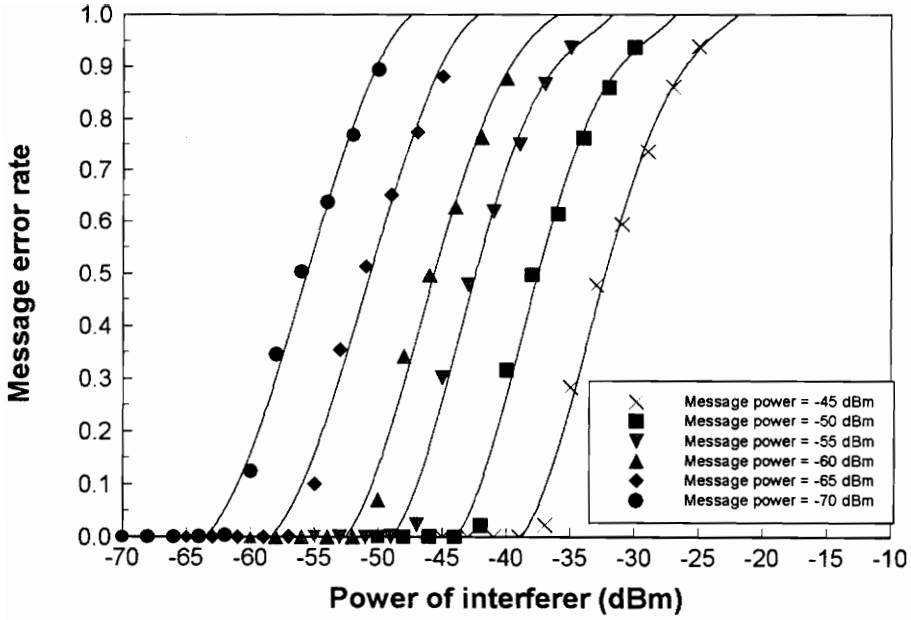

Figure 5.14 Loral Curves (-45 dBm to -70 dBm)

6.0 PHASE II TESTING-GRAYSON EQUIPMENT

This chapter describes the second phase of testing in detail. The first section explains the equipment set up, which involved additional hardware and assembly programming for control. The following sections give some examples of the messages generated for the test. Both of these sections are relevant to the validity of the test since the testing is attempting to replicate IVDS collisions. Error rate data will be used in Chapter 7 to compare the performance of the two types of receivers.

6.1 Phase II Set Up

The second phase of testing was designed to mirror the first phase as much as possible. The goal of the second phase of collision testing was to study the Grayson prototype receiver's performance in the presence of colliding packets. The test is done by transmitting an initial 2-3 bits of data from the master transmitter and then engaging the slave transmitter to act as jammer. The Grayson prototype receiver can achieve PN lock within the first bit or two of information from the master transmitter. The point of interest for the test is the regime where the jamming signal begins to affect greatly the arrival message error rate or bit error rate.

Like the first phase, two DSP microprocessors are used to implement the message transmission strategy. The same ADSP-2181's that are used to set the frequency synthesizer and modulate data messages are also wired together to form a master-slave relationship. This relationship allows the master transmitter to synchronize with the slave transmitter by enabling it prior to transmitting its own message. The slave waits in a loop to receive an interrupt signal from the master. After receiving the interrupt signal, the slave transmitter delays a predetermined time before transmitting its own message. This time delay is about 10-20 microseconds. After the master transmitter finishes transmitting a single data packet, it waits in loop approximately 100 ms and repeats the same message. Since the master always enables the slave, it controls exactly when the message collision

will occur. The messages of the two transmitters are entirely different so that a "switch-over" point from the desired signal to the jammer signal may be determined. Each message is 184 bits or 23 bytes long. The modulated serial bit rate from the ADSP-2181 into the MAXIM transmitter chip is 2 Mbps. The output of the transmitters is at 912 MHz. The transmitter outputs are run into HP attenuators to vary the power levels of both the jammer and the desired signal. Before entering the receiver, the attenuator outputs are combined in a 3 dB coupler.

At the receiver, the packets are demodulated with the CRC turned off. The data rate used by the receiver is 40 kHz. The WMI software is slightly modified to disable the queuing is disabled, allowing messages to scroll down the screen. Before receiving any data, the receiver software setting, the matched filter coefficients, thresholds, and radio receiver setting must be downloaded. TELEMATE software is used to capture the screen data to a text file to be analyzed.

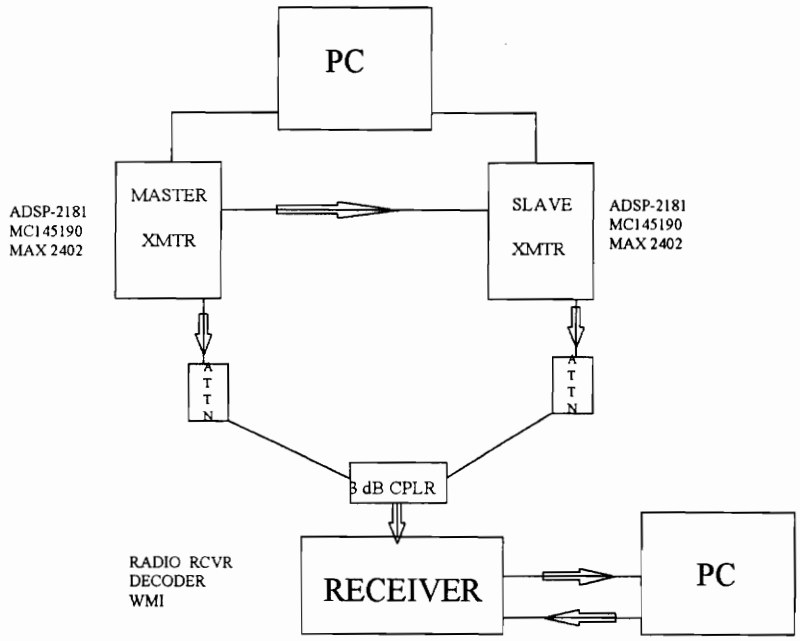

Figure 6.1 Phase II Set Up (Grayson)

Data trials were taken with desired signal powers ranging from -45 dBm to -85 dBm, in which jammer powers were varied from a 0 dB power difference to a 14 dB power difference. Each trial was repeated five times.

6.2 Test Messages

The following is a sample of a test message received in the Phase II testing with no errors.

AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST

Four *A* 's were used to ensure the message is correctly received initially by the receiver. The letters of the alphabet were used for easy identification of bit errors. The message byte length was chosen such that the **message duration (length)** was **4 ms**, as in Phase I, and for the IVDS channel. Compare this file to a test message with multiple errors.

AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMN/□ò"ð
AAAABCDEFGHIRI@MJX X1°
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHI*□
AAAABCDEFGHIJJLPP□``RuX
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHIJKLMNOPQRST
AAAABCDEFGHI¸{LMBHXX¸h□

Like KERMIT, TELEMATE log files convert all binary data into its ASCII equivalent. A small square indicates cases where an unprintable character appeared.

The second transmitter, the jammer, had a different message of four A' s followed by all X' s.

6.3 Output Files

Output files were generated using a program similar to the C program used for the Phase I testing. This version analyzed the Grayson data and output bit error and message error information. For each received test file, an output file was generated. Figure 6.2 is an example of a typical output file.

Message error distribution
total # of messages with 1 byte error : 62
total # of messages with 2 byte errors : 50
total # of messages with 3 byte errors : 44
total # of messages with 4 byte errors : 61
total # of messages with 5 byte errors : 46
total # of messages with 6 byte errors : 56
total # of messages with 7 byte errors : 61
total # of messages with 8 byte errors : 72
total # of messages with 9 byte errors : 71
total # of messages with 10 byte errors: 60
total # of messages with 11 byte errors: 45
total # of messages with 12 byte errors: 17
total # of messages with 13 byte errors: 6
total # of messages with 14 byte errors: 0
total # of messages with 15 byte errors: 0
total # of messages with 16 byte errors: 0
total # of messages with 17 byte errors: 0
total # of messages with 18 byte errors: 0
total # of messages with 19 byte errors: 0
total # of messages with 20 byte errors: 0
total # of messages with 21 byte errors: 0
total # of messages with 22 byte errors: 0
total # of messages with 23 byte errors: 0

Byte error distribution
total # of bytes with 1 bit error : 788
total # of bytes with 2 bit errors : 1056
total # of bytes with 3 bit errors : 889
total # of bytes with 4 bit errors : 736
total # of bytes with 5 bit errors : 360
total # of bytes with 6 bit errors : 106
total # of bytes with 7 bit errors : 26
total # of bytes with 8 bit errors : 162

********** TOTALS **********

total # of messages	: 916
total # of wrong messages	: 651
message error rate	: 0.71070
total # of wrong bytes	: 4123
total # of wrong bits	: 12425
bit error rate	: 0.07372

Figure 6.2 Sample Output File

6.4 Message Error Rate Data

The Mean Message Error Rate was calculated for each receiver power. The following figures represent the MER data found in Phase II Testing. Each graph plots the MER versus the power of the interference signal over a 14 dB scale X-axis. Analysis of the data collected will be provided in the following chapter.

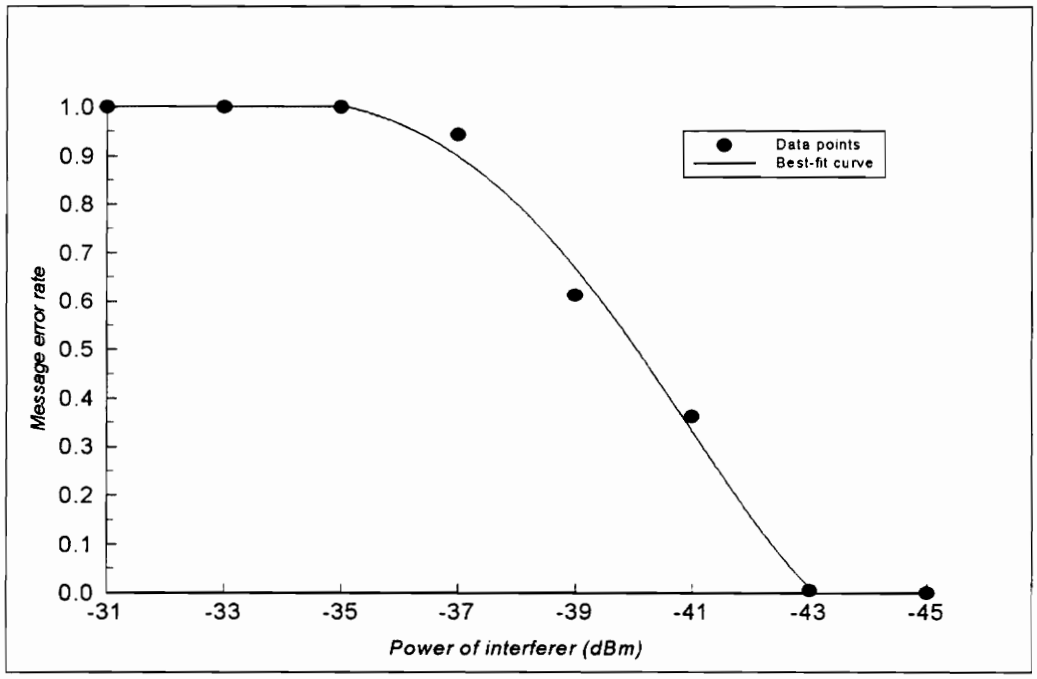

Figure 6.3 - Message error rate vs. interferer power for message power = - 45 dBm.

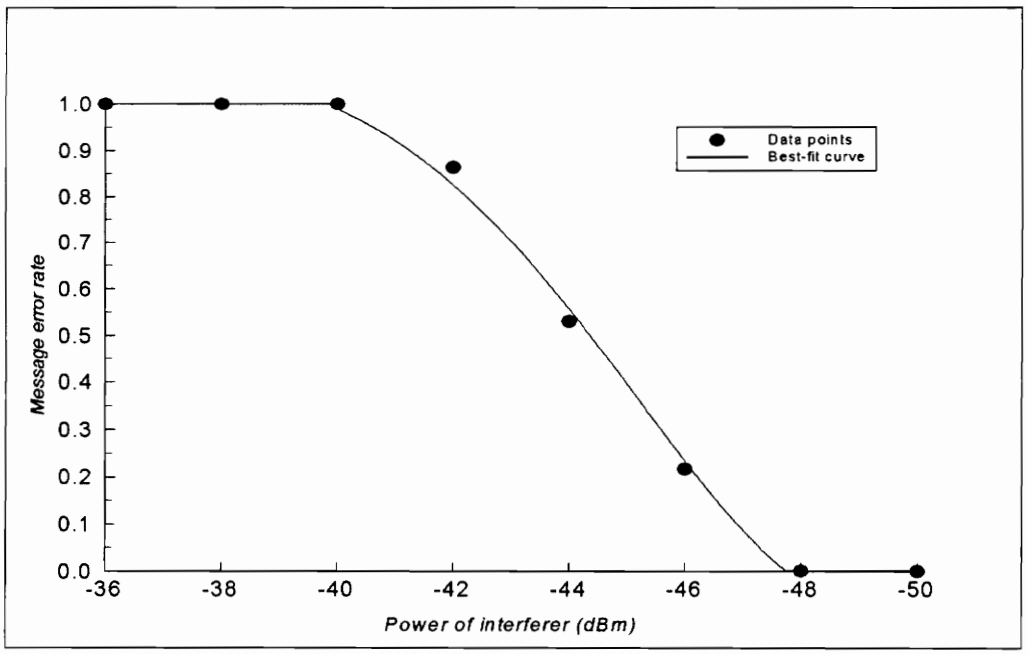

Figure 6.4 - Message error rate vs. interferer power for message power = - 50 dBm.

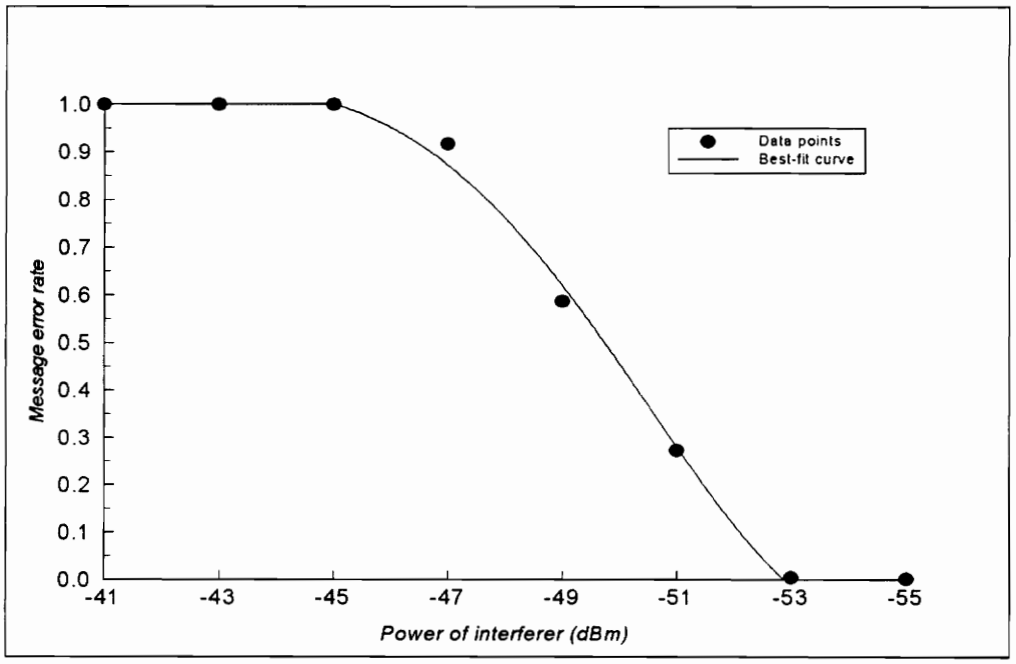

Figure 6.5 - Message error rate vs. interferer power for message power = - 55 dBm.

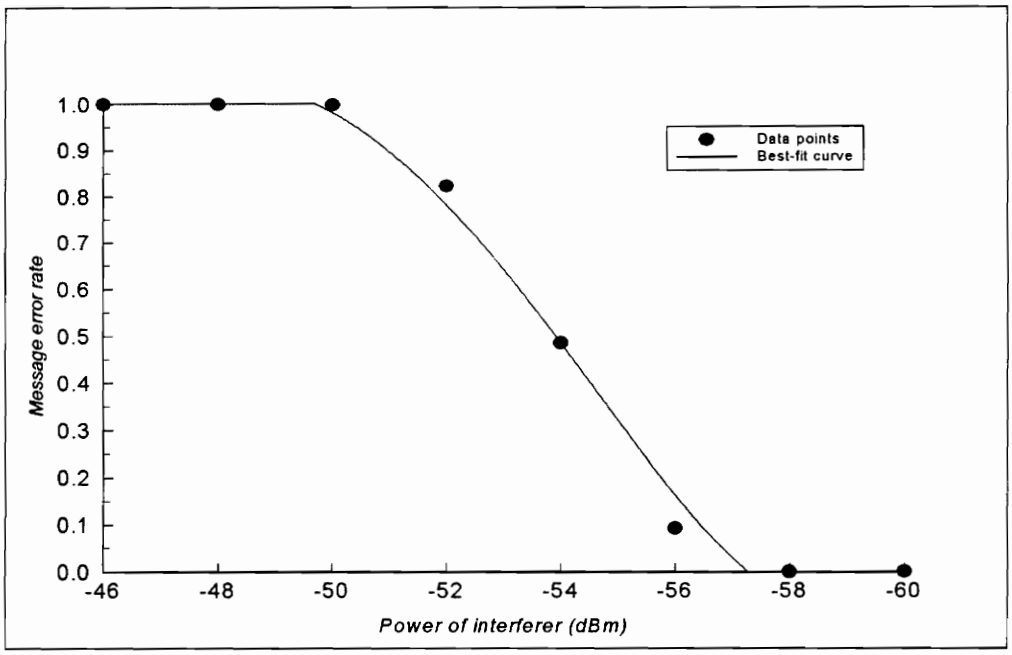

Figure 6.6 - Message error rate vs. interferer power for message power = - 60 dBm.

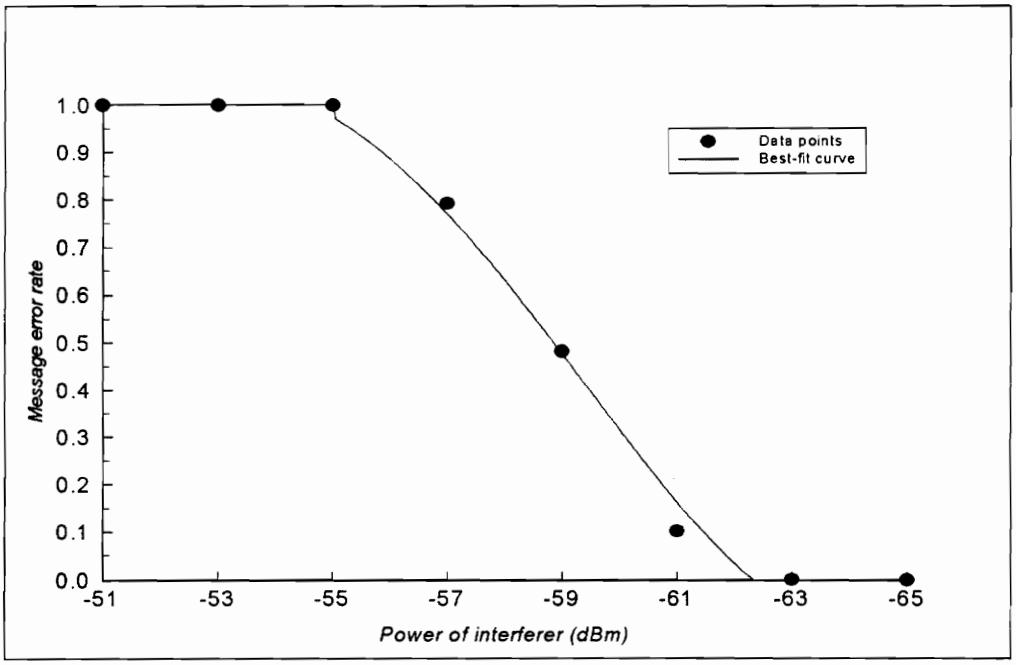

Figure 6.7 - Message error rate vs. interferer power for message power = - 65 dBm.

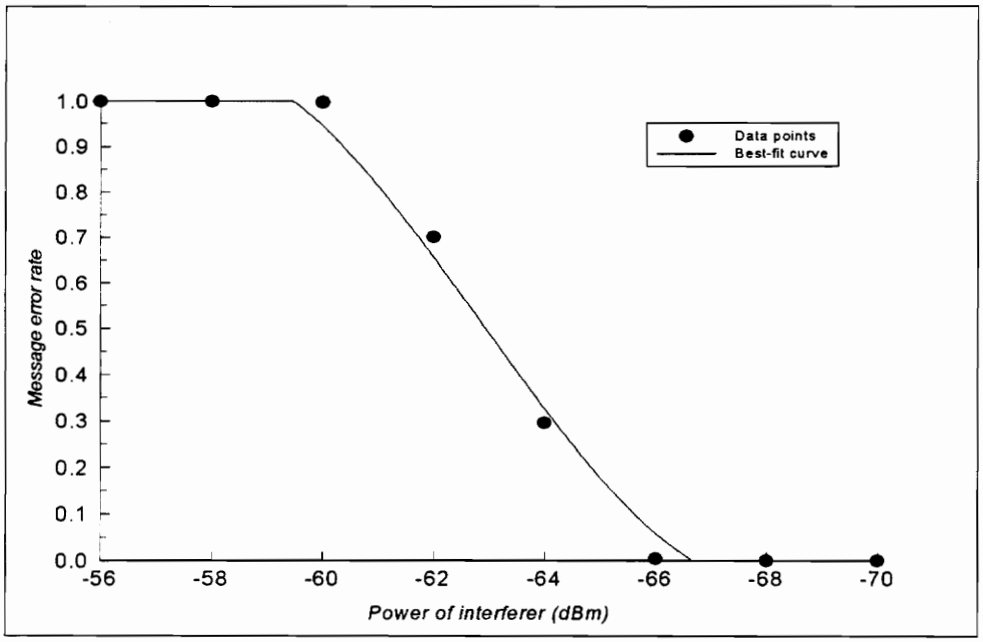

Figure 6.8 - Message error rate vs. interferer power for message power = - 70 dBm.

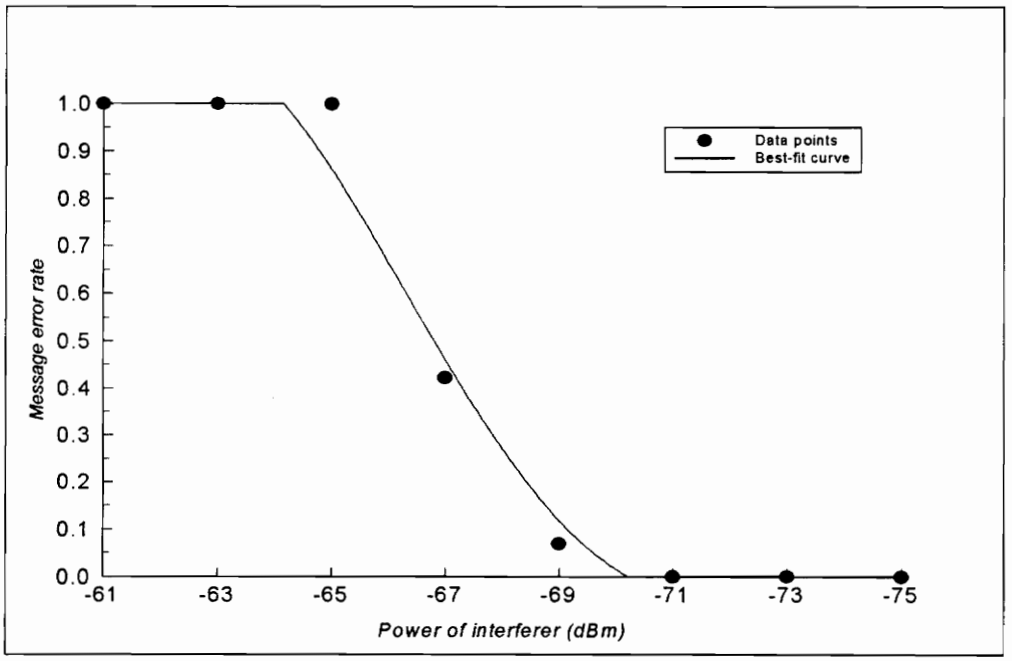

Figure 6.9 - Message error rate vs. interferer power for message power = - 75 dBm.

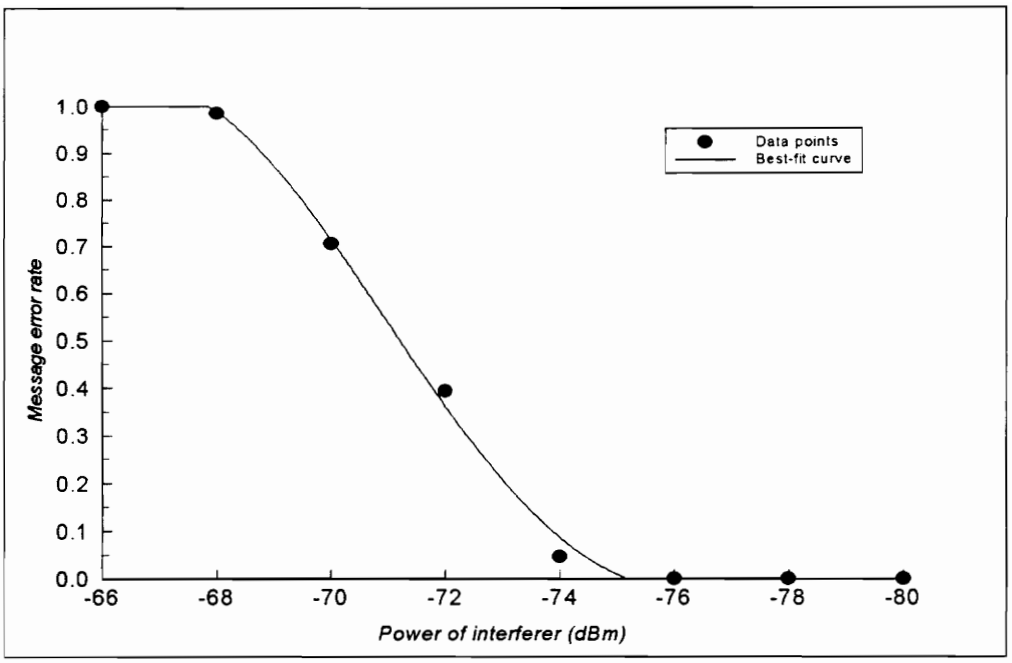

Figure 6.10 - Message error rate vs. interferer power for message power = - 80 dBm.

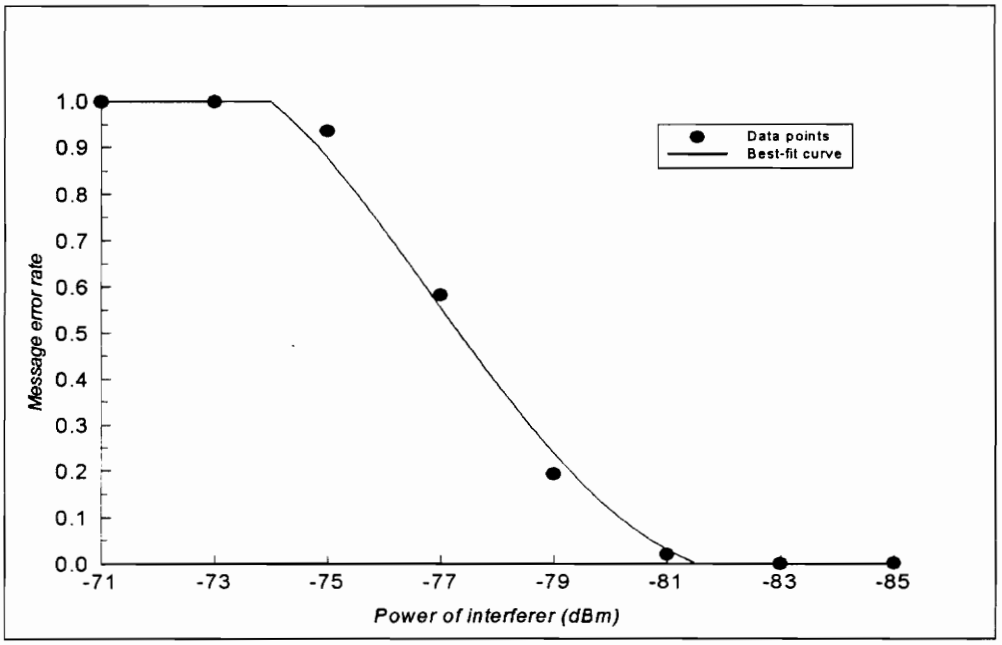

Figure 6.11 - Message error rate vs. interferer power for message power = - 85 dBm.

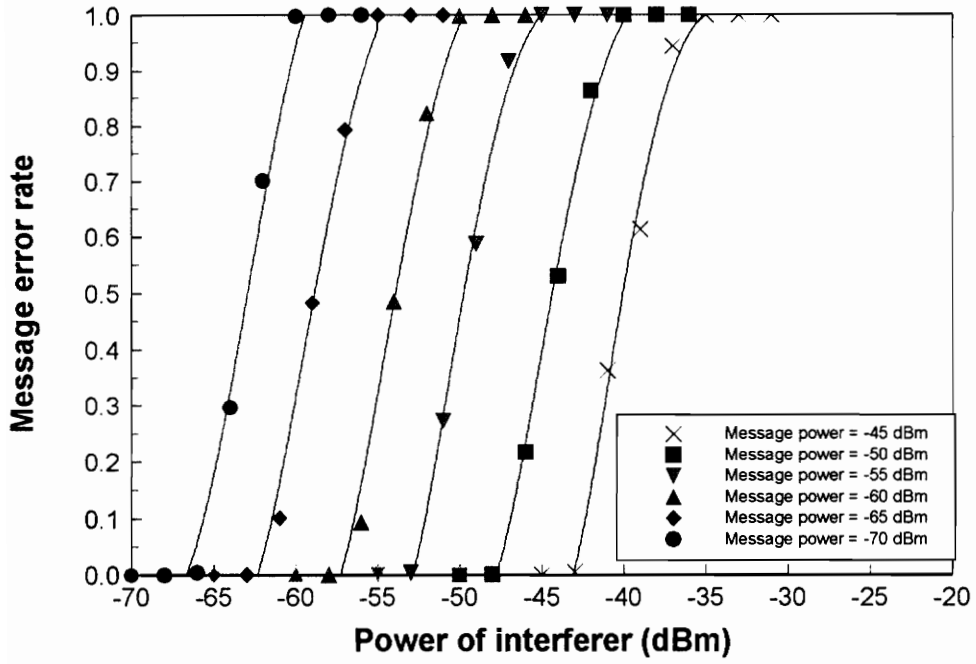

Figure 6.12 Grayson Curves (-45 dBm to -70 dBm)

7.0 DATA ANALYSIS

This chapter will discuss the results of the collision tests and analyze the jamming margin data. It will also compare the two receiver types' interference rejection properties.

7.1 PHASE I ANALYSIS-LORAL DATA

In Chapter 5, a series of curves was produced to evaluate the interference rejection capability of the Loral Spread Spectrum Receiver. The plots display the message error rates calculated from the 500 data trials run in Phase I of the collision study. This section will discuss the results in terms of jamming margins and identify packet error cases found in the test messages.

7.1.1 Jamming Margin and Interference Rejection (LORAL)

With the exception of Figure 5.7 (desired signal power of -75 dBm) the Loral EB-100 receiver operated with a jamming margin between **8-12 dB**. This is found through interpolation of the Chapter 5 plots. The jamming margin was found to be slightly dependent on incoming power levels. This is evident in the last few trials with message powers of -75 to -85 dBm, where the jamming margin seemed about 2-3 dB better than in the trials of -45 to -70 dBm. Figure 7.1 illustrates the concept of the jamming margin and what happens as the jammer power increases.

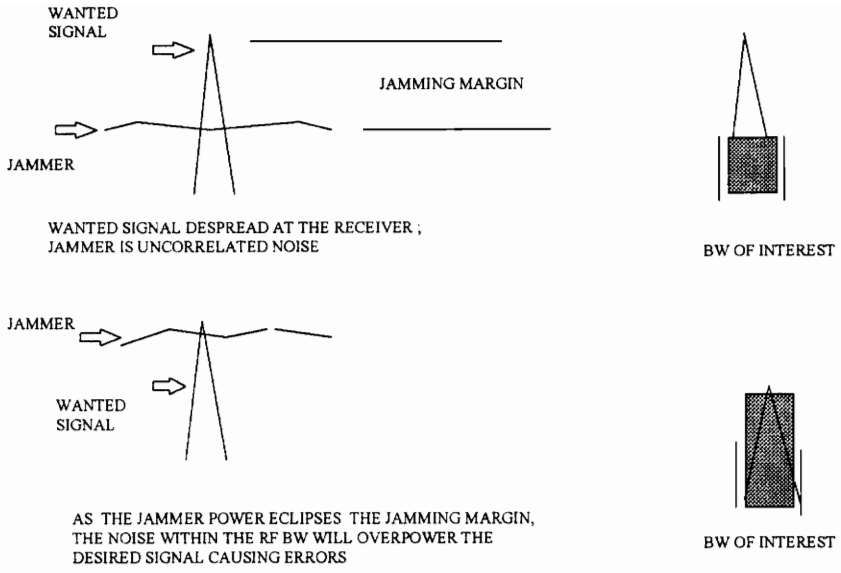

Figure 7.1 Jamming Margin

In Figure 7.1, the jammer is seen as uncorrelated noise. Even though the jammer itself uses the same spreading code as the wanted signal, it will be seen as this uncorrelated noise since the receiver locks on to the wanted signal first.

Although the jamming margin for the Loral EB-100 was found to be around 8-10 dB, **outage** was never reached, meaning no trial experienced a message error rate of 1.0. This result is very interesting. Even though the jammer power greatly exceeds the jamming margin, in some cases up to 12 dB, some packets still arrive uncorrupted. This is an interference rejection characteristic specific to sliding correlator receivers. The Loral EB-100 employs a Phase/Frequency Detector (PFD) and Phase Loop Filter (PLF, discussed in Chapter 4) for carrier recovery. The PFD detects the incoming phase and frequency of the incoming signal. The PFD passes its binary output into the PLF. The PLF converts the phase data to a control word for the Digital Phase Shifter (DPS). This control word allows the DPS to track the incoming signal's phase. Figure 7.2 illustrates the carrier recovery loop.

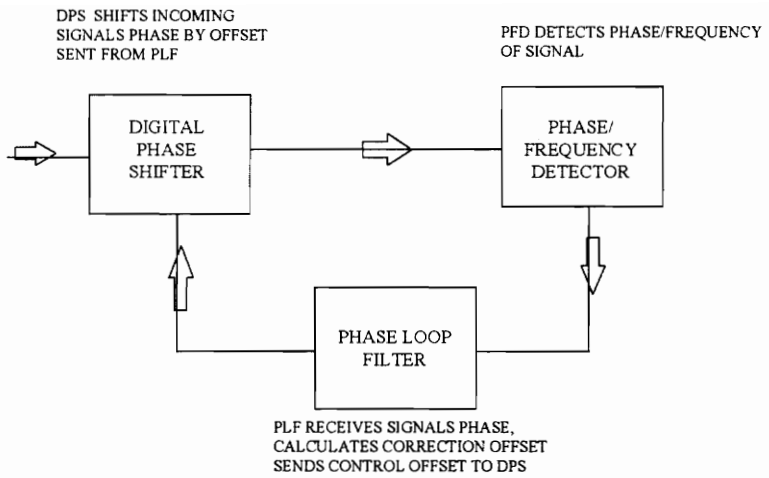

Figure 7.2 Loral Carrier Recovery Loop

The coherent detection process provides additional interference rejection. The carrier recovery loop has the ability to track the incoming signal's phase, thus allowing for packet reception even in cases of excessive jammer power. This may not have occurred had the message duration been greater than 4 ms. Since phase and PN lock are a stochastic process, the shorter the message duration the greater the chance for packet survival in a collision. Figure 7.3, taken from [1] helps to illustrate how carrier recovery helps in demodulating and tracking the incoming code sequence.

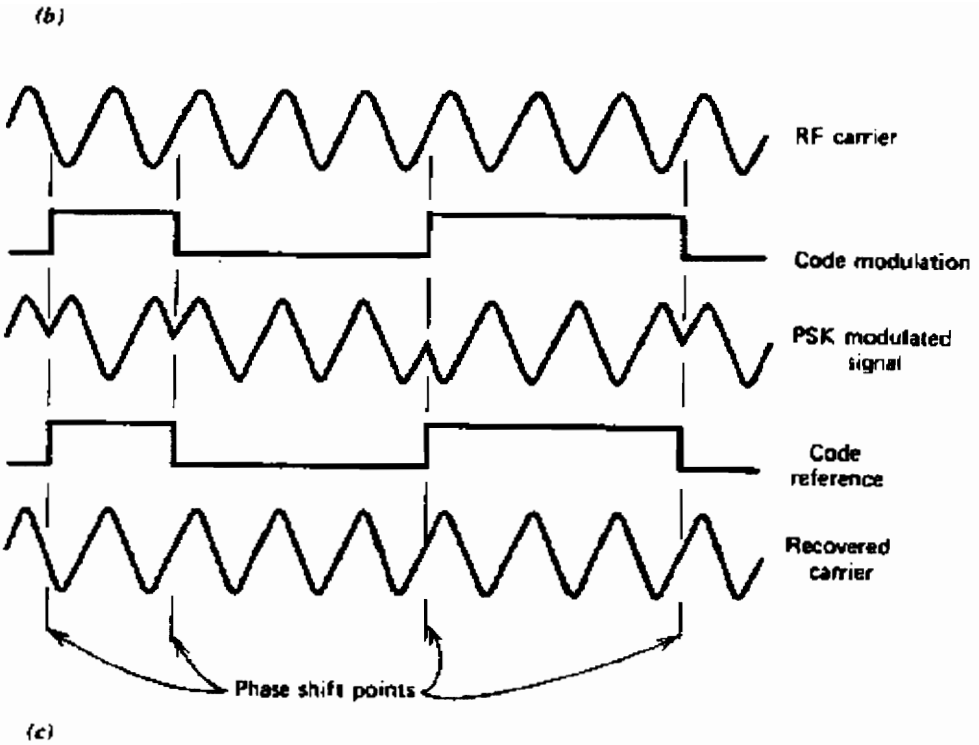

Figure 5.1 In line correlator carrier recovery: (*a*) modulating multiplier (PSK modulation); (*b*) in-line correlator (complementary PSK modulator); (*c*) waveforms in PSK (biphase) carrier recovery.

Figure 7.3 Demodulation using Carrier Reference (Figure 5.1 from [1])

7.1.2 Packet Error Cases

This section describes the three types of message errors encountered in Phase I testing. The three cases found in the testing were the bit error, the multiple byte error, and the loss of synchronization error.

7.1.2.1 Case 1-Bit Error

The bit error is the most simple type of packet error. Single bit errors begin to occur in small numbers on the threshold of the jamming margin. A single-bit error

example would be the receiver seeing ahtxt, instead of ahtst. The ASCII equivalent of the *x* is 1 bit different from that of the *s*.

In a few cases, these one or two single bit errors show up even in very low power differences between the jammer and desired signals. For example, one trial in five at 0 dB difference will usually contain a single-bit error. This is more than likely due to system noise, not the jammer, since each trial passes 1000 packets and each packet is 23 bytes long.

Multiple single bit error packets indicate that the jammer eclipses the jamming margin. As jamming powers rise above the jamming margin, receiver performance begins to degrade. Recalling equation [8] in Chapter 3, as the jammer power increases, the output signal-to-noise ratio suffers. At some point in the testing, the S/N falls below the minimum S/N. This is where the multiple single bit errors begin to appear.

7.1.2.2 Case 2-Multiple Byte Error

While multiple single (or even double and triple bit errors) may indicate that the jammer power level meets or slightly exceeds the jamming margin, multiple byte errors indicate that the receiver is now demodulating a combination of both the jammer and desired signals. An example of such an error would be receiving axlx], instead of ahtst. While the receiver remains in both PN and phase lock, the jammer power begins to affect the desired messages.

The jammer power becomes a problem to both the sliding correlator and the phase lock carrier recovery loop. At lower signal-to-interference levels, the PN code of the desired signal is detected and signals the phase recovery loop to lock on to the incoming phase of the desired signal. The Phase Locked Loop (PLL) is capable of tracking the desired signal's phase and frequency. However, as jammer-to-signal ratio increases, the phase noise introduced into the PLL becomes greater. Phase noise causes some bit errors. Also, at the same time, jammer noise in the correlator causes false threshold detections, again causing bit errors.

7.1.2.3 Case 3-Loss of Synchronization

Loss of synchronization errors occur when the jammer is well above the jamming threshold. An example of a loss of synchronization error would be receiving ah , instead of ahtst.

At some power level above the jamming margin, the jamming phase noise overpowers the PLL and forces the system out of lock. Although the receiver never actually switches over and captures the jammer, the jammer forces the receiver out of lock. Had the signal-to-interference levels in this test gone beyond 24-26 dB, the receiver would have experienced an outage, where no packets arrive uncorrupted. However, since the lock time required for the sliding correlator is just less than the length of the actual message, the data presents no valid evidence of the capture effect.

7.2 PHASE II ANALYSIS-GRAYSON DATA

In Chapter 6, a series of curves was produced to evaluate the interference rejection capability of the IVDS Grayson Receiver. The plots display the message error rates calculated from the data trials run in Phase II of the collision study. This section will discuss the results in terms of jamming margins and identify packet error cases found in the test messages.

7.2.1 Jamming Margin and Interference Rejection (GRAYSON)

From interpolating the Chapter 6 plots, the jamming margin for the Grayson Receiver is between **2-5 dB**. As in Phase I, the jamming margin is slightly dependent on message power levels, since the -75 to -85 dBm message power trials have 1-2 dB greater jamming margin than the trials at lower powers.

The Grayson Receiver employs a matched filter to synchronize with the incoming packet's PN code. This is a noncoherent or asynchronous type of detection. Since both the jammer and the desired signal have the same spreading code, the receiver will despread

the jammer at power levels where it exceeds the jamming margin as well as the minimum S/N. This is where the receiver experiences something similar to the capture effect. Referring to equation [13] in Chapter 3, the probability of receiving jammer signal over the desired signal depends on b, or the ratio of the two signal powers. If the receiver loses synchronization with the desired signal, it will attempt to regain synchronization. If the jammer-to-signal ratio is greater than capture ratio, the receiver will begin to synchronize with the jammer signal. In the Phase II tests, the primary transmitter sends 6 data bytes of its packet before the jammer packet is sent. In this time frame, the receiver synchronizes to the PN code of the primary transmitter. However, when the jammer collides with powers above the jamming margin, the addition power tends first to cause false detects at the correlator threshold detector and second, at greater power levels, the jammer is received and the desired signal becomes the interference.

As seen in the Chapter 6 plots, the matched filter receiver does not offer great interference rejection. In all cases, outage was reached within a few attenuation steps of the jamming margin (the slope of the curves were rather steep). The plots show a very sharp decline in receiver performance once the jamming margin is eclipsed.

7.2.2 Packet Error Cases

This section describes the three types of message errors encountered in Phase II testing. The three cases found in the testing were the bit error, switchovers, and the loss of synchronization errors.

7.2.2.1 Bit Errors / Multiple Byte Errors

As in Phase I, the bit errors begin to appear in tests where the jammer power has eclipsed the jamming margin. Unlike the Phase I bit errors, these tend to be multiple bit errors, not singe bit errors. These errors actually resemble the multiple byte errors found in Phase I. When a byte is received incorrectly, the bytes which follow are usually

corrupted as well. Thus, if the receiver experiences a byte or bit error in byte 17, bytes 18-23 tend to be corrupted as well. Below is a sample error of this type.

AAAABCDEFGHIJKLM@}jA:0Z

7.2.2.2 Switchovers

The switchover error looks almost identical to the previous type of error. However, these errors are evidence that the receiver has captured the second transmitter's message. In these errors, the jammer's message is received while the desired signal becomes the inteferer, hence, a switchover occurs. Below is a sample switchover error.

AAAABCDEFGHIJKLM@XXX:0Z

While only one X may be interpreted as a byte error, consecutive X 's clearly indicate the jammer has captured the receiver. The jammer packet collides with the desired packet between bytes 6 and 7. Most switchovers occurred after byte 16.

7.2.2.3 Loss of Synchronization Errors

The Phase I & II loss of synchronization errors are almost identical. When the jammer power exceeds well beyond the jamming margin, the receiver loses synchronization. A sample error is given below.

AAAABCDEFGHI

7.3 COMPARISON OF PHASES I & II

This section will discuss the receiver differences and their interference rejection capabilities.

7.3.1 Receiver Differences

Before comparing the two receivers' interference rejection capabilities, it is important to discuss the differences between the two receivers. The two most important differences between the two receivers are the process gain and the required lock times. The Loral EB-100 system operates with a process gain of 29.2 dB (10 log [8 Mhz /

9600]). The Grayson system operates with a process gain of 20 dB (10 log [4 Mhz / 40 KHz]). By inspection of the equations provided in Chapter 3, jamming margin is directly related to process gain. Thus, it is expected that the Loral EB-100 has the larger jamming margin.

The second major difference between the two receivers is their required lock times. The Loral EB-100, which uses the sliding correlator, requires a lock time equal to if not greater than the actual message length. In Phase I testing, the jammer's spread carrier was turned on and off, but the spread carrier of the transmitter of interest remained on throughout the test. While the message length was only 4-5 ms, the receiver would often take 3-5 ms to lock up. Therefore, if the Loral system was used to implement the IVDS system, the **message duration (length) would double** to ensure that the receiver locks on to the signal. For Phase I and II testing, the Loral and Grayson test messages were of equal duration(4 ms).

The Grayson system, employing the matched filter design, requires almost no lock time and can synchronize on the first incoming data bit.

7.3.2 Interference Rejection

From the jamming margin sections in this chapter, it is apparent that the Loral EB-100 receiver has a greater jamming margin than the Grayson prototype. In addition, the Loral EB-100 Receiver also proved to have better interference rejection capabilities when the jammer power exceeded the jamming margin.

Comparing the two sets of curves, the Phase II curves tend to have larger slopes, and in all cases the message error rate at the higher jammer powers was 1.0. The Phase I curves seemed to get close to the outage condition, but in no case was the MER ever 1.0. Even if the Grayson curves are shifted 9 dB, to make up for the process gain difference, the receiver still experiences outage at power levels where the Loral receiver does not. However, by shifting the Phase II curves by the process gain difference, the two systems have roughly the same jamming margin-within a few dB. Referring to equation [7] in

Chapter 3, the jamming margin is also dependent on system losses and output S/N, which may differ for each receiver by a few dB. Figure 7.4 shows how the two receivers' jamming margins compared at each power level.

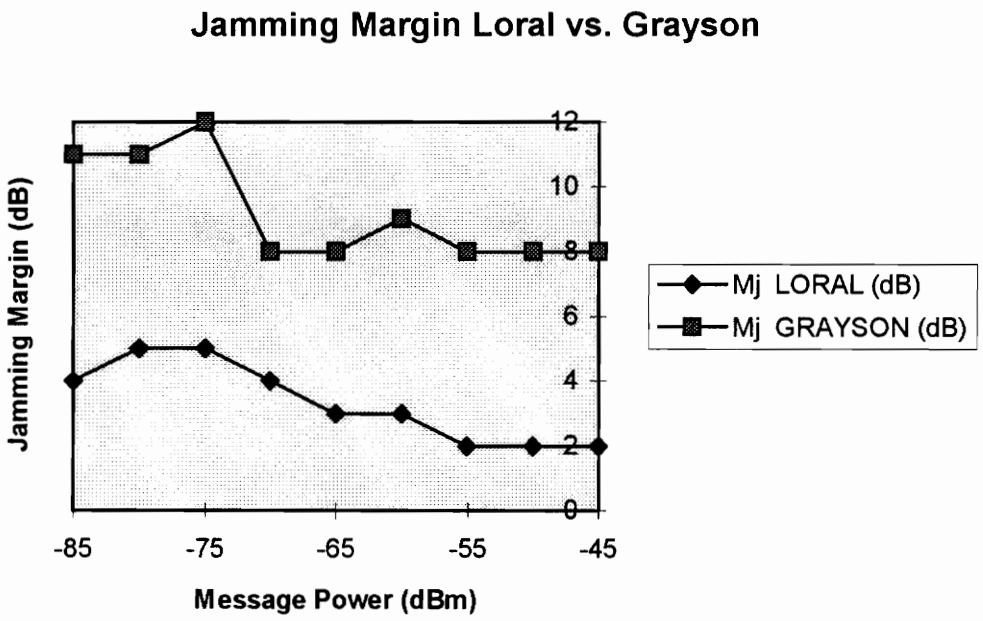

Figure 7.4 Jamming Margin Comparison

In comparing the types of errors found in the two data sets, all Phase II type errors tended to be catastrophic. All Phase II errors were multiple byte errors, since both switchover errors and loss of synchronization errors are also multiple byte errors. Although the IVDS system currently has no error correction capabilities, many of the Phase I single bit errors could be corrected with some additional coding.

Table 7.1 best illustrates the differences in the two receivers.

Table 7.1 Comparison of Receivers

	Loral EB-100	Grayson Prototype
Detection	**coherent**	**non-coherent**
Correlator Type	**sliding**	**matched filter**
Sensitivity(dBm)	**-20 to -90**	**-20 to -110**
Frequency (MHz)	**70**	**902-928**
Lock Time	**up to 4 ms**	**instantaneous**
RF Bandwidth	**8 MHz**	**4 MHz**
Information Rate	**9600 bps**	**40 Kbps**
Process Gain(dB)	**29.2**	**20**
Jamming Margin(dB)	**8-12**	**2-5**
Outage (dB)	**>20**	**6-8**

7.4 VALIDITY OF DATA

Looking at the set of curves generated in Phase I&II, the lower message power (-80 dBm, -85 dBm) graphs seem quite different from the plots at greater powers. Relative power had a slight effect on the jamming margin as mentioned earlier in this chapter, but in cases such as the Phase I -75 dBm message power plot, the jamming margin was as high as 12 dB(see Figure 7.3). The reason for such a jump had less to do with the actual systems than with the attenuators used in the testing. The attenuators were accurate to with in 3 dB at attenuations above 70 dB. Thus, the attenuators may have been a step size off at higher attenuations. In Phase II, this problem was given more attention. A signal generator, power meter, and spectrum analyzer were used to characterize each attenuator step to ensure the attenuation was correct.

Message Error Rate Standard Deviations were calculated for each trial in both Phase I & II. Most standard deviation values were less than 6% with one exception where it was 21%.

S/J (dB)	0	-2	-4	-6	-8	-10	-12	-14	-16	-18	-20
Message											
Power (dBm)											
-45	0.00032	0.00048	0.00048	0.00048	0.00285	0.018	0.01127	0.01289	0.01233	0.01352	0.00512
-50	0.00048	0	0.00048	0.00032	0.00562	0.06881	0.05005	0.04678	0.05511	0.00874	0.0112
-55	0.00048	0.00032	0.00048	0.00032	0.00568	0.06668	0.046	0.04677	0.05322	0.02964	0.0057
-60	0	0.00032	0.00048	0	0.0004	0.00887	0.00912	0.01765	0.00905	0.00996	0.0057
-65	0.00032	0.00032	0.00032	0.00032	0.00064	0.01171	0.00971	0.01302	0.00981	0.01036	0.01771
-70	0	0.00032	0	0.00072	0.00273	0.04762	0.01903	0.01075	0.0134	0.01015	0.00944
-75	0	0.00032	0.00032	0.00048	0.00048	0.00032	0.00113	0.00783	0.01536	0.0112	0.00483
-80	0.01558	0.00121	0.00048	0	0.00032	0.00081	0.01117	0.03983	0.06008	0.04658	0.0305
-85	0.00048	0	0.00032	0	0.0004	0.00796	0.00746	0.03176	0.06874	0.0692	0.04607

Figure 7.5 Mean MER Standard Deviations for Phase I - Loral Data

Signal/Jammer Power (dB)	0	-2	-4	-6	-8	-10	-12	-14
Message Power (dBm)								
-45	0	0.00149	0.01879	0.02597	0.00649	0	0	0
-50	0	0.00128	0.01112	0.02403	0.00292	0	0	0
-55	0.00086	0.00239	0.01145	0.009	0.00954	0	0	0
-60	0.00052	0.00052	0.00862	0.01174	0.00584	0.00001	0	0
-65	0.0005	0.00078	0.0118	0.00712	0.00625	0	0	0
-70	0	0	0.00192	0.21634	0.01016	0.00098	0	0
-75	0	0.00109	0	0.03032	0.04788	0.00053	0	0
-80	0.00057	0	0.00085	0.01011	0.02464	0.00111	0.00207	0
-85	0.00109	0	0.00742	0.02866	0.02806	0.0135	0	0

Figure 7.6 Mean MER Standard Deviation for Phase II - Grayson Data

8.0 CONCLUSION

This final section discusses the overall results and conclusions of the thesis as well as mentions some possible future work ventures.

8.1 OVERALL RESULTS AND TRADE-OFFS

The thesis supports the conclusion that not only does the Loral EB-100 Receiver have better interference rejection than the Grayson prototype, but that coherent receivers, in this case, will outperform noncoherent receivers in interference rejection. Coherent detection allows the receiver an additional reference other than the PN code on which to synchronize.

Given that the Loral Receiver has the better interference rejection capability, the trade-off between message duration and the probability of collision must be studied to determine the best receiver for the IVDS channel. To justify using the Loral Receiver over the Grayson Receiver, the user capacity calculations need to be redone in the simulator program in [5] using twice the current message duration. This is necessary to meet the required lock time of the Loral Receiver. With twice the message duration, the simulator program will show that the channel can accommodate only half as many users as with original message length. Second, the Loral Receiver can handle only those collisions where the jammer is below the jamming margin, otherwise the packet may be corrupted (chance increases with power differences between the desired signal and the jammer). However, data from the Proof of Concept Test shows that power differences of 20 dB, even from the same distances, are common. Therefore, this interference rejection improvement in using the Loral equipment will be relevant in only a few collision cases.

The interference rejection capabilities of the Loral EB-100 Receiver proved to be better than the Grayson Receiver, but for IVDS, the Grayson Receiver is best suited for the channel. This conclusion is based on the following premises:

1. The Loral EB-100 Receiver requires a long lock time which, if used, would double the IVDS message duration, which in effect would cripple the channel performance shown in [5]-longer message duration limits the number of retransmissions.

2. Power levels seen in the Proof of Concept Test showed that the interference rejection improvements the Loral Receiver offers would aid in only a few collision cases--in general, the desired message will be more powerful, and therefore will be received uncorrupted, or the jammer will be more powerful and corrupt the wanted signal.

3. The multi-access strategy implemented for the IVDS channel relies on retransmissions over random intervals to ensure packet arrival; losing packets in collisions is expected.

4. The Grayson Receiver offers sufficient interference rejection such that packet data will survive a collision where the jammer power is equal to or less than the desired signal power.

8.2 FUTURE WORK

Recommended future work includes improving the channel simulator discussed earlier and used in [5] and continuing with similar testing in a wireless environment with multiple transmitters. Both the improvement of the simulator and the wireless study will contribute to developing a robust one-way channel.

8.2.1 Simulator

The original simulator program in [5] is designed to test the channel capacity given a set number of retransmissions, time intervals between retransmissions, and message arrival rates. In a message collision, the simulator discards all packet data from the colliding messages.

To improve the second generation simulator program, the probability that packet data may survive a collision should also be included. This is no simple task and becomes dependent on incoming signal power levels to the receiver. This will add a fourth degree of freedom in the simulator's calculations. Perhaps the best way to implement this new

variable would be to randomize the incoming power levels. Thus, the simulator could compare power levels of incoming packets and determine whether any packet could survive a collision. The incoming signal powers could use a Gaussian distribution with mean and variance values found from the Proof of Concept Test.

8.2.2 Wireless Channel Study with Multipath

In addition to improving the channel simulator, the channel should be tested in a wireless environment to validate the simulator and test the operation of the hardware developed for the IVDS system. By using a setup similar to the Proof of Concept Test, multiple transmitters could send messages to a common receiver to test the system's message arrival rate capacity and retransmission strategy.

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Vita

Andrew James Harmon was born in Fayetteville, NC in 1972. He grew up in numerous places to include Mineral, VA, Bamberg, Germany, and Staunton, VA. He graduated from R.E. Lee High School and came to Virginia Tech in 1990. As an undergraduate he concentrated in electronics, obtaining a B.S. in Electrical Engineering in 1994. In August of 1996, after working under Dr. Bostian and the Center for Wireless Telecommunications, he completed his Masters Degree in Electrical Engineering. Following his defense, he enters the Army as a Second Lieutenant.