# Characterization of Dopant Diffusion in Bulk and lower dimensional Silicon Structures

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Comparison of Diffusion Mechanisms in Bulk and lower dimensional MOSFET structures

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ABSTRACT

The semiconductor industry scaling has mainly been driven by Moore's law, which states that the number of transistors on a single chip should double every year and a half to two years. Beyond 2011, when the channel length of the Metal Oxide Field effect transistor (MOSFET) approaches 16 nm, the scaling of the planar MOSFET is predicted to reach its limit. Consequently, a departure from the current planar MOSFET on bulk silicon substrate is required to push the scaling limit further while maintaining electrostatic control of the gate over the channel. Alternative device structures that allow better control of the gate over the channel such as reducing short channel effects, and minimizing second order effects are currently being investigated.

Such novel device architectures such as Fully-Depleted (FD) planar Silicon On Insulator (SOI) MOSFETS, Triple gate SOI MOSFET and Gate-All-Around Nanowire (NW) MOSFET utilize Silicon on Insulator (SOI) substrates to benefit from the bulk isolation and reduce second order effects due to parasitic effects from the bulk. The doping of the source and drain regions and the redistribution of the dopants in the channel greatly impact the electrical characteristics of the fabricated device. Thus, in nano-scale and reduced dimension transistors, a tight control of doping levels and formation of pn junctions is required. Therefore, deeper understanding of the lateral component of the diffusion mechanisms and interface effects in these lower dimensional structures compared to the bulk is necessary.

This work focuses on studying the dopant diffusion mechanisms in Silicon nanomembranes (2D), nanoribbons ("1.X"D), and nanowires (1D). This study also attempts to benchmark the 1D and 2D diffusion against the well-known bulk (3D) diffusion mechanisms.

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## Chapter 1: Introduction

In this section the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) era will be discussed to understand the importance of the device, its applications, evolution, and operation. The fundamentals of this device are needed to understand second order effects that impact the electrical characteristics and drive this research topic.

### 1.1 Metal Oxide Semiconductor Field Effect Transistor

#### 1.1.1 MOSFET Basics

The N-channel MOSFET transistor is shown in Figure 1. It consists of a p-type substrate typically doped with boron, and source and drain wells which are n-type regions doped with phosphorus or arsenic atoms. The region between the source and the drain is referred to as the channel area, on which silicon dioxide ($SiO_2$) is deposited followed by a highly doped polysilicon or a metal gate. $SiO_2$ has been the desired dielectric since it is thermodynamically stable on Si. In the same manner, a P-channel MOSFET can be obtained by using an n-type substrate and doping the source and drain regions with boron to form p-type wells. In addition, the complementary metal oxide semiconductor (CMOS) is fabricated by combining both an N-MOSFET and a P-MOSFET on the same substrate. In this case the P-MOSFET is fabricated by creating N-well in the substrate in which the P-channel MOSFET is formed.

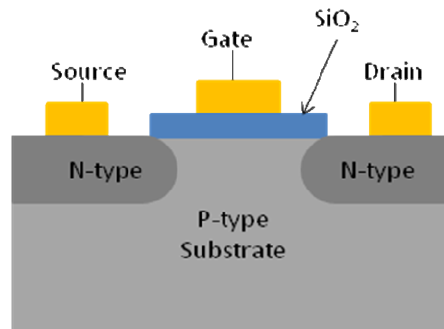


Figure 1: MOSFET structure

#### 1.1.2 Device operation

The transistor is a voltage controlled device where the gate bias voltage determines the on/off state. The device consists of three operating regions: cutoff, triode (also called linear region), and saturation regions. For an N-MOSFET when a negative gate voltage with

respective to the source ($V_{GS}$) is applied, the majority carriers (holes) accumulate underneath the gate, thus inhibiting conduction from source to drain; this region is the so-called cutoff region. As the gate bias voltage becomes positive, the holes are repelled towards the bottom of the substrate creating a depletion region underneath the gate. As the positive gate bias is increased, minority carriers (electrons) accumulate underneath the gate creating an n-type channel. The voltage that turns the channel "on" is the threshold voltage ($V_T$) at which inversion of carriers from holes to electrons occurs, enabling conduction between source and drain regions. In the triode region, the drain current increases linearly with the drain to source voltage ($V_{DS}$). However, when $V_{DS}$ is larger than the effective voltage ($V_{GS}$-$V_T$), the channel is pinched off leading to saturation of the drain current. The latter case describes the saturation regime. For the P-MOSFET, the same reasoning applies, the cutoff region occurs when $V_{GS}$ is positive and electrons are accumulated underneath the gate. In the triode region, $V_{GS}$ and $V_{DS}$ are both negative and $|V_{GS}|$ is larger than $|V_{DS}|$. In the saturation region, $|V_{GS}-V_T|$ is smaller than $|V_{DS}|$, leading to the channel being pinched-off on the drain side.

Ideally the drain current is equal to 0 in the cutoff region. Equation (1) and (2) display the mathematical relationship of the drain current.

In linear or triode region:

$$I_D = \mu C_{ox}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \tag{1}$$

In Saturation region:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \tag{2}$$

Where $I_D$ = drain current (A), μ = carrier mobility ($cm^2/Vs$), $C_{ox}$= oxide capacitance ($F/cm^2$), W= width of channel, L= length of channel, $V_{th}$= threshold voltage, $V_{GS}$ and $V_{DS}$ are gate to source and drain to source voltages respectively. The carrier mobility is a measure of the ease of the carrier motion when a voltage bias is applied. The oxide capacitance depends on the gate dielectric thickness and dielectric constant and will be discussed later.

### 1.1.3 Application

MOSFETs are the dominant electronic device used in integrated circuits (IC). More than 99% of all ICs are MOSFETs used for random access memory (RAM), flash memory, processors, and other applications. There are between 1000 and 2000 transistors in a square millimeter of a chip area [1]. Moreover, transistors are found in analog circuits for amplification purposes, in digital circuits, in flash memory, in RAMs, in non-volatile memories (NVM), in processors and many other electronic circuits. Thus, these devices are present in our daily electronics ranging from computers, cell phones, TVs, cameras, MP3, IPODS, cars, memory sticks, to medical equipments and have a great impact in society.

### 1.1.4 Moore's Law

Since its publication in 1975 by Gordon Moore, Moore's law has predicted the future of technology in semiconductor industry. The law predicts that the number of transistors on an integrated circuit (IC) will double every one year and a half to two years [2]. Semiconductor scaling is a direct consequence of Moore's law. Scaling provides the ability to shrink the devices feature sizes to increase the transistor density on a chip while obtaining performance enhancement. Moreover, device characteristics such as speed, operating voltage, power consumption, and leakage current among many more are improved. In addition, the price of circuit chips drops as a consequence of scaling. At the same time, the miniaturization of the devices allows the implementation of different circuits on the same chip area, thus increasing the circuit complexity. A plot depicting Moore's law is shown in Figure 2 where the size of a chip is shown for various product ranging from a microprocessor unit, memory cell to the flash and Dynamic RAM (DRAM). As observed the size of the chip has been decreasing over the years as a result of Moore's law. In other words, the density of transistors in a single chip has been increasing over the years.

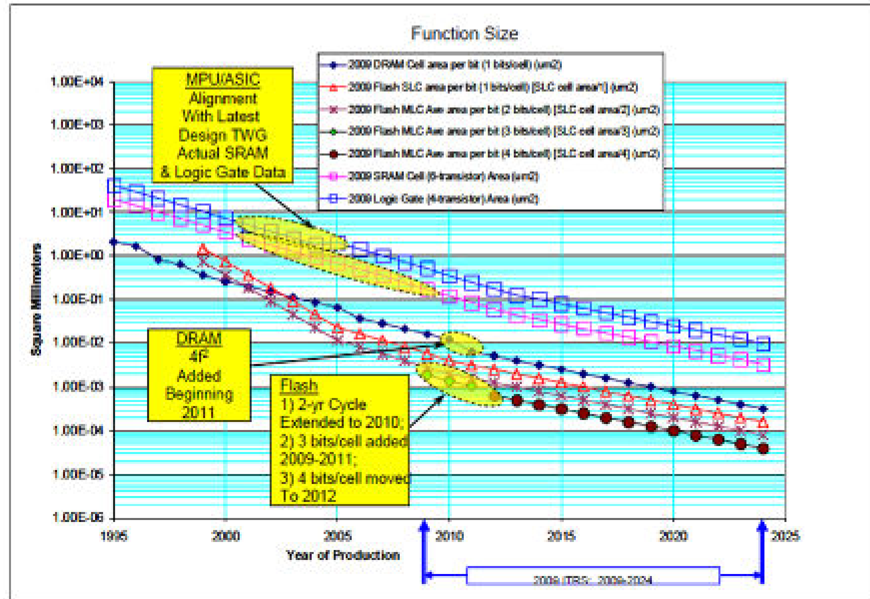



*Figure 9 2009 ITRS Product Function Size Trends:*
*MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]*

Figure 2: 2009 ITRS Product Function Size Trends [3]

### 1.1.5 Scaling

Scaling of transistors has allowed the semiconductor industry to reduce the manufacturing cost per chip while improving device performance. The transistor characteristics are improved by scaling different components of the structures such as the doping junction depth of the source of drain regions, shortening the channel length, reducing the oxide thickness and replacing $SiO_2$ with high-k dielectrics and through the choice of the metal gate. As discussed above, the $I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$ of the transistor in the cutoff, linear and saturation regions evaluate the device performance.

#### 1.1.5.1 Channel length

From equation (1) and (2), it can be seen that the drain current is inversely proportional to the channel length L. The channel length and width of the transistor are typically by a scaling factor of 0.7 each reducing the total channel area by a factor of 0.49. The electric field across the channel $V_{DS}/L$ is inversely proportional to the channel length. Thus for a shorter channel length, the channel electric field increases accordingly. As a consequence of the channel scaling, undesired second order effects, which will be discussed later, occur.

#### 1.1.5.2 Oxide Capacitance

For decades, the material of choice as the gate dielectric that enabled the scaling was silicon dioxide ($SiO_2$), the native oxide of Si which forms at room temperature from Si being exposed to the atmosphere. Moreover, $SiO_2$ was desired because of its thermodynamic stability; also high quality oxide can be grown at high temperatures. However, the scaling limit of $SiO_2$ was reached at about ~1-2 nm, thickness after which, the device properties are degraded. It has been shown using electron energy loss spectroscopy (EELS) that a thickness of ~7-8 Å is required to have the full band gap of $SiO_2$ [4,5]. Furthermore, oxide reliability is compromised for thinner film [6], which results in short device lifetime. As the oxide thickness is scaled below 2nm, key parameters that are essential for device operation such as oxide breakdown, channel mobility, gate leakage current and the reliability of the dielectric degrade significantly. The $SiO_2$ layer scaling has reached a limit where it is practically impossible to avoid high gate leakage current through quantum mechanical tunneling [7]. In addition to gate leakage current, boron penetration from the heavily doped polysilicon gate was an important issue.

Thus, the $SiO_2$ gate dielectric is replaced by a higher dielectric constant (k) material where k (dielectric) is larger than k ($SiO_2$) =3.9. It is clear that the material of choice to replace $SiO_2$ has to be compatible with CMOS process technology, thermally stable, and has to have realistic reliability. By increasing the k value, one can also increase the thickness d of the dielectric resulting in a decrease in leakage current and tunneling.

As mentioned in the previous section, increasing $C_{ox}$ improves the drain current. Equation (5) shows the relationship between the capacitance, area, dielectric constant and thickness. The capacitance C is proportional to the dielectric constant and the dielectric thickness. One way of scaling is to reduce the dielectric thickness. The smaller the thickness d, the higher the capacitance C becomes. The other is to replacing the ε with a material with higher k value.

$$C = \frac{k\varepsilon A}{d} \tag{3}$$

Where C is the capacitance, A the cross sectional area, d the dielectric thickness, k the dielectric constant and ε is the vacuum permittivity.

These High k dielectric materials can be grown thicker for the same equivalent oxide thickness (EOT). EOT is the theoretical $SiO_2$ thickness needed to achieve the same capacitance density as the dielectric. The EOT is given by the following expression.

$$EOT = \frac{k_{ox}}{k_{high-k}} t_{high-k} \Rightarrow t_{high-k} = \frac{k_{high-k}}{k_{ox}} EOT \qquad (4)$$

Where $k_{ox}$ = 3.9 for $SiO_2$, EOT= equivalent oxide thickness, $k_{high-k}$= dielectric constant of the high-k material, $t_{high-k}$= physical thickness of the high-k material needed to replace $SiO_2$.

For example, assuming an EOT of 2 nm (20Å), and a dielectric material with a k=80, a thickness $t_{high-k}$= 41 nm of the dielectric can be grown. For the same EOT, high-k dielectrics can greatly reduce leakage current and boron penetration while increasing the oxide capacitance density, hence improve the device performance. Figure 3 shows the gate leakage current and the power consumption of a high-k dielectric compared to $SiO_2$. One can clearly see a reduction of both leakage current and power consumption by three orders of magnitude when $SiO_2$ is replaced by a high-k dielectric for the same EOT of 15Å. The reduction depends more or less on dielectric constant of the high-k material.

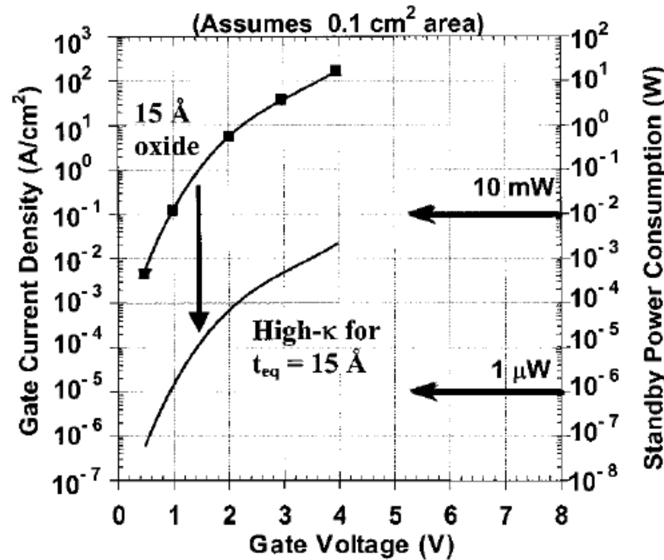



Figure 3: Comparison of gate leakage current and power consumption for 15Å $SiO_2$ and high-k for the same EOT. $T_{eq}$ = EOT= 15 Å. [6]

### 1.1.5.2.1 High-k Materials Properties

As mentioned above, high-k dielectrics can be grown thicker for the same EOT and offers a reduction in the gate leakage current and an increase in the oxide capacitance. However, to select the best suitable high-k material to replace $SiO_2$ in the 45 nm technology

node and beyond, the material electrical, mechanical, and structural properties have to be taken into account. A summary of the most studied high dielectric constant materials is given in **Table 1**

Table 1. Material properties of high-k materials [6]

| *Material* | *Dielectric Constant (k)* | *Band gap $E_G$ (eV)* | *$\Delta E_C$ (eV) to Si* | *Crystal Structure (s)* |
|---|---|---|---|---|
| SiO2 | 3.9 | 8.9 | 3.2 | Amorphous |
| $Si_3N_4$ | 7 | 5.1 | 2 | Amorphous |
| $Al_2O_3$ | 9 | 8.7 | 2.8 | Amorphous |
| $Y_2O_3$ | 15 | 5.6 | 2.3 | Cubic |
| $La_2O_3$ | 30 | 4.3 | 2.3 | Hexagonal, cubic |
| $Ta_2O_5$ | 26 | 4.5 | 1-1.5 | Orthorhombic |
| $TiO_2$ | 80 | 3.5 | 1.2 | Tetragonal, rutile |
| $HfO_2$ | 25 | 5.7 | 1.5 | Monoclinic, tetragonal, cubic |
| $ZrO_2$ | 25 | 7.8 | 1.4 | Monoclinic, tetragonal, cubic |

Hafnium-based oxides such as $HfO_2$, $HfSi_xO_y$, $HfSi_xO_yN_z$, and $HfO_xN_y$ are the leading candidates to replace $SiO_2$ [6].

**1.1.5.2.2 Metal gate**

In order to enable scaling beyond the 45nm technology node, the polysilicon gate was switched to a metal gate. The polysilicon gate was heavily doped p-type or n-type for a PMOS and a NMOS respectively. However, as a result of the down scaling of transistor, the polysilicon gate is experiencing an increase in gate dopant depletion phenomenon which degrades the drive current of the MOSFET [8]. In addition, with the subsequent anneal following implantation of the source and drain regions for dopant activation, diffusion through the oxide and into the channel increases. This phenomenon is more severe in boron doped PolySi. The large gradient of the boron concentration between the heavily doped poly-Si and the light background doping in the channel, boron atoms tend to diffuse through the thin oxide and into the channel. The boron diffusion in the channel causes an undesired drift in the threshold voltage $V_T$ of the device:

$$V_T = V_{FB} - 2\psi_B - \frac{\sqrt{4\psi_B \varepsilon_s q N_A}}{C_{ox}} \qquad (5)$$

Where $V_{FB}$ is the flatband voltage, $\psi_B = E_F - E_i$, $N_A$ is the substrate doping concentration. It can be observed from equation (5) that the threshold voltage can be shifted by the doping concentration which takes part in $\psi_B$ and the root term. Although, Polysilicon gates have been long desired since their work function can be altered by the doping type and level, these films are thermodynamically unstable on high-k dielectric. Thus, polysilicon gate is switched to metal gates from 45 nm and beyond nodes due to compatibility issues with high-k gate dielectric [9].

#### 1.1.5.3 Source and drain doping

As part of the device scaling, the source and drain (S/D) vertical and lateral dimensions must be scaled. Thus the length and width of the S/D regions are scaled accordingly as well as the junction depth of the S/D dopants. On the second hand, the S/D regions must be doped at a higher concentration to avoid an increase in the resistivity. In addition, the background doping concentration in the channel must also be increased to maintain the same source to drain isolation [10]. For a node of 18 nm channel length, the junction depth is predicted to be 6.5 nm [11].

Initially solid source diffusion was used to dope source and drain regions using solid sources such as $P_2O_5$ and $B_2O_5$. However, it was difficult to control the lateral junction, concentration profile, lateral diffusion and the uniformity across the wafer. Next, phosphorus and boron gas were used as the sources of dopants for silicon. In order, to follow the scaling technology, different doping techniques were required such as dopant ion implantation. During implantation, the charged boron and phosphorus particles bombard the Si sample. The implantation energies are varied between 1keV and 1MeV resulting in ion redistribution and different penetration range. Thus, the dopant distribution can be controlled as well as the junction depth and the doping concentration by implanting the adequate dose. The average depth is controlled by the acceleration energy and the dose is controlled by the implantation current.

A disadvantage of the implantation is that it creates damages in the crystal since Si atoms are displaced and thus point defects such as vacancies and interstitials are created. Additionally, most of the dopants are not activated during the implantation since they do not occupy a lattice site but rather an interstitial one. In order to repair the crystal damage

and activate the dopants,   an annealing step is required after the implantation. The annealing can be performed using furnace annealing; however, the temperature and time budgets are consuming. The ramp down and ramp up times are long and the furnace ambient needs to be controlled closely. Rapid thermal annealing (RTA) systems have a transient lamp heating which can rapidly ramp up to temperatures up to 1100 °C in few seconds. The annealing can be performed under atmospheric conditions or at low pressure under isothermal conditions. The typical lamps are tungsten filaments or arc lamps which allow more efficient annealing and thus shorter annealing time are needed than for a furnace case. In order to reduce diffusion length even further, Non-melt and melt laser annealing techniques are also implemented where the dopants can be activated readily without allowing dopant diffusion. In the melt laser annealing the Si is amorphized during the laser treatment and recrystallized afterwards, allowing dopants to occupy lattice sites without much diffusion. In these last techniques, the lateral and in-depth junction depths can be precisely controlled.

### 1.1.6 Second Order effects

The realistic MOSFET behavior is non-ideal and second order effects are observed specially with scaling growing that impact the device performance greatly. These second order effects correlate greatly with the source drain and channel doping profile and concentration.

The channel modulation effect is due to the drain bias voltage which causes the drain-channel junction to be in reverse bias mode. The drain bias voltage applied to operate the MOSFET creates a depletion region at the channel-drain side. Thus, the effective channel length is decreased by the drain bias voltage by ΔL, where $\Delta L = \sqrt{\frac{2\varepsilon_s}{qN_A}(V_{DS} - V_{DSsat})}$,

where $\varepsilon_s$ is the semiconductor relative permittivity (11.7 for Si), $N_A$ is the substrate doping, $V_{DS}$ is the drain voltage, and $V_{DSsat}$ is the saturation drain voltage. Since the effective channel length decreases with the $V_{DS}$, the current increases in the saturation region unlike the ideal case where the current should remain constant. The drive current becomes dependent on the drain voltage instead of the just being modulated by the gate voltage. The

channel modulation effect worsens as the channel length decreases. Additionally, the channel conductance $g_d$ is no longer equal to 0 and increases with drain voltage.
The drain induced barrier lowering (DIBL) is the barrier lowering caused by the action of the drain bias voltage. As the channel length decreases, the action of the drain bias decreases the barrier on the source side leads to a lower threshold voltage and increase of subthreshold slope. The drain field reaches through the channel and thus alters the device characteristics. As the drain voltage increases, the threshold voltage decreases and this worsens at shorter channel lengths.
Punch through is also an issue that affects the scaling. As the drain voltage increases, the depletion region increases on the channel-drain side; if this depletion region extends to the source side, punch through occurs and the gate is no longer in control of the channel.

### 1.1.7 Evolution of MOSFET

As shown in the ITRS map below in Figure 4, different device structures and materials have been implemented or are foreseen in the future to maintain and improve the transistor device characteristics. The polysilicon gate was replaced by a metal gate to suppress dopant diffusion from the gate to the channel and also because of the depletion region created within the poly gate during device operation. The high-k dielectric replaced the $SiO_2$, SiON gate insulator to allow further scaling by reducing gate leakage current, and improving reliability. In order to improve the electrostatic control of the gate over the channel, MOSFETs on SOI substrates replace the bulk substrate MOSFET. The SOI substrates improve second order effects and also provide isolation of the channel from the bulk Si. In the partially depleted SOI (PDSOI), the SOI is thick enough to allow depletion and inversion in the layer. In the Fully depleted SOI (FDSOI), the Si layer is thin enough that the entire layer is inverted; thus the SOI thickness is the channel inversion thickness. Eventually, the multiple gate FET (MGFET) and multiple channel FET (MUFET) on Si bulk and SOI substrates are considered to be the ultimate device structures which will allow further scaling of the device to increase speed, lower power consumption, reduce threshold voltage, increase drive current, reduce second order effects [12,13,14,]. These devices include the FinFET, the double and triple gate FET, and eventually the Wrap Around gate Nanowire [15], where the gate oxide and metal will be deposited around the channel using

atomic layer deposition which is so far the best proven technique to achieve such conformal deposition and good step coverage.

Current and future research will focus on channel engineering. For Si, the channel is forced under tensile or compressive stress by etching source and drain areas and filling it with a material of different lattice constant than Si for example $Si_xGe_{1-x}$ which has a larger lattice constant than Si based on the Ge content in SiGe. By applying stress in the channel, the band structure in the channel area is modified leading to a change in the curvature of the conduction and valence band which is proportional to the inverse of the carrier effective mass. Thus, by increasing the curvature of the bands, the effective mass is reduced which in turn increases the mobility of carriers in the channel. Additionally, the mobility of carriers is higher in SiGe source and drain regions. High mobility semiconductor materials are believed to be the ultimate response to higher speed devices and reducing power consumption. Materials such as Ge and III-V semiconductors have larger mobility than Si and by varying the composition and material compound; the band gap and electronic characteristics of the device can be chosen effectively.

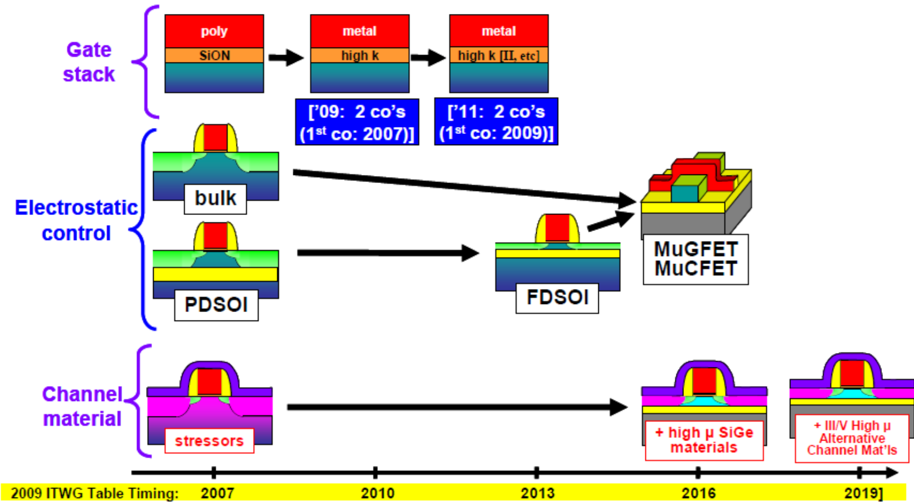



Figure 4: ITRS FET device map [16]

### 1.1.7.1 General Interest in nanostructures [17]

A general interest in nanostructures is currently rising. First of all since the properties of nanostructures exhibit significant differences from the bulk material such as the band structure, electrical, mechanical and optical properties. In fact, band engineering drives the big interest in nanostructures, where band gaps can be increased by reducing the nano-

material thickness. In semiconductor, reducing the dimensional freedom in carrier motion can induce modulation in the density of states as well as an increase of the material bandgap compared to the bulk material. Additionally, new device structures and applications emerge from band engineering which is done by designing different materials to structure the final device. By integrating other semiconductor materials on Si, different device applications including solar cells, logic devices, lasers and detectors could eventually be implemented on the same wafer. For optoelectronics, many compound semiconductors are preferred over Si because of the direct bandgap which increases absorption and light emission over indirect bandgap materials (such as Si, Ge). As discussed previously, to avoid substrate and device coupling and parasitic conduction, isolation from the bulk is often desired which explains the need for SOI-like substrates. Therefore semiconductor nanostructures are becoming popular because they provide an opening to more advanced devices. Different novel device applications and manufacturing methods are discussed extensively in [17]. Early device application of nanomembranes and nanowires has been demonstrated for the device architecture of Silicon-On-Nothing (SON) and GeON, allowing accommodation of a SOI-type and GeOI devices on a bulk Si wafer. The approach has been successfully extended to multi-channel and multi-gate devices.

#### 1.1.7.2 Literature on NW Fabrication techniques

Various fabrication techniques are being implemented and studied for semiconductor nanowire growth including bottom up and top-down approaches. In bottom-up approaches, the nanowire is grown, where as in top down approaches the nanowire is patterned or etched into the substrate or film.

##### 1.1.7.2.1 Bottom-up approach

One of the most popular approach for growing Si nanowire is by using vapor liquid solid (VLS) technique in which gold is used as the catalyst [18,19,20]. Gold droplets are formed by depositing thin film gold on the substrate and annealing it under vacuum to form gold nano-droplets. Under Si vapor, the Si grows on the gold catalyst and the dimensions can be controlled based on the size of the droplets. The Si nanowire growth occurs in the vertical direction and for device processing, the catalyst needs to be removed and the nanowire displaced physically to the active device area. Additionally, for Wrap around gate

nanowire, it is difficult to have access to the entire surface of the nanowire for gate stack deposition. It has also been reported in [21], where an aluminum catalyst was used, that gold catalyst leads to trapping of holes and electrons and contamination of the nanowires. Although different techniques are extensively being studied to produce high quality nanowire, obtaining a single crystalline Si nanowire and the post growth processing of the grown nanowire into transistor devices remain a big challenge.

###### 1.1.7.2.2 Top-down approach

In top down approaches, a combination of photolithography patterning and etching steps are implemented to carve the nanowire into the substrate. E-beam lithography is a technique which allows patterning of a photoresist by using a source of electrons as the exposure method. This lithography technique is quite advanced and can be used to pattern nano-sized photoresist patterns. However, since the write time is long, the processing throughput is very low because each active area is patterned individually.
Another method is by combining optical lithography and conformal film deposition technique, anisotropic etching and selective material etching. This method is described in more details in the following sections. It utilizes the spacer technology which is well known in semiconductor processing to prevent reduction of the effective channel length from the lateral diffusion of source/drain dopants into the channel. In the presented nanowire process flow, silicon oxide spacers are formed which serve as hard mask for Si etching. The limitation is in how small of a nanowire can be fabricated. However, the etched nanowire could further be trimmed by self-limiting oxidation.

# Chapter 2: Fabrication Experiment

## 2.1 Purpose of research

As discussed previously, the redistribution of source and drain dopants into the channel and substrate area impacts greatly the behavior of the MOSFET. Ideally, the channel length of the transistor is equal to the gate length. However, as depicted in Figure 5 , the effective channel length of the transistor is shorter than the designed channel length. As a consequence of the annealing step and subsequent high temperature processing steps, the source and drain dopants will redistribute around the channel area and thus the effective channel length will be shorter than the gate length. From the previous equations, the drain

current is inversely proportional to the channel length. Thus, the device behavior will be different. In addition, second order effects explained in the previous section strongly correlate with the S/D doping profile: the channel length modulation worsens with the shorter effective channel length, the depletions regions from the source and drain sides will be closer together which could potentially lead to punch-through. Furthermore, the gate loses electrostatic control over the channel as the channel length shortens and DIBL effects are more pronounced. The depletion region width at the drain side depends on the bias voltage and the doping profile at the p and n side of the junction. Assuming an abrupt junction, the depletion width W:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)V_{bi}} \qquad (6)$$

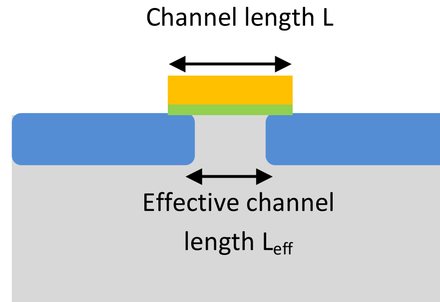



Figure 5: Effective channel length of MOSFET depicted.

In bulk Si structures, the diffusion of dopants is well understood. Initially, solid source doping was the method used to incorporate impurities in the source and drain regions during device fabrication. In order to achieve shallow depths in a controllable and repeatable manner, implantation was preferred as the method of doping as a consequence of scaling requirements. After implanting impurities in the crystal, an annealing step is necessary to activate dopants which will occupy a lattice site substituting a Si atom to free their electrons or holes to the crystal. During this annealing step, in depth and lateral diffusion is expected to occur, where dopants will redistribute themselves and increase the junction depth. In order to minimize this diffusion effect, different annealing techniques are implemented depending on the technology replacing the conventional furnace annealing which were done at elevated temperatures and for a long time. Unlike in conventional furnace annealing, rapid thermal annealing (RTA) requires only short duration with a significantly higher temperature ramp up (down) rate; then it would be preferable to

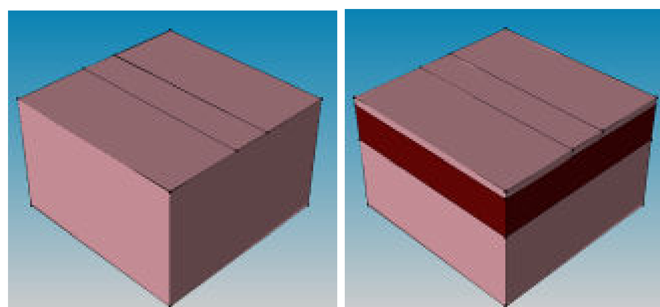
prevent extensive diffusion of impurities during activation. Furthermore, laser annealing allows the activation of dopants while eliminating diffusion of dopants.
In Si nanostructures, the diffusion of dopants has not been studied extensively. In thin SOI substrates, the Si active layer is considerably thinner than the thickness of the bulk, thus it is valid to investigate the diffusion of dopants in such structures. For MOSFET structures such as in the fully depleted SOI MOSFET (FD-SOI), the SOI layer is so thin, that the entire Si is depleted during operation, in this case the structure can be considered as a 2D nanostructure. While the nanowire MOSFET (NW-MOSFET) can be considered a 1D nanostructure since the diameter of the nanowire is typically only few nm. The diffusion in nanostructures is expected to differ from that of the bulk because of the reduced dimension and also the segregation effects which become more severe in SOI substrates. Different structures that resemble the ones described previously are fabricated to study the difference in the diffusion mechanisms in bulk compared to nanostructures. For practical reasons that will be dealt with more extensively in the next section, conventional characterization methods cannot be employed to measure the lateral junction depth in nanostructures due to their lack of resolution. Thus, electrical I-V measurements are used to correlate the resistance change the lateral diffusion in the structure.

## 2.2 Test structures

Because of the nano-scale and reduced dimensions, a precise control of doping levels and of the formation of pn junctions is required. This, in turn, necessitates precise understanding of diffusion mechanisms and surface effects that are likely to be significantly different from the bulk diffusion properties studied extensively in the scientific literature. In terms of diffusion mechanism, the novel nano-structures represent a radical departure from the conventional bulk MOSFET diffusion. While the dopant diffusion in bulk MOSFETs is largely a 3D phenomenon modulated by surface effects such as segregation and mechanical stresses, the diffusion in the new device architectures takes place in lower dimensional media. This work focuses on the dopant diffusion physics and mechanisms in silicon nanomembranes (2D), transitional nanoribbons (“1.X”D), and nanowires (1D) (see Figure 6), and attempts to benchmark the 1D-2D diffusion against the well-known bulk (3D) diffusion for exactly the same processing conditions. Particular attention is paid to

interface effects as they are likely to dominate the diffusion mechanisms in the aforementioned nanostructures.

In order to study the lateral diffusion of Si dopants in bulk compared to nanostructures, structures that resemble novel MOSFET structures were fabricated. As in the planar transistor, the Bulk structure shown in Figure 6 has source, channel and drain regions. Similarly, the nanomembrane, nanoribbon and nanowire structures resemble a FD-SOI transitor, a triple gate MOSFET and a NW-MOSFET respectively. The bulk and SOI substrates are p-type substrates with (100) wafer orientation. The experiment focuses on the diffusion of boron and phosphorus dopants in a p-type silicon substrate. In the case of boron, a resistor type structure is used, where the source and drain regions are doped using boron solid source diffusion, while the channel is masked by silicon dioxide. Meanwhile, in the case of phosphorus an n-p-n structure type is used, where the source and drain regions are doped using phosphorus solid source diffusion. As shown in Figure 6, all structures are fabricated on 400 µm square length silicon mesa islands with various channel lengths ranging from 5, 10, 20, 50 and 100 µm. The SOI substrates are provided by SOITEC and were fabricated using the smart cut technology. The dummy substrate is 800 µm thick, the BOX is 146 nm and the active Si layer, so called SOI, is 88 nm thick. Furthermore, the silicon nanomembranes, the nanoribbons and the nanowires are fabricated on the SOI substrates and thus are only 88 nm thick. The width of the nanoribbon channel ranges from 5-100 µm, acting as a transitional structure between the nanomembrane and the nanowire structures. However, in this work, the focus is only on the channel width of 5 µm. Additionally, in the NW structures twin nanowires were fabricated with a diameter ranging between 90 to 160 nm.



a. Bulk structure b. Nanomembrane structure

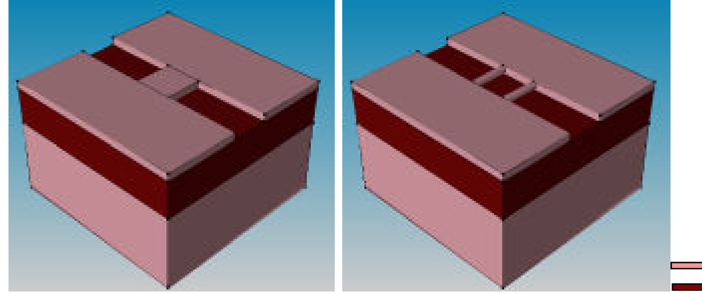


Figure 6: Bulk and nanostructure samples for diffusion study

Among each structure described, three sets of samples were fabricated: in one case, the source, drain and channel regions are all doped with the same dopant impurities to collect the resistance of the channel when it is uniformly doped. This sample is the control sample which allows us to monitor the rest of the samples since the S/D and channel are exposed to the ambient during the diffusion and the following annealing steps in the furnace. Therefore, the change in resistance of the control sample is monitored. In another case, two other samples which have a silicon dioxide mask on the channel area which acts a diffusion barrier against dopants during the solid source diffusion of the source and drain areas were fabricated. In the subsequent annealing steps, the oxide mask is maintained in the channel area on one sample and etched off in the other sample. These two latter samples provide the data for the interface effects in the lateral diffusion of S/D dopants into the channel. As shown in Figure 7 the three samples described previously are fabricated for each bulk, nanomembrane, nanoribbon and nanowire structures accounting for a total of 12 samples for boron doped samples and 12 samples for phosphorus doped samples. The fabrication technique for these samples will be discussed in detail in the following sections. Plasma enhanced chemical vapor deposited (PECVD) silicon oxide films are utilized as the diffusion barrier masks to prevent doping of the channel. Initially a pre deposition step at 1000 °C for 45 min in the furnace allows doping of the S/D regions. Following are two series of 3 hr drive-in steps at 1000 °C, where the mask is maintained on the channel to study the interface impact on the diffusion mechanisms in one sample and in the other sample the mask is removed prior to the annealing step. Additionally, I-V measurements are collected after the initial diffusion step, as well as in between drive-in steps. From the I-V measurement experimental data, the lateral diffusion length in the different structures will be extracted by using modeling and simulation.

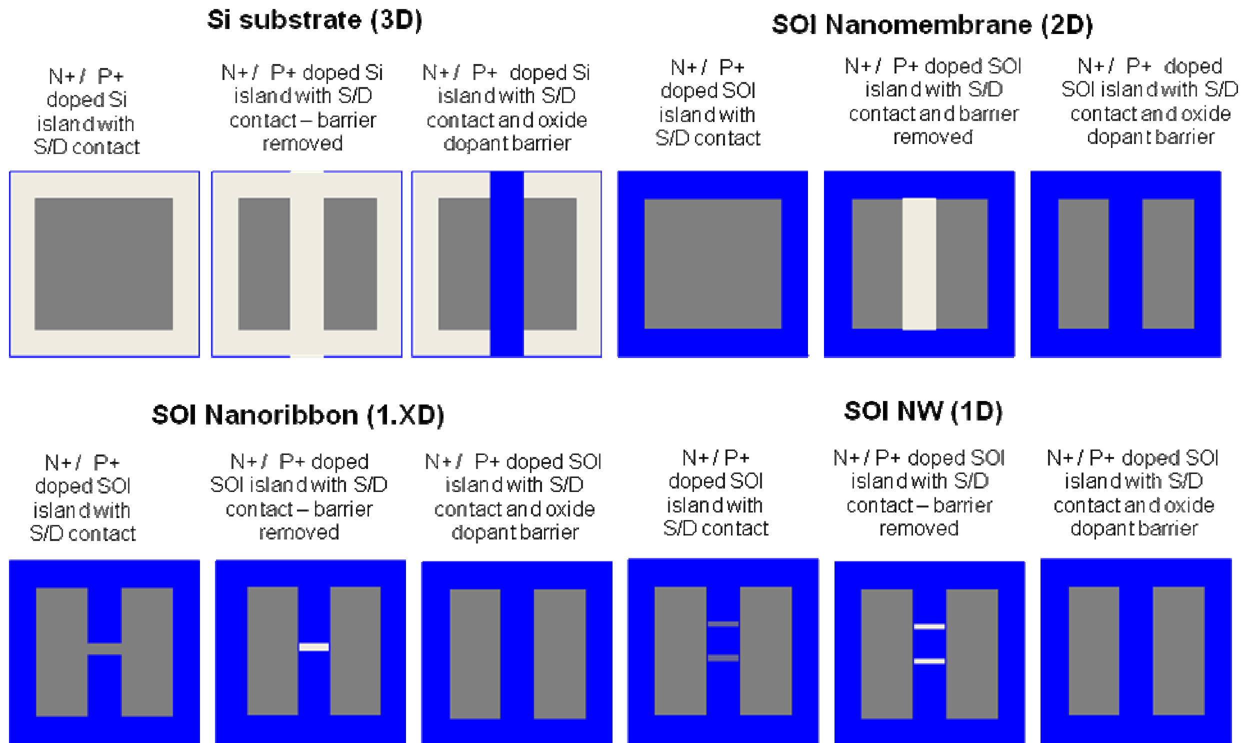


Figure 7: Diffusion test samples

### 2.3 Process Flow

A process flow was designed for each structure using a set of two masks. For each structure presented in the previous section, the process flow will be explained in details. In the following sections, a review of how the process flows for certain structures were optimized will be shown as well. The two photomask designs will be used for the active area (mesa-islands) patterning, the source and drain doping, the channel formation (both for the nanoribbon and nanowire), the channel mask and the source and drain contacts. It must be noted that all the nanostructures are fabricated on SOI substrates.

#### 2.3.1 Bulk structure

The Si bulk samples are fabricated on a substrate about 500 µm of thickness with 100 orientation. On the bulk, mesa islands are patterned to form the active device area and to be able to define consistently source and drain areas for the oxide diffusion barrier mask but also the source and drain contact areas. Thus the first patterning step allows us to define alignment marks for the subsequent steps in order to accurately identify the devices even after stripping the source and drain contacts. The purpose is to etch about 100 nm deep Si mesa-islands. The mesa-island patterning can be done using dry or wet etching. In the case

of dry etching, a photolithography step is done using the active area mask to pattern the positive photoresist. Then the exposed silicon areas can be etched using dry etching technique in the deep reactive ion etcher (DRIE) or the SAMCO reactive ion etcher (RIE), as shown in Figure 8. The details of the etching conditions and gases used will be covered in the following sections. The photoresist can then be stripped off the silicon using acetone. In the case of wet etching, few silicon etchants can be used such as KOH, TMAH, HNA which in some cases could require a hard mask because of the poor selectivity to the photoresist. A thin oxide or nitride film can be used as the hard mask for Si wet etching. For example, if TMAH is used as the Si wet etchant, the selectivity between Si to PECVD oxide and nitride etching is higher than 100 and above 1000 for grown oxide films [22]. Thus, only about 1 nm of oxide or nitride would be necessary to etch 100 nm of silicon. However, for practical reasons, an oxide or nitride layer of about 30 nm can be deposited using the plasma enhanced chemical vapor deposition (PECVD). Then, photolithography can be performed to pattern photoresist and mask the hard mask for oxide (nitride) etching. After oxide (nitride) etching, using buffered HF (BHF) or dry etching, the photoresist must be stripped before Si wet etching, followed by removal of oxide (nitride) mask which can be done in BHF. The wet etching method would require more process steps than the dry etching technique, but it can be used if a dry etching tool is not available. Additionally, the step profile for the two techniques would also differ depending on the etching isotropy.

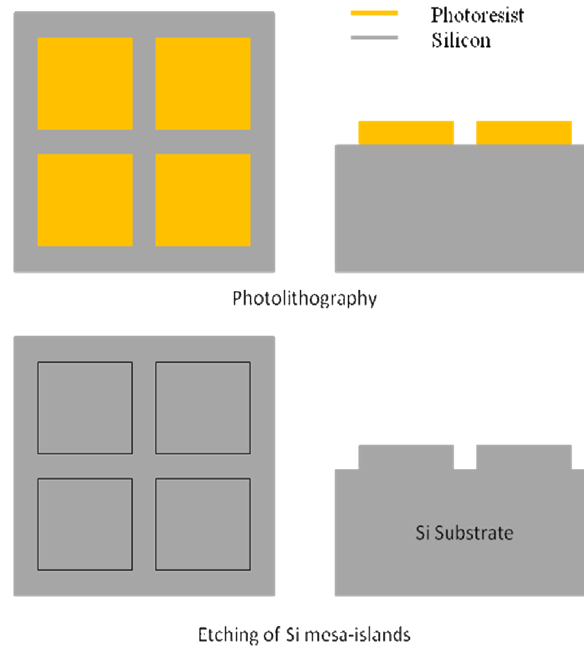



Figure 8: Process flow for mesa-islands in bulk Silicon showing top-view and cross sectional view

### 2.3.2 Nanomembrane structure

As mentioned previously the nanomembrane is fabricated on SOI substrates. The top Si layer which is the SOI is only 88 nm, the buried oxide (BOX) is 146 nm and the Si substrate is about 800 µm. Since the SOI is isolated from the bulk Si by the BOX, then the thin active Si layer is considered a nanomembrane. In turn, the nanomembrane is a two dimensional structure since its dimension is reduced in the direction of the bulk material. The aspect ratio between the in-plane area and the cross-sectional area is about 5000. Similarly to the bulk structure process flow, only one mask is required to fabricate the nanomembrane. The active area mask is used to perform lithography followed by a dry etch. In the nanomembrane, the BOX layer will act as an etch stop if the selectivity of Si to oxide in the etching technique used is high. Here also, a wet etching technique can be used alternatively, which might require additional hard mask if the etchant attacks photoresist too aggressively. The process flow for the nanomembrane structure is shown in Figure 9. Thus, the active device areas are separated from one another by the BOX isolation.

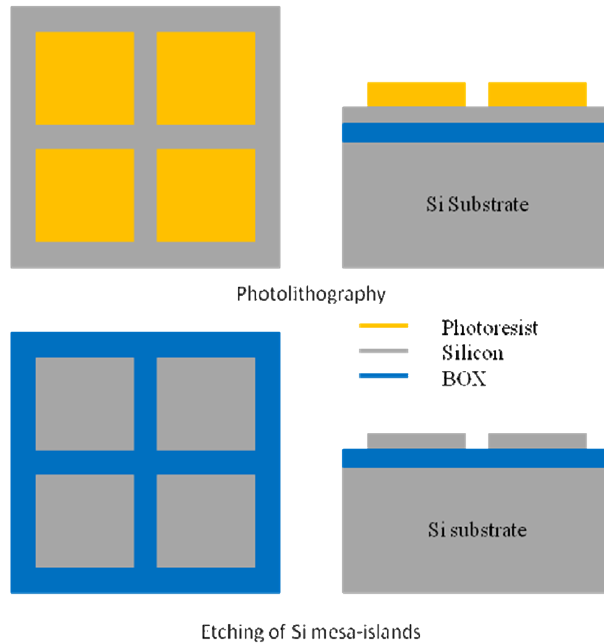



Figure 9: Nanomembrane process flow showing top-view and cross sectional view

### 2.3.3 Nanoribbon structure

In order to fabricate the nanoribbon structures, two masks and two types of photoresist are required. The first mask is the active area mask used in the previous structures and the second is the channel area mask. In addition, both a positive photoresist and a negative photoresist are needed to process the nanoribbons. Three photolithography steps and combination of material etches are required to complete this process. First blanket PECVD silicon dioxide is deposited on the SOI substrate. Then, photolithography is performed using the second mask to pattern the positive resist into strips. Following, the oxide hard mask is patterned into oxide strips which will protect the channel area during subsequent Si etch. The oxide can be etched using BHF or dry etching technique, after which the photoresist is stripped using acetone. Next, photolithography is performed again using the second mask, this time rotated by 90° with a negative photoresist to open windows that allow access to the excess Si to be etched. Then, Si is dry etched, the negative resist stripped and the oxide mask removed in BHF. Finally, another photolithography step is needed to pattern the mesa-islands using the first mask. The exposed Si is etched in DRIE or RIE and the photoresist is stripped. The above described steps are depicted in Figure 10. A method of reducing the process steps will be shown in another section. As seen below,

eight steps are required to fabricate this structure including photolithography, oxide deposition, oxide and Si etching.

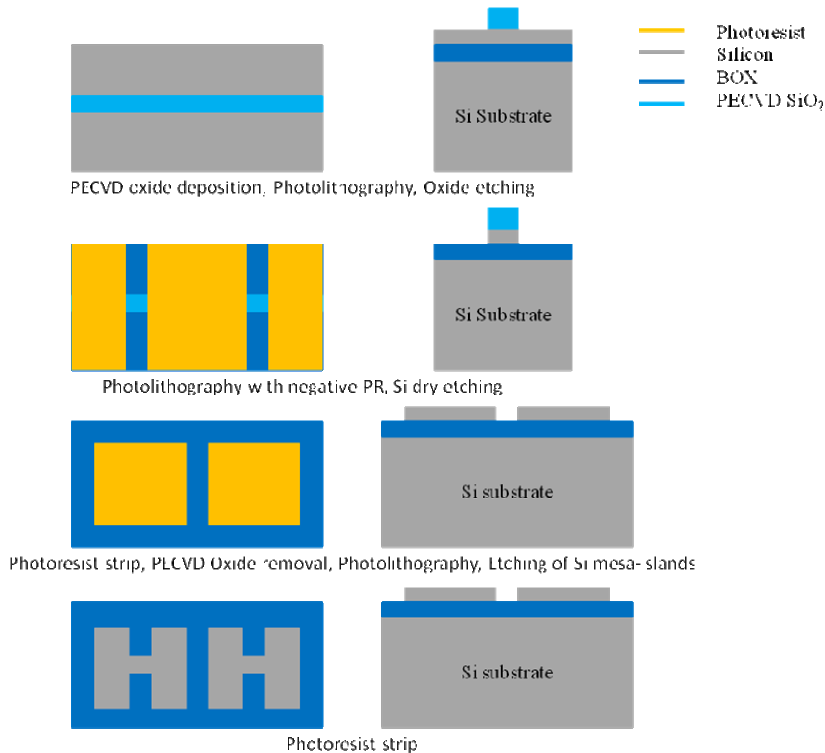



Figure 10: Nanoribbon Process flow showing both top-view and cross section views

### 2.3.4 Nanowire structure

In fabricating the nanowire structure, the same two masks used previously for the nanoribbons will be also used for the NW structures. The technique used to fabricate the NW is a top-down approach on SOI substrates which will result in twin nanowires. Here, the active areas are patterned by performing photolithography with positive photoresist and using the first mask. The exposed Si is etched down to the BOX using dry etch. Following, PECVD silicon nitride is deposited on mesa islands and on the rest of the wafer surface. Next, photolithography is performed using the channel mask (second mask) to pattern nitride into strips. Nitride is dry etched in a RIE system and caution needs to be taken to prevent overetching of the silicon. The etching can be controlled using timed etching if the etch rate is uniform and consistent from run to run. An alternative is to use a combination of dry and wet etching. In this case, the dry etching removes the majority of the film and the wet etch removes the remaining thin film without overetching the Si and limiting the undercut. Additionally, the photoresist soft mask is stripped in acetone. Then, a blanket

PECVD oxide layer is deposited over the nitride strip, exposed active areas and BOX areas uniformly. Since PECVD provides good step coverage, the nitride walls are also covered with the oxide film. Next, the blanket oxide film is etched anisotropically in the RIE system to form the so-called oxide spacers. The spacer technology allows the extension of lateral structures by tens of nm and is used extensively in CMOS processing. By etching blanket oxide previously deposited on nitride strips, the oxide remains on the sidewalls of the nitride strips due to the anisotropic etch. The spacers formed will then serve as the hard mask for the twin nanowire etch. To take advantage of the spacers as the Si etch hard mask, the nitride strips need to be etched selectively to the oxide spacers. Wet etching of nitride in phosphoric acid ($H_3PO_4$) is used to remove the nitride strips while leaving behind the oxide spacers. The height and width of the spacers are degraded during the nitride etch because of the finite selectivity between the bulk nitride and the thin oxide spacer. Typically, the spacers' width is in the order of 90 – 160 nm, after the removal of the nitride layer. Finally, the same masking technique used in the nanoribbon flow is utilized for the nanowire; a photolithography step is used with negative resist and the second mask (rotated by 90°) to protect source and drain regions and etch the excess Si in the channel area. Here, the Si underneath the oxide spacers will not be etched, thus forming twin nanowires. The photoresist can then be stripped in acetone. The steps described above are depicted in Figure 11.

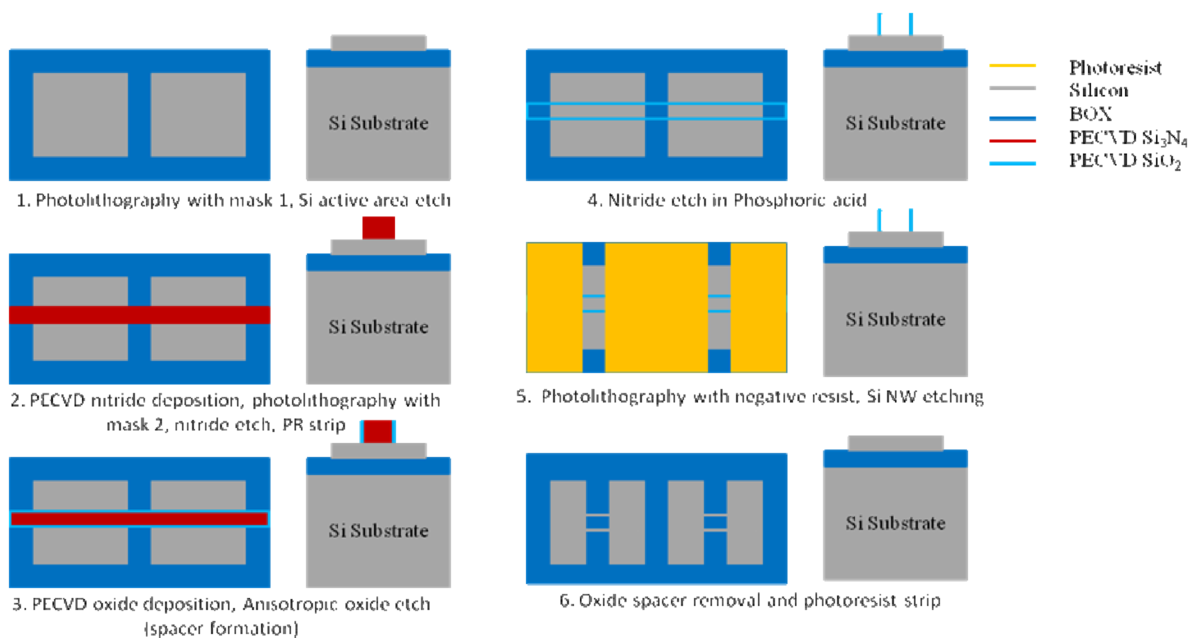



Figure 11: Nanowire Process flow with Top and cross section views

In the next section the process characterization will be discussed in detail, followed by the fabrication techniques used to improve the processing of these nanostructures as well as images from the fabricated samples.

### 2.4 Process Characterization

In order to successfully process the diffusion samples with optimum conditions, characterization of each processing step is required. The characterization step is usually done on dummy silicon wafers. The purpose is to ensure that each process step is repeatable and also compatible with the previous or next process steps or material. Standard process techniques and equipment for semiconductor fabrication have been used to process the diffusion samples. Each processing step required for this project will be described extensively in the next sections.

#### 2.4.1 Cleaning

In semiconductor fabrication, cleaning is an essential step of the process especially before any high temperature processing step. Contamination is a major concern for semiconductor since certain contamination such as metals can inhibit the device performance or act as traps, donors, acceptor impurities in the host substrate. Some of the known Si contaminants such as sodium are light elements and can diffuse fast in undesired regions of the device or substrate and alter the behavior of the device when contamination occurs in significant quantities. Other sources of contamination occur during the various processing steps. Thus, it is essential to efficiently clean the substrates during the processing and mostly prior to the pre-deposition and drive-in steps.

Various methods of cleaning recipes can be used to remove residual impurities from the Si substrates, either using wet chemical cleaning, dry or vapor cleaning. In wet chemical cleaning, solvents or mixture of acids can be used for cleaning. The most abundant solvents used for standard cleaning before photolithography or etching steps are acetone, isopropyl alcohol (IPA), Deionized (DI) water. The combination of acetone, IPA and DI water removes organic residual. DI water is used to rinse wafers in general whether it is after an acid etch or solvent clean. RCA is the original standard clean used in the semiconductor industry to remove organic and inorganic impurities.

In order to remove polymer residuals such as photoresist residuals, piranha clean is used. The piranha solution used is a mixture of sulfuric acid ($H_2SO_4$) and hydrogen peroxide ($H_2O_2$) with a volume ratio of 7:3 respectively at a temperature between 100 -140 °C for a duration of 10-15 min. Piranha removes gross organic materials from the wafer by wet-chemical oxidation of the Si wafers. Typically, it is necessary to remove the thin oxide layer grown after a piranha clean [23]. First the sulfuric acid is heated to 80 °C, after which $H_2O_2$ is slowly added and from the chemical reaction the temperature will raise. The wafer is then inserted in the mix and the cleaning is more efficient when the mix is enclosed to prevent evaporation of reactants. The cleaning will last between 10 to 15 min, after which the wafer needs to be rinsed under DI water for about 2-5 min to remove any residuals from the thick mixture. Next, the wafer is dipped in 50:1 $H_2O$:HF to remove the oxide grown from the piranha clean for about 30 s-1 min and rinsed under DI for about 2 min or more again. However, piranha does not remove inorganic residuals such as metals. Instead, the standard clean 2 (SC-2) is used to dissolve and remove alkali, metal traces and metal hydroxides from Si. The mixture consists of 6:1:1 $H_2O$: $H_2O_2$:HCl heated to a temperature about 80 °C and wafer cleaning duration of about 10-15 min is sufficient. First DI water is poured in the container then $H_2O_2$ followed by HCl and the mixture is heated to the specified temperature. Finally, after cleaning the wafer in the SC-2 mixture, it is rinsed for about 2 min in DI water. Usually, a dip in 50:1 HF will remove any oxide or ionic residuals, followed by a DI rinse again. The wafers are dried using dry $N_2$ gas to blow dry the Si substrates after each DI rinse.

Additionally $O_2$ plasma is also used to remove polymer residual from the wafer after lithography steps or etching steps. The oxygen plasma is available in various dry etching tools or in the plasma asher. Oxygen species are excited by the plasma and react with organic molecules to form water vapor or $CO_2$ which are then evacuated from the chamber via the vacuum pump.

The samples fabricated for the diffusion experiment are cleaned using $O_2$ plasma clean after stripping photoresist following an etching step to remove any polymer residuals left behind, followed by acetone IPA and DI water clean. Prior to the dopant pre-deposition step conducted at high temperature, the samples are cleaned using the piranha and SC-2 acid cleans described previously.

### 2.4.2 Photolithography

Photolithography is the most widely used form of lithography in the semiconductor industry, to transfer mask pattern on substrates or thin films. The combination of photolithography and etching steps is used to fabricate device structures with various functions. The concept is to spin photoresist which is a photo-sensitive polymer onto the substrate, whose solubility properties can be altered when exposed to UV light. The desired patterns are first transferred to a hard photomask, which is in turn used in the photolithography process. The photomask is a glass substrate on which chrome or chrome oxide (most common materials) is patterned. Glass areas of the photomask are transparent and will thus allow the UV light to pass through. However, areas of the photomask covered with chrome or chrome oxide are opaque and will block the UV light. Consequently patterns are obtained by combining the properties of the mask and the photoresist. There are two types of photoresist: positive and negative photoresists. When positive photoresist is used, the exact replica of the mask is obtained in the resist pattern. However, if negative resist is used, the reverse pattern of the mask is obtained. In positive lithography, the photoresist areas which are exposed to UV light are soluble when developed, while the unexposed areas are insoluble in the developer. On the other hand, in negative lithography exposed photoresist areas are insoluble and unexposed areas are soluble when developed, see Figure 12. The photolithography processes for the diffusion structures are all done using channel 2 of the MA-6 mask aligner which is the g-line, UV light wavelength of 436 nm.

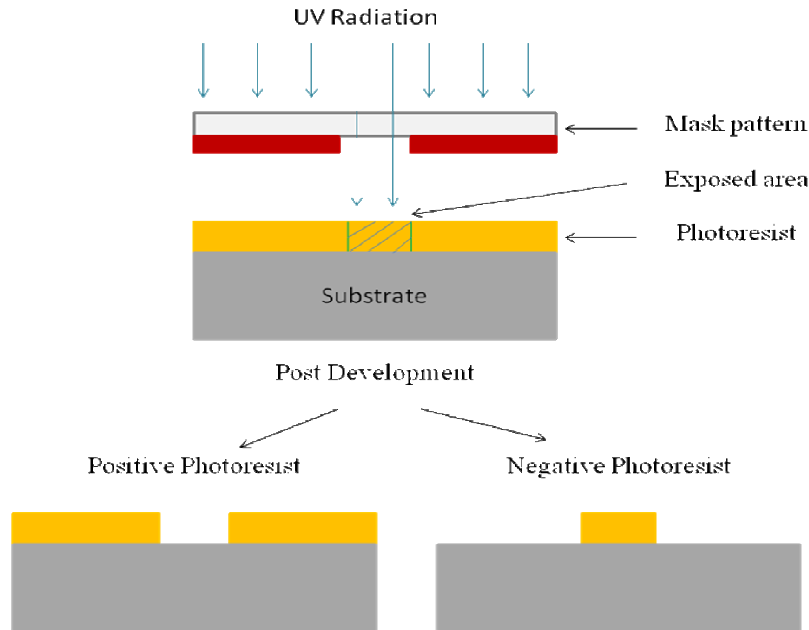
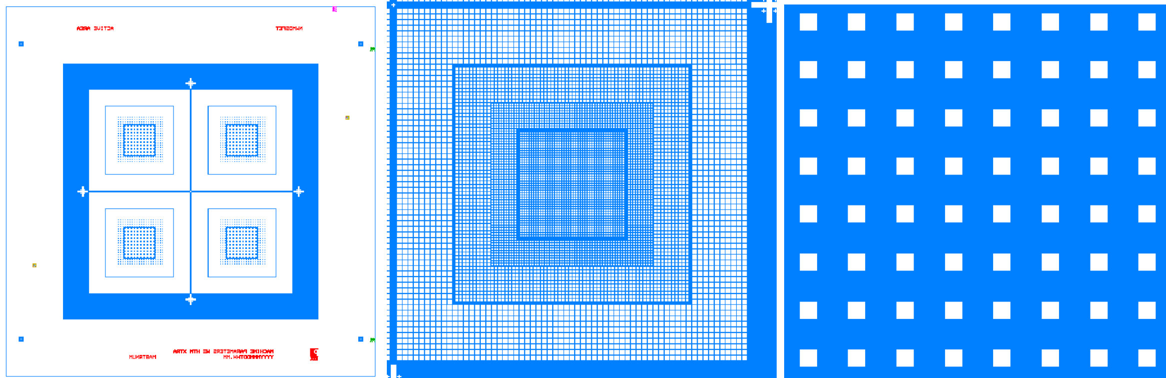


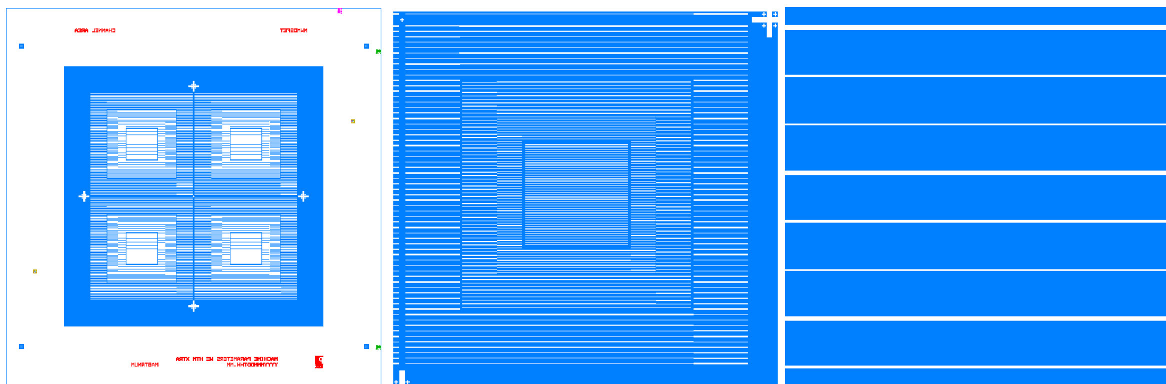

Figure 12: Negative and Positive Photolithography

#### 2.4.2.1 Mask layout

As described in the previous section, two photomasks were designed to fabricate the diffusion structures. In order to process the nanowire structures, three masks are necessary: the first mask for the active area patterning, the second for nitride strip patterning, the third for Si nanowire etch. The first mask is the active area mask which allows patterning of the Si mesa-islands. The mask patterns are square areas of length varying from 80, 100, 200 to 400 µm with a spacing of 150 µm between the structures. Instead of two separate masks, the channel mask was designed to serve both as a second and a third mask by just rotating it by 90°. Thus, the first mask had to be designed in such a way that it would have rotational symmetry to accommodate the second mask. As seen in Figure 13, the first mask is formed by repeating one block in four quadrants which are all the same. On the outer area of the block are the large patterns and in the inner area are the smaller size patterns. Also, by making the first mask patterns square, the desired rotational symmetry is obtained. Large alignment marks facilitate the mask alignment step and the smaller 1µm alignment mark improves the alignment precision and accuracy. The channel mask has lines of width varying from 5, 10, 20, 50, 100 µm which are the channel length in the diffusion structure.



Active area mask layout showing square areas of different sizes



Channel area mask layout showing chrome lines of different sizes for different size square areas

Figure 13: Photomask layout

#### 2.4.2.2 Photoresist recipes

As described previously in the process flow, both negative and positive lithography techniques are used to process the nanoribbon and nanowire samples. First the Si wafer is cleaned using acetone and IPA. If the wafer is cleaned with DI water in a prior cleaning step, then a dehydration hot plate bake at around 150 °C for at least 5 min is recommended to evaporate hydrogen and promote adhesion of the photoresist to the substrate. Additionally, hexamethyldisilazane (HMDS), which promotes the adhesion of photoresist to the substrate, is spun. Next the photoresist is spun to the wafer, followed by a pre bake (soft bake) to evaporate the resist solvents. Then the wafer is exposed, followed by the development step and the post bake to harden the resist prior to any etching or deposition steps.

Instead of acquiring both positive and negative photoresists, the image reversal photoresist AZ5214 was used instead. When exposed once, the image reversal photoresist behaves as a

positive resist. However, if a reversal bake and a followed exposure follow the first exposure, the resulting pattern will be just as the negative lithography pattern. Thus, the photoresist can be virtually implemented as a positive or negative photoresist. After long characterization of the image reversal (IR) resist, the conclusion was that it is more favorable to use it only in the negative resist mode. When the AZ5214 resist is used as a positive resist, the repeatability is a big concern. The IR resist adheres very poorly to the substrate when used in the positive resist mode. Dehydration times of up to 20 min at 150 °C where performed to help with adhesion to the substrate. Furthermore, HMDS can alter the sensitivity of the resist to the exposure. HMDS is normally applied by vapor deposition to only obtain a monolayer of an adhesion layer, since this technique is not available it is instead applied by spinning, which could result in a fairly thick adhesion layer. When the resist is applied on the HMDS layer, some evaporation from the HMDS to the resist occurs during the resist soft bake. This effect is seen during the development after the exposure step. Typically, exposure times between 5-9 s are sufficient to obtain the desired pattern with a development time less than 1 min. Instead, when HMDS is used in the process, the pattern cannot be developed even after development times as long as 5 min with exposure times up to 25 – 30 s. Different recipes were implemented to solve this adhesion issue, without HMDS the patterns are displaced after development (Figure 14), when HMDS is applied the development time is at 5 times larger than expected, the resist becomes less sensitive to the UV exposure. The number of drops of HMDS was counted and it was observed that reducing the HMDS amount applied improves the development time, also in some cases short bake times of the HMDS before applying the resist helps with the development time. However, the process is very hard to control, also the optimum recipe might not be repeatable is some cases. Thus, for the positive lithography and negative lithography, S1813 positive photoresist AZ5214 IR resist were used consecutively. In the negative lithography mode, adhesion is not an issue for AZ5214 IR resist.

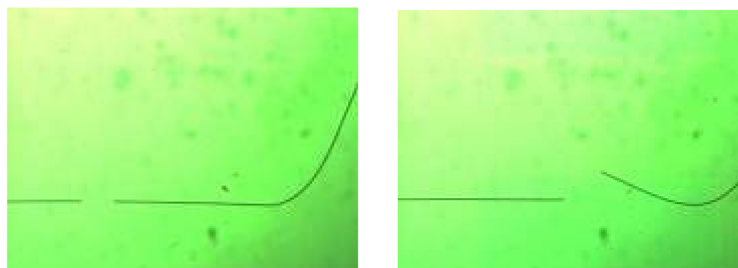


Figure 14: Microscope images showing displace photoresist lines due to adhesion issues

For both processes, a dehydration bake of 5 min at 150 °C is recommended, followed by spinning of 2 drops of HMDS at a spin speed of 4000 rpm for 45s. The photoresist is also spun at the same spinning conditions as the HMDS unless a liftoff process is being implemented, in which case a lower spin speed of 2000 rpm is recommended to obtain a thicker resist. The softbake is done at 100°C for 1 min. For S1813 resist, an exposure of 7 s at 11mW/cm$^2$ is sufficient to achieve a development time less than 1 min, a post bake at 100 °C for 1min. Microscope images of the active area S1813 photoresist patterns on the substrate are shown in Figure 15 below.

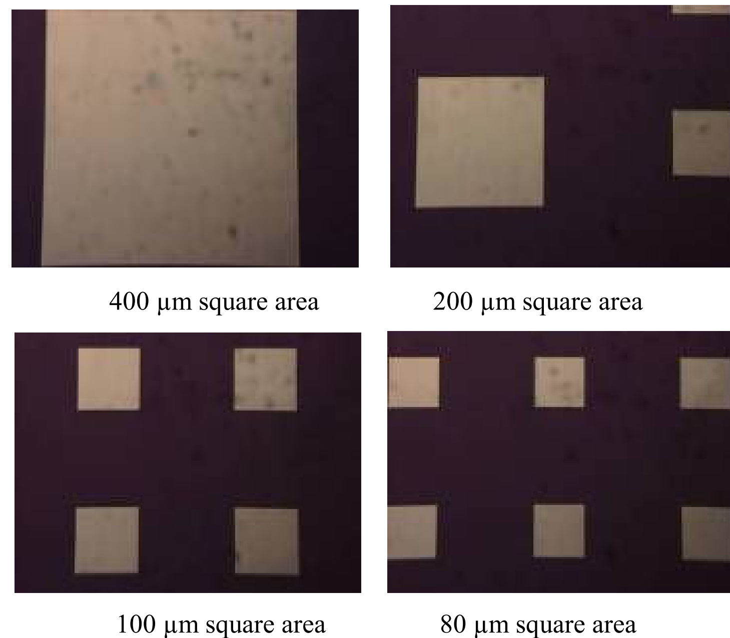



Figure 15: S1813 Photoresist patterns on substrate after exposure with active area mask

For AZ5214 IR resist, the first exposure is 4s long to generate the pattern, followed by a reversal bake at 115 °C for 1 min which reverses the photosensitivity properties of the resist layer. After this first exposure and reversal bake, the areas which did not get exposed behave as a positive resist and are soluble in the developer if exposed the second time, and the areas which have been exposed behave as a negative resist and are insoluble in the developer if exposed the second time. Thus, flood exposure energy of at least 200 mJ/cm$^2$ (18 s in g-line) is needed after the reversal bake to expose the areas which have not been exposed in the first exposure. The AZ5214 IR resist process steps are depicted in Figure 16. In Figure 17, the IR resist pattern in the negative mode is shown, the channel area mask is

used to generate the pattern resulting in an opening in the channel area to allow access to excess Si etch to form Si NW. Additionally, IR resist profile has a negative slope and thus is desired for liftoff processes.

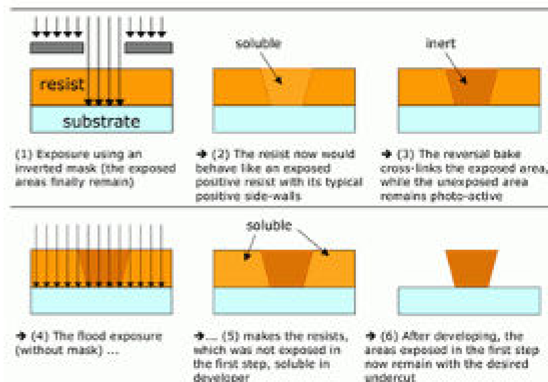



Figure 16: How image reversal resist works [24]

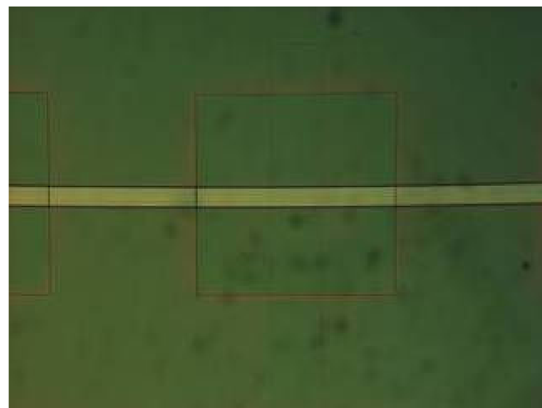


Figure 17: AZ5214 IR photoresist on Si island with resist opening in channel area for Si NW etch

Additional the properties of the AZ5214 were investigated and exploited further which resulted in a provisional patent being filed. This new lithography process will be described separately in another section.

### 2.4.3 PECVD

The Trion plasma enhanced chemical vapor deposition (PECVD) model is utilized to deposit silicon oxide and silicon nitride for the diffusion structure processing. The Trion PECVD is a parallel plate configuration also called a triode reactor shown in Figure 18. The RF of 13.56 MHz is put at the top plate and a RF of 360 kHz is put on the bottom plate which is the substrate chuck. The high frequency controls the plasma density while the low

frequency controls the acceleration of ions towards the substrate and promotes surface reaction. The inductive coupled plasma (ICP) controls the plasma density.

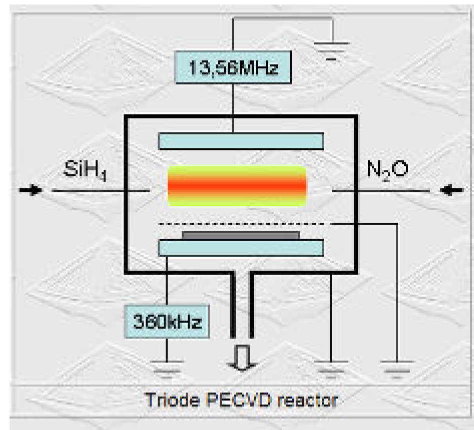



Figure 18: PECVD Triode reactor [25]

For silicon oxide deposition, silane ($SiH_4$) gas and nitrous oxide ($N_2O$) gas are used as reactants: $3SiH_4 + 6N_2O \rightarrow 3SiO_2 + 4NH_3 + 4N_2$. (7)

For silicon nitride deposition, silane and ammonia ($NH_3$) gases are used as the reactant gas:

$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 6H_2$ (8)

The following recipes in Table 2 are used for $SiO_2$ and $Si_3N_4$ depositions. The quality, uniformity, deposition rate and density of the oxide and nitride films can be controlled by the parameters listed in the table below. It must be noted that during the deposition, the ICP/RIE reflective powers must be monitored and maintained at steady values. During ideal deposition conditions, the ICP reflective power must be less than 6W and the RIE power less than 1-2W. Both powers control the plasma density and the flow of ions towards the surface substrate and thus high reflective powers will affect the deposition rate and quality of the film. The process deposition uniformity and rate is monitored by measuring the oxide/nitride thickness at different locations of the wafer (center, top, bottom, right, left) using the filmetrics, which is an optical measurement technique. Under these conditions, the deposition rate of oxide is stable at about 1nm/s with wafer uniformity of about 5-6%. The deposition rate of nitride is between 1.1 – 1.3 nm/s with wafer uniformity of about 10%.

Table 2: PECVD $SiO_2$ and $Si_3N_4$ recipes

| PECVD parameters | $SiO_2$ | $Si_3N_4$ |
|---|---|---|
| Pressure (mT) | 900 | 600 |
| ICP forward power (W) | 175 | 175 |

| | | |
|---|---|---|
| RIE forward power (W) | 50 | 50 |
| $SiH_4$ flow rate (sccm) | 300 | 600 |
| $N_2O$ flow rate (sccm) | 71 | 0 |
| $NH_3$ flow rate (sccm) | 0 | 15 |
| Substrate chuck temperature °C | 360 | 360 |

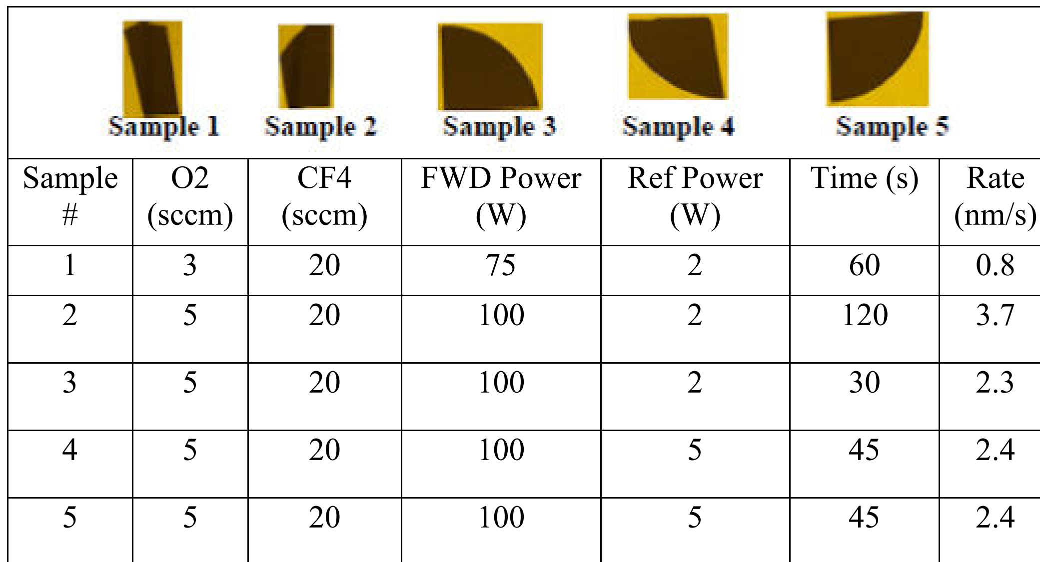
### 2.4.4 Dry Etching

Dry etching equipments are plasma based reactors driven by a combination of both physical and chemical etching. Plasma is formed by introducing a suitable gas into a high vacuum chamber and applying an RF field to that chamber so that a glow-discharge occurs. The gas is selected for its ability to produce reactive species upon excitation that will react chemically with the surface to be etched, forming volatile compounds. When the RF field is applied, the gas becomes ionized with essentially equal numbers of positive and negative ions. The plasma may also contain a population of free radicals which is an atom or collection of atoms, that is electrically neutral, but exhibits incomplete chemical bonding, making it highly chemically active. It is these reactive free radical species that are of primary interest in plasma etching applications. The plasma etching of substrate material is driven by the presence of free radical species, the position of substrate near the plasma to promote diffusion of radical species on the surface, the absorption of the etching species on the surface to promote chemical reaction, and the ease of desorption of by products from substrate surface and out of the plasma environment [26].

Dry etching is needed in this process to pattern the Si mesa-islands and the different hard masks including the nitride strips, the oxide spacers, the Si nanowires, and the oxide diffusion barrier mask. Initially, the Samco Reactive Ion etch (RIE) was being used to pattern the Si mesa-islands and dielectric masks. However, the etch rates were not stable. The etch rate varies with the etch time, the longer the etch time, the lower the etch rate. Thus it was hard to control the etching process and determine the stopping point to avoid over-etching the underlying film layer. Furthermore, the etch uniformity is poor for oxide and nitride films, which is an issue for the spacer process. For Si mesa-islands, the etching of the structure is not a critical step, especially for the SOI where the underlying BOX is an etchant stop. Thus, the following recipes were implemented to characterize the optimum etching conditions for the Si mesa-islands etch. In this equipment, Si is etched by mixing $CF_4$ and $O_2$. Only the Fluorine in $CF_4$ etches Si, however it has been reported that $O_2$

presence is needed to prevent build up of fluorocarbon on the Si and inhibit access of fluorine to the Si [27]. From Table 3 below, samples 1 and 2 are 1/8 the size of a 4" diameter Si wafer, while samples 3-5 are ¼ the size of the wafer. The etch rate for sample 1 is considerably lower since both the $O_2$ flow rate and power used are lower. The etch rate of sample 2 is the highest although the same gas flow and power were used for samples 3-5; however because sample 2 is half the size of the rest, the etch rate was much faster.

Table 3: Characterization data for Si dry etch in $CF_4$ and $O_2$




| Sample # | O2 (sccm) | CF4 (sccm) | FWD Power (W) | Ref Power (W) | Time (s) | Rate (nm/s) |
|---|---|---|---|---|---|---|
| 1 | 3 | 20 | 75 | 2 | 60 | 0.8 |
| 2 | 5 | 20 | 100 | 2 | 120 | 3.7 |
| 3 | 5 | 20 | 100 | 2 | 30 | 2.3 |
| 4 | 5 | 20 | 100 | 5 | 45 | 2.4 |
| 5 | 5 | 20 | 100 | 5 | 45 | 2.4 |

The same process conditions for samples 2-5 were used to etch the Si and SOI mesa-islands. Figure 19 below shows an optical microscope image of the Si and SOI mesa-islands after the photoresist is stripped.

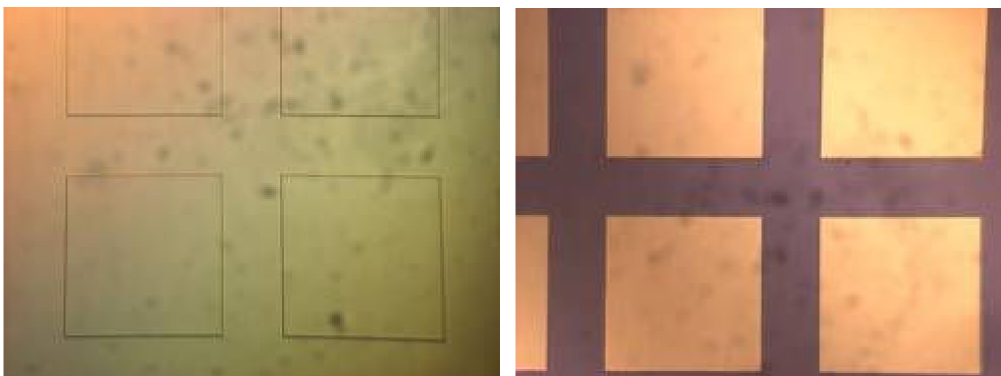


Figure 19: Si mesa-islands (left). SOI mesa-islands (BOX in dark blue, 88nm thick Si in yellow-green)

The Deep Reactive Ion etcher (DRIE) is a highly anisotropic dry etching technique which can produce high aspect ratio trenches. The Alcatel DRIE employs the Bosch process

which combines an etching step followed by a passivation step to produce long range anisotropically etched structures. First Si is etched using $SF_6$ and the sidewalls and bottom of the step is then passivated using $C_4F_8$, which gets removed from the bottom in the subsequent $SF_6$ etching step. Thus, the sidewalls of the trench are protected during the subsequent $SF_6$ etching cycle resulting in a long range anisotropic etch. This technique is preferred for the nanowire and nanoribbon channel etches since it is anisotropic etch and thus the etch is more controlled. Additionally, the etching is uniform and the etch rates are highly stable. Few process parameters such as the ICP power, the $SF_6$ and $C_4F_8$ flow rates were modified. Moreover, the etch duration to passivation duration ratio were reduced for 7 to 1, in order to minimize any overetching and optimize the etching profile. In the Si etch recipe used 8 s is sufficient to etch the nanowire and nanoribbon structures. Figure 20 shows optical microscope image of the nanoribbon and a Secondary electron microscope (SEM) image of the nanowire, after Si DRIE etch and photoresist strip.

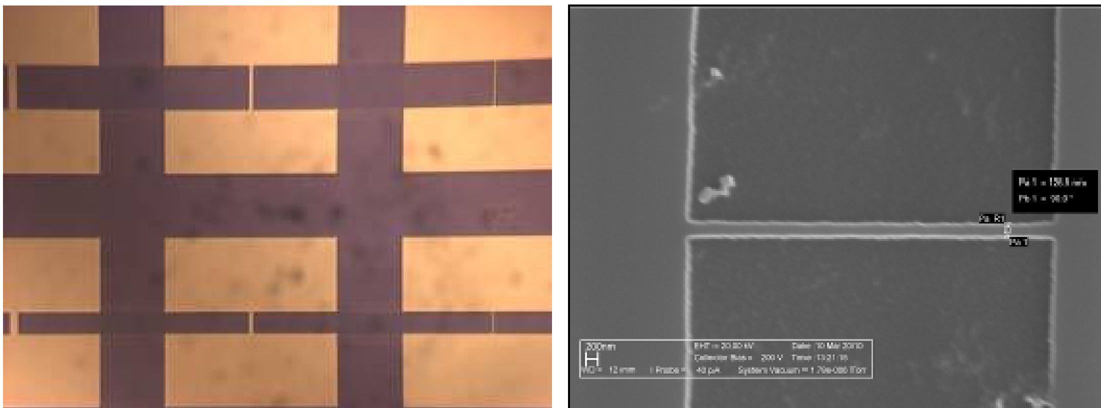


Figure 20: Nanoribbon structure (left). SEM image of Nanowire structure with 120 nm diameter (right)

Additionally, oxide and nitride etching were done in the DRIE using $C_4F_8$ as the reactant gas. The etching rates are stable, reproducible with good wafer uniformity. The power was decreased to slow down the etch rate to about 60 Å/s to avoid over etching the underlying Si film. The only disadvantage observed was a polymer build up whenever the etching stops, whether it is before or after the Si layer is reached. This problem was observed during the characterization of the oxide etch rates. A blanket PECVD oxide film deposited on Si was being etched in the DRIE. The oxide film was etched in different steps with a film thickness measurement after each step to monitor the etch rate and uniformity. However, after the first etch and measurement step, the oxide was not getting etched after

being placed back in the DRIE chamber. Instead, when measuring the oxide thickness, the thickness was seemingly growing. From the colors on the wafer, it was clear that a thick layer of oxide was still on the surface of the substrate. The wafer was rinsed in DI water to observe whether it would be hydrophobic or hydrophilic. It is known that Si is hydrophobic and $SiO_2$ is hydrophilic. However, the surface of the wafer which is supposed to have an oxide layer on it, was hydrophobic. The substrate was cleaned in $O_2$ plasma which helps strip polymers, after which the oxide thickness measurement were acceptable when compared to the oxide color chart and the surface was then hydrophilic as expected. Thus $O_2$ clean was incorporated as part of the oxide and nitride etching to remove the polymer whenever additional etching is required. The optical microscope images of the nitride channel strips on Si islands are shown in Figure 21.

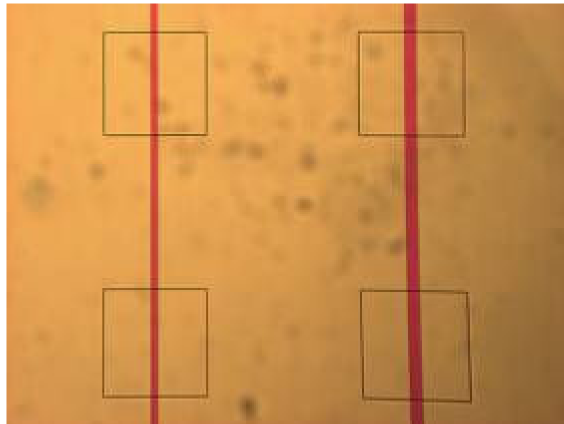


Figure 21: Image of nitride strips on Si islands prior to oxidation deposition for spacer formation

### 2.4.5 Wet Etching

In the processing, BHF (Buffered HF) is used to etch silicon dioxide and remove $SiO_2$ and $Si_3N_4$ from undesired regions of the Si substrate. Typically 10:1 BHF is used to remove or etch thick oxide films. In order to deglaze the Si after the pre deposition where phosphorus glass forms, the substrate is dipped in BHF for about 30 s -1min. An easy check to see if the film is entirely removed from Si is to observe the hydrophobic/hydrophilic properties of the substrate. Si is hydrophobic while oxide and nitride are hydrophilic films, thus by monitoring these behaviors, it can be checked that the film is removed. The characterized etch rate is about 67 nm/min and remains stable in 10:1 BHF. In addition by diluting the 10:1 BHF with DI water to obtain 50:1 BHF, the native oxide can be removed as well as the oxide that is grown for annealing Si in the furnace in $N_2$ ambient.

Phosphoric acid of 85% in aqueous solution etches the nitride with a selectivity of 3:1 to the oxide. The phosphoric acid etch is done at about 100 ºC where 100 mL of acid is heated at a hot plate temperature of about 180 ºC. The phosphoric acid is used to remove the nitride selectively to the oxide after the oxide spacer formation. The phosphoric acid etching temperature was optimized to obtain the highest selectivity in order to prevent the oxide spacers from getting completed eroded during the nitride etch.

Another wet etching step is required to etch Al with selectivity to Si and $SiO_2$. After the dopant pre deposition step and the annealing steps, Al is deposited in the source and drain regions as contact electrodes for IV measurements. Before, the subsequent annealing step which is at 1000 ºC, the Al is removed from the source and drain regions and since the Si is exposed after Al is removed and $SiO_2$ is exposed during the etching process, it is imperative that the oxide and Si films be immune to the etchant chosen. From [28], the Al etchant aqua regia (3 HCl: 1$HNO_3$ : 2$H_2O$) at 30 ºC is highly selective to oxide and Si with an etch rate of 0 nm/min.

### 2.4.6 PVD and metallization

Physical vapor deposition (PVD) is a deposition technique which is based on evaporation or sputtering of solid source material from a crucible or target to a substrate. The PVD equipment used is the Kurt Lesker PVD 250 model which is an e-beam evaporation based tool, where the deposition material is melted using a source of electrons. The crucible contains the source material and is cooled using water during the deposition to avoid melting and contamination. The deposition is done under the high vacuum, where highly energetic electrons impact the crucible until the evaporation temperature of the material is reached and deposition starts.

#### 2.4.6.1 Al contact

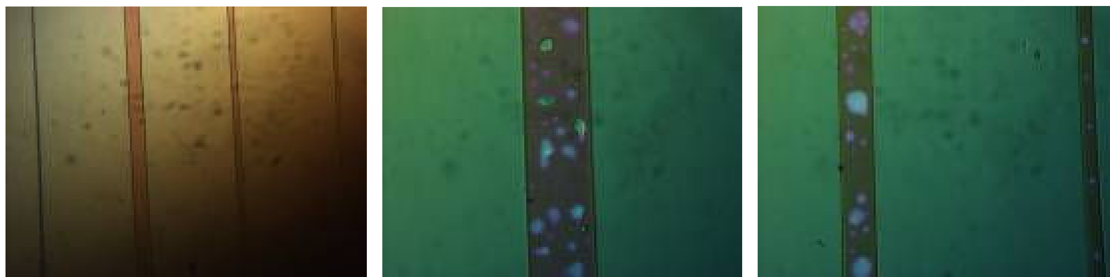
Al contacts are deposited on source on drain regions to serve as electrodes in I-V measurements. Al deposition in the e-beam PVD system is well known and currently a recipe is already implemented for Al deposition in the automatic mode. In the automatic, the user inputs the desired thickness and the tool performs the deposition based on specifications such as power ramp rate and deposition rate. The PVD can also run in the manual mode, where the user can control the e-beam shape (longitudinal and lateral amplitudes), the rotational frequency, the current ramp rate, the deposition rate, etc. The

thickness is monitored using a crystal which monitors the thickness based on the density and Z-ratio of the material, The Z-ratio is a parameter that corrects the frequency-change-to-thickness transfer function for the effects of acoustic-impedance mismatch between the crystal and the deposited material. For example, the density and Z-ratio of Al are 2.73 $g/cm^3$ and 1.080 respectively. For the diffusion experiment, Al is deposited at least on six different occasions after annealing and drive-in steps for boron and phosphorus samples. Thus, it is imperative to extend the lifetime of the crucible, which easily cracks due to thermal shock and high currents. Furthermore, the manual mode is used for the diffusion experiment since the ramp up and ramp down can be better controlled to avoid cracking the crucible. Additionally, the chamber pressure is lowered to about $1\times10^{-6}$ Torr before the deposition so that the required current is lower than for a higher pressure. Thus, a high deposition rate is obtained at lower current: the deposition rate is about 1.8 Å/s at a pressure of $4.5\times10^{-6}$ Torr and e-beam current of 140 mA, while the deposition rate is 4 Å/s at a pressure of $1.5\times10^{-6}$ Torr and e-beam current of 40 mA. For the contacts, a thickness of 150 nm of Al is deposited.

### 2.4.7 Diffusion

The source and drain are doped with phosphorus or boron using solid source diffusion. The phosphorus glass substrates and boron glass substrates are put in close proximity to the wafer. During the pre deposition process, phosphorus (boron) doped silicon oxide grows on the Si substrate and simultaneously, the dopants diffuse into the silicon. First, the wafers are cleaned thoroughly in piranha and SC-2 clean described previously, then the cleaned boat, the substrate and solid sources are loaded to a quart boat. The furnace is ramped up to 600 °C and $N_2$ flow of 3L/min is turned on to fill the furnace with $N_2$ for at least 3 min and minimize other ambient gas flow. The boat is then loaded in the furnace and the temperature is ramped to 1000 °C and the $N_2$ flow is ramped up to 5L/min after this temperature is reached the pre deposition is timed for 45 min. After the pre deposition is finished, the temperature is ramped back down to 600 °C before slow unloading. The furnace ramp up rate is about 27 °C/min and the furnace ramp down rate slower at about 8.9 °C/min.

In order to prevent doping of channel during source and drain solid source diffusion. A diffusion barrier mask needs to be deposited on the channel area. This diffusion barrier mask is chosen such that it prevents diffusion of boron and phosphorus into the channel. An ideal candidate for the barrier mask is silicon nitride. From [26], during constant source diffusion, an oxide thickness of 300 nm is required for phosphorus and 500 nm for Boron for a pre-deposition temperature of 1000 °C for an hour. Nitride is reported to be a more efficient diffusion barrier than oxide since the diffusivity of phosphorus and boron is lower in nitride. However, the deposited PECVD nitride showed signs of pinholes as shown in Figure 22. In this case, phosphorus doping is demonstrated and the $P_2O_5$ glass diffuses through the nitride and reaches the silicon forming pits on the Si surface after the etching of the phosphorus glass, called the deglazing step.



$Si_3N_4$ on Si pre Phosphorus doping $P_2O_5$ Pits in $Si_3N_4$ channel strips post Phosphorus doping

Pits observed in $Si_3N_4$ after deglazing of sample in HF. Pits also observed on Si after nitride removal

Figure 22: Damage observed in nitride and Si after Phosphorus doping

Instead of using nitride as the diffusion barrier mask, oxide was chosen since this damage is not observed in an oxide mask. The vendor also recommends introducing small amount of $O_2$ in the furnace during the doping process to avoid Si damage, however, because of the thin SOI thickness of only 88 nm, purposefully introducing $O_2$ in the chamber will result in oxidation and consumption of Si. Instead, thin $SiO_2$ of about 30 nm was deposited on the source and drain regions, to reduce oxidation of the Si and to prevent damage. Two experiments were characterized; the first one consisted of depositing 800 nm thick of oxide

on Si and doping it with solid source diffusion at 1000 °C for 2 hrs and doing SIMS measurement to verify that the underlying Si remained undoped. Thus, the experiment is a check to see if the oxide is an efficient diffusion barrier. Figure 23 shows the SIMS profiling resulting from the sample and confirmed that Phosphorus did not diffuse into the Si layer. Furthermore, an experiment was conducted to understand how the phosphorus profile in Si varies if a 30 nm thick oxide protective layer is deposited to protect the S/D regions. Figure 24 shows that the peak concentration drops and the junction is shallower when an oxide protective layer is deposited on Si, however, the concentration remains high for desired Ohmic contact and for the diffusion experiment.

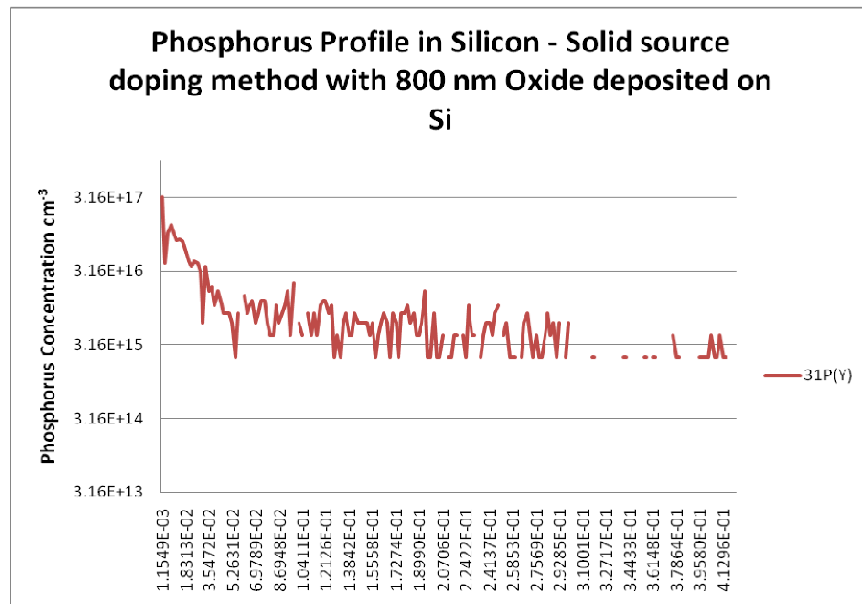



Figure 23: Phosphorus profile in Si after diffusion barrier oxide mask of 800 nm used

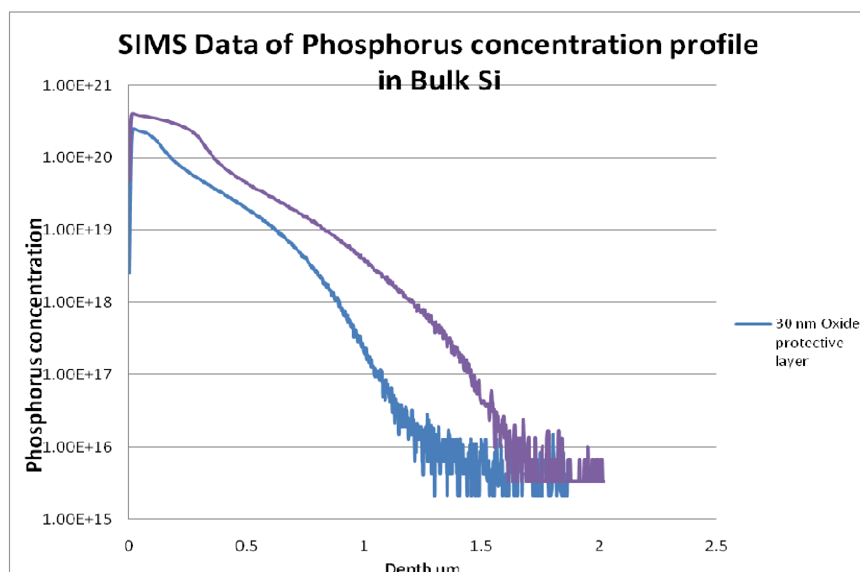



Figure 24: Comparison of Phosphorus profile with and without oxide protective layer

## 2.5 Spacer and Nanowire Process Fabrication

The most challenging fabrication is the nanowire structure formation since nanowire width between 90 nm – 160 nm are fabricated by combining g-line photolithography with the spacer technology. The fabricated nanowires can only be seen after the fabrication using secondary electron microscopy (SEM). Thus, the most critical step is the fabrication of spacers for which the process steps are depicted in Figure 25. Initially, a PECVD nitride film is deposited on the Si islands. Next, the nitride layer is patterned into strips centered at the active area using the second mask. The width of the strips varies from 5, 10, 20, 50, 100 µm. Subsequently, a conformal PECVD oxide film is deposited on the wafer. Using $C_4F_8$ DRIE plasma, the oxide is etched back anisotropically leaving just thin oxide spacers along the vertical sidewalls of the nitride strip (and Si islands as well). Subsequently, the nitride strip is removed in hot phosphoric acid. Despite the significant selectivity (10:1) of bulk nitride film etch relative to bulk oxide film etch [27]; in this last step, the twin oxide spacers (width and height) will undergo significant erosion due to their small features and etch exposure from three sides. The role of the nitride and oxide thicknesses in the final oxide spacer dimensions will be discussed in the Experimental Results section.

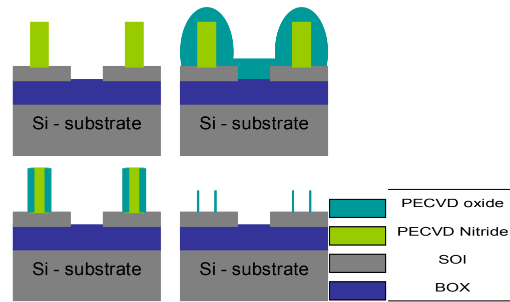



Figure 25: Illustration of oxide spacer formation

The following step is the Si nanowire etching. In the subsequent step, the second mask is now being rotated by 90 ° to pattern negative photoresist (PR) which serves as a soft mask for S/D regions during the Si twin nanowire $SF_6$ plasma etch.

### 2.5.1 Experimental Results

As discussed previously, the most critical step of this process flow is the formation of the oxide spacers which serve as a mask for twin Si nanowires etch. The initial characterization experiments were done on bulk Si substrates to reduce substrate costs. Figure 26 shows the initial oxide spacer fabricated. The microscope images capture the nitride strip on the Si active area after formation of the oxide spacers. The thickness of the nitride (~ 340 nm) is determined using a profilometer. The thickness of the oxide deposited on top of the nitride strips is ~320 nm. The oxide etch rates in $C_4F_8$ plasma were previously characterized, in order to obtain the etch time necessary to form the spacers. SEM images, both top and cross sectional views, of these spacers are shown in Figure 26. As shown in the cross section view, the resulting shape of the spacer is triangular. The measured spacer width at the base was about 140 nm and the height about 90 nm.

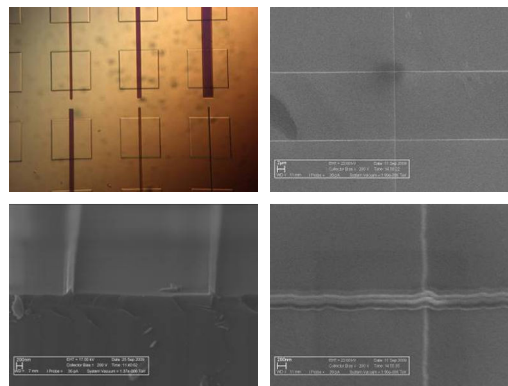


Figure 26: $Si_3N_4$ strips on Si islands (top left), SEM images of twin spacers post removal of 5µm wide $Si_3N_4$ strip (top right and bottom).

In general, the nitride strip thickness and deposited oxide thickness determine respectively the height and width of the spacers. Conformal step coverage is required during PECVD oxide deposition to guarantee a high quality oxide spacer mask. The oxide spacers serve as masks for subsequent Si nanowire etch. The spacers' final dimensions depend on the selectivity of the oxide spacer etch relative to the nitride during the phosphoric acid etch of nitride. Larger dimensions of the nitride regions compared to the oxide spacers' dimensions reduce the selectivity between the two materials. One observes that the top of the spacer is narrower than its bottom, pointing to the expected enhanced erosion of the top part of the spacer. Consequently, this effect reduces the height of the spacer even further.

The following experiment was performed to understand the impact of the ratio of the deposited nitride thickness to the oxide thickness on the final spacer width, which in turn determines the dimensions of the Si NW. In this experiment, about 400 nm of PECVD nitride has been deposited and patterned into strips. The sample was then broken into multiple pieces. On each piece the deposited oxide thickness has been varied. **Table 4** indicates the average nitride thickness as well as the oxide deposited on each piece. As illustrated in the process flow, the oxide was etched back anisotropically to form spacers. The nitride strip were then removed in phosphoric acid etch. Each sample underwent approximately the same phosphoric acid etch time, temperature and agitation. The thicker the nitride and the longer the nitride etch time, the narrower is the resulting spacer width. The resulting spacer widths are listed in the third column of Table 4. A sub 100 nm spacer width was achieved. Also the SEM images of these spacers are shown in Figure 27. It must be noted that the height of the spacer is important since the oxide spacer mask has to withstand the subsequent Si etch to form the Si nanowire.

Table 4: Dependency of spacer width on deposited oxide and nitride thickness

| Sample # | Nitride thickness (nm) | Oxide thickness (nm) | Spacer width (nm) |
|---|---|---|---|
| 1 | 398 | 397 | 260 |
| 2 | 401 | 187 | 160 |

| 3 | 392 | 148 | 110 |
|---|---|---|---|
| 4 | 386 | 98 | <90 |

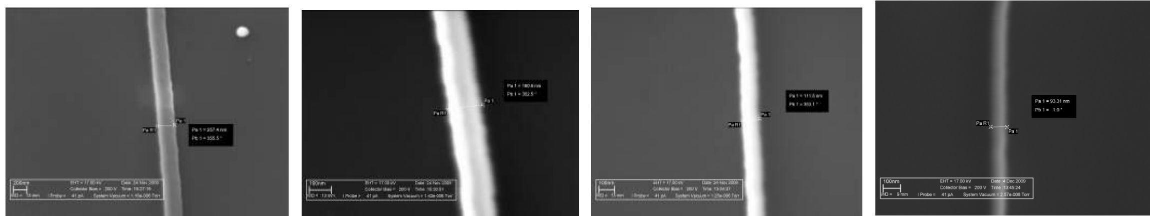


Figure 27: SEM of spacers from sample 1-4 (top-left to right, bottom left to right)

The subsequent step in the process flow is to etch the Si NW using negative PR as a mask which protecting S/D regions. This process step was tested on Si bulk wafers, as shown in Figure 28 below. The opening in the PR represents the channel area. The first SEM image shows twin spacers 20 µm apart and a 5 µm channel length. The second SEM image is a close up image showing the Si surface roughness around the spacer, due to the Si etching in $SF_6$ plasma.

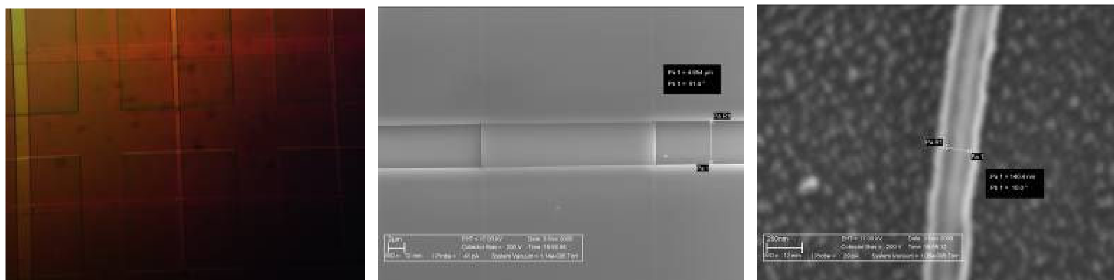


Figure 28: Optical microscope (top left) and SEM image of negative PR mask on S/D regions (top right). Close up image of spacer post Si etch (bottom left).

## **Chapter 3: Image Reversal Photolithography** [29, 30]

As described previously, the image reversal photoresist can be used as a negative or positive resist. In order to reverse the image of the mask pattern on the photoresist pattern, one needs to perform an image reversal bake and a flood exposure after the first mask exposure. The image reversal bake renders the previously exposed resist to be inert to the flood exposure, while the never exposed resist areas remains photosensitive despite the reversal bake. Furthermore, the idea behind the image reversal is to have a resist that can be used for positive and negative photolithography. However, other properties were exploited that were never presented previously, resulting in two provisional patents (VTIP 11-017 and VTIP 11-033).

## 3.1 Simplification of Process flow

The patent ideas emerged from the need to cut down the process flow from the Al source and drain contact patterning. As described previously, the Al contact is deposited on the entire source and drain regions using the only two masks available (active area and channel area masks). The Al contact can be patterned in two different ways using conventional lithography. First, an Al deposition is required in areas outside the channel area using positive lithography and lift-off technique with the channel area mask. Then, the active area mask is used combined with positive lithography to pattern Al by etching the excess Al outside the active area regions. The other way, is to use negative lithography with the active area mask and perform liftoff to deposit Al in the active area region followed by negative lithography to etch Al outside the channel area. The latter method is not preferred since etching in the channel area would be required and would expose the channel area and cause potential damages. The processing steps for the first process flow option are depicted in Figure 29. To avoid Al contamination of plasma chambers, a wet etching method was implemented to etch the excess Al outside of the active area and avoid shorts between devices. The Al is etched using Aqua regia recipe described in the wet etching section: (3 HCl: 1$HNO_3$: 2$H_2O$) because of its high selectivity to Si and $SiO_2$. However, as shown in Figure 30, a large undercut was observed, resulting in a great reduction in the Al covered area on the source and drain regions. Of course, the etch rate can be slowed down by decreasing the temperature to room temperature and by reducing the HCl content in the mix, however, the undercut is so large that switching method would be more encouraging. Thus, another method was explored, the test was to use image reversal (IR) resist and replace the flood exposure after the reversal bake with a second exposure using a mask.

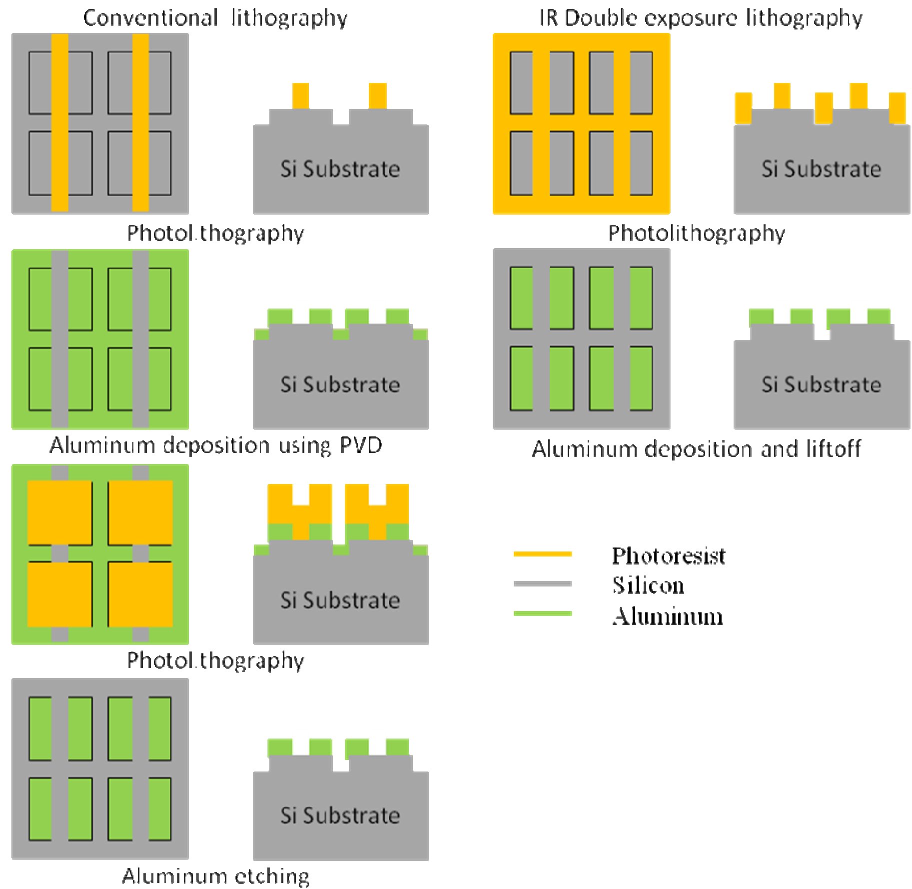



Figure 29: Comparison of process flow using conventional lithography and Image Reversal double exposure lithography

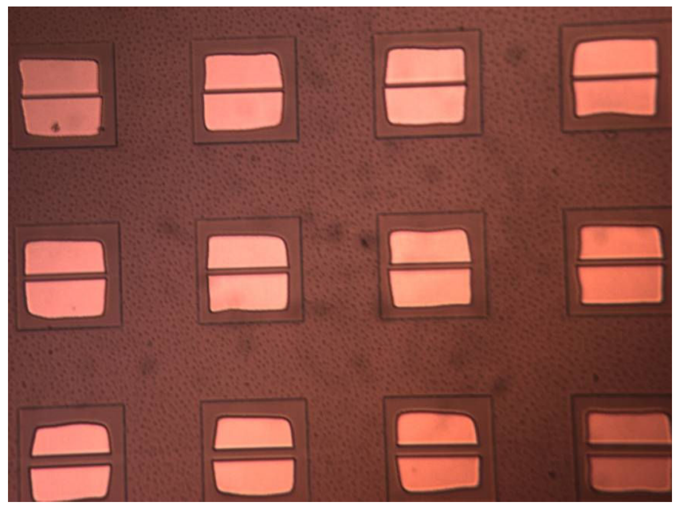


Figure 30: Aluminum undercut on source and drain regions after Aqua regia etch

First the IR resist is exposed using the active area mask, then a reversal bake is performed followed by a second exposure with the channel area mask. Figure 31, shows the IR resist areas and their exposure conditions. As described by the manufacturer, areas exposed

before the reversal bake would be inert to other exposures, areas not exposed are still sensitive to UV light, after the reversal bake. Additionally, it was observed, that areas which are never exposed and those exposed only the first time are insoluble when developed.

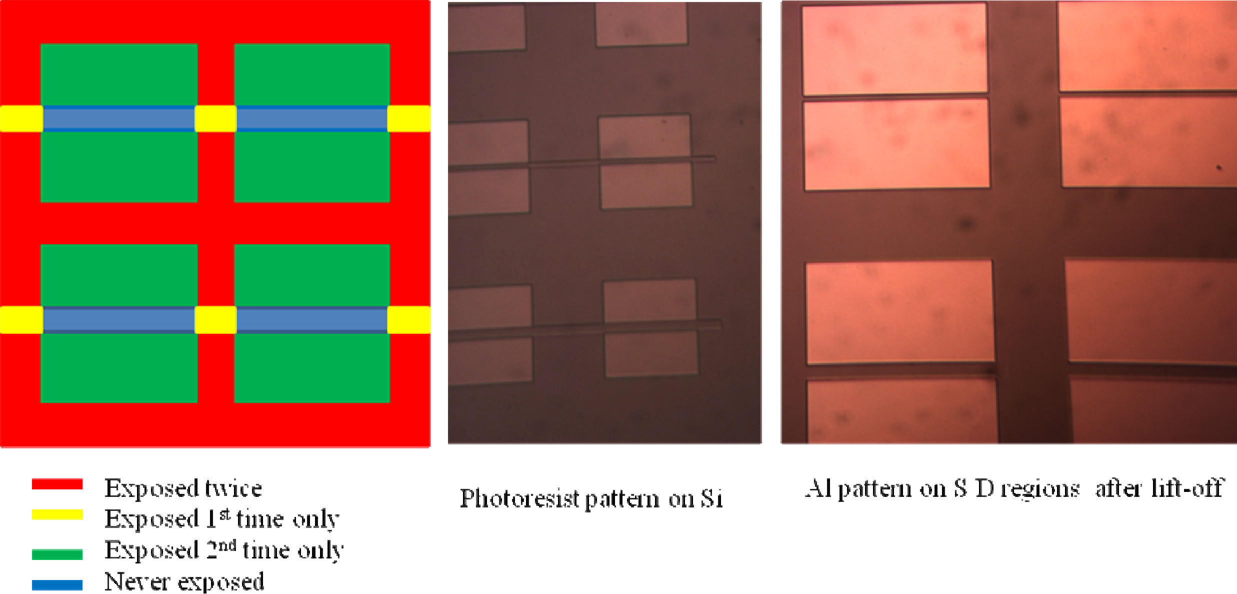



Figure 31: IR lithography properties

The underlying concept of the proposed method is summarized in Figure 31 below. The first mask is shown on the left and the position of the second mask overlaid on the first. The first exposure is done using mask 1 followed by a reversal bake and a second exposure using mask 2. As shown in the Figure 31, the areas never exposed, exposed the first time only, and exposed twice are insoluble when the photoresist is developed. However, the areas that are not exposed the first time but exposed the second time only are soluble in the developer, leaving the final resist pattern shown below.

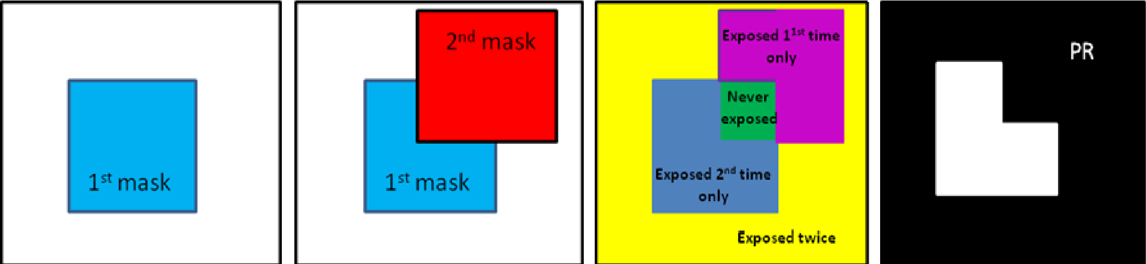



Figure 32: Concept of the double exposure using image reversal resist in one single PR layer

### 3.1.1 Comparison with the conventional double exposure method

Double patterning has emerged as the likely lithography approach to bridge the gap between ArF immersion lithography and EUV. A new patterning method, that combines multiple (double or more) exposures with image reversal in a single photoresist (PR) layer to generate patterns decomposed in separate exposure steps, is proposed. The principle of this approach consists of applying image reversal PR by first exposing the PR with the 1st mask, performing the reversal bake step and exposing the PR the 2nd time with the 2nd mask. In addition, the PR can optionally be developed after the 1st exposure before the reversal bake to generate a different pattern. The final PR pattern is determined by the properties of the image reversal PR: during the final development, the areas of PR that were never exposed, only exposed during the 1st exposure and exposed twice are insoluble. Crucially, only the PR areas exposed during the 2nd exposure (after reversal bake) are soluble. The final PR pattern after development is a composition of areas of insoluble PR segments. This technique has been extended to triple exposures where the first two exposures are conventional double exposures and the 3rd exposure takes place after the reversal bake. In conventional double exposure patterning, the final small pitch pattern is processed using two separate lithography and etching steps with a hard mask such that only larger pitch patterns are exposed . The proposed method lowers the cost-of-ownership (CoO) of double exposure significantly, since in lieu of two PR layers it uses only one PR layer. Using simple "primitive" mask patterns for the 1st and 2nd (and 3rd) exposures, the method produces complex patterns, that are impossible to obtain in a single PR layer with the double exposure technique. This approach mitigates also the diffraction distortion effects, especially for inside corners present in "+" "L" and "T" shaped pattern structures. In case of triple exposure, the diffraction rounding of the outside corners can be mitigated as well. The proposed method lends itself to a generation of composite masks by overlaying aerial images of simple "primitive" masks in the same PR layer, thus simplifying the mask design. The image reversal technique as the final step can be targeted for the resolution of the smallest features taking advantage of the negative photoresist slopes. This approach can be retrofitted into existing older generation photolithography, obviating in many cases the use of optical proximity corrections (or using OPC for further resolution enhancements) and thus boosting the yields significantly. The method shares the requirement of tight

overlay accuracy approaching now 3 nm [31] with extant double exposure methods. This technique is attractive particularly for NAND, NOR, DRAM, and SRAM cell with highly regular lithography patterns. Examples for photolithography process flow reduction, mitigation of diffraction effects, and mask decomposition are provided. The CoO comparison between the proposed vs the conventional double exposure/patterning method is also discussed in details.

In Figure 33 the proposed method is compared with the conventional double exposure technique [32]. As can be seen, compared with single exposure approach there are only two additional steps in the single PR layer patterning: PR image reversal bake and 2$^{nd}$ exposure.

Figure 33: a. process flow for a conventional double exposure (left) b. significantly reduced process flow according to the proposed method (right).

Using our method, a hard mask is unnecessary and different etching steps are also eliminated, reducing the steps to one lithography step and etching the substrate. Thus the cost-of-ownership of the proposed double exposure method compared with the conventional double exposure technique (see Figure 33a) is significantly lowered. By the same token the throughput is significantly increased. Effectively, owing to the image reversal two hard mask patterning steps with two separate PR layers are created in a single physical PR layer.

### 3.1.2 Lithography process reduction and simplification

This technique was implemented to pattern nanoribbon structures on SOI substrates with 88 nm thick Si using two masks (active area mask and channel area masks) designed for novel MOSFET structures. Figure 34 illustrates a comparison between the process flow where

conventional lithography is used and the process flow using our lithography technique. In the conventional lithography, the following steps are required: 1. Pattern Si mesa-island. 2. Deposit Silicon oxide. 3. Pattern oxide using channel area mask. 4. Etch oxide. 5. Perform lithography using channel area mask and negative resist. 6. Etch Silicon. 7. Remove oxide.

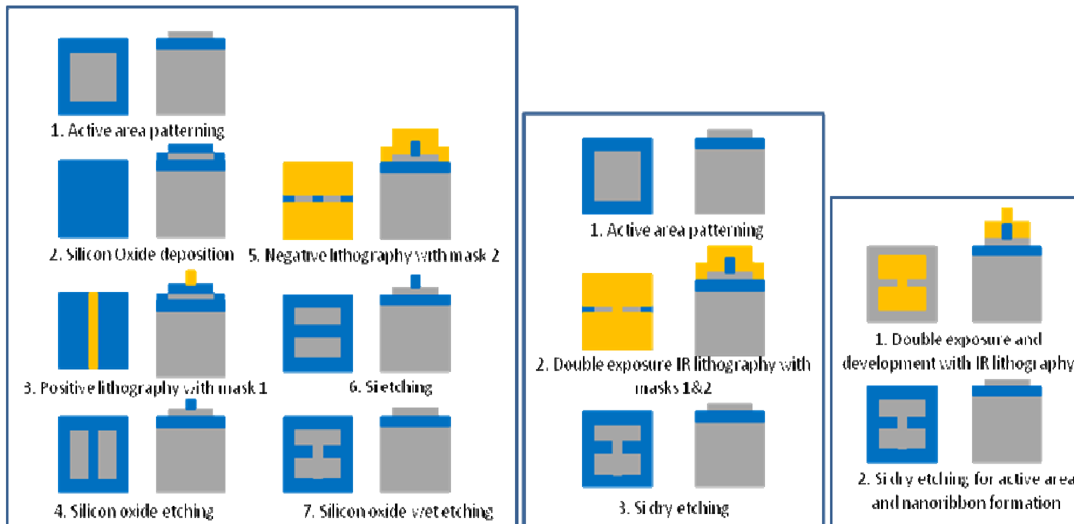



Figure 34: Process flow to produce an H-shaped structure on thin SOI Si mesa islands: left -conventional process flow, center – process flow using the proposed method with two exposures, right – process flow using the proposed method with three exposures.

Using our approach with two exposures, the steps are as followed: 1. Pattern Si mesa-island. 2. Perform our lithography approach using the channel area mask twice while rotating it by 90° in the second exposure with a reversal bake in between exposures. 3. Etch Silicon. In addition, our technique can also be used with triple exposures. First the active area mask is used to expose and develop the image reversal photoresist, followed by a 2nd exposure with the channel area mask, a reversal bake and a 3$^{rd}$ exposure with the channel area mask rotated by 90° before developing

Figure 35a shows the image reversal resist pattern after development. Two exposures with the channel area mask were used to generate the pattern in Figure 35a. Figure 35b shows the silicon on buried oxide (BOX) after etching of the nanoribbon. Finally, Figure 35c illustrates the case where three exposures were used with the resist developed after a first exposure with the active area mask followed by two other exposures with the channel area mask and a reversal bake in between.

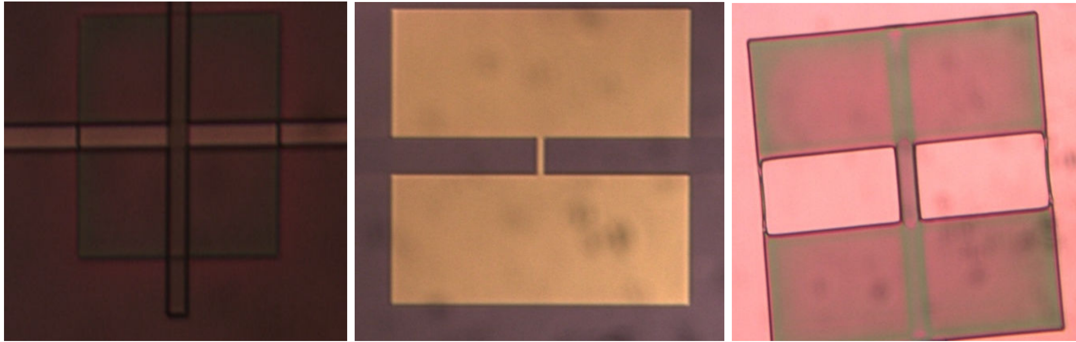


Figure 35: a. PR pattern after two exposures with channel area mask. b. Si Nanoribbon pattern on BOX. c. PR pattern after three exposures with active area and channel area masks

### 3.1.3 Example of pattern generation from the same mask

The next example in Figure 36 shows the PR patterns that were obtained after shifting the active area mask in different directions. "L" and "+" soluble patterns were obtained in the PR after two exposures with a reversal bake in between.

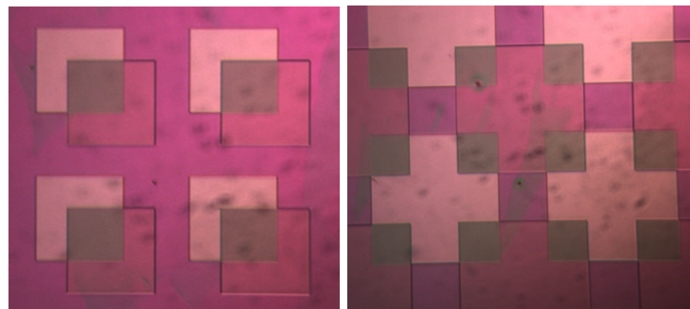


Figure 36: PR pattern after two exposures with active area mask shifted in different **directions.**

## 3.2 Mitigation of diffraction effects (corner rounding)

The key to preventing the diffraction distortion effects is to avoid  the line segments in close proximity to one another that are not elements of the same straight line. A classical example are the adjacent arms of a cross structure shown in Figure 36a. The diffraction interaction between the line segments perpendicular to one another creates a rounding effect such that at small enough critical dimensions, the cross can no longer be resolved. The advantage of the proposed method is that at a respective exposure there are no line segments perpendicular to one another belonging to the respective arms of the cross. Therefore, in the proposed method using the masks shown in Figure 36b will result in perfectly resolved inside corners as shown in Figure 37c. The outside corners will suffer the same pull-back and rounding as in the conventional techniques.

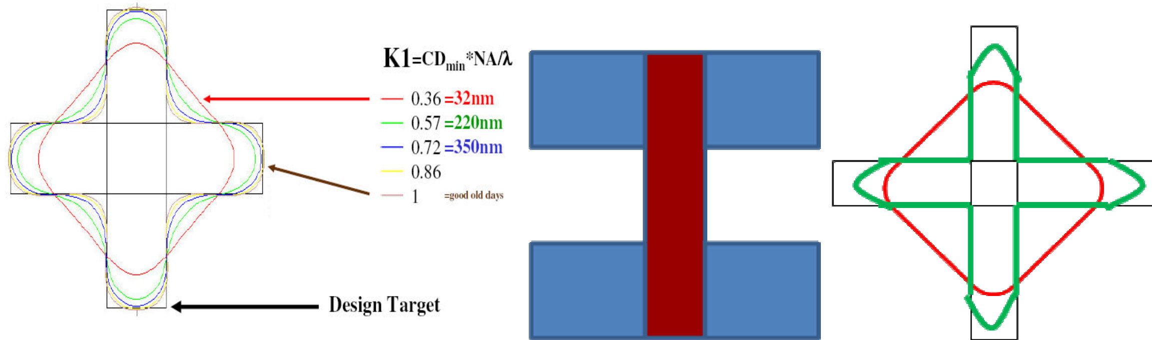



Figure 37: a. Distortion in image patterning with decreasing optical wavelength. b. Dual mask (there are several options) suggested to generate cross pattern using image reversal. c. Expected PR pattern with our method in green with inside corners preserved; red line indicates the resolution limit of the conventional lithography (see Figure 6a).

The outside corners at the ends of arms of the cross can be resolved at the expense of the triple exposure technique in conjunction with image reversal. This case is being discussed in the next paragraph. Another example of avoiding the rounding of inside corners of trenches patterned in the PR layer is shown in Figure 37. The PR is exposed using the 1st mask, followed by a reversal bake and an exposure with the 2nd mask. After developing the PR, the pattern in Figure 37c is obtained where the corners are never directly exposed but the pattern is broken down in two exposures in the same resist layer.

### 3.2.1 Example of triple exposure with image reversal

With triple exposure and image reversal a cross structure can be resolved with great fidelity, i.e. both the inside and outside corners are well resolved in a single photoresist layer. The three different masks that are used to that purpose are shown in Figure 38a, b, and c. Clearly adjacent line segments perpendicular to each other never are subject to diffraction interaction. First the resist is exposed using mask 1 and developed (Figure 39a); the same pattern is exposed again using the second mask followed by a reversal bake and a third exposure. After the last development, the crosses are generated and since simple mask structures were overlaid in such a manner to avoid corners being exposed, the final resist pattern would replicate the desired shape. The intermediary results and the final result are shown in Figure 40.

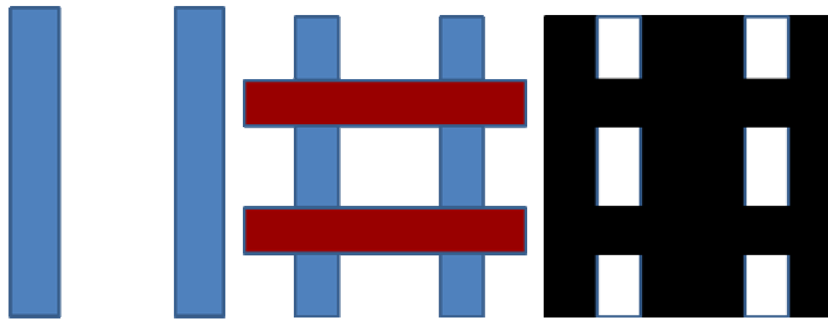


Figure 38: Dual mask suggested to pattern structures shown on right and avoid rounding of corners: a. mask 1 (left). b. Mask 2 overlaid on mask 1 (mid). c. PR pattern after development (right)

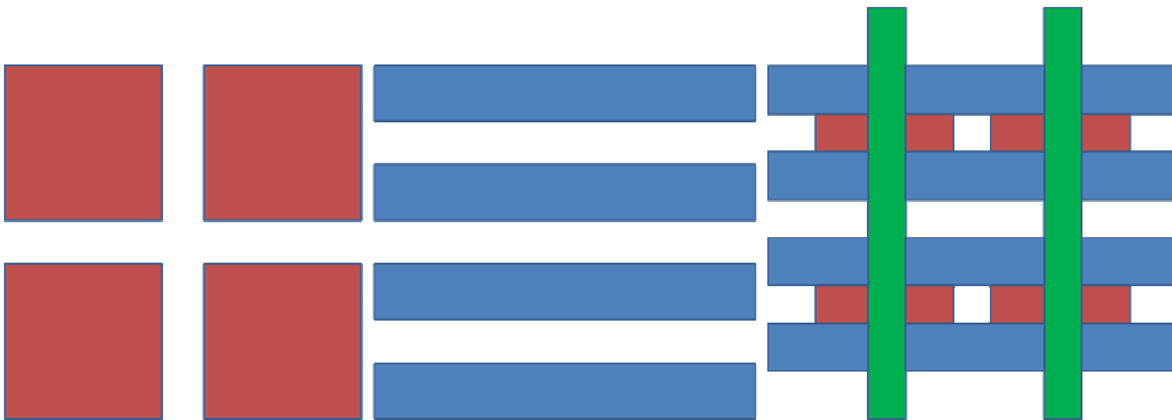
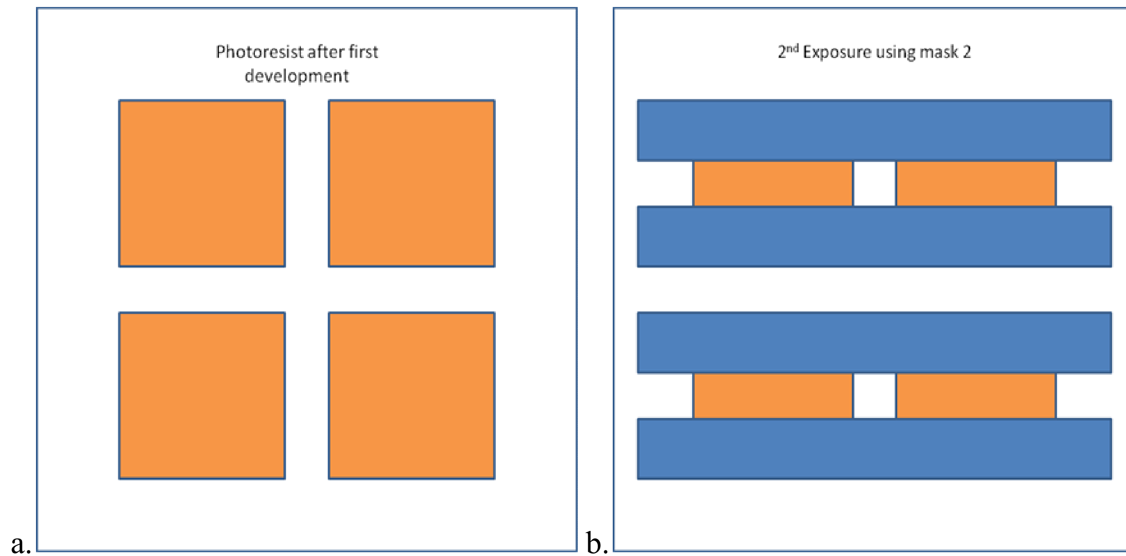


Figure 39: a. Mask 1 (left). b. Mask 2 (middle). c. Mask 3 overlaid on mask 1 and 2 (right).



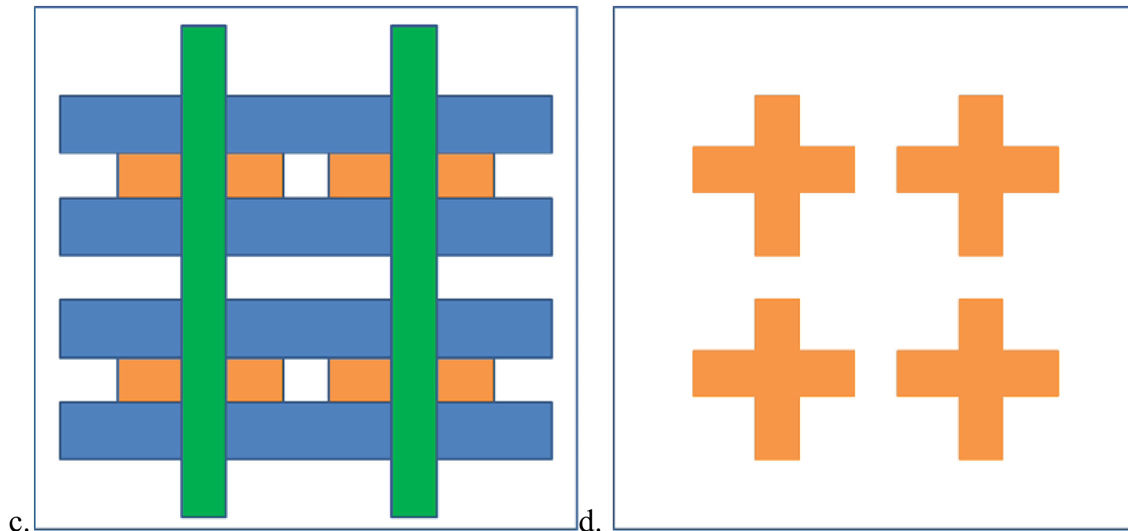



Figure 40: a. Image resist pattern after first exposure with mask 1. b. Developed pattern exposed 2nd time with mask 2 followed by a reversal bake. c. Pattern exposed 3rd time with mask 3. d. Image reversal pattern after final development.

The above examples illustrate two important aspects of the proposed method. A virtual composite mask can be decomposed in simple "primitive" masks that are actually used during the respective exposures. In many cases the mask decomposition is not unique and the actual choice will be driven by process parameters and process stability. The mask decomposition should be also driven by the requirement to avoid inside corners whenever possible in the design of "primitive" masks. At the same time, this objective diffraction distortions and allows near perfect resolution of structures far below the resolution of the final structure itself at the prevailing photolithography generation. Basically a CD structure can be resolved if the technology allows resolution of CD parallel lines. The issue of the resolution hinges therefore on the overlay precision. If the overlay precision is 3nm [2], no structures with features smaller than 3-5 nm will be resolvable.

### 3.3 Construction of optimum mask (mask algorithm) [33]

Additionally, an algorithm to perform a layout based on the principles of double exposure with IR resist was created. This patent disclosure describes a method and algorithm of how to decompose the original mask in two overlaid masks in the optimum way to assure the best pattern resolution and printability. The mask decomposition method applies to the lithography technology disclosed on patent disclosure VTIP 11-017.

This particular algorithm applies to the case when the photoresist (PR) is not developed after the first exposure. A similar algorithm can be established for the case when PR is being developed after the first exposure. Here the algorithm is shown in some detail to illustrate the principles on which the algorithms are based. First the layout should be done in the usual manner by generating the final desired patterns for positive PR lithography. Then, by applying the proposed algorithm, the mask can be decomposed in two simple mask patterns to generate the equivalent final resist pattern with image reversal resist using double exposure.

The resist properties are that: areas never exposed, exposed twice and exposed the 1$^{st}$ time only are insoluble, areas exposed the 2$^{nd}$ time only are soluble when developed. For resist areas where solubility is desired, the resist should be exposed only after the reversal bake. Thus, those areas of interest should be opaque on mask 1 and transparent in mask 2.

For areas that are insoluble, multiple mask combinations are available, the area of interest in: mask 1 and mask 2 opaque (PR never exposed), mask 1 and mask 2 transparent (PR exposed twice), mask 1 transparent and mask 2 opaque (exposed 1$^{st}$ time only). In result, the mask design becomes more flexible for optimum printability.

The problem of the mask decomposition is the following: There are many combinations of mask 1 and mask 2 layouts which lead to the desired overlay pattern. In a particular case a lithography expert would be able to select the best mask combination given his insight of how lithography works. However, in complicated layouts a human intervention would be too time consuming, not cost-effective, and error-prone. Therefore there is a need for a computer algorithm which makes sure that the optimum mask combination has been selected. For the selection of mask combinations different target functions can be chosen and different selection criteria. Here we propose an algorithm that selects a mask combination that ensures the optimum resolution and printability of the final structure that needs to appear on the wafer.

### 3.3.1 Example

In this example (Figure 41), the decomposition process of the mask layout is being depicted. The desired resist pattern is shown in blue; the red and green patterns are the possible mask layout for layer 1 and layer 2 respectively. In conventional lithography, the

areas in blue on the mask would be opaque while the outside areas would be transparent. The first rule for mask decomposition is that areas that are transparent on original (conventional) mask pattern must be opaque on mask 1 layout and transparent on mask 2 layout of the IR lithography method. The second decomposition rule is that for areas that are opaque on initial mask pattern, three different combinations are allowable for each block on the superposed mask layers: i) opaque-opaque, ii) transparent-opaque, iii) transparent-transparent (specification 1st mask – 2nd mask). As shown in Figure 41, this leads to a large number of possible mask combinations. Therefore the algorithm has to be complemented by selection rules.

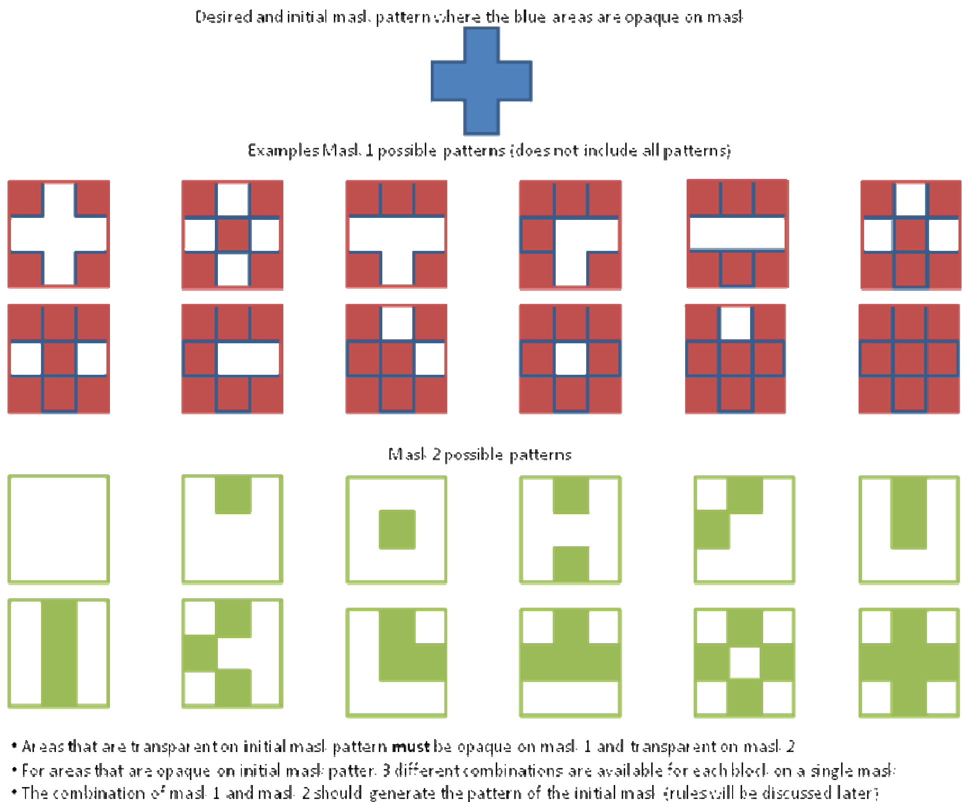



Figure 41: Example showing the desired mask pattern for conventional lithography and the decomposition of mask layers for IR lithography method.

In the initial mask pattern, the following assumption can be made: blocks that are opaque will be assigned the value 0 and the transparent ones the value 1. If mask layer 1 is called logic variable A, mask layer 2 is called logic variable B, and the outcome of the logic operation should correspond to the initial mask C then the logic operation for the mask decomposition is:

$$\overline{A} \cdot B = C \qquad (9)$$

| MASK | | PR | |
|---|---|---|---|
| Opaque | Transparent | Insoluble | Soluble |
| 0 | 1 | 0 | 1 |

| Mask 1 (A) | Mask 2 (B) | Initial mask (C) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

In Figure 42, the possible patterns for layout 1 and layout 2 that could individually satisfy the design rules are presented. The criteria are that the areas of resist that should be soluble should be opaque in layer 1 and transparent in layer 2. For the outside areas, any block combination is allowed; some of the patterns are shown for layer 1 and layer 2. Next, the combination of layer 1 and layer 2 that meet the first design rule, the logic operation in equation (9), must be selected. Any combination eliminated would result in a pattern different than the desired “cross” pattern.

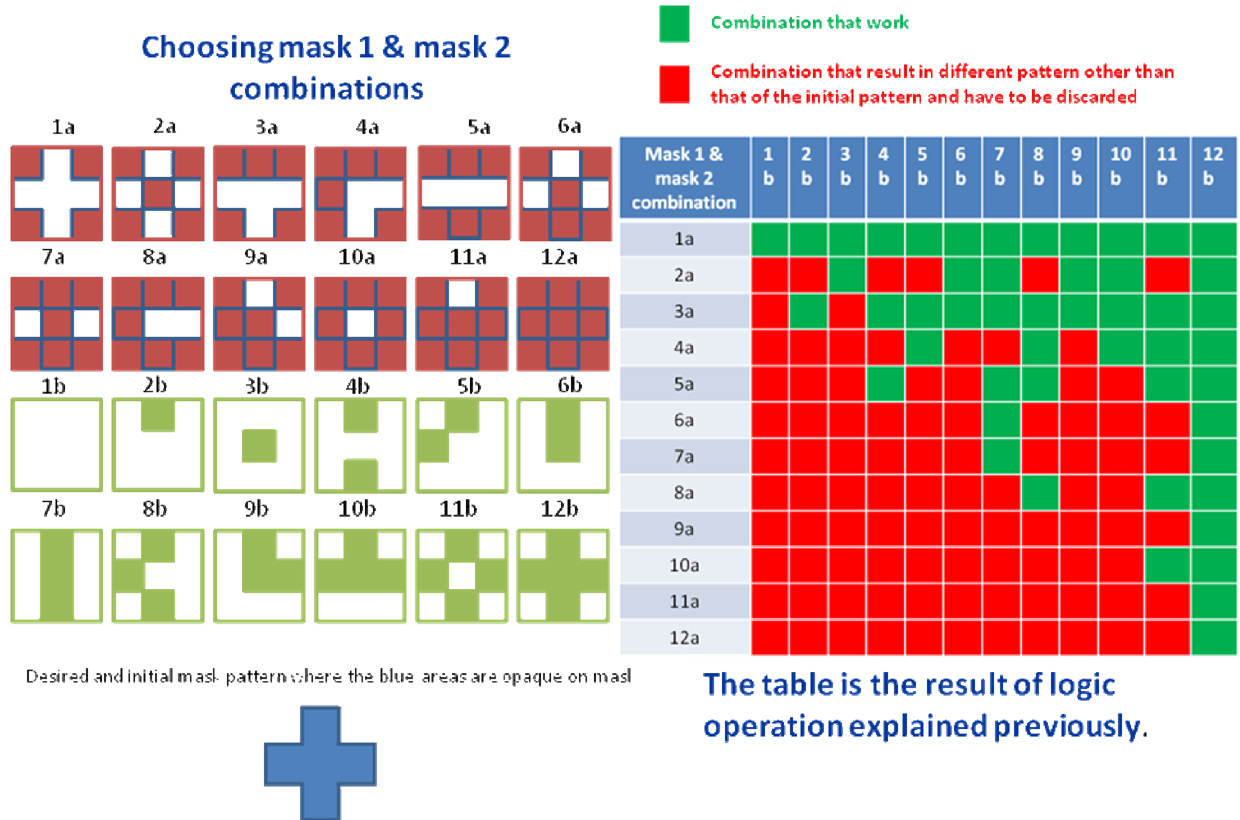



Figure 42: Possible patterns for mask 1 & 2 layouts and selection of combinations that generate desired pattern.

After picking all the combinations of mask 1 and mask 2 equivalent to the initial mask pattern, the best combination(s) should be selected. The best combinations are the ones that contain the least inside and outside corners together to avoid pattern distortion during exposure. The corners are counted in a specific manner. From each block, if the two adjacent blocks have the same values and opposite to the value of the corner, then that case will be counted as a corner. See Figures below. Thus, the number of corners is counted from each block and added all together. Figure 43 shows how corners are counted from each block. The minimum number of corners counted on each mask layer is 1 since the purpose is to minimize the number of corners in both mask layers. The number of corners is counted by multiplying the number of corners in layer 1 and layer 2. Thus, the minimum number of corners in the layer has to be 1 to avoid the counting to equate to 0 and lead to errors.

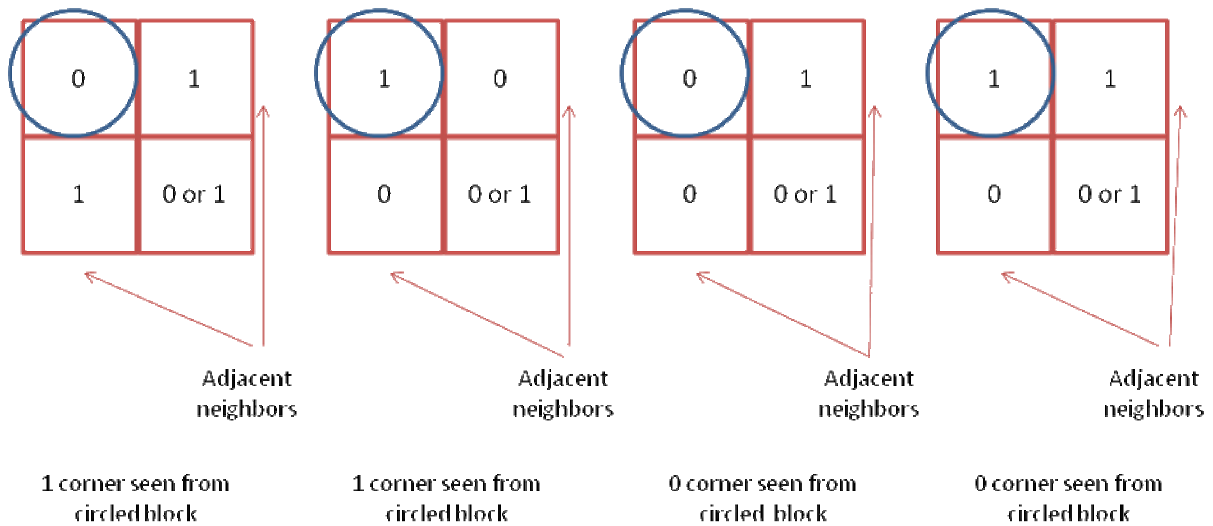
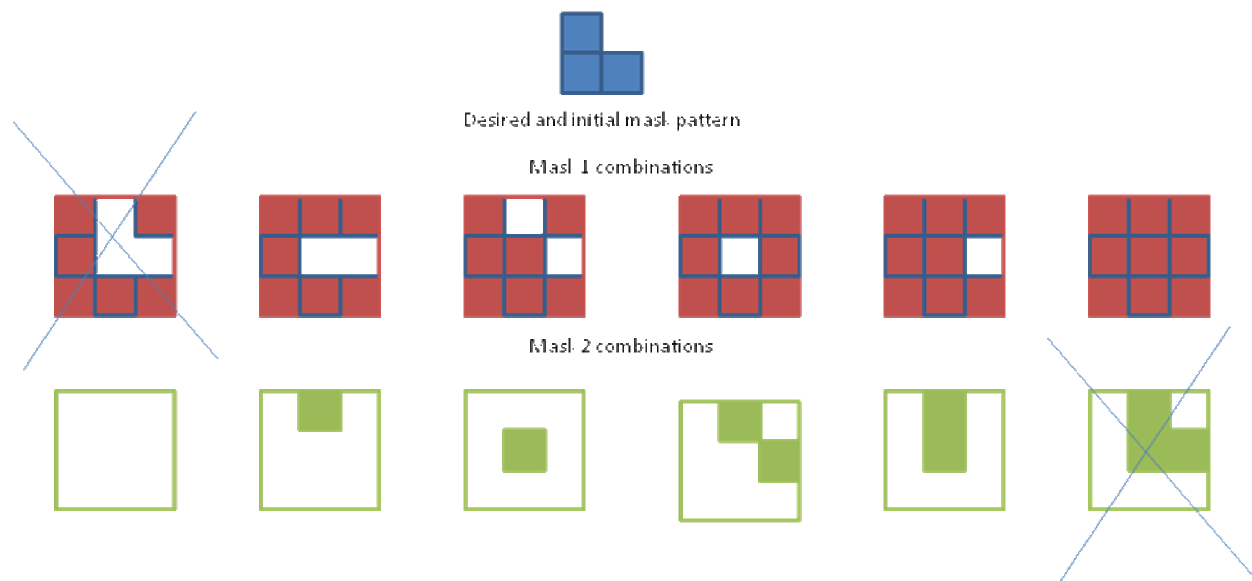



Figure 43: Counting of corners that would cause distortion of resist patterns

As a figure of Merit FoM= (corners from mask 1 + 1) * (corners from mask 2 + 1)
Best combination of mask 1 and mask 2 will be the one with smallest FoM or FoM=min. Also, mask 1 and mask 2 patterns that are the same patterns (or exact opposite) as the initial mask (designed for positive lithography) should be omitted. See example below in Figure 44.

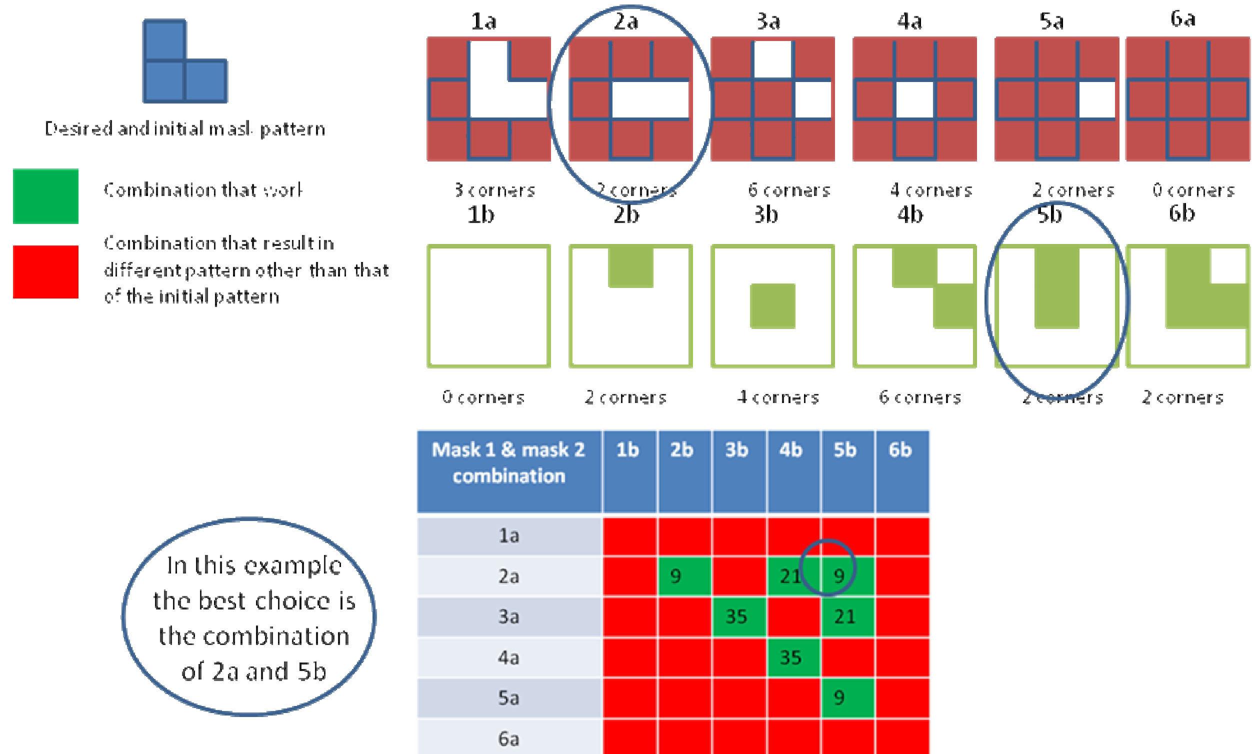



**Excluded masks are just the original masks and would not lead to mask decomposition.**

Figure 44: Mask patterns that are exact or opposite replicas of initial mask are omitted.

From Figure 44, after counting the number of corners and eliminated mask replicas, only three mask combinations (out of 36) with min (FoM) = 9 will remain. Thus, the best combination of layer 1 and layer 2 that reduces pattern distortion needs to be picked. The

optimum mask combination is selected according to the criteria of largest continuous rectangles. The best final choice of mask 1 and mask 2 contain areas that form the largest rectangle or square that is opaque or transparent, as shown in Figure 45.




| Mask 1 & mask 2 combination | 1b | 2b | 3b | 4b | 5b | 6b |
|---|---|---|---|---|---|---|
| 1a | | | | | | |
| 2a | | 9 | | 21 | 9 | |
| 3a | | | 35 | | 21 | |
| 4a | | | | 35 | | |
| 5a | | | | | 9 | |
| 6a | | | | | | |

Figure 45: Ultimate criteria for selection of mask combination

Thus, the largest number of consecutive blocks which together form a rectangle or a square will determine the ultimate the mask layout for double exposure using IR photoresist.

In the example from Figure 42, it can be shown that for the cross pattern, the corner-counting method presented before leads to a unique and optimal choice of a mask combination. If the condition FoM=min gives a unique optimum mask decomposition, the rule of largest contiguous rectangles does not have to be invoked. The optimum mask combination in Figure 42 is 5a and 7b, since FoM for this combination is FoM=2 (=minimum). There is only one mask combination with FoM=2.

All the possible patterns for mask 1 and all the possible patterns for mask 2 have to be generated first by breaking the initial mask pattern into blocks. In this case, the only rule is that for the transparent areas in the initial mask, the same areas in mask 1 should be opaque and transparent in mask 2

The combinations of mask 1 and mask 2 that will not generate the same pattern as the initial mask are eliminated using the following logic AND operation where bar over mask1 denotes the logic complement: $(\overline{mask1})\cdot(mask\,2)=(initial\;\;mask)$

All the combinations that don't obey this rule are eliminated. Also, any mask that replicates the exact pattern or the exact opposite as the initial mask is discarded. Then, the combination(s) that have the least number of total corners (= [corners from mask 1 + 1] *[ corners from mask 2 + 1]) are selected. Often this leads to a unique solution. Finally, masks with largest opaque/transparent rectangles or squares are preferred over not contiguous rectangles/squares.

# Chapter 4: Experimental Results and Discussions

## 4.1 SIMS profiles

The SIMS profile of Phosphorus in bulk Silicon was obtained after performing a solid source diffusion at 1000 °C for one hour. This data provides the profile of phosphorus for resistance calculation and also the junction depth where the phosphorus concentration is equal to the background boron doping concentration. Thus, the boron background doping concentration can also be determined from this curve shown in Figure 46. As expected, three regions can be observed in the phosphorus profile: the high concentration region ($>10^{20}$ cm$^{-3}$), the kink region and the tail region. In the high concentration region, the concentration of phosphorus is practically constant. In the kink region, the phosphorus ions/atoms disassociate with the charged Si vacancies. Finally, most of the diffusion occurs in the tail region which is the low concentration region. In the SIMS plot, the curve saturates to a value which is approximately $4\times10^{15}$ cm$^{-3}$ and representative of the junction depth concentration where the phosphorus and boron concentrations are equal. The measurements become noisy around that concentration since the detection limits of the equipment is closed to being reached. This profile is used in modeling the diffusion in both bulk and nanomembrane structures.

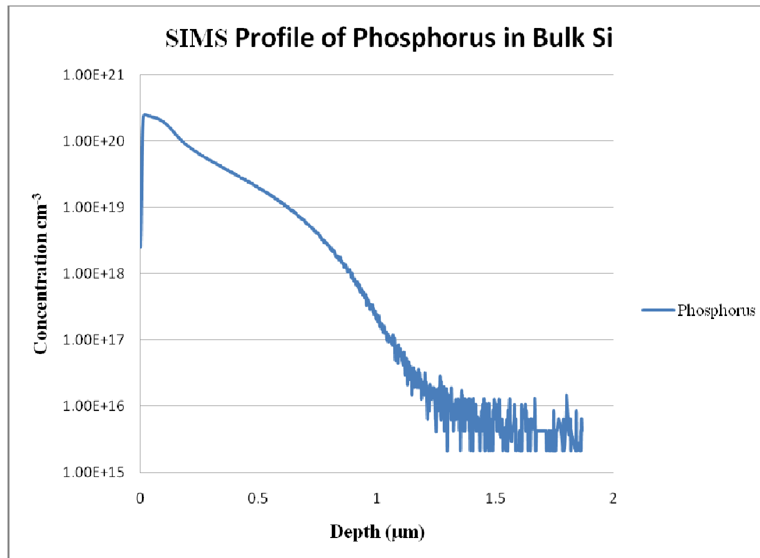


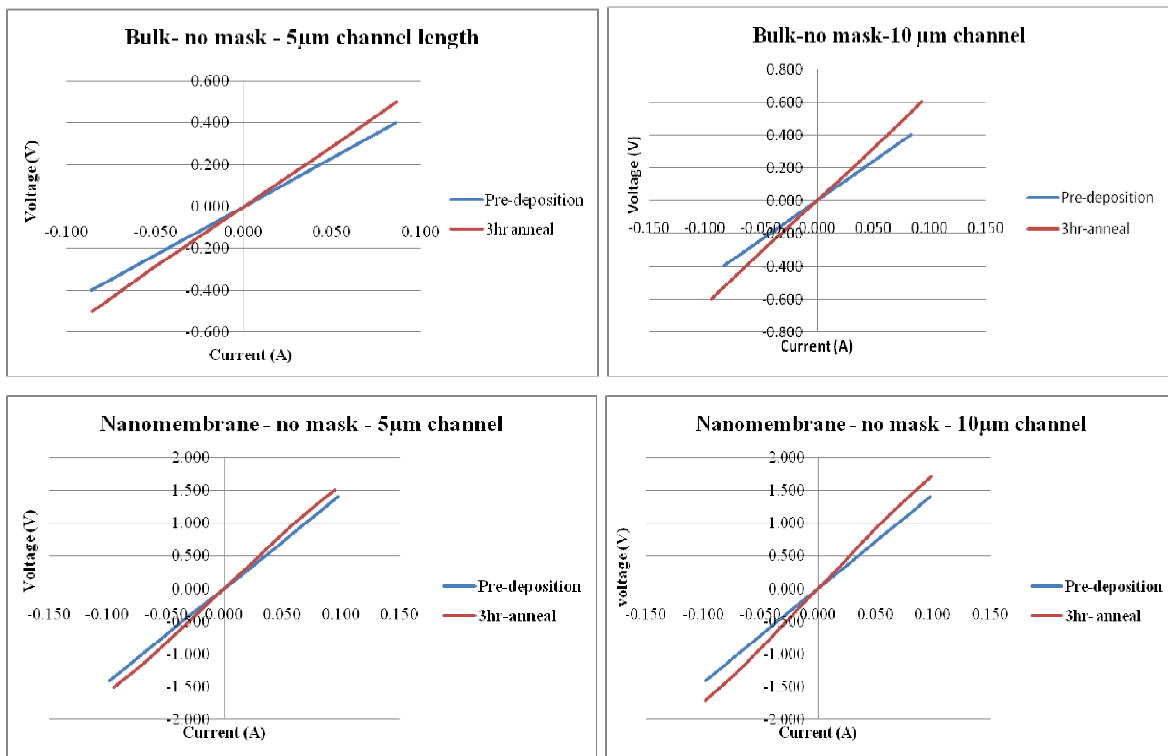

Figure 46: Phosphorus profile in Bulk Si

## 4.2 Phosphorus (I-V)

During the predeposition step, the source, drain and channel regions are doped except for the samples on which oxide diffusion barrier is deposited on the channel area. The uniformly doped samples are used to monitor the in-depth diffusion in the sample since the entire region is exposed to the furnace ambient during the diffusion. It also is a good method of determining how the lateral diffusion is progressing in the channel since it represents the case where the phosphorus dopants penetrate the entire channel region. The lateral diffusion is evaluated on samples on which the oxide is deposited on the channel region. Thus, I-V measurements are collected after the pre-deposition step and after an annealing period of 3hr. As the dopants progress in the channel, the channel resistance is expected to drop resulting in an increase of current. All samples are doped and annealed simultaneously in the furnace at a temperature of 1000 °C in $N_2$ ambient.

The active area is a square mesa island of 400 µm and the channel length varies from structure to structure between 5, 10, 20, 50, 100 µm. Although the diffusion experiment focuses on the shortest channel length of 5 µm, measurements collected from structures with longer channels allows extracting additional data and understanding how the contact length impacts the measurement. The source and drain Al contacts are deposited on the entire source and drain areas. For the uniformly phosphorus samples, the I-V characterization was done on all channel length after the pre-deposition and the 3 hr

annealing, Figure 47. For the bulk, nanomembrane and nanoribbon structures, the resistance of the channel increases after the 3 hr annealing. However, the nanowire resistance decreases after the annealing. In fact, the resistance increasing is expected since the channel, source and drain are all exposed to the furnace ambient, although the dominant gas is $N_2$ the carrier gas, some $O_2$ infiltrates the furnace and thus some oxidation occurs during the annealing. The silicon dioxide grows on the phosphorus doped area and thus consumes about 8 nm of doped Si. In the nanowire structure, the dimensions of the structure is extremely small, thus some clustering is expected to occur resulting in the electrical deactivation of the phosphorus. Thus, the annealing step allows diffusion and activation of the phosphorus atoms specially that the oxide growth incorporates interstitial point defects which in a significant amount in such a small structure and promote the diffusion of phosphorus. Furthermore, the I-V curves in the nanowire showed some non-linearities that might be due to current crowding effect since the current lines squeeze from a 400 × 200 µm source area to a 90-130 nm diameter channel structure and spread back to a drain area.



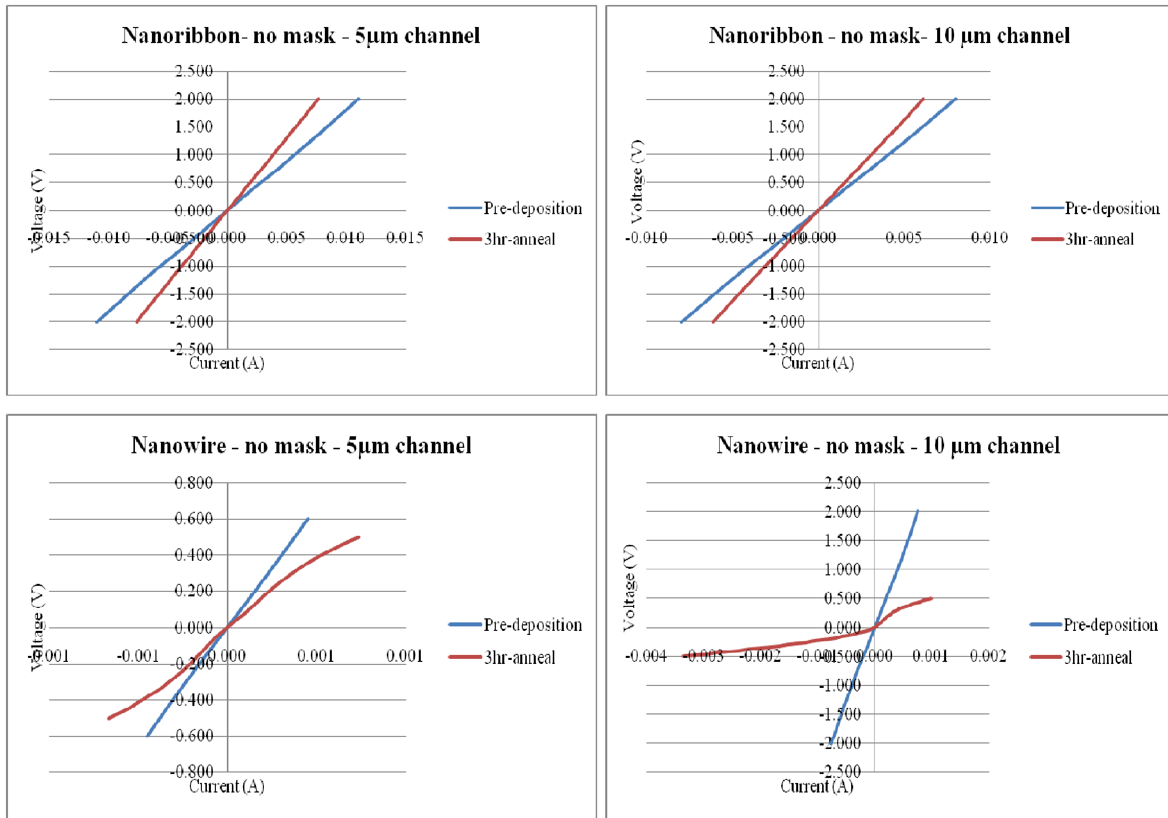



Figure 47: I-V measurements for phosphorus doped source, drain and channel regions.

Additionally, I-V measurements were collected on samples where an oxide diffusion barrier is masking the channel region, preventing phosphorus doping from penetrating the channel area. I-V measurements were taken after the pre-deposition step where the source and drain regions are doped and after the 3hr annealing period. In this case, the resistance of the channel decreases after the annealing of the bulk, nanomembrane and nanoribbon samples. As seen in Figure 48, more voltage is required to obtain the same current before annealing. Since the channel is mask, it is not exposed to the ambient, only the source and drain regions are exposed to the ambient. Furthermore, 800 nm of oxide mask is thick enough to mask against dopant diffusion specially that the diffusion of phosphorus in oxide is extremely small and under constant source diffusion, this thickness would still be an efficient mask. However, for the nanowire structures, the resistance increases after the annealing. The results become more complex to interpret in this case but it does point to a difference in the junction behavior. It can be observed from the IV curves, that non-linearities were present in the I-V before the annealing, which seem to be annihilated after

the diffusion. The change in resistance for each of the structure is calculated:

$$\frac{\Delta R}{R} = \frac{R_1 - R_2}{R_1}$$

where $R_1$ is the resistance measured after the pre-deposition step and $R_2$ is the resistance after the 3hr annealing step. As observed in Table 1, the change in resistance ΔR/R is 0.625 for bulk Si, 0.43 for the nanomembrane structure, 0.087 for the nanoribbon and negative for the nanowire. The change in resistance decreases as the structure dimension decreases. Furthermore, these results suggest that the lateral diffusion decreases in lower dimensional structures because of the surface to volume ratio change and the segregation effects on nanostructures. These results will be discussed in more details.

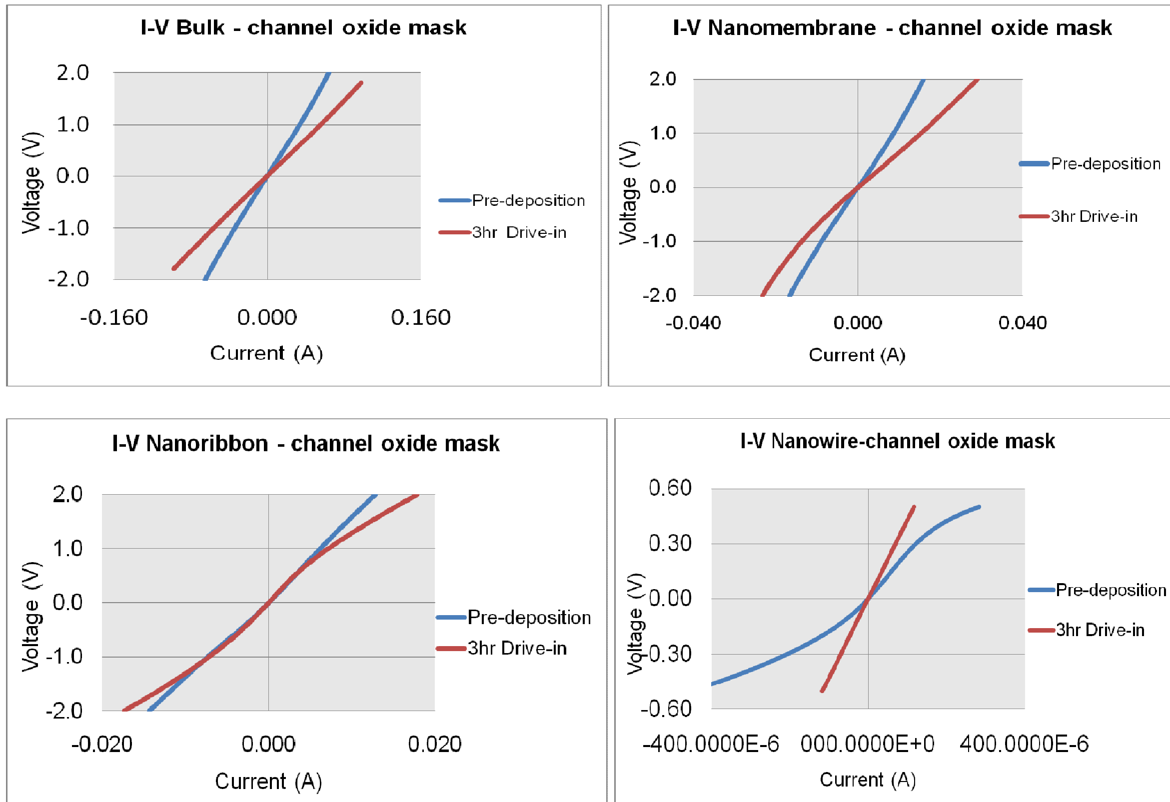


Figure 48: I-V characteristics of bulk and nanostructures with oxide mask and channel length of 5 µm

Table 5: Resistance change after 3hr anneal versus the structure

| Structure | ΔR/R |
|---|---|
| Bulk | 0.625 |
| Nanomembrane | 0.43 |
| Nanoribbon | 0.087 |
| Nanowire | < 0 |

## 4.3 Discussion of Results

### 4.3.1 Based resistance

The resistance is calculated as $R = \frac{\rho L}{A}$, where ρ is the resistivity of the material in Ω-cm, L is the length in cm and A is the cross sectional area $cm^2$. The resistivity of the material, Si in this case, is the inverse of the conductivity $\sigma = ne\mu_n + pe\mu_p$, where n and p are the electron and hole concentrations respectively, e is the electron charge 1.6E-19 C and $\mu_n$ and $\mu_p$ are the electron and hole mobilities respectively. The mobility μ is proportional to the scattering time of the carrier, which is the time between two successive collision events: $\mu = \frac{e\tau}{m^*}$. From the band structure of Si, the conduction band has 6 minimas near the X-point of the Brillouin zone, while the top of the valence band is at the Γ point, making Si an indirect bandgap material. The surfaces of equal energy in the band structure form an ellipsoid resulting in two effective masses: longitudinal mass $m_l$ and transverse mass $m_t$ for the electron. For the hole, the effective masses are that of the light hole, the heavy hole and the split off band. An effective mass for the density of states in the conduction band can be obtained as an average which is $0.36m_0$ and $0.81m_0$ for the electron and the hole respectively where $m_0$ is the free electron mass [34].

The scattering time is calculated using the Matthiessen's rule:

$$\frac{1}{\tau} = \sum_i \frac{1}{\tau_i} \quad (10)$$

where i is the scattering mechanism. The scattering time τ depends on different scattering mechanisms: local impurity scattering, surface roughness scattering, acoustic phonon scattering and coulomb scattering [35]. Thus, in this case, the scattering mechanism with the lowest scattering time will dominate the effective scattering time. From [35], the effective mobility is derived from the following equation:

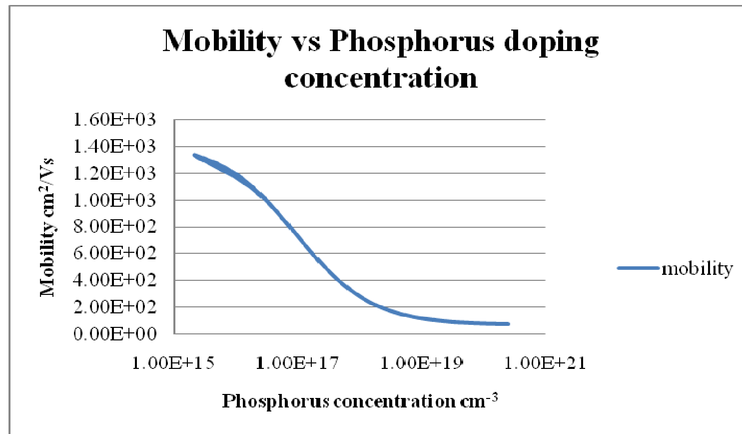
$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{coulomb}} \quad (11)$$

The acoustic phonon mobility is $\mu_{ac} = \frac{qh^3 \rho \mu_I}{m^* m_\mu Z_A^2 k_B T}$ (12)

where h is the Dirac constant, $\rho$ the area mass density of silicon, $\mu_I$ the sound velocity, $m^*$ the effective mass $m_\mu$ the mobility mass, $Z_A$ the deformation potential and $k_B$ Boltzmann constant. The bulk mobility $\mu_b$ can be obtained for holes and electrons by using

$$\mu_b = \mu_0 + \frac{\mu_{max} - \mu_0}{1 + (\frac{N}{C_r})^\alpha} - \frac{\mu_I}{1 + (\frac{C_s}{N})^\beta} \text{ [36]} \quad (13)$$

where $\mu_0$ the minimum mobility is 68.5 and 44.9 $cm^2/Vs$ respectively for electrons (phosphorus source) and holes (boron source), $\mu_{max}$ is 1417 $cm^2/Vs$ for electrons and 470.5 $cm^2/Vs$ for holes, $C_r$ and $C_s$ are fitting parameters, $\alpha$, $\beta$, $\mu_I$ are model parameters. The mobility limited by surface roughness $\mu_{sr}$ and coulomb scattering $\mu_{coulomb}$ are ignored in this case since $\mu_{sr}$ is inversely proportional to the transverse electric field and $\mu_{coulomb}$ is inversely proportional to the fixed oxide charge which are both present only in the presence of a gate and gate bias, since our structures are not transistors, these mobility values will tend to infinity and thus will not affect the effective mobility since the transverse field and the oxide charged traps are equal 0. Using equation (13) and the SIMS profile shown in Figure 46, the mobility vs concentration was plotted for Phosphorus doped Si in Figure 49. The mobility in bulk Si drops with increasing doping concentration because of impurity scattering.



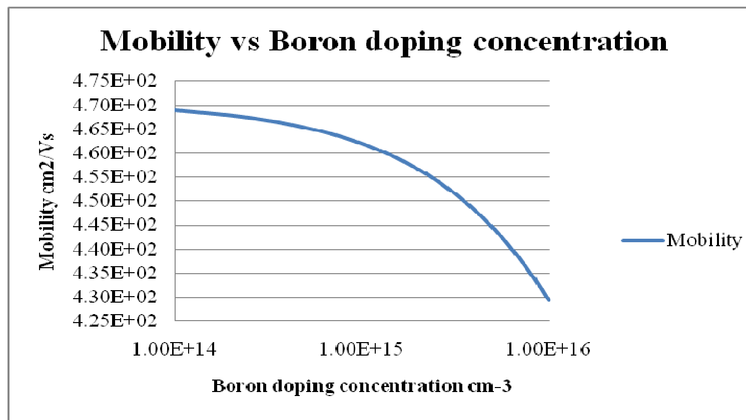




Figure 49: Mobility dependence on doping concentration

In an n+ doped region, where the donor concentration $N_D$ is approximately $10^{20}$ $cm^{-3}$, the electron concentration is approximately $N_D$ and the hole concentration is $n_i^2/N_D = (1.45\times10^{10})^2/N_D = 2.1$ $cm^{-3}$ at room temperature. Thus the conductivity due to holes is negligible in front of that of the electrons since the electrons concentration is about 20 orders of magnitude higher than the holes concentration.

The electron or hole densities depend on both the doping concentration in Si and the donor (acceptor) level of the dopants. For an n-type dopant, the donor level is closer to the conduction band and for a p-type dopant, the acceptor level is closer to the valence band. The ionization energy of the dopant is defined as the separation in energy between the donor (acceptor) energy level and the bottom of conduction (top of the valence) band. An electron bound to its donor atom needs an energy equal or greater to the ionization energy to transition to the conduction band and participate in conduction. The ionization energies

for phosphorus and boron in Si are both 0.045 eV. Thus at room temperature about 90% of all donors are ionized or give away their electrons to the crystal.

In the structures uniformly doped in phosphorus, the resistivity can be approximated as

$$\rho \approx \int \frac{1}{n(x) e \mu_n(x)} \tag{14}$$

where n(x) is a function of the depth and is $0.18(N_D\text{-}N_A)$, the number of ionized donors minus acceptors, $\mu_n$ the mobility varies with depth since the concentration of phosphorus varies with depth and e is the charge. From simulation, the bulk and nanomembrane resistance agree well with the experimental measurements (slope of I-V curve). The measured bulk and nanomembrane resistances are 4.65 Ω and 14 Ω respectively for a 5 μm channel length.

For structures where the channel is undoped, the resistivity depends on the hole concentration and the hole mobility since the channel is p-type or boron doped.

In nanostructures, the effective mobility is expected to increase significantly when compared to the bulk mobility. It was reported in [36,37, 38,39,40] that the mobility in nanowire Si transistor is significantly higher than in bulk Si transistor because the dominance of the mobility due to surface scattering $\mu_{sr}$ decreases significantly because of the electron-phonon wavefunction overlap, the surface scattering effects also decreases.

The absolute resistance value are of interest only to verify the accuracy of the electrical measurements, rather the change in resistance is the value needed to evaluate the change in the lateral diffusion in undoped (boron background doping) channels and in-depth diffusion in phosphorus doped channels. So far, the experimental results agree with the simulation which will be discussed next.

# Chapter 5: Modeling of Dopant Diffusion

## 5.1 Role of point defects

The phosphorus and boron atoms are electrically active when they replace a Si atom and occupy a lattice site. In order to diffuse in the crystal, the dopants D interact with native point defects in the crystal called interstitials I and vacancies V. The interstitials are Si atoms that are in between lattice sites and diffuse easily around the crystal, while vacancies are empty lattice sites unoccupied by Si, Figure 50. These point defects can form mobile pairs with the dopant atoms, which redistribute around the crystal in a random thermal

motion. This diffusion model is known as the pair diffusion model [41]. Thus the diffusion of dopant atoms is closely linked to point defects in the crystal. The effective diffusivity $D_{eff}$ in the presence of point defects is expressed as:

$$\frac{D_{eff}}{D^*} = f_I \frac{C_I}{C_I^*} + (1 - f_I)\frac{C_V}{C_V^*} \quad [42] \qquad (15)$$

Where $D^*$ is the equilibrium diffusivity, $f_I$ is the fraction of diffusion due to intersticialcy mechanism, $C_I$ is the interstitial concentration, $C_I^*$ is the interstitial equilibrium concentration, $C_V$ is the vacancy concentration and $C_V^*$ is the vacancy equilibrium concentration. Equation (15) reflects the impact of the point defects on the diffusivity of the dopant atoms. The intersticialcy component has been reported to be between 0.16-0.38 for phosphorus and 0.17-0.45 for boron [43, 44, 45, 46].

In fair's model, Boron diffuses by a $B^+V^-$ vacancy pair, where the extrinsic diffusivity $D_x$ is expressed as: $D_x = D^0 + D^+(p/n_i)$ (16)

Where $D^0$ is the neutral dopant diffusivity, $D^+$ is the $B^+$ diffusivity, p is the hole concentration and $n_i$ is the intrinsic carrier concentration. Thus, the boron diffusion is enhanced when $p>n_i$. Also, it has been recently reported that the intersticialcy component of boron diffusion is estimated to be more than 98% [47]. The phosphorus diffusion is explained as a vacancy dominated diffusion [42], where the extrinsic diffusivity is

expressed as $D_x = D^0 + D^{=}(\frac{n}{n_i})$ (17)

However, other researchers found evidence of intersticialcy component in the diffusion [48, 49].

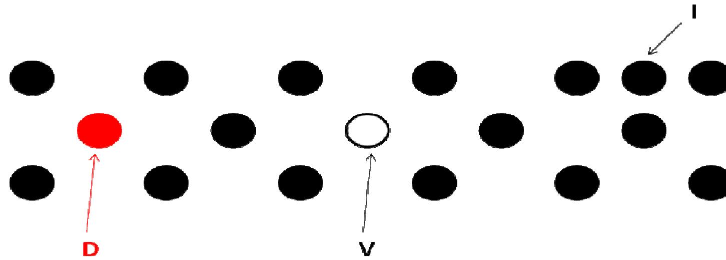



Figure 50: Point defects and dopants depicted in crystal lattice

The random walk model results in Fick's first and second laws:

$$J = -D\frac{\partial C}{\partial x} \qquad (18)$$

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \quad (19)$$

Where J is the dopant flux, D the diffusion constant and C the concentration.

Both the error function and Gaussian profiles originate from these differential equations after implementing the boundary conditions by keeping the surface concentration constant or changing over time.

## 5.2 Dopant segregation effects

At the interfaces, in this case oxide-silicon interface, the impurities will redistribute until equilibrium is reached at both sides of the interface. Thus the impurities are greatly affected by segregation effects because of the difference in diffusivity between the oxide and the silicon. The segregation coefficient m is defined as the ratio of the equilibrium concentration of impurity in Silicon divided by the equilibrium concentration of impurity in Silicon oxide. For phosphorus, the segregation coefficient m is greater than 1, resulting in the impurities piling up in the Si side of the interface. For Boron, the segregation coefficient m is less than 1, thus the impurities are depleted in the Si side of the interface, Figure 51.

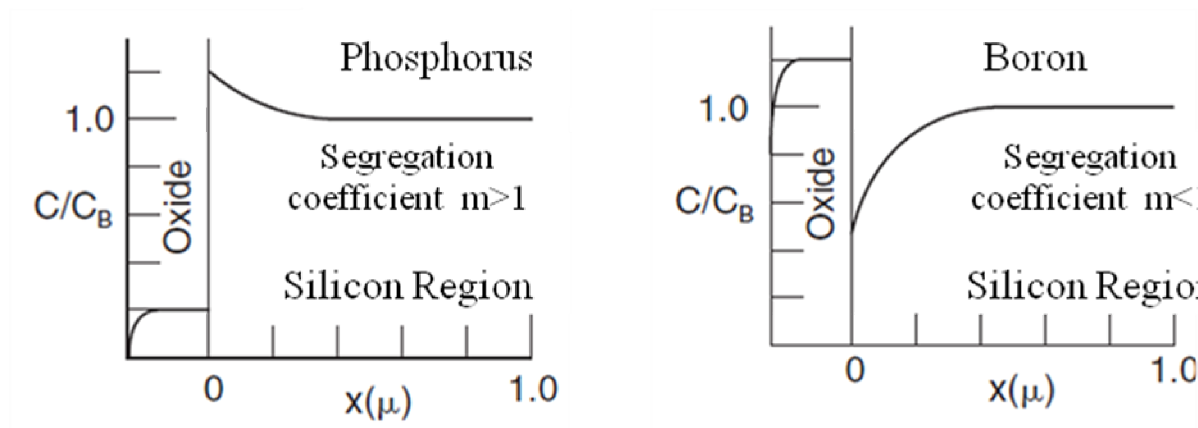



Figure 51: Segregation effects on Boron and Phosphorus profiles at oxide-silicon interface

These segregation effects have a greater impact in Si nanostructures than in bulk, since segregation occurs at both sides (top and bottom interfaces) such as in thin SOI substrates. In these structures, the segregation effects shape the impurity profile in thin Si layers, which can result in diffusion enhancement or retardation because of the shape of the diffusion front.

### 5.3 Modeling Diffusion

The TCAD Sentaurus Sprocess has been used to simulate the diffusion profiles of phosphorus in silicon. The "Charged React" model is the most advanced dopant diffusion model which makes it also the most computationally expensive due to the large number of equations required [50]. In this model, the immobile substitutional dopants and the mobile charged dopant –point defects pair species are considered [51].

Initially, the bulk structure uniformly doped with phosphorus was modeled to fit the adequate diffusion model with the SIMS profile. This same model was then implemented on the nanomembrane structure. The simulated phosphorus profile in Si bulk and nanomembrane is shown in Figure 52. The fitted profile is the constant source diffusion profile, the profile was also analyzed after a 3hr annealing period where furnace ramp ups and ramp downs were considered. The samples are loaded when the furnace reaches 600 °C, the ramp up to 1000 °C takes 15 min, after which 3 hr of drive in is timed and the ramp down to 600 °C takes 45 min. As seen in Figure 52, the concentration of the bulk profile drops significantly and the junction depth is extended because of the in-depth diffusion. However, in the nanomembrane, the concentration drops slightly only since the underlying layer is the BOX.

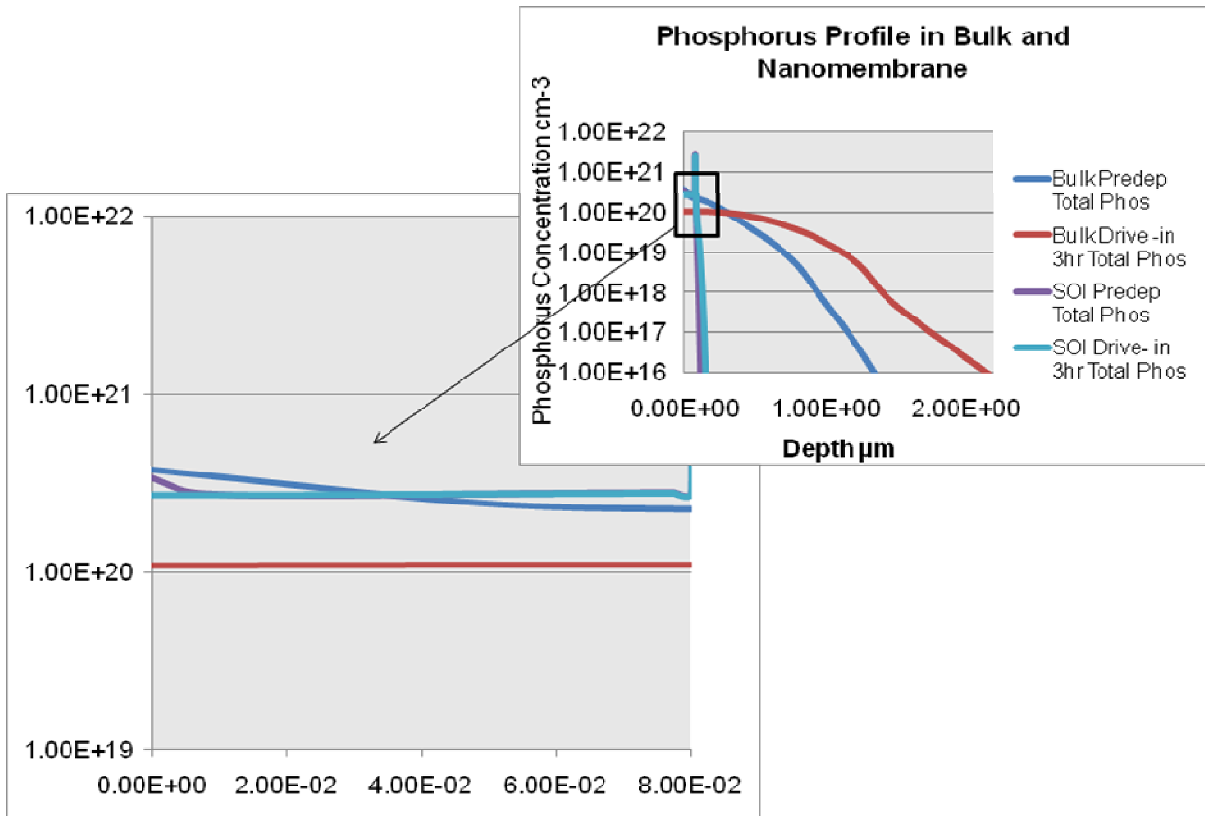



Figure 52: Simulated Phosphorus profile in bulk and nanomembrane

## 5.4 Effect of dimension reduction on diffusion

In order to understand the effect of reducing the volume reduction in nanomembrane compared to the bulk material, two scenarios were implemented: the first scenario consists of comparing Si bulk and a released nanomembrane (BOX etched), in both structures the channel is masked with oxide during the pre-deposition and annealing steps; the second scenario consists of comparing Si bulk and released nanomembrane, with an oxide mask in the channel only during the pre-deposition. Figure 53 shows the phosphorus lateral profile in a bulk Si and an 80 nm thick released nanomembrane (Si on nothing) after the dopant pre-deposition and after a 3 hr annealing period. It can be observed that the lateral diffusion is more enhanced in the bulk Si than in the Si on Nothing structure by 90 nm at a phosphorus concentration of $1.6\times10^{16}$ $cm^{-3}$. Figure 54 consists of the same structures as those in Figure 53 except that the oxide mask is removed before the annealing process. In Figure 54, the lateral diffusion in bulk progresses faster than in Si on Nothing by 150 nm at $1.6\times10^{16}$ $cm^{-3}$. The surface to volume ratio of the Si on Nothing is considerably higher than the bulk surface to volume ratio by 5 orders of magnitude. Thus, the geometry impacts the

lateral diffusion. The lateral diffusion is further enhanced when the oxide is removed because of the segregation effects from the Si-$SiO_2$ interface which are eliminated by etching away the oxide mask before the annealing.

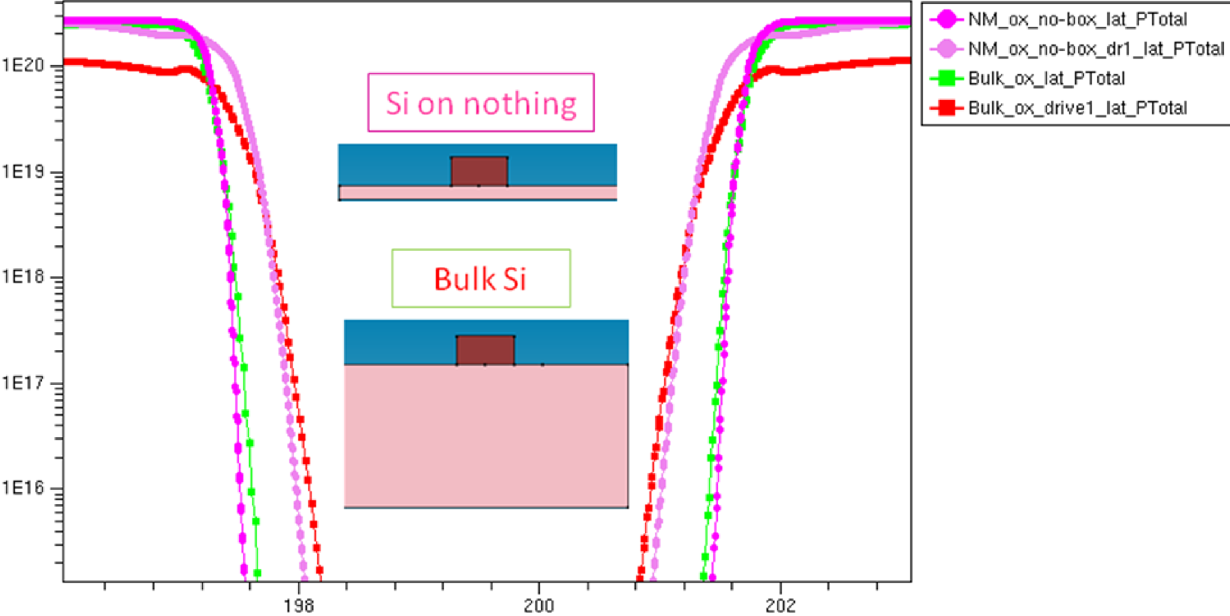



Figure 53: Lateral diffusion in bulk Si and 80 nm thick Si on nothing with channel mask with oxide

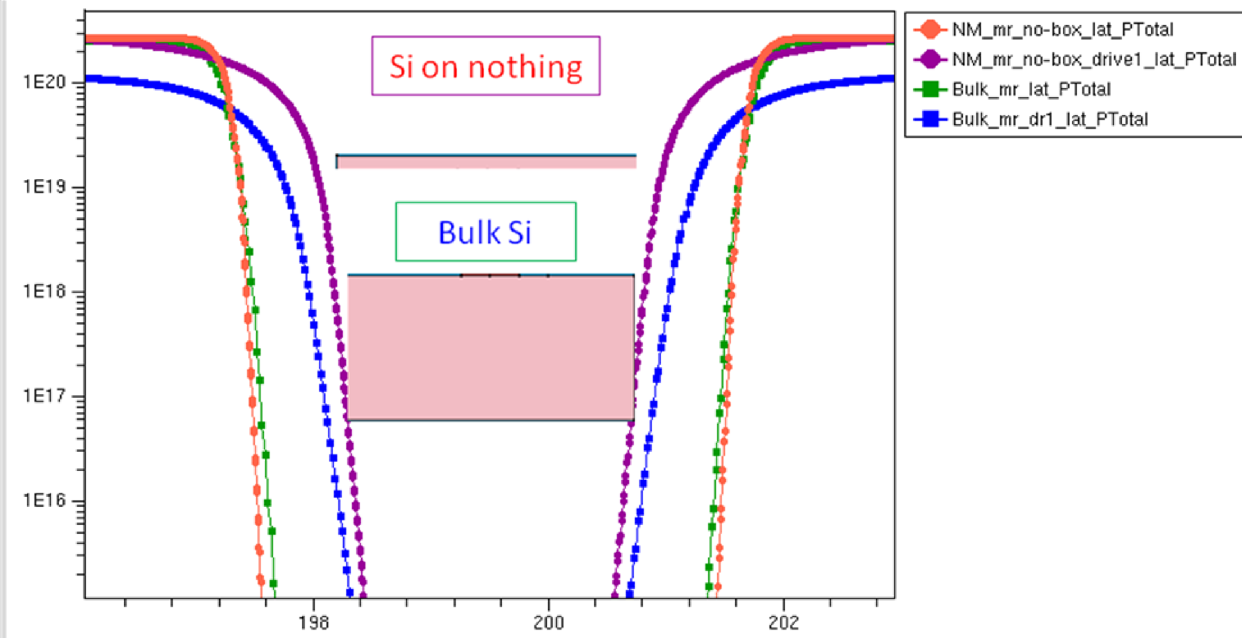



Figure 54: Lateral diffusion in bulk Si and 80 nm thick Si on Nothing with channel mask removed before annealing

## 5.5 Interface Segregation Effects

The segregation effects were discussed previously, it is expected that the interface effects will have a greater impact in the nanomembrane (2D) and 1D nanostructures because of the significant difference between the surface to volume ratio compared to bulk (3D). The segregation coefficient of phosphorus in a Si-$SiO_2$ system is greater than 1, thus the phosphorus dopants tend to accumulate at Si side of the interface. These effects are observed in both bulk and nanostructures. However, the surface to volume ratio is at least 4 orders of magnitude greater in nanostructures compared to bulk. Thus, the segregation effects will be more severe in small dimensional structures. It must be noted that the nanostructures in SOI suffer from segregation from the BOX and the channel oxide interface. Figure 55 shows the phosphorus lateral profile in an 80 nm thick nanomembrane around the undoped channel after source and drain doping and annealing. During the drive-in step, the channel oxide mask is maintained in one structure and etched away in the other structure. As expected, the doping profiles after the doping overlap since the two structures are the same during the doping. However, after removing the oxide from the channel during the annealing from one sample, the profiles of the two samples no longer overlap. In fact the lateral diffusion is enhanced in the sample without channel oxide by 70 nm which is quite significant when compared to current channel length of 20 nm. The impact of the segregation effects on the diffusion is observable in this scenario.

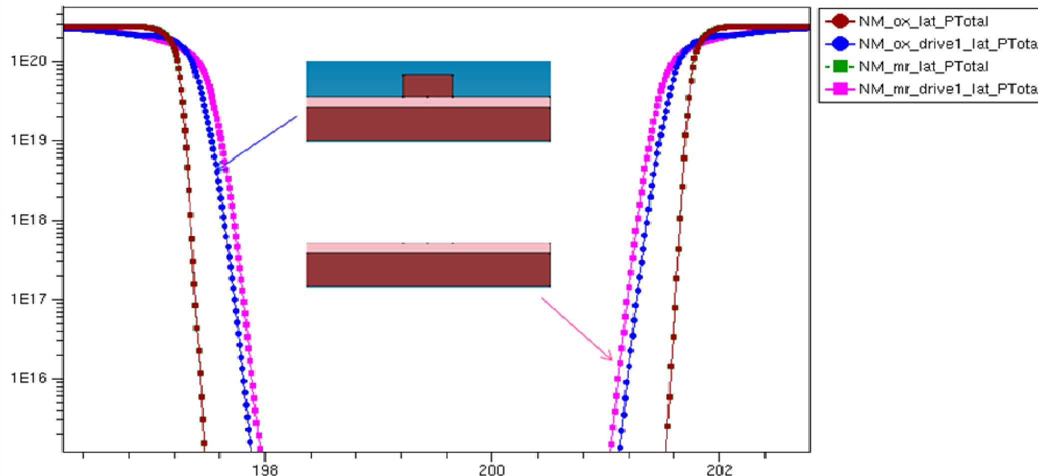



Figure 55: Phosphorus Lateral diffusion profile after pre-deposition and annealing with and without oxide mask in channel

To understand this effect better, the phosphorus lateral diffusion is evaluated in two nanomembranes structures (Si on nothing and SOI) shown in Figure 56. The two active Si layers are both 80 nm thick. The lateral diffusion profiles are shown after doping and annealing processes for both structures in Figure 56. Even after the doping, the lateral diffusion in the Si on nothing nanomembrane progresses faster (by 70 nm) than in the SOI nanomembrane. As shown in the case in the previous scenario, the segregation effects from the BOX retards the diffusion in the SOI nanomembrane

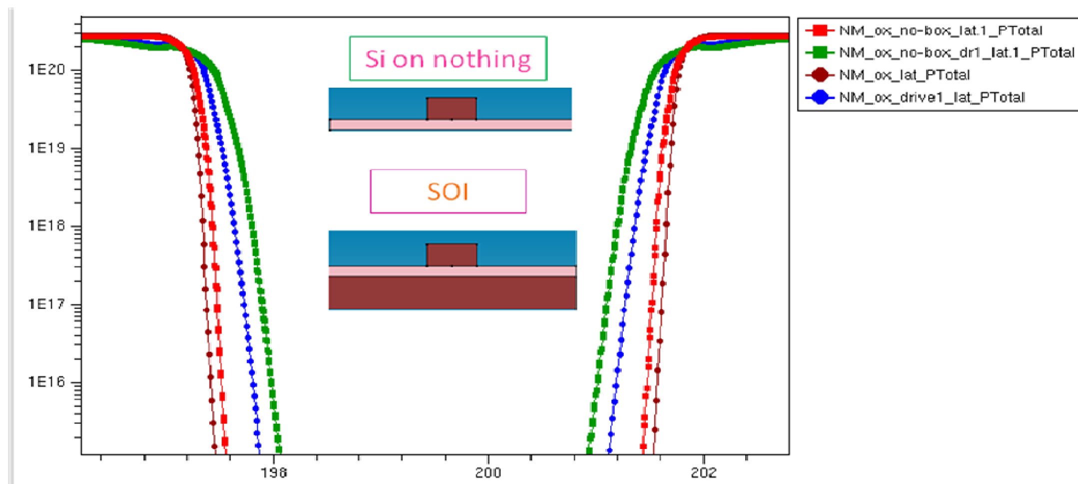



Figure 56: Phosphorus lateral diffusion profile in SOI and Si on nothing structures after pre-deposition and 3hr anneal with oxide on the channel

In Figure 57, lateral diffusion in Si on nothing nanomembrane is compared to SOI nanomembrane, where the channel oxide mask is removed before the drive in process. Similar observations can be made; the lateral diffusion is retarded in the SOI nanomembrane compared to the Si on Nothing. The gap between the lateral junction depths grows from 70 nm to 400 nm in the drive-in profile since there are no oxide interfaces in the Si on Nothing nanomembrane.

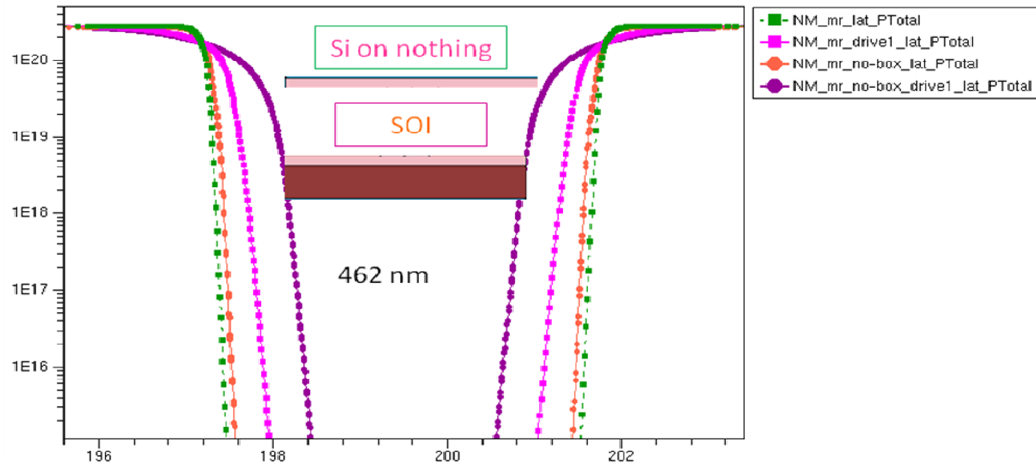
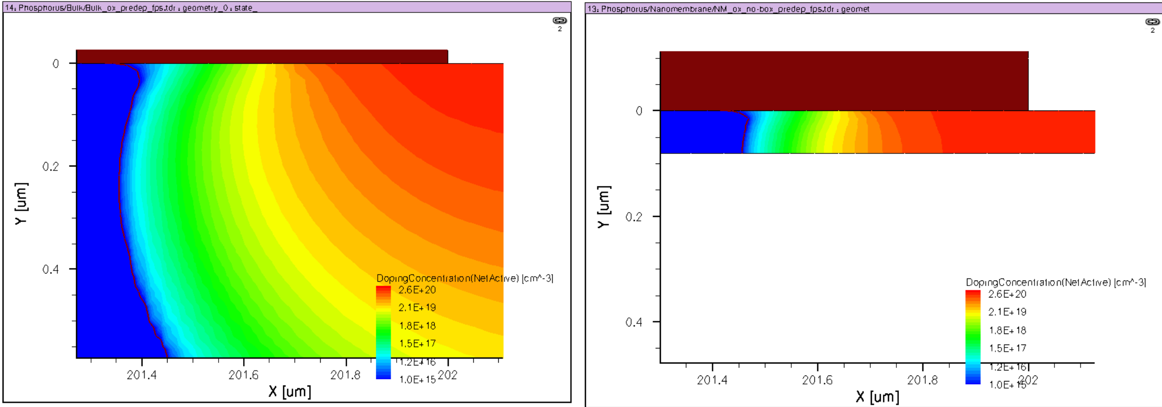



Figure 57: Phosphorus lateral diffusion profile in SOI and Si on Nothing after doping and oxide removed during annealing

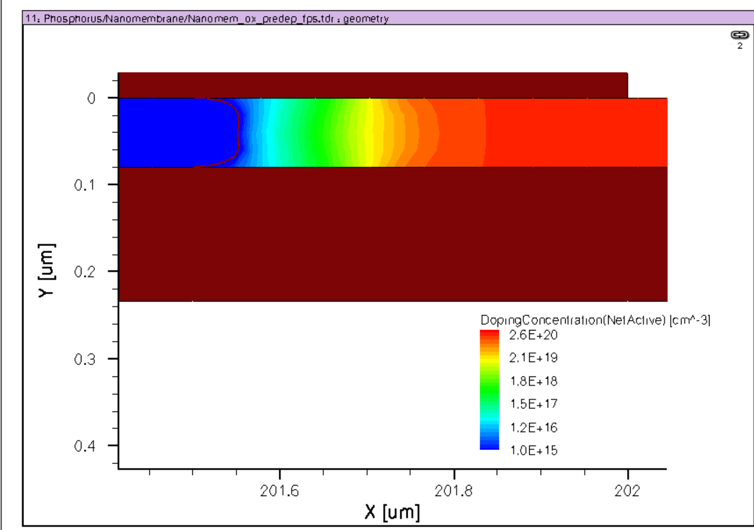
In all the previous scenarios, the impact of the segregation effects in Si bulk and nanomembrane was assessed. In fact, it was observed that the dopant segregation in a Si-$SiO_2$ interface retards the diffusion of phosphorus. This effect can be observed in both bulk and nanomembrane interfaces; however, the interface segregation is much more severe in nanomembranes because of the surface to volume ratio difference. Figure 58 below shows the active concentration profiles in bulk, Si on Nothing nanomembrane and SOI nanomembrane after doping source and drain regions with phosphorus. The images show the channel-drain side of the structure. Part of the oxide channel mask is shown in dark red and for the SOI the BOX is also shown in dark red. The blue color represents the Boron background doping; thus a line is drawn to depict the lateral junction. Each color is representative of an active doping concentration level. As seen, in Figure 58a-b, the accumulation of phosphorus doping at the Si/$SiO_2$ interface is observed. In Figure 58c, the accumulation of phosphorus occurs at both Si-channel $SiO_2$ and the Si-BOX interfaces, thus the accumulation is even greater than in the previous structures which can be seen from the large curvature of the lateral junction line. In the electrical measurements discussed in the previous sections, the change in resistance due to diffusion time decreases with decreasing dimension (3D to 1D). This decrease is correlated with the accumulation of phosphorus at the interfaces which retards the overall diffusion front in nanomembrane, nanoribbon and nanowire compared to bulk Si. This accumulation of phosphorus could lead to deactivation of dopants at the interface which can no longer participate to the conduction and thus reduce the measured change in resistance. The resistance is proportional to the carrier

density which decreases with deactivation of dopants, thus reducing the resistance decrease due to diffusion time. In nanoribbon and nanowire, the lateral junction line curvature is expected to increase since more dopant accumulation is predicted with the increase number of oxide interfaces. In both the nanoribbon and nanowire, the oxide is wrapped around the channel leading to more severe segregation effects. In fact, from the electrical measurements, the nanowire resistance increased after 3 hr long anneal.




a. Channel-drain side shown in bulk

b. Channel-drain side shown in Si on Nothing




c. Channel-drain side shown in SOI

Figure 58: Phosphorus doping profile at the channel-drain side for bulk Si on Nothing, SOI nanomembranes after source and drain doping. Oxide mask shown in dark red and buried oxide in SOI in dark red.

## Chapter 6: Additional work

### 6.1 Study of the Silicidation of Niobium Deposited by Physical Vapor Deposition [52]

Initially Niobium was considered as a candidate for the source and drain electrodes since it can withstand high temperatures with a melting above 2000 °C, to avoid removing the electrodes before every furnace annealing step. However, first the behavior of Nb deposited on Si and annealed at 1000 °C had to be understood. NbSi compounds are known to exist however these films are deposited using CVD techniques and thus there has been previous report on annealing of deposited Nb on Si. Interesting results were observed leading to further investigation of this topic.

Amorphous niobium was deposited by physical vapor deposition on a silicon (100) wafer and $SiO_2$ surfaces. The formation of niobium silicide was investigated by annealing amorphous Nb in the temperatures ranging from 400 °C to 1000 °C. The resistivity of Nb silicide is significantly higher than that of Nb for all annealing temperatures. The Nb silicidation as a function of temperature has been investigated. Different compounds of $Nb_XSi_y$ have been characterized. It has been observed that Nb silicidation is accompanied by a strong volume expansion of about 2.5. The films' structural properties were studied using X-Ray diffraction, energy dispersive spectroscopy, and atomic force microscopy. The X-Ray diffraction characterization of the Nb on Si sample annealed at 1000 ºC showed the presence of hexagonal $Nb_5Si_3$ phases with a dominant peak in the (200) direction. A distinct transition from Stranski-Krastanov to Volmer-Weber film growth has been observed at 400 °C. The observed increase in surface roughness of niobium silicide films correlates strongly with the grain size growth.

#### 6.1.1 Introduction

Niobium is a superconducting metal with high melting temperature which makes it suitable for superconducting electronic applications (Josephson junctions) and high temperature applications. However, Nb can form $Nb_xSi_y$ compounds having insulating characteristics and capable of withstanding very high temperatures with a melting temperature above 2123 $^oK$ on the Niobium rich side [53]. $Nb/Nb_xSi_{1-x}/Nb$ junctions are being considered for superconducting electronics applications as a replacement to

Nb/$AlO_x$/Nb junctions [54] Thus, it is of interest to understand different methods of $Nb_xSi_y$ compound formation and their morphological characteristics. In contrast to $Nb_xSi_y$ compounds exhibiting insulating characteristics, some $Nb_xO_y$ compounds with different phases display superconducting properties [55] Thus, it is of interest to understand the silicidation of Nb and the simultaneous formation of $Nb_xO_y$ along with its impact on the electrical properties of the resulting compounds.

Different techniques have been used to fabricate NbSi compounds such as co-sputtering Nb and Si simultaneously [53], chemical vapor deposition (CVD) of Nb on SiC [56], NbSi compound [57] using CVD. However, the properties of $Nb_xSi_y$ resulting from physical vapor deposition (PVD) on Si and annealing have not yet been investigated.

In this work, the silicidation of Nb was studied by X-ray diffraction (XRD) by energy dispersive X-ray spectroscopy (EDS), and by atomic force microscope (AFM) to elucidate the crystallographic phases. The electrical properties were characterized using a four-point probe. In addition to forming $Nb_xSi_y$ from the deposition and annealing of Nb on a Silicon substrate, Nb was also deposited on an intermediate layer of grown $SiO_2$.

### 6.1.2 Experiment and Fabrication

Niobium thin films were deposited by PVD. A Lesker PVD 250 system was used to deposit 160 nm of Niobium on 4" Si (100) wafers at 50ºC. The Si substrates underwent a few cleaning steps before the Niobium deposition including a series of acetone/Isopropyl alcohol and Deionized water rinses, followed by etching in diluted 50:1 HF to remove the native oxide. Another set of samples was fabricated by depositing Nb on a grown silicon oxide ($SiO_2$) layer, which was then annealed simultaneously with the previous samples, where Nb was directly deposited on Si. The thermal $SiO_2$ layer was grown on a HF etched Si wafer using an oxidation furnace at 1000 ºC. A continuous dry oxidation/wet oxidation/dry oxidation series was used in order to obtain higher quality thermal oxide at the interface. The total oxide thickness that was grown was 469 nm. The Niobium film was deposited on bare Si wafers and on $SiO_2$/Si substrates by Kurt Lesker PVD 250 using an e-beam system). The deposition rate was maintained around 1Å/s for optimum film uniformity throughout the entire process. The chamber pressure was $\sim 4 \times 10^{-6}$ Torr.

After deposition, a portion of the wafer was cleaved for post-deposition annealing. The samples were annealed in a furnace tube at temperatures ranging from 400 $^{o}$C to 1000 $^{o}$C with 200 $^{o}$C increments. For each annealing condition, the furnace is ramped up to a temperature of about 200 ºC lower than the annealing temperature and the tube is filled with Nitrogen ($N_2$) flowing at a rate of 1L/min. After loading the samples in the hot furnace, the temperature is ramped up to the annealing temperature and the nitrogen flow rate is increased to 3L/min. The furnace temperature ramp rate is approximately 40 ºC/min. Thus all samples are annealed in Nitrogen ambient for 30 min at a stable temperature. Following the steady temperature annealing duration of 30 min, the furnace is ramped down back to a temperature 200 ºC lower than the annealing temperature at which the sample is slowly unloaded. The annealing steps described above are displayed in **Error! Reference source not found.**.

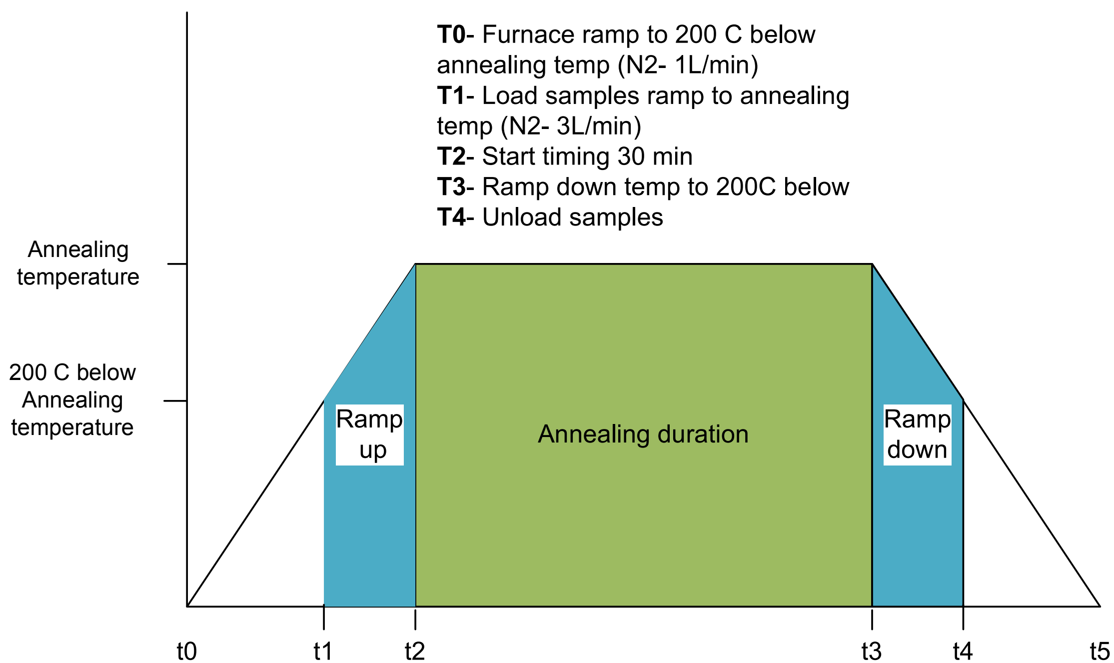



Figure 59: Annealing experiment timeline showing furnace annealing steps.

The crystal structure and the crystalline phase of the resulting niobium silicide film were characterized by a Rigaku Miniflex XRD machine with a Cu $K_{\alpha}$ X-ray ($\lambda$ = 1.54Å).

The EDS analysis was performed using a SEM (JSM-6060LV) by JEOL. The surface morphology was investigated using a Nanoscope Dimension™ 3100 AFM by Veeco.

### 6.1.3 Discussion and results

Initially, the samples were analyzed by Energy-dispersive X-ray spectroscopy (EDS). The EDS spectra for the as-deposited samples are shown in Figure 60. The data shows no sign of other contaminants present in the film besides the elements expected such as Nb, Si, and O in the case of Nb/$SiO_2$ samples.

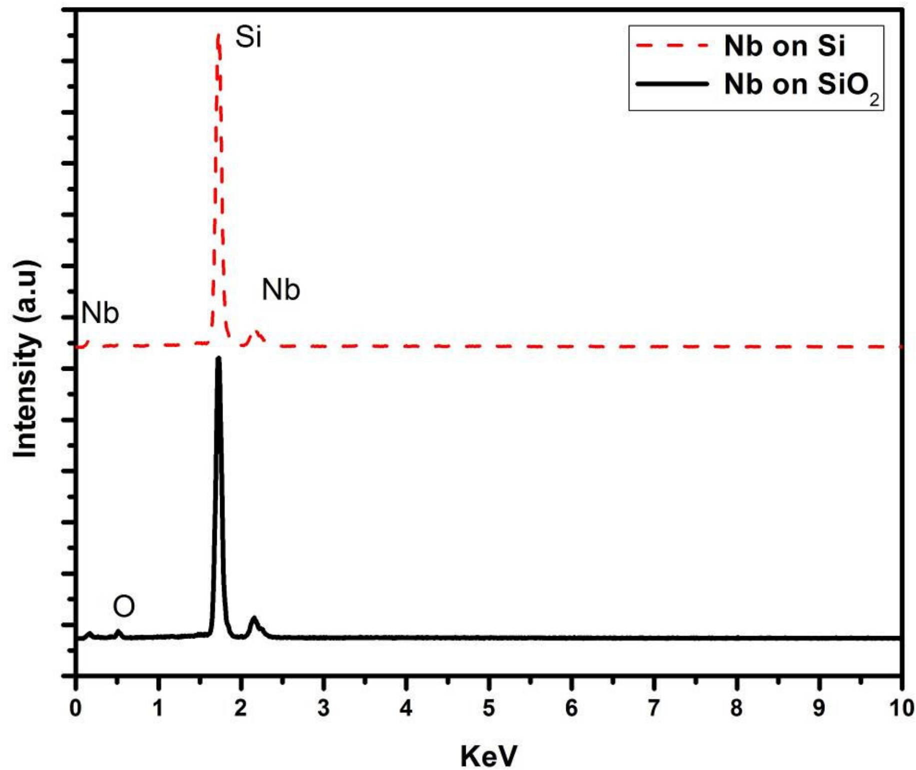



Figure 60: EDS spectrum of Nb/Si and Nb/SiO2 as deposited sample. (dashed line) represents Nb/Si and (solid line) represents Nb/$SiO_2$ samples.

In Figure 61, a microscopic image of an area showing both exposed $SiO_2$ and as-deposited Nb on $SiO_2$ is displayed. A liftoff technique was used to pattern the as-deposited Nb film in order to compare the thickness before and after annealing of the Nb film. First, photoresist was patterned in strips on a silicon substrate and Nb was deposited on the patterned substrate using PVD. Then, the substrate was submerged in acetone to remove the photoresist and leave Niobium on the substrate over areas that did not have photoresist from the start. The resulting Nb pattern is shown in Figure 62a) after the liftoff step was

performed and Figure 62b) shows the deposited Nb thickness measured using a profilometer. Figure 62c) shows the same Nb pattern after annealing at 1000 ºC and in the same way Figure 62d) shows the resulting film thickness measured. The deposited Nb film is about 1750 Å before annealing and the resulting niobium silicide compound thickness is about 4800 Å after annealing. Also, the resulting characteristic color and texture change could be readily detected by optical microscopy. Thus, a growth of over 3000 Å and the concomitant volume expansion of a new compound, which is thought to be a form of $Nb_xSi_y$, are observed.

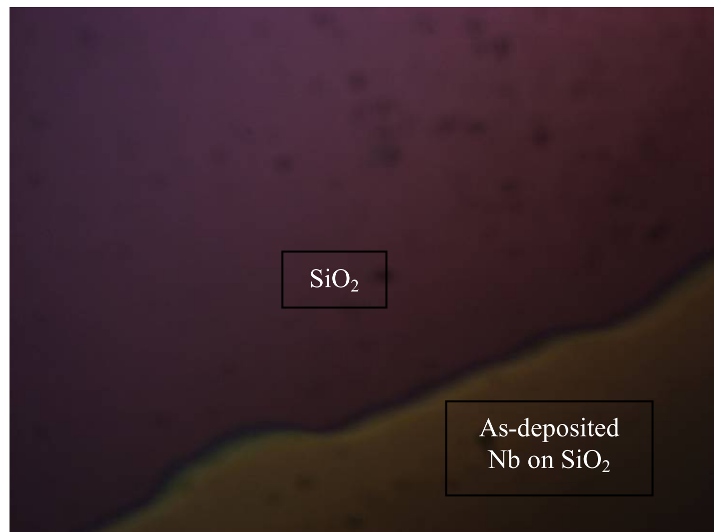
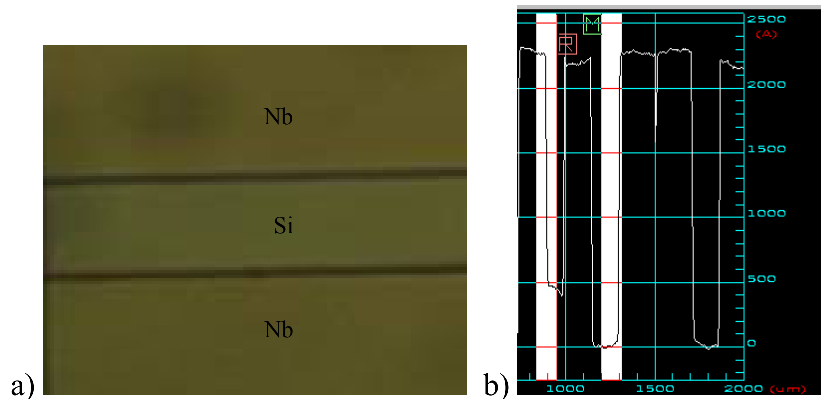



Figure 61: As-deposited Nb on $SiO_2$ and exposed grown $SiO_2$



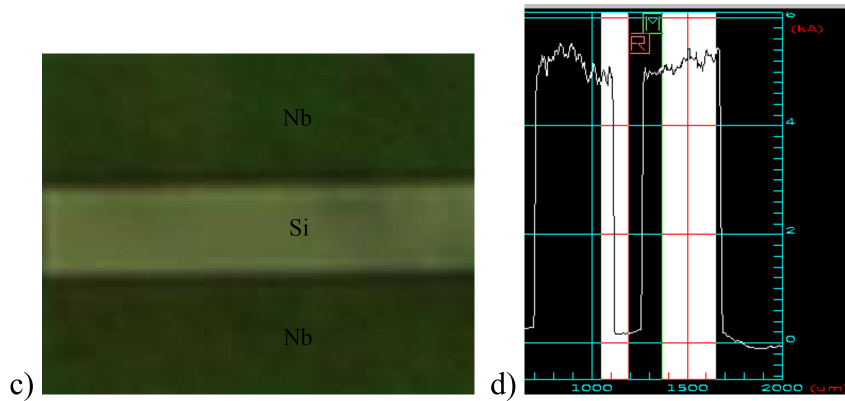
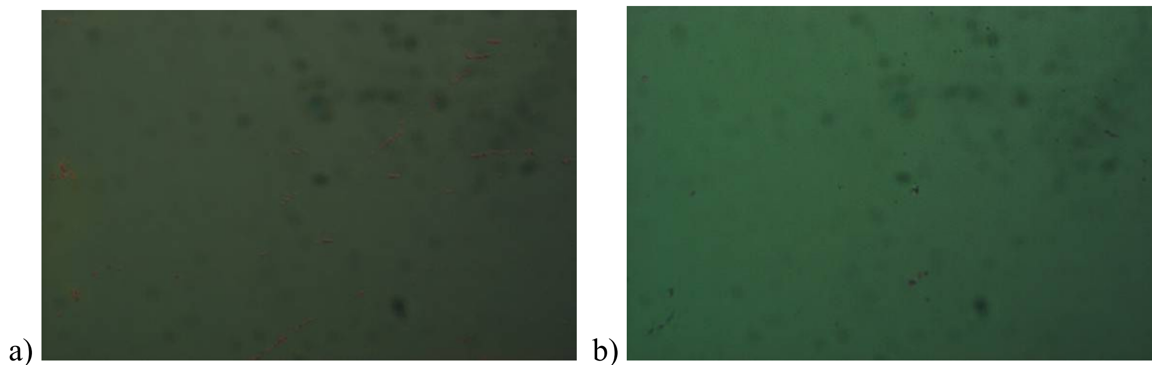



Figure 62: a) Nb strips on Si after liftoff b) Profilometer measurement of Nb thickness after liftoff (1750 Å) c) Nb strips on Si after annealing d) Profilometer measurement of resulting compound after annealing (4800 Å)

In Figure 63, the optical microscope images are shown when Nb is deposited on Si and annealed at different temperatures. The color of the resulting niobium silicide compound varies for different annealing temperatures. The film roughness becomes more noticeable as the annealing temperature increases. The same observation is made for the Nb which is deposited on $SiO_2$ and annealed at different temperatures, see Figure 64. For each temperature, the Nb on Si and the Nb on $SiO_2$ were annealed at the same time in the furnace; however, the colors of the two films Nb/Si and Nb/$SiO_2$ are different after annealing.



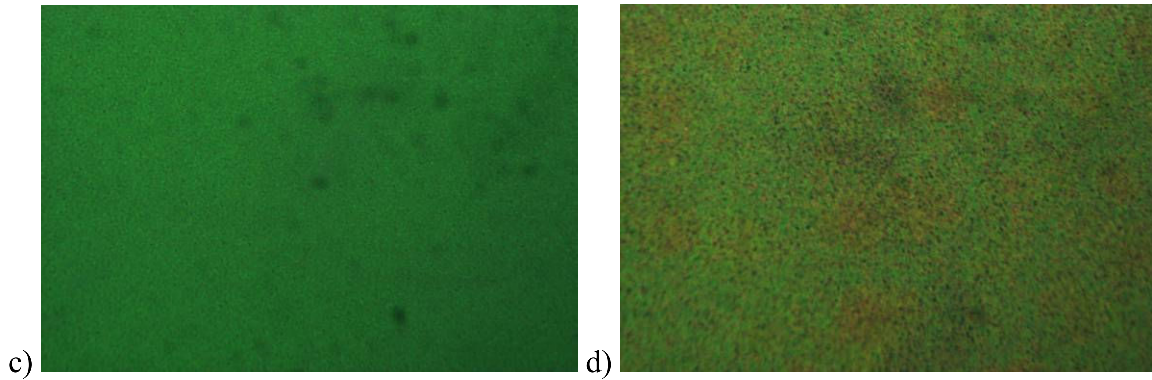


Figure 63: a) Nb on Si annealed at 400 ºC Nb. b) on Si annealed at 600 ºC. c) Nb on Si annnealed at 800 ºC. d) Nb on Si annealed at 1000 ºC

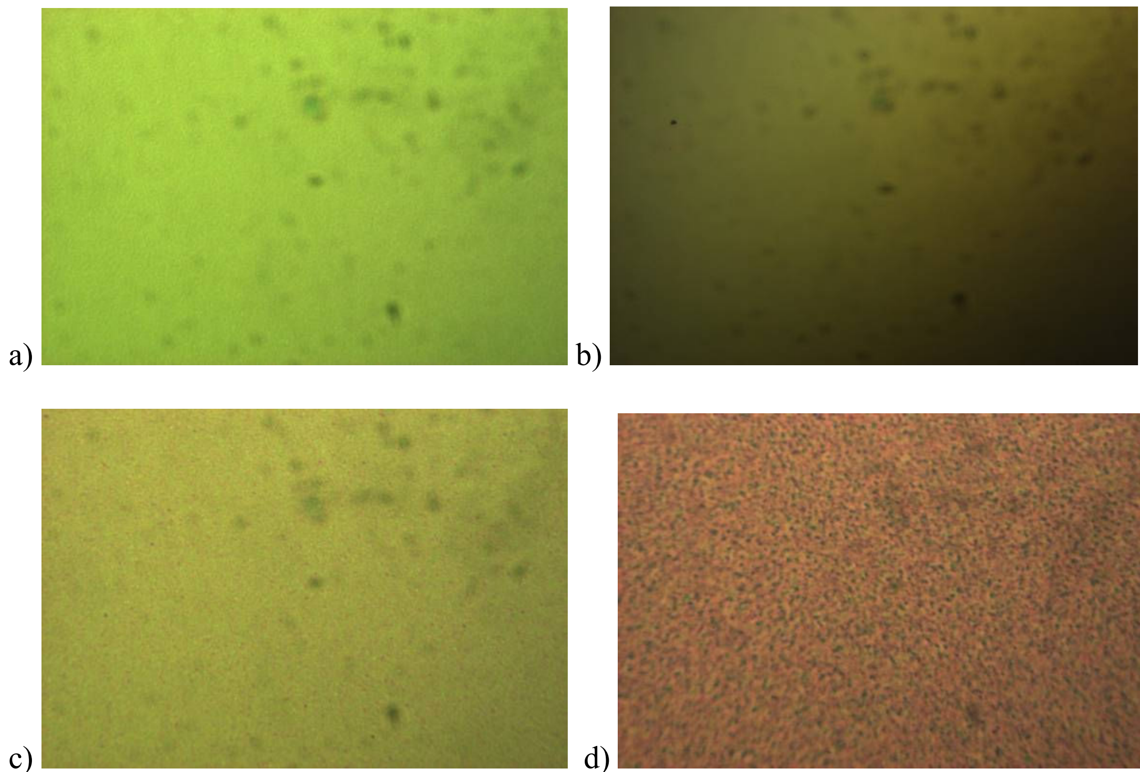


Figure 64: a) Nb on $SiO_2$ annealed at 400 ºC. b) Nb on $SiO_2$ annealed at 600 ºC. c) Nb on $SiO_2$ annnealed at 800 ºC. d) Nb on $SiO_2$ annealed at 1000 ºC

In addition to the optical imaging, the niobium silicide film surface morphology was investigated by AFM. The AFM analysis revealed an increase in roughness as the annealing temperature increases from 400 $^{o}$C to 1000 $^{o}$C. The AFM roughness RMS plots of both the Nb on Si and Nb on $SiO_2$ systems are shown in Figure 65. The roughness RMS value is constant at about 2.5 nm for both Nb/Si and Nb/$SiO_2$ for annealing temperatures up to 600$^{o}$C. However, for annealing temperatures above 600 $^{o}$C, the RMS increases

exponentially as shown in Figure 65. This observation is consistent for both Nb/Si and $Nb/SiO_2$ samples.

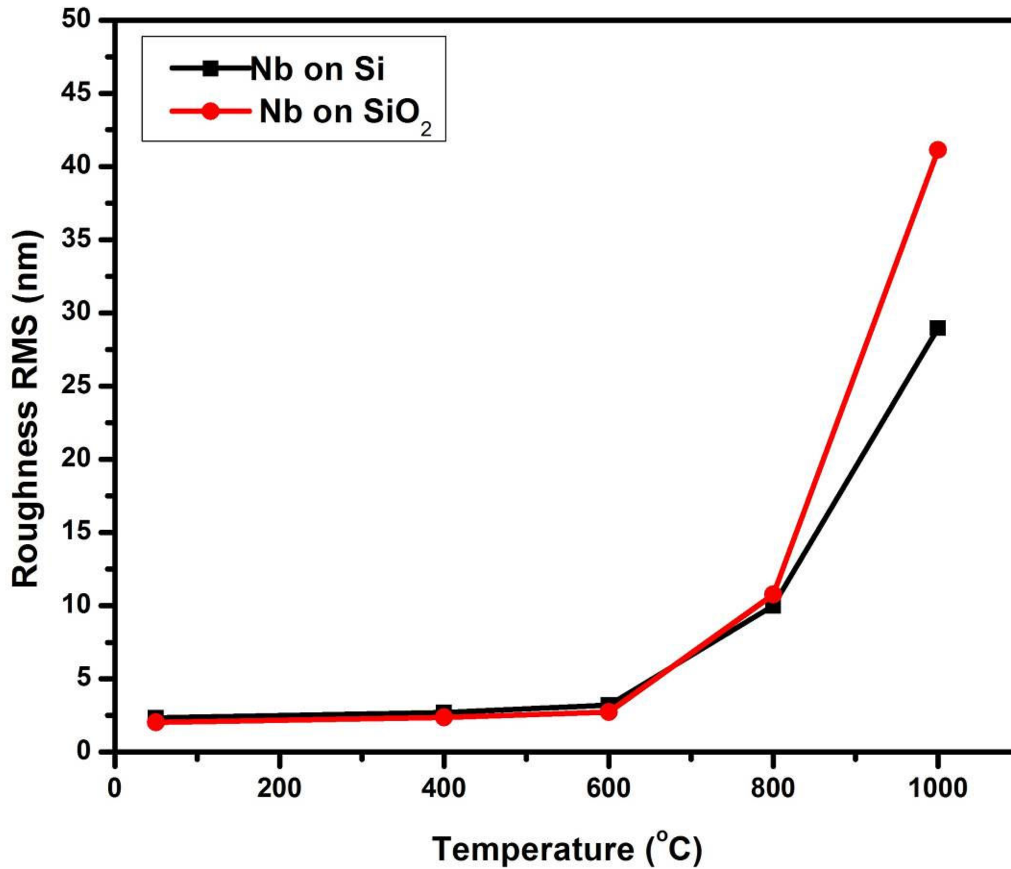



Figure 65: AFM roughness study of Nb/Si and $Nb/SiO_2$ as a function of temperature. (square) represents experimental data for Nb/Si system and (circle) represents $Nb/SiO_2$ system.

The grain size was also measured from the AFM data. Analogous to the roughness plot, the average grain size increases exponentially for annealing temperatures greater than 600 $^oC$. The as-deposited Nb grain size value is ~50 nm for Nb/Si compared to ~25 nm for $Nb/SiO_2$. For an annealing temperature of 1000 $^oC$, the grain size is ~230 nm for Nb/Si samples and ~170 nm for $Nb/SiO_2$. The results of the grain size measurement are shown in Figure 66.

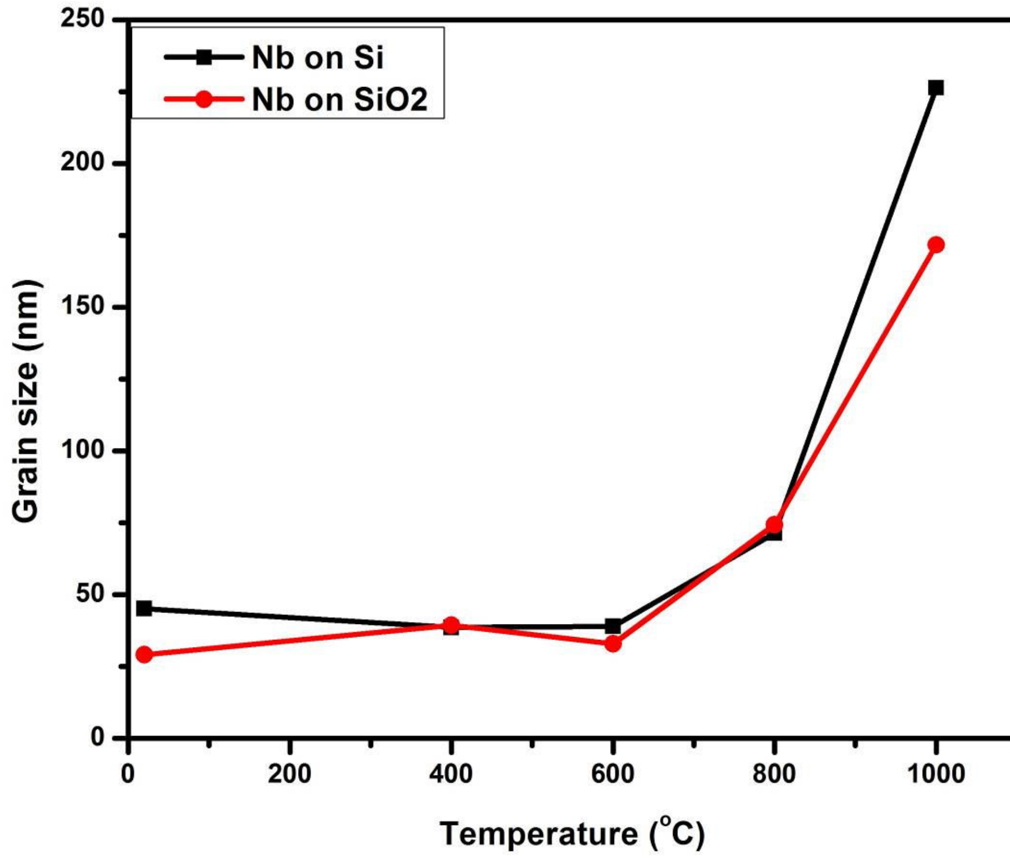



Figure 66: Grain size of Nb/Si and Nb/$SiO_2$ as a function of temperature. (circle) represents data for Nb/$SiO_2$ while (square) represents Nb/Si.

Figure 67 and Figure 68 displays the AFM images of the different samples used in this study. Considerable grain growth has occurred in these figures as a function of increasing annealing temperature for both Nb/Si and Nb/$SiO_2$ samples. Thus, there is a direct linear correlation between the surface roughness and grain growth. This relation holds true for both Si and $SiO_2$ substrates. The difference between the Nb silicides on Si and $SiO_2$ substrates seems to be that $SiO_2$ provides a limited Si supply relative to the Si substrate for the silicidation reaction.

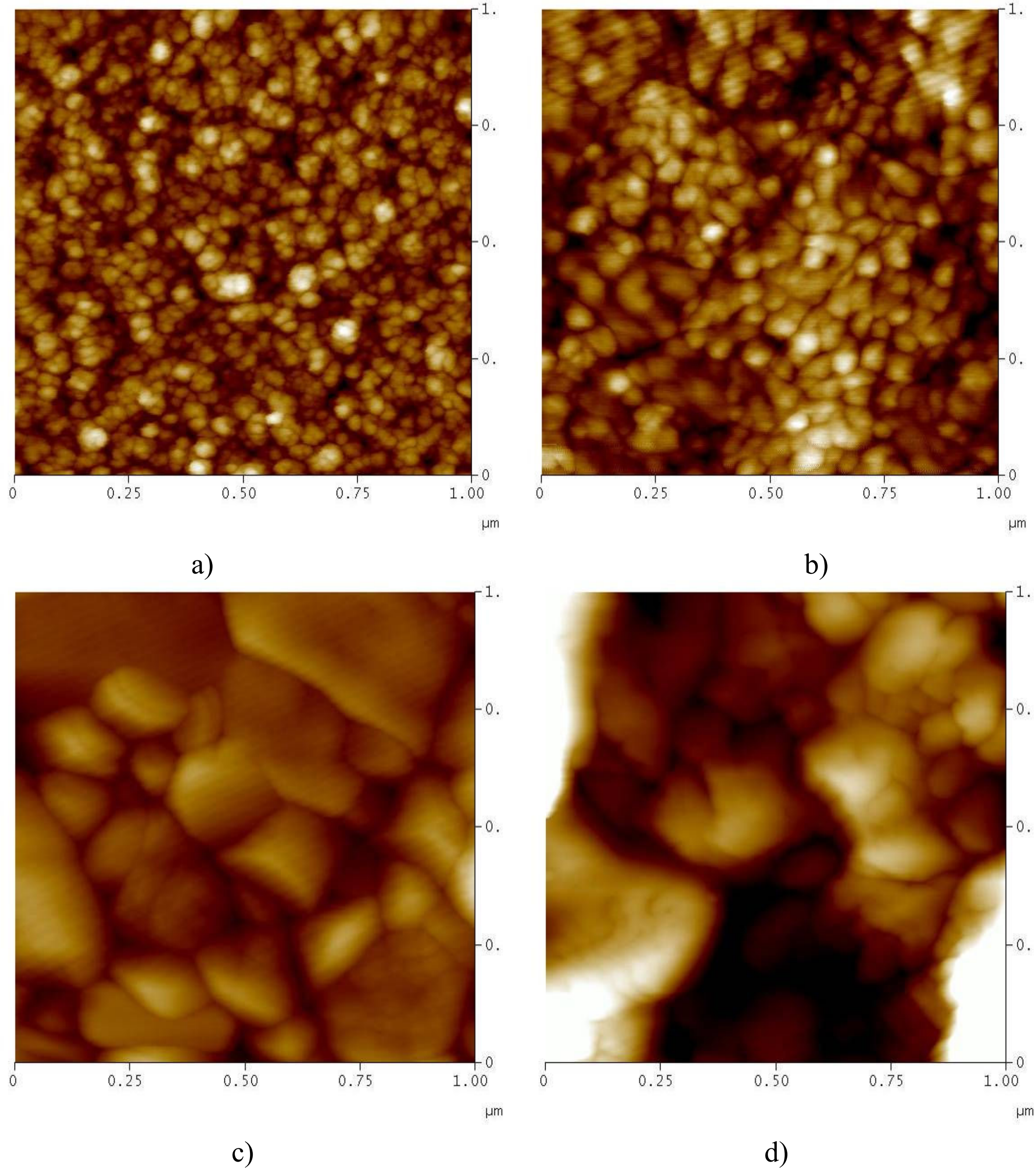



Figure 67: AFM images of Nb on Si samples. a) post-deposition annealing at 400 $^{o}$C, b) post-deposition annealing at 600 $^{o}$C, c) post-deposition annealing at 800 $^{o}$C, d) post-deposition annealing at 1000 $^{o}$C.

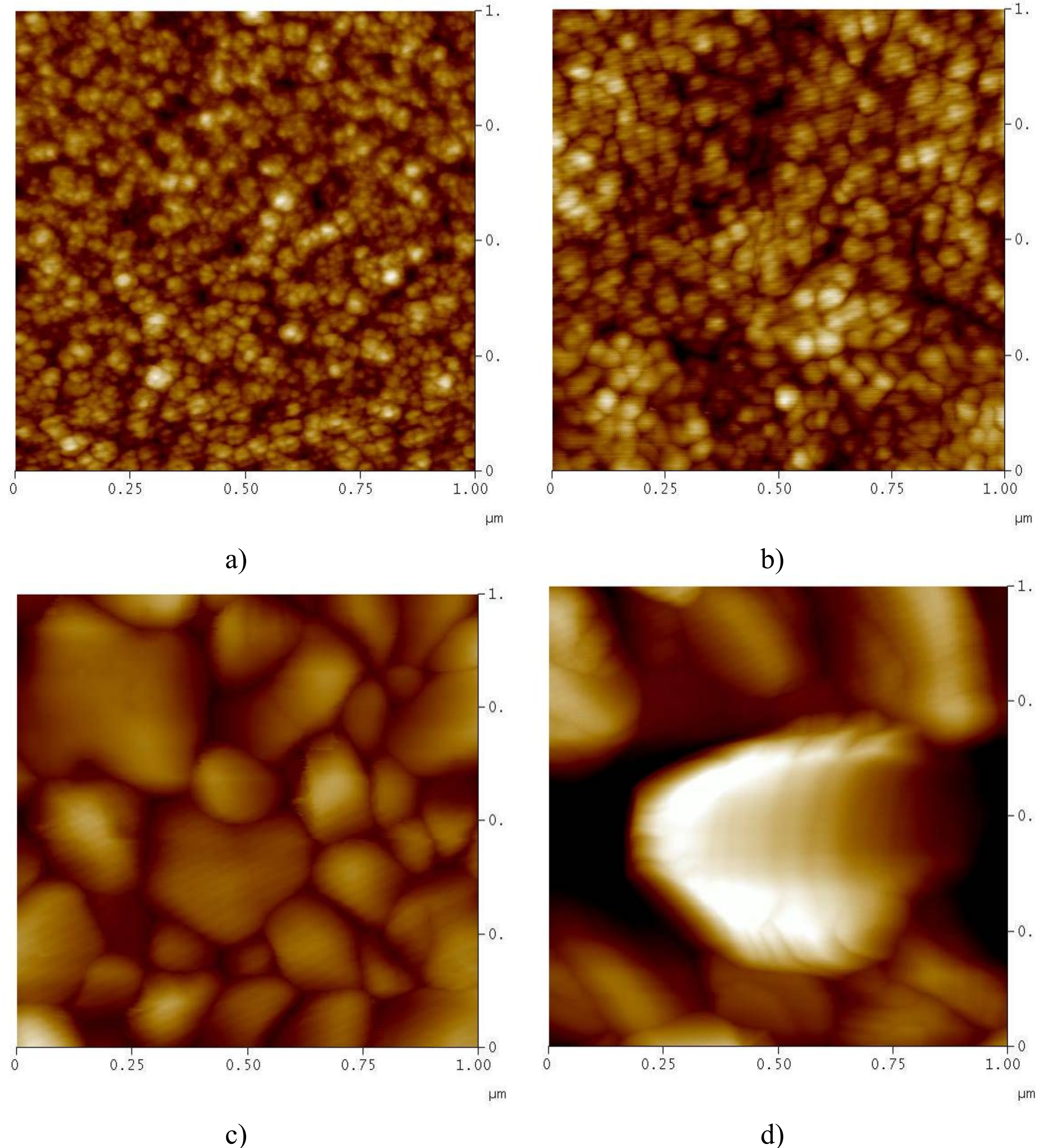



Figure 68: AFM images of Nb on $SiO_2$ samples. a) post-deposition annealing at 400 $^oC$, b) post-deposition annealing at 600 $^oC$, c) post-deposition annealing at 800 $^oC$, d) post-deposition annealing at 1000 $^oC$.

Fractal dimensions have been widely used to study the growth process of thin films [56,57,58] Three main growth models can be used to describe thin film growth. There are Frank Van der Merwe, Volmer-Weber, and Stranski-Krastanov film growth models. Frank Van der Merwe growth is characterized by a layer by layer growth. The Volmer-Weber model is characterized by an island growth and heterogeneous nucleation. While in the Stranski-Krastanov model, a mixture of island growth and layer-by-layer growth is found

[59]. The fractal geometry describes the scaling structure of a film surface by a number called the fractal dimension. From the fractal dimension, the growth model can be determined [56]. The fractal dimensions of *D'<1.5, D' ≈ 1.5, and D' > 1.5* correspond to Volmer-Weber, Stranski-Krastanov and Frank Van Der Merwe growth, respectively. The fractal dimensions were extracted from the WSxM software [60]  Figure 69 shows the fractal dimension as a function of annealing temperature. Our PVD deposited Nb thin films follow the Stranski-Krastanov model (which implies you should observe crystallites embedded in amorphous Nb). From the XRD measurements, there is a broad halo peak for the as deposited and samples annealed at low temperatures confirming the amorphous nature of the films. As the annealing temperature is increased, there is a mix phase confirmed by the sharp peaks superimposed on the broad peak from the amorphous Nb. As the post deposition annealing temperature increases to 600 $^{o}$C and above, the growth mode switches from Stranski-Krastanov to Volmer-Weber model. The onset of Volmer-Weber model, which is characterized by island growth, correlates well with the significant increase in roughness and grain size for the samples annealed  at higher temperatures. As a result, the silicidation of Nb deposited by PVD takes place in an island growth manner.

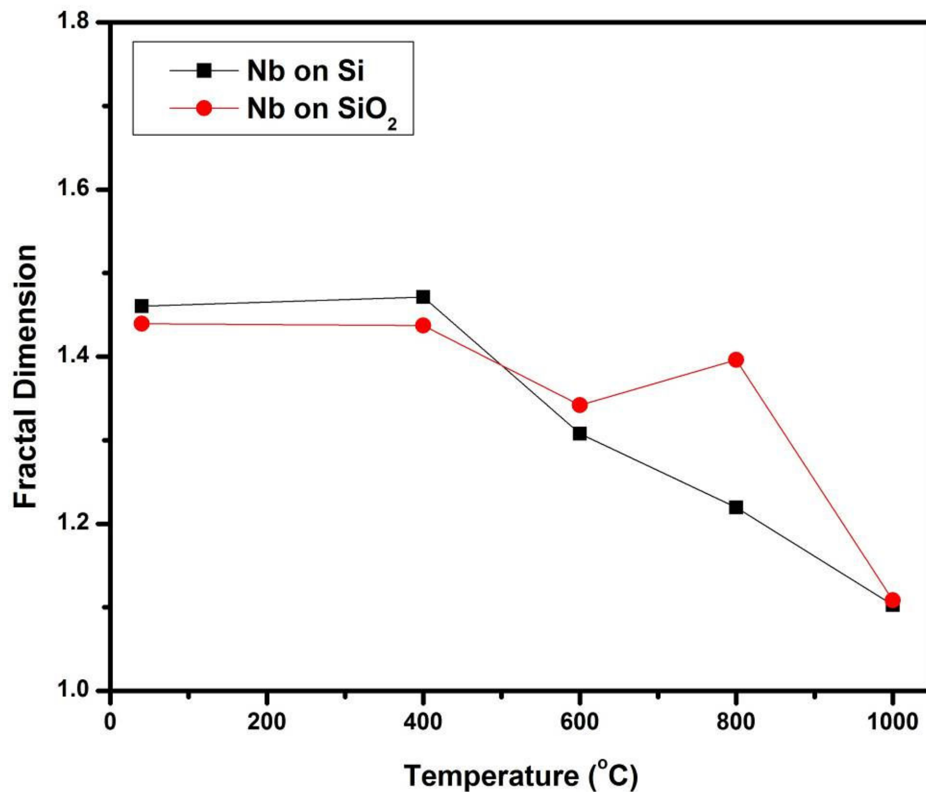
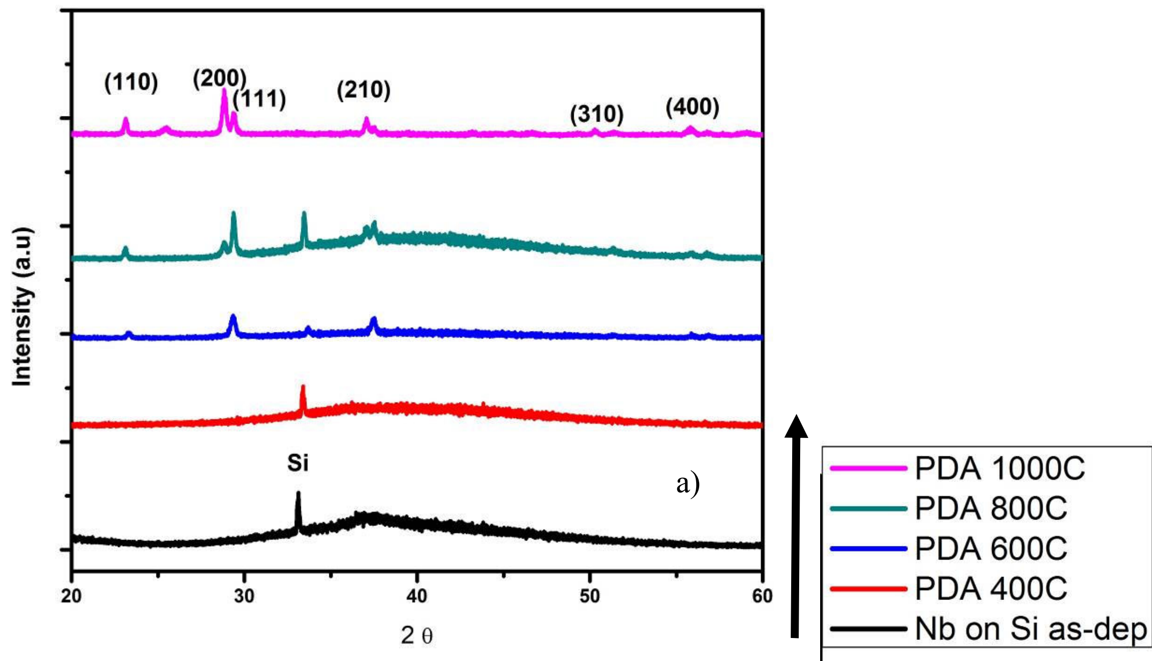


Figure 69: Fractal dimension as a function of annealing temperature. (square) represents data for Nb/Si and (circle) represents data for Nb/$SiO_2$.

This observation is also confirmed by the X-ray diffraction (XRD) analysis. From Figure 70, a phase change can be seen as the annealing temperature is increased beyond 600 $^oC$. The as-deposited samples are amorphous as observed in Figure 70, where only Si peaks are present. However, at annealing temperatures of 600 $^oC$ and above, additional peaks corresponding to hexagonal phases of niobium silicide appear as a consequence of the onset of silicidation. The different phases were identified from JCPDS PDF# 03-065-3599.



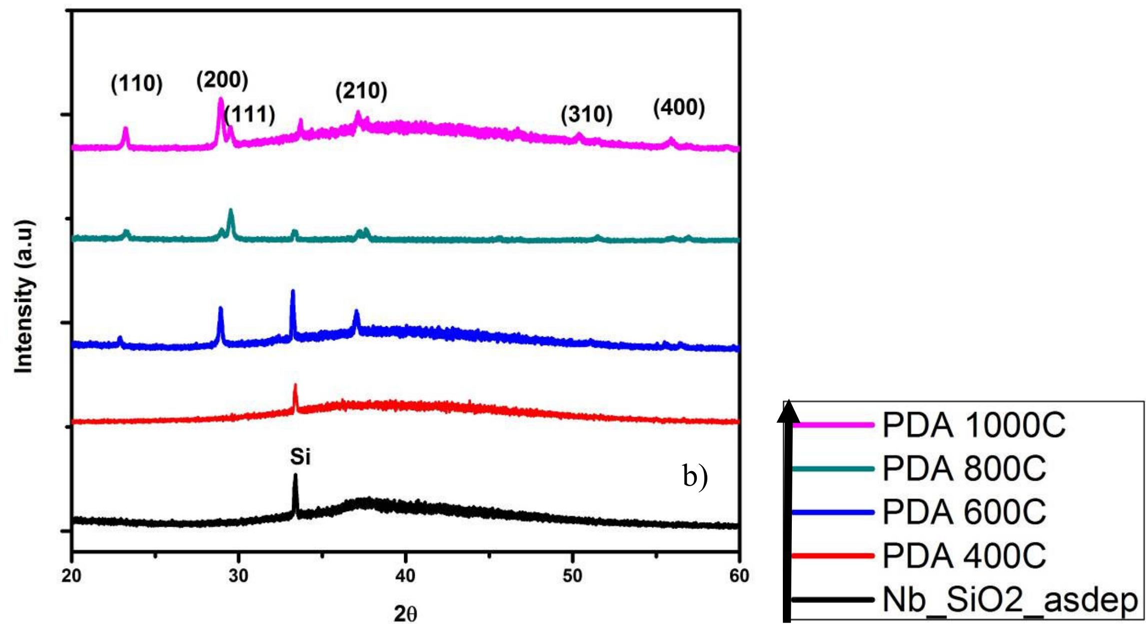



Figure 70: XRD Plot as a function of temperature. a) Nb/Si as a function of temperature. b) Nb/$SiO_2$ as a function of temperature.

In Figure 71, the XRD data for the Nb/Si sample annealed on 1000 ºC is shown. The resulting XRD data corresponds to the hexagonal phase of $Nb_5Si_3$ with a preferential growth in the (200) direction. On the sample annealed at the highest annealing temperature phases of $NbSi_2$ were also detected.

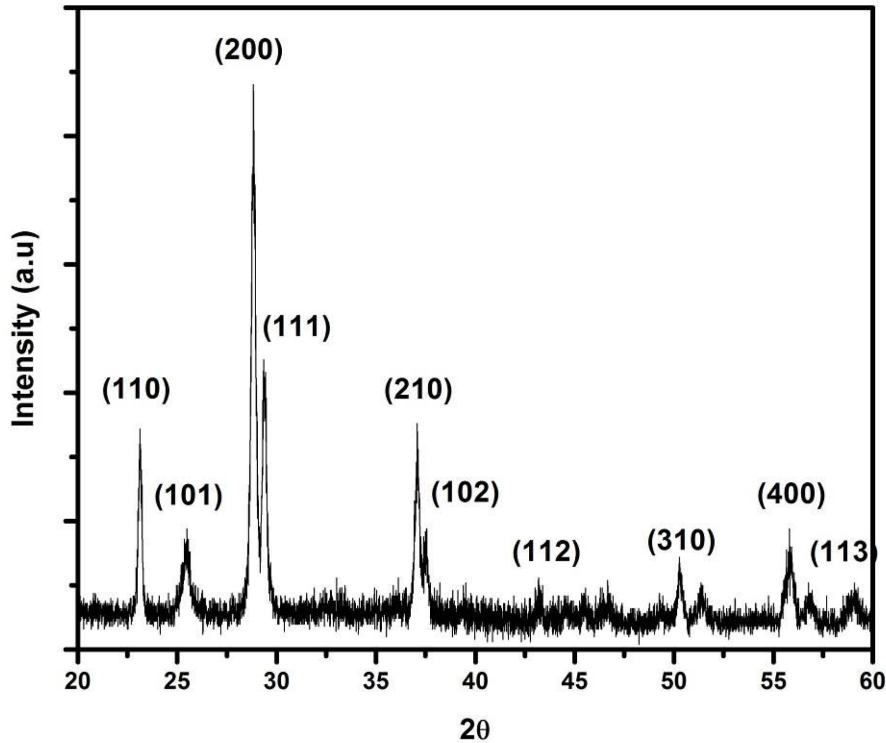



Figure 71: XRD plot of Nb/Si annealed at 1000 °C. The silicidation takes place with a growth preferency in the (200) direction.

To complete the characterization, the sheet resistance of all the samples of Nb on Si and Nb on $SiO_2$ were measured at room temperature. Figure 72 shows the sheet resistance data for both Nb/Si and Nb/$SiO_2$ at different annealing temperatures. The sheet resistance follows the same trend for both sample types: the resistance increases gradually for as-deposited samples and those annealed at 400°C and 600 °C. Moreover, the resistivity of the sample annealed at 600 °C increases by 4 orders of magnitude for Nb/Si and 5 orders of magnitude for Nb/$SiO_2$ when compared to the lower annealing temperatures. Additionally, the sheet resistance seems to somewhat saturate for samples annealed at or greater than 600°C. This is likely to be indicative of the fact that at higher temperatures all of Nb has been consumed. Thus the low resistivity Nb has been all exhausted and transformed into a high resistance silicide. The results agree with our previous conclusion from the characterization data showing that the silicidation seems to be significantly starting at an annealing temperature above 600 °C, since the resistance of the samples annealed at 600 °C increases by at least 4 orders of magnitude when compared to the resistance of those samples annealed at 400 °C. The difference between Si and $SiO_2$ substrates is again the

limited supply of Si needed for the silicidation reaction with Nb, which may result in non-stoichiometric niobium silicide films.

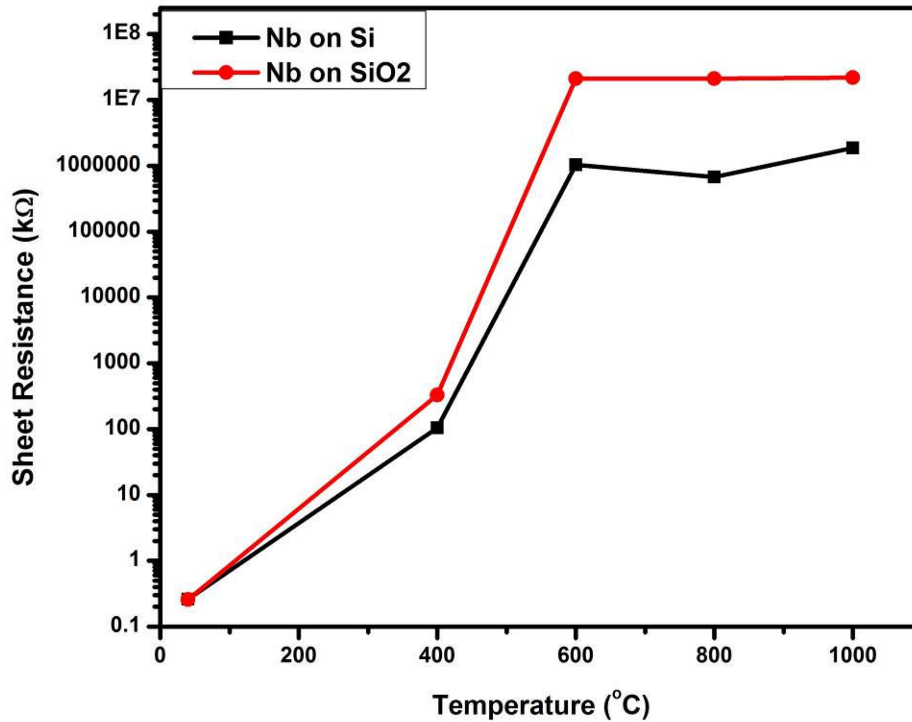



Figure 72: Annealing Temperature dependence of the Sheet Resistance of Nb/Si and Nb/$SiO_2$. (circle) represents the data for Nb on $SiO_2$ and (square) represents data for Nb on Si.

### 6.1.4 Conclusion

Amorphous Nb thin films were deposited by PVD on bare Si subtrates and on $SiO_2$ covering Si wafers at a temperature of 50º C. Post-deposition annealing at temperatures above 600 °C resulted in silicidation. According to a fractal analysis the as-deposited niobium silicide films followed the Stranski-Krastanov growth mode. As the silicidation starts, the growth mode transitions to the Volmer-Weber growth model. The resulting XRD data corresponds to the hexagonal phase of $Nb_5Si_3$ with a preferential growth in the (200) direction. Additional peaks of $NbSi_2$ are detected when the Nb/Si sample is annealed at 1000 ºC. In both cases, the sheet resistance of the resulting film increases with increasing annealing temperature up to 600 °C, after which it saturates when the available Nb is fully consumed.

## Chapter 7: Conclusion and Future Work

Silicon structures were fabricated to characterize and understand the diffusion of phosphorus and boron dopants in bulk compared to nanostructures. The nanostructures fabricated resemble closely the structures of Si novel transistor devices such as the FDSOI MOSFET, the triple gate SOI MOSFET and the wrap around gate NW MOSFET. Lateral diffusion in these nanostructure MOSFETs must be precisely controlled to predict device behavior and enable further scaling of transistors. Second order effects observed in shorter channel transistors correlate strongly with the source and drain doping and the redistribution of dopants around the channel.

For phosphorus, both electrical measurements and simulation results agree in that the segregation effects at the Si-$SiO_2$ interfaces are a root cause of the retardation of lateral diffusion in nanostructures. In fact, because of the segregation coefficient larger than 1, phosphorus impurities accumulate at the Si side of the interface thus retarding the diffusion front in the core of the Si channel. The accumulation of these phosphorus atoms at the interface for long annealing time and increasing concentration could result in their electrical deactivation such as in the case of the nanowire where the oxide is around its entire surface. The surface to volume ratio is much larger in nanostructures than in bulk which also plays an important role on how the segregation effect impacts the diffusion. In terms of transistor performance, it would be expected that lateral diffusion would improve in the novel device structures for the case of the n-channel where Si-Silicon oxide interface is present.

For boron, the structures have already been fabricated and the pre-deposition and analysis remains to be done. It is known that the segregation coefficient of boron in a Si-$SiO_2$ system is less than 1. Thus, Boron impurities are depleted at Si side of the Si-$SiO_2$ interface. In this case, $SiO_2$ might enhance the diffusion of Boron and could result in a faster lateral diffusion in nanostructures.

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