CHAPTER 5

CHARGE CONTROL OF THREE-PHASE BUCK RECTIFIERS

5.1 Introduction

As discussed in the previous chapters, the three-phase buck, or buck-derived PWM rectifier (referred to as a buck rectifier hereafter) is a viable candidate for applications where power factor correction (PFC) is required, or a variable output voltage, good output regulation and fast dynamic response are needed [A1]-[A8]. The circuit diagram of the buck rectifier with a single-stage LC input filter is redrawn in Fig. 5.1 in its simplest non-isolated form.

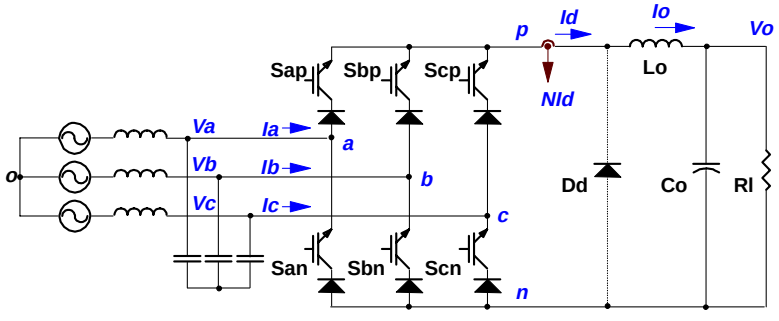


Fig. 5.1. Three-phase buck PWM rectifiers.

Theoretically, the input phase currents of a buck rectifier can be shaped sinusoidally just by the sensing of the input phase voltages and its average output voltage regulated by the voltage-mode control. However, some forms of current-mode control is still preferred for various reasons. As in dc-dc converters, current-mode control can achieve faster system dynamics and better system damping. It also facilitates the implementation of over-current protection and multi-converter paralleling.

As disclosed in Chapters 2 for the non-isolated case and in Chapter 4 for the isolated case, a particular problem of duty-cycle distortion arises in the soft-switched buck rectifiers. In these cases, the duty-cycle distortion is incurred on only one of the two active duty-cycles in a switching cycle because of the intervention of the soft-switching action. With the active phases rotate with the 60^o sectors of the input voltages, the duty-cycle distortion also occurs on different phases, and causes input currents to deviate from their sinusoidal form, increasing output voltage ripple and deteriorating the rectifier performance. Hence, a control scheme with the capability to accurately control the average current of *each* phase is needed to counter this kind of duty-cycle distortions. This leads to the thinking of resorting to the average current-mode control which is widely used in the control of various PFC circuits.

As shown in Fig. 5.1, various currents in the buck rectifier are available to implement current-mode control. The most popular way is to sense the dc-side inductor current I_d to implement average current-mode or PI control [A2] [A11] [A31]. An apparent shortcoming of this scheme is that only the average output filter inductor current is controlled, while the input phase currents may still contain distortions arising from, for example, the switching frequency ripple of the inductor current. Basically, the two active duty-cycles are still generated directly from a common modulation index which is in turn derived from the

control loops. Therefore, it falls short to correct the distortions in the soft-switched buck rectifiers.

DSP-based algorithms can be a way to tackle the problem. However, considerable control hardware resources and software efforts are necessary. It is also practically difficult to refine the algorithm to cover the whole operating manifold of a practical rectifier system [B8].

It has been known that charge control or *instantaneous average current mode control* is suitable to control the average value of a unidirectional current with any shape, especially a pulsating current where other current-mode controls either fail or behave poorly [F4]-[F10]. For that reason, it appears an ideal candidate to the problems associated with the soft-switched buck rectifiers and is also possible to provide a rather generic and low-cost control means for any buck or buck-derived rectifier system. Because the charger controller is reset in every switching cycle, it is easy to guarantee the smooth transition between the 60^{o} sector boundaries of the input phase voltages.

In this chapter, the basic concept of the charge control for dc-dc converters is extended to the control of three-phase buck PWM rectifiers. The resulting scheme directly shapes the individual input phase current to track the corresponding input phase voltage, realizes six-step PWM, and is very simple to implement and easy to integrate. The control scheme for a non-isolated buck rectifier is developed in Section 5.2, the implementation and design guidelines are discussed in Section 5.3, the simulation and experimental results are given in Section 5.4, and Section 5.5 is devoted to the extension of the scheme to other buck-derived rectifier systems.

5.2 Concept of Charge Control of Three-Phase PWM Rectifiers

5.2.1 Charge Control of dc-dc Converters [F4]-[F5] [F7] [F9]

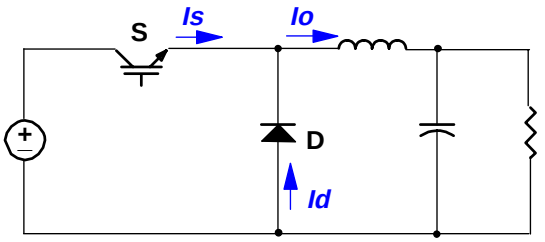
The basic concept of charge control for dc-dc converters is illustrated in Fig. 5.2 for the case of a simple buck converter. The charge controller consists of a resettable integrator, a PWM clock which gives out a fixed frequency signal, C_{lk}, a comparator Comp, and a RS register RS in Fig. 5.2(b). Theoretically, either the switch current, I_s, or the diode current, I_d, can be sensed to feed the integrating capacitor C. If the switch current is sensed, the switch is turned on by the PWM clock, and when the integrated charge, CV_{Ct}, reaches the preset reference value, I_r, which is usually given out by the output voltage regulation loop, the comparator output toggles, the switch S is turned off, and trailing-edge PWM results. At the same time, the integrator is reset by the reset switch Sr, and prepared for operation for the next cycle as shown in Fig. 5.2(b) and (c). If the diode current is used to drive the integrator, leading-edge PWM is a natural consequence.

The integrator voltage at end of the on-duty-cycle T_1 is

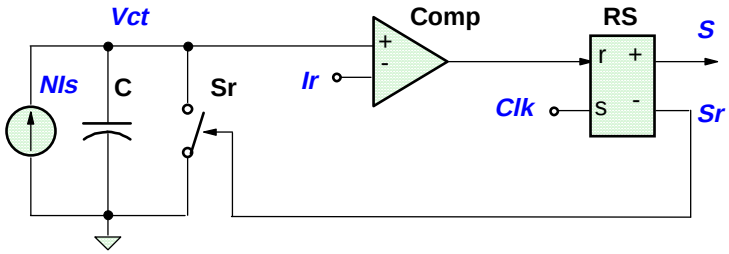
$$V_{ct}(T_1) = \frac{Q}{C} = \frac{1}{C}\int_0^{T_1}(NI_s)dt = \frac{NT}{C}\langle I_s\rangle = I_r, \tag{5.1}$$

where $$\langle I_s\rangle = \frac{1}{T}\int_0^{T_1} I_s dt = \frac{Q}{NT} = \frac{C}{NT}I_r \propto I_r \tag{5.2}$$

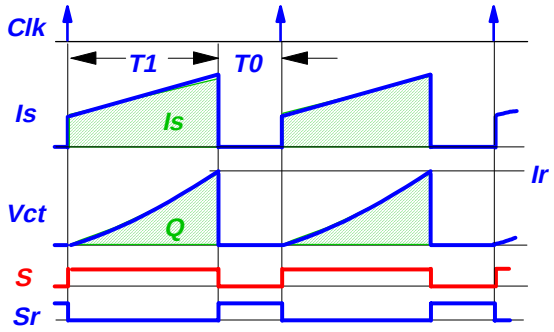
is the average switch current in a PWM cycle, N the current scaling factor in the sensing circuit, Q the charge accumulated on the integrating capacitor at T_1, and T the PWM period. It is clear from (5.1) and (5.2) that the average switch current in a PWM period is exactly proportional to the charge accumulated on the integrating capacitor and the reference current. Consequently, the average switch current can be precisely controlled on a cycle-by-cycle basis.



(a) buck dc-dc converter.



(b) Charge controller.



(c) High-frequency operation waveforms.

Fig. 5.2. Charge control of buck dc-dc converters.

5.2.2 Charge Control of Three-Phase Buck Rectifier

For three-phase buck rectifiers, the input phase currents are pulsating. In order for the converter to draw balanced sinusoidal currents from a balanced set of sinusoidal input voltages, $V_\phi = [V_a, V_b, V_c]$, the average phase current $\langle i_\phi \rangle$ needs to be controlled such that

$$\left\langle i_\phi \right\rangle = \left[\langle I_a \rangle, \langle I_b \rangle, \langle I_c \rangle\right] = \frac{1}{R} V_\phi \cos\theta, \tag{5.3}$$

where $\theta = \angle(V_\phi, \langle I_\phi \rangle)$ is the displacement angle, and R is the equivalent loading impedance per phase. Assume that the converter loss can be neglected, then the output power P_o of the converter is

$$\begin{aligned} P_o &= (V_\phi, I_\phi) = \frac{1}{R}\Big(\sum_{i=a,b,c} V_i^2\Big)\cos\theta \\ &= \frac{3}{2}\frac{1}{R} V_m^2 \cos\theta = Const. \end{aligned}, \tag{5.4}$$

where V_m is the peak value of the input phase voltage. As a result, good output voltage regulation can be achieved with a fast outer voltage loop.

It is suggested in (5.3) that a simple way to shape the input current vector $\left\langle i_\phi \right\rangle$ is to directly control its average value to track its input voltage vector V_ϕ. This observation insinuates that charge control, which is best suited for average value control of a pulsating variable, can potentially be extended to furnish the required functions.

The input phase currents of the three-phase buck rectifier shown in Fig. 5.1 are a combination of its switch currents, as is the dc-side current I_d. But at any time, only one pair of switches, each from the upper and lower half of the bridge respectively, carry the current drawn from a particular phase. This leads to the conclusion that it is possible to sense only the dc-side current to decipher all the switch current information and control the corresponding switches to enforce the required average currents.

The resulting charge control scheme of three-phase buck rectifiers by sensing only the dc-side current I_d is illustrated in Fig. 5.3. It inherits the basic form and elements of the charge controller for dc-dc converters, but two current references and corresponding PWM modulators are incorporated. According to the six-step PWM principle for buck rectifiers,

in a PWM period, only two phase currents need to be controlled through two active duty cycles, denoted as T_1 and T_2 in Fig. 5.4(b), while the current of the third phase is naturally enforced. To take a 60° sector of an input line cycle, where $|V_a| > |V_b|$ or $|V_c|$ as shown in Fig. 5.4(a), as an example, only the lower switches of phase *b* and *c*, i.e. S_{bn} and S_{cn}, needs to be modulated, while S_{ap} of phase *a* can be on all the time. In the shaded 30° segment with $|V_c| > |V_b|$, if both of S_{bn} and S_{cn} are turned on by the PWM clock at the beginning of a PWM cycle as in Fig. 5.4(b), S_{bn} will not actually carry current because of the blockage of its series diode until at the end of T_1, when the integrated voltage V_{Ct} reaches the comparing level set by I_{r1} on Comp1 and proportional to $|V_c|$. At that moment, S_{cn} is turned off, and S_{bn} takes over the load current till the end of T_2, when V_{Ct} hits the comparing level set by I_{r2}, which is proportional to $|V_b + V_c|$, or $|V_a|$, and the integrator gets reset by the reset signal S_r from register RS2. As a result,

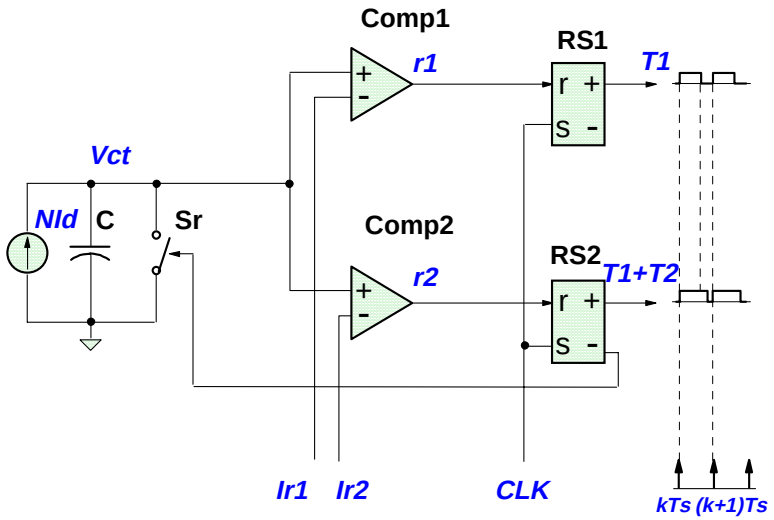


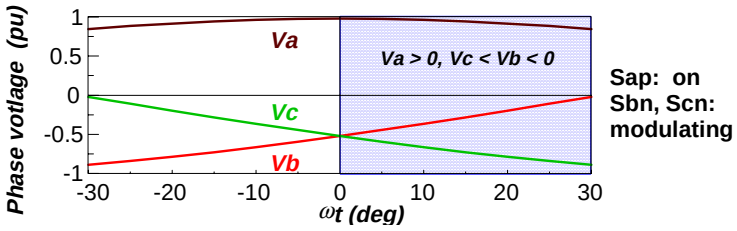
Fig. 5.3. Proposed charge controller of three-phase buck rectifiers.

$$\langle I_c \rangle = \frac{1}{T}\int_0^{T_1} I_d dt = \frac{Q_c}{NT} = \frac{C}{NT} I_{r1} \propto |V_c|, \tag{5.5}$$

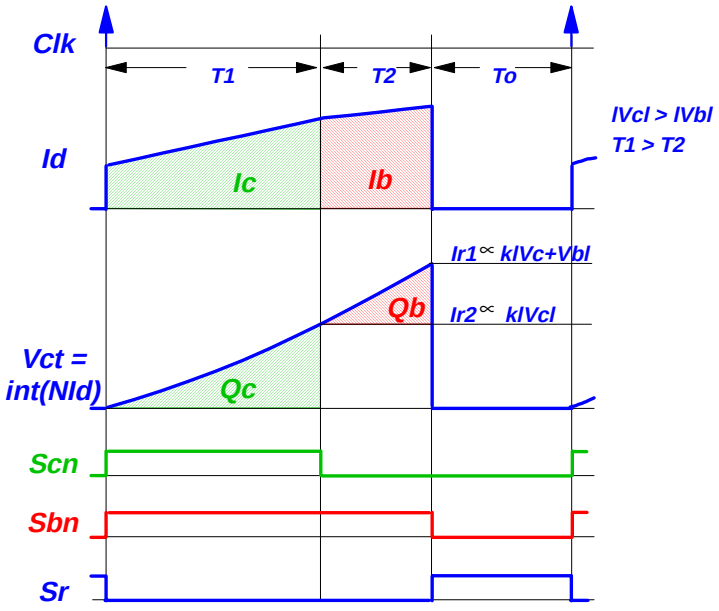
and $$\langle I_b \rangle = \frac{1}{T}\int_{T_1}^{T_1+T_2} I_d dt = \frac{Q_b}{NT} = \frac{C}{NT}(I_{r2} - I_{r1}) \propto |V_b|, \quad (5.6)$$

where Q_c and Q_b are the charges accumulated on the integrating capacitor during T_1 and T_2 respectively.

In the other half of the 60° sector in discussion, where $|V_b| > |V_c|$, the reference I_{r1} will be derived from $|V_b|$ and the first duty-cycle T_1 will be directed to S_{bn} accordingly.



(a) Input phase voltages in a 60° sector.



(b) High frequency operation waveforms.

Fig. 5.4. Operation principles of charge control of buck rectifiers.

It can be seen that because of the existence of an integrator in the current control loop, the noise immunity of the scheme is excellent, so it is well suited for high power applications. Also, the feature that the controller resets in every PWM cycle is very beneficial in order to achieve smooth transition between the 60° sector boundaries within a line cycle.

Figure 5.5 shows the block diagram to generate the current reference signals, I_{r1} and I_{r2}. The absolute value of the sensed input phase voltage V_ϕ is taken through the ABS block, and then fed into two multiplexers MUX1 and MUX2. The segment information of the input phase voltages, *Seg*, is composed of the signs of the input phase and line voltages, and is used to select the appropriate phases to generate the current references according to the rules that

$$\begin{aligned} V_1 &= Med\{|V_i|, i \in (a,b,c)\}, \\ V_2 &= Max\{|V_i|, i \in (a,b,c)\}, \end{aligned} \tag{5.7}$$

where *Med* represents the function to take the medium value among the three rectified phase voltages. V_1 and V_2 are then multiplied by the control voltage V_{con}, usually from the output voltage regulator in the case of the rectifier, to obtain the reference currents.

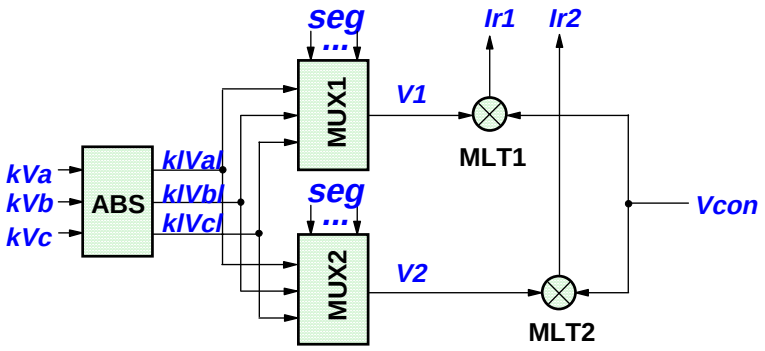


Fig. 5.5. Average phase current reference generation.

5.3 Implementation and Design Guidelines

The proposed charge control concept for buck rectifiers is simple to realize. It requires only one phase of PWM clock, and only one current needs to be sensed, while no carrier signals, which are normally a mandate in other carrier-based PWM and control schemes, are required. The complete system block diagram is shown in Fig. 5.6. Besides the charge control and reference generation blocks discussed above, the input voltage identifier generates the 30° segment and 60° sector signal *Seg* from the sensed input voltages. The signal is used to drive both the reference generation block and the PWM signal distribution logic block. The latter converts and steers the basic PWM signals T_1 and $T_1 + T_2$ to the appropriate switches. The output voltage compensator has the same function as that in buck rectifiers with other control schemes, and the only difference is that the compensator structure can be simpler and the bandwidth can be widened compared to that with only voltage-mode control.

Besides the appropriate signal scaling, design of the charge controller of buck rectifiers is as simple as that of a dc-dc converter. The criteria to select the integrating capacitor C is to ensure the integrator and the PWM modulator will not saturate under steady-state operation with low input line and full load, or full output power. Assume the converter is designed for a maximum modulation index *m*, in low-line and full load operation, and the switching cycle ripple current can be neglected, then it can be shown that the maximum voltage on the integrating capacitor, V_{ct}^{max} happens in the middle of a 60° sector, i.e. at $\omega t = 0^{o}$ for the case shown in Fig. 5.4(a), and can be derived as

$$V_{ct}^{max} = V_{ct}(T_1 + T_2)\Big|_{\omega t=0^o} = \frac{2N}{C}\int_0^{T_1} I_d dt$$
$$\approx \frac{2N}{C}\frac{mT}{2} I_d = \frac{NmT}{C}\frac{P_o}{V_o} = \frac{2NT}{3C}\frac{P_o}{V_m^l \cos\theta} \quad , \tag{5.8}$$

where $V_o = \frac{3}{2} V_m^l \cdot m\cos\theta$ (5.9)

is the regulated output voltage, V_m^l the peak value of the low-line phase voltage, and T the PWM period. From (5.8), it follows that

$$C \geq \frac{2NT}{3V_{ct}^{max}}\frac{P_o}{V_m^l \cos\theta} . \tag{5.10}$$

To take a design example, N = 1/1000, m = 0.9, T = 20 μS, P_o = 5 kW, V_{ct}^{max} =12 V, V_ϕ = 176 - 264 V (for a nominal input of 220 V with variation), then V_o = 300 V, and C = 28 nF.

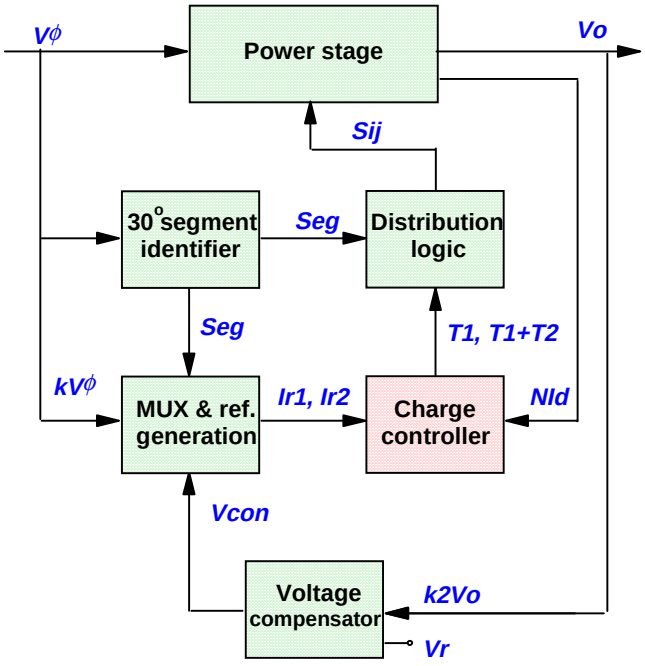


Fig. 5.6. System block diagram of charge controlled buck rectifiers.

One subtle issue associated with charge control is the subharmonic oscillation which may happen at light load when the output filtering inductor current, for the case of buck derived topologies, becomes discontinuous, or in other words, the circuit runs into discontinuous mode (DCM). But unlike the case of the single-phase PFC circuit, where the circuit has to run into DCM, independent of the load level, around the zero crossing area of the input current twice a line cycle, zero-crossing of phase currents in a three-phase buck rectifier does not present any problem simply because the output inductor current is still in CCM. When the load becomes really light, and DCM inductor current happens, subharmonic oscillation of input phase current may occur. However, because the phase current and the power processed under the circumstance is very low, it has no detrimental effect on the circuit operation, and is tolerable.

In the isolated buck rectifier case, the subharmonic oscillation becomes an issue because it may lead to the flux unbalance of the transformer. A simple corrective measure is to superpose a fictitious current ramp signal on the sensed dc-rail current only when the load current is lower than certain level and the circuit runs into DCM.

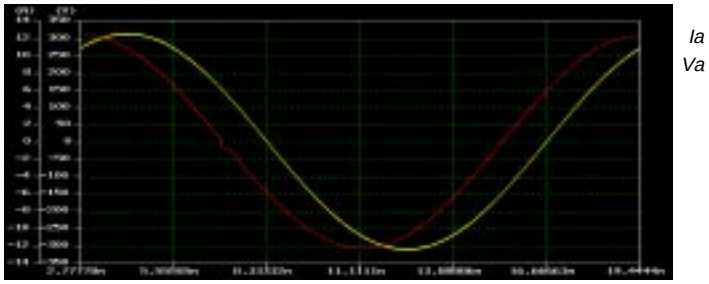
5.4 Simulation and Preliminary Test Results

5.4.1 Simulation Results

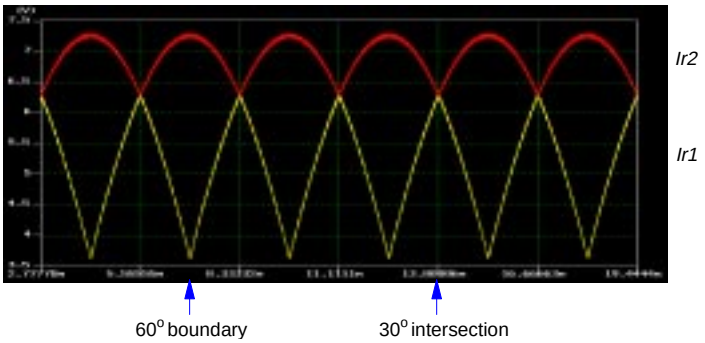
The buck rectifier system as shown in Fig. 5.6 without the outer voltage regulation loop is simulated in the circuit simulator SABER. Figure 5.7 (a) through (d) shows the simulation results for the case of V_ϕ = 220 V, and P_o = 3 kW. The clock frequency is set to 50 kHz. The dc-side filtering inductor is 300 μH, and the output filter capacitor is 40 μF loaded by a 9 Ω resistive load. A two stage LC filter with a parallel damping branch and

total shunt capacitor of 50 μF, and series inductor of 400 μH per phase is connected at the input to smooth out the pulsating phase current the rectifier draws.

Figure 5.7(a) shows the simulated phase current before the filter. Phase current with very low harmonic distortion is achieved. Although not necessarily so, the current reference of the buck rectifier is derived to be in phase with the phase voltage. As a result, the resulting phase current is leading the phase voltage because of the capacitive current component in the filter capacitors.

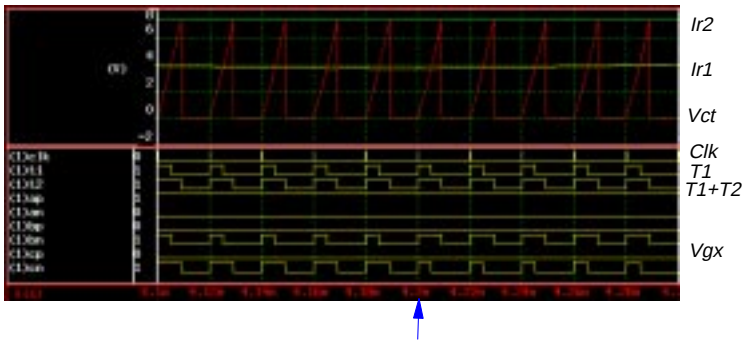


(a) Phase voltage and phase current before the two-stage filter.

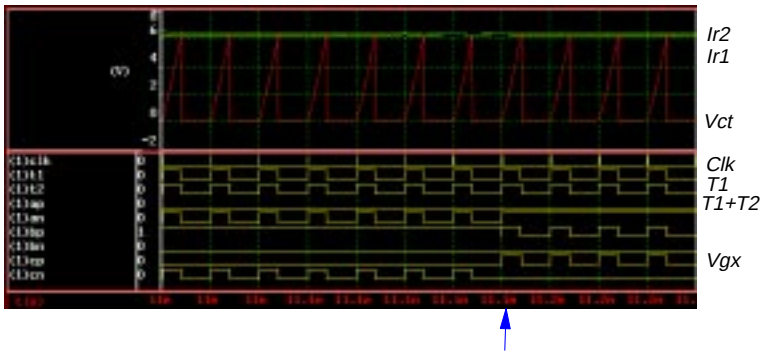


(b) Average phase current references.

Fig. 5.7. Simulation results.



(c) High-frequency waveforms in the middle of a 60° sector when the two active duty-cycles are equal. The arrow indicates the intersection instant.



(d) High-frequency waveforms at the boundary of a 60° sector when one of the two active duty-cycles shrinks to zero. The arrow indicates the sector boundary.

Fig. 5.7(Continued). Simulation results.

The two current references I_{r1} and I_{r2} in a line cycle with frequency of 60 Hz are shown in Fig. 5.7(b). It can be seen that the transitions between 60° boundaries and 30° intersections in the middle of a sector are always smooth, and the waveforms are consistently repeating for every 60°. Figure 5.7(c) and (d) further shows the details during these transitions.

In Fig. 5.7(c), it can be clearly seen that in the middle of a sector when the two active duty-cycles become equal, the basic PWM signals, T_1 and T_1+T_2, maintain their continuity,

but are reassigned to the two modulating switches, S_{bn} and S_{cn} in this case. The transition between 60° sectors is shown in Fig. 5.7(d) when T_2 shrinks to zero, and the other duty cycle T_1 reaches its maximum. Active switches in modulation also change. There are not any enormity seen for any of the signals in the controller during all these transitions.

5.4.2 Preliminary Experimental Results

A prototype of the complete controller together with the power stage as shown in Fig. 5.6 has been designed and built to verify the control scheme. The PWM clock frequency is 48 kHz derived from a 12.288 MHz oscillator. All the logic functions contained in the 30° segment identification, charge controller, and distribution logic blocks are implemented in a small programmable logic device (PLD). The dc-side current I_d is sensed with a Hall current sensor module with a turns-ratio of N = 1/1000.

Shown in Fig. 5.8 are test results with two dc inputs to mimic the case corresponding to one particular point of an ac input line cycle, i.e. $\omega t = 15^\circ + 180^\circ$ referred to Fig. 5.4(a). In this case, the emulated input phase voltage V_ϕ = 110 V, and accordingly, V_a = -164 V < 0, and V_c = 120 V > V_b = 44 V > 0. Therefore, the corresponding two dc input voltages are V_{ca} = 284 V, and V_{ba} = 208 V (referred to in Fig. 5.1). S_{bp} and S_{cp} are modulating while S_{an} is kept on all the time. The output voltage is 180 V and output power is 1.1 kW. It can be seen that both modulating switches are turned on at the same time by the PWM clock, but the small duty-cycle T_2 does not actually start until the big one, T_1, ends with the turn-off of S_{cp}, as is clear on the waveform of V_{pn}.

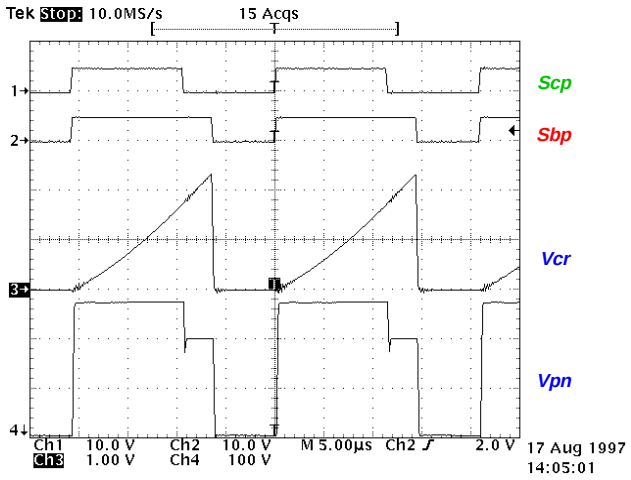


Fig. 5.8. Preliminary experimental results.

5.5 Extension and Applications

The charge control concept proposed in this paper is actually generic to multiphase buck rectifiers. Discussed thus far is only its simplest form, which corresponds to six-step PWM with concentrated or lumped freewheeling (zero) duty-cycle, i.e. in a PWM period, the two non-zero duty-cycles are always consecutive, and the zero duty-cycle is not distributed in between. With a few revisions, the concept can be extended to realize different six-step PWM schemes, such as center-aligned PWM. Moreover, it can also be easily adapted to various three-phase buck rectifier topologies.

5.5.1 Charge Control of Three-Phase Non-Isolated Buck Rectifier without a Freewheeling Diode

In some applications, the extra dc-side freewheeling diode in Fig. 5.1 does not exist, as is usually encountered in a current-linked rectifier/inverter system. In this case, the freewheeling current flows through the rectifier bridge branches, and the dc-rail current

becomes continuous. However, the phase current information can still be extracted from the dc-rail current in the same way as discussed above, and theoretically no any modification needs to be made.

During the freewheeling period, the sensed dc-rail current, which is usually a current source in nature, is by-passed to the reset switch, and is thus shorted to ground. Thus, it will not interfere with the operation of the charge controller. The only difference is that without the freewheeling diode the rectifier bridge is usually controlled to be normally on, instead of normally off, to reduce the conduction loss, so the pulse distribution logic needs to be modified accordingly.

In the case of soft-switched buck rectifiers, PWM schemes with lumped zero duty-cycle are preferred because the auxiliary commutation circuit needs to be activated once in a PWM period to achieve soft-switching. Unfortunately, that soft-switching event usually modifies one of the two active duty-cycles, and contributes to the distortion of input phase currents. With the charge control scheme proposed in this paper, this problem is solved because the average current of each phase is controlled individually, and the duty-cycle is instantaneously adjusted to achieve the commanded average phase current.

5.5.2 Charge Control of Three-Phase QSS Isolated Buck Rectifier

The family of three-phase QSS isolated buck rectifiers [B6] - [B8] incorporates a front-end six-switch buck bridge with a full-bridge dc-dc converter with phase-shift control and various zero-voltage/zero-current switching (ZVZCS) schemes, while the dc-link filtering elements are eliminated. Flux balance on the isolation transformer is achieved by directing the PWM signals to each pair of switches in diagonal positions in the dc-dc full-bridge part of the converter for the two consecutive PWM cycles. In this case, the pulsating

dc-link current can still be sensed to implement the charge control scheme. The only necessary revision is again on the distribution logic part. A modular two counter can be used to toggle the PWM pulses between the two mentioned pairs of bridge switches. Similar to the situation of soft-switched non-isolated buck rectifiers, one extra benefit of the family of converters with charge control is that the potential duty-cycle distortion to at least one input phase because of the ZVZCS operation can be easily corrected.

5.5.3 Charge Control with Center-Aligned Six-Step PWM

The PWM scheme which distributes the zero or freewheeling duty-cycle equally between the two non-zero duty-cycles is usually called a center-aligned six-step PWM. With this PWM scheme the peak-to-peak switching frequency ripple current on the output inductor and the associated losses are minimized [8]. To adapt the proposed charge control concept to this PWM scheme, two phases of triangular carriers with 180^o phase shift are needed.

As illustrated in Fig. 5.9 for the example corresponding to the case in Fig. 5.4(a), the absolute values of the scaled-down input phase voltages, $k|V_b|$ and $k|V_c|$ in this case, are directly compared to the triangular carriers, V_{cr1} and V_{cr2}, respectively, to determine the turn-on instant of the modulating switches, i.e. S_{bn} and S_{cn} in this case. When the carrier intersects the corresponding phase voltage reference and becomes lower, the modulating switch for that phase is turned on, and the integrator in the charge controller starts to integrate. When the integrator voltage V_{Ct} reaches the average input phase current reference as before from the sensed phase voltage and the output voltage feedback loop, the switch is turned off, and the controller resets

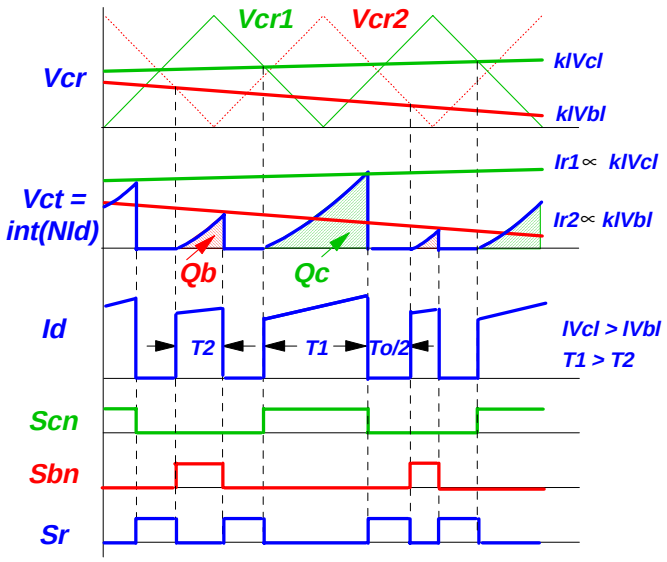


Fig. 5.9. Center aligned PWM of buck rectifier with charge control.

itself. Next, the modulating switch for the other active phase repeats the same process. As a result, in a carrier cycle, the integrator is activated and reset twice, and the zero duty-cycle, T_0, is equally distributed in the two non-zero duty-cycles, T_1 and T_2, while the average phase currents are precisely controlled.

5.6 Summary

The concept of charge control of three-phase buck PWM rectifiers is proposed in this chapter. It controls precisely the average input phase currents to track the input phase voltages by sensing and integrating only the dc rail current, realizes six-step PWM, and features simple implementation, fast dynamic response, excellent noise immunity, and is easy to realize with analog circuitry and integrate.

One particular merit of the scheme is its capability to correct any duty-cycle distortion incurred on only one of the two duty-cycles which often happens in the soft-

switched buck rectifier topologies because of the intervention of the soft-switching action. Another merit with this scheme is the smooth transition of the input currents in the 60^o sector boundaries because the charge controller is always reset in every switching cycle.

The concept, implementation, and design guidelines are addressed. Simulation and preliminary experimental results show that smooth operations and high quality sinusoidal input currents in the full line cycle can be achieved. The proposed control scheme can be easily extended to realize different PWM patterns, and to control various three-phase buck rectifier-based systems, including the QSS isolated ZVZCS buck rectifiers proposed in the previous chapter.