

Design of 1.7 kV SiC MOSFET Switching Cells for Integrated Power Electronics Building Block (iPEBB)

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ABSTRACT

The need for high-density power electronics converters becomes more critical by the day as energy consumption continues to grow across the world. Specifically, the need for medium-voltage (MV) high-density converters in power distribution systems, electric ships, and airplanes become more critical as weight and space becomes more a premium. The limited space and footprint require new packaging technologies and methods to develop an integrated power converter.

The advancement of wide-bandgap (WBG) devices like silicon carbide (SiC) allows converters to have higher power and faster switching... To benefit from these devices, the packaging of the converter needs to be carefully considered. This thesis presents the design of a 250 kW integrated power electronics building block (iPEBB) for future electric system applications. This work explores the common substrate concept that would serve as the electrical, thermal, and mechanical foundation for the converter. State-of-the-art organic direct-bonded copper (ODBC) is explored to serve as the material foundation for the common substrate. Multi-domain simulations are used to design the integrated SiC bridges to achieve a power loop inductance of 3.5 nH, a maximum temperature of 175 °C, and a weight of 16 kg. ODBC and silicon nitride switching cells are packaged and analyzed in order to see the benefits on a multi-layer design as well as determining electrical and thermal trade-offs. The insights gained from hardware testing will help in the redesign and refinement of the iPEBB.

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GENERAL AUDIENCE ABSTRACT

This thesis presents the design of an integrated power electronics building block (iPEBB) for high-density systems. The PEBB concept allows for modular converters that can perform various power conversions. The design begins with exploring state-of-the-art substrates that will serve as the foundation for the iPEBB. Due to the integrated design, the substrate plays a vital role in the thermal, electrical, and mechanical performance, and contributes to the weight and reliability of the iPEBB. State-of-the-art organic direct-bonded copper (ODBC) substrates and multi-layer silicon nitride substrates are explored in this work. The ODBC is used to develop a common substrate for the converter, which allows for a high level of integration between different SiC half-bridges. Switching-cell prototypes based on the ODBC and multi-layer silicon nitride are fabricated to provide insight into the electrical and thermal performance of different substrates. This information will aid in the further redesign and refinement of the iPEBB concept.

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Chapter 1 Introduction

1.1 Background

Modular, medium-voltage (MV) converters have grown in popularity due to their ability to be scaled to higher voltage and current ratings and their reduced production and maintenance costs [1]. In the past two decades, the power electronics building block (PEBB) has become a popular converter design concept due to its ability to reduce costs and improve reliability [1]. The PEBB concept was originally proposed by the Office of Naval Research (ONR) in 1997 for future electric ships [2]. Since then, many versions and variations of PEBBs have been developed for various industries and applications. PEBBs seek to integrate the fundamental components, such as power semiconductor devices, gate drivers, magnetics, and capacitors, to create flexible power converters that can be used in a variety of applications. The PEBB concept allows for each PEBB converter to be stacked in parallel or in series in order to achieve higher current and voltage ratings. The PEBB concept is especially attractive since a universal converter design can be used to conduct various power conversions, which helps reduce production and maintenance costs.

Some early PEBBs were based on the three-level neutral-point clamped (3L-NPC) topology and the five-level neutral-point clamped (5L-NPC) topology using insulated gate bipolar transistor (IGBT) devices [3][4]. But silicon devices have limitations in terms of voltage and temperature ratings that can limit the performance, power density, and modularity of PEBBs. This limitation is especially acute in applications such as electric ships, airplanes, etc. where weight and space are critical. Many MV Si-based PEBB designs tend to be bulky and to require some form of rack-level design to implement. The reduced

power density and increased volume deteriorates the fundamental benefits of a modular converter design that the PEBB champions. On the other hand, if new technologies make it possible to increase the power density while limiting the footprint and weight of PEBBs for on-board power systems, it will allow for a reduction in overall costs of transportation and renewable energy applications.

The advancement of wide-bandgap (WBG) technologies in the past few years has opened new frontiers for modular, MV converters. WBG devices such as silicon carbide (SiC) have a higher switching speeds, higher breakdown voltages, and higher operating temperatures than traditional silicon devices [5]. This recent advancement in semiconductor technology has enabled high-density, fast switching converters that can be implemented in various power systems and renewable energy grids. With the commercialization of WBG technology, PEBBs can replace Si IGBTs with cost-effective SiC metal-oxide semiconductor field-effect transistors (MOSFETs). WBG devices are able to switch five times faster with one-fifth the switching losses of IGBTs having similar ratings. By leveraging new WBG devices, new possibilities of a light weight, MV PEBB are possible. Hybrid IGBT / SiC based PEBBs have recently been explored as a bridge between the two technologies. Some recent demonstrations of PEBBs include a 100 kW, 28 kHz, hybrid Si-IGBT/SiC- MOSFET three-level T-type PEBB with a power density of 27.7 kW/l.

But there are still many fundamental roadblocks that limit wide scale implementation of WBG devices, including thermal and EMI concerns. Although SiC devices offer higher switching speeds than Si devices, the device switching losses and thermal concerns are scaled up along with it. The high heat flux underneath SiC makes

effective cooling systems critical to the viability of SiC-based PEBBs. Furthermore, with higher switching frequencies, the dv/dt will be higher and cause electromagnetic interference (EMI) related issues. Critical trade-offs and mitigation strategies must be implemented for a SiC-based PEBB.

To explore the implementation of WBG devices, various SiC-based PEBBs have been demonstrated in recent years using different topologies. A 100 kW, 100 kHz SiC-based H-bridge PEBB, named the PEBB 1000, has recently been demonstrated (Figure 1). The PEBB 1000 uses two 1.7 kV SiC half-bridge modules along with a state-of-the-art busbar, smart gate drivers, and magnetics to form a 5 kW/l modular, MV converter [6]. The PEBB 1000 was a critical step forward in the design of MV converters that are scalable. The PEBB 1000 attempts to be to be a self-contained unit that can serve as a least-replaceable unit (LRU) aboard electric ships... The PEBB 1000 is intended to be configured for a modular multi-level converter (MMC) design and uses the switching-cycle control (SCC) mode in order to minimize size of capacitors and passive components [7] [8] [9] [10] (Figure 2).

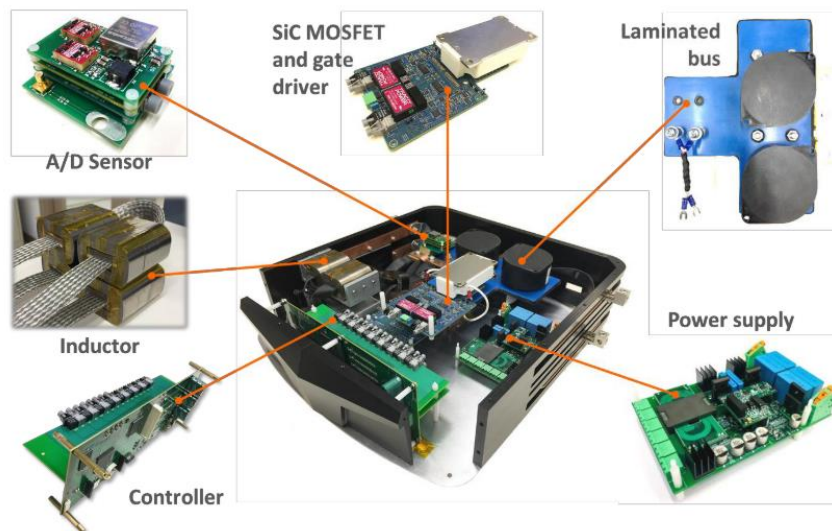


Figure 1: The internal structure of the PEBB 1000 with discrete components [7].

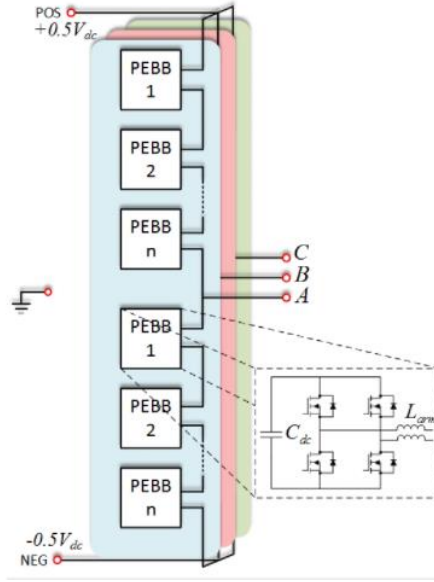


Figure 2: MMC stack up of H-bridge based PEBB 1000 [7].

Beyond the H-bridge, other SiC-based PEBB concepts allow for direct MV grid connection to serve a low-voltage (LV) load (Figure 3). A 100 kVA, 175 kHz PEBB was designed with a high-frequency MV solid-state transformer (SST) to provide galvanic isolation in the converter [11]. SST-based PEBBs are of great interest to researchers because they offer the ability to build a variety of static power conversion equipment. The challenge with SSTs involves reduction in size of the magnetics in order to achieve a higher power density.

The three H-bridges that form the SST-based PEBBs are packaged with TO-268 1.7 kV SiC MOSFETs on an insulated metal substrate (IMS). A variation of the design, using two H-bridges on either side of a SST transformer, is presented in [12]. It is designed with an open-frame rail structure that can be lifted by two people (Figure 4). Of special interest is the reduction of transformer size by increasing the switching frequency of the

converter. This increased switching frequency will be needed to reduce the size of passive components but will cause issues with EMI and thermal performance. To address this concern, work has been done to implement soft-switching techniques for the inner bridges that interface to the converter. The soft-switching techniques outlined in [13] will allow for the PEBB to switch at high frequencies while minimizing losses compared to hard-switching converters. In [14], the topology and the control methods are compared to show that a CLLC based control scheme for the inner DC-DC bridges is more practical than a dual active bridge (DAB). Figure 4 shows the design of a SiC-based PEBB that with a 250 kHz air-cooled transformer.

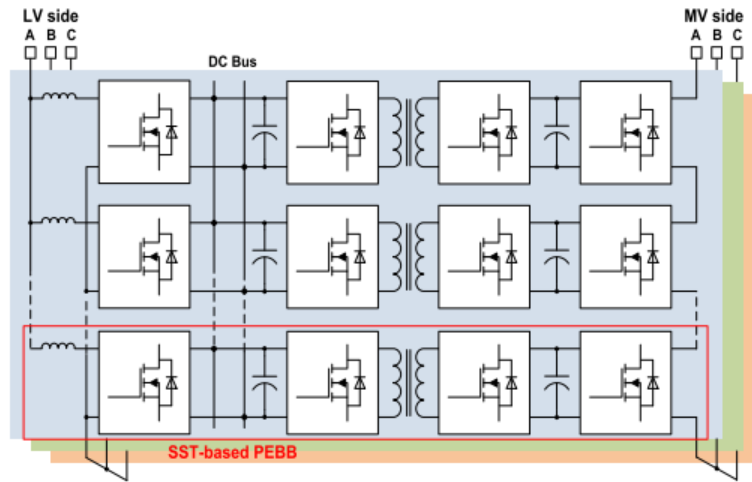


Figure 3: Example of a MV grid connection using SST-based PEBBs [12].

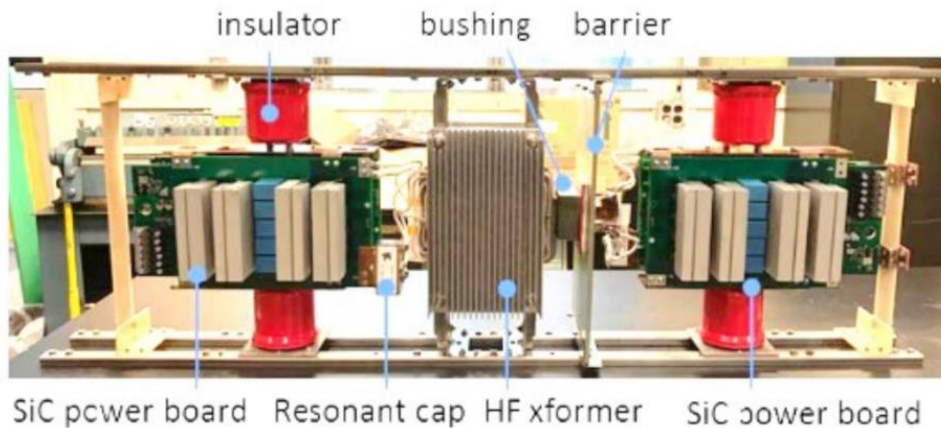


Figure 4: MV SST-based PEBB design [9]

The topology and the grid-level consideration are key to the development of the iPEBB. Thus far, SST-based converters have been slow to be adopted due to the fact that they are limited by the voltage and power ratings of the devices driving them. With the advancement of SiC devices, high-voltage and high-frequency PEBBS with SSTs can become a reality. The high-voltage, high-frequency capability of WBG devices make voltage and current regulation a possibility. The SST-based topology also allows support for a regulated DC bus that can be connected to microgrids and renewable energy sources [15].

The SST-based converters basically work by transforming 50/60 Hz AC voltage to a higher frequency, that is then stepped up or down by the SST and returned back to the 50/60 Hz needed by the load [16]. There are many different topologies and circuit designs to allow for isolated AC-AC conversion, which is of interest in applications such as microgrids [17]. There is a direct AC-AC topology that facilitates the SST to step down from high-voltage AC to low-voltage AC. The iPEBB is designed to have a three-stage conversion, with the SST providing galvanic isolation in the DC-DC stage [18]. A majority of SSTs have been designed with the configuration shown in Figure 5:

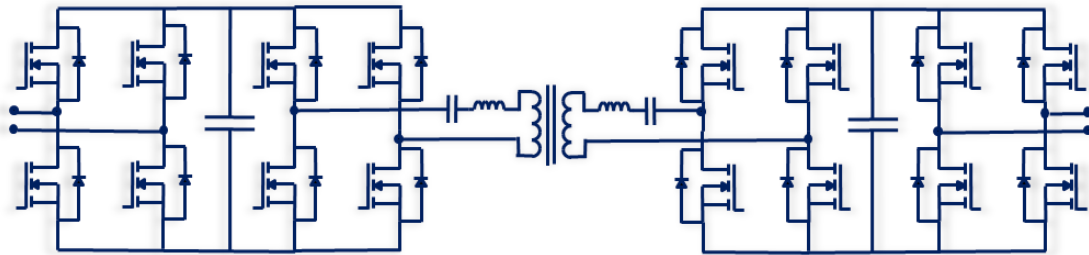


Figure 5: iPEBB topology.

This configuration has two H-bridges on either side of the SST and employs bidirectional power conversion. This is a popular configuration due to the fact that there are more available topologies for each of the bridge stages. This allows for more design flexibility to improve efficiency and optimize converter performance. Many interesting features, such as voltage sag compensation, renewable storage integration, and VAR compensation, can be achieved. Recently, this configuration has been adopted by General Electric (GE), who has developed a high- and low-voltage rectifier/inverter and soft-switching DC-DC stage using 10 kV, 120 A SiC half-bridge power modules. This initial work by GE was later adopted into the SST SiC-based PEBB shown in Figure 3.

The SST-based PEBBs can also be connected in series or parallel for high-voltage and high-current applications. Although the iPEBB (thus far) does not select a particular control scheme and connection method, it can be configured by various approaches. Some of the ones highlighted in the literature include the following three [17].

- Input series output parallel (ISOP)
- Input parallel output parallel (IPOP)
- Input series output series (ISOS)

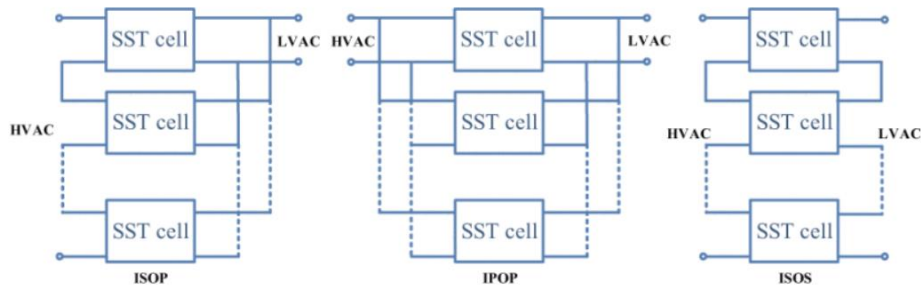


Figure 6: SST in high-voltage and high-power system [17].

Although this thesis does not focus on the grid-level application, topology, or control scheme of the iPEBB, it is still important to see the practical applications for the converter. The similar bridge layout between the two sides of the converter plays a critical role in the design simplification and manufacturing of the iPEBB. Furthermore, the various flexible connections allow for the different power conversions needed by power systems aboard electric ships.

1.2 Packaging

Both the PEBB 1000 and the SST-based PEBB have shown that SiC devices can help increase the overall power and speed of the converter. A critical aspect of implementing and fully benefiting from SiC devices involves the packaging of the devices themselves. Often times SiC devices are packaged in discrete packages and can be easily placed on a printed circuit board (PCB). Other times they are part of a multi-chip power module (MMPM) and are a building block for various converters. The SiC device's package provide the electrical, thermal, and mechanical structure that enables the use of the semiconductor itself.

While packaging might be an afterthought for most converters, it is critical to a high-density, fast-switching design. Often times, the packages used for Si devices are substituted for WBG devices like SiC and GaN. Unfortunately, preexisting packages are not optimized to get the full benefit of WBG devices. Figure 7 shows a generalized half-bridge module and schematic in order to highlight critical aspects of a half-bridge power module/package. In most traditional packages, the bottom layer starts with a heatsink and is followed by a thermal interface material (TIM) that allows for good contact between the module and the cooling system. Above the TIM is a substrate that provides electrical isolation between the

devices on top and the cooling system. On the topside of the substrate is a die-attach layer that helps connect the semiconductor to the substrate. The most common die-attach includes solder and silver sinter. On top of the semiconductor are wirebonds that help connect the device to the various potentials within the package. There are often metal connectors soldered onto the substrate that help interface the devices to the rest of the system. The entire module is usually encapsulated in silicone gel or molding compound to help protect the devices and provide electrical insulation.

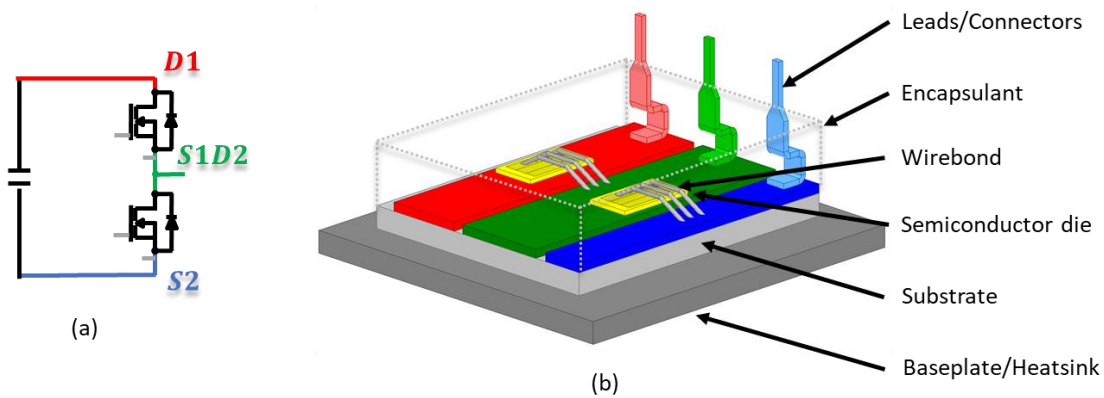


Figure 7: a) Half-bridge schematic, and b) generalized half-bridge module layout.

Many of the critical aspects of packaging can be extended beyond the power modules and into a converter design in order to achieve higher density. High-density integration has become a critical topic in the field of power electronics. This is especially true in the field of WBG packaging, where the layout and design can have dramatic effects on the thermal, electromagnetic interference (EMI), and switching performance of the converter.

Much research has been done on packaging in order to minimize the parasitic inductance and improve current sharing between devices. Since SiC devices are highly sensitive to parasitic inductance at high switching frequencies, it is crucial to minimize the stray inductance within a package [19]. Parasitic inductance can cause dangerous voltage

overshoots and ringing that can damage the device and reduce efficiency. Work has been done on how best to minimize parasitic inductance within MCPMs by optimizing the layout. Furthermore, innovate packaging methods involving multi-layer designs and unique interconnects have also been shown to minimize the gate and power loop parasitic inductance and improve switching transients. Furthermore, EMI is a major concern and is also a focus of this work [20].

Another important aspect of device packaging is the thermal performance and management. It is critical that the package take into consideration effective external cooling and the thermal resistance from the device to ambient. There are many things that affect the thermal performance, from the layout, to the selection of substrate, and to the interface material used between different layers of the module[21].

Most packaging topics have focused on a half-bridge module, due to it being the fundamental building block for a majority of converters. The half-bridge and H-bridge modules are modular and can be used to form various topologies for different power conversions[22]. There are also emerging SiC-based neutral-point clamped (NPC) power modules that allow for the flexibility of being used as a buck, boost, or half-bridge module[23]. Although the use of power modules to form converters seems logical and practical, it can come at the price of high-density integration and manufacturability.

In the previous section, the PEBB 1000 was introduced. It used two commercial 1.7 kV SiC half-bridge modules to form an H-bridge converter. The PEBB 1000 is comprised of many discrete components—SiC half-bridge modules, gate drivers, magnetics, and capacitors. These components are connected using additional mechanical parts, such as screws, busbars, and baseplates. The connection of multiple discrete

components limits the volumetric power density, performance, and manufacturability of the PEBB. This represents a disadvantage from a PEBB standpoint, eroding from the many benefits offered (scalability, flexibility, and reliability) by the modular concept that it embodies. Furthermore, discrete is the duplicity of functions that exist in this type of realization, which invariably affect the power density and costs of PEBB units.

This issue is further exacerbated when considering more complex topologies that involve more devices, and that half-bridges will require additional busbars and connectors and limit the high-density nature of PEBBs. A key design goal of the substrate's physical layout will be the minimization of the power- and gate-loop parasitic inductances of the half-bridge configuration. This becomes a critical challenge when there are multiple bridges and multiple devices in parallel.

1.3 *Research Objectives*

To address the need for a MV converter that offers flexibility in power conversion and a high level of manufacturability, integrated power electronics building g blocks (iPEBBs) are currently being explored for future electric ships. The iPEBB presented in this work aims to achieve lighter weight, improved manufacturability, greater performance, and higher power density. The iPEBB topology allows for flexible (DC/DC, DC/AC, AC/DC), galvanically isolated, bidirectional power conversion. The target specifications for the iPEBB are shown in Table I. The power, switching frequency, and weight targets for the iPEBB demand a unique approach to power converter design and integration.

To meet these demands, the design of the iPEBB takes into consideration the converter-level packaging, which includes a unique power stage layout and advanced substrate technology. Electrical, thermal, and mechanical simulations are completed to

inform the design and are followed by fabrication and testing of a half-bridge module. The insights gained from hardware testing will go into future refinement and integration of the iPEBB.

This is the first detailed report of the iPEBB, and as such, will focus on studying the packaging possibilities and limitations of the different designs. This thesis will focus on the initial design of the iPEBB and explore the different advanced substrate technologies that allow for the possibility of a high-density, fast switching converter. From a technical standpoint, the biggest impedances to PEBBs in general are the issue of thermals and EMI. This is especially true for the iPEBB, which will be switching at 500 kHz. Another critical component of the iPEBB is the high-frequency transformer from Fast Watt. Although it is crucial to the iPEBB design and layout, this thesis will only mention the design and prototyping of the transformer in relation to the rest of the iPEBB and the high-density design.

Table 1: Target values for the iPEBB.

<i>Parameter</i>	Target Value
Voltage	1 kV
Power	250 kW
Switching Frequency	500 kHz
Weight	16 kg

The design of a 250 kW, 500 kHz converter with an SST that weighs less than 16 kg is a highly ambitious goal, and this work seeks to remove barriers to making that a reality. The combination of power and switching speed makes the iPEBB a highly attractive yet challenging problem to tackle. Researchers at Fraunhofer Institute have

recently prototyped a 100 kW traction inverter with a power density of 51 kW/l and switching frequency up to 100 kHz [24].

This work will seek to explore state-of-the-art substrate materials and layouts in order to develop a high-density, highly manufacturable design for the iPEBB. In this work, a common substrate concept is analyzed in order to better understand its feasibility and to identify design advantages. The common substrate allows for the integration of multiple active and passive components onto a unified platform, which will serve as the electrical interconnects, cooling system[21], and mechanical support for the converter. By adopting and advancing many of the power module packaging technologies, an initial design of the common substrate is shown in this work.

Furthermore, to better understand the trade-offs associated with various substrates in terms of application in the iPEBB, half-bridge switching-cell prototypes are tested. Critical aspects such as thermal performance, electrical performance, and EMI mitigation strategies are explored in this work. The integrated nature of the iPEBB is crucial, since the topology that will be used is similar to the one shown in [12]. This topology is also highlighted below. Since there are as many as eight half-bridges (four H-bridges) within the converter, a highly integrated design will be required that can also be easily manufactured.

1.4 Thesis Organization

This thesis is organized into simulation and hardware-based sections in order to explore the design and feasibility of the iPEBB. Chapter 2 covers the advanced substrate technology that is being explored in order to provide a foundation for the converter. In Chapter 3, more detailed analysis and information about the common substrate concept is

highlighted. This will focus on the initial electrical, thermal, and mechanical aspects of a common substrate concept. Based on this, the design and testing of two switching-cell prototypes are highlighted in Chapters 4 – 7. These chapters will focus on the packaging of the switching cells and key insights for the iPEBB common substrate design. Chapter 8 will focus on the summary, major conclusions, and ideas for future work involving the iPEBB.

Chapter 2 Substrate Survey and Analysis

2.1 *Introduction*

Substrates play a vital role in the design of the iPEBB, since they play a critical role in the electrical, thermal, and mechanical performance of the converter. The substrate plays an important role in the reliability and manufacturability of the iPEBB as well. For this work, various substrate materials were explored including organic and inorganic substrate materials. Inorganic substrates include ceramic-based insulation. Organic-based substrates encompass a large family of different polyimide and epoxy-based insulation types.

2.2 *Ceramic Substrates*

Most commercial power modules are packaged with ceramic-based substrates, due to their ability to carry high current, provide high voltage isolation (15 - 20 kV/mm), and operate at high temperatures (125 °C to 200 °C).

Direct-bonded copper (DBC) ceramic substrates are the industry standard due to their low coefficient of thermal expansion (CTE) and good heat-spreading characteristics[25]. In the DBC process, at a high temperature, a thin copper oxide on the copper foil is leveraged in order to bond between the copper and the ceramic. A eutectic bond is the combination of multiple metals that will allow for transformation of solid to liquid at certain temperatures. Aluminum oxide (Al_2O_3) DBC is relatively inexpensive and widely available, but aluminum nitride (AlN) DBC is often preferred in MV applications due to its superior thermal conductivity [26] (Table I). In fact, AlN has thermal conductivity that is seven to eight times higher than Al_2O_3 . Yet, AlN suffers from

a low bending strength (300-400 MPa) and might cause issues related to mechanical strength [27].

Active metal braze (AMB) is another technology that allows for thick metal layers to be brazed to ceramics. Silicon nitride (Si_3N_4) is often used with AMB technology due to its high fracture toughness and reliability. Si_3N_4 has the robust bending strength of 600 MPa. It also has a thermal conductivity of 90 W/m·K, which is still three to four times higher than Al_2O_3 . Furthermore, Si_3N_4 often comes at a thickness of less than 0.32 mm. Hence, the thin nature of the substrate allows for the compensation of lower thermal resistance of the insulation layer. The literature has shown that the overall resulting thermal resistance is approximately the same as AlN [25]. Although it has many advantages, Si_3N_4 AMB is more expensive and not as widely available as DBC substrates. Overall, ceramics offer good thermal conductivity and dielectric strength; however, their brittle nature limits their maximum metallization thickness. The high elastic modulus of ceramics also results in delamination of the DBC under thermal cycling [26].

2.3 Organic Substrates

Organic substrates, an alternative to ceramics, have also grown in popularity. Organic substrates are popular in the microelectronic packaging field, where high power is often not seen [28] [29] [30] [31]. But recently, higher-power modules have also started to adopt organic substrate technology despite the fact that its insulation layer offers poor thermal conductivity. Organic substrates using a thin epoxy or polyimide insulation layer have recently been implemented in insulated gate bipolar transistor (IGBT) power modules [32]. Furthermore, analysis on integrated metal substrates (IMSS) for SiC-based traction applications have shown promising results [33]. Additionally, graphite-embedded organic

substrates have been demonstrated for SiC-based power modules [34]. This highlights the ability of organic substrates to be able to bond to various conductors and materials, as well as offering more flexibility in power module design.

Recently, new organic laminate epoxy resin composite dielectric (ERCD) was implemented in a 1.2 kV SiC Bi-Directional Field Effect Transistor (BiDFET) switch. Many people in industry are looking to organic substrates due to the high cost of DBC/AMB-based substrates [35]. As an alternative, organic laminated substrates are much more cost-effective, and are already widely commercialized. PCB technology often uses organic-based insulation, but due to its poor thermal performance, it is difficult to implement for high-power applications. Furthermore, polyimide-based substrates cost about 40% of AlN per sq. inch [36], and allow for easier implementation of vias and multilayer designs. Although ceramics also offer multi-layer designs with vias, they are often a more expensive and time-consuming option. The persistent issue with organic substrates is their lower thermal conductivity. Research has been done to see if a composite insulation layer with higher thermal resistance can be developed. Furthermore, designs with thicker copper metallization for better heat spreading are also possible [37].

One organic substrate that is being explored for the iPEBB is a polyimide-based organic direct-bonded copper (ODBC). The ODBC offers many attractive benefits that can improve the reliability and electrical performance of power modules. Table I shows parameters for the ODBC considered in this work. Although the polyimide used in the ODBC has lower thermal conductivity than ceramics, its higher dielectric strength and ductility enable thin layers (as low as 25 μm) to be used. This, along with the thick metallization, reduces the thermal resistance and makes the ODBC a viable candidate for

SiC power modules. ODBC also has high thermo-mechanical reliability; the ODBC can endure 5,000 thermal shock cycles (from -40 °C to 200 °C) without delamination [37].

Table 2 : Substrate comparison.

Parameter	AL₂O₃ DBC	ALN DBC	Si₃N₄ AMB	ODBC
<i>Thermal Conductivity (W/m·K)</i>	24	170	90	Through-Plane: 0.7 In-Plane: 2
<i>Dielectric Strength (kV/mm)</i>	20	20	20	> 100
<i>Minimum Dielectric Thickness (mm)</i>	0.32	0.63	0.25	0.025
<i>Maximum Footprint Size (mm)</i>	127 × 178	127 × 178	127 × 178	> 300 × 600
<i>Maximum Metallization Thickness (mm)</i>	0.3	0.3	0.8	> 0.5

Additional testing was completed on the ODBC in order to better understand this state-of-the-art substrate. To see the ODBC's electrical performance, samples were prepared for partial discharge (PD) testing. The goal of this test is to look at the partial discharge inception voltage (PDIV) of an ODBC sample with a 35 µm insulation. If this electric field exceeds the breakdown field strength of the ODBC insulation material, then PD events can occur. Repetitive PD events can ultimately result in insulation failure, thus destroying the power module or converter. The test setup used a 100 kV 60 Hz power supply for the excitation (Figure 8).

A high-frequency current probe (ETS-Lindgren 91550-1) was used to measure the PD current, and a high-voltage passive probe (Tektronix P6015A) was used to measure the applied voltage. The 50 mm by 50 mm ODBC sample was submerged in oil during testing, and the voltage was slowly increased. The test shows a PDIV of approximately ~ 3.6 kV RMS (Figure 9). This shows that an encapsulated ODBC switching cell will be able to operate at a 1 kV voltage level without any PD issues.

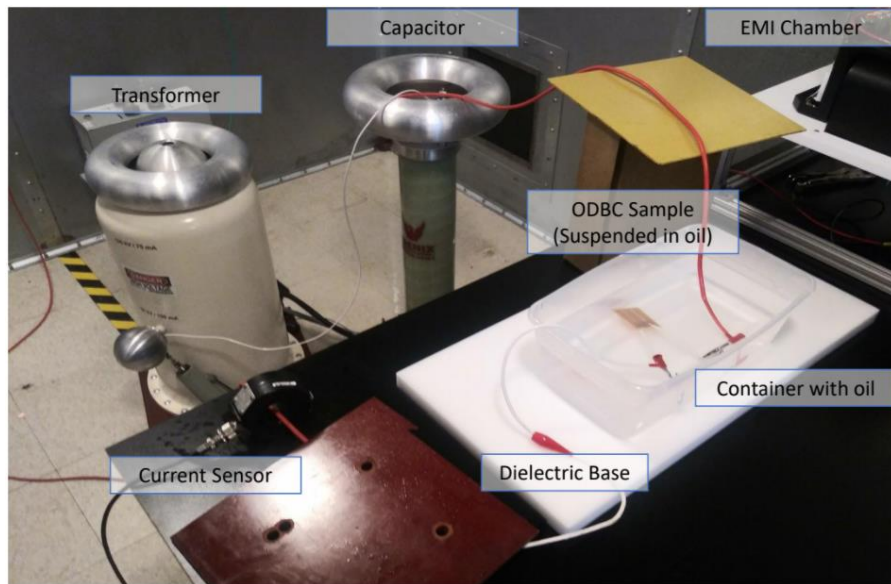


Figure 8: PDIV test setup.

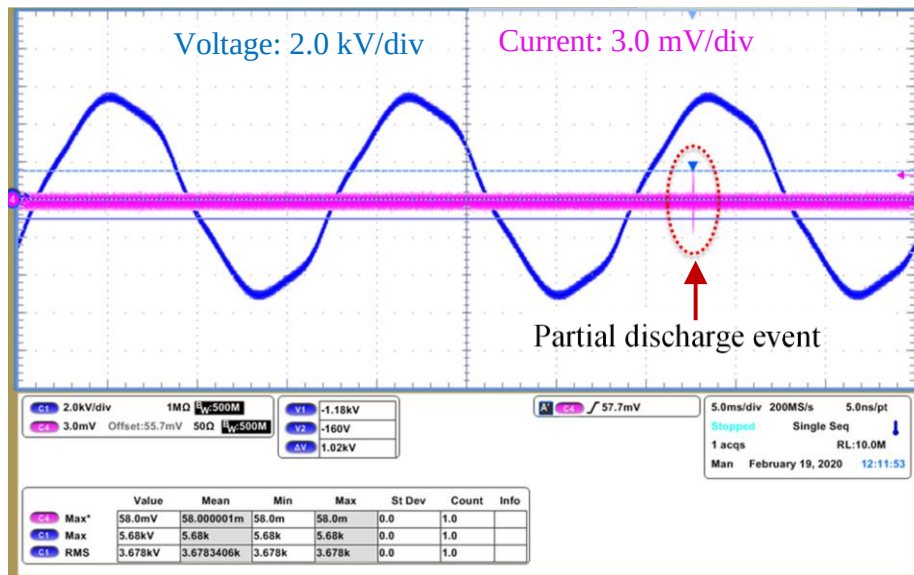


Figure 9: PDIV of a single-layer ODBC substrate.

2.4 iPEBB Substrate Implementation

As previously mentioned, the substrate plays a vital role for the electrical, thermal, and mechanical performance in the iPEBB. The survey of organic and ceramic substrates provided some insight into the benefits, limitations, and key trade-offs for various materials. Ceramic substrates are traditional for power modules and offer better thermal performance than organic-based substrates. On the other hand, the ceramic substrate market is often monopolized by a handful of companies and can be expensive to manufacture compared to organic-based substrates. Organic-based substrates for higher-power applications have recently grown in interest due to the fact that they offer more design flexibility and lower costs than ceramic substrates.

Organic-based substrates offer the chance to envision the iPEBB common substrate concept. Ceramic substrates are often limited by their footprint size due to the brittle nature of the material. This is usually not a problem for power modules since a majority fall within the footprint specifications. But for the iPEBB, where many SiC components and SSTs are placed onto the substrate, it can be a problem. This issue can be resolved by adding a baseplate and having multiple ceramic substrates to form the converter. However, this approach increases the complexity of manufacturing and erodes the integrated nature of the iPEBB that makes it unique.

The following section will describe the design of the common substrate based on the ODBC material. Key limitations and benefits are highlighted, and concerns about the thermal and electrical performance are analyzed.

Chapter 3 **iPEBB Design**

3.1 *Introduction*

The development of the iPEBB employed electromagnetic and thermal finite element analysis (FEA) to optimize the layout of the unit. By designing a unique integrated power stage, instead of employing discrete modules, the iPEBB seeks to achieve low power- and gate-loop inductance, uniform current distribution, and good thermal performance ($T_j < 175^\circ\text{C}$), while also minimizing conducted EMI. FEA simulations on ODBC technology and on the common substrate are highlighted. Electrical, thermal, and mechanical simulations are completed to inform the design and identify key trade-offs and insights of the design. The high-frequency SST is not directly included in this work, although the SST impact of the common substrate and the rest of the system are highlighted.

3.2 *Exploring iPEBB Layout*

The layout of the iPEBB needs to take into consideration the integration of the unique bi-directional topology that forms the core of the design. The iPEBB also takes advantage of dual-sided cooling, where both the top and bottom sides of the iPEBB are cooled using rack-level cooling. Figure 10 shows a side view of the latest iPEBB design. It seeks to use a common substrate design that will have the various MOSFETs and passive components placed directly onto it. Additional connections are placed in the back where the converter will be able to interact with the other iPEBBs, either in series or in parallel. Noticeably, there is no additional baseplate since the common substrate seeks to serve that

purpose as well. The weight, manufacturability, and the implementation of the iPEBB concept depends heavily on the common substrate and the high-frequency SST.

At the core of the iPEBB is a high-frequency SST developed by Fast Watt LLC. Power conversion using medium or high-frequency transformers (in lieu of line-frequency transformers) provides a substantial reduction in the size of the transformer core and windings. However, the insulation system needed to allow for MV applications can become a sizeable fraction of the transformer volume and may present a thermal barrier preventing effective cooling. In [38], insulation material is analyzed for high-frequency transformers. In fact, most medium- or high-frequency transformer designs have typically used oil or epoxy insulation, or relied on the use of MV cables to provide insulation between the primary and secondary cores [39] [40][41].

In the iPEBB, the proposed transformer design uses an insulating sheet coated with stress-grading conductive and semiconductive layers to separate the primary-side windings and primary-side magnetic core from the secondary-side windings and secondary-side magnetic core (Figure 10). Furthermore, the insulating sheet between the primary and the second side also acts as an ‘air gap.’ Hence the thickness and material of the insulating sheet is carefully selected based on the isolation requirements as well as the desired magnetizing impedance to satisfy the circuit optimization.

Furthermore, iPEBB gate drivers and circuitry concepts are shown placed above the H-bridges in order to provide a low-gate-loop inductance design. In future sections, information about the common substrate concept design and analysis will be complete.

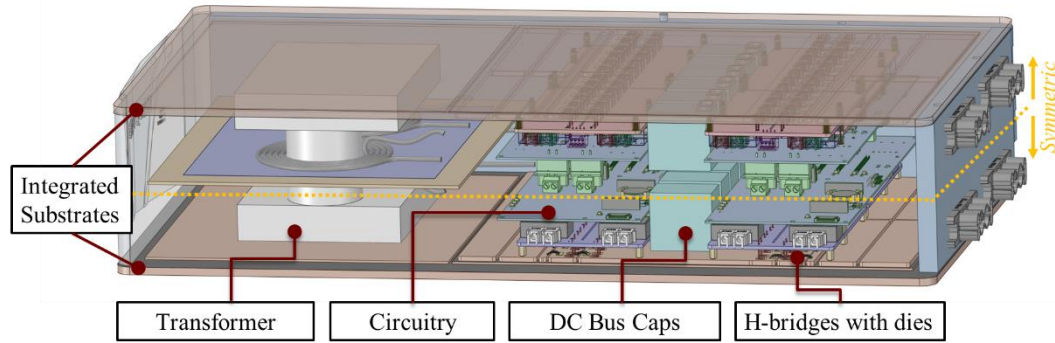


Figure 10: Internal layout of the iPEBB concept.

3.3 Common Substrate Design

At the core of the iPEBB is a common substrate that will serve as the foundation for the converter. In most power electronics systems, discrete power modules are mounted onto a baseplate and interconnected using a busbar to form the topology. All variations of PEBBs mentioned in the earlier section employed discrete power modules or discrete packaged devices to form the various topologies. In the iPEBB, the topology is realized by bonding and interconnecting 1.7 kV SiC MOSFET bare dies and passive components to a common substrate. The common substrate will provide multiple functions, including electrical connections through a substrate-based busbar, a unified cooling platform, and mechanical support for the entire power stage. Figure 11 shows the multi-layer nature of the common substrate, where the multi-layer design is used for electrical purposes. The entire common substrate is not part of the multi-layer design, only the location of the SiC MOSFET bare dies that can benefit from such a design. For the transformer, a single-layer design is used in order to reduce the thermal resistance in order to cool the transformer core. Additional work will need to be completed to gain a better understanding of the appropriate cooling methods for the transformer windings.

The multi-layer design serves as a busbar as well as a low-impedance path for EMI. This type of design would only be possible with organic-based substrates where multiple layers can easily be manufactured and implemented through a lamination process. The large footprint the iPEBB is based on is possible due to the ductile nature of the ODBC insulation material. The thin nature of the polyimide layer offers a >95% power loop inductance cancellation.

The integrated power stage offers small power-loop inductance, good heat dissipation, and low EMI, while meeting strict weight limitations (less than 16 kg). Figure 12 shows the iPEBB topology [11], with key elements of the primary side highlighted. The topology features eight half-bridges (four per side), a high-frequency transformer (orange) to provide the galvanic isolation, and DC-link (green) and resonant (purple) capacitors. To minimize the size of the transformer, the target switching frequency for the inner bridges is 500 kHz. To achieve this high switching frequency, soft switching is employed for the inner bridges through a CLLC topology. The outer bridges (blue) will be hard switching (between 10-30 kHz) and interface to the AC or DC line.

Figure 12 shows the iPEBB concept that is being explored, with the common substrate for the primary side shown. The iPEBB unit is 550 mm by 300 mm by 100 mm in size, and is intended to be inserted into a rack, which will provide cooling to both the top and bottom common substrates [21]. The components that make up the SiC bridges are integrated onto the common substrate for better electrical and thermal performance. The primary core of the transformer and the resonant components are placed on the common substrate, which provides mechanical support, heat spreading, and a low-thermal-

resistance path to the rack cooling. The primary and secondary sides of the iPEBB have identical common substrates, which simplifies manufacturing and reduces cost.

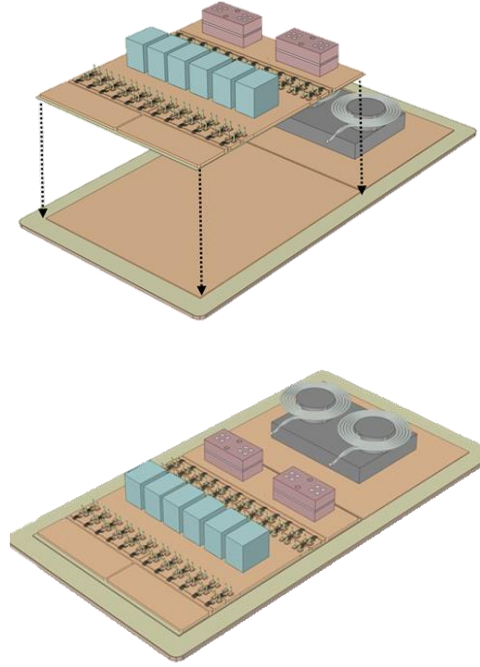


Figure 11: iPEBB common substrate concept.

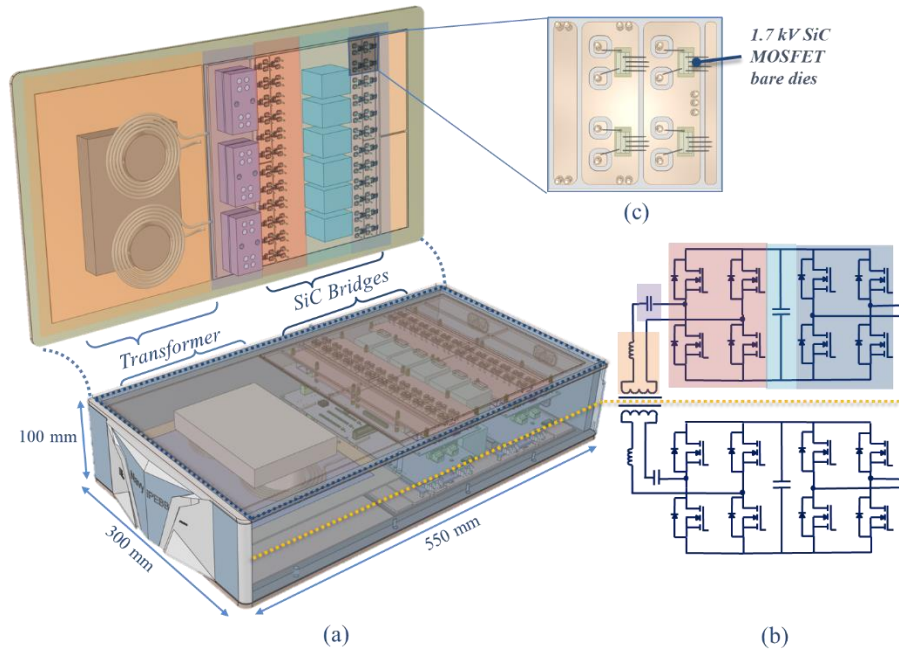


Figure 12: (a) iPEBB design with a top view of the primary side, (b) iPEBB topology, and (c) switching-cell portion of the SiC H-bridges.

With the common substrate concept, the thicker metallization can be closer to the die. Figure 13 highlights the cross-section between the PEBB 1000 and the iPEBB showing the design of the common substrate. In the PEBB 1000, where multiple discrete power modules are used, there are three interface layers (grease, solder, etc.). There is an interface between the die and the AlN DBC substrate, and between the AlN DBC to the power module baseplate. Furthermore, there is an additional interface where the power module is placed on a baseplate that helps provide mechanical support for the entire converter. Although this type of design is feasible, it requires redundancies in the design as well as additional steps and materials, which adds to the cost and complexity of the converter. On the other hand, with the iPEBB common substrate concept, the entire converter can be based on a single manufactured platform. The iPEBB concept has only one interface layer between the bare die and the common substrate. The rest of the cross-section is the common substrate where a multilayer design is used for electrical benefits. This not only helps reduce manufacturing costs but also simplifies the process by eliminating additional processes and interface layers.

Thicker copper metallization near the die level helps with the heat spreading, but also requires careful consideration of thermo-mechanical impacts. The thick copper near the die can cause additional strain and thermo-mechanical issues on the die-attach layer, which can degrade the reliability and life cycle of the iPEBB. This topic will be covered in further detail in later sections.

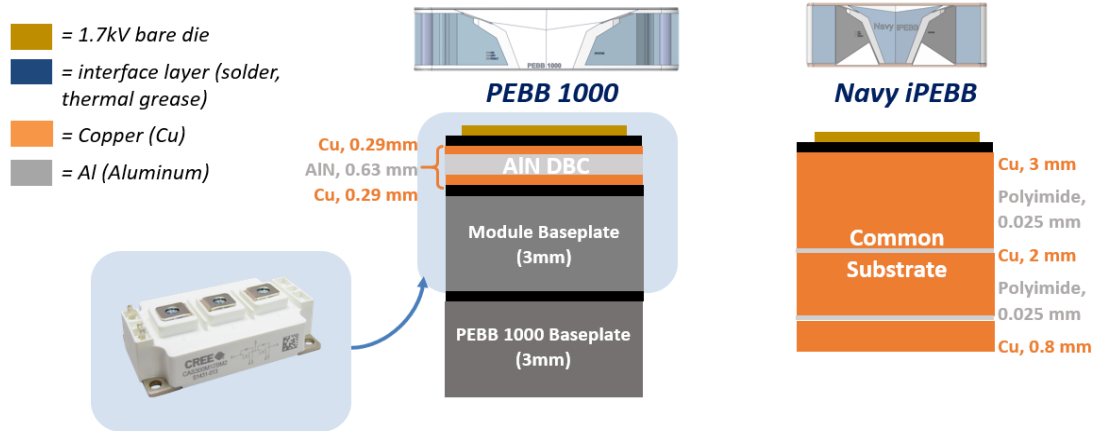
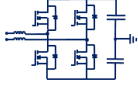
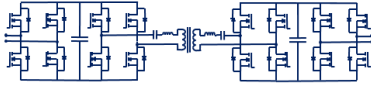


Figure 13: Comparing the cross-sections of the PEBB 1000 and iPEBB below the die shown the common substrate concept.

The common substrate concept helps simplify the manufacturing and packaging of the iPEBB compared to traditional module or PCB based converters. Below in Table 3 is a comparison of the PEBB 1000 and the iPEBB and the ability of the common substrate to help achieve the high-density goal. With four times the number of H-bridges, a high-frequency SST, the iPEBB's common substrate is vital for integrating the multiple components. This helps triple the power density of the converter, despite it having more components and devices than the PEBB 1000. Furthermore, the iPEBB's goal weight is around 16 kg (35 lbs), which is needed in order to enable the iPEBB to be carried around electric ships.

The common substrate and the layout (which will be described) helps the iPEBB power stage behave like a power module, where all components are placed onto a unified platform. Despite this, there are still many unknowns and risks with the common substrate concept. Simulation and hardware work is carried out in order to identify key take aways.

Table 3: Comparison between the goals of the PEBB 1000 and the iPEBB.

Converter	 <i>PEBB 1000</i>	 <i>iPEBB</i>
Topology		
Power Rating	100 kW	250 kW
Number of H-Bridges	1	4
Power Density	5 kW/l	12-15 kW/l
Weight	~27 lbs	~35 lbs

3.4 SiC Bridge Layout

This section covers the design of the common substrate, including information about the layout, device arrangement, and packaging material selection. Initial simulation and analysis on the electrical, thermal, and mechanical performance of the common substrate are presented with key trade-offs identified. Due to the potential benefits afforded by ODBC, it was used to design a common substrate to serve as the main electrical, thermal, and mechanical base for the iPEBB. A critical goal of the common substrate is to simplify the design and integration of the four H-bridges (eight half-bridges) that comprise the iPEBB topology. Figure 14 (a) shows the iPEBB common substrate, which forms the 550 mm by 300 mm footprint of the converter. The integrated SiC bridges are color coded to correspond to the nodes in the schematic shown in Figure 14 (c). The red represents the positive bus (D1), the blue represents the negative bus (S2), and the green represents the output node (S1D2). A close-up view of the integrated SiC bridges, which is comprised of

four half-bridges, is shown in Figure 14 (b). Each half-bridge has six 1.7 kV bare die MOSFETs in parallel.

The design of the integrated SiC bridges employs a symmetric layout, where the soft- and hard-switching half-bridges are mirror images of each other and share identical layouts. In Figure 14 (b), the half-bridges highlighted in the orange bracket will interface to the transformer, and the half-bridges highlighted in the blue bracket interface to the AC or DC line. The two sets of half-bridges are connected on the multi-layer common substrate, which employs vias to connect the top and middle metallization. The vias are specifically placed to provide a low-inductance connection between the negative DC bus (S2 node) pads on the top copper layer and the middle copper layer (Figure 14 (e)).

By using multiple copper layers for electrical connections, the iPEBB can take advantage of negative mutual inductance cancelation that can help reduce the power loop inductance [42]. Furthermore, the multi-layer design allows the common substrate to serve as a busbar to the entire system. The substrate-based busbar design maximizes the multi-purpose nature of the common substrate and minimizes the need for complex lead frames, metal-stamped busbars, and wires that would be associated with interfacing multiple discrete power modules.

The placement of the dies was carefully selected to address many of the issues associated with having multiple parallel devices. Having six dies in parallel per switch position increases the concern there might be uneven current sharing between devices. Previous work has shown that asymmetrical parasitics among paralleled dies can cause a large current imbalance [43]. This means that during transient events, certain dies will experience more current than others due to an uneven parasitic inductance. The dies that

experience this extra current will have larger losses and higher junction temperatures, and will fail before their projected lifetime.

To address this issue, a symmetrical layout was developed for the iPEBB power stage. A portion of the integrated SiC bridges, referred to as a switching cell, was designed and analyzed (Figure 14 d). The design takes advantage of the superior reverse conduction characteristics of the SiC MOSFET, which eliminates the need for external antiparallel diodes. Hence, the switching cell consists of only two paralleled 1.7 kV SiC MOSFETs per switch position.

Thanks to the multi-layer design, the two paralleled SiC MOSFETs could be placed symmetrically to achieve identical power loops. Having identical power loop inductance for each switching cell reduces the chances of current imbalance between dies. Furthermore, the devices are parallel along their shorter side to minimize thermal coupling between adjacent devices. For the gate loop, a balanced inductance is achieved by having individual gate and Kelvin connections for each die. The Kelvin connection prevents negative feedback between the gate and power source, thereby increasing the switching speed. By having balanced gate loops for each die, the need for additional embedded gate resistors is reduced, enabling faster switching speeds.

An ANSYS Q3D extractor was used to extract the parasitic inductance information for the gate and power loops. The gate-loop inductance is 6 nH for each MOSFET in the switching cell. The strong negative mutual inductance cancelation offered by the thin dielectric material reduces the power-loop inductance to 3 nH. Most of the inductance comes from the wirebonds, which are used for the MOSFET interconnects. For this simulation, the dielectric thickness was 35 μm . In later subsections, the influence of the

dielectric thickness on the design will be further explored. The substrate-based busbar design also allows for placement of the DC-link capacitors directly on the common substrate for cooling and electrical connection. Figure 14 (c) shows the DC-link capacitors with the substrate patterning beneath it. The blue S2 pads connect capacitors to the middle layer through vias. There are six, 1.5 kV, 10 μ H film capacitors that make up the 60 μ H DC-link. They are placed equidistant from both the hard-switching and soft-switching bridges for a balanced power loop between parallel dies and parallel half-bridges.

Film capacitors were chosen for the DC-link due to their ability to offer the voltage level and capacitance level required for the iPEBB. Film capacitors have an operating temperature of less than 120 °C, which requires careful placement on the common substrate. For this reason, FEA thermal simulations were used to optimize the DC-link capacitors placement to be 32 mm from the bare dies on either side to minimize their exposure to high temperature.

The substrate-based busbar enables low parasitic inductance, even when the DC link is moved further away. In fact, the ANSYS Q3D extractor shows that the power loop for a switching cell is only increased by 0.5 nH to 3.5 nH when measuring from the DC-link capacitors, as illustrated in Figure 14 (b). Furthermore, the low-inductance design allows for the elimination of additional decoupling capacitors, which reduces the number of components.

Another advantage of the multi-layer substrate design is that it acts as a common-mode (CM) screen to reduce EMI issues. For the converter-level design EMI is also a major concern. The WBG design offers higher dv/dt than traditional silicon devices, and that exacerbates the EMI. Conducted EMI ($\sim < 30$ MHz) is an important issue for WBG devices

since it causes induced current through the ground that can affect the rest of the electrical system. Radiated EMI ($\sim >30$ MHz) can propagate through space, causing disturbances and distortions in nearby electrical systems. The parasitic capacitance of the substrate patterning is a major contributor to the EMI performance of a module. Often, the solution to the EMI of WBG devices is to slow them down so they do not have harsh transients, which means not utilizing all of the technology's benefits. But many EMI mitigation strategies go from the package level to the system level. The iPEBB seeks to take advantage of the packaging-level EMI mitigation strategies instead of relying on large filters and magnetics to do so. Due to the fast-switching requirement of the iPEBB, high dv/dt is expected. This has been shown to exacerbate EMI issues. The CM screen redirects the CM current back into the DC bus and away from the ground. This method has been shown to be effective in power modules that use ceramic-based substrates [42]. The main criterion for an effective CM screen is making sure the impedance of the screen path is lower than that of the ground path, especially at high frequencies. Thanks to the low-inductance design of the common substrate, the implementation of the CM screen should be possible.

On the other hand, due to the thin dielectric layer associated with organic substrates, the large capacitance from the switching node (CS1D2) to the CM screening layer increases the output capacitance (C_{oss}) of the bottom-switch MOSFETs. This larger C_{oss} will impact the losses and efficiency of a converter. For the soft-switching bridges, the increase in C_{oss} can be minimized by the leakage inductance from the transformer. For the hard-switching bridges, this capacitance remains an issue. One way to reduce CS1D2's impact on the C_{oss} is to increase the dielectric thickness, which would reduce the capacitance coupling between the switching node and the CM screening layer. But increasing the dielectric

thickness would also reduce the mutual inductance cancelation that is vital for low-inductance designs.

Analysis was completed on the electrical trade-offs between C_{S1D2} and the mutual inductance coupling coefficient (k) when the dielectric thickness is varied for the switching cell, as shown in Figure 14 (d). Results reveal that when the dielectric thickness is swept from 25 μm to 125 μm , the C_{S1D2} is dramatically reduced from 686 pF to 137 pF, which is an 80% decrease. This in turn minimizes the increase in C_{OSS} from a 200% increase to a 35% increase over the original C_{OSS} for the bottom-switch MOSFETs. Meanwhile the k coefficient slightly decreases from 0.96 to 0.91. From an electrical perspective, increasing the dielectric would be a simple way to minimize the capacitance coupling. But it should be noted that increasing the dielectric thickness would increase the thermal resistance and make cooling the devices on the common substrate more difficult. These trade-offs and possible redesign concepts will be analyzed in the discussion subsection later.

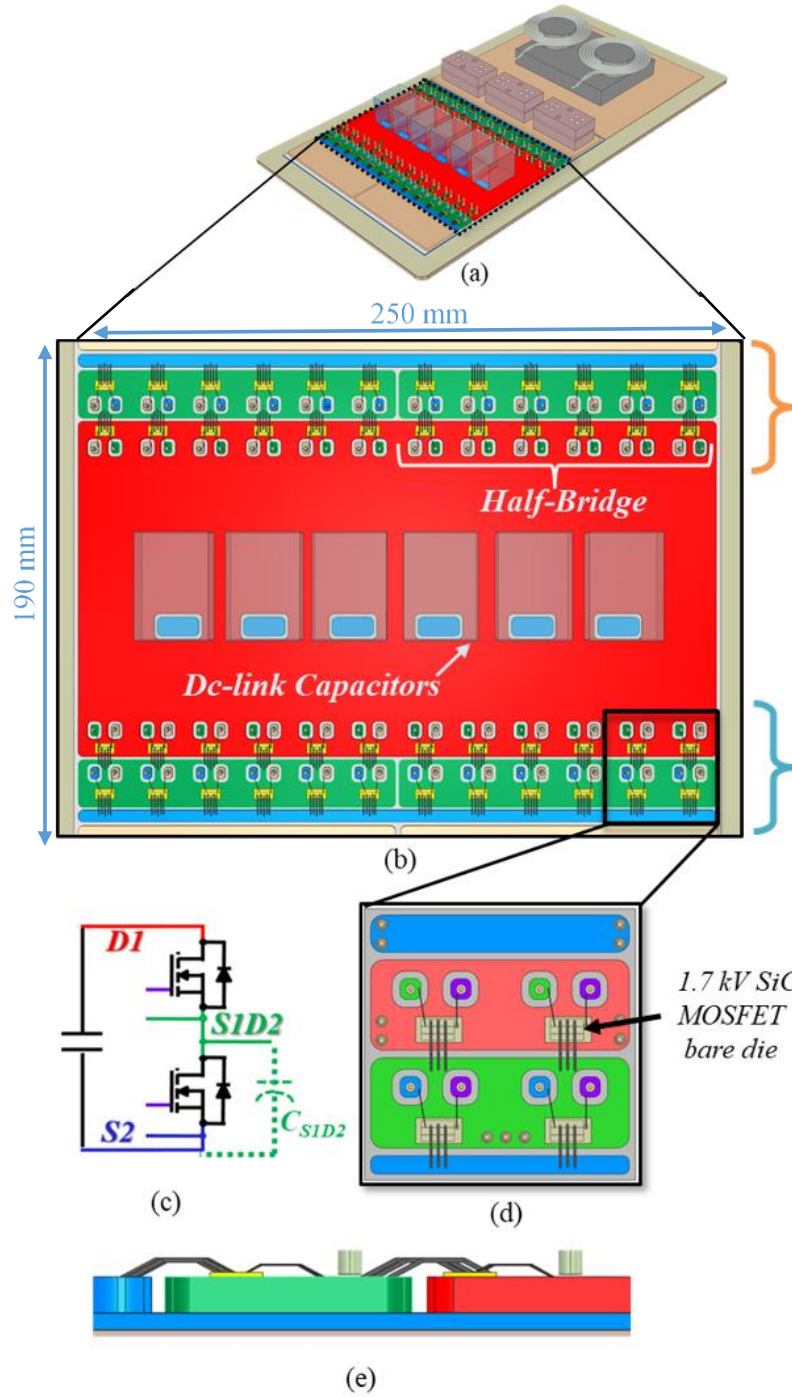


Figure 14: (a) Common substrate with the integrated SiC bridges, (b) top view of the integrated SiC bridges, (c) half-bridge schematic, (d) switching cell, and (e) cross-section of multi-layer ODBC common substrate.

Furthermore, current density distribution simulations were completed on an H-bridge portion of the iPEBB to better see the current sharing that would occur within the

iPEBB. Figure 3 shows the current distribution of a single- vs. multi-layer iPEBB half-bridge design. From the results it can be seen that the current distribution is better in a multi-layer design and offers a higher level of mutual inductance cancelation.

3.5 Mechanical Analysis

The structural integrity of the common substrate is critical to assessing the feasibility of the iPEBB concept. For the transformer, the common substrate mainly offers mechanical and thermal benefits. Because of this, a single-layer design is used for the area of the transformer to minimize the number of dielectric layers and to reduce weight. Figure 15 (a) shows a cross-section of the common substrate where the transformer cores will be placed for cooling. A concentrated weight of the transformer (~ 5 kg) causes the common substrate to deflect, resulting in non-uniform contact to the double-sided rack-level cooling system, shown in [21].

Since the ODBC offers the ability to laminate various metals and thicknesses, the metallization under the transformer can be manipulated to minimize deflection, while meeting the weight target for the iPEBB. To better understand the mechanical properties and limitations of the common substrate, preliminary mechanical simulation work was completed.

In the simulation, the common substrate was secured using 18 screw holes that were placed equidistant around the edge where the common substrate would meet with the iPEBB housing. The screws are size 10-32 and are like the ones used to secure the baseplate in the PEBB 1000. Force in Newtons was applied for the various components on the common substrate to see the deflection along the Z-axis.

Figure 15 (b) shows the deflection and weight of the common substrate when the copper (Cu) and aluminum (Al) thickness underneath the transformer is varied. Results show it is possible to reduce the deflection to less than 0.6 mm, while keeping the top and bottom common substrates weighing less than 4.6 kg each. This will allow the iPEBB to meet the 16 kg weight limit needed for easy handling. The rack design, including the pressure applied and contact interface, will ultimately decide the allowable deflection. This initial simulation shows that it is possible to minimize that deflection with strategic metallization type and thickness of the common substrate.

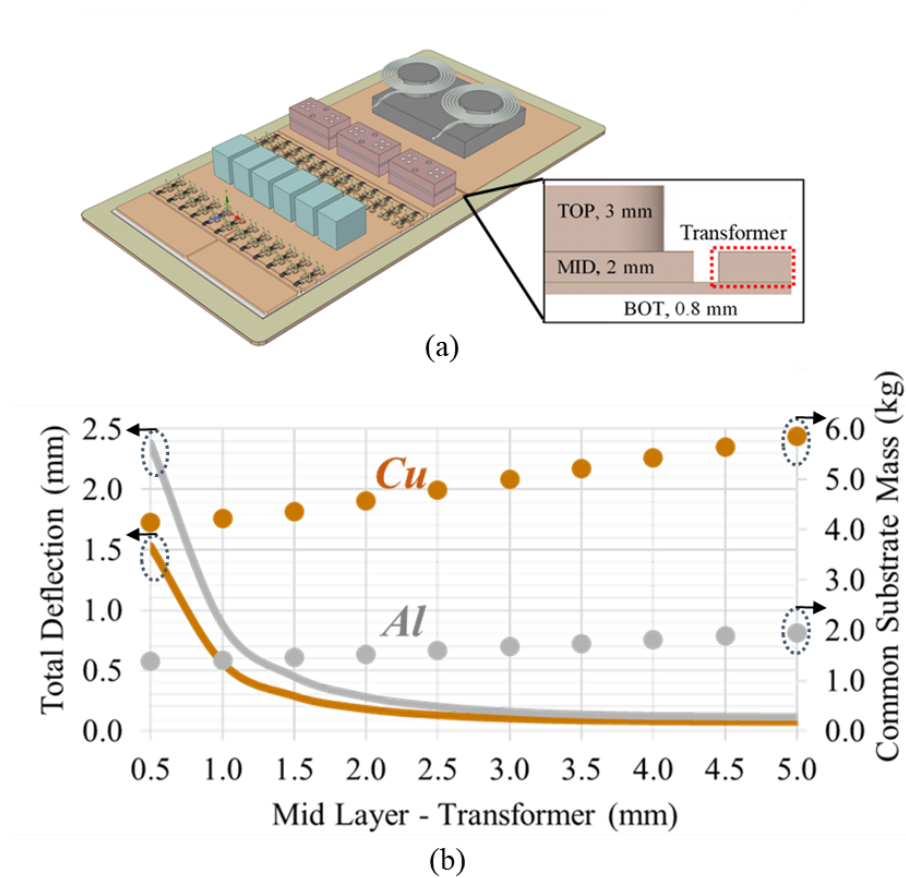


Figure 15: (a) Cross-section of the common substrate, (b) deflection vs. weight as the thickness of the metallization under the transformer is varied for Cu and Al options.

3.6 Thermal Analysis

A multi-layer design offers many electrical benefits that would make the iPEBB a reality, but the addition of a second dielectric layer can impact the thermal performance of the converter. Steady-state thermal finite element analysis (FEA) was performed on the switching cell shown in Figure 15 (d) to evaluate the impact of a multi-layer design. For the multi-layer (ML) ODBC, the Cu thicknesses of the top, middle, and bottom layers were varied one at a time, while holding the other two layers at 0.8 mm. Each bottom-switch die was assigned a 70 W loss, and a conservative cooling coefficient of 2000 W/m²K was applied. The results show that the top Cu thickness has the greatest impact on the maximum temperature for the ODBC (Figure 16 (a)), due to the low thermal conductivity of the 35 μ m polyimide layer.

A data point from Figure 16 (a) is selected and the cross-section results are shown in Figure 16 (b). From the simulated results, most of the heat spreading takes place in the top Cu, and there is an approximately 20 °C temperature drop across each polyimide layer. Therefore, the top Cu should be the thickest, and the middle and bottom layers should be minimized to reduce the total substrate weight. Furthermore, in a previous subsection it was concluded that the switching-node capacitance (CS1D2) can be reduced with a thicker dielectric but would increase the thermal resistance of the common substrate. When the dielectric thickness is increased from 35 μ m to 75 μ m, the peak temperature increased by ~17 °C under the same conditions as Figure 16 (b). It should be noted that reducing the CS1D2 will also minimize losses, which will relax the cooling requirement of the iPEBB.

Previous PEBBs used commercial power modules and a thick common baseplate for mechanical support and interface to the cooling system. The addition of thicker

baseplates adds significant weight, increases the number of thermal interfaces, and provides minimal thermal benefit. With the iPEBB concept, the thickest metal can be closest to the die, enabling maximum thermal performance while minimizing weight. When looking at a side view of the iPEBB where a common substrate is used to develop the power stage instead of discrete modules, this becomes clear (Figure 13). The PEBB 1000, on the other hand, uses a module and various interface layers to form the PEBB 1000 structure. Although this is possible, it does limit the manufacturability and increase the complexity of adding additional interface layers.

Figure 17 shows an H-bridge position of the iPEBB where the dies are assumed to have a loss of 70 W. It is clear that spacing the dies further apart helps make sure that there is minimal thermal coupling, but there are limitations to the heat spreading due to the gate and Kelvin pads that are located close to the die. Having these gate and Kelvin pads near the dies reduces the power loop inductance but limits the heat spreading of the various devices. This is especially true for the ODBC where the polyimide insulation layer has poor thermal conductivity and will require additional heat spreading in order to cool the devices successfully. This is further exacerbated by the multi-layer design, where two insulation layers are needed and the thermal resistance increases. From the layout, the placement of the dies across their shorter side helps minimize thermal coupling. This is critical when considering the fact there are six dies in parallel per switch position.

Removing the gate and Kelvin pads and replacing them with a wirebondless design would save crucial regions of copper needed to improve thermal performance and would allow the dies to be placed closer together in order to minimize the parasitic capacitance to the middle metal layer. This will, of course, come with trade-offs as far as a more complex

manufacturing process. Further analysis on the critical nature of these trade-offs is needed going forward.

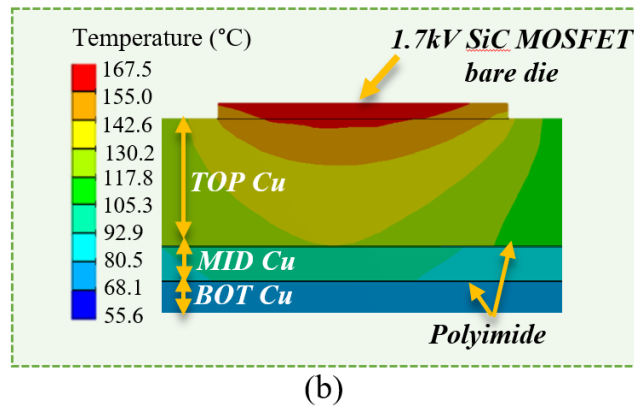
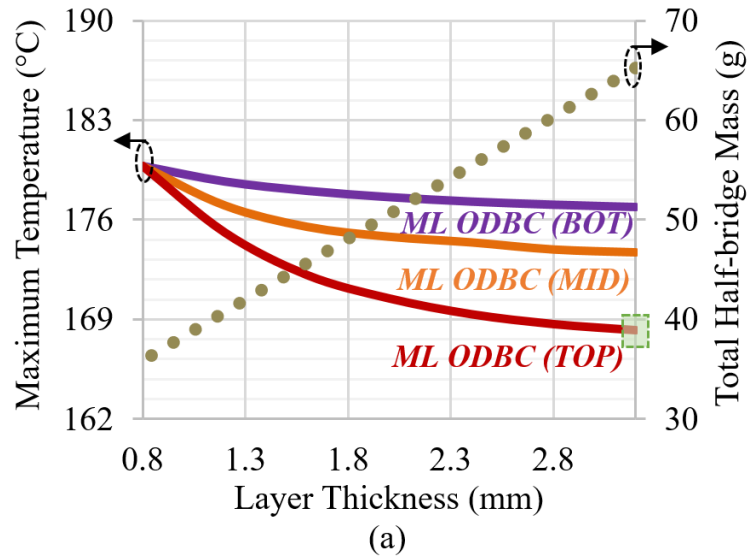


Figure 16 : FEA results with 70 W loss per die (bottom switch) and 2000 W/m²K: (a) temperature and mass vs. Cu thickness for ML ODBC layers, and (b) cross-section of a datapoint from the ML ODBC showing the temperature gradient between layers.

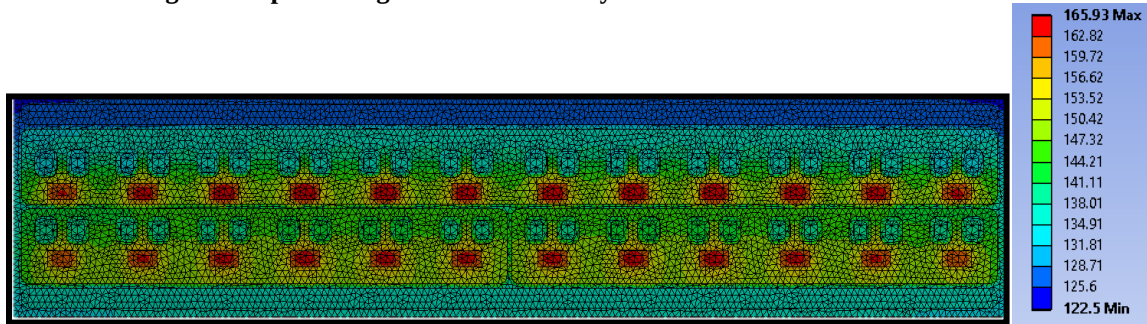


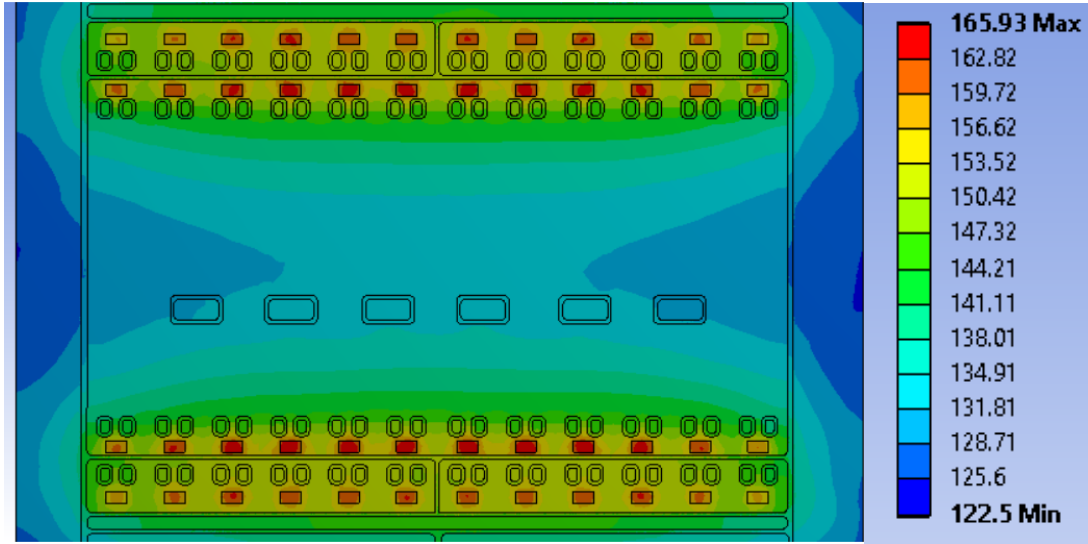
Figure 17 : FEA results with 70 W loss per die (bottom switch) and 2000 W/m²K: (a) temperature and mass vs. Cu thickness for ML ODBC layers, and (b) cross-section of a datapoint from the ML ODBC showing the temperature gradient between layers.

Furthermore, initial thermal simulations were completed on the entire unified SiC bridges of the common substrate. Once again, the thermal loss of 70 W per die was assumed for comparison's sake. In this simulation, consideration was given to the two H-bridges that form a single common substrate and a single side of the resonant converter. There are forty-eight 1.7 kV SiC MOSFET bare dies in total in the simulation. They are spaced about 8 mm apart in order to minimize thermal coupling between the dies. The dies are also rotated in order to parallel them along their shorter side. From prior simulation work, this has also shown to minimize thermal coupling. A cooling coefficient of 2000 W/(m²K) is applied to the backside of the common substrate and steady-state thermal simulations are run. It must be noted that there are some simplifications made, including to the die-attach layer. For such a large-scale simulation, meshing and simulating a thin die-attach layer would be computationally expensive. Furthermore, a conservative cooling coefficient of 2000 W/(m²K) is selected. With proper contact between the iPEBB and the rack-level cooling, this can be significantly increased.

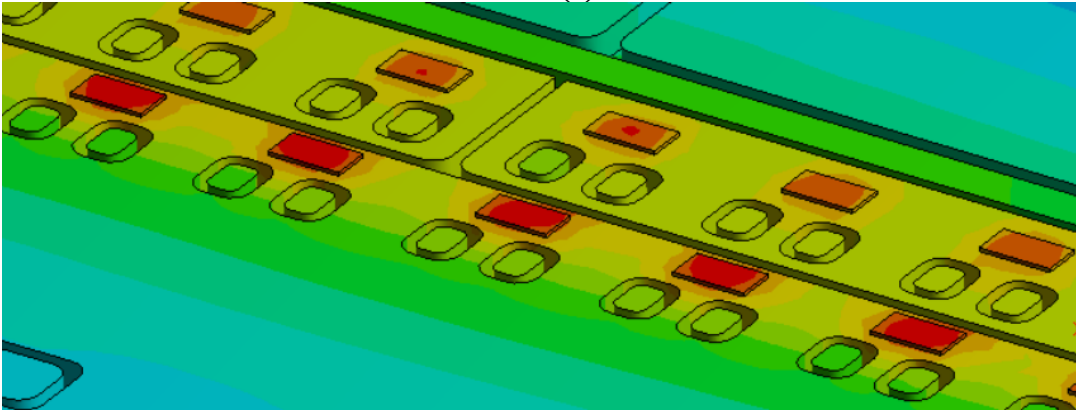
Based on previous thermal simulations, the top copper layer is made to be 3 mm in order to offer the best heat spreading, the middle layer is 2 mm, and the bottom layer is 0.8 mm. This is because the bottom layer has the least impact on thermal performance, and hence can be minimized in order to meet weight requirements.

From the simulation results shown below in Figure 18, there are some interesting results. The common substrate busbar helps spread the heat out of the top switch's bare dies that are in parallel. The two bridges are placed far enough apart that there is minimal thermal coupling between the two H-bridges. Furthermore, the temperature near the center where the capacitors will be placed is ~120 Celsius. Additionally, from the results it is clear

that thermal coupling still takes place when a large number of bare dies are placed along the same line. The dies towards the center heat up more than the ones on the outside. The bare dies for the bottom switch are cooled more than the top switch due to the fact that the gate and Kelvin pads limit the heat spreading of the top switch.



(a)



(b)

Figure 18: (a) Thermal performance of intergrated SiC bridges of a common substrate, and (b) close-up view of the bare dies (70 W loss per die and 2000 W/(m²K)).

A closer look at the dies shows that the gate and Kelvin pads limit heat spreading and concentrate the heat in a localized area that increases the maximum junction temperature the devices experience.

In the actual iPEBB operation, the inner bridges will be soft switching and at a higher frequency (500 kHz), which will allow for the minimization of losses. Meanwhile, the outer bridges will be hard switching at a lower switching frequency (10-30 kHz). Although it is difficult to predict all the losses the converter might experience without accurate electrical simulations and hardware testing, the steady-state thermal results do give an idea of the thermal performance of the multi-layer ODBC-based common substrate design.

The cooling of the common substrate is also an area where additional analysis and simulation work will be needed. As previously stated, by eliminating an additional baseplate and interface layer, the common substrate can be cooled more easily and in a more unified way. Literature on cooling strategies for PEBBs [21] shows that various options can be considered. For previous PEBBS such as the PEBB 1000, air cooling was considered due to the power rating of the converter. But for a 250 kW, high-density converter such as the iPEBB, rack-level cooling will be needed. There are many challenges associated with rack-level cooling, including getting good contact between the bottom of the iPEBB and the power corridor's rack-level system.

Other options are also possible, including heat pipes that allow for more rapid spreading of heat from concentrated areas. All these options remain viable for the iPEBB and will need to be explored to advance the cooling technology of PEBBs.

3.7 *Thermo-Mechanical Analysis*

Having thick copper near the die raises concern about thermo-mechanical stress and reliability on the die-attach layer. Most reliability work has looked at the thickness of the die-attach itself and the impact of CTE on the DBC substrate. It is shown that excessive CTE mismatch can warp or damage the bare dies [44].

Thermo-mechanical simulations on a multi-layer organic substrate were presented in [45]. A thermal cycle simulation between 40 °C and 150 °C was completed and the stress on the solder die-attach was calculated. Simulation results show a slight increase in the strain energy density values of the solder layer when the top copper metallization is increased from 0.5 mm to 4 mm. This has the potential to erode the reliability of the common substrate, but further analysis on the impact on the system-wide reliability must be completed. From a reliability standpoint, it has been highlighted that the ODBC was able to handle more than 5000+ thermal shock cycles without delamination. This provides a major advantage for ODBC substrates that the iPEBB can leverage. Additional reliability testing will be needed to understand the full impact of converter-level reliability.

Chapter 4 ODBC Switching-Cell Design

4.1 Introduction

To better understand the electrical and thermal implications of using an ODBC substrate instead of traditional ceramics, a half-bridge switching cell was designed and fabricated. This ODBC switching cell will help in understanding critical aspects of using organic substrates for the iPEBB. Furthermore, the electrical and thermal viability of a single-layer module design is explored.

4.2 Switching-Cell Design

The switching cell was based on patterning PD samples and was designed based on substrate availability. Despite this, critical electrical and thermal trade-offs for the ODBC-based substrates are analyzed. A 50 mm by 50 mm ODBC sample was patterned to form a half-bridge design. The substrate has 0.5-mm-thick copper for the top and bottom metallization, and a 35- μm -thick dielectric layer. A majority of the previous work on organic substrates has focused on the thermal aspect and how best to overcome the poor thermal conductivity of the dielectric layer. In this work, thermal measurements will be taken and an electrical analysis will be completed. The work in this section is carried out based on substrate availability and packaged with standard packaging procedures and materials.

4.3 Electrical Analysis

The parasitic capacitance of the DBC patterning is a major contributor to the EMI performance of a module. A generalized power module layout, in which the different nodes

of a half-bridge power module are color coded with the module layout, is illustrated in Figure 19. The figure shows the parasitic inductances from the leads and traces as well as the parasitic capacitance to the baseplate. The three terminals of the module (D1, S1D2, and S2) are associated with the colors red, green, and blue, respectively. Shown in green is the switching-node capacitance, which is a major source of CM noise. Induced current from the parasitic capacitance can flow into the rest of the system. This induced current (and the associated parasitic capacitance) is the major focus of EMI-related research. Often, the solution to EMI issues in power modules is to slow them down so they do not have harsh transients. Unfortunately, this means not utilizing all of the technology's benefits.

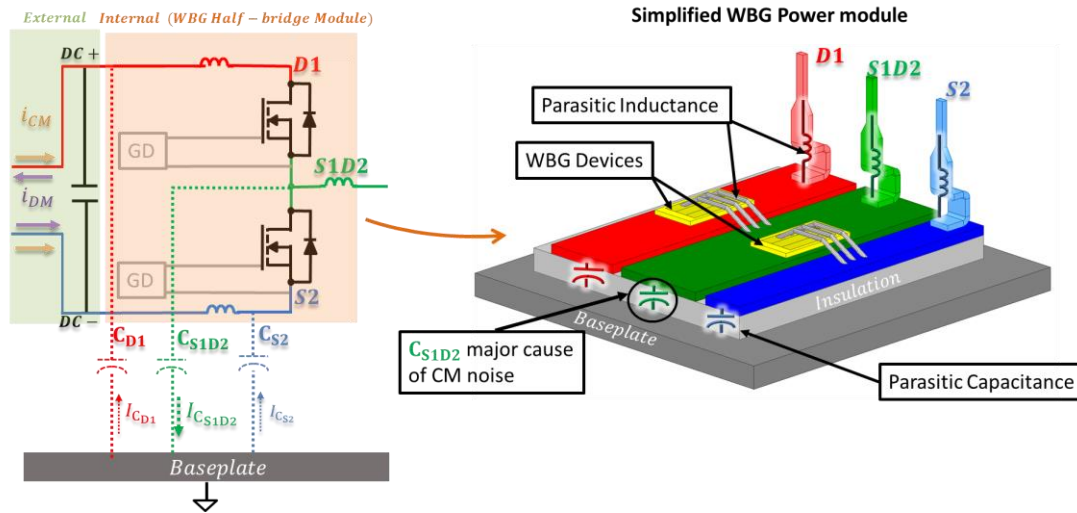


Figure 19: Half-bridge module schematic and generalized half-bridge module layout highlighting the parasitics.

Most power electronics converters use magnetic filters to reduce EMI flowing from the power stage into the remaining system. Often time these are passive filters and can take up large amounts of space. Both DM and CM filters can be used separately or in conjunction to reduce the overall noise within the system [46]. Work has been done on filter building blocks (FBBs) that can be used for various three-phase systems. Although

concepts like FBB seem promising, the filter magnets' high-frequency performance is often limited by their magnetic materials and filter parasitics [14]. Furthermore, work has also been done on digitally active filters to help reduce the size and weight of the magnetics. Although digitally active filters are an attractive option due to their ability to reduce the size of magnetic components and work with existing controllers, their cost and reduced performance at high frequencies limits their usefulness [47].

Furthermore, traditional damping techniques, such as RC snubbers and ferrite beads, have been shown to be effective for WBG devices. The benefit of RC snubbers is that they are easy to implement and affordable. The trade-offs come in the form of increased losses. In most cases, the RC snubbers are placed close to the half-bridge in order to provide a path for the high-frequency oscillations to bypass. Most of the heat and losses come from the added resistor, but the resistor can be adjusted to minimize losses and achieve needed damping [48]. Another method for reducing EMI involves damping oscillations with ferrite beads [49]. The ferrite beads are placed in the current path and offer high-frequency damping. It is often preferred to utilize RC snubbers due to their higher efficiency and minimal loss. The trade-offs for this method include an increased implementation complexity compared to other methods. The bead's selection is often tedious and requires careful analysis and characterization to properly work within a circuit or motor-drive system [49]. Fundamentally, the RC snubbers and ferrite bead methods offer the ability to reduce voltage oscillations during switching events, which minimizes EMI [50].

In [50] the ferrite bead eliminates a majority of the voltage oscillations, and shows a reduction in EMI noise towards the 30 MHz range. Another method for reducing EMI

involves balancing the impedance to form a Wheatstone bridge. In this formation, the CM current can be canceled. This method's challenge is that the parasitic extraction must be very accurate and requires an extended design time. But this method has shown to reduce EMI noise up to 30 dB in the 150 kHz to 30 MHz range. Other techniques involve balancing the parasitic capacitance ground in motor-drive applications by separating heatsinks [51]. This decouples the interaction between the upper and lower switches and reduces differential-mode (DM) EMI, which reduces the chances that the DM noise exacerbates CM noise [51]. Beyond the traditional EMI mitigation strategies, new and unique methods have also emerged to minimize EMI in the packaging or circuitry level. One of these methods involves the use of an active gate driver (AGD) [52].

This gate-driver technology uses an adjustable gate resistance during switching events to reduce ringing. By decreasing the ringing, there is less voltage oscillation and hence less EMI noise being produced. In most cases, resistors are placed directly inside a module or on a gate driver to slow down the switching speed, but this is an inefficient method that can increase losses [53]. By employing AGD, the EMI can be reduced without having to sacrifice a large amount of efficiency. The AGD uses various resistor values during a switching transient to reduce oscillations. The gate resistance system can also use a closed-loop control to improve the response speed. An AGD with high resolution has also been developed to incrementally increase or decrease the resistance level [53]. This, in turn, allows for more precise control of the switching transient and reduces EMI. It has been shown that this AGD can reduce EMI noise by 13 dB at 200 MHz and 10 dB at 1 GHz [53]. Although this is an attractive method of reducing EMI while preserving efficiency, the development and implementation of AGD can be tedious and time-

consuming. The cost of implementation is often a major roadblock for AGD to be widely adopted.

Most researchers believe that the best way to reduce EMI is to minimize it as close to the die level as possible during the design process. Doing so minimizes the need for external solutions that add unwanted complexity and costs. That is why in recent years, WBG device packaging has taken on a more prominent role in EMI mitigation strategies. The literature shows that one of the best ways to reduce the EMI caused by current and voltage ringing is to minimize the power loop's parasitic inductance [54]. This insight has given birth too many novel and unique methods for reducing the packaging-level inductance.

Another interesting EMI mitigation strategy that can take place inside of modules is the balancing technique. This technique has been described in the previous section, where it was done externally with a Wheatstone bridge. This method seeks to balance the parasitics within the module to aid in reducing EMI. As shown in [55], an unbalanced DC bus can cause the spread and propagation of EMI noise through a system. Through this novel method, a noise reduction of up to 30 dB is seen at the 30 MHz regions. Although conventionally, 30+ MHz tends to be in the radiated EMI region, there is also conductive EMI in play. The unbalanced DC bus causes an unbalanced voltage to drop along with the positive and negative terminals. This voltage drop can cause CM noise to be emitted through the capacitance going to the baseplate [55].

The voltage oscillation during testing can couple with the capacitance and inductances causing large DM-to-CM conversions. The literature focuses on the IGBTs and not SiC MOSFETs, but similar mitigation strategies can be explored for SiC devices. It is recommended that the module be built with flip-chip technology to reduce the inductance in the power loop and have a balanced design in order to suppress this conversion [55]. It is also noted that the gate and source pads must

be taken into consideration, since they add additional parasitics to the DC bus and can cause EMI-related issues. It is also recommended that stray capacitance from the gate be minimized as well. The copper pads should be minimized for the gate pad but this solution must be weighed against increased manufacturing complexity. It is also essential to balance the parasitic inductance within the module, and it is recommended that decoupling capacitors be placed within the module to reduce the commutation loop [56]. This interesting method shows that EMI-related issues can be addressed in the geometry and the layout of the power module and at the packaging level. This method has not been extensively studied beyond [55], but it shows merit for further analysis and exploration to better understand the benefits and limitations of the balancing technique.

Another unique method for reducing EMI within a converter involves the leakage cancellation method [57]. In this method the ratio of the S1D2 capacitance (C_{ag}) to the total module capacitance to the baseplate (C_{bp}) can be manipulated to minimize or cancel the leakage current through the baseplate. In [57], the baseplate capacitance is manipulated so that the ratio between C_{ag} and C_{bp} is equal to $q_{ac} = 1/4$. It is shown that the induced current through the baseplate can be cancelled out. It also shows that different values of q_{ac} can exacerbate the leakage current. A CM equivalent model is also presented in order to estimate the leakage current and the overall CM noise. It should be noted that this is highly specific for a single-phase half-bridge inverter implementation where the input and output impedance are equal to each other and cannot be universally applied. Even though it is highly dependent on the topology, this evaluation is valuable because it demonstrates that proper application of a suitable CM model can be employed to reduce emissions in a deterministic fashion, even without the introduction of CM filters.

This method was of interest for the ODBC switching cell. Most EMI-related work focuses on DBC-based power modules, where the total parasitic capacitance is bounded by

the 0.25 mm to 1 mm ceramic thickness. The ODBC can have dielectric thicknesses that are 10 times thinner than the thinnest ceramic. In [58], the issue of high coupling capacitance is shown to be an intrinsic feature of organic substrate-based power modules. In this paper, an organic substrate-based power module will be modelled and evaluated to demonstrate that EMI can be mitigated through careful layout of the substrate regions.

To better understand and analyze the impact of a thin dielectric layer on a power module's EMI performance, a half-bridge power module was designed and fabricated using an ODBC substrate. Figure 20 (a) shows the layout of the ODBC module color coded to the half-bridge schematic shown in Figure 20 (b). The half-bridge was designed with the EMI mitigation strategy of reducing the A node area to be 25% of the total substrate area. This has been shown to minimize C_{ag} , which in turn minimizes CM noise.

The cross-section view of the ODBC module is shown in Figure 20 (c), where a 35 μm polyimide layer provides electrical isolation between the 0.5 mm top and bottom copper layers. There are two parallel 1.7 kV SiC MOSFETs per switch. The design also takes advantage of the reverse conduction characteristics of the SiC MOSFET by eliminating the need for external antiparallel diodes. For the gate loop, a balanced inductance is achieved by having individual gate and Kelvin connections for each die. The Kelvin connection prevents negative feedback between the gate and power source and allows for faster switching speeds. According to the ANSYS Q3D extractor, the gate-loop inductance is 6 nH for each MOSFET. The power-loop inductance is 17 nH at 1 MHz when including the leads.

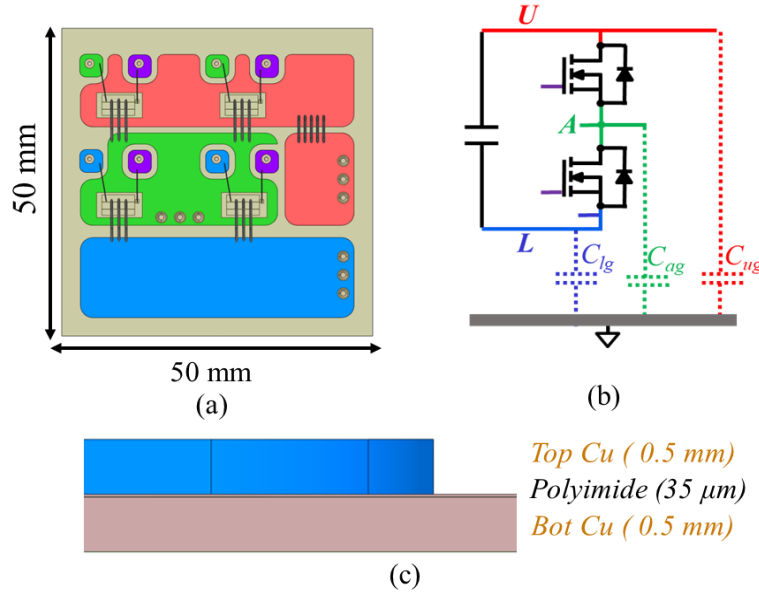


Figure 20 : (a) ODBC-based half-bridge layout, (b) half-bridge schematic, and (c) cross-section of the ODBC.

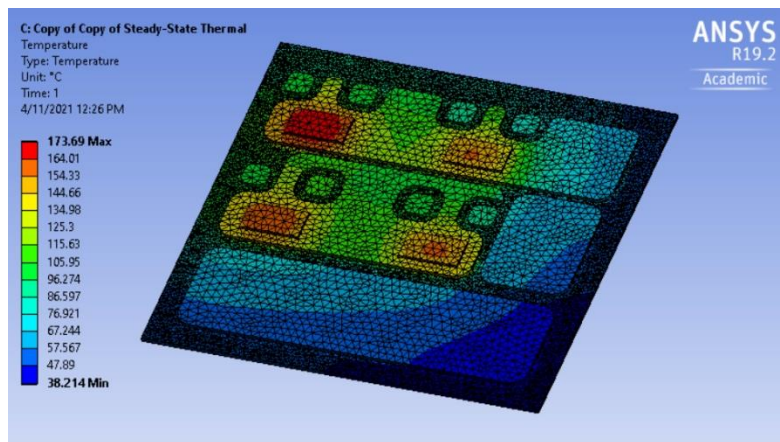
4.4 Thermal Analysis

Patterning the ODBC substrate in order to achieve leakage cancelation does come with some critical trade-offs. In order to minimize the green pad, the four dies are forced to clump together in one corner of the module. Furthermore, the gate and Kelvin pads near the dies remove critical copper needed for heat spreading. A majority of the substrate area is not used for die placement since it is critical for the leakage inductance cancelation method.

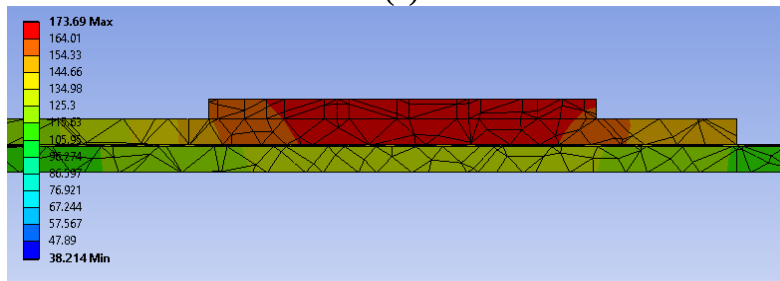
Shown below in Figure 21 (a) is the ODBC switching cell with a loss of 70 W per die and a cooling coefficient of 2000 W/m²K. From the result, it is clear that the top left die heats up 20 to 30 degrees more than the other devices on the switching-cell. This is due to the fact that there is minimal copper for the heat to spread across. Figure 21 (b) shows the cross-section of the top right bare die. As opposed to the thermal results shown with

thicker metallization for the common substrate, the thinner metal in the actual switching cell limits heat spreading. The location of the polyimide layer is clearly denoted, because that is where the heat is spread out at an 80-degree angle, instead of the 45-degree angle that would be the case for DBC substrates.

Meanwhile, the bottom right bare die is much cooler, even though it is also near many etched patterns. The copper on the bottom and top layers allows for full heat spreading in all directions, as shown in Figure 21 (b).



(a)



(b)

Figure 21 : (a) ODBC switching-cell thermal performance with 70 W loss per die and 2000 W/m²K, and (b) cross-section of the top left die.

4.5 Switching-Cell Packaging

The packaging of the ODBC module begins with etching the copper substrate to form the half-bridge design. To achieve the desired pattern, a Kapton mask is used to protect the 0.5 mm top copper layer from the ferric chloride etchant solution. The Kapton mask was extended by 600 μm to compensate for the over-etching that will take place during the patterning process (Figure 22). This is especially critical for the gate and source pads where over-etching can limit pad space or remove copper regions needed for the dies' heat spreading. Furthermore, the thin dielectric layer means that slight variations produced through etching of the top copper can impact the capacitance-to-baseplate by between 10-15%. Due to the adjustment in the Kapton mask and standardized etching process, the variations in capacitance between ODBC samples were minimized.

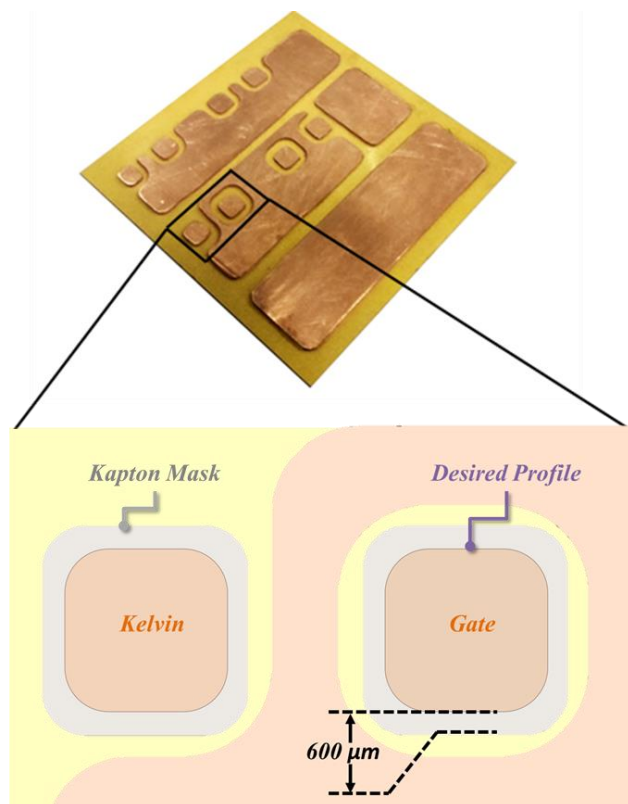


Figure 22 : Example of the chemical etching process for the ODBC module.

The etching variation is shown in Figure 23, where the modified Kapton mask and the original mask are shown. It is clear from the results that the original mask over-etched the gate and Kelvin pads, while the modified Kapton mask was able to preserve much of the needed copper. Furthermore, the over-etching removed critical areas where the leads and wire bonds will need to be placed.

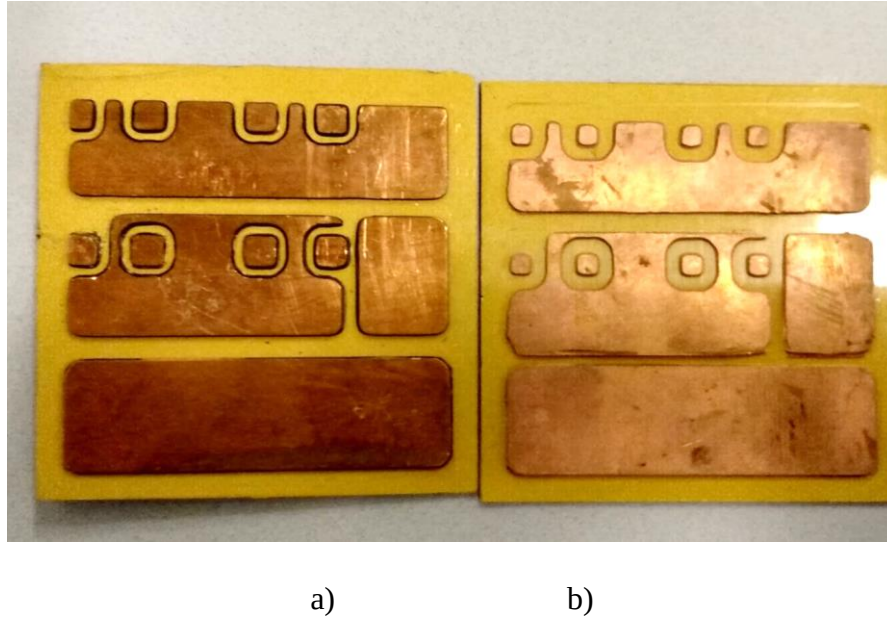


Figure 23: Etching with a) a modified Kapton mask, and b) the original mask.

The ODBC module is fabricated using high-yield, industry standard technology. Cree 1.7 kV 45 m Ω bare-die MOSFETs are placed on bare-copper ODBC substrates. 10 mil Al wire bonds are used for interconnects because they are a standard, cost-effective, and high-yield technology. Sn96.3/Ag3.7 solder was used for the die-attach due to its simple processing and high melting temperature of 221°C. The module is encapsulated in SilGel 612, which is a cost-effective and widely available silicone gel with a high dielectric strength of 20 kV/mm. A special housing structure was printed using Formlabs high-temperature resin and was attached to the substrate using high-temperature EPO-TEK

353RD. The summary of the materials used in fabrication is shown in Table 4. The layout of the different material locations is shown in Figure 24. The fabricated ODBC module prototype is shown Figure 26.

Table 4 : ODBC Switching-cell packaging material selection.

Component	Selected Material
Die	Cree 1.7 kV 45 mΩ Bare Die
Die Attach	Sn96.3/Ag3.7 Solder
Die Interconnect	10 mil Al Wire Bond
Encapsulant	SilGel 612
Housing	Formlabs High-Temp Resin
Substrate	ODBC

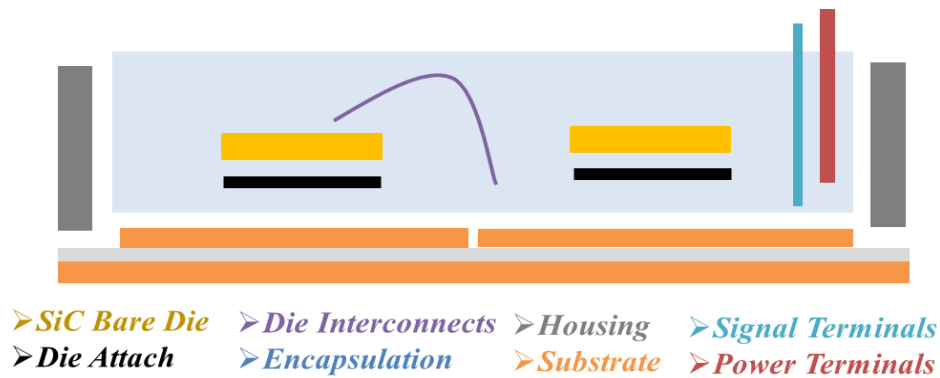


Figure 24 : Layout of different components in ODBC module.

Additional work was done in order to explore the die-attach further. Although solder is the industry standard and has decent performance, silver sinter paste also holds a lot of promise. As an alternative, NBE nanoTach nano-silver (Ag) paste is being explored for pressure-less silver sintering of the dies. An Ag sinter die-attach offers many advantages, including minimal voiding, higher thermal conductivity, and good thermal cycling performance. Most Ag sintering takes place on Ag-plated substrates. In this work,

the sintering is done on the bare Cu to reduce cost. This is made possible by removing the oxidation layer and using higher-flux Ag sintering paste. Initial shear testing using the Ag sintered bond on bare Cu shows a good bonding strength of 28 MPa. The grain size of the bare Cu and the oxidation level will impact the quality of the bond.

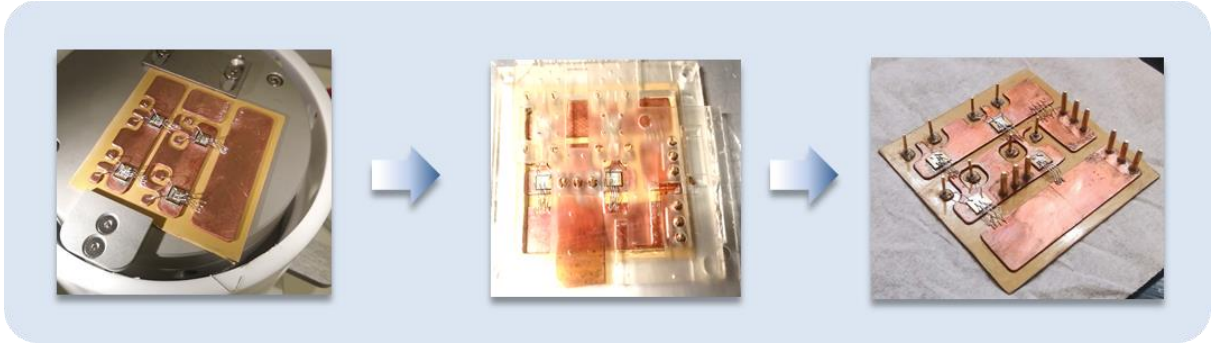


Figure 25: The ODBC switching-cell packaging process.

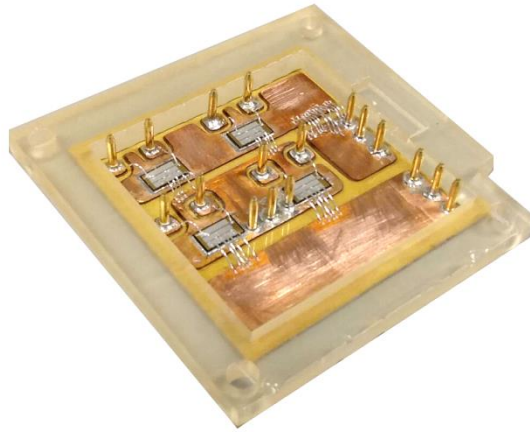


Figure 26: 1.7 kV ODBC switching-cell prototype.

Chapter 5 ODBC Switching-Cell Testing

5.1 Introduction

To better understand the electrical and thermal implications of using an ODBC substrate instead of a traditional ceramic, a half-bridge switching cell was designed and fabricated. This ODBC switching cell will help in understanding critical aspects of using organic substrates for the iPEBB. Crucial aspects of the ODBC switching cell, including the switching performance, EMI, and thermal performance, were analyzed.

5.2 Static Characterization

The ODBC switching cell had static characterization performed on the module in order to verify that the SiC MOSFET devices survived the packaging process and are functioning properly. Figure 27 shows the I-V curves at 25 °C for different V_{GS} values applied to each of the four dies. The results show reasonable performance between the four dies in comparison with their data sheet results. Based on these initial static characterization results, dynamic testing was performed in order to see the switching performance.

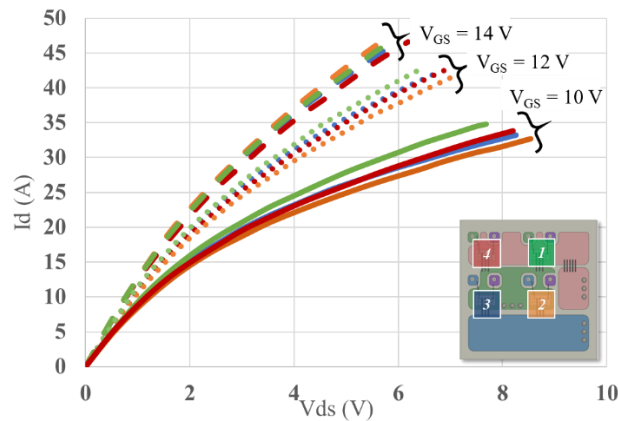


Figure 27: Output characteristics of drain current vs. drain-source voltage for switching cell ($T_J = 25$ °C).

5.3 *Double-Pulse Test Setup*

To test the ODBC module, a testbed was developed to carry out dynamic electrical testing. Since the module's target switching frequency is 500 kHz, high drive currents are needed. As a result, current boosters were included to guarantee optimal performance and fast switching speed. Since the current boosters increased the distance between the gate driver IC and the MOSFETs, a PNP transistor was placed close to the module to provide a low-impedance path for the Miller clamp. Based on the system requirements, the gate drivers use the UCC21750 IC, which supports switching frequencies up to 1 MHz, has high driving currents, and reasonable rise and fall times. The gate drivers are designed to be vertically connected to the rest of the setup to allow for thermal imaging of the module during testing.

The gate drivers are attached to the interface board, which serves as a platform to connect the module to the gate drivers and the DC bus. The interface board includes decoupling capacitors to help minimize the power-loop inductance and provide measurement points for the drain-to-source and gate-to-source voltages and drain current. The interface board also has strategic cutouts above the bare dies for thermal monitoring and imaging (Figure 28). Furthermore, the interface board also hosts the input and output capacitors needed for zero-voltage switching (ZVS) buck operation. This will be completed as part of future work on verifying the switching speed of the ODBC switching cell.

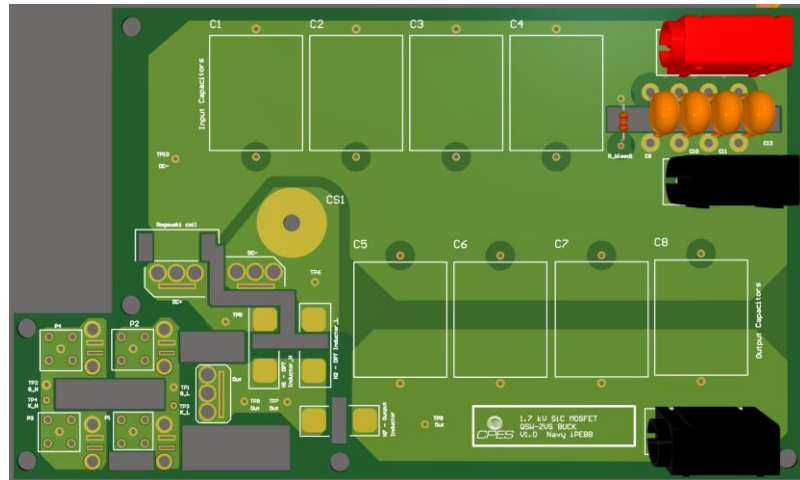


Figure 28: Interface board for the ODBC switching cell.

The complete iPEBB testbed setup, shown in Figure 29, will be used to obtain double-pulse test results. Mini-BNC connectors help interface the gate-driver boards to the interface board and offer it mechanical support as well. The interface board is also designed to allow for space around the edge of the module that will allow for easy clamping or bolting down to the cold plate for improved cooling.

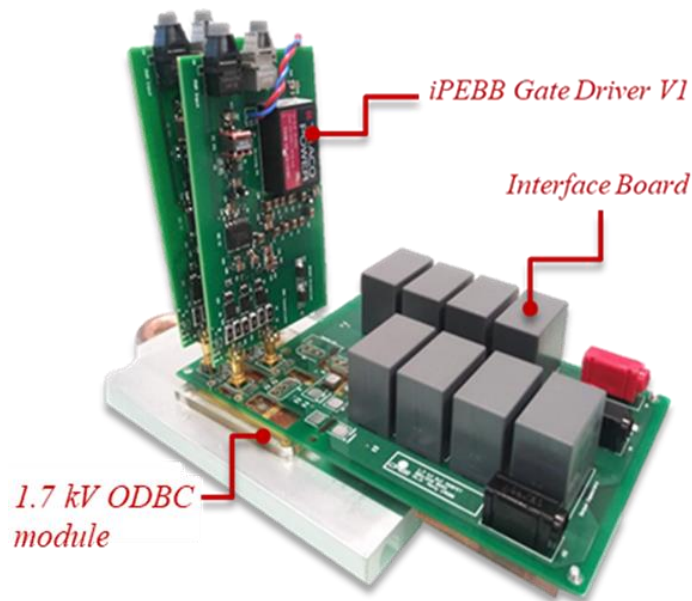


Figure 29 : The iPEBB testbed setup for dynamic electrical testing.

5.4 Double-Pulse Test Result

Double-pulse tests (DPTs) were performed at room temperature on the fabricated half-bridge ODBC module using the setup shown in Figure 29. A DPT is a standardized test methodology used to assess the switching characteristics of half-bridge modules. The double pulse was applied to the bottom-side switch of the module, and the body diodes of the topside SiC MOSFETs were used for freewheeling the current when the bottom-side MOSFETs were off. The schematic for the DPT performed is shown in Figure 30.

Table 5 lists the conditions and equipment used for the DPT. To measure the drain-to-source voltage (V_{DS}) of the high-side SiC MOSFETs, a high-voltage, high-bandwidth (200 MHz), differential probe was used. An SDN-10 shunt resistor was used to measure the MOSFET drain current (I_D). A 380- μ H inductor was placed across the top-side switch. A gate-to-source voltage (V_{GS}) of 20 V and -4 V was applied to turn on and turn off the bottom-side MOSFETs. Figure 31 shows the turn-on and turn-off switching characteristics of the module at 1 kV and 53 A. External gate resistances of 10 Ω and 5 Ω were used for the turn-on and turn-off, respectively. As shown by the figure, at turn-off the dv/dt approaches 27 V/ns, and the voltage overshoot is $\sim 10\%$ of the DC bus voltage. During turn-on, the dv/dt is 16 V/ns. Also, during turn-on, the di/dt is approximately 1.8 A/ns and the current overshoot is $\sim 55\%$ of the inductor current.

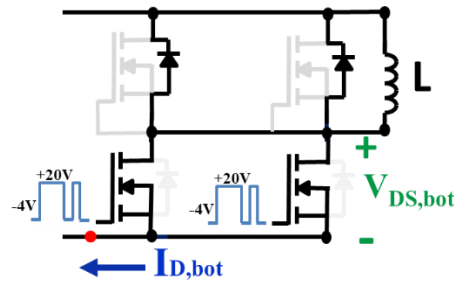


Figure 30 : Schematic of double-pulse test (DPT) of top switch (two MOSFETs in parallel).

Table 5 : Double-pulse test setup.

Components	Parameters
Inductor	380 μ H
Gate Turn-off/ Turn-on Voltage	-4 V / +20 V
Gate Turn-on Resistor	10 Ω
Gate Turn-off Resistor	5 Ω
DC Bus Voltage	1 kV
V_{DS} Measurement	Tektronix THDP0200 H
I_{DS} Measurement	SDN-10 Shunt Resistor
Oscilloscope	Tektronix MSO54
Power Supply	ALE Systems 802L

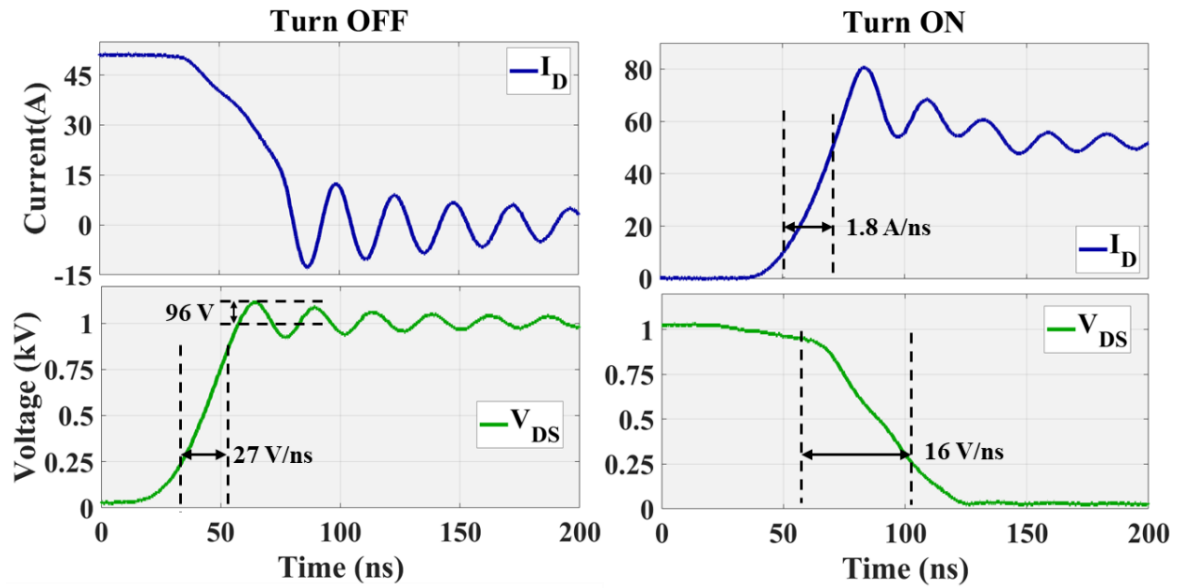


Figure 31: Double-pulse test of the single-layer ODBC module showing the (a) turn-off and (b) turn-on waveforms at 10 Ω and 5 Ω gate resistance, respectively. Drain current shown on top and drain-source voltage shown on the bottom.

Figure 31 shows the turn-on and turn-off switching characteristics of the module at 1 kV and 53 A. External gate resistances of 10 Ω and 2.5 Ω were used for the turn-on and turn-off, respectively. As shown in Figure 32, during turn-off the dv/dt approaches 36 V/ns and the overshoot is $\sim 9\%$ of the DC bus voltage. During turn-on the dv/dt and di/dt are 16 V/ns and 1.7 A/ns, respectively. Furthermore, a current overshoot of 28.6 A is seen during turn-on. The estimated switching loss for the device during turn-on is 1.9 mJ and during turn-off is 1.1 mJ. The switching losses for the entire turn-on and turn-off time are 3 mJ.

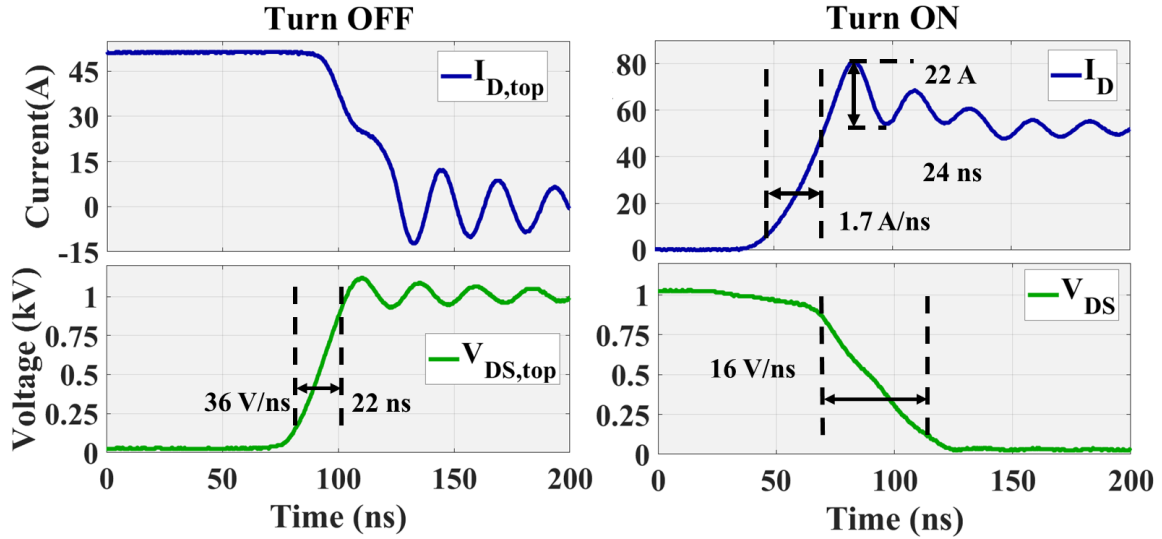


Figure 32 : Double-pulse test of the single-layer ODBC module showing the (a) turn-off and (b) turn-on waveforms at 10 Ω and 5 Ω gate resistance, respectively. Drain current shown on top and drain-source voltage shown on the bottom.

5.5 EMI Test Setup

One of the major concerns with organic-based substrates like the ODBC is that the thin nature of the polyimide dielectric layer raises potential concerns with regard to CM behavior and conducted emissions. Therefore, as part of this work, a detailed analysis of the CM implications of the module design presented herein was conducted. The EMI

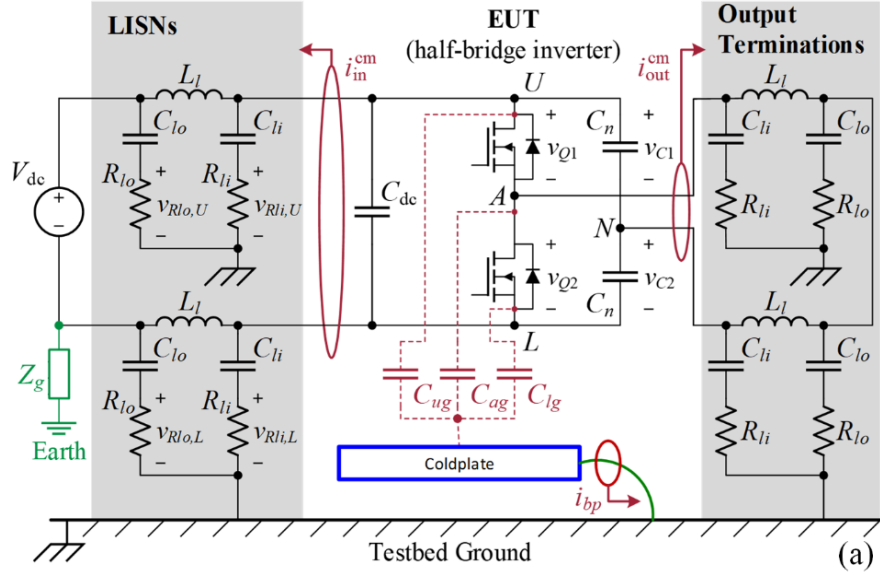
testing of the ODBC switching cell was completed by the University of Alabama as part of a collaborative effort.

This work was based on the leakage current cancelation method mentioned previously. The EMI characterization testbed shown in Figure 33 (a) was leveraged for this purpose. This testbed is based on the conducted emissions portion of the MIL-STD-461 [59] but is modified to account for the parasitic coupling of the converter output to the system ground network, which is a common characteristic of practical converter systems. The common-mode equivalent model (CEM) of this testbed when fitted with a half-bridge inverter, as shown in Figure 33 (b), was recently published [60] [61]. Since close agreement between the predictions of the CEM and the measured behavior of the testbed was achieved in [60], this CEM and testbed are employed as a benchmark to evaluate the CM emissions impact of the ODBC module and compare it to a commercial 1.2 kV Cree module.

Conducted emissions are quantified (and therefore compliance is determined) by measuring the voltage induced across the inboard line impedance stabilization network (LISN) resistors, R_{li} , during operation of the equipment under test (EUT). From the perspective of the LISNs, the CEM of Figure 33 (b) makes it clear that there are two primary paths for CM current flowing through the LISNs to return: (1) via the output terminations and (2) via the power module baseplate. It is primarily the current through this second path that is affected by the module design. In [60] [61], it is shown that the effective voltage source driving CM current through the module baseplate can be expressed as:

$$v_{bp,eff} = \left[\frac{Z_{in}}{2*(Z_{in}+Z_{out})} - \frac{C_{ag}}{C_{bp}} \right] \cdot \left(\frac{v_q}{2} \right), \quad (1)$$

Where Z_{in} and Z_{out} represent the CM impedance of the input and output terminations to the ground plane, respectively. C_{ag} represents the capacitive coupling of the phase node, C_{bp} represents the total coupling of all three module terminals to the ground plane, and v_q represents a trapezoidal stimulus formed by the difference in the two switch voltages. The difference operator in Equation (1) implies the possibility of a CM voltage cancellation for this topology that would eliminate current through the power module baseplate [60] [61]. For the special case of the testbed in which the input and output terminations are equal ($Z_{in} = Z_{out}$), baseplate current elimination occurs when $C_{ag}/C_{bp} = 0.25$.



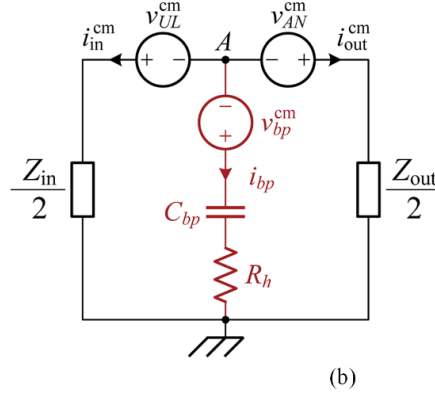


Figure 33 : (a) Practical configuration of EMI characterization platform with half-bridge inverter as the equipment under test (EUT), (b) the CM equivalent model of this system [51].

It is noted that other values of terminating impedances will shift this cancellation point to a different capacitive ratio. This CM voltage cancellation has been previously validated by manipulating the capacitive coupling of a commercial SiC MOSFET half-bridge module (CAS120M12BM2) [60]. In this work, the analysis in [60] [61] is leveraged to assess the CM emissions impact of the module coupling characteristics of the ODBC module in question.

This is done by separately exercising the CEM of Figure 33 (b) with the measured values of baseplate coupling for the ODBC module and for the reference Cree module, which are provided in Table 6.

Table 6: Module baseplate capacitance value.

Module	C _{UG} (pF)	C _{AG} (pF)	C _{LG} (pF)
CAS120M12BM2	191	255	102
Prototype ODBC	459	318	503

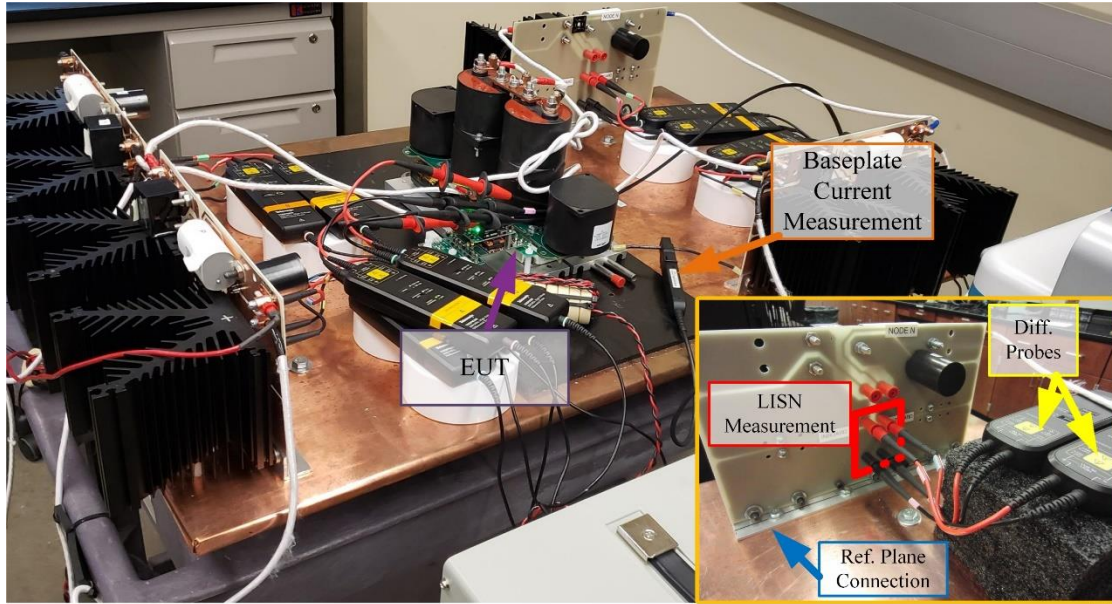


Figure 34 : Realized EMI characterization testbed [50].

5.6 EMI Test Results

Each module (switching cell) was experimentally evaluated using the testbed shown in Figure 34. The testing and results were completed by the University of Alabama in order to verify the ODBC design. Differential probes were used to measure the voltages across each LISN resistor (R_{li} and R_{lo}). Often, leakage current through the baseplate can be calculated from the LISN resistors, but can also be gathered by measuring with a current probe placed between the cold plate (where the modules are mounted) and the ground.

For testing, each module is evaluated in a half-bridge inverter operating with fixed-duty-ratio pulse-width modulation (PWM) at 100 kHz with a dead time of 400 ns and a gate resistance of $2\ \Omega$. It should be noted that extracting the parasitics carefully and considering the various couplings that might take place are critical to the experimental

setup. Further details regarding the parasitics and operation of the testbed are reported in [60] [61].

A comparison of the CEM predictions and the empirical measurement for both modules is provided in Figure 35. The left column presents the results for the BM2 module, and the right column presents the results for the ODBC module. In Figure 35 (a) and Figure 35 (e), a time-domain comparison of the CM LISN voltage is provided for both modules. The CM LISN voltage is calculated via Equation (2):

$$V_{Rli}^{cm} = \frac{1}{2}(v_{Rli,U} + v_{Rli,L}). \quad (2)$$

In the equation, $v_{Rli,U}$ and $v_{Rli,L}$ are the mixed-mode voltage measurements across the upper- and lower-rail inboard LISN resistors, respectively. The LISN voltage is of particular interest since it is often used during qualification. In this system design the CM often dominates over the CM contribution to the EMI noise. From the results, the switching-frequency behavior in the time-domain V_{Rli}^{cm} is similar for both modules. This is because the behavior is induced by CM current flowing through the output termination instead of the baseplate. Furthermore, a high-frequency resonance waveform is seen in the V_{Rli}^{cm} for the BM2 module, while this is not seen in the V_{Rli}^{cm} for the ODBC module.

The different EMI performance of the BM2 and the ODBC module is also seen in the frequency domain graphs shown in Figure 35 (b) and Figure 35 (f). Some key takeaways are:

- At frequencies <1 MHz, the BM2 and ODBC show similar behavior.
- At frequencies between 1 MHz and 10 MHz, the BM2 shows CM resonance at 1-2 MHz.

- A null is observed at 5-6 MHz in the BM2 module, while it is seen at 10 MHz for the ODBC module.

The possible reason for this shift is the different edge rates of the two modules. The ODBC module has only two bare dies in parallel, while the BM2 module has six dies in parallel. The fact that the BM2 module has three times as many dies slows down the switching speed. In fact the switch voltage rise time for the BM2 module is about 176 ns (5.6 MHz), compared to 85 ns for the ODBC module (11.8 MHz).

From these initial results, it is clear that the CEM model does a decent job in predicting the CM LISN voltage. The ODBC empirical and CEM results are difficult to match at high frequencies due to the fact that there are small parasitics within the system. Additionally, the spectral comparisons in Figure 35 (b) and Figure 35 (f) demonstrate good agreement for both the odd and even harmonics of V_{Rli}^{cm} .

Another critical aspect of the EMI measurement is to look at is the CM current flowing through the baseplate (i_{bp}). The baseplate leakage current is shown in in Figure 35 (c) and Figure 35 (g) for the BM2 and the ODBC module, respectively. As previously stated, the CM current is important to understand because the induced current can flow through the rest of the system and increase the conducted emissions seen within a converter. It is also a critical parameter in emissions and compliance standards for power modules and converters. From the baseplate current results, a few key observations can be made:

- The BM2 module i_{bp} waveform shown in Figure 35 (b) demonstrates a peak value of nearly 500 mA. Its oscillation is the same CM resonant frequency that was identified in the V_{Rli}^{cm} spectrum.

- The ODBC module i_{bp} waveform in Figure 35 (g) demonstrates a peak value below 100 mA and no CM resonance is seen.

This is due to the CM voltage cancellation phenomenon described previously because the C_{ag}/C_{bp} ratio of the ODBC module is approximately 0.25; whereas the C_{ag}/C_{bp} ratio of the BM2 module is 0.47. It should be noted that the residual content present in the ODBC module i_{bp} waveform occurs mostly at high frequencies (>10 MHz), as shown in Figure 35 (h).

Importantly, the frequency domain plots of Figure 35 (d) and Figure 35 (e) demonstrate that the baseplate leakage current of the system is reduced by 20 dB across a wide frequency range for the case of the ODBC module, as compared to the BM2 module. This reduction is achieved despite two factors, which are generally known to increase conducted emissions and baseplate current. These include:

The 2.3 times higher total baseplate capacitance of the ODBC module compared to the BM2 module. All other factors remaining equal, this difference would be expected to produce 2.3 times higher baseplate current for the ODBC module compared to the BM2 module due to the attendant reduction in CM impedance.

The second factor is the two times higher switching edge rates achieved for the ODBC module compared to the BM2 module. Again, this difference would be expected to approximately double the baseplate current for the ODBC module compared to the BM2 module.

However, the baseplate current of the ODBC module is both predicted by the CEM and verified experimentally to be a small fraction of the baseplate current of the BM2 module when operated in the same testbed at the same operating conditions. The reason

for this difference is the significant influence contributed by the C_{ag}/C_{bp} ratio on the CM driving voltage expression of Equation (1). It is noted that the implementation of this cancellation phenomenon is dependent both on the converter topology and the impedance of the input and output CM terminations. Nevertheless, this study demonstrates that the C_{ag}/C_{bp} ratio represents an interesting insight that designers can use to reduce CM current even in modules with high capacitive coupling.

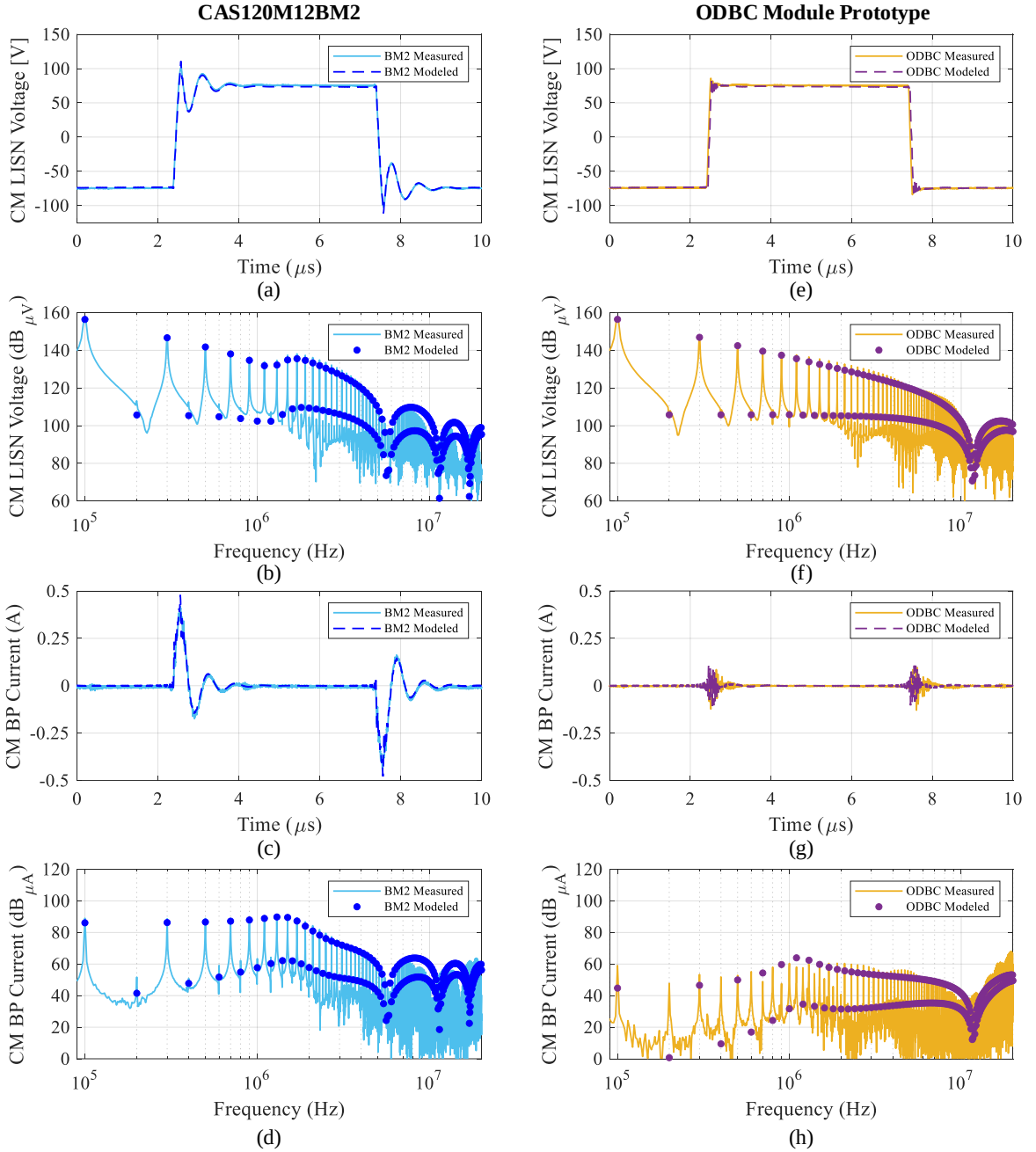


Figure 35: Comparison of CAS120M12BM2 and ODBC measurement results to their equivalent models: (a) time-domain and (c) frequency-domain inboard CM voltage at the input LISNs for the CAS120M12BM2; (e) time-domain and (f) frequency-domain inboard CM voltage at the input LISNs for the ODBC module; and (g) time-domain and (h) frequency-domain leakage current through the MCPM baseplate for the ODBC module.

The design of the ODBC was based on the leakage current cancelation method that was shown in this section. The patterning of the substrate in order to cancel the leakage current at the exact ratio of 0.25 is a highly specialized case. This collaborative effort does highlight some critical aspects of reducing EMI on the packaging level. CM-EMI-related issues do not necessarily come from the die level but from the package level. The reduction in the coupling between the switching node to the baseplate is critical in most application. This can be done in many different ways, such as increasing the insulation thickness and minimizing the switching node footprint.

As previously mentioned, this can have negative effects on other aspects of the power module including thermal properties. This is especially true for the ODBC-based modules where preservation of copper is critical in improving thermal performance. In the next section, empirical thermal results are analyzed to see what key takeaways can be observed from the switching-cell design.

5.7 Thermal Test Setup

Thermal testing on a single-layer ODBC module was completed to better understand the thermal resistance of the module. The test used the JEDEC JESD 51–14 transient dual-interface measurement method, which is a well-known and industry-wide accepted technique [62] [63]. The phase 12B thermal analyzer from Analysis Tech is used to measure the thermal resistance of the two parallel dies comprising the bottom switch of the ODBC module (Figure 36). Again, for this test, the ODBC module has a 35 μm insulation layer with 0.5 mm copper metallization on either side. For thermal testing, the module has been packaged with Cree 1.7 kV, 45 Ω bare dies using Sn96.3/Ag3.7 solder.

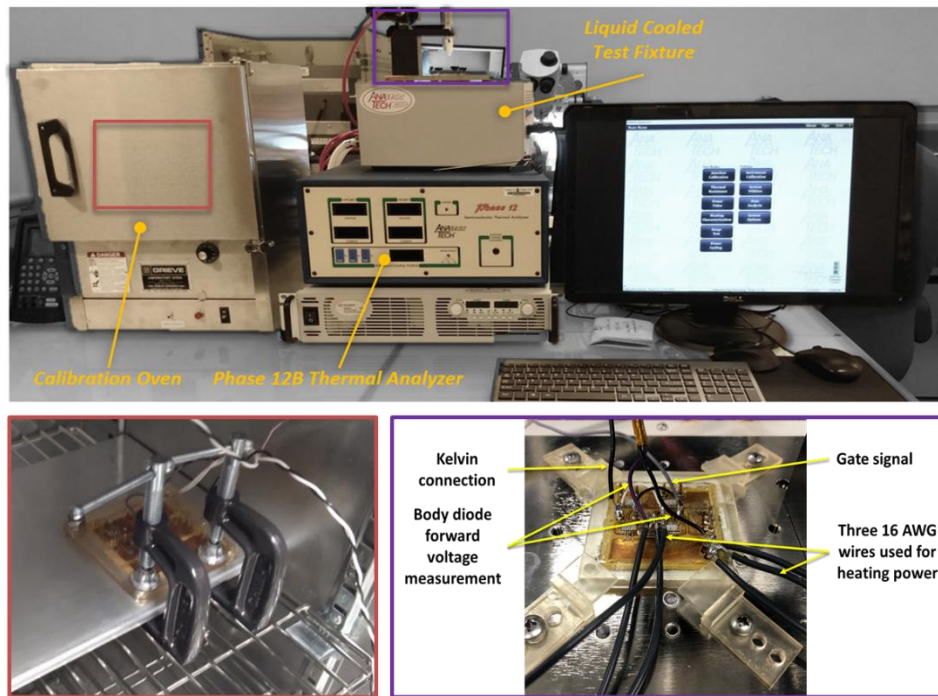


Figure 36: The phase 12B thermal analyzer setup used to measure the thermal resistance of the ODBC module.

5.8 Thermal Test Results

The body diode forward voltages of the bottom switch were calibrated in the oven up to 130 °C and using a measurement current of 20 mA. Heating characterization was performed using the liquid-cooled test fixture (T_{fluid} 26°C) by applying a heating pulse through the channels of the parallel MOSFETs, waiting for the junction temperature to reach steady state, turning the heating pulse off, and measuring the junction-to-ambient thermal impedance as the junction cools (Figure 37). The JEDEC standard requires that heating characterization be performed on the package with two different thermal interface materials (TIMs) placed between the package and the cold plate. One must be a high-

thermal-conductivity TIM such as Dow Corning 340 thermal grease, and the other must be a lower-thermal-conductivity TIM such as silicone oil.

To achieve the same desired steady-state junction temperature during both heating characterizations, the correct heating power needs to be identified. The necessary heating powers were 88 W and 94 W for the silicone oil and thermal grease tests, respectively. Figure 38 shows the thermal impedance over time for the two different heating characterizations performed. The impedance at the divergence point is assumed to be the junction-to-case thermal resistance, $R_{th, jc}$, since the divergence is caused by the difference in thermal conductivity of the TIMs. The results show that the thermal resistance of the module is $\sim 0.89\text{ }^{\circ}\text{C/W}$ (Figure 38).

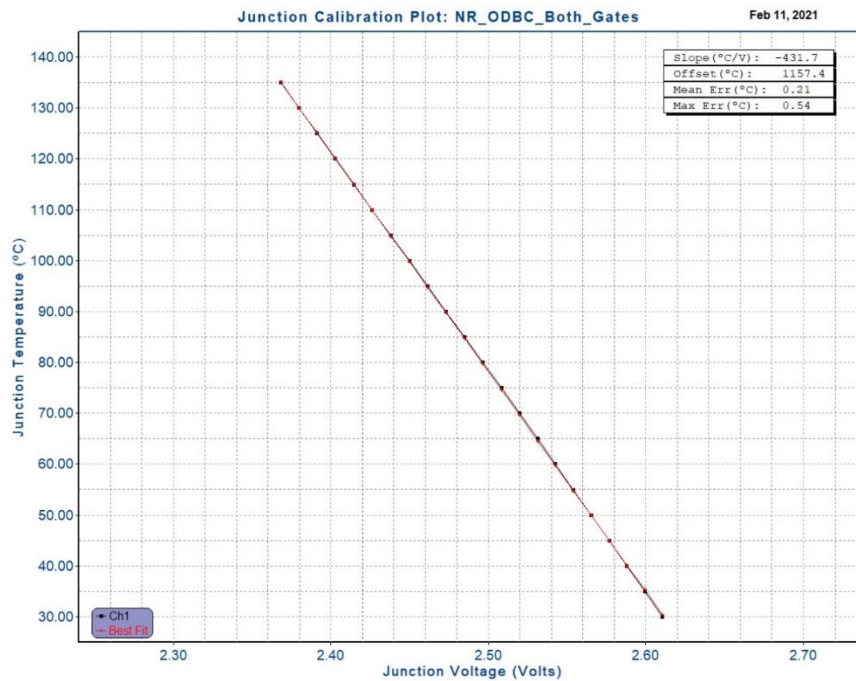


Figure 37 : Junction calibration method.

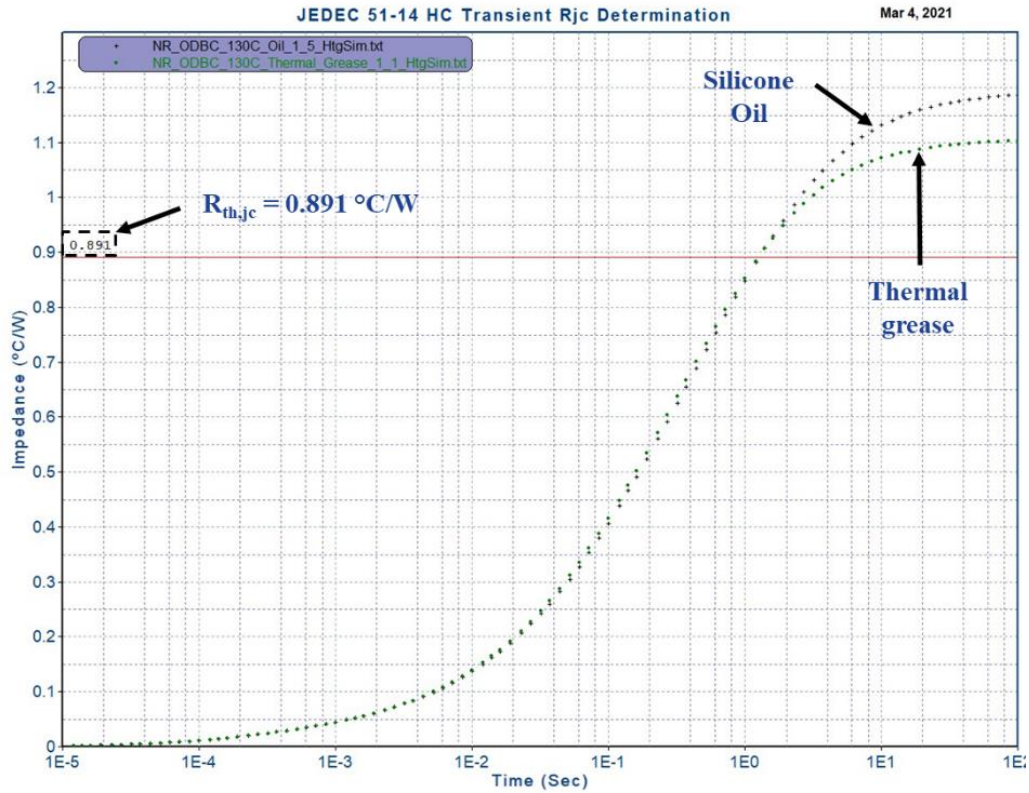


Figure 38 : The thermal impedance of the ODBC module using different TIMs in accordance with the JEDEC JESD 51–14 transient dual-interface measurement method.

The single-layer ODBC module was designed based on substrate availability, but it helps serve as a baseline for further investigation. The thermal performance is in the expected range for ODBC samples with 0.5 mm metallization. These results confirm that the patterning of the substrate will need to be reviewed. The addition of gate and Kelvin pads near the die helps reduce the gate-loop inductance but removes some copper that is critical to heat spreading.

The single-layer ODBC module’s patterning minimized the S1D2 pad to mitigate EMI issues, but it limits the heat spreading and reduces the thermal performance. Going forward, the die placement must be analyzed to maximize the heat spreading, while reducing the S1D2 pad to minimize C_{S1D2} . Additionally, ODBC samples of varying

dielectric and metallization thicknesses need to be measured to develop a trend line and pattern for thermal resistance modeling.

5.9 *Single-Layer ODBC Switching-Cell Discussion*

The results from the electrical testing show that reasonable switching performance can be achieved with the single-layer design. The switching speed of the switching cell can be improved further by minimizing the power-loop inductance. Work has been done on optimizing the inductance cancellation techniques for a single-layer multi-chip power module. But there are limitations in reducing the power-loop inductance with a 2D, single-layer design. Furthermore, even though the design minimizes CP1, there is still capacitive coupling to ground. Higher dv/dt rates can exacerbate EMI-related issues even further.

To achieve improved switching performance, a multi-layer design is preferred. By using two electrical layers, a higher level of mutual inductance cancellation to minimize the power loop can be implemented. This lower inductance will reduce the voltage overshoot and oscillations, enabling faster switching. Furthermore, a multi-layer design also offers the ability to employ a CM screen, which can redirect the CM current produced by fast switching back into the DC bus instead of into the ground.

Although a multi-layer design offers many electrical benefits, there are thermal, weight, and integration trade-offs that are critical for the iPEBB that must be considered. The next section will focus on these trade-offs and present a multi-layer switching-cell prototype.

To better understand the trade-offs for a multi-layer design, thermal and weight analysis using steady-state thermal FEA was completed on the design shown in Figure 14.

Both multi-layer ODBC (ML ODBC) and multi-layer silicon nitride (ML Si₃N₄) substrates were analyzed.

For the ML ODBC, the top copper (Cu) thickness was varied while the other two layers were held at 0.8 mm. The design flexibility offered by the ODBC allows thick metallization close to the die for better heat spreading. Furthermore, analysis in [45] shows that the top Cu layer has the biggest impact on thermal performance due to the poor thermal conductivity of the two polyimide dielectric layers.

For the ML Si₃N₄, the top and bottom layers were constant at 0.8 mm, and the middle Cu was varied. This was determined by the manufacturer's capabilities. As mentioned in Section III, the Si₃N₄ has a limited footprint due to the brittle nature of ceramic substrates. So, a 3 mm Cu baseplate was added to emulate the iPEBB where two H-bridges (12 switching cells) are needed to form one side of the converter. In the simulation, a 70 W loss per die of the bottom switch was applied with a cooling coefficient of 2000 W/m²K. Results show the ML Si₃N₄ has 10 % lower peak temperature than the ML ODBC, but the baseplate causes the ML Si₃N₄ to weigh 60 % more than the ML ODBC, which does not need a baseplate (Figure 39). Therefore, while the ML Si₃N₄ offers superior thermal performance, the ML ODBC offers weight and integration advantages.

Although the limited footprint size of the ML Si₃N₄ remains a roadblock in integrating multiple H-bridges together, the weight concern can be overcome with optimizing the baseplate thickness for weight and mechanical performance. Furthermore, alternative metals and conductors [45] can be explored for the baseplate material. For the ML ODBC, the poor thermal conductivity of the two polyimide layers remains a downside, but an effective rack-level cooling system can compensate with a higher cooling coefficient

[21]. Many of the alternative conductors shown in Chapter 2 can be used to minimize the weight of the baseplate.

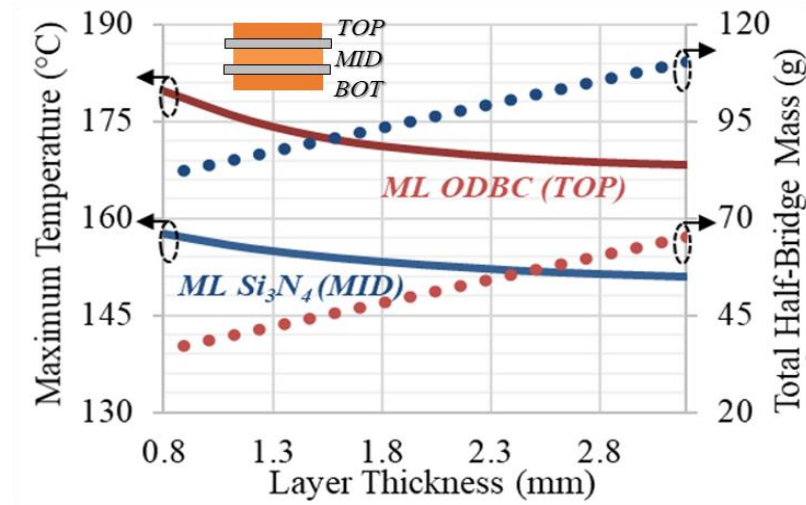


Figure 39 : FEA results for ML ODBC and ML Si₃N₄ with 70 W loss for bottom switch and 2000 W/m²K.

Chapter 6 Si_3N_4 Switching-Cell Design

6.1 *Introduction*

To better understand the electrical and thermal implications of using a multi-layer substrate instead of a traditional 2D layouts, a half-bridge Si_3N_4 switching cell was designed and fabricated. Multi-layer Si_3N_4 AMB substrates were previously demonstrated for low-voltage applications with 1.2 kV devices at 600 V (0.25 mm Si_3N_4) and 850 V (0.15 mm Si_3N_4) DC bus [64] [65]. Both show that the Si_3N_4 design helps reduce the overall power-loop inductance and reduce overall EMI through a CM screen.

It has been shown that a CM screen can reduce the overall induced CM current going to the baseplate by redirecting it to the DC bus. Various modules using the CM screen implemented within power modules have been shown in the literature [66] [67] [68]. Patents, such as one from Infineon, show a method for diverting the current back into the DC by using stacked DBC substrates. The design allows for two parasitic capacitances in series and reduces the overall capacitance. In Infineon's patent, they proposed to connect the middle metal layer to the positive or negative DC bus. The induced current that is flowing through the baseplate capacitance is sent to the module's middle metal layer (hence the DC bus) instead of to the baseplate. This is an attractive and straightforward way to reduce the overall effect of CM on the system implementation. One thing to keep in mind is that the amount of current that will be diverted into the DC bus will depend on the path's high-frequency impedance. Hence, it is critical to reduce the parasitic inductance of this path to fully reap the benefits of a CM screen [66].

The use of wire bonds and other traditional packaging technologies is cost-effective and easy to implement but can also introduce additional parasitics that can minimize the CM screen's effectiveness. The Infineon patent stated that vias were not used in the design due to their high cost, although they help reduce the overall cost. The literature also has examples of using a multi-layer silicon nitride module that has been shown to have a low parasitic design and an effective CM screen [67]. The design uses vias to connect the top and middle layers of the module. The middle layer metal is connected to the negative bus potential. This allows for low overshoot and faster switching speed of the power module. This design also allows improved EMI performance, with 14 dB noise reduction compared to a Cree 1.2 kV reference module.

Various ceramics have been explored for a multilayer design. From the literature, the use of AlN direct-bonded aluminum (DBA) is shown to offer a CM screen and good performance for a high-voltage power module. Instead of having the second DBA be a path for current to flow through, it is instead connected to the mid-point of the DC bus [66]. By doing this, the electric field experienced by the top DBA is reduced. By stacking additional DBAs on top of the bare dies, a full 3D design is utilized in order to minimize the power-loop inductance [69] [70]. The use of an AlN DBA or DBC is highly attractive, especially since its superior thermal performance allows for decent thermal performance despite the additional insulation layer. Although the multi-layer DBA has many advantages, the use of a multi-layer silicon nitride module allows for a high level of mutual inductance cancelation to go along with the CM screen. However, it must be noted that a major trade-off is that the thin silicon nitride dielectric (0.25 mm) also increases the parasitic capacitance across the bottom switch. This increases the output capacitance and can slow

down the module. Regardless, the combination of a low-inductance design and thick metallization make the multi-layer silicon nitride substrate very attractive for this work.

Based on this literature, multi-layer silicon nitride substrates from Rogers Corporation were acquired. They were patterned to allow for gate and Kelvin source pads for each die and room for two parallel 1.7 kV SiC bare-die MOSFETs.

The use of a wirebond-less design is highly attractive for this multi-layer concept in order to minimize parasitics and hence lower the voltage ringing. But the implementation of a wirebond-less design often comes with a more complicated manufacturing process and cost, and offers a lower yield. Hence, wirebonds were once again employed as a cost-effective, high-yield technology.

6.2 *Electrical Analysis*

The electrical layout of the switching cell is shown in Figure 40 (a). A multi-layer design was employed for the switching cell in order to reduce the power-loop inductance and offer a CM screen. Figure 40 (a) shows a schematic that is color coordinated to the switching-cell design. Figure 40 (b) shows the layout of the two 1.7 kV SiC MOSFETs per switch. The design also takes advantage of the superior reverse-conduction characteristics of the SiC MOSFET by eliminating the need for external antiparallel diodes. Figure 40 (c) shows the side view of the switching cell, where vias connect the top S2 Cu to the middle S2 Cu. The parasitic capacitance between the devices and the baseplate is a path for CM current under high dv/dt switching [20]. By using a multi-layer design, the middle metallization layer acts as a CM screen and redirects the CM current into the DC bus instead of into the ground.

An Agilent 4294A impedance analyzer was used to measure the parasitic capacitance, as shown in Figure 40 (c). The trade-offs of the CM screen include a 33% increase in COSS, which impacts the switching speed and efficiency. According to the ANSYS Q3D extractor, the gate-loop inductance is 6 nH for each MOSFET. For the gate loop, a balanced inductance is achieved by having individual gate and Kelvin connections for each die. The Kelvin connection prevents negative feedback between the gate and power source, thereby increasing the switching speed. By having balanced gate loops for each die, the need for additional embedded gate resistors is reduced, enabling faster switching speeds.

The 0.25 mm dielectric offers strong negative mutual inductance cancellation and reduces the power loop to 3.5 nH, according to the ANSYS Q3D. The use of silicon nitride for the insulation also means there can be much thicker metallization of the substrate, which allows for superior heat spreading. Although the use of wirebonds adds additional parasitics, for initial testing it was an effective and industry-standard technology. Furthermore, a 14 nF, C0G, 1.7 kV high-temperature decoupling capacitor is also embedded in the module to reduce the power-loop inductance. C0G was selected because its capacitance value is stable with temperature and voltage.

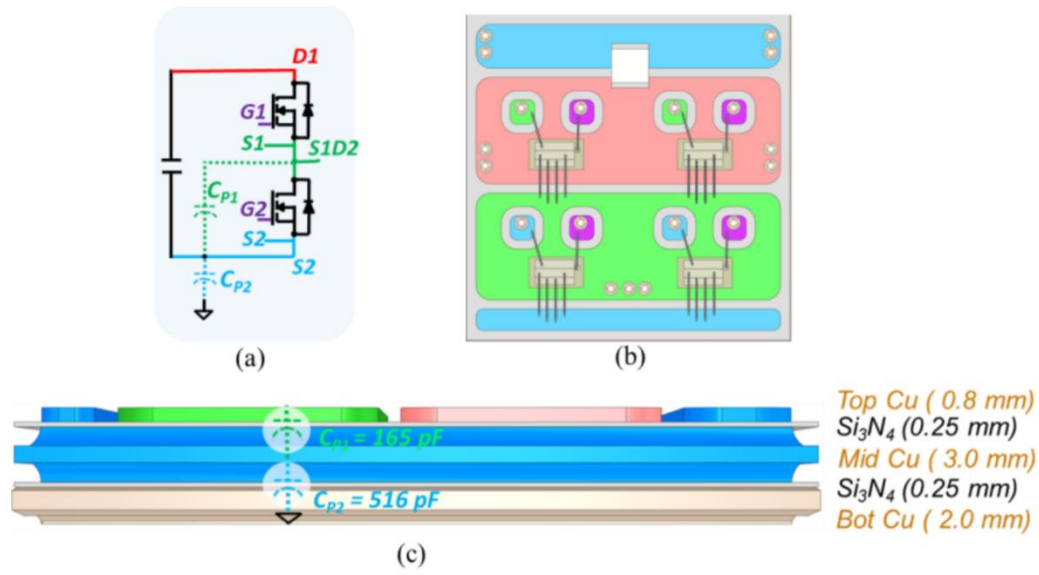


Figure 40 : (a) Half-bridge schematic, (b) multi-layer silicon nitride switching cell, and (c) cross-section of the multi-layer silicon nitride switching cell.

In order to better understand the impact of the CM screen on the switching cell, simulation was completed. The switching cell highlighted in Figure 40 (b) was simulated using the silicon-nitride substrate and ODBC substrate with and without a CM screen. Parasitic capacitance and inductances were pulled using an ANSYS Q3D extractor and input into the LTSpice module of a boost converter.

The schematic of the simulation is shown below in Figure 41. The parasitic capacitance of C_{p1} and C_{p2} is shown and the current going into the LISN is measured. The LISN uses a 50Ω termination and provides a stable input impedance into the system. The LTSpice model makes use of the SPICE model provided by Cree Wolfspeed for their 1.7 kV 45 m Ω bare die. It should be noted that these are simulated results and are only meant to show the difference a CM screen makes in terms of noise. Hardware verification will need to be pursued later.

From the results shown in Figure 42, it is clear that the CM screen reduces the noise at the input by near 20 dB. It should be noted that the ODBC has 10 times lower dielectric thickness, resulting in a larger parasitic capacitance to ground than the silicon nitride module. The single-layer (SL) designs for both modules are similar, and the multi-layer (ML) design with a CM screen is also similar.

However, the ML Si_3N_4 is slightly more effective in reducing the overall noise than the ML ODBC. This could be due to a variety of reasons, including analyzing where the CM current flows through and what the impedance of that CM screen path is for both ML switching cells. A higher parasitic inductance can also cause additional ringing, and as a result, the ODBC could present higher noise than the Si_3N_4 . Overall, the ML designs have lower high-frequency noise due to the CM screen.

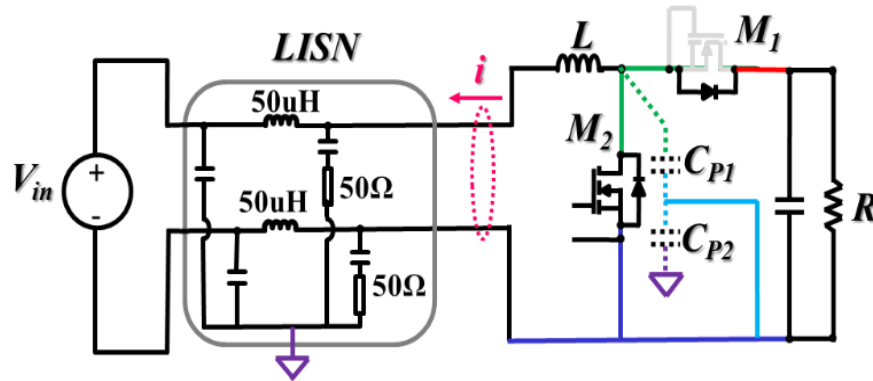


Figure 41: Boost converter setup for EMI testing of switching cell.

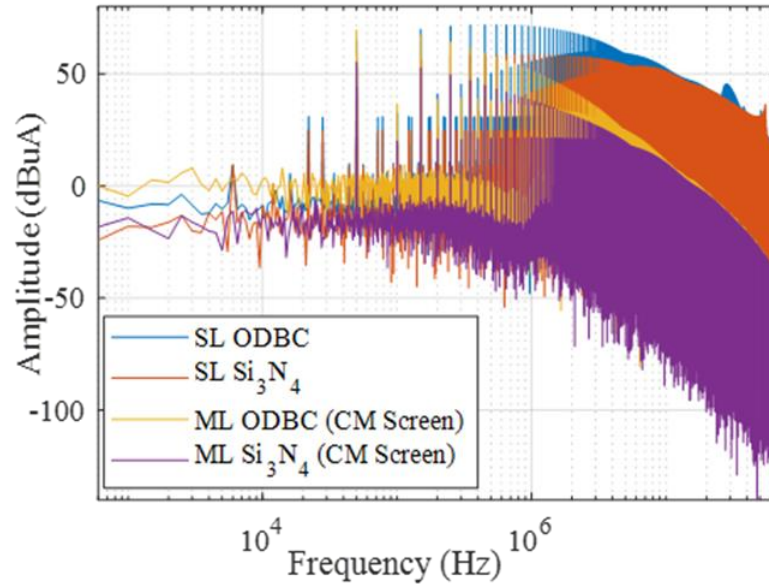


Figure 42: Simulated EMI results for ODBC and silicon nitride using a CM screen.

Another electrical aspect of the multi-layer silicon-nitride substrate that must be looked at is the electric field across the top insulation layer. Although this is a much more critical issue for higher-voltage power modules (3.3 kV – 10 kV), it is still something that must be considered. The voltage potential across the top insulation layer can cause high electric field and PD issues. Below in Figure 43 is the side view of the multi-layer silicon nitride module and a 2D drawing that represents its cross-section. The ANSYS Maxwell was used to see the electric field around the triple-point area where the insulation (silicon nitride), the metal (copper), and the air (or encapsulant) meet.

From the results, it is clear that there are specific stresses at the triple point. Hence, it is critical to make sure that region is properly encapsulated. The unique geometry of the silicon-nitride substrate makes this even more difficult, since the curvature and shape of the middle metallization raises the possibility of air bubbles becoming trapped during encapsulation and degassing. This will be an important factor that will be taken into account during the packaging process for the Si₃N₄ switching cell later on.

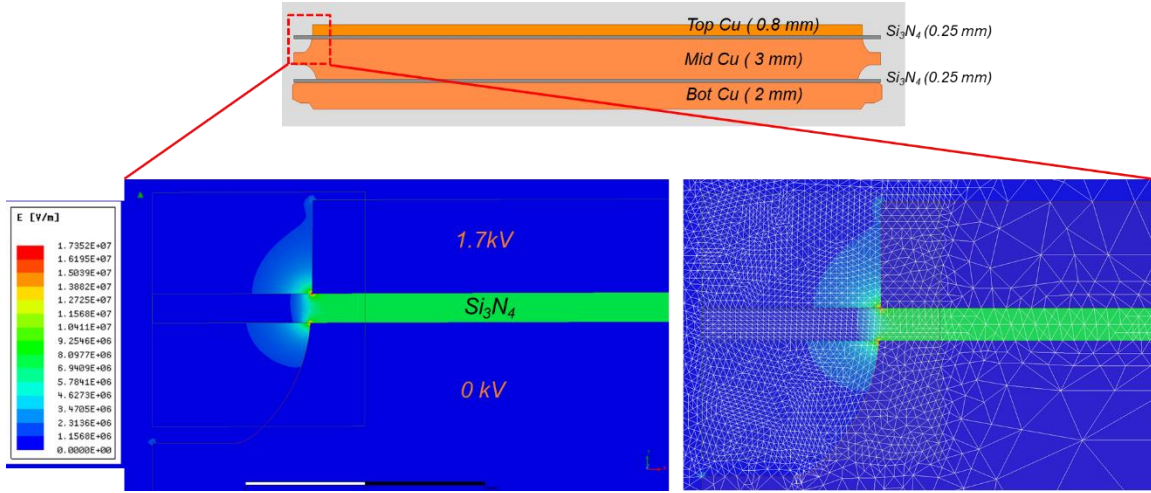


Figure 43 : A 2D drawing of the Si_3N_4 switching cell with ANSYS Maxwell electric field results showing the impact of different voltage potentials on a multilayer design.

6.3 Thermal and Weight Analysis

Another important aspect of the switching cell is the thermal performance. As previously stated, the thicker Cu of Si_3N_4 AMB substrates offers the benefits of better heat spreading and lower thermal resistance. A thickness of 0.25 mm for the Si_3N_4 insulation layers allows for a high mutual inductance cancelation for the power loop while meeting the thermal requirements needed for the iPEBB. Better thermal performance is seen when copper thickness is increased (> 2 mm) which allows for better heat spreading. However, thicker Cu metallization increases the weight.

Analysis on the trade-offs between thermal and weight was done on the multi-layer Si_3N_4 AMB substrate. The top Cu was held constant at 0.8 mm, the bottom was held at 2 mm, and the middle Cu was varied. These values were determined by the Si_3N_4 AMB's metallization capabilities. It has been calculated that each iPEBB switching cell must weigh less than 87 g in order to meet the 16 kg converter weight target. FEA results with 70 W

loss per die and 2000 W/m²K cooling convection are shown in Figure 44. It shows that a 3 mm middle Cu layer is optimal for the thermal and weight trade-off. This simulation was done with a conservative cooling convection, but further thermal analysis of cooling strategies for PEBBs will be studied, including pin-fins and heat pipes, will need to be completed to better understand the trade-offs between thermal performance and weight. Furthermore, the AMB process works with copper metallization and does not provide the flexibility that organic-based substrates do in terms of bonding to alternative conductors. In the next section, further empirical thermal resistance information will be analyzed in order to better understand the impact of multiple insulation layers.

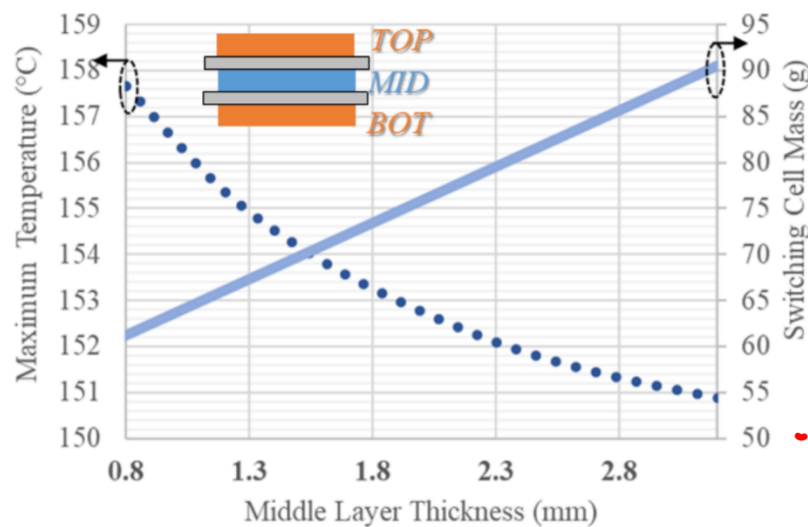


Figure 44 : FEA results with 70 W loss per die and 2000 W/m²K. Temperature and mass vs. Cu thickness of the Si₃N₄ mid-layer.

6.4 Switching-Cell Packaging

For the packaging process, high-yield, industry-standard technology is used to fabricate the switching cell. Multi-layer Si₃N₄ AMB substrates from Rogers Corporation are used. 10 mil Al wire-bonds are used for interconnects due to them being standard, cost

effective, and a high-yield technology widely used in industry. Two different die-attaches are being evaluated for the switching cell. The switching cell is encapsulated in SilGel 612, which is a cost-effective and widely available silicone gel. Its high dielectric strength (20 kV/mm) makes it suitable for this design. A special housing structure was printed using Formlabs high-temperature resin (Figure 45 (a)).

The housing structure allows for clamping around the bottom section of the middle metal layer. This will help secure the housing to the substrate mechanically and allow for encapsulation of the critical region across the top insulation layer. This will eliminate the need for an additional baseplate for the housing to sit on in order to encapsulate the module. The housing structure along with the 3D rendering of the substrate is shown in Figure 45 (b). The teeth of the housing will slide into the slots of the middle metal layer, and the two pieces of the housing structure will make good contact in order to support the switching-cell structure.

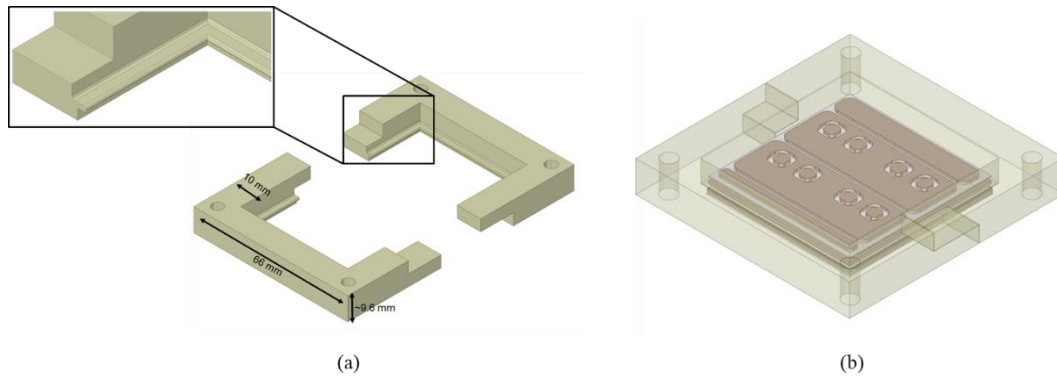


Figure 45 : a) Housing design, and b) 3D rendering of the switching cell with housing.

The unique housing structure will require a two-step encapsulation process to ensure that there are no air pockets in the middle layer. This is especially critical, since any air bubbles trapped in the middle layer could be a source of PD events. The housing was

optimized in order to fully seal the bottom section of the middle layer and the bottom layer from the rest of the module (Figure 46).

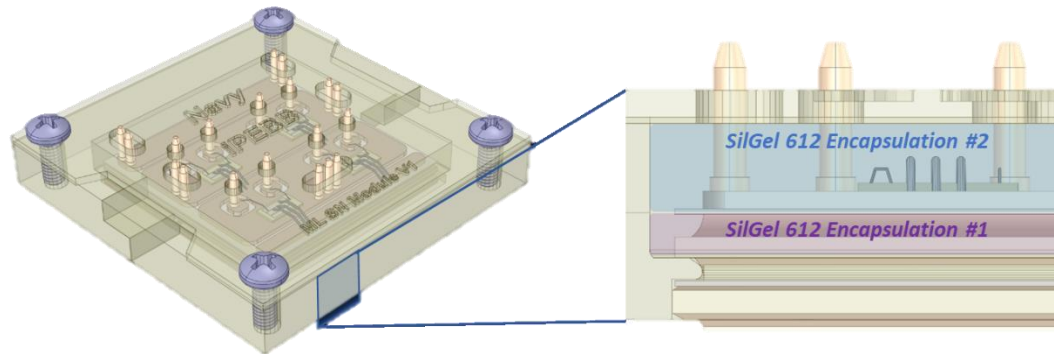


Figure 46 : Cross-section view showing the two-step encapsulation.

The module is built with the same materials shown in Table 4. The Si_3N_4 switching cell is first soldered with four 1.7 kV SiC MOSFET bare die. The substrate is wirebonded with 10 mil Al wire, and pin connectors are soldered on afterwards. The housing is clamped on and epoxy is used to seal the bottom and the two halves of the housing. Various iterations of the housing were developed in order to be able to clamp properly around the middle layer of the substrate. The most effective version has a large lip that secures the housing while offering 2 mm of space for any air bubbles from the middle layer to escape during the encapsulation process.

SilGel 612 encapsulant is carefully poured into the structure to complete the first encapsulation step. The encapsulant covers only the middle layer and will allow for any trapped air bubbles to escape. The encapsulant is then cured at 100 °C for an hour. After curing, the second encapsulation layer is completed and checked for any stray air bubbles. The Si_3N_4 switching cell is then covered with a 3D printed lid in order to protect the encapsulant from dust and environmental factors. The packaging process is shown in Figure 47, and the final Si_3N_4 switching cell is shown in Figure 48. It should be noted that

since the soldering takes place in air, there is oxidation of the substrate. This can be easily overcome by soldering in a vacuum or plating the substrate in silver or gold to minimize the effects of oxidation.

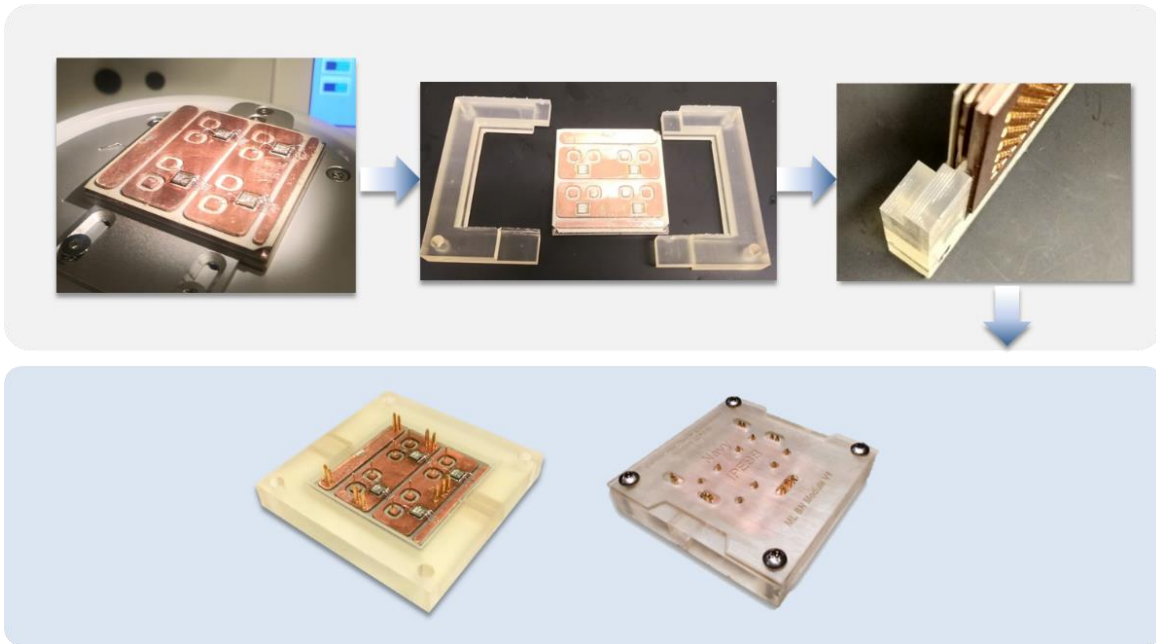


Figure 47 : a) 3D rendering of the switching cell with housing, and b) cross-section view showing the two-step encapsulation.



Figure 48: Si₃N₄ switching-cell module.

Chapter 7 Si_3N_4 Switching-Cell Testing

7.1 *Introduction*

The Si_3N_4 switching cell shown in the previous section will be tested in order to gain further insight into the substrate and the multi-layer design. Initial electrical and thermal testing were completed and are presented in the follow section, which is then followed up with a discussion highlighting key take aways from the testing result.

7.2 *Double-Pulse Test Setup*

In order to complete initial electrical testing on the Si_3N_4 switching cell, a new interface board was designed. This board will help interface the various pins on the module to allow for different probe connections. One of the unique challenges in this design is the distributed pin layout of the power terminals. Having power terminals on either side of the Si_3N_4 switching cell helps with current sharing within the module but can complicate the design of the interface board. Hence, a two-layer interface board was designed in order to balance the parasitics and to allow for easy connection of the current and voltage probes.

A 3D model of the interface board is shown in Figure 49. There are cutouts on the board to allow for easier placement of the Rogowski coil in order to measure the current of the top and bottom switches. The Si_3N_4 switching-cell interface board also allows for connection with the iPEBB gate drivers, similar to that in the ODBC switching cell. A complete image of the testbed with the gate drivers, interface board, and silicon nitride module is shown in Figure 50. Further details about testing results and future modifications are covered in the next section. The different components selected for the test are shown

in Table 7. It is similar to the ODBC test setup, except a Rogowski coil is used to measure the current flowing through the bottom switch.

The gate drivers for this setup are the same as the one used for the ODBC switching cell. This interface board is designed specifically for a double-pulse test and will not be used for a buck testbed setup like the ODBC switching-cell interface board.

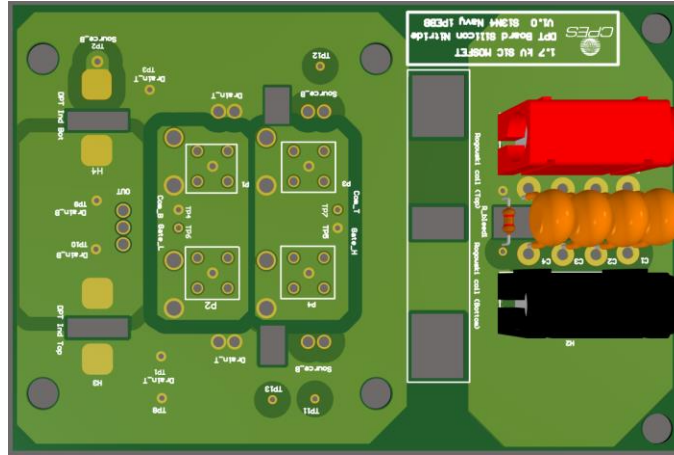


Figure 49: 3D drawing of the Si₃N₄ switching-cell interface board.

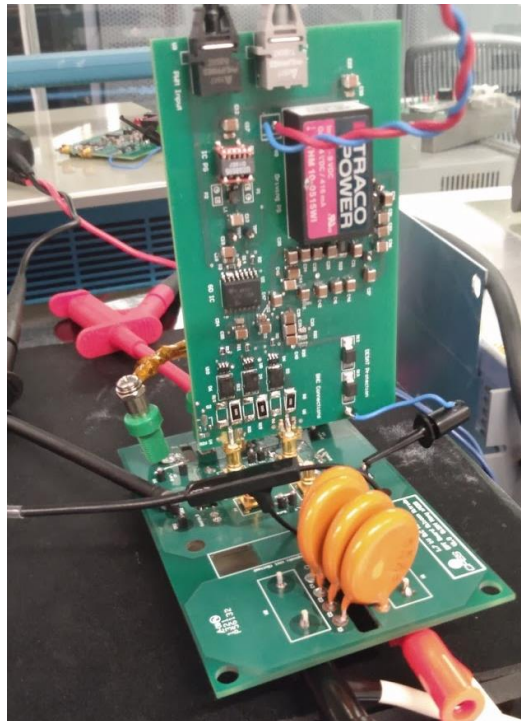


Figure 50: Si₃N₄ switching-cell testbed setup.

Table 7: Components used to measure the current in for the silicon nitride switching cell.

Components	Parameters
Inductor	380 μ H
Gate Turn-off/ Turn-on Voltage	-4 V / +20 V
Gate Turn-on Resistor	10 Ω
Gate Turn-off Resistor	5 Ω
DC Bus Voltage	1 kV
V _{DS} Measurement	Tektronix THDP0200 H
I _{DS} Measurement	SDN-10 Shunt Resistor
Oscilloscope	Tektronix MSO54
Power Supply	ALE Systems 802L

7.3 Double-Pulse Test Result

A double-pulse test was completed on the two parallel bottom switch bare dies. The testing was completed at 1 kV and 53 A. The resulting waveforms are shown in Figure 51. It must be noted that the gate driver had a 15 Ω gate resistance for both the turn-on and turn-off. From the results, it is clear that the performance is reasonable but can be further improved. The dv/dt is 25 V/ns and the current overshoot is 44 A (Figure 52). It must be noted that these initial tests had an issue of the switching-cell pins matching with the connections on the interface board. Hence, additional leads were used in order to make the connection, with the recognition that the additional leads add to the parasitic inductance. Further testing will need to be completed in order to verify the low-inductance design. Additionally, embedding decoupling capacitors in order to minimize the parasitic inductance of the pin leads will also be taken into consideration. A prototype of the design with embedded decoupling capacitors is shown in Figure 53.

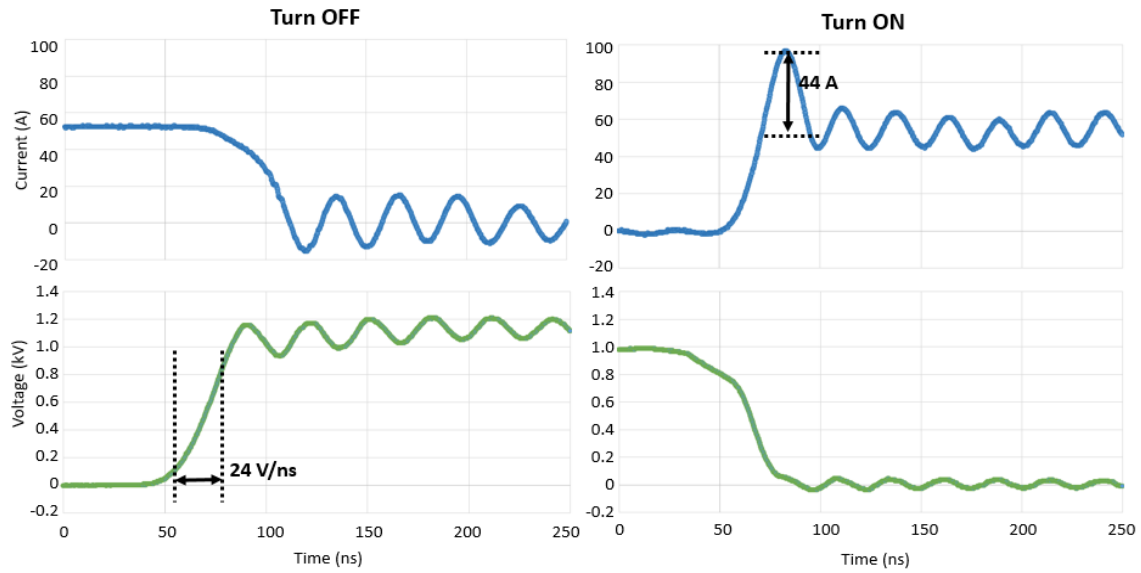


Figure 51: Double-pulse test of Si_3N_4 switching cell at 1 kV, 53 A ($15\ \Omega$ gate resistance).



Figure 52: The additional leads to connect the Si_3N_4 switching cell to the interface board.

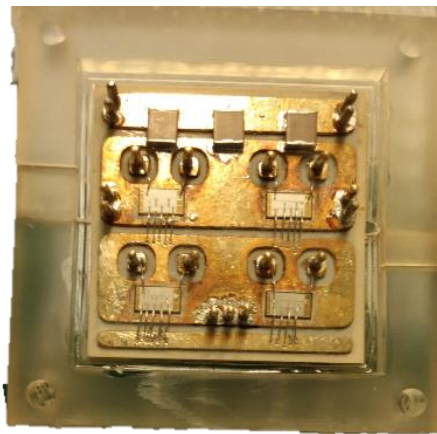


Figure 53: New Si_3N_4 switching cell with embedded decoupling capacitors in order to minimize parasitic inductance.

7.4 Thermal Test Setup

The thermal test setup is similar to the one shown in section five where the ODBC switching cell was tested on an Analysis Tech machine using the same JEDEC standard. Shown below is the test setup with the Si_3N_4 switching cell placed on the cold plate in order to complete the thermal resistance measurement and heating characterization (Figure 54). Clamps were 3D printed to apply downward force on the module to ensure good contact with the cold plate. The leads going from the analyzer to the module are soldered onto the pin connectors. The same thermal interface materials highlighted in Chapter 5 were used for this test as well. Once again, the same 1.7 kV SiC MOSFET bare dies as the ones in the ODBC switching cell were also used. One important caveat that must be mentioned is that the bottom of the Si_3N_4 switching cell does have planar pin-fins that will affect the surface contact with the cold plate and might impact the results. Regardless, these initial results do provide an important insight into the layout as well as the thermal resistance of the switching cell.

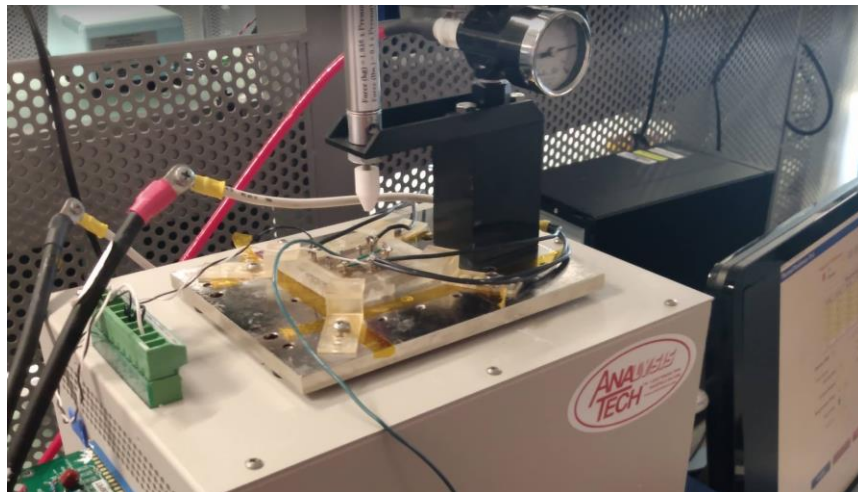


Figure 54: Si_3N_4 switching cell on the Analysis Tech thermal analyzer.

7.5 Thermal Test Results

Initial thermal resistance measurements were completed using the JEDEC JESD 51–14 transient dual-interface measurement method. The body diode forward voltages of the bottom switch were calibrated in the oven up to 130 °C and using a measurement current of 20 mA. The heating pulse was applied through the channel and the junction-to-ambient thermal impedance was measured. This is a similar procedure completed for the ODBC switching cell shown in Chapter 5. The results show that the thermal resistance of the module ~ 0.285 °C/W (Figure 55).

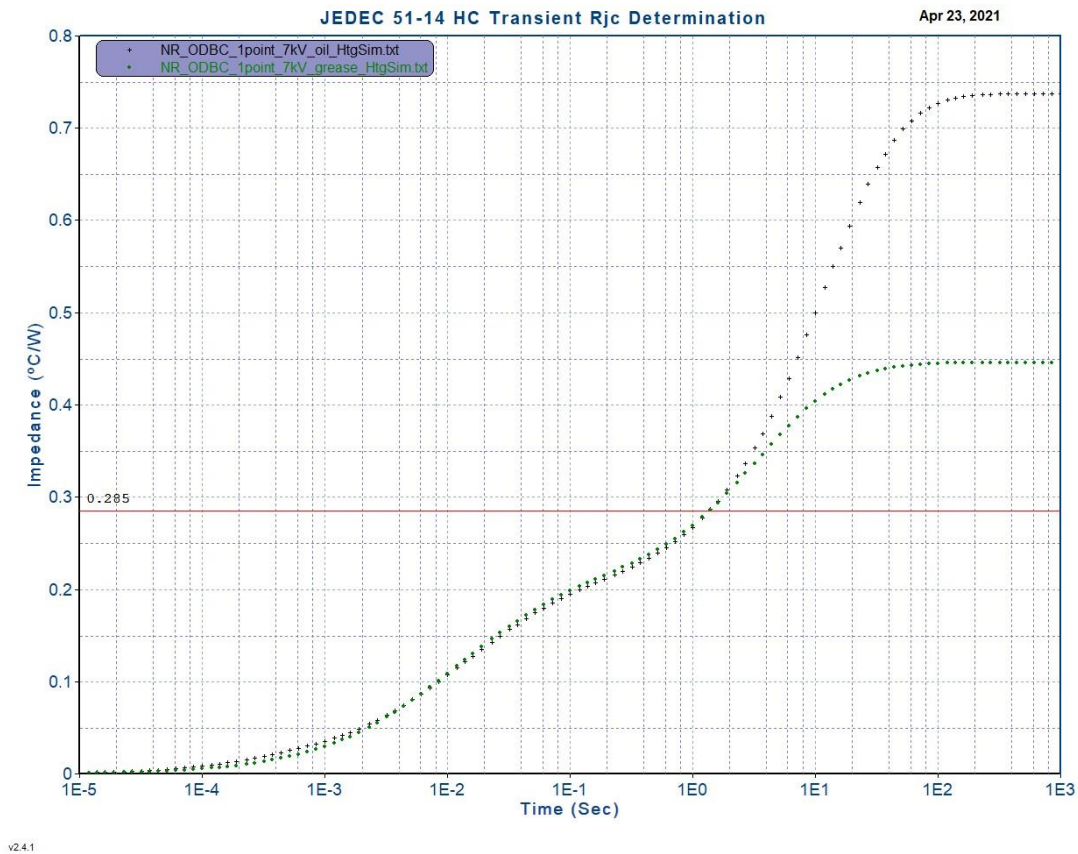


Figure 55: The thermal impedance of the Si₃N₄ switching cell using different TIMs in accordance with the JEDEC JESD 51–14 transient dual-interface measurement method.

This initial thermal resistance data reveals that the Si_3N_4 switching cell has very good thermal performance even with two dielectric layers. This confirms the fact that the thicker metallization in the middle layer helps with the heat spreading and helps compensate for the lower thermal conductivity of the ceramic layer. Further testing also needs to be completed in order to better understand the impact of the pin-fins on the bottom, as well as the impact of oxidation and the solder die-attach layer for the module (Figure 56). The impact of having less surface contact than regular modules is a critical aspect that has the potential to impact the thermal resistance value. This test must also be repeated to take into consideration errors that might be seen as part of the thermal analyzer algorithm to find the break point between the two-interface materials.

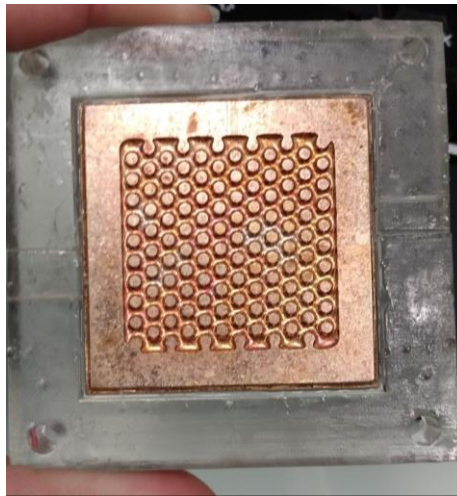


Figure 56: Pin-fins located at the bottom of the silicon nitride switching cell.

7.6 Si_3N_4 Switching-Cell Future Work

Additional EMI testing will need to be completed on the Si_3N_4 switching cell in order to confirm the effectiveness of the CM screen. Although the CM screen for multi-layer designs has been demonstrated previously, studying the low-impedance path to the second metal layer is still an area of research that needs to be explored further.

Additionally, work on exploring pressure-less silver sintering on bare copper will also be pursued. Silver sintering allows for superior thermal performance with minimum voiding in the die-attach layer. The oxidation and the copper grain size can have an impact on the quality of the die-attach and ability of the dies to be attached properly. Work has been done on silver sintering on bare copper for DBCs, but AMB-based substrates have drastically different copper grain size, which will impact the silver sintering profile [71]. This is also true for the ODBC which has a mirror finish copper design, which makes wire bonding, sintering, and soldering more difficult. Shown in Figure 57 is an X-ray of the die-attach of a soldered die for a bare copper substrate with significant voiding seen.

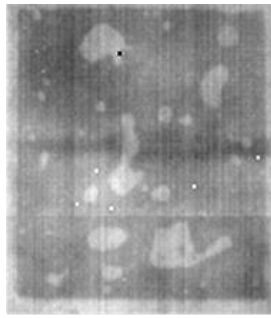


Figure 57: X-ray of the solder die-attach for the bare copper substrate.

Chapter 8 Conclusion and Future Work

8.1 Summary

Wide-bandgap technology has opened a new frontier of medium voltage (MV) converters for power electronics applications. The power electronics building block (PEBB) concept is not new, but the work highlighted in this thesis proposes an integrated version that attempts to apply many of the packaging technologies and methods seen in power modules to the converter level. At the core of the iPEBB is the common substrate concept, which attempts to provide the electrical, thermal, and mechanical foundation for the entire converter. Various substrates and layouts are surveyed and explored in order to identify ones that can serve as the foundation for the iPEBB.

Simulation work was performed to design a common substrate that will serve as the electrical, thermal, and mechanical foundation of the iPEBB. SiC MOSFET bare dies and passive components that form the iPEBB topology will be directly placed on the common substrate to provide electrical interconnects and a unified platform for cooling. To form the common substrate, various ceramic and organic materials were explored, such as organic DBC (ODBC). To inform the design, hardware fabrication and testing of a half-bridge module on a single-layer ODBC substrate is presented. Switching tests were performed at 1 kV, revealing a dv/dt of 27 V/ns and a voltage overshoot of approximately 96 V. The thermal resistance measurements and simulations confirmed that thicker top-side metallization will be needed for improved heat spreading.

This thesis also explores state-of-the-art ceramic-based substrates like the multi-layer silicon nitride. Packaging of this substrate is completed, and initial testing results are

presented. From the initial results, it can be seen that the multi-layer silicon nitride can overcome the poor thermal conductivity of the two insulation layers by employing thick metallization that allows for better heat spreading. Furthermore, analysis was done on the switching cell in order to determine the trade-offs for the weight and thermal performance for the iPEBB. These insights will go into a multi-physics redesign of the iPEBB and will advance high-density medium-voltage converters for future electric systems.

8.2 Conclusion

The ODBC is a promising technology that is compatible with a variety of conductors and comes in thick metallization and large footprints. The thick metallization offers heat spreading and mechanical support for the converter. The ODBC's large footprint offers the ability to eliminate the need for a baseplate thereby reducing the number of thermal interfaces, reducing the weight below 16 kg, and simplifying the manufacturing process. The common substrate uses a multi-layer ODBC design to provide a common-mode (CM) screen and a low-power loop inductance for fast-switching applications. But the implementation of the common substrate will require trade-offs, including increased thermal resistance associated with a multi-layer design.

In this work a common substrate concept was proposed and two switching-cells based on the ODBC and silicon nitride were fabricated and tested. Key takeaways from the ODBC switching cell are that a single-layer design can give reasonable performance that would be expected with a 2D design, but the power loop inductance and current imbalance between the bare dies makes a single-layer design difficult to fully implement in the iPEBB. Furthermore, the high parasitic capacitance to ground is an intrinsic feature of organic-based substrates like the ODBC and is a source of many common-mode EMI-

related issues. There are many ways to reduce the coupling to ground including a common-mode screen with a multi-layer design and the current cancellation method. The leakage current cancellation method was explored for the single-layer ODBC and shows that in a special case where the input and output impedance of an inverter are equal, the switching node capacitance can be tuned to be 0.25 of the total baseplate capacitance. Thermal testing shows that the ODBC suffers from poor thermal conductivity with a thin metallization on top. Simulation work shows that increasing that top copper thickness helps with heat spreading and helps compensate for the poor thermal conductivity of the insulation layer. This is also very critical in a mutli-layer ODBC structure that is the basis of the iPEBB.

To further study a mutli-layer design and the trade-offs that might be seen, a multi-layer silicon nitride-based switching cell was designed and fabricated. The initial results show that the mutli-layer design helps reduce the power loop inductance, but the incorporation of leads does add stray inductance. Furthermore, the use of two insulation layers has the potential of worsening thermal performance. Testing shows that the mutli-layer silicon nitride switching cell can compensate for that lower thermal conductivity with thicker metallization.

The fabrication and testing of these switching cells highlights the electrical and thermal trade-offs that need to be considered when developing the iPEBB common substrate. The ODBC substrate offers design flexibility and a high level of integration between active and passive components that form the iPEBB topology. But the thermal and voltage isolation trade-offs must be further explored in order to find the optimal iPEBB design.

8.3 Future Work

This thesis has covered the initial phase of the iPEBB work, which involves scoping out the project and completing initial design and hardware prototypes to inform further redesigns of the converter. Going forward, the modules presented will be tested in a QSW-ZVS buck setup in order to emulate the soft-switching aspect of the iPEBB. Completing the soft switching of the converter will give a better insight into the module's loss that will inform the converter design. Furthermore, the next phase will involve further redesign of the iPEBB based on the common substrate concept. The simulations highlighted in this work gave some valuable insight for the iPEBB design but were also labor intensive and manually done. A multi-physics approach will be taken in order to automate the redesign and will enable converter-wide optimization going forward. Grid-level work in the internal designs of the iPEBB will also be taken into consideration during the redesign process.

From a hardware perspective, the fabrication of a multi-layer ODBC module with thicker metallization will be critical for further prototypes. Working with manufacturers to develop a multi-layer design will be critical in realizing the common substrate concept. Furthermore, wirebond-less interconnects will also be explored in order to eliminate the need for gate and Kelvin source pads, which will simplify the patterning of the common substrate. Furthermore, the elimination of wirebonds can help minimize stray inductance and allow for faster switching speeds. The employment of a wirebond-less design must be weighed against manufacturability, which is a key goal of the iPEBB design.

Another aspect of the future iPEBB work will involve the integration of the circuitry closer to the power stage. Due to the fast-switching, low-inductance requirements of the iPEBB, bringing critical components like the current booster stage of the gate driver

closer to the bare die level should be explored. Furthermore, the integration of current sensors such as Rogowski coils closer to the die level will allow for better fault protection and current sensing.

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