

Use of SIMO Conversion for Optimizing LED Light Drivers

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Thesis submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical and Computer Engineering

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September 25, 2012
Blacksburg, Virginia

Keywords: LED Lighting, SIMO, MIROF, Multi-String

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Abstract

As a growth industry, tremendous cost pressures are pushing the LED lighting market away from traditional power electronics converters and towards solutions that are more unconventional. Lower quality LED lights use simple low-cost converters, whereas high end product may add complexity in order to achieve a more dramatic energy savings.

SIMO technology represents an opportunity in LED lighting to combine the low cost of single-stage converters with the energy saving capability of a two-stage, multiple string solution. This paper describes the modeling, analysis, design, and testing of a Multiple Independently Regulated Output Flyback (MIROF) converter, used in LED lighting for the purpose of multiple string control. This converter is based upon SIMO technology applied to a PFC Flyback converter.

The result was the development of a novel control method and an operational demonstration unit. A cost comparison of the MIROF and a conventional two-stage driver shows a promising cost reduction benefit for the former, and comparative testing shows favorable performance of the MIROF converter compared to the two-stage approach.

In loving memory:

Lucia S. Gilliom

and

Francis C Saul

Acknowledgements

First and foremost I would like to graciously thank my thesis committee for their patience during this process. In particular Dr Lai was critical in putting this project together, and it could not have been achieved without his support and input to the program.

In addition, to all those friends and family who would not let me forget my work, I thank you as well. My father, all of my siblings, Eric Bushey, John Boyd, and others who continually asked about my progress were a welcome source of motivation throughout the project.

I would like to thank Cree Lighting not only for their financial contributions and support, but also for the hard work of many individuals. In particular I would like to thank Praneet Athalye for his inspiration of the topic, Mike Harris for his leadership, and Doug Keiter without whose coaching I may never have finished.

Finally, and most importantly, I would like to thank my wife Whitney. Thank you for enduring countless hours of my absence, thank you for your support, and thank you for driving over mountains to the defense.

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Abbreviations

BCM – Boundary Conduction Mode

CCM – Continuous Current Mode

DCM – Discontinuous Current Mode

DSP – Digital Signal Processor

FET – Field Effect Transistor

LED – Light Emitting Diode

MIMO – Multiple Input Multiple Output

MIROF – Multiple Independently Regulated Output Flyback

PFC – Power Factor Correction

PWM – Pulse Width Modulation

RGB – Red/Green/Blue

SIDO – Single Inductor Dual Output

SIMO – Single Inductor Multiple Output

SISO – Single Input Single Output

ZCD – Zero Current Detect

Chapter 1. Introduction

1.1 Lighting Industry

The lighting industry is in the midst of a period of heavy change. Incandescent bulbs—a mainstay of the industry for the last century—will be globally affected by legislation to restrict the use of inefficient lighting. In some countries such as members of the European Union legislation has already taken effect, whereas in others such as the United States legislation will take effect in the near future. In all cases the laws will eventually mandate higher efficiency standards than are currently available with incandescents^[1], and are therefore expected to ultimately restrict their use entirely.

The legislation in question was motivated by several factors, the first being cost: high efficiency lighting would stand to save significant energy if it were universally adopted^[2]. Another is the “green” movement^[3] that has been gaining traction across the world—this is the effort to reduce consumption and focus on sustainable sources of energy to slow the impact of climate change and global warming. The final factor is the sudden availability of new and innovative technologies in the field of lighting.

Compact fluorescents, represent one alternative to the use of incandescent lighting. Compact fluorescents (or CFLs) are more efficient and can typically draw less than one quarter^[4] of the power of a comparable incandescent. Their expected lifetime is also greater, and CFLs can typically last 8 to 15 times longer than an incandescent^[5]. The cost of CFLs is greater than incandescent bulbs and therefore makes them less attractive to some, however, it can easily be demonstrated that CFLs will pay for themselves in reduced cost of ownership in as little as 1 month^[6].

On the other hand compact fluorescents have some problems that have served as a barrier to their universal adoption into the lighting market. Color quality can be difficult to achieve with CFLs and many consumers prefer the warm light of an incandescent to the sharp,

uncomfortable light of a CFL. CFLs are also manufactured with hazardous chemicals such as Mercury^[7], and have drawn intense scrutiny over whether they are safe to use within the household. While CFLs provide several benefits over incandescents, it is not clear they are the best choice as a wholesale replacement.

A second alternative to incandescents is solid state or LED lighting. LED lighting is achieved electronically, and employs Light Emitting Diodes as a light source. LEDs are manufactured in standard processes that are typical for silicon parts, and do not contain dangerous chemicals such as Mercury^[8]. LED lights can also be used with technologies such as CREE True White® to deliver soft, pleasant light that matches incandescent very closely.

The goal of any company offering an alternative to incandescent lights is to offer a comparable product at a comparable price. LED lights come in all forms and the products that are most cost competitive tend to have the poor light quality that is typical of fluorescents. Generally speaking as the light quality increases so too does the price, and products whose light quality is visually imperceptible from incandescent bulbs are very expensive compared to both incandescents and CFLs.

High quality LED lighting must become more cost effective if it is expected to capture any major share of the lighting market. LED lights provide the same cost of ownership benefits that compact fluorescents do, and can even pay for themselves as replacements for CFLs. However, the extended benefits of LED lights come at an even greater up-front cost. The lowest cost LED lighting products which are currently available are inefficient and aesthetically repellant, whereas high quality products despite their ultimate cost benefits are seen as simply too expensive.

The purpose of this paper is to explore one alternative to standard LED driver technology with the goal of identifying it as an opportunity to reduce system cost in LED lighting.

1.2 LED Lighting Market Trends

LED lighting is a young, burgeoning industry. The volume of sales in the LED lighting market has increased dramatically over the last decade and will continue to do so into the next^{[9][10]}.

In addition to a growing perception that LED lights are safe, quality products the growth in this market is enabled by a continuous focus on reducing product cost. There is tremendous pressure to pull cost out of these products to meet the rising demand of the market.

1.3 Cost Reduction Strategies

All LED lights require electrical systems to convert high AC voltage to low voltage DC current. These electrical systems come in a variety of forms, but are typically a major contributor to cost in any LED lighting system. Simple LED lights may consist of a single AC/DC converter as shown in Figure 1. More complex systems may include a secondary power stage as shown in Figure 2. The secondary stage adds cost, but has the benefit of being able to control multiple string currents. This is important because a multiple color light can convert power to light more efficiently and therefore reduce cost of ownership to the consumer.

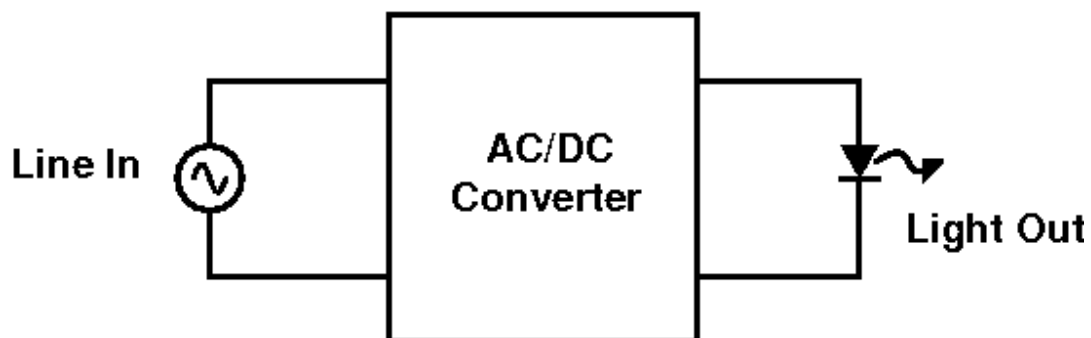


Figure 1 – Single Stage LED Light Electrical System

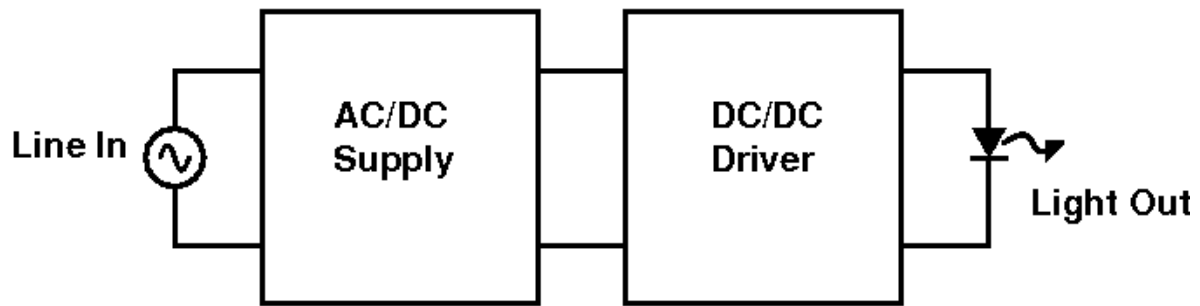


Figure 2 – Dual Stage LED Light Electrical System

Color mixing is one solution to the problem of creating white light from LEDs^[11], and when this solution is used a secondary power stage becomes critical. Color mixing is a type of optical science which aims to achieve high quality optical output by combining several lower quality point sources. For instance, a purple colored light is the result of combining blue and red LEDs. A white light may be produced by similarly combining various other colors of LEDs.

Color mixing requires two power stages because each of the colors will have a unique contribution level. For instance producing a white light may require supplying more blue light than red. The blue light source in this case must be driven to produce more output than the red source. This can be achieved in two ways with LED sources: (1) use more blue LEDs than red and drive both at the same current, or (2) drive an equal number of blue LEDs at a higher current than the reds. The former strategy can be used with various LED colors to deliver an arbitrary color point, however, manufacturing tolerance of the LEDs will have a strong effect on the output (in terms of color and luminosity), making it difficult to achieve a specification.

It is advantageous therefore to drive each LED color at its own unique current^{[12][13]}. This allows a fine degree of control over the color point, and can nullify the effect of LED tolerancing if the current levels are selected during the assembly process. Multiple-string control can also allow for the setting of an arbitrary color point by the consumer. This solution requires a secondary power stage which acts as a circuit to regulate current for each LED color. An RGB system, for instance, would require 3 separate current regulators, as shown in Figure 3.

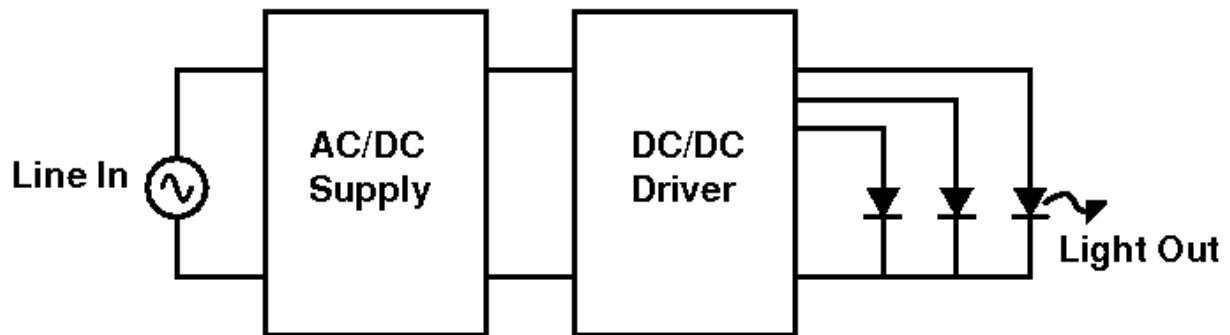


Figure 3 – Three String Secondary Controller

The above system offers an excellent solution for color mixing, although the total cost is much greater than that of a single stage AC/DC. If there were an alternative available that offered multiple string outputs in a single stage design, then the cost and performance benefits would represent the best of both worlds. This is technically possible using a multiple output flyback, however, this topology does not allow *independent* regulation of the multiple outputs. One output may be regulated precisely, and the others are dependent on the first output and the turns ratio of the transformer, which is constant. A true solution needs to offer precise and independent regulation of each output without adding a second stage.

A Single Inductor Dual Output (SIDO) or Single Inductor Multiple Output (SIMO) switching strategy is a compelling answer to the question of how to achieve the desired combination of cost and performance^{[14]-[27]}. SIMO is a method for time sharing the energy in a single inductor to spread it across multiple outputs. An example of a SIMO buck is shown in Figure 4.

SIMO converters offer several advantages over multiple independently regulated converters. The most obvious benefit is clearly the reduction in part count (and therefore cost) from the standard converters to the SIMO. Changing from a configuration shown in Figure 5a below to that shown in Figure 5b can reduce system part count significantly in some cases. This is discussed further in Section 5.1.

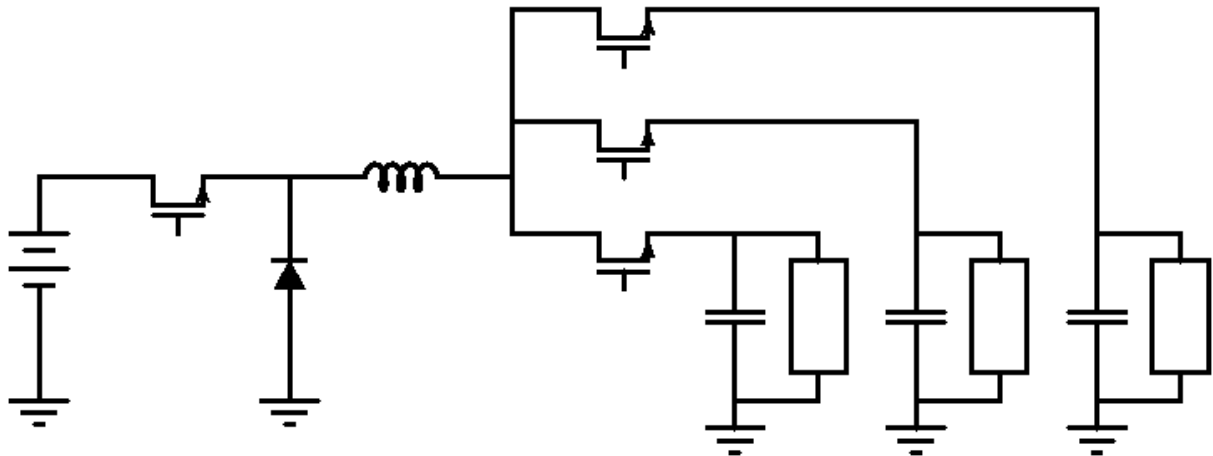


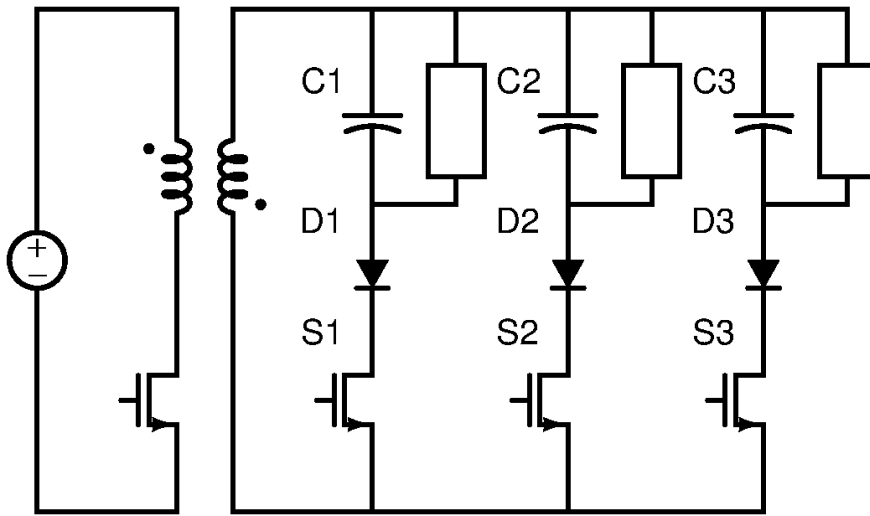
Figure 4 – SIMO Buck

In the case of an AC/DC flyback there is no inductor, and therefore a SIMO configuration of a flyback might be called a Single *Transformer* Multiple Output converter. This is vague because a *standard* flyback is capable of multiple outputs with a single transformer, so the term MIROF (Multiple Independently Regulated Output Flyback) converter will be used here. Hereafter, the term MIROF will be used to describe a SIMO configured flyback whereas the term SIMO by itself will refer generally to any configuration with a multiplexed inductive current source rather than a specific topology. A MIROF converter is shown in Figure 5a

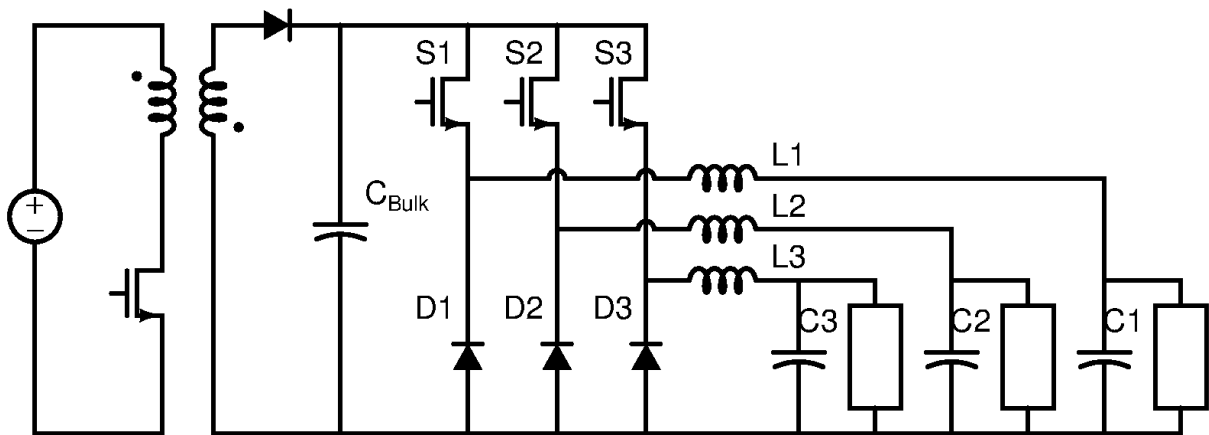
This paper will focus on assessing the cost and performance capabilities of a MIROF converter in comparison with a conventional two-stage approach such as the one shown in Figure 5b. The objective will be to demonstrate via modeling, analysis, design, and testing that a PFC enabled MIROF is possible, and then to compare its performance to a standard two-stage converter.

1.4 MIROF Conversion

The most obvious benefit of using a MIROF over a conventional 2-stage is the absence of the buck inductors labeled L1-L3 in Figure 5b. These inductors can be a costly portion of the circuit, and therefore a solution which removes them could potentially offer a substantial savings.



(a) MIROF Converter



(b) 2-stage Converter

Figure 5 – MIROF Converter vs Conventional 2-Stage Conversion

There are other opportunities for cost reduction as well. The controller for a MIROF converter must be consolidated into one digital device, potentially reducing the cost. The caveat here, however, is that a controller for a MIROF circuit must be much more complex than a standard flyback or buck controller, and necessarily digital. This added complexity will offset the cost benefit of consolidation, but it also requires more work during the development of the

converter. The controller required to stabilize this circuit requires clever use of system theory and is discussed in Section 3.

Beyond use of control theory it is also necessary to manipulate the instrumentation of the converter in order to approximate a linear system. This will not necessarily have an impact on system cost, but it will also require added attention during the development of the converter. All these considerations and the hardware implementation of the MIROF controller are discussed in Section 4.

The MIROF converter is also more complex to implement than a standard 2 stage supply and requires the use of a microcontroller or DSP and associated embedded software. The design and implementation of these digital systems is a major part of the overall design, and is discussed in Section 5.

These cost benefits, unfortunately, do not come without a sacrifice. Performance of the MIROF is not as good as the 2-stage approach. Being a PFC-type controller, the output regulation of a MIROF is slow with a bandwidth of less than 60Hz. The string currents in this circuit are direct outputs of the PFC circuit and are not buffered by a second power stage. Therefore they are slow to regulate and susceptible to input disturbances. Whether or not this is acceptable is a matter of application, and LED lighting may be a good example of an application where these tradeoffs are acceptable. Performance metrics are discussed in Section 6

Chapter 2. System Modeling and Control

2.1 SIMO sequencing

Basic operation of any SIMO style power electronics converter depends on time multiplexing of current from an inductive current source. There is more than one way to accomplish this^{[14][15]}, and modeling of these systems is directly and heavily affected by what strategy the designer uses to split current among SIMO channels.

For instance, a SIMO converter may pass current to each channel once during each switching cycle or it may pass current through only one channel during each switching cycle. In the latter example, the controller would rotate through all channels once every n switching cycles, where n is the number of channels. The difference between these strategies is illustrated in Figure 6.

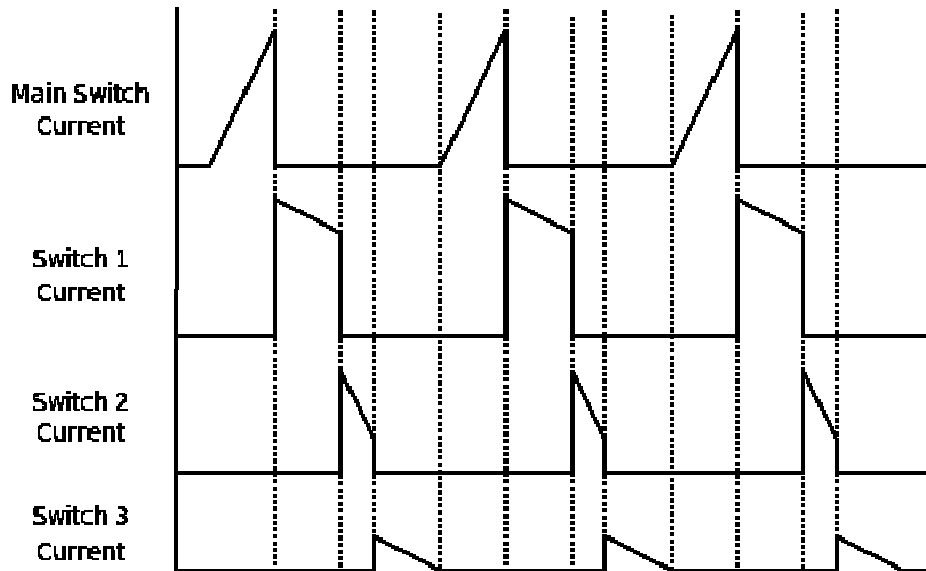
The difference between these two control strategies affects not only the linear modeling of the system but the requirements on the controller. Note that in Figure 6b, the total RMS values of 1, 2, and 3 are different for each channel, demonstrated by the following equation:

$$A_1 \neq A_2 \neq A_3 \quad (1)$$

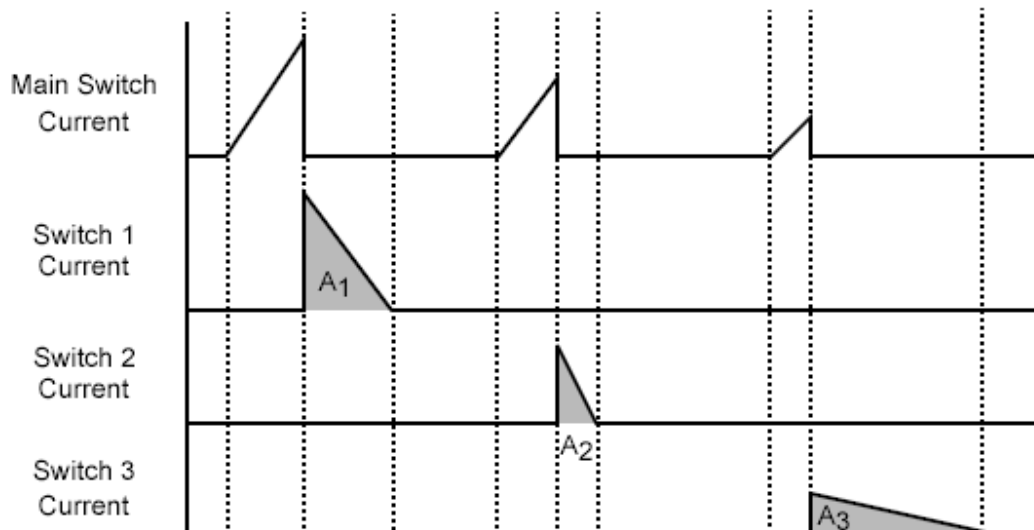
For consolidated sequencing this imbalance can be achieved simply by carefully controlling the time that each channel conducts current. All three channels conduct during the switching cycle, therefore each switching cycle is the same since the period of repetition is one switching cycle.

For interleaved sequencing in this example, the period of repetition is three switching cycles. If the converter is run in discontinuous current mode (DCM) as shown in the figure, then the only way to independently control the conduction time of each channel is via the conduction time of the main switch. This means that the main switch conduction time will potentially vary from one switching cycle to the next. This would have a significant effect on both the controller

requirements and the converter operation. Not only would a powerful DSP be needed to generate a pulse train with constantly cycling pulse widths, but THD and EMI requirements may be more difficult to meet.



(a) Consolidated sequencing



(b) Interleaved sequencing

Figure 6 – Consolidated vs Interleaved Sequencing for SIMO

2.2 System characteristics

Keeping in mind that the requirements imposed upon the converter and the system will impact the scope of this project, the following requirements were selected at the outset:

- The converter must demonstrate Power Factors of 0.9 or above when powered by a 120V AC source. This is required because it is a requirement in most lighting applications.
- The converter will be MIROF style. This is chosen because it is a relatively simple converter, it is capable of Power Factor Correction (PFC), and the load and source can be isolated in future implementations. Isolation is an important option in lighting applications.
- The converter will run in DCM. This offers the advantage of a simple implementation of PFC (fixed on time control).
- The converter will switch using consolidated sequencing. This is chosen for 2 reasons: (1) it offers a simpler switch timing implementation than alternated sequencing since the main switch timing stays relatively constant from one cycle to the next, and (2) it offers a more interesting control systems topic for a research paper.

There is one last decision that must be made regarding sequencing and switch timing which is a direct result of the PFC requirement. By nature, the load current of a PFC circuit will vary in proportion to the line voltage. At the peak of the AC input line the load will see twice the average source current coming from the PFC whereas at zero crossing no current will flow from the PFC. In a PFC Flyback circuit the output current appears as is shown in Figure 7

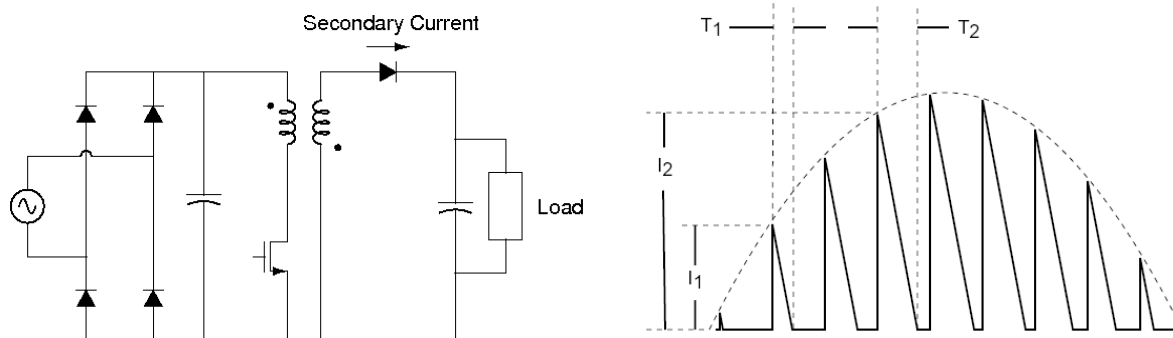


Figure 7 – PFC Flyback Output Current

Note from the waveform diagram that both conduction time and peak current change throughout the line cycle. This introduces a subtle complication for a SIMO converter designed to operate with integrated PFC. Two alternatives for managing the secondary conduction time are available: fixed time and fixed ratio.

2.3 Fixed Time and Fixed Ratio Sequencing

Fixed time sequencing is typical of SIMO implementations without PFC^{[14]-[27]}. In fixed time sequencing each of the switches is held on for a known fixed period of time after the main switch is turned off. This is straightforward in non-PFC implementations, however, the varying nature of the secondary conduction current in a PFC circuit causes the fixed conduction time to have a peculiar effect. As the line voltage transitions from its peak to the zero crossing the total conduction time for all channels combined will fall from its peak value to zero. If the controller attempts to hold each channel in conduction for a fixed period of time then each channel will drop out one at a time as the total conduction time reduces to zero. This is shown in Figure 8.

In this example all periods marked with “T1” are equal to each other in time. The same is true for periods marked “T2”. The time period designated “A” represents the moment where the line voltage is at its peak. At this moment all channels are conducting for their full time. During the period marked “B” channels 1 and 2 conduct for their full periods, however, the inductor (or transformer in the case of a MIROF converter) is depleted of energy before the full conduction

time has passed for channel 3. During the time period marked “C” channel 1 is still conducting for its full time, however, the magnetic component is depleted during the conduction time for channel 2. Not only does this mean that channel 2 will not conduct for its full time, but channel 3 is excluded completely. At this point channel 3 will not receive any more current until the next line cycle. During period “D” only channel 1 conducts although the magnetic component is depleted before the full conduction time for that channel has passed.

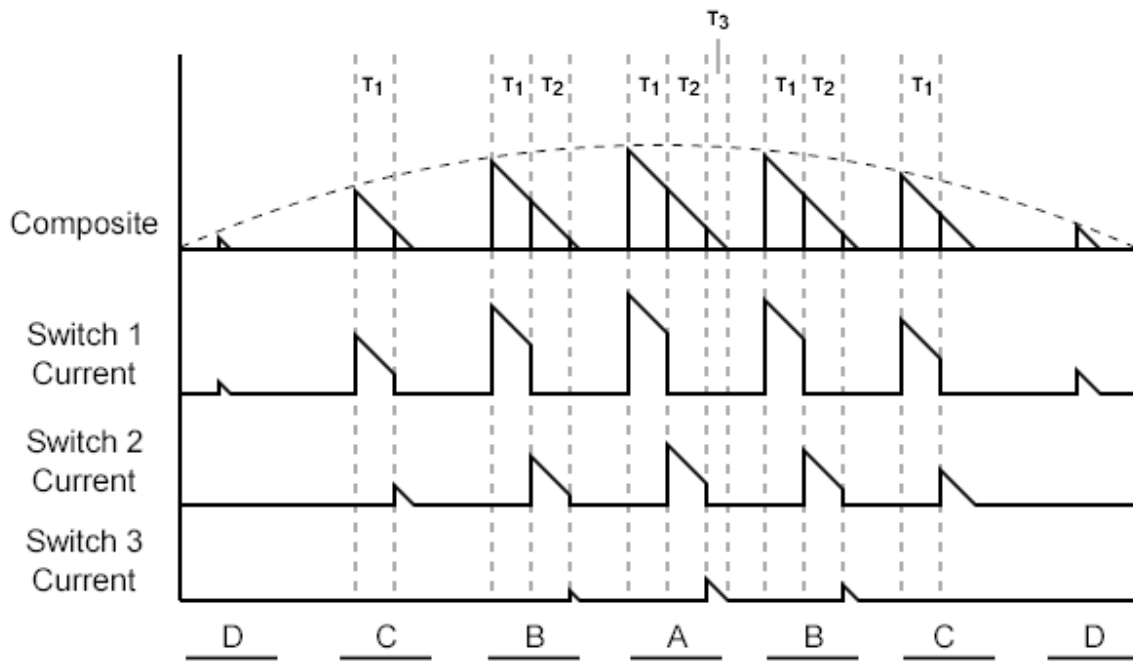


Figure 8 – Fixed Time Sequencing of a PFC SIMO Converter

Exclusion of channels during the line cycle is not ideal, although it can be accommodated for in the design by using heavy bulk capacitance to keep the load powered during periods of exclusion. This is not necessarily problematic since PFC circuits tend to require such heavy capacitance by their nature. Periodic exclusion will just make the requirement slightly more stringent. It is also interesting to note that in this configuration channels which spend the most time excluded (channel 3 in the above example), will demand a much longer conduction time per unit of load current. This is necessary to counteract the long exclusions.

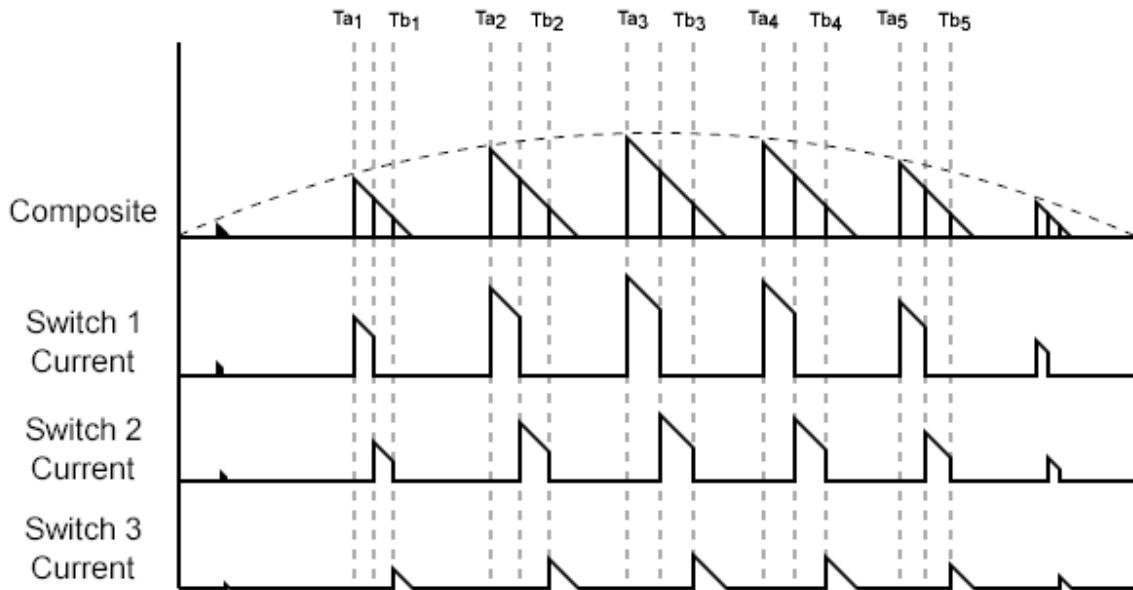


Figure 9 – Fixed Ratio Sequence Timing

Ratio of channel conduction times remains constant and can be illustrated by the equation

$$\frac{T_{a_1}}{T_{b_1}} = \frac{T_{a_2}}{T_{b_2}} = \frac{T_{a_n}}{T_{b_n}}$$

where n is any integer

The alternative to fixed time sequencing is fixed ratio sequencing. Fixed ratio sequencing differs from fixed time sequencing in that all channels conduct over the entire line cycle. This is accomplished by reducing the channel conduction time as the line voltage transits from peak to zero crossing. The maximum conduction time for each channel occurs at the peak of the line input. As the channel conduction times decrease with the total conduction time they decrease in such a way that the ratio of one channel conduction time to another remains constant. This is shown in Figure 9

Fixed ratio sequencing has one major drawback: the fact that the channel conduction time changes for every switching cycle, and therefore must be updated continuously. Comparatively fixed time sequencing allows the channel conduction time to be the same from one switching

cycle to the next and only requires that the controller update the switching period several times per line cycle.

From the perspective of system requirements it is much simpler to keep the channel conduction period the same. For this reason fixed time sequencing was initially chosen as the switch timing strategy for the MIROF converter.

2.4 System modeling with fixed time sequencing

The system may be modeled by modeling each of the channels individually. Taking channel 1 first, we can simplify the schematic to the circuit in Figure 10a.

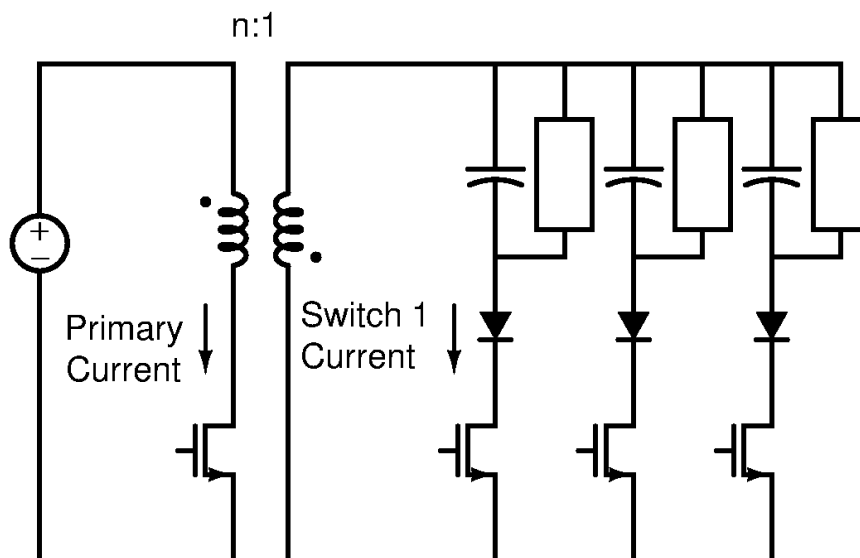
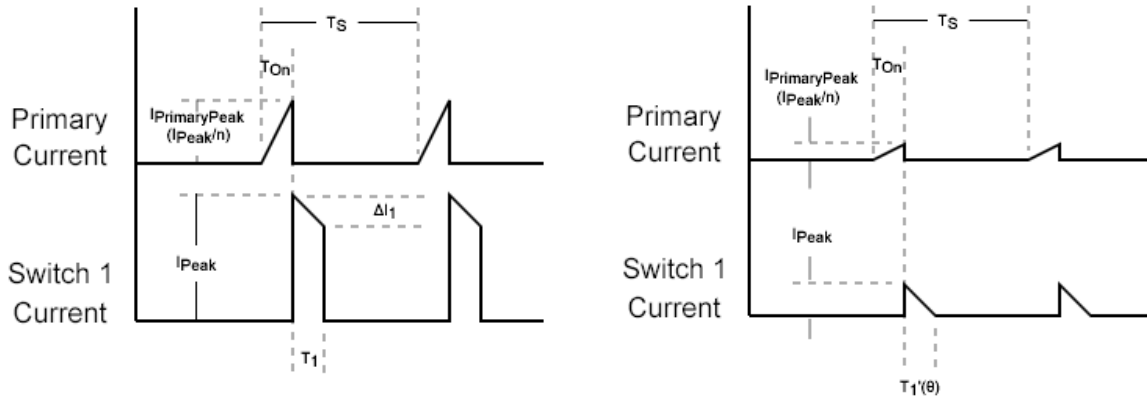


Figure 10 – Simplified Circuit Configuration Modeling Only Channel 1

In this circuit switch Q_0 is closed for time T_{On} , and beginning immediately after it is opened switch Q_1 is closed for time T_1 . This timing and the current waveforms associated with them are shown in Figure 11.

In this single channel configuration the peak current that the primary FET sees over the switching cycle is $I_{PrimaryPeak}$, and is defined by the following equation:

$$I_{PrimaryPeak}(\theta) = \frac{V_{In}(\theta) \cdot T_{On}}{L_p} \quad (2)$$



- a) Channel 1 conducts for time T_1 and stops before energy is depleted from the transformer
- b) Transformer is depleted of energy before time T_1 has passed. No energy is left for subsequent channels

Figure 11 – Waveforms for Channel 1

where L_P is the inductance of the transformer primary winding.

$I_{PrimaryPeak}$ is expressed above as a function of input phase angle θ since it is dependent on the input voltage V_{In} which is assumed to be sinusoidal. Specifically:

$$V_{In}(\theta) = V_{InPeak} \cdot \sin(\theta) \quad (3)$$

After the primary conduction cycle, the magnetizing current is forced through the secondary tap of the transformer, and the peak current here is greater than $I_{PrimaryPeak}$ by a factor of n , the turns ratio:

$$I_{Peak}(\theta) = I_{PrimaryPeak}(\theta) \cdot n = \frac{V_{In}(\theta) \cdot T_{On} \cdot n}{L_P} \quad (4)$$

The quantity ΔI_1 , shown in Figure 11a, represents the change in transformer current over time T_1 . It is defined by the following equation:

$$\Delta I_1 = \frac{V_1 \cdot T_1 \cdot n^2}{L_P} \quad (5)$$

where V_1 is the voltage across the capacitor in series with Switch 1 (Q_1).

It is necessary to model the average current through Q_1 since the target application for this converter is an LED string current controller (The string current is equal to the current through Q_1 when both are averaged over the line cycle). The average Q_1 switch current can be modeled in two ways, depending on whether there is energy left in the transformer at the end of time T_1 . A waveform with remaining energy is shown in Figure 11a, whereas a waveform with the transformer energy depleted completely before time T_1 has passed is shown in Figure 11b.

In a fixed time sequence configuration, both of these conditions will exist at different parts of the line cycle (see Figure 8), so it is necessary to model both. The Q_1 average current shown in Figure 11a can be defined by the Equation 6:

$$I_{Avg1}(\theta) = \frac{I_{Peak}(\theta) \cdot T_1 - \frac{1}{2} \cdot \Delta I_1 \cdot T_1}{T_S} \quad \text{for } I_{Peak}(\theta) \geq \Delta I_1 \quad (6)$$

Substituting Equation 4 and 5:

$$I_{Avg1}(\theta) = \frac{V_{InPeak} \cdot n \cdot T_{On} \cdot T_1}{L_P \cdot T_S} \cdot \sin(\theta) - \frac{n^2 \cdot V_1 \cdot T_1^2}{2 \cdot L_P \cdot T_S} \quad \text{for } I_{Peak}(\theta) \geq \Delta I_1 \quad (7)$$

The average current shown in Figure 11b can be defined by Equation 8:

$$I_{Avg1}(\theta) = \frac{\frac{1}{2} \cdot I_{Peak}(\theta) \cdot T_1'(\theta)}{T_S} \quad \text{for } I_{Peak}(\theta) < \Delta I_1 \quad (8)$$

Where:

$$V_1 = \frac{L_P}{n^2} \cdot \frac{I_{Peak}(\theta)}{T_1'(\theta)} \Rightarrow T_1'(\theta) = \frac{L_P \cdot I_{Peak}(\theta)}{n^2 \cdot V_1} \quad (9)$$

Combining Equations 4, 8, and 9 yields:

$$I_{Avg1}(\theta) = \frac{V_{InPeak}^2 \cdot T_{On}^2}{2 \cdot L_P \cdot V_1 \cdot T_S} \cdot \sin^2(\theta) \text{ for } I_{Peak}(\theta) < \Delta I_1 \quad (10)$$

θ_1 may be defined as the input line phase angle for which the following equation is true:

$$I_{Peak}(\theta_1) = \Delta I_1 \quad (11)$$

Combining Equations 4, 8, and 11, and solving for θ_1 yields:

$$\theta_1 = \arcsin\left(\frac{V_1 \cdot T_1 \cdot n}{V_{InPeak} \cdot T_{On}}\right) \quad (12)$$

θ_1 represents the input phase angle at which exists the boundary between Equations 7, and

10. Or, to put it another way, Equation 7 is true for $\pi/2 \geq \theta \geq \theta_1$, and Equation 10 is true for $\theta_1 \geq \theta \geq 0$.

As stated previously, the current through switch Q_1 is equal to the current through the load, but only when the two are averaged over the line period. This is because capacitor C_1 is intended to hold the V_1 voltage up through the line cycle, during which time the instantaneous power to the load from the converter varies between 0 and twice the nominal power.

Since averaging the converter output current over the input line cycle is the only way to determine the average current to the load then the following equation must be evaluated:

$$I_{AvgCycle1} = \frac{1}{\pi/2} \cdot \int_0^{\pi/2} I_{Avg1}(\theta) \cdot d\theta \quad (13)$$

Note: the assumption that is made here is that the average output current for the quadrant $0 \leq \theta \leq \pi/2$ is equal to the average output current for all other quadrants and is also equal to the average of the full line cycle, $0 \leq \theta \leq 2\pi$.

The integration is piecewise since the evaluation of I_{Avg1} is dependent on θ . Combining Equations 7, 10, and 13 yields the following:

$$I_{AvgCycle1} = \frac{2}{\pi} \cdot \left[\int_0^{\theta_1} \frac{V_{InPeak}^2 \cdot T_{On}^2}{2 \cdot L_P \cdot V_1 \cdot T_S} \cdot \sin^2(\theta) \cdot d\theta + \int_{\theta_1}^{\pi/2} \frac{V_{InPeak} \cdot T_{On} \cdot T_1 \cdot n}{L_P \cdot T_S} \cdot \sin(\theta) - \frac{V_1 \cdot T_1^2 \cdot n^2}{2 \cdot L_P \cdot T_S} \cdot d\theta \right] \quad (14)$$

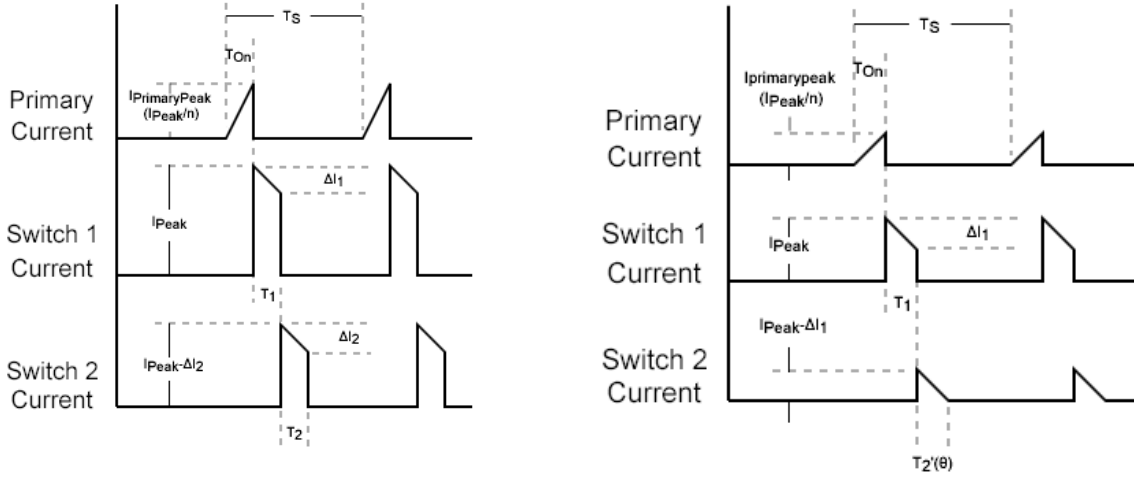
Evaluating the integral terms, and substituting Equation 12 for all instances of θ_1 , Equation 14 can be simplified to the following:

$$I_{AvgCycle1} = \frac{2}{\pi} \cdot \left\{ \frac{V_{InPeak}^2 \cdot T_{On}^2}{4 \cdot L_P \cdot V_1 \cdot T_S} \cdot \left[\arcsin \left(\frac{V_1 \cdot T_1 \cdot n}{V_{InPeak} \cdot T_{On}} \right) - \frac{V_1 \cdot T_1 \cdot n}{V_{InPeak} \cdot T_{On}} \cdot \sqrt{1 - \frac{V_1^2 \cdot T_1^2 \cdot n^2}{V_{InPeak}^2 \cdot T_{On}^2}} \right] + \frac{V_{InPeak} \cdot T_{On} \cdot T_1 \cdot n}{L_P \cdot T_S} \cdot \sqrt{1 - \frac{V_1^2 \cdot T_1^2 \cdot n^2}{V_{InPeak}^2 \cdot T_{On}^2}} + \frac{V_1 \cdot T_1^2 \cdot n^2}{2 \cdot L_P \cdot T_S} \cdot \left[\arcsin \left(\frac{V_1 \cdot T_1 \cdot n}{V_{InPeak} \cdot T_{On}} \right) - \frac{\pi}{2} \right] \right\} \quad (15)$$

Channel 2 can be evaluated in a similar way. The waveforms for Channel 2 are shown in Figure 12.

Beginning with Equation 14 and substituting channel 2 variables for their channel 1 counterparts and $I_{Peak} \cdot \Delta I_1$ for I_{Peak} yields the following definition for the channel 2 current averaged over the line cycle:

$$I_{AvgCycle2} = \frac{2}{\pi} \cdot \left[\int_{\theta_1}^{\theta_2} \left(\frac{V_{InPeak}^2 \cdot T_{On}^2}{2 \cdot V_2 \cdot L_P \cdot T_S} \cdot \sin^2(\theta) - \frac{V_{Peak} \cdot V_1 \cdot T_{On} \cdot T_1 \cdot n}{V_2 \cdot L_P \cdot T_S} \cdot \sin(\theta) + \frac{V_1^2 \cdot T_1^2 \cdot n^2}{2 \cdot V_2 \cdot L_P \cdot T_S} \right) \cdot d\theta + \int_{\theta_2}^{\pi/2} \left(\frac{V_{InPeak} \cdot T_{On} \cdot T_2 \cdot n}{L_P \cdot T_S} \cdot \sin(\theta) - \frac{V_1 \cdot T_1 \cdot T_2 \cdot n^2}{L_P \cdot T_S} - \frac{V_2 \cdot T_2^2 \cdot n^2}{2 \cdot L_P \cdot T_S} \right) \cdot d\theta \right] \quad (16)$$



a) Channel 2 conducts for time T_2 with energy left in the transformer

b) Energy is depleted from transformer before time T_2 has passed

Figure 12 – Waveforms for Channel 2

Note that during the period between 0 and θ_1 the channel 2 current is zero. This is true because during this time the transformer energy depletes to zero before time T_1 has passed as shown in Figure 11b. Therefore only channel 1 receives current during this time.

Evaluating Equation 16 and substituting $\arcsin\left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}}\right)$ for θ_2 yeilds:

$$I_{AvgCycle\ 2} = \frac{2}{\pi} \cdot \left[\begin{aligned} & \left(\frac{V_{Peak}^2 \cdot T_{On}^2}{2 \cdot V_2 \cdot L_P \cdot T_S} \cdot V_1 \cdot T_1 \cdot n - \frac{V_{Peak} \cdot V_1 \cdot T_{On} \cdot T_1 \cdot n}{V_2 \cdot L_P \cdot T_S} \right) \cdot \sqrt{1 - \left(\frac{V_1 \cdot T_1 \cdot n}{V_{Peak} \cdot T_{On}} \right)^2} \\ & + \left(\frac{V_{Peak} \cdot V_1 \cdot T_{On} \cdot T_1 \cdot n}{V_2 \cdot L_P \cdot T_S} + \frac{V_{Peak} \cdot T_{On} \cdot T_2 \cdot n}{L_P \cdot T_S} - \frac{V_{Peak}^2 \cdot T_{On}^2}{2 \cdot V_2 \cdot L_P \cdot T_S} \cdot \frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}} \right) \cdot \sqrt{1 - \left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}} \right)^2} \\ & + \left(\frac{V_{Peak}^2 \cdot T_{On}^2}{4 \cdot V_2 \cdot L_P \cdot T_S} + \frac{V_1^2 \cdot T_1^2 \cdot n^2}{2 \cdot V_2 \cdot L_P \cdot T_S} + \frac{V_1 \cdot T_1 \cdot T_2 \cdot n^2}{L_P \cdot T_S} + \frac{V_2 \cdot T_2^2 \cdot n^2}{L_P \cdot T_S} \right) \cdot \arcsin\left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}}\right) \\ & - \left(\frac{V_{Peak}^2 \cdot T_{On}^2}{4 \cdot V_2 \cdot L_P \cdot T_S} + \frac{V_1^2 \cdot T_1^2 \cdot n^2}{2 \cdot V_2 \cdot L_P \cdot T_S} \right) \cdot \arcsin\left(\frac{V_1 \cdot T_1 \cdot n}{V_{Peak} \cdot T_{On}}\right) \\ & - \left(\frac{V_1 \cdot T_1 \cdot T_2 \cdot n^2}{L_P \cdot T_S} + \frac{V_2 \cdot T_2^2 \cdot n^2}{L_P \cdot T_S} \right) \cdot \frac{\pi}{2} \end{aligned} \right] \quad (17)$$

Finally, the cycle average of channel 3 is similar with the exception that it conducts in only one mode of operation: the switch is always left on until transformer energy is depleted. Since channel 3 is the last channel, there is no need to leave energy in the transformer for subsequent channels. The waveform for channel 3 is shown in Figure 13.

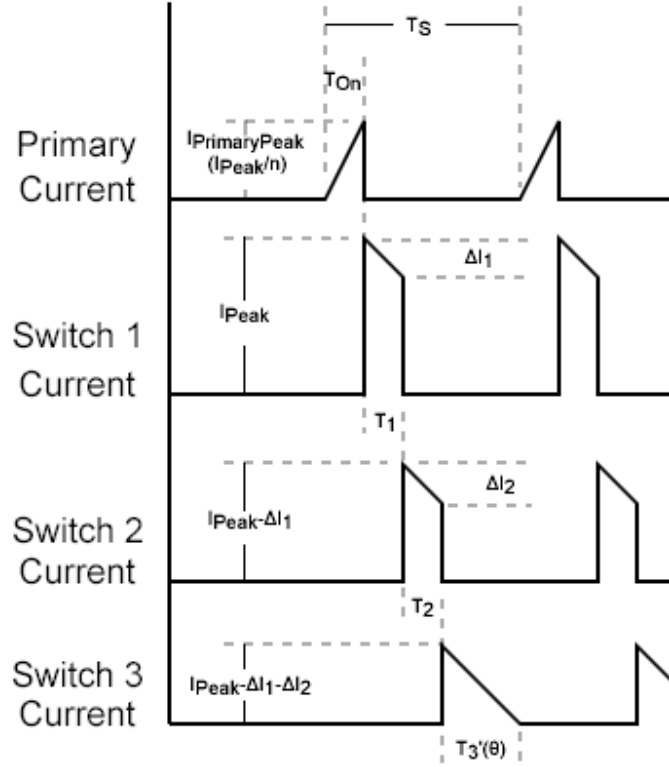


Figure 13 – Waveform for Channel 3

The current in channel 3 averaged over the time T_s is defined as follows:

$$I_{Avg3}(\theta) = \frac{1}{2} \cdot \frac{(I_{Peak}(\theta) - \Delta I_1 - \Delta I_2) \cdot T_3'(\theta)}{T_s} \quad \text{for } I_{Peak}(\theta) \geq \Delta I_1 + \Delta I_2 \quad (18)$$

Where:

$$V_3 = \frac{L_P}{n^2} \cdot \frac{I_{Peak}(\theta) - \Delta I_1 - \Delta I_2}{T_3'(\theta)} \Rightarrow T_3'(\theta) = \frac{L_P \cdot (I_{Peak}(\theta) - \Delta I_1 - \Delta I_2)}{n^2 \cdot V_3} \quad (19)$$

Combining Equations 18 and 19 yields:

$$I_{Avg3}(\theta) = \frac{(I_{Peak}(\theta) - \Delta I_1 - \Delta I_2)^2}{2 \cdot V_3 \cdot T_S \cdot n^2} \text{ for } I_{Peak}(\theta) \geq \Delta I_1 + \Delta I_2 \quad (20)$$

I_{Avg3} evaluates to zero for all other values of $I_{Peak}(\theta)$. Therefore, averaging over the full line cycle:

$$I_{AvgCycle3} = \frac{1}{\pi/2} \cdot \int_0^{\pi/2} I_{Avg3}(\theta) \cdot d\theta = \frac{2}{\pi} \cdot \int_0^{\theta_2} \frac{(I_{Peak}(\theta) - \Delta I_1 - \Delta I_2)^2}{2 \cdot V_3 \cdot T_S \cdot n^2} \cdot d\theta \quad (21)$$

Where θ_2 is the input phase angle where I_{Peak} is equal to the sum $\Delta I_1 + \Delta I_2$. It evaluates identically to the example for channel 2:

$$\theta_2 = \arcsin\left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}}\right) \quad (22)$$

Combining Equations 21 and 22, and evaluating yields the form:

$$I_{AvgCycle3} = \frac{1}{\pi \cdot L_P \cdot V_3 \cdot T_S} \cdot \left[\begin{aligned} & V_{Peak}^2 \cdot T_{On}^2 \cdot \left(\frac{\pi}{4} - \frac{1}{2} \arcsin\left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}}\right) \right) \\ & + \frac{V_2 \cdot T_2 \cdot n}{2 \cdot V_{Peak} \cdot T_{On}} \cdot \sqrt{1 - \left(\frac{V_1 \cdot T_1 \cdot n}{V_{Peak} \cdot T_{On}}\right)^2} \\ & - 2 \cdot V_{Peak} \cdot T_{On} (V_1 \cdot T_1 \cdot n + V_2 \cdot T_2 \cdot n) \cdot \sqrt{1 - \left(\frac{V_1 \cdot T_1 \cdot n}{V_{Peak} \cdot T_{On}}\right)^2} \\ & + (V_1 \cdot T_1 \cdot n + V_2 \cdot T_2 \cdot n)^2 \cdot \left(\frac{\pi}{2} - \arcsin\left(\frac{V_2 \cdot T_2 \cdot n}{V_{Peak} \cdot T_{On}}\right) \right) \end{aligned} \right] \quad (23)$$

Equations 15, 17, and 23 represent a set of simultaneous equations where T_{On} , T_1 , and T_2 are the unknowns. All other variables in these equations, including the controlled outputs, V_1 , V_2 , V_3 , $I_{AvgCycle1}$, $I_{AvgCycle2}$, and $I_{AvgCycle3}$, may be assumed constant.

As an example, the following values may represent a system typical for a 3 string LED light using Red, Green, and Blue strings.

$$\begin{array}{lll}
 V_{Peak} = 120V \cdot \sqrt{2} & L_p = 210\mu H & n = 3 \\
 & T_s = 10\mu s & \\
 I_{AvgCycle1} = 400mA & I_{AvgCycle2} = 350mA & I_{AvgCycle3} = 250mA \\
 V_1 = 38.88V & V_2 = 40.8V & V_3 = 28V
 \end{array}$$

Table 1 – Steady State System Values

Using MathCAD to substitute values above and simultaneously solve Equations 15, 17, and 23 to evaluate T_{On} , T_1 , and T_2 yields:

$$T_{On} = 3.82\mu s \qquad T_1 = 0.97\mu s \qquad T_2 = 1.17\mu s$$

Table 2 – Steady State Switching Periods

Using these values for T_{On} , T_1 , and T_2 will drive a set of LED loads at the desired current for the given operating point, however, in any real-world application the operating point will not be constant. V_{Peak} is an uncontrolled input and therefore must be considered a disturbance. Also, the LED loads in question may not draw exactly the intended current at the intended voltage and the load will almost certainly change with respect to temperature.

For these reasons it is desirable to create a linear model of the system for the purpose of enclosing it with a control system.

2.5 System Linearization and Modeling

It is clear by inspection that Equations 15, 17, and 23 are non-linear. This is due to not only square root and arcsin terms, but also to V_{Peak} , V_1 , V_2 , V_3 , and T_{On} appearing in the denominator of fractional terms and the existence of product terms between these variables. Non-linearity is

not ideal for application of a control system, however, non-linear systems can typically be linearized around a specific operating condition. Also, Equations 15, 17, and 23 must be slightly modified to put them in terms of a typical linear system, shown in Equation 24

$$\frac{d}{dt} \bar{x}(t) = \mathbf{A} \bar{x}(t) + \mathbf{B} \bar{u}(t) \quad (24)$$

$$\bar{y}(t) = \mathbf{C} \bar{x}(t) + \mathbf{D} \bar{u}(t) \quad (25)$$

$I_{AvgCycle}$ variables are not states since they depend directly on inputs and can change instantaneously from one switching cycle to the next. Therefore the equations describing $I_{AvgCycle}$ currents must be redefined in terms of state variables in order to fit them to the form of Equation 24.

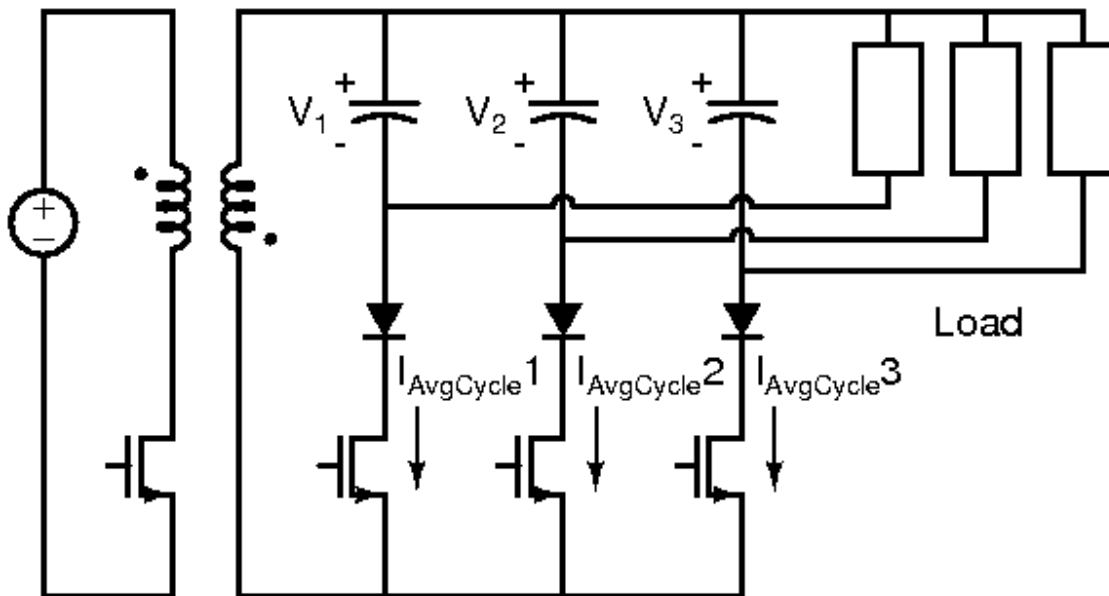


Figure 14 – MIROF Converter with System Variables Shown

The application circuit is shown with the system voltages and currents in Figure 14. The capacitor voltages V_1 , V_2 , and V_3 represent system states in this case (Note: earlier the author asserted that these voltages could be assumed constant. This is true in the steady state operating point the system is designed to run in. V_1 , V_2 , and V_3 are controlled dynamic outputs,

and therefore are intended to be constant). The inductor current would normally also constitute a state, however, that is not the case in this example. Since the converter runs in discontinuous current mode the transformer energy is completely depleted at the end of each switching cycle. Therefore the current level in the transformer primary during one switching cycle has no effect on the level during the next cycle. This represents the ability by the transformer to change its state “instantaneously” at frequencies below the switching frequency. Since we are not interested in frequencies above the switching frequency, we will consider the transformer to not represent a state in this system.

The inputs to the system are V_{Peak} , T_{On} , T_1 , and T_2 . V_{Peak} is not a controlled input, and therefore will be considered a disturbance. For simplicity it will be included in the u vector with the controlled inputs.

Finally, the outputs are defined as the cycle currents which are the system variables that we are interested in directly controlling. Based on these definitions the system will have the following form:

$$\frac{d}{dt} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \mathbf{A} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \mathbf{B} \begin{bmatrix} T_{On} \\ T_1 \\ T_2 \\ V_{Peak} \end{bmatrix} \quad (26)$$

$$\begin{bmatrix} I_{AvgCycle1} \\ I_{AvgCycle2} \\ I_{AvgCycle3} \end{bmatrix} = \mathbf{C} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \mathbf{D} \begin{bmatrix} T_{On} \\ T_1 \\ T_2 \\ V_{Peak} \end{bmatrix}$$

The state equations for V_1 , V_2 , and V_3 can be derived from the equation:

$$I = C \frac{dV}{dt} \quad (27)$$

Using the following model we can define each output of our system:

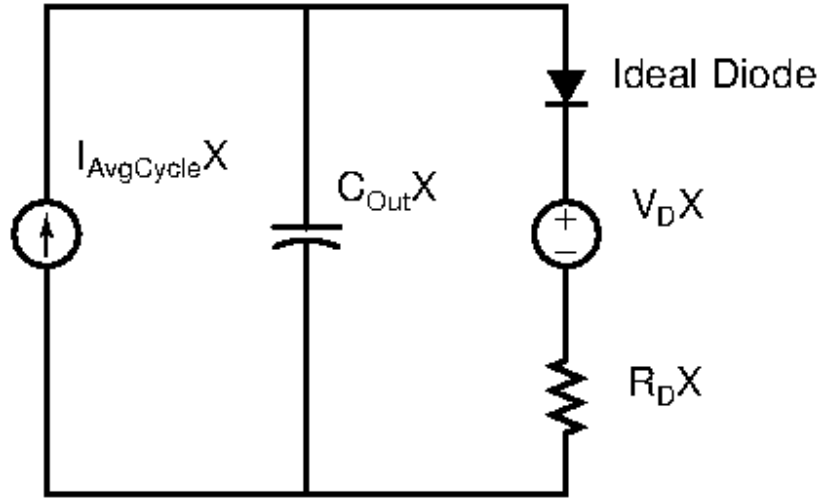


Figure 15 – Linear LED Load Model

V_{DX} and R_{DX} in the figure above represent a linear approximation of the LED load. These characteristics for the individual LEDs are estimated from the component datasheet^[28]. The values of these characteristics are then determined by multiplying the individual values by the number of LEDs in each string. The system value calculations are shown below in Table 3:

$$V_{D1} = 12 \cdot 2.99V = 35.88V \quad V_{D2} = 12 \cdot 3.0001V = 36.001V \quad V_{D3} = 12.7505 \cdot 2V = 25.501V$$

$$R_{D1} = 12 \cdot 0.625\Omega = 7.5\Omega \quad R_{D2} = 12 \cdot 1.333\Omega = 15.996\Omega \quad R_{D3} = 14 \cdot 0.714\Omega = 9.996\Omega$$

Table 3 – LED Linear Characteristics

Defining the state equation for the capacitor voltage in Figure 15 gives us a generic state model for all three of our states:

$$\frac{d}{dt} V_X = \frac{I_{AvgCycleX} - \frac{V_X - V_{DX}}{R_{DX}}}{C_{outX}} \quad (28)$$

Using Equation 28 and substituting Equations 15, 17, and 23 for $I_{AvgCycle1}$, $I_{AvgCycle2}$, and $I_{AvgCycle3}$ respectively will yield the state equations of the system. As indicated previously, these

equations are non-linear and must be linearized^[29]. Matrix **A**, shown in Equation 26, can be solved as follows:

$$\mathbf{A} = \begin{bmatrix} \frac{\delta}{\delta V_1} \frac{I_{AvgCycle\ 1}(V_1) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle\ 1}(V_2) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle\ 1}(V_3) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} \\ \frac{\delta}{\delta V_1} \frac{I_{AvgCycle\ 2}(V_1) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle\ 2}(V_2) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle\ 2}(V_3) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} \\ \frac{\delta}{\delta V_1} \frac{I_{AvgCycle\ 3}(V_1) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle\ 3}(V_2) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle\ 3}(V_3) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} \end{bmatrix} \quad (29)$$

After performing the derivation steady state values in Table 1 and the switching periods in Table 2 may be substituted for all variables in the resulting matrix except the differentiated states. When this is done, the A matrix evaluates to the following:

$$\mathbf{A} = \begin{bmatrix} -255 & 0 & 0 \\ -7.9 & -121 & 0 \\ -6.6 & -14.6 & -122 \end{bmatrix} \quad (30)$$

Incidentally, the eigenvalues of this matrix—solutions to the equation $\mathbf{A}\lambda = \bar{p}\lambda$ —are negative and therefore indicate that the system is stable^[30] in the operating point that we've chosen:

$$\bar{\lambda} = \begin{bmatrix} -122 \\ -121 \\ -255 \end{bmatrix} \quad (31)$$

Solving for B, C, and D matrices is similar and is shown below:

$$\mathbf{B} = \begin{bmatrix} \frac{\delta}{\delta T_{On}} \frac{I_{AvgCycle1}(T_{On}) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta T_1} \frac{I_{AvgCycle1}(T_1) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta T_2} \frac{I_{AvgCycle1}(T_2) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle1}(V_{Peak}) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} \\ \frac{\delta}{\delta T_{On}} \frac{I_{AvgCycle2}(T_{On}) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta T_1} \frac{I_{AvgCycle2}(T_1) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta T_2} \frac{I_{AvgCycle2}(T_2) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle2}(V_{Peak}) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} \\ \frac{\delta}{\delta T_{On}} \frac{I_{AvgCycle3}(T_{On}) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta T_1} \frac{I_{AvgCycle3}(T_1) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta T_2} \frac{I_{AvgCycle3}(T_2) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle3}(V_{Peak}) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} \end{bmatrix} \quad (32)$$

$$\mathbf{B} = \begin{bmatrix} 2.325 \cdot 10^8 & 6.413 \cdot 10^8 & 0 & 6.283 \\ 2.642 \cdot 10^8 & -3.181 \cdot 10^8 & 3.693 \cdot 10^8 & 7.141 \\ 3.051 \cdot 10^8 & -2.662 \cdot 10^8 & -2.975 \cdot 10^8 & 8.246 \end{bmatrix} \quad (33)$$

$$\mathbf{C} = \begin{bmatrix} \frac{\delta}{\delta V_1} I_{AvgCycle\ 1}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 1}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 1}(V_3) \\ \frac{\delta}{\delta V_1} I_{AvgCycle\ 2}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 2}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 2}(V_3) \\ \frac{\delta}{\delta V_1} I_{AvgCycle\ 3}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 3}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 3}(V_3) \end{bmatrix} \quad (34)$$

$$\mathbf{C} = \begin{bmatrix} -1.824 \cdot 10^{-3} & 0 & 0 \\ -4.199 \cdot 10^{-3} & -1.765 \cdot 10^{-3} & 0 \\ -5.9 \cdot 10^{-3} & -7.56 \cdot 10^{-3} & -8.929 \cdot 10^{-3} \end{bmatrix} \quad (35)$$

$$\mathbf{D} = \begin{bmatrix} \frac{\delta}{\delta T_{On}} I_{AvgCycle\ 1}(T_{On}) & \frac{\delta}{\delta T_1} I_{AvgCycle\ 1}(T_1) & \frac{\delta}{\delta T_2} I_{AvgCycle\ 1}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 1}(V_{Peak}) \\ \frac{\delta}{\delta T_{On}} I_{AvgCycle\ 2}(T_{On}) & \frac{\delta}{\delta T_1} I_{AvgCycle\ 2}(T_1) & \frac{\delta}{\delta T_2} I_{AvgCycle\ 2}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 2}(V_{Peak}) \\ \frac{\delta}{\delta T_{On}} I_{AvgCycle\ 3}(T_{On}) & \frac{\delta}{\delta T_1} I_{AvgCycle\ 3}(T_1) & \frac{\delta}{\delta T_2} I_{AvgCycle\ 3}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 3}(V_{Peak}) \end{bmatrix} \quad (36)$$

$$\mathbf{D} = \begin{bmatrix} 1.232 \cdot 10^5 & 3.399 \cdot 10^5 & 0 & 3.33 \cdot 10^{-3} \\ 1.4 \cdot 10^5 & -1.686 \cdot 10^5 & 1.957 \cdot 10^5 & 3.785 \cdot 10^{-3} \\ 2.715 \cdot 10^5 & -2.369 \cdot 10^5 & -2.648 \cdot 10^5 & 7.339 \cdot 10^{-3} \end{bmatrix} \quad (37)$$

These matrices represent the linear system equivalent of our converter at the operating point we've chosen. Since the nature of electronic systems is highly variable (load currents and input voltages are unpredictable and can change rapidly) it is preferable to use a matrix of classical SISO (Single Input Single Output) compensators as opposed to a single modern MIMO (Multiple Input Multiple Output) compensator. This is true because SISO compensators tend to be more robust to great changes in plant conditions than do their MIMO counterparts^[29].

Problematically, this is not necessarily possible for all multistate systems. As a requirement, the unrelated inputs and outputs of the plant must be decoupled from one another^[31]. Using the MIROF converter as an example, this means we would want T_{on} to have a strong effect on V_1 and no effect on the other two output voltages. T_1 would have a strong impact on V_2 , but no impact on V_1 and V_3 , and T_2 would have a strong impact on V_3 but no impact on the others.

This is not always easy to evaluate since the correlation between input and output is frequency dependent, however, at a minimum the system DC gain must meet this requirement. The DC gain matrix is very useful since it's easy to compute. \mathbf{H}_{DC} represents the DC gain of our linearized converter and is shown below:

$$\bar{y}_{SteadyState} = \mathbf{H}_{DC} \cdot \bar{u}_{SteadyState} \quad (38)$$

Where:

$$\mathbf{H}_{DC} = \mathbf{D} - \mathbf{C} \cdot \mathbf{A}^{-1} \cdot \mathbf{B} \quad (39)$$

Evaluating Equation 39 yields the following form for Equation 38:

$$\begin{bmatrix} I_{AvgCycle1} \\ I_{AvgCycle2} \\ I_{AvgCycle3} \end{bmatrix} = \begin{bmatrix} 1.215 \cdot 10^5 & 3.353 \cdot 10^5 & 0 & 3.285 \cdot 10^{-3} \\ 1.325 \cdot 10^5 & -1.742 \cdot 10^5 & 1.903 \cdot 10^5 & 3.58 \cdot 10^{-3} \\ 2.306 \cdot 10^5 & -2.13 \cdot 10^5 & -2.629 \cdot 10^5 & 6.232 \cdot 10^{-3} \end{bmatrix} \cdot \begin{bmatrix} T_{On} \\ T_1 \\ T_2 \\ V_{Peak} \end{bmatrix} \quad (40)$$

Equation 40 tells us several things: first since the values in the fourth column are all very small, it tells us that the disturbance V_{Peak} has a much smaller impact on the outputs than the controlled inputs do. Secondly, since the values in the third row are generally greater in magnitude than their counterparts in the other two rows, it tells us that the inputs (including the disturbance V_{Peak}) tend to have greater impacts on $I_{AvgCycle3}$ than they do on either $I_{AvgCycle1}$ or $I_{AvgCycle2}$. Third, for the output $I_{AvgCycle2}$ there is very little difference between the gain factors of the three controlled inputs, meaning that they all have nearly equal control over channel 2.

While the first point is generally desired for any linear system points 2 and 3 give strong evidence that this system does not have the desired decoupling characteristics that we are looking for.

2.6 I/O Decoupling

Poor system decoupling in our example above may be in part attributed to the fact that while T_1 and T_2 are intended to control the current in strings 1 and 2, T_{On} does not have a channel that it controls directly. T_3 would be ideal for controlling a 3rd string current, and while this is technically a system characteristic it is not directly controllable since the period ends at the point that the transformer is depleted of energy (as opposed to when a switch changes state).

It is therefore desirable to redefine the inputs of the system so that they each have some relevance to an individual string current. Imagine then a conditioning system, $F(s)$, that appears before the plant and transforms the inputs into a more useful form. Such a system is shown below in Figure 16.

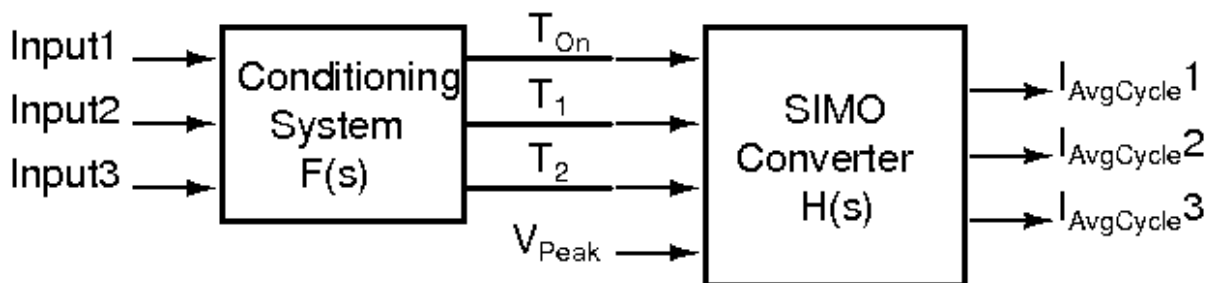


Figure 16 – Input Conditioning System $F(s)$ Decouples System $H(s)$

As a starting point assume that for the system $F(s)$ $Input_1$ and $Input_2$ pass directly through to T_1 and T_2 respectively with no gain or summing terms. Presumably these inputs would have full control over $I_{AvgCycle1}$ and $I_{AvgCycle2}$ with no coupling since T_1 and T_2 control the string current conduction times of strings 1 and 2. Upon further inspection, however, it becomes clear that time T_1 has a significant impact on the conducted current output of string 2, since changing the

T_1 conduction time will affect the current with which string 2 begins its conduction time. This is illustrated in Figure 17.

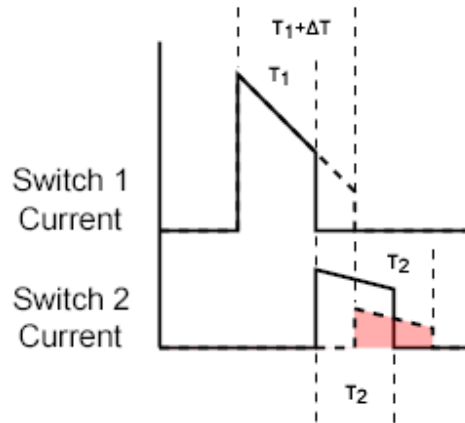


Figure 17 – Effect of T_1 on I_2

$Input_1$ therefore must not only control T_1 , but must compensate for an effect on string 2 by also controlling either T_{On} or T_2 directly. It seems clear that attempting to control T_2 with T_1 would likely result in the same coupling problems that we’re trying to eliminate, so controlling T_{On} is the preferred method.

This must be done carefully. T_2 for instance has the same effect on the conducted current of string 3—it reduces the current of the subsequent string when lengthened and increases current when shortened—it has *no* effect, however, on the conduction current of channel 1. This is due simply to the fact that channel 1 has completed conduction altogether by the time the switch on string 2 begins its conduction time. Increasing T_{On} in this case will offset the effect of the T_2 change on string 3, but it will also have the effect of increasing the current in string 1. Input 3 is also dangerous—the only way to increase current in string 3 is by increasing T_{On} thereby increasing current in all channels.

The solution lies with the fact that each switching period bounds the cumulative conduction time of the 4 switches. Since the system is fixed frequency, there is a defined amount of time that the switching series must be accomplished in. Not only must the entire switching series be

completed, but the transformer energy must also be depleted to zero before the next switching cycle begins.

We would like the total switch conduction time to come very close to 100% of the switching period in order to maximize our use of the transformer core and keep RMS currents low. Since the converter is running in fixed time mode, the switch conduction time will not change over the course of the input voltage half cycle, but rather will change slowly and only in response to control laws. Because we're running at close to 100% conduction throughout the entire half cycle, there is not much room for the switch periods to grow. In order for one to be longer, another one (or both of the others) must become shorter.

This is the answer that will help us complete our decoupling system. Each input must have some direct control over T_{On} , and as each input grows, so must T_{On} . Based on These requirements we define T_{On} below:

$$T_{On} = u_1 + u_2 + u_3 \quad (41)$$

For T_1 , T_2 , and T_3 , we will assume they share the rest of the conduction time and that each is in proportion to the others as its input counterpart is in proportion to the other inputs. More specifically:

$$T_S - T_{On} = T_1 + T_2 + T_3 \quad (42)$$

$$\frac{T_1}{u_1} = \frac{T_2}{u_2} = \frac{T_3}{u_3} \quad (43)$$

Note that T_3 is not the same as the value T_3' discussed in Section 2.4. T_3 represents the on-time of switch 3 which is the same throughout the entire input voltage line cycle (even if Switch 3 does not conduct current for the entirety of its on-time). T_3' is the conduction time of channel 3, and it does not include the time for which current through switch 3 is zero.

Using Equations 42 and 43 we can obtain the definition for T_1 as follows:

$$\frac{T_1}{T_S - T_{On}} = \frac{u_1}{u_1 + u_2 + u_3} \quad (44)$$

Solving for T_1 and substituting Equation 41:

$$T_1 = \frac{u_1}{u_1 + u_2 + u_3} \cdot (T_S - (u_1 + u_2 + u_3)) \quad (45)$$

Solving for T_2 in the same fashion:

$$T_2 = \frac{u_2}{u_1 + u_2 + u_3} \cdot (T_S - (u_1 + u_2 + u_3)) \quad (46)$$

We can solve T_3 similarly, although this is only a reference value since T_3 is not a valid input to our plant.

Using values of T_{On} , T_1 , T_2 , and T_S from Table 1 and Table 2 we may solve Equations 41, 46, and 48 simultaneously to find u_1 , u_2 , and u_3 . The solution yields the following vector:

$$\bar{u} = \begin{bmatrix} 5.99 \\ 7.208 \\ 25.02 \end{bmatrix} \cdot 10^{-7} \quad (47)$$

Equations 41, 45, and 46 represent our conditioning system $F(s)$. This may be linearized the same way that we linearized our initial system:

$$F(s) = \begin{bmatrix} \frac{\delta}{\delta u_1} T_{On}(u_1) & \frac{\delta}{\delta u_2} T_{On}(u_2) & \frac{\delta}{\delta u_3} T_{On}(u_3) \\ \frac{\delta}{\delta u_1} T_1(u_1) & \frac{\delta}{\delta u_2} T_1(u_2) & \frac{\delta}{\delta u_3} T_1(u_3) \\ \frac{\delta}{\delta u_1} T_2(u_1) & \frac{\delta}{\delta u_2} T_2(u_2) & \frac{\delta}{\delta u_3} T_2(u_3) \end{bmatrix} \quad (48)$$

$F(s)$, however, is a matrix gain with no states, and therefore should be referred to as \mathbf{F} .

Substituting the values of vector \bar{u} into the result of Equation 48 produces the matrix below:

$$\mathbf{F} = \begin{bmatrix} 1 & 1 & 1 \\ 1.206 & -0.41 & -0.41 \\ -0.493 & 1.123 & -0.493 \end{bmatrix} \quad (49)$$

\mathbf{F}_{Full} , a more complete form of the matrix \mathbf{F} , which includes a passthrough for the disturbance input V_{In} may be found by creating a fourth row and column with a unity gain. This will allow us to multiply \mathbf{F} by the DC gain matrix \mathbf{H}_{DC} .

$$\mathbf{F}_{Full} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1.206 & -0.41 & -0.41 & 0 \\ -0.493 & 1.123 & -0.493 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (50)$$

Finally, the DC gain of the full system may be computed by multiplying the two DC gain matrices:

$$\bar{\mathbf{y}}_{SteadyState} = \mathbf{H}_{DC} \cdot \mathbf{F}_{Full} \cdot \bar{\mathbf{u}}_{SteadyState} \quad (51)$$

$$\begin{bmatrix} I_{AvgCycle 1} \\ I_{AvgCycle 2} \\ I_{AvgCycle 3} \end{bmatrix} = \begin{bmatrix} 3.945 \cdot 10^6 & -0.12 \cdot 10^6 & -0.12 \cdot 10^6 & 0.025 \\ -2.745 \cdot 10^6 & 6.681 \cdot 10^6 & 1.76 \cdot 10^6 & 0.057 \\ 0.78 \cdot 10^6 & 0.78 \cdot 10^6 & 3.976 \cdot 10^6 & 0.059 \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ V_{Peak} \end{bmatrix} \quad (52)$$

The above gain matrix represents a definite improvement over the system in Equation 40. In this system the diagonals are the largest gains (in magnitude) of the entire system. $I_{AvgCycle 1}$, for instance, may easily be controlled by u_1 with minimal influence from the other inputs, and the same is true of the other output currents and their inputs respectively.

While we have achieved decoupling in this system, the system is still highly non-linear (this is apparent by examining Equations 15, 17, 23 from which our system matrices were derived).

Extreme nonlinearity is undesirable because it will narrow the range of operating points in which our controller will stabilize the system.

At this point we will reconsider our use of fixed time sequencing and instead evaluate fixed ratio sequencing (Figure 9) to see whether it will yield a solution which is more linear.

2.7 Fixed Ratio Sequence Modeling

Creating a system model for a fixed ratio sequence is much like creating a model for a fixed time sequence, although there are some important differences. For instance on-time of the switches is no longer a direct input. This is true because the on-time changes as a function of input phase angle. Instead we would prefer to use an input that represents a percentage of secondary conduction time—that way the input may stay constant throughout the input phase angle and update infrequently. Figure 18 shows the switch timing of switches 1, 2, and 3.

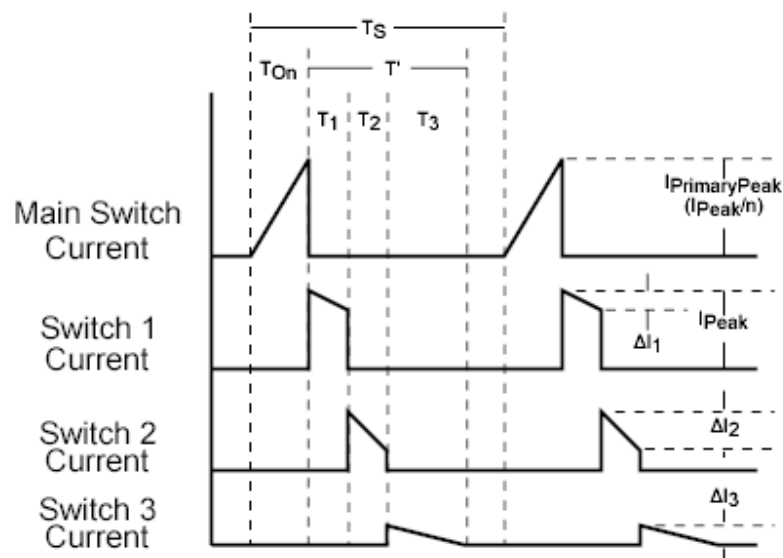


Figure 18 – Fixed Ratio Timing Diagram

Since T_1 , T_2 , and T_3 are constantly changing, we must define three inputs which we may use to control the switch time:

$$d_1 = \frac{T_1}{T'} \quad d_2 = \frac{T_2}{T'} \quad d_3 = \frac{T_3}{T'} \quad (53)$$

Using these inputs we can calculate the average current through each string. Beginning with string 1 and substituting T_1 (above) into Equation 6 from Section 2.4:

$$I_{Avg1}(\theta) = \frac{I_{Peak}(\theta) \cdot d_1 \cdot T'(\theta) - \frac{1}{2} \cdot \Delta I_1(\theta) \cdot d_1 \cdot T'(\theta)}{T_S} \quad (54)$$

Unlike Equation 6, Equation 54 is true for all values of θ . This is because for fixed ratio sequencing each of the switches conducts before the transformer is depleted of energy. Each switch conducts for a specified percentage of the secondary conduction time.

Aside from the variables that have already been defined in previous sections, the following equation must be used to evaluate Equation 54 (The proof of this equality can be found in Appendix B):

$$T'(\theta) = \frac{L_P \cdot I_{Peak}(\theta)}{n^2 \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (55)$$

Combining Equations 54, 53, 55, 4, and 5 yields the following form:

$$I_{Avg1}(\theta) = \frac{V_{In}^2(\theta) \cdot T_{On}^2 \cdot d_1}{T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \cdot \left[1 - \frac{V_1 \cdot d_1}{2 \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \right] \quad (56)$$

Using Equation 13 to average the channel 1 current over the line cycle, and substituting Equations 56 and 3 yields the following:

$$I_{AvgCycle1} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_1}{T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \cdot \left[1 - \frac{V_1 \cdot d_1}{2 \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \right] \cdot \int_0^{\pi} \sin^2 \theta \cdot d\theta \quad (57)$$

Finally Equation 62 can be simplified to the following form:

$$I_{AvgCycle1} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_1}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \cdot \left[1 - \frac{V_1 \cdot d_1}{2 \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \right] \quad (58)$$

This is clearly an improvement over Equation 15, and the solutions for $I_{AvgCycle2}$ and $I_{AvgCycle3}$ are similarly consolidated:

$$I_{AvgCycle2} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_2}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \cdot \left[1 - \frac{V_1 \cdot d_1 + \frac{1}{2} \cdot V_2 \cdot d_2}{(V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \right] \quad (59)$$

$$I_{AvgCycle3} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_3}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \cdot \left[1 - \frac{V_1 \cdot d_1 + V_2 \cdot d_2}{(V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \right] \quad (60)$$

While these are attractive compared to the previous solution, there are still further simplifications that can be made. By changing the order that the secondary switches conduct, we can not only reduce the complexity of the average string current calculation, but also force the average string current to be nearly linear with respect to inputs d_1 , d_2 , and d_3 .

2.8 Alternated Sequence Modeling

One problem with both the fixed time and fixed ratio sequence solutions previously presented is that there is inequity in the scale of the input signals. Channel 3 for instance always has the smallest average current value given equal conduction time among the three channels. This is true because Channel 3 always conducts after the other two, and therefore after the transformer has been partially depleted of energy by both Channel 1 and Channel 2.

Since the average current of channel 3 is small with respect to Channels 1 and 2, a change in the input d_3 will not produce as great an effect as an equal change applied to either of the other channels. Hence the sensitivity of $I_{AvgCycle3}$ to d_3 is small with respect to the sensitivity of $I_{AvgCycle2}$ to d_2 . This in turn is small compared to the sensitivity of $I_{AvgCycle1}$ to d_1 .

While this is not in itself a problem, it adds complication to a potential compensator for this system. The difference in sensitivities of the three channels can be reconciled by conditioning

the inputs with a static gain, although the gain factors are dependent on the state of the inputs d_1 , d_2 , and d_3 , and therefore will change with operating point.

This problem inspired an interest in alternating the order of conduction for the three switches. As an example, consider a scenario where each channel takes a turn as the first in the series, and the sequence repeats every three switching periods. In this configuration inputs d_1 , d_2 , and d_3 , will yield equal control over their respective outputs by virtue of the fact that they all have equal access to the high energy state of the transformer.

This previous example accomplishes the goal of equalizing I/O sensitivities; however, at the time that this solution was being considered preliminary calculations showed that the resulting average cycle currents were increasingly nonlinear with respect to inputs d_1 , d_2 , and d_3 . Another potential solution is to directly reverse the switch sequence every other switching period, shown below:

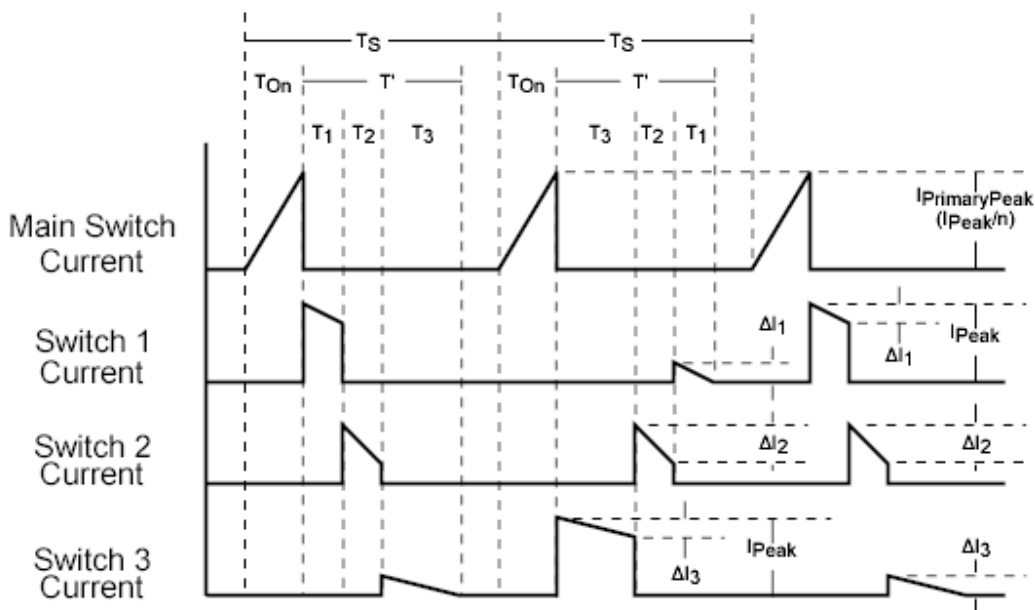


Figure 19 – Direct Reverse Sequence for Alternated Sequence SIMO

In this configuration, the average current for Channel 1 is calculated as the average of the two T_s periods:

$$I_{Avg1}(\theta) = \frac{1}{2} \cdot \left[\frac{I_{Peak}(\theta) \cdot T_1(\theta) - \frac{1}{2} \cdot \Delta I_1(\theta) \cdot T_1(\theta)}{T_S} + \frac{\frac{1}{2} \cdot \Delta I_1(\theta) \cdot T_1(\theta)}{T_S} \right] \quad (61)$$

Equation 61 can be simplified to the following:

$$I_{Avg1}(\theta) = \frac{I_{Peak}(\theta) \cdot T_1(\theta)}{2 \cdot T_S} \quad (62)$$

Combining Equation 62 with 4, 53, and 55 yields the following solution:

$$I_{Avg1}(\theta) = \frac{V_{In}(\theta)^2 \cdot T_{On}^2 \cdot d_1}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (63)$$

The dual period average for Channel 2 is similar except that it begins in a slightly different form:

$$I_{Avg2}(\theta) = \frac{1}{2} \cdot \left[\frac{(I_{Peak}(\theta) - \Delta I_1(\theta)) \cdot T_2(\theta) - \frac{1}{2} \cdot \Delta I_2 \cdot T_2(\theta)}{T_S} + \frac{(I_{Peak}(\theta) - \Delta I_3(\theta)) \cdot T_2(\theta) - \frac{1}{2} \cdot \Delta I_2 \cdot T_2(\theta)}{T_S} \right] \quad (64)$$

In order to reduce Equation 64, the following definition is needed: (This can be proved by inspection of Figure 19)

$$I_{Peak}(\theta) = \Delta I_1(\theta) + \Delta I_2(\theta) + \Delta I_3(\theta) \quad (65)$$

Combining Equations 64 and 65, the solution reduces to the same form as the average current for Channel 1:

$$I_{Avg2}(\theta) = \frac{I_{Peak}(\theta) \cdot T_2(\theta)}{2 \cdot T_S} \quad (66)$$

I_{Avg3} can be solved identically to I_{Avg1} , and therefore the full solutions to the remaining average channel currents are as follows:

$$I_{Avg2}(\theta) = \frac{V_{In}(\theta)^2 \cdot T_{On}^2 \cdot d_2}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (67)$$

$$I_{Avg3}(\theta) = \frac{V_{In}(\theta)^2 \cdot T_{On}^2 \cdot d_3}{2 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (68)$$

The average current over the full line cycle may be calculated in the same way that the average line cycle current was calculated on Page 36. Performing the calculation yields the following for the three channel currents:

$$I_{AvgCycle1} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_1}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (69)$$

$$I_{AvgCycle2} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_2}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (70)$$

$$I_{AvgCycle3} = \frac{V_{Peak}^2 \cdot T_{On}^2 \cdot d_3}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)} \quad (71)$$

The above equations appear to be very close to linear. They also appear to be decoupled since the d_x input consistently appears in the numerator of its respective output current with no other d inputs. The only exception to these observations is the $(V_1 d_1 + V_2 d_2 + V_3 d_3)$ term in the denominator. This term is a weighted average of the output voltages, and therefore the individual inputs are presumed to have a reduced impact through this term (since they only represent a portion of the average).

This must be verified so we will calculate the system matrices as we did in Section 2.5.

2.9 Alternated Sequence Linearization and Decoupling

In the following evaluation of the new linear system, we will use the same decoupling strategy that was used in Section 2.6. Instead of creating a separate conditioning system, however, we will substitute the decoupling variables directly into our system equations.

Below Equations 41 and 44 are repeated and modified to accommodate the new input variables:

$$T_{On} = u_1 + u_2 + u_3 \quad (72)$$

$$d_x = \frac{u_x}{u_1 + u_2 + u_3} \quad (73)$$

Equation 73 in this case is a generic definition for d_1 , d_2 , and d_3 .

Substituting Equations 72 and 73 into the system equations 69, 70, and 71, and simplifying yields the following new system equations:

$$I_{AvgCycle1} = \frac{V_{Peak}^2 \cdot (u_1 + u_2 + u_3)^2 \cdot u_1}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot u_1 + V_2 \cdot u_2 + V_3 \cdot u_3)} \quad (74)$$

$$I_{AvgCycle2} = \frac{V_{Peak}^2 \cdot (u_1 + u_2 + u_3)^2 \cdot u_2}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot u_1 + V_2 \cdot u_2 + V_3 \cdot u_3)} \quad (75)$$

$$I_{AvgCycle3} = \frac{V_{Peak}^2 \cdot (u_1 + u_2 + u_3)^2 \cdot u_3}{4 \cdot T_S \cdot L_P \cdot (V_1 \cdot u_1 + V_2 \cdot u_2 + V_3 \cdot u_3)} \quad (76)$$

Setting up the linearization as in Section 2.5, state matrix **A** is defined as follows:

$$\mathbf{A} = \begin{bmatrix} \frac{\delta}{\delta V_1} \frac{I_{AvgCycle 1} (V_1) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out 1}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle 1} (V_2) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out 1}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle 1} (V_3) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out 1}} \\ \frac{\delta}{\delta V_1} \frac{I_{AvgCycle 2} (V_1) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out 2}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle 2} (V_2) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out 2}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle 2} (V_3) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out 2}} \\ \frac{\delta}{\delta V_1} \frac{I_{AvgCycle 3} (V_1) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out 3}} & \frac{\delta}{\delta V_2} \frac{I_{AvgCycle 3} (V_2) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out 3}} & \frac{\delta}{\delta V_3} \frac{I_{AvgCycle 3} (V_3) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out 3}} \end{bmatrix} \quad (77)$$

Solving the partial derivative and substituting previous system parameters from Table 1, Table 2, and Table 3, \mathbf{A} evaluates to:

$$\mathbf{A} = \begin{bmatrix} -260 & -6.5 & -5.4 \\ -6.5 & -123 & -4.1 \\ -3.2 & -2.4 & -114 \end{bmatrix} \quad (78)$$

The eigenvalues of matrix \mathbf{A} are negative and indicate that the system is stable:

$$\bar{\lambda} = \begin{bmatrix} -261 \\ -123 \\ -113 \end{bmatrix} \quad (79)$$

The definitions and actual values for matrices \mathbf{B} , \mathbf{C} , and \mathbf{D} are all below:

$$\mathbf{B} = \begin{bmatrix} \frac{\delta}{\delta u_1} \frac{I_{AvgCycle1}(T_{On}) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta u_2} \frac{I_{AvgCycle1}(T_1) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta u_3} \frac{I_{AvgCycle1}(T_2) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle1}(V_{Peak}) - \frac{V_1 - V_{D1}}{R_{D1}}}{C_{Out1}} \\ \frac{\delta}{\delta u_1} \frac{I_{AvgCycle2}(T_{On}) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta u_2} \frac{I_{AvgCycle2}(T_1) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta u_3} \frac{I_{AvgCycle2}(T_2) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle2}(V_{Peak}) - \frac{V_2 - V_{D2}}{R_{D2}}}{C_{Out2}} \\ \frac{\delta}{\delta u_1} \frac{I_{AvgCycle3}(T_{On}) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta u_2} \frac{I_{AvgCycle3}(T_1) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta u_3} \frac{I_{AvgCycle3}(T_2) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} & \frac{\delta}{\delta V_{Peak}} \frac{I_{AvgCycle3}(V_{Peak}) - \frac{V_3 - V_{D3}}{R_{D3}}}{C_{Out3}} \end{bmatrix} \quad (80)$$

$$\mathbf{B} = \begin{bmatrix} 6.531 \cdot 10^8 & 1.746 \cdot 10^8 & 2.435 \cdot 10^8 & 10.673 \\ 1.387 \cdot 10^8 & 5.991 \cdot 10^8 & 1.826 \cdot 10^8 & 8.005 \\ 0.688 \cdot 10^8 & 0.65 \cdot 10^8 & 3.694 \cdot 10^8 & 8.246 \end{bmatrix} \quad (81)$$

$$\mathbf{C} = \begin{bmatrix} \frac{\delta}{\delta V_1} I_{AvgCycle\ 1}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 1}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 1}(V_3) \\ \frac{\delta}{\delta V_1} I_{AvgCycle\ 2}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 2}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 2}(V_3) \\ \frac{\delta}{\delta V_1} I_{AvgCycle\ 3}(V_1) & \frac{\delta}{\delta V_2} I_{AvgCycle\ 3}(V_2) & \frac{\delta}{\delta V_3} I_{AvgCycle\ 3}(V_3) \end{bmatrix} \quad (82)$$

$$\mathbf{C} = \begin{bmatrix} -4.599 \cdot 10^{-3} & -3.449 \cdot 10^{-3} & -2.874 \cdot 10^{-3} \\ -3.449 \cdot 10^{-3} & -2.587 \cdot 10^{-3} & -2.156 \cdot 10^{-3} \\ -2.874 \cdot 10^{-3} & -2.156 \cdot 10^{-3} & -1.796 \cdot 10^{-3} \end{bmatrix} \quad (83)$$

$$\mathbf{D} = \begin{bmatrix} \frac{\delta}{\delta U_1} I_{AvgCycle\ 1}(T_{On}) & \frac{\delta}{\delta U_2} I_{AvgCycle\ 1}(T_1) & \frac{\delta}{\delta U_3} I_{AvgCycle\ 1}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 1}(V_{Peak}) \\ \frac{\delta}{\delta U_1} I_{AvgCycle\ 2}(T_{On}) & \frac{\delta}{\delta U_2} I_{AvgCycle\ 2}(T_1) & \frac{\delta}{\delta U_3} I_{AvgCycle\ 2}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 2}(V_{Peak}) \\ \frac{\delta}{\delta U_1} I_{AvgCycle\ 3}(T_{On}) & \frac{\delta}{\delta U_2} I_{AvgCycle\ 3}(T_1) & \frac{\delta}{\delta U_3} I_{AvgCycle\ 3}(T_2) & \frac{\delta}{\delta V_{Peak}} I_{AvgCycle\ 3}(V_{Peak}) \end{bmatrix} \quad (84)$$

$$\mathbf{D} = \begin{bmatrix} 3.461 \cdot 10^5 & 0.926 \cdot 10^5 & 1.291 \cdot 10^5 & 5.657 \cdot 10^{-3} \\ 0.735 \cdot 10^5 & 3.175 \cdot 10^5 & 0.968 \cdot 10^5 & 4.243 \cdot 10^{-3} \\ 0.613 \cdot 10^5 & 0.578 \cdot 10^5 & 3.288 \cdot 10^5 & 3.536 \cdot 10^{-3} \end{bmatrix} \quad (85)$$

Finally, solving for the \mathbf{H}_{DC} matrix, defined in Equation 39:

$$\begin{bmatrix} I_{AvgCycle\ 1} \\ I_{AvgCycle\ 2} \\ I_{AvgCycle\ 3} \end{bmatrix} = \begin{bmatrix} 3.299 \cdot 10^5 & 0.721 \cdot 10^5 & 1.115 \cdot 10^5 & 5.172 \cdot 10^{-3} \\ 0.614 \cdot 10^5 & 3.022 \cdot 10^5 & 0.836 \cdot 10^5 & 3.879 \cdot 10^{-3} \\ 0.511 \cdot 10^5 & 0.4506 \cdot 10^5 & 3.178 \cdot 10^5 & 3.232 \cdot 10^{-3} \end{bmatrix} \cdot \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ V_{Peak} \end{bmatrix} \quad (86)$$

Equation 86 shows that the system DC gain is well decoupled. This is apparent since the $\mathbf{H}_{1,1}$, $\mathbf{H}_{2,2}$, and $\mathbf{H}_{3,3}$ terms are greater in magnitude than all other terms. Each of the $I_{AvgCycle}$ terms shows about 3 times more sensitivity to its respective input than to the other two inputs. Also, this system is fairly linear and will remain so regardless of the operating point—which was not the case with the fixed time sequence model.

While the DC gain of the system may be well decoupled, it is not clear whether the diagonal gains $\mathbf{H}_{1,1}$, $\mathbf{H}_{2,2}$, and $\mathbf{H}_{3,3}$ remain large with respect to all other gains over the entire frequency spectrum. To evaluate this we must look at the Magnitude plot of each gain in the $\mathbf{H}(s)$ matrix.

We can find a full description of the system $\mathbf{H}(s)$ using Equations 24 and 25. By solving Equation 24 for \bar{x} and then substituting the result into Equation 25, we find the following result:

$$Y(s) = [\mathbf{C} \cdot (s\mathbf{I} - \mathbf{A})^{-1} \cdot \mathbf{B} + \mathbf{D}] \cdot U(s) \quad (87)$$

Where s is the Laplace domain variable representing $\frac{d}{dt}$, and $Y(s)$ and $U(s)$ are the Laplace transforms of the time dependent vectors $\bar{y}(t)$ and $\bar{u}(t)$, respectively. The result of this calculation is too large to be displayed, but the Mathcad file used to calculate the results may be viewed in Appendix C.

The result of the calculation is a matrix of s-domain transfer functions. For the \mathbf{H} matrix shown below:

$$H(s) = \begin{bmatrix} H_{1,1}(s) & H_{1,2}(s) & H_{1,3}(s) & H_{1,4}(s) \\ H_{2,1}(s) & H_{2,2}(s) & H_{2,3}(s) & H_{2,4}(s) \\ H_{3,1}(s) & H_{3,2}(s) & H_{3,3}(s) & H_{3,4}(s) \end{bmatrix} \quad (88)$$

The following Bode magnitude plots show the frequency dependent gain magnitudes:

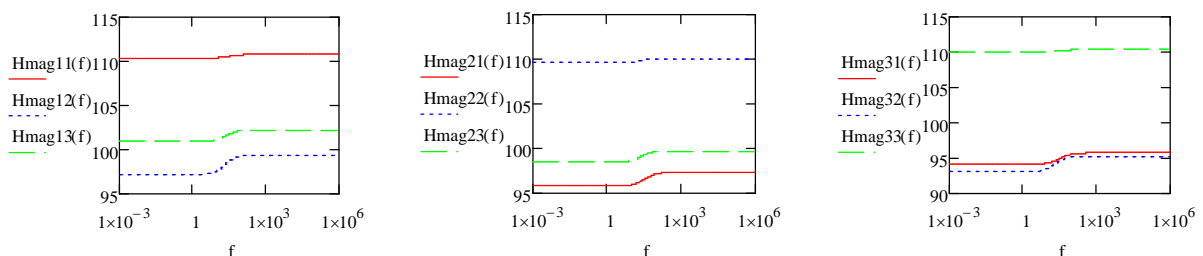


Figure 20 – H Matrix Gains Over Frequency

Figure 20 shows that the diagonal gains $H_{1,1}(s)$, $H_{2,2}(s)$, and $H_{3,3}(s)$ are each nearly 10dB greater in magnitude than all other gains over the entire frequency range. Note that the gains in the fourth column are not shown, but they are well below all other gains for all frequencies. This is evidence that the system is fully decoupled.

2.10 Closed Loop Feedback

Now that we have a system that we are satisfied with we can design a compensator to control it. Since the system is decoupled we can realize the goal of using a matrix of simple SISO compensators to stabilize the system. Using classical SISO compensators will increase the system's robustness to disturbance and will also simplify design and implementation. A diagram of the system with individual SISO controllers is shown in Figure 21

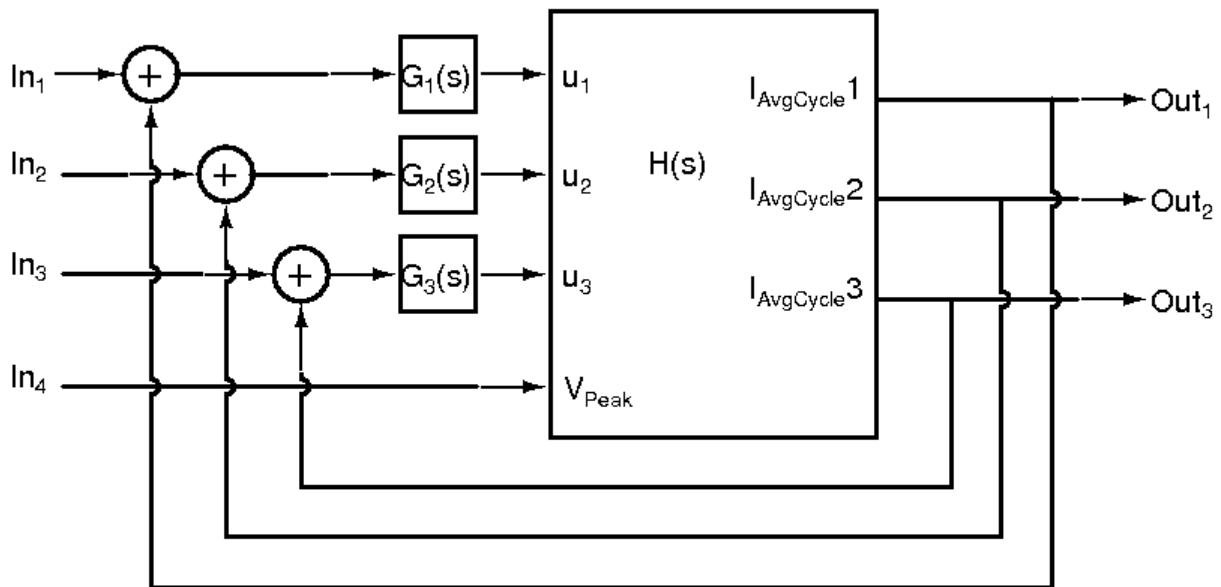


Figure 21 – System with Individual SISO Controllers

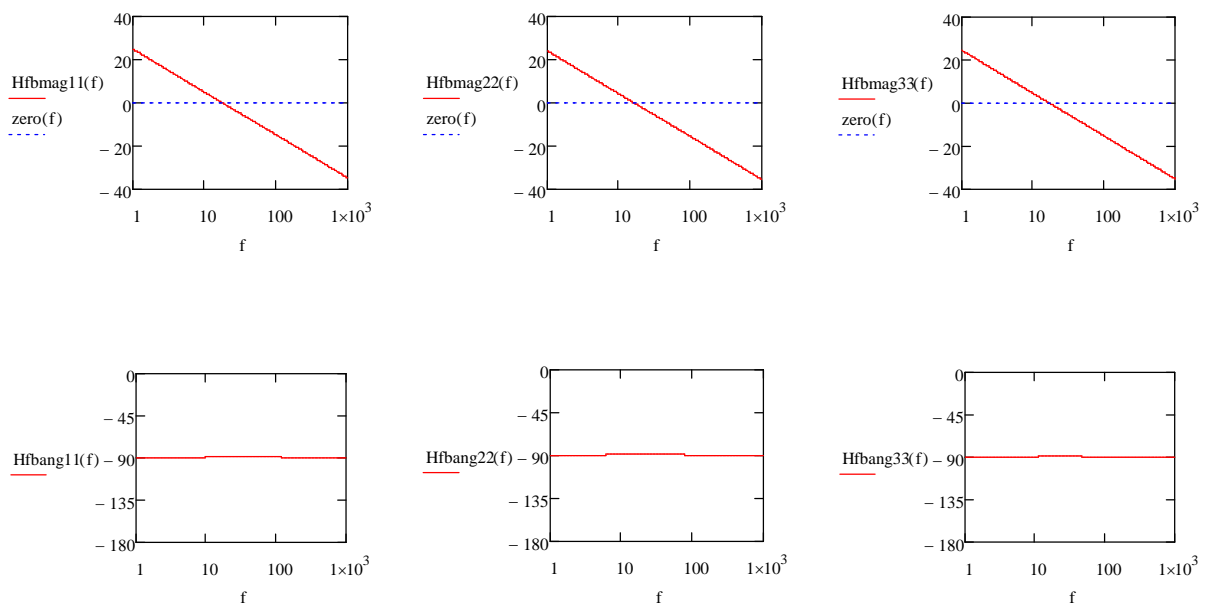
$H_{1,1}(s)$, $H_{2,2}(s)$, and $H_{3,3}(s)$, as Figure 20 shows, may practically be considered frequency independent gains. There is some dynamic phase shift near 30Hz, but this phase is negligible and can be dismissed. Using an integrating compensator with a gain is enough to stabilize these systems. For simplicity we will use the same controller for each of the three systems.

Because this is a PFC system we will need to have the controller reject frequencies above 120Hz^[32]. We will close the loop below 60Hz which is the Nyquist frequency.

The following compensator will be used to stabilize the system:

$$G(s) = \frac{1}{3000 \cdot s} \quad (89)$$

The loop gains for the diagonal systems are expressed by multiplying $G(s)$ and $H_{x,x}(s)$ where X represents each of the three channels. The Bode plots of the three diagonal loop gains are shown below:



(a) $G(s) \cdot H_{1,1}(s)$ Loop Gain

(b) $G(s) \cdot H_{2,2}(s)$ Loop Gain

(c) $G(s) \cdot H_{3,3}(s)$ Loop Gain

Figure 22 – Diagonal Loop Gains for Compensated System

The three systems above are clearly stable and responsive to reference inputs. It is prudent, however, to verify that that the complete closed loop system is stable based on its eigenvalues. In order to do this we must first create a new state space system, $\mathbf{K}(s)$, which

describes the initial system with the feedback loop. Figure 23 shows a block diagram of this implementation in a state space form with the initial system $H(s)$ outlined.

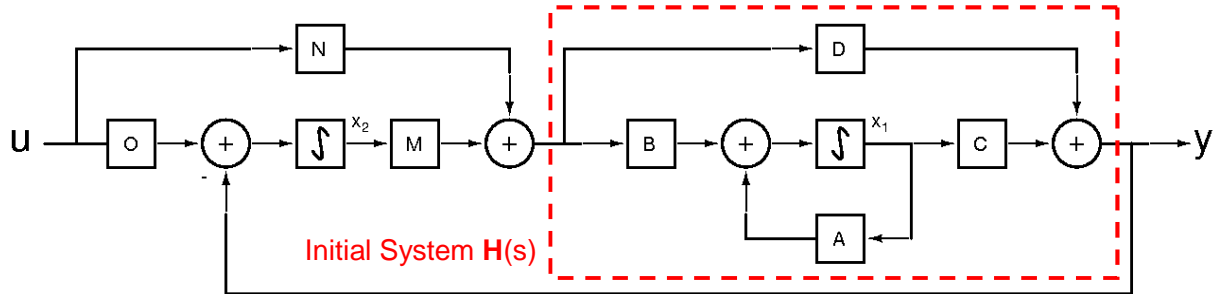


Figure 23 – Block Diagram of State Space System $K(s)$

$K(s)$ has two sets of state variables—one for the initial system and one for the compensator.

The compensator matrix gains are shown below in

$$\mathbf{M} = \begin{bmatrix} \frac{1}{3000} & 0 & 0 \\ 0 & \frac{1}{3000} & 0 \\ 0 & 0 & \frac{1}{3000} \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{N} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \mathbf{O} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

Table 4 – $K(s)$ System Matrices

\mathbf{M} is the compensator matrix gain, and holds the DC gain value for the compensator $G(s)$. \mathbf{N} allows the fourth input, V_{Peak} to pass directly through without an integrating term, as shown in Figure 21. Finally, \mathbf{O} passes the reference inputs through to the comparator and error stages. Using the diagram in Figure 23 we can come up with a new set of system equations representing the total system $\mathbf{K}(s)$:

$$\frac{d}{dt} \bar{x}_2 = \mathbf{O}\bar{u} - \mathbf{C}\bar{x}_1 - \mathbf{D}[\mathbf{M}\bar{x}_2 + \mathbf{N}\bar{u}] \quad (90)$$

$$\frac{d}{dt} \bar{x}_1 = \mathbf{A}\bar{x}_1 + \mathbf{B}[\mathbf{M}\bar{x}_2 + \mathbf{N}\bar{u}] \quad (91)$$

$$\bar{y} = \mathbf{C}\bar{x}_1 + \mathbf{D}[\mathbf{M}\bar{x}_2 + \mathbf{N}\bar{u}] \quad (92)$$

Consolidating these into a pair of system equations yields the following:

$$\frac{d}{dt} \begin{bmatrix} \bar{x}_1 \\ \bar{x}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{BM} \\ -\mathbf{C} & -\mathbf{DM} \end{bmatrix} \cdot \begin{bmatrix} \bar{x}_1 \\ \bar{x}_2 \end{bmatrix} + \begin{bmatrix} \mathbf{BN} \\ \mathbf{O} - \mathbf{DN} \end{bmatrix} \cdot \bar{u} \quad (93)$$

$$\bar{y} = [\mathbf{C} \quad \mathbf{DM}] \cdot \begin{bmatrix} \bar{x}_1 \\ \bar{x}_2 \end{bmatrix} + [\mathbf{DN}] \cdot \bar{u} \quad (94)$$

Finally, we solve for the eigenvalues of the new A matrix:

$$\bar{\lambda} = \begin{bmatrix} -276 \\ -170 \\ -103 \\ -114 \\ -82.7 \\ -82.7 \end{bmatrix} \quad (95)$$

All eigenvalues are negative and therefore the system is stable.

This reversed sequence MIROF converter is the system which we intend to implement and test against a standard solution. Above we have proven that our system is stable and controllable, and we have determined what compensation will be necessary. We also discussed the tradeoffs between a fixed time and fixed ratio switch sequencing scheme, and explained the benefits of using a fixed ratio reversed sequence every other switching cycle.

Chapter 3. Circuit Implementation

3.1 General Schematic

The generic circuit for the MIROF topology is shown in Figure 24. A complete schematic is included in Appendix A. Also shown below in Figure 25 is a photograph of the implemented light driver with LED load attached.

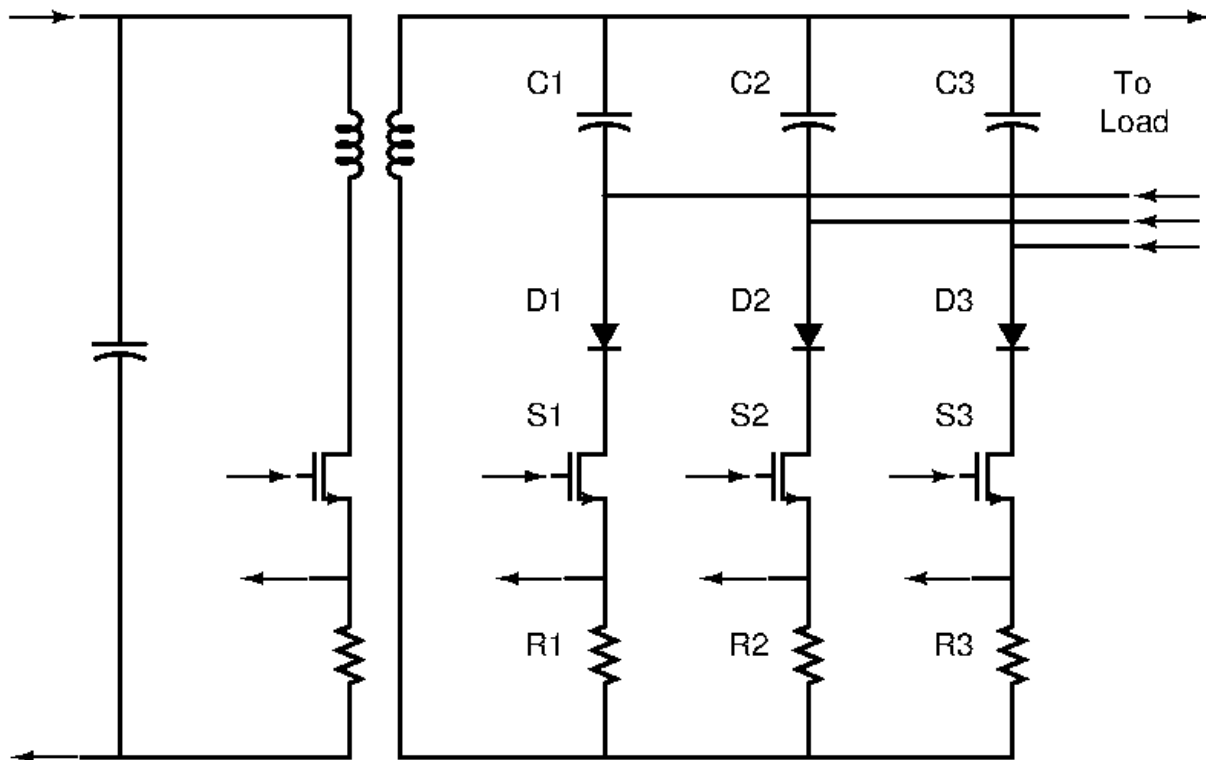


Figure 24 – MIROF Topology

Based on our system model there are several support circuits that we will need in order to implement this topology. For instance, a microcontroller or DSP would be the simplest way to realize the matrix gains needed for the control algorithm, and digital controllers are common in SIMO applications^{[33]-[36]}. Gate drives and auxiliary power supplies are also necessary and are typical for most power electronics circuits.

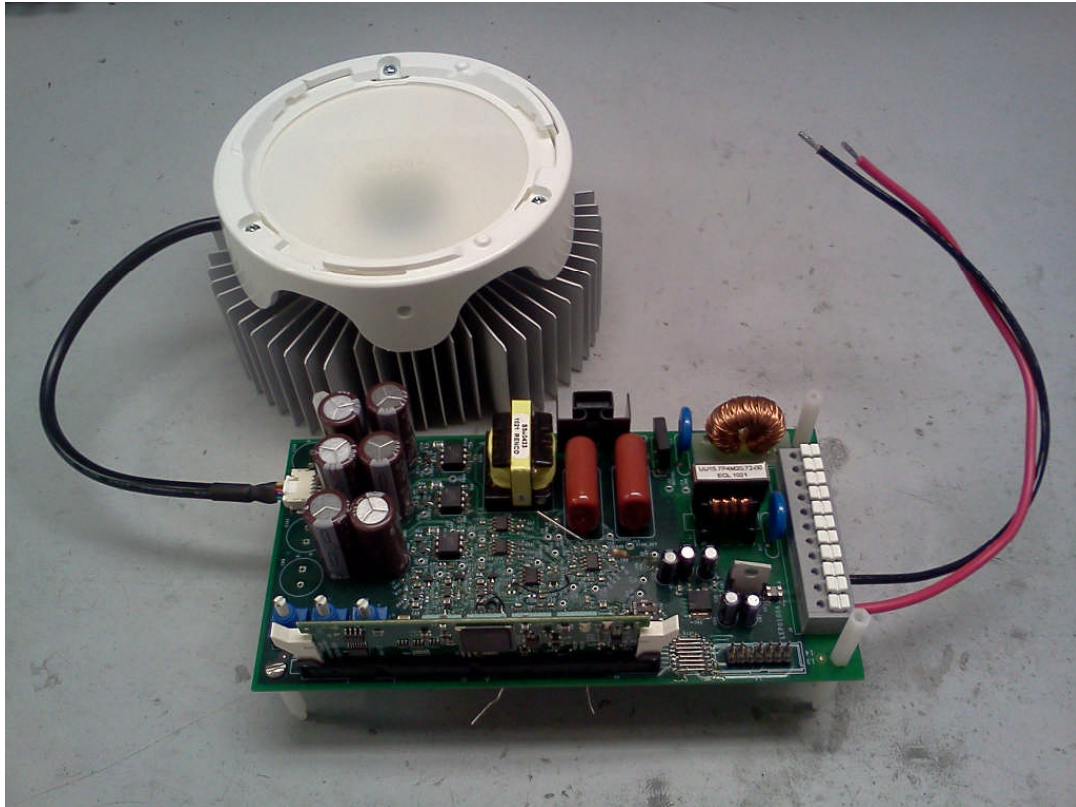


Figure 25 – Photograph of Implemented Circuit

3.2 String Current Measurement

Beyond these circuits we will also need a circuit that will allow us to read the average cycle current in each of the LED strings. This is the fundamental output of our system, and we need to be able to estimate it in order to assign a reference input and close the loop around it.

To begin, we will refer to Figure 24. It is safe to assume that the net current through capacitors C_1 , C_2 , and C_3 is zero over one half line cycle of the input. This must be true because we are controlling for constant current through our load, and the load current is directly affected by the capacitor voltage. Therefore if there is no change in the load current then there must be no change in the capacitor voltage, and hence no net current flowing through the capacitor. If capacitor net current is zero, then by Kirchhoff's law the net current through the load must be equal to the net current through switches Q_1 , Q_2 , and Q_3 . Therefore, the average

cycle current may be determined by measuring the current (or voltage) across resistors R_1 , R_2 , and R_3 , and averaging over the line cycle.

Finding the average can be a matter of filtering or integration. In this case the average current is being measured over relatively long time periods (8.3ms), and would require accordingly large electrical components. For instance, an RC filter with a time constant of 83ms (achieving a 10X attenuation at the half cycle frequency) and an R value of 10k Ω would require a capacitor of 10 μ F. This value is close to being inconveniently large, and capacitors of this value may be difficult to procure.

Another problem with filtering is the loss of dynamic range. Voltages across the sense resistors will be fairly small (less than 500mV for a 1 Ω resistor) and will be difficult to measure accurately with a standard A/D converter.

The alternative to filtering is integrating the current. The average of any signal may be achieved by integrating it and then dividing the result by the total time of integration (this style of control is sometimes referred to as "charge control" and can be used in a slightly different implementation in power electronics systems to improve the dynamic performance of some converters^{[37]-[40]}). For systems with a constant sampling time, the division may be represented by a constant gain factor. Our system for instance is expected to operate on 60Hz power systems. This represents a good system with which to use an integrator.

The last benefit of integration is that it requires that only one sample be taken per half line cycle; indeed, it is difficult to sample any faster with a standard PFC. A single sample, assuming our integration time is constant and accurate, will give us exactly the average current over the period in question. Filtering will give a good approximation, but the filtered output of a sinusoidal wave will always be sinusoidal. Sampling at the wrong time may give you a reading at the peak or trough of the waveform and may result in a corresponding offset.

Based on these arguments an integrating average current detector was chosen for this design. The circuit diagram is shown below in Figure 26.

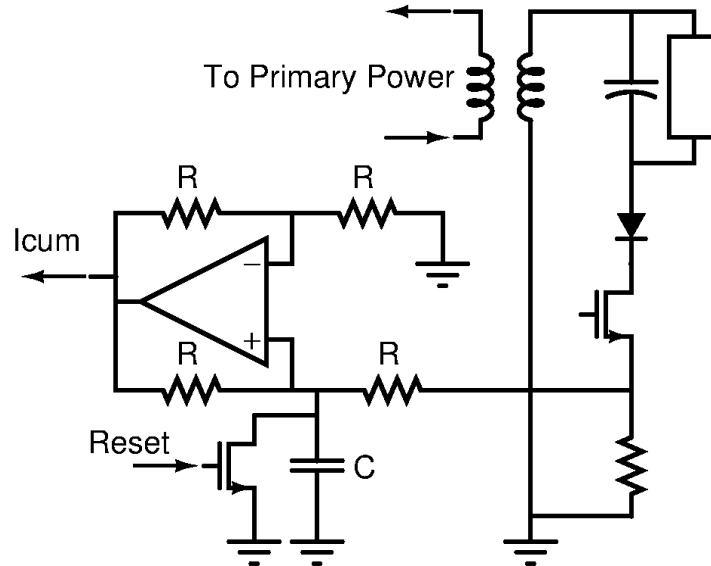


Figure 26 – Current Integrating Circuit

A reset is necessary because without it the circuit will integrate positive current until the amplifier saturates. The microcontroller should issue a reset pulse after the integrated current is read and before the next integrating cycle begins.

One last point on the integrator circuit: it is, in fact, possible to sample faster than once every half line cycle. Consider Figure 27 below:

The time average value of the load capacitor voltage is shown as a dotted line. The points at which the instantaneous voltage crosses the time average value are indicated with a heavy dot. Since the instantaneous voltage is the same at each of these points, we know that the net current into the capacitor between these points is zero.

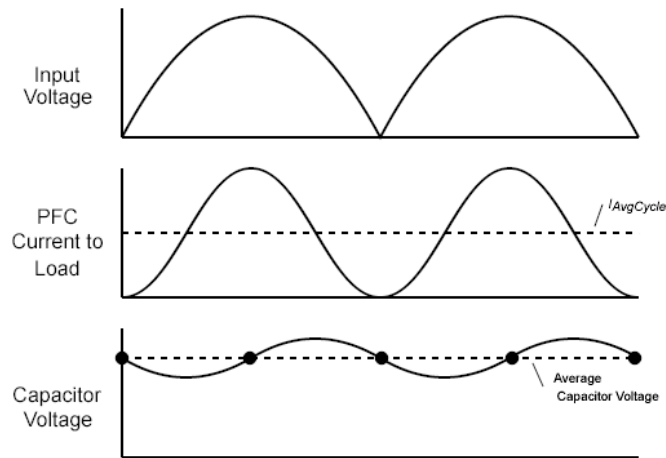


Figure 27 – PFC Waveforms

Again by Kirchhoff's law, we know that over these periods the net current through the switch and through the sense resistor R must be equal to the current through the load. Therefore, by sampling the integrated current across R at each of these points will give us our load current scaled linearly by R and one quarter of our line period.

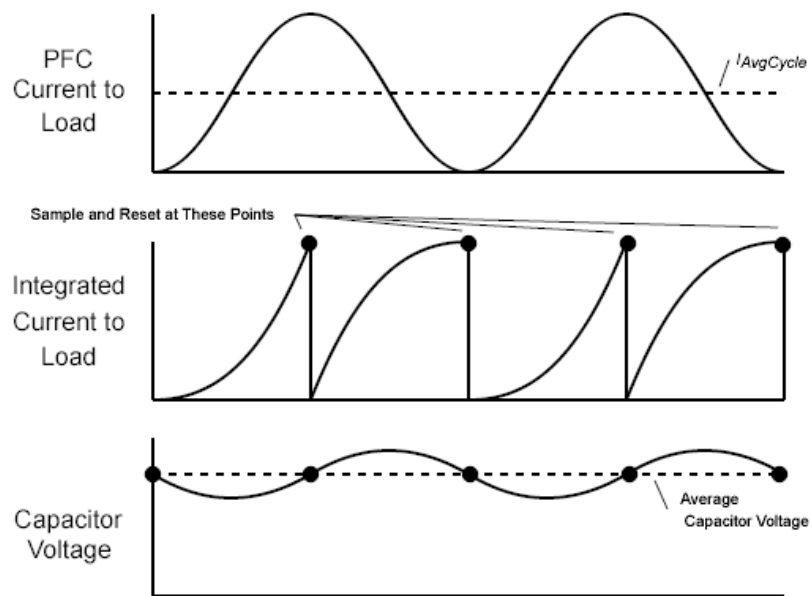


Figure 28 – PFC Waveforms with Integrated Load Current

Above, Figure 28 shows the integrated PFC current to load with the sampling points indicated. Directly after each sample the microcontroller resets the integrator circuit, pulling the output down to zero.

3.3 Overvoltage Protection

While it is not necessary to directly control the voltage across the load capacitors, it is necessary to make sure they are not charged to dangerously high voltage levels. This is especially true since it may not be uncommon to see light configurations where the driver and the light are in separate enclosures connected by a harness. If the harness were to become disconnected or severed then the controller would simply keep driving current into the capacitor with no load to draw it away. The capacitor would simply charge to higher and higher voltages until it failed.

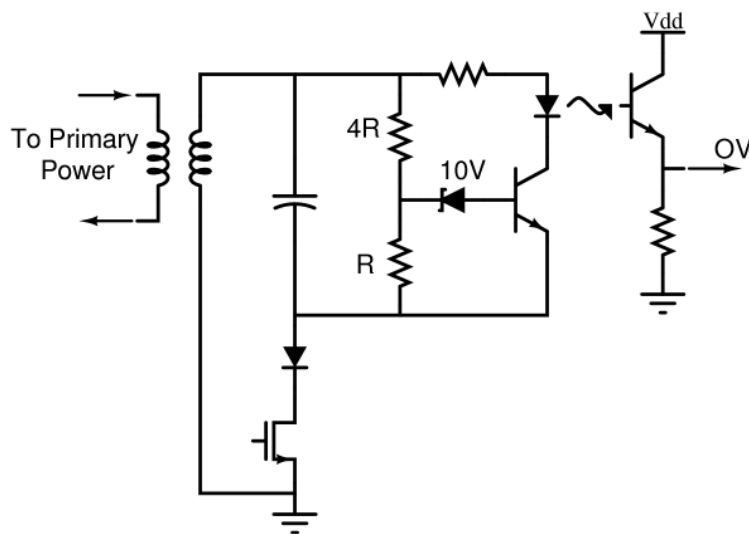


Figure 29 – Overvoltage Protection Circuit

An OV circuit here is tricky because the capacitor voltages are not referenced to ground. Further, the “ground” reference for the load is continually changing as the switches cycle through a sequence. Based on these difficulties I decided that the best option was to use an

isolated detector. I also decided to allow each of the overvoltage circuits to report separately. This would allow the greatest flexibility in servicing the error, potentially allowing the unit to drive the two remaining strings if one were to become open.

The circuit for the overvoltage protection is shown in Figure 29

3.4 Phase Detection

PFC circuits often require a sinusoidal reference with which to shape the input current. In most cases this sinusoidal reference is the input voltage itself. In the case of our converter however, there is no need for a sinusoidal reference. Since the converter is to run in DCM mode, PFC may be achieved simply by turning switch Q_0 on for the same time during each switching cycle. Equation 96 shows the formula for average current into the input of a flyback converter.

$$I_{Avg} = V_{In} \cdot \frac{T_{On}^2}{2 \cdot T_S \cdot L_P} \quad (96)$$

As the equation above shows, I_{Avg} is inversely proportional to T_S , the switching period, and L_P , the primary inductance of the transformer. Both of these are system characteristics and remain constant at all times. I_{Avg} is directly proportional to V_{In} , the input voltage, and the square of T_{On} . If T_{On} remains constant throughout an entire line cycle, then I_{Avg} will be a constant multiple of V_{In} , and therefore will be sinusoidal.

Based on the calculation above we know it is not necessary to measure the voltage directly. It *is* necessary, however, to know the relative phase of the input voltage. This is true for two reasons: first, based on the description of the integrating current sense circuit we know that it must be sampled and reset at specific phase angles of the input voltage waveform. If these measurements are not taken at the correct instant, then there is a risk that the samples will not accurately reflect the true integrated LED current (since the capacitor may have absorbed some of the converter output current).

Second we know that the average-by-integration method is accurate for a fixed frequency. If, on the other hand, there is any frequency drift on the line voltage or if the circuit is expected to work with foreign power grids then there must be some accommodation in the circuit to measure the input line frequency. This is necessary both to adjust the current sample time and to apply an offset to the result (so that the average value of the waveform is determined for the proper integration period).

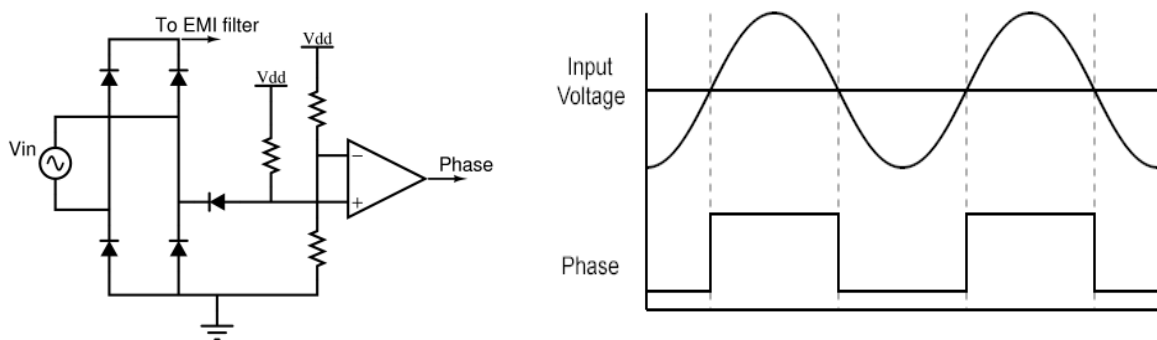


Figure 30 – Phase Detect Circuit

Instead of scaling the input voltage and feeding the result into an A/D converter on the microcontroller we might prefer to turn the phase waveform into a digital signal instead with the rising and falling edges representing the zero crossings at 0 and 180°. The reasons for this are straightforward—decoding a digital signal is much simpler for a microcontroller than interpreting an analog signal. Also, a digital signal may drive interrupt logic, and therefore the options for handling a dynamic digital line are more flexible than that for an analog line.

The circuit below in Figure 30 shows a circuit that accomplishes the goal of turning the input voltage waveform into a digital phase waveform.

3.5 Zero Current Detection

The system described in Section 2.8 uses the terms d_1 , d_2 , and d_3 as inputs. These terms represent portions of the secondary conduction time which together sum to 100%. Our system

derives the levels for these inputs with the compensator, and then must drive the converter with them.

In order for the controller to drive these parameters correctly it first must know the secondary conduction time. Once this has been determined the controller drives switches Q_1 , Q_2 , and Q_3 for a period of time equal to d_1 , d_2 , and d_3 multiplied by the secondary conduction time, respectively.

What this means is that the secondary conduction time must be measured. It may be possible to observe this value with a linear system, however, such complicated systems as observers are preferably avoided in applications where cost is a primary design consideration. This is because observer systems tend to require expensive microcontrollers or DSPs.

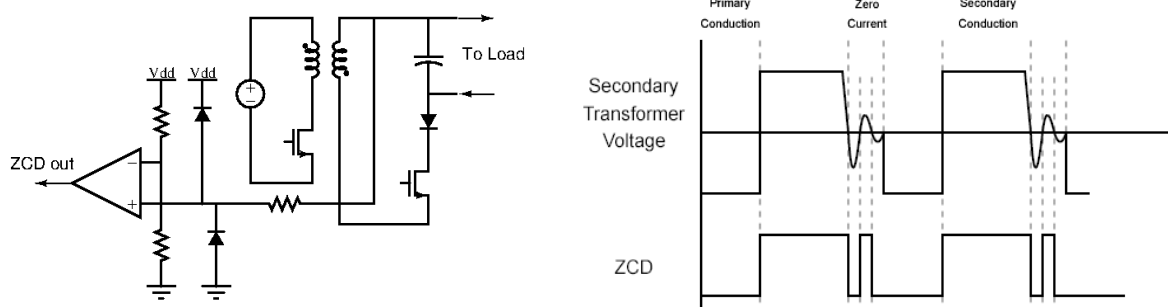


Figure 31 – Zero Current Detect Circuit

The secondary conduction time begins when the primary switch turns off and ends when the transformer is depleted of energy. Sensing the point at which the transformer depletes to zero energy (or current) is straightforward and can be accomplished with a standard circuit called a Zero Current Detect (ZCD). A typical ZCD is shown in Figure 31.

To measure the secondary conduction time, the controller may simply begin a timer when the primary switch turns off and stop the timer at the next edge of the ZCD output. This circuit may also be implemented partially within the microcontroller if there is a comparator available with a satisfactory switching delay.

3.6 Microcontroller Selection

Typically great care must be taken by a designer to make sure that she selects a microcontroller that is suitable to the application. The most common tradeoffs in these systems are speed and feature count versus cost. Since our application is driven primarily by cost, we should make sure that we select a microcontroller with only as many features as are needed and which runs at the lowest acceptable speed.

The first known requirement is that the controller must be capable of driving 4 FETs, which means that it should have four instances of a PWM control peripheral. These are standard features in microcontrollers, and are typically available in inexpensive devices. Unfortunately it can be difficult to find reasonably priced controllers which have four PWM control blocks.

The second requirement relates to switching time of the converter. We would like this converter to be comparably sized to currently available solutions. Flyback AC/DC supplies in LED lighting applications can have typical switching frequencies of 75-150kHz, and since switching frequency is a major driver for converter size we will target a switching speed in the middle of this range—100kHz—as the desired frequency.

We will (somewhat arbitrarily) also require that at this switching frequency our PWM controller maintains at least ten bits of resolution. This is chosen because lower resolutions will result in visible discretization of light levels of the final product.

The ten bits of resolution correlates to a PWM step size of approximately 10ns, as shown in Equation 97:

$$T_{Step} = \frac{T_{Switch}}{2^{10}} = \frac{10\mu s}{1024} = 9.77ns \quad (97)$$

Where T_{Step} is the PWM step size and T_{Switch} is the PWM switching time (the reciprocal of the switching frequency 100kHz).

A step size of 10ns corresponds to a PWM clock rate of 100MHz, which is extremely fast for most microcontrollers. This clock rate may only be available in a DSP solution.

The microcontroller must at a minimum also have 5 digital inputs with interrupt support for 2 of them, and 3 input channels for an A/D converter. These will unquestionably be available for any part meeting the requirements above.

After evaluating all the above requirements I selected the TMS320F28335 Delfino DSP by Texas Instruments for this project.

3.7 Miscellaneous Hardware

The only hardware left to be specified for this project is auxiliary, support, and debug circuitry. The hardware below was chosen as follows:

- Gate Drivers: Standard dual low-side drivers were chosen to drive the FET gates
- Auxiliary Power: For the demonstration unit auxiliary and control voltages—18V, 5V, and 3.3V—were derived from an external source. 18V was an input and 5V and 3.3V were sourced from linear regulators connected to 18V.
- DIP Switches: Two DIP switches were added and connected to digital inputs of the DSP for debug purposes.
- Potentiometers: Three potentiometers were configured to divide 3.3V and report to A/D inputs on the DSP. These were also added to allow the user external access to control string currents and light color.

A full system schematic is available in Appendix A.

Chapter 4. Embedded System Software

4.1 PWM Controllers

The most important element of the embedded software for this project is clearly the implementation of the PWM controllers. This is due to the fact that we are using such a novel switching algorithm: the reverse sequence described in Section 2.8.

The first and most obvious option for coded PWM implementation is to manually flip the sequence of secondary PWMs after each switching cycle. This is inefficient to say the least, as it requires mandatory action by the microcontroller every switching period ($10\mu\text{s}$).

As it turns out, however, there is already a requirement that the controller update the PWM pulses on a regular basis. The inputs d_1 , d_2 , and d_3 of our converter model represent duty cycles of the secondary switches. The absolute timing of the switches depends on these inputs and the secondary conduction time, $T'(s)$. Since $T'(s)$ changes constantly with the input line voltage, so does the timing of the switches Q_1 , Q_2 , and Q_3 . This requires us to continually update the PWM counter for the secondary switches, although, the input line voltage changes very slowly with respect to the switching period (there are over 1600 switching cycles during a full input line cycle), so it may not be necessary to update the secondary switch counters every switching cycle. We may be able to get away with changing the counters every 3rd or 10th cycle for instance.

Since we may have no other reason to update the switch counters every cycle, we prefer not to burden the processor with the task of manually flipping the sequence each cycle. Besides, there is another reason to avoid this: Some microcontrollers, and specifically the DSP we have chosen, have a feature that buffers a change in the PWM counter. This feature is intended to prevent runt pulses by ensuring a new count/compare value is loaded at the same point in the PWM sequence each time it is updated. This buffering adds a 1-switching-cycle

delay to any updates and is not conducive to allowing rapid “toggle” updates that occur every cycle.

Thus we would prefer a solution which we can set once and which will produce alternating switching cycles properly after that given a constant $T'(s)$.

Below Figure 32 shows a DSP implementation that could yield the results we are looking for. This utilizes an “up-down counter” method of generating PWM switches, where a digital counter is compared to a reference value (represented by CmpA and CmpB in the figure below), and the result of the comparison determines the state of the PWM output.

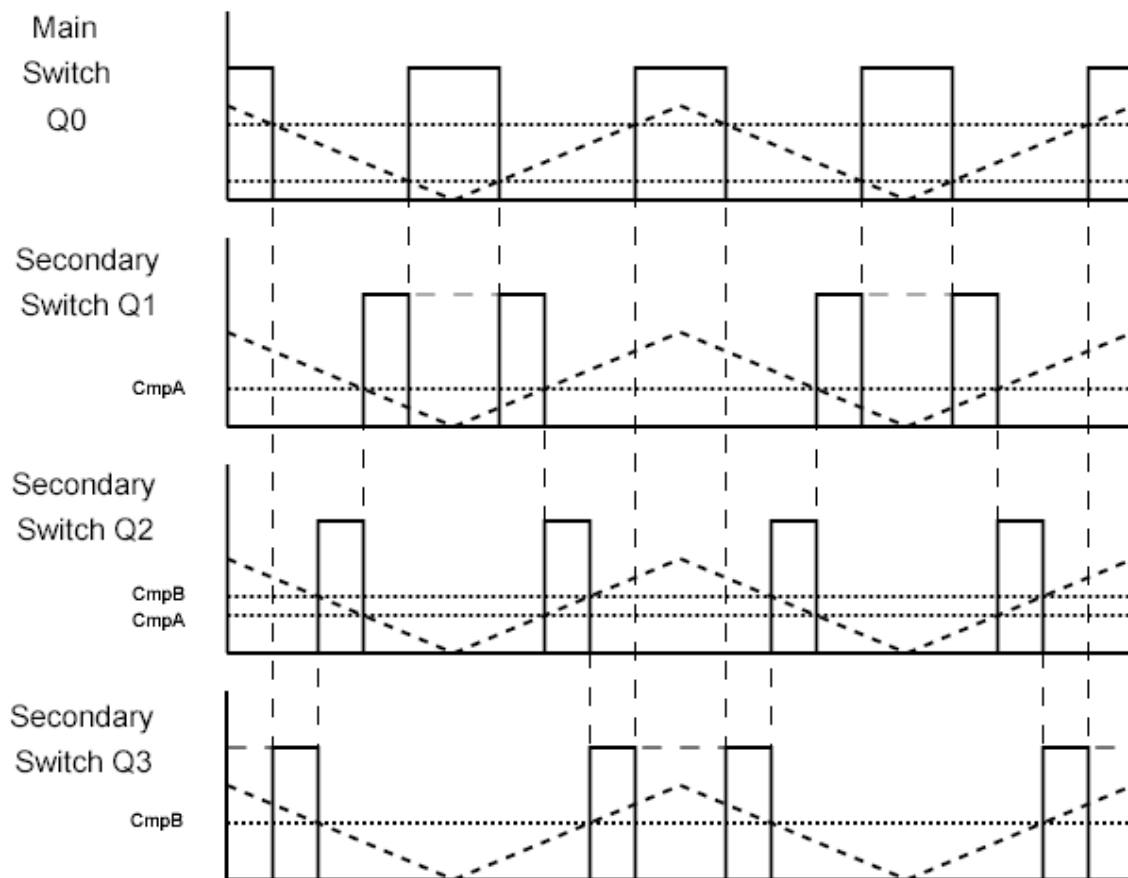


Figure 32 – DSP Controlled Switch Timing

The reader may note several points from Figure 32: first, note that secondary switch Q1 and secondary switch Q3 do *not* need to be opened or turned off during the time that primary switch Q0 is conducting. This is true because during primary conduction time the voltage on the transformer secondary will be negative and will reverse bias the secondary diodes, preventing current from flowing. Keeping Q1 and Q3 on during these times will simplify the switch sequencing.

Second, note that the main switch Q0 and the secondary switch Q2 both have *two* reference values to which the PWM counter must be compared. This is not an option in all microcontrollers, and must be listed as a specific feature requirement in our selection of digital controllers. Fortunately, the TMS320F28335 is capable of this type of PWM operation.

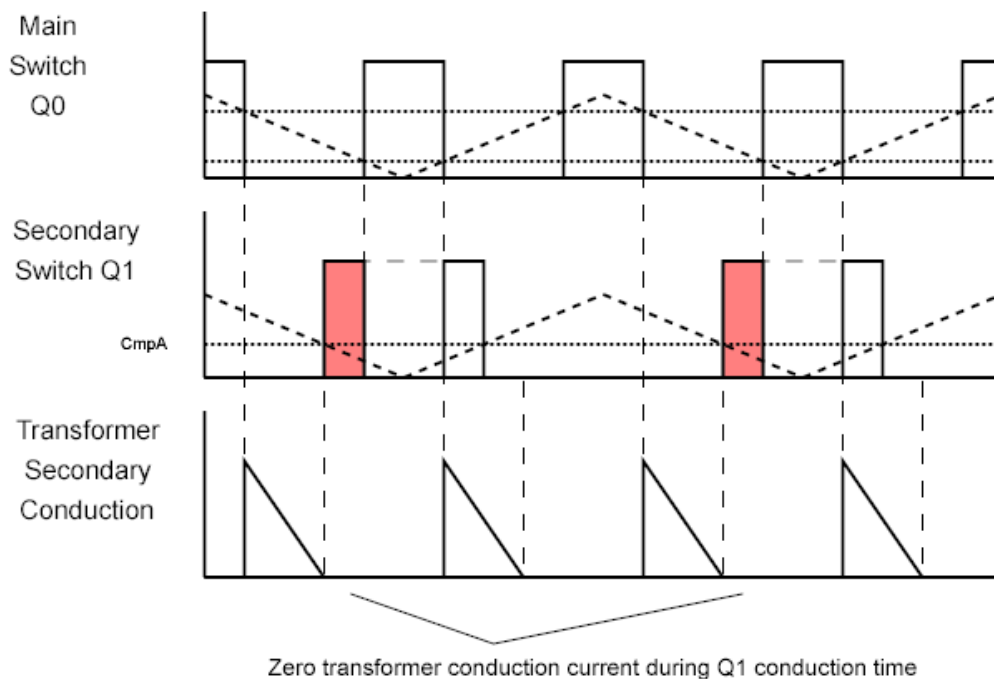


Figure 33 – Effects of DCM Conduction on Alternated Switch Timing

Unfortunately, using this sequencing algorithm is not as simple as it initially looks. Since the converter is running in DCM mode the transformer will source current for only a portion of the

time between the opening and subsequent conduction of switch Q0. This will necessarily interfere with the conduction of at least one of the secondary switches (and eventually all of them as the input line voltage moves from its peak to the zero crossing) as shown in Figure 33.

Such a switch configuration violates the assumptions of our model, since the time of current conduction for each switch must be identical in the forward phase and reverse phase.

Therefore we must include some accommodation in the timing algorithm for the effect of dead time in secondary conduction.

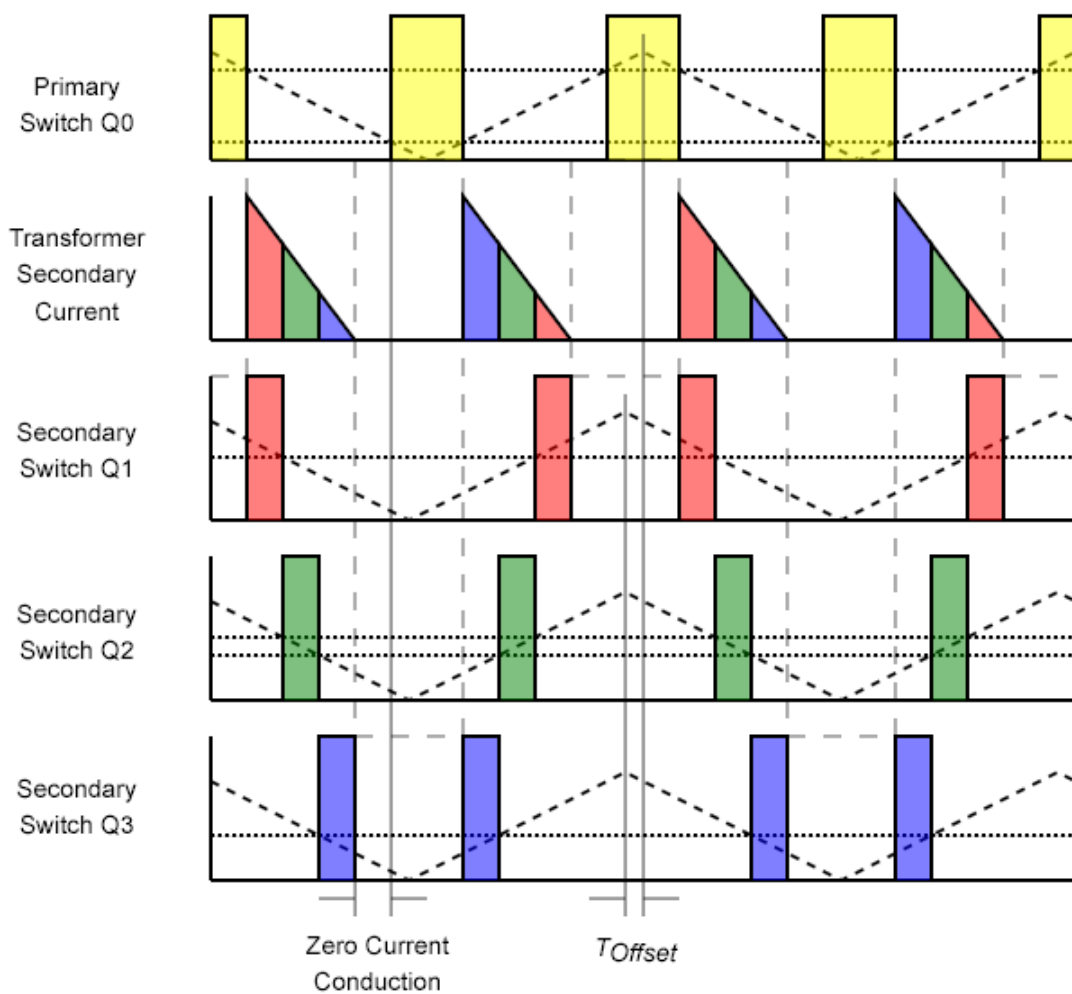


Figure 34 – Switch Timing with Offset

Figure 34 shows a new switch timing diagram which incorporates a phase shift between the primary and secondary switch counters. In this example the secondary switch counter leads the primary switch counter by the value of T_{Offset} .

Figure 34 shows that with the correct T_{Offset} switches Q_1 , Q_2 , and Q_3 not only can all conduct on the forward and reverse sequence, but the timing for each switch can be equal on the forward and reverse sequences as well. Determining the correct offset time is simply a matter of solving identities in the figure above. For switch Q_1 and Q_3 we want the on transition and the off transition to occur at the same reference—CmpA and CmpB respectively. This means that the time between the switch on transition and the zero (or max) count is the same time between the zero (or max) count and the off transition.

Based on this requirement and Figure 34 we define T_{Offset} with the following equation:

$$T_{On} + T_{Zero} = 2 \cdot (T_{Offset} + \frac{1}{2} \cdot T_{On}) \quad (98)$$

Simplifying and solving for T_{Offset} yields:

$$T_{Offset} = \frac{1}{2} \cdot T_{Zero} \quad (99)$$

The majority of these parameters and the sequencing characteristics may be selected in the system setup portion of the code. The conduction times for switches Q_0 through Q_3 and the offset time T_{Offset} must instead be updated regularly—every single switching cycle or perhaps as infrequently as every third switching cycle. This operation is described in the following sections.

4.2 A/D Sample Timing and Filtering

As described in Section 0, the controller must poll the voltage on the string current integrators four times every line cycle in order to accurately determine the LED string current. The sampling points must also be at specific phase angles relative to the input voltage

waveform. These requirements indicate that the controller must lock phase to the input voltage waveform using a form of digital PLL.

Attempts to implement a closed loop PLL in software were unsuccessful, so instead a simpler method was used. The controller simply measures the time of a full line cycle and then divides it by four. This then becomes the new sampling period, and the first sample is taken at the time that the new line period begins (at the zero crossing).

Two interrupt subroutines are used to accomplish this. `Forty_ms_counter_ISR()` is a function that is called every 40µs and which times the A/D samples. `Sync_AD_ISR()` is a function that is called once each line cycle when the Phase Detect circuit indicates a positive zero cross. `Sync_AD_ISR()` times the line period by counting the number of times `Forty_ms_counter_ISR()` is called in between zero crossings. `Sync_AD_ISR()` then divides the value of the full line period by four to find the A/D sampling period, and the first sample is taken immediately.

Once the A/D sample is completed it will be used as an input to the feedback compensator in the system. The Since A/D sampled systems are typically susceptible to noise it would be to our great benefit to filter the samples before they are passed to the compensator.

There are two inputs to the system that are measured by the A/D converter: the current sense input that represents the LED string current, and the reference input that generates the target current from a potentiometer. The latter is simple to filter since we expect it to change fairly slowly with respect to the line frequency. The filter in this case can have a heavy time constant which will ensure a very smooth output.

The filter is implemented as shown in Equation 100, where z^{-1} represents a z-domain single sample time delay.

$$Reference = Reference \cdot z^{-1} - \frac{Reference \cdot z^{-1}}{32} + \frac{ADsample}{32} \quad (100)$$

In this equation *Reference* is a 16 bit value. The A/D converter on the DSP that we've chosen has a resolution of only 12 bits, so a full count of *ADsample* is 16 times smaller than a full count of *Reference*. Note that in the implemented code *ADsample* is only divided by two in order to account for this offset.

Equation 100 represents a first-order filter with a time constant of 32 samples, or 133ms in a 60Hz system. This means it will take more than a half second to settle to 5% in response to a step input, which is a detectable delay to the human eye. This should be acceptable since the transition is smooth, however less sampling may be used to improve response time by the system.

Filtering the current sense node, on the other hand, is more difficult. We would prefer to filter as little as possible in order to allow us to close the loop at a high frequency. This is preferable because we don't want a line disturbance to have a visible effect on the light output.

Sample 1	Current Sense 1
Sample 2	Current Sense 2
Sample 3	Current Sense 3
Sample 4	Current Sense 1
Sample 5	Current Sense 2
Sample 6	Current Sense 3
Sample 7	Current Sense 1
Sample 8	Current Sense 2
Sample 9	Current Sense 3
Sample 10	Current Sense 1
Sample 11	Current Sense 2
Sample 12	Current Sense 3
Sample 13	Reference 1
Sample 14	Reference 2
Sample 15	Reference 3
Sample 16	No Sample

Table 5 – A/D Sampling Order

The A/D converter on the TMS320F28335 is capable of taking up to 16 samples in rapid succession. Our design requires only 6 samples to be taken, and therefore the unused samples may be employed to help guarantee a stable value of the current sense. For instance, multiple samples of each current sense line may be taken as shown below in Table 5. By taking four

samples of each current sense line and averaging them, a degree of filtering can be achieved with no delay at all.

There is another thing that makes the sampling of the current integrator circuits difficult. Due to the shape of the current integrator output waveform it is highly sensitive to the timing of the A/D sampling. A slight shift in A/D sample timing at the peak of the input waveform can create a large shift in the output voltage of the integrator at the time of the sample. An example of this is shown below in Figure 35.

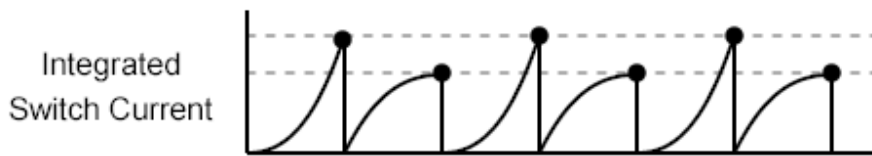


Figure 35 – Irregularity in Current Sense Integrator Sampling

In order to minimize the impact of this cycling the latest sample should be averaged with the sample preceding it. After this average is taken then the result can be filtered as normal. The process of averaging and filtration is outlined in Equations 101 through 103.

First the four 12-bit samples are added together to create a 14-bit average.

$$AverageSample = Sample1 + Sample2 + Sample3 + Sample4 \quad (101)$$

Next, the sample average is added together with the previous average to create a 15-bit time-averaged sample.

$$TimeAverage = AverageSample + PreviousAverage \quad (102)$$

Finally, the time averaged sample is filtered in a first-order filter with a time constant of one sample to achieve light filtering and to raise the final result to 16 bits.

$$SampledResult = SampledResult \cdot z^{-1} - \frac{SampledResult \cdot z^{-1}}{2} + TimeAverage \quad (103)$$

4.3 Input Conditioning and Closed Loop Control

The model of Section 2.9 and 2.10 require implementation of control laws and an “input conditioner” in the microcontroller. Most microcontroller control loops also require signal conditioning of the input signals (in our case the reference and current sense inputs—covered in the previous section) as well as the output signals (the PWMs to the primary and secondary switches—covered in Section 4.1).

A typical microcontroller feedback loop for our system might look like the diagram below in Figure 36.

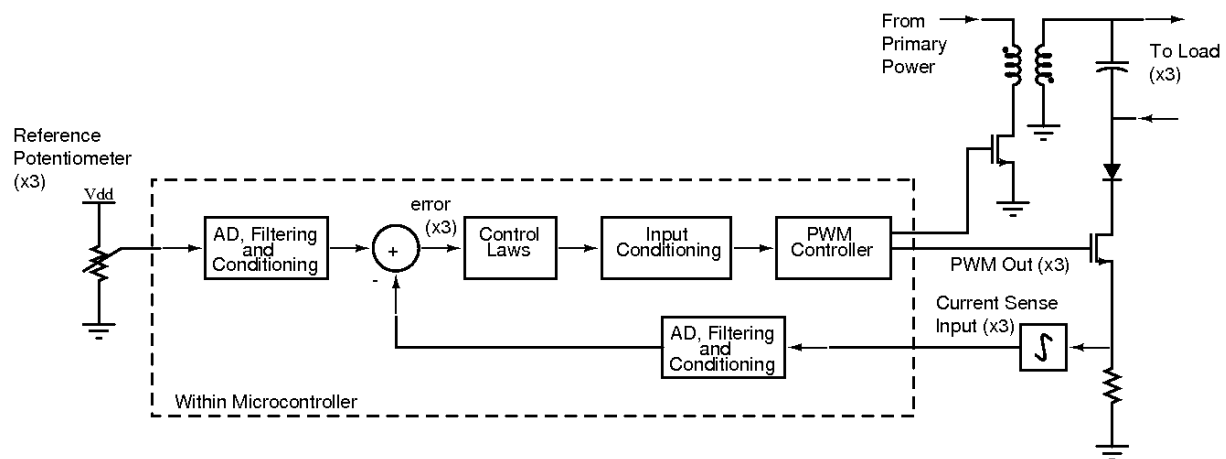


Figure 36 – Microcontroller Feedback Diagram

Now that we have the inputs to the system, we can use them to calculate the error and the loop response. Based on the compensator model in Section 2.10, we can create a loop gain compensator encoded in the microcontroller. Before implementing the compensator in code, we must determine the conversion factors between the real world values and their bit-wise values in the microcontroller.

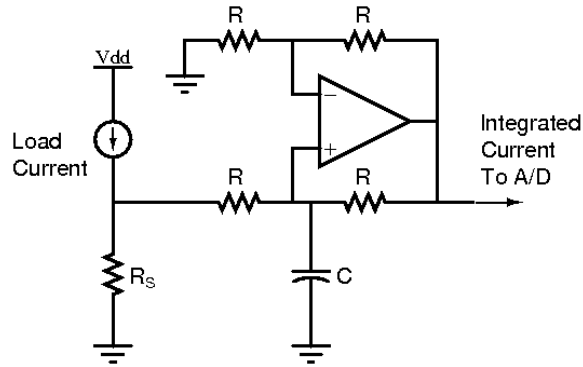


Figure 37 – Current Integrating Circuit

Figure 37 shows the current integrating circuit from Section 0. This circuit can be shown to have the following I/O characteristic:

$$V_{Out} = \frac{2 \cdot R_s}{R \cdot C} \cdot \int I_{Load} \cdot dt \quad (104)$$

Since we know the time of integration, and we're primarily interested in the average load current, the following simplification is possible:

$$V_{Out} = \frac{2 \cdot R_s \cdot T_{Sample}}{R \cdot C} \cdot I_{Avg} \quad (105)$$

Where I_{Avg} is the time average of current I_{Load} , and T_{Sample} is the A/D sampling period, which represents the time of integration between samples. The DC I/O characteristic can then be determined as shown below:

$$\frac{V_{Out}}{I_{Avg}} = \frac{2 \cdot R_s \cdot T_{Sample}}{R \cdot C} = 7.04 \frac{V}{A} \quad (106)$$

Where:

$$\begin{aligned} T_{Sample} &= 4.166ms & R_s &= 0.51\Omega \\ R &= 6.04k\Omega & C &= 0.1\mu F \end{aligned}$$

Next the A/D conversion factor must be determined. A full count of 16 bits represents the maximum A/D input voltage of 3.3V

$$ADfactor = \frac{2^{16} - 1}{3.3V} = 19860 \frac{bits}{V} \quad (107)$$

A conversion from average current to microcontroller variable is simply the combination of the two:

$$InputFactor = 7.04 \frac{V}{A} \cdot 19860 \frac{bits}{V} = 139700 \frac{bits}{A} \quad (108)$$

The output conversion factor is simpler, requiring only the PWM clock speed (150MHz).

$$OutputFactor = 150 \cdot 10^6 \frac{bits}{s} \quad (109)$$

The compensator for this system is shown in Equation 89, and is reproduced below for convenience:

$$G(s) = \frac{1}{3000 \cdot s} \quad (110)$$

This means an error of 1A should integrate to a primary switch on time of one-three-thousandth of a second after integrating for a period of one second. In order to accomplish this, we need a scaling factor: k . The samples are scaled and cumulatively summed in order to perform the integration, and since there are 240 samples per second, the total cumulative sum is simply the average sample times 240.

$$1A \cdot \frac{139700 \frac{bits}{A}}{k} \cdot 240 = \frac{1}{3000} \cdot s \cdot 150 \cdot 10^6 \frac{bits}{s} \quad (111)$$

Solving the above equation for k yields:

$$k = 671 \quad (112)$$

Using this gain factor in the closed loop feedback of our controller will give us a series of equations as shown below:

$$\text{Error} = \text{Reference} - \text{SampledResult} \quad (113)$$

$$\text{State} = \text{State} \cdot z^{-1} + \frac{\text{Error}}{671} \quad (114)$$

These equations must be performed for each of the three reference/output currents.

Finally, the input conditioning circuit must be added to complete the code. This is the system described in Section 2.6 which we implemented to decouple the non-diagonal terms in the DC gain matrix. The main terms of the conditioning circuit described in Equations 72 and 73. They are repeated below for convenience:

$$T_{On} = u_1 + u_2 + u_3 \quad (115)$$

$$d_x = \frac{u_x}{u_1 + u_2 + u_3} \quad (116)$$

These equations are quite simple to implement and take almost exactly the same form in the code as they do in the system description. They are shown below:

$$\text{MainCount} = \text{State 1} + \text{State 2} + \text{State 3} \quad (117)$$

$$\text{ApercentOf Dprime} = \frac{\text{State 1}}{\text{MainCount}} \quad (118)$$

$$\text{BpercentOf Dprime} = \frac{\text{State 2}}{\text{MainCount}} \quad (119)$$

MainCount in Equation 117 above represents the on-time of the primary switch, and specifically is the number of 150MHz clock cycles that the primary switch conducts for. States 1, 2, and 3 are the integrator outputs solved in Equation 114 for each respective reference input.

ApercentOfDprime and *BpercentOfDprime* represent the on-time of secondary switches 1 and 2 as a percentage of the total secondary conduction time. The value for switch 3 is not necessary since it will always be what is left of 100% after switch 1 and 2 complete their conduction.

Once these two values are calculated they must then be multiplied by the secondary conduction time (or critical time) to yield the total switch conduction time.

4.4 Secondary Conduction Measurement and Switch Timing

`Load_secondary_on_times_ISR()` is a function that measures the secondary conduction time of each switching cycle and then calculates the secondary switch times for the next cycle. This function is called by the PWM interrupt service halfway through the conduction time of the primary switch. The function waits for the primary switch to end conduction and then simply waits for an indication from the ZCD circuit that the transformer has been depleted of energy.

The value of the PWM counter is stored at this point into a value named *CritCount*. *CritCount* is equal to *MainCount* (the on-time of the primary switch) plus the secondary conduction time. The variable name *dprimeCount* is used to represent the secondary conduction time.

$$dprimeCount = CritCount - MainCount \quad (120)$$

These values along with T_{Offset} , defined in Equation 99, may be used to find the secondary switch on-time values:

$$Account = MainCount + T_{Offset} + ApercentOfDprime \cdot dprimeCount \quad (121)$$

$$Bcount = Acount + BpercentOf Dprime \cdot dprimeCoun t \quad (122)$$

These values may then be loaded directly into the PWM control registers. If the PWM controllers have been set up as shown in Section Chapter 4, then the circuit will work as intended.

4.5 Frequency Regulation

The final element of controlling the circuit is placing a regulation loop around the input frequency. As mentioned in Section 0, our input voltage is expected to be a 60Hz sinusoid. We would prefer for this circuit to work for both 50Hz and 60Hz, however, and if we see a change in the input line cycle then it will cause our integrator input circuit to improperly calculate the average current.

The way to solve this problem is to apply a gain factor to the input reference that is proportional to the input line period. This will require a higher cumulative current from a circuit that is running at a lower frequency. The higher current accumulated over a longer period of time will yield the same average current as a lower cumulative current at a faster frequency.

Below is a code sample taken from the project:

```
// Account for Frequency
// -----
Freq_adjust = 139;
Freq_adjust = AD_delta/Freq_adjust;
Freq_target1 = Filtered_target1 * Freq_adjust;
Freq_target2 = Filtered_target2 * Freq_adjust;
Freq_target3 = Filtered_target3 * Freq_adjust;
```

This code shows the use of a gain factor, *Freq_adjust*, which is directly proportional to *AD_delta*. *AD_delta* represents one-quarter of the input line period, and is the value used to time the A/D samples. This code effectively creates a robust solution for regulating around the input line frequency.

Chapter 5. Results

Once the converter is implemented we need a metric by which to measure its suitability to our application. Since we are offering the MIROF converter as a low-cost alternate to the standard solution, it is reasonable to compare the two to see where the benefits and drawbacks lie. The standard used for comparison is the two-stage converter shown in Figure 5b. The following chapter focuses on comparing the cost, size, and performance of the standard two-stage solution with that of the MIROF converter.

5.1 Cost Comparison

The two systems which we intend to compare are similar in several ways. For instance, they are intended to power the same load and are presumed to have similar performance requirements such as for conducted EMI. Our cost comparison of the two systems will be based on the component delta between the two, and therefore common parts (EMI filter and load components: LEDs, harnesses, heatsink) will not be included.

The following parts have been removed from the BOM cost for the purposes of this comparison:

- EMI Components (common)
- Primary Power Components—Transformer, Rectifier Bridge, Primary Switch, etc (common)
- Potentiometers, DIP Switches (used for debug only)
- SO-16 resistors (used for debug only)
- Linear regulators (will be replaced with auxiliary power taps in final design).
- Circuit board (pricing should be similar from one to the other)

From the two-stage schematic there were also several parts that were removed for this comparison. These include common parts, parts whose function is not duplicated by the MIROF converter solution, and parts which we expect to appear in the final version of the MIROF circuit (for instance a start-up circuit).

Table 6 below shows a cost breakdown of the component differential between the two systems. Note that this comparison does not include the digital controller for the MIROF

converter solution. With the two systems as shown the MIROF offers a cost savings of over \$3, which is potentially significant, even in larger systems. Unfortunately, this does not represent a revolutionary price decrease, however it is clear there is some benefit available.

Description	Quantity	Price	Total
Common Value 0603 Caps	17	0.01	0.17
Large Value 0603 Caps	6	0.02	0.12
Common Value 0805 Caps	10	0.02	0.2
Large Value 0805 Caps	1	0.1	0.1
High Voltage Caps	8	0.03	0.24
Large Chip High Voltage Caps	6	0.05	0.3
Electrolytic Bulk Cap	2	0.41	0.82
Auxiliary Bulk Cap	4	0.05	0.2
Buck Diodes	3	0.1	0.3
Signal Diodes	10	0.036	0.36
Common Mode Choke	1	0.35	0.35
Buck Inductors	3	0.6	1.8
Optocoupler	2	0.1	0.2
Buck Controller	1	0.7	0.7
Chip Resistor	55	0.01	0.55
Large Chip Resistor	7	0.05	0.35
PFC Controller	1	0.35	0.35
Reference	2	0.257	0.514
Zener Diode	3	0.02	0.06
Buck FET	3	0.16	0.48
Signal BJT	4	0.01	0.04
Op Amp	1	0.1	0.1
Voltage Supervisor	1	0.15	0.15
Op Amp	1	0.2	0.2
Secondary Diode	1	0.277	0.277

Two Stage Total 8.931

Description	Quantity	Price	Total
0603 common value caps	11	0.01	0.11
0603 high capacitance	10	0.02	0.2
0805 common values caps	3	0.02	0.06
High voltage 1206 caps	7	0.03	0.21
Electrolytic bulk cap	3	0.41	1.23
Secondary Diode	4	0.036	0.144
Optocouplers	3	0.09	0.27
Chip Resistors	66	0.01	0.66
Large Chip Resistors	8	0.05	0.4
Secondary FETs	3	0.157	0.471
Gate Drives	2	0.39	0.78
High Speed Comparator	1	0.085	0.085
Dual Comparator	1	0.065	0.065
Zener	3	0.02	0.06
Dual Signal Diode	1	0.02	0.02
Signal BJT	3	0.02	0.06
Signal FET	3	0.03	0.09
Integrator Op Amp	3	0.2	0.6

MIROF Total 5.515

Table 6 – Cost Comparison Chart

The digital controller changes the story of the cost savings when added to the MIROF total cost—the part was quoted at more than \$13. This cost addition is absolutely unacceptable, and demonstrates a need to migrate the MIROF solution to a cheap microcontroller.

The second form of cost comparison is in the form of circuit board area and total volume. The MIROF converter used for this research was designed specifically to have a similar component height to the two-stage solution it is being compared to. Therefore we will assume that the volume of these solutions scales linearly with the circuit board area.

Figure 38 below shows a comparison between the board areas of the two solutions. The MIROF is on the left while the two stage solution is shown with the two converters broken into separate boards. Calculating the total area of the two solutions gives a value of 22.14 in² for the MIROF compared to 21.69 in² for the two stage converter.

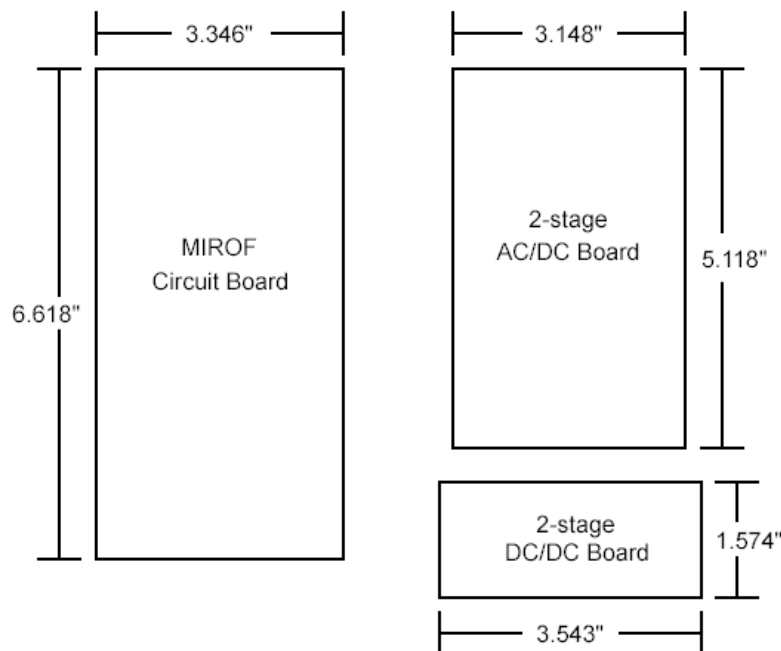


Figure 38 – Board Area Comparison

There is room on both boards which goes to circuits that are not duplicated on the other solution—debugging circuitry on the MIROF as opposed to feature specific circuitry on the two-

stage converter. The space taken by these extra circuits is assumed to be roughly equal and therefore will not contribute to any differences between the two.

While the two stage solution is slightly better in terms of board area, a difference of 2% is negligible. A designer can safely assume that these systems will be equal in board space and volume.

5.2 Steady State Performance

The MIROF and two-stage converters may also be measured by standard power supply performance metrics: Efficiency, response time, output ripple, and line regulation. Due to the integrator method of measuring the string current, it is also useful to quantify the line frequency regulation.

The most important performance metric is arguably the power supply efficiency. Table 7 below shows the efficiency of the MIROF solution, with a typical total power supply efficiency of 71%. This is not a very good mark, although part of the reason for the low efficiency is the high auxiliary power being drawn from the 18V source.

Typically in lighting systems auxiliary power is supplied from a winding on the transformer, although in this system auxiliary power is drawn through linear regulators from an independent DC supply (this configuration was chosen to simplify the design). This coupled with the fact that the microcontroller is an extremely high performance part means that there is a much larger auxiliary power requirement than for a typical lighting power supply.

With this in mind, a second measurement, Line Efficiency—the efficiency of the power supply without the auxiliary power taken into account, is shown as an alternative to the total efficiency. We will assume that the efficiency of an optimized system will lie somewhere between these two measurements.

Line Frequency	60 Hz			50 Hz		
Input Voltage	108.2	120.28	132.36	108.27	120.3	132.33
Input Current	0.352	0.321	0.293	0.343	0.308	0.281
Auxiliary Voltage	17.99	17.99	17.99	17.99	17.99	17.99
Auxiliary Current	0.147	0.147	0.147	0.148	0.148	0.147
Power Factor	0.98	0.98	0.97	0.99	0.99	0.98
Line Power	38.09	38.61	38.78	37.14	37.05	37.18
Total Input Power	40.73	41.25	41.43	39.80	39.71	39.83
Vred	27.98	28.04	27.92	27.78	27.81	27.75
Ired	0.285	0.284	0.283	0.277	0.276	0.277
Vgreen	37.97	38.07	37.87	37.62	37.67	37.56
Igreen	0.282	0.282	0.282	0.275	0.275	0.274
Vblue	37.82	37.91	37.74	37.53	37.57	37.48
Iblue	0.282	0.282	0.282	0.273	0.273	0.272
Output Power	29.35	29.39	29.22	28.29	28.29	28.17
Line Efficiency	77.1%	76.1%	75.4%	76.2%	76.4%	75.8%
Total Efficiency	72.1%	71.2%	70.5%	71.1%	71.2%	70.7%

Table 7 – MIROF Power Supply Efficiency

In comparison, Table 8 shows the efficiency of the conventional two-stage converter. Note that the efficiency here is better than that of the MIROF converter. This is especially true when comparing the conventional converter to the total efficiency of the MIROF. This is an unexpected result, as there is no theoretical reason that the MIROF should suffer an efficiency disadvantage to a standard flyback with a second stage buck. The difference is possibly due to a difference in operating point (the standard converter is a 230V system) between the two, as well as a slightly larger (and therefore more efficient) transformer in the two-stage converter. While these don't necessarily explain the performance differences between the two, it seems clear that the MIROF does not offer a definitive efficiency advantage.

Line Frequency	60 Hz			50 Hz		
Input Voltage	205.47	230.59	255.63	205.62	230.74	255.86
Input Current	0.167	0.153	0.144	0.166	0.152	0.142
Power Factor	0.94	0.92	0.89	0.95	0.93	0.91
Input Power	34.31	35.28	36.81	34.13	35.07	36.33
Vred	26.56	26.56	26.54	26.66	26.59	26.62
Ired	0.113	0.113	0.113	0.111	0.112	0.111
Vgreen	36.24	36.34	36.29	36.61	36.43	36.51
Igreen	0.395	0.395	0.395	0.395	0.395	0.395
Vblue	36.09	36.19	36.14	36.45	36.27	36.35
Iblue	0.267	0.267	0.267	0.267	0.267	0.267
Output Power	26.95	27.02	26.98	27.15	27.05	27.08
Total Efficiency	78.5%	76.6%	73.3%	79.5%	77.1%	74.5%

Table 8 – Two-stage converter efficiency

The next metric by which we want to compare the two is the output current ripple on the LED strings. The current level through the LEDs has a direct impact on the light output, and therefore the current ripple can have an effect on the aesthetic quality of the light. Below, Table 9 and Table 10 show the LED ripple current for the MIROF and two-stage converters, respectively.

There are two things to note: first note that the ripple current of the MIROF is dependent on the input line frequency. This is because the MIROF is a flyback PFC, and therefore the output will have a sinusoidal component at twice the input line frequency. The sinusoidal voltage output is due to the shape of the output current of the converter (shown in Figure 27). A sinusoidal current with fixed amplitude across a capacitance will result in a sinusoidal capacitor voltage which varies with a varying signal frequency. For systems with variable input voltage, the LED string capacitors must be sized for the worst case input line frequency (50Hz for a universal supply).

Second, while the ripple current seems comparable in magnitude from one system to the next note that the MIROF ripple is at twice the input line frequency (120 or 100Hz), whereas the

ripple for the two-stage converter is at the buck switching frequency (180kHz). 180kHz is imperceptible to the human eye, however 100Hz is very close to being visible. Any slight perturbations may cause some noticeable flicker. Thus the MIROF may represent a risk to the quality of the light output of the system, however, more work must be done to quantify this risk.

Line Frequency	60 Hz			50 Hz		
Input Voltage	108.2	120.23	132.86	108.23	120.8	132.38
Input Current	0.353	0.318	0.29	0.341	0.305	0.28
I ripple (red)	0.156	0.150	0.156	0.175	0.173	0.178
I ripple (green)	0.093	0.091	0.093	0.105	0.105	0.107
I ripple (blue)	0.113	0.107	0.113	0.127	0.124	0.130

Table 9 – MIROF LED Current Ripple

Line Frequency	60 Hz			50 Hz		
Input Voltage	205.6	230.82	255.86	205.65	230.59	255.72
Input Current	0.165	0.151	0.141	0.166	0.153	0.143
I ripple (red)	0.073	0.073	0.073	0.073	0.073	0.074
I ripple (green)	0.095	0.096	0.095	0.095	0.095	0.095
I ripple (blue)	0.088	0.086	0.086	0.086	0.086	0.086

Table 10 – Two-Stage LED Current Ripple

5.3 Transient Performance

Transient response is also a critical aspect of power supply performance. In the case of LED lighting, requirements are driven mostly by the visual aspects of the light. For instance, one might require an LED lighting supply to respond to a line variance in such a way that there is no visible effect on the light output.

For the purposes of this evaluation, we will simply compare the transient responses of the two systems and give a qualitative analysis of the performance of the MIROF converter. The transient characteristics that we will evaluate are the on/off step, line voltage regulation, and line frequency regulation.

Figure 39 shows the difference between rise times of the MIROF converter and the two-stage approach. Note that the rise time of the two-stage converter red string is nearly 10 times faster than all strings of the MIROF converter. While this is an impressive difference, the rise time of the MIROF converter strings is less than 200ms. This time period is consistent with the thermal time constant of an incandescent bulb. Typically this would be considered acceptable performance for a solid state light.

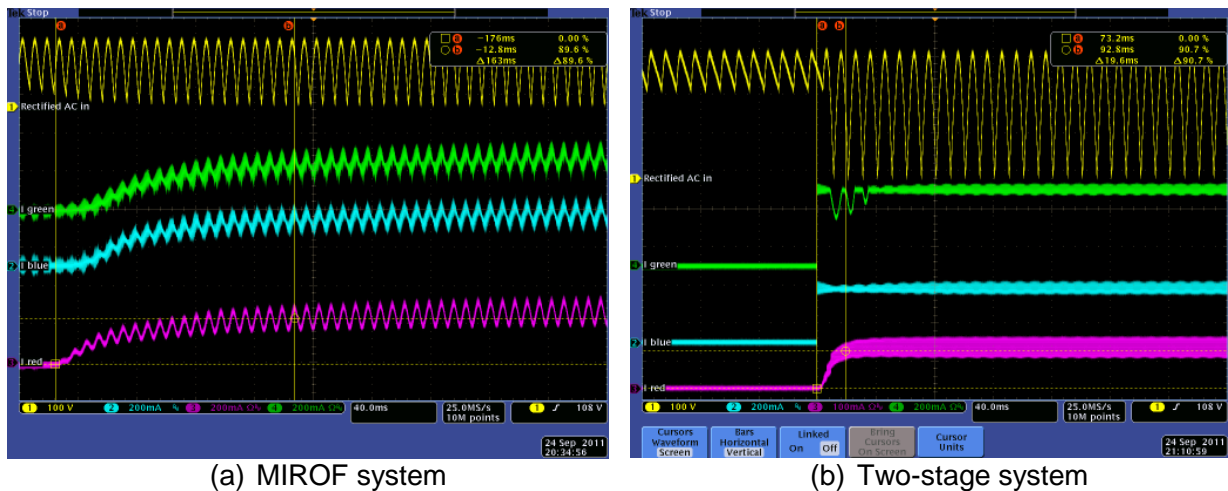


Figure 39 – LED Current Rise Time in MIROF Vs Two-Stage System

The fall time of the two systems is comparable to the rise times. The fall time of the blue and green strings of the two-stage converter is approximately three times faster than the fall time of the MIROF converter. Again, the MIROF converter, while slower, responds quickly enough to be comparable to an incandescent. Figure 40 shows fall-time waveforms for each of the two systems.

There is one last thing to note about the rise and fall times of the two converters: the buck style control of the conventional two-stage system allows it to turn the string current on and off nearly instantaneously. Note the red string current in Figure 40: the fall time of this string is much faster than that of the blue and green strings—approximately 15 μ s. This is possible because the buck converter on the secondary of the two-string system is able to turn current to the load off. When it does the small amount of energy in the buck capacitors depletes fairly

quickly. There is much more energy in the flyback capacitors by comparison. This is necessary due to the PFC requirements of the converter. When the flyback stops supplying current to the load the energy in its load capacitors takes much longer to deplete compared to the buck.

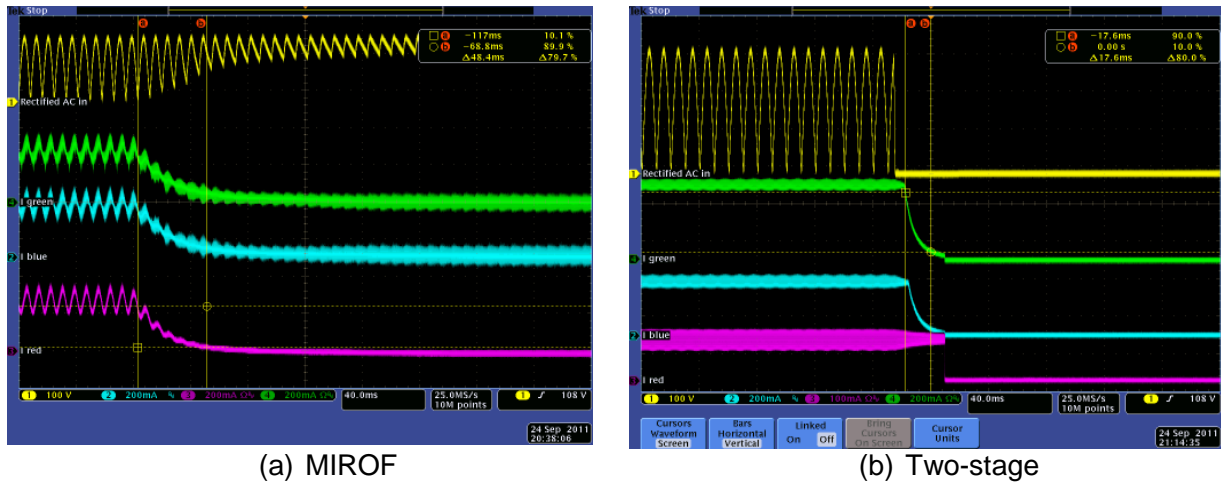


Figure 40 – LED Current Fall Time

The buck converter on the secondary of the two-stage converter therefore provides a buffer from the energy on the flyback load capacitors. This is advantageous not only for the fall time, but also for the rise time, where the two stage converter may start from a condition where the flyback capacitors are already charged. The MIROF must charge these capacitors from zero when the light is enabled which takes significantly more time.

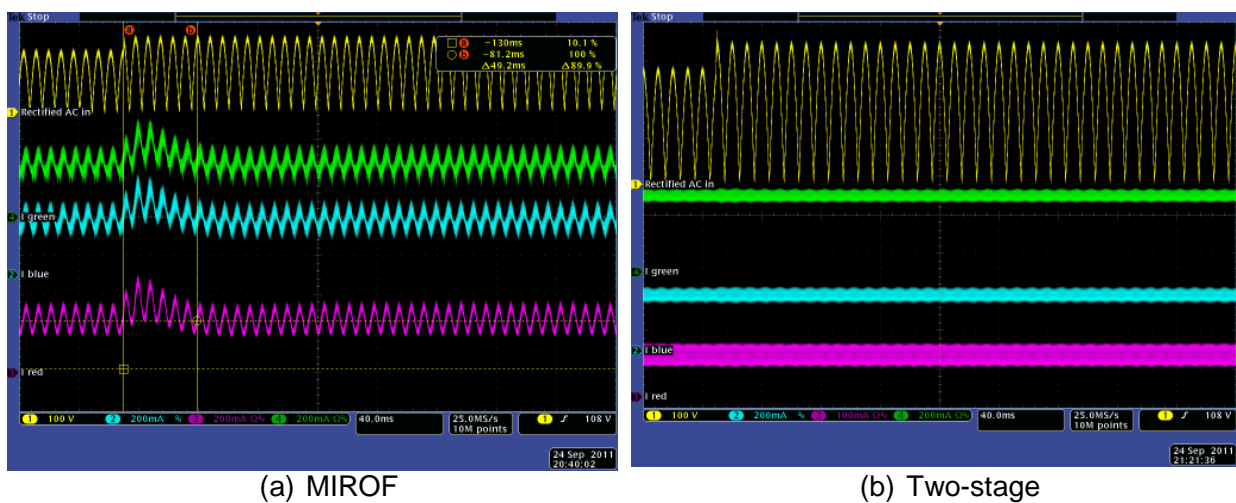


Figure 41 – Response to Line Voltage Step

Figure 41 above shows the response by each system to a step in input line voltage. The MIROF waveform shows a clear perturbation in the string current, which is also visible to the eye as a “pulse” of the light. The two-stage converter in contrast literally shows no response to the line change whatsoever in terms of visible light change or by inspection of the waveform. This is an area where the MIROF converter is clearly inferior to the two-stage approach, although again, depending on the requirements of the system the MIROF performance may be acceptable.

Finally, the last aspect of dynamic performance is the response to a step in line frequency. This is not typically a requirement of PFC systems simply because a step in input line frequency does not perturb the line current in most cases. The MIROF in this case is an exception since the load current is measured via an integrating circuit. Once the input line frequency changes, the controller must sense the change and react to it.

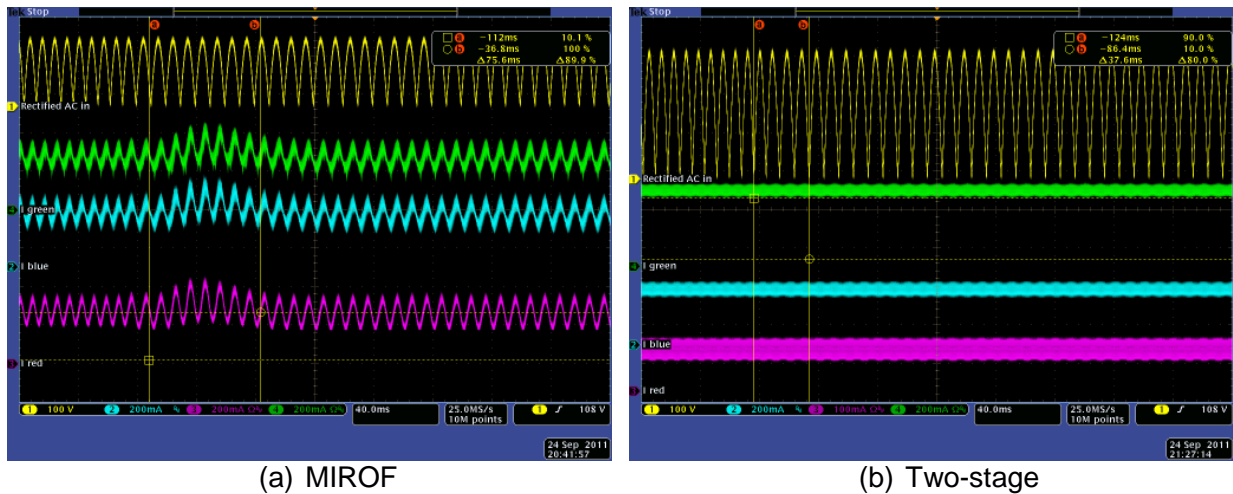


Figure 42 – Response to Line Frequency Step

Figure 42 above shows the responses of the two converters to a step in line frequency. Again the perturbation to the MIROF load current is evident, and is also slightly visible as a change in output light level. The two-stage current on the other hand is completely unaffected, as would be expected for most systems with this type of PFC solution. This is another area where the two-stage is clearly superior, however dramatic changes in line frequency tend to be

very rare. This is a case where the inferior performance of the MIROF may be easily overlooked since the occurrence of this particular perturbation is unlikely.

Chapter 6. Conclusions

The MIROF converter seems to be an attractive alternate to the standard two-stage converter design. It allows the designer to remove multiple expensive inductor components and it consolidates the control for the system into a single controller, allowing for a more integrated design.

In Chapter 2 and Chapter 3, analysis and design is laid out for the MIROF—a novel implementation of SIMO Flyback converter. The design is validated and demonstrated to be functional and effective in later chapters. Finally, the MIROF is compared against both the current standard of technology and the benchmarks for acceptability. While the performance of the MIROF is lackluster compared to the two-stage converter, it is nonetheless acceptable based on common performance specifications.

The most important goal of implementing a MIROF system is reduction of total system cost. In the price comparison of Section 5.1 we find that the MIROF system does offer benefits to reduce system cost. One outlier in the cost equation is the expensive DSP that was chosen for the purposes of demonstrating this technology. This component will have to be migrated to a less expensive microcontroller in order for the MIROF converter to be truly viable. Otherwise the MIROF offered cost benefits consistent with what we expected at the outset.

The steady state performance evaluation in Sections 5.2 shows that the performance of the MIROF is comparable to the standard two-stage converter. Disregarding the power draw of the oversized DSP the MIROF runs with an efficiency that is in the same range as the two-stage design. Regarding ripple current to the load, there is a slight increase from the two-stage to the MIROF, however this can be minimized by designing a higher bulk capacitance into each string. Ultimately the application and customer will decide to what extent this is acceptable, however there were no indications of degradation to light performance in the demonstration unit.

Dynamically, the MIROF is clearly inferior to the two-stage, although it is acceptable based on standard specifications for light performance. The latter is well equipped to handle line transients without allowing any impact on the light output—simply because there are two stages, and therefore more buffer between the source and the load, however the MIROF meets specifications for maximum transient duration, and shows no visible degradation to light quality under typical utility transient conditions.

Looking forward, there is still work to be done before the MIROF can be introduced as a productionable product. First and foremost the DSP which was used to demonstrate the technology must be migrated to a simpler and more cost effective device. Such a component will not be capable of producing the complex switching waveforms required by this model. Therefore work will be required to simplify the model to meet the capabilities of a simpler controller.

Next, isolation of the primary and secondary circuits is an important option for LED lighting designers. This is not something that was considered during the design of the demonstration circuit (in which the primary and secondary grounds are connected). Isolation is important because it allows the customer access to the LEDs without danger of electric shock. In non-isolated designs special lenses may be used to offer this protection, however this invariably has a negative impact on the optical efficiency of the light, and therefore their use is eschewed unless absolutely necessary. More work is required to determine how isolation will impact the cost of the MIROF converter.

Dimming compatibility is also not something that was considered for this demonstration and is absolutely critical for the marketability of a general lighting product. Dimming of a multiple color light is not typically straightforward, and more work is needed to understand how an analog dimming technique can be applied to this topology while maintaining a consistent color temperature.

Finally, the EMI of the system must be evaluated and a solution must be put in place. This may be challenging since the path from the MIROF output to the load is hard switching with respect to the input line voltage, and therefore represents a “loud” source of EMI. Isolation of primary and secondary grounds may go a long way in mitigating the EMI risk with this converter, although more work must be done to show precisely what the performance currently is.

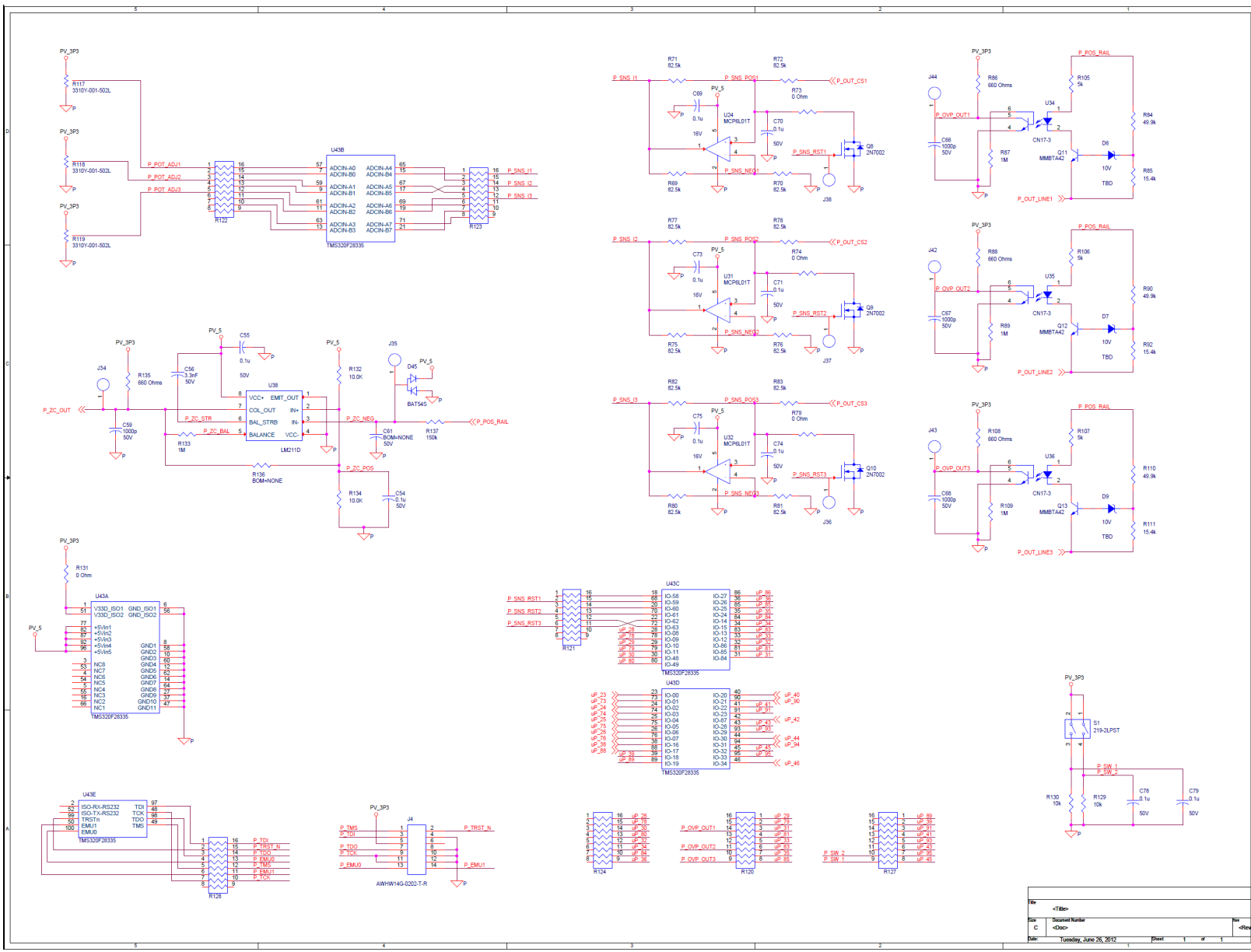
Generally speaking, the demonstration unit described in this paper represents an excellent first step towards using SIMO technology in high-end LED Lighting. Based on the models and novel method presented in this paper, the MIROF converter may serve as a vehicle for reducing the cost of multi-string LED lights, although there is work left to be done. With the aid of future work, SIMO technology can help achieve the goal of reducing driver cost without compromising the performance of color controlled LED lighting products.

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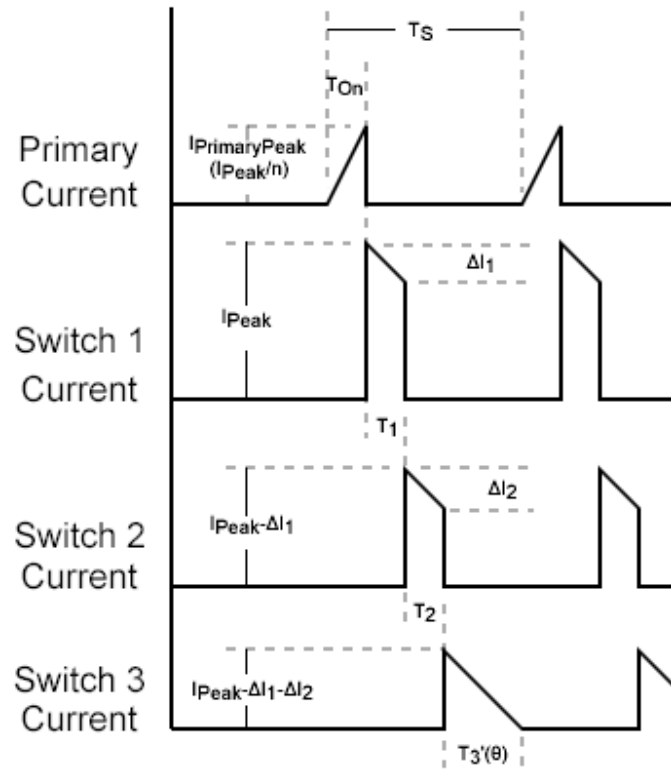
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Appendix B Proof of Equation 55



Current Through the Secondary Conduction Channels

Using the diagram above, and defining ΔI_3 as the peak current of Switch 3, we can by inspection state:

$$I_{\text{Peak}} = \Delta I_1 + \Delta I_2 + \Delta I_3$$

Combining Equation 53 with a generic form of Equation 5 yields:

$$\Delta I = \frac{V_x \cdot d_x \cdot T \cdot n^2}{L}$$

Combining the above equations yields:

$$I_{Peak} = \frac{V_1 \cdot d_1 \cdot T' \cdot n^2}{L_P} + \frac{V_2 \cdot d_2 \cdot T' \cdot n^2}{L_P} + \frac{V_3 \cdot d_3 \cdot T' \cdot n^2}{L_P}$$

$$\frac{L_P \cdot I_{Peak}}{n^2} = T' \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)$$

$$T' = \frac{L_P \cdot I_{Peak}}{n^2 \cdot (V_1 \cdot d_1 + V_2 \cdot d_2 + V_3 \cdot d_3)}$$

Appendix C Mathcad File of the Constant Ratio System

MIROF System Simulation with Reverse Sequence Switching and Decoupling Conditioner

Power Converter General Parameters

RMS Input Voltage	$V_{inrms} := 100V$	Nominal Input Power	$P_{nom} := 50W$	Transformer Turns Ratio	$n := 3$
Peak Input Voltage	$V_{inpk} := V_{inrms} \cdot \sqrt{2} = 141.421V$	Switching Frequency	$f_s := 100kHz$	Primary Transformer Inductance	$L_p := 210\mu H$
"Nominal" Output Voltage	$V_{outnom} := 40V$	Switching Period	$T_s := \frac{1}{f_s} = 10 \cdot \mu s$	Secondary Transformer Inductance	$L_s := \frac{L_p}{n^2} = 23.333 \cdot \mu H$

LED and Output String Parameters

	Green	Blue	Red
Output Voltage	$V_{out1} := 12 \cdot 3.24V = 38.88V$	$V_{out2} := 12 \cdot 3.4V = 40.8V$	$V_{out3} := 14 \cdot 2V = 28V$
Diode Model Forward Voltage	$V_{d1} := 12 \cdot 2.99V = 35.88V$	$V_{d2} := 12 \cdot 3.0001V = 36.001V$	$V_{d3} := 14 \cdot 1.8215V = 25.501V$
Diode Model Resistance	$R_{d1} := 12 \cdot 0.625\Omega = 7.5\Omega$	$R_{d2} := 12 \cdot 1.333\Omega = 15.996\Omega$	$R_{d3} := 14 \cdot 0.714\Omega = 9.996\Omega$
String Current	$I_{out1} := 400mA$	$I_{out2} := 300mA$	$I_{out3} := 250mA$
Load Capacitance	$C_{out1} := 530\mu F$	$C_{out2} := 530\mu F$	$C_{out3} := 890\mu F$
Initial Guess for Conditioned System Input	$u1_{guess} := 1.612 \cdot 10^{-6}$	$u2_{guess} := 1.209 \cdot 10^{-6}$	$u3_{guess} := 1.008 \cdot 10^{-6}$

Unitless Values for Linearization

$$\begin{aligned}
 T_{s\text{scalar}} &:= \frac{T_s}{s} = 1 \times 10^{-5} & L_{p\text{scalar}} &:= \frac{L_p}{H} = 2.1 \times 10^{-4} & V_{in\text{scalar}} &:= \frac{V_{inpk}}{V} = 141.421 \\
 V_{1\text{scalar}} &:= \frac{V_{out1}}{V} = 38.88 & V_{2\text{scalar}} &:= \frac{V_{out2}}{V} = 40.8 & V_{3\text{scalar}} &:= \frac{V_{out3}}{V} = 28 \\
 I_{1\text{scalar}} &:= \frac{I_{out1}}{A} = 0.4 & I_{2\text{scalar}} &:= \frac{I_{out2}}{A} = 0.3 & I_{3\text{scalar}} &:= \frac{I_{out3}}{A} = 0.25
 \end{aligned}$$

System Equations for Output String Currents

$$I_{cycle1}(u1, u2, u3, Vin, V1, V2, V3) := \frac{Vin^2 \cdot (u1 + u2 + u3)^2 \cdot u1}{4 \cdot T_{sscalar} \cdot L_{pscalar} \cdot (V1 \cdot u1 + V2 \cdot u2 + V3 \cdot u3)}$$

$$I_{cycle2}(u1, u2, u3, Vin, V1, V2, V3) := \frac{Vin^2 \cdot (u1 + u2 + u3)^2 \cdot u2}{4 \cdot T_{sscalar} \cdot L_{pscalar} \cdot (V1 \cdot u1 + V2 \cdot u2 + V3 \cdot u3)}$$

$$I_{cycle3}(u1, u2, u3, Vin, V1, V2, V3) := \frac{Vin^2 \cdot (u1 + u2 + u3)^2 \cdot u3}{4 \cdot T_{sscalar} \cdot L_{pscalar} \cdot (V1 \cdot u1 + V2 \cdot u2 + V3 \cdot u3)}$$

System Equations for Capacitor Voltages

$$dV1(u1, u2, u3, Vin, V1, V2, V3) := \frac{I_{cycle1}(u1, u2, u3, Vin, V1, V2, V3)}{\frac{C_{out1}}{F}} - \frac{V1 - \frac{Vd1}{V}}{\frac{C_{out1}}{F} \cdot \frac{Rd1}{\Omega}}$$

$$dV2(u1, u2, u3, Vin, V1, V2, V3) := \frac{I_{cycle2}(u1, u2, u3, Vin, V1, V2, V3)}{\frac{C_{out2}}{F}} - \frac{V2 - \frac{Vd2}{V}}{\frac{C_{out2}}{F} \cdot \frac{Rd2}{\Omega}}$$

$$dV3(u1, u2, u3, Vin, V1, V2, V3) := \frac{I_{cycle3}(u1, u2, u3, Vin, V1, V2, V3)}{\frac{C_{out3}}{F}} - \frac{V3 - \frac{Vd3}{V}}{\frac{C_{out3}}{F} \cdot \frac{Rd3}{\Omega}}$$

Solve Simultaneous Equations to Find Steady State System Inputs

Given

$$I_{cycle1}(u1_{guess}, u2_{guess}, u3_{guess}, Vin_{scalar}, V1_{scalar}, V2_{scalar}, V3_{scalar}) = I1_{scalar}$$

$$I_{cycle2}(u1_{guess}, u2_{guess}, u3_{guess}, Vin_{scalar}, V1_{scalar}, V2_{scalar}, V3_{scalar}) = I2_{scalar}$$

$$I_{cycle3}(u1_{guess}, u2_{guess}, u3_{guess}, Vin_{scalar}, V1_{scalar}, V2_{scalar}, V3_{scalar}) = I3_{scalar}$$

$$T := \text{Find}(u1_{guess}, u2_{guess}, u3_{guess}) = \begin{pmatrix} 1.61 \times 10^{-6} \\ 1.207 \times 10^{-6} \\ 1.006 \times 10^{-6} \end{pmatrix}$$

$$T_{on} := (T_0 + T_1 + T_2) \cdot s = 3.823 \cdot \mu s$$

$$d1 := \frac{T_0}{T_0 + T_1 + T_2} = 0.421 \quad d2 := \frac{T_1}{T_0 + T_1 + T_2} = 0.316 \quad d3 := \frac{T_2}{T_0 + T_1 + T_2} = 0.263$$

$$T_{prime} := \frac{Vin_{pk} \cdot T_{on}}{n \cdot (V_{out1} \cdot d1 + V_{out2} \cdot d2 + V_{out3} \cdot d3)} = 4.92 \cdot \mu s$$

Linearization to Produce the System Matrices

$$\text{Amat}(u1, u2, u3, \text{Vin}, V1, V2, V3) := \begin{pmatrix} \frac{d}{dV1}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV2}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV3}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) \\ \frac{d}{dV1}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV2}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV3}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) \\ \frac{d}{dV1}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV2}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{dV3}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) \end{pmatrix}$$

Eigenvalues: $\text{Eamat} := \text{eigenvals}\left(\text{Amat}(T_0, T_1, T_2, \text{Vinscalar}, V1\text{scalar}, V2\text{scalar}, V3\text{scalar})\right) = \begin{pmatrix} -260.685 \\ -123.467 \\ -113.355 \end{pmatrix}$

$$\text{Bmat}(u1, u2, u3, \text{Vin}, V1, V2, V3) := \begin{pmatrix} \frac{d}{du1}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du2}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du3}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{d\text{Vin}}dV1(u1, u2, u3, \text{Vin}, V1, V2, V3) \\ \frac{d}{du1}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du2}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du3}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{d\text{Vin}}dV2(u1, u2, u3, \text{Vin}, V1, V2, V3) \\ \frac{d}{du1}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du2}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{du3}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) & \frac{d}{d\text{Vin}}dV3(u1, u2, u3, \text{Vin}, V1, V2, V3) \end{pmatrix}$$

$$\text{Cmat}(u1, u2, u3, \text{Vin}, V1, V2, V3) := \begin{pmatrix} \frac{d}{dV1}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV2}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV3}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \\ \frac{d}{dV1}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV2}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV3}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \\ \frac{d}{dV1}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV2}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{dV3}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \end{pmatrix}$$

$$\text{Dmat}(u1, u2, u3, \text{Vin}, V1, V2, V3) := \begin{pmatrix} \frac{d}{du1}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du2}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du3}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{d\text{Vin}}(\text{Icycle1}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \\ \frac{d}{du1}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du2}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du3}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{d\text{Vin}}(\text{Icycle2}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \\ \frac{d}{du1}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du2}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{du3}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) & \frac{d}{d\text{Vin}}(\text{Icycle3}(u1, u2, u3, \text{Vin}, V1, V2, V3)) \end{pmatrix}$$

Steady State Values of the System Matrices

$$A_{dc} := \text{Amat}(T_0, T_1, T_2, \text{Vinscalar}, \text{V1scalar}, \text{V2scalar}, \text{V3scalar}) = \begin{pmatrix} -260.249 & -6.508 & -5.423 \\ -6.508 & -122.835 & -4.067 \\ -3.229 & -2.422 & -114.423 \end{pmatrix}$$

$$B_{dc} := \text{Bmat}(T_0, T_1, T_2, \text{Vinscalar}, \text{V1scalar}, \text{V2scalar}, \text{V3scalar}) = \begin{pmatrix} 6.542 \times 10^8 & 1.749 \times 10^8 & 2.439 \times 10^8 & 10.673 \\ 1.389 \times 10^8 & 6.001 \times 10^8 & 1.829 \times 10^8 & 8.005 \\ 6.895 \times 10^7 & 6.51 \times 10^7 & 3.7 \times 10^8 & 3.973 \end{pmatrix}$$

$$C_{dc} := \text{Cmat}(T_0, T_1, T_2, \text{Vinscalar}, \text{V1scalar}, \text{V2scalar}, \text{V3scalar}) = \begin{pmatrix} -4.599 \times 10^{-3} & -3.449 \times 10^{-3} & -2.874 \times 10^{-3} \\ -3.449 \times 10^{-3} & -2.587 \times 10^{-3} & -2.156 \times 10^{-3} \\ -2.874 \times 10^{-3} & -2.156 \times 10^{-3} & -1.796 \times 10^{-3} \end{pmatrix}$$

$$D_{dc} := \text{Dmat}(T_0, T_1, T_2, \text{Vinscalar}, \text{V1scalar}, \text{V2scalar}, \text{V3scalar}) = \begin{pmatrix} 3.467 \times 10^5 & 9.271 \times 10^4 & 1.293 \times 10^5 & 5.657 \times 10^{-3} \\ 7.364 \times 10^4 & 3.18 \times 10^5 & 9.696 \times 10^4 & 4.243 \times 10^{-3} \\ 6.137 \times 10^4 & 5.794 \times 10^4 & 3.293 \times 10^5 & 3.536 \times 10^{-3} \end{pmatrix}$$

System DC Gain (Plant)

$$H_{dc} := D_{dc} - C_{dc} \cdot A_{dc}^{-1} \cdot B_{dc} = \begin{pmatrix} 3.305 \times 10^5 & 7.222 \times 10^4 & 1.117 \times 10^5 & 5.172 \times 10^{-3} \\ 6.145 \times 10^4 & 3.027 \times 10^5 & 8.375 \times 10^4 & 3.879 \times 10^{-3} \\ 5.121 \times 10^4 & 4.514 \times 10^4 & 3.183 \times 10^5 & 3.232 \times 10^{-3} \end{pmatrix}$$

Definition of Constants

$$I := \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \quad j := \sqrt{-1}$$

Generate Gain Magnitude Plots from the System Equation, H(s), for all I/O Combinations

$$H(s) := C_{dc} \cdot (sI - A_{dc})^{-1} \cdot B_{dc} + D_{dc}$$

$$H_{mag11}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{0,0}|)$$

$$H_{mag12}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{0,1}|)$$

$$H_{mag13}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{0,2}|)$$

$$H_{mag14}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{0,3}|)$$

$$H_{mag21}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{1,0}|)$$

$$H_{mag22}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{1,1}|)$$

$$H_{mag23}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{1,2}|)$$

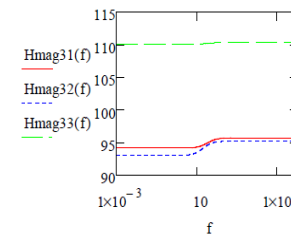
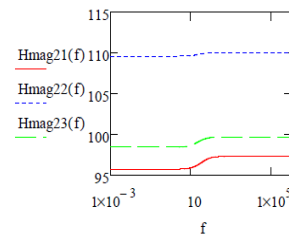
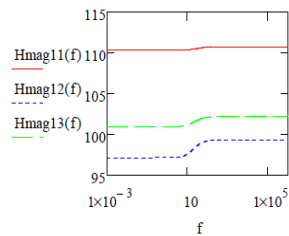
$$H_{mag24}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{1,3}|)$$

$$H_{mag31}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{2,0}|)$$

$$H_{mag32}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{2,1}|)$$

$$H_{mag33}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{2,2}|)$$

$$H_{mag34}(f) := 20 \cdot \log(|H(j \cdot 2 \cdot \pi \cdot f)_{2,3}|)$$



Generate Bode Plots of the Loop Gains for the Diagonal Systems

$$C(s) := \frac{1}{3000 \cdot s}$$

$$\text{zero}(f) := 0$$

$$\text{Hfb11}(s) := H(s)_{0,0} \cdot C(s)$$

$$\text{Hfbmag11}(f) := 20 \cdot \log(|\text{Hfb11}(j \cdot 2 \cdot \pi \cdot f)|)$$

$$\text{Hfbang11}(f) := \frac{180}{\pi} \arg(\text{Hfb11}(j \cdot 2 \cdot \pi \cdot f))$$

$$\text{Hfb22}(s) := H(s)_{1,1} \cdot C(s)$$

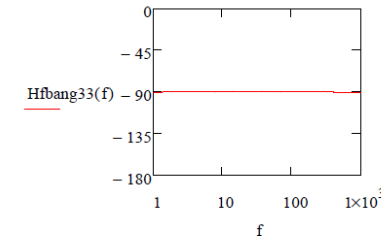
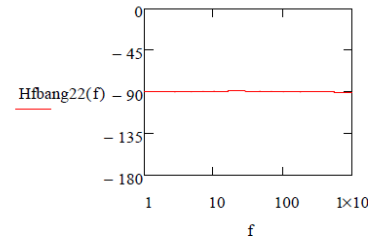
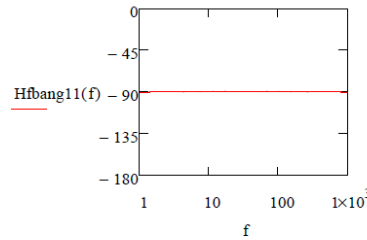
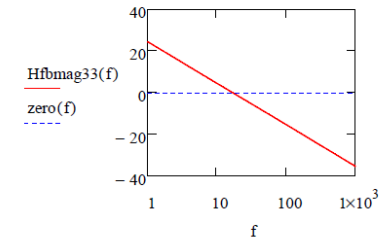
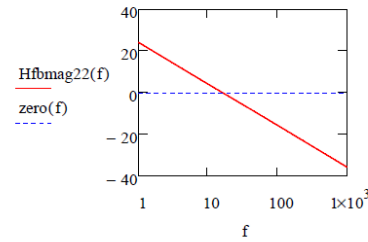
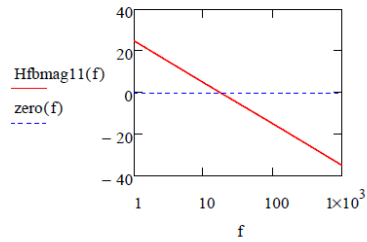
$$\text{Hfbmag22}(f) := 20 \cdot \log(|\text{Hfb22}(j \cdot 2 \cdot \pi \cdot f)|)$$

$$\text{Hfbang22}(f) := \frac{180}{\pi} \arg(\text{Hfb22}(j \cdot 2 \cdot \pi \cdot f))$$

$$\text{Hfb33}(s) := H(s)_{2,2} \cdot C(s)$$

$$\text{Hfbmag33}(f) := 20 \cdot \log(|\text{Hfb33}(j \cdot 2 \cdot \pi \cdot f)|)$$

$$\text{Hfbang33}(f) := \frac{180}{\pi} \arg(\text{Hfb33}(j \cdot 2 \cdot \pi \cdot f))$$



Generate A matrix for the Closed-Loop System and Find Eigenvalues to Demonstrate Stability

$$\text{Mdc} := \begin{pmatrix} \frac{1}{3000} & 0 & 0 \\ 0 & \frac{1}{3000} & 0 \\ 0 & 0 & \frac{1}{3000} \\ 0 & 0 & 0 \end{pmatrix}$$

$$\text{Ndc} := \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}$$

$$\text{Odc} := \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

$$\text{Afb} := \text{stack}(\text{augment}(\text{Adc}, \text{Bdc} \cdot \text{Mdc}), \text{augment}(-\text{Cdc}, -\text{Ddc} \cdot \text{Mdc}))$$

$$\text{eigenvals}(\text{Afb}) = \begin{pmatrix} -275.925 \\ -169.687 \\ -103.149 \\ -114.426 \\ -82.84 \\ -82.84 \end{pmatrix}$$