Integration Challenges in High Power Density Wide Bandgap Based Circuits for Transportation Applications

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Abstract

Because of the increasing emphasis on environmental concerns, there has been a growing demand for lower fuel consumption in modern transportation applications. To reduce fuel comsumption, higher efficiency, higher power density power converters are desired. The new generation of wide bandgap (WBG) power semiconductor devices pushs the switching frequency and output power of the electric system in transportation to a higher level thanks to their higher blocking voltage, higher operating frequency, and smaller parasitic elements. With benefits such as size reudcetion, costs saving, and reliability improvement, integration technologies have been widely adopted in power electronic systems, especially with the emergence of WBG semiconductor devices. These improvements will futher translate into reduced fuel consumption, extended operating range, and increased passenger compartment.

Transportation applications pose a challenging environment for converter integration. The fast switching speed and the high blocking voltage of WBG semiconductor devices also put forward higher requirements for converter integration. First, the power converters used in transportation applications are often powered from the batteries that support multiple loads. During load changes, crank, or jump-start, undesired transients exist, which requires the power converters to be capable of operating under a wide-input-voltage range. This requirement results in a very limited design region of acceptance, making the converter hard to handle uncertainties. However, the integration process might bring large uncertainties, such as material property changes. This phenomenon can degrade converter performance or even cause design failures. Besides, the power converters for

transporation applications oftern work in harsh environment, such as high ambient temperature or low air density. The former can lead to overheated and the latter degrades insulation strength, both of which hinder high power density design. Moreover, with the advent of all kinds of portable devices, converters are required to deliver more power. The introduction of universal serial bus (USB) power delivery (PD) extends the delivered power. To meet the specification, the power converters should provide a wide-output-voltage range, which brings challenges to the converter design. Furthermore, the charger is usually fed by an ac voltage of more than 100 V, which is then stepped down to 5 V – 20 V. The high step-down ratio increases the converter loss.

To address the wide-input-voltage and high-temperature challenges, a dual-output, PCB-embedded transformer based active-clamp Flyback (ACF) gate-drive power supply (GDPS) for automotive applications is proposed. It has been demonstrated that the PCB-embedding technique effectively improves converter power density. The final prototype achieves a power density of 53.2 W/in^3, a peak efficiency of 89.7 %, a transformer input-output capacitance of 9.7 pF, an input-voltage range of 9.9 V – 28 V, and a maximum operating temperature at low-line (LL) voltage of 105 °C and 115 °C at high-line (HL) voltage.

Yet the above unit failed to meet all of the design targets due to the material property degradation in transformer. This degradation is caused by the mechanical stress induced in the integration process. To investigate its impact on wide-input-voltage converter design, several PCB-embedded magnetic boards are fabricated with different core materials and stress levels. Based on the analysis, experimentally derived correction factors are proposed and applied to the models used in the multi-objective optimization (MDO) process. The improved design successfully achieves the targeted wide-input-votlage range.

When aircrafts climb during flight, air density reduces and the breakdown voltage decreases

correspondingly. The insulation design becomes a challenge for the gate driver for SiC-based airborne applications. To provide sufficient insulation strength and achieve high power density simultaneously, a Paschen curve based insulation co-ordination is proposed. Electric-field control methodology is applied to the layout design. By properly designing the field control plates, the peak electric field has been shifted from the air to fr4 material that features much higher dielectric strength. The proposed gate driver attains a small size of 128.7 mm × 61.2 mm × 23.8 mm. Partial discharging tests are conducted in an altitude chamber. The experimental result shows that the proposed gate driver provides sufficient insulation strength at 50, 000 ft.

To tackle the wide-output-voltage range and high-step-down ratio challenges in the USB-C PD charger in airborne applications, a LLC converter with PCB-winding based transformer with built-in leakage inductance is presented. A flying-capacitor based voltage divider (FCVD) switching bridge is proposed to replace the conventional half-bridge or full-bridge switching bridge. The propsed FCVD shows a current reduction of over 50 % than the conventional half-bridge with the same circuit elements. The prototype achieves a high efficiency of 90.3 % to 93.2 % over 5 V to 20 V outputs, and a high power density of 73.2 W/ in^3, which is almost two time larger than the state-of-the-art power density. Partial discharging tests are also conducted in an altitude chamber. A partial discharing inspection voltage of 800 V is found at 10, 000 ft, which is much higher than the requirement.

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General Audience Abstract

Because of the increasing emphasis on environmental concerns, there has been a growing demand for lower fuel consumption in modern transportation applications. The new generation of wide bandgap (WBG) power semiconductor devices and various integration technologies enable electronic systems in transportation to achieve higher efficiency and higher power density. These improvements will futher translate into reduced fuel consumption, extended operating range, and increased passenger compartment. However, transportation applications put more requirements on power converter designs. This dissertation, therefore, focusing on addressing the integration challenges in high power density WBG-based circuits for transportation applications from the aspects of wide-input-voltage range, material properties degradation, harsh environment, and wide-output-voltage range together with high step-down ratio.

To meet the wide-input-voltage and high temperature requirements in automotive applications, a dual-output, PCB-embedded transformer based active-clamp Flyback (ACF) dc-dc converter is proposed. The final prototype achieves a power density of 53.2 W/in^3, a peak efficiency of 89.7 %, a transformer input-output capacitance of 9.7 pF, an input-voltage range of 9.7 V – 28 V, and a maximum operating temperature at low-line (LL) voltage of 105 °C and 115 °C at high-line (HL) voltage.

Yet the above unit failed to meet all of the design targets due to the material property degration in PCB-embedded transformer. This degradation is caused by the mechanical stress during integration process. To investigate its impact on automotive converter, several PCB-embedded

magnetic boards are fabricated with different core materials and stress levels. Based on the analysis, experimentally derived correction factors are proposed and applied to the models used in the multiobjective optimization process. The improved design successfully achieves the targeted wide-input-votlage range.

When aircrafts climb during flight, air density reduces and thus insulation strength decreases correspondingly. Instead of using oversized altitude correction factors provided by IEC standards, a Paschen curve based insulation co-ordination is proposed. Electric-field control methodology is applied to the gate driver layout. The proposed gate driver attains a small size of 128.7 mm × 61.2 mm × 23.8 mm. Partial discharging test is conducted in an altitude chamber. The experimental result shows that the proposed gate driver provide sufficient insulation strength at 50, 000 ft.

To tackle the wide-output-voltage range and high-step-down ratio challenges in the USB-C PD charger in airborne applications, a LLC converter with PCB-winding based transformer with built-in leakage inductance is presented. A flying-capacitor-based voltage divider (FCVD) switching bridge is proposed to replace the conventional half-bridge or full-bridge switching bridge. The propsed FCVD shows a current reduction of over 50 % than the conventional half-bridge with the same circuit design. The prototype achieves a high efficiency of 90.3 % to 93.2 % over 5 V to 20 V outputs, and a high power density of 73.2 W/ in^3, which is more than two time larger than the state-of-the-art power density. Partial discharging tests are also conducted in an altitude chamber. A partial discharing inspection voltage (PDIV) of 800 V is found at 10, 000 ft, which is much higher than the requirement.

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Chapter 1 Introduction

1.1 Application background

For decades, trains, vehicles, aircraft and other forms of transportation have played an important role in modern life. Energy used for transportation has experienced tremendous growth as well. Transportation consumes two-thirds of the world's petroleum and has become the largest contributor to global environmental change [1]. Environmental concerns are increasing; thus, there is a growing demand for lower fuel consumption in modern transportation applications. To reduce fuel consumption, a more efficient system design is desired. One popular option is to reduce transportation's weight and size. On average in the U.S., every 100 kg of weight reduction will achieve a reduction of 0.69 L/100 km in fuel consumption [2]. Since power converters are ubiquitous in transportation applications, their performance significantly affects transportation, which becomes one of the driving forces for high efficiency, high power density converter design.

A. Automotive applications

In a conventional gas-powered car, there is a battery supportting the electrical loads. The battery is typically 12 V for small passenger cars and 24 V for larger trucks. The battery is charged by an alternator. The power distribution system supports multiple loads including body systems, chassis systems, power steering, powertrain system, safety and convenience system, etc. As more and more advanced technology and comfort features are added to new cars, those electrical loads consume more power. As the power level increases, the load current climbs and brings in a significant amount of conduction loss. Copper wire is required to be thicker for carrying high current and the copper weight imposes a negative impact on car fuel efficiency.

The sales of advanced electric drive vehicles (EVs) such as hybrid-electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEV), fuel cell electric vehicles (FCVs), and battery electric vehicles (BEVs) have increased from less than 500 thousand in 2014 to more than 2 million in 2019, and they account for about 3% of the global passenger car sales in 2019 [4]. All of them require power electronics to function. Fig. 1- 1 shows an example of an electric network of an electric drive system. In an electric system drive, power is distributed at multiple levels. The car is powered by a high voltage battery, which is typically 400V - 800V. The dc-dc converter steps down the voltage from the battery to the auxiliary loads. Typical loads include the informative system, LED lights, advanced driver-assistance systems (ADAS), etc. As car-related informative technology develops, the number of electric components increases significantly and so do the electrical loads. The dc-dc converter needs to have both high efficiency to save the battery power and high power density to reduce the weight for longer mileage.

B. Airborne applications

The electrical system of an airplane is expected to climb from $19 billion in 2020 to $37 billion before 2030 [5]. The electrical system of an aircraft includes the power generation system, power distribution system, power conversion system, and energy storage system. The combination

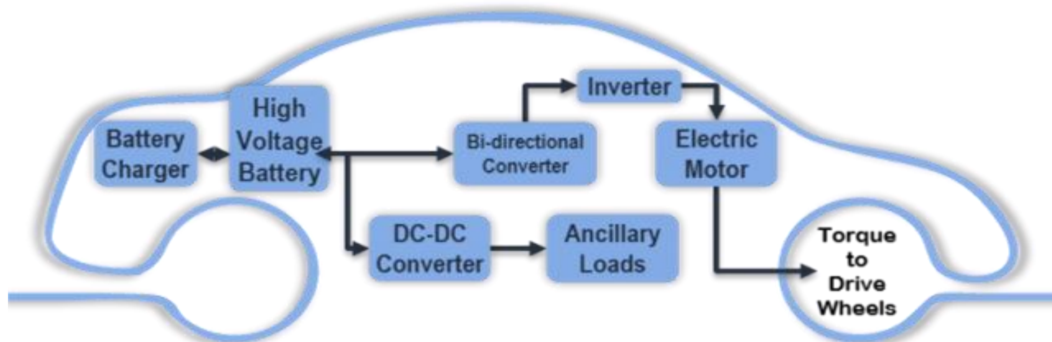


Fig. 1- 1. The electrical system of an electric drive system [3].

of the power distribution system and power conversion system accounts for more than half of the global aircraft electrical system market.

One example of the electric network in aircraft is shown in Fig. 1- 2. A typical electric power system for aircraft includes six ac generators, two batteries, rectifier units, transformers, and loads [7]. The generators provide the power to both the high-voltage bus and the low-voltage bus. The bus voltage supports a number of aircraft subsystems. The rectifier unit converts three-phase ac power to dc power. The batteries provide the power to essential subsystems in an emergency condition.

The hydraulic system is greatly important in conventional aircraft architecture. Its disadvantages include low fuel efficiency and the need for corrosive fluids. The electric power system reduces the weight of the airplane and therefore improves the fuel efficiency. Moreover, there is a growing demand for electric technology. The electrified system provides some major benefits including better faulty management, load regulation, diagnostic monitoring, and scalability. As a result, more and more power-hungry digital systems are installed in airplanes.

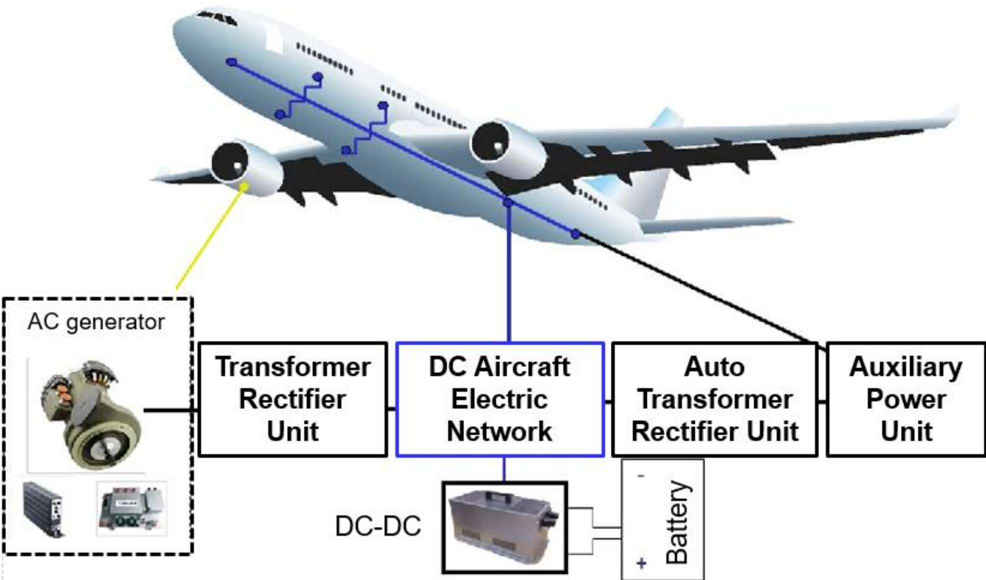


Fig. 1- 2. Power electronics in aircrafts [6].

For the reasons above, power electronics plays a crucial role in the next generation of the aircraft. The power distribution system needs to be scaled up to meet the current demand. The efficiency of the electrical system needs to be improved for better thermal management. Heat removal is typically expensive, and a higher electrical system efficiency help to reduce both the initial cost and operating cost. The size and weight of the power conversion system is expected to be small for better fuel efficiency.

1.2 Emerging Wide-bandgap power semiconductor devices in transportation applications

To achieve a better performance, wide bandgap (WBG) semiconductor devices attract widespread attention. Among the possible semiconductor material candidates, Silicon Carbide (SiC) and Gallium Nitride (GaN) show the best tradeoff between theoretical characteristics, real commercial availability of the starting material, and maturity of their technological processes [8].

The key properties of SiC, GaN and Silicon (Si) materials are compared in Fig. 1- 3. The

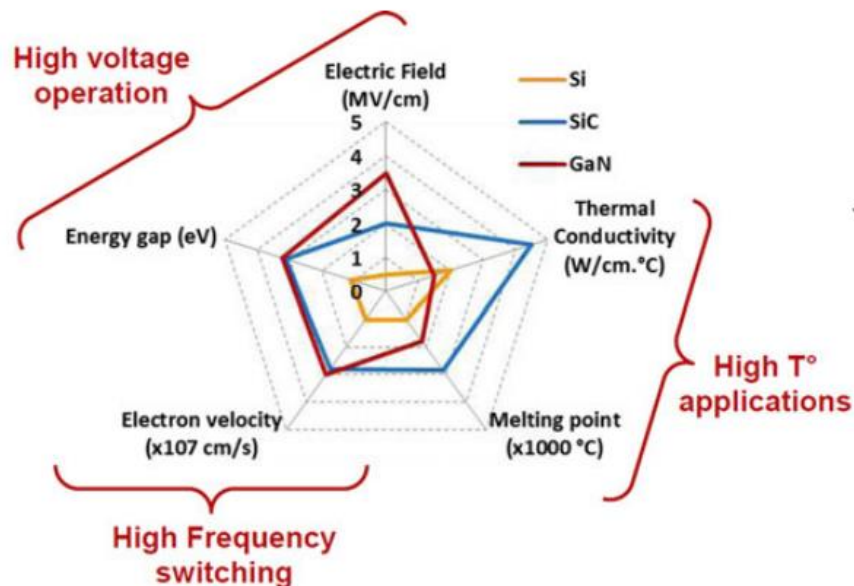


Fig. 1- 3. Summary of Si, SiC, and GaN relevant material properties [8].

higher breakdown electric field of WBG devices allows thinner and higher doped voltage-blocking layers [9]. It results in a lower voltage drop and smaller ON-state resistance compared to their Si counterparts at the same voltage rating. In addition, the higher electron saturation velocity of WBG semiconductors allows a higher switching speed. The *dv/dt* of Si IGBTs can hardly reach 8 kV/μs, while that of SiC MOSFET and GaN HEMTs can reach 18 kV/μs [10] and 103 kV/μs [11] respectively. In addition, the p-n junction leakage current remains relatively low thanks to their lower intrinsic carrier concentration [12], which allows them to operate in high temperature environments.

As depicted in Fig. 1- 4, the new generation of power semiconductor devices pushes the switching frequency and output power of the electric system in transportation to a higher level [13]. This improvement will further translate into reduced fuel consumption, extended operating range, and increased passenger compartments [14]-[16]. By replacing Si IGBT with

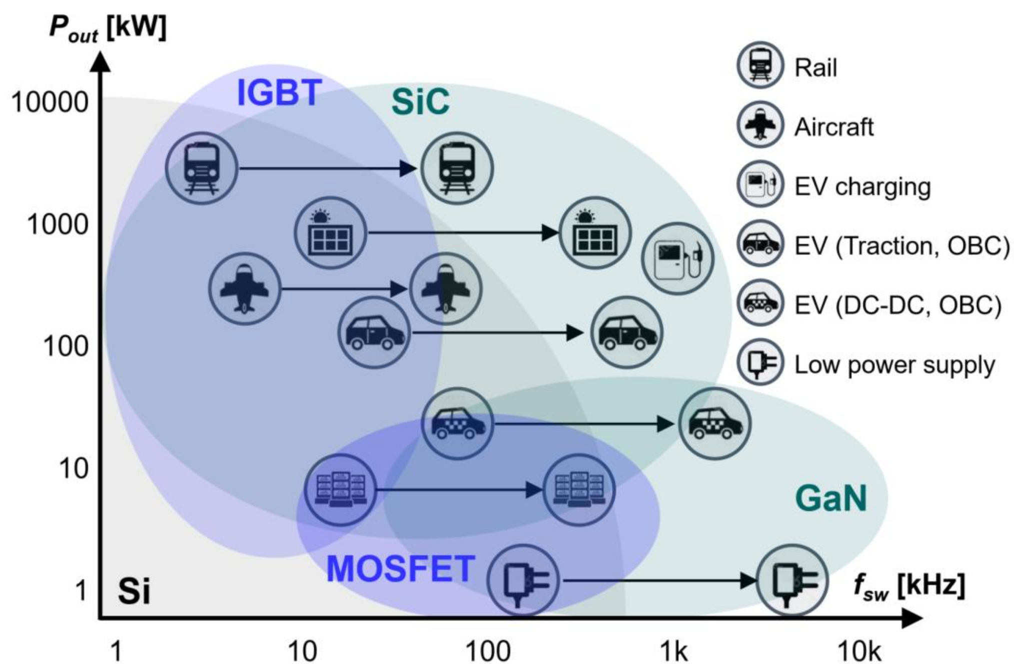


Fig. 1- 4. Emerging of WBG semiconductor devices in transportation applications [13].

the SiC MOSFET, the inverter for an EV traction drive improves the average efficiency by 9.6 % to 13.1 %, compared to the Si IGBT inverter for different drive cycles [17]. In [18], a SiC-based traction inverter was successfully operating at an ambient temperature of 120 °C. The cooling system is significantly simplified, thus reducing the size and weight. By pushing the switching frequency, the size and weight of the WBG-based converters are 4.72 liters smaller and 4.6 kg lighter than the Si converter due to the reduced filter requirement [19].

Thanks to the efficiency, size and weight improvement with WBG semiconductor devices, the fuel economy in transportation is improved [20], [21]. A 10 % growth in fuel efficiency and an 80 % volume reduction in the power control unit are expected in future development.

1.3 Integration in power electronic systems

With benefits such as size reuduction, costs saving, and reliability improvement, integration technologies have been widely adopted in power electronic systems, especially with the emergence of WBG semiconductor devices [22]. According to the device characteristics and fabrication process, the integration technologies can be classified into active component integration, passive component integration, and auxiliary component integration.

A. Integration of active components

The integration of active components aims to reduce parasitic inductance and size, and improve thermal dissipation. Active integration technologies include interconnection technology, packaging materials, structure, etc. Examples are shown in Fig. 1- 5.

Since WBG devices have a much faster switching speed than their Si counterparts do, they are more sensitive to prarasitic elements. During switching transients, the parasitic inductance can resonate with the devices parasitic capacitance, leading to undesirable ringing that increases

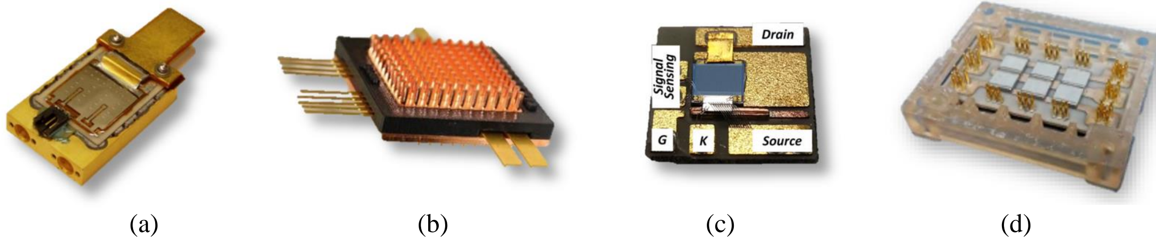


Fig. 1- 5. Integration technologies of active components: (a) hybrid blade module [29], (b) double-side cooling [50], (c) stack-die GaN [53], and (d) stack-substrate SiC module [54].

electromagnetic interference (EMI) [23]. The parasitic inductances can also cause disastrous overvoltage across the drain-source of the devics. This becomes a concern when short-circuit (SC) fault exists. The high *dv/dt* and *di/dt* value of the WBG devices can make the fault current and voltage rapidly rise up to more than ten times of those seen during normal operation, leading to an extensively higher accumulated energy and a fasater destruction process. In an effort to reduce the parasitic inductances, conventional wire-bonding technology has been replaced with ribbon [24], [25], flexible PCB [26]-[30], solid posts, shims, or bumps [31]-[33], solder balls or ball grid arrys [34], direct-bonded solder [35], or vias in PCB or ceramic substrates [36]-[38].

The packaging materials limits the devices operating temperature. To enable WBG devices operating at temperature above 200 °C, advanced packaging materials are needed to provide compatible Coefficient of Thermal Expansion (CTE) with WBG chips, and reliable high temperature performance [39]. Advanced packaging materials include substrate materials [40] that provides cooling, interconnection, and mechanical support for the power modules, die-attaching materials [41]-[44] used to attach semiconductor dies to a package, and encapsulation materials [45] used to protect power module against mechanical stress, electrical breakdown, chemical erosions, radiation, etc.

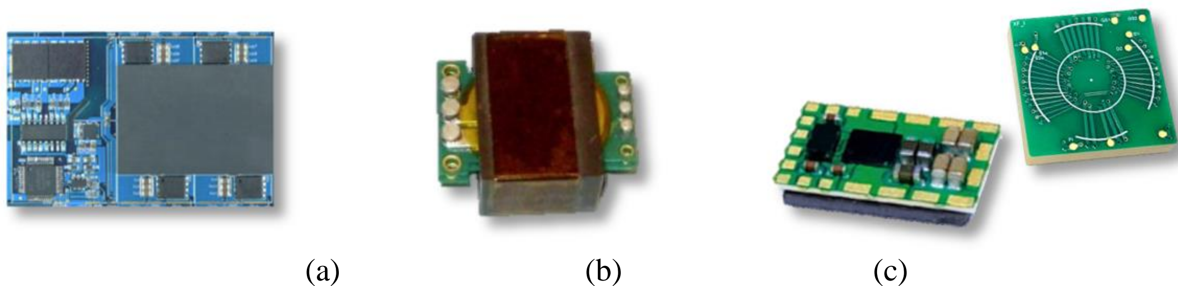
Many research groups have opted to replace the conventional 2D layout structure with 2.5D

structures [46]-[49] and 3D structures [50]-[52] regarding the packaging structure. Both 2.5D and 3D structure show distinct improvement in parasitic inductance and thermal dissipation. A new package using a stack-die configuration together with re-arrangement of the wire-bonding structure is developed in [53] for high-voltage cascade GaN devices. It eliminates the package-related common-source inductance (CSI) that causes noise and voltage ringing. By stacking two substrates and integrating the common-mode current screen into the power module [54], the electric field and high-frequency noise have successfully reduced.

B. *Integration of passive components*

Passive components, especially magnetic components, often take consideratble space in power converters, which becomes one of the main bottlenecks for improving the power density. The advent of WBG semiconductor devices makes it possible to push the switching frequency to the order of Mhz, which makes the size of magnetic components much smaller. However, the move to the higher frequency range brings challenges such as larger core loss and ac winding loss. Efforts have been made by several research groups to counteract the negative effects of high frequency. Examples are shown in Fig. 1- 6.

A matrix transformer with magnetic integration has been introduced in several research



(a) (b) (c)

Fig. 1- 6. Integration technologies of passive components: (a) integrating two transformer cores into one using flux cancellation [55], (b) PCB winding [58], and (c) embedded magnetic [61], [62].

studies [55]-[57]. In this structure, a single transformer is broken down to a number of elemental transformers. Two UI cores can be combined into one EI core by properly designing the winding layout. The elemental transformers have the same turns number, and their secondary windings are connected in parallel. As a result, the voltage-second exerted on each elemental transformer will be the same, and the net flux in the center leg is diminished. Therefore, the center leg can be removed. This integration concept reduces the transformer core size and consequently, the core loss.

An integration technique is also widely applied to winding design. The move to higher frequency operation not only shrinks the magnetic component size, but also reduces the voltage-second across the magnetic component. Therefore, less inductance is required and a low number of turns is sufficient, which provides the opportunity to adopt the print circuit board (PCB) as the winding [55]-[59]. In addition, the PCB winding structure eliminates the labor-intensive manufacturing process and it offers improved reliability with a significant improvement of power density and EMI.

Resonant converters are gaining more and more attention thanks to their soft-switching feature and good regulation capability. To achieve regulation capability, sufficient resonant inductance should be provided. To minimize the passive component quantity, [59] and [60] integrate the resonant inductor into the transformer. This integration is achieved by utilizing a gapped EI core. Windings are distributed asymmetrically on the side legs, which generates unbalanced flux. A flux that is not fully coupled between the transformer primary winding and secondary winding will be forced to flow through the center leg, and thus the inductance can be controlled. This method utilizes the transformer leakage inductance as resonant inductance, and thus it reduces the number of passive components.

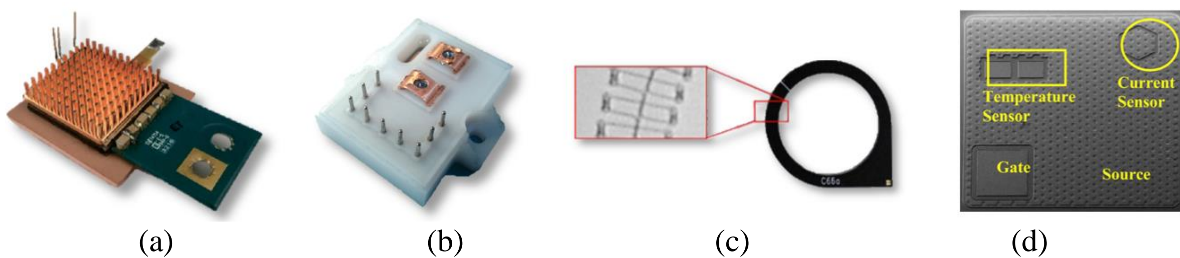
Embedding the passive component into the PCB is another option to improve power density [61], [62]. In this structure, magnetic core is emedded into multi-layer PCB, serving a substrate carrying the rest of the circuit. PCB vias and traces are used to construct the windings. The wasted space between the magnetic component and active layer can be removed so the power density can be improved.

C. Integration with auxilliary components

Integrating the converter with some associate components is also a popular option. It brings many benefits, such as reduced parasitics, improved thermal conductivity, and better performance. Examples are shown in Fig. 1- 7.

Some power modules integrate decoupling capacitor to reduce parasitic inductance. [63]-[68]. Placing the capacitors inside the module effectively shortens the commutation loop, and the parasitic inductance between the connections of the module to the external circuit is eliminated, achieving over 60 % reduction in loop inductance. Moreover, this technology reduces EMI because it can provide a more balanced layout. The more balanced layout can achieve a noise reduction up to 30 dB in the critical frequency range [67].

To fully utilize the native WBG device’s capability in terms of higher switching speed and



(a) (b) (c) (d)

Fig. 1- 7. Integration technologies of auxiliary components: (a) integrated decoupling capacitor [63], (b) integrated gate driver [69], (c) integrated current sensor [72], and (d) integrated temperature sensor [75].

higher operating frequency, higher driving speed is desired. However, it will inevitably generate high *di/dt* and *dv/dt*. To this end, integrating gate drivers into the modules has been done by several research groups [69], [70]. It has been demonstrated that this integration technology effectively reduces the gate loop inductance by minimizing the loop path.

Sensors are also frequently integrated into the power modules or the gate drivers to provide information for monitoring. In [71] and [72], a Rogowski coil based switch current sensor (RSCS) is integrated into the gate driver. The conventional desaturation protection method is replaced by the RSCS-based method. The latter approach shows a three times faster short-circuit fault detection and 50 ns less reaction time. As a result, the peak current and voltage are reduced by 400 A and 400 V, respectively [73]. Temperature sensor can be also integrated into gate driver [74], or into module [75]. The integrated temperature sensor enables active thermal control and condition monitoring of the devices, such as state-of-health, remaining useful life, maintenance scheduling, etc.

1.4 Integration challenges in WBG-based transportation application

All kinds of integration technologies are applied in power electronics. They demonstrate excellent improvements in parasitic inductance reduction, miniaturization, efficiency, etc. However, the advent of WBG semiconductor devices puts forward higher requirements for integration technologies. Furthermore, the harsh working environment of a transporation application puts more constraints on the converter design, and makes it more difficult to adopt integration technologies.

A. Wide-input-voltage operation

Transportation applications pose a challenging environment for converter integration. For

other applications like consumer electronics, converters are mostly embedded within systems, and they are well protected from the outside world with its unpredictable power supply and environmental variations. However, for the converters used in transportation applications, they are often powered directly from the batteries that also feed other loads. When the load changes, undesired transients exist and the converters powered directly from these batteries are required to work under a wide-input-voltage range to ensure a safe operation. For automotive applications, power converters should survive to undesired transients, including crank and jump-start as outlined in the international or manufacturing standards [76], [77].

The wide-input-voltage requirement limits the design region of acceptance. First, the wide-voltage-gain puts a lot of pressure on the controller. The duty cycle required by the switches should not exceed the capability of the controller, whose range is normally 30 % to 90 %. Fail to meet this requirement results in insufficient voltage gain. If frequency-controlled resonant converters are adopted, the switching frequency range will be very wide. As a result, a large EMI filter is required.

The wide-input-voltage range also brings difficulties in soft-switching design. The primary current decreases as the input voltage increases in the same load condition. To provide sufficient charging current at high voltages, the magnetizing inductance is reduced, leading to a high conduction loss especially at low voltages. Moreover, the working condition is changing with the input voltage, making converter optimization complicated.

B. Performance degradation

Integration technologies offer many benefits, but they also bring uncertainties to the design. The properties of the materials might change during the integration process, and their effect on the

materials is usually difficult to predict.

Take ferrite material as an example. Ferrite materials have been widely used, thanks to their high permeability and low core loss density. However, they exhibit magneto-mechanical properties that deteriorates permeability when subjected to mechanical stress, such as the pressure applied during the PCB fabrication process. Specifically, the applied mechanical stress generates local anisotropy in the sintered spinel grains such that minimum energy occurs when the magnetization is perpendicular to the applied stress in initially isotropic materials [78]–[81]. Stronger applied fields will then be required to rotate the magnetization through the stress direction, resulting in higher coercivity and reduced permeability [82]. It is hard to predict the degree of degradation by either analytical or numerical methods because it depends on the specific material used, geometry, and the fabrication process. This phenomenon makes ferrite integration hard to apply in transportation applications, which are not able to handle large uncertainty due to the strict constraints. To avoid design failures, another material that is less sensitive to mechanical stress has to be used, but this material might not be the best candidate at the targeted voltage and power level. Another solution could leave a much larger design margin; however, it might be overdesigned. Both of these solutions degrade converter performance.

C. Harsh environment

The power converters for transporation applications often work in harsh environments. As depicted in Fig. 1- 8, the working temperature of automotive converters is much higher than room temperature, especially when they are placed under the hood of the vehicle, where the ambient temperature is extremely high, up to 125 °C. Considering the limited space, forced convection is usually not available for auxiliary components like gate-driver power supply (GDPS). Therefore,

operating reliably in a high temperature environment becomes one of the design targets.

In addition, different transportation moves between different environments. Aircraft experiences variations in stress and temperature during flight. The pressure of the working environment for aircraft varies from 10,000 Pa to 400,000 Pa. As the altitude increases, the air density decreases, which degrades the air insulation strength, and can be explained by the Paschen curves shown in Fig. 1- 9. The temperature drops as the aircraft climbs due to exposure to decreasing ambient air temperature. Exposure to extremes in temperature and air density can lead

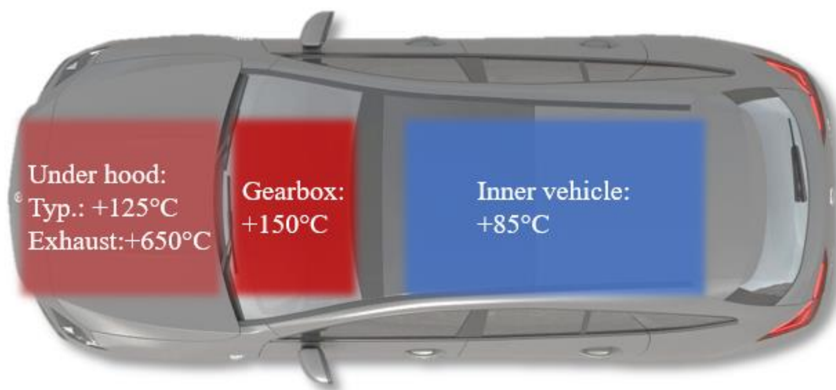


Fig. 1- 8. Temperature distribution in vehicle.

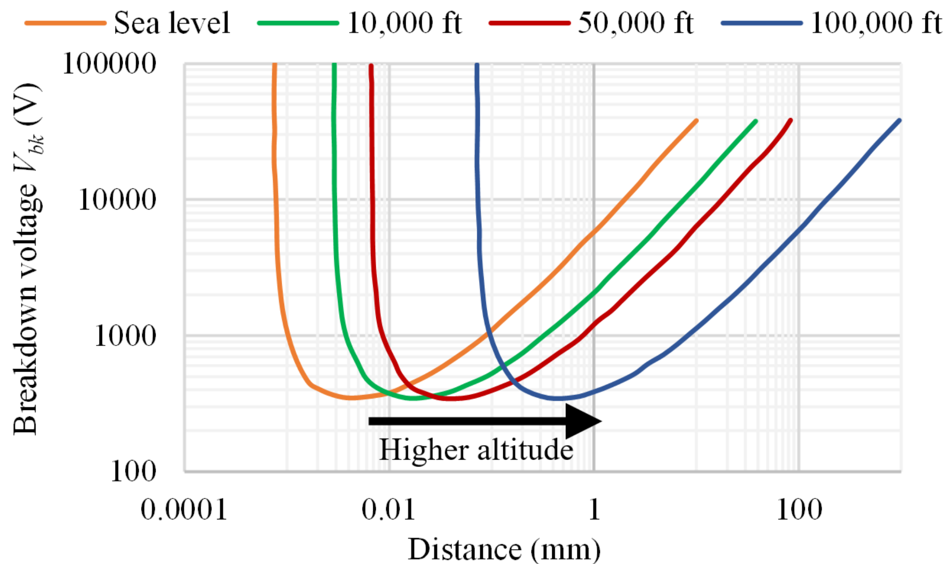


Fig. 1- 9. Paschen curve at different altitude.

to insulation degradation, causing damage to the power electronic system.

D. Wide-output-voltage and high-step-down ratio

At present, billions of portable devices are sold around the world for applications ranging from smaller electronic devices like smartphones and cameras to higher power consuming devices such as desktops and tablets. All kinds of portable devices make people's lives easier and more convenient, but they also add requirements to power converters especially for transportation applications. Due to the advent of a wide variety of consumer electronic devices, a new Universal Serial Bus (USB) specification known as USB power delivery (PD) has been introduced to increase the power delivery. USB PD supports 5 – 20 V and there are four voltage rails, which are 5 V, 9 V, 15 V and 20 V, respectively. To meet the USB-C PD specification, power converters should provide a wide-output-voltage range. The wide-output-voltage range puts a lot of stress on the controller and it leads to a very limited accepted design space as the wide-input-votlage range does. Since four nominal operating points need to be optimized simultaneously, converter optimization becomes extremely difficult because each of them has its own optimization focus.

Apart from the wide-output-voltage operation, high-step-down ratio is also required by the charger applications. There are ac-dc stage and dc-dc stage in the charger applications. The ac-dc stage is fed by an ac power source with voltage over 100 V, and it generates a high voltage dc bus (e.g. 200 V) for the second dc-dc stage. The dc-dc stage is responsible of stepping down the high voltage to low voltage of 5 – 20 V, representing a step-down ratio of 10 – 40. The high step-down ratio will put a high voltage stress across the transformer.

1.5 Dissertation outline

The objective of this research is to solve the integration challenges in WBG-based circuits in

transportation applications. The outline of this dissertation follows.

In Chapter 2, an optimal design of a dual-output, wide-input-voltage, PCB-embedded transformer-based ACF dc–dc converter is presented. The converter design procedure, including circuit design, transformer optimization, component selection, and constraints are first illustrated, seeking to achieve maximum power density and efficiency. Prototypes with a PCB-embedded transformer are constructed and tested. Experimental testing results including efficiency measurement, isolation capacitance, power density, and high temperature testing are shown. The permeability degradation in ferrite material caused by the embedding process is also revealed in this chapter.

In Chapter 3, the permeability degradation phenomenon in ferrite material and its impact on wide-input-voltage converter design is discussed. This degradation is caused by the embedding process. The experimental testing results with hand-wound transformer and PCB-embedded transformer are compared to show the embedding impact on converter performance. Furthermore, several PCB-embedded magnetic boards are fabricated with different core materials and stress levels to investigate this effect. Base on the analysis, experimentally derived correction factor is proposed to improve the accuracy of the model used in the multi-objective optimization process developed in Chapter 2. Prototypes with a hand-wound, PCB-embedded transformer and improved PCB-embedded (iPCB-embedded) transformer are built and compared, verifying that the improved design successfully achieves the targeted wide-input-voltage range. These are tested within a 10-W dual-output high power density (53.2 W/in^3) integrated ACF converter prototype built and based on GaN devices operating at 1 MHz.

In Chapter 4, a comprehensive design of an enhanced gate driver for a SiC-based generatr rectifier unit (GRU) for airborne applications is presented. To maximize the power density,

breakdown voltage in the Paschen curve was converted to the break down electic field (E-field) to determine the insulation co-ordination. E-field control methodology is applied to the gate driver layout. By properly designing the field control plates, the peak E-field has successfully shifted from the air to fr4 material that features much higher dielectric strength. The gate driver prototype attains a small size of 128.7 mm × 61.2 mm × 23.8 mm, significantly contributing to the system power density. Partial discharging tests are conducted in an altitude chamber. The experimental result shows that the proposed gate driver provides sufficient insulation strength at 50,000 ft.

Chapter 5 presents the design of an LLC resonant converter for a USB-C PD charger in airborne applications. The converter design procedure, including circuit design, PCB-winding-based transformer design, active component selection, are fisrt demonstrated. A flying-capacitor based voltage divider (FCVD) switching bridge is proposed to replace the conventional half-bridge or full-bridge switching bridge. A PCB-winding based transformer with built-in leakage inductance is adopted to improve power density. Prototypes are built and tested, showing a distance loss reduction in both the semiconductor devices and transformer with the proposed FCVD. The final prototype achieves a high power density of 73.2 W/in^3, which is almost twice of the state-of-the-art power density.

Chapter 6 summarizes and concludes this dissertation.

Chapter 2 PCB-Embedded Transformer Based Wide-Input-Voltage Gate-Drive Power Supply Design

2.1 Introduction

In modern automobiles, electronic devices are ubiquitous. An example of the power archtitechture in a vehicle is shown in Fig. 2- 1. A WBG-based ac-dc converter converts the ac voltage generated by the motor to the dc voltage that supports the main battery. A dc-dc converter steps down the high-voltage dc bus of 450 V to a low-votlage dc bus of 12 V, which supports the auxiliary battery that provides power for starter and engine, and other loads including body systems, chassis systems, power steering, convenience system, etc. The gate-drive power supply (GDPS) presented in this chapter is fed by the 12-V dc bus, and its output is connected to the gate-source terminals of the SiC-based half-bridge in the ac-dc converter.

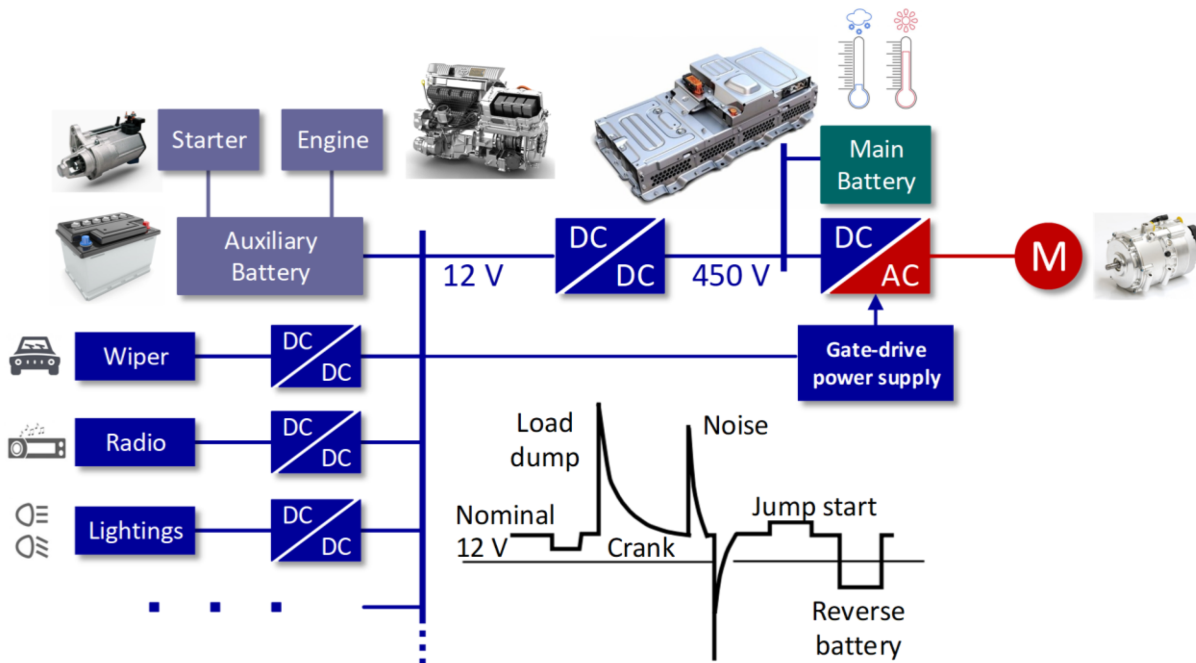


Fig. 2- 1. Power architechture in vehicle.

Compared to other dc-dc converter applications, this GDPS faces some of the most challenging electrical requirements. Unlike other applications like consumer electronics, whose converters are mostly embedded within sytems and well protected from the outside world with its unpredictable power supply and environmental variations, the automotive applications are powered from the battery that also feeds multiple loads. When the load changes, or during crank and jump-start, undesried transient exists. Therefore, the power converters in automotive applications should present survivability to these undesired transients as outlined in the international or manufacturing standards [83], [84]. This requires these circuits to be powered directly from the battery operating reliably over a wide-input-voltage range.

The proposed GDPS is placed under the hook of the vehcle, where thermal dissipation is relatively poor. The GDPS works in harsh environment of high ambient temperature, up to +125 °C [85], and it cannot be cooled by forced convection. As a result, high efficiency is mandatory to ensure safe operation. The size and weight of the vehicles significantly affect fuel comsumption. Due to the increasing emphasis on the environmental concerns, industries are seeking higher power density and higher efficiency converter. Therefore, high power density is desired to free up the limited space for other critical functionalities. For the above reasons, GDPSs for automotive applications target wide-input-voltage operation, high efficiency, and high power density.

Accordingly, there has been a growing trend seeking converter integration to achieve higher power density. The printed-circuit-board embedding (PCB-embedding) technique has been demonstrated as an effective way to achieve this target. Moreover, it also favors automated manufacturing and miniaturization [86], [87]. In this structure, magnetic cores are embedded in a multi-layer PCB that serves as a substrate to host the rest of the converter circuit. By saving the footprint of the transformer and removing the extra space between the transformer and other

components, a more compact design can be achieved. The fabrication process is compatible with conventional multi-layer PCB technology. This standardized process also reduces the cost because it involves fewer manual steps. Considering all of the above, the PCB-embedded technique is adopted to build the transformer.

Over the past years, research groups and industry have sought to develop applications featuring high efficiency and high power density in an effort to improve the performance and reduce the size and weight. Generally, magnetic components such as the transformer take up most of the space. According to the design method, the designed size and weight of transformers decrease significantly when the operating frequency increases, which becomes a driving force for the use of Wide-Bandgap (WBG) semiconductor devices, such as Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs). GaN devices are used in the proposed GDPS, thanks to their higher switching frequency, higher blocking voltage, and higher operating temperature capability. In effect, they facilitate a significant performance improvement of both power density and efficiency.

In this chapter, a GDPS with two isolated outputs of 24 V is designed. Its input voltage ranges from 9.7 V to 28 V, and the power rating of each output is 5 W. A PCB-embedded transformer used as a substrate carrying all of the converter circuitry, clearly contributes to the cost and size. The GaN devices from EPC are selected for their small ON-state resistance R_{ds} and output capacitance C_{oss}. First, the circuit design, including topology selection, operation mode selection, and turns ratio selection is presented. Second, the transformer structure, design constraints, optimization approach and its results are introduced. Next, the components selection, layout design, hardware assembly, and the qualification of the proposed GDPS are given. The summary and

conclusion end the chapter.

2.2 Circuit design

2.2.1 Topology selection

The PCB-embedded transformer structure is adopted in this work. In this structure, the transformer serves as a substrate carrying the rest of the circuit, and all other components are placed on the top of the substrate. Therefore, the space is limited and it requires a simple topology. Besides, active components such as GaN devices and rectifier diodes are the bottleneck in the high temperature operation because usually they have the lowest temperature rating. To avoid overheated, soft switching should be achieved in all load conditions to restrict the loss.

There are several topology candidates. One of the most popular isolated soft-switching topologies is the LLC resonant converter [88]-[90]. It offers many advantages. Priamry devices can achieve zero-voltage-switching (ZVS) turned-on in all input voltage ranges and all load conditions. Because of the resonance, current flowing through each semiconductor devices is sinusoidal, thus the turn-off current is smaller. In addition, the duty cycle applied to the switches is 50 %, which offers a symmetrical operation. However, the component number increases, making it difficult to achieve high power density.

Examples of the LLC circuit are shown in Fig. 2- 2 and Fig. 2- 3. In Fig. 2- 2, a dual-output LLC resonant converter with a full-bridge connection is provided. Since there are two isolated outputs, one primary, two secondary windings, and eight rectifier diodes are needed. These diodes not only increase the active component loss, but also require more space. Another LLC configuration with center-tapped connection at the secondary side is shown in Fig. 2- 3. In this configuration, one primary, four secondary windings, and four rectifier diodes are required. Even

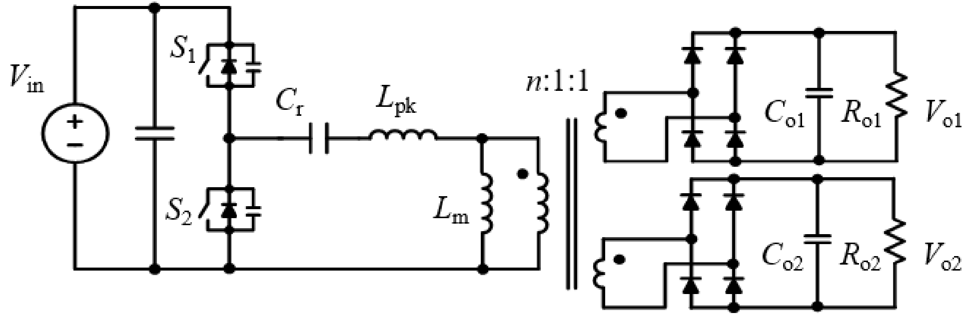


Fig. 2- 2. Full-bridge LLC resonant converter.

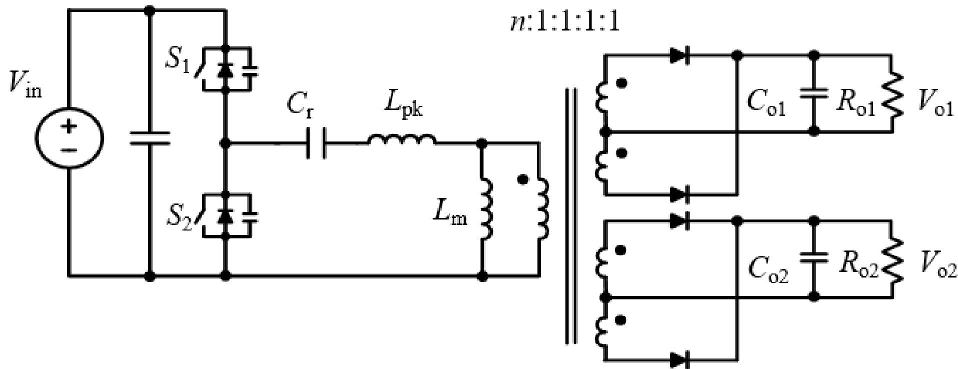


Fig. 2- 3. Center-tapped LLC resonant converter.

though the number of the rectifier diodes is cut down by half, more windings are required, which will need a much larger window area in the transformer core for placing the windings. Apart from the large size, winding loss might increase.

Quasi-resonant converters [91]-[93] are also under consideration. The benefit of these topologies is their fewer components and relatively low voltage and current stress. However, soft switching is lost in light or variable load conditions. It will result in a significant growth in switching loss that damages the devices at a high ambient temperature. The control design is also complicated in quasi-resonant converters. Few controllers are available and it complicates the design.

Another candidate is the active-clamp flyback (ACF) topology shown in Fig. 2- 4. Its structure

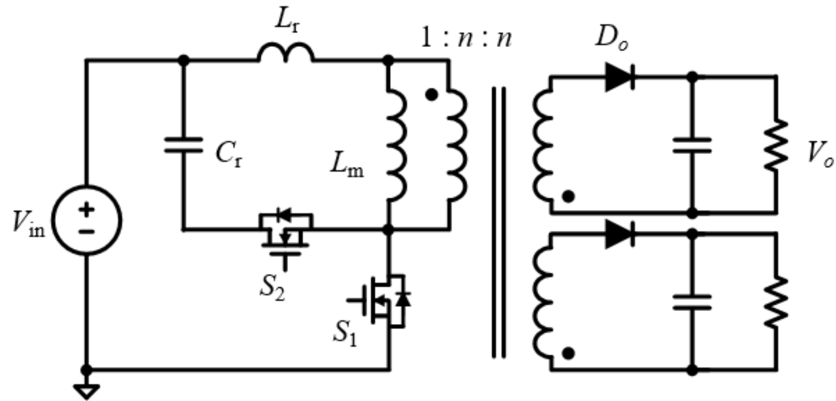


Fig. 2- 4. Active-clamp flyback converter.

is simple; it is composed of the conventional flyback converter with an additional clamping circuit consisting of a resonant capacitor and auxiliary swtich. The resonant capactior recycles the transformer leakage energy and it helps the primary devices achieve soft switching. ZVS turned-on can be achieved in all condition by selecting sufficient leakage inductance. The voltage stress and current stress are relatively low. Because of the above advantages, ACF topology is selected, based on its better performance in both power density and efficiency.

The design flow diagram of the wide-input-voltage ACF converter is illustrated in Fig. 2- 5. As shown, the process is partitioned into three iterative steps, namely the converter, circuit, and component levels. As seen in the figure, the converter level sets the main sweeping loop. The input voltage V_{in}, which affects the converter loss, size, and component selection, is the main variable being swept from 8.5 V to 28 V. For a given V_{in}, the circuit level design is then performed. Simulation and analytical models are used at this stage to obtain the component values (e.g., clamping capacitance C_r, leakage inductance L_r, magnetizing inductance L_m, and effective turns ratio n_e), as well as the different operation parameters (e.g., current flowing through components and voltage across components). All design loops follow the constraints of the converter operational requirements, such as ZVS realization, controller duty-cycle range, core loss density

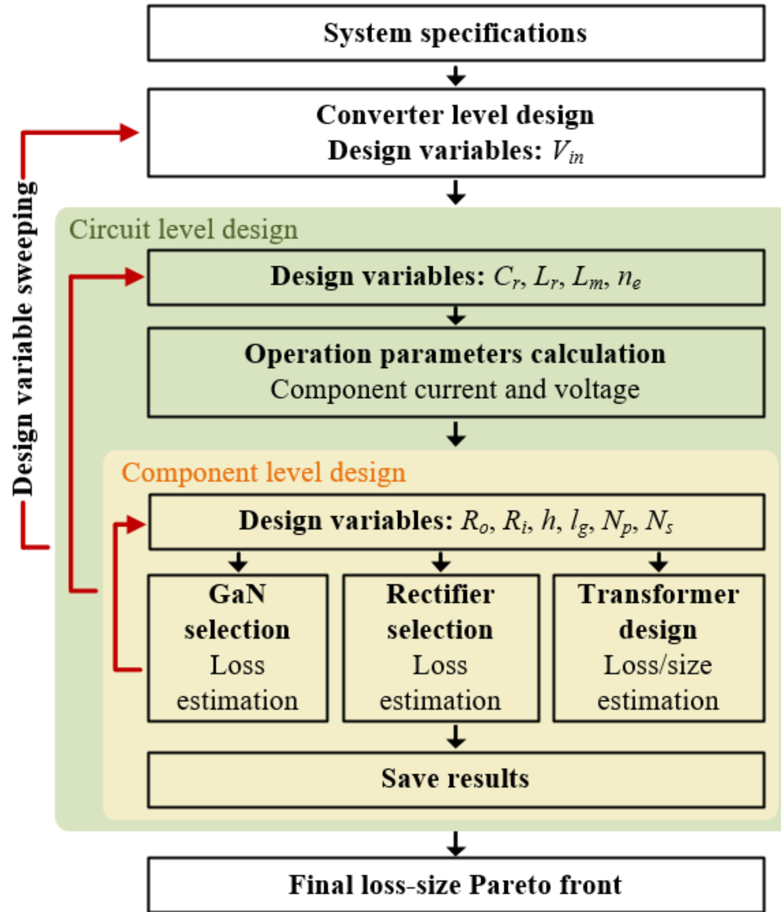


Fig. 2- 5. Wide-input-voltage ACF converter design procedure.

limitation, etc. The results are then fed to the component level design, where GaN devices, rectifier diodes, and the ACF transformer are selected and designed.

Given that the size of the GaN device and diode candidates considered are all below 7 mm^3, only the ACF transformer was taken into account for the converter size estimation. Lastly, all possible combinations in the design space are swept, mapping the corresponding performance space in terms of power density and loss, establishing the Pareto front of optimal solutions between these two design variables.

2.2.2 Operation mode and turns ratio selection

There are two operating modes in the ACF converter: One is the Critical Conduction Mode

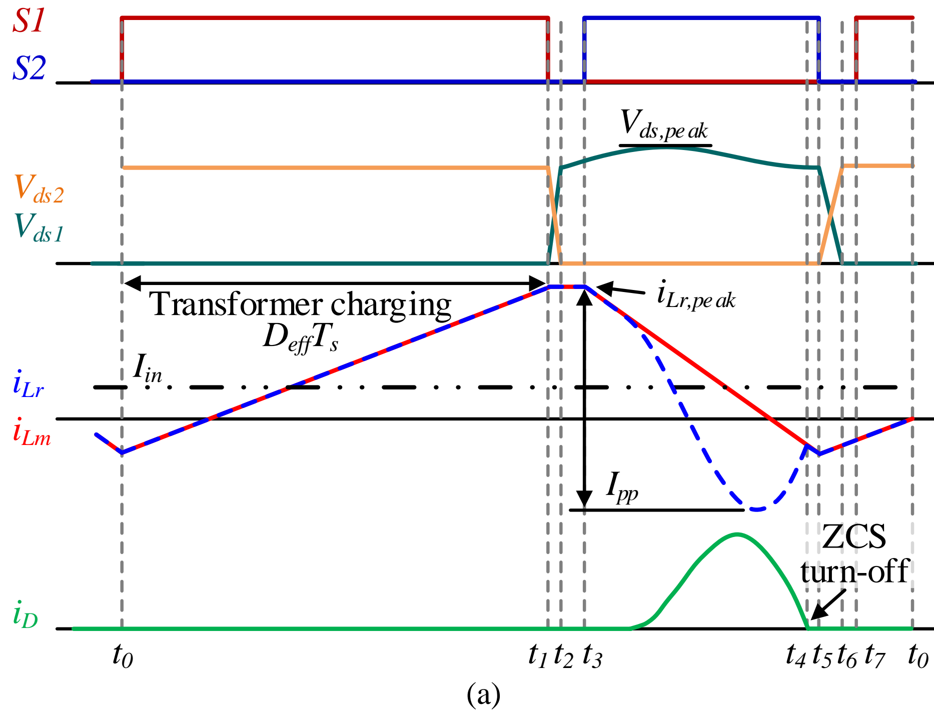
(CRM), and the other one is the Continuous Conduction Mode (CCM). CRM allows the secondary diodes to be turned off under zero-current switching (ZCS) at the expense of higher conduction loss and voltage stress of the primary devices. On the contrary, the current and voltage stress in the CCM operation is much smaller, but the ZCS operation of the secondary rectifier diodes is lost. Therefore, a tradeoff exists between the device's conduction loss and the diode's reverse-recovery loss. At lower voltages, the conduction loss of the primary switches dominates due to the higher current. As the input voltage increases, the reverse-recovery loss of the rectifier diodes plays the leading role. As a result, the selection of the operating mode is difficult.

The main waveforms of CRM and CCM of ACF converters are shown in Fig. 2- 6. The detailed operations are well documented in [94]-[96]. The key difference between these two operation modes is that the magnetizing inductance current i_{Lm} in CRM becomes negative for a portion of each switching cycle, while i_{Lm} never reverses its direction. The boundary condition between these two operating modes is when the minimum i_{Lm} is equal to zero.

$$i_{Lm} = \frac{P_{in}}{D \cdot V_{in}} - \frac{D \cdot V_{in}}{2f_s(L_r + L_m)} \tag{2. 1}$$

where P_{in}, V_{in}, D, f_s, L_r and L_m are input power, input voltage, duty cycle, switching frequency, leakage inductance, and magnetizing inductance, respectively. By properly designing L_r and L_m, the operating mode can be selected. Since the converter performance changes with the input voltage, multiple simulations under different input voltages should be conducted and compared. Because the active components have a much lower rated temperature compared to other components, it is more importation to restric the active component loss. Therefore, it will be used to select the operating mode and transformer turns ratio.

The active component loss at $n = 1$, $n = 1.5$, and $n = 2$ are shown in Fig. 2- 7. The range of the



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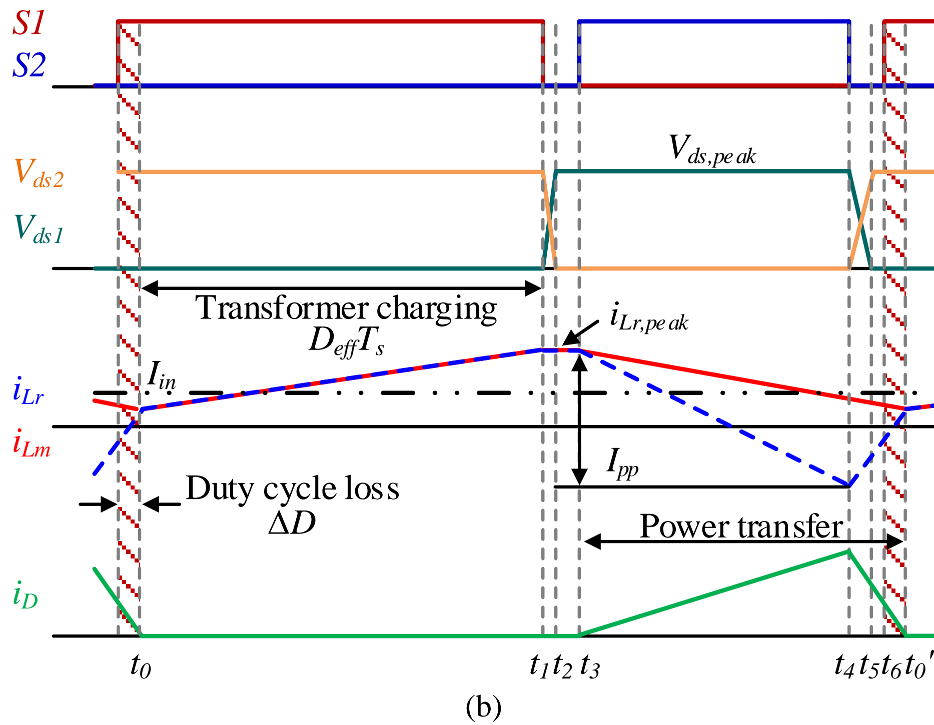
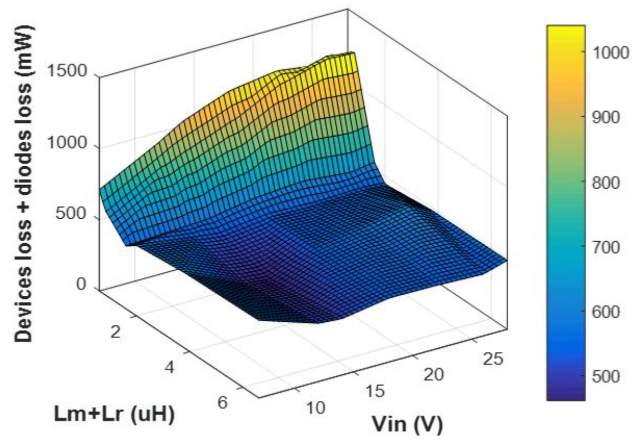


(b)

Fig. 2- 6. Main waveform of (a) CRM operation, and (b) CCM operation.



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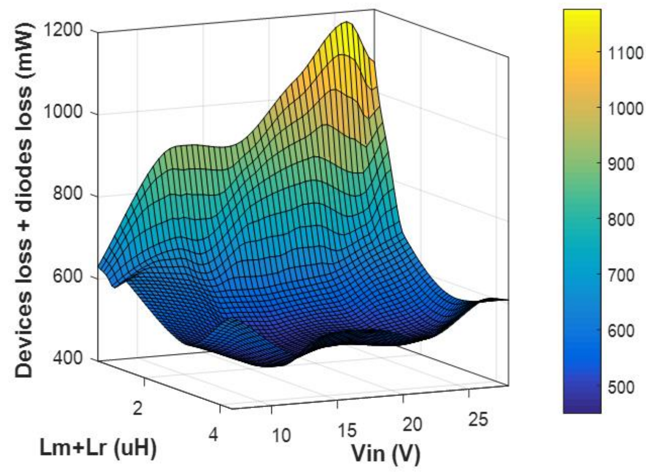

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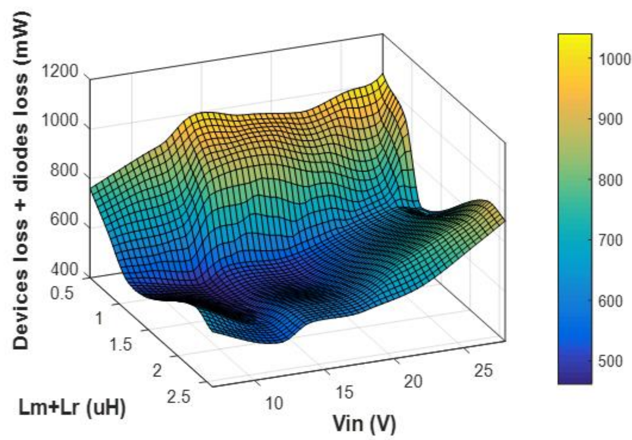


(c)

Fig. 2- 7. Active components with different inductance and input voltage at (a) n=1, (b) n=1.5, and (c) n=2.

transformer ratio is determined by the controller maximum duty cycle and the ZVS requirement. It is found that the loss increases drastically when the magnetizing inductance L_m and leakage inductance L_r decrease. The loss is caused by the conduction loss of the primary devices because of the large current ripple. When the magnetizing inductance L_m and leakage inductance L_r become large enough, the device loss is restricted thanks to the smaller current ripple, and the diode loss is more dominating. Therefore, the total loss starts to increase slightly resulting from the growth of the diode loss. Based on this analysis, CCM is selected.

The ZVS realization is more challenging in CCM. Unlike CRM, only the leakage inductance participates in discharging the output capacitances of the primary device (C_{oss} during dead time). Therefore, the leakage inductance should be sufficient. As shown in Fig. 2- 8, the rectifier diodes are not ideal, and their junction capacitance C_j take part of the leakage energy. The larger the turn ratio n, the more required energy from the diodes. However, if the turns ratio is too small, the required duty cycle range will be beyond the controller's capability. The transformer size, efficiency, and voltage gain should be effectively balanced when selecting its turns ratio.

According to Fig. 2- 7, it is found there is a dramatic change of the active component loss with

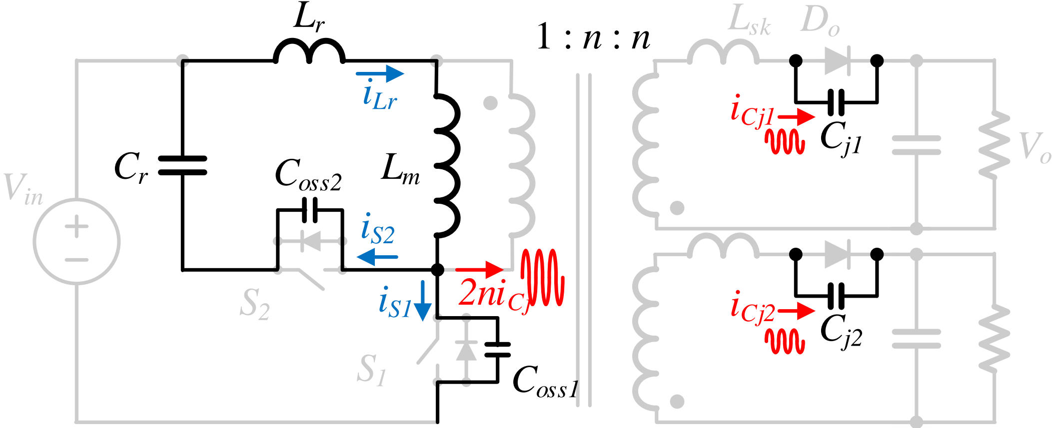


Fig. 2- 8. Operation during dead time period.

different inductances, while it changes slightly with the input voltage. The simulation results at nominal voltage $V_{in,nom} = 12$ V are used to select the transformer turns ratio. The simulated results at nominal voltage are illustrated in Fig. 2- 9. As seen, $n = 1$ has a lower overall loss and wider design range compared with $n = 1.5$ and $n = 2$; thus, it is selected.

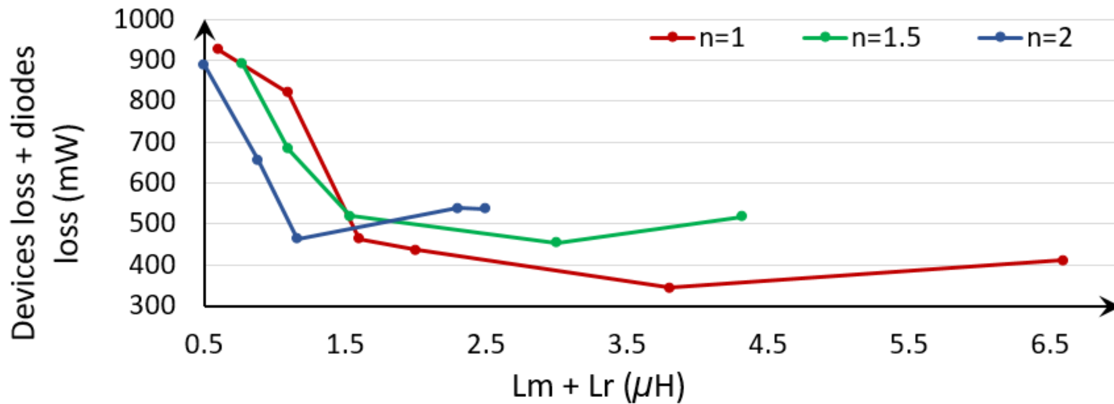


Fig. 2- 9. Simulated loss of active components with different inductance and turns ratio at nominal input voltage.

2.3 PCB-embedded transformer design

2.3.1 Transformer structure

The proposed transformer structure is shown in Fig. 2- 10. As shown, the toroidal core is fully embedded into the PCB material. The top and bottom sides of the windings are laid out as PCB traces and the vias construct the vertical connection between the traces. The air gap with a length of l_g locates in the middle of the two secondary windings to ensure a symmetric layout so that it provides identical inductances and balanced output voltage for the two loads. The top and the front view of the transformer are shown in Fig. 2- 11. R_i, R_o, h defines the inner radius, outer radius, and height of the magnetic core respectively. d_w describes the distance between the winding vias and the core. This parameter is given by the PCB manufacturer, and it must be at least 0.5 mm to

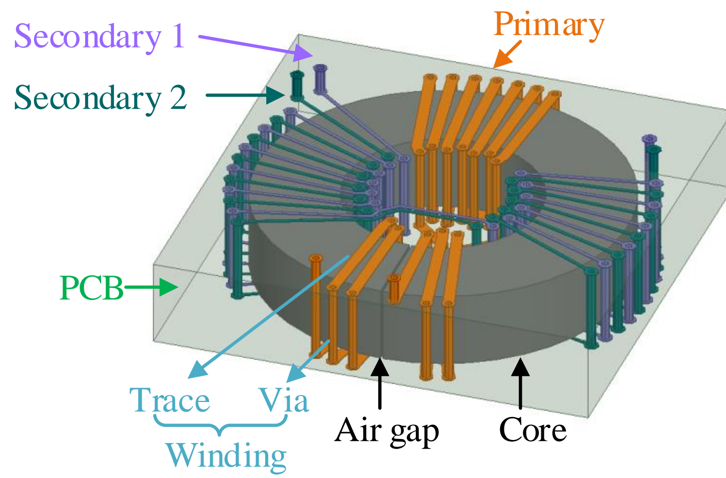
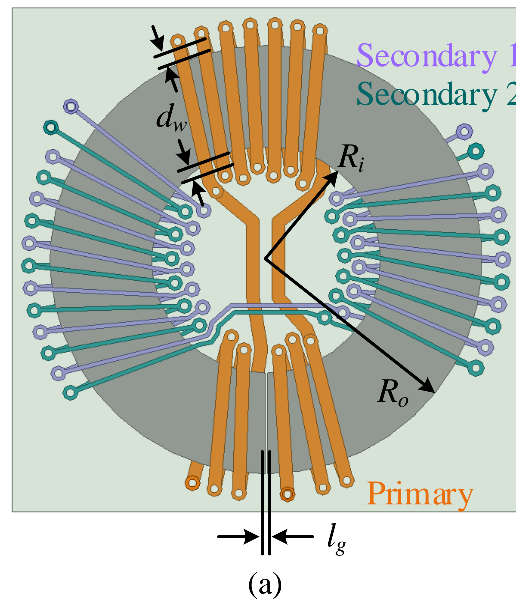
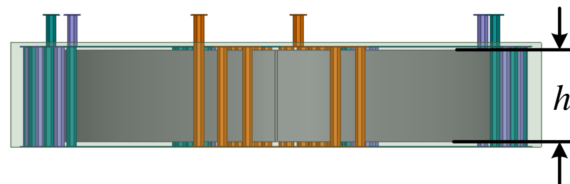


Fig. 2- 10. PCB-embedded transformer structure.



(a)



(b)

Fig. 2- 11. (a) Top and (b) side view of the PCB-embedded transformer.

ensure that via-holes will not hit and break the core during fabrication. The loose structure of the windings inevitably leads to the large leakage inductance. This is because part of the magnetic flux goes into the surrounding PCB material instead of circulating in the core [97]. Efforts should be made to control the leakage inductance due to the aforementioned design constraints. Interleaving and partial interleaving are well known techniques used to reduce leakage inductance [98]; they help relieve voltage stress on devices and increase converter voltage gain. The drain-source voltage V_{ds} of the devices are given by (2. 2).

$$V_{ds} = V_{in} + \frac{V_o + V_{sk}}{n} + \frac{2L_r f_{sw} P_{in}}{V_{in} D_{eff}(1 - D_{eff})} \tag{2. 2}$$

where V_{sk} is the voltage across the secondary leakage inductance L_{sk}. According to (2. 2), V_{sk} should be minimized because it helps decrease V_{ds}. A smaller L_r is preferred for the same reason; yet, it should be sufficient to achieve ZVS in all conditions. To this end, the perfect-interleaving configuration is adopted between the two secondary windings while partial-interleavaing configuration is adopted between the primary winding and secondary windings. As illustrated in Fig. 2- 11 (a), secondary 1 and secondary 2 are perfectly interleaved and grouped together partially interleaving with the primary winding.

In terms of the core material selection, P61 from ACME is chosen for its high curie temperature of 280 °C and low core loss density of 150 kW/m^3 at 50 mT, 100 °C, and 1 MHz. The TU-872 SLK from TUC, Taiwan, is selected for its high glass transition temperature T_g and its coefficient of thermal expansion (CTE) to ACME.

2.3.2 **Optimization constraints**

Unlike the CRM operation where the magnetizing current reverses its direction for a portion of each switching cycle and helps to achieve soft switching, ZVS realization in the CCM operation

becomes more difficult. Only the leakage inductance participates in discharging the output capacitances of the primary device (C_{oss}) and the junction capacitances of the rectifier diode (C_j). To achieve soft switching, the leakage inductance energy E_r should be larger than the capacitance energy E_c at time instant t_4 (when S2 is turned off) show in Fig. 2- 6 (b) in all conditions [95]:

$$E_r \geq E_c \,|_{@S2\ turn\ off}$$

$$E_r = \frac{P_{in}^2 L_r}{D_{eff}^2 V_{in}^2} + \frac{D_{eff}^2 V_{in}^2 L_r}{4 f_{sw}^2 (L_m + L_r)^2} + \frac{P_{in} L_r}{f_{sw}(L_m + L_r)}$$

$$E_c = C_{oss}\left(V_{in} + \frac{V_o}{n_e}\right)^2 + 2C_j (n_e V_{in} + V_o)^2 \qquad (2.\ 3)$$

The difficulty in solving (2. 3) is the fact that the resonant capacitor voltage (V_{Cr}) is a function of the value of L_r. However, in a practical design situation, the resonant inductor voltage at t_4 is relatively small compared to (V_{in} + V_o/n_e). Therefore, (2. 3) can be solved for an approximate value of $V_{Cr} = V_o/n_e$.

Apart from the ZVS realization, the turns ratio range is also restricted by power density. The total turn number of the proposed transformer equals to $(1+2n_e)N_p$, where N_p is the turn number at the primary winding. A slight increase in the turns ratio significantly augments the total turns and easily exceeds the maximum turns that the window area can handle. However, it is a key variable to achieve the desired output voltage. The turns ratio can be increased by reducing the primary turns, but the efficiency is compromised. The transformer size, efficiency, and voltage gain should be effectively balanced when selecting its turns ratio.

To provide sufficient voltage gain, the designed duty cycle D for switch S_1 should not exceed the digital controller capability. The maximum duty cycle in this paper is 90 %, which is the limit of the current-mode PWM controller UCC2803 from Texas Instruments [100]. In CCM operation, duty-cycle loss is significant at low voltages. Specifically, when the gate signals of the next

switching period arrive, the leakage inductance current is at its negative peak value—and largely different to the magnetizing inductance current. During this period, switch S_1 is turned on, but the ACF transformer is not charged by the input. With the addition of L_r, the effective duty cycle D_{eff} (as defined by the charge cycle of the ACF transformer) is less than S_1 switch duty cycle D as shown in (2. 4), where f_{sw} and ΔD is switching frequency and duty-cycle loss. In the case under consideration, to achieve ZVS in all conditions, the leakage inductance has to be at least 1.1 μH, which leads to a 9 % ΔD at Low-Line (LL) voltage ($V_{in,LL}$). Accordingly, the duty cycle needed can easily exceed the controller capability.

$$D_{eff} = \frac{V_o(L_m + L_r)}{n_e L_m V_{in} + V_o(L_m + L_r)}$$

$$\Delta D = \frac{1}{D}\frac{2L_r P_o f_{sw}}{\left(V_{in} + \frac{V_o}{n_e}\right)V_{in}}$$

$$D = D_{eff} + \Delta D \tag{2. 4}$$

In conclusion, constraints resulting from the wide-input-voltage requirements lead to a limited

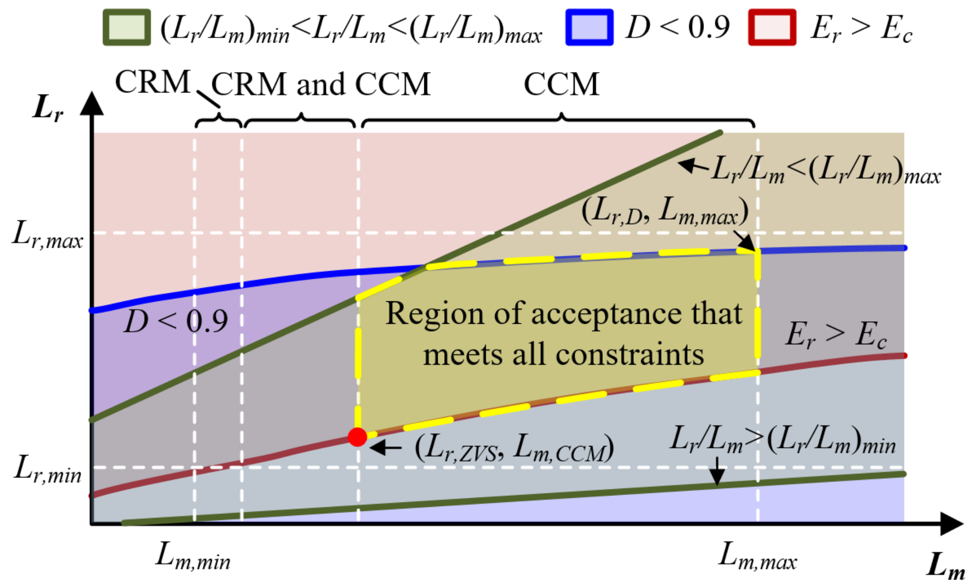


Fig. 2- 12. Region of acceptance of a 10 W, dual-output GDPS with an input range of 8.5 V to 28 V.

design space for the ACF transformer. The region of acceptance for a 10 W, dual-output, PCB-embedded transformer GDPS with a targeted input range of 8.5 V to 28 V is illustrated in Fig. 2-12, where $L_{r,max}$, $L_{r,min}$, $L_{m,max}$, and $L_{m,min}$ are the achievable maximum and minimum leakage and magnetizing inductances determined by the power density and winding structure. The controller's duty cycle capability, ZVS realization, operating mode, and the power density requirements form the barriers to the region of acceptance. The constraints are summarized in Table 2. 1, where $L_{r,ZVS}$, $L_{r,D}$, and $L_{m,CCM}$, are the minimum leakage inductance to achieve ZVS, the maximum leakage inductance that will not exceed the controller duty cycle capability, and the minimum magnetizing inductance to achieve CCM operation.

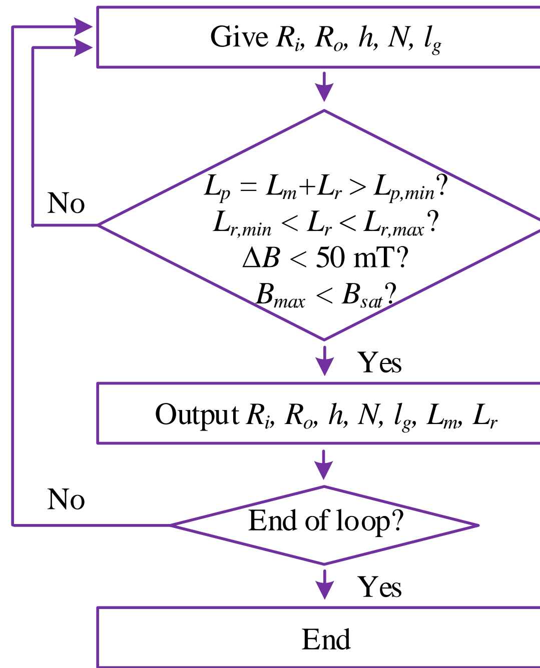
Table 2. 1. Constraints of A 10-W, Wide-Input-Voltage ACF Operating in CCM Operation

Parameter	Value	Constraint
$L_{r,ZVS}$	1.1 μH	ZVS realization
$L_{r,D}$	1.6 μH	Controller's duty cycle capability
$L_{m, CCM}$	7.9 μH	CCM Operation mode requirement
$L_{m, max}$	20.1 μH	Power density restriction

2.3.3 **Multi-objective optimization and results**

The MDO optimization process for transformer is depicted in Fig. 2- 13. There are four optimization variables: the inner radius R_i, outer radius R_o, height h and the primary/secondary turn number N. To attain the targeted power density, the R_o and h are limited to 8.5 mm and 4 mm, respectively. The optimization process consists of three steps. The first step is to run the sweeping program shown in Fig. 2- 13 (a) and collect all of the designs within constraints. $L_{p,min}$, $L_{r,min}$, and $L_{p,max}$ are required by the CCM operation, ZVS, and controller duty cycle, respectively. ΔB is the peak-peak flux density and is set to 50 mT to restrict the core loss. The maximum flux density B_{max} should not exceed the saturation flux density B_{sat} of the core material. This process ends when all

of the possible designs satisfying the targeted power density have been swept. The second step is the loss minimization described in Fig. 2- 13 (b). During this process, the loss of all designs collected in Fig. 2- 13 (a) was analyzed. With the given dimensions and turns, 3D models are built



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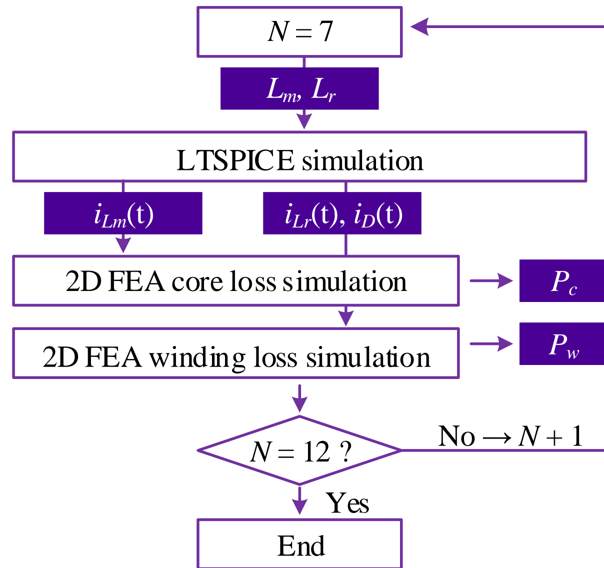


(b)

Fig. 2- 13. MDO optimization process: (a) sweeping program, and (b) loss minimization.

and used in an FEA simulation to attain the transformer properties, including L_r, L_m, and L_{sk}. SPICE models are used to build the simulation circuit, by which the device loss and the diode loss are given. The circuit simulation also provides the current waveforms: i_{Lm}(t) for FEA core loss simulation, and i_{Lr}(t) and i_D(t) for FEA winding loss simulation. This step ends when the losses of all designs collected in Fig. 2- 13 (a) have been analyzed, and the one with the lowest loss is selected. The last step is to check the transformer input-output capacitance C_{io}. The model is shown in Fig. 2- 14 (a) and its equivalent circuit is provided in Fig. 2- 14 (b). Since the The C_{io} is mainly determined by the winding structure and core material, the simulation model is simplified by removing the air gap. The C_{io} consists of four parts: the core resistance R_c, primary-secondary winding capacitance C_{ps}, primary winding-core capacitance C_{pc}, and secondary winding-core capacitance C_{sc}. Q3D simulation is done to estimate the C_{io}.

With the aforementioned models, the optimized design can be given. The designed R_o, R_i, h, l_g, and N are 4.5 mm, 8.5 mm, 3.5 mm, 0.1 mm and 12, respectively. A hand-wound transformer shown in Fig. 2- 15 is built to evaluate the design. Table 2. 2 enumerates the simulation results and the measured results with a hand-wound transformer, providing a good accuracy of the models.

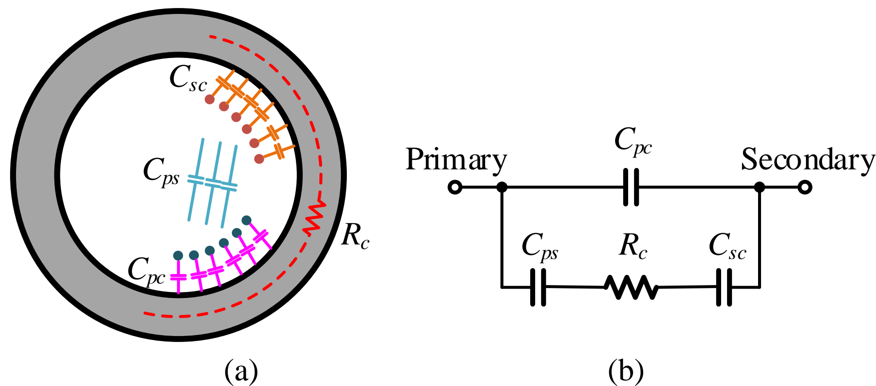


Fig. 2- 14. (a) Simplified 2D Cio model, and (b) its equivalent circuit.

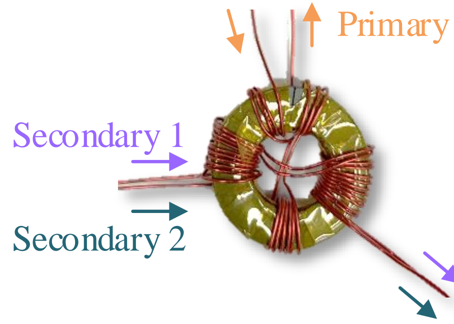


Fig. 2- 15. Hand-wound transformer with the proposed winding structure.

Table 2. 2. Optimized Transformer Properties

Parameter	Simulated Value	Measured Value
L_r	1.09 μH	1.43 μH
L_m	18.67 μH	18.5 μH
L_{sk}	108.4 nH	143 nH
n	1.04	0.98
C_{io}	1.63 pF	2.95 pF

2.4 Hardware assembly and qualification

2.4.1 **Hardware assembly**

With the designed circuit and transformer properties, the primary devices and the secondary diodes can be selected based on the circuit simulation with SPICE models. Considering the maximum voltage of the two devices is simulated to be less than 80 V, the EPC GaN devices with more than 100 V ratings are considered. Small ON-state resistance R_{ds}, output capacitance C_{oss} and total gate charge Q_G are preferred to minimize the loss. Table 2. 3 enumerates the candidates for S1 and S2. Each of them has five candidates; there are 25 combinations in total. The simulated device loss of these 25 combinations in full input range are shown in Fig. 2- 16. Three curves with the lowest loss at low line $V_{in,LL}$ = 8.5 V, nominal voltage $V_{in,nom}$ = 12 V, high line $V_{in,HL}$ = 28 V are highlighted. The EPC2007C and EPC2012C are selected for S1 and S2, respectively, for their

Table 2. 3. Device Candidates and Their Properties

	Part #	V_{ds} (V)	I_{ds} (A)	R_{ds} (mΩ)	Q_G (nC)	C_{oss} (pF)
S1	EPC2007C	100	6	30	2.2	110
	EPC2016C	100	18	16	4.5	210
	EPC2052	100	8.2	10	3.6	192
	EPC2212C	100	18	13.5	4	238
	RPC2012C	200	5	100	1.8	64
S2	EPC2007C	100	6	30	2.2	110
	EPC2016C	100	18	16	4.5	210
	EPC2052	100	8.2	10	3.6	192
	RPC2012C	200	5	100	1.8	64
	RPC2019	200	8.5	50	2.5	110

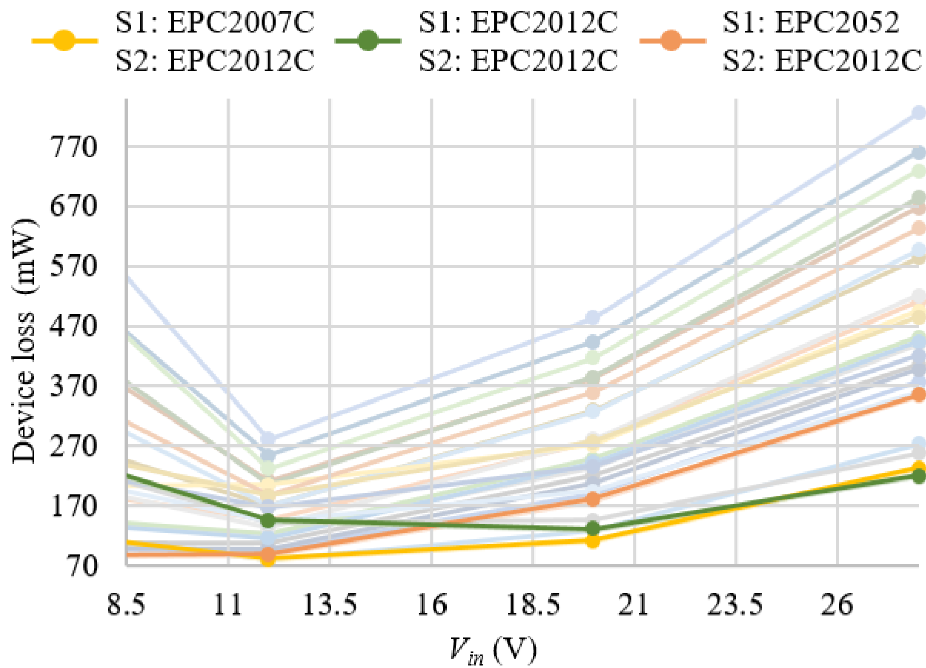


Fig. 2- 16. Device loss simulation results in full input voltage range.

lower overall loss in full input range. Furthermore, the Si Schottky diode DFLS1100 is selected as the rectifier diodes. The 200 V, half-bridge driver, LGM1210 from Texas Instruments, is used to drive S1 and S2. The high stability isolated error amplifier, ADuM3190 from Analog Devices, is chosen as the isolator. The low-power BiCMOS current-mode PWM controller, UCC2803 from Texas Instruments, is selected for its wide duty cycle range.

The converter layer structure is shown in Fig. 2- 17. There are seven layers in total: layers 1 to 4 are active layers; layers 5 and 6 are winding layers; layer 7 is the terminal layer. Correspondingly, there are three groups of vias in the converter. The diameters of there vias are determined by the board thickness. Buried vias are used in both active layers and transformer vias. Active layers and transformer layers are connected by the termianl vias.

Since the dual-output GDPS proposed in this paper is for automobile inverters with a DC voltage of 400 V, the primary-secondary side and secondary-secondary side distances must satisfy the creepage distance requirements at 600 V; thay are 3 mm for the exposed pads and 1.2 mm for the external layers as labeled in Fig. 2- 18. Apart from the creepage distance requirements, the copper areas for the devices and diodes on the top layer should be designed as large as possible to

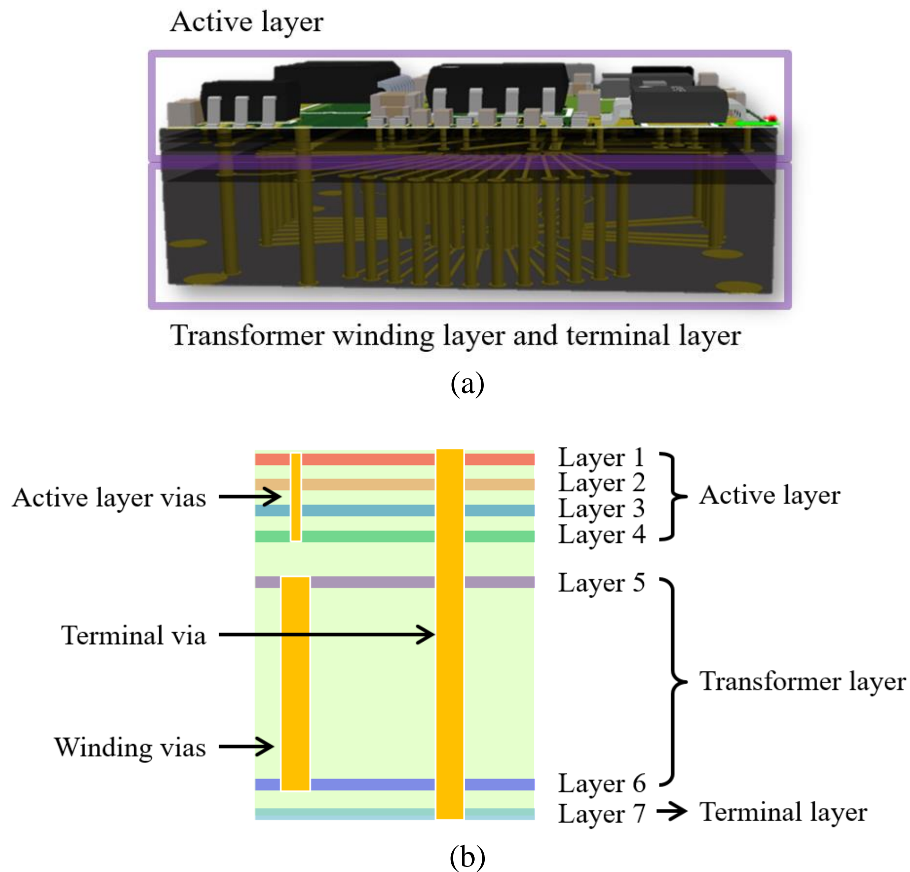


Fig. 2- 17. (a) Front-view of the 3D model, and (b) converter layer structure.

dissipate the heat.

The final GDPS is built and shown in Fig. 2- 19. The length, width, and height of the GDPS are 21 mm, 20 mm, and 7.35 mm, respectively. The volume of the GDPS is 0.188 in^3, representing a power density of 53.2 W/in^3. The test prototype is shown in Fig. 2- 20. A two-layer test board with a dimension of 60 mm x 45 mm is designed to place the terminals and test pins. No copper areas are used so they will not serve as heat sinks and affect the GDPS thermal performance.

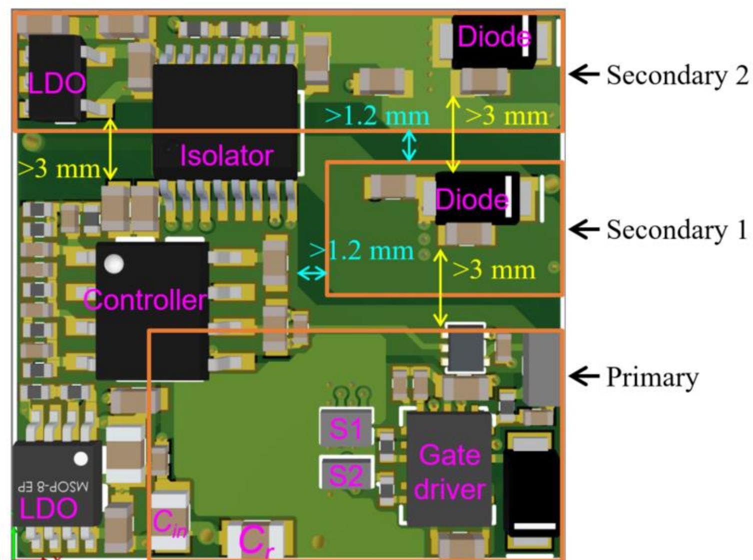


Fig. 2- 18. 3D top view of the GDPS.

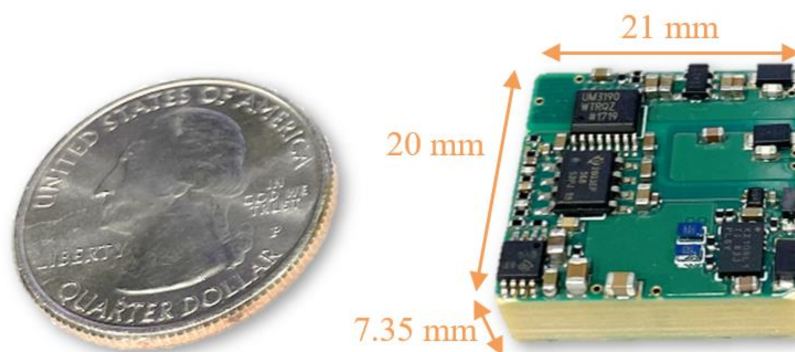


Fig. 2- 19. Gate-drive power supply

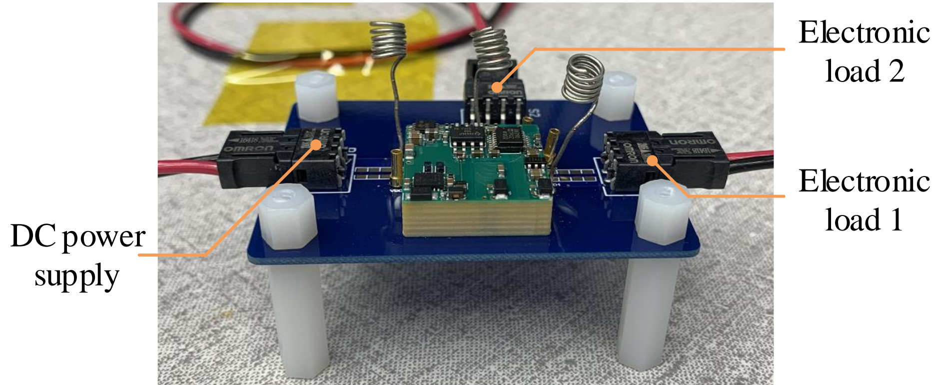


Fig. 2- 20. Testing prototype.

2.4.2 **Experimental results**

The waveforms at nominal input in full load condition are shown in Fig. 2- 21. The transformer current, drain-source voltage of the S1, gate signals of S1 and S2 are labeled as i_{Lr}, $V_{ds,S1}$, $V_{gs,S1}$, and $V_{gs,S2}$, respectively. Secondary 1 outputs 24.1 V and secondary 2 outputs 24.14 V, showing a good balance between the two loads and providing efficiency of 89.7%. ZVS operation of both devices is achieved; their body diodes conduct reversely before the gate signals arrive. Fig. 2- 22 provides the efficiency curve over the whole input range. The highest efficiency exists at nominal voltage V_{in} = 12 V. The efficiency drops due to the higher device conduction loss,

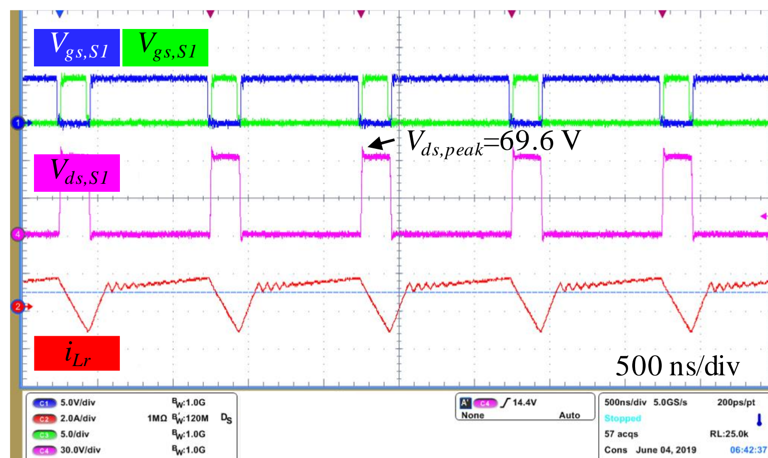


Fig. 2- 21. Experimental testing results in dual-output, full load condition at nominal voltage V_{in} = 12 V. V_{o1} =24.1 V, V_{o2}=24.1 V, η=89.7%.

transformer winding loss at low voltages, and the higher diode reverse-recovery loss at high voltages.

To validate the thermal performance of the GDPS, high-temperature testing is conducted using a thermal chamber. During the test, the prototype was placed inside the thermal chamber and the ambient temperature T_A was increased from 50°C to 115°C gradually. The case temperature T_c of the transformer, S1, diodes, and secondary LDO were measured using thermocouples. The GDPS was operated for more than 30 minutes at each measuring point to ensure that the junction temperature T_j of the components was stabilized. The measured T_c under the low line and high line condition are shown in Fig. 2- 23. The calculated junction temperature of the S1, diodes and secondary LDO at the highest ambient temperature in low line ($T_{j,LL}$) and high line ($T_{j,HL}$) condition are summarized in Table 2. 4.

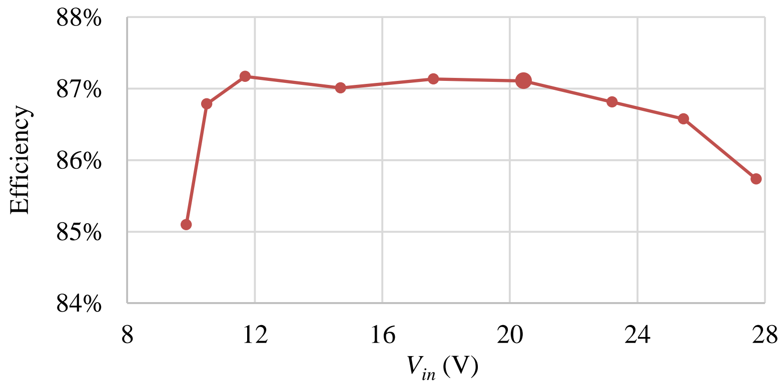
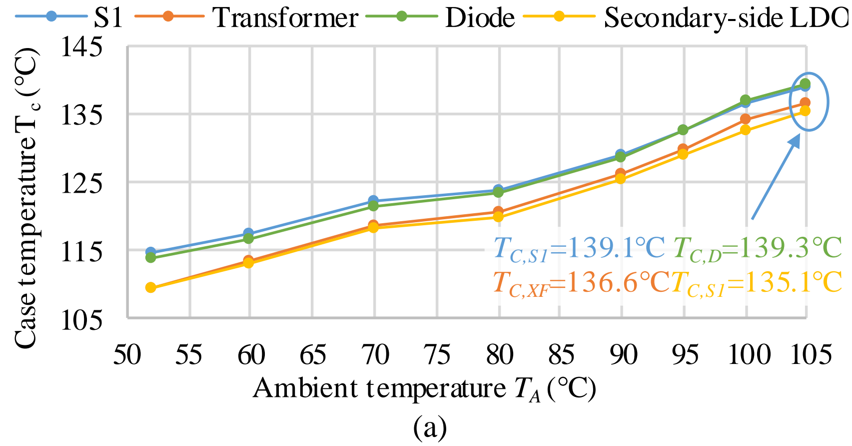


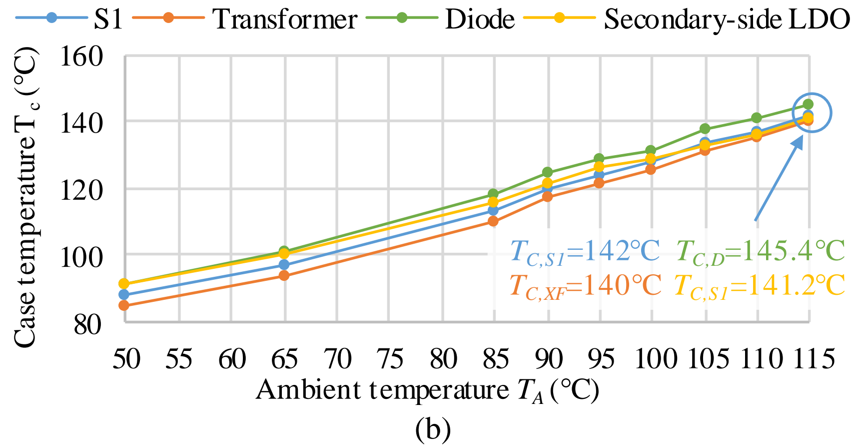
Fig. 2- 22. Efficiency over full input voltage range.

Table 2. 4. Calculated Junction Temperature

	$T_{j,max}$ (°C)	R_{jc} (°C/W)	$T_{j,LL}$ (°C)	$T_{j,HL}$ (°C)
S1	150	3	139.7	142.6
D_o	175	21	142.0	148.1
LDO	150	210.4	142.7	148.8



(a)



(b)

Fig. 2- 23. Case temperature T_c of S1, transformer, diode and secondary side LDO at (a) low line, and (b) high line.

2.5 Summary and conclusion

This chapter presents the design of an integrated GDPS with a PCB-embedded transformer for WBG based automotive applications. ACF topology is selected for it shows a good tradeoff between simplicity and high efficiency. GaN devices are selected for their small size and higher operating frequency. The PCB-embedded technique is utilized and it highly improves the power density. A prototype is built. It achieves a power density of 53.2 W/in^3, a wide-input-voltage range of 9.7 V to 28 V, a C_{io} of 9.7 pF, a peak efficiency of 89.7 % and a high operating temperature of

105 °C and 115 °C at low line and high line respectively.

The utilization of GaN devices contributes to the power density and efficiency, and they show an excellent thermal performance, thanks to their low ON-state resistance R_{ds} and output capacitance C_{oss}. Permeability degradation is found due to the mechanical stress in the fabrication process, significantly increasing the transformer winding loss and device conduction loss. Furthermore, the effect of the permeability degradation on core loss density is still under investigation. The above factors possibly lead to a higher temperature rise in the PCB-embedded transformer that restricts the operating temperature. A larger core or better core materials are needed to extend the operating temperature range or the input voltage range; otherwise, one of them must compromise to attain the targeted power density.

Chapter 3 Analysis of using PCB-embedded ferrite in transportation applications

3.1 Introduction

Nowadays, increasing the power density of power converters becomes one of the main driving forces in power electronics development. In converter design, magnetic components are key elements in achieving high power density because they take up most of the space. One promising approach to reduce their size and weight is the integration of magnetic components into printed circuit boards (PCBs). In this structure, the magnetic core is embedded into the multi-layer PCB. Traces and vias are used to build the windings. The transformer serves as a substrate carrying the rest of the circuit. The power density is effectively improved by removing the wasted space between the transformer and the other components.

Featuring high permeability and low core loss density, ferrite materials are widely used in both industry and academic groups. However, they exhibit magneto-mechanical properties that can deteriorate permeability when subjected to mechanical stress, such as the pressure applied during the PCB fabrication process. Specifically, the applied mechanical stress generates local anisotropy in the sintered spinel grains such that minimum energy occurs when the magnetization is perpendicular to the applied stress in initially isotropic materials [78]–[81]. Stronger applied fields will then be required to rotate the magnetization through the stress direction, resulting in higher coercivity and reduced permeability [82]. This occurs during the encapsulation [101]-[103] and lamination process [104]. In [82], it was revealed that the degradation in the permeability of encapsulated ferrites caused by commercial adhesive material could vary from 15–75 %. In [104], two transformers were built, and the inductances were compared before and after lamination,

showing an 84 % inductance drop. In [105], the effect of the mechanical stress on ferrites was investigated, and it showed a change in the shape of the magnetic hysteresis loop being proportional to the applied stress. Because of this, using ferrite materials in PCB-embedded applications brings uncertainties to the converter design and design failures might occur.

In this chapter, the permeability degradation in a PCB-embedded ferrite applications, and how it affects wide-input-voltage-range converter design is studied. Several PCB-embedded magnetic boards are fabricated to investigate its impact, based on which, correction factors are derived and applied to the modeling used in the multi-objective optimization (MDO) process. Prototypes with hand-wound and PCB-embedded transformers are built and compared, verifying that the improved design successfully achieves the targeted wide-input-voltage range. These are tested within a 10 W, dual-output, high power density (53.2 W/in^3), integrated ACF converter prototype built and based on GaN devices operating at 1 MHz.

3.1.1 **Permeability degradation in PCB-embedded ferrite**

Following the multi-objective optimization (MDO) procedure in 2.2, a 10 W integrated gate-drive power supply (GDPS) for wide-bandgap (WBG) based automotive applications was designed and assembled. The efficiency versus input voltage of the GDPSs with a hand-wound and PCB-embedded transformer are depicted in Fig. 3- 1. As seen, the GDPS with PCB-embedded transformer achieved a peak efficiency of 89.7 % and an input voltage range of 9.7–28 V, while the same unit operating with a hand-wound flyback transformer—instead of a PCB-embedded one—achieved 94 % peak efficiency, and it successfully met the 8.5–28 V input-voltage-range requirement. The efficiency reduction is caused by the permeability degradation in the PCB-embedded ferrite. The smaller inductance leads to a larger rms current, so the conduction loss of active component and transformer loss are increased. In addition, this phenomenon also changes

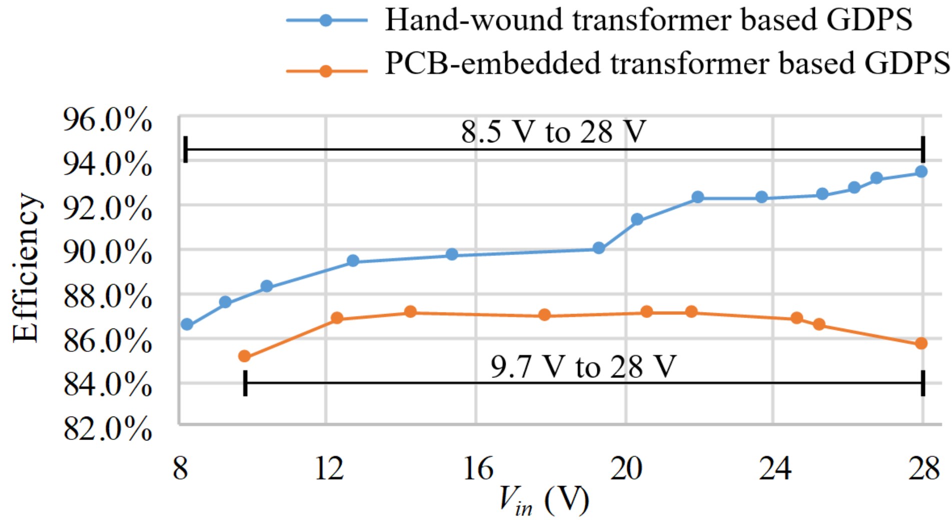
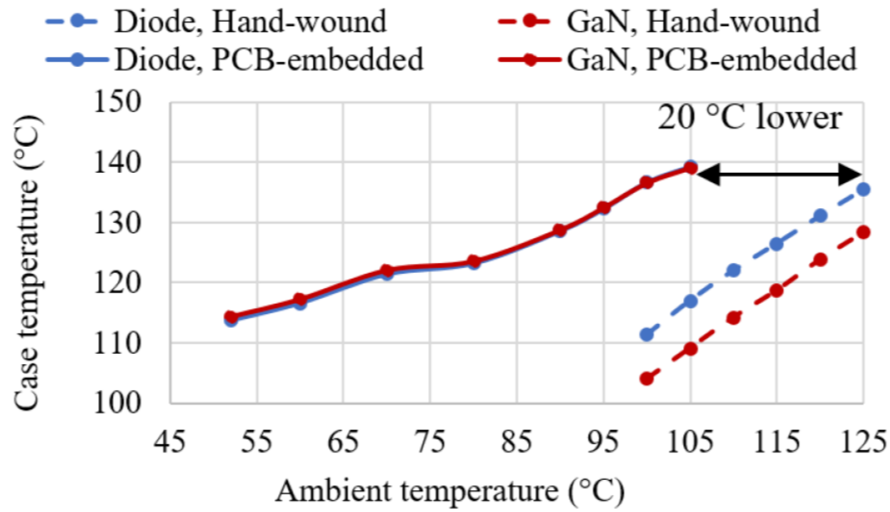


Fig. 3- 1. Efficiency comparison between hand-wound transformer based GDPS and PCB-embedded transformer based GDPS.

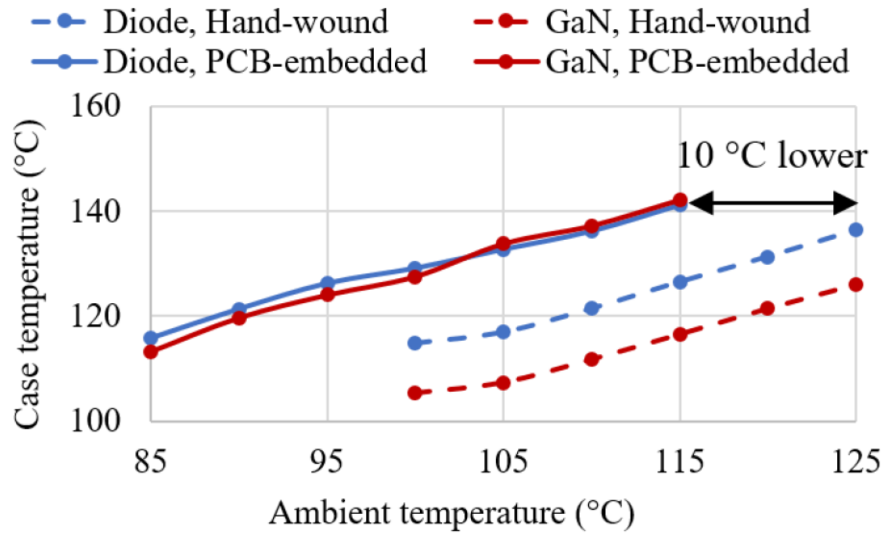
the inductance ratio in ACF transformer, which narrows down the input-voltage range.

The case temperature of active components of GDPSs with both hand-wound transformer and PCB-embedded transformer are also compared in Fig. 3- 2. The maximum operating temperature is reduced by 20 °C and 10 °C at LL and HL condition, respectively. The reduction is caused by the lower efficiency in the PCB-embedded transformer. Besides, the fr4 material has a relatively poorer thermal dissipation. When it is placed beneath the circuit, it acts like a heat source heating up the surrounding temperature. Therefore, the actual ambient temperature of the active components will be much higher.

The self-inductance of two hand-wound transformers and nine PCB-embedded transformers are measured and compared; all of which are depicted in Fig. 3- 3. As seen, the self-inductances of the two hand-wound transformers show similar value and match the optimization results; however, the self-inductances of the PCB-embedded transformers reveal a huge inductance reduction of up to 10.5 μH, which is 53% of the designed value. Apart from the inductance reduction, the nice PCB-embedded transformers present a larger inductance variation of 3.6 μH.



(a)



(b)

Fig. 3- 2. Case temperature comparison between GDPS with hand-wound transformer and PCB-embedded transformer at (a) LL, and (b) HL voltage.

The percentage changes between the nine PCB-embedded transformers, the hand-wound transformer, and the designed value are listed in Table 3. 1. This apparent performance degradation by the PCB-embedded transformer was the result of a mismatch between the designed transformer magnetizing inductances and the values ultimately attained. This mismatch, in turn, was caused by the degradation of the magnetic core permeability during the embedding process where the host

prepreg and core PCB materials are subjected to high temperature and pressure during the lamination process. On the other hand, the hand-wound transformer showed good matching with the target self-inductance and coupling coefficient values, as shown in Table 3. 1. The leakage inductance of the hand-wound transformer is 31 % higher than the designed, as well as the PCB-embedded transformer, due to its winding cannot be well fabricated as the design shape. The PCB-embedded technique can produce almost the same winding structure as designed.

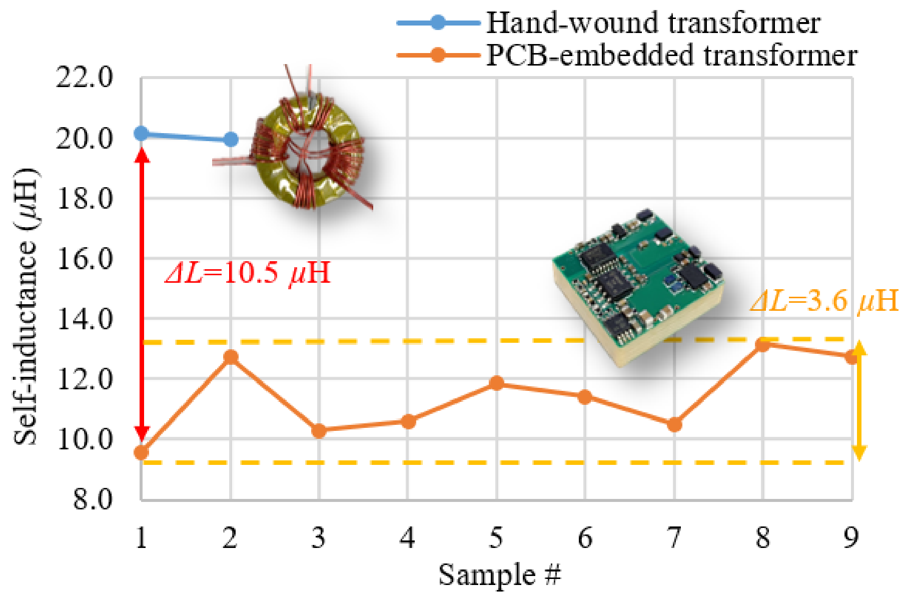


Fig. 3- 3. Permeability degradation due to the mechanical stress.

Table 3. 1. Properties Comparison between hand-wound and PCB-embedded transformer

Properties	Design	Hand-wound	Compared to Design	PCB-embedded									Compared to Design
L_p (μH)	19.8	19.9	+1 %	9.57	10.59	10.55	11.84	11.39	10.54	13.15	12.72	10.28	−52 % to −34 %
k_{12}=k_{13}	0.953	0.96	+1 %	0.93	0.937	0.938	0.945	0.944	0.938	0.95	0.95	0.93	−2.6 % to −0.3 %
L_r (μH)	1.09	1.43	+31 %	1.12	1.13	1.09	1.09	1.09	1.11	1.12	1.12	1.08	−0.9 % to +3.7 %
L_m (μH)	18.7	18.5	−1 %	8.45	9.46	9.46	10.75	10.3	9.43	12.03	11.6	9.2	−55 % to −34 %
n_e	1.04	0.98	−6 %	1.03	1.06	1.06	1.06	1.06	1.05	1.02	1.02	1.06	−2 % to +2 %
L_r/L_m	0.058	0.077	+33 %	0.133	0.119	0.115	0.101	0.106	0.118	0.093	0.097	0.117	+60 % to +129 %

3.1.2 **Embedding impact on automotive converter design**

In the design of power electronic converters and systems, design variables such as circuit topology, magnetic design, and control algorithm are selected, and the component values and control parameters are determined to fulfill system specifications and requirements. For each point in a multi-dimensional design space, after following a general system design flow, it will result in a single or multiple points in a multi-dimensional performance space depending on the number of available component-selection options [106]. In terms of the optimization process, Fig. 3- 4 graphically illustrates the effect of the PCB-embedded transformer where the blue dot in the design space (formerly an optimal design point per the MDO procedure developed), was instead mapped outside of the acceptable performance region. Had the impact on the transformer been known, this design point would have been discarded as one failing to meet the GDPS performance requirements, specifically due to the saturation of the controller duty cycle leading to a reduced input-voltage range.

The effect of the above is a reduction in the design space region as shown in Fig. 3- 5. Specifically, the increased L_r/L_m ratio lowered the upper boundary according to (2. 4), and the

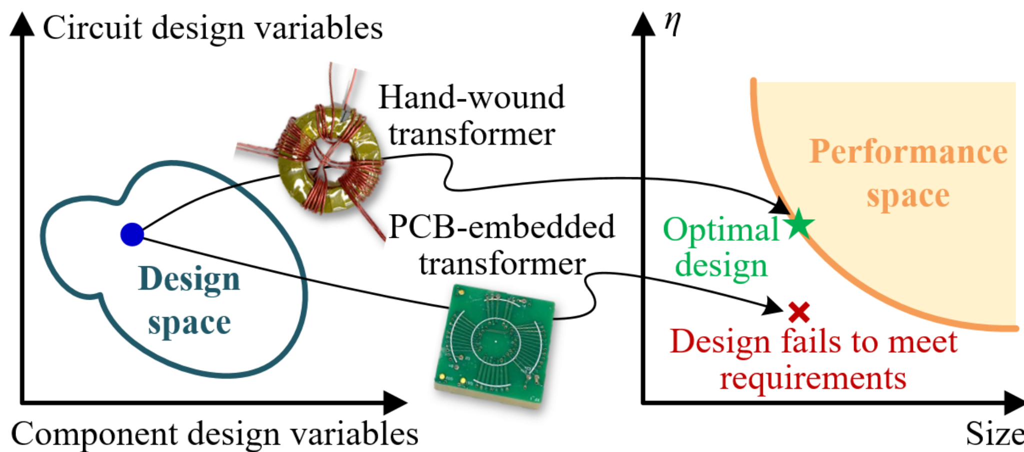


Fig. 3- 4. Multi-objective optimization: mapping from design space to performance space of hand-wound transformer and PCB-embedded transformer.

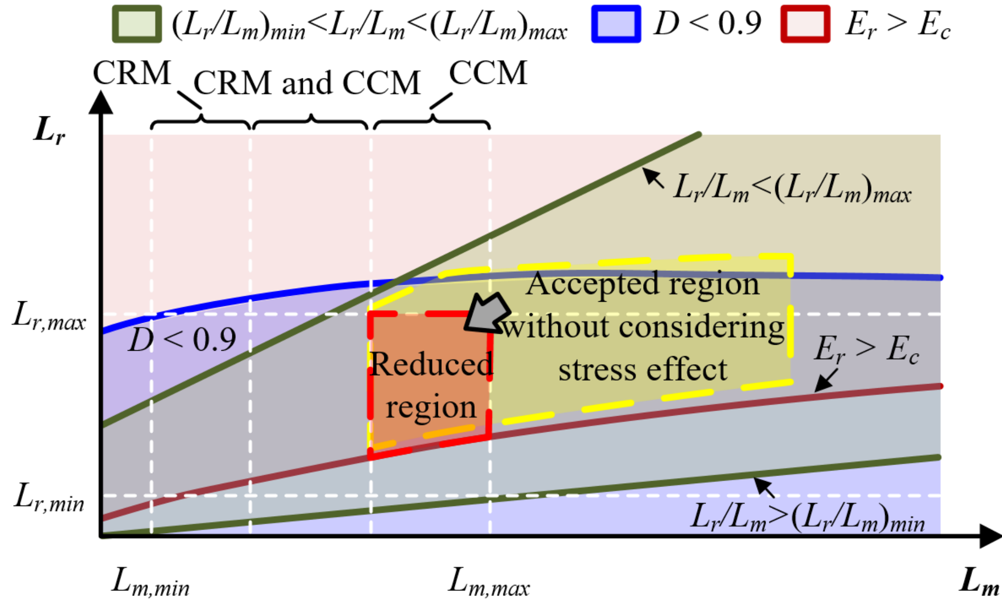


Fig. 3- 5. Reduced design region caused by embedding process.

drastic reduction in self-inductance (the sum of the leakage and magnetizing inductances) shortened the magnetizing inductance region, strongly reducing the design space as evinced in this figure. Further, the 34 % reduction in self-inductance increased the peak inductor current by 53 % and its ripple by 35 %, which leads to a 6.3 % reduction in peak efficiency. Nonetheless, the change in leakage inductance expanded the ZVS operating region.

In all, the permeability degradation is inevitable due to the large stress that the magnetic core is subjected to during the embedding process, especially in higher power applications requiring larger cores with bigger surfaces. Accordingly, the models used in the MDO process should account for this change, as will be discussed in the following section.

3.2 PCB-embedded magnetic board design and fabrication

Several boards with multiple PCB-embedded magnetic cores were fabricated to evaluate the change in the magnetic properties of the core material that results from the mechanical stress that they endure during the embedding process. The results are discussed hereinafter.

3.2.1 **Material and structure**

A 3-D model view of the PCB-embedded magnetic board is shown in Fig. 3- 6. Transformers or inductors can be constructed in these boards by inserting wires through the via holes. Each board contains four ferrite cores, all of them with the same dimensions. Four magnetic boards were built under increasing applied pressure, 100 PSI, 200 PSI, 350 PSI, and 450 PSI, with the purpose of measuring the effect on the leakage and magnetizing inductances, the coupling coefficient, the effective turns ratio, and the input-output capacitance under these conditions. The maximum applied pressure was 450 PSI, as the suggested maximum pressure for PCB fabrication is 350 PSI [107]. A magnetic board without lamination was also constructed to serve as the control group.

The GDPS in question targets a wide-temperature operation ranging from −40 to +125 °C. Accordingly, the glass transition temperature (T_g) of the PCB material candidates for this application should be high enough to ensure that the PCB, acting as host of the GDPS, does not transition from glass to the rubber-like state during the converter operation. In addition, given that ferrite cores are brittle, the Coefficient of Thermal Expansion (CTE) of the PCB material should be close to the ferrite chosen to avoid the cracking of the core during manufacturing or under repetitive power (and temperature) cycling [108]. For this purpose, the polyimide-based prepreg (P26) and core material (P96) for high temperature operation [109] from Isola was selected for the

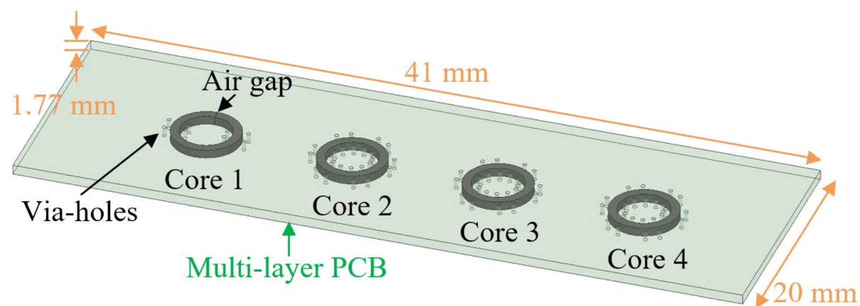


Fig. 3- 6. 3D model of the PCB-embedded magnetic board.

PCB construction. This material features T_g = 260 °C, X/Y-axis CTE of 13/14 ppm/°C, and Z-axis of 1.5 %.

Three popular ferrite materials, P61 from ACME, and ML91S and ML95S from Hitachi, were chosen for their high Curie temperature Tc (280 °C) and low power loss density Pv (≤ 250 kW/m3) at 1 MHz. Table 3. 2 shows the specifications of the ferrite cores in question as well as their physical dimensions. As shown in Fig. 3- 6, core 1, with an air gap of 0.1 mm, was designed to emulate the ACF ferrite core structure depicted in Fig. 3, featuring two-turn primary and secondary windings. Core 2, core 3, and core 4 had no air gap, and were used to build 12-turn inductors, seeking to assess the impact of permeability degradation caused by the embedding process while evaluating different magnetic materials. Further, since the input-output capacitance C_{io} is a key property of GDPS limiting the flow of common-mode (CM) currents to ground [110], 6-turn transformers with unity turns-ratio were also built using these cores to investigate the change in C_{io}.

Table 3. 2. Properties and dimensions of the ferrite cores

	Core 1	Core 2	Core 3	Core 4
Material	P61	P61	ML95S	ML91S
Tc (°C)	280	280	280	280
Pv @50mT (kW/m3)	150	150	250	110
OD (mm)	12	12	12	12
ID (mm)	9	9	9	9
H (mm)	1.5	1.5	1.5	1.5
lg (mm)	0.1	N/A	N/A	N/A

3.2.2 **PCB-embedded magnetic board lamination**

The lamination steps are illustrated in Fig. 3- 7. First, the PCB materials were cut in the shape of the ferrite cores. Then, the ferrite cores were put into the PCB stack as shown in Fig. 3- 7**Error! Reference source not found.** (b). Next, the PCB-embedded magnetic board was moved to the

hydraulic press machine for lamination following the processing guide outlined in [107]. During the dual stage pressure cycle, the prepreg materials were melted to connect the PCB core materials, and the air within the layers was extracted. After lamination, the ferrite cores were fixed within the PCB as shown in Fig. 3- 7 (c). With the cores embedded in the PCB, via-holes were drilled by the PCB router. Wires were then inserted through the vias to construct the windings, which are

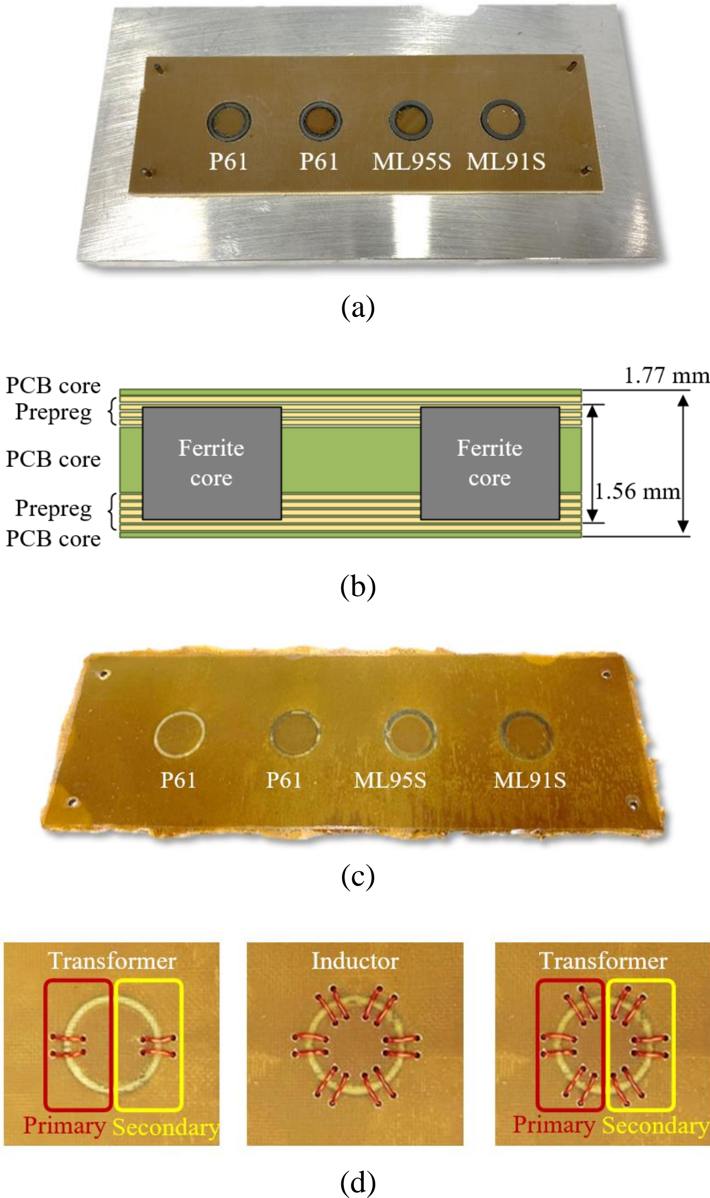


Fig. 3- 7. (a) Core assembly. (b) PCB stackup. (c) PCB-embedded magnetic board without via-holes. (d) Winding structures.

shown in Fig. 3- 7 (d).

3.3 PCB-embedded ferrite properties trend investigation

The impact of stress on ferrite cores is frequency dependent. Taking the 12-turn inductors made of P61 as examples, Fig. 3- 8 shows the inductance versus frequency curves under 0 PSI and 450 PSI. The dc inductance L_{DC} before lamination is 9.19 μH. At f_1, inductance starts to increase slightly and then it drops due to the combination of eddy currents in the ferrite core as well as skin and proximity effect in the windings. When the frequency reaches f_2, the inductance increases again due to the stray capacitance. After lamination, both f_1 and f_2 move to a higher frequency (> 1 MHz), which is out of the GDPS operating range; therefore, the inductance performance at frequency over 1 MHz is not discussed in this dissertation. Properties including self-inductance, leakage and magnetizing inductance, coupling strength, effective turns ratio, and input-output capacitance are discussed as follows.

The dc inductance versus pressure curves of the three materials are shown in Fig. 3- 9. 12-turn inductors shown in **Error! Reference source not found.** (d) were measured. It is found that

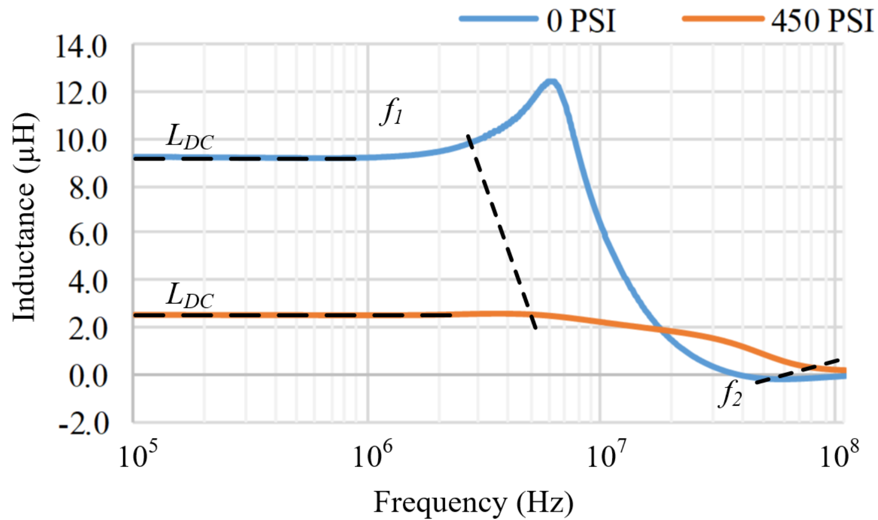


Fig. 3- 8. Inductance versus frequency under 0 PSI and 450 PSI with core 1.

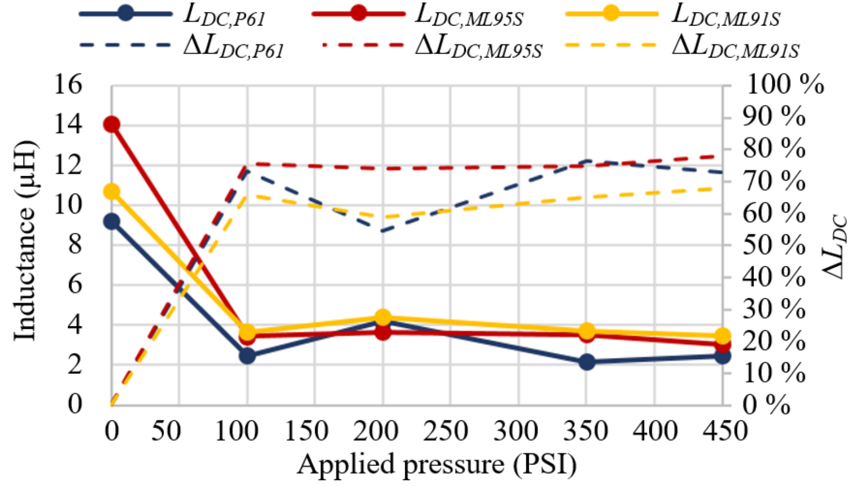


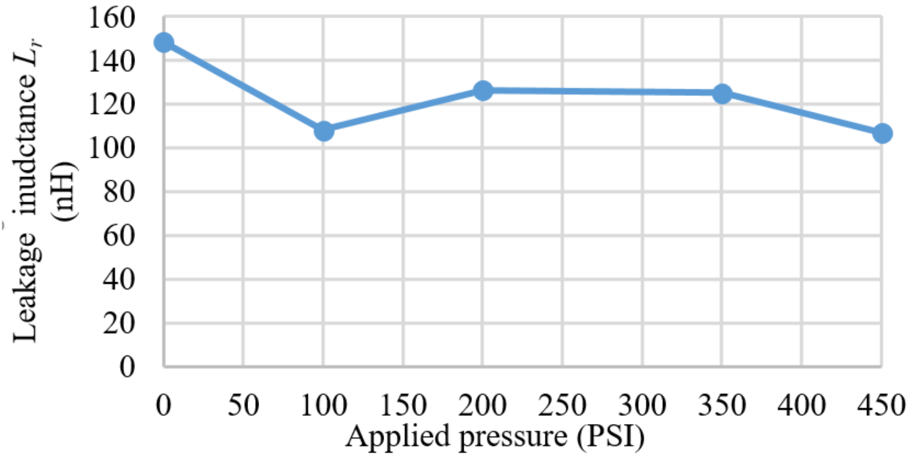
Fig. 3- 9. Inductance and percentage change under different applied pressure.

the inductances of all materials reduce significantly once the stress was applied. It is worthwhile to point out that materials have different stress resistivity. The percentage change of the dc inductance L_{DC} is defined as follows:

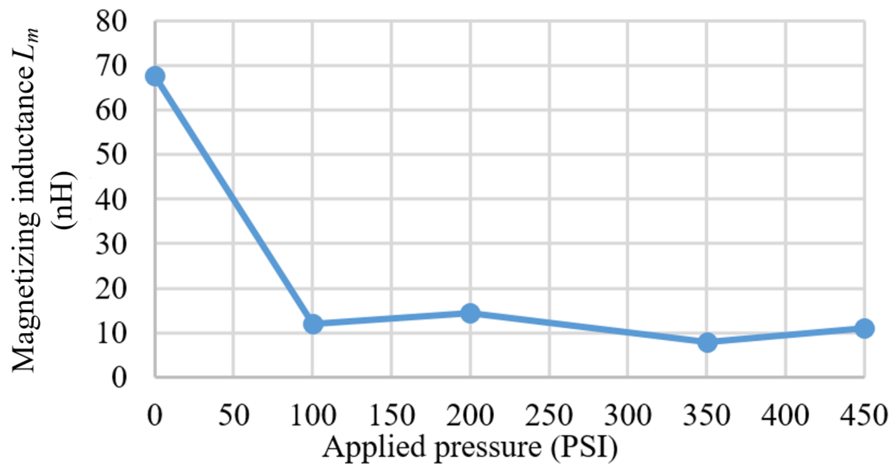
$$\Delta L_{DC} = \frac{L_{DC,NP} - L_{DC,AP}}{L_{DC,NP}} \% \tag{3. 1}$$

where $L_{DC,AP}$ and $L_{DC,NP}$ are the dc inductance with and without applied pressure. According to Fig. 3- 9, the L_{DC} of P61, ML95S, and ML91S drops by 55 % to 76 %, 74 % to 78 %, and 59 % to 68 % between 100 and 450 PSI respectively, indicating that stress has the least impact on ML91S. In this specific case, it is also found that the inductance reduction occurs once a light stress is applied to the ferrites, but the influence of the stress level is relatively weak. As illustrated in Fig. 3- 9, ΔL_{DC} reached 55 %, 74 %, and 59 % once a 100-PSI stress was applied, while it only increased 21 %, 4 %, and 9 % when the stress changed from 100 PSI to 450 PSI.

The stress impact on leakage inductance L_r, magnetizing inductance L_m, coupling coefficient k, and effective turns ratio n_e are analyzed by using the 2-turn transformers shown in **Error! Reference source not found.** (d). L_r, L_m and n_e are derived from the transformer matrix, which



(a)



(b)

Fig. 3- 10. (a) Leakage inductance and (b) magnetizing inductance versus applied stress measured by 2-turn transformers. Parasitic capacitance C_{io} versus applied stress.

can be given by the open-circuit and short-circuit impedance measurement. Assuming the fringing effect is negligible; the leakage inductance is determined by the winding geometry. According to Fig. 3- 10 (a), the leakage inductance is almost independent of the applied stress. The difference is caused mainly by the difference in the winding between samples. On the other hand, the embedding process reduces the ferrite permeability that significantly affects the magnetizing inductance. As seen in Fig. 3- 10 (b), L_m dropped from 68 nH to 12 nH once a 100 PSI stress was applied, and it fluctuated between 8 nH and 14 nH when the stress changed from 100 PSI to 450

PSI. This follows the conclusion given by Fig. 3- 9. The fluctuation could be caused by ferrite property differences between the samples as well as pressure and temperature variation during the dual-stage press. As the pressure and the temperature of the dual-stage press machine used to fabricate the PCB-embedded magnetic boards were manipulated, they floated within a certain range, which also leads to the fluctuation in Fig. 3- 10 (b).

This phenomenon hinders the wide-input-voltage design in achieving the required effective duty cycle, as D_{eff} increases with the increase of L_r/L_m according to (2. 4). Moreover, it might bring higher voltage stress on the devices given by the third part of (3. 2).

$$V_{ds,S1} = V_{in} + \frac{V_o + V_{sk}}{n_e} + \frac{2L_r f_s P_n}{V_{in} D_{eff}(1 - D_{eff})} \tag{3. 2}$$

The effective turns ratio n_e versus applied stress is shown in Fig. 3- 11. Generally, the effective turns ratio n_e is larger than the actual turns ratio due to the leakage flux. Since the coupling strength between the primary and secondary windings is weakened by the embedding process, the effective turns ratio n_e increases correspondingly. According to Fig. 3- 11, n_e increases by 70.4 %. This means that the junction capacitance C_j of the rectifier diodes absorbs more energy, which could affect ZVS operation. However, it reduces the second part in (3. 2), which could relieve the voltage

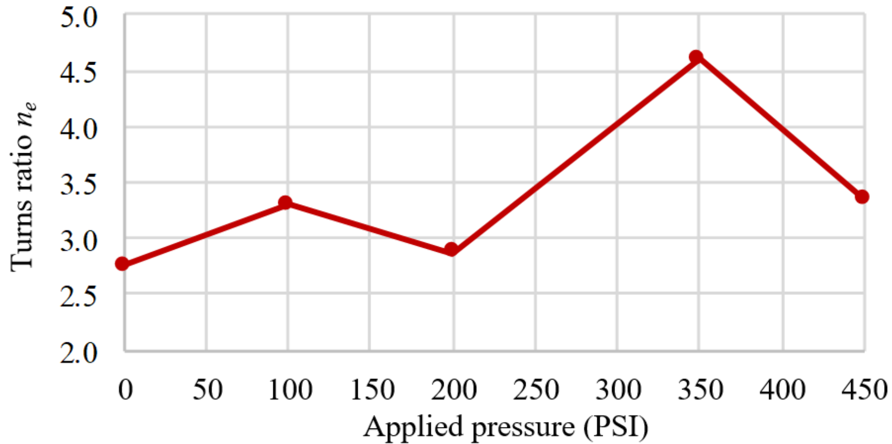


Fig. 3- 11. Turns ratio n_e versus applied stress.

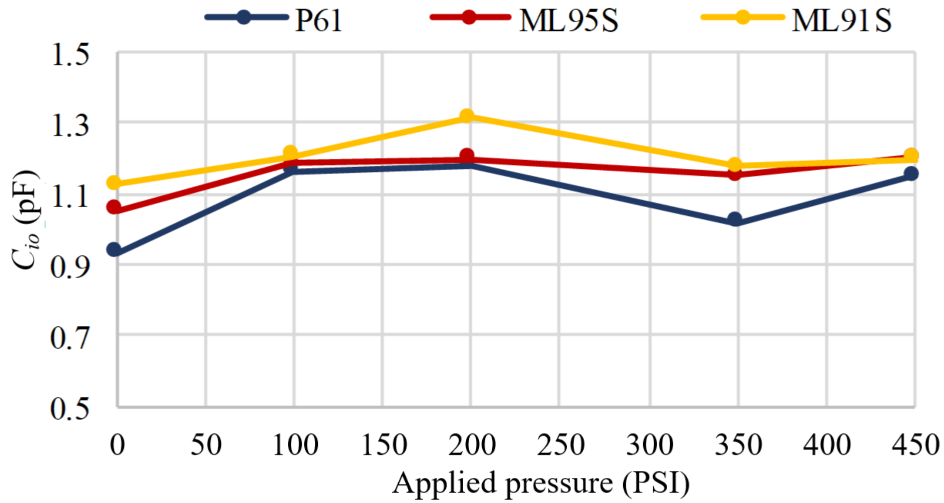


Fig. 3- 12. Parasitic capacitance C_{io} versus applied stress.

stress on the primary devices.

The C_{io} are also measured by the 6-turn transformer shown in **Error! Reference source not found.** (d). The results are given in Fig. 3- 12. Compared to the control group, the increase in C_{io} is less than 0.3 pF for all materials, which is small enough to be neglected.

In conclusion, the stress induced by the PCB-embedded process has a significant impact on the transformer design. It not only leads to permeability degradation that results in higher current stress and conduction loss, but also weakens the coupling strength that brings uncertainties to the wide-input-voltage design and ZVS realization. The C_{io} is mainly determined by the winding structure and is barely affected by the embedding process.

3.4 Solution discussion and improvements

As shown in Fig. 3- 5, the valid design region in the optimization process is significantly reduced by the embedding of the magnetic cores. It could easily lead to rendering the design targets unattainable if the stress effect is not properly accounted for during the design itself.

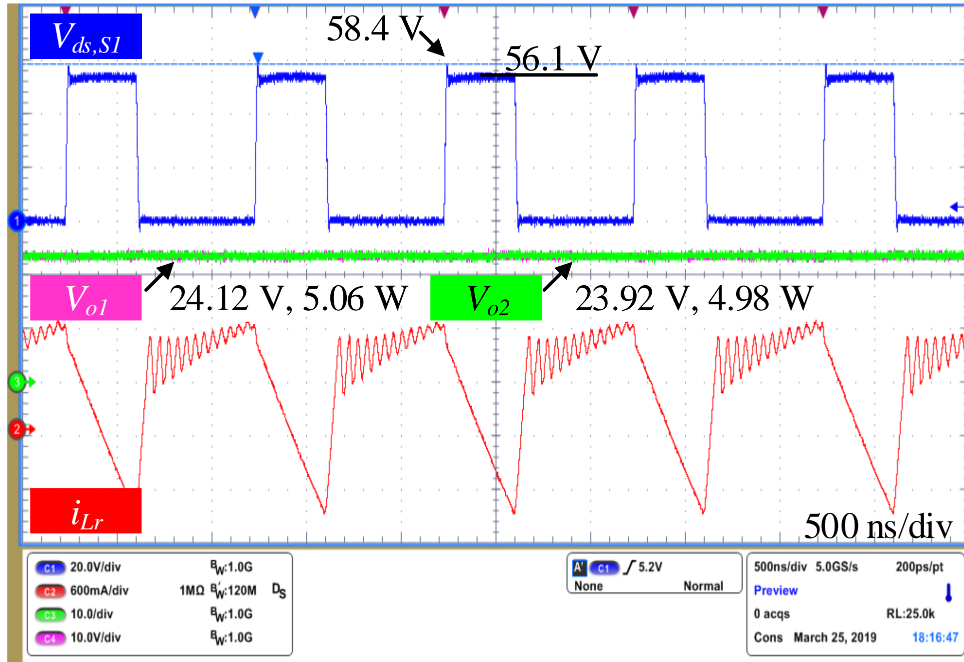


Fig. 3- 13. Experimental testing results of the hand-wound transformer based GDPS at nominal input $V_{in,nom}$=12 V and rated power P_o=10.0W. $V_{ds,S1}$=58.4 V, D=62%.

3.4.1 **Solution discussion**

The main waveform of the hand-wound transformer based GDPS at nominal voltage and rated power is shown in Fig. 3- 13. The required duty cycle and the voltage stress on primary devices at this operating point are 62 % and 58.4 V, respectively. Accordingly, it achieves the target input voltage operating range of 8.5–28 V.

Fig. 3- 14 shows the experimental results of the PCB-embedded transformer based GDPS at the same operating point. As seen, the required duty cycle and the voltage stress increase to 81 % and 73.2 V with the same transformer design. The achieved input-voltage range of this design is hence reduced to 9.7–28 V. It fails to meet the wide-input-voltage requirement due to the weaker coupling strength of the ACF transformer. The peak efficiency also drops by 6.3 % as Fig. 3- 1 shows, illustrating why remedial steps are needed in the design of the GDPS.

There are two main ways to address this degradation problem. The first way is to develop

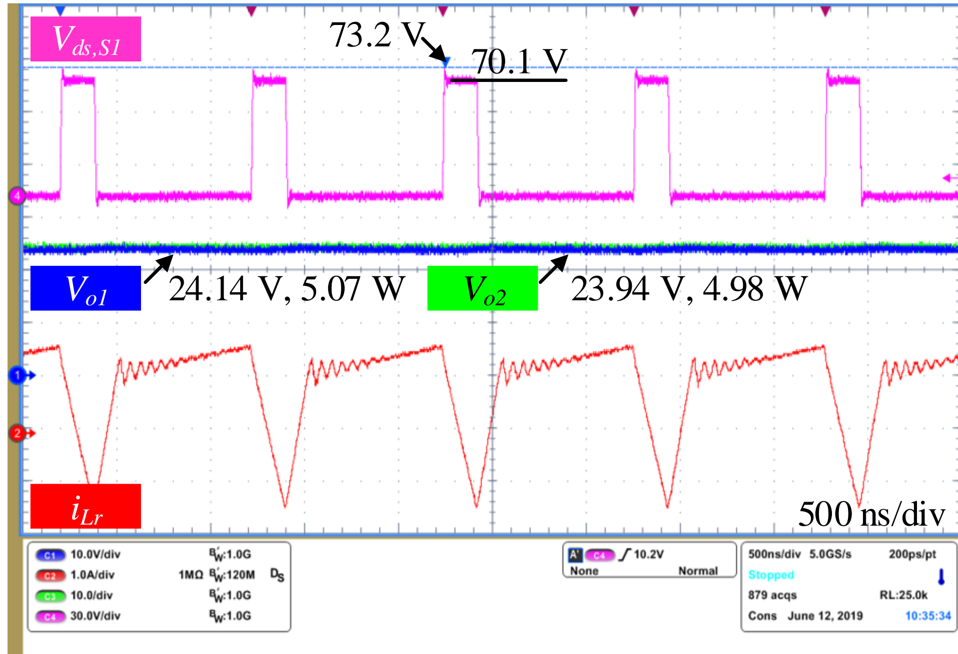


Fig. 3- 14. Experimental testing results of the PCB-embedded transformer based GDPS at nominal input $V_{in,nom}$=12 V and rated power P_o=10.1W. $V_{ds,S1}$=73.2 V, D=81%.

fabrication techniques avoiding the stress on the ferrite, similar to the 1 W single-output GDPS with the PCB-embedded transformer manufactured by Murata [111]. This GDPS utilizes a hollow PCB to hold the magnetic core eliminating the stress, but it is not compatible with conventional PCB manufacturing. This structure also increases the winding-to-core distance, resulting in a less effective window area, higher winding losses, and a lower power density. The loose structure of the winding also increases the leakage inductance because more magnetic flux goes into the air instead of circulating in the core, which narrows down the input voltage range. The power supply presented in [112] is compatible with conventional PCB manufacturing and successfully addresses the permeability degradation issue at low frequency. In this design, a cavity that is slightly larger than the magnetic core is built to withstand stress, but it has the same disadvantages as [111]. Furthermore, the inductance drops at high frequency; the reason of which is still under investigation.

3.4.2 **Proposed experimentally derived correction factor**

The second solution is to keep the fabrication process unchanged and add correction factors to the permeability and the coupling coefficient, by which other transformer properties can be predicted more accurately. This solution is feasible, straightforward, and low-cost, but the drawback is that it sacrifices either power density or efficiency. In addition, since the inductance reduction depends on the specific ferrite material used, the core geometry, and the fabrication process itself, it is very difficult to predict the final transformer properties by either analytical or numerical methods. Therefore, the approach followed in this chapter, is to test PCB-embedded transformer samples to measure the change induced following the same fabrication process, deriving experimentally the proper correction factors for the optimization process.

To this end, nine transformer samples were built and tested to derive the correction factors. The worst-case properties and their correction factors are summarized in Table 3. 5, where μ_r is the relative permeability, and k_{12}, k_{13}, k_{23} are the coupling coefficient between the primary and secondary 1 windings, between the primary and secondary 2 windings, and between the secondary 1 and secondary 2 windings, respectively. The difference between k_{12} and k_{13} is negligible; hence, they are assumed identical in what follows. The relative permeability μ_r of the PCB-embedded transformer samples is calculated to be 174.6 per (3. 3), giving a correction factor of 0.19. The coupling coefficients are also given by comparing the transformer matrices, which are also listed in Table 3. 3. 3D FEA simulations were done to verify the proposed method, which are illustrated in Table 3. 4. As seen, the simulation results with correction factors are closer to the measurement, compared to the one without considering the permeability degradation.

$$L = \frac{N^2 \mu_0 \mu_r A_c}{l_g \mu_r + l_c} \tag{3. 3}$$

Table 3. 4. WORST-CASE PROPERTIES OF THE PCB-EMBEDDED TRANSFORMER

Property	Hand-wound transformer	PCB-embedded transformer	Correction factor
μr	900	174.6	0.19
k12 (k13)	0.960	0.928	0.97
k23	0.993	0.978	0.98

| k23 | 0.993 | 0.978 | 0.98 |

3.4.3 Improved PCB-embedded transformer based GDPS and qualification

The above implies that for designs seeking to achieve high power density, the achievable inductance range will be restricted, limiting the number of design cases that are capable of meeting the desired wide-input-voltage performance space requirement. To offset this effect, a larger core or larger number of turns is required in the GDPS in question, specifically N_p, N_{S1}, and N_{S2} need

Table 3. 3. Model Improvement With Proposed Correction Factors

Properties	Measurement	FEA simulation w correction factors	Compared to Measurement	FEA simulation w/o correction factors	Compared to Measurement
Lp (μH)	10.3	10.9	+6 %	19.8	+92 %
k12=k13	0.928	0.929	+0.1 %	0.953	+3 %
Lr (μH)	1.08	1.17	+8 %	1.09	+1 %
Lm (μH)	9.2	9.73	+5 %	18.7	+103 %
ne	1.06	1.03	−3 %	1.04	−2 %
Lr/Lm	0.117	0.120	−3 %	0.058	−50 %

to increase by at least 1.44 times. However, there is not enough window area to accommodate for these extra turns. Hence, a core with 2.08 times larger A_c is the only way to increase the inductance in this design.

Alternatively, in an effort not to sacrifice power density, the input-voltage range of the transformer in question extends from 9.7 ~ 2.8 V to 7 ~ 28 V by eliminating a turn in the primary

winding. This is summarized in Table 3. 5, which compares the hand-wound transformer, the previously designed PCB-embedded transformer, and the improved PCB-embedded (iPCB-embedded), showing how the latter design successfully meets the wide-input-voltage range requirement. Fig. 3- 15 demonstrates the operation of the GDPS at minimum input voltage of 7 V,

Table 3. 5. Transformer Comparison

Property	Hand-wound transformer	PCB-embedded transformer	iPCB-embedded transformer
N_P	12	12	11
N_S	12	12	12
V_{in} (V)	8.3~28	9.7~28	7~28

showing it can successfully generate the two output voltages of 24 V. Compared to the original design, the input range is increased by 2.7 V, tackling the design problem effectively.

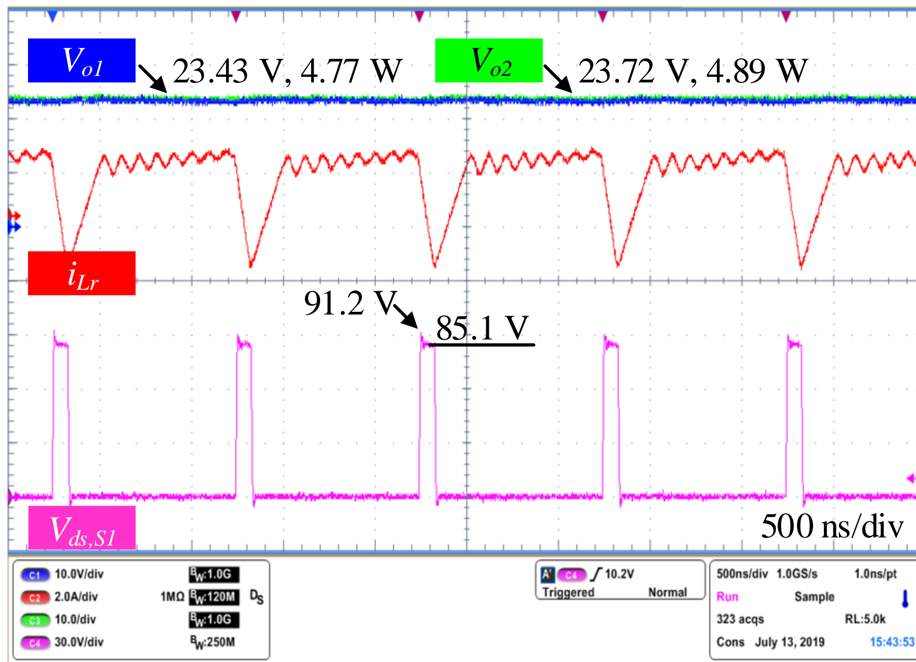


Fig. 3- 15. Experimental testing results of the iPCB-embedded transformer based GDPS with applied correction factors at achievable minimum input $V_{in,min}$=7 V and rated power P_o=9.7 W. $V_{ds,S1}$=91.2 V, D=92%.

3.5 Design tradeoffs of iPCB-embedded transformer

The PCB-embedding technique has great potential in power electronic converters. It not only significantly increases the power density and the insulation strength, but also reduces the manual fabrication steps; however, it also brings uncertainties into the design process. In general, designers would leave a margin to handle manufacturing variability, which is normally around ±10 % (or less). Yet, the variability of the PCB-embedded ferrite applications is extremely large (might be over 100 %). Certain applications, such as the GDPS proposed in this dissertation (wide-input-voltage, high power density, high operating ambient temperature ACF converter), have strict constraints that make it hard to handle large uncertainties. To avoid design failures, it is important to accurately predict the transformer parameters. The challenge of utilizing the PCB-embedding technique in such applications is the difficulty in attaining accurate embedded ferrite properties. In this paper, the model was improved by adding the experimentally derived correction factors, and the final prototype successfully met the requirements. New discoveries may follow, such as a more accurate model of the embedded ferrite, and an improved fabrication process that mitigates the stress effect on the ferrite.

3.6 Summary and conclusions

The measurement of the PCB-embedded ferrite properties were conducted in this chapter. The stress induced by the embedding process significantly influenced the inherent material characteristics of the ferrite core used to implement the transformer of the ACF converter in question. Specifically, it degraded the ferrite permeability and the coupling strength between windings. Quantifying these changes through experimentally derived correction factors improved the modeling accuracy and effectiveness of the multi-objective optimization process developed,

and effectively identify the appropriate set of designs that meet the performance space requirements. As a result, the proposed 10 W, dual-output integrated GDPS for SiC power module automotive applications met its design targets.

Chapter 4 Enhanced Gate Driver Design for SiC Based Airborne Applications

4.1 Introduction

Over past years, the aerospace industry has sought to develop Generator Rectifier Units (GRUs) featuring high efficiency, high power quality, and high power density. This is all in an effort to improve the performance as well as reduce the size and weight of critical system components. Wide-bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs, have emerged increasingly as a viable alternative to silicon (Si) IGBTs in airborne applications. However, their great characteristics lead to some challenging collateral effects. The gate driver, as the adjacent electronic unit to SiC-MOSFET modules and the essential interface between the control system and power stage, faces significant challenges.

First, it should present sufficient insulation strength when subjected to 540 V under a low-pressure condition at 50,000 ft. The pressure of the working environment for aircraft varies from 10,000 Pa to 400,000 Pa [114]. As the altitude increases, the air density decreases, which degrades the insulation strength. This phenomenon is also explained by the Paschen curves shown in Fig. 4- 1. As seen, the breakdown voltage V_{bk} decreases when altitude becomes higher. To avoid discharges, a correction factor is commonly used by converters operating at high altitude, so that a safe clearance distance can be maintained. However, most of the standards provide an altitude correction factor at altitude only up to 4,000 m (13,123 ft), which is not sufficient in the proposed GRUs. Only one standard, IEC 60664-1 [115], provides an altitude correction factor of 6.67 at 50,000 ft, but it might lead to an overdesign that reduces the power density.

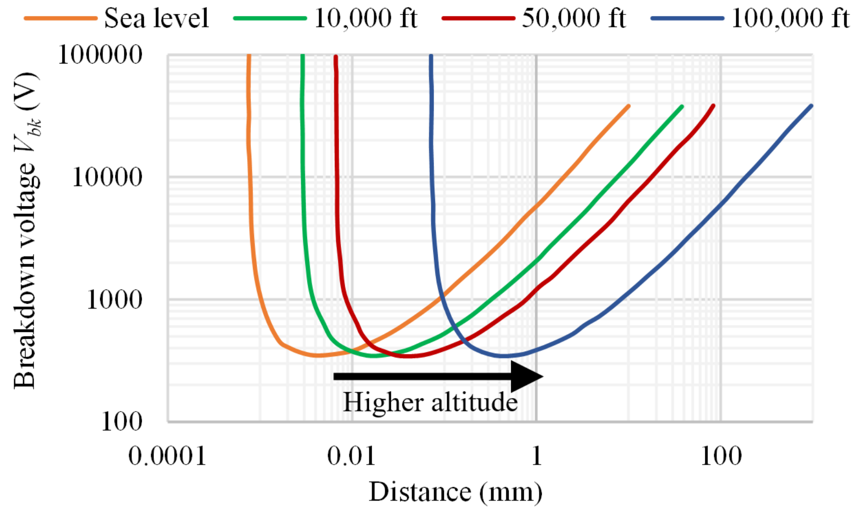


Fig. 4- 1. Paschen curve at different altitude.

Second, faster detection and protection are desired when wide-bandgap (WBG) devices are adopted. In general, the internal parasitic inductance and the ON-state resistance of WBG semiconductor devices are small thanks to their more compact package. As a result, the *di*/*dt* at turn-on and turn-off transients are fast. When short-circuit (SC) and over-current (OC) faults occur, the fast *di*/*dt* causes the current to rise rapidly to a high level damaging the system in several μs, leading to a much shorter fault withstanding time compared to the conventional Si IGBT [116]. Therefore, the SC and OC protection design in the gate driver for SiC-based applications is very challenging.

Printed circuit boards (PCBs), with advantages of low profile, low cost, and perfect fit for automated manufacturing and mass production, have been widely used as carriers of electronic components. As solid insulators, they have a much higher dielectric strength (40 kV/mm) compared to dry air (3.3 kV/mm). With this feature, electric-field (E-field) control methodology is frequently applied to the gate driver PCB layout design to re-arrange the E-field distribution [117], [118]; therefore, the peak electric field E_{pk} can be shifted from the air to the PCB dielectric, effectively reducing the field strength along the surface of the PCB in air.

There are several methods to sense the switch current. The desaturation (DeSAT) method is commonly used for IGBT-based applications. The implementation of the DeSAT method is simple and low-cost, but its inherent "blanking-time" delay hinders the fast fault detection. Another possibility is to adopt power semiconductor devices that feature a current sense function, but that is not compatible with all power semiconductor devices, effectively narrowing down the candidate list. The switch current information can also be attained by measuring the gate-source voltage or gate charge, but this method is not applicable to the fault-under-load SC [119]. Further, switch current measurement can be realized using a shunt resistor, a current transformer, a Rogowski coil, or by voltage measurement over the power module parasitic inductance [120]. Among these, the Rogowski coil was an excellent current detector for SC and OC faults thanks to its high bandwidth, wide measurement range, and good accuracy [121]; therefore, it is implemented on the proposed gate driver.

In this chapter, a comprehensive design of a gate driver for SiC-based GRUs for variable frequency airborne applications is presented. Details on the gate driver operating principles and implementation, including the gate driver architecture, Rogowski switch-current sensor (RSCS) design, and gate driver functionalities, are first illustrated. Insulation and layout design, including the insulation co-ordination determination, E-field management strategay, and layout considerations, are then introduced. A prototype was built and experiments were conducted, successfully verifying that the design achieves all of the targets.

4.2 Operation principles and implementation

4.2.1 Gate driver architecture and component selection

The high-level gate driver architecture for a 1.2 kV, 475 A SiC MOSFET half-bridge module

is shown in Fig. 4- 2. The proposed gate driver in this chapter features an active miller clamp circuit, SC protection, OC protection, and phase-current reconstruction. +270 V and −270 V DC voltage is applied to the positive DC terminal (+DC) and negative DC terminal (−DC), respectively. The gate driver primary side circuit, where most of signal processing components and logic units are located, shares the same ground with the controller. The commercial gate-drive power supplies (GDPSs), driver ICs, and the digital isolators (D-ISOs), provide insulation and noise immunity between the gate driver primary side circuit and the driving circuit. The 5.7 kVrms, single-channel, isolated gate-driver IC UCC21732 from Texas Instruments [122], is selected as the gate driver ICs. The single-channel, 5 kV, single-channel digital isolator, ADuM210N from Anolog Devices [123], is selected as the D-ISOs. The 5.2kV_{DC}, isolated 2W gate-drive dc-dc converter, MGJ2D242005SC from Murata Manufacturing [124], is used as the GDPS. The

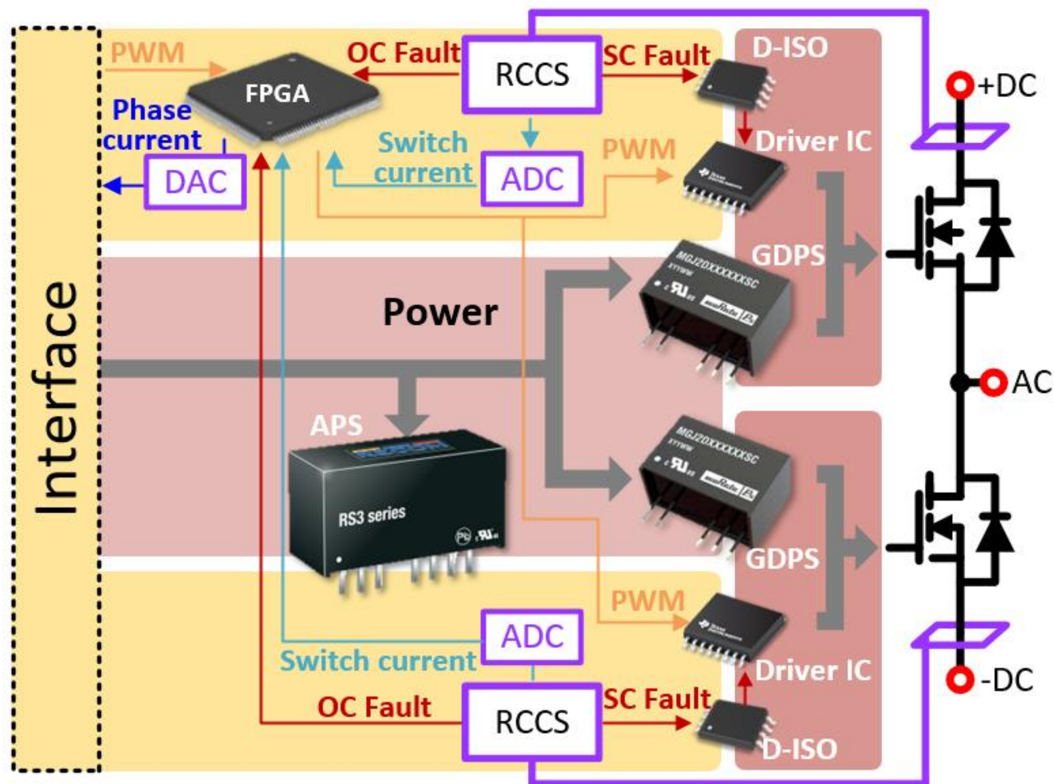


Fig. 4- 2. Gate driver architecture.

components and their properties are summarized in

The RSCSs, which sense both top side and bottom side switch current, are also placed at the gate driver primary side circuit. Graphically illustrated in Fig. 4- 3, the switch current measurement contains a high bandwidth loop used for SC protection and a low bandwidth loop used for OC protection and phase current reconstruction. In the high bandwidth loop, the output of the RSCS is directly connected to the SC comparator and the high frequency ringing information of the switch current remains. When the SC fault existed, the comparator outputs a fault signal, which will be sent to the driver IC secondary side directly through D-ISO. The corresponding gate driver IC will turn off the SiC MOSFET and report the fault to the FPGA and the controller, enabling a fast fault detection. In the low bandwidth loop, there is an RC filter with low cut-off frequency, which eliminates the high frequency ringing. When there is an OC fault, the comparator outputs a fault signal, and it will be sent to the FPGA. Then the FPGA shuts down both driver ICs and reports

Table 4. 1. Component List and Their Properties

Component	Manufacturer	Part Number	Insulation voltage	CMTI
Gate driver	TI	UCC21732	5.7 kVrms	150 V/ns
D-ISO	ADI	ADuM210N	5 kV	100 V/ns
GDPS	Murata	MGJ2D242005SC	5.2 kV_{dc}	> 200 V/ns
APS	Recom	RS3-2405D/H3	3 kV	N/A

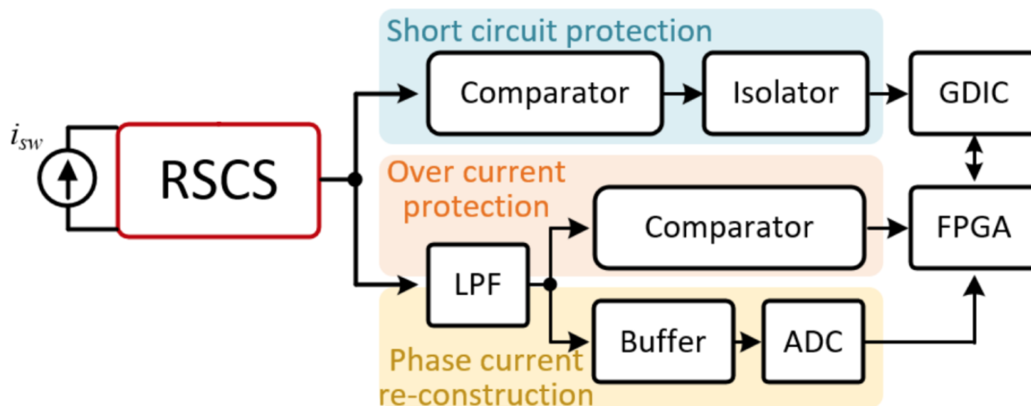


Fig. 4- 3. Switch current measurement with RSCS.

OC fault to the controller. ADCs are used to convert the analog RSCS output to a digital signal communicating with the FPGA that performs the phase current reconstruction. DACs are used to convert digital signals at FPGA output to analogy signals used by the controller.

4.2.2 **Rogowski Switch-Current Sensor (RSCS) design**

Featuring temperature and I/V independency, low latency, and high bandwidth, RSCS has been demonstrated as a suitable option for SC protection for WBG semiconductor devices. Therefore, it is used in the SC protection and OC protection of the gate driver presented in the proposed gate driver.

The equivalent circuit of the RSCS is shown in Fig. 4- 4 [125]. It consists of a Rogowski coil constructed of PCB traces and vias, an integrator with an active reset switch, a low-pass filter, and a buffer.

The reset switch S_{rst} is added to the integrator circuit to reset the integrator output to zero when the SiC MOSFET is turned off. In practice, an ideal integrator with infinite gain at zero frequency does not exist, which causes offset voltages at the RSCS output [126]. This voltage cannot be used for either protection or phase current reconstruction because the real amplitude of the drain current cannot be correctly sensed. With S_{rst} across the integrator capacitor C_i, the switch current sensor can eventually sense the pulsating current with the correct amplitude.

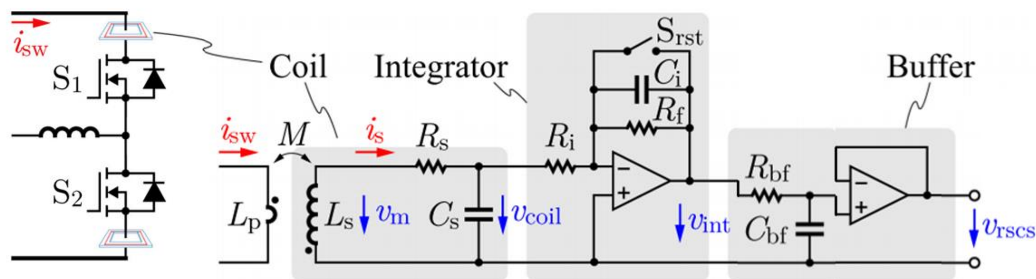


Fig. 4- 4. Equivalent circuit of the RSCS.

After the integrator, there is a low-pass filter (LPF), which is used to eliminate unnecessary high-frequency ringing information. Its cutoff frequency f_{cutoff} is designed to be 19 MHz in the proposed gate driver. The buffer stage follows the LPF and it serves as a voltage follower for impedance matching.

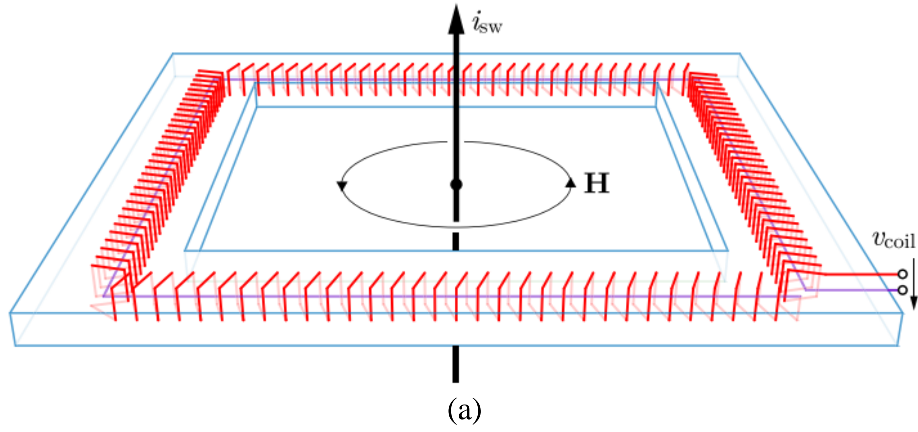
The lumped model of the Rogowski coil includes a mutual inductance M, a primary-side self-inductance L_p, a secondary-side self-inductance L_s, a winding resistance R_s, and a stray capacitance C_s. The Rogowski coil serves as a differentiator that generates the di/dt value of the switch current i_{sw} with a scale of M. Then this di/dt information is integrated back to the current information. Assuming that R_f is large enough and the value of L_s, R_s and C_s are much smaller than R_i, the transfer function of the RSCS can be simplified as follows:

$$\frac{V_{rscs}(s)}{I_{sw}(s)} = \frac{M}{R_i C_i} \tag{4. 1}$$

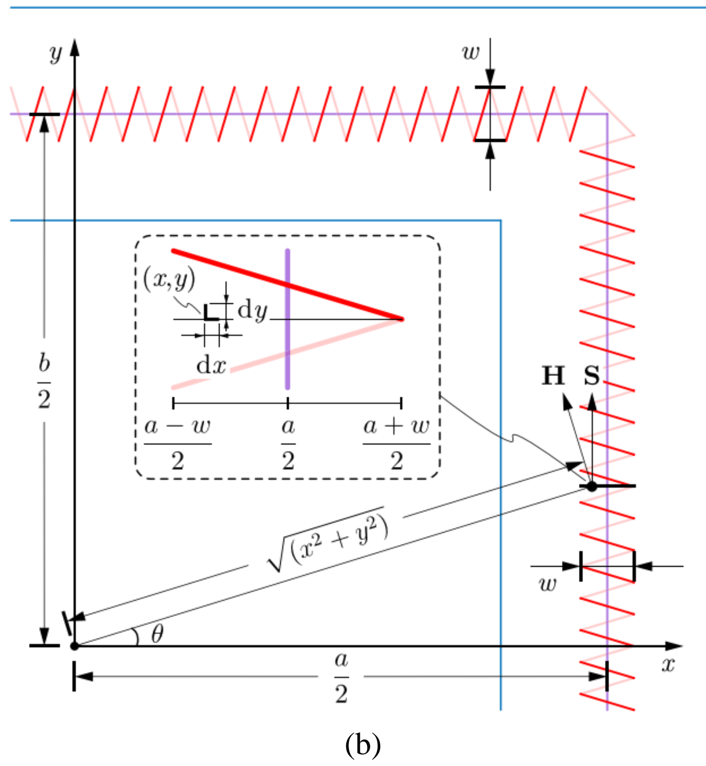
The mutual inductance M and the self-inductance L_s can be given using the analytical models derived in [125]. The calculation is based on the geometric dimensions of the rectangular coil, which is shown in Fig. 4- 5. The parameters and the dimensions are listed in Table 4. 2, where a, b, h are the length, width, and height of the Rogowski coil, and w is the width of the cross-section area of the Rogowski coil. The length a and the width b are limited by the module dimensions, while the height h is determined by the PCB thickness. The total turns N is designed as large as possible to maximize the RSCS gain.

Table 4. 2. RSCS parameters and Dimensions

Parameter	Value	Parameter	Value
a	18 mm	Total turns N	112
b	17.95 mm	Total length	71.9 mm
h	0.87 mm	M	1.7 nH
w	1 mm	L_s	220 nH



(a)



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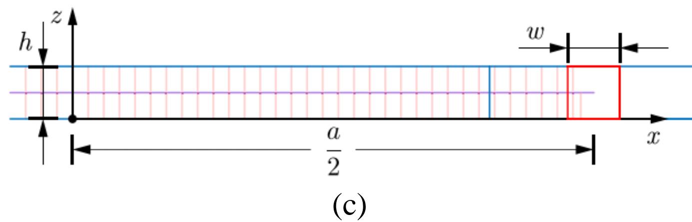


(c)

Fig. 4- 5. PCB-embedded Togowski coil: Red: winding traces. Purple: compensation traces. (a) Perspective, (b) top, and (c) front view [125].

4.3 Insulation coordination definition and layout design

As previously discussed, the insulation requirement between top side and bottom side driving circuits is 540 V, and the insulation requirement between gate driver primary side circuit and top- or bottom-side driving circuits is 270 V. Since the only altitude correction factor provided by the IEC standard is 6.67 that could be oversized reducing power density. An insulation coordination is necessary to satisfy the insulation target and maintain a small size at the same time.

4.3.1 **Insulation coordination definition**

To define the insulation coordination, breakdown voltage V_{bk} is converted to breakdown electric field E_{bk}, which can be given by:

$$E_{bk} = \frac{V_{bk}}{d} \tag{4. 2}$$

where d is the distance between the two conductors. The E_{bk} versus d curve at 50,000 ft is shown in Fig. 4- 6. The range of d is determined by the PCB manufacturing capability and distance between the top and bottom driving circuit for the SiC-based half-bridge module. It can be found that E_{bk} decreases with the growth of d, and its minimum value at targeted range is 600 V/mm. A

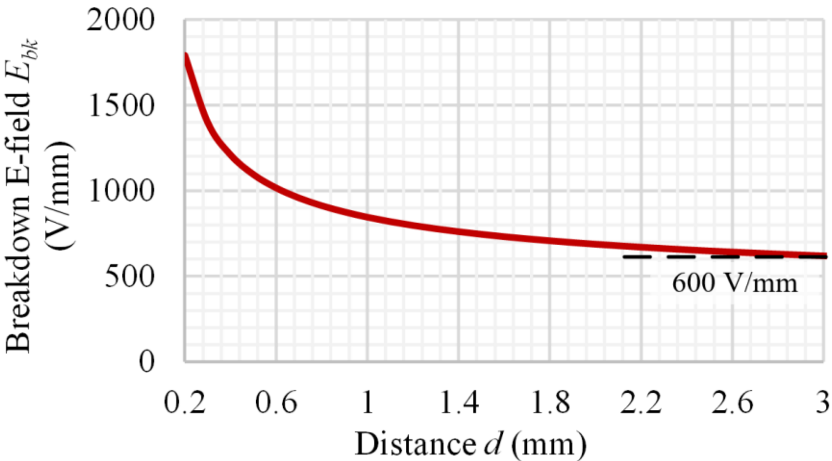


Fig. 4- 6. Breakdown electric field Ebk versus distance d at 50, 000 ft.

50 % margin is applied to the insulation design to ensure a safe operation; namely, the maximum E-field strength along the surface of the PCB in the air E_{air} is 300 V/mm.

4.3.2 **Layout design with E-field control methodology**

E-field control methodology has been widely used to control the field distribution in and around the PCB [119], [120]. Electric field distribution is significantly affected by conductor geometry and clearance. It is well known that sharp corners in the conductor geometry can lead to a high E-field concentration. Therefore, all copper features in the proposed gate driver are designed to have rounded corners with a finite fillet radius to lower the field strength over a specific area [127]. Additionally, the E-field distribution of the PCB is influenced by the layout of the external conductors. For this reason, the clearance distance between the two conductors that have a high voltage difference should be sufficient to reduce the E-field strength. Additionally, all copper conductors are embedded in the internal layers, and the external layers are only for surface terminations to the circuit components. This is because the solder mask coating on an external layer may contain bubbles and other contaminates leading to surface tracking between the two conductors. Also, as a thin coating layer, it can be easily scratched away exposing the conductor and its thickness is not sufficient to reduce the E-field at the critical PCB-Air interface. In order to further reduce the electric field in the high E-field area, internal power plates are utilized as field control plates to shift the peak electric field from the air to the PCB, which has a higher breakdown field strength.

The PCB stackup of the proposed gate driver is shown in Fig. 4- 7. To enhance the insulation strength, traces and vias should be placed in the internal layers and embedded by the fr4 materials. Since the RSCSs are very close to the high-voltage points due to the compact package of the SiC modules, the Rogowski coils are fully embedded in the PCB. Buried vias are used to enhance the

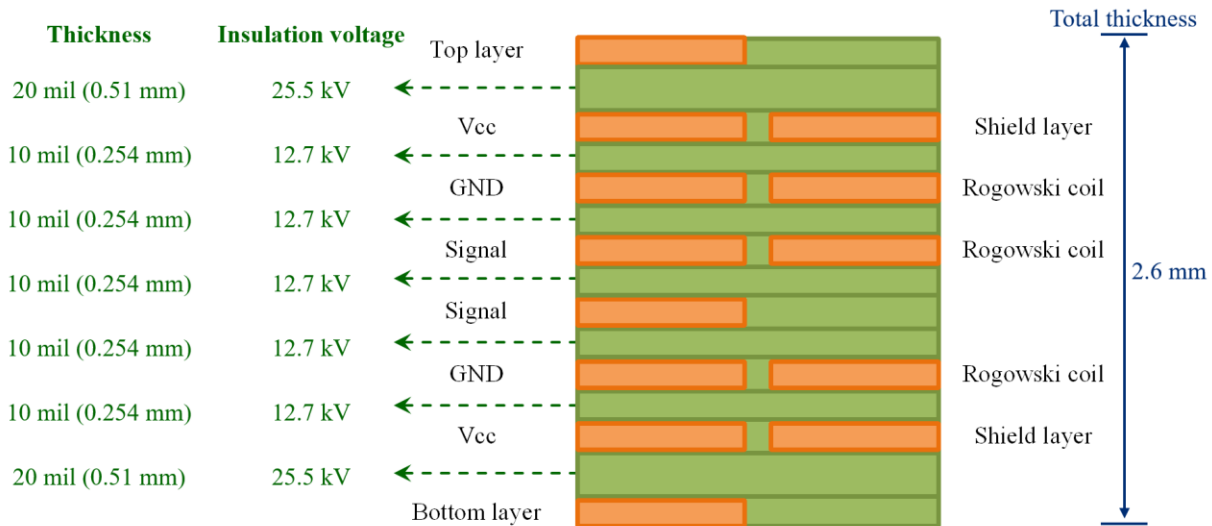


Fig. 4- 7. PCB stackup design for increasing insulation strength.

insulation strength. The fr4 thickness between layer 1and layer 2, as well as layer 7 and layer 8, are designed to be 20 mil (0.51 mm) to provide an insulation voltage of 25.5 kV. Since the voltage between the sensed busbar and the processing circuit is jumping with the SiC devices, shield layers are added to bypass the common-mode (CM) noise of the top side RSCS [128].

The top view of the terminal area in the gate driver is shown in Fig. 4- 8. Three spacers with are used between the busbar and SiC modules. As labeled in Fig. 4- 8, d_{bs} and d_{bc} is the distance between the board edge and spacer, and the distance between the board edge and copper. Since the terminal area is one of the high E-field areas, 2D FEA simulations were done to select d_{bs} and d_{bc}.

The simulation results are illustrated in Fig. 4- 9. It is shown that increasing d_{bs} and d_{bc} helps to reduce the electric field. To control the E_{air} below 300 V/mm, $d_{bs}+ d_{bc} > 2.6$ mm should be satisfied. To minimize the electric field around the Rogowski coil, d_{bs} and d_{bc} are designed to be 2 mm and 1.5 mm, respectively.

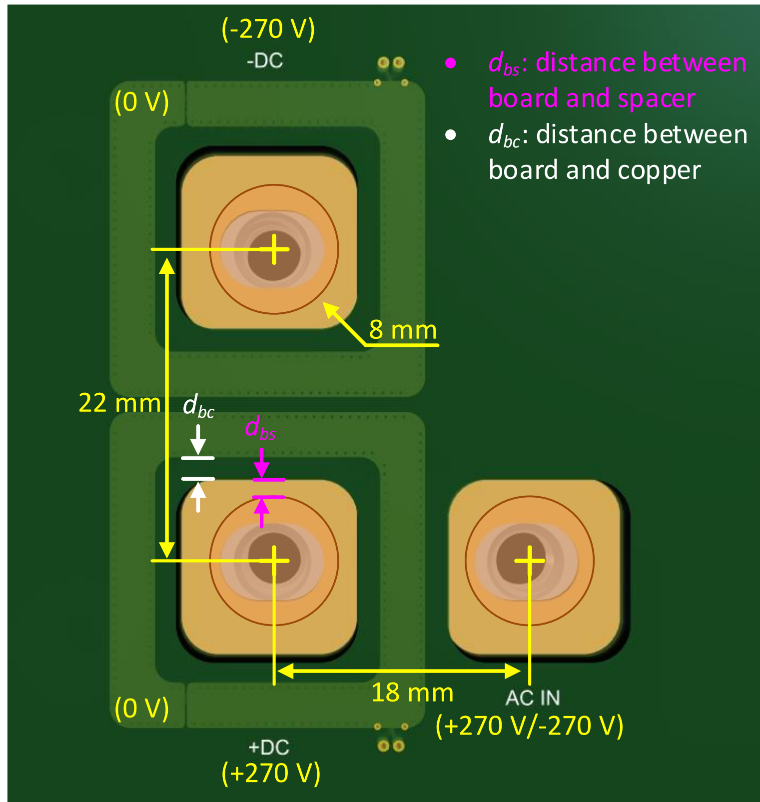


Fig. 4- 8. Top view of the terminal area in gate driver.

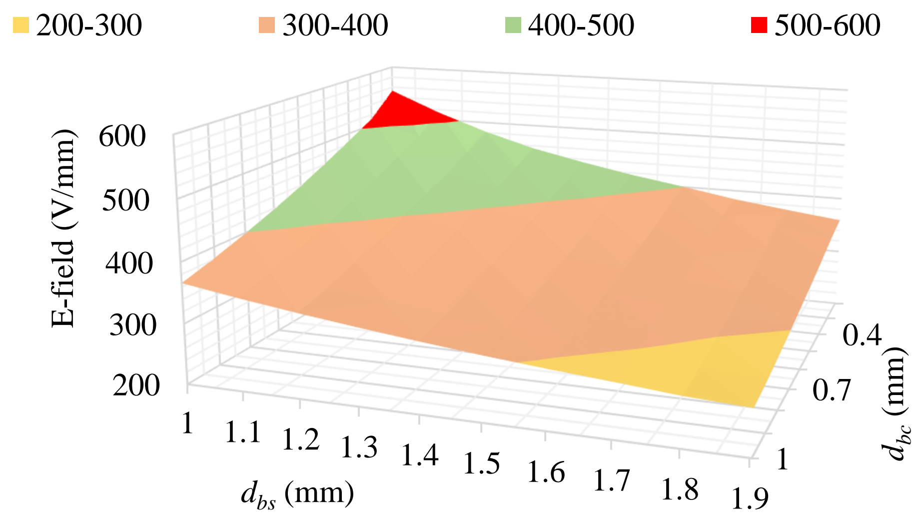


Fig. 4- 9. 2D FEA simulation result.

4.3.3 E-field simulation model and results

The E-field control methodology described above is implemented in the gate driver layout design. The top view of the 3D model of the proposed gate driver is shown in Fig. 4- 10. The interested areas, which are the areas around the edge of the +270 V and −270 V, are also highlighted in Fig. 4- 10. To verify the insulation design, 3D FEA simulations were conducted with ANSYS Maxwell. The 3D model used for E-field simulation is shown in Fig. 4- 11. In this model, only components at the interested areas were kept, which significantly sped up the 3D FEA simulation.

The worst-case simulation result that shows the E-field distribution between the top-side and bottom-side driving circuits, is depicted in Fig. 4- 12. By properly designing the field control

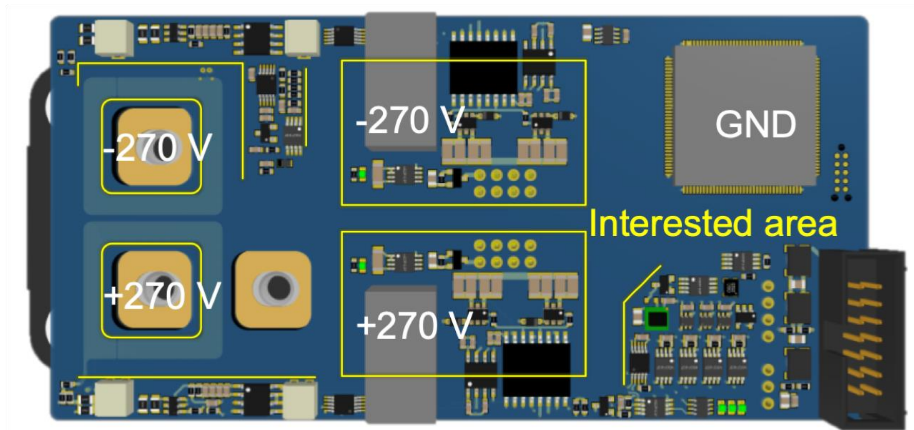


Fig. 4- 10. 3D top view of the proposed gate driver.

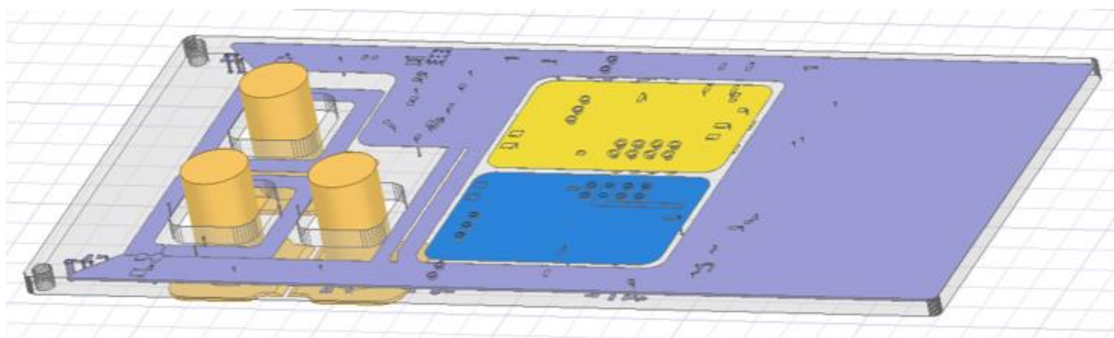


Fig. 4- 11. Simplifed model for 3D FEA E-field simulation.

plates, the peak E-field in air E_{air} was successfully designed below 300 V/mm. The highest E-field is shifted from the air to the PCB, showing sufficient insulation strength.

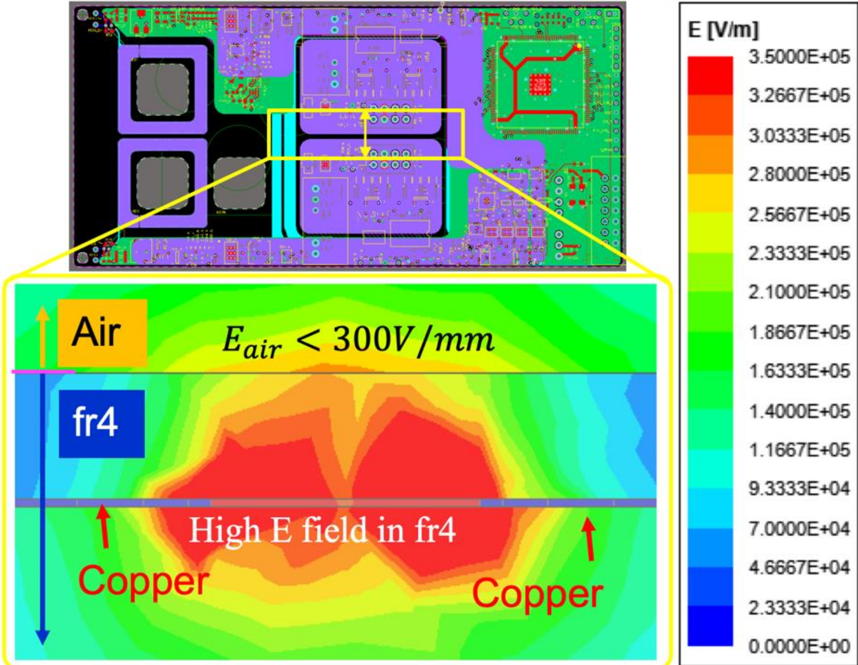


Fig. 4- 12. 3D FEA E-field simulation result: worst case.

4.4 Hardware assembly and qualification

4.4.1 Gate driver assembly

The test prototype is shown in Fig. 4- 13. The length, width and height of the gate driver

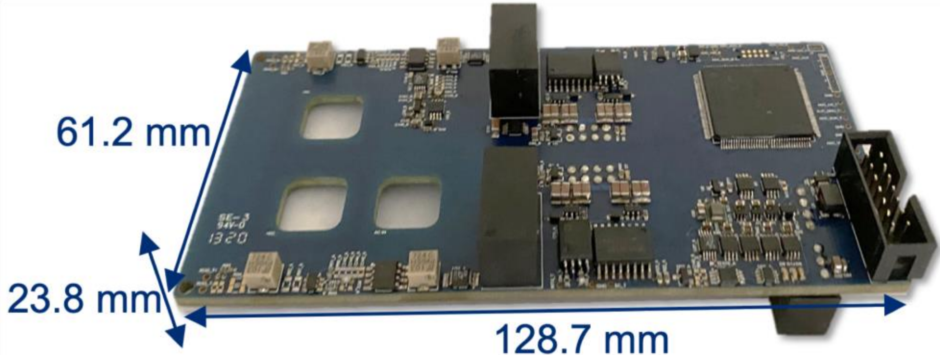


Fig. 4- 13. Gate driver prototype.

presented in this paper is 128.7 mm, 61.2 mm, and 23.8 mm, respectively.

To validate the SiC MOSFET switching behavior and the gate driver performance, double-pulse tests (DPT) were conducted for both the top and bottom switch of the SiC half-bridge module. The DPT test setup is shown in Fig. 4- 14, where a low-current-rating busbar is used.

The experimental results are shown in Fig. 4- 15. The voltage overshoot and undershoot of the top device at 540 V, 235 A are 306 V and -58 V; and the voltage overshoot and undershoot of the bottom device at the same operating condition are 86.4 V and -88 V. The differences are caused by the voltage probes used to measure the drain-source voltage V_{ds} and the property difference between the top and bottom SiC MOSFETs. The V_{ds} of the bottom device was measured by a high bandwidth (1 GHz) passive probe, while the V_{ds} of the top device was measured by a low bandwidth (350 MHz) differential probe. As seen, the voltages and currents in turn-on and turn-off transients were within the device's capability thanks to the small parasitic inductance in the power loop.

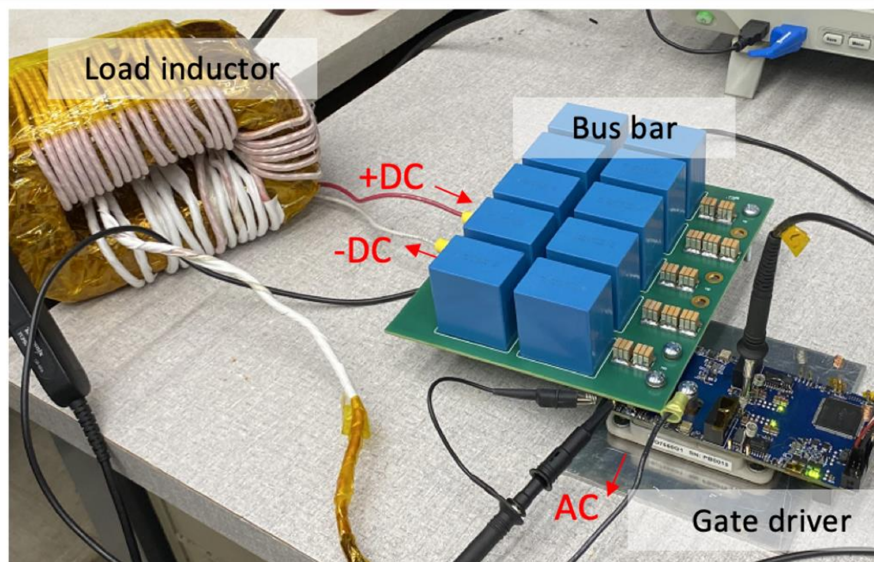
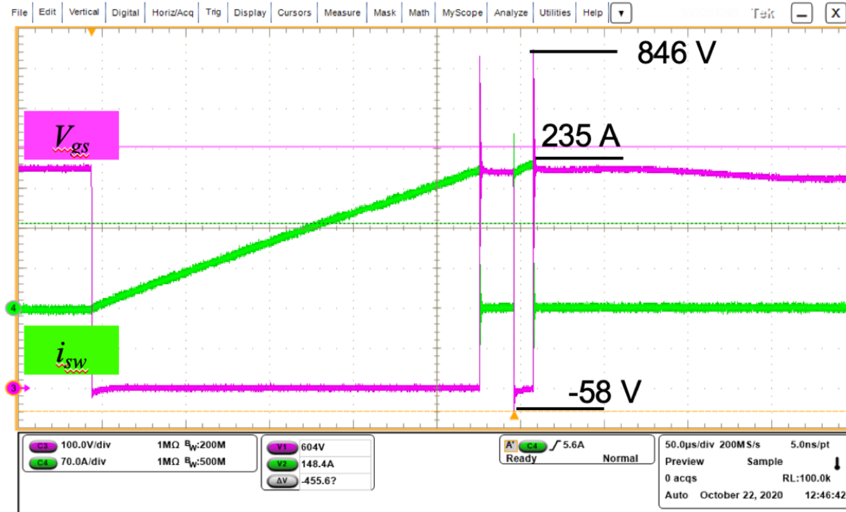
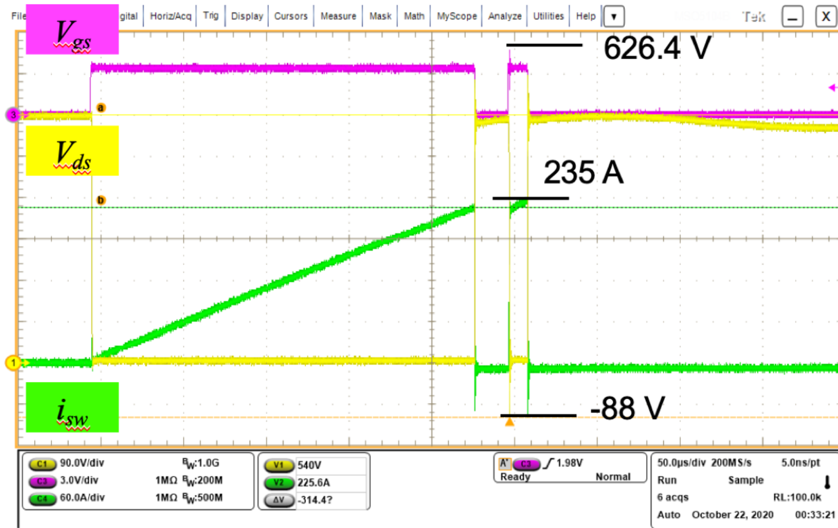


Fig. 4- 14. Double-pulse testing setup.



(a)



(b)

Fig. 4- 15. Double-pulse testing results of (a) top switch, and (b) bottom switch.

4.4.2 Low-pass-filter effect caused by coil stray capacitance

The experimental testing results of the RSCS in a 3-pulse test are shown in Fig. 4- 16, where v_{gs}, i_{sw}, v_{int}, and v_{rscs} are the gate signal, switch current, integrator output, and RSCS output, respectively. By comparing the sensor output v_{rscs} and the switch current i_{sw}, it is found that v_{rscs} did not follow i_{sw}. A low-pass-filter (LPF) effect existed in the RSCS sensor. As a result, some

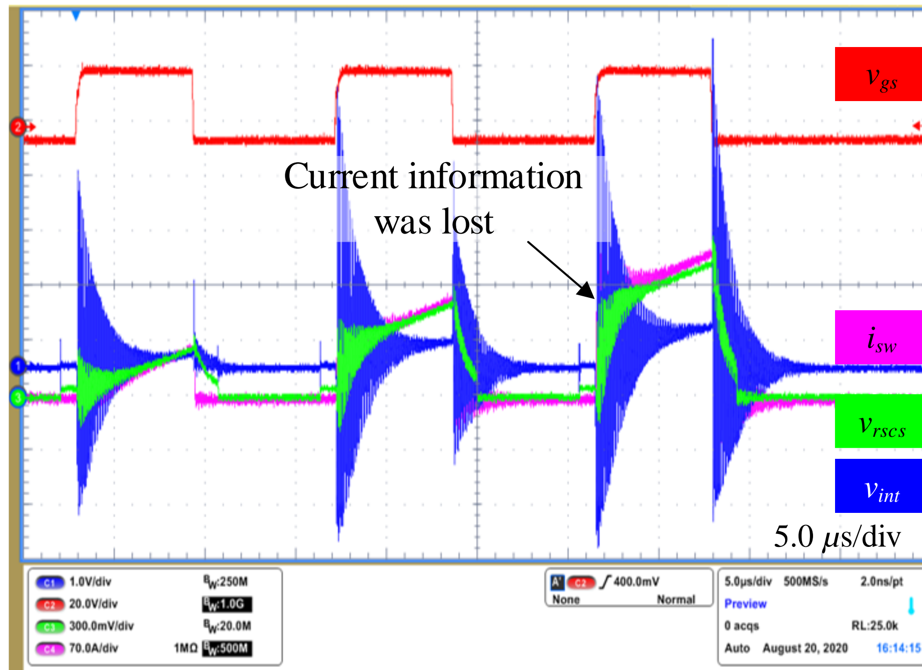


Fig. 4- 16. Experimental testing result of the RSCS with shield layers.

current information was lost at switching transient, and it was worse at higher *di/dt*. The LPF effect is not acceptable in RSCS design; it disables the SC protection that leads to damages in the system when a fault exists. The LPF is formed by the coil self-inductance L_s and stray capacitance C_s. Since sufficient L_s is necessary to provide sensing gain of the RSCS, effort should be made to reduce the C_s.

The C_s is determined by the coil structure and the shield layers. To investigate the impact of the shield layers on C_s, two coil designs illustrated in Fig. 4- 17 were compared. Fig. 4- 17 (a) shows the original design and Fig. 4- 17 (b) shows the design without the shield layers. According to the 3D simulation, the original design performs 43.1 pF stray capacitance, while the stray capacitance drops to 5.3 pF by removing the shield layers. Shield layers increase the stray capacitance because they add more conductors to the RSCS coil. To ensure a reliable SC protection, shield layers were removed from the RSCS coil.

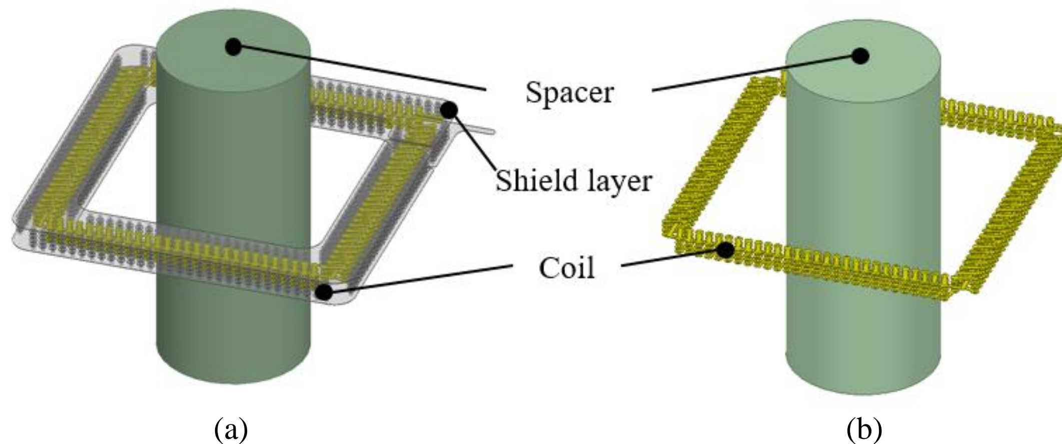


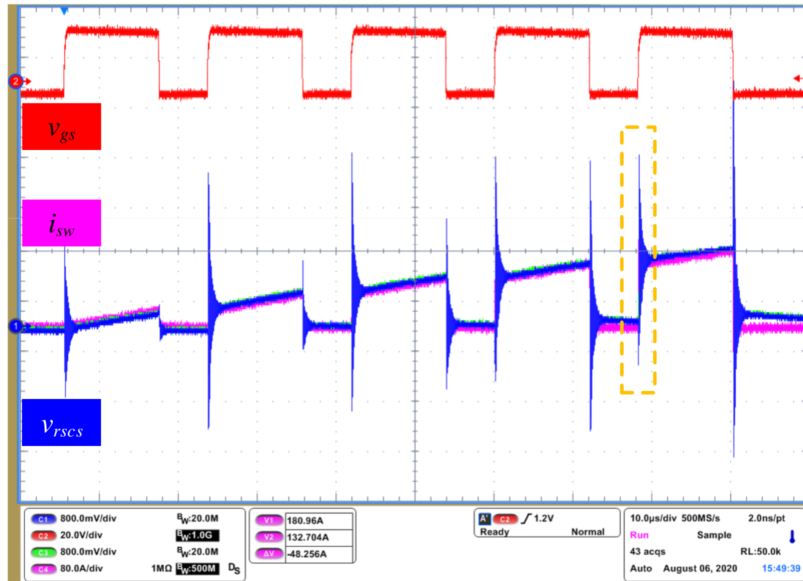
Fig. 4- 17. Q3D simulation model of (a) with shield layers, and (b) without shield layers.

The experimental testing results of the RSCS without shield layers in a five-pulse testing at 130 A are shown in Fig. 4- 18. As can be seen, the RSCS successfully tracked the switch current, which verifies that the RSCS performance is improved by removing the shield layers. No CM noise was found in the system.

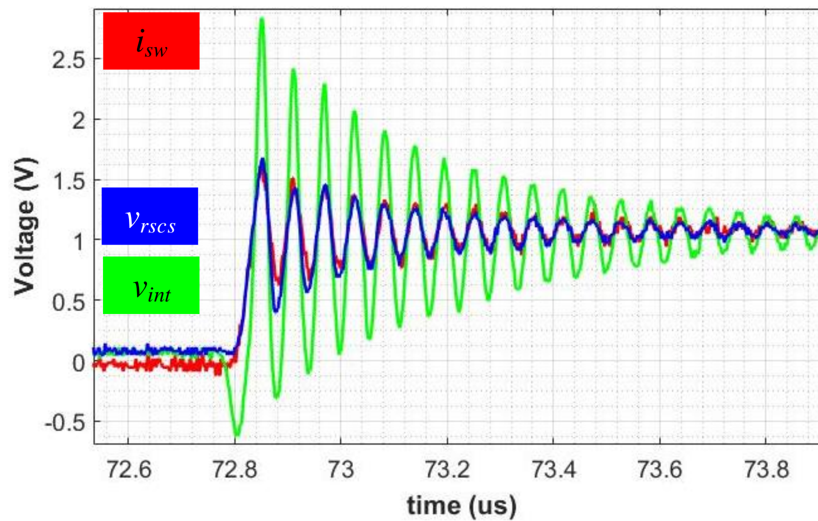
4.4.3 **Preshoot effect and possible solutions**

By removing the shield layers from the RSCS coils, the LPF effect issue was successfully solved with switch current up to 130 A. However, when the switch current went up, another issue existed, which is illustrated in Fig. 4- 19. As seen, undesired offset voltages were found at the RSCS output. They appeared at random, and their values were unpredictable. The offset voltages are also unacceptable in the RSCS design because they might falsely trigger SC protection that affects GRU operation or disable the SC protection that causes circuit damage.

The offset voltages are caused by the pre-shoot effect in the integrator. The equivalent circuit and the waveforms of the integrator affected by the pre-shoot effect are shown in Fig. 4- 20. The Rogowski coils output the $-Mdi/dt$ value feeding the integrator input. If the switching speed is very fast, the $-Mdi/dt$ value becomes so large that it will induce a step voltage at the integrator



(a)



(b)

Fig. 4- 18. (a) Experimental testing result of RSCS without shield layer, and (b) zoom-in waveform in a five-pulse testing.

input. Since the op-amp is not ideal and it needs response time, the step-like voltage will cross through the integrator resistors R_i and capacitor C_i to the output V_{int} until the op-amp enters normal operation.

The 1200 kV, 475 A SiC half-bridge modules GE12047BCA3 from General Electric (GE)

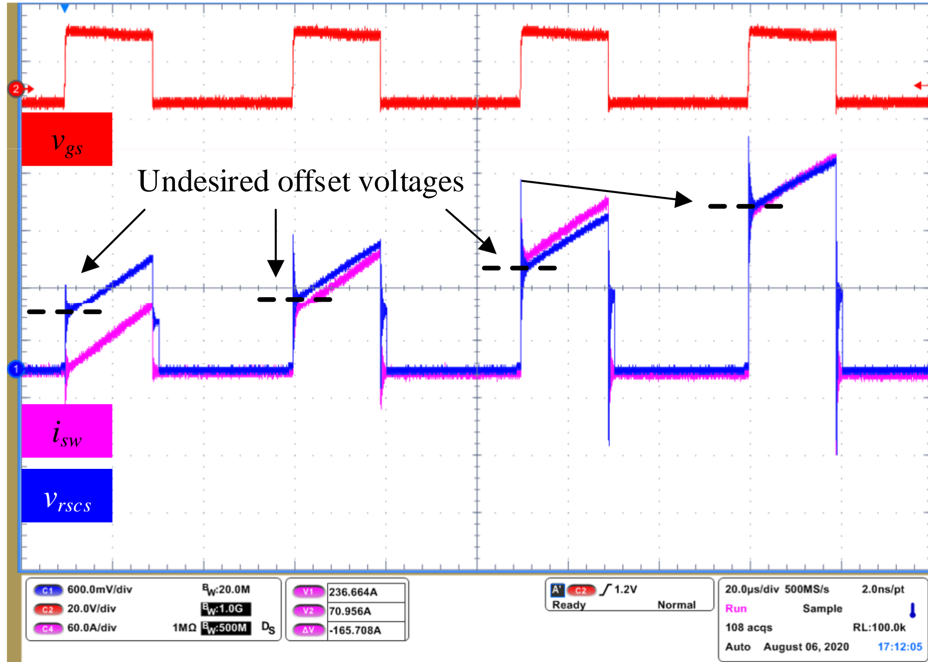
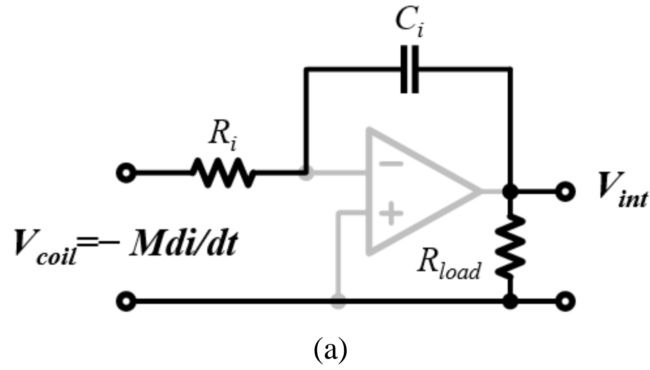


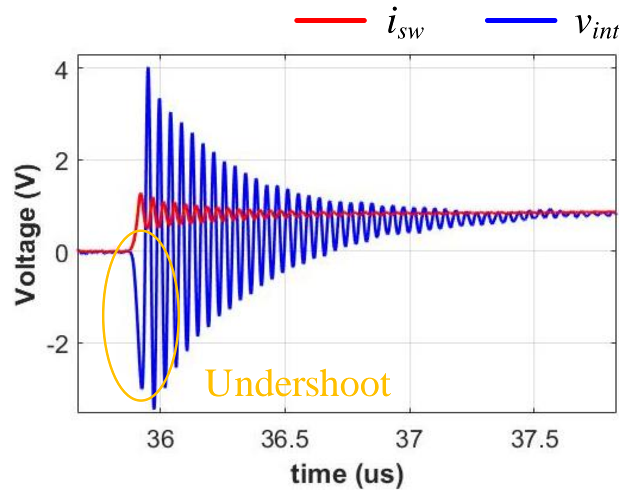
Fig. 4- 19. Undesred offset voltages at RSCS output when i_{sw} > 130 A.

[129] are adopted to build the GRUs. The main feature of these modules is the use of the GE-proprietary power overlay technology that allows for internal us structures with exceedingly low parasitic inductance value of less than 5 nH. Because of the extremely small parasitic inductance, the *di/dt* of the switch current i_{sw} at 235 A can reach 16 A/ns, which is six time larger than its competitors are. As a result, the pre-shoot effect existed and it makes the RSCS malfunctional.

There are several methods to eliminate the pre-shoot effect. In [130], different integrator circuits are compared. The comparison reveals that a non-inverting integrator alleviated the pre-shoot effect because it removes the path between the input and output of the op-amp. However, the gate driver processing circuit needs to be redesigned which would mean extra cost and time. Another solution is to add a voltage divider consisting of two resistors between the Rogowski coil and the integrator. This method is equivalent to reducing the mutual inductance M. The zoom-in waveforms of i_{sw} and v_{rscs} are shown in Fig. 4- 21. As seen, no pre-shoot effect was found. This



(a)



(b)

Fig. 4- 20. (a) The equivalent circuit and (b) waveforms of the integrator that is affected by the pre-shoot effect.

solution is simple and low cost, but it reduces the RSCS sensing gain and makes it easier to pick up noise. The last solution is to slow down the module switching speed by adding more gate resistance. The drawback of this solution is that the switching loss will increase. However, since safe operation is the highest priority, and the switching speed is still very fast even with higher resistance, it does not degrade the system performance. Therefore, it is adopted to solve the pre-shoot effect. The experimental waveform is shown in Fig. 4- 22. As seen, the RSCS successfully tracks the switch current, verifying a safe and reliable SC protection to the system.

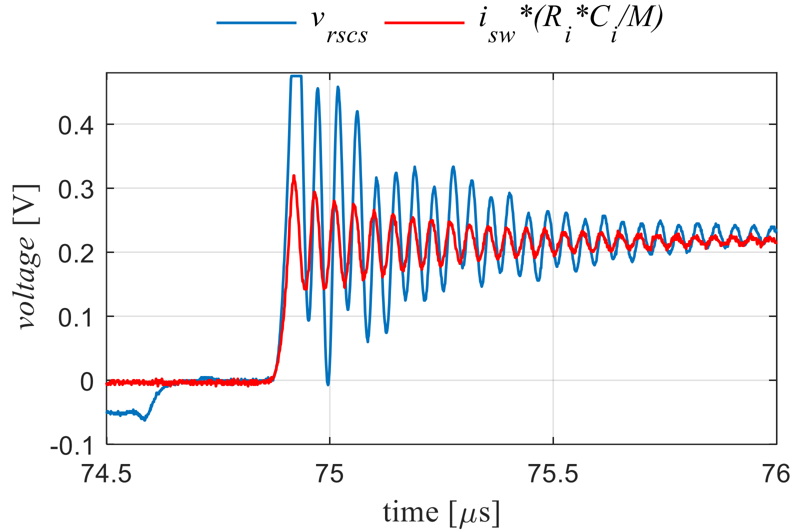


Fig. 4- 21. Waveform comparison between RSCS output and converted switch current.

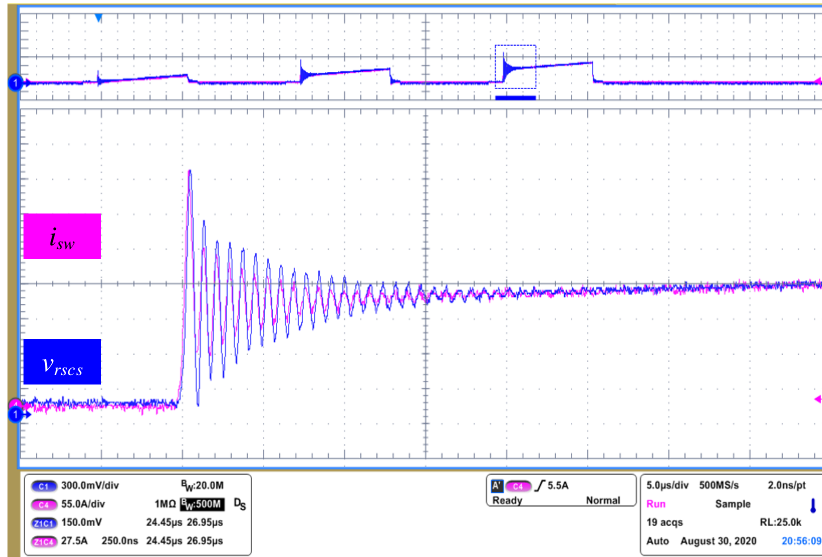


Fig. 4- 22. Experimental waveform of the RSCS output and switch current in the three-pulse test.

4.4.4 **Partial discharging testing at 50,000 ft**

Partial discharging (PD) tests were conducted in an altitude chamber to ensure that the proposed gate driver can withstand its target voltage of 540 V without any PD at 50,000 ft. As shown in Fig. 4- 23, all exposed pads at the same voltage potentials were tied together by copper tapes. 540 V was applied to the top-side driving circuit, while the voltage potential of the bottom-

side driving circuit was connected to the ground. By controlling the air density in the altitude chamber, the air condition at different altitude can be emulated. Fig. 4- 24 depicts the partial discharging inspection voltage (PDIV) at different altitude, showing that the insulation strength degrades with the growth of the altitude. The PDIV at 50,000 ft is 617.2 V, successfully meeting the insulation target. As shown in Fig. 4- 25, breakdown existed at the edge of the bottom-side driving circuit. This is due to the short distance between the connectors to the top and bottom MOSFET, which agrees with the conclusion given by the 3D FEA simulation discussed in 4.3.3. This distance determined by the half-bridge module becomes the constraint in the insulation design.

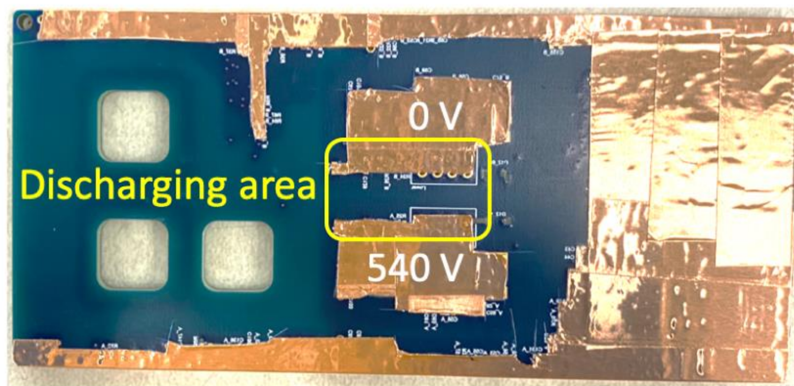


Fig. 4- 23.Top view of the gate driver PCB for partial discharging testing.

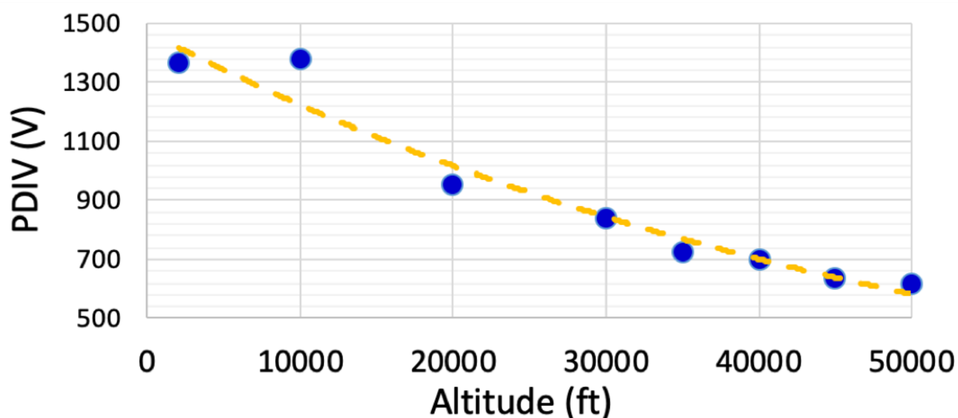


Fig. 4- 24.Partial discharging inspection voltage at different altitude.

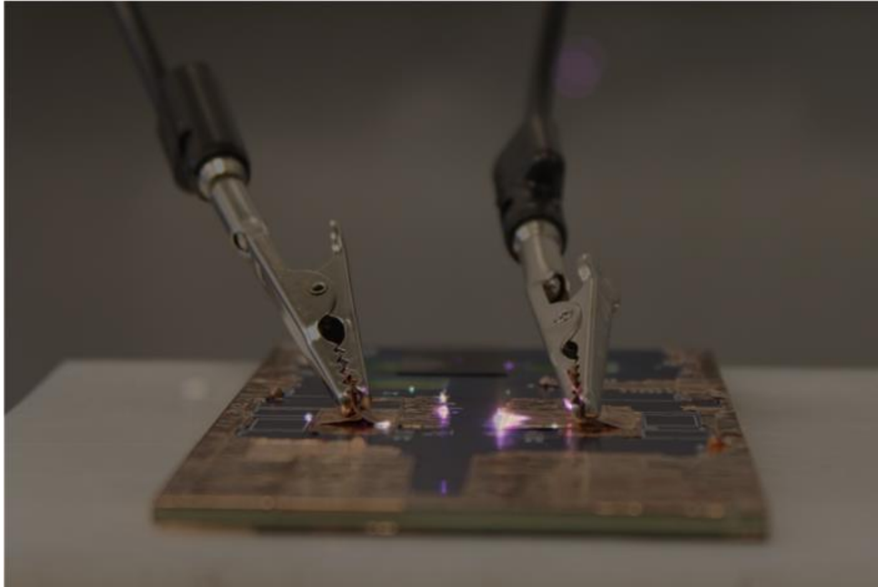


Fig. 4- 25.Partial discharging area.

4.4.5 **Three-phase continuous testing**

The final assembly of the GRU is shown in Fig. 4- 26. Three SiC modules are placed on the bottom of the GRU. The AC, +DC, and –DC terminals are connected to the busbar by spacers. The AC spacers in the busbar are extended to connect the three-phase inductor. The gate drivers

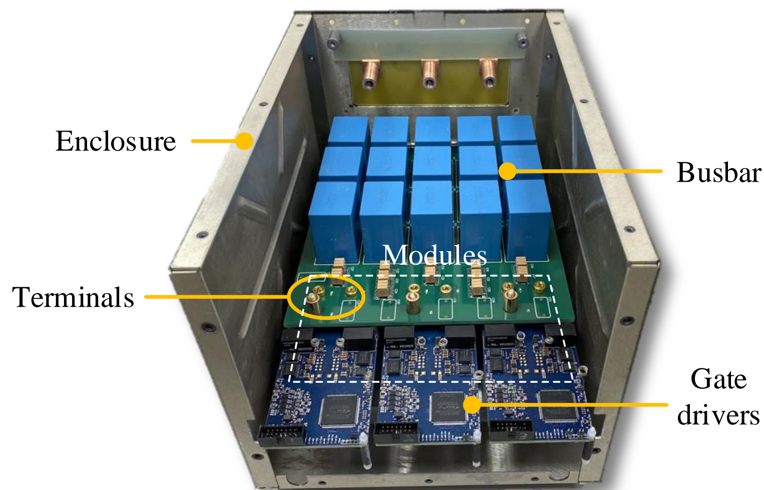


Fig. 4- 26.Assembled GRU.

are inserted between the modules and busbar to sense the switch currents. The testing setup for the three-phase continuous test is shown in Fig. 4- 27. An interface board is connected to the GRU and communicates to the gate drivers.

The experimental waveform of the three-phase continuous testing is shown in Fig. 4- 28, where line-to-line voltage v_{LL} and three phase current i_a, i_b, i_c, are measured.

Fig. 4- 27.Test setup for three-phase continuous testing.

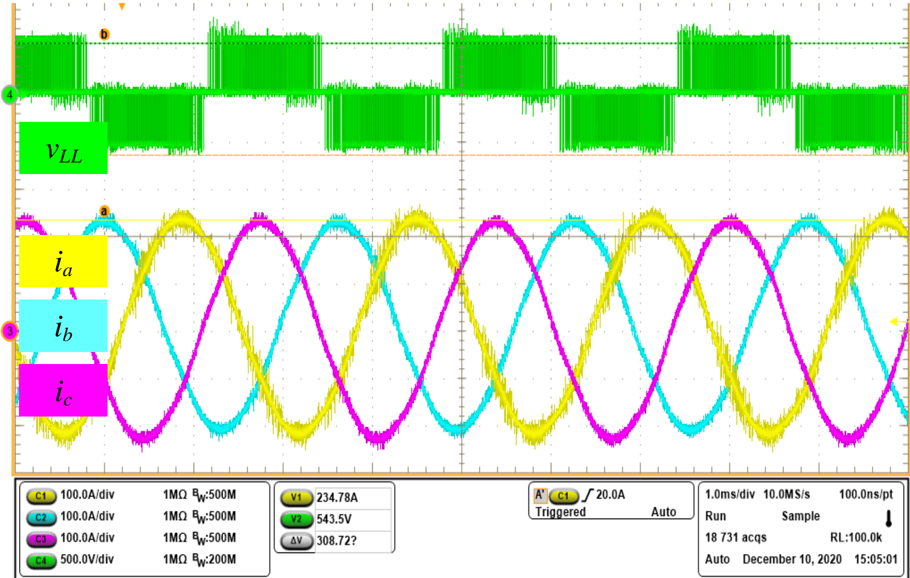


Fig. 4- 28.Experimental waveform of the three-phase continuous testing at 540 V, 235 A.

The bus voltage is 540 A and the peak phase current is 235 A. The whole unit ran for over 30 minutes, successfully verifying the design.

4.5 Summary and conclusions

In this chapter, a comprehensive design of an enhanced gate driver for SiC based GRU for airborne applications is presented. To maximize the power density, breakdown voltage in Paschen curve was converted to the break down E field to determine the insulation co-ordination. E-field management is applied to the gate driver layout by properly designing the field control plates, by which the peak E field successfully shifted from the air to fr4 that features much higher dielectric strength. The gate driver prototype attains a small size of 128.7 mm × 61.2 mm × 23.8 mm, significantly contributing to the system power density.

Chapter 5 Design of USB-C Power Delivery Charger for Aircraft Applications

In this chapter, the stage of an integrated, highly compact USB Type-C Power Delivery (PD) charger for aircraft applications is presented. The high-frequency isolated dc-dc converter has the following specifications: 15 -100 W, 5-20 V dc output, feeding from a 200 V input bus. The main challenge in this work is to achieve high power density and high efficiency over four nominal outputs. A LLC resonant converter was adopted because of its soft-switching feature and good regulation. A flying-capacitor-based voltage divider (FCVD) switching bridge is proposed to provide additional voltage gain, which significantly improved the efficiency and power density.

In this chapter, an overview of the proposed FCVD switching bridge is first illustrated. Thereafter the detailed operation of the 2-switch-cell (2S) FCVD-LLC resonant converter and 4-switch-cell (4S) FCVD-LLC resonant converter are provided. Circuit design, including switch cell selection, turns ratio selection, operation mode selection, inductances and resonant tank design, is then presented. Multi-objective optimization (MDO), seeking to achieve maximum power density and efficiency in the four nominal operations, is applied to the transformer. Prototypes were built and tested, verifying that the design successfully achieves the targeted efficiency and power density.

5.1 Introduction

5.1.1 **Overview of USB-C PD charger**

Nowadays, portable electronic devices are growing dramatically at an incredible speed with new and sophisticated functionality [131], [132]. These multifunctional devices need to be charged

at regular intervals at defined voltage and power levels. The Universal serial bus (USB) has become a ubiquitous protocol for connectors for electronic devices. To increase the power delivery, a new USB specification known as USB power delivery (PD) has been rencently introduced [133]. With USB PD, power can achieve up to 100 W because the voltage can be increased to 20 V and current can be increased up to 5 A. Thanks to the USB PD specification, the number of applications that can be powered using a USB cable is extended. As shown in Fig. 5- 1, instead of just being restricted to smartphones, cameras, and smaller electronic devices, higher power consuming devices like desktops, tablets, and monitors can be powered through a USB charger.

The USB Type-C plug interface has 24 pins and is shown in Fig. 5- 2. The D+ and D- pins are differential pairs used for the USB 2.0 connectivity. The RX and TX differential pairs can be used for a USB 3.0/3.1 protocol or be utilized by other USB Type-C functionalities. Channel configuration pins perform functions such as cable attachment and removal detection,

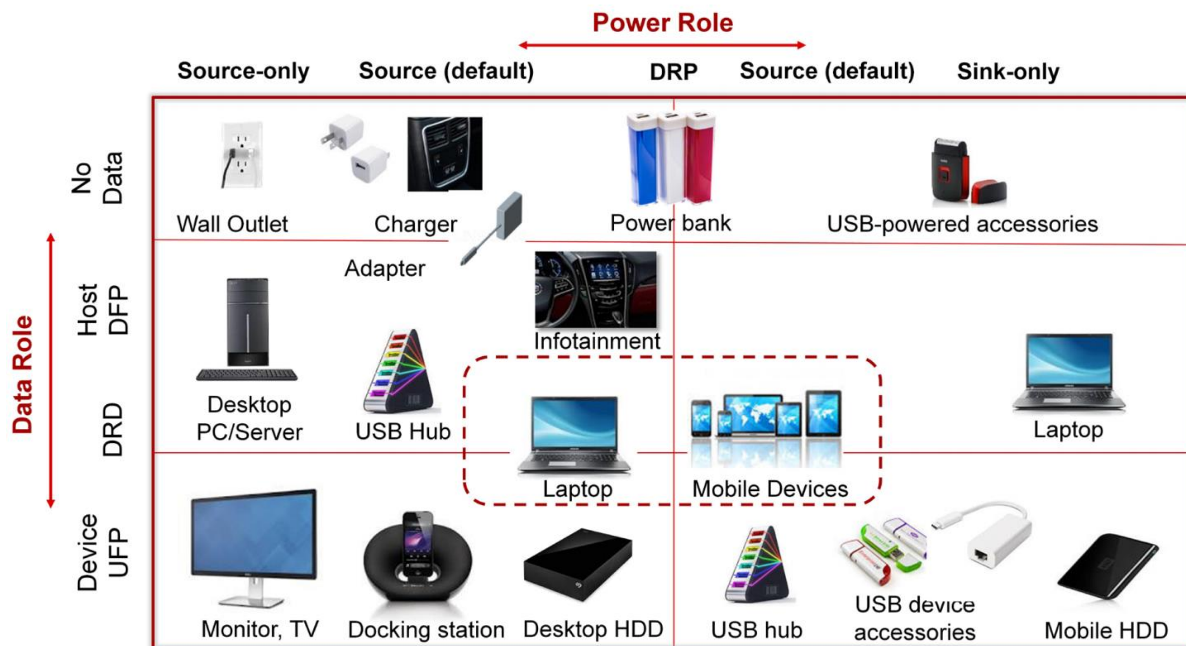


Fig. 5- 1. USB Type-C example apTable 5- I. USB Type-C Power Delivery Charger

receptacle/plug orientation detection, and current advertisements. V_{bus} and GND pins are the power and return paths, which can deliver a maximum power of 100 W.

A monotonic incremental power rule regarding the USB PD is shown in Fig. 5- 3. According to the rule, it supports 5-20 V, and there are four voltage rails, which are 5 V, 9 V, 15 V and 20 V, respectively. The USB PD specification enforces voltage profiles as a function of maximum power. For example, if the power advertised on a port is more than 15 W, 9 V shall be offered. Because of the monotonic incremental power rule, there are four nominal operation points to be optimized, namely 5 V/3 A, 9 V/3 A, 15 V/3 A, and 20 V/ 5 A, respectively.

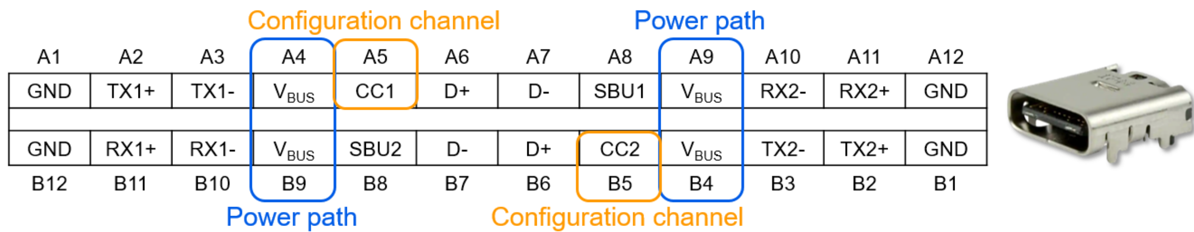


Fig. 5- 2. Pin diagram of USB Type-C connector.

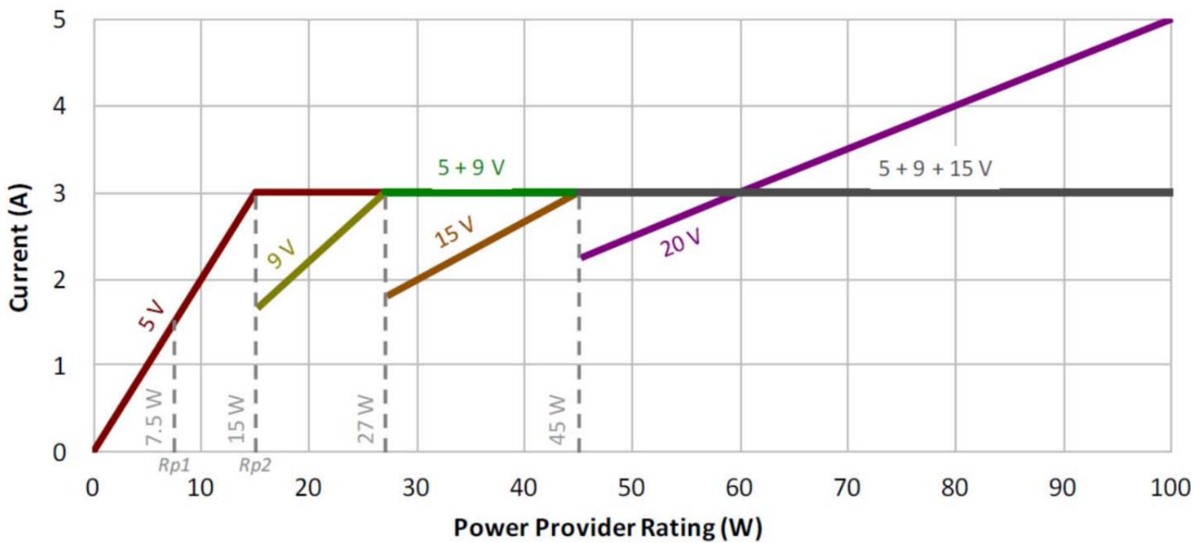


Fig. 5- 3. USB power rule [133].

5.1.2 Survey of power delivery system

Fig. 5- 4 shows the state-of-the-art ac-dc-dc converters and chargers for consumer electronics and aircraft applications. There are many commercially available USB Type-C PD chargers with the power density ranges from 5.7 to 12.5 W/in^3 [134]-[136]. Recently developed power delivery systems from serveral research groups and industry are shown in [137]-[140]. Fig. 5- 5 depicts an aircraft in-seat power system architecture from Astronic [137], which illustrates the use of a Type-C USB PD unit to power multiple USB outlets within a seat group. Fig. 5- 6 shows the specific unit in question, a 240 W (4 × 60 W), 3.3 W/in^3 EmPower charger with alternative outlet modules. These units are typically fed from a 115 V, 400 Hz ac bus. Apprareo developed a dual port, USB charger [138] for portable electronic devices used in aircraft applications; it supports 60 W (2 × 30 W) with a power density of 13.9 W/in^3. Ribarich [139] designed a 150 W universal ac input PFC front end, an LLC step down adapter, which achieved 94.7 % efficiency and 39.3 W/in^3 power density. A 300 W GaN-based ac-dc converter was designed by the same research group; the efficiency and power density are 95 % and 29 W/in^3, respectively [140]. From the state-of-the-art

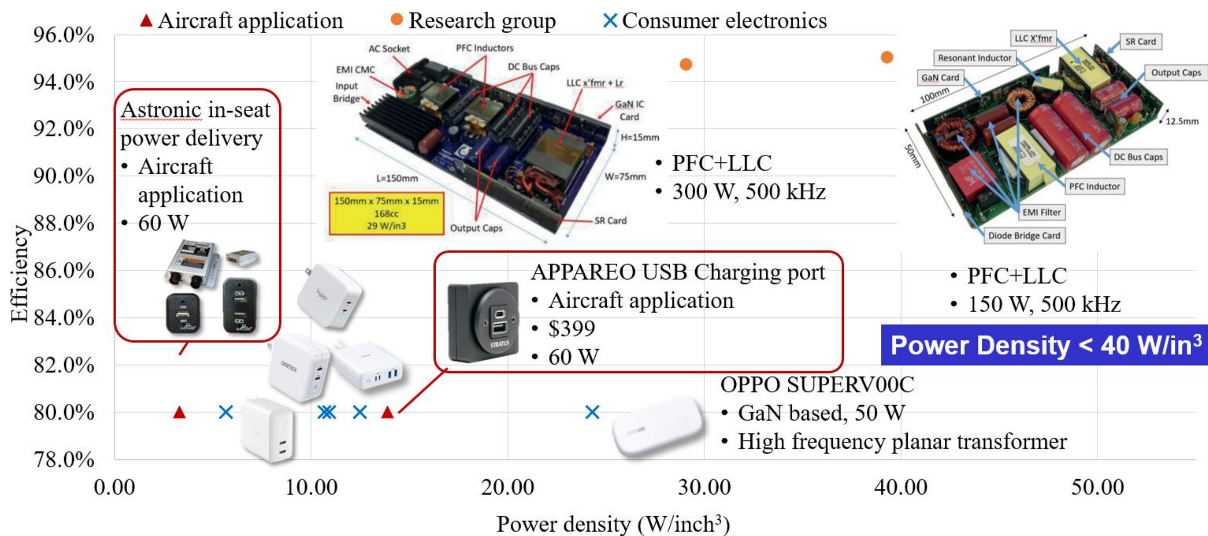


Fig. 5- 4. State-of-the-art ac-dc converter and chargers.

ac-dc-dc converters, it is found that their power density is all below 40 W/in^3, which represents one of the main challenges in this work.

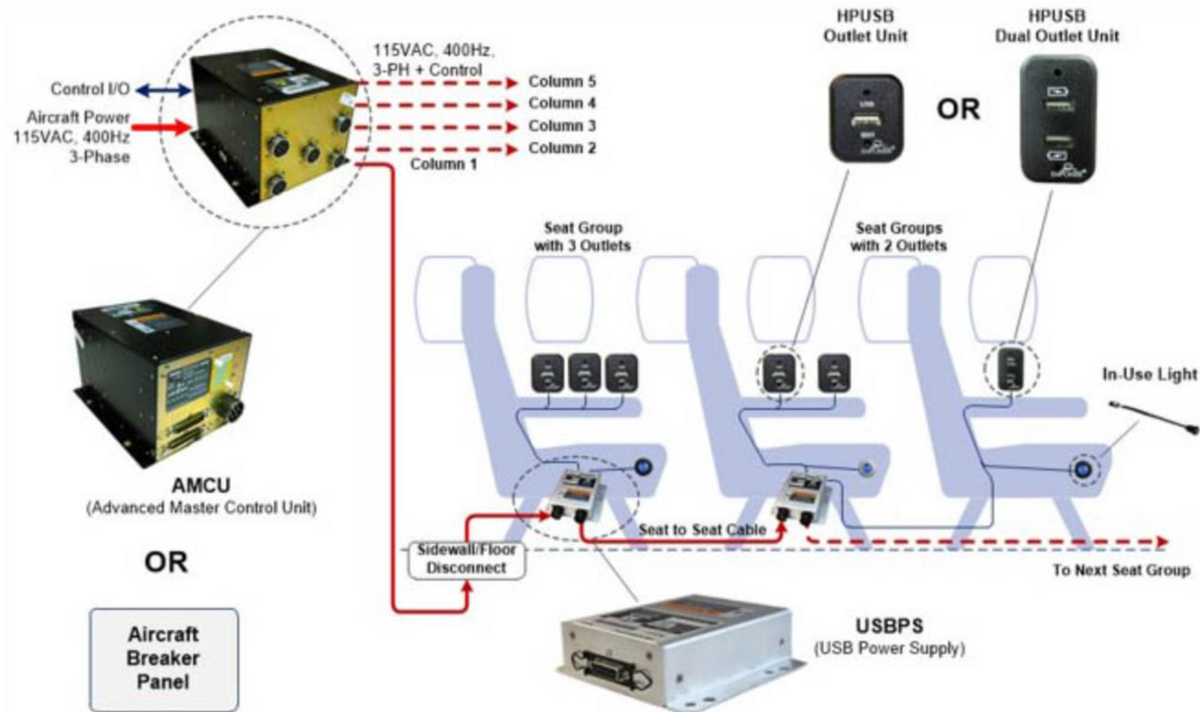


Fig. 5- 5. Block diagram of Astronics USB in-seat power system [137].

Fig. 5- 6. Astronics EmPower Type-C USB PD unit [137].

5.1.3 **Design challenges**

The specification of the USB-C PD charger in question is listed in Table 5. 1. As previously mentioned, USB PD chargers provide 5 V, 9 V, 15 V and 20 V output voltages, successfully extending the number of applications that can be powered using a USB cable. However, in the design of USB-C PD chargers, four nominal operating points need to be optimized simultaneously.

Table 5. 1. USB Type-C Power Delivery Charger Specification

Input	96 to 130 Vrms, 360 to 800 hz
Output	5 V/ 3 A, 9 V/ 3 A, 15 V/ 3A, and 20 V/ 5 A
Altitude	10,000 ft
Power density	50 W/inch^3
Efficiency	> 83 % @ nominal, >75 % @ 10% load

In most cases, it will be difficult to find one solution that fits all nominal operating points because each of them has its own optimization focus.

Since the output voltage range of the USB-C PD charger is very wide dependent upon the different charged applications, voltage regulation becomes challenging. If PWM converters are used, their controllers have to provide sufficient duty cycle capability; otherwise, the converters might fail to regulate the output. Moreover, the wide-voltage-range requirement leads to very limited acceptance of the region of transformer design, which would degrade converter performance. A similar problem appears in the resonant converter. The wide-voltage-range capability requires a wide range of switching frequency, which brings difficulties in control design. Also, at higher voltage gain operation (e.g., 20 V voltage rail), the switching frequency deviates from the resonant frequency greatly, making it very hard to optimize the converter, thus compromising the overall efficiency [141].

The USB-C PD charger proposed in this dissertation operates at 10,000 ft. Since the air density decreases at high altitude, the insulation strength degrades. Many standards provide altitude correction factors for clearance distance to ensure safe operation, but these correction factors are usually very conservative. Using those correction factors results in an oversized design.

5.1.4 **Technical approaches**

With the introduction of wide bandgap (WBG) devices, the switching frequency of the converter can be pushed to the order of megahertz, which opens up the opportunity to shrink the

size of the magnetic components and increase the converter power density [142]. In recent years, with the rapid development of printed circuit board (PCB) technology, research into power converter design that includes a low-profile planar magnetic component and PCB winding technologies has attracted widespread attention. Compared to conventional wire-wound magnetic components, PCB winding planar magnetic components provide many advantages, such as low profile, good thermal characteristic, ease of manufacturability, cost reduction, modularity, etc [143]. Besides, as solid insulators, they have a much higher dielectric strength (>40 kV/mm) compared to dry air (3.3 kV/mm). With this feature, electric field (E-field) control methodology is applied to the layout design, shifting the peak E-field from the PCB surface in the air to the PCB dielectric, which effectively reduces the E-field in the air.

The USB-C PD charger presented in this chapter requires a wide-output range from 5 V to 20 V, making it very difficult for conventional PWM converters to achieve high efficiency. For example, to ensure zero-voltage switching (ZVS) in all operation ranges, a large switching turn-off current is required, which results in large turn-off loss [144], [145]. This issue can be solved by using an LLC resonant converter, in which the magnetizing inductor current i_{Lm} is utilized to realize ZVS in all load conditions, and there is no need to increase turn-off current. As a result, turn-off switching loss is significantly reduced. Furthermore, when the converter switching frequency is equal or less than the resonant frequency, secondary rectifiers will work under a zero-current switching (ZCS) condition, which effectively reduces the switching loss of the secondary rectifiers.

A conventional half-bridge (HB) LLC with a center-taped connection is shown in Fig. 5- 7. The switching bridge generates a square waveform to excite the resonant tank. The resonant tank constructed by a resonant capacitor C_r and a resonant inductor L_r, outputs a resonant sinusoidal

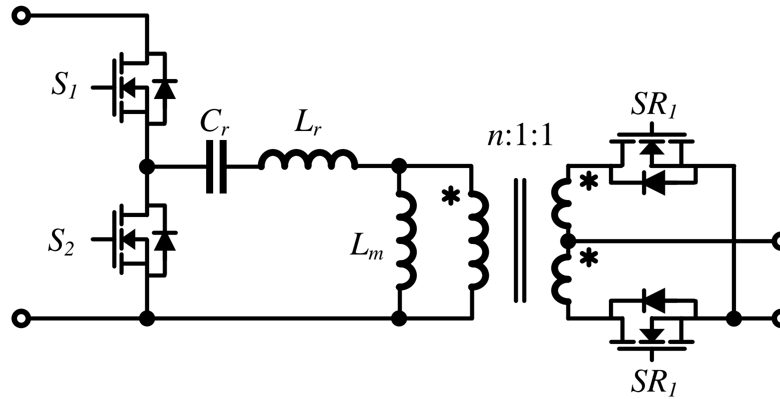


Fig. 5- 7. Conventional LLC resonsant converter with center-taped connection.

current that is scaled and rectified by the transformer and rectifier circuit [146]. At resonate frequency f_r, the converter gain equals to one. By adjusting the switching frequency f_s, the resonant tank impedance is changed, and the voltage gain is changed accordingly. In this way, the LLC resonant converter can work in a wide operation range. However, when f_s is far away from f_r, the efficiency drops significantly due to the higher energy circulating in the resonant tank [147]. This characteristic will not affect converter performance in some applications such as power supplies in a distributed power system. It only happens during the holdup time that is normally in tens of milliseconds, but it will degrade converter performance severely if it is designed in nominal operations. To tackle this problem, variable intermediate dc-link voltage was adopted by several research groups [148]-[152]. The key approach of the variable intermediate dc-link voltage is to track the maximum efficiency point of the second stage dc-dc resonant converter in each operation and change the intermediate dc-link voltage accordingly. In this manner, the resonant converter always operates around its optimal point, but it scarifies the ac-dc stage efficiency. Moreover, the increased dc-link voltage adds more voltage stress on the power semiconductor devices. As a result, many device candidates with smaller ON-state resistance $R_{ds,on}$ and output capacitance C_{oss} are left out. Taking all of the above into consideration, variable intermediate dc-link voltage is not

considered in this work.

Apart from the wide operating range requirement, the high step-down ratio of the USB Type-C PD charger also causes some problems. According to the specification listed in Table 5. 1, the minimum intermediate dc-link voltage is 200 V. With a fixed dc-link voltage of 200 V, the step-down ratio of the LLC converter is from 10 to 40. Due to the high step-down ratio and its relatively low power, the quality factor Q of LLC in question is below 0.1. The LLC converter with a low Q value can easily meet the gain requirement, but it will lose regulation capability when the switching frequency is above the resonant frequency, which limits the converter voltage gain to be not less than one. In addition, a low Q value means high circulating energy and high rms current, causing high conduction loss. Moreover, since the minimum turns ratio to satisfy the gain requirement is 20, if a conventional HB LLC was used, the voltage across the magnetizing inductance will reach 400 V at 20 V output. This generates a large peak-to-peak magnetizing inductance current.

To reduce the peak-to-peak and rms current flowing through the semiconductor devices and transformer, alternative LLC configurations were investigated. Two popular LLC configurations suitable for step-down converters are shown in Fig. 5- 8. The transformer in primary-series-secondary-parallel (PSSP) configuration depicted in Fig. 5- 8 (a) is also known as a matrix transformer [142], where a single transformer is broken down to a number of elemental transformers interconnected in parallel and series connections. Current stress in secondary rectifiers is relieved, and there is no current sharing issue. However, each transformer is still subject to the same voltage excitation; therefore, the core loss is multiplied and the core size increases. Additionally, there is no improvement in the primary circuit, as the equivalent circuit is the same as the conventional LLC converter after reflecting the secondary circuit to the primary.

The other LLC configuration, primary-parallel-secondary-parallel (PPSP) is illustrated in Fig.

5- 8 (b). By paralleling the power stage, the current stress of all semiconductor devices can be reduced. However, the component count is doubled, and the peak-to-peak value of the magnetizing inductance current increases.

To solve the aforementioned problems, a novel flying-capacitor-based voltage divider

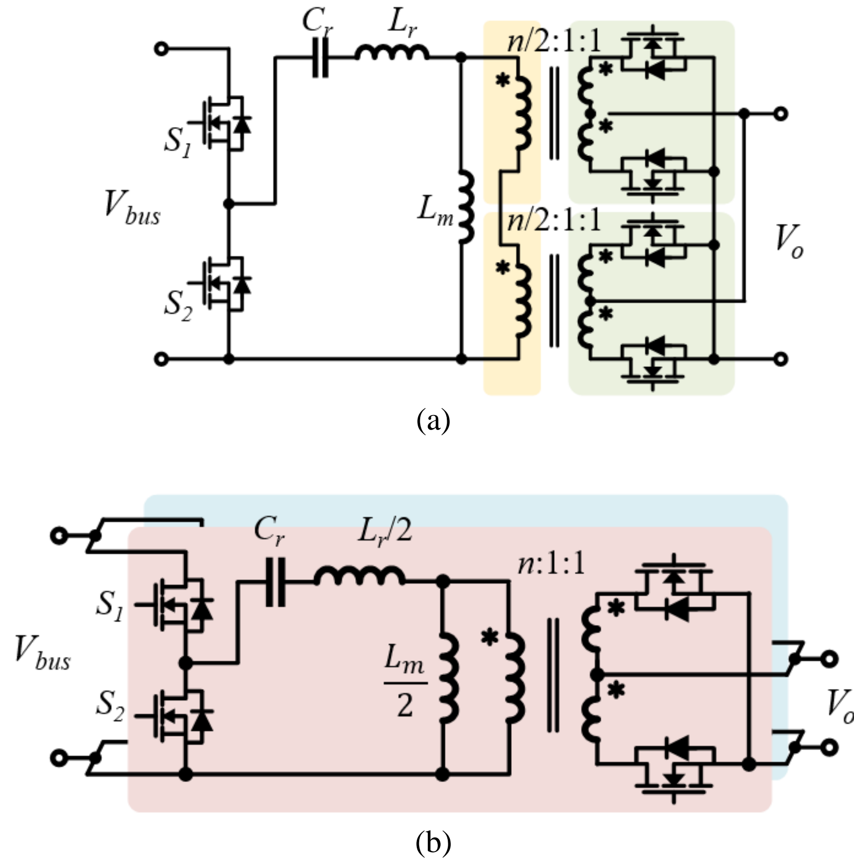


Fig. 5- 8. Alternative LLC configuration: (a) primary series secondary parallel (PSSP), and (b) primary parallel secondary parallel (PPSP).

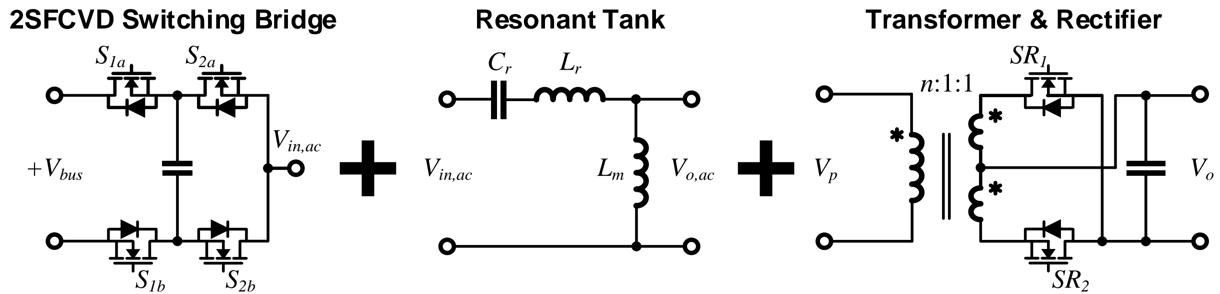


Fig. 5- 9. Structure of proposed 2SIVD-LLC converter with 2-switch cell.

(FCVD) LLC configuration is proposed. The structure of a 2-switch-cell FCVD-LLC (2SIVD-LLC) resonant converter is depicted in Fig. 5- 9. In this configuration, a 2SFCVD switching bridge replaces the conventional HB or full-bridge (FB) switching bridge in the LLC converter. It serves as a voltage divider that can generate multiple voltage levels, and it offers an additional step-down ratio to the LLC converter so the transformer turns ratio can be reduced. The number of voltage levels is determined by the number of switch cell. An N-level FCVD will have the $(N-1)$ switches cell and $(N-2)$ flying capacitors.

The proposed FCVD has many advantages. First, it is easy to implement. The FCVD can replace the conventional HB or FB directily without changing the operation or circuit of the LLC resonant converter. Seconday, it offers multiple operation modes to match different nominal outputs of the USB Type-C PD charger; therefore, the LLC converter can always operate around resonant frequency without scarifying the efficiency of the ac-dc stage. Third, at operations except full-bus mode (FBM), the switching frequency is lower than the magnetic component frequency. The switching loss of the power semiconductor devices is much lower in a FCVD switching bridge than a conventional HB or FB switching bridge at the same magnetic component frequency. Fourth, the self-balanced flying-capacitor structure reduces the voltage across semiconductor devices, which allows lower voltage rating devices with smaller parasitics and footprint to be used. Fifth, the transformer turns ratio is reduced significantly, owing to the additional step-down ratio provided by the FCVD, leading to a lower voltage across the magnetizing inductance. It not only cuts down the loss, but also gives more freedom to the transformer design. Lastly, it has rich configurations. It can has split bus configuration that shown in Fig. 5- 10 (a). Four-level and five-level FCVD can also be achieved by adding more switch cells, which are illustrated in Fig. 5- 10

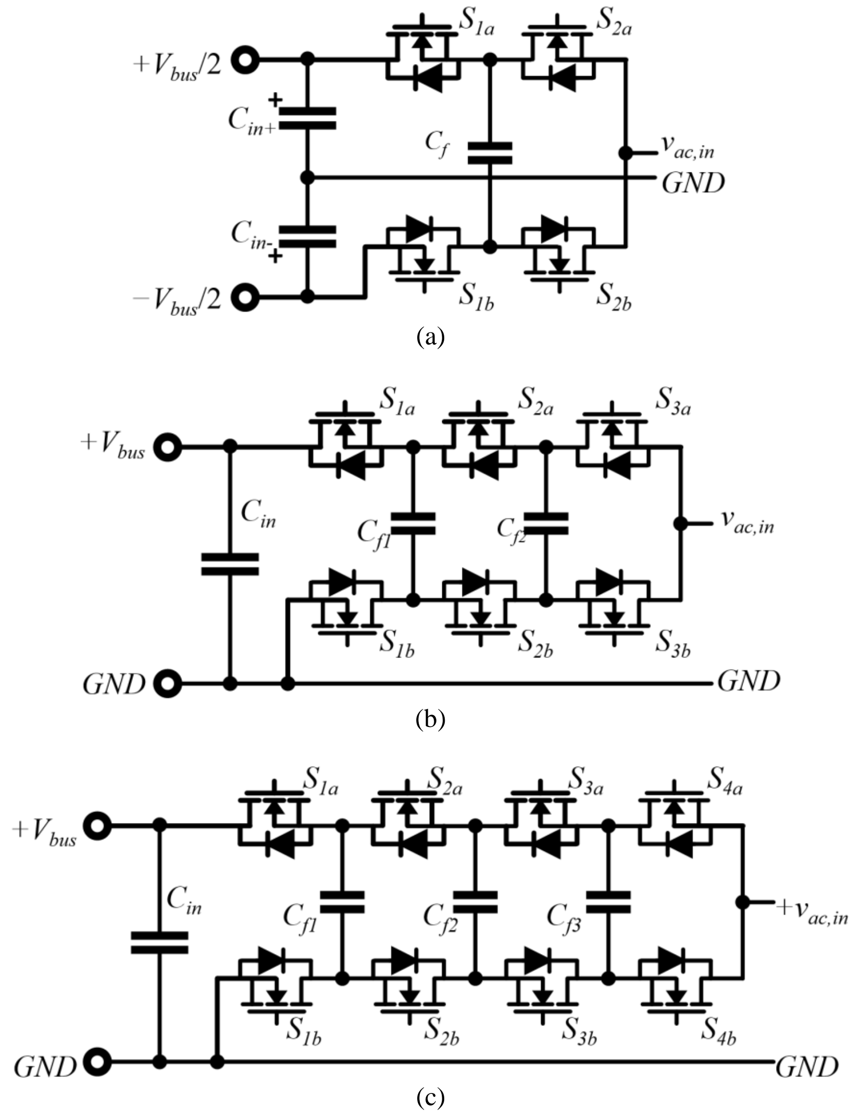


Fig. 5- 10. Alternative FCVD configurations: (a) 2SFCVD with split bus, (b) 3SFCVD, and (c) 4SFCVD.

(b) and Fig. 5- 10 (c), respectively. The selection of the FCVD configuration can be done according to the system specifications.

In this chapter, a detailed operation of the 2SFCVD-LLC and 4SFCVD-LLC converter will be given. The 2SFCVD-LLC is adopted to demonstrate the design. Following this, the converter design, including circuit design, transformer optimization, and component selection is discussed in detail. Finally, prototypes are built to verify the design.

5.2 Flying-Capacitor-Based Voltage Divider (FCVD) LLC Resonant Converter Analysis

5.2.1 2SFCVD-LLC resonant converter analysis

5.2.1.1. 2SFCVD switching bridge working principle

The equivalent circuit of a 2SFCVD-LLC resonant converter is shown in Fig. 5- 11. The operation states of a 2SFCVD switching bridge are shown in Fig. 5- 12. The 2SFCVD can output three voltage levels of 0 V, $V_{bus}/2$, and V_{bus}, respectively. In steady-state operation, the flying capacitor C_f naturally balances voltage by $V_{bus}/2$. The gate signals for the top and bottom device of each switch cell (e.g., S_{1a} and S_{1b}; S_{2a} and S_{2b}) are complementary. The corresponding gate signals of S_{1a} and S_{2a} are also provided in Fig. 5- 12, where "1" represents ON and "0" represents OFF. Shown in Fig. 5- 12 (a), all bottom devices are turned on, and the switch bridge output V_{sw}

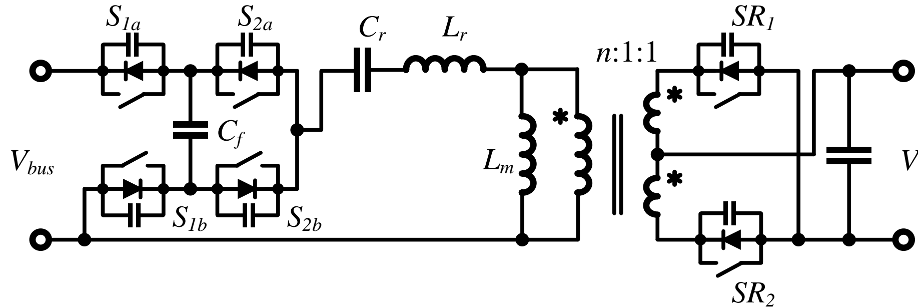


Fig. 5- 11. Equivalent circuit of proposed 2SFCVD-LLC converter.

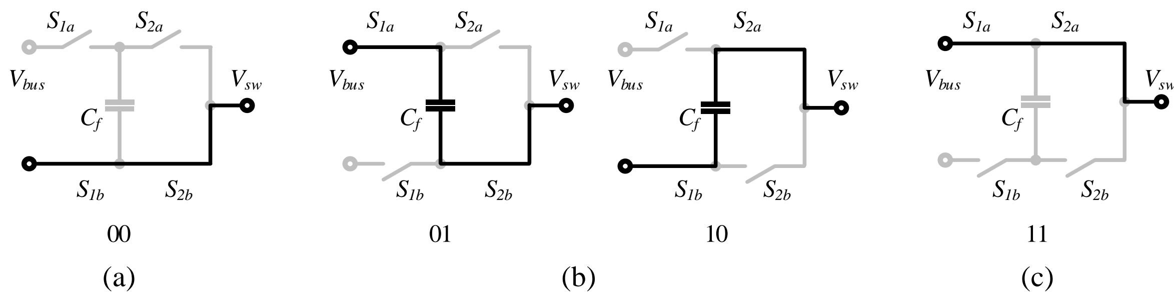


Fig. 5- 12. 2SFCVD switching bridge operation states that output (a) 0 V, (b) V_{bus} /2, and (c) V_{bus}.

is tied to the ground and outputs 0 V. If only one top device is turned on as illustrated in Fig. 5- 12 (b), the flying capacitor C_f is connected to the power loop, and the FCVD outputs $V_{bus}/2$. When all the top devices are turned on, which is depicted in Fig. 5- 12 (c), V_{sw} is connected to V_{bus}. There are two operation modes in 2SFCVD-LLC: half-bus mode (HBM) and FBM, which will be demonstrated in detail as follows.

5.2.1.2. Operation principle in HBM

In HBM, the FCVD switches between 00, 01, and 10 operation states. The switching sequence is 00 → 10 → 00 → 01, and then back to 00. The gate signals and key waveforms are illustrated in Fig. 5- 13. As seen, in one complete switching cycle, FCVD outputs 0 V and $V_{bus}/2$ twice, so the magnetic component frequency f_m=2f_s. Considering the reduced drain-source voltage, the switching loss of the 4SFCVD is only 1/4 of the conventional HB switching bridge at the same

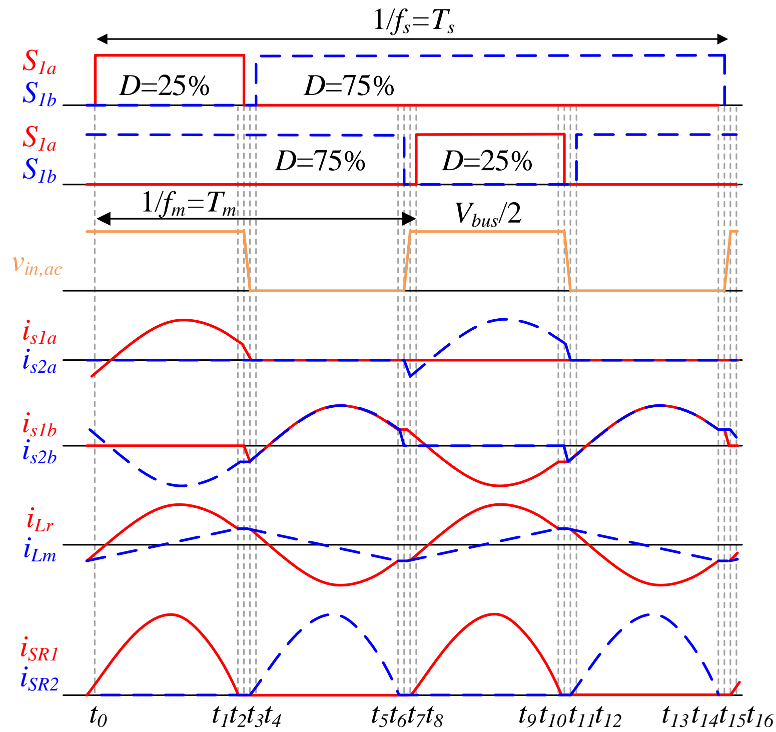


Fig. 5- 13. Gate signals and key waveforms in HBM.

magnetizing component frequency. In the conventional HB or FB LLC converter, the duty cycle defined as the ON time of the top device is always equal to 50 %, while in the 2SFCVD in HBM, the duty cycle of each top device is 25 %. Therefore, the current stress on the top devices is smaller than the bottom devices.

Fig. 5- 14 and Fig. 5- 15 depicts the converter operation states in HBM. Since the proposed LLC resonant converter in this chapter will lose regulation when its voltage gain is lower than one due to its small Q value, the operation where the switching frequency is higher than resonant frequency is not discussed in this chapter. The 2SFCVD-LLC converter operating in HBM has 18 operation states in one switching period T_s, and they are described as follows:

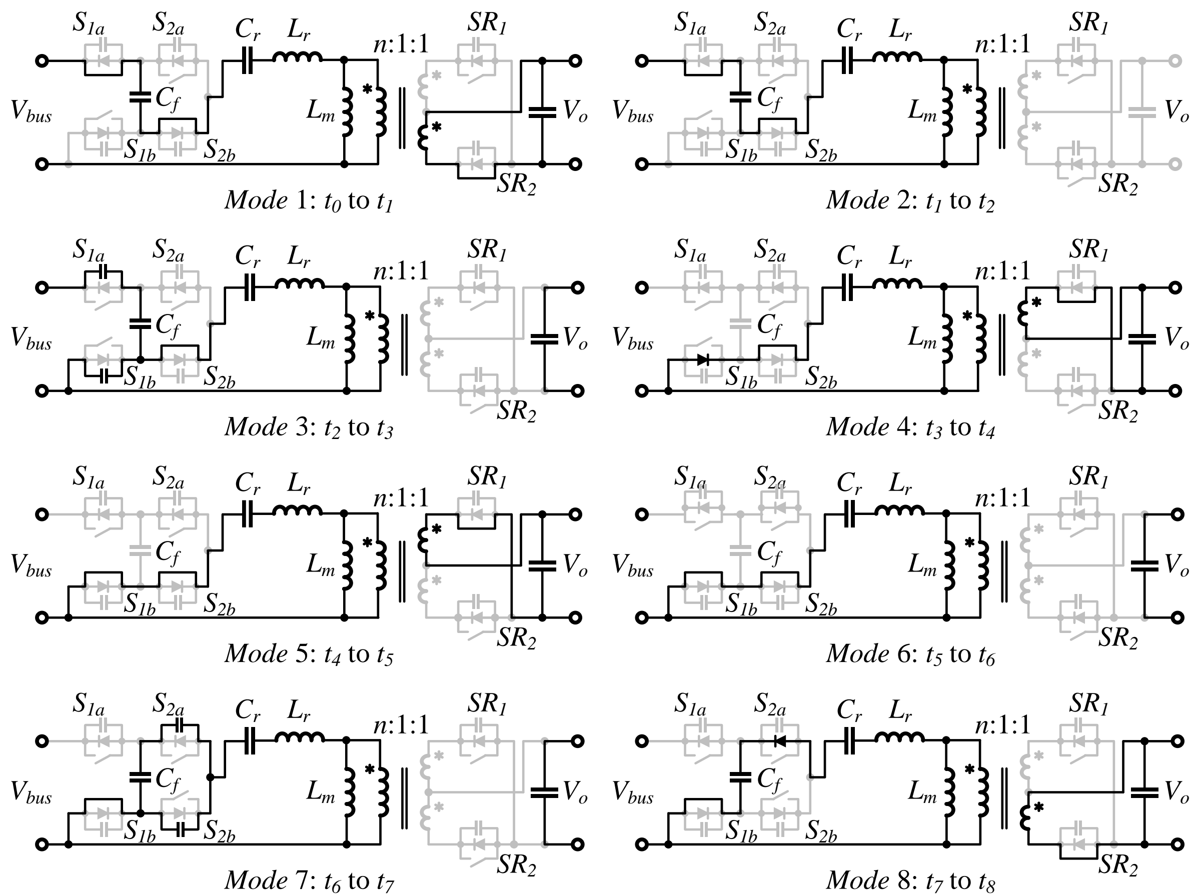


Fig. 5- 14. 2SFCVD-LLC converter operation states in half-bus operation: *Mode* 1 – 8.

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, switch S_{1a}, S_{2b} and flying capacitor C_f are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o, and thus i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_1 and t_2.

3) Mode 3 (*Dead Time*, $t_2 < t < t_3$): At time t_2, S_{1a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a} and S_{1b}. This mode ends when the C_{oss} of S_{1a} and S_{1b} are fully charged and discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of S_{1b} is fully discharged and its body diode starts to conduct. ZVS can be achieved when S_{1b} is turned on at this period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, S_{1b} is turned on and S_{1b} and S_{2b} are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$, and thus i_{Lm} linearly decreases.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally, and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, S_{2b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{2a} and S_{2b}. This mode ends when the C_{oss} of S_{2a} and S_{2b} are fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of S_{2a} is fully discharged and its body diode starts to conduct. ZVS can be achieved when S_{2a} is turned on at this period.

9) Mode 9 (*Power Transfer*, $t_8 < t < t_9$): Between time t_8 and t_9, switch S_{2a}, S_{1b} and flying capacitor C_f are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

10) Mode 10 (*Energy Circulation*, $t_9 < t < t_{10}$): Between time t_9 and t_{10}, switch S_{2a}, S_{1b} and

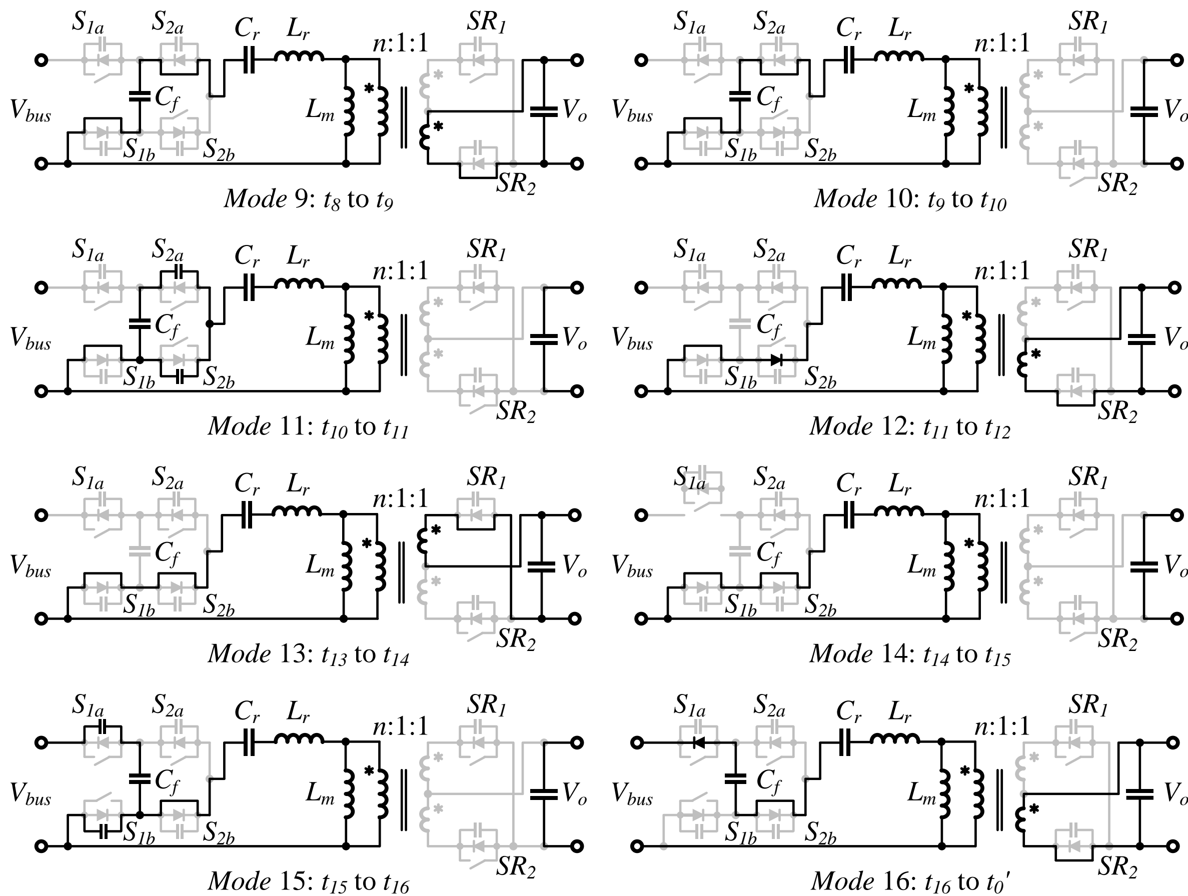


Fig. 5- 15. 2SFCVD-LLC converter operation states in half-bus operation: *Mode* 9 – 16.

flying capacitor C_f are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

11) Mode 11 (*Dead Time*, $t_{10} < t < t_{11}$): At time t_{10}, S_{2a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{2a} and S_{2b}. This mode ends when the C_{oss} of S_{2a} and S_{2b} is fully charged and discharged.

12) Mode 12 (*ZVS Realization*, $t_{11} < t < t_{12}$): At time t_{11}, the C_{oss} of S_{2b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{2b} is turned on at this period.

13) Mode 13 (*Power Transfer*, $t_{12} < t < t_{13}$): At time t_{12}, S_{2b} is turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

14) Mode 14 (*Energy Circulation*, $t_{13} < t < t_{14}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

15) Mode 15 (*Dead Time*, $t_{14} < t < t_{15}$): At time t_{14}, S_{1b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{2a} and S_{2b}. This mode ends when the C_{oss} of S_{1a} and S_{1b} are fully charged and discharged.

16) Mode 16 (*ZVS Realization*, $t_{15} < t < t_0'$): At time t_{15}, the C_{oss} of S_{1a} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{1a} is turned on at this period.

5.2.1.3. Operation principle in FBM

The gate signals and key waveforms of the 2SFCVD in FBM are shown in Fig. 5- 16. In this operation mode, the same gate signals with 50 % duty cycle are applied to all top or bottom devices. Flying-capacitor C_f is bypassed. The FCVD switches between 00 and 11 operation states. The

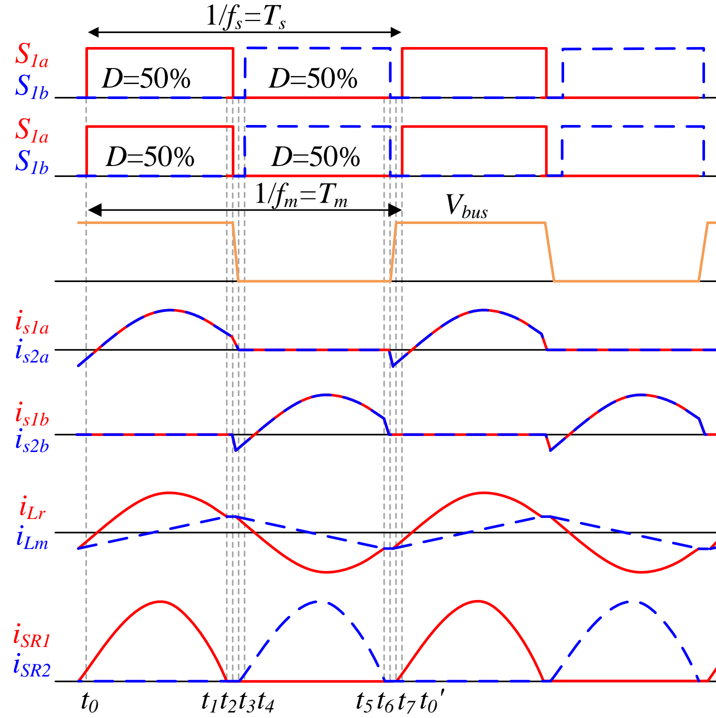


Fig. 5- 16. Gate signals and key waveforms of FBM.

magnetizing component frequency equals to the switching frequency $f_m=f_s$.

Fig. 5- 17 depicts the converter operation states in full-bus operation. The operation where the switching frequency is higher than resonant frequency is not discussed in this chapter. The 2SFCVD-LLC converter operating in FBM has 8 operation states in one switching period T_s, and they are described as follows:

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, top switches S_{1a} and S_{2a} are turned on. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o; thus, i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm},

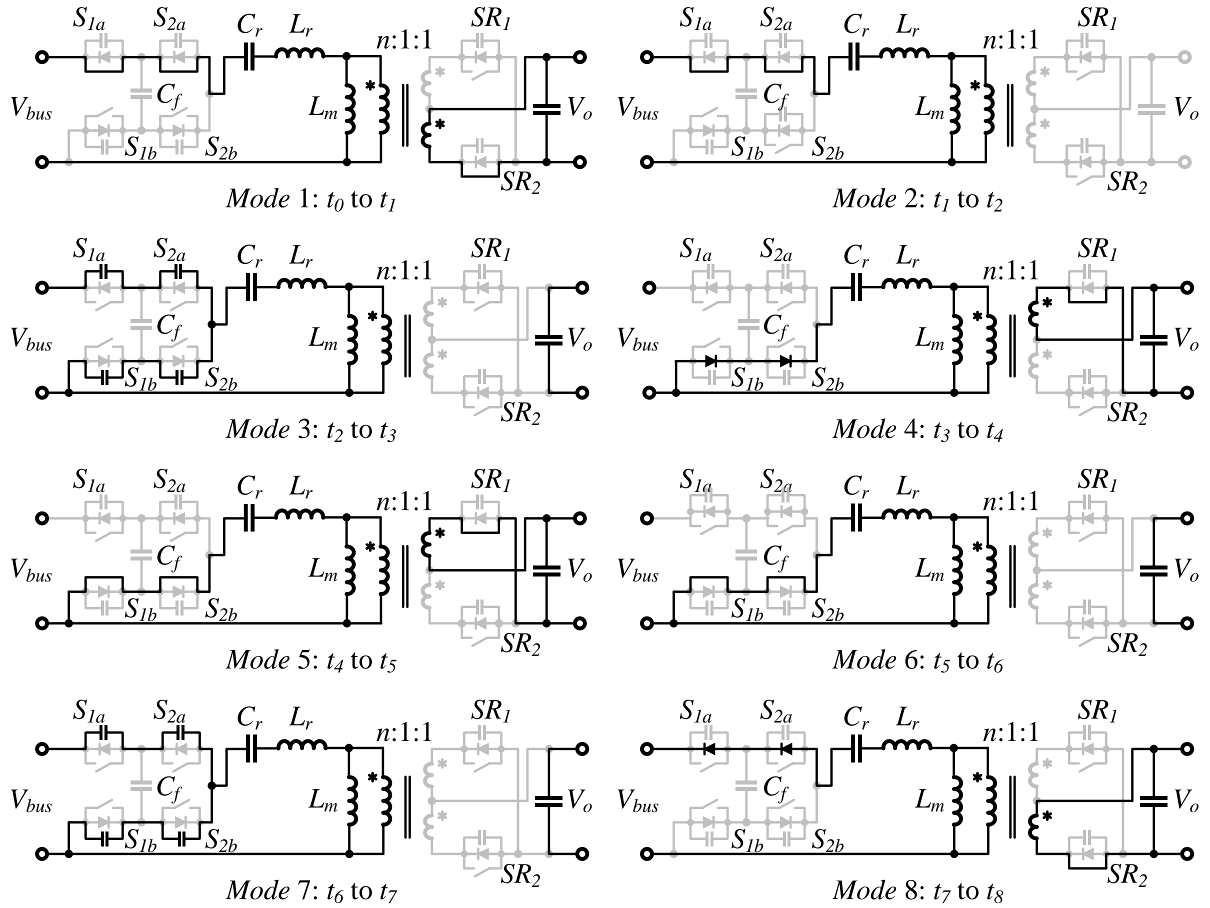


Fig. 5- 17. 2S-FCVD LLC operation states in FBM.

SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_1 and t_2.

3) Mode 3 (Dead Time, t2 < t < t3): At time t_2, S_{1a} and S_{2a} are turned off. The magnetizing inductance current iLm that equals to resonant tank current i_{Lr}, charges and discharges output capacitor Coss of S_{1a}, S_{2a}, S_{1b} and S_{2b}. This mode ends when the C_{oss} of all semiconductor devices are fully discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of S_{1b} and S_{2b} are fully discharged, and their body diodes start to conduct. ZVS can be achieved when S_{1b} and S_{2b} are turned on at this period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, S_{1b} and S_{2b} are turned on and conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant, and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$; thus, i_{Lm} linearly decreases.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, S_{1b} and S_{2b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{2a} and S_{2b}. This mode ends when the C_{oss} of all semiconductor devices are fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of S_{1a} and S_{2a} are fully discharged, and their body diodes start to conduct. ZVS can be achieved when S_{1a} and S_{2a} are turned on at this period.

5.2.2 **4SFCVD-LLC resonant converter analysis**

The equivalent circuit of a 2SFCVD-LLC resonant converter is shown in Fig. 5- 18. The operation states of a 2SFCVD switching bridge are shown in Fig. 5- 19. The 4SFCVD can output five voltage levels of 0 V, $V_{bus}/4$, $V_{bus}/2$, $3V_{bus}/4$, and V_{bus}, respectively. In steady-state operation, the flying capacitor C_{f1}, C_{f2}, and C_{f3} naturally balance voltage by $3V_{bus}/4$. $V_{bus}/2$, and $V_{bus}/4$, respectively. As a result, the voltage stress across each semiconductor device is $V_{bus}/4$. The gate signals for the top and bottom device of each switch cell are complementary. The corresponding

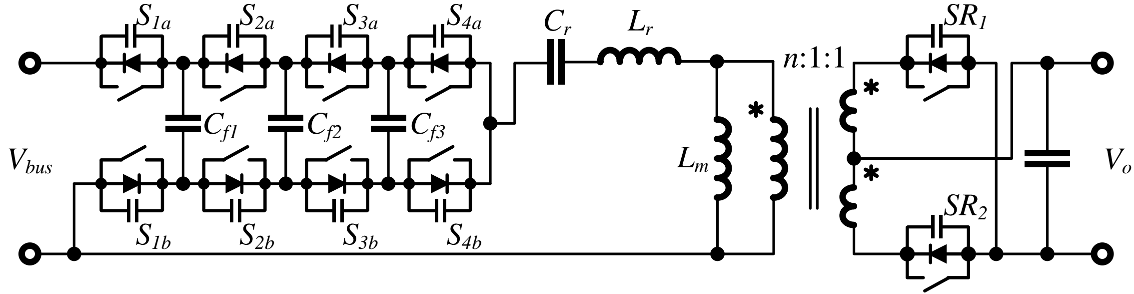


Fig. 5- 18. Equivalent circuit of proposed 4SFCVD-LLC converter.

Fig. 5- 19. 4SFCVD switching bridge operation states that output (a) 0 V, (b) V_{bus} /4, (c) V_{bus}/2, (d) 3V_{bus} /4, and (e) V_{bus}.

gate signals of the top devices are also provided in Fig. 5- 19, where “1” represents ON and “0”

represents OFF. Shown in Fig. 5- 19 (a), all bottom devices are turned on, and the switch bridge output V_{sw} is tied to the ground and outputs 0 V. If only one top device is turned on as illustrated in Fig. 5- 19 (b), the FCVD outputs $V_{bus}/4$. When two of the four top devices are turned on as illustrated in Fig. 5- 19 (c), the FCVD outputs $V_{bus}/2$. Shown in Fig. 5- 19 (d) where three of the four top devices are turned on, the FCVD outputs $3V_{bus}/4$. When all the top devices are turned on, which is depicted in Fig. 5- 12 (c), V_{sw} is connected to V_{bus}. There are four operation modes in 4SFCVD-LLC: ¼-bus mode, HBM, ¾-bus mode, and FBM, which will be demonstrated in detail as follows.

5.2.1.4. Operation principle in ¼-bus mode

In ¼-bus mode, the FCVD switches between 0000, 0001, 0010, 0100, and 1000 operation states. The switching sequence is 0000 → 1000 → 0000 → 0100 → 0000 → 0010 → 0000 → 0001, and then back to 0000. The gate signals and key waveforms are illustrated in Fig. 5- 20. As seen, in one complete switching cycle, FCVD outputs 0 V and $V_{bus}/4$ four times, so the magnetic component frequency f_m=4f_s. Considering the reduced drain-source voltage, the switching loss of the 4SFCVD is only 1/16 of the conventional HB switching bridge at the same magnetizing component frequency. In the 4SFCVD in ¼-bus mode, the duty cycle of each top device is 12.5 %. Therefore, the current stress on the top devices is smaller than the bottom devices.

Fig. 5- 21 depicts the converter operation states in ¼-bus mode. Since the proposed LLC resonant converter in this chapter will lose regulation when its voltage gain is lower than one due to its small Q value, the operation where the switching frequency is higher than resonant frequency is not discussed in this chapter. The 4SFCVD-LLC converter operating in ¼-bus mode has 32 operation states in one switching period T_s, and they are described as follows:

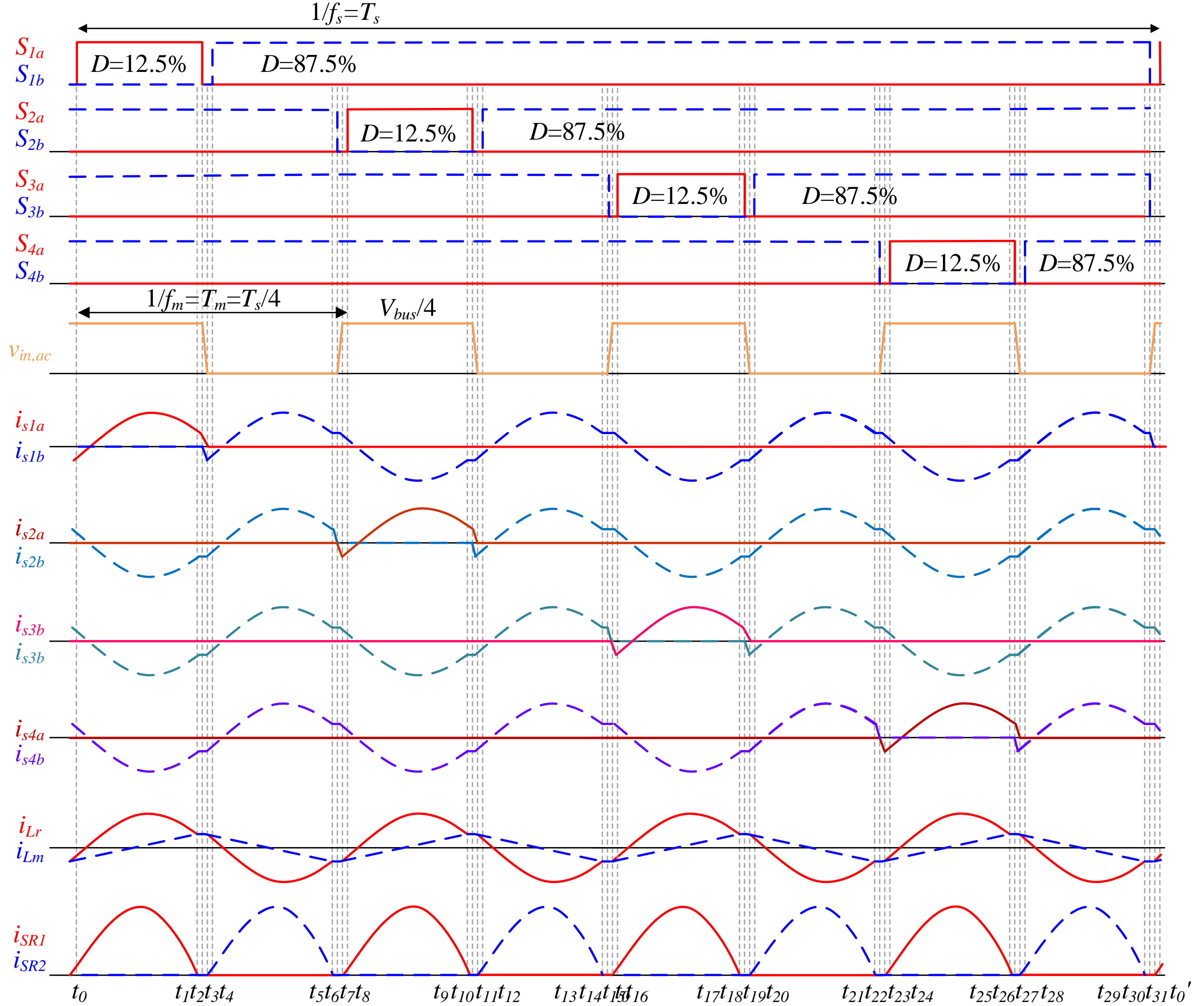


Fig. 5- 20. Gate signals and key waveforms of ¼ mode.

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, switch S_{1a}, S_{2b}, S_{3b}, S_{4b} and flying capacitor C_{f1} are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o, and thus i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r

between t_1 and t_2.

3) Mode 3 (*Dead Time*, $t_2 < t < t_3$): At time t_2, S_{1a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a} and S_{1b}. This mode ends when the C_{oss} of S_{1a} and S_{1b} is fully charged and discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of S_{1b} is fully discharged and its body diode starts to conduct. ZVS can be achieved when S_{1b} is turned on at this period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, S_{1b} is turned on and all bottom devices are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$, and thus i_{Lm} linearly decreases.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally, and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, S_{2b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{2b} and S_{2a}. This mode ends when the C_{oss} of S_{2b} and S_{2a} is fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of S_{2a} is fully discharged and its body diode starts to conduct. ZVS can be achieved when S_{2a} is turned on at this period.

9) Mode 9 (*Power Transfer*, $t_8 < t < t_9$): Between time t_8 and t_9, switch S_{2a}, S_{1b}, S_{3b}, S_{4b} and flying capacitor C_{f1} and C_{f2} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

10) Mode 10 (*Energy Circulation*, $t_9 < t < t_{10}$): Between time t_9 and t_{10}, switch S_{2a}, S_{1b}, S_{3b}, S_{4b} and flying capacitor C_{f1} and C_{f2} are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

11) Mode 11 (*Dead Time*, $t_{10} < t < t_{11}$): At time t_{10}, S_{2a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{2a} and S_{2b}. This mode ends when the C_{oss} of S_{2a} and S_{2b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 7*.

12) Mode 12 (*ZVS Realization*, $t_{11} < t < t_{12}$): At time t_{11}, the C_{oss} of S_{2b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{2b} is turned on at this period.

13) Mode 13 (*Power Transfer*, $t_{12} < t < t_{13}$): At time t_{12}, S_{2b} is turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

14) Mode 14 (*Energy Circulation*, $t_{13} < t < t_{14}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

15) Mode 15 (*Dead Time*, $t_{14} < t < t_{15}$): At time t_{14}, S_{3b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{3a} and S_{3b}. This mode ends when the C_{oss} of S_{3a} and S_{3b} is fully charged and discharged.

16) Mode 16 (*ZVS Realization*, $t_{15} < t < t_{16}$): At time t_{15}, the C_{oss} of S_{3a} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{3a} is turned on at this period.

17) Mode 17 (*Power Transfer*, $t_{16} < t < t_{17}$): Between time t_{16} and t_{17}, switch S_{3a}, S_{1b}, S_{2b}, S_{4b} and flying capacitor C_{f2} and C_{f3} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

18) Mode 18 (*Energy Circulation*, $t_{17} < t < t_{18}$): Between time t_{17} and t_{18}, switch S_{3a}, S_{1b}, S_{2b},

S_{4b} and flying capacitor C_{f2} and C_{f3} are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

19) Mode 19 (*Dead Time*, $t_{18} < t < t_{19}$): At time t_{18}, S_{3a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{3a} and S_{3b}. This mode ends when the C_{oss} of S_{3a} and S_{3b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 15*.

20) Mode 20 (*ZVS Realization*, $t_{19} < t < t_{20}$): At time t_{19}, the C_{oss} of S_{3b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{3b} is turned on at this period.

21) Mode 21 (*Power Transfer*, $t_{20} < t < t_{21}$): At time t_{20}, S_{3b} is turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

22) Mode 22 (*Energy Circulation*, $t_{21} < t < t_{22}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

23) Mode 23 (*Dead Time*, $t_{22} < t < t_{23}$): At time t_{22}, S_{4b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{4b} and S_{4a}. This mode ends when the C_{oss} of S_{4b} and S_{4a} are fully charged and discharged.

24) Mode 24 (*ZVS Realization*, $t_{23} < t < t_{24}$): At time t_{23}, the C_{oss} of S_{4a} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{4a} is turned on at this period.

25) Mode 25 (*Power Transfer*, $t_{24} < t < t_{25}$): Between time t_{24} and t_{25}, switch S_{4a}, S_{1b}, S_{2b}, S_{3b} and flying capacitor C_{f3} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

26) Mode 26 (*Energy Circulation*, $t_{25} < t < t_{26}$): Between time t_{25} and t_{26}, switch S_{4a}, S_{1b}, S_{2b}, S_{3b} and flying capacitor C_{f3} are conducting. The operation of the resonant tank, transformer and

SR is the same as *Mode* 2.

27) Mode 27 (*Dead Time*, $t_{26} < t < t_{27}$): At time t_{22}, S_{4a} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{4a} and S_{4b}. This mode ends when the C_{oss} of S_{4a} and S_{4b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 23*.

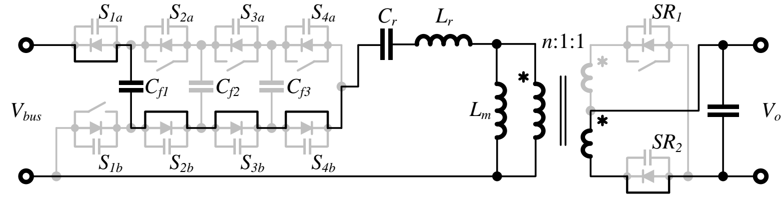
28) Mode 28 (*ZVS Realization*, $t_{27} < t < t_{28}$): At time t_{27}, the C_{oss} of S_{4b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{4b} is turned on at this period.

29) Mode 29 (*Power Transfer*, $t_{28} < t < t_{29}$): At time t_{28}, S_{4b} is turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

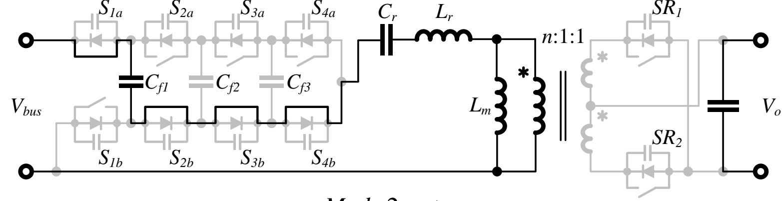
30) Mode 30 (*Energy Circulation*, $t_{29} < t < t_{30}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

31) Mode 31 (*Dead Time*, $t_{30} < t < t_{31}$): At time t_{30}, S_{1b} is turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1b} and S_{1a}. This mode ends when the C_{oss} of S_{1b} and S_{1a} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 3*

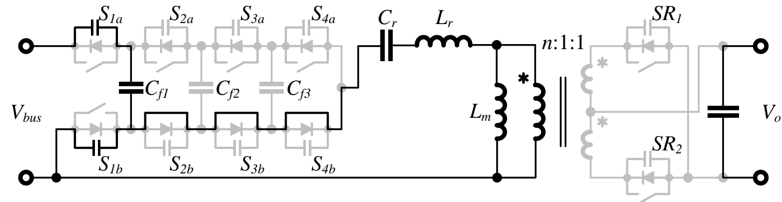
32) Mode 32 (*ZVS Realization*, $t_{31} < t < t_0'$): At time t_{31}, the C_{oss} of S_{1a} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{1a} is turned on at this period.



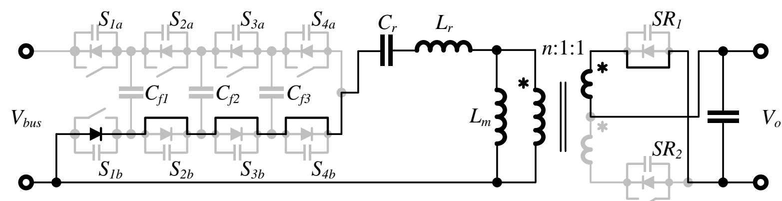
Mode 1: t_0 to t_1



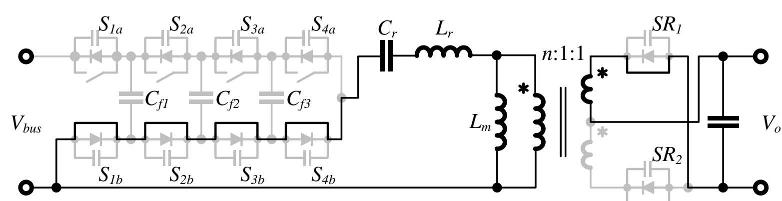
Mode 2: t_1 to t_2



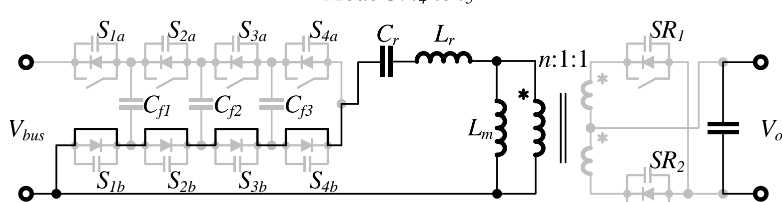
Mode 3: t_2 to t_3



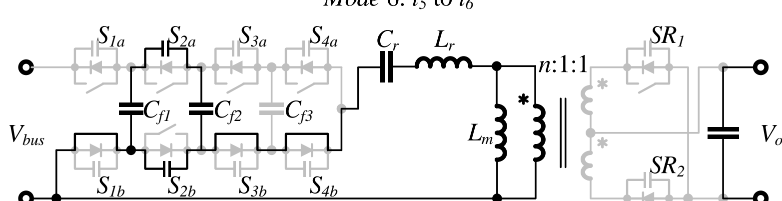
Mode 4: t_3 to t_4



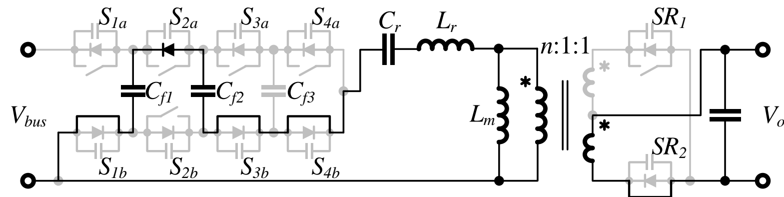
Mode 5: t_4 to t_5



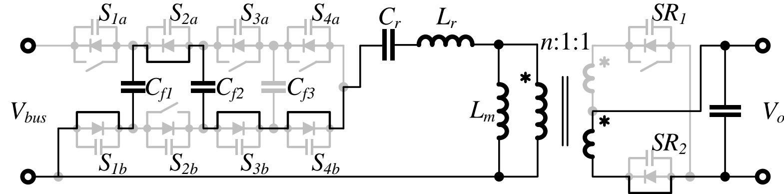
Mode 6: t_5 to t_6



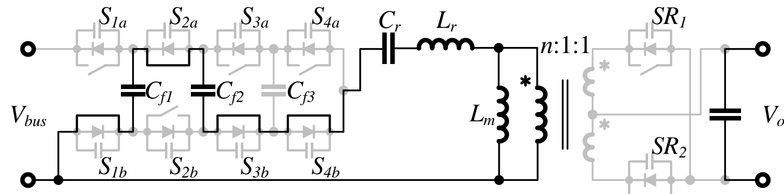
Mode 7: t_6 to t_7



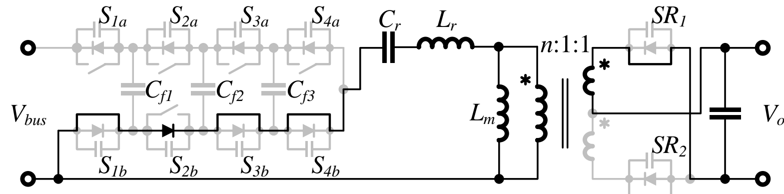
Mode 8: t_7 to t_8



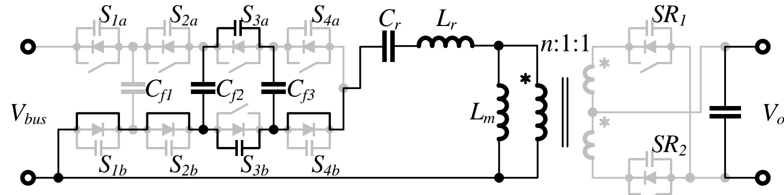
Mode 9: t_8 to t_9



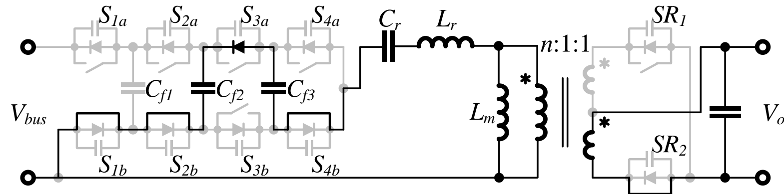
Mode 10: t_9 to t_{10}



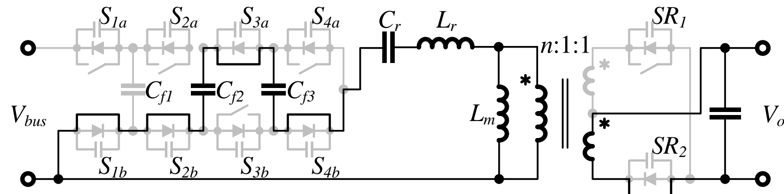
Mode 12: t_{11} to t_{12}



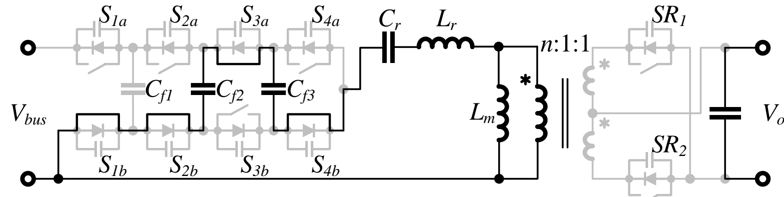
Mode 15: t_{15} to t_{16}



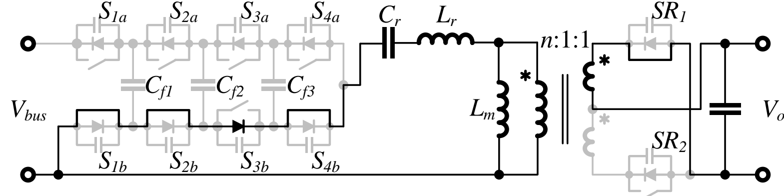
Mode 16: t_{16} to t_{17}



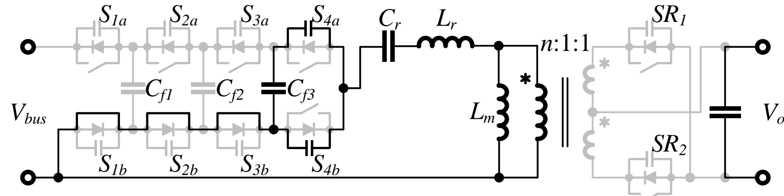
Mode 17: t_{17} to t_{18}



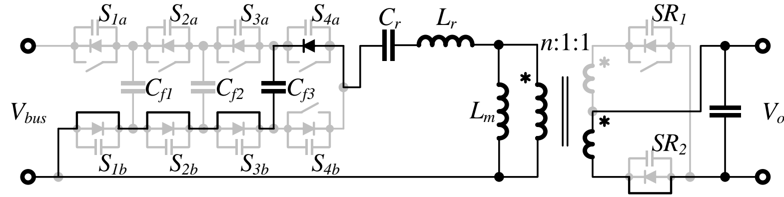
Mode 18: t_{18} to t_{19}



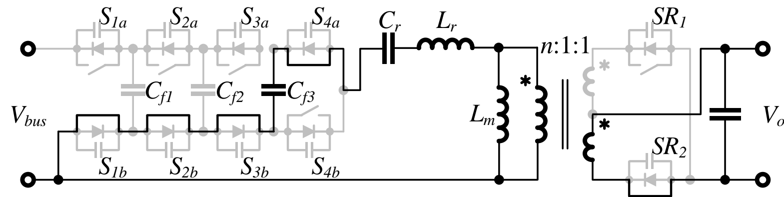
Mode 20: t_{20} to t_{21}



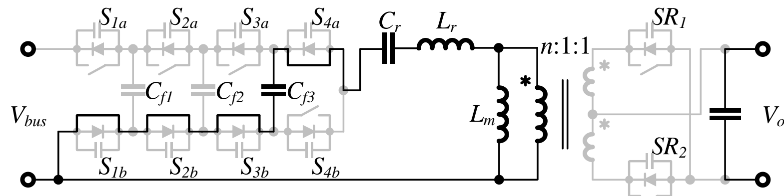
Mode 23: t_{23} to t_{24}



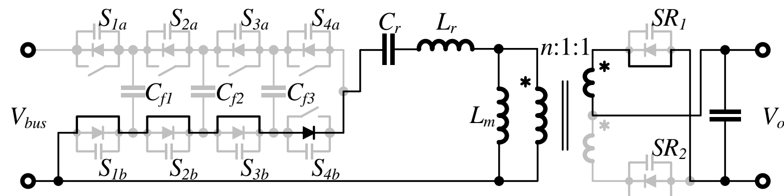
Mode 24: t_{24} to t_{25}



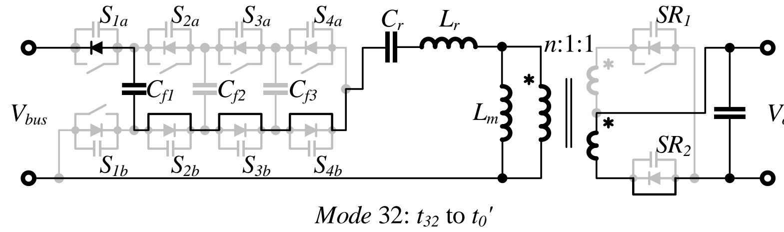
Mode 25: t_{25} to t_{26}



Mode 26: t_{26} to t_{27}



Mode 28: t_{28} to t_{29}



Mode 32: t_{32} to t_0'

Fig. 5- 21. 4SFCVD-LLC operation states in ¼ mode.

5.2.1.5. Operation principle in HBM

In HBM, the FCVD switches between 0000, 1100, and 0011 operation states. The flying capacitors C_{f1} and C_{f3} are bypassed. The switching sequence is 0000 → 1100 → 0000 → 0011, and then back to 0000. The gate signals and key waveforms are illustrated in Fig. 5- 22. As seen, in one complete switching cycle, FCVD outputs 0 V and $V_{bus}/2$ twice, so the magnetic component frequency $f_m=2f_s$. Considering the reduced drain-source voltage, the switching loss of the 4SFCVD

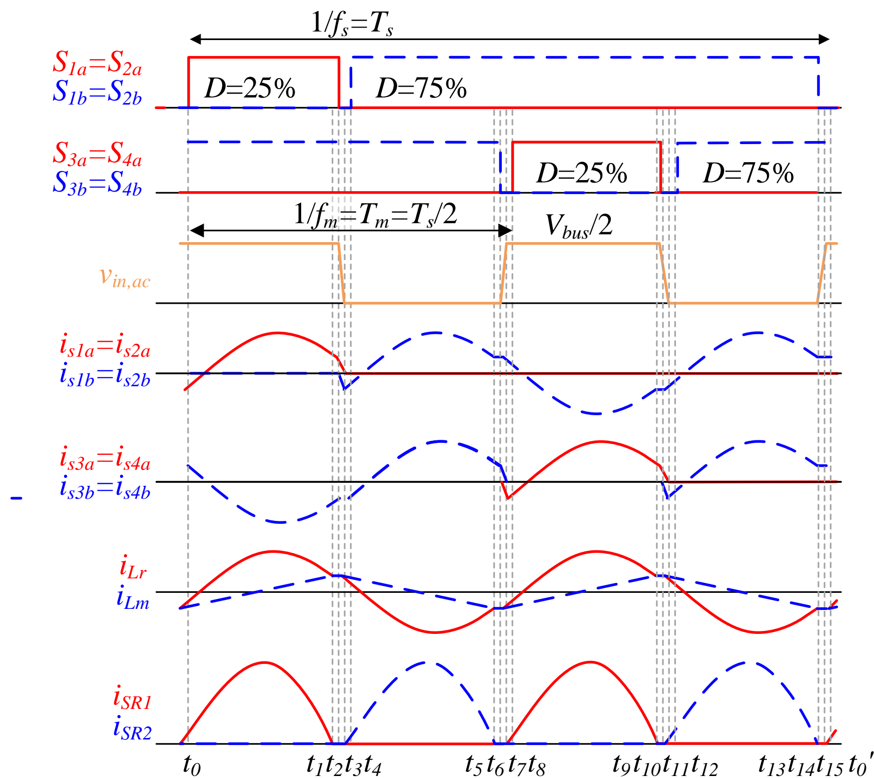


Fig. 5- 22. Gate signals and key waveforms of HBM.

is only 1/8 of the conventional HB switching bridge at the same magnetizing component frequency. In the 4SFCVD in HBM, the duty cycle of each top device is 25 %. Therefore, the current stress on the top devices is smaller than the bottom devices.

Fig. 5- 23 depicts the converter operation states in ¼-bus mode. Since the proposed LLC resonant converter in this chapter will lose regulation when its voltage gain is lower than one due to its small Q value, the operation where the switching frequency is higher than resonant frequency is not discussed in this chapter. The 4SFCVD-LLC converter operating in HBM has 16 operation states in one switching period T_s, and they are described as follows:

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, switch S_{1a}, S_{2a}, S_{3b}, S_{4b} and flying capacitor C_{f2} are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o, and thus i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_1 and t_2.

3) Mode 3 (*Dead Time*, $t_2 < t < t_3$): At time t_2, S_{1a} and S_{2a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a}, S_{2a}, S_{1b} and S_{2b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{1b} and S_{2b} is fully charged and discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of S_{1b} and S_{2b} is fully discharged and their body diode starts to conduct. ZVS can be achieved when S_{1b} and S_{2b} are turned on at this

period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, S_{1b} and S_{2b} are turned on and all the bottom devices are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$, and thus i_{Lm} linearly decreases.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally, and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, S_{3b} and S_{4b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{3a}, S_{4a}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of S_{3a}, S_{4a}, S_{3b} and S_{4b} is fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of S_{3a} and S_{4a} is fully discharged and their body diodes start to conduct. ZVS can be achieved when S_{3a} and S_{4a} are turned on at this period.

9) Mode 9 (*Power Transfer*, $t_8 < t < t_9$): Between time t_8 and t_9, switch S_{3a}, S_{4a}, S_{1b} and S_{2b} and flying capacitor C_{f2} are conducting. The operation of resonant tank, transformer and SRs is the same as *Mode* 1.

10) Mode 10 (*Energy Circulation*, $t_9 < t < t_{10}$): Between time t_9 and t_{10}, switch S_{3a}, S_{4a}, S_{1b} and S_{2b} and flying capacitor C_{f2} are conducting. The operation of the resonant tank, transformer and SRs is the same as *Mode* 2.

11) Mode 11 (*Dead Time*, $t_{10} < t < t_{11}$): At time t_{10}, S_{3a} and S_{4a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{3a}, S_{4a}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of S_{3a}, S_{4a}, S_{3b} and S_{4b} is fully charged and discharged.

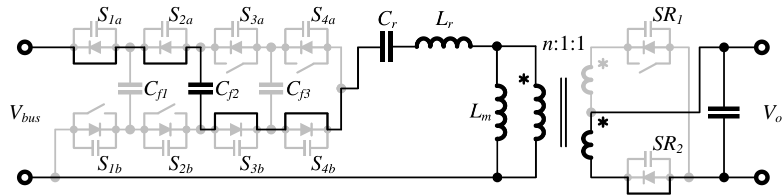
12) Mode 12 (*ZVS Realization*, $t_{11} < t < t_{12}$): At time t_{11}, the C_{oss} of S_{3b} and S_{4b} is fully discharged, and their body diode starts to conduct. ZVS can be achieved when S_{3b} and S_{4b} are turned on at this period.

13) Mode 13 (*Power Transfer*, $t_{12} < t < t_{13}$): At time t_{12}, S_{3b} and S_{4b} are turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

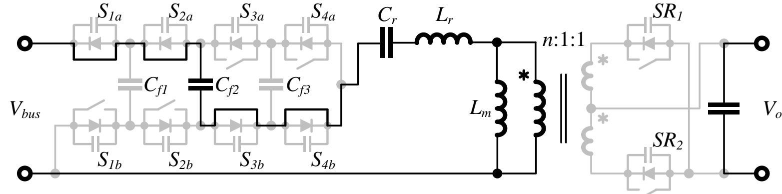
14) Mode 14 (*Energy Circulation*, $t_{13} < t < t_{14}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

15) Mode 15 (*Dead Time*, $t_{14} < t < t_{15}$): At time t_{14}, S_{1b} and S_{2b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{1a}, S_{2a}, S_{1b} and S_{2b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{1b} and S_{2b} is fully charged and discharged.

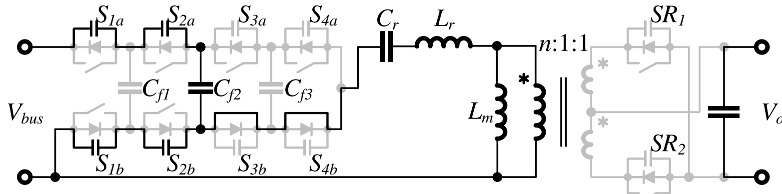
16) Mode 16 (*ZVS Realization*, $t_{15} < t < t_0'$): At time t_{15}, the C_{oss} of S_{1a} and S_{2a} is fully discharged, and their body diode starts to conduct. ZVS can be achieved when S_{1a} and S_{2a} are turned on at this period.



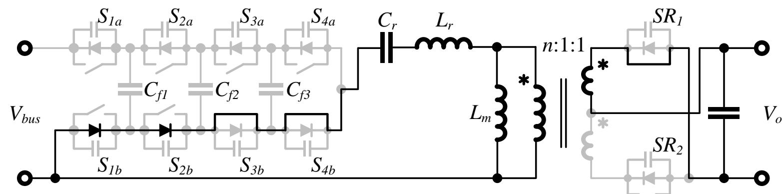
Mode 1: t_0 to t_1



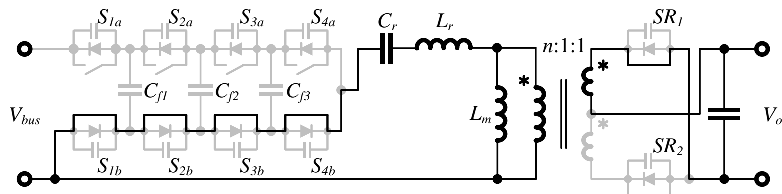
Mode 2: t_1 to t_2



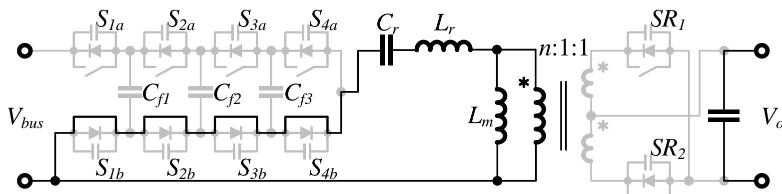
Mode 3: t_2 to t_3



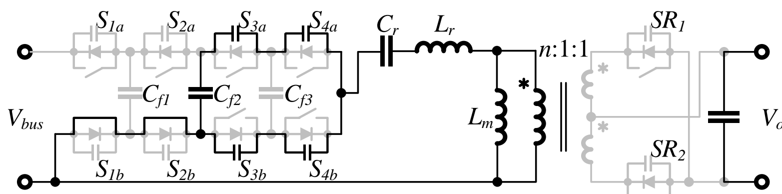
Mode 4: t_3 to t_4



Mode 5: t_4 to t_5



Mode 6: t_5 to t_6



Mode 7: t_7 to t_8

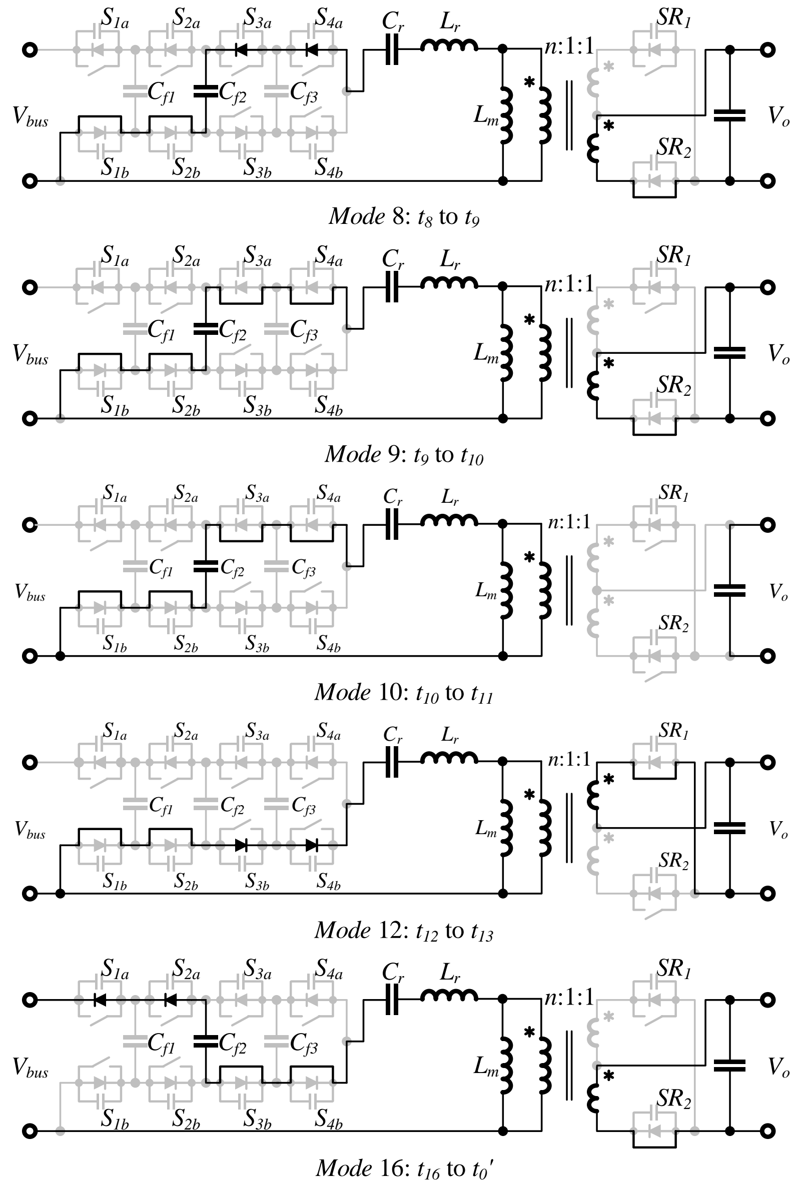


Fig. 5- 23. 4SFCVD-LLC operation states in HBM.

5.2.1.6. Operation principle in ¾-bus mode

In ¾-bus mode, the FCVD switches between 0000, 1110, 1101, 1011, and 0111 operation states. The flying capacitors C_{f1} and C_{f3} are bypassed. The switching sequence is 0000 → 1110 → 0000 → 1101 → 0000 → 1011 → 0000 → 0111, and then back to 0000.. The gate signals and key waveforms are illustrated in Fig. 5- 24. As seen, in one complete switching cycle T_s as labelled in

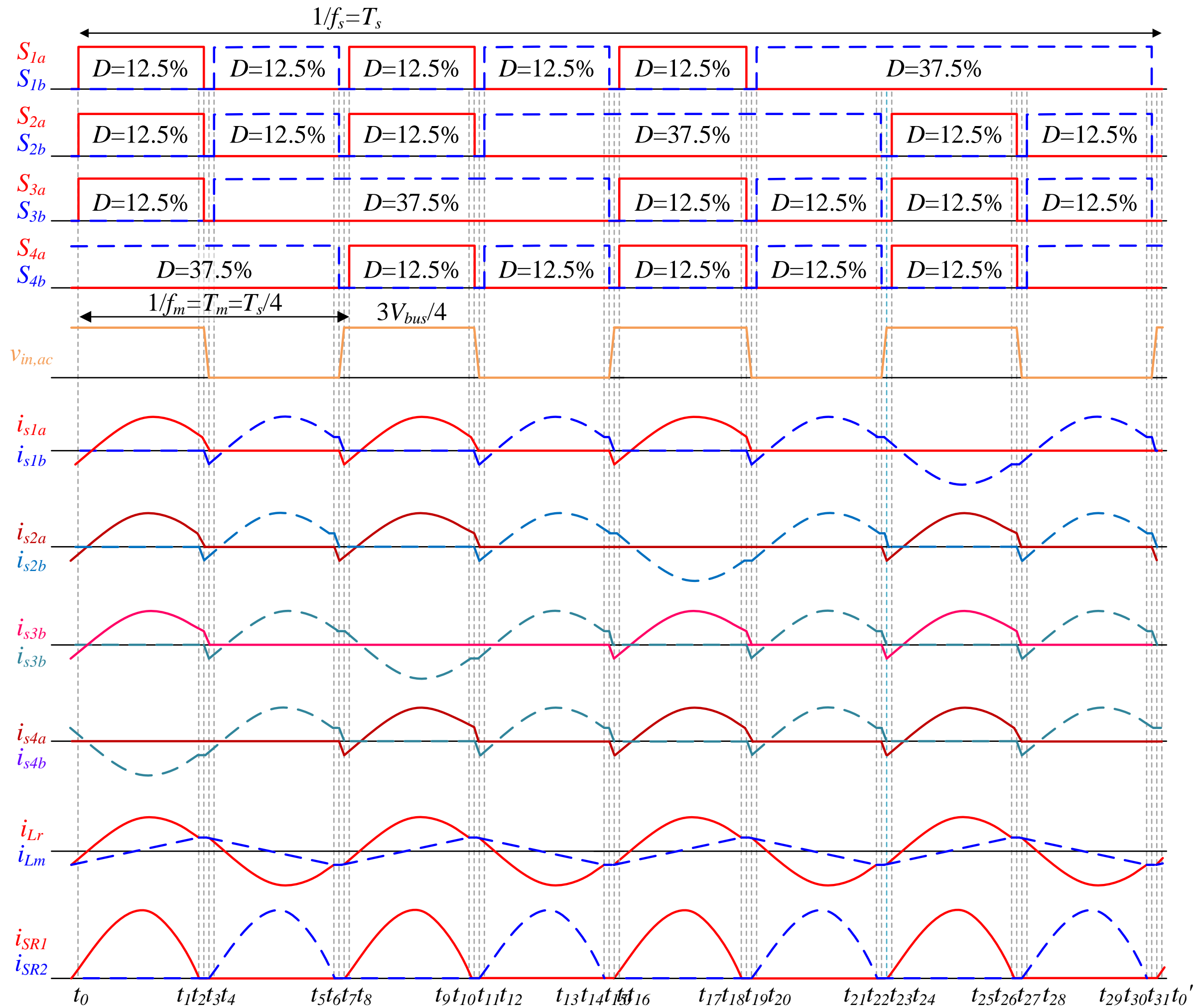


Fig. 5- 24. Gate signals and key waveforms of ¾ mode.

Fig. 5- 24, FCVD outputs 0 V and $3V_{bus}/4$ four times, so the magnetic component frequency $f_m=4f_s$. In one switching period, each power semiconductor device switches three times, so the switching loss of the 4SFCVD is 3/16 of the conventional HB switching bridge at the same magnetizing component frequency. In the ¾-bus mode, the current stress on the top devices is also smaller than the bottom devices.

Fig. 5- 25 depicts the converter operation states in ¾-bus mode. Since the proposed LLC resonant converter in this chapter will lose regulation when its voltage gain is lower than one due to its small Q value, the operation where the switching frequency is higher than resonant frequency

is not discussed in this chapter. The 4SFCVD-LLC converter operating in ¾-bus mode has 32 operation states in one switching period T_s, and they are described as follows:

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, switch S_{1a}, S_{2a}, S_{3a}, S_{4b} and flying capacitor C_{f3} are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o, and thus i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_1 and t_2.

3) Mode 3 (*Dead Time*, $t_2 < t < t_3$): At time t_2, S_{1a}, S_{2a} and S_{3a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a}, S_{2a}, S_{3a}, S_{1b}, S_{2b} and S_{3b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{3a}, S_{1b}, S_{2b} and S_{3b} is fully charged and discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of S_{1b}, S_{2b} and S_{3b} is fully discharged and their body diode starts to conduct. ZVS can be achieved when S_{1b}, S_{2b} and S_{3b} are turned on at this period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, S_{1b}, S_{2b} and S_{3b} are turned on and all bottom devices are conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, the SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$, and thus i_{Lm} linearly decreases.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally, and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, S_{1b}, S_{2b} and S_{4b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a}, S_{2a}, S_{4a}, S_{1b}, S_{2b} and S_{4b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{4a}, S_{1b}, S_{2b} and S_{4b} is fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of S_{1a}, S_{2a} and S_{4a} is fully discharged and its body diode starts to conduct. ZVS can be achieved when S_{1a}, S_{2a} and S_{4a} are turned on at this period.

9) Mode 9 (*Power Transfer*, $t_8 < t < t_9$): Between time t_8 and t_9, switch S_{1a}, S_{2a}, S_{4a}, S_{3b} and flying capacitor C_{f2} and C_{f3} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

10) Mode 10 (*Energy Circulation*, $t_9 < t < t_{10}$): Between time t_9 and t_{10}, switch S_{1a}, S_{2a}, S_{4a}, S_{3b} and flying capacitor C_{f2} and C_{f3} are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

11) Mode 11 (*Dead Time*, $t_{10} < t < t_{11}$): At time t_{10}, S_{1a}, S_{2a} and S_{4a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1a}, S_{2a}, S_{4a}, S_{1b}, S_{2b} and S_{4b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{4a}, S_{1b}, S_{2b} and S_{4b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 7*.

12) Mode 12 (*ZVS Realization*, $t_{11} < t < t_{12}$): At time t_{11}, the C_{oss} of S_{1b}, S_{2b} and S_{4b} is fully

discharged, and its body diode starts to conduct. ZVS can be achieved when S_{1b}, S_{2b} and S_{4b} are turned on at this period.

13) Mode 13 (*Power Transfer*, $t_{12} < t < t_{13}$): At time t_{12}, S_{1b}, S_{2b} and S_{4b} are turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

14) Mode 14 (*Energy Circulation*, $t_{13} < t < t_{14}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

15) Mode 15 (*Dead Time*, $t_{14} < t < t_{15}$): At time t_{14}, S_{1b}, S_{3b} and S_{4b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{1a}, S_{3a}, S_{4a}, S_{1b}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of of S_{1a}, S_{3a}, S_{4a}, S_{1b}, S_{3b} and S_{4b} is fully charged and discharged.

16) Mode 16 (*ZVS Realization*, $t_{15} < t < t_{16}$): At time t_{15}, the C_{oss} of S_{1a}, S_{3a} and S_{4a} are fully discharged, and their body diode starts to conduct. ZVS can be achieved when S_{1a}, S_{3a} and S_{4a} are turned on at this period.

17) Mode 17 (*Power Transfer*, $t_{16} < t < t_{17}$): Between time t_{16} and t_{17}, switch S_{1a}, S_{3a}, S_{4a}, S_{2b} and flying capacitor C_{f1} and C_{f2} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

18) Mode 18 (*Energy Circulation*, $t_{17} < t < t_{18}$): Between time t_{17} and t_{18}, switch S_{1a}, S_{3a}, S_{4a}, S_{2b} and flying capacitor C_{f1} and C_{f2} are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

19) Mode 19 (*Dead Time*, $t_{18} < t < t_{19}$): At time t_{18}, S_{1a}, S_{3a} and S_{4a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{1a}, S_{3a}, S_{4a}, S_{1b}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of S_{1a}, S_{3a}, S_{4a}, S_{1b}, S_{3b} and S_{4b} is fully charged and discharged. The equivalent circuit of this mode is the same as

Mode 15.

20) Mode 20 (*ZVS Realization*, $t_{19} < t < t_{20}$): At time t_{19}, the C_{oss} of S_{1b}, S_{3b} and S_{4b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{1b}, S_{3b} and S_{4b} are turned on at this period.

21) Mode 21 (*Power Transfer*, $t_{20} < t < t_{21}$): At time t_{20}, S_{1b}, S_{3b} and S_{4b} is turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

22) Mode 22 (*Energy Circulation*, $t_{21} < t < t_{22}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

23) Mode 23 (*Dead Time*, $t_{22} < t < t_{23}$): At time t_{22}, S_{2b}, S_{3b} and S_{4b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of S_{2a}, S_{3a}, S_{4a}, S_{2b}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of S_{2a}, S_{3a}, S_{4a}, S_{2b}, S_{3b} and S_{4b} are fully charged and discharged.

24) Mode 24 (*ZVS Realization*, $t_{23} < t < t_{24}$): At time t_{23}, the C_{oss} of S_{2a}, S_{3a} and S_{4a} is fully discharged, and their body diode starts to conduct. ZVS can be achieved when S_{2a}, S_{3a} and S_{4a} are turned on at this period.

25) Mode 25 (*Power Transfer*, $t_{24} < t < t_{25}$): Between time t_{24} and t_{25}, switch S_{2a}, S_{3a}, S_{4a}, S_{1b} and flying capacitor C_{f1} are conducting. The operation of resonant tank, transformer and synchronous rectifier (SR) is the same as *Mode* 1.

26) Mode 26 (*Energy Circulation*, $t_{25} < t < t_{26}$): Between time t_{25} and t_{26}, switch S_{2a}, S_{3a}, S_{4a}, S_{1b} and flying capacitor C_{f1} are conducting. The operation of the resonant tank, transformer and SR is the same as *Mode* 2.

27) Mode 27 (*Dead Time*, $t_{26} < t < t_{27}$): At time t_{22}, S_{2a}, S_{3a} and S_{4a} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges

output capacitor C_{oss} of S_{2a}, S_{3a}, S_{4a}, S_{2b}, S_{3b} and S_{4b}. This mode ends when the C_{oss} of S_{2a}, S_{3a}, S_{4a}, S_{2b}, S_{3b} and S_{4b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 23*.

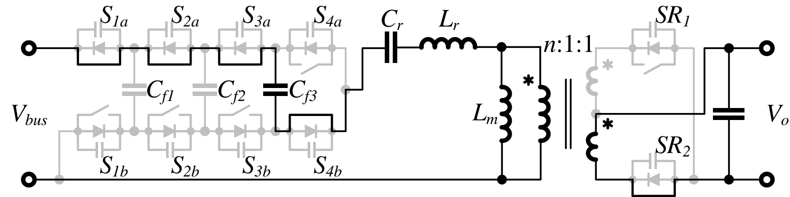
28) Mode 28 (*ZVS Realization*, $t_{27} < t < t_{28}$): At time t_{27}, the C_{oss} of S_{2b}, S_{3b} and S_{4b} is fully discharged, and its body diode starts to conduct. ZVS can be achieved when S_{2b}, S_{3b} and S_{4b} are turned on at this period.

29) Mode 29 (*Power Transfer*, $t_{28} < t < t_{29}$): At time t_{28}, S_{2b}, S_{3b} and S_{4b} are turned on. The operation of the resonant tank, transformer, and SRs is the same as *Mode* 5.

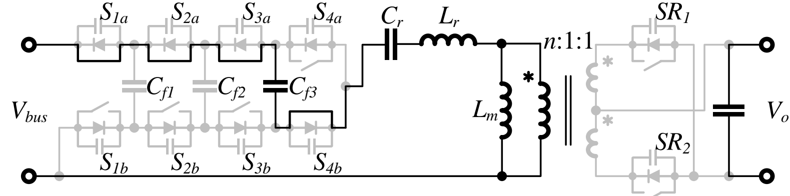
30) Mode 30 (*Energy Circulation*, $t_{29} < t < t_{30}$): The operation of the resonant tank, transformer, and SRs is the same as *Mode* 6.

31) Mode 31 (*Dead Time*, $t_{30} < t < t_{31}$): At time t_{30}, S_{1b}, S_{2b} and S_{3b} are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr} charges and discharges output capacitor C_{oss} of S_{1b} and of S_{1a}, S_{2a}, S_{3a}, S_{1b}, S_{2b} and S_{3b}. This mode ends when the C_{oss} of S_{1a}, S_{2a}, S_{3a}, S_{1b}, S_{2b} and S_{3b} is fully charged and discharged. The equivalent circuit of this mode is the same as *Mode 3*

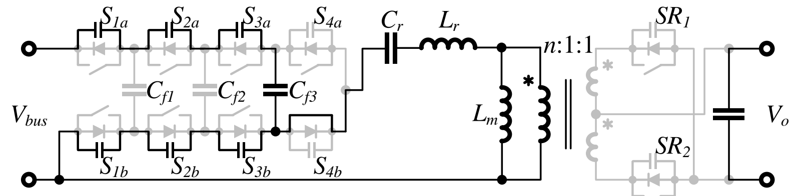
32) Mode 32 (*ZVS Realization*, $t_{31} < t < t_0'$): At time t_{31}, the C_{oss} of S_{1a}, S_{2a} and S_{3a} is fully discharged, and their body diode starts to conduct. ZVS can be achieved when S_{1a}, S_{2a} and S_{3a} are turned on at this period.



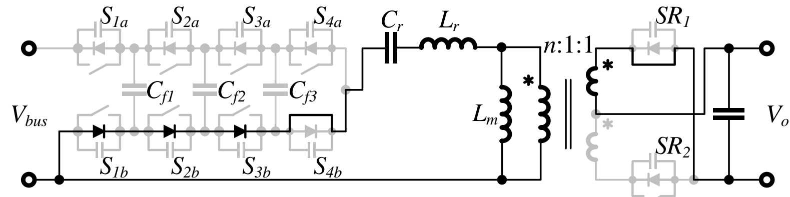
Mode 1: t_0 to t_1



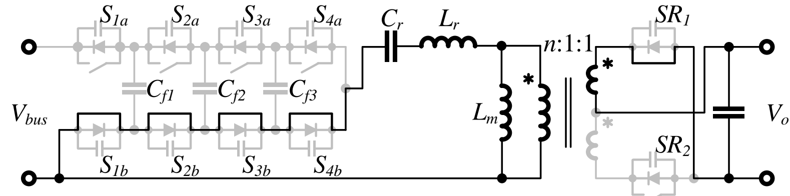
Mode 2: t_1 to t_2



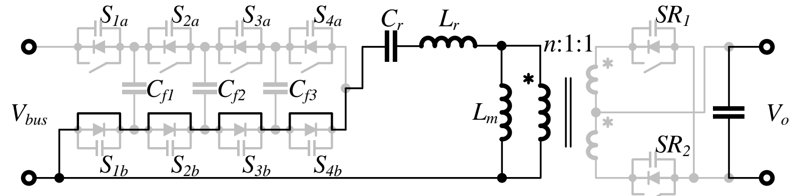
Mode 3: t_2 to t_3



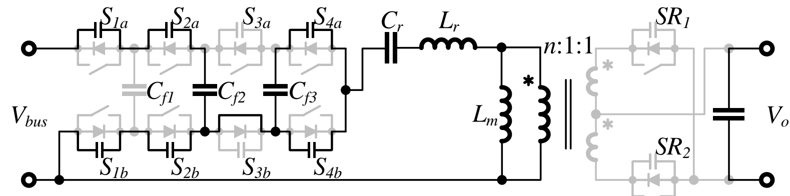
Mode 4: t_3 to t_4



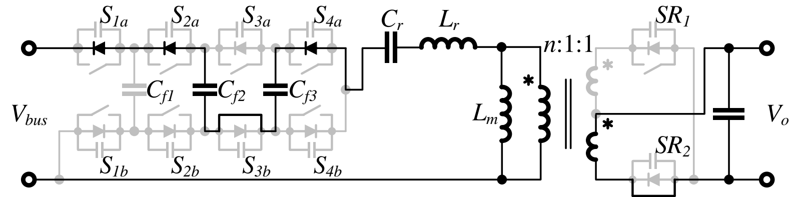
Mode 5: t_4 to t_5



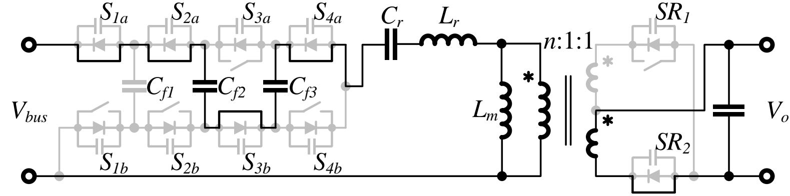
Mode 6: t_5 to t_6



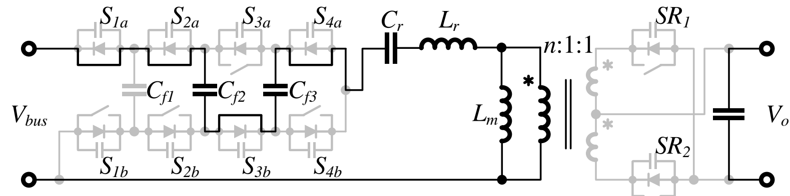
Mode 7: t_6 to t_7



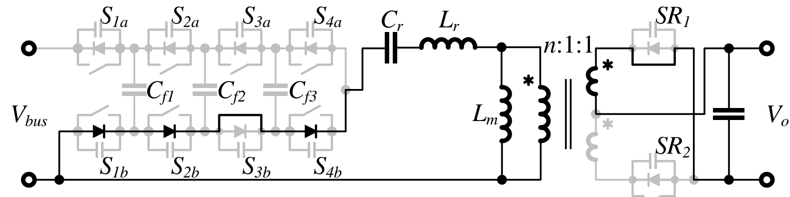
Mode 8: t_7 to t_8



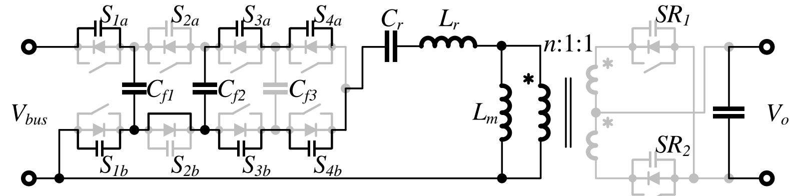
Mode 9: t_8 to t_9



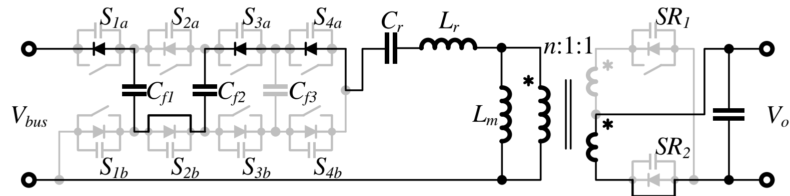
Mode 10: t_5 to t_{10}



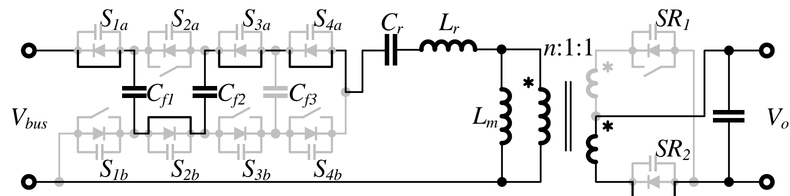
Mode 12: t_{11} to t_{12}



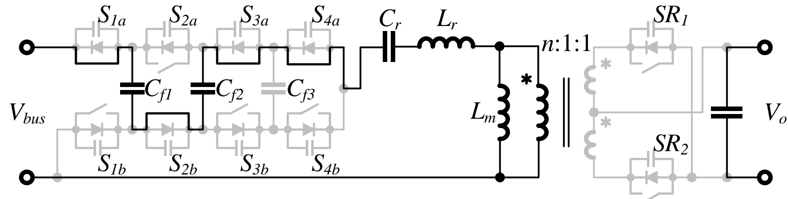
Mode 15: t_{14} to t_{15}



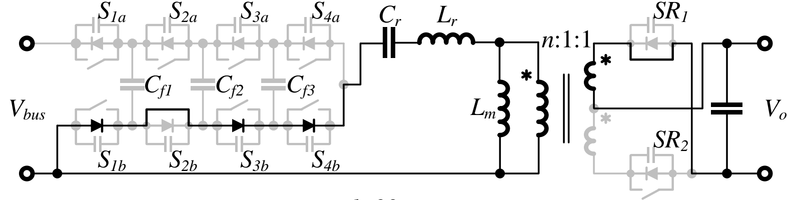
Mode 16: t_{15} to t_{16}



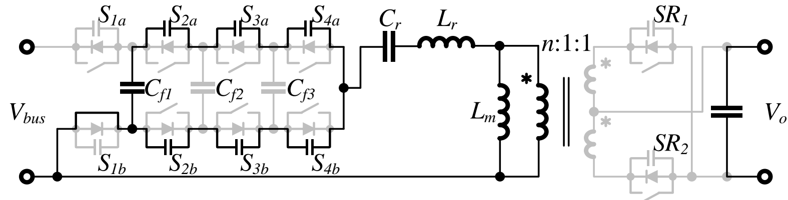
Mode 17: t_{15} to t_{16}



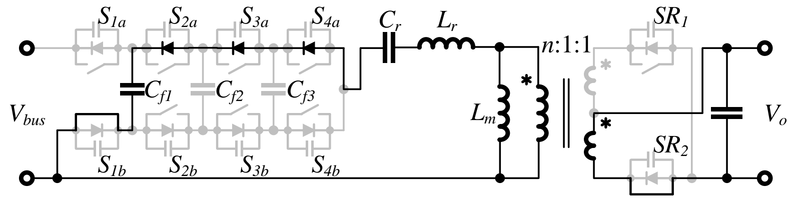
Mode 18: t_{17} to t_{18}



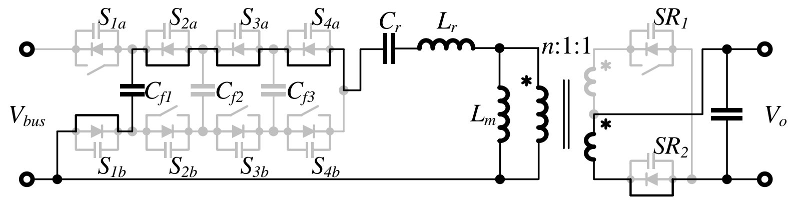
Mode 20: t_{19} to t_{20}



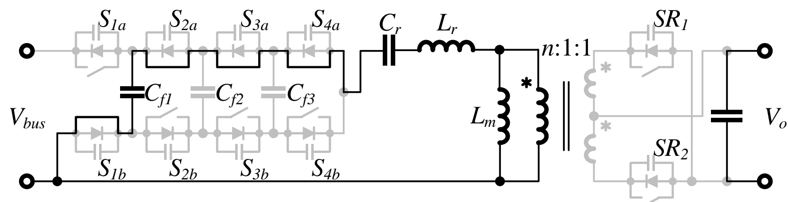
Mode 23: t_{22} to t_{23}



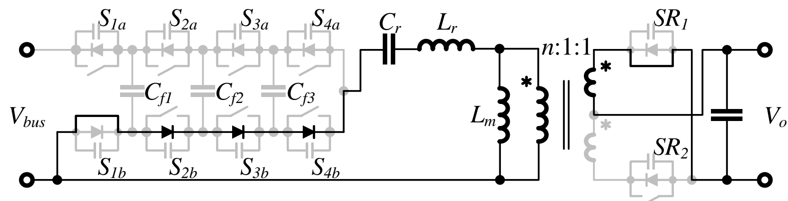
Mode 24: t_{23} to t_{24}



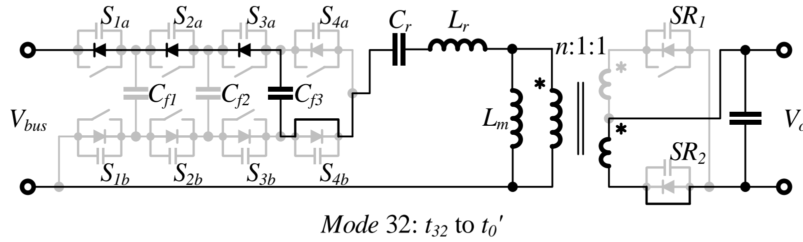
Mode 25: t_{24} to t_{25}



Mode 26: t_{25} to t_{26}



Mode 28: t_{27} to t_{28}



Mode 32: t_{32} to t_0'

Fig. 5- 25. 4SFCVD-LLC operation states in ¾-bus mode.

5.2.1.7. Operation principle in FBM

The gate signals and key waveforms of the 2SFCVD in full-bus operation are shown in Fig. 5- 26. In this operation mode, the same gate signals with 50 % duty cycle are applied to all top or bottom devices. Flying-capacitors are bypassed. The FCVD switches between 0000 and 1111 operation states. The magnetizing component frequency equals to the switching frequency $f_m=f_s$.

Fig. 5- 27 depicts the converter operation states in full-bus operation. The operation where the switching frequency is higher than resonant frequency is not discussed in this chapter. The

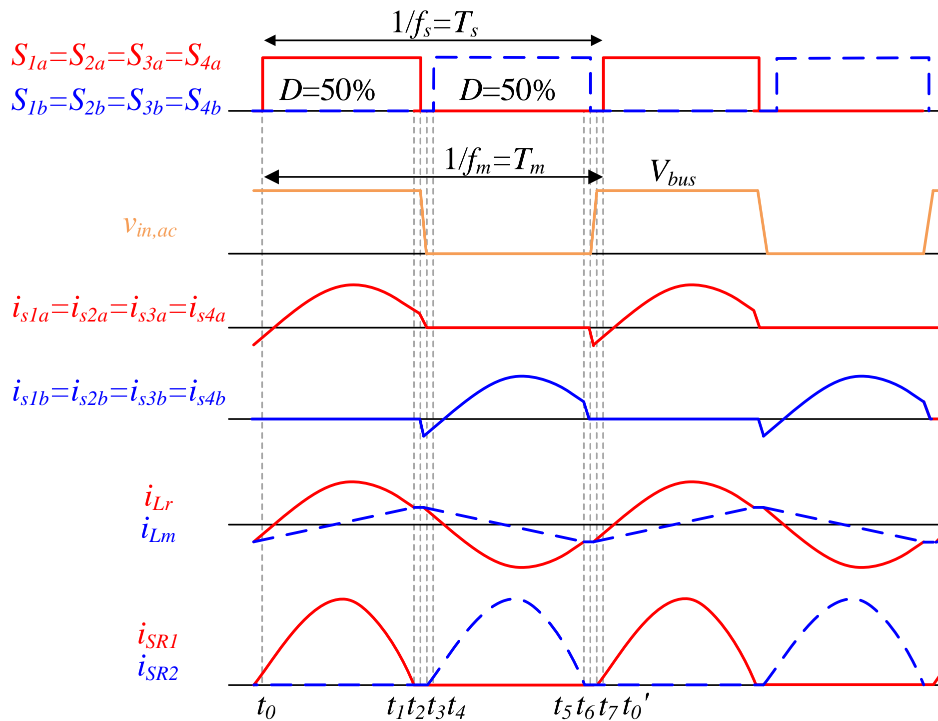


Fig. 5- 26. Gate signals and key waveforms of FBM.

4SFCVD-LLC converter operating in FBM has 8 operation states in one switching period T_s, and they are described as follows:

1) Mode 1 (*Power Transfer*, $t_0 < t < t_1$): Between time t_0 and t_1, all top switches are turned on. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant and the resonant tank current i_{Lr} is larger than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, SR_2 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to nV_o; thus, i_{Lm} linearly increases.

2) Mode 2 (*Energy Circulation*, $t_1 < t < t_2$): At time t_1, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_2 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_1 and t_2.

3) Mode 3 (Dead Time, $t_2 < t < t_3$): At time t_2, all top devices are turned off. The magnetizing inductance current iLm that equals to resonant tank current i_{Lr}, charges and discharges output capacitor Coss of both top and bottom devices. This mode ends when the C_{oss} of all semiconductor devices are fully discharged.

4) Mode 4 (*ZVS Realization*, $t_3 < t < t_4$): At time t_3, the C_{oss} of the bottom devices are fully discharged, and their body diodes start to conduct. ZVS can be achieved when the bottom devices are turned on at this period.

5) Mode 5 (*Power Transfer*, $t_4 < t < t_5$): At time t_4, the bottom devices are turned on and conducting. Transformer leakage inductance L_r and resonant capacitor C_r are in resonant, and the resonant tank current i_{Lr} is smaller than the magnetizing inductor current i_{Lm}. According to the polarity of the transformer, SR_1 is conducting. As a result, the voltage across the magnetizing inductance V_{Lm} equals to $-nV_o$; thus, i_{Lm} linearly decreases.

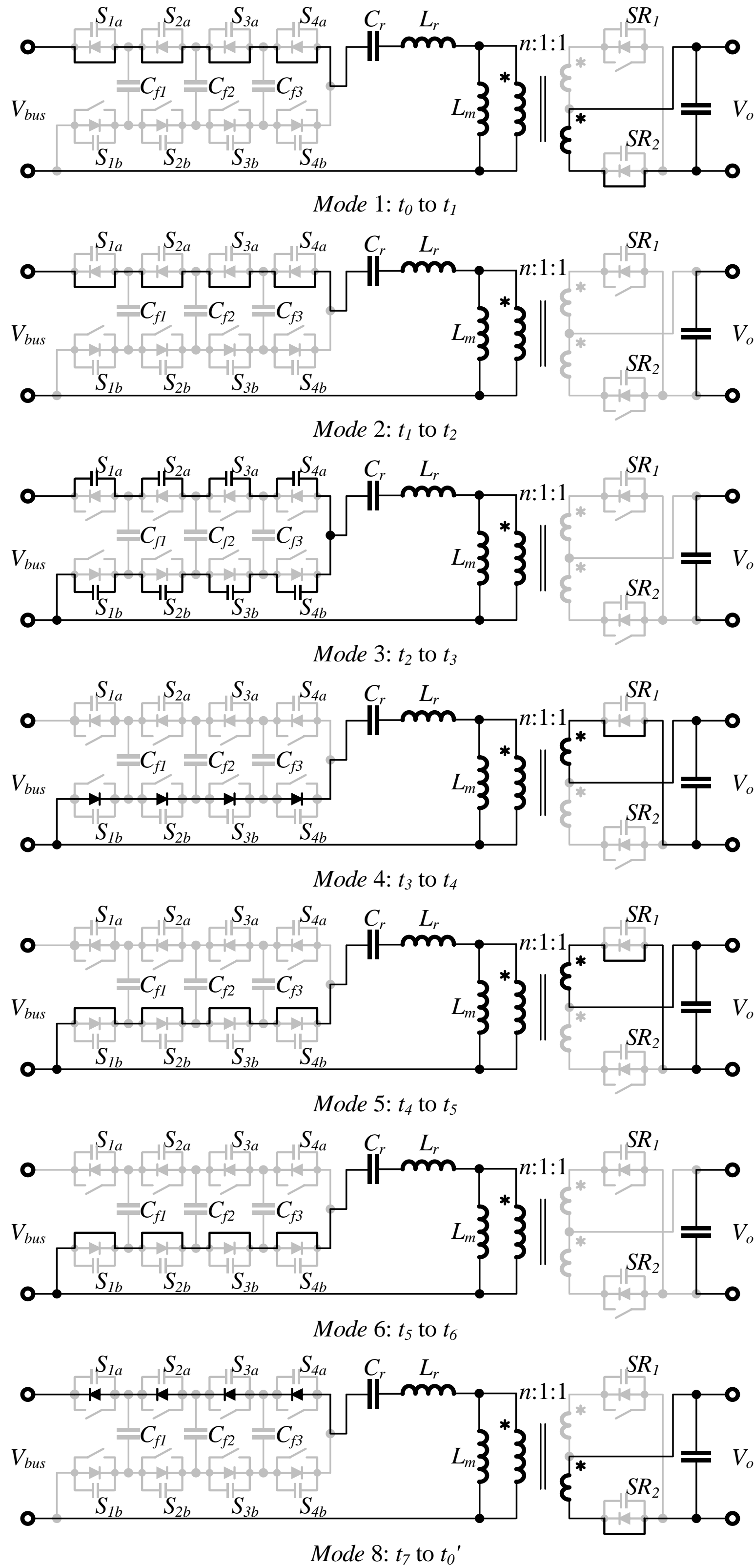


Fig. 5- 27. 4SFCVD-LLC operation states in FBM.

6) Mode 6 (*Energy Circulation*, $t_5 < t < t_6$): At time t_5, i_{Lr} resonates back and equals to i_{Lm}. After that, magnetizing inductance L_m begins to participate in the resonant. Since i_{Lr} equals to i_{Lm}, SR_1 is turned off naturally and ZCS is achieved. The energy stored in L_m is transferred back to C_r between t_5 and t_6.

7) Mode 7 (*Dead Time*, $t_6 < t < t_7$): At time t_6, the bottom devices are turned off. The magnetizing inductance current i_{Lm} that equals to resonant tank current i_{Lr}, charges and discharges output capacitor C_{oss} of the top and bottom devices. This mode ends when the C_{oss} of all semiconductor devices are fully charged and discharged.

8) Mode 8 (*ZVS Realization*, $t_7 < t < t_8$): At time t_7, the C_{oss} of the top devices are fully discharged, and their body diodes start to conduct. ZVS can be achieved when the top devices are turned on at this period.

5.2.3 **Switch cell selection**

The loss simulation results of the active component in HB-LLC, 2SFCVD-LLC and 4SFCVD-LLC with the same circuit design are compared in Fig. 5- 28. As seen, the use of FCVD significantly reduces active component loss. The active component loss in 2SFCVD-LLC is 55 % to 70 % less at the four outputs compared to conventional HB-LLC. The use of 4SFCVD further

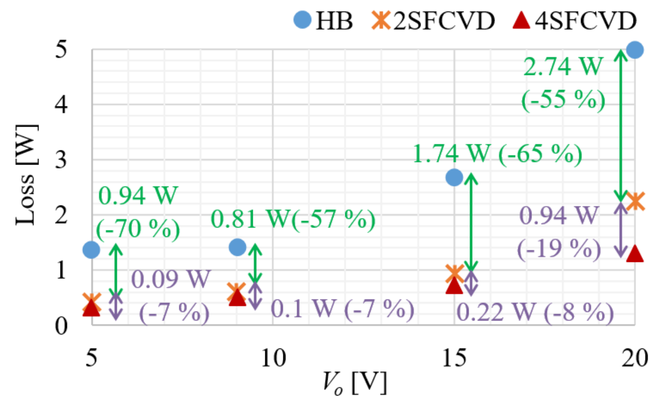


Fig. 5- 28. Active component loss cTable 5- II. Resonant Tank Gain in Two Modesomparison

reduces the active component loss by 7 % to 19 % thanks to its four operation modes to fit the four outputs. However, more semiconductor devices are quired, which complicates the circuit design. In addition, more space will be needed to place the semiconductor devices. Therefore, there is a tradeoff between efficiency, power density and simplicity when selecting the switch cell. Considering above, 2SFCVD is selected in the proposed LLC converter for its simple circuit and small size.

5.3 2SIVD-LLC Resonant Converter Circuit Design

A. Resonant frequency and turns ratio selection

To reduce the voltage across magnetizing inductance and to increase the Q value, transformer turns ratio n should be minimized. The converter resonant tank gain G_t at ARP is given by:

$$G_t = \frac{V_{o,ac}}{V_{in,ac}} \tag{5. 1}$$

Where $V_{o,ac}$ is the resonant tank ac output that is equal to $n \cdot V_o$, and $V_{in,ac}$ is the resonant tank ac input that is equal to $V_{bus}/4$ (HBM) or $V_{bus}/2$ (FBM). To satisfy the minimum gain requirement, the turns ratio $n = n_{min}$ is selected in (5. 2) and the ARP is placed at 5 V/ 3 A nominal point accordingly.

$$n_{min} = \frac{V_{bus}}{4 \cdot V_{o,min}} = 10 \tag{5. 2}$$

Fig. 5- 29 shows the impact of f_r on Q value in the four nominal outputs. The investigation stops at 1MHz because of the frequency modulation capability of the controller. In this estimation, the total inductance is set to 40 μH and the leakage inductance L_r ranges from 4 μH to 10 μH. Although there is not a direct method for selecting the optimum Q value, a moderate value of around 0.5 is commonly selected as a starting point [153]. As shown in Fig. 5- 29, the Q value is much smaller than 0.5 even when L_r reaches 10 μH. To minmize the circulating energy, f_r is and

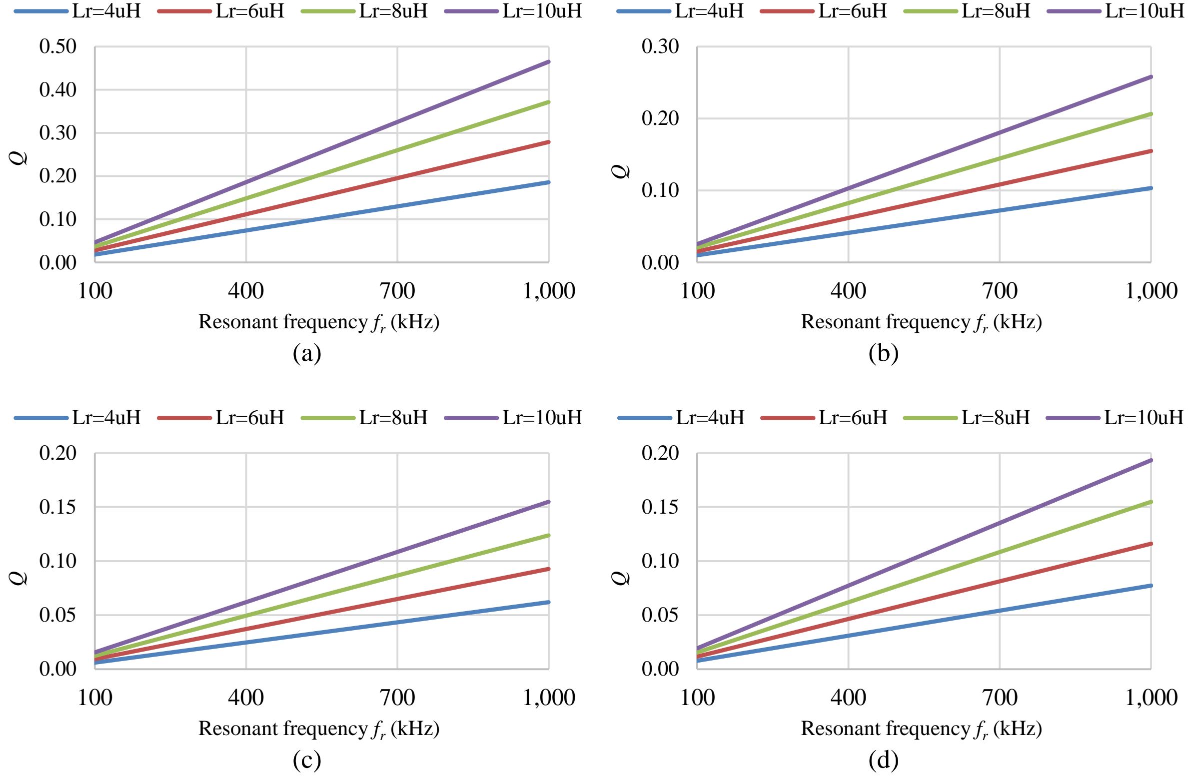


Fig. 5- 29. Q value versus f_r in (a) 5 V/ 3 A, (b) 9 V/ 3 A, (c) 15 V/ 3 A, and (d) 20 V/5 A.

selected as 1 MHz.

B. Operation mode selection

2SFCVD switching bridge offers two operation modes: HBM and FBM. Considering the turns ratio n is selected to be 10, 5 V/ 3 A and 9 V/ 3 A output can only operate at HBM due to the minimum gain requirement, while 15 V/ 3 A and 20 V/ 5 A can operate at either HBM or FBM. The resonant tank gain G_t of 15 V/ 3 A and 20 V/ 5 A outputs are listed in Table 5. 2. The resonant tank gain G_t is calculated in (5. 3) − (5. 7) [153]. As seen, it is affected by quality factor Q, inductance ratio m, and it can be controlled by adjusting the switching frequency f_s.

Table 5. 2. Resonant Tank Gain in Two Modes

Nominal Output	$G_{t@half\text{-}bus}$	$G_{t@full\text{-}bus}$
15 V/ 3 A	3	1.5
20 V/ 5 A	4	2

$$G_t(Q, m, F_x) = \frac{F_x^2(m-1)}{\sqrt{(m \cdot F_x^2 - 1)^2 + F_x^2 \cdot (F_x^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \tag{5. 3}$$

$$m = \frac{L_r + L_m}{L_r} \tag{5. 4}$$

$$Q = \frac{\sqrt{L_r/C_r}}{n^2 R_o} \tag{5. 5}$$

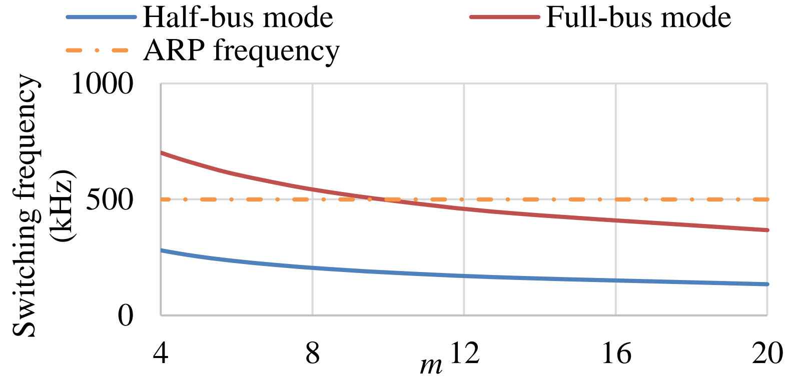
$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5. 6}$$

$$F_{x,HBM} = \frac{2f_s}{f_r}$$
$$F_{x,HBM} = \frac{f_s}{f_r} \tag{5. 7}$$

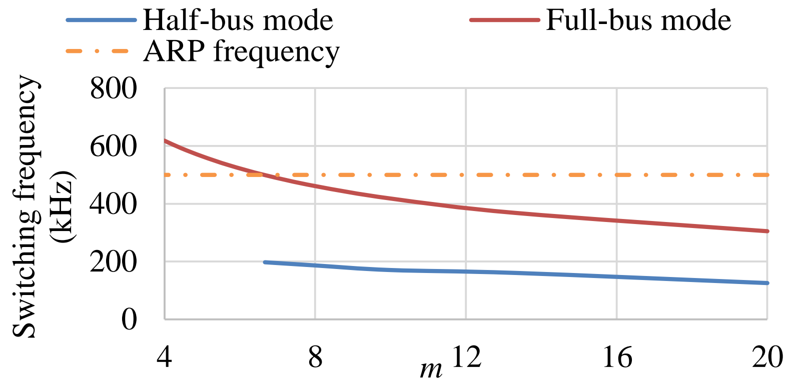
The frequency range comparison between HBM and FBM at 15 V/3 A and 20 V/5 A output are shown in Fig. 5- 30. Since the required G_t doubles in HBM, the switching frequency f_s is far away from the f_{ARP} in both 15 V/3 A and 20 V/5 A. Wide switching frequency range will bring difficulites to control design and EMI filter design. In addition, if HBM was selected, the magnetizing component frequency drops significantly due to the higher G_t, leading to a high voltage-second across the transformer. Therefore, FBM is adopted by both 15 V/3 A and 20 V/5 A output.

C. Inductance ratio m selection

The converter design targets at maximizing the power density and efficiency at four nominal outputs. To ensure high efficicency, ZVS should be provided in full load condition at all nominal outputs. Among them, 5 V/ 3 A is the most difficult case. At this operating point, the LLC converter operates at resonant frequency, and the primary and secondary conduction loss is determined by the magnetizing inductance [159]. Therefore, magnetizing inductance should be maximized to



(a)



(b)

Fig. 5- 30. Frequency range comparison in HBM and FBM at (a) 15 V/ 3 A, and (b) 20 V/ 5 A.

reduce RMS current at primary side and secondary side. To ensure ZVS turn on, the peak magnetizing inductance current should be able to discharge GaN devices output capacitance within deadtime, which gives the maximum magnetizing inductance value to be 30 μH.

Inductance ratio *m* is a parameter that significantly affects converter operation. Its impact on active component loss is shown in Fig. 5- 31. With a given L_m, *m* increases as L_r decreases, which is equivalent to reducing *Q* that causes higher conduction loss. By increasing L_r, conduction loss is well restricted, but the improvement becomes limited when L_r reaches a certain value. It should be noted that oversized L_r should be avoided because it comes with a large voltage across C_r. Considering above, the preferred *m* range is from 5 to 15, by which the voltage across C_r and the active component loss can be restricted to 300 V and 4 %.

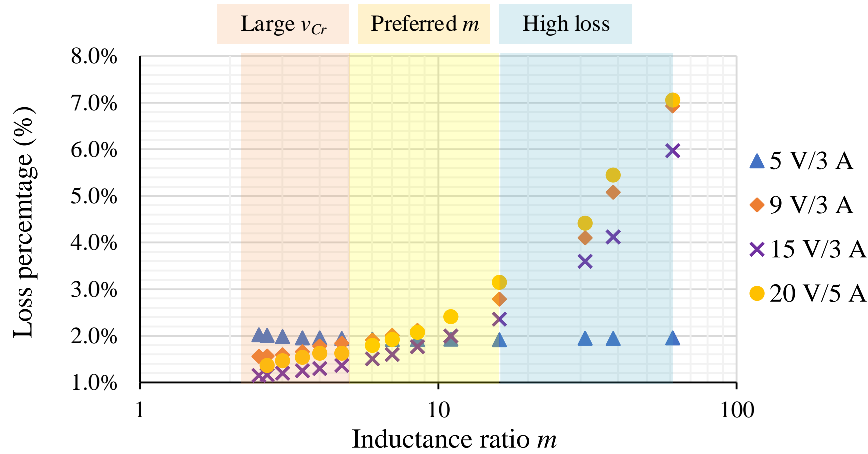


Fig. 5- 31. Loss comparison under different inductance ratio *m* at four nominal outputs.

5.4 Transformer Design

5.4.1 Transformer structure and models

After selecting the turns ratio and the 2SFCVD operation modes, the resonant tank gain G_t ranges from 1 to 2. When the required converter gain increases, switching frequency decreases accordingly. To limit the switching frequency range, sufficient resonant inductance should be provided. Several methods have been proposed to introduce the resonant inductance. In [154], five planar E cores were stacked together for transformer and resonant inductor to achieve sufficient leakage inductance and high efficiency, but the structure is complicated. In [155], the resonant inductor was integrated with matrix transoformer, and part of the resonant inductor magnetic core was removed to improve power density. However, an additional magnetic core was still required to build the resonant inductor. Another method is to utilize a gapped E core to generate flux that is not coupled between primary and secondary windings [156], [157]. In this structure, the transformer leakage inductance is served as the converter resonant inductance and no additional magnetic core is needed. Moreover, the leakage inductance and the magnetizing inductance are controlled by the winding turns and air gaps. As a result, large distance between primary winding

and secondary windings is not required, and most of the interleaving is kept, which reduces the ac winding resistance. The 2D front view of the three-winding transformer with built-in leakage inductance is shown in Fig. 5- 32. By assigning uneven primary-to-secondary turns ratio on two side legs as well as designing the air gaps l_{gs} and l_{gc} properly, leakage flux can be controlled and confined within the center leg.

A. Inductance calculation

The reluctance model for the proposed transformer is shown in Fig. 5- 33, where Φ_1, Φ_2, and Φ_3 represent the flux flowing through left leg, center leg and right leg, respectively. N_{p1}, N_{s11}, and N_{s21} are the turn number of primary winding, secondary winding 1, and secondary winding 2 at the left leg, while N_{p2}, N_{s12}, and N_{s22} are the turn number at the right leg. i_p, i_{s1}, and i_{s2} are the current at the primary winding, the secondary winding 1 and the secondary winding 2, respectively.

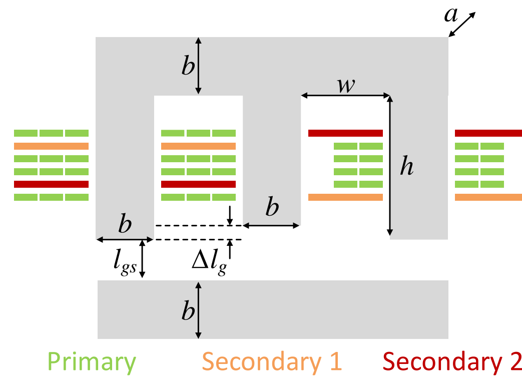


Fig. 5- 32. 2D view of three-winding transformer with integrated leakage inductance

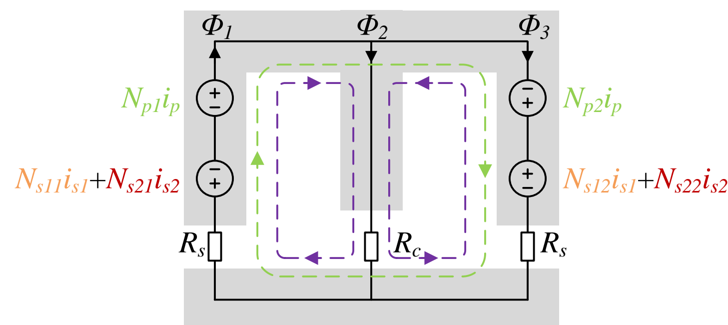


Fig. 5- 33. Relectance model of the transformer in Fig. 5- 32.

To simplify the calculation, two assumpsions are made: 1) the relative permeability of the transformer core is much larger than 1, and thus only the reluctance of the air is considered; 2) Leakage flux in the air is very small and can be ignored. Under these two assumpsions, the flux can be calculated in (5. 8) − (5. 10) with the dimension defined in Fig. 5- 32.

$$R_s = \frac{l_{gs}}{\mu_0 ab}, R_c = \frac{l_{gs} + \Delta l_g}{\mu_0 ab} \tag{5. 8}$$

$$R_a = R_s + \frac{R_s R_c}{R_s + R_c}, R_b = R_a \frac{R_s + R_c}{R_c} \tag{5. 9}$$

$$\begin{aligned} \Phi_1 &= \frac{N_{p1}i_p - (N_{s11}i_{s1} + N_{s21}i_{s2})}{R_a} + \frac{N_{p2}i_p - (N_{s12}i_{s1} + N_{s22}i_{s2})}{R_b} \\ \Phi_3 &= \frac{N_{p1}i_p - (N_{s11}i_{s1} + N_{s21}i_{s2})}{R_b} + \frac{N_{p2}i_p - (N_{s12}i_{s1} + N_{s22}i_{s2})}{R_a} \\ \Phi_2 &= \Phi_1 - \Phi_3 \end{aligned} \tag{5. 10}$$

Based on the reluctance model, the inductance matrix of the three-winding transformer can be derived in (5. 11) − (5. 12), where L_{11}, L_{22}, L_{33} are the self-inductance, and $L_{12} = L_{21}$, $L_{13} = L_{31}$, $L_{23} = L_{32}$ are the multual inductance.

$$\begin{bmatrix} v_{\mathrm{p}} \\ v_{\mathrm{s1}} \\ v_{\mathrm{s2}} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix} \cdot \begin{bmatrix} di_{\mathrm{p}}/dt \\ di_{\mathrm{s1}}/dt \\ di_{\mathrm{s2}}/dt \end{bmatrix} \tag{5. 11}$$

$$\begin{aligned} L_{11} &= N_{p1}\left(\frac{N_{p1}}{R_a} + \frac{N_{p2}}{R_b}\right) + N_{p2}\left(\frac{N_{p1}}{R_b} + \frac{N_{p2}}{R_a}\right) \\ L_{22} &= N_{s11}\left(\frac{N_{s11}}{R_a} + \frac{N_{s12}}{R_b}\right) + N_{s12}\left(\frac{N_{s11}}{R_b} + \frac{N_{s12}}{R_a}\right) \\ L_{33} &= N_{s21}\left(\frac{N_{s21}}{R_a} + \frac{N_{s22}}{R_b}\right) + N_{s22}\left(\frac{N_{s21}}{R_b} + \frac{N_{s22}}{R_a}\right) \\ L_{12} &= N_{s11}\left(\frac{N_{p1}}{R_a} + \frac{N_{p2}}{R_b}\right) + N_{s12}\left(\frac{N_{p1}}{R_b} + \frac{N_{p2}}{R_a}\right) \\ L_{13} &= N_{s21}\left(\frac{N_{p1}}{R_a} + \frac{N_{p2}}{R_b}\right) + N_{s22}\left(\frac{N_{p1}}{R_b} + \frac{N_{p2}}{R_a}\right) \\ L_{23} &= N_{s11}\left(\frac{N_{s21}}{R_a} + \frac{N_{s22}}{R_b}\right) + N_{s12}\left(\frac{N_{s21}}{R_b} + \frac{N_{s22}}{R_a}\right) \end{aligned} \tag{5. 12}$$

To perform identical secondary inductances, (5. 13) should be satisfied, which leads to the

constraints shown in (5. 14).

$$L_{22} = L_{33}$$
$$L_{12} = L_{13} \tag{5. 13}$$

$$N_{s11} = N_{s21}$$
$$N_{s12} = N_{s22} \tag{5. 14}$$

The T-model of a three-winding transformer is shown in Fig. 5- 34. The leakage inductance at primary winding, secondary winding 1 and secondary winding 2 (L_r, L_{sr1}, L_{sr2}), the magnetizing inductance (L_m), and turns ratio (n) can be calculated in (5. 15) based on the inductance matrix [158].

$$L_m = \frac{L_{12} \cdot L_{13}}{L_{23}}$$
$$L_r = L_{11} - L_m$$
$$n = \frac{L_{12}}{L_{23}} = \frac{L_{13}}{L_{23}}$$
$$L_{sr1} = L_{22} - \frac{L_{12}L_{23}}{L_{13}}$$
$$L_{sr2} = L_{33} - \frac{L_{13}L_{23}}{L_{12}} \tag{5. 15}$$

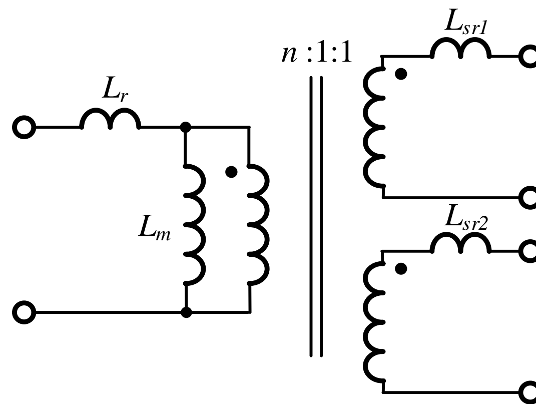


Fig. 5- 34. T-model of a three-winding transformer.

B. Transformer loss model

The transformer core loss is calculated by Steinmetz Equation. For a given EI core shown in Fig. 5- 32, the flux density inside the core can be calculated by (5. 16).

$$B_1 = \frac{\Phi_1}{ab} = (\frac{N_{p1}i_p - N_{s11}i_{s1} - N_{s21}i_{s2}}{R_a} + \frac{N_{p2}i_p - N_{s12}i_{s1} - N_{s22}i_{s2}}{R_b})\frac{1}{ab}$$
$$B_2 = \frac{\Phi_2}{ab} = \frac{(R_a - R_b)[(N_{p1} - N_{p2})i_p - (N_{s11} - N_{s12})i_{s1} - (N_{s21} - N_{s22})i_{s2})]}{R_a R_b}\frac{1}{ab}$$
$$B_3 = \frac{\Phi_3}{ab} = (\frac{N_{p1}i_p - N_{s11}i_{s1} - N_{s21}i_{s2}}{R_b} + \frac{N_{p2}i_p - N_{s12}i_{s1} - N_{s22}i_{s2}}{R_a})\frac{1}{ab} \tag{5. 16}$$

With the given working condition, i_p, i_{s1}, and i_{s2} are considered as known varibles. Therefore, the core loss density can be calculated by:

$$P_{v1} = kf_s^{\alpha}\Delta B_1^{\beta}$$
$$P_{v2} = kf_s^{\alpha}\Delta B_2^{\beta}$$
$$P_{v3} = kf_s^{\alpha}\Delta B_3^{\beta} \tag{5. 17}$$

Where ΔB_1, ΔB_2, ΔB_3 and are the peak-to-peak flux density at the left leg, center leg, and right leg respectively. k, α, β are referring to the constants used in the Steinmetz Equations that are provided by the core manufacturer. ML95S from Hitachi Metals, Ltd is selected as the core material thanks to its low core loss density for the frequency ranging from 400 kHz to 1 MHz under 25 °C to 100 °C. With given core loss density, the transformer core loss can be calculated by (5. 18).

$$P_{core} = ab[(P_{v1} + P_{v3})(h + 3b + 2w) + P_{v2}(h - l_{gs} - \Delta l_g)] \tag{5. 18}$$

To estimate the ac winding loss, 2D transient FEA simulation in Maxwell is performed with the transient current excitation of the primary and secondary sides.

5.4.2 Multi-objective optimization and results

The PCB winding structure limits the total turns of the transformer. As a result, there are only

two options for the transformer turns: N_P: N_{s1}: N_{s2} =10: 1: 1 or N_P: N_{s1}: N_{s2} =20: 2: 2, where N_P, N_{s1}, N_{s2} are the total turn number of the primary winding, the secondary winding 1, and the secondary winding 2, respectively. Since the magnetizing inductance L_m is much smaller than 30 μH when the cross-section area $ab < 100$ mm^2 and the range of inductance ratio m is very limted with N_P: N_{s1}: N_{s2} =10: 1: 1, N_P: N_{s1}: N_{s2} =20: 2: 2 is adopted. Following (5. 14), two winding configurations shown in Fig. 5- 35 are available. In configuration 1, all secondary turns are wound at one side leg, while in configuration 2, each side leg has one of the two turns of each secondary windings.

To maximize power density and reduce core loss, h should be minimized and it is set to (3 mm + l_{gc}), which is sufficient to hold the PCB. From the above analysis, there are 8 variables to be optimized: a, b, w, l_{gs}, Δl_g, N_{p1}, N_{s11}, and N_{s12}. N_{s11} and N_{s12} determine the winding configuration

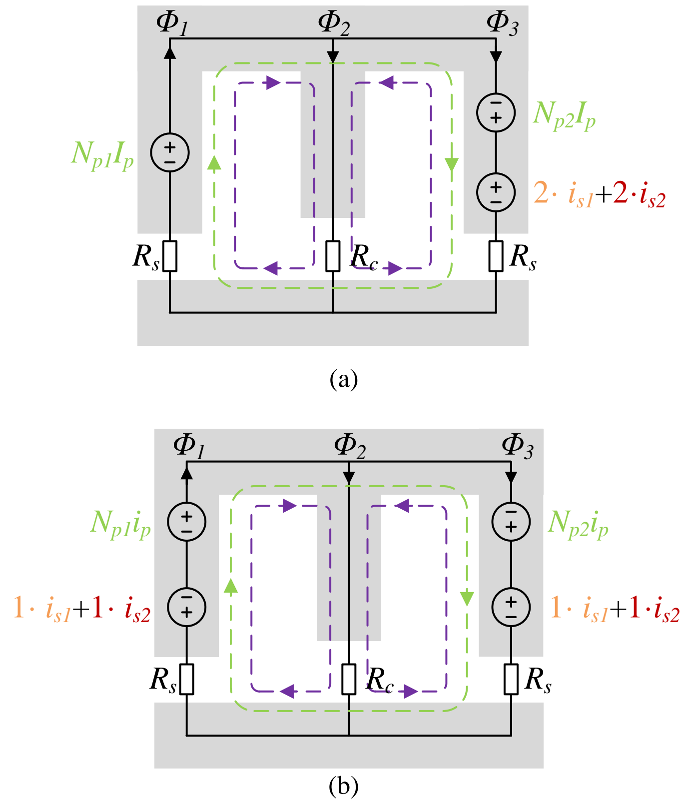


Fig. 5- 35. (a) Configuration 1 and (b) configuration 2.

enumerated in Fig. 5- 35, w adjusts the winding dc resistance, and a, b, l_{gs}, Δl_g, N_{p1} control inductance L_r and L_m. The impact of Δl_g is relatively small compare with other variables. However, oversized or undersized Δl_g will bring difficulties in achieving the desired inductance range. Considering this, Δl_g is selected to be 0.2 mm.

The transformer optimization flow diagram is illustrated in Fig. 5- 36. The first step of the optimization is to import transformer parameters, by which the inductances can be calculated. When the inductance ratio meets $5 \leq m \leq 15$ requirement, simulation will be done to obtain operation parameters (e.g. flux in each leg, current flowing through components, and voltage across components) at four nominal outputs. The parameters are then fed to the converter loss

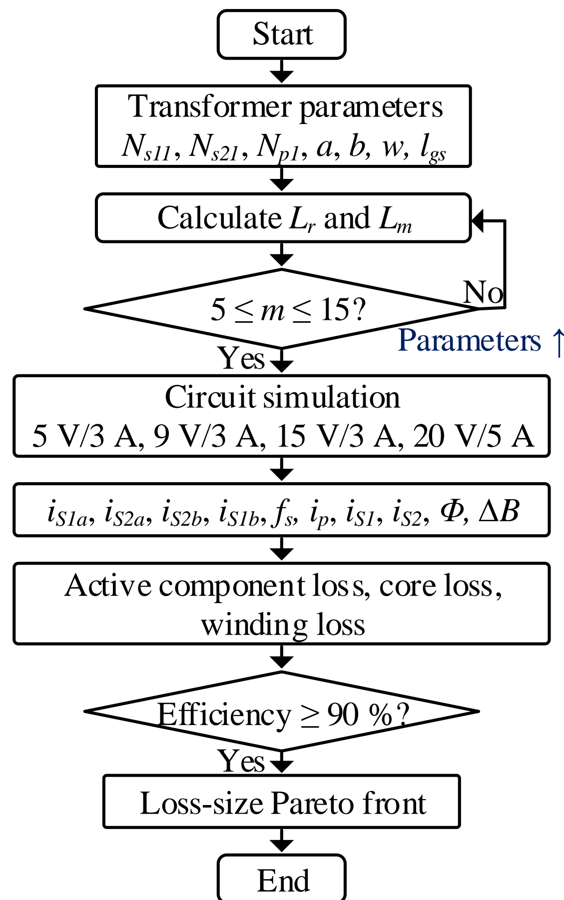


Fig. 5- 36. Transformer optimization procedure.

analysis, where active component loss, transformer core loss and winidng loss are simulated and calculated. After sweeping all possible designs, optimal design can be selected based on the loss-size Pareto front.

The optimization results are shown in Fig. 5- 37. During the optimization, the efficiency of four nominal outputs of all designs are analyzed and only the designs with efficiency $\eta \geq 90$ % in all nominal conditions are considered. The transformer design selection is based on the maximum nominal efficiency and volume. One design point with 93.8 % maximum efficiency and 0.357 inch^3 volume is selected as the final design. The transformer dimension and properties are listed in Table 5. 3.

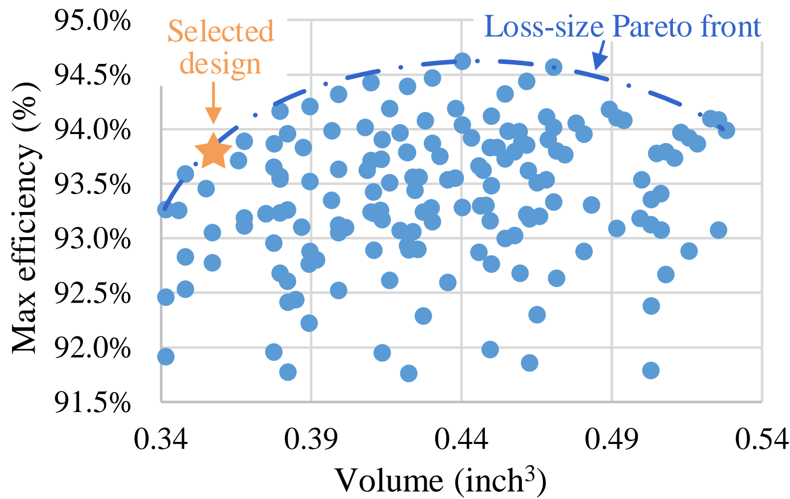


Fig. 5- 37. Optimization result.s and Properties.

Table 5. 3. Transformer Dimensions and Properties

Parameter	**Value**	**Parameter**	**Value**
a	22.5 mm	N_{p1}	2
b	4 mm	$N_{s11}=N_{s21}$	1
w	5 mm	L_r	6.4 μH
l_{gs}	1.2 mm	L_m	29.7 μH

5.4.3 **Comparison between 2SIVD and HB**

The adoption of 2SIVD switching bridge significantly improves converter efficiency. The waveform comparison between 2SFCVD-LLC and HB-LLC at four nominal outputs are depicted in Fig. 5- 38. The current and voltage stress comparison of active and passive components are shown in Table 5. 4 and Table 5. 5, respectively. Thanks to the additional step-down ratio provided by the FCVD switching bridge, the required transformer turns ratio is reduced from 20 to 10, which halves the voltage across magnetizing inductance. As a result, the magnetizing inductance peak current $I_{Lm,p}$, leakage inductance rms current $I_{Lr,rms}$, and secondary side rms current $I_{sr,rms}$ are reduced by 49.1 % ~ 55.2 %, 21.7 % ~ 49.6 %, and 10.9 % ~ 17.7 %, respectively. Moreover, the maximum resonant tank G_t reduces from 4 to 2, and thus the required frequency range is much narrower, which makes the control and EMI filter design easier.

Table 5. 4. Active Component Current and Voltage Stress Comparsion between 2SIVD-LLC and Conventional LLC in Four Nominal Outputs.

	$I_{t,rms}$ (A)			$I_{b,rms}$ (A)			V_{ds} (V)			$I_{sr,rms}$ (A)		
	HB	IVD	Δ%	HB	IVD	Δ%	HB	IVD	Δ%	HB	IVD	Δ%
5 V/ 3 A	0.40	0.22	−43.8	0.40	0.41	3.5	200	100	−50	2.72	2.42	−10.9
9 V/ 3 A	0.99	0.40	−59.5	0.99	0.73	−26.0	200	100	−50	3.52	3.03	−13.9
15 V/ 3 A	1.79	0.83	−53.4	1.79	0.83	−53.4	200	100	−50	3.95	3.10	−21.4
20 V/ 5 A	2.51	1.26	−50.0	2.51	1.26	−50.0	200	100	−50	6.65	5.47	−17.7

Table 5. 5. Passive Component Current and Voltage Stress Comparsion between 2SIVD-LLC and Conventional LLC in Four Nominal Outputs.

	$I_{p,rms}$ (A)			$I_{Lm,pk}$ (A)			$V_{Cr,pk}$ (V)		
	HB	IVD	Δ%	HB	IVD	Δ%	HB	IVD	Δ%
5 V/ 3 A	0.6	0.8	−44.1	0.81	0.41	-49.1	132.8	76.0	-42.8
15 V/ 3 A	2.5	1.2	−52.7	3.74	1.66	−55.7	386.5	207.4	−46.3
20 V/ 5 A	3.6	1.8	−49.6	5.04	2.26	−55.2	527.6	290.3	−45.0

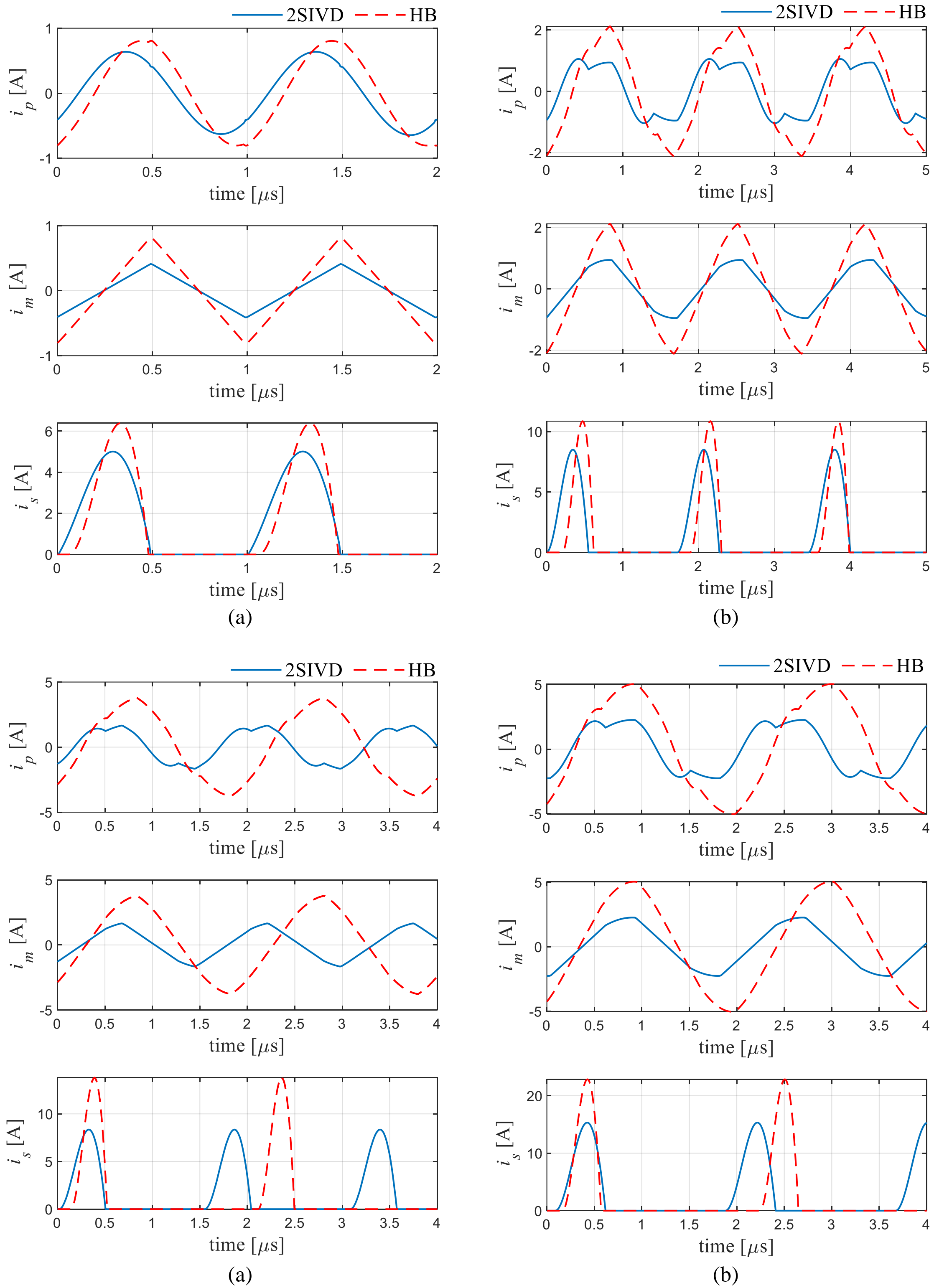


Fig. 5- 38. Simulation waveform comparison between 2SIVD and HB in (a) 5 V/3 A, (b) 9 V/3 A, (c) 15 V/ 3A, and (d) 20 V/ 5

5.5 Hardware assembly and qualification

5.5.1 Component selection and hardware assembly

With the designed transformer properties, the semiconductor devices of FCVD and SR can be selected based on the circuit simulation with SPICE models. The voltage across primary devices is 100 V. GaN devices with more than 150 V voltage rating are considered. Smaller ON-state resitance $R_{ds,on}$, output capacitance C_{oss}, and total gate charge Q_G are preferred to minimized the loss. The highest voltage stress across secondary SR is 40 V. GaN devices with more than 60 V are considered. Since the secondary current is much higher than the primary current, the $R_{ds,on}$ of

Table 5. 6. Device Candidates for FCVD and Simulation Results

	Manufacturer	Part #	V_{ds} (V)	I_{ds} (A)	R_{ds} (mΩ)	Q_G (nF)	C_{oss} (pF)
FCVD	EPC	EPC2012C	200	5	70	1.3	64
	EPC	EPC2019	200	8.5	50	2.5	110
	EPC	EPC2207	200	14	22	5.9	130
SR	EPC	EPC2031	60	48	2.6	21	980
	EPC	EPC2218	100	231	3.2	14	562
	EPC	EPC2053	100	246	3.8	15	642

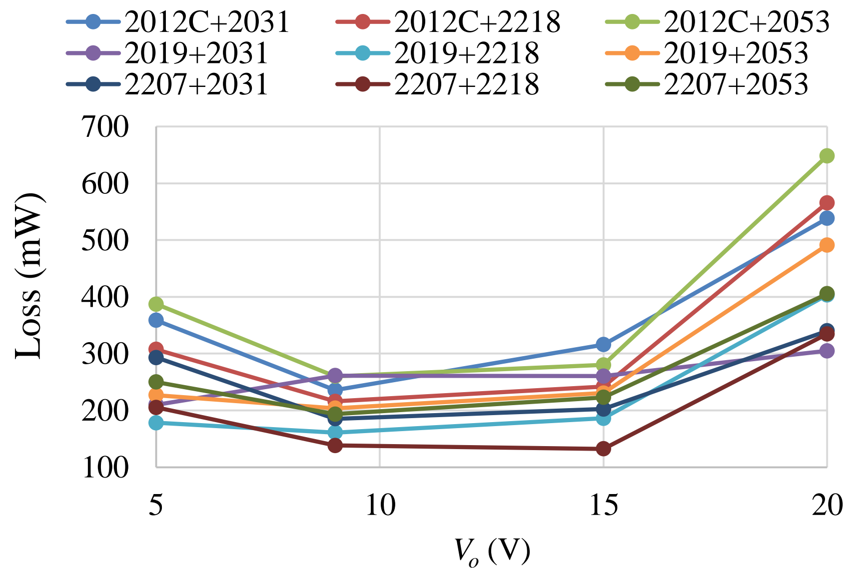


Fig. 5- 39. Active component loss in 5 V/ 3A, 9 V/ 3A, 15 V/ 3A, and 20 V/ 5 A.

SRs should be minimized to reduce conduction loss. When secondary SR is turned off, its output capactor C_{oss} will be charged by parts of the primary current. Therefore, oversized C_{oss} should be avoided. Table 5. 6 enumerates the candidates for the semiconductor devices for FCVD and SR. The simulation results of active component loss are shown in Fig. 5- 39. As seen, EPC2012C and EPC2218 show less overall loss. They are selected as the devices for FCVD and SRs. Two 200 V, half-bridge gate driver, LMG1210 from Texas Instruments, are used to drive the four GaN devices in FCVD for their high CMTI of 100 V/ns. NCP4305 from ON Semiconductor are chosen for the secondary side SR driver thanks to its precise true secondary zero current dectection and high operating frequency.

The test prototype is built. Its top and bottom view are shown in Fig. 5- 40. The length, width, and height of the converter is 43.8 mm (1.72 inch), 40.1 mm (1.58 inch), and 11.2 mm (0.44 inch), respectively. The total volume is 1.196 inch^3, representing a power density 83.6 W/ inch^3 at 100 W, which is more than two time larger than the state-of-the-art power density.

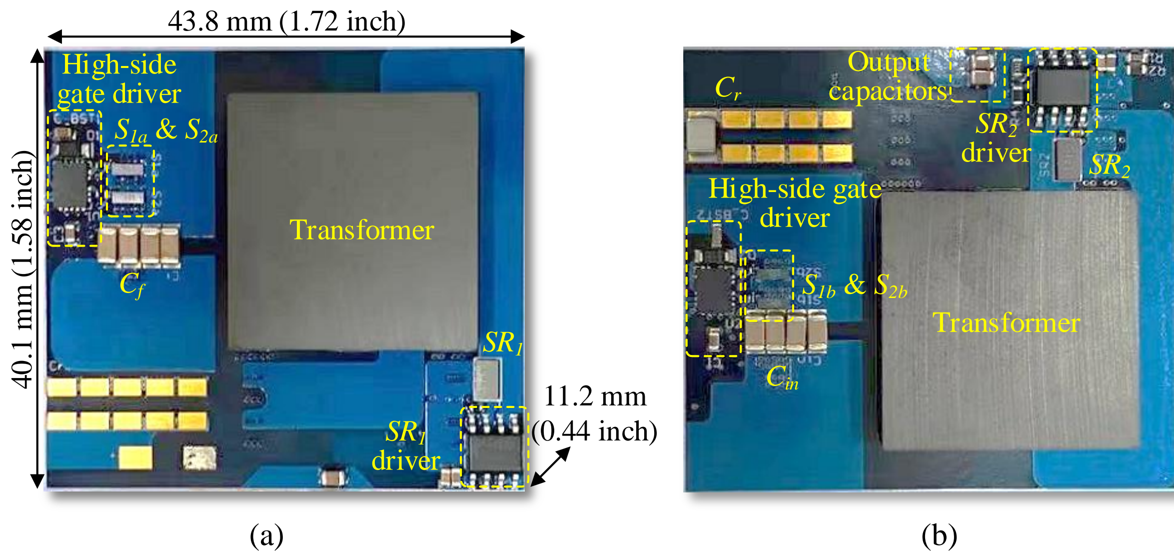
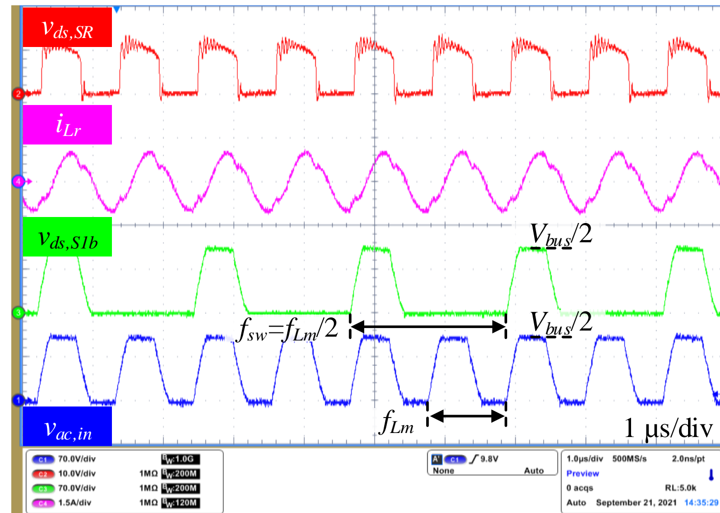


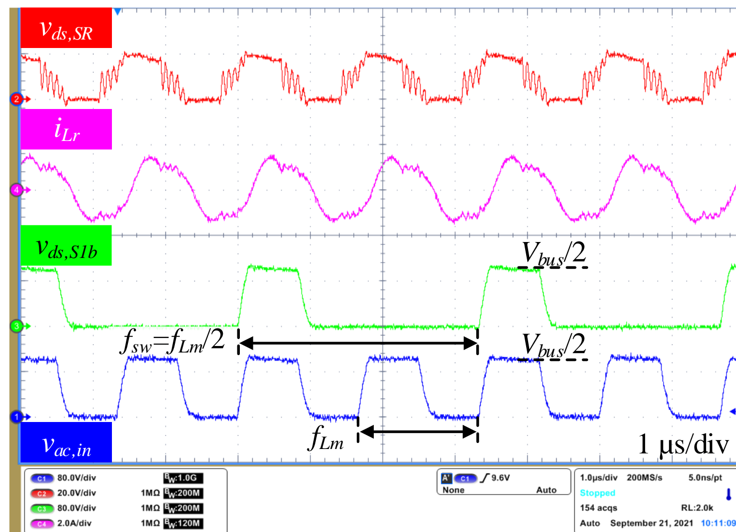
Fig. 5- 40. Top and bottom view of 2SFCVD-LLC converter prototype.

5.5.2 Experimental testing results

The waveforms of the proposed FCVD based LLC resonant converter in half-bus mode are shown in Fig. 5- 41, where $v_{ds,SR}$, i_{Lr}, $v_{ds,S1b}$, $v_{ac,in}$ are the drain-source voltage of the secondary SR, leakage inductance current, drain-source voltage of S_{1b} in FCVD, and the FCVD output voltage, respectively. As seen, the self-balanced flying-capacitor structure halves the drain-source voltage



(a)

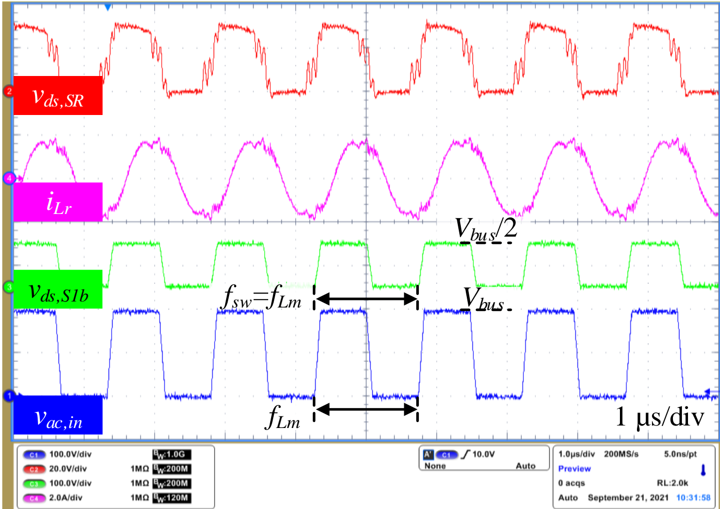


(b)

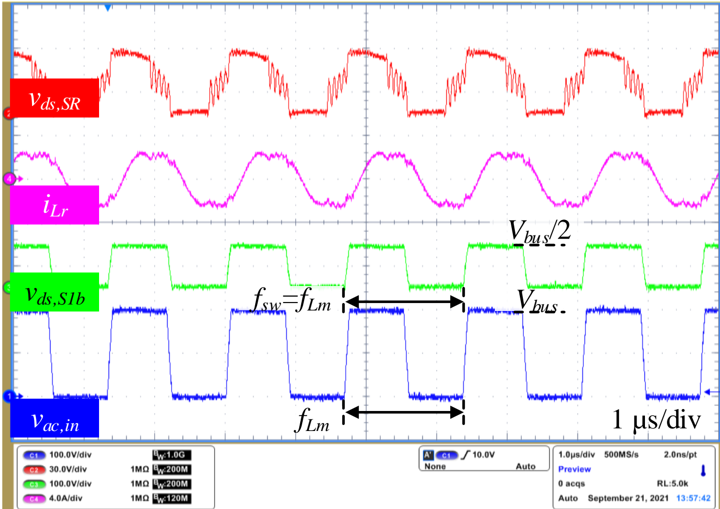
Fig. 5- 41. Experimental waveform in half-bus operating mode at (a) 5 V/3 A and (b) 9 V/3 A.

of semiconductor devices to $V_{bus}/2$. In half-bus mode, the switching frequency of all primary devices are half of the magnetic component frequency. The lower voltage and switching frequency significantly reduce the switching without compromise the magnetic component size.

The waveforms of the proposed FCVD based LLC resonant converter in half-bus mode are shown in Fig. 5- 42. In this operating mode, the flying capacitor is bypassed so that FCVD outputs



(a)



(b)

Fig. 5- 42. Experimental waveform in full-bus operating mode at (a) 15 V/3 A, and (b) 20 V/5 A.

full bus voltage. The switching frequency of the primary devices is equivalent to the magnetic component frequency. Since two GaN devices are connected in series and they withstand the bus voltage together, the voltage stress across each GaN device is still half of the bus voltage.

Fig. 5- 43 shows the efficiency measurement at 5 V/ 3 A, 9 V/ 3 A, 15 V/ 3A, and 20 V/5 A in full load condition. The efficiency at 5 V/ 3 A is lower than the simulation result. The error is caused by the inaccurate model of the GaN devices. In experiment, the output capacitance is larger than the simulation value. Therefore, a larger current is required to discharge C_{oss} during deadtime period. To increase the discharging current, magnetizing inductance has to be reduced, which lowers the efficiency of other operating points.

The loss breakdown of the four nominal outpus are shown in Fig. 5- 44, where FCVD P_{sw}, FCVD P_{con}, P_c, $P_{w,}$, and P_{sr} are the switching loss of primary devices in FCVD, conduction loss of primary devices in FCVD, transformer core loss, transformer winding loss, and SR loss, respectively. Other losses includes terminal loss in FCVD and transformer windings, and the loss in resonant capacitor.

It can be seen that at 5 V/ 3 A, the switching loss of the primary devices dominates. This working condition has the lowest rms current and voltage but a high switching frequency,

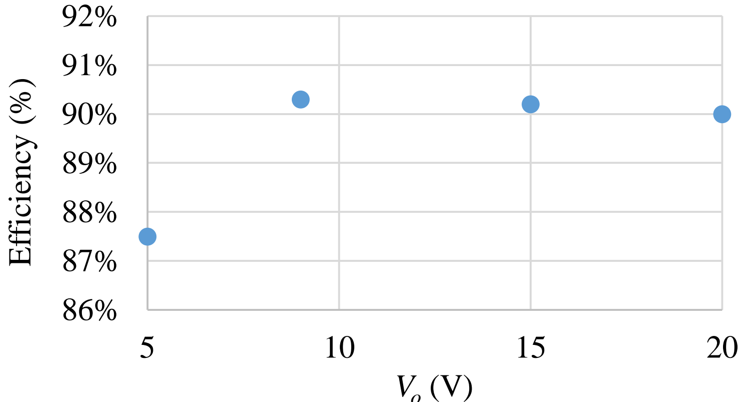


Fig. 5- 43. Efficiency at the 5 V/ 3 A, 9 V/ 3 A, 15 V/ 3A, and 20 V/5 A in full load condition.

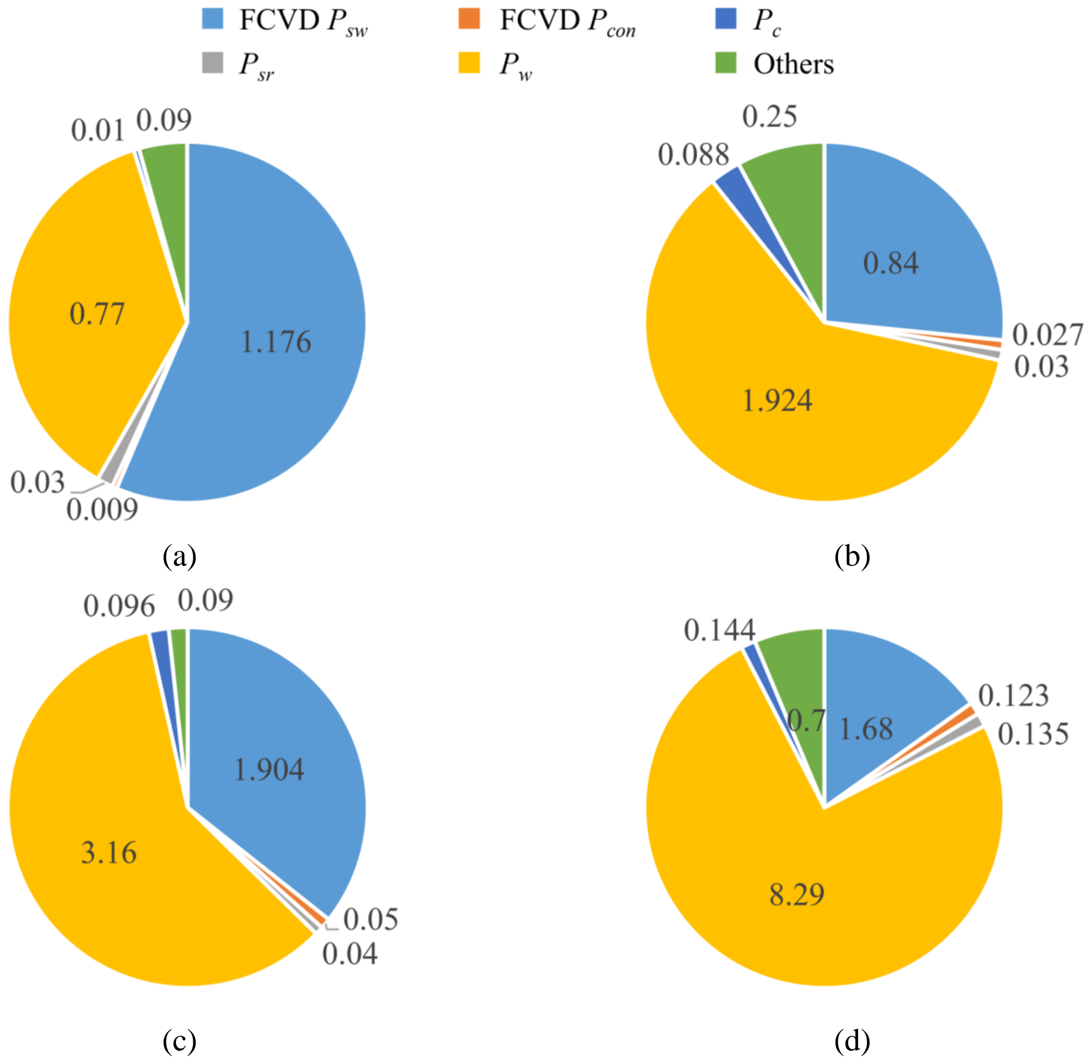


Fig. 5- 44. Loss breakdown of (a) 5 V/ 3 A, (b) 9 V/ 3 A, (c) 15 V/ 3 A, and (d) 20 V/5 A.

therefore, the switching loss of the primary devices takes most of the converter loss. As output voltage and power increase, the transformer winding loss starts to take the leading role. To reduce the winding loss, effort should be made to reduce the dc and ac resistance of the transformer winding. It can be achieved by increasing the width of the PCB winding traces, or lower the operating frequency at the expense of converter power density. The loss of SR are almost negligible even the current is relatively large thanks to the very small $R_{ds,on}$.

5.5.3 Experimental testing results with revised layout

The PCB-winding structure is advantageous over conventional winding, but it also has large interwinding capacitance C_{ps}. The C_{ps} of the prototype (Ver. 1) shown in Fig. 5- 40 is measured as 240 pF. The large C_{ps} is caused by the fully interleaving structure between the primary and the secondary winding, the close distance between two copper layers, and the higher permittivity of fr4 material compared to the air.

The interwinding capacitance is an undesired feature in converter designs, because it generates a coupling path for the common-mode (CM) noise. It will affect ZVS realization, and it is detrimental to signal processing. To suppress the CM current, a larger EMI filter is required.

To restrict the C_{ps} within 100 pF, the transformer winding layout is revised. Compared to the prototype Ver. 1, the degree of the interleaving is reduced by placing all the secondary turns on the external layers. As a result, less layers are needed, and a thicker fr4 layer can be used to increase the distance between the primary and the secondary winding. Moreover, heavier copper weight can be selected thanks to the less copper layers; therefore, the dc resistance in the power loop and transformer winding trace can be reduced by half.

The prototype with revised layout (Ver. 2) is shown in Fig. 5- 45. The measured C_{ps} is successfully reduced to 68 pF. The length, width, and height of the converter is 42.5 mm (1.67 inch), 47.3 mm (1.86 inch), and 11.2 mm (0.44 inch), respectively. The total volume is 1.367 inch^3, representing a power density 73.2 W/ inch^3 at 100 W.

The efficiency comparison between two prototypes are illustrated in Fig. 5- 46. As seen, the efficiency of the Ver. 2 at the four nominal outputs in full load condition is all over 90 %, which meets the efficiency target. Compared to the Ver. 1, the efficiency of the Ver. 2 is improved by 0.33 % to 3.3 % because of its heavier copper weight, and the elimination of the secondary winding

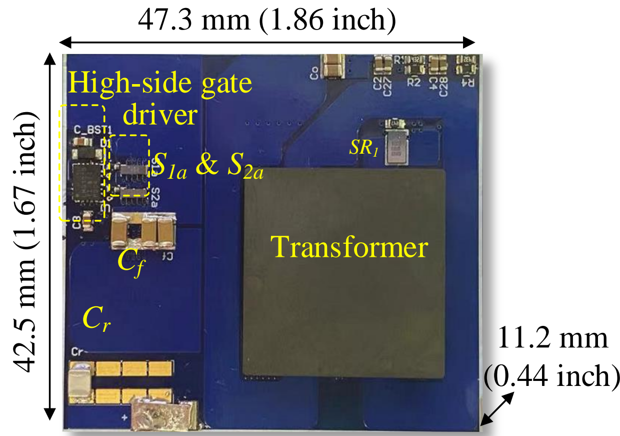


Fig. 5- 45. Top view of small inter-winding capacitor 2SFCVD-LLC converter prototype (Ver. 2).

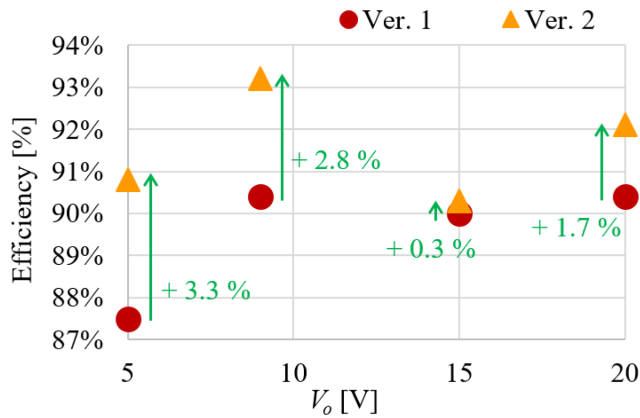


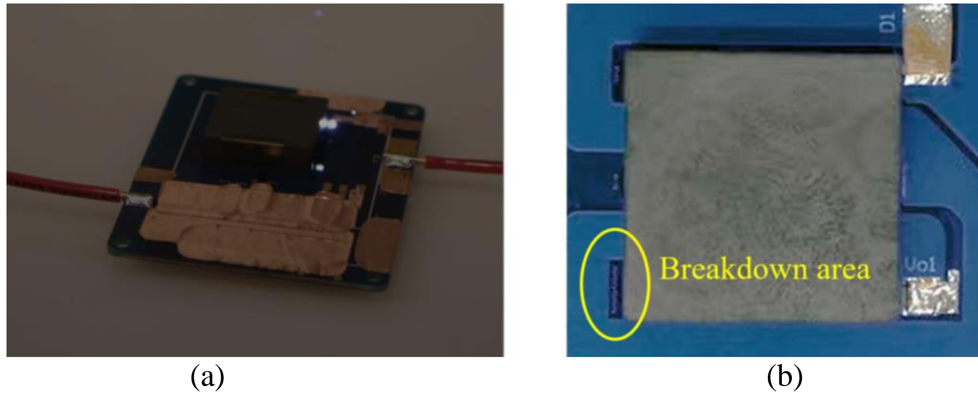
Fig. 5- 46. Efficiency comparision between two prototypes.

vias between the two turns. However, the power density of the Ver. 2 drops by 10.4 W/in^3. More space is required to place the SRs and windings. It represents a tradeoff between efficiency and power density. Considering the reduced size of the EMI filter and the better noise immunity, the reduction in the power density is acceptable.

5.5.4 **Insulation design validation**

Partial discharging (PD) test was conducted in an altitude chamber to ensure that the proposed converter can withstand its target voltage of 200 V without any PD at 10, 000 ft. As shown in Fig. 5- 47 (a), both the primary circuit and secondary circuit are shorted by copper tapes and they are

connected to the high-volrage power supply with wires. High voltage was applied to the primary terminal and the secondary terminal was tied to the ground. 700 Vrms voltage was applied to the converter for more than 30 minutes, showing a sufficient insulation strength. The partial discharging inspection voltage (PDIV) is found to be 800 V at 10,000 ft. The breakdown area is between the vias of the primary winding and the trace of the secondary winding.



(a) (b)

Fig. 5- 47. Breakdown area of (a) converter (b) zoom-in view.

5.6 Summary and Conclusions

This chapter presents the design of a LLC resonant converter for USB-C PD charger in airborne applications. A flying-capacitor based voltage divider (FCVD) switching bridge is proposed to replace the conventional half-bridge switching bridge. The FCVD provides many benefits such as less the voltage stress on semiconductor devices, smaller switching frequency, and smaller transformer turns ratio. PCB-winding based transformer with built-in leakage inductance is adopted to improve power density. Prototypes are built and tested, showing a distince loss reduction in both semiconductor devices and transformer. The final prototype achieves a high efficiency of over 90 % at the four outputs, and a high power density of 73.2 W/in^3, which is almost twice of the state-of-the-art power density.

In conclusion, the insulation strength of the proposed 2SFCVD-LLC converter is sufficient

without using the E-field control methodology. If the converter moves to a higher altitude or higher voltage operation, the E-field control methodology should be applied to the layout design. The bottleneck will be either the GaN devices or transformer windings. Larger board might be needed to increase the insulation strength.

Chapter 6 Conclusions

Due to the increase emphasis on environment concerns, there has been a growing demand for lower fuel consumption in modern transporation applications. Since power electronics is unbiqutous in transporations, the performance of power converters has a significant impact on the transportation's efficiency, size and weight. To further reduce converter loss and size, various integration technologies, including the integration of active components, passive components, and associate components, are widely applied to power converter design.

The transportation applications pose a challenging environment for converter integration. The power converters for transportation applications are often powered directly from the batteries that also feed other loads. When the load changes, undesired transients exist, which requires the converters to work under a wide-input-voltage range. The wide-input-votlage requirement will put more constraints in the converter design. As a result, the design region of acceptance will be very limted, making the converters hard to handle design uncertainties. However, the integration process might bring huge uncertatinty such as material property change. This change is usually hard to predict by either analytical or numerical methods because it depends on the specific material used, geometry, and the fabrication process. This phenomenon can cause converter performance degration or even lead to design failure. Besides, power converters for transportation applicatiosns often work in harsh environment, where its ambient temperature can be up to 125 °C, or the air pressure can be as low as 1.6 PSI. Efforts should be made to improve the efficiency and insulation strength to ensure a safe operation. Moreover, the development of all kinds of consumer electronic devices adds more requirements the charger design. Different output voltage levels such as 5 V, 9 V, 15 V, and 20 V should be provided by the chargers. This wide-output-

voltage range makes the converter design complicated.

To tackle the above integration challenges, a novel PCB-embedded transformer based gate-drive power supply (GDPS) for automotive applications is designed in chapter 2. The proposed GDPS targets at high power density, wide-input-voltage, and high temperature operation. By utilizing the PCB-embedding technology, a high power density of 53.2 W/in^3 is achieved. It also demonstrates that the GaN devices are good candidates for high temperature applications. They function reliably at a high ambient temperature up to 140 °C. However, the PCB material has a poorer thermal dissipation. When the PCB-embedded transformer is used as a substrate carrying the rest of the circuit, it becomes a heat source heating up the air around active components. As a result, the maximum operating temperature reduces.

It is found that the embedding process cause permeability degradation in ferrite materials. To investigate the embedding impact on ferrite materials, several PCB-embedded magnetic boards consisting of four different ferrite cores are fabricated under different stress levels. An experimentally derived correction factor based on worst-case properties is proposed to improve the model accuracy. It avoids design failures by extending the input-voltage range, but the efficiency degradation still exists in this method. Larger cores should be used to improve the efficiency.

To solve the insulation strength degradation in high altitude, a completed design of an enhanced gate driver for SiC based aircborne application is presented in Chapter 4. To achieve high power density, a Paschen curve based insulation coordination is proposed. Instead of using oversized correction factors provided by IEC standards, the proposed method converts the breakdown voltage into breakdown electric field, and thus the required clearance distances are much smaller. However, the closer distance between two conductors increase the parasitic

capacitance. More attention should be paid to the layout design; otherwise, the large parasitic capacitance will distort the information and cause malfunctions in the circuit (e.g. low-pass-filter effect in the integrated current sensor).

Chapter 5 presents the design of a PCB-winding transformer based LLC resonant converter with a wide-output-voltage range. A flying-capacitor based voltage divider (FCVD) switching bridge is proposed to replace the conventional half-bridge or full-bridge switching bridge. It shows a distinct reduction in both active component loss and transformer loss once a 2SFCVD is used, but the loss improvement is not obvious when more switch sets are added. In addition, the high electric field areas in the proposed LLC converter are the area between drain and source pad of primary GaN devices, and the area between the vias of the transformer primary winding and the traces of the secondary winding. Unlike the gate driver proposed in Chapter 4, E-field control methodology is difficult to apply in these areas. The insulation strength of the latter can be improved by using buried vias or increasing the clearance distance, but the insulation strength of the former is limted by the package. Devices with larger packages should be used. Adding more switch set is equivalent to increasing insulation strength, as it reduce the drain-source voltage across devices. However, the efficiency might drop due to the increased device quantity.

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