Chapter 2

Development of Integrated Magnetic Circuits for Low-Voltage, High-Current Applications

A lot of low voltage output applications require relatively high input voltage, e.g., 48 V, 100 V, etc., because high voltage is more efficient in distributing current. To minimize the power loss and protect the output load from possible over-voltage due to the failure of the semiconductor devices, a step-down isolation transformer is required in this type of low voltage power supply design. In the past, a lot of research efforts have been carried out to improve the efficiency of power converters [C1-C28].

There are several popular topologies for low voltage converter applications:

i. Active clamp forward converter with synchronous rectifiers (ACFCSR) [C2, C3, C6, C8, C11, C13, C21].
ii. Half-bridge center-tapped rectifier with synchronous rectifiers (HBCTRSR) and asymmetrical duty cycle control [C9, C19, C20, C23].
iii. Half-bridge current doubler rectifier with synchronous rectifiers (HBCDRSR) and asymmetrical duty cycle control [B16, C7].
iv. Forward current doubler rectifier with synchronous rectifiers (FCDRSR) [B18, C10, C14, C22, C23, C26].

Operated at 50% duty cycle, all of these topologies can provide the optimum secondary waveform for direct self-driven synchronous rectifications.

All of the card-mounted power modules require very high efficiency for low voltage and high current output because of limited spacing for the heat sink. An application example seen in the aircraft power system, Example 2-1, is the initial driving force of the topology development in this work because it has the most stringent requirements in every physical dimension (profile and footprint) and efficiency. In the following discussion, this

example will be used to illustrate the winding design. A brief review will reveal that none of the existing conventional topologies can meet the requirements of high density, low profile, and high efficiency simultaneously. Therefore, new integrated magnetic circuits will be developed. A new magnetic integration procedure is proposed to integrate both cores and windings.

Example 2-1 Application with fixed input and fixed output

- V_{in}=60 V
- V_o=3.3 V
- I_o=30 A
- Output ripple: +/-2% of output voltage
- Eff>=90%
- Profile: 0.18″
- Footprint: 1.5″x1.5″
- Density: >150 W/in^3

2.1. Overview of Existing Low Voltage Converter Topologies

This section investigates the existing low voltage converter topologies and seeks the optimum topology for very low profile, high density, and high efficiency power modules.

2.1.1. Active Clamp Forward Converter with Synchronous Rectifiers (ACFCSR)

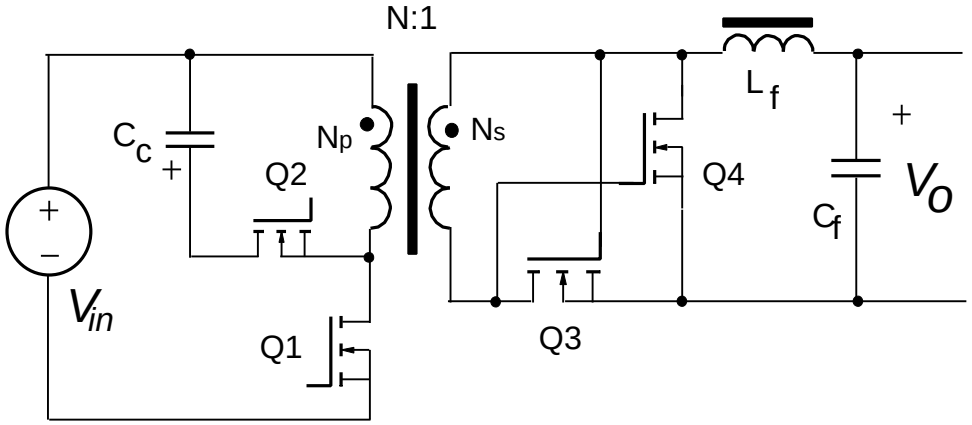
Active clamp reset minimizes the voltage stress on the MOSFETS and provides good driving waveform for direct self-drive synchronous rectifiers. The magnetizing energy and leakage energy are fully recovered. At 50% duty cycle, direct self-driven synchronous rectifiers minimize the conduction loss in the rectifiers. This circuit is capable of dealing with variable input and variable output applications. There are several drawbacks of this circuit, however:

It is difficult to achieve a very low profile transformer design because of the high turns ratio. In Example 2-1, for the single-turn secondary configuration, the transformer needs eight turns of the primary winding and one turn of the secondary winding. As shown in Figure 2-1(b), if each primary winding layer has two turns of primary winding, and a

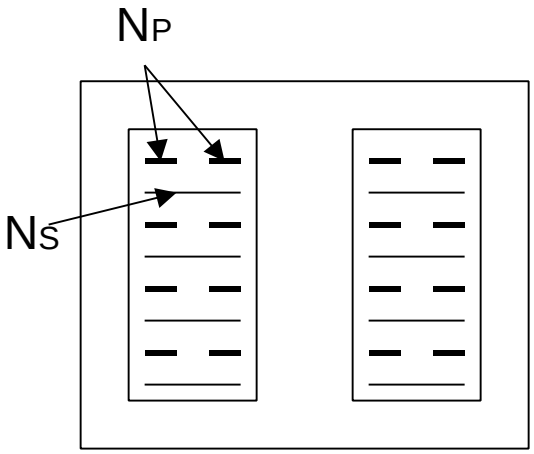
fully interleaved winding structure is adopted, the complete winding will have eight layers.

At 50% duty cycle, a large inductor and a large filter capacitor are required to meet the output ripple specification.

Therefore, ACFCSR is not the best topology for a very low profile, high density power module.



(a)



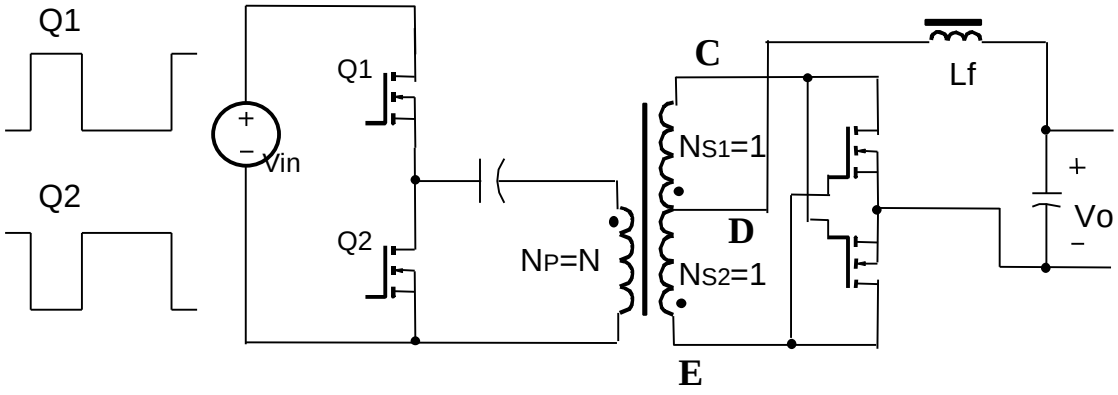
(b)

Figure 2-1 Active clamp forward converter with synchronous rectifier

2.1.2. Half-Bridge Center-Tapped Rectifier with Synchronous Rectifiers (HBCTRSR) and Asymmetrical Duty Cycle Control

HBCTRSR uses a smaller filter inductor than the forward circuit. When the duty cycle is close to 50%, the output ripple current is minimized. The size of the output capacitor can be very small. With asymmetrical duty cycle control, the direct self-driven synchronous rectification can be adopted. The conduction loss in the rectifiers is minimized at 50%

duty cycle. Soft-switching can be easily obtained with asymmetrical duty cycle control. The switching frequency can be increased, resulting in a smaller filter size.



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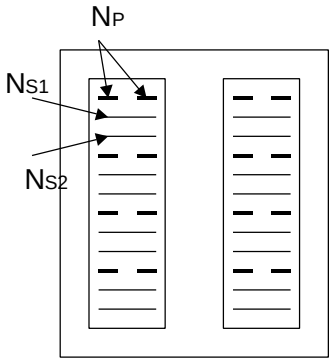

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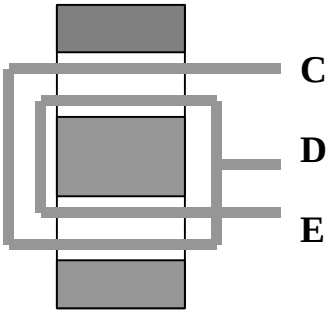


(c)

Figure 2-2 HB center-tapped rectifier with SR

However, it is difficult to achieve a low-profile transformer design because of the additional secondary winding. Since each high current secondary winding usually needs several copper layers in parallel at high switching frequency, the height increase caused by the extra secondary winding is fairly significant. Figure 2-2(b) shows its winding design for Example 2-1. This circuit needs eight turns of primary winding and two single-

turn secondary windings. When the fully interleaved structure is adopted, the complete winding needs 12 layers.

There are three high current terminations from the transformer secondary windings and five high-current interconnections in the circuit. As shown in Figure 2-2(c), arranging three high current terminations might be difficult.

As a result, this topology is not the most promising for very low profile, high density power modules.

2.1.3. Half-bridge Current Doubler Rectifier with Synchronous Rectifiers (HBCDRSR) and Asymmetrical Duty Cycle Control

The current doubler rectifier circuit is very popular for high current applications because it adopts two filter inductors with each inductor sharing half of the output load current. The design of each inductor becomes easier. More importantly, this circuit has ripple current cancellation technique. The ripple currents in two inductors (L1 and L2) are out of phase, and the resulting output ripple current is very small. Consequently, the required filter capacitor size can be small.

Compared to the previous two circuits, HBCDRSR reduces the number of the primary winding turns by half. It is easier, therefore, to design a very low-profile transformer. As shown in Figure 2-3(b), the complete winding design for Example 2-1 contains only four layers.

However, the existence of three magnetic components results in a large footprint and makes layout and packaging design difficult. Three high-current windings and six high-current interconnections reduce the efficiency for high current applications.

Therefore, it is impossible to use this topology to achieve very high power density.

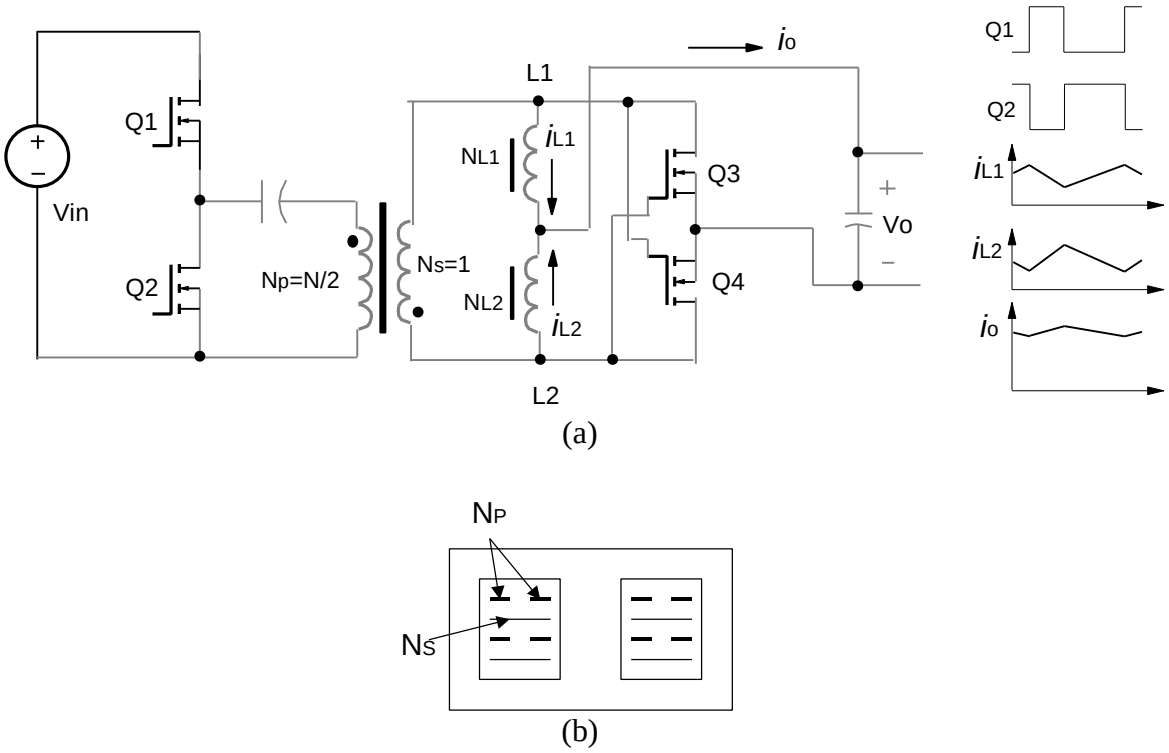


Figure 2-3 HB current doubler rectifier with synchronous rectifier

2.1.4. Prior-Art Half-Bridge Current Doubler Rectifier Circuit With IM Technique

Concluding the discussion, only HBCDRSR is able to achieve very low profile requirement. However, three magnetic components (three cores and four windings) make it impossible to minimize the footprint of the complete power supply. The integrated magnetic technique can be adopted to minimize the overall size of the magnetic devices.

Figure 2-4 shows the prior-art IM technique in HBCDRSR circuit. The overall footprint of the magnetic devices is greatly reduced. However, since there are three windings in each core window, the winding profile is not as low as that of the discrete transformer. As shown in Figure 2-4(b), the complete winding implementation for Example 2-1 consists of six layers. The profile of the winding is higher than that of the transformer in the discrete magnetic circuit. The complete magnetic device with single-turn implementation, as shown in Figure 2-5, still occupies fairly large footprint. It requires six high current interconnections (five for winding terminations, one for layout interconnection), and two layers of copper to implement.

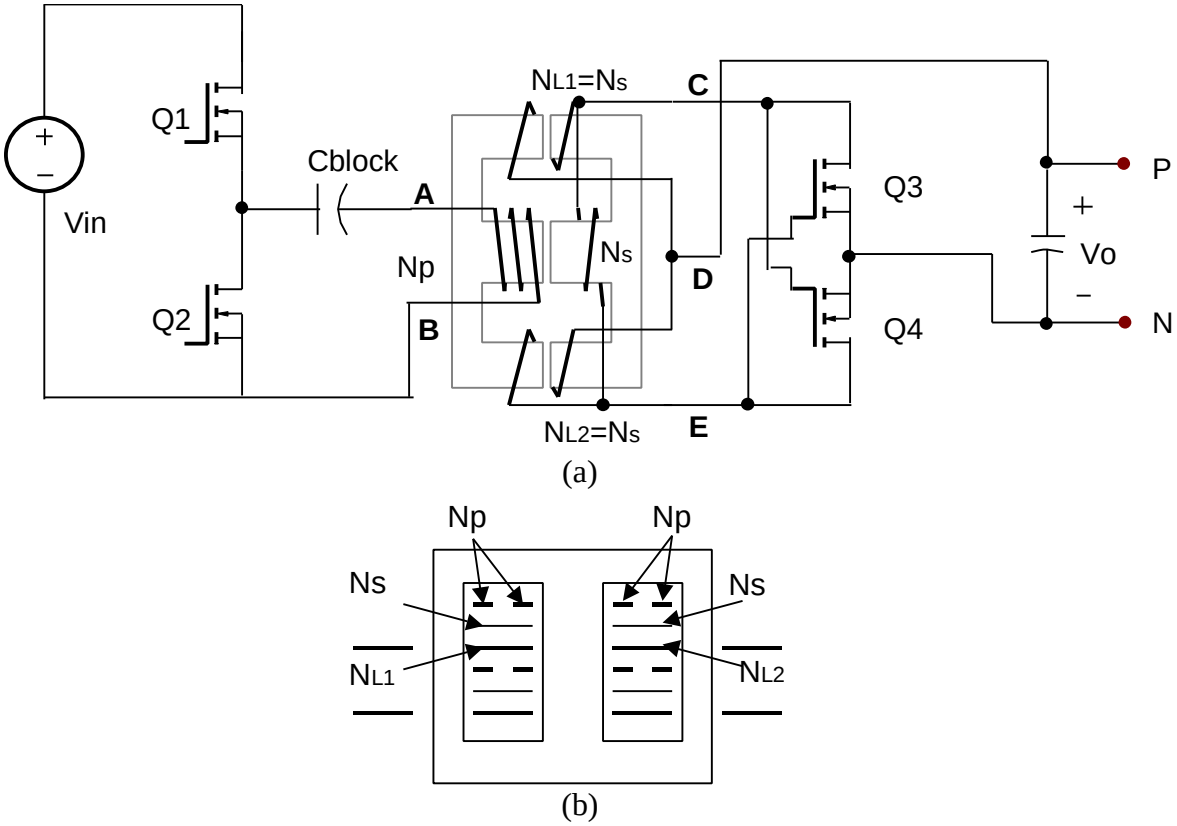


Figure 2-4 HBCDRSR with prior-art integrated magnetics

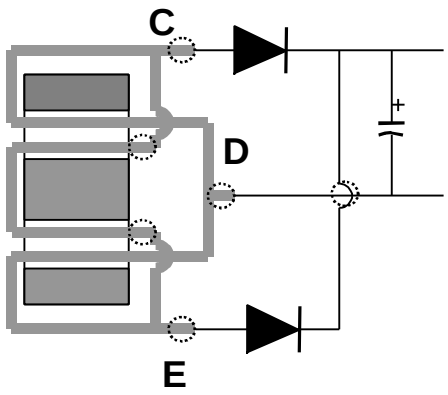


Figure 2-5 Prior-art single-turn secondary layout

2.2. Proposed Integrated Magnetic Circuits

To further reduce the size and height of the IM device in the prior-art IM circuit, a new magnetic integration procedure is proposed to integrate both cores and windings. The derivations of the improved integrated magnetic circuits for the current doubler rectifier

will be used examples to demonstrate the proposed magnetic integration procedure. The developed circuits will prove to be the best topology for very low profile, high density, and high efficiency power supply applications such as in Example 2-1.

2.2.1. Half-Bridge Current Doubler Rectifier Circuit with Improved Integrated Magnetic (HBCDRCI^{2}M)

As shown in Figure 2-6, there are four steps in the proposed magnetic integration procedure. The electrical network with one transformer and two inductors has three ports: ab, cd, and de. At first, as shown on the left side of Figure 2-6(a), i_p is injected to port ab. The inductance looking into port ab can be derived as:

$$L_{ab} = L_m // \left[\left(\frac{N_p}{N_s} \right)^2 L_1 + \left(\frac{N_p}{N_s} \right)^2 L_2 \right]$$

Eq. 2-1

where "//" represents the parallel combination of two impedances.
If L1, L2 and Lm are implemented according to the following equation,

$$L_1 = \frac{N_s^2}{R_1} \qquad L_2 = \frac{N_s^2}{R_2} \qquad L_m = \frac{N_p^2}{R_c}$$

Eq. 2-2

L_{ab} can be expressed in terms of R_1, R_2, and R_c:

$$L_{ab} = \frac{N_p^2}{R_c + R_1 // R_2}$$

Eq. 2-3

To obtain an integrated magnetic structure, L_{ab} should be implemented on a single core with a flux of j_c enclosed by N_p winding. Based on the definition of inductance,

$$L_{ab} = \frac{N_p j_c}{i_p}$$

Eq. 2-4

the relationship between flux and amp-turn can be derived from Eq. 2-3 and Eq. 2-4:

$$j_c = \frac{N_p i_p}{R_c + R_1 // R_2}$$

Eq. 2-5

The corresponding reluctance circuit is shown in the middle of Figure 2-6(a). This reluctance circuit can be further implemented by an E-core structure with Np winding on the center post, as shown on the right side of Figure 2-6(a). Following the same procedure, the reluctance circuits and the physical magnetic structures with port cd or port de seeing current can be derived as shown in Figure 2-6(b) and (c), respectively. By applying the theory of superposition, the complete magnetic structure with all three ports seeing currents can be derived as shown on the right side of Figure 2-6(d). By replacing the discrete current doubler circuit with this integrated magnetic structure, a new HB current doubler rectifier with improved IM is derived, as shown in Figure 2-8.

The definition of reluctances is shown in Figure 2-7. They are expressed as

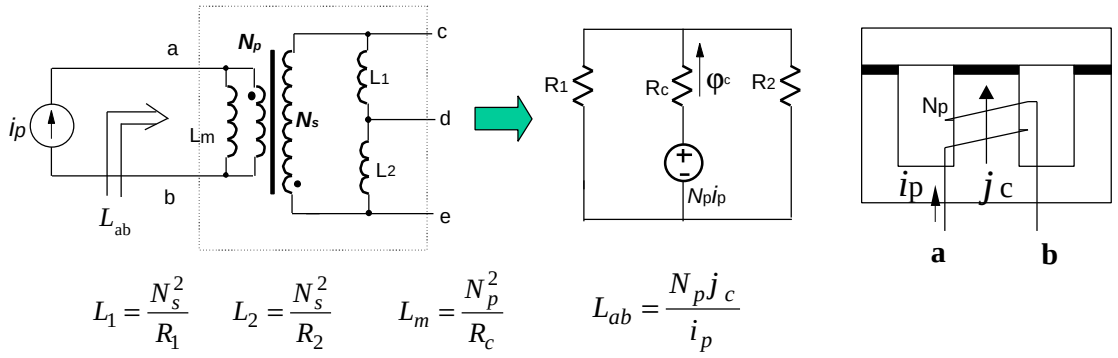
$$R_1 = \frac{l_{1c}}{m_c m_0 A_1} + \frac{l_{1g}}{m_0 A_1} \approx \frac{l_{1g}}{m_0 A_1}$$

$$R_2 = \frac{l_{2c}}{m_c m_0 A_2} + \frac{l_{2g}}{m_0 A_2} \approx \frac{l_{2g}}{m_0 A_2}$$

$$R_c = \frac{l_{cc}}{m_c m_0 A_c} + \frac{l_{cg}}{m_0 A_c} \approx \frac{l_{cg}}{m_0 A_c}$$

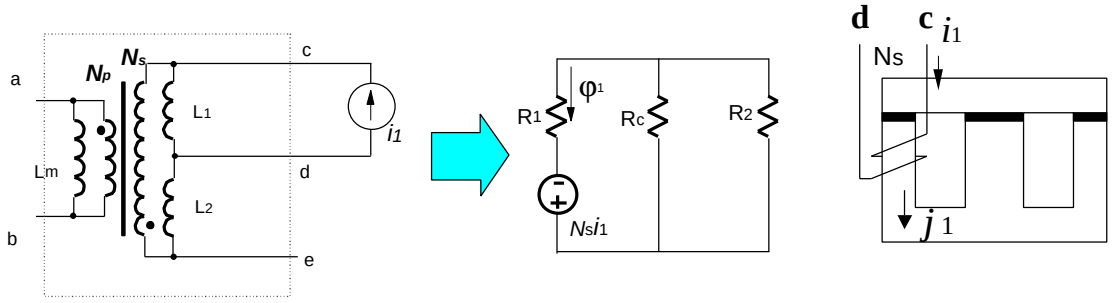
Eq. 2-6

where A_1, A_2, and A_c are the cross-sectional areas of each core leg, l_{1c}, l_{2c} and l_{cc} are the magnetic mean paths of each core leg, l_{1g} l_{2g} and l_{cg} are gapping lengths of each core leg, m_c is the relative permeability of the core and m_0 is the permeability of the air.



$$L_1 = \frac{N_s^2}{R_1} \qquad L_2 = \frac{N_s^2}{R_2} \qquad L_m = \frac{N_p^2}{R_c} \qquad L_{ab} = \frac{N_p j_c}{i_p}$$

(a)



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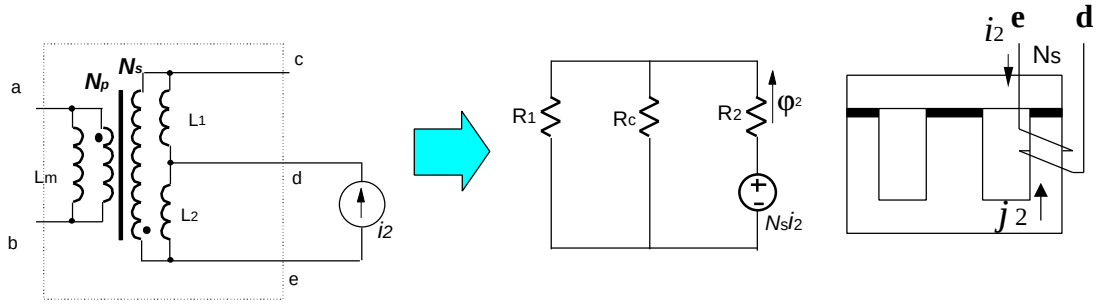

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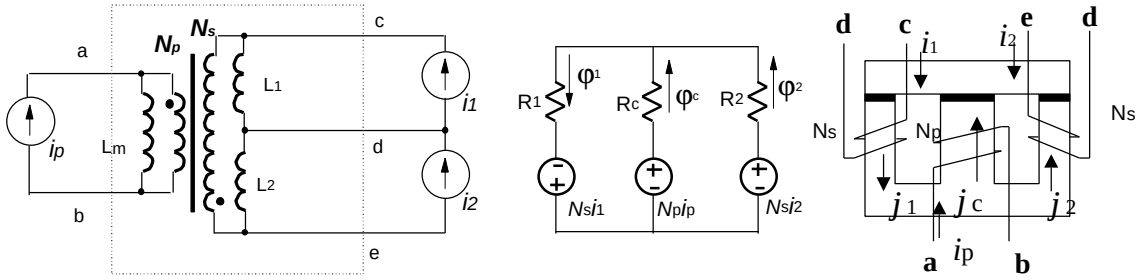


(d)

Figure 2-6 Magnetic integration of current doubler circuit. (a) Step 1: inject a current i_p to port ab and derive an E-core structure with N_p winding on center post, (b) Step 2: inject current i_p into port cd to and derive an E-core structure with N_s on one outer leg, (c) Step 3: inject current i_p into port ed to and derive an E-core structure with N_s on the other outer leg, (d) Step 4: inject currents to all three ports and derive an E-core structure with each core leg hosting one winding by applying superposition theory.

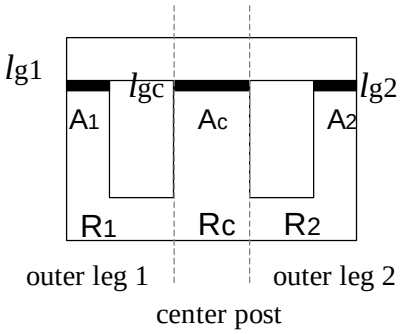
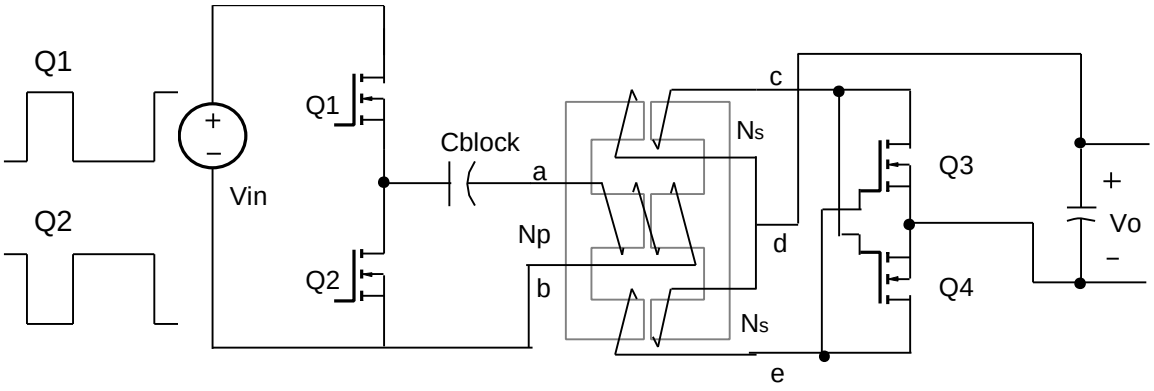
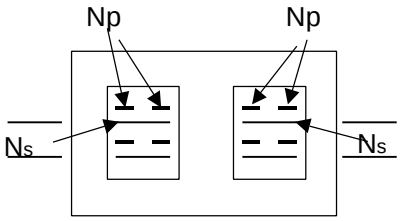


Figure 2-7 Definition of reluctance in E-core



(a)



(b)

Figure 2-8 HB current doubler rectifier circuit with improved IM structure

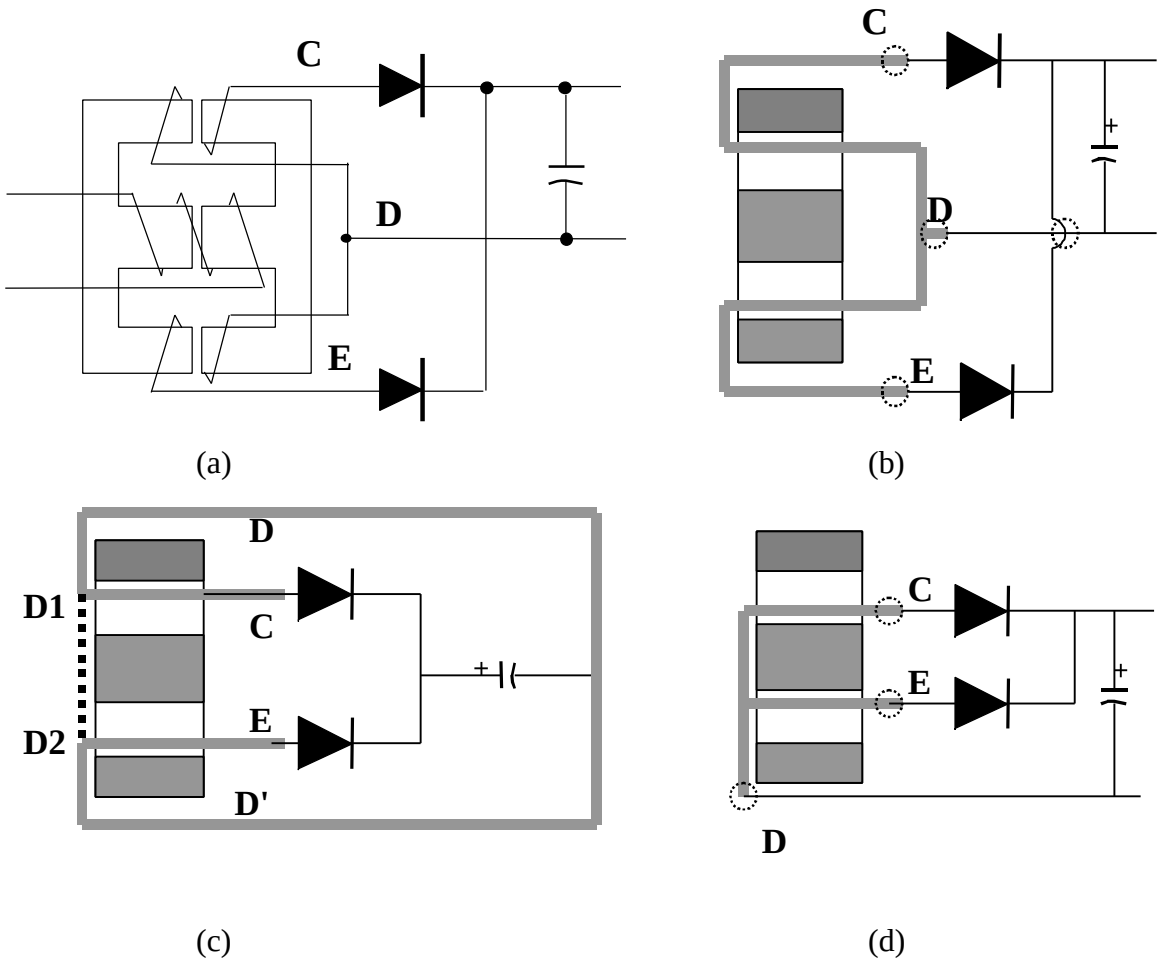


Figure 2-9 Single-turn secondary implementations of the improved IM structure for current doubler rectifier circuit, (a) diagram of improved IM structure, (b) first implementation of single-turn secondary winding, (c) second implementation of single-turn secondary winding, (d) third implementation of single-turn secondary winding (preferred).

Because the reluctance of air gap is usually much higher than that of the magnetic core, the reluctance of each core leg can be approximated by the reluctance of the air gap in the corresponding core leg.

Plugging the derived IM structure into the HB configuration, the HB current doubler rectifier circuit with improved IM (HBCDRCI^{2}M) is obtained, as shown in Figure 2-8. Compared to the prior-art IM current doubler rectifier circuit shown in Figure 2-4(a), the proposed IM circuit eliminates the transformer secondary winding on the center post. As a result, in each core window, there are only two windings. As shown in Figure 2-8(b),

the complete winding implementation for Example 2-1 consists of only four layers. The profile is, therefore, minimized.

The single-turn implementation also proves to be very simple. Figure 2-9 (a) shows the diagram of the proposed IM structure for the current doubler rectifier circuit. Figure 2-9 (a) describes the first implementation of single-turn secondary configuration. If two rectifiers are moved to the other ends of the outer leg windings, the second implementation can be derived as shown in Figure 2-9(c). Since the voltage potentials of D1 and D2 are equal, two nodes D1 and D2 can be shorted, as shown as the dotted line in Figure 2-9(c). By removing the redundant trace in Figure 2-9(c), the third implementation is obtained as shown in Figure 2-9(d). The third implementation features only three interconnections (including winding terminations and layout) and a minimum footprint. It is therefore the preferred implementation. Compared to the single-turn secondary configuration of the prior-art integrated magnetic structure for current doubler rectifier, the proposed technique reduces the number of the high current interconnections and minimizes the footprint of the magnetic devices.

With the asymmetrical duty cycle control, the transformer in the discrete magnetic current doubler rectifier circuit has to be gapped, resulting in a higher primary side conduction loss. In the integrated magnetic circuits, the center post of E-core may not be gapped. This helps lower the primary conduction loss.

Therefore, the proposed circuit has the minimum profile, footprint, and lowest power loss. It is the most promising topology for high density, high efficiency, low voltage, and high current output applications.

The proposed IM circuit originated from the current doubler rectifier circuit and was obtained through a new magnetic integration procedure. As will be analyzed later on, the two outer legs of this magnetic core stored different amount of energy. The design focus is then to prevent the flux saturation in the outer leg with higher energy.

2.2.2. Improved Current Doubler Rectifier Circuit and Its Integrated Magnetics

In the HB current doubler rectifier circuit, the asymmetrical duty cycle control is widely adopted because it minimizes the switching loss and facilitates the gate drive of the synchronous rectifiers. However, the dc gain of this control is parabolic, as shown in Figure 2-10. The dc gain can be expressed as

$$\frac{V_o}{V_{in}} = \frac{N_s}{N_p} D(1-D)$$

Eq. 2-7

Only 0-50% of the duty cycle range can be used. For a wide input range, the duty cycle for high input voltage can be very low because of the parabolic shape of the gain curve. The voltage stress on the secondary side MOSFETs and the current stress on the primary side MOSFETs increase.

The current stresses on the primary side MOSFETs are estimated as

$$I_{Q1,rms} \approx \frac{I_{in}}{\sqrt{D}} \qquad I_{Q2,rms} \approx \frac{I_{in}}{\sqrt{1-D}}$$

Eq. 2-8

where I_{in} is the input dc current.

And the voltage stresses on the secondary side MOSFETs are estimated to be

$$V_{Q3} \approx \frac{V_o}{1-D} \qquad V_{Q4} \approx \frac{V_o}{D}$$

Eq. 2-9

At low duty cycle, the voltage stress on the secondary rectifiers and the current stress on the primary side switches are very unbalanced. The maximum current stress on Q1 and the maximum voltage stress on Q4 increase dramatically as the duty cycle decreases. Therefore, the practical input range of HB current doubler rectifier circuit and its IM versions are relatively narrow.

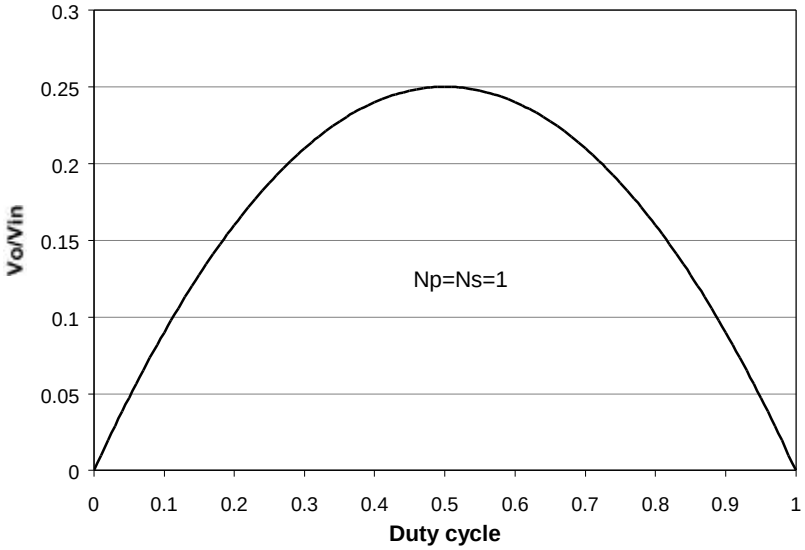


Figure 2-10 DC gain of HB current doubler rectifier circuit

To overcome these limitations, an improved HB current doubler rectifier is proposed as shown in Figure 2-11 [B9, C16]. An additional transformer with a turns ratio of N1:N2 is added. The resulting dc gain of this circuit is expressed as

$$V_{\mathrm{o}} = V_{\mathrm{in}} \frac{N_2}{N_{\mathrm{p}}} \frac{D(1-D)}{1+D(N_2/N_1-1)}$$

Eq. 2-10

Figure 2-12 shows the dc gain of the proposed circuit. It can be seen that the maximum duty cycle range for the output regulation is extended beyond 50%. For N2/N1=2, the maximum available duty cycle is about 60%. Therefore, the duty cycle range can be centered closer to 50%. According to Eq. 2-8 and Eq. 2-9, the voltage stress on Q3 and the current stress on Q1 are reduced.

Table 2-1 Comparison of voltage stress and current stress of HB current doubler rectifier circuit and the porposed circuit. Np=1, Iin=1 A, Vin=16.67~25 V, Vo=5 V

	N1=2, N2=2	N1=1, N2=2
D	0.11-0.18	0.23-0.4
IQ1,max (A)	***3***	***2***
IQ2,max (A)	1.1	1.3
VQ3,max (V)	3	4.2
VQ4,max (V)	***23***	***11***

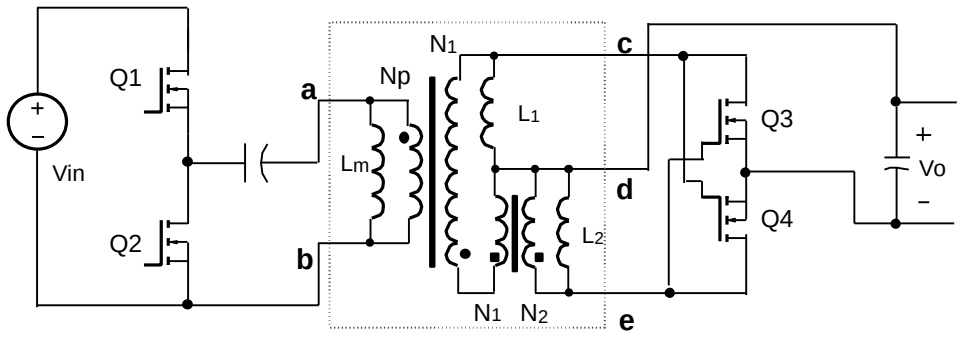


Figure 2-11 HB with improved current doubler rectifier circuit [B9, C16]

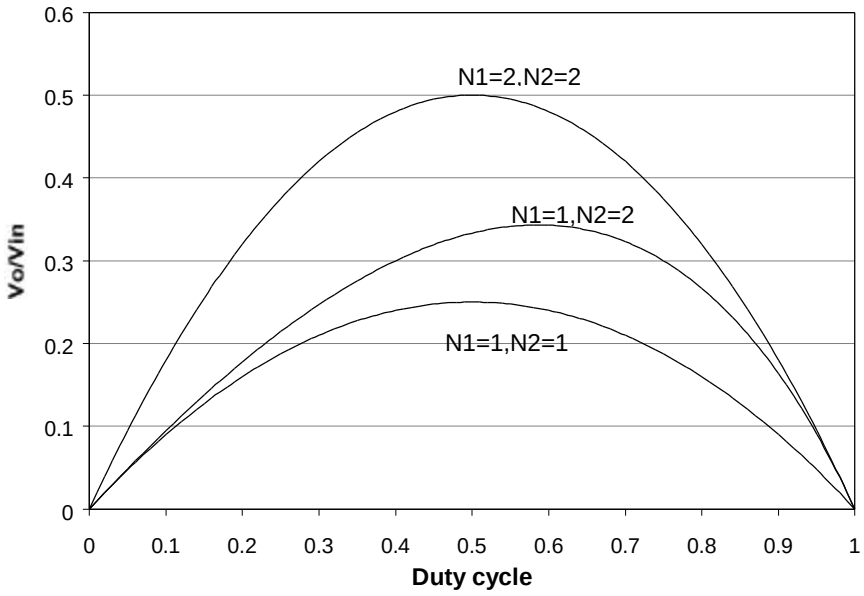


Figure 2-12 DC gain of HB improved current doubler rectifier circuit (Np=1)

To derive the integrated magnetic implementation of the proposed circuit, the same procedure discussed in Figure 2-6 is applied. As shown in Figure 2-13(a), a current source is injected into the port ab of the framed magnetic network, as shown on the left side of Figure 2-13(a). The inductance looking into port ab is derived as

$$L_{ab} = L_m \,//\left[\left(\frac{N_p}{N_1}\right)^2 L_1 + \left(\frac{N_p}{N_1}\right)^2 L_2\right].$$

Eq. 2-11

If L1, L2 and Lm are realized by the following equations:

$$L_1 = \frac{N_1^2}{R_1} \qquad L_2 = \frac{N_2^2}{R_2} \qquad L_m = \frac{N_p^2}{R_c},$$

Eq. 2-12

and L_{ab} is implemented on a single core with flux, j_c,

$$L_{ab} = \frac{N_p j_c}{i_p}.$$

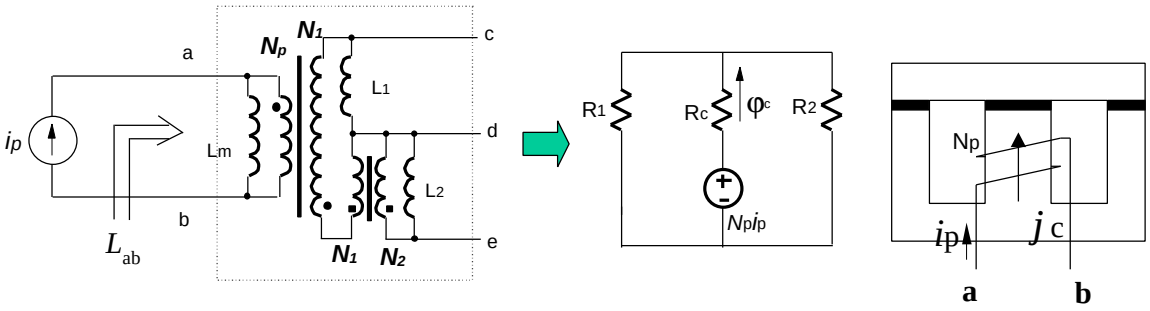
Eq. 2-13

The following relationship can be derived by combining Eq. 2-11, Eq. 2-12, and Eq. 2-13,

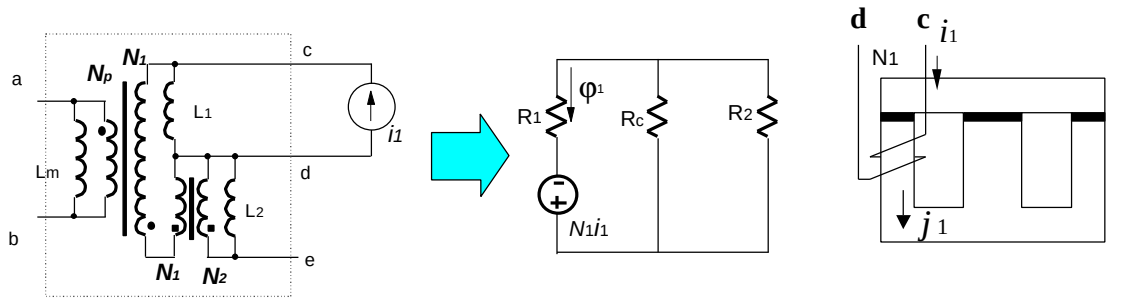
$$j_c = \frac{N_p i_p}{R_c + R_1 // R_2}.$$

Eq. 2-14

From this equation, the equivalent reluctance circuit can be derived as shown in the middle of Figure 2-13(a). The physical implementation of this reluctance circuit is shown on the right side of Figure 2-13(a). Similarly, by injecting the current source into Ports cd and de, as shown in Figure 2-13(b) and (c), the respective reluctance circuit models and physical implementations can be derived. According to the superposition theory, the complete reluctance circuit with all three ports seeing current sources is obtained in the middle of Figure 2-13(d). From this reluctance circuit, the physical magnetic structure, shown on the right side of Figure 2-13(d), can be derived.



(a)



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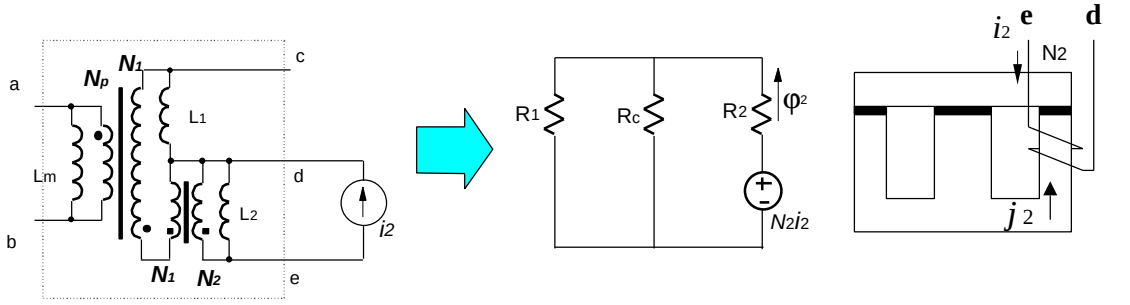

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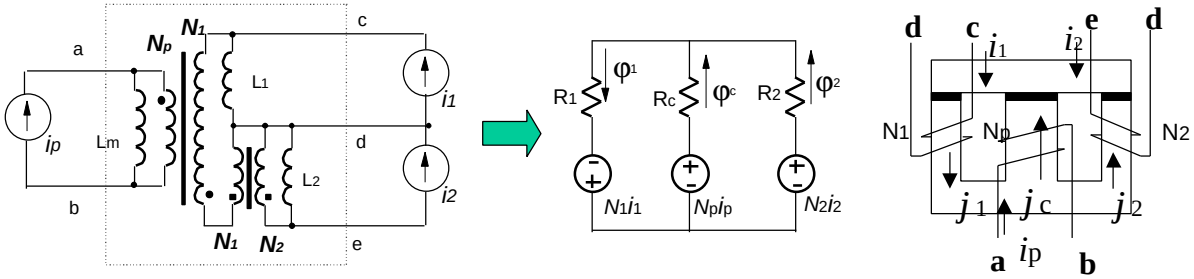


(d)

Figure 2-13 Derivation of new integrated magnetic structure (a) inject current source into port ab, (b) inject current into port cd, (c) inject current into port de, (d) new integrated magnetic structure via superposition theory [C16]

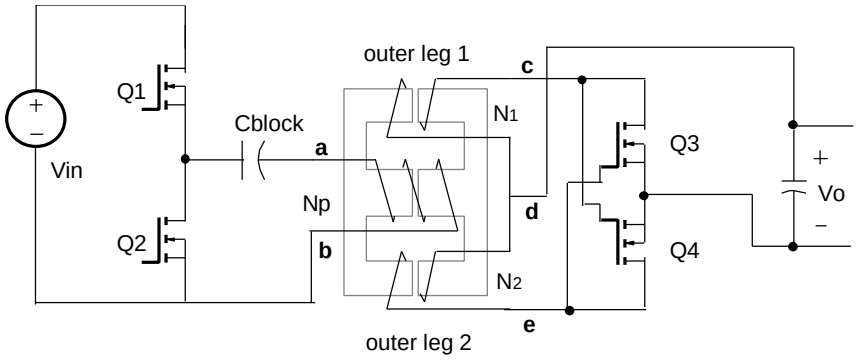
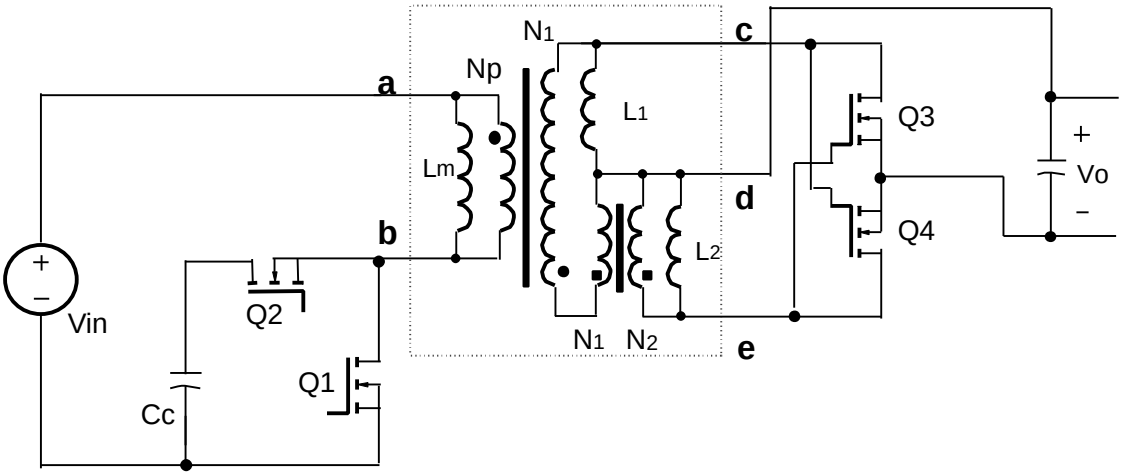


Figure 2-14 Proposed integrated magnetic circuit for HB with improved current doubler rectifier circuit

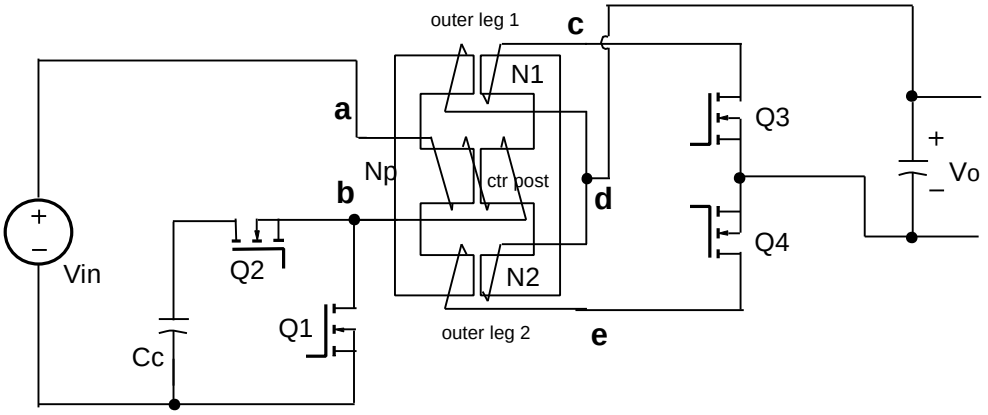
This diagram of the magnetic structure for the improved current doubler rectifier circuit is the same as that shown in Figure 2-8: a three-leg core with one winding on each core leg. The additional transformer N1:N2 in the improved current doubler rectifier circuit can be implemented by adjusting the turns ratio of two outer leg windings. Plugging the derived integrated magnetic structure into the original circuit gives the final circuit in Figure 2-14. In later discussions, the proposed circuit will be referred to as the Half-Bridge Circuit with Improved Integrated Magnetics (HBI^2M).

2.2.3. Other Converters with Improved Integrated Magnetics

By rearranging the primary side circuit of the proposed HBI^2M circuit, a "forward" type circuit was proposed, as shown in Figure 2-15. Like the previous integrated magnetic circuit, this integrated magnetic structure allows a different number of winding turns on two outer legs. The resulting dc gains are shown in Figure 2-16. When N1=N2, the conversion gain is the same as that of forward converter. Consequently, this circuit is named *forward* circuit with improved integrated magnetics (FI^2M). When N2 and N1 are different, the converter topology is electrically different from the regular forward circuit, as proved by the transfer functions shown in Figure 2-16 [B20]. It can also seen from Figure 2-16 that the input or output regulation range of FI^2M can be wider than the regular forward circuit for the same duty cycle range if N2>N1. And the voltage stress on both primary side MOSFETs and secondary side MOSFETs can be reduced.



(a)



(b)

Figure 2-15 Circuit diagram of proposed FI^{2}M, (a) electrical circuit diagram, (b) integrated magnetic implementation

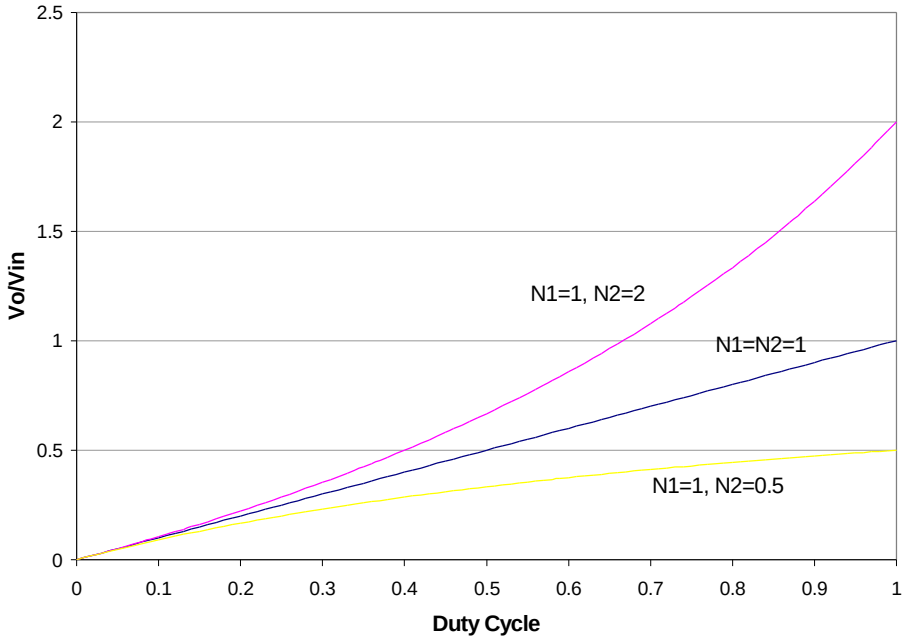


Figure 2-16 DC gain of FI^{2}M

Figure 2-17 shows two more examples of circuit topologies with the proposed IM structures. Full bridge type circuits are generally intended for high input voltage and high power application.

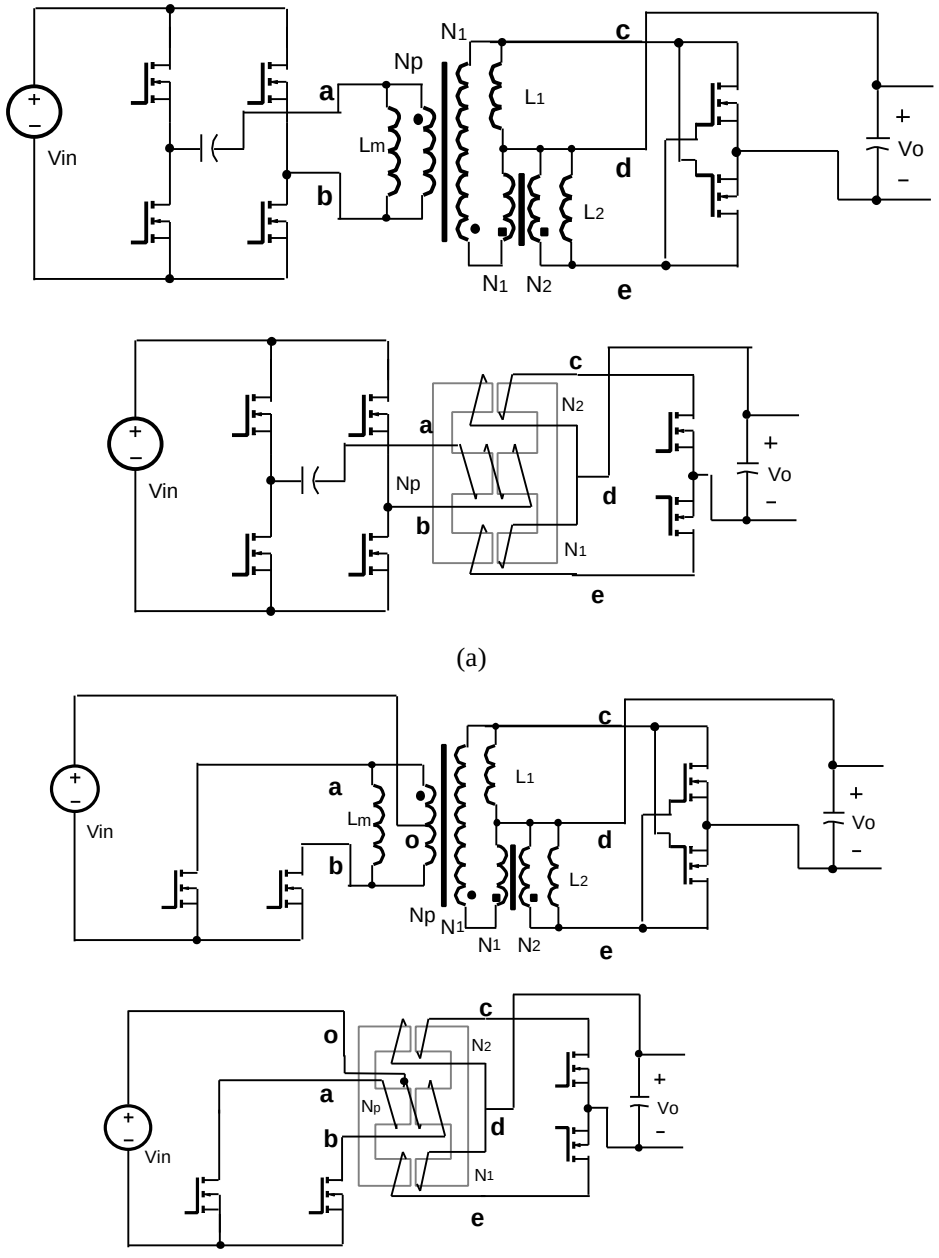


Figure 2-17 Other Circuit Topologies with Proposed Integrated Magnetic Structure

2.3. Summary of Proposed Magnetic Integration Procedure

Since the prior art IM structures [B1, B2, B4, B5, B16, B17] attempt to maintain the winding voltage and current unchanged, the number of the windings cannot be reduced.

As presented in the previous sections, the objective of the proposed magnetic integration procedure is to keep the *port voltage* and *port current* of the overall magnetic network unchanged, rather than winding voltage and current of the individual magnetic component. The goal is to replace the lumped magnetic network by an integrated magnetic structure. Therefore, it is possible to eliminate some individual windings in the final integrated magnetic structure and keep the port voltage and current unchanged. By injecting current source into one port of the magnetic network, the inductance looking into this port with the other port open circuited can be derived. Because the magnetic integration will not change the port property, the port inductance should also remain unchanged. The final integrated magnetic structure will utilize a single core to implement this port inductance. Therefore, a relationship between the flux in the integrated magnetic structure and the port current can be derived in terms of the reluctances. The reluctance circuit can be obtained. The physical magnetic structure is then obtained from the reluctance circuit.

For a magnetic network with m ports, it requires m+1 steps to complete magnetic integration.

Step 1: a current source is injected to Port 1 with other ports open. The inductance into this port is then expressed as the function of the parameters of each magnetic component (winding turns, reluctances, etc.). Because this inductance must be implemented on a single magnetic core (requirement of the magnetic integration), the flux coupled by this reluctance can expressed as the function of *port current*, and the parameters of each magnetic component (winding turns, reluctances, etc.). The corresponding magnetic reluctance circuit and the physical implementation are then derived from the relationship of amp-turns, fluxes, and reluctances.

Step 2-m: repeat Step 1 for the rest m-1 ports.

Step m+1: By applying the super-position theory, the final magnetic structure can be derived.